
Micro Linear
Applications Handbook

INTRODUCTION

Micro Linear Corporation, headquartered in San Jose, California, designs, develops and markets high performance analog and mixed signal integrated circuits for a broad range of applications within the communications, computer and industrial markets. By combining its analog expertise with a unique development methodology, Micro Linear offers to its customers highly-integrated system-level solutions that add value and reduce systems costs.

This applications handbook contains application notes and briefs based on standard products which are focused on the following application areas:

Local Area Networks

Telecommunications

Hard Disk Drives

Magnetic Tape Drives

Magneto-Optical Drives

Motor Controls

Switch Mode Power Supplies

DC to DC Converters

Fluorescent Lamp Ballasts

Data Acquisition Systems

Bus Products

Most of the application notes found in this book are based on actual designs. These designs originated as evaluation kits for the specific parts. Micro Linear Corporation provides evaluation kits for most new devices to demonstrate the features of the part and speed up the evaluation of the part by customers. The kit includes a fully assembled PC board with all the necessary components, as well as a copy of the application note, parts list, and user guide with instructions on how to set up, use, and test the board. Gerber files are also included for guidance on the board layout to insure good performance of the circuit.

Kit descriptions are included in the data book as an "MLXXXXEVAL" part number. For example, the ML2223EVAL is an evaluation kit for the ML2223 12-bit plus sign serial A/D converter. A one page description of the evaluation kit can be found in the Micro Linear data book under the heading of ML2223EVAL in the table of contents. The kits are available directly from the factory or from a distributor for a nominal charge to our customers.

Micro Linear Corporation Applications Handbook

LIFE SUPPORT POLICY

MICRO LINEAR'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF MICRO LINEAR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Application Note 1

FB3600 Digital Logic Design

Micro Linear's Bipolar ASIC Technology allows the mixture of both analog and digital circuitry on an integrated circuit. Micro Linear has combined the advantages of TTL, and ECL logic on our FB3600 family of bipolar tile arrays. Our +5 volt version of ECL can interface to the outside world at standard TTL, CMOS or 10K ECL levels. It requires the use of only a standard +5 volt power supply. On-chip, gate propagation delay times as low as 2 nanoseconds are possible. High density ECL digital components occupy fifty percent of Micro Linear's FB3635 tile array. In addition, a certain amount of digital logic can be implemented on all of the FB3600 tile arrays.

Traditionally, 10K ECL logic uses -5.2 volts supply. This additional supply is only needed for applications requiring an external ECL logic interface. Our FB3635 and FB3621 tile arrays contain schottky components. These components are often useful for implementing high speed TTL & CMOS output drivers. On-chip ECL Logic requires a voltage reference which changes over temperature. Normally, on-chip voltage references are designed to be stable over variations in temperature. The schematic diagram for this circuit has been provided.

This application note has been designed to aid a design engineer using a workstation with Micro Linear's analog ASIC design libraries. The circuits provide basic building blocks which can be integrated on our FB3600 family of tile arrays. The circuitry and discussion provided in this application note provide a starting point for the design engineer's own workstation circuit design and simulations.

Two Input ECL NOR Gate

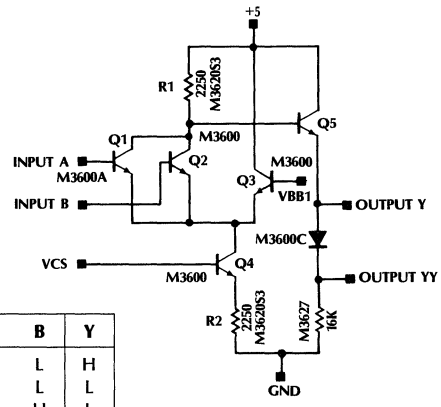
One of the major advantages of ECL logic is that the transistors never saturate. This plus the small signal swings reduce the propagation delay time through the gate. The propagation delay can be adjusted by changing the current level used by the circuit. The gate propagation delay decreases as the operating current level increases.

The ECL NOR gate, shown in figure 1, is designed for conventional +5 volt power supply operation. VCS is a preset bias voltage of 1.35 volts. This develops a voltage drop of 750mV across R2. The two ECL inputs (Input A & Input B) have a logic high (true) value of 4.25 volts and a logic low (false) value of 3.50 volts. VBB1 is a preset bias voltage which is about half way between the logic high and logic low voltages.

Micro Linear's single +5V operation is different from traditional 10K ECL logic which uses a single -5.2 volt supply. This establishes the 10K ECL logic high level in between -.810 and -.960 volts and a logic low level is in between -1.650 and -1.850 volts.

The NOR gate operates on the current flow from Q4. All the current from Q4 will be steered through either the Q3 leg or the Q1/Q2 leg of the circuit. If either Input A

Figure 1. NOR Gate



A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

or Input B logic voltage is high, all the current will flow up the Q1/Q2 leg of the circuit. This occurs because either or both transistors (Q1, Q2) have an input voltage which is above Q3 input voltage. Current flowing up the Q1/Q2 leg will cause a 750mV voltage drop to occur across R1 (same resistance as R2). This also results in Output Y being set at 5 volts minus 750mV minus 750mV (Q5 base to emitter voltage drop). Thus, Output Y is set at a logic low level (3.05 volts).

Both inputs need to be logic low for Output Y to have a logic high result (4.4 volts). In this case, the voltages on both Q1 and Q2 bases are less than the voltage on the base of Q3. This will cause all the current from Q4 to flow up the Q3 leg. The base of Q5 will be about 5 volts since the voltage drop across R1 is close to zero.

It is important to note that R1 always equals R2 and that the voltage drops (typically 750mV) across the base emitter will change with temperature. Since all the transistors on this IC are about the same temperature, they and the ECL voltage references will all track together with temperature. Thus the ECL logic works well over variations in temperature. The absolute values of the voltages stated above will change slightly with temperature. The values of resistors R1, R2, and R3 are adjusted for the desired speed vs power tradeoffs. The values shown in the NOR gate (figure 1) are typical values.

Figure 1 also shows an Output YY terminal. Some ECL logic gates need to have an extra diode voltage drop for its output. We will call this the "bias level B" output/input. The Output Y terminal does not have this extra diode voltage drop. Thus, we will call this the "bias level A" output/input.

Two Input ECL NAND/AND Gate

The basic operation of this gate's differential pair and the two output stages is very similar to the NOR gate discussion. The NAND/AND gates input stage requires Input A to be a "bias level A" input and Input B to be a "bias level B" input. A "bias level A" input needs to be driven by a "bias level A" output. Similarly, a "bias level B" input needs to be driven by a "bias level B" output.

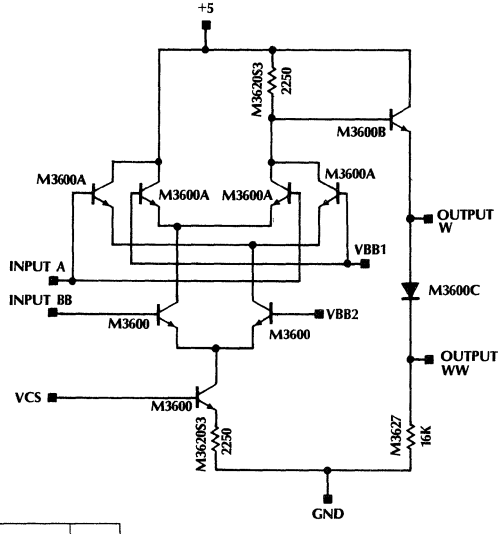
The NAND/AND gate shown in figure 2 has two output sections. The NAND output uses section A output stage. The AND output uses section B output stage. This gate can have either output stages omitted.

The NAND gate has its "bias level A" result on Output X and its "bias level B" output on Output XX. Similarly, the AND gate has its "bias level A" result on Output W and "bias level B" output on Output WW.

Two Input ECL XOR Gate

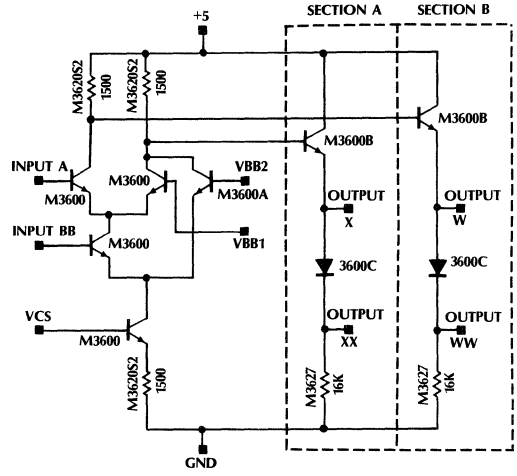
The basic operation of this gate's two differential pair and the output stages is very similar to the NAND/AND gate discussion. Figure 3 contains a circuit diagram for this gate. It uses one "bias level A" (Input A) input and one "bias level B" input (Input BB). The gates output is available as "bias level A" (Output W) and as "bias level B" (Output WW).

Figure 3. XOR Gate



A	B	W
L	L	L
H	L	H
L	H	H
H	H	L

Figure 2. NAND/AND Gate



A	B	X	W
L	L	H	L
H	L	L	L
L	H	L	L
H	H	L	H

ECL Data Latch

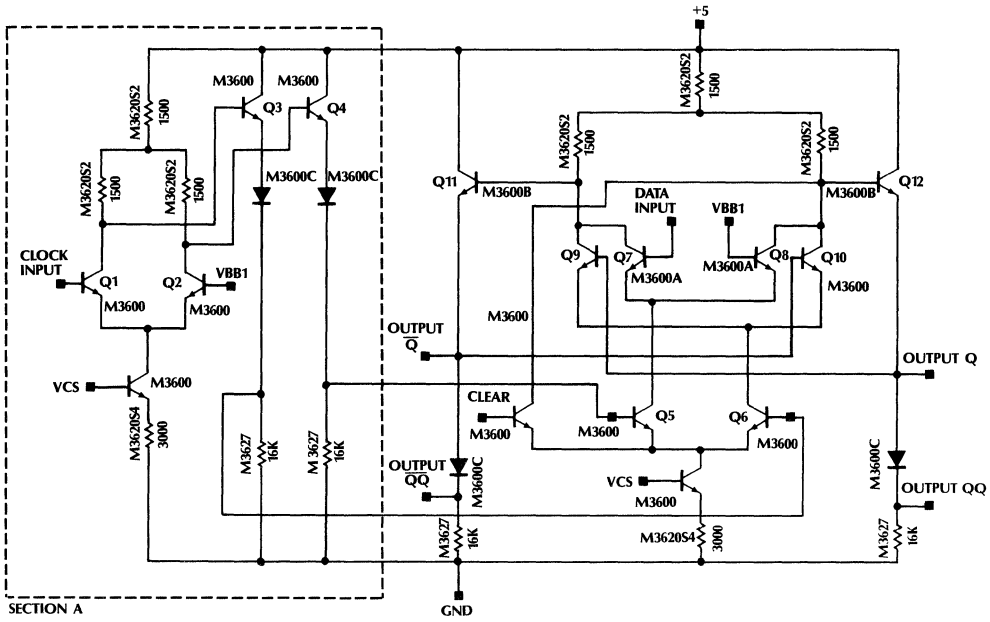
The circuit diagram for a single bit ECL data latch is shown in figure 4. As long as the Clock Input is logic high, the data latch will pass the data from the Data Input through to the output. If the input data changes, the output will track the change. This is called the pass through mode of operation. The pass through mode will end as soon as the Clock Input signal changes to logic low. When this transition occurs, the current value of input data will latch. The data latch will remain fixed as long as the clock remains low. Should the Clock Input return to the high state, the data latch will return to the pass through mode of operation. The data latch is level triggered instead of edged triggered.

Both the Clock Input and the Data Input are "bias level A" inputs. The "bias level A" outputs are Q and $\overline{Q}$. The "bias level B" outputs are QQ and $\overline{QQ}$.

When the Clock Input is high, the current value of the Data Input will be present at the Q and QQ outputs. An inverted version of Data Input will be present at the $\overline{Q}$ and $\overline{QQ}$ outputs. When the Clock Input is low, the latched value of the previous Data Input will be present at the Q and QQ outputs.

The data latch circuit contains circuitry to adjust the Clock Input signal. The circuitry shown in section A contains a circuit for converting a "bias level A" logic input into two "bias level B" output signals. The two output signals reflect the input signal and a complement of the input signal.

Figure 4.



The "bias level A" clock input signal drives the base of Q1. Transistor Q1 and Q2 form a different pair. The base of Q2 is driven by a reference voltage which is midway between logic high and logic low. When the Q1 input signal is high, the current will flow only through the Q1 leg of the differential pair. This will cause the collector of Q1 to have a voltage of about 4.25 volts and the collector of Q2 to have a voltage of about 5 volts. Substantial current will now flow through Q3. Thus, a "bias level A" logic low is present at the emitter of Q3. The diode in series with Q3 emitter shifts the output voltage to a "bias level B" output. This "bias level B" output will have a logic low value. Note that the Q3 outputs represent the complement of the Clock Input signal. Thus, a low Clock Input signal will result in a logic high output at the emitter of Q3.

A buffered version of the Clock Input signal is provided. This output will have the same logic level as the Clock Input signal. A "bias level A" version of the Clock Input signal is available at the emitter of Q4. The diode in series with Q4 emitter shifts the output voltage to a "bias level B" output.

The buffered Clock Input signal and its buffered complement will drive the bases of Q5 and Q6, respectively. When the data latch is in the data pass through mode (Clock Input high), transistor Q5 is turned on and transistor Q6 is turned off. If the Data Input is logic high, all of the current in the differential pair (Q7 & Q8) will flow in the Q7 leg. The current flow through the resistor in the Q7 leg will produce a 750mV drop. This sets the collector of Q7 at 4.25 volts. This will cause Q11 emitter to be at "bias level A" logic low (output $\overline{Q}$). Output $\overline{QQ}$ will be "bias level B" logic low. The lack of current flow in the Q8 leg will cause the collector of Q8 to be at about 5 volts. This will cause the emitter of Q12 to be logic high ("bias level A"). Output QQ will be at "bias level B" logic high.

When the Data Input is logic low, then all of the current will flow through the Q8 leg. Transistor Q11 emitter will now be at logic high. Output $\overline{QQ}$ will be at "bias level B" logic high. Transistor Q12 emitter will now be at logic low and the output QQ will be at logic low.

The data latch will store the current state of the output when the Clock Input signal changes to logic low. This will cause transistor Q5 to turn off and transistor Q6 to turn on. The base of Q9 gets its input from output Q. The base of Q10 gets it's input from the output $\overline{Q}$. Since it takes a few nanoseconds for Q11 and Q12 to change state after the input data changes, the data latch is now getting its input data from the previous output data. This feedback loop causes the data latches output to remain fixed.

The data latch also contains a CLEAR input. This input should normally be logic low ("bias level B"). A logic high will reset the data latch to logic low. As long as the CLEAR input is logic high, the data latch will remain reset.

One Bit ECL Register or Flip Flop

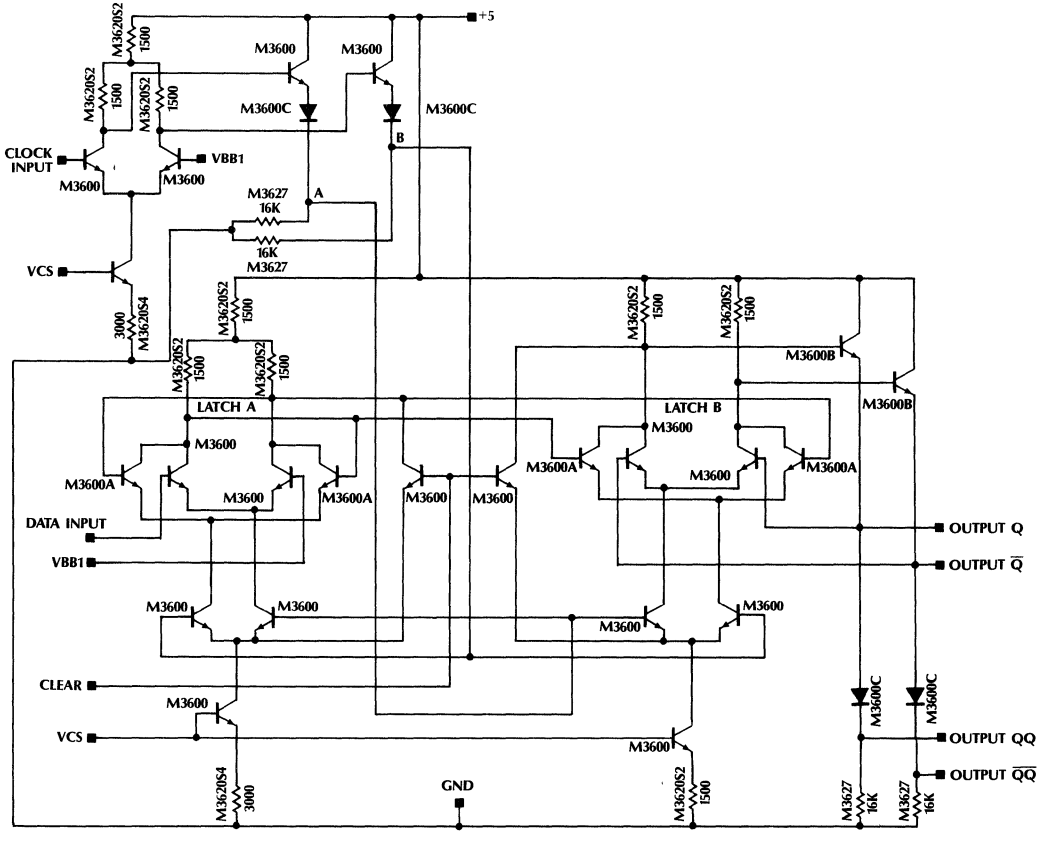
The circuit shown in figure 5 can be used as a single bit positive edge triggered register or as a flip flop. We shall first review its operation as a one bit register. This circuit latches the Input Data upon the Clock Input changing from logic low to logic high. The data will remain latched until the next time the Clock Input changes from logic low to logic high. Similar to the data latch circuit, the Clock Input and Data Input signal are both "bias level A" inputs. The register has four outputs. The outputs are available in both "bias level A" (Q and $\overline{Q}$) and "bias level B" (QQ and $\overline{QQ}$). The register's stored value (Q and QQ) and its complement value ($\overline{Q}$ and $\overline{QQ}$) are also provided.

This circuit is simply two data latches in series. Both data latches use a common clock. When one latch is in the data pass through mode, the other latch is latched. When the Clock Input signal is high, data latch A is latched and data latch B is in the pass through mode. When the Clock Input signal is low, data latch A is in the data pass through mode and data latch B is latched. If the Clock Input signal changes from low to high, latch A will latch its current input data and data latch B will pass data latch A output values directly to its output. This can change the data register's output. If the Clock Input signal changes from high to low, the output data will not change since latch B will latch itself using data provided by latch A previous outputs. Note that a flip flop can be implemented by connecting the register's $\overline{Q}$ output to the register's Data Input.

The register also contains a CLEAR input. This input should normally be logic low ("bias level B"). A logic high will reset the register to logic low. As long as the CLEAR input is logic high, the register will remain reset.

The Clock Input circuit has two "bias level B" outputs (point A and B). If these output connections are switched, the register will latch upon a logic high to low transition. This will cause it to be in pass through mode whenever the Clock Input is low. The data register will latch its data whenever the Clock Input is high.

Figure 5. Register or Flip Flop

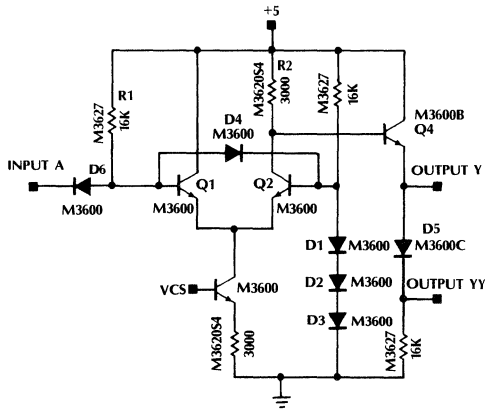


TTL and CMOS Input Interface Circuit

This circuit, shown in figure 6, converts a TTL or CMOS logic level input into an on-chip ECL level input. Output Y is a "bias level A" version of Input A. Output YY is a "bias level B" version of Input A. Transistors Q1 and Q2 forms a differential pair. The string of three diodes (D1, D2, and D3) sets the base of transistor Q2 at 2.25 volts. Given a high TTL/CMOS logic level drive at Input A, resistor R1 will bias the base of Q1 to be above the base Q2. This will cause all of the current to flow through the Q1 leg of the differential pair. Since the voltage drop across R2 will be about zero, the base of Q4 will be at 5 volts. The emitter of Q4 will be "bias level A" logic high. A "bias level B" version of this output will be produced at Output YY.

When Input A is driven by a TTL/CMOS low logic level, the base of Q1 will be biased below the base of Q2. Now all of the current will flow through the Q2 leg of the differential pair. The current flow will causes a 750mV voltage drop to occur across R2. The emitter of Q4 (Output Y) is now set at a "bias level A" logic low. Diode D5 produces a "bias level B" version of this output.

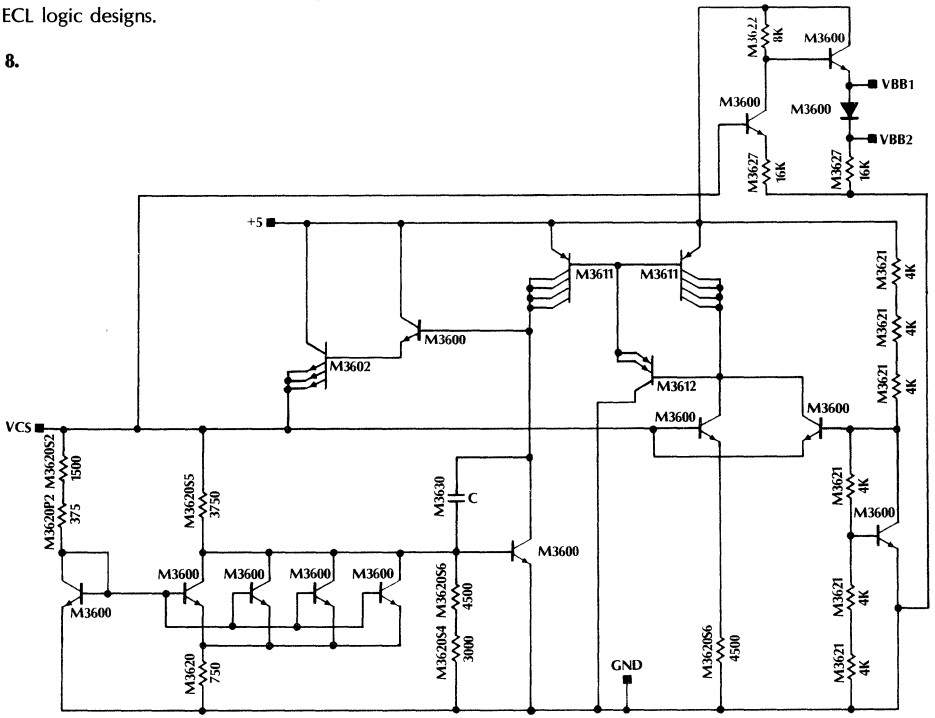
Figure 6. Input Interface



Voltage Reference for FB3600 ECL Logic

The circuit shown in figure 8 supplies the necessary reference voltages for our ECL logic. It has been designed to vary the output voltage with temperature. This block has been designed by Mirco Linear's engineering department as a standard function block to be included on all ECL logic designs.

Figure 8.



On-chip ECL to TTL or CMOS Output Interface

The circuit shown in figure 7 takes an on-chip "bias level A" ECL input and produces a TTL/CMOS compatible output. If the input is logic high (true) then the output will be logic high (true). The circuit simply buffers and shifts the logic voltage level from on-chip ECL voltage levels to TTL/CMOS voltage levels.

Section A contains circuitry similar to the CLOCK input for the data latch circuit. It converts the input into two signals (buffered version and a complement buffered version). If the input is driven by a high logic level, Q1 will be turned on and Q2 will be turned off. This causes the base of Q3 to be 4.25 volts and the base of Q4 to be 5 volts. Transistors Q3 and Q4 drives the bases of Q5 and Q6 respectively. Since the base voltage of Q4 is greater than the base voltage of Q3, the base voltage of Q6 will be greater than the base voltage of Q5. This will cause all of the current in the Q5 & Q6 differential pair to flow in the Q6 leg. If Input A is driven by a logic low level, all of the current in the Q5 & Q6 differential pair will flow in the Q5 leg.

The collector of Q6 drives the final output circuitry in section B. When Input A is at logic high, the collector of Q6 will be at .9 volts. The voltage drop across the base and emitter (.75 volts) of Q7 and Q8 will result in the bases of Q11 and Q12 being driven by less than .2 volts. Transistors Q11 and Q12 will be switched off. Since Q11 is off, the base of Q13 will be close to 5 volts. This turns Q13 on and results in a voltage of about 4.2 volts at the Output.

If Input A is at logic low, the collector of Q6 will be at 1.5 volts. The voltage drop across the base and emitter of Q7 and Q8 will result in the bases of Q11 and Q12 being driven by about .9 volts. This will turn on Q11 and Q12. With Q11 turned on, Q13 will be turned off and Q12 will be switched on. The output voltage will be about .75 volts.

We have just reviewed how section A circuitry drives the differential pair of Q5 & Q6. We have also reviewed how the collector of Q6 drives the output drive circuitry contained in section B. Next, we will examine how the Q5 & Q6 differential pair have been biased.

Section D contains a circuit known as a base emitter voltage multiplier. The voltage at the collector of Q15 will be determined by the following equation,

$$\text{Voltage at collector of Q15} = [1 + (R1/R2)] \times .75$$

The value of R1 and R2 is 10KΩ and 4KΩ respectively. The .75 represents the typical voltage drop across a transistors base to emitter. This sets voltage at the collector of Q15 at 2.6 volts. The voltage drop across the base and emitter of Q14 will set the collector voltage of Q5 at 2.6 – .75 = 1.85 volts.

When all of the current flows in the Q5 leg of the differential pair (Q5 & Q6), there will not be a voltage drop across the circuitry in section E (no current flow). The collector of Q6 is now set at 1.85 volts. If all of the current flows in the Q6 leg of the differential pair, there will be a .75 voltage drop across the diode. This sets the collector of Q6 at 1.1 volts.

The circuitry in section F provides a bias current for a current mirror. Resistor R3 value was chosen for a .5mA current flow with a 4.4 voltage drop across it. This input bias current generates the base to emitter voltage for Q16 which drives the bases of Q17, Q18, Q9 and Q10. Each of these transistors will sink .5mA.

Transistors Q19, Q21 and Q20 also form a current mirror. Transistor Q20 and its 8K emitter resistor have been added for stability. The purpose of the current mirror is to keep the curent flowing through Q3 and Q4 approximately equal.

Transistors Q11 and Q12 are schottky clamped transistors. They consist of a npn transistor with a schottky diode connected between the base and the collector. The function of this diode is to limit the current flowing into the base. This prevents the transistor from saturating. The schottky diode sends the excess base current into the collector. This limits the voltage drop across the collector and the emitter to about 200mV. The typical base emitter voltage drop is .75 volts. These devices can be replaced with regular npn transistors if the logic's switching rates are low (a few MHz). Saturated transistors have much slower switching times than non saturated transistors.

Voltage Reference for FB3600 ECL Logic

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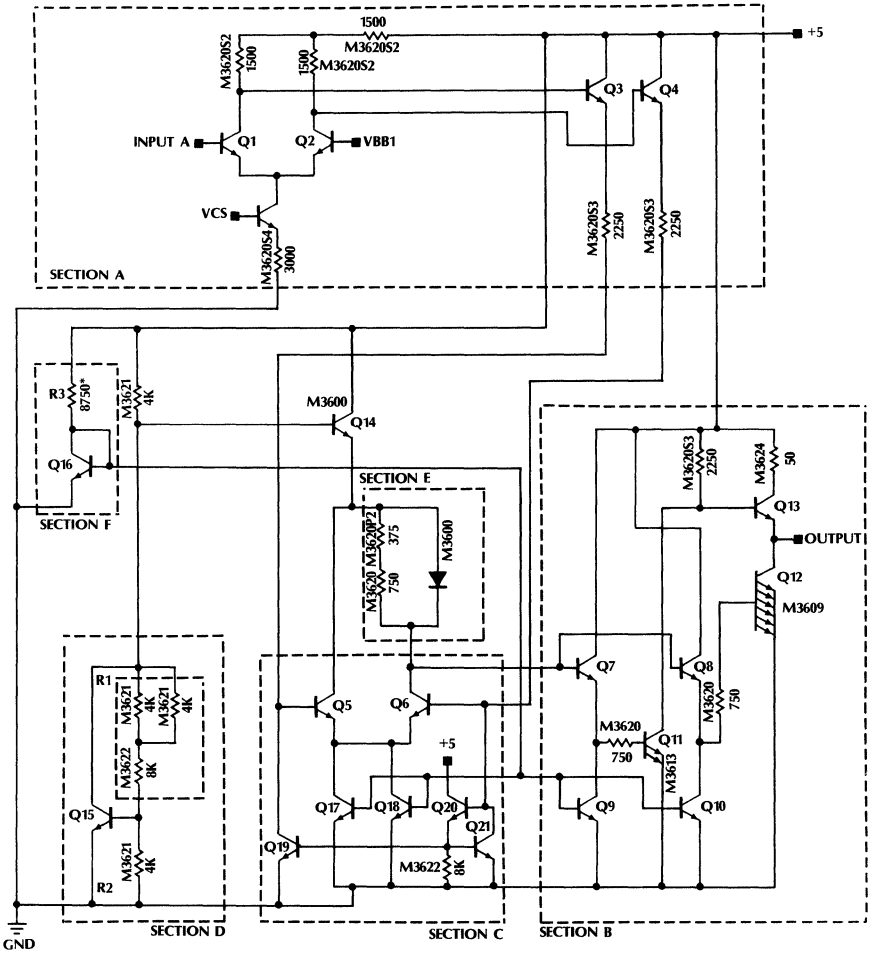
Figure 7. Output Interface



* BUILD UP OUT OF M3620s

Micro Linear

Application Note 2

Trimming Analog Bipolar Arrays

High performance analog integrated circuits are becoming a necessity in the design of state of the art analog/digital systems. With standard analog IC's this requires the designer to specify premium performance parts. These same premium performance circuit functions are not typically available in semicustom arrays. By utilizing trimming techniques, though, improved performance can still be obtained. Trimming analog bipolar arrays is a very viable, cost effective approach for improving the key parameters of a circuit.

If tighter specifications are required than can be obtained using good design techniques the circuit may be trimmed at the wafer level by a technique of selectively shorting zener diodes. This is known commonly as zener zapping. This technique can be used to trim the input offset voltage of an op amp or the output voltage of a precision reference. For example, the offset voltage of our MLC350[1] operational amplifier can be trimmed from a maximum of 7mV to less than 1mV. The MLC340 voltage reference can be trimmed to an accuracy of better than 1%. Many types of parameters may be trimmed within the limitations of the technique as described below.

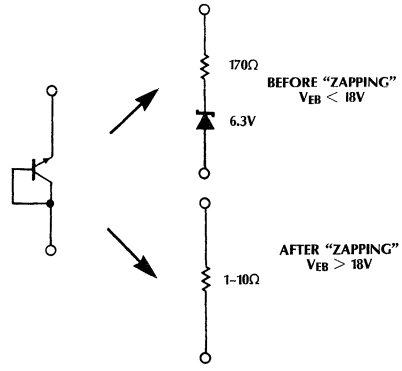
Although there are other ways in which a bipolar integrated circuit may be trimmed, zener zapping has become well established because it does not require extra processing steps and can be implemented at the wafer level. Unlike laser trimming, the technique is not limited to altering a resistive element, and does not require a large capital investment. Fusible links, another well-established method, requires currents in the ampere range in order to blow the standard 1 micron thick aluminum, resulting in a questionable blown connection. A thinner link would require additional wafer processing steps.

The Zener Zapping Technique

This process is called zener zapping because the emitter-base diode of a bipolar transistor is permanently shorted by passing a relatively large current through it while in the reverse breakdown avalanche mode. It produces a reliable 1-10 ohm link between the emitter and base pads. (See Fig. 1) This is a very reliable connection because of the double short which actually occurs. The first short is caused by the destruction of the pn junction. In addition, the presence of a large electric field during thermal runaway causes metal to migrate across the silicon surface beneath the oxide layer, producing a second short.

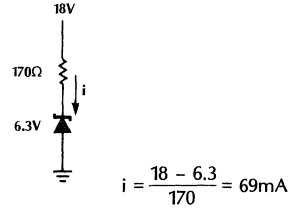
This set of events occurs when the voltage across the emitter-base junction is increased beyond the 6.3V

Figure 1.



avalanche breakdown point, to above 18V. At about 18V the instantaneous power dissipation exceeds 1.2W (figure 2) and an oscillatory, thermal runaway condition occurs. In less than a second the junction is destroyed leaving a 1-10 ohm short. The current required is less than 300mA, so remote probe pads (the bonding pads) can be used without damage to the pads or traces.

Figure 2.

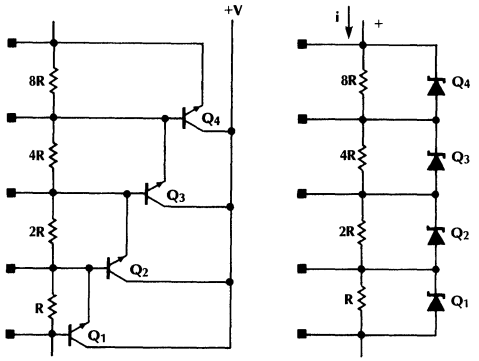


$$i = \frac{18 - 6.3}{170} = 69mA$$

Power Dissipation = iV = (69mA)(18V) = 1.24W

The circuit in figure 3 illustrates a simple implementation of this technique to alter the total resistance of a circuit path. Before any of the zeners are blown the total resistance equals 15R. This value can be altered to equal any integer multiple of R from 1R to 15R by selectively blowing only four zeners in a binary fashion. This is possible due to the binary arrangement of the resistor values. For example, to obtain a resistance of 5R, Q_2 and Q_4 should be shorted resulting in 4R + 1R = 5R. Note that 5 equals 0101 in binary which is represented by Q_4, Q_3, Q_2, Q_1 with shorts being 0's and opens being 1's.

Figure 3.



This type of circuit arrangement has two restrictions of which the designer should be aware. During normal operation of the circuit, the current through the resistor string should not be allowed to flow opposite to the direction indicated in the drawing. This would forward bias the base-emitter junction of the transistors, and effectively short out a resistor intended to be used. In addition, the forward voltage drop across each of the resistors should not exceed the zener breakdown voltage, about 6.3V. This would allow current to flow out of the resistor string and through the zener, altering the intended operation of the circuit.

The preceding example illustrates the use of zener zapping to alter a resistive element in a circuit. In many cases modifying a current source is a more useful way of trimming a design. Figure 4a shows trimmable current sources used to reduce the input offset voltage of an op amp.

In this example the balance of current in two circuit paths is altered using zener zapping. This technique is particularly useful for reducing the input offset voltage of an operational amplifier which has added emitter degeneration in the input stage in order to improve slew rate (figure 4b). The emitter resistors used in this circuit, R_6 and R_7, will contribute significantly to the offset voltage of the input stage. By modifying the balance of current between I_A and I_B the increased offset voltage V_{OS} can be compensated. In this example there are again 4 bits of trimming resolution with the 3 least significant bits controlling one current path and the most significant bit controlling the other. With this configuration the balance of current can be altered in either direction. In other words, the current in T_1 can be increased or decreased relative to T_2.

Figure 4a.

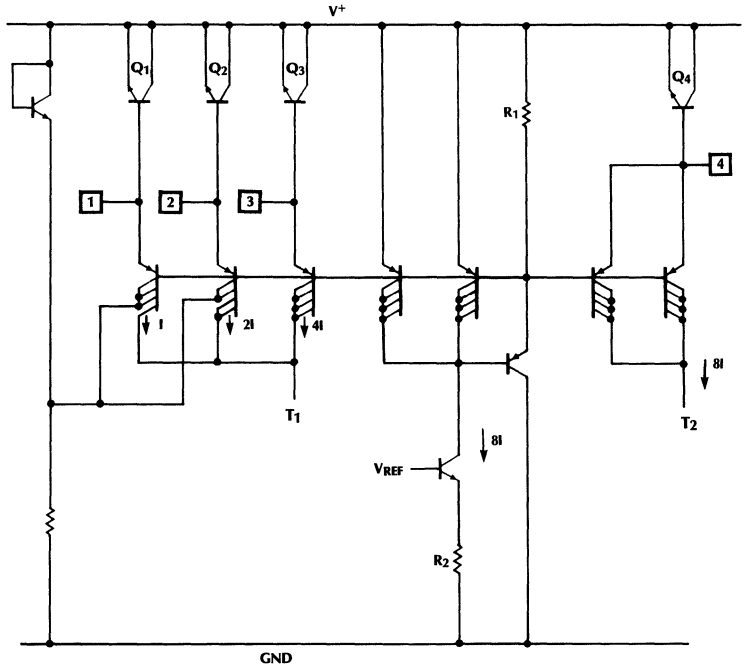
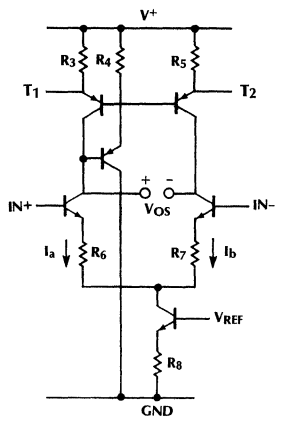


Figure 4b.



To increase the current through T_1 relative to T_2 you simply short Q_1, Q_2, and Q_3 in a binary fashion to get increments of I from 1I to 7I. To increase the current through T_2 relative to T_1 you short Q_4 which increase the current through T_2 by 8I. Then if you want less current, short Q_1, Q_2, and Q_3 in a binary fashion to offset the increase in T_2 by increments of I down to 1I.

The source of current in the trim circuit should be of the same type as the circuit to be trimmed so their temperature coefficients will match. In this case the V_{REF} in both circuits should be the same, and resistors R_2 and R_8 should be of the same type.

Shorting zeners is an irreversible process. Thus, it is important to check the results of a trim bit pattern before actually destroying the junctions. This is done by shorting the probe pads externally in the desired pattern through relays. In this way all combinations can be tried and the best results can be chosen and implemented.

Although these two examples both use 4 bits (4 zeners) to trim a circuit, any number can be used to get more or less resolution. The designer should be aware though of the practical limitations of each circuit to be trimmed. Other error terms like temperature coefficients will eventually become significant, and additional trimming beyond this point would be fruitless. In addition, the more zeners you use, the more probe pads are required. In a full custom circuit where minimum die size is the ultimate goal, the additional die area required for the diodes, pads and trim circuitry may become significant. An array, however, typically has unused components available for the trim circuitry, and you only have to be concerned with the number of bonding pads available. If all of the pads are already being used for pinouts then a larger array would be required.

These examples illustrate the usefulness and flexibility of zener zapping. There are many other potential applications for this technique though, and with a good understanding of the basic diode shorting process the design engineer can be creative in its application.

[1] The MLC350 is one of the circuits in Micro Linear's library of macrocells. Performance details of this circuit and other macrocells can be found in the FB300 Macrocell and Component Library booklet.

Micro Linear

Application Note 3

Design Techniques for Low Input Bias Current

Analog systems often require high impedance inputs to accommodate the demand for higher accuracy. Measurement systems which interface to photodetectors or high impedance transducers require devices with low offset voltage and low input bias current. This is necessary to receive and amplify the signal without introducing any significant errors. Under this constraint, the designer will often select a FET as the primary input device. Although a FET input stage may be appropriate in a discrete circuit design, there are other all bipolar techniques which are just as effective and better suited to an analog array. In some cases, these techniques will out perform the FET alternative.

This application note describes three alternatives for obtaining low input bias currents. The design techniques described can be applied to many different types of circuits from simple emitter followers to complex amplifiers. For example, a typical all bipolar operational amplifier can achieve input bias currents of about 100nA with an offset voltages of about 1mV[1]. Unfortunately these characteristics are still not good enough for many of the applications previously mentioned. The input bias current can be minimized by using one of the following design techniques, **1)** reducing the collector current **2)** using a Darlington configuration **3)** employing current cancellation techniques. This document will briefly describe the first two methods but will provide a detailed analysis of the cancellation technique as it provides the best performance trade-off and is the most involved.

Reducing the Collector Current

The simplest approach to achieve low input bias current is to reduce the collector current of the input transistors. Since the base current tracks the collector current by a factor of beta, reducing the collector current of the input transistors will reduce the input bias current into the bases. Beta will degrade at lower collector currents (figure 1), however, setting a practical limitation on this technique at about 50pA base current. If the circuit does not require a high slew rate or high gain bandwidth, this may be an acceptable method.

The Darlington Configuration

Figure 2 shows a differential Darlington configuration which will reduce the input bias requirements by a factor of beta. It will also double the offset voltage and reduce the voltage gain by 2. The offset voltage doubles due to the additional mismatching of the added devices, while the voltage gain suffers because only one-half of the input signal appears across the inner pair of transistors. A higher slew rate and gain bandwidth, though, can be achieved with this technique, over simply reducing the collector current, but it requires more components.

Figure 1. Current Gain vs. Collector Current

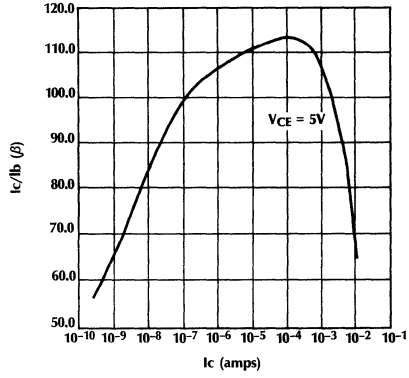
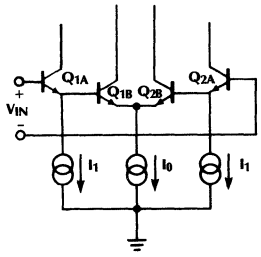


Figure 2.



$I_1 \ll I_0$

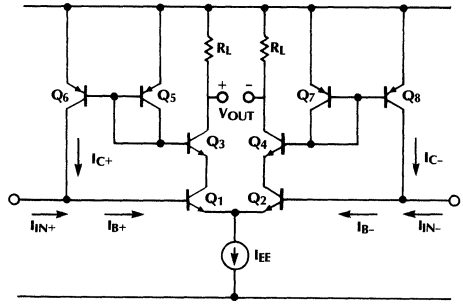
The Cancellation Technique

An all bipolar solution to low input bias current with low offset voltage while maintaining high collector currents for noise, slew rate or bandwidth reasons requires a technique called Input Bias Current Cancellation.

Input bias current cancellation is a circuit design technique which measures the input current and forces an equivalent amount back into the input nodes (figure 3). Ideally, this results in perfect cancellation of the input current. In the circuit in figure 3, the base currents into Q_3 and Q_4 duplicate the base currents into Q_1 and Q_2. These currents are then sensed by Q_5 and Q_7 and equivalent currents are fed back, via Q_6 and Q_8, into the input nodes. The total current at each input is thus,

$$I_{IN} = I_B - I_C$$

Figure 3.



Assuming all PNP betas (β_P) are equal, all NPN betas (β_N) and all base-emitter voltage drops are equal,

$$I_C = I_B \frac{\beta_N}{(1+\beta_N)} \frac{\beta_P}{(2+\beta_P)}$$

$$I_{IN} = I_B \left(1 - \frac{\beta_N}{(1+\beta_N)} \frac{\beta_P}{(2+\beta_P)}\right)$$

If all betas are very high,

$$I_C = I_B$$

so

$$I_{IN} = 0$$

The main contributor to cancellation errors in this circuit is the low beta of the PNP devices. This sets a practical limitation on this technique at about 5–10% of the uncanceled current, as shown by the following example.

Assumptions: $\beta_N = 100$, $\beta_P = 30$, $I_B = 70nA$

$$I_{IN} = 70 \left(1 - \frac{100}{1+100} \frac{30}{2+30}\right)$$

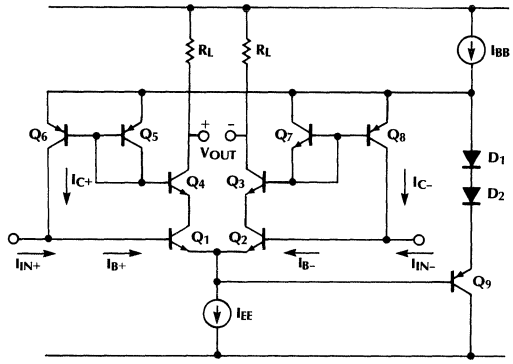
$I_{IN} = 70\ (.0718)$

$I_{IN} = 5nA$

This technique does not reduce the input *offset* current. In fact, the additional circuitry, with its additional mismatches, increases the offset current by a factor of about 3. The input bias current can be reduced to about the same value as the offset current, setting the limitation on this technique at about 1–10nA.

In the equations above, the betas of PNPs in the current mirror were assumed to be equal. To enhance the viability of this assumption, the V_{CE} of each PNP should be kept equal. With the cancellation circuitry tied to the positive supply the V_{CE} of Q_6 and Q_8 will change with the input voltage, while the V_{CE} of Q_5 and Q_7 will remain constant. This further aggravates any beta mismatch which already exists. To reduce this effect the circuit can be self-biased using current source I_{BB}, diodes D_1 and D_2, and transistor Q_9, as shown in figure 4.

Figure 4.



This circuit keeps the voltage across the cancellation circuitry fixed as the input common mode voltage changes, which in turn keeps the beta of each device constant.

These techniques for reducing input bias current demonstrate the reality of achieving levels sometimes thought only possible with JFETs or MOSFETs. Circuits being considered for analog array integration which contain discrete FETs or FET input op amps should not be categorized as not possible. Rather, each individual circuit should be analyzed for its critical parameters, keeping in mind the trade-offs described above. If none of the bipolar solutions is adequate an external FET can always be used as an input buffer.

[1] The offset voltage can be reduced by making use of wafer trimming techniques. At Micro Linear a process called zener zapping is used. For more information about this process see the application note titled "Trimming Bipolar Arrays".

Micro Linear

Application Note 4

High Frequency Complex Filter Design Using the ML2111

Charles Yager
Carlos Laber

1.0 Introduction

Switched capacitor filters have been growing in popularity because of their advantages over active filters. Switched capacitor filters don't require external precision capacitors like active filters. Their cutoff frequencies have a typical accuracy of ±0.3%, and they are less sensitive to temperature changes. This allows consistent, repeatable filter designs. Another distinct advantage of switched capacitor filters is that their cutoff frequency can be adjusted by changing the clock frequency. Switched capacitor filters offer higher integration at a lower system cost.

Until the introduction of the ML2111, commercially available switched capacitor filters were limited to about 20 KHz center frequencies. The ML2111 uses the versatile architecture of the MF10 with enhanced performance to reach center frequencies of up to 150 KHz with Q values up to 20.

Designing high frequency, high order filters using the ML2111 is the main topic of this application note. Particular attention is focused on mode 1c, which has the advantage of operating at high frequencies while allowing the center frequency to clock ratio to vary based on external resistors. A flexible building block is introduced which implements all the necessary types of bi-quads to realize high order complex filters. Finally an example is given which illustrates the design of an eighth order Elliptic bandpass filter with a center frequency of 90 KHz and a passband from 81 KHz to 100 KHz.

The first part of the application note covers a variety of issues: layout, how fast the system clock can be changed for sweeping filters, and some differences between continuous and sampled data filters. For the reader who is already familiar with sampled data filters, section 2 on Effects of Sampling, Aperature, Aliasing, and Signal Reconstruction may be skipped.

2.0 Effects of Sampling

Since the ML2111 is a switched capacitor filter, it behaves as a sampled data system. Switched capacitor filters, as opposed to digital filters, are analog sampled data systems. The signal remains in the analog domain, as the charge on a capacitor. Whether using an analog or digital sampled data system, the effects of sampling the signal must be considered.

Figure 1 shows a time domain input and output signal of an analog sampled data system. In the ideal case, the sampled data system, samples the input signal instantaneously, or with an impulse function. The amplitude of each sample is equal to the instantaneous amplitude of the input signal. The output is a series of narrow pulses, each separated by time T, the sampling period.

2.1 Aperture

Since an impulse function in the time domain corresponds to a flat spectrum in the frequency domain, the input spectrum is exactly reproduced in the frequency domain, however, in reality the sampling signal is periodic and has a finite pulse width. When convoluting a finite pulse width with an input spectrum F(jω) with unity amplitude, the result is found to be:

$$F_{st}(j\omega) = \frac{\tau}{T}\,\frac{\sin(\omega\tau/2)}{\omega\tau/2} \sum_{n=-\infty}^{\infty} F[j(\omega - n\omega_s)] \qquad (1)$$

Figure 1: Signal Processing Systems

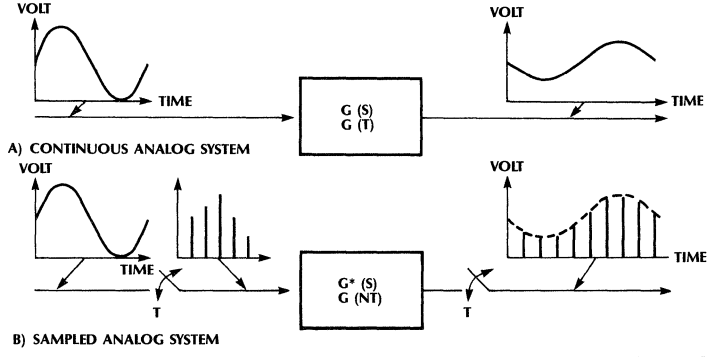
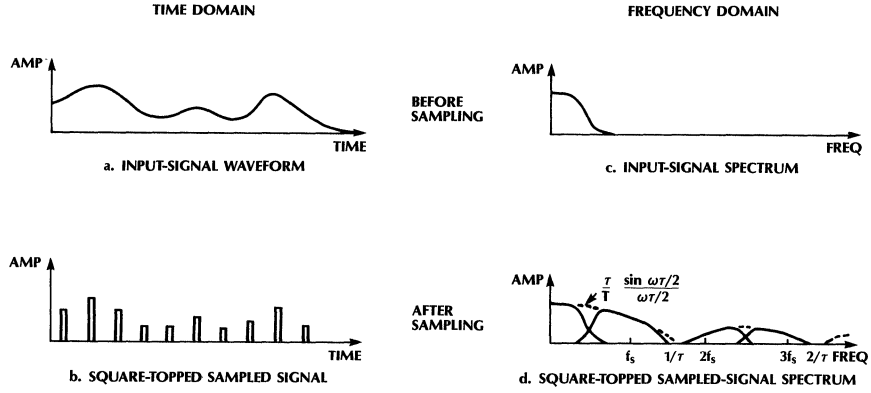


Figure 2: Analysis of a Sampled Signal



From this equation, the gain is a continuous function of frequency defined by (τ/T) $(\sin(\omega\tau/2)/(\omega\tau/2))$ where τ is the sample pulse width in seconds, T is the sample period in seconds, and ω the frequency in radians per second.

The time and frequency domain plots for the finite pulse width sampled signal are shown in figure 2. Figure 2 is a plot of the previous equations where the frequency spectrum is formed around multiples of the sampling frequency. As long as the adjacent spectra do not overlay (aliasing distortion), the continuous signal can be reconstructed from the discrete samples.

To evaluate the amplitude distortion caused by having a finite pulse width, one can simply solve equation 1. Since the ML2111 has a zero-order hold τ/T is unity. Assuming a 7.5 MHz sampling frequency and a bandwidth of 150 KHz, the amplitude distortion or attenuation is 5.7×10^{-3} dB.

The equation shows that when the sampling frequency is 40-50 times greater than the bandwidth, the aperture effects are negligible.

2.2 Aliasing

Another potential source for distortion in a sampled data system is aliasing. Aliasing distortion occurs when the input frequency to a sampled data system contains frequency components above one half the sampling frequency. These higher frequency components beat with the sampling frequency and are reflected back into the baseband causing aliasing distortion.

The additional spectral components caused by sampling the input signal are the sum and differences of the input frequencies with multiples of the sampling frequency. For example, assume the input to a sampled data system is a sine wave with a frequency of 100 KHz (f_i) sampled at 250 KHz (f_s), as shown in figure 3a. The first few spectral components will be at: (f_i = 100 KHz; original signal, $f_s - f_i$ = 150 KHz, $f_s + f_i$ = 350 KHz, $2f_s - f_i$ = 400 KHz, $2f_s + f_i$ = 600 KHz, . . .) Now assume f_i has a second harmonic, which would be at 200 KHz, the spectral components are shown in figure 3b. If our bandwidth of interest were from DC to $f_s/2$, then the $f_s - 2f_i$ component interferes with the original signal. If we were to reconstruct the original signal by lowpass filtering it, we could not separate the aliased component, $f_s - 2f_i$ = 50 KHz, from the original signal.

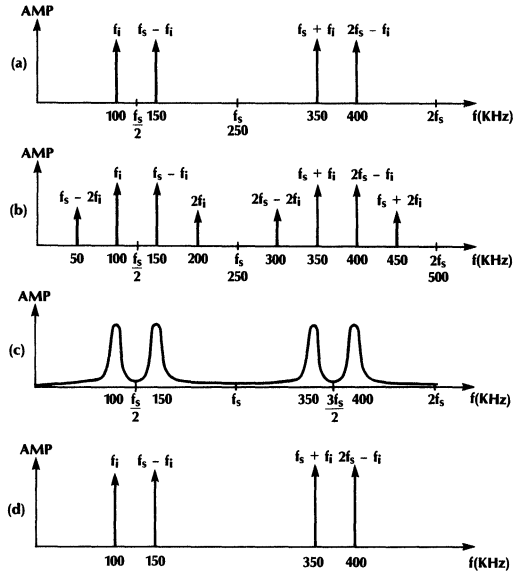
If our bandwidth of interest is a bandpass, the aliased component may not interfere. For example, if the ML2111 were to be used as a four pole bandpass filter with a center frequency at 100 KHz and a Q = 10 as shown in figure 3c, then the aliasing components in the above example would be filtered out as shown in figure 3d. But if the ML2111 were to be used as a low pass filter, then the $f_s - 2f_i$ aliased component would not be filtered out by the ML2111, and an anti-aliasing filter would be needed.

If the input signal is not band-limited, and the aliasing components fall within the bandwidth of interest, then a lowpass filter or anti-aliasing filter must be placed in front of the ML2111. This filter must be a continuous filter rather than a sampled data filter, however, the complexity of this filter is typically much less than the ML2111 filters, and its frequency response is less critical allowing for relaxed component tolerances.

Since no frequency component can be totally eliminated, one must determine the acceptable amplitude of the aliasing components that will *not* impact the Signal to Noise ratio of the system.

The higher the ratio of sampling frequency to input bandwidth, the lower the requirements on the anti-aliasing filter. Figure 4 shows the effects of sampling rate

Figure 3. Aliasing Distortion Using Sample Data Filters



rate on the separation of sampled signal spectra. Note the amount of overlap increases as the sampling frequency is decreased for a fixed input signal bandwidth. In general, the higher the sampling frequency, the less aliasing distortion. Since the ML2111's sampling frequency is typically either 50 or 100 times greater than the input bandwidth, the aliasing distortion may be negligible.

2.3 Signal to Noise Ratio and Aliasing Distortion

To determine whether aliasing distortion could be a problem, one must first determine the Signal to Noise Ratio of the overall system. Aliasing distortion less than the signal to noise ratio is of no concern.

The data sheet specifies noise based on Q and bandwidth. From these specs one can deduce the S/N ratio of one bi-quad in the ML2111. Using a simplified example, a bandpass filter with a Q = 10 and a system clock to center frequency ratio of 50:1 has noise that is 262 μVrms over a 750 KHz bandwidth; taken from the specs in the data sheet. To determine the maximum input signal amplitude, one must consider the slew rate spec. The typical value is 2 V/μsec, however a comfortable safety margin is 1.495 V/μsec for the commercial temperature range and 1.256 V/μsec for the military temperature range. The slew rate = $2\pi fA$, where f is the maximum input frequency, and A is the peak amplitude in volts. Therefore A = 1.495E6/(2*π*100E3) = 2.3 Volts; and the S/N = 78 dB.

Based on a 100 KHz bandpass filter with a Q = 10, f_{CLK}:f_0 = 50:1, and a signal to noise ratio of 78 dB, what sort of anti-aliasing filter would be sufficient? One must first look at the spectrum of the input signal, particularly in the 4.895 MHz to 4.905 MHz frequency range since this is the range that will be reflected back into the bandwidth of interest, 95 KHz to 105 KHz. If the frequency components in the 4.895 MHz to 4.905 MHz are below 78 dB, they will have a minimum impact on the signal to noise ratio. Let's assume that these frequency components are down only 20 dB. Then the anti-aliasing filter will have to attenuate the frequencies in the 4.895 MHz to 4.095 MHz range by 78 - 20 = 58 dB, and pass the frequencies in the 95 KHz to 105 KHz frequency range with no attenuation. A simple two pole Butterworth filter with a cutoff frequency of 170 KHz will be sufficient, however there will be an attenuation of about 0.5 dB at 100 KHz due to this filter.

Figure 5a shows a Sallen-Key active filter capable of implementing two poles, and figure 5b shows a Rauch filter also implementing two poles. These two active filters are good examples to use for anti-aliasing and reconstruction filters. Using the Rauch filter for the above example, C_5 = 400 pF, C_8 = 90 pF, and R = R_4 = R_6 = R_7 = 5 KΩ. Fortunately the cutoff frequency for the antialiasing and reconstruction filters are not critical since capacitors can vary 5% and resistors can vary 1%. Taking into account component tolerance for our example, the cutoff frequency can vary worst case from 152 KHz up to 178 KHz.

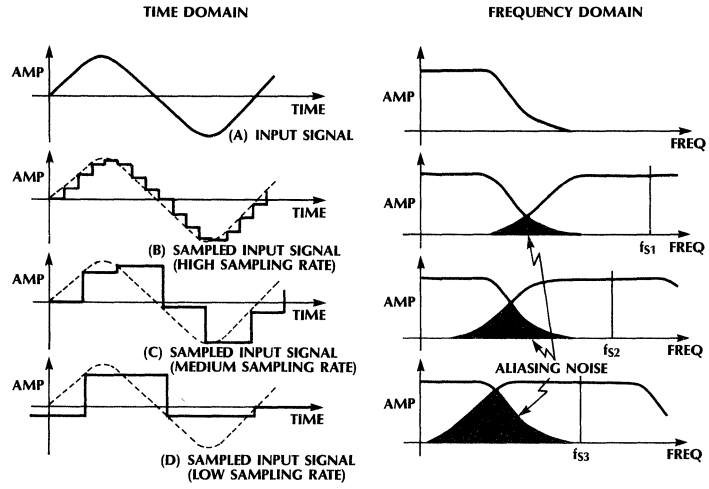
The important aspects to note are that one must first determine the signal to noise ratio in the bandwidth of interest. Based on this bandwidth, are there any frequencies that will be reflected back into the bandwidth of interest, and if so how much will they need to be attenuated? Remember that frequency components reflected back outside of the bandwidth of interest, will be filtered by the ML2111. Since the ratio of the sampling frequency to the center frequency is large on the ML2111, most designs will not need an anti-aliasing filter, and if they do, a simple two pole butterworth should suffice.

2.4 Signal Reconstruction

The output signal of a switched capacitor filter contains higher frequency components since it is a sampled signal. Many systems can accommodate these higher frequency components; however, if they interfere with the system's performance, then a signal reconstruction filter can be employed.

A time domain and frequency domain plot of the output from the ML2111 is given in figure 6. The output signal changes amplitude every clock period. These sharp transitions elicit high frequency components in the output signal. Once again, the fact that the ratio of the sampling frequency to the input bandwidth is high, reduces these distortion effects. As a result of the sin (x)/x envelope, the higher frequency components are attenuated. For example, assuming the input bandwidth is 100 KHz and

Figure 4: Effects of Sampling Rate on Aliasing Noise



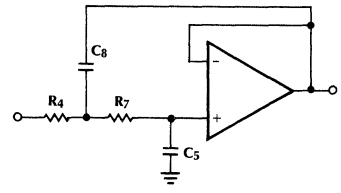
the sampling rate is 5 MHz, the frequencies around 4.9 MHz are down 34 dB, and they degrade towards zero as the frequency reaches 5 MHz. A single pole reconstruction filter with a cutoff frequency at 200 KHz would add an additional attenuation of 27 dB at 4.9 MHz but would attenuate the output by 1 dB at 100 KHz. A two pole Butterworth as in figure 5a or 5b would yield 58 dB of attenuation at 4.9 MHz and only 0.5 dB at 100 KHz.

3.0 Layout Considerations

The layout of any board with analog and digital circuitry combined mandates careful consideration. The most important steps in designing a low noise system are:

1. All power source leads should have a bypass capacitor to ground on each printed circuit board (PCB). At least one electrolytic bypass capacitor (50 μF or more) per board is recommended at the point where all power traces from the ML2111 join prior to interfacing with the edge connector pins assigned to the power leads.
2. Layout the traces such that analog signal and capacitor leads are far from the digital clock.
3. Both grounds and power supply leads must have low resistance and inductance. This should be accomplished by using a ground plane where ever possible. Either multiple or extra large plated through holes should be used when passing the ground connections through the PCB.
4. Use a separate trace for clock ground, and connect it to the edge connector board ground.
5. Use ground plane on both sides of PC board.
6. All power pins on ICs should have 0.1 μF and a 0.01 μF capacitors in parallel tied to ground, and as close to the power pins as possible.
7. Stray capacitance, lead lengths, and traces, on pin 4 and 17, the negative input of the op amp, should be kept to a minimum, particularly for high frequency filters which are more sensitive.

Figure 5a. Sallen-Key Filter

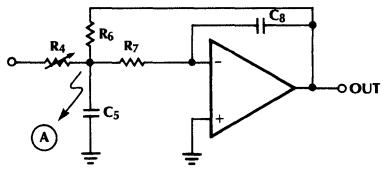


$$\frac{1}{s^2B + sC + 1}$$

$B = R_4R_7C_5C_8 = 1/\omega_0^2 \qquad R_4 = R_7$

$C = C_5 (R_4 + R_7) = 1/Q\omega_0$

Figure 5b. Rauch Filter



DC Gain: $\frac{R_6}{R_4} = H(0)$ [Minimize Parasitic C at Node (A)]

Transfer function: $\frac{H(0)\ (1/B)}{s^2 + s(C/B) + 1/B} = \frac{H(0)\ \omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$

$B = R_6R_7C_8C_5$

$C = \frac{R_6R_7C_8 + C_8(R_6 + R_7)R_4}{R_4}$

Choose Butterworth response for example:

$\omega_0 = 2\pi[170\ KHz] \approx 1.06 \times 10^6$ rad/s
$Q = .707$

say $R_4 = R_7 = R_6 = R \Rightarrow 1/\omega_0^2 = R^2C_8C_5$

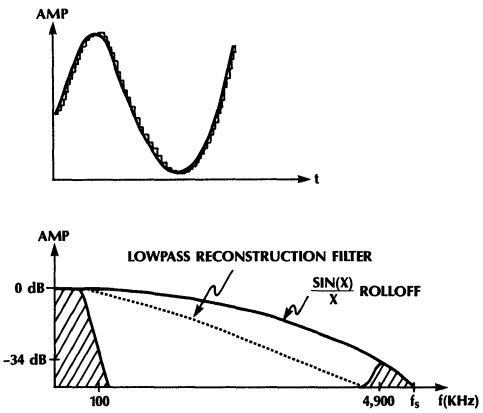
$C = RC_8 + C_8(R_6 + R_7) = RC_8 + 2C_8R = 3RC_8$

$$\Rightarrow \frac{C}{B} = \frac{3RC_8}{R^2C_8C_5} = \frac{3}{RC_5} = \frac{\omega_0}{Q}$$

$$\Rightarrow \begin{cases} C_5 = \frac{3Q}{R\omega_0} \\ C_8 = \frac{1}{\omega_0^2R^2C_5} \end{cases}$$

say $R = 5\ K\Omega$
$\therefore C_5 = 400\ pF$
$C_8 = 90\ pF$

Figure 6: Signal Reconstruction



3.1 Clocks and Output Loading

It is important to properly terminate the clock input to prevent overshoot. Each pin has protection diodes for Electro-Static Discharge (ESD), and any overshoot of more than 0.3 to 0.5 volts will be injected directly into the ML2111's ground and/or supplies. Matching the characteristic impedance of the line will prevent any ringing thus reduce clock noise.

When operating with high clock frequencies, the output of the op amp and integrators should be properly loaded. Ideally these outputs—LP, BP, and N—like to drive a total of 2 to 3 mA of peak current each. Assuming the output voltage swing is ±2 volts, the sum of R_5 and R_6, in mode 1c for example, should be 2 V/2 mA or about 1,000 ohms; assuming no other resistors are connected. Sometimes this is difficult to do if the ratios and loading cannot simultaneously be achieved. In this case an additional loading resistor placed as close as possible to the output pin will serve the purpose of properly loading the outputs.

4.0 Sweeping Filters

One particularly nice feature of sampled data filters is the fact that the center frequency of a filter is directly related to the clock frequency. For a lowpass filter, increasing the clock frequency increases the cutoff frequency. Even though the center frequency increases proportionally with the clock, Q stays constant. Therefore in a bandpass filter, increasing the clock frequency increases the center frequency as well as the bandwidth. Table 2 in the data sheet illustrates this relationship. (Note that there is some Q deviation as the system clock goes beyond a certain value. Refer to figure 2E in the data sheet for a graph of this phenomenon)

A good rule of thumb for the maximum rate a filter can be swept is that the Sweep Rate should be less than the square of the bandwidth of the filter. This will reduce attenuation of the passband as a result of sweeping the filter. The theoretical derivation of this approximation is as follows.

Assume we have a bandpass filter with an in-band signal that starts at t = 0. The output of the filter will exponentially increase until it reaches the steady state gain of the passband. After 4 time constants (τ), the output sine wave will be at 98% of its final amplitude.

Sweeping a filter is analogous to keeping the filter constant and sweeping the input frequency. To prevent the filter from attenuating the sweeping input signal by more than 2% or 0.16 dB:

$$\text{Sweep Rate} < BW/4\tau \quad (2)$$

but the time constant can be approximated by:

$$\tau \simeq Q/2\pi f_0 \quad (3)$$

and,

$$Q = f_0/BW \text{ or } BW = f_0/Q \quad (4)$$

substituting τ and BW into equation (2) results in:

$$\text{Sweep Rate} < \pi BW^2/2 \quad (5)$$

5.0 High Frequency Operation

There are three basic modes for the ML2111 — mode 1, 2 and 3. Within each mode there are several variations as shown in the table below.

Mode 1*	High Frequency Mode
1, 1a, 1d 1b, 1c	f_0 up to 150 KHz; Q up to about 20** f_0 up to 100 KHz; Q up to about 30
Mode 2	**Flexible for Notches**
2, 2a, 2b	f_0 up to 30 KHz; Q up to about 30
Mode 3	**Most Flexible/Low Component Count**
3, 3a	f_0 up to 30 KHz; Q up to about 30

* Q and f_0 have an inverse relationship. This table is only an approximation. Actual performance depends on board layout and stray capacitance.

** 15% or less Q deviation. Higher Q's can be realized with greater deviation.

Mode 1 is the only mode which has the input amplifier outside the resonant loop. This is important because the input amplifier reduces the bandwidth potential of the filter. *Only Mode 1 can achieve filters with resonant frequencies up to 150 KHz.*

Inserting an ML2111 into an MF10, LMF100, or LTC1060 socket and increasing the clock frequency does not automatically increase the bandwidth potential up to 150 KHz. If these pin-compatible parts were designed using Mode 1, the bandwidth improvements would be realized; however if they were used in another mode, there would be limited bandwidth improvements.

Complex, high order filters usually have pole pairs with different center frequencies; Elliptical and Chebyshev filters are two examples. To realize two pole pairs in one ML2111 with different center frequencies, one must either use two different clocks, or use a mode which allows the center frequency to be modified by external resistors.

Using different clock frequencies to realize poles with different center frequencies is not recommended. Besides the additional expense of providing more than one clock, the two system clocks may beat with each other and possibly result in side tones that falls within the passband of the filter. Additionally if anti-aliasing is needed, separate anti-aliasing filters would be needed for each stage.

Looking at tables 1 and 2 in the ML2111 data sheet, one can see the modes that allow the center frequency to be modified by external resistors. These modes each have an additional coefficient multiplied by $f_{CLK}/100(50)$. From the block diagrams one can see that the modes which allow the center frequency to be modified, feedback the LP output using a resistor divider. The modes that restrict the ratio to 50 or 100 have a unity gain LP feedback.

If the coefficient multiplied by $f_{CLK}/100(50)$ is greater than or equal to 1, as in Mode 1b, then the ratio of f_{CLK} to f_0 can be less than 50 or 100. Whereas if this coefficient is less than or equal to 1, then the ratio of f_{CLK}:f_0 can be greater than or equal to 50 or 100. Reducing the ratio of f_{CLK} to f_0 to less than 40 to 50 is not recommended. As the ratio of the sampling frequency to the center frequency is reduced, the approximation of a sample data filter to a continuous filter is reduced. Aperture effects increase, aliasing effects may increase, harmonics in the output increase, and the warpage between the discrete and the continuous filter increase. 40 to 50:1 is the minimum recommended ratio of f_{CLK} to f_0.

Based on the above arguments one might conclude that 100:1 is better than 50:1. In general this is true for switched capacitor filters, but not for the ML2111. The specifications in the data sheet show that a 50:1 ratio provides a more accurate Q than a 100:1, and a 50:1 ratio allows higher frequency filters.

Mode 3 is the most flexible since the center frequency can be greater than or less than $f_{CLK}/100(50)$ by selecting R_2 and R_4. Its also the most efficient since it has the lowest component count. However mode 3 can only work up to 30 to 40 KHz or Qs up to the 10 to 30 range; higher f_0 can be obtained with lower Qs. Sometimes a small capacitor (C_4) across R_4 can compensate the filter response and offer less Q deviation. The value should be selected by setting C_4 equal to $1/2\pi R_4 BW$ where BW is approximately equal to 2 to 4 MHz.

Another reason mode 3 can only be used at lower frequencies is that there is a true sample and hold at the positive input of the summer. This sample and hold adds a 7.2 degree delay at the center frequency when using a 50:1 ratio (360°/50). By using a higher ratio this delay is lowered. Since the ML2111 allows a higher system clock than other competing devices, this delay can usually be made smaller for similar center frequencies.

In conclusion, for high frequency filters use Mode 1. For complex filters with various center frequencies use Mode 1c. In most cases one should choose 50:1 over 100:1 ratio for more accurate Q's and center frequencies.

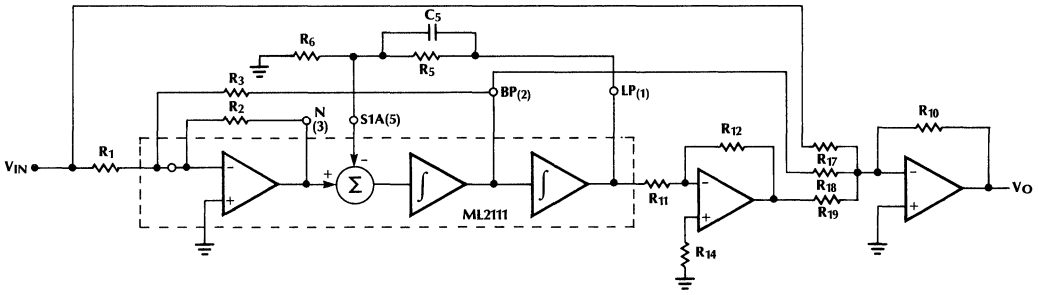
5.1 A Flexible Building Block

Figure 7 shows the block diagram of a second order section which includes both a complex pole pair and a complex zero pair. The poles are provided by the ML2111 and the zeros realized by one and sometimes two external op amps. This building block uses mode 1c which allows the poles to have a center frequency based on external resistors as well as the clock, plus it can be used in higher frequency filters since the op amp is outside of the resonant loop. The same feedforward circuit can be used on other modes as well, but for high

frequency filters, where each complex pole pair has a different center frequency, mode 1c is the best choice. As mentioned before, only when Butterworth filters are desired, use mode 1 to achieve higher frequencies and a higher dynamic range. The transfer function for the flexible building block is given below.

$$\frac{V_O}{V_{IN}} = \left(-\frac{R_{10}}{R_{17}}\right)\left[\frac{s^2 + \frac{R_2}{R_3}\left[1 - \frac{R_{17}}{R_{18}}\frac{R_3}{R_1}\right]s\omega_1 + \left[1 + \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)\right]\frac{R_6}{R_5 + R_6}\omega_1^2}{s^2 + \frac{R_2}{R_3}s\omega_1 + \frac{R_6}{R_5 + R_6}\omega_1^2}\right] \quad (6)$$

Figure 7: Flexible Building Block



At least one and sometimes two external op amps are required to realize the zeros. The first op amp serves as an inverter, while the second one sums the input signal with the lowpass and bandpass outputs. A fast op amp should usually be used with greater than 10 MHz bandwidth to minimize signal phase shifts. Depending on the application, sometimes a slower amplifier will suffice. In some cases no external op amp is necessary and the second op amp in the ML2111 if not being used will suffice. This was done in figure 34 in the data sheet.

With the Flexible Building Block a lowpass, highpass, notch, and allpass section can be realized by properly positioning the zero locations. Zero locations are chosen by selecting the appropriate resistors. The difference between the lowpass output provided by the ML2111 in mode 1c and the lowpass function realized by the flexible building block is that in mode 1c the response is monotonically decreasing, while the Flexible Building Block has a complex zero pair which inserts a ripple in the stop band and flattens out at high frequency.

Since the Flexible Buidling Block uses mode 1c, the pole equations remain the same whether there is feedforward or not. What changes is the zero location and the DC gain. The following equations are used to determine the pole locations and Q for the Flexible Building Block, which uses mode 1c.

$$f_0 = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R_6}{R_5 + R_6}}$$

$$Q = \frac{R_3}{R_2}\sqrt{\frac{R_6}{R_5 + R_6}}$$

A handy set of equations to convert pole and zero locations given in rectangular coordinates to f_0 and Q values is as follows:

Complex Pole = $\sigma + j\omega$;

$$f_0 = \frac{\sqrt{\sigma^2 + \omega^2}}{2\pi} \quad Q = \frac{1}{2}\sqrt{1 + (\omega/\sigma)^2} \quad (7)$$

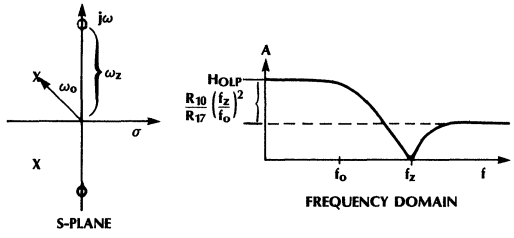
By cascading several of these building blocks, complex high frequency Elliptical filters can be realized.

5.2 Lowpass

For a lowpass design with a notch, the zeros should be placed on the $j\omega$ axis at frequencies greater than the poles' center frequency. In the numerator of the transfer function for equation 6, the coefficient for $s\omega_1$ should be set to zero; setting $\frac{R_3}{R_1} = \frac{R_{18}}{R_{17}}$.

Since $\frac{R_6}{R_5 + R_6}\omega_1^2 = \omega_0^2$, the coefficient

$1 + \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)$ determines the center frequency of the zero. In this form it is always greater than one, therefore the center frequency of the zero is always greater than the center frequency for the poles; hence a lowpass filter. The pole/zero location and the frequency response are shown below.



Equations for the lowpass configuration:

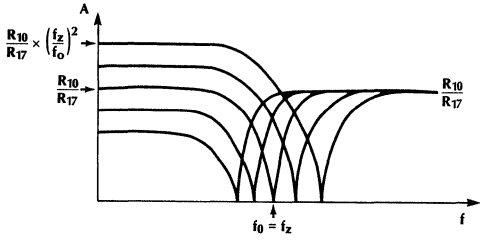
$$\frac{R_{17}}{R_{19}} = \frac{\left(\frac{f_Z}{f_0}\right)^2 - 1}{\frac{R_2}{R_1}\left(1 + \frac{R_5}{R_6}\right)} \qquad f_Z = f_0\sqrt{1 + \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)}$$

$$\text{DC Gain} = H_{OLP} = \left(-\frac{R_{10}}{R_{17}}\right)\left(1 + \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)\right)$$

The ratio of the zero to the pole frequency determines the DC to high frequency attenuation.

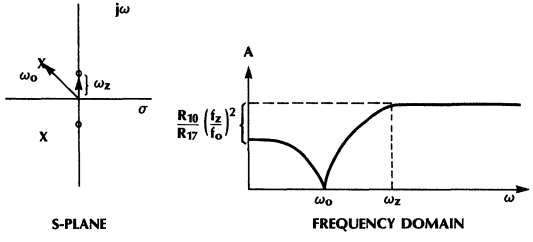
When the zeros are at the same frequency as the poles the bi-quad becomes a notch, and there is no difference between the high frequency and low frequency gain. The larger the difference between the pole and zero frequencies, the greater the rejection. Figure 8 illustrates the relationship between pole/zero location and gain.

Figure 8: Varying f_Z and Keeping f_0 and Q Constant



5.3 Highpass

For a highpass filter the zeros must be less than the center frequency for the poles. The pole/zero plot and the frequency plot are shown below.



To place the zeros at a lower frequency than the poles the coefficient $1 + \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)$ must be less than one. This can be done by removing the inverter in figure 7, which makes the sign of R_{19} negative. To place the zeros on the jω axis, once again $\frac{R_3}{R_1} = \frac{R_{18}}{R_{17}}$. Equations for the highpass configuration:

$$f_Z = f_0\sqrt{1 - \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)}$$

$$H_{OHP} = -\frac{R_{10}}{R_{17}}$$

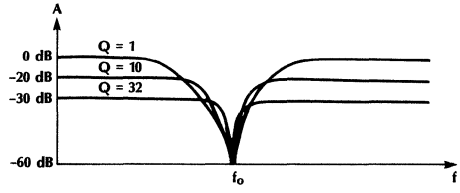
5.4 Notch

Even though mode 1c provides a notch output, the notch realized by the flexible building block achieves 0 dB of gain at DC and at high frequencies regardless of the Q value. The problem with the notch in mode 1c is that

$$H_{ON1}\ (f \rightarrow 0) = H_{ON2}\ (f \rightarrow f_{CLK}/2) = \frac{\sqrt{\frac{R_6}{R_5 + R_6}}}{Q}.$$

As Q increases $H_{ON1,2}$ must decrease otherwise the bandpass output node, BP pin 2 or 19, will saturate. The restriction is that $H_{OBP} = 1 = -R_3/R_1$. Let's take a simple case when $R_5 = 0$, then $H_{ON1} = H_{ON2} = 1/Q$. The plot below shows the notch for different Q's in mode 1c.

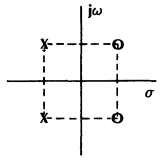
Figure 9: Mode 1c Notch when $R_5 = 0$



To realize the notch using the Flexible Building Block the zeros must be placed on the jω axis at the same resonant frequency as the poles. Therefore from equation 6, $\frac{R_3}{R_1} = \frac{R_{18}}{R_{17}}$ and $R_{19} \rightarrow \infty$. Setting R_{19} equal to infinity means removing it from the circuit; which saves an op amp and a few resistors. H_{OBP} still must equal one, however the gain at DC and $f_{CLK}/2$ is independent of Q; $H_{ON1}\ (f \rightarrow 0) = H_{ON2}\ (f \rightarrow f_{CLK}/2) = -R_{10}/R_{17}$. Tuning R_{18} adjusts the depth of the notch. See figure 34 in the data sheet for an example.

5.5 Allpass Equalizer

An allpass filter is used to linearize the filter's phase response. A linear phase response results in a constant group delay. An allpass filter keeps the gain constant and just shifts the phase. To keep the gain constant and only shift the phase, the poles and zeros must be equal but on opposite sides of the s-plane as shown below.



S-plane representation of 2nd order Allpass Filter

The Flexible Building Block can function as an allpass when $R_{19} \rightarrow \infty$ and $\frac{R_{17}R_3}{R_{18}R_1} = 2$. The Transfer function for the allpass is:

$$\frac{V_O}{V_{IN}} = \left(-\frac{R_{10}}{R_{17}}\right) \frac{s^2 - \frac{R_2}{R_3}\omega_1 s + \frac{R_6}{R_5 + R_6}\omega_1^2}{s^2 + \frac{R_2}{R_3}\omega_1 s + \frac{R_6}{R_5 + R_6}\omega_1^2} \qquad (8)$$

5.6 Frequency Compensation

In some cases it is possible to improve the Q accuracy and minimize Q deviation by adding a capacitor (C_5) in parallel with R_5 in figure 7. This capacitor serves as compensation for a pole at around 2.4 MHz in the output of LP. The zero location should be placed at around 2.4 MHz, where the internal pole is. Unfortunately C_5 adds a pole as well as a zero to this branch. If this pole is too close to the zero, the benefit of C_5 is diminished. The zero location is: $f_Z = 1/2\pi R_5C_5$ and the pole location is: $f_p = 1/2\pi(R_5 \parallel R_6)C_5$, ($R_5 \parallel R_6$ is the parallel equivalent resistance). The larger the ratio of the pole frequency to the zero frequency, the better this capacitor will serve.

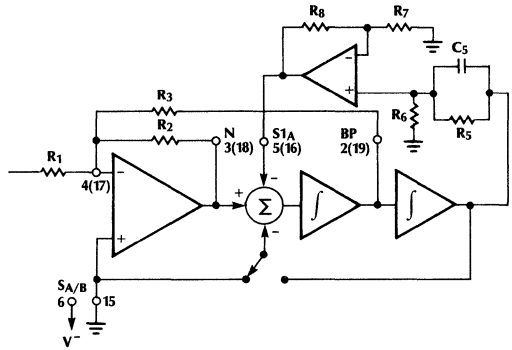
The highest center frequency attained is when R_5 equals zero. (Note: Practically speaking R_5 should never be zero, to allow fine tuning of f_0.) Unfortunately C_5 cannot properly compensate the 2.4 MHz internal pole with a negligible value for R_5. To overcome this problem, compensation can be achieved at high frequencies using an op amp in the LP feedback branch as shown in figure 10.

The center frequency in mode 1c is calculated by the following equation:

$$\frac{f_{CLK}}{f_0} = \frac{50}{\sqrt{k}}$$ where k = Transfer function

With a passive feedback loop using R_5 and R_6, $k = \frac{R_6}{R_5 + R_6}$. However when using the op amp configuration as in figure 10, $k = \left(\frac{R_6}{R_5 + R_6}\right)\left(1 + \frac{R_8}{R_7}\right)$. When k = 1 the ratio is 50. Using active feedback in mode 1c has the unique advantage of allowing the ratio of clock to center frequency to be less than 50 by setting k greater than 1. It is not recommended to use ratios less than 40-50, however this feature does allow more freedom in tuning the center frequency of the pole above or below the ratio of 50. If the circuit uses a crystal for f_{CLK}, and the pole needs to be tuned, R_8 could be a potentiometer to allow tuning of the pole. For this compensation to work $\frac{R_8}{R_7}$ should be 4-9 to provide phase lead before phase lag.

Figure 10: Compensation Using Active Feedback for High Frequency Poles



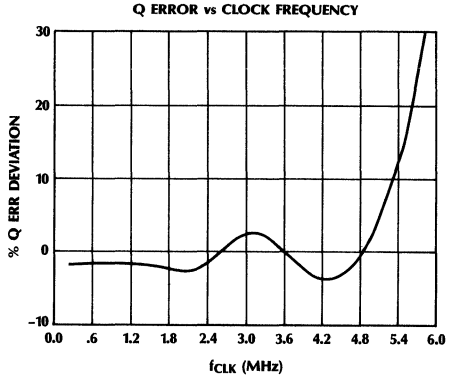
C_5 = 33-66pF (Depends on board's parasitics)
R_8 = 1800Ω ; R_7 = 200
R_6 = 100Ω, R_5 = 900Ω

Using mode 1 instead of mode 1c as configured in figure 7, is a better solution for high frequency poles; however there are certain cases where mode 1 cannot be used. For example, if one of the two bi-quads in the ML2111 is already used in mode 1c, then the other one must also operate in mode 1c. It would be less expensive to add an op amp to the second bi-quad of an existing ML2111 than to add an additional ML2111 just to use one bi-quad operating in mode 1.

Figure 11a shows the Q accuracy vs. clock frequency in mode 1c using passive feedback for a Q approximately equal to 10. Q inaccuracy dramatically increases just beyond 100 KHz center frequency. Figure 11b shows Q accuracy vs. center frequency in mode 1c using active feedback with a DC transfer function of 1. The op amp used for this measurement was an AD5539, where

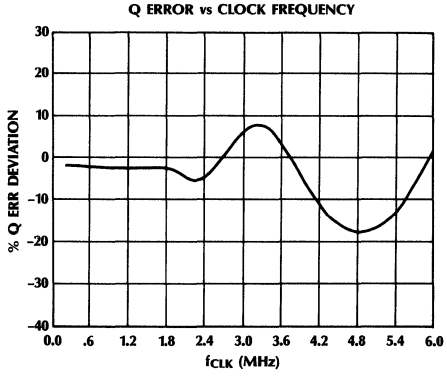
$\frac{R_8}{R_7} = \frac{R_5}{R_6} = 9$. This op amp is a good choice because it has a wide bandwidth, 220 MHz, and is low cost. The figure shows that Q deviation does not dramatically increase until well beyond 120 KHz; therefore for higher frequency operation and high Q, the use of mode 1c with active feedback is recommended.

Figure 11a: Mode 1c with Passive Feedback



$\frac{R_3}{R_2} = 10$; $R_5 = 0$; $R_1 = R_3 = 20K$

Figure 11b: Mode 1c with Active Feedback



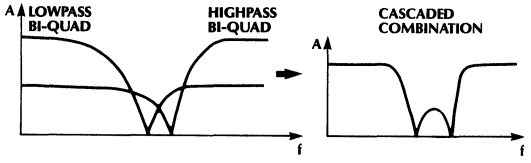
$C_5 = 33pF$; $\frac{R_3}{R_2} = 10$; $R_5 = 0$; $R_1 = R_3 = 20K$

6.0 Design Methodology for Complex Filters

The previous section described how to use the Flexible Building Block to implement lowpass, highpass, notch, and allpass second order sections. Higher order filters are achieved by cascading these second order sections. For example an Elliptical notch is accomplished by cascading lowpass and highpass sections as shown in figure 12.

An Elliptical bandpass is also a combination of highpass and lowpass sections, except for a bandpass filter the cutoff frequency for the highpass bi-quads are lower than the cutoff frequency for the lowpass.

Figure 12: Fourth Order Elliptic Notch



Once the pole and zero location have been determined for the filter desired, the next step is to choose the proper mode of operation and translate the center frequency and Q values for each pole and zero into resistor values. If the pole and zero locations are given in real and imaginary values, they can be converted to f_0 and Q by using equation 7.

For center frequencies between 0 and 20 KHz, either mode 3 or mode 1c can be used. Sometimes mode 3 or mode 3a will result in a lower component count. However mode 3 should be used with caution since high Qs and high parasitic capacitance on pin 4 and 17 can lead to oscillations. This can usually be compensated by using a capacitor across R4, which provides some phase lead, and low value resistors such as 1-2 Kohms.

For center frequencies between 20 to 100 KHz, where each pole has a different center frequency, mode 1c should be used. This range can be extended up to 120 KHz with active compensation in the LP feedback path as shown in figure 11b. The combination of high Qs (20 to 30), and high frequencies (above 80 to 100 KHz), and parasitic capacitance across R_6, can lead to oscillations. This can be dealt with by placing a capacitor C_5 across R_5, or by using active compensation. Additionally the signal swing should be limited to about 1 to 1.4 volts peak-to-peak.

For filters where f_0 is the same for all pole locations, such as Butterworth, Lowpass or Highpass. High order filters with cutoff frequencies up to 150 KHz can be realized using mode 1. In this case the signal level can be increased to 2.82 volts peak-to-peak.

7.0 Design Example

The following is an example an eighth order Elliptic bandpass filter with a center frequency of 90 KHz and a bandwidth of 19 KHz. This filter was designed built and tested on its own printed circuit board. A print of the masks for the PCB, and a photograph of the performance of the filter is included at the end of this section.

In general, high Q filters (Elliptic and Chebyshev) will have higher sensitivity to component and temperature variations and higher noise than low Q filters such as Butterworth and Bessel.

a) 8th Order Elliptic Bandpass with the following Filter characteristics:

Amax: 0.5 dB (peak to peak passband ripple)

Amin > 50 dB (stopband attenuation)

(f_1, f_2) Passband: 81,000 to 100,000 Hz
(geometrically symmetric) $\Rightarrow f_c^2 = f_1 \times f_2$

(f_c) Center: 90,000 Hz

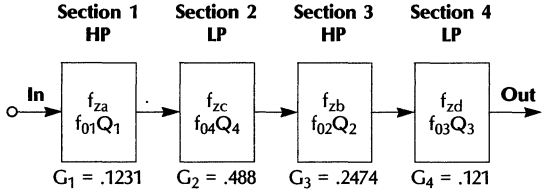
Stopband: 70.5 KHz to 115 KHz

b) Obtain:

Poles
- f_{01} = 80839 Hz, Q_1 = 30.2
- f_{02} = 85820 Hz, Q_2 = 10.86
- f_{03} = 94383 Hz, Q_3 = 10.86
- f_{04} = 100200 Hz, Q_4 = 30.2

Zeros
- f_{za} = 69185 Hz
- f_{zb} = 50082 Hz
- f_{zc} = 117080 Hz
- f_{zd} = 161733 Hz

c) After considering a few pole-zero pairing combinations the following (not necessarily optimum) combination was adopted.



Note: G_i are the high frequency gains. (= R_{10}/R_{17})

Because of difficulty in solving equations first order equation were calculated and final values found by using potentiometer.

d) Choose f_{CLK} = highest f_0 = 100200
@ 50:1 $\Rightarrow 50f_0$ = 5.01 MHz. Choose ~ 10% higher f_{CLK} = 5.5 MHz. It's better to choose a slightly larger f_{CLK} to be able to adjust R_5.

e) Design Procedure.

Section 1. *) Want a ratio = $\frac{5.5\ \text{MHz}}{80839\ \text{Hz}} \cong 68 = R_t$

in Mode 1c $R_t = 50 \times \sqrt{1 + \frac{R_5}{R_6}} \Rightarrow 1 + \frac{R_5}{R_6} = 1.8516$

Assume $R_5 + R_6 = 1000\ \Omega$

then $1 + \frac{R_5}{R_6} = \frac{1000}{R_6} = 1.8516$

$\Rightarrow R_6 \cong 540\Omega$ (fixed R)

$\Rightarrow [R_5 = R_6\ (1.8516 - 1) \cong 460\ \Omega]$ [1000 Ω trim pot]

*) Want Q = 30.2 use following approximation:

$$\frac{R_3}{R_2} \approx \frac{Q\sqrt{1 + \frac{R_5}{R_6}}\ \text{(Note)}}{1 + Q(f_0/f_X)} \quad ; \text{where } f_X = 2.4\ \text{MHz (internal pole)}$$

$\cong 20.4 \Rightarrow$ assume R_2 = 2000 Ω
and $R_3 \approx 40.7$ KΩ (100 K trim pot)
and initially assume $R_1 = R_3 = 40.7$ KΩ

*) Zero. Use the following approximation.

f_{za} = 69185 Hz

$$\frac{R_{17}}{R_{19}} \cong \frac{1 - (f_z/f_0)^2}{\frac{R_2}{R_1}\left(1 + \frac{R_5}{R_6}\right)} = \frac{1 - (69185/80839)^2}{1/20 \times 1.8516} = 2.89$$

Since R_{19} loads the LP output then assume $R_{19} > 5000\Omega$. Also since later we will fine tune the gains this relationship will slightly change. Thus, initially assume a higher R_{17} which can be change later if needed.

Choose $R_{17} \cong 30$ KΩ (fixed R)
and $R_{19} \approx 10$ KΩ (20 KΩ trim pot)
choose $R_{18} = R_{17}$ (initially)
and $R_{10} = R_{17} \times G_1 = 30K \times .123 = 3690\ \Omega$ (fixed R)

(Note: This is a first order approximation that underestimates the value of Q, whose final value will be tuned in later in the breadboard stage.)

f)
1. By looking at the bandpass output adjust R_5 until the peak frequency is f_0, in this case 80839 Hz
2. Then adjust R_3 until Q = 30.2
3. Then change R_1 until the peak of the bandpass or lowpass output (larger of the two) is about 0 dB. R_1 does not need to be a trim pot.
4. Now by looking at the output of the section adjust R_{19} to place the zero at the correct frequency (in this case 69185 Hz)

5. Adjust R_{18} to obtain a deeper notch. Sometimes R_{18} is not needed at all and can be removed from the circuit.
6. Check the high frequency gain so that it is G_1 = .1231
7. Design the rest of the sections the same way
8. Keep R_{10} of first section as a trim pot to slightly trim gain of the whole filter (if important in the application).

For this design these are the final values:

Section 1.

R_1 = 94.5 KΩ
R_2 = 2 KΩ
R_3 = 66.2 KΩ (100 K pot)
R_5 = 452 Ω (1 KΩ pot)
R_6 = 540 Ω
R_{10} = 3.83 KΩ
R_{17} = 32.4 KΩ
R_{18} = 15 KΩ
R_{19} = 4.65 KΩ
$H_{LP\ PEAK}$ = 1.1512 (+1.22 dB)
$H_{BP\ PEAK}$ = .846 (–1.45 dB)

Section 2.

R_1 = 65 KΩ
R_2 = 2 KΩ
R_3 = 47.4 KΩ (100 K pot)
R_5 = 170 Ω (500 Ω pot)
R_6 = 830 Ω
R_{10} = 14.34 KΩ
R_{17} = 28.7 KΩ
R_{18} = ∞
R_{19} = 2.9 KΩ
$H_{LP\ PEAK}$ = 1.12 (+.984 dB)
$H_{BP\ PEAK}$ = .972 (–.247 dB)

Section 3.

R_1 = 31.5 KΩ
R_2 = 2 KΩ
R_3 = 23.3 KΩ (50 K pot)
R_5 = 389 Ω (1 KΩ pot)
R_6 = 600 Ω
R_{10} = 9.05 KΩ
R_{17} = 40 KΩ
R_{18} = 16.86 KΩ
R_{19} = 6.35 KΩ
$H_{LP\ PEAK}$ = 1.074 (+.62 dB)
$H_{BP\ PEAK}$ = .834 (–1.58 dB)

Section 4.

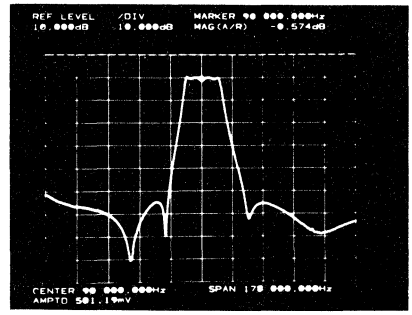
R_1 = 25 KΩ
R_2 = 2000 Ω
R_3 = 21.4 KΩ (50 K pot)
R_5 = 279 Ω (500 Ω pot)
R_6 = 732 Ω
R_{10} = 12 KΩ
R_{17} = 99.97 KΩ
R_{18} = ∞
R_{19} = 6 KΩ
$H_{LP\ PEAK}$ = 1.12 (+.924 dB)
$H_{BP\ PEAK}$ = .953 (–.418 dB)

Note: All R's are 1% metal film 1/4W
Trim pots are 25 turns. 1/2W

When placing resistors in and out of the ML2111 filter circuit, specifically R_3, the filter will oscillate at f_0 due to the Q going to infinity. Also when designing high frequency high Q filters, such as f_0 = 100 KHz and Q = 30 like pole #4, high voltage swings may cause nonlinear operation provoking oscillations. Changing f_{CLK} momentarily to a much lower value will restore the filter to a stable linear operation. Thus it is important for high frequency, high Q filters to limit the input signal swing to about 500-700 mV peak.

7.1 Performance Measurements, Schematics and PCB Layout

Figure 13: Frequency Response of Eighth Order Elliptic Filter.



The center frequency is at 90 KHz with the lower cutoff at 81 KHz and the upper cutoff at 100 KHz. The stopband is down -55 dB at 70.5 KHz and 115 KHz.

Figure 14: Passband of Filter Showing 0.5 dB Ripple.

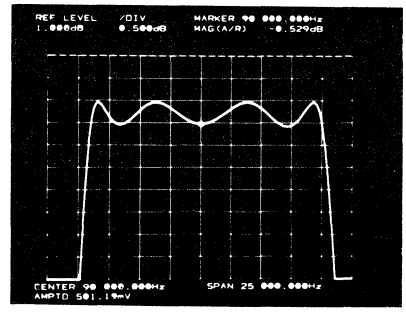
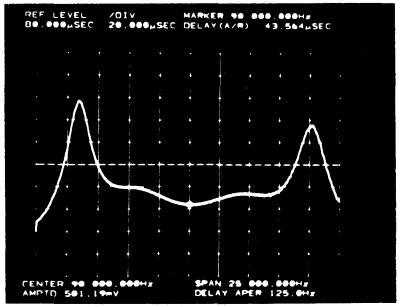
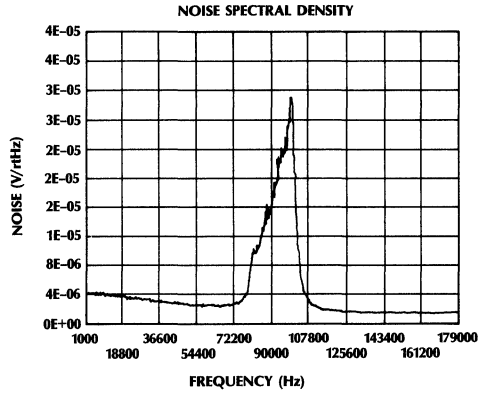


Figure 15: Group Delay.



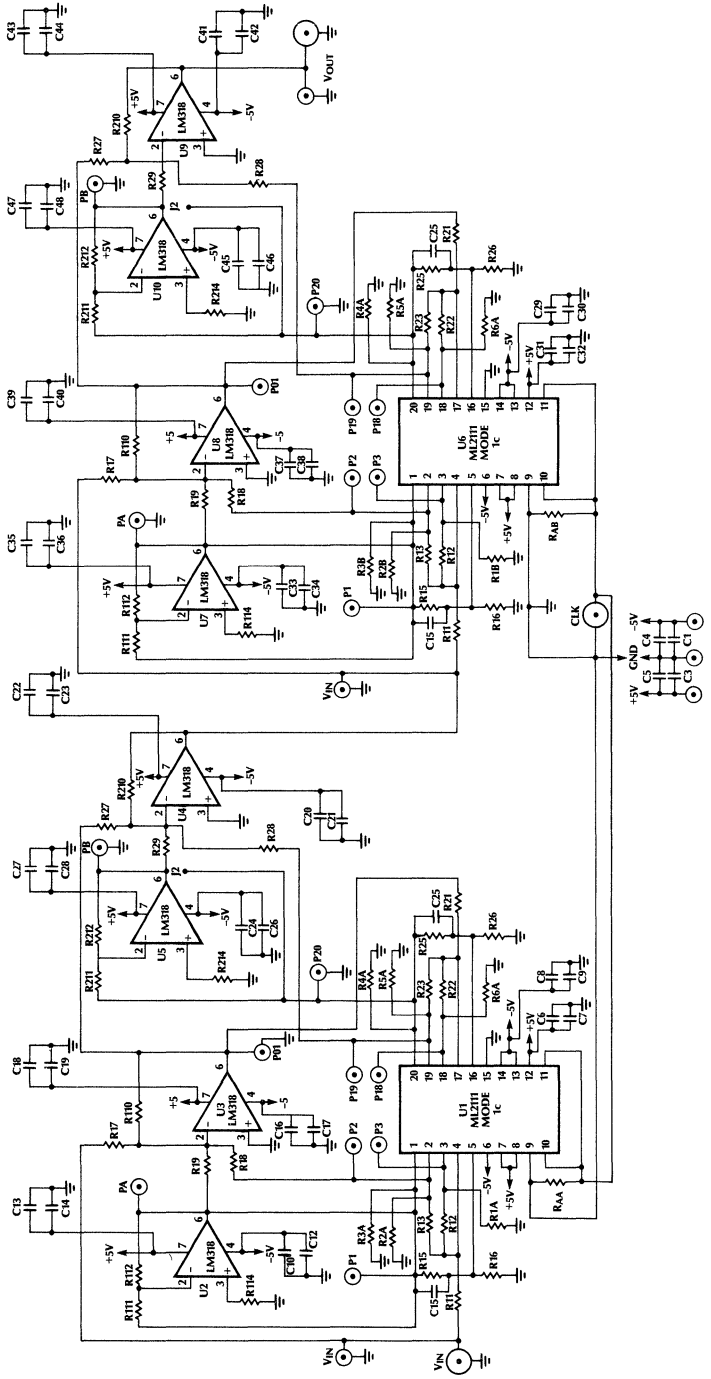
A constant group delay can be achieved by adding allpass equalizer sections to this filter.

Figure 16: Power Spectral Density of the Noise



This plot shows that the pole/zero pairing and order of the bi-quad sections chosen was not optimum as far as noise is concerned. The plot shows that the upper band edge of noise is higher than the lower band edge. A different combination of pole/zero pairing and order pairing would have yielded a flatter noise response and possibly a lower noise value; which would have then improved the S/N ratio. The current design yields S/N of about 40 dB assuming a noise bandwidth from 1 KHz to 179 KHz. Input voltage = 353 mV_{rms}, output noise voltage = 3.14 mV_{rms}.

Figure 17: Schematic Diagram of Printed Circuit Board



(Note that U2 and U7 are not used in this design. This is a general purpose development board and not a minimal component count design).

Figure 18a: PCB Layout Component Side

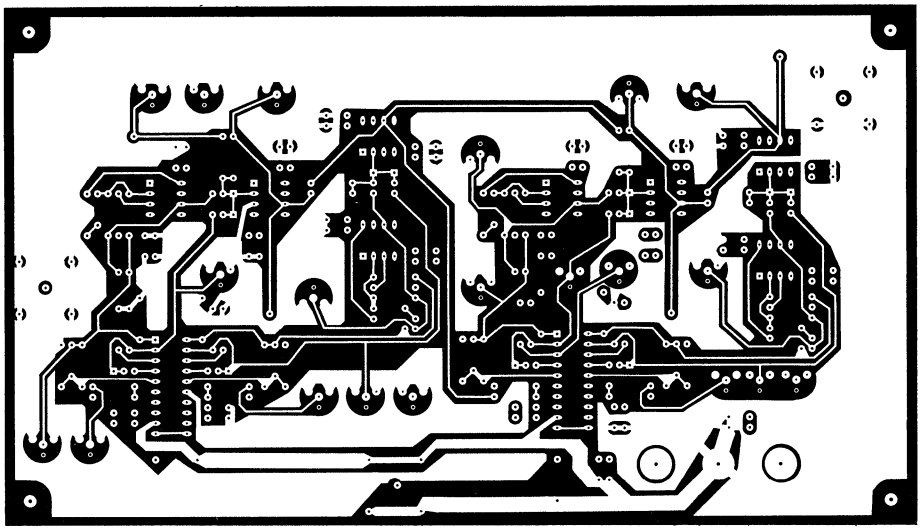
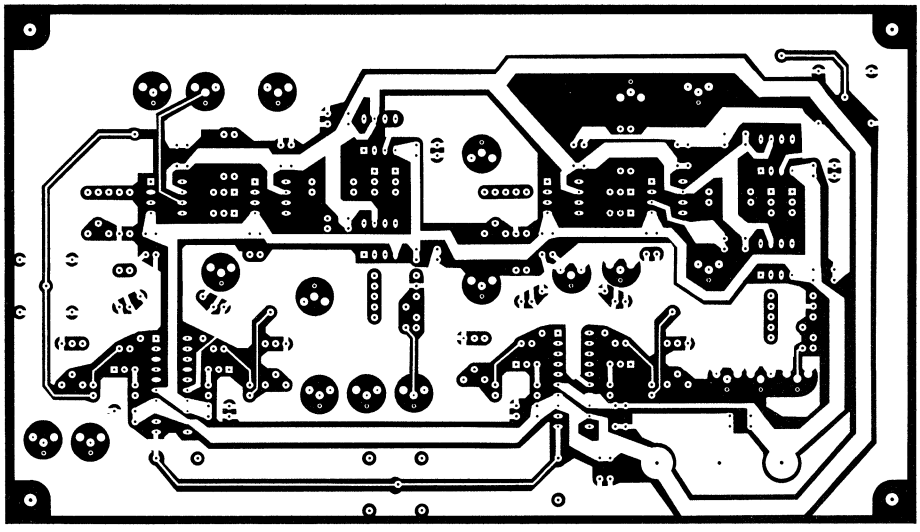


Figure 18b: PCB Layout Solder Side



ML2111 Application Board Parts List

Part #	Value	Note
Resistors		
R1A	1 KΩ	
R2A	500 Ω	
R3A	1 KΩ	
R4A	1 KΩ	
R5A	500 Ω	
R6A	1 KΩ	
R11A	94.5 KΩ	
R12A	2 KΩ	
R13A	66.2 KΩ	100 KΩ Pot
R15A	452 Ω	1 KΩ Pot **
R16A	540 Ω	
R17A	32.4 KΩ	
R18A	15 KΩ	
R19A	4.65 KΩ	10 KΩ Pot*
R110A	3.83 KΩ	10 KΩ Pot*
R111A	OPEN	
R112A	OPEN	
R114A	OPEN	
RAA	100 Ω	
RAB	100 Ω	
R210A	14.3 KΩ	
R211A	5 KΩ	
R212A	5 KΩ	
R214A	2.5 KΩ	
R21A	65 KΩ	
R22A	2 KΩ	
R23A	47.4 KΩ	100 KΩ Pot
R25A	170 Ω	500 Ω Pot**
R26A	830 Ω	
R27A	28.7 KΩ	
R28A	OPEN	
R29A	2.9 KΩ	10 KΩ Pot*
R1B	1 KΩ	
R2B	500 Ω	
R3B	1 KΩ	
R4B	1 KΩ	
R5B	500 Ω	
R6B	1 KΩ	
R110B	9.05 KΩ	
R111B	OPEN	
R112B	OPEN	
R114B	OPEN	
R11B	31.5 KΩ	
R12B	2 KΩ	
R13B	23.3 KΩ	50 KΩ Pot
R15B	389 Ω	1 KΩ Pot**
R16B	600 Ω	
R17B	40 KΩ	
R18B	16.86 KΩ	
R19B	6.35 KΩ	50 KΩ Pot*

Part #	Value	Note
Resistors (Continued)		
R210B	12 KΩ	
R211B	5 KΩ	
R212B	5 KΩ	
R214B	2.5 KΩ	
R21B	25 KΩ	
R22B	2 KΩ	
R23B	21.4 KΩ	50 KΩ Pot
R25B	279 Ω	500 Ω Pot**
R26B	732 Ω	
R27B	100 KΩ	
R28B	OPEN	
R29B	6 KΩ	100 K Pot*
Capacitors		
C15A	OPEN	
C25A	OPEN	
C15B	OPEN	
C25B	OPEN	
C1	100 µF	bypass
C3	100 µF	bypass
C4	0.1 µF	bypass
C5	0.1 µF	bypass
C6	0.1 µF	U1 bypass
C7	0.01 µF	U1 bypass
C8	0.1 µF	U1 bypass
C9	0.01 µF	U1 bypass
C10	OPEN	U2 bypass
C12	OPEN	U2 bypass
C13	OPEN	U2 bypass
C14	OPEN	U2 bypass
C16	0.1 µF	U3 bypass
C17	0.01 µF	U3 bypass
C18	0.1 µF	U3 bypass
C19	0.01 µF	U3 bypass
C20	0.1 µF	U4 bypass
C21	0.01 µF	U4 bypass
C22	0.1 µF	U4 bypass
C23	0.01 µF	U4 bypass
C24	0.1 µF	U5 bypass
C26	0.01 µF	U5 bypass
C27	0.1 µF	U5 bypass
C28	0.01 µF	U5 bypass
C29	0.1 µF	U6 bypass
C30	0.01 µF	U6 bypass
C31	0.1 µF	U6 bypass
C32	0.01 µF	U6 bypass
C33	OPEN	U7 bypass
C34	OPEN	U7 bypass
C35	OPEN	U7 bypass
C36	OPEN	U7 bypass
C37	0.1 µF	U8 bypass
C38	0.01µF	U8 bypass

ML2111 Application Board Parts List (Continued)

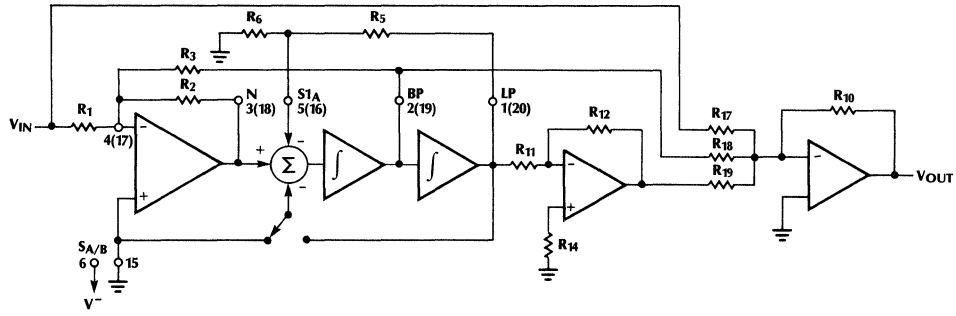
Part #	Value	Note
Capacitors (Continued)		
C39	0.1 μF	U8 bypass
C40	0.01 μF	U8 bypass
C41	0.1 μF	U9 bypass
C42	0.01 μF	U9 bypass
C43	0.1 μF	U9 bypass
C44	0.01 μF	U9 bypass
C45	0.1 μF	U10 bypass
C46	0.01 μF	U10 bypass
C47	0.1 μF	U10 bypass
C48	0.01 μF	U10 bypass
Jumpers		
J1A	IN	
J2A	OUT	
J1B	IN	
J2B	OUT	

Part #	Value	Note
ICs		
U1	ML2111CCP	
U2	OPEN	
U3	LM318H	
U4	LM318H	
U5	LM318H	
U6	ML2111CCP	
U7	OPEN	
U8	LM318H	
U9	LM318H	
U10	LM318H	
Miscellaneous		
20	scope probe sockets	
3	BNC connectors	
3	female banana plugs	
2	20 pin low profile sockets	

* Gain and zero frequency adjustment. May not be needed if application can tolerate slight variations in stop band.
** R5 - In most cases R5 can be replaced by a 1% resistor after trimming has been done.

Appendix A. Flexible Building Block Summary

Lowpass —



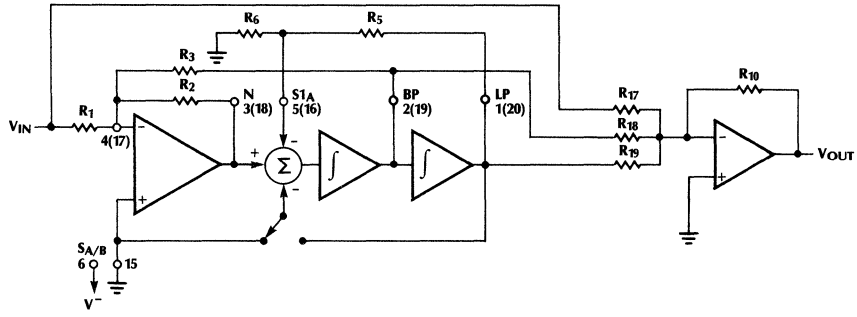
$$f_0 = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_6}{R_5 + R_6}} \; ; \; Q = \frac{R_3}{R_2} \sqrt{\frac{R_6}{R_5 + R_6}}$$

$$f_Z = f_0 \sqrt{1 + \frac{R_2 R_{12} R_{17}}{R_1 R_{11} R_{19}} \left(1 + \frac{R_5}{R_6}\right)} \; ;$$

$$H_{OLP} = \left(-\frac{R_{10}}{R_{17}}\right) \left(1 + \frac{R_2 R_{12} R_{17}}{R_1 R_{11} R_{19}} \left(1 + \frac{R_5}{R_6}\right)\right)$$

$$\frac{R_3}{R_1} = \frac{R_{18}}{R_{17}}$$

Highpass —

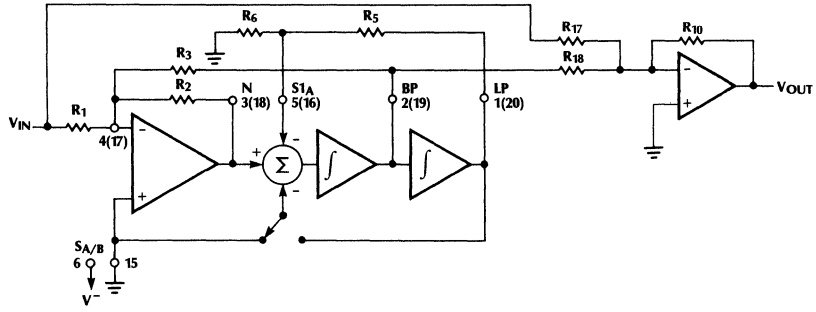


$$f_0 = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_6}{R_5 + R_6}} \; ; \; Q = \frac{R_3}{R_2} \sqrt{\frac{R_6}{R_5 + R_6}}$$

$$f_Z = f_0 \sqrt{1 - \frac{R_2 R_{12} R_{17}}{R_1 R_{11} R_{19}} \left(1 + \frac{R_5}{R_6}\right)} \; ; \; H_{OHP} = -\frac{R_{10}}{R_{17}}$$

$$\frac{R_3}{R_1} = \frac{R_{18}}{R_{17}}$$

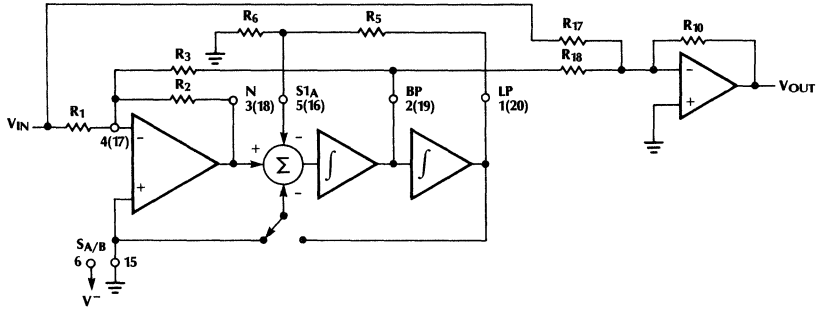
Allpass —



$$f_0 = f_z = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_6}{R_5 + R_6}} \; ; \; Q = \frac{R_3}{R_2} \sqrt{\frac{R_6}{R_5 + R_6}}$$

$$H_{OAP} = -\frac{R_{10}}{R_{17}} \; ; \; \frac{R_{17}R_3}{R_{18}R_1} = 2$$

Notch —



$$f_N = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_6}{R_5 + R_6}} \; ; \; Q = \frac{R_3}{R_2} \sqrt{\frac{R_6}{R_5 + R_6}}$$

$$H_{ON1}\,(f \rightarrow 0) = H_{ON2}\,(f \rightarrow f_{CLK}/2) = -\frac{R_{10}}{R_{17}} \; ; \; \frac{R_3}{R_1} = \frac{R_{18}}{R_{17}}$$

Appendix B. Derivation of Flexible Building Block Transfer Function

$$V_N = -\frac{R_2}{R_1} V_{IN} - \frac{R_2}{R_3} V_{BP}$$

$$V_{BP} = \frac{\left(V_N - \frac{R_6}{R_5 + R_6} V_{LP}\right)}{s} \omega_1$$

$$V_{LP} = \frac{V_{BP}\,\omega_1}{s}$$

$$\frac{s\,V_{BP}}{\omega_1} = -\frac{R_2}{R_1} V_{IN} - \frac{R_2}{R_3} V_{BP} - \frac{R_6}{R_5 + R_6} \frac{V_{BP}\,\omega_1}{s}$$

$$V_{BP}\left[\frac{s}{\omega_1} + \frac{R_2}{R_3} + \frac{R_6}{R_5 + R_6}\frac{\omega_1}{s}\right] = -\frac{R_2}{R_1} V_{IN}$$

$$\frac{V_{BP}}{V_{IN}} = \left(-\frac{R_3}{R_1}\right) \frac{\frac{R_2}{R_3} s\omega_1}{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6} \omega_1^2}$$

$$V_O = -\frac{R_{10}}{R_{17}} V_{IN} - \frac{R_{10}}{R_{18}} V_{BP} + \frac{R_{12}}{R_{11}}\frac{R_{10}}{R_{19}} V_{LP}$$

$$f_1 = \frac{f_{CLK}\,2\pi}{50} \qquad H_{OBP} = -\frac{R_3}{R_1}$$

$$f_0 = \sqrt{\frac{R_6}{R_5 + R_6}}\,\frac{f_{CLK}\,2\pi}{50} \qquad Q = \frac{R_2}{R_3}\sqrt{\frac{R_6}{R_5 + R_6}}$$

$$\omega = 2\pi f$$

$$V_O = -\frac{R_{10}}{R_{17}} V_{IN} - \frac{R_{10}}{R_{18}}\left(-\frac{R_2}{R_1}\right) \frac{s\omega_1\,V_{IN}}{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6}\omega_1^2} + \frac{R_{12}R_{10}}{R_{11}R_{19}}\left(-\frac{R_2}{R_1}\right) \frac{\omega_1^2\,V_{IN}}{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6}\omega_1^2}$$

$$V_O = \left(-\frac{R_{10}}{R_{17}}\right)\left[\frac{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6}\omega_1^2 - \frac{R_{10}R_2R_{17}}{R_{18}R_1R_{10}} s\omega_1 + \frac{R_{12}R_2R_{17}}{R_{11}R_1R_{19}}\omega_1^2}{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6}\omega_1^2}\right]$$

$$\frac{V_O}{V_{IN}} = \left(-\frac{R_{10}}{R_{17}}\right)\left[\frac{s^2 + \frac{R_2}{R_3}\left(-\frac{R_{10}}{R_{17}}\right)\left[\frac{R_{10}R_3}{R_{18}R_1} - \frac{R_{10}}{R_{17}}\right] s\omega_1 + \left[1 + \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)\right]\frac{R_6}{R_5 + R_6}\omega_1^2}{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6}\omega_1^2}\right]$$

$$\frac{V_O}{V_{IN}} = \left(-\frac{R_{10}}{R_{17}}\right)\left[\frac{s^2 + \frac{R_2}{R_3}\left[1 - \frac{R_{17}}{R_{18}}\frac{R_3}{R_1}\right] s\omega_1 + \left[1 + \frac{R_2R_{12}R_{17}}{R_1R_{11}R_{19}}\left(1 + \frac{R_5}{R_6}\right)\right]\frac{R_6}{R_5 + R_6}\omega_1^2}{s^2 + \frac{R_2}{R_3} s\omega_1 + \frac{R_6}{R_5 + R_6}\omega_1^2}\right]$$

Micro Linear

Application Note 5

ML2200, ML2208 Software Driver

1.0 Introduction

This application note presents a very simple software driver for the ML2200/ML2208 Data Acquisition Peripheral. As mentioned in the data sheet, under section 6.0 "Methods of Data Transfer to the Microprocessor", there are several ways to handle the A/D converted data output from the ML2200/ML2208; 1) Data on Demand, 2) Polling; 3) Interrupt, or 4) DMA. This application note presents a driver for Data on Demand.

An application using Data on Demand requires the A/D converted data at arbitrary times, as opposed to the other three methods of data transfer which requires the microprocessor to periodically read the data. The ML2200/ML2208 operating in a Data on Demand mode is not running continuously. Data on Demand would be more characteristic of a data acquisition application rather than a signal processing application which would need to sample a signal periodically in order to be able to reconstruct it.

The driver is written in pseudo code, which is no particular language but should be easily translatable to any computer language. It is a step-by-step process of reading and writing values to ML2200/ML2208 registers.

Four modules are covered: Initialization, Activate Conversion and Read Data, Self Test Diagnostic, Self Calibration Diagnostic, Power Down and Power Up Modules. Initialization covers power-up procedures and optionally may call Self Test and Self Calibration Diagnostic modules. Activate Conversion is the steady state module that is called each time the A/D data is desired. Power Down and Power Up are used only if this capability is desired.

Initialization Mode (Power-On Initialization)

```
1)  Power on
2)  Write (40H) to Control Register          ; Reset
3)  Write (80H) to Control Register          ; Set Calibration
4)  Wait 16,520 external clocks
5)  Read Status Register
6)  Is CLCP = 1, Yes: continue, No: go back to step 5
7)  Write (40H) to Interrupt Acknowledge Register   ; CLCPAK
-)  Call (Self Calibration Diagnostic Module)       ; OPTIONAL

                                             ; Use Program shown on last page figure 1

8)  Write (88H) to Index Register            ; Point to first
9)  Write (08H) Window High Reg              ; instruction RAM use
10) Write (26H) Window Low Reg               ; auto increment
11) Write (01H) Window High Reg
12) Write (26H) Window Low Reg
13) Write (02H) Window High Reg
14) Write (26H) Window Low Reg
15) Write (03H) Window High Reg
16) Write (26H) Window Low Reg
17) Write (04H) Window High Reg
18) Write (26H) Window Low Reg
19) Write (05H) Window High Reg
20) Write (26H) Window Low Reg
21) Write (06H) Window High Reg
22) Write (26H) Window Low Reg
23) Write (87H) Window High Reg
24) Write (26H) Window Low Reg
```

25) Write (0AH) to Control Reg ; set MSTR bit so
; that pulse goes out
; each conversion and
; put in DMA mode to
; facilitate reading
; data.
26) Write (0BH) to Control Reg ; Set Run bit
27) Call (Self Test Diagnostic Module) ; OPTIONAL

; end of initialization module.

Activate Conversion and Read Data Module

(Called each time A/D converted data is desired)

1) Read status register
2) Is ISQ = 1? Yes: continue, No: go back to step 1
3) Write (10H) to Interrupt Acknowledge Reg ; acknowledge ISQ
4) Wait (8 × 31.4 μs = 251.2 μs)
5) Read status register
6) DBR = 1? Yes: continue; No: go back to step 5
7) Read Window Low Register save as High Byte ; DMA mode allows
Read Window Low Register save as Low Byte ; μP to read High and
8) Go back to step 7 seven more times ; Low bytes at same
9) Return ; address

Self Test Diagnostic Module

(Assumes the program in figure 1 is already loaded in the Instruction RAM as performed in the initialization module. When the SLFT bit is set, the diagnostic program is the same one as shown on page 22 of the data sheet. This module sets the SLFT bit, starts a conversion, then checks the data for the results.)

1) Read Control Register
2) Or (20H) ; Set SLFTST in
; Control Register
3) And (7FH) ; don't set CAL bit
4) Write back into control register
5) Call (ACTIVATE CONVERSION AND READ DATA MODULE)
6) Check selftest data ; Data 0 = 0
; Data 1 = +1
; Data 2 = –1
; Data 3 = 0

(Note: these values may not be exact due to the potential noise in the system)

7) Read Control Register
8) And (5FH) ; clear SLFT bit
9) Write back into control register
10) Return

Self Calibration Diagnostic Module

(This can be used to verify that the part is properly calibrated. It should be called between steps 7 and 8 in the initialization module. This test is not necessary since each production part is fully tested before it is shipped.)

1) Write (08H) to Index Register ; Point to the first
2) Write (88H) to Window High Register ; Instruction
3) Write (60H) to Window Low Register ; Load with RDCAL
4) Write (01H) to Control Register ; Set RUN bit
5) Read Status Register ; Wait for ISQ
6) Is ISQ = 1? Yes: continue, No: go back to step 5
7) Write (10H) to Interrupt Acknowledge Register ; Start Program
8) Read Status Register
9) Is DBR = 1? Yes: continue, No: go back to step 8 ; Wait for Data
10) Write (00H) to Index Register ; Point to Data
11) Read Window Low Register
12) Is Data = 0FFH? Yes: Failed Calibration, No: continue
13) Write (00H) to Control Register ; Take out of Run Mode
14) Return

Power Down Module

1) Read Control Register ; Clear the Run Bit
2) And with (7EH)
3) Write Control Register
4) Read Status Register and Process any conditions
5) Write (0FFH) to Interrupt Acknowledge Register ; Clear all Interrupt
6) POWER DOWN (PDN pin goes low) ; Conditions
7) Return

Power Up Module (Coming from a Power Down State)

1) POWER UP (PDN pin goes high)
2) Wait (10 msec)
3) Read Control Register ; Set the Run Bit
4) Or with (01H)
5) And with (7FH)
6) Write to Control Register
7) Return

	Last	ALRMEN	Mode	CHAN	Cycle	Gain	REF
SEQ0	0	0	Intra Sequence Pause	CH0	13	1	Internal
SEQ1	0	0	Immed Execute	CH1	13	1	Internal
SEQ2	0	0	Immed Execute	CH2	13	1	Internal
SEQ3	0	0	Immed Execute	CH3	13	1	Internal
SEQ4	0	0	Immed Execute	CH4	13	1	Internal
SEQ5	0	0	Immed Execute	CH5	13	1	Internal
SEQ6	0	0	Immed Execute	CH6	13	1	Internal
SEQ7	1	0	Immed Execute	CH7	13	1	Internal

Figure 1. ML2208 Program Used in Driver

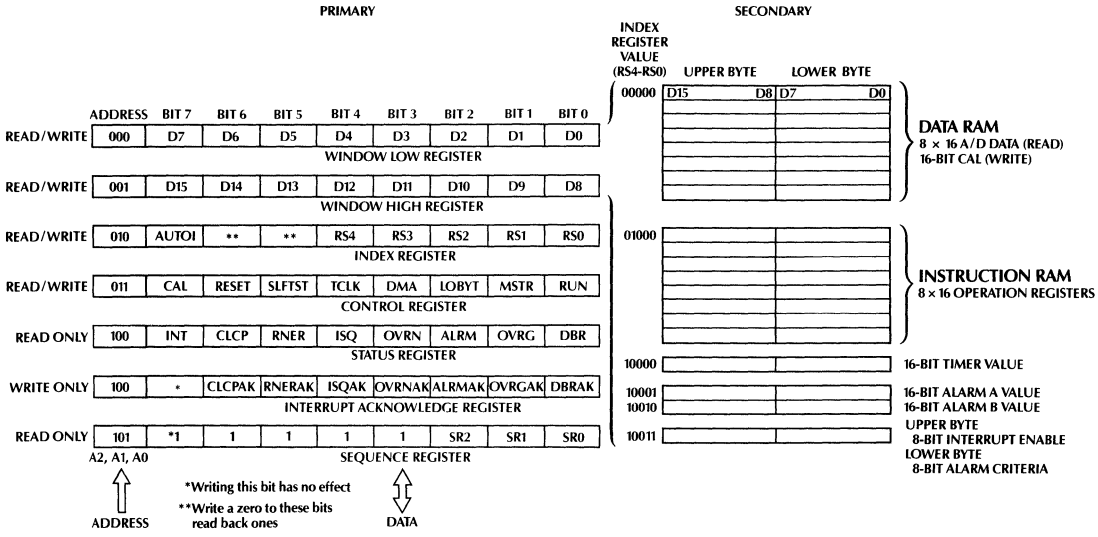


Figure 2. ML2200/ML2208 Registers

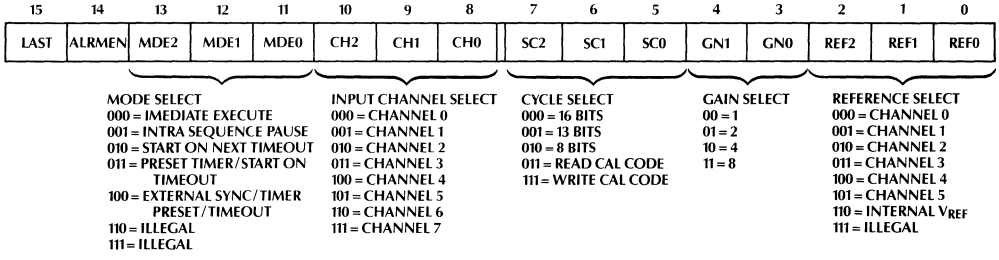


Figure 3. ML2208 Bit Map of Instruction RAM

Micro Linear

Application Note 6

Fiberoptics

Introduction

Although fiberoptic technology has been around for some time, its cost and the lack of standardization has hindered its widespread application, until recently. The introduction of new integrated circuits developed specifically for fiberoptic systems has lowered the costs, making fiberoptic links more competitive. Applications in Telephony, LANs, WANs, and point to point high speed interfaces, have helped make fiberoptics one of the fastest growing segments in the electronics market.

Micro Linear's fiberoptic products can be used to implement a range of different fiberoptic interfaces. Data rates up to 100 Megabaud which are compatible with ECL or TTL are achievable using a single 5 volt supply. Most of the applications for these products require bandwidths above 1MHz, where the quality of the interface can be compromised with a poor implementation. With this in mind, having a thorough understanding of fiberoptics will significantly contribute to the success of a circuit design. This application note will address the transmit and receive circuits, some important PC board layout techniques, and will conclude with a sample circuit and board layout.

Fiberoptics

Fiberoptic systems have several key advantages over their wire equivalents, which account for the continued effort to make them practical in more applications. The most significant advantage is the low level of attenuation seen with high frequency signals. This feature allows a higher degree of multiplexing than is achievable using wire. This is exactly what is needed for long distance telephone lines and computer networks. Other attractive features include a lack of RFI radiation and a low sensitivity to EMI noise. These characteristics make it easier to meet FCC regulations and increase the security of data transmissions.

In a fiberoptic system (figure 1) digital data is coded into a serial bit stream represented by bursts of light from a laser diode or LED. This light is channeled by the fiber to a PIN photodiode at the receiver which is sensitive to the frequency of the light transmitted. Because light effects the reverse current flow through a PIN photodiode, a transimpedance amplifier is required to convert this current to a voltage and boost the low level signal to something usable. A quantizing circuit usually follows because variable fiber lengths and conditions will distort the signal. The Quantizer squares the signal and conforms to standard interface levels (ECL or TTL).

Fiberoptics is not a perfect interface, though. The signal level can be attenuated by insertion loss at the transmitter and receiver, connector loss, and transmission loss. These losses limit the maximum length of the fiber and affect the requirements of the transmitter and receiver. In order to accommodate a worst case situation, a flux budget should be developed so that minimum circuit performance levels can be ascertained.

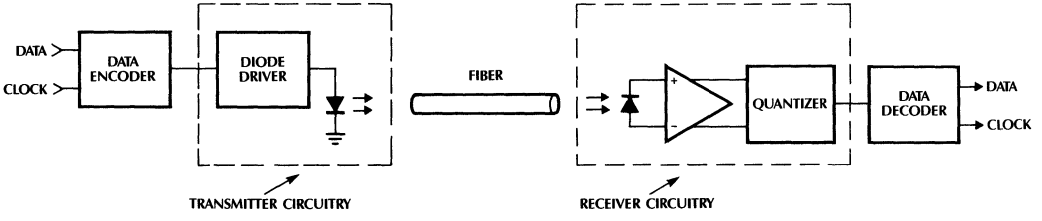


Figure 1.

Defining a Flux Budget

$$10 \log \left(\frac{\phi_T}{\phi_R}\right) = \alpha_O L + \alpha_{TC} + \alpha_{CR} + n\alpha_{CC} + \alpha_M$$

A flux budget is a mathematical representation of the optical power in a fiberoptic system. It accounts for connector losses, attenuation due to fiber length, and a safety margin defined by the designer. Defining this budget is one of the first things that should be done when designing a fiberoptic link.

Each of the terms is defined as follows:

ϕ_T is the flux (μW) available from the transmitter
ϕ_R is the flux (μW) required by the receiver
α_O is the fiber attenuation constant (dB/km)
L is the fiber length (km)
α_{TC} is the transmitter-to-fiber coupling loss (dB)
α_{CC} is the fiber-to-fiber loss (dB) for in-line connectors
n is the number of in-line connectors
α_{CR} is the fiber-to-receiver coupling loss (dB)
α_M is the safety margin (dB)

A graphical representation of the flux budget is shown in figure 2. Option (a) depicts the use of in-line connectors. Option (b) is without them.

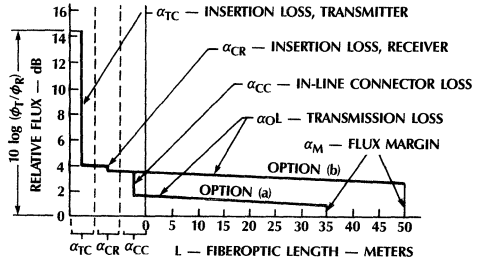


Figure 2.

To keep power consumption at a minimum, the appropriate starting point is the minimum acceptable signal level at the receiver. This minimum received power level, summed with several interface losses gives the minimum output power of the LED. If the fiber length can vary in a given system then the dynamic range of the receiver is important and the maximum received power must also be calculated.

Dynamic Range

The dynamic range of the receiver must be large enough to accommodate all the variables a system may present. Figure 3 shows an example dynamic range calculation for transmission distances ranging from 10 meters to 1000 meters with 12.5dB/km cable, and up to two in-line connectors.

α_{LED} = LED output variation	= 7.0dB
α_{LDC} = LED driver variation	= 2.2dB
$\alpha_O L$ = 1km × 12.5dB/km	= 12.5dB
$n\alpha_{CC}$ = 2 × 2dB	= 4.0dB
α_M	= 3.0dB
Thermal Variations	= 1.0dB
Dynamic Range	29.7dB

Figure 3.

The Circuit Design

The combination of low receiver input sensitivity with significant dynamic range requires the receiver to have two important features: amplitude control and AC coupling.

An offset voltage in the receiver will reduce its sensitivity by not allowing low level signals to trigger the digital output circuit. The circuit in figure 4 contains both AC coupling between the transimpedance and limiting amplifiers, and a DC restoration loop around the limiting amplifiers. These two features keep the offset voltage through the receiver to an absolute minimum, thus maximizing sensitivity.

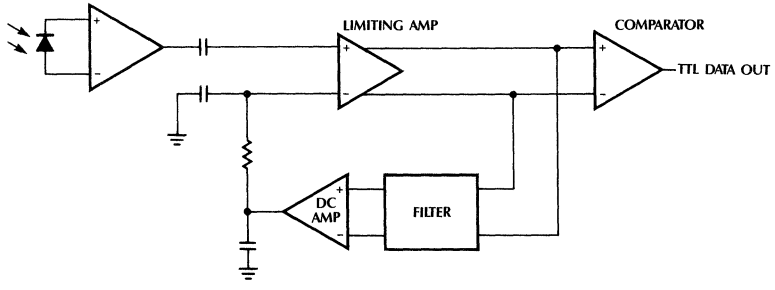


Figure 4.

In order to handle a wide dynamic range, like 50dB, special attention must be given to the receiver circuit design. Applying a large input signal to a typical amplifier can cause the transistors in the signal path to saturate resulting in pulse width distortion and reduced bandwidth. Some technique of controlling the amplitude must be incorporated in order to protect the signal integrity.

Amplitude control can be achieved with either an AGC circuit or with the use of limiting amplifiers. An AGC circuit keeps the transistors out of saturation by reducing the gain of the circuit as the signal amplitude increases. A limiting amplifier simply limits the signal amplitude to a point before saturation. This technique results in a simpler, higher bandwidth design and so was chosen by Micro Linear.

Data Format

The data format is important since it affects the bandwidth and duty cycle which the interface must accomodate. There are many ways to code data in a serial format. Some codes allow unlimited consecutive symbols while others do not. Those that do not are called Run-Length-Limited (RLL) codes. A fiberoptic interface which incorporates AC coupling to increase sensitivity can only pass RLL type codes. The particular run-length-limited code chosen must be considered carefully since it will affect the bandwidth of the system.

Manchester code is popular in AC coupled systems because it has a 50% duty cycle and can be encoded and decoded with relatively simple circuits. In Manchester code two symbols are used for each bit transmitted. This doubles the fundamental frequency which the interface must handle. A more efficient RLL code is 4B5B. This code uses 5 symbols to send 4 bits. This represents an increase in efficiency from 50% (Manchester) to 80% (4B5B). A fiberoptic interface which will transmit 40 Megabits per second using 4B5B coding must accomodate 50 Megabaud (symbols per second). Since there are always 2 symbols per cycle the minimum system bandwidth is 25 Megahertz. If Manchester code was used to transmit 40 Megabits per second the interface would have to handle 80 Megabaud or a minium bandwidth of 40 Megahertz.

Bandwidth

From the example just described you can see how the code chosen effects the minimum bandwidth of the fiberoptic interface to be designed. The optimum system bandwidth is actually somewhat higher though due to four conflicting concerns: noise, intersymbol interference, power, and bit error rate.

If an interface were designed with a 3dB bandwidth equal to the minimum bandwidth as described above, level transitions would be smooth, like a sine wave. This is not desirable for a digital signal. Also, smooth rise and fall times will cause interference between adjacent symbols resulting in a distortion of the output signal. This is known as intersymbol interference. A fiberoptic interface with a higher bandwidth will have faster rise and fall times and less intersymbol interference. On the other hand, a higher bandwidth will increase the noise on the output signal. When you combine these two opposing effects with the desire for low power and a low BER (Bit Error Rate) (which also conflict), an optimum bandwidth can be derived. The curve in figure 5 indicates the optimum bandwidth is about 50% higher than the minimum bandwidth.

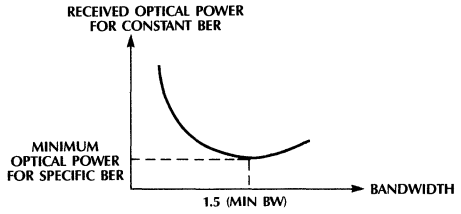


Figure 5.

Transmitter Design

The light source can be either a laser diode or an LED. Because a laser diode has such a narrow spectrum of radiant light it is called a Single Mode light emitter. Multi Mode light emitters radiate a wider spectrum of light. LEDs are Multi Mode and as such suffer from a higher level of chromatic dispersion, caused by different propagation velocities for light of different wavelengths. This is the dominant bandwidth limiting factor for LED driven fiberoptic links. Light emitting diodes have an emission spectrum on the order of 40 to 60nm full width at half maximum amplitude centered at 820nm. On the other hand, LEDs are much cheaper than laser diodes and can be modulated in the 100MHz range, making them suitable for short to medium distance communications such as LANs and point-to-point computer interfaces.

LEDs are current driven devices so a current modulation circuit is needed to use the LED as a data transmitter. In applications where the data rate is less than 10MHz a circuit similar to figure 6 will be adequate to drive the LED without a significant amount of pulse width distortion. Unfortunately, LEDs do not turn on or off linearly nor are their rise and fall times equal. For data rates above 10MHz these characteristics need to be considered in order to get the best possible performance.

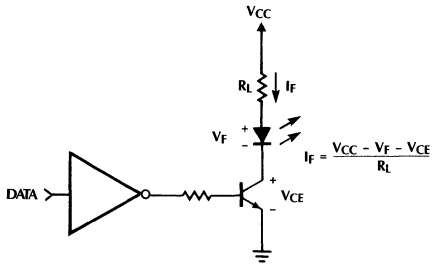
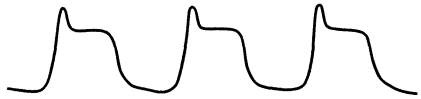


Figure 6.

Two techniques which can be used to improve the turn-on time of an LED are "pre-bias" and "drive current peaking". Pre-bias is a small forward voltage applied to the LED in the "off" state. This voltage prevents the junction and parasitic capacitances from discharging completely when the LED is in the "off" state, thus reducing the amount of charge that the driver must transfer to turn the emitter back on. Drive current peaking is a momentary increase in LED forward current that is provided by the driver during the rising and falling edges of the current pulses that are used to modulate the emitter. The time constant of this peaking circuit needs to be equal to the minority carrier lifetime of the emitter so that the rise and fall times will be improved without causing excessive overshoot of the optical pulses. Figure 7 shows the problems which can result from excessive peaking.



OPTICAL OVERSHOOT DUE TO EXCESSIVE PEAKING OF THE LED DRIVE CURRENT

Figure 7.

The circuit in figure 8 implements both the pre-bias and peaking techniques described above. When the DATA signal is low the voltage divider created by R_1 and R_2 can be set-up so the voltage between R_1 and R_2 is slightly less than the LED turn-on voltage. This pre-bias voltage prevents the LED capacitance from discharging completely which allows the LED to turn on faster because less time is required to completely charge the junction capacitance. The time to completely charge the LED can be reduced further by increasing the amount of current flowing in the LED duirng turn-on. The capacitor in this circuit has the effect of connecting R_3 in parallel with R_2 for a short time during level transitions. This momentary condition allows additional current to flow through R_3 and the LED. By matching the R_3C time constant to the minority carrier lifetime of the LED, *peak* performance is achieved.

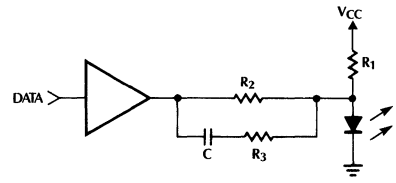


Figure 8.

LEDs are characteristically harder to turn off than to turn on. This phenomenon is commonly refered to as the long-tailed response, and is depicted in figure 9 as it relates to transmitted optical power. Circuits such as the one in figure 6 exhibit this problem because there is no low impedance path to dissipate the stored charge in the LED when turning off. In order to compensate for this an active pull down configuration should be used. For the circuit in figure 8, this can be achieved by using an input buffer with a totem pole output structure. When the DATA signal is low, the lower transistor of the totem pole is active. Acting as a current sink, this device provides a low impedance path for the charge stored in the LED junction, reducing pulse-width distortion and the magnitude of the long tail.

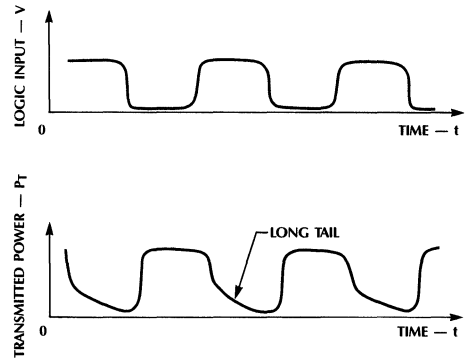


Figure 9.

Receiver Design

For optimum performance the receiver needs to combine a wide dynamic range (about 50dB), high sensitivity (down to 1μW), high bandwidth (50MHz) and compatibility with standard digital interfaces (ECL or TTL). Another feature which is required in some fiberoptic systems is a Link Monitor. This circuit monitors the input level and sets a flag and/or disables the digital output when the input falls below a predetermined point.

The four major functional blocks of a receiver are the optical to current conversion, the current to voltage conversion, the analog to digital conversion, and the Link Monitor. A PIN photodiode and a transimpedance amplifier can be used to perform the first two functions while the third and fourth require several discrete standard devices and a significant amount of design effort or one of Micro Linear's Quantizer products.

There are several manufacturers of discrete PIN photodiodes and transimpedance amplifiers which are suitable for this application. Some of these manufacturers offer both functions in a single module compatible with fiberoptic connectors. These modules, like the Hewlett Packard HFBR-24X6, isolate the most noise sensitive section of the receiver, the PIN photodiode to transimpedance amplifier connection, and protect it from outside influences. In addition, they are relatively low cost, and eliminate the need to design the fiberoptic connector hardware.

The output of these receiver modules is a low level analog voltage which is directly proportional to the incident optical power. This signal needs to be amplified, squared-off, and appropriately level shifted (for ECL or TTL outputs). As described earlier, a limiting amplifier can be used in this application to accomodate a wide input dynamic range while maintaining a high bandwidth.

Building a high speed analog to digital conversion circuit which must perform over a wide dynamic range with low offsets using off-the-shelf components is difficult. Furthermore, a worst case analysis may be impossible because some of the parameters critical to a fiberoptic receiver design, such as input offset and input referred noise are not always included in the discrete component specifications. The typical bandwidth of these devices may be known but the minimum is not always guaranteed, yet this is required for a worst case analysis.

The ML4621 Quantizer

The ML4621 Quantizer eliminates these problems by providing a monolithic solution. This product includes a limiting amplifier front end, a comparator output section and a Link Monitor. The differential data path between the amplifier section and the comparator section is available to the user for filtering or wave shaping. In addition, both ECL and TTL outputs are available, and the Link Monitor peak detector can be controlled with an external current source or the value of the peak detector capacitor.

Input Amplifier Section

The ML4621 has a two stage limiting amplifier with a DC restoration feedback loop. Figure 10 shows this input circuitry in detail. The two input coupling capacitors C_1 and C_2 perform two important functions. First they eliminate any offset voltage created by the transimpedance amplifier, and in addition they create a high pass filter at the input of the Quantizer. This filter establishes the low corner frequency, f_L, of the Quantizer's 3dB bandwidth.

$$f_L = \frac{1}{2\pi\ 8000\ C} \qquad (C = C_1 = C_2) \qquad (1)$$

8000 represents the parallel combination of the DC bias setting resistors 10K and 35K. Using a 0.1μF capacitor for C_1 and C_2 establishes a corner frequency at about 200Hz. C_4 and C_5 control the high corner frequency, f_H.

$$f_H = \frac{1}{2\pi\ 425\ C} \qquad (C = C_4 = C_5) \qquad (2)$$

425 represents the internal impedance at nodes CF1 and CF2. Using a 20pF capacitor for C_4 and C_5 establishes a corner frequency at about 19MHz. If CF1 and CF2 are left open the high corner frequency will be >50MHz for the ML4621. Equation 2 applies when 2 capacitors are tied between CF1 and CF2 to the ground. If one capacitor is used between CF1 and CF2, the value derived for C should be divided by two.

The bandwidth of the receiver, as defined by $f_H - f_L$, can be adjusted to the particular needs of different systems. The high pass filter not only eliminates DC offsets but also reduces any low frequency power supply noise picked-up in the transimpedance amplifier and associated traces. The low pass filter reduces high frequency noise which directly effects the signal to noise ratio and thus the sensitivity of the receiver. Since these circuits were designed for maximum bandwidth, some band limiting should be used as indicated in figure 5 to maximize sensitivity.

Although the input is AC coupled, the offset voltage *within* the limiting amplifiers will be present at V_{OUT+} and V_{OUT-}. This is represented by V_{OS} in figure 11. In order to reduce this error a DC feedback loop is incorporated. First, the DC component of V_{OUT+} and V_{OUT-} is developed through an RC filter of 25K and 10pF. Then a difference amplifier circuit with a gain of 10 is used to provide a single ended signal, stored in C_3, which can be fed back into the inverting input terminal. This negative feedback loop nulls the offset voltage, forcing V_{OS} to be zero.

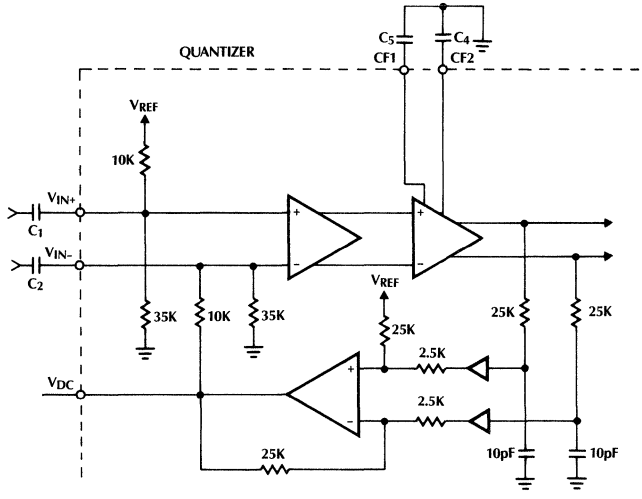


Figure 10.

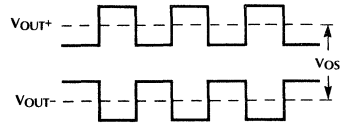


Figure 11.

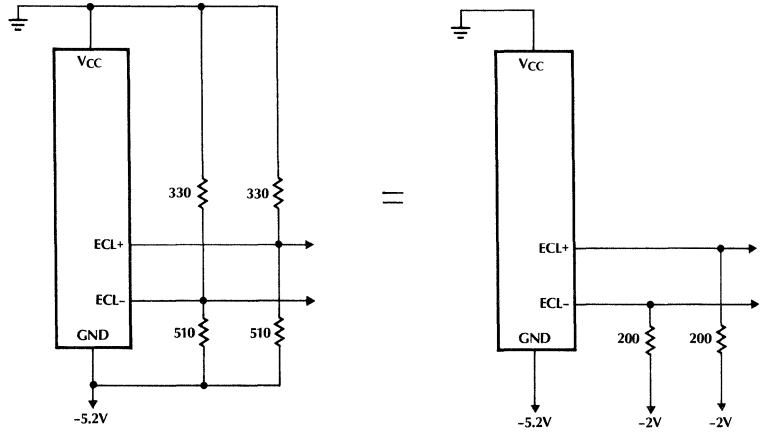


Figure 12.

The limiting amplifiers have a maximum output voltage swing of about 700mV$_{P-P}$. Since the gain of the amplifiers is 75, input signals greater 9mV will be clipped at about 2.7V and 3.4V. Typically this signal is connected directly to the comparator inputs. If some filtering or wave shaping is desired between the amplifier output and the comparator input, the ML4621 should be used since these nodes are brought out to pins. If AC coupling is involved, the DC bias must be reestablished between (GND + 2V) and (V_{CC} – 1V). Also, the loading on V_{OUT+} and V_{OUT-} should be kept below 3mA, and be aware that CMP+ and CMP– will sink about 25μA.

Output Comparator Section

The ML4621 has both ECL and TTL outputs. If the ECL output is to be used, the power to the TTL output section can be removed by connecting V_{CC} TTL and GND TTL to V_{CC}. This will reduce the V_{CC} supply current by 5 to 10mA. The Quantizer can be powered by –5.2V (V_{CC} = 0V and GND = –5.2V), which produces standard ECL output levels, or +5V (V_{CC} = +5V and GND = 0V), providing raised ECL levels. The ECL outputs on the ML4621 can source up to 10mA, so a 200Ω load tied to –2V (below V_{CC}) can be accommodated. If a –2V supply is not available, connecting the ECL output to GND through a 510Ω resistor, and to V_{CC} through a 330Ω resistor will provide the same voltage swing as 200Ω tied to –2V (see figure 12).

The output comparator is gated with the $\overline{\text{CMP ENABLE}}$ pin which is active low. When $\overline{\text{CMP ENABLE}}$ is high, ECL+ is held high, ECL– is held low, and TTL OUT is held high. If the Quantizer is powered by +5V and ground then any external TTL compatible signal can be used to control this pin. If a –5.2V supply is used, the signal should be appropriately level shifted. In either case, the $\overline{\text{TTL LINK MON}}$ pin can be used to drive the $\overline{\text{CMP ENABLE}}$ pin directly. The $\overline{\text{TTL LINK MON}}$ is an output signal from the Minimum Signal Discriminator circuit providing the Link Monitor function.

Link Monitor Section

The $\overline{\text{TTL LINK MON}}$ and $\overline{\text{ECL LINK MON}}$ pins both provide an output signal indicating when the input data signal is below a user defined acceptable level. Under normal operating conditions this output will be low, indicating the data is of acceptable amplitude. The voltage levels on the $\overline{\text{TTL LINK MON}}$ pin are TTL compatible if the power supply is +5V. With a –5.2V supply the $\overline{\text{ECL LINK MON}}$ output pin will provide single ended ECL levels. The $\overline{\text{TTL LINK MON}}$ pin can also be used to drive an LED, providing a visible link status indicator. This pin can sink up to 10mA.

The Minimum Signal Discriminator circuit contains a peak detector, a comparator, and output level shift circuitry (figure 13). The droop rate of the peak detector is:

$$\frac{dV}{dt} = \frac{I_{ISET}}{C_6} \qquad (3)$$

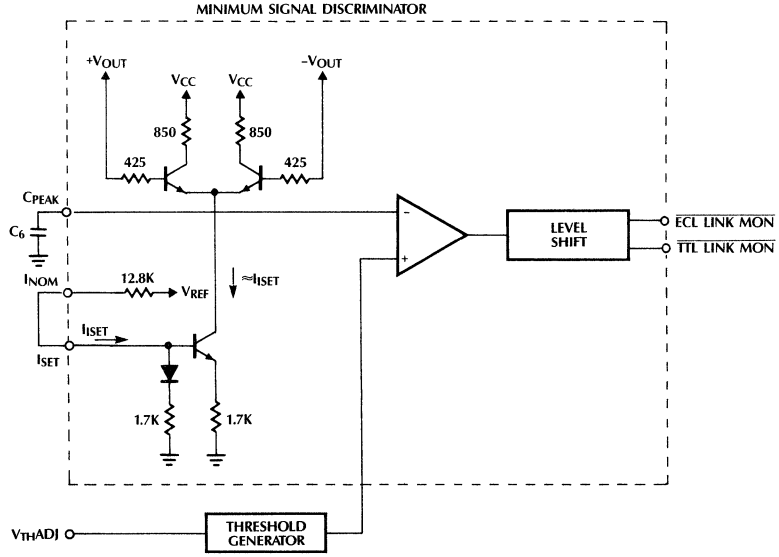


Figure 13.

The peak detector droop rate can be controlled adjusting either the value of C_6 at the C_{PEAK} pin or I_{ISET} at the I_{SET} pin. If I_{NOM} is connected to I_{SET}, I_{ISET} will be 125μA. The droop rate for this product can be adjusted with C_6. The ML4621 has these extra pins, which allows the user to set I_{ISET} with an external resistor, R_{EXT}, tied between I_{SET} and V_{CC}. I_{ISET} would then be:

$$I_{ISET} = \frac{V_{CC} - 0.7}{R_{EXT} + 1700} \quad (4)$$

The output of the peak detector is a DC voltage proportional to half the peak-to-peak voltage between V_{OUT+} and V_{OUT-}. If this signal is larger than the voltage provided by the Threshold Generator circuitry the TTL LINK MON and ECL LINK MON pins will both be low.

The Threshold Generator level shifts the reference voltage at $V_{TH}ADJ$ through a circuit which has a temperature coefficient matching that of the limiting amplifiers. This improves the accuracy of the Link Monitor over temperature. The relationship between $V_{TH}ADJ$ and V_{TH} (the minimum voltage at the input which will trigger the Link Monitor) is:

$$V_{TH}ADJ = 600V_{TH} + 0.7 \quad (5)$$

In this equation V_{TH} is the *peak* value of the input signal. The operating range over which these equations apply is indicated by the graphs in figure 14. The on-chip reference voltage, V_{REF}, can be tied directly to

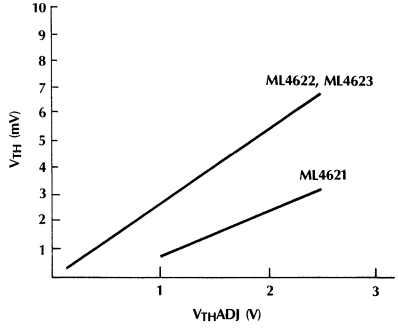


Figure 14.

$V_{TH}ADJ$ to set the threshold level. This 2.5V low impedance source will set the threshold at its maximum allowable level as indicated in the graph. A lower threshold level can be set by dividing down V_{REF} with a resistor string, as in figure 15. The $V_{TH}ADJ$ voltage can be calculated as follows:

$$V_{TH}ADJ = V_{REF}\frac{R_2}{R_1 + R_2} \quad (6)$$

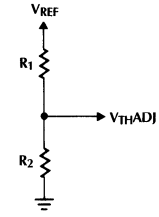


Figure 15.

If, for example, you were using the ML4621 and you wanted the Link Monitor to trigger when the received optical power went below 1μW (-30dBm), you first need to calculate the resultant voltage at V_{IN+} and V_{IN-}. If you were using the HFBR-24X6 Fiberoptic Receiver with a responsivity of 8mV/μW, the peak-to-peak voltage would be:

$$1\mu W \times 8mV/\mu W = 8mV_{P-P} \quad (7)$$

So the Link Monitor should trigger at some point slightly lower than 4mV peak, say 3mV. The reference voltage at $V_{TH}ADJ$ should then be:

$$V_{TH}ADJ = 600(.003) + 0.7 = 2.5V \quad (8)$$

This is a convenient value since the reference voltage supplied by the Quantizer, V_{REF}, is 2.5V. Thus, shorting V_{REF} to $V_{TH}ADJ$ on the ML4621 will set the minimum input signal level at about 3mV.

The Link Monitor has about 0.4mV (peak) hysteresis built-in. $V_{TH}ADJ$ in equation 5 is the *high* threshold level (the trigger point when the input voltage is rising). The *low* threshold level (the trigger point when the input voltage is falling) is about 0.4mV less than the sevels given in these equations. More hysteresis can be induced by connecting a resistor between TTL LINK MON and $V_{TH}ADJ$ creating a positive feedback loop.

A Sample Circuit

The circuit in this section (figure 16) is a point-to-point fiberoptic interface designed to pass 20MBd data over 1 kilometer of 62.5/125μm fiber cable. The main components are the ML4632 LED driver, the HFBR-1414 LED, the HFBR-2416 Receiver, and the ML4621 Quantizer. Choosing -30dBm for the minimum received optical power makes equations 7 and 8 applicable and allows V_{REF} to be used to set the Link Monitor.

Applying figure 5 to the 20MBd data rate yields an optimal bandwidth of about 15MHz. Using equation 2, the value for C_5 is derived by setting f_H equal to 15MHz and solving for C. The lower corner frequency, f_L, should be chosen so that, at least, any 60Hz line noise is filtered out. Choosing 0.1μF for C_1 and C_2 will set the lower corner at 200Hz (equation 1).

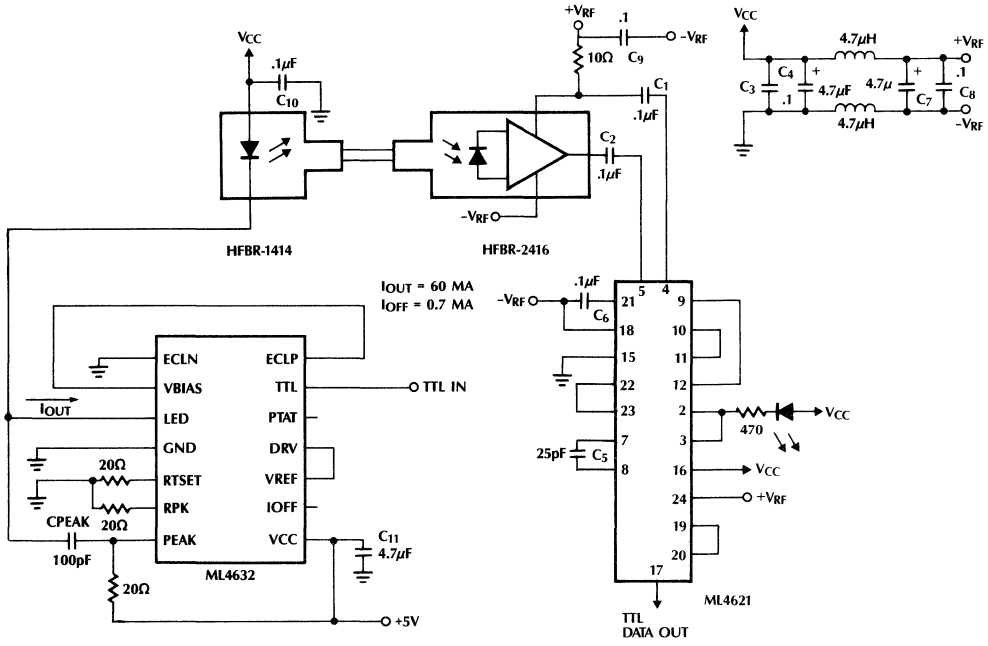


Figure 16.

The only external component left to calculate is C_6. Since the baud rate is 20MBd, the time between peaks in the Link Monitor's peak detector is 50ns. If no more than 0.1% droop is acceptable under the worst case conditions (when the input signal is the smallest), and the internal current source I_{ISET} is used, then C_6 is calculated as follows:

Smallest input signal = 3mV

Gain through amplifiers = 75

Smallest voltage at V_{OUT+} and V_{OUT-} = 3mV × 75 = 225mV

Smallest acceptable droop voltage = 0.1% × 225mV = 225μV

$$\text{Slowest acceptable droop rate} = \frac{225\mu V}{50ns} = 4.5V/\mu s$$

$$\text{Smallest } C_6 = \frac{125\mu A}{4.5V/\mu s} = .028\mu F$$

A 0.1μF capacitor is a convenient acceptable value for this application.

Now that the minimum received power is known, a flux budget can be developed for the interface, and the required optical power from the LED can be derived. Since the output power of the HFBR-1414 is specified out of a short length of fiber attached to the LED unit, no α_{TC} term is required in the flux budget. If no in-line connectors are used and the remaining terms are:

ϕ_R = 1μW
α_O = 10dB/km
L = 1km
α_{CR} = 0.2dB
α_M = 3.0dB

solving the flux budget equation for ϕ_T yields:

$$10 \log \frac{\phi_T}{\phi_R} = \alpha_O L + \alpha_{CR} + \alpha_M \qquad (9)$$

$$10 \log \frac{\phi_T}{1\mu W} = 10(1) + 0.2 + 3 = 13.2dB$$

$$\log \phi_T - \log 1\mu W = 1.32$$

$$\log \phi_T + 6 = 1.32$$

$$\log \phi_T = -4.68$$

$$\phi_T = 20.9\mu W \ (-16.8dBm)$$

The HFBR-1414 has a minimum Peak Output Optical Power of 31.6μW (–15dBm) when coupled to a 62.5/125μm fiber cable, and when a forward current (I_F) of 60mA is applied. Since the optical output power vs. forward current relationship of the LED is approximately linear, the forward current required to get the minimum output power, 31.6μW, can be calculated as follows:

$$\frac{20.9\mu W}{31.6\mu W} \times 60mA = 40mA \qquad (10)$$

To program the ML4632 RTSET can vary from 12 to 30 ohm. This will allow and drive current of 40mA to 100mA. For more detailed information refer to the ML4632 Data Sheet.

Now, to make sure there is no chance of saturating the receiver with too much power, a dynamic range calculation is in order. Since there are no in-line connectors and the cable length is fixed, the only dynamic range components are the thermal variations (α_T), the user defined system margin (α_M), the LED output power tolerance (α_{LED}), and the LED drive circuit tolerance (α_{LDC}):

$$\alpha_{LDC} = 10 \log \frac{\frac{100}{60}(-12dBm)}{\frac{40}{60}(-12dBm)} = 3.97dB \quad (11)$$

$$\alpha_{LED} = 10 \log \frac{-9dBm}{-16dBm} = 7.0dB \quad (12)$$

α_{LDC}	= 3.97dB
α_{LED}	= 7.0dB
α_M	= 3.0dB
α_T	= 1.0dB
Dynamic Range:	14.98dB

So the maximum input power (ϕ_{TMAX}) the HFBR-2416 Receiver will see is:

$$10 \log \frac{\phi_{TMAX}}{1\mu W} = 14.98dB \quad (13)$$

$$\phi_{TMAX} = 31.47\mu W$$

This is well below the 150μW maximum spec for the HFBR-2416, and the resultant output voltage is

$$31.47\mu W \times 8mV/\mu W = 251.76mV_{P-P} \quad (14)$$

This is well below the 1.4V maximum input voltage of the ML4621.

The Board Layout

Refer to Application Note 15.

Micro Linear

Application Note 7

Expanding the ML2200 Input Multiplexer

Harlan Ohara & Vince Cardinale

1.0 Introduction

If the four channel differential input multiplexer on the ML2200 is insufficient for your application, it can be expanded using one of three methods described in this document. An expanded input multiplexer will greatly enhance the processing power of the ML2200 but will restrict some of its flexibility. The limitations of each circuit are discussed at the end of this application note.

The first circuit controls up to 64 differential inputs but restricts the ML2200 to always run eight operations. The second circuit controls up to 128 single ended inputs and again restricts the ML2200 to always run eight operations. The third circuit is limited to eight differential inputs but is fully programmable in the number of operations. Each circuit is fully synchronized with the ML2200 and can be built with off-the-shelf components.

Although this application note discusses only the ML2200, the ML2208 can be used as well. Only minor operational issues within the ML2208 are affected.

2.0 General Theory of Operation

An external counter (74LS163) is used to control the additional multiplexer devices (DG506 or DG507). The counter is incremented by the SYNC pin of the ML2200, which must be programmed as an output. The SYNC pin is suitable for this purpose since it always signifies the start of a new operation.

Synchronization with the ML2200 is achieved by utilizing the DBR pin to load input channel #1 into the counter. Since the DBR signal comes out after the sequence of operations are complete and the next sequence is started, it is too late to correctly synchronize the counter prior to the beginning of the next sequence. Synchronizing on the "1" count, however, will always reset the counter to the proper value if synchronization is ever lost.

Due to the above described behavior, a "boundry" problem exists in the very first sequence of operations *and* the first operation of the second sequence after the chip is started. In order to get out of this problem, the RUN bit of the control register is decoded and duplicated in these circuits. The RESET signal is also brought in. These signals force the counter to predetermined states and relieves the "boundry" problem.

3.0 A 64-Channel Differential Input Circuit

This circuit, shown in figure 1, provides up to 64 additional input channels. Two 74LS163 counters, U5 and U6, are used to develop the address for each channel. Only 6 of the 8 available counter bits are needed to control the channel selection. The 3 LSBs are used to drive the multiplexer (DG507) address bus and the 3 MSBs are decoded and used to drive each multiplexer's enable pin. A 74LS138 (U7) is used to decode the MSBs, providing control for 8 multiplexer chips. The 2 unused counter bits could be used to address additional multiplexers, providing control for up to 256 channels.

A D-type flip-flop (U4A, 74LS74) is used to reset both counters whenever the ML2200 is reset or not in RUN mode. This is accomplished by presenting an active low signal at the synchronous clear inputs of the counters whenever either the RESET or HALT condition exists. When the ML2200 is placed in RUN mode, the first SYNC pulse resets the counters to zero instead of incrementing them. At the same time, the first SYNC pulse clears the resetting condition by clearing the flip-flop.

The other flip-flop in this circuit, U4B, is used to trap the 0 to 1 transition of the DBR signal. This transition causes the output of U4B to go low, which sets up the counters for a load cycle. The next SYNC pulse (which should correspond to the first operation of the ML2200) will then load the counter with a "1", forcing the counters to be synchronized to the sequence. As before, the same pulse that performs the load operation also clears the load operation.

U1 (74LS138) and U2 (74LS379) form the logic that decodes the RUN bit from the microprocessor bus to develop one of the conditions that resets the counters. U1 simply decodes the address of the control register within the ML2200 and U2 latches the status of the RUN bit.

This circuit requires operations to be done in groups of eight and each operation within the group must have the same characteristics.

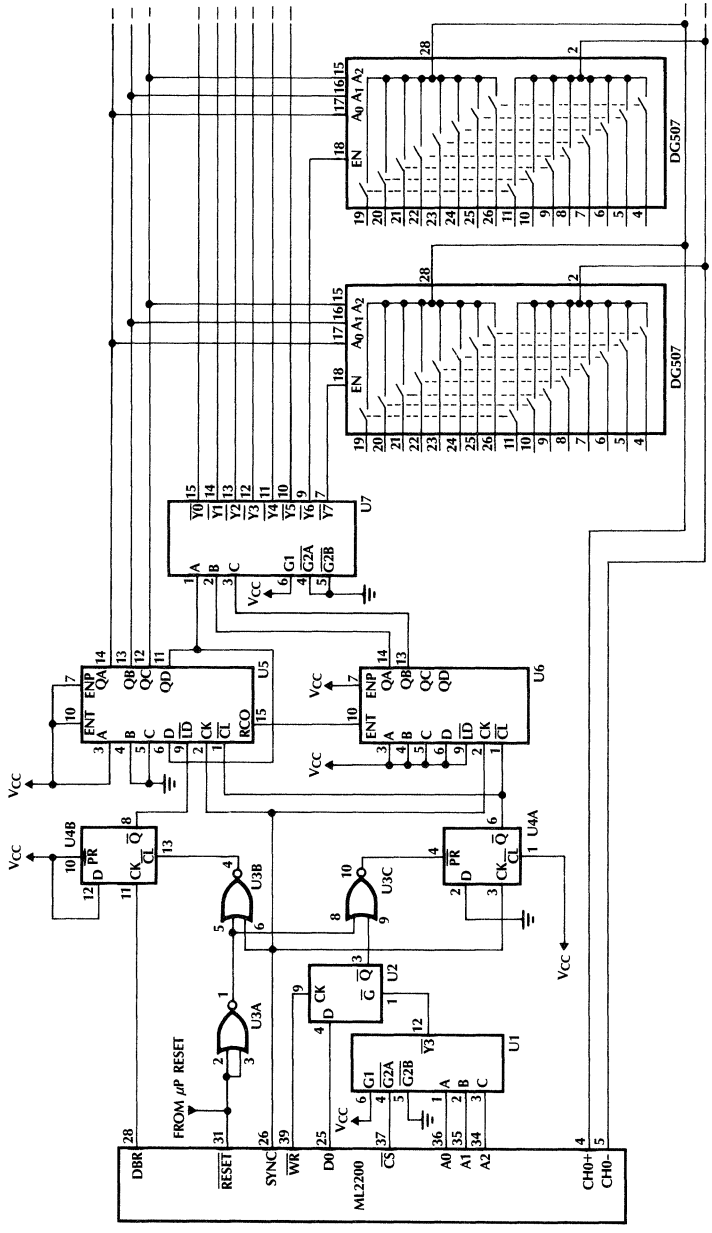

DG507
DG507
U7
U5
U6
U4B
U4A
U3B
U3C
U3A
U2
U1
VCC
FROM μP RESET
DBR
RESET
SYNC
WR
D0
CS
A0
A1
A2
CH0+
CH0-
ML2200

Figure 1.

4.0 A 128-Channel Single Ended Input Circuit

This circuit, shown in figure 2, is identical to the differential circuit with three exceptions:

1. Four address bits are used to drive each multiplexer, since each multiplexer chip now contains 16 channels instead of 8.
2. The decoder chip (U7) is shifted one bit up on the counter output. This makes room for the extra bit needed for multiplexer addressing.
3. DG506 multiplexers are used because this is a single ended application.

This circuit requires operations to be done in groups of eight and each operation within the group must have the same characteristics.

5.0 An 8-Channel Diferrential Input Circuit

This circuit, shown in figure 3, is very similar to the two previous circuits. It still uses two D-type flip-flops to load and reset the counters. The difference here is that register U7 (74LS379) is provided at address location 6 within the 8 byte ML2200 address space and is used to store a count equal to the number of operations programmed by the microprocessor in the ML2200.

Address location 6 and 7 are spare locations within the ML2200 address space. A 74LS85 (U8) four bit comparator is used to reset the counter to zero when the maximum count is reached. A single DG507 provides the eight input channels.

This circuit is not restricted to performing operations in groups of eight. Each channel can be programmed and initiated individually. This flexibility is maintained at the expense of limiting the number of differential inputs to eight.

6.0 Circuit Limitations

In order to maintain synchronization with the ML2200, these circuits contain several inherent limitations which are described below:

1. The SYNC pin is limited to use as an output.
2. These designs allow less settling time for external input circuits, such as instrumentation amplifiers, than otherwise would be possible.
3. The capability to do random reference selection is lost.
4. The capability to do random input channel selection is lost. Input channels must be scanned sequentially.

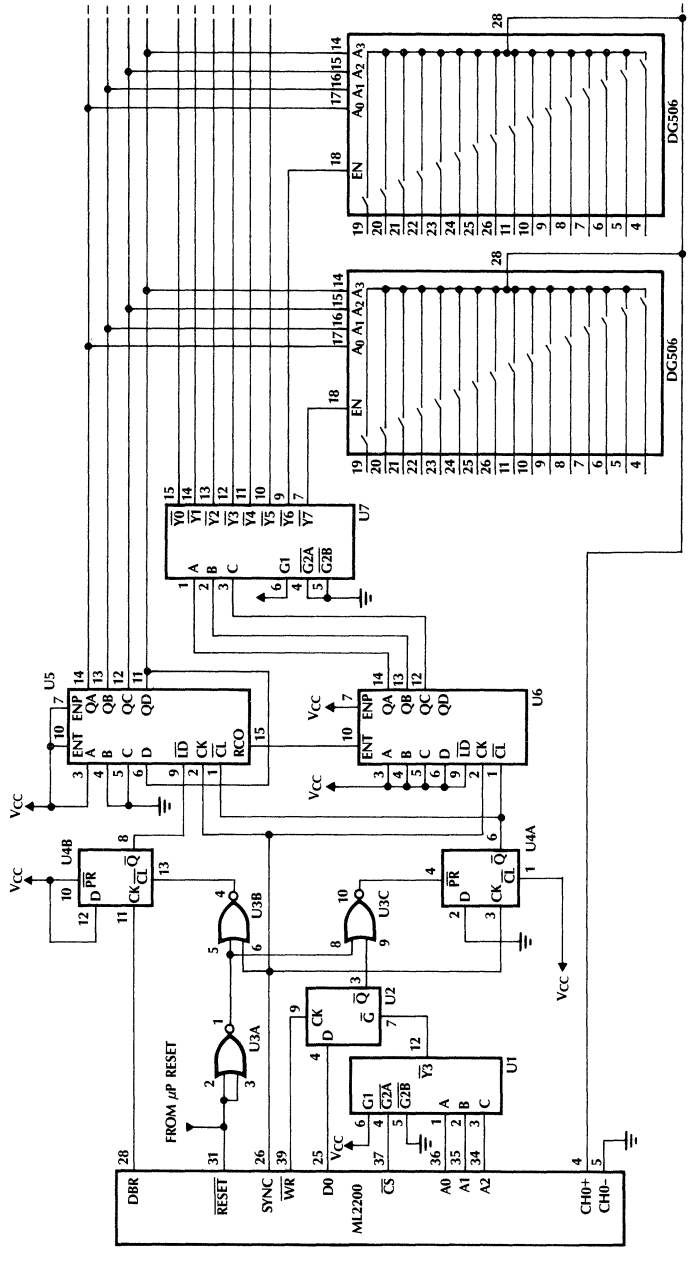

DG506
DG506
U7
U5
U6
U4B
U4A
U3B
U3C
U3A
U2
U1
VCC
FROM μP RESET
DBR
RESET
SYNC
WR
D0
CS
A0
A1
A2
CH0+
CH0-
M12200

Figure 2.

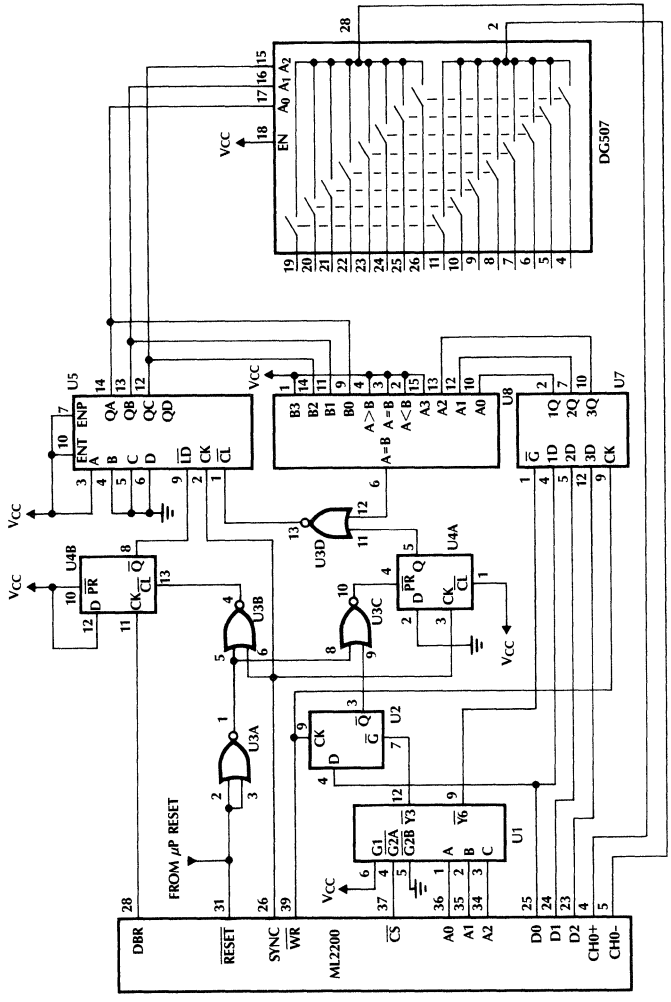

DG507
ML2200
DBR
RESET
SYNC
WR
CS
A0
A1
A2
D0
D1
D2
CH0+
CH0-
FROM μP RESET
VCC
U1
U2
U3A
U3B
U3C
U3D
U4A
U4B
U5
U7
U8

Figure 3.

Micro Linear

Application Note 8

Harlan Ohara

One Pin Crystal Oscillators

1.0 Introduction

Micro Linear has frequently used a one pin oscillator design in its CMOS chips. The concept of a one pin oscillator may seem peculiar to some at first, but the design topology has been around for many years, dating back to vacuum tube days. This topology is shown in Figure 1 and is commonly known as the Colpitts oscillator. The only difference compared to previous implementations is that an MOS transistor is used as the active element.

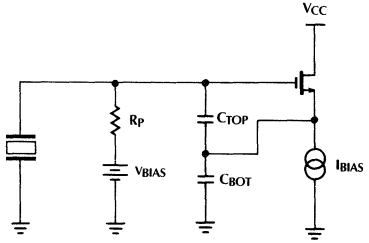


Figure 1.

There are two important advantages to using this particular topology versus the more common two pin design (which is called a Pierce oscillator):

1. Only one pin is required, leaving the extra pin for maximum functionality. This is increasingly important as chips become more complex in function.
2. No external components are usually required except for the crystal. If extremely high frequency accuracy is required, then an external capacitor in parallel with the crystal can be used to trim the frequency.

All is not free, however, there are some disadvantages:

1. This design is less tolerant of external parasitics to ground than the two pin design. This is not usually a problem since the designs used in Micro Linear's circuits have been provided with sufficient margin to handle typical printed circuit board parasitics.
2. Flexibility in terms of user adjustment of design parameters is less in this design. Again, this is not seen to be a problem for two reasons:
   a) Board level designers rarely adjust the two pin design parameters.
   b) Enough margin is provided so that adjustment is not needed.

2.0 Theory of Operation

Exact circuit analysis of the oscillator is a complex procedure for several reasons:

1. In a practical design situation, the system equations are a minimum of 5th order. Exact hand calculations are difficult at best.
2. Final oscillation conditions are not only based on small signal analysis, but very dependent on large signal non-linear situations.
3. The crystal model is generally a simple case in small signal analysis but element parameters can change with excitation level.

In this section, no attempt is made to provide a complete exact analysis. An alternate approach is taken in which hand calculations can closely approximate the small signal solution. This approach is also much more heuristically satisfying in that effects of design parameter changes can be seen without applying a lot of math. This also serves to provide the user with a way to calculate an approximate frequency of oscillation if more exact frequency tolerances are required other than just plugging the crystal in.

For the more technically inclined, an exact small signal sample design procedure is presented in Appendix A using the MathCAD™ program on an IBM-compatible PC. This is possible due to the presence of a root solver capability in MathCAD. Users of HP calculators or numerical analysis computer programs can also perform this analysis. Appendix B contains an example procedure to estimate final oscillation amplitude while Appendix C goes through the procedure to calculate the closed loop root locus plot which is then used to estimate oscillator startup time.

2.1 Crystal Model

The typical crystal model is shown below:

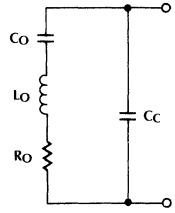


Figure 2.

Typical values for the 12.352 megahertz crystal used in some of Micro Linear's telecom chips are:

$L_O := 8.005814 \cdot 10^{-3}$ henries
$C_C := 5.10 \cdot 10^{-12}$ farad
$C_O := 20.7558 \cdot 10^{-15}$ farad
$R_O := 15$ ohms

The admittance of the crystal is:

$$Y_{XTL}(s) := C_C \cdot s + \frac{1}{L_O \cdot s + \frac{1}{C_O \cdot s} + R_O}$$

Plot 50 points versus frequency:

$x := 1 \ldots 50$

Define radian frequency values:

$\omega_x := 12.346 \cdot 10^6 \cdot 2 \cdot \pi + x \cdot 120$

Plot real (resistive) part:

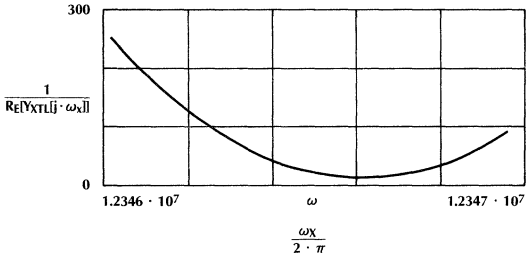


Figure 3.

Plot susceptance:

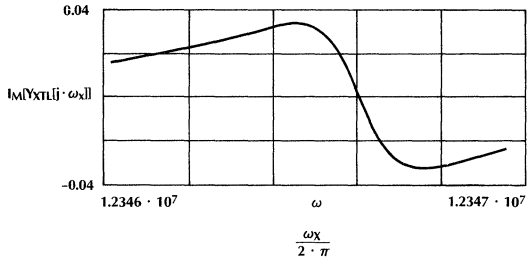


Figure 4.

Note that at the series resonance frequency of:

$$\frac{1}{2 \cdot \pi \cdot \sqrt{L_O \cdot C_O}} = 1.2346608 \cdot 10^7 \text{Hz}$$

the susceptance is zero and the resistance is: $R_O = 15$.

Oscillators that operate the crystal in the series mode use this characteristic as part of a feedback loop in which the loop gain is maximum at this frequency. Above this frequency the susceptance is inductive. Oscillators such as this one-pin design (and the two-pin Pierce) operate the crystal in the parallel mode, "using it as an inductor."

2.2 Simplified Hand Calculation of Loop Gain:

In this section, a simplified (but approximate) method of calculating the loop gain is shown. This method also demonstrates in a more heuristic way how loading affects the oscillator and how one may choose the crystal characteristics, especially the series resistance R_O. The calculation for the approximate frequency of oscillation is also shown. This calculation is quite accurate.

Before we proceed with the calculations. two general principles will be presented that are used to make the calculations. Derivations of these principles can be found in reference [1]:

1. In Figure 5, it is seen that an RLC circuit with series loss can be represented by a circuit with parallel loss (resistance). This applies when the circuit Q is high (>10).

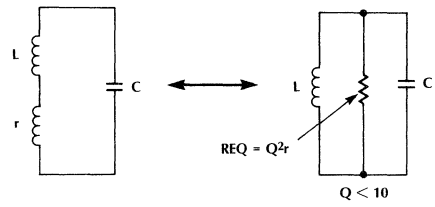


Figure 5.

2. In Figure 6, an RLC circuit with series capacitors can be classified as a "parallel resonant transformer" circuit. Again, this is accurate only when the Q is high (this is easily satisfied with crystal circuits, with Q's in the ten to hundreds of thousands). In this case, the two capacitors act like a transformer with a turns ratio of:

$$n := \frac{C_1}{C_1 + C_2}$$

Hence any resistance can be reflected by the square of the turns ratio.

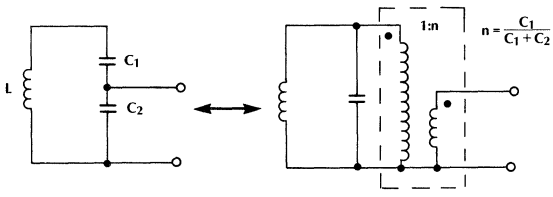


Figure 6.

Using principle 1) from above, we can construct a crystal model which has a parallel loss element:

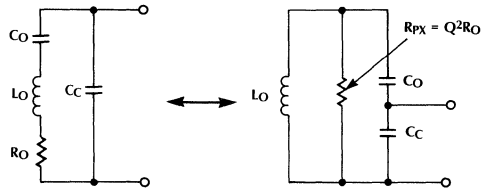


Figure 7.

Using principle 2) from above, we can now reflect the loss element to the crystal terminals by the "turns ratio."

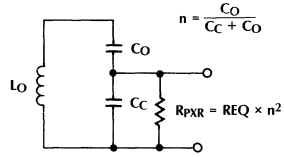


Figure 8.

At this point, we should develop the small signal equivalent of the oscillator circuit:

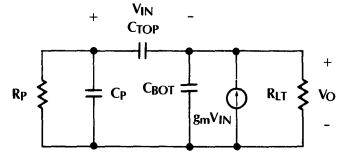


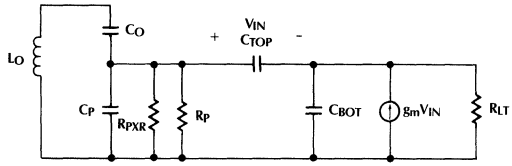
Figure 9.

In Figure 9 the MOS transistor has now been replaced by its small signal equivalent circuit. In this instance, g_m is the small signal transconductance of the transistor and is set by the DC bias current. R_{LT} is the parallel combination of the drain to source conductance and the "body bias factor" (if the source is not at the same potential as the bulk). Derivations of these parameters can be found in reference [2].

C_P is the parallel combination of all circuit reactive parasitics found at the oscillator pin, including the crystal case capacitance, C_C. C_{TOP} and C_{BOT} are on-chip capacitors with sizes chosen for a particular design range.

R_P is the resistance of an on-chip DC bias resistor for the gate of the MOS device *plus* any dissipative loss present at the oscillator pin to ground. This is any lossy effects due to circuit board or socket dissipation factors at the frequency of oscillation.

We now connect the crystal to the oscillator circuit. Note that the reflection and transformer calculations above must be done with all circuit capacitances taken into account:



$$\omega_O = \frac{1}{\sqrt{L_O \cdot C_{TOT}}}, \quad C_{TOT} = \frac{C_O \cdot C_{PTOT}}{C_O + C_{PTOT}}, \quad C_{PTOT} = \frac{C_O \cdot C_{PTOT}}{C_O + C_{PTOT}} + C_P$$

Figure 10.

Let us assign some typical values to the components:

$R_{LT} := 80 \cdot 10^3$ ohms $g_m := 1.6 \cdot 10^{-3}$ Amps/Volt
$C_P := 10 \cdot 10^{-12}$ farad $C_{TOP} := 16 \cdot 10^{-12}$ farad
$R_P := 100 \cdot 10^3$ ohms $C_{BOT} := 16 \cdot 10^{-12}$ farad

We will use the crystal values defined above with the exception that C_C is now included in C_P, which represents all capacitive parasitics present at the pin.

The total capacitance present at the pin including C_{TOP} and C_{BOT} is:

$$C_{PTOT} := \frac{C_{TOP} \cdot C_{BOT}}{C_{TOP} + C_{BOT}} + C_P \qquad C_{PTOT} = 1.8 \cdot 10^{-11}$$

The total capacitance seen across the crystal inductance is:

$$C_{TOT} := \frac{C_O \cdot C_{PTOT}}{C_O + C_{PTOT}} \qquad C_{TOT} = 2.073 \cdot 10^{-14}$$

This capacitance in parallel with the crystal inductance just so happens to produce a resonant frequency which is very close to the frequency of oscillation:

$$\omega_O := \frac{1}{\sqrt{L_O \cdot C_{TOT}}} \qquad \omega_O = 7.762 \cdot 10^7$$

$$\frac{\omega_O}{2 \cdot \pi} = 1.2353724 \cdot 10^7$$

Note that this frequency is .014% higher than the specified 12.352 Megahertz. This is because this crystal was ground with a specified capacitive load of 18pF across its terminals. In our case, we only have about 13pF.

The circuit Q is now calculated:

$$Q := \frac{1}{\omega_O \cdot R_O \cdot C_{TOT}} \qquad Q = 4.143 \cdot 10^4$$

The equivalent parallel resistance across the crystal inductance is now calculated using principle 1) above:

$$R_{PX} := Q^2 \cdot R_O \qquad R_{PX} = 2.574 \cdot 10^{10}$$

This is now reflected to the oscillator pin using principle 2) above:

$$R_{PXR} := R_{PX} \cdot \left[\frac{C_O}{C_O + C_{PTOT}}\right]^2 \qquad R_{PXR} = 3.415 \cdot 10^4$$

This is now combined with the parallel resistance present at the oscillator pin:

$$R_{PTOT} := \frac{R_{PXR} \cdot R_P}{R_{PXR} + R_P} \qquad R_{PTOT} = 2.546 \cdot 10^4$$

Note that this can be reflected again through the "capacitive transformer" of C_{TOP} and C_{BOT}:

$$R_{PTOTR} := R_{PTOT} \cdot \left[\frac{C_{TOP}}{C_{TOP} + C_{BOT}}\right]^2$$

$$R_{PTOTR} = 6.364 \cdot 10^3$$

We now combine this with the resistance present at the transistor source:

$$R_L := \frac{R_{LT} \cdot R_{PTOTR}}{R_{LT} + R_{PTOTR}} \qquad R_L = 5.895 \cdot 10^3$$

This is the load resistance. This multiplied by the transconductance will give us our gain up to the source of the transistor from the input.

$$g_m R_L = 9.433$$

Note that the input to our circuit is the voltage applied across the gate to source of the MOS transistor, or in other words, the voltage across C_{TOP}. Using the "capacitive transformer principle" we can determine that the loop gain is:

$$A_L := \frac{C_{BOT}}{C_{TOP}} \cdot g_m \cdot R_L \qquad A_L = 9.433$$

This gives us our loop gain, which hopefully is more than 1 to allow oscillations. Note that this compares favorably with the exact analysis given in Appendix A of 9.41.

This is a good time to pause and reflect on what the above analysis tells us:

1. It is seen that the oscillation frequency depends on the total capacitance at the oscillator pin in series with the crystal capacitor C_O. Since C_O is very small (typically 10's of femto-farads) external capacitance has a small effect on the oscillation frequency. This provides a means of "tweaking" the frequency to an exact value with a trimmer capacitor placed from the oscillator pin to ground.
2. Using the "capacitive transformer" principle, it is seen that large values of capaitance at the oscillator pin reduces the loop gain since the crystal resistance is now reflected into a smaller value and hence the product $g_m \cdot R_L$ is smaller. Oscilloscope probes can contribute a significant amount of parasitic and should be used carefully when debugging this circuit. If frequency trimming is employed by placing a parallel adjustment capacitor to ground, it must be done carefully so that the loop gain is not made too small.
3. Lossy components at the oscillator pin also reduces the product $g_m \cdot R_L$. This is especially important at higher crystal frequencies, where printed circuit board material or socket material becomes more and more lossy. The value of the on-chip bias resistor varies with frequency from about 1MΩ to about 100kΩ (over a 1 to 20 MHz range). Note that this is a fairly high impedance which is easily affected by external parasitics. Oscilloscope probes can be particularly lossy at these frequencies.

2.3 Three More Important Criteria for Consideration:

Three more important items need to be covered. These items may or may not be OK even if the loop gain calculation is adequate (more than 1):

1. Oscillator phase margin.
2. Nyquist criterion.
3. Final oscillation amplitude

The theory for the above criteria is too lengthy to cover in an application note; only a brief qualitative explanation will be given. The reader is encouraged to consult references [3], [4], and [5]. The exact analysis given in Appendix A will cover the phase margin and Nyquist criterion.

Oscillator Phase Margin:

Figures 11A through 11D in Appendix A show the open loop transfer characteristics of the oscillator. 11A shows the overall magnitude over a wide range of frequencies.

The crystal characteristic is not visible since it occurs over a very narrow range. 11B shows the phase characteristic.

These curves show that the circuit produces a single pole rolloff of 6dB per decade and a final phase shift of 90 degress. Examining the circuit in Figure 10, we see that the loop transfer function starts out at 180 degrees out of phase. This is because the output is developed across C_{BOT} and the input is taken across C_{TOP}. At DC, the voltage across C_{TOP} is of opposite phase to that of C_{BOT}, since the top side of C_{TOP} has a DC path to ground. The single pole rolloff is primarily due to (but not exactly) the combination of R_{LT} and the total capacitance seen at the source of the MOS transistor to ground. The crystal inductance combined with the circuit capacitances can almost provide another 180 degrees of phase shift. This, combined with the 180 degrees from the active element will provide ALMOST, but not quite the 360 degrees needed for oscillation. This is where the single pole rolloff comes in. Examining 11C shows that the loop gain peaks first then dips. This is due to primarily a complex pole pair and a complex zero pair. The peak is a result of the crystal resonating with all circuit capacitances:

$$\omega_P := \frac{1}{\sqrt{L_O \cdot C_{TOT}}} \qquad \omega_P = 7.7620737 \cdot 10^7$$

The complex zero pair comes about when the crystal resonates with all capacitances except for the C_{TOP} and C_{BOT} combination:

$$\omega_Z := \sqrt{\frac{1}{L_O \cdot \left[\frac{C_P \cdot C_O}{C_P + C_O}\right]}} \qquad \omega_Z = 7.7656489 \cdot 10^7$$

The phase shift at the complex pole pair passes through zero and the amplitude peaks to provide the oscillation point. The phase then goes past the point needed for oscillation and then passes through zero again at the complex zero location, returning to the 90 degree point where it started. The amount that the phase shift passes the point necessary for oscillation is called the phase margin. This depends on:

1. The proximity of the complex zero and pole pair, which is determined by the difference in value of the C_{TOP} and C_{BOT} combination relative to the external circuit capacitances. Large parasitics decrease the distance between the pole and zero pair, degrading the phase margin.
2. The circuit "Q," which is a function of the reflected crystal resistances. Applying the reflection algorithm described above shows that large capacitive parasitic values produce a lower "reflected" crystal resistance and thus a lower "Q." Additionally low values of parasitic loss resistances present at the oscillator pin will have the same effect.

If both of the above situations exist, the phase may not cross the zero point at all and oscillations will not start. The exact analysis procedure in Appendix A gives a quantitative description of this situation.

Nyquist Criterion:

In Figures 11C and 11D in Appendix A, note that the loop gain falls to below unity at the complex zero point. A situation can exist where perhaps, if g_M is large, the loop gain will remain above unity, even at the complex zero frequency. This represents a violation of the Nyquist criterion for oscillation in that the Nyquist plot never encircles the –1,0 point. This can happen with crystals at the lower frequencies around 1MHz or so. Appendix A gives a quantitative analysis of this situation, and reference [5] goes in detail for the theory.

Final Oscillation Amplitude:

This section outlines a qualitative explanation of the final oscillation amplitude. For a complete analysis, refer to references [1] and [4]. Appendix B gives an example analysis using the numerical methods of the MathCAD software on an IBM PC. If the user is interested at a higher level, please contact Micro Linear for design parameters.

Given the loop gain at the frequency where the phase shift crosses zero, oscillations start and then increase in amplitude. The waveforms across C_{TOP} and C_{BOT} in Figure 10 are close to sinusoidal due to the high Q of the circuit. The drain current of the MOS transistor, however, is a square law version of the gate to source voltage. Thus, at large signals, the effective g_M of the transistor is reduced by a factor which is related to only the first harmonic of the drain current. This is the only component which is fed back around the loop due to the high Q. For a given small signal loop gain, the amount of oscillation amplitude necessary to maintain the large signal loop gain at one will determine the final oscillation amplitude. For a typical Micro Linear design, this usually falls within the power supplies. Occasionally, then the loop gain is high, the amplitude may exceed the power supplies but is "clamped" by the input static protection diodes present on the oscillator pin. This forward biases the substrate, but the input protection structure of the oscillator pin prevents any harmful effects from this phenomenon.

3.0 Design Parameters

The following section outlines some parameters necessary to perform the hand calculation analysis described above and the exact analysis in Appendix A for various Micro Linear chips at the time of this application note:

ML2200, ML2208, ML2230, ML2233, ML2221:
These designs are restricted to 3–7MHz only; no frequency trim. Provide minimum parasitic from pin to ground possible.

C_{TOP}: 10pF
C_{BOT}: 12pF
Typical g_m: 500μA/V
Typical R_{LT}: 8kΩ
R_P at 3MHz: 240kΩ (see Appendix D)
R_P at 7MHz: 140kΩ

ML2031, ML2032:
These designs are restricted to 3–15MHz only; frequency trimming with capacitor allowed if desired.

C_{TOP}: 16pF
C_{BOT}: 16pF
Typical g_m: 1.6mA/V
Typical R_{LT}: 80kΩ
R_P at 3MHz: 220kΩ (see Appendix D)
R_P at 15MHz: 100kΩ

ML2035, ML2036:
These designs are restricted to 2–18MHz only; frequency trimming with capacitor allowed if desired.

C_{TOP}: 18pF
C_{BOT}: 18pF
Typical g_m: 1.6mA/V
Typical R_{LT}: 80kΩ
R_P at 2MHz: 290kΩ (see Appendix D)
R_P at 15MHz: 100kΩ

In addition, the package pin capacitance is needed along with any stray capacitance due to the bond wire, etc. These values vary from device to device, but an approximate value would be about 1–3pF.

4.0 Crystal Specifications

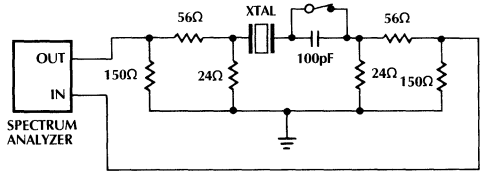
For most situations, standard microprocessor type crystals will work fine in these circuits. If more precise frequency tolerance or unusual frequencies are desired, a special grind will have to be orderd from a crystal manufacturer.

1. Calculate what capacitance will be seen by the crystal in your board, then specify this to the crystal manufacturer.
2. An approximation of the series resistance tolerable can be made using the above analysis or the exact analysis in Appendix A. One fact which is rarely known is that crystal resistances on startup can be much higher than when the crystal is being excited. Specify both a low level maximum series resistance and an operating level series resistance (e.g., 10nW to 1μW startup level and 1μW to 200μW operating level). An equation to calculate crystal dissipation is given in Appendix A.
3. Frequency tolerances of about .005% are common, tighter tolerances are available.
4. Frequency stability over temperature (0–70°C) of about .005% are common; special order for extended temperature range or tighter tolerance.
5. Frequency stability is typically dominated by the crystal itself. Temperature coefficients of the parasitic capacitances come into play and can be calculated using the equations described above. Variation of the oscillator g_m and internal capacitance values versus temperature has a very minor role in stability (1–5ppm or so over 0–70°C).

5.0 Board Level Design Verification

Some simple tests can be performed during the debugging process to verify that the crystal being used and the parasitics present are acceptable for manufacture:

1. Measure the crystal parameters. A procedure to do this is described below. This is a procedure described in reference [6].



1. MEASURE PEAK AMPLITUDE AND FREQUENCY: f_S PEAK AMPLITUDE GIVES R_Q VALUE.
2. OPEN SWITCH, MEASURE PEAK FREQUENCY (THIS SHIFTS UP)
   $\Delta f = \frac{1}{8\pi^2 f_S C_T L_O}$ C_T = 100pF + C_C (CASE CAPACITANCE)
   SOLVE FOR L_O.
3. $f_S = \frac{1}{2\pi\sqrt{L_O C_O}}$, SOLVE FOR C_O

2. Observe crystal startup at the high temperature/low power supply specification of your system. Crystal startup is the most stringent test of the design. Often times the series resistance of the crystal at low levels is many times that at operation. Do this over a wide sample range of the intended crystal to be used.

3. Be sure that the oscillator amplitude is at least 2 volts peak to peak at the high temperature/low supply case. This is to insure that the buffer that squares the sine wave up remains operational. If less than 2 volts, consider using a crystal with a lower series resistance or decrease parasitic capacitance on the oscillator pin. Do not use long lead lengths or traces from the oscillator pin to the crystal.
4. Observe crystal startup times. This is a good indication of available loop gain. Crystal startup time is a function of the real part of the closed loop transfer function. Appendix C provides a sample of how to calculate a root locus plot versus varying g_m's.
5. When observing the oscillator pin, use a FET probe or use a standard probe in series with a 1pF capacitor to prevent loading the pin with excessive parasitic. When observing frequency stability, use a spectrum analyzer with an antenna wire pickup to minimize parasitic effects. Alternately, if a buffered output of the oscillator is available, measure the frequency at this point.

6.0 References

[1] Clarke-Hess, "Communications Circuits: Analysis and Design," Addison-Wesley Publishing Company, 1971.

[2] P.R. Gray and R.G. Meyer, "Analysis and Design of Analog Integrated Circuits," Second Edition, John Wiley and Sons, 1984.

[3] J.T. Santos and R.G. Meyer, "A One Pin Crystal Oscillator for VLSI Circuits," *IEEE Journal of Solid State Circuits*, Vol SC-19 No. 2, April 1984.

[4] R.G. Meyer and D.C.F. Soo, "MOS Crystal Oscillator Design," *IEEE Journal of Solid State Circuits*, Vol SC-15, No. 2, April 1980.

[5] M.A. Unkrich and R.G. Meyer, "Conditions for Start-Up in Crystal Oscillators,"*IEEE Journal of Solid State Circuits*, Vol SC-17, No. 1, February, 1982.

[6] N.J. Watson, "Crystal Testing Using Spectrum Analyser TF 2370," Application Note No. 14, Marconi Instruments.

APPENDIX A

ONE PIN OSCILLATOR DESIGN

This document is an exact small signal analysis of the one pin oscillator using the MathCAD software package.

******define units first:

$rad \equiv 1$ $\qquad$ $TOL \equiv 10^{-6}$ sets MathCAD tolerance

$deg \equiv \pi \cdot \frac{rad}{180}$

******Define Parameters:

$Ctop \equiv 16 \cdot 10^{-12}$ $\qquad$ $Cbot \equiv 16 \cdot 10^{-12}$ $\qquad$ $Cc \equiv 5 \cdot 10^{-12}$ (xtal case cap)

$Ro \equiv 15$ $\qquad$ $Lo \equiv 8.005813989 \cdot 10^{-3}$ $\qquad$ $Co \equiv 20.7558457 \cdot 10^{-15}$

****Serial Resonant Frequency $\omega s := \frac{1}{\sqrt{Lo \cdot Co}}$ $\qquad$ $\frac{\omega s}{2 \cdot \pi} = 1.2346594 \cdot 10^{7}$

****Crystal Q: $Qxtal := \frac{1}{\omega s \cdot Ro \cdot Co}$ $\qquad$ $Qxtal = 4.14 \cdot 10^{4}$

****CAPACITOR DIVIDER:

****Equivalent C of Capacitor Divider: $Ceq := Ctop \cdot \frac{Cbot}{Ctop + Cbot}$

$Ceq = 8 \cdot 10^{-12}$

****Transformer Ratio for Capacitive Divider: $n := \frac{Ctop}{Ctop + Cbot}$

$n = 0.5$

****Impedance Reflection Ratio for Capacitive Divider:

$zc := n^{2}$ $\qquad$ $zc = 0.25$

****Transistor Characteristics:

$gm := 1.6 \cdot 10^{-3}$ $Rlt := 80 \cdot 10^{3}$

****Pin Characteristics:

**External pin parasitics--this is the real and imaginary parts of any external parasitic at the oscillation frequency):

$Rext := 100 \cdot 10^{3}$ $Cext := 5 \cdot 10^{-12}$

****Total Parallel Capacitance:

$Cptot := Cc + Cext + Ceq$

$Cptot = 1.8 \cdot 10^{-11}$ $Cpt := Cptot - Ceq$

$Cpt = 1 \cdot 10^{-11}$

****Equivalent Capacitance for Pole Pair:

$Cpol := Co \cdot \frac{Cptot}{Co + Cptot}$ $Cpol = 2.073 \cdot 10^{-14}$

****Approximate Frequency of Oscillation:

$Wpol := \frac{1}{\sqrt{Lo \cdot Cpol}}$ $Fpol := \frac{Wpol}{2 \cdot \pi}$ $Fpol = 1.235371 \cdot 10^{7}$

****Ratio of the Capacitive Divider Between Crystal and Oscillator:

$nx := \frac{Co}{Co + Cptot}$ $nx = 0.001$

****Impedance Reflection Ratio:

$zx := nx^{2}$ $zx = 1.327 \cdot 10^{-6}$

****Q with Cload: $Q := \frac{Wpol \cdot Lo}{Ro}$ $Q = 4.143 \cdot 10^{4}$

****Equivalent Parallel R for Crystal Only:

$Rpx := Q^{2} \cdot Ro$ $Rpx = 2.574 \cdot 10^{10}$

****Reflected Value of the Crystal Resistance at the Oscillator:

$Rxtal := Rpx \cdot zx$ $\quad Rxtal = 3.415 \cdot 10^{4}$

Total parallel resistance at the oscillator pin:

$Gsum := \frac{1}{Rext} + \frac{1}{Rxtal}$ $\quad Rsum := \frac{1}{Gsum}$ $\quad Rsum = 2.546 \cdot 10^{4}$

****Reflected Parallel R at Oscillator to Transistor Source:

$Rref := Rsum \cdot zc$ $\quad Rref = 6.364 \cdot 10^{3}$

****Total Load Seen at Transistor Source:

$Rl := Rref \cdot \frac{Rlt}{Rref + Rlt}$ $\quad Rl = 5.895 \cdot 10^{3}$

****Loop Gain Calculated with Reflection Method:

$Al := gm \cdot Rl \cdot \frac{Cbot}{Ctop}$ $\quad Al = 9.433$

**in dB: $\quad 20 \cdot \log(Al) = 19.493$

**********EXACT CALCULATIONS:**********

**Polynomial Coefficients for Zeros:

$n0 := 1$

$n1 := (Co \cdot Ro + Co \cdot Rext + Cpt \cdot Rext)$

$n2 := (Co \cdot Lo + Co \cdot Cpt \cdot Ro \cdot Rext)$

$n3 := (Co \cdot Cpt \cdot Lo \cdot Rext)$

guess first zero location:

$\omega := \frac{-1}{Rext \cdot (Cpt + Co)}$ $\quad \omega = -9.9792871 \cdot 10^{5}$

$s := \omega$

$z1 := root\left[n3 \cdot s^{3} + n2 \cdot s^{2} + n1 \cdot s + n0, s\right]$

$z1 = -9.9792906 \cdot 10^{5}$

guess complex zero pair location:

$$\omega := \sqrt{\frac{1}{Lo \cdot \frac{Co \cdot Cpt}{Co + Cpt}}} \qquad \omega = 7.7656404 \cdot 10^{7}$$

$s := \omega \cdot i$

$z2 := root\left[n3 \cdot s^{3} + n2 \cdot s^{2} + n1 \cdot s + n0, s\right]$

$z2 = -1.9722866 \cdot 10^{3} + 7.7656391 \cdot 10^{7}\, i$

***** Zeros:

$z1 = -9.9792906 \cdot 10^{5}$

$z2 = -1.9722866 \cdot 10^{3} + 7.7656391 \cdot 10^{7}\, i$

**********Poles:

**Coefficients for Poles:

$d0 := 1$

$d1 := (Co \cdot Ro + Co \cdot Rext + Ctop \cdot Rlt + Ctop \cdot Rext + Cbot \cdot Rlt + Cpt \cdot Rext)$

$$d2 := \begin{bmatrix} Co \cdot Lo + Co \cdot Ctop \cdot Ro \cdot Rlt + Co \cdot Ctop \cdot Ro \cdot Rext + Co \cdot Ctop \cdot Rlt \cdot Rext \ \ldots \\ + Co \cdot Cbot \cdot Ro \cdot Rlt + Co \cdot Cbot \cdot Rlt \cdot Rext + Co \cdot Cpt \cdot Ro \cdot Rext \qquad \ldots \\ + Ctop \cdot Cbot \cdot Rlt \cdot Rext + Ctop \cdot Cpt \cdot Rlt \cdot Rext + Cbot \cdot Cpt \cdot Rlt \cdot Rext \end{bmatrix}$$

$d3 := Co \cdot Ctop \cdot Lo \cdot Rlt + Co \cdot Ctop \cdot Lo \cdot Rext + Co \cdot Cbot \cdot Lo \cdot Rlt + Co \cdot Cpt \cdot Lo \cdot Rext \ \ldots$

$+ Co \cdot Ctop \cdot Cbot \cdot Ro \cdot Rlt \cdot Rext + Co \cdot Ctop \cdot Cpt \cdot Ro \cdot Rlt \cdot Rext \qquad \ldots$

$+ Co \cdot Cbot \cdot Cpt \cdot Ro \cdot Rlt \cdot Rext$

$d4 := Co \cdot Ctop \cdot Cbot \cdot Lo \cdot Rlt \cdot Rext + Co \cdot Ctop \cdot Cpt \cdot Lo \cdot Rlt \cdot Rext \ \ldots$

$+ Co \cdot Cbot \cdot Cpt \cdot Lo \cdot Rlt \cdot Rext$

guess first pole location:

$$\omega := \frac{-1}{(Rext)\cdot(Ctop + Cbot + Cpt)} \qquad \omega = -2.3809524\cdot 10^{5}$$

$s := \omega$

$$p1 := root\left[d4\cdot s^{4} + d3\cdot s^{3} + d2\cdot s^{2} + d1\cdot s + d0, s\right]$$

$$p1 = -2.492\cdot 10^{5}$$

guess second pole location (this is dominant pole)

$$\omega := \frac{-1}{Rlt\cdot\left[Cbot + \frac{Ctop\cdot Cpt}{Ctop + Cpt}\right]} \qquad \omega = -5.6423611\cdot 10^{5}$$

$s := \omega$

$$p2 := root\left[d4\cdot s^{4} + d3\cdot s^{3} + d2\cdot s^{2} + d1\cdot s + d0, s\right]$$

$$p2 = -8.6971683\cdot 10^{5}$$

guess complex pole pair location:

$$\omega := \frac{-1}{\sqrt{Lo\cdot\frac{Co\cdot(Cpt + Ceq)}{Co + Cpt + Ceq}}} \qquad \omega = -7.7620652\cdot 10^{7}$$

$s := i\cdot\omega$

$$p3 := root\left[d4\cdot s^{4} + d3\cdot s^{3} + d2\cdot s^{2} + d1\cdot s + d0, s\right]$$

$$p3 = -1.3566881\cdot 10^{3} - 7.7620647\cdot 10^{7}\,i$$

**********Summary:**********

$tp := 2\cdot\pi$

$$z1 = -9.9792906\cdot 10^{5} \qquad \frac{z1}{tp} = -1.5882534\cdot 10^{5}$$

$$z2 = -1.9722866\cdot 10^{3} + 7.7656391\cdot 10^{7}\,i \qquad \frac{z2}{tp} = -313.899161 + 1.2359398\cdot 10^{7}\,i$$

$p1 = -2.492351 \cdot 10^{5}$

$p2 = -8.6971683 \cdot 10^{5}$

$p3 = -1.3566881 \cdot 10^{3} - 7.7620647 \cdot 10^{7}\, i$

$\frac{p1}{tp} = -3.9666998 \cdot 10^{4}$

$\frac{p2}{tp} = -1.3841973 \cdot 10^{5}$

$\frac{p3}{tp} = -215.9236169 - 1.235371 \cdot 10^{7}\, i$

**********System Function:**********

$$H(s) := \frac{gm \cdot Rlt \cdot \left[n3 \cdot s^{3} + n2 \cdot s^{2} + n1 \cdot s + n0\right]}{d4 \cdot s^{4} + d3 \cdot s^{3} + d2 \cdot s^{2} + d1 \cdot s + d0}$$

**********Plot System Function**********

$x := 1 \,..\, 80$

$$1_x := \frac{x}{10}$$

$$\omega x := \left[\frac{1}{tp \cdot 10}\right]$$

$$20 \cdot \log\left(\left|\left[H\left[i \cdot \omega x_x\right]\right]\right|\right)$$

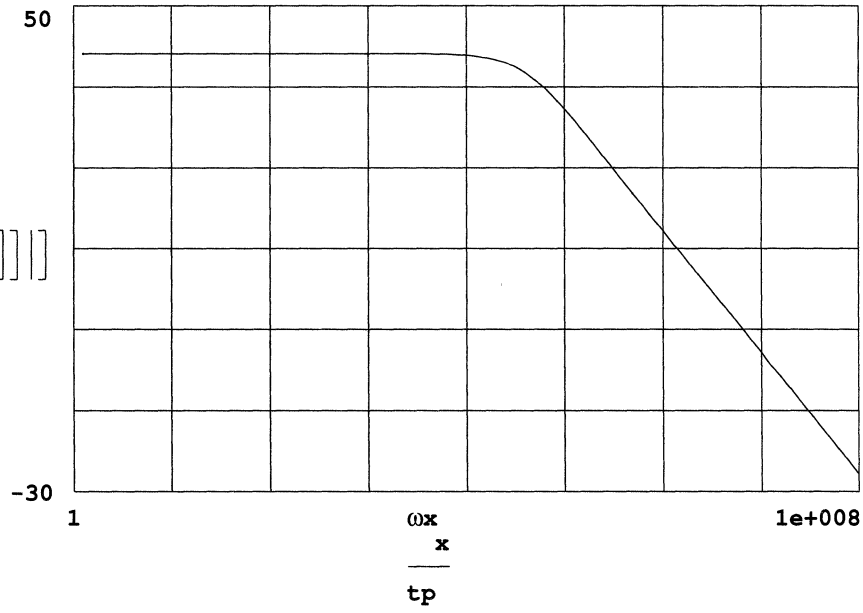


Figure 11A

plot phase:

$$Ph := \left\lceil \arg(H(i \cdot \omega x)) \cdot \frac{180}{\pi} \right\rceil$$

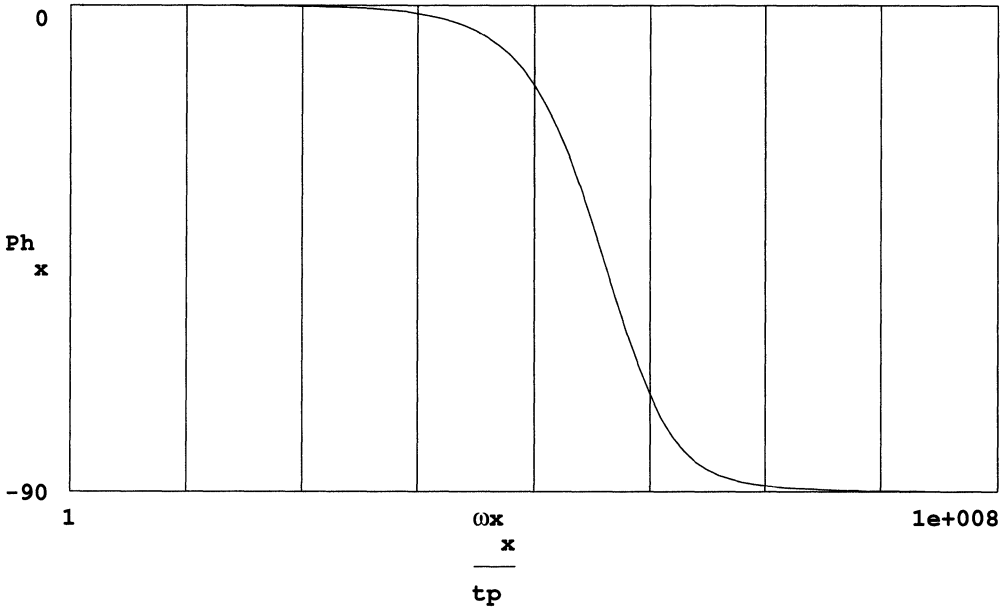


Figure 11B

plot an expanded area around the complex pole/zero pair:

$n := 0 \,..100$

$range := (|Im(z2)| - |Im(p3)|) \qquad range := range \cdot .2$

$lo := |Im(p3)| - range$

$hi := |Im(z2)| + range$

$$\omega x_n := \left\lceil (hi - lo) \cdot \frac{n}{100} + lo \right\rceil$$

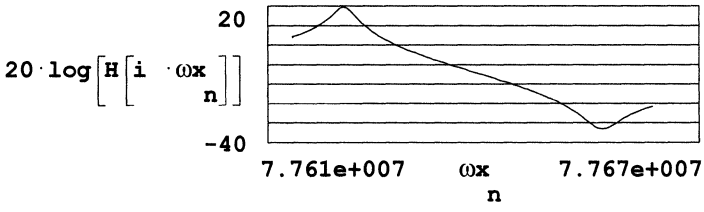


Figure 11C

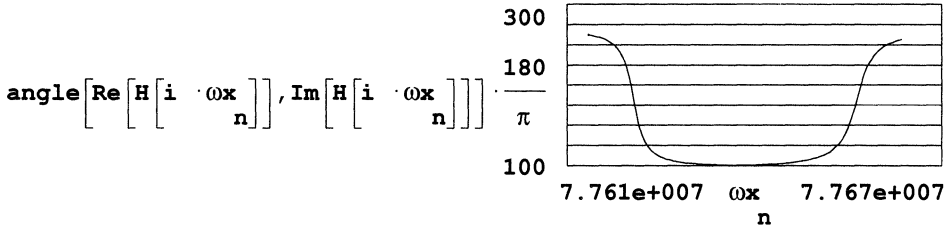


Figure 11D

Nyquist plot:

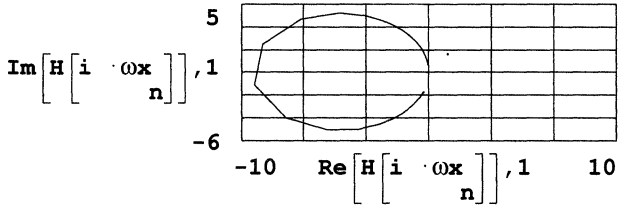


Figure 11E

$\omega g := i \cdot (Im(p3) + 10)$ $\qquad \frac{\omega g}{tp} = -1.2353708 \cdot 10^{7}\, i$

Find exact frequency of phase zero crossing due to complex pole pair:

$\omega osc := root(Im(H(\omega g)), \omega g)$

check:
$arg(H(\omega osc)) = 180 \cdot deg$

Exact zero phase frequency and amplitude:

$\frac{\omega osc}{tp} = -1.2353722 \cdot 10^{7}\, i$ $\qquad |H(\omega osc)| = 9.41$

Find exact zero phase and amplitude due to complex zero pair:

guess first:

$\omega g := i \cdot (Im(z2) - 100)$

$\frac{\omega g}{tp} = 1.2359383 \cdot 10^{7} i$

$\omega zer := root(Im(H(\omega g)), \omega g)$

check:

$arg(H(\omega zer)) = -179.999 \cdot deg$ $\quad |H(\omega zer)| = 0.02$ amplitude

$\frac{\omega zer}{tp} = 1.2359386 \cdot 10^{7} i$ frequency

Find phase margin for oscillator (maximum phase between complex pole and zero pair):

$\omega x_n := -\left[(|\omega zer| - |\omega osc|) \cdot \frac{n}{105} + |\omega osc| + 100 \right]$

$\pi - \max\left[\overline{angle(Re(H(i \cdot \omega x)), Im(H(i \cdot \omega x)))}\right] = -79.361 \cdot deg$

APPENDIX B

This goes through an example calculation of the reduction in small signal gm due to a certain amplitude across Ctop or the gate of the MOS device. The analysis can be carried out in a more general manner and graphs can be plotted out for the purpose of providing a graphical solution to ascertain the final oscillation amplitude given an initial set of bias conditions. The procedure is for example purposes only. If the reader requires more specific information, please contact Micro Linear directly.

This analysis was carried out in MathCAD.

define some numbers:

MOS transistor threshold voltage: $vt := .926$

MOS transistor k factor: $\beta := \frac{700}{4.2} \cdot 47 \cdot 10^{-6}$

$\omega := 1$ here, frequency doesn't matter, so make it 1

$vbq := 1.158$ dc bias value of gate to source

simple MOS equation for drain current

$$id(vgs) := if\left[vgs > vt, \left[\frac{1}{2} \cdot \beta \cdot (vgs - vt)^2\right], 0\right]$$

$idq := id(vbq)$ calculate dc bias current

$idq := 2.112 \cdot 10^{-4}$

$vin(t,vb) := vb + a \cdot \cos(\omega \cdot t)$ define the gate to source excitation

$gmq := \sqrt{2 \cdot \beta \cdot id(vbq)}$ small signal gm at dc bias

$gmq = 0.0018173$

Find the average bias voltage of vgs which MUST equal the dc bias current:

$TOL := 10^{-8}$ guess $vb := vbq - .2$

Given

$$\frac{1}{2 \cdot \pi} \cdot \int_0^{2 \cdot \pi} id(vin(t,vb))\, dt \approx idq$$

$newvb := Find(vb)$

$newvb = 0.898$ $vbq = 1.158$ compare to new bias

check:

$$\left[\frac{1}{2\cdot\pi}\cdot\int_0^{2\cdot\pi} id(vin(t,newvb))\ dt\right] = 2.112\cdot 10^{-4}$$

This represents a shift of:

vbq - newvb = 0.26 volts in vgs bias

for a sine wave amplitude of:

a ≡ .5 volts peak of vgs (note: this is NOT the output voltage!)

This gives a steady state vgs of:

vg(t) := vin(t,newvb)

The first harmonic of the drain current is:

$$id1 := \frac{1}{\pi}\cdot\int_0^{2\cdot\pi} id(vg(t))\cdot\cos(\omega\cdot t)\ dt$$

$id1 = 3.624\cdot 10^{-4}$ The large signal gm, or GM is now calculated:

$$GM := \frac{id1}{a} \qquad GM = 7.247\cdot 10^{-4}$$

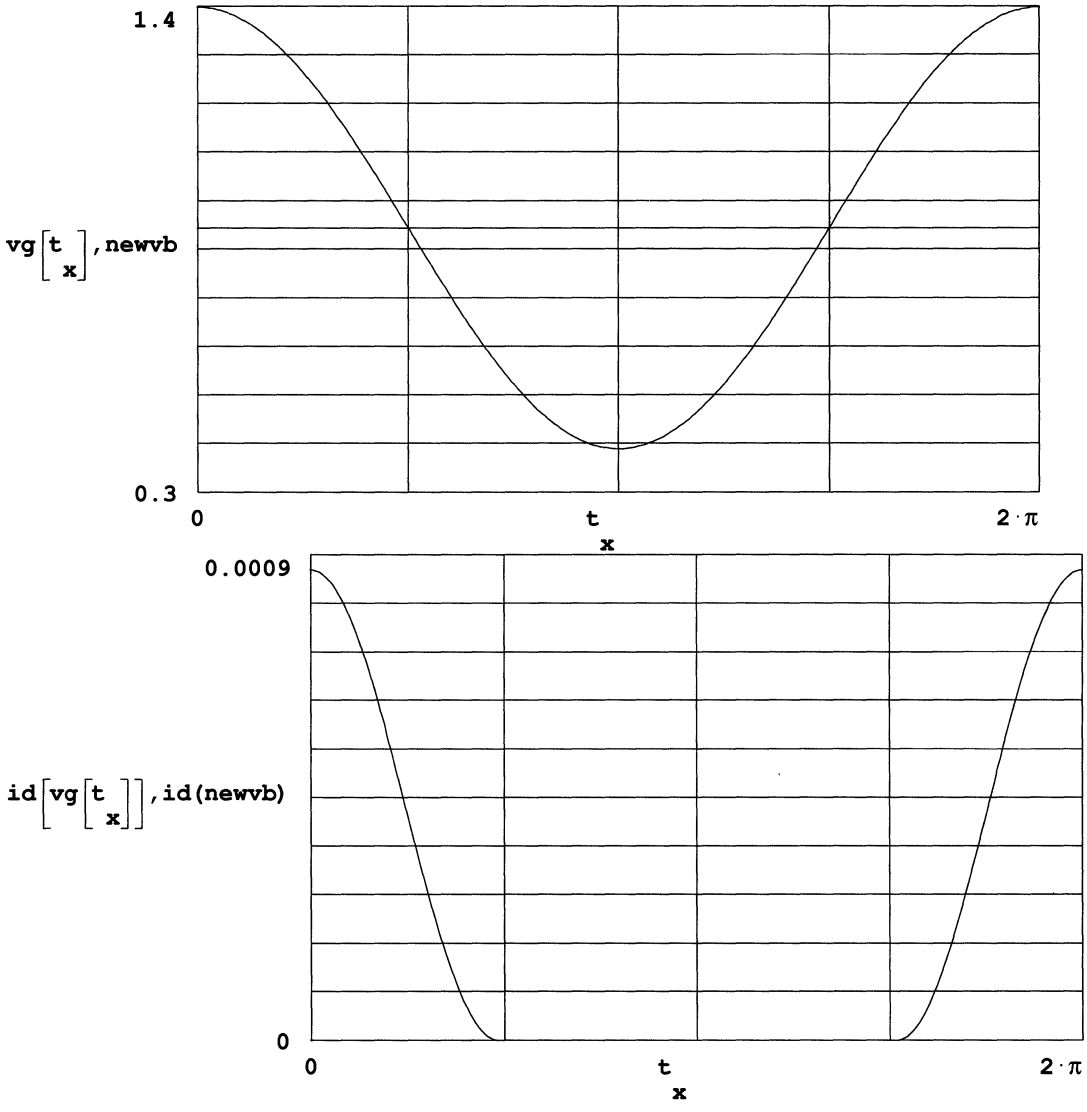
The normalization of GM/gm is now shown:

$\frac{GM}{gmq} = 0.399$ This shows a reduction of the small signal gm.

Plot gate voltage and drain current in steady state:

x := 0 ..255

$$t_x := \frac{2\cdot\pi\cdot x}{255}$$


1.4
vg[t, x], newvb
0.3
0
t
x
2·π
0.0009
id[vg[t, x]], id(newvb)
0
0
t
x
2·π

APPENDIX C

Oscillator Root Locus Calculation

This calculates the real and imaginary parts of the closed loop transfer function. The real part is the time constant of the initial exponential startup transient.

define a range of gm values to calculate over:

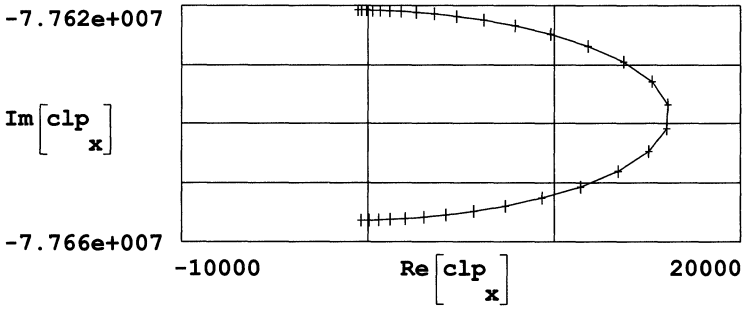
$x := 40 \,..10$

$$gm_x := 10^{-\left[\frac{x}{10}\right]} \qquad TOL \equiv 10^{-6}$$

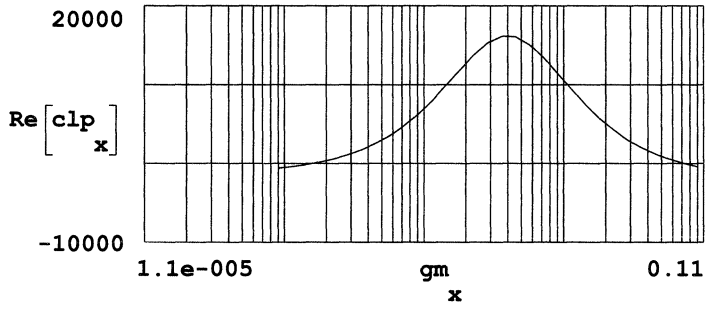
Calculate root locus for gm. These are the roots of the characteristic equation of the closed loop transfer function. See Appendix A for the definitions of the coefficients shown below:

$$clp_x := root\left[\left[\begin{array}{l} d4 \cdot s^4 + \left[d3 + n3 \cdot gm_x \cdot rmb\right] \cdot s^3 + \left[d2 + n2 \cdot gm_x \cdot rmb\right] \cdot s^2 \ldots \\ + \left[d1 + n1 \cdot gm_x \cdot rmb\right] \cdot s + d0 + n0 \cdot gm_x \cdot rmb \end{array}\right], s\right]$$

Root Locus Plot:



Real part of closed loop transfer function versus gm:



Note in the above plot that there is a limited range of gm's for which the poles of the closed loop transfer function remain in the right half plane. In other words, too low a gm creates too low a gain. However, too high gm values also violate the Nyquist Criterion.

APPENDIX D

This shows how to calculate the real part of the on chip bias resistor Rp for inclusion in the loop gain calculations. This was done on MathCAD.

This is a calculation of the Real part of a distributed RC network with one end shorted to ground. A parallel R part is calculated.

ORIGIN := 1 m := 1 ..3

Following DC resistance values are for the ML2031, ML2035, and ML2200. The total capacitance is also calculated for the network.

$$r0 := \begin{bmatrix} 3 \\ 240\cdot 10 \\ 3 \\ 640\cdot 10 \\ 6 \\ 10 \end{bmatrix} \qquad c0_m := r0_m \cdot 100 \cdot .08 \cdot \frac{10^{-15}}{4\cdot 10^{3}}$$

Define a range of frequencies to use: n := 1 ..40

$$f_n := n \cdot \frac{10^{6}}{2} \qquad \omega := (f \cdot 2 \cdot \pi)$$

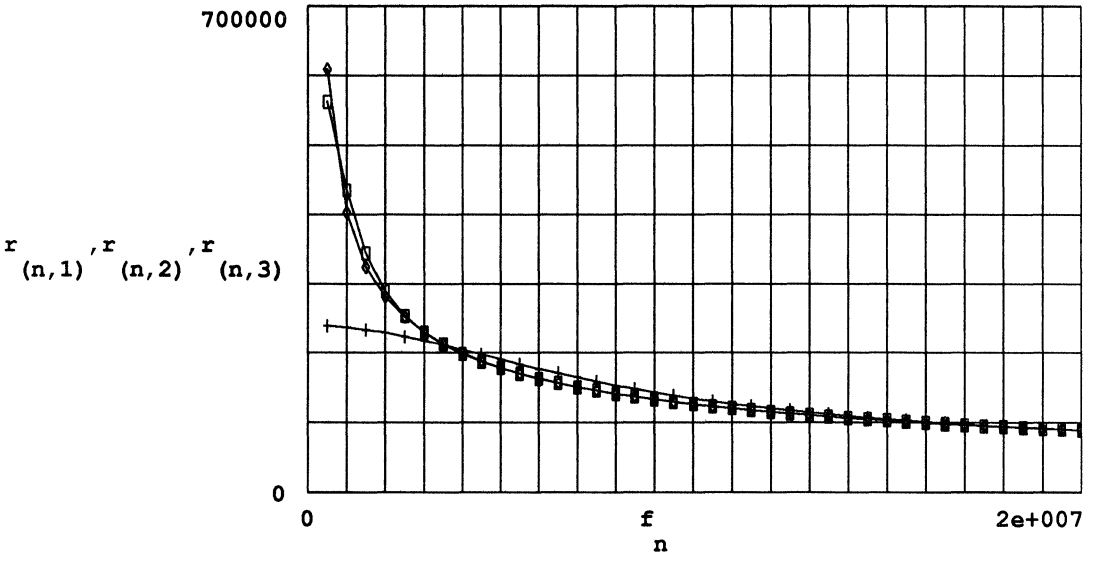
Calculate the admittance of the distributed network:

$$\Gamma_{n,m} := \sqrt{i \cdot \omega \cdot c0_n \cdot r0_m} \qquad Z0_{n,m} := \sqrt{\frac{r0_m}{i \cdot \omega \cdot c0_n}} \qquad y1 := \left[\frac{1}{Z0 \cdot \tanh(\Gamma)}\right]$$

Extract the real part and invert to get resistance:

$$r := \left[\frac{1}{Re(y1)}\right]$$

Plot the real part versus frequency:



diamonds=ML2200, boxes=ML2035, pluses=ML2031

Micro Linear

Application Note 10

An Improved Method of Load Fault Detection

High frequency supply designs pose unique problems in fault detection. A typical method of output fault detection in most standard controllers is to provide a cycle-by-cycle current limit (V_{TH1}) to limit the peak current in the output switch. In addition, these controllers have a second current limit (V_{TH2}), which is typically set 40% higher than the cycle by cycle limit. Crossing V_{TH2} on the I_{SENSE} input resets the Soft Start circuit and allows current in the output to decay before re-starting the system.

In theory, by the time the power output stage can begin to turn off from having crossed V_{TH1}, the output current will have exceeded V_{TH2} and a soft start reset wil be performed. This technique works well if leakage inductance is low and turn-off delay is high enough to cause enough energy to transfer to the output inductor, causing the current to build up in subsequent cycles (figure 2a). This current build up takes place when the output is short circuited because the output inductor has almost no voltage across it and therefore a very shallow discharge slope. If, however, energy transfer is low due to fast turn-off of the outputs (which is desirable to minimize switching losses) energy transfer to the output inductor will be minimized, resulting in the supply continually running at the cycle by cycle current limit to a short circuit with no reset occurring (figure 2b).

High frequency controllers are designed to minimize T_{PD} and turn off the output MOSFET gates quickly. This implies that the event which triggers soft start reset will not persist for very long if it is detected at all. The short persistence of the triggering event requires that Q1 discharge C1 in a very short time, typically resulting in a partial discharge and an inadequate reset. A solution to this problem (figure 3) is implemented in all of Micro Linear's PWM IC's. Flip-flop (F2) and comparator (A4) are added to the circuit, to ensure a full reset. If desired, a delay (as implemented in the ML4809 and ML4811) can also be added before restart, which lowers the system's effective duty cycle allowing the supply to cool down.

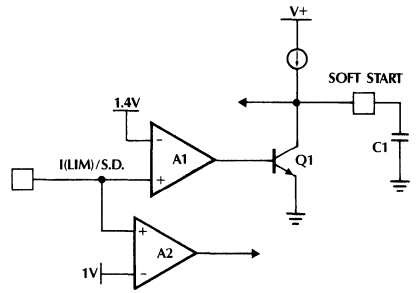


Figure 1. Typical Two Threshold Current Limit/Fault Detect

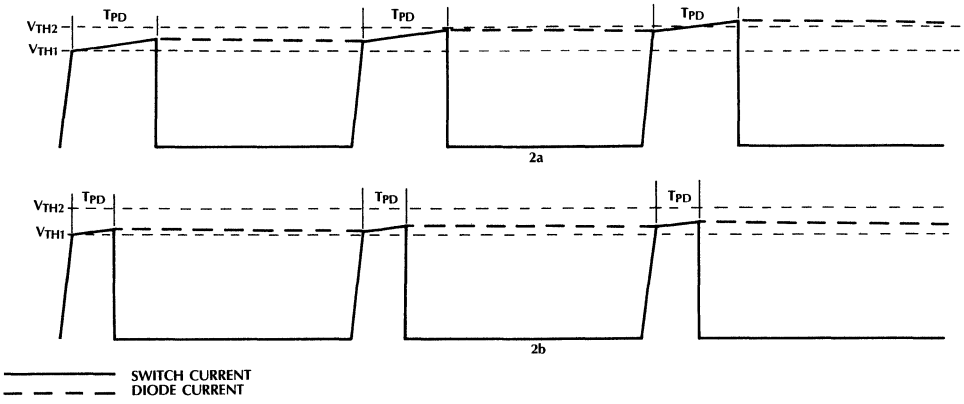


Figure 2. Current Waveforms During Output Short Circuit Slow Output Turn-Off (2a) and Fast Turn-Off (2b)

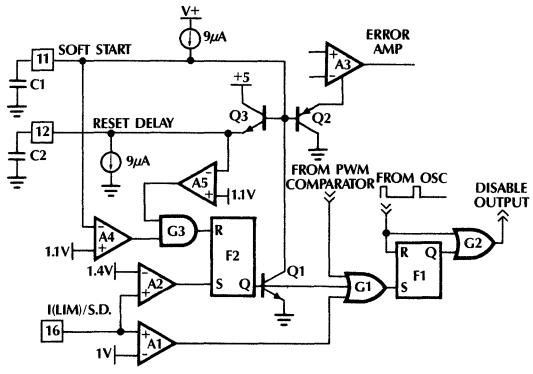


Figure 3. Improved Soft Start Reset with Delay — ML4809

Integrating Fault Detection

The "two threshold" detection technique described above limits the system designer's freedom to optimize his magnetics and minimize switching time. Since detecting the fault relies on building inductor current up on successive cycles, propagation delay cannot be minimized (as shown in figure 2) for this technique to work. Since these two parameters are important terms in high frequency supply efficiency, the need to compromise due to inadequacies in fault detection presents a problem.

A method of circumventing this problem involves "counting" the number of times the controller terminates the PWM cycle due to the cycle by cycle current limit.

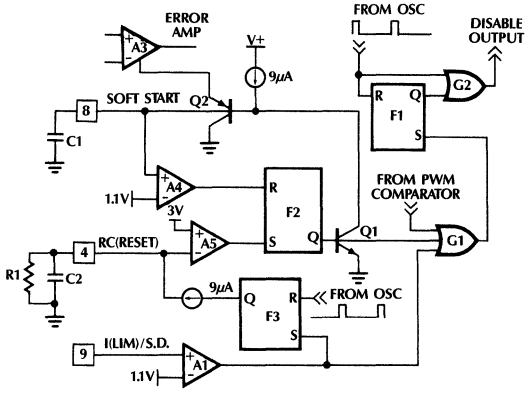


Figure 4. Integrating Soft Start Reset Circuit with Delay (ML4811)

Figure 4 shows the Integrating Fault Detect circuit. When the I_{LIM} signal (switch current) crosses the 1.1V threshold A1 signals the F1 to terminate the cycle and sets F3, which is reset at the beginning of each PWM cycle. The output of F3 turns on a current source to charge C2. When, after several cycles, C2 has charged to 3V, A5 turns on F2 to discharge soft start capacitor C1. Charge is continually bled from C2 by R1. If a current surge is short lived (for instance a disk drive start-up or a board being plugged in to a live rack) the control can "ride out" the surge (figure 5a) with the switch protected by the cycle by cycle limit. R1 and C1 can be selected to track diode heating, or to ride out various system surge requirements as required.

If the high current demanded is caused by a short circuit (figure 5b), the duty cycle will be short and the output diodes will carry the current for the majority of the PWM cycle. C2 charges fastest for low duty cycles (since F3 will be on for a longer time) providing for quicker shutdown during short-circuit when the output diodes are being maximally stressed.

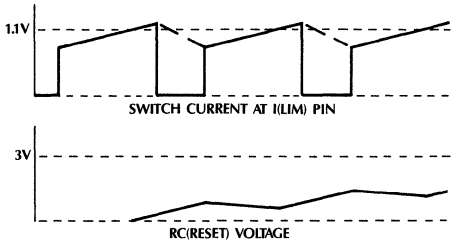


Figure 5a. Integrating Fault Detection Response to Load Surge

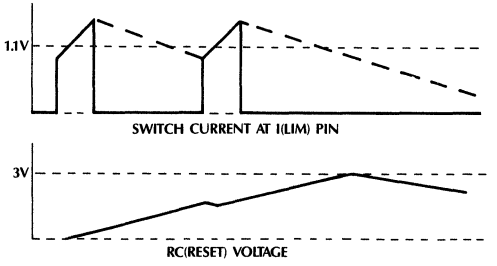


Figure 5b. Response to Load Fault (Short Circuit)

The Integrating Fault Detection circuit allows reliable detection of output faults independent of supply magnetics and propagation delays. Additionally, this method of fault detection is inherently noise immune, programmable, and can distinguish between load surges and load faults (short circuits).

Micro Linear

Application Note 11

Mehmet K. Nalbant

Power Factor Enhancement Circuit

A simple enhancement circuit for the ML4812 is described. The circuit which will be called the power factor enhancement circuit greatly improves the power factor while reducing the total harmonic distortion of the current waveform.

The circuit details for implementing the power factor enhancement circuit are given below. Figure 1 shows the schematic diagram of the circuit. The circuit operates by generating a small DC current bias and injecting it into the I_{SINE} (pin 6) input of the ML4812. This current injection has the net effect of improving the zero current crossover distortion. It does this by lifting the shoulders of the current waveform around the zero crossover areas.

The circuit in the dotted lines in Figure 2, shows the details of the implementation. The circuit automatically adjusts the amount of the injected DC bias as a function of the line voltage. The reason behind the variable amount of DC current injection is that at lower input voltages, the amount of DC bias that is required is less.

Based on experience, the amount of bias required at 220 VAC is approximately four times higher than at 120 VAC. The proper scaling can be adjusted by choosing appropriate values for the various resistors used and the zener diode voltage. The amount of bias that is required is a function of the boost inductor value and the ramp compensation. For best performance the value of the inductor should be chosen as high as possible which in turn will necessitate a small amount of ramp compensation.

One way to find the required bias currents is summarized below: the first step is to find the optimum bias at the nominal operating point, for example, at 120 VAC. This is done by connecting a variable resistor to the reference output of the IC. The initial value of the resistor is selected such that, the bias current equals the peak to peak ramp compensation voltage when the duty cycle is at its maximum. After the optimum value at the nominal operating conditions is found the input voltage is increased to 220 VAC and the same procedure above is repeated to find the optimum value of the resistor at the 220 VAC nominal operating conditions. The bias currents corresponding to the two resistor values above can be used to calculate the values of the components in the enhancement circuit. The formulas for calculating the various components are given below:

$$V_{C3\ (VIN)} = \frac{0.9V_{IN(RMS)}\ R6}{R1 + R2 + R6} \quad (1)$$

$$I_{ISINE(VIN)} = \frac{V_{C3} - V_{BE} - V_Z - V_{ISINE}}{R7} \quad (2)$$

$$r = \frac{I_{ISINE(220\ VAC)}}{I_{ISINE(120\ VAC)}} \quad (3)$$

$$r = \frac{V_{C3(220\ VAC)} - V_{BE} - V_Z - V_{ISINE}}{V_{C3(120\ VAC)} - V_{BE} - V_Z - V_{ISINE}} \quad (4)$$

Where:

$I_{ISINE(VIN)}$ = Bias current into the I_{SINE} input as function of the input voltage.

V_{BE} = Base emitter voltage of Q3 (0.7V nominal).

V_{ISINE} = Voltage at I_{SINE} input, typically 0.7V.

r = Ratio of bias current at 220 VAC input to the bias current at 120 VAC input.

By chosing a value for $V_{C3(220\ VAC)}$ the value of $V_{C3(120\ VAC)}$ is also found. These two values can be substituted to the equation above to calculate the required value for V_Z. The value of R7 can be found by using (2). The values of the remaining components can be calculated by using (1).

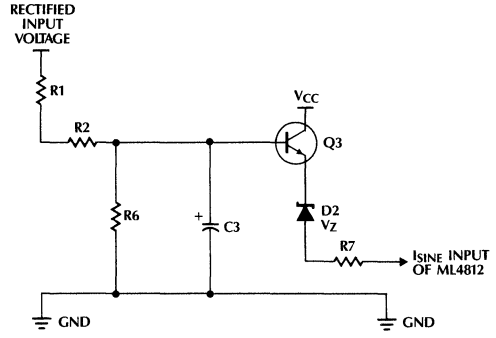


Figure 1. The Enhancement Circuit

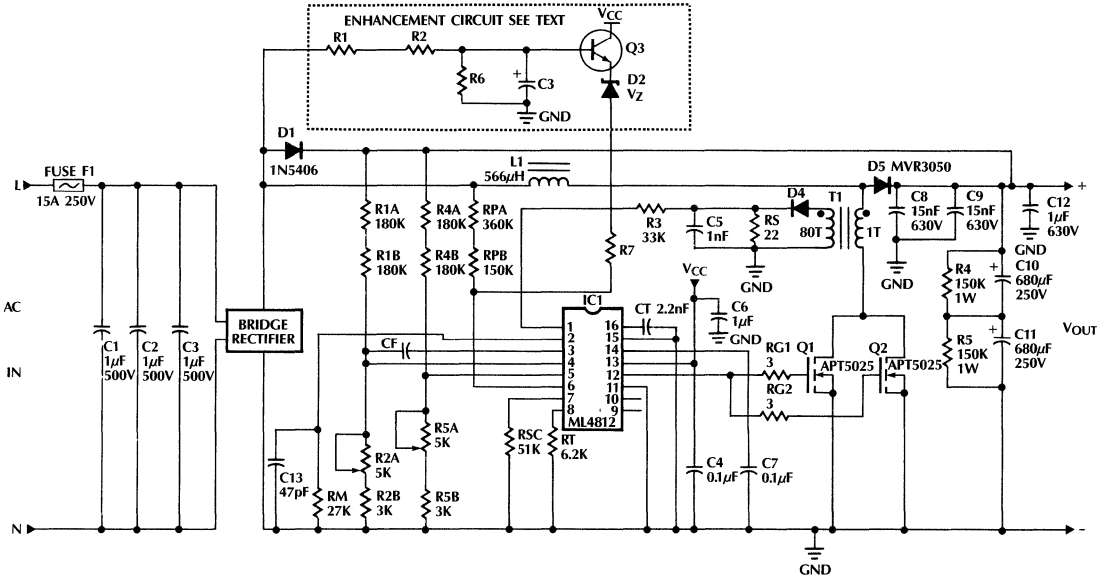


Figure 2. 1KW Enhanced Power Factor Correction Circuit

The circuit of Figure 2, is a 1KW input, power factor regulator. For this circuit the values of the enhancement circuit components were as follows:

R1 + R2 = 330K
R6 = 22K
R7 = 22K
D2, V_Z = 3.5V
Q3 = 2N2222 or any equivalent small signal transistor.
C3 = 10µF electrolytic cap

Table 1 shows the performance of the power factor regulator with and without the enhancement circuit.

Table 1. Effect of Enhancement Circuit on Power Factor

Input Voltage (VAC)	Input Power (W)	Power Factor	
		With Enhancement	Without Enhancement
120	742	.998	.991
	365	.994	.976
220	706	.996	.976
	352	.969	.940

Micro Linear

Application Note 12

Generating Phase Controlled Sinewaves with the ML2036

Vince Cardinale

Introduction

The 16-bit resolution of the ML2036 combined with its Inhibit feature makes it a powerful tool for generating precision sinewaves. It can produce frequencies from DC to 50kHz in 1Hz increments with –40dB harmonic distortion *and* has the control to stop the output at any given time or at the next zero crossing, *with no external components.*

Precise phase control can also be obtained with the addition of a few external devices. With the addition of phase control two or more ML2036 sinewave generators can be synchronized at any angle from 0 to 360 with better than 1 degree resolution.

Inhibit Mode

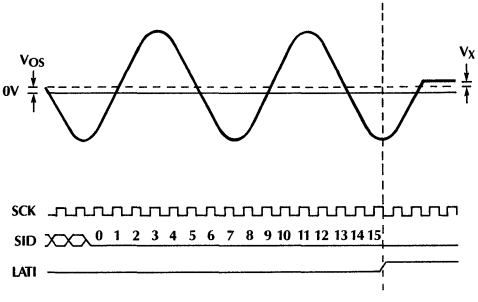
In order to place the ML2036 in Inhibit mode three conditions must occur simultaneously. The three-level P_{DN}–INH input pin must be at the V_{SS} voltage (–5V), the shift register must be loaded with all zeros, and the LATI pin must be a logic "1" (+5V). Once these three conditions are met the output continues to operate until it reaches $V_{OS} + |V_X|$ if the next zero crossing is positive going, or $V_{OS} - |V_X|$ if the next zero crossing is negative going, and then holds this level (see figure 1). The output will stay at this voltage until a new frequency is loaded into the data latch, at which point the output will continue where it left off. If the output stopped at zero after approaching from below 0V then it will start-up going positive. If it stopped after approaching from above 0V then it will start-up going negative.

Initialization

In order to synchronize the ML2036 you must first initialize it so it will start up at a known point in the sinewave. By using the Inhibit mode you can stop the part at 0V but you can't be sure from which direction it approached zero, or more importantly which direction it will start-up. If you can guarantee that it stopped while approaching from below 0V then you can be sure it will start-up going positive. This can be done if the LATI pin is not allowed to be high when the output is above ground. The circuit in figure 2 and the following procedure demonstrate how this can be implemented.

Initialization Procedure

1) Power up
2) Set LAT high
3) Set INH low
4) Load MSB: **0001 0000 0000 0000** :LSB
5) Set LAT low
6) Wait at least 1 output cycle time
7) Load all 0s
8) Set INH high (INH must go high before LAT by at least a NAND gate delay)
9) Set LAT high
10) Wait at least 1.5 output cycle times
    Output stops at 0V going high
11) Load desired frequency
12) Set LAT low
    Output begins at 0V going high
13) Set INH low



$$|V_X| = \frac{V_{PEAK}}{256} \text{ ; For } f_{OUT} \leq \frac{f_{CLK}}{2048}$$

$$|V_X| \leq \frac{V_{PEAK}}{256} + V_{PEAK} \text{ Sine } \left(\frac{8\pi f_{OUT}}{f_{CLK}} + \frac{\pi}{512}\right)$$

$$\text{For } f_{OUT} > \frac{f_{CLK}}{2048}$$

Figure 1. Inhibit Mode

Synchronization

At the completion of step 10 the part is initialized. Its output is stable at about 0V and will start up going positive. If you want to synchronize the output with some external event you can load the shift register with the desired frequency (step 11) and then set LAT low (step 12) synchronously with the external event. If you want to synchronize two ML2036 sinewave generators together initialize them both as described, and then set LAT low (step 12) on both circuits simultaneously.

Precise phase control between two parts can be achieved by initializing both parts, starting one and then waiting a known time before starting the other. For example, to produce two 5kHz sinewaves with 90° phase shift you should wait 50μs between starting each circuit. Since the ML2036 uses a 3MHz reference clock to update the output (assuming a 12MHz clock is used to drive CLK_{IN}) the phase resolution will be 0.6°. This resolution will vary from 0.0012° for two 10Hz signals to 6° for two 50kHz signals.

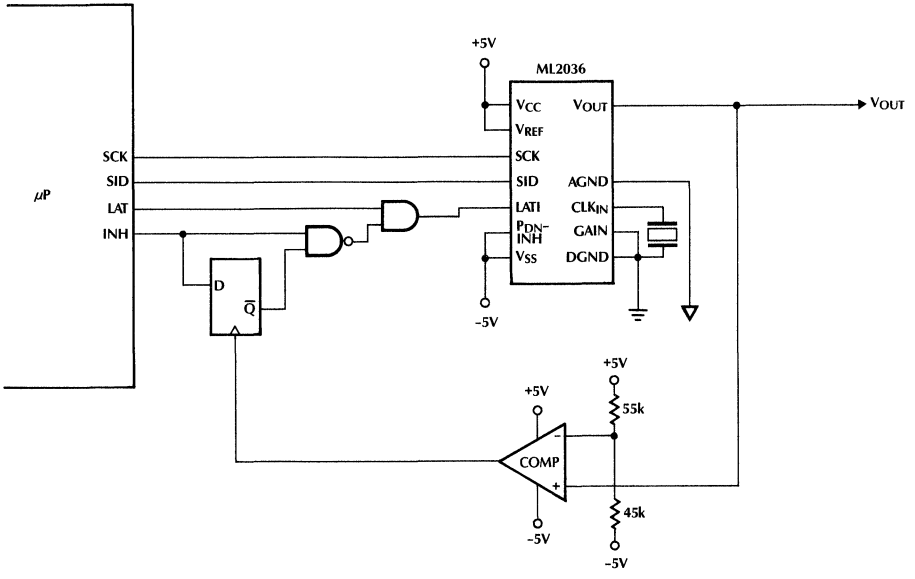


Figure 2.

Application Note 13

Designing with 10Base-T Transceivers

INTRODUCTION

Micro Linear's family of 10Base-T transceivers offer highly integrated solutions for internal and external MAUs (Media Attachment Units) as well as HUB MAUs. These chips offer a high performance current drive transmitter with very low jitter and RFI noise. The ML4652 and ML4658 are 10Base-T transceivers that provide an AU interface for internal and external DTE MAUs while ML4654 and ML4655 provide TTL and ECL interfaces suited for Multiport Repeaters.

The following application note will cover some of the design issues that arise when designing either type of Media Attachment Units for Local Area Networks based on 10Base-T.

INTERNAL (EMBEDDED) MAUs WITH SHARED AUI PORT

Figure 1 shows a detailed schematic for an internal MAU design with a shared AUI (Attachment Unit Interface) port. The optional port requires additional circuitry as defined in the IEEE 802.3 specifications for proper termination and protection at the serial interface chip (or Manchester Encoder/Decoder) and the 10Base-T transceiver chip connected to an AUI port.

An AUI connection requires termination impedance of 78Ω on the receive end of the transmission lines (DI and CI). As such R1 and R2 in parallel with R3 and R4 provide the proper termination. This also applies to the receive output pins 4 and 5 of the transceiver chip. The 357Ω resistors for R3 and R4 was chosen to properly bias the driver circuitry (see section on AUI driver output). The 2kΩ values for R7 and R8 were chosen to provide the BIAS voltage for Tx+ and Tx– inputs. This also will not load down the 78Ω transmission line when the AUI port is connected and the transceiver chip is tri-stated. The output AUI drivers of the transceiver chip must be tri-stated to not load down the transmission lines when the AUI port is connected and the twisted pair port is disconnected. Powering down the chip will tri-state the outputs.

The transceiver can be powered down by switching V_{CC} to ground. This includes power to the device, +5V at RRSET and RTSET resistors, all status LEDs and center tap of the transformer. When the device is powered down, the Tx±, Rx± and COLL± pins form a substrate diode to ground. This causes the output of DO, DI and CI to be at approximately 0.7V, which loads down the data lines. Since this is not desirable, we need to add six 0.01µF capacitors in series with these pins as shown in figure 1. This way we isolate the Manchester Encoder/Decoder from the Tx± pins and the AUI from the Rx± and the COLL± pins.

The isolation transformer is required for protection of the transceiver chip from 16V with respect to the system ground at the AUI interface during a fault condition as specified in 7.4.1.6. and 7.4.2.6 sections of the IEEE 802.3 standards for both the driver and the receiver.

If a shared AUI port is not required, then the design becomes simpler. Figure 13 of the datasheet shows AC coupling between the serial interface and the transceiver. This is to block DC bias voltage of the serial interface chip that may not match that of the transceiver. Micro Linear's transceivers require the input bias to be between 2.5V and 4.5V for CI and DI. If the two chips are compatible one can eliminate the AC coupling capacitors and bias resistors. By using a DC coupled interface, biasing the driver outputs is all that is needed for proper operation (Figure 2).

Twisted Pair Interface

The twisted pair connection to 10Base-T requires additional filtering and isolation components. The output structure of the twisted pair drivers are of the current drive type. This poses several very significant advantages when driving the twisted pair medium. Because the drivers are current driven, the differential outputs are well matched for a balanced signal transmission. Balanced transmission is crucial for meeting tight regulations on signal shapes. Also current driven outputs produce lower common-mode voltages for a lower EMI radiation. This can be a very significant issue when facing FCC regulations. Another advantage to current mode is that output drive, can be easily adjusted to compensate for losses in the transformer or output filter. RTSET will set the level of output drive current by the relationship:

$$RTSET = (RL/100) \times 220$$

where RL is the characteristic impedance of the twisted pair cable.

The twisted pair differential output will see an effective resistance of 50Ω from the parallel combination of the two 200Ω resistors and reflected secondary AC line impedance of 100Ω for unshielded twisted pair. By driving 42mA to the 50Ω complex load, the differential signal voltage will swing ±2.5V peak around the 5V bias point when taking transients into consideration.

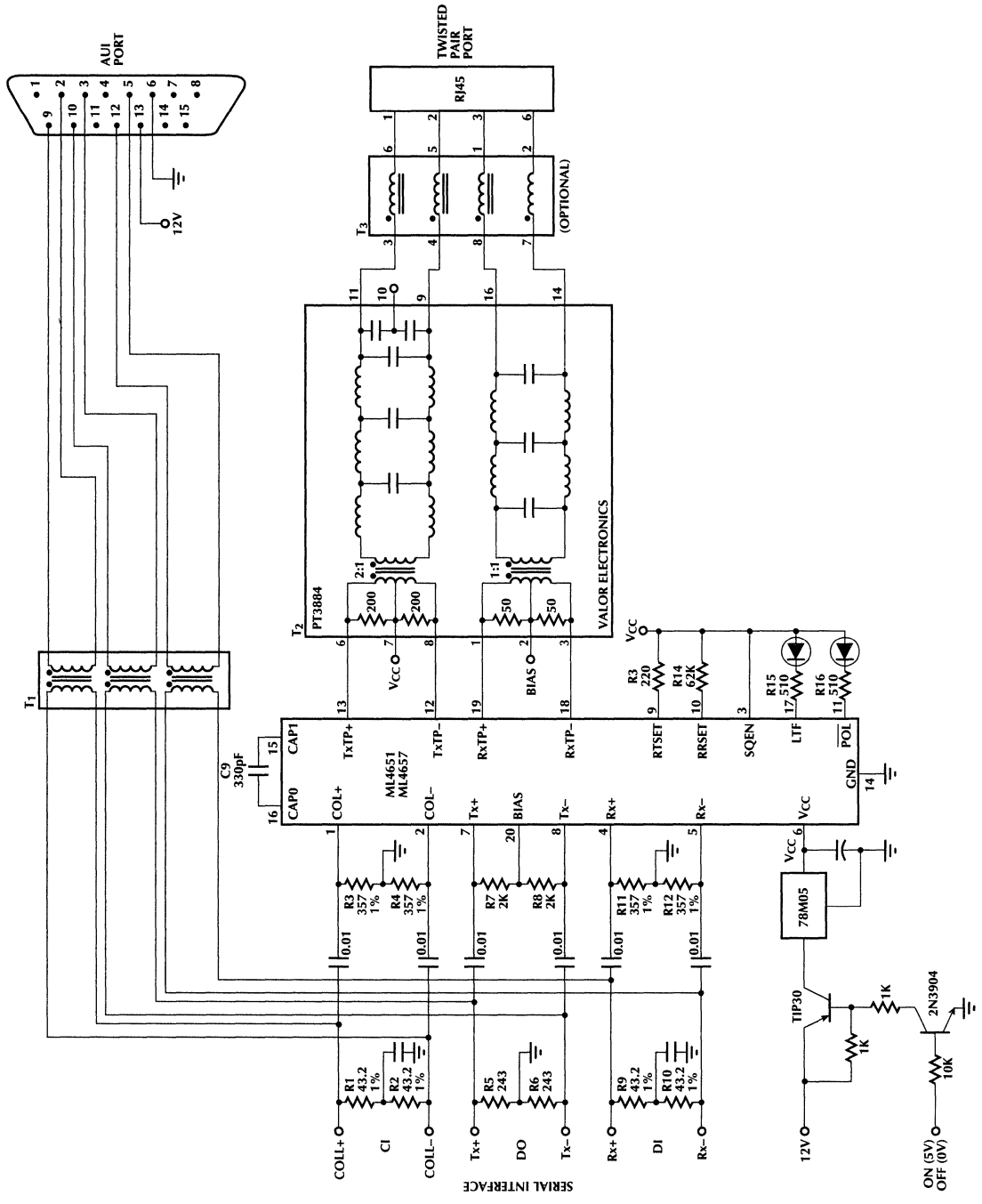


Figure 1. Internal MAU with Shared AUI Port

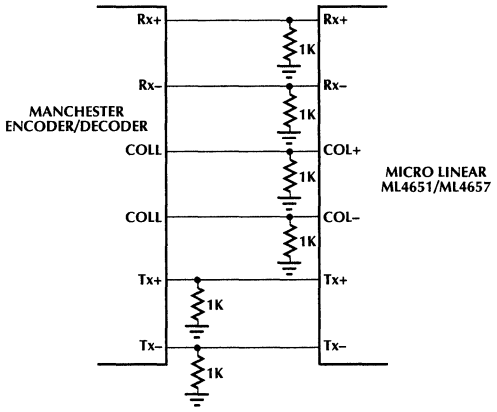
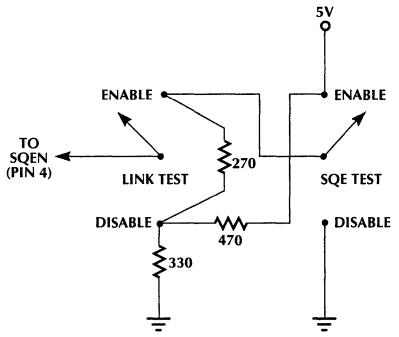


Figure 2. DC Coupled Interface for DTE Card Application

The isolation and filter components for both transmit and receive lines can all be integrated into one dip package style module. One such product can be obtained from Valor Electronics in San Diego. There are several other manufacturers who have these products available (refer to Figure 13 in the datasheet).

The output chokes shown in Figure 1 will pass any differential signal but block common mode voltages. Because Micro Linear's 10Base-T transceivers have very low common mode output voltage, this extra filtering choke may not be needed. Good board layout will also help.



SQE Test	Link Test	SQEN Pin 4
Enable	Enable	5V
Enable	Disable	3.3V
Disable	Enable	0V
Disable	Disable	1.2V

Figure 3. Mode Selection Circuit

EXTERNAL MAU

An external MAU design typically adds more LED outputs for status indication and adds circuitry for configuring the chip for SQE and Link Test options (See Figure 12 of datasheet). The selection of SQE and Link Test circuitry can be implemented in various ways. One such option is to use two SPDT switches to produce the proper voltage levels (Figure 3). The selected voltage to the SQEN input pin (pin #4 for ML4652 and ML4658) will internally configure the chip for the option to activate SQE test or Link test.

AUI DRIVER OUTPUT

The output structure of the driver stage connecting to the AUI is an open emitter type. The output is biased at typically 4.2V when high and 3.6V when low. That is a differential voltage of about ±0.6V across a 78Ω load which calculates to about 7.7mA output current during transmission. A 360Ω resistor at the output pin sets its current at 11.7mA when high and 10mA when low. In the case when the positive output is high, the current (I_O) flowing out of its drive transistor is the sum of 7.7mA and 11.7mA (Figure 4). That means the current flowing out of the negative output is 10mA minus 7.7mA. It then becomes apparent that the termination resistance must be low enough as to not shut off either of the output drive transistors but not too low as to saturate the transistor and dissipate excessive power.

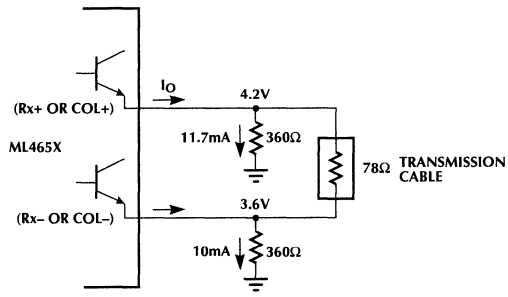


Figure 4. AUI Driver Circuitry

Micro Linear

Application Note 14

Generating Fixed Frequency Sine Waves with ML2035

Jon Klein

The ML2035 Programmable Sine Wave Generator is a convenient solution for generating accurate sine waves. Often an accurate fixed sine wave reference is required in applications such as Uninterruptable Power Supplies. Normally a microcontroller or microprocessor is used to program the ML2035's output frequency.

Most power supplies do not incorporate a microprocessor. This application note will show several alternate methods for programming the ML2035 for 50 or 60Hz sine wave output using off-the-shelf components.

The circuit in Figure 1 programs the ML2035 for 60Hz. The circuit shifts in the decimal number 141 to get to 60Hz with a NTSC color burst crystal (3.579545 MHz).

The 'HC4060 counter is used as an oscillator and timer. Q5 stays high for 16 clock cycles. During the first 8, the 'HC165 shifts out the codes on A thru H which are the complements of 141 (Binary 1000 1101) LSB to MSB respectively. During that time, SI on the 'HC165 shift register is also high. That means that for the next 8 clock cycles the Q BAR output will be low, loading in 0's for the most significant 8 bits. SCK on the ML2035 and CLK on the shift register are run from complementary phases of the oscillator, since the 'HC165 changes data on the rising edge of its CLK and the ML2035 latches the same data on the rising edge.

F_{OUT}	D(dec)	Hex Value	Binary Value	74HC165 Code ABCD EFGH	Frequency Error
50	117	75	0111 0101	1000 1010	–0.15%
60	141	8D	1000 1101	0111 0010	0.28%

Table 1. Data Codes for ML2035 using a 3.575945 MHz Crystal

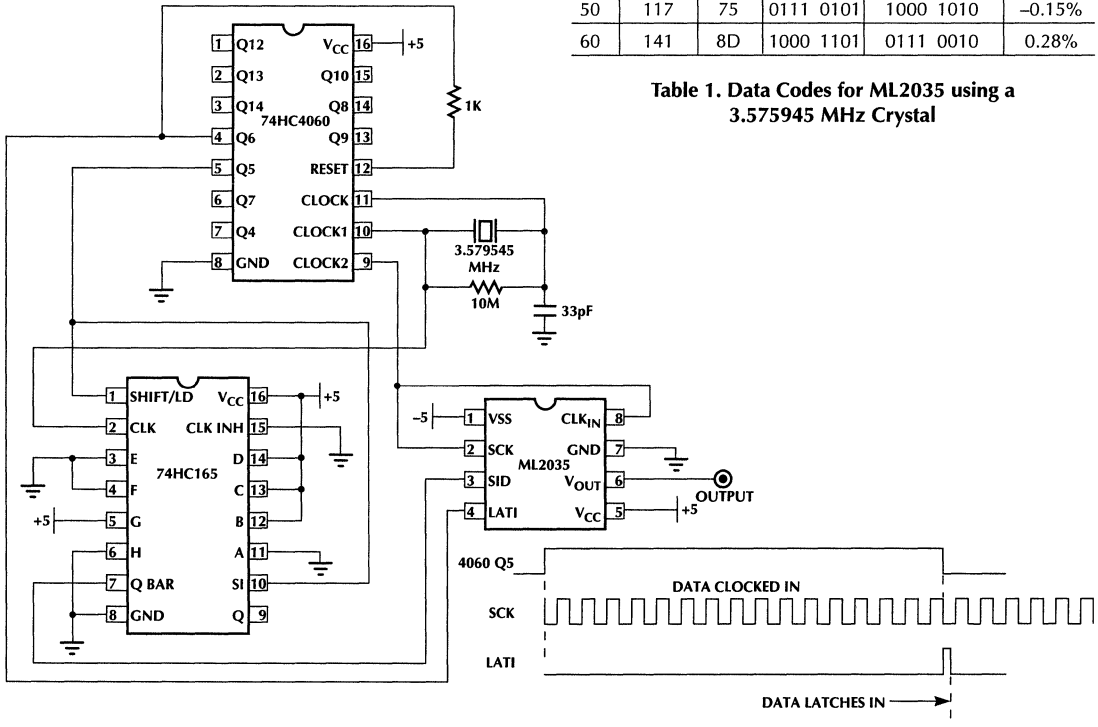


Figure 1. Programming the ML2035 for 60Hz. output using NTSC color burst crystal.

When Q5 goes low again, Q6 goes high providing a reset for the counter and also a short pulse for the LATI input. The 1K resistor between Q6 an the 4060 Reset line delays the reset slightly, effectively stretching the LATI pulse to 50nS.

This circuit could also be run from +10V and GND by creating an "artificial ground" at 50% of the 10V line (two 1K resistors and a 10µF capacitor).

For 50 Hz output use the code shown in the table 1.

The circuit in Figure 1 allows the use of an inexpensive and readily available crystal, but has the disadvantage of not being "single pin" programmable for 50/60 Hz. The circuit in Figure 2 requires a non-standard, more expensive crystal frequency but has the advantages of being pin programmable for 50/60 Hz and eliminating the shift register. A 2.4576 MHz crystal is a standard value. A frequency of 2.467238 MHz is required to generate exactly 50 and 60Hz with no error.

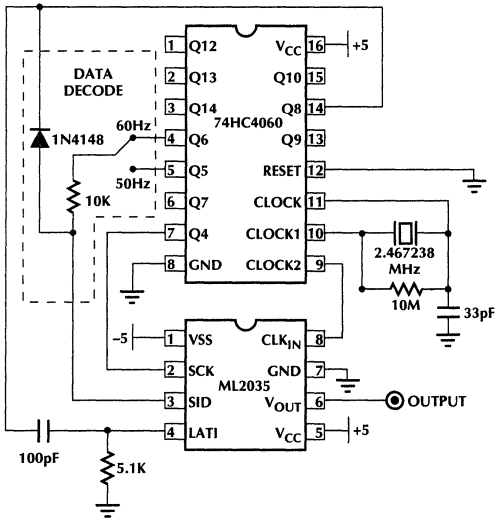


Figure 2. Single Jumper 50 or 60 Hz selection

These lower frequency (below 3.5Mhz) crystals, however tend to be larger in size and significantly more expensive.

F_{OUT}	D(dec)	Hex Value	Binary Value	Frequency Error
50	170	AA	1010 1010	–0.39%
60	204	CC	1100 1100	–0.39%

Table 2. Data Codes and error terms for ML2035 using a 2.4576 MHz standard crystal

Table 3 shows the codes necessary to generate 50 and 60 Hz sine waves with the circuit in Figure 1 from various standard crystal frequencies. Note that for the highest accuracy, the 4.194304 MHz crystal yields both 50 and 60Hz sine waves with no frequency error.

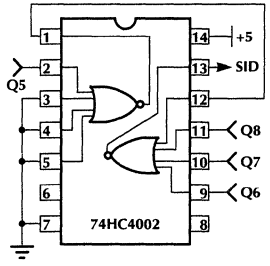
$F_{CRYSTAL}$ (MHz)	F_{OUT}	D(dec)	D(hex)	74HC165 Code ABCD EFGH	Error
4.00	50	105	69	1001 0110	0.14%
4.00	60	126	7E	1000 0001	0.14%
4.194304	50	100	64	1001 1011	0.00%
4.194304	60	120	78	1000 0111	0.00%
6.00	50	70	46	1011 1001	0.14%
6.00	60	84	54	1010 1011	0.14%
8.00	50	52	34	1100 1011	–0.82%
8.00	60	63	3F	1100 0000	0.14%

Table 3. Shift register values and frequency errors for various standard crystal values (fig 1).

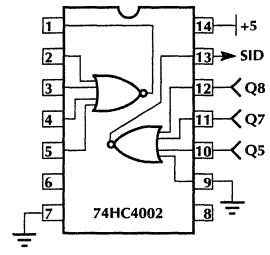
To generate 400Hz and 1KHz tones, the circuit of Figure 2 must be modified to shift in 0 for the first 8 clock pulses and the data in table 4 for the last 8 clocks. This can be accomplished by replacing the "Data Decode" blocks of Figure 2 with the decoding shown below.

$F_{CRYSTAL}$ (MHz)	F_{OUT}	D(dec)	D(hex)	74HC165 Code ABCD EFGH	Error
6.5536	400	512	200	1111 1101	0.00%
6.5536	1000	1280	500	1111 1010	0.00%

Table 4. Generating 400Hz and 1Khz sine waves



400Hz Decode



1Khz Decode

Suggested Crystal Manufacturers:

Nymph/Saronix: (415) 855-6829

Pletronics: (206) 776-1800

Manijeh Fadaee

Designing an IEEE 802.3 10BASE-FL Transceiver

INTRODUCTION

The ML4662 10BASE-FL Transceiver with the ML4621/ ML4622/ML4624 fiber optic quantizer construct both an internal and external 10BASE-FL MAU (Media Attachment Unit) described in the IEEE 802.3 standard. The ML4662 through its standard 802.3 AU (Attachment Unit) interface can be connected to an AUI cable, Ethernet Manchester Encoder/Decoder or Hub controller. The following topics will be discussed in this Application Note:

1) ML4662 Features
2) ML4621/ML4622/ML4624 (ML462X) Features
3) Filtering Power & Ground
4) Attachment Unit Interface
5) Interfacing ML4662 to National DP83950 Repeater Interface Controller
6) Interfacing ML4662 to AMD 79C980 Repeater
7) Interfacing ML4662 to AT&T T7202 Multi-Port Repeater
8) 10BASE-FL System Specification
9) Layout Considerations
10) Initial debug of the 10BASE-FL board

ML4662 FEATURES

The ML4662 integrates many of the functions needed for a 10BASE-FL transceiver. The Attachment Unit Interface complies with the IEEE standard offering Transmit, Receive, and Collision pair signals. Data transmission includes transmit squelch, a 1MHz idle signal, and the jabber function. The receiver accepts ECL compatible levels from the ML462X quantizer, passing through the receive squelch and into the AUI. The complete 10BASE-FL state machine is also incorporated including collision detect, loopback, and low light conditions.

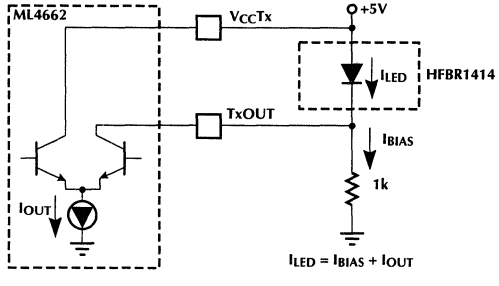


Figure 1.

One of the features is the capability to disable or enable the SQE function. This allows a 10BASE-FL transceiver to be connected to a DTE as well as a repeater. When connecting to a DTE, SQE must be enabled. When connecting to a repeater, SQE is disabled.

The ML4662 transmitter consists of a current driver output (TxOUT) which directly drives an HP fiber optic LED transmitter (HFBR1414). The output current is switched through the TxOUT pin during the on cycle and the V_{CC}Tx pin during the off cycle as shown in figure 1. Since the sum of the current in these two pins is constant, V_{CC}Tx should be connected as close as possible to the V_{CC} connection for the LED.

The 1KΩ pulldown resistor on the TxOUT pin prebiases the LED by applying a small forward current while the LED is in the "off" or low light state. The prebias current prevents the junction and parasitic capacitances from discharging completely when the LED is in the "off" state, thus reducing the amount of charge that the driver must transfer to turn the diode back on.

The resistor on the RTSET pin controls the amount of current driven by this pin (TxOUT). RTSET and the pulldown resistor together set the extinction ratio. To calculate RTSET value for a certain sink current (maximum 74mA) at TxOUT use this equation:

$$RTSET = (52mA/I_{OUT})\ 162\Omega$$

The ML4662 Transmitter has been designed to drive the cathode of the LED (note: higher optical power transmitted corresponds to the low logic state). Current flowing through the LED corresponds to a logic low. When Tx– > Tx+ (DO on AUI), current flows and this will be a logic low. When Tx+ > Tx– (DO on AUI), no current flows (except bias) corresponding to a logic high.

The receiver inputs are ECL levels (the ML4662 receiver inputs) coming from the ML462X. When $LMON_{IN}$ (TTL) coming from the ML462X is low, and the level of the received signal exceeds the receive squelch requirement, the receive data is buffered and transmitted out to DI pair.

The five LED status outputs are active low, open collector outputs. They provide a visible status of the link as follows:

$\overline{\text{XMT}}$: is on when transmission is taking place.

$\overline{\text{RCV}}$: is on when the transceiver is receiving a frame from the ML462X (V_{IN}+ and V_{IN}–).

$\overline{\text{CLSN}}$: is on when the transmitter and the receiver are active at the same time (collision). When a collision takes place a 10MHz ± 15% square wave with a 50% ±10% duty cycle will be sent out to COL+ and COL– output pins.

$\overline{\text{JAB}}$: turns on when the transmitter is on for more than 20 to 150 msec. When the jabber is on, in order to not bring down the network, the jabber logic disables the transmitter and turns on the collision signal COL+ and COL–.

$\overline{\text{LMON}}$: is on when LMON_{IN} coming from the ML462X is low and there are signal transitions on RX+ and RX–.

ML462X FEATURES

The ML462X data quantizer is used for signal recovery applications in Fiber Optic systems. The ML462X has a wide bandwidth and large gain which makes it capable of accepting an input signal from a fiber optic receiver as low as 2mV. This analog input gets converted to digital outputs at the TTLOUT pin or ECL+ and ECL– output pins.

The TTL output has been disabled in this Application Note by pulling up TTL_{VCC} and TTL_{GND} since ECL output levels are required by the ML4662. The 3K pulldown resistors on the ECL outputs of the ML4621 keep the outputs biased in their operating range. Due to internal pulldown resistors in the ML4622 and the ML4624, the external pulldown resistors are not required if the ECL output are the only outputs being used. The ML4662 inputs present a minimal load to the ML462X ECL outputs.

ML462X includes a two stage input limiting amplifier with a DC restoration feedback loop. The bandwidth of the ML4621 can be adjusted to the particular needs of the application with the capacitor across pin 7 and 8 (CF1 and CF2 for high corner frequency). The 0.1µF (ML4621) or the 0.01µF (ML4622/24) input capacitors on V_{IN}+ and V_{IN}– set the low corner frequency. (The output source impedance of the fiber optic receiver must be kept low "about 50Ω" to make the input capacitors on V_{IN}+ and V_{IN}– effective).

Since the logic condition for the 802.3 FOIRL is as follows:

"light" = 0
"dark" = 1

The received signal has to get inverted before it goes to the RXIN+ & RXIN– inputs of the ML4662. When the output of the Fiber Optic receiver (HFBR2416) is connected to the V_{IN}+ of the ML462X, the signal is non-inverted at the ECL+ & ECL– outputs. Therefore, the ECL+ must be connected to the RXIN– of the ML4662 and the ECL– to the RXIN+ of the ML4662. The output of the Fiber Optic receiver (HFBR2416) may be connected to the V_{IN}– of the quantizer to invert the ECL outputs of the ML462X. If this is done, the following connections must be made.

ECL+ → RXIN+
ECL– → RXIN–

The Link Monitor function is implemented by the minimum signal discriminator and the threshold generator circuits. The $\text{TTL}_{LINKMON}$ and $\text{ECL}_{LINKMON}$ outputs both indicate when the input data signal is less than a user defined acceptable level. This is done by monitoring the input signal and peak detecting the output of the limiting amplifier and comparing this level with the voltage at V_{THADJ}. V_{THADJ} is set by the user as specified in the data sheet. To set the minimum input signal of the ML4621 to 3mV, V_{REF} can be tied directly to V_{THADJ} to provide 2.5V at V_{THADJ}.

ML4621: $V_{THADJ} = 600\ V_{INTH(P)} + 0.7$ (1)
ML4622: $V_{THADJ} = 500\ V_{INTH(P-P)}$ (2)
ML4624: $V_{THADJ} = 417\ V_{INTH(P-P)}$

In these equations V_{INTH} is the peak or peak to peak value of the input signal. The receiver sensitivity can be calculated when the Hewlett Packard HFBR2416 with a typical responsivity of 6mV/µW is being used.

ML4621: $V_{INTH(P)}$ = 3mV(Peak) ($V_{THADJ} = V_{REF}$)
Received Power = 6mV(P–P)/(6mV/µW)
= 1µW = –30dBM (PEAK)

ML4622: $V_{INTH(P-P)}$ = 5mV(Peak to Peak)($V_{THADJ} = V_{REF}$)
Received Power = 0.833µW = –30.7dBM (PEAK)

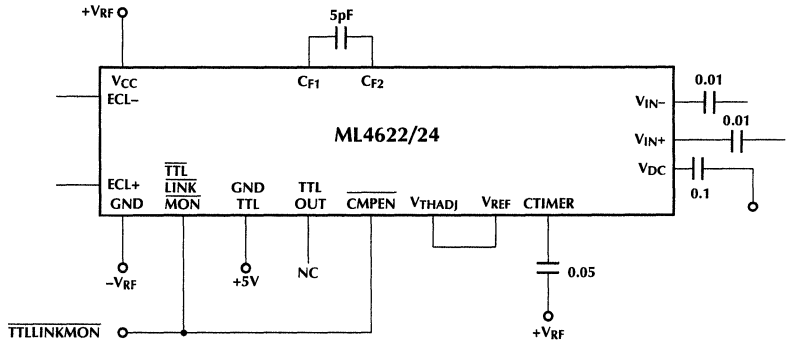
Note: Peak Power = Average Power + 3dBM

This meets the IEEE802.3 10BASE-FL receiver specifications. A lower threshold level can be set by dividing down V_{REF} with a resistor divider, as shown in Figure 2b. By choosing 1K and 140Ω, the V_{THADJ} will be 2.2 volt in the ML4621 which will set the minimum power level at about 2.4mV peak and minimum launch power at –33dBM (considering worst responsivity of 4.5mV/µW). However due to a better stability of the link monitor in the ML4622, both standards will be met considering the worst conditions by tying the V_{THADJ} to V_{REF}. For more detailed information refer to Application Note 6 and Application Brief 1.

In the case of oscillation at $\text{TTL}_{LINKMON}$, hysteresis can be added to the ML4621 in two different ways as follows:

1. Adding a feedback resistor from the $\text{TTL}_{LINKMON}$ output to the V_{THADJ} (this will only work if a resistor divider is being used to arrive at V_{THADJ}).
2. A capacitive feedback can be implemented by connecting a capacitor from the $\text{TTL}_{LINKMON}$ to the ISET pin on the minimum signal discriminator (this will apply if V_{REF} is tied to the V_{THADJ}.
   Note: Adding a 300 ohm to 600 ohm pull-up resistor at the $\text{TTL}_{LINKMON}$ to +5Volt may be needed for the stability.

Based on the layout, the value of the hysteresis resistor and capacitor change. Since hysteresis has been added internally to the ML4622 and the ML4624 to increase the stability, the external hysteresis components are not required.



NOTE: IF TTLOUT IS USED, TIE GNDTTL TO UNFILTERED GROUND AND REMOVE L1. IF TTLOUT AND ECL OUTPUTS ARE BOTH USED, ADD 3k PULLDOWN RESISTORS AT ECL OUTPUTS.

Figure 2A. Fiber Optic Receive Circuit A

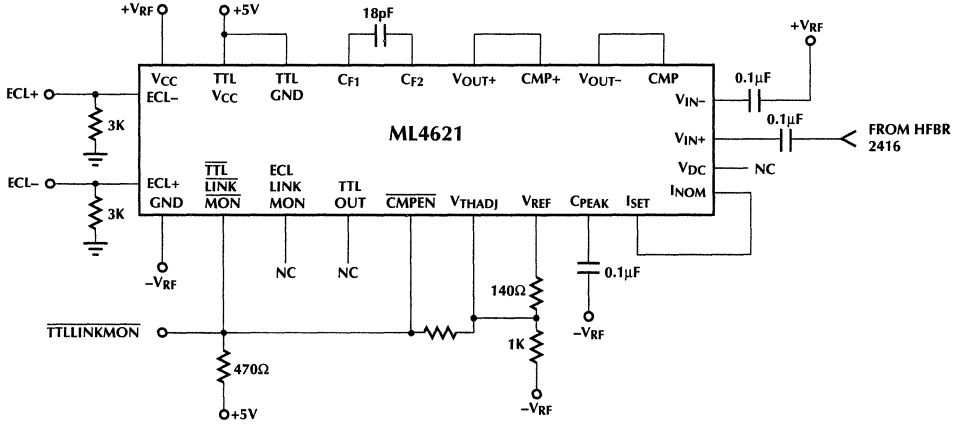


Figure 2B. Fiber Optic Receive Circuit B

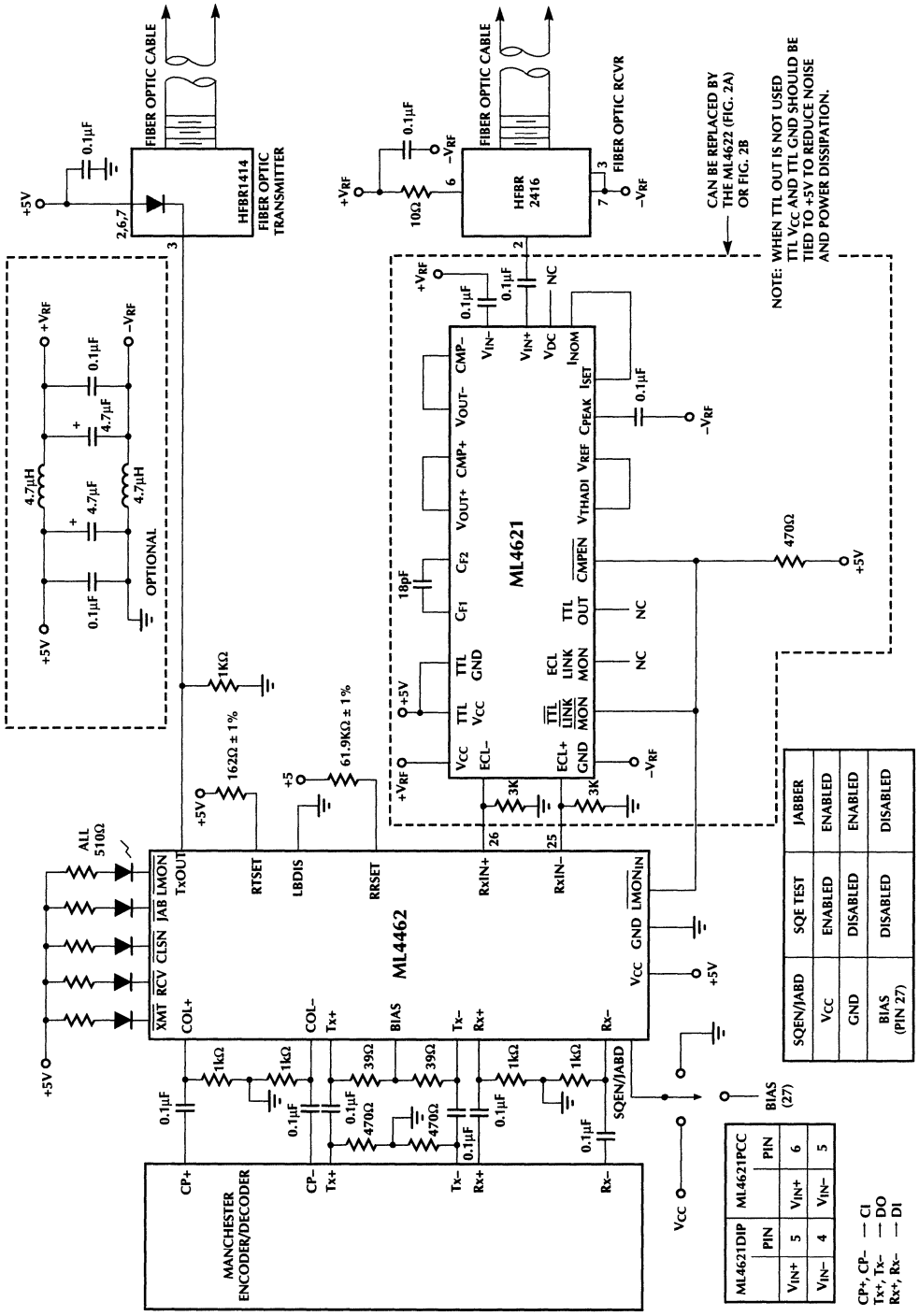


Figure 3. Internal MAU with AC Coupling

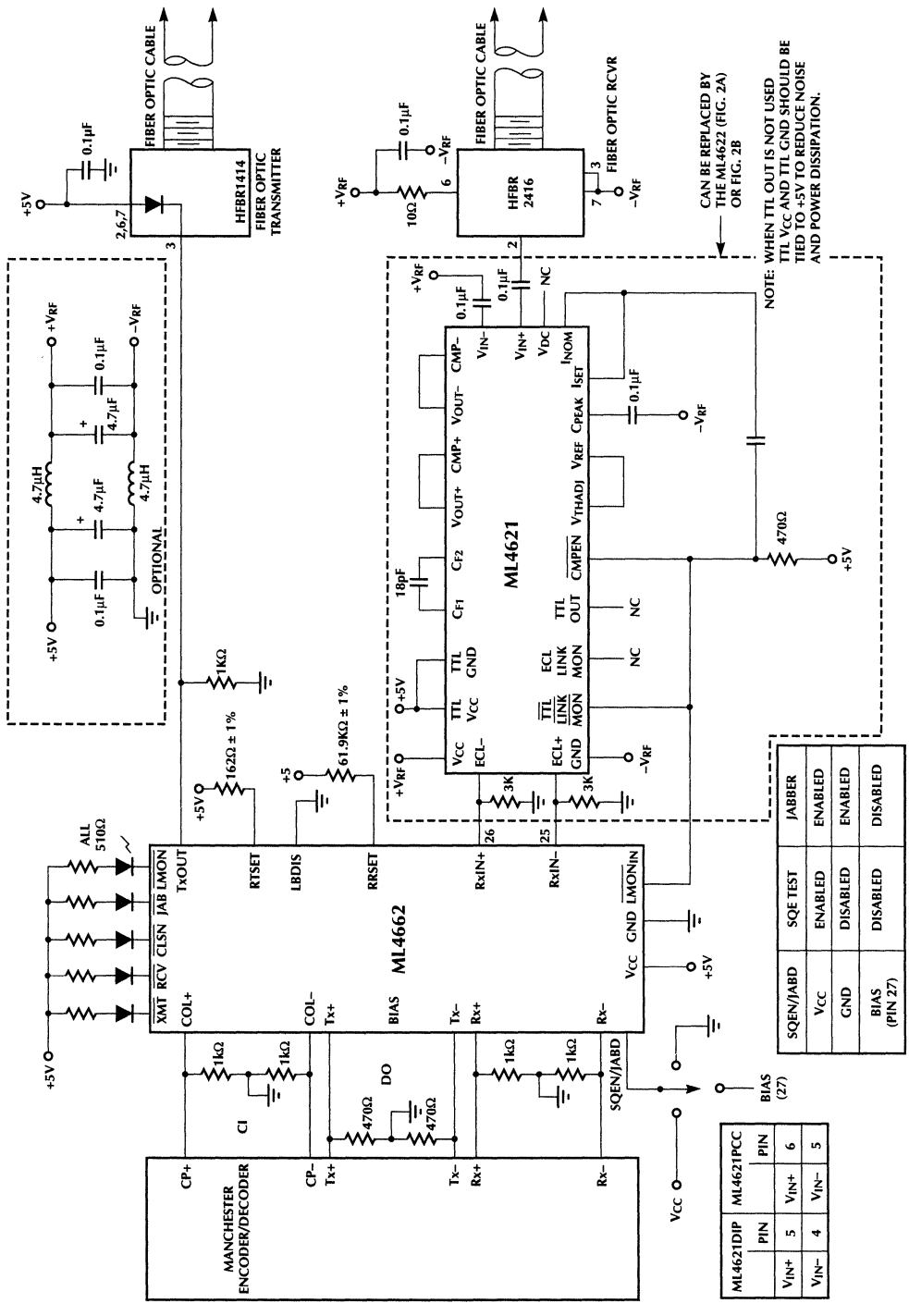


Figure 4. Internal MAU with DC Coupling

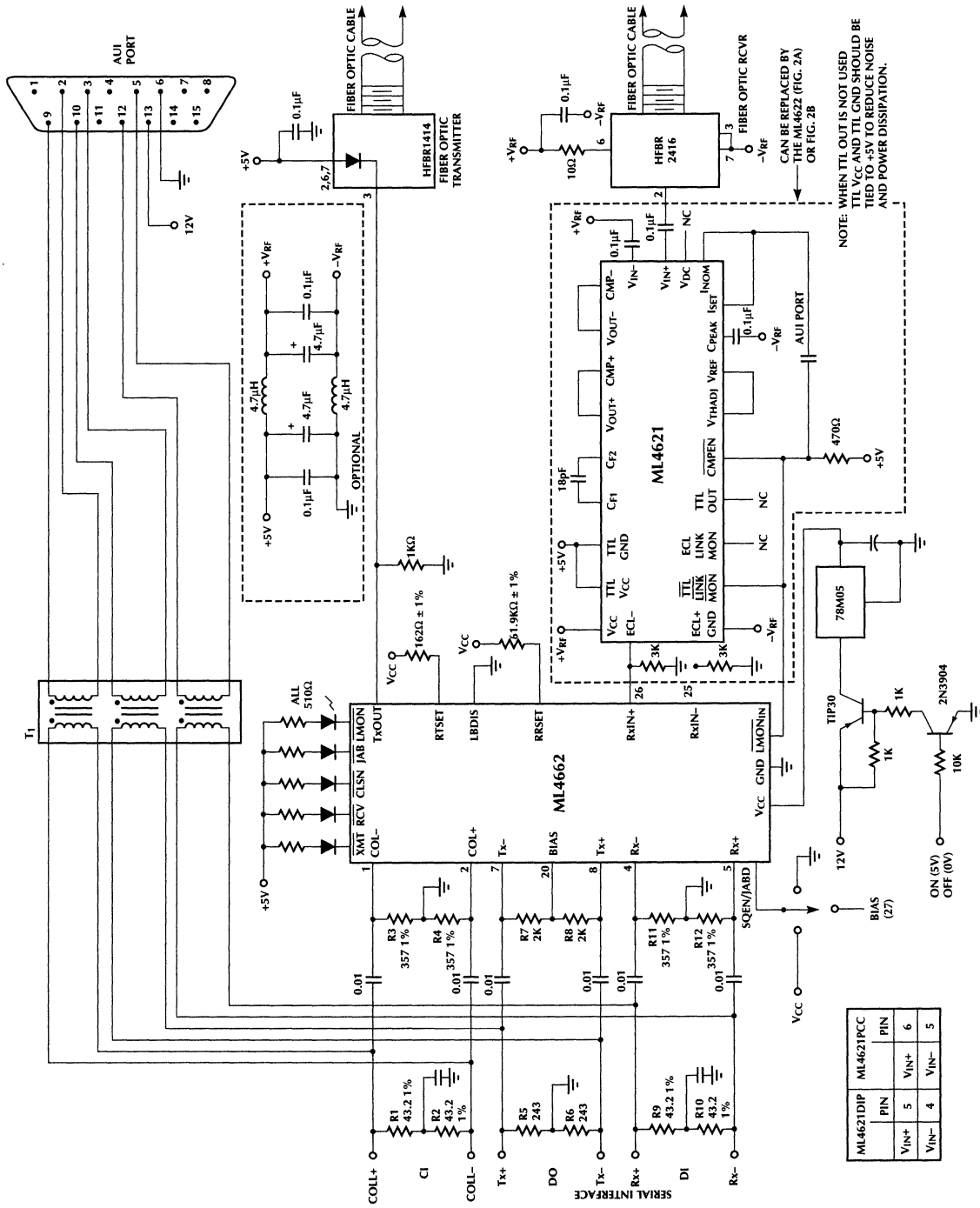


Figure 5. Internal MAU with Shared AUI Port.

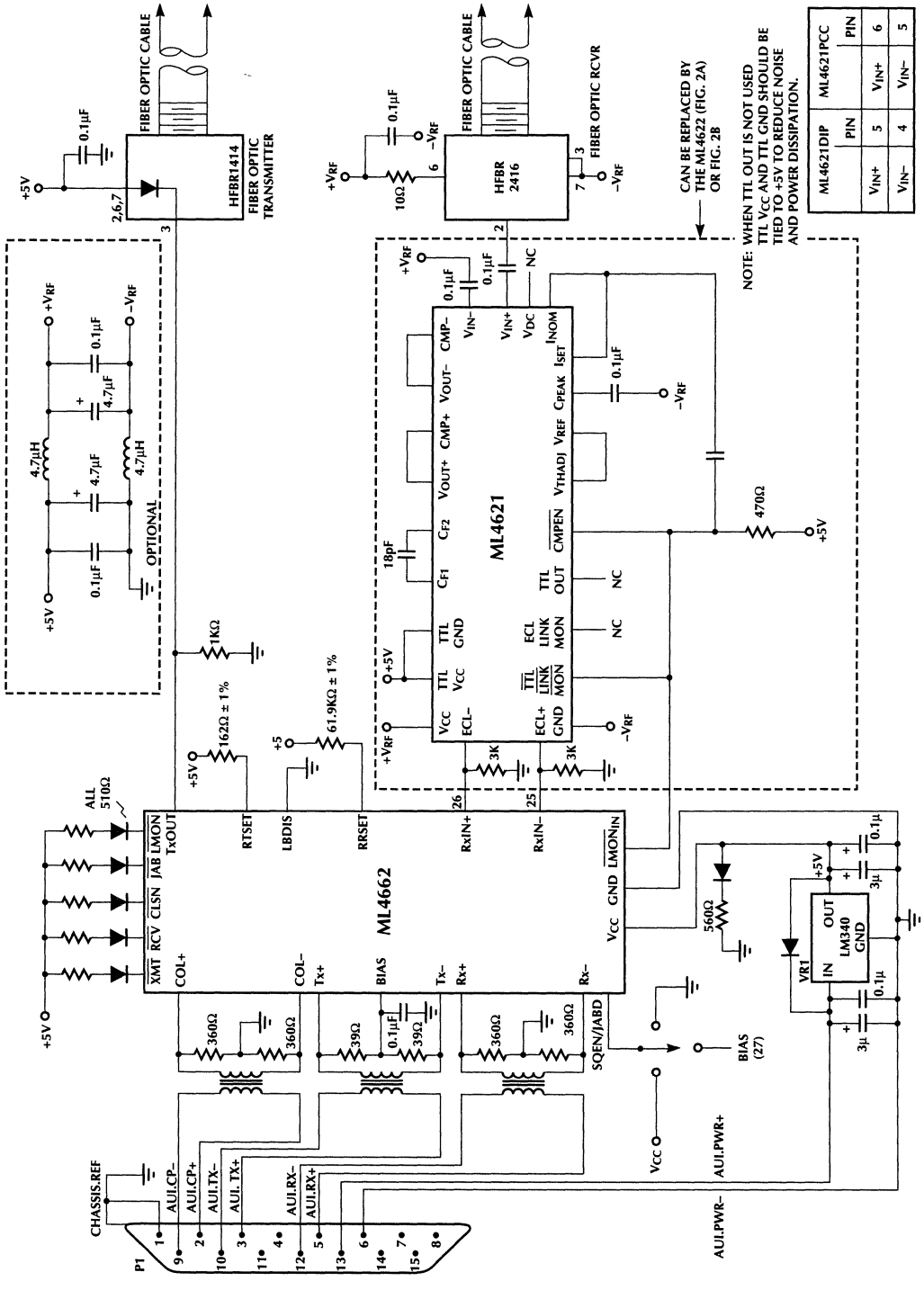


Figure 6. External MAU

FILTERING POWER AND GROUND

Filtering is necessary since unintended feedback through the power supply system (the metallic conductive path of the +5V power line or the Ground reference line for the receiver) can create sustained oscillations or degrade the sensitivity of the receiver. Filters in the power supply for the post-amplifiers, comparator stages and the receiver, prevent noise generated by the quantizer output from being conducted back through the power system to the input amplifier stage.

The quantizer inputs are sensitive low level inputs. V_{CC} and Ground Decoupling are necessary. Disabling the TTL output (by connecting TTL_{GND} and TTL_{VCC} to V_{CC}) of the quantizer will also reduce noise.

ATTACHMENT UNIT INTERFACE

The ML4662 and the ML462X can be used as an internal MAU with the option of having a shared AUI port or as an external MAU. Figures 3, 4, 5 and 6 show a detailed schematic for these three configurations.

Internal MAU: The AU interface may be AC coupled through 0.1µF capacitors across DO, DI, CI pair (Figure 3). They may be DC coupled if the DC levels DO (2V to V_{CC} – 0.5V), DI (3.6V to 4.5V), CI (3.6V to 4.5V) of the manchester encoder/decoder & the ML4662 are the same (Figure 4). (If DC coupling is used, the BIAS pin is not connected and the 39Ω resistors are not needed.) If AC coupling interface is used, DO which is an input must be DC biased (shifted up in voltage) through the BIAS pin for the proper common mode input voltage.

DI and CI are emitter follower outputs which need external 1KΩ or greater (depending on the particular manchester encoder/decoder) pulldown resistors to ground.

By using 1K pull down resistors we can minimize power dissipation by not having to drive the 78Ω AUI cable.

Internal MAU with Shared AUI Port: The AU interface is AC coupled through isolation transformers T1 (Figure 5). This is to protect the transceiver chip, from 16V with respect to the system ground at AUI interface during a fault condition (as specified in 7.4.1.6 and 7.4.2.6 section of the IEEE 802.3 standards for both the driver and the receiver). In addition, it blocks the DC offset voltage of the AUI port that may not match that of the transceiver. An AUI connection requires termination impedance of 78Ω [(R1 + R2)||(R3 + R4)] on the receive end of the transmission lines (DI and CI). The 357Ω resistors for R3 and R4 are chosen to properly bias the driver circuitry. The 2K resistors on TX+ and TX– provide common mode bias input voltage for the ML4662.

The 243Ω resistors (R5, R6) drive the DO pair (either the DO pair of the AUI port of the ML4662). The output AUI drivers of the transceiver must be tri-stated in order to not load down the transmission lines when the AUI port is connected and the FIBER OPTIC port is disconnected.

When the device is powered down, the TX±, RX± and COLL± pins form a substrat diode to the ground. Hence, the output of DO, DI and CI is clamped to one diode drop. Since this is not desirable, we need to add six 0.01µ capacitors at these pins as shown in figure 5. This way we isolate the Manchester Encoder/Decoder at TX pair and the AUI at RX and COL pairs.

+5V to the chip and to all the circuit must be removed when the chip is powered down. This includes power to the chip, +5V at RRSET and RTSET resistors and all status LEDs.

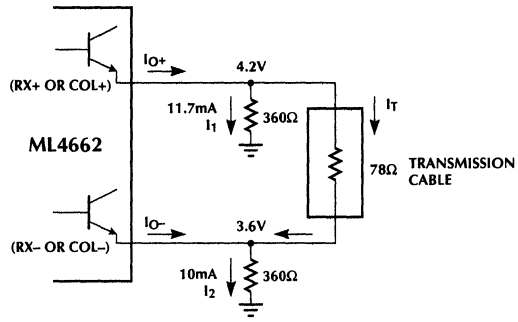


Figure 7. AUI Driver Circuitry.

External MAU: The AU interface is AC coupled through isolation transformers (Figure 6). An AUI connection requires termination impedance of 78Ω. Two 39Ω, 1% resistors tied to DO pair provide impedance matching (78Ω) as well as the proper common mode input voltage to the ML4662.

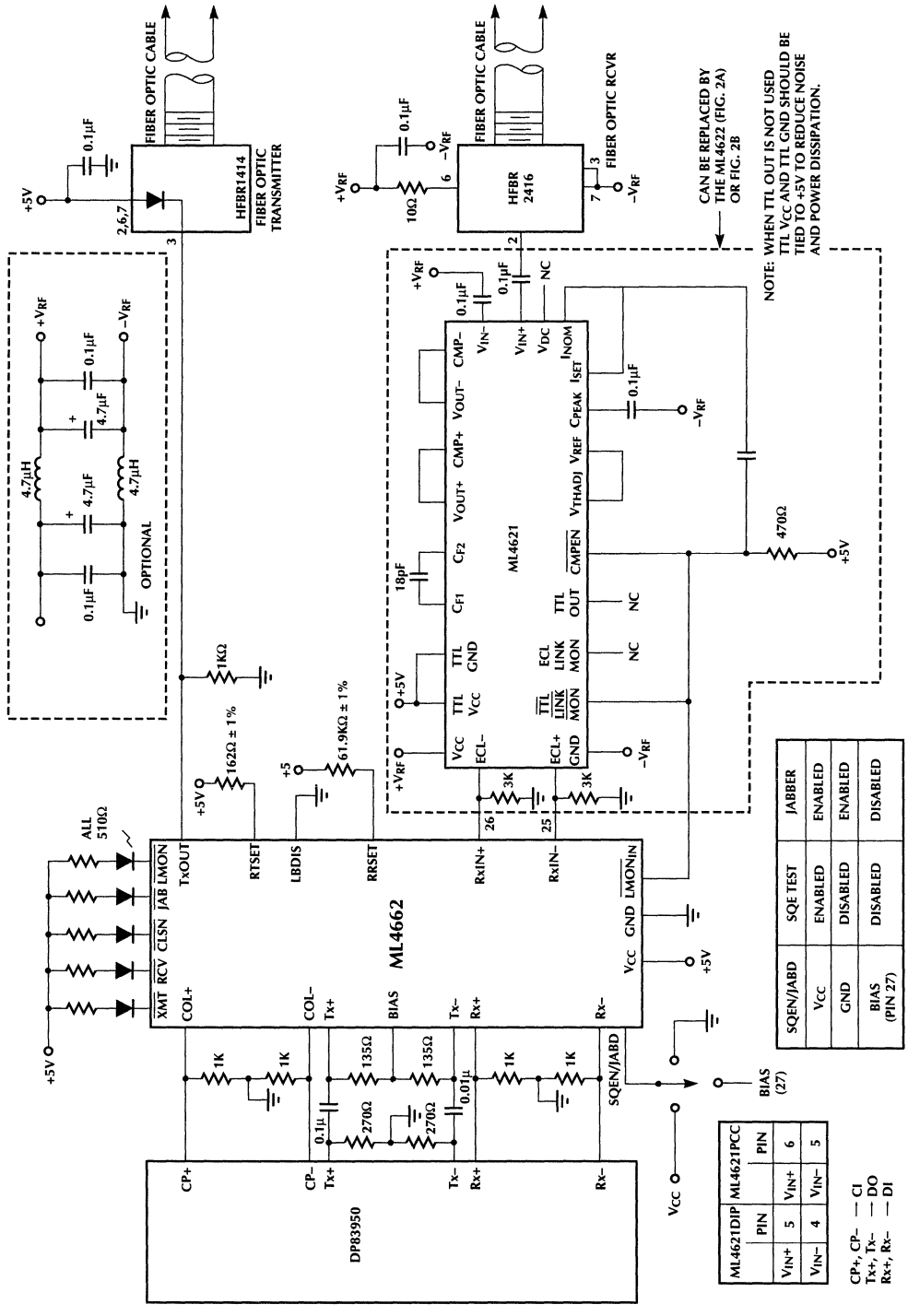
DI and CI pairs are emitter follower outputs. The output structure of the driver stage (RX+, RX–, COL+, COL–) is open emitter (Figure 7). The output is biased at typically 4.2V when high and 3.6V when low. That is a differential voltage of about +0.6V across a 78Ω load.

The pulldown resistors have to be chosen such that during transmission, a minimum of 2.0mA can be sourced by RX– or COL–. By using a 360Ω pulldown resistors the RX– or COL– source 2.3mA and the RX+ or COL+ source 19.4mA as follows:

$I_T = 0.6V/78\Omega = 7.7mA$

$I_{O+} = I_1 + I_T$
$I_{O+} = (4.2V/360\Omega) + 7.7mA$
$I_{O+} = 11.7mA + 7.7mA$
$I_{O+} = 19.4mA$
$I_{O-} + I_T = I_2$
$I_{O-} = I_2 - I_T$
$I_{O-} = (3.6V/360\Omega) - 7.7mA$
$I_{O-} = 10mA - 7.7mA$
$I_{O-} = 2.3mA$

The termination resistance must be low enough (minimum 200Ω) to not shut off either of the output drive transistors, but not too low in which case the output transistors could saturate.



ML4621DIP		ML4621PCC
PIN		PIN
V_{IN+}	5	6
V_{IN-}	4	5

Figure 8. Interfacing the ML4662 to DP83950

INTERFACING ML4662 TO DP83950 OR DP83955

The ML4662 and ML462X can be used in a HUB application. Figure 8 shows the interface between the ML4662 and the National Semiconductor DP83950 Repeater Interface Controller (RIC) The DI and CI pairs are DC coupled but DO is AC coupled with 0.01µF in each lead. The 1KΩ pulldown resistors on the DI and CI pairs provide the necessary source current to drive DI & CI pairs.

N-PORT FIBER REPEATER

To build a fiber repeater network we need to use existing 10BASE-T multiport repeater controller chips with fiber optic transceivers. National (DP83950 or DP83955) and AMD (79C980, IMR), repeater chips, can be interfaced to the ML4662 10BASE-FL transceiver. Each Twisted Pair (TP) port of these chips has an internal 10BASE-T transceiver. A different approach should be taken for designing the ML4662 with these chips.

National Repeater: The integrated 10BASE-T transceivers in the National repeater chip can be disabled. Since each Twisted Pair (TP) port is compatible with AUI (Attachment Unit Interface) compliant transceivers, we interface each TP port to the ML4662 through the AUI interface as shown in figure 8. The receive and collision pair (RX±, COL±) are DC coupled and the transmit pair (TX±) is AC coupled. AC coupling is needed at the transmit pair due to different common mode voltage between the TX± of the ML4662 and the National chip. Loopback is enabled in the ML4662 in order to have collision circuit enabled.

AMD repeater: The TP ports in the IMR repeater chip are designed to interface to 10BASE-T only, and it is difficult to interface them to AUI. So the interface between the IMR and the ML4662 is through the AUI of the ML4662 and the TP port of the IMR. To have a successful link, the following steps should be done:

— Link test pulse should not be sent to the ML4662. Since the link test pulses does not get generated on the TXD– of the IMR chip, this pin drives the TX– of the ML4662 as a single ended input, figure 9.

— A resistor divider is used to biased the TX+ of the ML4662 properly (about 3.2V).

— Another resistor divider is used to bias the receive data at RXD– of the IMR.

— The IMR detects a collision during simultaneous transmission and reception. So, the CI pair (COL±) of the ML4662 is not used in this design.

— A 100 ohm resistor eliminates the reflection and it takes care of over driving the TX– by the TXD–.

— A 100 ohm resistor might be needed to eliminate reflection due to the length of RX+ signal line.

— A pulldown resistor at the RX+ of the ML4662 satisfies the ML4662 output requirement.
A 0.1µF capacitor is used to AC couple the receive signal due to different common mode voltage range of the RX+ and RXD+.

— Loopback on the ML4662 should be disabled. This is due to interpreting loopback data as collision by the IMR.

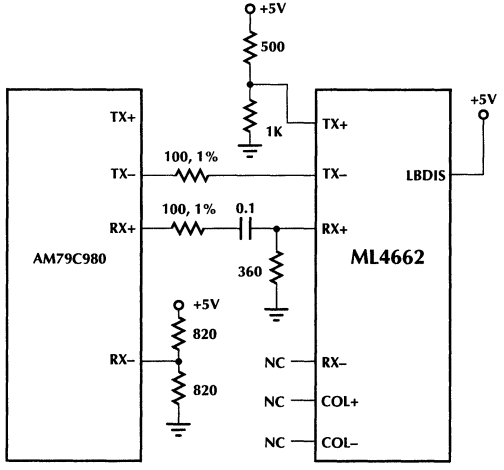


Figure 9. Interfacing the ML4662 to the AMD Repeater

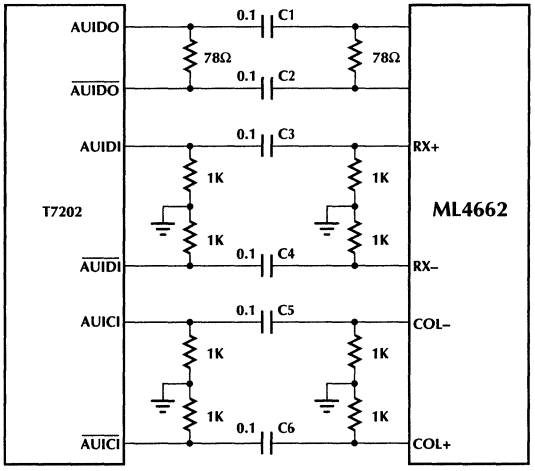


Figure 10. Interfacing the ML4662 to the AT&T Repeater

Interfacing the ML4662 to T7202: T7202 is AT&T multiport repeater controller IC with 12 twisted pair ports and 2 AUI ports. The ML4662 can interface to the AUI port of the T7202 without the need for a transformer as shown in figure 10. The following should be done:

— The DO pair (TX+ and TX–), input to the ML4662 must be DC biased for the common mode input voltage. This is accomplished by having two 39 ohm resistors to the BIAS pin of the ML4662.

— The CI pair should be wired with the reversed polarity so that COL+ of the ML4662 goes to the CI of the AT&T part and the COL– to the CI+.

10BASE-FL SYSTEM SPECIFICATIONS

Some of the key parameters required by the IEEE 802.3 10BASE-FL Standard are listed below:

Transmitter Specifications

1. Peak Emission Wavelength = 790 to 860nm.
2. Spectral Width < 75nm. This is determined by measuring the Full Spectral Width at Half Maximum Amplitude (FWHM) of the LED optical emission. This parameter must be measured at the maximum temperature at which the LED will be operated.
3. Minimum Extinction ≥ 13dB
   Extinction = $|P_{I(ON)} - P_{T(OFF)}|$, where P_T = peak transmitted optical power measured in dBm.
4. Optical Rise/Fall time T_R and T_F < 10ns.
5. $|T_R - T_F| \leq 3$ns.
6. Transmitter Jitter ≤ 2ns.
7. Nominal average power, beginning of life –15dBm
8. Transmit power tolerance ±3dBm
9. Transmit power degradation, end of life –2dB

Receiver Specifications

1. Overdrive limit = –12dBm (average) maximum.
2. Sensitivity ≥ –32.5dBm (average) minimum.
3. The data output of the receiver must be inhibited before the Bit Error Ration of the fiber optic link degrades to greater than 10^{-9}.

Total Link Specifications

1. Transmitter/Receiver must be compatible with fibers having the following core/cladding diameters: 50/125, 62.5/125, 85/125 and 100/140.
2. Link must operate at least at a maximum length of 2Km with each type of fiber.

LAYOUT CONSIDERATIONS

The fiber optic transceiver consisting of the ML4662 transceiver and the ML462X fiber optic quantizer are simple to implement from a data point of view. Electrically, the quantizer is resolving 2mv signals in a logic environment that has an abundance of 5 volt signals. The fiber optic receiver and the quantizer require careful layout, attention to noise coupling, and very clean power supply busses. The following recommendations should be considered while laying out the printed circuit artwork.

POWER SUPPLY

1. Isolate and filter the power and ground to the ML462X (analog portion) and HP receiver (to ensure that noise is not coupled into the low level receiver inputs). This can be accomplished with a pi filter that has a 4 to 7µH inductor in both the power lead as well as the ground lead.
2. Make sure that adequate decoupling is used on both sides of the pi filter, on each chip, and at the fiber optic transmitter and receiver. The fiber optic receiver should be decoupled from the +5 Volt Filtered bus with a 10 ohm resistor and decoupling capacitor. Allow room for large (0.47µF) decoupling capacitors and determine if they can be reduced during testing of the prototypes.

GROUND PLANE

1. The printed circuit board should be a 4 layer board with the +5V. and ground each providing a shielding plane on the inner layers. The fiber optic receiver and the ML462X analog front ends should have its own power supply planes separate from the +5 Volt and Ground planes for the remaining circuitry. These planes should be separated by an air gap physically and electrically by the power supply pi filter from the logic +5 volt and ground.
2. Connect unused pins of HP receiver to the low level receiver Ground.

TRANSMITTER

1. The transmitter output (TXOUT) traces should be as short as possible and make them wide to lower their characteristic inductance.
2. Keep RRSET and RTSET traces (of the ML4662) and resistors away from each other.

GENERAL LAYOUT

1. The physical layout for the receiver should be in a straight line to minimize the trace lengths and potential for noise coupling between the logic signals at the output of the quantizer and the low level signals on the inputs.
2. The trace from the output of the HP fiber optic receiver to the ML462X (V_{IN}+, V_{IN}–) should be as short as possible and shielded if possible.
3. Because of the high gain low level input circuitry in the ML462X, parasitic feedback from the high-level logic-compatible output must be kept to a minimum in order

to prevent undesired oscillations. This is accomplished with a layout which physically separates the receiver inputs (V_{IN}+, V_{IN}–) and outputs (ECL+, ECL–, TTLOUT, CMPEN, $TTL_{LINKMON}$, $ECL_{LINKMON}$).

4. If the TTL outputs of the ML462X are not used, Connect GNDTTL and VCCTTL to +5 volt (this will disable the TTL driver).

INITIAL DEBUG OF THE 10BASE-FL BOARD

1. AUI is connected but Fiber Optic cable is not connected.

   a. Look for 1MHz Idle signal at pin 18 of the ML4662. If there is no Idle signal, verify the following:

      i) Ground and +5V to the ML4662.
      ii) RRSET must be 61.9k (1%) at pin 13 of the ML4662 to +5V
      iii) RTSET should be 162 ohm at pin 12 of the ML4662 to +5V to set the current driven by the TxOUT to 52mA.

   b. The LMON LED must be OFF. If the LMON LED is ON, check the $TTL_{LINKMON}$. If it is low, measure the noise level at filtered power and ground, V_{IN}+ and V_{IN}– of the ML462X. If the peak noise level at the input of the ML462X is greater than the minimum V_{INTH} (Equations 1 and 2), the $TTL_{LINKMON}$ gets activated (low).

   c. The RX LED must be OFF. Otherwise there must be transitions on RX+ and RX– (pins 25 and 26 of the ML4662) less than 3µsec apart because of one of the following reasons:

      i) Too much noise at the inputs of the ML462X (not filtering properly).
      ii) Feedback between the inputs and outputs of the ML462X (poor layout).
      iii) Crosstalk between TxOUT (pin 18 of the ML4662) and inputs of the ML462X (poor layout).

2. Connect Receive Fiber (HFBR2416) to Fiber Optic LED transmitter (HFBR1414) which is sending active idle signal. (Either from another MAU's LED transmitter or from the same MAU's LED transmitter with loopback disabled.)

   a. The LMON LED must go ON and the RX LED must be OFF. If the LMON LED is OFF, verify the following steps:

      i) The Receive Power must be within the 10BASE-FL standard range.
      ii) Verify the idle signal at V_{IN}+ or V_{IN}– of the ML462X
      iii) $TTL_{LINKMON}$ (pin 2 of the ML462X) must be low.

   b. If the RX LED is ON as well as the LMON LED, check step 1c.

3. Start to transmit. The LMON and TX LEDs must be ON. The RX and CLSN LEDs must be OFF in the transmitting MAU if two MAU's are being used. In this case, if the RX and CLSN LEDs are on, check step 1c.

4. Disconnect the Fiber Optic cable from the HFBR2416. The LMON LED must go OFF. If the LMON LED stays on, check step 1b. The RX LED must be OFF. Otherwise check step 1c.

5. After successfully completing the initial debug of the 10BASE-FL board, verify that the board meets 10BASE-FL specifications.

Figure 11 is schematic of the 10BASE-FL evaluation board (ML4662EVAL) which meets the 10BASE-FL standard. This board incorporates all the above critical points of the layout as shown in Figures 12 through 17. The ML4662EVAL is available for purchasing.

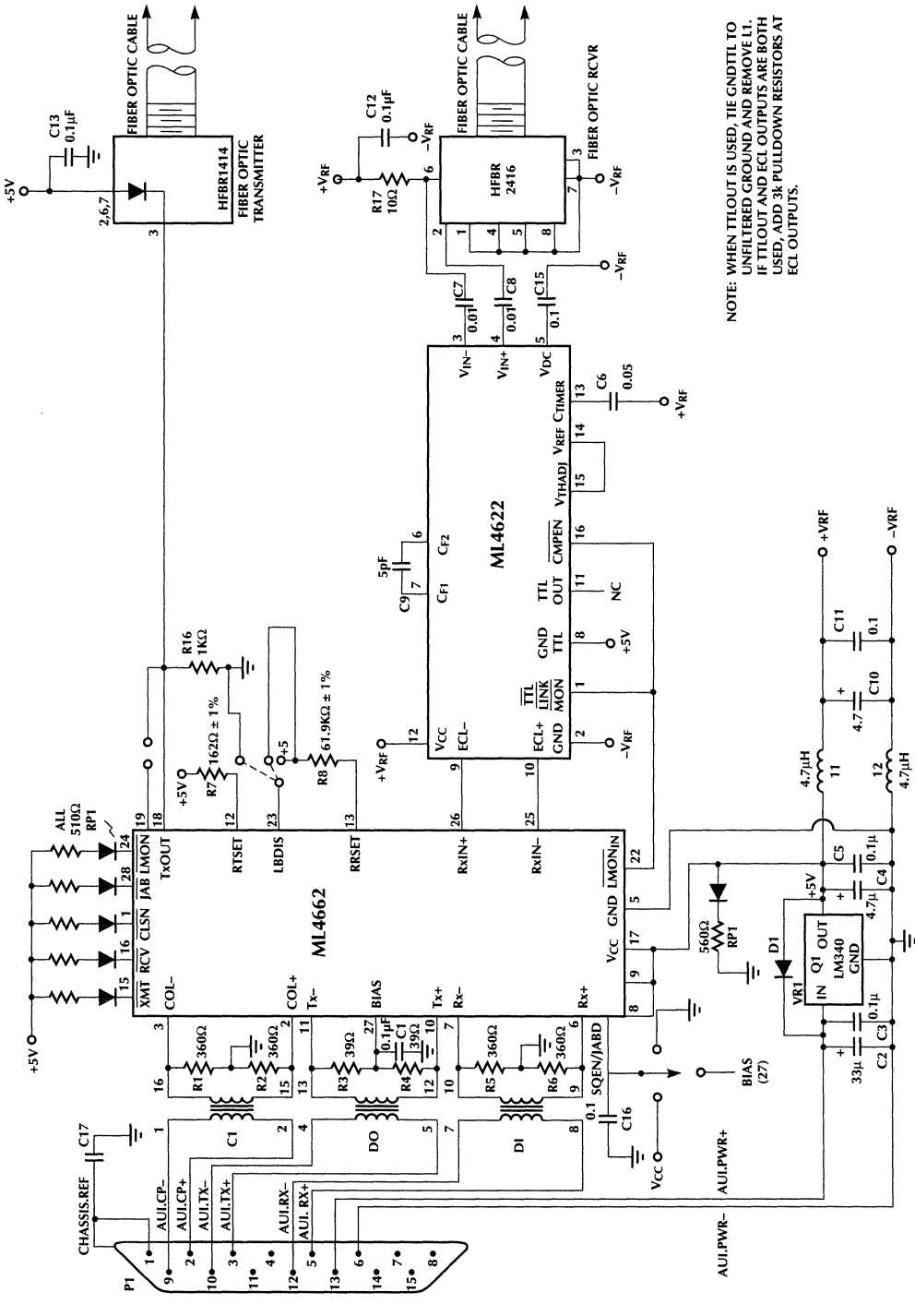


Figure 11. ML4662 EVAL Board

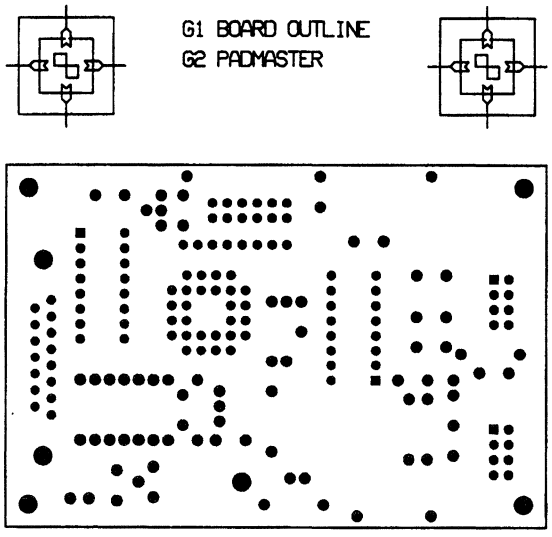


Figure 12.

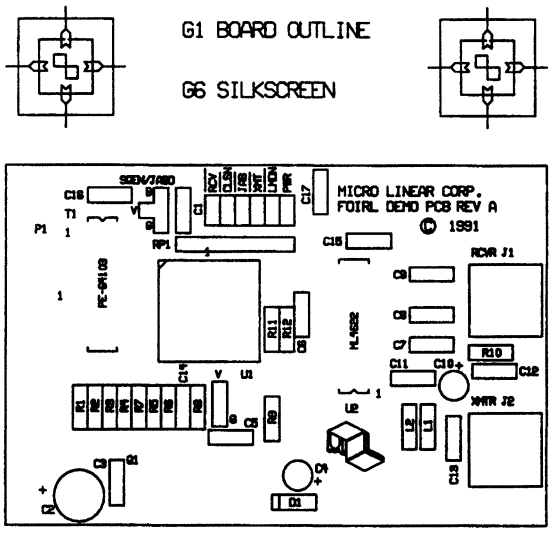


Figure 13.

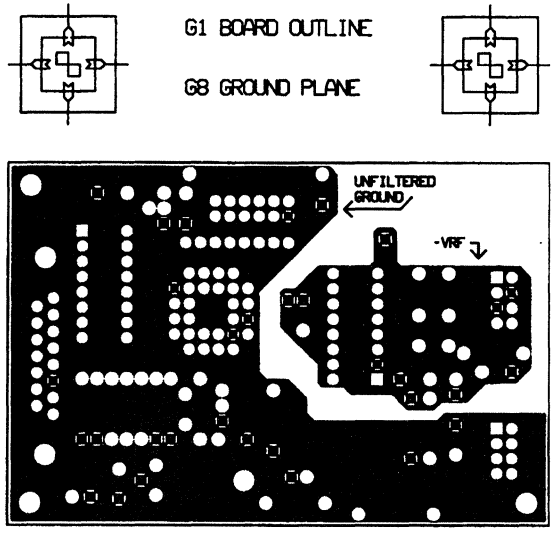


Figure 14.

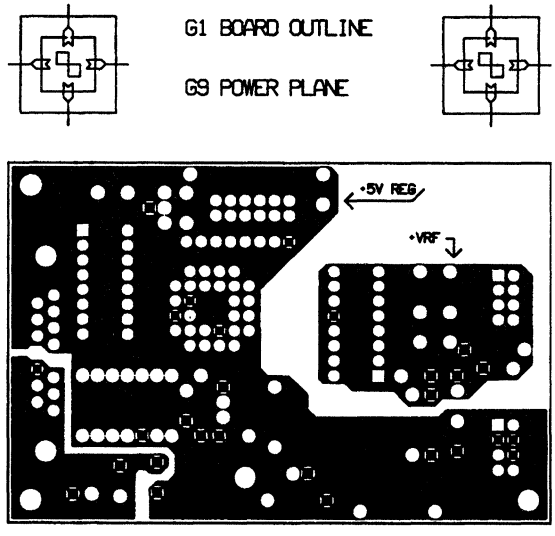


Figure 15.

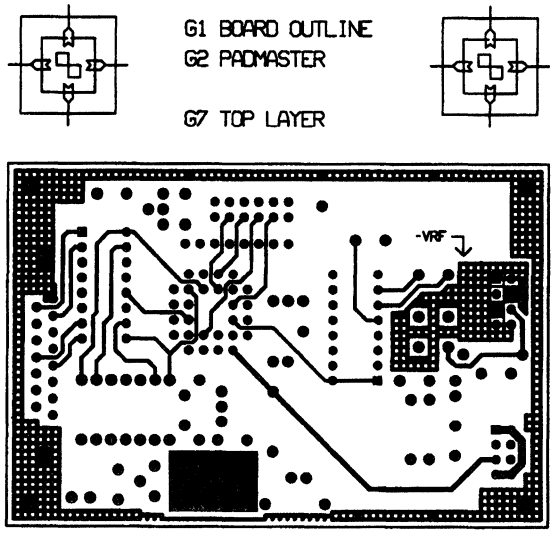


Figure 16.

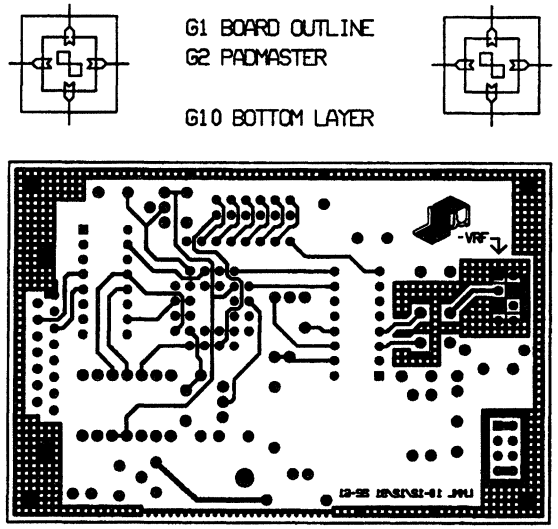


Figure 17.

Mehmet K. Nalbant
William Cho

Theory and Application of the ML4821 Average Current Mode PFC Controller

I. THEORY OF OPERATION

The ever increasing importance of power factor correction has prompted the design and availability of many power factor controller Integrated Circuits. Power factor correction requires special control circuits that are able to force the input current waveshape to be sinusoidal and in phase with the input sinusoidal voltage.

There are several ways that this can be accomplished. One method is the average current mode controlled boost topology power factor correction circuit, using the ML4821 dedicated average current mode controller IC. This paper is going to present enough theoretical background information along with practical examples to enable the design of such circuits.

Average current mode control can produce a high quality input sinusoidal current waveform. Although it can be used with many different power supply topologies, it excels when it is used with the continuous inductor current, boost topology.

Power Factor Correction

What is power factor? Enough has been said and written in the past couple years about this question. Therefore we are not going to elaborate on it. Instead we are going to look into how a power factor correction circuit operates.

Figure 1, shows the simplified block diagram of a power factor correction circuit. The circuit functions by monitoring the input full wave rectified line voltage as well as the output voltage. The two feedback signals are combined to set up the current trip points that shape the input current waveform to be sinusoidal and yet still regulate the output over line and load variations.

From now on we are going to use the acronym PFC instead of power factor controller.

Figure 2 shows the basic circuit diagram of a PFC with all necessary connections made. The heart of the circuit is the current modulator. The modulator consists of a linear multiplier, a current amplifier, and a PWM comparator. These three functional blocks enable the circuit to force the input current to be sinusoidal.

A current that is proportional to the input full wave rectified voltage is produced with the help of resistor RL. We will call this the **reference**. The reference is applied to one of the inputs of the multiplier. The other input of the multiplier is the output of the error amplifier. For the time being we are going to assume that the output of the error amplifier changes slowly compared to the line frequency. This is in general true since the bandwidth of this amplifier is set low by its feedback components.

The multiplier is a current input type. This enables the multiplier to have greater ground noise immunity. When there is a current at its input, its terminal voltage is a diode drop between 0.7V and 1V. In fact it is part of a current mirror. **Therefore a voltage source of low impedance should never be applied to this input.**

The output of the multiplier is current that is the product of the reference current and the output of the error amplifier that monitors the output voltage. This output current is applied to resistor Rc (see Figure 2). This voltage subtracts from the sensed voltage across Rs and is applied to the current error amplifier. Under closed loop control the current error amplifier will try to keep this voltage differential close to zero volts. This forces the voltage

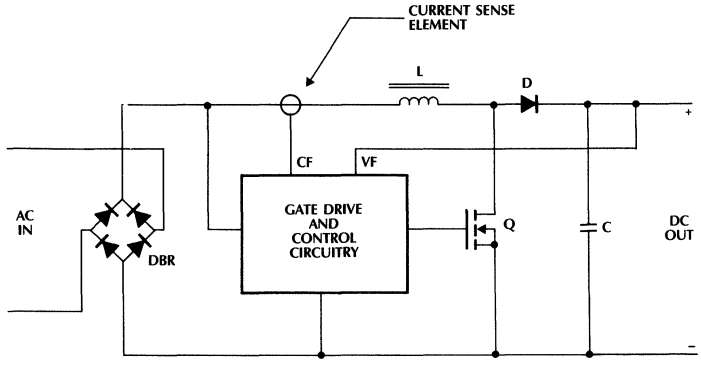


Figure 1. Top level block diagram of the power factor controller

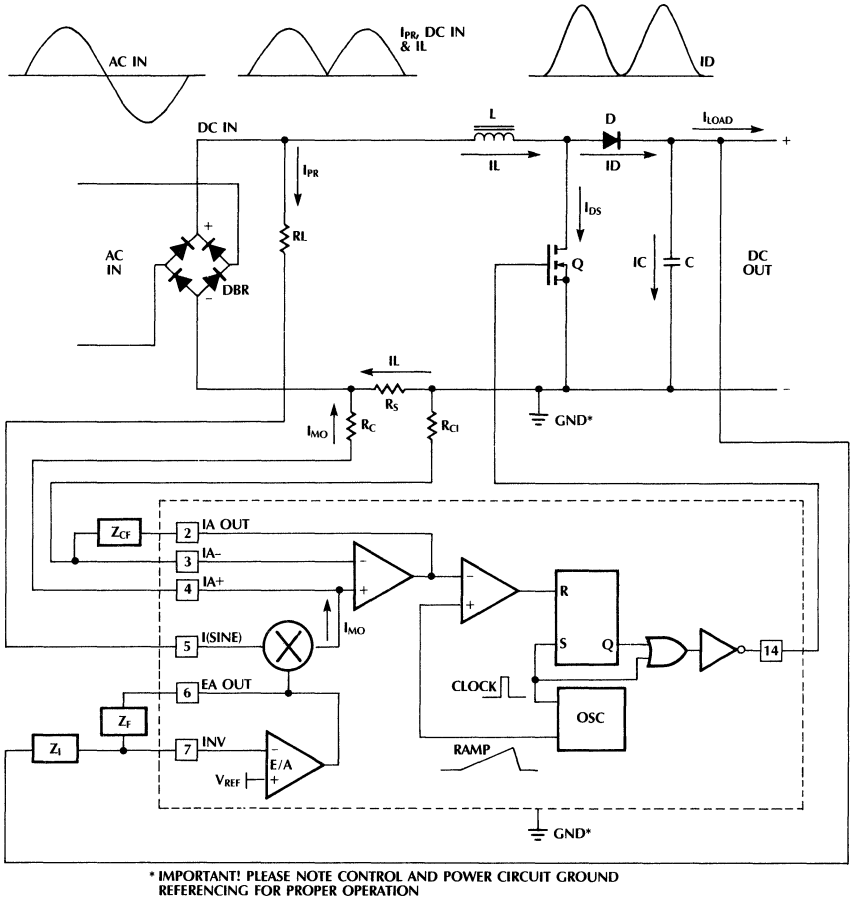


Figure 2. Basic PFC circuit

produced by the return current on Rs to be equal to the voltage across Rc. Since this requires dissipative sensing, Rs is a power resistor of very low value.

The amplified current error signal is then applied to the inverting input of the PWM comparator. The other input of the PWM comparator is the ramp generated by the timing capacitor of the oscillator. Pulse width modulation is obtained when the amplified error signal that sets up the trip point modulates up and down.

The rest of the circuit is very similar to conventional PWM control schemes. In this topology however, the loops operate around zero volts.

Multiple Loop Control

The PFC circuit is a multiple loop controlled circuit. There are two control loops, not counting the fault control loops such as peak current limit and overvoltage protection.

The first loop is the current loop that forces the input current to be sinusoidal. The second loop is the output voltage control loop that keeps the output voltage above the peak of the input voltage. The output voltage of a continuous inductor current boost regulator has to be set above the maximum peak of the input voltage in order to function correctly as a PFC. For a PFC that will operate to 260VAC the output voltage should be at least 370VDC at its minimum point.

To gain familiarity with the operation of the PFC it is necessary first to understand the waveforms and signals at the various critical points. Some of these waveforms are shown at the top of the schematic of Figure 2. By definition the average value of the input current follows a sinusoidal shape. That means also that the average value of the boost inductor L has to be sinusoidal. We say the average value because there is current ripple at the

switching frequency. 100KHz is a good trade-off point between inductor size and circuit efficiency. Switching losses in the circuit will include major losses in the MOSFET, output diode, and the inductor. Because the MOSFET is charged to the output voltage at every turn-off, switching losses will be significant at any input voltage and output current. The output diode must reverse recover high current with the full output voltage. Core losses in the inductor will not be as significant because the 100KHz AC ripple current is relatively low compared to the almost DC 120Hz rectified sinusoidal current.

For the purposes of this next analysis we are going to ignore the current ripple in the inductor. Lets also assume that somehow the MOSFET duty cycle is such that the inductor is forced to carry a current that has a full wave rectified sinusoidal waveshape. From the operation of the boost circuit there needs to be equilibrium throughout the entire 50Hz or 60Hz cycle. Large signal equations describing the operation of the boost circuit should hold.

$$V_{OUT} = \frac{V_{IN}}{1 - D_{ON}} \tag{1}$$

and

$$D_{ON} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{2}$$

Since $V_{IN} = v_{IN}(t) = \sqrt{2}V_{INRMS}|\sin(\omega t)|$ we get

$$D_{ON} = d_{ON}(t) = \frac{V_{OUT} - \sqrt{2}V_{INRMS}|\sin(\omega t)|}{V_{OUT}} \tag{3}$$

Also by definition

$$\hat{i}_l(t) = \sqrt{2}\frac{P_{OUT}}{V_{INRMS}}|\sin(\omega t)| \tag{4}$$

The MOSFET current is the inductor current chopped at high frequency with the above duty cycle. The diode current on the other hand is the inductor current chopped at high frequency with duty cycle $(1 - d_{ON(t)})$. By substituting we can get an expression for the average current that passes through diode D (i.e. ID = $i_d(t)$).

Note that the little hat on top of the variables denotes average value.

$$\hat{i}_d(t) = \hat{i}_L(t)(1 - d_{ON}(t)) \tag{5}$$

By substituting (3) and (4) into (5),

$$\hat{i}_d(t) = 2\frac{P_{OUT}}{V_{OUT}}\sin^2(\omega t) \Rightarrow$$
$$\Rightarrow \hat{i}_d(t) = \frac{P_{OUT}}{V_{OUT}} - \frac{P_{OUT}}{V_{OUT}}\cos(2\omega t) \tag{6}$$

As can be seen from the above equation the diode current consists of two parts. It has an average value consistent with the output power and output voltage (first term). Also it has an AC component with a peak value equal to that of the average value. The DC part of this current is simply the output load current. It flows through the output load. The AC part however flows through the output capacitor C. Consequently it may become a parameter when determining the value of this capacitor.

Now lets get back to the loops of the PFC. Earlier we mentioned that there are two control loops; an inner high bandwidth current loop and a much slower outer voltage loop. Figure 3 shows the two loops in block diagram form. First we are going to examine the two loops separately. Then we are going to see the criteria for proper connection.

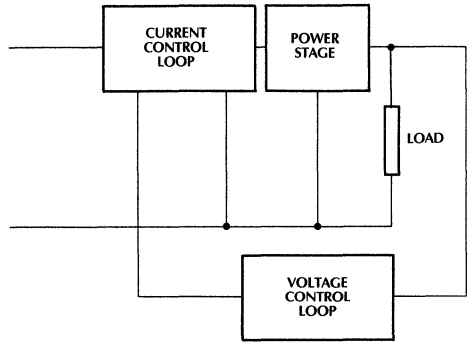


Figure 3. The two loops of a PFC. Inner current loop and outer voltage loop.

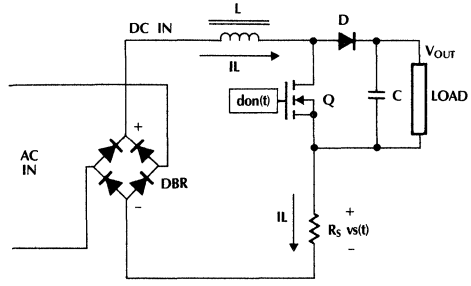


Figure 4. The power stage.

The Current Control Loop

The current control loop constitutes the inner loop and its job is to force the input current waveshape to follow the shape of the input voltage. It does this by modulating the duty cycle of the MOSFET in the power stage. The input voltage is a full wave rectified sinewave. Thus it is harmonically rich. The current control loop along with the power stage has to have enough bandwidth to follow this full wave rectified waveform. It can be shown that a bandwidth of a few KHz is sufficient. In order to proceed we need to derive expressions that give the responses of both the power stage and of the current loop.

As can be seen from Figure 4 the input of the power stage is the duty cycle output of the current pulse width modulator. Therefore we can describe the power stage as a functional block that has as its input the duty cycle information and as output the sensed voltage across the sense resistor Rs. The average current that flows through this resistor is equal to the average current that flows at the input of the PFC.

We can define

$$G_{PS}(s) = \frac{V_S(s)}{D_{ON}(s)} \tag{7}$$

as the gain of the power stage. The response can be found by assuming that the output voltage is constant and by using the state space averaging technique. The response shows a single pole roll off and is given by

$$I_L(s) = \frac{V_{OUT} D_{ON(s)}}{sL} \tag{8}$$

Since $V_S(s) = R_S I_L(s)$,

$$G_{PS}(s) = \frac{V_{OUT} R_S}{sL} \tag{9}$$

The above expression gives the small signal gain of the power circuit in the complex s-domain. It is the ratio of the sensed current waveform voltage to the incremental changes in the duty cycle. We can go one step further and incorporate in the above power stage gain the gain of the pulse width modulator. To do this we first have to find the gain of the modulator itself. For that we have to know the amplitude of the applied ramp to the noninverting input along with the allowable voltage swing range at its inverting input. The gain of the modulator is

$$G_{PWM} = \frac{\Delta D_{ON}}{\Delta V^-} \tag{10}$$

where ΔV^- is the voltage at the inverting input of the PWM comparator.

For the ML4821 the amplitude of the oscillator is 5.2V peak to peak. Therefore when the voltage at the (–) of the PWM comparator changes by 5.2V the duty cycle goes from zero to full duty cycle. If we assume that the deadtime is very small (normally around 5%) the gain of the PWM stage becomes

$$G_{PWM} = \frac{1}{5.5} \tag{11}$$

Now we can combine the gains of the power and PWM stages to get the following

$$G_{PST} = \frac{V_S(s)}{V^-(s)} = \frac{V_{OUT} R_S}{5.5sL} \tag{12}$$

Note that in actuality $V^-(s) = V_{IA\,OUT}(s)$. Therefore the overall current loop response will be determined by the responses of the current amplifier and the power stage. The overall response will be dictated by the required current loop bandwidth. For good waveform quality the total response should have a bandwidth of a few KHz.

Determination of the Current Loop Bandwidth

There is a theoretical upper limit for this bandwidth and is given by the following equation

$$f_{CLCO} = \frac{f_S}{6} \tag{13}$$

Thus for an operating frequency of 100KHz the maximum allowable current loop bandwidth is approximately 16KHz

The Gain Adjustor

Analysis of the voltage control loop shows that as the RMS AC input voltage goes up, the system gain increases by V_{RMS}. The gain increases with input voltage since the input voltage drives the one input to the multiplier. The second term is because the dI/dT on the inductor increases in proportion to the input voltage.

Since the gain varies with V_{RMS}, it then follows that the unity gain crossover frequency of the loop will change with a 1:8 ratio as the line changes from 90VAC to 260VAC. This complicates the loop design since the wide variation in crossover frequency would require the low line crossover frequency to be set very low while the high line crossover frequency would be set high.

The ML4821 cancels the square law dependency by adjusting the gain of the multiplier as a function of the RMS input voltage. The multiplier gain is equal to:

$$\frac{1}{kV}$$

Where k assumes one of two values in the active region (active region is the voltage range that appears on pin #8 that corresponds to the desired operating input voltage range). Voltage on pin #8 is a scaled down average of the rectified input AC voltage. Below we are going to see ways for designing an appropriate network that will accomplish this task.

Lets take a look at Figure 5. This curve shows the gain adjustor gain with respect to the voltage at pin #8. The curve has been separated in two parts. The right hand part is for operation under normal conditions in the voltage range from minimum line voltage to maximum line voltage (90VAC to 260VAC). 85VAC on the curve has been chosen to account for tolerances. Under normal operating conditions as input voltage decreases the gain increases compensating for the drop in the loop gain.

Under brownout conditions (below 85VAC) the gain decreases to limit the amount of current that is drawn from the line thus preventing an overload condition. This is a very useful feature since in many cases the load for a PFC is a constant power load. The input current has to go high to compensate for a drop in the input voltage.

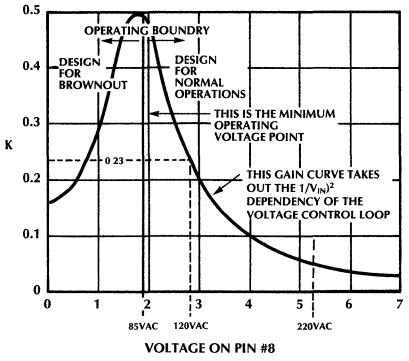


Figure 5. K-factor. Gain adjustor gain with respect to the voltage at pin #8.

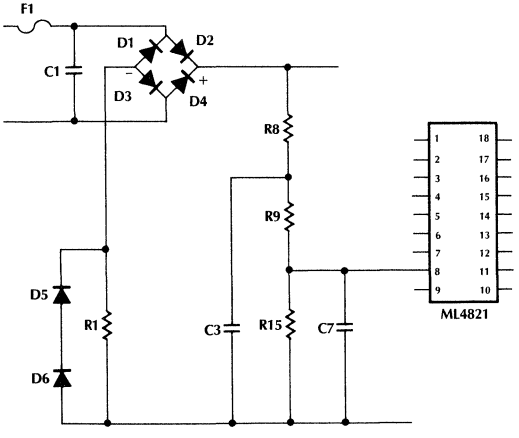


Figure 6. V_{RMS} sensing network.

Figure 6, shows the way pin #8 should be connected to the input line. The network consists of R8, C3, R9, R15 and C7 to form a two stage RC low pass filter and voltage divider. To calculate the values of the components, we must first select the minimum operating voltage point. Then we correspond this to the start of the brownout condition. From Figure 5, this is 85VAC which corresponds to approximately 2V at pin #8. On the same axis 2.8V corresponds to 120VAC. In other words when the input voltage is 120VAC the voltage at pin #8 must be 2.8V. Therefore the output voltage of the below filter/ divider network should be 2.8V.

The RMS value of the input sinewave is equal to the RMS value of the full wave rectified sinewave after the full bridge rectifier. The average value of the full wave rectified sinewave on the other hand is proportional to its RMS value and they are related as follows

$$V_{AVG} = \frac{2\sqrt{2}V_{INRMS}}{\pi} \qquad (14)$$

The average voltage at pin #8 is given by

$$V_{PIN\#8} = \frac{R15}{R8+R9+R15} V_{AVG} \qquad (15)$$

Assuming:
R8 = 910K
R9 = 91K
R15 can be found by equating the above equation to 2.8V and solving it.

This yields an R15 value of 27K. The values of C3 and C7 are chosen for good attenuation at 120Hz and minimum delay. Typical values are as follows

C3 = 0.1µF
C7 = 0.47µF

For most applications these values are good even though the values of the resistors may change to accommodate different brownout or operating conditions. The values are output power independent.

With the gain adjustor functional, the multiplier output current is given by

$$I_{MO} = K \times I_{SINE} \times (V_{EAOUT} - 0.8) \qquad (16)$$

where

I_{SINE} = reference current through pin #5.

K = gain adjustor gain (this quantity is dependent on the voltage present at pin #8). This is related to k from previous discussion. But is not equivalent.

$V_{EA\ OUT}$ = output voltage of the error amplifier.

The maximum value of the multiplier output current is limited by the value of the timing resistor and it is given by

$$I_{MO\,MAX} = \frac{2.5}{R_T} \qquad (17)$$

Typical value for R21 for 100KHz operation is 6.2K, in which case $I_{MO\ MAX}$ = 400µA.

It is a good idea to limit the maximum output current of the multiplier below the current limit point, but high enough to get maximum output power.

Output Capacitance

This a good point to talk about the output capacitance. The parameters that affect its choice are listed below

1. Hold-up time capability, usually 20msec for computer power supplies.
2. Ripple current handling capability.
3. Allowable third harmonic distortion.

The hold-up time capability is the amount of time at rated output power that will take the capacitor voltage to discharge to a minimum operating voltage. The start point of the dropout should be the minimum operating output voltage, for this type of PFC this is usually less than the nominal value of 380VDC.

$$C_{OUT} = \frac{2P_{OUT}t_{HLD}}{V_{OUT\,MIN}^2 - V_{OP\,MIN}^2} \quad (18)$$

where:

C_{OUT} = output capacitance.

P_{OUT} = output power.

t_{HLD} = hold-up time, normally 20msec.

$V_{OUT\,MIN}$ = minimum value of the output regulated voltage, normally happens at full load.

$V_{OP\,MIN}$ = minimum input voltage of the driven load, usually a switching power supply.

The chosen capacitor should be able to handle the ripple current that will flow through it. The peak value of this ripple current, as it was found earlier is equal to the output DC current. The RMS ripple current through the capacitor is

$$I_{COUT\,RMS} = \frac{I_{OUT\,DC}}{\sqrt{2}} \quad (19)$$

The third consideration in the determination of the output capacitor is the output ripple voltage which can be found using the following

$$\left|V_{OUT\,RIPPLE}\right|_{PEAK} = I_{OUT\,DC}\sqrt{\left(\frac{1}{4\pi f_L C_{OUT}}\right)^2 + ESR^2} \quad (20)$$

where:

f_L = line frequency.

ESR = ESR of the of the output capacitor.

Depending on the amount of the output capacitor the contribution of the ESR on the output ripple voltage may not be ignored.

The output ripple voltage will contribute to the third harmonic distortion of the input current. The actual amount will depend on the value of the output ripple voltage and the gain of the error amplifier at 120Hz.

The Voltage Control Loop

The inner current control loop can be modelled as a controlled current source. This simplifies the analysis of the voltage control loop.

Typical loads for a PFC are switching power supplies which are essentially constant power loads. These kinds of loads exhibit negative resistance at their input terminals. An increase in the input voltage causes a drop in the input current. It is therefore important that the voltage control loop error amplifier is correctly compensated. The two other types of loads are the constant resistance and the constant current.

Before we proceed with the design of the voltage control loop we have to analyze the loop to find out what parameters affect its dynamics. Earlier we mentioned that this loop has a very low bandwidth. If the bandwidth of this loop is high, excessive amount of the second harmonic component present at the output will be injected in the control loop causing third harmonic distortion of the input current.

Typical values for this loop are between 10Hz and 20Hz. To find the open loop voltage gain we have to calculate the change in the output voltage of the error amplifier that produces the required maximum output power change. This can be calculated by using the following expression

$$\Delta V_{EAOUT} = \frac{P_{IN} \times R_S \times R_L}{R_{MO} \times K \times V_{RMS}^2} \quad (21)$$

where:

P_{IN} = maximum input power.

R_S = current sense resistor.

R_L = input voltage sense resistor that connect to pin #5.

R_{MO} = resistor at the output of the multiplier.

K = gain adjustor gain at V_{RMS}, from the curve of Figure 5, K at 120VAC is 0.23.

V_{RMS} = input RMS voltage, this voltage is normally 120VAC.

Thus the open loop gain can be found to be

$$\left|G_{V.O.L.}\right|_{dB} = 20\log\frac{P_{IN}}{2\pi f C_{OUT} V_{OUT\,DC} \Delta V_{EAOUT}} \quad (22)$$

where:

G_{VOL} = open loop response for the voltage error amplifier.

The above expression gives the response of the magnitude with respect to frequency. The response has a –20dB/ decade slope and a constant phase lag of 90 degrees.

A suitable error amplifier configuration is shown in Figure 7.

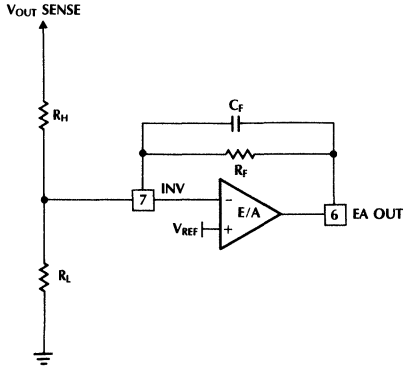


Figure 7. Error amplifier configuration.

Calculation of the output voltage sense resistors R_h and R_l: We have to pick a value for the output voltage under full load. The load regulation of the PFC can be expected to be 15 to 30V. Therefore if we pick a minimum output that is high under full load, there is the danger that under no load conditions the output voltage will be over 400V. Normally a minimum value of 370V will result at a high value of less than 400V. The reason for this seemingly poor regulation is the configuration of the error amplifier with a feedback resistor R_f that is close in value or less than R_h. Much better DC regulation can be obtained by using a blocking capacitor in series with R_f, but it will degrade the transient response of the circuit introducing a bounciness to the input current under transient conditions.

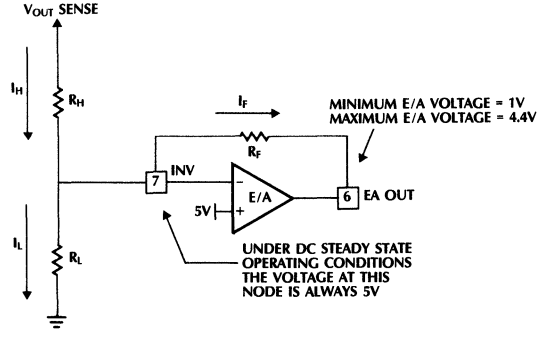


Figure 8. DC part of the feedback circuit. It is used for sense component calculations

The output voltage of the error amplifier should be designed for 4 to 5 volts maximum at full load. Higher voltage gives better noise immunity and dynamic range. However that means the output voltage will have a larger variation due to its influence on the output voltage dividers. A good place to start is 4.4V. A value for R_h is picked that is normally between 680KΩ and 1MΩ. In this case we are going to pick 825KΩ. The value of the feedback resistor is found based on the loop design criteria. With these two values and minimum output voltage defined, R_l can be calculated using the following formula.

$$R_l = \frac{5R_hR_f}{R_f(V_{OUT\,MIN} - 5) - 0.6R_h} \qquad (23)$$

See Figure 8 for definitions of the parts.

With the above chosen and calculated values one now can calculate the maximum output voltage under no load conditions as follows

$$V_{OUT\,MAX} = R_h\left(\frac{4.3}{R_f} + \frac{5}{R_l}\right) + 5 \qquad (24)$$

Calculation of the OVP components: The sense resistors for the OVP circuit are easier to calculate. The voltage at which point the OVP circuit will act is being determined in part by the maximum tolerable voltage at the output before damage due to overvoltage that can occur. A good rule of thumb which may not be applicable in all cases is to set a voltage that is 10 to 15V higher than $V_{OUT\,MAX}$ as calculated by the above expression. Therefore $V_{OVP} = V_{OUT\,MAX} + 10V$.

OVP protection is facilitated by connecting a voltage divider to pin #11. The high side of this divider is connected to the output terminals of the PFC and the low side to ground. For the time being we are going to call these two resistors R_{OVPh} and R_{OVPl}. We are going to assume a value for the high side resistor and calculate the value of the low side. For that purpose one can use the following formula

$$R_{OVPl} = \frac{5R_{OVPh}}{V_{OVP} - 5} \qquad (25)$$

The OVP pin on ML4821 is a multifunction pin. Pin #11 is also used for remote shutdown. When this pin is pulled to ground the IC shuts down. The pin can be pulled to ground using a small signal FET or bipolar transistor such as the 2N2222. Due to this multifunctionality, the pin should be biased higher than 1.0V whenever the part needs to be operated without the input power applied. ***Extreme care should be exercised however when input power is applied.*** It should be made sure that the voltage on this pin reflects the correct divided down output voltage for safe operation.

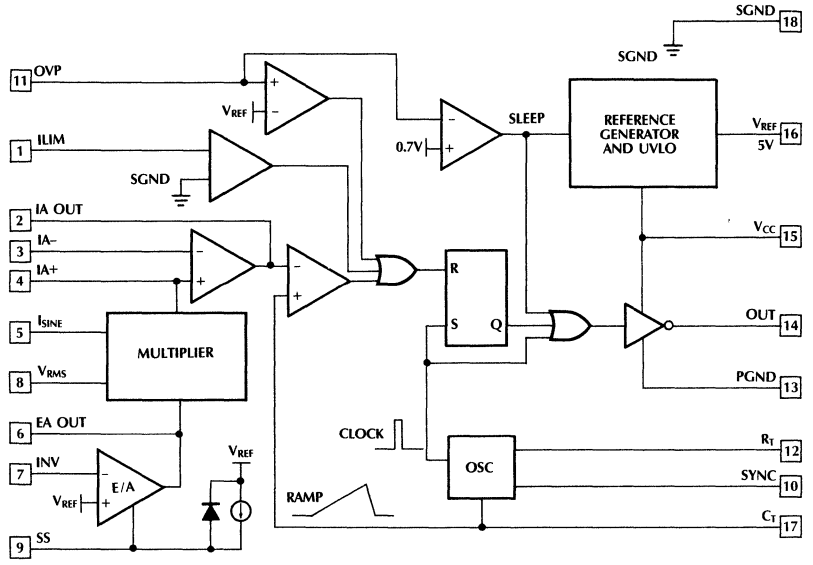


Figure 9. Block diagram of the ML4821

Block Diagram of the ML4821

Figure 9, shows the block diagram of the ML4821. So far we have covered most of the functions of this IC. But there are additional functions to extend its usefulness in various applications.

One of them is the SYNC function that enables the IC to frequency lock to an external oscillator. Pin #10 is reserved for this function. A positive pulse on this pin of 2V or higher resets the oscillator's comparator and initiates a discharge cycle for the timing capacitor connected to pin #17. For proper operation however the ML4821 oscillator should be set to operate at a frequency that is roughly 10-15% lower than that of the external driving source.

The rectangular block labeled multiplier combines both the multiplier function and the gain adjustor functions that we mentioned earlier.

Another useful function is the Soft Start function. This may be a useful function in some applications where controlled output voltage rise is desired. To use this function effectively however it is necessary to have an auxiliary bias power supply able to supply and maintain power to the control circuitry while the output voltage of the PFC is rising up slowly. The amount of the Soft Start capacitance required is a function of the delay in the output voltage rise time and the internal charging current.

The undervoltage lockout function of the IC can be used for off-line start-up as shown in Figure 10.

The Boost Inductor

One of the key components in the PFC is the boost inductor. The value of this inductor affects many other design parameters. Most of the current that flows through this inductor is at low frequency (assuming low percentage ripple). This is particularly true at the lowest input voltage where the input current is highest.

Normally the acceptable level of ripple current is between 10 and 20%. For operation at 100KHz the following formula will produce acceptable results

$$L = \frac{300}{P_{OUT}} mH \qquad (26)$$

The peak to peak ripple current for any input output voltage combination can be found by using the following formula

$$\Delta I_{L_{P-P}} = \frac{V_{IN}(V_{OUT\,DC} - V_{IN})}{f L V_{OUT\,DC}} \qquad (27)$$

where:

V_{IN} = peak value of the input full wave rectified waveform.

f = operating frequency.

For an output voltage of 380V the maximum peak to peak ripple happens when the input voltage is 134VAC and its value can be calculated using

$$\Delta I_{L_{P-P\,MAX}} = \frac{V_{OUT\,DC}}{4fL} \qquad (28)$$

This ripple current which has a triangular shape will produce a ripple voltage at the switching frequency and its harmonics on the input impedance.

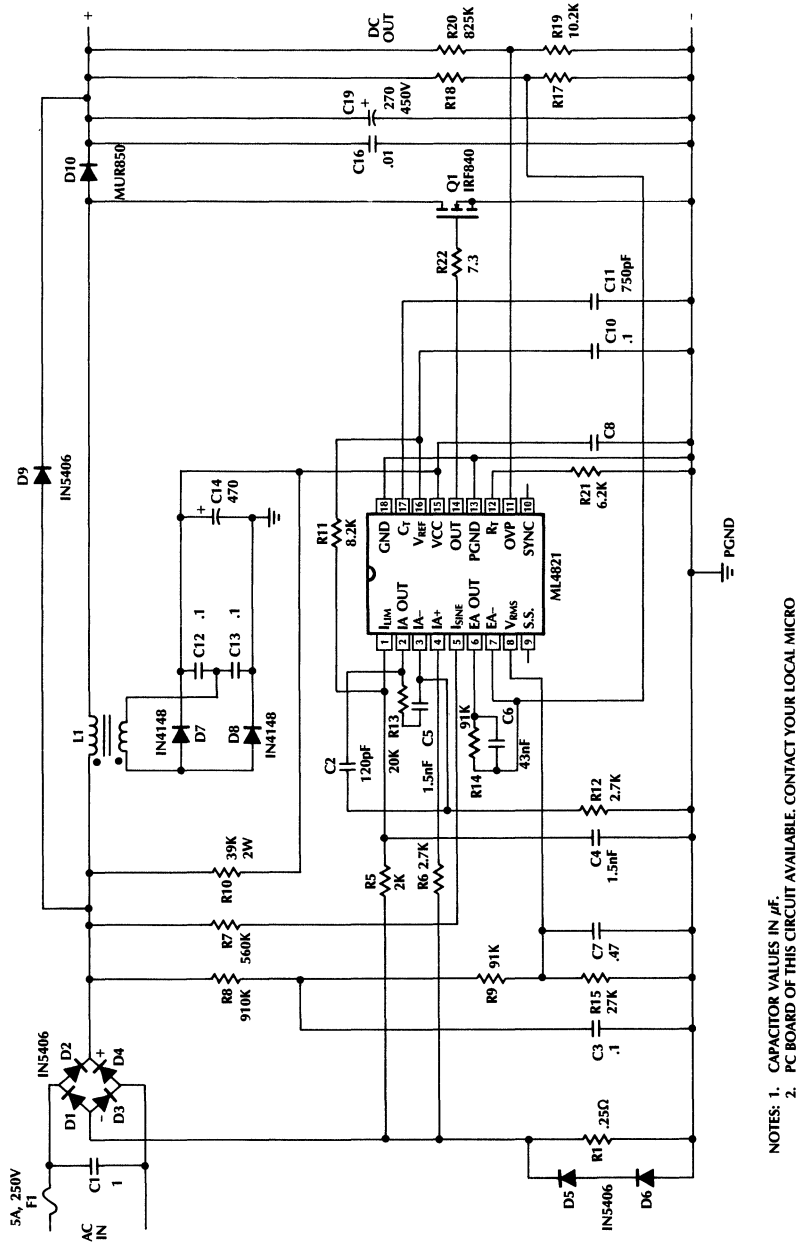


Figure 10. Schematic diagram of the 200W PFC

The Input High Frequency Bypass Capacitor

This capacitor which should normally be at the line side of the input bridge rectifier helps to bypass the high frequency ripple current. Its impedance is few Ohms at the switching frequency. Therefore there is a need for additional filtering at the input, if differential conducted noise specifications are to be met. Note that this capacitor has to be an approved across the line type (an X-type capacitor).

II. DESIGN OF A 200W, 100KHz PFC

The complete schematic diagram of a 200W PFC is shown in Figure 10. We are going to cover in detail the pin by pin design of this PFC. We will use the formulas and the procedures presented in the previous sections. Although the design is at 200W it can easily be extended for power levels above that.

We are going to start the design by choosing the main components such as the boost inductor L1 and output capacitance.

The Boost Inductor: We can use (26) for the calculation of the inductor value

$$L = \frac{300}{200}\text{mH} = 1.5\text{mH} \qquad (29)$$

The maximum peak current that this inductor will see is simply the peak of the input sinusoid plus 1/2 the ripple current due to the switching action at 85VAC. Assuming 90% efficiency the input power will be 222W. This results in an input RMS current of approximately 2.6Arms with corresponding peak value of 3.7A. The peak to peak ripple current at 85VAC is 540mA. Therefore the peak inductor current will be 4.0A. The choice for the core material should be such that the inductance value will not change when this current passes through the winding.

It is important to remember that the higher the inductance, the lower the ripple current, which in turn means less filtering required on the input line to meet line conducted noise requirements. It also means lower core losses. The cost is more number of turns.

Good candidates for core materials are:

Powder Iron Cores

Mollypermalloy Cores

Gapped Ferrite Cores, provided that the gap is not excessive.

Normally for any reasonable core material, core loss is not an issue due to the large number of turns required for such an inductor. The critical parameter is the change in their permeability under high current excitation, and a large number of turns. Therefore a careful analysis should be made to determine suitability of a core material for the given application.

For the present application we are going to choose a powder iron core of toroidal form. The core material is from Micrometals Inc., and the part number is T184-40 and it will contain 102 Turns. The inductor will maintain approximately 80% of its zero current inductance at 4.0A. Therefore the inductance value will drop to 1.2mH at 4.0A. This will be the value that should be used to recalculate the peak to peak ripple current when time comes to design an input filter for the PFC. Also because the ripple current will increase, the current limit point should be set higher to account for this variation.

The Output Storage Capacitor: At an earlier section we mentioned the criteria for the selection of this capacitor. Lets assume that we need a hold-up time of 20msec and the output voltage is allowed to drop from 370V to 330V before regulation is lost in the driven switching power supply. We can use (18) to calculate a capacitance value

$$C_{OUT} = \frac{2\times(200\text{W})\times(20\text{msec})}{(370\text{V})^2-(330\text{V})^2} = 285\mu\text{F} \qquad (30)$$

The rated voltage of this capacitor should be at least 450V. The closest standard value offered by UNITED CHEMI-CON is 270µF type SMG with a voltage rating of 450V (a 330µF can also be used). Note that two capacitors of lower voltage rating can also be connected in series (i.e., 250V) provided that shunt ballasting resistors are also used.

The Output Diode: The output diode (D10) should be an ultra fast type capable of supporting the peak input current for a couple of milliseconds. Power dissipation is the limiting factor. For this design an MUR850 was chosen. Note that various manufacturers may be working on diodes with better reverse recovery characteristics.

Surge Bypass Diode: This diode labeled D9 on Figure 10 helps to bypass surges at the input line during start-up. This prevents possible saturation of inductor L1.

Output Circuit Very High Frequency Bypass: Capacitor C16 serves this purpose. It is used to control the output dI/dT loop. It can be a high voltage high frequency ceramic type of 0.01µF.

Oscillator Circuit: Pins #12 and 17.

Timing resistor (R21): The choice for this resistor sets both the charging current for the timing capacitor, and some other internal currents. One of them is the maximum multiplier current (see formula 17). For a PFC operating at 100KHz a typical value for this resistor is 6.2K.

Timing capacitor (C11): For details on how to calculate its value refer to data sheet. For this application its value is 720pF.

Gate Drive: Pin# 14

The gate driver of the IC can directly drive power MOSFETs, normally a series resistor is used to damp any oscillations that may arise due to parasitic trace inductances and the gate capacitance. Its value should be chosen such that it will not result in excessive switching losses. If two paralleled MOSFETs are driven then their gates should be decoupled using two individual gate resistors.

For this example a gate resistor of 10Ω was used.

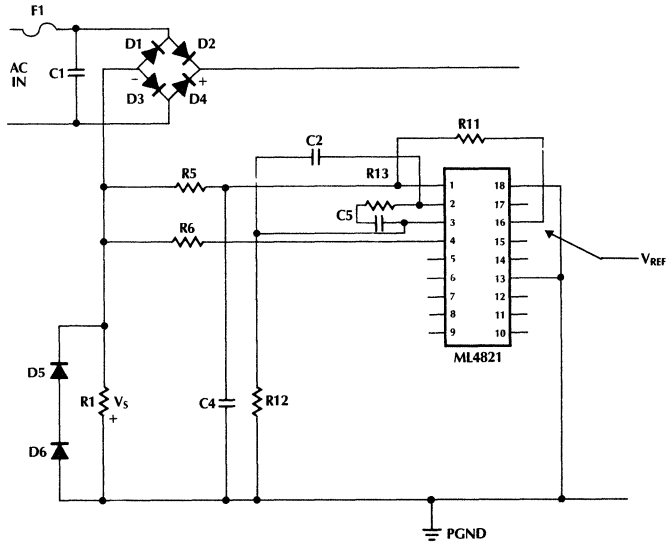


Figure 11. Current limit and current sense circuit connections

Depending on the layout a Scholtky diode may be necessary across the gate drive to ground due to substrate current injection which can produce unpredictable behavior. The cathode should be connected to pin #14 and anode to ground. It should be placed as close to the IC as possible. Substrate current injection occurs when an output pin is forced more than about 0.5V below ground.

Power and Signal Grounds: Pins #13 and 18

These two grounds should go to ground plane and they should be connected together with the shortest possible trace length.

V_{REF}: Pin #16

The V_{REF} pin of the IC should be decoupled very well with a high quality ceramic capacitor. A typical value is 1µF. For higher power levels (P_{OUT} > 500W) additional capacitance may be required for proper operation.

Overvoltage Protection: Pin #11

This protects against accidental increases of the output voltage. As soon as a voltage higher than the set limit is detected the IC stops sending pulses to the MOSFET, until the voltage has dropped to safe limits. In a boost regulator if the voltage loop ceases to operate the only way to limit the output voltage from rising to destructive levels is the overvoltage protection circuit.

Also due to the low bandwidth of the voltage control loop there may be situations that the voltage may rise to destructive levels such as sudden removal of the output load. Under those conditions the OVP circuit will activate preventing further rise.

Formula (25) is used to set the activation limit of the OVP circuit.

From Figure 10, assuming the value of R20 = 825K, R19 can be found as follows

$$R19 = \frac{5 \times (825 \times 10^3)}{400 - 5} = 10.2K \qquad (31)$$

V_{CC}: Pin #15

This is the supply pin of the IC. Normally a quality ceramic capacitor should be connected to this pin as close as possible to the body of the IC for effective decoupling. For low power applications (< 500W) 1µF may be sufficient, but for higher power applications experience shows that two individual capacitors could be necessary.

In order to facilitate off-line start-up the IC has a large Under Voltage Lockout hysteresis. For bootstrapped operation a reservoir capacitor (C14) is charged with a small current through R10 which is connected to the input high voltage line. When the voltage on this capacitor reaches 16V the IC "wakes-up". A winding on L1 (see Figure 10) "steals" part of the energy to supply the current requirements of the IC. This way the circuit continues to operate.

The time that it takes initially for the voltage to reach 16V, and therefore for the circuit to start, is a function of the resistor R10. This is a power resistor and for as long as power is applied it wastes power, usually about 2W.

The value of C14 is being determined by the current requirements of the circuit. C14 has to be sufficiently large for the circuit to bootstrap. However it should not be too large because it will take a long time initially to charge it to 16V, and turn on the IC.

Current Limit: Pin #1

As in every switching regulator, there is a need for current limit in the PFC as well. To understand its operation better, lets look at Figure 11.

The current limit point is set by R11 and R5. The value of R5 can be selected first. Then the value of R11 is calculated using the following. In this case R5 = 2.0K. Assuming a current limit voltage of 1.2V across the sense resistor.

$$R11 = \frac{V_{REF}}{V_S} R5 = \frac{V_{REF}}{I_{IN} R1} R5 \qquad (32)$$

where:

I_{IN} = current at which limiting action should start.

$R1$ = sense resistor.

$$R11 = \frac{5}{1.2}(2.0K) = 8.2K$$

For proper operation, the sense voltage across R1 that triggers the current limiting action should be greater than the sense voltage produced at low line and full load. In this case current limiting action starts when the sense voltage is 1.2V. Therefore at full load and at low line the sense voltage should be less than 1.2V. A 15% less voltage corresponds to 1.0V.

Current Sense Circuit: Pins #3 and 4.

These two pins are used to sense the return current of the power circuit. The average value of this current is forced to follow the sinewave shape as being determined by the IC. Pin #4 is at the same time connected to the output of the multiplier. As you recall the maximum value of the multiplier output current was set to be 400µA by the timing resistor R21.

In the current limit section we said that at maximum power and low line the sense voltage should be 1.0V. Therefore R6 should be chosen such that it will produce 1.0V at 400µA.

$$R6 = \frac{1.0V}{400\mu A} \cong 2.7K \qquad (33)$$

Earlier we calculated that the expected maximum peak current is 4.0A. Using this value R1 can now be calculated

$$R1 = \frac{1.0V}{4.0A} \cong 0.25\Omega \qquad (34)$$

The value of R12 which is a feedback resistor for the current amplifier is chosen to be equal to R6. This is set to cancel out the input bias current of the current amplifier. Hence R12 = 2.7K.

Design of the Current Loop Amplifier Components: Pins #2, 3, and 4.

The design of the current loop is one of the most critical tasks in the overall design. To do that we have to have knowledge of the open loop response of the power stage. Equation (12) gives this response which is plotted in Figure 12.

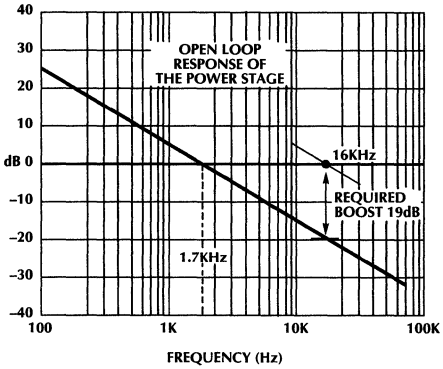


Figure 12. Open loop response of the power stage, and required boost for 16KHz loop crossover.

The required gain boost for unity gain crossover at 16KHz, as set by (13), can be calculated by using (12).

$$\frac{380 \times 0.24}{2 \times \pi \times 5.5 \times (16KHz) \times (1.5mH)} = 0.11 \text{ or } -19dB \qquad (35)$$

An appropriate current amplifier response that will accomplish this is shown in Figure 13. The equations that give the asymptotic gain response in each one of the three regions are given below.

$$[1] \ldots\ldots\ldots |G|_{dB} = 20\log\frac{1}{2\pi f R12 C5} \qquad (36)$$

$$[2] \ldots\ldots\ldots |G|_{dB} = 20\log\frac{R13}{R12} \qquad (37)$$

$$[3] \ldots\ldots\ldots |G|_{dB} = 20\log\frac{1}{2\pi f R12 C2} \qquad (38)$$

In order to complete the design of the current control loop, we have to calculate the feedback component values. Using (37) the value of R13 is found as

$$20\log\frac{R13}{R12} = 19dB \Rightarrow R13 \cong 20K \qquad (39)$$

$$C5 = \frac{1}{2 \times \pi \times f \times R12 \times 10^{\frac{19}{20}}} \Rightarrow C5 \cong 2.3nF \qquad (40)$$

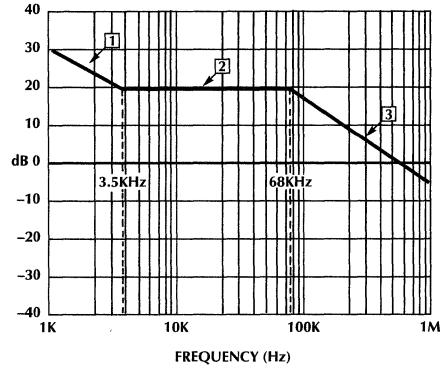


Figure 13. Desired current error amplifier response.

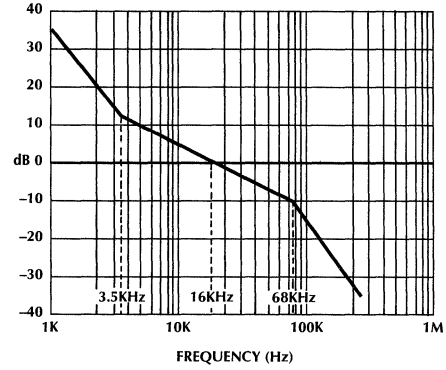


Figure 14. Overall closed current loop response.

where:

f = 3.5KHz

$R12$ = 2.7K

Gain boost = 19dB

$$C2 = \frac{1}{2\times\pi\times f\times R12\times 10^{\frac{19}{20}}} \Rightarrow C2 \cong 120\text{pF} \qquad (41)$$

where:

f = 68KHz

With the values of the feedback components now calculated we can plot the overall closed loop response of the inner current loop. Keep in mind that logarithmic slopes and gain values just need to be added to get the overall response. The result is shown in Figure 14.

Calculation of R7, the I_{SINE} Resistor: Pin# 5.

In a previous calculation we have assumed that the maximum voltage of the error amplifier is 4.4V. The minimum voltage under normal operating conditions is about 0.8V. That necessitates a change in the output voltage of the error amplifier of 3.6V from no load to full load. Note that due to feedforward compensation the output of the error amplifier will not change for line variations. It is important also to note that the amplifier output is capable of going to 7.5V.

Equation (21) can be solved for R7.

$$R7 = \frac{\Delta V_{EAOUT}\times K\times V_{RMS}^2\times R6}{R1\times P_{IN}} \qquad (42)$$

Substituting the known values in the above we get

$$R7 = \frac{3.7\times 0.23\times 120^2\times 2200}{210\times 0.24} = 535\text{K} \qquad (43)$$

The nearest standard value for R7 is 560K. With this resistor value, the I_{SINE} current should be calculated to check the input current range corresponding to the line input voltage range. The multiplier requires that the Isine current be less than 500µA as suggested in Fig 8 of the data sheet.

Design of the Voltage Loop Amplifier Components: Pins #6 and 7.

Equation (22) gives the magnitude of the open loop gain. The response has a –20dB/decade slope with constant 90 degree phase lag. To proceed with the design of the error amplifier feedback components we have to pick the unity gain crossover frequency. In this application we are going to crossover the 0dB line at 10Hz.

The frequency where the open loop response crosses over the 0dB (unity gain) line can be found by solving (22) for f.

Figure 15, shows the open loop along with desired amplifier responses.

$$f = \frac{P_{IN}}{2\pi C_{OUT} V_{OUT\,DC}\ \Delta V_{EAOUT}} \qquad (44)$$

$$f = \frac{210}{2\times\pi\times 270\times 10^{-6}\times 380\times 3.7} = 88\text{Hz} \qquad (45)$$

Now we can complete the design of the error amplifier feedback components. For unity gain crossover at 10Hz the amplifier needs to have an attenuation of 19dB at 10Hz.

$$20\log\frac{R14}{R18} = -19\text{dB} \Rightarrow R14 = 92\text{K} \qquad (46)$$

Then we calculate the value of C6. For that we look up the asymptotic break point of the response curve, which in this case is 40Hz.

$$C6 = \frac{1}{2\pi f R14} = \frac{1}{2\times\pi\times 40\times(92\text{K})} = 43\text{nF} \qquad (47)$$

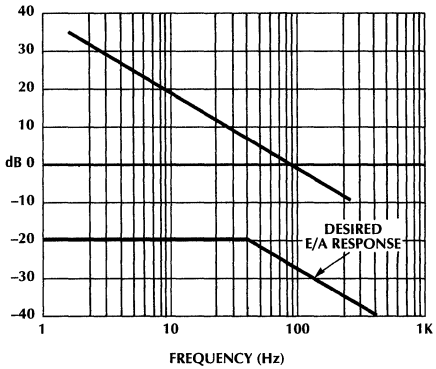


Figure 15. Open loop and desired error amplifier response.

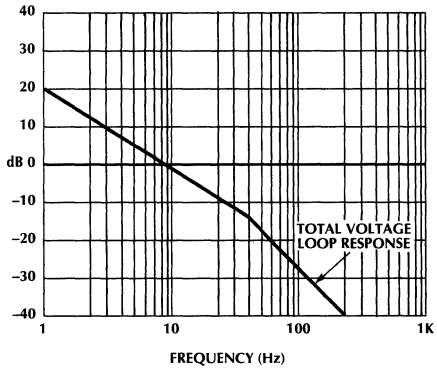


Figure 16. Total voltage closed loop response.

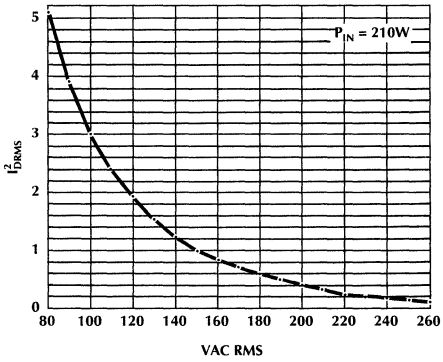


Figure 17. Square RMS drain current versus input RMS voltage.

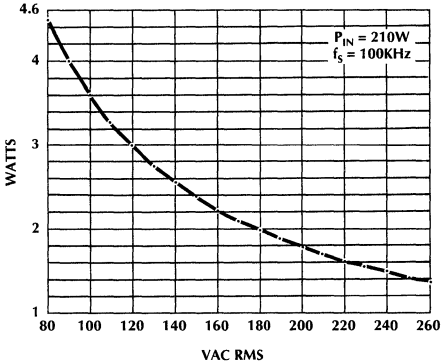


Figure 18. Switching power loss for a 200W PFC operating at 100KHz versus the input voltage.

Figure 16, shows the overall closed voltage loop response.

Voltage sense resistor calculation:

R18 was already assumed to be 825K. R17 can be calculated using (23).

$$R17 = \frac{5\times(825\text{K})\times(91\text{K})}{91\text{K}(370-5)-0.6(825\text{K})} = 10.38\text{K} \qquad (48)$$

Losses In The Power MOSFET Q1:

There are three kind of losses in the power MOSFET, these are listed below:

1. Conduction Losses, due to the conduction of the drain current.
2. Capacitive Losses, due to the charge and discharge of the total drain source capacitance. This is a switching loss.
3. Turn-On and Turn-Off Losses, these are also switching losses.

The conduction losses can be calculated by using (49). Equation (49) gives the RMS value of the drain current which can be used to calculate the conduction losses. As can be expected it is a function of the input power and input and output voltages.

$$I_{DRMS} = \frac{2P_{IN}}{V_{INRMS}}\sqrt{\frac{1}{4}-\frac{2\sqrt{2}V_{INRMS}}{3\pi V_{OUT}}} \qquad (49)$$

The assumption made in the derivation of the above is that the ripple to average current ratio is very small which is normally true for this kind of PFC. It happens in the low input voltage range. In reality the nonzero ripple will increase the value of the calculated RMS current by a small amount.

Figure 17 gives the value of the square of the RMS drain current with respect to the input RMS voltage. One can use this graph to calculate the power loss due to conduction in the MOSFET. This is simply

$$P_{CMOSFET} = I^2_{DRMS} \times R_{D-SON} \qquad (50)$$

For our design example the minimum line was 85VAC. Using the graph above that corresponds to a value of 4.5. Using an IRF840 type MOSFET and assuming that its ON resistance at the operating temperature will be 50% higher than its 25°C resistance, the conduction power loss will be 5.4W. At 120VAC the power loss will be 2.2W, and at 220VAC will be 0.34W! As you can see it is quite difficult to have an optimum circuit at the same time with wide input voltage range. For specific applications where the input voltage range is narrow it is more advantageous to have the output voltage closer to the maximum peak of the input voltage.

Lets give an example with respect to the last statement made in the paragraph above. Lets assume that the power level is still the same but that the operating voltage range is 85VAC to 135VAC and that the output voltage is 200VDC. With these operating parameters (50) yields a value of 2.99, which corresponds to power loss of 3.6W, Compare this to 5.4W in the above example.

Normally efficiency measurements are made at nominal operating voltages i.e., 120VAC. However the PFC should be able to function without failure at low line conditions. That necessitates careful selection of components and thermal design for good reliability.

Capacitive losses in the MOSFET are due to discharge of the total drain source capacitance. We use the term total because the drain gate capacitance contributes to this loss too. The losses can be calculated using (51).

If we assume a total capacitance of 350pF then (51) yields 2.5W.

$$P_{CAP\,D-S} = \frac{1}{2} C_{D-S} V_{OUT}^2 f_S \qquad (51)$$

The calculation of switching losses are a little more difficult since they are a function of many things such as gate drive conditions that may include the physical layout. In any case an equation that can be used to give some indication of these losses is given below:

$$P_{SWITCHING} = \frac{2\sqrt{2} V_{OUT} f_S P_{IN} t_{TR}}{\pi V_{INRMS}} \qquad (52)$$

where:

t_{TR} = transition time

f_S = switching frequency (= 100KHz in this case).

Assuming waveform symmetry during both turn-on and turn off transitions and ignoring possible secondary effects we can use (52) to calculate the switching losses. Our example was designed at 120VAC and 210W input with a reasonable value for the transition time of 50nsec. The resulting losses are approximately 3W.

As a final step lets add up all the losses in the MOSFET for 120VAC. The resulting total loss is 7.7W. If this yields an unacceptable efficiency, an optimized MOSFET switch should be used. Loss calculations can be made using the three equations. Note that the derivation of these equations is rather long and tedious requiring careful modelling.

III. EVALUATING A PFC CIRCUIT

This part of the application note will give practical information that may be useful when trying to get the bread board up and running to meet required specifications. It will show that measuring power factor, harmonic current content, and efficiency may impose new challenges to even experienced power supply design engineers. Also it will contain some performance data that may serve as a reference point.

Waveforms

Operating waveforms are shown in the following figures. They are taken with output at 200W and input at 120VAC. Figure 19 shows the power factor corrected input current waveform. Upper waveform is current at 1A per division. Voltage and current are in phase and identical. Figure 20 shows the inductor waveform. The shaded portion of the upper waveform indicates the ripple current riding on top of a rectified sinusoidal current. The lower waveform is an expanded view of the upper waveform. Figure 21 shows the current limit waveform on pin 1. As the input current increases, the valleys of this waveform approach zero volts. However, because the multiplier current is limited to 400µA, the current waveform will sag before the current reaches the current limit level. Current limit level is reached during a transient condition when the inductor current increases rapidly before the voltage loop can compensate for it. Figure 22 shows the output of the current amplifier (pin #4). It sets up the trip points of the PWM comparator.

REMINDER: The OVP pin requires at least 0.7V for the chip to begin operation.

Layout

Board layout is critical in this application as it is in any power control circuits. One must pay close attention to the high current circulating paths. The control circuitry and it associated ground plane should be away from the high current power paths as much as possible. Current should be steered away from the high impedance nodes such as the input to both error amplifiers as well as to both current limit and OVP comparators. Also magnetic fields generated by the magnetics components as well the switching power components can inject noise into the high impedance nodes such as that to the current limit comparator. The heat sink should either be grounded or at least AC coupled to ground by a high frequency ceramic capacitor and kept as far away from the IC as possible.

Power Factor

Input power factor, harmonic current content, and waveshape are all used when describing the performance of a power factor circuit. It is important to keep in mind that regulatory specifications such as the IEC555 for Europe will require that just the harmonic current levels meet certain limits. The proposal currently sets these limits (for Class D) as a function of power level up to 300W. Above 300W, the limits are absolute. Thus even a low power factor number at high input line voltage can easily meet the limits since the input current level is

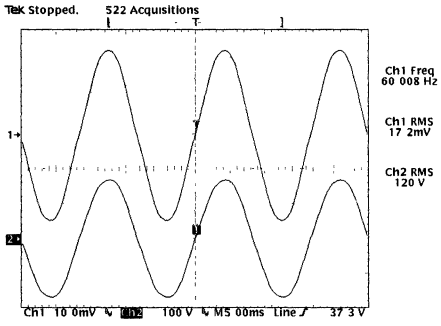


Figure 19. Input current and waveform.

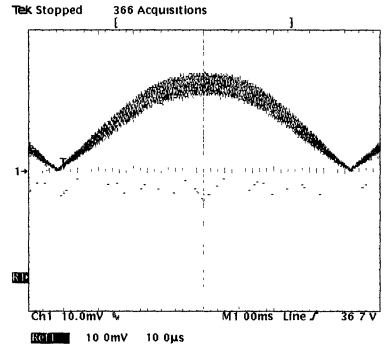


Figure 20. Inductor current magnified 1K times.

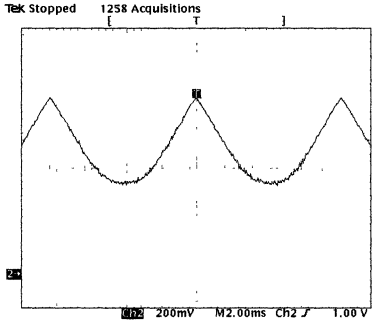


Figure 21. Current limit comparator.

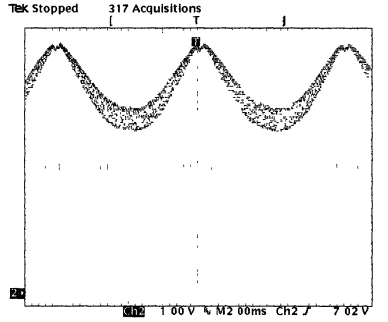


Figure 22. Current amp output.

proportionally low. Nevertheless power factor is a good parameter for measuring the capabilities of a power factor circuit.

To measure power factor, one must have a very reliable power meter that accurately measures both apparent power (product of RMS voltage and RMS current) and true average power. Some of the older model meters measure power factor by determining the phase angle between current and voltage waveform. Obviously this will not work for our purposes.

True average power for distorted AC waveforms can only be determined when the current and voltage are simultaneously sampled which is then multiplied and integrated. There are several meters on the market that are possible candidates for this purpose. But none that we have looked at seem to do the job as well as the one offered by Voltech. The Voltech PM1000 measures true power by sampling the waveform and analyzing the analog signal using digital methods. It uses DSP to filter, multiply, and integrate both voltage and current simultaneously.

A study was done by comparing the results of a power factor measurement with the Voltech to that of another well known meter manufacturer who perform the multiplication and integration of the power signal VIA analog methods. Both meters gave nearly identical measurements when evaluated against a calibrated standard reference unit. However when the units were set up in the lab to measure power factor of an actual switching power circuit, only the Voltech gave the expected measurement readings. For whatever the reason the analog meter gave grossly false readings. Noise in the switching circuit is prime suspect. This does not suggest that meters with analog circuits can not be designed to reject noise and work effectively whatever the waveshape and environment. But one should be very careful about which meters are trustworthy when it comes to measuring power with non-sinusoidal and noisy waveforms.

Harmonic current

Harmonic current content can be measured using the Voltech PM1000. It gives a percentage of the fundamental up to the 13th harmonic. Results of this method was compared to that of the HP spectrum analyzer 3585A. The results were quite close. The Voltech PM3000 which is a three phase power meter measures harmonic currents to the 99th. Results show that harmonic current level beyond the 13th harmonic remain low throughout the spectrum. The proposed IEC555 specification is expected to require harmonic current content conformity to the 40th.

Efficiency

The three power devices add up to almost all of the losses. The inductor, MOSFET, and diode were selected to meet desired performance specifications at relatively low cost. An IRF840 seemed to provide the best performance at these power levels. A larger MOSFET (APT5025) did improve efficiency at low input voltage. However its larger output capacitance increased switching losses significantly at 100KHz. A very common 8A ultra-fast rectifier (MUR850) was used for the output diode. This oversizing was done because larger diodes have lower reverse recovery times for a given current level. New diodes have been introduced with lower reverse recovery times. A low cost ferrite EC core was used with AWG21 wires. There was very little temperature rise in the magnetic material. However the wires heated up at low input voltage where RMS current is significant. A low cost powdered iron with AWG20 magnet wire was also tried. Efficiency decreased about one percent.

Efficiency measurement requires accurate measurement of the output average power as well as the input average power. Because the output voltage as well as output current is DC, one might just measure the two readings using typical lab bench top DMM. However for one reason or another, this output power measurement did not match the measurement results of the average power reading of the Voltech power meter. The output power measurement was off by a factor of almost 6%. The bench top DMM used was Fluke's 8050A. To get truly accurate efficiency measurements, the same power meter should be used to measure both the output power as well as the input power.

Efficiency measurements for this application note was done on a Voltech PM3000 three phase power meter. This meter allows the connection of both the input power as well as the output power into one metering unit. Efficiency can be easily determined by measuring the input and output power with a push of a button. Accuracy however does not come easy even with this approach. The output power reading randomly varied up to 3% under steady state conditions.

Two different model meters from the same manufacturer gave current reading that was off by two to three percent. This might indicate that even if one was to go out of the way to obtain two same meters from the same manufacturer, efficiency measurements as well as other parameters may not be guaranteed to be as accurate as one may require.

Table 1. Performance Data

	PO = 50W					PO = 100W					PO = 150W					PO = 200W				
	V_O	P_O	P_i	PF	*n*	V_O	P_O	P_i	PF	*n*	V_O	P_O	P_i	PF	*n*	V_O	P_O	P_i	PF	*n*
	$I_{FUNDAMENTAL}$					$I_{FUNDAMENTAL}$					$I_{FUNDAMENTAL}$					$I_{FUNDAMENTAL}$				
%HARMONIC	3rd	5th	7th	9th	11th	3rd	5th	7th	9th	11th	3rd	5th	7th	9th	11th	3rd	5th	7th	9th	11th
	13th	15th	17th	19th	21st	13th	15th	17th	19th	21st	13th	15th	17th	19th	21st	13th	15th	17th	19th	21st
V_{IN} = 90VAC	395	54	62	0.99	0.87	387	105	117	0.99	0.90	379	153	166	0.99	0.92	371	197	218	0.99	0.90
	I_{FUND} = 0.67A					I_{FUND} = 1.3A					I_{FUND} = 1.8A					I_{FUND} = 2.4A				
	3.5	1.7	0.04	0.32	0.30	3.1	1.6	0.02	0.23	0.21	2.9	1.5	0.05	0.22	0.24	2.4	1.6	0.20	0.27	0.37
	0.06	0.05	0.05	0.01	0.11	0.04	0.03	0.06	0.01	0.01	0.09	0.18	0.18	0.12	0.13	0.24	0.24	0.24	0.15	0.15
V_{IN} = 120VAC	393	52	61	0.99	0.85	386	105	115	0.99	0.91	378	150	161	0.99	0.94	369	194	212	0.99	0.91
	I_{FUND} = 0.51A					I_{FUND} = 0.96A					I_{FUND} = 1.3A					I_{FUND} = 1.8A				
	3.7	2.2	0.12	0.46	0.37	3.2	1.9	0.05	0.29	0.25	3.1	1.9	0.01	0.21	0.26	2.9	1.9	0.09	0.15	0.12
	0.14	0.05	0.08	0.05	0.23	0.10	0.07	0.11	0.05	0.03	0.07	0.05	0.09	0.07	0.03	0.09	0.03	0.03	0.01	0.02
V_{IN} = 180VAC	394	52	60	0.96	0.87	385	105	114	0.99	0.92	378	151	163	0.99	0.93	369	190	207	0.99	0.92
	I_{FUND} = 0.34A					I_{FUND} = 0.64A					I_{FUND} = 0.87A					I_{FUND} = 1.2A				
	4.6	2.3	1.6	2.1	2.7	4.7	2.2	0.06	0.51	0.49	4.5	2.0	0.03	0.39	0.34	4.4	1.7	0.08	0.31	0.28
	1.9	1.0	0.87	0.95	0.66	0.18	0.17	0.12	0.12	0.08	0.11	0.12	0.12	0.10	0.04	0.11	0.09	0.09	0.04	0.02
V_{IN} = 220VAC	393	53	61	0.93	0.87	383	102	114	0.97	0.90	374	150	162	0.99	0.93	365	192	207	0.99	0.93
	I_{FUND} = 0.28A					I_{FUND} = 0.52A					I_{FUND} = 0.71A					I_{FUND} = 0.95A				
	5.4	2.4	0.21	1.0	1.0	5.3	2.8	0.02	0.77	0.51	4.9	2.3	0.08	0.56	0.35	4.7	2.3	0.06	0.47	0.33
	1.8	2.8	2.7	2.0	1.0	0.41	0.47	0.38	0.25	0.15	0.21	0.25	0.23	0.17	0.06	0.15	0.21	0.18	0.18	0.04
V_{IN} = 260VAC	394	53	62	0.87	0.85	387	103	15	0.95	0.90	379	153	164	0.97	0.93	372	195	208	0.98	0.94
	I_{FUND} = 0.24A					I_{FUND} = 0.44A					I_{FUND} = 0.61A					I_{FUND} = 0.82A				
	6.2	4.5	0.59	0.76	1.3	5.3	3.4	0.94	0.47	1.7	4.9	2.8	0.27	0.63	0.58	4.7	2.4	0.16	0.51	0.34
	0.96	1.1	0.36	1.5	2.3	1.4	0.80	1.0	1.4	1.0	0.26	0.35	0.53	0.24	0.10	0.24	0.26	0.38	0.14	0.01

The following are specifications to two inductors that may be considered for the 200W PFC converter.

Magnetics, Inc.
(412) 282-8282
OP44317 (Ferrite, EC)
N_p = 118 turns, AWG21
N_s = 5 turns, AWG30
gap = 1.7mm

Micrometals
(714) 630-7420
T184-40 (Powdered Iron, Toroid)
N_p = 102 turns, AWG20
N_s = 3 turns, AWG30

Performance Data

Table 1 shows the results obtained from an application circuit. Pertinent power and power factor measurements were taken as well as the harmonic current content as a percentage of the fundamental. It is intended to be a typical reference point in which to judge new designs. It is not unlikely that the performance can be improved and optimized via various methods.

Application Note 17

A Power Controller for Battery Powered Systems

William Cho

TABLE OF CONTENTS

I. INTRODUCTION

Battery powered products require the DC to DC converter and related power circuits to be highly efficient at minimum size and cost. To meet these goals new approaches are required.

The ML4862 replaces P channel MOSFETs and Schottky diodes with lower cost N channel MOSFETs to improve system efficiency. And it combines all necessary functions into one IC in order to most effectively reduce size and cost of the solution. Also flexibility of the approach will allow optimized designs for specific applications.

In applications where the processor shuts down and the system goes into deep sleep, the regulator chip must also power down into a micro amp sleep mode. Then when power is being delivered, the losses in the switching power conversion circuit must be kept to a minimum. The ML4862 maximizes battery life in either modes. It reduces current consumption down to micro amps while supplying power to a few supervisory IC's through a 5V linear regulator. Then when power is being delivered, the ML4862 uses low $R_{DS(ON)}$, N-channel MOSFETs to increase the efficiency of the entire system.

II. STEP DOWN (BUCK) CONVERTER WITH SYNCHRONOUS RECTIFICATION

When the battery voltage as well as the adapter voltage is higher than the load voltage, a step down "Buck" converter employing synchronous rectification provides the high efficiency solution required in portable applications. With low $R_{DS(ON)}$ power MOSFETs, power conversion efficiencies above 90% can be readily obtained.

Figure 2 shows the schematic of a typical application circuit. Operating specifications are as follows :

Input Voltage Range:	5.5V to 25V
Output:	5V 1.5A max
	3.3V 1.0A max
Output Ripple Voltage:	50mVpk-pk
Output Regulation:	± 5%

SYNCHRONOUS RECTIFICATION

Synchronous rectification refers to the method in which the power conversion circuit uses a power MOSFET in place of the catch diode for circulating inductor current (Figure 1). This significantly reduces the loss associated with the forward drop of the output rectifier. A Schottky diode with a forward drop of 0.5V at the rated current level can contribute more than 5 percent of the losses for a 5V output depending on the input voltage. A low $R_{DS(ON)}$ MOSFET can significantly reduce this loss

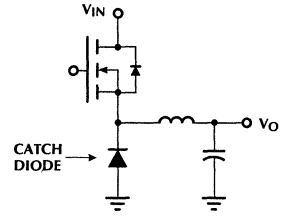


Figure 1. Typical Step Down Regulator

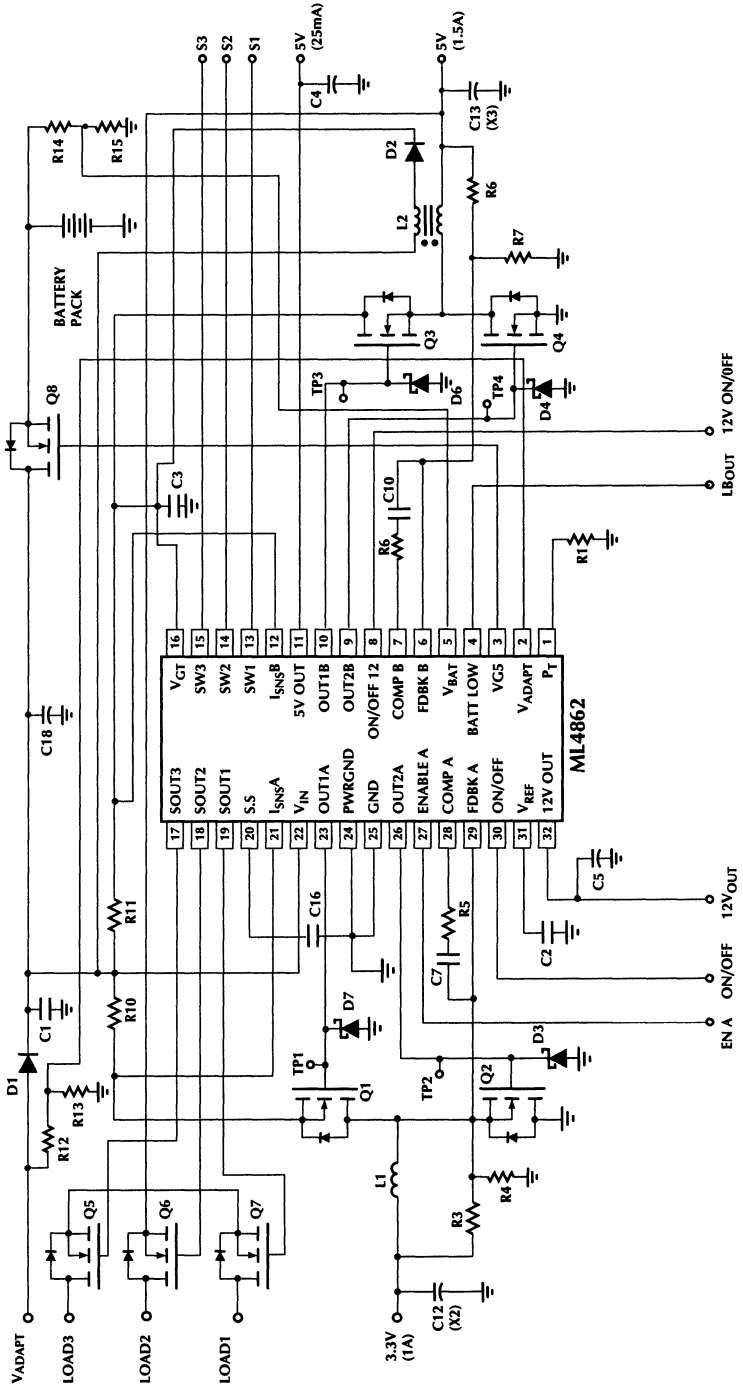


Figure 2. Typical Application Circuit

component. For a 3.3V system synchronous rectification is an absolute must. Also contributing to the attractiveness of this approach is the growing selection and availability of low $R_{DS(ON)}$, low voltage power MOSFETs in attractive surface mount packages.

This new controller makes synchronous rectification considerably easier to implement. The control IC provides two gate drive outputs where one is the inverse of the other. An anti shoot through circuitry is included to keep both FETs from ever being on at the same time.

Figure 3 shows both highside and lowside gate drive waveforms for both regulators. With a 10V input, gate voltage for the highside (upper) MOSFET is 20V. This guarantees that the gate to source voltage of the upper MOSFET is 10V. This higher than input gate voltage can be generated from an additional winding on the main 5V output inductor. By tying one end of the secondary to the input voltage and providing a two to one turns ratio, the gate drive voltage is guaranteed to be 10V above the input at any input voltage.

The lower gate drive is limited to 15V max. Each regulator operates independent of the other.

In high current, high input voltage applications low current Schottky diodes across the drain to source of low side MOSFETs (Q2 and Q4) can increase efficiency by 1%. This is due to relatively slow reverse recovery characteristic of the power MOSFET's intrinsic diode. This loss component will become more significant as input voltage or frequency is increased.

MOSFET SELECTION

Low voltage, low Rdson MOSFETs have become available that allow synchronous rectification to become an attractive solution in applications demanding high efficiency. MOSFETs can have Rdsons ranging anywhere from a few milliohms to hundreds of milliohms.

While these new MOSFETs are typically "logic level" devices, enhancing them with 10V will reduce the Rdson by 25 to 100 percent.

MOSFET selection will be based on voltage, Rdson, cost, and size. Typically a MOSFET has higher input capacitance if the die size is larger. Larger die size is required when Rdson needs to be reduced or voltage rating of the device needs to be increased. Thus average gate charge/discharge current increases proportionately. Also switching transitions may increase depending on input capacitance of the MOSFET. Thus a reduction in MOSFET Rdson may not always result in proportionate improvement in efficiency.

A good starting point is to assume about 1% of the output power to conduction losses in the switches. With this assumption:

for the highside MOSFET,

$$R_{DS(ON)} = \frac{V_I}{100I_O}$$

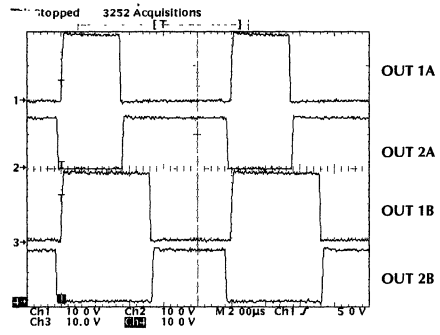


Figure 3. Gate Drive Waveforms of both Regulators.

for the low side MOSFET,

$$R_{DS(ON)} = \frac{V_O V_I}{100I_O(V_I - V_O)}$$

where,

V_I = minimum input voltage

I_o = maximum output current

A table is provided below that lists the appropriate MOSFETs for use with the ML4862. They are low in Rdson, low in input capacitance, and are available in surface mount packages.

A Schottky diode is required at the gate drive pins of all four MOSFET driver outputs (pin 9,10,23 and 26) to clamp the negative going voltages. For the lower MOSFET, parasitic capacitance from drain to gate of the lower MOSFET cause the gate of the MOSFET to go negative when the upper MOSFET is turned off and current begins to conduct through the diode of the lowside switch.

The gate of the upper MOSFETs is pulled negative through a parasitic gate to source capacitance during a transient, low load condition when inductor current that was actually going back into the input is suddenly shifted to the lower MOSFET when the lower MOSFET is turned on.

TABLE 1. MOSFET SELECTOR GUIDE FOR ML4862

MTD10N05E	50V, 0.1ohm	DPAK	Motorola	;for 1 to 2 A
MTD3055E	60V, 0.13ohm	DPAK	Motorola	;for 1A and under
MMDF4N02	20V, 0.1ohm, dual	S08	Motorola	;1A to 2A, low Vi
SI9956	20V, 0.1ohm, dual	S08	Siliconix	;1A to 2A, low Vi
Si9955	50V, 0.3ohm, dual	S08	Siliconix	;low Ii and high Vı
Si9410	30V, 0.03ohm	S08	Siliconix	;2A to 4A
IRFR020	50V, 0.1ohm	DPAK	I.R.	;for 1A to 2A

INDUCTOR

The inductor plays a critical role in the overall performance of the converter circuit. Off the shelf inductors are specified with three main parameters. These are inductance, maximum DC current, and maximum DC resistance. These specifications dictate the size of the inductor. AC core loss is another important aspect of the inductor. However this data is typically not provided by the inductor vendors.

Of the many varieties of magnetic materials available two types of materials that would be well suited for this application is worth noting. One is low loss powdered iron and the other is ferrite.

Powdered iron toroidal inductors are typically mounted to some type of carrier for surface mounting in portable applications. Some of these inductors are specially designed for low loss characteristics. "Kool Mu" core material from Magnetics Inc. is one example.

Ferrite material is usually used in conjunction with a plastic bobbin on which the magnet wires are wound. The bobbins are available with surface mount pins. Bobbins allow additional voltages to be generated. Ferrites have lower core loss than powder irons. Also ferrites with bobbins are usually better suited for high speed, high volume manufacturing.

Toroids are best suited for low profile, low current applications. Toroids are mounted on some type of a surface mount carrier and is available as standard product.

Three suggested vendors for inductors and coupled inductors are:

Coiltronics
984 S.W. 13th Court
Pompano Beach, FL 33069
(305) 781-8900

Sumida
637 East Golf Road
Suite 209
Arlington Heights, IL 60005
(708) 956-0666

Pulse Engineering
P.O. Box 12235
San Diego, CA 92112
(619) 674-8100

All three companies have surface mount inductors good for portable applications. These vendors as well as various others can wind coupled inductors to exact specifications.

Determination of inductance required takes understanding of the current waveforms under low load conditions. Figure 4 shows the inductor current at light load conditions. Under this condition, part of the current is "shuttled" (channel 3) back and forth between the output capacitor and the input capacitor. Efficiency will suffer at this light load condition due to conduction and switching losses.

Inductor value for a given application can be determined by the following equation:

$$L = \frac{(V_I - V_O)V_O}{V_I f \Delta I}$$

where,

V_I = Minimum Input Voltage

f = Switching Frequency

Delta I (ΔI) is the amount of ripple current (or AC current) in the inductor. Its value should be approximately 40% of the maximum output current. 40% is a good trade-off starting point between high RMS losses due to high peak current if inductance is too low and high conduction losses due to high number of turns required if inductance required is too high. Ripple current anywhere from 20% to 100% of maximum output current should be acceptable. Ripple current in the inductor set up for 40% of the maximum output current will cause "shuttling" at output current less than 20%.

When a higher input voltage such as that from the adapter is applied to the input, ripple current in the inductor will increase. The ESR of the output capacitor should be low enough to keep the ripple voltage below the desired value.

Low ripple current translates to low core loss. Thus copper loss will likely dominate. It is desirable to have the DC resistance of the inductor be one quarter of the sum of the two MOSFETs. This will distribute the conduction losses evenly among the three power components.

Current rating for these inductors represents a current level at which either the inductance decreases from the initial value by some percentage or the temperature rises by some value above the ambient. Since the inductor is in series with the output, the maximum DC current rating of the inductor should be slightly above the maximum output current requirement. More specifically the peak inductor current which includes the ripple current should not exceed the maximum DC current rating of the inductor. Keep in mind that at higher current levels inductance decreases. Peak inductor current used to determine inductor size and output ripple voltage should reflect this variation.

The peak current rating of the inductor typically includes margin for variation in permeability of the material as well as its saturation level. Variation in permeability will vary the inductance for a given number of turns. Variation in saturation level varies the current level at which the inductor value has a steep roll off. Powdered iron inductors have a softer saturation curve than ferrites. Because of this and the fact that current limit trip point can be set many times the maximum output current level, it may be possible to have the output surge current exceed the maximum current rating of the inductor. A later section will cover in detail the current limit function.

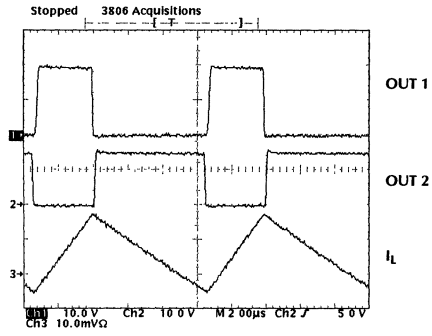


Figure 4. "Shuttling" Inductor Current

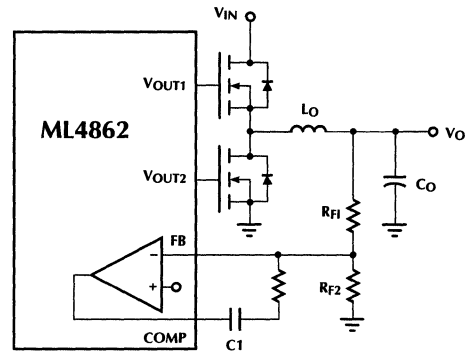


Figure 5. Feedback Loop

INPUT AND OUTPUT FILTER CAPACITORS

Input capacitance provides the filter for squarewave ripple current needed by the switching regulator when the power is being supplied by the adapter. Ripple voltage can be quite significant if enough capacitance is not provided. At low input voltage the ripple voltage can actually cut into the maximum power output capability of the regulator. Ripple voltage is a result of two effects. The primary contributor to ripple voltage is the ESR (Equivalent Series Resistance) of the capacitor. If ESR of the capacitor is 0.2 ohms, ripple voltage will be approximately 200mV for a 1 Amp inductor current. Another contributor to ripple voltage is voltage droop due to current being drawn out of the capacitor during the cycle. With a 50% duty cycle at 100KHz, 10V input, and 1 amp in the inductor, ripple voltage due to capacitor discharge is 50mV for a 100µF input capacitor.

Output capacitance is determined by the amount of ripple voltage allowed at the output. Like the input capacitor, ripple voltage is due to ESR and voltage decay of the output capacitor. However in this case the inductor is in series with the capacitor. Thus only the AC component of the inductor current contributes to the ripple voltage.

ESR varies as function of size and construction. Tantalum capacitors have lower ESR than electrolytic capacitors. Larger capacitors will show lower ESR.

Another factor in determining the amount of output capacitance is the requirement to keep the loop stable. Peripheral circuits get switched in and out of the output of the regulator by the power management circuits. Each peripheral unit will add to the total capacitance present at the output. Loop stability may be compromised if this switched in capacitance is too large. A good rule of thumb amount is to at least match the regulator output capacitance to the total load capacitance. For instance if the disk drives, communication devices, and display circuits add up to 300µF of total capacitance, the regulator should at least have that much capacitance to keep the loop stability manageable.

For the output capacitor 100µF of capacitance for every 500mA of output current is a good place to start.

COMPENSATION

Proper compensation achieves two important goals. One is stability of the circuit over the entire range of operating conditions. Variations in input voltage, output current, and output capacitance can cause the circuit to be unstable if not properly compensated.

Another important goal of loop compensation is to maximize the loop bandwidth of the converter. This is important if load can vary widely instantaneously.

A simple resistive compensation method can meet both of the criterias above and is illustrated below.

Control voltage (error amp output) to output (converter output) response transfer function has a two pole roll off due to L_O and C_O. A zero is required to keep the unity gain crossover slope to a single pole roll off. This provides the phase margin required for stable operation. The ESR (Equivalent Series Resistance) of the output capacitor provides this zero. If this zero occurs at a high frequency due to very low ESR, gain is required to raise the transfer function such that unity gain crossover occurs with a one pole roll off. If however ESR was high, unity gain crossover would occur at too high a frequency. Unity gain crossover bandwidth near the switching frequency will also result is unstable operation. The objective is to select the compensation values that will work between the maximum and minimum ESR value of the output capacitors.

The following equations estimate the minimum to maximum ESR that should be allowed at the output capacitors:

$$ESR_{MIN} = 0.5\sqrt{\frac{L_O}{C_{O_{MAX}}}}$$

$$ESR_{MAX} = \sqrt{\frac{L}{C_{O_{MIN}}}}$$

Minimum and maximum ESR may be less with lower input voltage. However, since the ESR varies somewhat and since secondary effects can become factors, the most practical method of compensation is to empirically determine the proper values. The following equations provide a starting point:

$$R_1 = 0.02\pi \text{ GBW } R_{f1}\sqrt{L_O C_{OMAX}}$$

$$C_1 \geq \frac{\sqrt{L_O C_{OMAX}}}{R_{f1}}$$

Once R1 is tried in the circuit and stability is not maintained throughout the line and load variations, R1 should be varied in a step by step fashion. Increasing R1 increases gain and compensates for low ESR capacitors while reduction in R1 is just the opposite. Once stability is maintained throughout load and line variations, C1 should be included to provide high DC gain. This provides improved line regulation.

CURRENT LIMIT AND SOFT START

Current sensing is required for current limiting in the event of a short circuit at the output. Since this is a catastrophic condition, current limit circuit is designed to initiate a latched soft start once current limit is triggered. This will reduce the average current in the inductor as well as the lower MOSFET to acceptable levels. Without a latched soft start, the current in the inductor can build up until one of the power devices fails.

Current limit circuitry also limits current on a cycle by cycle basis. This keeps the peak inductor current under controlled levels until the soft start capacitor is discharged. Figure 6 shows the cycle by cycle current limiting taking place during the first 4 cycles until the soft start capacitor (0.1µF) has been discharged enough to limit duty cycle by limiting the output voltage of the error amplifier. Trace 1 is output voltage. Trace 2 is the soft start capacitor voltage. Trace 3 is the inductor current. Trace 4 is gate drive of the upper FET.

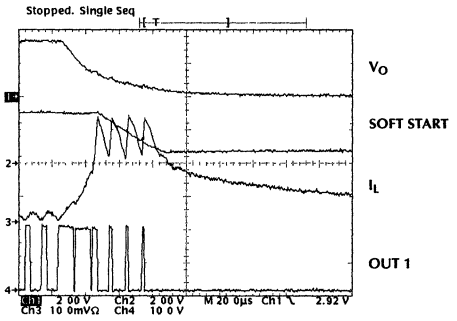


Figure 6. Short Circuit Condition Waveforms

Current limit threshold has been set at 200mV in the ML4862. Since trace width and length can be very tightly controlled the only variable is its thickness. Tolerance of the trace thickness may be as high as 30 percent depending on the production capability of the PC board manufacturer. A 1 oz copper circuit board trace of 10 mil wide and 2 cm long will provide approximately a 25 milliohm sensing resistor. This sets up a current limit trip point somewhere between 5A to 10A. This is a good set point range for a 1.5A output converter since its design should have about a 0.1 ohm $R_{DS(ON)}$ MOSFET. A 0.1 ohm $R_{DS(ON)}$ MOSFET can readily handle a pulsed current in the 10A range.

Filtering the I_{SENSE} pin is not recommended. The current limit comparator has a reduced bandwidth. Thus high frequency spikes will be ignored. However since the 100KHz ripple can easily reach 200mV, it is important to keep the impedance between V_{IN} (pin #22) and I_{SENSE} (pin #12 and #21) as low as possible. This way current limit will only occur when the differential voltage between V_{IN} and I_{SENSE} exceeds 200mV.

A 15µA current source charges the soft start capacitor. A 6.5mA current sink discharges the capacitor. The discharge latch releases when the capacitor has discharged to a voltage below a diode drop. In most applications, a 0.1µF capacitor will be sufficient to limit startup current in order to avoid output overshoot.

LAYOUT

Layout of the circuit is as important as would be in other power control circuits. High current paths should be kept as short as possible while providing wide traces to keep inductance and resistance to a minimum. Filter capacitors (C2, C3, and C4) should be placed as close to the IC as possible.

Since the sensing element for the current limit comparator will be a circuit board trace, the current path from the input capacitor to the sensing node should not include any stray resistance. This will require that the input capacitor (C18) be very close to the IC.

Prevent high current from circulating near the ground plane surrounding the IC. Current pulled from the input capacitor as well as that flowing through the lower MOSFET will be square wave current. Ground connections should make direct contacts to the ground plane to keep stray inductances to a minimum.

III. BOOSTED VOLTAGE FOR HIGHSIDE GATE DRIVE

Boosted voltage for highside gate driving can be accomplished in two ways. One is to use an inductor with an extra winding. This guarantees that the MOSFETs are fully enhanced at any input voltage. Also it can supply the high current needed for the 12V linear regulator. Another method uses a charge pump. This is a lower cost solution but limits the maximum voltage allowed.

COUPLED INDUCTOR

What appears to be a transformer in the schematic is actually a "coupled inductor" since it performs the function of an inductor. That is, it stores energy during one cycle and releases it during another. A transformer typically would not store energy but transfer energy from primary to secondary instantaneously.

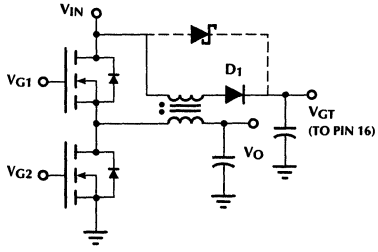


Figure 7. Coupled Inductor

Secondary winding (Figure 7) charges the capacitor on pin 16 (V_{GT}) to:

$$V_{GT} = V_O \frac{N_2}{N_1} + V_I$$

This guarantees that the highside switches will always get full enhancement regardless of the input voltage.

When the upper MOSFET is "on", the diode at the secondary of the inductor is reverse biased to block any current. Then when the upper MOSFET is turned off, the inductor current circulates through either the lower MOSFET in the primary or through the diode at the secondary whichever has a lower voltage.

A coupled inductor in a Buck topology has its limitation in its ability to regulate the secondary as other topologies do. Limitations are voltage drops due to resistance as well as magnetic coupling between the primary and the secondary. However, since the load current (which is the IC supply current) is fairly constant, variation in secondary voltage will be minimal.

If however the 12V linear regulator is used for high current purposes, secondary voltage (or V_{GT}) may drop as much as 3 to 4 volts depending on input voltage, output current, and inductor design. However since this is a momentary occurrence the gate drive voltage may drop a few volts without causing any detrimental effects.

Figure 8 shows current being shared between the primary (waveform 3) and secondary (waveform 4) windings as well as gate drive waveforms of the upper (waveform 1) and lower (waveform 2) MOSFETs.

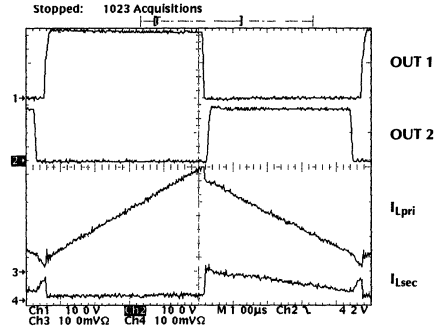


Figure 8. Primary and Secondary Current Waveforms

CHARGE PUMP

Another method of boosting voltage is to use a capacitor and a diode to charge pump the voltage. However this method has its limitations. Since the charge current must come from the input source the resulting voltage will be almost twice the input voltage. That means at low input voltage MOSFET gate to source enhancement will be low. And at high input voltages the enhancement voltage may exceed the 20V maximum gate to source voltage rating of power MOSFETs. The charge pump schematic is shown in Figure 9. Gate drive supply voltage (V_{GT}t) is:

$$V_{GT} = 2V_I - 2V_{DIODE}$$

This says that a system with a low input voltage range (6V to 18V) will have enhancement voltage as low as 5V at its lowest point. However since the maximum input voltage is also low, a low voltage (20V) MOSFET with low threshold can be used. Low threshold (logic level) MOSFETs typically have Rdson specifications at both 5V and 10V of V_{GS} (gate to source enhancement voltage).

As noted previously maximum gate to source enhancement for any power MOSFET is ±20V. Thus a system with a higher input voltage range will require a

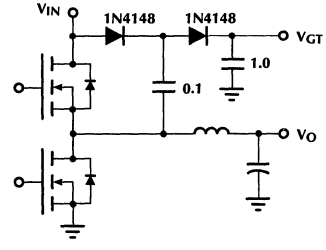


Figure 9. Gate Drive Voltage Charge Pump

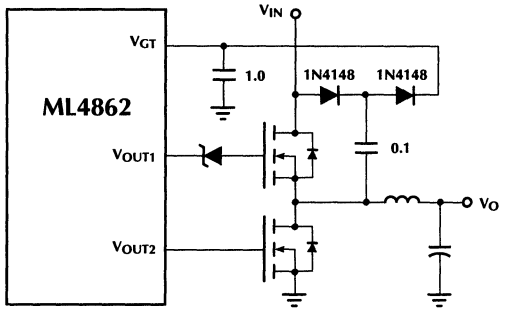


Figure 10. Zener Gate Drive Clamp for High Input Voltage

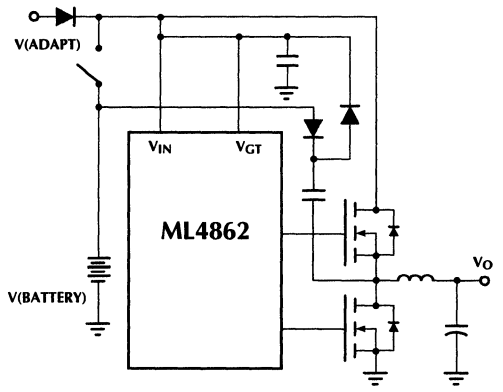


Figure 11. Charge Pump from the Battery

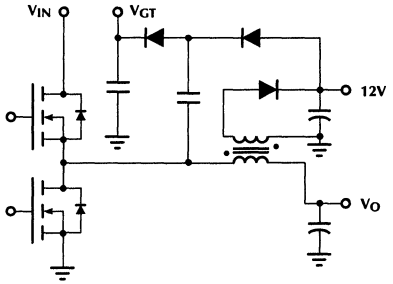


Figure 12. Auxiliary Winding and Charge Pump

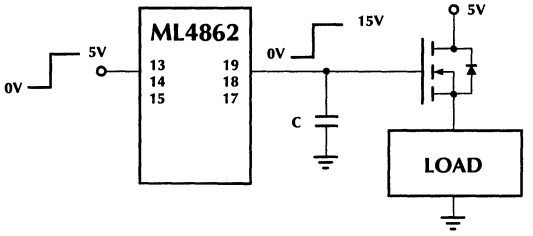


Figure 13. Load Switching Circuit

Zener diode to reduce the enhancement voltage when maximum input voltage will be applied (Figure 10). However enhancement voltage at lowest input voltage must also be considered. Low threshold MOSFETs may be required to accept a wide input voltage range using this method.

In cases where the adapter input voltage is too high, the battery can be used as the source voltage for the charge pump (Figure 11).

A combination of charge pump and coupled inductor can be also be used to generate the boosted voltage and an additional output voltage. This provides a minimum load to the auxiliary output since the IC will always draw some amount of current when powered up (Figure 12).

V_{GT} in this case is always about 12 volts above the input. This will guarantee full gate to source enhancement at any input voltage. The 12V output however can vary significantly (2 to 3 volts) over line and load variations. If a tightly regulated 12V is required, a linear post regulator is recommended. This subject is discussed further in a later section.

IV. ADDITIONAL FEATURE OF THE ML4862

The ML4862 contains additional features designed to increase the battery life of the system.

LOW LOSS BATTERY CONNECT SWITCH

A very low R_{DSON} N channel power MOSFET can be used to connect and disconnect the battery to the DC to DC converter. V_{GT} is used for the enhancement voltage required.

As soon as the adapter is connected to the portable unit the ML4862 will sense it and turn the MOSFET off. When the adapter is removed, current from the battery flows through the intrinsic body diode of the MOSFET. Then when the MOSFET is turned on, all of the current will flow through the lower resistance path. The fall time of the gate voltage is about 200ns. Rise time is around 3µs.

LOGIC TO 15V VOLTAGE TRANSLATORS

Load switching is required in many power management applications. In order to use low cost, low R_{DSON} N channel MOSFETs, 15 volts must be applied to the gate of the MOSFET to provide enough enhancement voltage needed. The ML4862 translates three logic level signals to 15V internally (Figure 13).

When a capacitive load is being switched in, it is important to consider slowing down the rate of turn on of the MOSFET switch. For example if the output of the 5V regulator has 300µf of capacitance and 100µF of capacitance is switched in with the load, the 5V output will drop hundreds of millivolts instantaneously until the feedback loop of the regulator can compensate for it.

To slow down the rate of fall, a capacitor is required from the gate of the MOSFET to ground as shown in Figure 13. Figure 14 shows that when a 100µF capacitor was switched into a regulator with 300µF of output capacitance, a 2.2nF capacitor on the gate of the MOSFET slowed down the gate waveform enough keep the outputs regulating. This is facilitated by having the gate drivers limit current to a few tens of microamps.

Load switching may be required to more than three locations. N channel MOSFETs can be used for high current loads while logic level P channel can be used for lower current sections.

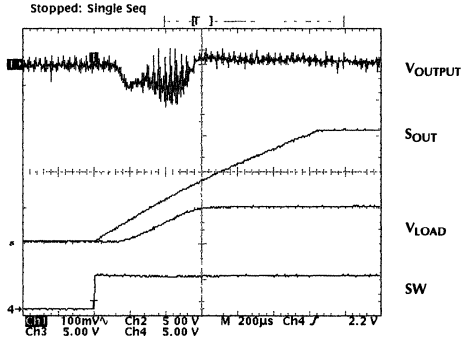


Figure 14. Capacitive Load Regulation

LOW BATTERY DETECT COMPARATOR

Low battery detect comparator can be used for any of several functions. These are:

1.Battery Low Indicator

2.Battery Removed Flag

3.Linear Regulator Dropout Indicator

4.Output Voltage Good Indicator

The output of the comparator is open collector.

FLASH MEMORY PROGRAM VOLTAGE REGULATOR

If 12V flash memory programing occurs very rarely, efficiency should not be of importance. For such applications a linear regulator is provided that steps down the boosted V_{GT} voltage to 12V. The linear regulator will potentially supply up to 100mA. The limitation will be power dissipation. Maximum output current is calculated by:

$$I_{O(MAX)} = \frac{P_{D(MAX)}}{V_{GT} - 12V}$$

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{D(MAX)}}{R_{OJA}}$$

Since the regulator will be used infrequently, a maximum peak junction temperature of 150°C can be tolerated. A typical application with 27V maximum V_{GT} voltage and 60°C maximum ambient temperature will be able to source 100mA of current continuously.

MICROPOWER 5V LINEAR REGULATOR

When the IC is put into sleep mode, only the reference, the linear regulator, and the comparator will be alive. The 5V micropower linear regulator can supply up to 25mA to supervisory IC's. A 10 µF capacitor on pin 11 is required for stable operation.

V. DESIGNING IN MORE FUNCTIONS

More functions can be added to the circuit by using external components. Another option is to incorporate additional features into a semi standard version of the IC. This is possible due to the USIC methodology used when developing the ML4862. A modified part can be realized by making as little a change as a single metal layer change. This provides a quick turn around, low risk method of arriving at the optimum solution.

"BURST" MODE

Burst Mode increases the efficiency of the regulator at very light loads. This is achieved by putting the IC into micro amp "sleep" mode between power cycles.

When "Mode A" point is pulled low, the main regulator loop is forced to take the output to a higher voltage (figure 15). However the open collector comparator releases the voltage divider set up at the inverting input of the hysteretic comparator. When the upper threshold is reached, the comparator shuts the IC down until the lower threshold is reached. Then the IC comes back alive to pump the output to the upper threshold again. Figure 16 shows the ripple voltage on the output capacitor. Output ripple due to the hysteresis is given by:

$$V_{RIPPLE} = 2.5\frac{R2(R3+R4)}{R1R2}$$

The soft start circuit must be disabled when in burst mode. However it is required during power up. The second

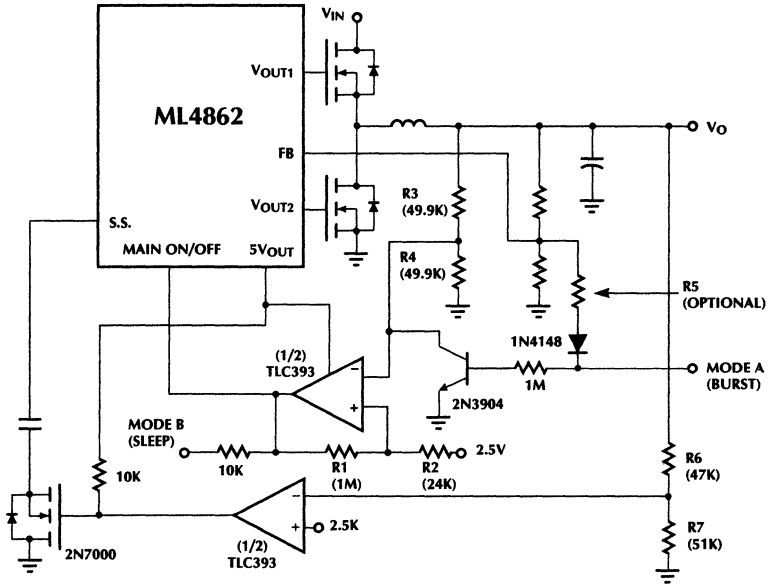


Figure 15. "Burst" Mode Circuit

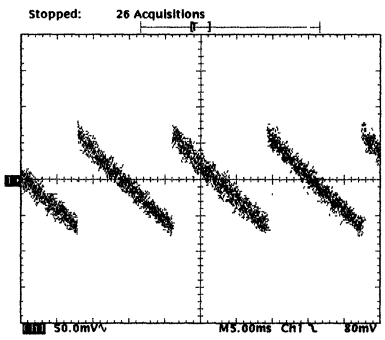


Figure 16. Output Ripple during "Burst" Mode

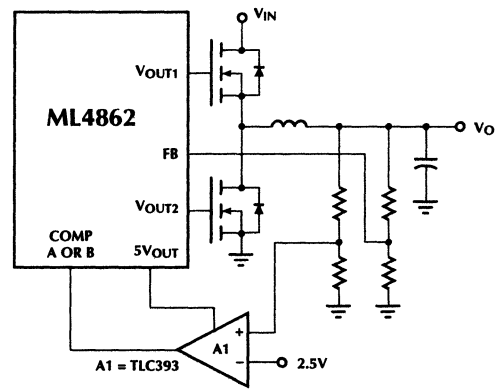


Figure 17. Supply Sequencing Circuit

comparator guarantees that the soft start capacitor is active only when the output is well below regulation voltage.

When the 5V output is monitored during "burst" mode, 3.3V output must be guaranteed to have load current less than that required by the 5V output. Otherwise 3.3V output will go out of regulation and may exhibit unstable behavior.

Efficiency in "burst" mode was measured for the typical application circuit. The results are as follows:

Input voltage: 10V

Efficiency at	5mA	65%
	10mA	69%
	15mA	72%
	50mA	75%
	100mA	80%

POWER SUPPLY SEQUENCING

Output voltage may be required to meet sequencing requirements during power up. This can be best accomplished by forcing the error amplifier output of the second regulator low while the first regulator output voltage is rising. Figure 17 shows one solution that can work. It forces the error amplifier output to be low on one regulator while the output voltage of the other is rising (Figure 18).

Some applications may require an additional soft start circuitry to keep the second output from overshooting. With the addition of a PNP transistor, a capacitor, and a resistor soft start can be achieved (Figure 19).

Another method of supply sequencing is to pull the FB pin high through a diode. This will set the upper drive (pin 10 or pin 23) low and the lower drive (pin 9 or pin 26) high.

AUXILIARY VOLTAGES

Additional negative or positive voltage can be produced with additional windings on the inductor. And due to synchronous rectification, auxiliary output current is not limited to some percentage of current level in the main output. Output current is limited only to the size of power devices selected.

Since additional windings on the inductor means a custom inductor, the method in which the winding is done as well as the selection of core material and geometry can impact the effectiveness of the solution.

The following steps should be taken to determine the coupled inductor required:

1. Determine maximum primary current which is the sum of worst case current between the primary and the secondary under all possible load current combinations. Secondary current should be referred to the primary by multiplying it with the turns ratio and duty cycle.

2. Determine inductance, maximum inductor current, and maximum DC resistance of the primary according to guidelines in Section II.

3. Regulation is a function of magnetic coupling and resistive drops due to variations in current levels. In cases where regulation must be tight (i.e. ±5%) a post regulator (i.e. linear regulator) will be required. In other cases where regulation may be loose (i.e. ±10%) post regulator may not be required if the following conditions can be met:

   a. Limited variations in output current.

   b. Tightly coupled magnetics.

   c. Limited variations in input voltage.

   d. Low voltage drops in winding resistance.

A high current, tightly regulated 12V output can be produced using an external regulator (Figure 20). The

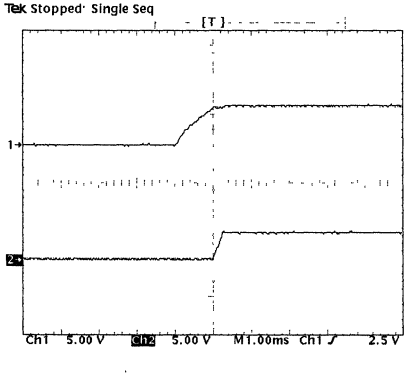


Figure 18. Both outputs during power up.

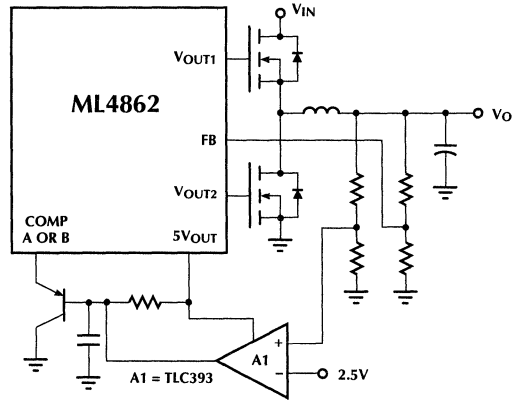


Figure 19. Supply sequencing with soft start

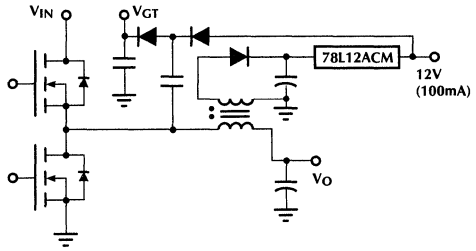


Figure 20. High Current 12V Output

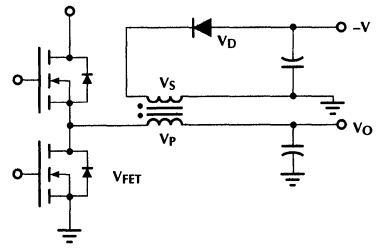


Figure 21. Auxiliary Winding for a Negative Voltage

dropout voltage of the linear regulator and the regulation range of the secondary must be considered when selecting the number of turns on the secondary. For a 100mA output regulator (i.e. 78L12ACM from Motorola), the drop out voltage is 2.5V maximum. And a typical secondary winding may drop in voltage of 2.5V. Thus the secondary output must be designed for 17V. This means a worst case power dissipation on the linear regulator of 500mW. This is well within the recommended maximum operating power dissipation range of the device.

Figure 21 shows how a negative voltage can be generated. In applications such as bias voltage for display contrast control, tight regulation is not required since its voltage must be adjustable. With the generated negative voltage, an adjustable negative linear regulator (i.e. LM337LM or Z) can be used.

VI. PARTS LIST AND EFFICIENCY DATA

Parts list for the typical application shown in Figure 2 is provided on the following page.

EFFICIENCY DATA

In order to get accurate efficiency measurements voltmeter connections should be made as close to the input and output filter capacitors as possible. The following lists the efficiency data taken with the typical application circuit.

Vin	I5 = 0.3A I3 = 0.3A	I5 = 1A I3 = 0.5A	I5 = 1.5A I3 = 1A
6V	91.6%	93.3%	92.6%
10V	87.7%	91.8%	91.5%
15V	84.0%	90.6%	90.9%
20V	80.7%	89.2%	89.9%
25V	77.6%	87.5%	88.8%

Efficiency can always be optimized to a certain power level and at a certain input voltage. One way of improving efficiency is to reduce the resistance of the inductor. However this requires a larger inductor. Another method of reducing losses is to reduce the switching frequency at the expense of a larger inductor. Also lower voltage and lower input capacitance MOSFETs help reduce losses. This is particularly true for low input voltage applications (18V max). 20V, dual N channel MOSFETs in S08 package from Motorola (MMDF2N02) is a good solution. A pin for pin equivalent part is also available from Siliconix (S19956).

One thing to keep in mind is that selecting a lower on resistance MOSFET does not always mean an improvement in efficiency. Efficiency will improve only if conduction loss of the MOSFET was higher than switching losses which includes gate charge current and power lost when simultaneous voltage and current is applied to the switch during switching transitions.

TABLE 2. PARTS LIST AND EFFICIENCY DATA.

Capacitors	
C1,C3	1.0, µF, Ceramic
C2,C16	0.1, µF, Ceramic
C4	10, µF, 6.3V (Aluminum Electrolytic)
C5	10, µF, 16V (Aluminum Electrolytic)
C7	15, nF, Ceramic
C10	4.7, nF, Ceramic
C12	100, µF, 4V (Aluminum Electrolytic) (X2)
C13	100, µF,6.3V (Aluminum Electrolytic) (X3)
C18	100, µF, 35V (Aluminum Electrolytic)
Resistors	
R1	130K
R3, R7, R8	10.0K, 1%
R4	31.6K, 1%
R5	82K
R6	56K
R10,R11	25mOhm, (PC trace or thin wire)
R12	75K
R13	24K
R14	750K
R15	240K
MOSFETs	
Q1,Q2, Q3,Q4	MTD10N05E, 50V, 0.10 Ohm (X4) (Motorola)
Q5,Q6,Q7	MMDF2N02, Dual 20V, 0.10 Ohm (X2) (Moto)
Q8	Si9410, 30V, 0.030 Ohm (Siliconix)
Diodes	
D1	MBRD330, 30V, 3A (Motorola)
D2	1N4148, 75V, 0.1A
D3,D4,D6,D7	BAT64-06 (Siemens) or BAT54A (Philips)
Inductors	
L1	CDR125, 47µH, 1.5A (Sumida Electric)
L2	CTX05-11209-1, 50µH, 1.5A (Coiltronics)

Resistors are 5% unless noted otherwise.

Application Note 19

Phase Modulated PWM Topology with the ML4818

by Mehmet K. Nalbant

INTRODUCTION

One of the biggest goals in power supply design is to get the maximum amount of output power while maximizing efficiency and minimizing both the cost and size of the respective power supplies. There are many conflicting parameters in trying to do so. For example, lets examine how the size of a power supply is a strong function of the size of the passive storage elements. It is well known that the size of inductors and capacitors greatly depends on the operating frequency. The higher the frequency the smaller the inductors and capacitors necessary. Increasing the operating frequency is one thing, implementing it is another. It is also a well known fact that increased operating frequencies result in lower efficiencies in PWM controlled switched mode power supplies.

Increasing the frequency of PWM controlled power supplies was one solution in the reduction of the passive elements. That posed some limitations due to the nature of operation. Simultaneous conduction of high currents in the presence of high voltage during turn-on and turn-off times at high frequencies resulted in high switching losses. Thus violating one of the most important parameters of the switching power supply design that is the efficiencies were now lower than in lower frequency operation.

This application note will introduce the "Phase Modulated PWM Topology" that overcomes many of the shortcomings of conventional PWM topologies at high operating frequencies.

LOSSES IN SWITCHING POWER SUPPLIES

The typical losses in switching power supplies can be divided in two classes conduction losses and switching losses. The most common switching element used in modern switching power supplies is the power MOSFET. This device when enhanced for conduction has a finite channel resistance named $R_{DS(ON)}$. When current passes through this device conduction losses result which are proportional to:

$$P_C = I^2_{DS(RMS)} R_{DS(ON)}$$

In addition to the conduction losses, due to the switching action of the device in the presence of high currents and high voltages, there are also switching losses. These losses can be further subdivided in turn-on , turn-off and capacitive discharge losses. Figure 1 shows how turn-off losses can result during switching in a simplified way.

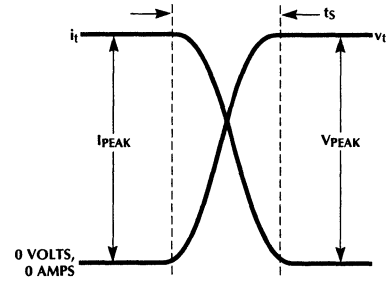


Figure 1. Waveforms in the switching element in a switching power supply during turn-off, assuming linear rise and fall.

The energy in turn-off instance can be found by integrating the product of the voltage and current waveforms over the complete switching interval i.e.,

$$W_{t_{OFF}} = \int_0^{t_S} v_t i_t dt$$

Assuming linear waveforms and symmetry the above integral can be simplified to the following:

$$W_{t_{OFF}} = \frac{1}{2} I_{PEAK} V_{PEAK} t_s$$

The total power lost therefore can be found by multiplying the above with the repetition rate, that is the switching frequency hence

$$P_{OFF} = \frac{1}{2} I_{PEAK} V_{PEAK} t_s f$$

To give an example suppose that the power switch switches 10 amps at 380 volts for 50nsec at 100KHz. The resulting power loss due to just this event would be 9.5 Watts. At 200KHz it would be 19 Watts and so on. This power loss must be dissipated by the switching element and poses a problem for the adequate removal of the generated heat. One can appreciate the losses at even higher frequencies.

Turn-on switching losses result in a similar manner. Assuming again symmetry the turn-on losses can be found by integrating the current and voltage waveforms over the switching interval.

$$P_{ON} = \frac{1}{2} I_{PEAK} V_{PEAK} t_s f$$

We are going to see later that the switching event is more complicated than what is depicted above due to the presence of parasitic inductive and capacitive components such as leakage and lead inductances and drain source capacitances.

To reduce the switching losses several methods were used such as dissipative and non dissipative snubbers. As the name implies dissipative snubbers dissipate their energy as heat, whereas the non-dissipative snubbers return their energy back to the input line, thus tending to be more efficient. In any case even with the use of non dissipative snubbers there remain problems that limit the maximum operating frequency.

Several respected institutions along with many manufacturers tried to find a way around the above problems. This resulted in the proliferation of several new power supply topologies with each one claiming to be the solution for operation at high frequencies.

Resonant power supplies thought to be a possible solution had their own share of problems. Although not a new technology they found a home in some applications. They were never really widely accepted by the industry. Part of the reason was the absence of analytical tools for the analysis and design and suitable controllers. Thanks to the efforts of many people they are better understood today but most of the manufacturers are still reluctant to put products on the market based on this technology.

Resonant power supplies encompass a wide range of topologies and they can be subdivided into three major subclasses. These are as follows:

1) Current resonant or zero current switching ZCS.

2) Voltage resonant or zero voltage switching ZVS.

and

3) Multi-resonant, in the majority of which both the current and voltage is resonant.

It is beyond the scope of this application note to give an exhaustive explanation for each type of the resonant conversion techniques. For more information, the interested reader can draw on the vast amount of technical papers published over the last few years. It suffices to say that among the resonant conversion techniques one that is of particular interest for high frequency operation is the zero voltage switching, or ZVS.

Switches such as power MOSFETs have a drain-source capacitance of several hundred picofarads. When this capacitance charges and discharges, energy is lost that results in power loss. Figure 2, shows a typical power switch configuration.

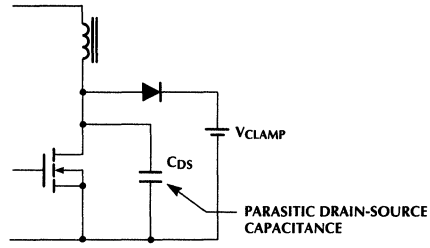


Figure 2. Typical switch stage of a switching power supply, with the parasitic drain-source capacitance shown explicitly.

The amount of power lost can be calculated by using the following formula

$$P = \frac{1}{2} C_{DS} V_{CLAMP}^2 f$$

As an example consider the following case C_{DS} = 500pF, V = 380 volts, f = 500KHz a circuit with these parameters results in a power loss of 18 watts. Therefore one can see the importance of capacitance C_{DS}.

In switching power supplies as we mentioned earlier it is often advantageous to use an external drain-source capacitance in the form of a snubber. This takes some of the burden of the switching loss from the switching device and puts it on the snubber circuits. The use of such capacitors further compounds the problem of capacitive discharge losses. If a way could be found to discharge the total drain-source capacitance non-dissipatedly then that would represent a solution to the problem. Figure 3, shows this concept, for the time being we are not going discuss the actual implementation of such a circuit. It is evident from the diagram that the switching loss can be reduced to zero if the voltage were also zero. From these diagrams it is evident that turn-on and turn-off power losses will be zero. Total switching times are in the order of 100nsec.

Zero Voltage Switching techniques represent such a solution. There are some limitations and shortcomings even to these techniques. When ZVS is accomplished through resonance of the voltage waveform then the design and analysis of such power supplies is more complicated. As a rule of thumb the operating drain currents are also higher than in PWM controlled power supplies.

To summarize, the ideal power supply would be the one that doesn't have operating frequency limitations because of switching losses, would be easy to design and manufacture and will be cost effective utilizing each one of its components to their fullest extent. In the next section we will discuss such a topology that has many of these desirable characteristics.

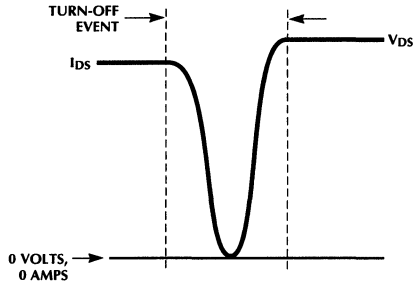


Figure 3a. Ideal turn-off waveforms of a ZVS switching element.

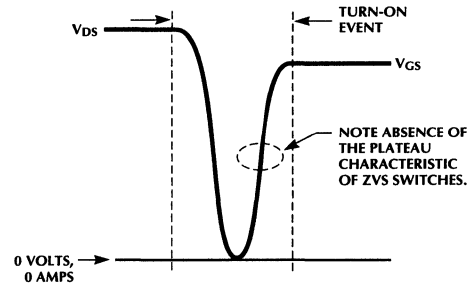


Figure 3b. Ideal turn-on waveforms of a ZVS switching element.

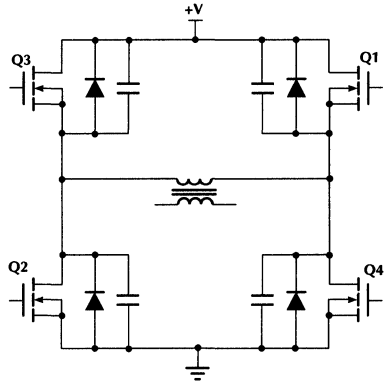


Figure 4. Typical H bridge power switch configuration as it is used in medium to high power switching power supplies.

PHASE MODULATED PWM TOPOLOGY (PMPT)

Phase modulated PWM Topology although not a panacea has many of the favorable characteristics mentioned above. It is a promising topology for medium to high power systems. Basically it is a full bridge topology with appropriately coordinated gate drive waveforms for each one of the MOSFETs in the H bridge. Its operating waveforms are very close to ideal. Turn-on and turn-off switching losses are almost eliminated. Operating drain currents are almost equivalent to those of a regular full bridge PWM topology, thus it does not require the use of expensive large die area MOSFET switches. The only difference is how the two topologies handle their respective switching events.

The analysis and design of the power circuit of the PMPT topology is identical to that of the classical PWM topology. Having said that, there are special set of considerations associated with the design of a high frequency high power transformer used in the PMPT.

The key idea behind the PMPT is that the voltage across the MOSFET is allowed to swing to "zero volts" just before the start of the next conduction cycle in the respective switches.

Figure 4, shows a typical H bridge configuration, the diodes and the capacitors across the MOSFETs are the intrinsic parasitic components present in these components. Typical values for the capacitors range anywhere from 100pF to 500pF for the larger devices. The reverse recovery time of the body diodes are in the range of 100nsec. In the figure snubber circuitry has not been shown.

The power switch section of the PMPT is identical to the one shown in Figure 4. To achieve PMPT operation the switches must be driven differently. In the regular PWM topology, gate drive is applied to the two diagonal switches based on the required duty cycle, then there is a period during which all switches are OFF (deadtime) and then gate drive is applied to the opposing diagonal switches.

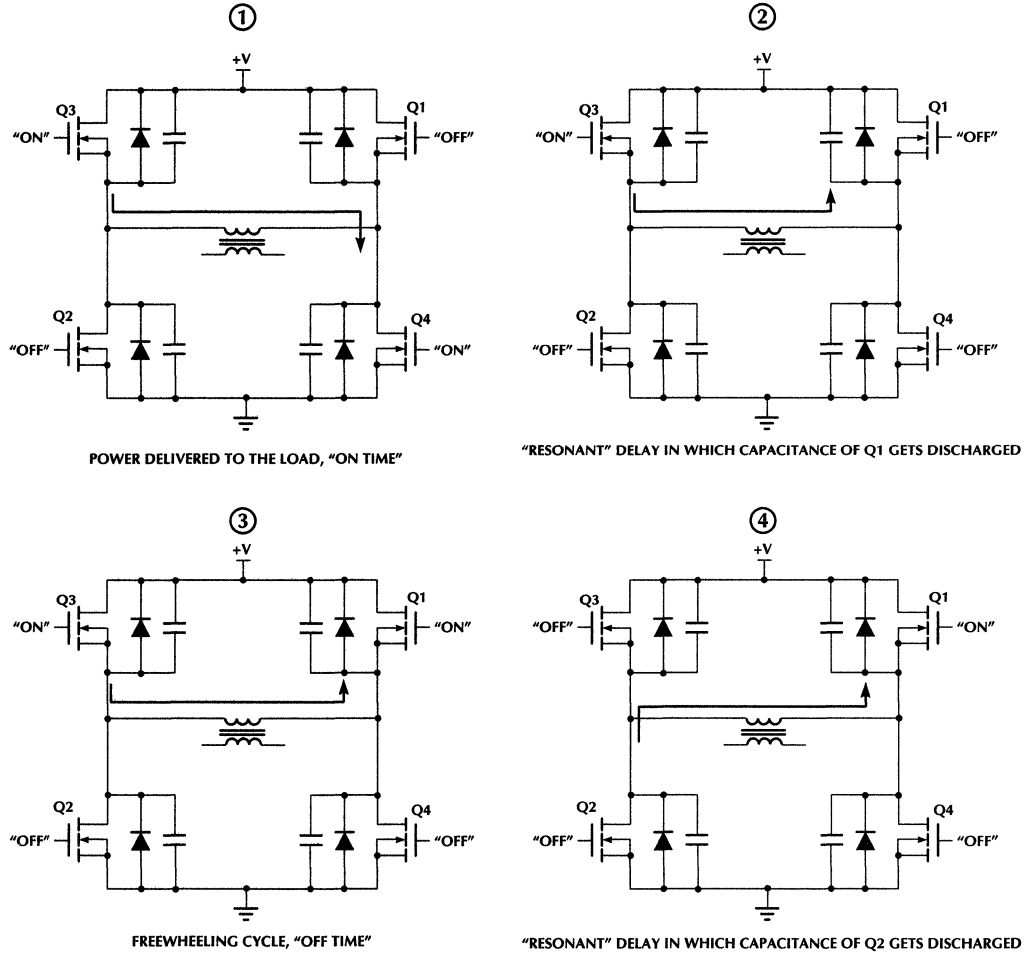


Figure 5a. PMPT power circuit cycles.

In the PMPT in order to accomplish ZVS, the leakage, and magnetizing inductances of the power transformer are utilized along with the drain-source capacitances of the power MOSFETs. The body diode of the MOSFETs also serves to clamp positive and negative going voltages. Thus the parasitic components of the MOSFETs are put to good use with this topology.

Sometimes in order to further reduce the turn-off losses additional capacitance may be necessary across the drain-source of each MOSFET.

The operation of the PMPT is best understood by examining one full cycle of events in the power circuit. For the time being one can assume that the power transformer magnetizing and leakage inductances will behave as current sources. Figures 5a and 5b show the power stage of the PMPT through one complete cycle.

1. The two diagonal MOSFETs are conducting, power is delivered through the transformer to the load. The primary load current is flowing through the leakage inductance of the transformer. The total primary current is equal to the load current plus the increasing magnetizing current of the transformer. The magnetizing current is of importance here since when the output load is very light there is very little reflected load current to complete the ZVS action.

2. Q4 turns off, the capacitance across Q1 was charged to +V when Q4 was ON with the turning OFF of Q4 the current through the transformer inductances starts to charge the drain-source capacitance of Q4 while at the same time discharges the capacitance of Q1. This action continues until the body diode of Q1 turns ON to clamp the voltage across Q1 to approximately –0.7V. The current through the transformer is sustained in the upper half of the power circuit as shown in the figure of phase (2).

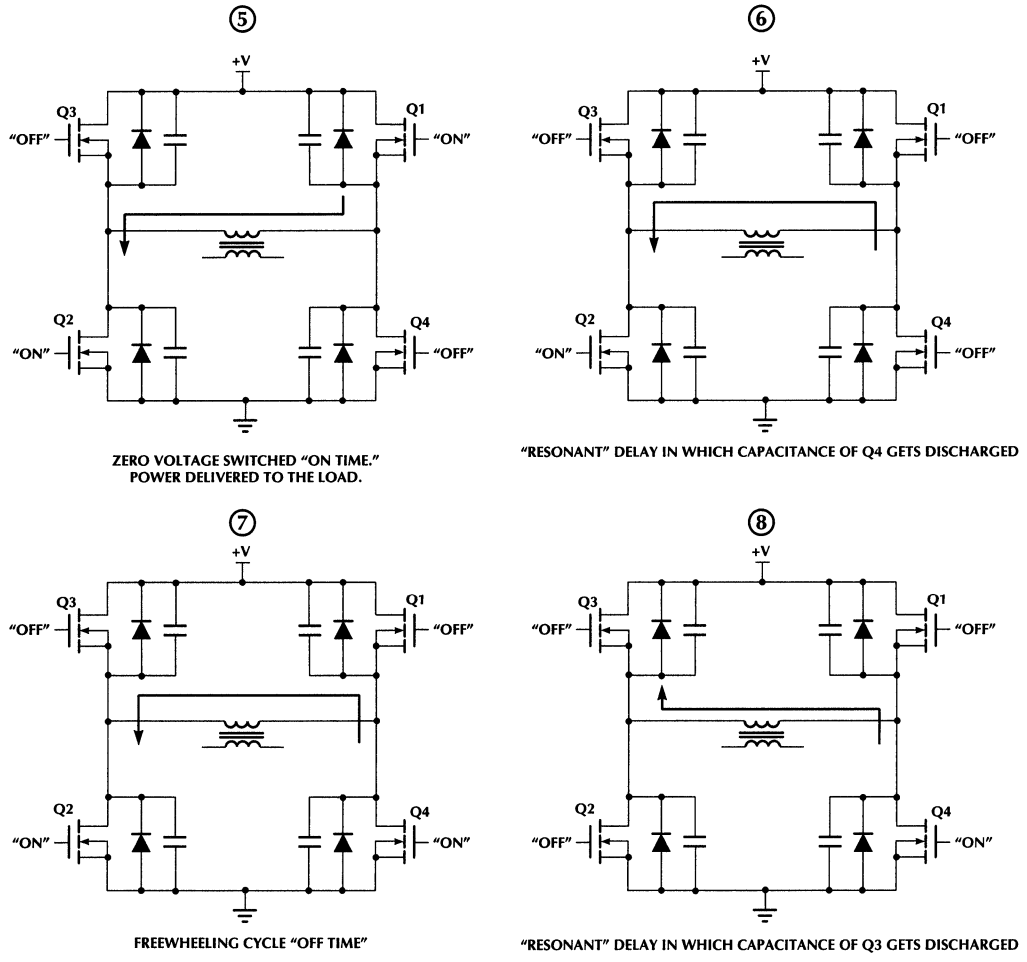


Figure 5b. PMPT power circuit cycles.

3. When the voltage across Q1 reaches approximately "0 volts" Q1 turns ON. The time that is required for the capacitance of Q4 and Q1 to reach the desired voltage is programmed as delays in the gate drive waveforms of the controller. This delay is programmable with an external resistor for complete flexibility. The current in this phase is circulating through the conduction channels of Q3 and Q1.

4. Q3 turns off, the transformer current now starts to charge and discharge the capacitances of Q3 and Q2 respectively. It requires again a finite amount of time for the drain voltage of Q2 to reach "0 volts" this time is consistent with the programmed delay at the outputs of the controller. It is the presence of this delay that makes ZVS possible. When the voltage across Q2 reaches "0 volts" then Q2 will be turned ON with no voltage across it. Thus accomplishing our goal of non-dissipative turn ON switching.

5. With the complete discharge of its drain source capacitance Q2 now is ready to turn ON. Power is delivered to the load through the conducting path of Q1 and Q2 for an amount of time that is determined by the control circuit. The product of this time, times two, times the operating frequency of the oscillator gives the duty cycle of the converter as in regular PWM converters.

$$\text{Duty Cycle} = 2t_{ON}f$$

Thus the calculation of output voltages or of the required transformer turns ratio becomes a task that is quite similar to that of the regular PWM converters. The difference is that in regular PWM converters the magnetizing inductance is maximized in order to get the minimum amount of magnetizing current. In the PMPT magnetizing current has to be at certain level to facilitate ZVS when the reflected load current to the primary is insufficient to do so. This magnetizing current adds to the reflected load

current thus requiring the use of a lower R_{DS} MOSFET. This is the penalty paid by using the PMPT. In any case the requirements are far less if conventional resonant technique were to be used.

6. Following the power transfer of the above diagonal pair, Q1 turns OFF. The voltage across Q4 starts to decrease, and when this voltage reaches "0 volts" the next phase starts.

7. In this phase Q4 turns on and the primary current circulates in the conduction channels of the lower pair.

8. Q2 turns OFF and the current starts to charge and discharge the capacitances of Q2 and Q3 respectively. When the voltage across Q3 has reached "0 volts" then Q3 turns ON non-dissipatedly and the complete cycle repeats itself from phase (1).

CONTROL CIRCUIT CONSIDERATIONS

The ML4818 PMPT controller has been designed to generate all the necessary timing and gate waveforms, and it contains logic circuitry for effective fault management that is of paramount importance in high power switching power supplies.

The control method involved instead of attempting to change the pulse width of the switches, changes the pulse width of the power pulse. Each of the switches operates under constant duty cycle that approaches 50%. In actuality the duty ratio is in the range of 40% to 45%. The remaining 5% to 10% of the time is being used for the ZVS action to take place. The above percentages may change with various operating frequencies. The effective maximum power pulse width can be much closer to 50%

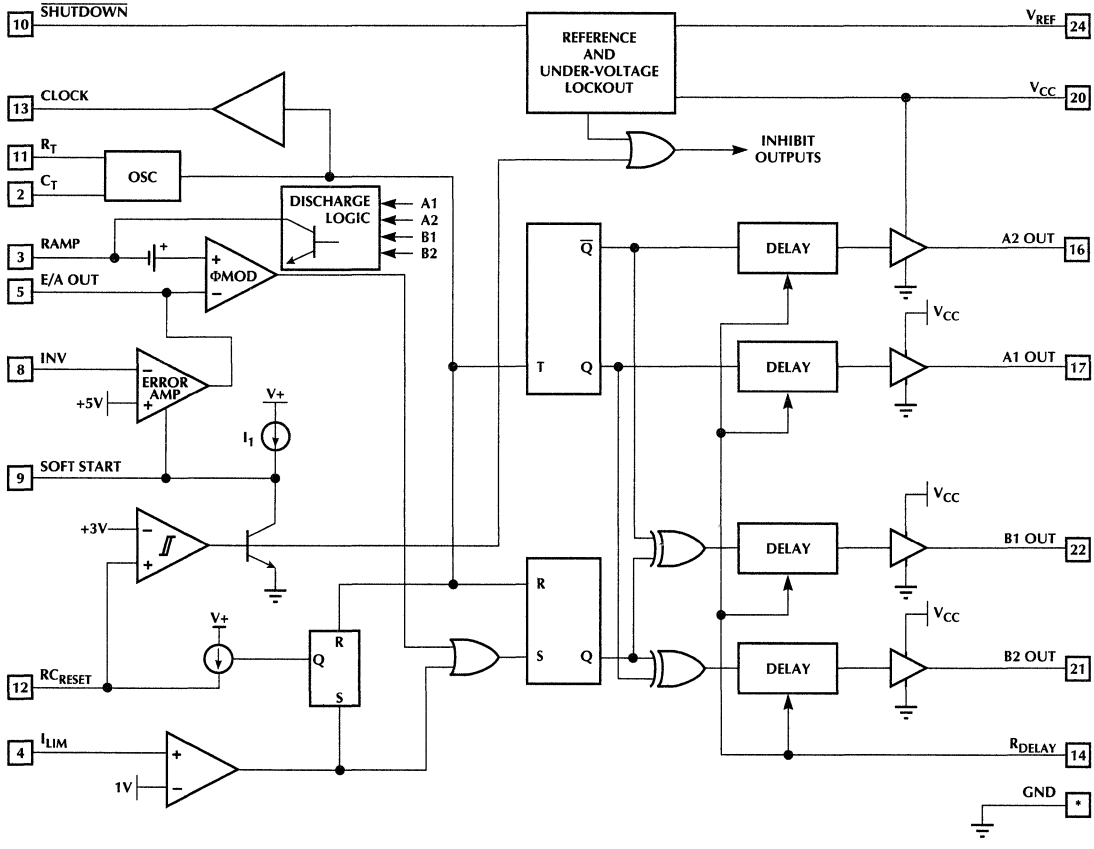


Figure 6. Functional Block diagram of the ML4818.

for optimum performance at lower frequencies (for example at 100KHz). A demonstration board is available from Micro Linear that operates at about 500KHz. Probing this board is a very good way of learning about the various operating modes of this very important class of PWM topologies.

Lets now discuss how phase modulation is accomplished. Earlier we mentioned that each of the four switches in the power bridge circuit has its own gate drive waveform. That requires four individual gate drive signals to be generated by the control circuit. This is exactly what the ML4818 does. The controller has four outputs that can directly drive the four MOSFETs. Figure 6 shows the internal block diagram of this controller.

In order to fully understand the control mechanism, we will look into the heart of the controller. Figure 7 shows the phase modulator core of the controller. All fault and supervisory circuitry has been left out. Also both of the complementary outputs and all driver and delay blocks have been left out for further simplicity. By examining how the other two outputs behave, one is able to grasp the basic operating principles of the phase modulator.

As can be seen from Figure 7, the core of the circuit is quite simple. Assuming that the two comparators are inactive for the time being the only stimulus that the circuit receives is from the clock pulse. Under this assumption the circuit reduces to the one shown in Figure 8.

From Figure 8, clearly if the set input of FFB is always logic "0" then the "Q" output of FFB will be reset or logic "0". From the operation of the exclusive OR gate then the "B" output will be equal to the inverted output of FFA i.e., outputs A and B will be 180 degrees out of phase from each other. Figure 9, shows the relevant waveforms.

If now we assume that a periodic stimulus is present at the set Input "S" of FFB occurring at some instance other than the clock pulse instance then the resulting waveforms will be different as is evident by examining Figures 8 and 9. The resulting timing diagram is shown in Figure 10.

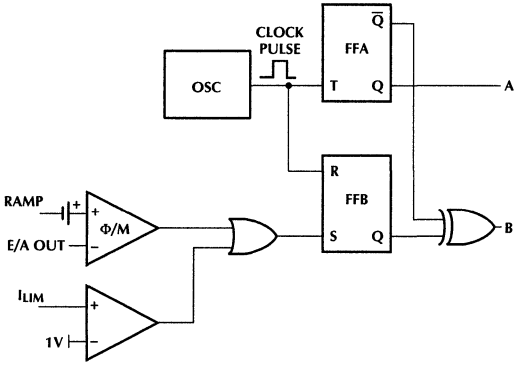


Figure 7. Phase modulator of the ML4818.

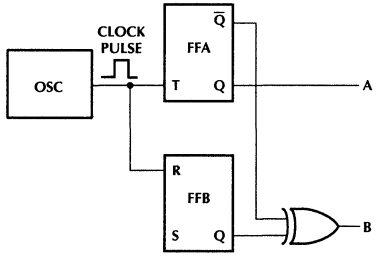


Figure 8. Phase modulator control logic.

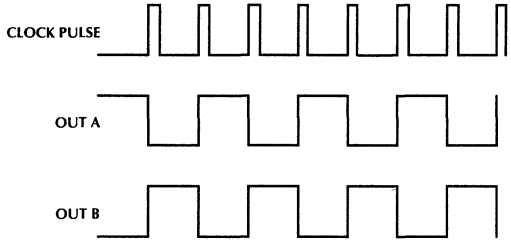


Figure 9. Timing waveforms of the basic phase modulator at the absence of stimulus other than the clock pulse.

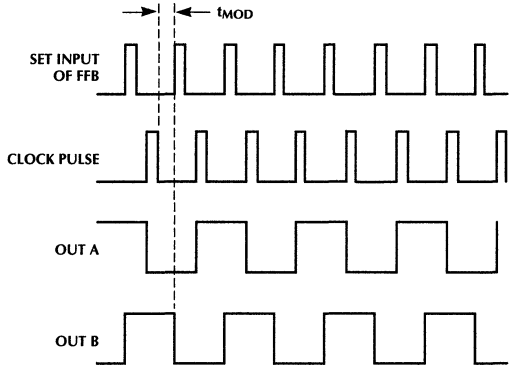


Figure 10. Resulting timing waveforms when there is a periodic stimulus at input "S" of FFB with period T equal to the period of the clock pulse.

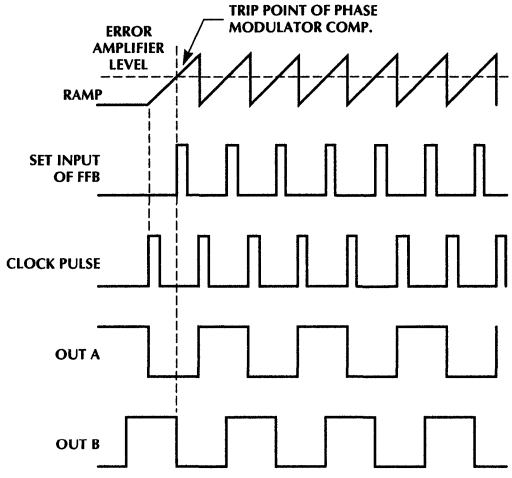


Figure 11. Generation of the set pulse for FFB. Ramp shape may be different in actual application.

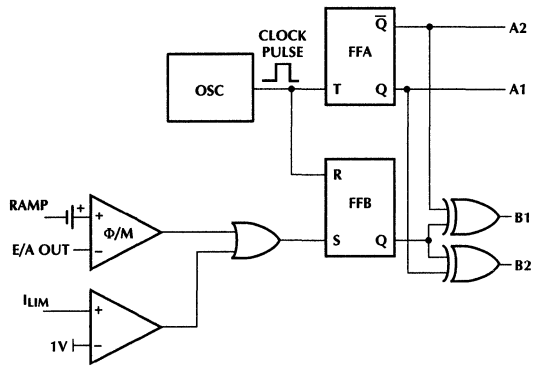


Figure 12. Complete logic diagram of the phase modulator with all four outputs shown.

Output "A" is free toggling whenever the clock pulse is present, whereas output "B" is the exclusive OR'ed output that is the result of outputs FFA, $\overline{Q}$ and FFB. The exclusive OR gate here functions as a controlled inverter. The other two outputs of Figure 6, behave in similar way with the only difference that they are 180 degrees out of phase with the ones described above.

By controlling time t_{MOD} then we are able to control the phase shift between outputs "A" and "B". The set input pulse for FFB is normally generated by either the phase modulator comparator of Figure 12, or by the current limit comparator. As in normal PWM regulators one input of the phase modulator comparator is the output of the error amplifier which sets the trip level and the other input is either a voltage ramp or the sensed primary (or secondary) current waveform of the power circuit. Figure 11, shows the generation of the set pulse and the resulting timing waveforms. When the output of the error amplifier changes then the trip level changes thus it is possible to continuously control time t_{MOD} by changing the trip level. In switching power supplies it is also necessary to limit the power pulse width whenever the primary load current exceeds certain predetermined value. The second comparator in Figure 7, serves that purpose. Thus the output of the phase comparator and of the current limit comparator are logic OR'ed to produce the set pulse for FFB. Figure 12, shows the complete logic diagram of the phase modulator with four outputs labeled A1, A2, B1, and B2 respectively.

The timing waveforms for all outputs can be derived from the above diagram. Figure 13, shows the relationship of the outputs with respect to each other.

DELAY OF THE GATE DRIVE WAVEFORM

So far we saw how controllable phase shifted outputs could be generated. We also saw that in order to have ZVS in the bridge circuit in the transition phase between conduction of the opposing legs, one of the MOSFETs is ON and the remaining are OFF. It is during this time that the drain source capacitance of the device next to turn ON is discharged to "zero volts". In the traditional H-bridge either two of the devices are ON or all of them are OFF.

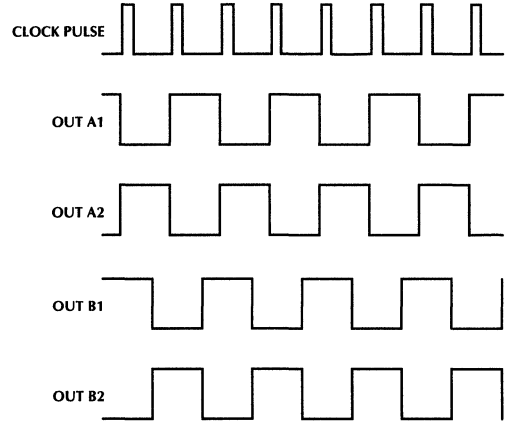


Figure 13. Timing diagram showing the waveform present on all four outputs of the phase controller.

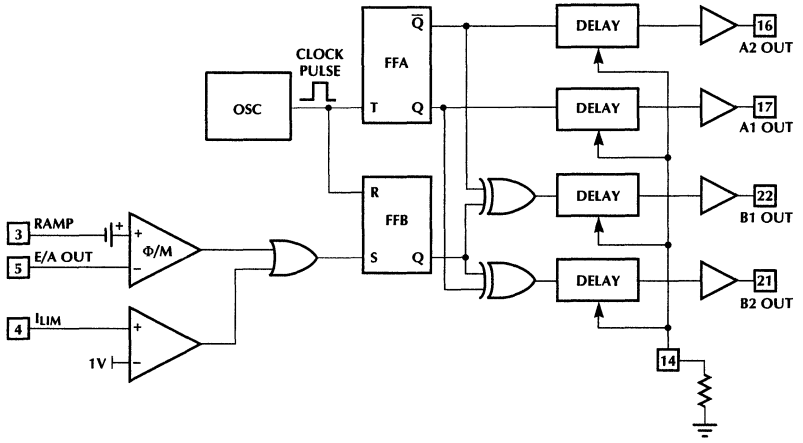


Figure 14. Phase modulator with delay and output driver blocks shown.

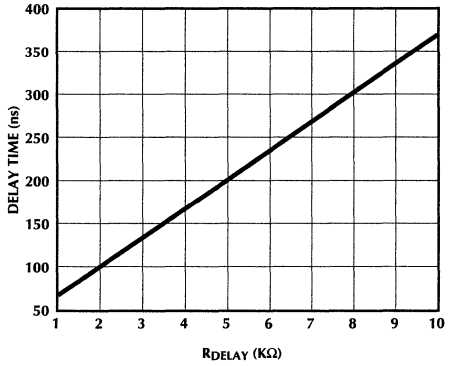


Figure 15. Chart for the determination of the external delay resistor.

In order to get this transition period it is necessary to modify the gate drive waveforms slightly. The modification consists of adding a predetermined amount of delay to the leading edge of the gate drive waveforms. Figure 14, shows the phase modulator along with the delay and output driver blocks. The delay blocks contain all the necessary electronics for the generation of the delay with the use of a single external resistor. The timing capacitor is integrated into the part. The value of the delay resistor R_{DELAY} can be found by using the chart of Figure 15, or it can be calculated by using the formula below

$$R_{DELAY} = \frac{DELAY(ns) - 33.34}{33.33} K\Omega$$

The individual gate drive waveforms are restricted to less than 50%. The resulting waveforms are shown in Figure 16. The shaded area in the leading edges shows the reduction in the pulse width. Note that the delays are only present at the leading edges of the waveforms. Hence the less than 50%

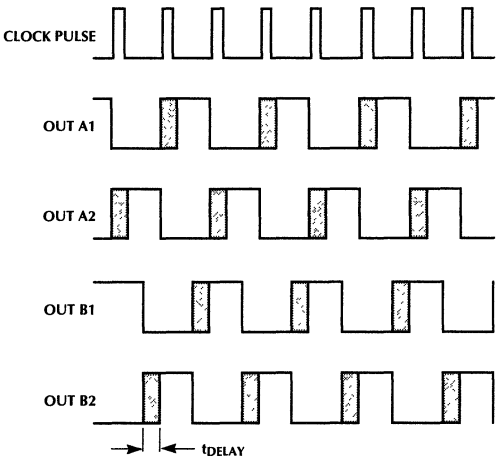
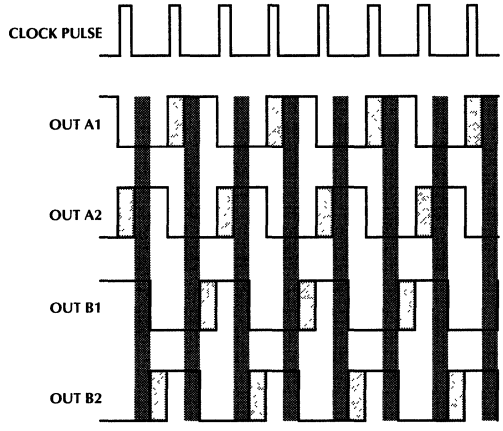


Figure 16. Leading edge delay of the drive waveforms necessary for ZVS operation.

duty cycle. Because all the drive signals have this delay complementary waveform symmetry is preserved. Although the delay time can be adjusted using an external resistor, it should be kept in mind that resulting actual delays in the power circuit may differ, this will be due to slew of the drive waveforms, also it requires a finite time to charge and discharge the gate capacitances of the MOSFETs.

The amount of time that is required to complete ZVS will vary as the load current reflected to the primary varies. The power transformer magnetizing inductance has to be able to develop enough current during "ON time" for ZVS to complete its cycle. That will require careful design of the power transformer. In most cases the transformer will have to be gapped. A side effect of the gapping will be the stabilization of the magnetizing inductance.

The idealized power transfer cycles of the PMPT are shown in Figure 17. Power transfer takes place during the hatched periods. The width of these periods depends on the phase relationship between the "A" and "B" outputs. A good way to observe the phase modulation action is watch the oscilloscope traces of "A1" and "B1" outputs.



Dark shaded areas denote times when power is transfered to the load. Light shaded areas denote the delay in the leading edge. Power is transfered to the load when (A1 = "1" & B1 = "1") and (A2 = "1" & B2 = "1").

Figure 17. Power transfer cycles of the PMPT.

DESIGNING FOR ZERO VOLTAGE SWITCHING

So far we saw that it is possible to do non-dissipative switching. The ML4818 power supply controller with its operational flexibility is able to provide all the necessary waveforms needed for such power supply. The most important thing left to be done is the design of the power transformer. Zero Voltage Switching properties greatly depend on this component.

Figure 18, shows the simplified equivalent model of a typical power transformer. The model is indeed very simple, actual transformers are very difficult to model due to the presence of primary and secondary effects such as saturation and inter-winding capacitances.

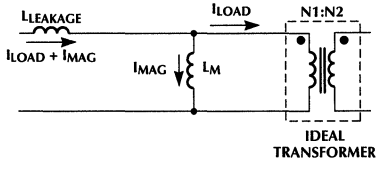


Figure 18. Simplified model of a real transformer.

It is obvious from Figure 18, that the current that will flow through the MOSFETs will be the sum of both the reflected secondary current which we call the load current and of the current that builds up in the magnetizing inductance of the transformer.

The load current is a function of the output load and can change anywhere from zero to its full rating as it reflects to the primary. The magnetizing current on the other hand is a function of the ON time and of the primary applied voltage. The output filter inductor where the load current flows through is normally very large. For all practical purposes the reflected current of the primary can be assumed constant during the intervals of interest.

$$I_{MAG} = \frac{V_{IN} t_{ON}}{L_M}$$

It is also important to remember that inductors can be approximated as current sources. With all this in mind lets now look into what happens when a power MOSFET switches OFF. Figure 19, shows one leg of the bridge circuit with the parasitic drain source capacitances. Assuming that the lower device was conducting current just prior to turning off the following events may happen.

If the gate drive waveform is fast enough and drops to zero volts before the drain source capacitance can charge to any significant voltage then the turn off event will be non-dissipative. This is the principle also with snubbers, where a large amount of external capacitance diverts the current from the channel for non-dissipative switching. Where the PMPT excels is that just before turn ON the energy stored in the snubber or drain source capacitances of the MOSFETs is returned back to the source as we saw earlier. This way there is not a penalty for using additional snubber capacitance. And since the turn ON is at zero voltage the switching event is lossless even at very high frequencies i.e., 500KHz and above.

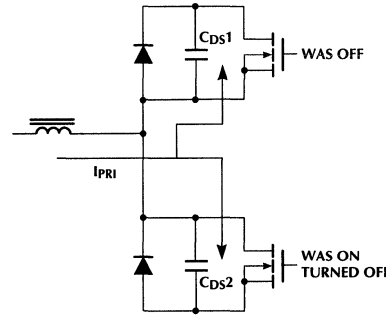


Figure 19. MOSFET switching in PMPT, and charge and discharge of the drain source capacitances.

In Figure 19, in order to discharge the drain source capacitances there needs to be a certain amount of current stored in the inductances of the transformer. Since the total charging current is the sum of the load currents and the magnetizing current, whenever the load current is low the charging has to be done by the current that the magnetizing inductance was charged. Hence the importance of the magnetizing inductance.

One can get quite complicated in trying to calculate the required amount magnetizing inductance necessary for ZVS. But the following simple procedure could be followed with some experimentation to get familiar with the technique.

The required maximum duty cycle is the first parameter to consider. Along with the delay that will be introduced by the delay circuit of the ML4818, in high frequency conversion the effective duty cycle will be reduced by the charging effect of the leakage inductance. Here we will assume that the reduction of the duty cycle by the charging of the leakage inductance is negligible (not true in most of the cases).

Lets assume that the required duty cycle results in a delay time t_D. In other words the time available to complete the charging of the drain source capacitance is t_D. *The charging configuration of the bridge circuit changes depending on its state just prior to ZVS. In Figure 19, the bridge circuit was delivering power to the secondary, so it was in a power transfer cycle just prior to the next ZVS. Under this condition the drain source capacitances will be charged linearly by a current equal to*

$$I_{PRI} = I_{LOAD} + I_{MAG}$$

This is not the worst case. The worst case happens after the above there is a period of freewheeling of the current before the next device turns ON with ZVS. This corresponds to phases (3) and (4) in Figure 5a. During this period the output diodes effectively short the transformer and the only inductance in the circuit is the leakage inductance and carries a current slightly less than at the end of the power transfer cycle. Therefore all the calculations are based on this case.

During phases (2) and (3) the capacitances charge linearly with the reflected load current. During phases (3) and (4) the capacitances resonate with the leakage inductance and charge in a resonant fashion. The worst case is when the load current is very close to zero. Under that condition the freewheeling current in the leakage inductance is equal to the magnetizing current at the end of the power transfer cycle.

The assumption we are going to make is that the delay time represents one quarter of the resonant cycle determined by the leakage inductance and twice the drain source capacitance of the MOSFETs, since there are two MOSFETs per side.

The procedure for calculating the necessary amount of the leakage and magnetizing inductances is shown below. An important note here is that in most of the cases the leakage inductance will be determined by the actual transformer construction and it will be a given. In that case the equation below could be used first to calculate the required amount of the delay time.

1. Calculate the required amount of either delay or leakage inductance value when one of them is the given value

$$\frac{1}{4t_D} = \frac{1}{T} = \frac{1}{2\pi\sqrt{2C_{DS}L_{LEAKAGE}}} \Rightarrow$$

$$L_{LEAKAGE} = \frac{2}{C_{DS}}\left(\frac{t_D}{\pi}\right)^2$$

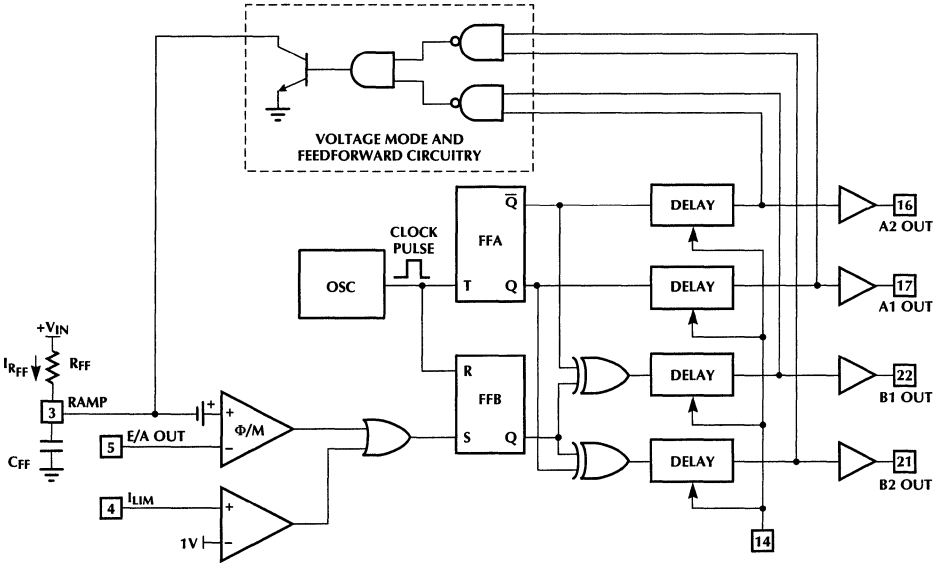


Figure 20. Voltage mode and feed-forward circuitry of the ML4818.

or

$$t_D = \pi\sqrt{\frac{C_{DS}L_{LEAKAGE}}{2}}$$

2. Calculate the minimum current for ZVS from the energy required to reach $V_{IN(MAX)}$. Note that twice the energy necessary to swing one leg of the bridge is required to be stored by the leakage inductance. This is because we have two ZVS actions during one complete power transfer cycle.

$$\frac{1}{2}L_{LEAKAGE}I^2_{MAG(min)} = 4\left(\frac{1}{2}C_{DS}V^2_{IN(max)}\right) \Rightarrow$$

$$L_{LEAKAGE}I^2_{MAG(min)} = 4C_{DS}V^2_{IN(max)} \Rightarrow$$

$$I_{MAG(min)} = \sqrt{\frac{4C_{DS}V^2_{IN(max)}}{L_{LEAKAGE}}}$$

3. Calculate the value of L_{MAG}.

$$L_{MAG} = \frac{V_{IN}t_{ON}}{I_{MAG(min)}}$$

Example: Lets suppose that the following are given

$$L_{LEAKAGE} = 15\mu H$$

$$C_{DS} = 225pF$$

$$V_{IN(max)} = 370Volts$$

$$t_{ON}\left(@V_{IN(max)}\right) = 1\mu sec$$

The calculations for the above example are as follows:

$$T_D = 3.14\sqrt{\frac{(225pF)(15\mu H)}{2}} = 129nsec$$

$$I_{MAG(min)} = \sqrt{\frac{4(225pF)(370V)^2}{15\mu H}} = 2.86A$$

$$L_{MAG} = \frac{(370V)(1\mu sec)}{2.86A} = 95.85\mu H$$

The value of the magnetizing inductance found above is somewhat low. This is because we made the assumption that there will be ZVS down to very light loads. If we do not allow the output load to go to very light loads or if we are willing to live with NZVS (Near Zero Voltage Switching) then the resulting magnetizing inductor values will be higher resulting in lower conduction losses. The value of magnetizing inductance that was chosen for the typical PMPT power supply of Figure 23, was 400µH, the value of the leakage inductance was approximately 15µH.

MORE ABOUT THE ML4818 CONTROLLER, VOLTAGE OR CURRENT MODE OPERATION

The ML4818 controller is able to control a PMPT converter operating either voltage mode or current mode. It contains special logic circuitry for that purpose. That same circuitry allows for voltage feed-forward in voltage mode operation. Figure 20, shows the logic circuit internal to the IC that enables the above.

Pin #3 is pulled to ground at the end of the power cycle and is kept at ground until the start of the next power transfer cycle. Thus the discharge of the feed-forward capacitor is enabled. An important note here is that the PMPT operating in voltage mode required the internal logic of Figure 20. It is not possible to operate voltage mode by only connecting pin #3 to the oscillator ramp. This is unlike conventional PWM regulators.

Feed-forward voltage mode operation provides automatic line correction without the need for the voltage control loop to change the duty cycle. The correction takes place within a single cycle. The current through resistor R_{FF} is proportional to input voltage therefore the charging time of the C_{FF} capacitor is proportional to input line voltage and consequently the time that it takes to reach the threshold set by the error amplifier.

$$I_{R_{FF}} = \frac{V_{IN}}{R_{FF}}$$

$$t_{ON} = \frac{V_{E/A}C_{FF}}{I_{R_{FF}}} = \frac{V_{E/A(max)}C_{FF}R_{FF}}{V_{IN(min)}}$$

The necessary values for any given application can be calculated using the above equations which can be solved for any of the unknown values. The resulting ramp will affect the open loop gain of the voltage control loop. The open loop gain will be independent of the variations in input voltage. The open loop gain for the voltage mode controlled case can be calculated by using the following.

$$G_{o.l.} = \frac{C_{FF}R_{FF}f_{OSC}}{N}$$

where N = Primary to secondary turns ratio

f_{OSC} = oscillator frequency

$G_{o.l.}$ = open loop voltage gain

For the circuit in Figure 23, the open loop voltage gain was calculated to be 7 or 16.9db, below the corner frequency of the output filter. In this case the corner frequency is 4.1KHz.

A TYPICAL PMPT POWER SUPPLY

Figure 23, shows a typical off-line PMPT supply, as it can be seen from the schematic diagram only a handful of components are required to build a fully functional power supply. Specifications for this supply are shown in Table 1.

The power supply was not optimized for any particular application. It is important to note that higher efficiencies

can be obtained by using lower loss magnetic materials and lower ON resistance MOSFETs.

The controller in this design is located at the primary side. The voltage feedback is accomplished with the use of an optocoupler. The current transfer ratio for this optocoupler is almost linear for a limited operating range, this enabled the use as it is shown in Figure 23. For more realistic applications an error amplifier at the secondary would probably be required. If an auxiliary supply is available then the controller itself can be situated in the secondary. Demonstration board that implements this power supply is available from Micro Linear Corp., it is a useful tool in gaining familiarity with this topology.

The control loop design for the voltage mode version of a PMPT supply is identical to that of a regular full bridge PWM converter. For simplicity in this case the loop is stabilized relying on the ESR of the output capacitor. The feedback components are calculated to give enough margin for loop stability.

The gate drive for the four MOSFETs is accomplished by using two drive transformers (T2 and T3). There are two secondary windings on each transformer to be able to drive the two MOSFETs in each leg of the bridge Figure 21, shows this configuration. The primary of the transformers connect to outputs A1, A2 and B1, B2 through a DC coupling capacitor to prevent drive core saturation under abnormal conditions. The windings of the transformers are trifilarly wound to minimize leakage inductances. A toroid of 0.5" outside diameter with 10 turns for each windings seem to function fairly well. The wires should be insulated to provide isolation.

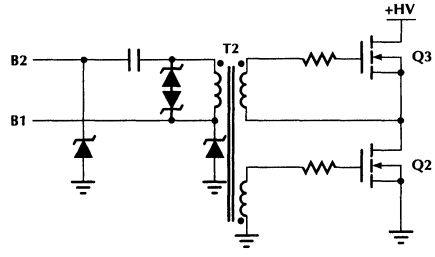


Figure 21. Gate drive scheme for fail-safe operation.

The power circuit consists of a DC blocking capacitor in series with the power transformer to prevent core saturation under unbalanced and abnormal conditions. The current transformer in series senses the current for cycle by cycle current limit. If the current limit persists then capacitor C8 charges to 3V triggering an internal comparator and shutting down the power supply. The resistor connected across C8 helps to discharge this capacitor and the power supply tries to soft start.

For high power applications where large size MOSFETs are used it may be necessary to use external gate drivers

Table 1.

Input Voltage Range	90VAC to 140VAC or 180VAC to 260VAC
Output Voltage	15V adjustable
Output Voltage Adjustment Range	12.6V to 20V (@ 120VAC and Iout=13A)
Output Current	13.3A
Line Regulation (90VAC to 140VAC)	<30mV
Load Regulation (10% to 100% @ 20VAC)	<300mV
Current limit set to approximately	15A
Output Power	200W
Efficiency at full load and 120VAC	82%
Output Voltage Ripple	250mV (without additional filtering)
Voltage ramp time at turn on (0V to 15V)	<8msec
Oscillator Frequency	500KHz
Average power under short circuit	<10W
Short Circuit Capability	Indefinite
Short Circuit Protection Method	Hiccups

Typical PMPT Power Supply Parts List

PART#	VALUE
Resistors	
R1, R2	240K, 1/4W
R3	82K, 2W
R4	39, 1/4W
R5, R20	1K, 1/4W
R9, R10, R11, R12	5.1, 1/4W
R6	4.3K, 1/4W
R7	240K, 1/4W
R8	7.5K, 1/4W
R13	510, 1/4W
R16	1K, 1/4W
R14	1K, 1/4W, POT
R15	100K, 1/4W
R17	330K, 1/4W
R19	100K, 1/4W
R21	5.1K, 1/4W
Capacitors	
C1, C2	680µF, 200V ELECTROLYTIC
C3	200µF, 25V, ELECTROLYTIC
C4	0.1µF, CER.
C5	680pF, PRECISION
C6	470pF, CER.
C7, C10, C15, C12, C16	1µF, CER
C8	56nF, CER
C9	0.33µF, 630V, POLYPROPYLENE
C11	100µF, 25V, ELECTROLYTIC
C14	0.01µF, 1KV, CER.
C18	1000pF, CER.
C20	220pF, CER.
C22	120pF, CER
C21	470pF, CER.
C23, C24	10nF, 1KV

PART#	VALUE
Diodes	
D1, D2	MUR150
D3, D4, D5, D6	1N5406, 3A, 600V
D9, D10, D11, D12	1N4148
D13	MBR3045PT, 30A, 45V, SCHOTTKY
D14, D15, D7, D8	1N5818, SCHOTTKY
D16, D17, D18, D19	1N5248, 18V ZENER
MOSFETs	
Q1, Q2, Q3, Q4	IRF840
IC's	
IC1	ML4818, PHASE-MOD. IC
OP1	MOC8102, OPTOCOUPLER
Inductors	
L1	200µH, 0.3A FILTER CHOKE
L2	15µH, LITZ WIRE, 15A FILTER CHOKE
Transformers	
T1	45T/2X4T/2X4T, Lmag = 400µH OBTAINED BY GAPPING, PRIMARY AND SECONDARIES ARE LITZ WIRE, Lleakage = 15µH, POT CORE, HIGH FREQUENCY MATERIAL
T2, T3	10T/10T/10T, GATE DRIVE TRANSFORMER, WOUND TRIFILAR ON 0.5" O.D. TOROID WITH INSULATED WIRE
T4	1T/80T, SAME CORE AS ABOVE, 80T IS AWG #28 MAGNET WIRE
Fuses	
F1	5A, 250V FUSE

to divert the power dissipation from the ML4818 controller to the external drivers. The drivers can be simple NPN-PNP pairs Figure 22, shows such a configuration.

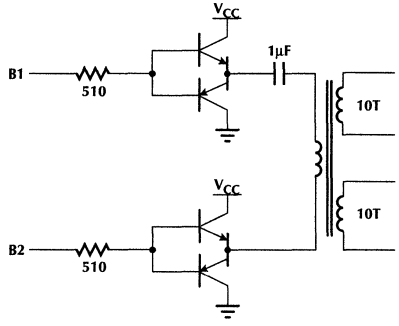


Figure 22. External gate drivers using NPN-PNP pairs.

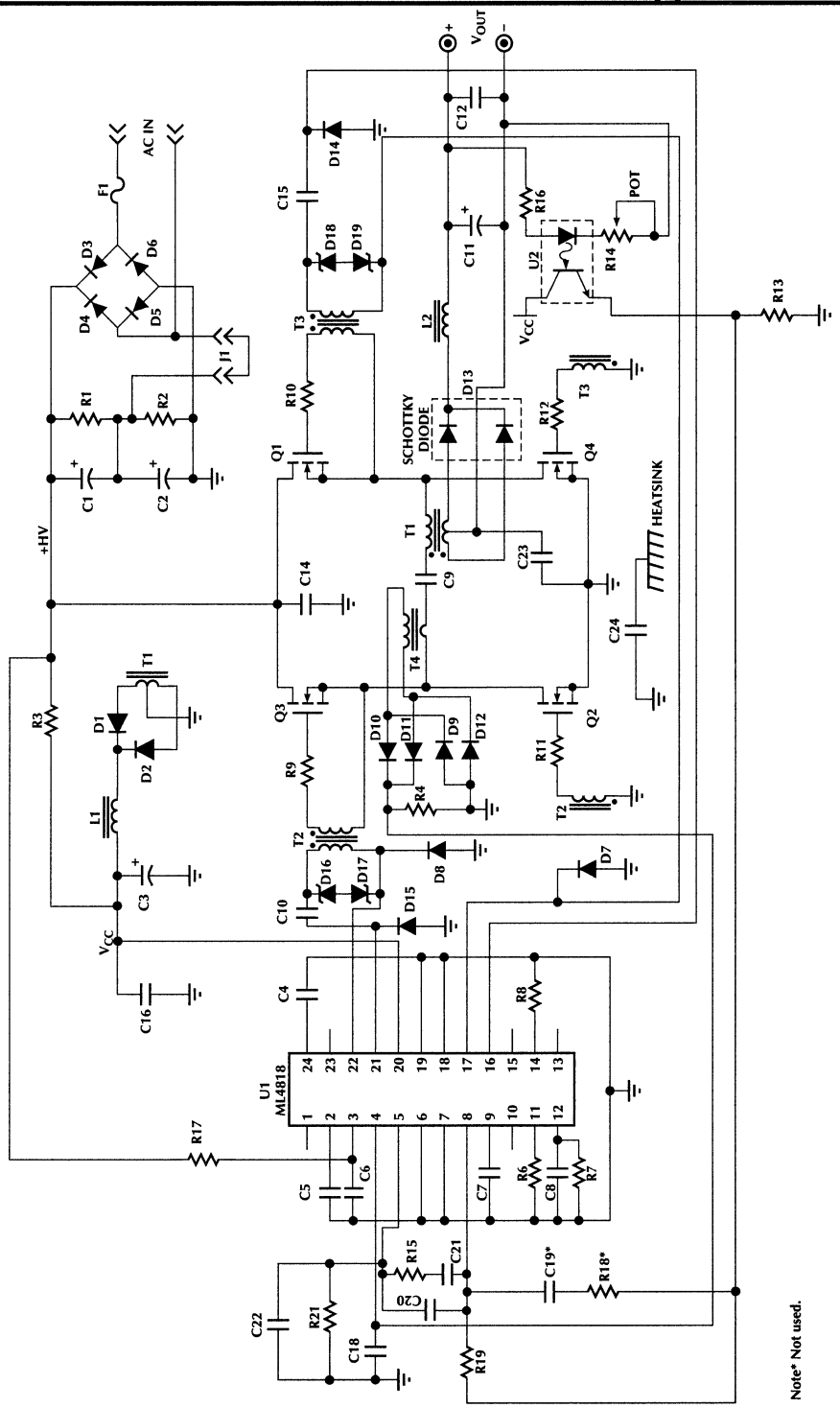


Figure 23. A typical voltage mode PMPT power supply.

Micro Linear

Application Note 20

Manijeh Fadaee

ML4642 AUI Multiplexer

I. THEORY OF OPERATION

The ML4642 AUI Multiplexer is 2:1 multiplexer. It is capable of connecting two stations (AUI interface) to a single AUI port. Additional ML4642 can be configured to allow the expansion of the number of stations (adapter cards or hubs) that can be multiplexed into the single AUI port.

The ML4642 allows an external Media Attachment Unit (MAU) to be shared by several stations. Jabber, Collision, SQE and Loop Back have been included in the multiplexer. For more detailed information refer to the ML4642 data sheet.

The following topics are discussed in this Application Note:

Section 1:Interconnecting 2 or More DTEs Without Using a MAU.

Section 2:Interconnecting 2 or More DTEs by Sharing One MAU.

Section 3:Transmission and Reception.

Section 4: Using the ML4642 in a HUB Application.

Section 5: How to Provide Power for Different Configurations.

Section 6: Advantages and features of the ML4642.

SECTION 1: INTERCONNECTING 2 OR MORE DTEs WITHOUT USING A MAU

We can categorize the ML4642 in 4 groups: 2 port MUX, type 0, type 1 and type 2.

2 port AUI MUX: The input ports are connected to stations directly and the output port is not connected.

TYPE 0: The input ports are connected to stations directly and the output port drives another ML4642.

TYPE 1: The input ports are driven by other ML4642s and the output port drives another ML4642.

TYPE 2: The input ports are driven by other ML4642s and the output port is not connected.

Two, Four and Eight port configurations are shown in Figures 2, 3 and 4. In configuring your system take the following matters into consideration:

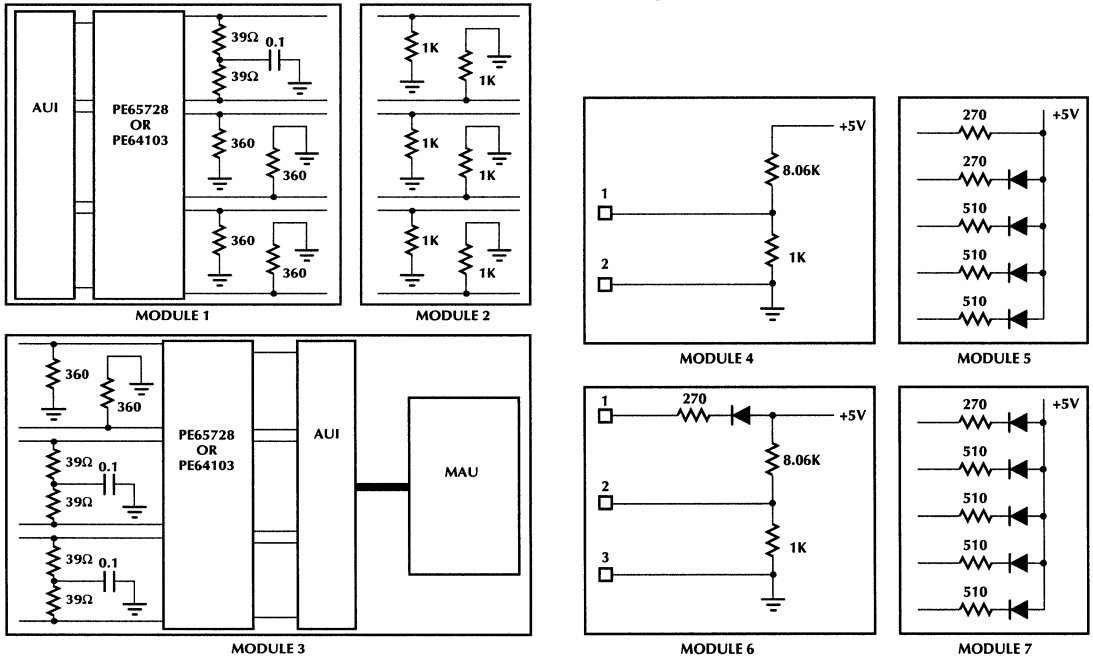


Figure 1.

Since channel 1 of the ML4642 has a higher priority, DTE with the higher priority should be connected to channel 1. Table 1 shows the order of priority of the DTEs for Figures 2, 3 and 4.

TABLE 1

FIGURES	STATIONS WITH THE ORDER OF PRIORITY
2, 5	S1 S2
3, 6	S1 S2 S3 S4
4, 7	S1 S2 S3 S4 S5 S6 S7 S8

RXLED/LPBK/SQE, pin 1 of the ML4642, implements 3 functions. This pin can be configured either as an input port to enable loopback and/or generate SQE, or as an output port to drive a LED. If none of these functions are needed, this pin must be pulled high by a 270 ohm pull up (+5V) resistor. Otherwise, 0.6V or ground should be applied to this pin.

Since in these configurations there is no MAU connected to the last ML4642, RXIN pair of the last ML4642 (2 ports AUI MUX or type 3) is not used, and there is no need to drive a LED. However loopback must be enabled by this pin. If the station requires SQE, tie this pin to the ground in the last ML4642 to enable loopback and SQE. If SQE is not needed, apply 0.6V to this pin in the last ML4642 to enable loopback. Since loopback and SQE are being taken care of by the last ML4642, pull this pin (pin 1) high in the other ML4642 as shown in figures 3 and 4.

JAB1/JDIS, pin 4 of the ML4642 serves two functions. It can be used as an input to disable the jabber, or it can be used as an output to drive a LED indicating jabber occurence at port 1. This pin (4) should drive a LED in the ML4642 connecting to a station directly (2 ports AUI MUX and type 0), and it should be tied to ground to disable jabber in the other ML4642. Disabling jabber in the other ML4642 prevents bringing the whole network down by shutting off the transmitter.

SECTION 2: INTERCONNECTING 2 OR MORE DTEs BY SHARING A MAU

Up to 8 DTEs or more can share one MAU or transceiver regardless of media by using the ML4642. As in section 1, there can be 4 groups of the ML4642: 2 port MUX, type 0, type 1 and type 2. Types 0 and 1 are exactly the same as section 1. The input ports in 2 port AUI MUX and type 2 are the same as section 1, but output port is connected to a MAU.

Two, Four and Eight port configurations are shown in Figures 5, 6 and 7. In configuring your system take the following matters into consideration:

Priority of DTEs must be set as explained in the previous section.

Since the last ML4642 is connected to a MAU, MAU generates the SQE, implements the loopback and drives the RXIN pair of the last ML4642. This results in driving a LED by this pin at the last ML4642 and pulling it high in the other ML4642s as shown in figures 6 and 7.

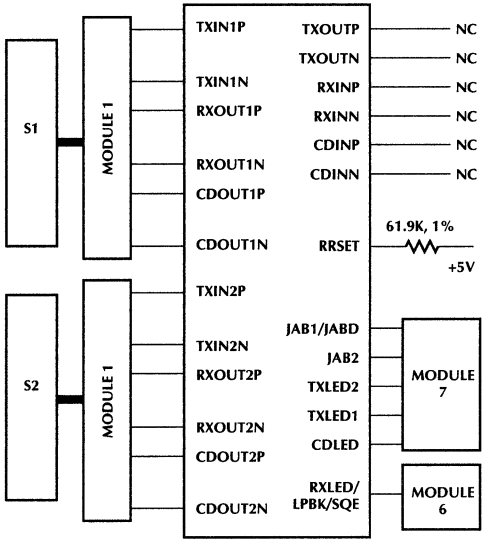


Figure 2. Two Port AUI Multiplexer without a MAU.

SECTION 3: TRANSMISSION AND RECEPTION

Transmission takes the place when one DTE starts to transmit data on one channel of the ML4642. The data will be transmitted out through TXOUT differential pair to the next ML4642 up to the last ML4642. If there is no MAU connected to the last ML4642, data will be looped back by the last ML4642 into the receive output pair (RXOUTP and RXOUTN). If there is a MAU connected to the last ML4642, data will be looped back by the MAU, and it will transmit out through the media to the other side of network. In either case data will eventually be received by every port through RXINP and RXINN. Based on the destination address of the transmitted data, data will be copied by one DTE and will be ignored by other DTEs.

SECTION 4: USING ML4642 IN THE HUB APPLICATION

Figures 8 and 9 show how an 8 port multiplexer can replace an 8 port hub. Since the last ML4642 is connected to the hub through a MAU, the RXLED/LPBK/SQE pin should be set as follows:

Since a MAU is connected to the last ML4642, loopback and/or SQE can be controlled by the MAU. If loopback and SQE are enabled by the MAU, you can drive an LED with this pin (1). Otherwise, apply 0.6V or ground to this pin to control loopback and SQE by the last ML4642.

Having all three choices available at pin 1 of the last ML4642 as shown in Figures 5, 6 and 7. This gives you flexibility to use any MAU since it does not have to support loopback and SQE. This pin should be pulled high by a 270Ω pull up (+5V) resistor on the other ML4642s.

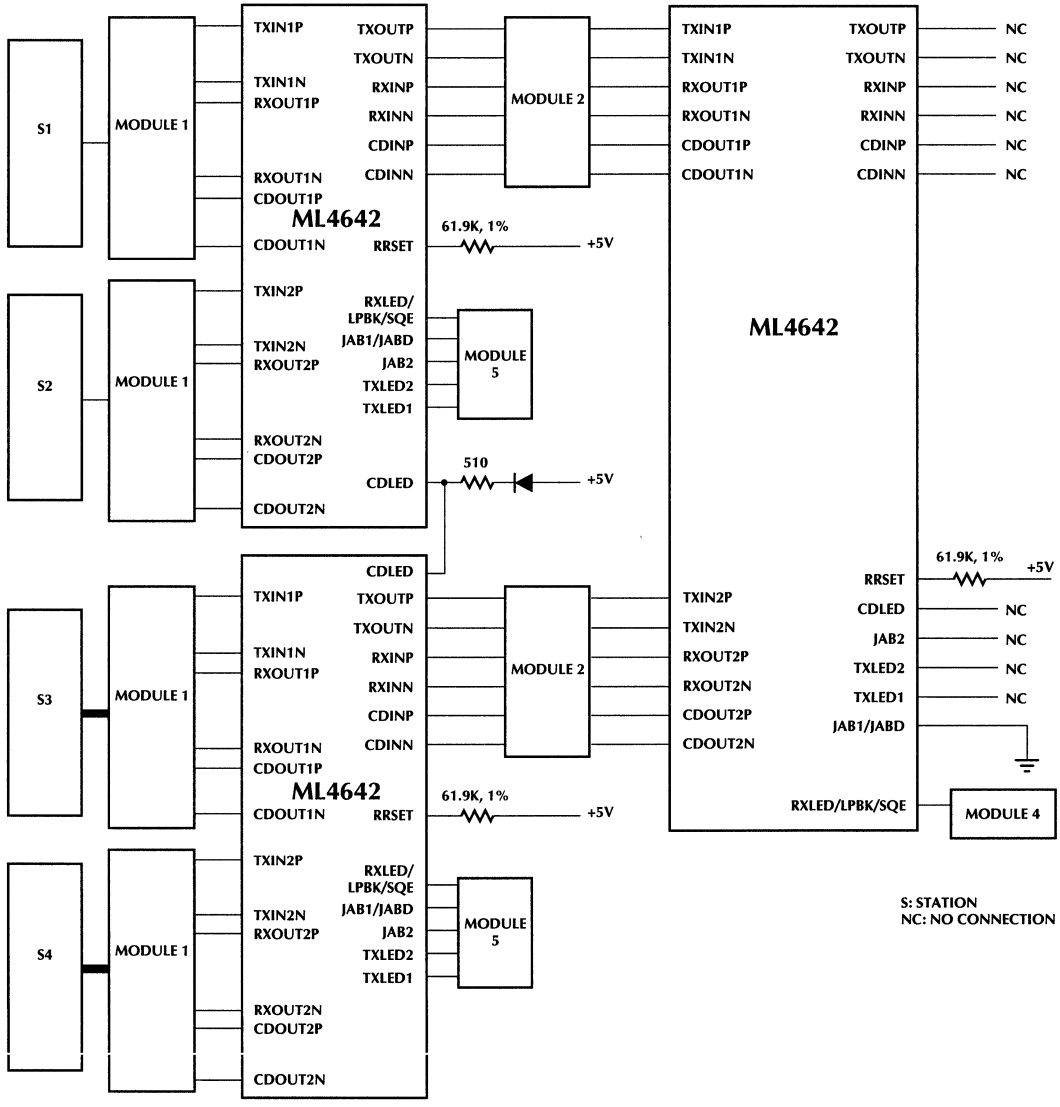


Figure 3. 4 Port AUI Multiplexer without a MAU.

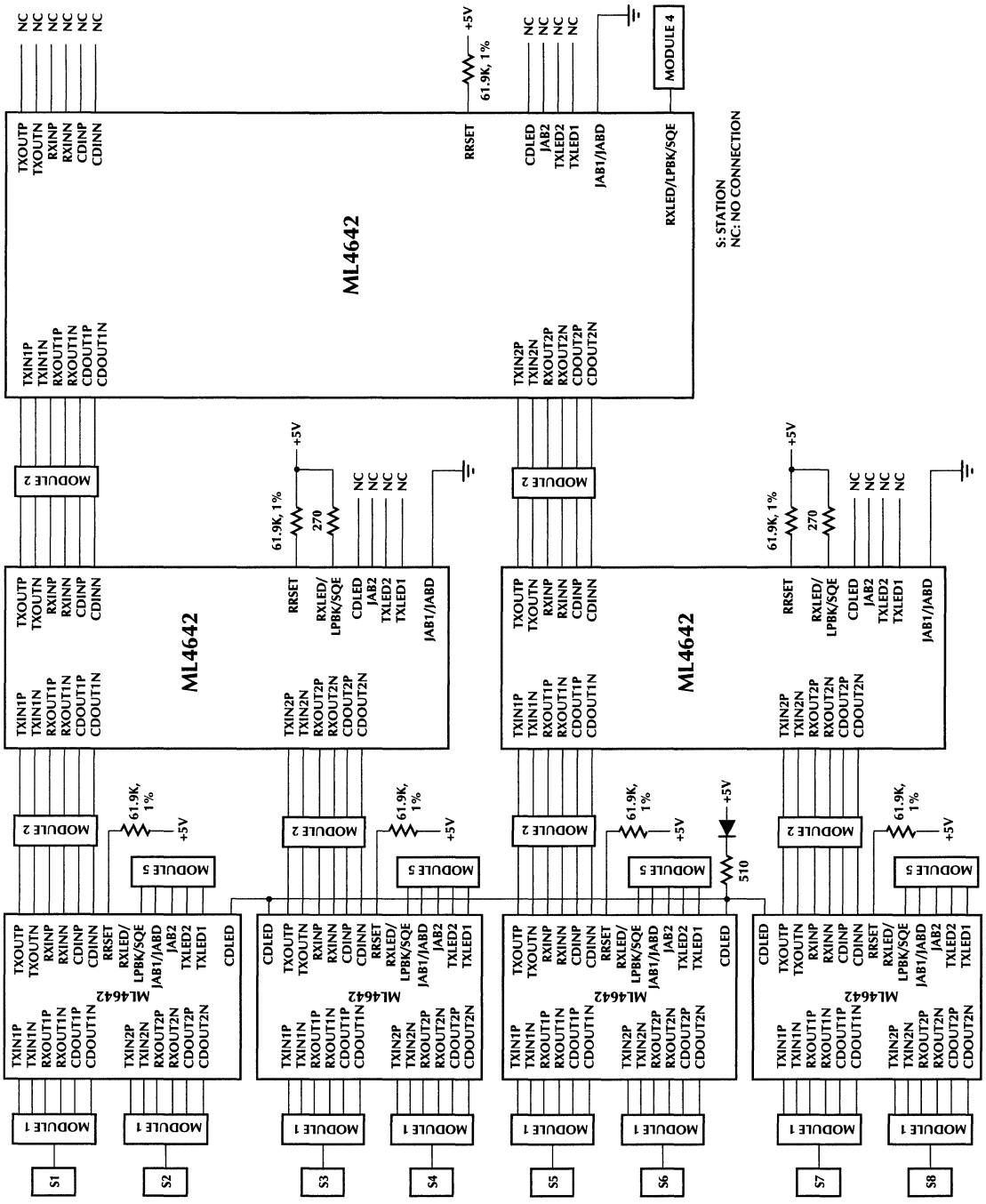


Figure 4. 8 Port AUI Multiplexer without a MAU.

SECTION 5: HOW TO PROVIDE POWER FOR DIFFERENT CONFIGURATIONS

AUI input ports provide power to the board and the MAU if there is one being used. One of the AUI input ports is used to provide +12V to the external MAU through an AUI output port. The other AUI input ports are used to supply power to the board after converting +12V to +5V. To meet the standard we want to make sure to not draw more than 500mA out of each AUI port. Depending on how many input ports are available and how much current the board consumes, different number of AUI input ports should be used to supply the power. power consumption for the board can be calculated as follows:

1) ICC_{MAX} for each ML4642 is 90mA. However this does not include the current from LED output pins or the pull down resistors at RXOUT, CDOUT and TXOUT pairs.

2) Since different value of pull down resistors are used for each type of ML4642, the current for each type should be calculated as follow:

—Type 0:

VOH = 4.1V
I(RXOUT) = I(CDOUT) = $2^{(1)}$ (4.1V/360Ω) = 22.8mA
I(TXOUT) = 2 (4.1V / 2K $^{(2)}$) = 4.1mA

—Type 1:

VOH = 4.1V
I(RXOUT) = I(CDOUT) = I(TXOUT) =
2(4.1V/2k) = 4.1mA

—Type 2:

VOH = 4.1V
I(RXOUT) = I(CDOUT) = 2 (4.1V/2k) = 4.1mA
I(TXOUT) = 2 (4.1V/360Ω) = 22.8mA

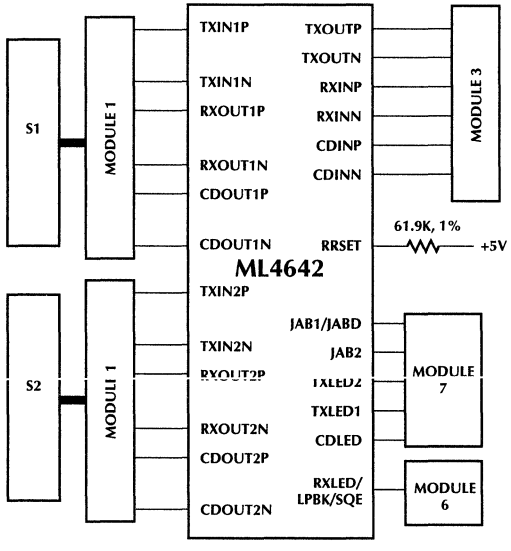


Figure 5. 2 Port AUI Multiplexer Sharing One MAU.

3) The current for the LEDs should be added.

4) At this step you should add all the above current to find out how many AUI ports must be used to supply the current without violating the AUI standard.

5) Tie pin 13 (Ground) coming from all the AUI input ports and the AUI output port together to provide a common Ground between the board, stations and the MAU. The following example shows you all the steps should be taken to supply power to the board and an external MAU.

EXAMPLE: Figure 10 shows the block diagram of a 8 port AUI Multiplexer sharing an external MAU. Power consumption can be calculated as follows:

1) ICC_{MAX} = 90mA for each ML4642.

2) Since MUX 1, 4, 5 and 7 are type 0, the current for each of them will be:

90mA + (22.8mA x 4$^{(3)}$) + 4.1mA$^{(4)}$ = 185.3mA

Current for MUX 2 and 6 which are type 1, will be:

90mA + (4.1mA x 4) + 4.1mA = 110.5mA

Current for MUX 3 which is type 2, will be:

90mA + (4.1mA x 4) + 22.8mA = 129.2mA

3) Figure 7 shows you all the LED status which can be driven by the output LEDs of the ML4642 for different type. If the MUX is type 0, 6 status LEDs can be driven by the LED outputs. The maximum number of LEDs being on at the same time is 6. If each LED draws 10mA, current for the output LEDs will be:

10mA x 6 = 60mA for the worst case

If MUX is type 1, no status LED needs to be driven, If MUX is type 2, one status LED (RXLED) can be driven as shown in figure 7. However if RXLED is driven by this pin, there is no need to drive RXLED at type 0. so current for this output LED which is 10mA, has already been covered by type 0.

4) Now we can calculate the total current consumes by each type of MUX.

Type 0: 185.3mA + 60mA = 245.3mA

Type 1: 110.5mA

Type 2: 129.2mA$^{(5)}$

This means one AUI can drive MUX 1, 2 and 3 or MUX 5, 6 and 7 with total current of 485mA (245.3 + 110.5 + 129.2). Therefore station 1 is capable of driving 3 MUX, station 5 can drive 2 other MUX (5 and 6), and station 3 can drive MUX 4 as shown in figure 10. Now we can use another station like 2 to drive the external MAU by supplying +12V to the AUI output port.

5) Tie pin 13 of all the AUI input ports together to have a common ground.

SECTION 6: ADVANTAGES AND FEATURES OF THE ML4642

— Since both input ports interface through AUI to a station, power to the chip and board can be provided by the AUI. This eliminates having external power supply. Using more than one AUI to provide power to the board in multi port MUX, guaranties not exceeding the current limit on the AUI interface (0.5Amp).

— An AUI MUX can be used in different networks regardless of media (coax, fiber, twisted pair).

— Using a multi port MUX, reduces cost by saving a MAU for each station. In addition it can minimize the number of hubs needed in a network as explained in section 4.

— Sharing a MAU between stations through a multi port MUX, reduces cable run.

— Using multi port MUX to communicate between stations and hubs, reduces network size by decreasing the number of HUBS and MAUs.

— Easy to use and design in different configurations.

— Because of the delay time from input to the output pairs, it might restrict the topology of the network for the worst case conditions.

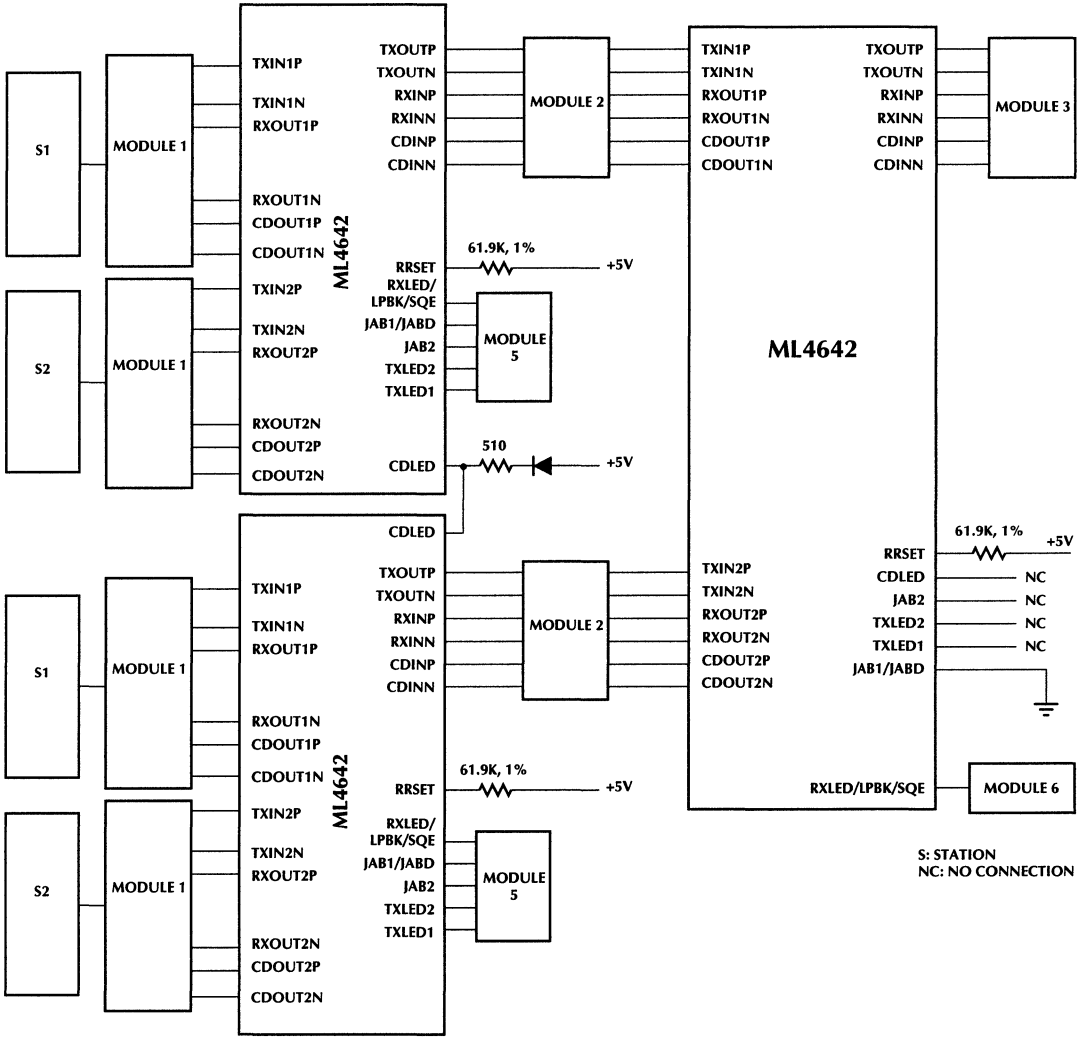


Figure 6. 4 Port AUI Multiplexer Sharing One MAU.

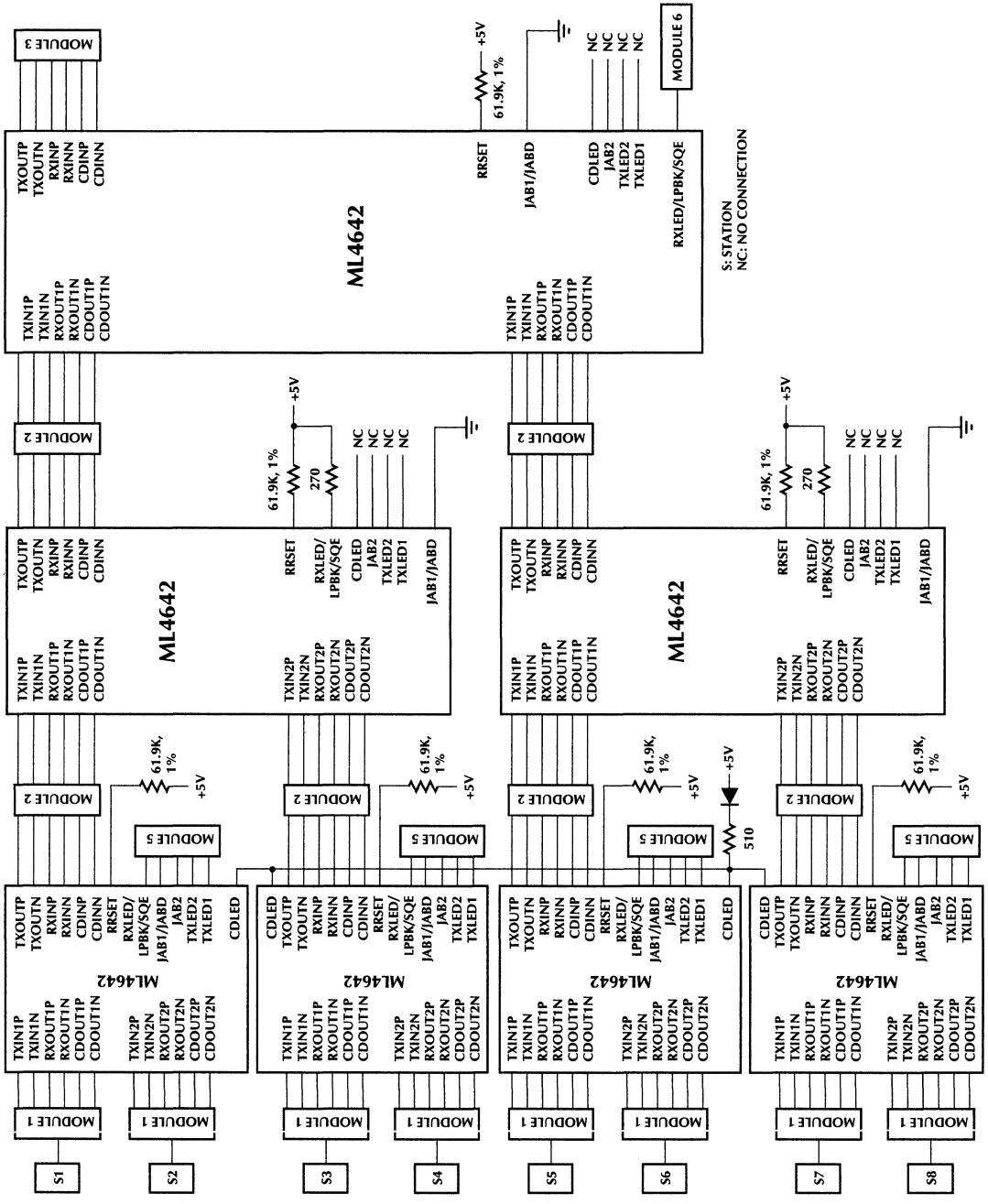


Figure 7. 8 Port AUI Multiplexer Sharing One MAU.

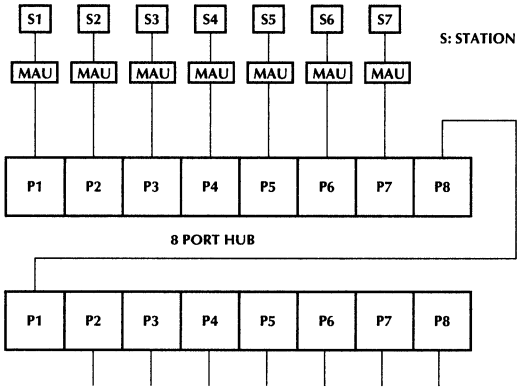


Figure 8. 8 Port Hubs without ML4642 (AUI Multiplexer).

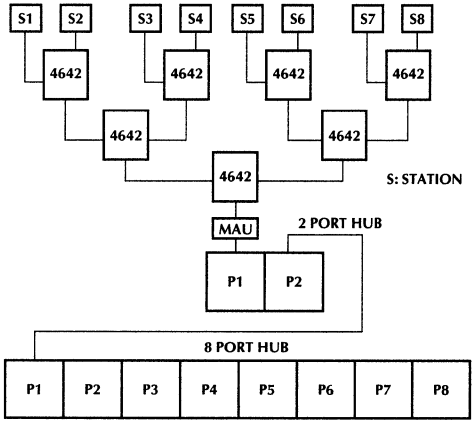


Figure 9. Using ML4642 in Hub Application.

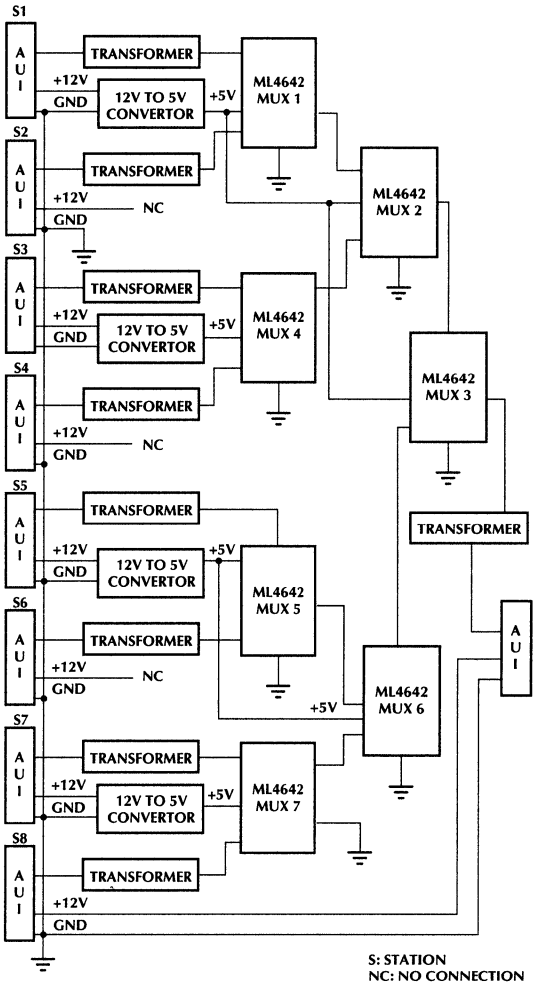


Figure 10.

1 Since each pair is a differential output, we must multiply it by 2

2 Using a 2k pulldown resistor instead of a 1k at RXOUT or CDOUT or TXOUT pairs decreases the current.

3 Includes current at the RXOUT and the CDOUT pairs for ports 1 and 2 of the ML4642.

4 Current at the TXOUT pair of the ML4642.

5 If there is a RXLED at this MUX, then there is no RXLED at type 0 MUX This means current for type 0 will be 235.3mA (185.3mA + 50mA) and current for type 2 will be 139 2mA (129.2mA + 10mA).

High-Speed Clock System Design with the ML6500 PACMan Programmable Adaptive Clock Manager

Ram Gopalan
Ken McBride

INTRODUCTION

Clock distribution is a significant design problem for systems operating above 10MHz. The PACMan Programmable Adaptive Clock Manager series of clock chips simplifies this design problem by significantly reducing clock skew, the source of most problems in high-speed clock distribution design. This application note examines the various aspects of clock system design using a system example.

Figure 1 shows an example of such a high-speed system with a clock subsystem. The system consists of a 64-bit CPU with a memory control subsystem, peripheral chips and a clock subsystem. The clock subsystem drives the various clock pins of the system. The clock subsystem consists of a crystal oscillator, XTAL OSC, a ML6500 PACMan master clock driver and a ML6508 PACMan slave clock driver. The ML6500 generates the primary clock signal and drives some of the system clock pins. The ML6508 generates copies of the clock from the ML6500 and drives the remainder of the system clock pins.

HIGH-SPEED CLOCK SYSTEM DESIGN

Synchronous digital systems — such as the one in Figure 1 — use the concept of a single clock coordinating the actions of all system components. In real systems, the low-to-high, controlling clock edges do not happen at the same time. The difference in time between the rising edge of one clock pin and another is called clock skew. Clock skew is generated by differences in delay between the clock synthesizer and the clock loads. This delay is a combination of the delay through different clock drivers and the time required for the clock to propagate down the PC board trace, or trace delay, and the time to slew the clock capacitive load.

The PACMan clock system minimizes clock skew. The PACMan generates multiple clock outputs where the low to high transitions of these clocks occur at the same time at the load. It does this by sensing each clock output, comparing it to a reference signal, and adjusting the clock output timing to make it occur at the same time as the reference signal.

HOW THE ML6500 WORKS

The ML6500 PACMan chip consists of a Phase Locked Loop (PLL) frequency synthesizer, a reference delay and output buffers with deskewing logic, as shown in the block diagram of Figure 2.

The PLL frequency synthesizer generates an internal clock, VCO output, from the reference clock or crystal oscillator input. The M and N registers set the VCO output frequency to a multiple of the input reference frequency. The PLL causes the VCO output frequency to be the reference frequency times (M/N). The M and N registers set the count values for the M and N counters, respectively. The M counter divides the reference input frequency by the contents of M, and the N counter divides the VCO output frequency by the contents of N. The PLL changes the frequency of the VCO output (Voltage Controlled Oscillator) in the direction that will cause the rising edges of its inputs — the outputs of M and N

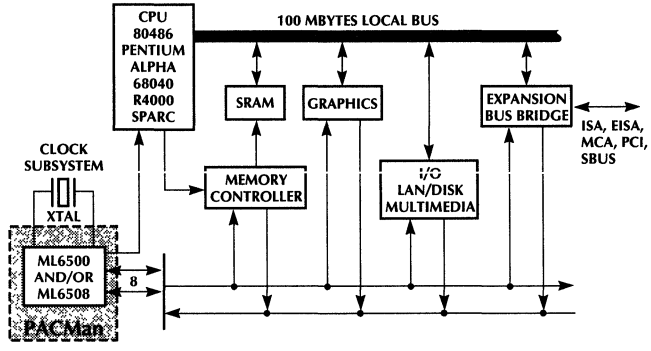


Figure 1. A 64-bit Microprocessor System

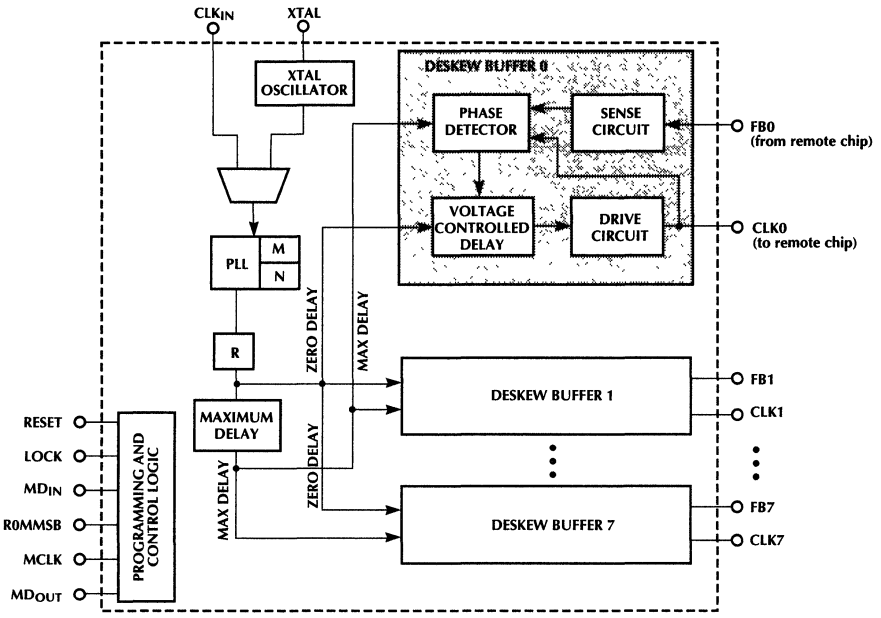


Figure 2. ML6500 Master Clock Chip Block Diagram

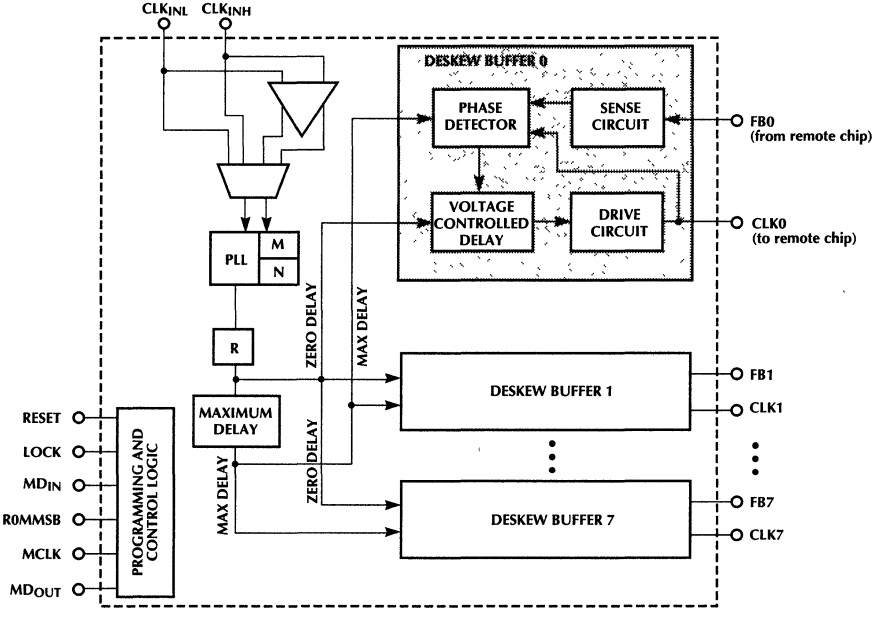


Figure 3. ML6508 Slave Clock Chip Block Diagram

programmable counters — to be aligned. The PLL increases or decreases the VCO output frequency until the VCO output frequency divided by N is exactly phase locked to the X1 input frequency divided by M. The VCO output is then reference frequency times (N/M).

The R counter divides the VCO output by 2, 4 or 8, as determined by the chip programming of the R register. Divide by 2 is the default value. The R counter is used to keep the VCO in its specified operating range of 80 to 160MHz. The output of the R counter is the VCO signal used by the deskew buffers.

The deskew buffers receive VCO output as an early version of the output clock. REF CLOCK is a delayed version of VCO output and is generated by passing VCO output through the Reference Delay. The deskew buffers cause the rising edges of their outputs to line up with the rising edge of REF CLOCK.

The ML6500 has eight clock outputs: CLK0 through CLK7. Two of these outputs, CLK6 and CLK7, may be delayed if so programmed. When programmed CLK6 is delayed by approximately 2ns relative to the other outputs. This delay is achieved by delaying REF signal to their deskew buffers by 2ns. When programmed CLK7 can be phase shifted by 180° relative to the other outputs. These delays occur at the load.

ML6508 SLAVE CHIPS FOR EXPANSION

The ML6508 PACMan Slave clock chip provides additional clock signals which are edge aligned with the ML6500 outputs for zero skew. Figure 3 shows a block diagram of the ML6508. The ML6508 is similar to the ML6500 except that it allows for a positive ECL, PECL input reference. The PLL receives a reference clock signal from one of the ML6500 clock outputs or from the small-swing differential reference outputs. The PLL causes the internal REF output to be aligned with the clock input. The ML6508 clock outputs are therefore aligned with the clock input, which is also the ML6500 clock output. The ML6508 outputs have the same phase as the other ML6500 clock signals. The ML6508 allows clock signals to be duplicated without introducing skew. As a result, you can design large clock systems with near zero skew.

SYSTEM CLOCK SKEW REQUIREMENTS

Clock skew is the main design parameter in high-speed clock systems. System timing determines clock skew requirements. The system timing diagram of Figure 4 shows the effect of clock skew. In this diagram, we have a data source such as the CPU driving a receiver such as an I/O device. The CPU puts data on the bus to be received and clocked in by the I/O device. The CPU makes the data valid on the bus for a set-up time, t_{BS}, before the clock. The CPU holds it valid for a hold time, t_{BH}, after the clock. The I/O device requires that data be present at its inputs for a set-up time, t_{IS}, before the clock, and that it be held valid for a hold time, t_{IH}, after the clock. The system timing design margin is the amount of excess time data is valid before the minimum required set-up time and after the minimum required hold time, beyond the minimum requirements. The design margin for data set-up is ($t_{BS} - t_{IS}$); for data hold, it is ($t_{BH} - t_{IH}$).

Let us consider the case where the I/O device receives an early version of the clock, called I/O CLOCK in Figure 4. This clock is early with respect to the CPU clock, the source of the data on the bus. The I/O device input set-up and hold window is relative to its clock. In Figure 4, I/O CLOCK has moved the input set-up and hold window early enough in the cycle that the data on the bus is not yet valid, and the input set-up requirements are violated. A similar situation can occur if the I/O device clock is late. If the clock is too late, the input hold clock requirements will be violated.

Excessive clock skew violates input set-up or hold requirements for control or data signals. The problem is also relative. The clock at the receiver is early or late with respect to the clock at the driver. In the case shown, the CPU is driving an I/O device, and the I/O device clock is early with respect to the CPU clock. If the I/O device is

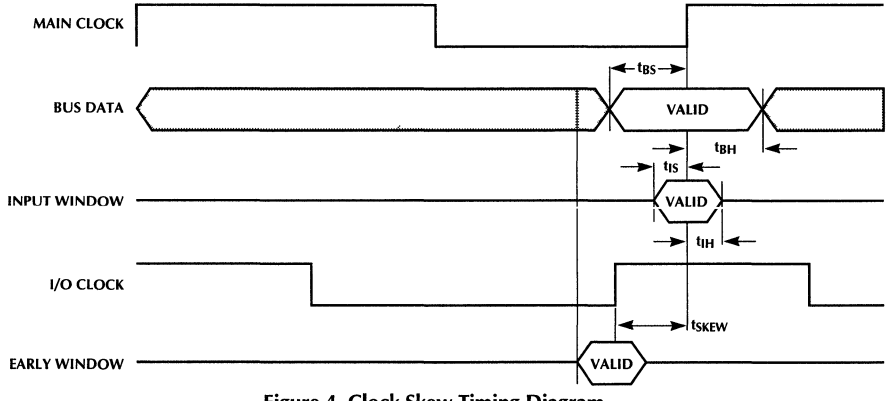


Figure 4. Clock Skew Timing Diagram

driving the CPU on the next cycle, the CPU clock will be late with respect to the I/O device!

The difference in timing between two clock signals is called clock skew. The difference in time between the rising edges of the MAIN CLOCK and I/O CLOCK in Figure 4 is the clock skew, t_{SKEW}.

The maximum value of skew is determined by the set-up time margin ($t_{BS} - t_{IS}$) for I/O CLOCK arriving early to the hold time margin ($t_{BH} - t_{IH}$) for I/O CLOCK arriving late. Since clock skew is relative, all combinations of data output set-up and hold and data input set-up and hold must be considered. The allowable clock skew is usually taken as the minimum of these combinations of set-up and hold margins.

You can compensate for excess clock skew by slowing the system clock in some cases. A slower clock allows data to be on the bus longer, allowing a larger set-up margin and a correspondingly larger allowable early clock skew. This works as long as there is an equivalently large hold time margin for the case of a late clock. In practice, this is seldom done. Slowing down the clock rate for the whole system to accommodate a looser clock system skew is too expensive. An excess skew of 1ns in a 50MHz system would require slowing the clock period from 20 to 21ns, a 5% reduction in system speed. Alternatively, you can use more expensive components to hold the same speed. The loss of system value in the first case or the increase in component cost in the second place usually outweighs the cost of a higher performance clock system.

CLOCK SKEW SOURCES

Clock skew has three primary sources: differences in clock driver output times, clock waveform switching point effects, trace delays, and capacitive loading. High-speed clock systems drive multiple pins, as shown in the system of Figure 5. Multiple clock drivers drive these pins, as many as one driver per pin in some cases. We can see how these sources generate clock skew by examining a simple passive clock system such as the system shown in Figure 5.

The passive clock driver system in Figure 5 uses a crystal oscillator and a passive TTL driver chip such as a 74F244. The 74F244 generates six clock outputs, CLOCK1 through CLOCK6. The first source of clock skew is the difference in propagation delay between the fastest and slowest of the 74F244 drivers. Differences in propagation delay through the drivers in devices such as the 74F244 must be estimated because they are not usually specified in their data sheets. The data sheet specifies a minimum propagation delay of 1.5ns and a maximum of 6.5ns, a potential output-to-output difference, or skew, of 5.0ns. In practice, the output-to-output skew of any pair of drivers on the same chip is 1 to 2ns. Some clock driver versions of these chips specify this skew for drivers on the same chip. If more than one chip is needed, however, the output-to-output skew is larger, perhaps 2–3ns. This is because some chips are faster than others, even if they are from the same lot.

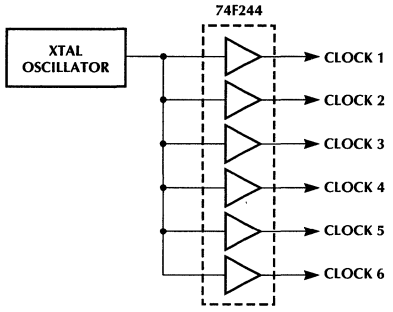


Figure 5. Passive Clock Driver System Example

The second source of skew is due to differences in output capacitive loading. Adding capacitance to an output increases its delay. A typical figure is 1.0ns per 50pF of loading. If one output has a 25pF load and another has 50pF load, this results in a skew of 0.50ns. Adding capacitance to an output increases its rise and fall time, and therefore its delay: it takes longer to get from a TTL high or low to the TTL threshold point of 1.4 volts. Clock systems are sensitive to the clock waveform. Clock signals with square edges and zero rise and fall times exist only in textbooks.

The third source of clock skew is trace delay. Typical trace delays for printed circuit cards are of the order of 0.25ns

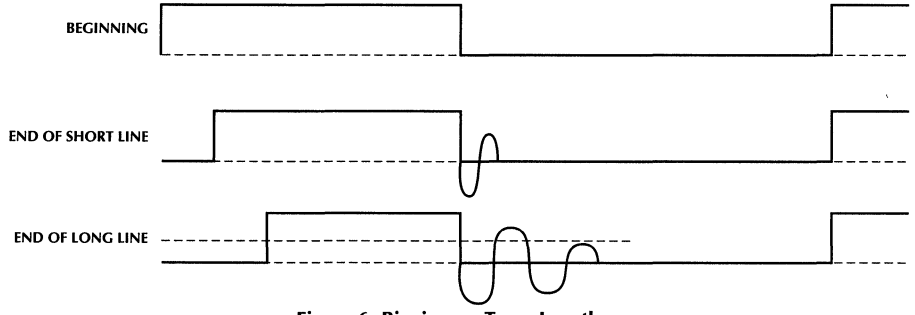


Figure 6. Ringing vs. Trace Length

per inch. If one clock trace is 1 inch and another is 3 inches, there is a trace length difference of 2 inches for a skew of 0.50ns. Our total skew for this system is now (Driver Skew + Loading Skew + Trace Delay Skew) = (1.0 + 0.5 + 0.5) = 2.0ns. This represents a good skew number for careful design. If you use two or more chips and there is more variation in trace delay or loading, this can easily rise to 3 or 4ns.

The ML6500 PACMan solves these skew problems in the following ways.

— **Skew from driver output-to-output delay variation.** Driver delay variations are compensated by the feedback system in the ML6500.

— **Skew from output-to-output load variation.** The ML6500 adjusts its outputs for zero output-to-output skew eliminating variation in output delay due to differences in loading, including differences in rise and fall times due to change in output waveform. The ML6500 can drive high capacitance clock pins — such as the clock pins on some CPUs — and still keep the skew to a minimum. The key here is that the ML6500 detects the output switching point in the same way as the load.

— **Skew from differences in trace lengths.** The ML6500 compensates for trace delay by sensing the switching point of the return signal from the clock pin it is driving. The ML6500 splits the difference in time between the drive switching point and the sensed switching point and makes the clock signal at the load have the same switching point as the reference clock on chip. This makes the trace delay effectively zero. Clock skew is now limited by internal tolerances in the ML6500 and second order effects.

NOISE AND RINGING CLOCK TRACES

The traces on the printed circuit board traces can distort the clock waveform with noise and ringing. This distortion can change the effective skew and, if severe, cause multiple clocking and system failure. Ringing at the end of an unterminated trace increases with line length and decreasing rise/fall time. Figure 6 shows the effects of increasing line length. As the trace gets longer, the ringing noise increases in magnitude and in period. Ringing can cause extra clock pulses. If the ringing amplitude exceeds the logic threshold, the ringing pulses look like valid logic pulses. One such pulse is shown in Figure 6, where the first ringing pulse after the high to low transition exceeds the logic threshold, shown as a dotted line.

The clock trace is a resonant circuit with the trace conductor providing the inductance and the load providing the capacitance along its length. This is shown in the simplified electrical model in Figure 7. C_{LOAD} in this model is the capacitive load of the clock pin being driven. Appendix 1 gives formulas for trace inductance and capacitance.

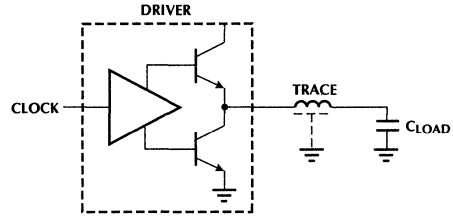


Figure 7. Clock Trace Simplified Electrical Model

Ringing noise is approximately proportional to the ratio of the trace resonant period (including the capacitive load) to the clock rise/fall time. When the trace length is short, the trace inductance and capacitance are low, the resonant frequency is high and the resonant period is small. The ringing magnitude is also small. As the trace length increases, its inductance increases as well as its capacitance. Its resonant period increases, and the ringing magnitude also increases. Increasing the load capacitance also increases the resonant period and ringing. As clock frequencies increase and rise/fall times become shorter, clock ringing becomes more of a problem. A trace that works with a 5ns rise may have unacceptable ringing with a 2ns rise time.

NOISE SENSITIVITY OF TTL SIGNALS

Ringing in TTL tends to be worse and more of a problem on high to low transitions than on low to high transitions. Figure 6 shows ringing only on the high to low transition. The high to low transition generates more ringing because TTL drivers have a stronger drive capability in the high to low direction than in the low to high direction. The stronger drive makes high to low transition time shorter and its ringing worse. When the high to low driver is fully turned on, it looks like a low resistance to ground, typically 3–10Ω. This low resistance provides little damping for the resonant circuit.

The low to high driver has a higher resistance that provides less initial drive to the resonant circuit and damps the ringing faster. "Totem pole" type TTL outputs used in bipolar TTL devices and some CMOS devices such as the FCTT series damp the low to high ringing even faster. In these outputs, the low to high driver turns off when the output rises above 3.5 volts. During the low to high transition, the driver charges the load capacitor through the trace inductance. The current flow started in the trace inductance continues to drive the load capacitance above the V_{OH} of the driver. When the inductor current reaches zero, the load capacitor is at some voltage above the V_{OH} of the driver. In a CMOS driver which has a resistive switch to V_{CC} in the pull-up direction, current begins to flow back into the driver since the load voltage is higher than the driver V_{OH}, continuing the resonant ringing action. In a totem pole output, the diode action of the

output turns it off, preventing current from flowing back into it. Thus, the load capacitor is charged to the peak of the ringing voltage — 4 or 5 volts — by the low to high transition and stays there without further ringing. This kills all ringing once the initial low to high step has been made.

High to low transitions in TTL are more sensitive to ringing noise than low to high. In TTL, the typical logic signal swings from 3.5 volts for a high to 0.2 volts for a low, and logic switching threshold is 1.4 volts. A positive ringing pulse in the high to low direction of greater than (1.4 – 0.2) = 1.2 volt generates a false pulse. A negative ringing pulse in the low to high direction must exceed (3.5 – 1.4) = 2.1 volts to generate a false pulse.

High to low transitions in TTL also generate more ringing noise. TTL drivers have low on resistance in the low state which provides little damping to the ringing resonant circuit. CMOS TTL drivers have higher impedance in the high state than the low state, providing more damping for ringing. If you use a TTL driver with a totem pole type TTL output, there is no ringing on the low to high transition so no negative ringing pulse is generated.

DRIVING SHORT CLOCK TRACES

The ML6500 drives two traces in series, as shown in Figure 8. TRACE #1 connects the ML6500 driver output to the load capacitor. TRACE #2 connects the load capacitor, C_{LOAD} to the ML6500 sense feedback input. C_{PIN} is the input capacitance of the sense pin. The ML6500 assumes that the delay in the drive path and sense paths are equal and compensates the output by moving it earlier by half the difference in time between the drive pin and sense pin signals. There are three cases of interest: short traces (<2"), medium length traces (2" < L < 8") and long traces (>8").

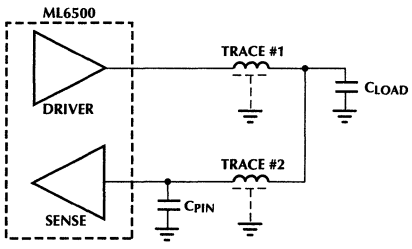


Figure 8. ML6500 Driving a Clock Pin

Short traces have small values of trace capacitance and inductance. The trace capacitance is typically much less than the load capacitance. If the trace capacitance is ignored, the two traces become two inductors. There are two delays in this circuit. The first is the delay from the driver to C_{LOAD}; the second is from C_{LOAD} to C_{PIN} and the sense input. The delay from the driver to C_{LOAD} is determined by the inductance of TRACE #1, C_{LOAD} and the rise time of the driver signal. The delay from C_{LOAD} to C_{PIN} is determined by the inductance of TRACE #2, C_{PIN} and the rise time of the signal at C_{LOAD}. SPICE models of this circuit show a delay from the driver to C_{LOAD} and little delay from C_{LOAD} to C_{PIN}, for $C_{LOAD} > C_{PIN}$. Most of the transient current flows in the TRACE #1 to C_{LOAD} path. SPICE result examples are given in the Appendix.

Traces to 2" and load capacitances to 50pF cause delays up to 1.0ns between the driver and C_{LOAD}. If there is zero effective delay in the sense path (the sense pin follows the load pin closely), the ML6500 compensation circuitry sees up to a 1.0ns difference between the drive and sense pins. The ML6500 changes the drive pin timing to compensate for half this value on the assumption (not valid in this case) that the delay in the drive and sense paths are equal. If the driver to C_{LOAD} delay is 1.0ns, the ML6500 changes the output timing by 1.0/2 = 0.5ns. This is half the amount required but is within the 1ns skew specification for the ML6500.

For short traces, the ML6500 compensates for the degradation in output rise time caused by TRACE #1 and C_{LOAD}. If TRACE #1 is quite short (<1"), most of the rise time degradation is caused by the loading effect of C_{LOAD} on the ML6500 driver output. The RC time constant of the ML6500 driver impedance and C_{LOAD} causes the delay. In this case, the ML6500 provides full skew compensation because there is very little difference in delay between the driver output pin and the sense pin.

The ML6500 circuitry adjusts the delay in the driver to cause the midpoint of the drive and sense pin signals to align with the reference signal. If the compensation circuit only monitored the drive pin, it would compensate for loading as seen at the drive pin. You can get this effect by connecting the sense and drive pins together. Since the two pins have the same timing, the midpoint is the same as the driver pin alone. If the TRACE #1 is quite short, you get the same effect. The delay from its inductance is with respect to the delay from the driver loading. This is similar to tying the drive and sense pins together. With little delay between the drive and sense pins, and the ML6500 to fully compensates for the rise time degradation.

If TRACE #1 is quite short (<1"), it may be possible to run a signal trace and eliminate TRACE #2. In this case, the drive and sense pins are connected together. SPICE models of these circuits show a typical difference in delay between drive and sense pin of 0.3ns or less for trace lengths of less than 1". Tying the drive and sense pins together and running a single trace results in an uncompensated delay of 0.3ns. Running the second, sense trace reduces this to 0.15ns. You can trade the 0.15ns improvement for the board space saved by not running the additional trace.

LONG TRACES ARE TRANSMISSION LINES

The lumped constant model of Figure 7 is useful as a guide to understanding short traces with high capacitance loads. However, a long trace acts more like a transmission line than a lumped constant resonant circuit. The distributed nature of the inductance and capacitance hints at this in the model of Figure 7. The transmission line model is more useful when the propagation delay of the trace is greater than one half of the signal rise or fall time. The equation for this is the following:

(Trace Length) x (0.144) > (Rise Time) / 2

A trace delay of 0.144ns per inch is representative for unloaded traces on conventional epoxy printed circuit boards. For clock edges with rise and fall times of 2ns, use the transmission line model for traces longer than 7 inches. Nothing magic happens at this characteristic length: what looks like ringing at 2" gradually looks like transmission line reflection by the time the trace length reaches 7".

The transmission line model is useful for two reasons. First, transmission lines have a characteristic impedance, and if you terminate a transmission line in this characteristic impedance, it kills the ringing. Second, you can estimate the propagation delay by using the trace transmission line propagation delay.

Transmission lines have propagation delay, characteristic impedance and reflection. The geometry and the material of the printed circuit card determine the transmission line characteristics of traces. Appendix 1 gives formulas for these characteristics. A good transmission line — such as a coaxial cable — propagates a signal with pure delay and no distortion if driven by and terminated in its characteristic impedance. The signal output from a pulse generator looks the same whether the 50Ω terminator is at the pulse generator output or at the end of a 50Ω coaxial cable connected to its output. If you terminate a transmission line in its characteristic impedance, what comes out of the line is exactly the same as what goes in. The driver output does not have to be matched to the transmission line. The driver impedance is important only if you do not terminate the line in its characteristic impedance.

If you do not terminate the transmission line in its characteristic impedance, some or all of the signal is reflected from the end. Equation #1 gives the amount and polarity of the reflection. Equation #2 gives the voltage at the terminator after reflection. V_{IN} is the input step voltage, and V_r is the reflected voltage. If V_r is positive, the step is in the same direction as the input step. If the termination impedance is 1% high, a 1% increase in voltage will be propagated back to the source. If it is 1% low, a 1% decrease in voltage will be propagated back to the source.

$$V_r = V_{IN}\left(\frac{R_t - Z0}{R_t + Z0}\right) \qquad \text{Equation \#1}$$

$$V_t = 2\left(\frac{R_t}{R_t + Z0}\right) \qquad \text{Equation \#2}$$

Where: V_{IN} = Transmission Line Input Voltage

V_r = Reflected Voltage

R_t = Terminating Resistance

Z0 = Transmission Line Impedance

V_t = Voltage at Terminator after Reflection

If the line is unterminated (the termination impedance is infinite), the pulse voltage propagating down the lines doubles when the pulse reaches the end, per Equation #2. This doubled voltage then propagates back to the source. If the source output impedance is equal to the transmission line impedance, the voltage at its output doubles, and that is the end of it. There is no reflection from the source, per Equation #1. This condition is called series termination. It means that the termination resistance is in series with the driver and there is no termination resistance at the load. The result is a perfect propagation of signal and no apparent reflection from the high impedance load.

If the source impedance does not equal the transmission line impedance, the reflection is re-reflected. This is the under-terminated series termination case. Equation #1 applies in this case as well, where V_{IN} is the original reflected value and V_r is the re-reflected value.

PARALLEL TERMINATION FOR CLOCK LINES

All clock lines must be terminated at the load end. This is called parallel termination. The simplest parallel termination is a resistor to ground across C_{PIN} equal to the transmission line impedance. Figure 9 shows this parallel termination scheme and several others. You have three problems to solve in parallel termination: determining the termination resistance value; driving it; and minimizing power dissipation caused by the terminator.

You can use the formulas in Appendix 1 to calculate the unloaded transmission line impedance of the trace. Adding capacitance to the line in the form of C_{LOAD} and C_{PIN} lowers the line impedance by the square root of the ratio of the load capacitance to the trace capacitance. The actual impedance is now a function of the original, unloaded impedance, the trace length ad the capacitances of C_{LOAD} and C_{PIN}. Adding these capacitances can reduce the effective line impedance by a factor of 2. You can estimated the proper termination resistance using the formulas; however, you should check the results to be sure that it kills the reflections.

The resistor to ground terminator has a problem: most TTL circuits are not designed to drive low resistances to ground. A 50Ω termination requires 60mA at the TTL high output voltage of the driver, V_{OH}, of 3.0 volts. While many TTL devices will drive 60mA to ground, most have a maximum rated DC drive current of less than 24mA at a V_{OH} of 2.4 volts. Power dissipation is the third problem with parallel termination. Simple termination schemes require significant power. A simple resistor to ground dissipates $(V_{OH})^2 / 2R_t$ for a TTL high.

V_{CC} termination helps the drive problem. By connecting the termination resistor to V_{CC}, the TTL device only drives current to ground. This current can be large, however. The TTL driver must sink V_{CC} / Rt of current. This is 100mA for a 50Ω load and 5 volts V_{CC}. V_{CC} termination also makes power dissipation worse. Power is now $(V_{CC})^2 / 2R_t$ for a TTL low.

Thevenin termination provides a compromise for the driver. The two resistors combine to form the termination resistance, and their ratio determines the effective termination voltage, which is usually set at 2.0 to 3.0 volts. In Figure 10, it is one half of V_{CC}, 2.5 volts. The drive current for a TTL low is cut in half by this scheme. However, power is now dissipated through the resistor network at a TTL high, adding to power dissipation. Thevenin termination also requires twice as many terminating resistors as the other methods, requiring added board space.

The voltage termination scheme eliminates the resistor network power by providing a termination voltage power supply. This reduces the power dissipated at the expense of an additional power supply.

BALANCING DRIVE AND SENSE DELAYS

The ML6500 compensates for trace delays using the assumption that the drive and sense traces (TRACE #1 and TRACE #2, respectively) have the same delay. The delays are nearly equal if the capacitive loading is equal: if $C_{LOAD} = C_{PIN}$. This will be true for a master ML6500 driving slave ML6510's because the input pin capacitances are equal. If C_{LOAD} is larger than C_{PIN} there will be a difference in delay. This difference is approximately 0.7 times the transmission line impedance multiplied by the difference in capacitance. SPICE simulation will give a more accurate value. The ML6500 circuitry will make the clock signal at the load pin early by this amount.

The drive and sense traces must be equal in length for equal delay. Also, they must be separated by a ground trace so they will not be coupled by crosstalk interaction. One method is to run the drive trace on one side of the ground plane and the sense trace on the other.

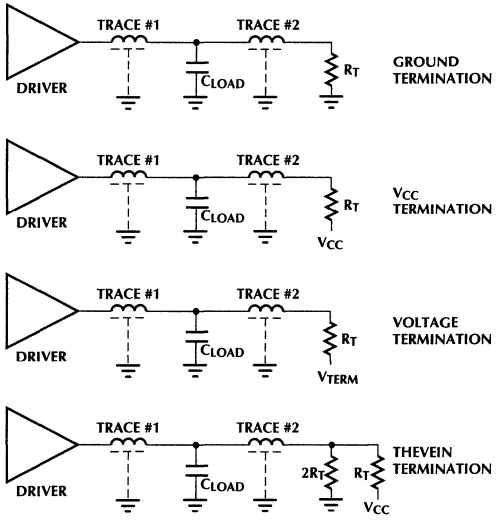


Figure 9. Parallel Termination Methods

PERFORMANCE DATA

The waveforms in the following figures show the ML6500 Master in 66MHz, 75MHz and 80MHz operation. The measurements are made at different Clock trace lengths with varying loads to show the skew and duty cycle performance of the device. The Tektronix TDS820 6GHz digital oscilloscope and P6207 4GHz FET probes with 0.4pF input capacitance are used for the test. The measurements indicated are Frequency, skew delay between clocks at the load, duty cycle and rise time. The clock trace length is between CLK0 at 2.5" and up to CLK4 at 9" with load variations from 5pF to 20pF as shown in the figures. The ML6500 Evaluation Kit in figures 12 and 13 is used for the measurements.

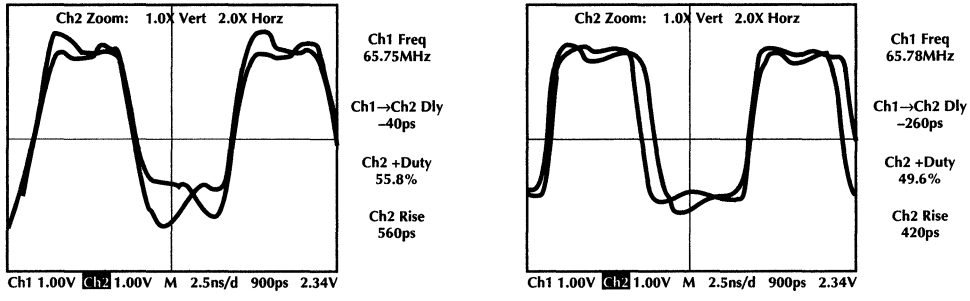


Figure 10. The waveform marked (a) shows two 66MHz clock signals. Channel 1 is connected at CLK1 which is 3.5" from the ML6500 with a 20pF load. Channel 2 is CLK6 which is 3" of PCB trace and 12" of coax cable and a 20pF load. The measured skew between the two is 40ps. Waveform (b) has channel 1 connected to CLK0 which is 2.5" and 5pF while channel 2 is CLK7 at 9" and 15pF. Here, the skew is 260ps.

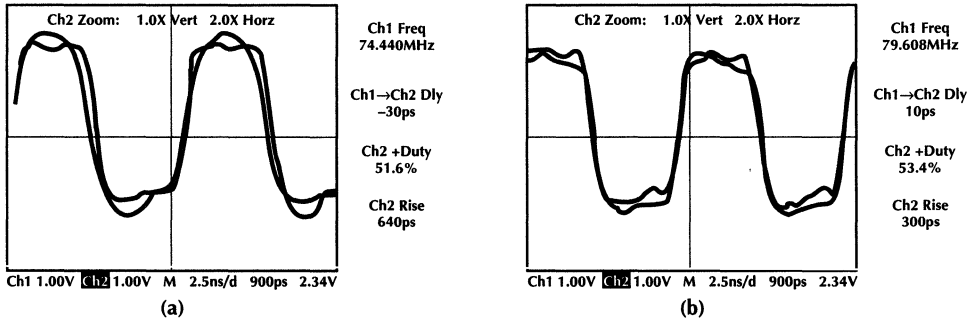


Figure 11. Waveform (a) is a 75MHz clock with channel 1 at CLK0 with 2.5" of trace and 5pF. Channel 2 is CLK4 with 9" and 15pF. The skew is 30ps. Wave form (b) is set at 80MHz with channel 1 the same as (a) and channel 2 at CLK5 with 9" trace and 10pF. The skew here is 10ps. Also notice the duty cycles are near 50% and over/undershoot is minimal.

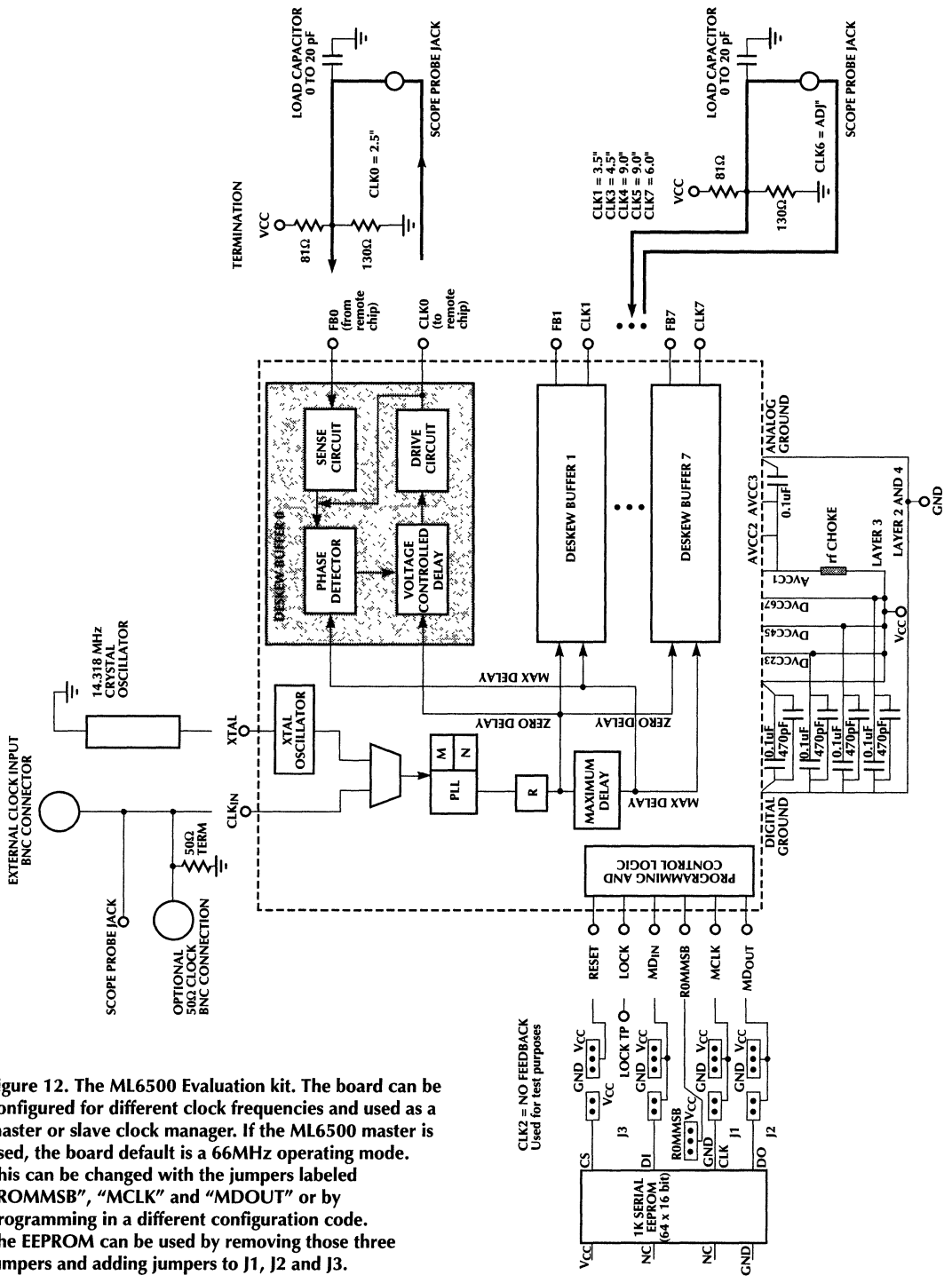


Figure 12. The ML6500 Evaluation kit. The board can be configured for different clock frequencies and used as a master or slave clock manager. If the ML6500 master is used, the board default is a 66MHz operating mode. This can be changed with the jumpers labeled "ROMMSB", "MCLK" and "MDOUT" or by programming in a different configuration code. The EEPROM can be used by removing those three jumpers and adding jumpers to J1, J2 and J3.

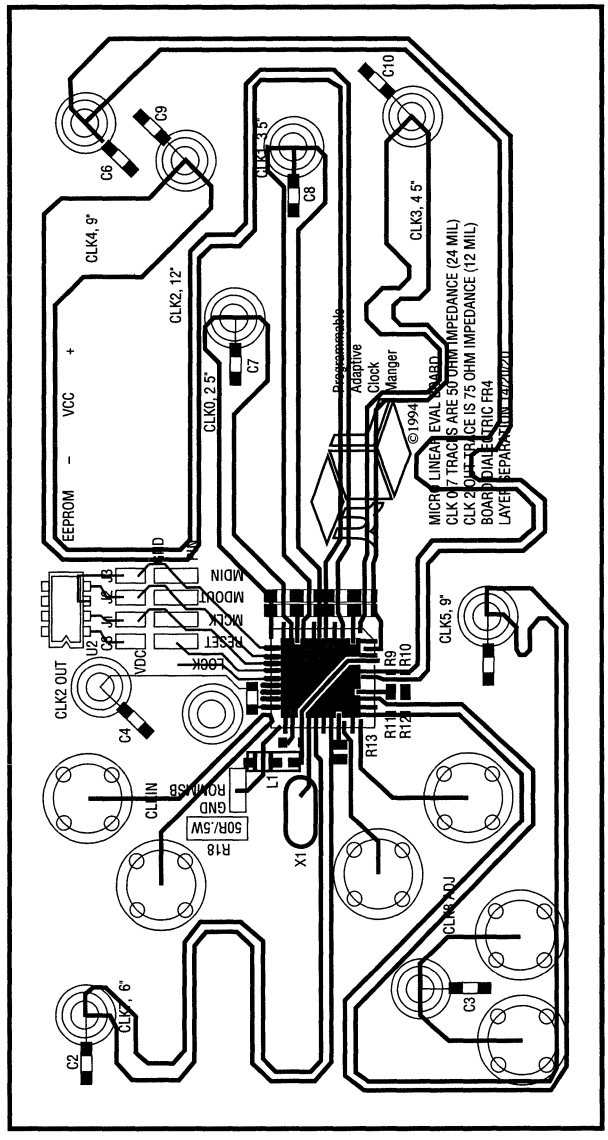


Figure 13. Top level view of the ML6500 evaluation board. The ground plane beneath the device is split between analog and digital grounds. All terminations and decoupling capacitors are as close to the device as possible.

APPENDIX 1: PRINTED CIRCUIT TRACE CHARACTERISTICS

The geometry of printed circuit traces and the dielectric constant of the printed circuit board material holding them determine their transmission line characteristics. Figure A1 shows the two major trace types used on PC boards, the surface Micro Stripline and the internal Stripline. Table 1 gives the equations for calculating their characteristics and some example values.

Adding load capacitance to a trace increases its effective distributed capacitance. This decreases its impedance and increases the delay per inch. The equations in Table 2 give the effective termination impedance and trace delay for single traces with capacitive loading.

Table 2 gives the unloaded characteristic impedance, propagation delay per inch, capacitance per inch and inductance per inch for various combinations of trace width and board thickness for both microstripline (Surface) and Stripline (internal) traces. Surface traces are on the board surface over a ground plane. The board thickness is the thickness between the trace and the ground plane. A 0.030 thickness corresponds to a 4-layer board; a 0.012 thickness corresponds to the surface of 6 layer board. Internal traces are between ground planes.

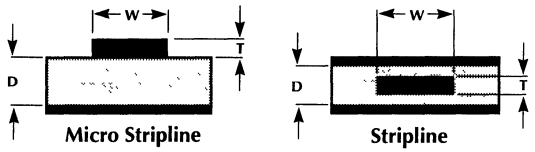


Figure A1: Printed Circuit Trace Geometries

The board thickness is the distance between the two ground planes and assumes that the trace is centered between them. The 0.026 thickness is for an internal trace on a 6-layer board where the 0.026 is the distance from a center ground plane to the surface layer of the board.

Table 3 shows the change in effective characteristics impedance and propagation delay for various combinations of transmission line length and capacitive loading. The PC board trace is 0.010" wide by 0.002" thick, and the board dielectric constant is 4.7 for glass epoxy PC board material. Other trace characteristics can be derived from Table 2.

Table 4 shows the trace resonant frequency for various traces and capacitive loads.

TABLE 1: PC TRACE CHARACTERISTICS

CHARACTERISTIC	SYMBOL	UNITS	MICRO STRIPLINE		STRIPLINE	
			EQUATION	EXAMPLE	EQUATION	EXAMPLE
Dielectric Constant	Er	—	—	4.7	—	4.7
Board Thickness	D	inches	—	0.012	—	0.026
Trace Width	W	inches	—	0.010	—	0.010
Trace Thickness	T	inches	—	0.002	—	0.002
Impedance	Z0	Ω	$\frac{87}{\sqrt{Er+1.41}}\ln\left(\frac{5.98D}{0.8W+T}\right)$	69.36	$\frac{60}{\sqrt{Er}}\ln\left(\frac{4D}{0.67\pi W\left(0.8+\frac{T}{W}\right)}\right)$	44.21
Delay per Inch	t_{PDZ}	ns/in	$\frac{1.017}{12}\sqrt{0.475Er+0.67}$	0.144	$\frac{1.017}{12}\sqrt{Er}$	0.183
Capacitance per Inch	C_Z	pF/in	$1000\frac{t_{PDZ}}{Z0}$	2.08	$1000\frac{t_{PDZ}}{Z0}$	3.27
Inductance per Inch	L_Z	nH/in	$t_{PDZ}Z0$	10.015	$t_{PDZ}Z0$	6.38
Capacitive Load	C_{LOAD}	pF	—	37	—	37
Impedance with Capacitive Load	Z	Ω	$Z0\sqrt{\frac{C_Z}{C_Z+\frac{C_{LOAD}}{L_Z}}}$	41.08	$Z0\sqrt{\frac{LC_Z}{LC_Z+C_{LOAD}}}$	29.94
Delay per Inch with Capacitive Load	t_{PD}	ns/in	$t_{PDZ}\sqrt{\frac{L_Z C_Z+C_{LOAD}}{L_Z C_Z}}$	0.244	$t_{PDZ}\sqrt{\frac{L_Z C_Z+C_{LOAD}}{L_Z C_Z}}$	0.213

TABLE 2: TRANSMISSION LINE CHARACTERISTICS FOR VARIOUS TRACES

TYPE	BOARD Er	BOARD THICK	TRACE WIDTH	TRACE THICK	Z0 OHMS	t_{PDZ} ns/in	CAP. pF/in	IND. nH/in
Surface	4.70	0.012	0.010	0.002	69.36	0.144	2.08	10.02
Surface	4.70	0.012	0.020	0.002	48.68	0.144	2.97	7.03
Surface	4.70	0.030	0.010	0.002	101.61	0.144	1.42	14.67
Surface	4.70	0.030	0.020	0.002	80.93	0.144	1.78	11.68
Surface	4.70	0.062	0.010	0.002	127.16	0.144	1.14	18.36
Surface	4.70	0.062	0.020	0.002	106.48	0.144	1.36	15.37
Internal	4.70	0.012	0.010	0.002	22.82	0.144	6.33	3.29
Internal	4.70	0.012	0.010	0.002	13.50	0.144	10.69	1.95
Internal	4.70	0.012	0.020	0.002	6.55	0.144	22.05	0.95
Internal	4.70	0.026	0.010	0.002	44.21	0.144	3.27	6.38
Internal	4.70	0.026	0.020	0.002	27.95	0.144	5.17	4.04

TABLE 3: TRACE IMPEDANCE AND DELAY vs. LENGTH AND LOAD CAPACITANCE

TYPE	BOARD THICK	TRACE WIDTH	CAP pF	0pF Load		5pF Load		10pF Load		20pF Load	
				Z0	ns/in	Z0	ns/in	Z0	ns/in	Z0	ns/in
Surface	0.030	2	2.84	101.61	0.144	61.17	0.24	47.80	0.31	35.84	0.41
Surface	0.030	3	4.26	101.61	0.144	68.93	0.213	55.55	0.264	42.59	0.344
Surface	0.030	4	5.68	101.61	0.144	74.11	0.198	61.17	0.240	47.80	0.307
Surface	0.030	6	8.53	101.61	0.144	80.67	0.182	68.93	0.213	55.55	0.264
Surface	0.030	8	11.37	101.61	0.144	84.68	0.173	74.11	0.198	61.17	0.250
Surface	0.030	10	14.21	101.61	0.144	87.39	0.168	77.85	0.188	65.49	0.244
Internal	0.026	2	6.53	44.21	0.144	33.28	0.192	27.79	0.230	21.94	0.291
Internal	0.026	3	9.80	44.21	0.144	35.98	0.177	31.10	0.205	25.35	0.252
Internal	0.026	4	13.06	44.21	0.144	37.60	0.170	33.28	0.192	27.79	0.230
Internal	0.026	6	19.59	44.21	0.144	39.46	0.162	35.98	0.177	31.10	0.205
Internal	0.026	8	26.13	44.21	0.144	40.51	0.158	37.60	0.170	33.28	0.192
Internal	0.026	10	32.66	44.21	0.144	41.17	0.155	38.69	0.165	34.82	0.183

TABLE 4: TRACE RESONANT PERIOD FOR VARIOUS TRACE LENGTHS AND LOADS

TRACE TYPE	BOARD THICK	LENGTH INCHES	TRACE IND. (nH)	TRACE CAP. (pF)	C_{LOAD} pF	FREQ. MHz	PERIOD ns
Surface	0.012	4.0	40.6	8.33	20	149	6.71
Surface	0.030	1.0	14.7	1.42	50	183	5.46
Surface	0.030	1.0	14.7	1.42	20	284	3.52
Surface	0.030	2.0	29.4	2.84	20	194	5.15
Surface	0.030	4.0	58.7	5.68	20	130	7.69
Surface	0.030	8.0	117.4	11.37	20	83	12.05
Internal	0.026	1.0	6.38	3.27	50	273	3.66
Internal	0.026	1.0	6.38	3.27	20	413	2.42
Internal	0.026	2.0	12.76	6.53	20	273	3.66
Internal	0.026	4.0	25.52	13.06	20	173	5.78
Internal	0.026	8.0	51.04	26.13	20	104	9.62

Theory and Application of the ML4864 Backlight and Contrast Controller IC

by George A. Hall &
K. Kit Sum

INTRODUCTION

The ML4864 is a high performance backlight and contrast controller integrated circuit specifically designed to control miniature fluorescent lamps (CCFLs) for portable computing and instrumentation equipment.

This device was designed to achieve high efficiency as well as high flexibility in design and application. Some of the key features are:

- Capable of driving all N-channel FETs.
- Self-synchronizing lamp driver section is designed for low loss zero voltage switching (ZVS).
- Lamp current is regulated by a buck switching converter which is synchronized to the lamp driver frequency for flicker free operation. The duty cycle is capable of operating from 0% to 100%.
- Oscillator operating frequency range is from 20KHz to 500KHz. The frequency is set by an external timing capacitor. The oscillator frequency is twice the lamp inverter switching frequency.
- Uses off the shelf power components including magnetic components.
- Separate flyback output can be generated for the required negative or positive contrast voltage. The duty cycle is capable of operating from 0% to 95%. Flyback frequency is fully synchronized to the rest of the circuit for flicker free operation.
- The lamp driver section can be shut down independently by logic control input, while the contrast voltage generator is running, resulting in reduced power consumption in the presence of ample ambient light and when a transflective LCD screen is used.
- Surface mount SSOP package of this circuit is available for space economy.

FUNCTIONAL BLOCK DIAGRAM

The ML4864 consists of three main operating functional blocks.

- A buck current regulator block that controls the lamp current.
- A current fed lamp driver block that uses a self-synchronizing scheme for low loss zero voltage switching (ZVS), and facilitates flicker free dimming.

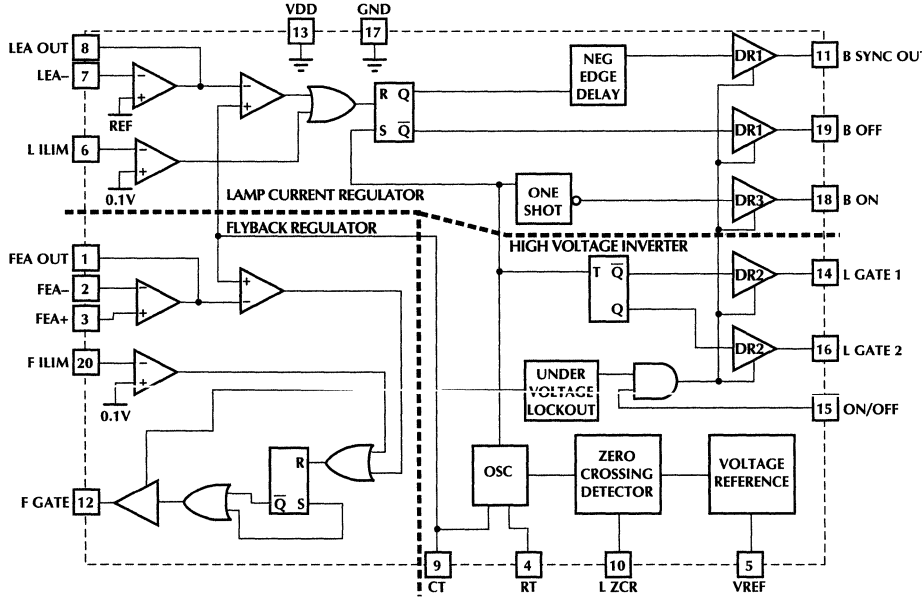


Figure 1. Block Diagram of the ML4864

- A contrast voltage generator block that generates and controls the levels of negative or positive voltages. This block can incorporate one of several switching topologies.

The simplified block diagram of the ML4864 is shown in figure 1. The three functional blocks are separated by the heavy dotted lines. For easier understanding, each block will be described and the necessary design information given.

To achieve frequency synchronization, all three blocks share a common oscillator. This feature helps reduce possible RFI and the effect of the 'walking' lines across the LCD screen. The operating frequency of the buck and the contrast regulator is twice that of the CCFL inverter frequency.

The synchronization of the oscillator is achieved by sensing the voltage at the center tap of the lamp inverter transformer.

DESCRIPTION OF THE LAMP INVERTER CIRCUIT

The lamp inverter circuit is comprised of the current regulating buck converter and the high frequency push-pull converter. The buck converter controls the magnitude of lamp current. This feature is instrumental in dimming control. The simplified equivalent electrical schematic of the driver section is shown in figure 2.

Due to the presence of L_1, the circuit shown in figure 2 is effectively a current fed parallel loaded parallel resonant circuit, which can be further simplified to that shown in figure 3.

The simplification in figure 3 assumes that two lamps are operating in parallel. If one lamp is used then the original output ballast capacitor value should be used in the calculations.

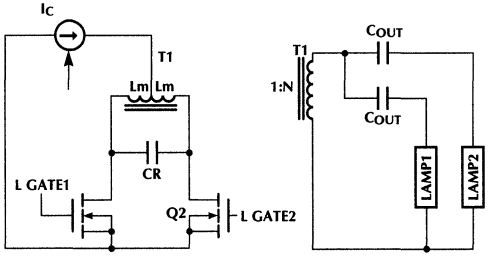


Figure 2. Simplified Lamp Driver Circuit.

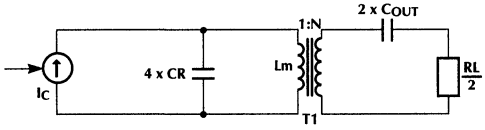


Figure 3. Simplified Lamp Driver Circuit.

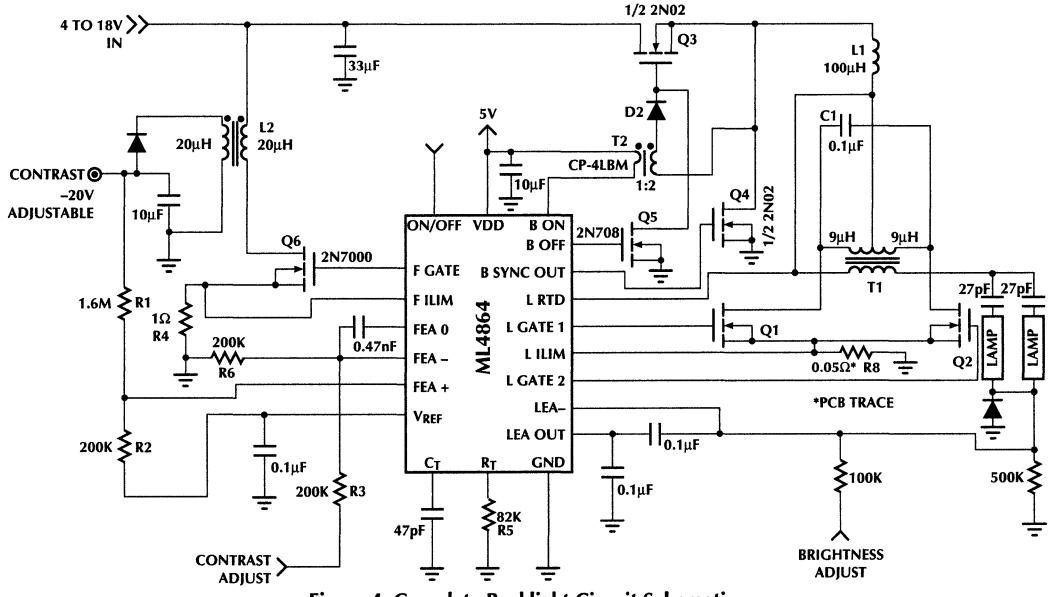


Figure 4. Complete Backlight Circuit Schematic.

L_m is the magnetizing inductance of the inverter transformer, which tunes with the resonant capacitor C_R to set the resonant frequency of the inverter. The oscillator frequency of the ML4864 is set slightly lower than the resonant frequency to ensure synchronization.

The current source labeled I_C in figure 3 is a conceptual current source which essentially takes the place of L1. Since the circuit always operates at resonance the impedance seen by the above current source is resistive and equal to the transformed impedance of the lamp which is given by the formula below:

$$R_L = \frac{V_L}{I_L}$$

Where: V_L is the operating voltage of the lamp at full brightness and I_L is the lamp current.

In most cases the value of the ballasting capacitor C_{OUT} is chosen such that its reactance is approximately three times the lamp resistance R_L. The two capacitors C_{OUT} are used to simulate two separate current sources, so that current will share between the lamps. The typical value for R_L is 100K Ohms. For a typical operating frequency of 50KHz, C_{OUT} yields a capacitive reactance of approximately 300K. The value of C_{OUT} can be calculated to between 10 to 33pF. The best choice for this capacitor is generally between 27 to 33pF.

OSCILLATOR

The oscillator frequency is set externally through R_T and C_T. The equation below gives the relationship between frequency and timing components. This frequency should be set slightly below the resonant frequency of the inverter. See figure 2.

$$f_{OSC} = \frac{1}{3.51 R_T C_T}$$

Under steady state conditions, the oscillator frequency will be locked to twice the natural frequency of the lamp inverter resonant frequency. The minimum resonant frequency (that will be used to calculate the oscillator timing components) can be calculated by using the following formula:

$$f_{MIN} \cong \frac{1}{2\pi\sqrt{L_m\left(4C_m + nN^2 C_{OUT}\right)}}$$

Where n is the number of lamps at the output with ballasting capacitors C_{OUT}, N is the primary to secondary turns ratio of T1, L_m is the primary inductance of T1 and CR is the capacitance across the primary. Based on this information the oscillator free running frequency is set to approximately 10% to 15% less than twice the minimum frequency of the resonant tank.

$$C_T \cong \frac{\sqrt{L_m\left(4C_m + nN^2 C_{OUT}\right)}}{R_T}$$

$$R_T \cong \frac{\sqrt{L_m\left(4C_m + nN^2 C_{OUT}\right)}}{C_T}$$

Example Calculation:

$L_m = 12 \times 10^{-6}$ $\quad C_m = 0.1 \times 10^{-6}$

$C_T = 47 \times 10^{-12}$ $\quad n = 2$

$C_{OUT} = 27 \times 10^{-12}$ $\quad N = 135$

$$f = \frac{1}{2\pi\sqrt{L_m\left(4C_m + nN^2 C_{OUT}\right)}} = 3.905 \times 10^4 \text{Hz}$$

$$R_T = \frac{\sqrt{L_m\left(4C_m + nN^2 C_{OUT}\right)}}{C_T} = 8.671 \times 10^4 \Omega$$

The natural frequency of the resonant tank will increase as the lamp(s) are dimmed. The upper bound of this increase can be estimated by the formula below:

$$f_{MAX} \cong \frac{1}{4\pi\sqrt{L_m C_m}}$$

For the previous example this will be:

$L_m = 12 \times 10^{-6}$ $\quad C_m = 0.1 \times 10^{-6}$

$$f_{MAX} \cong \frac{1}{4\pi\sqrt{L_m C_m}} = 7.264 \times 10^4 \text{Hz}$$

Thus the lowest operating frequency will be at full brightness.

REFERENCE

The reference voltage is 2.5 volts ±2%. To guard against noise it is necessary to connect a 0.1µF capacitor across the reference to ground. This precise reference voltage helps to stabilize the brightness and contrast from unit to unit.

BUCK REGULATOR AND GATE DRIVE CIRCUIT

The ML4864 design is based on a 5V BiCMOS process to obtain the highest possible efficiency and size economy. The buck converter power MOSFET switch, Q3 is driven by a special gate drive circuit.

This drive circuit consists of T2, D2 and Q4. T2 has the dual function of isolating the drive signal and stepping up its voltage for adequate enhancement of Q3. T2 is a standard surface mount transformer that can be obtained from many coil manufacturers. The ML4864 has been designed such that a short duration (approx. 150ns) voltage pulse is applied to T2. This pulse charges the gate of Q3. The charge is trapped at the gate by D2 until the end of the ON-time at which point the gate of Q3 is discharged by Q4. This drive technique enables the ML4864 to control power at voltages that are higher than its own maximum operating voltage rating of 5V.

The gate drive transformer requirements are listed below:

- Leakage inductance <300nH.
- Primary magnetizing inductance >3µH.

SELECTION OF THE BUCK INDUCTOR

The buck inductor L_1 plays a central role in the proper operation of the inverter circuit. The inductance value determines the mode of operation. It is important to choose the correct value for a given application.

To find the inductor value it is necessary to consider the inductor ripple current. The following formula can be used in approximating the inductor peak to peak current.

$$i_{LP-P} \cong \frac{V_{TP}}{4.7 f_{OSC\ MIN} L_b}$$

Where: i_{LP-P} is the peak to peak inductor current, V_{TP} is the peak voltage at the center tap of T1 (the waveform at this point is a full wave rectified sinewave), f_{OSC} min is the minimum oscillator frequency at full brightness, lowest input voltage and L_b is the inductance of the buck inductor L1.

The above equation can also be stated in terms of the input voltage, under steady state operating conditions:

$$i_{LP-P} \cong \frac{V_{IN\ MIN}}{3 f_{OSC\ MIN} L_b}$$

Normally the inductor peak to peak current is chosen to be a small fraction of the overall DC current level. This is one of the design criteria for the inductor.

Choosing i_{LP-P} to be 10% to 20% of the maximum inductor current is a good compromise. The inductance can be expressed in terms of all the known quantities as follows:

$$L_b \cong \frac{3.3 V_{IN\ MIN}^2}{f_{OSC\ MIN} P_L}$$

Where: P_L is the maximum lamp power (if more than one lamp is used then the total consumption of all the lamps).

Example:

$V_{IN\ MIN}$ = 5V, PL = 6W

$f_{OSC\ MIN}$ = 85KHz

$$L_b \cong \frac{3.3 V_{IN\ MIN}^2}{f_{OSC\ MIN} P_L} = 1.618 \times 10^{-4}\ \text{Henry}$$

In this case the calculated inductor value is 160µH. This value can be optimized for any specific application.

INVERTER TRANSFORMER

The inverter transformer T1 has a dual role. Besides stepping up the low voltage to a higher value suitable for the operation of the lamp(s), it is also part of the drain resonant tank circuit. The magnetizing inductance of this transformer is the resonating inductor. This transformer normally is an off the shelf part available from different coil manufacturers. The inverter transformer used in the example circuit is made by Coiltronics, part number: CTX110602-1. It is capable of driving two 3W lamps with a start voltage of 1.5KV. The magnetizing inductance range for the above transformer is 9 to 13µH.

RESONATING CAPACITOR (C1)

Typically, the value of this capacitor falls between 0.047µF to 0.22µF, depending on the frequency and power level. It should be a low tolerance (±5% typical) low loss type component. A polypropylene or equivalent type capacitor should perform quite well. Some polyester film types may also be suitable for this application.

When used with the above-mentioned inverter transformer, with the two lamps at full brightness, a 0.1µF capacitor yields an approximate operating frequency of 48KHz.

CURRENT LIMIT CIRCUIT OF THE BUCK CONVERTER

The buck regulator current control circuit utilizes peak current sense for shutting down the FET instantaneously under over current conditions. The sense resistor is fabricated from the 50mΩ of printed circuit board trace resistance. This is adequate in most of the cases.

DIMMING OF THE CCFL LAMPS

Dimming is accomplished by summing a DC current to the inverting input of the buck error amplifier (pin 7). When a voltage is available instead of current then a resistor can be used.

Figure 5, shows such an arrangement. The 100K resistor connected to pin 7 that goes to brightness adjust control which serves this purpose.There are several ways of generating the "BRIGHTNESS ADJUST" voltage. The simplest method is by using a potentiometer as shown in figure 5.

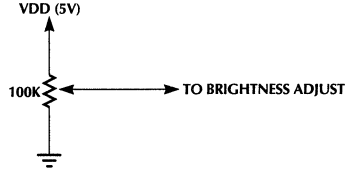


Figure 5. Dimming voltage generation.

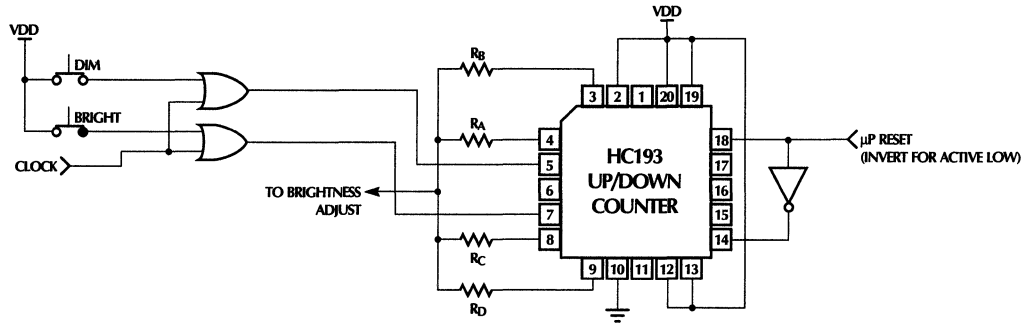


Figure 6. Dimming voltage generation using a Digital UP/DOWN counter.

In the event that the control signal is a PWM modulated digital signal, the circuit shown below may be used.

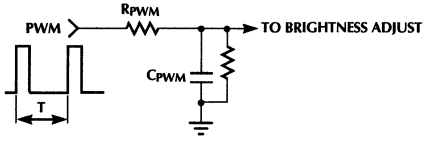


Figure 7. Dimming voltage generation using a PWM signal.

For proper operation the following criterion must be met:

$$C_{PWM} \geq \frac{3T}{R_{PWM}}$$

Another method that can be used for dimming is by using a digital up down counter. (See figure 6.) In this method two push button type switches are used to selectively route the clock pulse either to "UP count" port or to the "DOWN count" port. On initial turn-on the circuit requests full brightness. This can be changed by tying pins 12,13, 19 and 20 of the counter chip to ground. In this condition the circuit will request a full dim condition. Resistors R_A, R_B, R_C and R_D are chosen to provide the required current to the brightness control input. These resistors are chosen to have the 8:4:2:1 ratio for approximately 16 levels of brightness control. For a higher control resolution, an eight bit counter can be used.

CONTRAST VOLTAGE GENERATOR SECTION

The ML4864 also contains the necessary control circuitry to implement a positive or negative voltage for the LCD contrast control function. This controller is synchronized to the master clock of the circuit.

To generate a negative voltage the regulator can be configured as a flyback regulator. Figure 8, shows the negative contrast voltage control regulator configuration.

The output voltage of the regulator can be calculated by the following formula:

$$V_{OUT} = -V_{REF}\frac{R_1}{R_2} + \left(1 + \frac{R_1}{R_2}\right)V-$$

Where: V_{REF} = 2.5V, Vout is the negative contrast output voltage and V– is the voltage at the inverting pin of the error amplifier (pin 6).

When V– = 0V the output voltage can be calculated by using:

$$V_{OUT} = -V_{REF}\frac{R_1}{R_2}$$

Example: R1 = 1.6M, R2 = 200K

$$V_{OUT} = -2.5\frac{1.6M}{200K} = -20V$$

To generate a positive contrast control voltage the regulator can be configured as shown in figure 9.

The output voltage of the regulator can be calculated by the following formula:

$$V_{OUT} = V_{REF}\left(1+\frac{R_1}{R_2}\right)$$

SELECTION OF THE FLYBACK TRANSFORMER

The flyback transformer used in this application is an off the shelf item manufactured by Coiltronics. The part number of this inductor is CTX20-1. Depending on the output current other parts can be selected for optimum efficiency.

LAMP OUT CONDITION

When the lamp is not connected or accidentally disconnected, the starting voltage could continue to build up until it reaches a hazardous level.

To prevent this hazard, one resistor R_{SET}, one diode D_4 and one zener diode D_Z are added to the circuit. The resistor value should be chosen high enough for a time constant consistent with the stability of the circuit. The zener voltage should be selected for a voltage above the starting voltage for the selected lamp. See figure 2.

OPERATING WAVEFORMS OF THE LAMP DRIVER SECTION

Figure 10 shows some of the waveforms present in critical parts of the circuit.

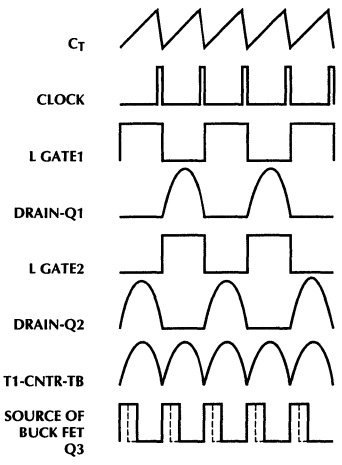


Figure 10. Operating waveforms of the lamp driver section.

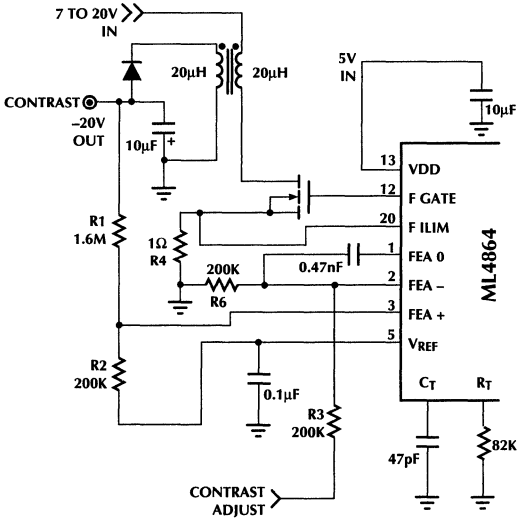


Figure 8. Negative contrast voltage generator circuit.

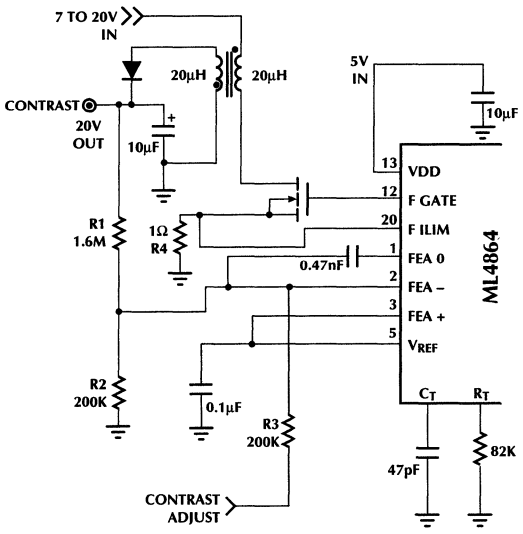


Figure 9. Positive contrast voltage generator circuit.

Active SCSI Terminator — Important Issues Capacitance & Power Dissipation

Ram Gopalan
Tom DeLurio

INTRODUCTION

The SCSI bus is essentially a cable that can be as simple as a flat ribbon cable or as advanced as shielded differential twisted pairs. For this reason, a well-designed active termination is important for reliable data transfer between the Host/Initiator (motherboards, host adaptor add-on cards etc.) and up to seven Targets which could be hard disk drives, CD-ROMs, tape drives, scanners, etc. along 72 feet of cable at 10 MB per second. No easy task considering the complexities of each device and the varying impedance of some of the cheaper cables that are available. Micro Linear's active terminator has been designed to exhibit much lower capacitive loading compared to other competing devices while optimizing the V-I characteristics. This document compares the ML6509 to the offerings from Texas Instruments and Dallas Semiconductor and outlines the capacitance measurement used to get the values. Also provided is a thermal study for the 16 pin SOIC and 20 pin TSSOP packages and a discussion of the device's thermal shut-down mode.

TERMINATOR CAPACITANCE ISSUE

Disconnect capacitance is a very important specification for an active SCSI terminator. The SCSI bus is a transmission line environment and is terminated at the two ends of the bus. Any device in between must not be terminated or it will load down the bus and the system may be subjected to data integrity problems due to double clocking etc. All SCSI devices must have the capability to be terminated so that they can be used anywhere on the bus. Hence an existing termination must either be physically pulled off the SCSI device (such as a passive termination) or the termination must be logically disconnected when a device no longer requires termination. An active termination has the advantage of having a control pin to disconnect the terminator but it is still physically connected to the bus. The underlying problem is that the disconnected device must not add too much capacitance when turned off. The added capacitance may violate the SCSI specification for total capacitive loading at that node and any distributed capacitance along a transmission line, will also alter the bus impedance.

The X3T9.2/855D, revision 12, SCSI-3 document recommends a procedure for measuring pin capacitance in Annex E. The objective of this procedure is to determine the lumped capacitance imposed on each signal conductor of the bus proper by a SCSI device connected thereto. The model for this procedure assumes the bus in the ribbon cable form, passing through an insulation-displacement SCSI connector, the mating part that is mounted on a SCSI device controller printed-wire board. The bus connector is removed from the device, along with every source of power. One or more device connector circuit-common pins are connected together to form an effective circuit-common node. An R-F admittance bridge (or equivalent), operation at 1 MHz is connected successively to each signal pin in the device connector, with reference to the circuit-common node. The signal applied during measurement is biased to 0.5V D.C. and is 0.4V peak to peak in amplitude. The characteristics are determined in terms of parallel combination of a conductance and a capacitative susceptance which corresponds to the capacitance referred to in the SCSI standard.

RESULTS OF CAPACITANCE MEASUREMENT USING GENERAL TECHNIQUE

An experiment was conducted in the lab where the ML6509 disconnect capacitance was compared to the Dallas DS2107S and Texas Instruments TI 2218-285. The test setup to make the capacitance measurements is shown in figure 1 and consisted of an HP model 4275A Multi-Frequency LCR meter and a test fixture. The test frequency was a 10 MHz square wave (to emulate fast SCSI speeds), an oscillation level at 0.7V and the meter biased at 2V. The DUT was powered-up and in disconnect mode. Each pin was measured with respect to ground. In order to cancel the effect of the capacitance due to the socket, probes, the meter etc., each test socket pin was measured empty and the value subtracted from each DUT pin measurement to cancel the contribution from them.

The results of the experiment are summarized in Table 1. As can be seen, the DS2107S offers a capacitance per termination line of approximately 23 pF at the node, while the TI2218-285 offers a capacitance per termination line of approximately 10 pF at the node. The ML6509 offers an average capacitance per termination line of approximately 4.5 pF at the node. The ML6509 production test will guarantee this capacitance to be below 5 pF on each line (rev C). The capacitance value significantly change the characteristic impedance of the cable and cause reflections which results in lowering the data integrity on the bus. Under the same test conditions, the TI part is relatively better then the DS2107S but is still worse than the ML6509.

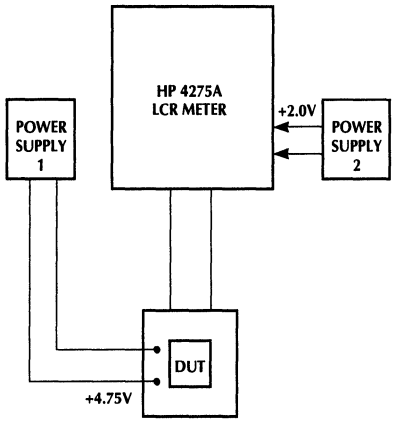


Figure 1. Test Setup

TABLE 1 CAPACITANCE MEASUREMENTS (pF) USING GENERAL TECHNIQUE

Termn Line #	ML6509 TSSOP (REV C)	ML6509 SOIC Rev B	ML6509 SOIC Rev C	DS2107S SOIC	TI2218-285 TSSOP
L1	4.6	7.1	3.7	23.3	12.0
L2	3.8	6.6	3.9	23.6	11.8
L3	4.4	6.6	3.8	23.6	10.8
L4	4.8	6.4	3.9	23.5	9.5
L5	4.8	6.8	3.9	23.5	10.9
L6	4.8	6.8	4.1	23.3	9.5
L7	4.9	7.5	4.0	23.5	10.6
L8	4.8	9.0	4.1	23.6	10.7
L9	4.3	9.0	3.9	23.7	11.0

RESULTS OF CAPACITANCE MEASUREMENTS USING ANSI RECOMMENDED TECHNIQUE

The same experiment was conducted to measure disconnect capacitance of the ML6509, Dallas DS2107S and Texas Instruments TI 2218-285 in accordance with the ANSI recommended technique. The test frequency was a 1 MHz square wave, an oscillation level at 0.4 Vp-p and the meter biased at 0.5V. The DUT was powered-up and in disconnect mode. Each pin was measured with respect to ground. In order to cancel the effect of the capacitance due to the socket, probes, the meter etc., each test socket pin was measured empty and the value subtracted from each DUT pin measurement to cancel the contribution from them.

The results of the experiment are summarized in Table 2. As can be seen, the DS2107S offers an average capacitance per line of approximately 30 pF at the node, while the TI2218-285 becomes inductive as observed by the negative readings, which could imply problems of a different kind on the SCSI bus. The ML6509 offers an average capacitance per line of approximately 6.5 pF at the node with this measurement technique. Hence under the same test conditions, the TI part is the worst as it turns inductive, the DS2107S part is much better then the TI part but is still no match for the ML6509 at 7 pF average per line.

TABLE 2 CAPACITANCE MEASUREMENTS (pF) USING ANSI TECHNIQUE

Termn Line #	ML6509 TSSOP REV C	ML6509 SOIC REV C	DS2107S SOIC	TI2218-285 TSSOP
L1	6.0	6.9	33.0	–292
L2	6.5	6.9	33.1	–277
L3	6.5	7.1	33.2	–277
L4	6.8	7.1	33.3	–271
L5	6.7	7.1	32.7	–268
L6	7.0	7.3	25.5	–311
L7	7.0	7.3	25.9	–312
L8	6.7	7.0	25.8	–264
L9	6.2	7.0	25.9	–305

POWER DISSIPATION ISSUE THERMAL MEASUREMENTS

The AC power dissipation characteristics of an active terminator are described somewhat differently then what is commonly used for a standard integrated circuit. This is because SCSI terminators are not specified with respect to capacitive loading. The device does no "drive" a capacitive load at a stated frequency because as mentioned earlier, SCSI is a transmission line environment which theoretically has zero capacitance if terminated with the lines' characteristic impedance. When an output is active, it is at a logic low (0.2V) and sources 24mA. When inactive at a logic high (2.85V), the output sources only 0.5mA. If all outputs are low, the part sources 216mA. This seems extreme and it is under dc conditions. Fortunately, in actual use, all nine outputs are held low for no more then 50 ns at a time in a 10MBps SCSI bus system on the two most active lines, /REQ and /ACK. Also, on average, only 50% of the outputs will be low at the same time for that short duration.

The ML6509CT device in the TSSOP has a heat sink internally on which the die is set. The heat is dissipated through the heat sink pins 2, 8, 12, 18.

The ML6509 also has a low power mode for driving small cable lengths or for use in portable applications. In this mode, the terminator only sources 1mA per output. When the device is in disconnect mode, it does not draw more than 100 µA, and in standby mode when the outputs are high, not more than 5mA is used by the device. This is much less than the constant current that flows through a resistor divider in a passive termination.

To determine the average junction temperature for a SCSI device, the following equation for Maximum Junction Temperature (Tj) is used:

$Tj = (\theta ja)\ (Pd) + T_A$

where:

Maximum $Pd_{LOW} = (5.5V - 0.2V)\ (24mA)\ (9) = 1.15W$

Maximum $Pd_{HIGH} = (5.5V - 2.8V)\ (0.5mA \times (9) = 0.012W$

Maximum $T_A = 70°C$ (25°C is room temperature)

Pd is the power dissipation and is minimal with all outputs high, but increases rapidly in the low state. Normally, Pd is calculated with the equation CV^2f which increases with frequency(f), but for this device the thermal resistance is used as the value that varies with time. It is measured versus the duration of active low output time which raises the junction temperature of the die. Determining thermal resistance of the part in a system is estimated by the total amount of time that all 9 outputs are low. At 10 MBytes per second on the SCSI bus under normal conditions, the time the die is actually heated will be much less then 1 second and off the lower end of the chart (less than 30°C/W). This would cause junction temperature to be 104°C as given by:

$Tj = (30°C/W)\ (1.16W) + 70°C = 104.8°C$

assuming Ambient Temperature (T_A) is 70°C.

The Tj of 104°C predicts an MTBF of over 1800 years. If all outputs are stuck low and the die is heated to a steady state and reaches a thermal resistance of 107°C/W, the junction temperature will reach 194°C and MTBF will be unacceptable. To prevent damage to the device, the ML6509 has a thermal shutdown feature that disables the outputs when a junction temperature of 170°C is reached. A possible extreme scenario would be if all lines are stuck active low for 70 seconds and the ambient temperature is 70°C, then Tj is given by:

$Tj = 87°C/W)\ (1.16W) + 70°C = 170°C$

and then part thermal shutdown circuitry will disable the outputs.

GRAPH 1

This chart shows the plot of heating time versus thermal resistance. The Heating Time on the bottom axis represents the amount of time that all 9 outputs are tied active low which heats the die. Thermal resistance (θja) on the vertical axis increases over time and reaches a steady-state of 107°C/W after 500 seconds under zero airflow conditions. The corresponding die junction temperature rises according to the equation

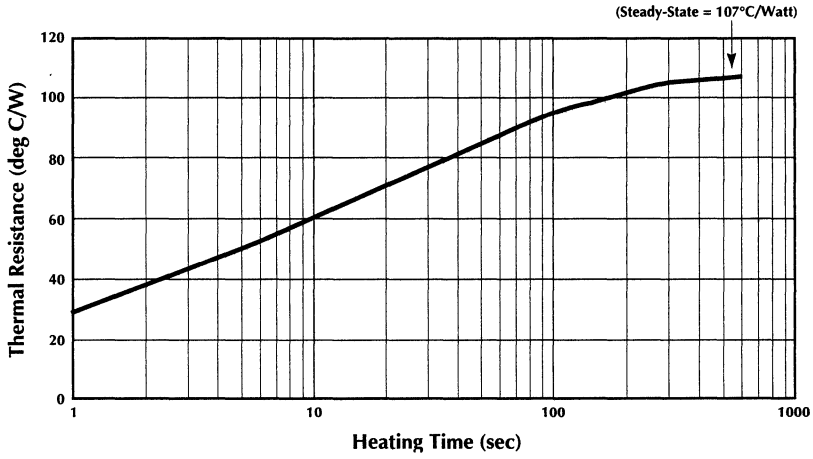
$Tj = (\theta ja)\ (PD) + T_A$

GRAPH 2

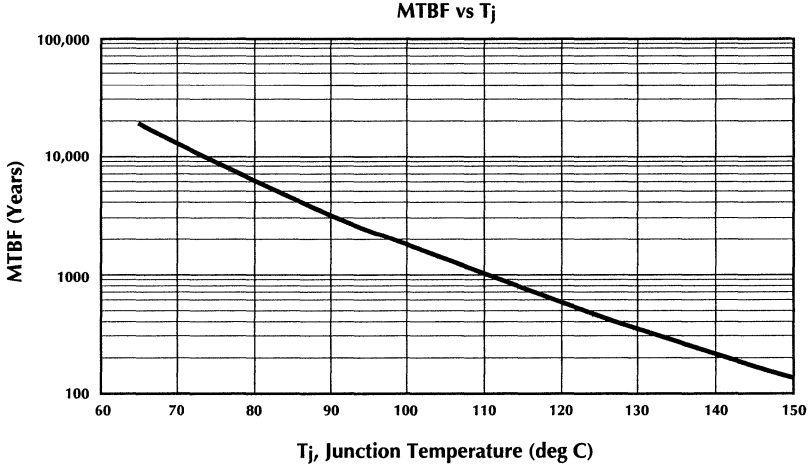
This chart provides the Mean Time Between Failures (MTBF) versus Junction Temperature (Tj). After calculating the average Junction Temperature at which the device will be operating, MTBF can be used to determine the effective lifetime of the device.

SUMMARY

The ML6509 Active SCSI Terminator offers the lowest capacitance (5 pF) in the industry today and is the only SCSI Terminator chip where the capacitance spec is guaranteed through production test. The ML6509 uses industry standard packages and supports an internal heat sink to handle the power dissipation. The data presented shows how the power dissipation issue can be handled and in the worse case the onboard thermal shutdown circuitry gets activated when the junction temperature reaches in the ballpark of 170°C hence preventing a catastrophic failure. Please contact Micro Linear's application engineering department, if you need any assistance with SCSI Terminators.



Graph 1. Shows the Heating Time vs Thermal Resistance (θ_{ja}) for the TSSOP package.



Graph 2. Shows the Mean Time Between Failures (MTBF) vs Junction Temperature (T_j) for the TSSOP package.

Application Note 26

Urs Mader
K. Kit Sum
Jim LoCascio

Power Conversion Efficiencies for Miniature Fluorescent Lamp

INTRODUCTION

Unlike an incandescent lamp, the fluorescent lamp requires a ballast to stabilize its operation. When considering power conversion efficiency of a fluorescent lamp and its ballast, the first thing to understand is the brightness in relation to the power consumed to obtain this brightness. However, the most efficient case is not necessarily the case for maximum brightness. In other words, the maximum efficiency case could be one of a brightness less than maximum, yet the ratio of brightness to power consumption is highest.

When measuring efficiencies of fluorescent lamps and ballasts, three efficiencies are of interest: (1) fluorescent lamp efficiency (Light Output/Lamp Power Input); (2) ballast efficiency (Lamp Power Output/Ballast Power Input); and (3) total system efficiency (Light Output/Ballast Power Input). However, because the ballast can affect the fluorescent lamp efficiency, the product of the fluorescent lamp efficiency and the ballast efficiency does not necessarily predict the total system efficiency.

Total system efficiency is of most interest to the system designer, but measuring absolute light output is not an easy task. However, relative light measurements are quite accurate. So, there are two things one can do: (1) Measure the ballast efficiency; and (2) Compare the system efficiencies of two ballasts with the same lamp running under identical conditions. In order for (2) to give meaningful results, the lamp must be operated at the same temperature, brightness and proximity to ground.

This application note will not delve into the details of brightness measurement, but will content with only disclosing this method of conversion efficiency evaluation.

LAMP EFFICIENCY

Fluorescent lamp efficiency is measured in lumens per Watt and is a function of temperature, age, brightness, proximity to ground and operating frequency. When measuring light output, these influences must be considered if consistent results are to be expected. When measuring ballast system efficiency, comparative measurements are made with the same lamp, brightness, temperature, and proximity to ground.

LAMP TEMPERATURE AND EFFICIENCY

Fluorescent lamp efficiency is measured in lumens per Watt and is a strong function of temperature. Lamp temperature is measured at the coldest spot on the tube, and is referred to as the "cold spot temperature." The following description provides some insight into the nature of the temperature dependence (see Figure 1).

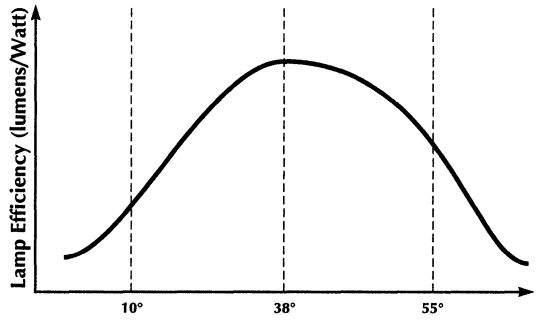


Figure 1. Temperature vs. Lamp Efficiency for Constant Lamp Power

Liquid mercury and other additive gases such as neon are present in the fluorescent tube. The mercury evaporates somewhat at room temperature and adds mercury atoms to the gas. The neon is essential for starting the lamp at cold temperatures when insufficient mercury is in the gas. After the lamp has ignited, the ionized mercury gas emits ultraviolet radiation which is converted to visible light by the fluorescent powder that coats the inside surface of the tube.

The mercury will condense on the coldest spot in the tube, and this "cold spot" will control the partial pressure of mercury in the gas. Since the partial pressure of mercury determines the amount of ultraviolet radiation produced, the temperature of the cold spot will have a direct effect on the amount of visible light produced.

Also, the conversion of ultraviolet light to visible light by the fluorescent powder becomes less efficient at high temperatures. However this effect is not as prominent as that of the mercury pressure. Most tubes have their maximum light output with their cold spot at 38°C.

LAMP AGE AND EFFICIENCY

The lamp efficiency is dependent on its total run time (Figure 2). The first 100 hours is referred to as the burn-in time and shows an increase in light output. This increase is due to the redistribution of liquid mercury within the tube. After the first 100 hours, the tube gradually grows dimmer until its end of life is reached. This second effect is due to the gradual degradation of the fluorescent powder on the inside surface of the tube.

Anytime the lamp's mounting geometry is changed, the cold spot may move to a new position on the lamp. If nothing is in contact with the lamp tube, the cold spot will be in the middle of the tube. If mounting clips are used to support the lamp, the cold spot will be at one or both of the mounting clips. Moving the cold spot will cause the mercury to redistribute; the redistribution is usually complete within 100 hours. For this reason, to make precise light measurements, it is preferable to mount the lamp in a fixed position. The lamp should "burn-in" in this position for 100 hours before making comparative measurements.

LAMP BRIGHTNESS AND EFFICIENCY

The lamp's efficiency is highest somewhere between maximum and minimum brightness (Figure 3). Therefore, when comparing system efficiencies, measurements should be made at identical brightnesses.

LAMP EFFICIENCY AND PROXIMITY TO GROUND

Miniature fluorescent lamps operate at high voltages (400V) and low currents (2mA). Under these conditions, capacitive leakage currents to ground are not negligible. These leakage currents conduct capacitively through the glass wall into nearby grounded metal objects such as the reflector. Lamp currents that conduct through the glass do not produce as much light as currents that pass through the entire lamp to the other electrode. Therefore, when making relative light output measurements, the same physical position of the lamp with respect to grounded objects is essential.

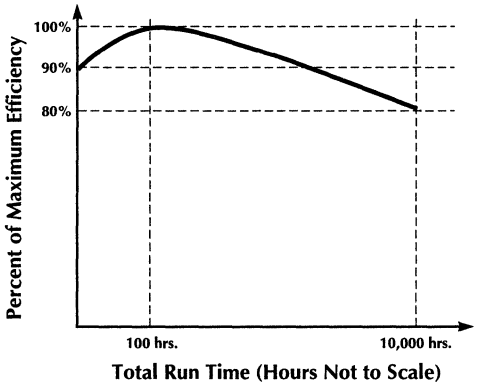


Figure 2. Lamp Efficiency vs. Total Run Time

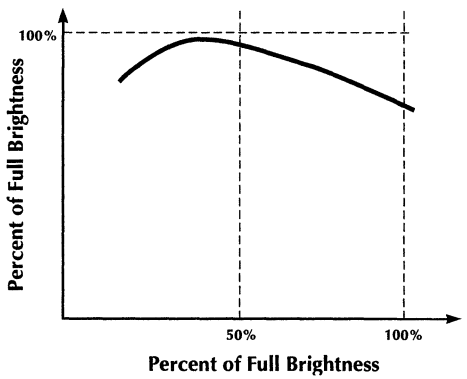


Figure 3. Brightness vs. Efficiency

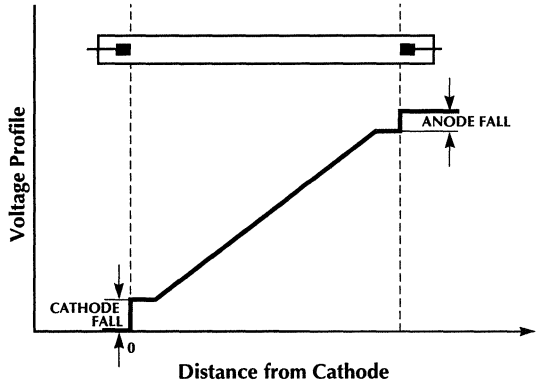


Figure 4. Lamp Voltage Profile

OPERATING FREQUENCY AND EFFICIENCY

To quantify the effect of operating frequency on lamp efficiency, an understanding about how electric current flows through the lamp is required. The lamp has two electrodes, the cathode and the anode. The cathode emits electrons into the gaseous space in the tube and the anode collects them at the other end. The movement of electrons from the gases to the electrodes requires work (energy) which is characterized by a voltage drop. The voltage drop between the cathode and the gas is called the cathode fall and the drop between the gas and the anode is called the anode fall. Light is produced between these regions; the ionized gas acts as a resistor and the voltage profile varies linearly along the length of the tube as is shown in Figure 4.

Cathode and anode fall voltages represent losses in the lamp because they do not produce light. These fall voltages are lower when operating the lamp at high frequency (greater than 10 kHz), thus resulting in more efficient operation.

Operation at low frequency (less than 1 kHz) allows the mercury plasma to ionize and recombine as the current in the lamp fluctuates over a cycle. This fluctuation causes the lamp to run at a lower efficiency.

High frequency lamp operation generally results in higher efficiency, however, operation above 10 kHz does not further improve the efficiency. In fact recklessly increasing the frequency beyond 10 kHz will only worsen capacitive leakage problems. Capacitive leakage not only has a negative effect on lamp efficiency, but also may interfere with other circuits.

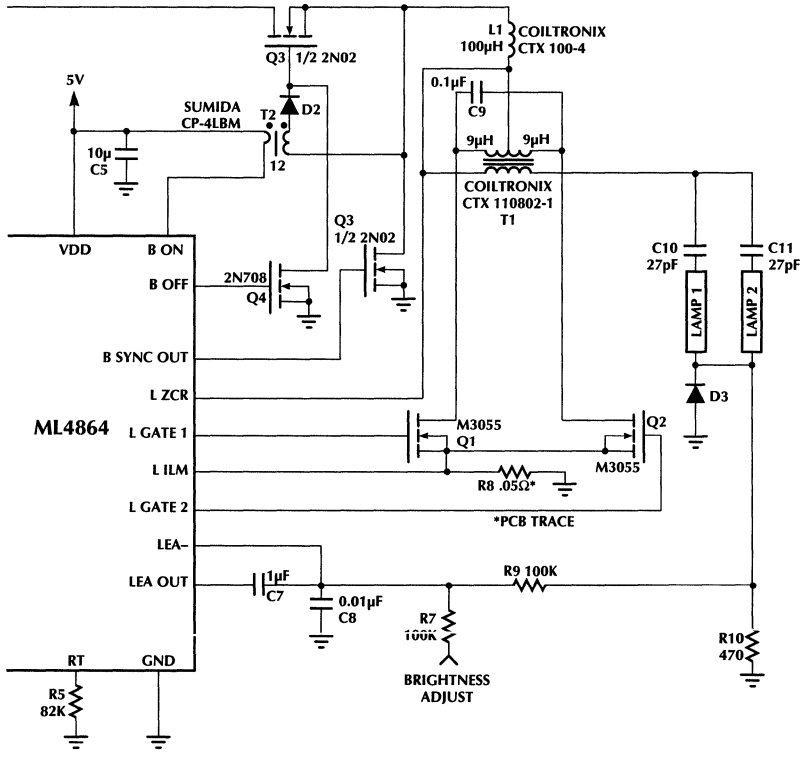


Figure 5. Typical Backlight Output Circuit

LIGHT MEASUREMENT GUIDELINES

The following is a list of guidelines for making good comparative system efficiency measurements.

1. Mount the lamp in a rigid, well defined structure.
   - — Make sure that points of contact with the tube remain stationary to avoid altering the location of the cold spot.
   - — Make sure that the lamp's position with respect to metallic objects is well defined. Be aware of the dominant capacitive paths to ground.
2. Burn-in the lamp by running it in the setup for 100 hours.
3. Monitor the ambient temperature. Be aware that measurements made in the morning may differ from those made in the afternoon depending on room temperature controls.
4. Allow the lamp to reach thermal equilibrium. This usually takes about 10 minutes.
5. Monitor the brightness. When comparing system efficiencies, adjust the ballast power to reach the same output brightness.
6. To make sure that ambient light does not interfere with the measurements, enclose the lamp in a light-proof container. Use the same container for lamp comparison.

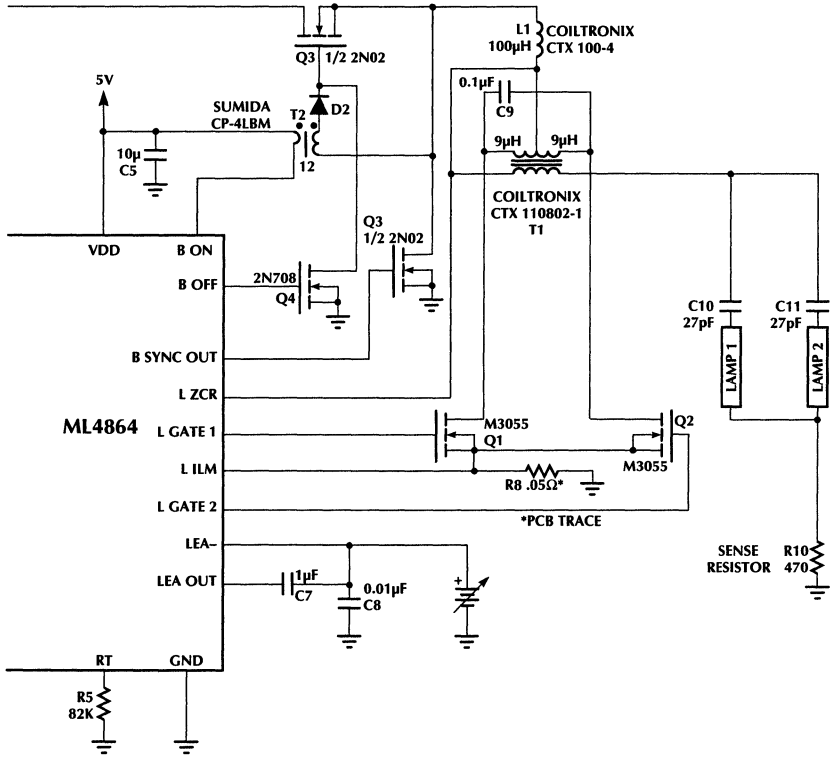


Figure 6. Loop Opened and Clamp Diode Removed

BALLAST EFFICIENCY MEASUREMENT PROCEDURES

POWER MEASUREMENT PROCEDURES

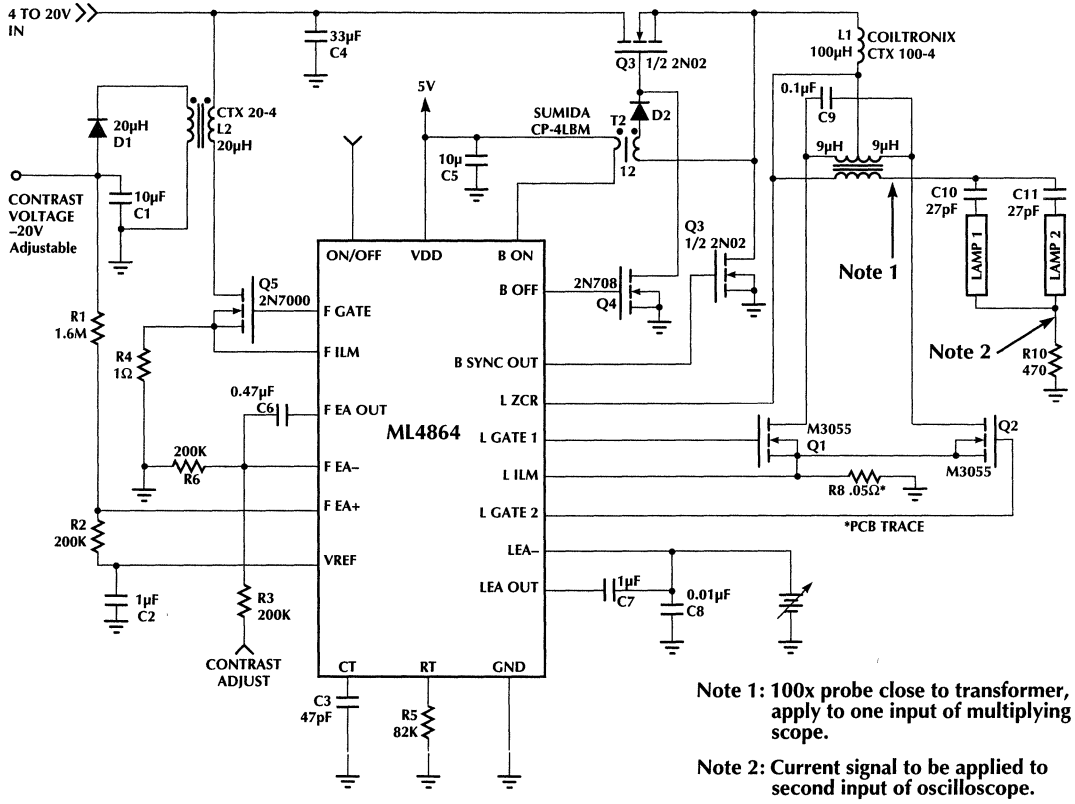
Power measurement is accomplished by a number of distinct operations to facilitate measurement of different quantities. The combined results of these measured quantities can then be used to arrive at the power conversion efficiency, which is the ultimate desired result. The ML4864 LCD backlight lamp driver circuit will be used as a vehicle for the description of this technique. Instantaneous power measurement will be made on the lamp circuit using the following procedures:

1. Open Loop

The first important quantity to measured is the lamp current. To measure the lamp current, the circuit shown in Figure 5 must be altered. The feedback loop signal is half-wave rectified and clamped by a diode. Because of this clamp diode, the lamp current signal is not a sinusoidal waveform and the current derived from the feedback circuit cannot be used for instantaneous power measurement.

Because of the non-sinusoidal waveform, phase difference and the effect of the clamp diode the following equation is true.

$V_{RMS\ OF\ LAMP} \times I_{RMS\ OF\ LAMP} \neq$ Instantaneous Lamp Power



Note 1: 100x probe close to transformer, apply to one input of multiplying scope.

Note 2: Current signal to be applied to second input of oscilloscope.

Figure 7. Probe Positions for High Voltage and Power Measurements

However, it is possible to obtain a sinusoidal lamp current waveform by simultaneously opening the control loop and removing the clamp diode.

The error amplifier circuit can be opened with a variable D.C. voltage source applied to the output of the amplifier to adjust the drive level of the open-loop system. See Figure 6.

2. Sense Resistor

The lamp current can now be measured by means of a single sense resistor. The current consumed by the lamp is now a true sinusoid, or at least as true as the high frequency resonant tank circuit can provide.

3. High Voltage Measurement

The high voltage is measured with a low capacitance 100X voltage probe applied to the high-voltage-end of the output winding of transformer T1 (Figure 7). The probe should be applied to the immediate vicinity of the winding (not on top of the output blocking capacitors of the lamps). This precaution will assure that the probe is applied at a low impedance point and that the probe loss will not significantly affect the accuracy of the measurement.

4. Power Measurement

Power measurement can be measured on a Tektronix Model 540 Digital Oscilloscope, or equivalent. The waveform obtained across the lamp current sense resistor is now a near sinusoid, and can be applied to one input of the oscilloscope. The voltage derived from the high voltage probe can be connected to the second input of the oscilloscope. A phase-correlated multiplication of the two input waveform will produce the power product, a quantity representative of the power consumed by the lamp.

5. Input Power Measurement

To facilitate more accurate input power measurement, and input filter should be inserted between the source and the ballast circuit to remove undesirable noise and interferences. The input D.C. current and voltage are then measured. The product of these two quantities is the input power.

6. Precautions in D.C. Measurements

If a D.C. current meter is connected between the input filter output terminal and the input terminal of the circuit board, the input voltage should be measured from the input terminal of the circuit board to ground. This procedure will guard against errors caused by the internal resistance of the current meter.

7. Input Power and Lamp Brightness

The ultimate goal of efficiency measurement is to identify the level of power input with the amount of light output. Unfortunately, lamp brightness is dependent on many factors external to the electronic ballast such as temperature of the lamp, age of the lamp, and location of the lamp with respect to ground. Therefore it makes a lot of sense to measure the power conversion efficiency of just the ballast. However, with identical electronics, the amount of light output will decrease with the advancing age of the lamp. Also, the method of drive can affect the amount of light output, regardless of its effect on lamp life.

Active SCSI Termination for Higher Reliability of Operation in Fast SCSI-2 and SCSI-3 Buses

Ram Gopalan

SCSI (Small Computer Systems Interface) is increasingly becoming a popular peripheral interface by virtue of its salient features which help to overcome the I/O bottleneck in computer systems today. With the increasing transfer speeds and cable lengths, come the associated transmission line effects, thus requiring termination. Passive termination schemes provided reliable operation in SCSI-1 systems, however meeting the promised performance goals of SCSI-2's fast SCSI at 10MB or SCSI-3's ultra fast SCSI at 20MB with any degree of reliability requires the use of active termination schemes. Higher speed, more peripherals and longer cables require the use of optimized active termination schemes on SCSI buses to maintain data integrity. This application note discusses the need for terminating a (transmission line) bus, the popular termination schemes and finally an optimized active termination scheme implemented through Micro Linear's ML6509, that helps achieve the goals of SCSI bus termination better with higher data integrity.

INTRODUCTION

The SCSI interface has evolved into a popular industry standard over the last couple of years. This is because the interface offers a cost effective means of boosting the I/O performance of mini and microcomputers. A flexible and versatile system, SCSI directs and manages the flow of information to and from up to eight devices per system, allowing each device to perform various functions simultaneously. The current SCSI-2 standard incorporates many specifications from the original SCSI-1 standard and additionally incorporates a number of enhancements, the most notable being the fast SCSI and wide SCSI options. These improvements coupled with the efforts of the ANSI committee on the proposed SCSI-3 standard, promise a bright future for SCSI.

SCSI devices are daisy-chained together using a common 50-conductor "A" cable and optionally, a 68-conductor "B" cable, making the signals common to all devices. Terminators applied at the ends of the cables assure communication-signal quality by matching the impedance encountered at the end of the cable to that of the cable itself. In other words, terminators at each end of the bus must have an impedance equal to that of the cable's characteristic impedance. Thus the pulse energy arriving at the cable termination is completely absorbed and none is reflected. Terminators may be connected either internally or externally to a SCSI device (refer Figure 1) Internal terminators are installed on the device's PC board. External terminators are built into connectors and encased in a connector shell. The terminators connector plug is then mated to a second rear-panel SCSI connector socket on the device as shown in Figure 1. Using internal terminators relieves the end user from worrying about terminations, especially with the advanced active terminators ICs available today that can be disconnected through software, however they do pose some difficulty to untrained users. External terminators eliminate the need to place internal terminators in every device because they are inserted only where necessary — at the ends of the bus. External terminators hence result in lower costs, easy identification and removal, and also provide a sturdy package to prevent damage, especially when reconfiguring the system.

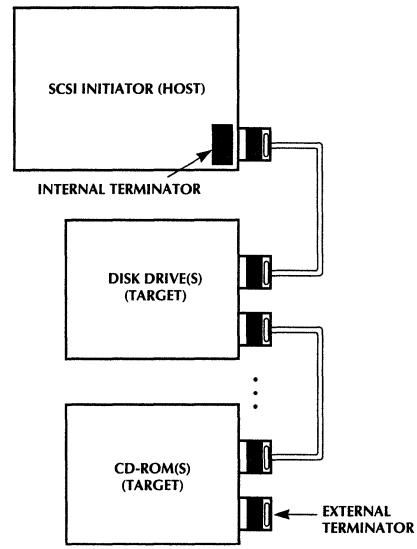


Figure 1. SCSI Bus Termination

With the advent of SCSI-2 and SCSI-3, it is clear that passive termination is often insufficient and must give way to active termination schemes. The SCSI-2 specification calls out for operation at 10MB over a 6 meter cable length (single ended, fast SCSI mode) while SCSI-3 is expected to up it to 20MB. The slower transfer rates of

SCSI-1 were very forgiving when it came to the physical interface. However with fast SCSI, stub lengths, the distance between stubs, cable designs and termination have become critical in order to get reliable operation. The primary problem is double clocking on the strobe lines which can occur as a result of reflection in the strobe lines due to impedance mismatches on the SCSI bus. One source of reflection is due to mismatch, when two cables of slightly different impedance are connected. Another source of reflection is stubs — the length of cable that hangs off the primary SCSI bus, (maximum allowed is 0.1m) and its position on the SCSI bus. Yet another source of reflection is the terminator, due to the difference between the impedance of the terminator and that of the line and its position, which is usually at the end of the cable. Most efforts by SCSI vendors are directed at the reflection problem using various termination techniques.

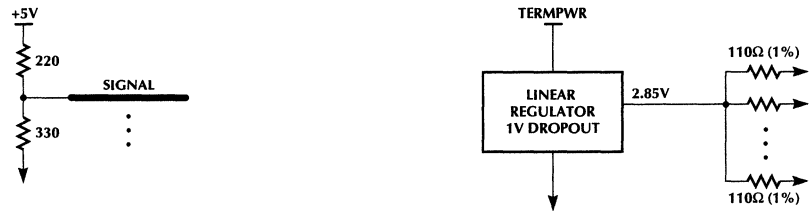
Active termination offers a potential solution to the reflection problem by attempting to address impedance mismatches by compensating for voltage drops and always maintaining a stable voltage to the terminating resistors. However, conventional active termination schemes have not proved to be effective with a fully loaded SCSI-2 bus. Another technique known as FPT (Forced Perfect Termination) uses the high speed switching capability of hot-carrier Schottky diode to approximate the "perfect" termination, however this technique currently exceeds the power guidelines presented in the SCSI-2 specification and hence is not usable.

Micro Linear has developed a MOSFET based active termination technique, which attempts to achieve a V-I characteristic that is close to the desired ideal characteristic, thus resulting in the realization of a "close to perfect" termination.

PASSIVE TERMINATION

The passive terminations used on single-ended SCSI-1 devices provided reliable operation even when fully configured systems were run at maximum cable lengths. SCSI bus lines are terminated into a resistive load consisting of a 220Ω (5%) connected to the TERMPWR line and 330Ω connected to ground, with an effective resistance equal to 132Ω, as shown in Figure 2. This technique has a number of disadvantages, the main one being that a resistive path always exists between TERMPWR and ground, hence dissipating power continuously, even when all the lines are negated. For a TERMPWR voltage of 4.8 volts, the terminator will dissipate 41mW per inactive line (8.6mA x 4.8V).

Another disadvantage of the passive termination technique is that the Thevenin voltage is not regulated and thus varies with TERMPWR. For a TERMPWR variation of 4.25V to 5.25V the output voltage varies from 2.55V to 3.15V. This creates a correspondingly large variation in the amount of current supplied to an asserted line through the 220Ω resistor. 1% resistors may be required to limit the amount of current supplied with a 5.25V TERMPWR line, to be less than the maximum specification called out by the SCSI standard. An added inconvenience of this technique is that disconnection of termination is a manual process. The main advantage of the passive termination scheme is that it offers low cost and low system complexity. However, meeting the promised performance goals of SCSI-2 and SCSI-3, with any degree of reliability, has turned out to be more difficult than anticipated. To cope with the more stringent requirements of SCSI-2, the standard recommends the use of active termination techniques like the one propounded by Paul Boulay.



Passive Terminator (Resistor Network)

Active Terminator (Boulay Type)

Figure 2. Termination Techniques

BOULAY TERMINATOR

The Boulay terminator, as shown in Figure 2, includes a voltage regulator as an active element. The voltage regulator provides a voltage source of 2.85V in series with a 110Ω resistor. This scheme is better suited to terminate lines with lower characteristic impedance, which is fairly common. Also the active voltage regulation improves noise immunity and a substantial reduction in average power dissipation is achieved because a negated or high impedance line conducts zero current through its 110 ohm termination resistor. Thus the only power dissipated is the 5–10 mA (typical) of current required to power the regulator.

Because the Thevenin voltage is regulated, the output current is for the most part immune to TERMPWR variations. However, in order to provide the maximum current permitted by the SCSI standard, without exceeding it, the 110Ω resistors must be 1%. If the resistors are incorporated on chip with the regulator, laser trimming is required, thus resulting in higher manufacturing costs.

To disconnect a Boulay terminator from the SCSI bus, it depends on whether the resistors are incorporated on chip or not. In the configuration where they are external, the resistor pack must be removed manually to achieve disconnection. In the configuration where the resistors are incorporated on chip with the regulator, an active switch is usually placed in series with each terminating resistor and a single pin is used to disable the regulator and open all switches.

The Boulay terminator overcomes many of the problems associated with the passive termination technique, thus resulting is more reliable system operation at higher speeds and over longer cables. However, the Boulay scheme is optimal only for a SCSI cable with a characteristic impedance of 110Ω.

TERMINATOR V-I CHARACTERISTICS

In the real world, however, 110Ω cables are few and far between. In a typical system, SCSI cable stock is in the 80 to 90Ω range and the impedance could even be lower for a heavily loaded bus. In a typical SCSI subsystem, the open collector driver, when asserted, pulls low and when it is negated, the termination resistance serves as the pull-up. A typical cable response for a pulse is shown in Figure 3. The receiving end of the cable will exhibit a single time delay, but when negated the initial step will reach an intermediate level, defined as V_{STEP}. The main problem of double clocking happens if the sampling occurs during this step portion. In order to get the most noise margin, the step needs to be as high as possible. V_{STEP} is defined as follows :

$$V_{STEP} = V_{OL} + (I_O \times Z_O)$$

where

V_{OL} = the Driver output low voltage
I_O = current from receiving terminator
Z_O = characteristic impedance of cable

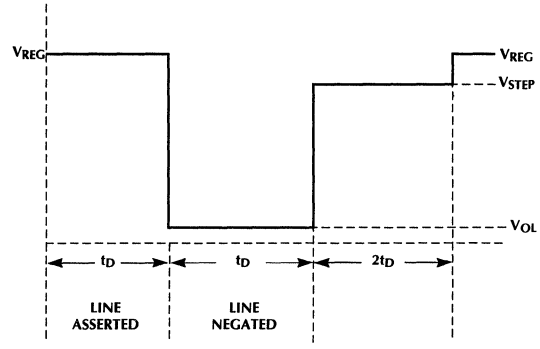


Figure 3. Cable response due to reflection

Lower impedance cables require a higher source current to achieve a sufficient voltage step when the traveling wavefront reaches the terminator end, from the driver impulse.

The V-I characteristics of the various termination schemes are shown in Figure 4. As can be inferred from this figure, a higher I_O suggests that the desired terminator V-I characteristics follow the 'ideal' V-I curve, i.e. 24 mA current source all the way up to 2.85V, for signal negation. However in the case of signal assertion, the 'ideal' curve poses a problem. This is because when the driver impulse wavefront reaches the terminator, it encounters what looks like a high impedance current source, which results in a large reflection back to the driver end, especially when the cable characteristic impedance is not 110Ω. This manifests itself as ringing in the middle of the line, in the case of middle of the line driver. Extensive simulation suggests that the Boulay V-I characteristic is desired for signal assertion transients, while the 'ideal' current source V-I characteristic is desired for signal negation transients. This implies that the V-I characteristics of the 'perfect' terminator falls somewhere in between, for optimum performance.

A terminator architecture which provides this type of V-I characteristic will have sufficiently better transient response for signal negations in systems with low cable impedances (Z_O). Signal assertion transients would be degraded somewhat but this can be partially offset with the use of appropriately designed negative clamping circuits. Interestingly enough the VDS-ID characteristic of a MOSFET transistor approximates this target characteristic, thus resulting in the design of an optimized active SCSI terminator like the ML6509.

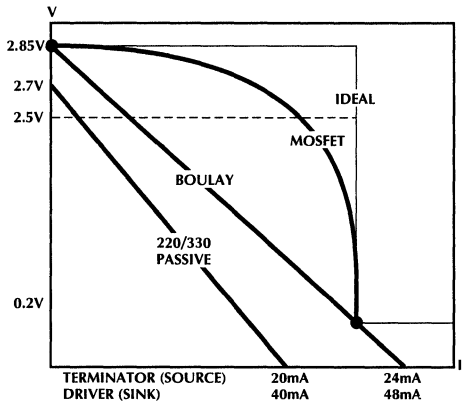


Figure 4. Terminator V-I characteristics

ML6509 - MOSFET BASED TERMINATOR

Architecture

This active SCSI terminator architecture also includes a voltage regulator as an active element (like the others discussed above), which provides a voltage source of 2.85V. However instead of 110Ω series resistors, MOSFETs are used, as shown in Figure 5. If a P-Channel MOSFET is biased in the triode region, it looks like a resistor most of the way down, to within VT of ground. If the P-Channel MOSFET were biased in the saturation region, it looks like a current source most of the way down. The VDS-ID characteristic of the MOSFET follows a trajectory that is in between the 'ideal' and the Boulay V-I characteristic, which coincidently happens to be the optimal characteristic desired to implement a 'perfect' terminator, as close as possible.

Operation

From an operating standpoint when a termination line is at high impedance, the MOSFET will pull the line up to 2.85V reference, since ID = 0. Feedback forces the ID = 24mA (max) when VD = 2.85V – 0.2V because this is what the reference MOSFET is biased at. In order to ensure the consistency of the V-I characteristic of this terminator, all the gates of the MOSFETs are tied together and require only one poly fuse trim resistor to trim the desired V-I characteristic. This work towards reducing the manufacturing cost significantly. Disconnection of the terminator from the SCSI bus is achieved by pulling a single gate line low. The line capacitance is typically less than 5 pF and the ML6509 is the only SCSI terminator to guarantee this specification. For more details on the capacitance and thermal issues associated with active SCSI terminators, please refer to Application Note 25.

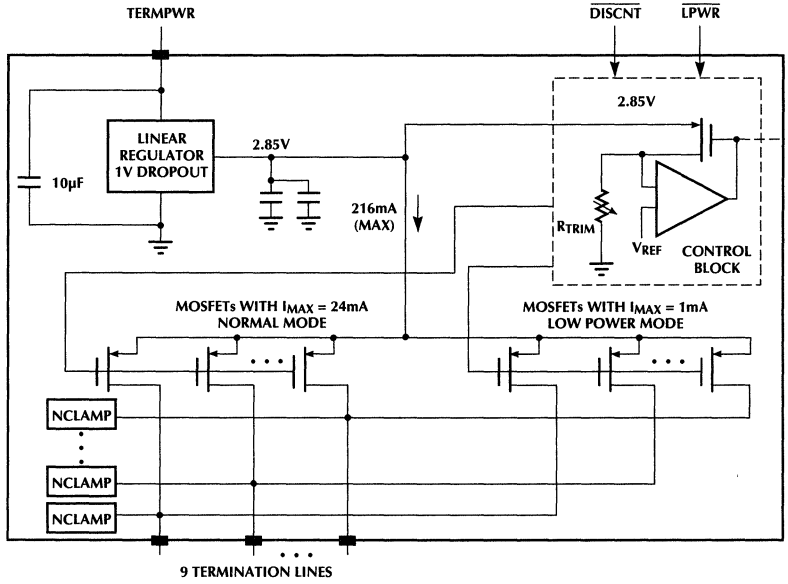


Figure 5. ML6509's MOSFET based active SCSI termination scheme

Lowpower Termination mode

With more and more notebook computers starting to offer SCSI on the motherboard and with the development of power conscious peripherals like the small form factor disk drives for such applications, even the lower power dissipation with conventional active termination schemes is not sufficient. In such applications, internal SCSI devices do not need the 24mA termination as the cables are short and the signals are very fast, hence transmission line effects are minimal. However when an external SCSI device is connected, the terminator needs to source the full 24mA current, to conform to the SCSI-2 specification. The MOSFET based active termination architecture essentially facilitates the offering of a lowpower termination mode implemented with smaller geometry MOSFETs (~1mA termination) biased by the same MOS gate reference voltage. This results in a very minimal silicon overhead, while the power dissipation is reduced by a factor of 24. With the help of a single pin ($\overline{\text{LPWR}}$), the termination can be switched to the full 24mA mode when connecting to an external SCSI-2 device.

OTHER FACTORS IN TERMINATION

There are a couple of other factors that are important with respect to active terminator solutions. These need to be taken care of to achieve the goals of a 'perfect' termination. Conventionally these were done with external components, however they are incorporated in the ML6509 chip, thus providing savings in real estate and cost.

Negative Clamp

A negative clamp circuit is essential to handle the signal assertion transients. This limits the amount of ringing when a line pulls low by sourcing additional current. It is not a violation of the SCSI-2 specification to source this additional current in a dynamic state, as long as the line doesn't settle on the clamp in the steady state. For this reason negative clamp circuits should start sourcing current when the line falls down close to ground (<0.2V). By default all active terminator implementations will provide some negative clamping due to the ESD diodes, but the turn-on is usually too low to make a difference.

Current sink capability

Most of the systems today use active negation drivers to drive the line back up to 2.85V, which is faster than if allowed to 'float up' through the resistor. Since the SCSI-2 specification allows the active negation driver to overshoot 2.85V to a maximum of 3.2V, in such a case current is sourced back through the termination element, thus requiring the regulator to sink current. Boulay terminators need to ensure that the regulator is designed to sink current, otherwise it will loose regulation. Even if the sink capability is implemented, it is limited to 3.5mA @ 3.2V overshoot, per line, as it is going through a 110Ω resistor. In the case of the MOSFET based terminator, current sinking is much better since the MOSFETs are biased in the triode region at 2.85V and they can sink up to 10 mA per line @ 3.2V and still maintain regulation.

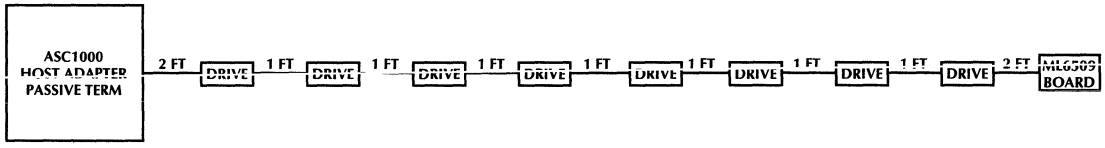
SYSTEM EVALUATION RESULTS

Some tests were done in the lab on a SCSI subsystem using ASP Inc.'s ASC1000 SCSI Host Adapter (which performs up to 12MB/s fast SCSI transfers and uses ML6509 active terminators) and also Adaptec's AHA1542 SCSI Host Adapter (which performs up to 10MB/s fast SCSI transfers). The host adapters were connected to a number of SCSI peripheral devices. These setups with the results are outlined below.

TEST 1

An full SCSI network was realized with a host adapter card having passive termination at one end, connected to seven SCSI disk drives daisy chained by 1 foot ribbon cables and the other end of the SCSI bus was terminated with a ML6509 eval board. The total cable length worked out to be 10 feet. The tests were done using both an Adaptec and ASP Inc. SCSI host adapter cards as the initiator. The signals were observed to be clean with 0.8V maximum low bounce and 2.5V minimum high ringing for a short duration.

10 FT SCSI RIBBON CABLE



Test 1

TEST 2

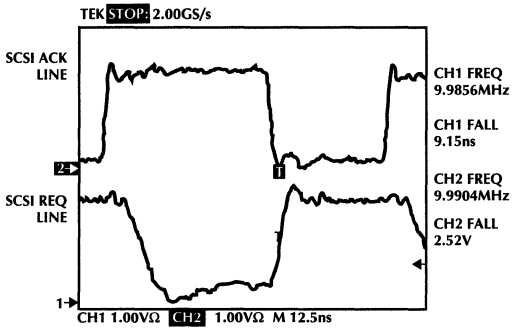
An ASC1000 SCSI host adapter with ML6509 based active termination was connected to a Maxtor 540 SCSI disk drive, with passive termination, using only a two feet SCSI ribbon cable. The REQ and ACK lines observed are shown. The terminator ensures that the signals are practically clean.

TEST 3

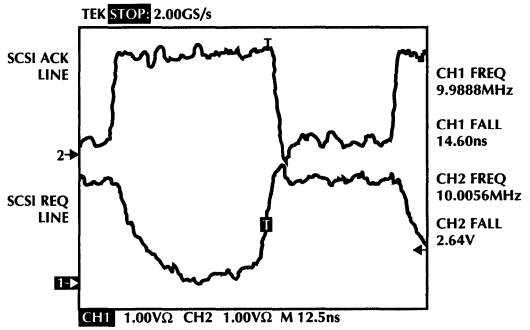
An ASC1000 SCSI host adapter with ML6509 based active termination was connected to a Maxtor 540 SCSI disk drive with passive termination, using a six feet SCSI ribbon cable. The REQ and ACK lines observed are shown. The effect of the slightly longer cable can be seen, however the terminator ensures that the signals are practically clean.

TEST 4

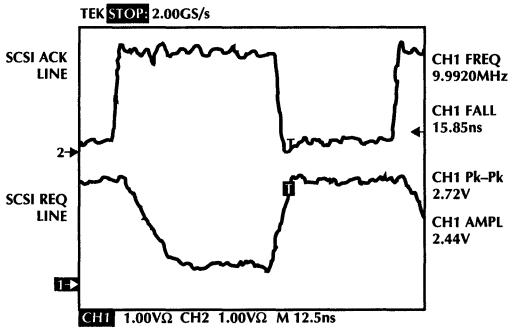
An ASC1000 SCSI host adapter with ML6509 based active termination was connected to three Maxtor 540 SCSI disk drive, with passive termination on the last drive, using a thirty feet SCSI ribbon cable. The REQ and ACK lines observed are shown. The terminator ensures that the signals are practically clean.



Test 2



Test 3



Test 4

CONCLUSIONS

In order to ensure a very high level of data integrity and reliability of operation in either the SCSI-2 or SCSI-3 bus environments, an optimized active termination technique that offers close to the 'pseudo perfect' termination for both signal assertion and signal negation is desired.

The passive termination technique is cheap but very far away from the desired V-I characteristics for signal negation and assertion. This starts making an impact especially with fast SCSI transfer rates and the utilization of full cable lengths.

The Boulay termination technique offers a characteristic that suits signal assertion but not quite what is desired for signal negation. A pure current source implementation could result in a characteristic that suits signal negation by following the 'ideal' curve however it is not quite acceptable for signal assertion.

The MOSFET based active SCSI termination technique implemented in the ML6509, discussed in this application note, attempts to realize a characteristic that is optimal for both signal assertion and signal negation.

A typical SCSI bus configuration using the ML6509 active SCSI terminator with the associated external components, is shown in Figure 6.

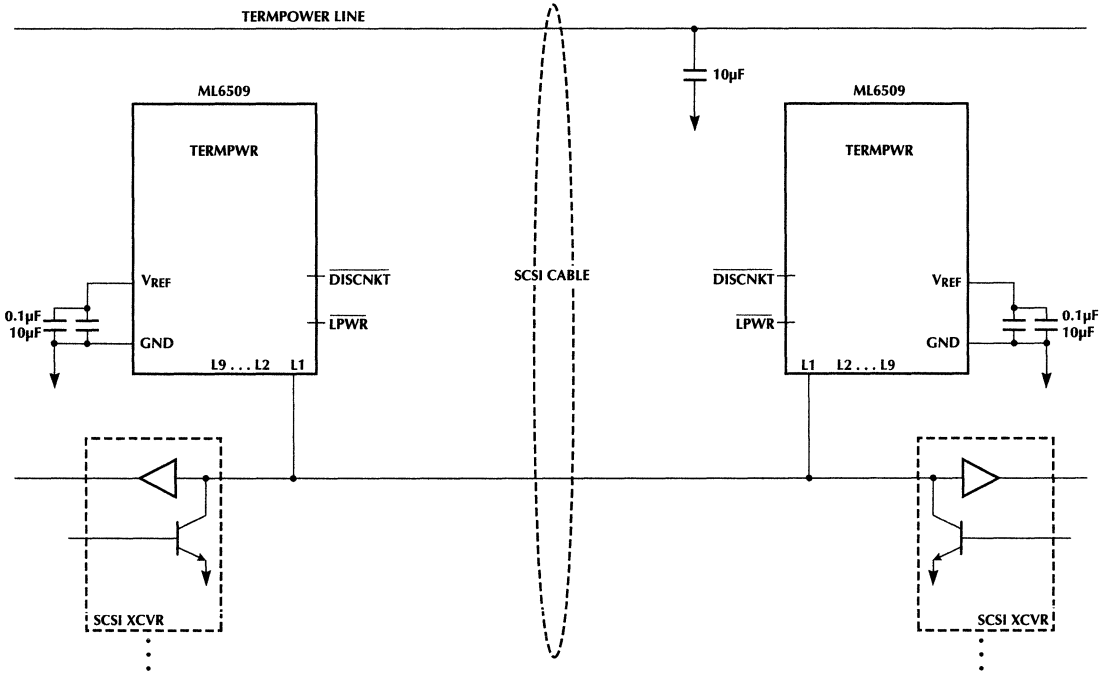


Figure 6. A typical SCSI termination configuration

Designing a 100MbP/s UTP Transceiver for Local Area Network

Manijeh
Fadaee

OVERVIEW

The ML6671 is a complete monolithic transceiver for 125 Mbaud MLT3 (Multi Level Threshold, 3 levels) encoded data transmission. The significance of this chip becomes evident when you consider today's requirement for wide-bandwidth transmission between computers and workstations. These computers, which may transmit applications involving color graphics, need high performance but a lower cost connectivity solution, with respect to FDDI. The use of UTP (Unshielded Twisted Pair) reduces the cost of a FDDI network by replacing expensive fiber optic cable and components with low cost copper wiring.

The key technical challenges in transmitting high speed data are controlling the emission and overcoming the bandwidth limitation of UTP. Therefore, in order to transmit data over UTP, the ANSI committee developed the X3T9.5 TP-PMD (twisted pair physical medium dependent) standard for twisted pair wiring. This standard allows the use of UTP category 5 and STP (Shielded Twisted Pair) cables in FDDI applications. To achieve the high transfer rates using these standards wires, three tasks must be performed: scrambling/descrambling, encoding/decoding and equalization. The latter two are performed by the ML6671.

The first requirement is a two level NRZI scrambling of the transmitted data. Once the data is scrambled to a two level NRZI and input to the chip, it gets converted to a multilevel threshold using the MLT3. After the data has made its journey through the twisted pair, the receiver uses adaptive equalization to compensate for phase distortion and level attenuation. The data is subsequently converted back to NRZI format and descrambled.

This application note will define these terms and standards and explain the benefits of each in achieving a low cost, high performance copper twisted pair network.

MLT3 LINE CODE

The MLT3 code is used for the FDDI-UTP network. MLT3 is very similar to the NRZI (Non Return to Zero, Inverted) code used in the existing fiber FDDI network. NRZI, is a two level unipolar code (0 and V) representing a "one" by a transition between two levels and a "zero" is represented by no transition as shown in Figure 1. MLT3 is a three level bipolar code (+V, 0 and –V) representing a "one" by a transition between two levels and "zero" as no transition as shown in Figure 1. Hence, the maximum fundamental frequency of the MLT3 is one-half that of NRZI. Figure 2 shows the power spectral density for MLT3 and NRZI. Essentially, the use of the MLT3 line code shifts much of the spectral energy to below 30MHz (as compared to NRZI). With the MLT3 coding scheme, 90% of the spectral energy is below 40MHz versus 70MHz for NRZI, which achieves the same data rate but does not require a wideband transmission medium.

One of the objectives of the ML6671 is to provide backward compatibility to existing FDDI PHY (physical layer controller) chip. Therefore, the interface of the ML6671 is intended to be compatible with the NRZI coded data provided by the FDDI PHY chip.

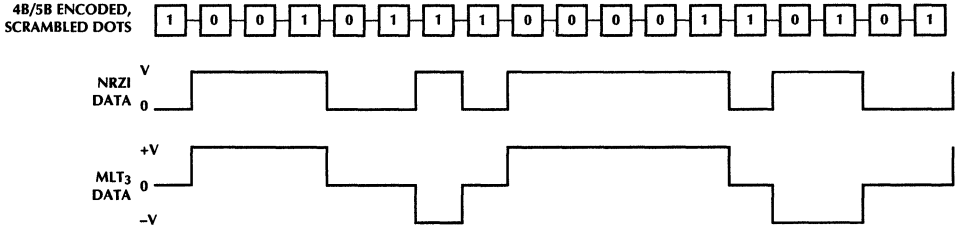


Figure 1. NRZI and MLT3 Waveforms

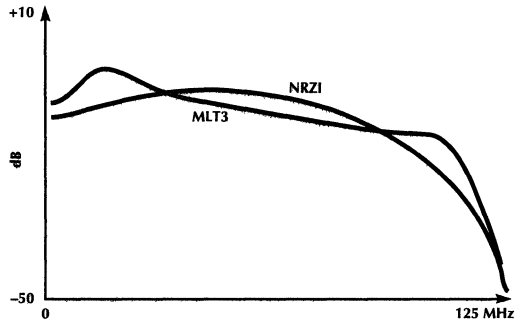


Figure 2. Power Density Spectra for NRZI and MLT

SCRAMBLING/DESCRAMBLING

In general, the robustness of a digital transmission system often depends on the statistical nature of the digital sources. For example, long strings of 0's and 1's can cause loss of the sychronization since the receiver clock is derived from the received data. Therefore, data must contain adequate transitions to assure that the timing recovery circuit will stay in sychronization.

FDDI allows for some repetitive data patterns that create energy peaks in the power spectral density of the line signal. These peak discrete spectral components are not desirable and must be suppressed.

The utilization of scrambling spreads these patterns and suppresses discrete spectral components by 20 to 25dB. This is due to the effect of randomization of the data and averages out the signal over a period of time. Thus, the peak energy is eliminated and emission improved. The ANSI committee has chosen Stream-Cipher scrambling as the technique for the FDDI-UTP network. The Stream-Cipher scrambler encodes a plain text NRZ bit stream by addition (modulo 2) of a key stream to produce a cipher text bit stream. It is implemented by adding an 11 bit linear Feedback Shift Register (LFSR) whose input bit is the exclusive-OR of its 11th and 9th previous bit, and which contains at least one non-zero bit. The shift register generates the key stream sequence which can be added to valid FDDI plain text streams with an average run length of approximately two consecutive zeros and a maximum run length of approximately 60 consecutive zeros.

Several commercial Stream-Cipher chips such as Motorola MC68834 and AMD 79C864 are available for FDDI UTP applications.

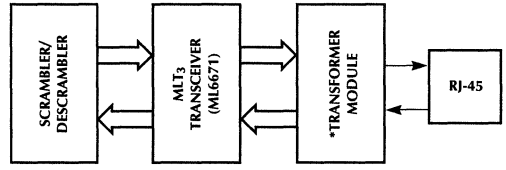
EQUALIZATION

During transmission of data over UTP distortion and ISI (intersymbol interference) are caused by dispersion in the cable. To overcome this signal corruption and distortion, the transmitted signal must be reconstructed from the incoming signal at the receiver. Equalization is used to overcome this signal corruption. However, the distortion is frequency dependent and loop length dependent. Since in most practical cases, the TP port characteristic is unknown and it is impractical to tune the equalizer specifically to each individual port. Hence, an adaptive equalizer is used in the TP-PMD standard to ensure proper compensation of the received signal.

By using an adaptive equalizer, the receiver automatically compensates for different lengths of cable without over equalizing or under-equalizing the line. The ML6671 monitors the energy of the received signal to determine the cable length and adjust the equalizer accordingly. The input signal level is inversely proportional to the cable length. Therefore, as the signal level decreases, the amount of equalization is increased to compensate for the line loss.

FDDI TP-PMD

The TP-PMD for the FDDI-UTP network is intended to be a physical replacement of the FDDI ODL (Optical Data Link) transceiver. It contains a scrambler/descrambler, a MLT3 transceiver (ML6671) and a filter-transformer module as shown in Figure 3. NRZI coded data is sent to the TP-PMD and the TP-PMD transmits the 125Mbit/s MLT3 coded data to the media. At the receive side, the MLT3 coded data is received and equalized and then is converted into NRZI coded data.



*Contact Belfuse or Pulse Engineering regarding Transformer Module
BEL Phone: (201) 432-0463
PULSE Phone. (619) 674-8198 or
(619) 674-8211

Figure 3. Block Diagram of the TP-PMD

Transmit Function

The ML6671 receives an NRZI code bit stream, which is at positive differential ECL (PECL) levels at the TXIN inputs. PECL level scrambled NRZI data is received by the ML6671 and then converted into MLT3 line code. The current driven transmitter then sends the data to the filter/transformer module. Since the output structure of the twisted pair drivers is current driven, it has the following advantages when driving the UTP medium:

- The differential outputs are well matched for balanced signal transmission. Balanced transmission is crucial for meeting tight regulations on signal shapes.
- Current driven outputs produce lower common-mode voltages for a lower EMI radiation. This can be a very significant issue in meeting FCC regulations.
- The output drive can be easily adjusted to compensate for losses in the transformer-filter module.

An external resistor between pin 17 and 18, RTSET1 and RTSET2, sets the output level. The value of the resistor across pins 17 and 18 is as follows:

$$RTSET = \frac{64 \times 1.25}{I_{OUT}}$$

For FDDI UTP applications, the ANSI X3T9.5 standard specifies the transmit voltage amplitude to be $2V_{P-P}$ or 1V ± 60mV. The UTP connection requires a termination impedance of 100Ω, each transmitter output is terminated by one 50Ω (R_L) resistor to provide the 100Ω termination impedance. Therefore,

$$I_{OUT} = \frac{2V(P-P)}{R_L} = \frac{2V}{50\Omega} = 40mA$$

The value of RTSET is

$$RTSET = \frac{64 \times 1.25}{40mA} = 2K$$

Using a 2K resistor sets the transmit level to 1 Volt peak with a rise time of 1ns between the levels of 10% and 90%.

The transmitter may be disabled by the TXOFF pin When this pin is pulled low, the transmitter's output goes to its center value ($I_{OUT}/2$) with no differential current flowing through the transformer.

Receive Function

The receive circuit of the ML6671 consists of an adaptive equalizer and MLT3 to NRZI converter. The equalizer adjusts its gain and frequency response as a function of the received signal. The equalization level is based on the energy level of the received signal. As the signal level decreases, due to higher attenuation by a longer cable, the amount of equalization is increased. The equalizer is designed to operate over a distance of 0 to 100 meters of category 5 type cable.

The ML6671 detects the MLT3 coded signal from the filter transformer module signal and activates the SD ± output signal when the input is above a preset the voltage level.

This preset voltage threshold level is 25% of the maximum equalization setting.

After the signal is equalized, it is converted to NRZI. *The ML6671 sends data out in NRZI form.*

An external resistor across RTH1 and RTH2 is used to set the internal equalization and signal detect levels. This resistor should be set to match the peak to peak transmit amplitude which is effected by the different magnetics. RTH can be calculated as follows:

$$RTH = \frac{V_{AMP} \times RSET}{20}$$

The V_{AMP}, peak to peak amplitude of transmit output with zero length cable, is 2V.

$$RTH = \frac{2 \times RSET}{20} = \frac{RSET}{10}$$

Thus, we can solve the RTH value since RSET is 5K

$$RTH = \frac{5K}{10} = 500\Omega$$

Link Status Function

The ML6671 monitors the line integrity and detects linkage with the signal detect circuit. A differential output pair SD± to the host indicates the status of the link. They are active when a data signal is presented with an amplitude exceeding a preset threshold. Otherwise, the signal detect circuit drives SD+ low and SD– high indicating an invalid link.

Loopback Function

Loopback is controlled through the LPBK pin coming from the PHY chip. When this pin is high, loopback is enabled. During loopback, the transmitted data from TXIN± does not transmit to the TXOUT±. Instead it is looped back to the receive data RXOUT± by an internal mux.

TP-PMD CIRCUIT FOR FDDI-UTP

Figure 4 shows a complete schematic of TP-PMD circuit using ML6671 with an external filter-transformer module. This TP-PMD transceiver is designed to replace an existing 1402U ODL FDDI transceiver. The external resistors and capacitors are chosen to meet the following conditions:

ECL Line Terminations

RXOUT± and SD± are emitter-followers generating positive ECL (PECL) levels when terminated by a pair of resistors. The resistors form a thevinin equivalent 50Ω termination. The following two equations are used to calculate the values of these resistors:

$$R_b = 2.6 \times Z_O = 2.6 \times 50\Omega = 130\Omega$$

$$R_a = \frac{R_b}{1.6} = \frac{130\Omega}{1.6} = 81\Omega$$

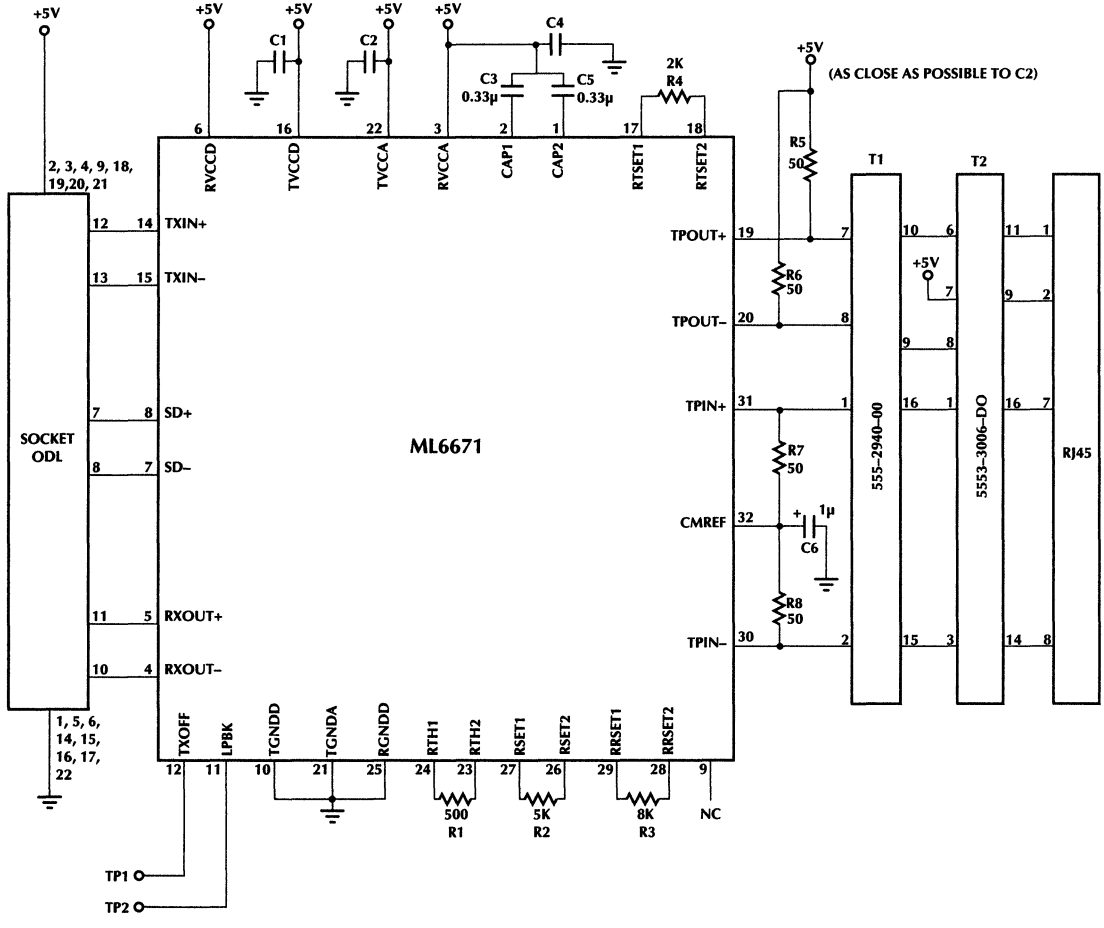


Figure 4. Schematic of the TP-PMD using the ML6671

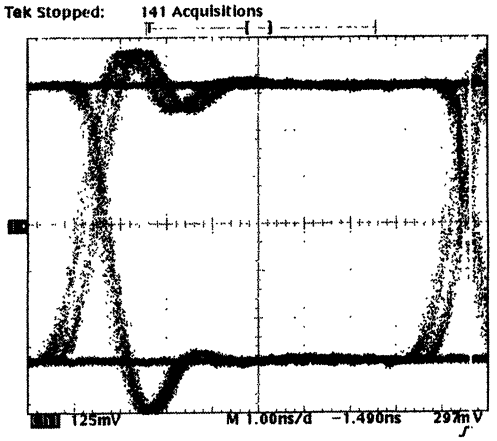


Figure 5. MLT3 Eye Pattern from the ML6671 Eval Board (0 meter UTP cable)

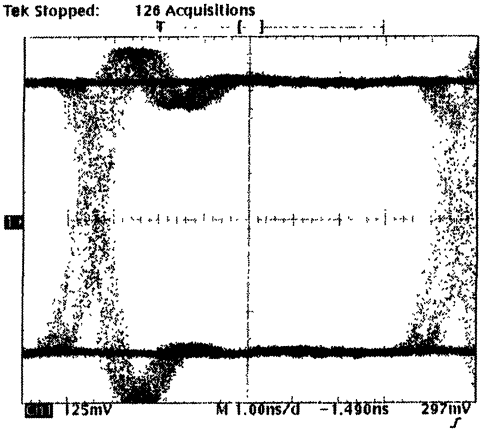


Figure 7. MLT3 Eye Pattern from the ML6671 Eval Board (50 meters UTP cable)

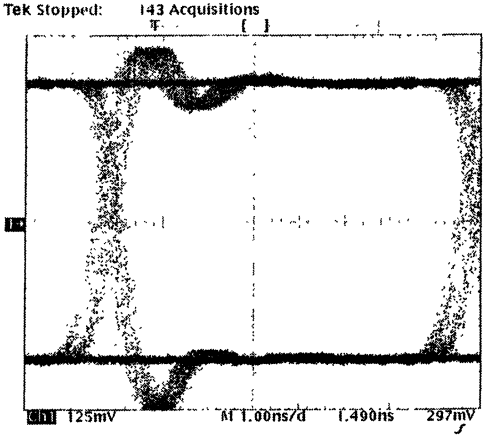


Figure 6. MLT3 Eye Pattern from the ML6671 Eval Board (25 meters UTP cable)

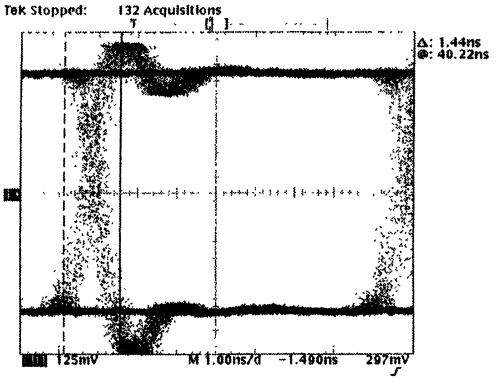


Figure 8. MLT3 Eye Pattern from the ML6671 Eval Board (110 meters UTP cable)

The same concept applies to the TXIN± outputs coming from the PHY. RXOUT±, SD± and TXIN± are not terminated in the TP-PMD schematic since they are terminated at the other end in the adapter cards and concentrator boards.

Media Termination

Two 50Ω resistors at TPOUT± and TPIN± implement 100Ω terminating impedance for UTP when looking back through the filter-transformer module. The TPOUT± must be terminated by a 50Ω resistor to +5V.

Common Mode

The received signal coming from UTP at TPIN± must be biased by the CMREF pin as shown in the schematic.

Equalizer and Link Detect Timings

- Two matching capacitors at CAP1 and CAP2 (0.33µf) set time constants to control for the adaptation of the equalizer loop and signal detect. The value of these capacitors should be large enough to handle the maximum run length which is 60 zeros for the FDDI-UTP. In addition, the Signal Detect output (SD±) should be asserted within 25µs to 1000µs for FDDI-UTP. This value is adjustable for different maximum run lengths and assertion times for other applications such as fast ethernet (100Mbps). Smaller capacitors cause faster response time.
- The resistor across RRSET1 and RRSET2 sets the time constants controlling the equalizer's transfer function. A 5K, 1% resistor across these pins limits the cable length to 100 meters while an 8K, 1% resistor expands the cable length to 130 meters.
- A 500Ω resistor across RTH1 and RTH2 sets the internal level for equalization and the signal detect circuit as explained previously in the receive function of the ML6671.

PERFORMANCE DATA

The ML6671 evaluation board provides access to all receive and transmit signals and waveforms required to test and evaluate the ML6671. As shown in Figures 5 to 10, the ML6671 meets the FDDI twisted pair standard.

Receive waveforms

The ML6671 eval board operates with different cable lengths. Figures 5, 6, 7 and 8 show the typical eye pattern of the NRZI signal at the RXOUT+ pin recovered by the adaptive equalizer for different cable length (from 0 to 110 meters). Regardless of cable length, the jitter is held below 3.0ns which is required by the standard.

Transmit Waveforms

Figure 9 shows a twisted pair template for the eye pattern of the differential output voltage during transmitting alternative one and zero (55). This figure also shows the TP-PMD waveform template superimposed over the measured waveform.

Output waveform droop is the decay of transmit output voltage following a signal transition from baseline to peak voltage. The output waveform droop should not exceed 3.0% of the differential transition voltage amplitude (neglecting overshoot). The waveform droop, measured at the output of the transformer (S553-3006-D0), meets the requirement for the standard as shown in Figure 10.

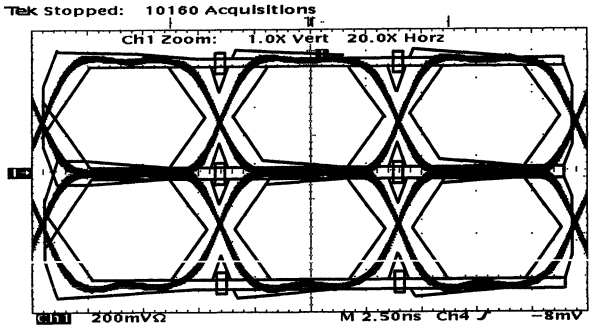


Figure 9. Twisted Pair Active Output Interface Template of the ML6671

Typical rise and fall time of the transmit output after the transformer is about 2ns as shown in Figure 11. Timing for the rise and fall time has not been finalized by the current draft of the FDDI twisted pair standard.

LAYOUT CONSIDERATIONS

To obtain optimum performance from the FDDI-UTP transceiver, careful attention must be given to the layout of the board. The routing of sensitive input traces relative to other components and traces must be considered in great detail. Data lines must be controlled impedance and properly terminated to minimize reflection that might degrade performance. Power supply pins must be protected from noisy operating conditions by proper filtering. To achieve this, the following should be considered:

- A two layer printed wiring board with a large ground plane on the component side should be utilized.
- To minimize the coupling of unwanted noise into the receiver, the receiver pins and traces connected to them should be shielded by placing a ground trace between the receiver's pins and connecting traces and other high-level paths. If shielding is not possible, route the transmitter-input traces and other traces carrying high-level signals as far away as possible from the receiver pins.
- When laying out the traces for the data lines (TXD, RXOUT, SD), signal lines should be kept as short as possible to minimize ringing and overshoot, as well as to simplify timing considerations arising from the propagation delay of a signal along a conductor. Ringing and overshoot are due to the intrinsic inductance and capacitance at the end of the line. Intrinsic inductance and capacitance are reduced by shortening the lines. The same concept applies to the TPOUT and TPIN high speed input and output signal lines.
- Each ECL data line should be terminated at the end of the line and should have a bypass capacitor, 0.01 to 1μF, on the voltage side of the resistor for each termination resistor. The termination helps to minimize the reflection due to mismatch.
- Try to avoid controlled impedance interruption (i.e., 90 degree bends) on all high speed lines. PC traces should be treated as transmission lines with continuous ground plane or power plane beneath each line.
- All 50Ω termination resistors at TPIN and TPOUT should be placed as close as possible to the pins of the ML6671.
- All paired lines (differential pairs) should have equal length, specially TPOUT traces
- The resistor across RTSET1 and RTSET2 should be 2K, 1% and next to the pins.

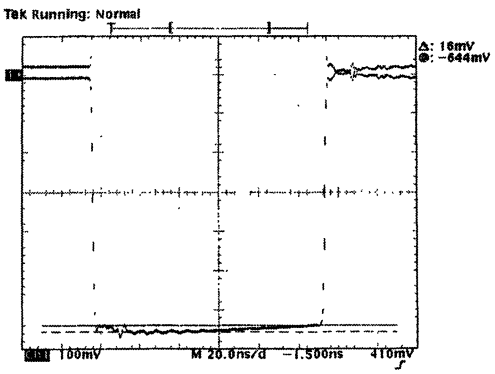


Figure 10. Output Waveform Droop

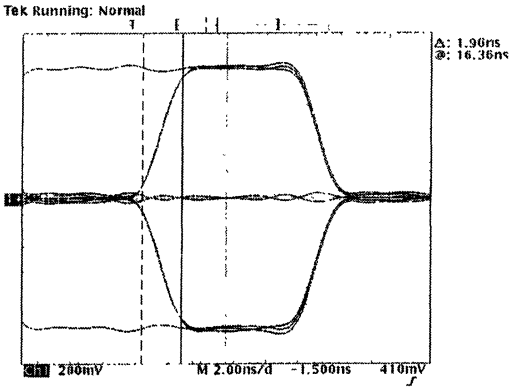


Figure 11. Rise and Fall Time of the Output Transmit Signal from the ML6671 Eval Board.

Application Note 29

Choosing an Inductor for Your ML4861 Application

Joe Vanden Wymelenberg

INTRODUCTION

When designing a power supply with the ML4861, inductor selection is the most important aspect of the design. The inductor plays a major role in determining maximum output current, system efficiency, radiated noise and the physical size of the circuit. And since the ML4861 requires only one or two other external components, the inductor can be a significant portion of the total cost of the power supply circuitry. The purpose of this application note is to familiarize you with the tradeoffs involved when choosing an inductor for your ML4861 design.

Before you start, you need to know some details about the system in which the part is being used. Specifically, you need to know the minimum and maximum input voltage, and the maximum current required at the output. If you're using standard alkaline batteries as your input, you can usually assume the batteries will operate at between 1.0V and 1.5V per cell. NiCad's and NiMH's usually operate over a tighter voltage range, so if the final user can swap-in different types of batteries the alkaline range is a good one to use.

INDUCTOR VALUE

The inductor value is set by the maximum output current required. Smaller values of inductance deliver more output current, but also require higher peak currents, which will cause efficiency to be lower. Therefore, it's important to choose the value of inductance that's just small enough to deliver the maximum output current under worst case conditions.

In Figure 1, the maximum output current of the ML4861-5.0 is shown as a function of input voltage. The curves represent different inductor values, from 10µH to 68µH. These are typical performance curves, so you'll need to give yourself some margin when using them to account for variations in inductance, efficiency and on time. If you don't have a good feel for how much these parameters might vary, use a 50% overbuild by multiplying your required maximum output current by 1.5.

To select the appropriate inductance, find the minimum input voltage on the horizontal axis. Then move vertically up to your maximum output current. The correct inductor value is indicated by the curve that is just above this worst case operating point. For example, let's say I have a two cell application where my maximum load current is 100mA. Giving myself 50% margin, I'm going to use 150mA as my maximum output current. A two cell input means my input voltage may drop to as low as 2.0V. Finding 2.0V and 150mA in Figure 1, I see that 18µH should be just low enough to satisfy my output current needs.

Maximum output current curves are also provided for the ML4861-3.3 and ML4861-6.0, and a 4.0V application of the ML4861-ADJ, in Figures 2 through 4. Below each of the Figures, in Tables 1 through 4, are the actual data plotted in the curves. Note that all output current curves are limited by a maximum output current of 500mA. This reflects the fact that the ML4861 was only designed to deliver up to 500mA of average output current. Operating at higher currents may reduce the operating life of the part and is not recommended (see the ML4861 data sheet).

EFFICIENCY

Typical efficiency curves for the ML4861 are shown in Figures 5 through 8. Input and output capacitors with 100mΩ of ESR were used and inductors had approximately 5mΩ of resistance per µH of inductance. In Figure 5, it can be seen that the efficiency achieved is primarily determined by the inductor value. Since switching currents increase linearly with input voltage, you might expect efficiency to drop off significantly at higher input voltages due to I-squared R losses. But higher resistive losses are counteracted by the fact that output power is also increasing as the square of the input voltage, and the ratio of losses to output power tends to remain fairly constant.

Efficiency is primarily set by resistive losses in the inductor, input and output capacitors, and the ML4861, and by core loses in the inductor. Since lower efficiency has an impact on the maximum output current, it's important to take another look at the inductor value chosen if your components have significantly higher resistance than what's described above, or the inductor is run beyond its maximum DC current rating. If your efficiency is significantly lower due to any of these effects, give yourself more output current margin by choosing a lower inductor value.

The inductor value should be between 10µH and 68µH. If an inductor value less than 10µH is chosen, the efficiency will be less than 75%, due to high peak inductor currents. At an inductance of 68µH the efficiency is about as high is it will get, somewhere between 90% and 95%. Using a higher inductance won't improve efficiency because switching losses in the ML4861 start to dominate the performance. Also, at inductances above 100µH, the ML4861 begins to have difficulty detecting the smaller inductor currents during synchronous rectification. Since higher inductance is usually associated with larger size and higher cost, this limit shouldn't be perceived as a compromise to the ML4861's performance in any application.

INDUCTOR CURRENT RATING

Inductors have energy ratings just like resistors have power ratings. It's important not to operate an inductor beyond its capabilities. Doing so may saturate the core and cause the inductor current to run away. In some cases the series resistance of the system will prevent this from occurring.

Knowing the maximum input voltage and the inductance, the peak inductor current can be estimated with the equation:

$$IL_{PEAK} = V_{IN(MAX)} \times \frac{T_{ON}}{L}$$

For our two cell, 100mA application, this current turns out to be about 1.67A.

When examining the current ratings of inductors, keep in mind that resistive components of the circuit tend to reduce peak inductor currents. In most cases, resistive components will drop the peak current to around 70% to 90% of this value. Also, large inductor currents tend to draw down the battery voltage significantly, further reducing this peak current, especially if a smaller input capacitance is used.

In most cases it's a good idea try several types of inductors, even some with lower current ratings. Look at the inductor current with a current probe at maximum input voltage. If the slope of the inductor current seems fairly constant, and not running away, you may want to use this inductor and live with any efficiency losses in order to reduce the inductors size and cost.

INDUCTOR RESISTANCE

In order to maximize efficiency, inductor resistance must be kept to a minimum. In general, the higher the inductor value, the higher the number of turns required and the higher its resistance. A figure of merit for inductors is the amount of resistance per µH of inductance. A good inductor will have less than 10mΩ/µH. Note that inductor resistance isn't always specified tightly, so a 10µH inductor may typically have only 50mΩ of resistance, even though it's only guaranteed to have less than 100mΩ

As before, there is a tradeoff to be made between size and efficiency. Smaller inductors also tend to be lower cost, but have higher resistance and lower efficiency. Try several types of inductors before deciding which one to use.

NOISE CONSIDERATIONS

A final issue that needs to be addressed is switching noise created by the regulator that finds its way into other sensitive, low level circuits nearby. Noise can couple into other circuitry in several ways.

Inductive coupling is said to occur when high currents in one trace couple magnetically, like a transformer, to an adjacent trace. And what better way for this to occur than through a sensitive trace located near the inductor of an ML4861 power supply. Inductors with large air gaps are typically more prone to this kind of problem, so if you have a sensitive circuit that needs to be nearby you should use a toroidal inductor, or a bobbin inductor with a ferrite sleeve.

Another way switching noise can couple into neighboring circuitry is through ground loops. This problem occurs when high switching currents in the power supply are conducted to a common ground through slightly resistive traces. High current transients can cause the ground to bounce due to these resistive drops. Care must be taken not to have power supply and small signal circuitry share the same ground trace. A similar argument can be made when laying out the output trace. In either case, the problem is reduced by lowering inductor currents, so choose the inductor value as high as possible.

The high frequency components of high slew rate switching voltages, such as that found on the V_L pin, can radiate through the air to other circuitry sensitive to RF. Since high slew rate voltages are necessary for efficient operation, the best technique for reducing this type of noise is to reduce the size of the antenna by keeping the V_L node as small as possible. Another RF reduction technique is to place a grounded conductive shield around the offending circuitry. In either case, you may want a smaller size inductor to keep the power supply layout tight.

SOURCES OF SMALL SURFACE MOUNT INDUCTORS

We've taken most of our measurements on the ML4861 using Sumida inductors, which seem to offer a good compromise between size and cost, versus efficiency and current handling capability. Most commonly used were the CD75, CD54 and CD43, and for low noise the CDR74B, CDRH64, and CDR63B types. Coiltronics and Dale also makes suitable inductors. These suppliers can be reached at the following numbers:

Sumida	(708) 956-0666
Coiltronics	(407) 241-7876
Dale	(605) 665-9301

	INDUCTANCE (µH)										
V_{IN} (V)	10	12	15	18	22	27	33	39	47	56	68
1.0	62.2	54.8	46.3	40.1	34.0	28.5	23.9	20.5	17.3	14.7	12.3
1.2	88.8	78.3	66.3	57.5	48.8	41.0	34.3	29.6	24.9	21.2	17.7
1.4	119.8	105.8	89.8	77.9	66.1	55.6	46.7	40.2	33.9	28.9	24.1
1.6	155.0	137.1	116.6	101.3	86.1	72.5	60.9	52.5	44.3	37.7	31.4
1.8	194.3	172.1	146.6	127.5	108.5	91.4	76.9	66.3	56.0	47.7	39.8
2.0	237.6	210.7	179.7	156.5	133.4	112.5	94.7	81.7	69.1	58.9	49.1
2.2	284.4	252.7	215.9	188.2	160.6	135.7	114.3	98.7	83.5	71.2	59.5
2.4	334.8	297.8	254.9	222.5	190.1	160.8	135.6	117.2	99.2	84.6	70.7
2.6	388.3	345.9	296.6	259.2	221.8	187.8	158.5	137.1	116.2	99.2	82.9
2.8	444.7	396.7	340.7	298.2	255.5	216.6	183.0	158.5	134.4	114.8	96.1
3.0	503.5	449.8	387.0	339.2	291.0	247.0	209.0	181.1	153.8	131.4	110.1
3.2		504.8	435.1	381.9	328.1	278.9	236.3	205.0	174.2	149.0	124.9
3.4			484.5	425.9	366.5	312.0	264.7	229.8	195.5	167.4	140.4
3.6			534.6	470.6	405.6	345.9	293.9	255.5	217.5	186.4	156.6
3.8				515.3	444.9	380.0	323.4	281.5	240.0	205.9	173.2
4.0					483.3	413.5	352.5	307.3	262.4	225.4	189.8
4.2					519.0	445.0	380.1	331.8	283.9	244.3	206.0
4.4						471.7	403.8	353.32	302.8	261.1	220.6
4.6						488.2	419.0	367.3	315.7	272.8	231.2
4.8						478.2	411.3	361.5	311.6	270.1	229.7

Table 1. ML4861 Maximum Output Current (mA), V_{OUT} = 5V.

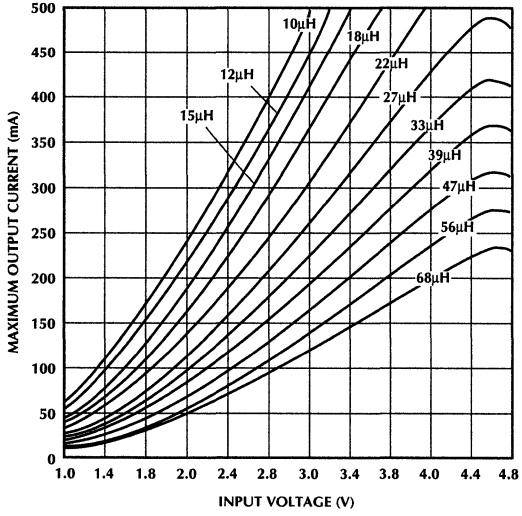


Figure 1. ML4861 Maximum Output Current V_{OUT} = 5V.

	INDUCTANCE (µH)										
V_{IN} (V)	10	12	15	18	22	27	33	39	47	56	68
1.0	82.6	74.2	64.1	56.3	48.4	41.1	34.7	30.1	25.5	21.8	18.3
1.2	117.0	105.3	91.2	80.3	69.1	58.8	49.8	43.2	36.7	31.4	26.3
1.4	156.4	141.0	122.5	108.0	93.2	79.4	67.4	58.6	49.8	42.6	35.7
1.6	200.3	181.1	157.7	139.3	120.5	102.9	87.5	76.1	64.8	55.5	46.6
1.8	248.3	224.9	196.4	173.9	150.6	128.9	109.9	95.7	81.6	70.0	58.8
2.0	299.5	271.9	238.0	211.2	183.4	157.3	134.3	117.1	100.0	85.9	72.3
2.2	353.1	321.1	281.8	250.6	218.1	187.5	160.4	140.1	119.9	103.2	86.9
2.4	407.7	371.4	326.6	291.0	253.9	218.8	187.6	164.2	140.8	121.3	102.4
2.6	460.9	420.5	370.6	330.9	289.3	250.0	214.9	188.5	162.0	139.9	118.4
2.8	508.8	464.5	410.1	366.8	321.5	278.6	240.2	211.2	182.0	157.5	133.6
3.0		494.5	436.9	391.3	343.7	298.6	258.2	227.7	196.8	170.9	145.5
3.2		475.0	418.4	374.3	328.7	285.9	247.8	219.1	190.1	165.8	141.8

Table 2. ML4861 Maximum Output Current (mA), V_{OUT} = 3.3V.

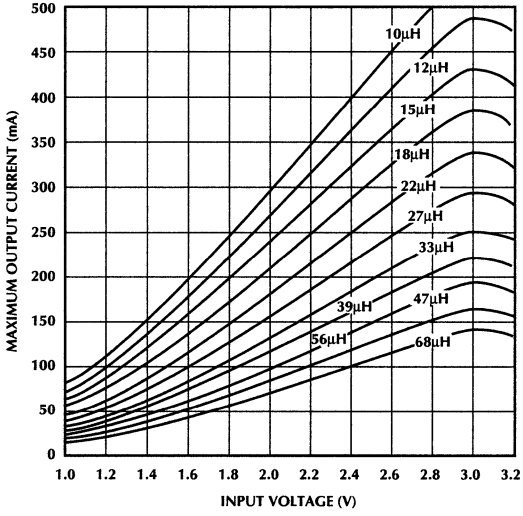


Figure 2. ML4861 Maximum Output Current . V_{OUT} = 3.3V

	INDUCTANCE (µH)										
V_{IN} (V)	10	12	15	18	22	27	33	39	47	56	68
1.0	72.9	64.8	55.4	48.3	41.2	34.8	29.3	25.3	21.4	18.2	15.2
1.2	103.7	92.4	79.1	69.1	59.0	49.9	42.1	36.3	30.7	26.2	21.9
1.4	139.3	124.3	106.7	93.4	79.9	67.6	57.1	49.3	41.8	35.7	29.8
1.6	179.5	160.5	138.1	121.0	103.7	87.9	74.3	64.3	54.5	46.5	38.9
1.8	223.9	200.6	173.0	151.8	130.3	110.6	93.6	81.1	68.8	58.8	49.2
2.0	272.2	244.3	211.1	185.6	159.6	135.7	115.0	99.7	84.7	72.4	60.7
2.2	324.0	291.3	252.3	222.1	191.3	163.0	138.3	120.1	102.1	87.4	73.3
2.4	378.7	341.0	296.0	261.0	225.3	192.2	163.4	142.0	120.9	103.6	87.0
2.6	435.6	392.9	341.7	301.9	261.1	223.2	190.0	165.4	141.0	120.9	101.7
2.8	493.8	446.1	388.8	344.1	298.1	255.4	217.8	189.8	162.1	139.2	117.2
3.0	552.0	499.4	436.1	386.6	335.7	288.1	246.2	214.9	183.8	158.1	133.3
3.2		550.8	481.8	427.9	372.3	320.2	274.3	239.9	205.6	177.1	149.5
3.4			522.9	465.2	405.6	349.7	300.2	263.1	226.0	195.1	165.1
3.6				492.7	430.4	372.0	320.2	281.3	242.3	209.7	178.0
3.8				493.6	431.7	373.9	322.8	284.4	245.7	213.4	181.8

Table 3. ML4861 Maximum Output Current (mA), V_{OUT} = 4V.

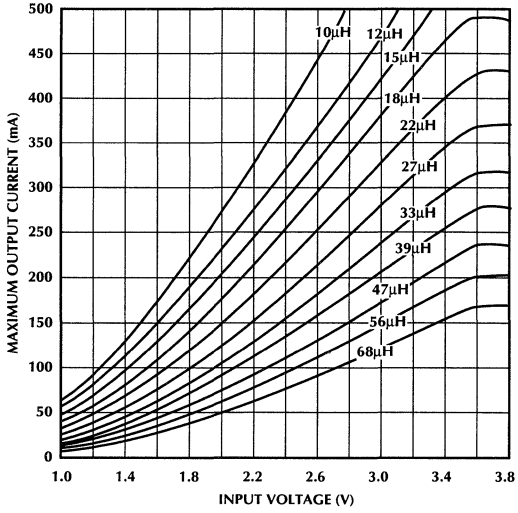


Figure 3. ML4861 Maximum Output Current (mA), V_{OUT} = 4V.

	INDUCTANCE (µH)										
V_{IN} (V)	10	12	15	18	22	27	33	39	47	56	68
1.0	52.2	45.9	38.8	33.5	28.4	23.8	19.9	17.1	14.4	12.3	10.2
1.2	74.6	65.7	55.6	48.1	40.8	34.2	28.7	24.6	20.8	17.7	14.7
1.4	100.9	88.9	75.3	65.3	55.3	46.5	39.0	33.5	28.3	24.0	20.0
1.6	130.8	115.4	97.9	84.9	72.1	60.6	50.8	43.8	36.9	31.4	26.2
1.8	164.3	145.2	123.3	107.1	91.0	76.5	64.3	55.4	46.7	39.7	33.1
2.0	201.2	178.0	151.5	131.6	111.9	94.3	79.2	68.3	57.7	49.1	40.9
2.2	241.5	214.0	182.3	158.6	135.0	113.8	95.7	82.5	69.7	59.4	49.5
2.4	285.1	252.8	215.7	187.8	160.1	135.0	113.6	98.1	82.9	70.6	59.0
2.6	331.7	294.5	q251.6	219.3	187.1	158.0	133.1	114.9	97.2	82.9	69.2
2.8	381.2	338.9	289.9	253.0	216.1	182.6	154.0	133.0	112.6	96.0	80.2
3.0	433.4	385.8	330.5	288.7	246.9	208.9	176.2	152.4	129.1	110.1	92.1
3.2	488.1	435.0	373.2	326.4	279.4	236.6	199.8	172.9	146.6	125.1	104.7
3.4	545.2	486.4	417.9	365.9	313.6	265.9	224.7	194.6	165.1	141.0	118.0
3.6		539.7	464.4	407.0	349.2	296.4	250.8	217.4	184.5	157.7	132.1
3.8			512.3	449.6	386.2	328.2	278.0	241.1	204.8	175.2	146.8
4.0				493.3	424.3	361.0	306.1	265.7	226.0	193.4	162.2
4.2				537.8	463.2	394.6	335.0	291.1	247.7	212.2	178.1
4.4					502.5	428.7	364.4	316.9	270.0	231.5	194.5
4.6						462.8	393.9	343.0	292.5	251.0	211.1
4.8						496.2	423.0	368.7	314.9	270.5	227.8
5.0						527.9	450.8	393.5	336.5	289.5	244.1
5.2							475.9	416.0	356.4	307.0	259.3
5.4							495.6	433.9	372.5	321.5	272.0
5.6							504.4	442.5	380.7	329.3	279.3
5.8							482.4	424.1	365.9	317.4	270.2

Table 4. ML4861 Maximum Output Current (mA), V_{OUT} = 6V.

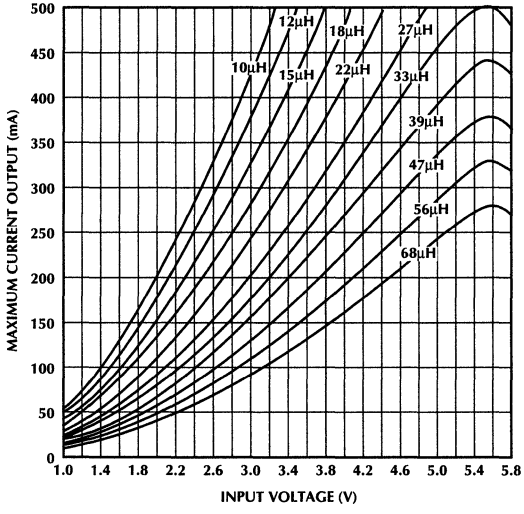


Figure 4. ML4861 Maximum Output Current V_{OUT} = 6V.

	INDUCTANCE (µH)										
V_{IN} (V)	10	12	15	18	22	27	33	39	47	56	68
1.0	76.5	79.4	82.4	84.6	86.6	88.4	89.8	90.8	91.8	92.6	93.3
1.2	75.9	78.8	82.0	84.2	86.3	88.1	89.6	90.6	91.6	92.4	93.1
1.4	75.3	78.3	81.5	83.8	85.9	87.8	89.3	90.4	91.4	92.2	93.0
1.6	74.7	77.8	81.1	83.4	85.6	87.5	89.1	90.2	91.2	92.1	92.9
1.8	74.2	77.3	80.6	83.0	85.2	87.2	88.8	90.0	91.1	91.9	92.8
2.0	73.6	76.8	80.2	82.6	84.9	86.9	88.6	89.8	90.9	91.8	92.6
2.2	73.1	76.3	79.8	82.3	84.6	86.6	88.3	89.5	90.7	91.6	92.5
2.4	72.6	75.9	79.4	81.9	84.3	86.4	88.1	89.3	90.5	91.5	92.4
2.6	72.2	75.5	79.0	81.6	84.0	86.1	87.9	89.1	90.4	91.3	92.2
2.8	71.7	75.1	78.7	81.2	83.7	85.9	87.7	89.0	90.2	91.2	92.1
3.0	71.3	74.7	78.3	80.9	83.4	85.6	87.5	88.8	90.0	91.1	92.0
3.2		74.3	78.0	80.6	83.2	85.4	87.3	88.6	89.9	90.9	91.9
3.4			77.7	80.3	82.9	85.2	87.1	88.4	89.7	90.8	91.8
3.6			77.4	80.1	82.7	85.0	86.9	88.3	89.6	90.7	91.7
3.8				79.9	82.5	84.8	86.7	88.1	89.5	90.6	91.6
4.0					82.3	84.6	86.6	88.0	89.4	90.5	91.5
4.2					82.2	84.5	86.5	87.9	89.3	90.4	91.5
4.4						84.5	86.5	87.9	89.3	90.4	91.4
4.6						84.6	86.5	88.0	89.3	90.4	91.5
4.8						84.9	86.8	88.2	89.6	90.7	91.7

Table 5. ML4861 Efficiency at Maximum Output Current (%), V_{OUT} = 5V.

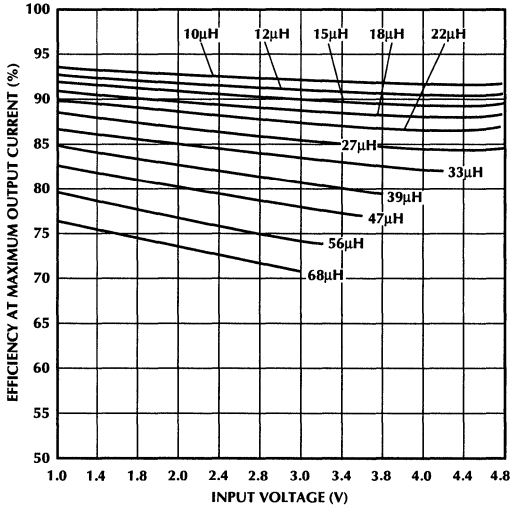


Figure 5. ML4861 Efficiency V_{OUT} = 5V.

	INDUCTANCE (µH)										
V_{IN} (V)	10	12	15	18	22	27	33	39	47	56	68
1.0	69.7	73.3	77.2	80.0	82.7	85.1	87.0	88.4	89.7	90.8	91.8
1.2	68.8	72.5	76.5	79.4	82.1	84.5	86.6	88.0	89.4	90.5	91.6
1.4	68.0	71.7	75.8	78.7	81.6	84.1	86.1	87.6	89.1	90.2	91.3
1.6	67.2	71.0	75.1	78.1	81.0	83.6	85.7	87.3	88.8	90.0	91.1
1.8	66.5	70.3	74.5	77.6	80.5	83.1	85.3	86.9	88.5	89.7	90.9
2.0	65.8	69.7	73.9	77.0	80.0	82.7	85.0	86.6	88.2	89.5	90.7
2.2	65.3	69.1	73.4	76.6	79.6	82.3	84.6	86.3	87.9	89.2	90.5
2.4	64.8	68.7	73.0	76.1	79.2	82.0	84.3	86.0	87.7	89.0	90.3
2.6	64.4	68.3	72.7	75.8	78.9	81.7	84.1	85.8	87.5	88.8	90.1
2.8	64.2	68.1	72.5	75.6	78.8	81.6	83.9	85.7	87.4	88.7	90.0
3.0		68.2	72.5	75.7	78.8	81.6	84.0	85.7	87.4	88.8	90.1
3.2		68.8	73.2	76.3	79.4	82.2	84.5	86.2	87.8	89.2	90.4

Table 6. ML4861 Efficiency at Maximum Output Current (%), V_{OUT} = 3.3V.

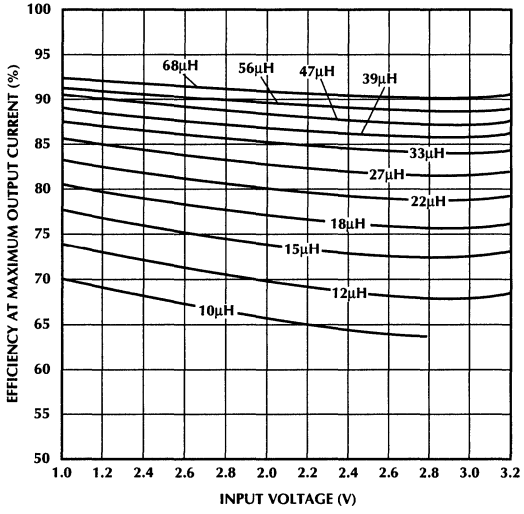


Figure 6. ML4861 Efficiency V_{OUT} = 3.3V.

	INDUCTANCE (µH)										
V_{IN} (V)	10	12	15	18	22	27	33	39	47	56	68
1.0	73.0	76.3	79.8	82.3	84.7	86.7	88.4	89.6	90.8	91.7	92.6
1.2	72.3	75.6	79.2	81.8	84.2	86.3	88.1	89.3	90.5	91.5	92.4
1.4	71.6	75.0	78.7	81.3	83.8	85.9	87.8	89.0	90.3	91.3	92.2
1.6	70.9	74.4	78.1	80.8	83.3	85.6	87.4	88.8	90.0	91.1	92.0
1.8	70.2	73.8	77.6	80.3	82.9	85.2	87.1	88.5	89.8	90.9	91.8
2.0	69.6	73.2	77.0	79.8	82.5	84.8	86.8	88.2	89.6	90.6	91.7
2.2	69.1	72.6	76.6	79.4	82.1	84.5	86.5	87.9	89.3	90.5	91.5
2.4	68.5	72.1	76.1	79.0	81.7	84.2	86.2	87.7	89.1	90.3	91.3
2.6	68.0	71.7	75.7	78.6	81.4	83.9	85.9	87.5	88.9	90.1	91.2
2.8	67.6	71.3	75.3	78.2	81.1	83.6	85.7	87.2	88.7	89.9	91.0
3.0	67.3	70.9	75.0	77.9	80.8	83.3	85.5	87.0	88.5	89.8	90.9
3.2		70.7	74.7	77.7	80.6	83.1	85.3	86.9	88.4	89.6	90.8
3.4			74.6	77.6	80.4	83.0	85.2	86.8	88.3	89.6	90.7
3.6				77.6	80.5	83.0	85.2	86.8	88.3	89.6	90.7
3.8				77.9	80.8	83.3	85.5	87.0	88.5	89.7	90.9

Table 7. ML4861 Efficiency at Maximum Output Current (%), V_{OUT} = 4V.

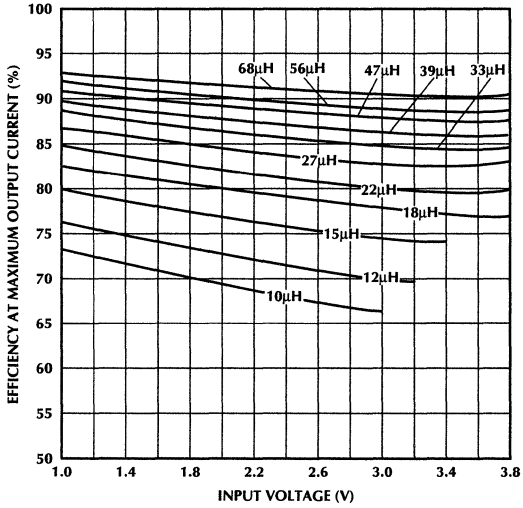


Figure 7. ML4861 Efficiency V_{OUT} = 4V.

	INDUCTANCE (µH)										
V_{IN} (V)	10	12	15	18	22	27	33	39	47	56	68
1.0	77.0	79.8	82.8	84.9	86.9	88.6	90.0	91.0	92.0	92.7	93.4
1.2	76.5	79.4	82.4	84.6	86.6	88.4	89.8	90.8	91.8	92.6	93.3
1.4	76.0	78.9	82.1	84.3	86.3	88.1	89.6	90.6	91.6	92.4	93.2
1.6	75.5	78.5	81.7	83.9	86.0	87.9	89.4	90.5	91.5	92.3	93.1
1.8	75.0	78.0	81.3	83.6	85.8	87.6	89.2	90.3	91.3	92.2	92.9
2.0	74.5	77.6	80.9	83.3	85.5	87.4	89.0	90.1	91.2	92.0	92.8
2.2	74.1	77.2	80.6	82.9	85.2	87.2	88.8	89.9	91.0	91.9	92.7
2.4	73.6	76.8	80.2	82.6	84.9	86.9	88.6	89.8	90.9	91.8	92.6
2.6	73.2	76.4	79.9	82.3	84.7	86.7	88.4	89.6	90.7	91.7	92.5
2.8	72.8	76.0	79.5	82.0	84.4	86.5	88.2	89.4	90.6	91.5	92.4
3.0	72.4	75.7	79.2	81.7	84.1	86.2	88.0	89.2	90.4	91.4	92.3
3.2	72.0	75.3	78.9	81.4	83.9	86.0	87.8	89.1	90.3	91.3	92.2
3.4	71.7	75.0	78.6	81.2	83.6	85.8	87.6	88.9	90.2	91.2	92.1
3.6		74.7	78.3	80.9	83.4	85.6	87.5	88.8	90.0	91.1	92.0
3.8			78.0	80.7	83.2	85.4	87.3	88.6	89.9	90.9	91.9
4.0				80.4	83.0	85.2	87.1	88.5	89.8	90.8	91.8
4.2				80.2	82.8	85.1	87.0	88.3	89.7	90.7	91.7
4.4					82.6	84.9	86.8	88.2	89.6	90.6	91.7
4.6						84.8	86.7	88.1	89.5	90.6	91.6
4.8						84.6	86.6	88.0	89.4	90.5	91.5
5.0						84.6	86.5	87.9	89.3	90.4	91.5
5.2							86.5	87.9	89.3	90.4	91.5
5.4							86.5	87.9	89.3	90.4	91.5
5.6							86.6	88.0	89.4	90.5	91.5
5.8							87.0	88.3	89.7	90.8	91.8

Table 8. ML4861 Efficiency at Maximum Output Current (%), V_{OUT} = 6V.

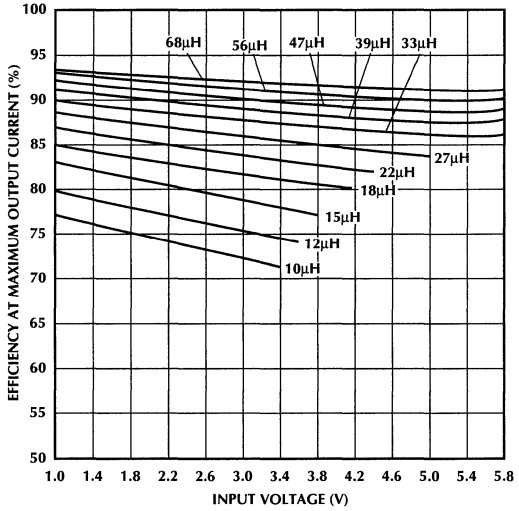


Figure 8. ML4861 Efficiency V_{OUT} = 6V.

Application Note 30

ATM Applications Using the ML6672

INTRODUCTION

Asynchronous Transfer Mode (ATM) has been recognized in the last few years as a communications architecture of choice which will unify public and private networks. Originally, ATM was selected as the transfer mode for Broadband ISDN (BISDN), and later it was adopted as the User-to-network interface (UNI) using the Synchronous Optical Network (SONET) defined from 155.52Mbps to 622.08Mbps as the physical layer interface standard. Soon after that, ANSI issued a draft standard for a physical layer BISDN User-to-Network Interface (UNI) based on DS3. This was important because with DS3 already tariffed in most areas, development for ATM could easily start. The ATM standard was quickly accepted by various computer and network companies which decided to incorporate ATM in their future networking plans. This resulted in ATM LANs which appeared well before the long haul ATM services.

There are several reasons for ATM's broad acceptance, some of which are:

ATM is based on a small fixed length packet (53 byte), called cells, which can be efficiently implemented in silicon because of the small storage space required.

ATM works not only in small local environments, but also in long haul international networks.

ATM is capable of supporting all kinds of traffic such as voice, video and data which was not possible with other wide area technologies.

ATM is scalable and can work at different speeds and physical media.

With all these reasons, the main driving force for any new and emerging technology, is going to be the type of new and innovative applications it can offer to the customers in order to motivate them to move and pay for these new technologies.

So, what kind of new applications and services can we expect in the market place?

EXPANDING LANS

Considering the benefits of ATM, such as manageability, security, scalability and high performance, it is no wonder that shared medium LANs and computer intensive work-groups are looking at using ATM as a broadband networking solution. ATM makes it possible to have virtual LANs, in which work-groups are defined logically, and can extend over multiple physical networks. It also offers higher speeds than most LANs today, and it can easily move to even higher transmission speeds without changing the network architecture.

ATM transports multimedia traffic, particularly video. Because of the small, fixed length cells of ATM, it is capable to accommodate a mixture of traffic types such as video, voice and data with different delay requirements. To do so, it is necessary to have sufficient bandwidth to transport large video files, and also to have the necessary bandwidth management capability to separate the low priority data traffic from the high priority data traffic such as audio and video information that needs to be delivered "real-time" with minimum delay. Isochronous support, which is not supported in Ethernet or FDDI, makes ATM very attractive for full motion video and other high bandwidth applications. (8 to 30Mbps for compressed video).

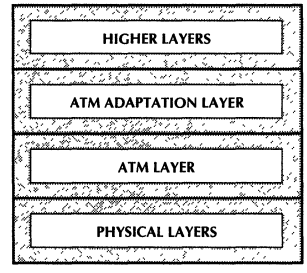


Figure 1. Protocol Reference Model.

ATM as the leading Wide Area Networking Technology (WAN) contender. Ideally, customers would like to pay only for what they send, and this implies sending as much traffic as necessary without any bandwidth limitations. The dynamic bandwidth allocation capability of ATM makes this the technology of choice for national and multinational networks.

BUT HOW DOES ATM WORK?

The ATM reference model can be subdivided into several sections, each performing a defined task.

PHYSICAL LAYER INTERFACE

The physical layer interface specifies the actual transport mechanism of signals ranging from 45Mbps to 622Mbps, and plans are in place to adopt carrier signals as high as 2.4Gbps and as low as 1.544Mbps or 2.048Mbps. ATM's original intention was to provide excellent performance at broadband rates in order to carry video, voice and data through the same medium. The ATM Forum has now developed a User Network Interface (UNI) specification document with two types of UNI's (Public and Private UNI).

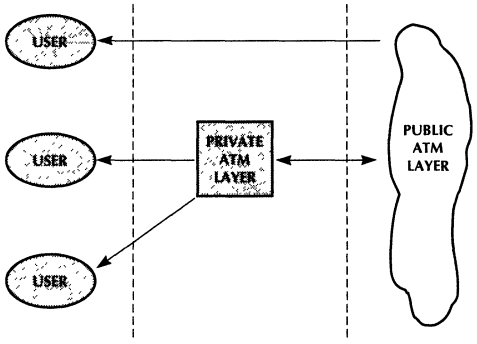


Figure 2. ATM Private and Public Physical Layer.

The Public UNI specifies the interface from an end terminal or local switch to the public network. This interface uses 45Mbps (DS3) defined by ANSI Committee T1 draft standard and 155Mbps defined by CCITT and ANSI.

The Private UNI specifies three interfaces. One interface uses a technology developed for FDDI and 4B/5B block coding (transmission rate of 125Mbaud). The other interface runs at a bit rate of 155Mbps and uses 8B/10B block coding which requires 191Mbaud. The third is a standardized CCITT and ANSI specification which uses the SDH/SONET frame structure, with a minimal subset of overhead octets of the SDH/SONET signal.

To attain interoperability at both, the public and the private UNIs, the ATM Forum expects to use the SDH/SONET 155Mbps interface. Work has also been started on running 155Mbps over copper twisted pair physical interfaces for desktop access. Micro Linear has developed an ATM UTP transceiver (ML6672) for 155Mbps NRZ encoded data transmission over Category 5 Unshielded Twisted Pair and Shielded Twisted Pair.

ATM LAYER

The key concept of ATM is that it is a connection oriented, packet like switching and multiplexing architecture which offers great flexibility to transport information. The ATM layer is responsible for attaching the header to the payload. The header contains a label which uniquely identifies a logical channel and is used for multiplexing, switching and routing of the information. Following the physical layer transport at the bit rate of the physical channel, bandwidth is allocated by proportionally assigning more headers of cells of logical channels. This dynamic bandwidth allocation structure differentiates ATM from the fixed bandwidth supported by Time Division Multiplexing Networks (TDM).

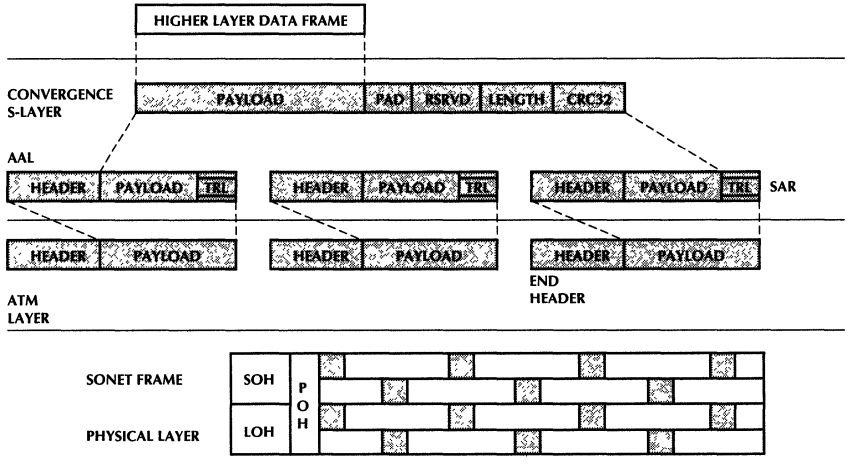


Figure 3. Transfer of User Information to ATM.

The ATM header carries the generic flow control at the UNI's, the payload identification, cell loss priority and header control. The payload identification provides information on the cell payload and whether the cell has encountered congestion. The cell loss priority provides information on which cells are eligible for discard under certain network conditions, and the header error control detects error conditions to prevent misdelivery of cell packets.

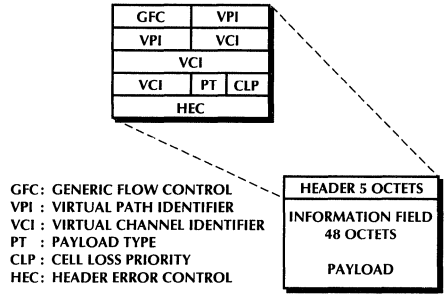


Figure 4. ATM Cell Format.

ATM ADAPTATION LAYER

The Adaptation layer does exactly that. It adapts the transfer of information between the ATM Layer and Higher Layer protocols (BISDN, SMDS or Frame Relay). This layer is only used by equipment that terminates signaling protocols since they need to extract the information for higher layer processing. Because of this, there are several AAL protocols defined, such as:

AAL Type 1: This protocol is intended for constant bit rate network services. DS1, for example, transfers information at a constant bit rate which requires some sort of timing recovery to maintain the bit timing across the network. Because ATM uses cells to transport information and does not have a strict timing structure, it is the function of AAL Type 1 to provide this functionality and avoid having over or underflows at the receiver.

AAL Type 3/4: This protocol adapts to the needs of SMDS (Switched Multi-megabit Data Service) connectionless services. SMDS like most other protocols transmit variable length frames or packets which are longer than the 48 octet cell payload of ATM. A transmitter will need to segment each of these frames into fixed size segments and place them into the payload. Conversely at the other end, these packets will have to be reassembled. In addition to the segmentation and reassembly process, a per-cell Cyclic Redundancy Check (CRC) is performed to prevent transmission errors, and a per-frame length check, to detect loss of cells in the frame.

AAL Type 5: This is a simple adaptation layer used by computer, hub and LAN manufacturers to adapt to high speed data communications. One of the features of this protocol is shown in figure 3 which uses information in the cell header to identify the first and last of the frames. This layer also uses a per frame CRC to detect both transmission and cell loss errors.

ATM APPLICATIONS

Considering the quick release of the BISDN User-to-Network Interface standard released by ANSI which was based on the DS3 (45Mbps) rate and format, a number of equipment manufacturers are enhancing their existing equipment to provide ATM capability. For example, equipment designed to support SMDS is being enhanced to provide DS3 access to an ATM network. This gives the customer the benefit of only being charged on whatever portion of the DS3 bandwidth they are using. Initial applications will include integrating high-speed LAN's with other data and video services. These applications include on-line viewing of real estate, advertising, publishing and home shopping. Other services will be video conferencing, HDTV, high-speed education and science networks, scientific modeling and stock market trading. As higher speed and bandwidth becomes available, supercomputer access is going to facilitate pharmaceutical engineers to simulate different molecular structures and medical images across the globe to provide consultation and diagnosis capability.

There are two kinds of hardware which are going to be necessary to build an ATM LAN. The first is the host interface card which allows the host to connect to the network, and the second is the switches which form the nodes of the network. These cards, as the example shown in Figure 5, interface to Multimode fiber or as recently proposed in the ATM Forum, through Unshielded Twisted Pair Copper wires.

There are two kinds of hardware which are going to be necessary to build an ATM LAN. The first is the host interface card which allows the host to connect to the network. Micro Linear has developed a complete monolithic transceiver solution for 155Mbaud NRZ encoded data transmission over Category 5 Unshielded Twisted Pair and Shielded Twisted Pair cables (ML6672) which complies to the newly emerging PMD standard presented in the ATM Forum. This device is implemented in a high-speed 1.5µm BiCMOS process with high drive capability, low power consumption and fast rise and fall times (<2ns). Some of the additional features which are provided by the ML6672 are a common mode reference to set the DC level for the equalizer and near end transformer winding. A link status circuit monitors the line integrity and provides a differential ECL 100K compatible output indicating the presence of a data signal with an amplitude exceeding a preset threshold to the rest of the circuitry.

ML6672 RECEIVER SECTION

The receiver section (refer to block diagram of ML6672) consists of an equalizing filter with a feedback loop for controlling the line compensation. The feedback loop contains a filter section and a detection block for determining the proper control signal. The adaptive equalizer is used to compensate for amplitude and phase distortion incurred by the cable. The adaptive control section determines the cable length and adjusts the equalizer accordingly. Two external capacitors are provided to set the time constant for the adaptation of the equalizer loop as well as the signal detect response. These two capacitors should have a value between 0.033µF and 1µF. The smaller the capacitor value, the quicker the response time. In addition, the internal time constant controlling the equalizer transfer function are set through an external 1% resistor connected to (RRSET1 and RRSET2).

Another separate 1% resistor connected across RTH1 and RTH2 sets the internal levels for equalization as well as the signal detect thresholds. This resistor is included to provide more flexibility between different magnetics. For applications using a 1:1 transformer on the transmitter and receiver section, the value of this resistor (typ. 250Ω) should be set to match the peak to peak transmit side amplitude.

$$V_{AMP} = \frac{16 \times 1.25 \times R_{TH}}{R_{SET}}$$

Where V_{AMP} is the amplitude of the transmit output with zero length cable.

For example, as the input signal amplitude diminishes, the amount of equalization increases until it reaches a maximum equivalent of 100m of twisted pair cable (Category 5). The adaptive control block governs both, the amount of equalization as well as the link detection status.

The link detection threshold has a fixed relationship to the overall equalization level which is currently 25% of the transmitted amplitude. This makes sure that a minimum signal level must be received for the link status to be true. After the input signal has been equalized, it is fed through a loopback multiplexer. This loopback multiplexer can be controlled with a TTL compatible input pin which enables the transmitter to receiver connection (local loopback).

Followed by the multiplexer is an ECL 100K compatible buffer stage which outputs the signals to compatible ATM physical interface chips.

ML6672 TRANSMITTER SECTION

The transmitter section of the ML6672 accepts ECL 100K compatible NRZ inputs at TxIN+ and TxIN– from the physical interface devices and sends the signals onto a two pin current driver (TPOUT+, TPOUT–) through an external low pass filter and transformer module. The output amplitude of the transmitted signals are programmable through an external 1% resistor (RTSET) which controls the differential output current as follows:

$$I_{OUT} = \frac{64 \times 1.25}{RTSET}$$

Note: The maximum recommended output current is 21mA.

The transmitter section also offers an enable function which forces the NRZ buffer to a quiet state whenever the TxOFF pin is asserted low.

Both the receiver and the transmitter are terminated into 100Ω on the secondary side of the transformer.

POWER SUPPLY, COMPONENT AND LAYOUT CONSIDERATIONS

Separate receiver and transmitter analog and digital power supply and ground pins are provided to isolate sensitive circuitry from noise generating digital functions. It is recommended to surrounding the layout with a solid ground plane and connect TGNDA and TGNDD directly to the ground plane. TVCCA and TVCCD should have separate leads to the main supply source, and TVCCA and RVCCA should have a small ferrite bead followed by a high frequency capacitor connected very close to the V_{CC} and ground pins to filter out high frequency noise which can degrade the receivers performance. All additional components should be as close to the device as possible to avoid potential problems.

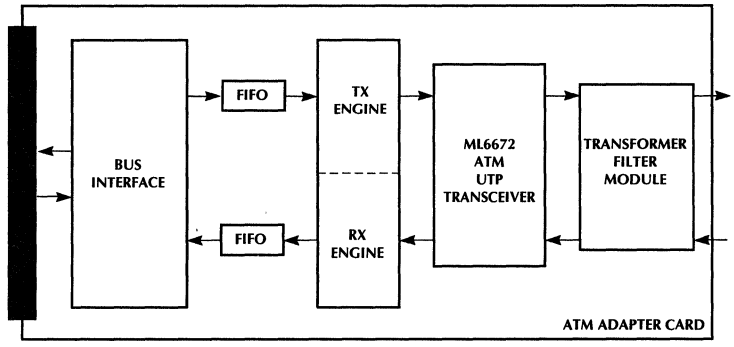


Figure 5. Typical ATM Card

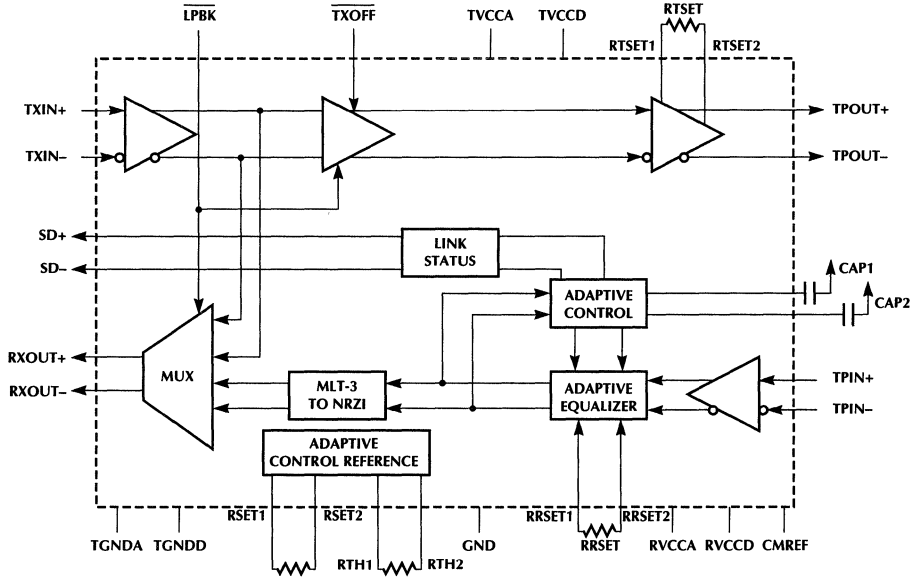


Figure 6. ML6672 Block Diagram.

George A. Hall
and Urs Mader

Theory and Application of the ML4874 and ML4876 LCD Backlight Controller ICs

INTRODUCTION

The ML4874 and ML4876 are high performance backlight and dimming controller integrated circuits specifically designed to control miniature cold-cathode fluorescent lamps (CCFLs) for portable computing and instrumentation equipment.

These devices are designed to achieve high efficiency as well as high application flexibility. Some of the key features are:

- Low Standby Current (<10μA)
- Differential Output Lamp Driver
- Up to 30% Less Power for Same Light Output
- Allow Use of all N-channel FETs
- Resonant Threshold Detect (RTD) Switching
- Regulated lamp current by means of a buck switching converter which is synchronized to the lamp driver frequency for flicker free operation. The duty cycle is capable of operating from 0% to 100%.
- Uses off the shelf power components including magnetic components.
- Improved Efficiency (≈95%)
- Surface mount SSOP package of this circuit is available for space economy.

FUNCTIONAL BLOCK DIAGRAM

All controllers in this series consist of two main functional blocks.

- A buck current regulator block that controls the lamp current.
- A current fed lamp driver block that uses a self-synchronizing scheme for low loss resonant threshold detect switching (RTD), and facilitates flicker free dimming.

The simplified block diagram of the ML4874 is shown in Figure 1. The timing of the circuit is controlled by setting the frequency of the oscillator by components connected to pins 4 and 9 and ground. For ML4876, only pin 9 is used for C_T. R_T is built-in internally. See Figure 14. For ML4874, there is a zener diode at pin 2 to set the voltage, whereas the ML4876 does not have this feature.

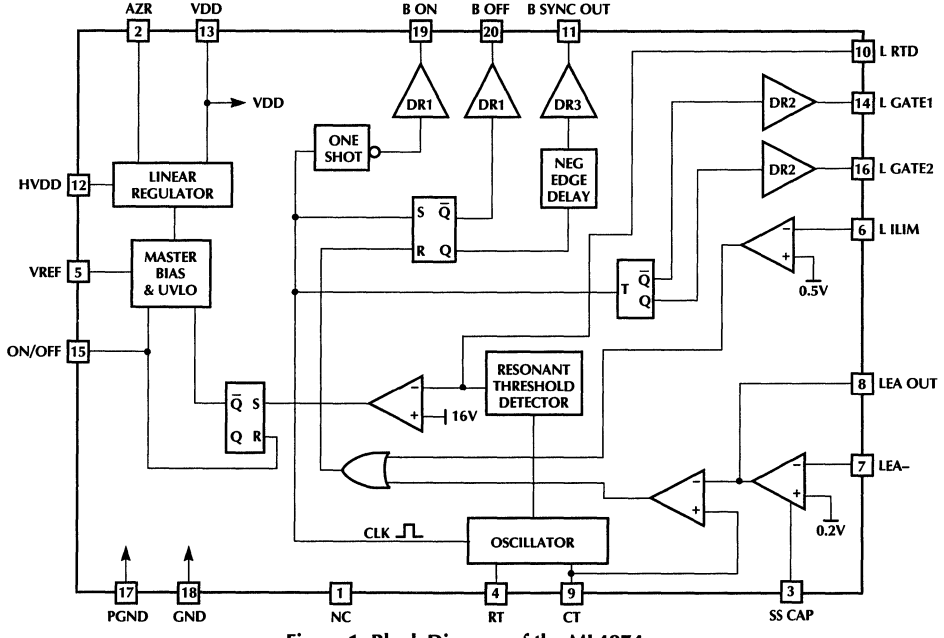


Figure 1. Block Diagram of the ML4874.

The frequency of the pre-regulator stage and the contrast regulator stage are synchronized with the inverter circuit which share a common oscillator. This feature helps to reduce possible RFI and the effect of the "walking" lines across the LCD screen. The operating frequency of the buck and the contrast regulator is twice that of the CCFL current frequency.

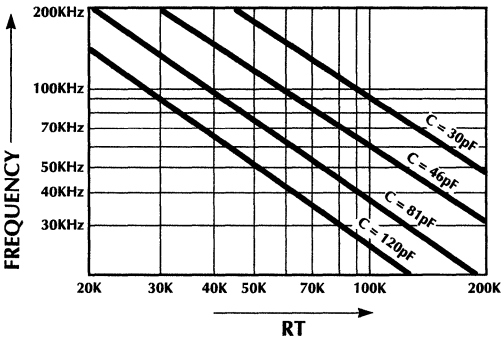


Figure 2. R_T and C_T Selection to Set Frequency for ML4874.

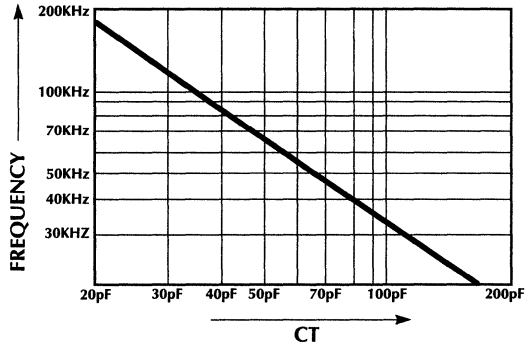


Figure 4. C_T Selection to Set Frequency for ML4876.

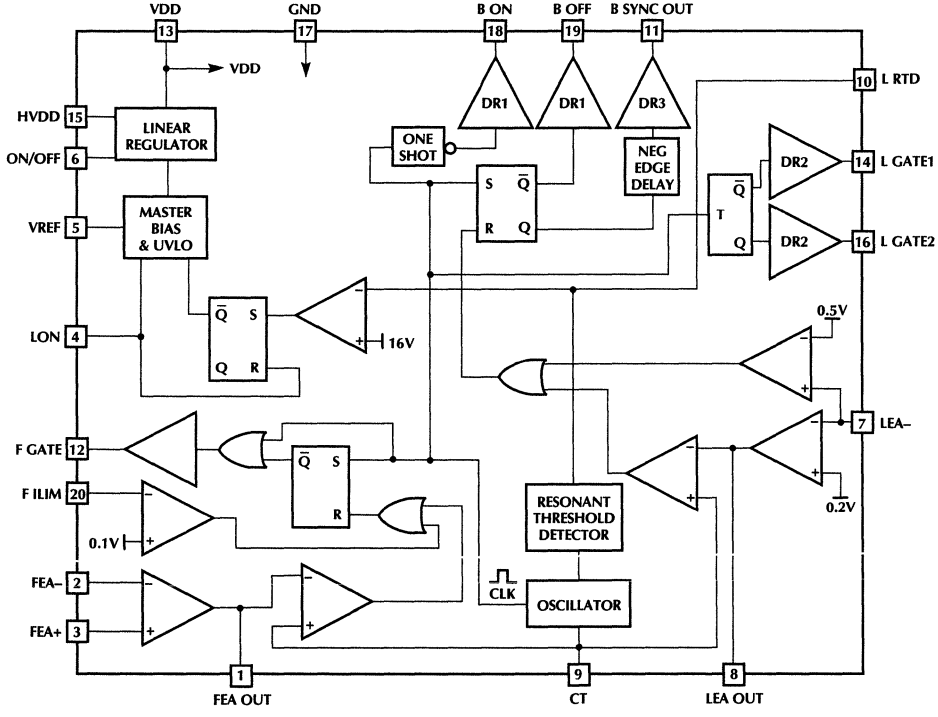


Figure 3. Block Diagram of ML4876.

SIMILARITIES AND DIFFERENCES BETWEEN THE ML4874 AND THE ML4876

Similarities

They are both high-efficiency differential backlight drivers, with low standby current (<10µA).

The buck regulator with synchronous rectification and resonant threshold detection are also common features.

Differences

The basic differences between the two controllers are tabulated below:

ML4874	ML4876
No Contrast	Contrast Control
Zener (Pin 2)	No Zener
R_T and C_T Pins	Only C_T Pin
Separate input for lamp current feedback and current limit	Both functions share one pin
L_{ON} pin for lamp only	L_{ON} and ON/OFF pins
Soft Start Pin	No Soft Start

DESCRIPTION OF THE LAMP INVERTER CIRCUIT

The lamp inverter circuit is comprised of the current regulating buck converter and the current-fed Royer-type inverter. The buck converter controls the magnitude of lamp current. This feature is instrumental in providing dimming control. The simplified equivalent electrical schematic of the driver section is shown in Figure 5. Due to the presence of L_1, the circuit shown in Figure 5 is essentially a current fed parallel loaded parallel resonant circuit, which can be further simplified to that shown in Figure 6.

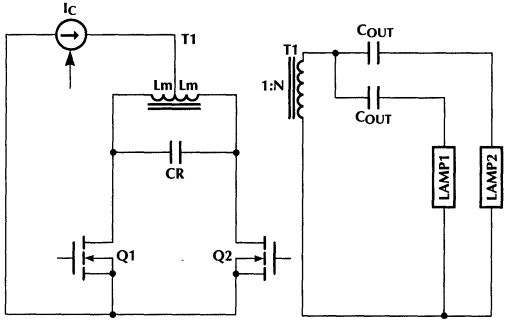


Figure 5. Simplified Lamp Driver Circuit.

The simplification in Figure 6 assumes that two lamps are operating in parallel. If one lamp is used then the original output ballast capacitor value should be used in the calculations.

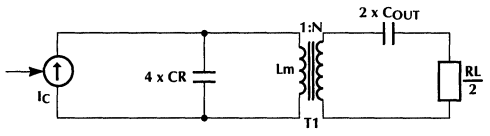


Figure 6. Simplified Lamp Driver Circuit.

L_m is the magnetizing inductance of the inverter transformer, which tunes with the resonant capacitor C_R to set the resonant frequency of the inverter. The oscillator frequency of the ML874/76 is set lower than the resonant frequency to ensure synchronization.

The current source labeled I_C in Figure 6 is a conceptual current source which models the function of L_1. Since the circuit always operates at resonance the impedance seen by the above current source is resistive and equal to the transformed impedance of the lamp which is given by the formula below:

$$R_L = \frac{V_L}{I_L} \qquad (1)$$

where V_L is the operating voltage of the lamp at full brightness and I_L is the lamp current.

In most cases the value of the ballasting capacitor C_{OUT} is chosen such that its reactance is approximately equal to the lamp resistance R_L. The two capacitors C_{OUT} are used to simulate two separate current sources, so that current will share between the lamps. The typical value for R_L is 100KΩ. For a typical operating frequency of 50kHz, C_{OUT} yields a capacitive reactance of approximately 100K. The best choice for this capacitor therefore lies between 27 to 33pF.

OPERATING WAVEFORMS OF THE LAMP DRIVER SECTION

Figure 7 shows some of the waveforms present in critical parts of the circuit. Refer to Figure 8.

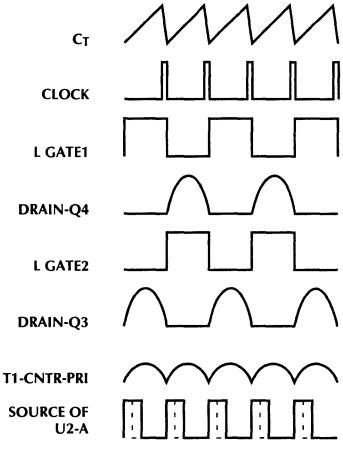


Figure 7. Operating Waveforms of the Lamp Driver Section.

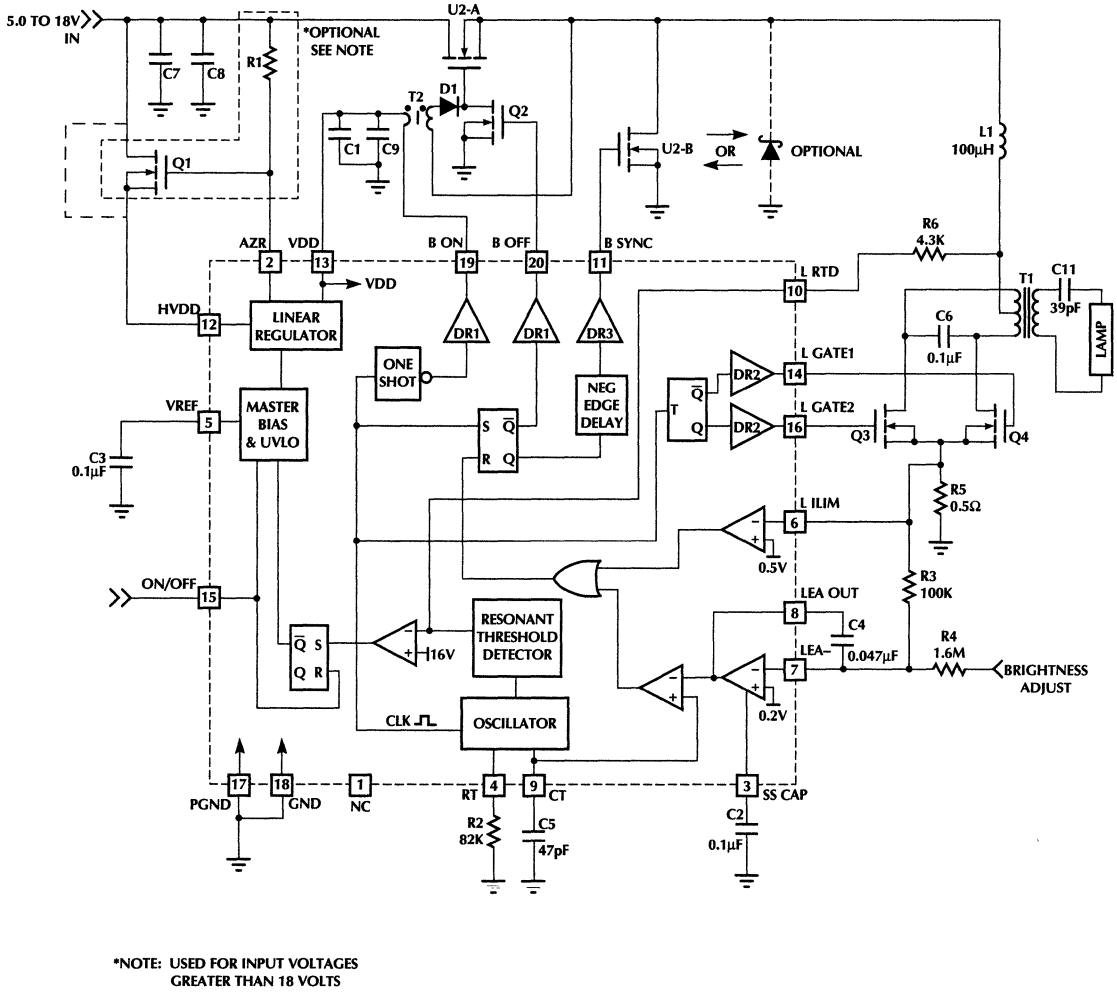
OSCILLATOR

The oscillator frequency is set externally through R_T and C_T for ML4874, and C_T only for ML4876 (R_T is a resistor of 82KΩ integrated on the chip). The equation below gives the relationship between frequency and timing components. This frequency should be set below the resonant frequency of the inverter. See Figures 2, 4 and 8.

$$f_{OSC} = \frac{1}{3.51 R_T C_T} \qquad (2)$$

Under steady state conditions, the oscillator frequency will be locked to twice the natural frequency of the lamp inverter resonant frequency. The lower bound on the resonant frequency (that will be used to calculate the oscillator timing components) can be calculated by using the following formula:

$$f_{MIN} \cong \frac{1}{2\pi\sqrt{L_m\left(4 C_R + n N^2 C_{OUT}\right)}} \qquad (3)$$



*NOTE: USED FOR INPUT VOLTAGES GREATER THAN 18 VOLTS

Figure 8. Typical Application Schematic for the ML4874.

Where n is the number of lamps at the output with ballasting capacitors C_{OUT}, N is the secondary to primary turns ratio of T_1, L_m is the primary inductance of T_1 and C_R is the capacitance across the primary. Based on this information the oscillator free running frequency is set to approximately 10% to 15% lower than twice the minimum frequency of the resonant tank.

$$C_T \cong \frac{\sqrt{L_m\left(4\,C_R + n\,N^2\,C_{OUT}\right)}}{R_T} \qquad (4)$$

$$R_T \cong \frac{\sqrt{L_m\left(4\,C_R + n\,N^2\,C_{OUT}\right)}}{C_T} \qquad (5)$$

Example Calculation for ML4874:

$L_m = 12 \times 10^{-6}$ $\quad C_R = 0.1 \times 10^{-6}$

$C_T = 47 \times 10^{-12}$ $\quad n = 1$

$C_{OUT} = 39 \times 10^{-12}$ $\quad N = 135$

$$f = \frac{1}{2\pi\sqrt{L_m\left(4\,C_R + n\,N^2\,C_{OUT}\right)}} = 43\,kHz \qquad (6a)$$

$$R_T = \frac{\sqrt{L_m\left(4\,C_R + n\,N^2\,C_{OUT}\right)}}{C_T} = 78\,k\Omega \qquad (6b)$$

The natural frequency of the resonant tank will increase as the lamp(s) are dimmed. The upper bound of this increase can be estimated by the formula below:

$$f_{MAX} \cong \frac{1}{4\pi\sqrt{L_m\,C_R}} \qquad (7)$$

For the previous example this will be:

$L_m = 12 \times 10^{-6}$ $\quad C_m = 0.1 \times 10^{-6}$

$$f_{MAX} \cong \frac{1}{4\pi\sqrt{L_m\,C_R}} = 72\,kHz \qquad (8)$$

Thus the lowest operating frequency will be at full brightness.

REFERENCE VOLTAGE

The reference voltage is 2.5 volts ±2%. To guard against noise, it is advisable to connect a 0.1µF capacitor across the reference to ground. This precise reference voltage helps to stabilize the brightness and contrast from unit to unit.

BUCK REGULATOR AND GATE DRIVE CIRCUIT

The ML4874/76 design is based on a 5V BiCMOS process to obtain the highest possible efficiency and size economy. The buck converter power MOSFET switch, U_{2A} is driven by a special gate drive circuit (see Figure 14).

This drive circuit consists of T_2, D_2 and Q_3. T_2 has the dual function of isolating the drive signal and stepping up its voltage for adequate enhancement of U_{2A}. T_2 is a standard surface mount transformer that can be obtained from many coil manufacturers. The ML4874/76 has been designed such that a short duration (approx. 150ns) voltage pulse is applied to T_2. This pulse charges the gate of U_{2A}. The charge is trapped at the gate by D_2 until the end of the ON-time at which point the gate of U_{2A} is discharged by Q_3. This drive technique enables the ML4874/76 to control power at voltages that are higher than its own maximum operating voltage rating of 5V.

The gate drive transformer requirements are listed below:

- Leakage inductance <300nH
- Primary magnetizing inductance >3µH.

SELECTION OF THE BUCK INDUCTOR (L1)

The inductor plays a central role in the proper operation of the inverter circuit.

To find the inductor value it is necessary to consider the inductor ripple current. The following formula gives the inductor peak to peak current ripple for when $V_{TP}<V_{IN}$.

$$i_{Lp-p} = \frac{V_{tp}}{2\pi f_{OSC}\,L_B}\left[1+\cos\left(2\frac{V_{TP}}{V_{IN}}\right)\right] \text{ For } V_{TP} < V_{IN} \qquad (9)$$

Where: i_{Lp-p} is the peak to peak inductor current, V_{IN} is the supply voltage, V_{TP} is the peak voltage at the tab of T_1 (the waveform at this point is a full wave rectified sinewave), f_{OSC} is the inverter operating frequency, and L_B is the inductance of the buck regulator.

Normally the inductor peak to peak ripple current is chosen to be a small fraction of the overall DC current level. However, the circuit continues to function adequately, when this ripple is as large as the DC current. Ripple currents larger than the DC current will lead to larger-sized inductors due to the high peak currents with large ripple.

If we define the percentage of ripple in the inductor as:

$\%\ \text{ripple} = \frac{i_{Lp-p}}{i_{Lave}}$, then L_B is given by the following equation.

$$L_B = \frac{1}{\%\ \text{ripple}} \times \frac{V_{TP}^{\,2}}{2\sqrt{2\pi\,f_{OSC\,MIN}\,P_{LMAX}}} \times\left[1+\cos\left(\frac{2V_{TP}}{V_{IN\,MAX}}\right)\right] \qquad (10)$$

Where: P_L is the maximum lamp power (if more than one lamp is used then P_L is the total consumption of all the lamps). The above equation is set up to give the worst case value for L_B. Choosing % ripple to be 66% minimizes the LI^2 rating for the inductor.

Example:

$V_{IN\ MAX}$ = 12 Volts, P_L = 2 Watts

$f_{OSC\ MIN}$ = 55 kHz, V_{TP} = 7.2 Volts

$$L_B = \frac{(7.2V)^2}{0.66 \times 2\pi \times \sqrt{2} \times 55kHz \times 2W}\left[1+\cos\left(2\frac{7.2V}{12V}\right)\right] \quad (11)$$

$$= 109\mu H$$

In this case the calculated inductor value is 109µH. A standard 100µH inductor was used in the application circuit. If core loss is a problem, increasing the inductance of L_B will help.

INVERTER TRANSFORMER (T1)

The inverter transformer T1 also has a dual role. Besides stepping up the low voltage to a higher value suitable for the operation of the lamp(s), it is also part of the resonant circuit. The magnetizing inductance of this transformer is the resonating inductor. This transformer is an off the shelf part available from different coil manufacturers. The inverter transformer used in the example circuit is capable of driving one 2W lamp with a start voltage of 1.5KV.

RESONATING CAPACITOR (C6 FOR ML4874, C12 FOR ML4876)

Typically, the value of this capacitor falls between 0.047µF to 0.22µF, depending on the frequency and power level. It should be a low tolerance (±5% typical) low loss type component. A polypropylene or equivalent type capacitor should perform quite well. Some polyester film types may also be suitable for this application.

When used with the above-mentioned inverter transformer with the two lamps at full brightness, a 0.1µF capacitor yields an approximate operating frequency of 48kHz.

CURRENT LIMIT CIRCUIT OF THE BUCK CONVERTER

The buck regulator current control circuit utilizes peak current sense for shutting down the FET instantaneously under over current conditions. The sense resistor is comprised of several resistors in parallel to obtain the desired value.

DIMMING OF THE CCFL LAMPS

Dimming is accomplished by summing a DC current to the inverting input of the error amplifier (pin 7). When a voltage is available instead of current then a resistor can be used.

Figure 8 shows such an arrangement. The 1.6MΩ resistor connected to pin 7 that goes to brightness adjust control serves this purpose. There are several ways of generating the "Brightness Adjust" voltage. The simplest method is by using a potentiometer as shown in Figure 9.

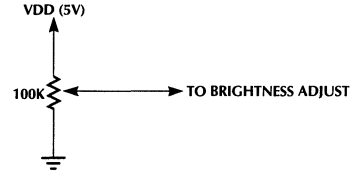


Figure 9. Dimming Voltage Generation.

In the event that the control signal is a PWM modulated digital signal, the circuit shown below may be used.

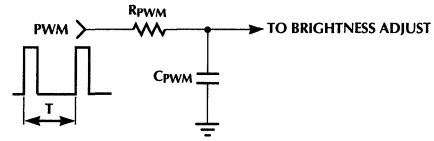


Figure 10. Dimming Voltage Generation using a PWM Signal.

If the PWM signal frequency is high compared to the bandwidth of the control loop, then it is possible to use the circuit of Figure 10 without the added R_{PWM} and C_{PWM}.

For proper operation, however, the following criterion must be met:

$$C_{PWM} \geq \frac{3T}{R_{PWM}} \quad (12)$$

Another method that can be used for dimming is by using a digital up down counter. In this method two push button type switches are used to selectively route the clock pulse either to "UP count" port or the "DOWN count" port. On initial turn-on the circuit requests full brightness. This can be changed by tying pins 12, 13, 19 and 20 of the counter chip to ground. In this condition the circuit will request a full dim condition. Resistors R_A, R_B, R_C and R_D are chosen to provide the required current to the brightness control input. These resistors are chosen to have the 8:4:2:1 ratio for approximately 16 levels of brightness control. For a higher control resolution, an eight bit counter can be used.

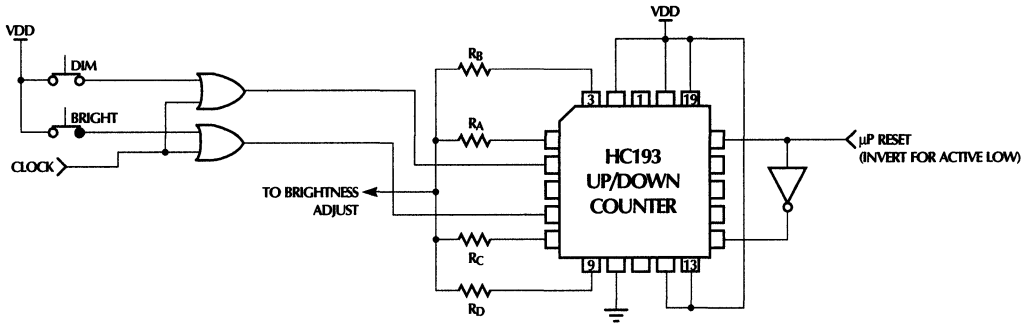


Figure 11. Dimming Voltage Generation using a Digital UP/DOWN Counter.

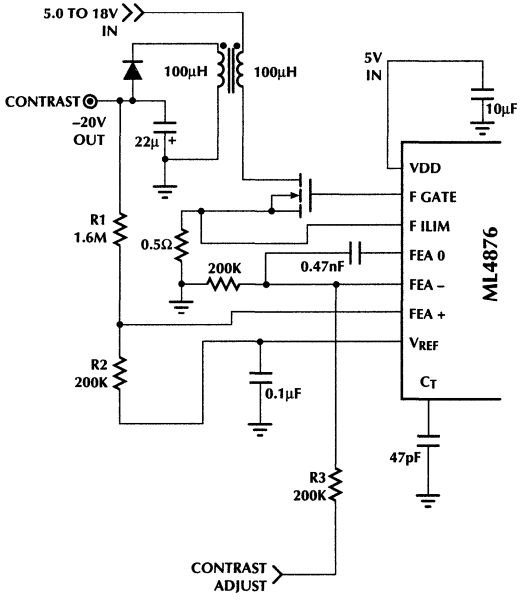


Figure 12. Negative Contrast Voltage Generator Circuit for ML4876 only.

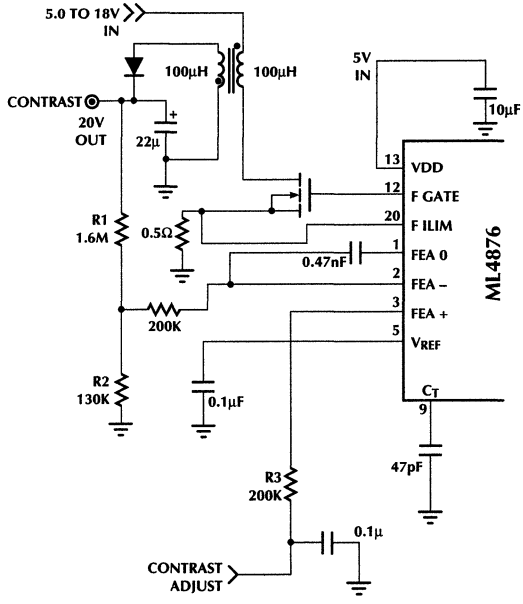


Figure 13. Positive Contrast Voltage Generator Circuit for ML4876 only.

CONTRAST VOLTAGE GENERATOR SECTION (ML4876 ONLY)

The ML4876 contains the necessary control circuitry to implement a positive or negative voltage for the LCD contrast control function. This controller is synchronized to the master clock of the circuit.

To generate a negative voltage the regulator can be configured as a flyback regulator. Figure 12, shows the negative contrast voltage control regulator configuration.

The output voltage of the regulator can be calculated by the following formula:

$$V_{OUT} = -V_{REF}\frac{R_1}{R_2} + \left(1+\frac{R_1}{R_2}\right)V- \qquad (13)$$

Where: V_{REF} = 2.5V, V_{OUT} is the negative contrast output voltage and V– is the voltage at the inverting pin of the error amplifier (pin 6).

When V– = 0V the output voltage can be calculated:

$$V_{OUT} = -V_{REF}\frac{R_1}{R_2} \qquad (14a)$$

Example: R_1 = 1.6M, R_2 = 200K

$$V_{OUT} = -2.5\frac{1.6M}{200k} = 20V \qquad (14b)$$

To generate a positive contrast control voltage the regulator can be configured as shown in Figure 13.

The output voltage of the regulator can be calculated by the following formula:

$$V_{OUT} = V_{REF}\left(1+\frac{R_1}{R_2}\right) \qquad (15)$$

SELECTION OF THE FLYBACK TRANSFORMER

The flyback transformer used in this application is an off the shelf item manufactured by various manufacturers. Depending on the output current other parts can be selected for optimum efficiency.

If the range of contrast control voltage is not very wide, the positive contrast voltage can be obtained from the boost configuration directly, thus eliminating one of the windings from Figure 13. If the contrast control voltage is required to adjust to zero, then the additional winding must be used.

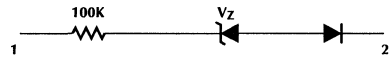
LAMP OUT DETECT

When there is no lamp in the socket, the output voltage will tend to rise to a high level anticipating the start of an actual lamp. This condition is detected by a resistor (R_6 for ML4874, R_8 for ML4876) which is connected to L RTD (pin 10). When the voltage rises above 16 volts at pin 10, the controller will shut down.

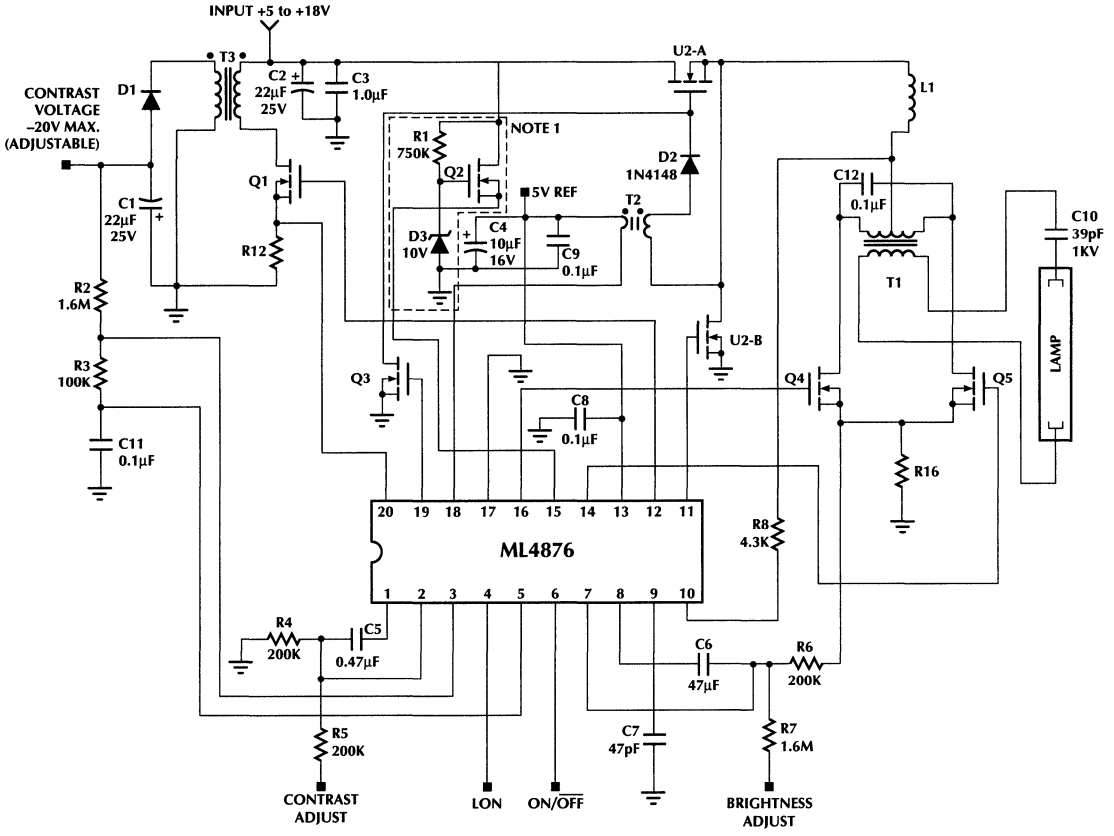
To accommodate different lamp types, sometimes it is desirable to have a voltage higher than 16 volts at the center-tap of the transformer. In this event, another resistor (R17, not shown) can be added between pin 10 and ground to form a voltage divider. The resultant voltage at pin 10 (L RTD) will be:

$$V_{PIN\,10} = V_{CENTER-TAP}\frac{R_{17}}{R_{17}+R_8} \qquad (16)$$

For applications that do not favor the shutting down of the controller, the output voltage can be limited by installing the following circuit, with terminal 1 connected to the center-tap of the transformer and terminal 2 connected to the junction of R_6 and R_7 (see Figure 14): ML4876 only.



When the voltage exceeds the designed value, the zener will breakdown and provide an additional feedback signal to lower the gain of the controller, thus limiting the output voltage.



NOTE 1
R1, D3, Q2 ARE OPTIONAL AND ALLOWS A BATTERY VOLTAGE RANGE FROM +7 TO +28V. REMOVING THESE COMPONENTS AND CONNECTING DIRECTLY TO THE INPUT VOLTAGE ALLOWS +5.0 TO +18V.

Figure 14. Application Schematic for the ML4876.

PARTS LIST OF A TYPICAL ML4874 BACKLIGHT CIRCUIT

All parts are SMD unless otherwise noted.

QTY.	DESCRIPTION	VENDOR/ PARTS	REV./ ISSUE
Resistors (All resistors are 1/4 watt)			
2	1.6M 5%	1206	R1, R4
1	82K 5%	1206	R2
1	100K Ohm 5%	1206	R3
2	1.0 Ohm 5%, 2 in parallel	1206	R5 (X2)
1	4.3K 5%	1206	R6
Capacitors			
1	33µF 6.3VDC Tantalum	Nichicon (F930J3366MC)	C1
1	22µF 25VDC Tantalum	Nichicon (F931D226MN)	C7
5	0.1µF 50VDC	1206	C2, C3, C8, C9
1	47pF 50VDC	0603	C5
1	0.1µF 63VDC Polyester	WIMA MKS-2 (or equal) leaded	C6
1	0.047µF 50VDC	0805	C4
1	39pF 1KV	leaded	C11
1	1µF/50V	1206	C10

QTY.	DESCRIPTION	VENDOR/ PARTS	REV./ ISSUE
Semiconductors			
1	1N4148	RLS4148-LL34	D1
2	2N7002	SOT-23	Q1, Q2
1	MMFD2N02E	SO 08 Dual FET	U2
1	MMFT3055ELT1	MOSFET SOT-223	Q3, Q4
Magnetics			
1	EPS136 #6345-020 or CTX210655-1	Sumida Coiltronics	T1
1	CP-4LBM 5201-JPS-021	Sumida	T2
1	CTX100-4 or CDR105	Coiltronics Sumida	L1
Lamp			
1	LFOM2476	Sharp	
Hardware			
6	Header pins 0.025 sq. posts		

PARTS LIST OF A TYPICAL ML4876 BACKLIGHT CIRCUIT

All parts are SMD unless otherwise noted.

QTY.	DESCRIPTION	VENDOR/ PARTS	REV./ ISSUE
Resistors (All resistors are 1206 unless otherwise noted)			
2	1.6M		R1, R2
1	200K		R3
2	200K		R4, R5
1	4.3K		R8
6	1.0 Ohm (resistors in parallel)		R9, R10, R11, R12 R13, R14, (R15, R16 Optional)
1	200K	0805	R6
1	1.6M	0805	R7
The following are on the break-off board			
2	10K Carbon, 10%, Leaded		R/PU (X2)
1	User selectable, Leaded		R Load
2	20K (Bourns 3352 Series, or similar)		R-POT (X2)
Capacitors			
2	22µF/25VDC Tantalum	Nichicon (F91E226MN)	C1, C2
1	1.0µF/50VDC	1206	C3
1	10µF/16VDC Tantalum	Nichicon (F931C106MB)	C4
2	0.047µF/50VDC	0805	C5, C6
1	47pF/50VDC	0603	C7
3	0.1µF/50VDC	1206	C8, C9, C11
1	39pF/1KV Ceramic Disk	Leaded	C10
1	0.1µF/63VDC	Leaded (WIMA MKS2)	C12

QTY.	DESCRIPTION	VENDOR/ PARTS	REV./ ISSUE
Diodes			
2	1N4148	RLS4148-LL34	D1, D2
1	Zener 10V	LL34	D3
Transistors			
2	2N7002	SOT-23	Q2, Q3
3	MMFT3055ELT1	MOSFET SOT-223	Q1, Q4 Q5
1	MMFD2N02E	Dual FET S008	U2
Magnetics			
2	CTX100-1 or CDR105	Coiltronics Sumida	L1, T3
1	EPS136 #6345-020 or CTX210655-1	Sumida Coiltronics	T1
1	CP-4LBM 5201-JPS-021 or Ferrite Bead 1Turn:2 Turns	Sumida	T2

G.A. Hall and J.H. Hwang

ML4824 Combo Controller Applications

GENERAL DESCRIPTION

This Application Note shows the step-by-step process to design a high performance supply. The equations shown in this document can also be used for different output voltages and total power.

The complete power supply circuit shown in Figure 6 demonstrates the ML4824's ability to manage high output power while easily complying with international requirements regarding AC line quality. The PFC section provides $380V_{DC}$ to a dual transistor current-mode forward converter. The output of the converter delivers +12V at up to 16 amps. The circuit operates from 80 to $264V_{AC}$ with both power sections switching at 100kHz.

THE PFC STAGE (Figure 1)

POWERING THE ML4824

The ML4824 is initialized once C_{30} is charged to 13V through R_{27} and R_{30}. PFC switching action now boosts the voltage on C_5 to 380V via T_1's primary inductance. T_1 then supplies a well regulated 13V for the ML4824 from its secondary winding and full wave rectifier consisting of D_3, D_4, C_{10} and C_{11}. T_1's primary to secondary turns ratio (N_{PRI}/N_{SEC}) is 25.5:1. For proper circuit operation, high frequency bypassing with low ESR ceramic or film capacitors on V_{CC} and V_{REF} is provided. Orderly PFC operation upon start-up is guaranteed when D_2 quick

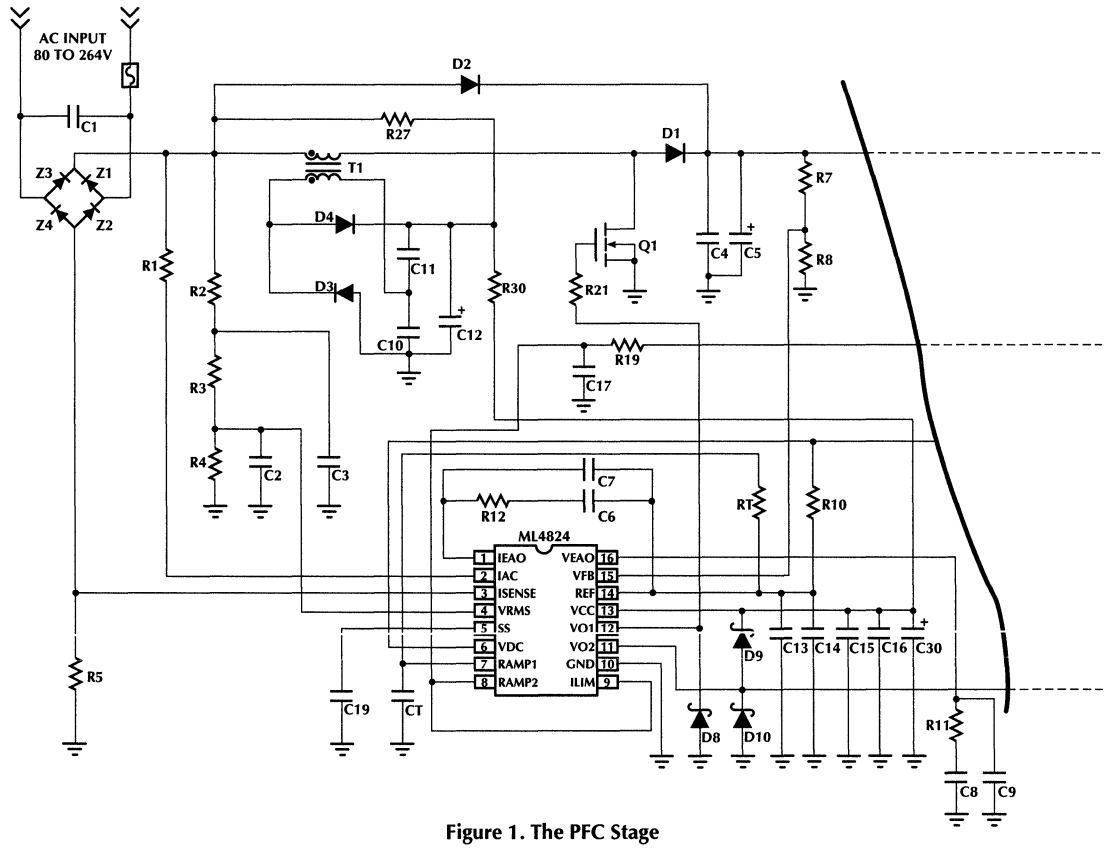


Figure 1. The PFC Stage

charges the boost capacitor to the peak AC line voltage before the boost switch Q_1 is turned on. This ensures the boost inductor current is zero before PFC action begins. The value of the regulated voltage on C_5 must always be greater than the peak value of the maximum line voltage delivered to the supply.

$$V_{C5} > \sqrt{2}V_{RMS(MAX)}$$
$$V_{C5} > (1.414)(264) \quad (1)$$
$$V_{C5} > 373V \text{ use } 380V$$

Because the ML4824 uses transconductance amplifiers the loop compensation networks are returned to ground (see the ML4824 data sheet for the error amplifier characteristics/ advantages). This eliminates the interaction of the resistive divider network with the loop compensation capacitors permitting a wide choice of divider values chosen only to minimize amplifier offset voltages due to input bias currents. For reliable operation R_7 must have a voltage rating of at least 400 volts.

Calculate the resistor divider ratio R_7/R_8.

$$\frac{R_7}{R_8} = \frac{V_{C5}}{2.50} - 1$$
$$\frac{R_7}{R_8} = \frac{380}{2.5} - 1 \quad (2)$$
$$\frac{R_7}{R_8} = 151$$

SELECTING THE POWER COMPONENTS

The ML4824 PFC section operates with continuous inductor current to minimize peak currents and maximize the available power. The inductance value required for continuous current operation in the typical application is found in equation 3.

$$T_{1(PRI)} = \frac{0.445V_{RMS(MAX)^2}}{(f_{PFC})(P_{OUT})}$$
$$T_{1(PRI)} = \frac{(0.445)(264)^2}{(1\times10^5)(200)} \quad (3)$$
$$T_{1(PRI)} = 1.55mH \text{ use } 1.5mH$$

The boost diode D_1 and switch Q_1 are chosen with a reverse voltage rating of 500V to safely withstand the 380V boost potential. The average and peak currents respectively through these components are:

$$I_{AVG} = \frac{\pi P_{OUT}}{2\sqrt{2}V_{RMS(MIN)}}$$
$$I_{AVG} = \frac{(3.1416)(200)}{(2)(1.414)(80)} \quad (4)$$
$$I_{AVG} = 2.78A$$

$$I_{PEAK} = \frac{\pi I_{AVG}}{2}$$
$$I_{PEAK} = \frac{(3.1416)(2.78)}{2} \quad (5)$$
$$I_{PEAK} = 4.37A$$

The boost capacitor value is chosen to permit a given output voltage hold-up time in the event the line voltage is suddenly removed.

$$C_5 \geq \frac{2(P_{OUT})(t_{HLD})}{V_{C5(NOM)^2} - V_{C5(MIN)^2}} \quad (6)$$

Where:

t_{HLD} = hold-up time (sec)

$V_{C5(MIN)}$ = minimum voltage on C_5 at which the PWM stage can still deliver full output power

A key advantage of using leading/trailing edge modulation is that a large portion of the inductor current is "dumped" directly into the load (PWM stage transformer) and not the boost capacitor. This relaxes the ESR requirement of the boost capacitor. For reference, equation 7 should be used as a starting point when choosing C_5's maximum ripple current rating (at 120Hz).

$$I_{RMS(C5)} = \frac{I_{OUT(C5)}}{\sqrt{2}} \quad (7)$$

$$\left(I_{PEAK} = \sqrt{2}\, I_{RMS(C5)}\right) \quad (7a)$$

SELECTING THE POWER SETTING COMPONENTS

The maximum average power delivered by the PFC stage is easily set using the following procedure:

1. Find the resistive divider ratio that results in the voltage at the V_{RMS} pin being equal to 1.20V at the lowest line voltage. The voltage at this pin must be well filtered and yet able to respond well to transient line voltage changes.

$$\frac{R_4}{R_{TOT}} = \frac{1.20\pi}{2\sqrt{2}V_{RMS(MIN)}} \quad (8)$$

The resistor and capacitor values in the typical example were found empirically to offer the lowest ripple voltage and still respond well to line voltage changes. Should a ratio be required which is greatly different from that found in equation 8, adjust the filter capacitor values according to equations 9 and 10.

$$C_3 = \frac{R_{TOT}}{2\pi f_1 R_2 (R_3 + R_4)} \quad (9)$$

$$C_2 = \frac{\left(1 + \frac{R_4 R_{TOT}}{R_2 (R_3 + R_4)}\right)}{2\pi f_2 R_4} \quad (10)$$

Where :

$f_1 = 15Hz, f_2 = 23Hz$

$R_{TOT} = R_2 + R_3 + R_4$

2. Find the constant of proportionality k_m of the multiplier gain k in equation 11a. To obtain "brown-out" action below the lowest input voltage the maximum gain of the multiplier must be used when finding k_M. The maximum gain (0.328) occurs when the V_{RMS} input of the multiplier is 1.20V. Equation 11(ref) is the general expression for the multiplier gain versus the line voltage.

$$k = \frac{k_M}{V_{RMS}^2}(ref) \quad (11)$$

$$k_M = kV_{RMS(MIN)}^2$$

$$k_M = (0.328)(80)^2 \quad (11a)$$

$$k_M = 2099$$

3. Now select the value of R_1 which permits the greatest multiplier output current without saturating the output. The maximum output current of the multiplier is 200µA.

$$R_1 \geq \frac{k\sqrt{2}V_{RMS(MIN)}(V_{EAO} - 1.5)}{200 \times 10^{-6}}$$

$$R_1 \geq \frac{(0.328)\sqrt{2}(80)(6.8 - 1.5)}{200 \times 10^{-6}} \quad (12)$$

$R_1 \geq 983k\Omega$ use $1M\Omega$

4. Selecting the value of the current sense resistor completes the calculations for the power setting components.

$$R_5 \leq \frac{R_{MULO}(V_{EAO} - 1.5)k_M}{(R_1)(P_{OUT})}$$

$$R_5 \leq \frac{(3500)(6.8 - 1.5)(2099)}{(1 \times 10^6)(200)} \quad (13)$$

$R_5 \leq 0.195\Omega$ use 0.15Ω

Where :

R_{MULO} = multiplier output termination resistance (3.5k)

VOLTAGE LOOP COMPENSATION (Figure 2)

Maximum transient response of the PFC section, without instability, is obtained when the open loop crossover frequency is one-half the line frequency. For this application the compensation components (pole/zero pair) are chosen so that the closed loop response decreases at 20dB/decade, crossing unity gain at 30Hz, then immediately decreasing at 40dB/decade. The error amplifier pole is placed at 30Hz and an effective zero at one-tenth this frequency or 3Hz. First find the crossover frequency (G_{PS} = 1) of the power stage. For reference, equation 15 finds the power stage pole, equation 16 the power stage DC gain.

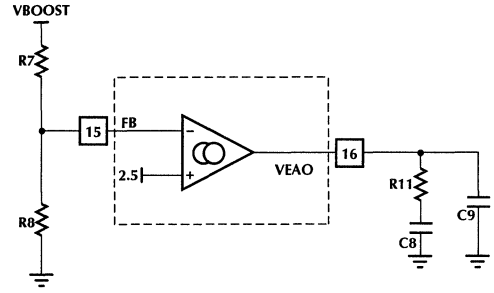


Figure 2. Voltage Amp Compensation

$$f_C = \frac{P_{IN(AVG)}}{2\pi V_{C5} V_{EAO(MAX)} C_5}$$

$$f_C = \frac{200}{(2)(3.1416)(380)(5.3)(270 \times 10^{-6})} \quad (14)$$

$f_C = 58.5Hz$

$$f_P = \frac{1}{\pi R_L C_5}$$

$$f_P = \frac{1}{(3.1416)(722)(270 \times 10^{-6})} \quad (15)$$

$$f_P = 1.63\text{Hz}$$

Where :

$$R_L = \frac{V_{C5}{}^2}{P_{OUT}}$$

$$G_{PS(DC)} = \frac{\sqrt{2} f_C}{f_P}$$

$$G_{PS(DC)} = \frac{(1.414)(58.5)}{(1.63)} \quad (16)$$

$$G_{PS(DC)} = 35.9 \ (31\text{dB})$$

Now the gain of the power stage at 30Hz is calculated.

$$G_{PS(30Hz)} = \frac{f_C}{30}$$

$$G_{PS(30Hz)} = \frac{58.5}{30} \quad (17)$$

$$G_{PS(30Hz)} = 1.95 \ (5.8\text{dB})$$

The power stage gain will be attenuated by the resistive divider R_7/R_8 according to equation 18.

$$G_{RDIV} = \frac{R_8}{R_7 + R_8}$$

$$G_{RDIV} = \frac{(2.37)}{(357 + 2.37)} \quad (18)$$

$$G_{RDIV} = 6.59 \times 10^{-3} \ (-43.6\text{dB})$$

The amount of error amplifier gain required to bring the open loop gain to unity at 30Hz is the negative of the sum of the power stage plus divider stage gain (attenuation):

$$G_{EA} = -(G_{PS(30)} + G_{RDIV})$$

$$G_{EA} = -(5.8 + (-43.6)) \quad (19)$$

$$G_{EA} = 37.8\text{dB} \ (77.6\text{V/V})$$

The value of R_{11}, which sets the high frequency gain of the error amplifier, can now be determined.

$$R_{11} = \frac{G_{EA}}{g_M}$$

$$R_{11} = \frac{77.6}{65.7 \times 10^{-6}} \quad (20)$$

$$R_{11} = 1.18\text{M use } 1.1\text{M}$$

Calculate C_8 which together with R_{11} sets the zero frequency at 3Hz.

$$C_8 = \frac{1}{2\pi R_{11} f_Z}$$

$$C_8 = \frac{1}{(2)(3.1416)(1.1 \times 10^6)(3)} \quad (21)$$

$$C_8 = 48\text{nF (use 47nF)}$$

Since the pole frequency is ten times the zero frequency the pole capacitor C_9 will be one-tenth the value of C_8.

$$C_9 = \frac{C_8}{10}$$

$$C_9 = \frac{47 \times 10^{-9}}{10} \quad (22)$$

$$C_9 = 4.7\text{nF}$$

CURRENT LOOP COMPENSATION (Figure 3)

The current loop is compensated exactly like the voltage loop with the exception of the choice of the open loop crossover frequency. To prevent interaction with the voltage loop, the current loop bandwidth should be greater than ten times the voltage loop crossover frequency but no more than one-sixth the switching frequency or 16.7kHz. The power stage crossover frequency is found in equation 23, the pole frequency in 24 and for reference the power stage DC gain is found in equation 25.

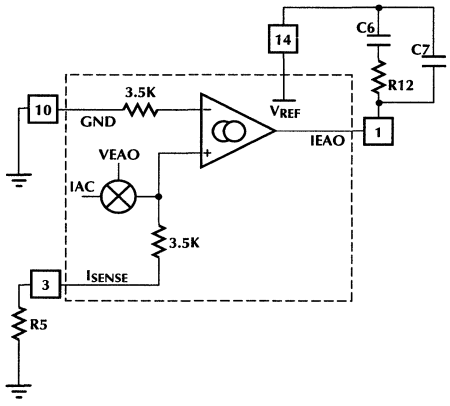


Figure 3. Current Amp Compensation

$$f_C = \frac{R_5 V_{C5}}{2\pi T_{1(PRI)} V_{RAMP(P-P)}}$$

$$f_C = \frac{(0.15)(380)}{(2)(3.1416)(1.5\times10^{-3})(2.5)} \quad (23)$$

$$f_C = 2.42\text{kHz}$$

$$f_P = \frac{1}{\pi R_L C_5}$$

$$f_P = \frac{1}{(3.1416)(722)(270\times10^{-6})} \quad (24)$$

$f_P = 1.63$Hz same as equation 15

$$G_{PS(DC)} = \frac{\sqrt{2} f_C}{f_P}$$

$$G_{PS(DC)} = \frac{(1.414)(2.42\times10^3)}{(1.63)} \quad (25)$$

$G_{PS(DC)} = 2099$ (66.4dB)

Find the gain of the power stage at 16.7kHz.

$$G_{PS(16.7kHz)} = \frac{f_C}{16.7\times10^3}$$

$$G_{PS(16.7kHz)} = \frac{2.42\times10^3}{16.7\times10^3} \quad (26)$$

$$G_{PS(16.7kHz)} = 1.45\times10^{-1}(-16.8\text{dB})$$

The current loop contains no attenuating resistors so proceed to find the error amplifier gain in equation 27.

$$G_{EA} = -(-G_{PS(16.7kHz)})$$

$$G_{EA} = -(-16.8) \quad (27)$$

$$G_{EA} = 16.8\text{dB}(6.9\text{V/V})$$

Now determine the value of the current error amplifier setting resistor R_{12}.

$$R_{12} = \frac{G_{EA}}{g_m}$$

$$R_{12} = \frac{6.9}{181\times10^{-6}} \quad (28)$$

$$R_{12} = 38.1\text{k use } 36\text{k}$$

Calculate the value of C_6 to form the zero at 1.6kHz.

$$C_6 = \frac{1}{2\pi R_{12} f_Z}$$

$$C_6 = \frac{1}{(2)(3.1416)(36\times10^3)(1.67\times10^3)} \quad (29)$$

$C_6 = 2.6$nF (use 2.7nF)

The pole capacitor C_7 is one-tenth the value of C_6.

$$C_7 = \frac{C_6}{10}$$

$$C_7 = \frac{2.7\times10^{-9}}{10} \quad (30)$$

$$C_7 = 270\text{pF}$$

THE PWM STAGE (Figure 4)

SOFT-STARTING THE PWM STAGE

The ML4824 features a dedicated soft-start pin for controlling the rate of rise of the output voltage and preventing overshoot during power on. The controller will not initiate soft-start action until the PFC voltage reaches its nominal value thereby preventing stalling of the output voltage due to excessive PFC currents. Furthermore, PWM action will be terminated in the event that the ML4824 loses power or if the PFC boost voltage should fall below $228V_{DC}$. The soft-start capacitor value (C_{19}) for 25ms of delay is found in equation 31.

$$C_{19} = (t_{SS})\left(\frac{50\times10^{-6}}{1.25}\right)$$

$$C_{19} = (0.025)\left(\frac{50\times10^{-6}}{1.25}\right) \qquad (31)$$

$$C_{19} = 1\mu F$$

SETTING THE OSCILLATOR FREQUENCY

There are two versions of the ML4824. The ML4824-1 where the PFC and PWM run at the same frequency and ML4824-2 where the PWM stage is 2X PFC frequency.

ML4824-1

In general it is best to choose a small valued capacitor C_1 to maximize the oscillator duty cycle (minimize the C_1 discharge time). Too small a value capacitor can increase the oscillator's sensitivity to phase modulation caused by stray field voltage induction into this node. For the practical example a 470pF capacitor was first chosen for C_1. Equation 32 is accurate with values of R_1 greater than 10k.

$$R_T \cong \frac{1}{0.51 f_{SW} C_T} - 961C_T$$

$$R_T \cong \frac{1}{0.51(1\times10^5)(470\times10^{-12})} - (961)(470\times10^{-12}) \qquad (32)$$

$$R_T \cong 41.2k$$

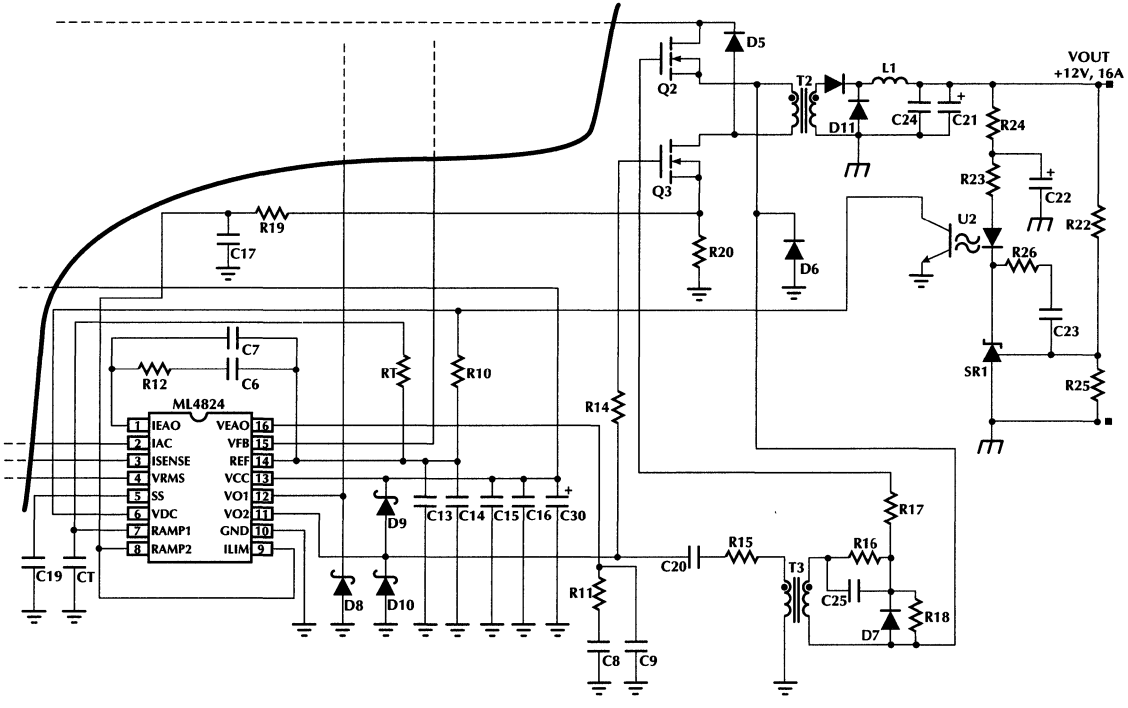


Figure 4. The PWM Stage

Note :

$t_{TOT} = t_{ON} + t_{OFF}$

$t_{ON} \cong 0.51 R_T C_T$

$t_{OFF} \cong 490 C_T$

ML4824-2

The ML4824-2 allows the user to operate the PWM stage at twice the PFC frequency, thereby reducing the physical size of the PWM stage magnetics and filter components. The PFC frequency is the same as the external oscillator frequency. The PWM frequency is formed by comparing the oscillator ramp voltage to internal voltage references which ideally make the duty cycle of the 2 waveforms generated during each oscillator cycle identical. The PWM section duty cycle must be balanced to minimize phase jitter. This is accomplished by making the oscillator dead-time (C_1 discharge time) equal to 2.5% of the total period. First choose the C_1 value from equation 33.

$$C_T \cong \frac{0.025}{490 fsw} \quad (33)$$

Now R_1 is found from equation (34) which is identical to equation 32.

$$R_T \cong \frac{1}{0.51 fsw C_T} - 961 C_T \quad (34)$$

As a final test, an in-circuit check of 2 adjacent PWM cycles should be examined for duty cycle balance. For more detail involving duty cycle balancing please refer to Micro Linear's Application Note 34.

CURRENT LIMIT

The PWM power stage operates in current mode using R_{20} to generate the voltage ramp for duty cycle control. The ML4824 limits the maximum primary current via an internal 1V comparator which when exceeded terminates the drive to the external power MOSFETs.
Maximum primary current is:

$$I_{PRI(MAX)} = \frac{1}{R_{20}}$$

$$I_{PRI(MAX)} = \frac{1}{0.5} \quad (35)$$

$$I_{PRI(MAX)} = 2 \text{Amps}$$

VOLTAGE MODE (FEED-FORWARD)

Should voltage mode control be used it is necessary to know C_5's peak voltage in order to choose the correct ramp generating components. Equation 36 finds the worse case peak to peak ripple voltage across C_5. To find the peak voltage divide the ripple voltage by two and add it to the regulated boost voltage. Remember that since the ML4824 employs leading/trailing modulation the actual peak to peak ripple voltage will generally be much less than the calculated value.

$$V_{R(C5)} = I_{OUT(C5)} \sqrt{\left(\frac{1}{4\pi f_L C_5}\right)^2 + ESR(C_5)^2} \quad (36)$$

Where :

f_L = line frequency

Solve equation 37 for the ramp resistor value. The ramp capacitor value should be in the range of 470pF – 10000pF. Choose a resistor with an adequate voltage rating to withstand the boost voltage.

$$R_{RAMP} = \frac{\sigma_{(MAX)}}{C_{RAMP} f_{SW} \ln\left(1 - \frac{V_{REF}}{V_{C5} + 0.5V_R}\right)} \quad (37)$$

Where:

$\sigma_{(MAX)}$ = maximum PWM duty cycle (0.45 for the ML4824–1)

V_R = peak to peak boost capacitor ripple voltage (equation 36)

THE POWER TRANSFORMER TURNS RATIO

The minimum output voltage at the secondary of T_2 is found in equation 38.

$$V_{SEC(MIN)} = \frac{V_{OUT}}{\sigma_{(MAX)}} + V_F$$

$$V_{SEC(MIN)} = \frac{12}{0.45} + 1.0 \quad (38)$$

$$V_{SEC(MIN)} = 27.7 \text{Volts}$$

The secondary voltage was chosen to be 30 volts to increase the output voltage hold up time. The transformer turns ratio is easily found from equation 39.

$$\frac{N_{PRI}}{N_{SEC}} = \frac{V_{C5}}{V_{SEC(MIN)}}$$

$$\frac{N_{PRI}}{N_{SEC}} = \frac{380}{30} \quad (39)$$

$$\frac{N_{PRI}}{N_{SEC}} = 38:3$$

The maximum secondary current with the output shorted is limited by equation 40.

$$I_{SEC(MAX)} = \frac{I_{PRI(MAX)} N_{PRI}}{N_{SEC}}$$

$$I_{SEC(MAX)} = \frac{(2)(38)}{3} \qquad (40)$$

$$I_{SEC(MAX)} = 25.3\text{Amps}$$

The output inductor and rectifier were chosen with maximum current ratings larger than the maximum secondary current.

OUTPUT FILTER COMPONENT FILTER SELECTION

L_1's value was chosen to efficiently minimize output ripple current thereby easing the ESR requirement of the filter capacitor. C_{21}'s ESR value is the dominant contributor to the output ripple. The maximum ESR value required is found in equation 41.

$$ESR_{(C21)} \leq \frac{V_R L_1 f_{SW}}{V_{SEC} \sigma_{(MAX)}} \qquad (41)$$

Where :

V_R = peak to peak output ripple voltage

OUTPUT VOLTAGE COMPENSATION

A TL431 shunt regulator SR_1 and opto-isolator U_2 perform output voltage setting and regulation. The opto crosses the primary to secondary safety boundary varying the voltage on the VDC pin to keep the output voltage constant against line and load changes. Using current mode control simplifies loop compensation leaving only a single pole and zero in the output stage. The pole is created from the output capacitor and equivalent load resistance. The zero is formed from the filter capacitor and its ESR. In this example, the action of the zero occurs well after the closed loop response has crossed unity, so it was not compensated with a pole. The output pole is canceled increasing the overall bandwidth by the addition of R_{26} and C_{23} which form a zero with TL431. For more information on using the TL431, including gain/phase versus frequency characteristics, please refer to the Texas Instruments Linear Data Handbook.

3.3V OUTPUT DESIGN CHANGES (Figure 5)

The latest microprocessors and support circuitry require a 3.3V supply for proper operation. The ML4824 is ideal for these applications including the energy efficient, ecologically friendly "Green PC's". If the total output power required varies greatly from 200 watts it will be necessary to re-select certain components beginning with the PFC stage. T_2's turn ratio must be adjusted according to equation 39 and another low current secondary winding added using the same turns ratio as originally found for the +12 volts. This second winding is necessary to power the TL431/opto circuit as the 3.3V output is not adequate to fully bias the feedback circuitry. C_{21} may be increased to reduce the output ripple voltage. The figure below displays a 3.3V output stage capable of supplying 16 amps.

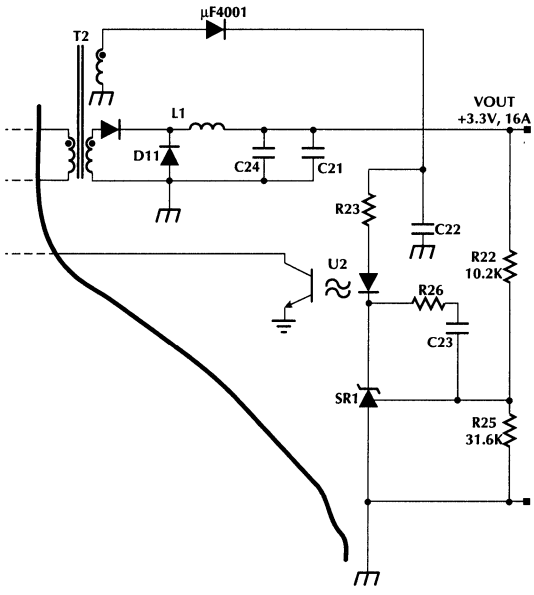


Figure 5. 3.3V Output Stage

NOTE: For more information see Application Note 34.

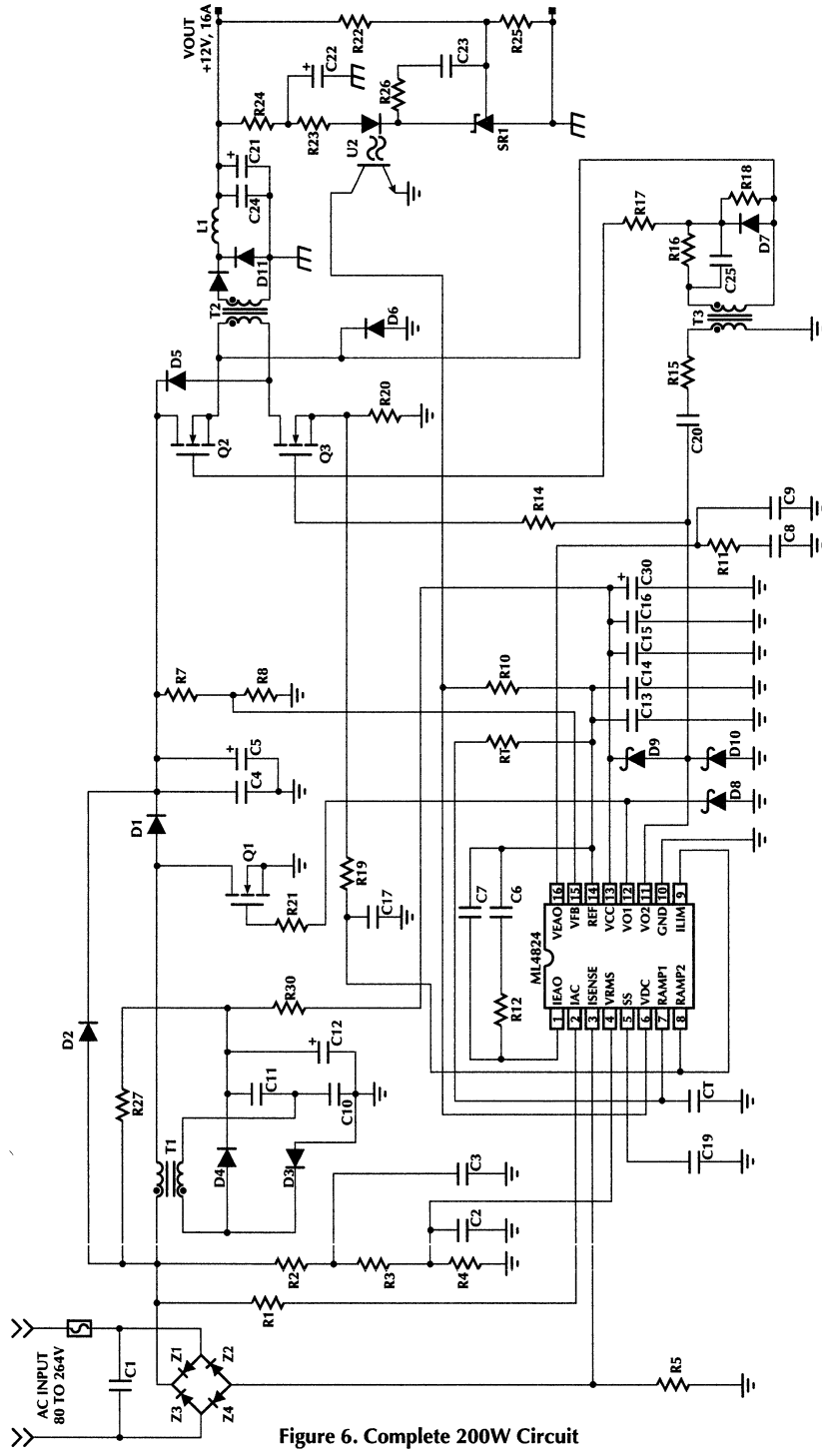


Figure 6. Complete 200W Circuit

ML4824, A Novel Method for an Off-Line PFC-PWM Combo Controller

Jeffrey H. Hwang
K. Kit Sum

INTRODUCTION

One of the most undesirable quantities experienced by utility companies is the high harmonic content of the line current. The harmonic content of this line current tends to cause transformer overheating at the substations, which are responsible for providing power to all sectors of a given area. For three-phase distribution, neutral currents will flow in the presence of these harmonics. For single-phase distribution, the narrow conduction angle demanded by capacitive input filters in switching power converters causes high harmonic content in the current waveform, resulting in lower operating efficiency.

A viable solution to this problem is the inclusion of a power factor correction (PFC) stage to facilitate more efficient power usage as well as lowering the harmonic content of the line current.

The most popular topology for this task is the switched-mode boost converter. Here the boost converter stage is inserted between the input rectifier and the bulk storage capacitor. This forces the input current to be in phase with the input voltage and provides a boosted D.C. voltage reservoir for the following power stage.

In many instances the power supply system must interface to a wide range input voltage (80-264V) requiring the boosted voltage be equal to or greater than 380VDC. For safe operation a capacitor with a voltage rating of at least 400V is necessary. Traditional cascaded power stages require large bulk capacitance values with low ESR to minimize peak to peak ripple voltage and lower self heating. Together these requirements result in a costly capacitor.

To understand why the bulk capacitor requirements are traditionally so stringent consider the circuit shown in Figure 1, a PFC power stage with resistive load. The bulk capacitor C1 must supply load current I0 when VSW is on, storing energy in the boost inductor L1. It must also "absorb" the peak current from L1 each time VSW switches off. The result of these currents into and out of C1 is a large ripple voltage across it. It is this large current with steep wavefronts that place the high demand on C1's bulk capacitance and ESR values to minimize output ripple.

Next, consider Figures 2 and 3, a PFC stage followed by an "unsynchronized" PWM stage. (**Note 1:** In this note the terms "unsynchronized" and "synchronized" are used to describe the switching action of 2 power switches operating from the same system clock. The switches are "synchronized" when one of them (SW2) turns on when the other (SW1) turns off. They are "unsynchronized" when both are switched on at the same time.) Here SW1 and SW2 are switched on and off at the same time. The peak currents and therefore the ripple voltage is less than a PFC stage with a resistive load. Even further reductions are possible by "synchronizing" the 2 stages (Figures 4 and 5).

Micro Linear's ML4824 Combo Controller IC is an integrated solution for systems benefitting from the advantages made possible by synchronizing the 2 cascaded power stages. In this application note the differences between the traditional combo modulation scheme (unsynchronized or trailing edge modulation) and the ML4824's leading/trailing edge modulation scheme are explained. A typical application is shown and test results are compared with the traditional approach. Then, a detailed look is taken inside the ML4824 and key design formulas are reviewed which enable the user to begin their own design.

CASCADE POWER CONVERTER

The cascade connection of power stages is a very effective and powerful tool in the design of state-of-the-art high frequency switch mode power converters (1). In recent years, power factor corrected power converters are rapidly gaining popularity. They offer improved performance when compared to traditional off-line switching power converters. However, special system stability considerations must be made.

Traditional trailing edge modulation results in a momentary no-load condition when the buck switch is turned off. This condition makes loop compensation difficult as it results in 2 poles located close to the RHPZ (Right Half Plane Zero) already in play because the boost inductor operates in continuous conduction current mode. Synchronous switching techniques as employed in the ML4824 push these poles further out in frequency allowing unity gain crossover to be placed at as high as one-half the line frequency.

For example, consider a single power stage boost converter as shown in Figure 1. The load of this stage is connected to the output filter and its value affects the loop response of the converter. When the load is reduced, the poles due to the inductor and the capacitor become closer and the phase margin is reduced.

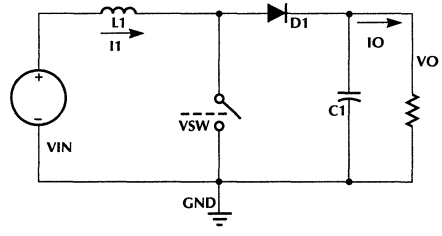


Figure 1. A Single Boost Power Stage with a Load.

In the cascade power stage, the load could be momentarily connected or disconnected. (See Figure 2 for a boost-buck cascade stage.) Many systems attempt to reduce the no load period by speeding up the loop response for the second stage and hence, a second (usually faster) clock has to be used resulting in a more complicated system.

TRAILING EDGE MODULATION AND LEADING EDGE MODULATION

Conventional pulse width modulation (PWM) employs trailing edge modulation in which the switch will turn on right after the trailing edge of the system clock. Then the error amplifier output voltage is compared with the modulating ramp. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned OFF. When the switch is ON, the inductor current will ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 3 shows a typical trailing edge control scheme.

In the case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock; when the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during the OFF time of the switch. Figure 4 shows a leading edge control scheme.

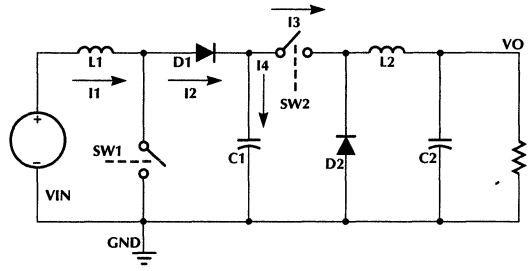


Figure 2. A Cascade Boost-Buck Power Converter without Synchronous Switching.

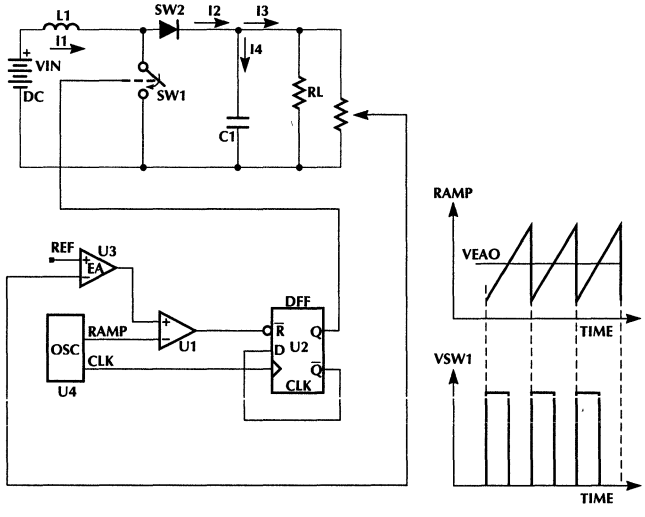


Figure 3. Trailing Edge Modulation Control Scheme.

THE OUTPUT VOLTAGE RIPPLE OF THE PFC STAGE

If the boost-buck cascade power converter of Figure 2 is applied to the off-line PFC/PWM power converter, the output ripple voltage of the PFC stage can be separated into two portions. One portion is due to the voltage drop across the C1's ESR. The other is due to dv/dt of C1. Assuming both converters are in the Continuous Conduction Mode (CCM), and conventional trailing edge modulation without synchronous switching is used, the ripple voltage is

$$\text{Total Ripple Voltage} = I_{2MAX} \times ESR + \frac{0.433 \times I_{2MAX}}{C_1 \times f_{PFC}} \quad (1)$$

$$I_{2MAX} = \frac{\text{Average Input Power} \times \sqrt{2}}{\text{Efficiency} \times V_{INRMS}} \quad (2)$$

If the dv/dt ripple voltage is dominant, dv reaches maximum when the phase of the input voltage waveform is at 60° or 120°.

One of the advantages of the new control scheme is that only one single system clock. Switch 1 (SW1) turns off and switch 2 (SW2) turns on at the same instant to minimize the momentary no load period, thus lowering ripple voltage generated by the switching action. With synchronous switching, the ripple voltage of the first stage is reduced.

Figure 5 shows the boost-buck cascade power converter with synchronous switching which differs from Figure 2 only in the switching sequence.

The ripple voltage of Figure 5 is

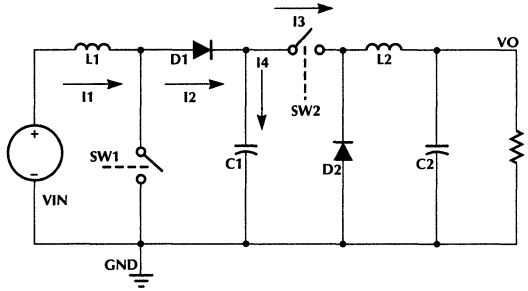


Figure 5. Synchronous Switching Cascade Power Converter.

Total Ripple Voltage =

$$\left(I_{2MAX} - I_3\right) \times ESR + \frac{0.433 \times \left(I_{2MAX} - I_3\right)}{C_1 \times f_{PFC}} \quad (3)$$

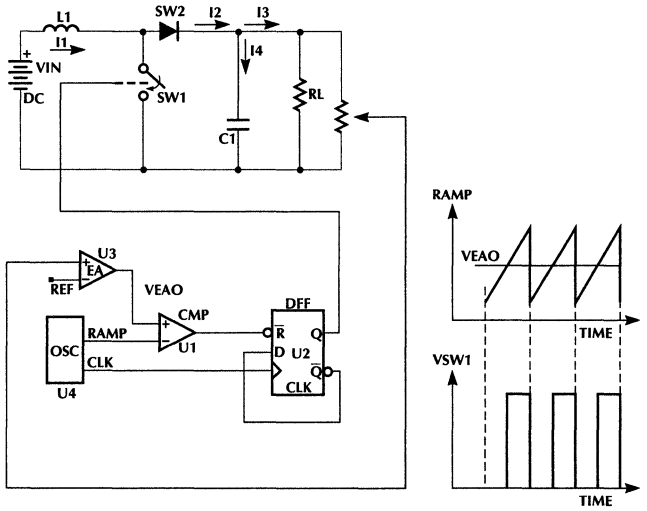


Figure 4. Leading/Trailing Edge Modulation Control Scheme.

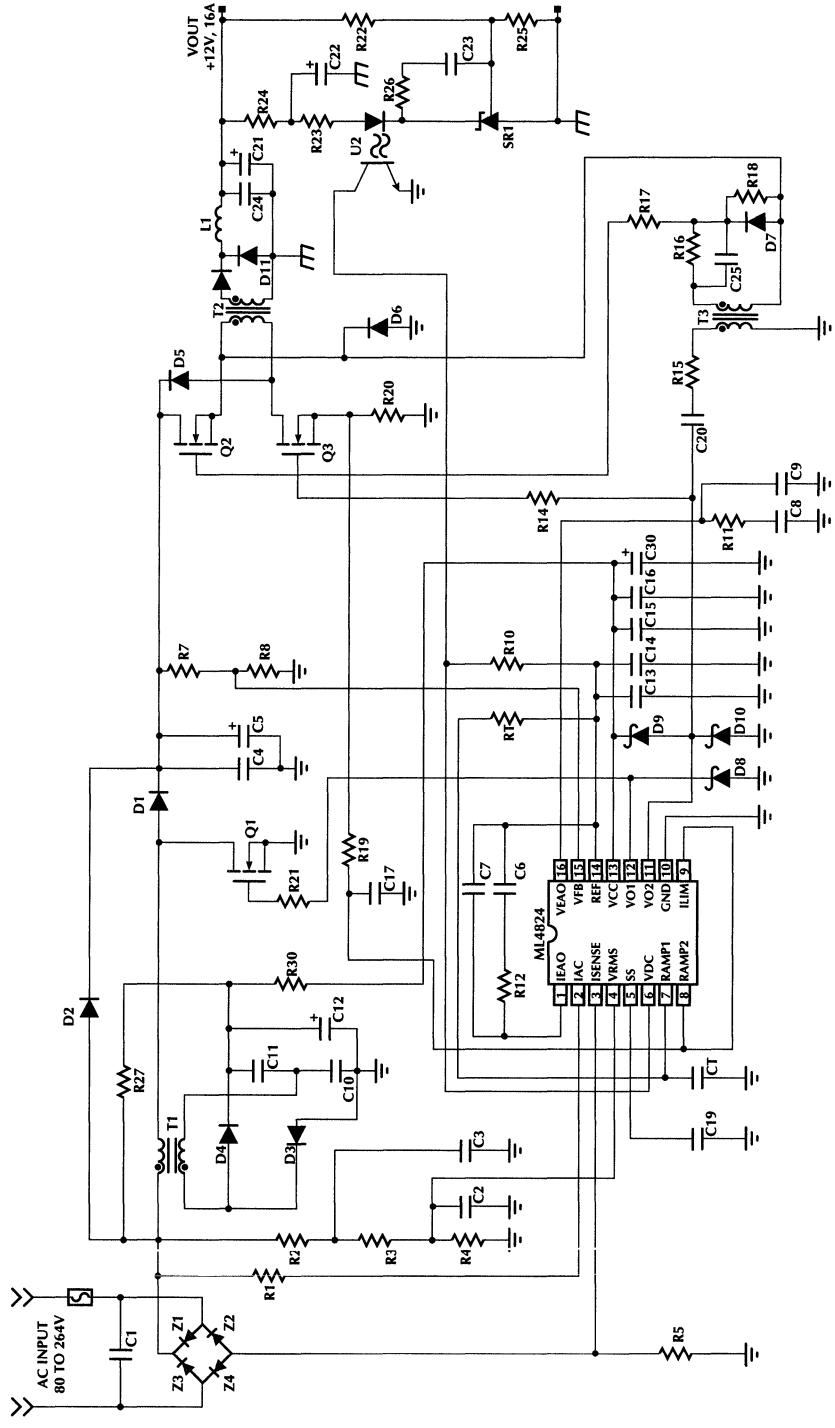


Figure 6. A 200W Off-Line PFC/PWM Power Converter with Synchronous Switching.

SYNCHRONOUS SWITCHING IN OFF-LINE PFC-PWM CASCADE POWER CONVERTER

A 200W off-line PFC/PWM cascade converter has been evaluated. Figure 6 shows the schematic of the 200W off-line PFC PWM cascade converter. The results show that the 120Hz component of the output ripple voltage has been reduced by 30%.

EXPERIMENTAL RESULTS

By virtue of the leading edge modulation PFC stage, working together with the trailing edge modulation PWM stage the system performance is enhanced. A comparison was made between the ML4824 and the ML4819 which employs trailing edge modulation for both power stages. The ML4819 is designed to function as a peak current controller with current mode PWM for the output stage. The test conditions are

C_{DC} = 50µF, V_{IN} = 220V A.C.,

Average Input Power = 75W,

f_{PFC} = 80KHz, and L_{PFC} = 1.5mH

See Figure 7.

APPLICATION CIRCUIT

POWER FACTOR SECTION

The function of the power factor correction section is to ensure the current follows the voltage in time and amplitude proportionally. This means that, for steady-state constant output power conditions, the current amplitude will follow the voltage amplitude in the same proportion at any instant in time. When the voltage amplitude is at 100%, current amplitude will be maximum. When the voltage is at 50% amplitude, the current amplitude will be at half its maximum value.

The result is a sinusoidal current waveform in phase with the incoming sinusoidal voltage waveform.

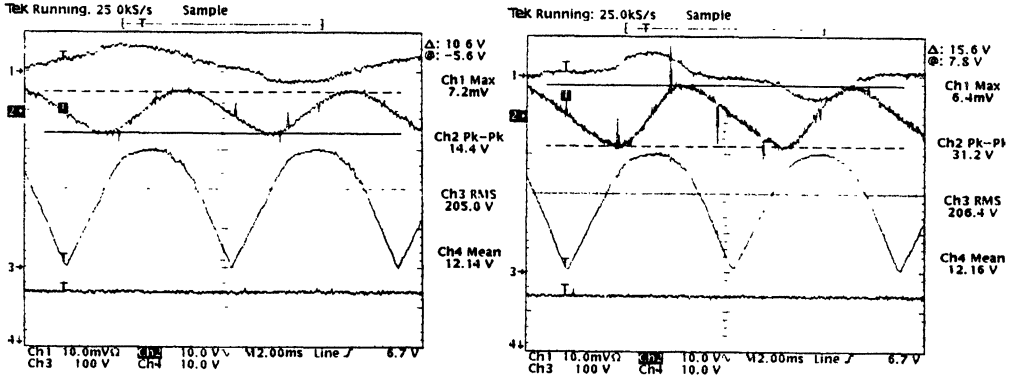
The power factor correction section is comprised of a boost type power stage with primary side of inductor T_1 as the input inductor. The secondary side is used as an auxiliary voltage source for powering the control circuit.

Since this stage is concerned with current processing, and the frequency of the current is related to the line frequency, the voltage control loop for this section is forced to have a slow response to allow the current to follow the voltage. This slow voltage loop response necessitates the addition of another power stage for faster and more accurate voltage processing.

The power factor correction section derives its timing from the same oscillator as the pulse width modulation section. This section has its own current limit comparator for current mode control. A comparator is also used for supplying over voltage protection commands.

ML4824 TEST RESULTS

ML4819 TEST RESULTS



(7a) (7b)

Figure 7. Comparison of Leading/Trailing Edge Modulation (Fig. 7a) to Trailing Edge Modulation only (Fig. 7b). (Middle traces are output ripple voltage.)

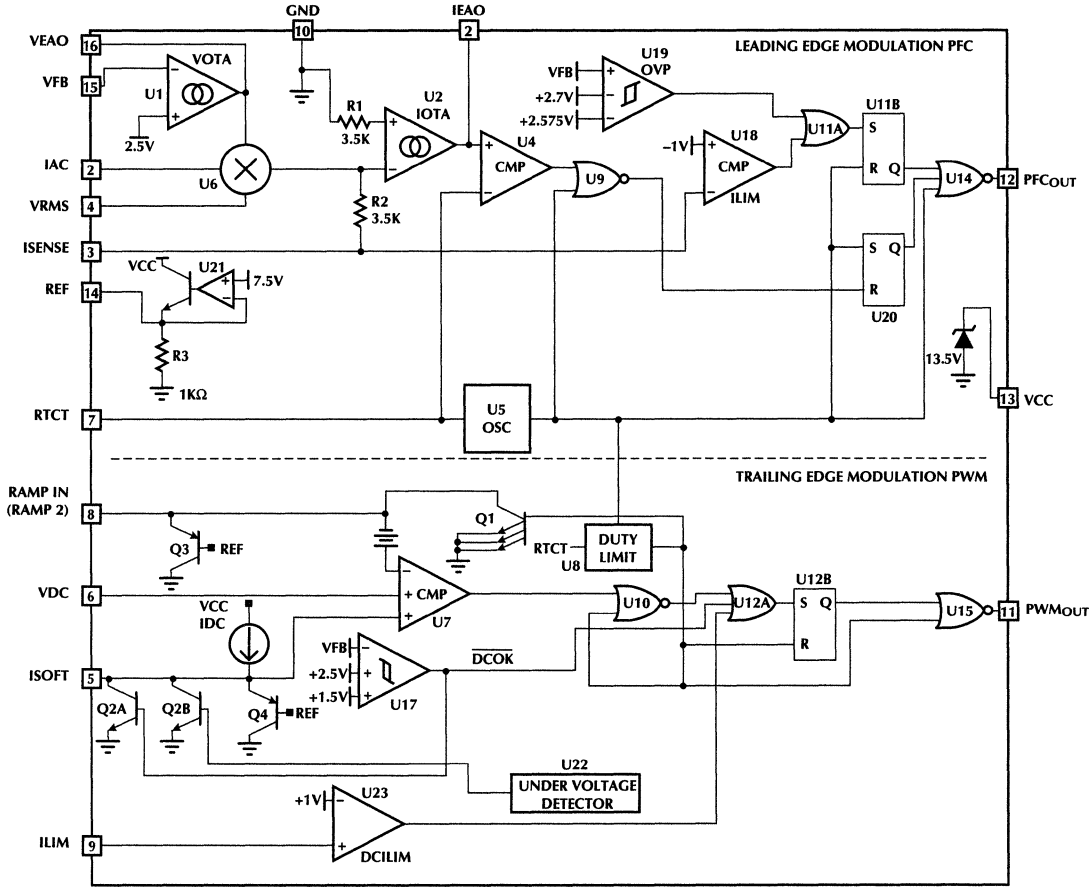


Figure 8. ML4824 Block Diagram.

PULSE WIDTH MODULATOR SECTION FOR DC TO DC CONVERTER

The pulse width modulator section is configured as a controller for a two-switch forward converter. The switch current is sensed via the voltage drop across resistor R_{18}. Resistor R_{19} and capacitor C_{17} function as a noise filter. The two switches toggle ON and OFF together at the same time. Reset of the primary side of the transformer T_2 is facilitated by diodes D_5 and D_6, which should be high voltage, high speed rectifiers.

OSCILLATOR

The oscillator frequency is determined by the values for R_T and C_T. The ON time of the oscillator is given by the following expressions:

$$T_{ON} = R_T C_T \ln \frac{V_{REF} - 1.25}{V_{REF} - 3.75} \quad (4)$$

$$\cong R_T C_T \times 0.51 \text{ for } V_{REF} = 7.5 \text{ volts}$$

$$T_{OFF} = 490 C_T \quad (5)$$

Typically, for the example circuit, which is operating at 80kHz, R_T is 52.3kΩ, and C_T is 470pF.

$$\text{Period, } T = T_{ON} + T_{OFF} + 2T_D \quad (6)$$

where T_D represents the propagation delay (approximately 20 nsec) of the circuit.

CONTROL RAMP

The peak-to-peak amplitude of the control ramp is set by the two voltages derived from the 7.5V bandgap reference. Two comparators are used. The upper threshold is 3.75V, the lower 1.25V. The potential difference between the two inputs to these two comparators is 2.5 volts, which is the peak-to-peak amplitude of the ramp.

This ramp is used in the power factor correction section. There is also a second ramp which can be derived from sensing the switch current, or for voltage mode control, can be derived from the output (feed-forward signal) of the power factor corrector.

THE MULTIPLIER

The gain of the multiplier is automatically controlled by the voltage feedback amplifier output voltage (VEAO) and the r.m.s. voltage (VRMS) from the rectifier input bridge. A third input to the multiplier is the 120Hz A.C. line input current (IAC), which supplies an in phase sinusoidal reference.

To reduce noise, current is sampled instead of voltage. A resistor at the IAC node connected to the line will generate an input current to the multiplier.

The multiplier output (IMULO) is also a 120Hz sine wave. The quality of this waveform is dependent entirely on the quality of the line voltage. If the line voltage is noisy, the output of the multiplier will also be noisy. This is the reason why the bandwidth of VRMS and VEAO have to be low.

D.C. O.K. COMPARATOR

The output voltage of the power factor correction section is monitored by the internal D.C. O.K. comparator. If the output of this section is too low, the pulse width modulator section will not be permitted to turn ON. Once the output level reaches 380 volts DC, the pulse width modulator section will commence soft-starting.

The power factor correction section can also be configured to have soft start by two possible arrangements. (1) the output of the current error amplifier is high impedance, and if the compensation network is tied to the reference voltage (pin 14), then the power factor stage will soft start. (2) If the first arrangement is not slow enough for safe starting, then extra components can be added to pin 16 to assist soft start. See the applications section in the data sheet.

VOLTAGE LOOP COMPENSATION AND WIDE BANDWIDTH TRANSCONDUCTANCE AMPLIFIER

The voltage loop compensation has been speeded up with a high gain wideband uncompensated transconductance stage. A unique transconductance curve is shown in Figure 11 which is different from the conventional operational amplifier. The transconductance amplifiers on ML4824 exhibits low transconductance when the two inputs of the amplifier are balanced; and transconductance will increase when the two input voltages are unbalanced. Because of such enhancement while the system is slewing, the system bandwidth and the slew rate also increases.

The transconductance amplifier itself does not require local feedback compensation. Loop compensation is also much easier to manage.

To design a compensation network, it is required to find the power stage voltage transfer function. However, precise PFC stage model is not available at high frequencies.

The conventional approach is to obtain a first order approximation. Below 30Hz or at half of the line frequency, the current mode model described in (2) is valid since the PFC stage never reaches the steady state above 30Hz.

The PFC stage is a resistor emulated at the line frequency. At the line frequency, the instantaneous input power, which is A.C., is not equal to the instantaneous output power, which is D.C. The instantaneous input power at the peak of the voltage waveform delivers more power than the average power required. Therefore the excessive power must be stored temporarily in the high voltage reservoir capacitor. At frequencies above the line frequency the instantaneous system power has not reached the steady state. Therefore the D.C. operating point for A.C. analysis cannot be determined. Because for any power stage the input voltage is also the system A.C. analysis D.C. operating point. Below one half of the line frequency, the system operating point can be averaged based on the average input power.

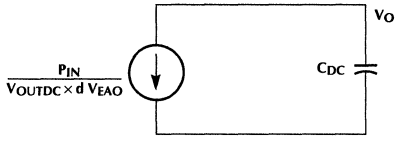


Figure 9. High Frequency Power Stage Model for Voltage Loop.

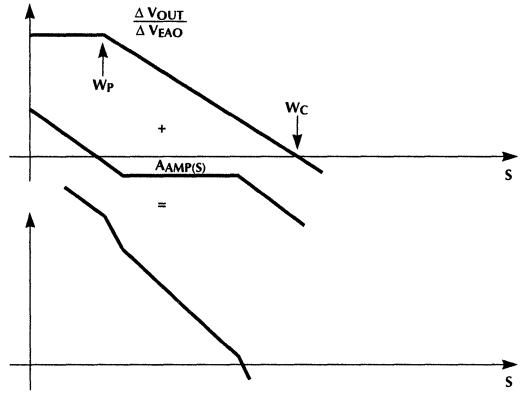


Figure 10. Overall Voltage Loop Response.

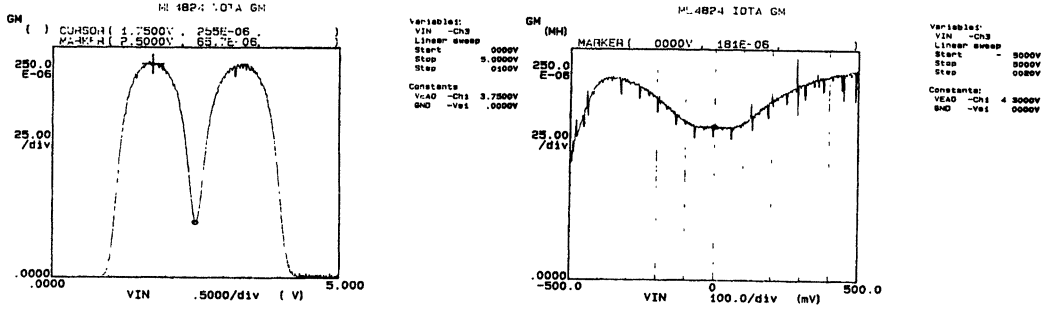


Figure 11. Voltage Loop OTA, U1, and Current Loop OTA, U2, Transconductance, GM.

For the voltage loop response above the line frequency, the first order model is simply a current source feeding the high voltage capacitor. (See Figure 9)

$$\frac{\Delta V_{OUT}}{\Delta V_{EAO}} = \frac{\text{AVERAGE } P_{IN}}{V_{OUT\,DC} \times \Delta V_{EAO} \times S \times C_{DC}}$$

$$= \frac{\text{AVERAGE } P_{IN}}{V_{OUT\,DC} \times 5.3V \times S \times C_{DC}} \quad (7)$$

Here the swing of the voltage loop error amplifier is 5.3V. This transfer function indicates the zero crossing frequency, W_C which is

$$\frac{\text{Average } P_{IN}}{V_{OUT\,DC} \times 5.3 \times S \times C_{DC}} \quad (8)$$

At frequencies below one half of the line frequency, the conventional current mode model can be applied. The model depicts a pole location. When the duty cycle is 1, the pole is

$$\frac{2}{R_L \times C_{DC}} \quad (9)$$

Now the compensation network can be designed. If lead lag compensation is applied, the loop cross-over frequency can be set around 30Hz assuming 60Hz line frequency. See Figure 10.

CURRENT LOOP COMPENSATION WITH WIDE BANDWIDTH TRANSCONDUCTANCE AMPLIFIER

The current loop error amplifier is a high performance wideband uncompensated transconductance amplifier. The designer can adjust his own bandwidth based on the system requirement. See Figure 11.

A procedure similar to the voltage loop can be used to obtain the transfer function for the power stage of the current loop. At high frequencies, the power stage behaves as a voltage source driving an inductor. See Figure 12.

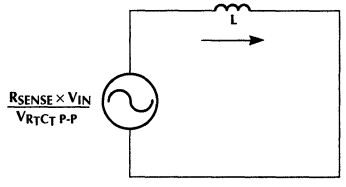


Figure 12. High Frequency Power Stage Model for Current Loop.

$$\omega_C = \frac{R_{SENSE} \times V_{IN}}{V_{R_TC_T\,P-P} \times L} = \frac{R_{SENSE} \times V_{IN}}{2.5V \times L} \quad (10)$$

$$\omega_P = \frac{2}{R_L \times C_{DC}} \quad (11)$$

CURRENT MULTIPLIER AND MAXIMUM AVERAGE POWER LIMIT

The function of the current multiplier is similar to the method used in ML4821 to generate a reference sine wave current in phase with the line voltage. The maximum input power is also set by the multiplier.

The Gain K is curve fitted to $1/V_{RMS}$ squared for universal input. (See Figure 13) Below 1.2V, K starts brown out and will not fit the $1/V_{RMS}$ square curve. This feature can be used to set the minimum A.C. input voltage, usually 80VAC. The I_{MULO} maximum current is limited at 200µA internally. R_{MUL} is an on-chip resistor of 3.5K. Because the high gain and the high bandwidth current loop transconductance amplifier will always keep the I_{MULO} x R_{MUL} (3.5K) = R_{SENSE} x I_{IN}. Since I_{MULO} is equal to K x (V_{EAO} – 1.5) x I_{AC}, and I_{AC} is derived from the rectified sinusoidal line voltage, I_{MULO} as sine wave reference is generated in phase with sinusoidal line voltage.

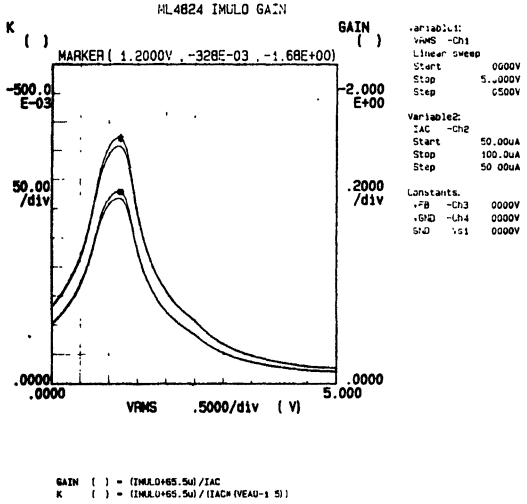


Figure 13. Multiplier Gain K.

TIMING DIAGRAM AND HOW TO IMPLEMENT DOUBLE FREQUENCY PWM FOR ML4824-2

There are two versions available to the user. In the ML4824-1, the PFC switching frequency is equal to the PWM switching frequency. These two sections synchronize at the rising edge of the system clock. In the ML4824-2, the PWM switching frequency is equal to twice the PFC switching frequency.

To implement $f_{PWM} = 2\ f_{PFC}$, the R_TC_T ramp has been used as a reference ramp and 4 timing areas has been generated. See Figure 14.

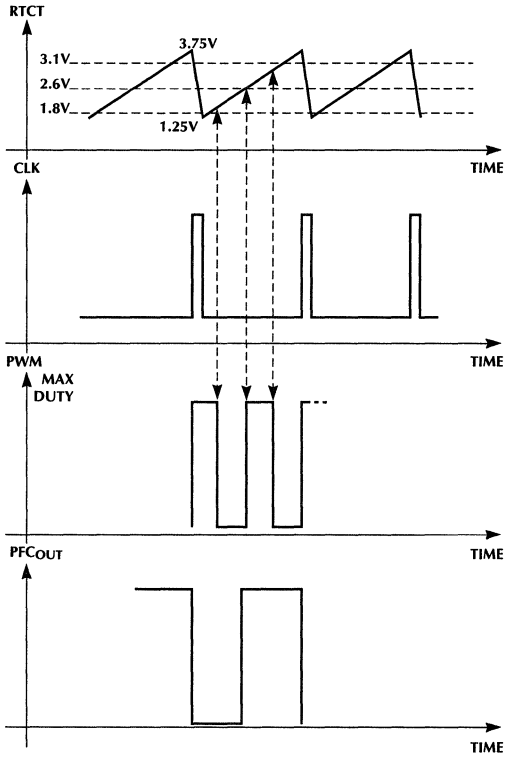


Figure 14. BL4824-2 Timing Diagram.

D.C. O.K. COMPARATOR, UNDER VOLTAGE, AND SOFT START

The D.C. O.K. comparator, U7 monitors the PFC output to disable or enable the D.C. to D.C. PWM section. It also discharges the I_{SOFT}, pin 5. When the PFC output reaches the design value, the PWM section will monotonically ramp up the D.C. output voltage. This feature will reduce the cost of the house keeping circuitry which generates a 13.0V, V_{CC}.

The I_{SOFT} pin 5 will be pulled down during Under Voltage lock-out which will ensure smooth transition to protect the components.

The PFC section also has the soft start feature due to the presence of the two transconductance amplifiers. Additional external soft start can be added in, i.e., additional delay time can be configured to permit more gradual increase to the final output power, which is requested by the PFC output through the Voltage Transconductance Amplifier.

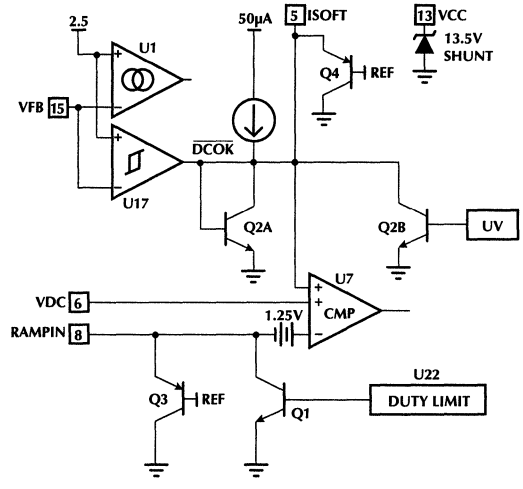


Figure 15. D.C. O.K. Comparator, PWM Comparator, and Soft Start.

VOLTAGE MODE WITH FEED-FORWARD RAMP

In the PWM section, a voltage mode control system can be configured instead of current mode control, if desired. A feed-forward ramp can be realized by connecting a resistor between PFC high voltage D.C. output and RAMPIN pin 8, and connecting a capacitor between RAMPIN pin 8 and GND.

CONCLUSION

An integrated solution which simplifies the off-line PFC power supply design has been shown. Leading edge modulation for synchronous switching is the main feature of this controller. Noise immunity of the ML4824 is excellent because of the use of leading edge modulation for the power factor correction stage and trailing edge modulation for the D.C. to D.C. second stage. At the DC. to DC. stage, the discharge NPN transistor Q1 RAMPIN pin 8 reduces the switching noise right after the switch is on, so it does not require a leading edge blanking. Other features include current-mode control, 14-pin package, soft start, wait state, on-chip shunt regulator, wide bandwidth error amplifier and many other fault detection functions. Finally, to achieve optimal off-line PFC/PWM cascade power converter design, we conclude:

1. The synchronous switching method should be utilized;
2. The duty ratio of the second stage should be close to 0.5.

For more information on a typical application, please see Application Note 33, "ML4824 Combo Controller Applications."

REFERENCE

1. Micro Linear ML4819 Data Sheet, Micro Linear Corporation, San Jose, California, 1993
2. R.D. Middlebrook, "Topics in Multiple-Loop Regulators and Current-Mode Programming" IEEE Power Electronics Specialists Conference, 1985 Record, pp. 716-732.
3. J. Dronik, "Is Cascade Connection of Power Converters Inefficient?" Proc. PCIM Power Conversion Conference pp. 34–43, 1993
4. Micro Linear ML4821 Data Sheet, Micro Linear Corporation, San Jose, California, 1993
5. ML4824 Data Sheet
6. Application Note 33

by John DeFiore

Using the ML4411 BLDC Motor Controller

INTRODUCTION

The purpose of this document is to explain the theory and application of Micro Linear's ML4411 brushless DC motor controller IC. It shows typical applications, along with information about choosing the various components necessary for proper operation. It presents in depth control system information for those who wish to use it, but the user can pick component values without extensive analysis by using the formulas developed for each component.

GENERAL DESCRIPTION

The ML4411 provides sensorless commutation for brushless DC motors. An integrating back EMF sensor, combined with an on-chip VCO and sequencer, form a phase locked commutation loop. Motor current control schemes allow linear or constant off time pseudo PWM modes. The ML4411 provides on chip braking and power failure detection. In 12V applications, the ML4411 can drive external P and N channel FET's directly. Interface circuitry will allow driving of higher voltage motors.

THEORY OF OPERATION

During startup, the motor is initially at rest and has no back EMF to lock the commutator loop. In order to get sufficient back EMF to close the loop, it is necessary to start the motor "open loop", until the motor attains a speed of about 100 RPM. To accomplish this, the VCO ramps linearly, accelerating the motor to speed. Once at minimum speed the loop is closed and the motor accelerates to operating speed under closed loop commutation. The non-energized phase provides the feedback necessary to properly commutate the motor. The phase voltage is integrated over a 60 degree interval. (Figure 1 shows an idealized phase waveform with the motor back EMF superimposed as the dotted line.)

If the commutation is perfect, no net voltage change will occur on the output filter. If the commutation is early or late, the output filter will pump up or down to bring the next commutation closer to the ideal position. (For a detailed servo analysis of the commutation loop see the section on picking critical component values.) Finally an external speed loop around the ML4411 provides speed control for those applications that require it.

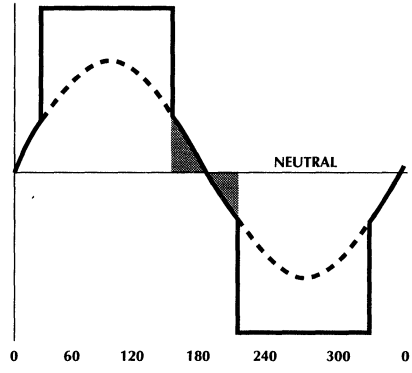


Figure 1. Motor Phase Waveform with Back-EMF Superimposed (Ideal Commutation)

HOW TO OPERATE THE ML4411

Figure 2 shows a typical application for the ML4411. The ML4411 is a flexible building block for motor driver systems. Because of the variations in the types of applications and motors, the first step in using the ML4411 is to choose the major system components. Some of the system level choices are:

Output Driver Selection and Interfacing

Output driver selection depends mainly on the motor voltage and current. For 12V motors, the chip can drive external N and P channel FET's directly. For motors up to 80V, the approach shown in Figure 6 can be used to drive the P channel FET's. For very high currents or voltages above 80V, the best scheme is to use N channel FET's in the high side, and use a high side drive interface, such as those available from IXYS, International Rectifier, and others. (See Figure 7). IGBT's could be used in place of FET's in this case. Note that during the alignment phase, the high side drivers are turned on first, and held on for the required settling time. This means that the typical charge pump scheme for driving the high side FET's will not work. A floating supply can be developed to provide power to the high side drivers.

Startup Implementation, (Analog vs. µP Control)

Startup schemes are critical with sensorless motor drivers. The reason a startup scheme is necessary is that the back EMF of the motor is used to determine the position of the rotor. If the motor is not rotating, or is rotating slowly, there is little or no back EMF to sense. The ML4411 uses an open loop approach to start the motor turning, then closes a PLL to lock the commutation phase to the phase of the rotor. The ML4411 has the capability to use analog startup circuitry. (See Figure 3). A microprocessor can give more flexibility and can also close a speed loop around the motor. The trade-offs are cost and circuit complexity vs. flexibility and ease of making changes. The following sequence starts the motor:

1. The IC is held in reset, (Pins 16 and 18 low). This applies full current to the windings by turning two of the upper and one of the lower drivers on. This will cause the rotor to move to a point which is 30 electrical degrees before the first commutation step. The IC must be held in this state until the rotor has settled. (See the section on choosing the reset capacitor for more information).
2. The reset pin (Pin 16) is driven high, which begins the ramp state. The resistor or current source on pin 21 sets a current which charges the filter on pin 20. This causes the VCO frequency to increase, commutating the motor in an open loop manner. This rate should not exceed the rate at which the rotor can turn, or the commutation loop will not lock.
3. When the motor has reached about 100 RPM the commutation loop can be closed by pulling the ENABLE E/A pin (Pin 18) high.
4. The user may with to poll the VCO/TACH out pin (Pin 15) to be sure the motor has actually started. To do this, shut off the output stage momentarily by pulling pin 8 low. Then wait for two edges on pin 15. The time between these edges can be measured and the part re-enabled after operation is assured.

CURRENT CONTROL (LINEAR OR PWM)

For low to moderate current applications, or applications where minimizing electrical noise is important, the ML4411 provides a linear current control mode. The low side drivers are controlled linearly based on the difference between the current command (I_{CMD} Pin 20) and the sensed current (I_{SENSE} Pin 12). This difference is amplified by transconductance amplifier A2 which has a gain of 1.875×10^{-4} Mho. A capacitor from the output of A2 to ground, C_{OTA}, compensates the loop with a dominant pole.

For higher current applications, or where power dissipation is important, the constant off time pseudo PWM loop provides another option. In this mode, a comparator compares the voltage on the I_{LIMIT} pin with the sense current. An internal one shot fires when the sensed current appearing as a voltage on pin 12 (times the gain of 5 provided by A1) exceeds the voltage on I_{LIMIT}. C_{OS} determines the one shot's off time. By choosing the off time appropriately, (See the section on choosing C_{OS}) the average current will be equal to the current on the I_{LIMIT} pin.

In this application, the transconductance amplifier A2 is not used, and its input must be tied to +5V in order to avoid interaction with the PWM.

Speed Control

Speed control is external to the ML4411. There are many ways to implement speed control. Some of the possibilities include:

Microprocessor control — A microprocessor measures the VCO frequency, which will be proportional to rotor speed when the commutation loop is locked. The processor then puts out either an analog signal to control the current, (through a D/A), or a PWM signal, which could be used to drive pin 6 (C_{OTA}). If pin 6 is used as a PWM input, the PWM signal must be amplified to swing from ground to the supply rail. Also, no capacitor should be connected to pin 6.

Analog control — The voltage on the RC pin, pin 20 will be proportional to motor speed. This can be compared to a reference, and used to drive the current loop. A PWM circuit could also be built with a ramp generator and a comparator. The output of the PWM could drive pin 6 as outlined above. See figures 6 and 7 for an example of analog speed control with PWM.

CRITICAL COMPONENT SELECTION

In order to properly select the critical components for the ML4411 you should know the following things:

1. The motor operating voltage.
2. The maximum operating current for the motor.
3. The number of poles the motor has.
4. The back EMF constant of the motor.
5. The torque constant of the motor.
6. The desired speed of operation.
7. The moment of inertia of the motor and its load.
8. The coefficient of viscous friction.

If you do not know one or more of the above values, it is still possible to pick components for the ML4411, but some experimentation may be necessary to determine the optimal value.

Caution!!!

Systems built with the ML4411 may contain voltage potentials capable of causing serious injury and components which, when failed, may shatter or explode. Please use extreme caution when operating these parts. The use of protective eye wear is strongly recommended!!! To safely observe in-circuit waveforms an isolation transformer should be inserted between the AC line and the circuit under test. Caution is required when testing the part with motors. Loose fitting clothing can catch in the rotor or motor load causing injury. Ties are especially dangerous. Do not attempt to hold or stop the rotor with your hand, as this can cause injury as well. Use a dynamometer for load testing.

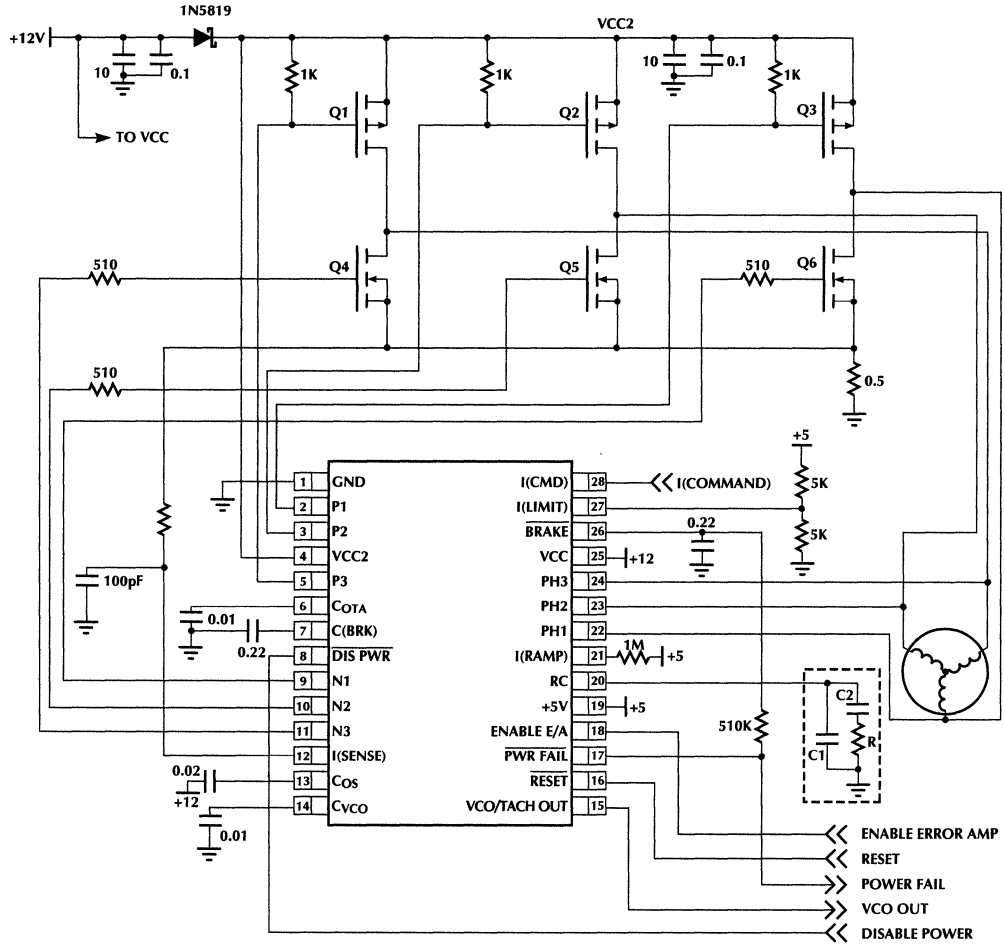


Figure 2. ML4411 Typical Application

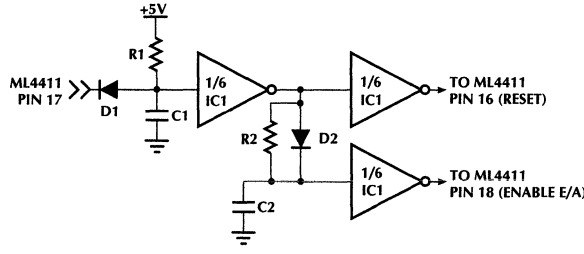


Figure 3. Analog Start-Up Circuit.

Operation of the ML4411 requires choosing the following components. The previous information is necessary to choose some of them.

1. R_{SENSE}, the motor current sense resistor.
2. The I_{SENSE} filter network.
3. The voltage divider for I_{LIMIT}.
4. C_{OS}, the one shot timing capacitor.
5. C_{VCO}, the VCO timing capacitor.
6. The reset capacitor for analog startup.
7. The ramp resistor.
8. The enable capacitor for analog startup.
9. The VCO filter components, C1, C2 and R.
10. C_{BRK}, the energy storage capacitor for braking.
11. C_{OTA}, the linear current loop compensation capacitor.

The purposes of these components are explained in the following sections, and the following motor will be used as an example for choosing components:

Voltage	12V
Number of poles	12
Ko	0.269
Kt	25×10^{-5} N x m/A
Desired RPM	5400
Viscous damping factor	0.4
Moment of Inertia	72×10^{-6} Kg x m^2
Maximum current	2A

R_{SENSE}

The function of R_{SENSE} is to provide a voltage proportional to the motor current, for current limit/feedback purposes. For maximum dynamic range without exceeding the input's linear range, the voltage at the I_{SENSE} input should not exceed 0.5V in normal operation. In order to pick a value for R_{SENSE}, it is necessary to know the maximum current delivered to the motor. This is a function of how much starting torque is required, the acceptable temperature rise in the windings, the rotational losses and the maximum permissible magnetic field. If the motor is sized correctly, the maximum current will be the current necessary to start the motor against its maximum load. This is given by the starting torque divided by the torque constant. A gain stage with a gain of 5 follows the sense resistor, and the I_{LIMIT} input has a range of 0-5V, so choosing R_{SENSE} to give an I_{LIMIT} voltage of 2.5V gives:

$$R_{SENSE} = \frac{0.5}{I_{MAX}}$$

I_{MAX} is the maximum motor current.

The power dissipation is obviously R_{SENSE} squared times I_{MAX}, so the resistor should be sized appropriately. For the example motor, R_{SENSE} should be 0.25Ω. The power dissipated is 1W, so choose a 2W resistor.

I_{SENSE} FILTER

The I_{SENSE} filter consists of an RC lowpass filter in series with the current sense signal. The purpose of this filter is to filter out noise spikes on the current, which may cause false triggering of the one shot circuit. It is important that this filter not slow down the current feedback loop, or destruction of the output stage may result. The recommended values for this circuit are R = 1KΩ and C = 100pF. This gives a time constant of 100ns, and will filter out spikes of shorter duration. These values should suffice for most applications. If excessive noise is present on the I_{SENSE} pin, the capacitor may be increased at the expense of speed of current loop response. The filter time constant should not exceed 500ns or it will have a significant impact on the response speed of the one shot current limit circuit.

I_{LIMIT} DIVIDER

If the I_{LIMIT} pin is not used as a current command for the constant off time PWM mode, it should be used as a current limit to limit the maximum current in the motor windings. The I_{LIMIT} pin is a **voltage** input, which sets the maximum current in the motor, before the current limit one shot fires and shuts off the lower devices in the power stage. One way to set this voltage is by using a voltage divider to the 5V rail. If the suggested method for picking R_{SENSE} is used, the divider should be set for 3V, in order to give a 20% headroom for component and motor variations. If a different value of R_{SENSE} was chosen, the I_{LIMIT} voltage should be:

$$I_{LIMIT} = 1.2 \times I_{MAX} \times R_{SENSE} \times 5$$

I_{LIMIT} is the voltage at pin 27.

The factor of 1.2 is to give some headroom for motor, load, supply and component variation. If this is not enough for your application, ILIMIT can be increased subject to the maximum ratings of the motor and the output stage. For the example motor, $1.2 \times 2 \times 0.25 \times 5$ gives an I_{LIMIT} voltage of 3 volts, as expected. Choosing 3K to ground and 2K to +5V gives a voltage divider string with 3V output and a total resistance of 5K. (Keeping the total divider resistance between 4K and 20K will minimize power dissipation while still providing sufficiently low output impedance.)

C_{OS}

The one shot capacitor determines the off time after the current limit is activated, i.e. the voltage on the I_{SENSE} pin (pin 12) exceeded the voltage on the I_{LIMIT} pin (pin 27). This value should allow the winding current to decay during the off time by an amount equal to the increase in the current in the minimum ontime. The minimum ontime for the one shot is approximately 1μs. In a system with low on resistance parts and high Q motor windings (The Q is the ratio of the winding's reactive impedance to the resistance.) it is necessary to have an off time given by the following equation:

$$T_{OFF} = 1.11 \times 10^{-6} \times V_{MOTOR}$$

V_{MOTOR} is the voltage applied to the motor windings.

The capacitance for a given off time may be read from the graph on P.5-113 of the datasheet, or for values larger than 30µs, the following formula may be used:

$$T_{OFF} = 947.4 \times C_{OS} + 5$$

T_{OFF} in microseconds, C_{OS} in microfarads.

Solving for C_{OS}:

$$C_{OS} = \frac{1.11\times10^{-6} \times V_{MOTOR} - 5\times10^{-6}}{947.4}$$

Now C_{OS} is in Farads.

This is the maximum value that C_{OS} should be. Higher average torque during the current limit cycle can be achieved by reducing this value experimentally, while monitoring the motor current carefully, to be sure that a runaway condition does not occur. This runaway condition occurs when the current gained during the on time exceeds the current lost during the off time, causing the motor current to increase until damage occurs. For most motors this will not occur, as it is usually a self limiting phenomenon. For the example motor, C_{OS} comes out to 8.8nF, so a 10nF capacitor would be a safe choice.

C_{VCO}

It is important to pick the VCO capacitor so that the nominal operating speed corresponds to about 6V at the RC pin (pin 20). In variable speed applications the voltage on pin 20 should also not exceed the minimum value of the VCC supply minus 3V, (or 9V for a fixed 12V supply). The VCO frequency is given by:

$$F_{MAX} = 0.05 \times N \times RPM$$

N is the number of poles.

The VCO gain is:

$$K_{VCO\,MIN} = \frac{2.42\times10^{-6}}{C_{VCO}}$$

So making a linear approximation, VCO frequency is given by:

$$F = K_{VCO} \times V_{RC}$$

Solving for V_{RC} which is the voltage at pin 20, we get:

$$V_{RC} = \frac{0.05\times N\times RPM\times C_{VCO}}{2.42\times10^{-6}}$$

Finally, setting V_{RC} equal to 6V, solving for C_{VCO} and simplifying, gives:

$$C_{VCO} \frac{2.904\times10^{-4}}{N\times RPM}$$

Now in a variable speed application, the previous equation can be used to ensure that the voltage at pin 20 does not exceed the minimum value of the VCC supply minus 3V, when the motor RPM is at the maximum. If it does, then pick C_{VCO} so that the nominal operating speed is reached at a correspondingly lower voltage into the VCO. For the example motor, C_{VCO} would be 4.48nF, so 4.7nF would be a good choice.

RESET CAPACITOR

The reset capacitor is C1 in the analog start up circuitry shown in Figure 3. If a microprocessor is used to control startup, the processor must leave the ML4411 in reset for a time equal to the settling time computed below. The function of the reset capacitor is to provide a time delay, during which the ML4411 will lock the rotor to a known position. During this time period the ML4411 turns on two of the upper and one of the lower output drivers. This results in a fixed current in the windings, a stationary magnetic field, and a locked rotor. If the position is not at a torque null during the reset period, it will require some time to move to the locked position, and settle. This time period is dependent on the motor, the load, the friction and eddy current losses, and current limit setting. Solving the differential equation for the motor/load system can give an approximate starting value.

Assuming that the magnetic field causes a restoring torque proportional to the angular displacement, the rotor torque is:

$$\tau = -k \times \theta$$

k is the restoring torque slope in N × M/radian, and θ is the displacement angle in radians.

Note that this is very similar to the settling of a damped spring mass system, and similar dynamics apply. The angular equivalent of F = M × A gives:

$$J\times\frac{d^2}{dt^2}\theta = -k\times\theta$$

J is the moment of inertia of the motor's rotor, plus load.

Adding a viscous friction and eddy current loss component:

$$J\times\frac{d^2}{dt^2}\theta + r\times\frac{d}{dt}\theta + k\times\theta = 0$$

r is the loss factor, which includes eddy current and viscous friction losses.

Solving the previous equation gives a resonant frequency of:

$$f = \frac{\sqrt{\frac{k}{J}}}{2\times\pi}$$

f is in Hz.

An N pole motor will have a worst case angle of π/N radians. A good approximation for settling time of a unit step to 5% is:

$$t_S = \frac{3}{\frac{r}{2 \times k} \times \sqrt{\frac{k}{J}}}$$

The r/2K factor is known as the damping factor, and can range from 0.1 in a motor with very little damping to 0.9 in a heavily damped motor. In an N pole motor, the torque nulls occur every $2 \times \pi/N$. In one half that angle, the motor goes from zero to full torque. Full torque is given by the motor torque constant, times the maximum current set by the I_{LIMIT} feature. Therefore, the restoring torque constant k is equal to:

$$k = \frac{N \times k_T \times I_{MAX}}{\pi}$$

I_{MAX} is the maximum current set by the I_{LIMIT} feature, in Amps. Kt is the motor torque constant in N × M, and N is the number of motor poles.

The reset capacitor must charge to the logic threshold trip voltage during the settling time. The charging equation is:

$$V = V_f \exp\left(-\frac{t_S}{tau}\right)$$

V is the trip voltage, ts is the settling time, tau is the RC time constant, and V_f is the charging supply.

Solving for the time constant:

$$tau = \frac{-t_S}{\ln\left(\frac{V}{V_f}\right)}$$

Solving for C:

$$C = \frac{-t_S}{\ln\left(\frac{V}{V_f}\right) \times R}$$

Where R is the charging resistor for the capacitor, or R1 in Figure 3. Assuming a logic level trip voltage of 1.4 volts, and a charging resistor of 1 Meg supplied by 5V and adding a 20% margin for things like variation in the logic threshold and supply voltage:

$$C = \frac{1.2 \times t_S}{1.273 \times 10^6}$$

For the example motor, the damping factor, r/2k is given as 0.4. Therefore, ts is approximately 1.5. Choosing a conservative standard value, the reset capacitor should then be 1.5µF.

Start with the value of C calculated as shown. If the motor has not settled before the ramp up phase, then it will be necessary to increase the value of C until the motor is motionless when the ramp starts. If fast starting is essential, and the above value seems too large, a decrease in C will allow for faster starting. Note that part to part and supply tolerances require some safety margin in the selection of C. If the motor constants and load inertia are not known, or if enough nonlinear elements are present in the load, (e.g. friction), an empirical method may be used to determine C. Start with a 1µF capacitor charged by a 1 Meg resistor. If the motor appears to have settled well before ramp up, half the capacitance value. If the motor has not settled by ramp up, double the value. When a change from not settled to settled, or vice verse is observed, home in on the optimum value by successively reducing the change in capacitance by 1/2, then increasing or decreasing the value as appropriate. This "binary search" method will allow quick convergence to the proper value.

ENABLE CAPACITOR

In the analog startup scheme, this capacitor provides a time delay after the reset period for the motor to ramp up to speed. This is C2 in Figure 3. The following equation gives an approximate starting value for this capacitor. If starting is not reliable, this capacitor may be increased until it is.

$$C = \frac{10.47 \times J}{\ln\left(\frac{V}{V_f}\right) \times R \times I_{MAX} \times K_t}$$

Where J is the total inertia, V is the logic trip voltage, Vf is the charging supply, Kt is the torque constant and R is the charging resistor. C is C2 in Figure 3, and R is the charging resistor for C2, or R2 in Figure 3.

Assuming a charging resistor of 1 Meg, and a logic trip level of 1.4V, for the example motor, C2 is approximately 1.2µF.

VCO FILTER (RC PIN)

The VCO filter consists of a capacitor to ground, in parallel with a series resistor and capacitor to ground. (See Figure 5). The pin that drives this network is a transconductance stage, so that the voltage out to current in transfer function of this block is simply the impedance of the block. The purpose of this network is to filter the VCO frequency out of the position/commutation loop, and to provide phase compensation for the loop so that it is stable. The impedance of the network is:

$$\frac{R \times C2 \times s + 1}{s \times (C2 + R \times C1 \times s \times C2 + C1)}$$

In order to properly determine the values for this filter, it is necessary to do a servo analysis on the entire commutation loop. If the reader does not have an extensive background in servo systems, the formulas at the end of this section along with Table 1 can be successfully used to pick values for these components. It is necessary to know the back-EMF constant, Ke, of the motor to pick these values correctly. Since the commutation loop must

have acceptable phase margin both at startup and at the maximum operating frequency, the compensation's phase lead should be located at the geometric mean between these two frequencies. For those who need detailed analysis the following information is given: The commutation loop is a phase locked loop, which locks to the rotor's position. Note that this inner loop does not attempt to modify the position of the rotor, but modifies the commutation times to match whatever position the rotor has. The speed loop changes the rotor velocity, and the commutation loop locks to the rotor's position to commutate the phases at the correct times. A servo analysis should start with a block diagram of the system dynamics (See Figure 4): The phase detector consists of the motor, the back EMF sampler/integrator, and the gm amplifier. The loop filter's transfer function follows the phase detector, and the VCO's gain is in the section on choosing C_{VCO}. Note that as in any PLL, the VCO is an integrator in that it accepts a voltage and outputs a frequency. Phase is defined as the integral of frequency, so this necessitates an s in the denominator of the VCO transfer function. Writing the expression for the open loop gain of the entire loop:

$$A_{OL} = Ke \times \frac{Kv}{2 \times \pi} \times \omega \times Atten \times gm \times \frac{R \times C2 \times s + 1}{s^2(C2 + R \times C1 \times s \times C2 + C1)}$$

Where Aol is the open loop gain, Ke is the back EMF constant of the motor in volts/radian/sec., Kv is the VCO gain in radian/sec/volt (NOT Hz/volt). ω is the rotor speed in radians/second (NOT RPM). Atten is the resistive divider ratio used to divide down the back EMF from high voltage motors, (Nominally 0.5 if no external resistors.), and gm is the transconductance of the phase detector amplifier. (See the section on back EMF attenuation resistors for more details on Atten.)

Simplifying the above equation by making the following substitutions:

$$Ko = Ke \times \frac{Kv}{2 \times \pi} \times \omega \times Atten \times gm$$

$$\omega z = \frac{1}{R \times C2}$$

$$\omega p = \frac{C2 + C1}{R(C1 \times C2)}$$

Yields:

$$A_{OL} = Ko \times \frac{s + \omega z}{s^2 \times C1(s + \omega p)}$$

Note that the s^2 in the denominator gives rise to two poles at the origin, and 180 degrees of phase shift. In order for this system to be stable, the zero formed by the numerator must give a positive phase shift when the magnitude crosses unity. This leads to the conclusion that the pole must occur after the magnitude crosses the unity gain frequency. The pole's frequency must be low enough to filter the VCO frequency out of the loop, and high enough to allow the zero to boost the phase margin of the loop are acceptable over all operating conditions. Writing the pole frequency as a multiple of the zero frequency gives:

$$\omega p = M \times \omega z$$

Then the maximum phase lead occurs at the geometric mean:

$$\omega_{MAXLEAD} = \sqrt{M \times \omega z}$$

In PLL design it is common to approximate a third order loop by a second order model. This is valid because the filter pole occurs well after the open loop response has reached unity gain. If we approximate the system as a second order PLL, a damping factor of 0.7 will give very little overshoot and good transient response to disturbances. For a second order system, the settling time to d% is given by:

$$t_S = \frac{-\ln\left(\frac{d}{100}\right)}{\zeta \times \omega n}$$

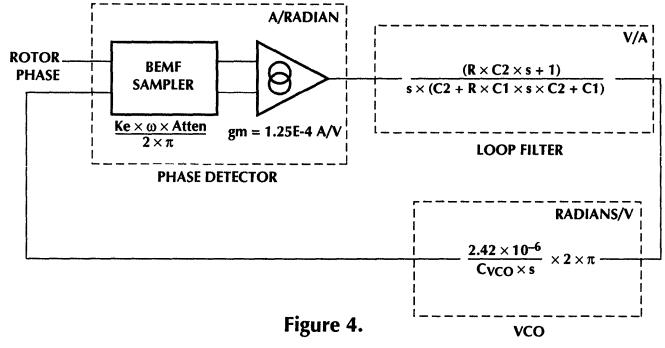


Figure 4.

Where ζ is the damping factor, and ωn is the natural frequency. If the PLL must settle within Ns cycles, then the time to settle is:

$$T_{ACQ} = \frac{Ns}{F_{VCO}}$$

Ns should be as small a number as possible while still allowing the loop filter to filter out the frequency components of the VCO. Asking for a settling time of one or two cycles would mean that the filter must respond on the order of the VCO frequency, and would not allow adequate filtering. Too long a settling time could cause improper commutation and loss of lock for abrupt changes in rotor position. A good choice for Ns would be 20 cycles. Using the second order relation:

$$\omega o = 2 \times \zeta \times \omega n$$

where ωo is the bandwidth and ωn is the natural or resonant frequency, and combining the above yields:

$$\omega o = -2 \times \ln\left(\frac{1}{100} d\right) \times \frac{F_{VCO}}{Ns}$$

This will be the required closed loop bandwidth of the commutation loop.

Now the maximum phase lead should occur when the open loop gain crosses unity, which will yield the maximum phase margin. Since the open loop gain varies with rotor speed, the best place to put the maximum phase lead is the geometric mean between the maximum rotor speed and the startup speed at the end of the ramp period. If the commutation loop closes after the ramp period at a speed of 100 RPM, then:

$$F_{VCO} = 0.05 \times N \times \sqrt{100 \times MAXRPM}$$

Where N is the number of poles, and MAXRPM is the maximum operation speed of the motor. Using the equation for $\omega_{MAXLEAD}$ and the above:

$$\sqrt{M} \times \omega z = -2 \times \ln\left(\frac{1}{100} d\right) \times \frac{F_{VCO}}{Ns}$$

Or:

$$\omega z = -2 \times \ln\left(\frac{1}{100} d\right) \times \frac{F_{VCO}}{(Ns \times \sqrt{M})}$$

Now returning to the original open loop gain equation, and noting that at the ωo frequency, the magnitude must equal 1, we get:

$$Ko \times \frac{\left| 1j \times 2 \times E \times \frac{F_{VCO}}{Ns} + 2 \times E \times \frac{F_{VCO}}{Ns\sqrt{M}} \right|}{\left(\left| 1j \times 2 \times E \times \frac{F_{VCO}}{Ns} \right| \right)^2 \times C1 \times \left| 1j \times 2 \times E \times \frac{F_{VCO}}{Ns} + 2 \times E \times \sqrt{M} \times \frac{F_{VCO}}{Ns} \right|} = 1$$

Where E = -ln(d/100). Solving for C1 yields:

$$C1 = \frac{1}{4} \times \frac{Ko}{\sqrt{M}} \times \frac{Ns^2}{\left(\ln\left(\frac{d}{100}\right)^2 \times F_{VCO}{}^2 \right)}$$

Then C2 is just:

$$C2 = C1 \times (M - 1)$$

And substituting back into the equation for ωz:

$$2 \times E \times \frac{F_{VCO}}{(Ns \times \sqrt{M})} = \frac{1}{\frac{1}{4} \times \frac{Ko}{\sqrt{M}} \times \frac{Ns^2}{(E^2 \times F_{VCO}{}^2)} \times (M-1) \times R}$$

Solving for R and simplifying:

$$R = 2 \times M \times \ln\left(\frac{d}{100}\right) \times \frac{F_{VCO}}{Ns \times Ko(1 - M)}$$

Requiring the PLL to settle to d = 3% in 20 cycles with a spread of 10 between the pole and zero gives the following equations.

$$C1 = \frac{4.07 \times 10^{-11} \times Ke \times RPM}{C_{VCO} \times F_{VCO}{}^2}$$

$$C2 = 9 \times C1$$

$$R = \frac{9.02}{C2 \times F_{VCO}}$$

where Ke is the back-E.M.F. constant in volts/radian/second., and RPM is the mean rotor speed in RPM.

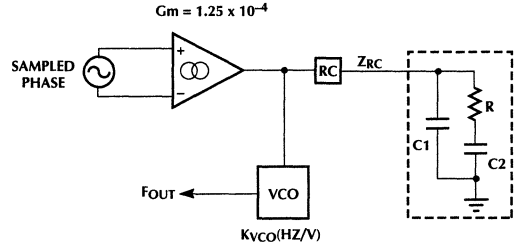


Figure 5. Back EMF Phase Lock Loop Components

TABLE 1.

CONSTANT	DESCRIPTION	FORMULA	RECOMMENDED VALUE
F_{VCO}	VCO frequency for mean motor speed (see text).	$F_{VCO} = 0.05 \times N \times RPM$	Depends on motor and application
M	Spread between pole and zero in loop filter.	$\omega p = M \times \omega z$	10-20
d	PLL will settle to d percent in Ns PLL cycles	$ts = \frac{-\ln\left(\frac{d}{100}\right)}{\zeta \times \omega n}$	3
Ns	The number of PLL cycles necessary to settle to d percent after a step of phase	$tacq = \frac{Ns}{F_{VCO}}$	20
Ko	The motor back EMF constant, in V/rad/S times the VCO gain, in Hz/V (note the unit change and the absence of the $2 \times \pi$ in the denominator), times the angular speed of the rotor, in rad/s times the back EMF attenuation constant, times the gm of the phase detector's transconductance amplifier.	$Ko = Ke \times Kv \times \omega \times Atten \times gm$ Ke is supplied by the motor manufacturer The VCO gain is $K_{VCO\,MIN} = \frac{2.42 \times 10^{-6}}{C_{VCO}}$ The angular speed of the rotor is the expressed in r/s. The back EMF attenuation (Atten) is the divider hooked between the motor and the PH1-3 back EMF sense inputs, (Nominally 0.5), and gm is 1.25E-4	Depends on motor and application

Table 1 summarizes the constants used in the equations for R, C1 and C2.

The phase margin is given by the following expression:

$$\Phi m = a\tan\left(\sqrt{M}\right) - a\tan\left(\frac{1}{\sqrt{M}}\right)$$

This is dependent only on the spread between the pole and the zero, because the uncompensated phase is 180 degrees due to the two poles at the origin. With M = 10, the maximum phase margin will be 55 degrees. These values should provide good performance in most applications.

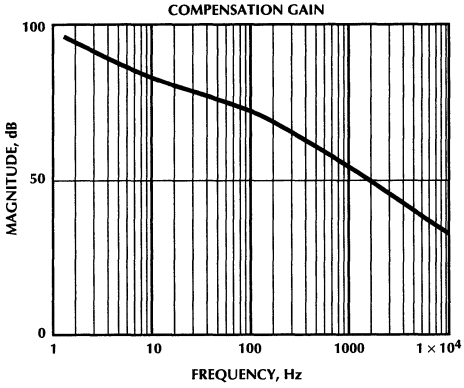
As an example, consider a motor with 12 poles, Ko = 0.269, a decade of separation between the pole and zero, 20 PLL cycles to settle to 3% of final value, and (min and max) RPM = 5400. First, the number of poles and the RPM require that F_{VCO} = 3240Hz. The value for ω in the formula for Ko should be based on the geometric mean between starting speed and operating speed. Plugging these values in for C1, C2 and R, we get:

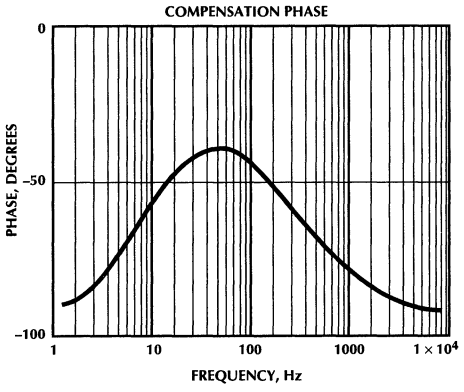
$$C1 = 0.228\mu F$$

$$C2 = 2.055\mu F$$

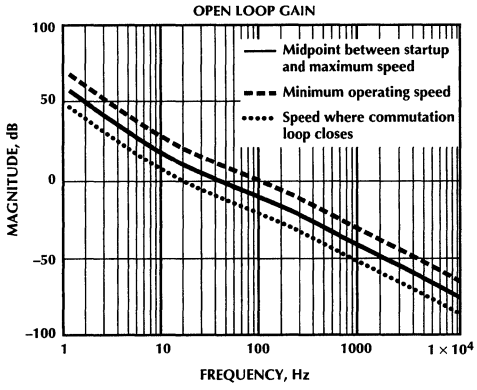
$$R = 4.691K\Omega$$

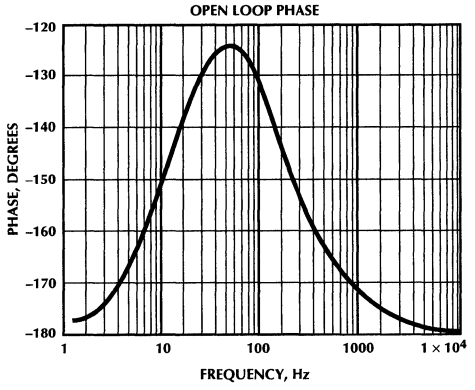
Plotting the Bode response of the filter alone:





This clearly shows the phase boost due to the compensation, and the rolloff to filter the VCO frequency. Now the overall loop bandwidth is calculated from the preceding equations to be 181Hz. The overall open loop gain and phase are shown in the following graphs:





As expected, the open loop gain at the center frequency crosses 0dB when the phase peaks, giving bandwidth of approximately 180Hz and a phase margin of 55 degrees. The phase margin at startup and at nominal speed are also better than 40 degrees. For variable speed applications, the phase margin will remain within these limits, provided the nominal speed is chosen to be the maximum speed, and the speed is controlled downward from there. Using this approach, the rotor speed can vary more than an order of magnitude and still maintain acceptable phase margin.

RAMP RESISTOR

This resistor, connected between pin 21 and VCC, programs the initial acceleration rate of the VCO during ramp. This current is programmed by a resistor between the +5V supply and pin 21. Pin 21 is approximately 0.7V above ground, so that the current is given by:

$$I_{RAMP} = \frac{5V - 0.7V}{R_{RAMP}}$$

This current is mirrored to pin 20, where it charges the loop filter, and causes the VCO frequency to ramp linearly. The voltage ramp on pin 20 is approximately:

$$V_{RC} = \frac{I_{RAMP}}{C1+C2} \times t$$

The angular rotor speed for a given voltage on pin 20 is:

$$\omega = \frac{2.42 \times 10^{-6} \times V_{RC}}{6 \times \pi \times C_{VCO} \times N}$$

V_{RC} is the voltage at pin 20 and N is the number of poles.

The angular rotor acceleration must not exceed the maximum acceleration that the motor and current limit can give:

$$\frac{2.42 \times 10^{-6} \times I_{RAMP}}{6 \times \pi \times C_{VCO} \times N(C1+C2)} < \frac{I_{MAX} \times Kt}{J}$$

IMAX is the current limit setting,
J is the moment of inertia of the rotor + load
Kt is the torque constant and N is the number of poles.

This leads to a minimum value for R_{RAMP}:

$$R_{RAMP} > \frac{4.3 \times 2.42 \times 10^{-6} \times J}{I_{MAX} \times Kt \times 6 \times \pi \times C_{VCO} \times N(C1VCO + C2VCO)}$$

The C1VCO and C2VCO are the capacitors in the loop filter connected to pin 20, not the reset or enable capacitors. If the minimum value does not allow reliable starting of your motor, try increasing the value by 20% at a time, until starting is reliable. If the moment of inertia and torque constants are not known, try using a 1 Meg resistor for R_{RAMP}, and increasing it as above if starting is not reliable. For the example motor, R_{RAMP} should be 600K.

C_{BRK}

C_{BRK} is a capacitor between pin 7 and ground. The function of this capacitor is to store energy so that when power fails, the ML4411 can still turn on the lower N channel devices for braking. 0.22µF will store enough energy in most cases. If you have a very large inertia, and require braking with power off, increasing this capacitance may be necessary.

C_{OTA}

If a linear current control loop is used for controlling the motor current, a capacitor from pin 6 to ground, C_{OTA}, provides compensation for this loop. The current loop's time constant must be well above the speed control loop, so that it does not contribute any phase lag. The closed loop gain for this loop is:

$$\frac{I_{MOTOR}}{I_{CMD}} = \frac{\frac{gm}{C_{OTA}}}{s + \frac{5 \times Rs \times gm}{C_{OTA}}}$$

gm is the transconductance of A2, and
Rs is the motor current sense resistor.

This puts a pole at:

$$fp = \frac{5 \times Rs \times gm}{2 \times \pi \times C_{OTA}}$$

Where fp is in Hz.

The value for gm is 1.874×10^{-4}, so using the example motor, with Rs = 0.25Ω and choosing 0.01µF for C_{OTA} gives a pole frequency of 3.73KHz, which is well above the frequency of any mechanical time constant. 0.01µF should be an acceptable value for most applications.

BACK EMF ATTENUATION RESISTORS

If you use the ML4411 with a motor supply which is higher than 12V, you must divide down the back EMF signals from the motor so as not to exceed 12V on the phase sensing inputs, PH1, PH2 and PH3. The ML4411 has internal 8K resistors to ground, so an external resistance in series with each phase and the respective phase sense input forms a voltage divider. (See Figure 7) This divider is the Atten constant in the previous formulas for picking the loop filter. For example for a 100V motor, the series resistors should give 12V at the ML4411 for the absolute maximum input voltage. Choosing 110V as the maximum voltage to allow some safety margin gives a divider ratio of 12/110 or 0.109. A series resistor of 80.6K gives a safe ratio of 0.09.

OUTPUT DRIVE

The ML4411 can drive external N and P channel FET's directly, if 12V operation is used. For voltages between 24V and 80V, an external cascode transistor can be used to level shift the drive voltages. For higher voltages, or large currents, external drivers, coupled with all N-channel FET's are the best solution. (IGBT's could be used as well.) The external FET's used with the ML4411 should be rated to handle the full current limit current plus appropriate derating. They should stand off at least 1.5 –2 times the motor supply voltage. Thermal considerations and heatsinking are important and should be given consideration in the preliminary design phase. In some applications, when a velocity loop is closed around a motor, and there is a large inertia attached to the motor, during deceleration the energy stored in the inertia can cause the motor to generate a current. This current will pump up the power supply capacitors to a potentially dangerous voltage, causing capacitor and output stage failure. If this is a problem, the solution is to add a circuit which senses when the supply voltage increases by a given amount and switches a resistive load into place to dissipate the energy. This problem does not occur when braking, but the N-channel FET's must handle most of the energy in the rotating mass if braking is necessary.

DRIVING MOTORS UP TO 80V

The schematic of Figure 6 shows how to drive motors up to 80V using a cascode approach. The external bipolar transistors stand off the higher voltage, and level shift the high side drive. The reason that this approach is restricted to 80V is the availability of high voltage P-channel FET's is limited, and the cost is high. It may be possible to use this approach with higher voltage motors if higher voltage P-channel FET's can be obtained. Speed/current control for higher power motors is best done via pulse width modulation. The speed control in the ML4411 can be pulse width modulated by not installing a capacitor on the C_{OTA} pin, pin 6, and driving this pin with the output of a pulse width modulator. (This PWM signal must swing 0-12V.) This is shown in figure 6. The speed from the RC pin, pin 20, is compared to a set speed. If the speed is faster or slower than required, the error signal will cause the pulse width modulator to decrease or increase the duty cycle accordingly, regulating the speed.

DRIVING HIGH VOLTAGE MOTORS

An example of one way to drive a high voltage motor is shown in Figure 7. The IR2130 provides the interface and drive capability for the larger FET's. The floating supply powers the 3 high side drive circuits. In the application notes for many of the FET drivers they show a "flying capacitor" approach to developing drive for the high side N-channel devices. This circuit connects a diode from the +12V rail to a capacitor, which has the other end hooked to the motor phase output. The "flying capacitor" charge pump scheme will not work with the ML4411, since during the reset period, the high side drives turn on first, and remain on for the reset duration. This does not allow the "flying capacitor" to charge. Speed control is accomplished as in the 80V example, with a PWM signal driving the C_{OTA} pin.

LAYOUT CONSIDERATIONS

Good layout practices are vital to getting the ML4411 to work reliably. In particular, the supplies must be well decoupled close to the chip with 0.1µF ceramic capacitors in parallel with 1µF electrolytic or tantalum capacitors. The supply to the output drivers must also be well decoupled close to the drivers with at least a 0.1µF in parallel with a good quality low ESR 10µF electrolytic. High current motors may require more capacitance. Controlling the current paths is important as well. If a groundplane is used, separate conductors (traces) should return the motor currents to the sense resistor which can connect to the ground plane near the supply ground. The same approach should be used for the supply voltage. The purpose of this technique is to keep the high current high speed signals out of the ground plane, to reduce system noise. If the supply voltage input is not near the power decoupling caps for the drivers, additional supply decoupling should be used where the supply enters the board. Watch capacitive coupling from high dv/dt signals into traces or planes on other layers. Use multiple vias to connect high current traces from the top of the board to the bottom. Standard layout practice applies to the rest of the circuit. Keep traces as short as possible, minimize high current loop length, etc.

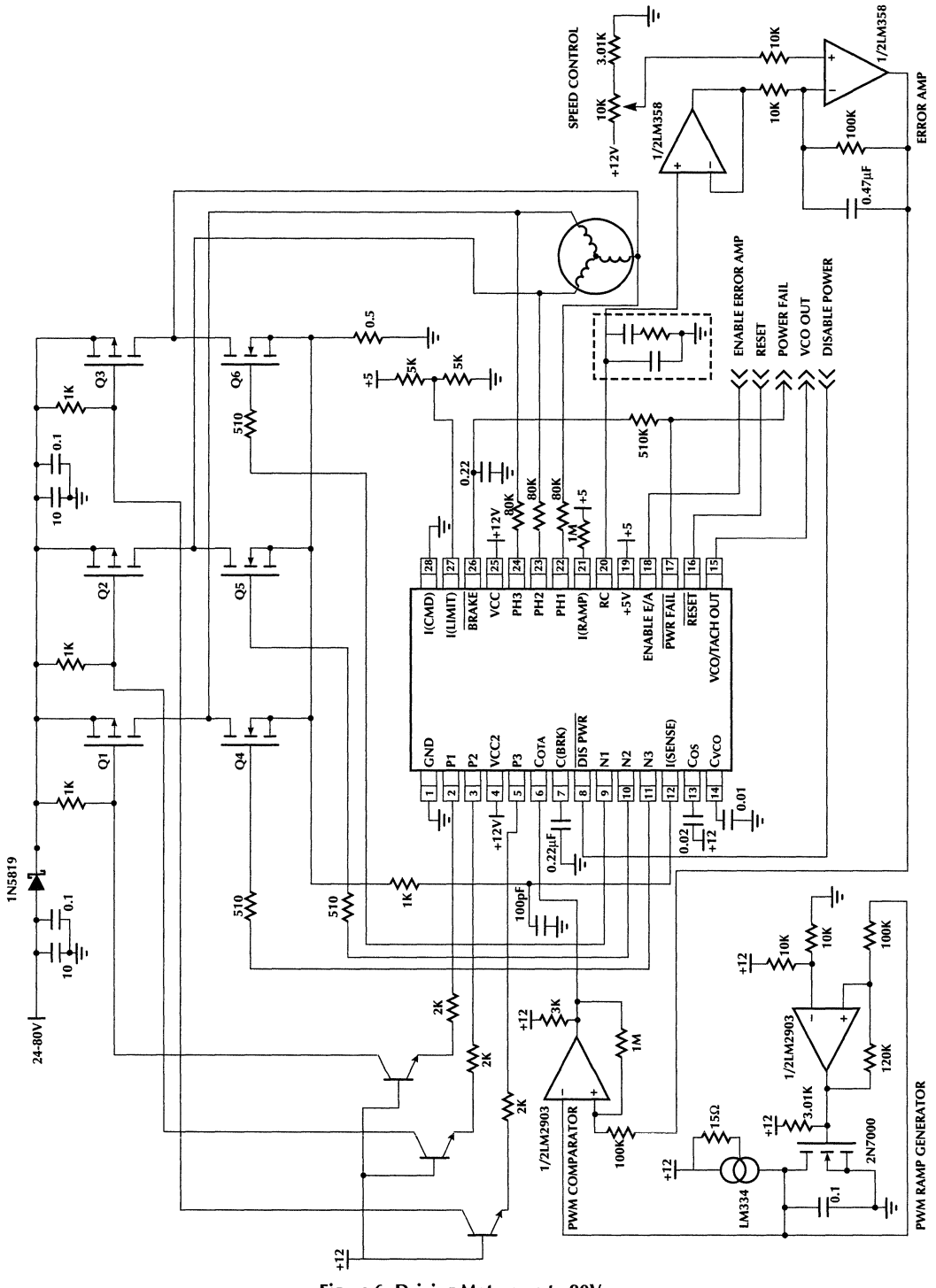


Figure 6. Driving Motors up to 80V

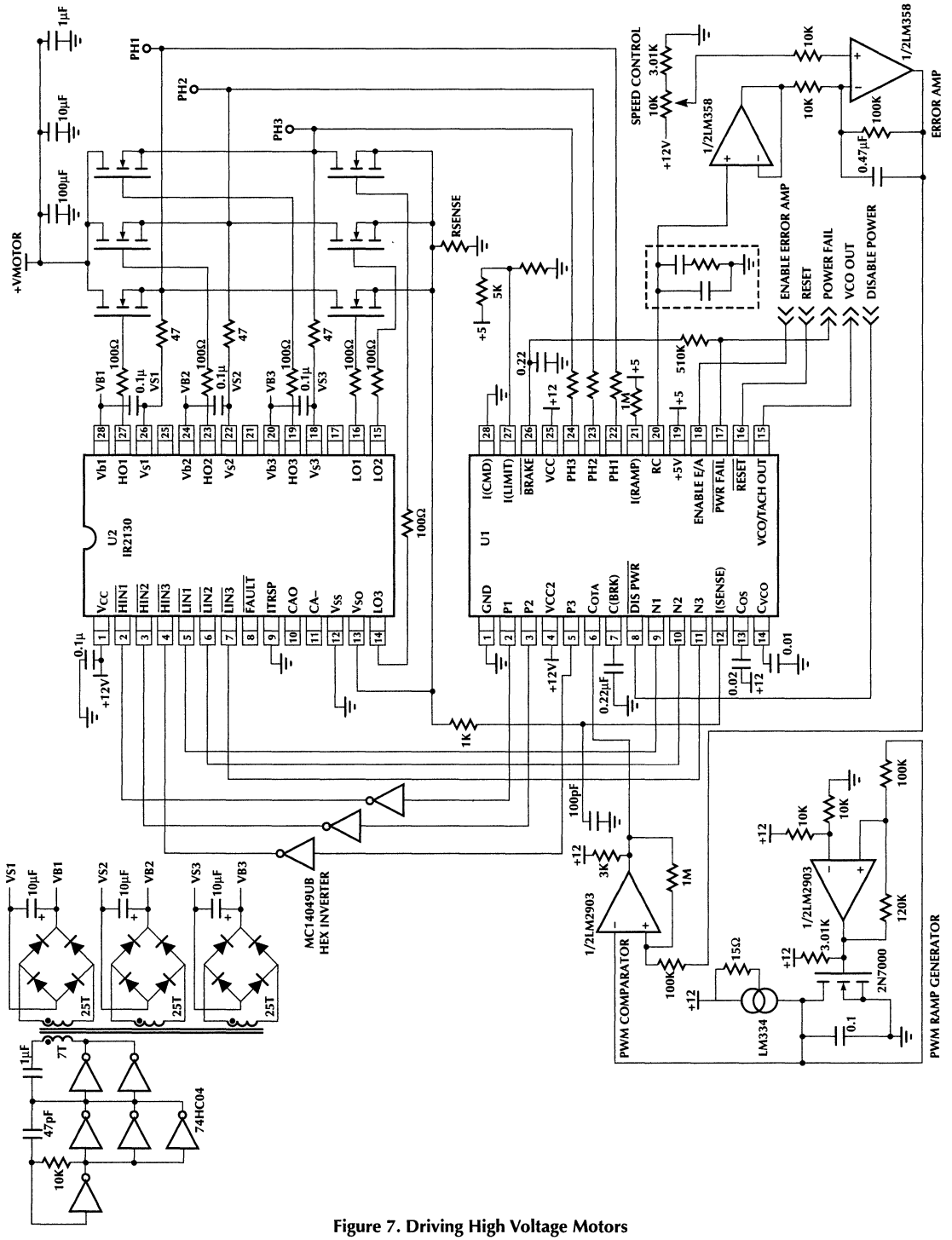


Figure 7. Driving High Voltage Motors

A Design Guide for the ML4873

Brenda Kovacevic,
and Willie Cho

INTRODUCTION

The growing popularity of battery powered equipment such as handheld instruments and laptop computers has led to a need for more efficient and compact power management systems.

Power circuits now must not only have great efficiency, but they must serve multiple functions by generating multiple voltages/currents and fit in increasingly smaller areas while doing so! Efficiency must be maintained over the entire range of operating conditions, and the circuitry itself must consume minimum power such that maximum operating time/battery life is realized. As the primary market for portable equipment is consumer, all the above must be achieved at minimal cost.

The ML4873, a highly integrated IC controller designed with these challenges in mind, provides a "user-friendly" solution for such applications. Two complete SMPS control systems for the generation of multiple supply voltages (typically 3.3V and 5V) are provided, as well as a 12V LDO regulator that can be used for programming EEPROMs or flash memories. All three voltages specified in the PCMCIA Type II document are provided. A 5V micropower linear regulator that can easily be converted to 3.3V with the addition of one zener diode is also provided for the monitoring logic.

Two innovative techniques are used to ensure the high efficiencies required; synchronous rectification to replace the voltage drops associated with Schottky diodes by the lower drops across power MOSFETS, and a "burst" mode for light load conditions. A sleep mode in which just microamps of supply current are consumed, can also be selected.

Cost and size can be reduced by using the recommended integrated magnetics approach for gate drive. The ML4873 was designed to use as few external components as possible, and is available in space saving 28 pin SOIC or SSOP packages.

BASIC OPERATION

MAIN PWM STAGES

Battery powered systems typically have higher battery voltages available than the 5V and 3.3V system requirements, so the featured topology is that of a buck (or step-down) regulator.

The two PWM stages each drive two N-channel power MOSFETs in a synchronous rectification scheme designed to improve overall efficiency and reduce cost. In a typical buck regulator, Schottky diodes with a forward voltage drop of roughly 0.45V would be used as rectifiers. When you use these in an 10–20V system, the resulting losses are not significant. At 5V and especially at 3.3V, the losses associated with these diodes can be responsible for more than 5-10% of the total system losses! This is clearly unacceptable in battery powered systems.

Synchronous rectification makes use of recent advances in power MOSFET technology; on resistances in the milliohm range are now commonplace! Many, such as the Siliconix "Little Foot" series, are also available in surface mount versions. This makes using power MOSFETs a compact as well as more efficient choice for rectification.

N-channel MOSFETS were chosen over their P-channel counterparts for a variety of reasons, not the least of which was the fact that a P channel FET must be larger than twice the size of an N-channel FET to obtain the same RDS_{ON}. As Si area determines cost, this means that they are also more expensive devices. The downside of using N-channel FETs is that we must provide additional enhancement to the gate above the positive rail of the device. This usually means using a charge pump, which can offset the cost savings of using an N-channel FET in the first place. In an SMPS system, we have magnetics "for free." All we have to do is add another winding, a cheap capacitor and an even cheaper diode and the job is done!

"Break-before-make" logic is included in each stage to ensure that one FET is off before the other is turned on, so that no "shoot-through" can occur. Cycle by cycle current limiting with a corresponding soft start are added safety features. Undervoltage lockout, active at 4.0V and below, prevents any spurious signals from turning the part on when it should be off.

In an effort to reduce the necessary operating currents of the ML4873, the two PWM stages share a common oscillator, reference and internal biasing.

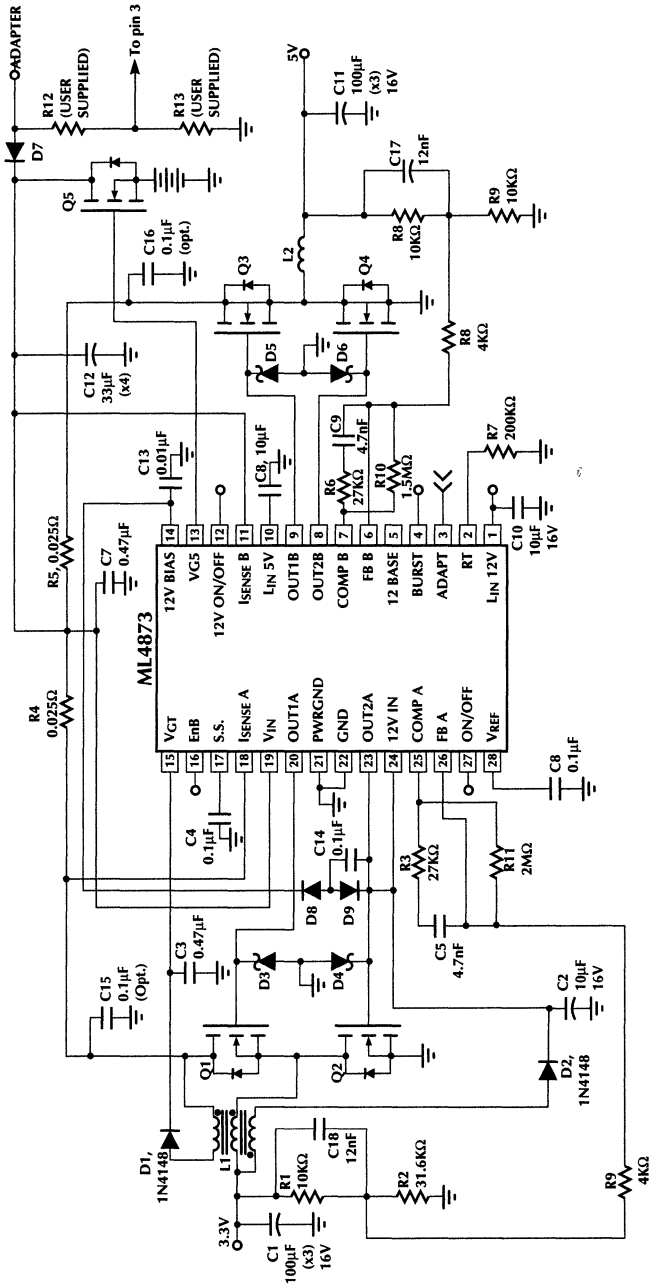


Figure 1. Design Example

12V Linear Regulator

The 12V linear regulator can source up to 60mA. If more current capability is required, an external NPN pass transistor can be used. (Figure 2) Applying a bias of approximately 1.5V above the input turns this garden variety linear regulator into a low drop out regulator. Drop out voltages of roughly 200mV can be expected.

5V Micropower Linear Regulator

The main function of this regulator is to provide power for power management or power managed peripheral devices that may be used.

This regulator remains operative during sleep mode, but does shut down during undervoltage lockout conditions, which occur at around 4V. 25mA max current is supplied by this regulator.

AC Adaptor Detection Circuitry

The ML4873 has also provided a method for detecting the presence of the AC adapter, and disconnecting the converter when it is charging. A low R_{DS}(on) N-channel power MOSFET is used as the switch; this eliminates the loss that would be associated with a diode when the system is running from a battery, and neatly disconnects the battery when the sensing comparator trips so that the battery sustains no drain while it is being charged.

Burst Mode for Light Loads

At light loads (when output current is less than 100mA), efficiency is lower due to a phenomenon peculiar to synchronous rectifier schemes known as "current shuttling" between the input and output. In a synchronous rectifier, the inductor current is allowed to go negative, which creates a condition at light loads in which the average inductor currents are larger than the output currents. This condition leads to large conduction losses across the inductor, and lowered efficiencies. In order to alleviate this, we have supplied the ML4873 with a light load "burst mode". Regulator A of each PWM stage has a pin available which puts the system into "burst" mode. When the burst comparator (pin voltage) is below its lower threshold, the regulator turns on, and turns off again when the burst pin voltage hits the higher threshold (Figure 3). The lower threshold is V_{REF} – 25mV, and the higher threshold is V_{REF} + 25mV. The output capacitors then remain charged as they are being turned on at low repetition rates. The efficiency is also maintained by putting the IC into the sleep mode in between repetitions. Repetition rate will be a function of output capacitance and load current.

DESIGN EXAMPLE AND GUIDELINES (FIGURE 1)

CHOOSING OPERATING FREQUENCY

Prior to designing an inductor, a compensation network, or evaluating losses and how to minimize them, one must choose an operating frequency. There are several trade-offs to be aware of; using a higher operating frequency will decrease the size of the required filter inductor and output capacitors, hence cost, but will induce higher switching losses associated with the power FETs. Often, the size of the heat sinks required to operate faster more than offsets the space savings of the magnetics!

Although the ML4873 was designed with 100kHz operation in mind, the frequency can be varied by the size resistor placed between the R_T pin and ground (Figure 4). This establishes the charge current for the internal capacitor. It should be noted that the discharge current is constant; hence dead time stays constant and max duty cycle will decrease with increases in frequency.

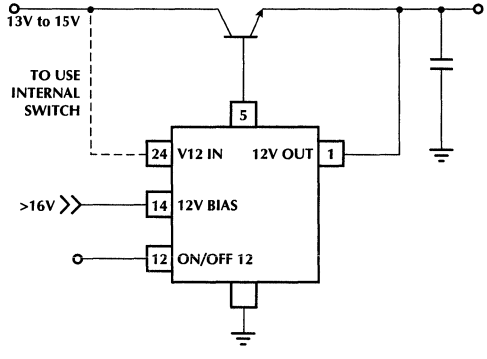


Figure 2. Higher Current 12V Linear Regulator

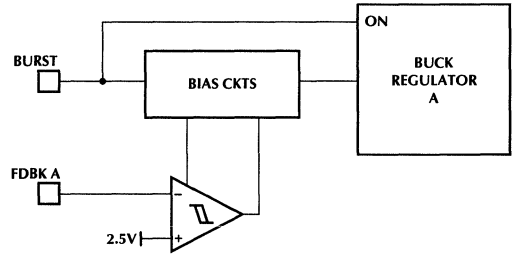


Figure 3. Burst Mode Comparator and Logic

Choosing Appropriate Power MOSFETS

A key element in determining the overall system cost, size and efficiency are the power FETs used as PWM switching elements. A low $R_{DS}(on)$ is desirable for optimizing efficiency, however, a low on resistance can often indicate a high gate capacitance. As I = CdV/dt, this means that more initial current is required to switch the FET on quickly. If the FET is switched on too slowly, it spends more time in the linear region of its characteristic curve with associated higher $R_{DS}(on)$ and losses. It is therefore important in this application to look at both $R_{DS}(on)$ and CISS to choose the best FET.

Another parameter to consider when choosing the output power FETs is the average drain current expected. It is a good idea to choose a MOSFET with a higher (say 1.2X) $I_{D(max)}$ than the maximum expected average drain current. One must also consider the thermal characteristics of the device; many FET manufacturers list an $I_{D(max)}$ that would be impractical to achieve due to the heat sink size required!

However, this spec is not as useful in determining the correct FET for the job as the SOA, or safe operating area spec. The ID spec was written for applications in which the FET would be operating continuously, not switched as it is SMPS systems. We are more concerned here with what instantaneous limits we must not exceed. The SOA is an area defined by V_{DS} and I_D which defines a boundary which, if crossed over for more than 1µs during either turn-on or turnoff, will result in damage to the FET (Figure 5). Switching transients due to leakage inductance should be estimated to check for a violation of this curve after the magnetics design is complete.

As a cross check for this, a pulsed or peak I_D spec is usually included. The definition of this (duration, or repetition rate of I pulses) varies from manufacturer to manufacturer, so it is a good idea to verify the conditions first.

Logic level MOSFETs that achieve full enhancement at "logic levels" (5V rather than 10V) can be used to improve efficiencies at light loads if this is desirable. There will also be a cost trade-off; logic level FETs are relatively new and more expensive due to higher processing costs.

A common trick for reducing the $R_{DS}(on)$, (once again, at the expense of the input capacitance), is to parallel two or more FETs. If this is done, it is a good idea to use two FETs only (more invites current hogging) that are available in a dual package to prevent any thermal differences. A dual package also ensures that the C_{ISS}'s are more evenly matched, ensuring matching rise and fall times.

Recommended FETs for this application include the Siliconix "Little Foot" series (second sourced by National Semiconductor), International Rectifiers's Logic Level FET series (prefix IRL), and Motorola's MTD family. Specific part numbers are summarized in Table 1.

A small Schottky diode is required at the gate drive pins of all four MOSFET driver outputs (pin 8, 9, 20 and 23) to clamp the negative going voltages. Parasitic capacitance from the drain to gate of the lower MOSFET causes its gate to go negative when the upper MOSFET is turned off and current is flowing through the body diode. The upper MOSFET's gate is pulled negative through the gate to source capacitance when its source potential changes from V_{IN} to ground, which results from the current path established through its body diode and the fully on lower MOSFET.

Choosing (or Designing) An Inductor

The most critical component to the performance of the overall circuit is the inductor. The first decision to be made is whether to design one or simply buy one off the shelf. Usually time constraints dictate the latter, however, higher efficiencies and greater optimization of key parameters can be achieved by taking the time to "tweak" the magnetics to fit the application.

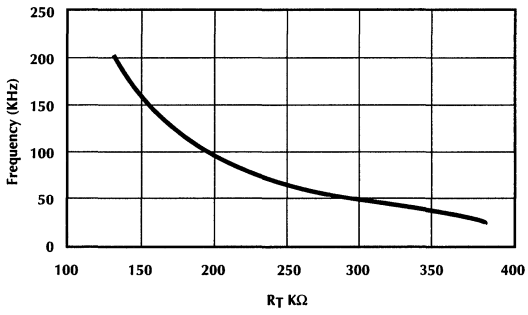


Figure 4. Oscillator Frequency vs. R_T

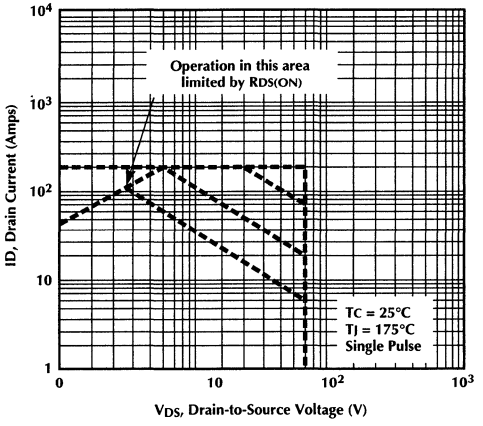


Figure 5. Maximum Safe Operating Area for the IRFZ445

Most suppliers of standard inductors will also perform a custom design for a slight extra charge.

"Off the shelf " inductors are usually specified by three main parameters only, inductance, maximum DC current, and maximum DC resistance. Inductance in a buck regulator topology is defined as:

$$L = \frac{(V_{IN} - V_O)V_O}{V_{IN}\, f\, \Delta I}$$

ΔI = maximum ripple I V_O = output voltage

f = switching frequency V_{IN} = input voltage

Maximum AC current, I_{PK}, can be estimated by either using the maximum output current and adding 1/2 the expected ripple current to it, or by simply guardbanding and multiplying the maximum output current by 1.5.

In order to distribute the losses evenly among all conduction elements, the DC resistance should be selected to be 1/4 of the sum of the RDS_{ONS} of the two switching MOSFETs.

To check for continuous mode operation (discontinuous mode operation occurs when the inductor empties itself of all stored flux during each off cycle, and results in lower efficiency and reduced maximum output power), we must look at the boundary current for which this happens with the selected inductance value.

$$ILB = \frac{D/F}{2L} \times (V_{IN} - V_O)$$

D refers to the duty cycle (use the minimum value for worst case), and f is the switching frequency.

If the expected output current at the operating point chosen will be greater than ILB, then the inductance value chosen will be sufficient to keep the supply in continuous mode operation. This equation is also useful for determining the limiting light load condition that will result in discontinuous mode operation. If the boundary is above the minimum light load that you expect to see, then another iteration of inductor value is necessary.

The inductor manufacturer may (but not always) also specify AC core loss; it is very important to make sure this is a minimum at the chosen operating frequency. Powdered iron cores are much less expensive, but have significantly higher core losses. The new "Kool Mu" material from Magnetics, Inc. is a powdered molyperm, and combines the benefits of using a powdered material (softer saturation curve, self-gapped) with the lower losses associated with molyperm. Coiltronics has inductors available that have been constructed from this new lower loss material. Solid ferrites also have low core losses. The best material with regards to losses is solid molyperm. It is usually quite expensive, which limits its use.

Recommended vendors are listed in Table 2.

VENDOR	LOCATION	PHONE NUMBER
Coiltronics	Boca Raton, FL	(407) 241-7876
Pulse Eng.	San Diego, CA	(619) 268-2400
Renco Elec.	Deer Park, NY	(516) 586-5566
Coilcraft	Cary, IL	(708) 639-6400
Gowanda	Gowanda, NY	(716) 532-2234

Table 2

Designing an inductor begins with choosing an inductor material that is appropriate for the operating frequency. Curves which show loss vs frequency are often provided in the material manufacturers data sheets. The above discussion of material types is also applicable here.

The next step is to select the geometry of the inductor to be used. Toroids have the best shielding characteristics, but are considered difficult to manufacture. Pot cores are also very popular when EFI/RFI noise is to be minimized, as the windings are almost entirely enclosed by ferrite material. They are, however, quite expensive. Although E cores tend to be too large in general for this type of application, Seimens has a series of EFD cores designed to be surface mountable, and low profile.

TABLE 1

SOURCE	P/N	R_{DS}(ON)	I_{DMAX}	VDSS	PKG	LOGIC L
Motorola	MTD10N05E	0.1Ω	10A	50V	Dpak	No
Int. Rect.	IRFZ46S	0.024Ω	38A	50V	SMD-220	No
Int. Rect.	IRLZ44S	0.028Ω	36A	60V	SMD-220	Yes
Int. Rect.	IRF7101	0.1Ω	3.5A	20V	SO-8	Yes
Siliconix	Si 9410DY	0.030Ω	7A	30V	SO-8	No*
Siliconix	Si 9936DY	0.050Ω	5A	30V	SO-8	No*
Siliconix	Si 9940DY	0.050Ω	5A	50V	SO-16 (dual)	No*

* = can be operated at 4.5V enhancement, but not specifically a logic level FET

Table 3 lists some recommended magnetic material/core vendors.

VENDOR	LOCATION	PHONE NUMBER
Micrometals	Anaheim, CA	(714) 630-7420
Ferroxcube	Saugerties, NY	(914) 246-2811
TDK	Skokie, IL	(312) 679-8200
Siemens	Iselin, NY	(201) 906-4300

Table 3

Selecting a core volume, V_E, is an iterative process in this application as the final form factor of the circuit will be dependent on how small the inductor can be made. Here is an example design procedure for ferrite materials (Note: this process will be different if powdered iron cores are used. Please consult the magnetic manufacturers information for this procedure). Calculate the first pass by using this equation:

$$V_E = \frac{I_{PK}^2 L\mu e\,(0.4\pi)}{B_O^2 \times 10^{-8}} \text{ (in cm)}$$

μe is effective permeability, and can be defined as the increase in inductance when the inductor is wound over a core instead of air. It is always a data sheet parameter. I_{PK} is peak inductor current.

B_O is peak flux density and can usually be estimated as 2500 gauss in most ferrite applications.

A more cautious way of estimating this is to look at the B-H curve specified for the material, and set this number equal to 1/2 the saturation value. Not every manufacturer uses the same units, so be careful here!

In space sensitive applications, it will quickly become obvious that something must be done to reduce μe! In most cases, we will need to add a gap to the core to reduce its size. Some data sheets, however, list cores that are already gapped. If a gapped core is standardly available, its gap size should be used in the calculations. Otherwise, select the core size that it desired, and work backwards with the above equation to obtain the μe that is needed. Gap size can be calculated by

$$g = \frac{l_E(\mu/\mu e - 1)}{\mu}$$

le, the magnetic path length, is also a standard data sheet parameter and should be specified in cm for this equation.

The previously mentioned method for checking for continuous vs discontinuous mode operation should now be used.

Next, the appropriate wire gauge should be determined by looking at the peak expected currents and wire gauge tables.

The number of turns needed can now be calculated by:

$$N = \frac{I \times l_E}{\mu e \times A_E \times (0.4\pi \times 10^{-8})}$$

Ae is effective core area, and is also a standard data sheet parameter.

Core losses are calculated by using the value of F_R found in the graph of loss vs frequency, and multiplying it by the core volume. Core losses for powdered iron are 25x that of ferrites!

If the manufacturer specifies this as core loss vs flux density and not vs frequency, this is estimated as:

$$B_{AC} = \frac{L \times I_{RIPPLE}}{2N \times A_E \times 10^{-8}}$$

I_{RIPPLE} = Peak ripple current in the winding

Copper losses are estimated to a first order by using:

$$\text{DC wire loss} = I_{RMS}^2 \times R_{DC}$$

R_{DC} is found from the wire gauge tables for a specific wire size, and is given in ohms/foot,and $I_{AVG}/\sqrt{2}$

The second order effects are added in by considering skin effect and proximity effect. A multiplication factor for the R_{DC} is selected from Figure 6, where the right hand axis is # of layers, the left hand axis is the factor itself, and the x axis is a function which takes skin depth into effect (see figure for pertinent equations). These second order AC wire losses are then:

$$\text{AC Wire Loss} = F_R \times R_{DC} \times I_{RIPPLE}^2$$

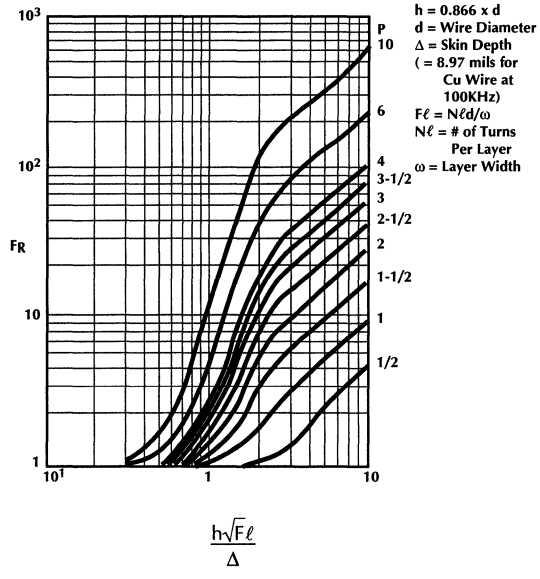


Figure 6. Ratio of AC to DC Resistance Due to Proximity Effect and Skin Effect

Total losses from the magnetics are then added up as the AC and DC winding losses plus the core losses. If the number is too high, then the previously described parameters can be "tweaked" until a reasonable value is reached.

Gate Drive and Linear Regulator Biasing Schemes

5V of gate enhancement voltage is required to turn on logic level FETs such as the ones used in this example. If regular FETs are used, 10V is necessary

If the 12V regulator is not needed, it can be used to provide a charge pump to enhance the gates (Figure 7). Taking into account all the voltage drops, the FETs will have about 8V of enhancement with a 12V supply. This approach is useful when a standard inductor is preferred.

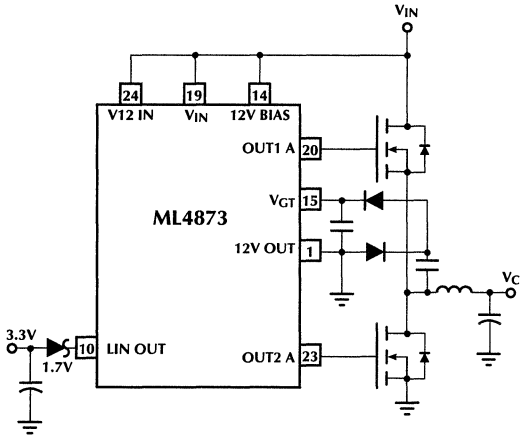


Figure 7. Charge Pump Gate Drive Voltage

For most applications, the best way to get the necessary gate drive is to use an integrated magnetics approach as shown in our design example. All we have to do is add additonal windings to either the 3.3V or the 5V inductor (however, it is recommended that the designer use the "A" regulator for the additional winding if burst mode is to be enabled).

The circuit in Figure 1 shows an integrated magnetics approach using the 3.3V out inductor to generate the V_{GT} potential (pin 15). Taking into account all necessary voltage drops, the turns ratio between the V_{GT} winding and the 3.3V primary should be 1:1 or 2:1 for 5V of enhancement, and 2 :1- 4:1 for 10V of enhancement. The voltage drops will vary with different line lengths, etc., so it is a good idea to experiment with the above ratios.

If the 5V output (B) inductor is used, the turns ratio between the Vgt winding and the primary should be 2:1 for 5V of enhancement and 3:1 for 10V of enhancement.

The key to reducing secondary output voltage variations is minimizing the winding resistances. As discussed previously, this is accomplished by minimizing number of turns, and using the smallest possible wire gauge.

One more secondary has been added to our scheme in the design example (Figure 1) to give us the input voltage required for the 12V linear regulator. The turns ratio here is 3.5:1 for the 3.3V version.

The 16 V bias voltage needed to operate the 12V regulator as an LDO can also be obtained by adding yet one more secondary to this inductor. A 1:1 turns ratio with the 3.3V inductor can be used if one end of the winding is tied to $V12_{IN}$ (14V).

An easier way of doing this is to simply tie the 12V bias pin (14) to the V_{GT} pin (pin 15) if 10V of enhancement is used. With 10V enhancement, this voltage is easily 17V.

Output Filter Design Considerations

In most applications, it is desirable to keep the output ripple voltages to a minimum. The primary contribution to ripple voltage is from the ESR or equivalent series resistance of the output capacitor(s). The second most important factor is the capacitance value.

The maximum desirable ripple voltage is usually well known, and is a function of the system requirements (ie PSRR, or power supply rejection ratio, of circuitry dependent on it for supply voltages).

In a buck regulator, the inductor current has the waveform of a "ramp on a step", where during the switch on-time the slope is $(V_{DC} - V_O)/L$, and during the off time it is $(V_O + 0.2)/L$. The center of this step is the DC output current of the regulator, and the peak to peak ramp amplitude, $I_2–I_1$, is usually estimated to be 0.2 I_{OUT}.

Using this expression for the current ramp, the effect of ESR on ripple voltage is given by:

$$V_{RIPPLE} = (0.2) \times (I_{OUT}) \times R_{ESR}$$

For capacitors such as aluminum electrolytics with appreciable ESR values, this is the primary contributor to the output ripple.

Capacitance size also affects ripple, and a minimum capacitance size can be determined by looking at this contribution to ripple voltage:

$$V_{RIPPLE} = \frac{[(0.2 \times I_{OUT}/4)t_{ON}]}{C}$$

$(0.2) \times (I_{OUT})/4$ is the average value of the triangle of inductor current during the on time of the switch.

A useful relationship to remember when using aluminum electrolytics is the $R_{ESR}C$ product is most often equal to 65×10^{-6}.

It is obvious that using a big capacitor and/or minimizing ESR is desirable for keeping ripple low. However, this is not always possible, as large capacitance values can cause instabilities in the feedback loop that are difficult to compensate as well as being large and not realistic for use in portable systems. ESR also tends to increase with increasing capacitance values.

ESR is frequency dependent, and should be measured at the switching frequency of the supply no matter what the capacitor data sheet says. A common trick for optimizing ESR and capacitance values without ending up with a supply the size of the moon is to parallel several capacitors. This works especially well if the capacitors used are of different materials, as they become resonant at different frequencies.

Electrolytics are the most cost effective solution and are available in a variety of temperature ranges and values. A better but more costly solution are the new Oscon polymeric capacitors from Sanyo, which have extremely low ESRs. Tantalums have very low ESRs, but are not generally available in large capacitance values.

Some ESR is desirable! If there were no output ESR, there would be no output zero to aid in stabilization of the double pole due to the LC corner frequency. This complicates the process considerably. A rough rule of thumb for a minimum ESR value is:

$$ESR_{MIN} = 0.1\sqrt{Lo/Co}$$

A large capacitance and small inductance value is important for minimizing surge impedance of the output filter, which results in good transient response to step load changes. This is an important performance measure in many applications with dynamic load requirements.

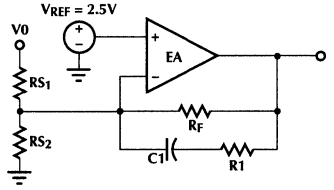
Another important consideration is the ripple current rating of the capacitors. Operating ripple of the supply must be less than the maximum specified by the manufacturer. This is usually specified to limit the temperature rise of the capacitor.

Designing a Compensation Network

Proper compensation is the most critical and easily the most difficult part of designing the supply. A well designed compensation network will accomplish two goals; first, it will ensure stability over the full range of operating and load conditions. Secondly, it will maximize loop bandwidth to allow for instantaneous load variations with minimal output voltage changes.

The ML4873 is a voltage mode converter, which means that we must compensate for a double pole occurring at $1/(2\pi\sqrt{Lo\ Co})$. The usual method of compensation for such a converter is a double pole, double zero approach. This is messy, and also can create problems due to unwanted poles and zeros from other combinations of the many R_S and C_S used in this approach.

If an appreciable capacitor ESR value exists, a better solution is to use the zero we have for free created by the output capacitor (Figure 8). Now, we only have to add one more zero to get the desired 45 degrees of phase margin.



$$F_{ZERO} \cong \frac{1}{2\pi R_1 C_1}$$

$$IF\ R_F \gg R_1$$

Figure 8. Basic Single Zero Compensation Scheme

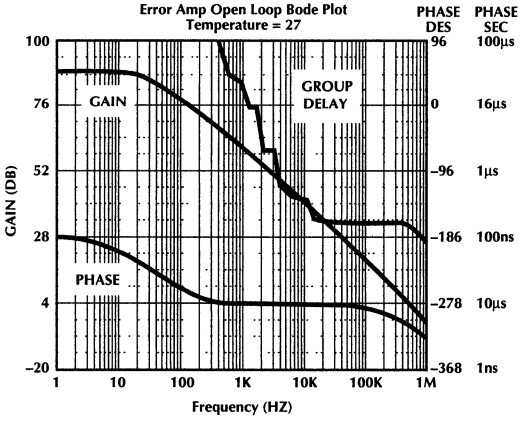


Figure 9. Open Loop Bode Plot of ML4873's Error Amplifier

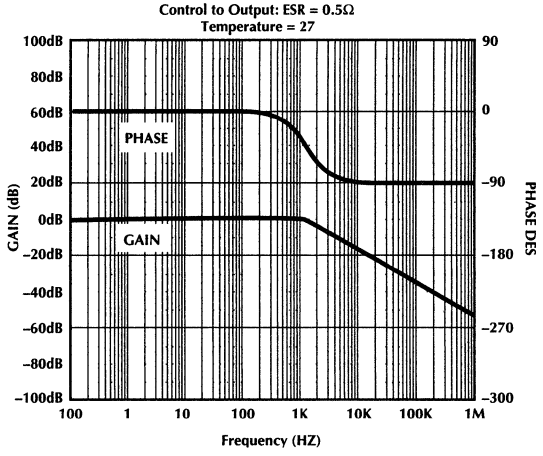


Figure 10. Bode Plot Showing the Gain and Phase of the Modulator to the Output

We can get away with this approach only when:

$$R_{ESR}C > \sqrt{LC/5}$$

This corresponds to a maximum ESR of 0.08 ohms in this design, with 300 µF of output capacitance.

The procedure used for designing this single zero compensation scheme for the 5V output was to first look at the open loop characteristics of the error amplifier. Experience has shown that the single pole in the error amplifier must be considered when compensating this circuit, as most controllers don't have internal ideal op amps as error amps. The ML4873 has 90 dB of open loop gain and a single pole at 31Hz (Figure 9).

Next, the gain of the modulator ,Mg, is determined as:

$$Mg = 0.5(V_{IN} - 1)/V_{RAMP}$$

V_{RAMP} = internally generated control circuit saw-tooth peak magnitude: 2.5V for the ML4873.

For a 50% duty cycle, V_{IN} will be about 10-11V. This works out to be about +6db. Now we must consider the losses from the output resistor divider. Since the error amplifier can only handle 2.5V at the input, we must divide the 5V down, giving us a loss = Gs = –6dB.

If we had no ESR zero, the combined modulator and output network would sit at roughly 0dB until it hit the output filter corner frequency. At 1.3kHz, we would roll off at –40dB/decade.

However, the ESR zero here is at 1kHz, so we only roll off at –20 db/decade.

In setting the appropriate gain, we must consider the trade off between having a wide bandwidth, and running the risk of gaining up the switching frequency and magnifying the switching noise. As a switcher is really a sampled data system, we could also get aliasing of the switching frequency if we are not careful. A safe bet is to set the unity gain crossover point at no more than 1/5 the switching frequency, which is 20kHz in this case.

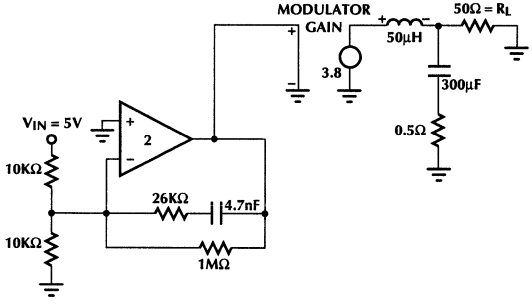


Figure 11a. Microcap Model with Single Zero Compensation Scheme

Looking at the Bode plot of the modulator (Figure 10), we see that roughly +20dB of additional gain is needed at 20KHz to bring the closed loop system to 0dB. We then set a DC feedback resistor to provide this using the Thevenin equivalent, $(R_{S1})x(R_{S2})/(R_{S1} + R_{S2})$, of the sampling resistors as our input resistor. This also provides more bandwidth from the non-ideal internal op amp at the expense of gain. This resistor needs to be large, so that it doesn't interfere with the zero to be placed in the feedback loop.

Next, we want to set the zero close to the double pole at the corner frequency to make sure that we have the required 45 degrees of phase margin. A good way to properly select the location of this zero is to simulate it using software such as Microcap(8), and vary its location until an optimum position can be found. Light load conditions should be used for the simulation, as they will represent the worst case conditions for phase margin. The use of good simulation tools also allows us to see the change in response vs. ESR variations (they will happen as a function of temperature, use, etc). The optimum location found by this method is 2kHz (Figure 11).

In cases where the ESR and output capacitor combination are too small, and the zero is too far out in frequency to properly compensate the double pole, we must add in another zero. The best way to do this is to use the approach shown in Figure 12, which was used in our design example. Once again, R_F provides gain reduction at DC for the error amplifier which gives us more bandwidth from the overall system.

Figure 13 shows the Bode plot obtained from this error amplifier approach. Through multiple simulations, it was determined that optimum placement of the zeros was at 1.3kHz (the double pole frequency), and 3.2kHz, respectively. Separating the zero frequencies instead of placing them both at the pole frequency gives us higher phase boost and helps to reduce the gain peaking or Q of the circuit.

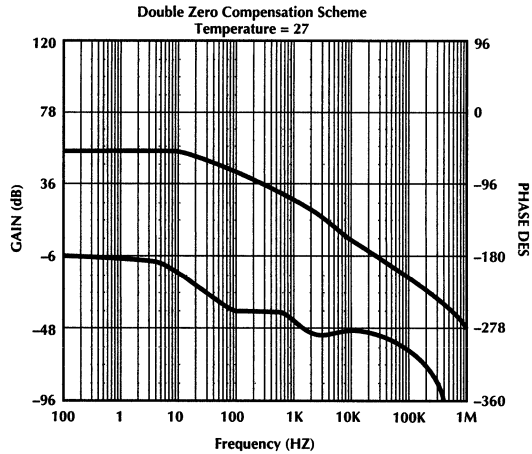
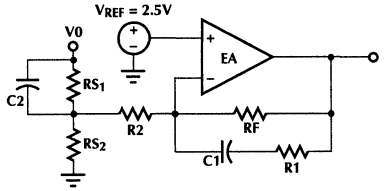


Figure 11b. Bode Plot of the Closed Loop Response Obtained When ESR = 0.5Ω, Using a Single Zero Compensation Scheme



$$F_{Z1} = \frac{1}{2\pi C_1 R_1} \text{ if } R_F \gg R_1$$

$$F_{Z2} = \frac{1}{2\pi C_2 R_2} \text{ (as } R_{S1} \text{ is shorted at sufficiently high frequency)}$$

Figure 12. Double Zero Compensation Scheme

As systems with low ESR tend to be heavily over-damped, phase changes much faster with frequency. Another way of ensuring stability, although not an absolute criteria, is to make sure that the slope of the Bode plot is only –20dB/decade at the crossover point.

The circuit as shown in Figure 1 was tested over all allowable conditions of line and load, and found to be stable.

Implementing Current Limit and Soft Start

Current sensing is vital to prevent any damage to the circuitry and/or load in the event of a short circuit.

The threshold has been set at 200mV internally in the ML4873. In this design, a 1 oz. copper trace, 10 mil wide and 2 cm long is used to provide a sense resistor with roughly 25 milliohm of resistance. This will set up a current trip point that will vary from 5–10A depending on temperature, etc. If the temperature coefficients of the PCB traces do not provide enough stability in resistance, an external resistor can be used. Dale Electronics (7), among others, provides many resistors that have excellent temperature stability, hence a predictable shutdown can be achieved.

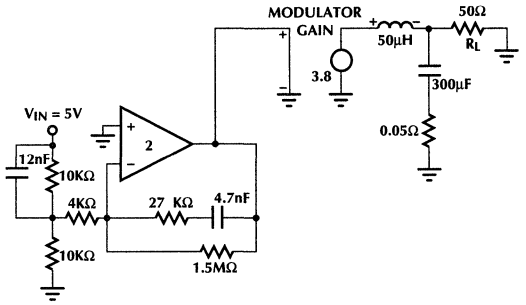


Figure 13a. Microcap Model for the Double Zero Compensation Scheme

Filtering the sense pin is not recommended. As the current sense comparator has a limited bandwidth, high frequency noise will be ignored.

In order to keep the 100kHz ripple (which could reach 200 mV) from causing spurious shutdowns, it is very important to keep the impedance between pins 22, 12 and 21 as low as possible.

Soft start is included to prevent in-rush currents generated during a short from damaging the FETs as it comes back up. It is triggered after an over current shutdown, and is important as over-current shutdown and sense is cycle by cycle. In the event of a short, soft start will reduce the volt second product of the inductor preventing any catastrophic failures.

A 15µA current source charges the externally supplied soft start capacitor, and a 6.5mA current sink discharges it.

Layout Techniques

In switched mode systems, layout is critical.

Solderless bread boards, or "white" boards, should not be used for prototyping as they are inherently noisy.

High current paths should be kept as short as possible while providing wide traces to keep inductance and resistance to a minimum. Filter capacitors (C3, C7, C8) should be placed as close to the IC as possible.

It is important not to mix signal, frequency compensation and feedback returns with high current returns.

A bus bar type ground plane may be helpful. All connections should be made directly to this if it is used to keep stray inductances to a minimum.

If the sensing element for the current limit comparator is a circuit board trace, the current path from the input capacitor to the sensing node should not include any stray resistances.

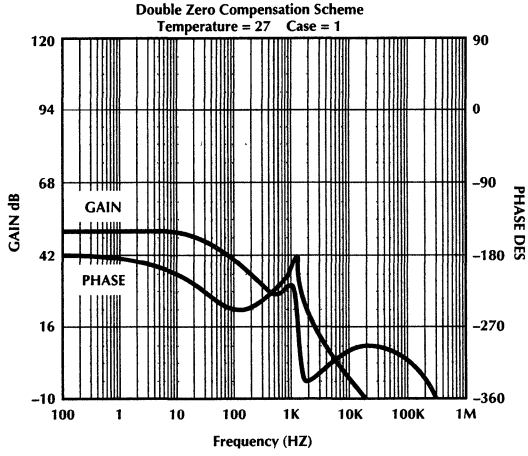


Figure 13b. Bode Plot of the Closed Loop Response Obtained When ESR = 0.05Ω Using a Double Zero Compensation Scheme

It is also a good idea to lay out the board such that the 5V and 3.3V outputs are on opposite sides. This will prevent any interaction effects between the two different magnetics.

Practical Realities of Burst Mode

The ML4873 has a burst mode pin with hysteresis that allows the designer to choose whether or not to use this option. Burst mode is only available on output A, the 3.3V output as shown in this application example (Figure 1).

When in burst mode, an audible noise may be heard from the inductor. Varnishing the wires used in the inductor will reduce this noise.

LOAD SWITCHING

Many battery operated systems use a load switch to disconnect power from the load when in sleep mode or other power saving modes. Figure 14 shows an easy way to implement this by using V12 IN to provide gate enhancement for a very low RDS_{ON} N channel FET switch. Q1 is used only for control and can be very small. Q2 must have a very low RDS_{ON} to prevent efficiency losses.

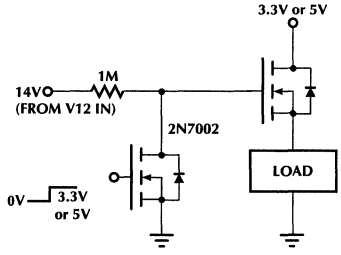


Figure 14. Load Switch

GENERATING A NEGATIVE CONTRAST VOLTAGE FOR LCD BACKLIGHTING

Many portable applications use an LCD display, which typically requires a negative adjustable bias voltage for backlighting. Figure 15 shows an example of such a negative regulator. An inverter is used to generate the polarity reversal. The zener diode is part of a start-up circuit only, and doesn't affect steady state circuit operation.

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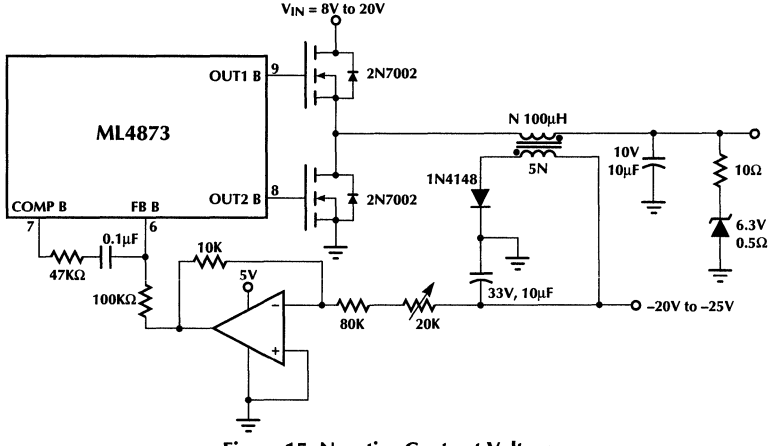


Figure 15. Negative Contrast Voltage

Applications Considerations and Circuits for the ML4861

by Daryl Sugasawara
and Jens Paetau

INTRODUCTION

Battery powered applications are becoming more desirable and common. In the past, battery powered applications were not suitable because of the high quiescent currents, low efficiency and the inability to operate at low input voltages. In addition, too many components and a large battery size made the design of small hand-held equipment not very practical.

This application note will highlight some of the design considerations when developing battery powered equipment, as well as illustrate some application circuits of the ML4861 boost converter. These applications are:

ML4861 EMI/RFI Output Filter
ML4861 Shutdown for 2-3 Cell Applications
ML4861 Shutdown for 1 Cell Applications
ML4861 AC Adapter Application Circuit
Paralleling of 2 or more ML4861s
Battery Charger using the ML4861

Designing battery powered systems require several considerations including efficiency (battery life), space (real estate), type of battery (small space) and cost. The ML4861 provides a complete solution for a DC to DC converter for battery powered applications with minimum components, very high efficiency, low input voltage and low cost. Various linear and switching regulators are available in the market today, but none with the high performance characteristics and versatility of the ML4861.

PERFORMANCE CONSIDERATIONS

Efficiency is perhaps the most important quality of switching regulators; especially for battery powered systems since this will translate directly into battery life. To accurately estimate the efficiency of a switching regulator, it is necessary to estimate all the losses of the power dissipating components. The ML4861 combines Pulse Frequency Modulation (PFM) and Synchronous Rectification to create a boost converter that is both highly efficient, low cost and very simple to use. The PFM approach is based on charging a single inductor for a fixed "on" time and then discharging it completely before the next cycle. This topology is particularly efficient since it will only use the switch in order to maintain the output voltage. At light loads, for example, it will pulse only every once-in-a-while in order to maintain the desired output voltage.

In theory, the overall efficiency of the converter is by definition the output power divided by the input power:

$$E(\%) = \frac{I_{OUT} \times V_{OUT}}{I_{IN} \times V_{IN}} \times 100 = \frac{I_{OUT} \times V_{OUT}}{(I_{OUT} \times V_{OUT}) + \Sigma P_{LOSS}}$$

where P_{LOSS} is the sum of all the losses of the converter.

To minimize the losses of the converter, it is necessary to minimize the quiescent current, the switch driver current, the switch "on" resistance, the freewheeling diode losses

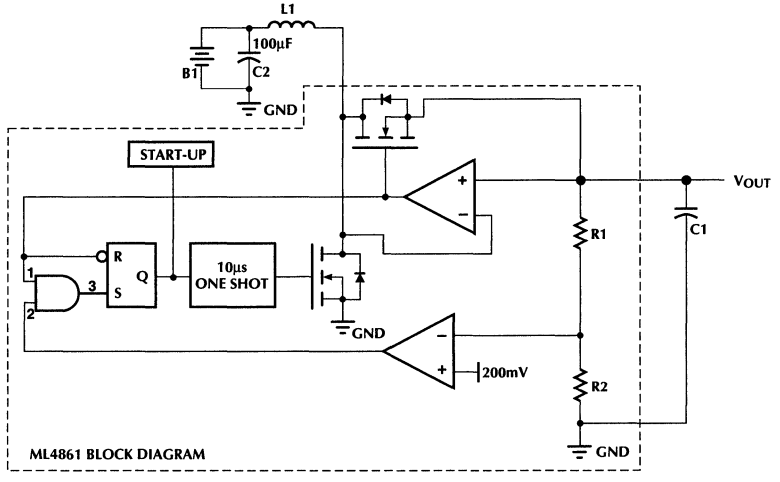


Figure 1. ML4861 Block Diagram

(i.e. P-Channel Synchronous rectifier losses), the inductor winding and core losses, and any other external resistances which may be dissipating any power.

The ML4861 quiescent current drawn into V_{IN} is only 50µA (typ) in addition to 5µA from the feedback resistors, R1 and R2. This drain current is particularly important for applications which consume very little power (<5mW) in the idle state and need to maximize their efficiency at low current levels.

The switch "on" resistance losses or DC losses of the switch are proportional to the square of the switch current, times the duty cycle (D).

$$P_{SW} = (I_{SW})^2 \times R_{ON} \times D$$

The ML4861 is manufactured in a low voltage BiCMOS process which minimizes the quiescent current and optimizes the R_{ON} resistance of the internal N and P channel devices. The AC current losses of the switch are negligible compared to the DC losses because of the zero current switching mechanism of the ML4861 topology.

Boost converters require an external diode which is often the major source of power loss in low current, low output voltage applications. The ML4861 includes a synchronous rectifier which uses a power P-MOSFET in place of the output diode. This significantly reduces the forward drop of the output rectifier and thus improves the efficiency by a minimum of 6%. For boost converters with output voltages as low as 3.3V, synchronous rectification is an absolute must.

Inductor losses are another important piece of the puzzle. Inductor core loss increases as the input voltage is increased since the peak current increases. Ferrite core materials will exhibit lower core losses than inductors wound on powdered iron cores. Also, the larger the core size, the lower the amount of core and copper loss. Core losses also decrease as switching frequency decreases. Thus, there is a trade-off between the size of the inductor and core and copper losses for a given operating frequency. Typically, larger inductors can improve the efficiency by 3 to 5%.

When selecting an inductor for the ML4861, important considerations are:

1. Determine the inductance value
2. Determine the type of inductor required (shielded, unshielded, low cost, low profile, smallest size, high efficiency.)

The inductance value can be determined two ways:

An approximate inductance value can be calculated by:

$$L = \frac{(V_{IN})^2 \times T_{ON} \times \eta}{2 \times V_{OUT} \times I_{OUT\,MAX}}$$

where T_{ON} = On-time of the internal one shot (10µs)

and η = Expected efficiency (0.7 to 0.9)

The second and best way to determine the inductance required, is to use the curves shown in the datasheet of the ML4861 (i.e. for a given maximum output current and minimum input voltage, a specific nominal inductor value can be chosen).

To determine the inductor type, it is necessary to look at the manufacturers selection guide. The recommended inductor vendors are:

Sumida	(708) 956-0666
Coiltronics	(407) 241-7876

These are the recommended surface mount inductor types. The selected inductor should have the lowest DC resistance and highest permissible DC current for the intended application.

	SUMIDA	COILTRONICS
Low Cost	CD54	
Low Profile	CD73	
High Efficiency	CD73	
Small Size	CD54	
Shielded Low Cost	CDR74B	CTX_–2P
Shielded Low Profile (Note 1)	CLS62	CTX_–1P
Shielded High Efficiency	CDR105B	CTX_–2
Shielded Small Size	CDRH64	CTX_–1

Note 1: May not apply for all applications because of the permissible DC Current.

The most important design consideration on the output capacitor is the effective series resistance (ESR). This resistance, which is in series with the capacitor leads, limits the effectiveness of the capacitor at high frequencies and determines the peak-to-peak output ripple of the converter. The value of the peak-to-peak voltage swing is typically between 30mV and 100mV. To effectively reduce the output ripple, additional capacitors can be connected in parallel.

Converters can be modeled as switched current sources driving the output capacitor; and the output capacitor can be modeled as an ideal capacitor in series with an inductor, in series with a parasitic resistance (ESR). It is the inductor which creates a voltage spike on top of the fundamental output ripple. This high transient noise can sometimes affect the performance of some electronics, and needs to be filtered out. To properly isolate this high frequency noise from the system circuitry, an LC filter can be added with a 3dB cutoff frequency one decade above the switching frequency of the converter. (Refer to Figure 2.)

Another application of the ML4861 which requires careful selection of components is the shutdown circuitry which can be included between the input of the ML4861 and the battery. (See Figure 3.) This MOSFET needs to have a low "on" resistance as well as a low gate threshold voltage to minimize the loss at low battery input voltages. In this application, the P-Channel MOSFET is turned "on" whenever the switch is closed. Opening S1 causes the MOSFET to turn "off", and thus disconnecting the battery from the rest of the circuitry. This simple mechanism provides zero current drain of the battery whenever set in the shutdown mode.

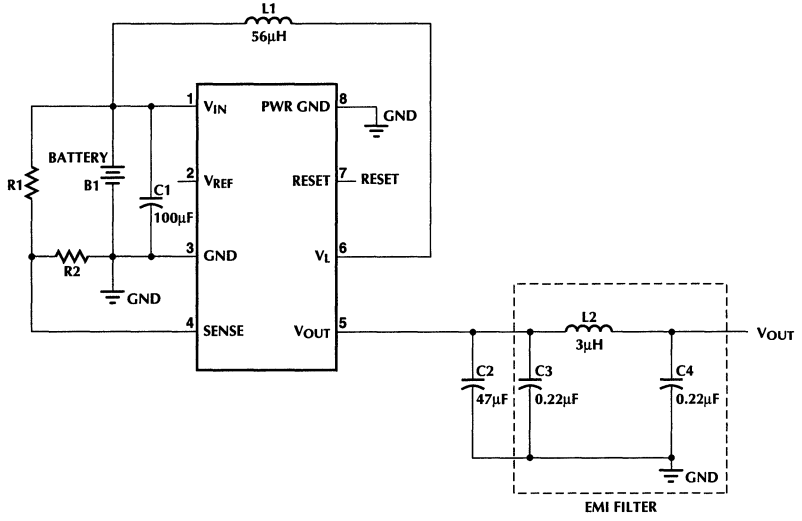


Figure 2. EMI/RFI Output Filter

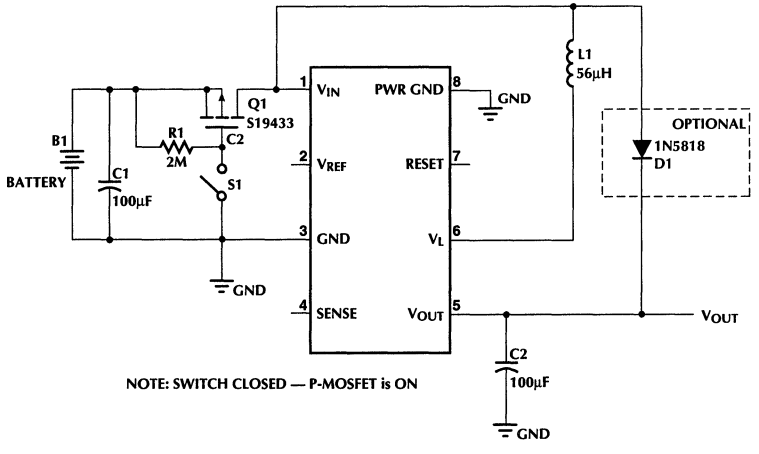


Figure 3. Shutdown Application Circuit for 2 to 3 Cell Batteries

Also note the optional diode protection included from pin 1 to pin 5. This diode protects the device from fast rising input voltages and assures proper start-up conditions.

Single cell applications which require a shutdown mechanism need to use the adjustable version of the ML4861. (See Figure 4.) This application circuit uses the external voltage divider (R1 and R2) to set the desired output voltage up to a maximum of 6V. The diode in series with the switch is intended to pull the sense pin high and thus disabling the ML4861.

Many times it is necessary to be able to connect and disconnect the battery whenever an AC adapter is used to power the system circuitry and/or also to charge the battery and extend the operating life of the same. (Please refer to Figure 5.) The next application circuit is very similar to the 2 to 3 cell shutdown circuit used in Figure 3. In this application, a zener diode generates a reference voltage which in conjunction with an NPN pass transistor is used to pre-regulate the input voltage to the ML4861 and to supply the required current from the AC adapter to the boost regulator. A pull-up resistor connected to the reference voltage senses the presence of the AC adapter and disables the MOSFET. This isolates the battery from the boost regulator and thus extends the battery life. A small charge path can also be included from the NPN transistor to the battery input to further extend the battery life.

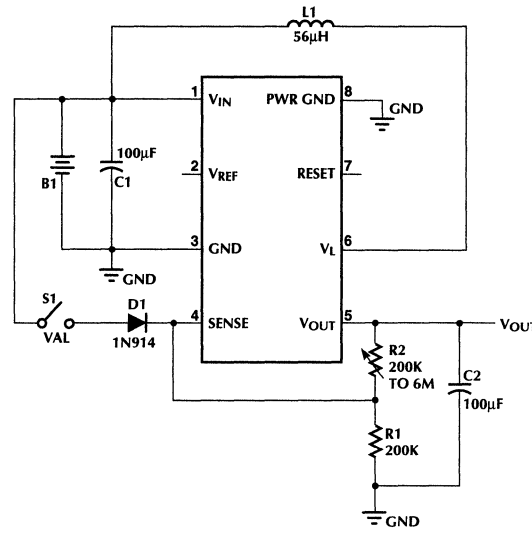


Figure 4. Shutdown Application Circuit for 1 Cell Battery Operation

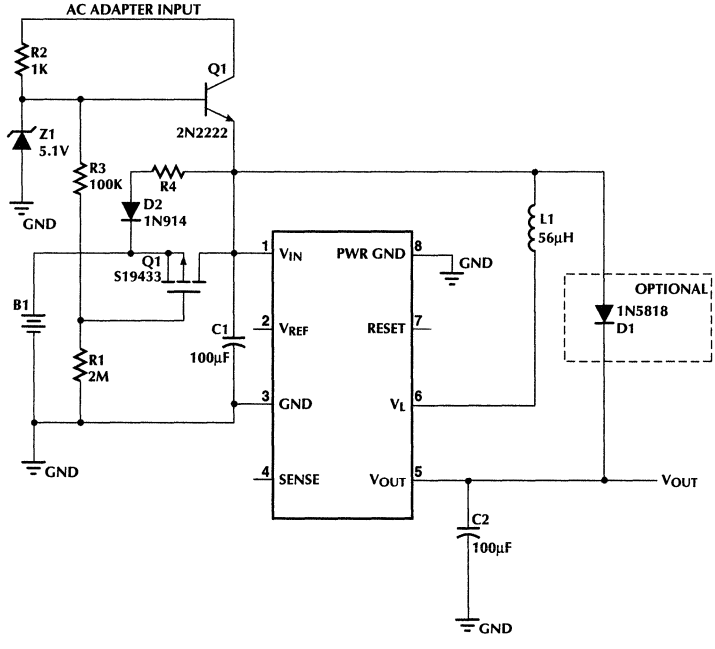


Figure 5. AC Adapter Application Circuit

Many times it is necessary to be able to supply more current than the maximum output current the boost converter can handle for a given input voltage and desired efficiency level.

The next application circuit shows a method of achieving higher current and efficiency levels out of the ML4861 boost regulator. (See Figure 6.)

Paralleling of the two converters is simple and has the advantage of achieving higher currents at higher efficiency levels. Both input and output capacitors can be shared, however it is always best to locate both input and output capacitors as close to the device as possible. In addition, having two capacitors on the output effectively halves the ESR and thus reduces the peak to peak output ripple. The inductor can not be shared because each of the converters is operating independent of each other. As a matter of fact, one of the converters will always supply the first half of the total available supply current, until it reaches a maximum. At this point, the second converter takes over and supplies the remaining half.

Paralleling also has the advantage of increasing the efficiency for a set output current. For example, supplying 150mA with 2V input, requires a 27µH inductor and achieves 83% efficiency. Paralleling two devices, and again supplying 150mA with 2V input requires a 56µH inductor, and achieves 90% efficiency.

Another application of the ML4861, is a battery charger application. (See Figure 7.) This circuit uses the adjustable version of the ML4861 to charge 4 NiCad cells with a single Alkaline battery. The output capacitance in this application circuit is required since the 40Ω resistor will create a large ripple voltage on the output. Efficiency of the converter will depend on the input voltage and charge current requirements.

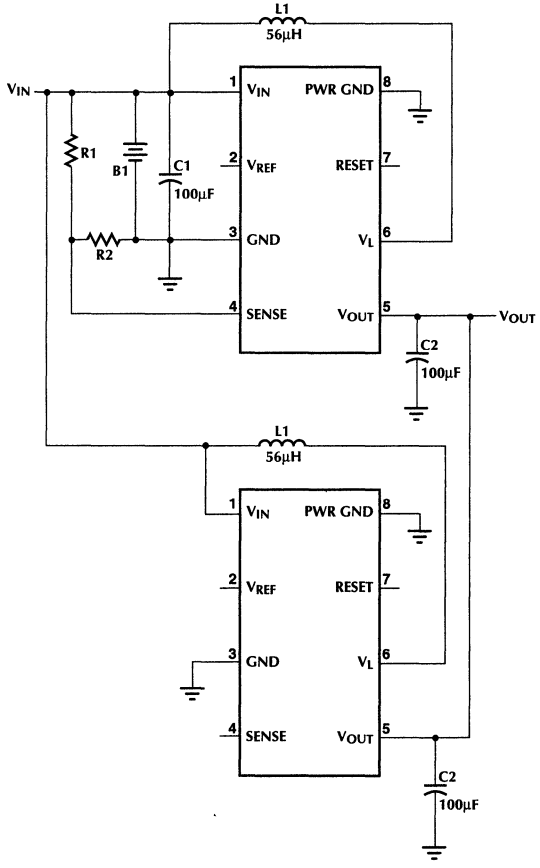


Figure 6. Paralleling Application Circuit

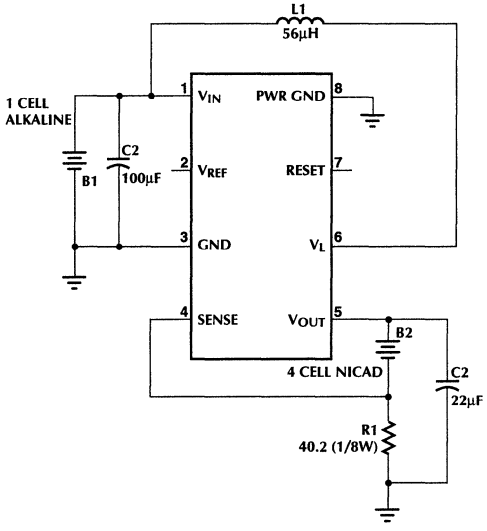


Figure 7. Battery Charger Application

by Daryl Sugasawara
and Jens Paetau

Safety, EMI and RFI Considerations

INTRODUCTION

The filtering of conducted and radiated noise is an intricate part of the design of a power supply or DC to DC converter. This Application Note addresses the origin of generated EMI and RFI and the best ways to control them. The topics discussed will be:

- Background on Safety Agencies and Documents
- EMI filter design for higher power Switch Mode Power Supplies
- EMI sources and ways to control them
- PCB layout considerations
- EMI and RFI Filter considerations for low power boost converters; ML4861 design example

SAFETY AGENCIES AND BACKGROUND

The main objective of the national and international safety regulatory agencies is to provide the user with a safe and quality product which is not going to interfere with other electronic equipment. These safety agencies and standards are different depending on the country they originated. Equipment manufacturers that would like to sell their product in these countries first need to get their product approved by the corresponding safety agencies. Most power supply manufacturers use the IEC (International Electro Technical Commission), VDE (Verband Deustcher Electrotechnik), or UL (Underwriters Laboratories) and CSA (Canadian Standards Association) as their base to the majority of the world's safety requirements. Regarding the radiated and conducted interference levels acceptable in the United States and internationally are FCC's Docket 20780 and VDE's 0806. One point to consider is that both, FCC and VDE standards exclude sub assemblies from compliance to these rules. This is understandable since power supply radiation and conduction characteristics can vary depending on different system level loading. Therefore the final product, where the switching power supply is to be used, must also comply to EMI and RFI specifications. Both agencies require manufacturers to minimize the radiated and conducted interference of their equipment which is connected to the AC mains and employs high frequency digital circuitry.

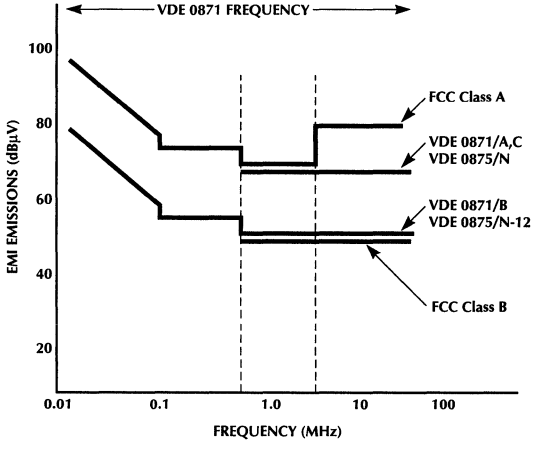


Figure 1. FCC and VDE Compliance Curves

VDE has subdivided its RFI regulations into two categories

a) 0-10KHz unintentional high frequency generation (VDE 0875, VDE 0879)

b) 10KHz-30MHz intentional high frequency generation (VDE 0871, VDE 0872)

The FCC includes all electronic devices which generate signals at a rate greater than 10KHz. The FCC and VDE regulations closely follow each other. The FCC class A specification covers business, commercial and industrial environments, while FCC B covers residential environments only. The main difference as can be seen in figure 1 is the frequency span covered by both agencies. The VDE frequency range for EMI and RFI emissions covers a spectrum from 10KHz to 30MHz, while FCC's frequency span covers only the range of 450KHz to 30MHz.

EMI FILTER DESIGN IN SWITCH MODE POWER SUPPLIES

How is EMI generated? Technically, EMI is generated by a varying electric or magnetic field and transmitting them by means of conductive, inductive or capacitive coupling, through free space or a combination of these means. Switching power supplies are one of the worst sources for EMI and RFI generation because of their inherent current voltage waveforms and very fast switching times. Switching transistors, MOSFETs, diodes, transformers, and inductors are the main source of RFI generation. The common mode noise generated by switching is a problem in large computer systems and can be controlled with an input filter between line, neutral and chassis. The differential noise, like transient response, is a function of the output filter capacitors and filter chokes.

To properly contain the conducted noise in power supplies, ceramic capacitors help reduce the high frequency noise and should be located as close to the connector (input/output) as physically possible. Note that some power supply topologies are better than others when it comes to the conducted noise. For example, a flyback power supply has a triangular current waveform which inherently generates less RFI noise than other converters such as a forward or a bridge converter that switch rectangular current waveforms.

Suppressing noise in switching power supplies is a very tricky business. Ideally EMI and RFI should be contained with a minimum increase in weight, circuit complexity, cost and efficiency. The idea is to block, or bypass the interference noise. This can be achieved by introducing a high impedance into the path of the interfering currents and bypassing them to ground through a low impedance path. One way to do this is to place filters on the input and output leads, but this is only helpful in cases where the system ground is very close to chassis ground.

For the AC lines, a coupled inductor with very low stray capacitance, two safety approved capacitors (x type) between the lines, and small capacitors (y type) between each line and ground should suppress switching noise to acceptable levels.

These capacitors and inductors are typically within the following values:

Cx = 0.1µF to 2µF

Cy = 2200pF to 33000pF

L = 1.8mH at 25A to 47mH at 0.3A

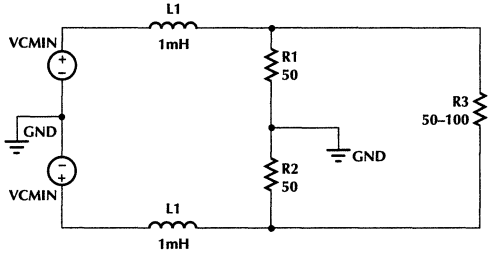


Figure 2A. First Order Filter

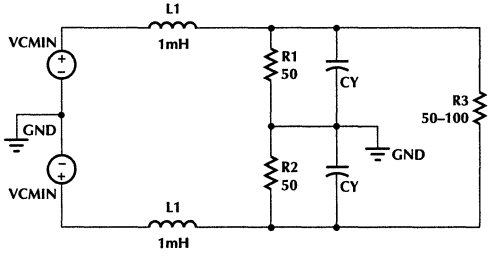


Figure 2B. Second Order Filter

The value of the common mode inductor for a first order filter (Figure 2A) is simply the load in ohms divided by the radian frequency at and above which the signal is to be attenuated. For example, attenuation above 4000Hz into a 50 ohm load would result in a 2mH inductor (50/2π4000). This would imply that the attenuation at 4000Hz would be 3dB, increasing at 6dB per octave.

The second order filter (Figure 2B) has two advantages in that it provides 12dB per octave attenuation and it provides greater attenuation at frequencies above the inductor self resonance. The typical common mode transfer function can be expressed as follows:

$$\frac{VCM_{OUT(S)}}{VCM_{IN(S)}} = \frac{1}{\frac{1+L}{R_L s + LCs^2}}$$

The damping factor which corresponds to the gain of the filter at the 3dB point, should be chosen to be anywhere between 1 and 4. In this example a value of 3 chosen and the following can be deduced:

$$\zeta = 3 = \frac{L\omega_N}{2R_L}$$

If we choose a cutoff frequency of 15KHz and a load resistance at the cutoff frequency of 50Ω, we can calculate the inductance as:

$$L = \frac{3 \times 2 \times R_L}{2\pi \times f_N} = \frac{3 \times 2 \times 50}{2\pi \times 15000} = 3.2mH$$

The filter capacitance (y-capacitors) can be calculated as:

$$C = \frac{1}{(2 \times \pi \times f_N)^2 L} = 0.035\mu F$$

If necessary, adjustments can be made to these components in order to reduce leakage current requirements set by the safety agencies. Another important point is to make sure that the resonant frequency of the input filter is lower than the switching frequency of the power supply. Higher frequency power supplies are usually easier to filter than lower frequency supplies.

The discharge resistor as recommended by VDE 0806 and IEC 380 is calculated as follows:

$$R = \frac{1}{2.21 \times C_X} \approx 1M\Omega$$

Where t = 1sec and C is the sum of x capacitors.

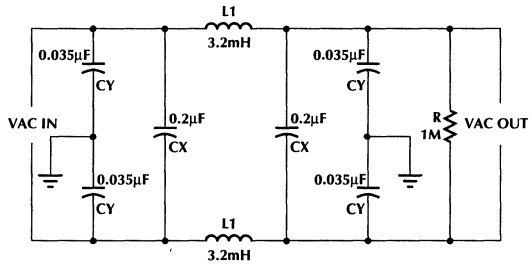


Figure 3. Second Order Filter

The final EMI filter for a power supply operating at power levels below 200W is shown in figure 3.

Further improvements to the frequency response of this pi filter can be achieved by inserting several such sections in series, but this would increase cost, weight and space. Other solutions which help the filtering of switching noise is converting the storage capacitors into a pi filter section, and connecting an extra line choke between the storage capacitors. Note that there are several manufacturers of EMI filter modules or components which can provide the power supply designer a ready solution for EMI and RFI suppression.

EMI SOURCES AND WAYS TO CONTROL THEM

Design considerations should be taken in the following areas, which are the typical RF generating sources:

- DC isolation
- Circuit grounding
- Susceptibility to audio frequency and RF noise conducted to the supply on power lines
- Interference generated in the supply and conducted to the other parts of the system on power lines
- Radiated interference and susceptibility
- Turn-on, turn-off transients

All of these problems can be solved by placing a component in the right place such as to avoid interference. This makes the layout of the power supply one of the most crucial steps when developing a switcher. Here are some hints on what to keep in mind when developing and laying out a power converter:

Care should be taken in the generation of fast rise current spikes resulting from the sudden reverse biasing of diodes used in the transformer rectifier circuitry.

Ringing in the transformer can be clamped out by placing snubbers across the windings. Snubbers are discrete circuits which reduce the switching transients dissipatively as heat, or non-dissipative, by returning the energy back to the input.

A small ferrite bead on the leads of the main MOSFET switching devices will suppress the generation of high frequency ringing at turn-on and turn-off periods.

A faraday shield, returned to DC ground, and placed between the primary and the secondary windings will prevent capacitive coupling of voltage transients into the power supply and output leads.

In order to minimize the lower and higher frequency harmonics generated in the transformer, a high permeability material must be chosen. This results in low exciting volt amperes and low core losses, which means better efficiency, smaller size and reduced weight. Also, decoupling RF noise at the source by using good high frequency capacitors with low inductance and low ESR is helpful.

Lead lengths needs to be kept to a minimum to avoid RF energy radiating into free space.

Decoupling outgoing leads with small capacitors will localize conducted energy before spreading to the rest of the circuitry.

PCB LAYOUT CONSIDERATIONS

It is always possible to contain or fix EMI and RFI to a certain degree, but the real trick is at the layout stage of the PC board. Consider switching waveforms as the ones generated from a DC to DC converter and the traces which carry these signals as the antennas. These traces are related in a complex way with the radiated fields from the converter. The prediction of radiation from a circuit requires the identification of the frequency content and their absolute magnitudes of the time domain waveform. Of particular importance is that there is no energy contained below the fundamental frequency, and 99% of the energy is contained below $1/(\pi\ tr)$ (where tr is the rise time of the waveform). Note that the edge rate is a key driver (or limiter) for the frequencies of concern. Power supply and DC to DC converter designers try to achieve fast rise and fall times to minimize the switching losses, but this high di/dt conditions will generate ground and trace bounce voltages which can excite components and cables to radiate in the common mode manner. Multi-layered boards which use good ground and power planes provide the low impedance power distribution necessary for good power supply decoupling. The following are some of the techniques used to minimize EMI and RFI generation:

Enclosing signals between power and ground planes achieves a locally shielded enclosure that reduces radiation by 30 to 40dB and also reduces radiated susceptibility and ESD susceptibility. Think of traces as transmission lines. A good rule is to keep signals with 1nsec rise or fall times shorter than 9cm (3.5in).

Traces which carry high frequency currents should be surrounded by a coplanar ground trace in order to reduce both radiation and crosstalk to other traces.

Another good design practice is to provide a chassis ground ring around the periphery of the board. This ring provides a formidable shield or field interceptor to prevent radiation at the circuit boundaries. This layout practice is also recommended as an interceptor for Electrostatic discharges, and thus provides a more robust design.

The use of ferrites is very effective to directly suppress high frequency energy by both reactive impedance and absorptive losses. Ferrite beads for example use soft magnetic materials which require little energy to alter the magnetic flux. These ferrites become more resistive at high frequencies, which effectively reduce the bandwidth and higher frequency energy content of digital signals. Ferrite chokes are also commonly used in loose wires to cancel out common mode and differential mode currents. These ferrites come in all kinds of shapes, sizes and mounting options (including surface mount).

Try and keep high frequency currents to a local area of the PCB. This practice limits the capability of those currents to excite an efficient radiator.

PCB Layout and Component Selection Summary:

1. Always use a solid ground and power plane (multi layer boards are preferred).
2. Border PCB with chassis ground trace.
3. Centrally locate high frequency clock circuits. (distribute signals symmetrically)
4. Locate line drivers and receivers close to the connectors.
5. Decouple high frequency currents locally.
6. Use shielded components.
7. Use bulk capacitors near ports.
8. Use ferrites for input/output lines.
9. Use narrow and buried traces when possible. (depends on the current it needs to handle)
10. Use high frequency ceramic (surface mount when possible) capacitors and locate close to the pin.
11. Keep high di/dt lines as short as possible.
12. Keep input and output leads away from electromagnetic noise generators.
13. Minimize capacitive coupling to chassis grounds.

EMI AND RFI CONSIDERATIONS FOR LOW POWER BOOST REGULATORS; ML4861 DESIGN EXAMPLE

The ML4861 is a small boost converter used in 1 to 3 cell battery applications. This DC to DC converter comes in three versions which are: 3.3V, 5V, 6V or adjustable V_{OUT}. One of the main features of this small boost converter is the fact that it only requires one inductor and two capacitors to form a complete battery boost converter operating from 1 to V_{OUT}–0.5V and offering very good efficiency (>90%). Some applications however, require that conducted and radiated noise be maintained to a minimum within a certain window of the frequency spectrum. In such cases, the appropriate selection of components and layout is very important. For example some pager or cellular applications may require to keep EMI and RFI noise to a minimum from 1MHz to 400MHz, in which case the following considerations should be made:

Use the above mentioned layout considerations when designing the PCB to minimize the radiated and conducted energy.

Use a shielded inductor with the appropriate inductance, maximum current and lowest possible DC Resistance value to optimize the efficiency of the converter. Use the tables shown in the data sheet of this device, and place it as close to the IC as physically possible. Note, the higher the inductance, the better the efficiency, but the lower the maximum current available. Also, the higher the input voltage, the higher the efficiency. For a given input voltage (1, 2 or 3 cells), select the highest inductance which meets the desired maximum output current, efficiency and size limitations of the design. The recommended inductor manufacturers which offer shielded power inductors are:

Coiltronics-CTX Series	Tel. (305) 781-8900
Sumida-CDRH Series	Tel. (708) 956-0666
Sumida-CDR63B, CDR74B and CDR105B Series	

Use low ESR capacitors close to the output voltage pin to minimize ripple voltage. It is also recommended to use two capacitors (one at the output of the ML4861 and one at the port) in case long VCC lines are required. The recommended capacitor manufacturers are:

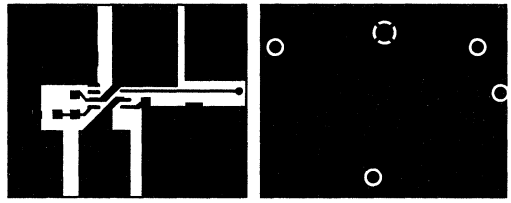
Matsuo-267M Series	Tel. (714) 969-2491
Sprague 595D Series	Tel. (603) 224-1961

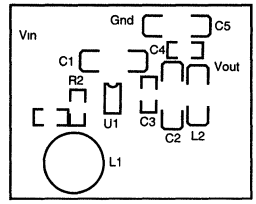
To further reduce the conducted noise to the rest of the circuitry, use high frequency ceramic capacitors preceded by a small ferrite bead to shunt high frequency noise as shown in Figure 4, Option 2. Another possibility is shown as Option 3, where a small, high frequency EMI filter is connected directly to the output port. When using these small filters, it is important to have a solid ground plane connected to chassis ground to effectively shunt the high frequency energy to ground. The recommended filters are:

Murata Erie	Tel. (800) 831-9172
NFM40R Series (Rated current = 200mA)	
NFM41R Series (Rated current = 300mA)	
NFM61R/H Series (Rated current = 2A)	

The selection of these filters improves the EMI and RFI feedthrough at the expense of efficiency of the converter. It is therefore important to choose a low DC resistance device which also meets the required converter current and insertion loss characteristics.

Included is the recommended layout and schematic. Note that the schematic includes several components which are optional and may not be required for the majority of applications.





ML4861 Suggested Layout

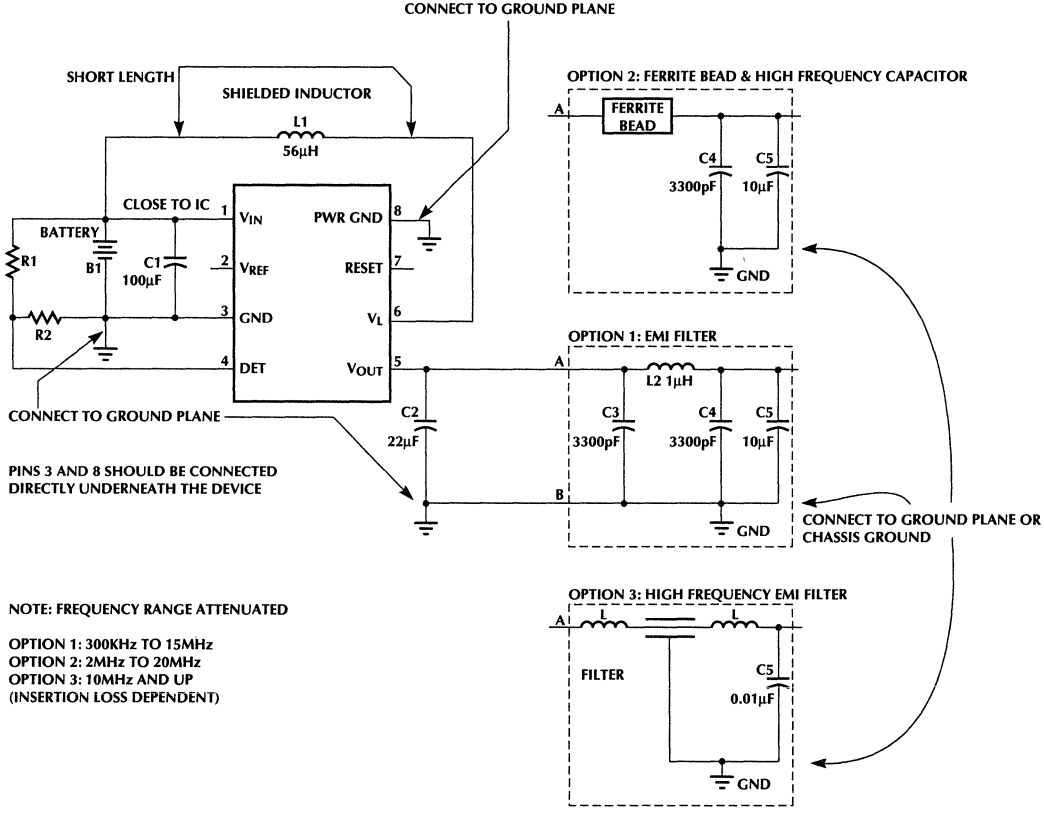


Figure 4. ML4861 EMI/RFI Circuit Suggestions

George A. Hall

Low Cost Electronic Ballast System Design

GENERAL DESCRIPTION

This application note describes a dimmable ballast system design using the ML4831 electronic ballast controller IC. This system can be evaluated using the ML4831EVALuation kit. The ML4831EVALuation board is a low cost, improved version of Micro Linear's ML4830 dimmable ballast EVAL board. Careful attention was given to reducing the magnetic's cost of the EVAL board as well as other costly components. In addition, the design was improved to both increase and linearize the dimming range, eliminate lamp shut-off at low intensities, reduce visible standing waves and simplify the lamp-out protection circuitry. All components used are inexpensive and easy to obtain.

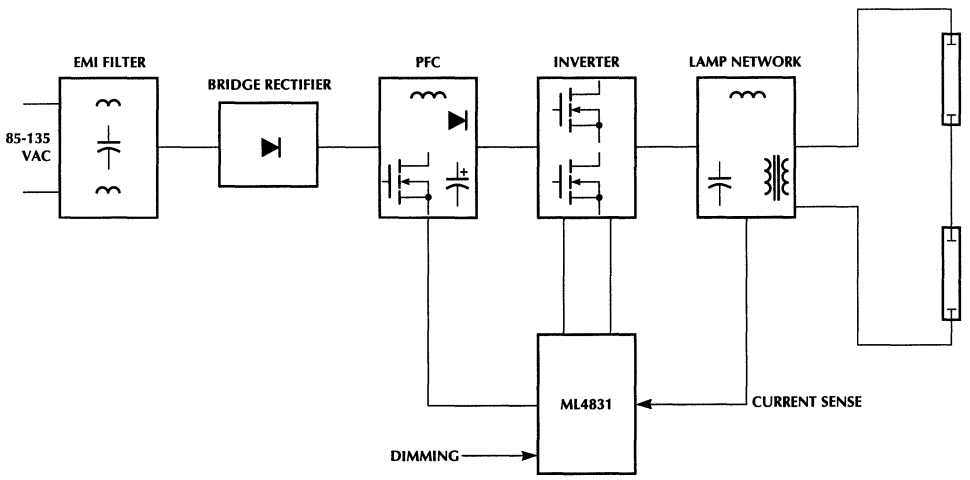
Operating from 85 to 135VAC line, the ML4831EVALuation board is a power factor corrected 60W electronic ballast with a dimming range capable of a 20:1 intensity change. Optimized to power two series connected T8 fluorescent bulbs, the ML4831EVAL board displays all the features of Micro Linear's latest ballast controller IC. The mode of operation used for pre-heat, striking and dimming of the bulbs is the widely accepted variable frequency, non-overlapping inverter topology. This EVAL board may be used with various bulbs other than T8's (such as T12's). See "Powering Other Fluorescent Lamps."

THEORY OF OPERATION

Figure 1 displays the block diagram of the ML4831EVAL board.

Applying AC line voltage to the EVAL board supplies start-up power to the ML4831 enabling gate drive for the PFC boost MOSFET Q1 and inverter FETs Q2 and Q3. PFC action generates a well regulated 205VDC supply for the lamp inverter circuit and steady-state supply voltage for the ML4831. The inverter stage consists of 2 totem pole configured N-channel power MOSFETs with their common node supplying the lamp network. The pair of MOSFETs are driven out of phase by the ML4831 with a 50% duty cycle. The lamp network is a parallel resonant circuit series-fed by the inverter transistors through a wave-shaping and current limiting inductor T3. The inductance of the resonant circuit is formed by T3's inductance and the primary inductance of the power transformer T4. The power transformer also provides safety isolation from the primary circuit to the bulbs. The lamp intensity is controlled by sampling the lamp current with current sensing transformer T5. T5's secondary current is converted to a voltage and fed to the ML4831's Lamp Feedback error amplifier. The amplifier output voltage varies in accordance with the amount of intensity required (set by potentiometer R23), internally adjusting the switching frequency to the inverter stage. The impedance characteristics of the lamp network results in lower lamp currents (and intensity) when the inverter stage frequency is increased.

BLOCK DIAGRAM



PERFORMANCE DATA

To measure system performance across the range of permissible input voltages use a variac or adjustable AC source.

A typical ML4831EVALuation board will have the following performance characteristics when operated as shown in the test conditions:

ML4831EVAL BOARD TEST RESULTS

	85VAC	120VAC	135VAC	Units
Efficiency	88	90	89	%
THD	2.32	2.12	2.35	%
P.F.	0.995	0.984	0.975	%

Test Conditions: 2 series wired T8 lamps (full intensity), 25°C
Equipment Used: Voltech Digital AC Power Analyzer #PM1000

The ML4831EVALuation board provides testpoints at the following circuit nodes:

TP1 GND
TP2 V_{CC}
TP3 INHIBIT
TP4 PFC Boost Voltage
TP5 Resonant Network (attenuated by 10x)

TYPICAL WAVEFORMS

Figures 2-5 display typical oscilloscope waveforms taken at various points on the eval board. A brief description precedes each figure. Test conditions and oscilloscope settings are given below each photo. The waveforms were taken with the eval board powering two series connected T8 bulbs.

PFC BOOST VOLTAGE (Fig. 2, TP4)

The DC bus for the inverter stage is derived from the rectified AC line. Note the 120Hz (2x line frequency) ripple voltage superimposed on the DC voltage. This is the result of the power factor correction of the AC line voltage. The peak to peak amplitude of the ripple voltage increases as the lamp intensity increases.

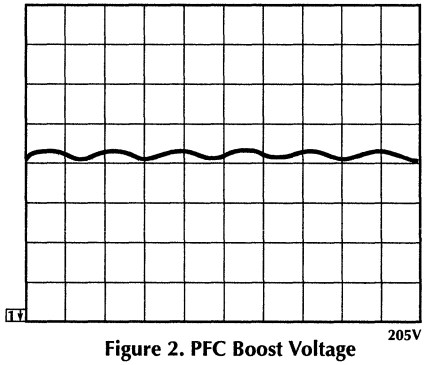


Figure 2. PFC Boost Voltage

Scope Setting: 100V/div, Horiz = 5ms/div
Test Conditions: Lamps @ maximum intensity, 120VAC
Equipment Used: Tektronix TDS540 Digitizing Scope

INVERTER VOLTAGE/CURRENT (Fig. 3)

The boosted DC bus voltage is chopped by Q2 and Q3 resulting in the square wave (upper trace) appearing at the input to the lamp network (Q2, Q3, T3 node). The resulting current in T3's primary winding appears in the bottom trace.

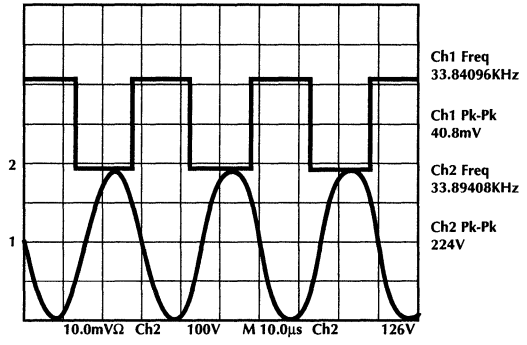


Figure 3. Inverter Output Voltage/Current

Scope Setting: Top = 100V/div, Bottom = 0.5A/div, Horiz = 10µs/div
Test Conditions: Lamps @ maximum intensity, 120VAC
Equipment Used: Tektronix TDS540 Digitizing Scope, Tektronix AM503 Current Probe Amplifier Assy

LAMP NETWORK VOLTAGE (Fig. 4, TP5)

The voltage at the T3, T4 and C19 node is so high as to warrant the use of an X100 probe for inspection. For safety and ease of visualization it is attenuated by 10x on the eval board by resistors R27, R28 and R29. Notice the positive DC offset voltage caused by the blocking capacitor C20. (The attenuator may not be needed for production).

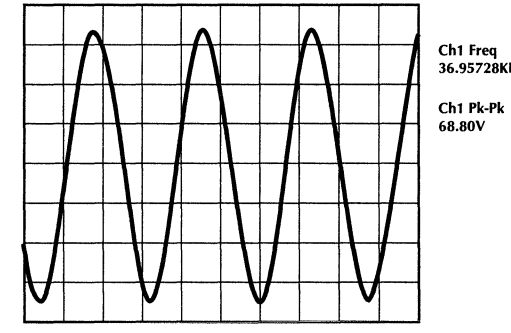


Figure 4. Lamp Network Voltage (atten. 10x)

Scope Setting: 10V/div, Horiz = 10µs/div
Test Conditions: Lamps @ maximum intensity, 120VAC
Equipment Used: Tektronix TDS540 Digitizing Scope

INVERTER/LAMP CURRENT (Fig. 5, T3 Pri, T4 Sec)

A comparison of the inverter current (same as Figure 5, lower trace) and lamp current is shown below. The phase difference is typical when an AC current source drives a parallel resonant network. There is however, no phase difference between the lamp current (T4 secondary current) and T4's primary current. The user will note an increase in the inverter current when the lamp current (and intensity) are decreased. This phenomena is a result of the decrease in total impedance of the lamp network at higher excitation frequencies and the "negative" resistance characteristic of the fluorescent lamp.

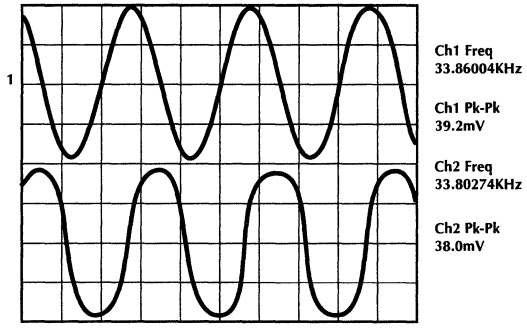


Figure 5. Inverter/Lamp Current

Scope Setting: Top = 0.5/div, Bottom = 0.1A/div, Horiz = 10µs/div
Test Conditions: Lamps @ maximum intensity, 120VAC
Equipment Used: Tektronix TDS540 Digitizing Scope, Tektronix AM503 Current Probe Amplifier Assy

LAYOUT CONSIDERATIONS

The ML4831EVAL Board contains high impedance, low level and low impedance, high level circuits and as such requires extra care in component placement, grounding and pc trace routing. This board makes use of a ground plane to achieve stable, noise free operation. When laying out a PC board for ballasts several precautions must be observed. The following list serves as a guide to ease the layout and minimize re-layout revisions.

1. Return the low side of the timing capacitor (C6) directly to the IC ground pin.
2. Bypass the reference and supply voltage pins directly to the IC ground pin with a 0.01µFd or greater low ESR capacitor.
3. Make a direct, low ohmic connection from the IC ground to the PFC current sense resistor (R1).
4. Return all compensation components directly to the IC ground pin, keeping the lead lengths as short as possible.
5. Use a ground plane (if permissible) for all low side (ground) connection points.
6. Whether using a ground plane or a single point ground layout, use heavy traces form the sense resistor/Q1 source node.
7. Separate rapidly changing waveforms; such as Q1's drain, from sensitive, high impedance circuits, such as the timing capacitor, PFC current sense input, error amplifier input/output, etc.

POWERING OTHER FLUORESCENT LAMPS

The ML4831EVAL Board design was optimized to power T8 lamps with cathodes requiring pre-heating prior to ignition. With little or no circuit modifications, other lamps can be driven with this board. For example, this EVAL board was used to power T12 lamps. Due to the different impedance of these lamps, the board delivers about 8 watts (4 watts/lamp) less.

For higher wattage lamps the PFC boost voltage can be increased by either increasing the value of R12 and R9 or decreasing the value of R13. Use extreme caution when attempting this as C11's voltage rating of 250V may be exceeded resulting in venting or catastrophic failure of the capacitor!!!

Lower wattage bulbs may not require any circuit modification, however, because of different lamp impedance characteristics, it may be necessary to decrease R5's (RSET) value to allow lower lamp intensities. Increasing T5's primary turns may also be necessary to achieve lower lamp intensities.

For rapid start lamps, adjusting the value R15 and C13 will shorten the pre-heat time while removing these components will eliminate the pre-heat time. See the ML4831 data sheet for details.

Instant start lamps have no cathode(s) and therefore no need for pre or sustained heating. If desired, remove R15 and C13 and employ the connection technique shown in Figure 6. For operator safety and to avoid circuit failure insulate any remaining wires from the EVAL board.

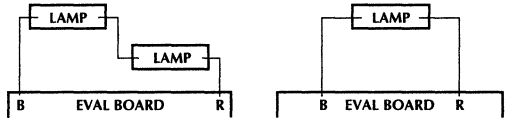


Figure 6. Dual/Single Instant-Start Lamp Connections

TABLE 1: PARTS LIST FOR THE ML4831EVAL EVALUATION KIT

CAPACITORS

QTY.	REF.	DESCRIPTION	MFR.	PART NUMBER
2	C1, 2	3.3nF, 125VAC, 10%, ceramic, "Y" capacitor	Panasonic	ECK-DNS332ME
1	C3	0.33µF, 250VAC, "X", capacitor	Panasonic	ECQ-U2A334MV
4	C4, 8, 9, 22	0.1µF, 50V, 10%, ceramic capacitor	AVX	SR215C104KAA
2	C5, 21	0.01µF, 50V, 10%, ceramic capacitor	AVX	SR211C103KAA
1	C6	1.5nF, 50V, 2.5%, NPO ceramic capacitor	AVX	RPE121COG152
2	C7, 12	1µF, 50V, 20%, ceramic capacitor	AVX	SR305E105MAA
1	C10	100µF, 25V, 20%, electrolytic capacitor	Panasonic	ECE-A1EFS101
1	C11	100µF, 250V, 20%, electrolytic capacitor	Panasonic	ECE-S2EG101E
1	C13	4.7µF, 50V, 20%, electrolytic capacitor	Panasonic	ECE-A50Z4R7
3	C14, 15, 17	0.22µF, 50V, 10%, ceramic capacitor	AVX	SR305C224KAA
1	C16	1.5nF, 50V, 10%, ceramic capacitor	AVX	SR151V152KAA
1	C19	22nF, 630V, 5%, polypropylene capacitor	WIMA	MKP10, 22nF, 630V, 5%
1	C20	0.1µF, 250V, 5%, polypropylene capacitor	WIMA	MKP10, 0.1µF, 250V, 5%
1	C23	0.068µF, 160V, 5%, polypropylene capacitor	WIMA	MKP4, 68nF, 160V, 5%
1	C24	220µF, 16V, 20%, electrolytic capacitor	Panasonic	ECE-A16Z220
1	C25	47nF, 50V, 10%, ceramic capacitor	AVX	SR211C472KAA
1	C26	330pF, 50V, 10%, ceramic capacitor	AVX	SR151A331JAA
1	C27	22µF, 10V, 20%, electrolytic capacitor	Panasonic	ECE-A10Z22
RESISTORS:				
1	R1	0.33Ω, 5%, 1/2W, metal film resistor	NTE	HWD33
1	R2	4.3K, 1/4W, 5%, carbon film resistor	Yageo	4.3K-Q
2	R3, 26	47K, 1/4W, 5%, carbon film resistor	Yageo	47K-Q
1	R4	12K, 1/4W, 5%, carbon film resistor	Yageo	12K-Q
1	R5	20K, 1/4W, 1%, metal film resistor	Dale	SMA4-20K-1
1	R6	360K, 1/4W, 5%, carbon film resistor	Yageo	360K-Q
1	R7	36K, 1W, 5%, carbon film resistor	Yageo	36KW-1-ND
3	R8, 22, 11	22Ω, 1/4W, 5%, carbon film resistor	Yageo	22-Q
1	R9	402K, 1/4W, 1%, metal film resistor	Dale	SMA4-402K-1
1	R10	17.8K, 1/4W, 1%, metal film resistor	Dale	SMA4-17.8K-1
1	R12	475K, 1/4W, 1%, metal film resistor	Dale	SMA4-475K-1
1	R13	5.49K, 1/4W, 1%, metal film resistor	Dale	SMA4-5.49K-1

TABLE 1: PARTS LIST FOR ML4831EVAL EVALUATION KIT (Continued)

QTY.	REF.	DESCRIPTION	MFR.	PART NUMBER
RESISTORS: (Continued)				
4	R14, 17, 24, 25	100K, 1/4W, 5%, carbon film resistor	Yageo	100K-Q
1	R15	681K, 1/4W, 5%, carbon film resistor	Yageo	681K-Q
2	R16, 29	10K, 1/4W, 1%, metal film resistor	Dale	SMA4-10K-1
1	R18	4.7K, 1/4W, 5%, carbon film resistor	Yageo	4.7K-Q
1	R21	33Ω, 1/4W, 5%, carbon film resistor	Yageo	33-Q
1	R23	25K, pot (for dimming adjustment)	Bourns	3386P-253-ND
1	R27	48.7K, 1/4W, 1%, metal film resistor	Dale	SMA4-48.7K-1
1	R28	41.2K, 1/4W, 1%, metal film resistor	Dale	SMA4-41.2K-1
DIODES:				
4	D1, 2, 3, 4	1A, 600V, 1N4007 diode (or 1N5061 as a substitute)	Motorola	1N4007TR
2	D5, 6	1A, 50V (or more), 1N4001 diodes	Motorola	1N4001TR
1	D7	3A, 400V, BYV26C or BYT03 fast recovery or MUR440 Motorola ultra fast diode	GI	BYV26C
8	D8, 9, 10, 11 12, 13, 14, 15	0.1A, 75V, 1N4148 signal diode	Motorola	1N4148TR
IC's:				
1	IC1	ML4831, Electronic Ballast Controller IC	Micro Linear	ML4831CP
TRANSISTORS:				
3	Q1, 2, 3	3.3A, 400V, IRF720 power MOSFET	IR	IRF720
MAGNETICS:				
1	T1	T1 Boost Inductor, E24/25, 1mH, Custom Coils P/N 5039 or Coiltronics P/N CTX05-12538-1 E24/25 core set, TDK PC40 material 8-pin vertical bobbin (Cosmo #4564-3-419), Wind as follows: 195 turns 25AWG magnet wire, start pin #1, end pin #4 1 layer mylar tape 14 turns 26AWG magnet wire, start pin #3, end pin #2 NOTE: Gap for 1mH ±5%		
1	T2	T2 Gate Drive Xfmr, L_{PRI} = 3mH, Custom Coils P/N 5037 or Coiltronics P/N CTX05-12539-1 Toroid Magnetics YW-41305-TC Wind as follows: Primary = 25 turns 30AWG magnet wire, start pin #1, end pin #4 Secondary = 50 turns 30AWG magnet wire, start pin #5, end pin #8		

TABLE 1: PARTS LIST FOR ML4831EVAL EVALUATION KIT (Continued)

MAGNETICS: (Continued)

QTY.	REF.	DESCRIPTION	MFR.	PART NUMBER
1	T3	T3 Inductor, L_{PRI} = 1.66mH, Custom Coils P/N 5041 or Coiltronics P/N CTX05-12547-1 E24/25 core set, TDK PC40 material 10 pin horizontal bobbin (Plastron #0722B-31-80) Wind as follows: 1st: 170T of 25AWG magnet wire; start pin #10, end pin #9. 1 layer of mylar tape 2nd: 5T of #32 magnet wire; start pin #2, end pin #1 1 layer of mylar tape 3rd: 3T of #30 Kynar coated wire; start pin #4, end pin #5 4th: 3T of #30 Kynar coated wire; start pin #3, end pin #6 5th: 3T of #30 Kynar coated wire; start pin #7, end pin #8 NOTE: Gap for 1.66mH ±5% (pins 9 to 10)		
1	T4	T4 Power Xfmr, L_{PRI} = 3.87mH, Custom Coils P/N 5038 or Coiltronics P/N CTX05-12545-1 E24/25 core set, TDK PC40 material 8 pin vertical bobbin (Cosmo #4564-3-419) Wind as follows: 1st: 200T of 30AWG magnet wire; start pin #1, end pin #4. 1 layer of mylar tape 2nd: 300T of 32AWG magnet wire; start pin #5, end pin #8 NOTE: Gap for inductance of primary: (pins 1 to 4) @ 3.87mH ±5%		
1	T5	T5 Current Sense Transformer, Custom Coils P/N 5040 or Coiltronics P/N CTX05-12546-1 Toroid Magnetics YW41305-TC Wind as follows: Primary = 3T 30AWG kynar coated wire, start pin #1, end pin #4 Secondary = 400T 35AWG magnet wire, start pin #5, end pin #8		
INDUCTORS:				
2	L1, 2	EMI/RFI Inductor, 600µH, DC resistance = 0.45Ω	Prem. Magnetics	SPE116A
FUSES:				
1	F1	2A fuse, 5 x 20mm miniature	Littlefuse	F948-ND
2		Fuse Clips, 5 x 20mm, PC Mount		F058-ND
HARDWARE:				
1		Single TO-220 Heatsink	Aavid Eng.	PB1ST-69
2		Double TO-220 Heatsink	IERC	PSE1-2TC
3		MICA Insulators	Keystone	4673K-ND

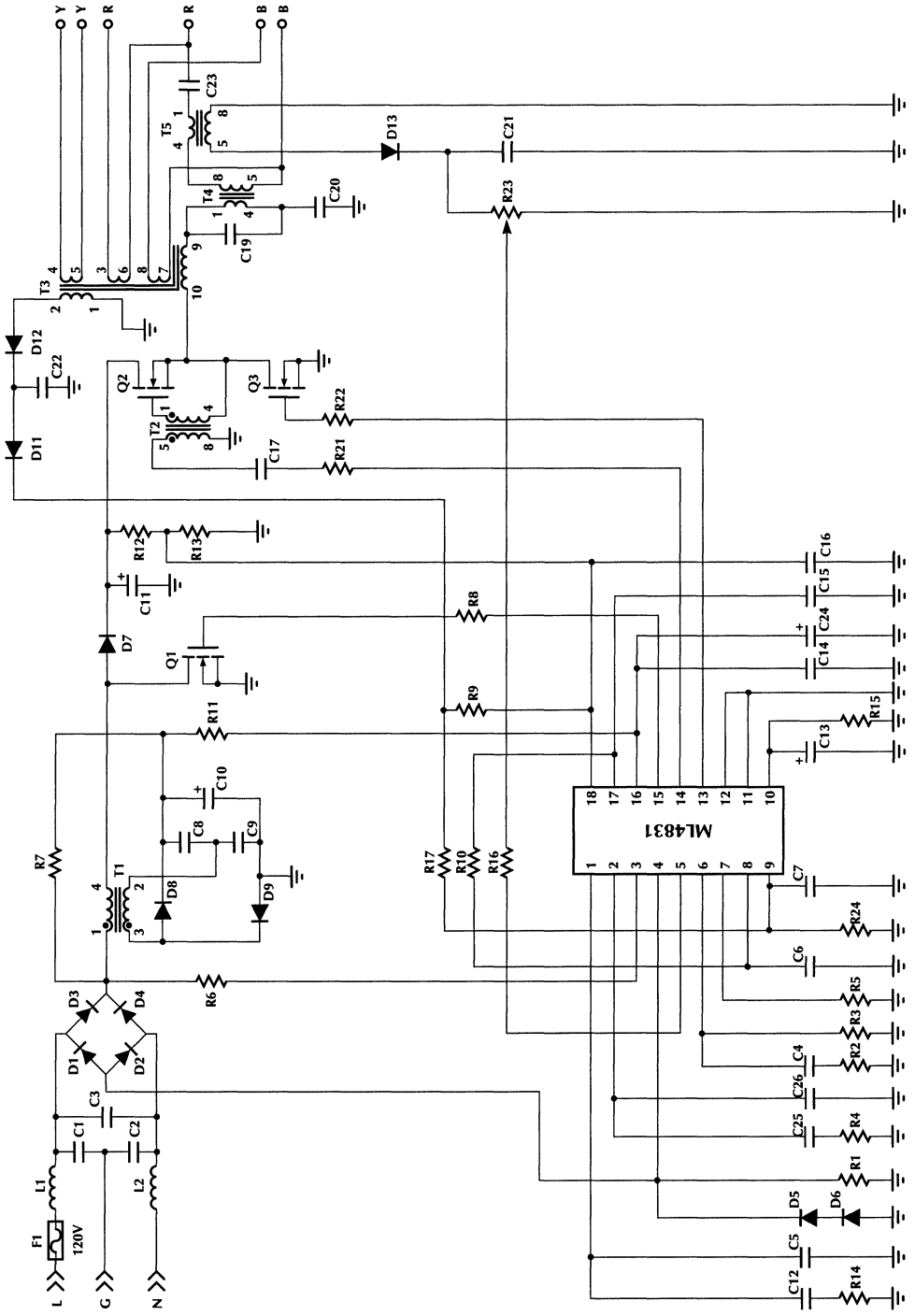


Figure 7. Circuit Schematic of the ML4831EVAL Evaluation Kit

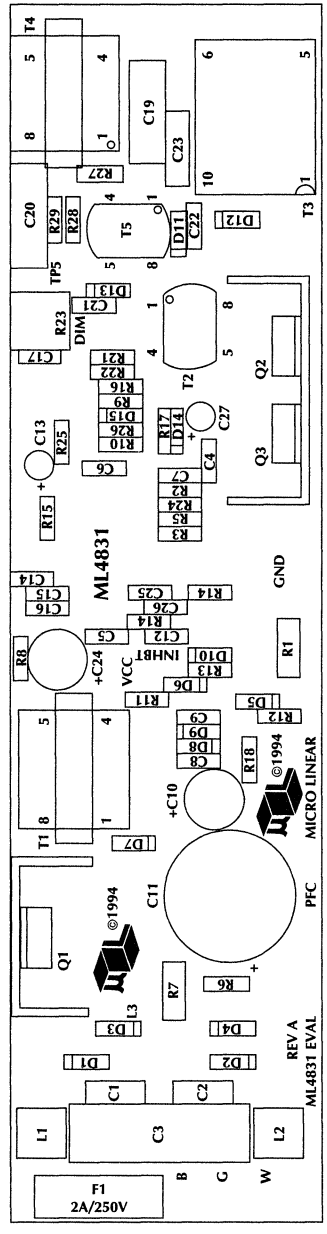


Figure 8. ML4831EVAL Component Silkscreen Layer

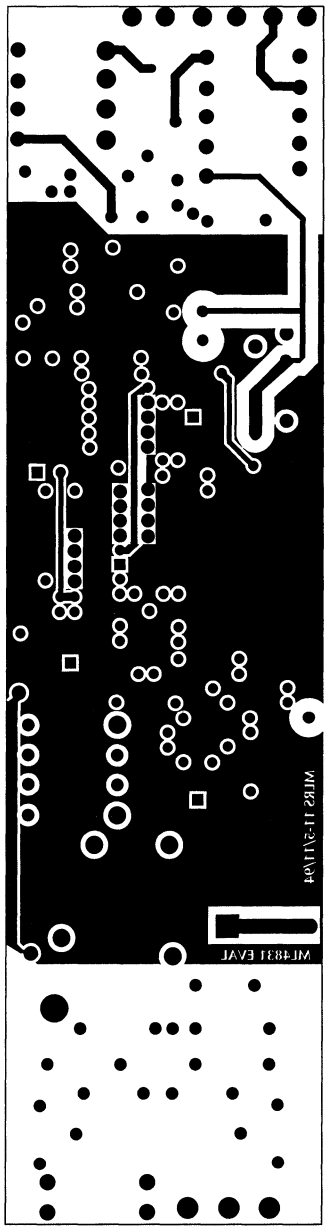


Figure 9. ML4831EVAL Ground Plane and Bottom Trace Layer

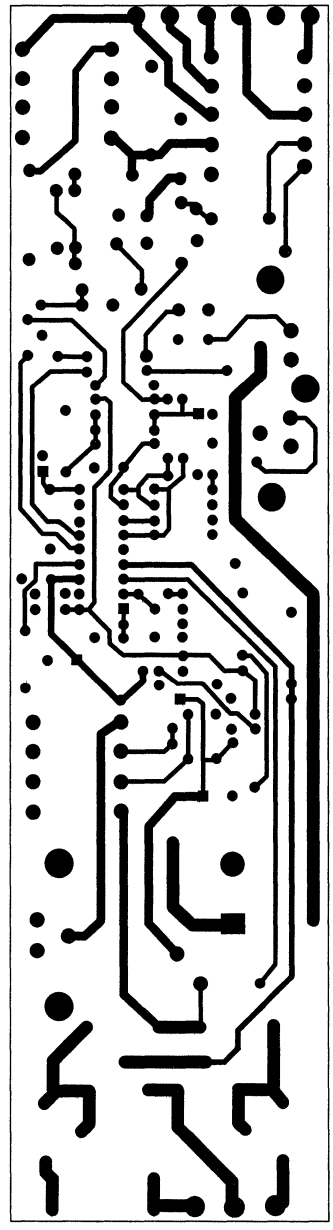


Figure 10. ML4831EVAL Top Trace Layer

12-Bit Plus Sign A/D Converter with PC Compatible Serial Interface

Tom DeLurio

GENERAL DESCRIPTION

The ML2223 12-bit plus sign A/D Converter has an asynchronous serial output designed specifically for the communications port (COM1 or COM2 etc.) of IBM PC-compatible computers. This is the same port used by the mouse or any other external serial port device such as modems and printers. The required data stream format for the COM port is automatically sent by the ML2223.
A basic circuit is shown in Figure 1 and requires few components. A serial interface IC is necessary to boost the logic signals to levels to meet the RS-232 serial-bus standard to drive long cables. The only other devices are an oscillator or crystal, voltage reference (optional) and the interface connector which can be either a 9 pin or 25 pin cable connector. The part has the option to run as slow as 400 baud or as fast as 19200 baud rates (or any intermediate desired baud rate based on standard crystal values) using the internal baud rate generator. Baud rates as high as 600 kbaud are possible with an external clock. This is truly a plug and play device and the data can be captured from the PC COM port through the port's UART to perform remote process monitoring and control as well as for PC digital oscilloscopes or sound recording. This application note describes the hardware and software design and performance of the ML2223EVAL kit from Micro Linear. The methods used can be customized for and system design using the ML2223 12-bit A/D converter

EVALUATION KIT AVAILABLE

The ML2223 evaluation kit is a combination of hardware and software to ease the interface between the PC and device without spending considerable time writing software or prototyping the circuit board. The board contains optional functions to set baud rate, reference voltage and analog multiplexing to allow user customization. The software provided ranges from a simple Assembly/C routine to a sophisticated GUI (Graphical User Interface) that furnishes software control over the hardware and an "oscilloscope" type display of the analog input.

LAYOUT/CIRCUIT DESIGN CONSIDERATIONS

The evaluation board layout is shown in Figure 2. The optional features include an adjustable reference, and analog multiplexer with counter. The reference voltage, MUX and baud rate can all be changed by jumpers on the PC board. The analog inputs are all differential or can be used single-ended if desired. The channel one input is tied to a standard BNC connector where the center signal conductor is connected to the positive input and the ground chassis is tied to the negative input. The other inputs are connected to header pins. The crystal is a

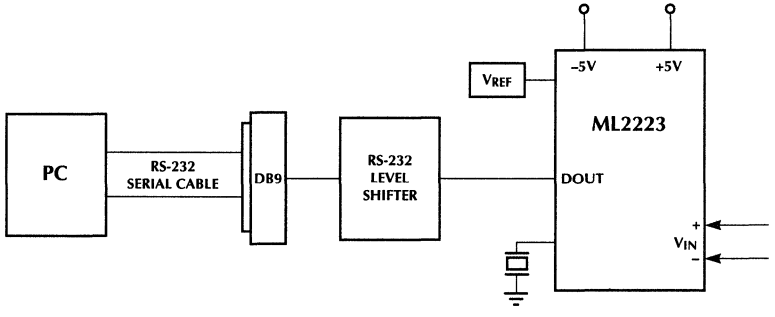
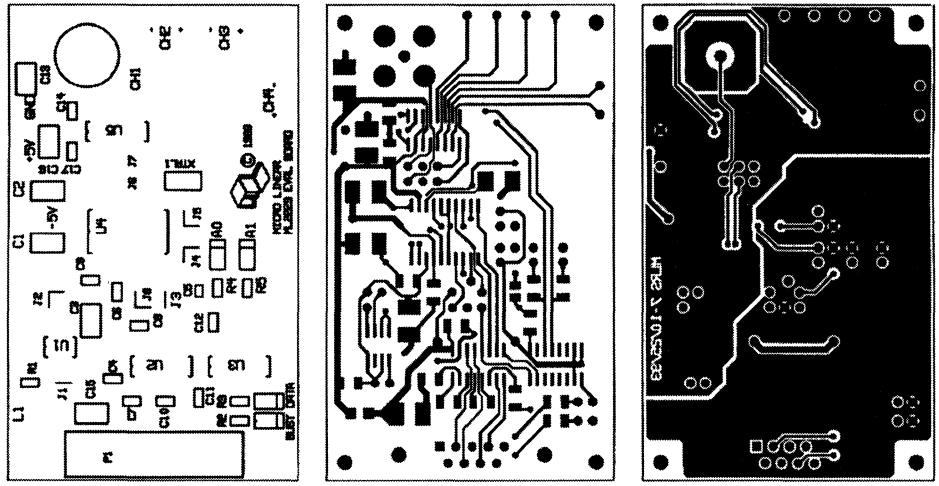


Figure 1. Block diagram of base system. These are the only required parts needed for a simple one channel connection to the PC serial COM port. For cost sensitive applications, the Voltage reference can be excluded and the V_{REF} pin connected directly to V_{CC}. However, this will effect converter accuracy.



Micro Linear can provide a Gerber file of this demonstration board.

Figure 2. Multi-channel demonstration board layout. The board contains optional features and jumpers to allow different baud rates, reference voltages and optional multiplexing inputs. The header pins labelled -5V, +5V and GND near the capacitors C1, C2 and C19 are where the external power supplies are connected.

surface mount ceramic device that oscillates at 2.457MHz. The parts list and Jumper configurations are in Table 1 and 2. The board layout is done with separate analog and digital grounds with rf chokes connected between the analog and digital ground planes and the V_{CC} traces. The chokes attenuate digital switching noise from the sensitive analog part of the board. Numerous power supply decoupling capacitors are used between the V_{CC}, V_{SS} and V_{REF} pins and ground. If cost is an issue, the decoupling caps are not mandatory. The eval board can be used as a test vehicle by systematically removing capacitors until noise becomes a problem in the analog signal and conversion accuracy is affected. Also, the ML2223 has a sample-and-hold input structure with no buffer between the S/H and the outside world. Therefore, the maximum source impedance that can be connected to the V_{IN} pins is 2kΩ. If a larger impedance is used, noise will be injected from the ML2223 to the source and cause inaccurate conversions. This can be alleviated by adding either an active buffer or a passive snubber network. A buffer will solve the impedance problem but may be expensive. The snubber network is a low cost solution consisting of a resistor and capacitor to ground. Typical values for the snubber are a 0.01µF in series with 10 to 50Ω. The snubber provides a path for the noise generated by the S/H.

TABLE 1: ML2223 EVALUATION BOARD PARTS LIST

RESISTORS			
R1	51.1Ohm	5%	1206 package
R2, R3	3.3K	5%	1206 package
R4, R5	470Ohm	5%	1206 package
CAPACITORS			
C1, C2, C15	33µF	6.3V Tantalum	2213 package
C3, C13, C16	15µF	10V Tantalum	2213 package
C4, C7, C10, C11	2.2µF	16V Tantalum	1206 package
C5	0.001µF	50V Ceramic	0805 package
C6, C8, C9, C12, C14, C17	0.1µF	50 V Ceramic	1206 package
CHOKES			
L1, L2	10µH Fair-Rite #2775021447		Surface Mount
CRYSTAL			
XTAL1	2.4577 MHz — Seiko Instruments		SCK2 package — Surface Mount
SEMICONDUCTORS			
U1	LT1431 Precision Reference		S8 package — 8-lead plastic SOIC
U2	LT1381 RS-232 transceiver		S16 package — 16-lead plastic SOIC
U3	74HC161A Presettable Counter		D16 package — 16-lead plastic SOIC
U4	ML2223 Micro Linear 12 bit plus sign A/D converter		S20W package — 20-lead plastic SOIC
U5	Maxim DG409 Dual Channel Analog Multiplexer, ±5V supplies		SE package — 16-lead plastic SOIC
LEDs	MT4093E-UR Marktech International Corp.		
HARDWARE			
P1 Connector	DB9S		Right Angle 9 Pin D-Shell Connector — female
HEADER PINS	2mm		32 Per Board
JUMPER BLOCKS	2mm		8 Per Board
BNC	CBJ22 Trompeter Electronics		4 leg 50 Ohm

TABLE 2: ML2223 EVALUATION BOARD JUMPER LIST. The default settings are shown below.

J1, J2	Both used to set the Reference Voltage	J1= Open and J2 = Closed in Horizontal position — V_{REF} = 2.5V J1= Closed and J2 = Closed in vertical position — V_{REF} = 5.0V (Default)
J3	Reset Pin	The ML2223 can be reset from the PC if J3 is closed. If left open, the device power-on resets only.
J4	Baud Rate divider	J4 = +5V — Rate is 19200 baud J4 = GND — Rate is 9600 baud (Default)
J5	Current or previous data mode (see Figure 3 for explanation)	J5 = +5V — Previous data mode J5 = GND — Current data mode (Default)
J6, J7	Vin+, Vin- Used to bypass the DG409	If J6 and J7 are at the top position toward pin 1 of the DG409, the MX409 multiplexer is bypassed. (Default is bottom position)
J8	Selects SCLK as an input or output	J8 = +5V — Input J8 = GND — Output (Default)
J9	SCLK Pin	If SCLK is an input (J8 = +5V) then an external clock or baud rate generator can control the data rate of the ML2223 output through J9.

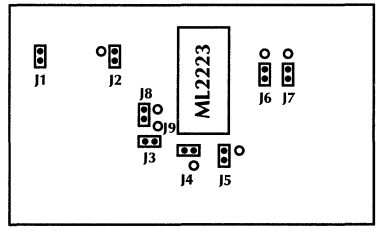


TABLE 3: ML2223 EVALUATION BOARD SOFTWARE LIST

The following is the software included on the disk provided in the Evaluation kit. There are two directories, the "C" directory contains the assembly and C programs and the Labwindo directory contains all the LabWindows™ runtime software. (See below for information on purchasing LabWindows).

README.txt	Text file	Read first for installation instructions
C DIRECTORY		
ML2223.exe	DOS executable file	Type ML2223 to run the software shown in Figure 9
ML2223.asm	Assembly code file	This is the assembly code used to access the 8250 or 16450/550 UART on the PC COM port I/O board. It is linked to the C code using QuickC Qlink ver4.01.
ML2223.c	C code file	The C code for ML2223.exe
Serial.h	Serial port library	This is a include function for the 16550
LABWINDO DIRECTORY		
ML2223AR.exe	Archive file	The Labwindows executable file is included in this self-extracting archive file.
ML2223LW.exe	Runtime LabWindows executable file	Type ML2223LW to run the LabWindows software shown in Figure
ML2223LW.c	LabWindows "C" code file	The LabWindows "C" code for ML2223LW.exe
DJM5.uir	LabWindows User Interface panel	Graphic User Interface panel
DJM5.h	Include Function for UIR	
SG.H	Assembly code Include file	Links the UART assembly code to LabWindows
DJMTONE.h	Sound include function	Button tone generator function
HCSELECT.exe	LabWindows printer file	LabWindows software to set the printer output configuration
ADAPTER.exe	LabWindows video monitor file	LabWindows software to set the video monitor configuration
PKZ204g.exe	Archive shareware program	This is a self-extracting archive program, license info is included.

LabWindows v2.3a
National Instuments, Inc.
6504 Bridge Point Parkway
Austin, Tx 78730-5039
Tel: 1-800-IEEE-488

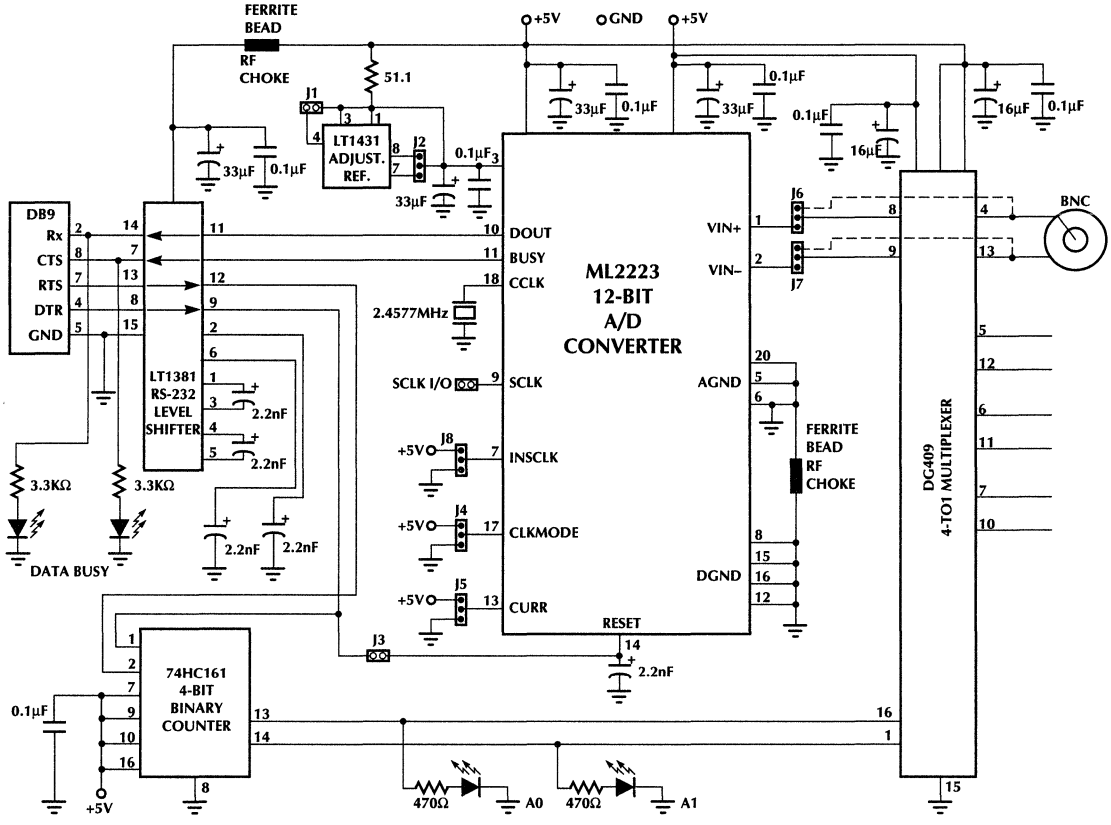


Figure 3. Schematic of eval kit PCB. Shown are all of the components. The jumper connections are shown and also indicated in the PCB layout in Figure 2. Not all of the components are necessary for satisfactory operation. Various decoupling capacitors, the multiplexer and counter can be removed from the board for experimentation.

ML2223 DEVICE PIN DEFINITIONS

CONTROL PINS:

Pin 14 ($\overline{\text{RESET}}$) — Reset Select Pin

$\overline{\text{RESET}}$ = High	ML2223 normal operation
$\overline{\text{RESET}}$ = Low	The ML2223 enters a reset state where the internal clock is stopped. During power on the reset pin must be held low for a period of 10ms for self-calibration. An external capacitor of 10µF tied to ground provides sufficient time for this process. Min. = 6µF.

Pin 17 (CCLKMODE) — Clock Mode Select Pin

CCLKMODE = HIGH	The ML2223's internal clock is equal to CCLK.
CCLKMODE = LOW	The ML2223's internal clock is equal to CCLK/2.

Pin 7 (INSCLK) — SCLK Mode Select Pin

INSCLK = HIGH	SCLK is an input pin and can be driven by an external source or baud rate generator.
INSCLK = LOW	SCLK is an output driven by the ML2223's internal clock.

Pin 13 (CURR) — Current or Previous Data Mode Select Pin

CURR = HIGH	The output data is transmitted at the end of the current conversion.
CURR = LOW	The data from the previous conversion or last conversion is transmitted at the start of the next conversion (one latency period, see figure 5).

CLOCK PINS:

Pin 18 (CCLK) — Internal clock input pin. The clock is generated by an external crystal tied from CCLK to DGND. The clock can also be generated by applying a clock directly to this pin.

Pin 9 (SCLK) — Serial data transmit clock. The serial data is transmitted at the rate of the clock present at this pin. The SCLK can be either internally generated as a function of CCLK or externally driven with a clock signal. When it is internally generated as set by INSCLK = LOW, it is equivalent to CCLK/128 when CCLKMODE = HIGH or CCLK/256 when CCLKMODE = LOW. If INSCLK = HIGH, then SCLK is an input pin and is set externally at the desired baud rate. This is useful if a faster baud rate then 19200 is desired.

FLAG PINS:

Pin 11 (BUSY) — Busy status flag. Normally low and goes high to indicate that a conversion is in progress. When the conversion is complete and data is available at the output pin, BUSY goes low again.

I/O PINS:

Pin 1 (VIN+) — Positive differential analog input. Range = $V_{SS} \le VIN+ \le V_{CC}$ and $|(VIN+)-(VIN-)| \le V_{REF}$.

Pin 2 (VIN–) — Negative differential analog input. Range = $V_{SS} \le VIN+ \le V_{CC}$ and $|(VIN+)-(VIN-)| \le V_{REF}$.

Pin 10 (DO) — Serial Data output. Digital output resulting from the A/D conversion. The serial data is clocked out on the falling edges of SCLK.

POWER SUPPLY PINS:

Pin 19 (V_{CC}) — Positive supply. +5V 5%. Decoupled to AGND.

Pin 3 (V_{REF}) — Voltage Reference Input. V_{SS} to V_{CC}. Referenced to AGND.

Pin 20 (AGND) — Analog ground. 0V. Common mode reference point of the internal differential circuitry.

Pin 4 (V_{SS}) — Negative supply. –5V 5%. Decoupled to AGND.

Pin 8 (DGND) — Digital ground. 0V.

DATA FORMAT AND PERFORMANCE

The output data from the ML2223 is in a two-byte serial format shown in Figure 4. The first byte contains the lower 8-bits of data starting LSB first and the second byte contains bit 9 through 12 with the "sign" bit indicating a positive or negative number. The two bytes are separated by the stop bits and the upper and lower order distinguished by the even or odd parity bits. The assembly code available in the evaluation kit sets up the IBM-PC compatible UART (either the 8250, 16450/550 or equivalent) for all data transmission modes and provides the algorithm to turn the serial data from the ML2223 into an integer from –4096 to +4096. The assembly code is used to read the first byte of data and test for odd or even parity. If odd, it reads the next incoming byte, if even, it stores the value as the first byte and then reads the next byte, tests for odd and stores it as the second byte. The "C" code is linked to the assembly code and provides a user interface which takes the raw number and converts it to voltage or a graphical format.

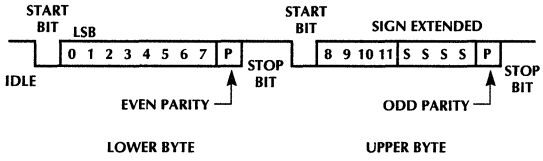


Figure 3. Serial data format sent by the ML2223. There are 8 idle bits between each 24 bit data frame. The start bit indicates the beginning of the first byte.

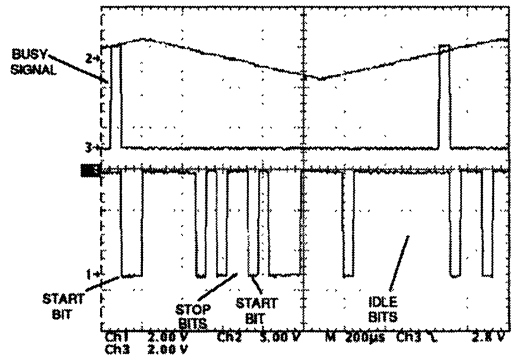


Figure 4. This is an example transmission at 19200 baud. The time between serial transmissions gates the acquisition of the analog signal. The Conversion time is the width of the BUSY signal and the total serial transmission is the time between busy signals. Data Timing

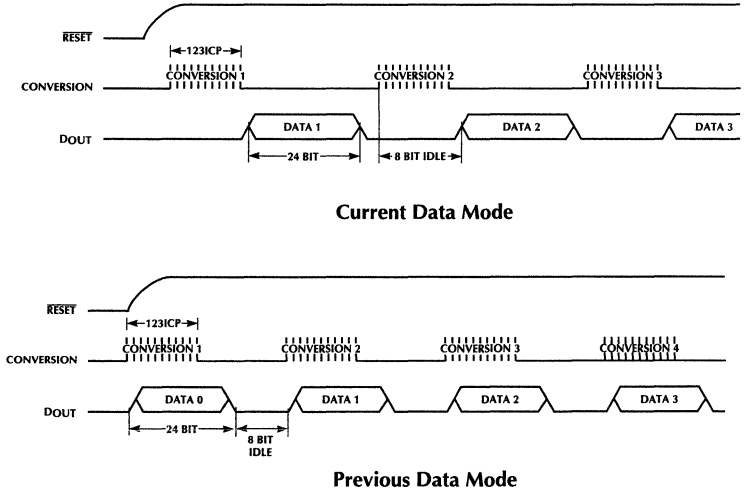


Figure 5. Serial data transmission modes sent by the ML2223. The top waveforms are for the "Current" data mode and the bottom are for "Previous" data mode. (Timing relations are not to scale.) ICP = Internal Clock Periods.

The ML2223 performs continuous conversion in either a "current" or "previous" data mode selected by the CURR pin (Figure 5).

The modes provide data either immediately following the current conversion or at the start of the next conversion. The device requires 123 internal clock periods (timing set by CCLK and CCLKMODE) to convert the analog input signal into digital code. In addition, the converted data is then fully transmitted in 32 "SCLK" clock periods before the next conversion. SCLK is the baud rate generator which sends the serial data to the PC COM port. SCLK can be set internally by the CCLK or can be driven externally based on the condition of the INSCLK pin.

As an example, if an external crystal value of 2.4576MHz is chosen for CCLK, and CCLKMODE is tied high, then the internal clock period is:

$$\text{Internal Clock Period} = \frac{1}{\text{CCLK}} = \frac{1}{2.4576\text{MHz}} = 406\text{ns}$$

Also, INSCLK is tied LOW so SCLK is internally driven. Since CCLKMODE is HIGH, then :

$$\text{SCLK} = \frac{\text{CCLK}}{128} = \frac{2.4576\text{MHz}}{128} = 19200$$

$$\text{SCLK Period} = \frac{1}{\text{SCLK}} = \frac{1}{19200} = 52\mu\text{s}$$

Therefore in this example with CURR set LOW, total conversion and transmission time is:

$$123 \times 406\text{ns} = 0.0499\text{ms}$$

$$32 \times 52\mu\text{s} = +1.66\text{ms}$$

$$1.71\text{ ms}$$

but if CURR is HIGH, total time is:

$$32 \times 52\mu\text{s} = 1.66\text{ms}$$

From this example, it can be seen that although the conversion time is under 50µs, the serial data takes an additional 1.66ms to clock out all 24 data bits plus 8 idle bits at a 19.2 kbaud rate on the serial bus. As an option, the SCLK pin can be switched from an output to and input pin by changing jumper J8 from a low to a high. An external clock can be connected to the header pin at pin 9 and the ground pin on J8 to obtain a faster serial data baud rate for transmission to the PC. If the PC has an 8250 UART, the top speed is 9600 baud, but if a 16450/550 UART is available, the baud rate can be as high as 256 kbaud if the 16550 is on a COM port I/O card with an 8MHz crystal. Also, the RS-232 interface device must be able to run at 256 kbaud. The ML2223 can run up to 600 kbaud by itself, but the limiting factors are the RS-232-to-UART interface and the length of the serial cable.

Operating the ML2223 SCLK at the top 16550 256 kbaud rate speed will provide a total conversion time of 125µs between samples. This is shown in Figure 6.

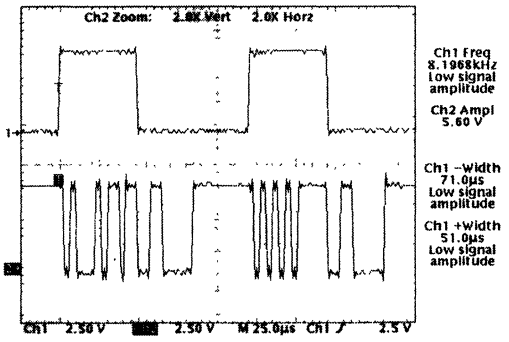


Figure 6. The waveform above shows the ML2223 board with an external 256 kbaud SCLK. The total conversion time from initial signal acquisition to data out is 125µs.

The assembly and "C" code is compiled using Microsoft QuickC Version 2.5. The software flow diagram is shown in Figure 7

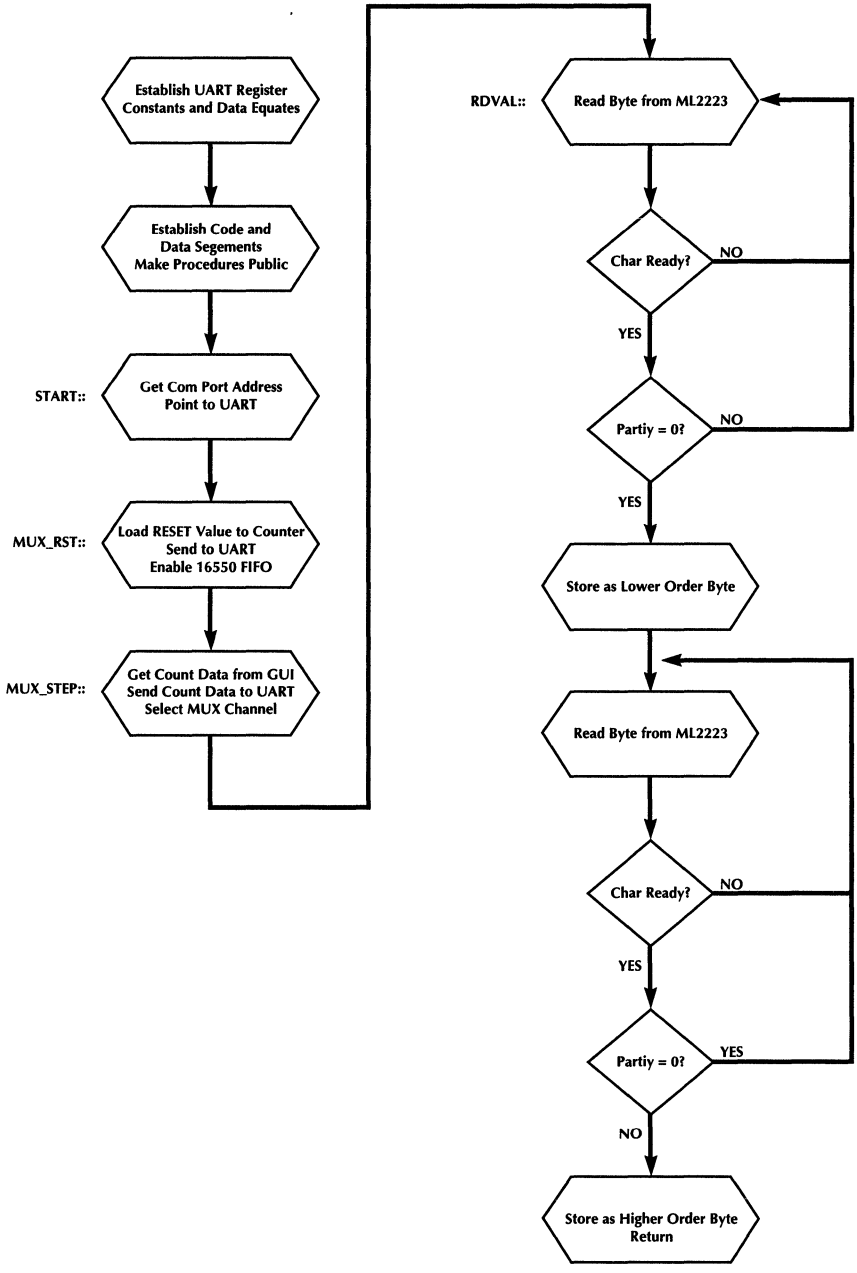


Figure 7. Software Flow diagram for the ML2223.asm assembly code.

.
The following is a listing of the ML2223.asm assembly code routines for the IBM P.C.

```
; ******************************************************
;
; UART register constants
BAL     equ             0       ; baud rate counter lsb.
IER     equ             1       ; interrupt enable reg.
BAH     equ             1       ; baud rate counter msb.
IIR     equ             2       ; interrupt identification reg.
FCR     equ             2       ; fifo control reg(only for 16550 UARTS)
LCR     equ             3       ; line control reg.
MCR     equ             4       ; modem control reg.
LSR     equ             5       ; line status reg
MSR     equ             6       ; modem status reg.
SPAD    equ             7       ; scratch pad reg.
;
; UART bit mask constants
RX_RDY equ              01H     ; receive char flag.
TX_RDY equ              20H     ; xmit buffer empty flag.
INT_MASK        equ             07H     ; interrupt mask value.
RX_ID  equ              04H     ; receive interrupt bit.
MC_INT equ              08H     ; modem control interrupt bit.
MUX_CLK         equ             01H     ; external mux clock bit.
MU_RST equ              02H     ; external mux reset bit.
CTS     equ             10H     ; clear to send bit.
DSR     equ             20H     ; data set ready bit.
DCD     equ             80H     ; data carrier detect bit.
AD_BUSY         equ             20H     ; a/d busy bit.
PAR_ERR         equ             04H     ; parity bit.
PTIME  equ              250d    ; pulse timeout value.
fifospc         equ             0C3H    ;fifo's enabled, trig = 14, dma mode = 0
;
; System clock location
CLOCK  equ              46cH
;
; boolean values
TRUE    equ             1
FALSE   equ             0
;
; data segment
DGROUP group  _DATA
_DATA  segment word public 'DATA'
       assume  ds:DGROUP
;
; all vars are public
;              public   _temp_2,_tout,_temp_1,_base
;
; vars
tout       dw 1         ; timeout value storage.
temp_1     dw 1         ; extra reg 1.
temp_2     dw 1         ; extra reg 2.
base       dw 1         ; comm port base address.
_DATA       ends
; code segment
.MODEL     large
.CODE
SE_TEXT        segment para public 'CODE'
       assume  cs:SE_TEXT
;
; declare procedures public - these procedure names are made available to external "C" code calls
the ;mux_rst procedure sends a signal from the UART to rset the multiplexer counter on the
evaluation ;board.
 PUBLIC_rdval,_mux_rst,_mux_step
;
_mux_rst  proc       far
       push    bp      ; save current values.
       mov     bp,sp   ; set frame.
       push    dx      ; save dx and,
       push    cx      ; cx registers.
```

```
        mov     ax,[bp+6]       ; get base value and,
        mov     dx,ax   ; point to 8250/16550 modem control
        add     dx,4d   ; register address.
        mov     al,2d   ; load mux reset value.
        out     dx,al   ; send to 8250/16550.
        mov     cx,PTIME        ; do a delay for nice output,
c_mux:
        dec     cx      ; pulse width.
        jne     c_mux   ; wait for delay,
        mov     al,0    ; then clear modem bit.
        out     dx,al   ;
        pop     cx      ; restore registers,
        pop     dx      ;
        pop     bp      ;
        ret             ; then back to main routine.
mov      al,fifospc       ;16550 only, fifo enabled and set to 14 bytes
mov      dx,fcr            ;location of fifo register
        out        dx,al
_mux_rst        endp
;
; The next procedure mux_step, gets a value off the stack and increments the multiplexer counter
the number of ;times indicated by the value. this points the MUX to a known channel.  The value
comes from user input.
;
_mux_step proc      far
        push    bp      ; save current values.
        mov     bp,sp   ; set up frame pointer.
        push    dx      ;
        push    bx      ;
        push    ax      ;
        mov     ax,[bp+6]       ; get port address and,
        mov     base,ax         ; put in i/o pointer.
        mov     ax,[bp+8]       ; get total count and,
        mov     bx,ax   ; put count into count reg.
c_mux_it:
        mov     dx,base         ; point to 8250/16550 modem control
        add     dx,MCR ; register address.
        mov     al,MUX_CLK      ; load mux reset value.
        out     dx,al   ; send to 8250/16550.
        mov     cx,PTIME        ; do a delay for nice output,
c_step:
        dec     cx      ; pulse width.
        jne     c_step ; wait for delay.
        mov     al,FALSE        ; then clear modem bit.
        out     dx,al   ;
        mov     cx,PTIME        ; do a delay for nice output,
c_stepper:
        dec     cx      ; pulse width.
        jne     c_stepper       ; wait for delay.
        dec     bx      ; are we done yet ?.
        jne     c_mux_it        ; do till count correct.
        pop     ax      ;
        pop     bx      ;
        pop     dx      ;
        pop     bp      ;
        ret             ; then back to main routine.
_mux_step       endp
;
; The final procedure reads the data from the serial port UART and returns packed word from
ML2223 a/d ;converter.  This is a two-step process.  The data is tested for parity on each
reading, if the parity is even, then ;the data is used as the first byte, if odd, ;the second
byte.  If the data indicates a value of 5000(should not be ;greater then 4096), a timeout is
indicated and an error is sent to the screen.
_rdval    PROC      far
        push    bp
        mov     bp,sp   ; set up frame pointer.
        push    dx
        push    cx
        mov     ax,[bp+6]       ; get comm port number,
```

```
        mov     base,ax         ; and put in base register
        mov     ax,[bx+8]       ; read timeout value.
        mov     tout,ax         ; and store to timeout reg.
try_again:
        mov     ax,tout         ; save timeout value,
        mov     temp_1,ax       ; for later.
        mov     temp_2,ax
        mov     dx,base         ; point to sio base register.
        add     dx,5    ; point to sio stat reg.
rd_char:
        in      al,dx   ; read line status register.
        mov     ch,al   ; save stat.
        and     al,RX_RDY       ; is a char ready ?.
        cmp     al,0    ;
        jne     got_char        ; loop till character.
        dec     temp_1 ; have we looked enough?.
        jnz     rd_char         ; if not continue loop.
        mov     ax,5000d        ; set timeout error flag.
        jmp     rd_char         ; and get back to caller.
got_char:
        mov     al,ch   ; restore stat.
        and     al,PAR_ERR      ; is parity correct ?.
        cmp     al,0    ;
        jne     try_again       ; jump if odd parity.
        mov     dx,base         ; rezero sio pointer.
        in      al,dx   ; read char.
        mov     cl,al   ; store it.
        add     dx,5    ; point to stat reg.
rd_char_2:
        in      al,dx   ; read line status register.
        mov     ch,al   ; save stat.
        and     al,RX_RDY       ; is a char ready ?.
        cmp     al,0    ;
        jne     got_char_2      ; loop till character.
        dec     temp_2
        jnz     rd_char_2
        mov     ax,5000d
        jmp     t_err_out
got_char_2:
        mov     al,ch   ; restore stat.
        and     al,PAR_ERR      ; is parity correct ?.
        cmp     al,0    ;
        je      try_again       ; jump if odd parity.
        mov     dx,base         ; point to sio base reg.
        in      al,dx   ; read char.
        mov     ch,al   ; store it.
me_out:
        mov     ax,cx   ; set for return.
t_err_out:
        pop     cx
        pop     dx
        pop     bp      ; restore registers.
        ret
_rdval          ENDP
SE_TEXT         ends
        end
```

ML2223.C FLOW CHART

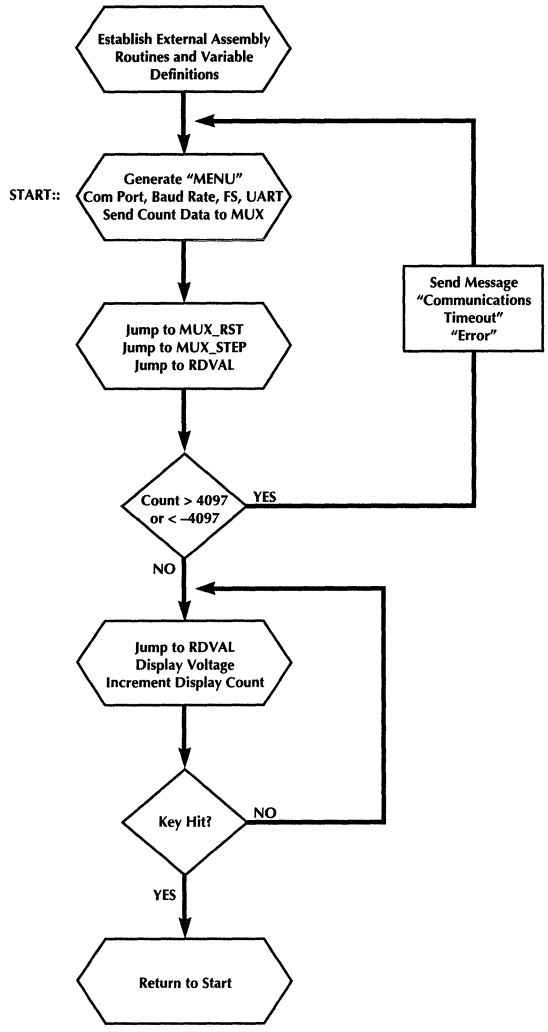


Figure 8. Software Flow diagram for ML2223.C "C" code for the DOS routine.

The ML2223.c "C" software for DOS routines follows:

```
#include <stdio.h>
#include "serial.h"
#define CR      0x0d
#define ENTER   13
#define ESC     27
extern  short     rdval(short,short);
extern  short     mux_rst(short);
extern  short     mux_step(short,short);
void  clrscrn (void);
void  InitDemo (void);
void  ResetTitle (void);
void  MenuTitle (void);
int   GetComPort (void);
int   GetBaud (void);
int   GetFIFO (void);
int   GetDemoInput (int, int);
float GetRange (void);
void  ResetDemo (void);
void  Acquire (int);
short     bdpntr, fifopntr, FSpntr, timeout, x, y, z;
short     base [3];
int       bawd, count, cm, fifoval, i, n;
int       bd [2], byt [2];
char      c;
char      *fifochar [2];
float     j, FSVal;
float     FS [2];
main()
{
  int DoLoop = 0, SelectMe;
  InitDemo ();   /* Initialize Arrays and Variables */
  ResetDemo ();
  while (1 == 1)
  {
    scanf ("%c", c);
    switch (c)
    {
      case '1':
      case '2':
      case '3':
      case '4':
        SelectMe = atoi (c);
        Acquire (SelectMe);
        break;
      case 'c':               /*Test for mux Reset*/
        mux_rst(base[cm]);
        close_port();
        ResetDemo ();
        break;
      case 'q':              /*Test for program end*/
        close_port();
  exit(0);
  break;
    }
  }
}
void ResetTitle (void)        /* Displays menu choices on VGA monitor*/
{
  clrscrn();
  printf ("*** MICRO LINEAR *** ML-2223 DEMO SOFTWARE ***\n\n");
  printf ("COM PORT is set for COM %d \n", cm);
  printf ("COM PORT is set at %ld baud\n", bawd);
  printf ("COM PORT is set at %d data bits\n", get_bits());
  printf ("COM PORT is set for %s parity\n",
          get_parity() == NO_PARITY ?
          "no" : (get_parity() == EVEN_PARITY ? "even" : "odd"));
  printf ("COM PORT is set for %d stop bit\n\n", get_stopbits());
  printf ("FULL SCALE RANGE: %1.2f Volts", FSVal);
}
```

```
void MenuTitle (void)
{
  printf ("<<<< ***** MENU ***** >>>>\n\n");
  printf ("(1) READ VOLTAGE CHANNEL NO.1\n");
  printf ("(2) READ VOLTAGE CHANNEL NO.2\n");
  printf ("(3) READ VOLTAGE CHANNEL NO.3\n");
  printf ("(4) READ VOLTAGE CHANNEL NO.4\n\n");
  printf ("(c) CHANGE COM PORT CONFIGURATION\n");
  printf ("(q) TO QUIT THE PROGRAM\n\n");
}
void clrscrn (void)                 /* clear the screen */
{
  int counter;
  counter = 0;
  while(counter != 255)
  {
    printf("\n");
    counter = counter + 1;
  }
}
int GetComPort (void)
{
  int DoLoop = 0;
  printf (
 " ** COM port: [1] COM1, [2] COM2, [ESC] Quit, [ENTER] Dflt: (COM%d) ",
     cm);
  DoLoop = GetDemoInput (cm, 1);
  printf ("%d\n", DoLoop);
  return DoLoop;
}
int GetBaud (void)
{
  printf (
 " ** Baud Rate: [0] 9600, [1] 19200, [ESC] Quit, [ENTER] Dflt: (%d) ",
     bd[bdpntr]);
  bdpntr = GetDemoInput (bdpntr, 0);
  printf ("%d\n", bd[bdpntr]);
  return bd[bdpntr];
}
int GetFIFO (void)
{
  printf (
    " ** Does computer have a 16550 (FIFO)?: [0] Yes, [1] No.\n");
  printf (
    "                                [ESC] Quit, [ENTER] Dflt: (%s) ",
     fifochar[fifopntr]);
  fifopntr = GetDemoInput (fifopntr, 0);
  printf ("%d\n", fifochar[fifopntr]);
  return byt[fifopntr];
}
float GetRange (void)
{
  printf (
 "Full Scale Range: [0] 2.5, [1] 5.0 [ESC] Quit, [ENTER] Dflt: (%f) ",
      FS[FSpntr]);
  FSpntr = GetDemoInput (FSpntr, 0);
  printf ("%d\n", FS[FSpntr]);
  return FS[FSpntr];
}
int GetDemoInput (EnterVal, PlusThis)
{
  int DoLoop = 5;
  while ((DoLoop != 0) && (DoLoop != 1) && (DoLoop != ENTER))
  {
    scanf ("%d",&DoLoop);
    if (DoLoop == ESC)
    {
      printf ("Quit...\n");
      exit (0);
    }
```

```
  }
  if (DoLoop == ENTER)
    DoLoop = EnterVal;
  return (DoLoop + PlusThis);
}
void UpdateDisplay (void)
{
  int counter = 0;
  float VVal;
  VVal = j*(FSVal/4096);
  printf ("%7.3fV\r",VVal);  /*Calculates voltage*/
  while(counter != count)      /*Slows display update on screen*/
  {
    printf("\r");
    counter += 1;
  }
}
void InitDemo (void)
{
  clrscrn ();
  printf ("*** MICRO LINEAR *** ML-2223 DEMO SOFTWARE SETUP***\n\n");
  base [1] = 0x3f8;
  base [2] = 0x2f8;
  cm = 1;
  bd [0] = 9600;
  bd [1] = 19200;
  bdpntr = 0;
  fifochar [0] = "Yes";
  fifochar [1] = "No";
  fifopntr = 0;
  byt [0] = 14;
  byt [1] = 0;
  FS [0] = 2.5;
  FS [1] = 5.0;
  FSpntr = 0;
  n = 0;
  z = 0;
  count = 2500;
}
void ResetDemo (void)
{
  cm = GetComPort ();
  bawd = GetBaud ();
  fifoval = GetFIFO ();
  FSVal = GetRange ();
  open_port(cm,4096);
  set_baud(bawd);
  fifo (fifoval);
  set_data_format(8,EVEN_PARITY,2);
  ResetTitle();
}
void Acquire (Pntr)
{
  int commerror;
  mux_rst(base[cm]);  /*Set MUX to Channel 1*/
  if (Pntr >= 2)  /*If Channel is not 1, then...*/
    mux_step(base[cm], Pntr - 1);  /*Set Channel to 2, 3, or 4*/
  commerror = 0;
  while ((commerror != 1) && (kbhit () == 0))
  {
    j = rdval(base[cm],timeout); /*Reads data from com port*/
    if (j >= 5000 || j <= -5000) /*Tests for timeout value*/
    {
      printf ("* communications timeout error *\n");
      commerror = 1;
    }
    else
      UpDateDisplay ();
  }
}
```

"C" SOFTWARE

The "C" program for DOS is shown in Figure 9. This is a simple text driven program where the user can select the COM port, baud rate, etc. and see a text readout of the input voltage signal. The screen update rate is the time that the readout is updated on the PC screen and is controlled with the "up" "down" arrows on the keyboard.

```
*** MICRO LINEAR *** ML-2223 DEMO SOFTWARE

COM PORT is set for COM2
COM PORT is set at 19200 baud
COM PORT is set at 8 data bits
COM PORT is set for even parity
COM PORT is set for 2 stop bit
FULL SCALE RANGE: 5.00 Volts

   <<<<***** MENU *****>>>>
(1) READ VOLTAGE CHANNEL NO.1
(2) READ VOLTAGE CHANNEL NO.2
(3) READ VOLTAGE CHANNEL NO.3
(4) READ VOLTAGE CHANNEL NO.4
(c) CHANGE COM PORT CONFIGURATION
(Φ) SLOWER UPDATE (E) FASTER UPDATE
(q) TO QUIT THE PROGRAM

Channel 1: -1.636V        Display Update:500
```

Figure 9. The simple Assembly/C software provides a basic readout of the analog input. Choices for channel selection and readout update rate are provided by screen prompts.

LABWINDOWS SOFTWARE PANEL

The LabWindows software is also written in a subset of "C" code and is linked to the assembly code as in the previous example. However, the "C" code contains specific routines for the LabWindows Graphics User Interface (GUI) shown in Figure 10. The code listing is included but it is only usable by owners of LabWindows. Only the "Runtime" version of LabWindows is permitted for general distribution which means the GUI and "C" code can be used as an executable instrument but not re-compiled. LabWindows is a product from National Instruments. The software controls are listed in Table 3. Some of the screen controls directly update the board by setting the multiplexer input while others are used in conjunction with board jumpers. The "zoom" controls make signal analysis easier as shown in Figure 11.

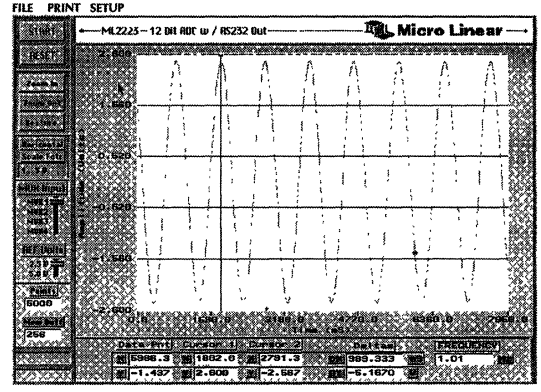


Figure 10. An example screen from the LabWindows RUN-TIME software.

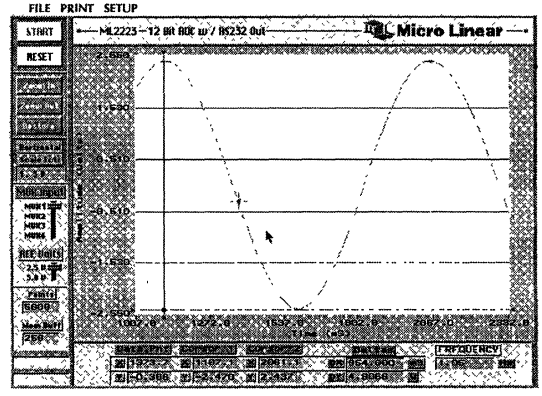


Figure 11. The signal captured in Figure 10 can be magnified with the "Zoom-in" function for further analysis. Up to 5X zoom-in capability is provided with movable cursors for measurements.

TABLE 3: THE SOFTWARE CONTROLS AND DISPLAYS FOR THE LABWINDOWS PANEL.

MENUS	
File	This is a menu button which has two functions that appear when pressed. Quit and Sales Info
Print	Under this menu are two options to either Print the entire panel or just the Graph.
Setup	This menu contains the port information. The options are COM1 or COM2 and the baud rate. Since the PC serial mouse is usually on COM1, COM2 is the default setting. The baud rate default is 19200, the baud rate is controlled by jumpers J4 and J8. J4 sets either 9600 or 19200. If J8 is changed to make SCLK and input (see table 2), and external clock can control the baud rate to use the other options in the menu.
CONTROLS	
Start	This button starts the program. Do not press until all board connections are made.
Reset	Clears all settings, acquired data and the graph.
Zoom in	Automatic scaling and zooming control for the waveform graph. The two moveable cursors with the full screen cross hairs determine the zoom boundaries. Up to 5X zoom is achievable.
Zoom out	Restores the graph to the previous zoom level.
Restore	Restores the graph to the original size.
Horizontal Scale Fctr	This control sets the graph time scale on the horizontal axis to customize for any PC com port.
Sound out	Currently unavailable
Mux Input	Direct software control which will change the mux input at the "Start" of the next reading. This slide control sends control bits to the counter on the board which updates the multiplexer address pins for the appropriate channel.
Ref Volts	This control is used with jumpers J1 and J2 to set the reference and full scale analog input range. If the reference is 2.5V, the analog input can swing from –2.5V to +2.5V. With 5V reference, the input swings –5V to +5V.
Points	Sets the number of data points to graph. The more points, the more displayed data.
Mem buf	Uses the PC DRAM as a memory buffer for slow computers.
DISPLAY INDICATORS	
Graph	The graph displays the calculated points from the –4096 to +4096 data count. The points are connected by straight lines. Each data point can be determined by the cursor with the small cross hairs which "snaps/sticks" to the point. The graph automatically scales the X (time) and Y (voltage) axis.
Data Pnt	The X (time) and Y (voltage) is displayed for the point the small cursor is "snapped" too.
Cursor 1	One of the zoom-in limits, these can also be used to make delta-type measurements
Cursor 2	The other zoom-in limit.
Deltas	The delta measurement from cursor 1 to cursor 2.
Frequency	The delta X (time) measurement converted to frequency

ML65244, ML65245 and ML65541 Ultra Fast Octal Buffer/Transceiver Family

INTRODUCTION

In the design of VLSI circuits and digital systems, the term buffer refers to a circuit's ability to drive load capacitance significantly larger than its own input capacitance. In integrated circuit design it often happens that a single gate (inverter) has to drive a large fanout which implies a large capacitance. Typical examples of large on-chip loads are internal busses, clock signals and control signals like the system reset, etc. These loads are typically of the order of 20pF to 100pF which is 1000 times more than a standard on-chip gate. The propagation delay of a signal through a CMOS inverter is directly proportional to the load capacitance. Hence a VLSI chip output stage driving one of the above loads would take 1000 times longer than the minimum gate delay if the device sizes are kept minimum. Increasing the sizes of the output device in VLSI chip does not help since the input capacitance of the larger devices will load the previous logic stage. Hence buffer circuits need to be placed between the VLSI gate and the load capacitance.

Extending this to the design of complex, high speed digital subsystems, similar situations arise where a large capacitive load needs to be driven. Typical examples of large off-chip loads are address and data busses. Because of the increasing complexity and number of pins on these chips, on-board drive capability cannot be provided for reasons of power dissipation and chip size. Hence buffer chips are needed to drive the large loads associated with main memory and cache memory designs. Buffer chips provide this drive capability at the expense of additional propagation delay. At these levels every nanosecond counts; and the propagation delay through the buffer becomes significant in determining the access time of the memory. The faster the buffer, the smaller the pressure on the memory access times. Hence, faster buffers can translate to significant cost savings.

Conventional digital CMOS buffers are implemented as multiple inverter stages. This presents a limitation on the fastest propagation delay that can be achieved for typical loads. In fact the fastest CMOS digital buffer available today (the FCT family) has a propagation delay of 3.2ns. This article discusses the design of a buffer using an analog approach rather than the conventional digital inverter approach. This results in a propagation delay of 1.5ns, and thus provides a significant advantage and relief to high speed digital sub-system designers.

BUFFER DESIGN BASICS

In the design of VLSI chips, single inverter based buffers are commonly used to drive a load capacitance C_L, which is n times larger than the input capacitance C_i of the inverter. A single inverter buffer is inserted between the logic gate and the load capacitance. Figure 1 shows the architecture of a single inverter buffer. The PMOS and NMOS transistors of the second gate are k times wider then those of the first, assuming the ratio between PMOS and NMOS is identical for both gates. Assuming the propagation delay of a minimal sized gate connected to a single minimal sized inverter is t_{pdo}, the total propagation delay of the inverter chain in figure 1 is given by :

$$t_{pd} = k \times t_{pdo} + \frac{n}{k} \times t_{pdo} = \left(k + \frac{n}{k}\right) \times tpdo$$

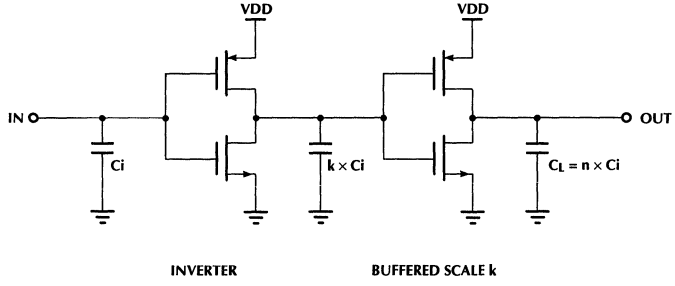


Figure 1. Single Buffer Architecture.

The first inverter is slowed down due to the k times larger load, while the second inverter benefits from the k times larger transistor scale-up to drive the larger load C_L. Setting the derivative of the propagation delay equation to zero, the optimal value of k is $\sqrt{n}$, derived by setting dt_{pd}/dk to zero and the optimal propagation delay for the circuit in figure 1 is $2 \times \sqrt{n} \times t_{pdo}$. Comparing the delay of a single inverter driving C_L versus a single inverter plus buffer, it is clear that inserting a buffer makes sense only when n > 4, which denotes an equivalent fanout of four gates.

CMOS BUFFER DESIGN — DIGITAL APPROACH

Conventionally in digital systems design, off-chip loads are very large. Hence buffer chips for driving these large capacitive loads are required. These have been conventionally implemented in CMOS using a chain of inverters, as shown in figure 2. The MOSFETS in each inverter stage are scaled up linearly with respect to the previous stage so that each inverter drives a progressively larger load. An optimal design is obtained by scaling up all stages with a constant factor k. This results in an identical delay per stage given by $t_{pd\ STAGE} = k \times t_{pdo}$. To achieve the same delay for the last stage, it is necessary

that $t_{pd} = k \times t_{pdo} + \frac{n}{k} \times t_{pdo} = \left(k + \frac{n}{k}\right) \times tpdo.$

Thus the propagation delay is given by $t_{pd} = n \times k \times t_{pdo}$ or substituting the expression for n,

$$t_{pd} = t_{pdo} \times I_N(x) \times \frac{k}{I_N(k)}.$$

Setting the derivative of this expression to zero, the optimal value of k is e and the optimal propagation delay is given by :

$$t_{pd(OPT)} = e \times I_N(x) \times t_{pd} = e \times I_N\left(\frac{C_L}{C_i}\right) \times t_{pdo}$$

Thus in order to buffer large capacitance with CMOS logic, it is necessary to cascade an even number of inverters, with each successive inverter being larger than the preceding one, eventually leading to an inverter that will drive the required load capacitance, at the required frequency. However, when doing this, the minimum propagation that can be achieved is proportional to the minimum gate delay of the process.

As an example, if the ratio of output to input load capacitance were 1000 then the propagation delay would be 1000 times that of the process' minimum gate delay in the case of an unbuffered approach, 63 times that of the process' minimum gate delay in the case of a single inverter approach and 19 times that of the process' minimum gate delay in the case of the multiple inverter buffer approach. It is easy to conclude that there is a real but process limited reduction in delay obtained with multiple inverter based buffers when driving very large capacitive loads. Each inverter stage represents an additional delay in the gating process because in order for a single gate to switch, the input must slew more than half of the supply voltage. Today the fastest available CMOS buffer (a member of the FCT-E logic family), has managed to drive a 50pF load with a propagation delay of 3.2ns.

HIGH SPEED BUFFER DESIGN — ANALOG APPROACH

Octal buffers are eight bit logic devices that are capable of driving load capacitance several times larger than their input capacitance. As discussed in the above section, these buffers are typically implemented in CMOS logic (digital approach) and made to be TTL compatible by sizing the input devices appropriately. By using an unique analog circuit approach that does not require cascaded logic gates, we at Micro Linear have produced an octal transceiver (ML65245), which offers a propagation delay of less than 1.5ns, while switching at 50MHz, into a 50pF load. It achieves its low and predictable propagation delay by using feedback techniques to produce an output that follows the input within a couple of hundred milli-volts. If the output voltage is not close to the input, then the feedback will source enough current to the load capacitance to correct the discrepancy.

The basic architecture of this analog approach is shown in figure 3. It is implemented in a 1.5µ BiCMOS process with all the active devices being NPNs — the fastest devices available in this process. In this circuit there are two paths to the output. Assume for the moment that the switches shown in figure 3 are closed. One path sources current to the load capacitance when the signal is asserted and the other path sinks current from the output when the signal is negated. The assertion path is the emitter follower path consisting of the level shift transistor Q1, the output transistor Q2 and the bias resistor R8. It sources current to

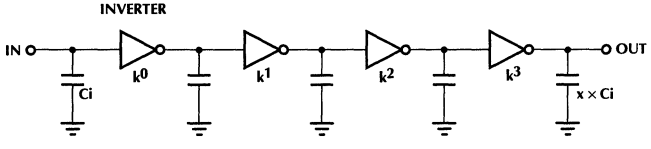


Figure 2. Multiple Inverter Buffer Architecture

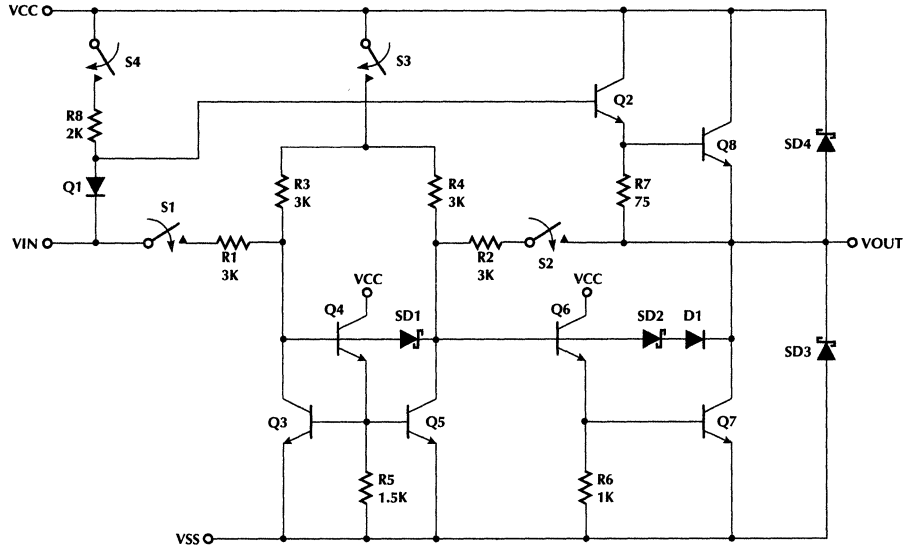


Figure 3. Analog Buffer Architecture.

the output through the 75 ohm resistor R7 which is bypassed by Q8 during fast input transients. The negation path is a current differencing amplifier connected in a follower configuration. The active components in this amplifier are transistors Q3-Q7. R3-R6 are bias resistors and R1 & R2 are feedback resistors. The key to understanding the operation of the current differencing amplifier is realizing that the current in transistors Q3 and Q5 are the same at all times and that the voltages at the bases of Q4 and Q6 are roughly the same. If the output is higher than the input, then an error current will flow through R2. This error current will flow into the base of Q6 and be multiplied by beta2 to the collector of Q7, thus closing the loop. The larger the discrepancy between the output and the input, the larger the feedback current and the harder Q7 sinks current from the load capacitor.

A number of MOSFETS have been used to tri-state outputs and minimize power in disabled buffers. The function of some of these MOSFETS have been included in figure 3 in the form of switches. S1 and S2 ensure that the buffers are tristated when they are open; S3 and S4 ensure that disabled buffers draw no current from V_{CC}. Other switches not shown in the diagram are used to pull the bases of Q4, Q6 and Q2 to ground when the buffer is disabled.

Also shown in the diagram are some diodes that are used as clamps. Two schottky diodes connected to the output SD3 and SD4 protect the output voltage from sustained excursions above and below ground. These also double as the electrostatic discharge protection for both the inputs and outputs of buffers since they are connected back to back in the layout. SD1 keeps the base of Q6 from going to ground. This helps the negation circuit to recover more quickly when the signal is asserted. SD2 and D1 are used as output clamps. They keep the output transistor Q7 from saturating. If Q7 was allowed to saturate, its base would draw lots of current from V_{CC}, and its recovery characteristics would be poor because of the excess charge that would be stored in its base.

The analog circuit implementation of a buffer/transceiver results in a number of advantages. The output rise and fall times closely match those of the input waveform while the output responds almost immediately to the input, with very low skew. Also oscillatory ground bounce is significantly reduced with this approach, as compared to CMOS transceivers, due to the bipolar output structure which damps the output ringing. Another advantage is that the resistor R7 in figure 3 acts like a termination resistor in some cases. This 75Ω resistor is in series with the output and therefore helps suppress noise caused by transmission line effects such as reflections from mismatched impedances.

PERFORMANCE CHARACTERISTICS

The analog buffer circuit approach discussed above has been fabricated in silicon as the ML65245 and proven to be successful. To verify the 1.5ns propagation delay through the part, a special printed circuit board was laid out and the buffer was made to drive different load capacitance at different frequencies. Figure 4 shows the input and output waveforms of the buffer driving a single 50pF capacitance at 33MHz. In all buffering applications, some degradation with load capacitance is to be expected. When driving larger load capacitance, the buffer must supply more current to the load in order to maintain a given output slew rate. In Micro Linear's analog buffer, the amount of current that can be supplied to the load is limited by the characteristics of the output NPNs. As the current in these transistors increases, their current gains tend to decrease and the amount of base current available is limited by the bias resistors on the chip. However, on the ML65245, peak currents to the load capacitance can exceed 150mA. The degradation of the ML65245 with capacitance is shown in figure 5. This data was taken with one line switching at 15MHz.

Also of interest are the input output characteristics of the ML65245. Since CMOS transceivers are gauged only by their output characteristics, the analog architecture we have chosen is unique. Its output characteristics depend on the difference between the input and the output. The output voltage and input current versus input voltage are shown in figure 6. Notice that the output is clamped for inputs less than approximately 0.3 volts and greater than V_{CC} minus 0.7. Also note that the input draws no current when the input voltage is about 3 volts. This means that unlike a CMOS buffer in which the output voltage cannot be determined when the input is allowed to float, the output of the ML65245 has no undetermined state. The output voltage versus output current characteristics of the

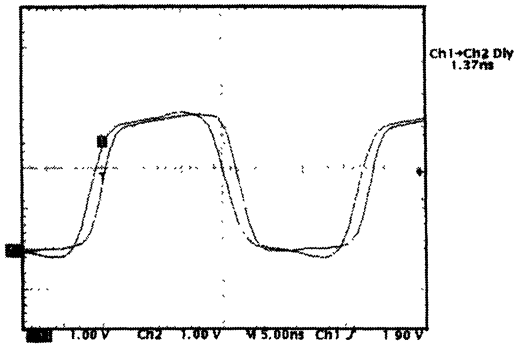


Figure 4. Typical Output Waveform.

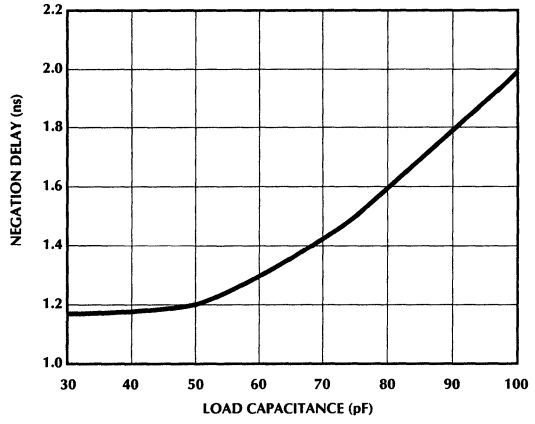


Figure 5. Propagation Delay versus Load Capacitance

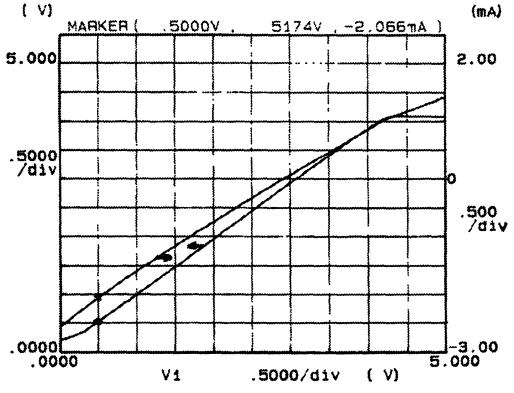


Figure 6. L_{IN} and V_{OUT} vs. V_{IN}.

ML65245 are also important. These are shown in figure 7a. In this case, the input voltage was fixed at two volts and the output current was swept from –50mA to 50mA. In a CMOS buffer application, the system designer would expect that these characteristics would be the same for any input voltage that caused the output to be high. However, in this case that would be wrong, because in the ML65245 the bias and feedback currents available to the output transistors in both paths depend on the input voltage, and the output voltage is clamped slightly above ground and slightly below V_{CC}. Figures 7b and 7c show V_{OH} vs. I_{OH}. In both cases, the outputs can sink or source more than 200mA.

Another interesting performance advantage comes from the fact that the output devices are bipolar and not CMOS. NPN bipolar devices are fabricated to carry current in one direction; from the collector to the emitter. They will carry current in the opposite direction, but the current gain will be dramatically worse. CMOS devices are symmetric with respect to the gate. When a CMOS gate is "on", it will conduct current equally well from the drain to the source or from the source to the drain. This dramatically affects the operation of the buffer during signal assertion when a capacitor with some initial condition is made to discharge to ground through the lead inductance of the output bond wire, the output device, and the lead inductance of the ground bond wire. Since the CMOS device carries current equally well in both directions, The output tends to oscillate at the L, C, resonant frequency when it reaches ground. In the ML65245, the output does not tend to oscillate since after the initial undershoot, the resistance of the output device becomes much greater than the resistance during the initial discharge of the load capacitor. This is illustrated in figure 8.

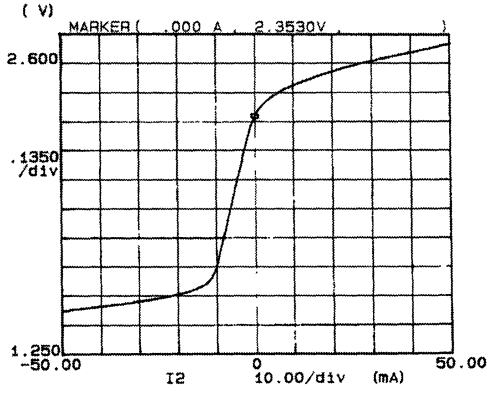


Figure 7a. V_{OUT} vs. I_{OUT}.

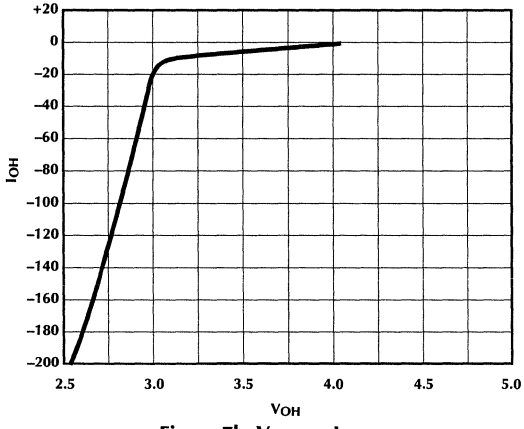


Figure 7b. V_{OH} vs. I_{OH}.

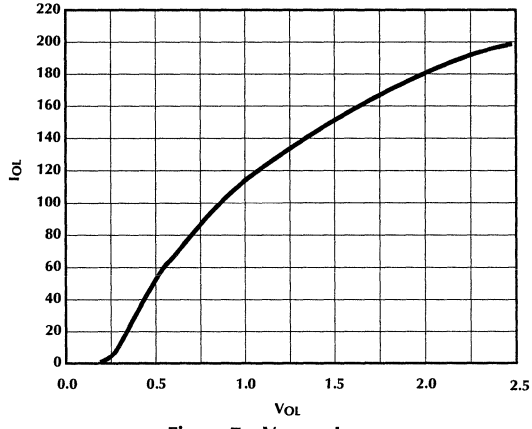
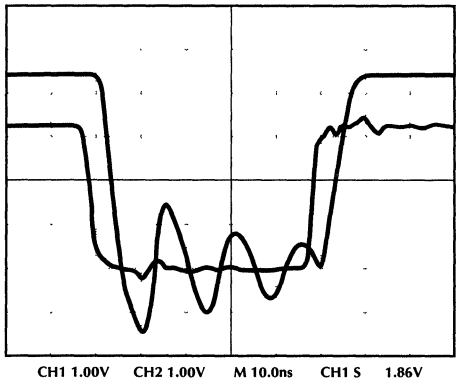
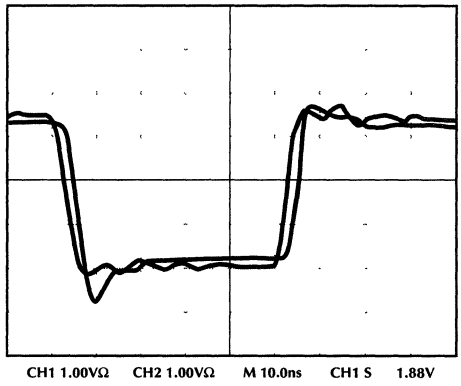


Figure 7c. V_{OL} vs. I_{OL}.



(a) FCT Buffer



(b) ML65245 Buffer

Figure 8. Buffer Output Switching with Four Typical Loads.

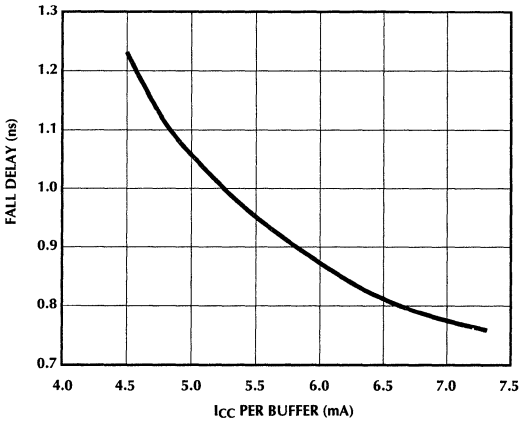


Figure 9. Negation Delay vs. I_{CC}

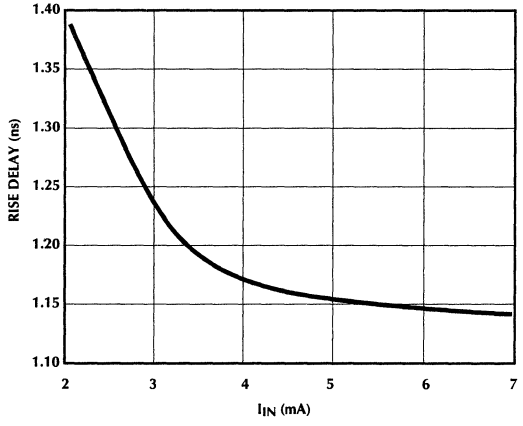


Figure 10. Assertion Delay versus I_{IN}.

Figures 8 (a) and (b) were both obtained using identical test jigs. Four outputs were made to switch loads of 50pF at 1MHz. The only difference was the part used. It is easy to see that there is a significant threat of double clocking using the CMOS part because after the initial transition, the ringing in figure 8 (a) comes back up to the TTL threshold.

LIMITATIONS OF THE ANALOG APPROACH

The limitations of this analog approach to digital transceiver design can be broken down into two questions. First, what limits the performance of the existing circuit design?; and second, what impact does this have on digital systems design?. What ultimately limits the performance of the analog buffer as a circuit is the process it was fabricated on. The goal of this circuit is to minimize propagation delay. Since there are two paths from the input to the output, the propagation delay can be broken down into assertion and negation delays. The speed limitation is a matter of charging and discharging internal capacitances with a given amount of idle current. Various bias currents in the buffer have a great impact on the propagation delay. Referring to the figure 3, the values of R1 through R4 determine the bias current in the current differencing amplifier that makes up the negation path. Decreasing these resistors speeds up that amplifier at the expense of power consumption. Negation delay versus I_{CC} is shown in figure 9. Similarly, the assertion path is largely dependent on the quiescent output current and the bias resistor R8. Decreasing this resistor decreases the assertion delay at the expense of input bias current. This relationship is shown in figure 10.

Another limitation of the analog buffer is that other digital functions are not readily adaptable to this scheme. The ML65245 performs the function V_{OUT} equals V_{IN}. In order to create an analog inverter, one would have to implement the function V_{OUT} equals V_{OH} minus V_{IN}. In order to implement this function with an amplifier, some additional information is needed. The chip would have to have a pin for the user to input the voltage V_{OH}. Hence, industry standard pin out could not be used. Another limitation along these lines is that latched buffers would be difficult without additional delay since there is no logic level comparison being made in the existing buffer. Because of this, the Micro Linear family of buffers consists of only three products — the ML65245 (octal transceiver), the ML65244 (FCT244 compatible octal buffer), and the ML65541 (FCT541 compatible octal buffer).

In addition to the limitations of the buffer as a circuit, there are issues that the systems designer should be aware of when using this type of buffer in his system. First, since the buffer is analog, it conforms to the analog function $V_{OUT} = V_{IN}$. For example if V_{IN} is 1.5 volts, that is where the output will want to be. If the system designer inputs a waveform that has overshoot, undershoot, ringing, and glitches, the output will have all of these to the extent that its bandwidth and large signal response can reproduce them. This may have a negative impact on the digital system in which the buffer is operating. However, it is difficult to say whether the effect will be greater using the ML65245 than it would be if a standard CMOS buffer were exposed to the same input glitches. Hence, such glitches should always be avoided in the overall system design.

THE ANALOG ADVANTAGE

Because its output follows its input, the Ultra Fast Buffer (UFB) series has several advantages over conventional logic buffers.

- It is FAST, 1.5ns delay at 50pF load. The linear amplifier imposes a small delay, and the rest of the delay is due to driving the capacitive load.
- Because it is very fast and because there is a well defined, stable linear amplifier delay from input to output, skew between outputs is very low, typically 0.25ns or less for matched output loading.
- Because the output is well controlled as the input ground bounce is exceptionally low, (less than 400mV, typical) even at 1.5ns propagation delay. This removes a significant worry item from your design list.
- The resistor in the output damps reflections and noise from other parts of the system, also helping to keep down system noise.
- It is inherently 3.3 volt compatible. The output follows the input. If the input swings between 0 and 3.3 volts, the output will swing between 0 and 3.3 volts.

SYSTEM APPLICATIONS

There are a wide variety of existing and future needs for high speed buffer/transceiver, especially in the main memory and cache memory designs of very high speed processor systems like Pentium™, PowerPC™, MIPs R4000™, Sparc™, etc. If the digital system designer can save several nanoseconds by using a higher speed buffer, then she has the option of maintaining system performance by using a cheaper memory or increasing system performance without spending more for a faster memory.

BUFFERING MAIN MEMORY

An example of a main memory application for the Intel PCI chipset with the Pentium™ processor is shown in figure 11. This discussion is only intended as a general reference. For details please refer to the appropriate Intel documentation. This system has a 66MHz host processor and a 33MHz main (DRAM) memory bus. The main memory row and column addresses (RAS & CAS) and write enable (WE) signals are provided by the PCMC chip (PCI Cache and Memory Controller). The DRAM SIMMs inputs present a heavy load to the PCMC and must be buffered. Three buffered copies of the address signals and write enable are required to drive the six row array. Using the ML65245 to buffer these signals gives the system designer extra margin to be able to use memory modules slower than the normally required 50/70ns modules. The burst read (page-hit) performance is typically 7-4-4-4 at 66MHz for 70ns DRAMs or 6-3-3-3 at 66MHz for 50ns DRAMs. This usually translates to significantly higher costs. With the speed improvement offered by the ML65245, a 6-3-3-3 burst with 60ns DRAMs may be achievable. This kind of main memory application for the ML65245 could potentially extend to other kinds of processor systems which do not require latched buffering.

Figure 12 shows a main memory design example with the ML65245 for the MIPs R4X00 RISC processor based system without secondary cache. As shown in the figure the ML65245 could be used as a data I/O transceiver or as an address buffer. The faster propagation delay essentially translates to a faster main memory access which allows for cost savings by using slower CDRAMs or DRAMs.

BUFFERING CACHE MEMORY

With the advent of higher power operating systems like Windows NT, NeXTStep, Cairo, etc, RISC processor designs like MIPs R4000 series are gaining momentum. In these systems the interface to secondary cache is a critical path in the address and bus control pins. Referring to figure 13, any propagation delay saved in the buffer translates to a slower SRAM access requirement. Consider a CPU design where the secondary cache bus operates at 75MHz. Table 1 examines the timing allocations for each step of the cache RAM t_{AA}.

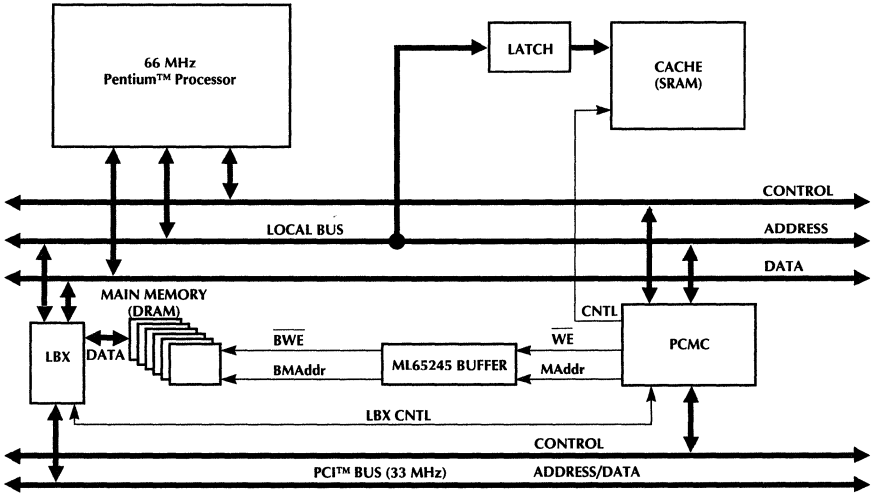


Figure 11. Main Memory Buffering for a Pentium System.

TABLE 1: TIMING ALLOCATIONS FOR CACHE RAM

	TWO CYCLES	CLK TO ADDR	BUFFER t_{pd}	DERATING	CPU SETUP	t_{AA}
FCT-E	26.5ns	–7ns	–3.5ns	–3ns	–3ns	10ns
ML65245	26.5ns	–7ns	–1.5ns	–3ns	–3ns	12ns

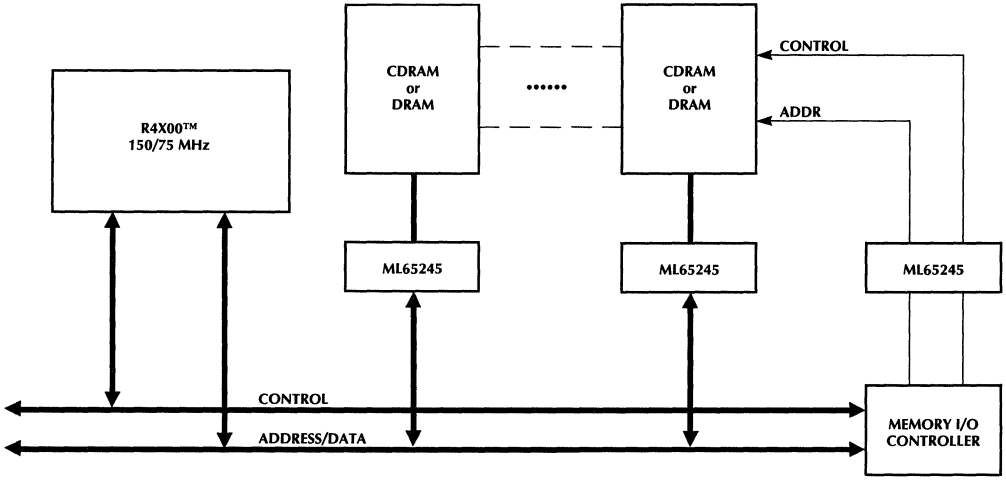


Figure 12. Main Memory Buffering for Non-cache MIPs R4000 System.

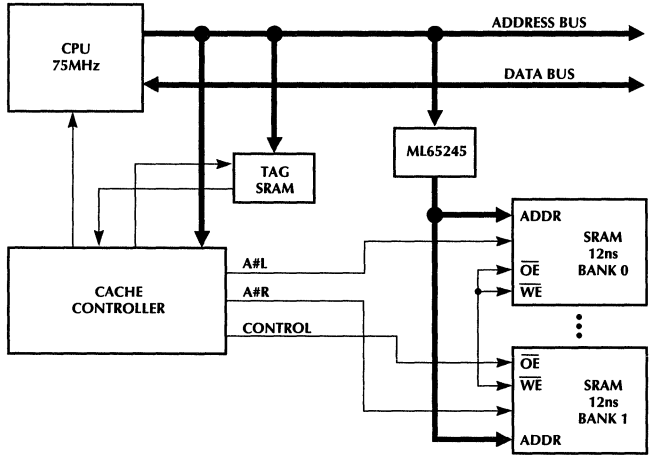


Figure 13. Cache Memory Buffering for a 75MHz CPU System with a Latched Address Bus.

Based on the above calculations, for a zero-wait-state cache performance, with minimal board space utilization, it is clear that with the fastest FCT buffer, 10ns SRAMs would be required for the cache memory, while with the ML65245 high speed buffer one could use 12ns SRAMs. This difference becomes even more significant in higher speed (100 + MHz) systems where the cache access times could be on the order of 6ns to 8ns. This access time difference could very well mean the difference between using expensive BiCMOS SRAMs versus less expensive CMOS SRAMs.

EXAMPLE COST ANALYSIS OF A R4000 SECONDARY CACHE MODULE BLOCK DESIGN

Shown below in figure 14 is a 256KB secondary cache module block for the R4000 family of RISC processors. It is built on a multilayer epoxy laminate substrate using eleven 16K x 4 SRAMs and two 74FBT2827 buffer/drivers. Generally four identical cache module blocks compromise a full secondary cache in a R4000 based 50MHz/75MHz, zero-wait state system. Table 2 shows a comparative cost analysis of building this cache module using the 74FBT2827 (which have a propagation delay of 4.0ns) versus using the ML65245 (which has a propagation delay of 1.5ns). The SRAM access time t_{AA} is the Cache Module speed minus Buffer t_{pd}. For purposes of this analysis it is assumed that the cost of the two buffers are more or less the same and the SRAM cost is based on distributor prices. This is just intended to show the relative order of savings, rather than the absolute value.

Hence it is clear that the high speed ML65245 results in significant cost savings through the use of slower SRAMs, as shown.

A SYNCHRONOUS DRAM MODULE

High performance computer systems with 66MHz and faster buses are starting to use synchronous DRAMs. These DRAMs are clock driven and have registered inputs and outputs. A typical 1 meg by 32 synchronous DRAM module would use 18 synchronous 1 meg by 4 DRAMs. This means each DRAM address line has 18 capacitive loads. The address and control pins for these 18 DRAMs must be buffered to keep this loading from the CPU, particularly because a system uses up to four modules.

Buffering the address and control lines for a synchronous DRAM module at 66MHz is not easy, as we can see from examining typical timing numbers. Assuming the address arrives at the module at 8ns after the rising edge of the clock and that the DRAM has a 3ns clock setup time., this leaves us only 15 + (8 + 3) = 4ns for buffering. If we do not make the 4ns speed, we must add a wait state with its performance degradation. We could use a conventional 74FCT244D at 3.8ns delay, but this would leave us with only 0.2ns margin, not counting flight delay on the module at 0.25ns per inch. If we use a ML65244 at 1.5ns, we have 2.5ns margin for flight delay and design margin.

TABLE 2: COMPARATIVE COST ANALYSIS

MODULE t_{AA}	SRAM t_{AA} W/ 2827 BUFFER	SRAM COST W/ 2827 BUFFER	SRAM t_{AA} W/ ML65245 BUFFER	SRAM COST W/ ML65245 BUFFER	COST SAVINGS W/ THE ML65245	SAVINGS PER PART
12ns	10.5ns	—	8ns	$1,562	$00	—
15ns	13.5ns	$1,562	11ns	$1,177	$385	$130
17ns	15.5ns	$1,177	13ns	$858	$319	$106
20ns	18.5ns	$858	16ns	$330	$528	$176
25ns	23.5ns	$275	21ns	$275	—	—

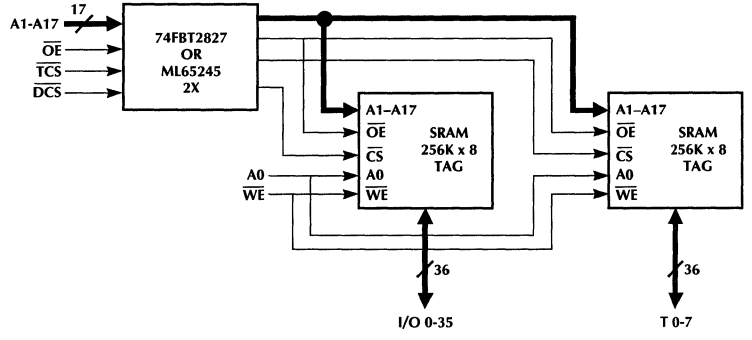


Figure 14. R4000 Secondary Cache Module Block Diagram.

THE UFB IN HIGH SPEED BUS DESIGNS

The UFB solves many difficult timing problems in high speed bus designs. Let us examine high speed memory subsystems to identify these problems. The block diagram of figure 15 shows a CPU with fast SRAM memory subsystem. The SRAM memory subsystem could be the main memory for high speed DSP processor such as the 320CX0, or it could be the external cache for a 386, 486, Pentium or other high speed RISC or CISC CPU.

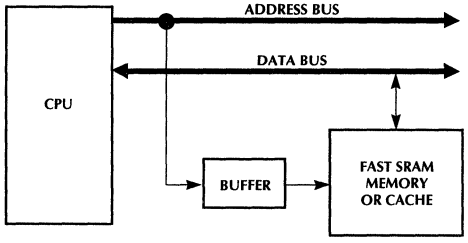


Figure 15. CPU Memory System Block Diagram.

In this block diagram, the address lines to the SRAMs are driven by a buffer. This buffer reduces the capacitive load on the CPU address bus. This is usually necessary if the SRAM system has 8 or more chips, because otherwise the capacitive loading of the SRAMs would significantly slow down the address bus for the whole system.

Figure 16 shows a general timing diagram for a CPU memory read data transfer. This timing diagram is common to 386, 486 and Pentium CPUs, and also applies to other CPUs such as the 320C30 DSP CPU and many RISC processors using different signal names. The timing diagram shows a single read data transfer. This could also be the first word of a multi-word burst data transfer.

The CPU generates the memory address after a delay of t_{ADDR} from from the start of the cycle. t_{ADDR} is usually about half a clock period. The address buffer adds a delay of t_{BUFFER} to the address signals. The SRAM adds a read access delay, t_{AA}. Finally, there is the data setup time required by the CPU, t_{DS}. An additional time for printed circuit trace delay called flight time (not shown), must be added. This delay, t_{TRACE}, represents the finite propagation delay of electrical signals along the printed circuit board traces. The sum of all these delays must be less than the time available, which is two clock periods in this case. The design timing margin, t_{MARG}, represents this excess time.

A good timing margin might be 5% of the time available. As CPU and bus speeds increase, this timing margin is harder to achieve. Table 3 illustrates this problem by showing hypothetical timing margins for x86 processors from 386 to Pentium.

The timing margin for the 386 system using 7ns buffer is generous. The speed of the memory subsystem is determined primarily by the 386 CPU in this case. In the 486 case, the propagation delays of the buffer and the traces are starting to become significant, but are still manageable. In the Pentium case, the propagation delay of the buffer becomes critical. If 12ns SRAMs are used, the timing margin becomes negative: you didn't make it in time. Using ultra fast buffers, however, converts this negative margin to a positive one.

If 12ns SRAMs are used, the timing margin becomes negative: you didn't make it in time. Using an ultra fast buffer, however, converts this negative margin to a positive one.

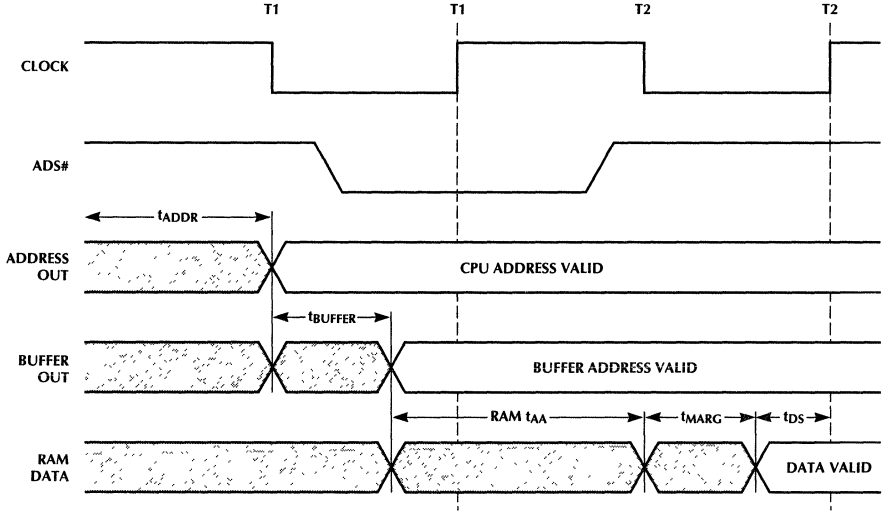


Figure 16. Memory Data Transfer Timing Diagram.

TABLE 3: DESIGN MARGIN FOR X86 CPU MEMORY SUBSYSTEMS

PARAMETER	386	486	PENTIUM	PENTIUM + UFB	UNITS
CPU Clock	16	33	66	66	MHz
Clock Cycle Time	62.5	30	15	15	ns
Total Time (2 Cycles)	125	60	30	30	ns
t_{ADDR}	40	16	10	10	ns
t_{BUFFER}	7	5	3.8	1.5	ns
t_{TRACE}	3	2	1.5	1.5	ns
SRAM t_{AA}	35	25	12	12	ns
CPU t_{DS}	10	5	3.8	3.8	ns
Total	95	53	31.1	28.8	ns
Margin, t_{MARG}	30	7	–1.1	+1.2	ns
Timing Margin, Percent	24%	11.7%	–3.6%	+4.0%	ns

Another way to view the significance of buffer delay is as a percentage of the bus clock period for various bus speeds, as shown in Table 4 This table shows that the 74FCT244D delay becomes more than 10% of the bus clock cycle time above 25 MHz. The ML65244 delay just reaches 10% at 66MHz. Even at 100MHz, the ML65244 delay is still only 15% of the bus clock cycle time.

Table 4: Buffer Delay versus Clock Period

BUS CLOCK FREQ. MHz	BUS CLOCK PERIOD ns	FCT244D % AT 3.8ns	ML65244 % AT 1.5ns
10	100	3.8	1.5
20	50	5.6	3.0
25	40	9.5	3.8
33	30	12.7	5.0
40	25	15.2	6.0
50	20	19.0	7.5
66	15	25.3	10.0
80	12.5	30.4	12.0
100	10	38.0	15.0

CACHE DESIGN: THE VALUE OF SPEED

Many systems need to re-power the address lines to the cache memory to drive the memory address capacitance. If you use a conventional high speed logic buffer such as the 74FCT244D, this usually means adding a wait state to the cache access time to compensate for the buffer delay. This degrades cache performance. L2 caches for 486 and Pentium systems use four word lines. This is typical of most other CISC and RISC CPU's. Using a ML65244 can save you from having to add this wait state.

A zero wait state design will transfer four words from the L2 cache to the CPU on a cache miss. This will take 5 clock cycles for minimum, zero wait state timing, also called 2111 timing. A one wait state design will require 6 clock cycles, or 3111 timing. The speed degradation versus wait states for four word line caches is shown in Table 5. Note that a single wait state degrades the CPU effective clock speed from 90MHz to 75MHz.

Table 5: Cache Speed versus Wait States

WAIT STATES	TIMING	SPEED	CPU CLOCK MHz	NET CLOCK MHz
0	2111	100%	90	66
1	3111	83%	75	55
2	4111	71%	64	47
3	5111	63%	56	41

There is some argument today that adding one wait state to an L2 cache does not seriously degrade speed. This is an argument from necessity because in most designs you have to add a wait state because you have no fast buffer to save you the necessary time. To the degree that you need an L2 cache, to that same degree, you need it fast. Adding a wait state causes a 17% speed reduction if your software is heavily using the L2 cache. This is a real problem if you are paying extra money for a fast CPU, only to lose your performance gain in the L2 cache timing.

The degradation in system speed shown in Table 3 assumes that the L2 cache performance limits CPU performance. This is a reasonable assumption, and becomes more reasonable with time. L2 cache use depends on the CPU L1 cache miss rate. The L1 cache miss rate depends on CPU internal speed and program statistics. As CPU internal speeds rise, the L1 cache miss frequency in misses per second will rise as well, for a given program. For example, a 100MHz Pentium with a 1.5:1 clock multiplier will generate caches misses at 1.5 times the rate of a 66MHz CPU. For a constant 66MHz bus speed, this means that the L2 cache will be accessed 1.5 times more often. Also, the more efficient you make the CPU internally, the more the L2 cache determines your performance.

A PENTIUM™ CACHE EXAMPLE

The 66MHz PentiumTM CPU uses an L2 cache. A zero wait state L2 cache has 2111 timing, achieving zero wait usually requires 66MHz burst mode SRAMs. The UFB allows you to make a 2111, zero wait state L2 cache using 12 nanosecond 32k x 8 asynchronous SRAMs.

When the L1 cache in the CPU misses, the CPU gets a four word burst of data from the L2 cache. The first cycle of a four word burst read is the critical cycle for timing. Figure 17 shows a timing diagram for this cycle. The timing margin, tMARG, must be positive, and is calculated in Table 6.

In the first clock period, T1, the CPU puts the address on the bus and asserts ADS#. For zero wait states, the L2 cache returns the first word of data at the end of T2. This two cycle first access corresponds to the 2 in the 2111 timing. The remaining three words come out on each successive clock cycle.

The address sequencing for the four words is unusual but well suited to L2 cache design. The second word has the same address as the first but with the least significant bit inverted. The third word has the same address as the first with the second least significant bit inverted, and the third address is the same as the first with both least significant bits inverted.

Figure 18 shows a block diagram of the Pentium L2 cache design. This design uses two banks of 32k x 8 SRAMs, for a 512 KByte cache.

The cache works by running the two banks in overlap. Both banks access during the first T2 cycle, T2a, and the cache control logic enables the output of bank 0 or 1 depending on the state of the least significant bit of the address. The CPU supplies the address for both banks through the ML65245's.

Figure 19 shows a timing diagram of the four word burst sequence. At the end of T2a, the CPU clocks in the data from the first bank. The cache controller turns off the first bank output enable and turns on the second bank's output enable. The second bank supplies the second word of data at the end of the second T2 cycle, T2b.

Also at the end of T2a, the cache control logic clocks the address from the CPU into both FCT374's. The second least significant bit of the address is inverted as it is clocked into the 374's. This is the correct address for 3 and 4 of the four word burst. the four word burst.

After clocking the address into the 374's, the cache control logic turns off 245's for the first bank and turns on its 374's. This starts the first bank accessing the third word of the burst, to be put on the bus in T2d. The first bank has two cycles of time to get ready for T2c. The second bank switches from its 245's at the end of T2b, in the same manner as the first bank, and it generates its word of data for T2d.

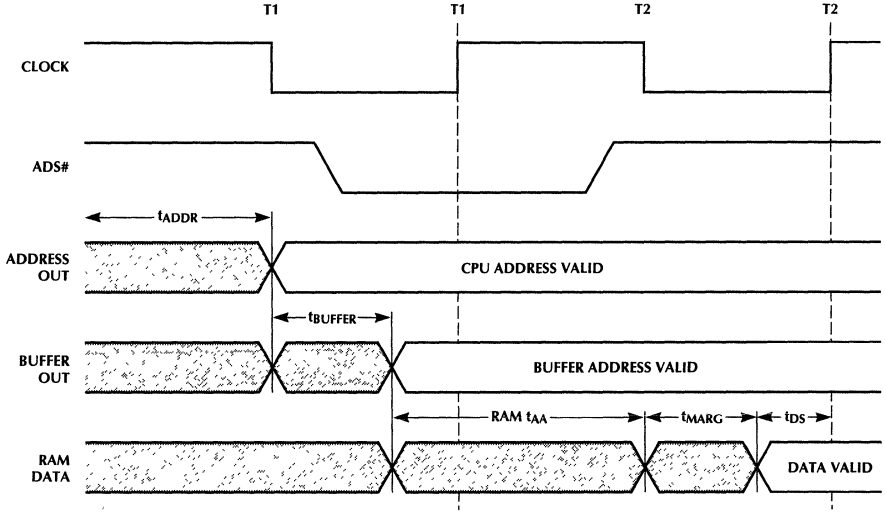


Figure 17. Pentium™ First L2 Cycle Timing Diagram.

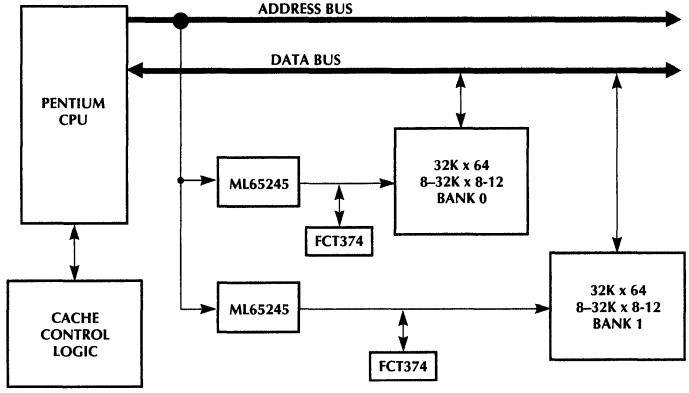


Figure 18. Pentium L2 Cache Block Diagram.

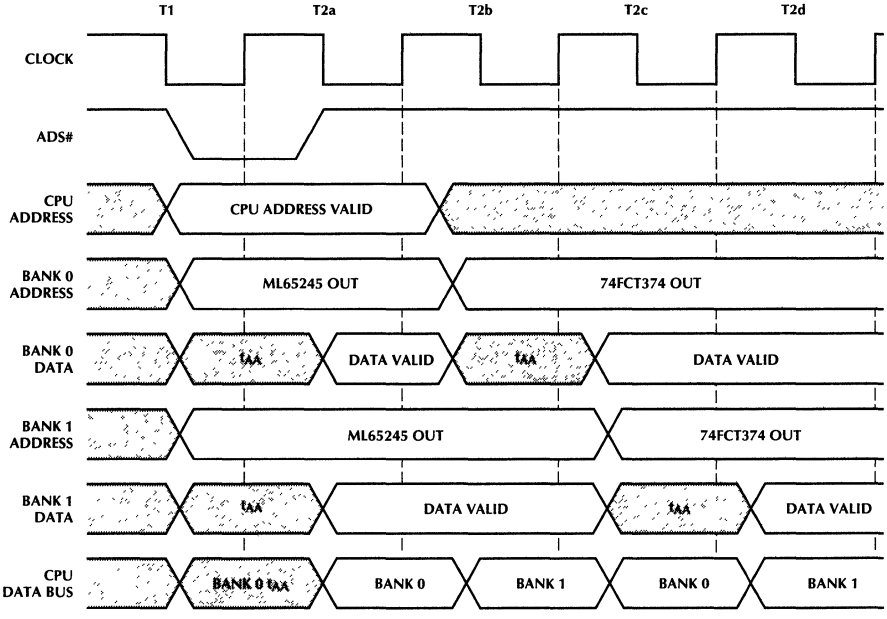


Figure 19. L2 Cache Burst Timing Diagram.

Table 6: Timing Margin for L2 Cache

SOURCE	VALUE, ns
Availabe Time: 2 clocks	+30
CPU Clock to Output	–8.0
CPU Loading Delay	–2.0
ML65245 Delay	–1.5
Trace Delay	–1.5
SRAM Access Delay	–12
CPU Data Setup Tome	–3.8
Total Delays	–28.8
Margin, t_{MARG}	+1.2

Although this design is suggestive rather than complete, it serves to indicate the possibilities of these devices. They allow you to consider designs that would otherwise be impossible, such as a zero wait state, 2111 cache for the Pentium using plain 32K x 8 SRAMs.

OTHER APPLICATIONS

The UFB can save 2.3 nanoseconds or more in bus designs. This feature strongly recommends the UFB to many designs where saving this time can mean performance improvement and design margin. Below is a list of just a few of these possible applications.

- DRAM Module Address Buffers
- Cache Module Address Buffers
- Big cache address buffers: 1 + MByte
- CPU Data Bus Transceivers
- PCI Bus Address/Data Buffers
- DSP: Address buffer for large SRAM
- ATE: probe buffers, pin drivers

Micro Linear

Application Brief 1

How to Set the Sensitivity of the ML4621, ML4622, ML4624

SECTION 1

HOW TO ADJUST THE SENSITIVITY OF THE ML4622/ML4624:

The sensitivity of ML462X is adjustable by changing the voltage level at V_{THADJ} pin. The sensitivity should be set at a point which guarantees error free operation with minimum signal level and the maximum noise level on the quantizer inputs. The first step is to determine the input threshold at which errors begin to occur. To determine this the following steps are recommended.

1) Tie V_{THADJ} to ground on the receiving station to find the maximum sensitivity.

2) Transmit *10^9 bits of data from transmitting station and verify that receiving station receives all the bits without any error.

3) If receiving station does not receive the data correctly, go to step 4). Otherwise measure the received power and attenuate the receive signal more. Then go to step 2.

4) At this point you know the maximum sensitivity of the receiving station before it receives any error. The minimum level must be at least –32.5dBM average to meet 10BASE-FL standard or –27dBM peak to meet FOIRL standard. Now you can set the sensitivity of the receiving station to any level you want as long as it is greater than the maximum sensitivity and less than minimum sensitivity (when $V_{THADJ} = V_{REF}$) of the ML4622/ML4624. The Link Mon signal will then turn off (high) before receiving any errors.

5) Now you should determined the proper voltage at V_{THADJ} which will meet 10BASE-FL standard with minimum signal level and the maximum noise level.

A) Signal Level: The responsivity of the HFBR2416 can be as low as 4.5mV/μW and as high as 11.5mV/μW. So we calculate minimum $V_{IN(P-P)}$ at the input of the quantizer when receive power is –29.5dBM peak.

R_P (MV/UW) = Responsivity of the HFBR2416

P_R (dBM) = Average receive power

$V_{IN(P-P)}$ = Input peak to peak voltage at the input of ML4622, ML4624

–29.5dB = 1.122μW

$V_{IN(P-P)}$ = 1.122μW X 4.5mV/μW

$V_{IN(P-P)}$ = 5.049mV (0)

Thus V_{THADJ} for the minimum signal level can be calculated as follow:

V_{THADJ} = 500 $V_{IN(P-P)}$ (IN mV)

V_{THADJ} = 500 (5.049) = 2.52V (1)

B) Noise Level: The maximum random noise ($V_{N(MAX)}$) of the HFBR2416 is 0.7mV which it occurs at a responsivity of R_P = 8.2mV/μW. This input signal will be attenuated by the internal low pass filter of the quantizer. If capacitor across CF1 and CF2 is 5pF, the attenuated noise voltage will be:

f = 1/2π800 (C+4) = 22.1MHZ

(ML4622/ML4624)

$$N=\left(\sqrt{\frac{22.1MHZ}{125MHZ}}\right)(.7mV)=.294mV_{P-P}$$

As shown in figure 1, the signal to noise ratio required at the fiber optic receivers comparator is:

S/N @ BER of 1 x 10^{-10} = 12.8 (FOIRL)

S/N @ BER of 1 x 10^{-9} = 12 (10BASE-FL)

We can calculate the signal level at the input of the quantizer.

S = $V_{IN(P-P)}$

$V_{IN(P-P)}$ = (12.8)(.294) = 3.76mV(P–P) (FOIRL)

$V_{IN(P-P)}$ = (12)(.294) = 3.52mV(P–P)

(10BASE-FL)

The link monitor threshold of the ML4622/24 should be set to reject the output voltage of the HFBR2416 when it is 3.52mV_{P-P} for the 10BASE-FL or 3.76mV_{P-P} for the FOIRL. The V_{THADJ} for this signal level can be calculated as follows:

V_{THADJ} = 500 (4.74) = 2.37V (ML4622)

V_{THADJ} = 417 (4.74) = 1.97V (ML4624) (2)

Setting the V_{THADJ} at 2.5V (tie to V_{REF}) will set the input threshold greater than the maximum noise level of both specifications. This will allow the quantizer to reject the worst case noise levels and meet both specifications for minimum signal level of 5.049mV_{P-P}.

*10^9 bits to meet 10BASE-FL standard and 10^{10} bits to meet FOIRL standard.

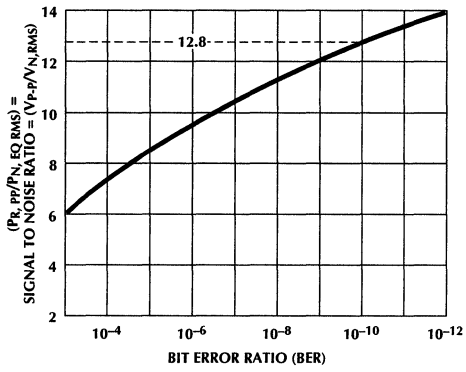


Figure 1.

SECTION 2

HOW TO SET V_{THADJ} FOR GREATER SENSITIVITY:

Lower voltage at V_{THADJ} gives you more sensitivity. By adding a resistor divider as shown in Figure 2 you can lower the voltage at V_{THADJ} to have sensitivity more than –29.5dBM peak. You can calculate the resistors' value as follow:

— Find the V_{THADJ} for the sensitivity you want at the input of the ML4622/ML4624.

$V_{THADJ} = 500\ V_{IN(P-P)}$

$V_{THADJ} = V_{REF}\ (R1/R1 + R2)$

$V_{REF} = 2.5V$

$V_{THADJ} = 2.5V\ (R1/R1 + R2)$ (3)

— Set R1 = 1k and solve EQU. 3 for R2.

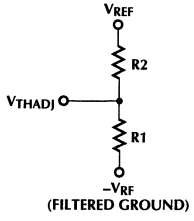


Figure 2.

SECTION 3

HOW TO SET V_{THADJ} IN THE ML4621 TO MEET 10BASE-FL STANDARD:

To determined proper voltage at V_{THADJ} we must calculate V_{THADJ} for the minimum signal level and the maximum noise level.

A) Signal Level: As we calculated in Section 1, the signal at the input of the ML4621 can be as low as 5.049mV peak to peak. Thus, V_{THADJ} for the ML4621 can be calculated as follow:

$V_{THADJ} = 0.7V + 600\ V_{IN(PEAK)}$ (IN mV)

$V_{THADJ} = 0.7V + 600\ (5.049/2)$

$V_{THADJ} = 2.21V$

B) Noise Level: As explained in section 1, we can calculate the input signal level at the ML4621 for the maximum random noise level of .7mV as follow:

$f = 1/2\pi 425C = 37.4MHZ$

(C=10pF across CF1 & CF2)

$$N=\left(\sqrt{\frac{37.4MHZ}{125MHZ}}\right)(.7mV)=.382mV_{P-P}$$

$V_{IN(P-P)} = (12.8)(.382) = 4.88mV_{P-P}$ (FOIRL)

$V_{IN(P-P)} = (12)(.382) = 4.58mV_{P-P}$ (10BASE-FL)

Since $V_{IN(P-P)}$ is less than 5.49mV (10BASE-FL requirement), we can set the V_{THADJ} to 2.21V by using a resistor divider from V_{REF}. The resistors can be calculated as follow:

$V_{THADJ} = V_{REF}\ (R1/R1+R2)$

$2.21V = 2.5V\ (R1/R1+R2)$ (4)

Choose R1 = 1K and solve equation 4 for R2.

$2.21 = 2.5V\ (1000/1000+R2)$

$R2 = 140\Omega$

Micro Linear

Application Brief 2

ML4632 Versus A Voltage Driven Output

INTRODUCTION

This Application Brief covers one of the issues which must be considered to meet IEEE 802.5, IEEE 802.4 and IEEE 802.3 FOIRL and 10BASE-FL. The Optical Power at the output of the LED transmitter (Launched Power) can violate these standards. One way to improve this parameter is to use a current source to drive a Fiber Optic LED transmitter.

ML4661/ML4662, FOIRL and 10BASE-FL transceivers, are the best solution for 802.3 applications (refer to Application Note 15). However if ML4661/ML4662 is not being used in a 802.3 application, ML4632 is the second option to be used.

On the other hand ML4632 can be used for the IEEE 802.4 and IEEE 802.5 (4Mbps) applications.

ANALYSIS

ML4632 is a Fiber Optic LED driver with a programmable current driven output. This will allow user to program the output current with the accuracy of ±10% through a resistor. The ML4632 can be used to drive a Fiber Optic LED transmitter like HP LED transmitter (HFBR1414). The ML4632 regulates the current through the HFBR1414 regardless of power supply variations or variations in V_F between LED transmitters. This will result in a more precise launch power at the output of the transmitter. However if a voltage driven output is used such as CMOS or Schotky gates, the variation in forward voltage (V_F) with forward current (I_F) and the power supply variation must be taken into account. These variations cause a wider range of Launched Power which will violate the standards.

LAUNCHED POWER

Table 1 shows the HFBR1414 Peak Launched Power measured out of 1m of cable and table 2 indicates Launched Power range for the FOIRL and 10 BASE-FL Standards.

TABLE 1

PARAMETERS	PEAK LAUNCHED POWER (dBM) MIN	TYP	MAX	CONDITIONS T_A(°C)	I_F
62.5/125µm Fiber Cable NA = 0.275	–15	–12	–10	25	60mA
	–16		–9	–40 to +85	
	–15.5		–10.5	25	55mA
	–16.5		–9.5	–40 to +85	

TABLE 2

802.3	PEAK LAUNCHED POWER (dBM) MIN	MAX
FOIRL	–18	–9
10BASE-FL	–17	–9

Note: Peak launch power = Average launch power +3dBM

Table 3 shows the Launch Power if ML4632 is used to drive HFBR1414. We choose 55mA as forward current to meet the HFBR1414's current condition.

TABLE 3

CONDITION	I_F	$P_{T(55mA)}$ (Note 1) MIN	MAX	$P_{T(IF)}$ (Note 2) MIN	MAX	P_R (dBM) (Note3)
High	60mA	–16.5	–9.5	–16.2	–9.2	+0.3
Nominal	55mA	–15.5	–10.5	–15.5	–9.5	0.0
Low	50mA	–16.5	–9.5	–16.9	–9.9	–0.4

Note 1: $P_{T(55mA)}$: Optical Power of the HFBR1414 when I_F is 60mA.
Note 2: $P_{T(IF)}$: Optical Power of the HFBR1414 for I_F = 55mA ±10%.
Note 3: P_R: is relative power ratio in dBM ($P_{T(IF)} - P_{T(55)}$).

Table 4 shows the Launched Power if a voltage source is used to drive the HFBR1414. To calculate I_F at high and low end, we can calculate the resistor value at nominal condition:

$R = (V_{CC} - V_F)/I_F$

$R = V_R/I_F$

$R = (5 - 1.7)/60mA = 55\Omega$

So I_F can be calculated for the low and high conditions.

CONCLUSION

Due to the HFBR1414's Optical Power range, Using a voltage source as the LED driver can violate the FOIRL and 10 BASE-FL standards. However using the ML4632 to drive the HFBR1414 meets both standards in the worst condition.

TABLE 4

CONDITION	V_F (V)	V_{CC} (V)	V_R (V)	I_F (mA)	$P_{T(60mA)}$ (Note 1)		$P_{T(IF)}$ (Note 2)		P_R(dBM)
					MIN	MAX	MIN	MAX	(Note3)
High	1.48	5.5	4.02	73.1	–16	–9	–15.2	**–8.2**	+0.8
Nominal	1.7	5.0	3.3	60	–15	–10	–15	–10	0.0
Low	2.09	4.5	2.41	43.8	–16	–10	**–17.8**	–11.8	–1.8

Note 1: $P_{T(60mA)}$: Optical Power of the HFBR1414 when I_F is 60mA.
Note 2: $P_{T(IF)}$: Optical Power of the HFBR1414 for different I_F.
Note 3: P_R. is relative power ratio in dBM ($P_{T(IF)} - P_{T(60)}$).

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