MEMOREX

1377 Display Station
Theory of Operations Manual

1377.21-00

Publication Number 1377.21-00

March 1979 edition

The information in this publication is subject to periodic revisions and to updates by Publications Bulletins. A bulletin is identified as Publication Number 1377.21-00XX, where "XX" equals "01" for the first bulletin released.

To request copies of this publication or any bulletin, send a Supplies Requisition (form number 7020) using the publication number to: Memorex Corporation, Marketing Distribution Center, San Tomas at Central Expressway, Santa Clara, California 95052.

A readers' comments form is provided at the back of this publication. If the form has been removed, please send comments to Memorex Corporation, Department 6313, M/S 14-32, San Tomas at Central Expressway, Santa Clara, California 95052.

PREFACE

This manual provides a detailed logic description of the Memorex 1377 Display Station. In connection with the logic diagrams, it is designed to enable the FE to make repairs to the 1377 PCB by replacing board components.

TABLE OF CONTENTS

BLANK PAGE

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The Memorex 1377 Display Station is a buffered alphanumeric display terminal used to enter data into or retrieve data from an IBM System/3, System/360, or System/370 computer. The 1377 is attached to the computer via a local control unit (IBM 3272 or equivalent) or via a remote control unit (IBM 3271 or equivalent). Connection to the control unit (CU) is by means of a 93-ohm coax cable (RG62/U or equivalent). Up to 32 terminals may be connected to each CU. Each terminal requires a separate coax cable (which can be up to 2000 feet long).

All 1377 logic is contained on a single PCB which is mounted beneath the keyboard. Power (+5, +12, -12 VDC) is supplied from a power supply housed in the monitor. All analog circuitry for the monitor is housed on a PCB in the monitor.

A block diagram of the 1377 showing control and data paths between major functional blocks is shown in Figure 1-1. Each of these functional blocks is described in the following paragraphs.

1.2 BUFFER

The buffer in the 1377 consists of a dynamic random access memory capable of storing 4096 ten-bit words; however, only 2000 words are used since the display consists of 25 lines of 80 characters. The first 24 lines are data which can be entered from the keyboard, received from the CU, or transmitted to the CU. The 25th line is reserved to display machine status and is not accessible to the user for data entry or display. The 10-bit word consists of 8 data bits, a parity bit, and a cursor bit. Data may be written into the buffer from the coax interface or from the MPU. Data may be read out of the buffer by the coax interface, the MPU, or the CRT display circuitry.

1.3 MICROPROCESSOR

A 6800 microprocessor (MPU) is used to handle keyboard input, perform editing operations, and generate most of the status information that is sent to the CU. Several peripheral chips are used to support the MPU. A 128-byte static RAM chip is used for temporary storage by the MPU. Two peripheral interface adapter (PIA) chips allow interfacing non-bus-oriented logic signals to the MPU. Three 2708 EPROM's (which store 1024 bytes each) are used to store the software which controls operation of the MPU. (Two of these EPROM's will be replaced by a 2048-byte ROM in future machines.)

1.4 COAX INTERFACE

The coax interface logic interfaces the coax I/O line to the MPU and to the buffer. It serializes or deserializes each word to or from the coax, decodes commands sent by the CU, and controls DMA operation between the coax and the buffer.

1.5 CRT DISPLAY

The CRT display circuitry reads data out of the buffer and converts it to video so that it can be displayed on a raster-scan type of CRT monitor. Since the persistence of the CRT phosphor is relatively short, the video image must be refreshed 60 times per second to maintain a flicker-free image for the user.

Images displayed upon the CRT may be formatted or unformatted. A formatted display contains one or more special control characters called attribute characters in the first 24 lines of the display. An attribute is a character which defines the characteristics of all the data in the field following it up to but not including the next attribute. Characteristics that may be defined by an attribute include normal versus high intensity, display versus nondisplay, protected versus non-protected, alphanumeric versus numeric, and light pen detectable versus not light pen detectable. An attribute can also be defined as any character in the buffer which has the most significant data bit (memory bit 7) on.

An unformatted display contains no attribute characters in the first 24 lines of the display. An unformatted display is displayable, normal intensity, not light pen detectable, and alphanumeric. An attribute always occupies a buffer position (and therefore a screen position) and is always displayed as a blank. Attribute characteristics wrap from end of line and from end of screen (end of screen is defined as the last character in the 24th line).

1.6 KEYBOARD

Operator input to the 1377 is via a 69- or 84-key keyboard. The 84-key keyboard is offered in three versions: typewriter, typewriter with numeric pad, and operator console. The 69-key keyboard is a data entry keyboard. Foreign versions of all but operator console are also available. All 84-key keyboards are electrically identical. Code translation for those keys which change via different keycaps is handled by the MPU. 69-key keyboards are electrically similar to each other, but some differences do exist on certain foreign keyboards.

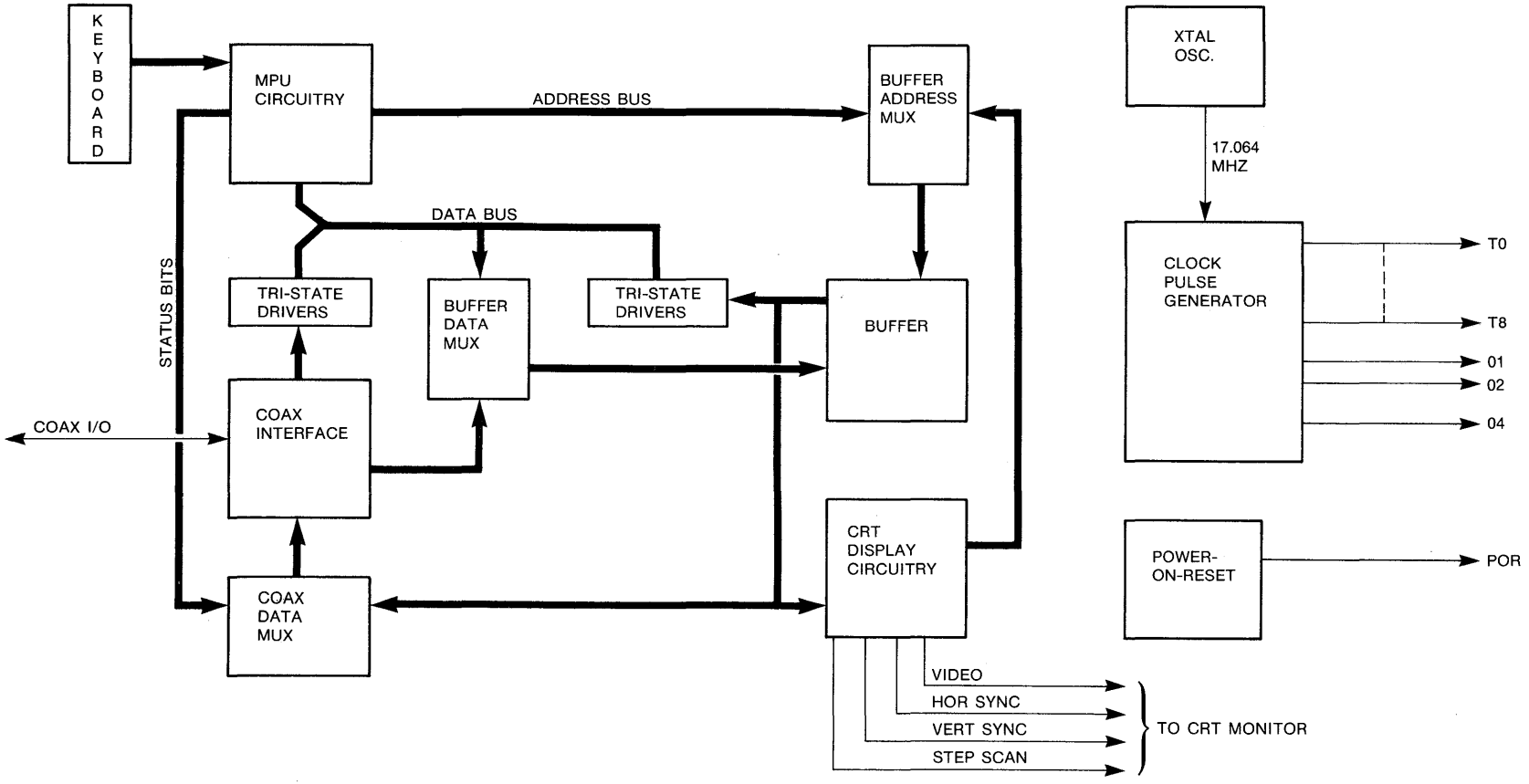

FIGURE 1-1. 1377 BASIC DATA FLOW AND TIMING

SECTION 2
INDICATORS

2.1 CURSOR

The cursor indicates where the next character entered from the keyboard will go on the screen. There should be one, and only one, cursor on the screen at all times, consisting of a reverse video image of the character in the cursor location. The contents of memory chip 10A determine the cursor location on the screen. Although no cursor, or more than one cursor, will not cause any error indication at the terminal, this condition will cause an error at the CU if the buffer is read by the CU.

2.2 LINE AND COLUMN COUNT

The left side of the 25th line normally displays the line and column address of the cursor. The MPU keeps track of the cursor address and writes this information into the appropriate buffer location to display at the beginning of the 25th line. If a parity error occurs during any readout of the buffer, (and readout occurs continuously due to screen refresh) the terminal will generate a status condition known as DEVICE CHECK. DEVICE CHECK will cause the line and column count numbers to disappear, and only the letters 'L' and 'C' will remain. This condition can only be reset by the CU writing a new screen of data (or by turning the machine off and back on).

2.3 STATUS INDICATORS

Three status indicators are written in the 25th line: INPUT INHIBITED, INSERT MODE, and SYSTEM AVAILABLE. The MPU turns the indicators off by writing nondisplay attributes in front of each; the indicators are turned on by writing a display attribute in front of each.

INSERT MODE is turned on in response to the INS MODE key on the keyboard; it is turned off in response to the RESET key on the keyboard.

SYSTEM AVAILABLE is turned on in response to a command from the CU; it is turned off in response to any of the keys causing an attention status to the CU (PA1, PA2, CLEAR, ENTER, TEST REQUEST, PF1-PF12).

INPUT INHIBITED is turned on in response to any of the keys causing an attention status to the CU or by any disallowed keyboard entry; it is turned off in response to a command from the CU (in most cases it can also be turned off by the RESET key).

SECTION 3
COAX LINE DISCIPLINE

3.1 GENERAL

Signals on the bidirectional coax cable consist of the following:

a. Control words transmitted by the CU which causes some action to occur in the terminals.

b. A status word transmitted by the display in response to a request from the CU.

c. Data words transmitted by the CU to the display. Data is always transmitted in blocks of 1920 characters.

d. Data words transmitted by the display in response to a read command from the CU. Data is always transmitted in blocks of 1920 characters.

In normal operation, the CU repetitively sends a control word called a poll and the display responds with a status word. This poll and response sequence continues until some attention condition occurs at the display which requires service by the CU. The sequence following the attention condition will vary depending upon what action is required.

Data on the coax is encoded into a 13-bit word with a 210-nanosecond negative pulse for a logic zero and a 630-nanosecond negative pulse for a logic one. The nominal voltage levels on the coax are ground and +8 volts (the lower voltage may be significantly higher than ground depending upon the length of coax cable). The first bit of a word is always a one; the last bit is a zero if transmitted by the CU and a one if transmitted by the display.

3.2 CONTROL WORDS

A control word is defined as any word transmitted by the CU in which bit two is a logical one. The purpose of the control word is to send a command (as opposed to data) to the display. The following commands are used with the 1377:

Poll (bits 2 and 4 set)—causes the display to respond with a status word.

Read (bits 2 and 5 set)—causes the display to transmit all 1920 characters in its buffer to the CU.

Write (bits 2 and 6 set)—precedes a block of 1920 characters being sent from the CU to the display.

Set System Available (bits 2 and 7 set)—causes the SYSTEM AVAILABLE legend to be turned on.

Unlock Keyboard (bits 2 and 8 set)—causes the INPUT INHIBITED legend to be turned off and the AID code to be reset.

EAU (bits 2 and 9 set)—causes all unprotected fields on the screen to be reset to nulls.

Reset Xmit Check (bits 2 and 10 set)—causes the TRANSMIT CHECK bit in the status word to be reset.

Ack (bits 2 and 11 set)—causes the INFO PENDING bit in the status word to be reset.

Read Poll (bits 2, 4, and 5 set)—causes the display to respond with a status word and prohibits additional keyboard input until after a read or write sequence is completed.

Sound Alarm (bits 2, 3, and 9 set)—causes the audible alarm to sound (this is the only command where bit 3 is set).

Combinations of bits may be used to execute more than one command in a control word, unless they are illegal combinations (such as 5 and 6 or 4 and 6). Bit 12 is used to maintain odd parity on bits 1 through 12.

3.3 STATUS WORD

The status word is transmitted by the display in response to a Poll or Read Poll command. Its function is to indicate any activity at the display requiring system attention. Bit 2 of the status word is always a logical zero. The following describes the purpose of each status bit:

Busy (bit 3 set)—indicates that the display is busy executing some keyboard function or performing an EAU operation.

Device Check (bit 4 set)—indicates that a buffer parity check has occurred. This bit is reset by a Write command.

Transmit Check (bit 5 set)—indicates that a parity error was detected on a data or control word received by the display. This bit is reset by a Reset Xmit Check command or by a Write command.

Info Pending (bit 6 set)—indicates DEVICE CHECK or that an attention interrupt has been generated by the display station operator. This bit is reset by the Ack command.

Parity (bit 12 set)—used to maintain odd parity on bits 1 through 12.

3.4 DATA WORD

Data and attribute information is transferred between the CU and the display in a block of 1920 data words. Bit 2 is always a logical zero. The following describes the meaning of each bit of the data word:

Cursor (bit 3 set)—One (and only one) word of the 1920 characters will have this bit on to indicate the cursor position.

Attribute (bit 4 set)—This bit being on defines an attribute character in bits 5 through 11. If this bit is off, bits 5 through 11 define an alphanumeric character.

Bits 5 through 11—When defined as alphanumeric data, bit 5 is the most significant bit and bit 11 is the least significant bit. When defined as an attribute (by bit 4 being a one):

Attribute Character
Bit Definitions
Bits 5-11

Bit 5 — not used
Bit 6 — 0 = Unprotected field
— 1 = Protected field
Bit 7 — 0 = Alpha field
— 1 = Numeric Field
— 00 = Normal intensity and not light pen detectable
Bits 8 & 9 — 10 = High intensity and light pen detectable
— 11 = Non-display and not light pen detectable
Bit 10 — not used
Bit 11 — 1 = Modified data tag (MDT) for previous field

Parity (bit 12 set)—used to maintain odd parity on bits 1 through 12.

SECTION 4
BASIC MACHINE TIMING

4.1 CRYSTAL OSCILLATOR

All of the timing used in the display is derived from a crystal oscillator. The oscillator circuit shown in Figure 4-1 generates a 17.064-MHz signal which is subsequently used as an input to produce all other clock and timing signals needed in the machine. Two external inputs allow disabling the oscillator and using an external clock for testing purposes; these inputs are not used in normal operation.

Resistors R36 and R37 allow two sections of 4F to operate in the linear region and control the amount of circuit gain. Capacitor C79 decreases the gain at higher frequencies to suppress spurious modes of oscillation, such as might occur due to parasitic capacitances. Pull-up resistors R38 and R44 provide noise immunity for the (normally) unused inputs.

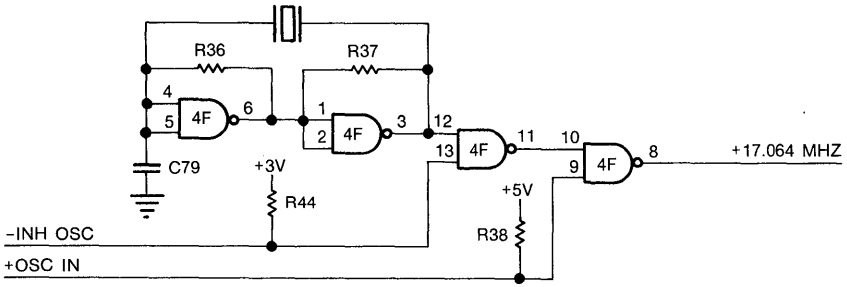

FIGURE 4-1. CRYSTAL OSCILLATOR

4.2 NINE-PHASE LOGIC CLOCK

The basic clock is divided down to produce nine distinct clock phases which are used for sequencing various logical operations. See Figure 4-2. A single negative bit is propagated through the eight-stage shift register producing eight mutually-exclusive clock pulses. The ninth pulse is produced by the eight-input NAND gate which detects when the shift register is empty (all outputs high). The NAND gate also inputs the negative bit to the shift register so that the cycle may repeat. Because the input frequency is 17.064 MHz, each clock phase will be 58.6 nanoseconds wide repeating every 527 nanoseconds.

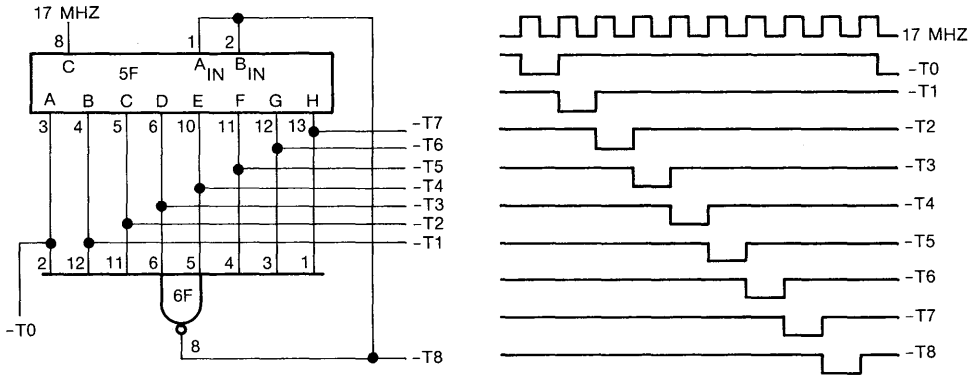

FIGURE 4-2. NINE-PHASE CLOCK

4.3 MPU CLOCK

The 6800 MPU requires a two-phase, nonoverlapping clock signal which swings from ground (+0.3, -0.1V) to V_{CC} (-0.3, +0.1V). Figure 4-3 show how these two clock phases are generated. In normal operation, 8F is toggled by the trailing edge of -T4. When 8F turns on, 7F turns on. The propagation delay of 7F and section three of 25B ensures that Ø2 will be off before Ø1 turns on. Ø1 is turned off at the leading edge of -T4, ensuring that Ø1 is off before Ø2 is toggled on. Resistors R2 and R3 ensure an adequate high level on the clock; resistors R4 and R5 help damp ringing on the clock lines.

The signal called -HOLD Ø1 allows temporarily halting the MPU (for less than 10 microseconds) when a coax I/O operation requires priority access to the buffer memory. Since the MPU can access the buffer only when Ø2 is

high, holding Ø1 high and Ø2 low solves the potential contention problem between the coax interface and MPU. Section three of 25B is required to ensure that Ø1 does not change state when both the set and reset inputs of 7F are low.

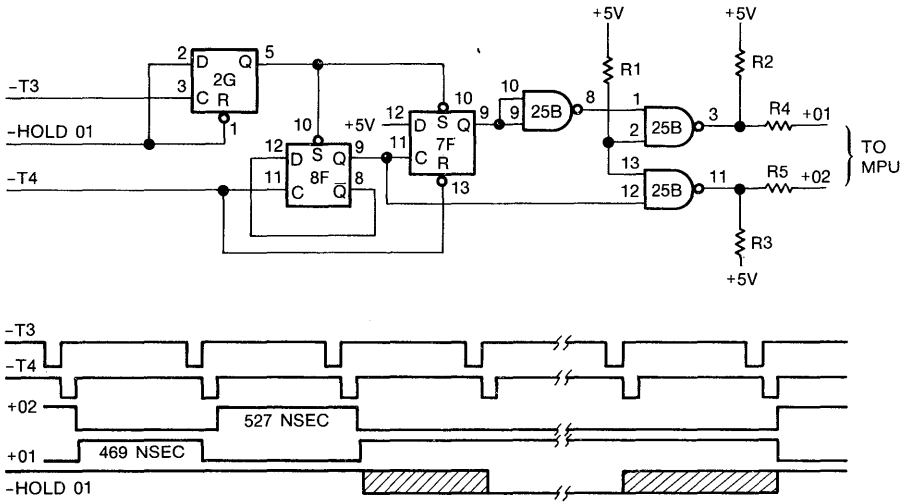

FIGURE 4-3. MPU CLOCK LOGIC AND WAVEFORMS

4.4 BUFFER CLOCKING

The TMS4060-2 dynamic RAM chips used in the buffer require a clock signal which swings from ground (±0.6V) to V_{DD} (-0.6, +1.0V). Figure 4-4 shows how this clock is generated. The clock pulse is normally about 350 nanoseconds wide; however, it is shortened during a buffer write operation to ensure that the data hold time requirement of the chip is not violated. Chip 11A converts the TTL level generated to the -12 volt swing required by the memory chip. CR8 and R41 help to damp ringing.

The signal called -RDMA is only used when the display is executing a Read command (transmitting its buffer contents to the CU). The function of this signal is to stretch the CE signal so that data remains valid at the buffer output for a longer period of time. This additional time is required because the coax interface and the buffer are not synchronized to each other.

The dotted line in the -WRITE BFR waveform shows the timing if the write is caused by the MPU; the solid line shows the timing if the write is caused by the coax interface.

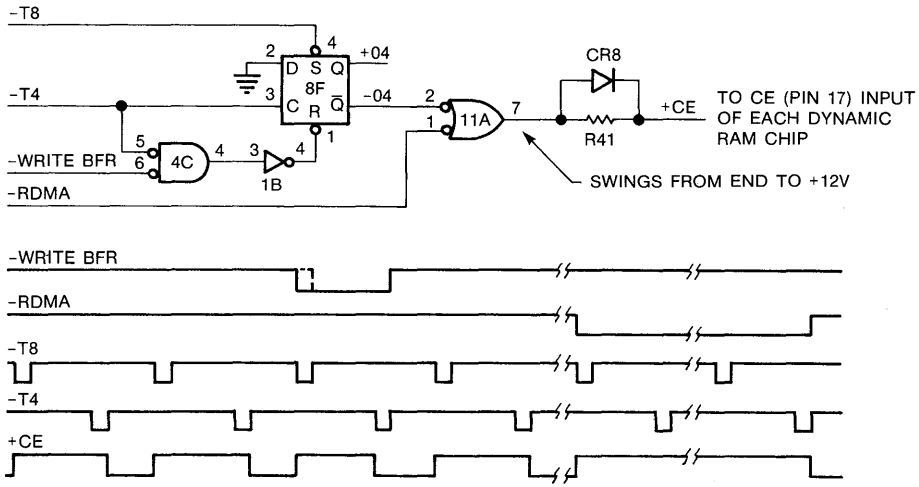

FIGURE 4-4. BUFFER CLOCKING LOGIC AND WAVEFORMS

4.5 POWER-ON-RESET (POR) CIRCUIT

The circuit shown in Figure 4-5 is used to generate a power-on-reset pulse of approximately 0.8 second. Using this pulse ensures that the machine comes up in a known condition. (The MPU requires some sort of reset pulse to cause it to start executing instructions in the proper sequence.)

Applying power to the logic board causes C5 to charge through R10 and the base-emitter junction of Q1. The charging current causes Q1 to pull the input of the inverter low. As C5 charges up and the charging current decreases, the collector of Q1 rises until the threshold of the inverter is reached. Feedback from the second inverter via CR2 causes the circuit to switch off, terminating the POR pulse. R9 and CR1 ensure discharging of CR5 when the power is turned off. The EXT RESET input is not used in normal operation but is available for purposes of test and debug of the PCB.

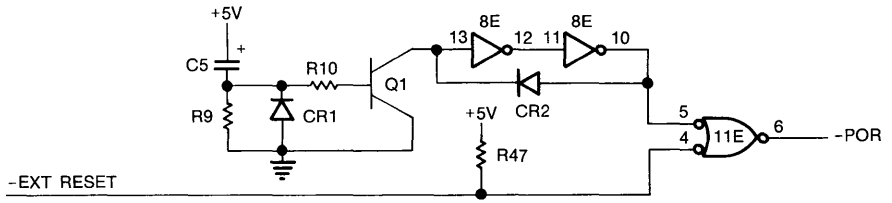

FIGURE 4-5. POR CIRCUIT

SECTION 5
CRT REFRESH CIRCUITY

5.1 GENERAL DESCRIPTION

Figure 5-1 shows a block diagram of the circuitry used to generate the signals required to drive the CRT monitor. This circuitry generates an address which is applied to the buffer, and the buffer reads out a word which is then converted to video. Each word is actually read out 12 times per refresh of the screen since there are 12 scans for each row of characters.

5.2 HORIZONTAL COUNTER

The horizontal counter consists basically of two decade counters which divide the character rate clock by 100. Characters are displayed for 80 character times, and horizontal retrace occurs during the remaining 20 character times. The carry output of the second counter generates a negative pulse which is propagated through 24 shift register stages. The shift register outputs are timing pulses which are used to generate signals related to the horizontal scanning cycle. See logic page DA001.

5.3 VERTICAL COUNTER

The vertical counter consists of two 4-bit binary counters and four 8-bit shift registers interconnected in such a way as to divide the output of the horizontal counter by 316. The count sequence is shown in Figure 5-2.

In addition, vertical timing signals such as vertical sync and blanking are generated by this counter. See logic pages DA000, DA001.

5.4 ADDRESS GENERATION

The display buffer refresh address is generated by a presettable, 11-bit binary counter. See logic page DA002 for the complete logic. This circuitry also serves as a DMA counter when data is being transferred between the buffer and the coax; mode control is via the multiplexer (7E) chip. The refresh-address generation must be interrupted (and the display will be blanked) during a DMA operation. (The DMA mode of operation of this circuit will be explained in a later section.)

The sequence begins by resetting the address register to zero during the vertical blanking interval. The address counter is loaded with the contents of the address register at the beginning of each horizontal scan. This register is zero for the first 12 scans after the vertical blanking interval. After being loaded, the counter increments one count for each character time. Thus, the counter generates addresses 0 through 79 twelve times. (The counter actually counts to 98 before being reloaded, but these counts above 79 occur during horizontal retrace and do not result in a displayable image.)

The address register is loaded at the end of every twelfth scan with the contents of the address counter; the three low-order bits are always loaded with zero. Thus, the address register will contain 0, 80, 160, 240, ..., 1920. The address counter then increments through the next 80 characters 12 times. This sequence continues, except that the last line contains only 9 scans instead of 12, until the beginning of the vertical blanking interval. At the end of the vertical blanking interval, the entire cycle is repeated.

The numerical representation of the cycle is as follows:

(0, 0, 1, 2, 3, ..., 79, ..., 98) X 12
(80, 80, 81, 82, 83, ..., 159, ..., 178) X 12

(1840, 1840, 1841, 1842, 1843, ..., 1919, ..., 1938) X 12
(1920, 1920, 1921, 1922, 1923, ..., 1999, ..., 2018) X 12
(0 through 98 during vertical blanking interval)

Repeated 60 times per second

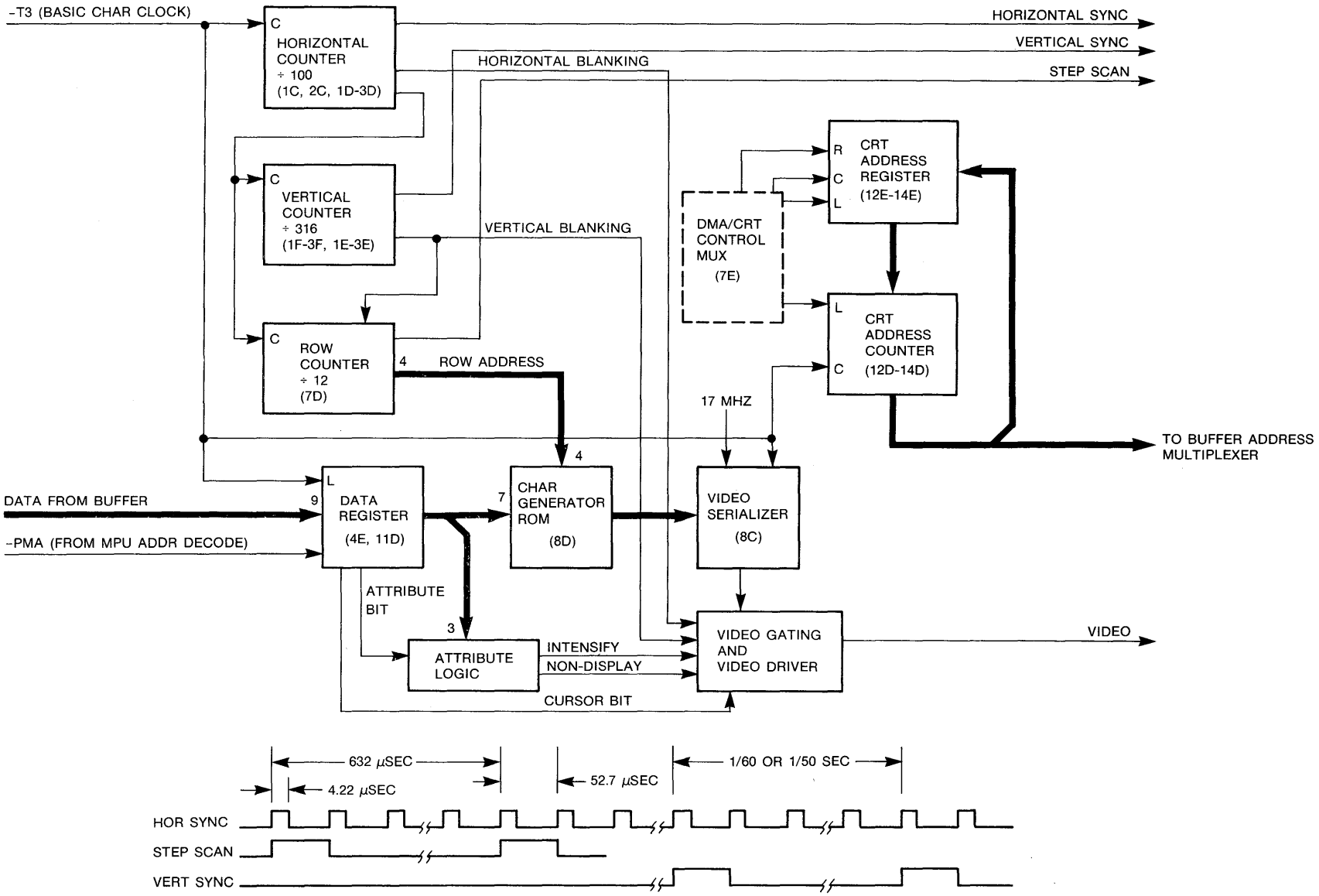

FIGURE 5-1. CRT REFRESH BLOCK DIAGRAM AND WAVEFORMS

COUNT NUMBER		COUNTER OUTPUTS 3F	1F		SHIFT REGISTER OUTPUTS 2F5	2E12	COMMENTS
1		0	0		1	0	Reset
2		0	0		1	1	
⋮		⋮	0		1	1	
17		15	0		1	1	
18	37,...,284	0	1	2,...,15	1	1	
19	38,...,285	1	1	2,...,15	1	1	This sequence
20	39,...,286	0	1	2,...,15	0	1	occurs 15 times.
21	40,...,287	0	1	2,...,15	1	1	
22	41,...,288	1	1	2,...,15	1	1	
23	42,...,289	2	1	2,...,15	1	1	
			1	2,...,15	1	1	
			1	2,...,15	1	1	
36	55,...,302	15	1	2,...,15	1	1	
303		0	0		1	1	Vertical sync
304		1	0		1	1	
305		0	0		0	1	
306		0	0		1	1	
307		1	0		1	1	
308		2	0		1	1	
⋮		⋮	0		1	1	
316		10	0		1	1	Last state

FIGURE 5-2. VERTICAL COUNTER SEQUENCE

5.5 CHARACTER GENERATOR AND VIDEO SERIALIZER

Data read out of the buffer must be converted to a form suitable for display by the CRT monitor. This is accomplished by using the 7 data bits and 4 row address bits to address a ROM which contains a do-matrix representation of the character. See Figure 5-3. The 7 parallel outputs of the character generator ROM are loaded into a shift register; clocking the shift register generates a serial video signal.

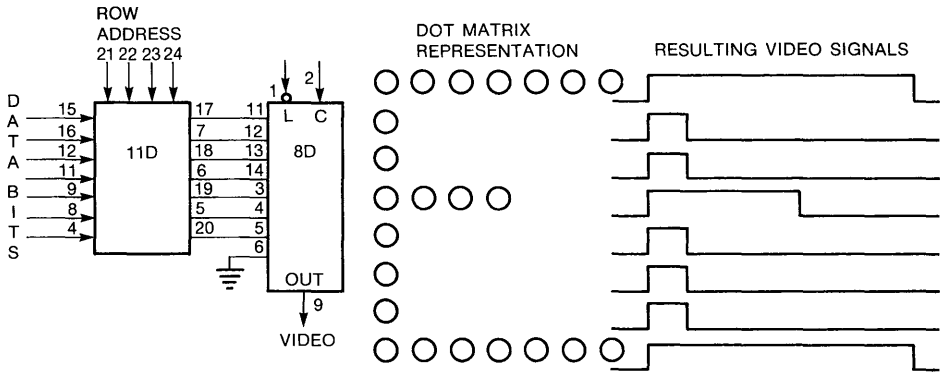

FIGURE 5-3. DATA TO VIDEO CONVERSION

Each of the 80 characters in a line is accessed sequentially to form the video for one scan of a line. Each is accessed again for the next scan; a total of twelve scans make up each line of characters. The first scan of a line is blanked (except for the cursor), and the last line is also blanked (because of step scan). The step scan signal (which is the twelfth count of the row counter) causes the CRT beam to move down several scans during a period of a single scan. The 7 × 8 dot matrix is normally displayed on scans 2 through 9; however, scans 10 and 11 are used for lower case characters with descenders and for some special characters.

5.6 ATTRIBUTE CIRCUITRY

The attribute portion of the CRT refresh circuitry has three main functions:

1. It causes attribute characters to display as blanks.
2. It causes a field to be normal or high intensity.
3. It causes a field to be displayed or not displayed.

Function 1 is implemented by bit OMB 7 on the logic (sometimes referred to as the attribute bit). This bit is always on for an attribute and off otherwise. When on, therefore, the bit is used to gate the video off.

Functions 2 and 3 are more involved because of the requirement that a field defined by an attribute must be able to wrap from the end of one line to the beginning of the next (or from the end of the screen to the beginning of the screen). This requires two bits of storage for each attribute—one to store the current attribute as characters are read out of memory, and one to store the attribute that was in effect at the end of the last line. The "last line" attribute then must be used to initialize the "current" attribute at the beginning of each scan. At the end of every twelfth scan, the "current" attribute must be used to update the "last line" attribute. Since the 25th line contains only nine scans, the attribute wrapped around to the beginning of screen will be that in effect at the end of the 24th line. Attributes read out during horizontal blanking are ignored so as not to store an invalid "last line" attribute.

The signal in Figure 5-4 called -RESET ATTRIBUTE LATCHES is required so that any transient attribute condition (occurring during DMA read or write) will not cause an incorrect condition to latch up. Also, the signal called +END OF 12TH SCAN is inactive during vertical blanking, and the signal called +ATTRIBUTE BIT is inactive during horizontal blanking. See logic page DA001 for more complete attribute logic. Attribute conditions other than display/non-display and normal/high intensity are handled by the MPU.

5.7 BLANKING CIRCUITRY

The video is blanked (gated off) by a number of conditions. Horizontal and vertical retrace, attribute character, non-display field, step scan, and keylock off are some self-explanatory blanking conditions. DMA blanking occurs for the duration of data transfer between the coax and the buffer; it is reset at the beginning of vertical blanking following completion of data transfer (defined as READ or WRITE latch being reset).

The final blanking condition occurs when the MPU accesses the buffer to read or write a character. Since the MPU and the refresh circuitry cannot access the buffer simultaneously, the MPU is assigned priority and the display is blanked for one scan of one character for each MPU access. Recognition of an attribute character by the refresh circuitry is also inhibited during a MPU access to the buffer.

Gates 13F and 4D on logic page DA001 are the points at which the blanking occurs.

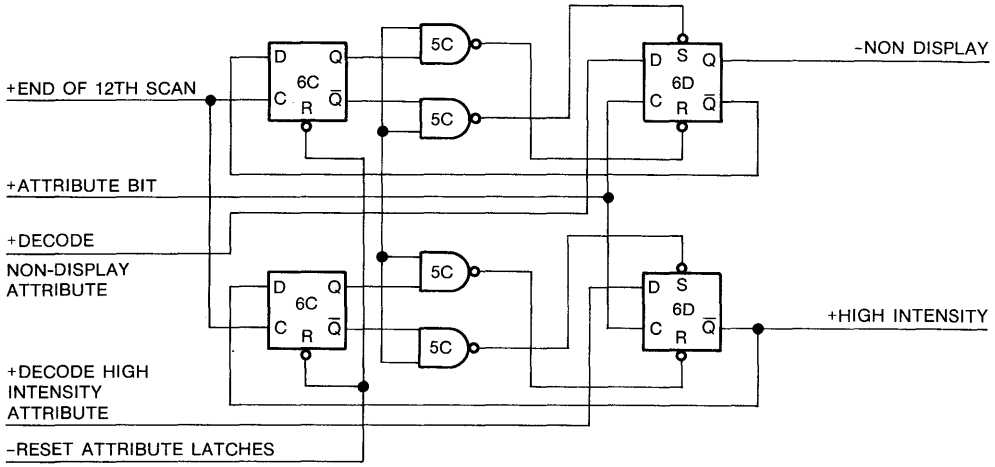

FIGURE 5-4. ATTRIBUTE SEQUENCING CIRCUIT

SECTION 6
MICROPROCESSOR-CONTROLLED FUNCTIONS

6.1 MPU AND SUPPORT CHIPS

The major components associated with the MPU, as well as the data flow associated with the MPU, are shown in Figure 6-1. Events which require a response by the MPU are keyboard input, light pen input, commands from the coax interface, and initial power-on. Responses by the MPU include altering the buffer contents (and therefore the display), sounding the audible alarm, and updating the status register.

Operation of the MPU is controlled by the two clock phases, Ø1 and Ø2, shown in Figure 6-1. All data transfers occur during Ø2; therefore any signals on the data bus during Ø1 are undefined. The address and control lines (R/W, VMA) are set up during Ø1 and remain valid for the duration of Ø2. The MPU generates the address of the device that it wishes to communicate with and the address is decoded to provide a chip-select signal for that device. Data is then transferred. Only one byte of data may be transferred for each Ø2 cycle. Since a common data bus is used, only one device at a time may be selected to put data onto the bus.

Software for the MPU is contained in three 2708 EPROM's (see logic page DA010). After power-on-reset, the MPU sends out addresses FFFE and FFFF to read out two bytes from EPROM in position 13E which constitute the address of the first instruction. Thereafter, the instruction sequence is determined by the contents of the EPROM's and the external inputs to the MPU.

The static RAM contains 128 bytes of R/W memory which are used by the MPU for temporary storage. This memory is not part of the buffer, and it does not store any displayable data. Part of this static RAM comprises the push-down/pop-up stack which stores information necessary to resume operation after an interrupt or subroutine completion.

PIA #1 interfaces data and strobe lines of the keyboard to the MPU. The strobe line causes the PIA to generate a maskable interrupt. The interrupt causes the MPU to read the data from the keyboard. Additional function lines (and control lines for the data entry keyboard) are read via PIA #2. Eight option switch settings can be read by the MPU via PIA #2. The status register is implemented by using 7 bits (programmed as outputs) of PIA #1. This register maintains 7 of the bits that are returned to the CU in response to a poll. One additional bit (programmed as an output) is used to sound the audible alarm. See appendix for further PIA bit definitions.

6.2 KEYBOARD INPUT

The keyboard is the major means of input by an operator to the terminal. Depressing a key causes the keyboard strobe line (to input CA1 of PIA #1) to go low. This, in turn, causes the interrupt line to the MPU to go low. The MPU then goes from an "idling" routine to its interrupt routine. The MPU reads the control register of the PIA to determine the source of the interrupt (if the interrupt was not caused by the keyboard, additional control registers in PIA #1 and PIA #2 would be read). The MPU then enables the "A" side of PIA #1, causing the eight data bits from the keyboard to be gated through to the MPU.

The keyboard data is analyzed by the MPU to determine what action is required. Depending upon which key is pressed and what keyboard is attached, the code received may have to be translated (e.g. pressing the Q key on a French keyboard requires translation of the "A" code received to the "Q" code desired). The code is written into the buffer (assuming it is a character to be displayed) at the current cursor position. The cursor is then incremented. Because the buffer is nine bits wide (excluding parity), three separate writes are required to add a character to the display—character is written, old cursor bit is erased, and new cursor bit is written. Examination of the buffer chip select circuitry will show that the eight data bits are accessed when the MPU supplies a hexadecimal address of 3XXX; the cursor bit is accessed for a 4XXX address.

If the data character entered is disallowed at the current cursor position (e.g. at an attribute, an alpha character in a numeric field, or the field is protected), the MPU will turn on the INPUT INHIBITED indicator and sound the audible alarm.

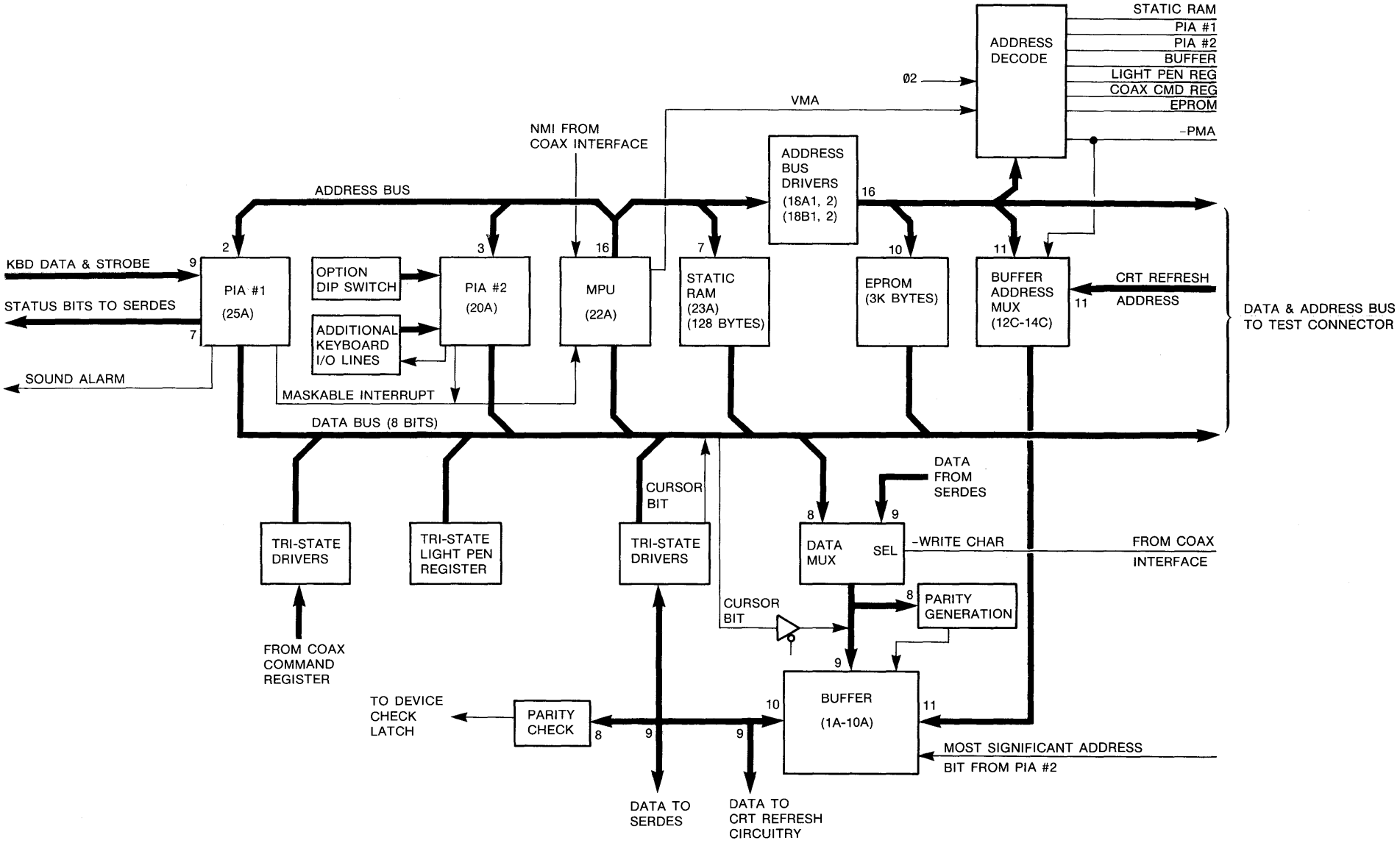

FIGURE 6-1. MPU BLOCK DIAGRAM

A control character entered from the keyboard will result in a number of different actions, depending upon the character. Some characters cause movement of the cursor to a new position. Some cause partial or complete clearing of the screen. Some cause modification of the status word and lock the keyboard; these will cause some additional action which is dependent upon host CPU programming.

6.3 COMMAND REGISTER

This set of inputs is the result of decoding a command from the CU (or a buffer parity error). If any of these eight bits (see logic page DA007) is set, a nonmaskable interrupt (NMI) is sent to the MPU. The NMI causes the MPU to switch to the NMI routine which tells the MPU to read the command register and take the appropriate action.

The CU Busy latch is set by a Read Poll command and reset by a Poll command. This command precedes a Read or Write command and causes the MPU to inhibit any additional keyboard input to the buffer.

The Read latch is set during the time that the display is transmitting its buffer to the CU. It is reset by transmitting the 1920th character. No MPU action occurs except to keep reading the command register until the Read command finishes.

The Write latch is set during the time that the display is receiving data from the CU. It is reset by receipt of the 1920th data character. After the latch is reset, the MPU searches the buffer to locate the new cursor address and the address of the first unprotected screen location. This information is necessary for the MPU to know where to place input characters from the keyboard.

The Device Check latch is set anytime a character with incorrect parity is read out of the buffer. It is reset by the next Write command. Setting this latch will cause the MPU to erase the line number and the column number in the 25th line and to inhibit further keyboard input. (This condition is easy to detect because it is the only time the letters "L" & "C" appear in the 25th line without any numbers.)

The Reset Info Pending latch is set by the Ack command and reset by the MPU after it resets bit 6 in the status word.

The EAU latch is set by the EAU command and reset by the MPU after it sets all unprotected characters in the buffer to nulls. Reset is accomplished by the PROGRAM BUSY line going inactive (negative transition). The PROGRAM BUSY line is kept active (high) by PIA #1 while the EAU subroutine is being executed.

The Unlock KBD latch is set by the Unlock Keyboard command and reset by the MPU after it turns off the INPUT INHIBITED indicator.

The Restore Sys Avail latch is set by the Set System Available command and reset by the MPU after it turns on the SYSTEM AVAILABLE indicator.

All four of the preceding commands (or as many as are set) are executed before any are reset (except EAU) since a common reset line clears all the latches. Reset is accomplished by an MPU write to the command register or the POR signal. A gated POR signal also resets the other four latches when the machine is powered on.

6.4 LIGHT PEN

The light pen itself consists of (1) a photosensitive detector coupled to an amplifier and single-shot and (2) a pressure-sensitive switch coupled to the movable light pen tip. Output from the light pen occurs whenever the CRT beam passes through the field of view of the photodetector.

When the light pen switch is activated, the light pen register and the light pen interrupt flip-flop are enabled (see logic page DA005). A pulse on the light pen strobe line then causes the light pen interrupt flip-flop to set and the current CRT refresh address (which is the location of the light pen) is strobed into the light pen register. The interrupt causes the MPU to read the light pen register, capturing the location of the light pen; two reads are necessary since the MPU can only read 8 bits at a time. The MPU then alters the MDT bit in the attribute character for the next field and changes the designator character (first character after the attribute defining a light pen detectable field) from a ? to a >. If the designator character was a space or null, an attention field was detected and the INFO PENDING bit and AID code are set in the status word as well as the MDT bit of the attribute character. The designator character is not changed.

6.5 STATUS REGISTER

The status register consists of those bits which make up the status word that is sent to the CU in response to a Poll or Read Poll command. It is physically implemented by 7 bits of the B side of PIA #1, the Device Check latch, and the Xmit Check latch. One of the PIA bits is ORed with the EAU latch and one is ANDed with the Reset Info Pending latch to provide the actual status bits transmitted. This is necessary to compensate for the time that it takes the MPU to update the PIA bits.

The Busy, Info Pending, and AID bits are generated by the MPU and latched by PIA #1. Clear and EAU are the operations which cause the busy bit to be turned on. The AID code is shown in Table 6-1.

6.6 OPTION SWITCHES

A DIP switch is included on the PCB to enable various optional features. See logic page DA002 for the meaning of each of the eight individual switches. These switches are interrogated by the MPU during the power-on sequence to enable the correct software routines.

6.7 BUFFER

The buffer is controlled from three different sources: the MPU, the coax interface, and the CRT refresh circuitry. The eight data bits written into the memory are also inputs to parity generator chip 23B (see logic page DA004). This chip causes odd parity to be generated and written along with the data. The eight data bits are applied to a parity checking chip (7B on logic page DA009) whenever data is read out of the buffer. Note that parity checking is inhibited for any data at address 1920 or above (since these characters are not part of the data), for anything that appears at the buffer output during a write, during initialization, and whenever the cursor bit is being accessed by the MPU.

Since the buffer stores nine bits (excluding parity), access by the MPU must be in two steps—one access for the eight data bits, and one access for the cursor bit (access by the coax or refresh circuitry is nine bits). This is accomplished by separate chip select signals for the cursor and data bits and by separate enable signals for the tri-state drivers that couple the buffer output to the MPU data bus (9D1 and 4 and 9C3 and 6 on logic page DA004).

TABLE 6-1. AID CODES

COAX STATUS WORD BIT POSITION					CODE CAUSED BY
7	8	9	10	11	
0	0	0	0	0	NO AID GENERATED
0	1	1	0	0	PA1 KEY
0	1	0	1	1	PA3 KEY
0	1	1	0	1	CLEAR KEY
0	1	1	1	0	PA2 KEY
1	0	0	0	0	TEST REQ KEY
1	0	0	0	1	PF1 KEY
1	0	0	1	0	PF2 KEY
1	0	0	1	0	PF3 KEY
1	0	1	0	0	PF4 KEY
1	0	1	0	1	PF5 KEY
1	0	1	1	0	PF6 KEY
1	0	1	1	1	PF7 KEY
1	1	0	0	0	PF8 KEY
1	1	0	0	1	PF9 KEY
1	1	0	1	0	PF10 KEY
1	1	0	1	1	PF11 KEY
1	1	1	0	0	PF12 KEY
1	1	1	0	1	ENTER KEY
1	1	1	1	0	LIGHT PEN

SECTION 7
COAX INTERFACE

7.1 DESERIALIZATION OF COAX INPUT

A block diagram of the coax interface is shown in Figure 7-1. Data received by the 1377 must be detected, converted to logic levels, and deserialized. This process is illustrated in Figure 7-2. Signals on the coax are fed to a comparator circuit which switches at approximately the 6-volt level. The comparator is fed to a logic gate which converts that signal to output a TTL level. It is then necessary to recover a clock which can be used to load the bits into a shift register.

The received signal is pulse-width-modulated with a nominal 210 nanoseconds for a logic zero and a nominal 630 nanoseconds for a logic one. Demodulation requires that a clock pulse be generated at a nominal 420 nanoseconds to sample the signal. A positive transition at point B is applied to the input of an eight-bit shift register. This shift register is clocked at 17 MHz, causing the positive transition to appear at point D from 293 to 351 nanoseconds later. The signal at point D is sent through three stages of gating and clocking into a flip-flop. The flip-flop Q output causes the shift register to be reset on the next cycle of the 17-MHz clock.

The Q output (point F) is a nominal 58.6-nanosecond clock pulse which is delayed by 351 to 410 nanoseconds from the positive transition at point B (actual delay is somewhat higher because of gate delays). This clock pulse is then used to shift data into the Serdes. Since the Serdes is initially cleared and the start bit is always a logic one, the twelfth clock pulse causes output Q12 to go high. The resulting output at point H indicates that the character has been deserialized, and valid data is available at the parallel outputs of the Serdes. Data remains valid only until the next clock pulse (at point F). The +CHAR IN strobe at point H is inhibited for two 17-MHz clock cycles (one before and one during the Serdes clock pulse) to avoid glitches in the circuitry that decodes the parallel Serdes outputs. When +CHAR IN signal goes inactive, the Serdes is reset (not shown).

Additional logic blocks shown in Figure 7-2 modify the normal operation explained above slightly. Latch Z1, which is normally set, is necessary to inhibit a second (spurious) output from shift register Z2 while a logical one is being received. Resetting the shift register also resets Z1, inhibiting the high level at point B from propagating through the shift register a second time. Gate Z5 is necessary to ensure that flip-flop Z7 will be on for only one cycle of the 17-MHz clock (in spite of the propagation delay difference through Z2, Z3, and Z4 for positive and negative levels). Gates Z3 and Z4 allow stretching the +CHAR IN signal by two cycles of the 17-MHz clock when a data (as opposed to control) character is being received. This is necessary to ensure that valid data is available (at Serdes parallel outputs) long enough to complete loading the buffer.

For the first 12 bits of a word, output Q6 of Z2 is used to generate the Serdes clock pulse. After the twelfth bit is received, and +CHAR IN becomes active and a data character is decoded, the -DMA R/W CLOCK signal goes low. This causes Q8 rather than Q6 to generate the Serdes clock pulse. The fact that the thirteenth bit is sampled later than normal does not cause a problem because it is always a logic zero. The -OUTPUT LATCH signal is used in several places to inhibit this circuitry during a transmit operation.

The subsequent operations depend upon what is decoded from the parallel Serdes outputs during +CHAR IN time. A Poll or Read will cause the Serdes to be parallel loaded with the character to be transmitted (rather than being reset), followed by a transmit operation. Any other received character will reset the Serdes so that all outputs are low.

7.2 SERIALIZATION OF COAX OUTPUT (POLL COMMAND RESPONSE)

Information is transmitted by the terminal for only two conditions—response to a Poll (or Read Poll) command and response to a Read command. The Poll results in a single (status) character being transmitted; the Read results in 1920 (data) characters being transmitted. This section details transmission of the status character while the Read sequence is covered in the next section.

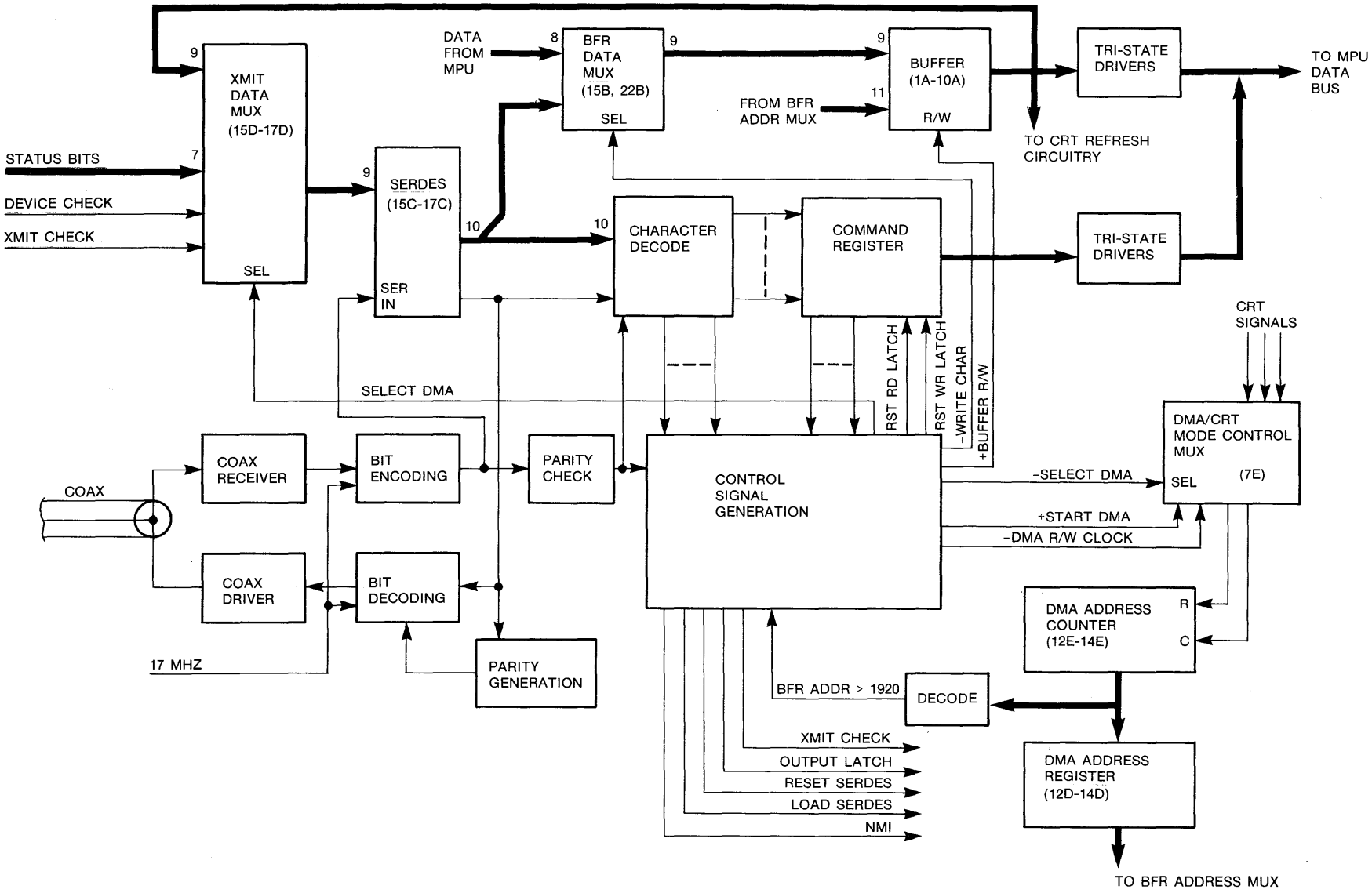

FIGURE 7-1. COAX INTERFACE BLOCK DIAGRAM

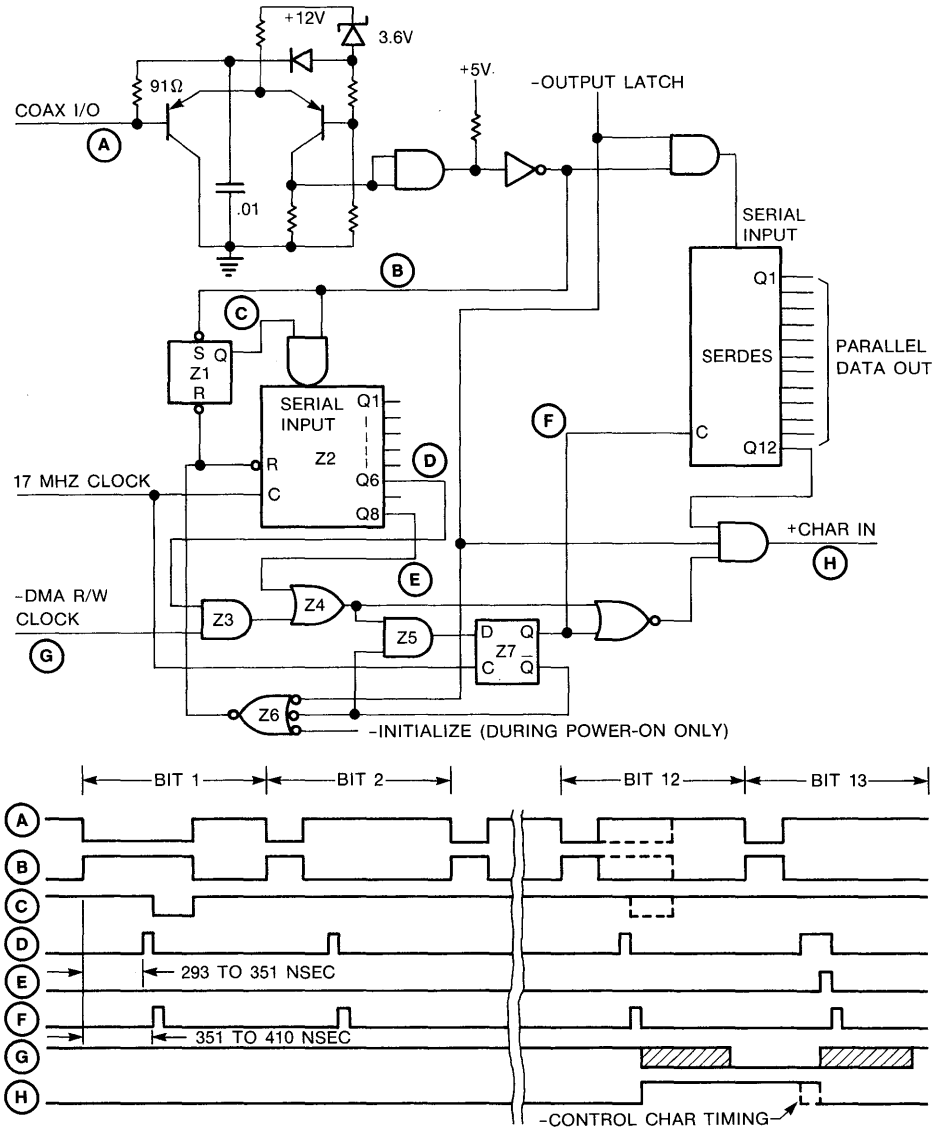

FIGURE 7-2. DESERIALIZATION OF COAX INPUT

The significant logic and timing associated with transmitting a single character is shown in Figure 7-3. A character is deserialized as described in the preceding section, decoded as a Poll command, and used to set the Poll latch; the Poll latch going true causes the transmit operation to actually start. The initial events are controlled by the last two clock pulses of the received character; thereafter, all events are controlled by the timing pulses generated by the Output Bit Width Counter. This counter is free-running (except when reset by an incoming character) with a count length of 15 cycles of the 17-MHz clock. The "1" BIT STROBE signal, which determines the pulse width of a logic one, is nominally 670 nanoseconds; the "0" BIT STROBE signal, which determines the pulse width of a logic zero, is nominally 180 nanoseconds. See logic page DA008 for details of this circuitry.

The Poll latch going true causes the Load Serdes latch to go true. This signal changes the Serdes from the shift to the load mode. The next Serdes clock pulse causes the parallel input (which, in this case, is the status word) to be loaded. The thirteenth SHIFT SERDES IN clock pulse sets the Output latch. This latch enables the SHIFT SERDES OUT signal which is used to shift the Serdes during a transmit operation. The first shift pulse causes the Serdes to be loaded and switches the Serdes back to the shift mode. It should be pointed out that the actual clock pulse to the Serdes is the ORing (not shown in Figure 7-3) of SHIFT SERDES IN and SHIFT SERDES OUT.

The output of the Serdes is applied to logic circuitry that encodes each bit into the pulse-width modulated signal required by the coax. This modulated signal is gated with the Output latch (and with SHIFT SERDES IN to avoid a glitch during the transition from receive to transmit) and fed to a driver whose output is connected to the coax cable. The "0" BIT STROBE is gated through for each bit. This ORing causes no problems since the "0" BIT STROBE is active for only the first 180 nanoseconds of the "1" BIT STROBE.

Application of the twelfth SHIFT SERDES OUT clock pulse causes the Poll latch to be reset and transmission of the parity bit. (Note that the source of this bit is the Parity latch, not the Serdes.) Application of the thirteenth SHIFT SERDES OUT clock pulse empties the Serdes and generates the signal called SR EMPTY. At the end of the thirteenth "1" BIT STROBE, the Output latch is clocked off. (Note that if the Read latch had been on, the Output latch would not have been reset; instead, the Serdes would have been loaded with another character to be transmitted.)

7.3 READ COMMAND RESPONSE

The first character of a Read command response is handled in a manner identical to that of the Poll command except that the Read latch is set instead of the Poll latch and the character is loaded into the Serdes from the buffer instead of from the status register. Serializing the next 1919 characters is accomplished with the same circuitry (Figure 7-3) by setting the Load Serdes latch during the last bit of each character. Transmitting the 1920th character resets the Read latch, which inhibits further setting of the Load Serdes latch.

Figure 7-4 shows some of the control logic and associated timing necessary to initialize and increment the DMA address counter and to synchronize data transfer between the buffer and the Serdes. The Read latch going true generates -SELECT DMA which switches the CRT/DMA address circuitry (logic page DA002) to the DMA mode of operation. The leading edge of -SELECT DMA causes a reset signal (+START DMA) which initializes the DMA counter to zero. The Read latch going true also generates the first LOAD SERDES pulse (see Figure 7-4). The LOAD SERDES pulse is used to generate a signal (RDMA) which is synchronized to the buffer timing (Ø4). Normally, valid data appears at the buffer output only for the last 150 nanoseconds of the Ø4 clock. Since this time would not usually coincide with the time when data was actually needed (to load the Serdes), it is necessary to stretch the memory cycle with RDMA until after the Serdes is loaded. Another signal derived from the LOAD SERDES pulse and synchronized to the buffer cycle is the DMA R/W CLOCK. This clock increments the DMA counter by one after the Serdes is loaded, and it changes the source of parallel inputs to the Serdes from the status register to the buffer. Note that incrementing of the DMA counter occurs on the positive (trailing) edge of -DMA R/W CLOCK; synchronization with the buffer cycle is required because dynamic RAMs allow address lines to change only during a portion of the cycle.

Generation of the RDMA and DMA R/W CLOCK signals is similar for characters after the first, except that -BIT 12 OR 13 TIME initiates them. Use of this signal is necessary because the LOAD SERDES signal does not occur early enough, with respect to the end of the 13th bit, to guarantee valid data out of the buffer when the Serdes is loaded. The transitions of several signals (RDMA, DMA R/W CLOCK, BFR ADDR -1920, and the trailing edge of the Read latch) in Figure 7-4 cannot be shown exactly because they are synchronized to the buffer cycle, while the others are not. The nominal transition value (at the midpoint of the shaded areas) shows the relationship that they have with each other.

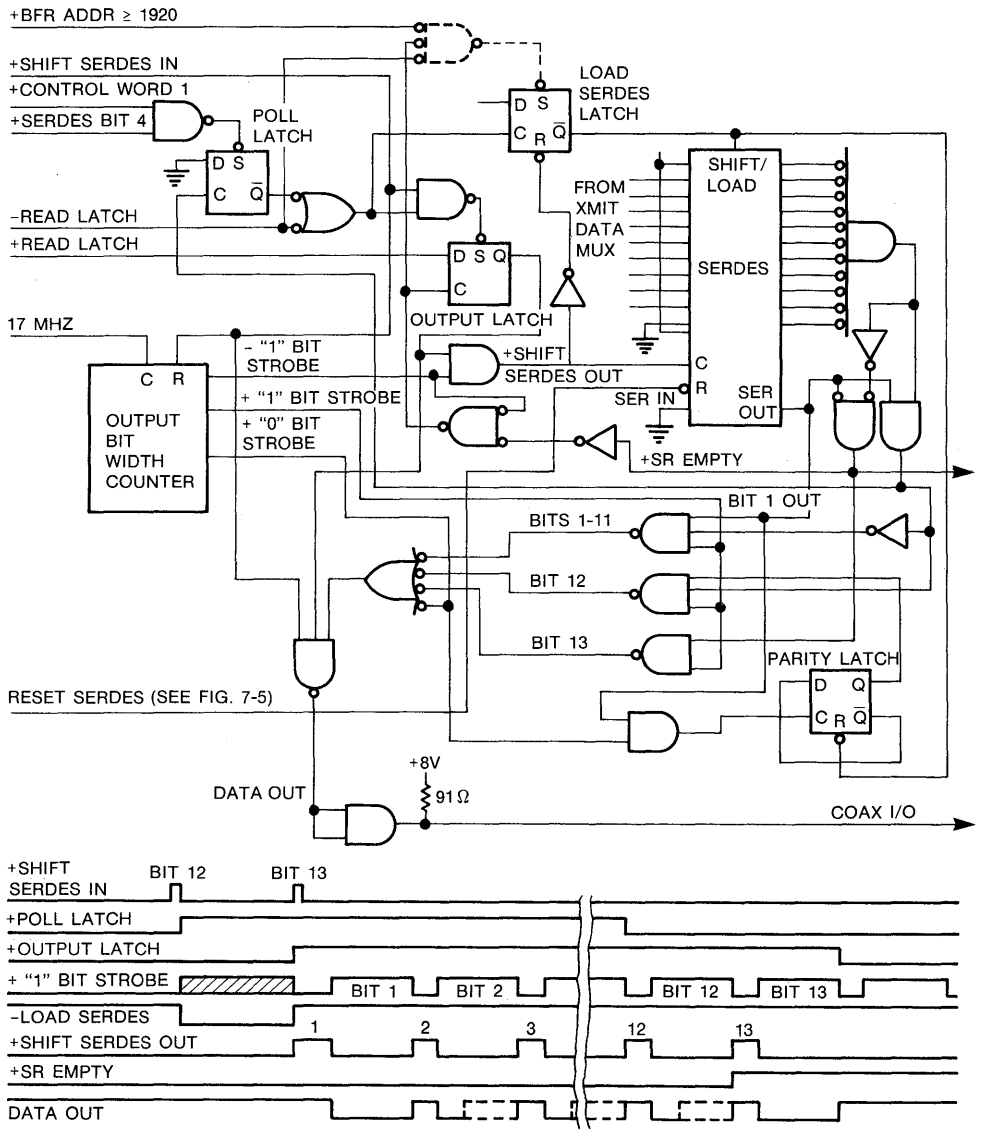

FIGURE 7-3. SERIALIZING RESPONSE TO A POLL

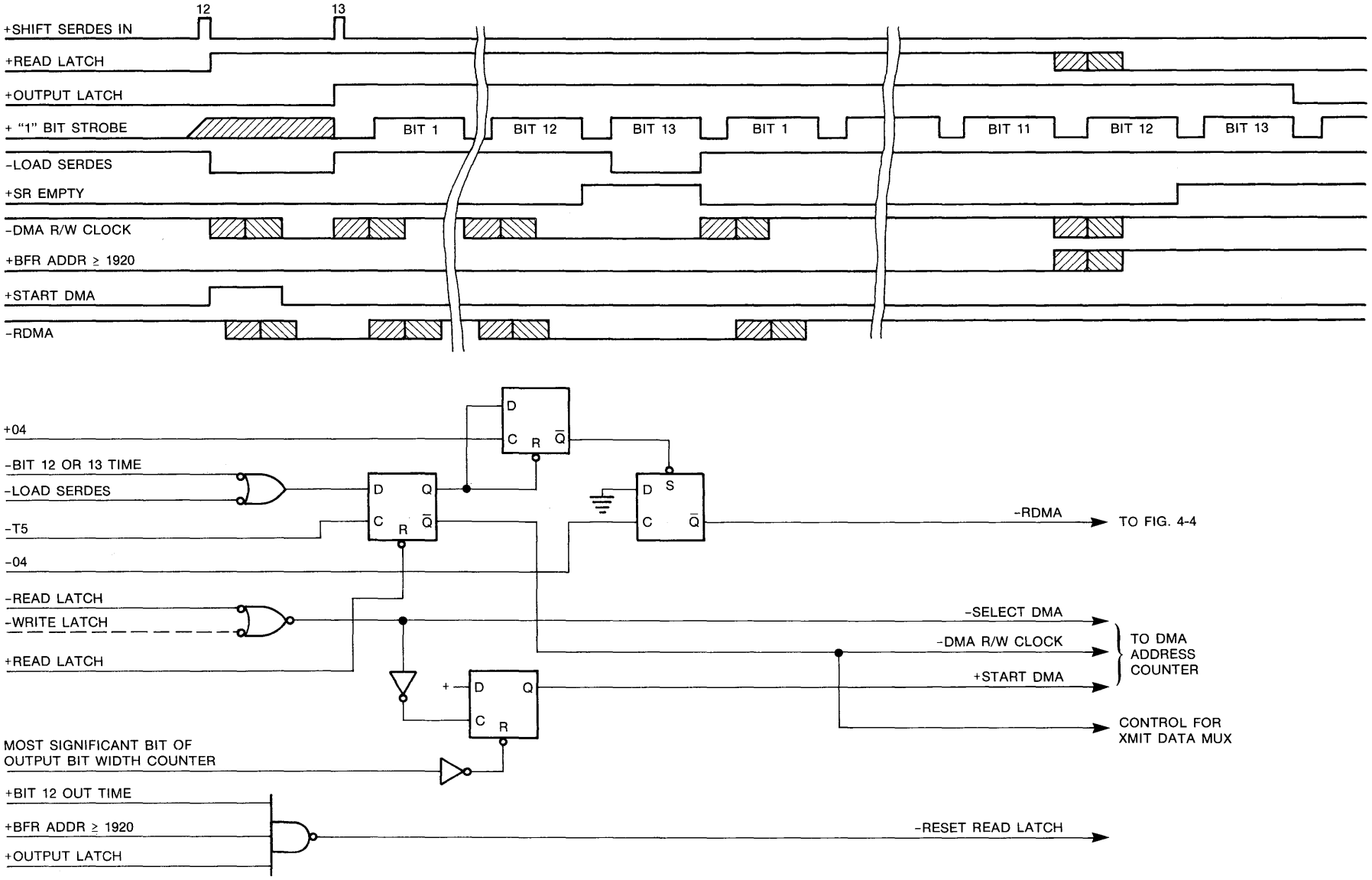

FIGURE 7-4. CONTROL FOR READ COMMAND RESPONSE

7.4 WRITE COMMAND RESPONSE

Setting the Write latch (by decoding a Write command) causes the control logic to be conditioned such that the next 1920 characters received are written sequentially into the buffer. See Figure 7-5 for the control logic and timing that relates to the WRITE command. Since the DMA Address Counter control signals (DMA R/W CLOCK, SELECT DMA, and START DMA) are quite similar to those for the Read command, no further explanation will be given in this section. The RESET SERDES signal, which is generated for all received characters except Read and Poll commands) clears the Serdes so that the next character can be deserialized.

Valid (deserialized) data appears at the output of the Serdes only during the +DATA CHAR IN strobe; therefore, data must be written into the buffer during this period or it will be lost. The +DATA CHAR IN strobe, which is asynchronous with the buffer cycle, is used to generate another signal which is synchronized with the buffer cycle. This signal is then used to generate proper timing for the R/W line which actually controls writing data into the buffer. The bit rate of the received coax signal (in a 3270 system) is such that valid data will always remain long enough to be written into the buffer, even though the coax and the buffer cycles are asynchronous with respect to each other.

7.5 ADDITIONAL COMMAND SEQUENCES

Decoding the Sound Alarm command causes a single-shot (25F on logic page DA004) to fire, generating a nominal 160-millisecond pulse. This pulse gates a vertical counter output to the speaker.

Decoding the Reset Xmit Check command (or Write command) causes the Xmit Check latch to be reset. This latch, which is one of the bits of the status word, is set only if a character is received with incorrect parity.

Decoding the Read Poll command causes both the Poll and CU Busy latches to be set. See Section 7.2 for the Poll latch sequence. The CU Busy latch being set or any of the other seven latches of the command register, causes the generation of a nonmaskable interrupt (NMI) to the MPU (see logic page DA007). The leading edge of the NMI signal causes the MPU to switch to its NMI routine. This software routine instructs the MPU to (among other things) read the command register and execute subroutines based upon which bits are set. The CU BUSY bit inhibits further processing of keyboard input in anticipation of a Read or Write command, which has priority for buffer access over the operator.

The remainder of the commands (Restore Sys Avail, Unlock Kbd, EAU, and Reset Info Pending) are decoded and used to set the corresponding latch in the command register (see logic page DA007). The action initiated by each is described in Section 6.3.

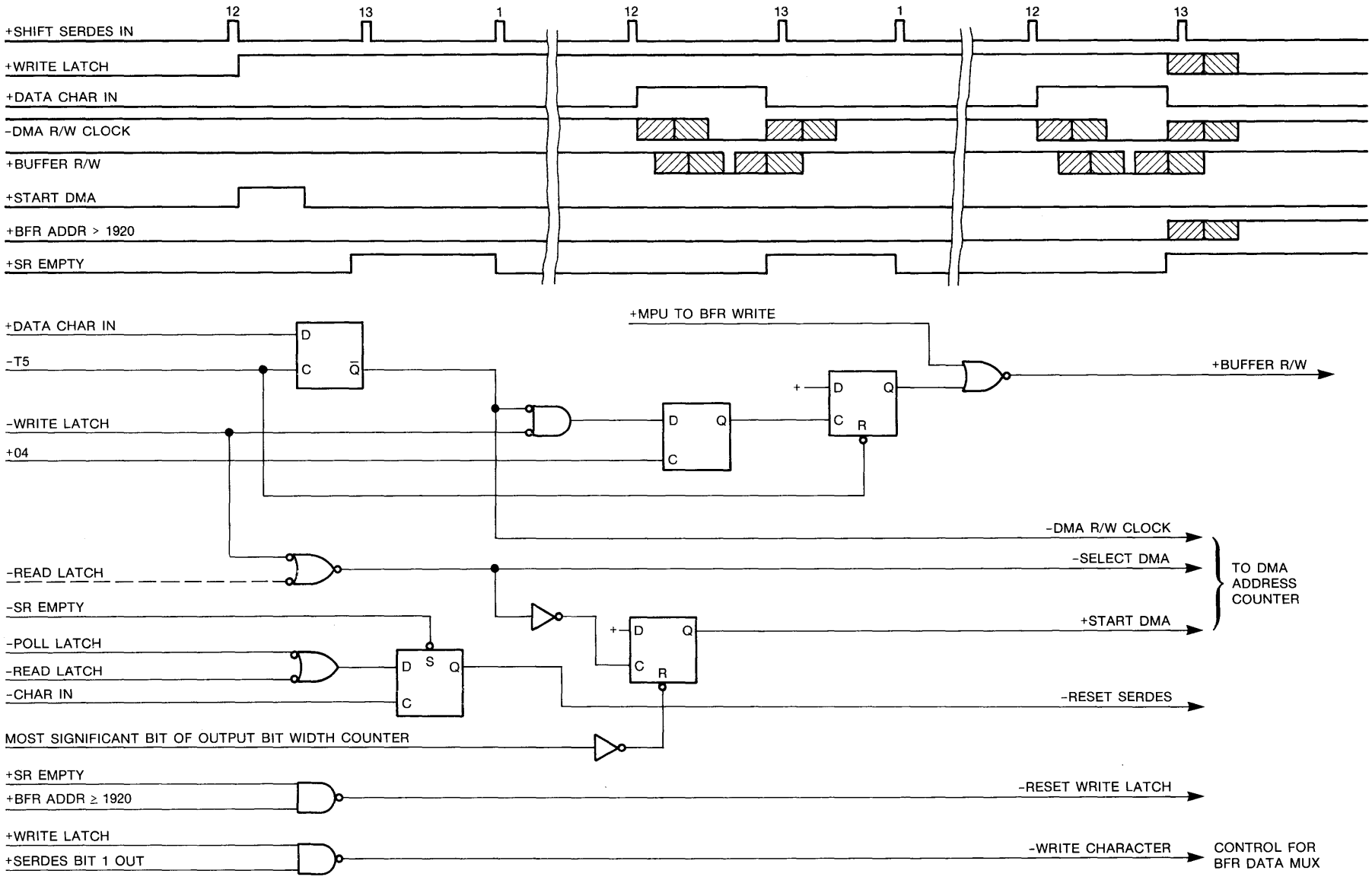

FIGURE 7-5. CONTROL FOR WRITE COMMAND RESPONSE

SECTION 8
INITIALIZATION SEQUENCE

Application of power to the 1377 logic causes the POR signal to reset hardware registers and latches. Termination of the POR pulse causes the MPU to start executing instructions stored in the read-only memory (ROM). The first routine executed by the MPU is that of initializing the PIA's, the statis RAM, and the buffer. First, it is necessary to define the stack pointer address as 0039_{hex} so that the first 58 bytes of the status RAM may be used by the MPU for temporary storage of subroutine and interrupt information. Then various constants are moved from ROM to the status RAM.

The internal registers of PIA #1 and PIA #2 must be initialized to determine which PIA I/O lines are inputs and which are outputs, and to determine which lines will generate interupts to the MPU. The most significant buffer address bit (one output from PIA #2) is set according to the setting of one of the option switches; this allows the upper 2K of the buffer to be used if any bad bits exist in the lower 2K. Additional option switches (inputs to PIA #2) are read to control which keyboard code translate table will be used. Software flags are cleared.

The buffer is cleared (both data and cursor) and the cursor is written to the first position. Then line 25 is cleared and the indicator legends are written to line 25. Software pointers and flags are set up for the initial screen format. Clearing the command register causes parity checking at the buffer output to begin. A software timing loop waits while the CRT refresh circuitry cycles through memory. If no parity error occurs during the timing loop, the audible alarm sounds, the keyboard is unlocked, interrupts are enabled, and operator input may commence.

SECTION 9
PARITY GENERATION AND CHECKING

9.1 COAX PARITY CHECKING

Parity of the received data is checked as the character is being deserialized. The Rec Parity flip-flop (see logic page DA008) is held set any time the Serdes is empty. The flip-flop is then toggled for each logic one that is received. When the twelfth bit is received, the flip-flop will be set if no parity error occurred. The Rec Parity flip-flop output is used to inhibit the decoding of any control character if a parity error occured; data characters with parity errors are written into the buffer as nulls. Note that a parity error in any received character will set the Xmit Check latch.

9.2 COAX PARITY GENERATION

Parity of the transmitted data is generated serially as data is shifted out of the Serdes. The Xmit Parity flip-flop (see logic page DA008) is reset when the Serdes is loaded and is toggled each time a logical one is read out of the Serdes. During the twelfth bit time, the output of the Xmit Parity flip-flop is transmitted. Note that the first and twelfth bits out of the Serdes are always logical ones; therefore, the flip-flip is toggled at least twice. Also note that the parity bit ensures odd parity for bits one through twelve; bit thirteen is not included in parity.

9.3 PARITY GENERATION FOR BUFFER INPUT DATA

Parity for data written into the buffer is generated in parallel by chip 23B (see logic page DA004). Note that odd parity is generated for the eight data bits and the cursor bit (IMB 8) is not included in parity.

9.4 PARITY CHECKING FOR BUFFER OUTPUT DATA

Parity is checked in parallel at the buffer output by chip 7B (see logic page DA009). Since data is valid only near the end of a memory cycle, a latch is clocked by the trailing edge of Ø4 to sample the output of the parity check circuit. If the BFR Parity Check latch ever gets set, it turns on the Device Check latch. Again note that the cursor bit (OMB 8) is not included in parity. Parity checking is inhibited while data is being written into the buffer, since data out is undefined during this time. Parity checking is also inhibited after POR until the buffer is cleared because the random data at power-on would certainly have (meaningless) parity errors. Finally, parity checking is inhibited for addresses above 1919 because this information is not part of the data that can be rewritten by the CU.

APPENDIX

GENERAL DEFINITIONS AND ABBREVIATIONS

AID
attention identification code (bits 7-11 of the status word).

ATTRIBUTE
one of 32 control characters which defines the characteristics of all data following it up to, but not including, the next attribute character. Characteristics include display vs. nondisplay, normal vs. high intensity, unprotected vs. protected, light pen detectable vs. not light pen detectable, and alphanumeric vs. numeric. Attributes are displayed as blanks.

BUFFER
the dynamic RAM memory that is used to store the data which is displayed on the CRT.

CRT
cathode ray tube.

CU
control unit (IBM 3271 or 3272 or equivalent).

DMA
direct memory access (hardware data transfer into or out of the buffer, as opposed to the MPU transferring (under software control) data into or out of the buffer).

EAU
erase all unprotected (reset to nulls all unprotected information on the screen).

EPROM
eraseable/programmable read-only memory (TI TMS 2708 or equivalent).

MDT
modified data tag (one bit of the attribute character which indicates modification of the data in the previous field by the display operator).

MPU
microprocessor (Motorola MC6800 or equivalent).

PIA
peripheral interface adapter (Motorola MC6820 or equivalent).

ROM
read-only memory (typically used to store the software which controls the MPU).

SERDES
serializer/deserializer (the three 4-bit shift register chips connected together to form a 12-bit shift register. It is used to serialize characters to be transmitted and deserialize characters that are received.)

WRAP
(as applied to a field defined by an attribute character) the process whereby the field continues from the end of one line to the beginning of the next line (or from the end of the 24th line to the beginning of the first line).

SIGNAL NAME ABBREVIATIONS AND DEFINITIONS

CA0-CA10
CRT refresh counter address bits 0 through 10.

IMB0-IMB8
input memory bits 0 through 8 (input data to the buffer).

INITIALIZE
signal generated after POR to inhibit coax I/O and buffer parity checking until after the MPU has completed its initialization routine.

IRQ
interrupt request (to the MPU).

KB0-KB7
keyboard bits 0 through 7 (data bits from the keyboard).

NMI
nonmaskable interrupt (to the MPU).

OMB0-OMB8
output memory bits 0 through 8 (data read out of the buffer).

OMB0
least significant data bit

OMB6
most significant data bit

OMB7
attribute bit

OMB8
cursor bit

PMA
processor memory access (signal generated to indicate that the MPU is accessing the buffer).

POR
power-on-reset (reset pulse of aproximately 800 milliseconds generated when power is first applied).

RA0-RA15
repowered (MPU) address bits 0 through 15. RA15 is the most significant bit and RA0 is the least significant bit.

RDMA
read direct memory access (a signal used to stretch the chip enable clock to the dynamic ram chips so that valid data appears at the buffer output long enough to load the Serdes).

VMA
valid memory address (MPU output used for address decoding).

1377 INTERNAL ADDRESS ASSIGNMENT

Address (Hex)	Contents
0000-007F	Static RAM—128 bytes address bit A7 low selects RAM
0080-00FF	PIA #2 address bit A7 high selects PIA #2
1000	PIA #1 A side: Keyboard interface (CA1=strobe, CA2=not used) data lines are positive logic; interrupts CA1 and CA2 are active low B side: Status Register Bits 0-4 are the AID code (positive logic with Bit 4 as MSB and bit 0 as LSB) Bit 5 is Info Pending (active low) Bit 6 is Device Busy (active low) Keyswitch F1 goes to bit 7 (active low) Light pen interrupt is CB1 (active high) CB2 causes alarm to sound (active low)
2000	Command Register—any bit on generates a Non-Maskable Interrupt (NMI) to the MPU Bit 0 Restore system available indicator Bit 1 Unlock keyboard Bit 2 Erase All Unprotected (EAU) } Reset by MPU* Bit 3 Reset Info Pending status bit Bit 4 Device Check Latch (bad parity in CRT memory) Bit 5 Write Latch Bit 6 Read Latch } Reset by hardware Bit 7 CU Busy Latch (inhibits KBD operation)
3000	4K byte dynamic RAM for CRT display (only 2K is used)
4000	4K bit dynamic RAM for CRT cursor (only 2K is used)
5000	Light pen register—high-order 3 bits (bit 2=MSB, bit 0=LSB)
5001	Light pen register—low-order 8 bits (bit 7=MSB, bit 0=LSB)

*EAU also reset by device going on.

1377 INTERNAL ADDRESS ASSIGNMENT (Cont.)

Address (Hex)	Contents
6400	1K bytes of EROM } OR 2K bytes of ROM
6800	1K bytes of EROM } OR 2K bytes of ROM
7400	Provision for two 1K byte EROMs if
7800	2K ROM is in address 6400
8000-FFFF	1K byte EROM or (future off board expansion to 32K bytes of ROM/RAM/EROM/PROM)

BIT ASSIGNMENTS FOR PIA #2

PB0 (S3)
PB1 (S4)
PB2 (S5)
PB3 (S6) } Select country/keyboard
PB4 (S7) KBD numeric lock special feature (enable = high)
PB5 (S8) Select upper/lower 2K of memory at initialization
PB6 F2 key on keyboard
PB7 F3 key on keyboard

PA0 Output controlling upper/lower 2K of Memory

PA1 Numeric shift out (from KBD) (active low)
PA2 Upshift input (to KBD) (active low)
PA3 Alpha shift out (from KBD) (active low)
PA4 Unused
PA5 (S1) Spare
PA6 (S2) Translate (switch on = active low) translate 3 LC char
PA7 Unused

CA2 Pin 11 on DE KBD
CB1 Pin n on DE KBD

CA1 Write latch (low to high transition input)
CB2 Reset Device Check (active low output)

ATTRIBUTE CHARACTER BIT DEFINITIONS

Attribute						Coax Data Word Bit Position						
Protect	Alpha/ Numeric	MDT On	High Intensity	Sel. Pen Det.	Non-display	6	7	8	9	10	11	Char.
U	A					0	0	0	0	0	0	SP
U	A	Y				0	0	0	0	0	1	A
U	A			Y		0	0	0	1	0	0	D
U	A	Y		Y		0	0	0	1	0	1	E
U	A		Y	Y		0	0	1	0	0	0	H
U	A	Y	Y	Y		0	0	1	0	0	1	I
U	A				Y	0	0	1	1	0	0	<
U	A	Y			Y	0	0	1	1	0	1	(
U	N					0	1	0	0	0	0	&
U	N	Y				0	1	0	0	0	1	J
U	N			Y		0	1	0	1	0	0	M
U	N	Y		Y		0	1	0	1	0	1	N
U	N		Y	Y		0	1	1	0	0	0	Q
U	N	Y	Y	Y		0	1	1	0	0	1	R
U	N				Y	0	1	1	1	0	0	*
U	N	Y			Y	0	1	1	1	0	1	)
P	A					1	0	0	0	0	0	-
P	A	Y				1	0	0	0	0	1	/
P	A			Y		1	0	0	1	0	0	U
P	A	Y		Y		1	0	0	1	0	1	V

ATTRIBUTE CHARACTER BIT DEFINITIONS (Cont.)

Attribute						Coax Data Word Bit Position						
Protect	Alpha/ Numeric	MDT On	High Intensity	Sel. Pen Det.	Non-display	6	7	8	9	10	11	Char.
P	A		Y	Y		1	0	1	0	0	0	Y
P	A	Y	Y	Y		1	0	1	0	0	1	Z
P	A				Y	1	0	1	1	0	0	%
P	A	Y			Y	1	0	1	1	0	1	—
P	S					1	1	0	0	0	0	0
P	S	Y				1	1	0	0	0	1	1
P	S			Y		1	1	0	1	0	0	4
P	S	Y		Y		1	1	0	1	0	1	5
P	S		Y	Y		1	1	1	0	0	0	8
P	S	Y	Y	Y		1	1	1	0	0	1	9
P	S				Y	1	1	1	1	0	0	@
P	S	Y			Y	1	1	1	1	0	1	'

U = Unprotected field
P = Protected field
S = Skip over field
A = Alphameric field
N = Numeric Field
Y = Yes

DISPLAYABLE CHARACTER SET (for U.S.)

BITS 3 2 1 0	HEX 1	000	001	010	011	100	101	110	111
		0	1	2	3	4	5	6	7
0 0 0 0	0	NUL	∞	≈	0	SP	&	-	0
0 0 0 1	1	a	j	Σ	1	A	J	/	1
0 0 1 0	2	b	k	s	2	B	K	S	2
0 0 1 1	3	c	l	t	3	C	L	T	3
0 1 0 0	4	d	m	u	4	D	M	U	4
0 1 0 1	5	e	n	v	5	E	N	V	5
0 1 1 0	6	f	o	w	6	F	O	W	6
0 1 1 1	7	g	p	x	7	G	P	X	7
1 0 0 0	8	h	q	y	8	H	Q	Y	8
1 0 0 1	9	i	r	z	9	I	R	Z	9
1 0 1 0	A	μ	π	≤	™	¢	!	¦	:
1 0 1 1	B	{	[	≥	®	.	$	,	#
1 1 0 0	C	°	\	÷	©	<	*	%	@
1 1 0 1	D	}	]	-	▪	(	)	—	'
1 1 1 0	E	↑	→	±	~	+	;	>	=
1 1 1 1	F	↓	←	×	^	|	¬	?	"

BITS 6 5 4

HEX 0

NUL 4 SP ARE BLANK

RELATIONSHIP BETWEEN COAX DATA WORD AND BUFFER DATA WORD

Buffer Memory Bit #	COAX Data Word Bit #	Definition for Alphanumeric Character	Definition for Attribute Character
P	12	Parity	Parity
0	11	LSB	MDT bit
1	10		Always zero
2	9	Data	00 = Normal Intensity/Not L.P. Detectable
3	8	Character Code	10 = Normal Intensity/L.P. Detectable 01 = Intensified/L.P. Detectable 11 = Nondisplay/Not L.P. Detectable
4	7		Alphanumeric/Numeric
5	6		Unprotected/Protected
6	5	*MSB	Not used
7	4	Always Zero	Always one
8	3	Cursor Bit	Cursor Bit
-	2	Always zero	Always zero
-	1	Always one	Always one

* 1 = upper case
* 0 = lower case

COMMENTS FORM

1377 Display Station Theory of Operations—1377.21-00

Please send us your comments; they will help us produce better publications. For our reference, please include publication number, revision level, and page number. When applicable, reference specific paragraph numbers. Possible areas to comment on: accuracy, clarity, organization, audience suitability, and illustrations.

DATE _____

NAME _____

MAILING ADDRESS _____

_____

_____

TELEPHONE _____

TELEX _____

PUBLICATIONS DEPARTMENT USE ONLY

_____
TECHNICAL REVIEWER

DATE _____

DISPOSITION _____

_____

RESPONSE SENT

DATE _____

MEMOREX

First Class

Permit No. 919
Santa Clara
California
95050

Business Reply Mail

No Postage Necessary if Mailed in the United States

Postage Will Be Paid By

Memorex Corporation

Publications Department
Mail Stop 14-32
San Tomas at Central Expressway
Santa Clara, California 95052