7200/7300 Processing Unit

Maintenance Manual

2601.001-01

MEMOREX

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PREFACE

This manual contains installation, operating, instructions, and maintenance information for the Memorex 7200/7300 Processing Unit for use by Memorex Field Engineers. The manual is organized as follows:

Section 1, Introduction, discusses the scope and intended use of the manual.

Section 2, Installation, contains unpacking instructions, procedures for connecting each peripheral subsystem or device to the Processing Unit, and a post-installation checkout procedure.

Section 3, Operating Data and Procedures, describes all controls and indicators on the System Control Panel, plus some of the more commonly used operating procedures using this Panel.

Sections 4 through 11 cover maintenance of all assemblies comprising the Processing Unit, including shared resources, power supplies and sequencer circuits, and integrated adapters for I/O processors. (Maintenance information about a particular peripheral device connected to the Processing Unit can be found in separate maintenance manuals for each device listed on the following page.) These eight sections can be divided into two general areas: "memory-jogging" maintenance aids, such as instruction repertoires and conversion tables, which apply to the complete Processing Unit (Section 4 and 5); and specific maintenance information relating to each assembly of the Processing Unit, such as shared resources and integrated adapters (Sections 6 through 11).

As a prerequisite for making maximum use of this manual, the reader should be thoroughly familiar with the 7300 Processing Unit Design Description Manual, Volumes I through IV (Publications Numbers 2501.001 through 2501.004).

This manual is designed for use with other related documents to provide a complete maintenance support package for the entire MRX/40/50 System. These manuals are listed on the following page by both title and number. The six-digit number (xxxxxx) is an Engineering Part Number and the seven-digit number (xxxx.xxx) is a Publications Number.

506109	MRX 7200/7300 Processing Unit Support Diagrams Manual, Volumes 1, 2, and 3
2801.001	7300 Processing Unit Illustrated Parts Catalog
2680.010	8010 Card Reader Model 001 Maintenance Manual
2680.020	8010 Card Reader Model 002 Maintenance Manual
2680.030	8010 Card Reader Model 003 Maintenance Manual
2581.001	8025 Card Reader/Punch Theory of Operation/ Diagrams/Maintenance Aids
2681.001	8025 Card Reader/Punch Maintenance Manual
2881.001	8025 Card Reader/Punch Illustrated Parts Breakdown
2650.001	5120 Printer Maintenance Manual
2850.001	5120 Printer Diagrams/Parts List
2630.001	3237 Magnetic Tape Transport Model II NRZI Operation and Servicing Manual
2830.001	3237 Magnetic Tape Transport Model II NRZI Illustrated Parts Breakdown
2645.001	3664 Maintenance Manual
203516	3664 Logic Diagrams Manual
2845.001	3664 Illustrated Parts Catalog
804011A	1240 Maintenance Manual
2861.001	1240 Illustrated Parts Catalog
2610.002	MRX/40 and 50 Systems Field Support Site Planning Manual

SECTION 1. INTRODUCTION

SCOPE OF MANUAL

The 7200/7300 Processing Unit Maintenance Manual provides information necessary to install, operate, and maintain the 7200 and 7300 Processing Units used in the Memorex (MRX) 40 and 50 Systems, respectively. The Processing Unit is the system central processing unit, performing all necessary computing and control functions required by the System. The main intent of this manual is to provide information about the Processing Unit only; however, some details of the peripheral devices that connect to the Processing Unit are also provided in the installation section. Diagnostic programs referenced in this manual also check functions of the peripheral devices as well as those of the Processing Unit. Hardware-oriented maintenance contained in this manual, however, is restricted only to logic present in the Processing Unit. Information required to maintain the peripheral devices which are separate from the Processing Unit is found in applicable peripheral device manuals referenced in the Preface.

RELATION TO SUPPORT DIAGRAMS MANUAL

This maintenance manual has been written to complement as much as possible the MRX 7200/7300 Processing Unit Support Diagrams Manual to provide an integral maintenance package for the Processing Unit. The Support Diagrams Manual contains all logic and schematic diagrams for the Processing Unit, plus many supplementary maintenance-oriented diagrams such as block diagrams and register formats. These drawings are contained in three volumes, with the supplementary diagrams contained in the first half of Volume 1 and the power schematics and logic diagrams contained in the second half of Volume 1, and Volumes 2 and 3. If a particular maintenance-oriented diagram is already in the Support Diagrams Manual, it is not repeated here; instead, a reference is made to the drawing in the Support Diagrams Manual by both the drawing number and the volume in which it is located. For information about the conventions and symbology used in the Support Diagrams Manual, refer to the introduction in the manual.

DIFFERENCES AMONG MODELS AND FEATURES

Maintenance information in this manual is applicable to both the 7200 and 7300 Processing Units, Versions 4 (60 Hz only) and 5 (50 or 60 Hz), with any or all features present. Differences between the 7200 and 7300 models, versions 4 and 5, and the presence or absence of particular features are called out on applicable PC module location maps in the Support Diagrams Manual and in appropriate locations in this manual.

SECTION 2. INSTALLATION

This section contains information for installing the MRX/40/50 System at the customer's site. Subjects covered are: site preparation, unpacking, cable connections, and post-installation checkout.

SITE PREPARATION

PRE-INSTALLATION CHECKS

Prior to installing the system, the installation site should be checked to verify that all facility requirements conform to those specified in the MRX/40 and 50 Systems Field Support Site Planning Manual and the customer's particular site plan. These requirements are shown in Figure 2-1 and summarized in the following paragraphs.

Air Conditioning - Humidity Control

Optimum operating conditions for the facility are 70 degrees F (21 degrees C) and 50% relative humidity under conditions of actual operation. The specified temperature and humidity optimum must be maintained at all times, including non-operating hours. Refer to the Site Planning Manual for detailed specifications for each device in a particular customer's system.

Primary Power - Facility Grounding

The facility power system should conform to that specified in the Site Planning manual with special emphasis on facility grounding. Each required receptacle should be inspected for grounding, electrical short, and correct phase rotation prior to turning power on. The power system should conform in general to the examples shown in the Site Planning Manual for 60 Hz and 50 Hz systems. Have the customer correct any input phasing problems.

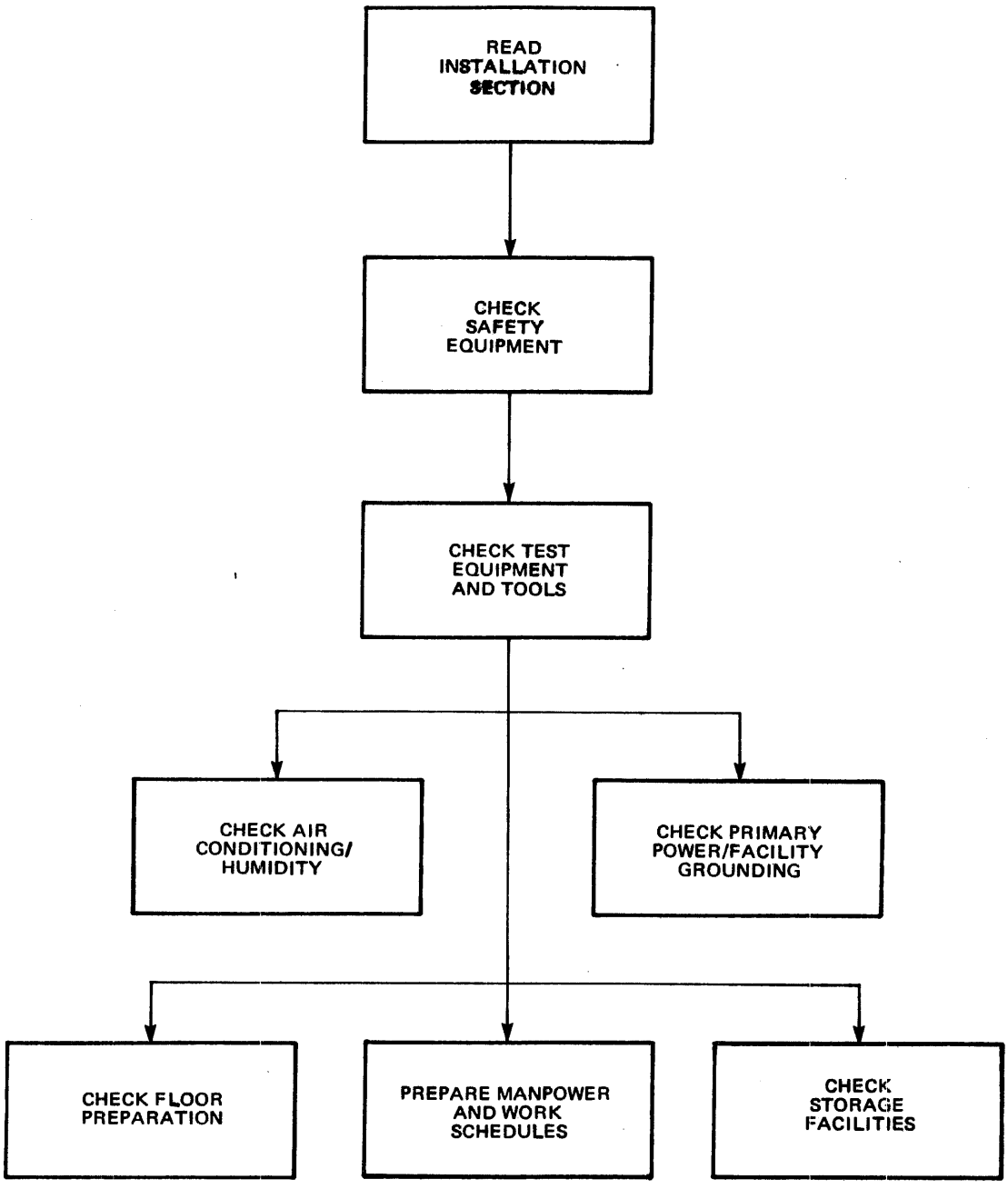

Figure 2-1. Pre-installation Sequence

Floor Preparation

If the facility is equipped with a raised floor, check that the cable cutouts or raceway match the approved floor plan. If the area under the raised floor is used as an air plenum, make sure the customer has adequately cleaned the area, including vacuuming if necessary. Also check that the customer has removed any sharp edges from cable ducts to prevent personnel injuries or cable damage. Underfloor cables should be installed before the units are positioned.

Storage Facilities

Customer storage facilities should be checked to insure that the facilities are suitable for file storage and offer adequate security and fire protection. The FSR storage area should be checked to insure that adequate space has been provided for equipment storage and the required number of convenience receptacles are present.

Special Tools and Test Equipment

In addition to the standard FSR tools and test equipment, the following special tools and test equipment will be useful for pre-installation checking.

- Oscilloscope, Tektronix Model 422
- AC Voltmeter (1/2% accuracy or better)
- Sling Psychrometer
- Three-foot carpenter's level

Manpower Allocation

A sample guide for manpower assignments is shown in Table 2-1. The times shown are for a system composed of three disc drives, three tape units, one card reader/punch and one printer. The system is assumed to have no unforeseen technical problems and all pre-installation preparations are assumed to be complete. In addition, the time estimate is based on installation by personnel familiar with the MRX/40/50 system, two men to a shift.

TABLE 2-1. SAMPLE MANPOWER ALLOCATION

ACTIVITY	DURATION (HRS.)
Supervise unloading	4
Unpack and position equipment	8
Install sub-floor cabling	8
Connect cabling	2
Perform voltage checks	6
Perform off-line checks	4
Perform micro-diagnostics	8
Perform diagnostics	12
Perform system check	4
Install skins and covers	4

Sample System Contains:

3 Disc Drives
3 Tape Units
1 Card Reader/Punch
1 Printer

SYSTEM CABLING DATA

All cables are shipped in the same container with their respective "FROM" unit*. The documentation supporting the cable shipment is contained in the packing list attached to the outside of the processing unit shipping container.

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*The "FROM" unit is the most remote device by cabling from the Processing Unit. This convention applies to all types of cables except primary cords and signal cabling for communications equipment. See Section 6 of the Field Support Site Planning Manual for more details.

Cable Identification

System cables are identified by part number tags attached near both ends of each cable. A third tag denoting the engineering change (EC) level of the cable is attached near one end of the cable (see Figure 2-2). After removing all cables from their respective cartons, check them against the shipping list and the system requirements. Damaged or omitted cables should be reported to the field manager.

Terminations

The last device on the disc multiplex cable and the last device on both selector channels (bus and tag cables) must be terminated. The bus and tag cable terminator part numbers are 700063 and 700064, respectively. The multiplex cable terminator part number is 203202. Bus tag, and disc multiplexer cable terminators are shipped inside the Processing Unit table.

Cable Placement

Sub-floor cables must be installed prior to positioning the equipment. Cables to be installed at floor-level should be sorted and routed between equipment after positioning. Cables at floor-level will require protective ramps. Place bus and tag cables so that a dark plug will connect to a light receptacle and vice versa (see Figure 2-2).

System Grounding Cables

In addition to the normal grounding provided via the I/O and power cables, a supplementary "star" grounding must be installed on each component not powered directly from the computer. "Star" grounding refers to the physical geometry of the wiring scheme. Using this technique, the computer is made the center of the system with radiating ground wires to all of the peripheral devices involved (see Figures 2-3 and 2-4).

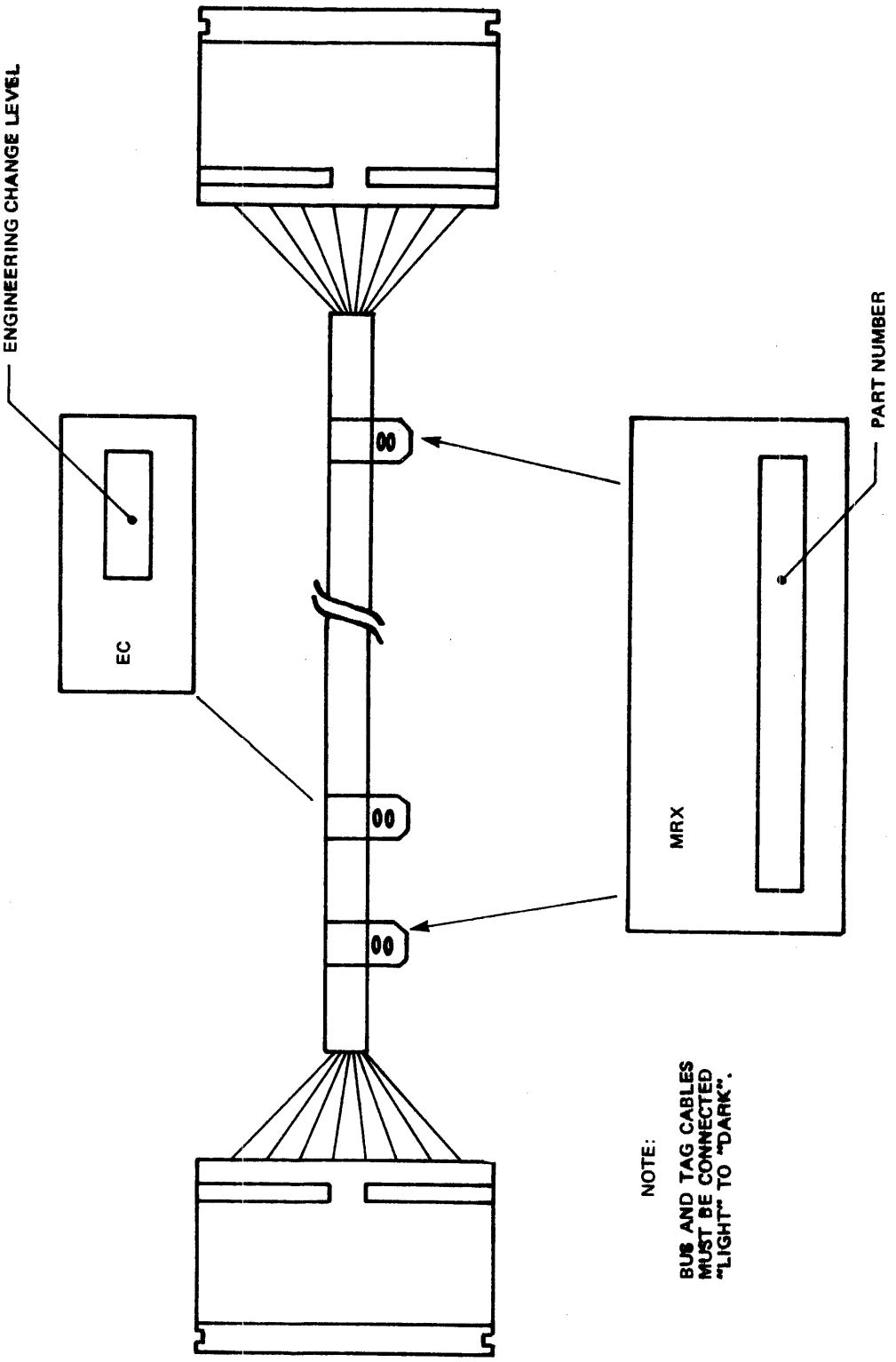


Figure 2-2. Cable Identification

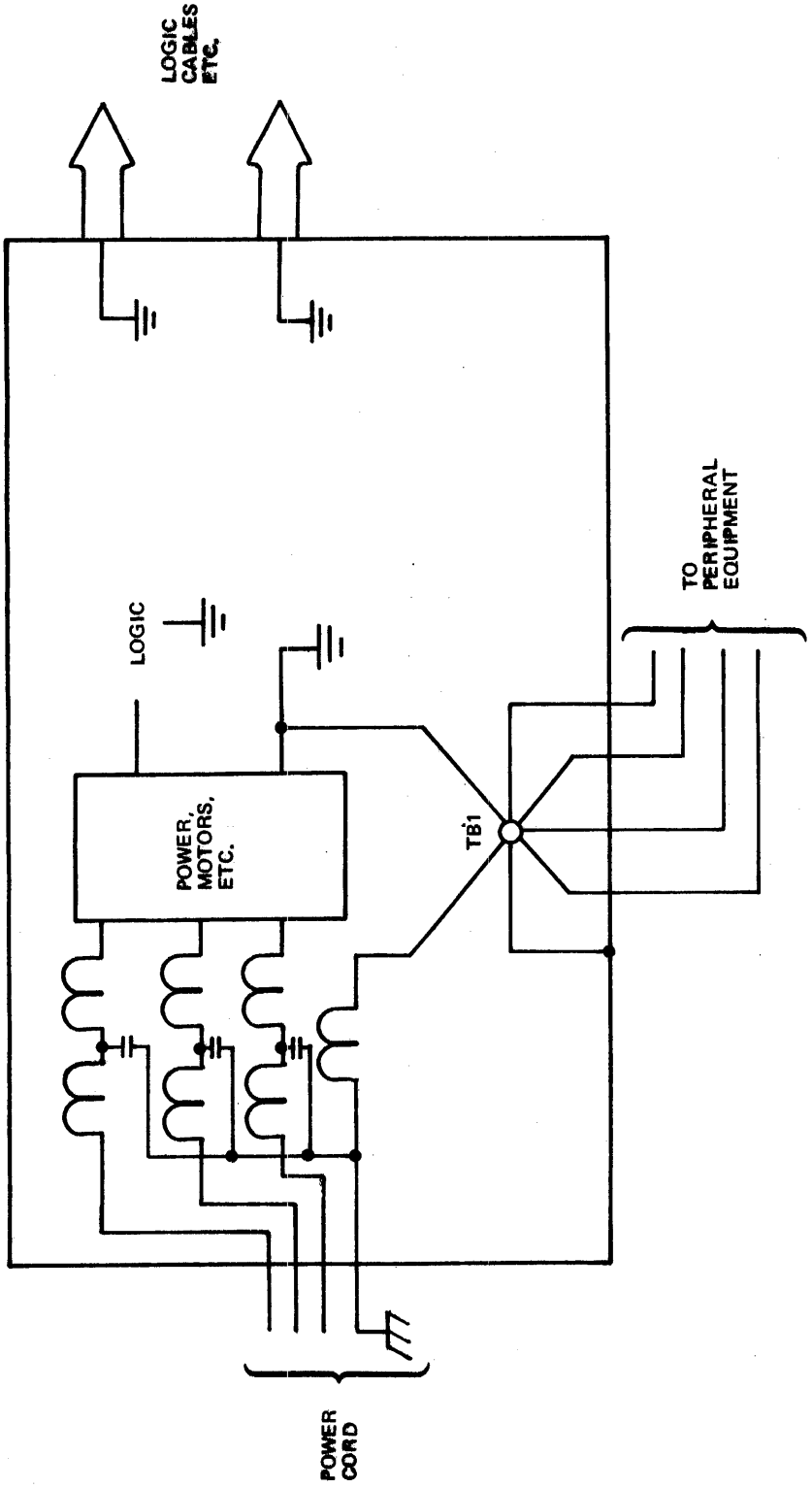


Figure 2-3. Processor Grounding Scheme

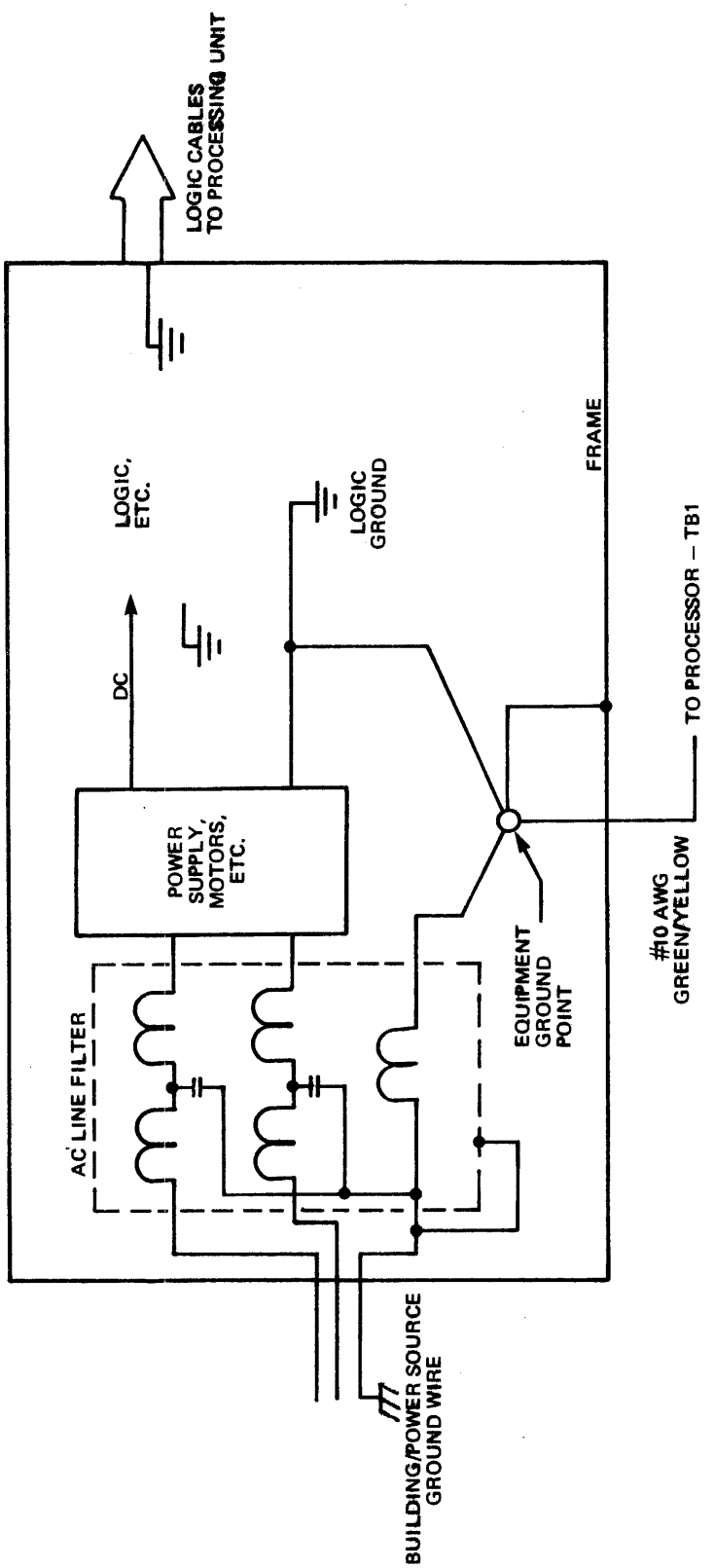


Figure 2-4. Peripheral Equipment Grounding Scheme

Input Power Transformer Adjustment

As a convenience in ordering and manufacturing machines, all supply voltage transformers in the Processing Unit are pre-tapped at the factory for an input voltage of either 208 VAC for 60-Hz machines or 220/380 VAC for 50-Hz machines. If the input voltage at the particular site is different from these two values, the transformer taps must be changed accordingly. Information for making these changes is found in the following Primary Input Voltage Adjust drawings in Volume 1 of the Support Diagrams Manual: 507092 for Version 4 machines, 507089 for Version 5 60-Hz machines, and 5070088 for Version 5 50-Hz machines. If necessary, refer to drawing 504472 in Volume 1 for locations of terminal blocks.

UNPACKING

1. Have delivering carriers or other trained personnel move packages to system site before unpacking.

2. Prior to unpacking, make an inspection of all package exteriors. If damage to exterior of package is note, contact carrier to make physical examination of damage. Carrier is required to complete a sign of damage report form. If no damage is noted, continue with next step.

3. Proceed to unpack units in accordance with unpacking instructions fastened to outside of each carton. (Small parts such as card extenders, test cards, and special set-up tools are shipped in a separate package inside the shipping carton for each unit.)

4. After unpacking each carton, inspect the unit for damage, loose or missing parts, etc. Particular attention should be paid to the following items:

   - Breakage or incorrect assembly
   - Bent, broken, or pushed out pins
   - Loose strands or wire or frayed insulation
   - Loose logic cards or incorrectly placed logic cards
   - Loose or missing nuts, bolts, or foreign objects
   - Cuts in cables
   - Improperly seated or broken indicator lamps

- Levers, knobs, and switches for proper operation

Items that cannot be repaired on site should be reported to the field manager.

5. Place equipment in locations specified by the customer's site plan.

6. Remove transport dollies under Processing Unit (Figure 2-5) as follows:

   a. Jack up rear of processing unit. (Block unit up for safety.)

   b. Remove rear processing unit dolly. Remove blocks and jack.

   c. Jack up processing unit bat wings. (Block unit up for safety.)

   d. Remove processing unit bat wing dollies. Remove block and jack.

7. Immobilize Processing Unit by screwing jack pads down and level using carpenter's level.

8. Refer to installation section of OEM manuals for any special installation instructions for the peripheral devices.

9. Before discarding packing material, examine for small parts that may have been missed. Also, do not throw away any returnable unpacking tools.

ASSEMBLY

1. Open two magnetic latches securing L-shaped door to left of System Control Panel.

2. Release two spring-lock fasteners securing Panel door on left side of door.

3. Open Panel door to gain access to large bolt hole centered behind bottom of Panel door.

4. Attach operator's table to front of CPU by means of bolt through bolt hole and two bolts in lower unit.

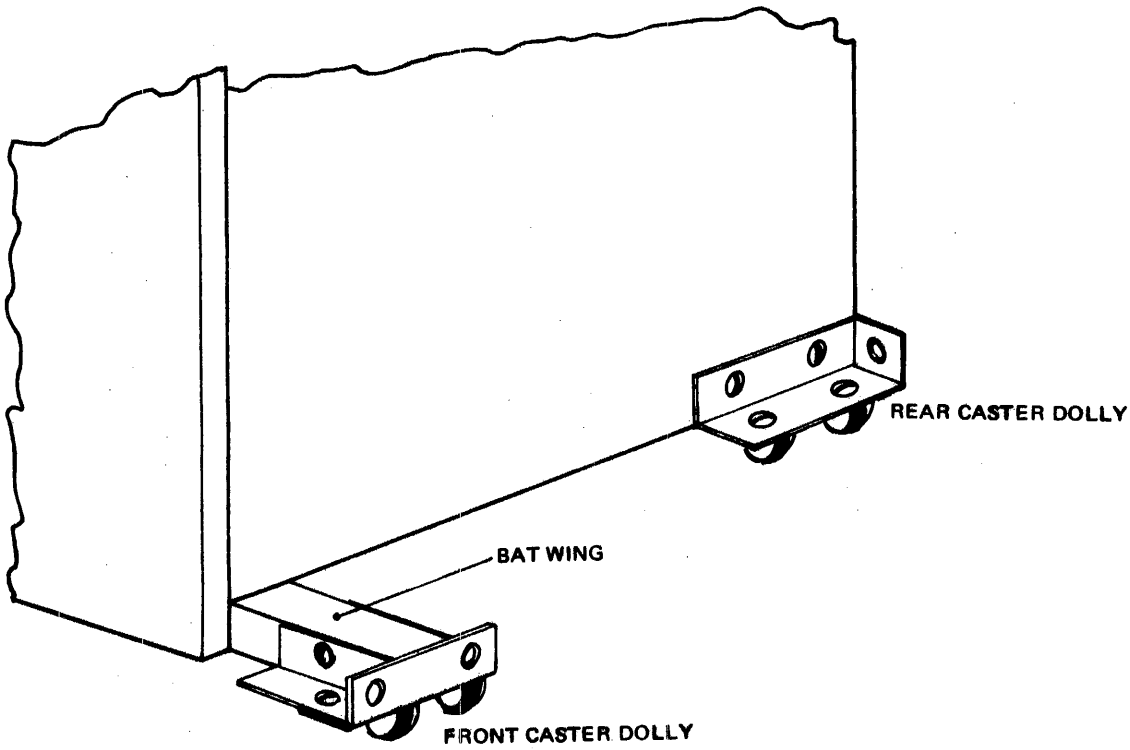


Figure 2-5. Processing Unit Transport Dollies

5. Lift top cover of card reader/punch to gain access to reader/punch assembly.

6. Locate shipping block on right side of reader/punch assembly. This block is located behind the triangular assembly mounting bracket, as shown in Figure 2-6. During shipment, this block is oriented in a downward position to immobilize the assembly, as shown in the figure. During operation, however, the block must be swung upward so that the assembly may float freely to prevent possible cracking of the frame casting during operation. Loosen screw and swing block upward.

7. Check installation of sections of card reader, tape subsystem, and disc subsystem for removing shipping blocks in these devices.

CABLE CONNECTIONS

In the following procedures, refer if necessary to Figure 4-1 for locations of all connector panels and other assemblies.

GROUND WIRE CONNECTIONS

1. Remove left side panel from processor by pulling bottom out and lifting up.

2. Raise right side panel to maximum height.

3. Remove panels that cover the I/O signal and power connectors from under operator's table. These connectors are shown in Figures 2-7 through 2-11.

4. Connect green ground wires between ground terminals on each peripheral device and individual terminals on TB01 (Figure 2-9). Locations of ground terminals on each peripheral device are shown in Figures 2-12 through 2-17. All terminals on TB01 may be used except terminal 1.

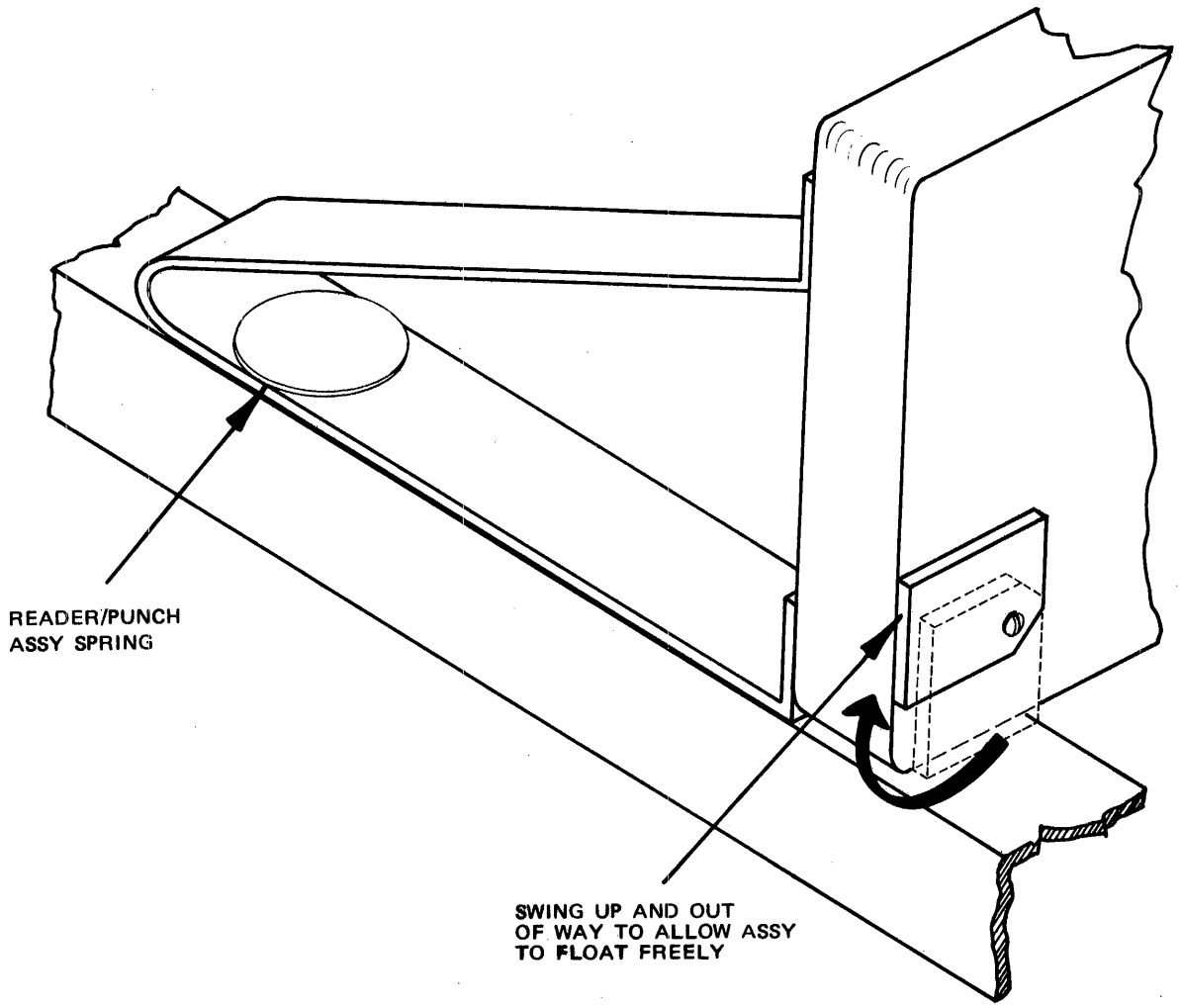


Figure 2-6. Card Reader/Punch Shipping Block

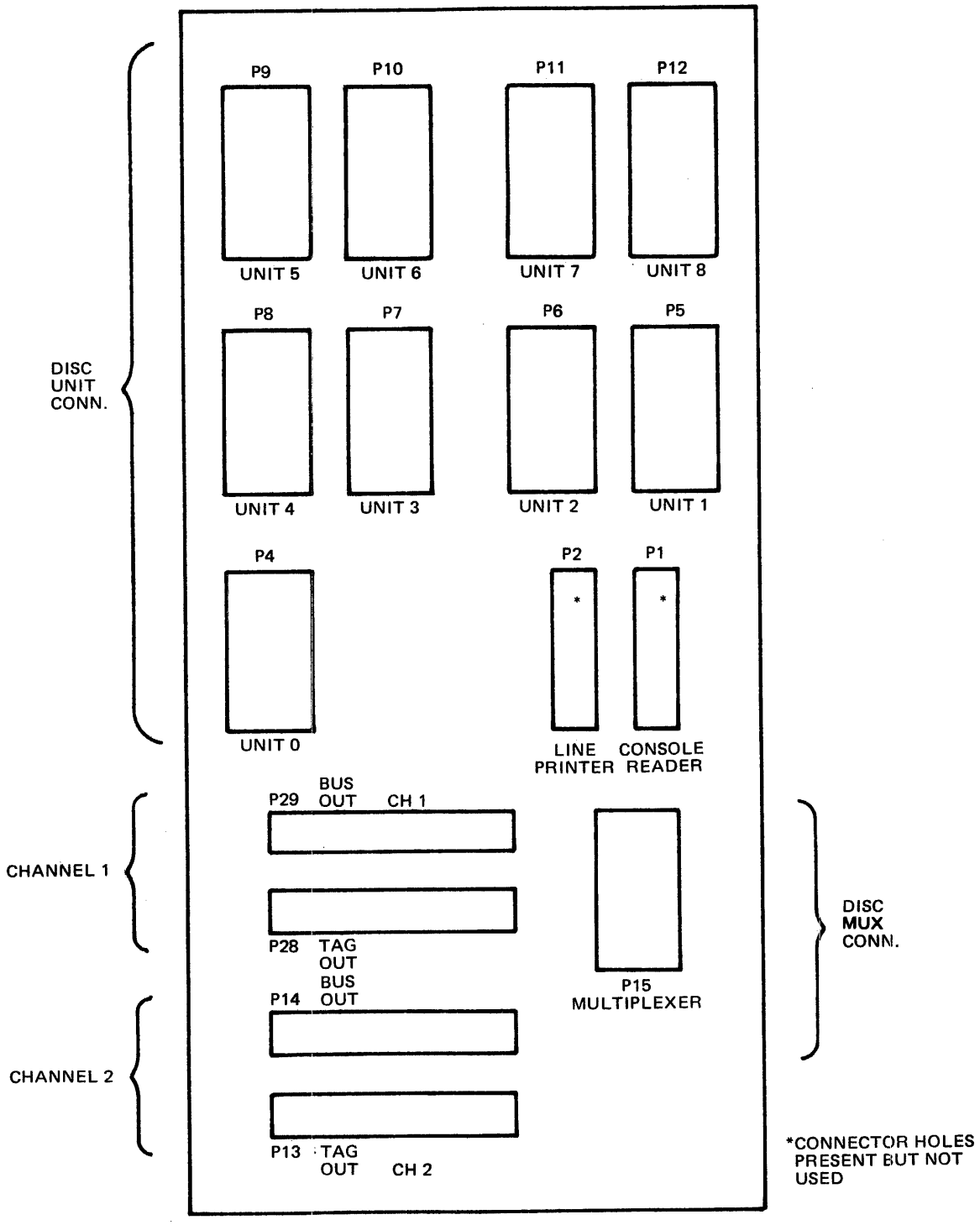


Figure 2-7. I/O Panel

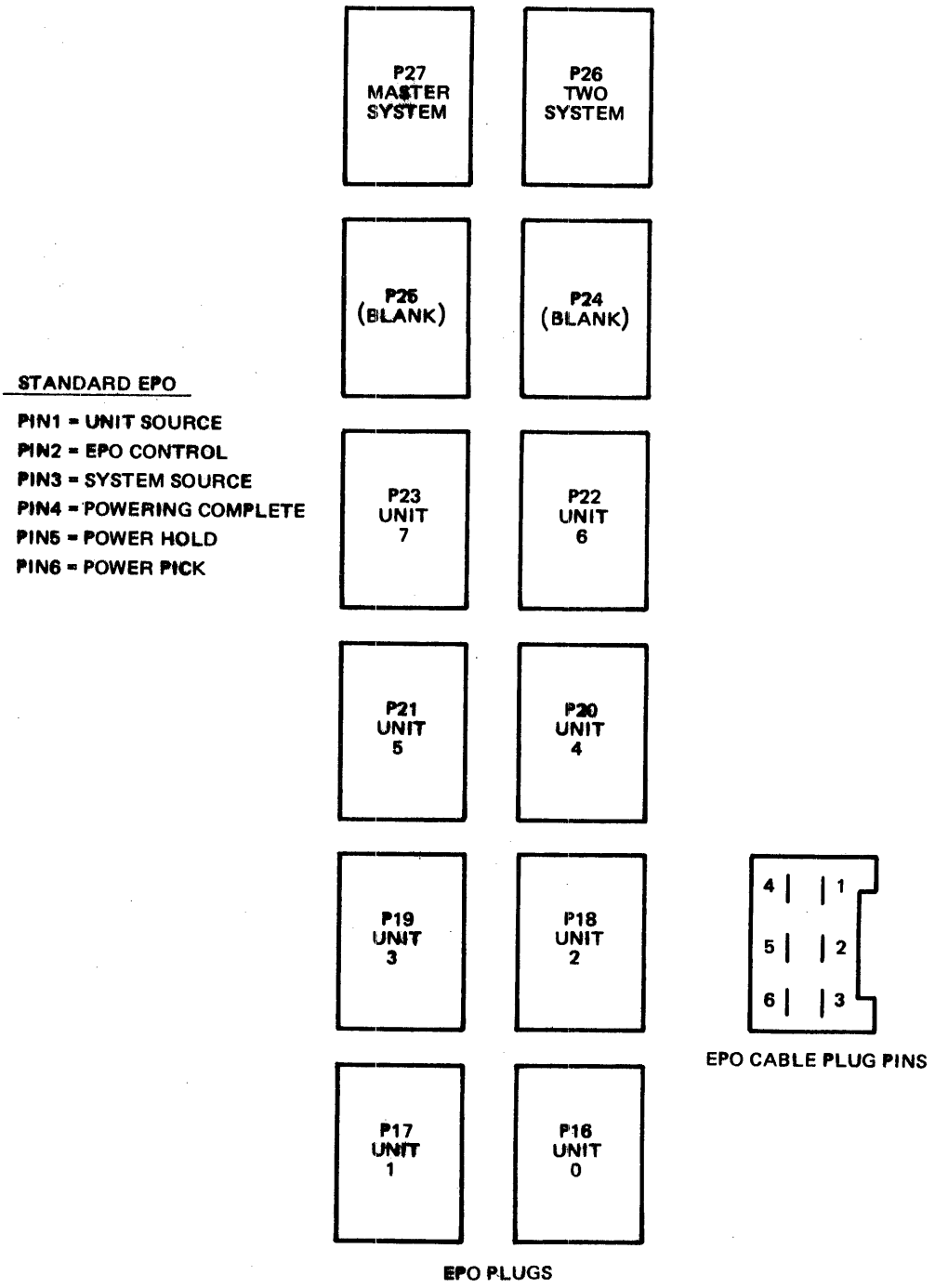


Figure 2-8. EPO Distribution Panel

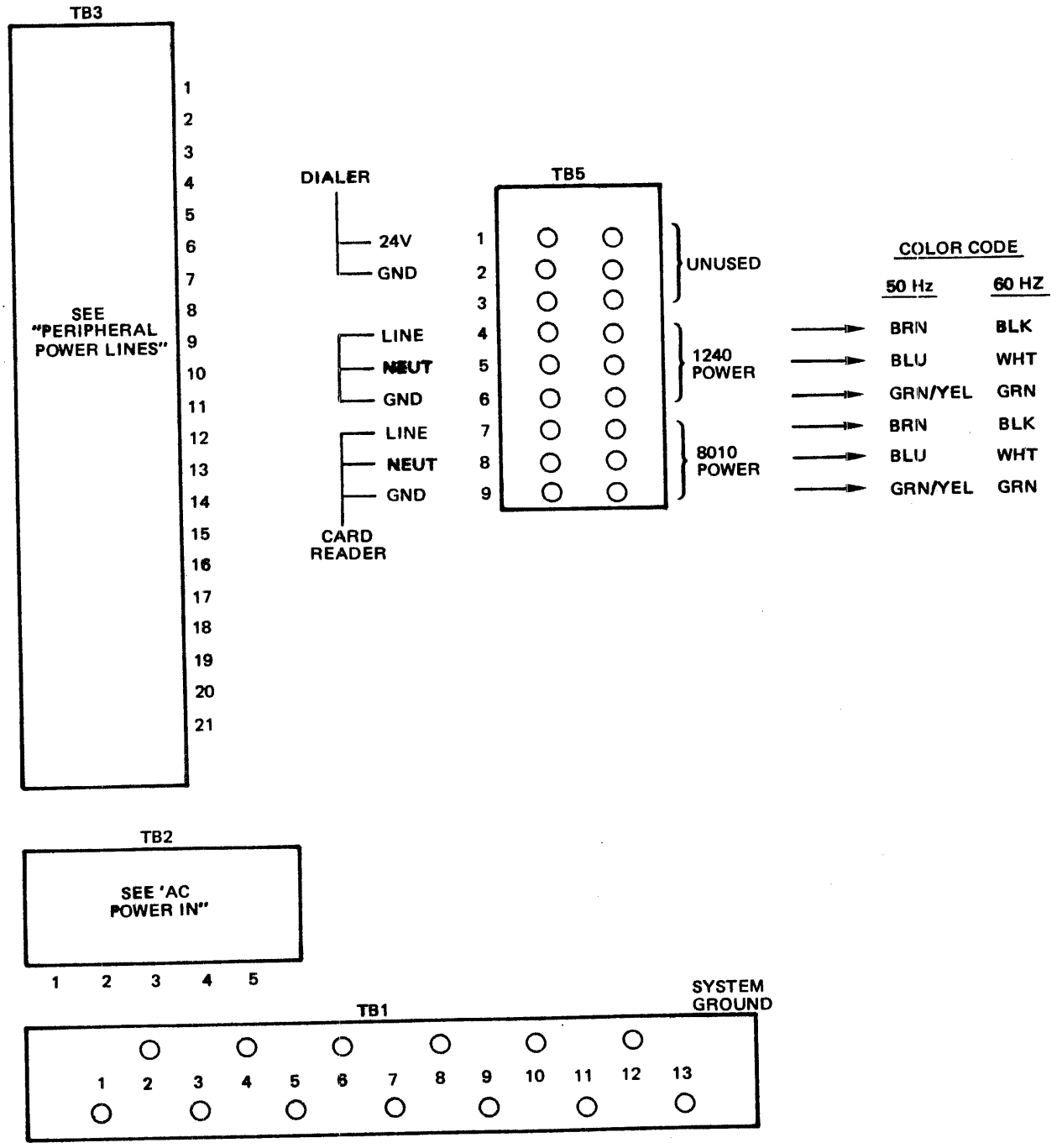


Figure 2-9. AC Distribution Panel

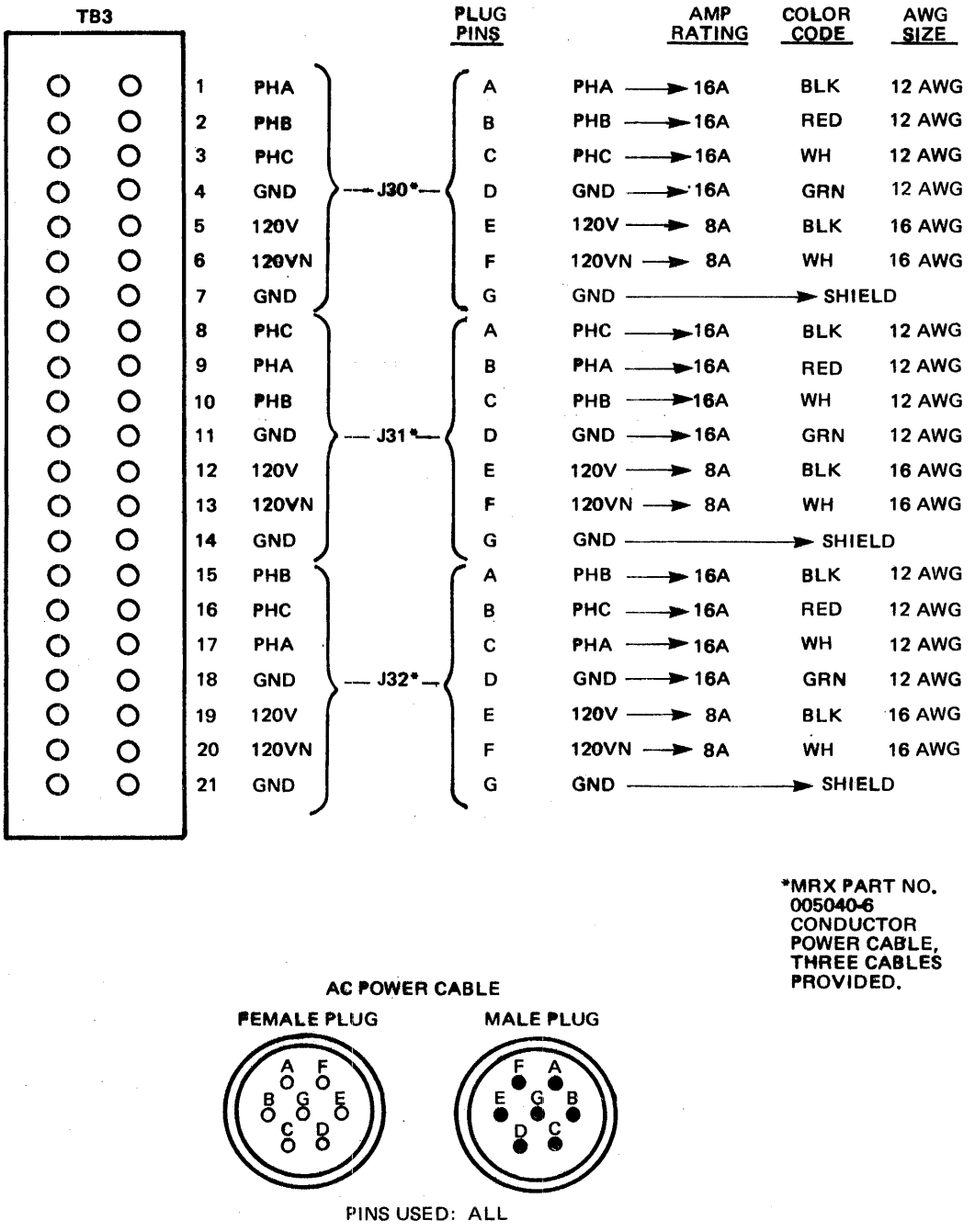
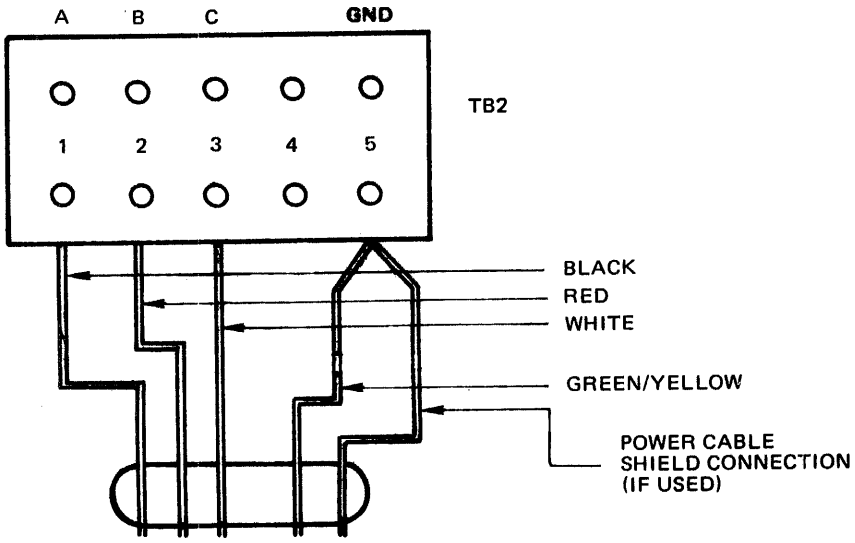
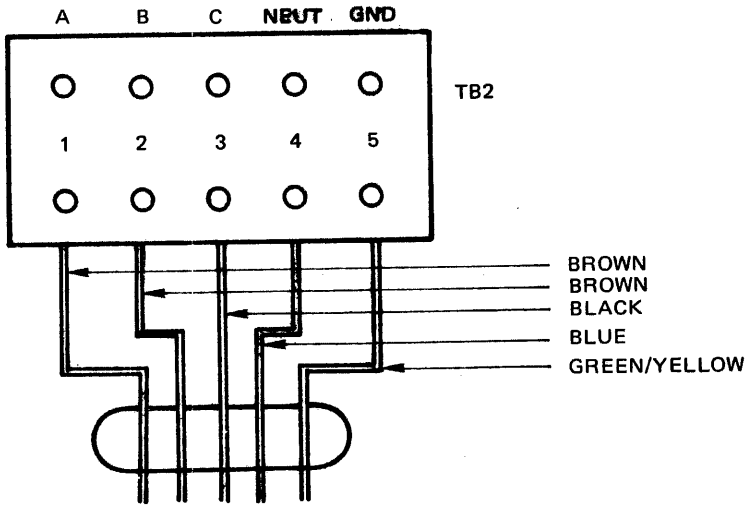


Figure 2-10. Peripheral Power Lines



a. 60 HZ CONFIGURATION



b. 50 HZ CONFIGURATION

NOTE:

AFTER INSTALLING POWER LINES, CHECK FOR PROPER FAN ROTATION. IF IMPROPER, CHECK CUSTOMER'S MAIN SUPPLY.

Figure 2-11. AC Power In

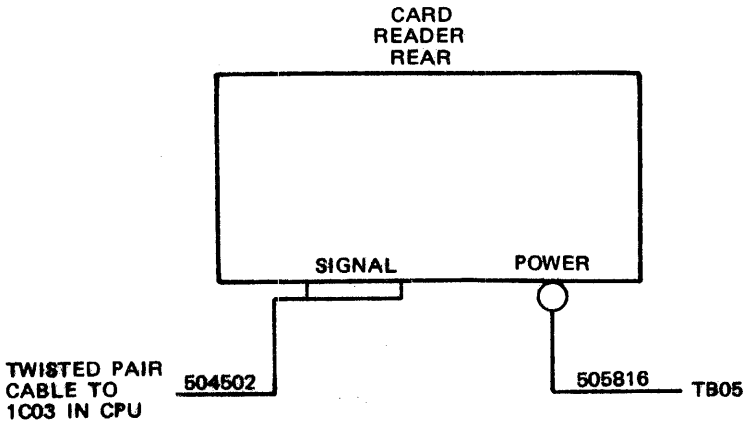


Figure 2-12. 8010 Console Card Reader Cable Connections

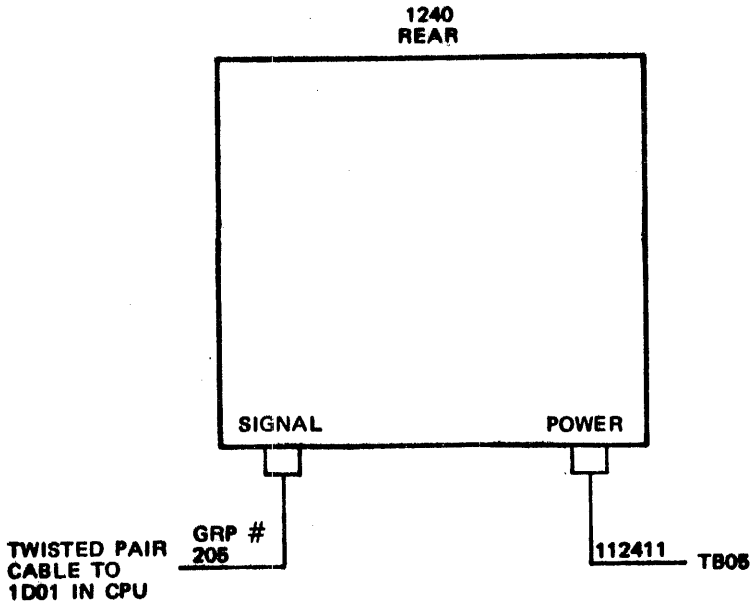


Figure 2-13. 1240 Console Cable Connections

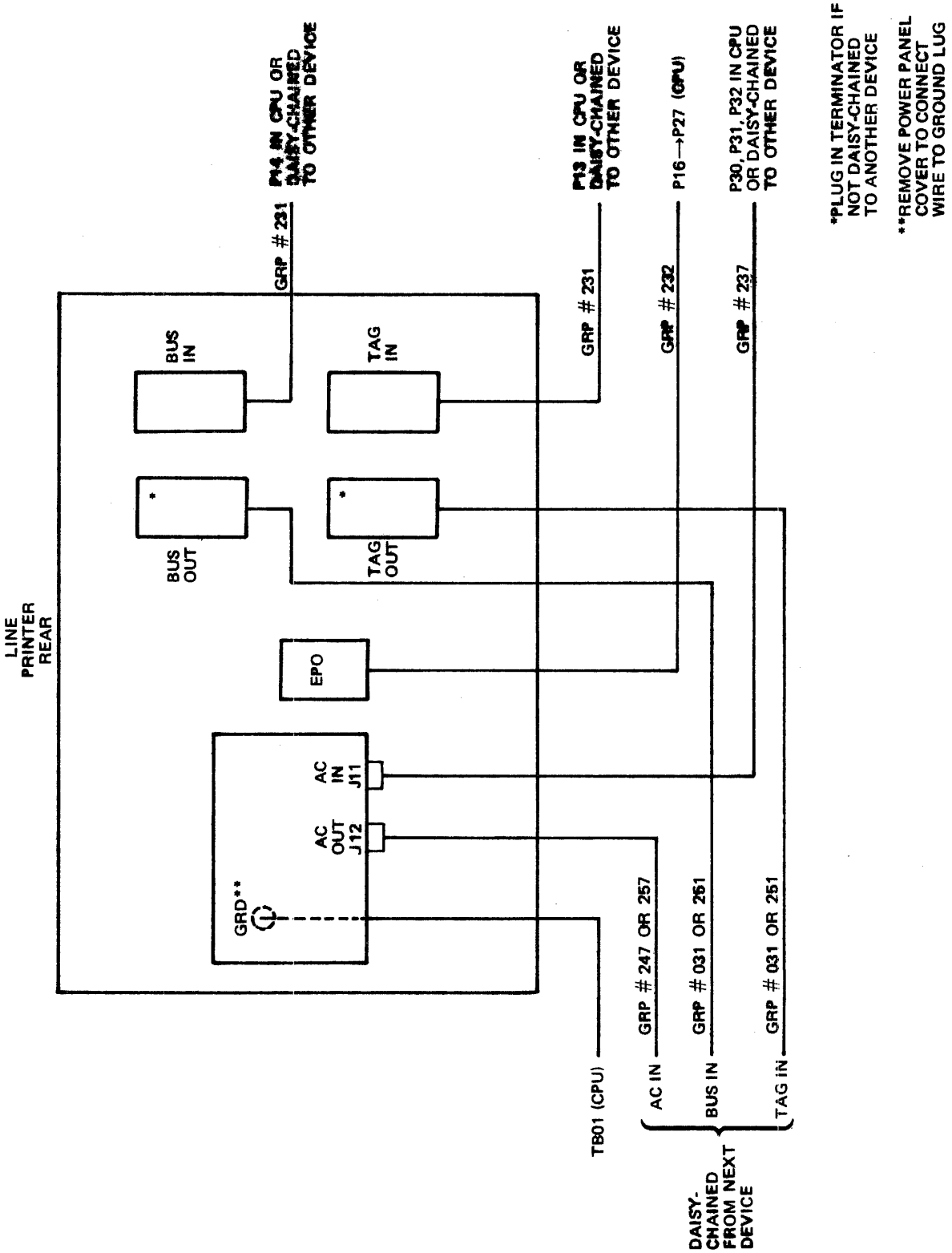


Figure 2-14. 5120 Line Printer Cable Connections

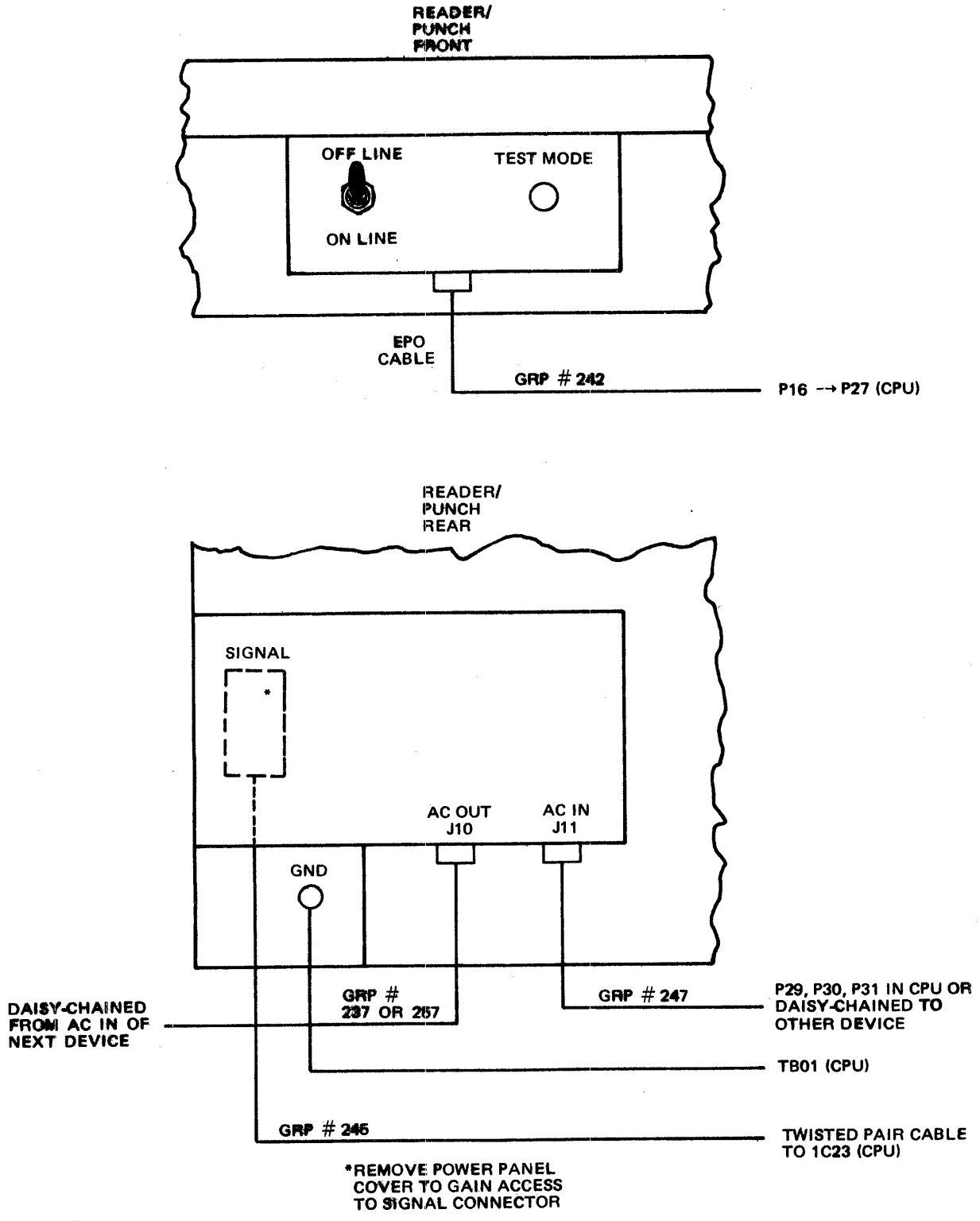


Figure 2-15. 8025 Card Reader/Punch Cable Connections

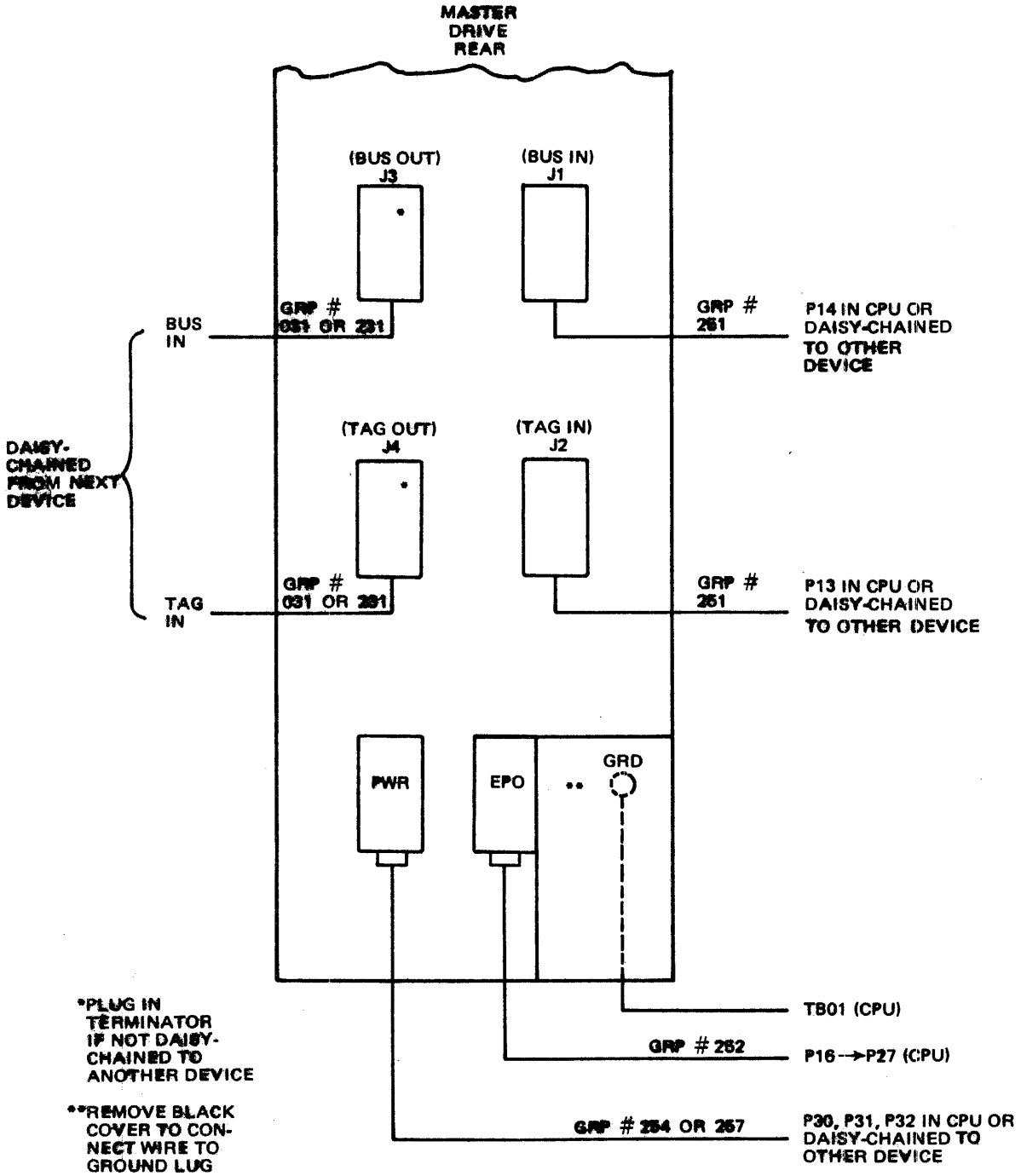


Figure 2-16. 3237 Master Tape Drive Cable Connections

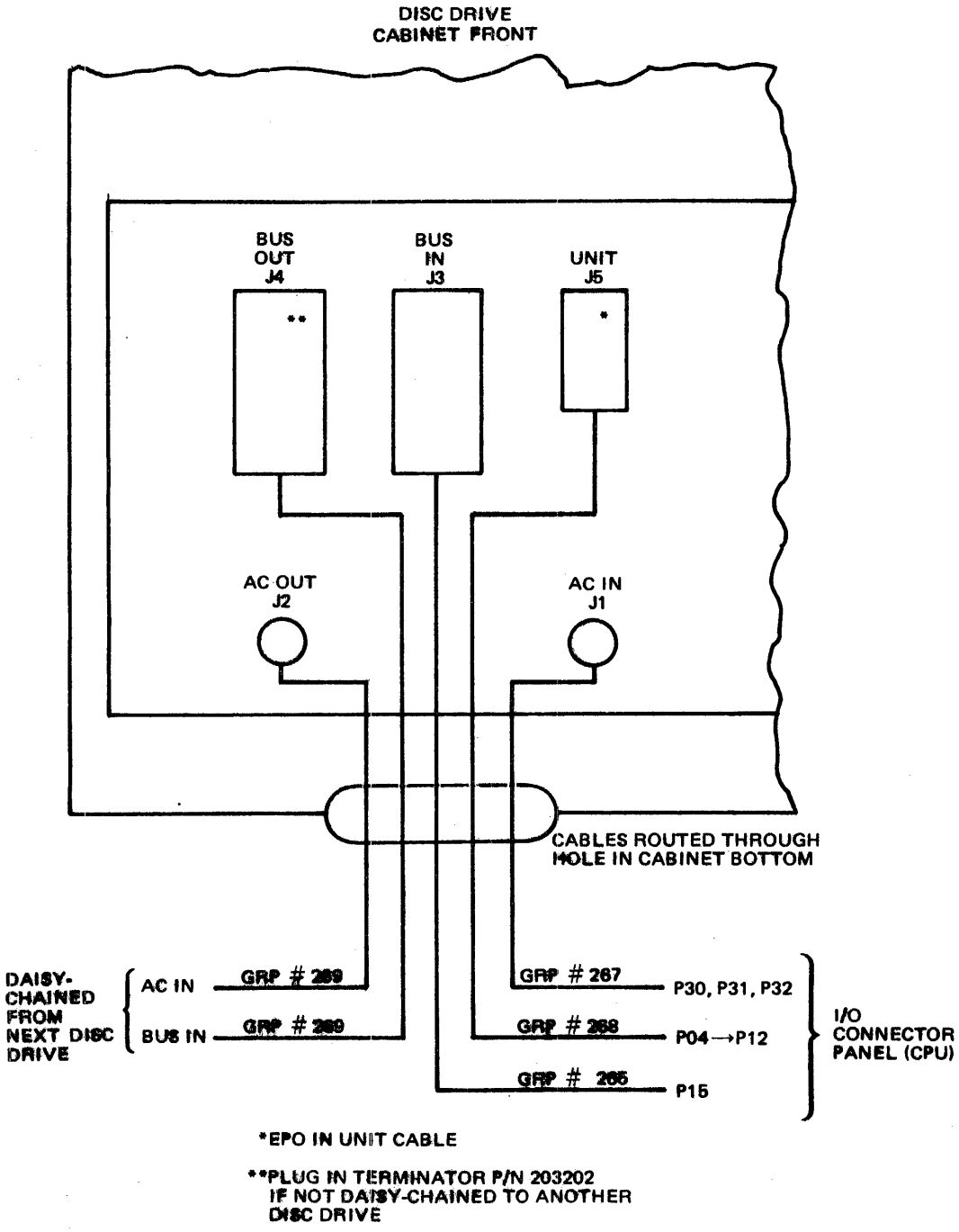


Figure 2-17. 1664 Disc Drive Cable Connections

POWER AND SIGNAL CABLE CONNECTIONS

Connect power and signal cables between the CPU and the peripheral device in accordance with the procedures below. (In Figures 2-12 through 2-17 referenced in these procedures, orderable cables are identified by cable group number and non-orderable cables by part number. In adition usage of the terms "FROM" and "TO" as cable origin/destination points is as defined in Section 6 of the Field Support Site Planning Manual.)

Power Cable Connections to TB05

Peripheral devices which require 120 VAC 60 Hz or 230 VAC 50 Hz single-phase power are supplied with this power from cables connected to TB05 under the operator's table. This terminal board permits connection of two power cables, which will usually be used to supply power to the 8010 console card reader and 1240 console. Connect the terminal ends of these cables to TB05 as follows:

	Wire Color	Signal	Terminal
8010 Console Card Reader	Green	Grd	TB05-9
	White	Neutral	TB05-8
	(third wire)	AC	TB05-7
1240 Console	Green	Grd	TB05-6
	White	Neutral	TB05-5
	(third wire)	AC	TB05-4

8010 Console Card Reader Connection

Connect the card reader to the CPU as described below. Locations of connectors on the card reader are shown in Figure 2-12.

1. Connect power cable between card reader power receptacle and source of 120 VAC, 1Ø power (TB05 pins 7, 8, and 9

2. Connect twisted-pair signal cable between card reader signal receptacle and CPU back panel pins at 1C03. At CPU, plug with black wires (grounds) connects to pins 4 through 42 (left column) and plug with white wires (signals) connects to plugs 3 through 41 (right column).

1240 Console Connection

Connect the console to the CPU as described below. Location of connectors on the console are shown in Figure 2-13.

1. Connect power cable between console power receptacle and source of 120 VAC, 1Ø power (TB05 pins 4, 5, and 6).

2. Connect twisted-pair signal cable between console signal receptacle and CPU back panel pins at 1D01. At CPU, plug with black wires (grounds) connects to pins 60 through 98 (left column), and plug with white wires (signals) connects to pins 59 through 97 (left column).

Peripheral Power Line (PPL) Cable Connection*

Peripheral devices which require three-phase power are supplied power by means of three PPL cables from the CPU. Up to nine devices can be powered from these cables, three devices per cable. Connections are made to each peripheral device in daisy-chain fashion via the AC IN and AC OUT receptacles in each device. To maintain optimum phase loading from one device to the next, each device rotates the phase fed to the next device by one phase leg. The three PPL cables are connected to the CPU by means of a junction box located under the operator's table to the lower right (Figure 2-18). This junction box, in turn, is fed with three-phase power from TB03. Connect cables from the junction box to TB03 in accordance with the information below:

Wire Color	Signal	Terminal DISC GRP 1	DISC GRP 2	DISC GRP 3
Large Black	ØA	TB03-15	TB03-8	TB03-1
Large Red	ØB	TB03-16	TB03-9	TB03-2
Large White	ØC	TB03-17	TB03-10	TB03-3
Large Grn/Ylw	GRD	TB03-18	TB03-11	TB03-4
Small Black	120	TB03-19	TB03-12	TB03-5
Small White	120 Conv	TB03-20	TB03-13	TB03-6
Grd Shield	GRD	TB03-21	TB03-14	TB03-7

* These connections are not required for 50 Hz machines.

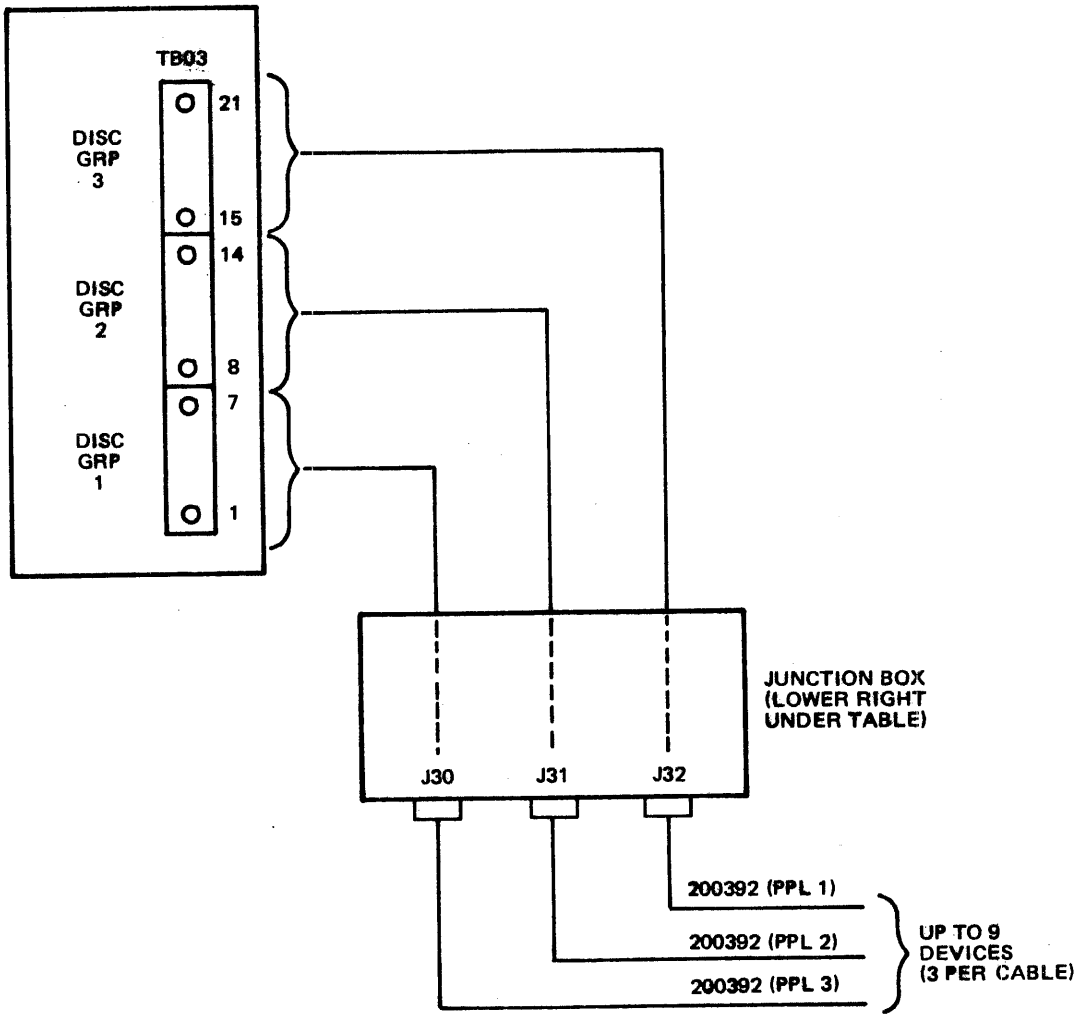


Figure 2-18. PPL Cable Connections

NOTE

When the daisy-chain method is used to supply 3-phase power to the devices discussed below, the following restrictions must be heeded:

a. All disc drives must be powered from the PPL's.

b. No more than three devices may be daisy-chained on one cable.

c. Disc drives may not be daisy-chained on a cable with other devices.

d. Power may not be daisy-chained through a tape subsystem to another subsystem.

5120 Line Printer Connection

Connect the line printer to the CPU as shown in Figure 2-14. Power cabling is subject to the restrictions of the preceding Note.

8025 Card Reader/Punch Connection

Connect the card reader/punch to the CPU as shown in Figure 2-15. Power cabling is subject to the restrictions of the preceding Note. At the CPU, connect the signal plug with black wires (grounds) to pins 58 through 96 of 1C23 and signal plug with white wires (signals) to pins 57 through 95 of 1C23.

3237 Master Tape Drive Connection

Connect the tape drive to the CPU as shown in Figure 2-16. Power and signal cabling are subject to the restrictions of the preceding Note.

3664 Disc Drive Connection

Connect the disc drive to the CPU as shown in Figure 2-17. Power cabling is subject to the restrictions of the preceding Note.

FINAL CONNECTIONS

1. Plug terminators, P/N 501220, into unused power sequence/EPO receptacles in power sequence control panel.

2. Connect wire end of main power cable to TB02 as shown below. Route wires through hole in bottom of terminal board box.

Wire	Signal	Terminal
Black	ØA	TB02-1
Red	ØB	TB02-2
White	ØC	TB02-3
Blue (if used)	Neutral	TB02-4
Grn/Ylw	Grd	TB0w-5

If power cable is shielded, connect shield wire to terminal 5.

POST-INSTALLATION CHECKOUT

TERMINAL BLOCK CHECKS

Check to see that screws are tight on the following terminal blocks and other assemblies. Refer to drawing 504472, Terminal Block Locations, in the 7200/7300 Processor Support Diagrams Manual for locations.

1. TB1, TB2, TB3, TB5; fuse blocks F4, terminals A, B, and C; CB1, terminals 1 through 6; KP2, terminals 1 through 6 and C1 and C2. All assemblies located on AC distribution unit.

2. TB6, TB7, TB8, TB9, TB50, also grounds to frame on TB55. Check that relays KP3, 5, and 6 are seated correctly. All located on AC switch assembly.

3. TB12, TB13, on auxiliary and storage transformers.

4. TB58 (SCR gates) located above SCR's. Check that PC module is located correctly.

5. Tighten all Phillips head screws on chassis 3 backpanel. Look for loose screws and washers.

6. TB59 on logic bulk supply transformer.
7. TB10, TB11 on +24V control supply.
8. TB65 on lamp supply (swing open System Control Panel).
9. TB54 on DC common bus right (front) end.

RESISTANCE CHECKS

Make resistance checks as follows:

1. Check for short circuits from supply to ground and between supplies by performing resistance checks in accordance with Table 2-2. (Refer to drawing 504480, Busing System in the Support Diagrams Manual for locations of buses).
2. Check resistance between +24 VDC control supply heat sink and frame (ground). Resistance should be at least 2.5 ohms.

TABLE 2-2. RESISTANCE CHECKS

Supply Name	Meter From Supply Output	Meter To Ground	Nominal Reading ohms	
			High	Low
+5 A	Bus 2	Bus 4	3.5	1.5
+5 B	Bus 3	Bus 4	4.5	2.3
+5 C	3E03-LL	Bus 4	8.5	3.8
-5	3E03-UR	Bus 4	10.5	3.5
+3	3E04-LL	Bus 4	3.3	3.3
-3	3E04-UR	Bus 4	9.0	4.8
+12	3C02-LL	Bus 4	25	6.5
-12	3C02-UR	Bus 4	25	7
+19	Bus 7	Bus 4	25	6
+23	Bus 6	Bus 4	20	4.5
+24	TB11-7	TB11-3	50	20
+28	TB65-9	TB65-11	20	4.5

NOTE

Resistance readings may vary from those given and therefore, are listed as a guide only. To obtain second reading, reverse ohmmeter leads after making first reading.

VOLTAGE CHECKS

Check voltages in system as follows:

1. Pull all logic and memory modules in chassis 1 and 2 except 1A01. There is no need to remove them completely, just far enough to disengage pins.

2. Check that the following circuit breakers are set (pushed in):

   a. CB2 (+12 VDC), CB3 (-12 VDC), and CB4 (storage) at rear of machine on left side.

   b. Logic drive supply CB located on supply above the auxiliary/storage transformer (left side).

   c. +24 VDC control supply CB.

3. Check that all modules in chassis 3 are pushed fully home. (If this is not done, it is possible to have a short-circuit from the backpanel to a module.

4. Plug receptacle end of main power cable into three-phase power source.

5. Turn main power switch S1 (located near bottom of AC distribution panel on right side) to ON. Check that POWER OFF lamp on System Control Panel lights.

6. Press POWER ON button. POWER ON and POWER OFF lamps should stay on together for about 15 seconds, then POWER OFF lamp should go out. This shows that the power up sequence is complete.

7. Check blower for correct rotation (air upwards). If blower runs backwards, turn power off, disconnect supply, and check color-coding of main power cable wires to TB2. If wired correctly, check phasing of customer's power mains.

8. Check all voltages using the DEVIATION METER and voltage selector in the top section of the System Control Panel. (If cover is closed, open by placing thumb in upper right corner of cover and pressing down.) All voltages should be within $\pm$5%, except the 24 VDC control and 28 VDC lamp supplies which may be $\pm$10%.

EMERGENCY POWER OFF (EPO) CHECKS

The emergency power off capability cannot be checked directly by pulling the EMERGENCY PULL knob on the System Control Panel because of possible equipment damage that might result. Therefore, an indirect procedure is used as described below:

1. Shut down system power by pressing the POWER OFF pushbutton on the Panel.

2. Pull the EMERGENCY PULL knob and listen for the EPO relays to unlatch.

3. Attempt to restore power to system by pressing the POWER ON pushbutton. It should be impossible to do so until the EMERGENCY PULL knob is manually reset. (Reset by opening Panel door and pressing up on catch to left of switch looking from rear.)

SHARED RESOURCES OPERATIONAL CHECK

Make an operational check of the shared resources (CPU and MS) as follows:

1. Insert the following modules into chassis 1 and 2, one by one, while monitoring +5 VDC on the bus corresponding to each chassis row:

   a. 1A02 through 1A30 (both +5 and -5 VDC must be monitored when AT module at 1A12 is inserted.)

   b. 1B16 through 1B24 and 1B26 through 1B29

   c. 1C09, 1C10, and 1C11; and 1C03 through 1C06 (if system has card reader) or 1C23 through 1C27 (if system has reader/punch)

   d. 2A11, 2A12, 2B11, 2B12, 2C11, and 2C12.

   CAUTION

   Turn system power off by pressing POWER OFF pushbutton when inserting or removing HH modules.

2. Insert HH modules in rows A, B, and C.

3. Load CPU1, CPU2, and CPU3 micro-diagnostic programs from cards using the card reader or reader/punch. (Refer to

the listing for operating procedures.) Run the micro-diagnostics under marginal voltages of +5, +4.7, and +5.3 VDC. (Before running margins, adjust +5 VDC to exactly +5.0 VDC via LOGIC A pot so that voltage margins will be within tolerance.)

4. Load the main storage micro-diagnostics from cards. (Refer to the listing for operating procedures.)

5. Run the routines under the following timing and voltage margins. Each margin should be tested for about two minutes for a 16K byte memory and about 5 minutes for a 65K byte memory. (Before running margins, adjust +19.8 VDC to exactly +19.8 VDC via MAIN STORAGE pot so that voltage margins will be within tolerance.)

   a. Voltages normal - Timing switch on 2B13 in the normal (up) position.

   b. Voltages normal - Timing switch in the middle position.

   c. Voltages normal - Timing switch in the down position.

   d. V(ss) (+19.8 volts) up 5% to 20.8 - Timing normal.

   e. V(ss) at 20.8 - Timing switch in the middle position.

   f. V(ss) at 20.8 - Timing switch in the down position.

   g. V(ss) down 5% to 18.8 - Timing normal.

   h. V(ss) at 18.8 - Timing switch in the middle position.

   i. V(ss) at 18.8 - Timing switch in the down position.

6. Return timing and voltage to normal.

7. Load the standard microcode into control storage from cards.

8. Load Quick Look, Control, and Command MLI diagnostic programs (part of the Design Verfication Routines set) cards. Run these diagnostics under the voltage and timing margins described in Step 3.

9. Repeat Step 6.

DISC SUBSYSTEM OPERATIONAL CHECK

Make an operational check of the disc subsystem as follows:

1. Insert IFA modules in the following locations while monitoring the chassis 1, row B +5, -5, +12, and -12 VDC buses:

1B01	1B10	1B13
1B02	1B11	1B14
1B09	1B12	1B15

2. Load and run the Disc Checkout diagnostics.

3. Load and run the Disc Exerciser diagnostics under control of the Maintenance Monitor. Select all available subtests and run each under the voltage margin conditions listed below:

   a. +5 VDC A for chassis 1, row B at 5 VDC

   b. +5 VDC A for chassis 1, row B at 5.3 VDC

   c. +5 VDC A for chassis 1, row B at 4.7 VDC

4. Repeat step 3 for all UNIT connectors J4 through J1%.

1240 CONSOLE OPERATIONAL CHECK

Make an operational check of the 1240 Console as follows:

1. Insert ICA outbound register and queue modules in 1C14 a 1C15, and ICA channel 0 modules in chassis 1, row D, whi monitoring the +5 VDC bus. (Refer to module placement map, if necessary, to determine which modules are associated with channel 0.)

2. Load and run the Communication Checkout diagnostics to check out the Console connected to channel 0.

3. Repeat Steps 1 and 2 to check out other channels of the system. If necessary, reconnect the terminal device to modules associated with these other channels.

BASIC DATA CHANNEL OPERATIONAL CHECK

Make an operational check of the basic data channels as follows:

1. Load the IOC Checkout and Card Reader Exerciser diagnostics. Run these diagnostics to check card reader read operations under marginal voltages of +5, +4.7, and +5.3 VDC.

2. Insert the IRPA modules in locations 1C23 through 1C27, one by one, while monitoring the +5, -5, +12, and -12 VDC buses.

3. Perform a reset/load and run the micro-diagnostics.

4. Load the IOC Checkout and Reader/Punch Exerciser MLI diagnostics. Check both reader and punch devices under marginal voltages of +5, +4.7, and +5.3 VDC.

5. Insert BDC2 external interface module 1C02 while monitoring the +5 VDC bus.

6. Load and run the IOC Checkout and Printer Exerciser diagnostics under voltage margins of +5, +4.7, and +5.3 VDC.

7. Insert BDC1 and BDC2 assembly/disassembly modules 1C01 and 1C02 while monitoring the +5 VDC bus.

8. Load the IOC Checkout diagnostics. Use these diagnostics to check BDC devices in assembly/ disassembly mode (not byte mode).

9. Remove BDC2 external interface module 1C02 and insert BDC1 external interface module 1C01.

10. Remove line printer bus and tag cables connected to P14 and P13 (BDC 2) and re-connect to P29 and P28 (BDC 1).

11. Load and run the IOC Checkout diagnostics to check the printer under voltage margins of +5, +4.7, and +5.3 VDC.

12. Using the IOC Checkout diagnostics, perform simultaneous checks on the card reader and reader/punch (BDC 2) and line printer (BDC 1). Make each check under voltage margins of +5, +4.7, and +5.3 VDC.

13. Using the IOC Checkout diagnostics, check the printer in the assembly/disassembly mode.

14. Remove BDC 1 external interface module 1C01 and insert BDC 2 external interface module 1C02.

15. Remove line printer bus and tag cables connected to P29 and P28 (BDC 1) and re-connect to P14 and P13 (BDC 2).

16. Using the IOC Checkout diagnostics, perform simultaneous checks on the card reader, reader/punch, and line printer (all BDC 2). Make each check under voltage margins of +5, +4.7, and +5.3 VDC.

17. Run the Card Reader, Reader/Punch, and Line Printer Exercisers simultaneously under voltage margins.

18. Insert BDC 1 external interface module 1C01.

19. Connect tape drive bus and tag cables to P29 and P28 (BDC 1).

20. Using IOC Checkout and Tape Exerciser diagnostics check all tape drive functions.

SYSTEM TEST UNDER BIAS CONDITIONS

Check the system with diagnostics under bias conditions in accordance with Table 2-3. Check voltage percent deviation with digital voltmeter.

INSTALLATION REPORT

Upon completing installation of the system, fill out MRX/40/50 Installation Report form MEG/FS 7167.

TABLE 2-3. BIAS TESTING

BIAS / DIAGNOSTIC	+5 A & B P/S, +5%	+5 A & B P/S, -5%	+5 A, +5% +5 B, -5%	+5 A, -5% +5 B, +5%			
CPU1 CPU2 CPU3							
	+5 A & B P/S, +5%	+5 A & B P/S, -5%	MS P/S +5%	MS P/S -5%	A & B, +5% MS, -5%	A & B, -5% MS, +5%	MS TIMING + & -
CONTROL COMMAND QUICKLOOK							
	+5 A & B P/S, +5%	+5 A & B P/S, -5%	+5 A, +5% +5 B, -5%	+5 A, -5% +5 B, +5%	MS P/S +5% A & B, -5%	MS P/S, -5% A & B, +5%	MS TIMING + & -
STORAGE w/o ECC STORAGE w/ECC							
	+5 A & B P/S, +5%	+5 A & B P/S, -5%	+5 A, +5% +5 B, -5%	+5 A, -5% +5 B, +5%			
IFA IRA IRPA CHAN1 CHAN2 1240 COMM ICA							

SECTION 3. OPERATING DATA AND PROCEDURES

INTRODUCTION

This section provides a functional description of each switch and indicator on the System Control Panel. Also included are step-by-step procedures for the most commonly used operations which may be executed through the panel.

CONTROLS AND INDICATORS

Controls and indicators on the System Control Panel are divided into five groups:

- Operator Group
- Programmer Group
- Maintenance Group
- System Activity Display Group
- Communications Activity Display Group

The following paragraphs provide a functional description for each control and indicator on the panel. The descriptions are arranged by panel group, starting with the bottom right control in each group and proceeding in a leftward and upward manner. The System Control Panel is illustrated in drawing 506104, Console Component Locations, in the Support Diagrams Manual, Volume 1.

NOTE

All pushbuttons are of the momentary-action type unless otherwise specified.

OPERATOR GROUP

- EMERGENCY PULL Knob

  When pulled, instantly removes all power from system except AC power to and DC power from the +24 vdc control supply (does not go through normal power-down sequence which is the case when using POWER OFF pushbutton).

  NOTE

  The EMERGENCY PULL knob is not meant for normal "power-off" sequencing since it can cause extensive equipment damage when pulled. Whenever this switch is used to remove power from the system, power cannot be reapplied until a mechanical interlock within the cabinet is released. (This is a maintenance activity.) Thus, the EMERGENCY PULL knob is intended to be used only in emergency situations (circumstances involving a safety hazard).

- POWER OFF Pushbutton/Indicator

  Turns system power off when POWER MODE switch is in LOCAL. This switch assures proper power-down sequencing. (The POWER OFF pushbutton has no effect while the POWER MODE switch is in REMOTE.)

  NOTE

  The POWER OFF indicator will be lit unless one of the following conditions exist: no primary power is available, the Main Disconnect switch is off, the EMERGENCY PULL knob has been pulled, or power is on (that period between the completion of a power-up sequence and the initialization of a power-down sequence).

- POWER ON Pushbutton/Indicator

  Turns system power on when the POWER MODE switch in the Maintenance Group is in LOCAL. This switch insures proper power-up sequencing. (The POWER ON pushbutton has no effect while the POWER MODE switch is in REMOTE.)

  NOTE

  Upon completion of the power-up sequence, a Reset/Load sequence is automatically initiated. Moreover, at completion of the Reset/Load sequence, an Autoload sequence is automatically initiated

provided the maintenance mode has not been selected. Further detail is provided in the procedures for loading CS and MS in either the operator or program mode.

- AUTOLOAD Pushbutton

Causes main storage to be loaded, starting at a location in Control Storage determined by the microprogram subroutine with data obtained either from disc drive zero (when LOAD SELECT switch is in DISC) or from cards (when LOAD SELECT switch is in CR or R/P). Starting addresses of the microprogram load routines are 0113 (hex) for a load from disc and 0112 (hex) for a load from cards.

- LOAD SELECT Switch

Determines input device used during a Reset/Load and/or Autoload sequence. Down position (R/P) selects card reader/punch as the input device. Center position (DISC) selects disc subsystem as the input device. Up position (CR) selects console card reader as the input device.

- SPEAKER VOLUME Control

Adjusts volume of the speaker located in upperright side of panel enclosure. This speaker is driven by the circuits associated with bit positions 13, 14, and 15 of the CONSOLE DATA REGISTER DISPLAY indicators.

NOTE

The relative loudness levels of these bits through the speaker are these: bit 14 will be twice as loud as bit 13 and bit 15 twices as loud as bit 14.

- I/O FAULT Pushbutton/Indicator

I/O FAULT will light if any of the following conditions occur:

1. Channel 1 Transmission Parity Error
2. Channel 2 Transmission Parity Error
3. Channel 1 Control Check Error
4. Channel 2 Control Check Error

5. Burst Check Error (during a Reset/Load operation from disc)

6. Failure of disc heads to retract during power-down sequence

Pressing I/O FAULT extinguishes the indicator. (Refer to individual I/O fault indications in the System Activity Display Group further in this section.)

- PROC FAULT Pushbutton/Indicator

PROC FAULT will light if any of the following conditions occur:

1. Control Storage Parity Error

2. Main Storage Parity Error

3. DC Voltage Fault

4. Over-Temperature condition

Pressing PROC FAULT extinguishes the indicator except in the case of a DC Voltage Fault or an Over-Temperature condition. In this case, the cause must be corrected for the switch to have effect.

- ALARM (located behind Panel)

Furnishes an audible signal when the LAMP TEST pushbutton is pressed or when any of the following conditions exist:

1. Blower failure within the computer

2. DC voltage fault

3. Failure of disc heads to retract during a power-down sequence

NOTE

When blower failure or DC fault conditions exist for approximately 60 seconds, the power-down sequence is automatically initiated. If the heads fail to retract from a disc during the power-down sequence, DC voltages will be removed within the computer. The power-down sequence will stop at that point until the problem is corrected.

- ALARM DISABLE Pushbutton/Indicator

  Pressing this pushbutton, if the audible alarm is on, causes the alarm to stop and the ALARM DISABLE to illuminate. When the alarm condition is corrected, the ALARM DISABLE will extinguish.

- LAMP TEST Pushbutton

  Pressing this switch causes all indicators to light and the alarm to sound. Releasing the switch returns them to their prior state.

- RESET/LOAD Pushbutton

  Causes data to be read from either cards or disc and transferred to either control storage and first-level decode address table or main storage, depending on whether the CONSOLE MODE SELECT selector is set to CS-WR or MS-WR and if the Maintenance Mode has been selected. Selection of cards or disc as input medium is determined by position of the LOAD SELECT switch. (See the procedures for performing CS loads for explicit instructions regarding the use of this pushbutton.)

  Upon completion of a Reset/Load operation from disc, an Autoload operation will automatically be initiated, providing Maintenance mode has not been selected.

PROGRAMMER GROUP

NOTE

Controls within this group are conditioned by the PROGRAM MODE pushbutton/indicator, except where otherwise designated.

- CONSOLE MODE SELECT Selector

  Selects basic mode of operation for panel:

  RO-RD - register option read

  RO-WR - register option write

  RF-WR - register file write

  RF-RD - register file read

OFF - selector disabled

MS-RD - main storage read

MS-WR - main storage write

CS-RD - control storage and first-level decode address table read or scan (enabled in Maintenance mode only)

CS-WR - control storage write (enabled in Maintenance mode only, except during a Reset/Load operation)

- CONSOLE RUN Pushbutton

Initiates the function selected on the CONSOLE MODE SELECT selector in a manner determined by the CONSOLE CONTROL SELECT switch.

- CONSOLE CONTROL SELECT Switch

The three-position switch governing the way in which a selected console control operation is executed:

STOP/STEP - stop and step

NORMAL - run continuously

BREAKPOINT - run as far as breakpoint (applies to CS-RD, CS-WR, MS-RD, and MS-WR only).

- CONSOLE MAIN STORAGE Switch

NOTE

This switch has no effect unless the relocation and Protection feature is installed.

This switch determines whether the contents of the S Register are interpreted as a System or Physical Main Storage Address during Panel-initiated MS references; i.e., MS-RD or MS-WR. When in the RELOCATE (up) position, the contents of the S Register are interpreted as a System Main Storage Address and is converted by the relocation mechanism into a Physical Main Storage Address. When in the OFF (down) position, the contents of the S Register are directly interpreted as a Physical Main Storage Address and will bypass the relocation mechanism.

- SYSTEM RESET Pushbutton

  The SYSTEM RESET pushbutton clears the following registers:

  1. EXTENDED REGISTER FILE

     Group I: Pu of all processor states

     Group II: Busy/Active, Tie-Breaker, Control, Privileged, Boundary-Crossing, Control Storage Scan, Console Address, and Data.

  2. SHARED RESOURCE REGISTERS

     Au, Bu, D, Su, Fu-1, Fu-2, and Forced Carry Register.

- PROGRAM MODE Pushbutton/Indicator

  Pressing this switch enables those switches located in the programmer group area of the panel. The pushbutton is illuminated when Program mode is selected.

- CONSOLE DATA REGISTER SELECT Selector

  Selects one of eleven registers to be displayed by the CONSOLE DATA REGISTER DISPLAY indicators. (Does not affect the pushbutton function.)

  Fu2 - Micro-Command Function register, rank 2 (enabled in Maintenance mode only)

  Fu1 - Micro-Command Function register, rank 1 (enabled in Maintenance mode only)

  RTC - Real-Time Clock register (enabled in Maintenance mode only)

  CSS - Control Storage Scan register (enabled in Maintenance mode only)

  B/A - Busy/Active register

  DATA - Console Data register

  D - Main Storage Data register (enabled in Maintenance mode only)

  Au - ALU Feeder register Au (enabled in Maintenance mode only)

Bu - ALU Feeder register Bu (enabled in Maintenance mode only)

SUM - output of ALU (sum of Au and Bu) (enabled in Maintenance mode only)

BC - Boundary-Crossing register (enabled in Maintenance mode only)

- CLEAR DATA Pushbutton

  Clears contents of Console Data register.

- CONSOLE DATA REGISTER DISPLAY Pushbutton/Indicators

  Twenty pushbutton/indicators horizontally located as five groups of four bits each. These groups function as follows:

  1. Pushbutton/indicators X0 - X3

     NOTE

     These pushbutton/indicators are not functional unless the Relocation and Protection feature is present.

     In the presence of the Relocation and Protection feature, pressing these pushbuttons will set corresponding bits in the segment tag portion of the Console Data register, causing the associated indicators to light.

  2. Pushbutton/indicators 00 - 15

     Pressing these pushbuttons will set corresponding bits in the Console Data register only, causing the associated indicators to light. During register display operations, however, the indicators light for corresponding bits set at the Fu2, Fu1, RTC, CSS, B/A, DATA, D, Au, Bu, SUM, or BC outputs as determined by the CONSOLE DATA REGISTER SELECT selector.

     The digital inputs to the Console Data register display lamp drivers in bit positions 13, 14, and 15 are also used as inputs to the panel speaker drivers.

- CONSOLE ADDRESS REGISTER SELECT Selector

  Selects one of four registers to be displayed by the CONSOLE ADDRESS REGISTER DISPLAY indicators. (Does not affect the pushbutton function.)

  S - Main Storage Address register

  Su - Control Storage Address register (enabled in Maintenance mode only)

  ADDRESS - Console Address register

  PE - Main Storage Parity Error Address register (enabled in Maintenance mode only)

- CLEAR ADDRESS Pushbutton

  Clears contents of Console Address register.

- CONSOLE ADDRESS REGISTER DISPLAY Pushbutton/Indicators

  Twenty pushbutton/indicators horizontally located as five groups of four bits each. These groups function as follows:

  1. Pushbutton/indicators X0 - X3

     NOTE

     These pushbutton/indicators are not functional unless the Relocation and Protection Feature is present in the 7200/7300 computer.

     In the presence of the Relocation and Protection Feature, pressing these pushbuttons will set corresponding bits in the segment tag portion of the Console Address register only, causing the associated indicators to light. During register display operations, however, the indicators light for corresponding bits set in the segment tag portions of the S, Console Address, and PE registers as determined by the CONSOLE ADDRESS REGISTER SELECT selector.

  2. Pushbutton/indicators 00 - 15

     Pressing these pushbuttons sets corresponding bits in the Console Address register only, causing the associated indicators to light. During register display operations, however, the indicators light for corresponding bits set in the Su, S, Console Address,

and PE registers as determined by the CONSOLE ADDRESS REGISTER SELECT selector.

- BREAKPOINT MODE SELECT Switches:

  1. WRITE DATA Switch

     When up (on), causes breakpoint stop at end of each main storage reference cycle in which data was written at breakpoint address.

  2. READ DATA Switch

     When up (on), causes breakpoint stop at end of each main storage reference cycle in which data was read at breakpoint address.

  3. READ INSTR Switch

     When up (on), causes breakpoint stop immediately after the machine language instruction is read at breakpoint address.

  4. RELOCATE/PHYSICAL Switch

     NOTE

     This switch has no effect unless the Relocation and Protection Feature is installed.

     This switch determines whether the System or Physical Main Storage Address is compared with the Breakpoint Address selection. Additionally, this switch determines whether the System or Physical Main Storage Addresses are sent to the CONSOLE ADDRESS REGISTER DISPLAY indicators when the SELECT selector is set to the S position. When in the RELOCATE (up) position, System Main Storage Addresses are selected. When in the PHYSICAL (down) position, Physical Main Storage Addresses are selected.

- BREAKPOINT ADDRESS SELECT Selectors

  Five selectors which provide a hexadecimal stop address for processor state(s) operating in the breakpoint mode. Also applies to console mode, MS-RD, MS-WR, CS-RD, and CS-WR selections.

- PROCESSOR SELECT Selector

  Selects one of the eight processor states to execute in the mode selected by the corresponding PROCESSOR CONTROL SELECT switches.

- PROCESSOR RUN Pushbutton

  Starts the processor state selected by the PROCESSOR SELECT selector.

- PROCESSOR CONTROL SELECT Switches

  Eight three-position switches which place individual processor states in one of three modes:

  STOP/STEP - Stop and step selected processor state.

  NORMAL - Allows selected processor state to run continuously.

  BREAKPOINT - Allows selected processor state to run until a breakpoint-comparison equality occurs.

MAINTENANCE GROUP

- POWER MODE Switch

  When in LOCAL position, places power on/off function under control of POWER ON and POWER OFF pushbutton/indicators. When in REMOTE position, transfers on/off function to remote control.

- LOGIC B Adjust

  Adjusts the +5 VDC supplied to chassis 2.

- LOGIC A Adjust

  Adjusts the +5 VDC supplied to chassis 1.

- MAIN STORAGE Adjust

  Adjusts the +19.8 and +23.3 VDC supplied to main storage.

- CYCLE STEP Switch

  This switch is for any processor state in the STOP/STEP mode; the switch causes the basic step to be one machine instruction when down (off) or one major cycle when up (on).

- EXECUTIVE DISABLE Switch

  When up (on), prevents Processor state 4 from being automatically started every 16.3 milliseconds by the real-time clock.

- INSTRUCTION REPEAT Switch

  When up (on), causes all processor's states to repeatedly execute the current machine language instruction. This applies to all processor modes.

- CS DISABLE Switch

  When up (on), causes all output from control storage to consist of 0's (equivalent to a succession of NOP (No Operation) micro-instructions).

- STORAGE PARITY DISABLE Switch

  When up (on), disables main and control storage parity error stops and traps. Does not disable MS PARITY ERROR or CS PARITY ERROR indicators.

- SELECT EVEN PARITY BYTE 0 Pushbutton (Alternate-action Switch)

  Pressing this pushbutton changes parity generation from odd to even for byte 0 of the word currently being written into main storage. Parity changes back to odd when pushbutton is pressed a second time.

- SELECT EVEN PARITY BYTE 1 Pushbutton (Alternate-action Switch)

  Pressing this pushbutton changes parity generation from odd to even for byte 1 of the word currently being written into main storage. Parity changes back to odd when pushbutton is pressed a second time.

- MAINTENANCE MODE Pushbutton/Indicator

  When in the ON position, this switch enables all System Control Panel controls in both the Program and Maintenance Groups. When in the OFF position, this switch disables all controls in the Maintenance Group only.

- Voltage Test Selector

  Selects voltage to be measured for deviation.

- Voltmeter

  Displays voltage deviation in that supply selected by Voltage Test Selector.

- SET D

  These two pushbutton/indicators perform as follows:

  1. SET Au Pushbutton/Indicator (Alternate-action switch)

     Sets all 1's into Au register.

     NOTE

     When SET Au and SET Bu pushbuttons are pressed simultaneously, all 1's are set into the D-Register and a carry is forced into the primary ALU adder as long as the pushbuttons are held pressed.

  2. SET Bu Pushbutton/Indicator (Alternate-action switch)

     Set all 1's into Bu register. (Note for SET Au pushbutton applies.)

- SELECT CS MINIMUM/OFF

  When pressed to the ON (illuminated) position, this pushbutton selects Control Store size of 4096 words maximum for Control Storage proper and 256 words maximum for the Address Table.

  NOTE

  Hardware information relative to the sizes of Control Storage and the FRJ decode Address Table are effective only during Console Control Storage Read, Console Storage Write, and Reset/Load operations.

When pressed to the OFF (non-illuminated) position, this pushbutton has no effect.

- Time Meter (located on left side of Panel)

  Displays elapsed time that computer power has been on.

SYSTEM ACTIVITY DISPLAY GROUP

- PROCESSOR STATE Indicators

  Dynamically indicate which processor states are executing major cycles.

- Status Indicators

  Twelve indicators that illuminate particular status conditions:

  1. MS PARITY BYTE 0 - Displays parity bit state of leftmost byte (bits 0 through 7) of the last word read out of MS. (Not enabled if ECC is present.)

  2. MS PARITY BYTE 1 - Displays parity bit state of rightmost byte (bits 8 through 15) of the last word read out of MS. (Not enabled if ECC is present.)

  3. MS PARITY ERROR - Displays state of MS Parity Error flip-flop. Indicator is on if flip-flop is set and off if flip-flop is cleared.

  4. CS PARITY ERROR - Indicates a parity error in CS or first-level decode address table.

  5. D.C. FAULT - Indicates that one or more DC power supply in system is not within allowable output range. Remains on until condition is corrected.

  6. OVER TEMP. - Indicates a blower failure condition within cabinet.

  7. HEADS EXTENDED - Indicates that heads in one or more disc files fail to retract during the power-down sequence.

  8. BURST CHECK - Indicates detection of a burst check error during a Reset/Load sequence from the disc file.

  9. CHANNEL 1 DATA CHECK - Indicates state of Channel 1 transmission flip-flop.

10. CHANNEL 1 CNTRL. CHECK - Indicates state of Channel 1 Control Check flip-flop.

11. CHANNEL 2 DATA CHECK - Indicates state of Channel 2 Transmission flip-flop.

12. CHANNEL 2 CNTRL. CHECK - Indicates state of Channel 2 Control Check flip-flop.

COMMUNICATIONS ACTIVITY DISPLAY GROUP

These indicators show the adapter/modem status for the 15 communications channels and the integrated communications adapter as follows:

- RECEIVED DATA (BB) - The ON condition indicates that the line is in the spacing condition (i.e., a binary zero). The OFF condition indicates that the line is in the marking condition (i.e., a binary one).

- TRANSMITTED DATA (BA) - The ON condition indicates that the line is in the spacing condition (i.e., a binary zero). The OFF condition indicates that the line is in the marking condition (i.e., a binary one).

- CLEAR TO SEND (CB) - The ON condition together with the ON condition on circuits CA, CC, and CD, indicates that the channel is in a transmit condition.

- RECEIVED LINE SIGNAL DETECTOR (CF) - The ON condition indicates that the modem is receiving a signal which meets its suitability criteria for demodulation.

- SECONDARY RECEIVED LINE SIGNAL DETECTOR (SCF) - The ON condition indicates the proper reception (where applicable) of the SECONDARY CHANNEL signal. It is used to indicate the circuit assurance status and to signal a reverse channel interrupt condition.

- DATA SET READY (CC) - The ON condition on this circuit is presented to indicate that the modem is connected to a communication channel and, for an auto answer network, has completed the transmission of the answer tone. For a private line, the ON condition indicates that the modem is ready.

- OFF HOOK (OH) - When answering a call, this signal ultimately completes a dc path to the serving Central Office, activating the incoming ringing signal. When originating a call, this lead is operated to obtain dial tone and then pulsed to generate the desired dial digits.

- RING INDICATOR (CE) - The ON condition indicates that a ringing signal is being received on the communication channel.

NOTE

Since under normal operation the communications handler will answer a call on the leading edge of the ringing signal, the ON condition on this indicator implies either a malfunction or that the channel is not enabled.

- ENABLE (EN) - The ON condition indicates that the line adapter is enabled and is therefore not in the master clear or loop test mode.

OPERATING PROCEDURES

GENERAL

This paragraph contains procedures which may be executed from the System Control Panel. These procedures enable loading control or main storage from either disc or cards, reading from or writing into main storage or registers within register files or register options, and executing programs.

Modes of Operation

The System Control Panel enables the system to operate in one of two fundamental control modes: processor control and console control. These two modes are not mutually exclusive from the hardware point of view, but should be clearly distinguished and kept separate in operating practice. This separation is necessary since the console mode can directly alter the contents of storage and registers and in this way could completely disrupt processor mode operations.

- The processor control mode is selected basically by the eight PROCESSOR CONTROL SELECT switches, the PROCESSOR SELECT selector, and the PROCESSOR RUN pushbutton. This mode enables the operator, in connection with programmed operations, to directly control execution of instructions by all eight processor states. Thus, individual processor states may be switched on and off or may be made to run one instruction at a time (STOP/STEP mode), etc. Except for the internal effects of the programs themselves, the processor mode does not enable the contents of storage to be altered.

- The console control mode is selected basically by the CONSOLE CONTROL SELECT switch, the CONSOLE MODE SELECT selector, and the CONSOLE RUN pushbutton. This mode does not involve any actual execution of instructions by a processor state, but allows any individual cell of main or control storage or any of the hardware registers to be displayed or altered under either hardware or software control. The panel is allocated major cycles just as though it were a ninth processor.

Each of the fundamental control modes is influenced by the three operating modes: operator mode, program mode, and maintenance mode. The three modes each determine a certain level of operating capability available to the operator.

1. The operator mode, selected when neither the PROGRAM MODE or MAINTENANCE MODE pushbutton is activated, restricts the operator to use of the operator group controls only. This group allows the operator to turn on and turn off the system, perform reset/load and autoload operations, and detect fault and status conditions. These operations are always available to the operator regardless of whether the system is in the processor mode or console mode.

2. The program mode, selected by the PROGRAM MODE push-button, enables an operator to use the controls of the programmer group as well as those of the operator group. This additional capability allows the operator to place the system in either the processor control or console control mode, thus enabling operations associated with these two control modes to be carried out.

3. The maintenance mode, selected by the MAINTENANCE MODE pushbutton, enabled an operator to use controls of the maintenance group in addition to those of the operator and program group. These controls allow the operator to initiate maintenance-related activities when operating in either the processor control or console control mode.

Breakpoint Facility

The breakpoint facility provides a way of terminating processor mode or console mode operations at a specific point in either main storage or control storage (including the first-level decode address table). This facility may be invoked if the selected processor is started either from the panel (PROCESSOR RUN pushbutton) or by internal operations, or if the computer is already executing instructions. During processor mode operations, the breakpoint operation is initiated by setting one of the PROCESSOR CONTROL SELECT switches to BREAKPOINT. The processor then proceeds until the storage location selected on the BREAKPOINT MODE SELECT selectors is accessed, at which point the processor stops. This breakpoint stop is interpreted in one of three ways, as selected by a corresponding breakpoint mode switch: READ INSTR, READ DATA, and WRITE DATA. Activating the READ INSTR switch will stop the processor after it reads the instruction at the breakpoint address. Activating the READ DATA switch will stop the processor after it reads the operand at the breakpoint address. Activating the WRITE DATA switch will stop the processor after it stores the operand at the breakpoint address.

NOTE

> Word mode addressing will not result in a breakpoint stop where the right-most byte (odd-numbered) address of the referenced word is designated in the breakpoint address switches. An example is the case of MS-RD or MS-WR operations which will not perform a breakpoint stop if the right-most byte address is designated by the breakpoint address switches.

A breakpoint stop activated by the READ INSTR switch will load only the first two bytes of an instruction. Thus, the reading of the M1, M2, L1, and L2 portions of 4-, 6-, and 8-byte instructions are treated as operand references for breakpoint purposes.

For console mode operations (when the CONSOLE CONTROL SELECT switch is set to BREAKPOINT), the breakpoint stop will always occur at the end of the storage reference cycle in which data is read or written at the breakpoint address.

SWITCHING POWER ON AND OFF

CAUTION

> During an emergency situation (conditions involving a safety hazard), power may be shut down by pulling the EMERGENCY PULL knob. However, pulling this knob can result in extensive equipment damage, including disc head crashing and loss of data in main storage. Use this knob only when a definite emergency situation exists; otherwise, use the POWER OFF switch described below.

To turn the computer on, insure that the LOCAL/REMOTE switch is in the LOCAL position; then simply press the POWER ON pushbutton. Upon completion of the power-up sequence, the POWER ON indicator will light. (The internal power-up switching sequence for the computer and disc drives is performed by the hardware.)

To turn the computer off, press and hold the POWER OFF pushbutton for about two seconds. (The delayed action of this switch is designed to prevent turning off power inadvertently.) The POWER OFF indicator will light.

LOADING CONTROL STORAGE FROM DISC

Loading control storage (CS) from the disc via the Panel can be performed in one of two ways: from a power-on condition or using the RESET/LOAD pushbutton. Essentially, the power-on condition loads CS when power is initially applied to the system (pressing the POWER ON pushbutton); using the RESET/LOAD pushbutton loads CS in the same manner as pressing the POWER ON pushbutton, but after power has been applied. Each of the two ways depends in which operating mode the Panel has been placed; operator mode, program mode, or maintenance mode. Generally, operator mode provides the maximum amount of internal hardware control with the least amount of operator intervention. In contrast, maintenance mode requires the greatest amount of operator intervention, but provides the greatest amount of flexibility in using the panel controls.

Power-On Condition

Loading CS from the disc by a power-on condition is normally performed in either the operator mode or program mode.

Operator Mode

1. Set the LOAD SELECT switch to DISC.

2. Select one, and only one, of the disc drives as logical drive 0 by partially inserting plug 0 into the drive select slot. (Do not insert plug all the way in at this time.)

3. Mount disc pack and enable power to disc drive 0 by pressing the START switch. (Insure that the READ ONLY and ENABLE switches are set.)

4. Press the POWER ON pushbutton. Upon completion of the power-up sequence and the restore operation (about 1 minute), drive number 0 in the select plug will light.

5. Set the MAINTENANCE MODE and PROGRAM MODE pushbuttons to the off position (can be done while step 4 progresses).

6. Complete selection of disc drive 0 by fully inserting plug 0. When drive heads have been restored and the power-on sequence has been completed, CS load will begin. Disc data will be loaded in sequential locations starting at address 0000 (hex) into both CS and the FRJ Decode Address Table, automatically followed by a load of MS.

Program Mode

1. Set the CONSOLE MODE SELECT selector to OFF and the CONSOLE DATA REGISTER SELECT selector to DATA.

2. Set the LOAD SELECT switch to DISC.

3. Select one, and only one, of the disc drives as logical drive 0 by partially inserting plug 0 into the drive select slot. (Do not insert plug all the way in at this time.)

4. Mount disc pack and enable power to disc drive 0 by pressing the START switch. (Insure that the READ ONLY and ENABLE switches are set.)

5. Press the POWER ON pushbutton. Upon completion of the power-up sequence and the restore operation (about 1 minute), drive number 0 in the select plug will light.

6. Set the MAINTENANCE MODE pushbutton to the off position and the PROGRAM MODE pushbutton to the on position (can be done while step 5 progresses).

7. Complete selection of disc drive 0 by fully inserting plug 0. When drive heads have been restored and the power-on sequence has been completed, CS load will begin. Disc data will be

loaded in sequential locations starting at address 0000 (hex) into both CS and the FRJ Decode Address Table, automatically followed by a load of MS.

Reset/Load Condition

Loading CS from the disc by pressing the RESET/LOAD pushbutton can be performed in the operator mode, program mode, or maintenance mode.

Operator Mode

1. Set the MAINTENANCE MODE and the PROGRAM MODE pushbuttons to the off position.

2. Set the LOAD SELECT switch to DISC.

3. Place disc pack on the disc drive selected as logical 0 and enable power to the drive by pressing the START switch. (Insure that the READ ONLY and ENABLE switches are pressed.)

4. Press the RESET/LOAD pushbutton. Disc data will be loaded in sequential locations starting at address 0000 (hex) into both CS and the FRJ Decode Address Table, automatically followed by a load of MS.

Program Mode

1. Set the MAINTENANCE MODE pushbutton to the off position and the PROGRAM MODE pushbutton to the on position.

2. Set the CONSOLE MODE SELECT selector to OFF and the CONSOLE DATA REGISTER SELECT selector to DATA.

3. Set the LOAD SELECT switch to DISC.

4. Place disc pack on the disc drive selected as logical 0 and enable power to the drive by pressing the START switch. (Insure that the READ ONLY and ENABLE switches are pressed.)

5. Press the RESET/LOAD pushbutton. Disc data will be loaded in sequential locations starting at address 0000 (hex) into both CS and the FRJ Decode Address Table, automatically followed by a load of MS.

Maintenance Mode

Preconditions.

NOTE

In all procedures listed, preconditions must be satisfied before the procedure can be executed.

1. MAINTENANCE MODE pushbutton/indicator ON.
2. CS DISABLE switch at OFF.
3. CONSOLE MODE SELECT selector at CS-WR.
4. CONSOLE CONTROL SELECT switch at STOP/STEP.
5. CONSOLE DATA REGISTER SELECT selector at DATA.*

Procedure for Loading Standard Microcode From 0000 (Hex)

1. Set the LOAD SELECT switch to DISC.
2. Place disc pack on the disc drive selected as logical 0 and enable power to the drive by pressing the START switch. (Insure that the READ ONLY and ENABLE switches are pressed.)
3. If disc pack is already mounted but disc heads are at an unknown position, restore them to cylinder 0 by partially removing and reinserting select plug 0.
4. Press SYSTEM RESET pushbutton.
5. Press RESET/LOAD pushbutton. Disc data will be read into control storage starting at the location contained in the Su-Register (in this case, 0000, since pressing SYSTEM RESET pushbutton generated a system reset condition). If load runs to completion, Control Storage and Address Table will be completely loaded. If load stops before completion (occurrence of burst check error), Su will contain address of last word loaded +1.

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*This step is optional since a CS write operation unconditionally forces data to be entered into the data register and contents of Su to be displayed via the address register indicators, regardless of the address and data register selector settings. It is suggested, however, that this step be performed as an aid in recalling which register contents are being displayed.

6. Upon completion of load, note BURST CHECK indicator in the maintenance group. If indicator is off, data was transferred from disc without a cyclic error. If indicator is lit, a cyclic error occurred.* Repeat steps 3, 4, and 5 to try a reload.

Verification (Optional). To check that control storage has been loaded properly, execute a control storage scan as follows:

1. Set CONSOLE MODE SELECT selector to CS-RD.
2. Set CONSOLE ADDRESS REGISTER DISPLAY selector to Su and CONSOLE DATA REGISTER DISPLAY selector to CSS.**
3. Position CONSOLE CONTROL SELECT switch to NORMAL.
4. Position STORAGE PARITY DISABLE switch to OFF.
5. Press SYSTEM RESET pushbutton.
6. Press CONSOLE RUN pushbutton. Su-Register display will stop on last address of first page (256-word block) in which a longitudinal parity error occurred, and on last address of succeeding pages containing parity errors upon pressing CONSOLE RUN button after last error stop. Su-Register display will also stop on last address of first unused page. Upon stopping at error, CSS register display will contain all 1's except in positions of bits that failed (and bits 9 and 10, which are not used). If no errors occur, it will keep running. Parity errors within the address table are detected by performing a horizontal parity check on bits 7 through 15 of each word stored (bits 0 through 6 are forced by hardware and are not checked). Check will stop on address of error where even parity was detected.

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*Bit 00 of the Console Address register display will also be lit if a cyclic error occurred.

**These steps are optional since a CS read operation unconditionally forces contents of Su to be displayed via address register indicators and contents of CSS to be displayed via data register indicators regardless of the address and data register selector settings. It is suggested, however, that these steps be performed as an aid in recalling which register contents are being displayed.

7. Stop the CS scan operation by momentarily setting the CONSOLE CONTROL SELECT switch to the STOP position.

LOADING CONTROL STORAGE FROM CARDS

Loading control storage (CS) from cards can be performed in one of two ways: from a power-on condition or using the RESET/LOAD pushbutton. Essentially, the power-on condition loads CS when power is initially applied to the system (pressing the POWER ON pushbutton); using the RESET/LOAD pushbutton loads CS in the same manner as pressing the POWER ON pushbutton, but is used after power is already on. Each of the two ways depends in which operating mode the Panel has been placed: operator mode, program mode, or maintenance mode. Generally, the operator mode provides the maximum amount of internal hardware control with the least amount of operator intervention. In contrast, the maintenance mode requires the greatest amount of operator intervention, but offers the greatest amount of flexibility in using the Panel controls.

Power-On Condition

Loading CS from cards by a power-on condition is normally performed in either the operator mode or the program mode.

Operator Mode

1. Set the LOAD SELECT switch to CR (if loading from card reader) or to R/P (if loading from reader/punch).
2. Press the POWER ON pushbutton.
3. Set the MAINTENANCE MODE and PROGRAM MODE pushbuttons to the OFF position.
4. Place microprogram card deck in the card hopper and start the card reader device. Card data will be loaded in sequential locations starting at address 0000 (hex) into both CS and the FRJ Decode Address Table.

Program Mode

1. Set the LOAD SELECT switch to CR (if loading from card reader) or to R/P (if loading from reader/punch).

2. Press the POWER ON pushbutton.

3. Set the MAINTENANCE MODE pushbutton to the OFF position and the PROGRAM MODE pushbutton to the ON position.

4. Set the CONSOLE MODE SELECT selector to OFF and the CONSOLE DATA REGISTER SELECT selector to DATA.

5. Place microprogram card deck in the card hopper and start the card reader device. Card data will be loaded in sequential locations starting at address 0000 (hex) into both CS and the FRJ Decode Address Table.

Reset/Load Condition

Loading CS from cards by pressing the RESET/LOAD pushbutton can be performed in the operator mode, program mode, or maintenance mode.

Operator Mode

1. Set the MAINTENANCE MODE and PROGRAM MODE pushbuttons to the OFF position.

2. Set the LOAD SELECT switch to CR (if loading from card reader) or R/P (if loading from reader/punch).

3. Place microprogram card deck in the card hopper and start the card reader device.

4. Press the RESET/LOAD pushbutton. Card data will be loaded in sequential locations starting at address 0000 (hex) into both CS and the FRJ Decode Address Table.

Program Mode

1. Set the MAINTENANCE MODE pushbutton to the OFF position and the PROGRAM MODE pushbutton to the ON position.

2. Set the CONSOLE MODE SELECT selector to CS-WR and the CONSOLE DATA REGISTER SELECT selector to DATA.

3. Set the LOAD SELECT switch to CR (if loading from card reader) or R/P (if loading from reader/punch).

4. Place microprogram card deck in the card hopper and start the card reader device.

5. Press the RESET/LOAD pushbutton. Card data will be loaded in sequential locations starting at address 0000 (hex) into both CS and the FRJ Decode Address Table.

Maintenance Mode

Preconditions.

1. MAINTENANCE MODE pushbutton/indicator ON.

2. CS DISABLE switch at OFF.

3. CONSOLE MODE SELECT selector at CS-WR.

4. CONSOLE CONTROL SELECT switch at STOP/STEP.

5. CONSOLE DATA REGISTER SELECT selector at DATA.*

---

*This step is optional since a CS write operation unconditionally forces data to be entered into the data register and contents of Su to be displayed via the address register indicators, regardless of the address and data register selector settings. It is suggested, however, that this step be performed as an aid in recalling which register contents are being displayed.

Procedure for Loading Standard Microcode From 000 (Hex).

1. Position LOAD SELECT switch to CR (if loading from card reader) or R/P (if loading from reader/punch).

2. Place microprogram card deck in card hopper and start the card reader device.

3. Press SYSTEM RESET pushbutton.

4. Press RESET/LOAD pushbutton. Cards will be read into control storage starting at the location contained in the Su-Register (in this case, 0000, since pressing SYSTEM RESET generated a system reset condition). On completion of the load, Su will contain the last word address +1, unless Control Storage and Address Table were completely loaded.

Procedure for Loading at Locations Other Than 0000 (Hex).

1. Select starting load location on BREAKPOINT ADDRESS SELECT selectors.

2. Set CONSOLE ADDRESS REGISTER SELECT selector to Su.*

3. Position CONSOLE CONTROL SELECT switch to BREAKPOINT.

4. Press CONSOLE RUN pushbutton. The Su-Register will now contain selected breakpoint address (indicated in CONSOLE ADDRESS REGISTER DISPLAY indicators).

5. Position LOAD SELECT switch to ALTERNATE (for card reader load).

6. Place microprogram card deck to be loaded in card reader and press the START button on the card reader.

7. Press RESET/LOAD pushbutton. Cards will be read into storage, starting at the location contained in the Su-Register. If load runs to completion, Control Storage and Address Table will be completely loaded. If load stops before completion, S will contain address of last word loaded +1.

---

*This step is optional since a CS write operation unconditionally forces data to be entered into the data register and contents of Su to be displayed via the address register indicators, regardless of the address and data register selector settings. It is suggested, however, that this step be performed as an aid in recalling which register contents are being displayed.

Verification (Optional). To check that control storage has been loaded properly, execute a control storage scan as follows:

1. Set CONSOLE MODE SELECT selector to CS-RD.
2. Set CONSOLE ADDRESS REGISTER DISPLAY selector to Su and CONSOLE DATA REGISTER DISPLAY selector to CSS.*
3. Position CONSOLE CONTROL SELECT switch to NORMAL position.
4. Position STORAGE PARITY DISABLE switch to OFF.
5. Press SYSTEM RESET pushbutton.
6. Press CONSOLE RUN Pushbutton. Su-Register display will stop on last address of first page (256-word block) in which a longitudinal parity error occurred, and on last address of succeeding pages containing parity errors upon pressing CONSOLE RUN pushbutton after last error stop. Su-Register display will also stop on last address of first unused page. Upon stopping at error, CSS register display will contain all 1's except in positions of bits that failed (and bits 9 and 10, which are not used). If there are no errors, it will keep running. Parity errors within the address table are bits 7 through 15 of each word stored (bits 0 through 6 are forced by hardware and are not checked). Check will stop on address of error where even parity was detected.
7. Stop the CS scan operation by momentarily setting the CONSOLE CONTROL SELECT switch to the STOP position.

LOADING MAIN STORAGE FROM DISC

Loading main storage (MS) from the disc can be accomplished in one of two ways: from a power-on condition or using the AUTOLOAD pushbutton. An MS load occurs automatically upon completion of the CS and FRJ Decode Address Table load if CS was loaded from a power-on or reset/load condition in either the operator mode or program mode. This paragraph, therefore, only describes loading of MS using the AUTOLOAD pushbutton in any of the three modes.

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*These steps are optional since a CS read operation unconditionally forces contents of Su to be displayed via address register indicators and contents of CSS to be displayed via data register indicators regardless of the address and data register selector settings. It is suggested, however, that these steps be performed as an aid in recalling which register contents are being displayed.

Autoload Condition

NOTE

Control storage must have been previously loaded to perform this operation.

1. If in Maintenance mode, set CS DISABLE, SET Au, SET Bu, and SELECT EVEN PARITY BYTE 0 and 1 switches at OFF.

2. Set LOAD SELECT switch to DISC.

3. Press AUTOLOAD pushbutton. Disc data will be loaded into MS in sequential locations starting at address 0000 (hex). Upon completion of the load, the address register indicators will contain the last word address +2.

LOADING MAIN STORAGE FROM CARDS

Loading MS from cards is accomplished by using the RESET/LOAD pushbutton. The operation can be performed only in the Maintenance mode.

Preconditions

NOTE

Control Storage must have been previously loaded to perform this operation.

1. MAINTENANCE MODE pushbutton/indicator ON.

2. CS DISABLE, SET Au, SET Bu, and SELECT EVEN PARITY BYTE 0 and 1 switches at OFF.

3. CONSOLE MODE SELECT selector at MS-WR.

4. CONSOLE CONTROL SELECT switch at STOP/STEP.

5. CONSOLE DATA REGISTER SELECT selector at DATA.

Procedure

1. Position LOAD SELECT switch to CR (if loading from card reader) or R/P (if loading from reader/punch).

2. Place card deck in card hopper and start the card reader device.

3. Set CONSOLE ADDRESS REGISTER DISPLAY pushbuttons to starting address.

4. Press RESET/LOAD pushbutton. Cards will be read into main storage using the contents of the Console Address register as the starting address. Upon completion of the load, the address register indicators will contain the last word address +2.

READING CONTROL STORAGE

Preconditions

1. MAINTENANCE MODE pushbutton/indicator ON.

2. CS DISABLE switch at OFF (down).

3. CONSOLE MODE SELECT selector at CS-RD.

4. CONSOLE DATA REGISTER SELECT selector at CSS.*

---

*This step is optional since a CS read operation unconditionally forces contents of Su to be displayed via address register indicators and contents of CSS to be displayed via data register indicators regardless of the address and data register selector settings. It is suggested, however, that this step be performed as an aid in recalling which register contents are being displayed.

Procedure

It is not possible to read directly from any control storage location or block of locations other than 0000 (hex) without first performing a breakpoint scan up to the starting location minus 1, since Su cannot be entered directly. For locations near 0000 (hex), however, it is easier to manually step to the desired location by setting the CONSOLE MODE SELECT selector to CS-RD, CONSOLE CONTROL SELECT switch to STOP/STEP, and pressing the CONSOLE RUN button for each address to be stepped.

Breakpoint Scan

1. Set CONSOLE MODE SELECT selector to CS-RD.

2. Position BREAKPOINT ADDRESS SELECT selectors to address minus 1 of location to be read.

3. Position CONSOLE CONTROL SELECT switch to BREAKPOINT.

4. Press CONSOLE RUN pushbutton. The Su-Register will be counted up to the breakpoint address. (Set CONSOLE ADDRESS REGISTER selector to Su to observe.)* The CONSOLE DATA REGISTER indicators (CSS) will now display a partial check sum. (All bit positions are used except 9 and 10.)

Displaying Contents of Consecutive Locations

After breakpoint scan:

1. Position CONSOLE CONTROL SELECT switch to STOP/STEP.

2. Press CONSOLE RUN pushbutton. Each time CONSOLE RUN button is pressed, Su will be increased by 1 and the contents of the next location will be displayed in the CONSOLE DATA REGISTER DISPLAY indicators.

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*This step is optional since a CS read operation unconditionally forces contents of Su to be displayed via address register indicators and contents of CSS to be displayed via data register indicators regardless of the address and data register selector settings. It is suggested, however, that this step be performed as an aid in recalling which register contents are being displayed.

WRITING CONTROL STORAGE

Preconditions

1. MAINTENANCE MODE pushbutton/indicator ON.
2. CS DISABLE switch at OFF.
3. CONSOLE MODE SELECT selector at CS-RD.
4. CONSOLE DATA REGISTER SELECT selector at CSS.*

Procedure

It is not possible to write directly into any control storage location or block of locations other than 0000 (hex) without first performing a breakpoint scan up to the starting location, since Su cannot be entered directly. For locations near 0000 (hex), however, it is easier to manually step to the desired location by setting the CONSOLE MODE SELECT selector to CS-RD, CONTROL SELECT switch to STOP/STEP, and pressing the CONSOLE RUN button for each address to be stepped.

Breakpoint Scan

1. Set CONSOLE MODE SELECT selector to CS-RD.
2. Position BREAKPOINT ADDRESS SELECT selectors to address of location to be written.
3. Position CONSOLE CONTROL SELECT switch to BREAKPOINT.
4. Press CONSOLE RUN pushbutton. The Su-Register will be counted up to the breakpoint address. (Set CONSOLE ADDRESS REGISTER selector to Su to observe.) The CONSOLE DATA REGISTER indicators (CSS) will now display a partial check sum.

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*This step is optional since a CS read operation unconditionally forces contents of Su to be displayed via address register indicators and contents of CSS to be displayed via data register indicators regardless of the address and data register selector settings. It is suggested, however, that this step be performed as an aid in recalling which register contents are being displayed.

Entering Data

After breakpoint scan:

1. Set CONSOLE MODE SELECT selector to CS-WR.

2. Position CONSOLE CONTROL SELECT switch to STOP/STEP.

3. Set the 14-bit word to be written (not using bits 9 and 10) into the Console Data register. Make sure that odd parity is maintained (bit 8 is parity bit).

4. Press CONSOLE RUN pushbutton. Each time CONSOLE RUN pushbutton is pressed, contents of the Console Data register display will be written into storage location specified by Su, and Su count will be increased by 1. To insure proper scan operation, the check word in the particular page must also be corrected.

5. To enter the contents of the Console Data register into all control storage locations, set CONSOLE CONTROL SELECT switch to NORMAL position and depress the CONSOLE RUN pushbutton.

READING MAIN STORAGE

Preconditions

NOTE

Control storage must have been previously loaded to perform this operation.

1. MAINTENANCE MODE or PROGRAM MODE pushbutton/indicator ON.

2. If in Maintenance mode, set CS DISABLE, SET Au, and SET Bu switches at OFF.

3. CONSOLE MODE SELECT selector at MS-RD.

4. CONSOLE CONTROL SELECT switch at STOP/STEP.

5. CONSOLE ADDRESS REGISTER SELECT selector at ADDRESS.

6. CONSOLE DATA REGISTER SELECT selector at DATA.

Procedure

1. Press CLEAR ADDRESS pushbutton.

2. Set the address of the main storage location to be read into the CONSOLE ADDRESS REGISTER DISPLAY pushbuttons.

3. Press the CONSOLE RUN pushbutton. Contents of selected location will be displayed in the CONSOLE DATA REGISTER DISPLAY indicators.

4. To read up to an address, enter starting address of block into CONSOLE ADDRESS REGISTER DISPLAY pushbuttons and ending address into BREAKPOINT ADDRESS SELECT selectors. Position CONSOLE CONTROL SELECT switch to BREAKPOINT and press CONSOLE RUN pushbutton.

5. To step through individual storage locations, repeat Step 4, except position CONSOLE CONTROL SELECT switch to STOP/STEP. Contents of each storage location will be displayed in sequence each time CONSOLE RUN pushbutton is pressed.

6. To dynamically read a storage location in the normal (continuous) mode, enter the word address of the location into the CONSOLE ADDRESS REGISTER DISPLAY pushbuttons with bit position 15 set. Set the CONSOLE CONTROL SELECT switch to NORMAL position and press the CONSOLE RUN pushbutton. The contents of the storage location entered in the console address register will be continuously displayed in the CONSOLE DATA REGISTER DISPLAY indicators.

WRITING MAIN STORAGE

Preconditions

NOTE

Control storage must have been previously loaded to perform this operation.

1. MAINTENANCE MODE or PROGRAM MODE pushbutton/indicator ON.

2. If in Maintenance mode, set CS DISABLE, SET Au, and SET Bu switches at OFF.

3. CONSOLE MODE SELECT selector at MS-WR.

4. CONSOLE CONTROL SELECT switch at STOP/STEP.

5. CONSOLE ADDRESS REGISTER SELECT selector at ADDRESS.

6. CONSOLE DATA REGISTER SELECT selector at DATA.

7. SELECT EVEN PARITY BYTE 0 and 1 pushbuttons to off position (if either is on, incorrect parity will be written and detected during subsequent read operation).

Procedure

1. Press CLEAR ADDRESS and CLEAR DATA pushbuttons.

2. Set the address of the main storage location to be written via the CONSOLE ADDRESS REGISTER DISPLAY pushbuttons.

3. Set the data to be written via the CONSOLE DATA REGISTER DISPLAY pushbuttons.

4. Press the CONSOLE RUN pushbutton. Contents of the data register will be written at the address specified in the CONSOLE ADDRESS REGISTER DISPLAY indicators.

5. To write the contents into all storage locations, set CONSOLE CONTROL SELECT switch to the NORMAL position and press the CONSOLE RUN pushbutton.

6. To write a block of data, enter starting address of block into the CONSOLE ADDRESS REGISTER SELECT pushbuttons and ending address into BREAKPOINT ADDRESS SELECT selectors. Position CONSOLE CONTROL SELECT switch to BREAKPOINT and press the CONSOLE RUN pushbutton. Contents of the data register will be written in sequence into all locations within the block.

7. To write data into individual storage locations within the block, repeat Step 6, except set the CONSOLE CONTROL SELECT switch to STOP/STEP. Contents of the data register will be written in individual locations in sequence each time the CONSOLE RUN pushbutton is pressed.

READING REGISTERS OF REGISTER FILES

Preconditions

NOTE

Control storage must have been previously loaded to perform this operation.

1. MAINTENANCE MODE or PROGRAM MODE pushbutton/indicator ON.
2. CS DISABLE switch at OFF.
3. CONSOLE MODE SELECT selector at RF-RD.
4. CONSOLE CONTROL SELECT switch at STOP/STEP.
5. CONSOLE ADDRESS REGISTER SELECT selector at ADDRESS.
6. CONSOLE DATA REGISTER SELECT selector at DATA.

Procedure

1. Press CLEAR ADDRESS pushbutton.
2. Set processor state number and number of the register in basic file or extended file (Group I or II*) into the CONSOLE ADDRESS REGISTER SELECT pushbuttons. Addresses of basic file and extended file, Groups I and II are listed in Figure 3-1.
3. Press CONSOLE RUN pushbutton. Contents of selected register will be displayed in bits 00 through 15 indicators of the CONSOLE DATA REGISTER DISPLAY. If the relocation and protection feature of the Register Option is present, contents of the segment tag register corresponding to the BRF register selected will be displayed in the X0 through X3 indicators of the CONSOLE DATA REGISTER DISPLAY.
4. To dynamically read a register in the normal (continuous) mode, repeat Steps 1 through 3, except set the CONSOLE CONTROL SELECT switch to the NORMAL position. The Console Data register indicators will continuously display the register contents as the running processor alters the contents.

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*The Group III registers of the extended register file many not be addressed by this mechanism.

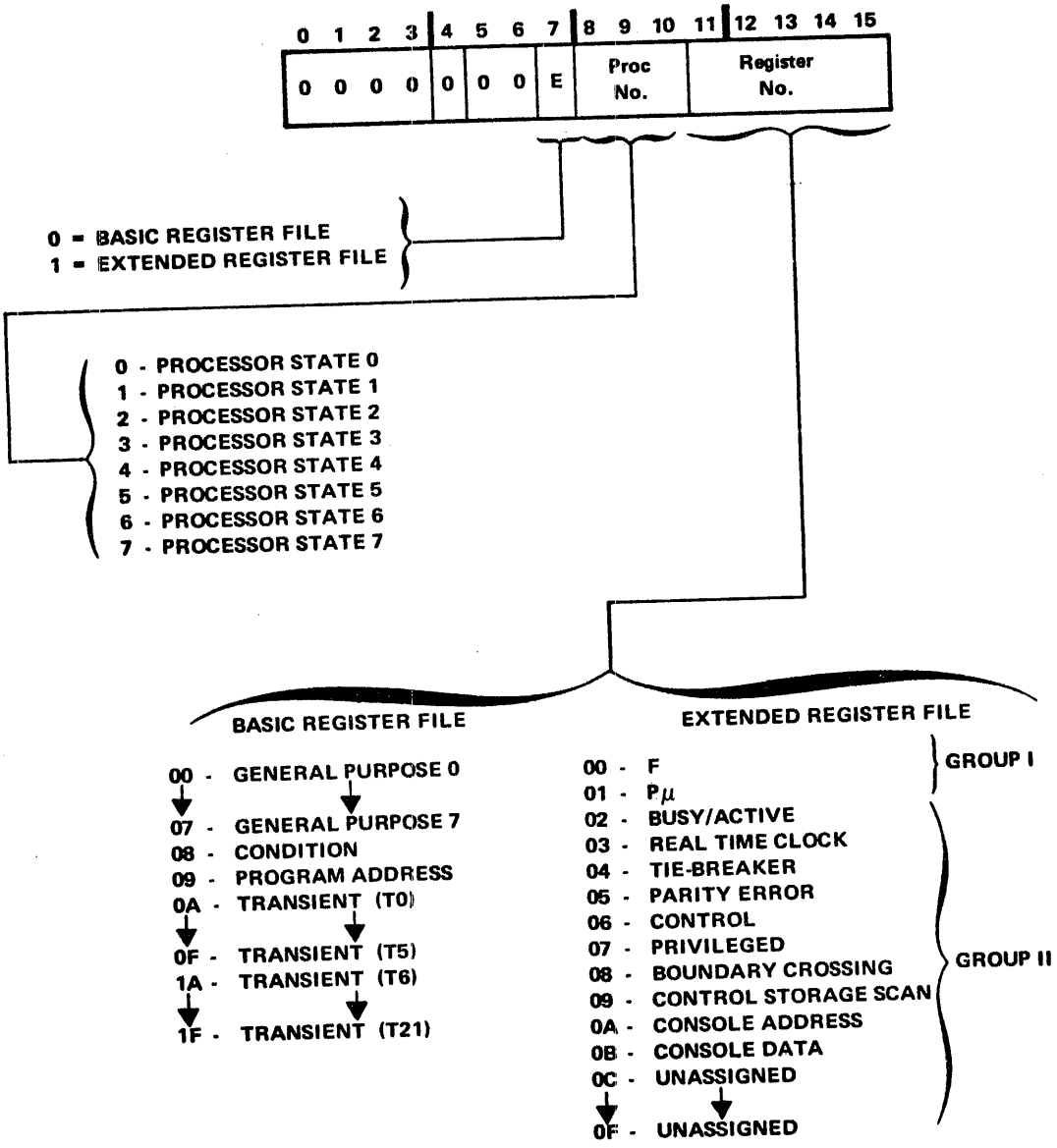

Figure 3-1. Register File and Associated Register Addresses

LOADING REGISTERS OF REGISTER FILES

Preconditions

NOTE

Control storage must have been previously loaded to perform this operation.

1. MAINTENANCE MODE or PROGRAM MODE pushbutton/indicator ON.
2. CS DISABLE switch at OFF.
3. CONSOLE MODE SELECT selector at RF-WR.
4. CONSOLE CONTROL SELECT switch at STOP/STEP.
5. CONSOLE ADDRESS REGISTER SELECT selector at ADDRESS.
6. CONSOLE DATA REGISTER SELECT selector at DATA.

Procedures

1. Press CLEAR ADDRESS and CLEAR DATA pushbuttons.
2. Set processor state number and number of the register in basic file or extended file (Group I or II*) via the CONSOLE ADDRESS REGISTER DISPLAY pushbuttons. Addresses of basic file and extended file, Groups I and II, are listed in Figure 3-1.
3. Set data to be loaded via the 00 through 15 pushbuttons of the CONSOLE DATA REGISTER DISPLAY. If the relocation and protection feature of the Register Option is present, load the segment tag associated with a selected BRF register into the X0 through X3 pushbuttons of the CONSOLE DATA REGISTER DISPLAY.
4. Press CONSOLE RUN pushbutton. Contents of Console Data register will be loaded into the selected processor register and corresponding segment tag register.

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*The Group III registers of the extended register file may not be addressed by this mechanism.

READING REGISTERS OF REGISTER OPTION

Preconditions

NOTE

Control Storage must have been previously loaded to perform this operation.

1. MAINTENANCE MODE or PROGRAM MODE pushbutton/indicator ON.
2. CS DISABLE switch at OFF.
3. CONSOLE MODE SELECT selector at RO-RD.
4. CONSOLE CONTROL SELECT switch at STOP/STEP.
5. CONSOLE ADDRESS REGISTER SELECT selector at ADDRESS.
6. CONSOLE DATA REGISTER SELECT selector at DATA.

Procedure

1. Press CLEAR ADDRESS button.
2. Set feature number, processor state number, and register number into the CONSOLE ADDRESS REGISTER DISPLAY pushbuttons as shown in Figure 3-2. There are two basic register address formats, depending on the feature selected. The first format is used to address feature registers associated with particular processor states. This format requires specifying the feature number only. Addresses of all registers in the register option are shown in Figure 3-3.
3. Press CONSOLE RUN pushbutton. Contents of selected register will be displayed in the CONSOLE DATA REGISTER DISPLAY registers.

LOADING REGISTERS OF REGISTER OPTION

Preconditions

NOTE

Control storage must have been previously loaded to perform this operation.

1. MAINTENANCE MODE or PROGRAM MODE pushbutton/indicator ON.
2. CS DISABLE switch at OFF.
3. CONSOLE MODE SELECT selector at RO-WR.
4. CONSOLE CONTROL SELECT switch at STOP/STEP.
5. CONSOLE ADDRESS REGISTER SELECT selector at ADDRESS.
6. CONSOLE DATA REGISTER SELECT selector at DATA.

Procedure

1. Press CLEAR ADDRESS and CLEAR DATA pushbuttons.
2. Set feature number, processor state number, and register number via the CONSOLE ADDRESS REGISTER DISPLAY pushbuttons as shown in Figure 3-2. Addresses of all registers of the option are listed in Figure 3-3.
3. Set the data to be loaded via the CONSOLE DATA REGISTER DISPLAY pushbuttons.
4. Press CONSOLE RUN pushbutton. Contents of the Console Data register will be loaded into the selected register.

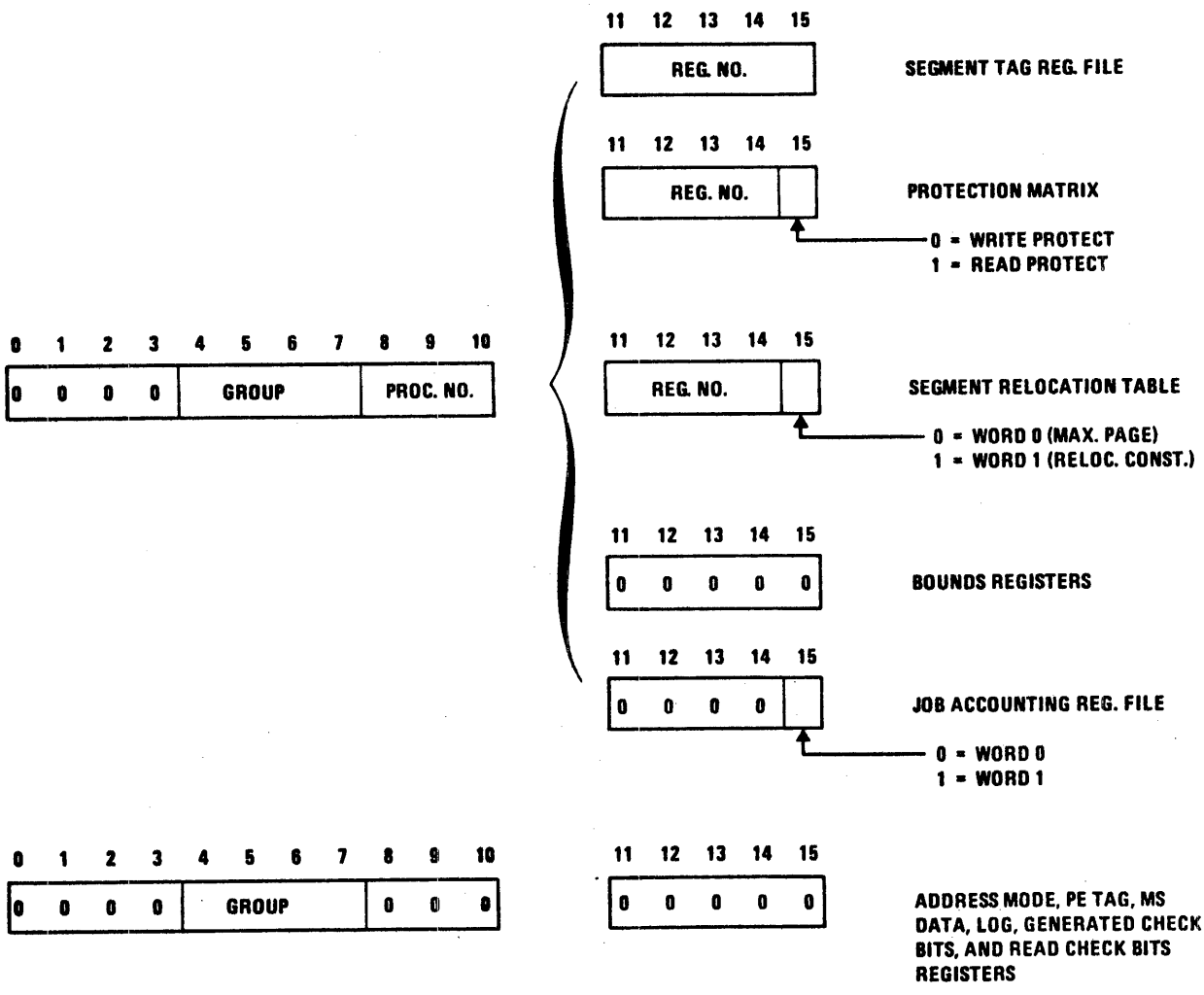


Figure 3-2. Register Option Address Format

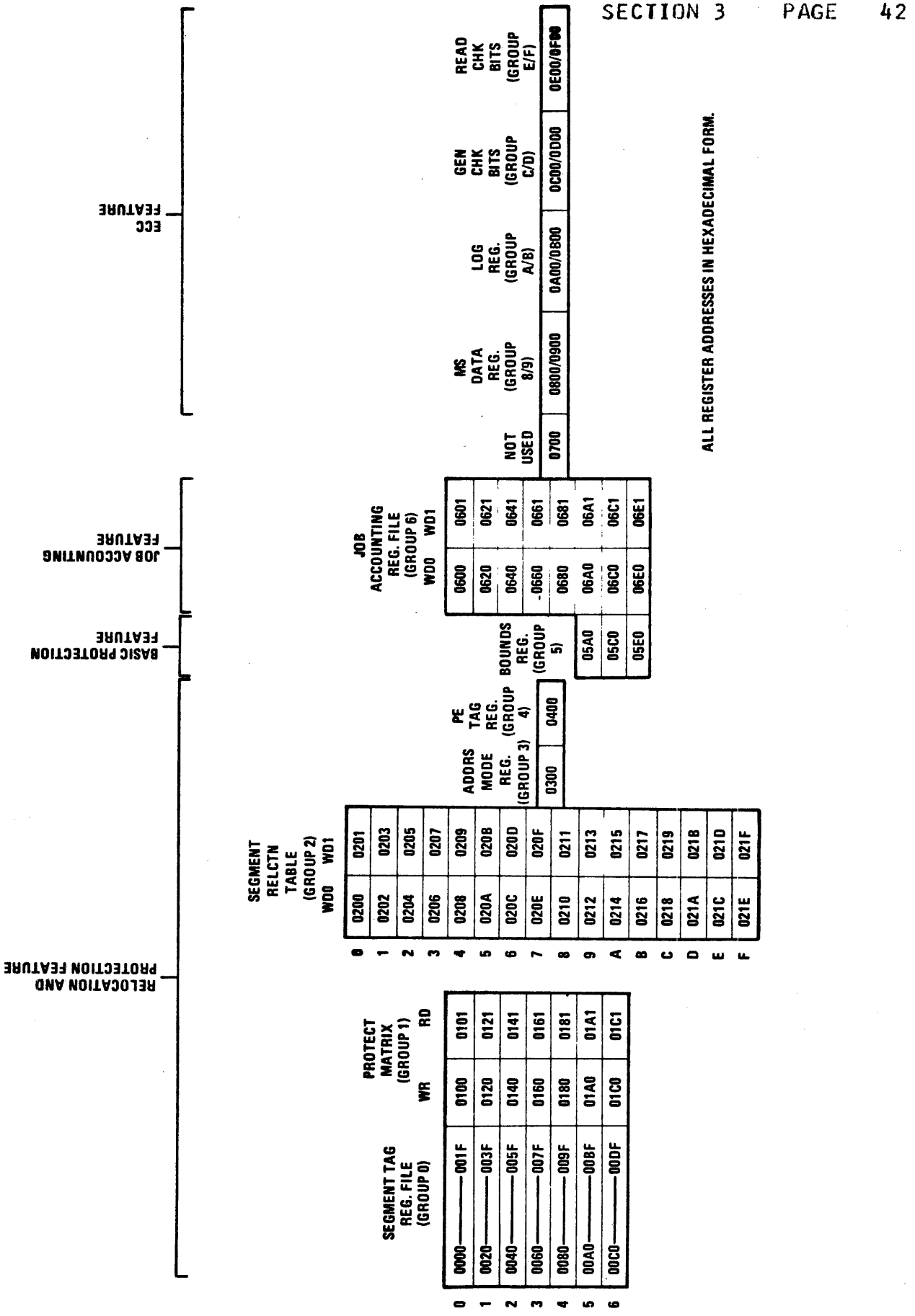


Figure 3-3. Register Option and Associated Register Addresses

READING SHARED RESOURCES REGISTERS

Preconditions

1. MAINTENANCE MODE or PROGRAM MODE pushbutton ON.
2. CS DISABLE switch at OFF.

Procedure

1. Press CLEAR ADDRESS and CLEAR DATA pushbuttons.
2. Set either CONSOLE ADDRESS REGISTER SELECT or CONSOLE DATA REGISTER SELECT selector to the register to be read. The contents of the register selected will be dynamically displayed in either the CONSOLE ADDRESS or CONSOLE DATA REGISTER DISPLAY indicators.

EXECUTING PROGRAMS

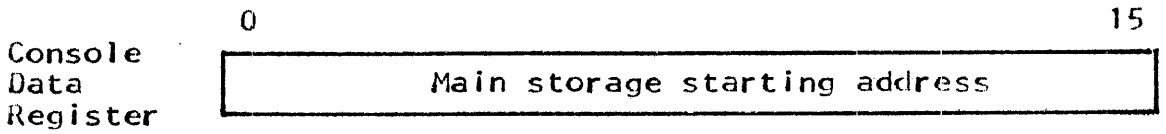
Preconditions

1. MAINTENANCE MODE or PROGRAM MODE pushbutton/indicators ON.
2. CS DISABLE switch at OFF.

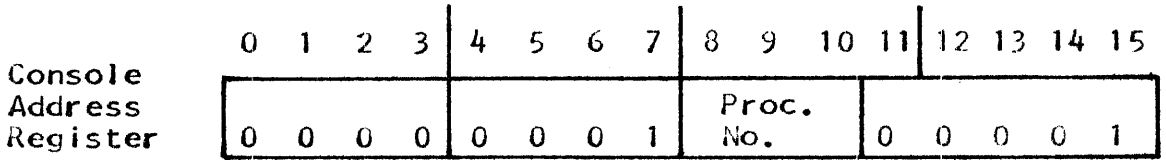
Procedure

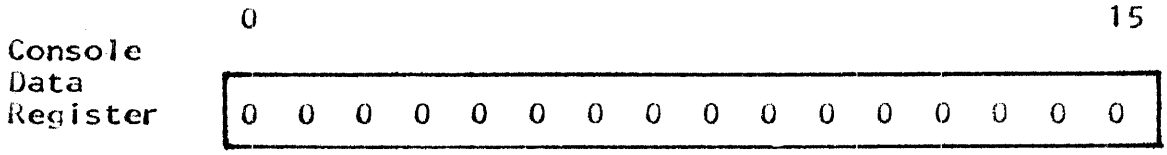
1. Use the Loading-Register-of-Register-File procedure to load desired main storage starting address into the P-Register (R9) of the processor to be run.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Console Address Register	0	0	0	0	0	0	0	0	Proc. No.				0	1	0	0	1



2. Use the Loading-Register-of-Register-File procedure to load 0000 (hex) into the Pu-Register (extended R1) of the processor* to be run:





3. If it is desired to start the processor at a particular location other than 0000 (hex) in control storage (microcode), use the above procedure to load the address of this location into Pu from the CONSOLE DATA REGISTER DISPLAY pushbuttons.

4. Select processor state on the PROCESSOR SELECT selector.

5. Select mode of operation on appropriate PROCESSOR CONTROL SELECT switch.**

6. If processor state is set to the breakpoint mode, select breakpoint address on BREAKPOINT ADDRESS SELECT selectors and select type of breakpoint on READ INSTR, READ DATA, or WRITE DATA switches.**

NOTE

Selecting the breakpoint mode for processor state 4 will stop and lock out all processor start signals except those orginating from the panel.

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*If no other processor states are in use (executing uI subroutines), the SYSTEM RESET button may be used to clear Pu (it clears Pu of all processor states).

**Steps 5 and 6 may be executed after Step 7 for program stop/step or breakpoint operations.

7. Press PROCESSOR RUN pushbutton. Selected processor state will execute instructions commencing at location contained in its P- (or Pu-) Register. (If the PROCESSOR CONTROL SELECT switch is set to the STOP/STEP position, only one machine language instruction is executed each time the PROCESSOR RUN pushbutton is pressed. The STOP/STEP position also disables I/O-originated start signals (Request and Attention) for processor states 0 through 3.)

8. Repeat steps 1 through 7 for other processors to be run.

SECTION 4. PREVENTIVE MAINTENANCE AND MAINTENANCE AIDS

PREVENTIVE MAINTENANCE

Run preventive maintenance (PM) checks on the 7200/7300 Processing Unit at the intervals listed in Table 4-1.

REMOVING/INSERTING MODULES WITH POWER ON

Any module of chassis 1 or 2 may be removed or inserted with power applied to the system (POWER ON pushbutton on System Control Panel set to ON), except the following:

1. The HH modules in chassis 2 may not be removed or inserted with power on.

2. The integrated adapter modules in chassis 1 may be removed or inserted only if power to the corresponding external subsystem is shut down.

No module of chassis 3 may be removed or inserted with power applied to the system.

COMPONENT LOCATIONS

Locations of major assemblies comprising the Processing Unit are shown in Figure 4-1. Locations of PC modules in chassis 1, 2, and 3 are shown in the following drawings contained in the 7200/7300 Processing Unit Support Diagrams Manual:

Drawing No.	Title
505963, Vol. 2	Module Placement, Chassis 1
505965, Vol. 3	Module Placement, Chassis 2
504485, Vol. 1	Module Placement, Chassis 3

Locations of IC elements on each PC module in chassis 1 and 2 are shown in Figure 4-2.

TABLE 4-1. PREVENTIVE MAINTENANCE SCHEDULE

ACTION	INTERVAL
Run MS micro-diagnostics (Section 5).	1-week intervals until 2000 hrs. accumulated on elapsed time meter, then 3 months
Run CPU micro-diagnostics (Section 5).	3 months
Check power supply voltages. If out of tolerance, troubleshoot in accordance with Section 10.	6 months
Check air filter. Replace if necessary.	6 months
Check for frayed or otherwise damaged cables.	6 months
Check that all access panels are properly mounted.	6 months
Clean dust and dirt off covers.	6 months

REGISTER FILE

Organization of the register file, both the BRF and ERF, is shown in drawing 505983, sheet 1, of the Support Diagrams Manual, Volume 1. Sheet 2 of this drawing defines the meaning of bits in each register of the BRF and Groups 1 and 2 of the ERF that are set under hardware control. Bits set in Group 3 registers of the ERF (I/O registers) are defined in the respective section of the manual that covers each peripheral adapter (ICA, BDC, and IFA).

MICRO-INSTRUCTION REPERTOIRE

Drawing 504674, Microcommand Repertoire, of the Support Diagrams Manual contains the micro-instruction (uI) repertoire. Table 4-3 lists the FRJ decode branch addresses for each machine language instruction (MLI).

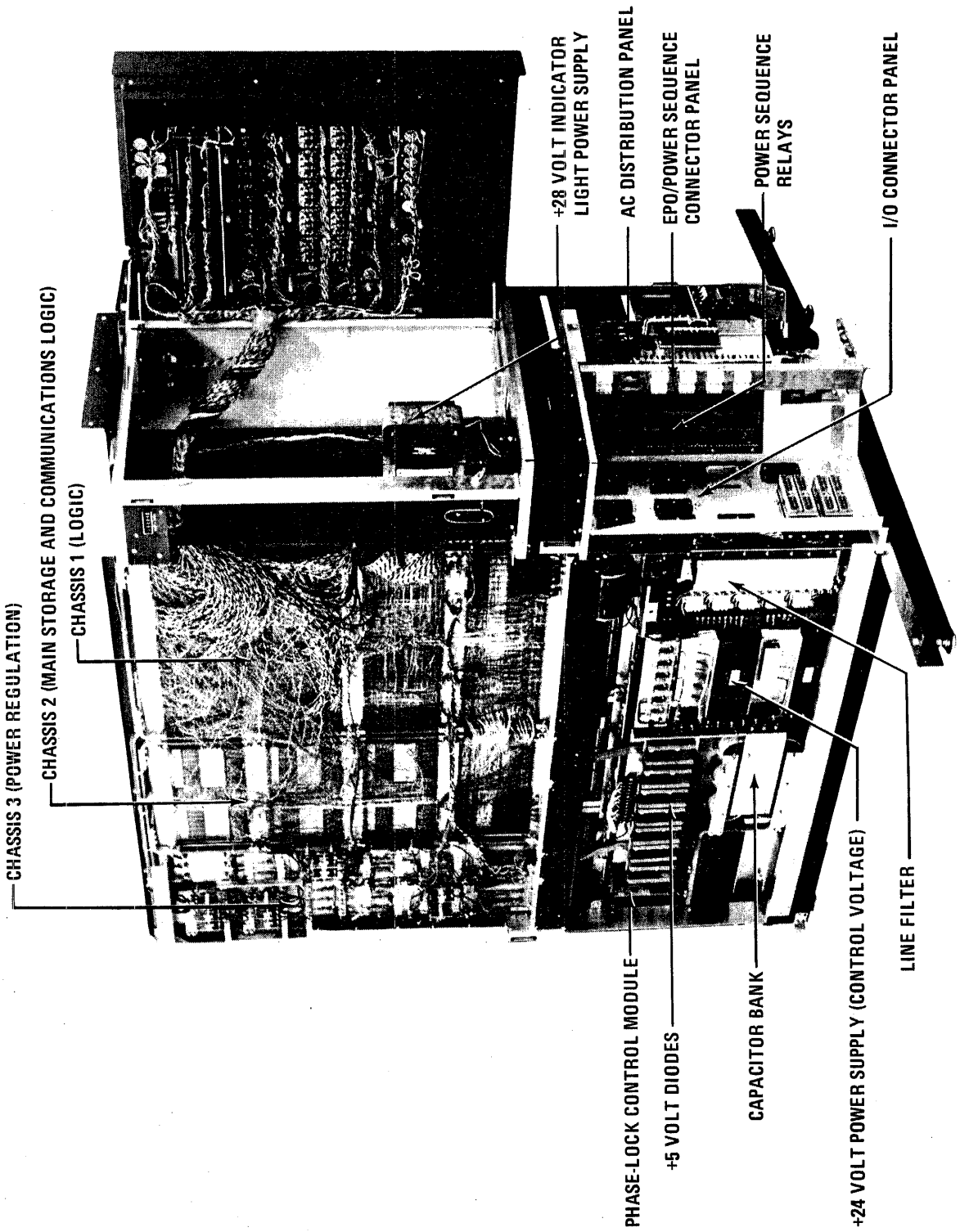
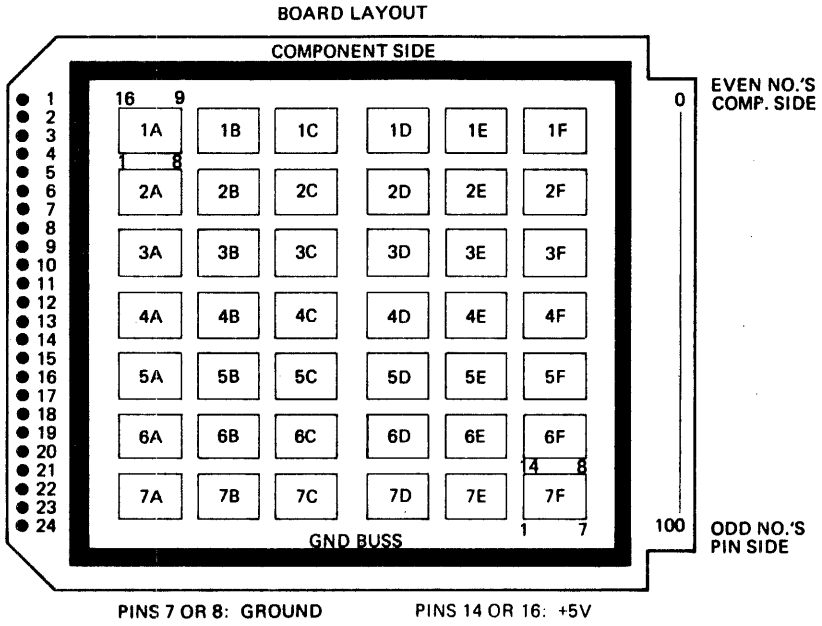
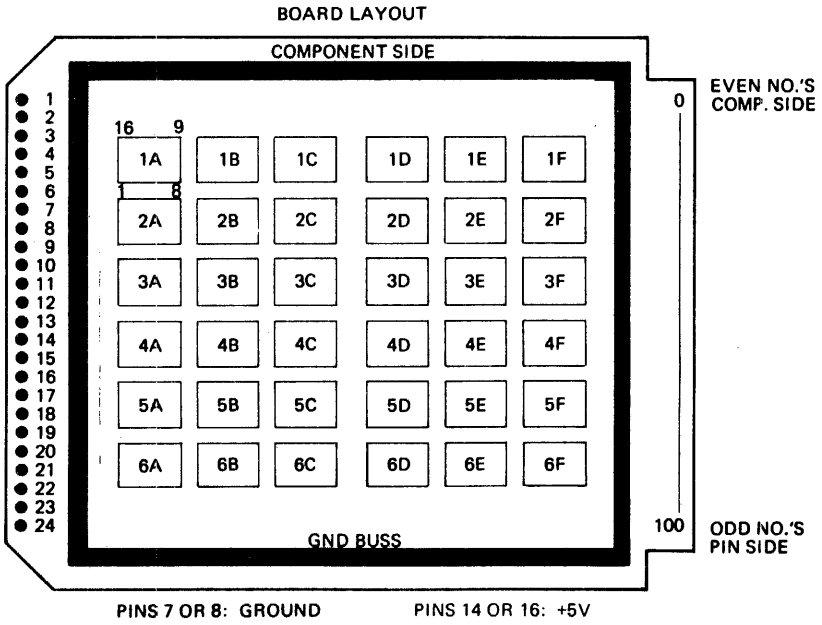


Figure 4-1. Component Locations, Processing Unit



a. 6 x 7 IC Element Module



b. 6 x 6 IC Element Module

Figure 4-2. PC Module Layout

MICRO-INSTRUCTION FORMATS

Figure 4-3 illustrates the ten different formats used by the uI's, with a list of uI's using each format.

MACHINE-LANGUAGE INSTRUCTION REPERTOIRE

The MLI repertoire is contained in the MRX/OS Programmer's Reference Card. For added convenience, a cross-reference of MLI's from mnemonic identifier in alphabetical order to function code, and from function code in numerical order to mnemonic identifier, is listed in Tables 4-3 and 4-4, respectively.

CODE CHARTS

Character assignments for both ASCII and EBCDIC transmission codes and Hollerith punching code information are tabulated in Tables 4-5 through 4-10. Tables 4-5 and 4-6 list ASCII code characters, coded both in MS bit position form and hexadecimal form. Tables 4-7 and 4-8 list the same information but for EBCDIC code characters. Table 4-9 lists character conversions between ASCII and EBCDDIC codes. Hollerith punching codes are listed in Table 4-10.

CONVERSION TABLES

Table 4-11 lists the decimal equivalents of powers of two from 0 to 35. Table 4-12 enables converting a number in hexadecimal form to equivalent decimal form. Tables 4-13 and 4-14 enable adding, subtracting, and multiplying single digits in hexadecimal form.

TOOLS AND TEST EQUIPMENT

A list of tools and test equipment required to maintain the Processing Unit is tabulated in Table 4-15.

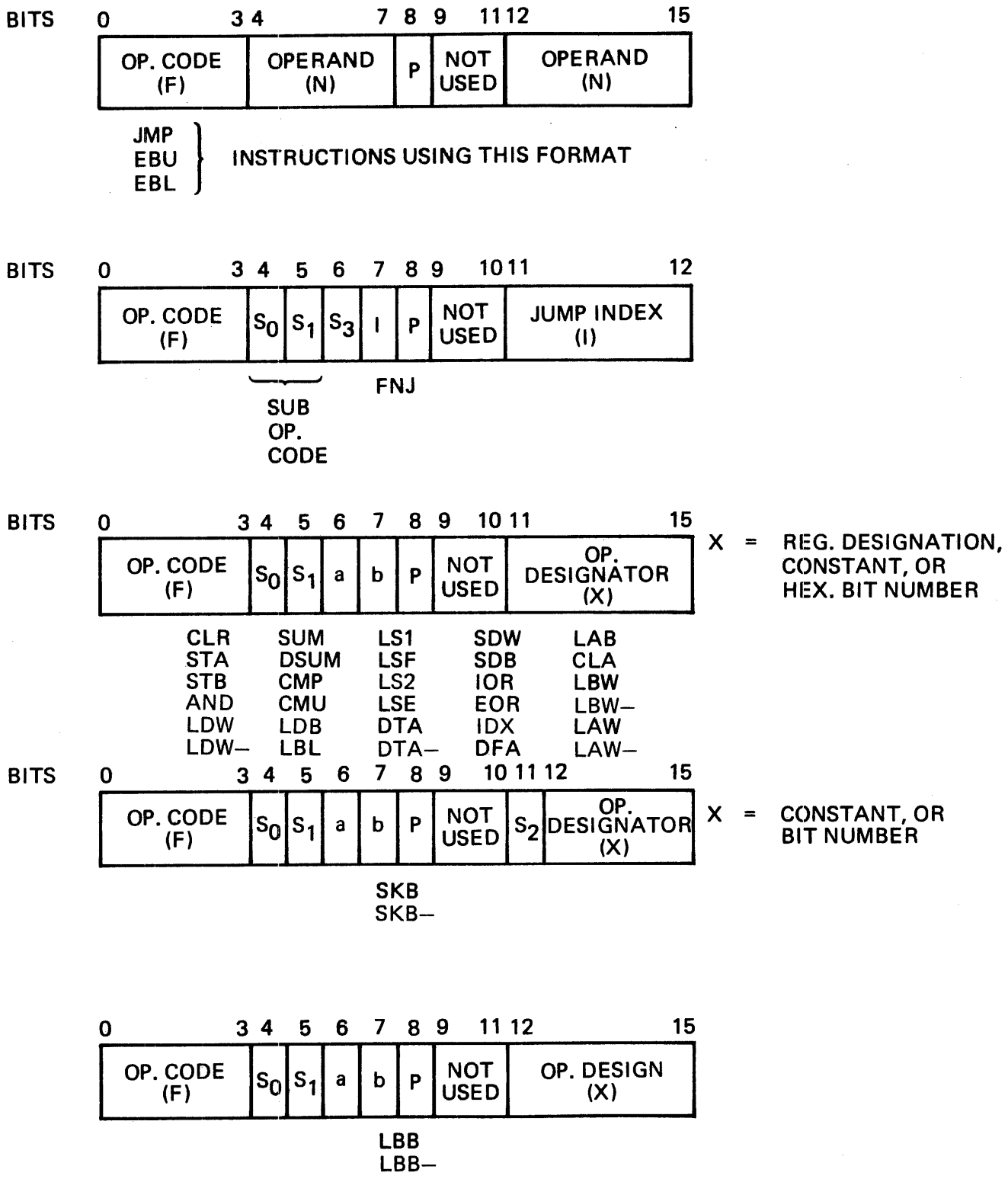


Figure 4-3. Micro-Instruction Formats (Page 1 of 2)

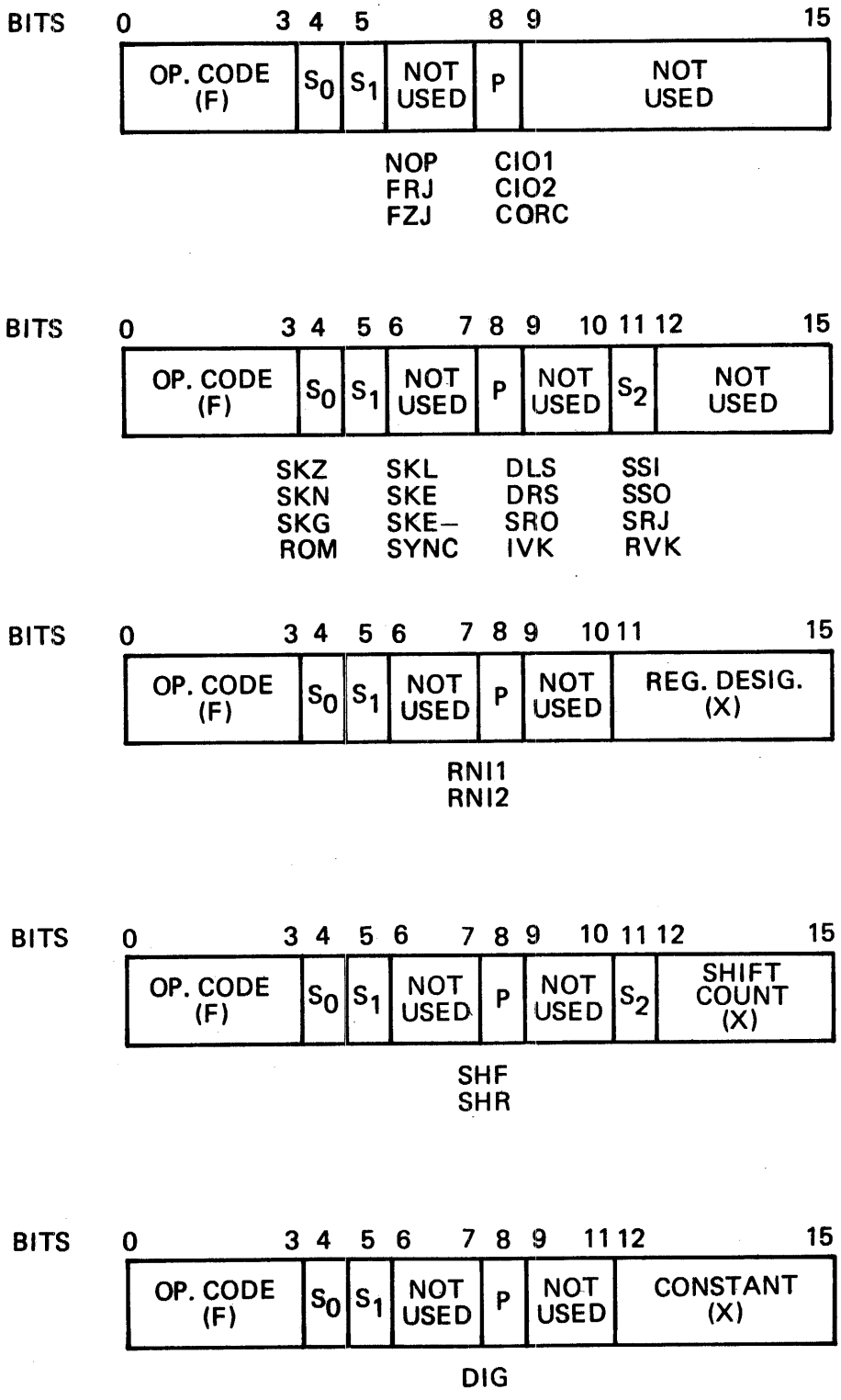


Figure 4-3. Micro-Instruction Formats (Page 2 of 2)

TABLE 4-2. FRJ DECODE BRANCH ADDRESSES

0-3 \ 4-7	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	20-29 R_1 R_2	20-29 R_1 (R_2)	20-29 (R_1) R_2	20-29 (R_1)(R_2)	2A R_1 R_2	2A R_1 (R_2)	2A (R_1) R_2	2A (R_1)(R_2)	2B R_1 R_2	2B R_1 (R_2)	2B (R_1) R_2	2B (R_1)(R_2)	2C-2F R_1 R_2	2C-2F R_1 (R_2)	2C-2F (R_1) R_2	2C-2F (R_1)(R_2)
1	30-39	30-39	30-39	30-39	3A	3A	3A	3A	3B	3B	3B	3B	3C-3F	3C-3F	3C-3F	3C-3F
2	A0-A9	A0-A9	A0-A9	A0-A9	AA	AA	AA	AA	AB	AB	AB	AB	AC-AF	AC-AF	AC-AF	AC-AF
3	B0-B9	B0-B9	B0-B9	B0-B9	BA	BA	BA	BA	BB	BB	BB	BB	BC-BF	BC-BF	BC-BF	BC-BF
4	60-63	60-63	60-63	60-63	64-67	64-67	64-67	64-67	68-6B	68-6B	68-6B	68-6B	6C-6F	6C-6F	6C-6F	6C-6F
5	70-73	70-73	70-73	70-73	74-77	74-77	74-77	74-77	78-7B	78-7B	78-7B	78-7B	7C-7F	7C-7F	7C-7F	7C-7F
6	00-03	04-07	08-0B	0C-0F	10-13	14-17	18-1B	1C-1F	40-43	44-47	48-4B	4C-4F	50-53	54-57	58-5B	5C-5F
7	80-83	84-87	88-8B	8C-8F	90-93	94-97	98-9B	9C-9F	C0-C3	C4-C7	C8-CB	CC-CF	D0-D3	D4-D7	D8-DB	DC-DF
8	E0	E0	E0	E0	E1	E1	E1	E1	E2	E2	E2	E2	E3	E3	E3	E3
9	E4	E4	E4	E4	E5	E5	E5	E5	E6	E6	E6	E6	E7	E7	E7	E7
A	E8	E8	E8	E8	E9	E9	E9	E9	EA	EA	EA	EA	EB	EB	EB	EB
B	EC	EC	EC	EC	ED	ED	ED	ED	EE	EE	EE	EE	EF	EF	EF	EF
C	F0	F0	F0	F0	F1	F1	F1	F1	F2	F2	F2	F2	F3	F3	F3	F3
D	F4	F4	F4	F4	F5	F5	F5	F5	F6	F6	F6	F6	F7	F7	F7	F7
E	F8	F8	F8	F8	F9	F9	F9	F9	FA	FA	FA	FA	FB	FB	FB	FB
F	FC	FC	FC	FC	FD	FD	FD	FD	FE	FE	FE	FE	FF	FF	FF	FF

*Value of A and B same as Row F
**Values of A and B do not apply

NOTE: (Boxheads represent hexadecimal address in a 256-word address table that points to the starting address, as modified by bits 2-6 of Sμ, for implementing the machine-language instruction indicated in the matrix.) Actual starting addresses in CS are listed in the CS printout.

TABLE 4-3. MACHINE LANGUAGE INSTRUCTION REPERTOIRE ARRANGED BY FUNCTION CODE (Page 1 of 3)

Function Code	Mnemonic	Class	Format	Description
10	RBA	CT	RR9	RESET BUSY/ACTIVE REGISTER
10	SBA	CT	RR9	SET BUSY/ACTIVE REGISTER
11	TST	CT	RR10	TEST AND SET TIE-BRAKER REGISTER
12	CTB	CT	RR10	CLEAR TIE-BRAKER REGISTER
13	SR	CT	RR8	SERVICE REQUEST
14	RCN	CT	RR11	RESET CONTROL REGISTER
14	SCN	CT	RR11	SET CONTROL REGISTER
15	RPM	CT	RR12	RESET PRIVILEGED MODE REGISTER
15	SPM	CT	RR12	SET PRIVILEDGED MODE REGISTER
20	MOVR	DT	RR1	MOVE REGISTER - REGISTER
21	CMPR	CP	RR1	COMPARE REGISTER - REGISTER
22	ADDR	AR	RR1	ADD REGISTER - REGISTER
23	SUBR	AR	RR1	SUBTRACT REGISTER - REGISTER
24	INVR	DT	RR1	INVERSE MOVE REGISTER - REGISTER
25	ANDR	BO	RR1	LOGICAL PRODUCT REGISTER - REGISTER
26	EORR	BO	RR1	EXCLUSIVE OR REGISTER - REGISTER
27	IORR	BO	RR1	INCLUSIVE OR REGISTER - REGISTER
28	MPYR	AR	RR1	MULTIPLY REGISTER - REGISTER
29	DIVR	AR	RR1	DIVIDE REGISTER - REGISTER
2A	CSTR	DT	RR16	CONDITION REGISTER STORE
2B	CLDR	DT	RR5	CONDITION REGISTER LOAD
2C	LLSR	SH	RR4	LOGICAL LEFT SINGLE SHIFT-BY-REGISTER
2D	LRSR	SH	RR4	LOGICAL RIGHT SINGLE SHIFT-BY-REGISTER
2E	RLSR	SH	RR4	ROTATING LEFT SINGLE SHIFT-BY-REGISTER
2F	ARSR	SH	RR4	ARITHMETIC RIGHT SINGLE SHIFT-BY-REGISTER
30	LODI	DT	RR2	LOAD IMMEDIATE
31	CMPI	CP	RR2	COMPARE IMMEDIATE
32	ADDI	AR	RR2	ADD IMMEDIATE
33	SUBI	AR	RR2	SUBTRACT IMMEDIATE
34	INVI	DT	RR2	INVERSE MOVE IMMEDIATE
35	ANDI	BO	RR2	LOGICAL PRODUCT IMMEDIATE
36	EORI	BO	RR2	EXCLUSIVE OR IMMEDIATE
37	IORI	BO	RR2	INCLUSIVE OR IMMEDIATE
38	MPYI	AR	RR2	MULTIPLY IMMEDIATE
39	DIVI	AR	RR2	DIVIDE IMMEDIATE
3A	PSTR	DT	RR16	PROGRAM ADDRESS STORE
3B	SHFK	SH	XX2	SHIFT PACKED DECIMAL
3C	LLDR	SH	RR4	LOGICAL LEFT DOUBLE SHIFT-BY-REGISTER
3D	LRDR	SH	RR4	LOGICAL RIGHT DOUBLE SHIFT-BY-REGISTER
3E	RLDR	SH	RR4	ROTATING LEFT DOUBLE SHIFT-BY-REGISTER
3F	ARDR	SH	RR4	ARITHMETIC RIGHT DOUBLE SHIFT-BY-REGISTER
40	SRZF	SK	RR3	SKIP IF REGISTER IS ZERO - FORWARD
41	SRZB	SK	RR3	SKIP IF REGISTER IS ZERO - BACKWARD
42	SRNF	SK	RR3	SKIP IF REGISTER NOT ZERO - FORWARD
43	SRNB	SK	RR3	SKIP IF REGISTER NOT ZERO - BACKWARD
44	SRPF	SK	RR3	SKIP IF REGISTER IS PLUS - FORWARD
45	SRPB	SK	RR3	SKIP IF REGISTER IS PLUS - BACKWARD
46	SRMF	SK	RR3	SKIP IF REGISTER IS MINUS - FORWARD
47	SRMB	SK	RR3	SKIP IF REGISTER IS MINUS - BACKWARD
48	SCTF	SK	RR7	SKIP ON CONDITION REGISTER TRUE - FORWARD
49	SCFF	SK	RR7	SKIP ON CONDITION REGISTER FALSE - FORWARD
4A	SCTB	SK	RR7	SKIP ON CONDITION REGISTER TRUE - BACKWARD
4B	SCFB	SK	RR7	SKIP ON CONDITION REGISTER FALSE - BACKWARD
4C	LLSI	SH	RR3	LOGICAL LEFT SINGLE SHIFT IMMEDIATE
4D	LRSI	SH	RR3	LOGICAL RIGHT SINGLE IMMEDIATE
4E	RLSI	SH	RR3	ROTATING LEFT SINGLE SHIFT IMMEDIATE
4F	ARSI	SH	RR3	ARITHMETIC RIGHT SINGLE SHIFT IMMEDIATE
50	ZADK	AR	SS1	ZERO AND ADD DECIMAL
51	CMPK	CP	SS1	COMPARE PACKED DECIMAL
52	ADDK	AR	SS1	ADD PACKED DECIMAL
53	SUBK	AR	SS1	SUBTRACT PACKED DECIMAL
54	MOVX	DT	SS1	MOVE CHARACTERS
55	CMPX	CP	SS1	COMPARE CHARACTERS
56	TRNX	DC	SS2	TRANSLATE
57	EDTX	DC	SS1	PACKED DECIMAL/ALPHA EDIT
58	PAKX	DC	SS1	PACK
59	UNPX	DC	SS1	UNPACK
5A	MOVL	DT	SS3	MOVE LONG
5C	LLDI	SH	RR3	LOGICAL LEFT DOUBLE SHIFT IMMEDIATE
5D	LRDI	SH	RR3	LOGICAL RIGHT DOUBLE SHIFT IMMEDIATE
5E	RLDI	SH	RR3	ROTATING LEFT DOUBLE SHIFT IMMEDIATE
5F	ARDI	SH	RR3	ARITHMETIC RIGHT DOUBLE SHIFT IMMEDIATE

TABLE 4-3. MACHINE LANGUAGE INSTRUCTION REPERTOIRE ARRANGED BY FUNCTION CODE (Page 2 of 3)

Function Code	Mnemonic	Class	Format	Description
60	MOVM	DT	XX1	MEMORY - MEMORY
61	CMPM	CP	XX1	COMPARE MEMORY - MEMORY
62	ADDM	AR	XX1	ADD MEMORY - MEMORY
63	SUBM	AR	XX1	SUBTRACT MEMORY - MEMORY
64	INVM	DT	XX1	INVERSE MOVE MEMORY - MEMORY
65	ANDM	BO	XX1	LOGICAL PRODUCT MEMORY - MEMORY
66	EORM	BO	XX1	EXCLUSIVE OR MEMORY - MEMORY
67	IORM	BO	XX1	INCLUSIVE OR MEMORY - MEMORY
68	MPYM	AR	XX1	MULTIPLY MEMORY - MEMORY
69	DIVM	AR	XX1	DIVIDE MEMORY - MEMORY
6A	MOVB	DT	XX1	MOVE BYTE
6B	DBYM	CP	XX1	COMPARE BYTE MEMORY - MEMORY
6C	TONR	BT	RR1	TEST FOR ON-BIT
6D	RONR	BT	RR1	REVERSE ON-BIT
6E	TOFR	BT	RR1	TEST FOR OFF-BIT
6F	ROFR	BT	RR1	REVERSE OFF-BIT
70	LODT	DT	RX1	LOAD TWO WORD
71	CMPT	CP	RX1	COMPARE TWO-WORD
72	ADDT	AR	RX1	ADD TWO-WORD
73	SUBT	AR	RX1	SUBTRACT TWO-WORD
A0	LOD	DT	RX1	LOAD MEMORY - REGISTER
A1	CMP	CP	RX1	COMPARE MEMORY - REGISTER
A2	ADD	AR	RX1	ADD MEMORY - REGISTER
A3	SUB	AR	RX1	SUBTRACT MEMORY - REGISTER
A4	INV	DT	RX1	INVERSE MOVE MEMORY - REGISTER
A5	AND	BO	RX1	LOGICAL PRODUCT MEMORY - REGISTER
A6	EOR	BO	RX1	EXCLUSIVE OR MEMORY - REGISTER
A7	IOR	BO	RX1	INCLUSIVE OR MEMORY - REGISTER
A8	MPY	AR	RX1	MULTIPLY MEMORY - REGISTER
A9	DIV	AR	RX1	DIVIDE MEMORY - REGISTER
AA	CVB	DC	RX4	CONVERT TO BINARY
AA	CVBT	DC	RX4	CONVERT TO BINARY-TWO WORD
AB	CVD	DC	RX4	CONVERT TO DECIMAL
AB	CVDT	DC	RX4	CONVERT TO DECIMAL-TWO WORD
B0	LODD	DT	RX2	LOAD DIRECT
B1	CMPD	CP	RX2	COMPARE DIRECT
B2	ADDD	AR	RX2	ADD DIRECT
B3	SUBD	AR	RX2	SUBTRACT DIRECT
B4	INVD	DT	RX2	INVERSE MOVE DIRECT
B5	ANDD	BO	RX2	LOGICAL PRODUCT DIRECT
B6	EORD	BO	RX2	EXCLUSIVE OR DIRECT
B7	IORD	BO	RX2	INCLUSIVE OR DIRECT
B8	MPYD	AR	RX2	MULTIPLY DIRECT
B9	DIVD	AR	RX2	DIVIDE DIRECT
BA	SF	SK	RR6	SKIP UNCONDITIONAL - FORWARD
BB	SB	SK	RR6	SKIP UNCONDITIONAL - BACKWARD
BC	SBIT	BT	RX5	SET BIT
BD	RBIT	BT	RX5	RESET BIT
BE	TBIT	BT	RX5	TEST BIT
BF	IBIT	BT	RX5	INVERT BIT
E0	BRZ	BR	RX1	BRANCH IF REGISTER IS ZERO
E1	BRN	BR	RX1	BRANCH IF REGISTER IS NOT ZERO
E2	BOF	BR	RX3	BRANCH IF BIT OFF
E3	BON	BR	RX3	BRANCH IF BIT ON
E4	BA1	BR	RX1	BRANCH ADD 1
E5	BA2	BR	RX1	BRANCH ADD 2
E6	BS1	BR	RX1	BRANCH SUBTRACT 1
E7	BS2	BR	RX1	BRANCH SUBTRACT 2
E8	BCT	BR	RX3	BRANCH ON CONDITION REGISTER TRUE
E9	BCF	BR	RX3	BRANCH ON CONDITION REGISTER FALSE
EA	BSR	BR	RX1	BRANCH AND SAVE RETURN
EB	BR	BR	RR5	BRANCH TO ADDRESS IN REGISTER
EC	BCH	BR	RX6	BRANCH - PRE-INDEXING
ED	B	BR	RX6	BRANCH - POST INDEXING
EE	NOP		RX1	NO OPERATION
EF	BCM	CT	RR13	BRANCH TO CONTROL MEMORY
F0	RDX	CT	RR14	READ EXTENDED REGISTER
F0	WRX	CT	RR14	WRITE EXTENDED REGISTER
F1	SIO	IO	RR4	SYSTEM I/O
F2	DIO	IO	RR4	DISK I/O
F3	RDC	IO	RR15	COMMUNICATIONS I/O
F4	WRC	IO	RR13	COMMUNICATIONS OUTPUT COMMAND
F5	INP	IO	RR2	INPUT FROM I/O REGISTER
F6	OUT	IO	RR2	OUTPUT TO I/O REGISTER
F7	LODB	DT	RX1	LOAD BYTE
F8	STOB	DT	RX1	STORE BYTE
F9	CBY	CP	RX1	COMPARE BYTE
FA	STO	DT	RX1	STORE REGISTER - MEMORY

TABLE 4-3. MACHINE LANGUAGE INSTRUCTION REPERTOIRE ARRANGED BY FUNCTION CODE (Page 3 of 3)

Function Code	Mnemonic	Class	Format	Description
FB	STOT	DT	RX1	STORE TWO-WORD
FD	RRO	CT	RX7	READ REGISTER OPTION
FD	WRO	CT	RX7	WRITE REGISTER OPTION
FE	RAR	CT	RX7	READ ANY REGISTER
FE	WAR	CT	RX7	WRITE ANY REGISTER
FF	RSAR	CT	RX7	RESTORE ALL REGISTERS
FF	SAR	CT	RX7	SAVE ALL REGISTERS

TABLE 4-4. MACHINE LANGUAGE INSTRUCTION REPERTOIRE ARRANGED BY MNEMONIC (Page 1 of 3)

Function Code	Mnemonic	Class	Format	Description
A2	ADD	AR	RX1	ADD MEMORY - REGISTER
B2	ADDD	AR	RX2	ADD DIRECT
32	ADDI	AR	RR2	ADD IMMEDIATE
52	ADDK	AR	SS1	ADD PACKED DECIMAL
62	ADDM	AR	XX1	ADD MEMORY - MEMORY
22	ADDR	AR	RR1	ADD REGISTER - REGISTER
72	ADDT	AR	RX1	ADD TWO-WORD
A5	AND	BO	RX1	LOGICAL PRODUCT MEMORY - REGISTER
B5	ANDD	BO	RX2	LOGICAL PRODUCT DIRECT
35	ANDI	BO	RR2	LOGICAL PRODUCT IMMEDIATE
25	ANDR	BO	RR1	LOGICAL PRODUCT REGISTER - REGISTER
5F	ARDI	SH	RR3	ARITHMETIC RIGHT DOUBLE SHIFT - IMMEDIATE
65	ANDM	BO	XX1	LOGICAL PRODUCT MEMORY - MEMORY
3F	ARDR	SH	RR4	ARITHMETIC RIGHT DOUBLE SHIFT-BY-REGISTER
4F	ARSI	SH	RR3	ARITHMETIC RIGHT SINGLE SHIFT - IMMEDIATE
2F	ARSR	SH	RR4	ARITHMETIC RIGHT SINGLE SHIFT-BY-REGISTER
ED	B	BR	RX6	BRANCH-POST INDEXING
E4	BA1	BR	RX1	BRANCH ADD 1
E5	BA2	BR	RX1	BRANCH ADD 2
E9	BCF	BR	RX3	BRANCH ON CONDITION REGISTER FALSE
EC	BCH	BR	RX6	BRANCH - PRE-INDEXING
EF	BCM	CT	RR13	BRANCH TO CONTROL MEMORY
E8	BCT	BR	RX3	BRANCH ON CONDITION REGISTER TRUE
E2	BOF	BR	RX3	BRANCH IF BIT OFF
E3	BON	BR	RX3	BRANCH IF BIT ON
EB	BR	BR	RR5	BRANCH TO ADDRESS IN REGISTER
E1	BRN	BR	RX1	BRANCH IF REGISTER IS NOT ZERO
E0	BRZ	BR	RX1	BRANCH IF REGISTER IS ZERO
E6	BS1	BR	RX1	BRANCH SUBTRACT 1
E7	BS2	BR	RX1	BRANCH SUBTRACT 2
EA	BSR	BR	RX1	BRANCH AND SAVE RETURN
F9	CBY	CP	RX1	COMPARE BYTE
6B	CBYM	CP	XX1	COMPARE BYTE MEMORY - MEMORY
2B	CLDR	DT	RR5	CONDITION REGISTER LOAD
A1	CMP	CP	RX1	COMPARE MEMORY - REGISTER
B1	CMPD	CP	RX2	COMPARE DIRECT
31	CMPI	CP	RR2	COMPARE IMMEDIATE
51	CMPK	CP	SS1	COMPARE PACKED DECIMAL
61	CMPM	CP	XX1	COMPARE MEMORY - MEMORY
21	CMPR	CP	RR1	COMPARE REGISTER - REGISTER
71	CMPT	CP	RX1	COMPARE TWO-WORD
55	CMPX	CP	SS1	COMPARE CHARACTERS
2A	CSTR	DT	RR16	CONDITION REGISTER STORE
12	C1B	CT	RR10	CLEAR TIE-BRAKER REGISTER
AA	CVB	DC	RX4	CONVERT TO BINARY
AA	CVBT	DC	RX4	CONVERT TO BINARY-TWO WORD
AB	CVD	DC	RX4	CONVERT TO DECIMAL
AB	CVDT	DC	RX4	CONVERT TO DECIMAL-TWO WORD
F2	DIO	IO	RR4	DISK I/O
A9	DIV	AR	RX1	DIVIDE MEMORY - REGISTER
B9	DIVD	AR	RX2	DIVIDE DIRECT
39	DIVI	AR	RR2	DIVIDE IMMEDIATE
69	DIVM	AR	XX1	DIVIDE MEMORY - MEMORY
29	DIVR	AR	RR1	DIVIDE REGISTER - REGISTER
57	EDTX	DC	SS1	PACKED DECIMAL/ALPHA EDIT
A6	EOR	BO	RX1	EXCLUSIVE OR MEMORY - REGISTER
B6	EORD	BO	RX2	EXCLUSIVE OR DIRECT
36	EORI	BO	RR2	EXCLUSIVE OR IMMEDIATE
66	EORM	BO	XX1	EXCLUSIVE OR MEMORY - MEMORY
26	EORR	BO	RR1	EXCLUSIVE OR REGISTER - REGISTER
BF	IBIT	BT	RX5	INVERT BIT
F5	INP	IO	RR2	INPUT FROM I/O REGISTER
A4	INV	DT	RX1	INVERSE MOVE MEMORY - REGISTER
B4	INVD	DT	RX2	INVERSE MOVE DIRECT
34	INVI	DT	RR2	INVERSE MOVE IMMEDIATE
64	INVM	DT	XX1	INVERSE MOVE MEMORY - MEMORY
24	INVR	DT	RR1	INVERSE MOVE REGISTER - REGISTER
A7	IOR	BO	RX1	INCLUSIVE OR MEMORY - REGISTER
B7	IORD	BO	RX2	INCLUSIVE OR DIRECT
37	IORI	BO	RR2	INCLUSIVE OR IMMEDIATE
67	IORM	BO	XX1	INCLUSIVE OR MEMORY - MEMORY
27	IORR	BO	RR1	INCLUSIVE OR REGISTER - REGISTER

TABLE 4-4. MACHINE LANGUAGE INSTRUCTION REPERTOIRE ARRANGED BY MNEMONIC (Page 2 of 3)

Function Code	Mnemonic	Class	Format	Description
	LDA	DT	RX1	LOAD ADDRESS
5C	LLDI	SH	RR3	LOGICAL LEFT DOUBLE SHIFT IMMEDIATE
3C	LLDR	SH	RR4	LOGICAL LEFT DOUBLE SHIFT-BY-REGISTER
4C	LLSI	SH	RR3	LOGICAL LEFT SINGLE SHIFT IMMEDIATE
2C	LLSR	SH	RR4	LOGICAL LEFT SINGLE SHIFT-BY-REGISTER
A0	LOD	DT	RX1	LOAD MEMORY - REGISTER
F7	LODB	DT	RX1	LOAD BYTE
30	LODI	DT	RR2	LOAD IMMEDIATE
B0	LODD	DT	RX2	LOAD DIRECT
70	LODT	DT	RX1	LOAD TWO WORD
5D	LRDI	SH	RR3	LOGICAL RIGHT DOUBLE SHIFT IMMEDIATE
3D	LRDR	SH	RR4	LOGICAL RIGHT DOUBLE SHIFT-BY-REGISTER
2D	LRSR	SH	RR4	LOGICAL RIGHT SINGLE SHIFT-BY-REGISTER
4D	LRSI	SH	RR3	LOGICAL RIGHT SINGLE SHIFT IMMEDIATE
	LST	DT	RX1	LOAD SEGMENT TAG
	MOVA	DT	RR1	MOVE ADDRESS
6A	MOVB	DT	XX1	MOVE BYTE
5A	MOVL	DT	SS3	MOVE LONG
60	MOVM	DT	XX1	MEMORY - MEMORY
20	MOVR	DT	RR1	MOVE REGISTER - REGISTER
54	MOVX	DT	SS1	MOVE CHARACTERS
A8	MPY	AR	RX1	MULTIPLY MEMORY - REGISTER
B8	MPYD	AR	RX2	MULTIPLY DIRECT
38	MPYI	AR	RR2	MULTIPLY IMMEDIATE
68	MPYM	AR	XX1	MULTIPLY MEMORY - MEMORY
28	MPYR	AR	RR1	MULTIPLY REGISTER - REGISTER
	MSTR	DT	RR1	MOVE SEGMENT TAG
EE	NOP		RX1	NO OPERATION
F6	OUT	IO	RR2	OUTPUT TO I/O REGISTER
58	PAKX	DC	SS1	PACK
3A	PSTR	DT	RR16	PROGRAM ADDRESS STORE
	RAMR	CT	RR9	RESET ADDRESS-MODE REGISTER
FE	RAR	CT	RX7	READ ANY REGISTER
10	RBA	CT	RR9	RESET BUSY/ACTIVE REGISTER
BD	RBIT	BT	RX5	RESET BIT
14	RCN	CT	RR11	RESET CONTROL REGISTER
F3	RDC	IO	RR15	COMMUNICATIONS I/O
F0	RDX	CT	RR14	READ EXTENDED REGISTER
5E	RLDI	SH	RR3	ROTATING LEFT DOUBLE SHIFT IMMEDIATE
3E	RLDR	SH	RR4	ROTATING LEFT DOUBLE SHIFT-BY-REGISTER
4E	RLSI	SH	RR3	ROTATING LEFT SINGLE SHIFT IMMEDIATE
2E	RLSR	SH	RR4	ROTATING LEFT SINGLE SHIFT-BY-REGISTER
6F	ROFR	BT	RR1	REVERSE OFF-BIT
6D	RONR	BT	RR1	REVERSE ON-BIT
15	RPM	CT	RR12	RESET PRIVILEDGED MODE REGISTER
	RPS	CT	RX7	RESTORE PROCESSOR STATE
FF	RSAR	CT	RX7	RESTORE ALL REGISTERS
	SAMR	CT	RR9	SET ADDRESS-MODE REGISTER
FF	SAR	CT	RX7	SAVE ALL REGISTERS
BB	SB	SK	RR6	SKIP UNCONDITIONAL - BACKWARD
10	SBA	CT	RR9	SET BUSY/ACTIVE REGISTER
BC	SBIT	BT	RX5	SET BIT
4B	SCFB	SK	RR7	SKIP ON CONDITION REGISTER FALSE - BACKWARD
49	SCFF	SK	RR7	SKIP ON CONDITION REGISTER FALSE - FORWARD
14	SCN	CT	RR11	SET CONTROL REGISTER
4A	SCTB	SK	RR7	SKIP ON CONDITION REGISTER TRUE - BACKWARD
48	SCTF	SK	RR7	SKIP ON CONDITION REGISTER TRUE - FORWARD
BA	SF	SK	RR6	SKIP UNCONDITIONAL - FORWARD
3B	SHFK	SH	XX2	SHIFT PACKED DECIMAL
F1	SIO	IO	RR4	SYSTEM I/O
15	SPM	CT	RR12	SET PRIVILEDGED MODE REGISTER
	SPS	CT	RX7	SAVE PROCESSOR STATE
	SPSR	DT	RR16	STORE PROGRAM SEGMENT TAG
13	SR	CT	RR8	SERVICE REQUEST
47	SRMB	SK	RR3	SKIP IF REGISTER IS MINUS - BACKWARD
46	SRMF	SK	RR3	SKIP IF REGISTER IS MINUS - FORWARD
43	SRNB	SK	RR3	SKIP IF REGISTER NOT ZERO - BACKWARD
42	SRNF	SK	RR3	SKIP IF REGISTER NOT ZERO - FORWARD
45	SRPB	SK	RR3	SKIP IF REGISTER IS PLUS - BACKWARD

TABLE 4-4. MACHINE LANGUAGE INSTRUCTION REPERTOIRE ARRANGED BY MNEMONIC (Page 3 of 3)

Function Code	Mnemonic	Class	Format	Description
44	SRPF	SK	RR3	SKIP IF REGISTER IS PLUS - FORWARD
41	SRZB	SK	RR3	SKIP IF REGISTER IS ZERO - BACKWARD
40	SRZF	SK	RR3	SKIP IF REGISTER IS ZERO - FORWARD
	SST	DT	RX1	STORE SEGMENT TAG
	STA	DT	RX1	STORE ADDRESS
FA	STO	DT	RX1	STORE REGISTER - MEMORY
F8	STOB	DT	RX1	STORE BYTE
FB	STOT	DT	RX1	STORE TWO-WORD
A3	SUB	AR	RX1	SUBTRACT MEMORY - REGISTER
B3	SUBD	AR	RX2	SUBTRACT DIRECT
33	SUBI	AR	RR2	SUBTRACT IMMEDIATE
53	SUBK	AR	SS1	SUBTRACT PACKED DECIMAL
63	SUBM	AR	XX1	SUBTRACT MEMORY - MEMORY
23	SUBR	AR	RR1	SUBTRACT REGISTER - REGISTER
73	SUBT	AR	RX1	SUBTRACT TWO-WORD
BE	TBIT	BT	RX5	TEST BIT
6E	TOFR	BT	RR1	TEST FOR OFF-BIT
6C	TONR	BT	RR1	TEST FOR ON-BIT
56	TRNX	DC	SS2	TRANSLATE
11	TST	CT	RR10	TEST AND SET TIE-BRAKER - REGISTER
59	UNPX	DC	SS1	UNPACK
FE	WAR	CT	RX7	WRITE ANY REGISTER
F4	WRC	IO	RR13	COMMUNICATIONS OUTPUT COMMAND
F0	WRX	CT	RR14	WRITE EXTENDED REGISTER
50	ZADK	AR	SS1	ZERO AND ADD DECIMAL

TABLE 4-5. ASCII CHARACTER TO MS BIT POSITION

Bit Positions 4, 5, 6, 7		Main Storage Bit Positions 0, 1, 2, 3															
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NUL	DLE	SP	0	@	P	`	p								
0001	1	SOH	DC1	!	1	A	Q	a	q								
0010	2	STX	DC2	"	2	B	R	b	r								
0011	3	ETX	DC3	#	3	C	S	c	s								
0100	4	EOT	DC4	$	4	D	T	d	t								
0101	5	ENQ	NAK	%	5	E	U	e	u								
0110	6	ACK	SYN	&	6	F	V	f	v								
0111	7	BEL	ETB	'	7	G	W	g	w								
1000	8	BS	CAN	(	8	H	X	h	x								
1001	9	HT	EM	)	9	I	Y	i	y								
1010	A	LF	SUB	*	:	J	Z	j	z								
1011	B	VT	ESC	+	;	K	[	k	{								
1100	C	FF	FS	,	<	L	\	l	¦								
1101	D	CR	GS	-	=	M	]	m	}								
1110	E	SO	RS	.	>	N	¬	n	~								
1111	F	SI	US	/	?	O	_	o	DEL								

TABLE 4-6. ASCII CHARACTER TO HEX EQUIVALENT

Character	Hex
A	41
B	42
C	43
D	44
E	45
F	46
G	47
H	48
I	49
J	4A
K	4B
L	4C
M	4D
N	4E
O	4F
P	50
Q	51
R	52
S	53
T	54
U	55
V	56
X	58
Y	59
Z	5A
a	61
b	62
c	63
d	64
e	65
f	66
g	67
h	68
i	69
j	6A
k	6B
l	6C
m	6D
n	6E
o	6F
p	70
q	71
r	72
s	73
t	74
u	75
v	76
w	77
x	78
y	79
z	7A
0	30
1	31
2	32
3	33

Character	Hex
4	34
5	35
6	36
7	37
8	38
9	39
Space	20
!	21
"	22
#	23
$	24
%	25
&	26
'	27
(	28
)	29
*	2A
+	2B
,	2C
-	2D
.	2E
/	2F
:	3A
;	3B
<	3C
=	3D
>	3E
?	3F
@	40
[	5B
\	5C
]	5D
↑	5E
←	5F
`	60
{	7B
|	7C
}	7D
~	7E
BEL	07
BS	08
CAN	18
CR	0D
DC1	11
DC2	12
DC3	13
DC4	14
DEL	7F
DLE	10
EM	19
ENQ	05
EOT	04
ESC	1B
ETB	17
ETX	03

Character	Hex
FF	0C
FS	1C
GS	1D
HT	09
LF	0A
NAK	15
NUL	00
RS	1E
SI	0F
SO	0E
SOH	01
STX	02
SUB	1A
SYN	16
US	1F
VT	0B

TABLE 4-7. EBCDIC CHARACTER TO MS BIT POSITION

		Main Storage Bit Positions 0, 1, 2, 3															
Bit Positions 4, 5, 6, 7		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
	Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NUL	DLE	DS		SP	&	-						{	}	\	0
0001	1	SOH	DC1	SOS						a	j	~		A	J		1
0010	2	STX	DC2	FS	SYN					b	k	s		B	K	S	2
0011	3	ETX	DC3							c	l	t		C	L	T	3
0100	4	PF	RES	BYP	PN					d	m	u		D	M	U	4
0101	5	HT	NL	LF	RS					e	n	v		E	N	V	5
0110	6	LC	BS	EOB / ETB	UC					f	o	w		F	O	W	6
0111	7	DEL	IL	PRE / ESC	EOT					g	p	x		G	P	X	7
1000	8		CAN							h	q	y		H	Q	Y	8
1001	9	RLF	EM						\	i	r	z		I	R	Z	9
1010	A	SMM	CC	SM		¢	!	¦	:								
1011	B	VT				.	$	,	#								
1100	C	FF	IFS		DC4	<	*	%	@								
1101	D	CR	IGS	ENQ	NAK	(	)	_	'								
1110	E	SO	IRS	ACK		+	;	>	=								
1111	F	SI	IUS	BEL	SUB	¦	¬	?	"								

Duplicate Assignment

TABLE 4-8. EBCIDIC CHARACTER TO HEX EQUIVALENT

Character	Hex
A	C1
B	C2
C	C3
D	C4
E	C5
F	C6
G	C7
H	C8
I	C9
J	D1
K	D2
L	D3
M	D4
N	D5
O	D6
P	D7
Q	D8
R	D9
S	E2
T	E3
U	E4
V	E5
W	E6
X	E7
Y	E8
Z	E9
a	81
b	82
c	83
d	84
e	85
f	86
g	87
h	88
i	89
j	91
k	92
l	93
m	94
n	95
o	96
p	97
q	98
r	99
s	A2
t	A3
u	A4
v	A5
w	A6
x	A7
y	A8
z	A9
0	F0
1	F1
2	F3
3	F3
4	F4
5	F5
6	F6
7	F7
8	F8
9	F9
&	50
-	60
/	61
$	5B

Character	Hex
¢	4A
!	5A
:	7A
#	7B
,	6B
.	4B
<	4C
*	5C
%	6C
@	7C
(	4D
)	5D
_	7D
+	4E
;	5E
>	6E
=	7E
¬	4F
?	5F
"	6F
(	7F
)	C0
/	D0
~	E0
'	A1
¦	79
BEL	6A
BS	2F
BYP	16
CAN	24
CC	18
CR	1A
DC1	0D
DC2	11
DC3	12
DC4	13
DEL	3C
DLE	07
DS	10
EM	20
ENQ	19
*EOB	2D
EOT	26
*ESC	37
*ETB	27
ETX	26
FF	03
FS	0C
HT	22
IFS	05
IGS	1C
IL	1D
IRS	17
IUS	1E
LC	1F
LF	06
NAK	25
NL	3D
NUL	15
PF	00
PN	04
*PRE	34
RES	27
RLF	14
	09

Character	Hex
RS	35
SI	0F
SM	2A
SMM	0A
SO	0E
SOH	01
SOS	21
Space	40
STX	02
SUB	3F
SYN	32
UC	36
VT	08

*ETB and EOB have the same hex assignment. PRE and ESC have the same hex assignment.

TABLE 4-9. EBCIDIC/ASCII CHARACTER CONVERSIONS

Data Link Character	Code Chart Sequence	
	EBCDIC	USASCII
SYN	nc	nc
SOH	nc	nc
STX	nc	nc
ETB	EOB(ETB)	nc
ETX	nc	nc
EOT	nc	nc
ENQ	nc	nc
ACK 0	DLE '70'	DLE 0
ACK 1	DLE /	DLE 1
NAK	nc	nc
DLE	nc	nc
ITB	IUS	US
WACK	DLE ,	DLE ;
RVI	DLE @	DLE <
TTD	STX ENQ	STX ENQ

nc--no change
' '--Indicates the hexadecimal representation (no graphic assignment).

TABLE 4-10. HOLLERITH PUNCHING CODES (Page 1 of 3)

GRAPHIC	CARD CODE	
	EBCDIC	USASCII
•		
0 •	0	
•		0
•		
1 •	1	
•		1
•		
2 •	2	
•		2
•		
3 •	3	
•		3
•		
4 •	4	
•		4
•		
5 •	5	
•		5
•		
6 •	6	
•		6
•		
7 •	7	
•		7
•		
8 •	8	
•		8
•		
9 •	9	
•		9
•		
A •	12-1	
•		12-1
•		
B •	12-2	
•		12-2
•		
C •	12-3	
•		12-3
•		
D •	12-4	
•		12-4
•		
E •	12-5	
•		12-5
•		
F •	12-6	
•		12-6
•		
G •	12-7	
•		12-7
•		
H •	12-8	
•		12-8
•		
I •	12-9	
•		12-9
•		
J •	11-1	
•		11-1
•		
K •	11-2	
•		11-2
•		
L •	11-3	
•		11-3

GRAPHIC	CARD CODE	
	EBCDIC	USASCII
•		
M •	11-4	
•		11-4
•		
N •	11-5	
•		11-5
•		
O •	11-6	
•		11-6
•		
P •	11-7	
•		11-7
•		
Q •	11-8	
•		11-8
•		
R •	11-9	
•		11-9
•		
S •	0-2	
•		0-2
•		
T •	0-3	
•		0-3
•		
U •	0-4	
•		0-4
•		
V •	0-5	
•		0-5
•		
W •	0-6	
•		0-6
•		
X •	0-7	
•		0-7
•		
Y •	0-8	
•		0-8
•		
Z •	0-9	
•		0-9
a •	12-0-1	
•		12-0-1
b •	12-0-2	
•		12-0-2
c •	12-0-3	
•		12-0-3
d •	12-0-4	
•		12-0-4
e •	12-0-5	
•		12-0-5
f •	12-0-6	
•		12-0-6
g •	12-0-7	
•		12-0-7
h •	12-0-8	
•		12-0-8

GRAPHIC	CARD CODE	
	EBCDIC	USASCII
i •	12-0-9	
•		12-0-9
j •	12-11-1	
•		12-11-1
k •	12-11-2	
•		12-11-2
l •	12-11-3	
•		12-11-3
m •	12-11-4	
•		12-11-4
n •	12-11-5	
•		12-11-5
o •	12-11-6	
•		12-11-6
p •	12-11-7	
•		12-11-7
q •	12-11-8	
•		12-11-8
r •	12-11-9	
•		12-11-9
s •	11-0-2	
•		11-0-2
t •	11-0-3	
•		11-0-3
u •	11-0-4	
•		11-0-4
v •	11-0-5	
•		11-0-5
w •	11-0-6	
•		11-0-6
x •	11-0-7	
•		11-0-7
y •	11-0-8	
•		11-0-8
z •	11-0-9	
•		11-0-9
•		
. •	12-3-8	
•		12-3-8
•		
▨	▨	▨
•		
& •	12	
•		12
Space	BLANK	
		BLANK

• Dot indicates printable graphic

▨ Shaded area indicates that card code and translator are not available for that graphic

TABLE 4-10. HOLLERITH PUNCHING CODES (Page 2 of 3)

GRAPHIC	CARD CODE	
	EBCDIC	USASCII
•		
$ •	11-3-8	
•		11-3-8
•		
* •	11-4-8	
•		11-4-8
•		
- •	11	
•		11
•		
/ •	0-1	
•		0-1
•		
, •	0-3-8	
•		0-3-8
•		
% •	0-4-8	
•		0-4-8
•		
@ •	4-8	
•		4-8
•		
# •	3-8	
•		3-8
¢ •	12-2-8	
< •	12-4-8	
•		12-4-8
(•	12-5-8	
•		12-5-8
+ •	12-6-8	
•		12-6-8
| •	12-7-8	
•		12-7-8
¦		
		12-11
! •	11-2-8	
) •	11-5-8	
•		11-5-8
; •	11-6-8	
•		11-6-8
¬ •	11-7-8	
•		11-7-8
- •	0-5-8	
•		0-5-8
> •	0-6-8	
•		0-6-8
? •	0-7-8	
•		0-7-8
: •	2-8	
•		2-8

GRAPHIC	CARD CODE	
	EBCDIC	USASCII
' •	5-8	
•		5-8
= •	6-8	
•		6-8
" •	7-8	
•		7-8
[		
•		12-8-2
\		
•		0-8-2
]		
•		11-8-2
^		
		1-8
{		
		12-0
}		
		11-0
~		
		11-0-1
NUL	12-0-1-8-9	
		12-0-1-8-9
SOH	12-1-9	
		12-1-9
STX	12-2-9	
		12-2-9
ETX	12-3-9	
		12-3-9
PF	12-4-9	
HT	12-5-9	
		12-5-9
LC	12-6-9	
DEL	12-7-9	
		12-7-9
SMM	12-2-8-9	
VT	12-3-8-9	
		12-3-8-9
FF	12-4-8-9	
		12-4-8-9
CR	12-5-8-9	
		12-5-8-9

GRAPHIC	CARD CODE	
	EBCDIC	USASCII
SO	12-6-8-9	
		12-6-8-9
SI	12-7-8-9	
		12-7-8-9
DLE	12-11-1-8-9	
		12-11-1-8-9
DC1	11-1-9	
		11-1-9
DC2	11-2-9	
		11-2-9
DC3 (TMX)	11-3-9	
		11-3-9
RES	11-4-9	
NL	11-5-9	
BS	11-6-9	
		11-6-9
IL	11-7-9	
CAN	11-8-9	
		11-8-9
EM	11-1-8-9	
		11-1-8-9
CC	11-2-8-9	
IFS	11-4-8-9	
IGS	11-5-8-9	
RS	5-9	
		11-6-8-9
US		
		11-7-8-9
DS	11-0-1-8-9	
SOS	0-1-9	
FS	0-2-9	
		11-4-8-9
BYP	0-4-9	
LF	0-5-9	
		0-5-9

• Dot indicates printable graphic

Shaded area indicates that card code and translator are not available for that graphic

TABLE 4-10. HOLLERITH PUNCHING CODES (Page 3 of 3)

GRAPHIC	CARD CODE	
	EBCDIC	USASCII
ETB (EOB)	0-6-9	
		0-6-9
ESC (PRE)	0-7-9	
		0-7-9
SM	0-2-8-9	
ENQ	0-5-8-9	
		0-5-8-9
ACK	0-6-8-9	
		0-6-8-9
BEL	0-7-8-9	
		0-7-8-9
SYN	2-9	
		2-9
PN	4-9	
IRS	11-6-8-9	
UC	6-9	
EOT	7-9	
		7-9
DC4	4-8-9	
		4-8-9
NAK	5-8-9	
		5-8-9
SUB	7-8-9	
		7-8-9
GS		
		11-5-8-9
IUS	11-7-8-9	

• Dot indicates printable graphic

Shaded area indicates that card code and translator are not available for that graphic

TABLE 4-11. POWERS OF TWO TABLE

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25

TABLE 4-12. HEXADECIMAL/DECIMAL INTEGER CONVERSION TABLE

LEFT-MOST BYTE				RIGHT-MOST BYTE			
BITS 0,1,2,3		BITS 4,5,6,7		BITS 8,9,10,11		BITS 12,13,14,15	
HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL
0	0	0	0	0	0	0	0
1	4096	1	256	1	16	1	1
2	8192	2	512	2	32	2	2
3	12288	3	768	3	48	3	3
4	16384	4	1024	4	64	4	4
5	20480	5	1280	5	80	5	5
6	24576	6	1536	6	96	6	6
7	28672	7	1792	7	112	7	7
8	32768	8	2048	8	128	8	8
9	36864	9	2304	9	144	9	9
A	40960	A	2560	A	160	A	10
B	45056	B	2816	B	176	B	11
C	49192	C	3072	C	192	C	12
D	53248	D	3328	D	208	D	13
E	57344	E	3584	E	224	E	14
F	61440	F	3840	F	240	F	15

EXAMPLE:

Convert $A4C7_{16}$ to decimal

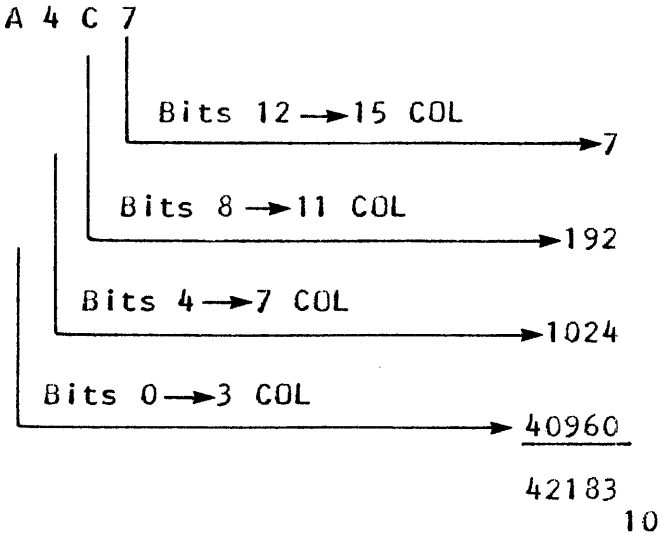


TABLE 4-13. HEXADECIMAL ADDITION AND SUBTRACTION TABLE

	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

TABLE 4-14. HEXADECIMAL MULTIPLICATION TABLE

Example: 2 x 4 = 08, F x 2 = 1E

	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2	02	04	06	08	0A	0C	0E	10	12	14	16	18	1A	1C	1E
3	03	06	09	0C	0F	12	15	18	1B	1E	21	24	27	2A	2D
4	04	08	0C	10	14	18	1C	20	24	28	2C	30	34	38	3C
5	05	0A	0F	14	19	1E	23	28	2D	32	37	3C	41	46	4B
6	06	0C	12	18	1E	24	2A	30	36	3C	42	48	4E	54	5A
7	07	0E	15	1C	23	2A	31	38	3F	46	4D	54	5B	62	69
8	08	10	18	20	28	30	38	40	48	50	58	60	68	70	78
9	09	12	1B	24	2D	36	3F	48	51	5A	63	6C	75	7E	87
A	0A	14	1E	28	32	3C	46	50	5A	64	6E	78	82	8C	96
B	0B	16	21	2C	37	42	4D	58	63	6E	79	84	8F	9A	A5
C	0C	18	24	30	3C	48	54	60	6C	78	84	90	9C	A8	B4
D	0D	1A	27	34	41	4E	5B	68	75	82	8F	9C	A9	B6	C3
E	0E	1C	2A	38	46	54	62	70	7E	8C	9A	A8	B6	C4	D2
F	0F	1E	2D	3C	4B	5A	69	78	87	96	A5	B4	C3	D2	E1

TABLE 4-15. TOOLS AND TEST EQUIPMENT

Description	MRX Part No.
Oscilloscope, Tektronix 465 or equivalent	203161
Digital Voltmeter	203154
Module Extender, 3-Layer Logic	505623
Module Extender, Power Logic	505554
Module Extender, Power with Lugs	505555

SECTION 5. DIAGNOSTIC PROGRAMS

Diagnostic programs run on the 7300 Processing Unit are divided into two groups: micro-diagnostics and MLI diagnostics.

The micro-diagnostics (also referred to as fault isolation routines) are coded in micro-instruction (uI) form and check the shared resources (CPU and main storage) by means of four programs: CPU1, CPU2, CPU3, and Main Storage.

The MLI diagnostics (also referred to as Design Verification Routines or DVR's) are coded in machine-language instruction (MLI) format and check both the shared resources and peripheral devices, including the adapters. The MLI diagnostics are divided into three classes of tests: Autoload, Stand Alone, and Maintenance Monitor.

Details about the MLI diagnostics, including procedures for running the programs and interpreting the results, are contained in the MRX/40 and 50 System Machine Language Diagnostics Operator's Guide. Descriptions of the micro-diagnostics and operating procedures are presently contained in the program listing for each program. At some future date, this information will be included in a formal fault isolation manual.

SECTION 6. SHARED RESOURCES

GENERAL INFORMATION

Information of a general nature which may assist in troubleshooting shared resources (CPU and MS) is presented in selected illustrations contained in both the Support Diagrams Manual and this manual. Illustrations in the Support Diagrams Manual consist of block diagrams and related figures which present overall characteristics of the CPU and MS. Illustrations in this manual are extracted from the 7300 Processing Unit Design Description Manual and consist of selected "memory-jogging" information, such as details of ERF Group I read/write operations. Illustrations related to the CPU are listed below:

Manual	Title	Draw/Fig. No.
7200/7300 Support Diagrams, Volume 1	CPU Block Diagram	503247
	Microcommand Repertoire	504674
	Register File Organization	505983
	7300 Major Cycle Timing	505988
	7300 Minor Cycle Timing	505989
	CS Proper/Address Table Block Diagram	505985
	Basic Storage Protect Block Diagram	506092
	Relocation and Protect Block Diagram	506093
	Job Accounting Block Diagram	506091
7200/7300 Maintenance Manual	Gray Code Counter and E-Timing Waveforms	6-1
	Normal Priority Timing	6-2
	ERF Group I Read/Write Timing	6-3
	CS Page Organization	6-4
	CS Address Selection	6-5

Illustrations related to MS are listed below:

Manual	Title	Draw/Fig. No.
7200/7300 Support Diagrams Manual	MS Special Conventions	506024
	MS With Parity Block Diagram	506067
	MS With ECC Block Diagram	506066
7200/7300 Maintenance Manual	MS Addressing Scheme	6-6

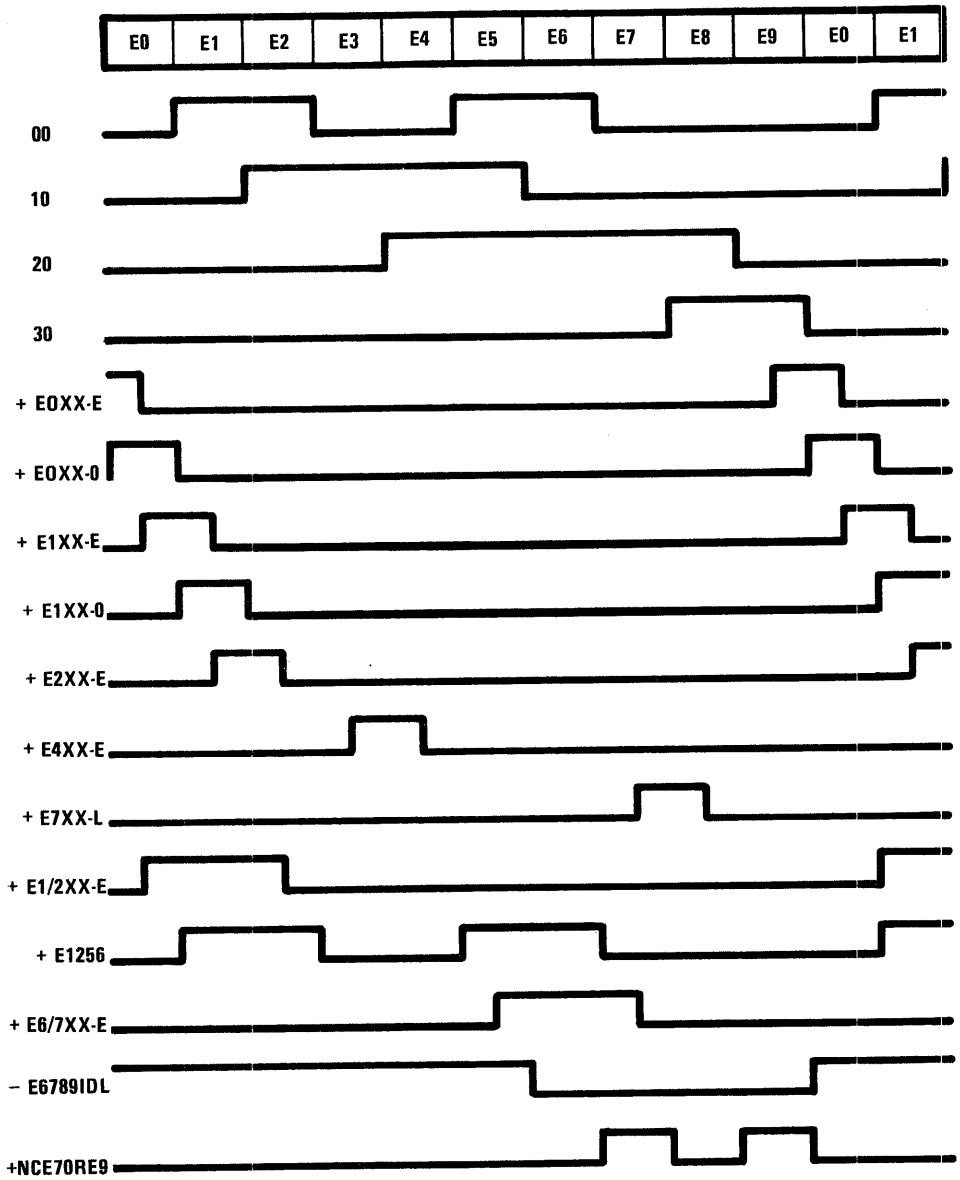


Figure 6-1. Gray Code Counter and E-Timing Waveforms

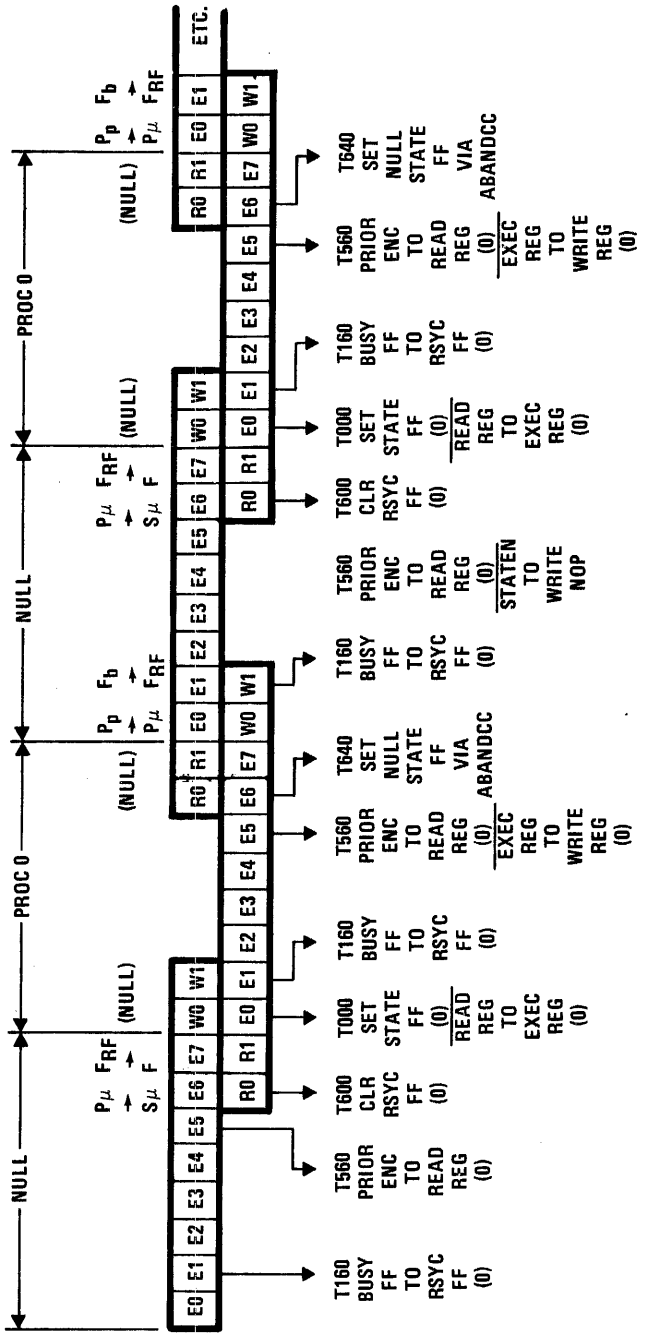
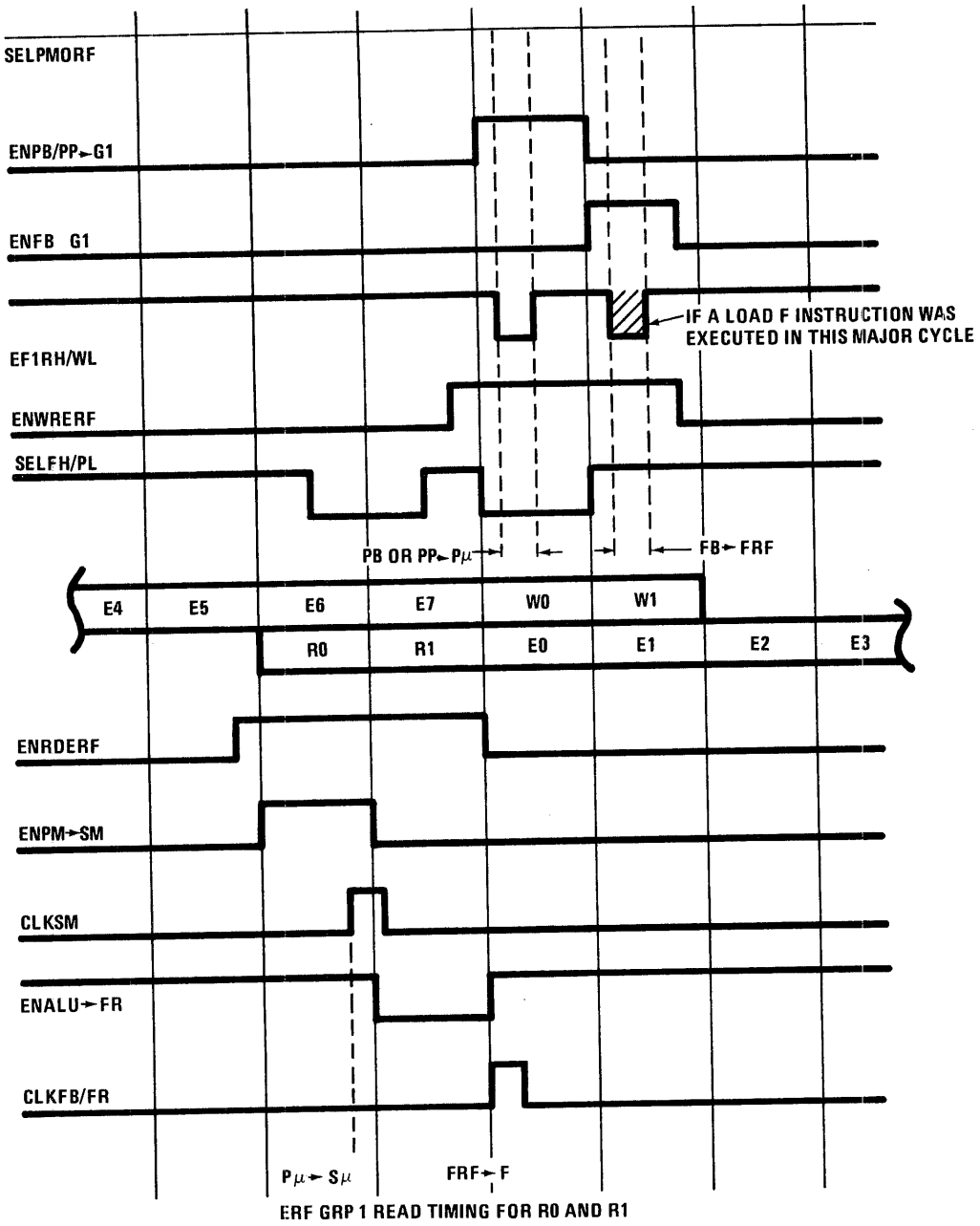


Figure 6-2. Normal Priority Timing



ERF GRP 1 READ TIMING FOR R0 AND R1

Figure 6-3. ERF Group I Read/Write Timing

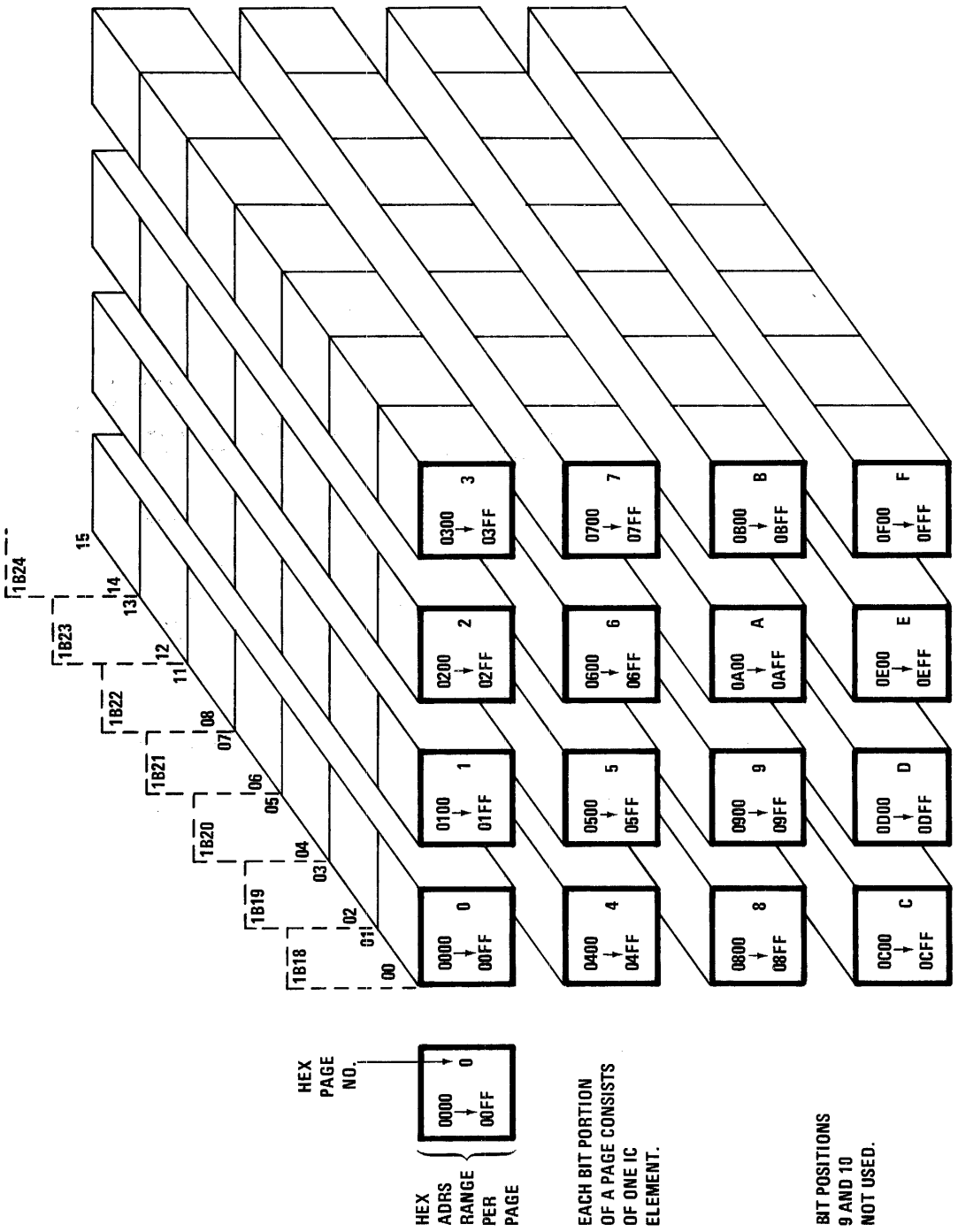


Figure 6-4. CS Page Organization

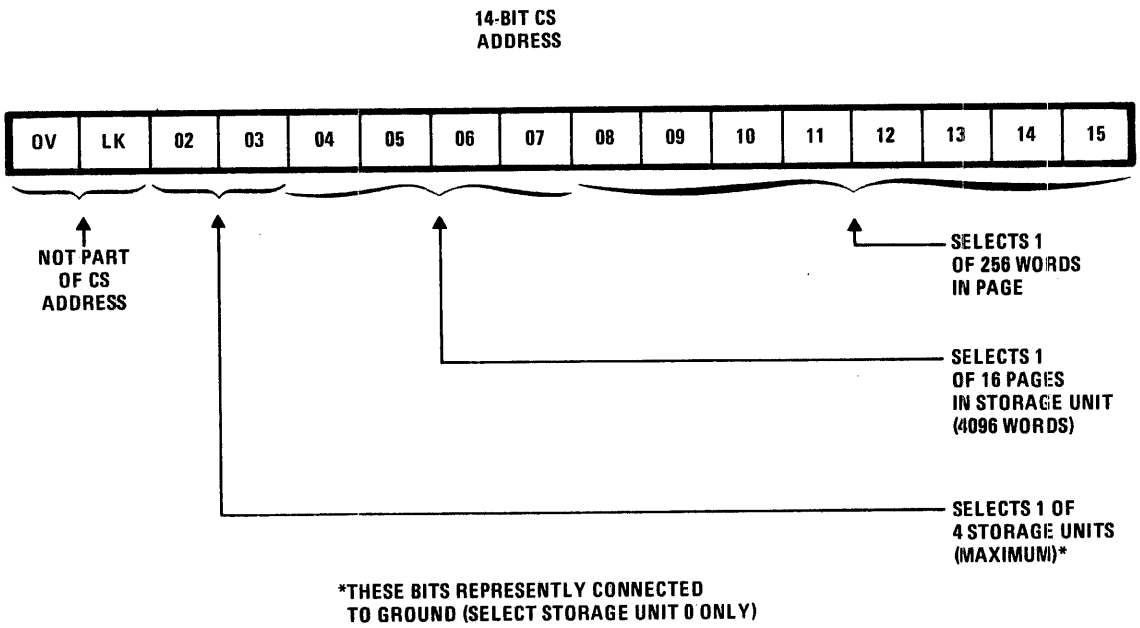


Figure 6-5. CS Address Selection

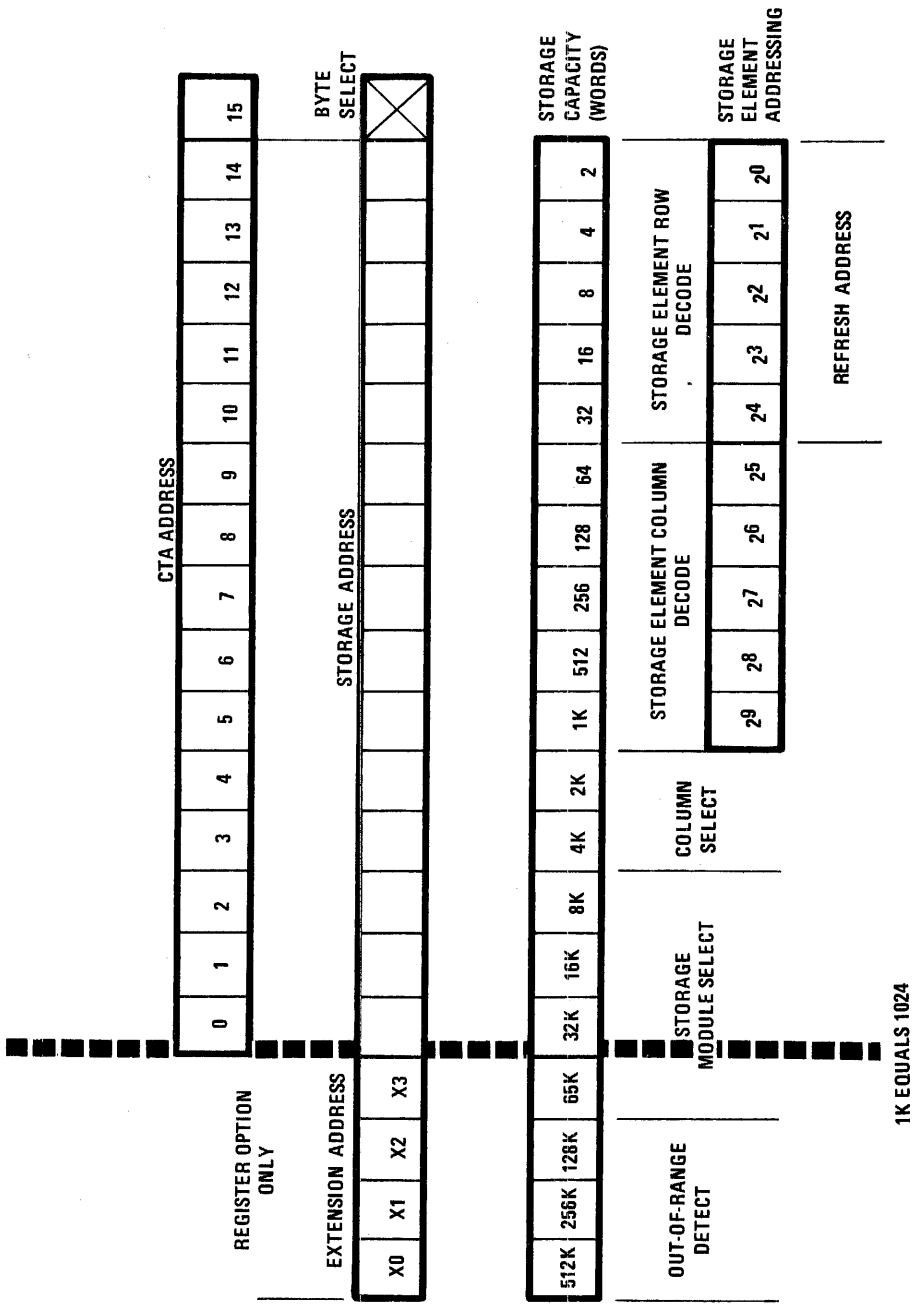


Figure 6-6. MS Addressing Scheme

TIMING CHECKS

NOTE

The following timing checks are very similar to those used to adjust timing during manufacture, modified only as necessary for use in the field. As such, they must be made with extreme care by qualified personnel using proper test equipment that is accurately calibrated. Of utmost importance is that you are convinced; after carefully analyzing other possible causes, that the difficulty is due to faulty timing. NEVER ATTEMPT TO "TUNE OUT" A PROBLEM BY ADJUSTING TIMING JUST AS A CONVENIENT METHOD OF GETTING THE SYSTEM BACK UP. The result invariably causes the problem to reappear somewhere else in the system. This time, however, the problem is doubly difficult to pinpoint because the real cause is being concealed by a faulty timing adjustment.

CPU TIMING CHECKS

Initial Checks

1. Insure that the power sequencer and power supplies have been tested and are working.

2. Be certain that there are no power-to-ground shorts on any of the PC modules.

NOTE

When reading the timing on the scope, assume that at 1.5 volts the logic switches from a logical "0" to a logical "1" and from a logical "1" to a "0".

Excursions Counter

1. Extend module TA15 and insure that time E0 through E7 are each 100 nanoseconds long for 7300 machines or 200 nanoseconds long for 7200 machines and are occuring consecutively. It may be necessary to start on the timing module at 1A12 (BB for 7300 machines or AT for 7200 machines) because times TX40-3 and TX00-2 are needed to drive the excursions counter.

Timing Chain I

1. Set up the oscilloscope using the 1 volt per centimeter scale, 0.1 usec per centimeter divided by 10, and sync internally.

2. Monitor 1A12 TP17 and adjust R17 for a 30-nsec negative pulse. Repetition rate must be 100 nanoseconds for 7300 machines or 200 nanoseconds for 7200 machines.

3. Sync on 1A12 TP17 and look at 1A16 TP19. Sweep R3 to see the range of movement of this pulse.

4. Adjust R3 to the center of its range and adjust R24 for a 30 nsec pulse at 1A16 TP19.

5. Sync on 1A16 TP19.

6. Check timing of all CPU clock and clock-related pulses in accordance with the following drawings in the Support Diagrams Manual, Volume 1: drawing 506194 for the 7300 CPU or drawing 507063 for the 7200 CPU. These drawings tabulate start times, pulse widths, signal polarity, test points, and modules to be removed in order to obtain the correct pulse. If timing is not as indicated, adjust corresponding pair of potentiometers on module 1A12 as listed in Table 6-1. Because adjustment of all signals by any one pair of pots is interrelated, it may be necessary to readjust all other signals of a group if any one has been adjusted.

MS TIMING CHECKS

NOTE

A three-wire, grounded soldering iron must be used when working on the modules. The HH modules (HK modules for 7200, phase 2 and 3 machines) should not be inserted until the timing is set up on the corresponding timing module and the proper signals are getting to the HH (HK) module slots.

Timer Delay Adjustment

The following procedure is used to adjust the width of the TIMER pulse from module 1A13, which is used to generate pulses $E0^{-}$ and $E0^{--}$ from the on-time E-timing chain on module 1A15.

1. Insure that the System is not operating in the consecutive-cycle mode by clearing bits 8 through 15 of the Control register.

2. Sync the oscilloscope on 1A13 TP2, set the display mode selector to CHOPPED, and set up for simultaneous display of the TIMER waveform at 1A13 TP2 and the TX20 waveform at 1A13 TP10. (See Figure 6-7.) Leading edge of the TIMER waveform will start somewhere between E650 and E700 (not critical).

3. If the System has only the non-ECC portion of the Register Option (RO) present (chassis 1), adjust pot R14 on 1A13 so that the trailing edge of the TIMER pulse falls exactly midway between the leading edges of the second and third TX20 pulses from the leading edge of the TIMER pulse; i.e., at E070 (point A on Figure 6-7). This produces a TIMER pulse of about 200 nanoseconds in width, which generates $E0^{-}$ on module 1A15.

4. If the System has both the non-ECC portion (chassis 1) and ECC portion (chassis 2) of the RO present, adjust pot R14 on 1A13 so that the trailing edge of the TIMER pulse falls exactly midway between the leading edges of the third and fourth TX20 pulses from the leading edge of the TIMER pulse; i.e., at $E070^{-}$ (point B on Figure 6-7). This produces a TIMER pulse of about 300 nanoseconds in width, which generates both $E0^{-}$ and $E0^{--}$ on module 1A15.

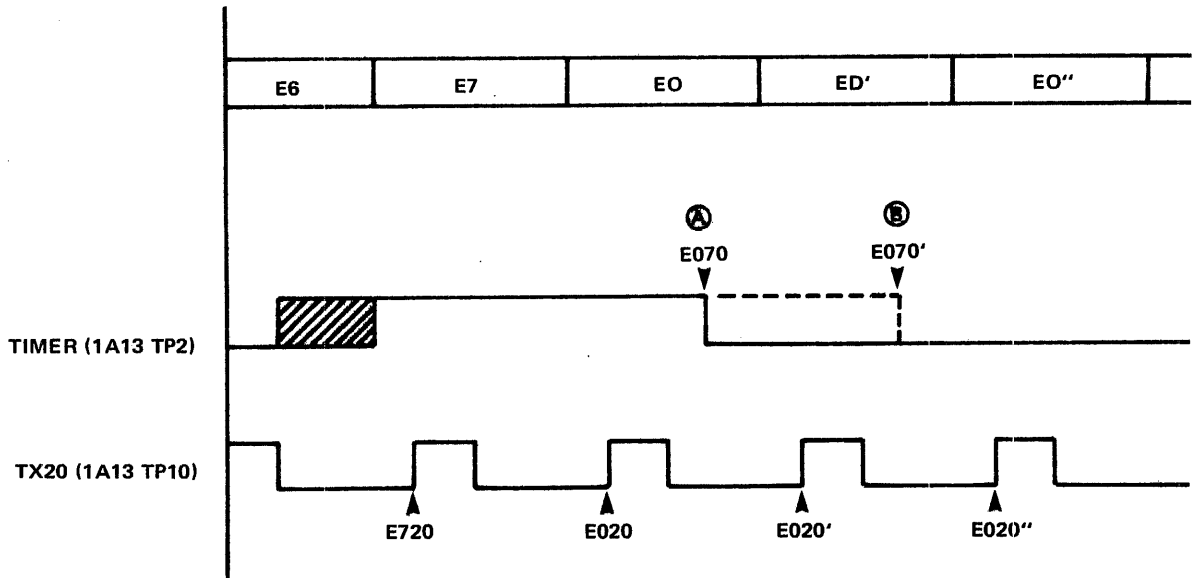


Figure 6-7. Timer Delay Waveforms

TABLE 6-1. CPU TIMING POTENTIOMETERS

SIGNAL	POT ADJUST
+CLKFM-0 +CLKFM-1 +CLKFB/FR0 +CLKFB/FR1 +TX00-N	R01 and R02
+TX00-1 +TX00-2 +TX00-3 +TX00-4	R03 and R04
+CLKAM/BM0 +CLKAM/BM1 +CLKDR +TX20-1 +TX20-2	R05 and R06
+TX40-1 +TX40-2 +TX40-3	R07 and R08
+TX60-1 +TX60-2 +TX60-3 +CLKBUFF +TX60-4	R09 and R10
+CLK-S/R0 +CLK-S/R1 +CLKS/RDR +TX80-N +TX80-N1	R11 and R12
+CLKMR/NR +CLKSM/PB +CLKPP +1X80-1 +TX80-2 +TX80-3 +CLKERFG2	R13 and R14
+CLKSR	R15 and R16
+NORMWR	R18 and R19
+LATEWR	R20 and R21
+BRFWRITE	R22 and R23

Refresh Timing Checks

1. Check to see that a clock pulse recurring every 800 nanoseconds (if a 7300 machine) or every 1600 nanoseconds (if a 7200 machine) is present on the following modules, unless ECC is installed (7300 machines only):

7300	7200,Ø1	7200,Ø2	7200,Ø3
2B12 TP2	2B12 TP2	2A10 TP1	2A10 TP1

2. Check operation of refresh counter by checking toggling rate of the following test points:

   a. 7300 and 7200,01 machines:

   2B11 TP2 - 42 usec
   2B11 TP3 - 84 usec
   2B11 TP4 - 167 usec
   2B11 TP6 - 333 usec
   2B11 TP7 - 665 usec

   b. 7200,02 and 7200,03 machines:

   2A10 TP10 - 42 usec

3. Check that REFRESH REQUEST and REFRESH signals occur every 42 usec at the following test points:

	7300	7200,Ø1	7200,Ø2	7200,Ø3
REFRESH REQ. Test Point	2B12 TP6	2B12 TP6	2A10 TP6	2A10 TP6
Polarity	+	+	-	-
REFRESH Test Point	2B12 TP10	2B12 TP10	2A10 TP11	2A10 TP11
Polarity	+	+	-	-

Timing Module Adjustments

Adjust the pulses below in accordance with timing data listed in the following timing diagrams, depending on the system model:

7300	7200,Ø1	7200,Ø2	7200,Ø3
506195 (parity) 506196 (ECC)	507065	-	507068

These timing diagrams, contained in Volume 1 of the Support Diagrams Manual, list test points, pulse widths, and leading and trailing edges for each pulse. Scope each pulse by syncing

negative and using the main storage clock pulse as a reference. Refer to step 1 of the Refresh Timing Check procedure above for test points at which this clock pulse appears. Each pulse is adjusted by means of a potentiometer contained on the timing module in each machine. This module contains twelve 15-turn screwdriver adjust potentiometers as shown in Figure 6-8. The type and location of this module for each machine model is as follows:

7300	7200,Ø1	7200,Ø2	7200,Ø3
HG,2B12 (parity) HC,2B12 (ECC)	HM,2B13	HK,2A10	HK,2A10

1. Gate Access Enable

   The critical point is the positive-going edge of the pulse. Adjust via GATE A.E. ADJ pot R22 on Figure 6-8.

2. Address Time (Set)

   Set CONSOLE MODE SELECT selector to MS-RD. Adjust the positive-going edge at this time via ADDRESS SET ADJ pot R24. The negative-going edge must be set later.

3. Precharge

   Set CONSOLE MODE SELECT selector to MS-WR. The negative-going edge is set via PRECHARGE DELAY ADJ pot R23. The positive-going edge of this signal has a switch for the purpose of running timing margins on the storage system. This switch is labeled TIMING MARGINS in Figure 6-8. With this switch in the upper (normal) position, the positive-going edge of the precharge signal should be set via PRECHARGE WIDTH ADJ pot R21. With the switch in the middle position, the positive-going edge should be 12 ±2 nanoseconds later than the normal position. With the switch in the lower position, the positive-going edge should be 12 ±2 nanoseconds earlier than the normal position.

4. Column Select

   Set CONSOLE MODE SELECT selector to MS-WR. The negative-going edge is set via COLUMN SELECT DELAY ADJ pot R26. Adjust the positive-going edge via COLUMN SELECT WIDTH ADJ pot R29.

5. Strobe/Clear SDR

   Set CONSOLE MODE SELECT selector to MS-RD. Adjust the positive-going edge of the Clear SDR signal via STROBE ADJ pot R30. After this adjustment has been set, the Strobe signal should be verified.

6. Address Time (Clear)

   Set CONSOLE MODE SELECT selector to MS-RD. The positive-going edge has been adjusted in step 2. Now adjust the negative-going edge via ADDRESS CLEAR ADJ pot R25.

7. Write

   Set CONSOLE MODE SELECT selector to MS-WR. Adjust the positive-going edge of this signal via WRITE DELAY ADJ pot R28 and the negative-going edge via WRITE WIDTH ADJ pot R27.

8. Digit

   Set CONSOLE MODE SELECT selector to MS-WR. Adjust the positive-going edge via DIGIT DELAY ADJ pot R31 and the negative-going edge via DIGIT WIDTH ADJ pot R32.

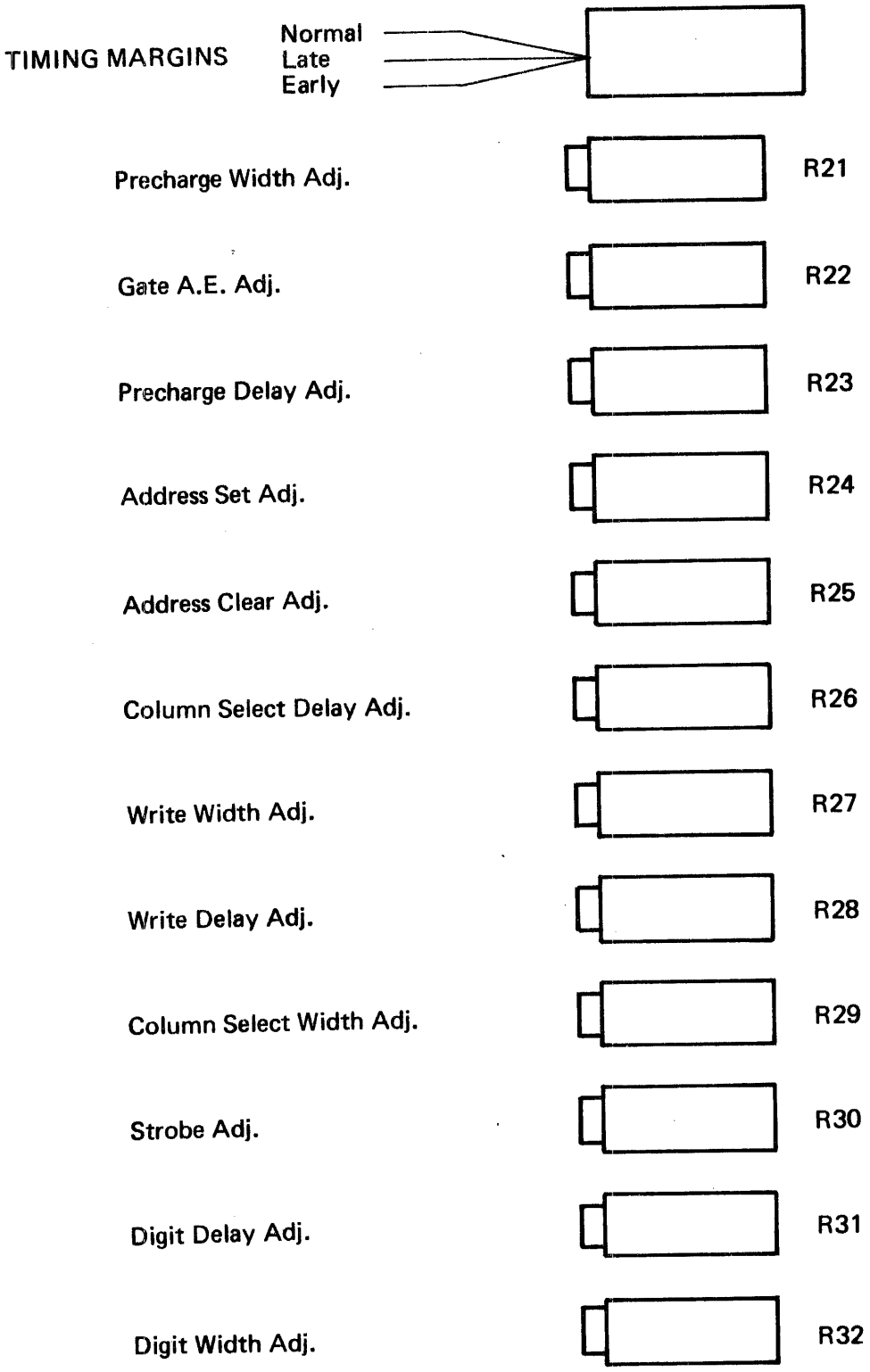


Figure 6-8. Timing Adjustment Potentiometers

SECTION 7. INTEGRATED COMMUNICATIONS ADAPTER

COMMAND WORD FORMATS

Tables 7-1 through 7-5 present the bit structure for each of the words transmitted between the shared resources and the Integrated Communication Adapter (ICA). Tables 7-1 and 7-2 illustrate formats for inbound (ICA to shared resources) and outbound (shared resources to ICA) words for asynchronous data transmission. Tables 7-3 and 7-4 present the same information but for synchronous transmission.

TABLE 7-1. ICA TO SHARED RESOURCES (ASYNCHRONOUS)

ER13	OUTPUT REQUEST				INPUT CHARACTER				UNSOLICITED STATUS				SOLICITED STATUS			
00	0	REQ. OFF	1	REQ. ON	0	REQ. OFF	1	REQ. ON	0	REQ. OFF	1	REQ. ON	0	REQ. OFF	1	REQ. ON
01	0	IDENTIFIER			0	IDENTIFIER			1	IDENTIFIER			1	IDENTIFIER		
02	0	BITS			1	BITS			0	BITS			1	BITS		
03	0	NOT			0	NOT			X	NOT			0	NOT		
04	0	USED			0	USED			X	USED			0	USED		
05	0				0				X				0			
06	X				0	GOOD PARITY	1	BAD PARITY	X				0	ECHOPLEX OFF	1	ECHOPLEX ON
07	X				0	NOT A CNTRL. CHAR.	1	CONTRL. CHAR.	X				0	EVEN PARITY	1	ODD PARITY
08	X	SAME AS UNSOLICITED STATUS BITS 6 15			X	M.S.B. OR 0 = GOOD PARITY			0	DATA SET RDY OFF	1	DATA SET RDY ON	0	DATA TERM RDY OFF	1	DATA TERM RDY ON
09	X				X	1 = BAD PARITY			0	CLEAR TO SEND OFF	1	CLEAR TO SEND ON	0	REQ. TO SEND OFF	1	REQ. TO SEND ON
10	X				X				0	RCVD LINE SIG DET OFF	1	RCVD LINE SIG DET ON	0	XMIT DATA MARK	1	XMIT SPACE CLAMP
11	X				X	DATA CHARACTER			0	SEC. RCVD L.S. DET OFF	1	SEC. RCVD L.S. DET ON	0	SEC. REQ. TO SEND OFF	1	SEC. REQ. TO SEND ON
12	X				X				0	RING IND. OFF	1	RING IND. ON	0	ON HOOK	1	OFF HOOK
13	X				X				0	NO-OP	1	LOST DATA	X			
14	X				X				0	NO-OP	1	NO STOP BIT	X	BAUD- RATE		
15	X				X	L.S.B.			0	NO-OP	1	CHANGE IN STATUS	X	CODE ①		

①	BAUD-RATE CODE
0	RESERVED
1	RESERVED
2	1200 B, SYNC.
3	1200 B, 120 C.P.S.
4	600 B, 60 C.P.S.
5	300 B, 30 C.P.S.
6	150 B, 15 C.P.S.
7	110 B, 10 C.P.S.

TABLE 7-2. SHARED RESOURCES TO ICA (ASYNCHRONOUS)

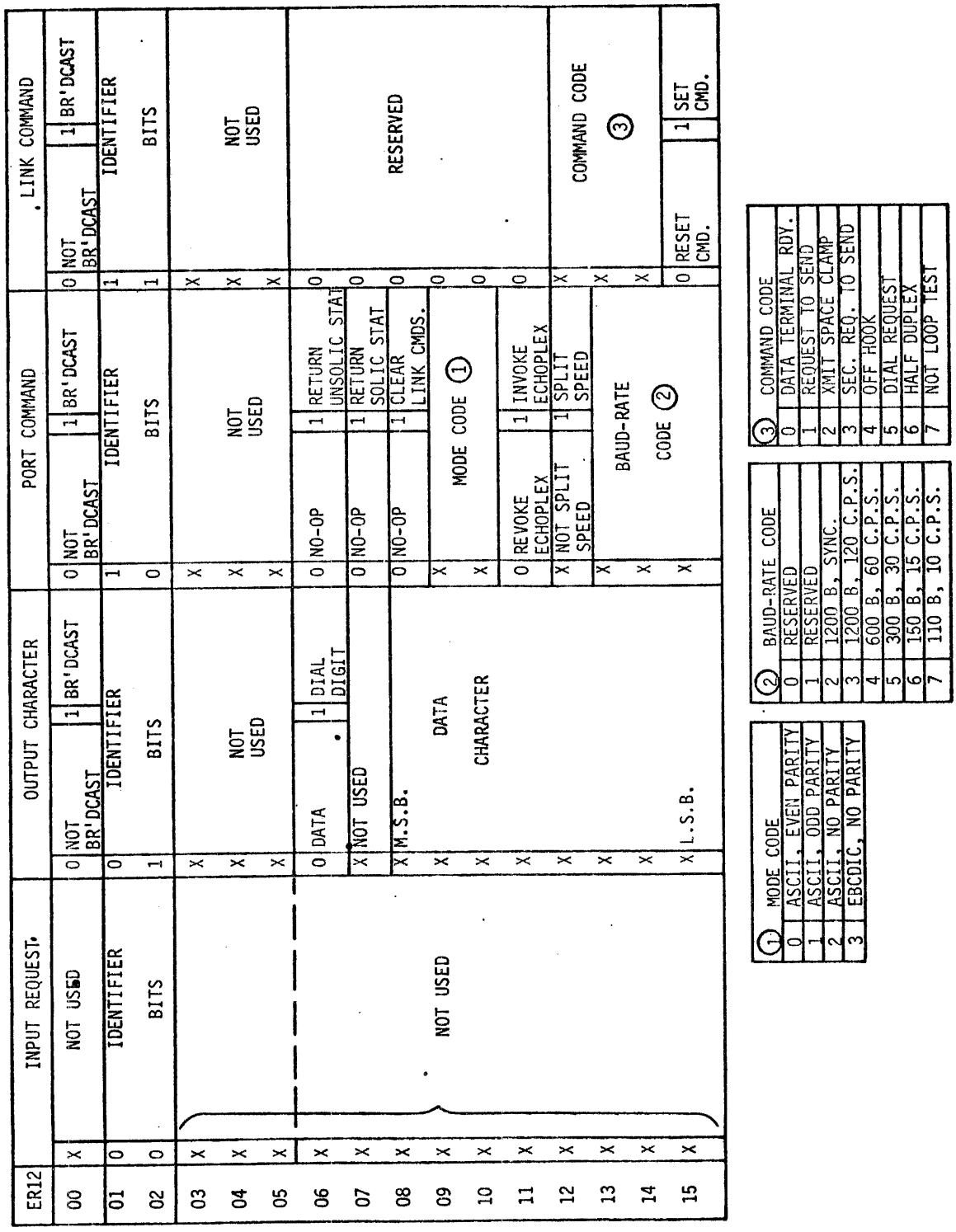


TABLE 7-3. ICA TO SHARED RESOURCES (SYNCHRONOUS)

ER13	OUTPUT REQUEST				INPUT CHARACTER				UNSOLICITED STATUS				SOLICITED STATUS			
00	0	REQ. OFF	1	REQ. ON	0	REQ. OFF	1	REQ. ON	0	REQ. OFF	1	REQ. ON	0	REQ. OFF	1	REQ. ON
01	0	IDENTIFIER			0	IDENTIFIER			1	IDENTIFIER			1	IDENTIFIER		
02	0	BITS			1	BITS			0	BITS			1	BITS		
03	0	NOT			0	NOT			X	NOT			0	NOT		
04	0	USED			0	USED			X	USED			0	USED		
05	0				0				X				0			
06	X				0	GOOD PARITY	1	BAD PARITY	0	NO-OP		B.C.C. RCVD.	0	XPARNT MD. DISABLED	1	XPARNT MD. ENABLED
07	X				0	NOT A CNTRL. CHAR.	1	CNTRL. CHAR.	0	NO-OP		B.C.C. ERROR	0	L.A. IS EBCDIC	1	L.A. IS ASCII
08	X				X	M.S.B. OR 0 = GOOD PARITY			0	DATA SET RDY. OFF	1	DATA SET RDY. ON	0	DATA TERM RDY. OFF	1	DATA TERM RDY. ON
09	X	SAME AS UNSOLICITED STATUS BITS 6 15			X	1 = BAD PARITY			0	CLEAR TO SEND OFF	1	CLEAR TO SEND ON	0	REQ. TO XMIT OFF	1	REQ. TO XMIT ON
10	X				X	DATA			0	RCVD. LINE SIG DET OFF	1	RCVD. LINE SIG DET ON	0	NOT XPARNT MODE	1	XPARNT MODE
11	X				X	CHARACTER			0	SEC. RCVD. L.S. DET OFF	1	SEC. RCVD. L.S. DET ON	0	SEC. REQ. TO SEND OFF	1	SEC. REQ. TO SEND ON
12	X				X				0	RING IND. OFF	1	RING IND. ON	0	ON HOOK	1	OFF HOOK
13	X				X				0	NO-OP	1	LOST DATA	0	NO-OP	1	EOT SEARCH MODE
14	X				X				0	NO-OP	1	TIMER EXP.	0	SYNC NOT ESTB.	1	SYNC ESTB.
15	X				X	L.S.B.			0	NO-OP	1	CHANGE IN STATUS	0	NOT DELETE SYNC MODE		DELETE SYNC MODE ON

NOTE: INPUT CHAR BIT 06 - USED FOR ASCII CODE
NOT IN TRANSPARENT MODE

TABLE 7-4. SHARED RESOURCES TO ICA (SYNCHRONOUS)

ER12	INPUT REQUEST		OUTPUT CHARACTER		PORT COMMAND		LINK COMMAND	
00	X	NOT USED	0 NOT BR'DCAST	1 BR'DCAST	0 NOT BR'DCAST	1 BR'DCAST	0 NOT BR'DCAST	1 BR'DCAST
01	0	IDENTIFIER	0	IDENTIFIER	1	IDENTIFIER	1	IDENTIFIER
02	0	BITS	1	BITS	0	BITS	1	BITS
03	X		X	NOT	X	NOT	X	NOT
04	X		X	USED	X	USED	X	USED
05	X		X		X		X	
06	X		0 DATA CHAR.	1 DIAL DIGIT	0 NO-OP	1 RETURN UNSOLIC STAT	X	
07	X		0 NOT XPARNT CNTRL. CHAR.	1 XPARENT CNTRL. CHAR.	0 NO-OP	1 RETURN SOLIC STAT	X	
08	X		X M.S.B.		0 NO-OP	1 CLEAR LINK CMDS.	X	RESERVED
09	X	NOT USED	X		X	NOT	X	
10	X		X	DATA	X	USED	X	
11	X		X	CHARACTER	0 NO-OP	1 RESYNC	0 DISABLE XPARNT MODE	1 EN-XPARNT MODE
12	X		X		X		X	
13	X		X		X	NOT	X	COMMAND
14	X		X		X	USED	X	CODE (1)
15	X		X L.S.B.		X		0 RESET CMD.	1 SET CMD.

(1)	COMMAND CODE
0	DATA TERMINAL RDY.
1	REQUEST TO XMIT
2	NOT DELETE SYNC MODE
3	SEC. REQ. TO SEND
4	OFF HOOK
5	DIAL REQUEST
6	EOT SEARCH MODE
7	NOT LOOP TEST

NOTE: MASTER CLEAR

LINE ADAPTER ADDRESSING

Table 7-5 shows the format for the line adapter address. This address is identical for both inbound (ER 1F) and outbound (ER 1D) command words, except that the Input Request command word requires no line address. These address bits are associated with each of the 16 line adapter modules as shown in drawing 506008, Communication Line Address Structure, in the Support Diagrams Manual.

TABLE 7-5. LINE ADAPTER ADDRESS BITS, ER 1D AND ER 1F

00 01 02 03	THESE EXTENDED ADDRESS BITS MUST BE ZEROS FOR LA ADDRESS 0-F
04 05 06 07	LINE ADAPTER ADDRESS (0-F)
08 09 10 11 12 13 14 15	RESERVED

RS-232C SIGNAL INTERCHANGE

Table 7-6 lists the names of EIA Standard RS-232C interface signals between the ICA and data modem, together with corresponding connector pin numbers and Bell System Alphabetical designations.

TABLE 7-6. EIA STANDARD RS-232C SIGNALS

Signal Name	Connector Pin No.	Bell System Design.
Protective Ground	1	AA
Transmitted Data	2	BA
Received Data	3	BB
Request to Send	4	CA
Clear to Send	5	CB
Data Set Ready	6	CC
Signal Ground Return (Common)	7	AB
Received Line Signal Detector	8	CF
(Reserved for Data Set Testing)	9	--
(Reserved for data Set Testing)	10	--
(Unassigned)	11	--
Sec. Received Line Signal Detector	12	SCF
Sec. Clear to Send	13	SCB
Sec. Transmitted Data	14	SBA
Transmitter Signal Element Timing	15	DB
Sec. Received Data	16	SSB
Receiver Signal Element Timing	17	DD
(Unassigned)	18	--
Sec. Request to Send	19	SCA
Data Terminal Ready	20	CD
Signal Quality Detector	21	CG
Ring Indicator	22	CE
Data Signal Rate Selector	23	CH/CI
Transmit Signal Element Timing	24	DA
(Unassigned)	25	--

Notation	Interchange Voltage	
	Negative	Positive
Binary State	1	0
Sig. Condition	Marking	Spacing
Function	OFF	ON

Figure 7-1 diagrams the direction of the RS-232C signal exchanges across the interface between the ICA and either an external modem or a local terminal. It shows that the Transmitted Data signal from the ICA appears at the modem as Transmitted Data (top half of figure) as Received Data. Other signals may be traced in the same manner.

(Note that the Off Hook signal from the ICA goes not to the modem, but to the Bell System's Data Access Arrangement. This line is required when the comm line uses a modem that has not been supplied by the Bell System.)

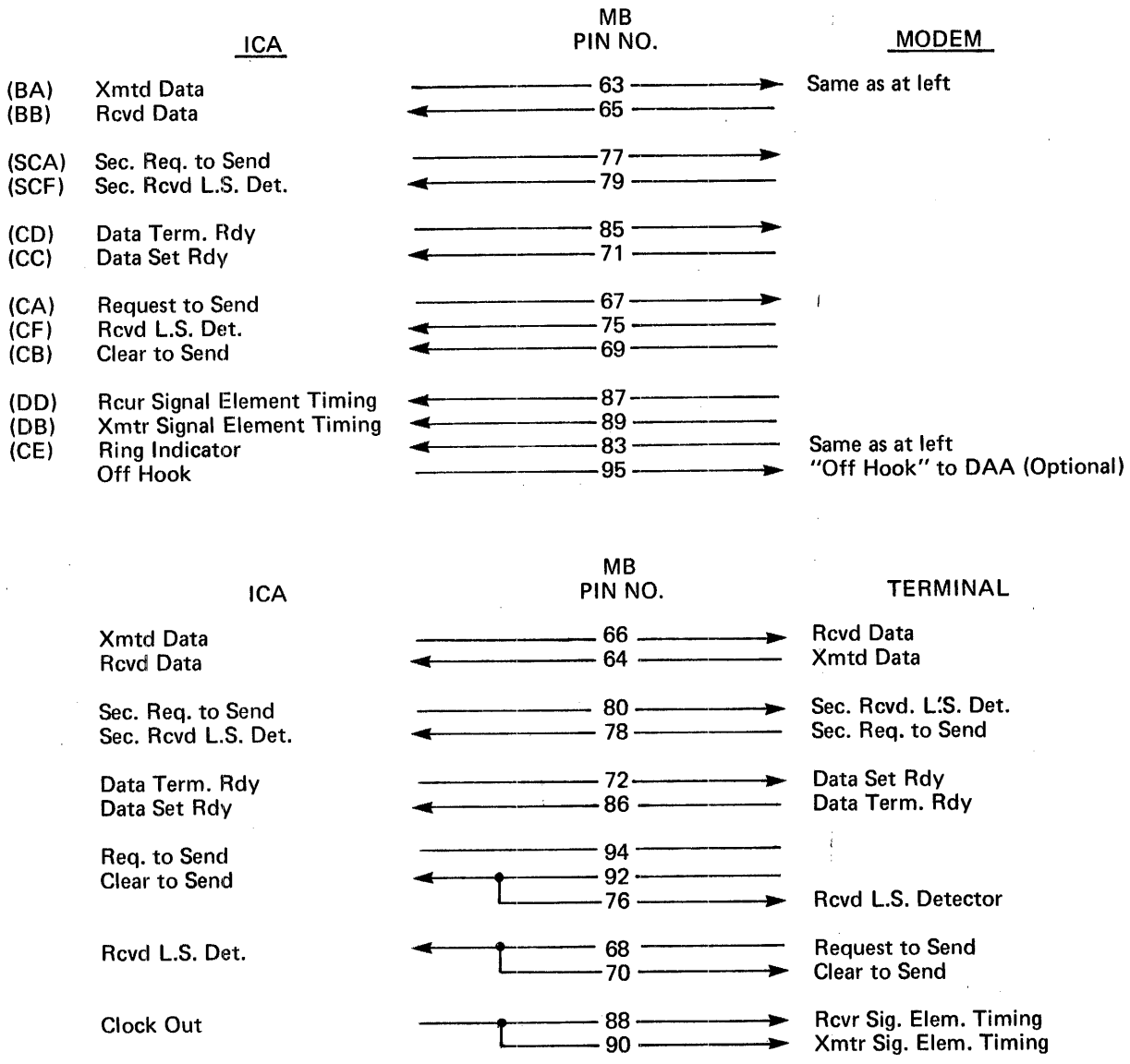


Figure 7-1. RS-232C Signal Exchange

SECTION 8. BASIC DATA CHANNEL

Command codes used to initiate operations in peripheral devices that communicate with the 7200/7300 Processing Unit via the basic data channel (BDC) are listed in Table 8-1. ERF Group III registers associated with the BDC and bit set therein are listed in Table 8-2.

TABLE 8-1. BDC DEVICE COMMAND CODES (Page 1 of 3)

Device	Operation	Command Code
Card Reader	Read (and Feed): EBCDIC Mode Card Image Mode	 02 22
	Test I/O No Operation Sense	00 03 04
Line Printer	Write (no Line Spacing)	01
	Write and Space: Space 1 line Space 2 lines Space 3 Lines Space 4 lines . . Space 14 Lines Space 15 Lines	 09 11 19 21 . . 71 79
	Space Immediate: Space 1 Line Space 2 Lines Space 3 Lines Space 4 Lines . . Space 14 Lines Space 15 Lines	 0B 13 1B 23 . . 73 7B
	Write and Skip: Skip to Channel 1 (top of form) Skip to Channel 2 Skip to Channel 3 Skip to Channel 4 . . Skip to Channel 11 Skip to Channel 12	 09 91 99 A1 . . D9 E1

TABLE 8-1. BDC DEVICE COMMAND CODES (Page 2 of 3)

Device	Operation	Command Code
Line Printer	Skip Immediate:	
	Skip to Channel 1 (top of form)	8B
	Skip to Channel 2	93
	Skip to Channel 3	9B
	Skip to Channel 4	A3
	.	.
	.	.
	Skip to Channel 11	D9
	Skip to Channel 12	E1
	Test I/O	00
	No Operation	03
	Sense	04
Card Reader/Punch	Read Only:	
	EBCDIC Mode	0A
	Card Image Mode	2A
	Feed and Select Stacker:	
	Without Offset	23
	With Offset	A3
	Read, Feed, and Select Stacker:	
	EBCDIC Mode, Without Offset	02
	EBCDIC Mode, With Offset	82
	Card Image Mode, Without Offset	22
	Card Image Mode, With Offset	A2
	Punch, Feed, and Select Stacker:	
	EBCDIC Mode, Without Offset	01
	EBCDIC Mode, With Offset	81
	Card Image Mode, Without Offset	21
	Card Image Mode, With Offset	A1
	Test I/O	00
	No Operation	03
	Sense	04

TABLE 8-1. BDC DEVICE COMMAND CODES (Page 3 of 3)

Device	Operation	Command Code
Magnetic Tape	Write Forward	01
	Read Forward	02
	Rewind	07
	Rewind and Unload	0F
	Backspace:	
	Block	27
	File	2F
	Forward Space:	
	Block	37
	File	3F
	Write Tapemark (End-of-File)	1F
	Erase Gap	17
	Force Error Mode:	
	Set	E3
	Clear	D3
	Test I/O	00
	No Operation	X5, X6, XD, XE
	Sense	04

TABLE 8-2. BDC REGISTER BIT ASSIGNMENTS

Reg. / Bit	BUS IN (ERF 10)	STATUS (ERF 10)	TAG IN (ERF 11)	TAG OUT (ERF 11)	RD CHAN CONT (ERF 12)
0	BUS IN 0	ATTN	ADRS IN	*	HDW CNT XFR
1	BUS IN 1	STAT MODIF	STATUS IN	*	RD OPER
2	BUS IN 2	CONT UN END	SVC IN	*	DIAGN MD
3	BUS IN 3	BUSY	OPRTL IN	*	DATA CHAIN
4	BUS IN 4	CHAN END	SEL IN	*	CONT CHK
5	BUS IN 5	DEV CHK	REQ IN	*	XMN CHK
6	BUS IN 6	UN CHK	DATA IN	*	ILL LGTH IND
7	BUS IN 7	UN EXEC	DISC IN	*	ASM/DISASM
8	BUS IN 0	INT SEL FL	*	ADRS OUT	MARK 0 IN
9	BUS IN 1	COMM INV	*	COMM OUT	*
10	BUS IN 2	WRG ADRS IN	*	SVC OUT	*
11	BUS IN 3	NO REQ IN	*	OPRTL IN	*
12	BUS IN 4	CONT CHK	*	SEL OUT	*
13	BUS IN 5	XMN CHK	*	SUPP OUT	*
14	BUS IN 6	ILL LGTH	*	DATA OUT	*
15	BUS IN 7	*	*	*	*

Reg. / Bit	RD BYTE CNT (ERF 13)	WR CHAN CONT (ERF 13)	BUS OUT (ERF 14)	WR BYTE CNT (ERF 18)
0				
0	0	HDW CNT XFR	BUS OUT 0	0
1	1	RD OPER	BUS OUT 1	1
2	2	DIAGN MD	BUS OUT 2	2
3	3	DATA CHAIN	BUS OUT 3	3
4	4	*	BUS OUT 4	4
5	5	*	BUS OUT 5	5
6	6	*	BUS OUT 6	6
7	7	ASM/DISASM	BUS OUT 7	7
8	8	*	BUS OUT 0	8
9	9	*	BUS OUT 2	9
10	10	*	BUS OUT 3	10
11	11	*	BUS OUT 4	11
12	12	*	BUS OUT 5	12
13	13	*	BUS OUT 6	13
14	14	*	BUS OUT 7	14
15	15	*	BUS OUT 8	15

* = Bit not defined

SECTION 9. INTEGRATED FILE ADAPTER

Information of a general nature which may assist in troubleshooting the disc Integrated File Adapter (IFA) is presented in selected illustrations contained in both the MRX 7200/7300 Support Diagrams Manual and this manual. Illustrations in the Support Diagrams Manual consist of unit and bus (multiplex) connector wiring diagrams referenced below:

Title	Drawing No.
Disc File Unit Connectors J04-J12 Wiring	506076, Vol. 1
Disc File Bus Connector J15 Wiring	506077, Vol. 1

Illustrations in this manual are extracted from the 7300 Processing Unit Design Description Manual and consist of selected "memory-jogging" information relating to command word, track, record, and gap formats. Command word formats are presented in Table 9-1, which lists each command word and associated ERF Group III register in which it is placed, and Figures 9-2 through 9-10, which show bit assignments of each command word listed in Table 9-1. Various track, record, and gap formats are shown in Figures 9-11 through 9-18.

TABLE 9-1. IFA REGISTER ASSIGNMENTS

MLI	Command	Reg. Address	Fig. Ref.
DIO	Write	Write ER 11 and 15	9-1
	Format Write	Write ER 11 and 15	9-2
	Read	Write ER 11 and 15	9-3
	Read Without Transfer	Write ER 11 and 15	9-4
	Search (same as Read)	Write ER 11 and 15	9-3
INP	--	--	9-5
OUT	Select Drive	Write ER 10	9-6
	CS Load	Write ER 11	9-7
	Diagnostics	Write ER 11	9-8
	Control	Write ER 11	9-9
	Write Hardware Status	Write ER 12	9-10
	Write Other Status	Write ER 13 or 17	9-11

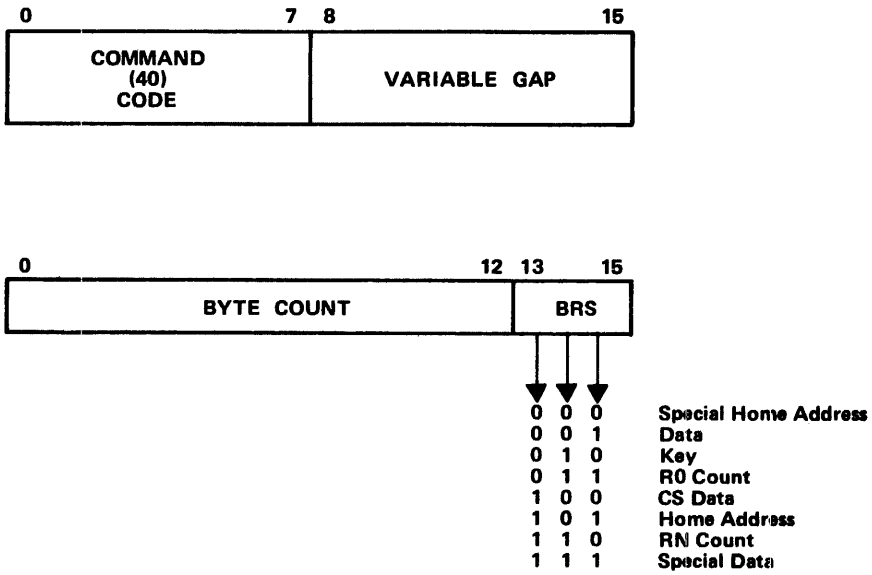


Figure 9-1. Write Command

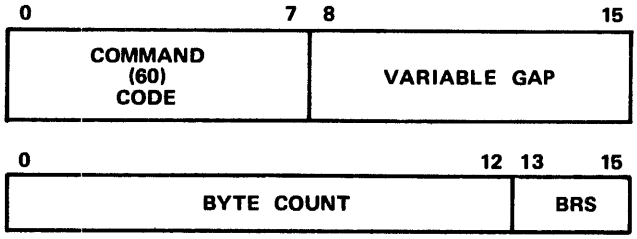


Figure 9-2. Format Write Command

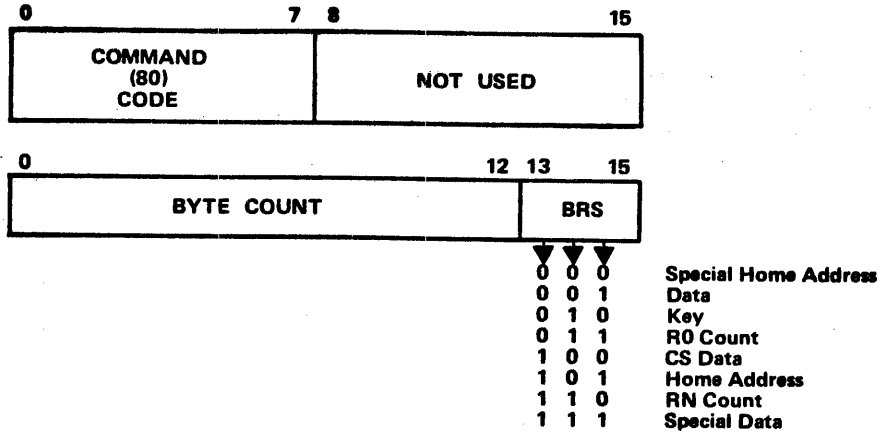


Figure 9-3. Read Command

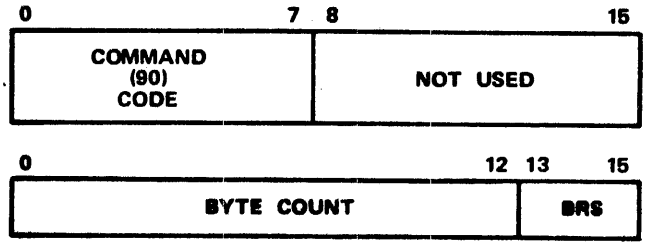


Figure 9-4. Read Without Transfer Command

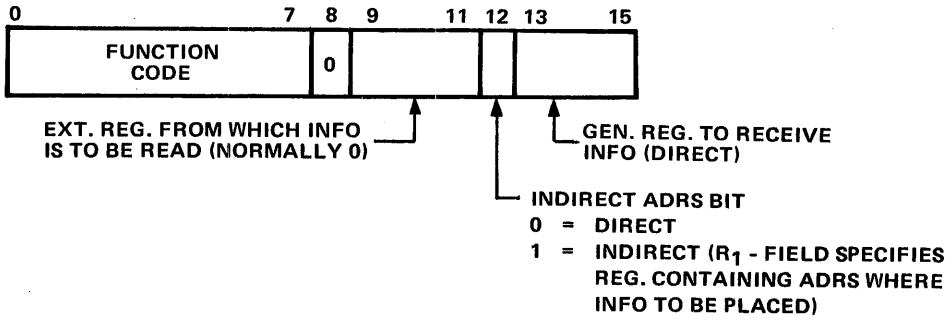


Figure 9-5. INP Instruction Format

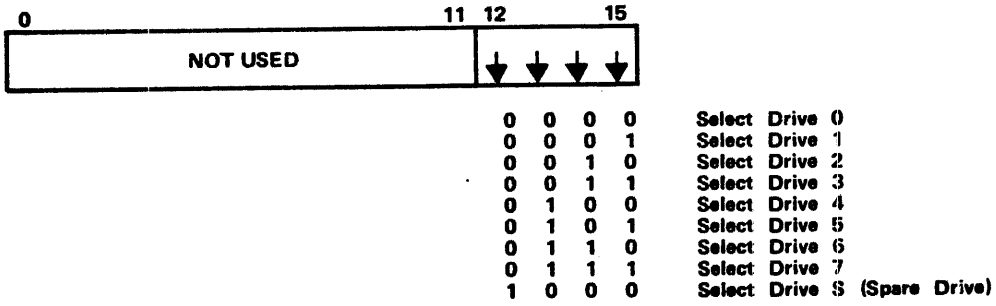


Figure 9-6. Select Drive Command

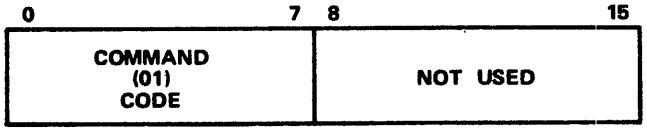


Figure 9-7. CS Load Command

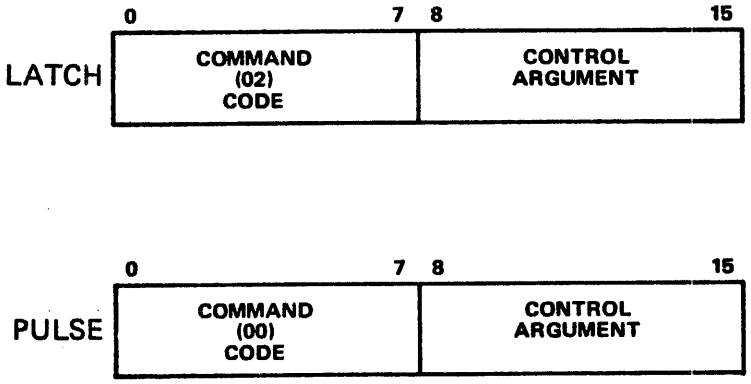


Figure 9-8. Diagnostics Command

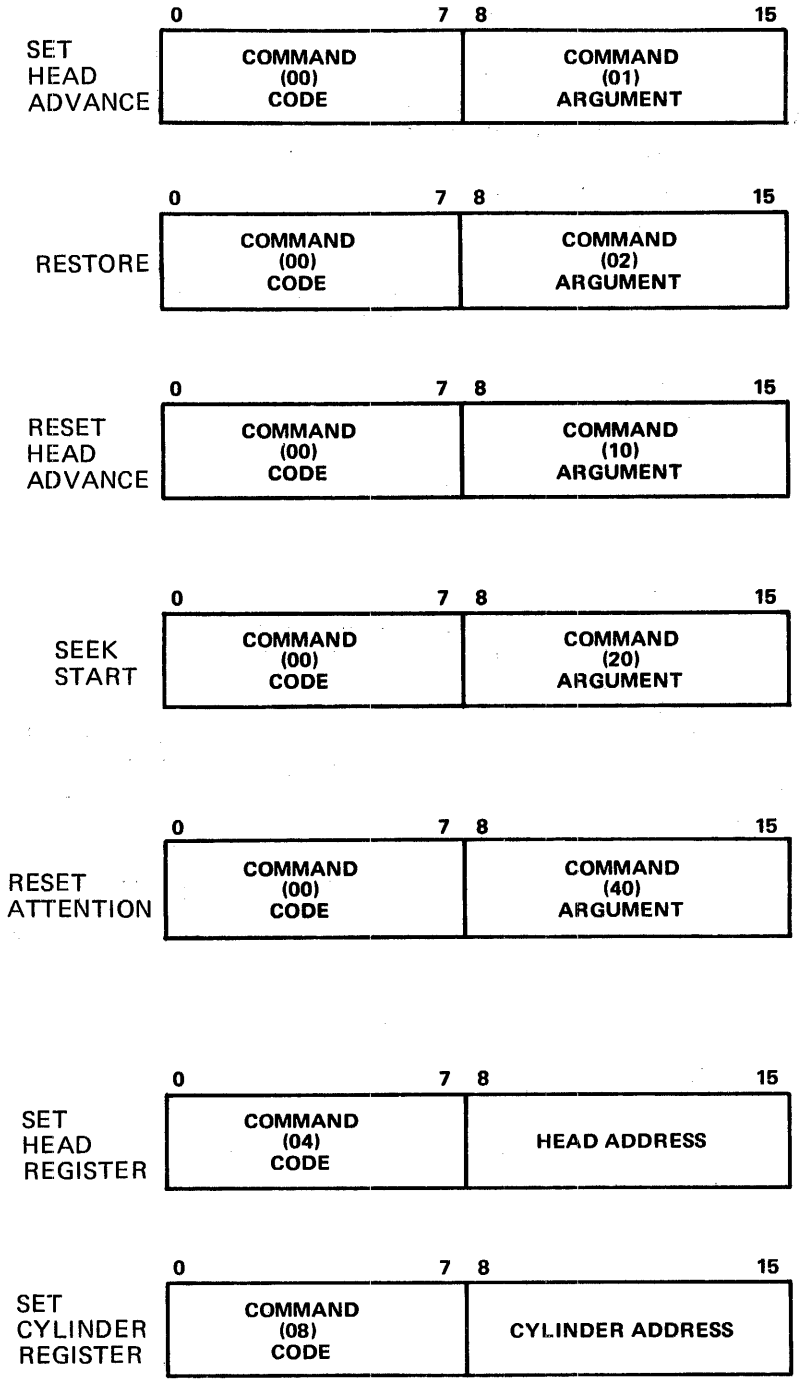
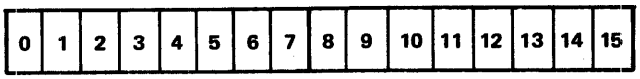
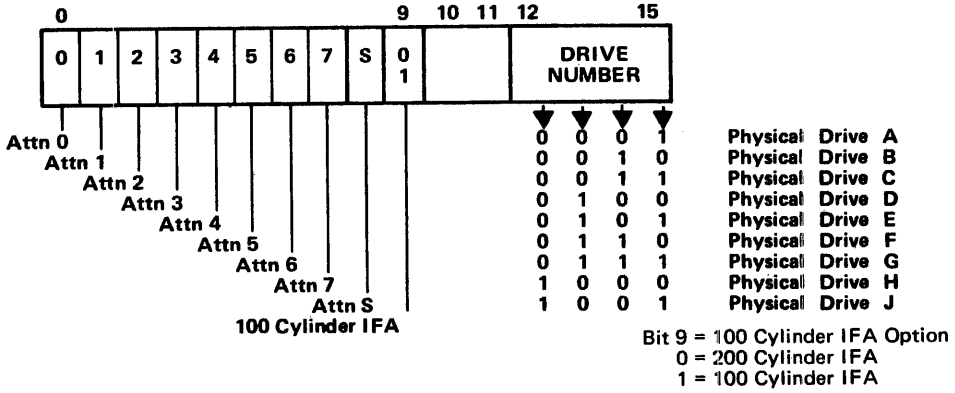


Figure 9-9. Control Commands



Bit	Meaning
0	IFA Status Not Valid or Command Early
1	IFA Missed Window or Command Early
2	IFA Window
3	IFA Track Boundary
4	IFA Read/Write Termination
5	IFA Burst Check Error
6	IFA Lost Data
7	IFA No Sync Compare
8	IFA 3rd Rev Sync Find
9	Disc Not On Line or Seek Incomplete and Not File Unsafe
10	Disc File Unsafe or Seek Incomplete and Not File Unsafe
11	Disc Read Only
12	Disc Pack Change
13	Disc End of Cylinder
14	Disc Write Current Sense
15	Disc Busy

Figure 9-10. Write Hardware Status Command



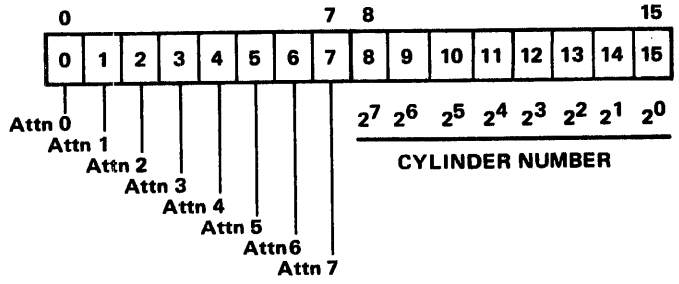


Figure 9-11. Write Other Status Command

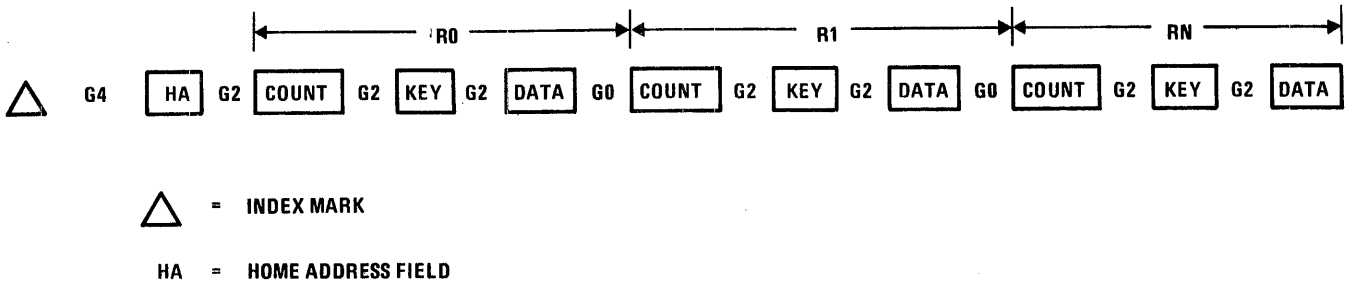
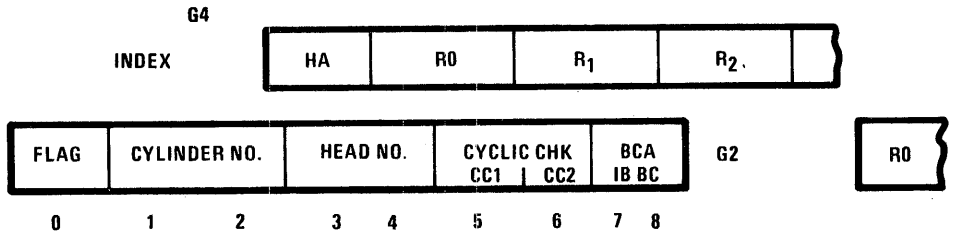
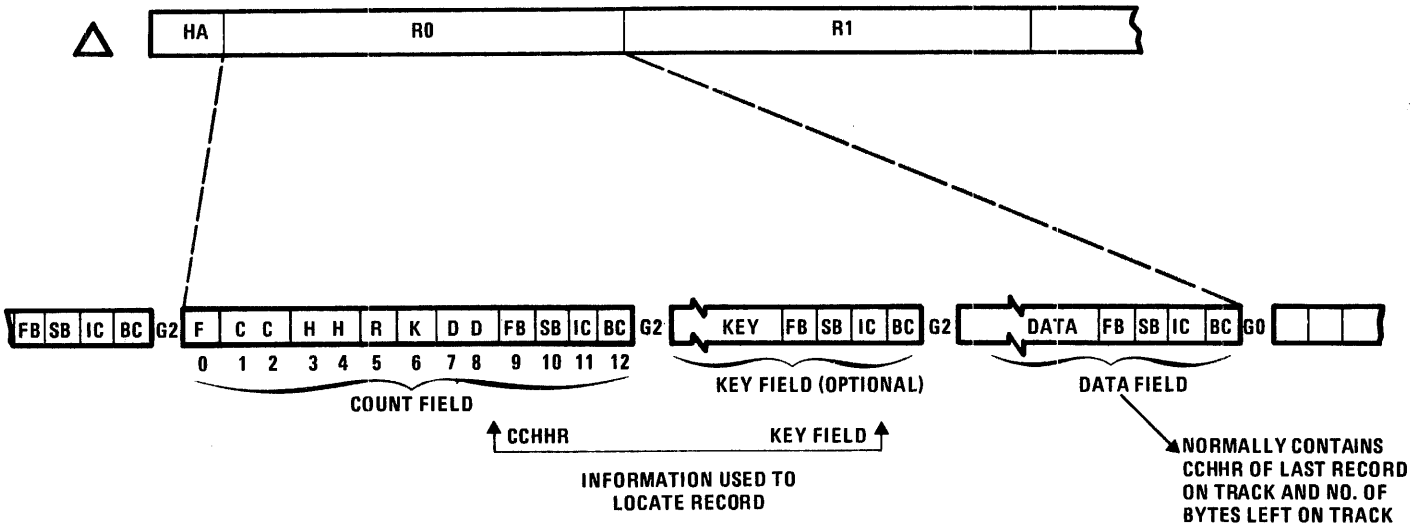


Figure 9-12. Track Format



FLAG (F)	1 BYTE	INDICATES TRACK CONDITION. BITS 0-5 ALWAYS ZERO. BIT 6 INDICATES TRACK CONDITION, 0=OPERATIVE, 1=DEFECTIVE,BIT 7 INDICATES TRACK USE 0=PRIMARY, 1=SECONDARY.
CYLINDER (C)	2 BYTES	CONTAIN CYLINDER ADDRESS OF TRACK. FIRST BYTE ALWAYS ZERO.
HEAD (H)	2 BYTES	CONTAIN HEAD ADDRESS OF TRACK (00-19). FIRST BYTE ALWAYS ZERO.
CYCLIC CHECKS	2 BYTES	CONTAINS RESIDUAL COUNT OF COMPLEMENTED EXCLUSIVE OR OF ALL DATA BITS IN THE FIELD (DOES NOT INCLUDE BRS).
INDICATOR BYTE (IB)	1 BYTE	ALWAYS SET TO ZERO.
BIT COUNT (BC)	1 BYTE	CONTAINS COMPLEMENT OF RESIDUAL COUNT OF ALL ONE BITS IN THE FIELD. INCLUDED ARE BITS IN THE SYNC BYTE, DATA FIELD AND FIRST CYCLIC CODE CHECK BYTE.

Figure 9-13. Home Address



F	=	FLAG	1 BYTE	
CC	=	CYLINDER NUMBER**	2 BYTES	
HH	=	HEAD NUMBER**	2 BYTES	
R	=	TRACK RECORD NUMBER	1 BYTE	– INDICATES SEQUENTIAL NUMBER OF RECORD ON THE TRACK
K	=	KEY FIELD LENGTH	1 BYTE	– DOES NOT INCLUDE BURST CHECK BYTES
DD	=	DATA FIELD LENGTH	2 BYTES	– DOES NOT INCLUDE BURST CHECK BYTES
FB	=	FIRST BYTE OF CYCLIC CODE	1 BYTE	BURST CHECK
SB	=	SECOND BYTE OF CYCLIC CODE	1 BYTE	
IC	=	INDICATOR BYTE*	1 BYTE	
BC	=	BIT COUNT BYTE	1 BYTE	

* IC ALWAYS SET TO ZERO
** FIRST BYTE ALWAYS SET TO ZERO

R0 – RN COUNT FIELD FLAG BYTE

BIT 0 AM DETECTION – ALWAYS ZERO IN R0, ALTERNATES ZERO TO ONE IN SUBSEQUENT RECORDS
BITS 1-5 ALWAYS ZERO
BIT 6 TRACK CONDITION
0 = OPERATIVE
1 = DEFECTIVE
BIT 7 TRACK USE
0 = PRIMARY
1 = SECONDARY

Figure 9-14. Record Zero

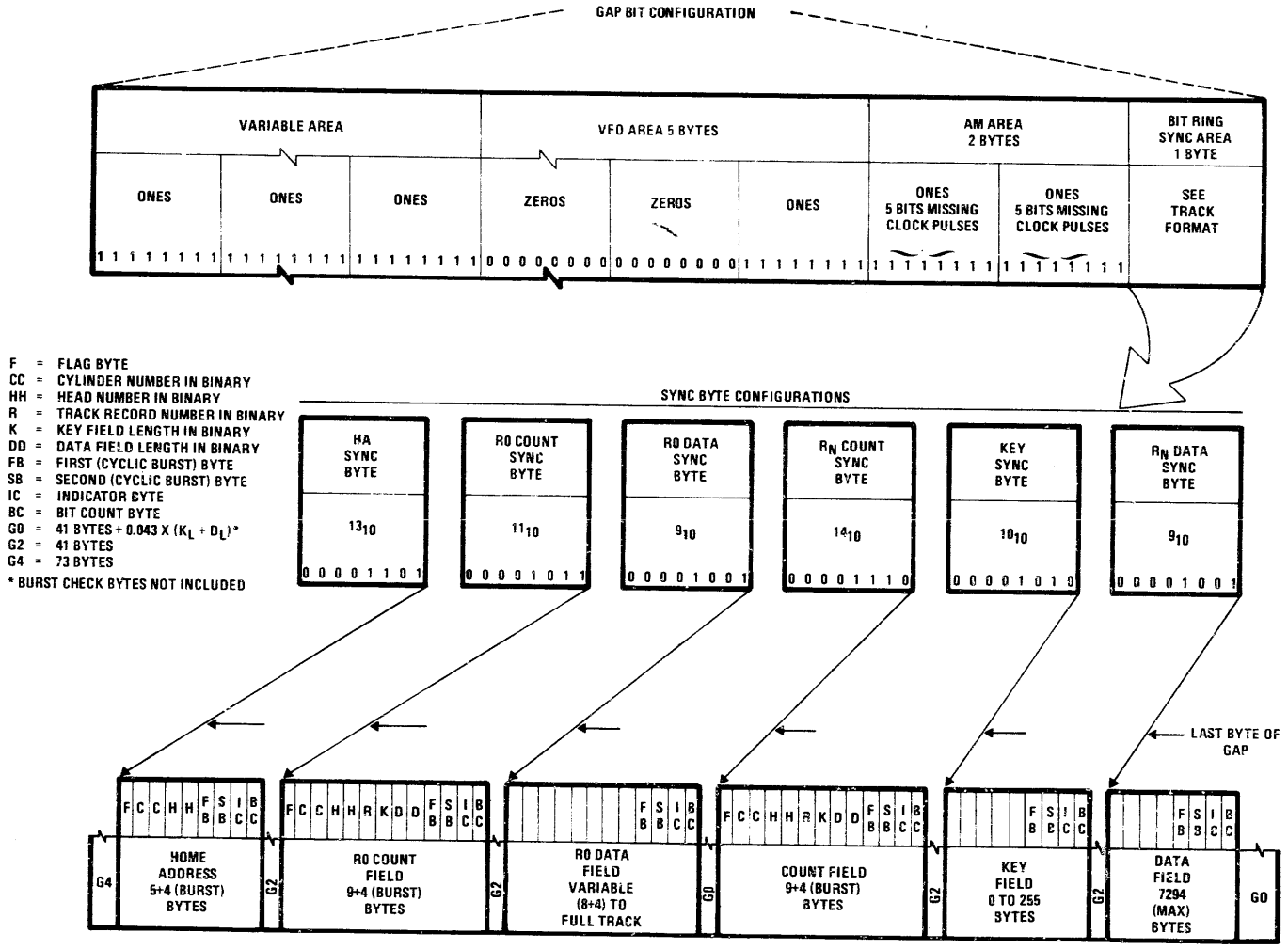


Figure 9-15. Gaps

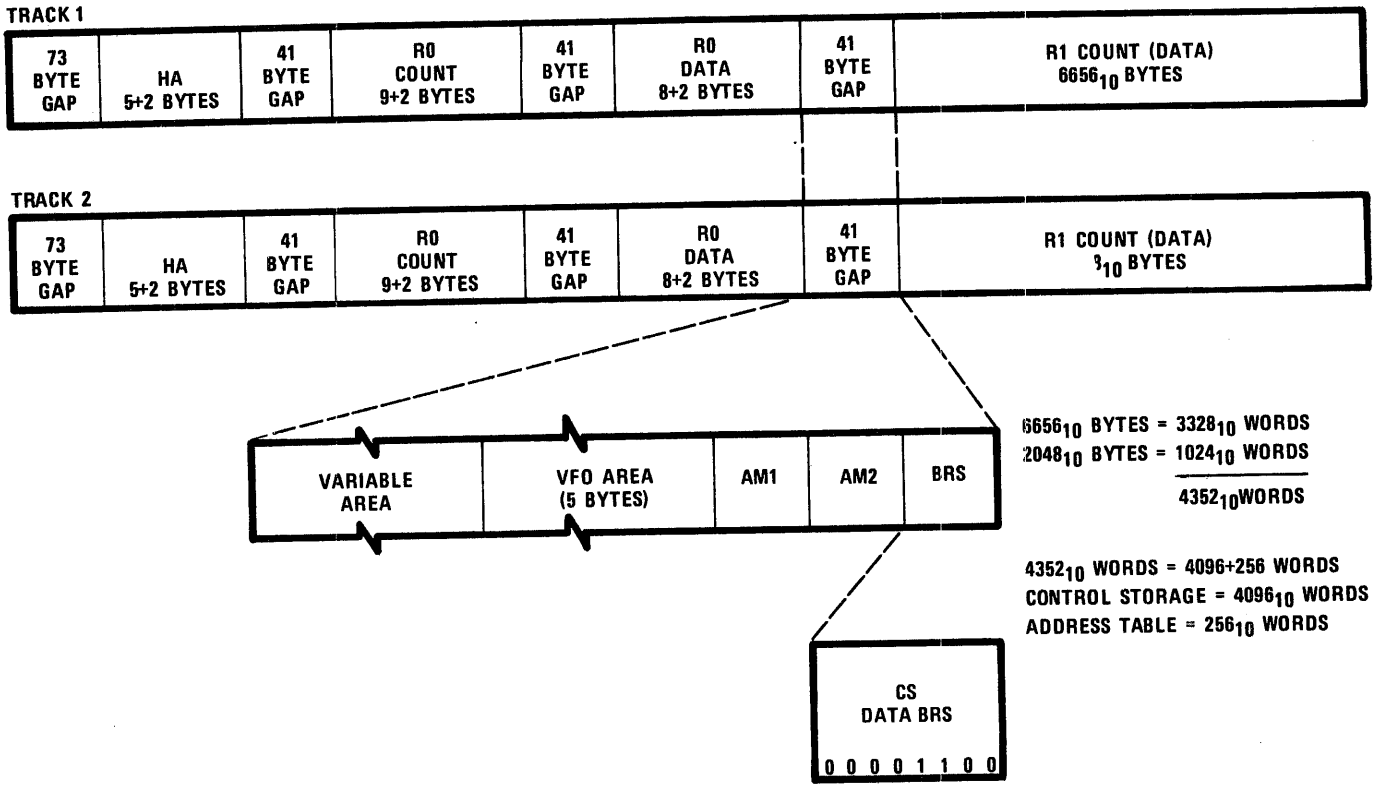


Figure 9-16. Special Track Format for CS Load - Drive

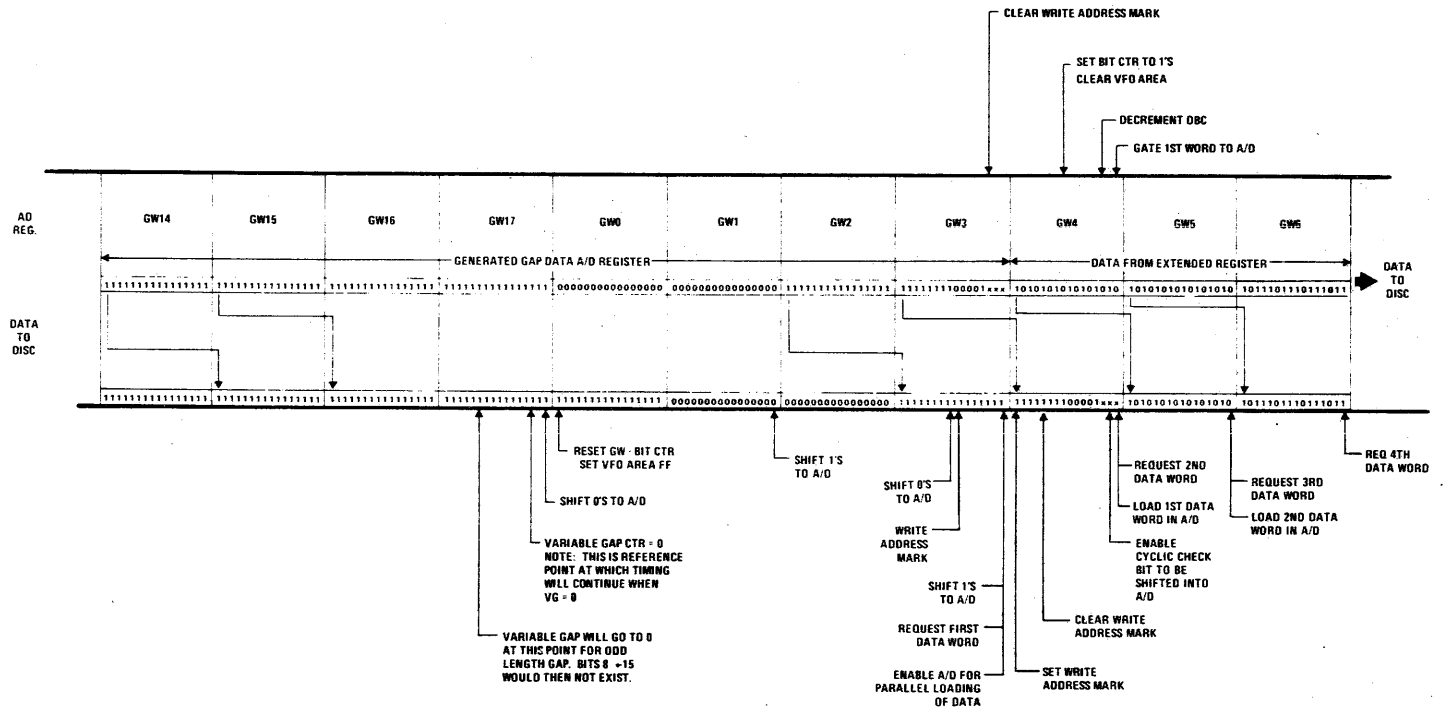


Figure 9-17. Write Timing 1

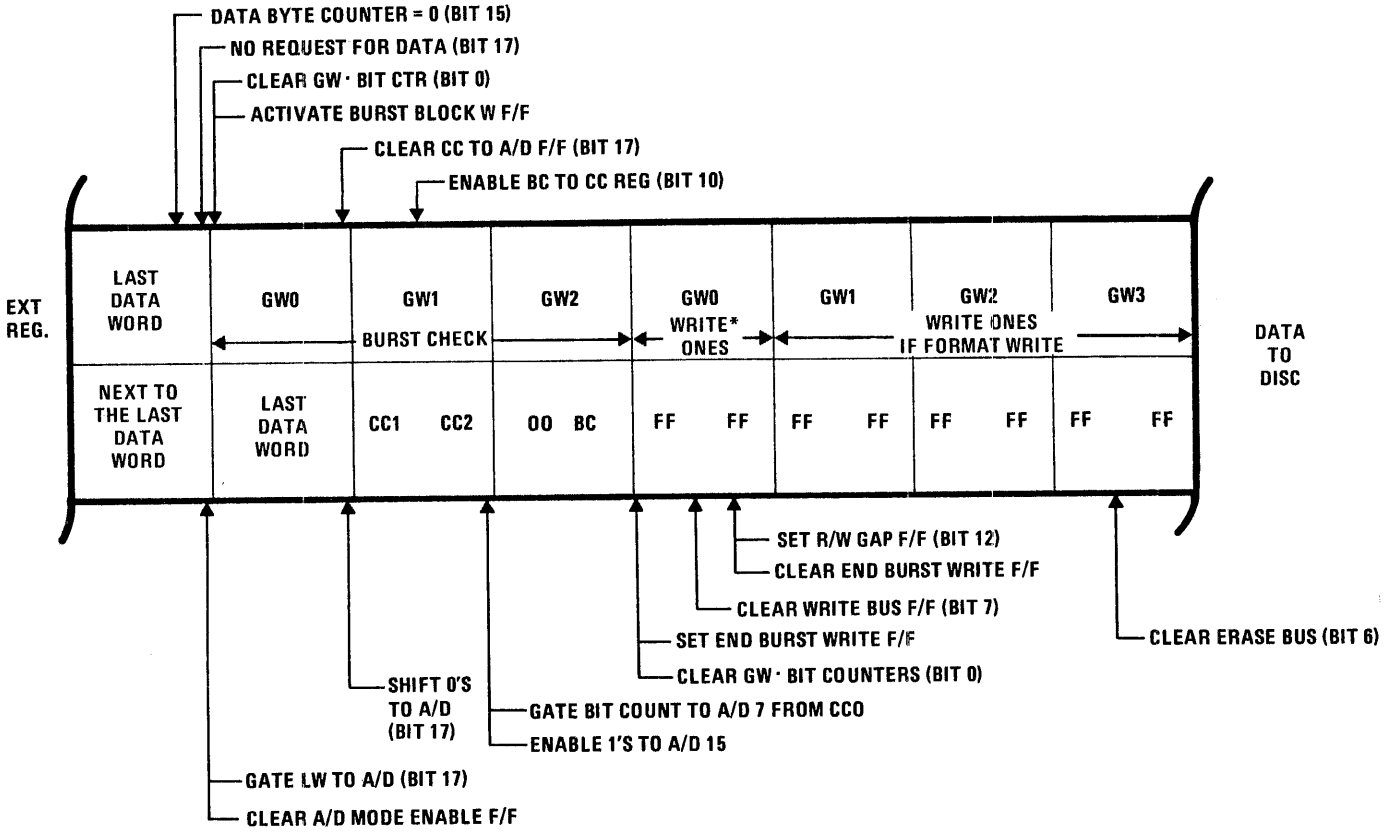
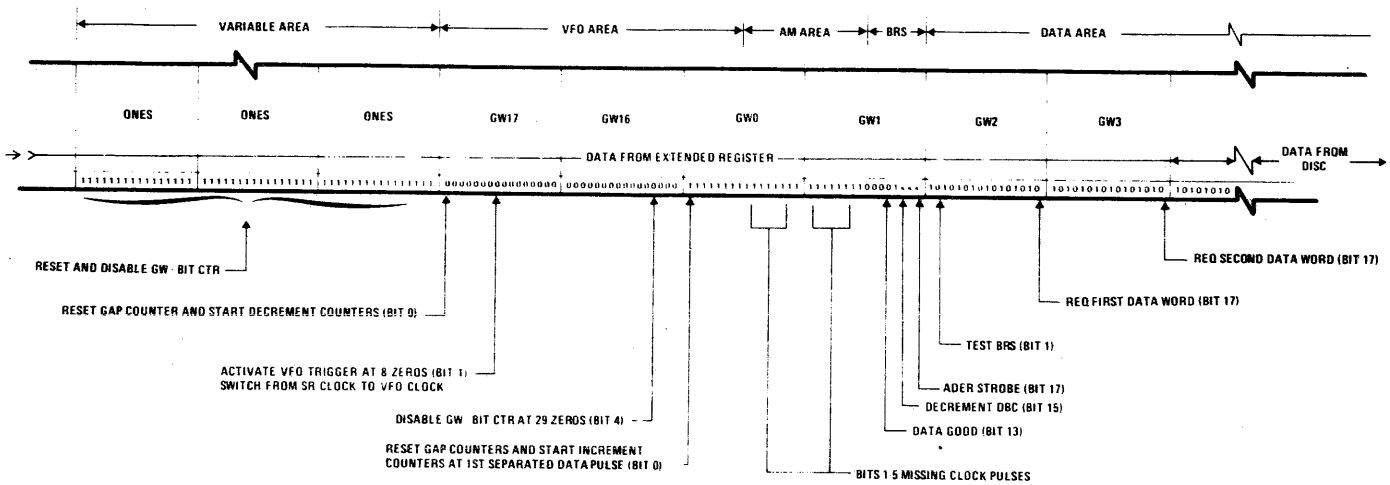


Figure 9-18. Write Timing 2



VARIABLE AREA BYTE COUNT

G4: 65 BYTES (NORMAL), 197 BYTES (HA ERROR)
G2: 33 BYTES
G0: 33 BYTES + 0.043 $(K_L + O_L)$ - 8 BYTES

GW16/GW17 BIT SEQUENCE - 0, 17, 16, 15, 14, 13, 12, 11
10, 7, 6, 5, 4, 3, 2, 1

NORMAL BIT SEQUENCE - 0, 1, 2, 3, 4, 5, 6, 7, 10, 11,
12, 13, 14, 15, 16, 17

Figure 9-19. Read Timing

SECTION 10. POWER SUPPLY SYSTEM

This section consists of troubleshooting checks and adjustments to restore power supply system to proper operating condition.

CAUTION

Use extreme caution when servicing any portion of the Power System. Lethal voltages (up to 450 VRMS) exist in some areas. In addition, extremely high current capacity exists in many areas.

Always follow these rules for your personal safety:

1. Remove all rings, watches, cuff links and all other metallic items from your arms.
2. When possible, work with only one hand.
3. Work with power off and/or the system unplugged whenever possible.
4. When the system is unplugged for servicing, tag the plug so that someone else won't plug it in.
5. When working in hazardous areas, do not work alone.
6. Keep safety covers on at all times, except when actually working in the protected area.
7. If safety devices must be bypassed, use extreme caution, and be sure to restore them to normal.
8. Electrical burns are deep. Get medical attention immediately.

TROUBLESHOOTING

FUSE CHECKS

Check for blown fuses in accordance with Table 10-1. Use applicable columns of this table, depending on version of power supply system.

TABLE 10-1. FUSE CHART

REF. DES.	VER. 4		VER. 5 50 HZ		VER. 5 60 HZ	
	RATING	MRX P/N	RATING	MRX P/N	RATING	MRX P/N
AC Switch Assembly						
F2A	6 AMP	501859	10 AMP	501860	6 AMP	501859
F2B	6 AMP	501859	*	*	6 AMP	501859
F9A	15 AMP	501861	15 AMP	501861	15 AMP	501861
F9B	15 AMP	501861	15 AMP	501861	15 AMP	501861
F9C	15 AMP	501861	15 AMP	501861	15 AMP	501861
F8A	10 AMP	501860	*	*	*	*
F8B	10 AMP	501860	*	*	*	*
F8C	10 AMP	501860	*	*	*	*
F10A	20 AMP	501862	20 AMP	501862	20 AMP	501862
F10B	20 AMP	501862	20 AMP	501862	20 AMP	501862
F10C	20 AMP	501862	20 AMP	501862	20 AMP	501862
F3A	10 AMP	501860	*	*	10 AMP	501860
F3B	10 AMP	501860	*	*	10 AMP	501860
F3C	*	*	*	*	*	*
F5	6 AMP	501859	6 AMP	501859	6 AMP	501859
F6	6 AMP	501859	6 AMP	501859	6 AMP	501859
F7	3 AMP	501858	3 AMP	501858	3 AMP	501858
AC Power Distribution						
F1A	50 AMP	501864	*	*	*	*
F1B	50 AMP	501864	*	*	*	*
F1C	50 AMP	501864	*	*	*	*
F4A	30 AMP	501868	20 AMP	501862	35 AMP	501865
F4B	30 AMP	501868	20 AMP	501862	35 AMP	501865
F4C	30 AMP	501868	20 AMP	501862	35 AMP	501865

*not used

VOLTAGE CHECKS

1. Check for presence of all voltages using DEVIATION METER on System Control Panel. The +24 VDC may be so low as not to indicate, also the +28 VDC. All other voltages selected should give a reading. Any voltage missing indicates fault in meter circuit or failure of sequences. (Module 3F03 should detect the missing voltage and cause the PROC FAULT lamp to light, the alarm to sound, and the system to power down.)

2. Connect meter between bus 1 (reg +11V) and DC COMM bus (ground) with meter on 12 VDC range. Meter should indicate 8-10 VDC.

SEQUENCER RELAY CHECKS

Make a visual check of all power sequencer relays for proper energizing sequence as follows.

Version 4 Processing Units

Relays are located on the power sequencer assembly and energize in the following order: K1, K2-K3-K4, K6, K7, K8-K9, K14, K15, K26, K10-K11, K12, K13, K16, K17, K18, K19, K20, K21, K22, K23, K24, and K25. Relay K5 is energized if the POWER MODE switch is set to REMOTE and de-energized if set to LOCAL.

Version 5 Processing Units

Relays are located on power sequencer modules JV, JW, and JY, and energize in the following order: K1, K2-K3-K4, K6, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, K20, K21, K22, K23, K24, K25, and K26. Relay K5 is energized if the POWER MODE switch is set to REMOTE and de-energized if set to LOCAL.

PHASE-LOCK MODULE SCR FIRING CHECKS

Connect meter between bus 1 (reg +11V) and DC COMM bus (ground). Turn power on and observe that the voltage rises slowly to its maximum value. This indicates that the "soft turn-on" of the SCR's is functioning properly.

ALARM CIRCUIT CHECK

Block holes in airflow sensor. After a few seconds the alarm should sound and the OVERTEMP light on the Panel should come on. Allow machine to complete power-off sequence and time the delay. Delay should be 60 seconds if current limit is present (or 30 seconds if no current limit). If necessary, adjust for correct delay by means of potentiometer on module 3F03.

ADJUSTMENTS

OVERVOLTAGE THRESHOLD ADJUSTMENTS

Initial Conditions

Before making any of the overvoltage adjustments described below, perform the following steps:

1. Check that all EPO sockets are jumpered with plugs wired: 1-2, 3-4, 5-6 (J16 to J23, J26 and J27).
2. Insert a jumper between pins U and V of disc-drive multiplex connector J15.
3. Connect jumper between 3F03-43 and 3F03-44. This prevents the machine powering off after 60 seconds upon detection of an overvoltage condition.

An adjustment table containing location of adjustment pots and voltage settings is included in drawing 504468, Adjustment Table, in the Support Diagrams Manual.

+23 VDC Threshold Adjustment

1. Turn power off to system and remove wires from 3D04-UL, UR, LL, and LR (+12, -12, +23, and +19V shunts). Tape the ends to prevent short circuits.

2. Mount a 25-ohm, 25-watt resistor onto the DC common bus by clamping one end in good electrical contact with the bus bar. (Suitable screw holes will be found in the bus below chassis 3.) Connect the free end of the resistor to 3D02-LL using a lead and crocodile clips.

3. Connect a DVM between ground and 3D02-UL to monitor output voltage. Connect another meter (50 VDC scale) across the 25-ohm resistor.

4. Turn power on to the system. Using the MAIN STORAGE adjust pot on the System Control Panel, increase the voltage to the overvoltage limit (25.4 volts) as measured by the DVM. When the limit is reached, the OV shunt circuit should turn on, indicated by a reading of approximately 25 volts appearing on the meter across the shunt. If the setting is correct, return the output voltage to its correct value (23.3V). The OV shunt should turn off, indicated by the shunt meter reading zero. (It may be necessary to bring the output voltage to below its correct value to reset the shunt, or even to power the machine off and on again.) Then return the output to nominal and proceed to the +19VDC Threshold Adjust procedure. If the setting is not correct (too low or too high) proceed to step 5.

5. Turn potentiometer 3D03 No. 1 (top pot) fully clockwise to desensitize the OV detect circuit. Then increase the output voltage to 25.4 volts using the MAIN STORAGE adjust pot. If this does not allow sufficient adjustment, turn pot 3F02 No. 3 clockwise to raise output voltage V(out). Then turn the overvoltage limit pot (3D03 No. 1) counterclockwise until the shunt meter deflects (about 25 VDC), indicating the shunt has turned on. Check setting by returning V(out) to nominal, or reducing it sufficiently to turn the OV shunt off. Then raise V(out) again and check that the OV shunt turns on at 25.4 volts. Readjust if necessary.

+19 VDC Threshold Adjustment

1. Turn power off to the system and move the shunt resistor lead from 3D02-LL to 3D02-LR. Also move DVM lead from 3D02-UL to 3D02-UR.

2. Turn power on to system and increase V(out) from 19.8 to 21.9 volts using the MAIN STORAGE adjust pot and, if necessary, by

turning pot 3F02 No. 4 clockwise. The overvoltage shunt should turn on at 21.9 volts, indicated by the shunt meter. If the setting is incorrect, proceed to step 3.

3. Turn the OV limit pot (3D03 No. 2) fully clockwise. Set the output voltage to the OV limit (21.9V) using the MAIN STORAGE adjust and 3F02 No. 4. Now turn 3D03 No. 2 counterclockwise until the OV turns on, indicated by a reading of approximately 21.9 volts appearing on the shunt meter. Check the setting using step 2 above.

4. Finally, disconnect the shunt resistor and turn the MAIN STORAGE adjust pot fully clockwise for maximum output. Then, using pot 3F02 No. 4, set the 19 VDC supply output to 21 volts. Return the 19V output to nominal (19.8 volts) using the MAIN STORAGE adjust pot, and check that the deviation meter reads zero. (If not, adjust pot No. 5 on VMTR-BD, shown on drawing 506081, Console Maintenance Group of the Support Diagrams Manual.) Then monitor the 23V output by putting the DVM lead onto 3D02-UL and adjust V(out) to nominal (23.3V) using pot 3F02-3. (This procedure insures that the storage supplies cannot be raised above the OV limit by the MAIN STORAGE adjust pot.)

5. Replace the +12, -12, +23, and +19 VDC shunts.

+5 VDC A Threshold Adjustment

1. Turn power off to the system and remove bus 4 (+5V A and B overvoltage shunt) connecting 3C04-LL/LR through 3C07-LL/LR to ground.

2. Connect the shunt resistor lead to 3C07-LR and the DVM lead to 3C07-UR.

3. Turn power on to the system and increase V(out) to 5.65 volts using LOGIC A adjust pot on the Panel and, if necessary, pot 3F07 No. 1. The overvoltage shunt should turn on at 5.65 volts, indicated by a reading of approximately 5 VDC on the shunt meter (change scale if necessary).

4. If adjustment is necessary, turn 3E07 No. 1 fully clockwise, set V(out) to 5.65 volts, and turn 3E07 No. 1 counterclockwise until OV turns on. Then repeat step 3.

+5 VDC B Threshold Adjustment

1. Follow the same basic procedure as for +5 VDC A above. Connect the shunt resistor to 3C05-LR and the DVM lead to 3C05-UR. Adjust V(out) to 5.65 volts using LOGIC B adjust pot and the 3F07 No. 2 pot, if necessary. If overvoltage adjustment is necessary, use pot 3E07 No. 2 to make the adjustment, as described in step 3 above.

2. Finally, disconnect shunt resistor and turn LOGIC A and LOGIC B adjust pots fully clockwise. Monitor 5 VDC A voltage and set to 5.5 volts using 3F07 No. 1, then return it to 5.0 volts with the LOGIC A pot. Monitor 5 VDC B voltage and set to 5.5 volts using 3F07 No. 2, then return it to 5.00 volts with LOGIC B pot. (This insures that the 5 VDC A and B supplies cannot be put into the overvoltage condition from the panel.)

3. Replace the +5 VDC A and B shunt.

-12, -5, -3, +3, +5, and +12 VDC Threshold Adjustments

1. Turn power off to the system and remove bus 8 (-5V and -3V shunt) from 3E05-UR and 3E06-UR and bus 9 (+5V and +3V shunt) from 3E05-LL and 3E06-LL.

2. Adjust the -12 VDC on threshold by connecting shunt resistor lead to 3C03-UR and DVM lead to 3C03-LR (Table 10-2). Turn power back on and turn pot 3F04 No. 1 clockwise to bring V(out) to -13.4 volts. At this point, the OV shunt should turn on, indicated by the shunt meter reading approximately -13V (reverse polarity and adjust range).

3. If adjustment is required, turn OV limit pot 3D05 No. 2 fully clockwise, then set V(out) to -13.4 volts using 3F04 No. 1. Turn 3D05 No. 2 counterclockwise until the OV turns on. Return V(out) to nominal -12V, then check using step 2. Finally, set V(out) to -12 volts.

4. Adjust the OV threshold for the remaining supplies using the procedure described in steps 2 and 3 above. Use the voltages and locations given in Table 10-2 for all adjustments. Note that +3V tracks off of (i.e., regulates from) -3V; therefore, -3V should be adjusted first. Also note that pot No. 1 on 3F05 may not be physically present; therefore, the top pot is No. 2.

5. Replace the shunts removed in Step 1.

TABLE 10-2. THRESHOLD ADJUSTMENT DATA

SUPPLY NAME = V(OUT)	CONNECT D.V.M. (V OUT)	CONNECT SHUNT RESISTOR	V(OUT) ADJUST POT	O.V. ADJUST POT	O.V. LIMIT (VOLTS)
-12V	3C03-LR	3C03-UR	3F04 No. 3	3D05 No. 2	-13.4
-5V	3E05-LR	3E05-UR	3F05 No. 3	3E05 No. 2	-5.65
-3V	3E06-LR	3E06-UR	3F04 No. 1	3E06 No. 2	-3.4
+3V	3E06-UL	3E06-LL	3F04 No. 7	3E06 No. 1	+3.4
+5V	3E05-UO	3E05-11	3F05 No. 2	3E05 No. 7	+5.3
+12V	3C03-UL	3C03-LL	3F04 No. 5	3D05 No. 7	+13.4

PHASE LOCK SCR FIRING ADJUSTMENTS

To set up the phase lock (P/L) amplifier which fires the SCR's in the bulk logic supply (REG +11) pre-regulator, proceed as follows:

1. With machine powered off (POWER OFF pushbutton set to OFF) but main breaker S1 turned on, connect a meter between TP1 and TP2 of the P/L amplifier module. It should read 2.5V DC. If not, adjust the BIAS (top) potentiometer on the P/L module.

2. Press the POWER ON button. The voltage between TP1 and TP2 should rise slowly and settle in the range 3.5-3.8 volts.

3. Now connect a moving-coil meter (not a DVM), using 10V DC scale, between bus 1 and DC common bus to monitor the REG +11 voltage. The voltage should be 8-10 volts. If not, adjust it to 8.5 volts with the OV (second) potentiometer on the P/L module.

4. Using 5V per division scale, 5 mV per division time base, and sync internal normal, scope the heat sinks of CR2 through CR7 in the logic bulk supply. The waveforms should be similar to that shown in Figure 10-1. In a perfectly adjusted system, the waveforms for all SCR's should be identical; i.e., the dx for all SCR's for both positive and negative halves of the cycle should be the same. If they are not, adjust in accordance with steps a and b on the following page.

a. Achieving the waveform shown in Figure 10-1 for the three pairs of SCR's depends on two interrelated adjustments: (1) making dx as close as possible for the three pairs of SCR's and (2) keeping dx as small as possible for stable firing. Making dx the same for all three pairs of SCR's is necessary to insure that all turn on to the same degree so that all supply an equal amount of current to the load. Adjustment of dx is provided by three phase adjust pots on the P/L module:

1) Phase A pot (No. 3) controls CR6 and CR7

2) Phase B pot (No. 4) controls CR4 and CR5

3) Phase C pot (No. 5) controls CR2 and CR3

If any one pair turns on harder (larger amount of dx) than the other two, turn its associated phase adjust pot counterclockwise. After reducing dx a little, scope the other two phases, whose dx's should have increased slightly. If two phases are now the same but the third is not turning on as hard, turn the phase adjust for that phase clockwise to make all three phases equal. By this means, it is possible to "balance" the SCR's. (However, any imbalance between two SCR's on the same phase, between the positive and negative halves of the cycle, cannot be cured since there is no adjustment provided.)

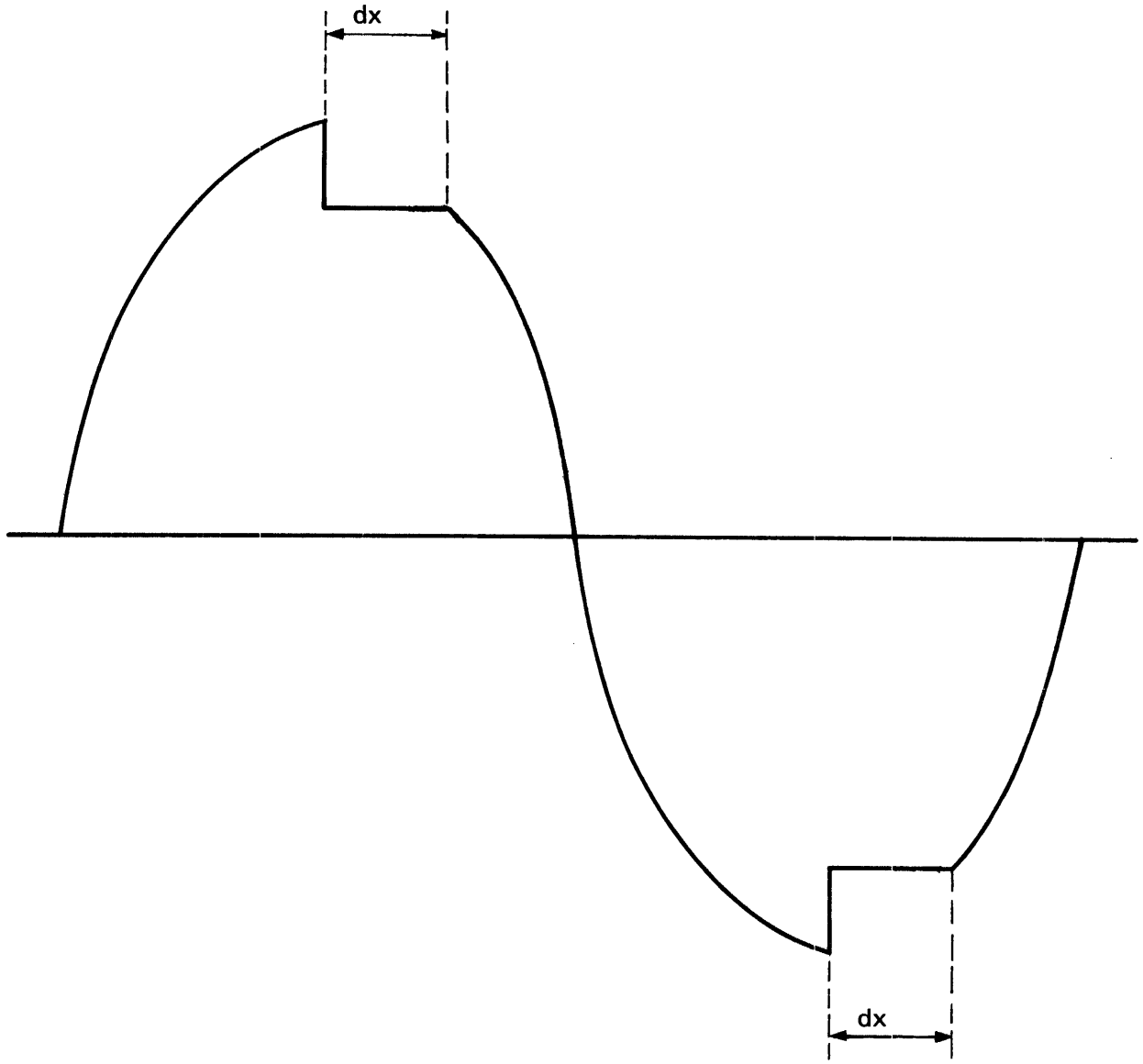


Figure 10-1. Phase Lock SCR Waveform

SECTION 11. SYSTEM CONTROL PANEL

Difficulties associated with the System Control Panel and associated Panel logic may be isolated by the procedures below. If necessary, refer to Section 3 of this manual for a functional description of all controls and indicators.

PANEL CONTROLS CHECK

1. Insure the proper operation of the following:

   a. CONSOLE ADDRESS and CONSOLE DATA REGISTER DISPLAY pushbuttons and indicators

   b. CLEAR ADDRESS, CLEAR DATA, and SYSTEM RESET pushbuttons

   c. CONSOLE ADDRESS and CONSOLE DATA REGISTER SELECT selectors

2. Set the Console Data register selector to Au and press the SET Au pushbutton. All the bits in the Console Data register should set.

3. Set the Console Data Register selector to Bu and press the SET Bu pushbutton. All the bits in the Console Data register should set. De-select the SET Au and SET Bu pushbuttons.

4. Set the Console Data Register selector to SUM. With all the bits in both Au and Bu set, the sum should equal FFFE (negative 2).

5. Set the Console Data register selector to D and press the SET Au and SET Bu pushbuttons at the same time. All the bits in the Console Data register should set.

6. Insure that the real time clock increments once every 16.6 milliseconds or once every 1.6 milliseconds, depending on whether a slow or fast real time clock is installed.

7. Start processors.

   a. Place all eight PROCESSOR CONTROL SELECT switches in the NORMAL position.

b. Press the PROCESSOR RUN button each time as the PROCESSOR SELECT switch is positioned in sequence from 0 through 7. The corresponding state lights should turn on.

c. Observe that the Busy/Active (B/A) register has an FF07 in it when all eight processor states are running.

8. Stop all eight processors by placing their PROCESSOR CONTROL SELECT switches in the STOP/STEP position. The Busy/Active register should now be cleared.

9. Place the CONSOLE MODE SELECT selector in the CS-WR position. This should select the Su and Console Data registers for display on the Console Address and Console Data register selectors.

10. Press the CONSOLE RUN button. Su should increment from 0000 through 0FFF, then jump to 4000 and increment to 40FF, and then jump to 1100. This holds true for each 4K increment of control storage and 256 words of address table.

RESOURCE ALLOCATION NETWORK CHECK

1. Extend module 1A16.

2. Insure that consecutive cycle mode is not enabled (CC bit of Control register not set).

3. Start processor 0 and check the state flip-flops with an oscilloscope to insure that the processor is running every other time slice.

4. Now start processor 1 and observe that each of the two processors is running during alternate time slices.

5. Start processor 2 and observe that all three processors are running an equal amount of time.

6. Start the remaining processors and insure that each processor gets to run an equal amount of time.

7. With all eight processors running, observe the B/A register. It should contain FF07. Stop all processors. The B/A register should be cleared.

8. Set the CS DISABLE switch to the up position.

CONTROL STORAGE AND ADDRESS TABLE LOAD CHECK

NOTE

Do not leave any AB modules on an extender for longer than 15 minutes, because the memory chips will overheat.

1. By doing a few control storage writes and then reading these locations, insure that the first few locations will hold all ones and also all zeros. (Bits 9 and 10 are not used.)

2. Write ones throughout control storage and then write zeros in every 256th location (every XXFF location). From location 4000 to location 40FF, write only bit 0 to a one.

3. Perform a CS scan operation. There should be no parity errors.

4. Write zeros throughout control storage and then write ones in every 256th location (every XXFF location). From location 4000 to location 40FF, write only bit 0 to a one.

5. Repeat step 3.

PANEL LAMP CHECK

1. Press LAMP TEST pushbutton. All Panel lamps should light and the alarm should sound.

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COMMENTS FORM

7200/7300 Processing Unit, Maintenance Manual – 2601.001-01

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