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MACROLINK INTELLIGENT DISK CONTROLLER
(MIDC)
PART NUMBER 202700
PRELIMINARY MANUAL

CONTAINS:

OVERVIEW
INSTALLATION SPECIFICATION
MIDC FAST FORMATTER
THEORY OF OPERATION
SCHEMATICS

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FOREWORD

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CHAPTER 1
OVERVIEW

1-1 DESCRIPTION OF AN MIDC DISK SYSTEM

The MACROLINK Intelligent Disk Controller (MIDC) provides Perkin-Elmer 3200 series and 7/32 - 8/32 processors with an SMD compatible high performance disk sub-system. The MIDC is fully compatible with the Perkin-Elmer IDC controller. Disk packs may be exchanged between the MIDC and IDC without any loss of data reliability. The MIDC disk system consists of the following:

(a) one to four disk drives (files) with industry standard SMD interface.

(b) and MIDC controller for interfacing these disk drives to the processor.

(c) a 20 foot 'A' and 'B' cable set for direct connection to the disk drive.

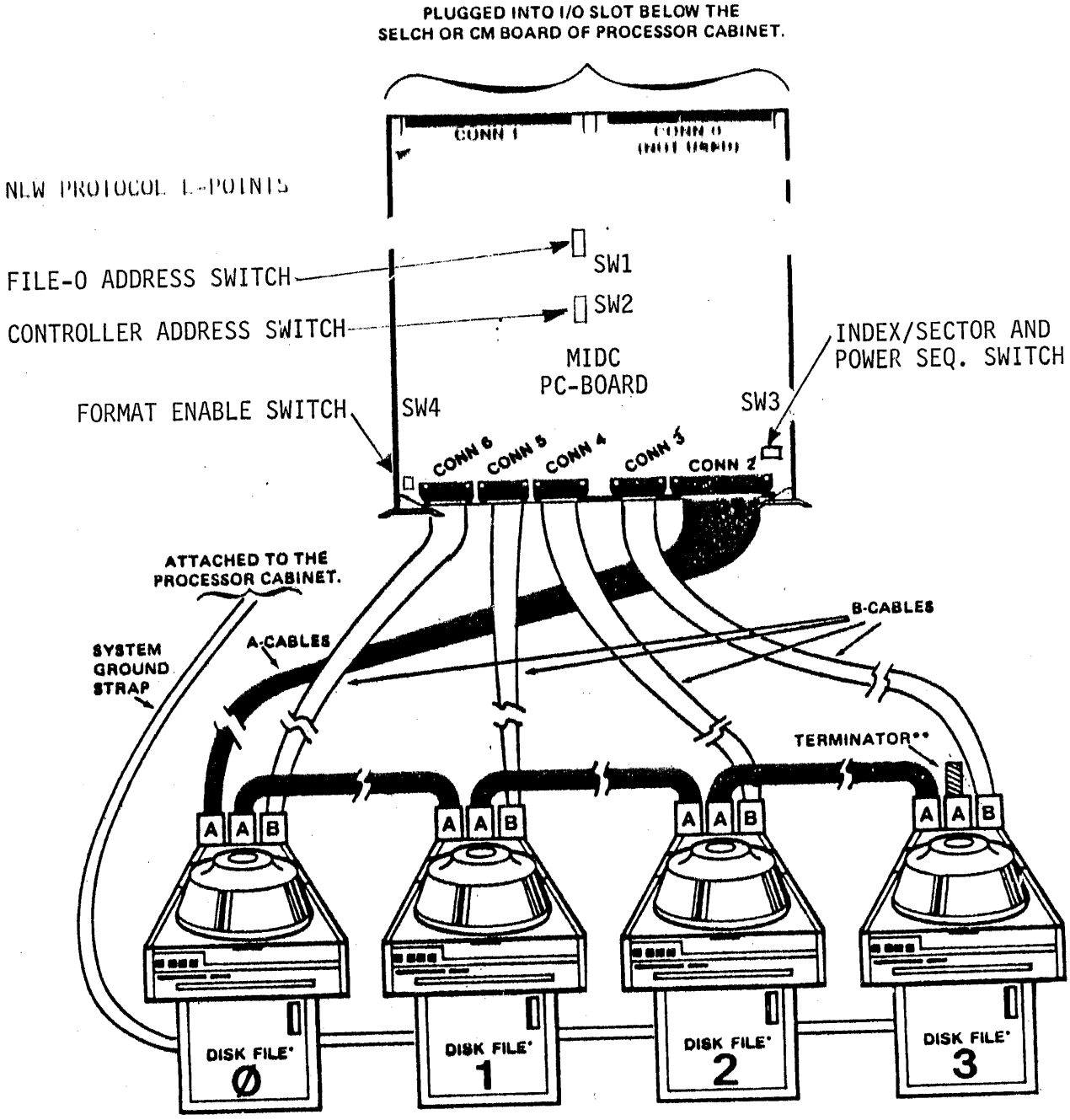
Figure 1-1 shows the MIDC PC-board. This board contains microprocessor logic for directly interfacing disk drives with P-E processors. Because of the high speed data transfers to and from the processor, a selector channel must be installed in the system. Either a 3200 Selector Channel (SELCH) or B-SELCH must be used. The MIDC has the capability of performing strobe-offset and track-offset sequences to recover data in the event of an error. It also has an automatic error-correction capability for correcting error bursts of up to 11 bits in length.

The MIDC can interface a maximum of four disk drives to the 3200 Series Processor, with overlapping seek and restore operations. These can be any size combination of standard SMD disk drives. For example, the drives interfaced may be a 80MB SMD, a 300MB SMD, a 160MB FSD and a 80MB CMD.

NOTE

The disk media of an MIDC system have a physical format that is different from and incompatible with the format of the MSM disk media. Some SMD disk drives allow installation of a dual-port option which permits two controllers to share a single disk drive. The MIDC cannot share a drive with an MSM controller.

Cabling from the MIDC board to the disk drives is direct with no interface panel between the controller and the disk drives.



* Jack numbers depend on the disk files configured.
** Last disk drive must have a terminator, as shown with the A-cable plug.

Figure 1-1. Basic MIDC Disk System

1-2 LIST OF RELATED PUBLICATIONS

Table 1-1 lists the Perkin-Elmer manuals related to the MIDC disk system.

Table 1-1. LIST OF RELATED PUBLICATIONS

PUBLICATION NUMBER	PERKIN-ELMER MANUAL
29-356	M48-018 Input/Output Bus Switch Manua|-Control Panel Installation Manual
29-727	Model 3200 Selector Channel (SELCH) Maintenance Manual
47-016	Channel Manager (CM)

1-3 PRODUCT SPECIFICATIONS

PHYSICAL

Dimensions:	Full board, 15 inches x 15 inches
Board Type:	Six-layer, glass epoxy
Weight:	2 1/2 lb. board (Shipping weight including 20 ft cables 7 lb.)
Mounting:	Horizontal rack, standard P-E

ELECTRICAL:

Power:	5VDC, at 8 Amps
Interface:	SMD standard using board edge mounted 3M connectors
Cable lengths:	Control cable "A" (daisy chain) - 100 ft maximum Data cable "B" (radial) - 50 ft maximum (Standard cable length supplied is 20 ft.)

ENVIRONMENTAL:

(Maximum ratings above which the useful life may be impaired)

Operating Temp.	0 C (32 F) to 50 C (122 F)
Storage Temp.	155 C (-76 F) to 85 C (185 F)
Vibration:	1.5 G at 5.5 Hz
Humidity:	95% relative, non-condensing

CHAPTER 2
INSTALLATION

2-1 INTRODUCTION

This chapter gives detailed parts lists and instructions for installing an MIDC disk system. Before reading this chapter, you should be familiar with Chapter 1.

2-2 PARTS LIST

MACROLINK PART NO.	DESCRIPTION
202700	MACROLINK Intelligent Disk Controller (MIDC) complete with "A" and "B" cables and installation manual
SMD-A-20	SMD Disk to Controller "A" cable, 20 ft.
SMD-B-20	SMD Disk to Controller "B" cable, 20 ft.
XXXXXX	Ground Strap, 20 ft.
XXXXXX	Macrolink MIDC Manual

2-3 UNPACKING INSTRUCTIONS

The MACROLINK Intelligent Disk Controller (MIDC) is normally shipped with one "A" control cable and one "B" data cable. It is packed in accordance with commercial packaging practices using an anti-static plastic bag and foam sponge to cushion the MIDC board during shipment.

Inspect the outside of the package for any signs that the contents may have been damaged. If the package has been damaged, make a record of the type and extent. If the MIDC or cables have been damaged during shipment, request that the carrier's agent inspect the damage and file a claim with the carrier. Usually, a claim must be filed within 7 days after receipt of a package.

Notify MACROLINK INC. 1150 East Stanford Court, Anaheim, CA 92805 of any discrepancies between invoice and received material or of any damage found during inspection.

2-4 INSTALLING AN MIDC DISK SYSTEM

Figure 1-1 is a general illustration of how to install the MIDC board into a processor chassis using standard SELCH protocol. If your processor configuration includes a Perkin-Elmer I/O Bus Switch, you must also refer to P-E publication #29-356 for the Bus Switch Installation Information. The "ALT PCTL" position of SW1-7 on the MIDC must also be set to "1" (OFF) to allow proper operation with the Bus Switch.

IMPORTANT - Prior to installing the MIDC Disk Controller in the processor, make sure that you set the two Address Switches and the Index Select Switch. Refer to the instructions on switch settings in the following paragraphs. Also, the SBSYO backplane jumper must be installed.

2-4.1 MIDC Switch Options

As seen in Figure 1-1, the MIDC has two address switches (SW1, SW2) in its upper center, an Index/Sec Select Switch in the lower-right corner (SW3) and a Format ON/OFF switch in the lower-left corner (SW4). The following sections explain how these switches should be set.

2-4.1.1 Controller Address Switch

As shown in Figure 2-1, the Controller Address Switch (SW2) has eight positions, numbered 1 thru 8, each with two possible settings: 0 or 1. A 0 setting corresponds to an ON setting of the switch position. Each position setting represents a bit in a 1-byte controller address, with position 1 being the most significant bit (MSB) and position 8 being the least significant bit (LSB). You must set the positions in this switch to the address wanted for your MIDC. See the following example:

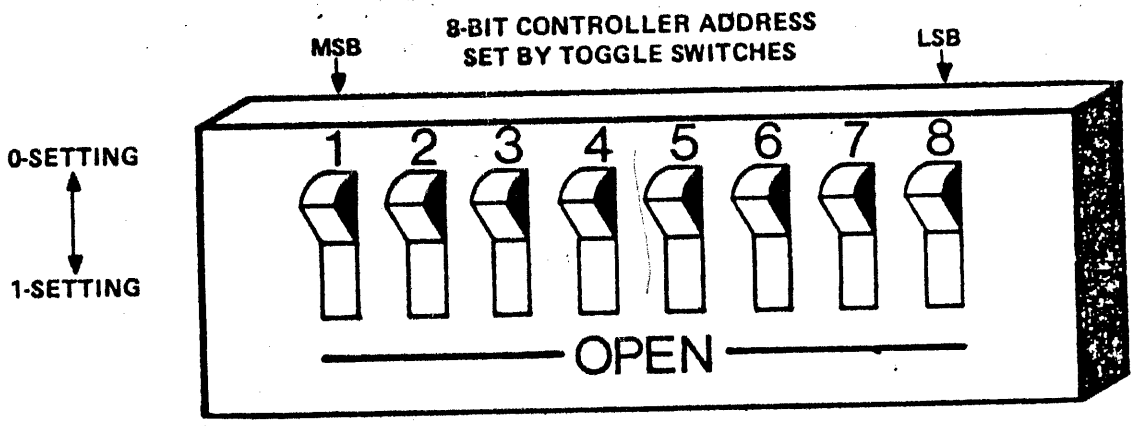


Figure 2-1 CONTROLLER ADDRESS SWITCH

2-4.1.2 File-0 Address Switch

As shown in Figure 2-2, the File-0 Address Switch (SW1) also has eight positions, numbered 1 thru 8, each with two possible settings: 0 or 1. Positions 1 thru 6 represent six bits in a 1-byte address for your disk file 0, with position-1 being the MSB. The other two bits of the 1-byte address are zero, and are not used for addressing. Position 7 is used to select the "new" high speed alternate SELCH protocol. Position 8 is not used.

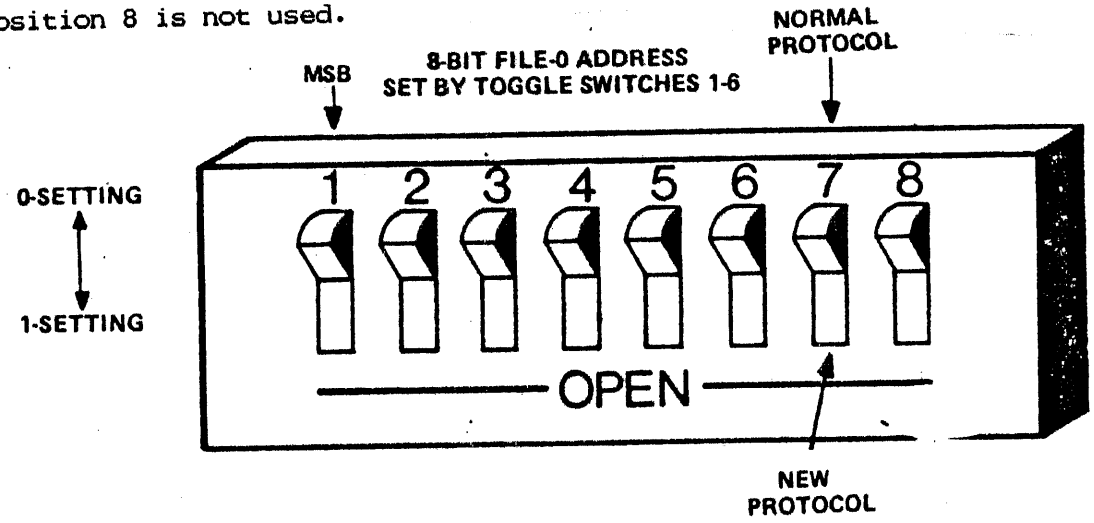


Figure 2-2. FILE-0 ADDRESS SWITCH

As an example for setting addresses on these switches, suppose you have an MIDC system consisting of one board and four disk files. You want the controller address to be X'FB' and the four disk file addresses to be X'FC' thru X'FF'. Before installing the MIDC board, you would set the Controller Address Switch to the binary value of 11111011 (for X'FB') and the file-0 Address Switch to 11111100 (for X'FC'). Disk files 1 thru 3 are automatically addressed at X'FD', X'FE'. X'FF', respectively.

Now with the desired addresses set on the two switches, you have the option of setting position-7 File-0 Address Switch. If you want to employ the normal SELCH protocol, push position-7 up to the 0-setting (ON). If your MIDC is plugged into the 25-foot cable of an I/O Bus Switch, you must push position-7 down tot he 1-setting, thereby employing the "new" high-speed SELCH protocol. For additional information on the I/O Bus Switch, refer to Perkin-Elmer Publication 29-356/ Also, as discussed in Section 2-4.2, the new protocol locations E2 and E4 should be strapped when an I/O Bus Switch is used.

2.4.1.3 Index/Sector Switch

For normal operation, positions 1-4 of SW3 should be set to the "OFF" position to allow the index and sector pulses from the drive to be selected from the "A" cable. If your drive is configured for "B" cable Index/Sector selection, the corresponding drive switch position should be set to the "ON" position to allow proper operation. SMD disk drives purchased from P-E are configured for "B" cable operation.

2.4.1.4 Power Sequencing Switch

The power sequencing switch is found at SW3 position 5. Power sequencing refers to the serial application of power to the disk files once the processor is turned on. If enabled, the first disk will spin up only after the CPU is on. Each additional disk will consecutively spin up. When you want your disk files to power-up sequentially, set SW3 position 5 "OFF". Also ensure that the Local/Remote Switch on each attached disk file is in the Remote position. Subsequently, when the processor is turned off, the disk files power down simultaneously. When SW3 position 5 is "ON" or when the Local/Remote Switch on each attached disk file is in the Local position, the disk files can be simultaneously powered up -- in parallel, as opposed to serial. The simultaneous application of power to the disk files may cause an excessive power surge. To determine the advisability of power sequencing, check your AC power requirements.

2.4.1.5 Format Enable Switch

The Format Enable Switch (SW4) should be OFF to prevent unintentional formatting. When a disk is being formatted, this switch must be ON. Formatting can only be accomplished by using an IDC formatter program, such as the P-E 06-268.

2-4.2 Alternate Protocol Strapping

As shown in Figures 1-1, the MIDC board has one strappable option. Locations E1, E2, E3, and E4 near IC location A24 are used to set the "new" high-speed SELCH protocol for special applications. When your MIDC is installed under an I/O Bus Switch, and when position-7 of the File-0 Address is in the 1-setting, you must strap locations E2 and E4, and cut E1 &E3. Although not normally required, locations E1 and E3 can be strapped for employing the high-speed protocol without the use of an I/O Bus Switch, as in the 3205. When installed in an 3205, the MIDC **MUST** be configured for alternate protocol (SW-7 ~~on~~ OFF).

2-4.3 Backplane Wiring

2-4.3.1 RACKO/TACKO Jumper Removal

On the Perkin-Elmer processor backplane, you must REMOVE the RACKO/TACKO wire wrap jumper between pins 122-1 and 222-1 at the slot location selected for the MIDC.

2-4.3.2 SBSYO Backplane Jumper

The chassis containing the B-SELCH or series 3200 SELCHMUST have a jumper from pin 224-1 of the Selector Channel slot to pin 224-1 of the MIDC slot. If a B-SELCH is used, the SBSYO signal on the B-SELCH must be strapped to the backplane pin 224-1 by joining pins E4-E5 (located near IC 147 of the B-SELCH). This signal is prewired on the 3205.V

224-1
224-1

2-4.4 Disk Drive Configuration

The disk file must be configured for 33 sectors. Refer to the disk drive manufacturer's manual for information on setting sectors.

2-4.5 7/32 - 8/32 Installation

The 7/32 and 8/32 CPU's may need to be modified to conform to the 3200 false sync time out of 30uS. On the 7/32 CPU A board, increase C86 to 2400 pF. The 8/32 IOU board can be modified by increasing the capacitor at 03E,3-14 from 1000pf to 1400pf. These changes will not affect the operation of the computer, but will allow for the increased processing time of some MIDC and IDC commands.

2-4.6 Interface Cables

See figure 1-1 for a typical cable arrangement. The cable-to-board connectors are of the 3M polarized type. The connector for the "A" cable has cable-locking clips that are engaged to retain the female 3M connector on the cable.

IMPORTANT - It is possible to engage an "A" type cable connector improperly if the cable is not the Macrolink supplied cable with the 3M female connector. If a non-3M connector is used on the "A" cable, insure that pin 1 on both cable and board connector are aligned properly before inserting cable into connector.

2-4.6.1 Single Disk Drive System

Install the "A" cable between the disk drive and the "A" cable connector on the MIDC board. If the cable has polarized 3M connectors, engage connector latches. If the cable has the optional cable connector design, ensure correct pin alignment before connecting the cable to the MIDC board connector. Ensure that the drive end of the "A" cable has a proper signal terminator installed. Refer to the disk drive manual supplied by the manufacturer for terminator information.

Install one "B" cable between disk drive and Drive 0 "B" connector on the MIDC board. Set the address selector of the drive to '0'. A ground cable should be connected between the frame of your disk drive and the Perkin-Elmer processor chassis

2-4.6.2 Multiple Disk Drive System

Install the "A" cable between your disk drive and the "A" cable connector on the MIDC board. If cable has the polarized 3M connector, engage connector latches. If cable has the optional cable connector design, ensure correct pin alignment before connecting the cable to the MIDC connector.

Install the "B" cables between each disk drive and its corresponding drive"B" connector (0-3) on the MIDC board, as determined by the disk drive (file) address sequence, the "B" cable connector choice must coincide with the disk drive address sequence (lowest address connected to drive 0 connector).

Install additional "A" cables between second disk drive and first disk drive. "Daisy Chain" any additional disk drives together and ensure the last disk drive in the chain has a signal cable terminator installed. For detailed installation procedures at the disk drive, refer to manual supplied by the SMD drive manufacturer

A grounding strap should be connected from disk drive to disk drive in daisy chain fashion. These connections should occur between frame grounds of each disk drive. The closest disk drive to the computer should have the ground strap connected to the Perkin-Elmer processor chassis.

2-5 INSTALLING DUAL-PORT OPTIONS

First be sure your disk drive system is equipped for dual-port operation. No special considerations or switch options need be made when installing the MIDC into a dual-port disk system. Please consult your specific drive manual for cabling and drive configuration information.

2-6 AC-POWER REQUIREMENTS

Be sure to plan in advance for the power requirements of the disk drive you have selected. Consider both current and voltage. Power requirements are found in the manufacturer's specifications and manual.

2-7 APPLICATION OF AC POWER

Depending on how you set SW3-5 ("ON for Local") on the MIDC board, you can apply power to the disk drives either simultaneously (in parallel) or sequentially (in serial). Section 2-7.1 describes simultaneous application of power, where SW3-5 is ON or the Local/Remote Switch of each disk file is in the Local position. Section 2-7.2 describes sequential application of power for a typical system, also referred to as power sequencing, where SW3-5 is off and the Local/Remote Switch of each disk file is in the Remote position.

2-7.1 Simultaneous Application of Power

In a typical disk system power may be applied simultaneously to the disk files by following this procedure:

1. Ensure all AC power input connections are correct.

2. At the front of each disk file, depress the START/STOP switch so it is unlit, i.e., so it is in the STOP position. Some fixed media drives don't have a START/STOP switch, and spin up upon application of primary power.

3. At disk file 0, the first drive in the MIDC system, set the AC Input-Power switch to the ON position. (At this time, a fixed media disk would start up.)

4. Depress the START/STOP switch so it is lit, i.e., so it is in the START position. This disk file should now start up. If the disk file does not start, make these additional checks:

   a. Ensure that the Remote/Local switch in the disk drive is set to the local position.

   b. Check AC Input power.

   c. Check fuses in the disk file.

5. At the next disk file installed on your system, set the AC Input-Power switch to the ON position. (At this time, a fixed-media disk would start up.)

6. Depress the START/STOP switch to the START position. This disk file should now start up. If it does not, make the same checks in step 6.

7. Repeat steps 7 and 8 for remaining disk files.

2-7.2 Power Sequencing

To apply power serially to the disk files attached to your controller, follow this procedure:

1. Ensure all AC power-input connections are correct.

2. In each disk drive, set the Remote/Local switch to the Remote position.

3. At the rear of each disk file, ensure that the AC Input-Power switch is in the ON position.

4. At the front of each disk file, depress the START/STOP switch to the START position. (This step applies only to removable-media disk files.)

5. Power-up the processor in which the controller is connected. The disk files now start-up sequentially, starting with disk file 0. When the processor is eventually turned off, the attached disk files simultaneously power down.

2-8 IDC TESTING AND FORMATTING

Once your MIDC system is installed and powered up, you can run the IDC Test Program to check for proper operation of your system. Follow this procedure:

1. Ensure you have an IDC-formatted media on your disk drive. If you do not, your disk must be formatted by loading and running the IDC Format Program, Part No. 06-268.

2. Load and run the IDC Test Program, Perkin-Elmer Part No. 06-267.

CHAPTER 3
MIDC FAST FORMATTER

3-1 GENERAL

The Macrolink Intelligent Disk Controller (MIDC) Fast Formatter, P/N 450201, performs pack analysis and header format of the disk pack or data module. Any errors found during the pack analysis phase will cause the corresponding sector to be flagged as defective. A list of all defective sectors is generated when the format process has completed. In addition, defective sector locations may be input directly to flag a specific sector as defective. This program will not function with the Perkin-Elmer IDC. However all P-E IDC tests and format programs will work with the MIDC.

3-2 REQUIREMENTS

The following is a list of the minimum hardware configuration required to run the formatter:

Macrolink MIDC P/N 202700 REV 3.0 or above microcode

32 bit CPU model 3200, 7/32 or 8/32

256KB memory

SELCH

SMD interface disk drive

Console device

List Device (may be console)

3-3 LOADING PROCEDURE

The MIDC Fast Format program is supplied in an OS image format. To load this program, mount the tape on a 1600 BPI tape drive and use the standard P-E IPL boot and respond as follows:

```
INPUT DEVICE=<TAPE UNIT>
FILEMARKS=0
```

After a short delay, the tape will be loaded into the system and started. **This tape cannot be loaded using MDL loader or X'50' sequence.**

The tape is generated with the following programs:

FAST FORMAT PROGRAM 450201 (OS IMAGE)
FM
IDC TEST 06-267 (OS IMAGE)
FM
IDC FORMAT 06-268 (OS IMAGE)
FM
FAST FORMAT PROGRAM 450201 (OBJECT)
FM

The IDC test can be loaded by entering '1' after FILEMARKS. The object format is for use with systems that do not have the standard 3200 series LSU boot loader. The user should copy the program into a suitable format for loading.

3-4 OPERATING PROCEDURE

1. Manually set the 'FORMAT' switch, locates on the left front of the MIDC to the 'ON' position. Place the drive on-line.

2. Enter options:

OPTION	FUNCTION	DEFAULT
SELCH	Selector Channel Address	X'F0'
DISCON	Disk Controller Address	X'FB'
DRIVE	Drive # 0 to 3	X'FFFF'
PACTYP	ID of Drive type and CE pack	X'CE00'
LOCYL	Low Cylinder Number	X'FFFF'
HICYL	High Cylinder Number	X'FFFF'

3. Type 'RUN' to start program execution.

The formatter will display the selected drive number, and sequence through the cylinders numbers for format, write, and read phases.

3-5 PROGRAM DESCRIPTION

3-5.1 Test 0

This test performs an initial status check of the SELCH, Disk Controller and File sections of the MIDC. If the status is correct, a Seek operation is performed to the LOCYL number. The header is written to Head 0, sector 0 of this cylinder along with an improper ECC halfword using the Write Format Command. A normal read date operation is performed and a Data Transfer Error should occur. The PRS is read and should be X'FE'. The final operation is a normal write format with the correct header and ECC character. Test 0 cannot be bypassed, and will terminate formatting if an error should occur.

3-5.2 Test 1

This portion of the diagnostic program performs the media certification and formatting. The modes are:

Pack Analysis
Format
Pack Data Write
Pack Data Read
Report Results

3-5.2.1 Pack Analysis

A halfword data pattern is written using the off-line write format command. A single halfword transfer from the SELCH to the disk controller is made. The controller uses this halfword to write a complete track. The contents of the RPS are read when the controller becomes idle, and should be zero. An off-line read is performed FMREAD times (from options), and indexes the offset table. On each pass, the RPS register is tested to ensure a full track has been read without error. When FMREAD has been reached, the data pattern is rotated one bit position, and the process is repeated. When SHIFT has been reached, the defective track table is examined for any entries. If any errors are set, the alternation routines are executed:

A single error will alternate the sector.

Multiple errors will cause the highest sector to be alternated and all other sectors to be flagged defective.

The entire pack is then written with the physical address of each sector. A final read phase reads and verifies no ECC errors, and proper sector address compares.

If any sectors have been flagged defective, a report is generated and sent to the list device.

3-6 FORMAT TIME

The basic format time of an 80MB drive (CDC RSD type) is 10 minutes. The write/read test adds an additional 3 minutes. The basic format time is increased by adding additional SHIFT and FMREAD options. FMREAD testing insures that all offset values will work on your pack and drive, and that media may be exchanged with other drives. Increasing the SHIFT option will test additional data patterns. With the default value of 2, all bit positions are tested for both 0 and 1.

FORMAT TIMES FOR 80MB CDC RSD

FMREAD	SHIFT	TOTAL TIME	
1	1	13 MINUTES	
1	2	16.5 MINUTES	(DEFAULT)
9	1	24 MINUTES	
9	8	123 MINUTES	

*These times are for error free packs.

3-7 OPTIONAL DRIVES

By selecting PACTYP B, the 5 optional table inputs are selected. Note that these are decimal values. The table has been preset for the Amcodyne Arapahoe 7110 drive. Non standard drives may be supported on OS/32 through DCB patches. The standard P-E diagnostic may indicate errors for configurations that are not supported. Macrolink will have a universal MIDC test program that can be configured for these drives in the future.

3-8 FLAW MAP

When the INFLAW flag is set to 1, the user is prompted at the start of the format to enter the map information that is supplied with most fixed-media drives. This flaw information is usually given as a decimal offset in bytes from the index. Divide this value by 600 to find the approximate physical sector number of the flaw, and enter the integer portion when prompted. If the format should be terminated and restarted, the flaw map information may be reused if desired. The user should note that the disk drive manufactures flaw map is generated using special analog test fixtures and represents the best indication of defective and marginal media. A full format using maximum SHIFT and FMREAD values will probably not find all of the latent flaws. A high speed format, in conjunction with the flaw map will produce the maximum media reliability.

OPTION TABLE

OPTION	MANDATORY	DEFAULT	DESCRIPTION
TEST	NO	0,1	TEST 0 - BASIC CONTROLLER TEST TEST 1 - PACK FORMAT TEST 2 - WRITE/READ TEST ONLY
DISCON	NO	X'00FB'	DISK CONTROLLER ADDRESS
SELCH	NO	X'00F0'	SELCH ADDRESS
PACTYP	YES	CE	IDENTIFIES PACK TYPE TO BE FORMATTED CE00 - CUSTOMER ENGINEER PACK 0000 - 67MB PACK 0001 - 256MB PACK 0002 - 675MB PACK 0003 - 16MB CMD REMOVABLE 0004 - 16MB CMD FIXED 0005 - 48MB CMD FIXED 0006 - 80MB CMD FIXED 0007 - CAPRICORN 0008 - 19.8MB REMOVABLE LARK 0009 - 19.8MB FIXED LARK 000A - 160MB FIXED (CDC 9715) 000B - OPTION TABLE INPUT
LOCYL	YES	X'FFFF'	STARTING LOW CYLINDER (HEX) FOR START OF FORMAT. MUST BE <= HICYL AND MAXIMUM FOR PACTYP. USUALLY SET TO X'0000'
HICYL	YES	X'FFFF'	ENDING HIGH CYLINDER FOR FORMAT. MUST BE >= LOCYL AND <= MAXIMUM FOR PACKTYP. USUALLY SET TO X'0336'
DRIVE	YES	X'FFFF'	SET TO 0,1,2 OR 3 FOR EACH DRIVE ADDRESS.
DATPAT	NO	X'6BD6'	DATA PATTERN USED FOR PACK CERTIFICATION
SHIFT	NO	X'0002'	NUMBER OF TIMES DATA PATTERN IS SHIFTED. MINIMUM OF 1, MAY BE INCREASED TO IMPROVE CHANCE OF FLAGGING ALL DEFECTIVE SECTORS. MAX VALUE OF 8 SUGGESTED.

FMREAD	NO	X'0001'	INCREASING ALLOWS STROBE/OFFSET TESTING 1 - STROBE NORM/OFFSET NORM 2 - STROBE EARLY/OFFSET PLUS 3 - STROBE LATE/OFFSET MINUS 4 - STROBE EARLY/OFFSET MINUS 5 - STROBE NORM/OFFSET MINUS 6 - STROBE LATE/OFFSET PLUS 7 - STROBE NORM/OFFSET PLUS 8 - STROBE LATE/OFFSET NORM 9 - STROBE EARLY/OFFSET NORMAL A - STROBE NORM/OFFSET NORMAL
CYL	NO	0644	PACTYP B TABLE INPUT. MAXIMUM CYLINDER NUMBER
TRK	NO	0002	PACTYP B TABLE INPUT. MAX TRACK (HEAD) NUMBER
HOFF	NO	0000	PACTYP B TABLE INPUT. HEAD OFFSET FOR FIXED/ REMOVABLE PACKS. SET TO 2 FOR LARK REMOVABLE PACK.
PSEC	NO	0032	PACTYP B TABLE INPUT. PHYSICAL SECTOR COUNT. NORMALLY 33, REDUCE TO 32 FOR LARK.
LSEC	NO	0062	PACTYPB TABLE INPUT. LOGICALSECTORCOUNT. NORMALLY 64, REDUCE TO 32 FOR LARK.
INFLAW	NO	0001	INPUT FLAW MAP INFORMATION. IF SET TO 1, FLAW LOCATIONS ARE ENTERED AT START OF TEST.
CLYPRT	NO	0001	SETS DISPLAY OF EVERY 'N' LINE OF DIAGNOSTIC RUN MESSAGE.
PANEL	NO	0000	SET TO 1 FOR HEX DISPLAY PANEL OUTPUT
DIAG	NO	0000	SET TO 1 FOR IMMEDIATE ERROR MESSAGE DISPLAY
NOMSG	NO	0000	SET TO 1 TO SUPPRESS MESSAGES
CONTIN	NO	0000	SET TO 1 FOR CONTINUOUS TESTING
INTLEV	NO	0000	INTERRUPT LEVEL
LOOP	NO	0000	RERUNS TESTS 'N' TIMES
OPTION			CAUSES OPTION TABLE TO BE PRINTED
RUN			CAUSES DIAGNOSTIC TO BE EXECUTED
CON			CAUSES DEBUG MODE TO BE ENTERED
@			CAUSES DEBUG MODE TO BE ENTERED

CHAPTER 4
THEORY OF OPERATION

4-1 GENERAL OVERVIEW OF MIDC

By understanding the flow of external I/O signals associated with the MIDC board, you will gain a general idea of what the MIDC does. With this objective in mind, Section 3-1 treats the MIDC as a blackbox and presents an overview of all the I/O lines to and from the MIDC connectors. Later sections discuss the internal operation of the MIDC.

Refer to Figure 1-1 in chapter 1. This figure illustrates the physical connections of an MIDC board. Figure 3-1 illustrates the I/O lines associated with the physical connectors. CONN 1 thru CONN 6, of lines: Section 3-1.1 describes the lines from MIDC CONN 1 to the SELCH or CM board plugged in to the processor. Section 3-1.2 describes the A-cable lines between MIDC connector CONN 2 and attached disk files. Section 3-1.3 describes the B-cable lines between MIDC connectors CONN 3 thru CONN 6 and the attached disk files.

NOTE

References in this chapter to the Selector Channel (SELCH and B-SELCH) also apply to the Channel Manager (CM).

Figure 4-1 MIDC I/O Signals

4-1.1 I/O Lines At Connector CONN 1

See Figure 3-1. The I/O lines at CONN 1 are connected to the SELCH plugged into the same processor chassis with the MIDC or installed under an I/O Bus Switch. These lines are classified here into five functional groups:

(1) Initialization Lines
(2) Data Lines
(3) Control Lines
(4) Protocol-Related Lines
(5) Interrupt-Related Lines

The following paragraphs, number (1) thru (5), describe the I/O lines within these groups.

(1) Initialization Lines

This group of lines initializes the MIDC logic:

(a) System Clear (SCLRO)
Input from the processor to Initialize MIDC logic during a system power-up, shutdown, or initialization operation.

(b) Early Power Fail (CLO7O)
Input from the processor to warn the MIDC of an imminent power failure.

(2) Data Lines

This group of sixteen I/O lines transfers data between the SELCH and the MIDC board:

(a) Halfword Data Bits (DOO:15)

SELCH or processor I/O consisting of halfword or a byte of data. With halfword I/O, data bits DOO:15 transfer the data for a read/write operation or the address for a disk cylinder or head, With byte I/O, DO8:15 transfer and MIDC or disk file address, a processor command, and MIDC or disk file status, a sector address,or Rotational Position Sensing (RPS) data.

(3) Control Lines

This group consists of these I/O lines:

(A) Address (ADRSO)
Input from the processor to inform MIDC that data bits DO8:15 contain an MIDC address or a disk file address. The addressed device is to be selected for subsequent I/O operation.

(b) Command (CMDO)
Input from the processor to inform MIDC that data bits DO8:15 contain a command for the selected device, i.e., the MIDC or disk file.

(c) Data Available (DAO)
Input from the SELCH or processor to inform MIDC that a halfword of data is available on DOO:15 for a write operation to MIDC.

(d) Data Request (DRO)
Input from the SELCH or processor that requests MIDC for a halfword of data on DOO:15 for a read operation from MIDC.

(e) Status Request (SRO)
Input from the SELCH or the processor to request and MIDC status or disk file status byte from data bits D08:15.

(f) Sync Return (SYNO)
MIDC output signaling the SELCH or processor that the MIDC has properly accepted and responded to a received control line signal.

(4) Protocol- Related Lines

This group of lines relates to the protocol exchanges between the SELCH and the MIDC boards:

(a) Employ I/O Bus Switch (BUSSWO)
MIDC output informing the SELCH that the MIDC employs the "new" high-speed SELCH protocol with and I/O Bus Switch.

(b) Set New Sequence (SNSO)
MIDC output informing the SELCH that the MIDC uses "new" high-speed SELCH protocol with out an I/O Bus Switch.

(c) Status Check (SCHKO)
MIDC output informing the SELCH of a bad MIDC status. This output applies only when the MIDC uses the high-speed SELCH protocol.

(d) SELCH Busy (SBSTO)
Input from the SELCH to inform MIDC that the SELCH IS currently busy with a block-data transfer.

(e) Halfword Mode (HWO)
MIDC output informing the SELCH that this controller (MIDC) is a halfword-oriented device.

(5) Interrupt-Related Lines

This group of lines relates to an interrupt request from the MIDC board:

(a) Attention (ATNO)
MIDC output requesting a processor interrupt, placing the MIDC into an interrupt-pending state.

(b) Receive Acknowledge (RACKO)
Input from the processor to acknowledge an interrupt from an MIDC; see item (a) above. If the MIDC has no interrupt pending, it passes the RACKO signal out as a TACKO signal to the next MIDC board stacked in the processor.

(c) Transmit Acknowledge (Tacko)
MIDC output consisting of a RACKO signal received by an MIDC having no interrupt pending.

4-1.2 I/O Lines at Connector CONN 2

See Figure 4-1. The I/O lines at CONN 2 are through the A-cable to the attached disk files. These lines are classified here into four functional groups:

(1) Select Lines
(2) Command/Address Lines
(3) Operational Status Lines
(4) Fault Status Lines

The following paragraphs, numbered (1) thru (4), describe the I/O lines within these groups.

(1) Select Lines

This group of lines is involved with the selection of a disk file:

(a) Unit Select Tag (USTAG)
MIDC output informing the attached disk files that the two Unit Select Lines (USELO and USEL1, described below) are supplying a binary-coded number, 0-3, to select a disk file.

(b) Unit Select Lines (USELO, USEL1)
MIDC output consisting of a binary-code number, 0-3, to select a particular disk file for I/O with the MIDC.

(2) Command/Address Lines

This group of lines supplies command and address data as control input to a selected disk file:

(a) Data Bus Bits (BOO:09)
MIDC output consisting of control or address data, e.g., a driver command, a cylinder address, or a head address. The content of these lines depends on the three tags discussed in items (b), (c), and (d) below.

(b) Control Tag (CT)
MIDC output indicating that BOO:09 are supplying a driver command.

(c) Select-Cylinder Tag (SCT)
MIDC output indicating that BOO:09 are supplying a cylinder address.

(d) Select-Head Tag (SHT)
MIDC output indicating that BOO:09 are supplying head-select or volume-select data.

(3) Operational Status Lines

These signals supply the normal operational status of a disk file.

(a) Unit Ready (UNRDYL)
Disk file output signaling MIDC that the selected disk file is ready for I/O with the MIDC.

(b) Dual-Port Busy (BUSY)
Disk file output applicable only to dual-port operation of a disk file. It informs MIDC that the disk file is currently selected by another MIDC.

(c) On-Cylinder Detection (ONCYL)
Disk file output that signals the MIDC once the heads of the selected disk file are positioned over an addressed cylinder

(d) Write Protect (WTPT)
Disk file output informing MIDC that the write-protect button on the disk file is depressed, i.e., that the disk file is in the write-protect mode.

(e) Power Sequencing (HOLD/PICK)
MIDC output of a ground signal that "picks and holds" power sequencing for the attached disk files in remote mode. (this signal is present when the processor is on and MIDC SEQ Pins 1 and 2 are not strapped.)

(4) Fault Status Lines

These signals supply the normal fault status of a disk file.

(a) Fault (FAULT)
Disk file output informing MIDC of a fault condition at a disk file.

(b) Seek Error (SKER)
Disk file output informing MIDC of a seek error at a disk file.

(c) Open Cable Detection (OBCAD)
Disk file output informing MIDC of an open cable or a loss of power, This signal prevents MIDC from outputting select or control data to the disk file.

4-1.3 I/O Lines at Connectors CONN 3 thru CONN 6

See Figure 3-1. The I/O lines on any one of these connectors --CONN 3, CONN 4, CONN 5, or CONN 6 -- are through a B- cable to a disk file. These lines are classified here into three functional groups:

(1) Control Lines
(2) Write-Related Lines
(3) Read-Related Lines

The following paragraphs, numbered (1) thru (3), describe the I/O lines within these groups.

(1) Control Lines

This group of lines passes various control signals to MIDC in order to coordinate the transfer of read/write data. The # symbol with each mnemonic denotes one of four numbers, 0-3. For one of the four possible disk files.

(a) Unit Selected Tag (USEL#)
Disk file output signaling MIDC that the disk file is now acquired, i.e., select, by the MIDC.

(b) Index (INX#)
Disk file output consisting of a pulse for every disk revolution. This pulse serves as an index for disk sector 0.

(c) Seek End (SKED#)
Disk file output signaling the end of a seek operation, either successful or unsuccessful.

(2) Write-Related Lines

This group of lines relates to write operations from the MIDC to a disk files.

(a) Servo Clock (SCLK#)
Disk file output used by the MIDC as input for the WCLK# signal; see (b) below.

(b) Write Clock (WCLK#)
MIDC output that synchronizes data written to the disk file.

(c) Write Data (WDAT#)
MIDC output consisting of data written to the disk file.

(3) Read-Related Lines

This group of lines relates to read operations from the disk file to the MIDC:

(a) Read Clock (RCLK#)
Disk file output that synchronizes data read from the disk file.

(b) Read Data (RDAT#)
Disk file output consisting of data read from the disk file.

4-2 I/O LINES OF THE MIDC BOARD

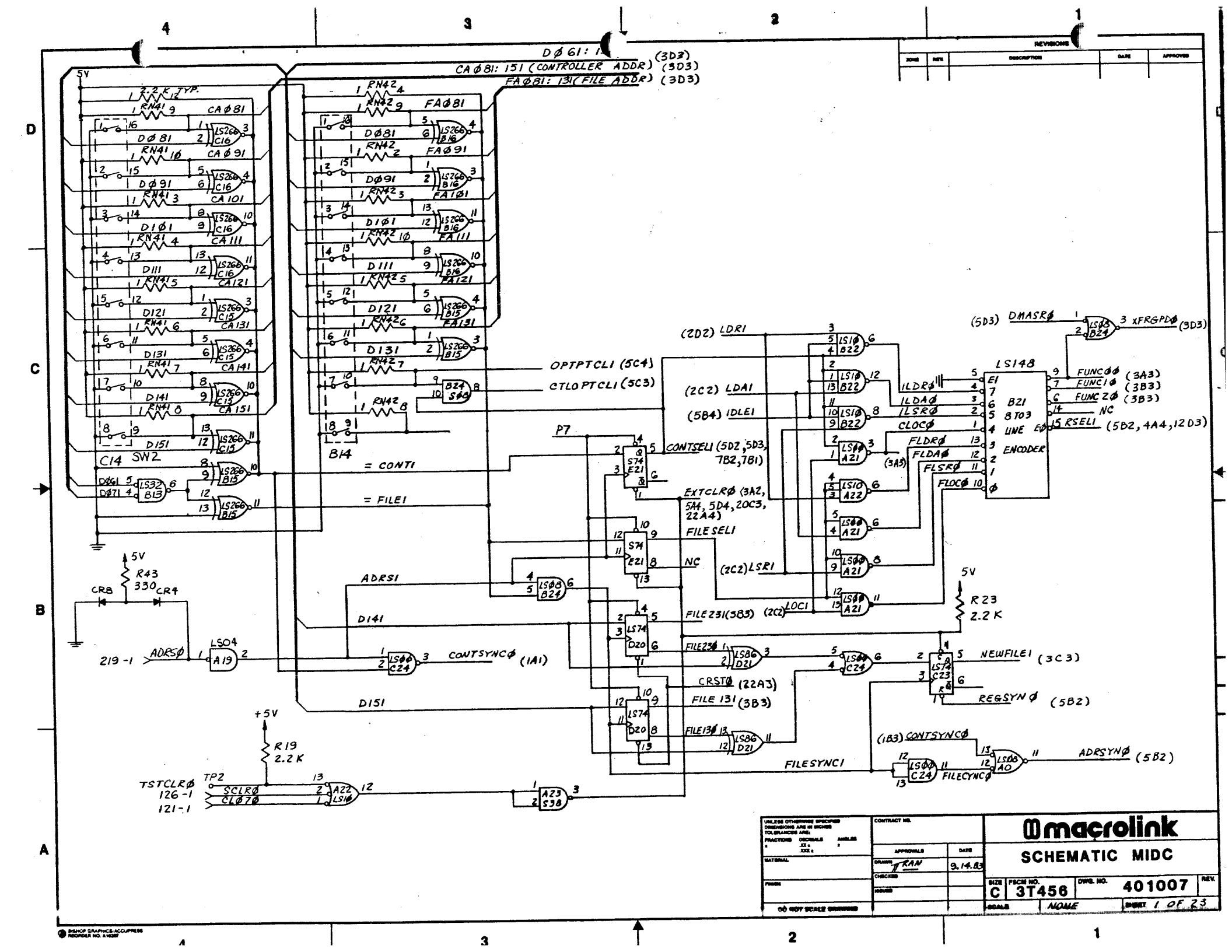
This section presents detailed descriptions of the same external I/O lines just overviewed in Section 3-1. Figure 3-2 shows the connectors of the MIDC board and serves as a reference to other figures that illustrate the I/O lines attached to the connector pins. Section 3-2.1 thru 3-2.3 describe these I/O lines.

NOTE

References in these descriptions to the Selector Channel (SELCH) also apply to the Channel Manager (CM).

Connector	Destination
CONN 0	Not Used
CONN 1	SELCH/MUS BUS of 3200 Processor
CONN 2	A-CABLE TO DISK FILE 0
CONN 3	B-CABLE TO DISK FILE 3
CONN 4	B-CABLE TO DISK FILE 2
CONN 4	B-CABLE TO DISK FILE 2
CONN 5	B-CABLE TO DISK FILE 1
CONN 6	B-CABLE TO DISK FILE 0

FIGURE 4-2. Connectors on MIDC Board



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FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

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SCHEMATIC MIDC

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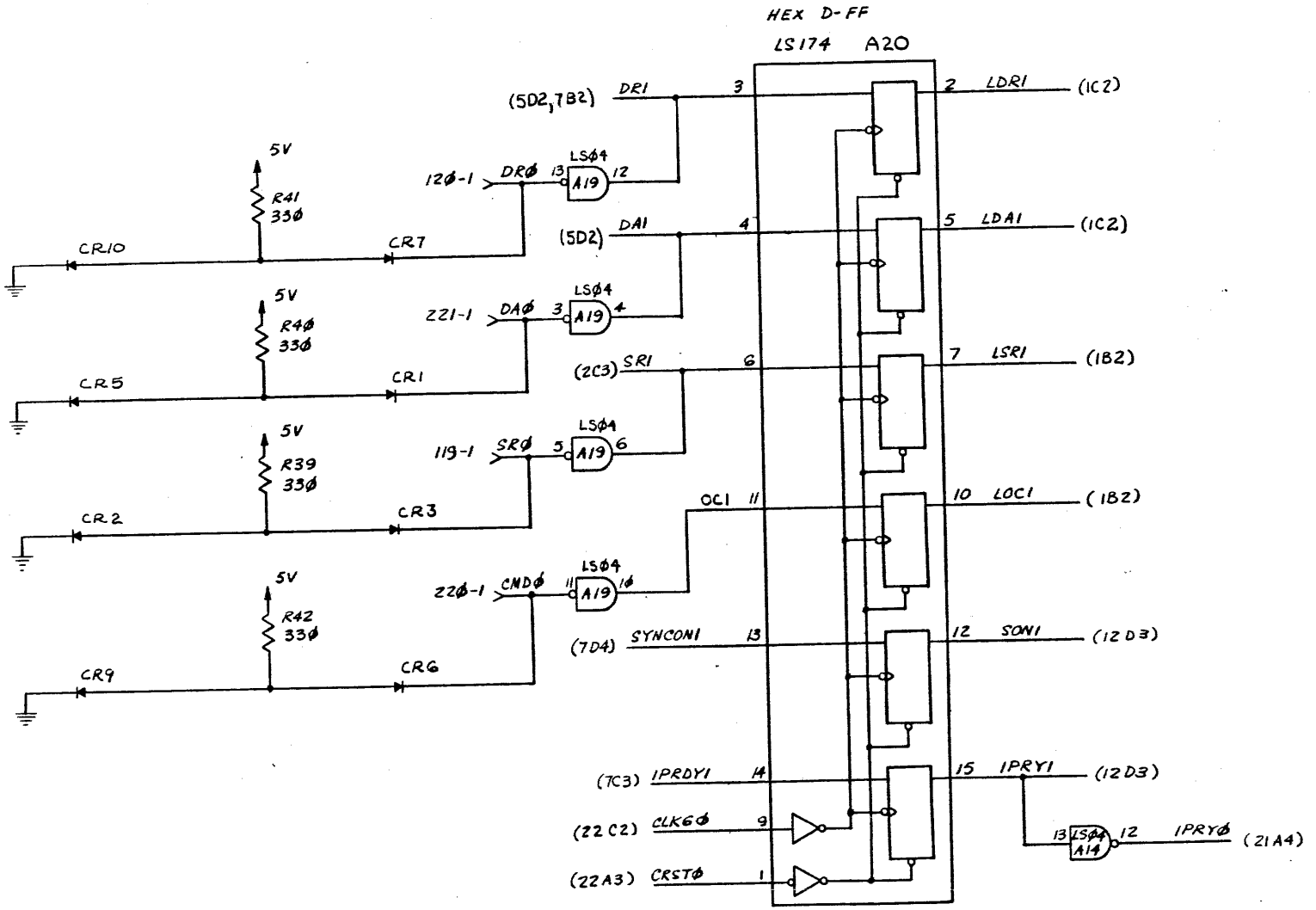

NOTES:
1. ALL DIODES ARE IN4454

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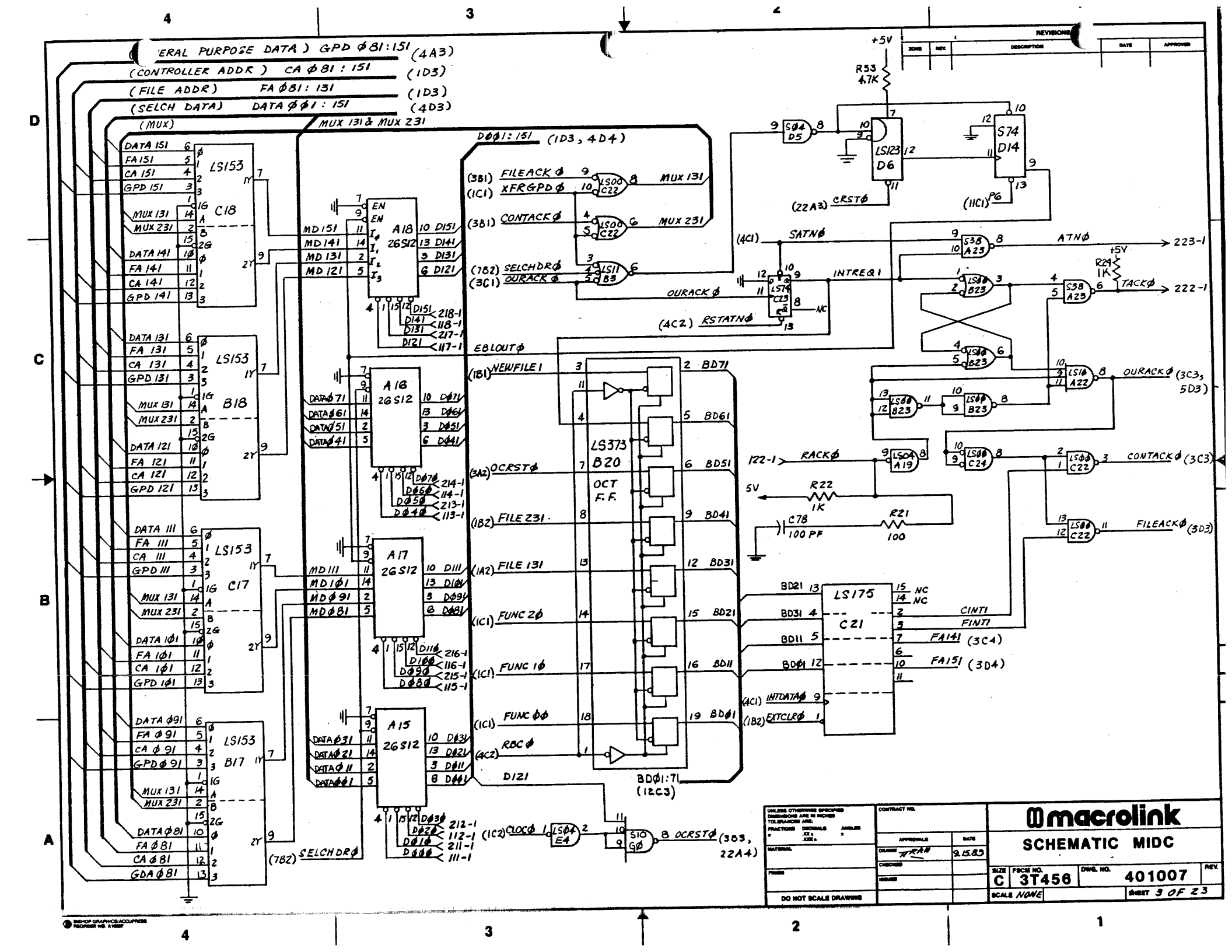
	ISSUED		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(CONTROLLER ADDR) CA Ø81 : 151 (1D3)
(FILE ADDR) FA Ø81: 131 (1D3)
(SELCH DATA) DATA ØØ1 : 151 (4D3)
(MUX) MUX 131 & MUX 231
DØØ1:151 (1D3, 4D4)
+5V
R53 4.7K
REVISIONS
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LS153 C18
LS153 B18
LS153 C17
LS153 B17
A18 2GS12
A16 2GS12
A17 2GS12
A15 2GS12
LS373 B20 OCT F.F.
LS175 C21
S74 D14
LS123 D6
S04 D5
LS00 C22
LS11 B3
LS74 C23
LS04 A19
LS04 E4
S10 G0
LS08 B23
LS08 A22
LS08 C24
S38 A23
R22 1K
C78 100 PF
R21 100
R24 1K
FILEACK Ø
XFRGPD Ø
CONTACK Ø
SELCHDR Ø
OURACK Ø
RSTATN Ø
SATN Ø
ATN Ø
INTREQ I
EBLOUT Ø
NEWFILE I
OCRST Ø
FILE Z31
FILE 131
FUNC 2Ø
FUNC 1Ø
FUNC ØØ
RBC Ø
CLOC Ø 1
D121
BDØ1:7I (12C3)
RACK Ø
INTDATA Ø
EXTCLR Ø
CINTI
FINTI
FA141 (3C4)
FA151 (3D4)
CONTACK Ø (3C3)
FILEACK Ø (3D3)
OURACK Ø (3C3, 5D3)
TACK Ø
CRST Ø
PG
NC
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SIZE C FSCM NO. 3T456 DWG. NO. 401007 REV.
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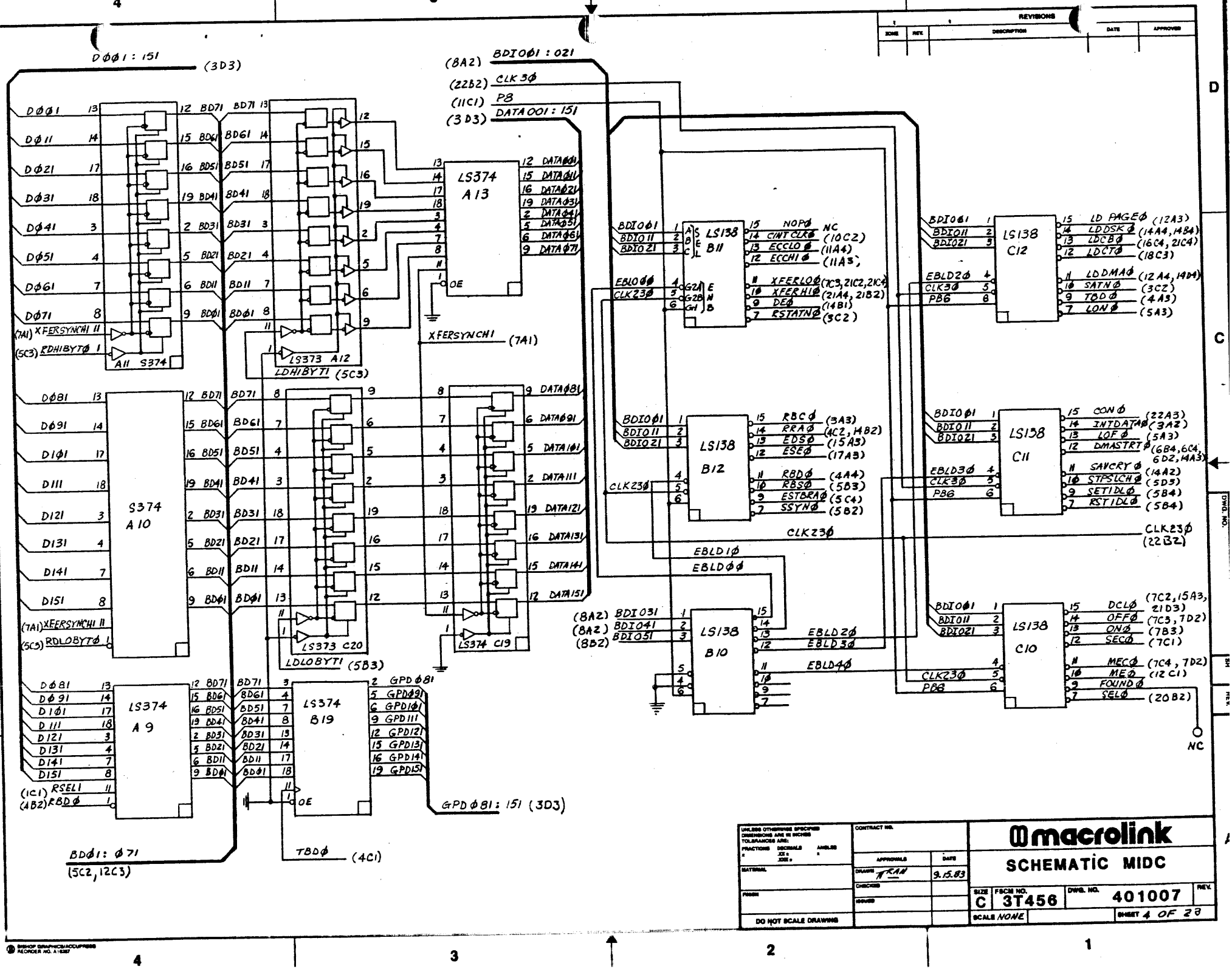
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DØØ1 : 151 (3D3)
(8A2) BDIOØ1 : 021
(22B2) CLK 3Ø
(11C1) P8
(3D3) DATA001 : 151
S374 A11
LS373 A12
LS374 A13
LDHIBYTI (5C3)
XFERSYNCHI (7A1)
S374 A10
LS373 C20
LS374 C19
LDLOBYTI (5B3)
LS374 A9
LS374 B19
OE
GPDØ81 : 151 (3D3)
TBDØ (4C1)
BDØ1 : Ø71 (5C2, 12C3)
LS138 B11
LS138 B12
LS138 B10
LS138 C12
LS138 C11
LS138 C10
CLK23Ø (22B2)
EBLD1Ø
EBLDØØ
EBLD2Ø
EBLD3Ø
EBLD4Ø
NC
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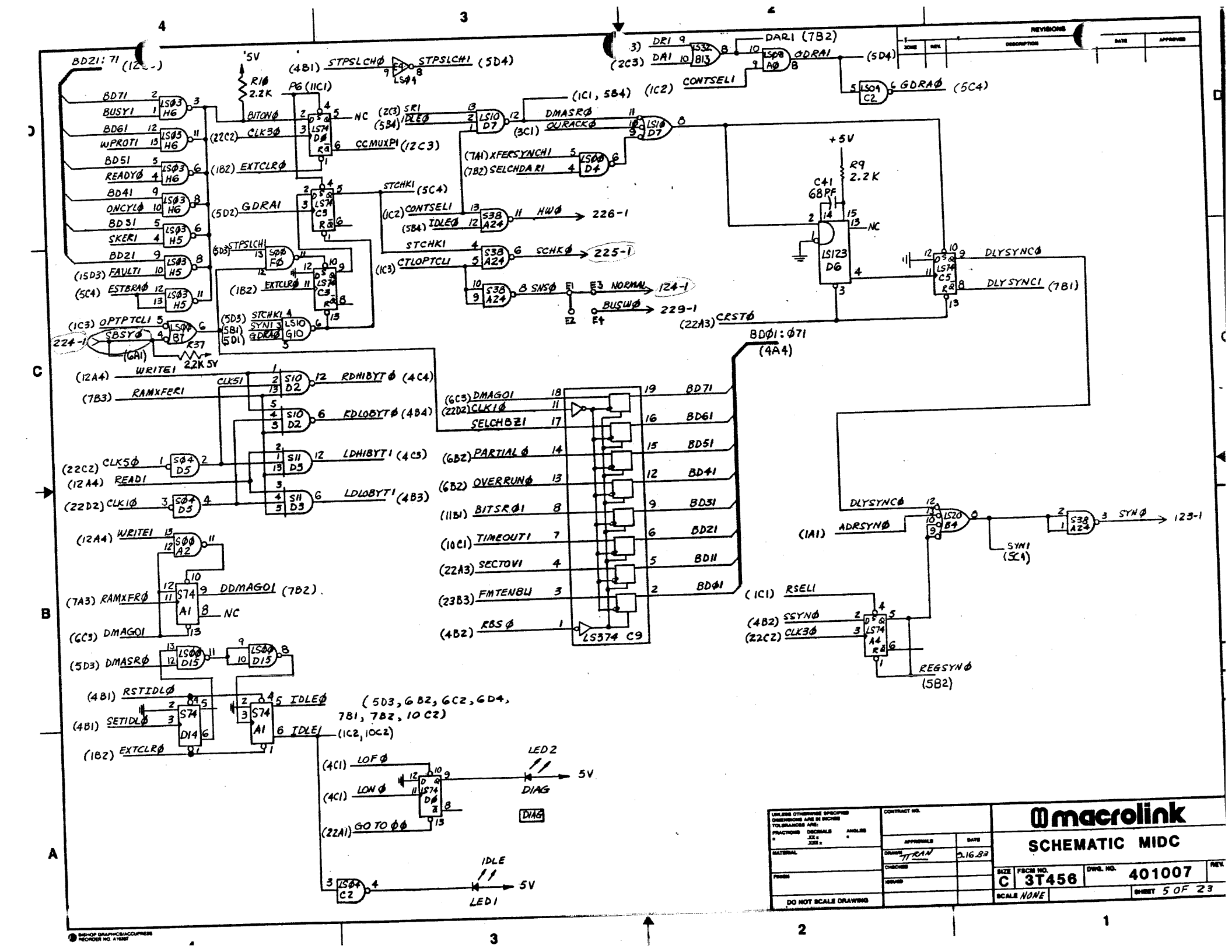
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5V
R10 2.2K
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BD6I
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BD5I
READYØ
BD4I
ONCYLØ
BD3I
SKERI
BD2I
FAULTI
ESTBRAØ
OPTPTCLI
SBSYØ
R37 2.2K 5V
BITONØ
CLK3Ø
EXTCLRØ
NC
CCMUXPI
STPSLCHØ
STPSLCHI (5D4)
GDRAI
STCHKI
SYNI
GDRAØ
DRI
DAI
DARI (7B2)
ODRAI
GDRAØ (5C4)
CONTSELI
SRI
IDLEØ
DMASRØ
QURACKØ
XFERSYNCHI
SELCHDARI
HWØ
226-1
SCHKØ
225-1
B SNSØ
NORMAL
124-1
BUSWØ
229-1
CRSTØ
+5V
R9 2.2K
C41 68PF
NC
DLYSYNCØ
DLYSYNCI (7B1)
BDØI: Ø71 (4A4)
WRITEI
RAMXFERI
CLK5I
RDHIBYTØ (4C4)
RDLOBYTØ (4B4)
CLK5Ø
READI
LDHIBYTI (4C3)
CLK1Ø
LDLOBYTI (4B3)
DMAGOI
CLK1Ø
SELCHBZI
PARTIALØ
OVERRUNØ
BITSRØI
TIMEOUTI
SECTOVI
FMTENBLI
RBSØ
LS374 C9
BD7I
BD6I
BD5I
BD4I
BD3I
BD2I
BD1I
BDØI
RAMXFRØ
DDMAGOI (7B2)
NC
DMASRØ
RSTIDLØ
SETIDLØ
EXTCLRØ
IDLEØ
IDLEI (1C2, 10C2)
(5D3, 6B2, 6C2, 6D4, 7B1, 7B2, 10C2)
LOFØ
LOWØ
GO TO ØØ
LED2
DIAG
LED1
IDLE
ADRSYNØ
SYNØ
SYNI (5C4)
RSELI
SSYNØ
CLK3Ø
REGSYNØ (5B2)
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SIZE C
FSCM NO. 3T456
DWG. NO. 401007
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SHEET 5 OF 23
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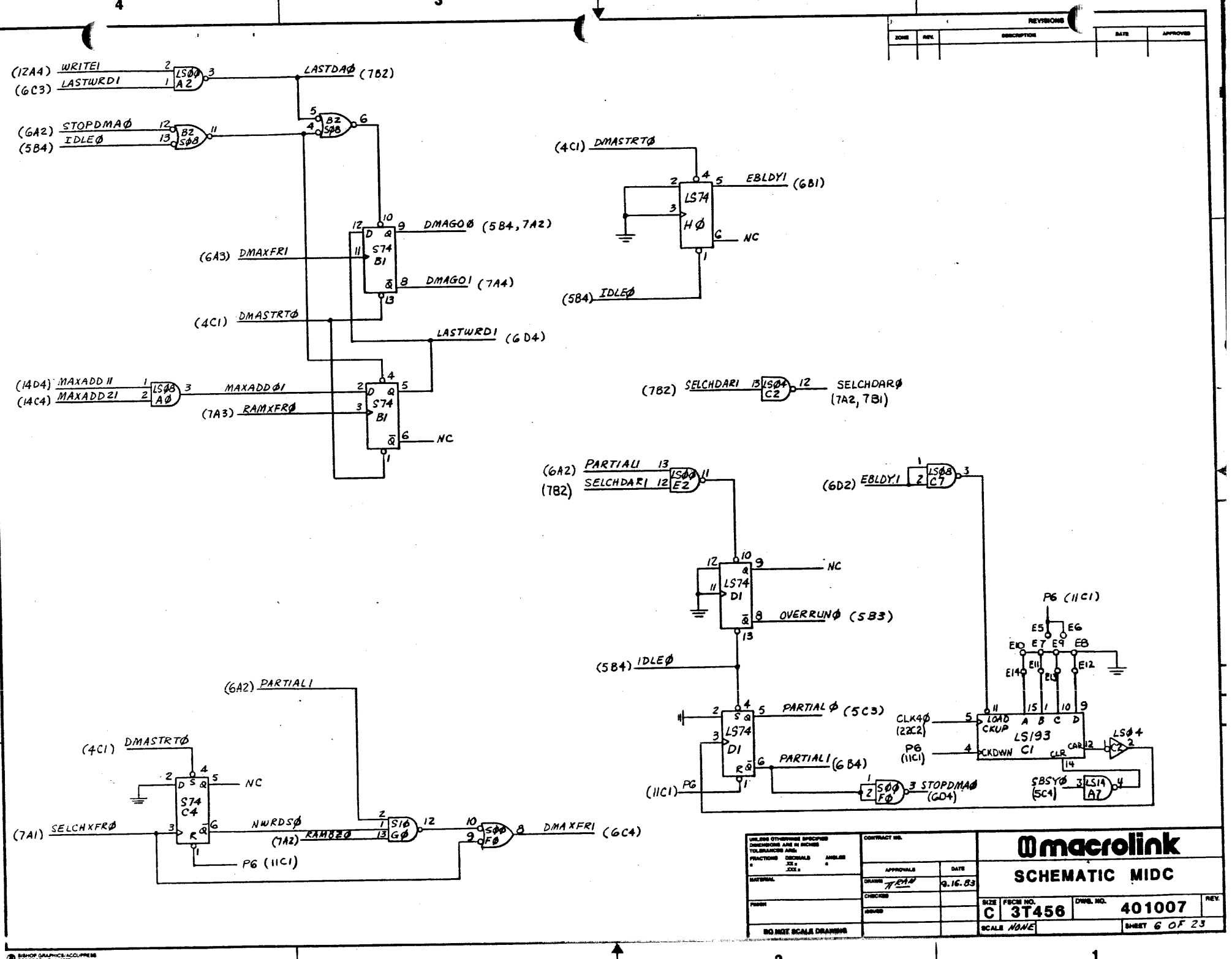

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SCHEMATIC MIDC

SIZE	FSCM NO.	DWG. NO.	REV.
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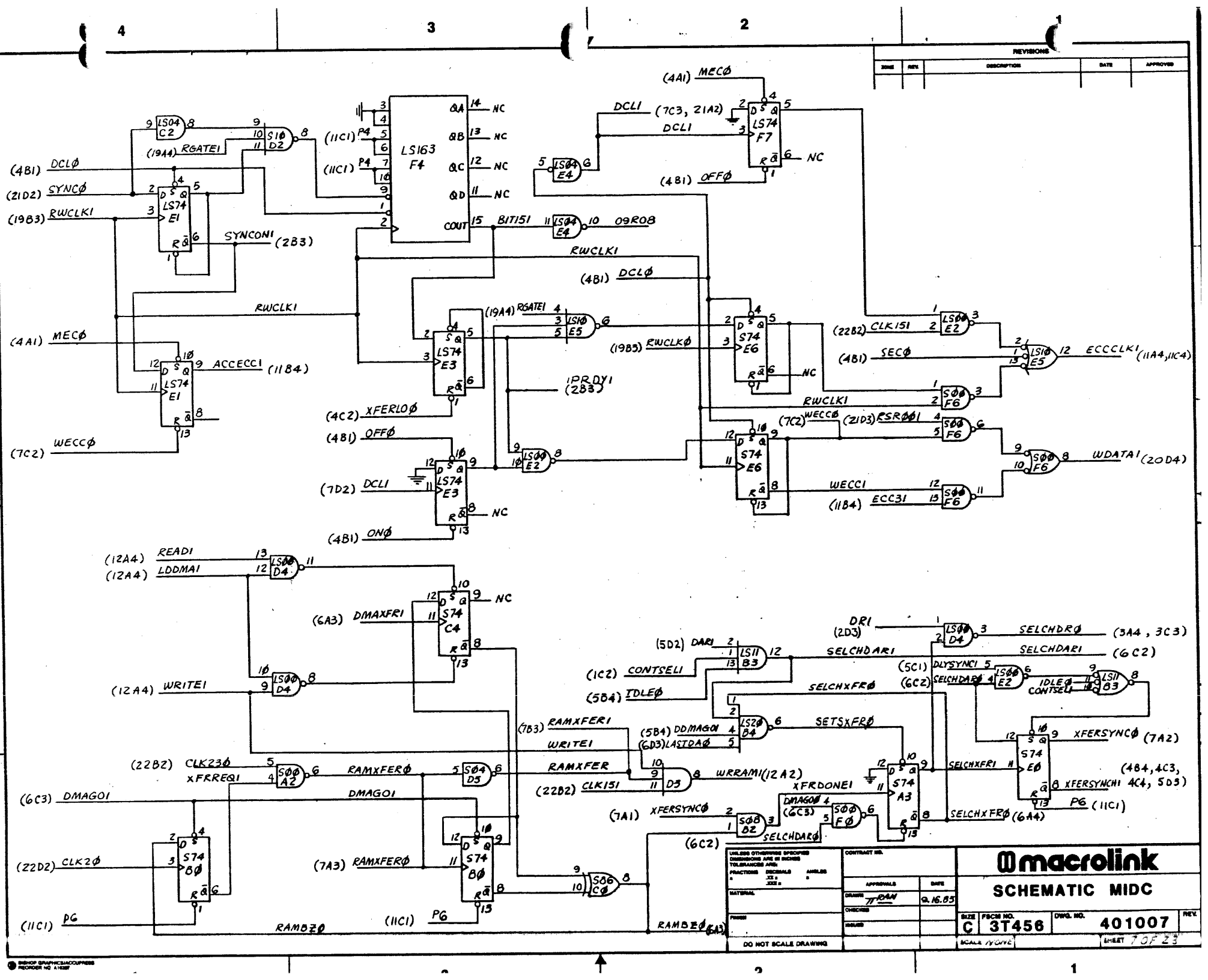
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LS74 S74 B2
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LS04 D4
LS04 D4
LS04 D5
LS04 A2
LS04 B2
LS04 C0
LS10 D2
LS10 E5
LS11 B3
LS11 B3
LS20 B4
(4A1) MECØ
DCLI (7C3, 21A2)
DCLI
(4B1) OFFØ
(4B1) DCLØ
(21D2) SYNCØ
(19B3) RWCLKI
(19A4) RGATEI
SYNCONI (2B3)
(11C1) BIT151
09R08
RWCLKI
(19B3) RWCLKØ
(22B2) CLK151
(4B1) SECØ
ECCCLKI (11A4,11C4)
RWCLKI
(7C2) WECCØ
(21D3) FSR00I
WDATAI (20D4)
WECCI
(11B4) ECC31
(4C2) XFERLOØ
IPRDYI (2B3)
(7D2) DCLI
(4B1) ONØ
(12A4) READI
(12A4) LDDMAI
(6A3) DMAXFRI
(12A4) WRITEI
(22B2) CLK23Ø
XFRREQI
RAMXFERØ
RAMXFER
(7B3) RAMXFERI
WRITEI
(22B2) CLK15I
WRRAMI (12A2)
(6C3) DMAGOI
DMAGOI
(22D2) CLK2Ø
(7A3) RAMXFERØ
(11C1) PG
RAMBZØ
(5D2) DARI
(1C2) CONTSELI
(5B4) IDLEØ
(5B4) DDMAGOI
(6D3) LASTDAØ
SETSXFRØ
DRI (2D3)
SELCHDRØ (3A4, 3C3)
SELCHDARI
SELCHDARI (6C2)
(5C1) DLYSYNCI
(6C2) SELCHDARØ
IDLEØ
CONTSELI
XFERSYNCØ (7A2)
SELCHXFRI
(4B4,4C3, 4C4, 5D3)
XFRSYNCHI
XFRDONEI
(7A1) XFERSYNCØ
DMAGOØ (2C3)
SELCHXFRØ (6A4)
SELCHDARØ
(6C2)
P6 (11C1)
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SCHEMATIC MIDC
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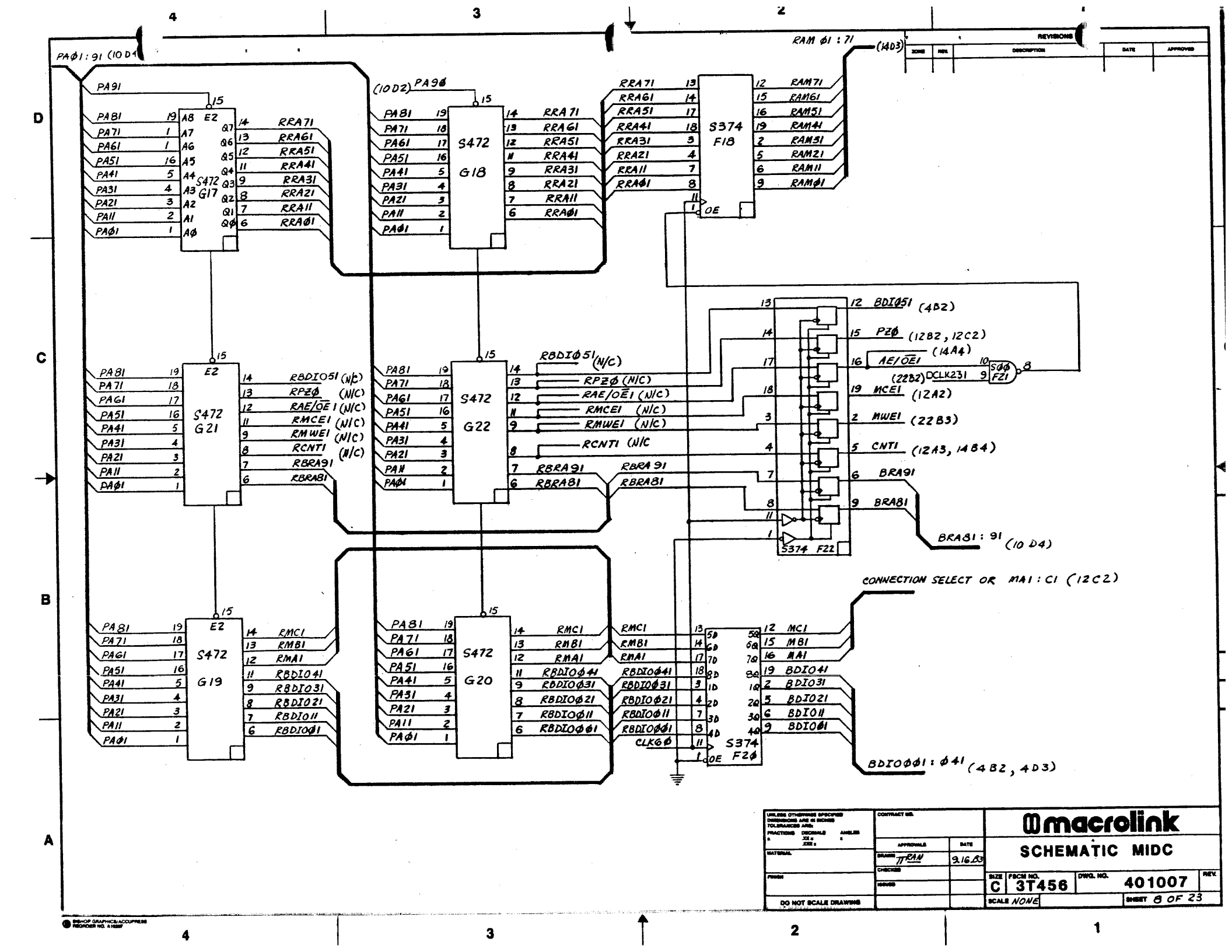
SHEET 7 OF 23


PAØI : 9I (10 D1)
PA9I
PA8I
PA7I
PA6I
PA5I
PA4I
PA3I
PA2I
PAII
PAØI
S472 G17
RRA7I
RRA6I
RRA5I
RRA4I
RRA3I
RRA2I
RRAII
RRAØI
(10D2) PA9Ø
S472 G18
S374 F18
OE
RAM Ø1 : 7I
(14D3)
RAM7I
RAM6I
RAM5I
RAM4I
RAM3I
RAM2I
RAMII
RAMØI
S472 G21
RBDIØ5I (N/C)
RPZØ (N/C)
RAE/OEI (N/C)
RMCEI (N/C)
RMWEI (N/C)
RCNTI (N/C)
RBRA9I
RBRA8I
S472 G22
RBDIØ5I (N/C)
RPZØ (N/C)
RAE/OEI (N/C)
RMCEI (N/C)
RMWEI (N/C)
RCNTI (N/C
RBRA9I
RBRA8I
BDIØ5I (4B2)
PZØ (12B2, 12C2)
(14A4)
AE/OEI
(22B2) DCLK23I
SØØ FZI
MCEI (12A2)
MWEI (22B3)
CNTI (12A3, 14B4)
BRA9I
BRA8I
BRA8I : 9I (10 D4)
S374 F22
S472 G19
RMCI
RMBI
RMAI
RBDIØ4I
RBDIØ3I
RBDIØ2I
RBDIØ1I
RBDIØØI
S472 G20
RMCI
RMBI
RMAI
RBDIØ4I
RBDIØ3I
RBDIØ2I
RBDIØ1I
RBDIØØI
CLKGØ
S374 F2Ø
OE
CONNECTION SELECT OR MAI : CI (12C2)
MCI
MBI
MAI
BDIØ4I
BDIØ3I
BDIØ2I
BDIØ1I
BDIØØI
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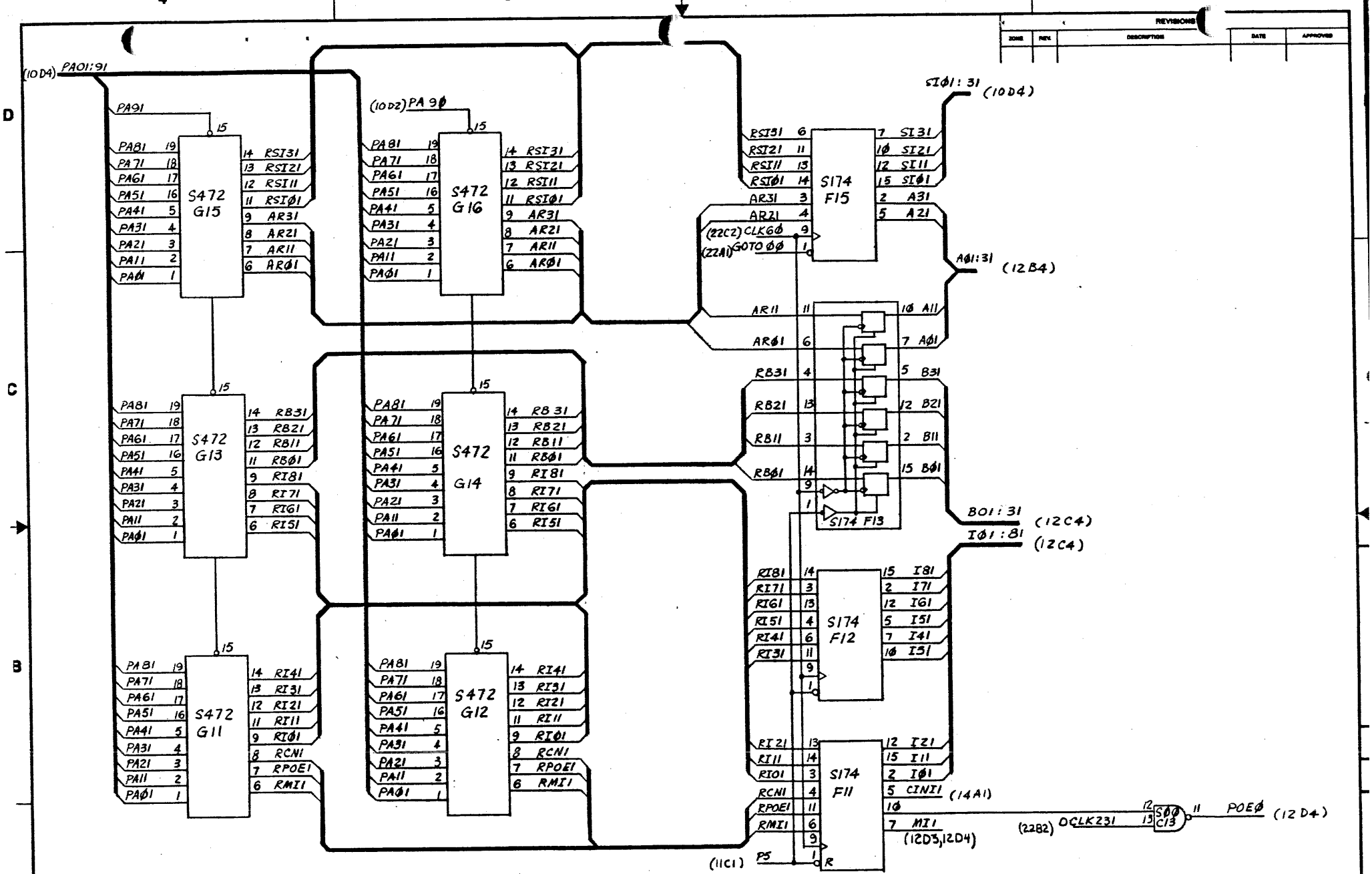
SHEET 8 OF 23
BISHOP GRAPHICS/ACCUPRESS REORDER NO. A1688



REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

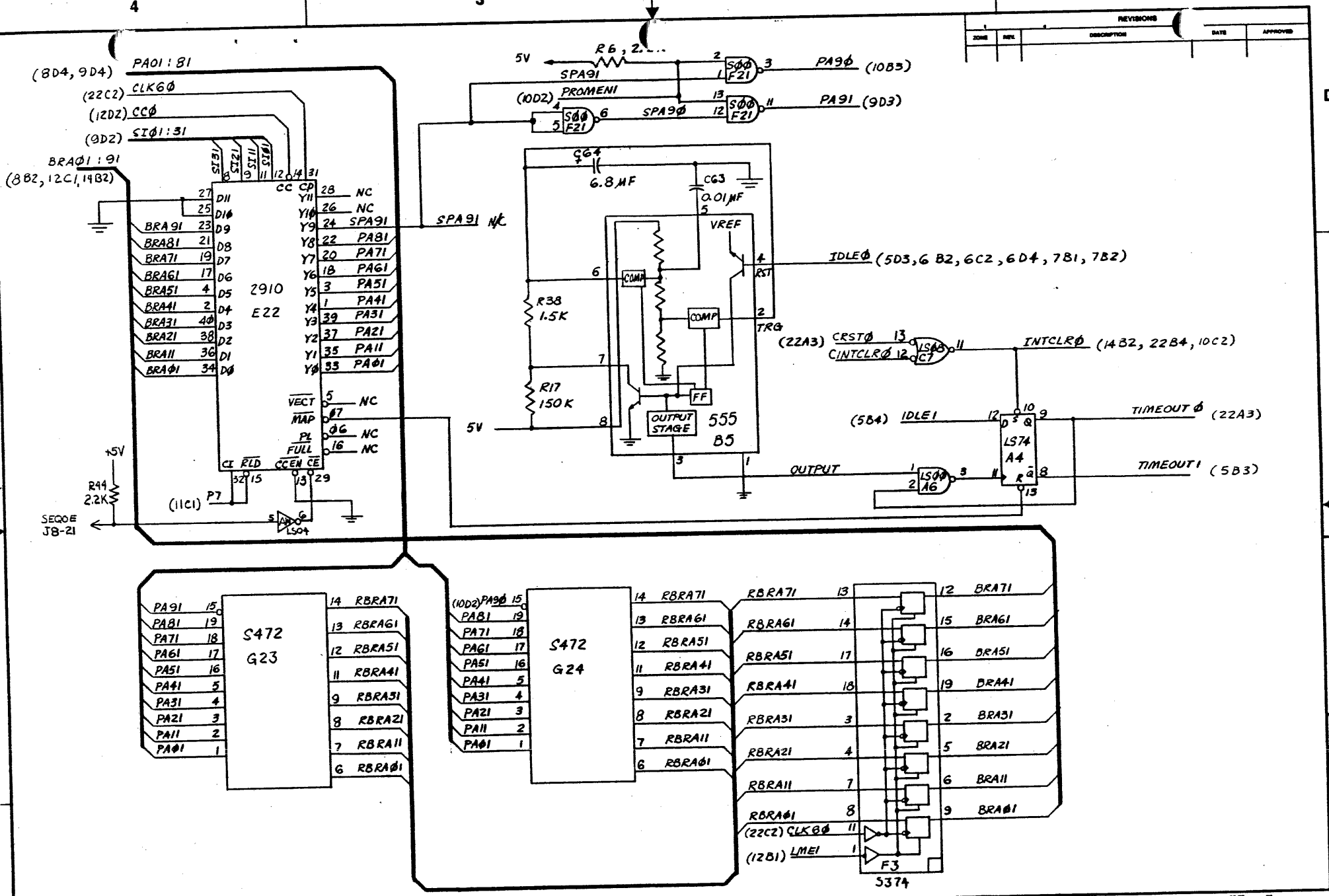
APPROVALS	DATE
DRAWN TRAN	9.19.83
CHECKED	
ISSUED	

macrolink

SCHEMATIC MIDC

SIZE C | FSCM NO. 3T456 | DWG. NO. 401007 | REV.

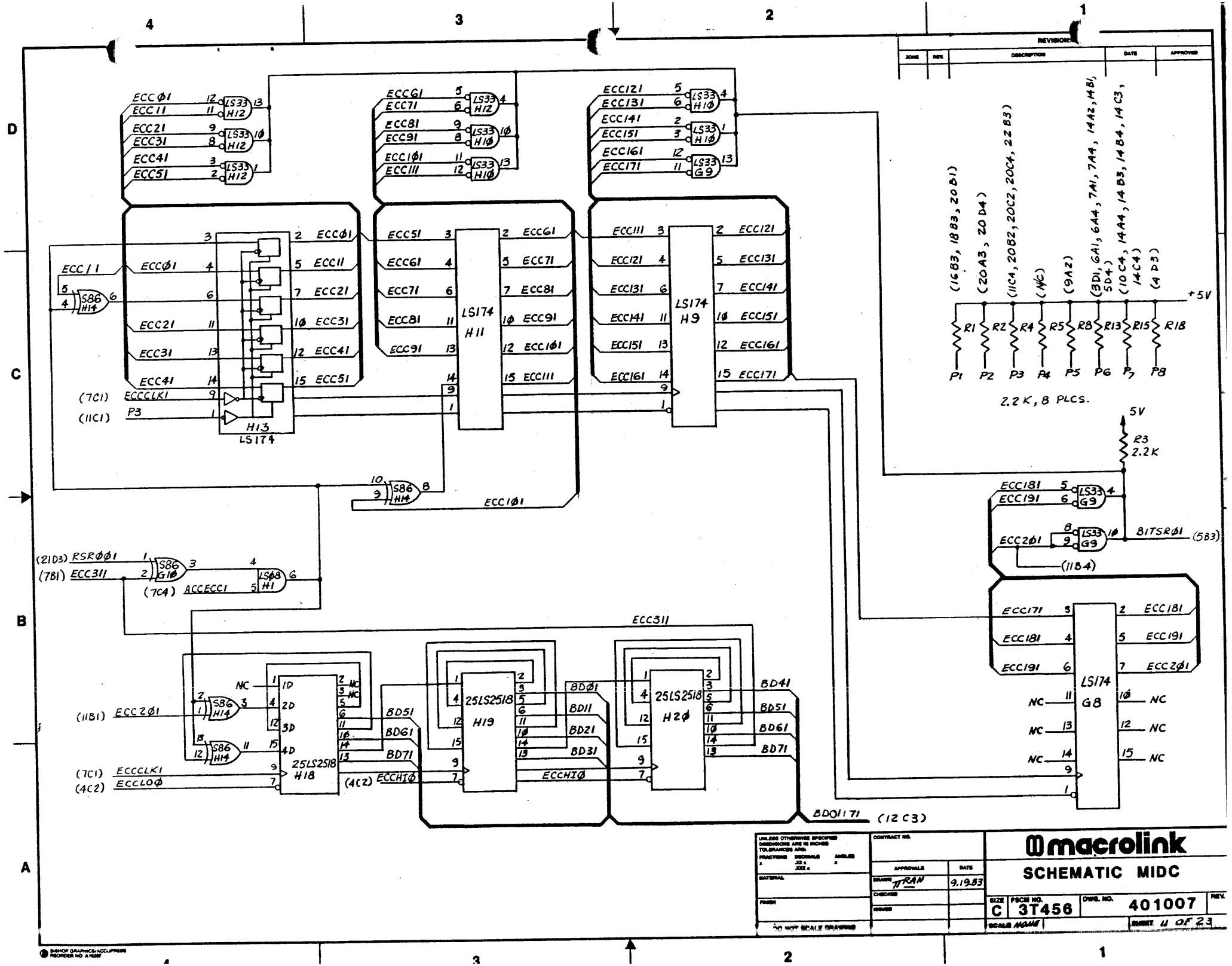
SCALE NONE | SHEET 5 OF 23

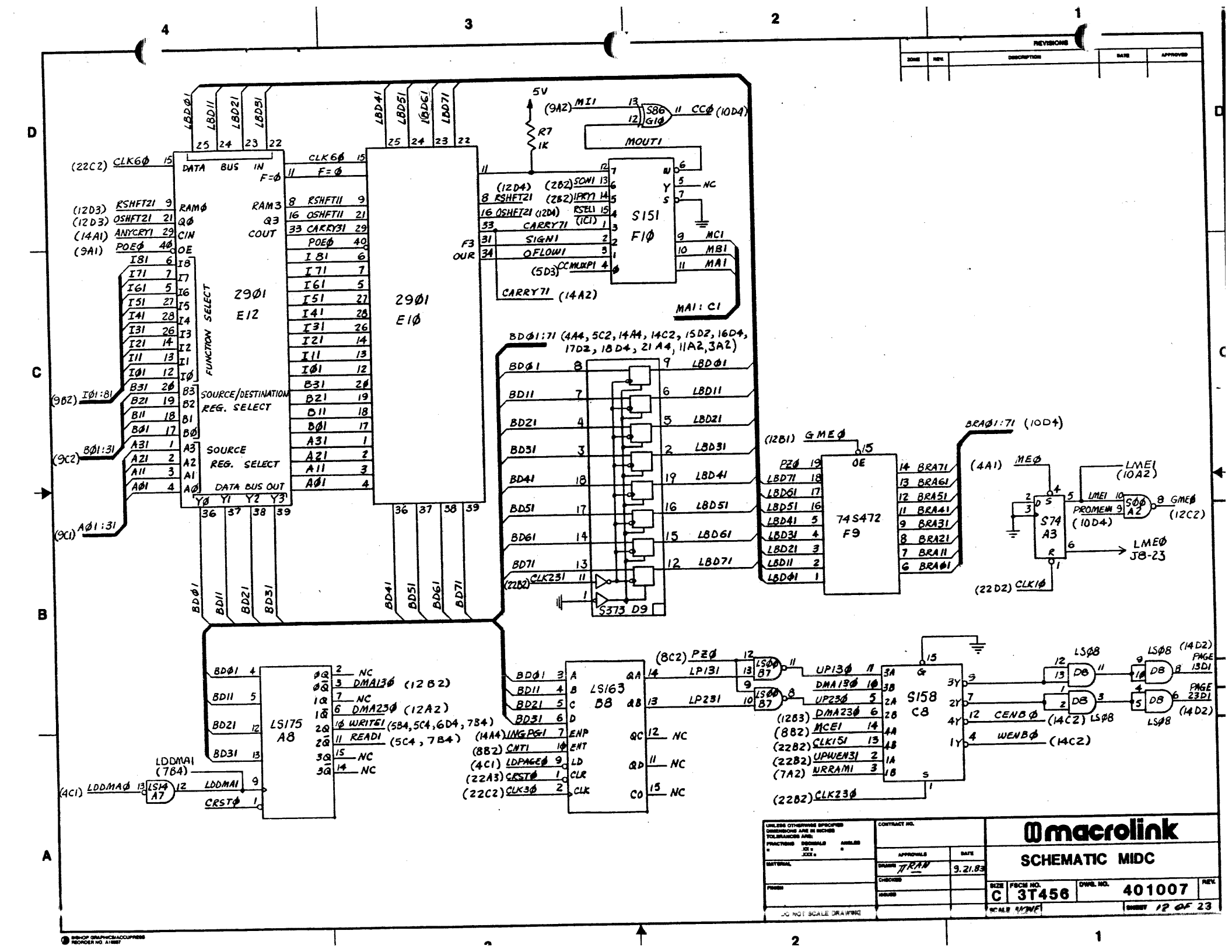


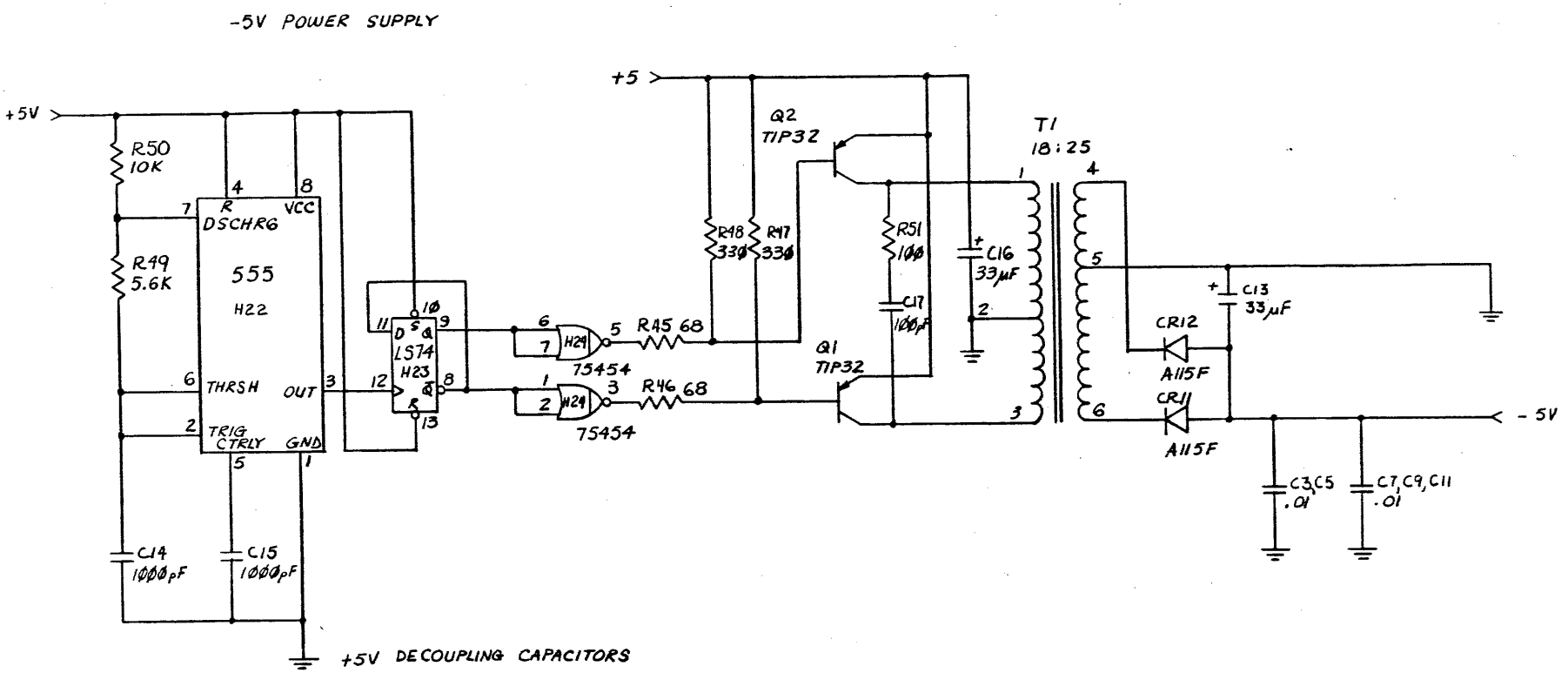
REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES	CONTRACT NO.	macrolink
MATERIAL	APPROVALS / DRAWN M.K.N.	DATE 9.19.83
FINISH	CHECKED	
DO NOT SCALE DRAWING	ISSUED	SCHEMATIC MIDC
	SIZE C	FSCM NO. 3T456
	DWG. NO.	401007
	REV.	
	SCALE NONE	SHEET 10 OF 23

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A16287


ECC01
ECC11
ECC21
ECC31
ECC41
ECC51
LS33 H12
ECC61
ECC71
ECC81
ECC91
ECC101
ECC111
LS33 H10
ECC121
ECC131
ECC141
ECC151
ECC161
ECC171
LS33 G9
LS174 H13
LS174 H11
LS174 H9
LS174 G8
S86 H14
S86 G10
S86 HH4
LS08 H1
(7C1) ECCCLK1
(11C1) P3
(2103) RSR0001
(781) ECC311
(704) ACCECC1
(11B1) ECC2001
(7C1) ECCCLK1
ECCL0Ø
(4C2) ECCHIØ
25LS2518 H18
25LS2518 H19
25LS2518 H20
BD01
BD11
BD21
BD31
BD41
BD51
BD61
BD71
BD0I171
(12C3)
(1683, 1883, 2081)
(20A3, 20D4)
(1104, 2082, 20C2, 20C4, 22B3)
(NC)
(9A2)
(3D1, 6A1, 6A4, 7A1, 7A4, 14A2, 14B1, 5D4)
(10C4, 14A4, 14B3, 14B4, 14C3, 14C4)
(4D3)
+5V
R1
R2
R4
R5
R8
R13
R15
R18
P1
P2
P3
P4
P5
P6
P7
P8
2.2K, 8 PLCS.
5V
R3
2.2K
BITSR0001
(5B3)
(1184)
REVISIONS
ZONE
REV.
DESCRIPTION
DATE
APPROVED
macrolink
SCHEMATIC MIDC
SIZE C
FSCM NO. 3T456
DWG. NO. 401007
REV.
SCALE NONE
SHEET 4 OF 23
DRAWN TRAN
9.19.83
CONTRACT NO.
APPROVALS
DATE
MATERIAL
FINISH
DO NOT SCALE DRAWING


REVISIONS
ZONE
REV.
DESCRIPTION
DATE
APPROVED
2901 E12
2901 E10
FUNCTION SELECT
SOURCE/DESTINATION REG. SELECT
SOURCE REG. SELECT
DATA BUS OUT
DATA BUS IN
S151 F10
74S472 F9
S373 D9
LS175 A8
LS163 B8
S158 C8
LS14 A7
BD0:7 (4A4, 5C2, 14A4, 14C2, 15D2, 16D4, 17D2, 18D4, 21A4, 11A2, 3A2)
MA1: C1
macrolink
SCHEMATIC MIDC
SIZE C
FSCM NO. 3T456
DWG. NO. 401007
REV.
SHEET 12 OF 23
DO NOT SCALE DRAWING
9.21.83



REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES °
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN TRAN	9.21.83
CHECKED	
ISSUED	

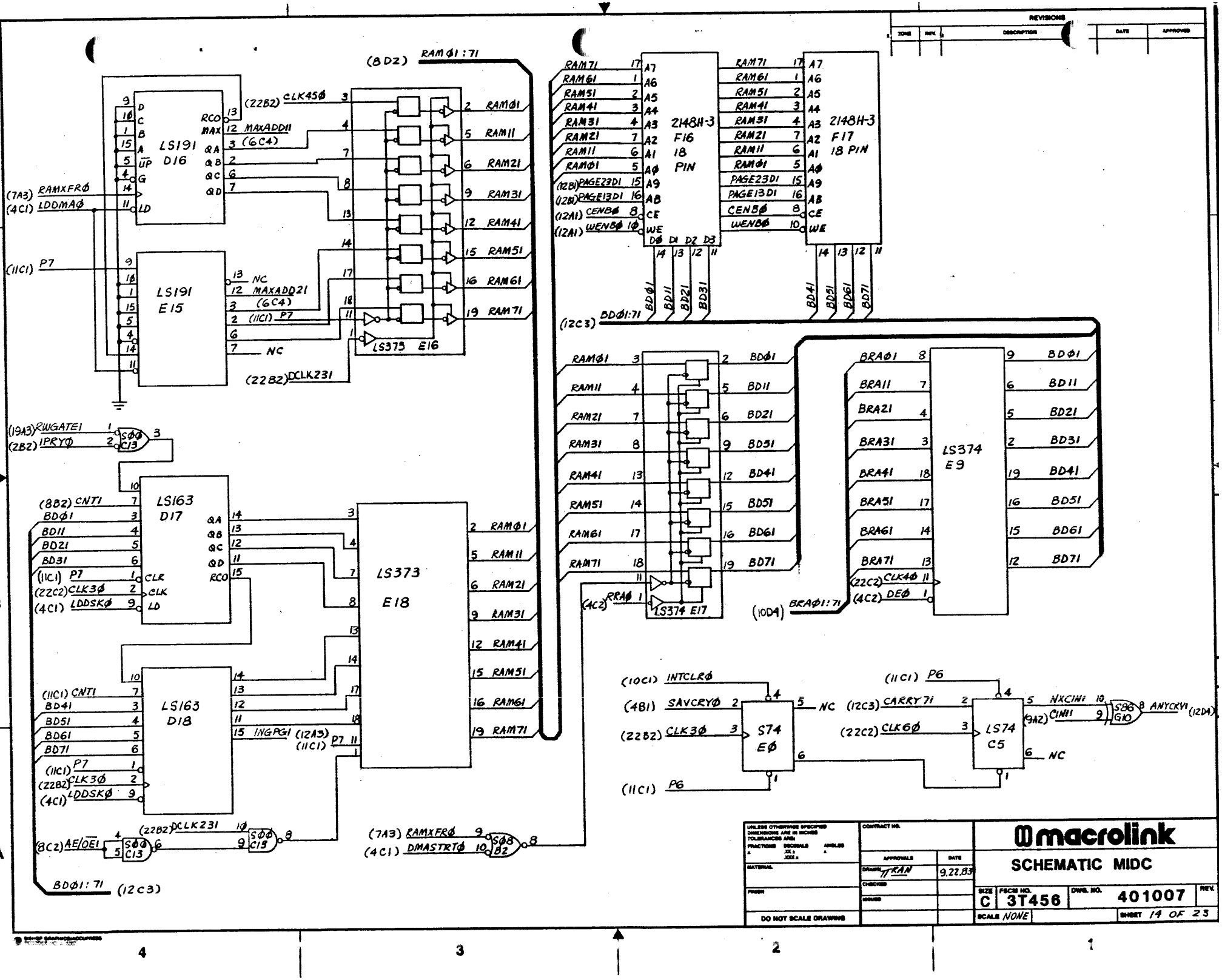
macrolink

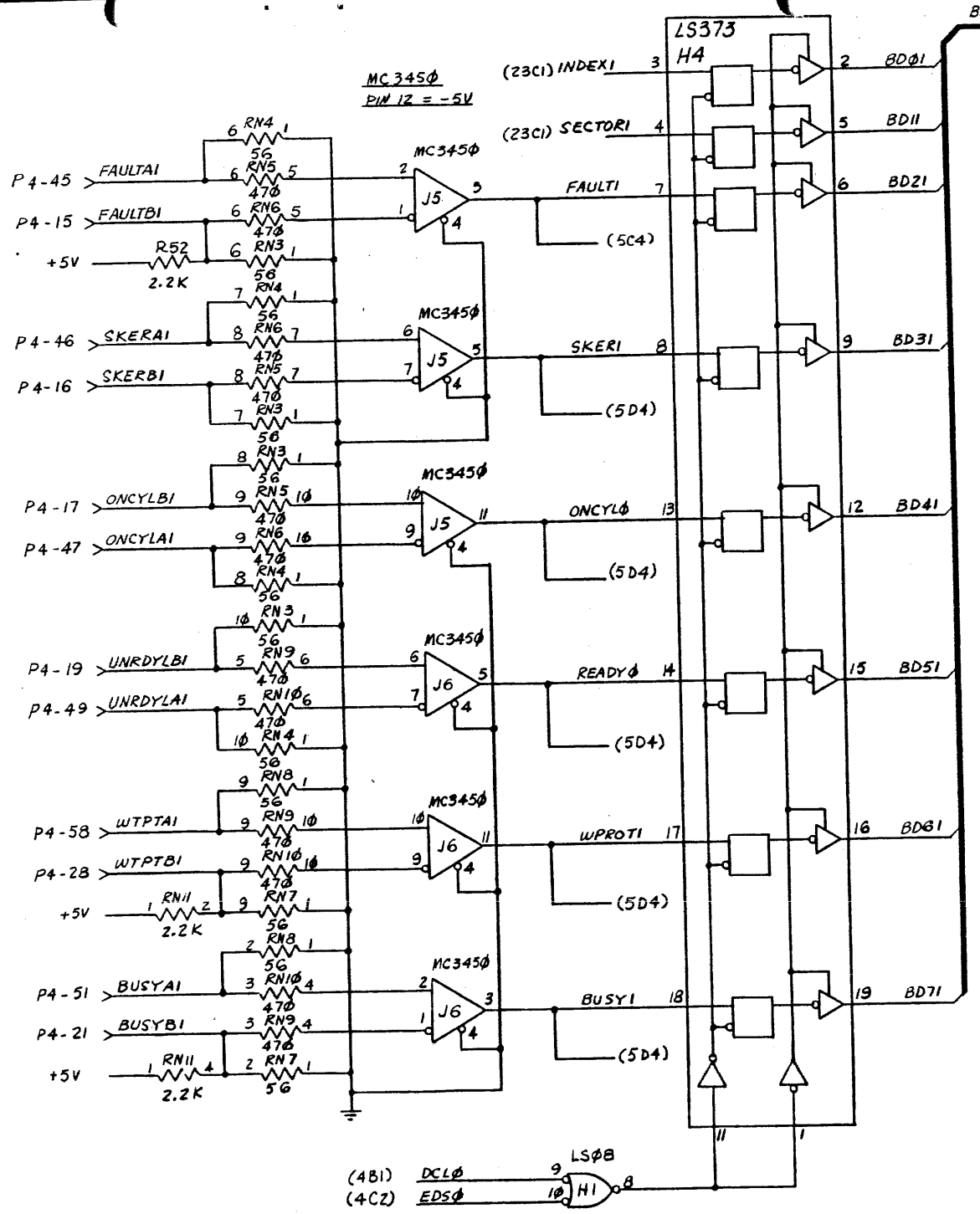
SCHEMATIC MIDC

SIZE C | FSCM NO. 3T456 | DWG. NO. 401007 | REV.

SCALE NONE | SHEET 13 OF 23

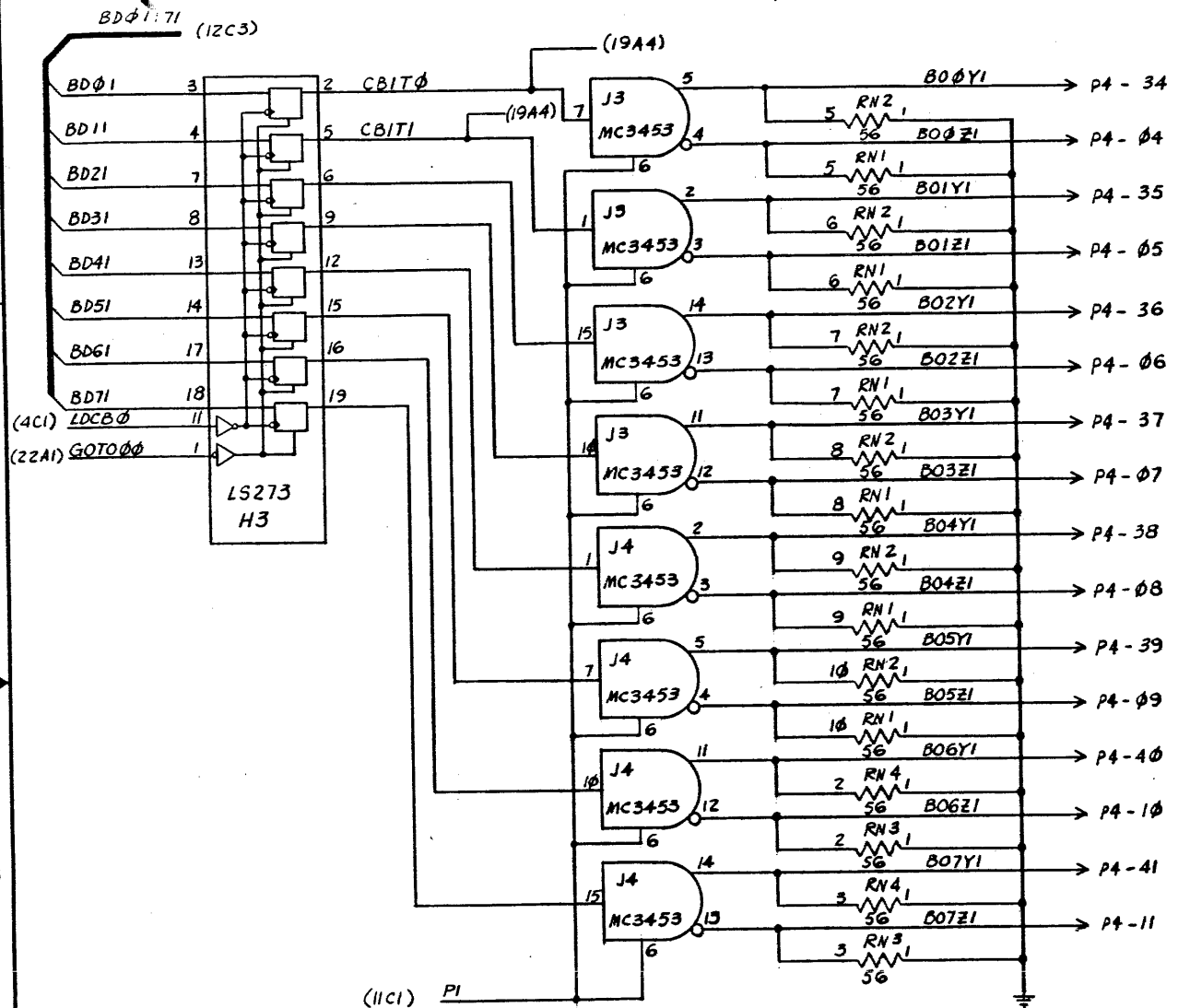
BISHOP GRAPHICS/ACCUPRESS REORDER NO. A16007


REVISIONS
ZONE
REV.
DESCRIPTION
DATE
APPROVED
(8D2) RAMØ1:71
LS191 D16
LS191 E15
LS375 E16
(22B2) CLK45Ø
(6C4) MAXADD11
MAXADD21
(11C1) P7
(22B2) DCLK231
(7A3) RAMXFRØ
(4C1) LDDMAØ
NC
2148H-3 F16 18 PIN
2148H-3 F17 18 PIN
(12B1) PAGE23D1
(12B1) PAGE13D1
(12A1) CENBØ
(12A1) WENBØ
BDØ1
BD11
BD21
BD31
BD41
BD51
BD61
BD71
(12C3) BDØ1:71
LS374 E17
(4C2) RRAØ
LS374 E9
(10D4) BRAØ1:71
(22C2) CLK4Ø
(4C2) DEØ
(19A3) RWGATE1
(2B2) IPRYØ
LS163 D17
LS163 D18
LS373 E18
(8B2) CNT1
(11C1) CNT1
(22C2) CLK3Ø
(4C1) LDDSKØ
(12A3) INGPG1
(8C2) AE/OE1
(4C1) DMASTRTØ
(10C1) INTCLRØ
(4B1) SAVCRYØ
(11C1) P6
S74 EØ
(12C3) CARRY7
(9A2) CIN11
(22C2) CLK6Ø
LS74 C5
NXCIN1
ANYCRY1
(12D4)
BDØ1:71 (12C3)
CONTRACT NO.
APPROVALS
DATE
DRAWN T RAN
9.22.83
CHECKED
ISSUED
MATERIAL
FINISH
DO NOT SCALE DRAWING
macrolink
SCHEMATIC MIDC
SIZE C
FSCM NO. 3T456
DWG. NO. 401007
REV.
SCALE NONE
SHEET 14 OF 23
4
3
2
1
D
C
B
A



REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

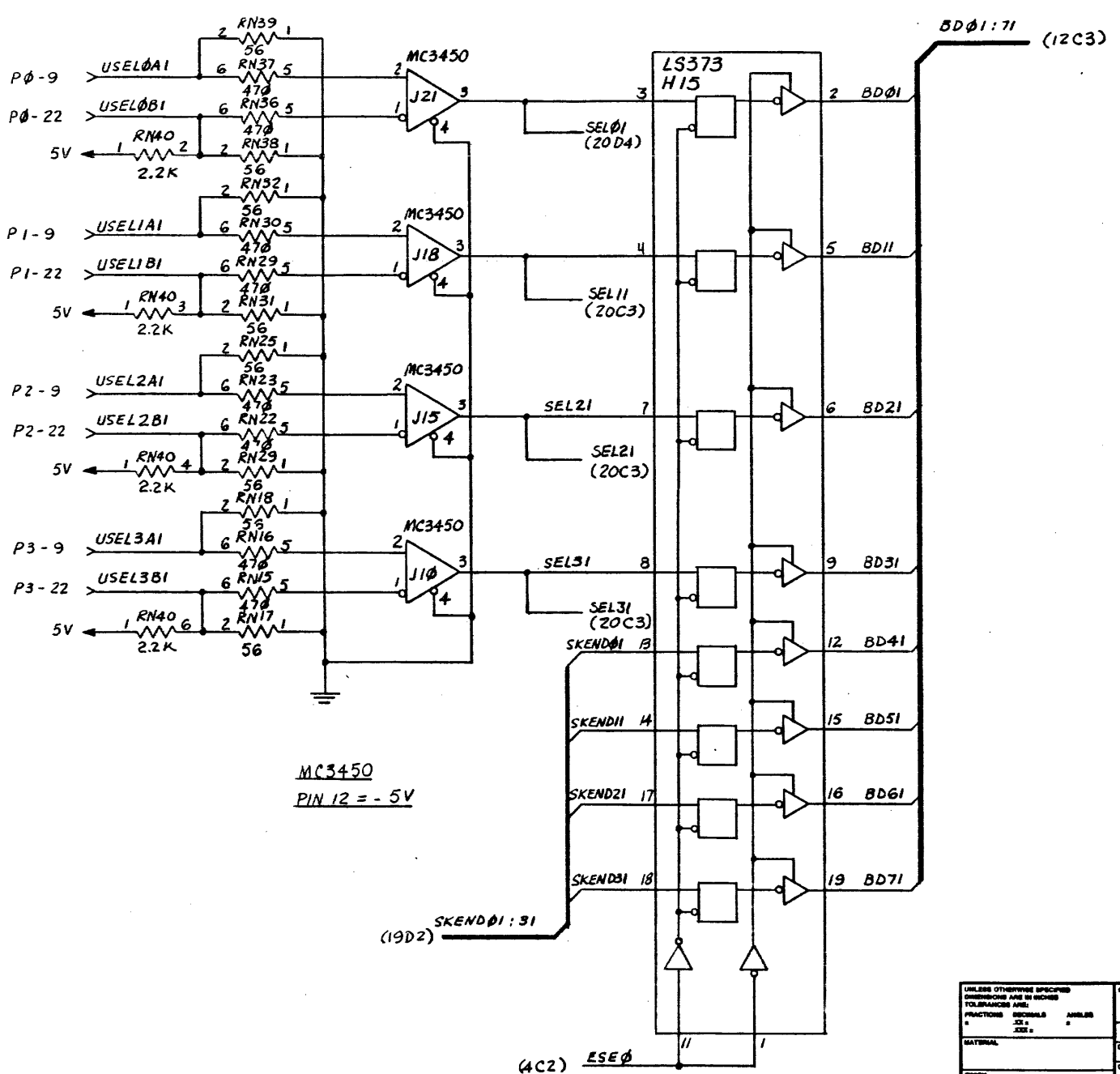
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ±	CONTRACT NO.	macrolink
MATERIAL	APPROVALS / DRAWN JT RAN	DATE 9.22.83
FINISH	CHECKED	SCHEMATIC MIDC
DO NOT SCALE DRAWING	ISSUED	SIZE C FSCM NO. 3T456 DWG. NO. 401007 REV.
		SCALE NONE SHEET 15 OF 23



MC3453
PIN 9 = -5V

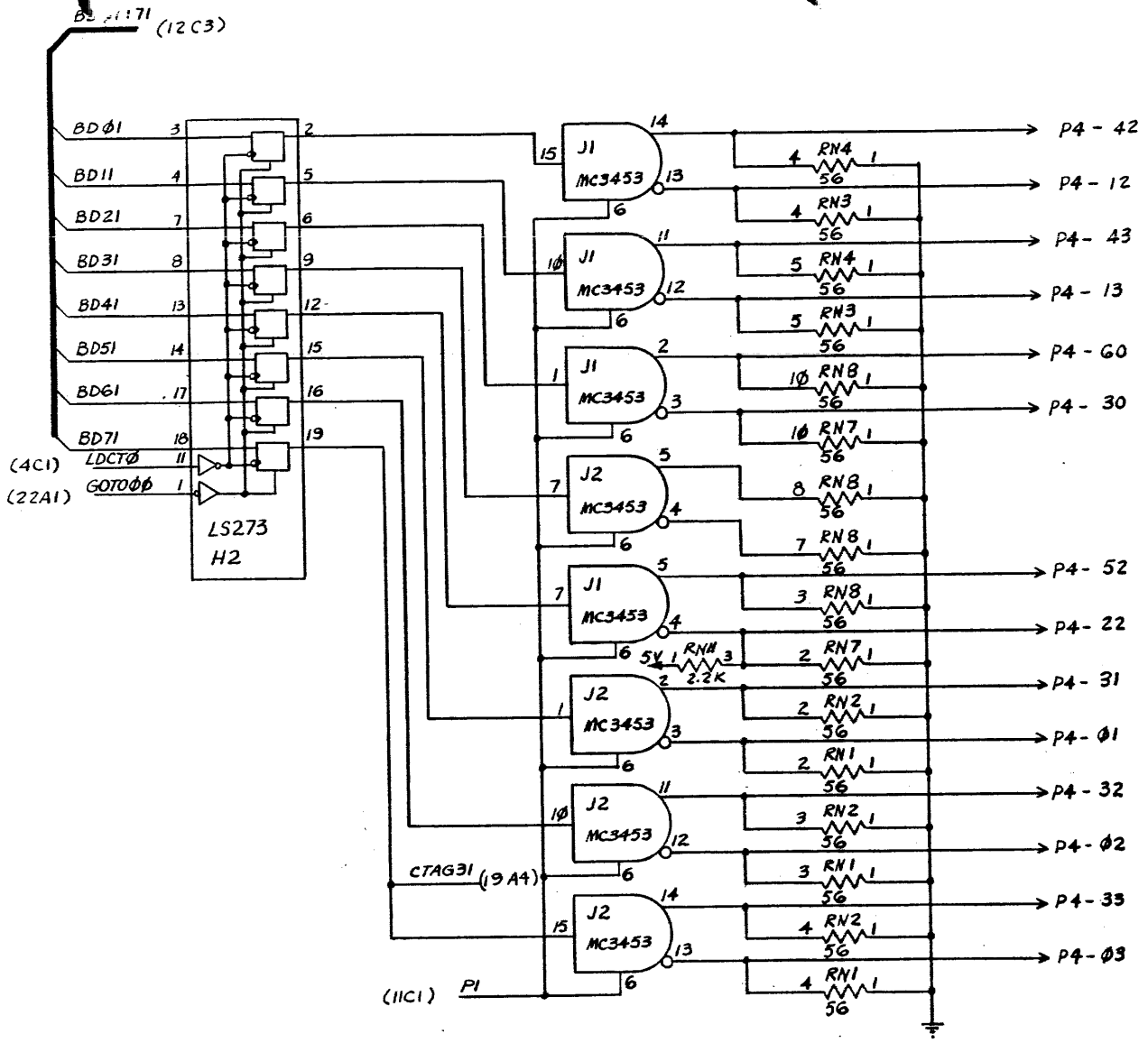
REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ±	CONTRACT NO.	macrolink
MATERIAL	APPROVALS / DRAWN TRAN	DATE 9.22.83
FINISH	CHECKED	SCHEMATIC MIDC
DO NOT SCALE DRAWING	ISSUED	SIZE C FSCM NO. 3T456 DWG. NO. 401007 REV.
		SCALE NONE SHEET 6 OF 29



REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	macrolink	
MATERIAL	APPROVALS / DRAWN TT RAN	DATE 9.22.83	SCHEMATIC MIDC
FINISH	CHECKED		SIZE C · FSCM NO. 3T456 · DWG. NO. 401007 · REV.
DO NOT SCALE DRAWING	ISSUED		SCALE NONE · SHEET 17 OF 23



MC3453

PIN Ø9 = -5V

REVISIONS

ZONE	REV.	#	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

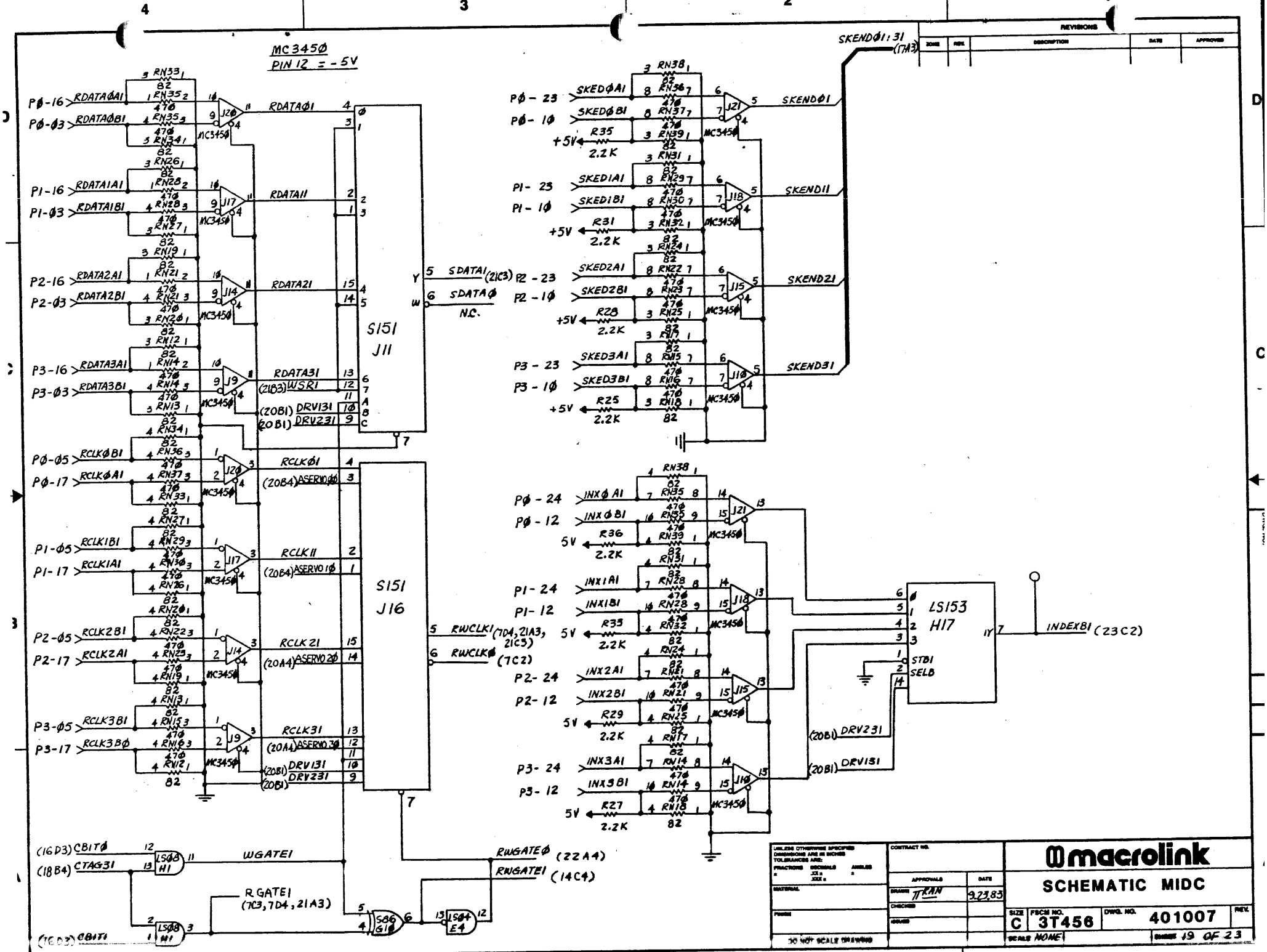
APPROVALS	DATE
DRAWN TRAN	9.23.83
CHECKED	
ISSUED	

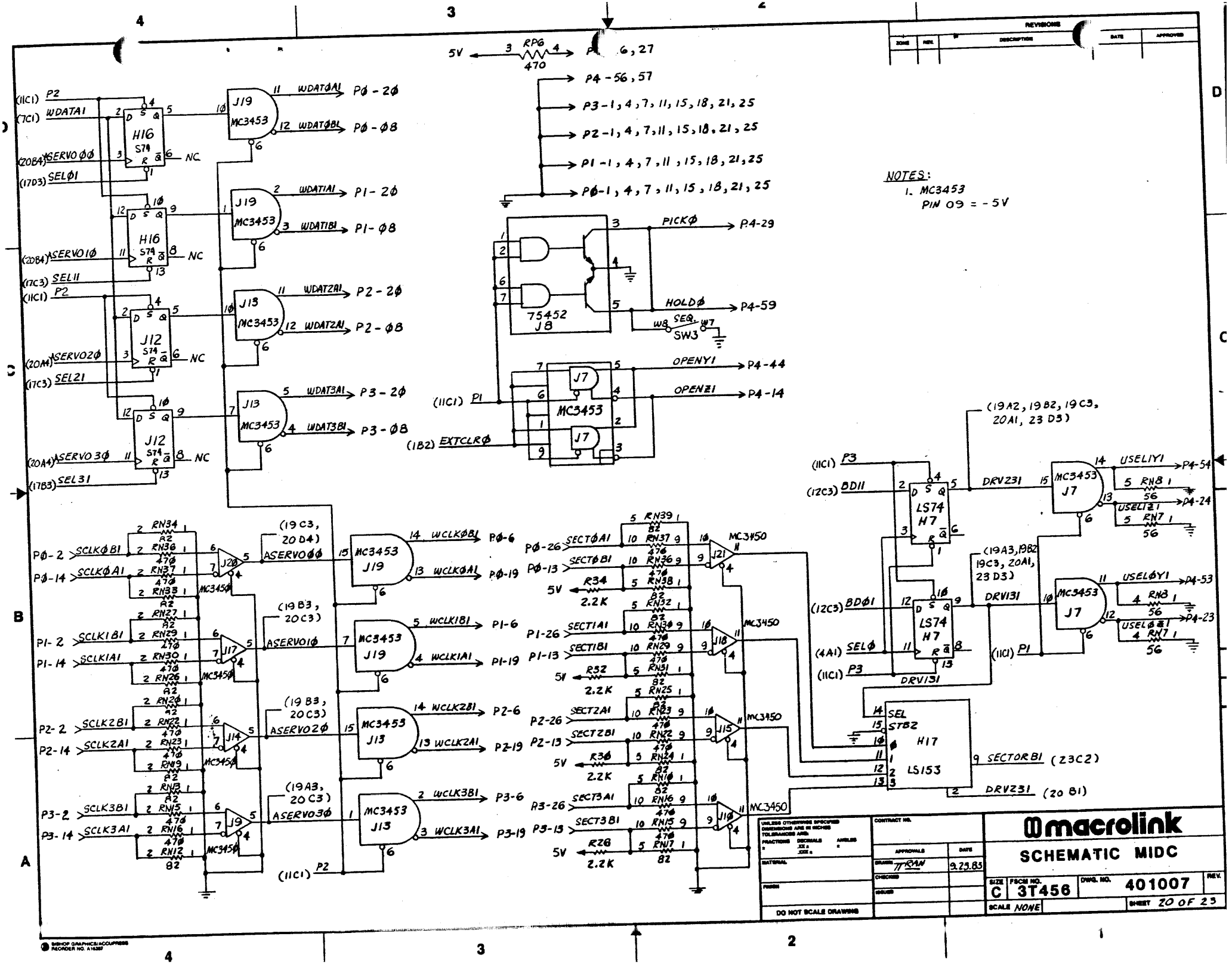
macrolink

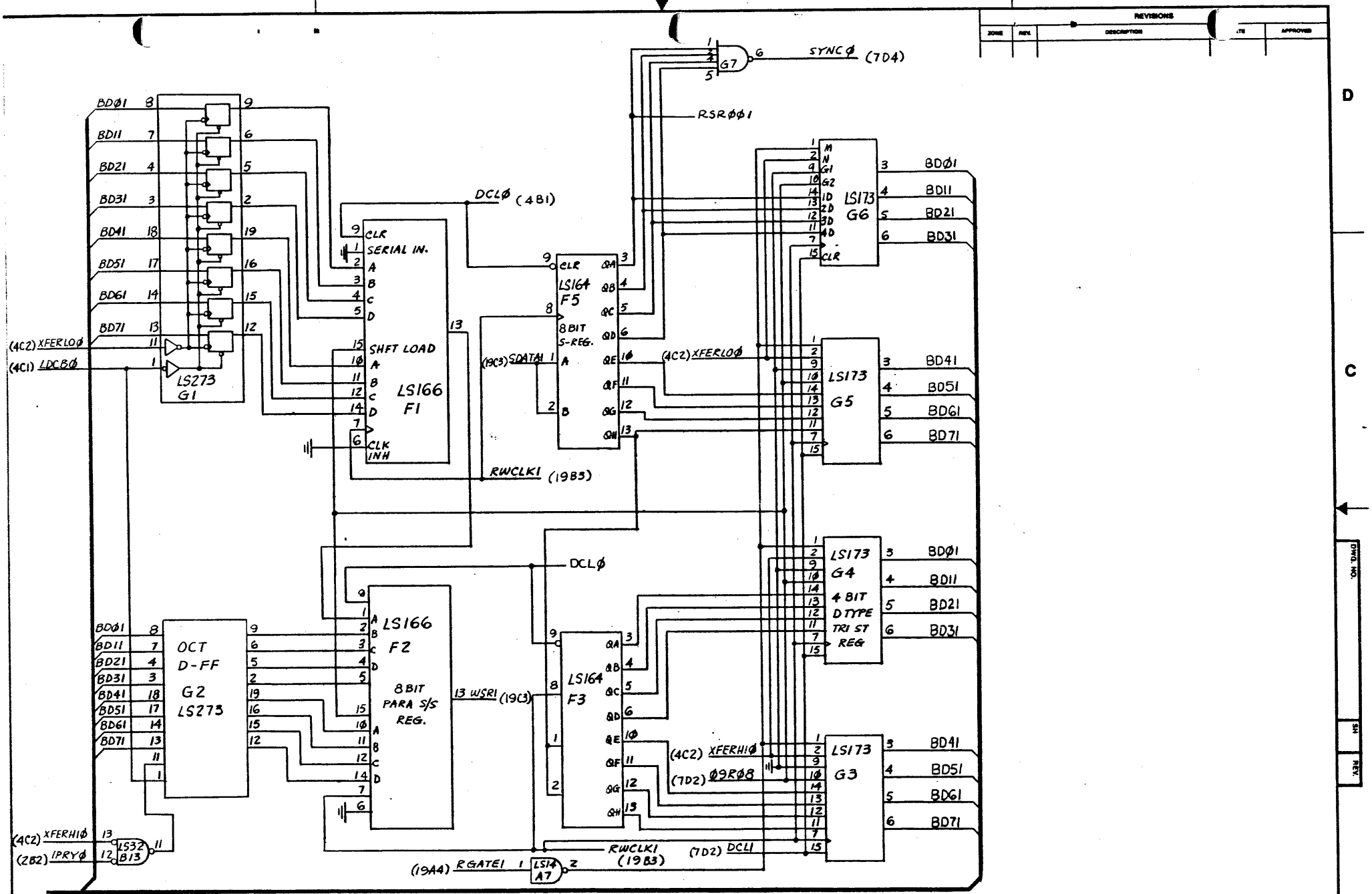
SCHEMATIC MIDC

SIZE C | FSCM NO. 3T456 | DWG. NO. 401007 | REV.

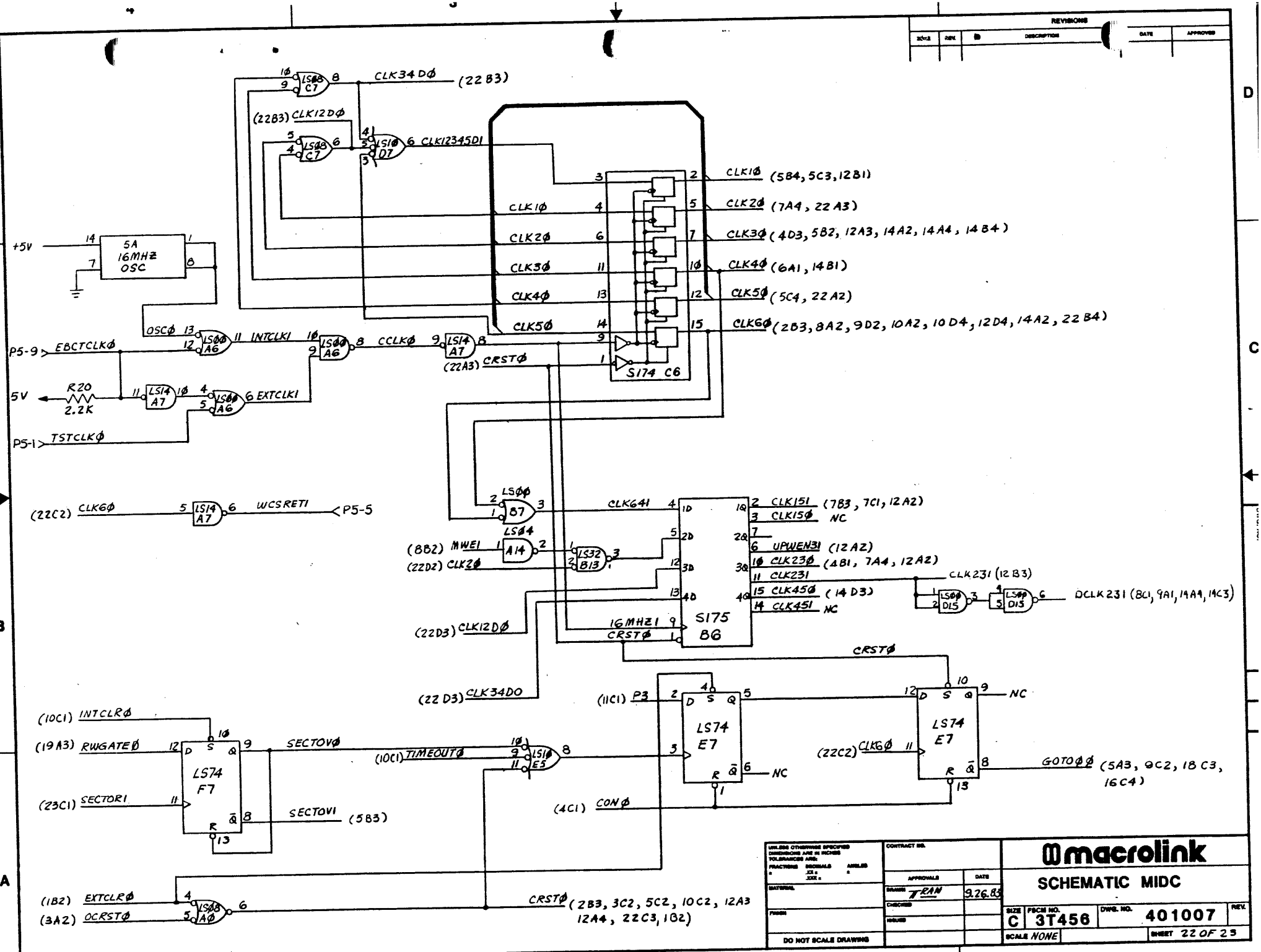
SCALE NONE | SHEET 18 OF 23

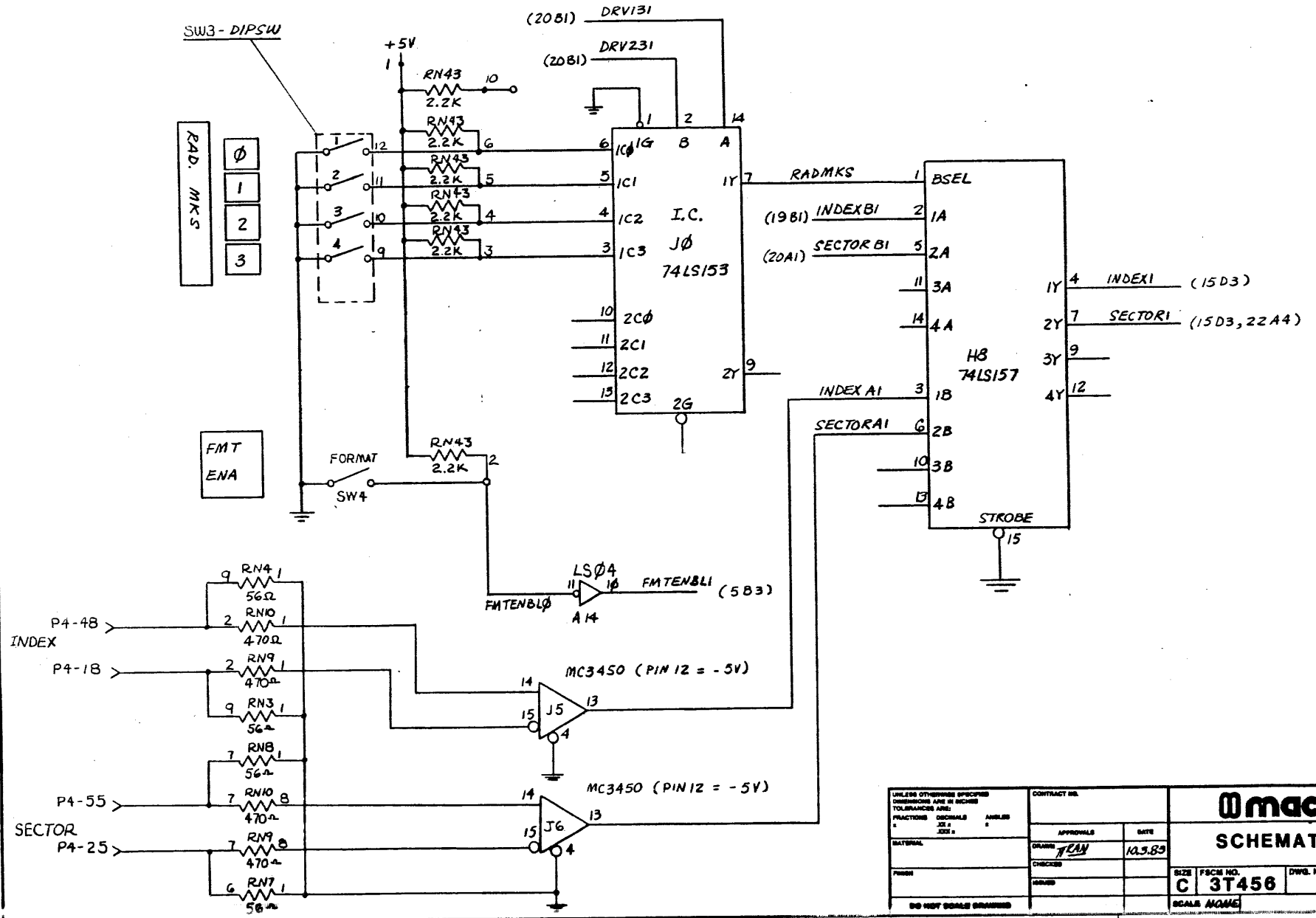

MC3450
PIN 12 = -5V
S151
J11
S151
J16
LS153
H17
SCHEMATIC MIDC
macrolink
SIZE C
FSCM NO. 3T456
DWG NO. 401007
SCALE NONE
SHEET 19 OF 23
DO NOT SCALE DRAWING


NOTES:
1. MC3453
PIN 09 = -5V
SCHEMATIC MIDC
macrolink
SIZE C
FSCM NO. 3T456
DWG. NO. 401007
REV.
SCALE NONE
SHEET 20 OF 23
DO NOT SCALE DRAWING
9.29.83
H16
J19
J12
J13
J8
J7
J20
J17
J14
J9
J18
J15
J10
H17
MC3453
MC3450
75452
LS74
LS153
SW3
RPG
470
2.2K
82
WDAT0A1
WDAT0B1
WDAT1A1
WDAT1B1
WDAT2A1
WDAT2B1
WDAT3A1
WDAT3B1
PICK0
HOLD0
OPENY1
OPENZ1
EXTCLR0
SERVO00
SERVO10
SERVO20
SERVO30
SEL01
SEL11
SEL21
SEL31
SCLK0B1
SCLK0A1
SCLK1B1
SCLK1A1
SCLK2B1
SCLK2A1
SCLK3B1
SCLK3A1
WCLK0B1
WCLK0A1
WCLK1B1
WCLK1A1
WCLK2B1
WCLK2A1
WCLK3B1
WCLK3A1
SECT0A1
SECT0B1
SECT1A1
SECT1B1
SECT2A1
SECT2B1
SECT3A1
SECT3B1
USELIY1
USELIZ1
USEL0Y1
USEL0Z1
DRV231
DRV131
BD11
BD01
SEL0
SEL
STBZ
SECTOR1B
P4-54
P4-24
P4-53
P4-23
P4-29
P4-59
P4-44
P4-14



DO NOT SCALE DRAWING	APPROVALS	DATE	macrolink
	DRAWN TRAN	9.23.83	SCHEMATIC MIDC
	CHECKED		SIZE C · FSCM NO. 3T456 · DWG. NO. 401007 · REV.
	ISSUED		SCALE NONE · SHEET 21 OF 23


CLK34DØ (22B3)
(22B3) CLK12DØ
CLK12345D1
CLK1Ø (5B4, 5C3, 12B1)
CLK2Ø (7A4, 22A3)
CLK3Ø (4D3, 5B2, 12A3, 14A2, 14A4, 14B4)
CLK4Ø (6A1, 14B1)
CLK5Ø (5C4, 22A2)
CLK6Ø (2B3, 8A2, 9D2, 10A2, 10D4, 12D4, 14A2, 22B4)
S174 C6
+5V
5A 16MHz OSC
OSCØ
INTCLK1
CCLKØ
P5-9 EBCTCLKØ
5V
R20 2.2K
EXTCLK1
P5-1 TSTCLKØ
(22A3) CRSTØ
(22C2) CLK6Ø
WCSRETI
P5-5
CLK641
CLK151 (7B3, 7C1, 12A2)
CLK15Ø NC
(8B2) MWE1
(22D2) CLK2Ø
UPWEN31 (12A2)
CLK23Ø (4B1, 7A4, 12A2)
CLK231
CLK231 (12B3)
CLK45Ø (14D3)
CLK451 NC
DCLK231 (8C1, 9A1, 14A4, 14C3)
(22D3) CLK12DØ
16MHZ1
CRSTØ
S175 B6
(22D3) CLK34DO
(10C1) INTCLRØ
(19A3) RWGATEØ
SECTOVØ
(10C1) TIMEOUTØ
(23C1) SECTOR1
SECTOVI (5B3)
(11C1) P3
LS74 E7
NC
(22C2) CLKGØ
GOTOØØ (5A3, 9C2, 18C3, 16C4)
(4C1) CONØ
(1B2) EXTCLRØ
(3A2) OCRSTØ
CRSTØ (2B3, 3C2, 5C2, 10C2, 12A3 12A4, 22C3, 1B2)
REVISIONS
DESCRIPTION
DATE
APPROVED
DO NOT SCALE DRAWING
macrolink
SCHEMATIC MIDC
SIZE C
FSCM NO. 3T456
DWG. NO. 401007
REV.
SCALE NONE
SHEET 22 OF 25



REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

CONTRACT NO.		
APPROVALS	DATE	
DRAWN TAN	10.3.83	
CHECKED		
ISSUED		

macrolink

SCHEMATIC MIDC

SIZE	FSCM NO.	DWG. NO.	REV.
C	3T456	401007	

SCALE NONE SHEET 23 OF 23

The MIDC TAPE contains Bootable Core images of the diagnostics.

The 8/32 LSCI does not appear to be able to Load them directly. Therefore A boot program (BOOT32) must be first loaded using the 50 sequence. The BOOT32 Loader is on the PE Distribution Tape for OS/32 R 7.2 & others.

May not need BOOT 32 for other Machines.

See Operators manual –
Section 2 "Loading OS/32"

See OS/32 7.2 "Software Packaging Information"
Section 7.

See MACROLINK IDC
Controller Manual

FILE MARKS	0	MIDC FAST FORMATTER R01
	1	MIDC DISC TEST VER. B
	2	IDC " TEST
	3	IDC FORMATTER
	4	MIDC FAST FORMATTER
	5	MIDC DISC TEST VER. B

INSTRUCTIONS TO LOAD MIDC FORMATTER AND/OR TESTS FROM 1600 BPI TAPE ON 8/32

1. MOUNT P-E 800 BPI OS/32 DISTRIBUTION TAPE ON 800 BPI DRIVE - this tape has BOOT32!

2. MOUNT MIDC TAPE ON 1600 BPI DRIVE

3. SET UP MEMORY

```
78:   85 A1
7A:   C5 41
7C:   C5 F1
7E:   0000

50:   D500
52:   00CF
54:   4300
56:   0080

84:   5000
86:   6000

30:   0000
32:   0000
36:   0000
38:   0000
```

C5 Seq Dev & Command to 800
Boot32 dev addr dev. code 1600
Boot32 dev addr selch 1600
file marks to skip on MIDC tape

} 50 sequence

} ILLEGAL INSTR or POWER FAIL VECTOR

TURN LSU OFF! PRESS INI
START AT LOC 50. (DTA, 50, ADR, RUN)