ADM-2

Maintenance Manual

PREFACE

This manual contains installation, maintenance, operation, and related theory necessary to maintain and troubleshoot the ADM-2 Interactive Display Terminal. A brief description of the unit and its options are included in the manual to assist the service technician in maintaining the equipment. For additional information on the ADM-2, write:

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714 N. Brookhurst St.
Anaheim, CA 92803

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SECTION ONE
INTRODUCTION

The ADM-2 Interactive Display Terminal is a microprogram-controlled device that provides a means of communicating with a remote computer and can offer the user the ability to do some limited independent processing at the display area.

The terminal is a complete self-contained unit. Included within the terminal's lightweight housing is a fan, cabling, and all required hardware. The keyboard is housed in a separate enclosure but can be mounted with the ADM-2 terminal, if desired. The ADM-2 terminal consists of four main functional sections, which are:

- Cathode Ray Tube (CRT) display and monitor
- Circuit Board with microcontroller, memory and logic
- Power Supply
- Keyboard with key encoding electronics.

Figure 1-1 illustrates the functional makeup of the ADM-2.

An ADM-2 character page (full screen) contains 24 character lines, each with 80 character positions, providing a total display capacity of 1920 characters per page. Display fields are refreshed at a rate set by a crystal oscillator synchronously with 60 Hz input power in the standard terminal. This rapid refresh rate generates flicker-free images and high contrast display even in bright light.

The ADM-2 transmits data to the computer (or data set) via a standard RS-232-C data interface. The standard code for ADM-2 transmissions is a ten-bit asynchronous serial ASCII code with even parity.

The ADM-2 can emulate an ADM-1 by using special sequence codes designated for this purpose. When emulating an ADM-1, with a serial printer, unformatted print must be specified by the program.

Optional equipment available with the ADM-2 include:

- Line Printer interface
- Polling interface
- 20ma Current Loop interface
- RS-232-C Extended interface
- Optional word structures in addition to the ten-bit code
- Composite Video.

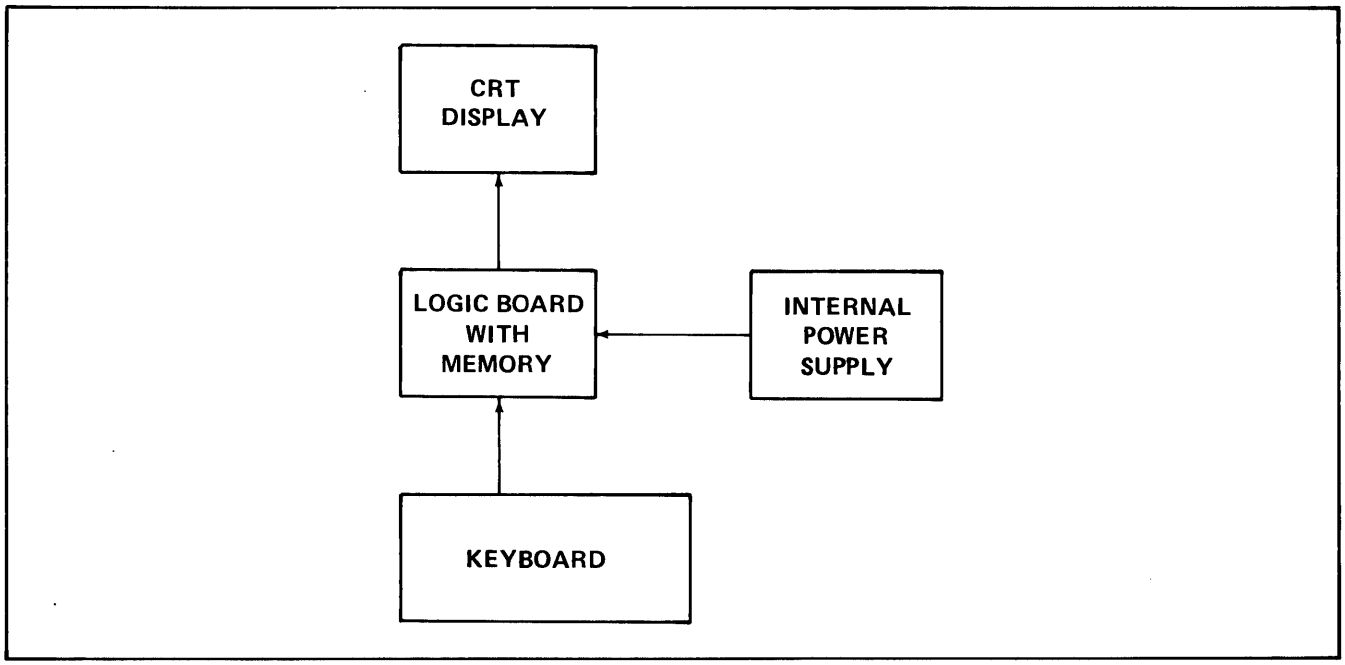


Figure 1-1. ADM-2 Functional Makeup

1.1 USE AND CAPABILITIES

The ADM-2 consists of four main sub-units: the monitor and display, keyboard, logic board, and power supply. These sub-units, along with their capabilities, are described below.

The monitor is a solid-state, all transistorized unit featuring printed circuit board construction. The monitor is used to display alphanumeric data. All data characters and controls may be entered on the screen from the keyboard or received from a remote computer. Reverse image display is automatically enabled any time the cursor is positioned over data. Display fields may be set to: blink, protect against overwriting, or show blank fields (for security reasons). The display also contains eight status indicators.

The standard ADM-2 character set contains 96 ASCII characters. A complete ADM-2 standard character set is depicted in Figure 1-2. Control characters can be displayed if transmission from computer or keyboard is preceded by an ASCII ESC U code sequence, setting the program mode. There are 32 control characters in the standard character set.

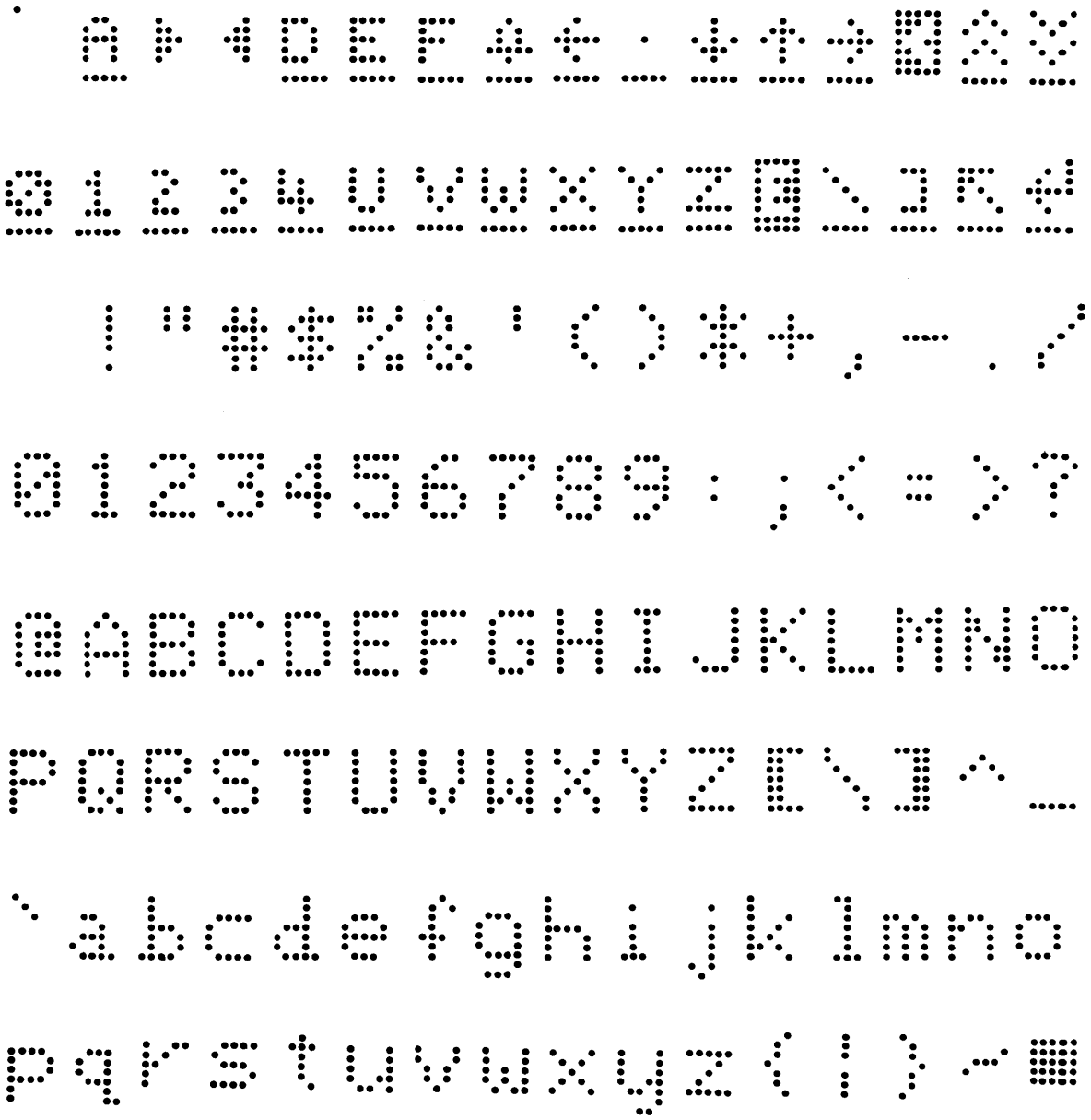


Figure 1-2. ADM-2 Character Format (By Ascending ASCII Codes)

The ADM-2 keyboard contains 118 keys. A rollover feature has been incorporated in the keyboard to protect against mis-keying. (If a key is depressed before a previously depressed key is released, the second key code cannot be transmitted until the first depressed key has been released.) The keyboard can be removed from the ADM-2 display unit enclosure and placed up to five feet away. Figure 1-3 illustrates the standard ADM-2 keyboard.

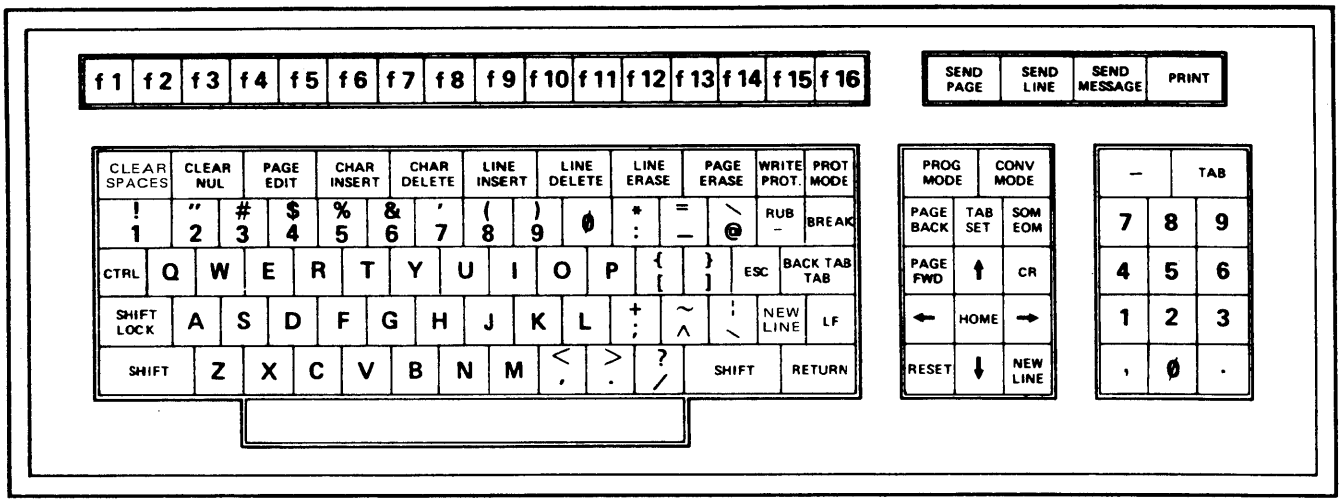


Figure 1-3. ADM-2 Keyboard

All ADM-2 functions are controlled by a single printed circuit board. This is the only logic board in the ADM-2, with the exception of the power supply assembly. The logic board contains the microcontroller, display memory, logic electronics, transmission rate control, and data interface electronics. Figure 1-4 shows the ADM-2 printed circuit board.

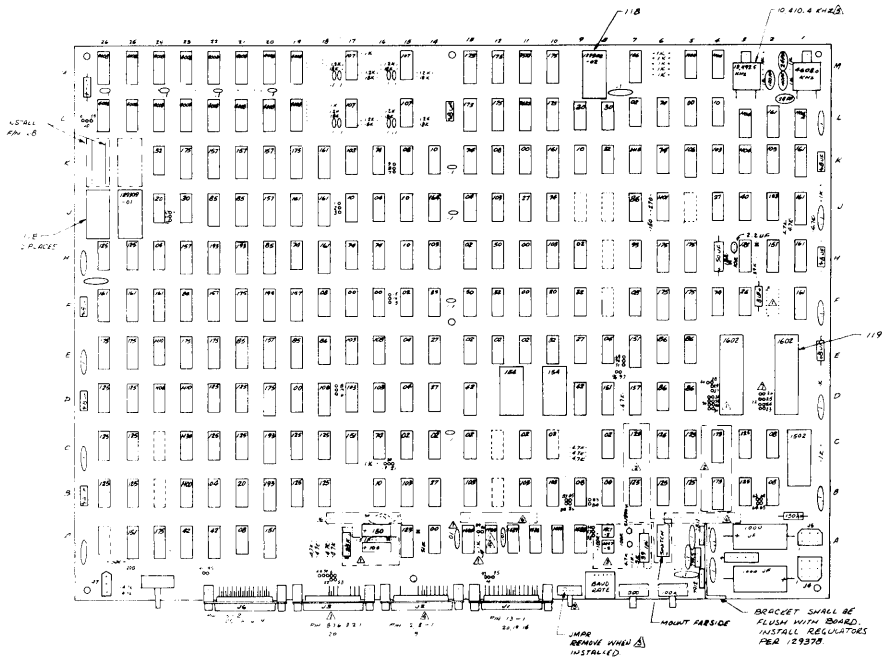


Figure 1-4. ADM-2 Printed Circuit Board

The ADM-2 power supply provides the main logic board with +5V DC. The power supply is rated at 12 amps and contains an internal voltage regulator, current limiter, and overvoltage protection. The power supply is capable of supplying the display terminal functions with a load regulation of .075%. The power supply is shown in Figure 1-5.

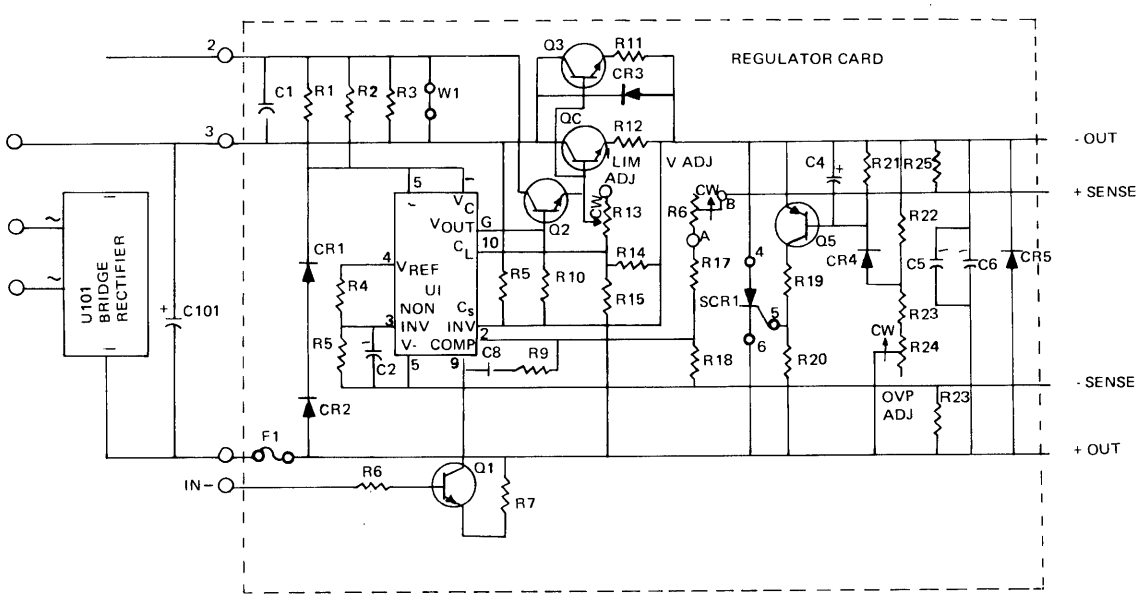


Figure 1-5. ADM-2 Power Supply

1.2 PHYSICAL DESCRIPTION AND SPECIFICATIONS

The ADM-2 Interactive Display Terminal is shown in Figure 1-6. The dimensions are noted in the figure.

Table 1-1 lists the specifications of the ADM-2. Table 1-2 lists the monitor specifications of the ADM-2 unit.

Figure 1-6. ADM-2 Interactive Display Terminal

Table 1-1. ADM-2 Specifications

GENERAL	
Input Power:	
Standard	115V, 60Hz
Optional	230V, 50Hz
Input Connector Type	Receptable, molex number 03-06-1041 Unit mating plug, molex number 03-06-2041
Operating Temperature	5° to 50° C (41° to 122° F)
Storage Temperature	-10° to 65° C (50° to 149° F)
Humidity	5% to 80% non-condensing
Altitude	Operates up to 10,000 feet
Dimensions (overall)	12½"H x 20½"W x 24"L
Weight	50 lbs
DISPLAY	
Lines of Characters	24
Characters per Line	80
Character Positions	1920 standard
Screen Phospher	White (P4)
Face Plate	Etched
Refresh Rate	60 pages per second
Status Displays	8 (with printer)
Control Character Display	32
Blinking Field Rate	4 per second
Page Roll	From bottom to top
Security Fields	Display is suppressed (no display)
Protected Fields	Reduced intensity for write protect
Cursor:	
Format	Reverse video block
Controls	Forespace, backspace, upline, downline, new line, return, home, tab, back-tab, position addressing, position reading
Screen	12" (diagonally); rectangular CRT with etched non-glare surface
Resolution (TV lines)	900 at 40 fl. (center) 800 at 40 fl. (corner)
Display Format:	
Standard	1920 characters 24 lines of 80 characters
Character Set:	
Generated	128 ASCII characters (upper/lower case, numeric, punctuation, control)
Displayed	64 ASCII characters (upper case, numeric, punctuation)
Character Generation:	5" by 7" dot matrix
Height	0.18"
Width	0.075"
Cursor	7" by 9" rectangle Homes to upper right
Refresh Rate:	
Standard	60Hz
Optional	50Hz
Dimensions (display)	12½"H x 20½"W x 17"L

Table 1-1. ADM-2 Specifications (Continued)

MEMORY

Storage Capacity	1920 characters
Security Locations	Display suppressed
Control Character Storage	In program mode, direct from keyboard or computer
Protected Fields	Character protect bit enabled

KEYBOARD

Construction	Solid-state logic; similar to a teletypewriter layout (data keys); separate unit with 5' cable
Character & Control Keys	68
Cursor & Format Keys	14
Numeric Keys Pad	14
Function Keys	16
Transmission Send Control Keys	Page, line, message, print
Interlocking Feature	Rollover protection of keys
Key Operation Force	2 ounces
Lighted Mode Keys	Shift lock, prot mode, write protect, program, conversation, page edit
Dimensions (keyboard)	3½"H x 20½"W x 9"L

COMMUNICATIONS

Interface:	
Standard	EIA RS-232-C
Optional	20 milliamp current loop; Extended RS-232-C port
Data Transfer Rates:	
Standard	110, 150, 300, 600, 1200, 2400, 4800, and 9600 baud
Optional	1800 baud
Send/Receive Modes	Full duplex, half duplex, or block (line, page, or message, all or foreground)
Optional Interface Mode Operation	Polling
Code for Transmission	Asynchronous ASCII
Word Format:	
Standard	10-bit code
Optional	9, 11, or 12-bit code
Parity:	
Standard	Even
Optional	Odd, fixed bit or none

DATA EDITING CONTROLS

Keyboard Editing:	
Character edit	Type over, insert, delete
Line edit	Insert, delete, erase to end of line
Page edit	Clear all or foreground to nulls or spaces; erase to end of page (replace all or foreground with nulls or spaces)
Computer Controlled Editing	All of above with receipt of an ESC sequence.

Table 1-2. ADM-2 Monitor Specifications

GENERAL

Temperature:	
Operating range	5° to 55° C (41° to 131° F)
Storage range	-40° to 65° C (-40° to 149° F)
Humidity	5% to 80% non-condensing
Input Voltage	105V to 130V rms (120V nominal)
Input Frequency:	
Standard	60Hz
Optional	50Hz
Output Voltages	+15V DC (short circuit protected)
	+12KV DC; 12.6V rms
Input Power	24 watts (nominal)
X-Ray Radiation	Comply to DHEW rules—42—CFR—part 78

CONTROLS

Contrast	500 ohm potentiometer carbon composition; appx. 1/8 watt
Brightness	100 kilohm potentiometer; appx. 1/8 watt

ELECTRICAL

Input Impedance:	Minimum Shunt Resistance	Maximum Shunt Capacitance
Video input	3.3K ohms	40 PF
Vertical drive input	3.3K ohms	40 PF
Horizontal drive input	470 ohms	40 PF

Video Amplifier:

Bandwidth	12MHz (-3db)
Rise and fall times (10% to 90% amplitude)	Less than 35 nsec (linear mode)
Storage time	15 nsec, maximum (linear mode)

Retrace and Delay Times:

Vertical	900 usec retrace, maximum
Horizontal	7 usec retrace plus 4 usec delay, maximum

INPUT DATA REQUIREMENTS

Input Connector	Printed circuit board edge connector (Viking number 2VK10X/1-2 or Amphenol number 225-21031-101)

Pulse Rate or Width:

Video	Pulse width = 100 nsec or greater
Vertical drive signal	Pulse rate=47 to 63 pulses per second
Horizontal drive signal	Pulse rate = 15000 to 16500 pulses per second

Amplitude:

Video low	0.0 to 0.4V
Video high	4V (± 1.5V)

Signal Rise and Fall Times (10% to 90% amplitude):

Video	Less than 20 nsec
Vertical drive signal	Less than 100 nsec
Horizontal drive signal	Less than 50 nsec
Input Signal Format	Shown in Figure 7-2

GEOMETRIC DISTORTION

The perimeter of a full field of characters will be an ideal rectangle to within ±1.5% of the rectangle height.

1.3 OPTIONS

The following options are available for use with the ADM-2:

- A **serial printer interface** which allows the ADM-2 to control a serial character printer using RS-232-C standards. Operation of the printer may be initiated from the keyboard or remotely from the computer. A number of baud rates are available to accommodate various printers.

- A **polling interface** is available which allows the ADM-2 to act as a polling terminal in a multipoint communications network. When the polling option is present, the ADM-2 is prevented from initiating transmissions except under control of the network control center. All message transmission is between the network control center and the selected terminal or terminals. Operation of the communications network and interaction of the ADM-2 terminals with the center is controlled entirely by a polling/addressing dialog initiated by the center.

- The ADM-2 comes with a standard **RS-232-C data interface.** An extension for this interface is available for driving a printer or other device with EIA RS-232-C voltage level signals. This interface appears to the auxiliary device as though the terminal were a data set.

- A **20ma current loop interface** is also available for the ADM-2. This interface complements the standard RS-232-C interface that comes with the ADM-2.

- The ADM-2 is equipped for **standard 60 Hz, 110 volt AC power.** 50 Hz and/or 230 volt AC power input are easily accommodated. The monitor supply transformer, power supply transformer, and input voltage connections to the main logic board can be reconnected for 230 volt AC.

- A **word structure option** allows the ADM-2 to transmit and receive data characters in any one of the asynchronous character formats shown in Figure 1-7. This option permits the codes shown to be used in addition to, and not in place of, the ADM-2 standard ten unit code. Codes are selected by re-strapping the synchronous receiver/transmitter chip on the main logic board.

- The **composite video option** converts video and sync signals from ADM-2 terminals to a composite video output through the use of an internal piggyback board. Data is then transmitted to a compatible composite video monitor located up to 1000 feet away through a single coaxial cable.

  The composite video option provides the capability of locating the control terminal in an area separate from the electronics, making it ideal for such applications as airport control towers, emergency communications centers, hospital areas, and other environments in which it is necessary to locate the terminal some distance from the computer.

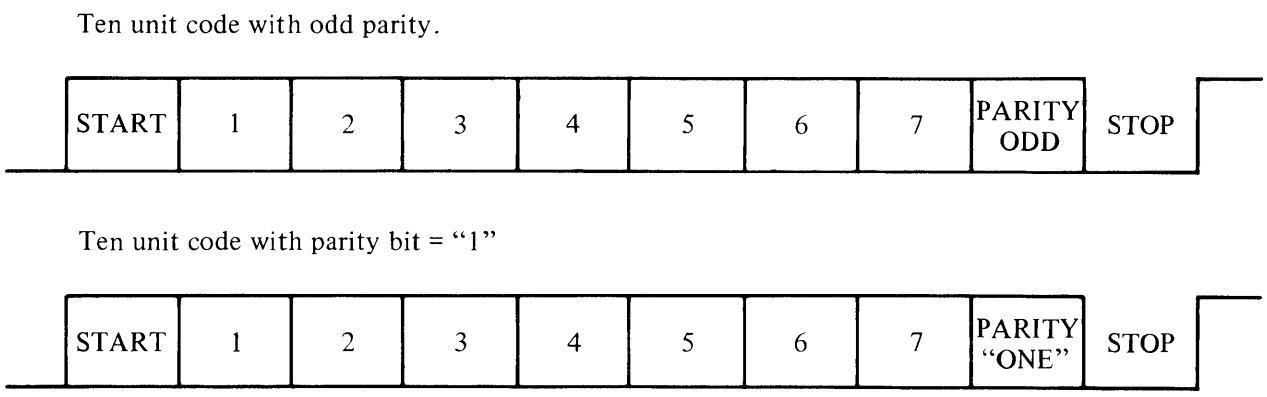
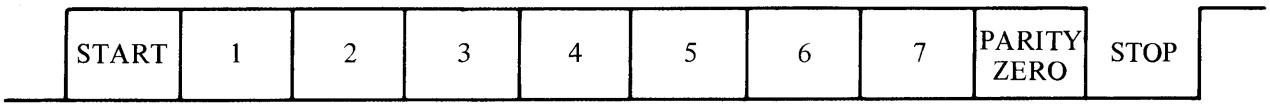
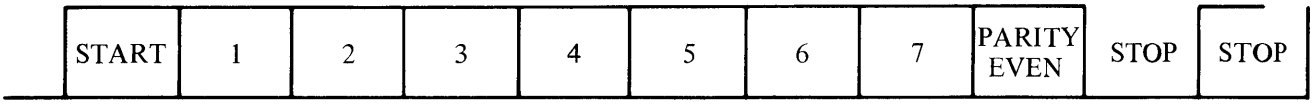


Figure 1-7. Word Format Codes

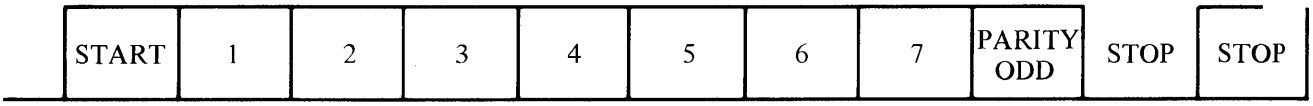
Ten unit code with parity bit = "0"



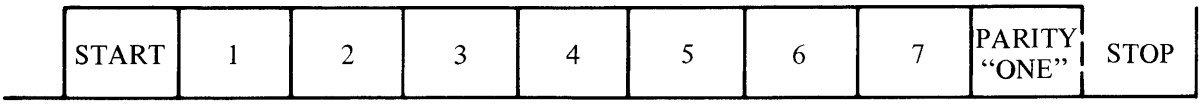
Eleven unit code with even parity.



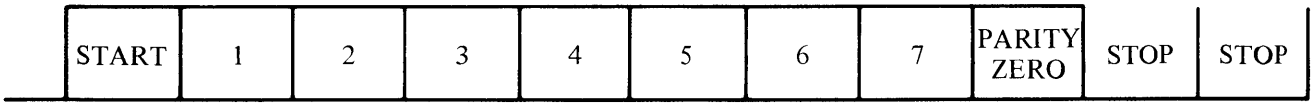
Eleven unit code with odd parity.



Eleven unit code with parity bit = "1"



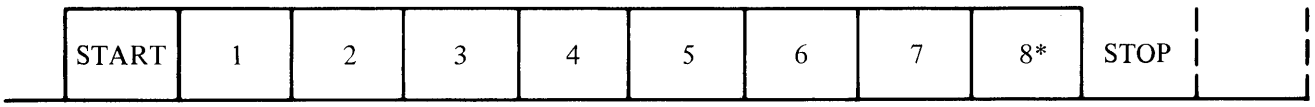
Eleven unit code with parity bit = "0"



A "protect" bit in the bit 8 position may be transmitted or received by the ADM-2. With this arrangement, the following formats can be accommodated.

If bit 8 = 1, the protect bit will be written = 1.

Ten or eleven unit code (one or two stop bits) with no parity bit.



Eleven or twelve unit code (one or two stop bits) with even or odd parity.

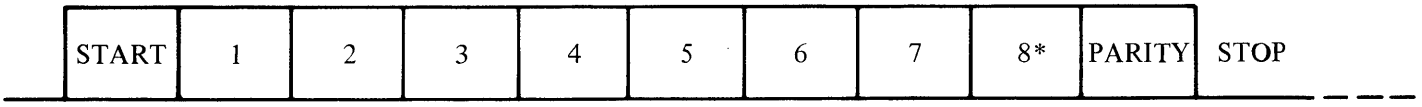


Figure 1-7. Word Format Codes (Continued)

SECTION TWO
INSTALLATION

This section contains installation instructions for the ADM-2 Interactive Display Terminal. A check-out procedure for the unit is also included.

2.1 GENERAL INFORMATION

The ADM-2 Interactive Display Terminal is suitable for desk or tabletop mounting in any normal office or commercial environment. All that is required for installation is a power connection, data signal interface connection to either the computer or the optional printer, and interconnecting cable connection between the keyboard and display unit.

2.2 UNPACKING

The ADM-2 units are packed using standard practices for shipping of electronic equipment. Every precaution is taken to ensure that each unit is complete and ready for installation upon arrival at the customer site. However, it is recommended that each unit be inspected upon receipt for intransit damage. Inspect for exterior evidence of damage. Contact the carrier and LSI immediately if damage is evident, specifying the nature and extent of the damage (if known).

If there is no apparent shipping damage, open the shipping carton and remove the items, checking them against the shipping list to verify carton contents. Contact LSI immediately in the event of a packing shortage.

Check that the serial number of the unit corresponds to that shown on the invoice. Visually inspect the exterior of the enclosure for evidence of physical damage which may have occurred in shipment.

Check the hardware to determine if any assemblies or screws have been loosened during shipment. Tighten as required. Inspect for dust or foreign material which may impair electrical contact when cable connections are made. Vacuum to remove any loose dirt.

The ADM-2 is now ready for installation.

2.3 INSTALLING THE ADM-2

The ADM-2 unit is fully assembled and operationally checked prior to shipment from the factory. Only the interconnecting cable, interface, and power must be connected at the site. The physical dimensions of the unit are shown in Figure 1-6. Installation power and environmental parameters are depicted in Table 1-1. In determining the installation area required, consideration must be given to access, power outlet required (a three prong plug), and environmental conditions. The unit also requires a table or desk for mounting.

To install the ADM-2 unit, proceed as follows:

a. Connect the data interface cable to the terminal using the information provided in one of the following tables:

   RS-232-C interface: Table 2-1.

   20ma current loop interface: Table 2-2.

   RS-232-C auxiliary interface: Table 2-3.

Table 2-1. RS-232-C Data Interface Connector J1 Signal/Pin List

PIN NUMBER	SIGNAL FUNCTION	CODE
1	Equipment Ground	AA
2	Transmit Data	BA
3	Receive Data	BB
4	Request to Send	CA
5	Clear to Send	CB
6	Data Set Ready	CC
7	Signal Ground	AB
8	Received Line Signal Detector	CF
20	Data Terminal Ready	CD

Table 2-2. 20ma Current Loop Data Interface Connector J1 Signal/Pin List

PIN NUMBER	SIGNAL FUNCTION	CODE
1	Equipment Ground	AA
4	Request to Send	CA
5	Clear to Send	CB
9	Current Loop Power (+20V through 910 ohms)	
10	Current Loop Output +	
11	Current Loop Return –	
12	Current Loop Input +	
13	Current Loop Return –	
14	Current Loop Power (+20V through 910 ohms)	

NOTES:

1. Current loop power (20 volts) is available on pins 9 and/or 14, if required.

Table 2-3. RS-232-C Auxiliary Interface Connections

FUNCTION	PIN NUMBER
Data Out to Device	Pin 3 (on BB)
Direct Connect (Two Wire) Option (129511)	Pin 9 Pin 14
Handshaking with the Device Done through EIA Signal CD	Pin 20

b. If the ADM-2 has a printer and/or polling interface option, refer to Section 2.4 of this manual.

c. Connect the cable between the keyboard and display unit.

d. Check the ON/OFF switch to ensure it is in the OFF position.

e. Plug the ADM-2 into a grounded AC outlet of the proper voltage.

(FOR STEPS f–h, THE SELECTOR SWITCHES ARE LOCATED ON THE REAR OF THE UNIT.)

f. Select the transmission baud rate in accordance with Table 2-4.

Table 2-4. Transmission Baud Rate Select

BAUD RATE	SWITCH SETTING (Thumb Wheel Type)
110	7
150	6
300	5
600	4
1200	3
2400	2
4800	1
9600	0

g. Select mode (B=block, F=full, H=half) with mode select switch.

h. Set EIA switch to the left for RS-232-C interface (standard) or to the right for the optional current loop interface.

i. Proceed to check out the ADM-2 unit.

The ADM-2 unit is checked out with the following procedure:

a. Set the ON/OFF switch on the rear of the ADM-2 to the ON position.

b. Check to see that the fan starts when power is turned on. If it does not, check the power switch and push red circuit reset button.

c. At turn on, listen for an audible tone that lasts approximately one second. If no tone is heard, look for cursor as in step d below.

d. If the cursor does not appear after a normal warm-up period, press the HOME key. If this fails to produce the cursor, reset the display by pressing the key. If there is still no cursor, it is possible the brightness and/or contrast controls are misadjusted. They are adjusted as follows:

   1. Set the contrast control to the middle of its range.

2. Turn the brightness control clockwise until the screen is bright, then reduce brightness slowly until the background is barely visible. The cursor should be present.

3. Adjust brightness and contrast for desired presentation.

4. If the cursor does not appear, check the power supply voltage; replace the monitor if necessary.

e. To check out transmittal and receival of data to and from a computer or modem in the non-block mode, proceed as follows:

1. Place the mode select switch in F (full) position.

2. Depress conversation mode key.

3. Remove the cable from the terminal output connector and jumper pins 2 and 3 together, and pins 4 and 5 together, on the terminal connector.

4. Type something on the keyboard; whatever is typed on the keyboard should appear on the screen.

f. Test the function of the character storage in memory by doing the following:

1. Run the cursor to the bottom of the display.

2. Test the page roll functioning of display characters by filling up a line, forcing the page to roll upward.

3. The memory storage of characters can be assumed to be working if the roll function operates correctly.

2.4 INSTALLING OF ADM-2 OPTIONS

2.4.1 Data Interfaces

The 20ma Current Loop interface complements the standard RS-232-C data interface. Table 2-2 lists the proper J1 connections for the optional data interface. J1 is connected to the computer, modem or acoustic coupler via cable.

The RS-232-C Extended interface is used as an auxiliary interface, enhancing the standard RS-232-C capabilities of the ADM-2. This interface connects to the next terminal in line via cable connector J2. Table 2-3 lists the proper pin connections for this interface.

2.4.2 Serial Printer Interface

The Serial Printer interface is connected to the J3 plug (at the rear of the ADM-2 unit) via cable connector. The pins listed in Table 2-5 are utilized for printer operation.

Table 2-5. J3 Serial Printer Interface Connector

PINS	FUNCTION
1	Equipment Ground
3	Serial Data to Printer
6	Terminal RTS (Request to Send) to Printer
7	Signal Common
8	ADM-2 Ready
20	Printer Ready

2.4.3 Polling Interface

The ADM-2 terminal must be assigned a device address, to identify the terminal, when operating in the polling mode. Any of the 96 ASCII characters may be assigned to the terminal as its device code. The terminal will recognize and respond only to a header containing its device address code.

To select the terminal's device address, a DIP switch device, with eight rocker switches, has been provided at the bottom of the ADM-2 unit. To set the address, proceed as follows:

a. Turn the ADM-2 unit on its side to expose the bottom panel. The DIP switch is accessible through the opening in the panel.

b. The DIP switch contains eight switches, numbered 1–8; number 1 represents the least significant bit (LSB) of the address. All switch settings are marked ON and OFF. A switch in the ON position produces a logic "zero"; a switch in the OFF position produces a logic "one."

NOTE

SWITCH NUMBER 8 MUST ALWAYS BE ON (A LOGIC "ZERO") FOR THE POLLING INTERFACE OPTION.

c. Set the switches to form a device address for the terminal. For an example, if ASCII "D" is selected as the device address, the switch setting would be as follows:

SWITCH NUMBER	1	2	3	4	5	6	7	8
ASCII "D" CODE	0	0	1	0	0	0	1	0
SWITCH POSITION	on	on	off	on	on	on	off	on

d. After setting the switches for the selected device address, return the ADM-2 unit to its upright position.

Polling interface installation information may be found in Appendix C.

2.4.4 Word Structure

To change the standard 10-unit code of the ADM-2, the asynchronous receiver/transmitter chip on the main logic board must be re-strapped as detailed in Appendix C.

The auxiliary asynchronous receiver/transmitter (used with a serial printer interface or the RS-232-C extended interface) may be re-strapped in accordance with the data in Appendix C.

2.4.5 Power Option

The ADM-2 is normally equipped to accept 60 Hz, 110V AC input power. If 50 Hz, 220V AC input power is to be used, the changes listed in Appendix C must be made.

In addition, change the crystal, installed at location M3 on the main logic board, to a crystal rated at 10,410.4KHz (standard LSI part number 800-A-10).

SECTION THREE
FUNCTIONAL DESCRIPTION

A simplified functional theory of operation for the ADM-2 Interactive Display Terminal is described in this section.

3.1 GENERAL

Figure 3-1 illustrates the functional operation of the ADM-2 in block diagram form. The standard ADM-2 is equipped with a keyboard, main logic board, CRT display, internal power supply, and RS-232-C data interface. Optional equipment available includes: polling interface, serial printer interface, 20ma current loop interface, and an extended data interface for either the RS-232-C standard data interface or the 20ma current loop interface. All functional blocks shown in Figure 3-1 are described in the following subsections.

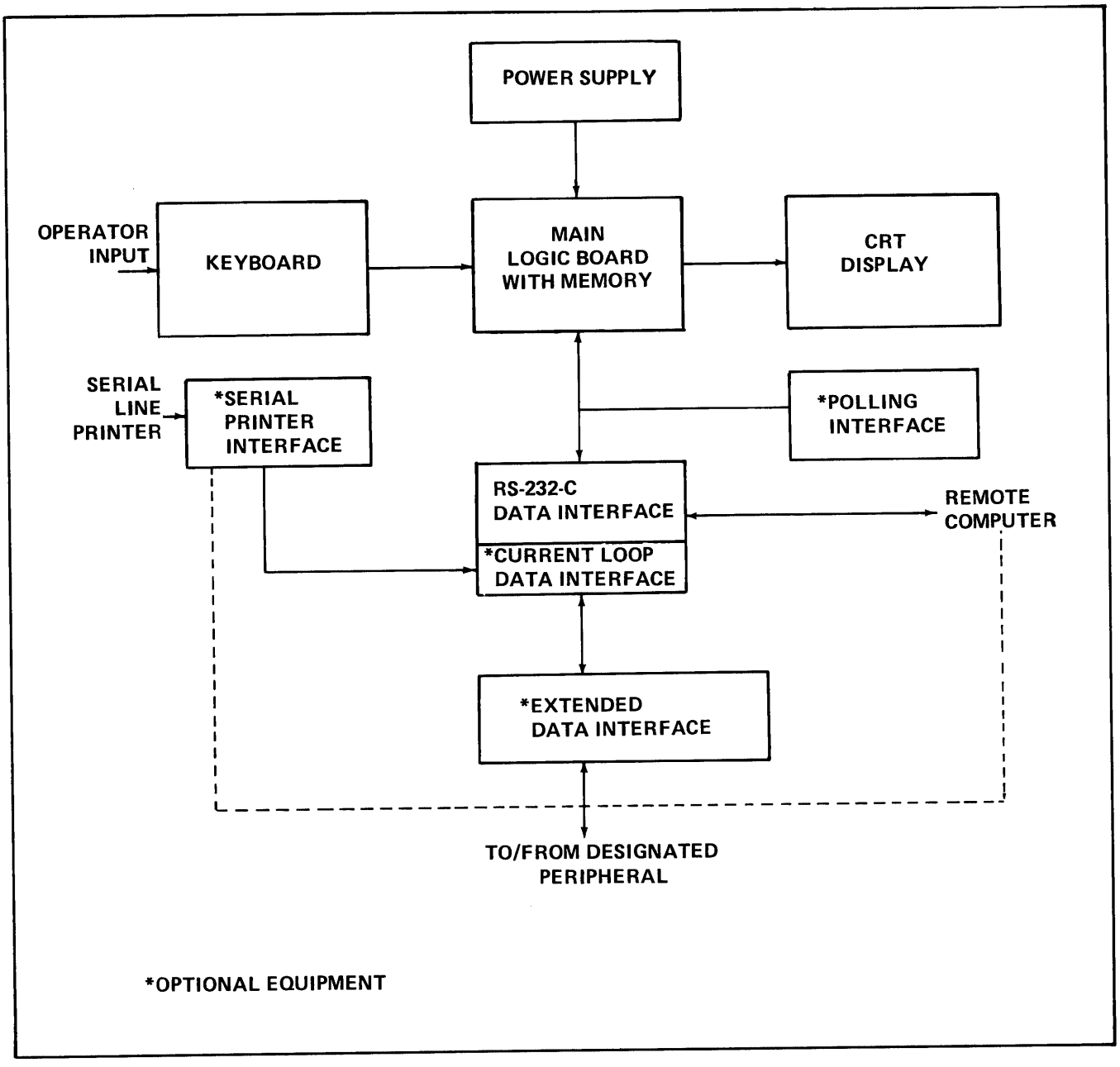


Figure 3-1. ADM-2 Functional Operation Block Diagram

3.2 CRT MONITOR AND DISPLAY

The monitor features printed circuit board construction with a self-contained power supply. The synchronization circuits have been custom designed to accept vertical and horizontal drive signals, thus enabling this monitor to interface with industrial or simple sync sources. This feature simplifies the user's sync processing and mixing, allowing the unit to operate without requiring composite sync. The monitor also features small miniaturized electronic packaging and durable construction techniques.

The display data is presented to the monitor video circuits in the form of a serial data stream. Character position and row counts are used to generate CRT sweep drive signals, with horizontal drive triggered by the start of each row, and vertical drive triggered when the character count in a row reaches 80 (indicating a full row of characters).

3.3 KEYBOARD

The ADM-2 keyboard contains 118 keys for alphanumeric display and control. When a key is depressed, it is encoded into a parallel ASCII character that appears on eight keyboard input lines (KD1–8). Accompanying the character is a keystrobe which alerts the program that a character is to be input from the keyboard.

Keystrobe is sensed by the condition logic in the terminal. A keystrobe indicates a key has been depressed. Keystrobe II indicates the character received by the terminal is a function character.

3.4 MAIN LOGIC BOARD

The main logic board consists of various integrated circuits, a few discrete components, and operational switches. The functions provided are:

- Generation of timing and control for all ADM-2 operations
- Data handling and data storage for display and/or transmission
- Interpreting control commands
- Controlling all activities in response to commands
- Generating the dot patterns for data displayed on the CRT
- Cursor display generation and cursor position control
- I/O interfacing, transmitting/receiving
- Protected/unprotected status generation for transmitted and/or displayed data.

The main logic board is a microprogram-controlled device. The board's main operations can be divided into four parts: memory (RAM), display, control (ROM), and asynchronous receiver/transmitter.

Figure 3-2 illustrates the data flow path on the main logic board.

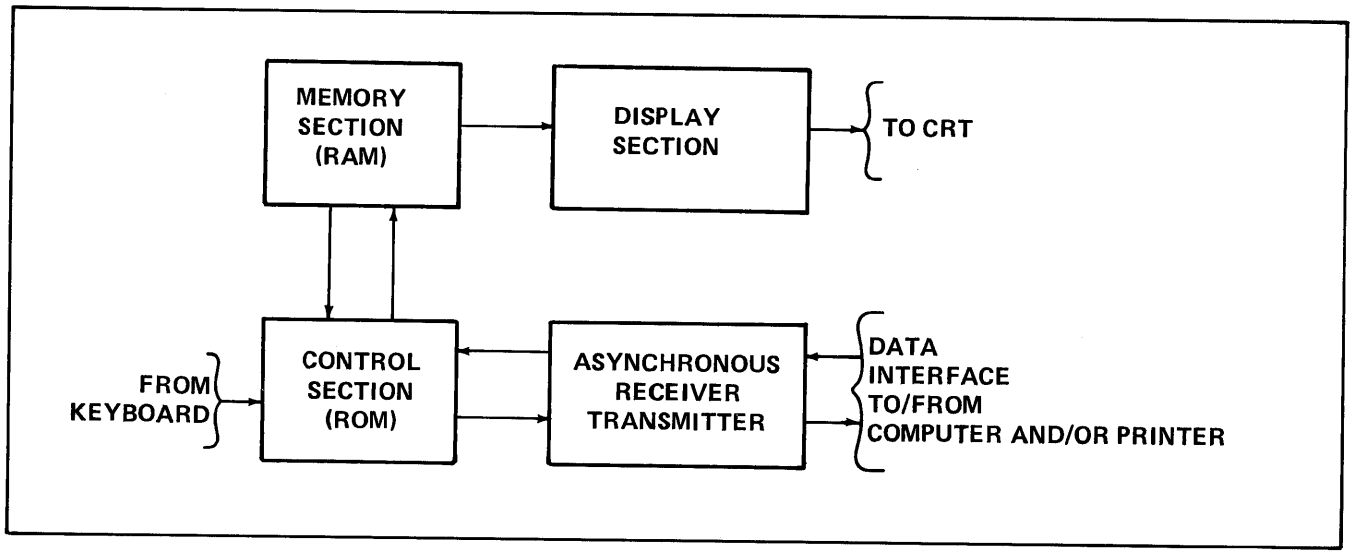


Figure 3-2. ADM-2 Main Logic Board Data Flow Path Block Diagram

The memory section consists of 16 random access memory (RAM) chips, providing for an 8-bit, 1920 word storage capacity (24 lines of 80 characters each). The memory section also contains conversion circuitry necessary to monitor display cursor position.

The display section provides the circuitry for:

- Character generation
- Row refresh logic
- Cursor display logic
- Timing control
- Blink and security field generation
- Reduced illumination for protected fields
- Control of 8-bit status indicators.

The control section contains a preprogrammed ROM (read-only memory) for information transfer control of all ADM-2 operations. The standard ADM-2 terminal functions are contained in microcode requiring four pages of ROM (256 8-bit words per page). The printer option requires an additional page of ROM, while the polling option necessitates two additional ROM pages.

The transmitter/receiver section consists of an LSI UART (universal asynchronous receiver/transmitter) chip which accepts serial ASCII code (either 10 or 11 unit codes) from a serial data interface (either RS-232-C or 20ma current loop) and transmits an equivalent 8-bit parallel code (data word) to the control section. The UART chip also functions in the reverse mode, i.e., accepts 8-bit parallel code from the control section and transmits ASCII serial code to the data interface.

Data flow control in the ADM-2 is based on RAM time-sharing between the display and control sections. The display section, responsible for the refresh function, is given RAM usage priority. The control section must relinquish control of the RAM whenever the display section requests it. The display section requires the RAM only 27% of the time, leaving 73% of the RAM's time available for the control section functions.

Main logic board data information and control commands are transferred internally between the various logic sections via an 8-bit tristate bus (TSB). The TSB is a bidirectional, central data path between all sections of the logic board. The three possible states of the TSB are:

a. **State One**—a true condition (logic "1") characterized by a +2.8V to +3.8V level or pulse.

b. **State Two**—a false condition (logic "0") characterized by a 0V to +0.6V level.

c. **State Three**—a high impedance load offered by drivers or specific logic circuits not presently using the TSB. This effectively disconnects these circuits from the TSB, minimizing the loading of the TSB. The registers connected to the tristate bus are listed in Table 3-1. These registers are specified in the ADM-2 microcontroller code.

3.5 POWER SUPPLY

The power supply module is mounted internally in the ADM-2 terminal; it provides +5V of DC to the main logic board. The power supply is rated at 12 amps and contains a solid-state voltage regulator and current limiter. Line and load regulation of .075% assures stable DC power for all terminal functions. The power supply can accept line voltage inputs of 115V AC or 230V AC (re-strapping is required for 230V AC).

3.6 RS-232-C DATA INTERFACE

The function of the RS-232-C interface is to provide a means of communication between the ADM-2 terminal and a remote computer or other device. The interface accepts data in the form presented by the computer or device and performs the necessary operations to translate the data into a form required by the terminal. The interface also works in the reverse mode (accepts data from the terminal and manipulates it into a form accepted by the device or computer). The RS-232-C converts -12V and +12V logic signals to TTL level signals.

Table 3-1. Tristate Bus Connected Registers

REGISTER SYMBOL	REGISTER NAME	DESCRIPTION
WDR	Write Data Register	Eight bit character register contains characters to be written into the RAM from tristate bus.
RDR	Read Data Register	Eight bit register to contain characters read from the RAM for transfer to tristate bus.
MACC	Memory Address Counter Character	Contains low order 7 bits of the RAM address accessible to the tristate bus (column).
MACR	Memory Address Counter Row	Contains high order 5 bits of the RAM address accessible to the tristate bus (row).
ART0	Communications Interface UART	Enable to transmitter holding register in UART.
ART1	Auxiliary Interface UART (printer)	Input bit from printer terminal (J3).
LIT	Literal (8-bit) Register	Used to transfer constants from ROM to tristate bus.
CPR	Cursor Row Position Register	Holding register for character position count.
CPRC	Cursor Position Row Counter	Register that contains present character position (horizontal).
LRC	Longitudinal Transmissions Check Register	For module 2 sum check of transmission characters.
RCV	Receiver	Receiver character register.
ADD		Switches set manually inside cabinet.
MAR	Margin Register	Eight bit utility register used for temporary holding of dynamic data.
CNTR	Counter Register	Eight bit utility register used for holding program counter during subroutine calls, and for incremented or decremented comparisons.
IND	Indicator Register	Eight bit register controls lighted indicators at right hand side of screen. "1" = lighted.
INPUT	Input Register	40 x 8-bit register used to hold characters received until the microprocessor can service the data input.

3.7 OPTIONS

3.7.1 Serial Printer Interface

This interface controls a serial character printer which is compatible with RS-232-C standards.

Two operating modes may be used with this interface: page mode or program mode.

In the page mode, characters are output to the printer at a selected baud rate, in a formatted data structure.

Data is input to the ADM-2 memory and displayed via keyboard or computer command. Then the cursor is positioned in the location at which the printer output is to stop. When an "ESC P" is entered and executed from the keyboard or computer, a GS code is written into the ADM-2 page buffer. The GS code will terminate the print operation at the cursor position at which it was set.

The cursor is automatically moved to the HOME position as the ADM-2 is made to begin outputting data to the printer. If the printer signals it is ready to accept data, the ADM-2 outputs a set of signals to initialize the printer. Data is transmitted to the printer consecutively as characters are read from the ADM-2 display buffer, beginning at the cursor's HOME position and continuing until the cursor reaches the location where the GS code was entered. Detection of a GS code signals the end of the print operation and returns the logic to an idle condition.

Data is transmitted asynchronously, in character, bit-serial format with a parity bit preceding the stop bit. Most applications use a 10-bit code with even parity.

In the program mode, the ADM-2 does not automatically format the page. Format codes must be contained in the data text in the ADM-2 memory buffer and displayed on the screen. In order to write the format codes, the ADM-2 is put in program mode via an "ESC U" command (from either the keyboard or the computer). This allows the required ASCII control codes to be written into the memory buffer of the ADM-2.

The program mode is cleared by an "ESC X" or "ESC U" command or by depressing the BREAK key on the keyboard.

3.7.2 Polling Interface

The ADM-2 may be used as a polling terminal in a multiprint communications network. In this mode, all message transmission to the polling terminal is controlled by the network control center.

The network control center transmits a header sequence to all terminals to initiate an output operation (transmit to a selected terminal from the central control center). Only the terminal with an address matching the header sequence responds to the initiating signal. If the addressed terminal is busy, the terminal disconnects from the control center. If the addressed terminal is not busy, it acknowledges the header sequence and waits for the control center to send an "STX" code. This code signals the start of transmission and causes "house cleaning" procedures to occur in the terminal in preparation for that transmission. The transmission is ended at any time by the network control center with the transmission of an "EOT" character, forcing the terminal into the idle state.

The network control center polls the terminals in the network to initiate an input operation (transmit to the control center from a terminal). An addressed terminal with no transmission ready responds to the polling with an EOT character. If the terminal has a transmission to be sent, it sends it to the control center. The terminal has several modes of operation, as described below.

Send

One of six characters specifies the information that the addressed terminal is to send. The function character (v, w, x, y, z, or {) is transmitted in the header sequence.

The six possible "send" functions are as follows:

a. **Send Line Foreground (v).** The terminal will send all foreground unprotected data in the line in which the cursor is positioned, starting at the beginning of the line and stopping at the cursor position. NUL characters are not transmitted. The terminal marks each protected area in the line with an FS character.

b. **Send Page Foreground (w).** The terminal will send all foreground data on the page, starting at the HOME location and ending at the cursor position. NUL characters are not transmitted. The terminal marks each protected area in the page with an FS character. Each end of line is indicated by an NL character.

c. **Send Line All (x).** The terminal will send all data, protected and unprotected, in the line in which the cursor is positioned, starting at the beginning of the line and stopping at the initial cursor position. All characters are transmitted, with the sequence ESC) preceding the first character of each protected field, and the sequence ESC(following the last character of each protected field.

d. **Send Page All (y).** The terminal will send all data, protected and unprotected, in the page, beginning at the HOME location and up to the initial cursor position. All characters are transmitted, with the sequence ESC) preceding the first character of each protected field, and the sequence ESC(following the last character of each protected field.

*e. **Send Message Foreground (z).** The terminal will send all foreground data following an STX code and ending with an ETX code. NUL characters are not transmitted. The terminal marks each protected area within the STX/ETX brackets by sending an FS character. If no STX (SOM ▶) is on the screen, transmission starts at HOME. If no ETX (EOM ◀) is on the screen, transmission stops at last position on the screen.

*f. **Send Message All ({).** The terminal will send all data, protected and unprotected, between the STX/ETX brackets. All characters are transmitted, with the sequence ESC) preceding the first character of each protected field, and the sequence ESC(following the last character of each protected field. If no STX (SOM ▶) is on the screen, transmission starts at HOME. If no ETX (EOM ◀) is on the screen, transmission stops at the last position on the screen.

* The SOM (STX) code (▶ symbol) and the EOM (ETX) code (◀ symbol) are entered on the screen by use of the SOM/EOM key with and without shift, respectively.

In polling operation, as in normal ADM-2 operation, control codes may be written by preceding the control code by ESC. ESC ETX will cause the ETX to be written to the screen rather than being interpreted as End of Text.

Sending Data

When the operator has set up the terminal for polling operation, the terminal waits for a valid (error-free) poll sequence. If a poll sequence is received and the terminal determines that it is the addressed unit, it transmits the sequence STX text ETX LRC. The LRC character is the module-2 sum of the text characters plus the ETX character.

The text of the message is sent in one of two formats, depending on whether or not the protect mode is set at the terminal:

a. **Protect mode off.** All foreground (unprotected) characters except NUL are sent. A US character is inserted in the character string as the cursor moves from the end of one line to the beginning of the next line.

b. **Protect mode on.** All foreground characters are sent. An FS character is sent to mark the location of each protected field.

After the terminal has sent the LRC character, it waits for the center to acknowledge receipt of the message. An acknowledgement will consist of one of three characters (ACK, NAK, or EOT). The terminal will respond to each character, or to another character or an error, in a different way, as follows:

a. **ACK.** Message was received successfully. Terminal sends EOT and disconnects.

b. **NAK.** Message was received with errors. Terminal retransmits the message and then waits for acknowledgement.

c. **EOT.** Retransmission is required. Next character may be the terminal address. Terminal positions cursor to the original position and waits to be polled.

d. **Another character or error.** Terminal positions cursor at the start of the message and waits for the next poll.

There are a number of methods used by the network center to select a terminal; they are described below.

Select

When the ADM-2 is addressed by the sequence EOT A_1A_1 q ENQ, it responds as follows:

a. If the terminal is busy, it sends character NAK to the center, and then disconnects. Busy is defined as any of the following states:

   1. The terminal is waiting to be polled,

   2. The operator is entering data, or

   3. The terminal is sending data to the printer.

b. If the terminal is not busy, it sends character ACK to the center, and then waits for the center to send STX. Any character received before STX is ignored.

c. After STX is received, the following events occur:

   1. The terminal clears the LRC accumulator, which accumulates characters of the incoming message for subsequent action based on the nature of the resulting LRC check character.

   2. When the entire message, including ETX, has been received by the terminal, and the LRC character is received, the contents of the LRC accumulator and the parity error flag are tested.

   3. If no error has been detected, the terminal sends character ACK to the center and disconnects in the idle state.

   4. If an error was detected in the message, the terminal sends character NAK and waits for the center to retransmit the message.

   5. The center may then retransmit the message, starting with STX. If the center wishes to terminate the operation after receiving NAK from the terminal, it may transmit an EOT character, instead of STX, setting the terminal to the idle state.

Sequential Select

The Sequential Select function sequentially addresses a number of terminals with a single, extended header. All addressed terminals (that are not busy) will receive the same message.

The header sequence is EOT A_1A_1 r A_2A_2 r . . . A_nA_n s.

Note that the last terminal is addressed with the Fast Select function, which is always followed by the sequence STX text ETX LRC.

a. Terminals (except A_n) will connect and wait for STX if they were idle when character "r" was received. Terminal A_n will connect unconditionally.

   When "r" is received in the "function" position of the header, each terminal tests to see whether or not its address code had preceded "r". If its address did precede "r", the terminal tests its busy status. If not busy, it will wait for the STX code and prepare to accept the incoming message. If busy, it disconnects without responding.

b. Following receipt of ETX LRC, all addressed terminals except A_n disconnect without responding. Terminal A_n will send either ACK or NAK to the center (depending on whether or not an error was detected), and then disconnect.

Fast Select

Fast Select permits fast, unconditional selection of a terminal. The header is EOT A_1A_1 s, and is followed directly by the sequence STX text ETX LRC.

On receiving the header, the addressed terminal will unconditionally connect (regardless of its busy status) and wait for STX. The terminal will not respond until after it has received the LRC character.

Broadcast Select

The Broadcast Select function addresses all terminals with a single header, so that they will receive

the same message. That is, Broadcast Select is the same as the Fast Select function except that the message is received even by busy terminals.

The header sequence is EOT A_nA_n. Note that the last terminal is addressed with the Fast Select function, which is always followed by the sequence STX text ETX LRC.

a. All terminals will connect, unconditionally, and wait for STX.

b. Following receipt of ETX LRC, all terminals except A_n disconnect without responding. Terminal A_n will send either ACK or NAK (depending on whether or not an error was detected), and then disconnect.

3.7.3 Additional Data Interfaces

The function of the standard RS-232-C interface is to provide a means of communicating between the transmission facilities and the computer. Not all devices use this method of communication. The ADM-2 has an optional 20ma current loop data interface available to allow the terminal to communicate with devices using this method.

The RS-232-C standard data interface can be complemented with an auxiliary RS-232-C data interface, to permit driving additional devices that are compatible with EIA RS-232-C voltage level signals. The interface operates exactly as the RS-232-C standard data interface (refer to Section Four).

SECTION FOUR
THEORY OF OPERATION

The ADM-2 theory of operation can be divided into four main logical subsections:

- Logic Board
- Monitor & Display
- Keyboard
- Power Supply

All four of these subsections are detailed in the following description.

4.1 MAIN LOGIC BOARD

The main logic board in the ADM-2 is the center of activity for all terminal operations. The board is a microcontrolled device which is responsible for:

- Clock and timing signals
- Generating the displayable dot patterns
- Generating the cursor
- Keeping track of cursor position
- Coordinating all data transfers
- TX and RX data from the computer, modem, or printer
- Storing data for display and TX
- RX control information from keyboard and modem
- Interpreting all control commands and controlling terminal activities accordingly
- Data status control (unprotected/protected) for display and transmission.

The basic functional organization of the ADM-2 main logic board is illustrated in Figure 4-1.

Figure 4-2 is a more detailed block diagram of the main logic board. Each block in this diagram is discussed in the following subsections.

(WHILE READING THE FOLLOWING DATA IN THIS SECTION (4.1), REFER TO THE SCHEMATIC DIAGRAMS IN APPENDIX A.)

4.1.1 Clock (Schematic P. 2)

The ADM-2 uses a crystal controlled oscillator as its master clock. The oscillator frequency is 12.4925 MHz for 60 Hz operation; 10.4104 MHz for 50 cycle operation. The oscillator output ($\overline{CLK}$) is applied to counters and gates throughout the logic board to provide basic timing signals. ADM-2 basic timing signals are shown in Figure 4-3.

4.1.2 Counters (Display Generation) (Schematic P. 2)

Display generation in the ADM-2 is provided by a series of counters. Dot Position, Character Position, Character Height, and Character Line counters are used to produce, on the CRT, a 5" x 7" character and a 7" x 9" cursor. Counter operation is started by a clocking pulse from the oscillator.

The dot position counter is a divide by 7 type, 4-bit counter. Its outputs (DPCx) are input to the video line register, and the indicator logic (shift register) for transmission to the video logic and the monitor drive logic, respectively. A DPC output signal also clocks the character position counter.

The character position counter is a divide by 104 type, 8-bit counter. It is used to keep track of the cursor position in the video timing logic. MAC is used to monitor the cursor position on the CRT. Character position counter output signals (CPCx) are sent to the data memory address logic, video line register logic, video logic, MACC control logic, indicator timing logic, and monitor drive logic. Output signals CPC4, 16, and 80 clock the character height counter.

The character height counter is a divide by 11 type, 4-bit counter. It is used to count the number of rasters in a line. The output signals (CHCx) are input to many functions of the video logic, including the character generator multiplexer, indicator video logic, and cursor enable F/F. The (CHC9) output signal clocks the character line counter.

The character line counter is a divide by 26 type, 4-bit counter. It is used mainly to keep track of the row position of the cursor. The character line counter output signals (CLCx) are sent as inputs to the video driver, indicator logic, and the cursor tracking logic of the MACR.

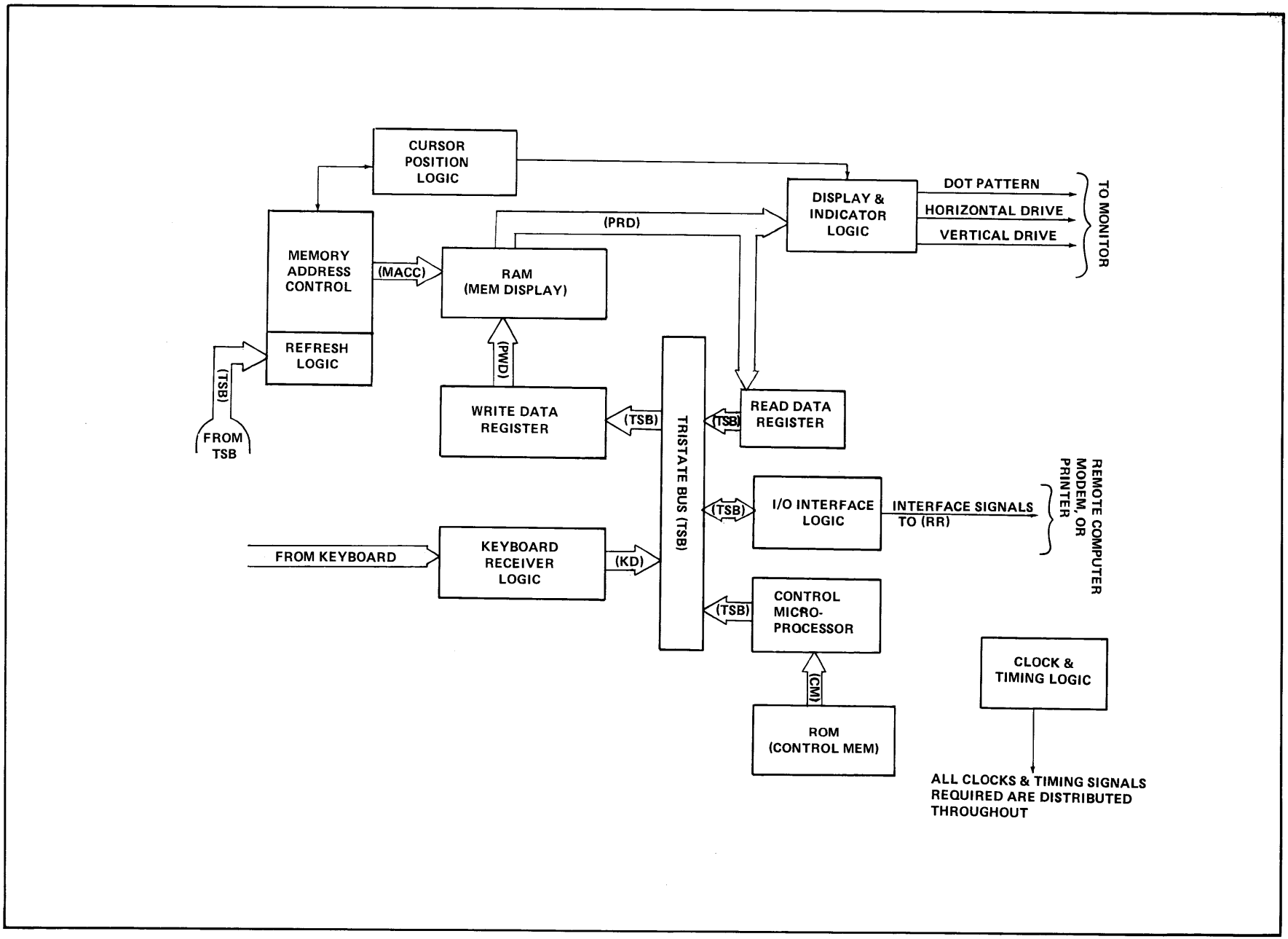


Figure 4-1. ADM-2 Logic Board Block Diagram

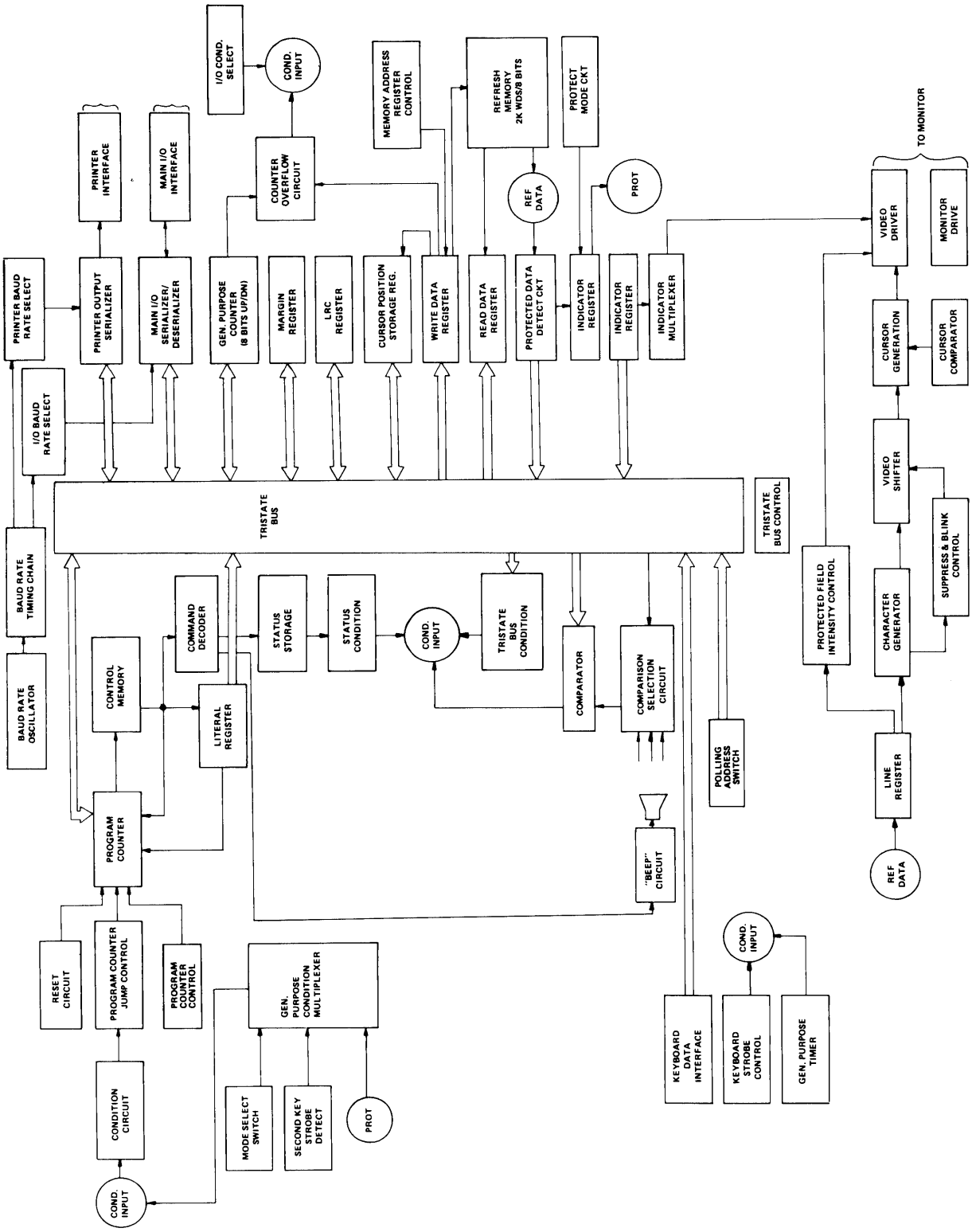


Figure 4-2. ADM-2 Main Logic Board Detailed Block Diagram

4.1.3 Tristate Bus (TSB) (Schematic P. 13)

The Tristate Bus provides a central data path between logic board elements. All counters and registers, excluding the display counters, are command memory controlled and have either outputs or inputs to the TSB. The TSB is multi-directional, eight bits wide, and can be put into three possible states, which are:

a. **State One**: A logical "1" or true condition. This is characterized by a +2.8V to +3.8V level or pulse.

b. **State Two**: A logical "0" or false condition. This state is characterized by a 0V to +0.4V level.

c. **State Three**: A high impedance load offered by transmitters of elements not connected to the TSB at a given time. This state, in effect, disconnects from the TSB elements not presently using the bus. Thus, active TSB drivers have a minimum loading effect.

All transfers over the TSB are determined by gating the characters on and off the TSB for loading into storage (memory or register) under the control of the microprocessor.

The output signals (CMx) of the command memory (ROM) are input to TSB decoders. The signals are decoded to determine what element may use the TSB. The control microprocessor gates the proper command memory outputs to the TSB decoders. The elements that may use the TSB are shown in Figure 4-3 and described below.

- **The Literal Register** (Schematic P. 13)—This register is used as a general purpose register by the programmer. It may: transfer or receive data between memory and the TSB; be used as a holding register for various operations (i.e., ESC code to trigger the function); it may be used to store program information or to store the program address when jumping off the page (lower four bits are connected to the page register.

  The literal register is loaded from the ROM memory (command memory) by the command decode logic. Output signals (LIT1-8) are sent to TSB drivers.

- **Comparison Circuit** (Schematic P. 18)—Comparison logic is used to compare the TSB with the MACC and literal register (7 or 8 bits) or the NULL code. The comparator logic receives its input signals from the MACC (MACCx) and literal register (LITx). The signals are sent through a 2:1 selector which sends only the enabled signals to the comparator circuit. Command decode logic signals (CMDx) enable the comparator and output the results of the compare as ($\overline{\text{COMP COND}}$). (If condition is met, the output is false).

- **TSB Bit Decoder** (Schematic P. 17)—The TSB has an associated decoder circuit to enable a test for the condition of any bit on the TSB. TSB bus signals (TSB1-8) are input to the decoder and tested as to their condition. The decoder output (TSB COND) is available to the jump logic to alter the program counter if a specified bit condition is encountered.

- **Write Data Register** (Schematic P. 14)—The write data register transfers eight data bits to memory from the TSB. The inputs to the write data register are the TSB bits (TSB1-8); the register is enabled by the command decode logic signals (CMDx). Data is output as (PWD1-8). Output signal (PWD8) also indicates whether write protect is on or off.

- **Read Data Register** (Schematic P. 14)—RAM memory output signals (PRD1-8) are read into the read data register. The register outputs the eight bits of data as (TSB1-8) to the TSB and the TSB buffers (ITSB1-8). Input signal (PRD8) is also decoded to determine if the character is protected.

- **Cursor Position Storage Registers** (Schematic P. 12)—There are two registers associated with the cursor position that transfer their data via the TSB. They are the cursor position row register and the cursor position character register.

  The **cursor position row register** records which of the 24 possible rows the cursor is in. It is a 5-bit register whose drivers are enabled by ($\overline{\text{TSB=CPR}}$) (P. 15). It receives its input signals from the MACR and MACC logic (P. 12) which actually track the cursor row. The output signals (TSB1-8) are the TSB bits which provide information on cursor position to the program.

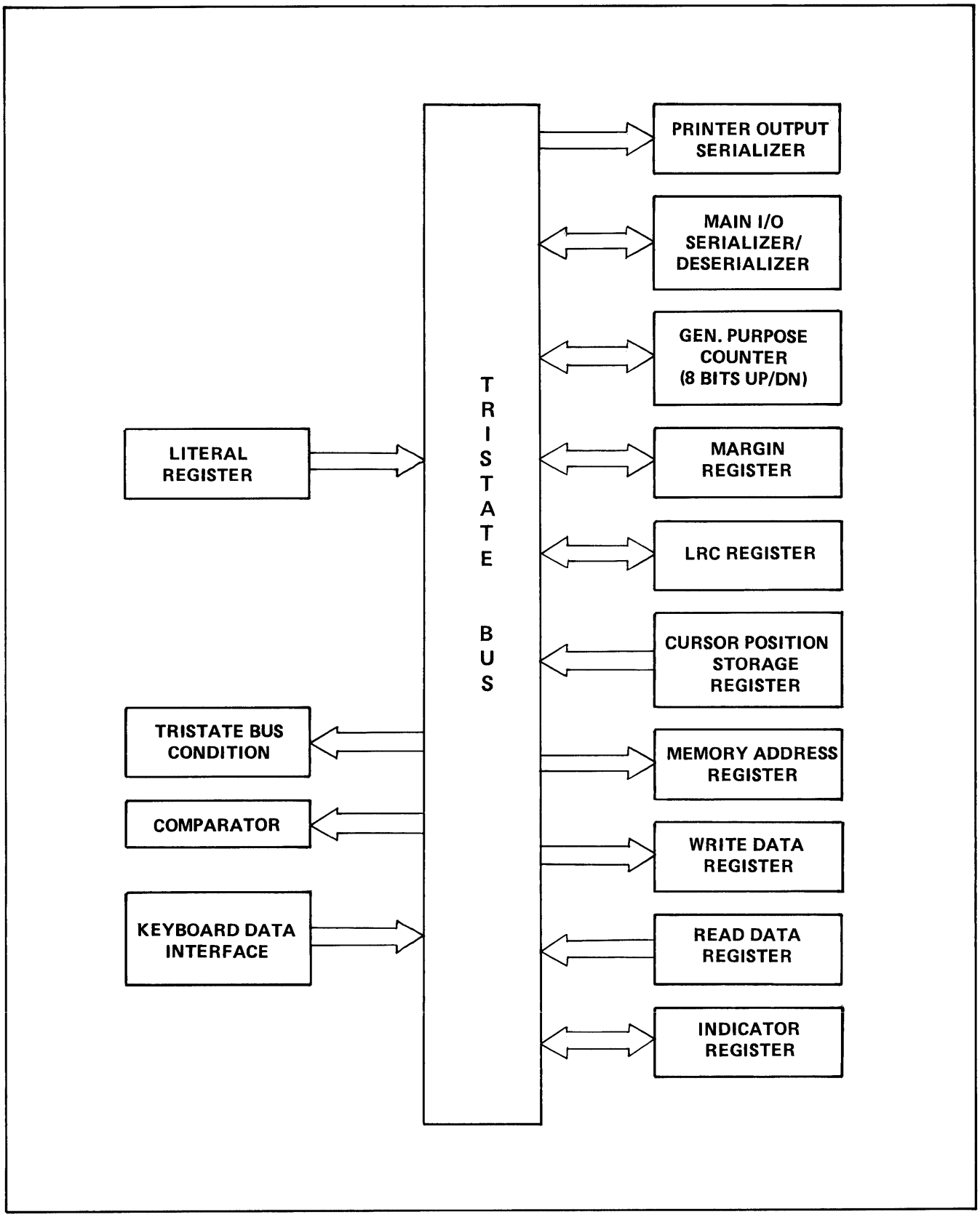


Figure 4-3. Tristate Bus and Elements that Use It

The **cursor position character register** records which of the 80 possible positions the cursor is in on the line. It is a 7-bit register which receives its input signals from the MACC logic, as does the row register. Again, the output signals (TSB1-8) provide information on cursor position to the program.

- **General Purpose Counter** (Schematic P. 18)—This counter (register) may be used by the programmer for various functions. The counter is multi-directional (can receive or send data to/from the TSB). The counter has the ability to be used as an up or down counter when the drivers for the TSB are enabled.

- **Indicator Register** (Schematic P. 7)—This register holds data that will be sent to the indicator generator and eventually to the monitor drive logic. The register is available to the TSB for program information. Register input signals are either TSB bits or its own output bits (INDx). The (INDx) signals are enabled to the TSB drivers when (TSB=IND).

- **Margin Register** (Schematic P. 10)—The margin register is another general purpose register providing desired information to the program via connecting outputs to the TSB.

- **Memory Address Register** (Schematic P. 12)—This register is loaded from the TSB and supplies output signals (MACCx) to: the counter overflow logic (to note end of page or end of line) and to the cursor position storage registers (to update). The memory address register receives its input signals from the memory control via TSB decoded commands (MACC, INC, DEC, LOA, SET), or is loaded by information from TSB itself.

- **LRC Register** (Schematic P. 15)—LRC compares the character sent with the character received by checking the data line and character code. It is used when a polling option has been installed and the terminal is operating in the polling mode. If the character and data line do compare, a logic "0" is output by the circuit. The LRC register is capable of being loaded from the TSB and outputting to the TSB.

- **Keyboard** (Schematic P. 19)—Keyboard inputs enter the logic board at J6. The J6 terminal output signals (KD1-8) are sent to TSB drivers which are enabled by (TSB=KEY). When the drivers are enabled, the keyboard data is transferred to the TSB (TSB1-8).

- **UART (Serializer/Deserializer Chip)** (Schematic P. 20)—The main I/O and printer I/O UART chips (interfaces) have a direct linkage to the TSB. The UART and the printer port can be loaded from the TSB. The TSB bits (TSB1-8) may be input to either UART. The interface will then serialize the data for output to the device or modem. The main port may accept serialized data and convert it to parallel data for transfer to the FIFO and then onto the TSB.

4.1.4 Microprocessor Logic

The microprocessor logic on the main logic board sequences and controls all logic board operations. The microprocessor logic consists of:

- Command memory address register
- Control memory ROM
- Command decode logic
- Condition logic
- Literal register
- Tristate bus control logic
- Program counter
- Status logic
- LRC register
- Compare logic
- General purpose counter

Figure 4-4 shows a block diagram of the microprocessor logic.

- **Command Memory Address Register** (Schematic P. 8)—The command memory address register is loaded from the program binary counter output signals (CM0-7). During microprogram execution, instructions are fetched according to the address in the command memory address register (CMA). After each instruction or literal is fetched from the ROM, the CMA is automatically incremented to the next sequential address. If the previous instruction was a jump command, the CMA is forced to the jump destination address.

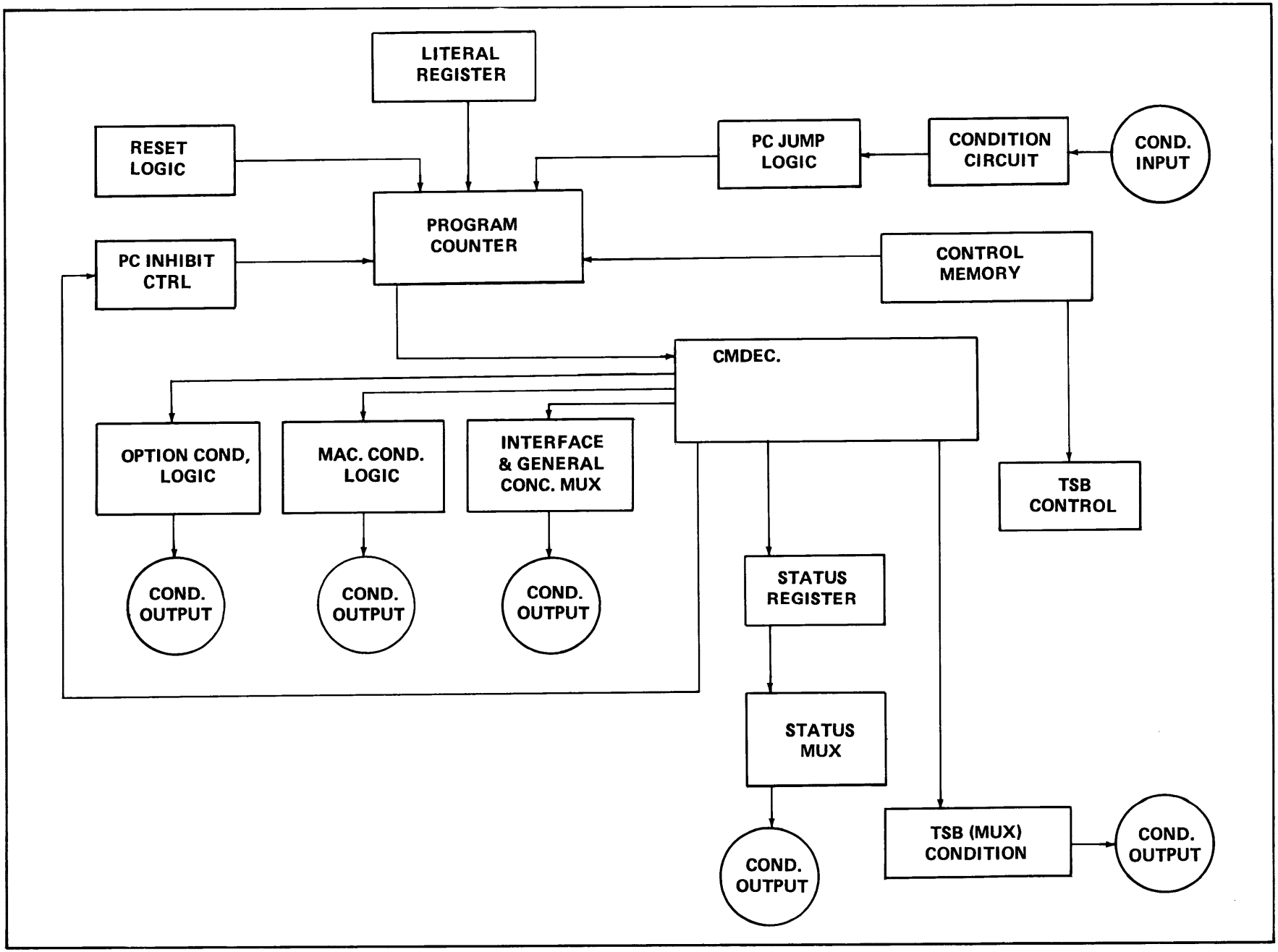


Figure 4-4. Microprocessor Logic Block Diagram

The CMA is an 8-bit register capable of addressing any word in the ROM memory. The 8-bit CMA (bits 0-7) selects a ROM address, and the 4-bit CMAP (bits 8-11) selects the ROM page. Bits 0-11 are sent to each ROM page in the ADM-2, but only the ROM with the proper decode of bits 8-11 will respond to the address. (Note: Two pages per ROM.)

- **Control Memory ROM** (Schematic P. 9)—All information transfers in the ADM-2 are controlled by the microprogram instructions stored in the control memory (ROM). The standard ADM-2 functions are contained in four pages of 1024 x 8 ROMs (ROMs are eight bits wide). Additional ROMs may be installed, extending the ADM-2 control memory capacity to eight pages of ROM (2048 words total).

  CMA signals (CMA0-11) are input to the ROMs. The responding ROM will output the data at the requested address to the literal buffer drivers. The command memory output driver signals (CM0-7) are made available to the TSB. ROM data may also be sent to the command decoder and the program counter.

- **Command Decode Logic** (Schematic P. 10)—Instructions fetched from the ROM are loaded into the command decoders by (CM) inputs to the three decoder chips. The data is then decoded into 25 control lines to direct all information transfers throughout the logic board. Command decoder output signals (CMDx) are utilized to interpret all functions except TSB decoder. The decoder signals are disabled during the second half of jump, jump on condition, LOA LIT instructions, or when the terminal is reset (SHIFT/RESET or "power on").

- **Condition Logic** (Schematic P. 8)—The ADM-2 microprogram contains routines which sense the status of various logic board elements. This status checking is accomplished by sampling the multi-source status line (COND). Prior to sampling (COND), the microprocessor enables only the path from the source it desires to check. If (COND) is satisfied, the program jumps to the appropriate routine or subroutine.

- **General Purpose Condition Multiplexer** (Schematic P. 19)—This multiplexer is used to test the condition of the listed elements. The multiplexer output signal (CONDB) is input to the multi-condition line (schematic P. 8) along with the other condition checks. The numerous gates filter into the decoder, and the decoder's output is controlled by the status of the tested condition. The program continues according to the directions received from the condition decoder output.

- **Literal Register** (Schematic P. 13)—The literal register is loaded from the control memory (ROM). The output signals (CMx) of the command memory feed to the program counter (for addressing) and to the literal register. The literal register output signals (LITx) are available to the TSB. Therefore, when the literal register is loaded from the ROM, via the tristate drivers, the output of the ROM is then available to the TSB. In effect, the literal register is used to transfer 8-bit data from memory to the TSB. The lower four bits load the page address register.

- **Tristate Bus (TSB) Control Logic** (Schematic P. 13)—The microprogram performs data transfers over the TSB by gating data from one of twelve possible sources, then gating the bus contents from the TSB into the desired destination. The signals which gate data onto the bus are generated in the TSB control logic by decoding the lower four bits (CM0-3) of the microprogram instructions. For the twelve TSB control commands, corresponding TSB control signals are generated. Each control signal causes the contents of a source to be gated onto the TSB.

  Input commands to the TSB control logic (CM0-3) are held by a register. The signals from the quad D-latch flip-flop register are output as (TSBR0-3). These new signals are now input to two decoders, where they are decoded into the control signal necessary to perform their designated operations.

- **Status Logic** (Schematic P. 16)—The microprogram can set, sense and clear a variety of flags in the eight individual registers to set global conditions to control the microprogram actions. The status is checked by the status bit register (using specified command codes). Status register output signals (STB1-8) are sent to a sense status bit multiplexer for determining the conditions of each status bit checked. The multiplexer outputs the signal ($\overline{\text{STB COND}}$) upon a favorable compare with the checked status bit. This signals the program that a flag is set.

4.1.5 Keyboard Logic (Schematic P. 17, 19)

The keyboard input data enters the main logic board at terminal J6. Keyboard input bits (KD1-8) are routed to a driver network for output to the TSB. The keyboard operation begins by the signal KEYSTROBE (for alphanumeric characters) which sets flip-flop B15 (schematic P. 17) during clock TS7E time. Gate B14 goes true (with KEYSTROBE and proper command decode) to make both legs of gate A2 true, causing COND KB to be output to the condition jump logic, and setting B15, forcing the Q output on pin 8 of flip-flop B15 to loop back and force the flip-flop reset on the next pulse of clock TS7E. This forces pin 8 low, making the bottom leg of gate A2 false. This causes COND KB to be sensed for only one instruction time.

If bit 8 from keyboard is true, then the key depressed is a function key, and the terminal responds with an SOH, FUN CHAR, and carriage return. If a strobe 2 is detected, the terminal reacts upon the character as a function character (ESC command, CLR SCREEN, LINC insert, etc.).

The keystrobe I is input to the mode selector chip, A20 (schematic P. 19). The TSB source decoder, A22 (schematic P. 13) enables keyboard data onto the TSB (TSB=KEY). This keystrobe pulse designates that the following character is a function character.

Keyboard data is carried by the TSB to the I/O interface logic for transmission and to the write data register for input into the refresh memory (in half duplex mode) for screen display. In the full duplex mode, keyboard data only is transmitted. Keyboard data will be displayed if it is echoed back from the modem or remote computer.

The keystrobe circuit is used for keyboard input.

4.1.6 External Interface Logic (Schematic P. 20-23)

The standard ADM-2 terminal has one serial I/O interface channel installed for external communications with a remote computer or a modem. A second I/O serial data channel is available as an option. Each I/O channel contains a UART (Universal Asynchronous Transmitter/Receiver) chip (shown on schematic P. 20, labeled D1 and D3) to interface between a serial data interface and the parallel ADM-2 control section.

Baud Rate Select (Schematic P. 21)

Baud rates (i.e., transmission rates) are user selectable from 110 to 9600 baud. A switch, in the rear of the unit, selects the desired baud rate (switch settings are described in Section 2 and listed on the upper right side of the schematic). This switch selects the baud rate of the ADM-2 terminal only. A separate setting is required for the selection of the printer option baud rate. On the ADM-2, logic board -13, the printer rate may be selected by switch F2 on the logic board. On the ADM-2, logic board -7, the printer rate may be selected by jumpers. In both cases, printer baud rates are available from 110 to 9600 baud; these printer baud rates may be different from the baud rate set for the ADM-2 terminal.

The baud rate oscillator clocks the baud rate timing chain (made up of the four binary counters) to start the I/O interface operation going. The timing chain will provide a transmit/receive clock (XRCLK) at a frequency selected, by the operator, to the standard UART logic. The timing chain will also provide a printer clock (PTCLK), if the printer option is present, to the second UART logic.

NOTE

ALL BAUD RATES, WITH THE EXCEPTION OF THE 110 BAUD, ALLOW FOR THE SELECTION OF STOP BITS WITH EITHER SWITCHES OR JUMPERS (DEPENDING ON THE BOARD). THE 110 BAUD RATE SELECTION AUTOMATICALLY CHOOSES TWO STOP BITS.

Universal Asynchronous Transmitter/Receiver (UART) (Schematic P. 20)

The UART is a combination transmitter and receiver. The receiver accepts serial ASCII 9, 10, or 11-bit codes from an RS-232-C or 20ma current loop interface and transmits an equivalent 8-bit parallel code to the control section of the ADM-2, via the TSB. The UART also accepts 8-bit parallel words, received from the ADM-2 TSB, and transmits them as serial ASCII strings of data over the RS-232-C or 20ma current loop interfaces. A full data transmission consists of a START bit, followed by seven or eight DATA bits, the PARITY bit (if parity is selected), and one or two STOP bits.

The standard I/O channel UART circuitry is set up to permit data transmission in either direction (i.e., either to or from the ADM-2). The UART chip is enabled by the transmit/receive clock (XMIT/RCV CLK) sent from the timing circuitry. XMIT/RCV CLK is the gated XR clock from the baud rate select logic and is sixteen times the baud rate.

The XMIT/RCV CLK is enabled by clear-to-send (CTS) from the interface. The line is controlled by TRE0 (transmit register empty) and THRE0 (transmit holding register empty). THRE0 goes low when the transmitter holding register receives a load signal.

The next request-to-send (RTS) signal from the interface will reset the XMIT/RCV CLK logic.

When transmitting to the I/O interface, input (TSB1-8) is received by the UART in a parallel format, and serial data is input to the UART chip for processing into a parallel data word which can be accepted by the 40 character buffer logic. The parallel data word from the FIFO is output to the TSB, as bits (TSB1-8). The data is held in this buffer until the microprocessor is ready to service the channel. When the channel is serviced, the bytes are output, in a parallel format (in the same order they were entered).

TSB bit 8 can be enabled or disabled on the main logic board to conform with the word structure being used. Bit 8 is controlled on the -13 logic board by switch D2. On the -7 logic board it must be jumpered from E28 to E27 (always on), E22 (always off), or E20 (Bit=TSB).

At the input side of the UART chip, the user can select the word structure desired. Pins 35, 39, 36, and 38 select Parity/Non-Parity, Even/Odd Parity, One or Two Stop Bits, and Seven/Eight Bit Code, when grounded. On the -7 logic board, a jumper must be placed between the pin and ground for each of the following:

- For Parity E22 to E26 (pin 35)
- Odd Parity E22 to E23 (pin 39)
- One Stop Bit E22 to E25 (pin 36)
- Seven Bit Code E22 to E24 (pin 38)

If the jumpers are not installed as above, the following is selected:

- No Parity (Pin 35 open)
- Even Parity (Pin 39 open)
- Two Stop Bits (Pin 36 open)
- Eight Bit Code (Pin 38 open)

On the -13 logic board (at UART input pin 20) switch C9-5 allows the user to choose whether a request-to-send (RTS) signal will be required with a receive data (RCVDAT0) pulse to pass data onto the UART.

The UART chip in the optional printer I/O channel works the same way as the UART chip in the standard I/O channel. The difference is in the circuitry used to support the UART chip. As the printer can receive but not transmit data, only one-way communication is required. The TSB is connected to the printer channel for loading the UART only. TSB bits (TSB1-8) provide the parallel data word to the UART for processing into a serial bit stream for output to the printer. All eight data bits of the TSB are connected directly to the UART input pins.

Pin 40 of the UART receives a printer clock (PL CLK) enable instead of the transmit/receive clock supplied to the standard channel. All parameter selections at pins 35-39 are the same as previously described.

Figure 4-5 is a block diagram of the Universal Asynchronous Receiver/Transmitter (UART) chip. Table 4-1 lists the specifications of the UART chip.

RS-232-C Interface (Schematic P. 22)

Data is sent to the outside world via an RS-232-C interface. This interface is standard on the ADM-2. An optional 20ma current loop interface may be used instead of the RS-232-C type. The type of interface is selected using a switch on the rear of the unit (for RS-232-C, the switch is positioned on the EIA side. For current loop interface, the switch is positioned on the CL side).

The RS-232-C is a simple driver circuit connecting to a remote computer or modem. Terminal J1 outputs data on pin 2 (BA). Pin 4 (CA) transmits the request-to-send signal, pin 5 (CB) receives the clear-to-send signal, and pin 3 (BB) receives data.

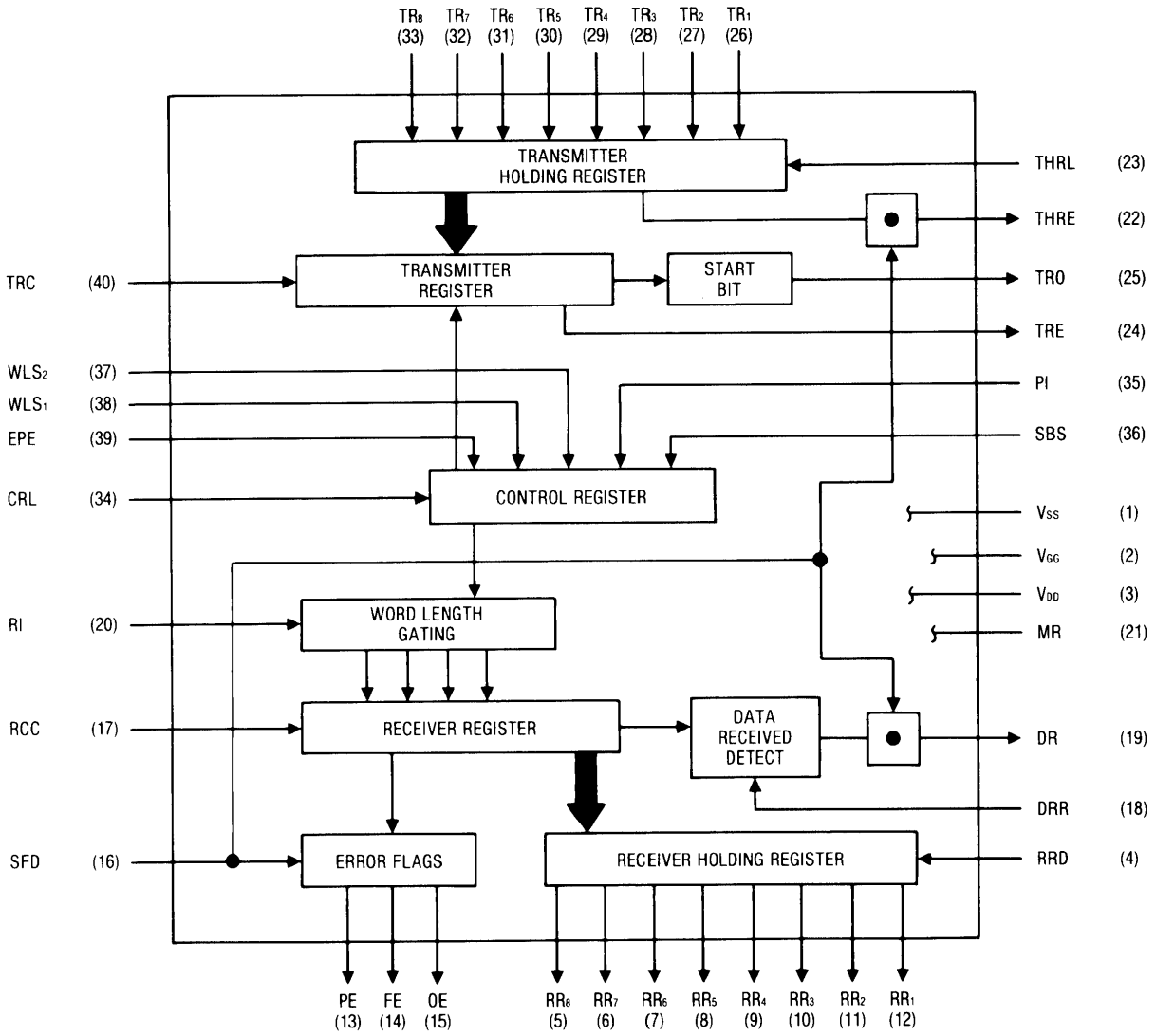


Figure 4-5. ADM-2 Asynchronous Receiver/Transmitter (UART) Block Diagram

An optional auxiliary RS-232-C interface may be added to the existing interface for additional output capabilities. The data sent to the extended interface is received via J2 pin 2. As shown on schematic page 22, the data received from the computer is transferred on to the extension port via pin 3.

20ma Current Loop Interface (Schematic P. 22)

The optional current loop interface is selected by a switch, on the rear of the ADM-2, in the CL position. The current loop interface employs an optical coupler to transfer the TTL data to its amplifier, through the diode output network to the current loop. The optical coupler completely isolates the current loop transmitter from the ADM-2. One leg of the current loop may be tied through a resistor to +20V DC to create a current source.

On the -13 main logic board, switch C9-1 closed gives the user the ability to inhibit RTS(CA) until CTS(CB) equals one. Switch C9-2 closed enables the user to inhibit RTS(CA) until RCVD Line Signal Detector (CF) equals one.

Switch C9-3, when closed, selects the use of the keyboard BREAK signal.

On the -7 main logic board, the same selection process as above is obtained by jumpering the CTS0, RLSD0, and BRK signals.

Table 4-1. UART Specifications

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	V_{SS}	+5 volts Supply
2	V_{GG} POWER SUPPLY	V_{GG}	-12 volts Supply
3	V_{DD} POWER SUPPLY	V_{DD}	Ground
4	RECEIVER REGISTER DISCONNECT	RRD	A high-level input voltage, V_{IH} applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_8-RR_1 data outputs (pins 5-12).
5-12	RECEIVER HOLDING REGISTER DATA	RR_8-RR_1	The contents of the RECEIVER HOLDING REGISTER appear on these lines in parallel if a low-level input voltage, V_{IL}, is applied to RRD. Program control selection of a word length less than eight (8) bits will cause the most significant bits of the character to be forced to a low-level output voltage, V_{OL}. The character will be right justified. RR_1 (pin 12) is the least significant bit of the character.
13	PARITY ERROR	PE	The status of the parity verification circuit appears on this line, if a low-level input voltage, V_{IL}, is applied to the STATUS FLAGS DISCONNECT (pin 16) control line. Wired OR capability is provided on this line, allowing PE lines from other arrays to be OR tied. A high level output voltage, V_{OH}, on this line (under the conditions above) indicates a PARITY ERROR in the received parity bit as programmed by the EVEN PARITY ENABLE control line (pin 39). The status is updated each time a character is transferred from the RECEIVER REGISTER to the RECEIVER HOLDING REGISTER.
14	FRAMING ERROR	FE	The status of the STOP bit detection circuit appears on this line if a low-level input voltage, V_{IL}, is applied to the STATUS FLAG DISCONNECT (pin 16) control line. Wired OR capability is provided on this line, allowing FE lines from other arrays to be OR tied. A high-level output voltage, V_{OH}, indicates that the received character has no valid STOP bit, i.e., the bit following the parity bit is not a high-level input voltage, V_{IH}.

Table 4-1. UART Specifications (Continued)

PIN NUMBER	NAME	SYMBOL	FUNCTION
15	OVERRUN ERROR	OE	The status of the DATA RECEIVED circuit appears on this line of a low-level input voltage, V_{IL}, is applied to the STATUS FLAG DISCONNECT (pin 16) control line. Wired OR capability is provided on this line, allowing OE lines from other arrays to be OR tied. A high level output voltage, V_{OH}, indicates that the previously received character was not read (DR line not reset) before the present character was transferred to the RECEIVER HOLDING REGISTER.
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR, and THRE circuit outputs.
17	RECEIVER REGISTER CLOCK	RRC	This clock is sixteen (16) times faster than the desired receiver shift rate.
18	DATA RECEIVED RESET	DRR	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic after power turn-on. It resets all registers and sets the serial output line to a high-level output voltage, V_{OH}.
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.

Table 4-1. UART Specifications (Continued)

PIN NUMBER	NAME	SYMBOL	FUNCTION
23	TRANSMITTER HOLDING REGISTER LOAD	THRL	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit DATA bits, PARITY bit, and STOP bit), are serially shifted out on this line. This line will remain at a high level output voltage, V_{OH}, when no data is being transmitted. A start of transmission is defined as the transition from a high-level output voltage, V_{OH}, to a low-level output voltage, V_{OL}, of the start bit.
26-33	TRANSMITTER REGISTER DATA INPUTS	TR_1-TR_8	Parallel 8-bit characters are input on these lines into the TRANSMITTER HOLDING REGISTER with THRL strobe. If a character of less than eight bits has been selected (by WLS_1 and WLS_2), the least significant bits only are accepted. The character is right justified into the least significant bit. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.

Table 4-1. UART Specifications (Continued)

PIN NUMBER	NAME	SYMBOL	FUNCTION
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH}, on the line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard-wired to a high-level input voltage, V_{IH}.
35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits. The STOP bit(s) will immediately follow the last data bit on transmission if parity is inhibited. A low-level input voltage, V_{IL}, enables the parity generation and verification circuits. PI will, when a high-level input voltage, V_{IH}, is applied, also clamp the PE line (pin 13) to a low-level output voltage, V_{OL}.
36	STOP BIT(S) SELECT	SBS	This line selects the number of STOP bits generated after the PARITY bit during transmission. A high-level input voltage, V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit.
37-38	WORD LENGTH SELECT	WLS_2-WLS_1	These two lines select the character length to be 5, 6, 7 or 8 bits. WLS_2 / WLS_1 / WORD LENGTH V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
39	EVEN PARITY ENABLE	EPE	This line selects either even or odd PARITY to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	TRANSMITTER REGISTER CLOCK	TRC	This CLOCK is sixteen (16) times faster than the desired transmitter shift rate.

4.1.7 Video Logic (Schematic P. 5, 6, 7, 11, 12, 19)

The video logic section of the main logic board includes all circuitry necessary to generate and transfer video information for monitor display. Video data and timing consist of:

- Horizontal and vertical timing for the CRT
- Video data to be displayed
- RAM output data
- Cursor display
- Protected field data

Figure 4-6 is a block diagram of the video logic section.

As shown on schematic page 5, the RAM output data (PRDx) is stacked in two 4-bit by 80-character shift registers (designated M11 and L11 on the schematic). RAM data is accessed one 80-character line at a time and sent to the shift register in 8-bit words.

Memory addressing of the RAM during display operations is controlled by (CPC2,4 and CLC1,2, 4,8,16) from the timing (counter) circuit. The characters in the shift register are shifted out one at a time as (SRx) to a character buffer and then to the character generator (character buffer and character generator are located on schematic P. 6). This serial shift-out operation occurs after the video logic initiates a horizontal raster scan (via CHC).

The lower five bits of the character generator are input directly to the video shift register (designated M7 in the schematic). Bits 1-7 are decoded to determine if a NULL code is required.

Gate (M5) inputs the results of the decoding into the character video shift register. The video shift register serializes the video data and gates it through a video driver network, which transmits the data to the monitor. The driver network decodes the condition of bit 8 of the character buffer (determined by flip-flop L6) to determine protect status. If a character is protected (bit 8 true), the video driver network outputs a slightly lower voltage level to the monitor, causing a reduced intensity.

The character generator produces the displayable video pulses which comprise the 5 by 7 inch dot matrix, illustrated in Section 1, Figure 1-2. For each line displayed, the character generator must receive all 80 characters seven times. It must generate seven lines of video pulses, one for each raster sweep. The raster count lines (CHC1,2,4,8) inform the character generator which sweep is currently taking place.

The character generator repeats the above operation 24 times (once for each screen line), inserting the necessary blanked raster lines for vertical interline spacing. The entire screen is refreshed at a 60 Hz rate.

Cursor Display (Schematic P. 6, 7, 11, 12)

The cursor logic includes position, tracking, and generation of the cursor on the CRT. Figure 4-7 illustrates, in block diagram form, the cursor logic on the main logic board.

The cursor is generated, positioned, and tracked by the MACC and MACR, MAC and CPR logic (schematic P. 11, 12). The indicator register receives cursor position data from the RAM via the TSB. Indicator register output bits (INDx) are sent to the indicator multiplexer, an eight-to-one device. The output signal of this multiplexer (INDICATOR VIDEO) is the actual video generator to the CRT. The signal is applied to the video driver logic (schematic P. 6) for transmission to the monitor.

The cursor position, as contained in the MACR and MACC control comparator logic (schematic P. 11) J21, J22, H20, is compared with the display address lines (CLCx and CPCx). When the display scan reaches the cursor position, the two addresses will be equal. A cursor video gate is generated (CURSOR). The CURSOR signal is applied to the video driver logic (P. 6) and sent to the monitor. The MACC and MACR condition circuit (P. 11, upper left) tracks the cursor continually and outputs a signal when the cursor is either at the end of page (bottom) or end of line (80th position). The signal out of this circuit (MAC COND) is applied to the condition input circuit (P. 8). The condition input circuit is used to control the program counter. The program counter, with the condition output signal (generated by the multiplexer designated E23), will access command memory (ROM), causing a new page to begin on the screen via a command from the microprogram.

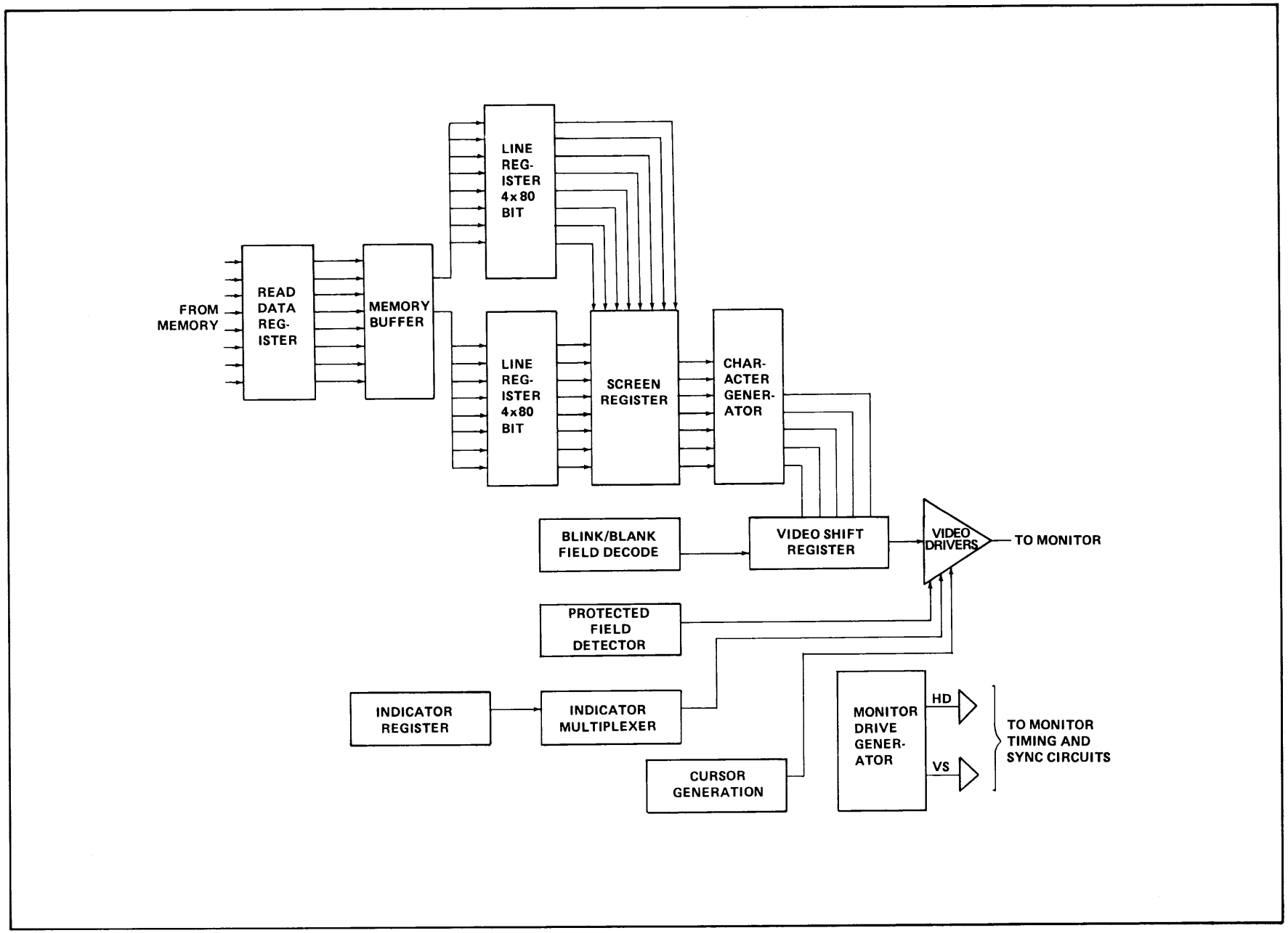


Figure 4-6. Video Logic Block Diagram

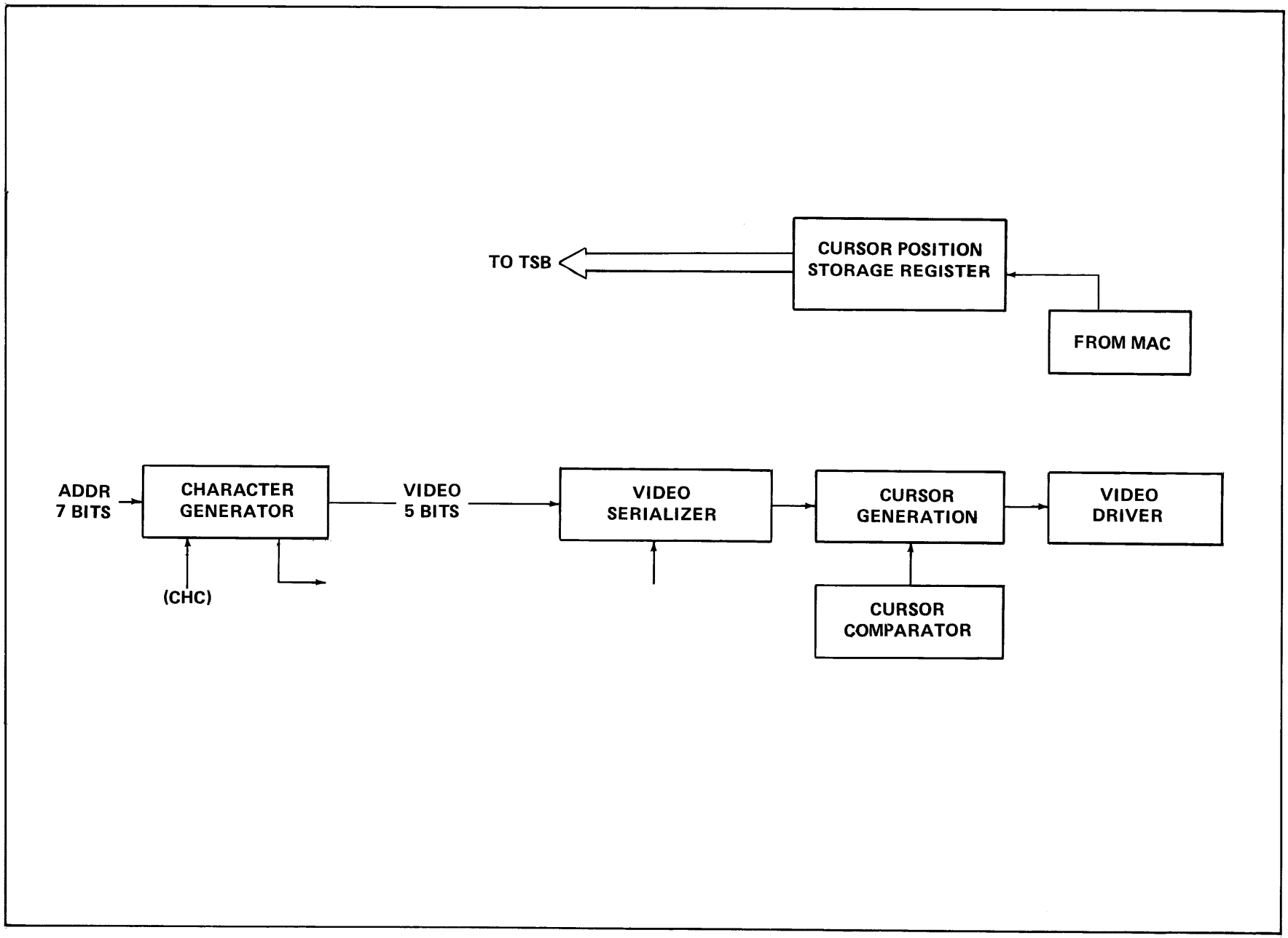


Figure 4-7. Cursor Logic Block Diagram

The memory address control logic (P. 11, middle) decodes the commands from the microprocessor directing the MAC and CPR counters (P. 12) to either load data or count up or down. The output signals from the control circuit (MACRLOD, MACRUP1, MACRDN1, MACCLOD, MACCUPC, MACCDNC) are applied to the input pins (4, 5, 11) of the up/down counters (H21, H22) on page 12.

The H21 counter circuit determines in what row the cursor is positioned and feeds this data to a compare circuit to determine whether the cursor is on the same row as it was when loaded. The H22 circuit feeds character position holding counters, which keep track of where the cursor is now and where it was first loaded. When the (MACR=CPRR) compare is made, the program terminates the transmission.

Monitor Drive Logic (Schematic P. 19)

The monitor driver circuit provides horizontal and vertical deflection signals to the CRT. The character position counter (CPC) clocks the J12 flip-flop and provides position information on terminal J4, pin 8 to the monitor. At column 80, a CPC pulse is gated to the character line counter. When CHC=9 and CLC=23, the vertical drive circuit counter is enabled. Vertical drive (V DRIVE) information is output to the monitor from J4, pin 9.

Blink and Blank Fields (Schematic P. 6, 7)

The video logic contains circuitry to produce a blinking field of data. The blink clock (produced by a one-shot counter) is gated with bit 6 of the character generator word (bit 6=true) to the indicator video multiplexer to produce a field blinking rate of four images per second. The blink clock is also applied as input pulses to a selection circuit (P. 6) for determining blink/blank.

The blank field operation is used for security purposes. The operator may designate particular fields in the character memory (RAM) to be non-display fields. The video indicator multiplexer decodes inputs to the character generator to determine if the blank field status should be set. The blank bit is applied to the same selection circuit as the blink bit for determining its condition before it is input to the video shift register.

Flip-flop K4 (P. 6) sets the save blink field (SAVBLKFLD) and save blank field (SAVSUPFLD). Flip-flop K5 (P. 6) sets the set blink field (BLK FLD) and set blank (suppress) field (SUPFLD) status.

4.1.8 Data Memory Address Logic (Schematic P. 3)

The memory address register (MACC and MACR on P. 12) is used to keep track of read and write memory data locations. The register outputs are sent to the data memory address logic (2:1 data selectors). The memory address register output signals (MACC1-7 and MACR1-5) are paired with character line and position counter signals to generate line and position coordinates for the display data. These coordinates are fed to another data selector circuit, which generates the proper RAM address.

4.1.9 Protect Mode Logic (Schematic P. 19)

The protect mode status bit is used as a global condition by the program to disable the overwriting of any characters in the RAM for which the write protect bit (bit 8) is set.

Flip-flop B13 is set, identifying the protect mode, when the input gate (C13) decodes the set protect mode command from the microprogram. The output signal (PROTMODE) is input to the operational mode multiplexer, which transmits the protect mode condition on the COND B output to the control logic. All data subsequently written into the RAM is checked to determine if bit 8 (write protect bit) is set.

With protect mode initiated, all characters with their write protect bit set are protected against overwriting. Multiplexer input gate (C14) detects protected characters upon input to the multiplexer. Output (COND B) informs the control logic that a character is protected.

4.1.10 Program Counter Logic (Schematic P. 8)

The program counter performs the same function in the ADM-2 as in any other system. The counter addresses command memory locations (ROM addresses) in sequential order, unless a jump condition exists; then it accesses the specified location set forth in the program. The counter is controlled by program counter control logic and by the condition input logic.

The program counter is a three stage binary counter (designated F25, F26, and F24 which is the page register, in the schematic). It is loaded from ROM output bits (CM0-7) and literal register output bits (LIT1-4). The program counter accesses ROM locations via 12 output lines (CMA0-11), which are also input to the command memory address register. The two most significant bits (CMA10, 11) enable the ROM chips.

The program counter control logic inhibits the program counter during memory busy and specified microprogram command operations (i.e., two-cycle instructions). A decoding circuit is used to detect the presence of an inhibiting command and output a counter inhibit signal (ENPC) which is applied to pin 10 of the program counter. The counter is disabled until a new enable signal is input or the logic is reset (in the case of a two-cycle instruction).

The condition input logic controls the program counter during jump conditions and special status conditions, which require program counter operations. An example of this type of operation occurs when the cursor is at position 80 on the last line of the screen. When an overflow occurs, the ROM must output a new instruction either starting a new screen page or terminating the operation.

4.1.11 Reset Logic (Schematic P. 17)

The ADM-2 has an automatic reset function for power-up operation. A keyboard or external reset may also be performed and produces the same reset signal as the power-up reset. The power-up reset (KRESETL) is provided by the one-shot (H3) pulsing gate J3.

4.1.12 Beeper Logic (Schematic P. 17)

The beeper logic produces an audible tone upon "power up" or receipt of a bell code. The signal that drives the speaker (CLC1) is the character line counter. (CLC1) is enabled to the speaker during one-shot operation (the only time the gate F3 is true).

4.1.13 Optional Timeout Logic (Schematic P. 17)

An optional timer is available for command decoding and noting a status condition. The output (COND TIME) signal is applied to the condition input logic. This option is useful for preventing a system "hang-up" and controlling the program counter when a timeout occurs.

4.1.14 Polling Option Logic (Schematic P. 17)

The polling option logic includes a switch bank, a set of drivers, and a margin register that connect to the TSB. The logic stores the address set by the switches. Up to 96 terminal addresses may be selected by the A6 switch bank. When the TSB is equal to the address selected by the switches, the logic is enabled and the terminal is in the polling network. Two extra pages of control memory are required to utilize this option.

Closing the switch produces a logic "0" for the associated bit. An open switch produces a logic "1" for the associated bit.

4.1.15 Printer Interface Option (Schematic P. 23)

The printer interface option decodes the printer commands from the program at gate C13 and issues a request-to-send (RTS) signal to the printer. The user must choose the RTS connection to the J3 terminal at installation. On the -13 logic board, the switches at A18 are used to select output pins 6 and/or 8 on J3. Switch 3 selects a loop back option, causing the RTS signal to automatically generate a clear-to-send (CTS) signal. If switch 3 is opened, the printer must send a CTS signal to the terminal. Switch 4 completes the loop back circuit.

On the -7 logic board, the same options are provided for with the use of jumpers.

J3 pin 2 and pin 3 are transmit and receive signals (respectively). They are sent to the I/O interface for input to the UART logic.

4.2 MONITOR LOGIC

4.2.1 Video Amplifier

The video amplifier consists of Q101 and its associated circuitry.

The incoming video signal is applied to the monitor through the contrast control through R109 to the base of transistor Q101.

Transistor Q101 and its components comprise the video output driver, with a gain of about 17. Q104, operating as a class B amplifier, remains cut off until a DC-coupled, positive-going signal arrives at its base and turns on the transistor. R111 adds series feedback, which makes the terminal-to-terminal voltage gain relatively independent of transistor variations as well as stabilizes the device against voltage and current changes caused by ambient temperature variations.

The negative-going signal at the collector of Q101 is DC-coupled to the cathode of the CRT. The class B biasing of the video driver allows a larger video output signal to modulate the CRT's cathode, resulting in a maximum available contrast ratio.

The overall brightness at the screen of the CRT is determined by the negative potential at the grid and is varied by the brightness control.

4.2.2 Vertical Deflection

Transistor Q102 is a programmable unijunction transistor and, together with its external circuitry, forms a relaxation oscillator operating at the vertical rate. Resistor R115, variable resistor R116, and capacitors C105 and C106 form an RC network providing proper timing.

When power is applied, C105 and C106 charge exponentially through R115 and R116 until the voltage at the junction of R116 and C105 equals the anode "A" firing voltage. At this time, one of the unijunction's diodes that is connected between the anode and anode gate "G" becomes forward biased, allowing the capacitors to discharge through another diode junction between the anode gate and the cathode "K" and on through R120.

R117 and R118 control the voltage at which the diode (anode-to-anode gate) becomes forward biased. This feature "programs" the firing of Q102 and prevents the unijunction from controlling this parameter. Therefore, the changing of firing points from one device to another, together with the temperature dependency of this parameter, is no longer the problem it was with conventional unijunction transistors.

The vertical oscillator is synchronized externally to the vertical interval from the vertical drive pulse at R113. At the time of the vertical interval, an external negative pulse is applied through R113, C104, and CR101 to the gate of Q102, causing the firing level of the unijunction to decrease.

The sawtooth voltage at the anode of Q102 is directly coupled to the base of Q103. Q103 is a driver amplifier and has two transistors wired as a Darlington pair. Their input and output leads exit as a three-terminal device. This device exhibits a high input impedance to Q102, and thereby maintains excellent impedance isolation between Q102 and Q104.

The output waveform from the unijunction oscillator is not suitable, as yet, to produce a satisfactory vertical sweep. Such a waveform would produce severe stretching at the top of the picture and compression at the bottom. C105 and C106 modify the output waveform to produce satisfactory linearity. The sawtooth waveform output at Q103 is coupled through R122, the vertical linearity control R121, and on to C106, where the waveform is shaped into a parabola. This parabolic waveform is then added to the oscillator's waveform and changes its slope. Slope change rate is determined by the position of the variable resistor R121.

Q103 supplies base current through R123 and R124 to the vertical output transistor, Q104. Height control R124 varies the amplitude of the sawtooth voltage present at the base of Q104 and, therefore, varies the size of the vertical raster on the CRT.

The vertical output stage, Q104, uses a power type transistor which operates as a class A amplifier. No output transformer is required, since the output impedance of the transistor permits a proper impedance match with the yoke connected directly to the collector. C107 is a DC-blocking capacitor which allows only AC voltages to produce yoke current. L1 is a relatively high impedance compared to the yoke inductance. During retrace time, a large positive pulse is developed by L1 which reverses the current through the yoke and moves the beam from the bottom of the screen to the top. Resistor R126 prevents oscillations by providing damping across the vertical deflection coils.

4.2.3 Horizontal Deflection

To obtain a signal appropriate for driving Q106, the horizontal output transistor, a driver stage consisting of Q105 and T101, is used. The circuitry associated with Q105 and Q106 has been designed to optimize the efficiency and reliability of the horizontal deflection circuits.

A positive going pulse is coupled through R127 to the base of Q105. The amplitude and duty cycle of this waveform must be as indicated in the electrical specifications (refer to Section 1.3) for proper circuit operation.

The driver stage is either cut off or driven into saturation by the base signal. The output signal appears as a rectangular waveform and is transformer-coupled to the base of the horizontal output stage. The polarity of the voltage at the secondary of the driver transformer is chosen such that Q106 is cut off when Q105 conducts and vice versa.

During conduction of the driver transistor, energy is stored in the coupling transformer. The voltage at the secondary is then positive and keeps Q106 cut off. As soon as the primary current of T101 is interrupted due to the base signal driving Q105 into cutoff, the secondary voltage changes polarity. Q106 starts conducting, and its base current flows. This gradually decreases at a rate determined by the transformer inductance and circuit resistance.

The horizontal output stage has four main functions:

- to supply the yoke with the correct horizontal scanning currents,
- to develop a "C" VDC supply voltage for use with the CRT,
- to develop a "B" VDC supply voltage for the video output stage, and
- to develop a "D" VDC for the CRT bias.

Q106 acts as a switch which is turned on or off by the rectangular waveform on the base. When Q106 is turned on, the supply voltage plus the charge on C113 causes yoke current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a positive voltage on its base, which causes the output circuit to oscillate. A high reactive voltage in the form of a half cycle negative voltage pulse is developed by the yoke's inductance and the primary of T2. The peak magnetic energy which was stored in the yoke during scan time is then transferred to C109 and the yoke's distributed capacity. During this cycle, the beam is returned to the center of the screen.

The distributed capacity now discharges into the yoke and induces a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the yoke moves the scanning beam to the left of the screen.

After slightly more than half a cycle, the voltage across C109 biases the damper diode CR103 into conduction and prevents the flyback pulse from oscillating. The magnetic energy that was stored in the yoke from the discharge of the distributed capacity is released to provide sweep for the first half of the scan and to charge C113 through the rectifying action of the damper diode. The beam is then at the center of the screen. The cycle will repeat as soon as the base voltage of Q106 becomes negative.

C113, in series with the yoke, also serves to block DC currents through the yoke and to provide "S" shaping of the current waveform. "S" shaping compensates for stretching at the left and right sides of the picture tube because the curvature of the CRT face and the deflected beam do not describe the same arc.

L101 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductive reactance allows a greater or lesser amount of the deflection current to flow through the horizontal yoke and, therefore, varies the width of the horizontal scan.

The negative flyback pulse developed during horizontal retrace time is rectified by CR104 and filtered by C110. This produces approximately "D" VDC which is coupled through the brightness control to the cathode of the CRT (V1).

This same pulse is transformer-coupled to the secondary of transformer T2 where it is rectified by CR2, CR106, and CR105 to produce rectified voltages of approximately 12KV (9 and 12 inches) or 9KV (5 inches), "C" VDC, and "B" VDC, respectively. 12KV or 9KV is the anode voltage for the CRT, and "C" VDC serves as the source voltage for grids No. 2 and 4 (focus grid) of the CRT. The "B" VDC potential is the supply voltage for the video output amplifier, Q101.

4.2.4 Low Voltage Regulated Supply

The monitor uses a series-pass, low voltage regulator designed to maintain a constant DC output for changes in input voltage, load impedance and temperature. Also included is a current limiting circuit designed to protect transistors connected to the "A" VDC output of the regulated supply from accidental output short circuits and load malfunctions.

The low voltage regulator consists of Q201, Q202, Q1, VR201, and their components. Q203 and its circuitry control the current limiting feature.

The 120 VAC primary voltage (220/240 V, optional) is stepped down at the secondary of T1 where it is rectified by a full wave bridge rectifier CR1. Capacitor C1 is used as a filter capacitor to smooth the rectified output of CR1. Transistor Q1 is used as a series regulator to drop the rectified voltage to "A" VDC and to provide a low output impedance and good regulation. Resistor network R207, R208 and R209 is used to divide down the "A" VDC voltage to approximately +6 VDC and apply this potential to the base of Q202. A reference voltage from zener diode VR201 is applied to the emitter of Q202. If the voltages applied to the base and emitter of Q202 are not in the proper relationship, an error current is generated through Q202. This error current develops a voltage across R202 which is applied to the base of emitter follower Q201 and then applied to the base of Q1 to bring the output voltage back to its proper level. R201 and C201 provide additional filtering of the rectified DC voltage.

Operation of this regulator may be better understood by assuming that a certain operation condition has caused the output voltage to increase above normal. This positive increase of voltage is transferred to the base of Q202 where it is compared to the zener voltage of VR201. The increase of forward bias of Q202 causes the collector voltage to drop as a result of the increased collector current through R202. This voltage is directly coupled to the base of Q1 through Q201, where it causes Q1 to conduct less and brings the regulated voltage back to its proper state.

The short circuit protection or current limiting action can be explained as follows: Assume the "A" VDC bus becomes shorted to ground. This reduced output voltage is sensed by the base of Q202, turning that transistor off because of the reverse bias across its emitter and base junction. Simultaneously, the increased current through R204 increases the forward voltage drop across the base and emitter junction of Q203 and turns it on. Prior to the short circuit condition, Q203 was cut off. The increased collector current through R202 decreases the collector voltage of Q203, which is detected by the base of Q201 and direct-coupled to the base of Q1, causing that conductor to conduct less. This closed loop operation maintains the current available to any transistor connected to the "A" VDC bus at a safe level during a short circuit condition. Circuit breakers and fuses are often used for this purpose. However, in the majority of cases these devices are not fast enough to protect transistors.

SECTION FIVE
OPERATOR CONTROLS & KEYBOARD

This section describes the controls, indicators, switches and keyboard used to operate the ADM-2 Interactive Display Terminal.

5.1 ADM-2 BACK PANEL CONTROLS

(These controls are shown in Figure 5-1.)

Figure 5-1. ADM-2 Back Panel View

5.1.1 Power ON/OFF Switch

The Power ON/OFF switch is located on the top right side of the back panel. This switch controls all power to the ADM-2. Placing the switch in the ON position will reset all ADM-2 circuitry, position the cursor at "HOME," and clear the display memory to unprotected space codes.

5.1.2 Mode Selector Switch

The Mode Selector Switch is located on the bottom left side of the back panel. The Mode Selector Switch is a three-position switch that selects full (F), or half (H) duplex conversational modes of operation or, in the middle position (B), selects the block transmission mode.

5.1.3 EIA Switch

This switch, located on the bottom right of the back panel, selects either the RS-232-C or current loop interface mode for communications.

5.1.4 Baud Rate Switch

This switch, located on the bottom right side of the back panel, selects the baud rate to be used. This is an eight-position thumb switch (0-7); switch settings and their corresponding baud rates are:

BAUD RATE	SETTING
110	7
105	6
300	5
600	4
1200	3
2400	2
4800	1
9600	0

5.1.5 Contrast Adjustment

This control sets the brightness of the displayed characters in relation to the display background. The contrast control should be adjusted after adjusting the brightness control.

5.1.6 Brightness Adjustment

The brightness adjustment, located on the bottom extreme right of the back panel, controls CRT brightness. It should be adjusted to the point at which characters are easily visible on the display (white characters and a black background).

The brightness control should be adjusted so that the white raster is just barely extinguished from the screen.

5.2 KEYBOARD

The ADM-2 terminal keyboard contains 118 keys (refer to Figure 1-3). The keyboard can be detached and located up to five feet from the display unit. The keyboard is designed with key rollover protection (i.e., if a key is depressed before a previously depressed key is released, the second key code cannot be transmitted until release of the first key).

The keyboard contains the following functional keys:

- Upper case
- Numeric
- Special characters
- Special characters with shift
- Special characters with CTRL or Shift/CTRL
- Special function keys.

An optional keyboard able to generate lower case letters may be installed. Keyboard operations are depicted in Table 5-1.

5.2.1 Data Keys

Depression of a data key will produce an ASCII 7-bit binary code which can be either stored in memory, displayed, or/and transmitted to the data interface.

There are 96 ASCII character codes that can be stored or displayed with the standard keyboard. Table 5-2 lists the available 96 ASCII binary codes and the keys that produce them.

Each depression of a data key produces a unique machine code that corresponds to the symbol on the keyboard. When two characters are shown on one key, the upper symbol is produced in the shift mode. The lower symbol is produced by depressing the key alone. Data keys do not repeat if held down like some of the special function keys.

The ADM-2 keyboard can be enabled and disabled locally using the following sequence of keystrokes, or remotely by computer control using ASCII codes:

ESC #	disables all keyboard functions except RESET
ESC "	enables the keyboard and restores keyboard control.

Since the ESC # sequence may be accidentally initiated manually, the keyboard is protected and may need to be unlocked by depressing the RESET key.

5.2.2 Shift Lock Key

This key locks the shift function for continuous use; data keys produce the code for the top symbol indicated on the key. The shift lock key has no effect on the special functions: PRINT, SEND, CLEAR, EDIT, or TAB keys. The shift lock is cleared by operation of either shift key.

5.2.3 Special Function Keys

The ADM-2 terminal has sixteen special function keys. These keys allow the operator to give concise three-code responses to frequently used inquiries or to direct the computer to access special programs or subroutines. The special function keys are identified as F1 through F16 at the top of the keyboard (refer to Figure 1-3). Table 5-3 depicts the special function keys with their transmitted codes.

5.2.4 Control Keys

The keyboard provides a number of control keys which are used for cursor, terminal, and data transmission operations. These keys and their uses are depicted in Table 5-1.

5.2.5 Status Keys

The keyboard provides the ADM-2 with a local method to set or clear status conditions. The eight indicators, on the right side of the display, show the current status conditions. Table 5-4 depicts the status conditions and the key or keys utilized to set or clear the status condition.

Table 5-1. ADM-2 Keyboard Operations

OPERATION	KEYS USED
CHARACTER DISPLAY	
1. Alphabetic Upper Case	A to Z
2. Alphabetic Lower Case (Optional with SHIFT)	a to z
3. Numeric	0 to 9 Main Keyboard or Numeric
4. Special Characters	: _ @ - [ ] ; ^ \ , . /
5. Special Characters with SHIFT	! " # $ % & ' ( ) * = ` { } + ~ ¦ < > ?
6. Special Characters with CTRL or CTRL/SHIFT	See below

ASCII CODE	DISPLAYED CHARACTER	KEYS USED
NULL		
SOH	A	CTRL/A
STX	◀	SHIFT/SOM-EOM, CTRL/B
ETX	▶	SOM-EOM, CTRL/C
EOT	D	CTRL/D
ENQ	E	CTRL/E
ACK	F	CTRL/F
BEEP	G	CTRL/G
BS	←	←, CTRL/H
HT	•	TAB, CTRL/I
LF	↓	LF, ↓, CTRL/J
VT	↑	↑, CTRL/K
FF	→	→, CTRL/L
CR	◢	RETURN, CR, CTRL/M
SO	≥	CTRL/N
SI	≤	CTRL/O
DLE	0	CTRL/P
DC1	1	CTRL/Q
DC2	2	CTRL/R
DC3	3	CTRL/S
DC4	4	CTRL/T
NAK	U	CTRL/U
SYN	V	CTRL/V
ETB	W	CTRL/W
CAN	X	CTRL/X
EM	Y	CTRL/Y
SUB	Z	CTRL/Z
ESC	E	ESC, CTRL/[
FS	\	CTRL/
GS	]	CTRL/]
RS	↖	HOME
US	↵	NEW LINE

Table 5-1. ADM-2 Keyboard Operations (Continued)

OPERATION	KEYS USED
7. No Display (ASCII SP)	SPACE
8. Protect Displayed Characters	PROT MODE, WRITE PROT
CURSOR CONTROL	
1. Cursor HOME	HOME
2. Position in Line	
a. Left margin of Same Line b. Same Column of Next Line c. Left Margin of Next Line	RETURN, CR LF NEW LINE
3. Position New Field	TAB SET, TAB, BACKTAB
4. Increment Up Down Left Right	↑ ↓ ← →
TERMINAL CONTROL	
1. Reset	RESET
2. Break	BREAK
3. Clear Screen or Foreground to:	
a. Spaces b. Null Codes	CLEAR SP CLEAR NUL
4. Audible Tone	CTRL/G
5. Display Extended Memory Control (Optional)	PAGE FWD, PAGE BACK
DATA TRANSMISSION CONTROL	
1. Transmission Mode	BLOCK MODE, CONV MODE
2. Transmission Initiation (Block Mode)	SEND LINE, SEND MESSAGE, SEND PAGE
3. Send to Printer	PRINT
4. Transmitted Text Delimiters	SOM - EOM
5. Special Functions	F1 to F16

Table 5-2. ASCII Codes with Associated Keys

KEY	LEGEND	UNSHIFTED 1st	UNSHIFTED 2nd	SHIFT 1st	SHIFT 2nd	CTRL 1st	CTRL 2nd	CTRL SHIFT 1st	CTRL SHIFT 2nd
1	F1	DC1	40	DC1	60	DC1	40	DC1	60
2	F2	DC1	41	DC1	61	DC1	41	DC1	61
3	F3	DC1	42	DC1	62	DC1	42	DC1	62
4	F4	DC1	43	DC1	63	DC1	43	DC1	63
5	F5	DC1	44	DC1	64	DC1	44	DC1	64
6	F6	DC1	45	DC1	65	DC1	45	DC1	65
7	F7	DC1	46	DC1	66	DC1	46	DC1	66
8	F8	DC1	47	DC1	67	DC1	47	DC1	67
9	F9	DC1	48	DC1	68	DC1	48	DC1	68
10	F10	DC1	49	DC1	69	DC1	49	DC1	69
11	F11	DC1	4A	DC1	6A	DC1	4A	DC1	6A
12	F12	DC1	4B	DC1	6B	DC1	4B	DC1	6B
13	F13	DC1	4C	DC1	6C	DC1	4C	DC1	6C
14	F14	DC1	4D	DC1	6D	DC1	4D	DC1	6D
15	F15	DC1	4E	DC1	6E	DC1	4E	DC1	6E
16	F16	DC1	4F	DC1	6F	DC1	4F	DC1	6F
17	SEND PAGE	ESC	35	ESC	37	ESC	35	ESC	37
18	SEND LINE	ESC	34	ESC	36	ESC	34	ESC	36
19	SEND MESSAGE	ESC	53	ESC	73	ESC	53	ESC	73
20	PRINT	ESC	50	ESC	70	ESC	50	ESC	70
21	CLEAR SPACES	ESC	3B	ESC	2B	ESC	3B	ESC	2B
22	CLEAR NUL	ESC	3A	ESC	2A	ESC	3A	ESC	2A
23	PAGE EDIT	ESC	4E	ESC	4F	ESC	4E	ESC	4F
24	CHAR INSERT	ESC	51	ESC	51	ESC	51	ESC	51

Table 5-2. ASCII Codes with Associated Keys (Continued)

KEY	LEGEND	UNSHIFTED 1st	UNSHIFTED 2nd	SHIFT 1st	SHIFT 2nd	CTRL 1st	CTRL 2nd	CTRL SHIFT 1st	CTRL SHIFT 2nd
25	CHAR DELETE	ESC	51	ESC	57	ESC	57	ESC	57
26	LINE INSERT	ESC	45	ESC	45	ESC	45	ESC	45
27	LINE DELETE	ESC	52	ESC	52	ESC	52	ESC	52
28	LINE ERASE	ESC	54	ESC	74	ESC	54	ESC	74
29	PAGE ERASE	ESC	59	ESC	79	ESC	59	ESC	79
30	WRITE PROT	ESC	28	ESC	29	ESC	28	ESC	29
31	PROT MODE	ESC	26	ESC	27	ESC	26	ESC	27
32	PROG MODE	ESC	55	ESC	75	ESC	55	ESC	75
33	CONV MODE	ESC	42	ESC	43	ESC	42	ESC	43
34	-	2D		2D		2D		2D	
35	TAB	09		09		09		09	
36	1 !	31		21		31		21	
37	2 ”	32		22		32		22	
38	3 #	33		23		33		23	
39	4 $	34		24		34		24	
40	5 %	35		25		35		25	
41	6 &	36		26		36		26	
42	7 ’	37		27		37		27	
43	8 (	38		28		38		28	
44	9 (	39		29		39		29	
45	0	30		30		30		30	
46	: *	3A		2A		3A		2A	
47	_ =	2D		3D		2D		3D	

Table 5-2. ASCII Codes with Associated Keys (Continued)

KEY	LEGEND	UNSHIFTED 1st	UNSHIFTED 2nd	SHIFT 1st	SHIFT 2nd	CTRL 1st	CTRL 2nd	CTRL SHIFT 1st	CTRL SHIFT 2nd
48	@ `	40		60		40		60	
49	- RUBout	5F		7F		5F		7F	
50	BREAK	-		-		-		-	
51	PAGE BACK	ESC	4A	ESC	6A	ESC	4A	ESC	6A
52	TAB SET	ESC	56	ESC	76	ESC	56	ESC	76
53	SOM EOM	ESC	03	ESC	02	ESC	03	ESC	02
54	7	37		37		37		37	
55	8	38		38		38		38	
56	9	39		39		39		39	
57	CTRL	—		—		—		—	
58	Q	71		51		11		11	
59	W	77		57		17		17	
60	E	65		45		05		05	
61	R	72		52		12		12	
62	T	74		54		14		14	
63	Y	79		59		19		19	
64	U	75		55		15		15	
65	I	69		49		09		09	
66	O	6F		4F		0F		0F	
67	P	70		50		10		10	
68	[{	5B		7B		1B		1B	
69	] }	5D		7D		1D		1D	
70	ESC	1B		1B		1B		1B	
71	BACK TAB TAB	ESC	69	ESC	49	ESC	69	ESC	49

Table 5-2. ASCII Codes with Associated Keys (Continued)

KEY	LEGEND	UNSHIFTED 1st	UNSHIFTED 2nd	SHIFT 1st	SHIFT 2nd	CTRL 1st	CTRL 2nd	CTRL SHIFT 1st	CTRL SHIFT 2nd
72	PAGE FWD	ESC	4B	ESC	6B	ESC	4B	ESC	6B
73	↑	0B		0B		0B		0B	
74	CR ret	0D		0D		0D		0D	
75	4	34		34		34		34	
76	5	35		35		35		35	
77	6	36		36		36		36	
78	SHIFT LOCK	-		-		-		-	
79	A	61		41		01		01	
80	S	73		53		13		13	
81	D	64		44		04		04	
82	F	66		46		06		06	
83	G	67		47		07		07	
84	H	68		48		08		08	
85	J	6A		4A		0A		0A	
86	K	4B		4B		0B		0B	
87	L	6C		4C		0C		0C	
88	; +	3B		2B		3B		2B	
89	^ ∿	5E		7E		0E		0E	
90	\ ¦	5C		7C		0C		0C	
91	NEW LINE	1F		1F		1F		1F	
92	LF	0A		0A		0A		0A	
93	←	08		08		08		08	
94	HOME	1E		1E		1E		1E	
95	→	0C		0C		0C		0C	

Table 5-2. ASCII Codes with Associated Keys (Continued)

KEY	LEGEND	UNSHIFTED 1st	UNSHIFTED 2nd	SHIFT 1st	SHIFT 2nd	CTRL 1st	CTRL 2nd	CTRL SHIFT 1st	CTRL SHIFT 2nd
96	1	31		31		31		31	
97	2	32		32		32		32	
98	3	33		33		33		33	
99	SHIFT	-		-		-		-	
100	Z	7A		5A		1A		1A	
101	X	78		58		18		18	
102	C	63		43		03		03	
103	V	76		56		16		16	
104	B	62		42		02		02	
105	N	6E		4E		0E		0E	
106	M	6D		4D		0D		0D	
107	, <	2C		3C		2C		3C	
108	. >	2E		3E		2E		3E	
109	/ ?	2F		3F		2F		3F	
110	SHIFT	-		-		-		-	
111	RETURN	0D		0D		0D		0D	
112	RESET	-		-		-		-	
113	↓	0A		0A		0A		0A	
114	NEW LINE	1F		1F		1F		1F	
115	,	2C		2C		2C		2C	
116	0	30		30		30		30	
117	.	2E		2E		2E		2E	
118		20		20		20		20	

Table 5-3. Special Function Keys with Transmitted Codes

SPECIAL FUNCTION KEY	CODE TRANSMITTED	
	SINGLE KEY	WITH SHIFT
F1	SOH @ CR	SOH ` CR
F2	SOH A CR	SOH a CR
F3	SOH B CR	SOH b CR
F4	SOH C CR	SOH c CR
F5	SOH D CR	SOH d CR
F6	SOH E CR	SOH e CR
F7	SOH F CR	SOH f CR
F8	SOH G CR	SOH g CR
F9	SOH H CR	SOH h CR
F10	SOH I CR	SOH i CR
F11	SOH J CR	SOH j CR
F12	SOH K CR	SOH k CR
F13	SOH L CR	SOH l CR
F14	SOH M CR	SOH m CR
F15	SOH N CR	SOH n CR
F16	SOH O CR	SOH o CR

Table 5-4. Status Displays

STATUS INDICATOR	CONDITION	KEY	SET STATUS	CLEAR STATUS
1	Keyboard Lock		ESC #	ESC "
2	* ADM-1 Mode		ESC %	ESC $
3	Unassigned		ESC c	ESC b
4	Unassigned		ESC e	ESC d
5	Unassigned		ESC g	ESC f
6	Message Waiting		ESC <	ESC >
7	Program Mode	PROG MODE	ESC U	ESC X
8	Page Edit Mode	PAGE EDIT	ESC N	ESC O

* ADM-1 Emulation Mode. If the ADM-2 is emulating an ADM-1 with serial printer, unformatted print must be requested by ESC p rather than ESC L.

5.3 BASIC OPERATOR PROCEDURES

5.3.1 ADM-2 System Start-Up

a. Connect the keyboard cable to the connector at the rear of the display unit.

b. Plug the power cord into a grounded 115V AC outlet.

c. Set the ON/OFF switch on the rear of the unit to the ON position.

d. The cursor should appear at the home position in approximately 20 seconds. The rest of the screen should be clear.

e. If the cursor does not appear after the 20 second warm-up period, adjust the brightness and/or contrast controls, as follows:

   The contrast control should be placed in the middle of its range. Then turn the brightness control clockwise until the screen is very bright; now back off the brightness slowly until the background is just visible. The cursor should be present at this time.

   Adjust the brightness and contrast for desired level of viewing.

The ADM-2 terminal is now ready for operation.

5.3.2 Initiating Escape Sequences

ESCAPE sequences are initiated locally by using the ESC key or remotely by computer control (transmitting an ASCII ESC code, which enables the ADM-2 under microprogram control to interpret the next character or string of characters as special control instructions). These sequences are used for:

a. Keyboard enabling/disabling

b. Formatting, i.e., field protection, field security and field blinking

c. Data transmission control: character, line, page or message

d. Data editing control

e. Absolute cursor addressing/reading

f. Selecting special operation modes

g. Controlling the serial printer (optional).

Table 5-5 is a list of escape sequences with the associated codes.

Table 5-5 is read as follows:

For a normal character set, locate the character desired under the GRAPHIC CHARACTER SET portion of the table. The number on top of the column represents the first three bits of the code (first digit); the numbers to the left and across from the character are the second four bits of the code (second digit).

The control set works in the same manner, except the CONTROL portion of the chart is used.

For the special codes, the escape key must be pressed in addition to the function key. For these operations, use the ESCAPE SEQUENCE portion of the table, again going to the top of the column for the first digit and to the left side (straight across) for the second digit of the code.

Table 5-5. ADM-2 Binary Codes

	CONTROL			GRAPHIC CHARACTER SET						ESCAPE SEQUENCE					
BITS	BITS	0	1	2	3	4	5	6*	7*	2	3	4	5	6	7
4321	765	000	001	010	011	100	101	110	111	010	011	100	101		
0000		NUL	DLE	SP	Ø	@	P	`	p				P PRINT PAGE		p UNFORMAT PRINT
0001		SOH	DC1	!	1	A	Q	a	q	!		A	Q INSERT CHAR		
0010		STX	DC2	"	2	B	R	b	r	" KBD ENA		B SET BLOCK	R DELETE LINE	b STATUS OFF	
0011		ETX	DC3	#	3	C	S	c	s	# KBD DISA		C SET CONV	S SEND MSG	c STATUS 1 ON	s SEND MSG ALL
0100		EOT	DC4	$	4	D	T	d	t	$ END MODE -1	4 SEND FG LINE	D	T ERASE LINE	d STATUS 2 OFF	t LINE TO NULL
0101		ENQ	NAK	%	5	E	U	e	u	% SET MODE -1	5 SENG FG PAGE	E INSERT LINE	U SET PGM MODE	e STATUS 2 ON	u CLR PGM MODE
0110		ACK	SYN	&	6	F	V	f	v	& SET PROTM	6 SEND ALL LINE	F	V SET TAB COLUMN	f STATUS 3 OFF	
0111		BEEP	ETB		7	G	W	g	w	/ CLEAR PROTM	7 SEND ALL PAGE	G	W DELETE CHAR	g STATUS 3 ON	
1000		(←) BS	CAN	(	8	H	X	h	x	(CLEAR WPROT		H	X CLEAR PGM MODE		
1001		(SKIP) HT	EM	)	9	I	Y	i	y	) SET WPROT		I BACK TAB	Y ERASE PAGE	i TAB (SKIP)	y PAGE TO NULL
1010		LF (↓)	SUB	*	:	J	Z	j	z	* CLEAR ALL NULL	: CLEAR FG NULL	J PAGE BACK	Z		
1011		VT (↑)	ESC	+	;	K	[	k	{	+ CLEAR ALL SPACE	; CLEAR FG SPACE	K PAGE FWD	[		
1100		FF (→)	FS	,	<	L	\	l	¦		< STATUS 4 ON	L	\		
1101		CR	GS	–	=	M	]	m	}		=	M	]		
1110		SO	(HOME) RS		>	N	^	n	~		> STATUS 4 OFF	N SET PAGE EDIT	^ START/END BLINK FIELD		
1111		SI	(NEW LINE) US	/	?	O	_	o	DEL		? READ CURSOR	O CLEAR PAGE EDIT	_ START/END BLANK FIELD		

*DISPLAYED AS UPPER CASE

5.3.3 Formatting Control

The operator can exercise format control from either the keyboard or the computer. Table 5-6 summarizes the format control functions available on the ADM-2. For detailed information on format control, refer to the ADM-2 Operator's Manual.

Table 5-6. Formatting Aids

FORMAT CONTROL	KEYBOARD CONTROL	COMPUTER CODES
Column Tab Set	TAB SET	ESC V
Tab	SHIFT-BACKTAB/TAB	ESC i, CTRL I
Back Tab	BACKTAB/TAB	ESC I
Blanked Security Field Start/End	ESC _	ESC _
Blinking Field Start/End	ESC ^	ESC ^
Protect Mode On	SHIFT-PROT MODE (Lit)	ESC &
Protect Mode Off	PROT MODE (Unlit)	ESC /
Write Protect Start	SHIFT-WRITE PROT (Lit)	ESC)
Write Protect End	WRITE PROT (Unlit)	ESC (

5.3.4 Data Editing

The ADM-2 has been designed with complete data editing capabilities. Editing may be done from either the keyboard or computer. Table 5-7 summarizes the data editing operations available. For detailed information on ADM-2 data editing operations, refer to the ADM-2 Operator's Manual.

Table 5-7. Data Editing Commands

OPERATION	KEYBOARD CONTROL	COMPUTER CODES
Clear Foreground to Spaces	CLEAR-SPACES	ESC ;
Clear Foreground to Null	CLEAR-NULL	ESC :
Clear All to Spaces	CLEAR-SPACES/SHIFT	ESC +
Clear All to Null	CLEAR-NULL/SHIFT	ESC *
Page Edit	PAGE EDIT	ESC N, ESC 0
Character Insert	CHAR-INSERT	ESC Q
Character Delete	CHAR DELETE	ESC W
Line Insert	LINE INSERT	ESC E
Line Delete	LINE DELETE	ESC R
Erase Line to Spaces	LINE ERASE	ESC T
Erase Page to Spaces	PAGE ERASE	ESC Y
Erase Line to Nuls	LINE ERASE/SHIFT	ESC t
Erase Page to Nuls	PAGE ERASE/SHIFT	ESC y

5.3.5 Cursor Control

Cursor addressing may be controlled from the keyboard or computer. A four character sequence (ESC=YX) is used to position the cursor, where Y and X represent the row and column coordinates of the cursor position desired. The HOME position (top row, leftmost column) is addressed by ESC=SPACE SPACE, and successive positions (down for Y or to the right for X) use ASCII codes in ascending order; these codes are shown in Table 5-8.

Table 5-8. ASCII Code Cursor Positioning

X or Y	ASCII CODE	X	ASCII CODE	X	ASCII CODE
1	SPACE	28	:	55	V
2	!	29	<	56	W
3	”	30	-	57	X
4	#	31	>	58	Y
5	$	32	?	59	Z
6	%	33	@	60	[
7	&	34	A	61	\
8	’	35	B	62	]
9	(	36	C	63	^
10	)	37	D	64	_
11	*	38	E	65	`
12	+	39	F	66	a
13	,	40	G	67	b
14	–	41	H	68	c
15	.	42	I	69	d
16	/	43	J	70	e
17	0	44	K	71	f
18	1	45	L	72	g
19	2	46	M	73	h
20	3	47	N	74	i
21	4	48	O	75	j
22	5	49	P	76	k
23	6	50	Q	77	l
24	7	51	R	78	m
25	8	52	S	79	n
26	9	53	T	80	o
27	;	54	U		

After the X coordinate is loaded, the position of the cursor is tested for protected status. If that position is protected, the cursor automatically skips to the first unprotected location in the forward direction.

The cursor's position may be transmitted to the data interface by the computer code ESC. The coordinates are transmitted as YX. This operation (i.e., transmitting of cursor position) cannot be initiated from the keyboard.

5.3.6 Data Transmission Control

The operator may be required to switch the ADM-2 data transmission mode from conversational to block, or vice versa. This is done locally by using the CONV MODE pushbutton key. The key is illuminated when the ADM-2 is in the conversational mode and unlighted when in the block transmission mode. The computer can initiate a mode change by transmitting an ESC B code for block mode or an ESC C code for conversational mode.

The operator may be required to select a baud rate and/or half or full duplex modes of operation. This procedure is explained in Section Two (Installation) of this manual.

Table 5-9 summarizes block transmission control functions. For detailed information on block transmission operator control, refer to the ADM-2 Operator's Manual.

Table 5-9. Block Transmission Functions & Controls

TRANSMISSION BLOCK	KEYS	COMPUTER ESC SEQUENCE
Special Function Command	F1 through F16	(none)
Defined Message (Foreground)	Send Message	ESC S
Defined Message (All)	Shift/Send Message	ESC s
Line (Foreground)	Send Line	ESC 4
Line (All)	Shift/Send Line	ESC 6
Page (Foreground)	Send Page	ESC 5
Page (All)	Shift/Send Page	ESC 7
Cursor Coordinates*	(See Note)	ESC ?

* Not available to operator; must be requested by computer.

5.4 OPERATOR PROCEDURES–POLLING MODE

Information to be sent by the terminal is first entered onto the display screen from the keyboard. To gain initial control of the keyboard, press CONV MODE key (if not in its lighted state), then type the information to be sent in response to polling.

When the information has been completely entered onto the display screen, press the appropriate keys (as follows) to enable the ADM-2 to respond to an incoming poll message:

a. **Send Line**, to cause the ADM-2 to send all unprotected characters on the line containing the cursor. To send all characters in the line, press with SHIFT key. The send operation is the same as the v or x forced SEND from the computer.

b. **Send Page**, to cause the ADM-2 to send all unprotected characters, through the previous cursor position, on the page. To send all characters in the displayed page, press along with SHIFT key. The send operation is the same as the w or y forced SEND from the computer.

c. **Send Message**, to cause the ADM-2 to send all unprotected characters in the display that are bracketed by SOM and EOM (STX and ETX) codes. To send all characters, press with SHIFT key. The send operation is the same as the z forced SEND from the computer.

If the terminal is in the ADM-1 mode of operation (entered by ESC % sequence, exited by ESC # sequence, and indicated by indicator 2 being on), the transmission of text is modified in the following manner:

a. The FS characters indicating the presence of protected fields are not sent.

b. The US characters indicating the movement from line to line are not sent.

When the "send" key is operated, the CONV key light will go out and the operator will no longer have control. If the operator wishes to regain control prior to the receipt of a POL sequence, he may do so by operating the RESET key which will return the ADM-2 to the idle state.

To remove the ADM-2 from polling mode operation and recover keyboard control, press CONV MODE key. This can also be done from the computer by inserting the ESC C at the end of the message.

NOTE

IF EOT, ETX, STX, ACK, NAK OR ANY CONTROL CHARACTER IS REQUIRED ON THE SCREEN, IT MUST BE PRECEDED BY AN ESC.

Function keys F1 through F16 will send four characters when the ADM-2 is polled. The character sequence is SOH text character ETX LRC. Note this is different than the normal message format in that the SOH replaces the STX.

To use any of the function keys, first depress the CONV key required to enable the keyboard and set compose status. Then depress the desired function key and note that the light under the CONV key goes out. This is a positive indicator to the operator that the terminal has set status waiting to be polled.

The ADM-2 should be connected to a non-echo modem such as the Bell 202S when operating in the polling environment.

The ADM-2 can be connected directly to the computer via an RS-232-C interface with lines of 50 feet or more, depending on data speed and environment.

The optional RS-232-C extension interface will allow several terminals to be connected together in a chain.

The optional DC1 box is available for use when the ADM-2 will be operated at greater distance from the modem or computer. The DC1 converts the RS-232-C to a two-wire direct connect operation and allows several terminals to operate in a party line fashion rather than chain.

The optional 20ma current loop interface can only be used point-to-point.

5.4.1 Polling Addressing Dialog

The network control center initiates an operation with a sequence of four or five characters. This sequence consists of the following:

a. EOT character.

b. Two address characters (same character transmitted twice). The ADM-2 address may be selected from any of 96 ASCII characters ("space" through DEL).

c. A function code character, which is one of the following:

P	(POL)
q	(Select)
r	(Sequential Select)
s	(Fast Select)
t	(Broadcast Select)
v, w, x, y, z, {	(Send)

Figures 5-2 through 5-7 show function code character's flow path.

d. Character ENQ, following function codes p, q, v, w, x, y, z, and { codes.

NOTE

IF A PARITY ERROR IS DETECTED IN A HEADER SEQUENCE, THE ADM-2 IGNORES THE ENTIRE HEADER.

When a terminal is addressed by the sequence EOT A_1A_1 p ENQ, it responds as follows:

a. If the ADM-2 has no message waiting to be sent, it sends an EOT character to the center.

b. If the ADM-2 does have a message to be sent, the terminal sends the message to the center.

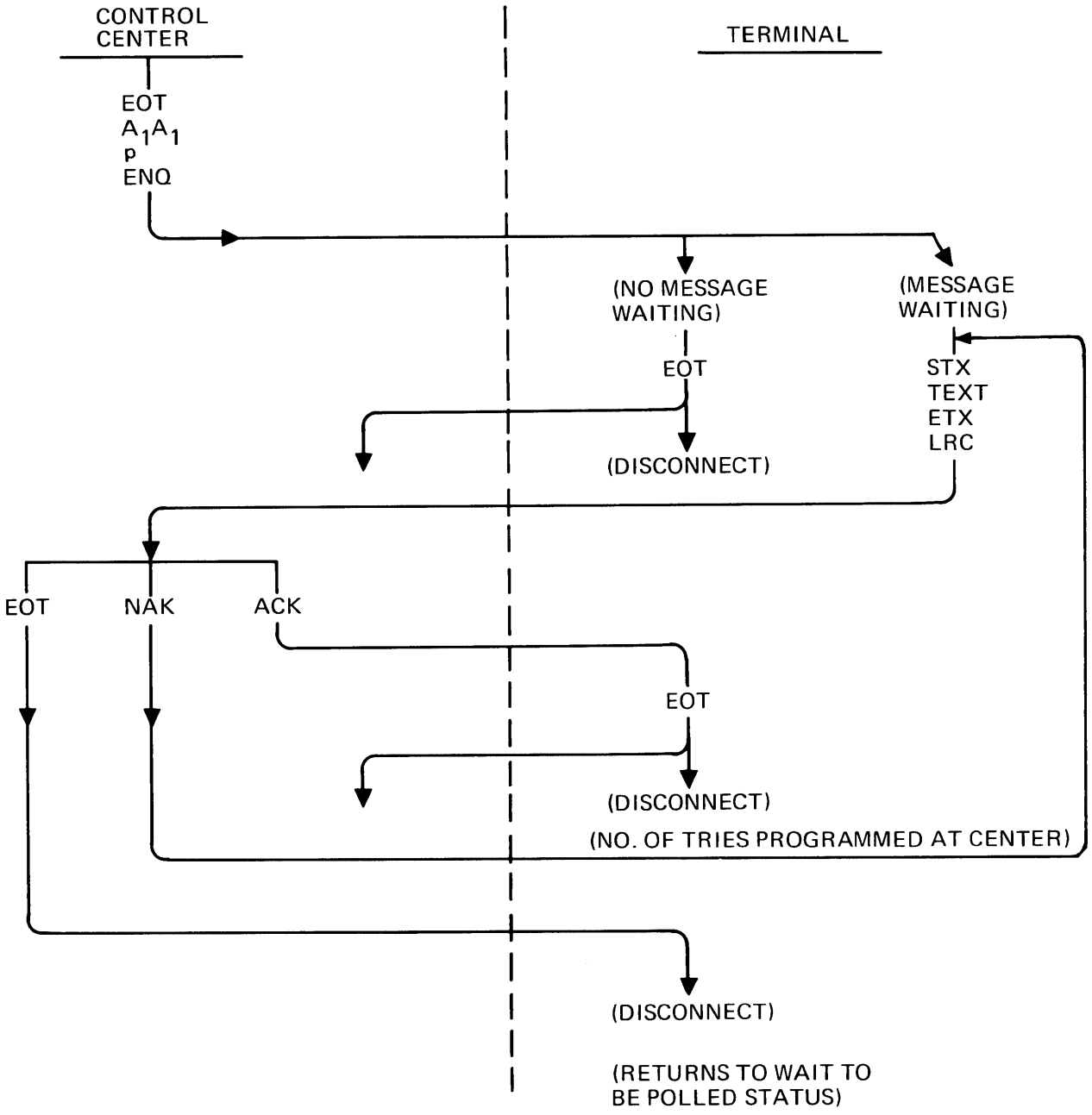


Figure 5-2. Poll Function Dialog, Flow Diagram

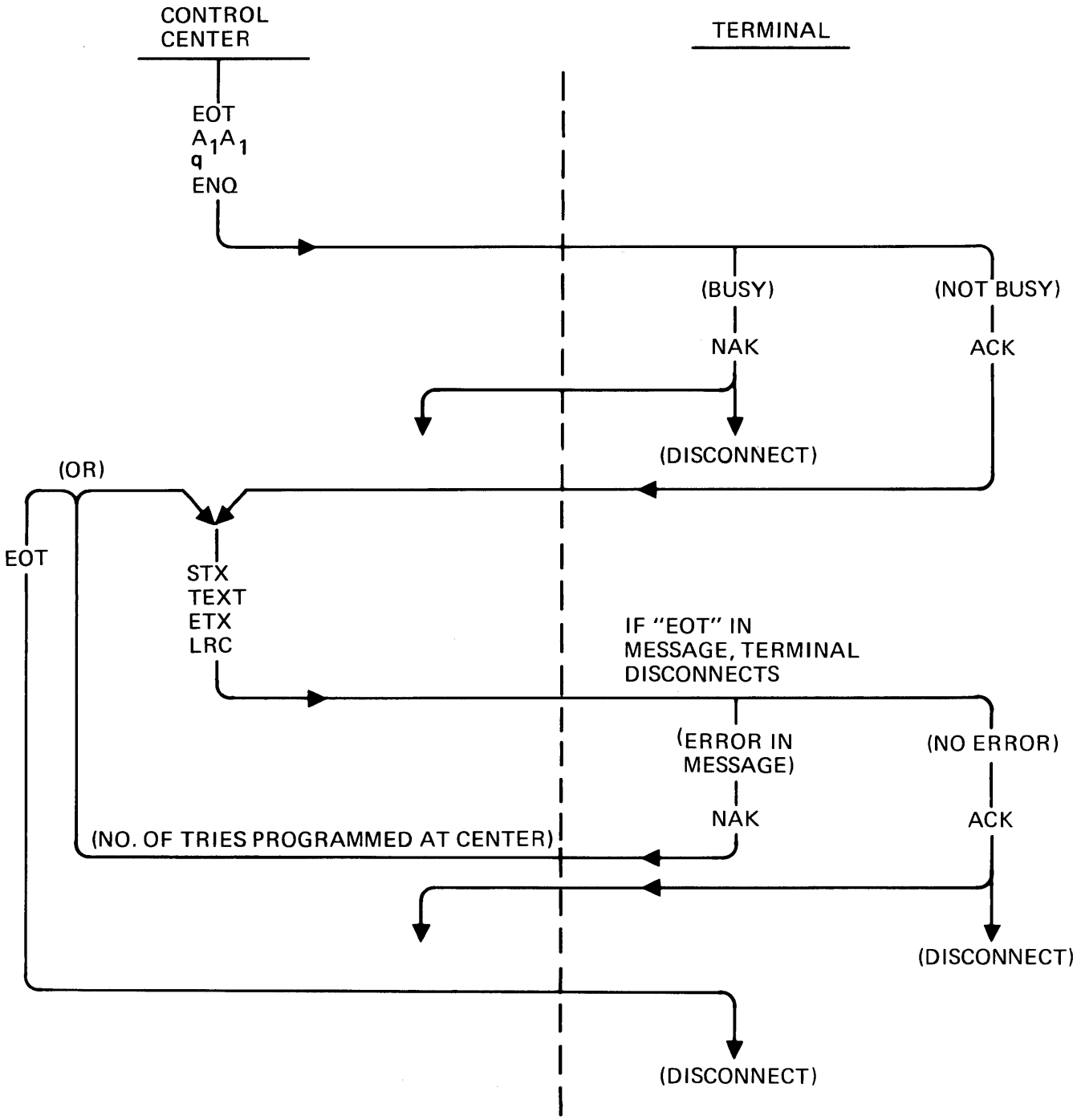


Figure 5-3. Select Function Dialog, Flow Diagram

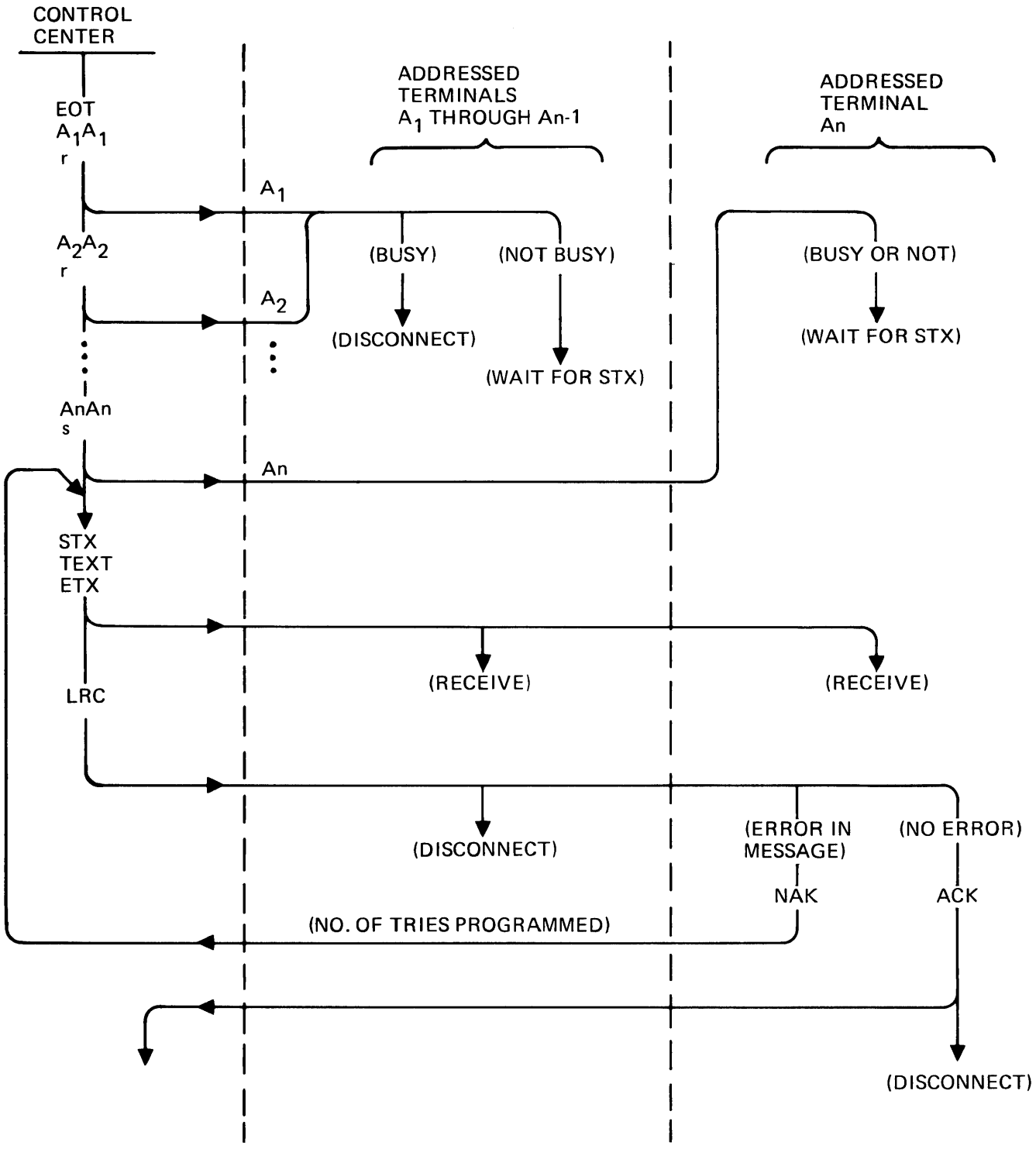


Figure 5-4. Sequential Select Function Dialog, Block Diagram

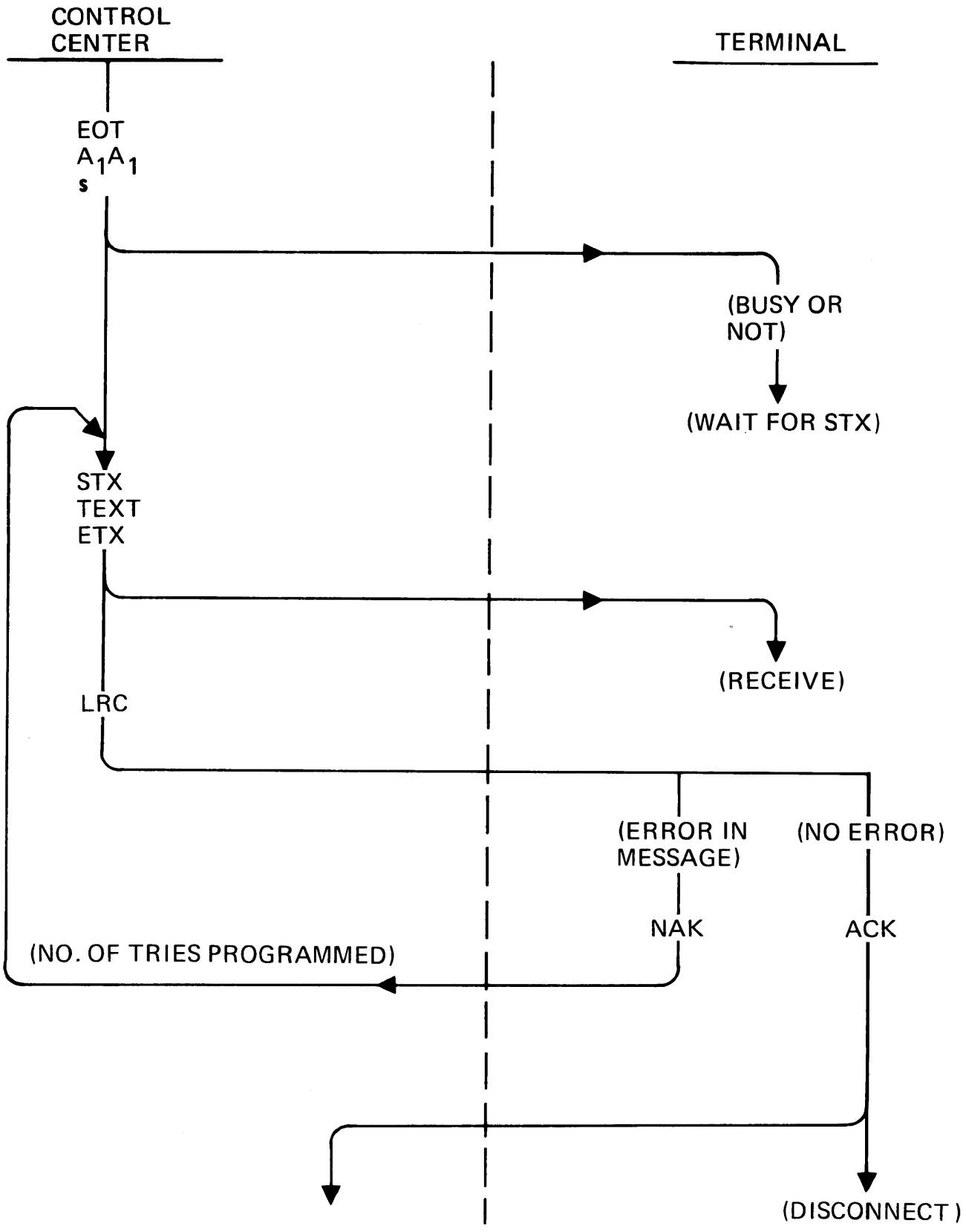


Figure 5-5. Fast Select Function Dialog, Block Diagram

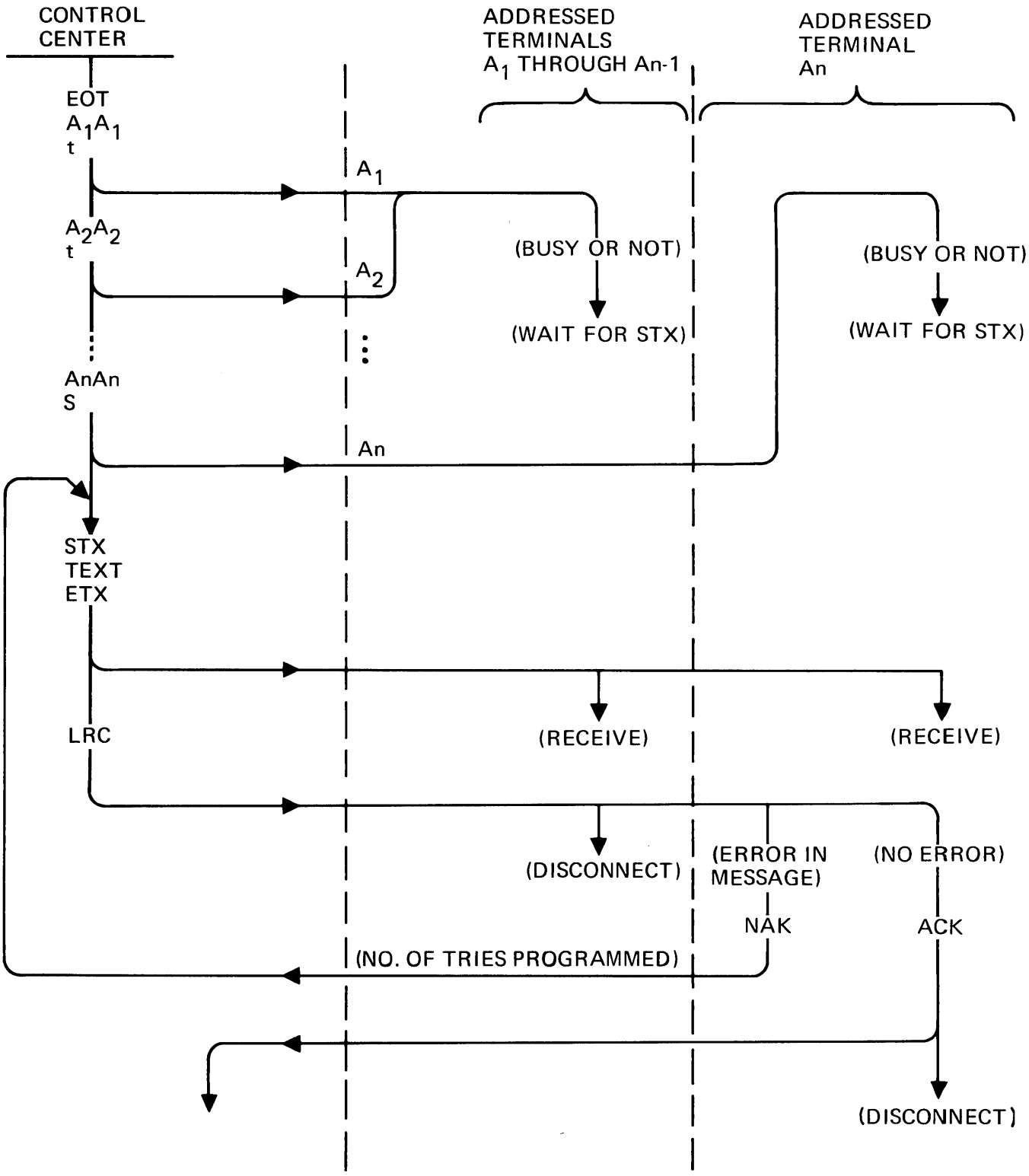


Figure 5-6. Broadcast Select Function Dialog, Block Diagram

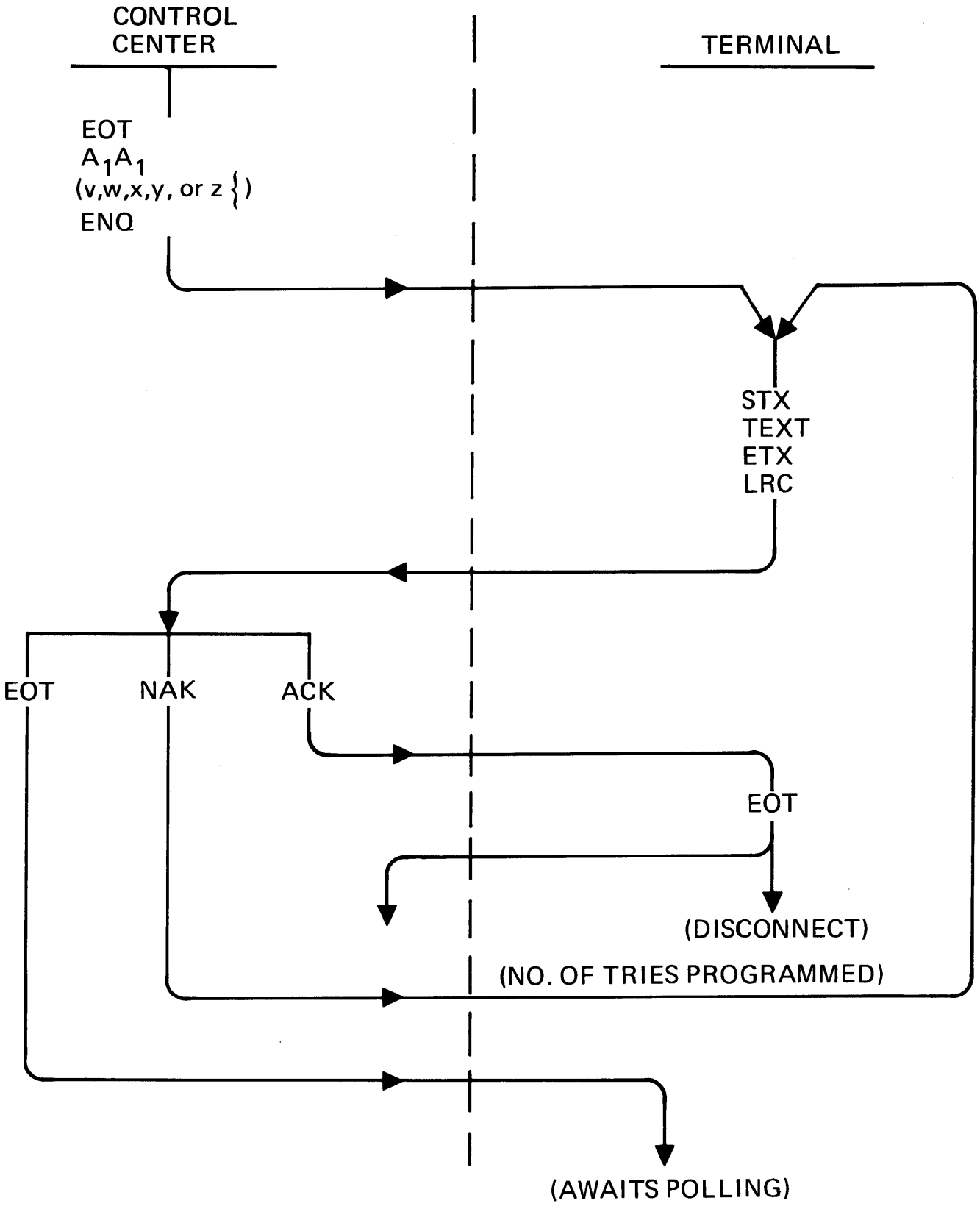


Figure 5-7. Send Function Dialog, Flow Diagram

SECTION SIX
LOGIC BOARD (MICROCONTROLLER) PROGRAMMING

All functions of the ADM-2 Interactive Terminal are controlled by the Main Logic Board. The Main Logic Board is controlled by a predetermined program stored in the ROM chip. This stored program, called the microprogram, initiates the necessary logic sequences to transfer data and control information between all functional units of the ADM-2. The information is exchanged between the functional units via an 8-bit parallel data path called a tristate bus (TSB). All TSB operations are done under microprogram control.

Table 6-1 is a listing of all ADM-2 functional units. These units transfer information via the tristate bus (TSB).

Table 6-1. ADM-2 Functional Units

UNIT MNEMONIC	UNIT	
RCV	From	External Serial Source via UART Receiver
KEY	From	Keyboard
CPR	From	Cursor position row register
CPC	From	Cursor position character register
LIT	From/To	Eight bit literal register
RDR	From	Random access page buffer via the Read Data Register
WDR	To	Random access page buffer via the Write Data Register
LRC	From/To	Modulo 2 adder and accumulator (7 bits)
ADD	From	Switch (8 bits) internal, manually set
MACR	From/To	Random access page buffer row counter (address register high order five bits)
INPUT		Utility Register *
OUTPUT		Utility Register *
CMD		Utility Register *
MAR	From/To	Margin Register
IND	From/To	Indicator Register
CNTR	From/To	Counter Register

* Unused in Standard ADM-2

Table 6-2 is a listing of the standard ADM-2 instruction set. The instructions listed are all single byte instructions (8 bits) with the exception of the Jump instructions, which require a second 8-byte operand.

Table 6-2. ADM-2 Instruction Set

001	READ	123	LOA ART0	251	JFC NULL
003	WRITE	124	CLR ART0	252	JFC LIT7
004	CLR WDR	130	SEL ART1	253	JFC LIT8
005	LOA WDR	131	SET RTS1	260	JFC STB1
006	SET WPROT	132	CLR RTS1	261	JFC STB2
007	CLR WPROT	133	LOA ART1	262	JFC STB3
016	SET PROTM	134	CLR ART1	263	JFC STB4
017	CLR PROTM	150	LOA LIT	264	JFC STB5
020	CLR MACC	156	CLR LRC	265	JFC STB6
021	LOA MACC	167	CLK LRC	266	JFC STB7
022	SET MACC	160	TSB=RDR	267	JFC STB8
023	INC MACC	161	TSB=KEY	300	JTC TSB1
024	DEC MACC	162	TSB=RCV	301	JTC TSB2
027	LOAD CPR	163	TSB=LIT	302	JTC TSB3
030	CLR MACR	164	TSB=CPC	303	JTC TSB4
031	LOA MACR	165	TSB=CPR	304	JTC TSB5
032	SET MACR	166	TSB=LRC	305	JTC TSB6
033	INC MACR	170	TSB=ADD	306	JTC TSB7
034	DEC MACR	172	TSB=INPUT	307	JTC TSB8
035	INH CUR	173	TSB=MAR	310	JTC KEYSTR
036	ENA CUR	174	TSB=IND	313	JTC CALL
037	SET BEEP	175	TSB=CNTR	314	JTC RTN
040	LOA OUTPUT	200	JFC TSB1	320	JTC OFLO
042	LOAD MAR	201	JFC TSB2	321	JTC MAC=CPR
044	LOA IND	202	JFC TSB3	322	JTC OPT1
045	CLR IND	203	JFC TSB4	330	JTC RDR
046	LOA CMD	204	JFC TSB5	331	JTC RPE
051	LOA CNTR	205	JFC TSB6	332	JTC RFE
052	INC CNTR	206	JFC TSB7	333	JTC ROE
053	DEC CNTR	207	JFC TSB8	334	JTC THRE
054	SET TIME	210	JFC KEYSTR	335	JTC CTS
055	SET BIN	213	JFC CALL	336	JTC TRE
056	CLR RTSEN	214	JFC RTN	337	JTC NRST/OPT2
057	SET RTSEN	220	JFC OFLO	340	JTC PROTM
060	CLR STB1	221	JFC MAC=CPR	341	JTC PROT
061	SET STB1	222	JFC OPT1	342	JTC INTIN
062	CLR STB2	230	JFC RDR	343	JTC FULL
063	SET STB2	231	JFC RPE	343	JTC KEYST2
064	CLR STB3	232	JFC RFE	344	JTC OPNC
065	SET STB3	233	JFC ROE	344	JTC RESET
066	CLR STB4	234	JFC THRE	345	JTC CONV
067	SET STB4	235	JFC CTS	346	JTC FDX
070	CLR STB5	236	JFC TRE	350	JTC MACC
071	SET STB5	237	JFC NRST/OPT2	360	JTC NULL
072	CLR STB6	240	JFC PROTM	352	JTC LIT7
073	SET STB6	241	JFC PROT	353	JTC LIT8
074	CLR STB7	242	JFC INTIN	360	JTC STB1
075	SET STB7	243	JFC FULL	361	JTC STB2
076	CLR STB8	243	JFC KEYST2	362	JTC STB3
077	SET STB8	244	JFC OPNC	363	JTC STB4
100	JMP	244	JFC RESET	364	JTC STB5
120	SET ART0	245	JFC CONV	365	JTC STB6
121	SET RTS0	246	JFC FDX	366	JTC STB7
122	CLR RTS0	250	JFC MACC	367	JTC STB8

Table 6-3 lists the tristate bus control instructions. Some of these instructions are repeated in other tables, as the instructions belong to more than one control grouping.

Table 6-3. Tristate Bus Control

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	DESCRIPTION
TSB=RDR	160	Set the TSB contents equal to RDR
TSB=KEY	161	Set the TSB contents equal to KEY
TSB=RCV	162	Set the TSB contents equal to RCV
TSB=LIT	163	Set the TSB contents equal to LIT
TSB=CPC	164	Set the TSB contents equal to CPC
TSB=CPR	165	Set the TSB contents equal to CPR
TSB=LRC	166	Set the TSB contents equal to LRC
TSB=ADD	170	Set the TSB contents equal to ADD
TSB=INPUT	172	Set the TSB contents equal to INPUT
TSB=MAR	173	Set the TSB contents equal to MAR
TSB=IND	174	Set the TSB contents equal to IND
TSB=CNTR	175	Set the TSB contents equal to CNTR

Display control and utility register control instructions are listed in Tables 6-4 and 6-5 respectively.

Table 6-4. Display Control

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	DESCRIPTION
INH CUR	035	Inhibits display of cursor
ENA CUR	036	Enables display of cursor
LOA IND	044	A one (1) on TSB complements corresponding IND bit.
CLR IND	045	Clears IND

Table 6-5. Utility Register Control

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	DESCRIPTION
TSB=MAR	173	Sets TSB contents equal to that of the MAR
LOA MAR	042	Sets MAR contents equal to that of TSB
TSB=CNTR	175	Sets TSB contents equal to that of the CNTR
LOA=CNTR	051	Sets CNTR contents equal to that of the TSB
INC CNTR	052	Increments contents of CNTR
DEC CNTR	053	Decrements contents of CNTR

RAM address instructions are listed in Table 6-6.

Table 6-6. RAM Address Control

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	DESCRIPTION
CLR MACC	020	Set character counter to left margin
CLR MACR	030	Set row counter to top row
LOA MACC	021	Set character counter to value on tristate bus
LOA MACR	031	Set row counter to value on tristate bus
LOA CPR	027	Sets contents of CPC and CPR equal to current contents of MACC and MACR, respectively
SET MACC	022	Set character counter to right margin
SET MACR	032	Set row counter to bottom row
INC MACC	023	* Move character counter right one position
INC MACR	033	* Move row counter down one line
DEC MACC	024	* Move character counter left one position
DEC MACR	034	* Move row counter up one line
SET BIN	055	This instruction, if followed immediately by LOA MACC or LOA MACR, will load the binary value of the (TSB) rather than the interpreted character value normally loaded.

* These operations will set OFLO if they cause character address to run off either margin or if they cause row address to run off top or bottom of page.

RAM memory control instructions are listed in Table 6-7.

Table 6-7. Random Access Memory Control

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	DESCRIPTION
READ	001	Transfers the contents of the RAM location indicated by the contents of MACR, MACC into the RDR
WRITE	003	Transfers the contents of the WDR into the RAM location indicated by the contents of MACR, MACC
LOA WDR	005	Replaces the contents of the WDR with the contents currently on the TSB
CLR WDR	004	Clears the WDR
TSB=RDR	160	Sets the contents on the TSB equal to the contents of the RDR
SET WPROT	006	Sets the write protect bit on all words subsequently written into the RAM
CLR WPROT	007	Clears the write protect bit on all words subsequently written into the RAM
SET PROTM	016	Set the PROTM. This status bit is used as a global condition by the program to disable the overwriting of any characters in the RAM for which the WPROT bit is set.
CLR PROTM	017	Clear the PROTM. This global condition enables the overwriting of write protected characters.

Flags are set or cleared by the microprogram to control specific hardware functions or to set global conditions controlling the microprogram actions. General flag instructions are:

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	ACTION
CLR	CAA	Clears the indicated flag. (See table flags for values of CAA.)
SET	CAA	Sets the indicated flag. (See table flags for value of CAA.)

Table 6-8 lists the specific flag instructions of the ADM-2.

Table 6-8. Table of Flags

MNEMONIC	SET	CLEAR	DESCRIPTION
WPROT	006	007	Write Protect
PROTM	016	017	Protect Mode
STB1	061	060	Program Global
STB2	063	062	Program Global
STB3	065	064	Program Global
STB4	067	066	Program Global
STB5	071	070	Program Global
STB6	073	072	Program Global
STB7	075	074	Program Global
STB8	077	076	Program Global
BEEP	037	(Clears automatically)	Causes one BEEP
RTS0	121	122	Communication Channel Request to Send
RTS1	131	132	Auxiliary Channel Request to Send
BIN	055	(Automatic after 1 cycle)	Modifies LOA & LOA MACR instructions

In addition to the main transmitter/receiver interface normally associated with the computer, an additional transmitter/receiver interface is accommodated by the instructions listed in Table 6-9.

Table 6-9. Auxiliary Asynchronous Receiver/Transmitter Control

MNEMONIC	$(D_{1,2}\ D_{1,0})$	DESCRIPTION
SEL ART0	120	Selects main receiver transmitter interface
SEL ART1	130	Selects auxiliary receiver transmitter interface
LOA ART0	123	Loads main transmitter from TSB
LOA ART1	133	Loads auxiliary transmitter from TSB
CLR ART0	124	Clear main data ready flag
CLR ART1	134	Clear auxiliary data ready flag

Table 6-10 lists the ROM control instructions.

Table 6-10. ROM Instruction Execution Sequence Control

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	DESCRIPTION
JMP	10P LLL	Causes next instructions to be taken from the location indicated by LLL on page P
JTC	3CC LLL	Causes next instructions to be taken from the location indicated by LLL on the local page if the condition indicated by CC is true. Instructions are taken in normal sequence otherwise. (See table of conditions for values of CC.) (See note below for CALL and RTN.)
JFC	2CC LLL	Causes next instructions to be taken from the location indicated by LLL on the local page if the condition indicated by CC is false. Instructions are taken in normal sequence otherwise. (See table of conditions for values of CC.) (See note below for CALL and RTN.)
(NOTE: Transfer of control to subroutines on the same page are facilitated by the CALL and RTN conditions as follows:)		
JFC CALL	213	Causes contents of the program counter to be transferred to CNTR prior to transfer of control
JFC RTN	214	Causes contents of CNTR to replace contents of program counter. LLL is ignored. CNTR must be incremented prior to this operation.

Table 6-11 is a list of miscellaneous control instructions in the ADM-2 instruction set.

Table 6-11. Miscellaneous Control Instructions

TRANSMISSION LONGITUDINAL CHECKING

A 7-bit modulo two added LRC is provided for transmission checking.

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	DESCRIPTION
CLR LRC	156	Clear LRC
CLK LRC	157	Replace each bit of the LRC with the modulo two sum of its prior setting and the corresponding bit of the TSB.

LITERAL CONTROL

The literal register provides a means of entering a constant from the ROM onto the tristate bus.

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	($D_{2,2}$ $D_{2,0}$)	DESCRIPTION
LOA LIT	150	XXX	The instruction causes the contents of LIT to be replaced by XXX.

NOTE: CONTENT OF LIT IS CHANGED BY JMP INSTRUCTION.

A number of instructions in the instruction set are employed to either set or record certain ADM-2 terminal conditions. Table 6-12 lists these condition instructions.

Table 6-12. Condition Instructions

MNEMONIC	CONDITION IDENTIFIER	DESCRIPTION
TSB1	00	Tristate Bus Bit 1
TSB2	01	Tristate Bus Bit 2
TSB3	02	Tristate Bus Bit 3
TSB4	03	Tristate Bus Bit 4
TSB5	04	Tristate Bus Bit 5
TSB6	05	Tristate Bus Bit 6
TSB7	06	Tristate Bus Bit 7
TSB8	07	Tristate Bus Bit 8
* STB1	60	Status Bit 1
* STB2	61	Status Bit 2
* STB3	62	Status Bit 3
* STB4	63	Status Bit 4
* STB5	64	Status Bit 5
* STB6	65	Status Bit 6
* STB7	66	Status Bit 7
* STB8	67	Status Bit 8
KEYSTER	10	Keyboard strobe
OFLO	20	MACC/MACR overflow or underflow
MAC=CPR	21	Set if MACR equals CPR
OPT1	22	Wire straps on main logic board
PROTM	40	Set if in character protection mode (write protect mode)
PROT	41	Character protect bit in RAM and protect mode

Table 6-12. Condition Instructions (Continued)

MNEMONIC	CONDITION IDENTIFIER	DESCRIPTION
CONV	45	Conversation mode
CALL	13	Subprogram call–contents of program counter transferred to CNTR when true
RTN	14	Subprogram return–transfers CNTR contents to program counter when true
RDR	30	Receiver data ready–character assembled
RPE	31	Received parity error–receiver detected parity error
RFE	32	RCVR framing error
ROE	33	RCVR overflow
THRE	34	Transmitter holding register–ready for next character
CTS	35	Clear to send (asynchronous transmission)–remote device ready for transmission
TRE	36	Transmitter register empty indicator
$\overline{\text{RESET}}$/OPT2	37	Reset by OPT2 (Strap)
INTIN	42	Extended memory option
KEYST2	47	Second key strobe true when depressed key is a control function
RESET	44	Reset key (also used with extended memory)
FDX	46	Full duplex, conversational mode
MACC	50	(TSB) equals (MACC)
NULL	51	(TSB) equals (NULL)
LIT7	52	(TSB) equals (LIT) seven bits only (1 through 7)
LIT8	53	(TSB) equals (LIT) eight bits

* All status bits are set by the microprogram for global control.

Figure 6-1 is a sample program using many of the ADM-2 instruction mnemonics previously described in this section.

PAGE	ROM ADDRESS OCTAL	ROM WORD OCTAL		ENTRY POINT LABLE	INSTRUCTION	
0	0	124	260	RESET	CLR ARTO	
0	1	17	270	○	CLR PROTM	
0	2	100	280	○	JMP	RESET10
0	3	104				
0	4	100	310	IDLE35X	JMP	IDLE35
0	5	32				
0	6	37	320	BELL	SET BEEP	
0	7	261	330	IDLE	JFC STB2	IDLE10
0	10	12				
0	11	124	340	○	CLR ARTO	
0	12	62	350	IDLE10	CLR STB2	
0	13	120	360	○	SEL ARTO	
0	14	36	370	○	ENA CUR	
0	15	234	380	○	JFC THRE	IDLE20
0	16	22				
0	17	236	390	○	JFC TRE	IDLE20
0	20	22				
0	21	122	400	○	CLR RTSO	
0	22	222	410	IDLE20	JFC OPT1	IDLE30
0	23	26				
0	24	105	420	○	JMP	POLIDLE
0	25	0				
0	26	365	440	IDLE30	JTC STB6	PRINTINGO
0	27	114				
0	30	330	450	○	JTC RDR	RECEIVE
0	31	165				
0	32	310	460	IDLE35	JTC KEYSTR	IDLE40
0	33	50				
0	34	337	470	○	JTC NRST	IDLE
0	35	7				
0	36	60	480	KRESET	CLR STB1	
0	37	174	490	○	TSB = IND	
0	40	206	500	○	JFC TSB7	KRESET10
0	41	46				

Figure 6-1. ADM-2 Microcontroller Program Example

PAGE	ROM ADDRESS OCTAL	ROM WORD OCTAL		ENTRY POINT LABEL	INSTRUCTION	
0	51	51	560	o	LOA CNTR	
0	52	35	570	o	DIS CUR	
0	53	207	580	o	JFC TSB8	IDLE50
0	54	57				
0	55	101	590	o	JMP	FKEY
0	56	161				
0	57	174	600	IDLE50	TSB=IND	
0	60	300	610	o	JTC TSB1	IDLE
0	61	7				
0	62	347	620	o	JTC KEYST2	ESCL02
0	63	206				
0	64	260	630	o	JFC STB1	IDLE60
0	65	71				
0	66	161	640	o	TSB=KEY	
0	67	101	650	o	JMP	ESCHAR
0	70	132				
0	71	150	660	IDLE60	LOA LIT	33
0	72	33				
0	73	175	670	o	TSB=CNTR	
0	74	352	680	o	JTC LIT7	IDLE70
0	75	100				
0	76	101	690	o	JMP	DATACHAR
0	77	0				
0	100	61	700	IDLE70	SET STB1	
0	101	5	710	o	LOA WDR	
0	102	100	720	o	JMP	IDLE
0	103					
0	104	15	730	RESET10	SET BLOCK	
0	105	320	740	o	JTC OFLO	RESET20
0	106	107				
0	107	156	750	RESET20	CLR LRC	
0	110	166	760	o	TSB=LRC	
0	111	42	770	o	LOA MAR	
0	112	100	780	o	JMP	CLEAR08
0	113	255				
0	114	337	790	PRINTING0	JTC NRST	PRINTING1
0	115	122				
0	116	66	800	o	CLR STB4	
0	117	71	810	o	SET STB5	
0	120	100	820	o	JMP	KRESET
0	121	36				

Figure 6-1. ADM-2 Microcontroller Program Example (Continued)

SECTION SEVEN
MAINTENANCE

7.1 PREVENTIVE MAINTENANCE (PM)

The ADM-2 is designed to operate with a minimum of scheduled maintenance (i.e., P.M.). A light cleaning from time to time is the only routine maintenance required. The cleaning procedure requires only a couple of minutes of operator time and insures hours of continued trouble-free operation of the unit.

Dust the unit using a brush or soft, damp, lint-free cloth. Any conventional spray cleaners may be used to remove stubborn smudges and fingerprints. DO NOT USE PETROLEUM BASED CLEANERS, AS THESE MIGHT HARM THE PLASTIC OR PAINTED SURFACE. Avoid wiping dust or lint into the keyboard area. When using a spray cleaner, prevent excessive spraying which could run down between the keys.

7.2 ADJUSTMENTS

Each adjustment and its procedure is listed in one of the following paragraphs. (Refer to monitor schematic (1-024-0508) and monitor board assembly (P. 7-19) drawings when performing these adjustments.)

7.2.1 Synchronization and Drive Signals

Apply horizontal and vertical drive signals to the horizontal and vertical drive terminals as indicated in the schematic.

The horizontal drive signal is required to initiate horizontal scan and high voltage, and should be connected before applying power to the monitor.

7.2.2 Low Voltage Supply

Set the DC voltage by variable resistor R208. This voltage can be monitored at the junction of R114 and R130.

7.2.3 Brightness

Usual video polarity produces white characters on a black background.

The brightness control (on the rear of the terminal) should be adjusted to a point where the white raster is just extinguished. The CRT will then be at its cutoff point. A maximum contrast ratio can be obtained when a video signal is applied.

7.2.4 Video Contrast

Q101 on the monitor board is designed to operate linearly when a +2.5V signal is applied to its base. The monitor incorporates in its circuitry a 500 ohm external contrast control to maintain this level. This control should be adjusted for a typical signal level of +2.5V peak-to-peak when measured at the video input terminal of the printed circuit board cable connector.

7.2.5 Vertical Adjustments

There is a slight interaction among the vertical frequency, height, and linearity controls. A change in the height of the picture may affect linearity.

a. Apply video and synchronization signals to the monitor.

b. Set the vertical frequency control (R116) near the mechanical center of its rotation.

c. Adjust the vertical height control (R124) for desired height.

d. Adjust the vertical linearity control (R121) for best vertical linearity.

e. Remove the vertical drive signal from the unit; or, alternately, use a short jumper lead to short the vertical drive input terminal of the printed circuit card edge connector to ground.

f. Readjust the vertical frequency control (R116) until the picture rolls up slowly.

g. Restore vertical drive to the monitor.

h. Recheck height and linearity.

7.2.6 Horizontal Adjustments

Raster width is affected by a combination of the low voltage supply, width coil L101, and the horizontal linearity sleeve (located on the neck of the CRT beneath the yoke).

a. Apply video and synchronization signals to the monitor. Insert the horizontal linearity sleeve about 2/3 of its length under the yoke. (If you received a monitor from the factory in which the placement of the linearity sleeve has been determined, make a mark on the sleeve and reinsert the sleeve to this mark when removal of the yoke and linearity sleeve are required.) If the linearity sleeve is inserted farther than necessary, excessive power will be consumed, and the horizontal output circuitry could be overstressed.

b. Adjust the horizontal width coil, L101, for the desired width.

c. Insert the linearity sleeve farther under the yoke to obtain the best linearity. Although this adjustment will affect the raster width, it should not be used solely for that purpose. The placement of the linearity sleeve should be optimized for the best linearity.

d. Readjust L101 for proper width.

e. Observe final horizontal linearity and width. Adjust as necessary.

No horizontal hold control is used in this monitor. The raster should be properly locked and centered when the horizontal drive signals as described above are used.

7.2.7 Focus Adjustment

The focus control (R107) provides an adjustment for maintaining best overall display focus. However, because of the construction of the gun assembly in the CRT, this control does not have a great effect on focus.

7.2.8 Centering

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke.

The ring magnets should not be used to offset the raster from its nominal center position because it would degrade the resolution of the display.

If the picture is tilted, rotate the entire yoke.

7.2.9 Power Supply Adjustment

The separate +5V power supply is not normally adjusted unless corrective maintenance is performed. The adjustments for the +5V power supply are in Section 7.5.

7.3 CORRECTIVE MAINTENANCE

Maintenance will normally be done on the logic board or sub-assembly level only. This procedure reduces down time and requires less time for repairs. The faulty PCBA or sub-assembly will be returned to the branch office or factory for repairs.

The technician should check the following when responding to a maintenance request before referring to the troubleshooting section of this manual.

a. Operator error. Check that the operator is performing a valid operation and is following a correct procedure. If possible, contact the operator who filed the complaint and have him define the trouble.

b. Machine error. Check for obvious problems, i.e., power fluctuations, bad communication lines, trouble at the main computer site.

c. Check the program being run. Are the instructions correct for the required operation? Are all switch settings correct? (Especially check the position of the mode switch, EAI switch, and baud rate switch.)

If none of the foregoing remedy the problem, refer to the troubleshooting section of this manual (Section 7.5) to help isolate the malfunction to a specific sub-assembly.

7.4 REMOVAL AND REPLACEMENT

This section describes the correct procedure to follow in order to disassemble the ADM-2 for removal and replacement of components. (The removal procedure for all sub-units is given below. Review the procedure for replacement of the sub-unit.)

CAUTION

BEFORE PROCEEDING WITH THE DISASSEMBLY OF THE ADM-2, ENSURE THAT THE ADM-2 IS UNPLUGGED FROM THE AC WALL OUTLET.

7.4.1 Keyboard

a. The keyboard unit plugs into the rear of the terminal. Loosen the two screws holding the keyboard plug to the connector and remove the plug.

b. Remove the four corner screws on the bottom of the keyboard assembly that hold on the cover.

c. Lift the cover off of the keyboard assembly.

d. Remove the seven screws that hold the keyboard to its base.

e. The keyboard is now able to be replaced. Do not forget the cable strain release when replacing the keyboard.

7.4.2 Display Unit Cover

a. The cover is fastened by five screws: two on each side of the unit and one in the rear of the unit. Remove all five screws and lift cover off gently.

7.4.3 Upper Chassis

a. The upper chassis is connected to the base by seven screws: two in front, one on each side, and three in the rear of the unit. Remove all seven screws.

b. Remove plugs J4 and J5 (located in the left rear of the unit).

c. The entire upper chassis can be removed from the base.

7.4.4 ADM-2 Logic Board

a. Remove the rear guide by extracting the three screws holding it to the base.

b. Remove the four plastic nuts and posts holding the board.

c. If present, the microprogram piggyback card must be removed.

d. Unlock and remove the three locking posts that hold the logic board.

e. The logic board may now be removed from its position.

7.4.5 Monitor Logic Board

a. Remove the seven connectors shown in Figure 7-8.

b. Remove the three grounds shown in Figure 7-8.

c. Record the color code of the wires as they are removed for ease in replacement.

d. Remove the edge connector from the board, and the connector from the back of the video tube.

e. The monitor board can now be removed from the four locking posts.

f. Lift the board out of the unit.

NOTE

WHEN INSTALLING A NEW BOARD, ALL ADJUSTMENTS MUST BE MADE.

7.4.6 Monitor Assembly

a. Remove the upper chassis (refer to Section 7.4.3).

b. Turn the upper chassis over and remove the three holding screws from the bottom.

c. Remove the edge connector from the PC board.

d. Remove the two wires from the AC terminal block.

e. Cut all ties to diagonal support bars (if any).

f. The monitor assembly should be free of upper chassis.

7.4.7 Power Supply

a. Remove the three input wires from the supply and note the color code for replacement.

b. Remove the four holding screws from the bottom of the chassis.

c. The power supply can now be removed.

7.4.8 Component Replacement

The replacement of a component on any printed circuit board requires care to prevent damage to circuit board etch. Clipping a component from the circuit board rather than unsoldering is the preferred method. Excessive heat from a soldering iron may result in damage to the component being replaced. The use of a soldering iron with a small copper alligator clip as a heat sink, and a time delay between the soldering of individual pins of a chip, are recommended.

In accordance with good maintenance practices, Lear Siegler does not recommend individual component replacement on any printed circuit board. Instead, the factory should be contacted relative to availability of special test equipment or factory rebuilt and tested replacement assemblies.

7.5 TROUBLESHOOTING THE ADM-2

The following is a suggested general outline for troubleshooting the ADM-2 Interactive Display Terminal or any similar terminal. The exact technique used will vary with the technician, but the method of using a set sequence of steps for quick fault isolation should remain unchanged.

a. Check the obvious first, i.e., unplugged from outlet, loose plugs and/or connectors, data set error, fuses blown, computer error, operator error, etc.

b. Record the state of the machine when the error occurred. Note operation being performed.

c. Substitution of the sub-assemblies is the quickest method of isolating the faulty area (when replacement components are available). Substitute the following:

- Main circuit board
- Keyboard
- Monitor board
- Monitor assembly
- Power supply
- Interconnecting cables.

d. By using an oscilloscope and/or multimeter, the faulty component may be determined, if replacement parts are not available.

e. After the problem has been diagnosed and the unit is replaced or repaired, test the ADM-2 by running the same operation as when the error or problem first occurred.

f. Record the symptoms, cause, and module, sub-assembly, or component that was replaced or repaired. This can be used for future reference.

7.5.1 Fault Isolation

The ADM-2 is divided into four main parts: logic board, keyboard, power supply, and monitor. Each of these parts performs a function in the ADM-2. By analyzing the failure carefully, the probable cause can be determined. Table 7-1 is an ADM-2 Failure Analysis Guide designed to give the reader a probable starting point from which to begin troubleshooting.

Table 7-1. ADM-2 Failure Analysis Guide

TYPE OF FAILURE	PROBABLE LOCATION OF FAILURE			
	Logic Board	Keyboard	Power Supply	Monitor
Audio Signal	1	2		
Clear Memory	1	2		
Clear Memory (Power Up)	1			
Cursor Control	1	2		
EDIT Control Option	1	2		
Parity Error	1			
Receive Data*	1			
Transmit Data*	1	2		
Character/No Cursor	1			
No Character/Cursor	1			
No Character/No Cursor	3		2	1
Data/No Sync	2			1
Data Wavy			1	2
Randomly Generated, Wrong Characters**	1	2		

* Check word structure specification and baud rate.
** Insure good connection of cable from keyboard to logic board.

The following flow charts (Figures 7-1 to 7-4) illustrate the procedure to follow when troubleshooting a specific malfunction.

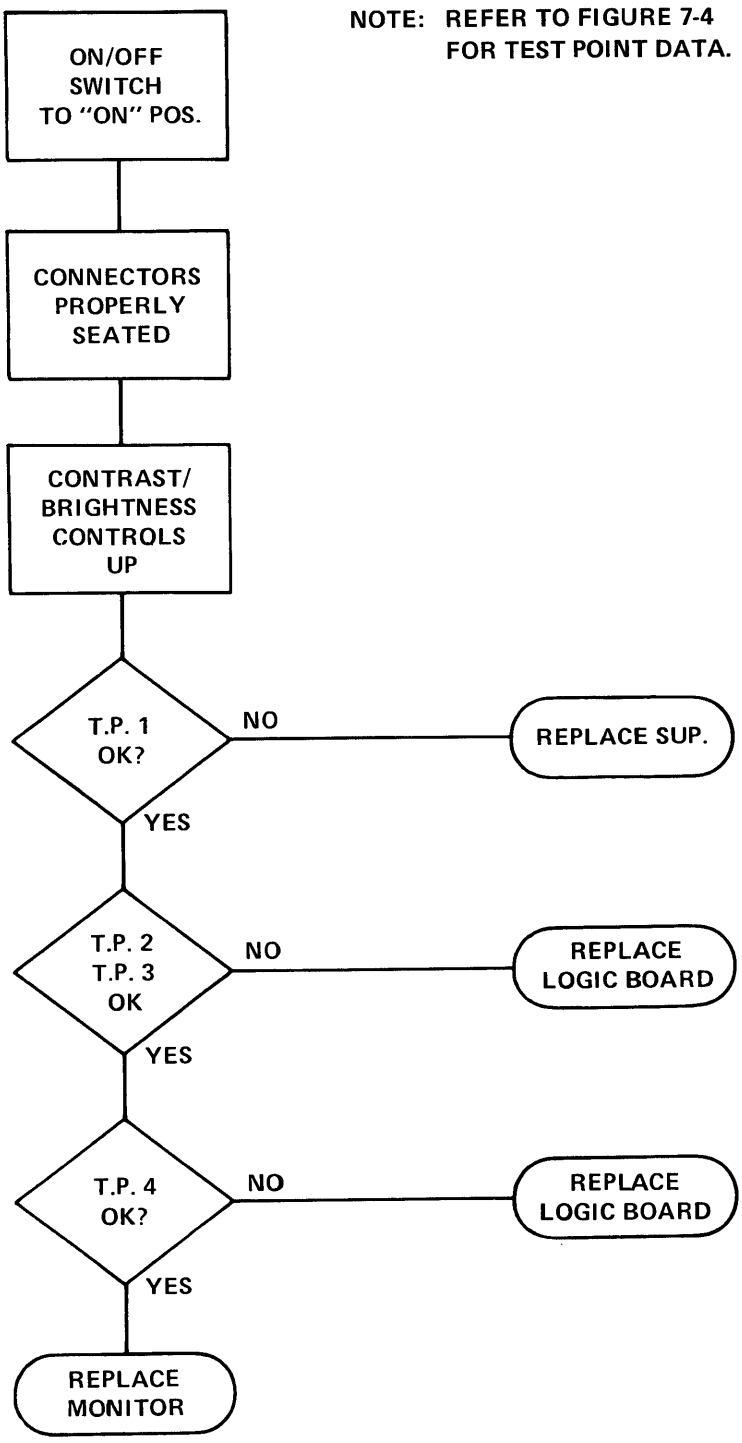


Figure 7-1. No Video Display/Erratic Video Flow Chart

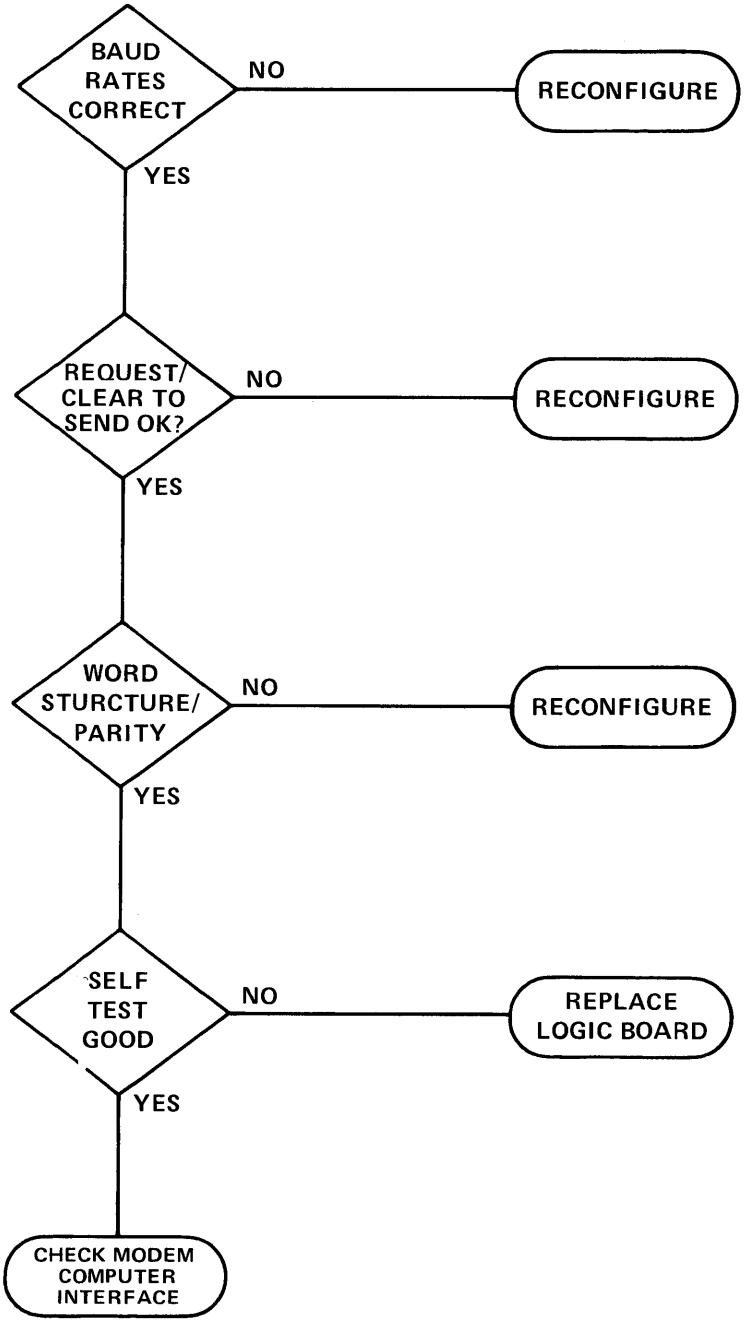


Figure 7-2. I/O Problems Flow Chart

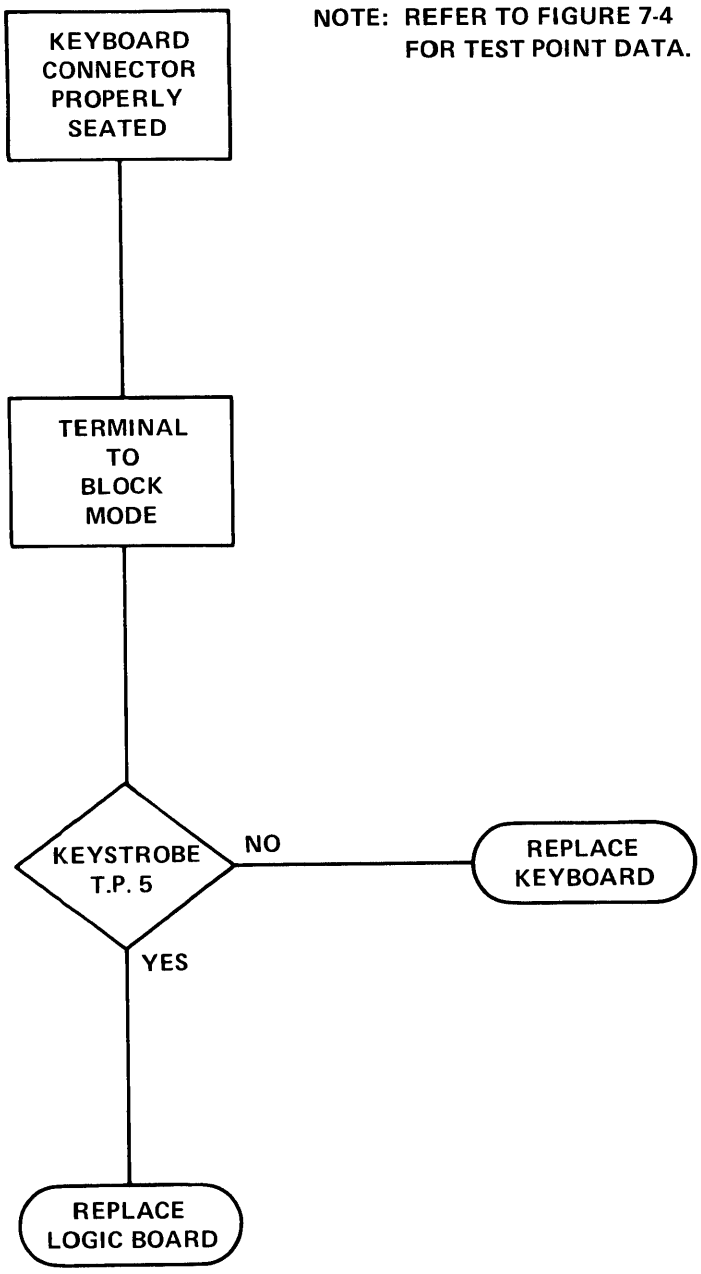
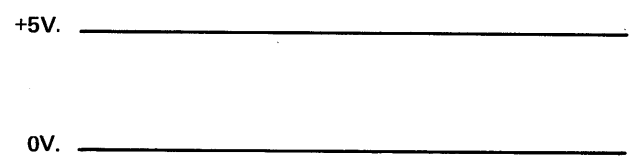
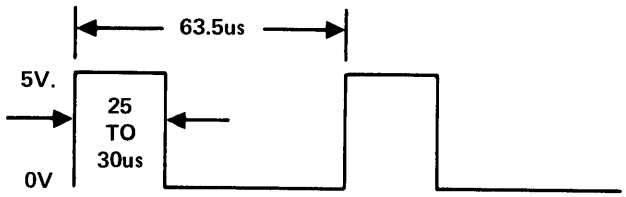


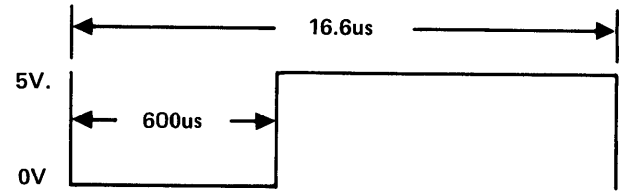
Figure 7-3. No Characters on Screen Flow Chart



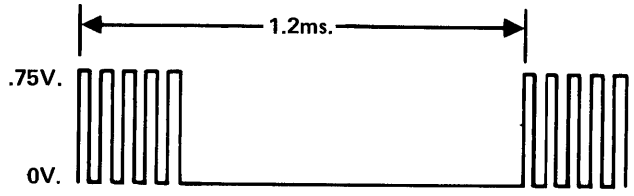
TEST POINT 1. 5.4 V.D.C ±5MV RIPPLE
(ON POWER SUPPLY)



TEST POINT 2. HORIZONTAL DRIVE
(CONNECTOR J-4 PIN 8)



TEST POINT 3. VERTICAL DRIVE
(CONNECTOR J-4 PIN 9)



TEST POINT 4. VIDEO SIGNAL – SIGNAL WILL VARY W/DATA
(CONNECTOR J-4 PIN 4)

TEST POINT 5. KEYSTROBE – SIGNAL
SIGNAL IS TRUE WHILE KEY DEPRESSED
(CONNECTOR J-6 PIN 6)

Figure 7-4. Test Point Data

Figure 7-5 indicates the number of null codes required for each transmission speed.

TRANSMISSION SPEED	NUMBER OF NULL CODES							
	110	300	600	1200	1800	2400	4800	9600
CLEAR SCREEN	0	0	0	3	4	5	9	16
CHARS INS	0	0	0	0	0	0	0	0
CHAR DEL	0	0	0	0	0	0	0	0
LINE INS	0	0	0	3	4	5	9	17
LINE DEL	0	0	0	3	5	7	13	23
ERASE LINE	0	0	0	0	0	0	0	0
ERASE PAGE	0	0	0	3	5	6	10	17
SKIP	0	0	0	3	5	6	10	17
PAGE ROLL	0	0	0	3	5	6	10	17

Figure 7-5. Null Codes Required Versus Transmission Speeds

7.5.2 Fault Location Determination

By proper use of the oscilloscope and multimeter, it is relatively simple to isolate a problem to the component with a section determined to be failing. The logic diagrams and assembly drawings required are in Appendices A and B of this manual.

Monitor Troubleshooting Hints

The high voltage for the monitor is generated from its own self-contained power supply. Additionally, the monitor assembly includes its own low voltage (15V DC) power supply.

CAUTION

DISCHARGE HIGH VOLTAGE BEFORE ATTEMPTING TO REMOVE OR REPLACE THE MONITOR ASSEMBLY.

Table 7-2 is a guide to common monitor problems.

Figure 7-6 shows important monitor waveforms. Figure 7-7 shows the monitor input signal format. Figure 7-8 shows monitor circuit board component location.

Table 7-2. Monitor Troubleshooting Guide

PROBLEM	PROCEDURE
Screen is dark.	Check "A" bus Q106, Q105, CR2.
Loss of video.	CR105, Q101.
Power consumption is too high.	Check horizontal drive waveform; check proper placement of horizontal linearity sleeve; Q105, Q106.
Low voltage bus incorrect (for units with a low voltage supply).	Q202, Q203, Q1 (Note: Low voltage supply will indicate low or "0" volts due to its current limiting action if a short is evident in the "A" volt line.

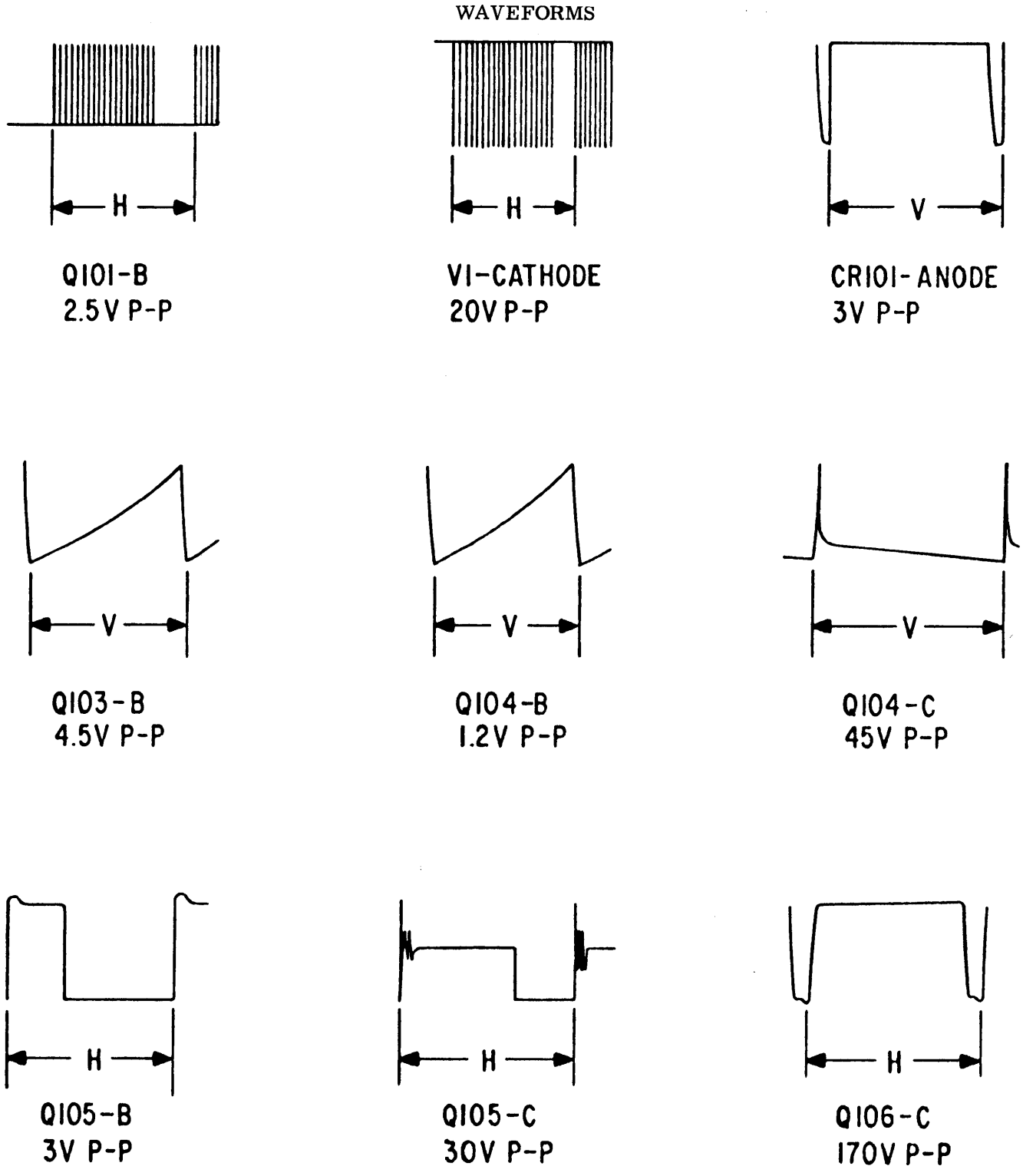


Figure 7-6. Monitor Voltage Waveforms

Internal Set Up Controls

(1) Height

(2) Vertical Linearity

(3) Vertical Hold

(4) Focus

(5) Width

(6) Low Voltage Adjust

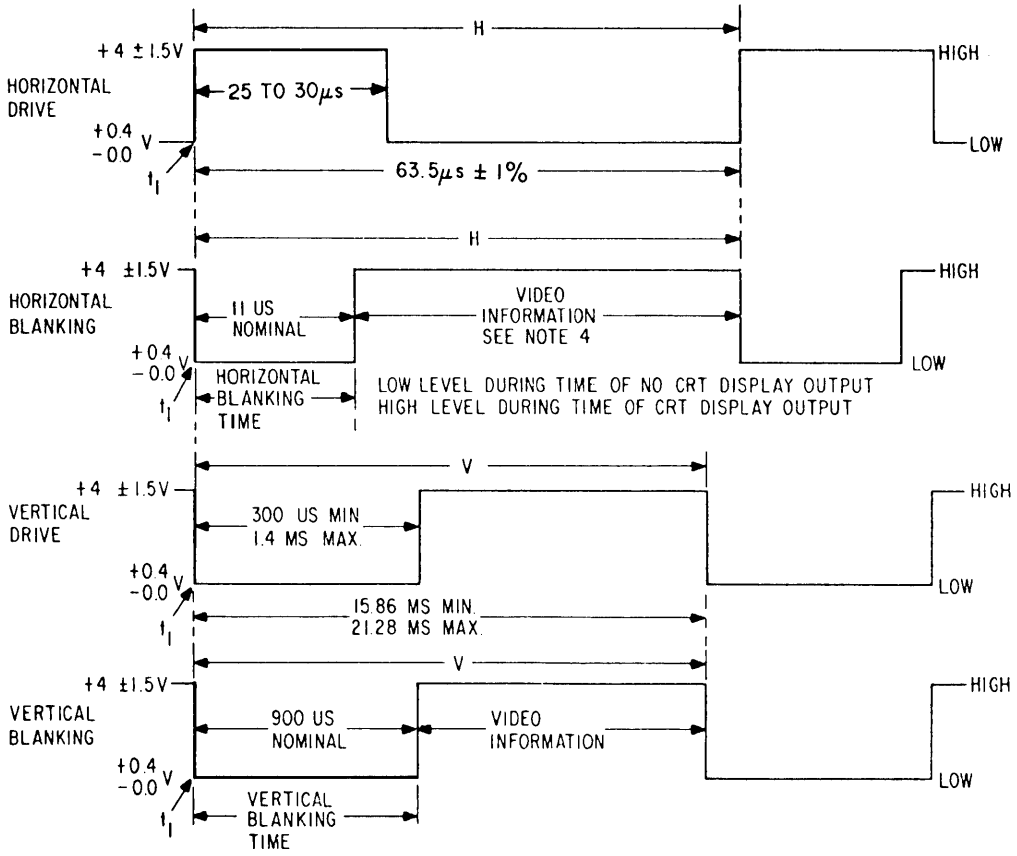


Figure 7-7. Input Signal Format

NOTES:

1. The leading edges of Drive and Blanking waveforms must start at time I_1. Nominal Blanking times should be observed.

2. H = Time from start of one line to start of next line.

3. V = Time from start of one field to start of next field.

4. Video pulse width should be equal to or greater than 100 nsec.

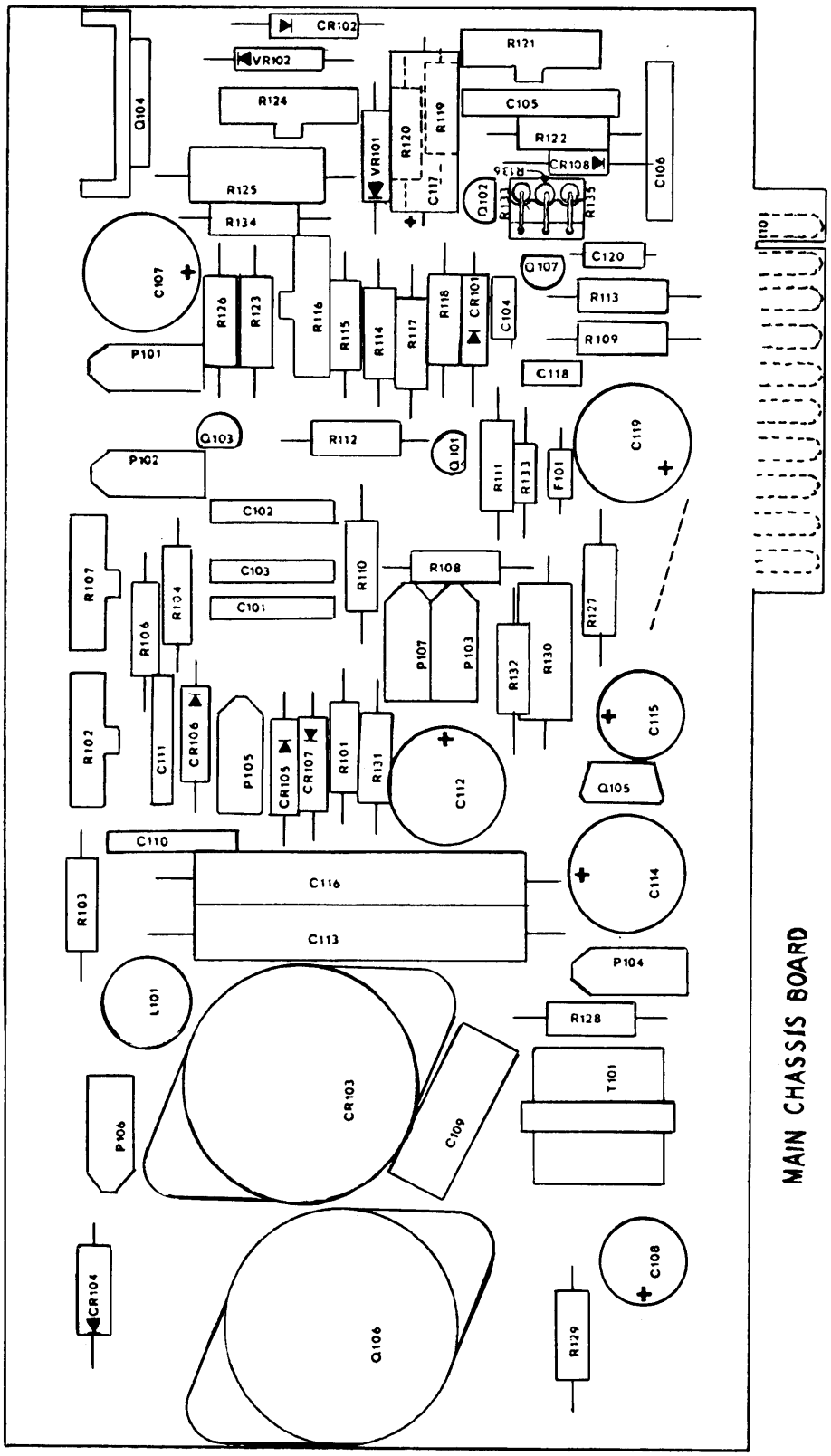


Figure 7-8. Monitor Circuit Board Component Location

Keyboard Troubleshooting Hints

The keyboard is considered a single replacement part except for the individual keys and the mounting hardware. The standard keyboard assembly contains 118 keys which provide pulses to the main logic board, which in turn generates the ASCII characters for transmission or display.

The most common problem with the keyboard is sticking of keys. Ensure that the cover is not binding the keys (sometimes the keys are hindered by the case pressing against them).

The ASCII code that should be generated by each key is shown in Table 5-2 in Section 5.

Main Logic Board Troubleshooting Hints

The main logic board is a self-contained functional unit, except for the power supply required to provide the +5V DC logic level.

Table 7-3 is a Main Logic Board Terminal Identification Chart. Each connector listed is explained below.

Connector J1 is for a Data Signal interface connection to the main logic board. Connectors J2 and J3 are used for the RS-232-C Extension Option and the Serial Printer Option, respectively.

Connector J4 supplies output signals from the main logic board to the CRT monitor. If the proper signals are present at connectors J5 and J6, examine the connector pins on P4.

Examine for obvious faults on main logic board. It is strongly recommended that no involved repairs be attempted on this board. Instead, contact the factory or authorized service representative.

Connector J5 primarily handles power inputs to the main logic board. The absence of proper inputs at terminals 1, 2, and 3 indicates failure in the AC power feed. A lack of proper voltage at terminal 6 indicates problems with the chassis mounted power supply or connector cable. Improper signals on terminals 4 and 5 indicate trouble with the main logic board.

Operate the keyboard and note if signal levels are present at terminals of connector J6; if signals are not present, examine keyboard assembly for obvious faults. Either repair or replace keyboard assembly.

Keyboard output levels are compatible with TTL circuits (logic "1" is +2.6V or greater at .10ma and logic "0" is less than 0.4V). The outputs are bounce free so that only one signal will be generated for each key depression. Two-key rollover interlocking is provided for all encoded keys. If a key is depressed before a previous operated key is released, the second key code is transmitted after the first key is released. A strobe pulse is provided with each encoded key output.

Figure 7-9 shows the main logic board assembly, detailing the terminal locations.

Power Supply Troubleshooting Hints

The power supply is mounted above the main circuit board on the chassis; it supplies the +5V DC to the main logic board (-5V, +12V, and -12V DC used by the main logic board are generated by regulator IC chips on the board itself).

The power supply is adjusted as follows:

a. Set current limit potentiometer for maximum current output (this is normal operating position).

CAUTION

DISCONNECT POWER SUPPLY OUTPUT LOAD BEFORE PROCEEDING THROUGH THE FOLLOWING STEPS.

b. Turn overvoltage protection potentiometer fully clockwise.

c. Adjust output voltage to +6V DC (nominal).

d. Adjust the overvoltage protection potentiometer counterclockwise to the point where output voltage is shut off.

e. Turn output voltage fully counterclockwise, then slowly clockwise until the output voltage reaches +6V DC (nominal). The output should then fall to the overvoltage level, verifying correct overvoltage protection adjustment.

f. Adjust the output voltage control to +5.2 volts DC, which is the normal operating voltage.

Table 7-3. Main Logic Board Terminal Identification Chart

CONNECTOR	TERMINAL SYMBOL	PINS	
RS-232-C Interface	J1	1-25	
RS-232-C Extension	J2	2	Transmit Data
		3	Receive Data
		4	Request to Send
		5	Clear to Send
		6	Data Set Ready
		8	Received Line Signal
		12	Secondary Received Line Signal
		19	Secondary Request to Send
Serial Printer (Option)	J3		
Monitor I/O	J4	1	Brightness
		2	Brightness
		3	Brightness
		4	Contrast
		5	Chassis Ground
		6	Video & Vertical Ground
		7	Horizontal Ground
		8	Horizontal Drive
		9	Vertical Drive
Logic Board Power	J5	1	AC Feed } 32 volts rms
		2	AC Feed }
		3	Equipment Ground
		4	Speaker
		5	Speaker
		6	DC Feed (+5 volts)
Keyboard I/O	J6	1	CTRL
		2	RESET
		3	
		4	BIT 8
		5	BIT 6
		6	BIT 4
		7	BIT 2
		8	BIT 1
		9	BIT 3
		10	BIT 5
		11	BIT 7
		12	PAGE EDIT
		13	SHIFT
		14	BREAK
		15	STROBE 1
		16	STROBE 0
		17	-20V POWER
		18	GROUND
		19	GROUND
		20	POWER } +5 volts
		21	POWER }
		22	PROTECT MODE
		23	CONVERSATIONAL MODE
		24	PROGRAM MODE

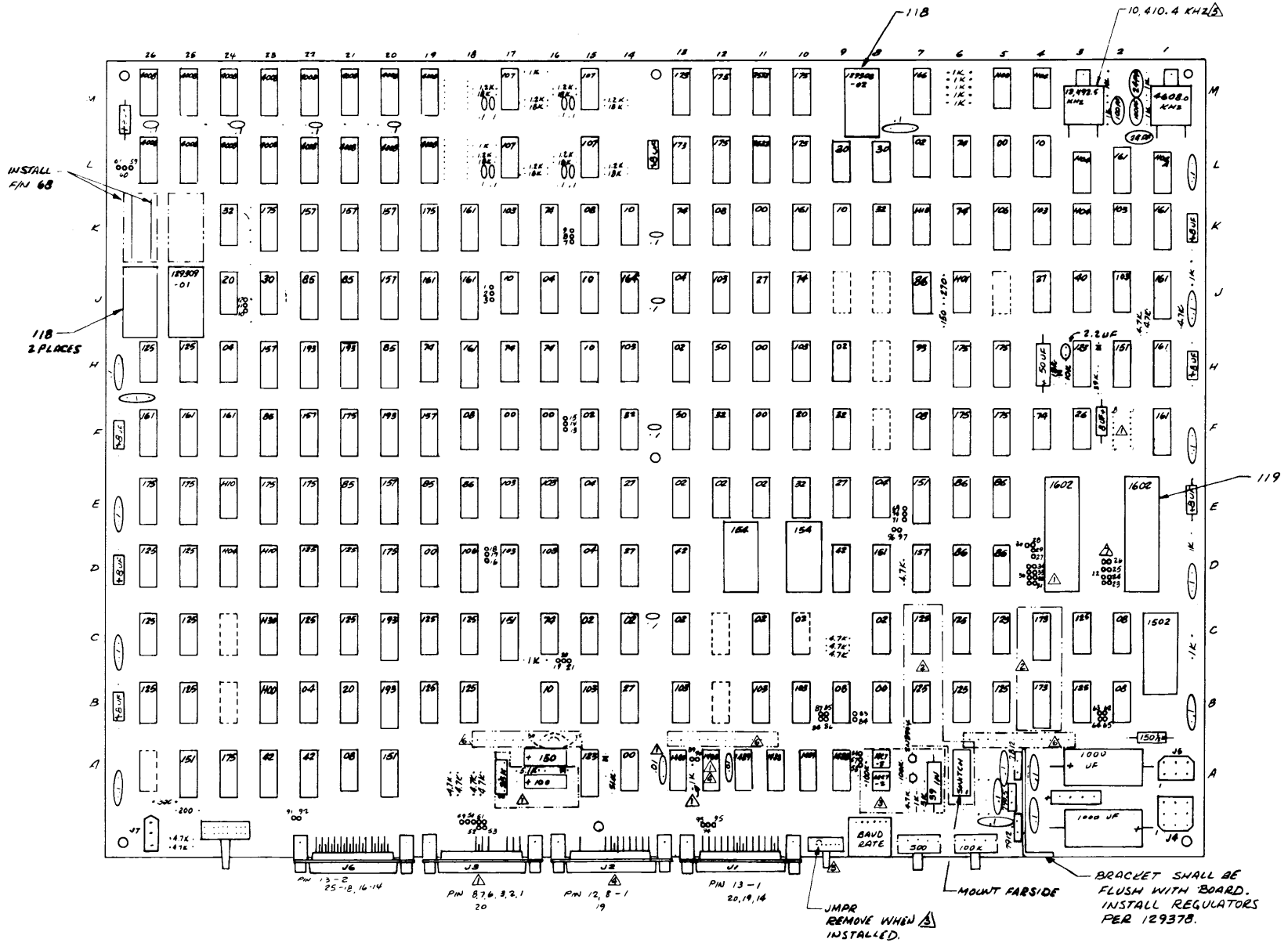


Figure 7-9. Main Logic Board Assembly with Terminal Locations

Troubleshooting ADM-2 Options

All ADM-2 options can be included in the previous troubleshooting procedures. The fastest way to determine if an optional device is failing, instead of the ADM-2 itself, is to simply replace or remove the option and test the ADM-2.

If an option operation only is failing, and the complete option cannot be removed from the unit, refer to the option drawings for locations of components while performing the procedures listed under Section 7.5, steps a-e.

7.6 RETURNING EQUIPMENT FOR REPAIR

Equipment returned to LSI must be shipped prepaid and must have a Return Goods Authorization (RGA) number on the outside top of the carton or the shipment may be lost, misrouted or returned to you. The following procedures should be followed:

a. Prepare the following information:

   1. Model type of equipment to be returned.
   2. Serial number.
   3. Reported symptom (if failure).
   4. Type of modification or option to be installed (if applicable).

b. Please call (714) 774-1010 ext. 371 or write to:

   Lear Siegler Inc./EID
   714 N. Brookhurst St.
   Anaheim, CA 92803
   Attn: Customer Service

   Please state that you would like a Return Goods Authorization number. At this time, we will record the information you prepared as well as a purchase order number, if applicable.

c. You will then be provided with an RGA number and the address of the depot where we request that you return the equipment.

NOTE

ALL MODIFICATIONS AND REPAIRS ARE FOB ANAHEIM, CALIFORNIA, CHICAGO, ILLINOIS, OR PHILADELPHIA, PENNSYLVANIA, WHICHEVER DEPOT IS USED. WARRANTY REPAIRS ARE TO BE SENT TO THE REPAIR DEPOT WITH FREIGHT PREPAID. THEY WILL BE RETURNED TO YOU WITH THE FREIGHT PREPAID.

APPENDIX A: ADM-2 PARTS LIST

129360-11 BOARD, PC ADM-2

COMPONENT NO.	QUANTITY	DESCRIPTION
128348-0	2	IC
128348-1	1	IC
128348-10	3	IC
128348-103	14	IC
128348-106	2	IC
128348-113	1	IC
128348-121	1	IC
128348-123A	2	IC
128348-125	22	IC
128348-1488	2	IC
128348-1489	3	IC
128348-1502	1	IC
128348-151	6	IC
128348-154	2	IC
128348-157	9	IC
128348-1602	2	IC
128348-161	13	IC
128348-164	1	IC
128348-166	1	IC
128348-173	3	IC
128348-175	17	IC
128348-193	5	IC
128348-2	13	IC
128348-26	1	IC
128348-27	6	IC
128348-30	1	IC
128348-3120	2	IC
128348-32	6	IC
128348-4	5	IC
128348-40	1	IC
128348-4102	16	IC
128348-42	4	IC
128348-74	12	IC
128348-7812	1	IC
128348-7912	1	IC
128348-8	10	IC
128348-85	6	IC
128348-86	6	IC
128348-93	1	IC
128349-104	4	CAP
128349-506	1	CAP
128349-805	8	CAP
128518-101	1	CAP, DM 15-101
128518-103	3	CAP
128518-104	12	CAP
128518-225	3	CAP 2.2 UF
128533-102	8	RESISTOR
128533-103	6	RESISTOR
128533-151	1	RESISTOR
128533-183	1	RESISTOR
128533-203	1	RESISTOR
128533-221	1	RESISTOR
128533-271	1	RESISTOR
128533-301	1	RESISTOR
128533-393	1	RESISTOR
128533-472	8	RESISTOR
128533-512	3	RESISTOR
128533-513	1	RESISTOR
128533-621	2	RESISTOR

129360-11 **BOARD, PC ADM-2**

COMPONENT NO.	QUANTITY	DESCRIPTION
128533-752	1	RESISTOR
128533-821	1	RESISTOR
128533-913	3	RESISTOR
128534-3	8	BRACKET
128578-0	8	IC
128578-10	8	IC
128578-20	3	IC
128578-30	4	IC
128578-4	7	IC
128578-50	2	IC
129308-2	1	CHARACTER GENERATOR
129309-1	1	ROM
129309-7	1	ROM
129329-104	6	CAP
129329-108	2	CAP
129349-107	1	CAP, TE1059.5
129360-13	1	BOARD, PC
129389-4	1	BRACKET
129471-151	1	RESISTOR
129471-911	2	RESISTOR, EB9115
129476-472	3	NETWORK, RESISTOR
801001	1	POT, 100K YQ8383
801002	1	POT, 500 YQ8384
802001	3	SOCKET CA14S10SD
802002	5	SOCKET CA16S10SD
802006	4	SOCKET CA24S10SD
802007	1	SOCKET CA28S10SD
802008	2	SOCKET CA40S10SD
802010	4	SOCKET, JACK 17-893
802011	17	SOCKET, SHORT PIN 17-1208
802012	40	CONNECTOR, 17-1209
804001	1	SWITCH, MSS-2250R
804002	1	SWITCH, MSS4350
804004	1	SWITCH, 435640-2
804005	2	SWITCH, 435640-3
804006	1	SWITCH, 435640-4
804008	1	SWITCH, CTS-235-1
804013	1	SWITCH, 1A216002G
805003	2	CAPACITOR, DM15-240
808001	1	RECTIFIER, BRIDGE MDA970-1
808003	6	DIODE, 1N 914
808005	1	DIODE, 1N 4002
809007	1	CONNECTOR, 09-18-5031
809010	1	CONNECTOR, 09-18-5061
809011	1	CONNECTOR, 09-18-5094
809013	4	CONNECTOR, 17-304-01
810001	2	TRANSISTOR, 2N3904
810004	2	TRANSISTOR, 2N5550
811002	AS REQ	CRYSTAL, 800A-10410.4KHZ
811006	1	CRYSTAL, 800A-12492.5KHZ
811007	1	CRYSTAL, 800A-4608KHZ
815002	1	COVER, 435238-5
819001	1	ISOLATOR, OPTICAL MCT-2
822402	2	NUT, 4-40 8003
822403	16	NUT, 4-40 5M PATT
823403	2	WASHER, 4 EXT. TOOTH
824006	8	RIVET, R3479X3/16
839001	2	INSULATOR, MYLAR, 43-77-2
839003	2	INSULATOR, 97405 OR 4X1/32

129356 KEYBOARD ASSY, ADM-2

COMPONENT NO.	QUANTITY	DESCRIPTION
129351-1	1	KEYBOARD
129353-3	1	HOUSING KEYBOARD
129355-3	1	CHASSIS, KEYBOARD DURA-COAT
129355-7	1	PLATE, PROTECTIVE
129395-41	1	CABLE
821406	4	SCREW, 4/24 SELF-TAP
821604	8	SCREW, 6-32X3/8 SEMS
823402	4	WASHER, SPLIT LOCK
823603	2	WASHER, 6 FLAT
832002	5	GROMMET, H559-3-2
832003	5	PLUNGER, NYLATCH H 323-3-3-2
832005	1	GROMMET, 1-62 G51H-B
834001	2	CLAMP, CABLE 3/8-6B
841001	6	FOOT, SJ151
841002	3	FOOT, SJ5504

129350 ADM-2 FINAL ASSY

COMPONENT NO.	QUANTITY	DESCRIPTION
128565-25	1	WIRE ASSY, 10" WHITE
128565-26	1	WIRE ASSY
128565-5	2	WIRE ASSY
128565-6	1	WIRE ASSY
128565-8	1	WIRE ASSY
128565-9	1	WIRE ASSY
128587-1	2	CAP
128595-3	1	PLATE, HINGE
129302-2	1	MONITOR, P4 ETCH
129305-13	1	BRACKET, FAN
129318-1	1	CABLE ASSY
129318-21	1	CABLE
129318-31	1	CABLE
129336-13	1	NAMEPLATE
129336-15	1	NAMEPLATE
129336-17	1	NAMEPLATE
129336-19	1	NAMEPLATE
129351-1	1	KEYBOARD
129352-3	1	HOUSING
129353-3	1	HOUSING KEYBOARD
129354-25	1	PANEL, REAR
129354-3	1	CHASSIS, TOP
129354-5	1	CHASSIS, BASE
129354-9	1	DUCT
129355-3	1	CHASSIS, KEYBOARD DURA-COAT
129355-7	1	PLATE, PROTECTIVE

COMPONENT NO.	QUANTITY	DESCRIPTION
129358-3	1	PLATE, ID
129360-11	1	BOARD, PC
129362	1	LOGO
129364-3	1	PLATE, ID
129365-5	1	NAMEPLATE
129366-3	1	BRACKET, HEATSINK
129395-41	1	CABLE
129398-3	1	REGULATOR
129398-5	1	TRANSFORMER
129455-3	1	CORD, POWER 115VAC
129487-1	1	SPEAKER
804003	1	SWITCH, TA101-TWB
815001	1	GUARD, FINGER, 6-182-033
819002	1	GASKET, 3/16X3/4X5'
821003	2	SCREW, 10-32X5/8 SEMS
821004	1	SCREW, 10-32X3/8 SEMS
821406	4	SCREW, 4/24 SELF-TAP
821604	17	SCREW, 6-32X3/8 SEMS
821605	3	SCREW, 6-32X1/2 SEMS
821607	1	SCREW, 6-32X5/8 TRUSS HEAD SS
821608	2	SCREW, 6-32X1/2 TRUSS HEAD SS
821609	2	SCREW, 6-32X3/4 TRUSS HEAD SS
821610	6	SCREW, 6-32X1/4 SEMS
821611	2	SCREW, 6-32X1/4 FH PHILLIPS
822602	8	NUT, PRESS 6-32-2
822603	4	NUT, NYLON N632-X
823003	1	WASHER, FLAT 10
823402	4	WASHER, 4 SPLIT LOCK
823603	2	WASHER, 6 FLAT
824003	8	RIVET, POT AD56ABS
824004	2	RIVET, POP AD52ABS
824005	3	RIVET, POP AAL63
83003	10	FASTENER, CADLE PANDUIT PLTIM-M
83004	1	FASTENER, SR-6P3-4
83005	3	FASTENER, SUPPORT LCBS-3N
83006	3	FASTENER, NAIL #16X1/2
832002	5	GROMMET, H559-3-2
832003	5	PLUNGER, NYLATCH H 323-3-3-2
832005	1	GROMMET, 1-62 G51H-B
834001	2	CLAMP, CABLE 3/8-6B
836001	1	CIRCUIT BREAKER, 81504.5
837001	1	BLOCK, 912-2-K179-K475-K474
838002	1	FAN 3-15-2470
839004	5	INSULATOR, NYLON NWG-3124
839006	4	INSULATOR, NYLON SP73
839007	4	INSULATOR, NYLON SP37
841001	12	FOOT, SJ151
841002	3	FOOT, SJ5504

APPENDIX B: ADM-2 WIRE LIST, CABLING, AND PIN ASSIGNMENTS

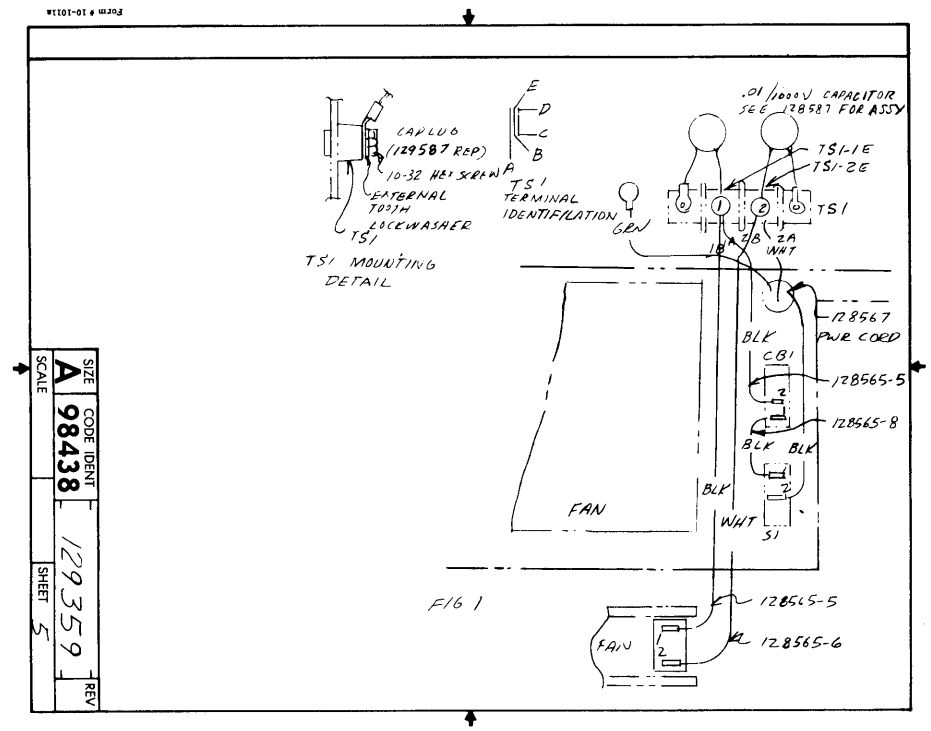
WIRE LIST

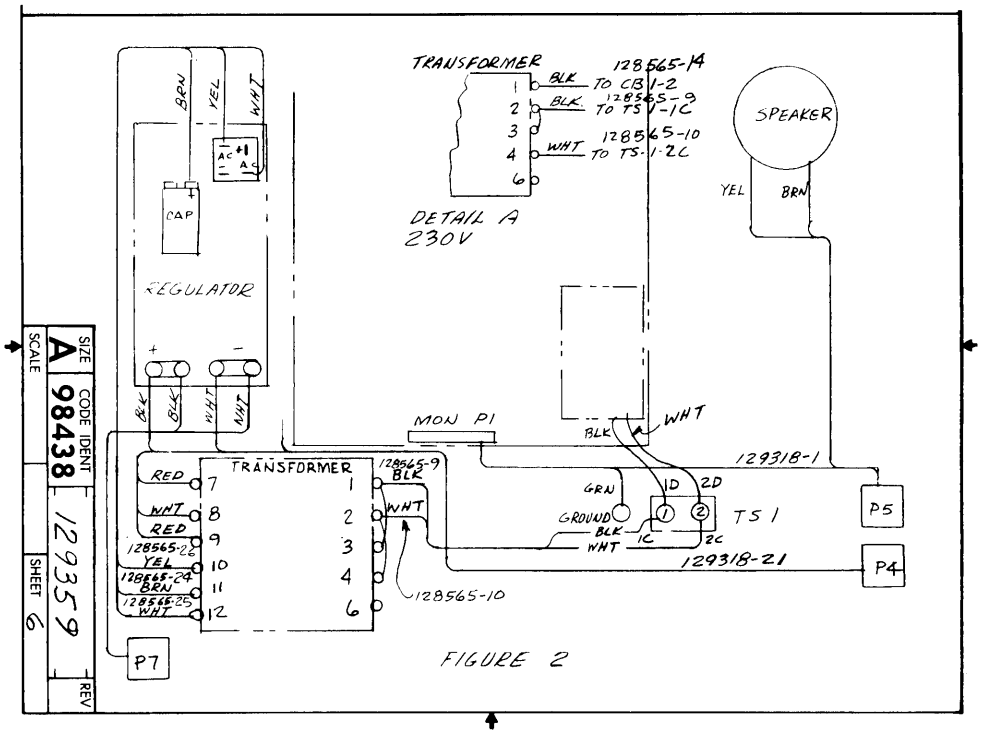
(Drawing No. 129359)

Qty.	Find No.	Part or Identifying No.	Nomenclature or Description	Material or Code Ident	Specification
1	1	129395-41	Cable		
	2				
A/R	3	8919(See list for color)	Wire, 20AWG (10x30)	-102O. D.	Belden or Equivalent
1	4	129318-1	Cable, Monitor		
1	5	129318-21	Cable, Power		
1	6	128567	Power Cord		
2	7	128565-5	Wire Assy 8" blk	16 AWG	
1	8	128565-6	Wire Assy 8" Wht	16 AWG	
1	9	128565-8	Wire Assy 4" blk	16 AWG	
1	10	128565-14	Wire Assy 17" blk	16 AWG	
1	11	128565-9	Wire Assy 13" blk	18 AWG	
1	12	128565-10	Wire Assy 13" wht	18 AWG	
1	13	128565-24	Wire Assy 10" brn	18 AWG	
1	14	128565-25	Wire Assy 10" wht	18 AWG	
1	15	128565-26	Wire Assy 10 yel	18 AWG	
1	16	129318-31	Cable, Power		
2	17	3000 #20A	Tab Terminal . 250		Arkless or Equivalent
A/R	18	FIT-105	Heat Shrinkable Tubing		Alpha or Equivalent

Termination Information							Wire Information					
			From		To		From End			To End	Wire	
Line #	Fig #	Wire # or Color	Ref. Des.	Pin	Ref. Des.	Pin	Conn	Termination	Conn	Termination	or Cable	Lgth
1	2		P4		Mon	P1					4	
2	2		P5		1*						5	
3		blk			S1	2						
4	1	wht			TS1	2A					6	
5		grn			2*							
6	1	blk	Fan	1	TS1	1B		(110 Tab)		(250 Tab)	7	(8)
7	1	wht	Fan	2	TS1	2B		(110 Tab)		(250 Tab)	8	(8)
8	1	blk	S1	1	CB1	1		(250 Tab)		(110 Tab)	9	(4)
9	1[5*]	blk	CB1	2	TS1	1A		(110 Tab)		(250 Tab)	7	(8)
10	2[5*]	blk	T1	1	TS1	1C		4*		(250 Tab)	11	(13)
11	2[5*]	wht	T1	2	TS1	2C		4*		(250 Tab)	12	(13)
12	2	blk	Mon[3*]		TS1	1D				17, 18		
13	2	wht	"		TS1	2D				17, 18		
14	2	brn	T1	11	Reg	Cap+		4*		(Spade)	13	(10)
15	2	wht	T1	12	Reg	AC		4*		(250 Tab)	14	(10)
16	2	yel	T1	10	Reg	AC		4*		(250 Tab)	15	(10)
17	2[5*]	blk	T1	1	T1	3		4*		4*	3	(3)
18	2[5*]	wht	T1	2	T1	4		4*		4*	3	(3)
19			KB	6*	P6							
20	2		P7		P. S Reg						16	
21	Detail	blk	CB1	2	T1	1		(110 Tab)		4*	10	(17)
22	A	blk	T1	2	TS1	1C		4*		(250 Tab)	11	(13)
23	Fig 2	wht	T1	4	TS1	2D		4*		(250 Tab)	12	(13)
24	230 V	blk	T1	1	T1	2		4*		4*	3	(3)

CODE NOTES:
1* - See 129318-21 for termination
2* - Terminate at GRD STUD
3* - Terminate existing wire from monitor
4* - Soldered termination
5* - 110V, 60 Hz
6* - See 129395-41 for term cable called out on 129356-1 KB Assy.





NOTES:

Remove green wire in cable 129318-1 terminated at chassis ground and terminate under mount screw of TS-1.

Route 129318-1 and 129318-21 cable assemblies between monitor and TS-1.

A.C. Wires 128565-9 and -10 shall be routed over and secured to top of fan along with monitor A.C. and fan A.C. wires.

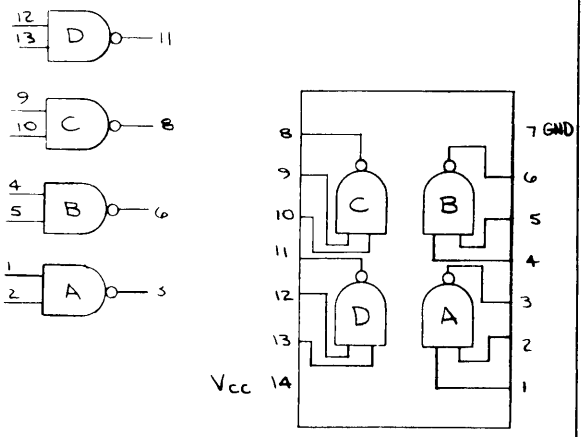
I.C. PIN ASSIGNMENTS FOR ADM SERIES

TYPE	PAGE	FUNCTION
7400	B-6	QUAD 2 NAND
74H01	B-6	QUAD 2 NAND
7401	B-6	HEX 1 NAND (O.C.)
7402	B-6	QUAD 2 NOR
7404	B-6	HEX 1 NAND
74H04	B-6	HEX 1 NAND
7405	B-6	HEX 1 NAND WITH OPEN COLLECTER
7408	B-7	QUAD 2 AND
7410	B-7	TRIPLE 3 NAND
74H20	B-7	DUAL 4 NAND
7426	B-6	QUAD 2 NAND (H.V.) – SAME AS 7400
7427	B-7	TRIPLE 3 NOR
7430	B-8	SINGLE 8 NAND
74H30	B-8	SINGLE 8 NAND
7432	B-8	QUAD 2 OR
7440	B-8	DUAL 4 NAND BUFFER
74H40	B-8	DUAL 4 NAND BUFFER
7442	B-8	1 OF 10 DECODER
74H51	B-9	DUAL AND/OR
7474	B-9	DUAL D FLIP-FLOP
74H85	B-9	4 BIT COMPARATOR
7486	B-9	QUAD 2 EXCLUSIVE OR
7493	B-10	4 BIT BINARY COUNTER
74H103	B-10	DUAL J-K FLIP-FLOP
74H106	B-10	DUAL J-K FLIP-FLOP

I.C. PIN ASSIGNMENTS FOR ADM SERIES (Cont.)

TYPE	PAGE	FUNCTION
745S113	B-10	DUAL J-K FLIP-FLOP W/PRESET
74121	B-11	MONOSTABLE MULTIVIBRATOR
74123	B-11	DUAL MONOSTABLE MULTIVIBRATORS W/CLEAR
74125	B-11	QUAD TRI-STATE BUS
74151	B-11	BINARY DATA SELECTOR/MULTIPLEXEX
74154	B-12	1 OF 16 DECODER
74157	B-12	QUAD 2 TO 1 DATA SELECTOR
74161	B-12	BINARY HEX COUNTER
74164	B-12	8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER
74166	B-13	8-BIT SHIFT REGISTER
74173	B-13	4-BIT D-TYPE REGISTER W/TRI-STATE OUTPUTS
74175	B-13	QUAD D-TYPE FLIP-FLOP
74193	B-13	4-BIT UP/DOWN COUNTER DUAL CLOCK/WITH CLEAR
75188	B-14	QUAD LINE DRIVER (RS232-C)
MC1488L	B-14	QUAD LINE DRIVER (RS232-C)
75189	B-14	QUAD LINE RECEIVER (RS232-C)
MC1489L	B-14	QUAD LINE RECEIVER (RS232-C)
2102	B-14	1024-BIT STATIC RAM
2602	B-14	1024-BIT STATIC RAM
1502	B-14	F.I.F.O. BUFFER REG.
1602	B-15	ASYNCHRONOUS RECEIVER/TRANSMITTER
3120	B-15	QUAD 80 BIT STATIC SHIFT REGISTER
129308–02	B-15	ROM
129309-01	B-15	ROM

MFG. NO. SN74H01N
SN74H00N
SN7400N
SN7426N
N8H80A

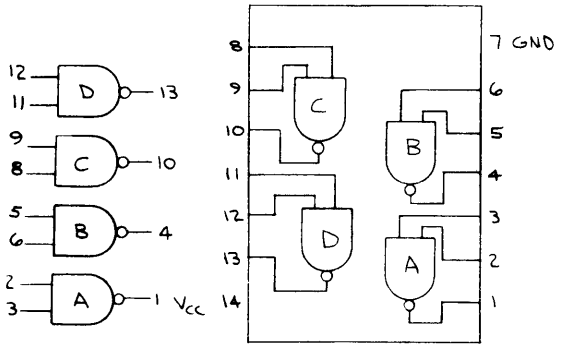


QUAD 2 NAND

SIZE	CODE IDENT		REV
A	98438	00 H01 08 26	N/C

SCALE NONE SHEET

MFG. NO. SN7401N

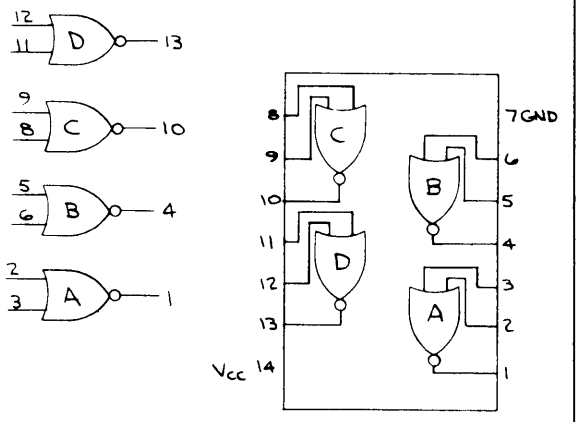


HEX 1 NAND (OC)

SIZE	CODE IDENT		REV
A	98438	01	N/C

SCALE NONE SHEET

MFG. NO. SN7402N

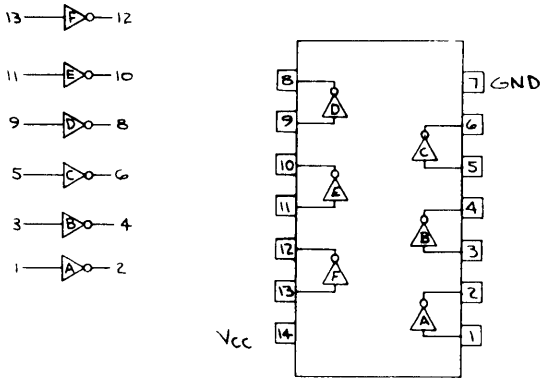


QUAD 2 NOR

SIZE	CODE IDENT		REV
A	98438	02	N/C

SCALE NONE SHEET

MFG. NO. SN74H04N
SN7404N
SN7405N

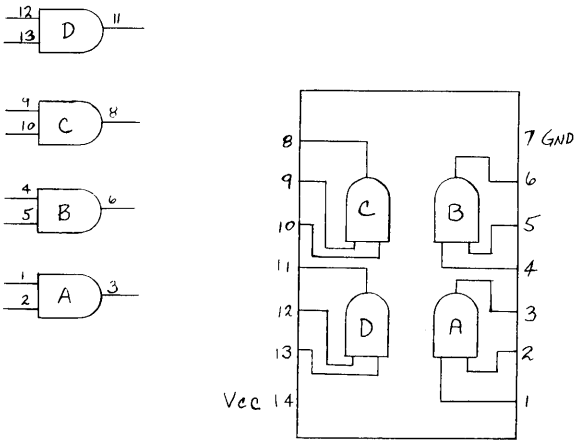


HEX 1 NAND

SIZE	CODE IDENT		REV
A	98438	04/05	N/C

SCALE NONE SHEET

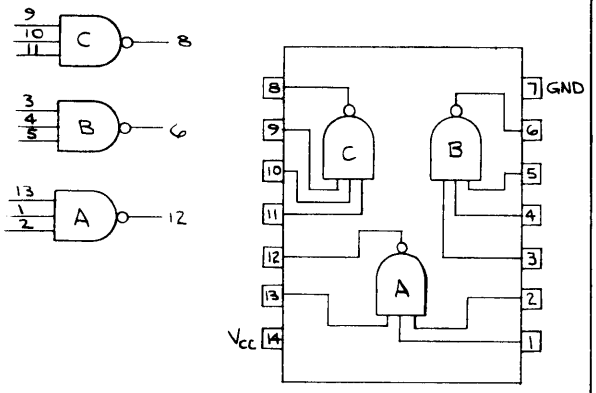
MFG. No. SN7408N



QUAD 2 AND

SIZE	CODE IDENT		REV
A	98438	08	N/C
SCALE None		SHEET 7	

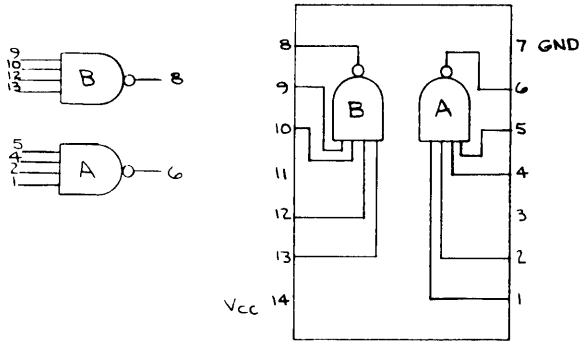
MFG. NO. SN74H10N
SN7410N
SN74H11N
U6A900359X



TRIPLE 3 NAND

SIZE	CODE IDENT		REV
A	98438	10/11	N/C
SCALE NONE		SHEET	

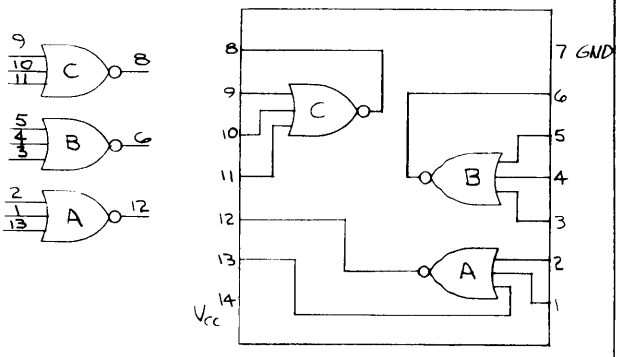
MFG. NO. SN74H20N
SN7420N
SN74H21N



DUAL 4 NAND

SIZE	CODE IDENT		REV
A	98438	20/21	N/C
SCALE NONE		SHEET	

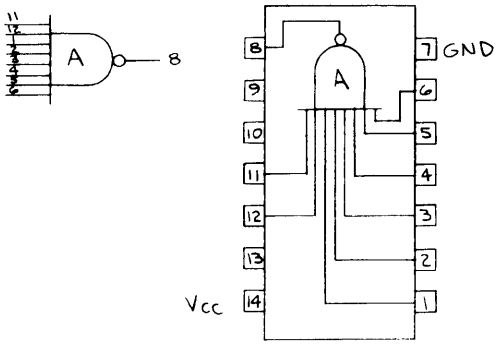
MFG. NO. 8875A
SN7427N



TRIPLE 3 NOR

SIZE	CODE IDENT		REV
A	98438	875/27	N/C
SCALE NONE		SHEET	

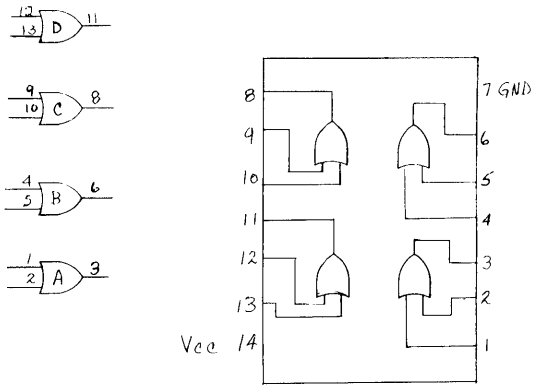
MFG. NO. SN74H30N
SN7430N



SINGLE 8 NAND

SIZE	CODE IDENT		REV
A	98438	30	N/C
SCALE NONE		SHEET	

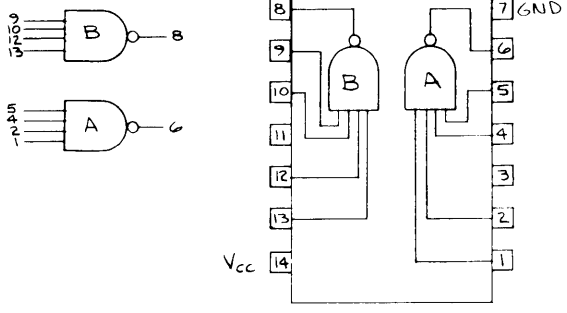
MFG. No. SN7432N



QUAD 2 OR

SIZE	CODE IDENT		REV
A	98438	32	N/C
SCALE NONE		SHEET 1	

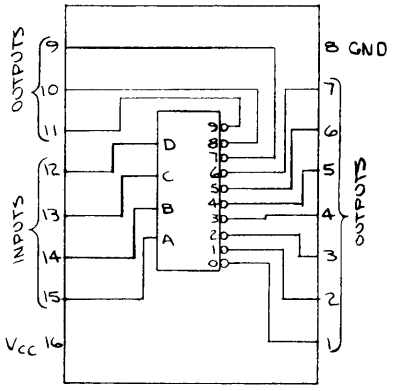
MFG. NO. SN74H40N
SN7440N



DUAL 4 NAND BUFFER

SIZE	CODE IDENT		REV
A	98438	40	N/C
SCALE NONE		SHEET	

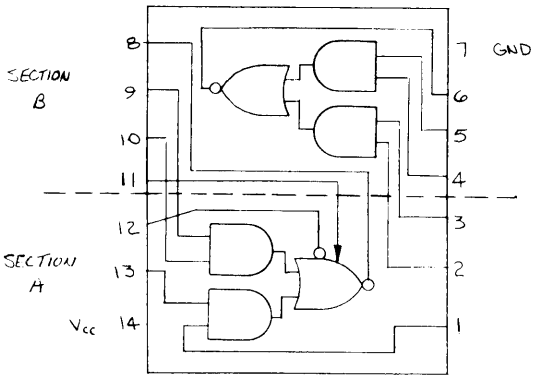
MFG. NO. SN7442N



1 OF 10 DECODER

SIZE	CODE IDENT		REV
A	98438	42	N/C
SCALE NONE		SHEET	

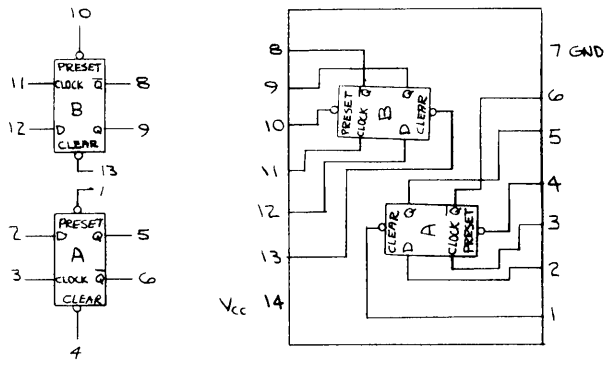
MFG. NO. SN74H51N



DUAL 2 AND/OR

SIZE	CODE IDENT		REV
A	98438	H51	
SCALE		SHEET	

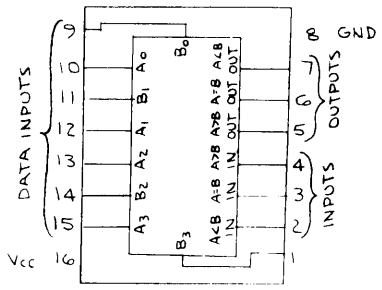
MFG. NO. SN7474N



DUAL D FLIP-FLOPS

SIZE	CODE IDENT		REV
A	98438	74	N/C
SCALE NONE		SHEET	

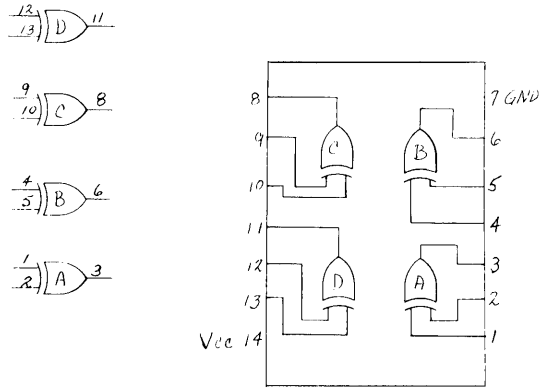
MFG NO. SN74H85N



4-BIT COMPARATOR

SIZE	CODE IDENT		REV
A	98438	H85	
SCALE		SHEET	

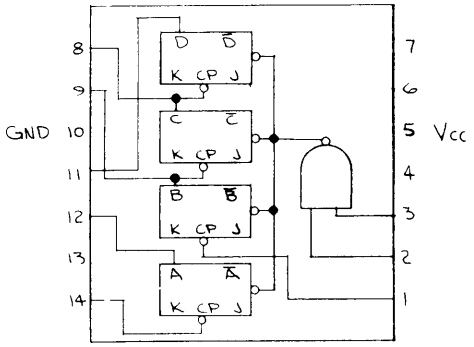
MFG. No. SN7486N



QUAD 2 EXCLUSIVE OR

SIZE	CODE IDENT		REV
A	98438	86	
SCALE NONE		SHEET 23	

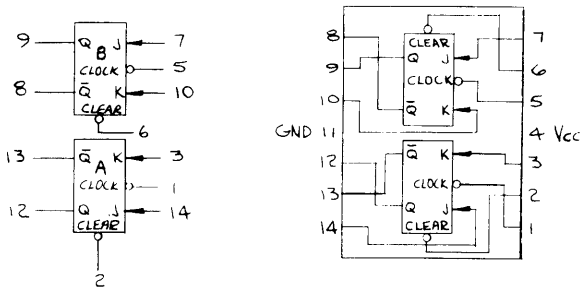
MFG. NO. SN7493N



4-BIT BINARY COUNTER

SIZE	CODE IDENT		REV
A	98438	93	
SCALE NONE		SHEET	

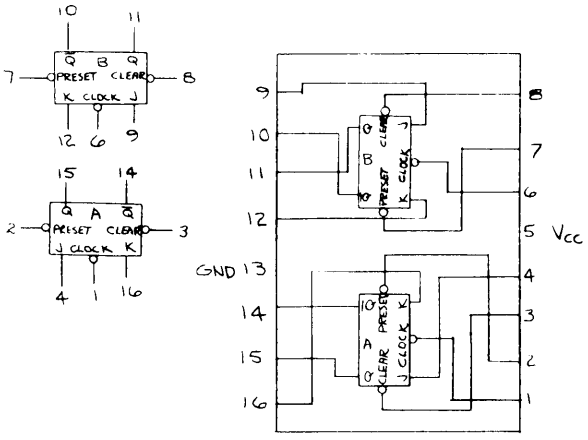
MFG. NO. SN74H103N



DUAL J-K FLIP-FLOP

SIZE	CODE IDENT		REV
A	98438	H103	
SCALE NONE		SHEET	

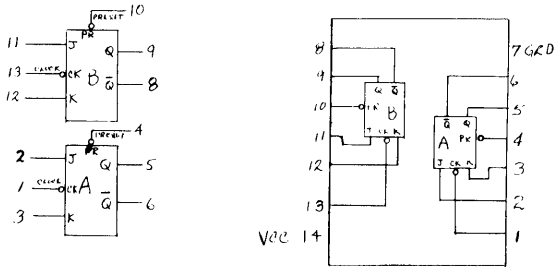
MFG. NO. SN74H106N



DUAL J-K FLIP-FLOPS

SIZE	CODE IDENT		REV
A	98438	H106	N/C
SCALE NONE		SHEET	

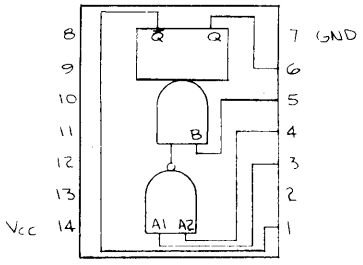
MFG. No. SN74S113N



DUAL J-K FLIP-FLOP W/ PRESET

SIZE	CODE IDENT		REV
A	98438	3113	N/C
SCALE NONE		SHEET 32	

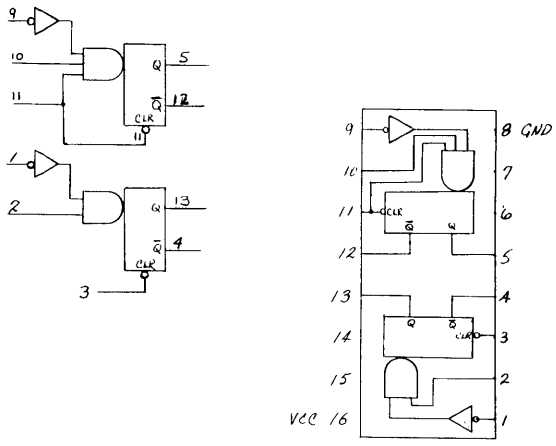
MFG. NO. SN74121N



MONOSTABLE MULTIVIBRATOR

SIZE	CODE IDENT		REV
A	98438	121	
SCALE NONE		SHEET	

MFG. No. SN74123N

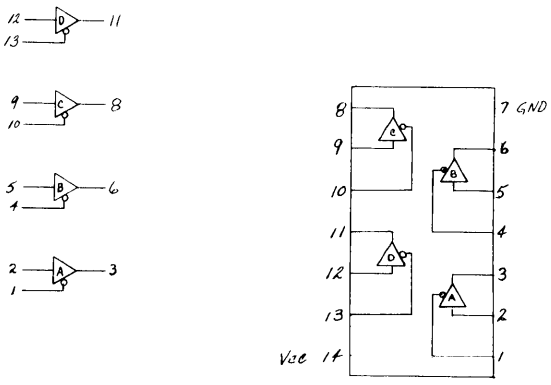


NOTE: NATIONAL 74123 is different in (CLR@ PIN 11) it is not tied to the input gate.

DUAL MONOSTABLE MULTIVIBRATORS W/CLEAR

SIZE	CODE IDENT		REV
A	98438	123	N/C
SCALE NONE		SHEET 35	

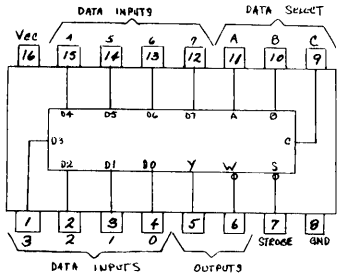
MFG. No. SN74125N



QUAD TRI-STATE BUS

SIZE	CODE IDENT		REV
A	98438	125	N/C
SCALE NONE		SHEET 36	

Mfg. No SN74151 SN74151A



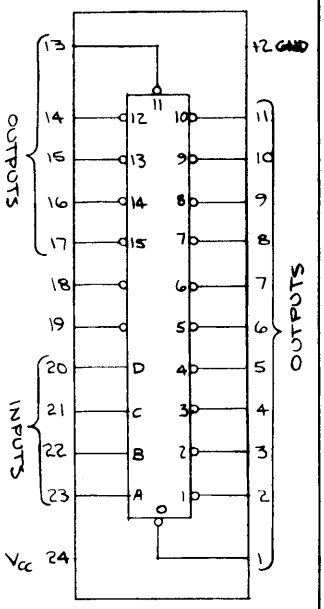
151A, 151
FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT					
C	B	A	S	Y	W
X	X	X	1	0	1
0	0	0	0	D0	$\overline{D0}$
0	0	1	0	D1	$\overline{D1}$
0	1	0	0	D2	$\overline{D2}$
0	1	1	0	D3	$\overline{D3}$
1	0	0	0	D4	$\overline{D4}$
1	0	1	0	D5	$\overline{D5}$
1	1	0	0	D6	$\overline{D6}$
1	1	1	0	D7	$\overline{D7}$

BINARY DATA SELECTOR/MULTIPLEXER

SIZE	CODE IDENT		REV
A	98438	151 / 151A	N/C
SCALE NONE		SHEET 37	

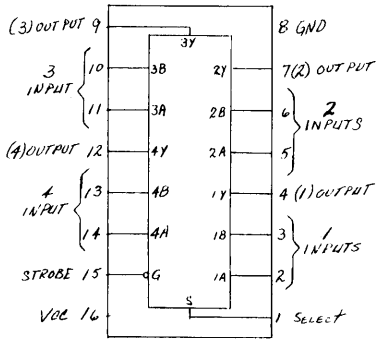
MFG. NO. SN74154N



1 OF 16 DECODER

SIZE	CODE IDENT		REV
A	98438	154	N/C
SCALE NONE		SHEET	

MFG. No. SN74157N

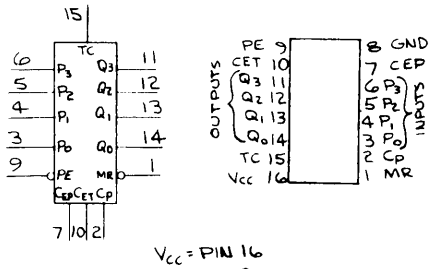


Strobe:
Select = 0 → A inputs
Select = 1 → B inputs

QUAD 2 to 1 DATA SELECTOR

SIZE	CODE IDENT		REV
A	98438	157	N/C
SCALE NONE		SHEET 39	

MFG. NO. U6B9316 59X
U6B9310 59X
74161N

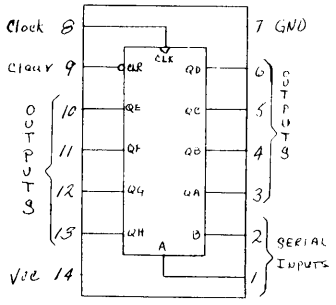


V_{CC} = PIN 16
GND = PIN 8

BINARY HEX. CTR.

SIZE	CODE IDENT		REV
A	98438	161	N/C
SCALE NONE		SHEET	

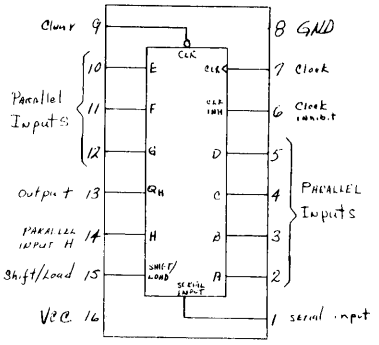
MFG. No SN74164N



8-Bit Parallel-out Serial Shift Reg.

SIZE	CODE IDENT		REV
A	98438	164	N/C
SCALE NONE		SHEET 41	

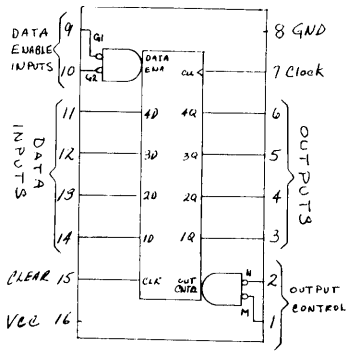
MFG. No. SN74166



8-Bit Shift Register

SIZE	CODE IDENT		REV
A	98438	166	N/C
SCALE None		SHEET 42	

MFG. No. SN74173N



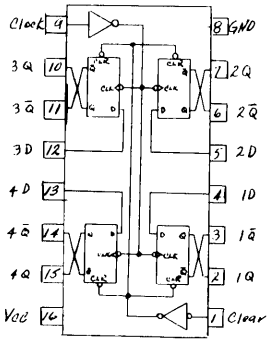
4-Bit D-Type Reg. w/Tri-State Outputs

SIZE	CODE IDENT		REV
A	98438	173	N/C
SCALE None		SHEET 43	

MFG. No. SN74175N

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

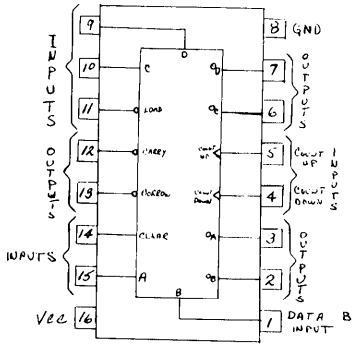
Function Table



Quad D-Type Flip-Flop

SIZE	CODE IDENT		REV
A	98438	175	N/C
SCALE None		SHEET 44	

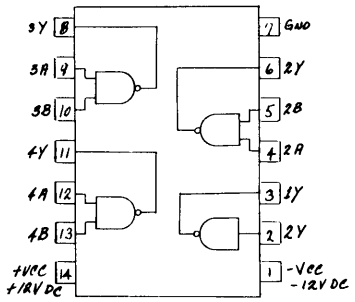
MFG. No. SN74193



4-Bit UP/DOWN COUNTER
DUAL Clock / with Clear

SIZE	CODE IDENT		REV
A	98438	193	N/C
SCALE None		SHEET 46	

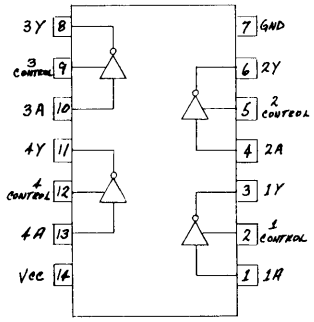
Mfg. No. SN75188
MC1488L



RS232C (OUTPUT -12 to +12)
QUADRUPLE LINE DRIVER

SIZE	CODE IDENT		REV
A	98438	SN75188 MC1488L	N/C
SCALE NONE		SHEET 49	

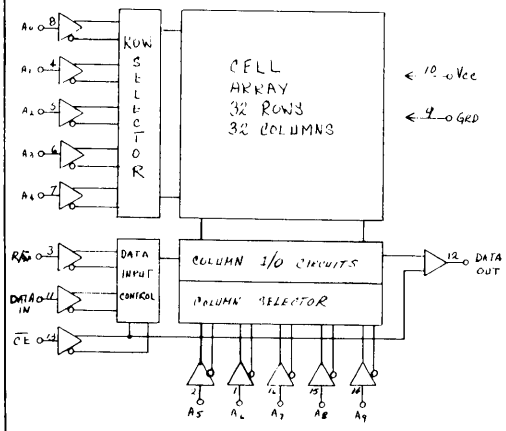
Mfg. No SN75189, SN75189A
MC1489, MC1489A

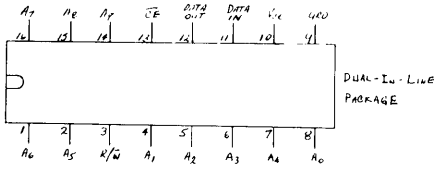


RS232-C (INPUT -12 TO +12)
QUAD LINE RECEIVERS

SIZE	CODE IDENT		REV
A	98438	75189, 75189A MC1489, MC1489A	N/C
SCALE NONE		SHEET 50	

MFG. No. MM2102
2602

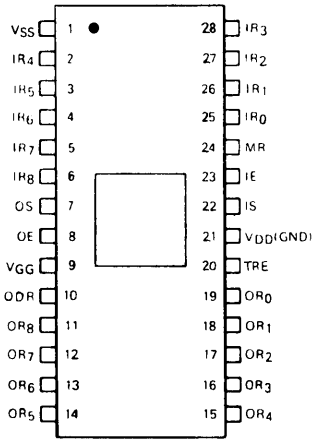




1024-Bit Static RAM

SIZE	CODE IDENT		REV
A	98438	2102 2602	N/C
SCALE NONE		SHEET 56	

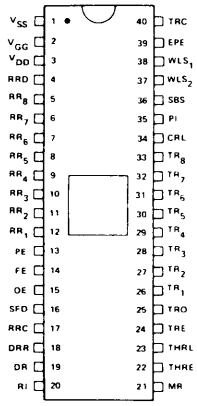
MFG. No. 1502



F.I.F.O. Buffer Reg.

1502

MFG. NO. 1602

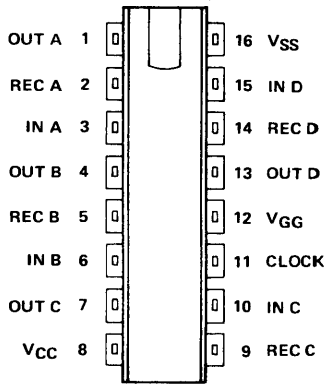


ASYNCHRONOUS RECEIVER/TRANSMITTER

1602

MFG. NO. 3120

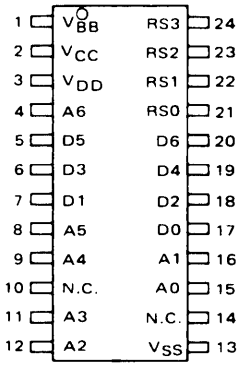
16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



QUAD 80 BIT STATIC SHIFT REGISTER

3120

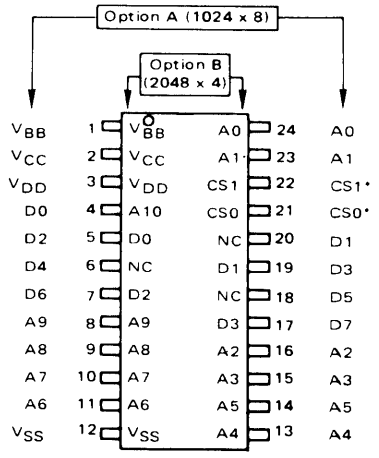
MFG. NO. 129308-02



ROM

129308-02

MFG. NO. 129309-01



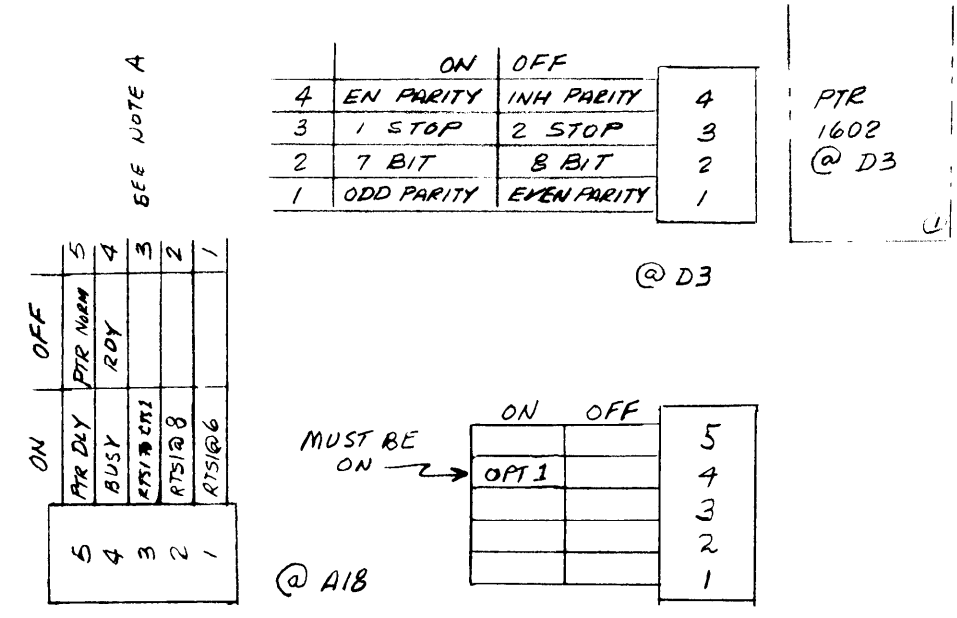
*MCM6561 and MCM6562 are pre-programmed to be selected with a low input at CS.

ROM

129309-01

APPENDIX C: ADM-2 OPTION DRAWINGS

FIND NO.		QTY REQD			PARTS LIST			
		13	9	5D	PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1		1	1	1	128348-1602	UART	D3	
2		2	2	2	128534-01	BRACKET		
3		REF	REF	REF	17-304-01	CONN HOUSING	AMPHENOL J3	
4		1	1	1	17-1208	SOCKET, SHORT	" @ 20	
5		6	6	6	17-1209	SOCKET, LONG	" @ 1,2,3,6,7,8	
6		1	1	1	17-893	JACK SOCKET	"	
7		4	4	4	4-40	NUT, HEX, STL, SMALL PATTERN		
8		1	1	1	CA 40 S-10, SD	SOCKET, 40 PIN	CIRCUIT ASSEMBLY	
9		1	1	1	128349-107	CAPACITOR, 100 UF, 3V	SPRAGUE	
10		1	1	1	IN914	DIODE		
11		1	1	1	128533-512	RESISTOR 5.1K		
12		1	1	1	" -203	" 20K		
13		1	1	1	128348-123	I.C.	A15	



A. IF INTERNAL DELAY (RTSI TO CTSI) IS REQUESTED CUT ETCH TO PIN 20 OF J3.

OPTION 1	SIZE A	CODE IDENT 98438	129504 REV B
TITLE PRINTER	SCALE		SHEET 2
SHEET 1 OF 2			

Form # 10-1011a

ITEM NO.	QTY REQD				PARTS LIST			
					PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1				1	128348-1488	I.C.	A12B	
2				1	128518-103	CAPACITOR		
3								
4								
5				1	128348-123	I.C.	A15	
6								
7				1	435640-3	SWITCH 5 POS	AMP	
8				1	435640-2	SWITCH 4 POS	AMP	
9								
10				REF		ROM	REF	1
11				REF		PROM	REF	1
12								
13								

NOTES: 1. SEE SHEET 16 FOR ROM/PROM PLACEMENT

OPTION 1
TITLE PRINTER
SHEET 2 OF 2

SIZE	CODE IDENT		REV
A	98438	129504	B
SCALE		SHEET 3	

Form # 10-1011a

FIG NO.	QTY REQD				PARTS LIST			
					PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1								
2				2	128348-125		B7, C7	
3				2	128348-173		B4, C4	
4								
5								
6				1	435668-7	SWITCH	AMP INC @A6	
7				1	435238-5	COVER	"	
8								
9				REF		ROM	REF	3
10				REF		PROM	REF	3
11								
12								
13								

NOTES: 1. ADD JUMPER E101 - E102

2. PLACE "CONV" SW. IN "BLOCK" (MIDDLE) POSITION

3. SEE SHEET 16 FOR ROM/PROM DESIGNATION & PLACEMENT

OPTION 2

TITLE POLLING

SHEET 1 OF 1

SIZE	CODE IDENT		REV
A	98438	129504	B
SCALE		SHEET 4	

Form # 10-1011a

FWD NO.	QTY REQD				PARTS LIST			
					PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1				2	MCT-2	OPTICAL ISOLATOR	MONSANTO	
2				2	2N3904	TRANSISTOR		
3				2	2N5550	"		
4				1	1N4002	DIODE		
5				1	1N914	"		
6				1	128533-221	RESISTOR 220		
7				2	-621	" 620		
8				2	-472	" 4.7K		
9				3	-913	" 91K		
10								
11				1	MSS-2250	SWITCH	ALCOSWITCH	
12				2	EB9115	RESISTOR, 910, .5W,	ALLEN BRADLEY	
13								

SEE 129360-11 FOR LOCATION

OPTION 3	SIZE A	CODE IDENT 98438	129504 REV B
TITLE CURRENT LOOP	SCALE		SHEET 5
SHEET 1 OF 1			

Form # 10-1011a

ITEM NO.	QTY REQD				PARTS LIST			
					PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1				1	128348-1488	I.C.		
2				REF	17-304-01	CONN, HOUSING	AMPHENOL J2	
3				1	17-1208	SOCKET, SHORT	" @19	
4				9	17-1209	SOCKET, LONG	" @1-8, 12	
5				1	17-893	JACKSCREW	"	
6				2	128534-03	BRACKET, CONN		
7				2		POP RIVET		
8				4	4-40	NUT, HEX, STL, SMALL PATTERN		
9								
10								
11								
12								
13								

OPTION 4
TITLE RS232 EXTENSION
SHEET 1 OF 1

SIZE	CODE IDENT		REV
A	98438	129504	B
SCALE		SHEET 6	

Form # 10-1011a

PARTS LIST

ITEM NO.	QTY REQD	PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1	1	800-A-10.4104 MHZ	CRYSTAL	STANDARD CRYSTAL M3	
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					

REPLACES 12.4925 MHZ CRYSTAL

OPTION 5

TITLE 50 HZ OPERATION

SHEET 1 OF 1

SIZE	CODE IDENT		REV
A	98438	129504	B

SCALE

SHEET 7

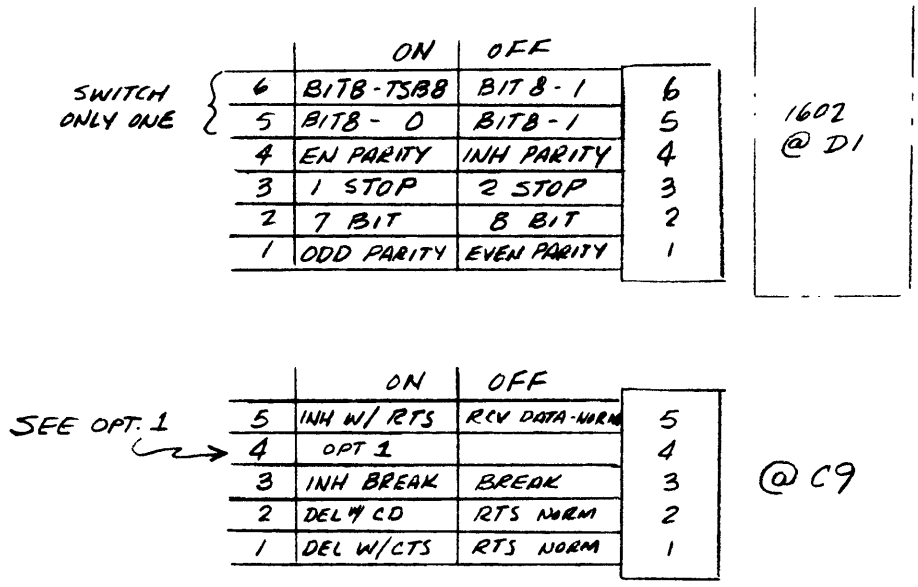
Form # 10-1011a

FIND NO.	QTY			REQD	PARTS LIST			
					PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1				REF	129309	ROM		
2				REF	129309			
3								
4				3	09-64-1122	FLAT WAFER, 12 PIN	MOLEX	
5								
6				1	129385	P.C. BOARD		
7								
8								
9				1	129390			
10				1	ICY-246-52	SOCKET	ROBINSON-NUGENT @ K26	
11				2	SP-72	STANDOFF 3/4	WECKESSER	
12				2	SP-53	" 7/16	"	
13				2	SP-41	" 1/4	"	

NOT AVAILABLE

OPTION 6	SIZE A	CODE IDENT 98438	129504	REV B
TITLE EXTENDED MEMORY				
SHEET 1 OF 1	SCALE		SHEET 8	

Form # 10-1011a



FOR JUMPERS AT E62-65 REFER TO 129501

OPTION 7 TITLE INTERFACE SHEET 1 OF 1	SIZE A	CODE IDENT 98438	129504 REV B
	SCALE		SHEET 9

Form # 10-1011a

JUMPER E103 TO 104 WILL INHIBIT DELAY

OPTION 8 TITLE RTS TURN OFF DELAY SHEET 1 OF 1	SIZE A	CODE IDENT 98438	129504	REV B
	SCALE		SHEET 10	

Form # 10-1011a

FIND NO.	QTY REQD				PARTS LIST			
					PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1				REF	129331-15	PROM	M23	1
2				REF	129331-16	PROM	M24	1
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								

NOTES: 1. SEE SHEET 16 FOR PROM PLACEMENT

2. REMOVE ROM @ J25

Form # 10-1011a

OPTION 9	SIZE A	CODE IDENT 98438	129504	REV D
TITLE ESC TRANSMIT				
SHEET 1 OF 1	SCALE		SHEET 11	

BEND PIN 36 ON 1602 @ D1 OUT OF SOCKET

OPTION 10
TITLE 2 STOP BITS
SHEET 1 OF 1

SIZE	CODE IDENT		REV
A	98438	129504	B
SCALE		SHEET 12	

Form # 10-1011a

Fig No.	QTY REQD					PARTS LIST			
						PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1					1	800-A-6.912 MHz	CRYSTAL	STANDARD CRYSTAL	1,2,3
2									
3									
4									
5									
6									
7									
8									
9									
10									
11									
12									
13									

NOTES:

1. SWITCH POSITION #3 WILL PRODUCE 1800 BAUD
2. WITH CRYSTAL INSTALLED 1800 BAUD IS THE ONLY CORRECT FREQUENCY. ALL OTHER SWITCH POSITIONS ARE OFF FREQUENCY
3. PRINTER BAUD RATES ARE ALSO OFF FREQUENCY

OPTION 11
TITLE 1800 BAUD
SHEET 1 OF 1

SIZE	CODE IDENT		REV
A	98438	129504	B
SCALE		SHEET 13	

Form # 10-1011a

ITEM NO.	QTY REQD				PARTS LIST			
					PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1				1	128348-123	I.C.	A15	
2								
3				1	128349-157	CAP 150/3V	SPRAGUE	
4				1	128533-513	RES 51K		
5				1	IN914	DIODE		
6								
7								
8								
9								
10								
11								
12								
13								

OPTION 12

TITLE TIME OUT

SHEET 1 OF 1

SIZE	CODE IDENT		REV
A	98438	129504	B
SCALE		SHEET 14	

Form # 10-1011a

ITEM NO.	QTY REQD				PARTS LIST			
					PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1				REF	129331-11	PROM	M23	1
2				REF	129331-12	PROM	M24	1
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								

NOTES: 1. SEE SHEET 16 FOR PROM PLACEMENT
2. REMOVE ROM @ J25

OPTION 13
TITLE LOAD CURSOR MOD.
SHEET 1 OF 1

SIZE	CODE IDENT		REV
A	98438	129504	B
SCALE		SHEET 15	

Form # 10-1011a

ROM/PROM PLACEMENT

F/N	CONFIGURATION: STD.	STD w/OPT 1 AND/OR OPT 2	OPT. 9	OPT. 9 w/OPT. 1	OPT. 13	OPT. 13 w/OPT. 1	OPT. 13 w/OPT. 2	OPT. 13 w/OPT. 1 AND OPT. 2		PART NO.	LOC	PAGE
1	1	1								129309-01	J25	0-3
2		1								129309-07	J26	4-7
3												
4												
5					1	1	1	1		129331-11	M23	0-1
6					1	1	1	1		129331-12	M24	2-3
7				1		1		1		129331-13	M25	4-5
8							1	1		129331-14	M26	6-7
9			1	1						129331-15	M23	0-1
10			1	1						129331-16	M24	2-3

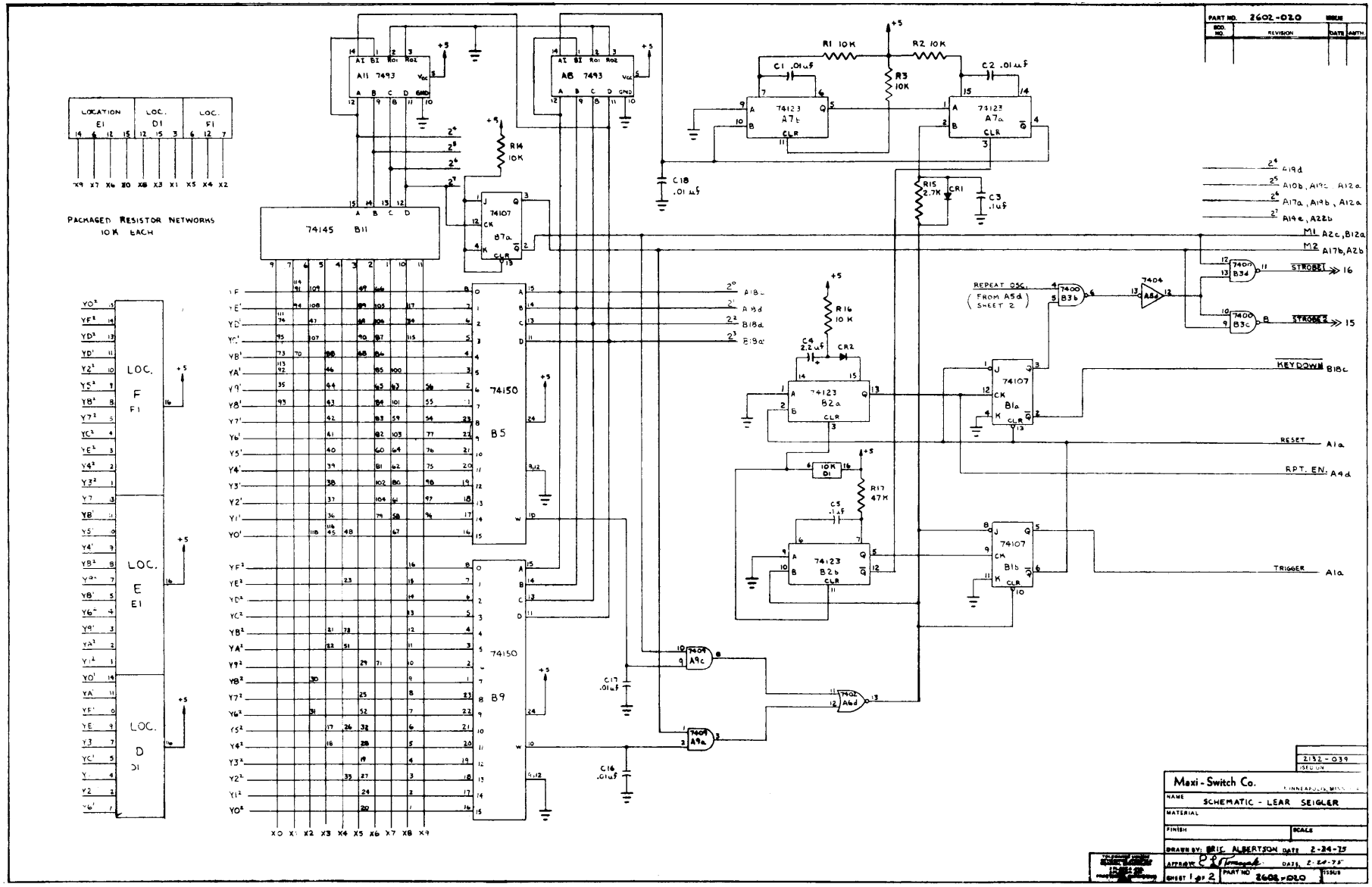
NOTE: 1. OPT's. 3, 4, 5, 7, 8, 10, 11, 12 NOT DEPENDENT ON ROM OR PROM

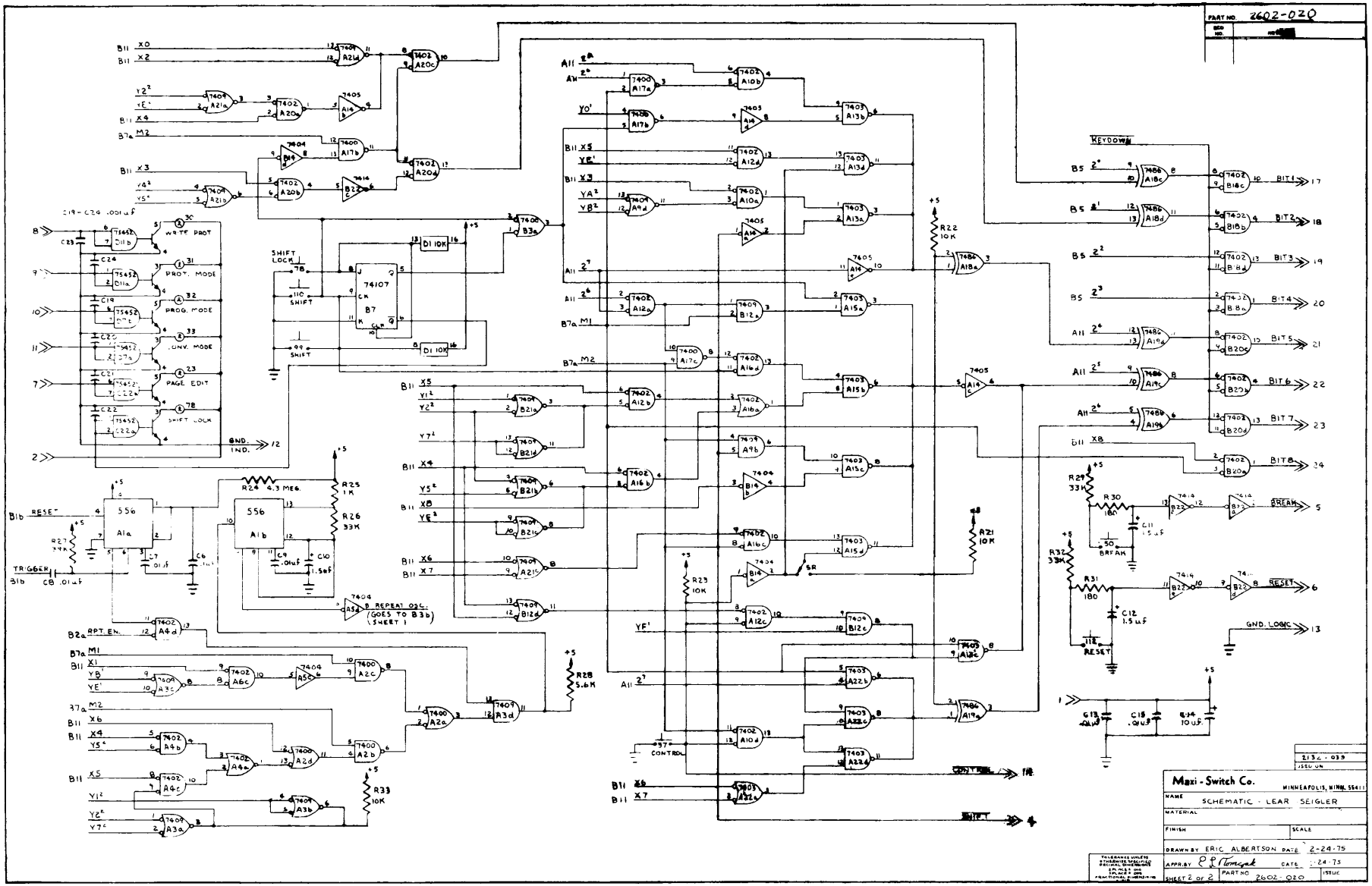
SIZE	CODE IDENT		REV
A	98438	129504	B
SCALE		SHEET 16	

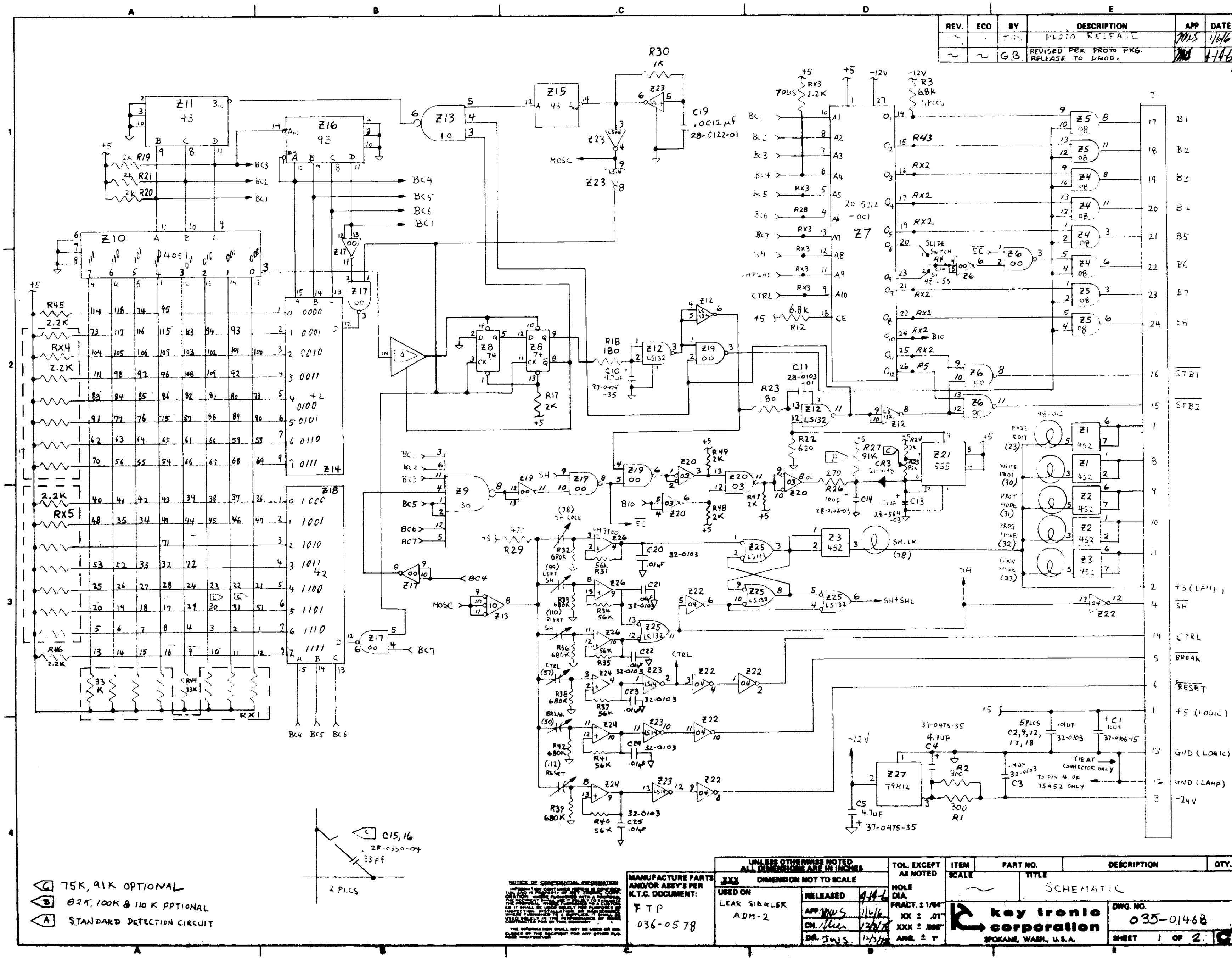
Form # 10-1011a

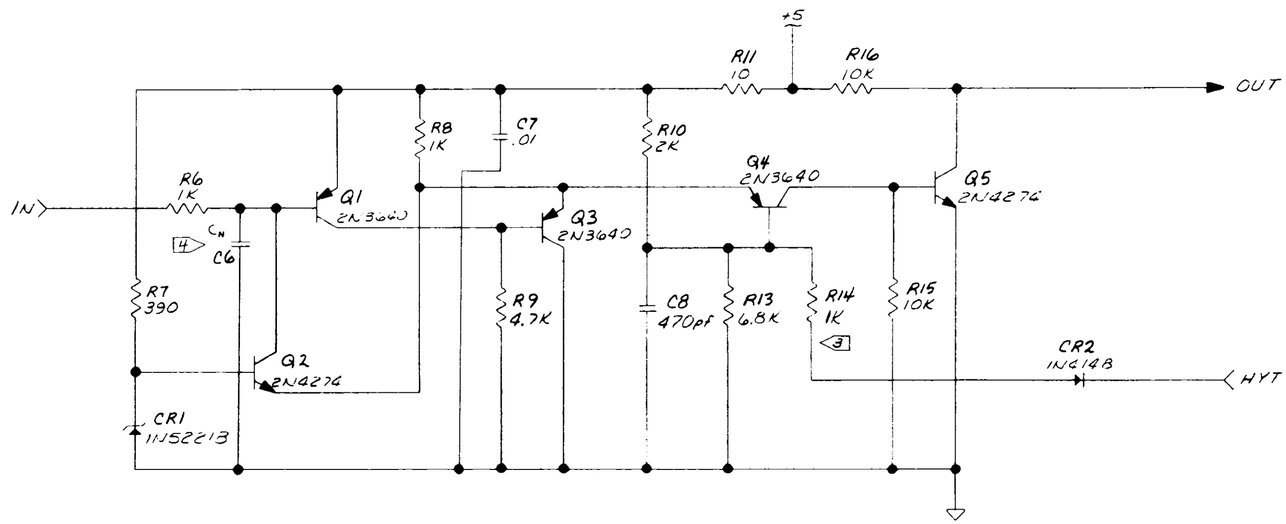
APPENDIX D: ADM-2 SUBASSEMBLIES

KEYBOARD


PART NO. 2602-020
REVISION
LOCATION E1
LOC. D1
LOC. F1
PACKAGED RESISTOR NETWORKS 10K EACH
74145 B11
74150 B5
74150 B9
74107 B7a
74123 A7b
74123 A7a
74123 B2a
74123 B2b
74107 B1a
74107 B1b
R1 10K
R2 10K
R3 10K
R14 10K
R15 2.7K
R16 10K
R17 47K
C1 .01uf
C2 .01uf
C3 .1uf
C4 2.2uf
C5 .1uf
C16 .01uf
C17 .01uf
C18 .01uf
CR1
CR2
REPEAT OSC. (FROM A5d SHEET 2)
KEYDOWN B1Bc
RESET A1a
RPT. EN. A4d
TRIGGER A1a
STROBE1 16
STROBE2 15
M1 A2c, B12a
M2 A17b, A2b
Maxi-Switch Co.
SCHEMATIC - LEAR SEIGLER
DRAWN BY: ERIC ALBERTSON DATE 2-24-75
SHEET 1 OF 2
PART NO 2602-020


PART NO. 2602-020
Maxi-Switch Co.
MINNEAPOLIS, MINN. 55411
NAME SCHEMATIC - LEAR SEIGLER
MATERIAL
FINISH
SCALE
DRAWN BY ERIC ALBERTSON DATE 2-24-75
APP'D BY DATE 2-24-75
SHEET 2 OF 2
PART NO. 2602-020
ISSUE
2132-033
KEYDOWN
WRITE PROT
PROT. MODE
PROG. MODE
CONV. MODE
PAGE EDIT
SHIFT LOCK
RESET
REPEAT OSC.
(GOES TO B3b SHEET 1)
RPT. EN.
SHIFT
CONTROL
BREAM
GND. LOGIC
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8


REV. ECO BY DESCRIPTION APP DATE
PROTO RELEASE
REVISED PER PROTO PKG. RELEASE TO PROD.
75K, 91K OPTIONAL
82K, 100K & 110K OPTIONAL
STANDARD DETECTION CIRCUIT
C15, 16
28-0350-04
33 pf
2 PLCS
MANUFACTURE PARTS AND/OR ASSY'S PER K.T.C. DOCUMENT:
FTP 036-0578
UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES
DIMENSION NOT TO SCALE
USED ON
LEAR SIEGLER ADM-2
RELEASED
TOL. EXCEPT AS NOTED
HOLE DIA.
FRACT. ± 1/64
ITEM PART NO. DESCRIPTION QTY.
SCALE
TITLE
SCHEMATIC
key tronic corporation
SPOKANE, WASH., U.S.A.
DWG. NO.
035-0146B
SHEET 1 OF 2
C



NOTE:
PROPRIETARY DOCUMENT
NOT TO BE DISCLOSED
TO UNAUTHORIZED PERSONS

4 ADD IF MATRIX IS NOISY; 100 pf NOMINAL
3 INCREASE VALUE IF KEY LOCKS UP
2. CAPACITOR VALUES IN uf
1. RESISTOR VALUES IN OHMS, ±5%, 1/4 W
NOTES-

DESCRIPTION
PROTO RELEASE
RELEASE TO PROD

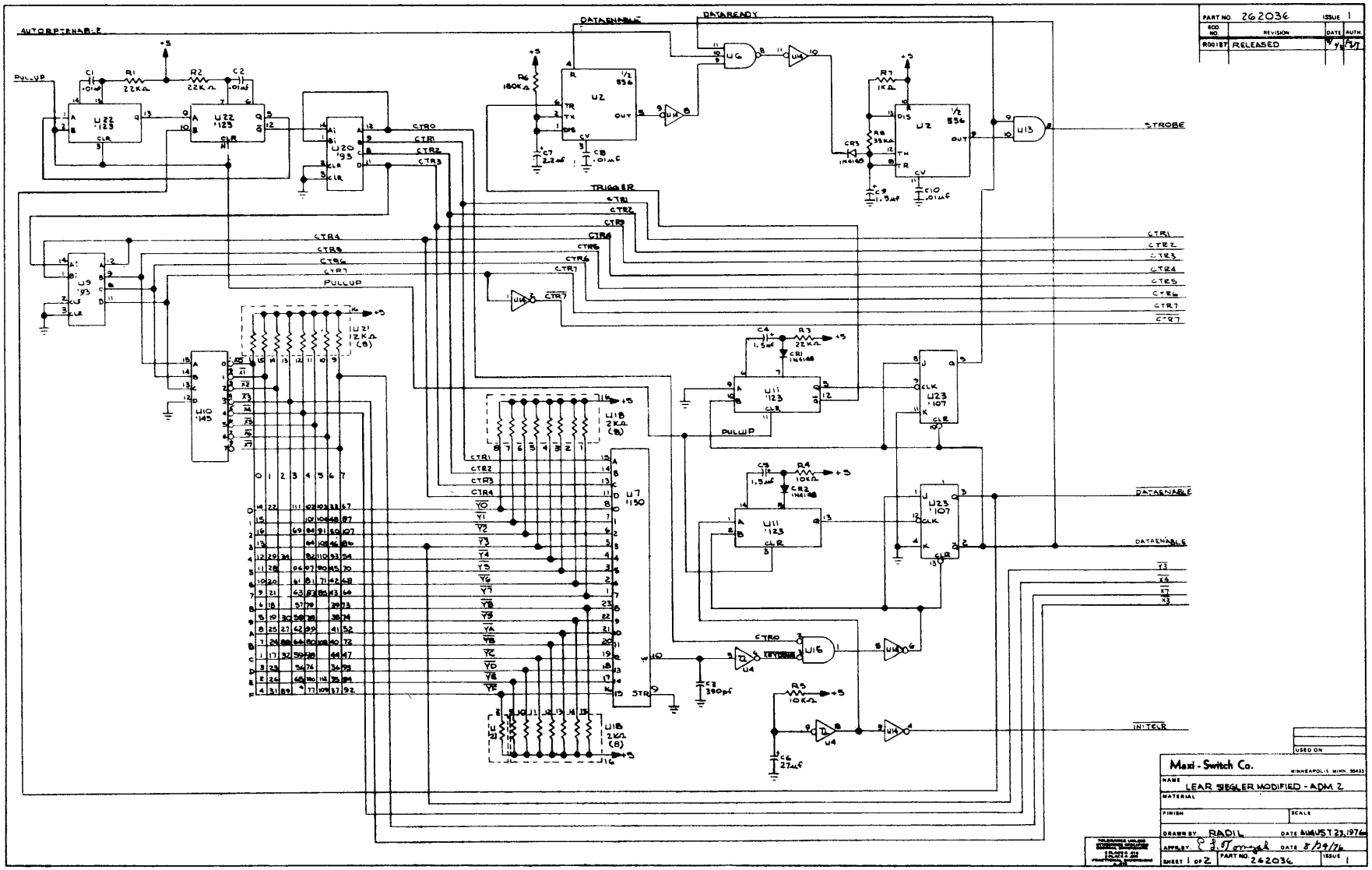
MANUFACTURE PARTS AND/OR ASSY'S PER K.T.C. DOCUMENT: 036-0578

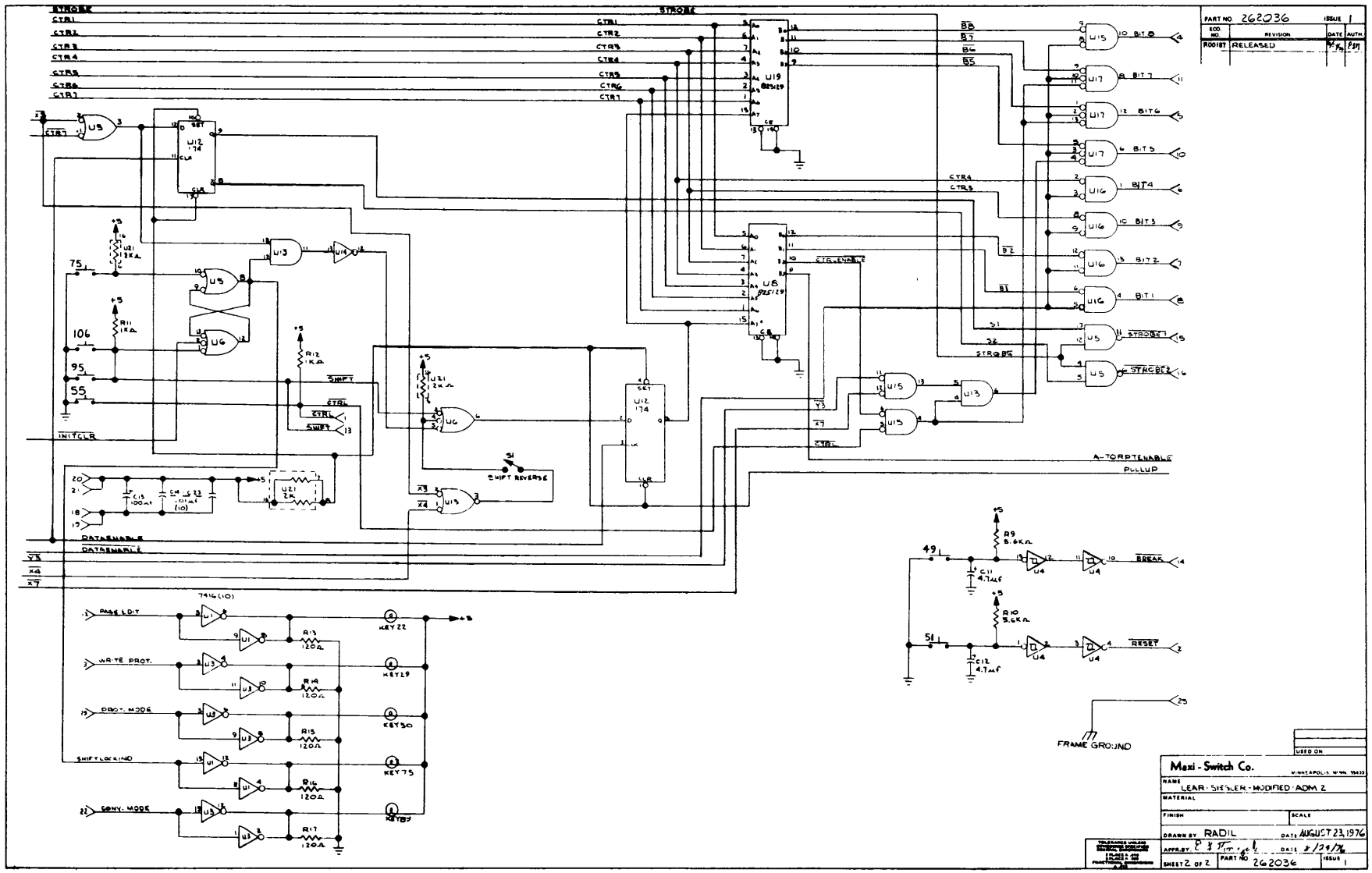
UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES
DIMENSION NOT TO SCALE

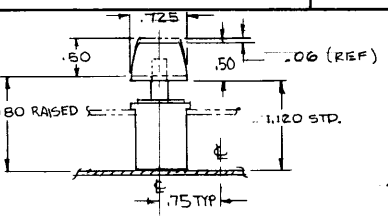
TITLE: SCHEMATIC

key tronic corporation
SPOKANE, WASH., U.S.A.

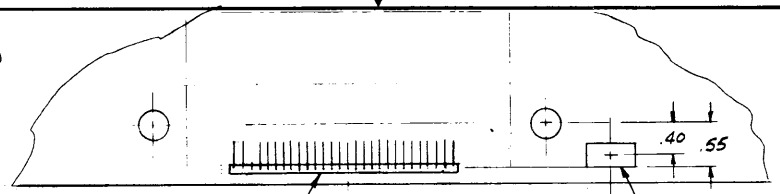
DWG. NO. 35-01468
SHEET 2 OF


AUTOREENABLE
PULLUP
DATAENABLE
DATAREADY
TRIGGER
STROBE
INITCLR
CTR0
CTR1
CTR2
CTR3
CTR4
CTR5
CTR6
CTR7
PART NO. 262036
ISSUE 1
REVISION
DATE
AUTH
R00187 RELEASED
Maxi-Switch Co.
MINNEAPOLIS, MINN. 55433
NAME LEAR SIEGLER MODIFIED - ADM 2
MATERIAL
FINISH
SCALE
DRAWN BY RADIL
DATE AUGUST 23, 1976
APP'D BY
DATE 8/24/76
SHEET 1 OF 2
PART NO. 262036
ISSUE 1
USED ON


STROBE
CTR1
CTR2
CTR3
CTR4
CTR5
CTR6
CTR7
INITCLR
DATAENABLE
A-TORPTENABLE
PULLUP
SHIFT REVERSE
FRAME GROUND
BIT 0
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
STROBE 1
STROBE 2
BREAK
RESET
PAGE EDIT
WRITE PROT.
PROT. MODE
SHIFT LOCK IND
SONY MODE
KEY 22
KEY 29
KEY 30
KEY 75
KEY 87
PART NO. 262036 ISSUE 1
ROOT87 RELEASED
Maxi-Switch Co.
NAME LEAR-SIEGLER-MODIFIED ADM 2
MATERIAL
FINISH
SCALE
DRAWN BY RADIL
DATE AUGUST 23, 1976
APP'D BY
DATE
SHEET 2 OF 2
PART NO 262036
ISSUE 1



TYP KEYBOARD SWITCH
SHOWING KEY HEIGHT & SIZE. (LENGTH OF KEYS & CORRESPONDING ℄ VARY, SEE PLAN VIEW

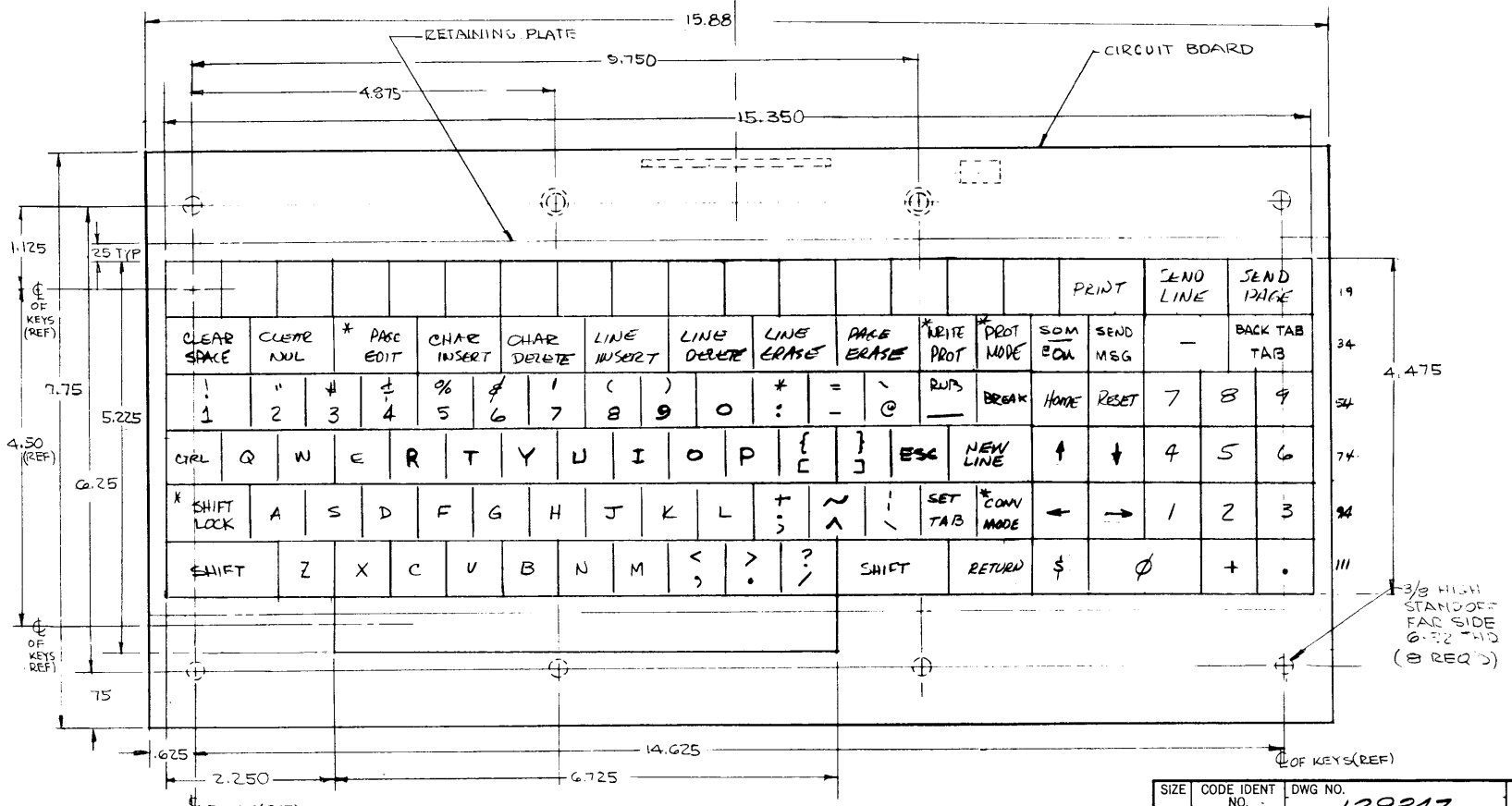


OUTPUT CONNECTOR
MOLEX PART NO.
22-05-2281
WITH PIN 26 REMOVED

SHIFT REVERSE FUNCTION SWITCH
ALCOSWITCH
PART NO. MSS-104DG-1

* INDICATES LIGHTED KEY.

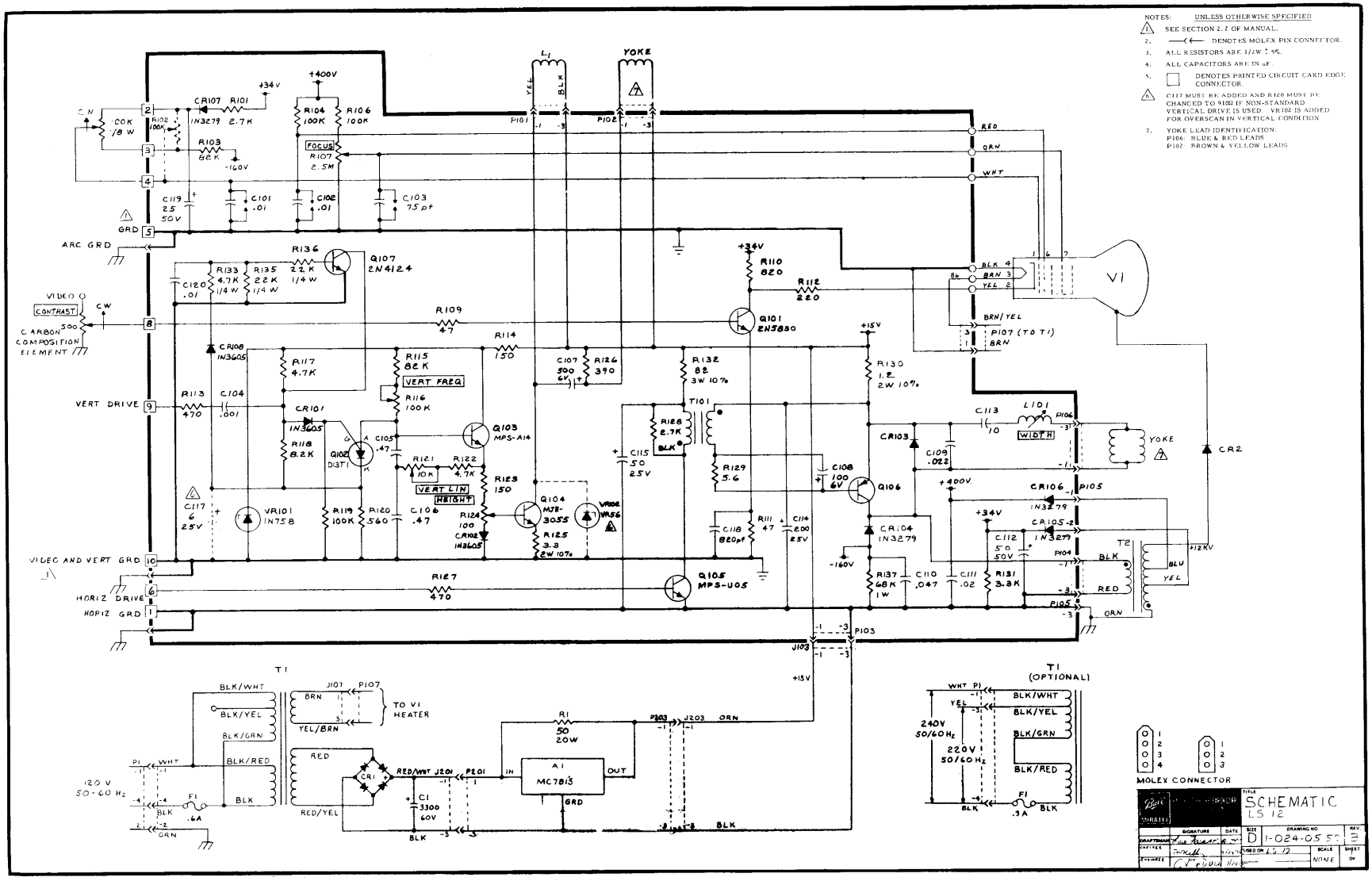
BOTTOM VIEW

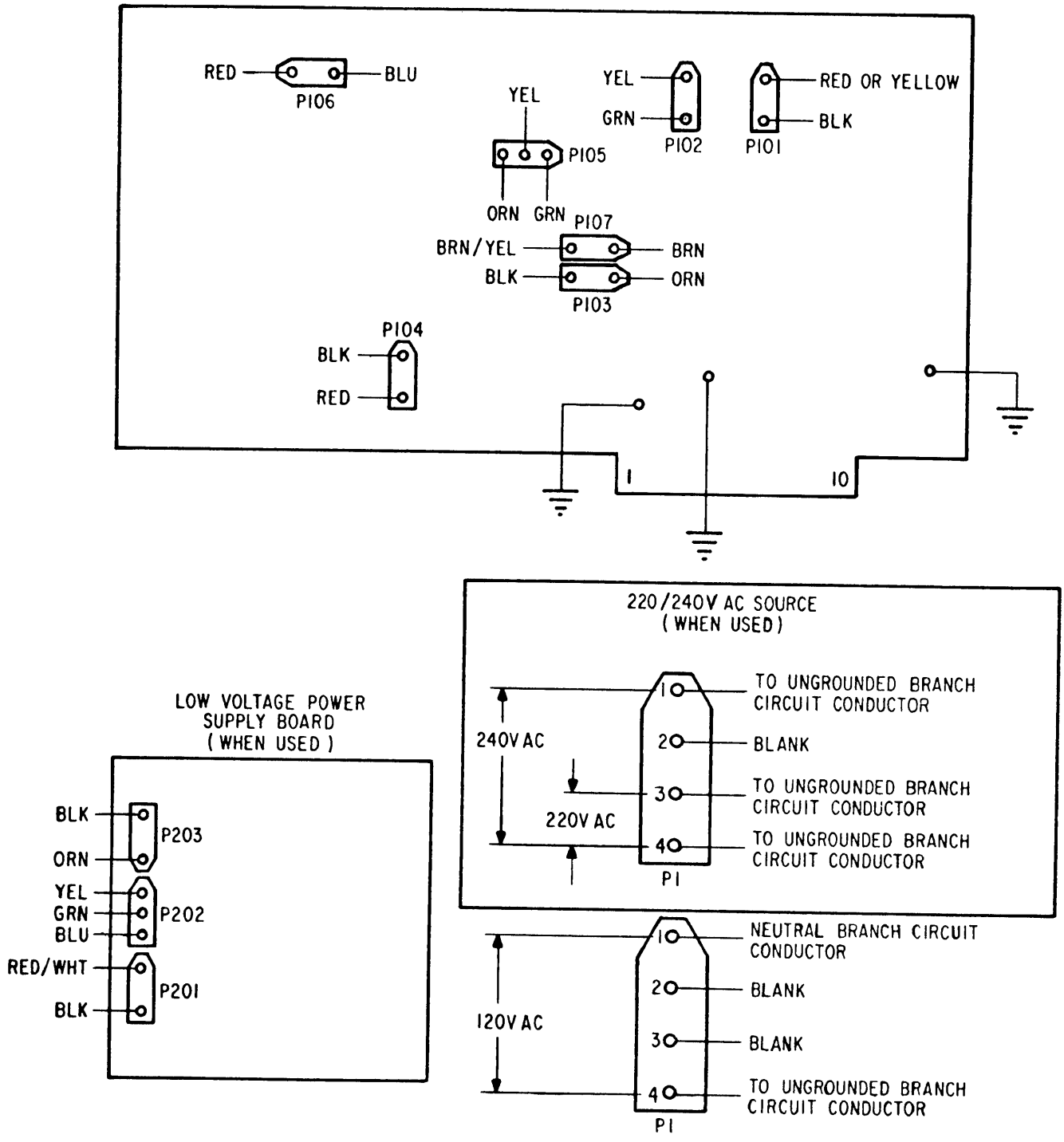


SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129347	
SCALE		SHEET 3	

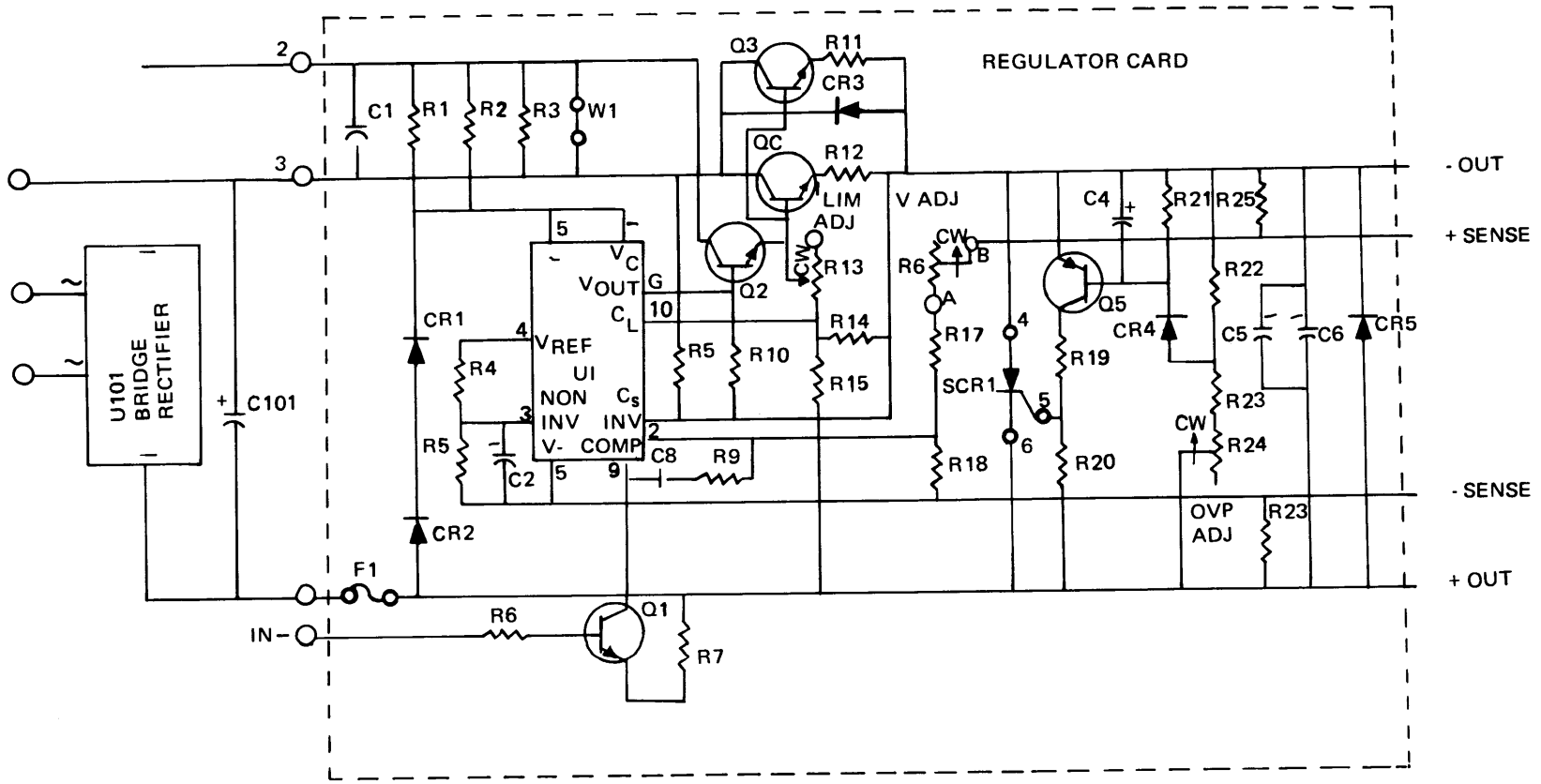
129347

MONITOR


NOTES: UNLESS OTHERWISE SPECIFIED
1. SEE SECTION 2.2 OF MANUAL.
2. DENOTES MOLEX PIN CONNECTOR.
3. ALL RESISTORS ARE 1/2W ± 5%.
4. ALL CAPACITORS ARE IN uF.
5. DENOTES PRINTED CIRCUIT CARD EDGE CONNECTOR.
6. C117 MUST BE ADDED AND R120 MUST BE CHANGED TO 910Ω IF NON-STANDARD VERTICAL DRIVE IS USED. VR102 IS ADDED FOR OVERSCAN IN VERTICAL CONDITION
7. YOKE LEAD IDENTIFICATION:
P106: BLUE & RED LEADS
P102: BROWN & YELLOW LEADS
+400V
+34V
+15V
-160V
YOKE
VIDEO CONTRAST
VERT DRIVE
HORIZ DRIVE
HOPIZ GRD
ARC GRD
VIDEO AND VERT GRD
FOCUS
VERT FREQ
VERT LIN HEIGHT
WIDTH
Q101 2N5830
Q102 D13T1
Q103 MPS-A14
Q104 MJE-3055
Q105 MPS-U05
Q106
Q107 2N4124
CR101 IN3605
CR102 IN3605
CR103
CR104 IN3279
CR105 IN3279
CR106 IN3279
CR2
VR101 IN758
VR102 VR56
T101
T2
T1
T1 (OPTIONAL)
TO V1 HEATER
120 V 50-60 Hz
240V 50/60 Hz
220V 50/60 Hz
MOLEX CONNECTOR
SCHEMATIC
LS 12
D
1-024-055
SCALE NONE


RED
BLU
P106
YEL
P105
ORN
GRN
YEL
GRN
P102
RED OR YELLOW
BLK
P101
P107
BRN/YEL
BRN
BLK
ORN
P103
P104
BLK
RED
1
10
220/240V AC SOURCE
(WHEN USED)
240V AC
220V AC
1
2
3
4
P1
TO UNGROUNDED BRANCH CIRCUIT CONDUCTOR
BLANK
TO UNGROUNDED BRANCH CIRCUIT CONDUCTOR
TO UNGROUNDED BRANCH CIRCUIT CONDUCTOR
LOW VOLTAGE POWER SUPPLY BOARD
(WHEN USED)
BLK
ORN
P203
YEL
GRN
BLU
P202
RED/WHT
BLK
P201
120V AC
1
2
3
4
P1
NEUTRAL BRANCH CIRCUIT CONDUCTOR
BLANK
BLANK
TO UNGROUNDED BRANCH CIRCUIT CONDUCTOR

POWER SUPPLY



MODEL 22D-100 SCHEMATIC

POWERTEC
AN AIRTRONICS SUBSIDIARY
9168 DESOTO AVENUE
CHATSWORTH CALIFORNIA 91311
(213) 882-0004 TWX 910-494-2092

SUB-MODULAR D.C. POWER SUPPLY

MODULE 22C-100

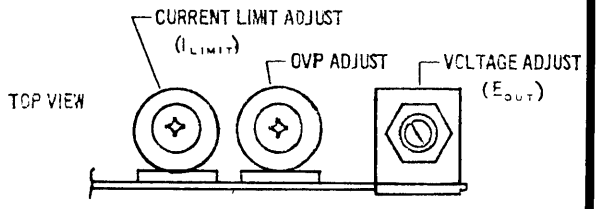
MODEL NUMBER–

ASSEMBLY NUMBER–

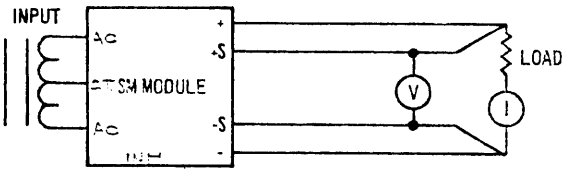
SPECIFICATIONS

WARNING: Requires power transformer to reduce line voltage to recommended input level.

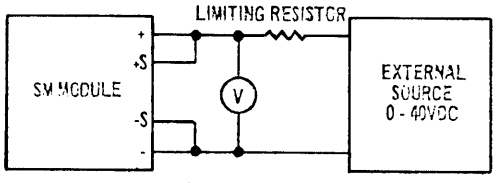
OUTPUT VOLTAGE	4.75V TO 7.0V
OUTPUT CURRENT	6.0A @ 5V – 5.2A @ 6V
LINE REGULATION	± .075%
LOAD REGULATION	± .075%
RIPPLE PEAK-PEAK	< 5MV
OVER CURRENT	50-130% OF FULL RATED LOAD
OVER VOLTAGE	105-135% OF RATINGS



POTIENTIOMETER LOCATION
FIGURE 1



CONNECTION DIAGRAM
FIGURE 2



OVP ADJUST SET-UP
FIGURE 3

ADJUSTMENT PROCEDURE

VOLTAGE ADJUST

Adjust output voltage to desired level at no load with unit connected as shown in figure 2. (Make sure OVP is in maximum clockwise position).

CURRENT LIMIT ADJUST

Adjust I_{LIMIT} to maximum clockwise position. Apply 125% of full load and adjust I_{LIMIT} until unit drops out of regulation 50 to 100mV.

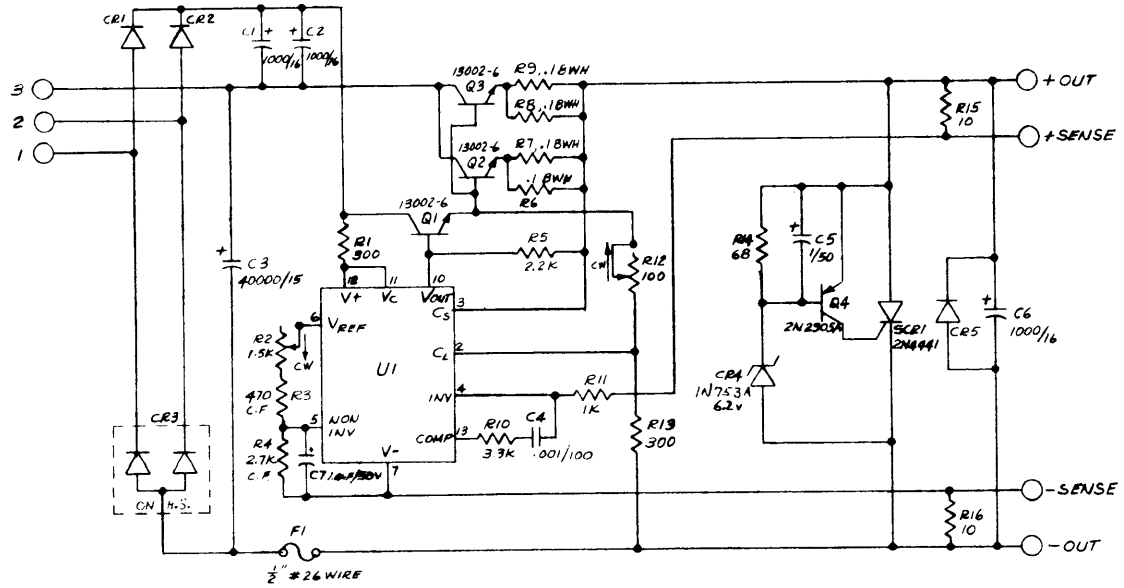
CAUTION: SO NOT RUN UNITS OVER 5 MINUTES WITH OUT ADDITIONAL HEAT SI NK

OVP ADJUST

Remove input power and load and apply an external voltage through a limiting resistor as shown in figure 3. Adjust OVP adjust until firing occurs at desired voltage as the external source is slowly increased. Select limiting resistor to limit current to 0.5ADC maximum after firing.

Refer to SM sales brochure PT3-9-72 for additional information and design parameters.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
A	PROD REL	9/24/74	
B	ECO# 015092	4/28/75	



COPY 20483 B

REFERENCE ONLY

QTY REQD	PART NO. OR TYPE DESIGNATION	SYM	NOMENCLATURE OR DESCRIPTION	CODE IDENT	MATERIAL, NOTES AND SPECIFICATIONS	ITEM NO.

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X ± .060
ANGLES X° ± 1°0' .XX ± .030
.X' ± 0'30' .XXX ± .010
DIM AND TOL PER MIL-STD-8
MACHINED DIA'S ON COMMON CENTER CONCENTRIC WITHIN .005 T.I.R.
125 MACHINED SURFACE ROUGHNESS PER MIL-STD-10
REMOVE BURRS, BREAK EDGES .010 MAX
DO NOT SCALE DRAWING
REPORT ERRORS TO ENGINEERING DEPT.
DO NOT MAKE CHANGES WITHOUT PROPER AUTHORIZATION

NEXT ASSY | FINAL ASSY
MATERIAL
FINISH

CONTRACT NO.

APPD		10/4/74
CHECK		8/26/74
DRAWN		8-22-74
APPROVED		
APPROVED		

POWERTEC DIVISION
AIRTRONICS INCORPORATED
9166 DEBOTO AVE., CHATSWORTH, CALIF. 91311

TITLE
SCHEMATIC —
8D406

SIZE	CODE IDENT NO.	DRAWING NUMBER	REV.
C	24429	20483	B

SCALE —
SHEET 1 OF 1

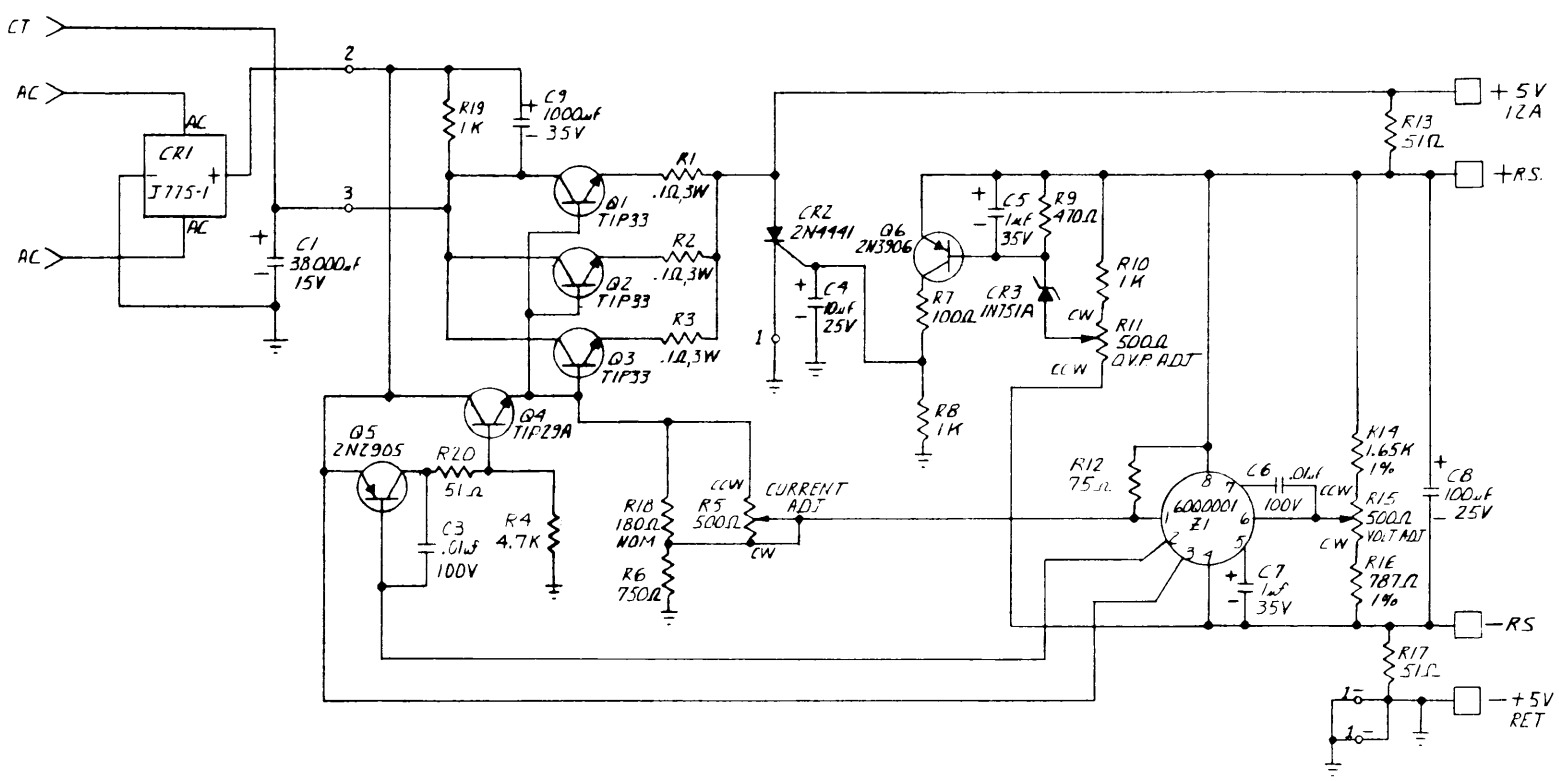
2. ALL CAPACITORS ARE IN MICROFARADS.
1. ALL RESISTOR VALUES ARE IN OHMS, ¼ WATT, ± 5%

NOTE: UNLESS OTHERWISE SPECIFIED

PART NUMBER AND INDENTURE	QUANTITY PER ASSY	DESCRIPTION	REMARKS
080-20478-001	1.	8D406 CUSTOM P/S	
081-20480-001	1.	ASSY PCB COMPONENT	A1
050-20479-001	1.	ASSY-HEATSINK BRKT	
010-19655-001	3.	TS NPN T03	Q1-3
011-19612-002	1.	DD 30A T03 CT	CR3
032-13035-001	1.	CAP 40000U/15V AE ST	C3
051-13175-005	1.	STRAP	
041-13285-010	1.	BRACKET	
051-13198-005	2.	SCREW 10-32X3/8 PPH	
051-13196-006	3.	SCREW 6-32X7/16 PPH	
051-13196-007	6.	SCREW MACH6-32 PN HD CAD 1/2	
051-13196-005	1.	SCREW 6-32X5/15 PPH	
051-13249-001	4.	MICA TSTR	
051-13066-002	1.	MICA SCR	
051-13278-001	4.	INSULATOR	
051-13196-003	5.	SCREW 6-32X1/4 PPH	
051-13240-004	2.	LUG SOLDER BRASS #5/16	
051-13199-002	2.	WASHER #6	
041-15132-007	.200 FT	TAPE INSULATION	
013-13015-001	1.	SCR 2N4441	SCR1
ECO-016073REV D	.REF		
081-20480-001	1.	ASSY PCB W/COMP	
055-20480-001	1.	ASSY PC B W/HDWR	

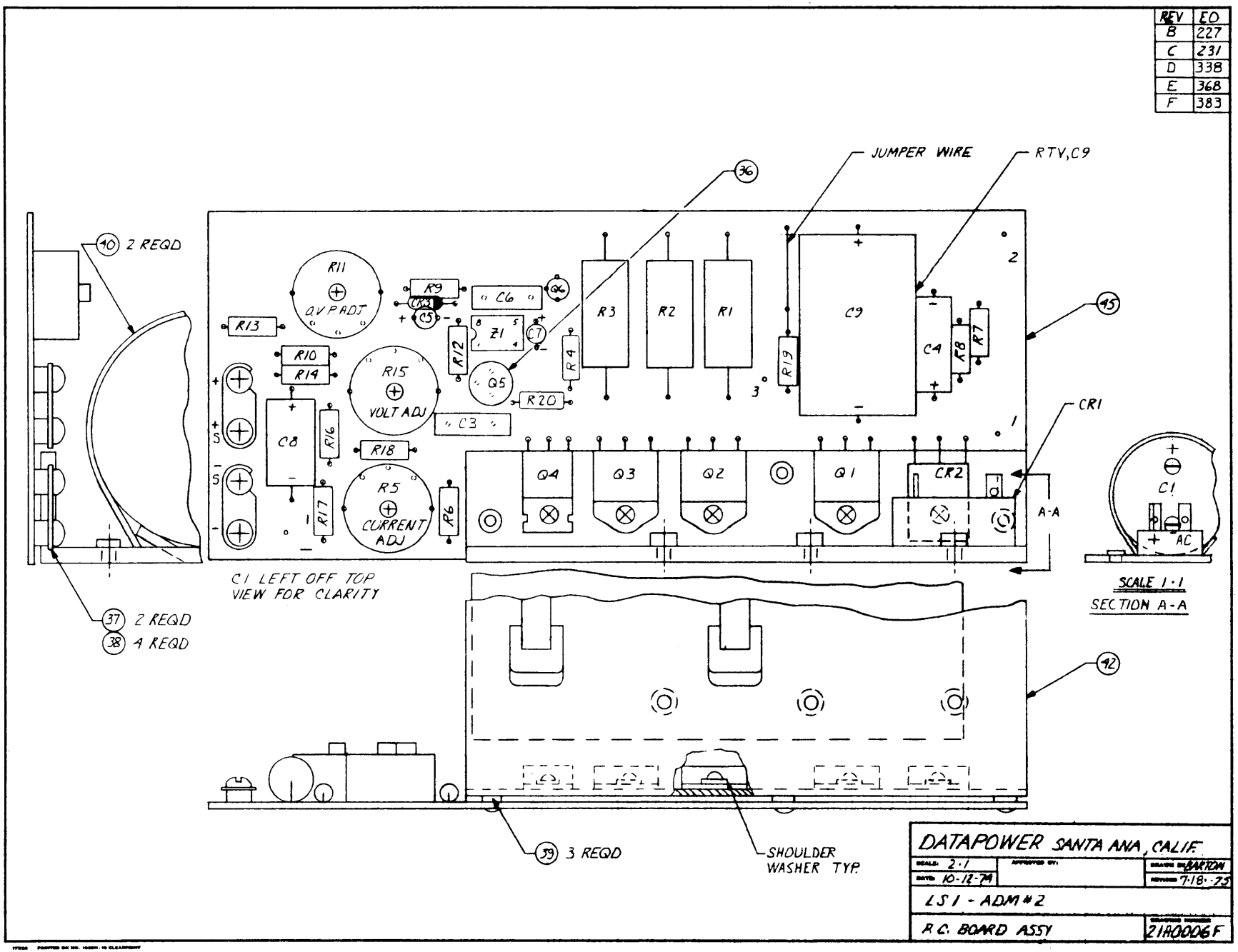
PART NUMBER AND INDENTURE	QUANTITY PER ASSY	DESCRIPTION	REMARKS
014-13034-003	1.	IC	U1
011-13009-003	3.	DD 1A D041 AL	CR1, 2, 5
012-16774-008	1.	ZD .4W D07 1N753A AL	CR4
010-13021-002	1.	TS PNP T05 2N2905A	Q4
032-13006-003	3.	CAP 1000U/15V AE BM	C1, 2, 6
031-13005-008	1.	CAP .002U/100V PF	C4
032-13006-001	1.	CAP 1U/50V AE BM	C5
020-13004-060	1.	RS 300 CC .5W 5% FL	R1
020-13004-058	1.	RS 240 CC .5W 5% FL	R13
020-13004-045	1.	RS 68 CC .5W 5% FL	R14
020-13004-081	1.	RS 2.2K CC .5W 5% FL	R5
020-13004-022	1.	RS 2.7 CC .5W 5% FL	R10
020-13004-025	2.	RS 10 CC .5W 5% FL	R15, 16
020-16046-065	1.	RS 470 CF .5W 2% AL	R3
020-16046-083	1.	RS 2.7K CF .5W 2% AL	R4
023-13016-008	1.	POT 1.5K BM 2W 20%	R2
023-13016-004	1.	POT 100 BM 2W 20%	R12
020-13023-073	1.	RS 1K CC .5W 5% AL	R11
024-13014-001	4.	RS .1 BWH 2W 10%	R6-9
052-13298-026	.050 FT	WIRE 26 GA	F1
051-19616-004	2.	WIRE JUMPER	W1, 2
032-13006-001	1.	CAP 1U/50V AE BM	C7
ECO-016073REV D	.REF		

REV	EO
B	227
C	338
D	368
E	383

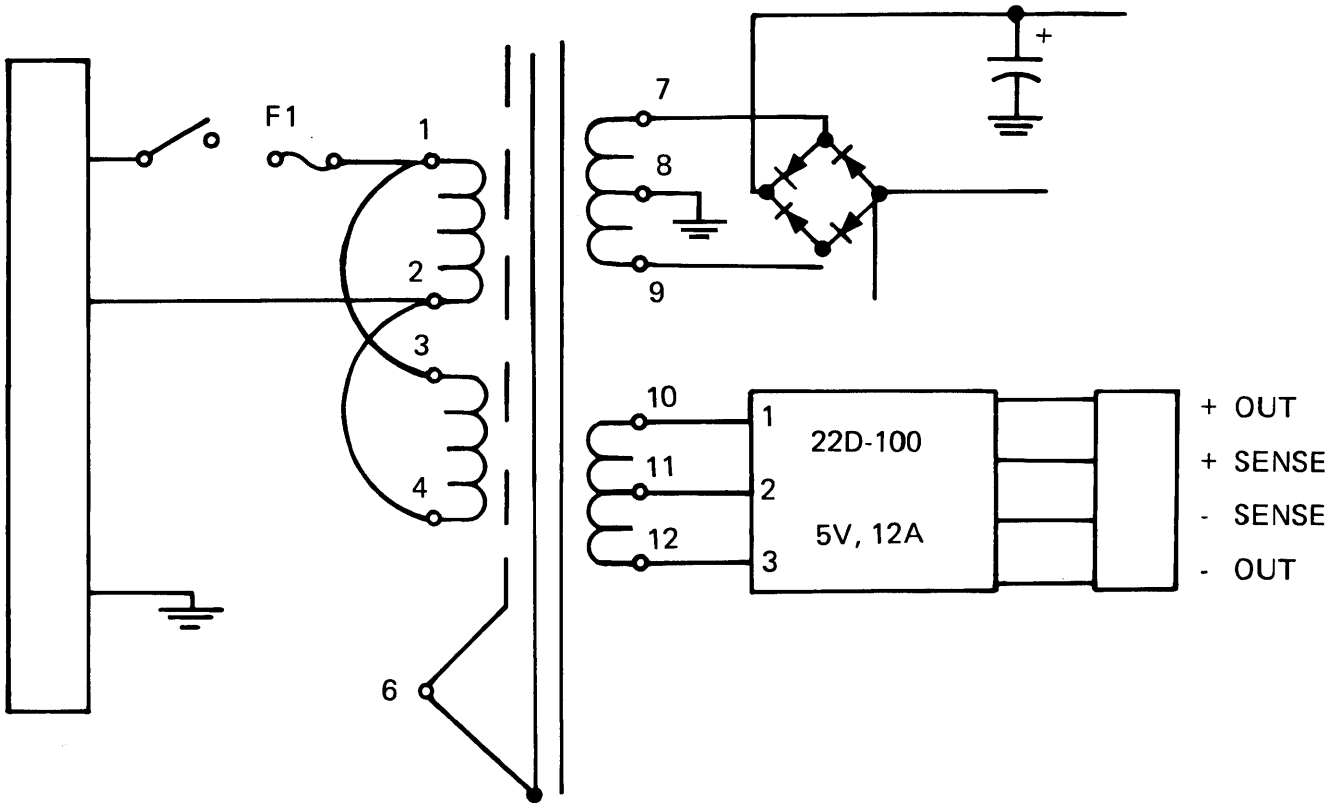


2 RXX INDICATES FACTORY SELECT.
1. ALL RESISTORS ARE 1/2 W 5%.
NOTE: UNLESS OTHERWISE SPECIFIED.

DATAPOWER SANTA ANA CALIF			
SCALE: ——	APPROVED BY:	DRAWN BY: E.C. ISLAS	
DATE: 8-29-74		REVISED 7-15-75	
L.S.I. 129398-11 ADM "2			
SCHEMATIC		DRAWING NUMBER 521A0006E	


REV | EO
B | 227
C | 231
D | 338
E | 368
F | 383
JUMPER WIRE
RTV, C9
36
45
92
10 2 REQD
37 2 REQD
38 4 REQD
39 3 REQD
SHOULDER WASHER TYP.
R11 O.V.P. ADJ
R15 VOLT ADJ
R5 CURRENT ADJ
R13
R10
R14
R9
CR3
C5
C6
Z1
C7
R12
Q5
R20
R4
C3
C8
R16
R18
R17
R6
R3
R2
R1
C9
C4
R8
R7
R19
Q4
Q3
Q2
Q1
CR2
CR1
C1 LEFT OFF TOP VIEW FOR CLARITY
A-A
C1
AC
SCALE 1·1
SECTION A-A
DATAPOWER SANTA ANA, CALIF.
SCALE: 2·1
DATE: 10-12-74
DRAWN BY: BARTON
REVISED: 7-18-75
LSI - ADM #2
P.C. BOARD ASSY
21A0006F

Qty.	Reference Designation	Description	Vendor/Part No.	Datapower Part No.
3	R13, 17, 20	RESISTOR, 51Ω, 1/2W, 5%	CARBON COMP	13R0510
1	R7	RESISTOR, 100Ω, 1/2W, 5%	CARBON COMP	13R0101
1	R12	RESISTOR, 75Ω, 1/2W, 5%	CARBON COMP	13R0750
1	R9	RESISTOR, 470Ω, 1/2W, 5%	CARBON COMP	13R0471
1	R6	RESISTOR, 750Ω, 1/2W, 5%	CARBON COMP	13R0751
3	R8, 10, 19	RESISTOR, 1K, 1/2W, 5%	CARBON COMP	13R0102
1	R4	RESISTOR, 4.7K, 1/2W, 5%	CARBON COMP	13R0472
1	R14	RESISTOR, 1.65K, 1/4W, 1%	RN60D	42R1651
1	R16	RESISTOR, 787Ω, 1/4W, 1%	RN60D	42R7870
3	R1-3	RESISTOR, .1Ω, 3W, 10%	IRC PW-3	56R0109
1	R18	RESISTOR NOM. 180ℓ, 1/2W, 5%	CARBON COMP	13R0181
3	R5, 11, 15	POT 500Ω	CTS 115R501A	74R0501
1	C9	CAPACITOR 1000uf 35V	MALLORY TCW102 TO 35N1F3P	35C0015
2	C6, 3	CAPACITOR .01uf 100V	SPRAGUE 225P10391WD3	11C0001
2	C5, 7	CAPACITOR 1uf 35V	ITT 4321216110	26C0002
1	C4	CAPACITOR 10uf 25V	SPRAGUE WHiiD1066025A	35C0002
1	C8	CAPACITOR 100uf 25V	SPRAGUE WH11D107G025E	35C0004
1	C1	CAPACITOR 38,000uf 15V (2" DIA X 3-1/8 LONG)	CALLINS 19-65CES-38000-15-I	30C0026
1	CR1	DIODE 25A 100V	J775-1	17D0002
1	CR2	DIODE SCR 8A 50V	2N4441	14D0002
1	CR3	DIODE 5.1V 5%	1N751A	12D0003
3	Q1-3	TRANSISTOR	T1P33	15Q0011
1	Q4	TRANSISTOR	T1P29A	15Q0003
1	Q5	TRANSISTOR	2N2905	14Q0001
1	Q6	TRANSISTOR	2N3906	12Q0001
1	Z1	I.C. REGULATOR	DATAPOWER	60Q0001
1		TRANSISTOR PADS T0-5	McNABB 400003	00Q0003
2		SHORTING BAR	H.H. SMITH 878	00E0007
4		SPACER	USECO #1530-B-1/8	35H0016
3		1/32 WASHER	SEASTROM 5602-18-32	84H0002
2		TIE WRAP	PANDUIT SST-4SM	00W0009
1		BRACKET-HEATSINK	DATAPOWER	15N0040
1		P.C. BOARD	DATAPOWER	D41P0003
	REF	TRANSFORMER	DATAPOWER	12T00012



VAC IN	T1 JUMP	APPLY POWER	F1
115	1-3, 2-4	1-2	3A
230	2-3	1-4	1.5A

B20117

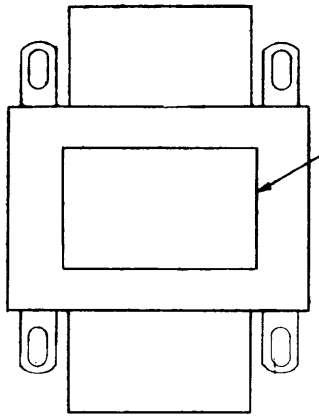
115/230 VAC + 15%
- 10%

47-63 Hz

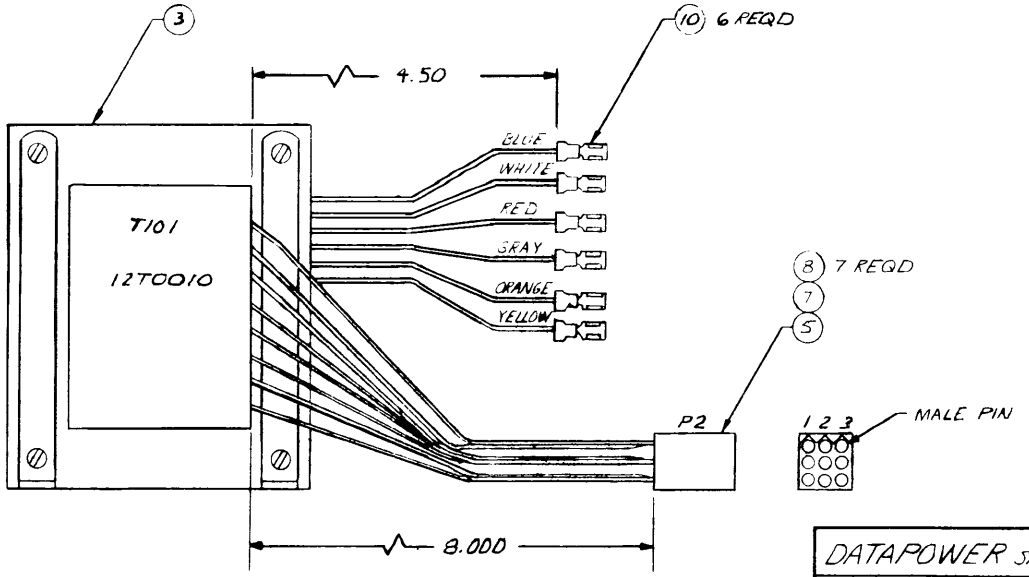
10 KG MAX

WIRING DIAGRAM PK1112

REV	ECO
A	186



PLACE NAME TAG APPROX.
WHERE SHOWN

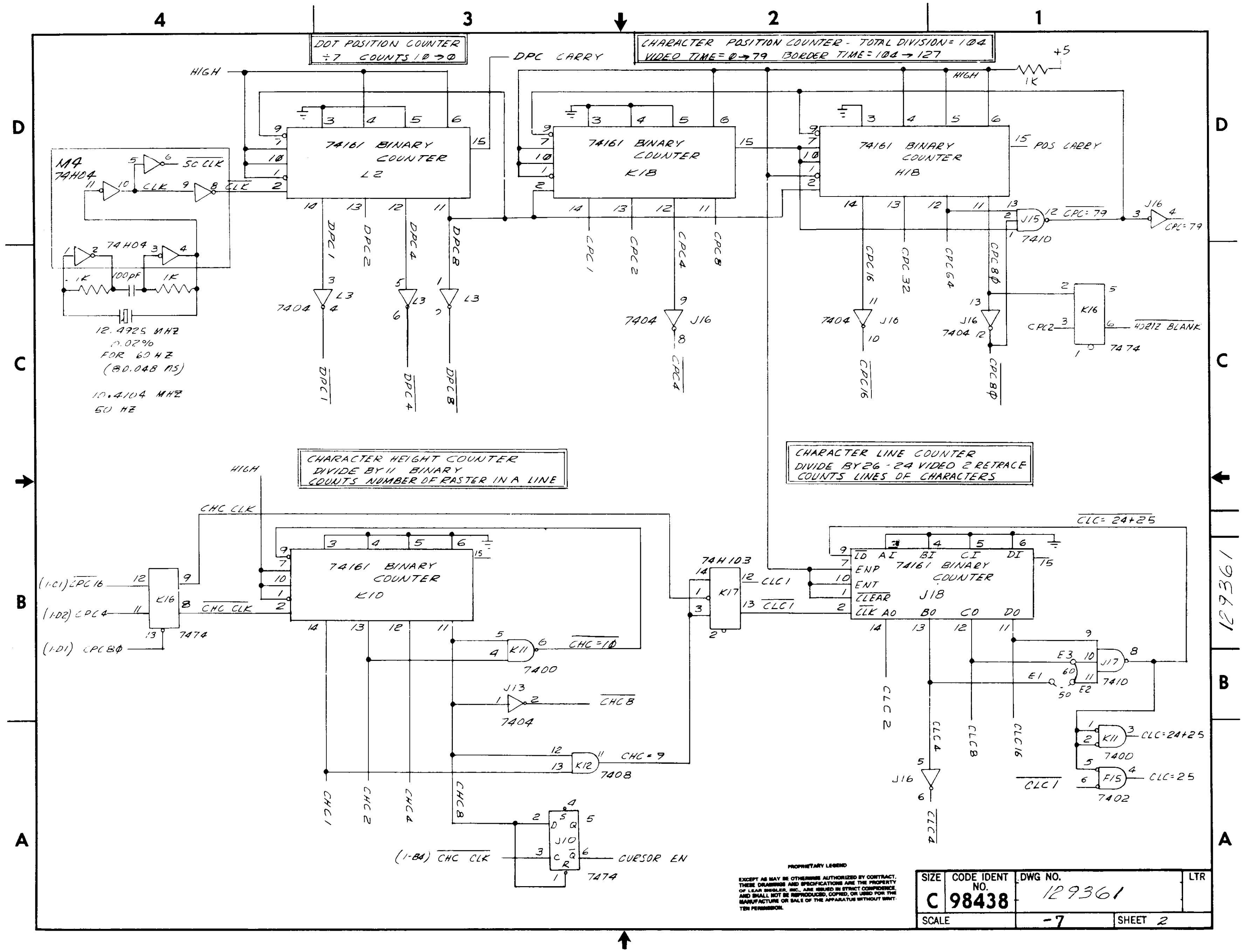


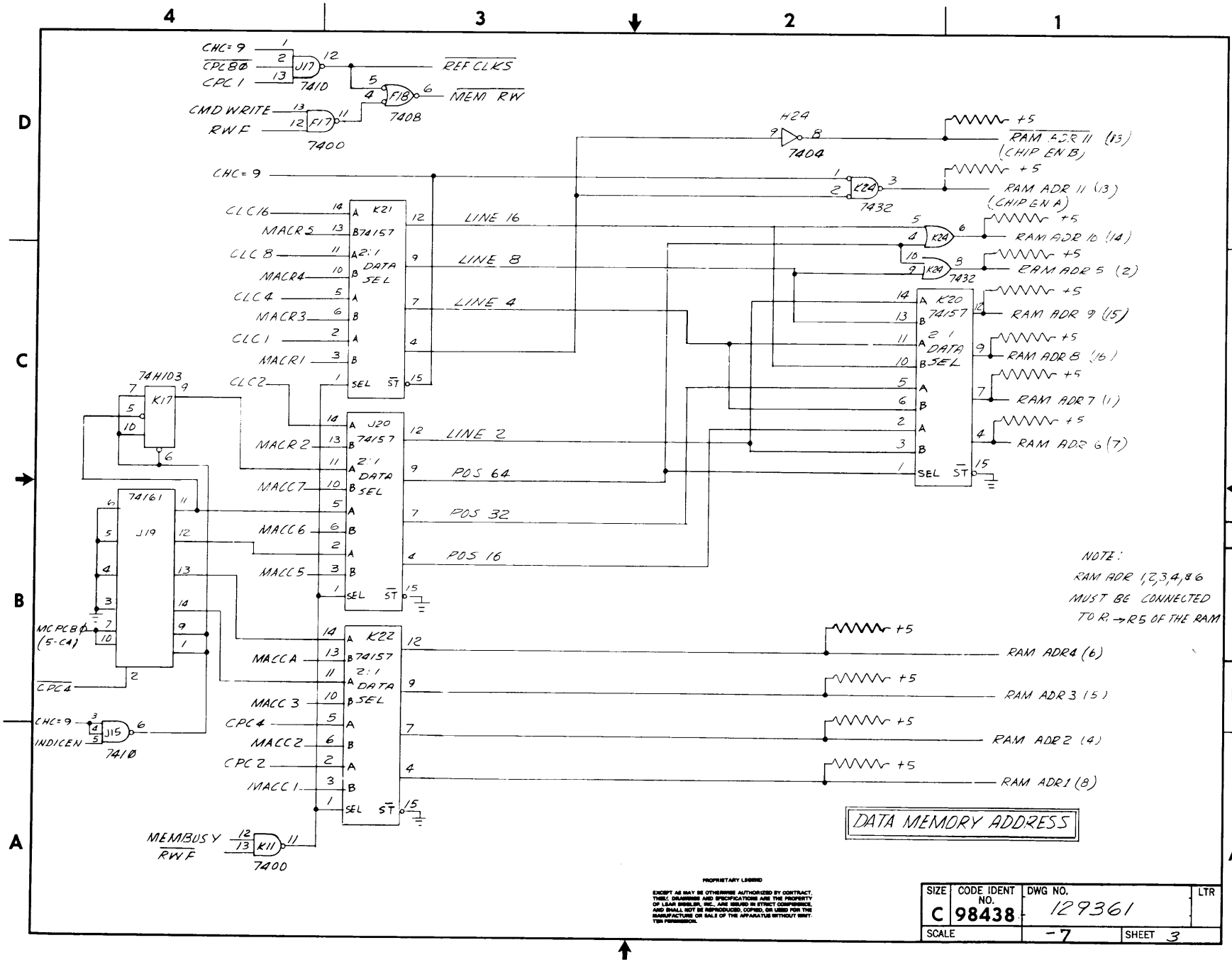
2. SEE S21A0009 FOR WIRING DIAGRAM
1. ALL DIMENSIONS ARE IN INCHES
NOTE: UNLESS OTHERWISE SPECIFIED

DATAPOWER SANTA ANA, CALIF.

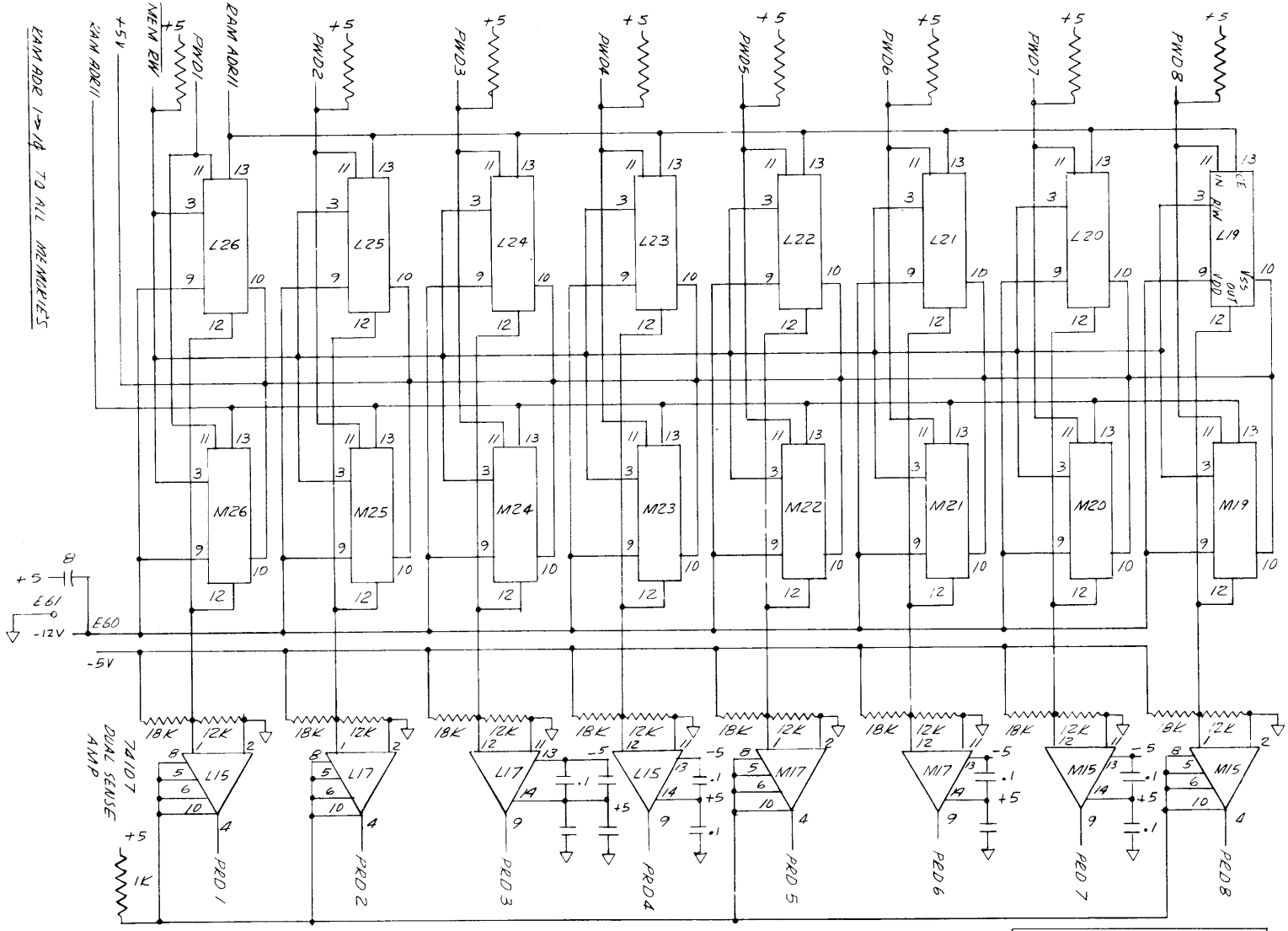
SCALE: 1-1	APPROVED BY:	DRAWN BY BARTON
DATE: 4.22.74		REVISED 9 5-74
LSI		
TRANSFORMER ASSY		DRAWING NUMBER 21A0004-1A

APPENDIX E: ADM-2 LOGIC DRAWINGS – -7, -13

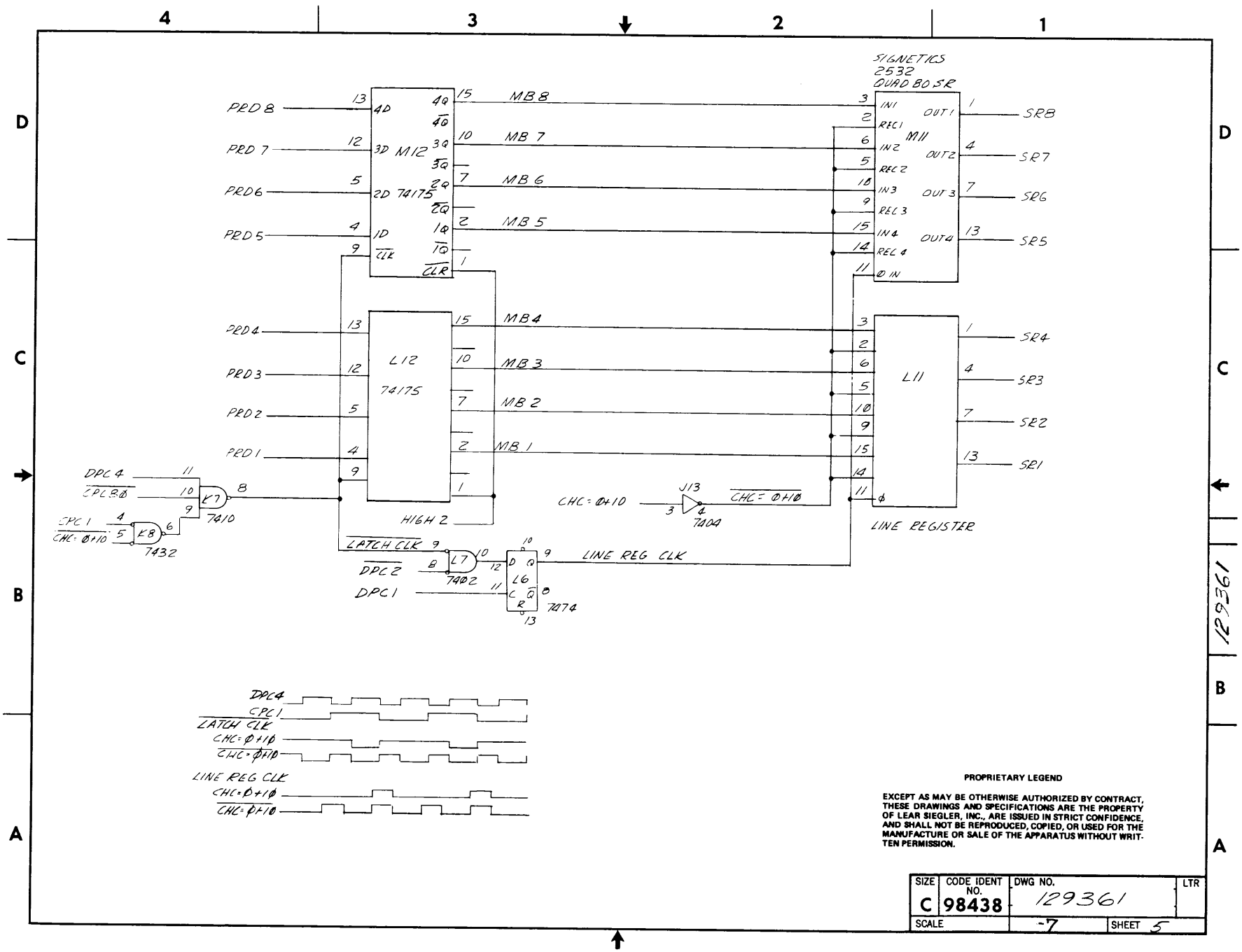

DOT POSITION COUNTER
÷7 COUNTS 10 → 0
DPC CARRY
CHARACTER POSITION COUNTER - TOTAL DIVISION = 104
VIDEO TIME = 0 → 79 BORDER TIME = 104 → 127
HIGH
+5
1K
74161 BINARY COUNTER L2
74161 BINARY COUNTER K18
74161 BINARY COUNTER H18
POS CARRY
M4 74H04
SC CLK
CLK
74H04
100pF
1K
12.4725 MHZ
.02%
FOR 60 HZ
(80.048 nS)
10.4104 MHZ
50 HZ
DPC1 DPC2 DPC4 DPC8
7404 L3
CPC1 CPC2 CPC4 CPC8
7404 J16
CPC16 CPC32 CPC64 CPC80
CPC=79
J15 7410
J16
K16
CPC2
40212 BLANK
7474
CHARACTER HEIGHT COUNTER
DIVIDE BY 11 BINARY
COUNTS NUMBER OF RASTER IN A LINE
CHARACTER LINE COUNTER
DIVIDE BY 26 - 24 VIDEO 2 RETRACE
COUNTS LINES OF CHARACTERS
CHC CLK
(1-C1) CPC16
(1-D2) CPC4
(1-D1) CPC80
74161 BINARY COUNTER K10
K11 7400
CHC=10
J13 7404
CHC8
CHC=9
K12 7408
CHC1 CHC2 CHC4 CHC8
J10 7474
(1-B4) CHC CLK
CURSOR EN
74H103 K17
CLC1
CLC=24+25
LD AI BI CI DI
ENP ENT CLEAR CLK A0 B0 C0 D0
74161 BINARY COUNTER J18
E3 E1 E2
J17 7410
CLC2 CLC4 CLC8 CLC16
J16
K11 7400
CLC=24+25
F15 7402
CLC=25
PROPRIETARY LEGEND
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE
-7
SHEET 2
129361



SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE	-7	SHEET 3	



SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE	-7	SHEET 4	



PROPRIETARY LEGEND

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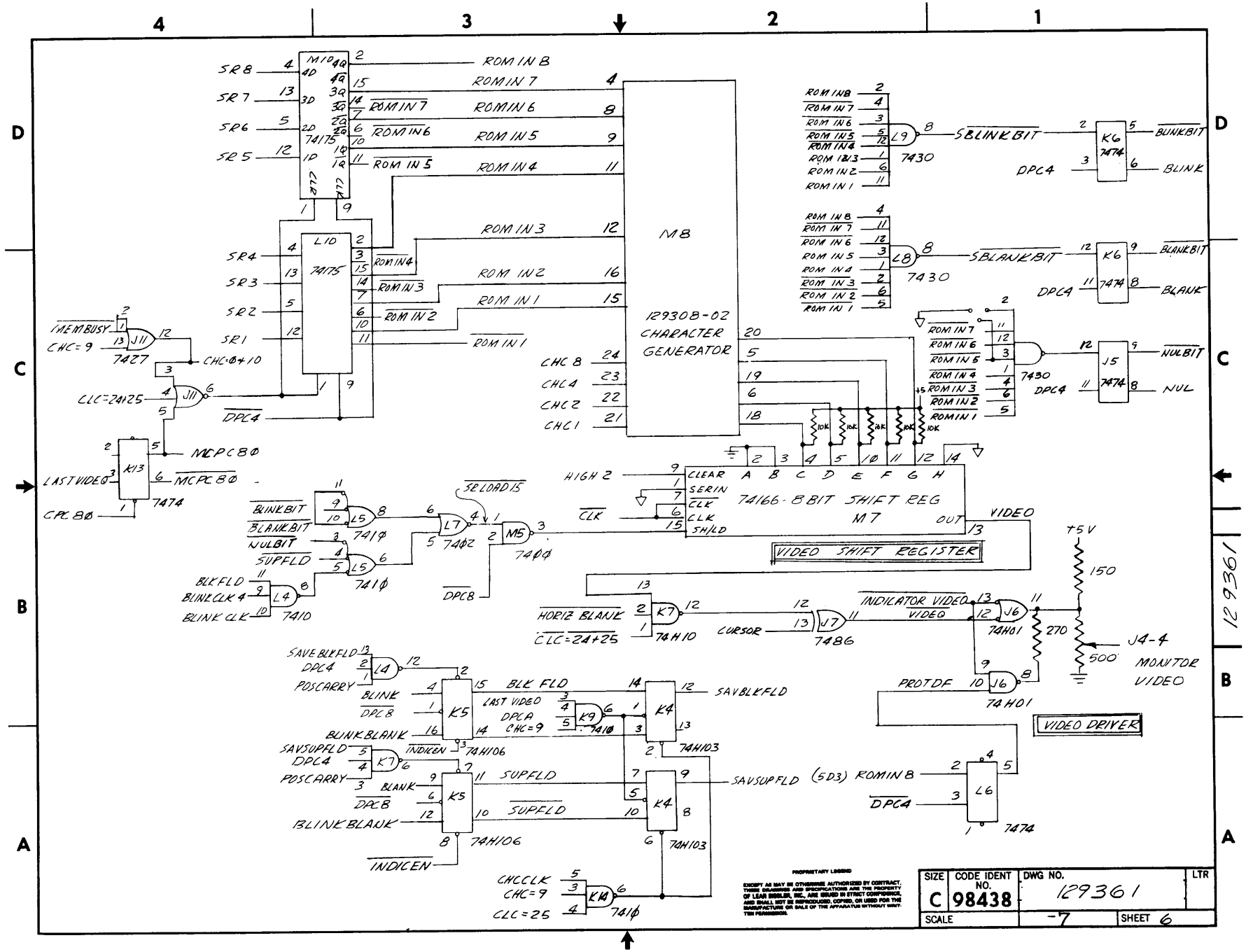
SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE	-7	SHEET 5	

129361


4
3
2
1
D
C
B
A
M10
74175
L10
74175
M8
129308-02
CHARACTER
GENERATOR
SR8
SR7
SR6
SR5
SR4
SR3
SR2
SR1
ROM IN 8
ROM IN 7
ROM IN 6
ROM IN 5
ROM IN 4
ROM IN 3
ROM IN 2
ROM IN 1
CHC 8
CHC 4
CHC 2
CHC 1
MEMBUSY
CHC=9
7427
CHC=8+10
CLC=24+25
DPC4
MCPC80
LAST VIDEO
K13
7474
CPC 80
BLINKBIT
BLANKBIT
NULBIT
SUPFLD
L5
7410
L7
7402
M5
7400
SR LOAD 15
DPC8
BLKFLD
BLINK CLK 4
BLINK CLK
L4
7410
HIGH 2
CLEAR
SERIN
CLK
SH/LD
74166-8 BIT SHIFT REG
M7
OUT
VIDEO
VIDEO SHIFT REGISTER
HORIZ BLANK
CLC=24+25
K7
74H10
CURSOR
J7
7486
INDICATOR VIDEO
VIDEO
J6
74H01
PROTDF
+5V
150
270
500
J4-4
MONITOR
VIDEO
VIDEO DRIVER
SAVE BLKFLD
DPC4
POSCARRY
BLINK
DPC8
BLINK BLANK
BLK FLD
LAST VIDEO
DPCA
CHC=9
K5
74H106
K4
74H103
SAVBLKFLD
SAVSUPFLD
INDICEN
SUPFLD
(5D3) ROMIN8
L6
7474
CHCCLK
CLC=25
K14
7410
L9
7430
SBLINKBIT
K6
7474
BLINK
L8
7430
SBLANKBIT
BLANK
L7
7430
NULBIT
J5
7474
NUL
10K
+5
PROPRIETARY LEGEND
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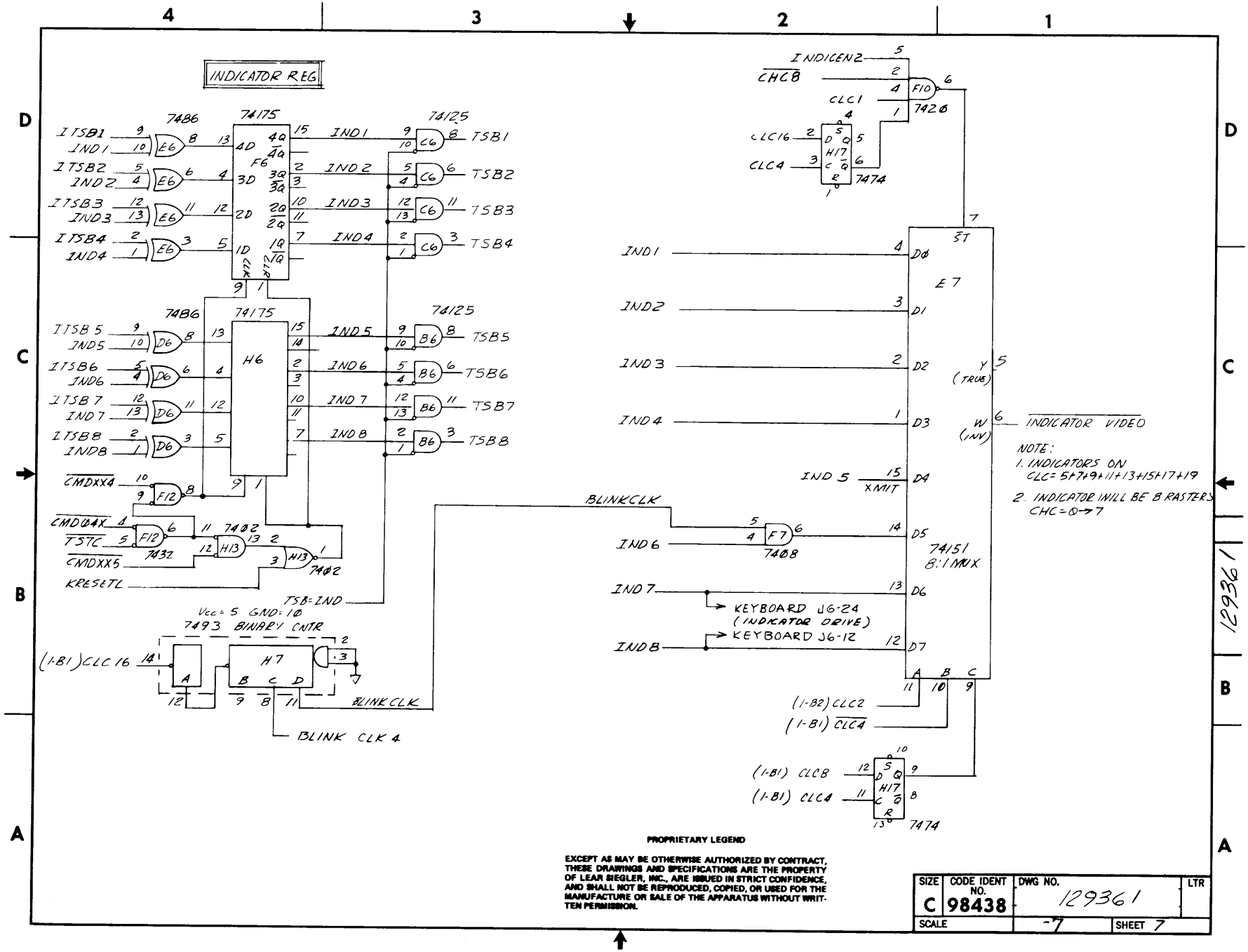
SIZE
C
CODE IDENT NO.
98438
DWG NO.
129361
LTR
SCALE
-7
SHEET 6


INDICATOR REG
7486
74175
74125
ITSB1
IND1
TSB1
ITSB2
IND2
TSB2
ITSB3
IND3
TSB3
ITSB4
IND4
TSB4
ITSB 5
IND5
TSB5
ITSB6
IND6
TSB6
ITSB 7
IND7
TSB7
ITSB8
IND8
TSB8
H6
F6
CMDXX4
CMDQ4X
FSTC
CMDXX5
KRESETL
7432
7402
TSB=IND
Vcc = 5 GND = 10
7493 BINARY CNTR
(1-B1) CLC 16
H7
BLINK CLK
BLINK CLK 4
INDICEN2
CHCB
CLC1
7420
CLC16
CLC4
7474
BLINKCLK
7408
74151
8:1 MUX
E7
INDICATOR VIDEO
NOTE:
1. INDICATORS ON
CLC= 5+7+9+11+13+15+17+19
2. INDICATOR WILL BE 8 RASTERS
CHC = 0 → 7
(1-B2) CLC2
(1-B1) CLC4
(1-B1) CLC8
PROPRIETARY LEGEND
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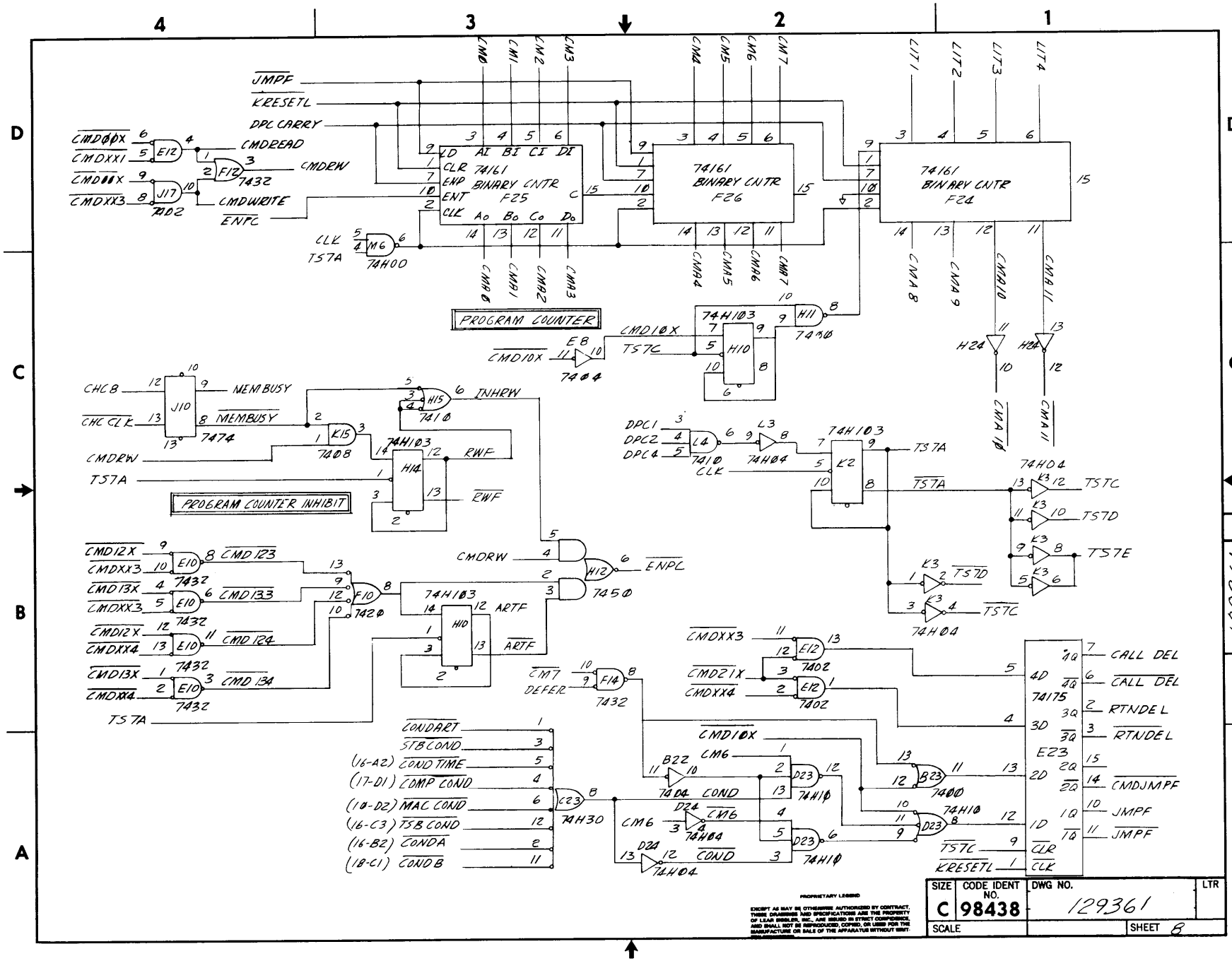
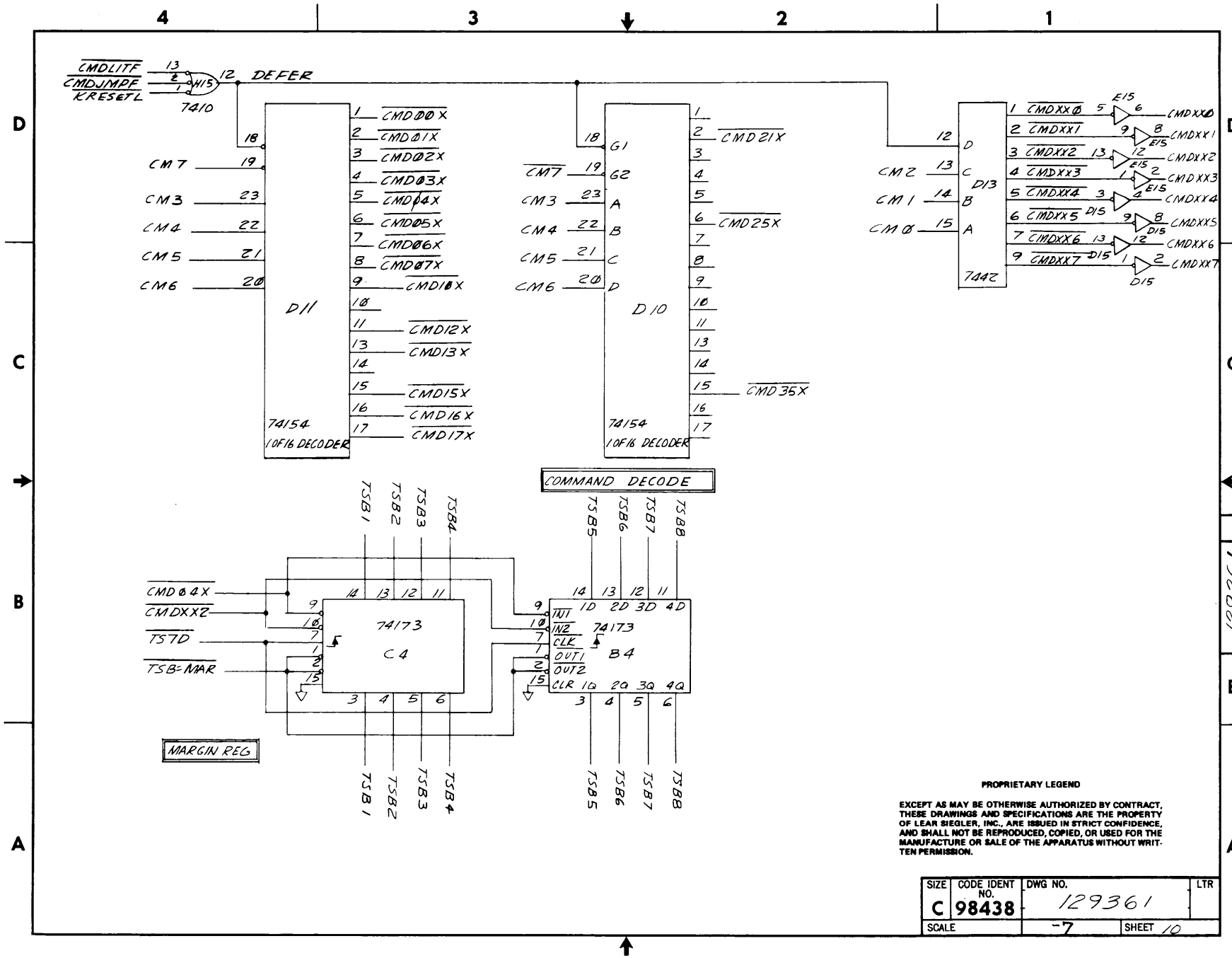
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE
SHEET 7


PROGRAM COUNTER
PROGRAM COUNTER INHIBIT
74161 BINARY CNTR F25
74161 BINARY CNTR F26
74161 BINARY CNTR F24
74H103
74175
E23
JMPF
KRESETL
DPC CARRY
CMDREAD
CMDRW
CMDWRITE
ENPC
CLK
TS7A
MEMBUSY
INHRW
RWF
ARTF
CMD123
CMD133
CMD124
CMD134
CONDART
STBCOND
COND TIME
COMP COND
MAC COND
TSB COND
CONDA
CONDB
DEFER
COND
CALL DEL
RTNDEL
CMDJMPF
JMPF
TS7C
TS7D
TS7E
ENPC
SIZE
CODE IDENT NO.
C
98438
DWG NO.
129361
LTR
SCALE
SHEET 8

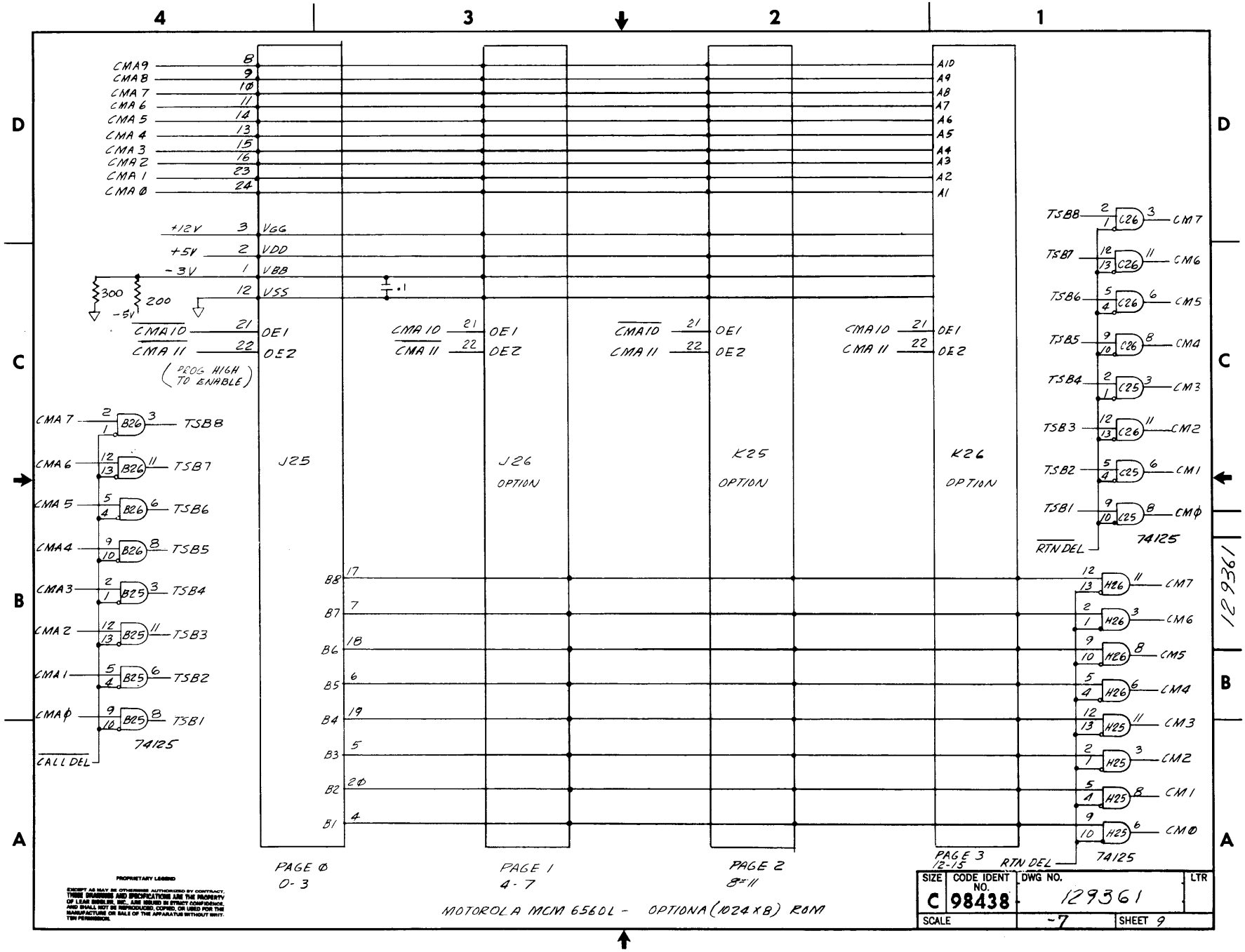


PROPRIETARY LEGEND

EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE		-7	SHEET 10

129361


4
3
2
1
D
C
B
A
CMA9
CMA8
CMA7
CMA6
CMA5
CMA4
CMA3
CMA2
CMA1
CMA0
+12V
+5V
-3V
-5V
300
200
VGG
VDD
VBB
VSS
CMA10
CMA11
OE1
OE2
(PROG HIGH TO ENABLE)
J25
J26
OPTION
K25
OPTION
K26
OPTION
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
B8
B7
B6
B5
B4
B3
B2
B1
CMA7
CMA6
CMA5
CMA4
CMA3
CMA2
CMA1
CMA0
B26
B25
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
74125
CALL DEL
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
C26
C25
CM7
CM6
CM5
CM4
CM3
CM2
CM1
CM0
74125
RTN DEL
H26
H25
CM7
CM6
CM5
CM4
CM3
CM2
CM1
CM0
74125
RTN DEL
PAGE 0
0-3
PAGE 1
4-7
PAGE 2
8-11
PAGE 3
12-15
MOTOROLA MCM 6560L - OPTION A (1024 x 8) ROM
PROPRIETARY LEGEND
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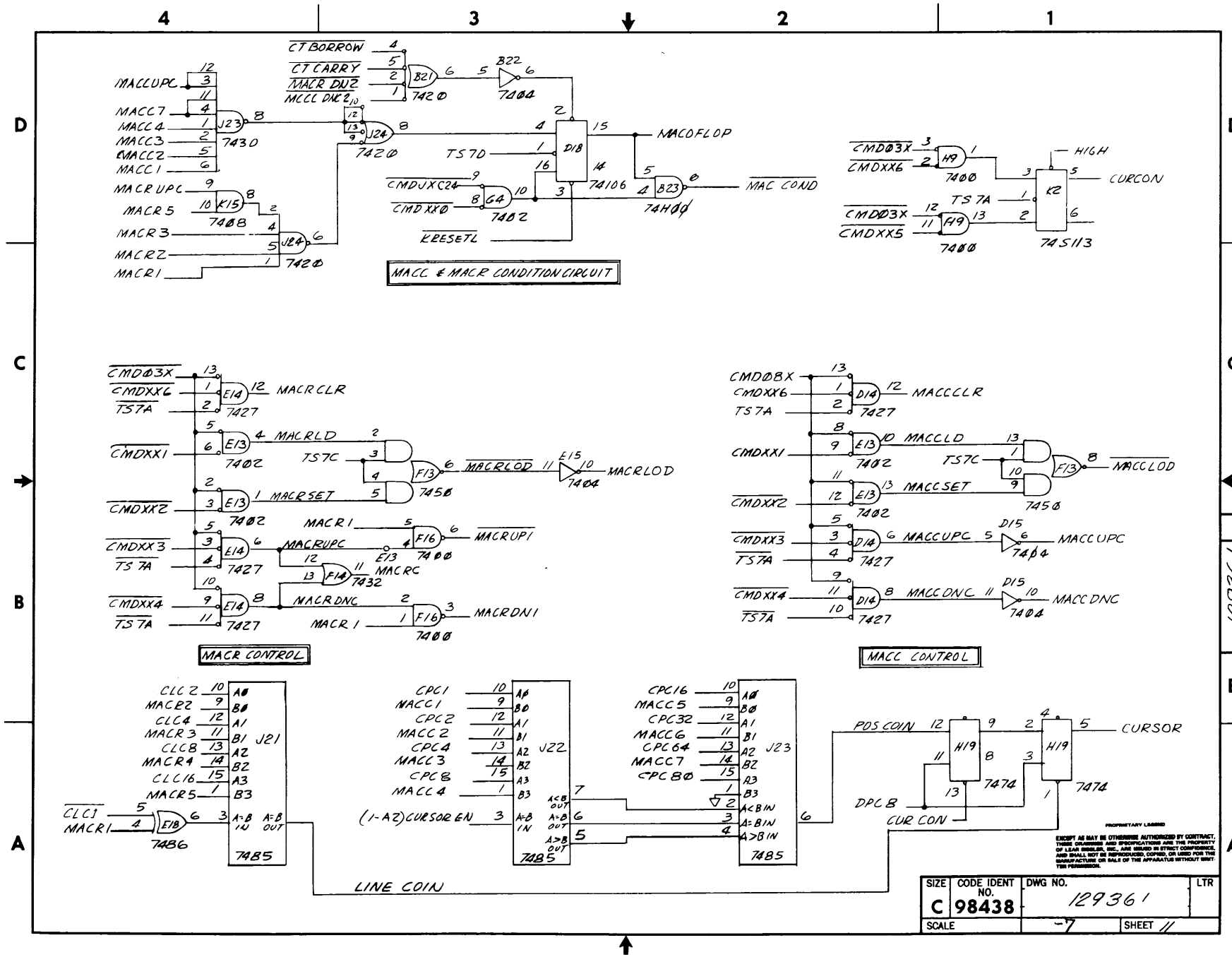
SIZE
C
CODE IDENT NO.
98438
DWG NO.
129361
LTR
SCALE
-7
SHEET 9

129361


4
3
2
1
D
C
B
A
MACCUPC
MACC7
MACC4
MACC3
MACC2
MACC1
MACRUPC
MACR5
MACR3
MACR2
MACR1
J23
7430
J24
7420
K15
7408
CTBORROW
CTCARRY
MACRDNZ
MCCLDNC2
B21
7420
B22
7404
TS7D
D18
74106
MACOFLOP
CMDJXC24
CMDXX0
G4
7402
B23
74H00
MAC COND
KRESETL
MACC & MACR CONDITION CIRCUIT
CMD03X
CMDXX6
H9
7400
HIGH
TS7A
CMD03X
CMDXX5
F19
7400
K2
74S113
CURCON
CMD03X
CMDXXC
TS7A
E14
7427
MACRCLR
CMDXX1
E13
7402
TS7C
F13
7450
MACRLOD
E15
7404
MACRLOD
CMDXX2
MACRSET
CMDXX3
TS7A
MACR1
MACRUPC
F16
7400
MACRUP1
MACRC
7432
CMDXX4
TS7A
MACRDNC
MACR1
MACRDN1
MACR CONTROL
CMD0BX
CMDXX6
TS7A
D14
7427
MACCCLR
CMDXX1
MACCLD
TS7C
MACCLOD
CMDXX2
MACCSET
CMDXX3
TS7A
MACCUPC
D15
7404
MACCUPC
CMDXX4
TS7A
MACCDNC
MACCDNC
MACC CONTROL
CLC2
MACR2
CLC4
MACR3
CLC8
MACR4
CLC16
MACR5
J21
CLC1
MACR1
E18
7486
A=B IN
A=B OUT
7485
LINE COIN
CPC1
MACC1
CPC2
MACC2
CPC4
MACC3
CPC8
MACC4
J22
(1-A2)CURSOR EN
A<B OUT
A=B OUT
A>B OUT
7485
CPC16
MACC5
CPC32
MACC6
CPC64
MACC7
CPC80
J23
A<B IN
A=B IN
A>B IN
7485
POSCOIN
H19
7474
CURSOR
DPC8
CURCON
PROPRIETARY LEGEND
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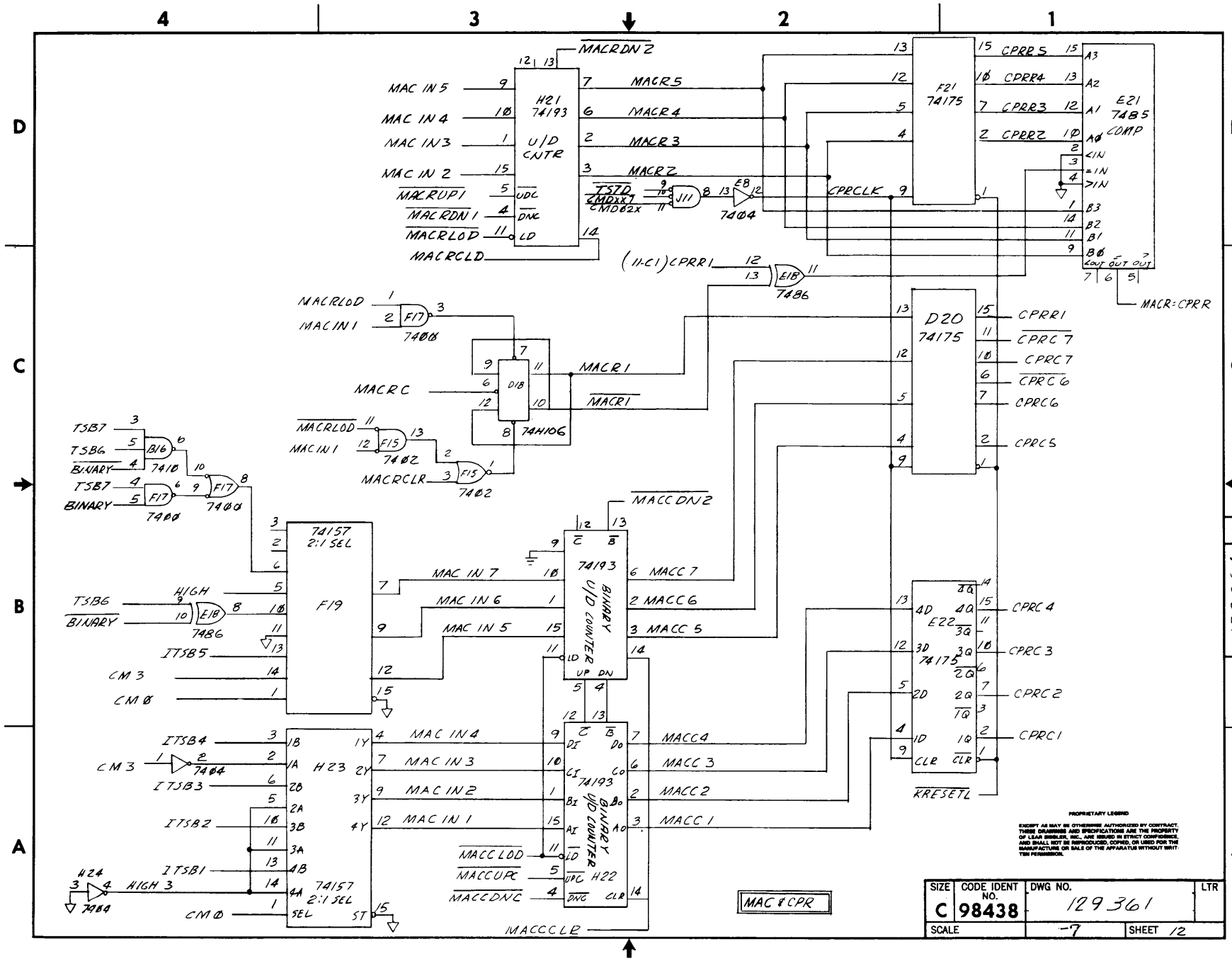
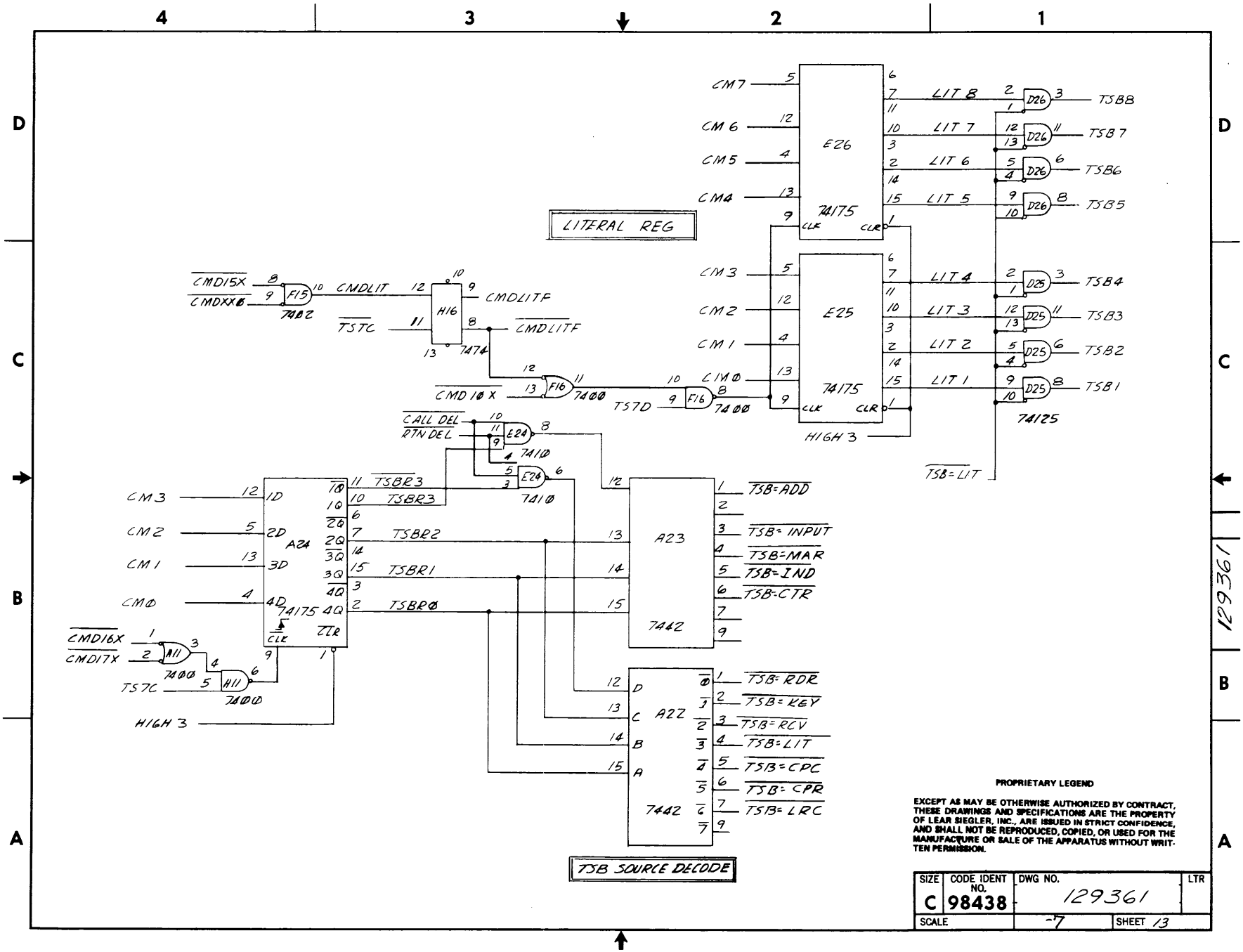
SIZE
C
CODE IDENT NO.
98438
DWG NO.
129361
LTR
SCALE
SHEET
129361


MACRDN2
MAC IN 5
MAC IN 4
MAC IN 3
MAC IN 2
MACRUP1
MACRDN1
MACRLOD
MACRCLD
H21 74193 U/D CNTR
MACR5
MACR4
MACR3
MACR2
TSZD
CMDxx1
CMD02x
J11
E8 7404
CPRCLK
F21 74175
CPRR5
CPRR4
CPRR3
CPRR2
E21 7485 COMP
<IN
=IN
>IN
B3
B2
B1
B0
COUT OUT OUT
MACR=CPRR
(11-C1)CPRR1
E18 7486
D20 74175
CPRR1
CPRC 7
CPRC 7
CPRC 6
CPRC6
CPRC5
MACRLOD
MACIN1
F17 7408
MACR1
MACRC
D18
MACR1
74H106
MACRLOD
MACIN1
F15 7402
MACRCLR
TSB7
TSB6
BINARY
B16 7410
TSB7
BINARY
F17 7408
F17 7408
74157 2:1 SEL F19
MACCDN2
74193 U/D COUNTER BINARY
MAC IN 7
MAC IN 6
MAC IN 5
MACC 7
MACC6
MACC 5
HIGH
TSB6
BINARY
E18 7486
ITSB5
CM 3
CM 0
E22 74175
CPRC 4
CPRC 3
CPRC 2
CPRC1
KRESETL
ITSB4
CM 3
7404
ITSB3
ITSB2
ITSB1
H24
HIGH 3
7404
H23 74157 2:1 SEL
MAC IN 4
MAC IN 3
MAC IN 2
MAC IN 1
74193 U/D COUNTER BINARY
MACC4
MACC 3
MACC2
MACC 1
MACCLOD
MACCUPC
MACCDNC
H22
MACCCLR
MAC & CPR
PROPRIETARY LEGEND
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE
-7
SHEET 12


LITERAL REG
E26
74175
E25
74175
74125
CM7
CM6
CM5
CM4
CM3
CM2
CM1
CM0
LIT 8
LIT 7
LIT 6
LIT 5
LIT 4
LIT 3
LIT 2
LIT 1
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
HIGH 3
TSB=LIT
CMD15X
CMDXX0
CMDLIT
CMDLITF
TSTC
CMD10X
TST0
CALL DEL
RTN DEL
A24
74175
TSBR3
TSBR2
TSBR1
TSBR0
CMD16X
CMD17X
TST7C
A23
7442
TSB=ADD
TSB=INPUT
TSB=MAR
TSB=IND
TSB=CTR
A22
7442
TSB=RDR
TSB=KEY
TSB=RCV
TSB=LIT
TSB=CPC
TSB=CPR
TSB=LRC
TSB SOURCE DECODE
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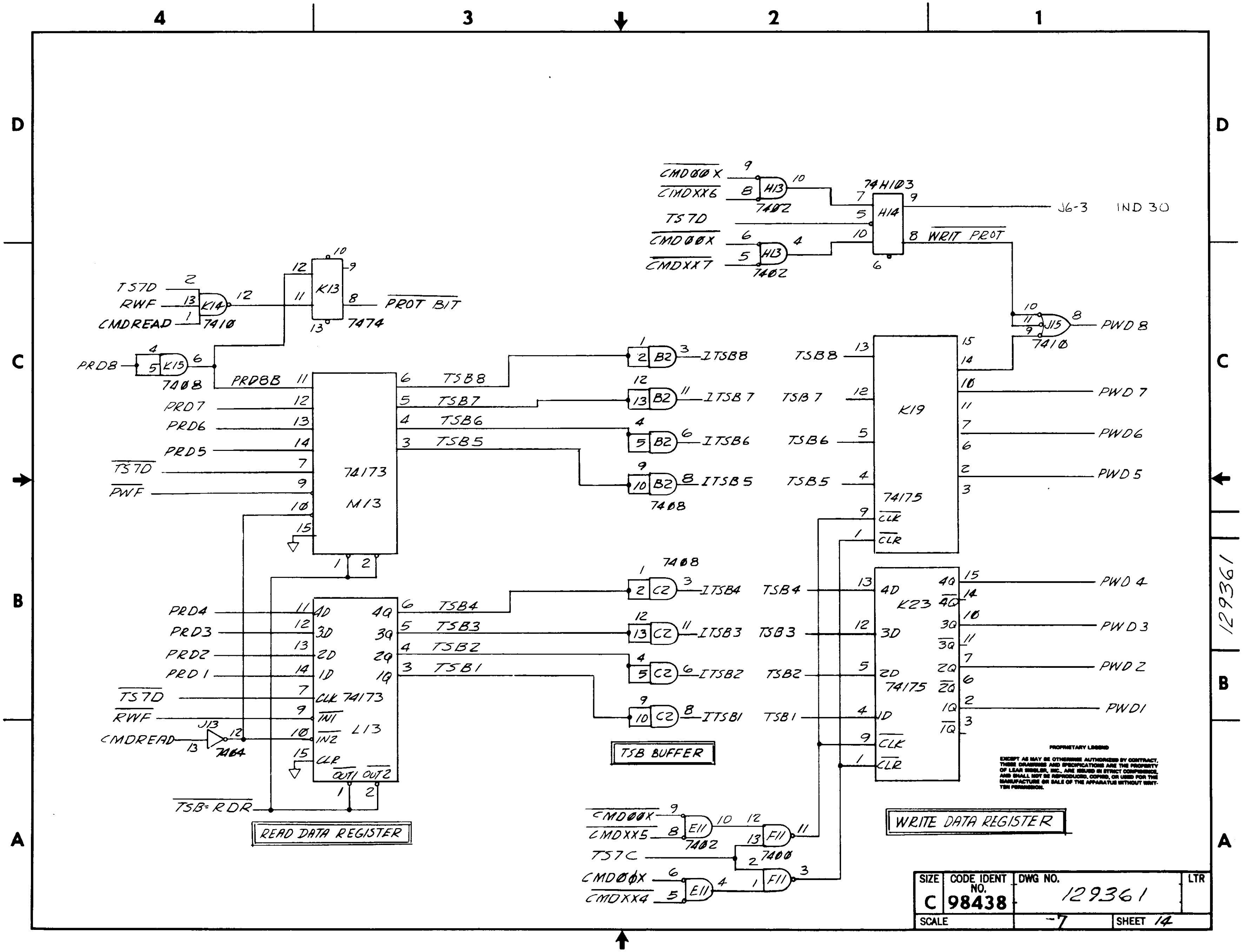
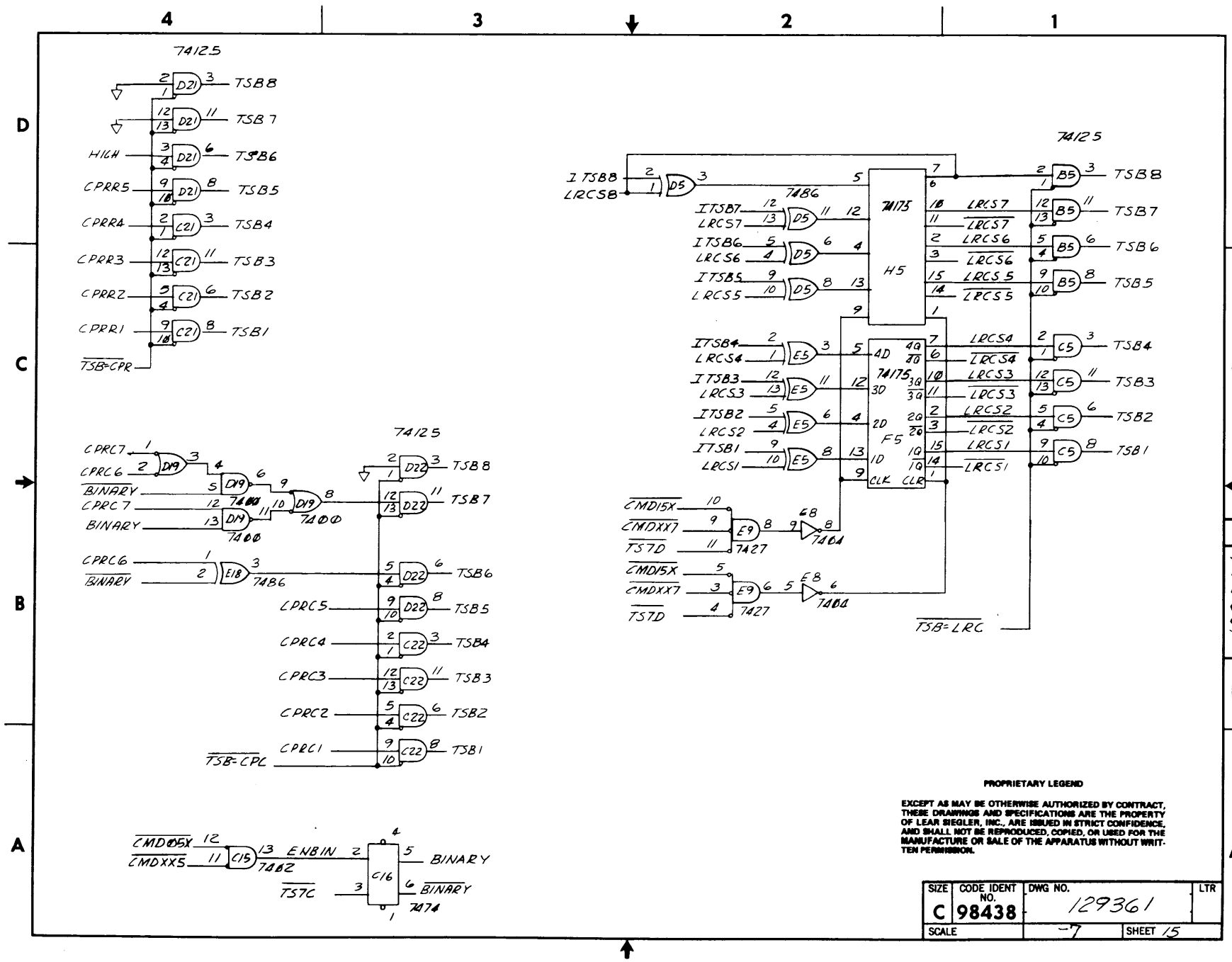
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE -7
SHEET 13



READ DATA REGISTER
TSB BUFFER
WRITE DATA REGISTER
TS7D
RWF
CMDREAD
K14
7410
K13
7474
PROT BIT
PRD8
K15
7408
PRD8B
PRD7
PRD6
PRD5
PWF
74173
M13
TSB8
TSB7
TSB6
TSB5
B2
ITSB8
ITSB7
ITSB6
ITSB5
CMD00X
CMDXX6
H13
7402
74H103
H14
J6-3
IND 30
WRIT PROT
CMDXX7
J15
PWD 8
K19
74175
CLK
CLR
PWD 7
PWD6
PWD 5
PRD4
PRD3
PRD2
PRD 1
L13
J13
7404
TSB=RDR
TSB4
TSB3
TSB2
TSB1
C2
ITSB4
ITSB3
ITSB2
ITSB1
K23
PWD 4
PWD 3
PWD 2
PWD1
CMDXX5
E11
F11
7400
TS7C
CMDXX4
PROPRIETARY LEGEND
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE
SHEET 14
129361



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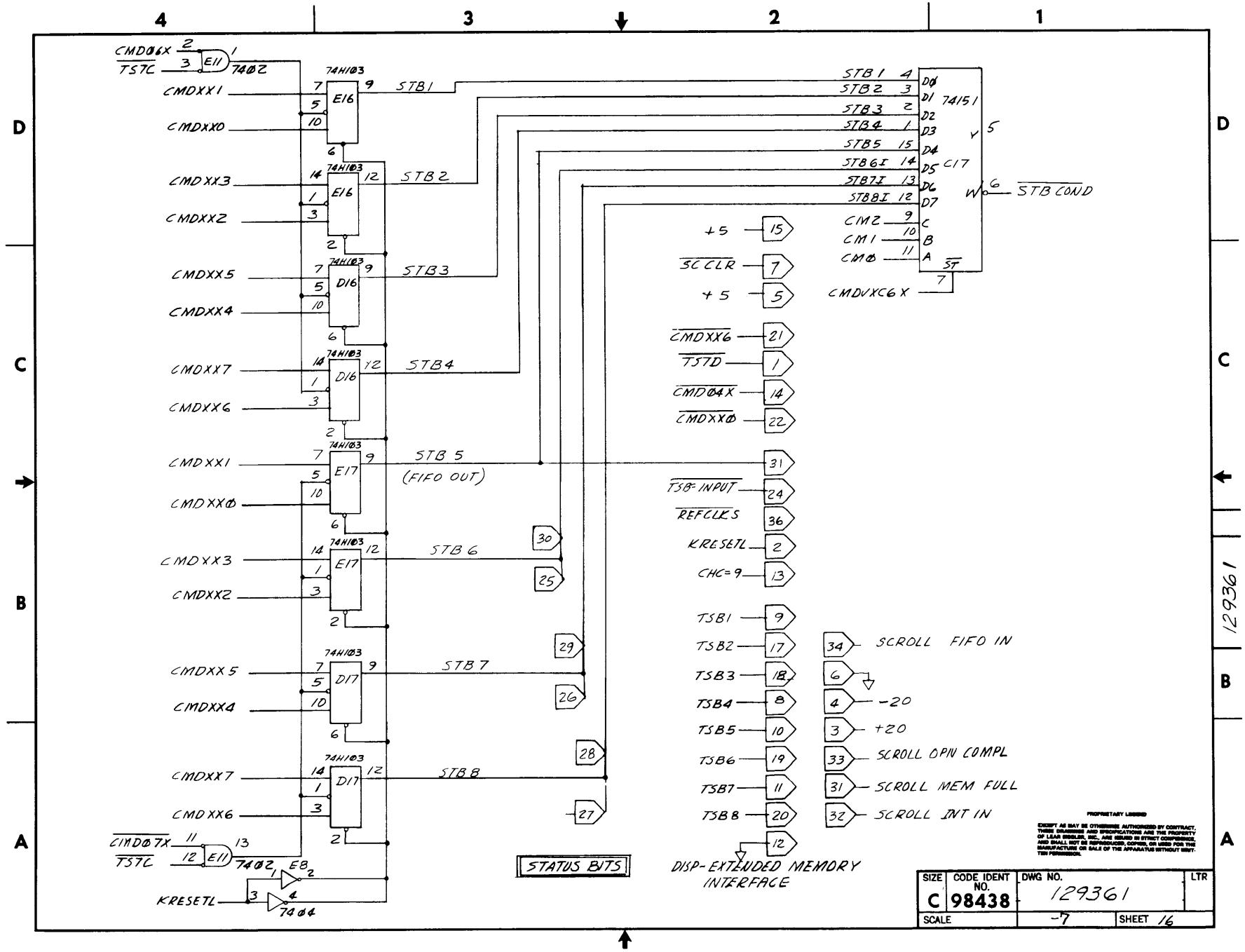
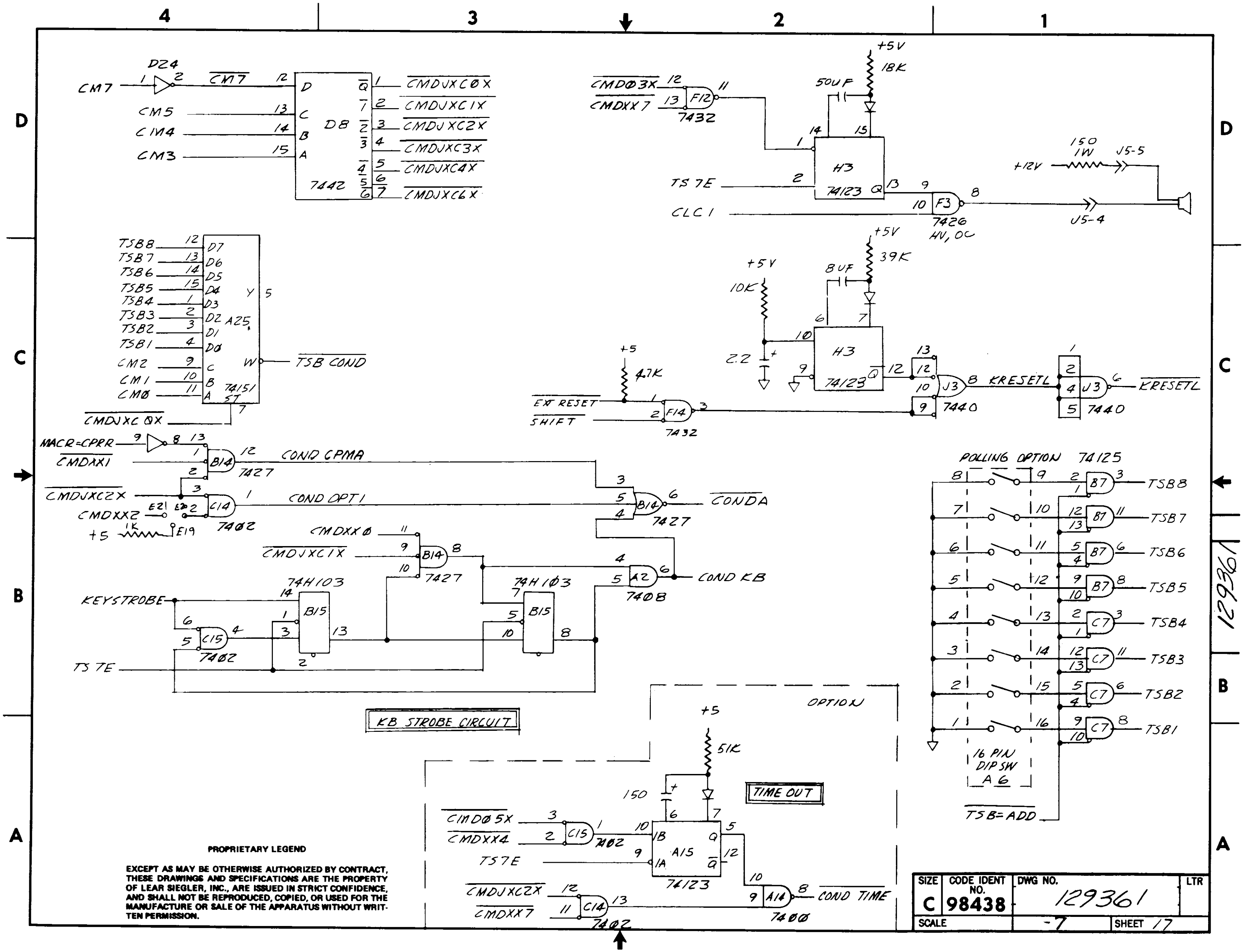
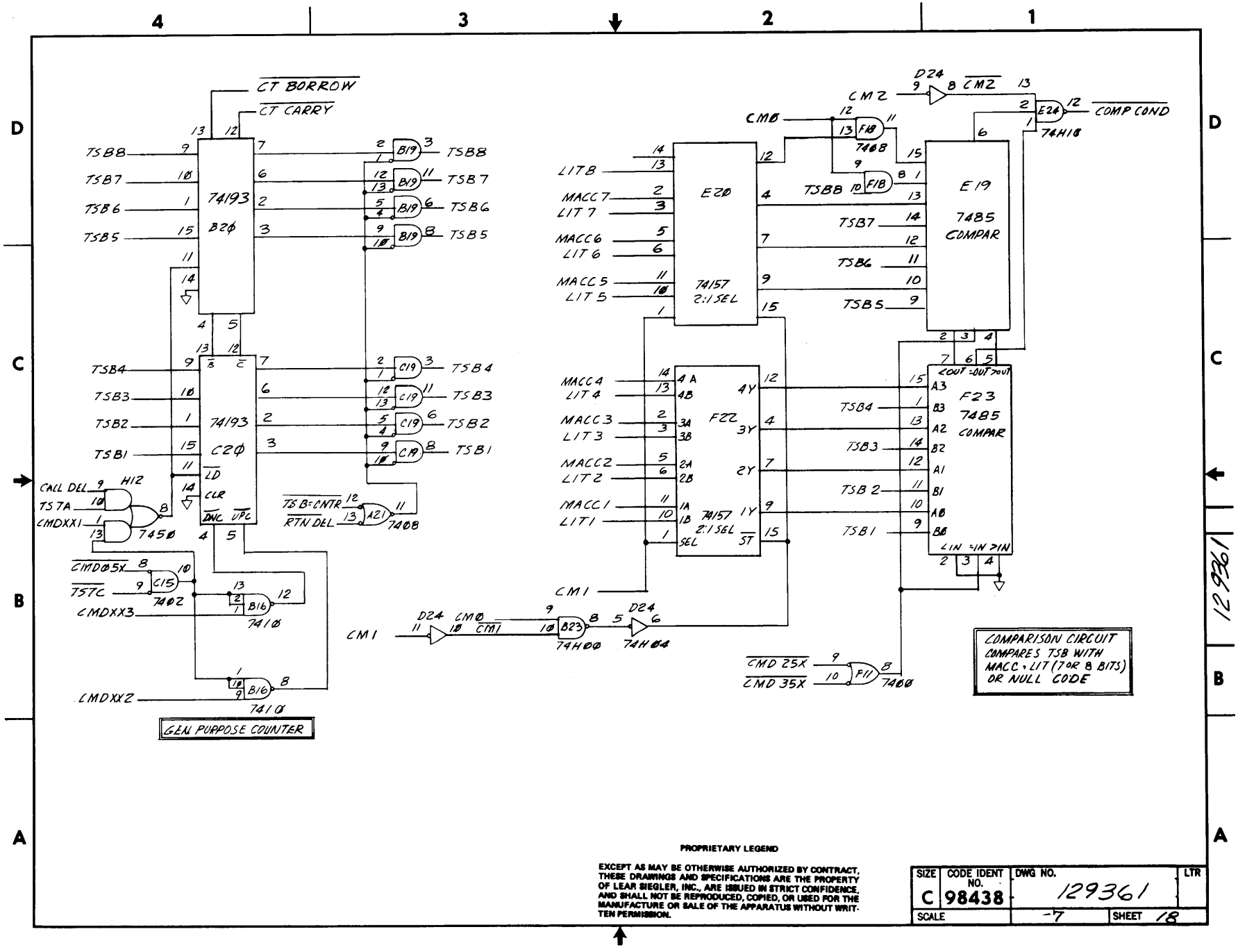
SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE		-7	SHEET 15

129361

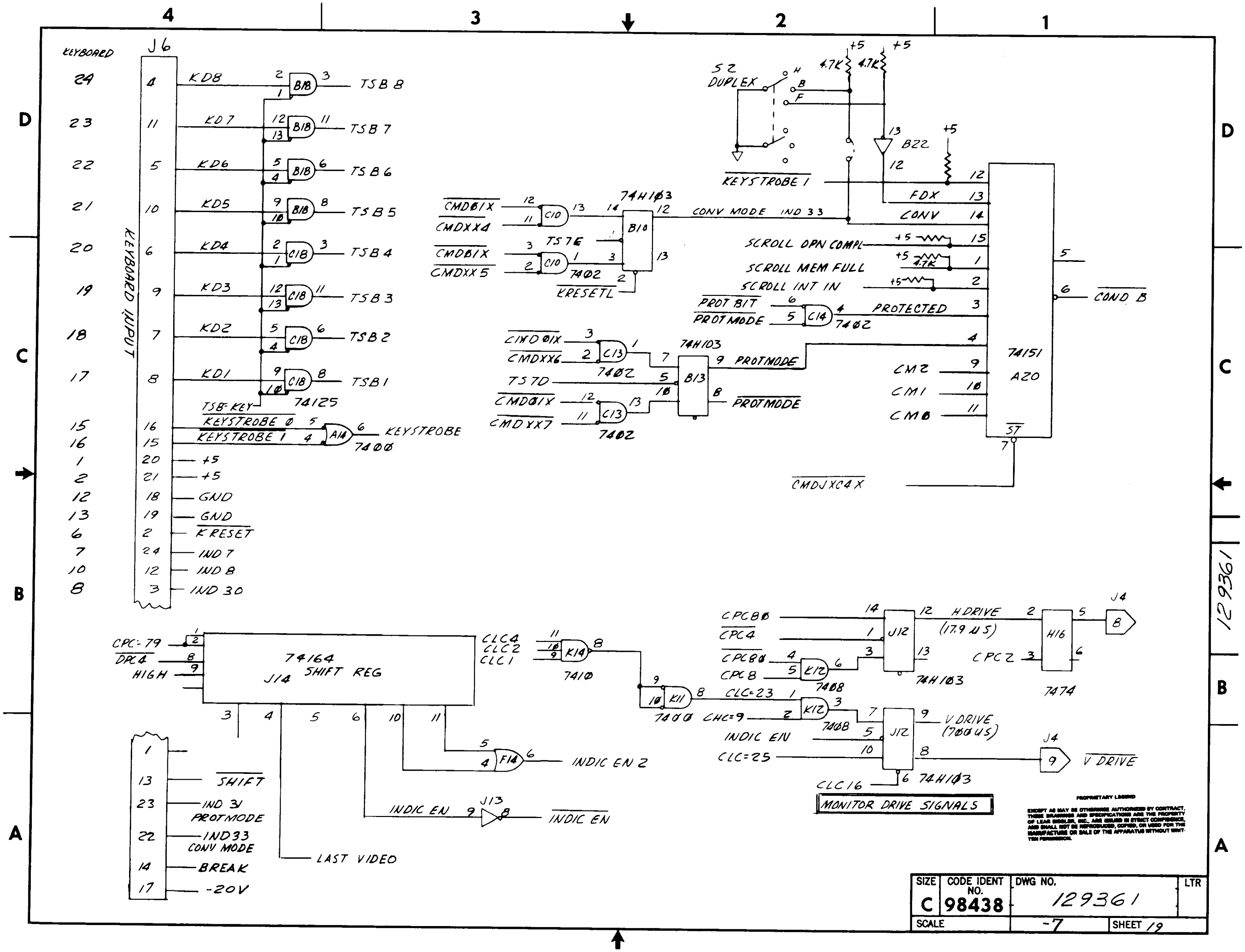

4
3
2
1
D
C
B
A
CMD06X
TST C
E11
74Ø2
74H103
E16
CMDXX1
CMDXX0
STB1
CMDXX3
CMDXX2
STB2
D16
CMDXX5
CMDXX4
STB3
CMDXX7
CMDXX6
STB4
E17
CMDXX1
CMDXXØ
STB 5
(FIFO OUT)
CMDXX3
CMDXX2
STB 6
D17
CMDXX5
CMDXX4
STB 7
CMDXX7
CMDXX6
STB 8
CMD07X
TST C
E8
74Ø4
KRESETL
STATUS BITS
74151
C17
STB1
STB2
STB3
STB4
STB5
STB6I
STB7I
STB8I
STB COND
CM2
CM1
CMØ
CMDVXC6X
+5
SCCLR
+5
CMDXX6
TSTD
CMD04X
CMDXXØ
TSB= INPUT
REFCLKS
KRESETL
CHC=9
TSB1
TSB2
TSB3
TSB4
TSB5
TSB6
TSB7
TSB8
SCROLL FIFO IN
-20
+20
SCROLL OPN COMPL
SCROLL MEM FULL
SCROLL INT IN
DISP-EXTENDED MEMORY INTERFACE
PROPRIETARY LEGEND
SIZE
CODE IDENT NO.
C
98438
DWG NO.
129361
LTR
SCALE
-7
SHEET 16
129361

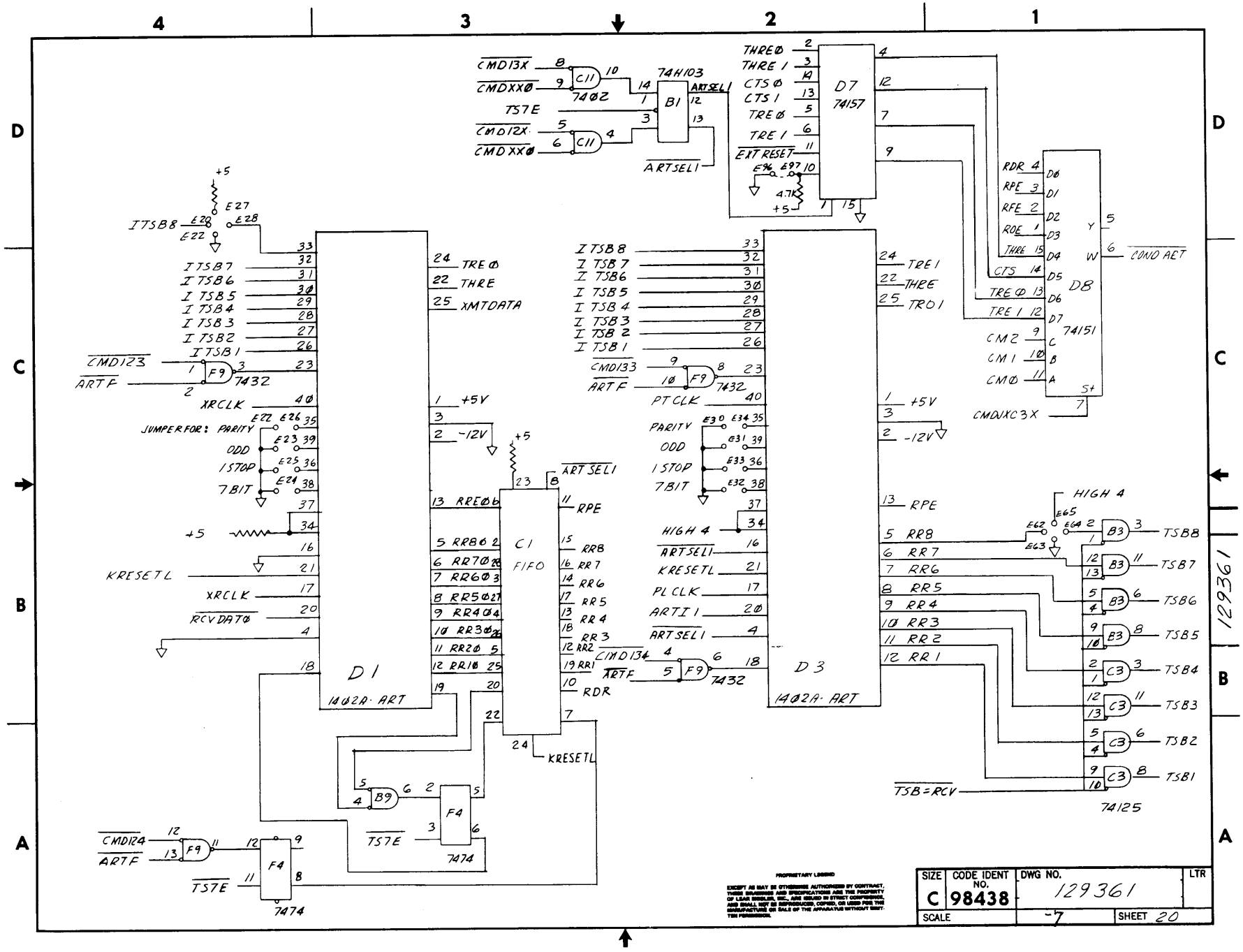


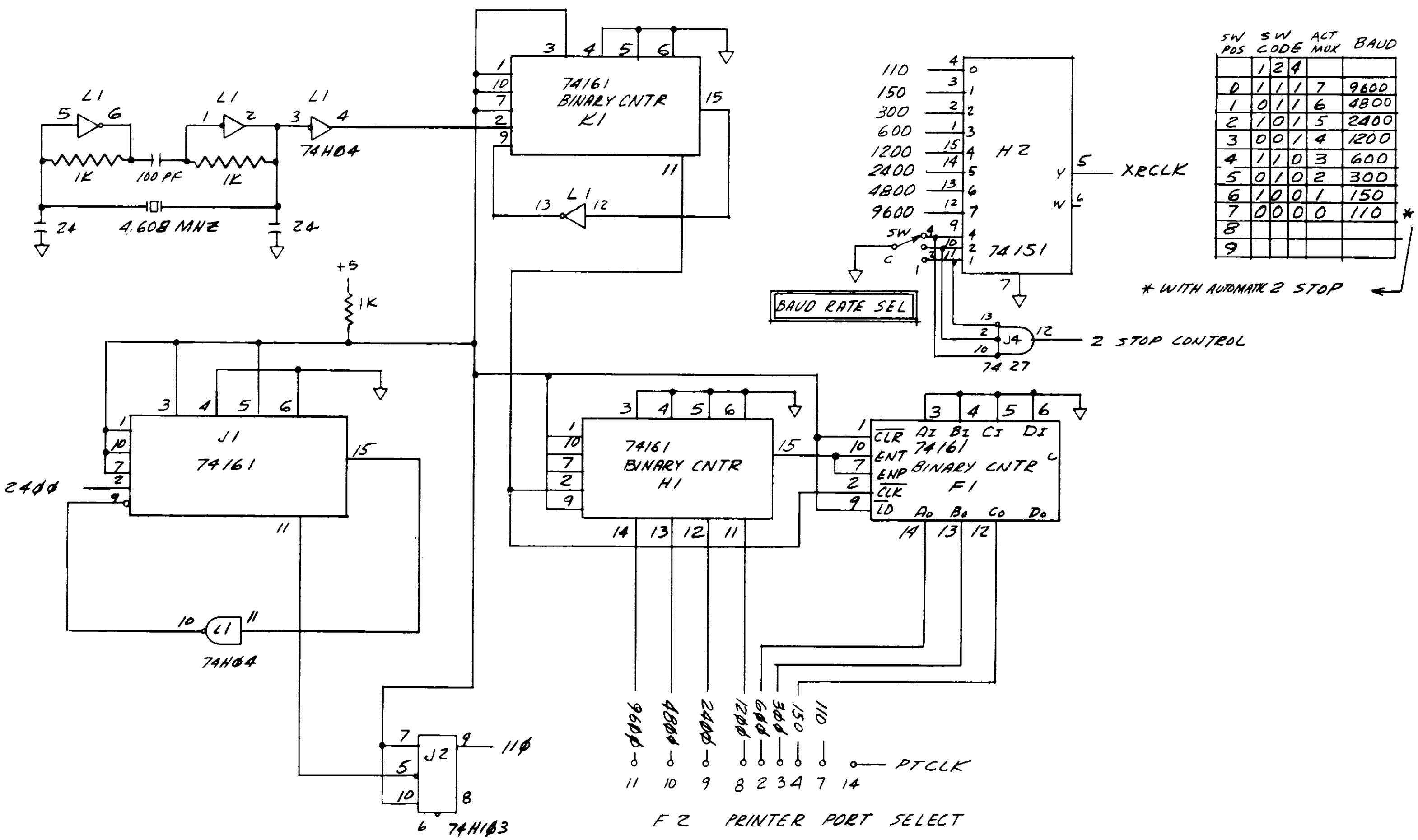
SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE		-7	SHEET 17



SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE		-7	SHEET 18


KEYBOARD
J6
KEYBOARD INPUT
KD8
KD7
KD6
KD5
KD4
KD3
KD2
KD1
TSB 8
TSB 7
TSB 6
TSB 5
TSB 4
TSB 3
TSB 2
TSB 1
B18
C18
74125
TSB KEY
KEYSTROBE 0
KEYSTROBE 1
KEYSTROBE
A14
7400
+5
GND
K RESET
IND 7
IND 8
IND 30
S2
DUPLEX
4.7K
+5
B22
KEYSTROBE 1
CMDB1X
CMDXX4
CMDB1X
CMDXX5
C10
TS7E
7402
74H103
B10
CONV MODE IND 33
KRESETL
FDX
CONV
SCROLL OPN COMPL
SCROLL MEM FULL
SCROLL INT IN
PROT BIT
PROT MODE
C14
PROTECTED
74151
A20
COND B
CMD01X
CMDXX6
TS7D
CMD01X
CMDYX7
C13
B13
PROTMODE
CM2
CM1
CM0
CMDJXC4X
CPC-79
DPC4
HIGH
74164
J14
SHIFT REG
CLC4
CLC2
CLC1
K14
7410
K11
7400
CLC=23
CHC=9
K12
7408
CPC80
CPC4
CPC80
CPC8
J12
H DRIVE
(17.9 μS)
74H103
H16
CPC2
7474
J4
V DRIVE
(700 μS)
INDIC EN
CLC=25
CLC16
MONITOR DRIVE SIGNALS
F14
INDIC EN 2
INDIC EN
J13
LAST VIDEO
SHIFT
IND 31
PROTMODE
IND33
CONV MODE
BREAK
-20V
PROPRIETARY LEGEND
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE
SHEET 19
129361


4
3
2
1
D
C
B
A
CMD13X
CMDXX0
TS7E
CMD12X
CMDXX0
C11
7402
B1
74H103
ARTSEL
ARTSEL1
THRE0
THRE 1
CTS 0
CTS 1
TRE 0
TRE 1
EXT RESET
D7
74157
4.7K
+5
RDR
RPE
RFE
ROE
THRE
CTS
TRE 0
TRE 1
CM2
CM1
CM0
D8
74151
CMD0
CMDXC3X
+5
E27
E28
E22
ITSB8
ITSB7
ITSB6
ITSB5
ITSB4
ITSB3
ITSB2
ITSB1
CMD123
ARTF
F9
7432
XRCLK
JUMPER FOR: PARITY
ODD
1STOP
7BIT
E22 E26
E23
E25
E24
KRESETL
XRCLK
RCVDATA
D1
1402A-ART
TRE0
THRE
XMTDATA
+5V
-12V
RRE0
RR8
RR7
RR6
RR5
RR4
RR3
RR2
RR1
RDR
C1
FIFO
ARTSEL1
RPE
KRESETL
B9
F4
7474
CMD124
ARTF
TS7E
ITSB8
ITSB7
ITSB6
ITSB5
ITSB4
ITSB3
ITSB2
ITSB1
CMD133
ARTF
PTCLK
PARITY
ODD
1STOP
7BIT
E30 E34
E31
E33
E32
HIGH 4
ARTSEL1
KRESETL
PLCLK
ARTI1
ARTSEL1
CMD134
ARTF
D3
1402A-ART
TRE1
THRE
TRO1
+5V
-12V
RPE
RR8
RR7
RR6
RR5
RR4
RR3
RR2
RR1
HIGH 4
E65
E62
E64
E63
B3
C3
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
TSB=RCV
74125
PROPRIETARY LEGEND
SIZE
C
CODE IDENT NO.
98438
DWG NO.
129361
LTR
SCALE
-7
SHEET 20

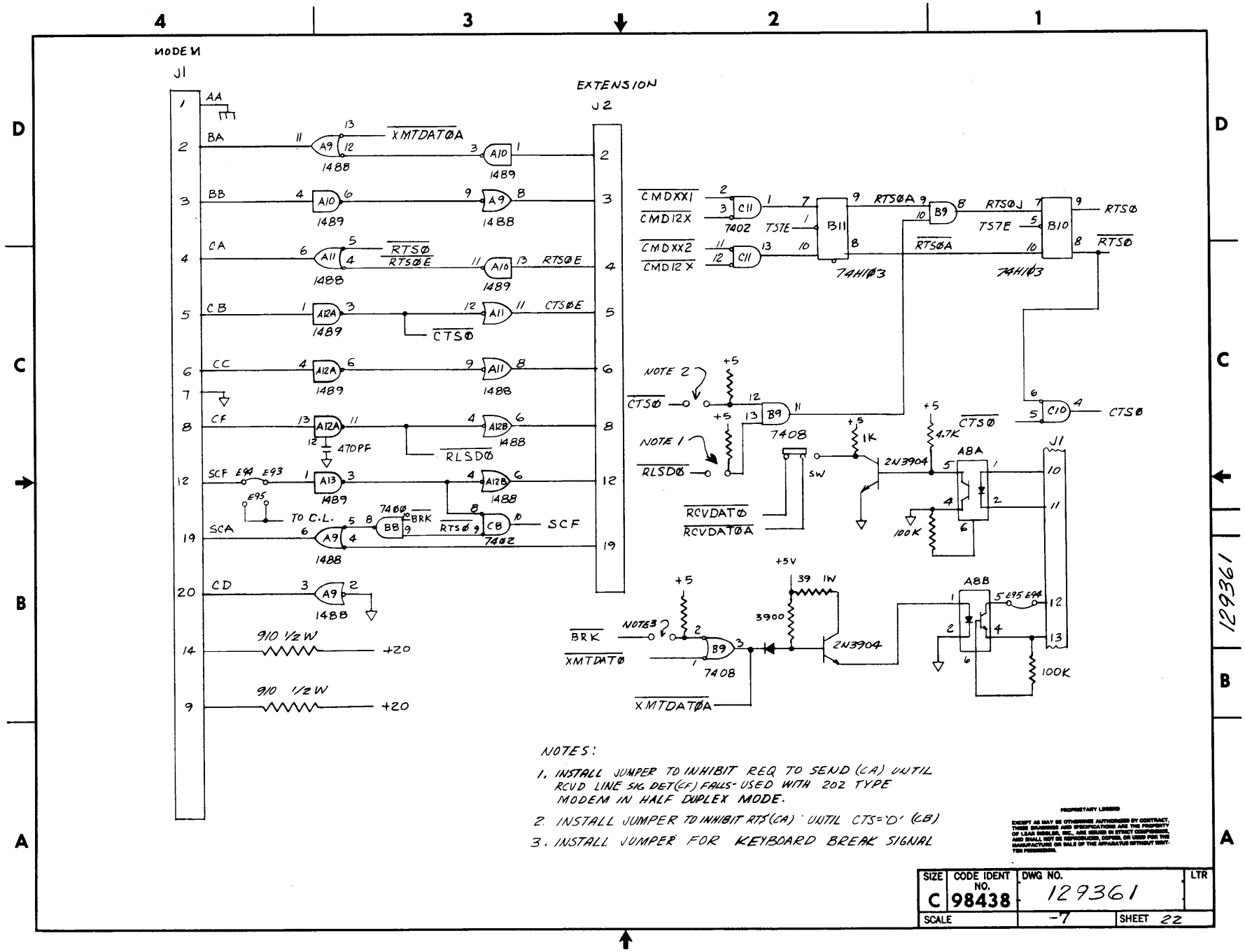


SW POS	SW CODE 1 2 4	ACT MUX	BAUD
0	1 1 1	7	9600
1	0 1 1	6	4800
2	1 0 1	5	2400
3	0 0 1	4	1200
4	1 1 0	3	600
5	0 1 0	2	300
6	1 0 0	1	150
7	0 0 0	0	110 *
8			
9			

* WITH AUTOMATIC 2 STOP

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE		7	SHEET 21

129361

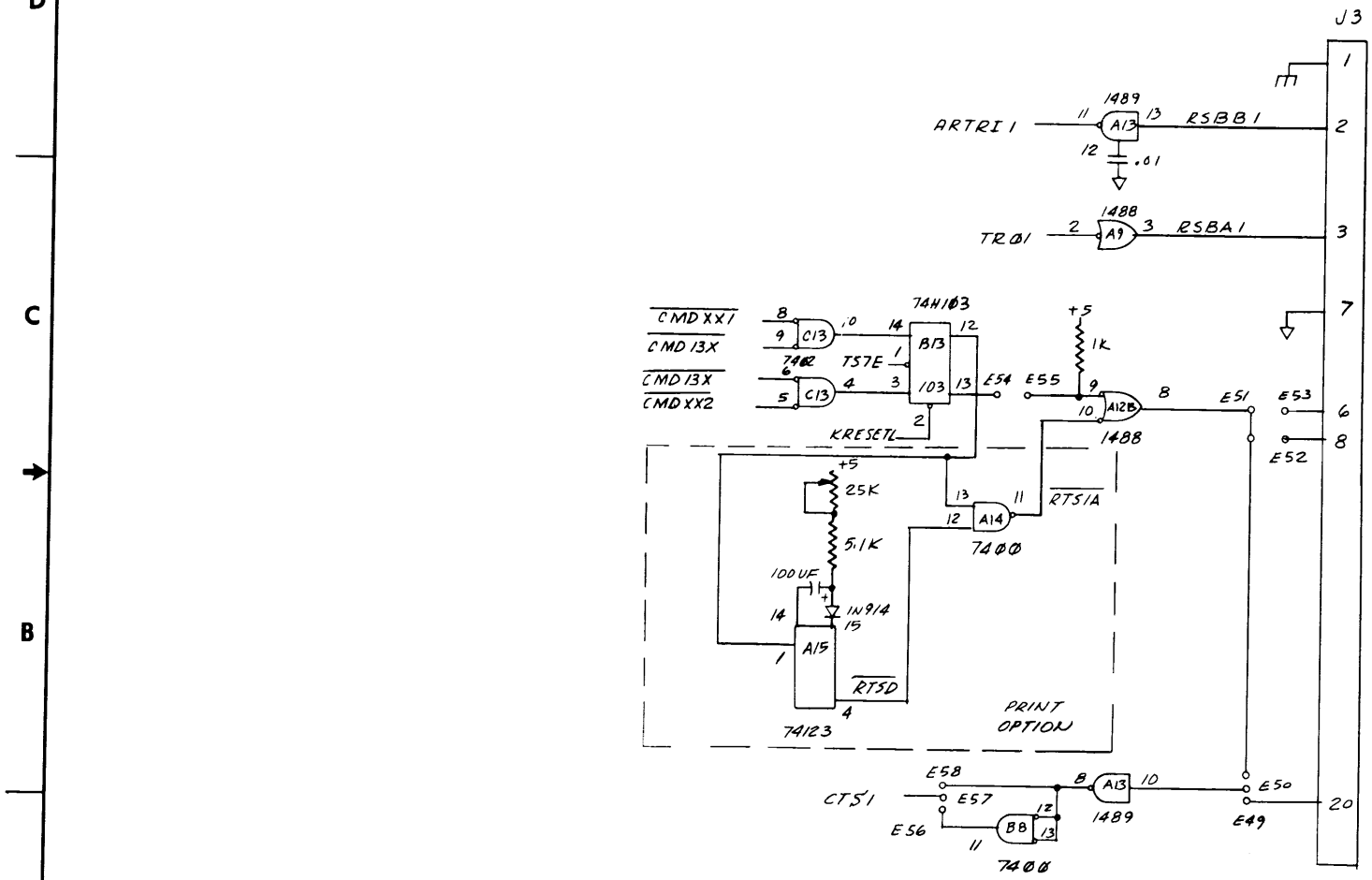


NOTES:

1. INSTALL JUMPER TO INHIBIT REQ TO SEND (CA) UNTIL RCVD LINE SIG DET(CF) FALLS- USED WITH 202 TYPE MODEM IN HALF DUPLEX MODE.
2. INSTALL JUMPER TO INHIBIT RTS(CA) UNTIL CTS='0' (CB)
3. INSTALL JUMPER FOR KEYBOARD BREAK SIGNAL

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE	-7	SHEET 22	

129361



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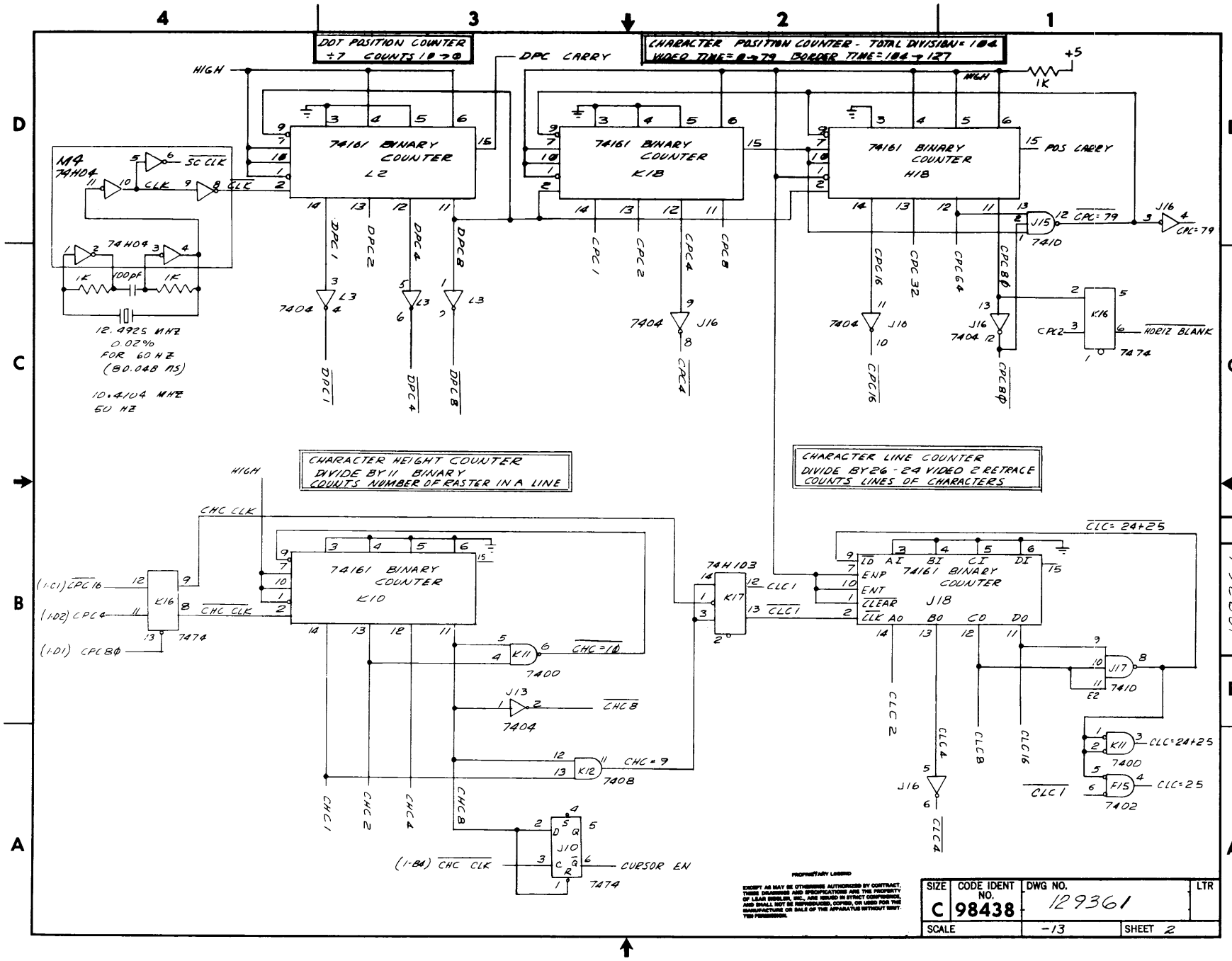
PRINTER OPTION

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE		-7	SHEET 23

129361


DOT POSITION COUNTER
÷7 COUNTS 10→0
CHARACTER POSITION COUNTER - TOTAL DIVISION = 104
VIDEO TIME = 0→79 BORDER TIME = 104→127
HIGH
DPC CARRY
+5
1K
74161 BINARY COUNTER L2
74161 BINARY COUNTER K18
74161 BINARY COUNTER H18
POS CARRY
M4 74H04
SC CLK
CLK
CLE
74H04
1K
100pf
1K
12.4925 MHZ
0.02%
FOR 60 HZ
(80.048 NS)
10.4104 MHZ
50 HZ
DPC 1
DPC 2
DPC 4
DPC 8
7404
L3
CPC 1
CPC 2
CPC 4
CPC 8
CPC 16
CPC 32
CPC 64
CPC 8Ø
J16
J15
7410
CPC=79
K16
7474
CPC2
HORIZ BLANK
CHARACTER HEIGHT COUNTER
DIVIDE BY 11 BINARY
COUNTS NUMBER OF RASTER IN A LINE
CHARACTER LINE COUNTER
DIVIDE BY 26 - 24 VIDEO 2 RETRACE
COUNTS LINES OF CHARACTERS
HIGH
CHC CLK
74161 BINARY COUNTER K10
(1-C1) CPC 16
(1-D2) CPC 4
(1-D1) CPC 8Ø
CHC CLK
7474
K11
7400
CHC=10
J13
7404
CHC 8
K12
7408
CHC=9
CHC 1
CHC 2
CHC 4
CHC 8
J10
(1-B4) CHC CLK
CURSOR EN
7474
74H103
K17
CLC1
CLC1
74161 BINARY COUNTER J18
LD
ENP
ENT
CLEAR
CLK
AI
BI
CI
DI
AO
BO
CO
DO
CLC=24+25
J17
7410
E2
K11
7400
CLC=24+25
F15
7402
CLC=25
CLC 2
CLC 4
CLC 8
CLC 16
CLC 1
CLC 4
J16
PROPRIETARY LEGEND
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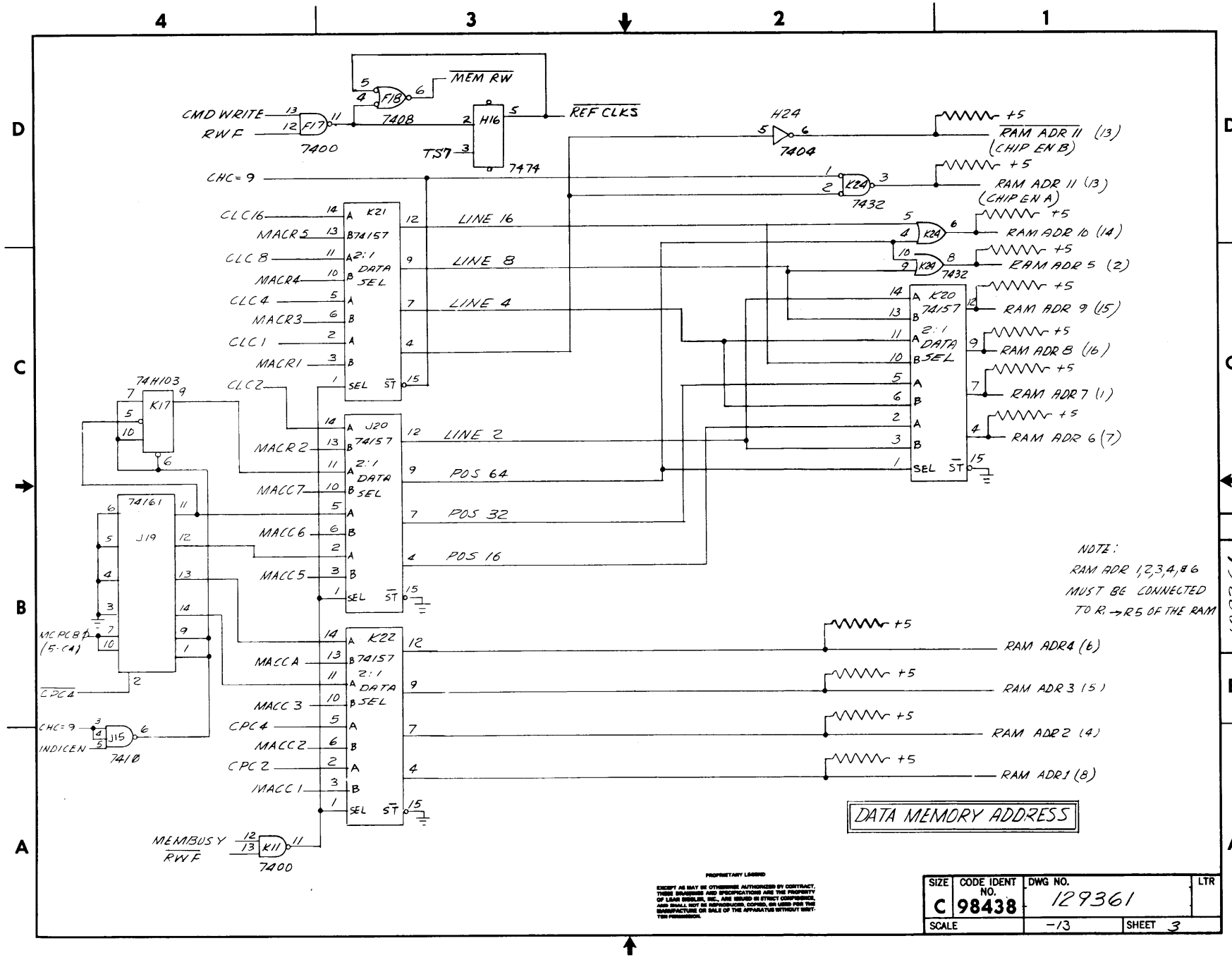
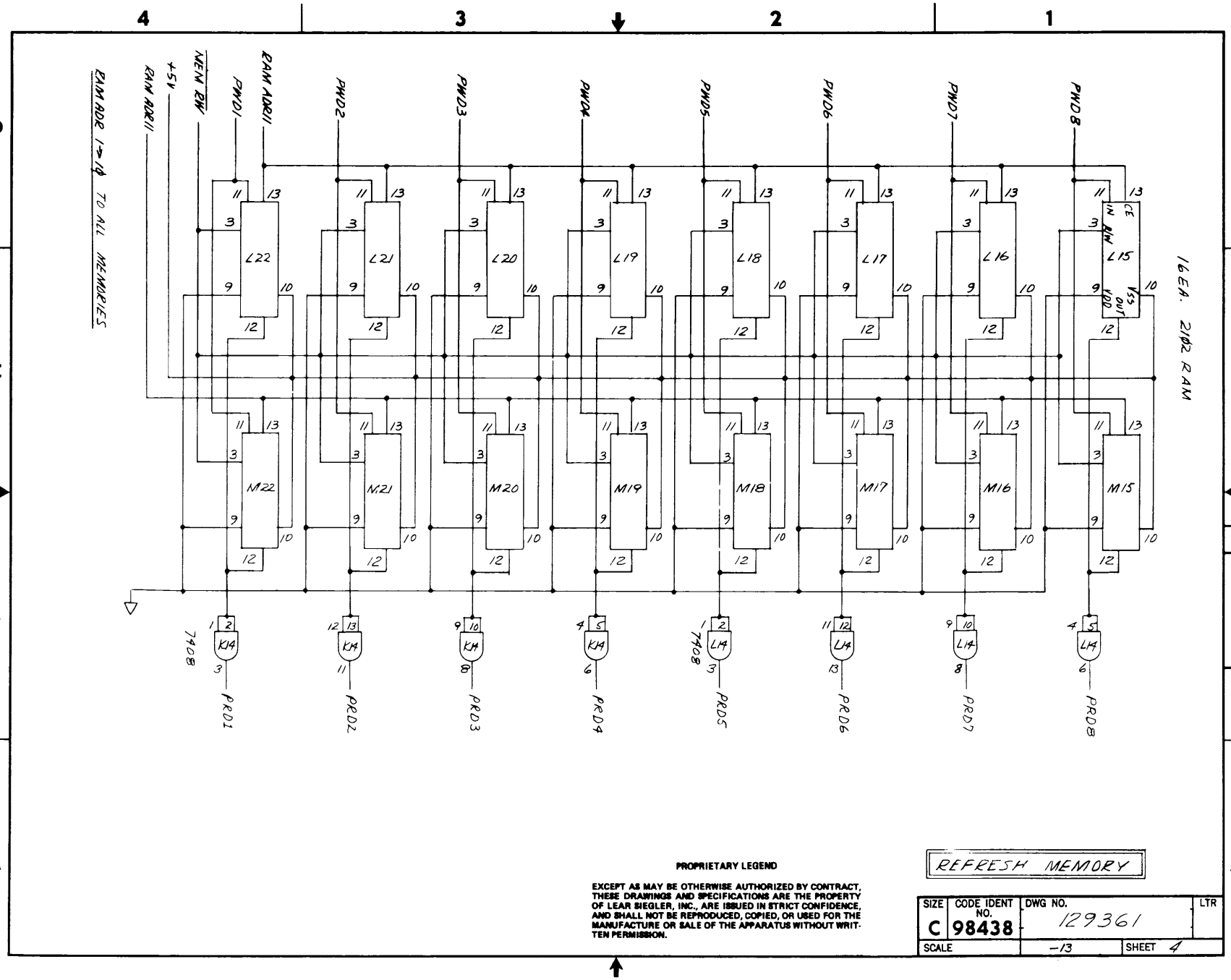
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE
-13
SHEET 2


MEM RW
CMD WRITE
RWF
7400
7408
H16
7474
REF CLKS
TS7
CHC=9
H24
7404
+5
RAM ADR 11 (13)
(CHIP EN B)
RAM ADR 11 (13)
(CHIP EN A)
7432
RAM ADR 10 (14)
RAM ADR 5 (2)
RAM ADR 9 (15)
RAM ADR 8 (16)
RAM ADR 7 (1)
RAM ADR 6 (7)
K21
74157
2:1 DATA SEL
CLC16
MACR5
CLC 8
MACR4
CLC 4
MACR3
CLC 1
MACR1
CLC2
LINE 16
LINE 8
LINE 4
74H103
K17
K20
J20
MACR 2
MACC7
MACC6
MACC5
LINE 2
POS 64
POS 32
POS 16
74161
J19
MACC A
MACC 3
CPC 4
MACC2
CPC 2
MACC 1
K22
RAM ADR4 (6)
RAM ADR 3 (5)
RAM ADR2 (4)
RAM ADR1 (8)
MACPCB
(5:C4)
CPC4
CHC=9
INDICEN
J15
7410
MEMBUSY
RWF
K11
7400
NOTE:
RAM ADR 1,2,3,4,8 6
MUST BE CONNECTED
TO R→R5 OF THE RAM
DATA MEMORY ADDRESS
PROPRIETARY LEGEND
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE
-13
SHEET 3
129361


4
3
2
1
D
C
B
A
RAM ADR 1 → 10 TO ALL MEMORIES
+5V
RAM ADR11
MEM RW
PWD1
RAM ADR11
PWD2
PWD3
PWD4
PWD5
PWD6
PWD7
PWD8
16 EA. 2102 RAM
L22
L21
L20
L19
L18
L17
L16
L15
M22
M21
M20
M19
M18
M17
M16
M15
CE IN
R/W
VSS
DOUT
VDD
7408
K4
L4
PRD1
PRD2
PRD3
PRD4
PRD5
PRD6
PRD7
PRD8
PROPRIETARY LEGEND
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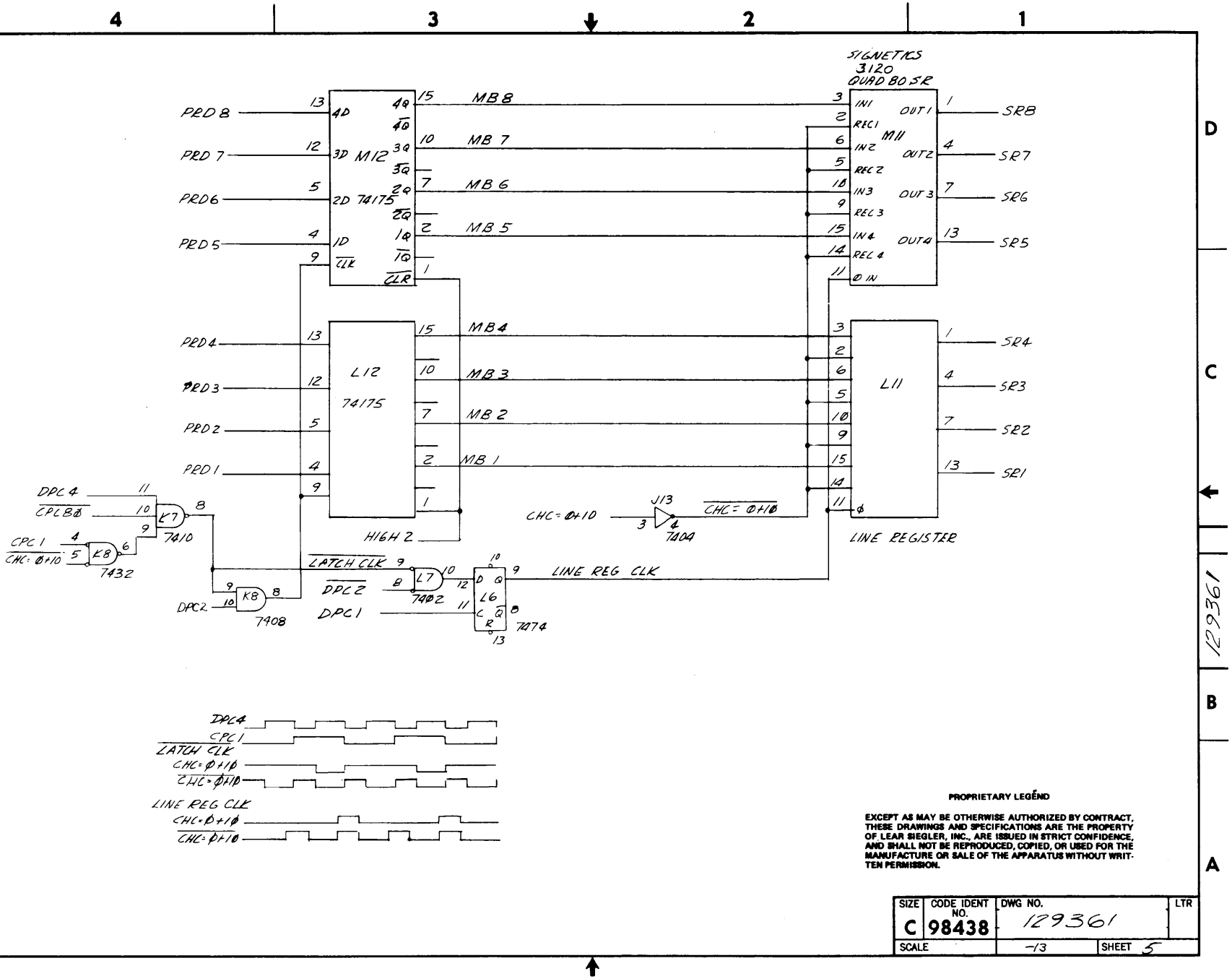
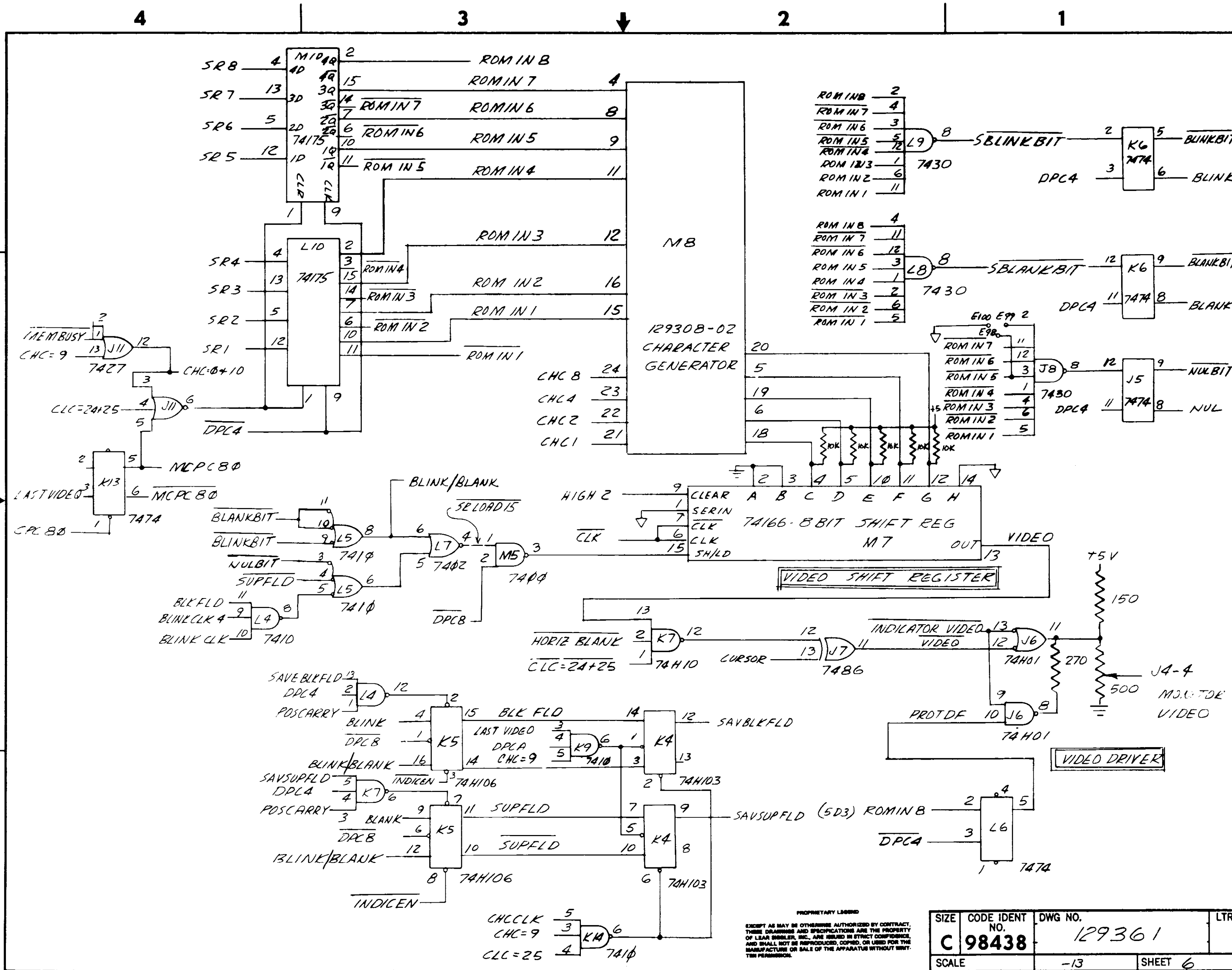
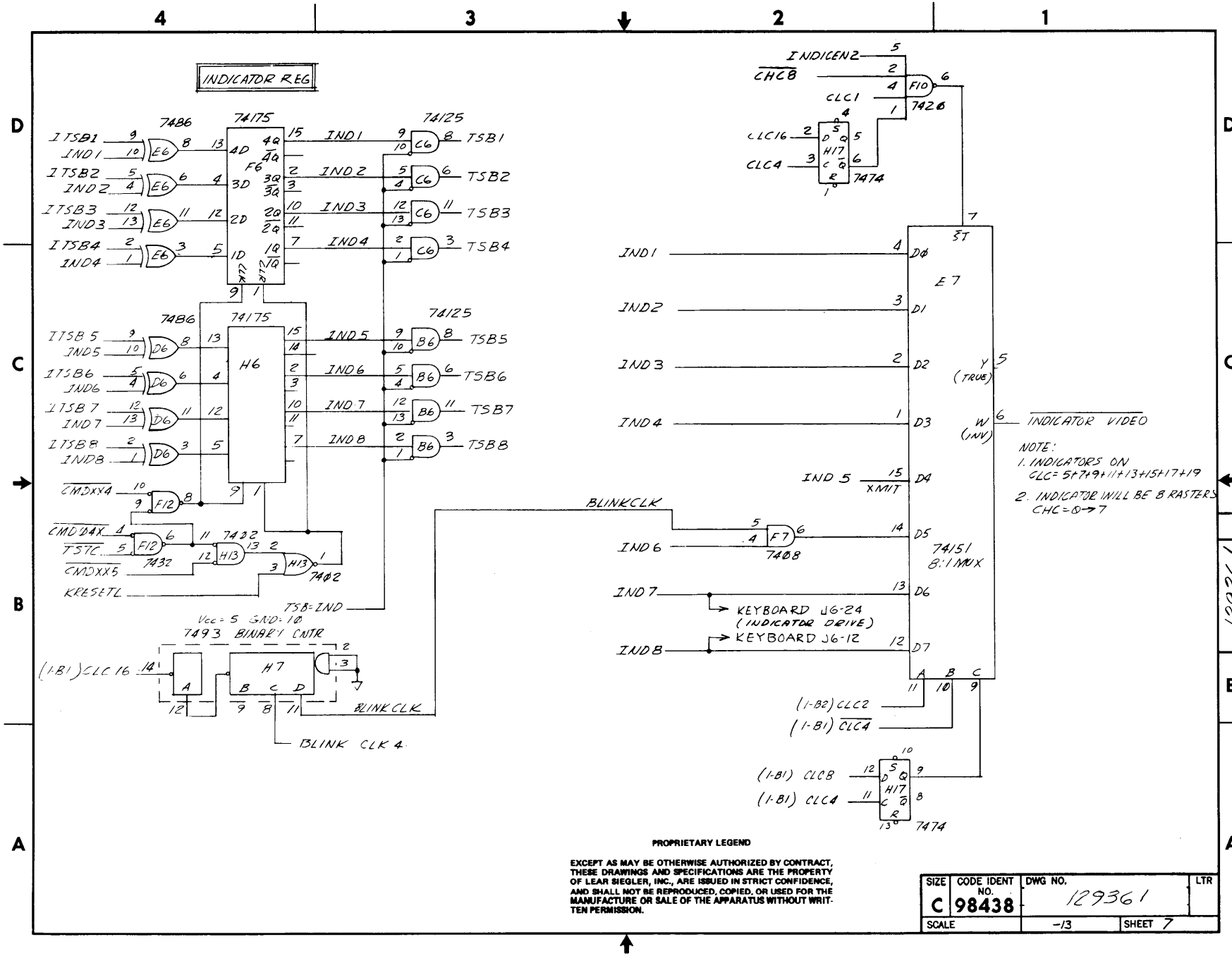
REFRESH MEMORY
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE
-13
SHEET 4
129361



SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE		-13	SHEET 5

129361


4
3
2
1
D
C
B
A
ROM IN 8
ROM IN 7
ROM IN 6
ROM IN 5
ROM IN 4
ROM IN 3
ROM IN 2
ROM IN 1
SR8
SR7
SR6
SR5
SR4
SR3
SR2
SR1
74175
L10
M8
129308-02
CHARACTER
GENERATOR
CHC 8
CHC 4
CHC 2
CHC 1
L9
7430
SBLINKBIT
K6
7474
BLINKBIT
BLINK
DPC4
L8
SBLANKBIT
BLANKBIT
BLANK
J8
J5
NULBIT
NUL
MEMBUSY
CHC=9
J11
7427
CHC=0+10
CLC=24+25
DPC4
K13
LAST VIDEO
MCPC80
CPC80
BLINK/BLANK
SELOADIS
HIGH Z
CLEAR
SERIN
CLK
SH/LD
74166 - 8 BIT SHIFT REG
M7
OUT
VIDEO
VIDEO SHIFT REGISTER
L5
7410
L7
7402
M5
7400
SUPFLD
BLKFLD
BLINK CLK
L4
DPC8
+5V
150
HORIZ BLANK
K7
74H10
CLC=24+25
CURSOR
J7
7486
INDICATOR VIDEO
J6
74H01
270
500
J4-4
MONITOR
VIDEO
PROT DF
VIDEO DRIVER
SAVE BLKFLD
POSCARRY
K5
BLK FLD
LAST VIDEO
K9
K4
74H103
SAVBLKFLD
INDICEN
74H106
SAVSUPFLD
SAVSUP FLD
(5D3) ROMIN B
L6
CHCCLK
CLC=25
K14
129361
PROPRIETARY LEGEND
SIZE
C
CODE IDENT NO.
98438
DWG NO.
129361
LTR
SCALE
-13
SHEET 6


INDICATOR REG
7486
74175
74125
ITSB1
IND1
ITSB2
IND2
ITSB3
IND3
ITSB4
IND4
TSB1
TSB2
TSB3
TSB4
F6
H6
ITSB5
IND5
ITSB6
IND6
ITSB7
IND7
ITSB8
IND8
TSB5
TSB6
TSB7
TSB8
CMDXX4
CMDDAX
TSTC
CMDXX5
KRESETL
7432
7402
TSB=IND
Vcc=5 GND=10
7493 BINARY CNTR
(1-B1)CLC16
H7
BLINK CLK
BLINK CLK 4
INDICEN2
CHC8
CLC1
F10
7420
CLC16
CLC4
7474
IND1
IND2
IND3
IND4
IND5
IND6
IND7
IND8
E7
74151
8:1 MUX
XMIT
(TRUE)
(INV)
INDICATOR VIDEO
BLINKCLK
KEYBOARD J6-24
(INDICATOR DRIVE)
KEYBOARD J6-12
(1-B2)CLC2
(1-B1)CLC4
(1-B1) CLC8
(1-B1) CLC4
NOTE:
1. INDICATORS ON CLC= 5+7+9+11+13+15+17+19
2. INDICATOR WILL BE 8 RASTERS CHC=0→7
PROPRIETARY LEGEND
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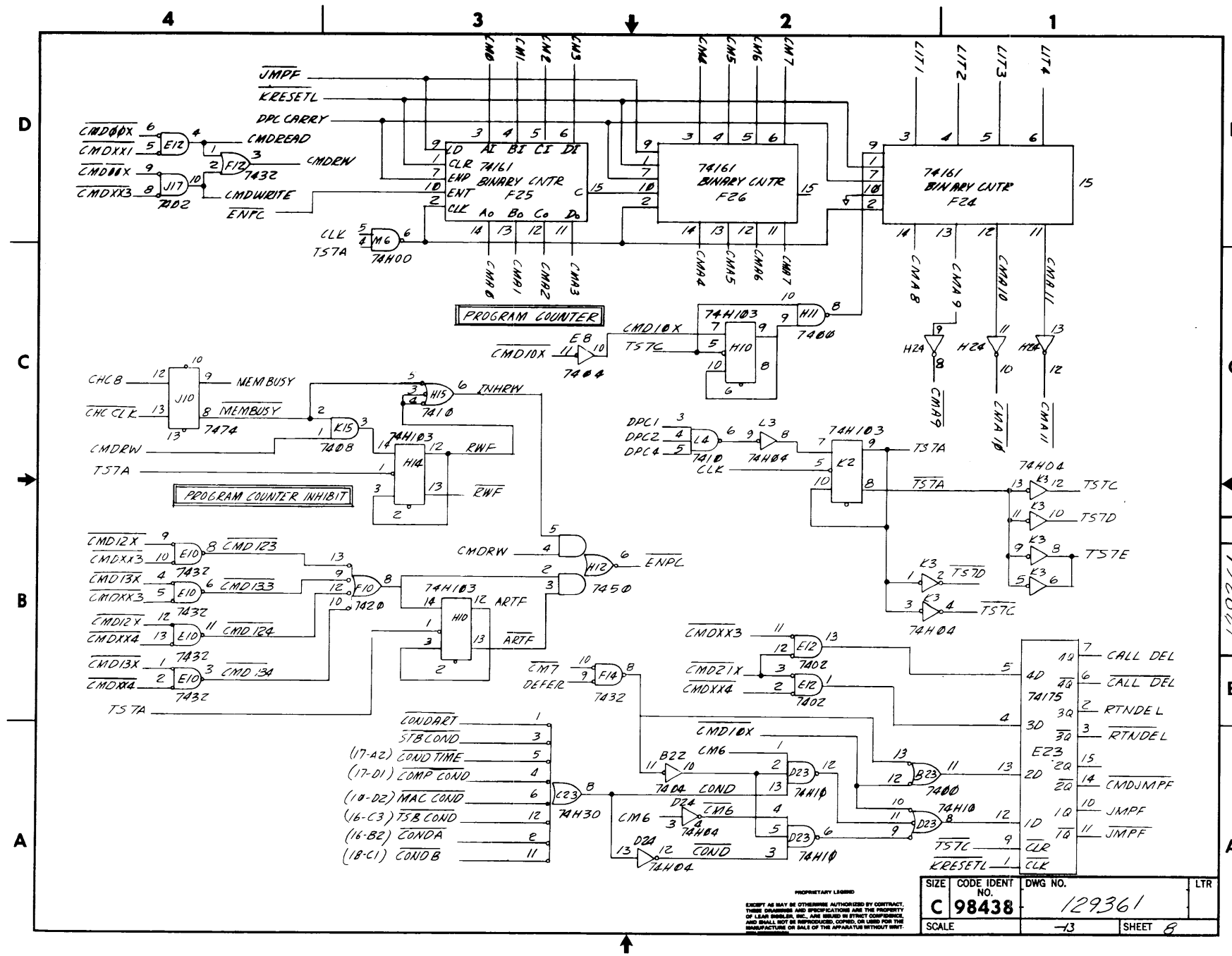
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE -/3
SHEET 7



PROPRIETARY LEGEND

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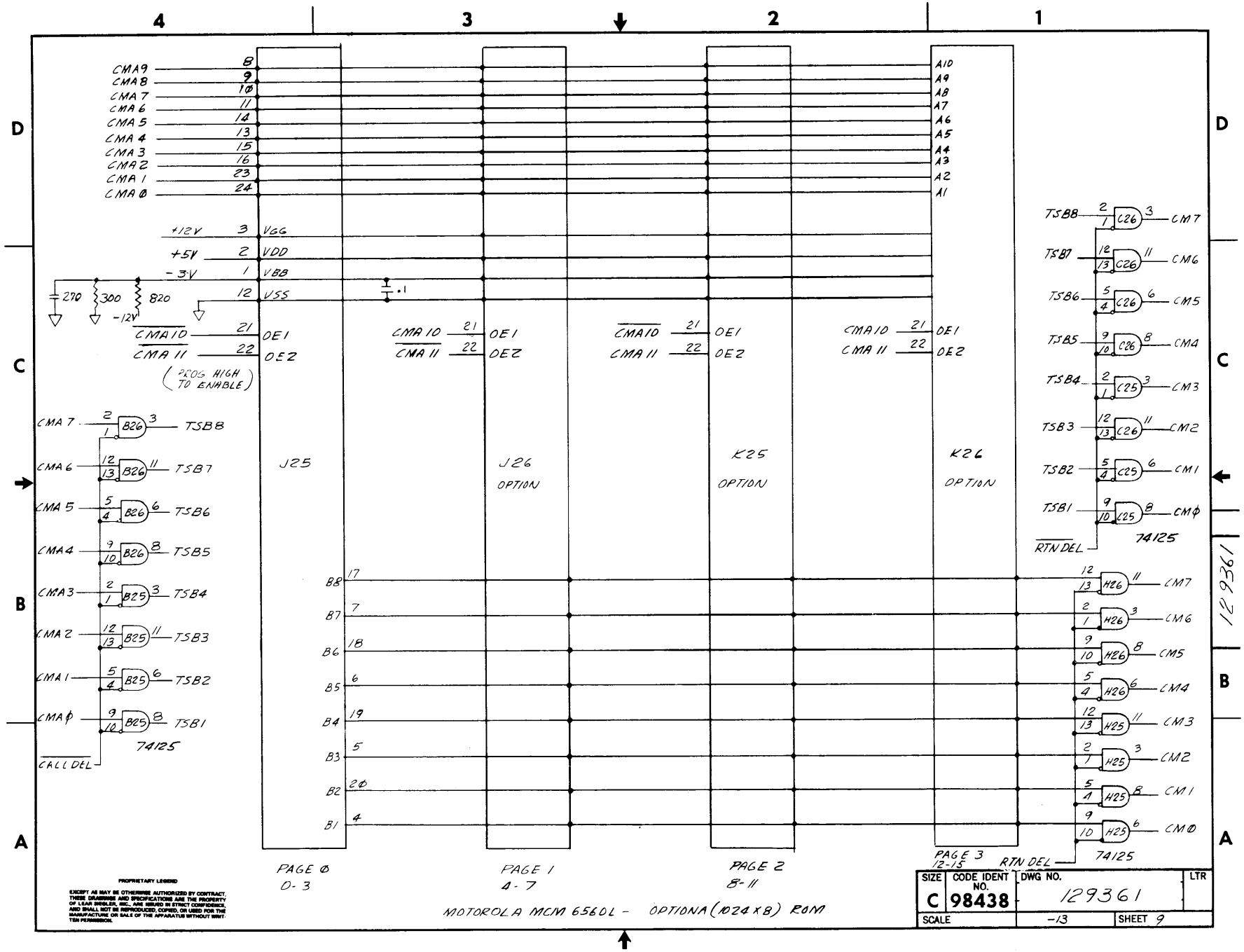
SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE		-13	SHEET 8

129361


4
3
2
1
D
C
B
A
CMA9
CMA8
CMA7
CMA6
CMA5
CMA4
CMA3
CMA2
CMA1
CMA0
+12V
+5V
-3V
-12V
270
300
820
.1
VGG
VDD
VBB
VSS
CMA10
CMA11
OE1
OE2
(PROG HIGH TO ENABLE)
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
J25
J26
OPTION
K25
OPTION
K26
OPTION
B26
B25
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
74125
CALL DEL
B8
B7
B6
B5
B4
B3
B2
B1
C26
C25
CM7
CM6
CM5
CM4
CM3
CM2
CM1
CM0
RTN DEL
H26
H25
PAGE 0
0-3
PAGE 1
4-7
PAGE 2
8-11
PAGE 3
12-15
MOTOROLA MCM 6560L - OPTION A (1024 X 8) ROM
PROPRIETARY LEGEND
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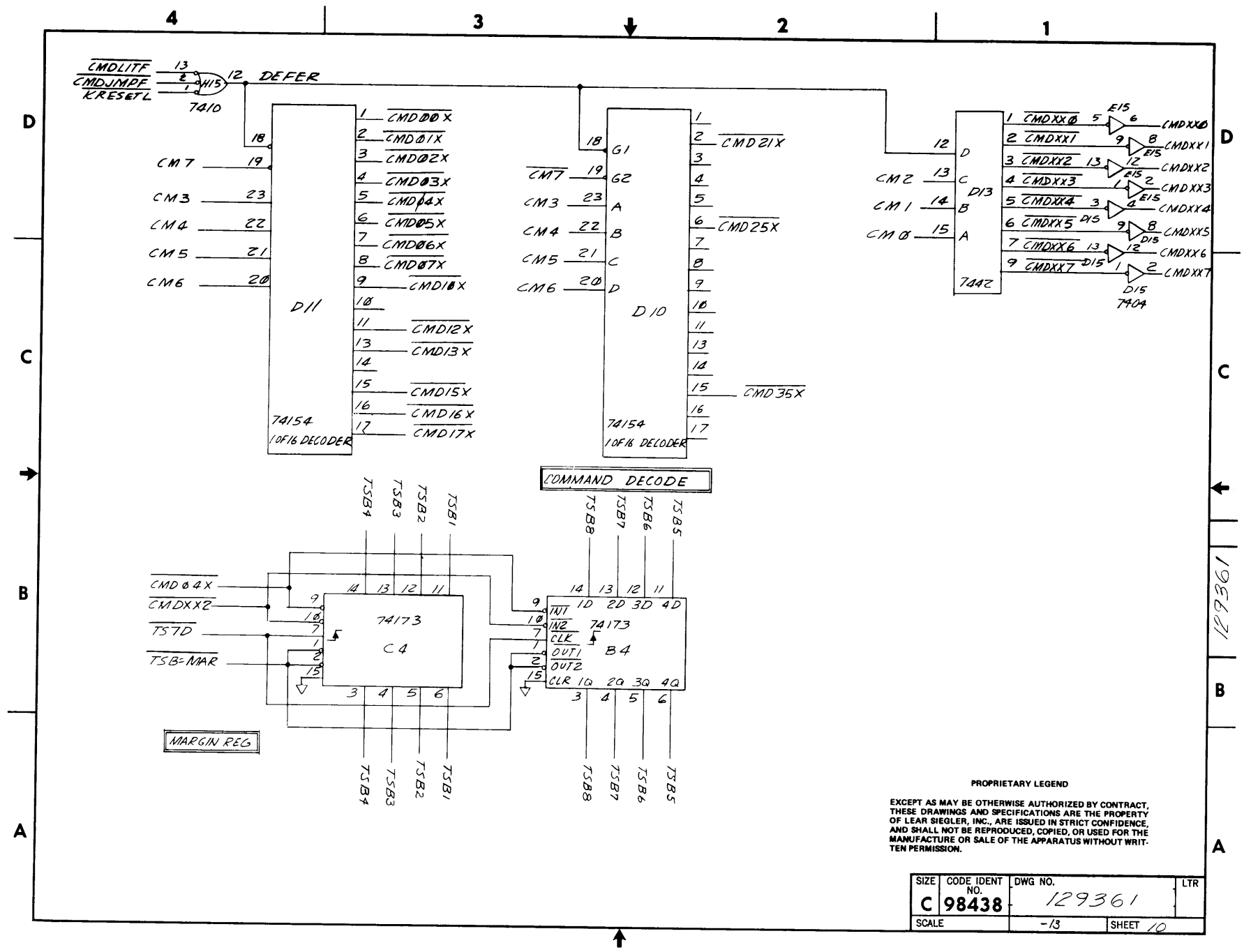
SIZE
C
CODE IDENT NO.
98438
DWG NO.
129361
LTR
SCALE
-13
SHEET 9


CMDLITF
CMDJMPF
KRESETL
H15
7410
DEFER
D11
74154
1OF16 DECODER
CM7
CM3
CM4
CM5
CM6
CMD00X
CMD01X
CMD02X
CMD03X
CMD04X
CMD05X
CMD06X
CMD07X
CMD10X
CMD12X
CMD13X
CMD15X
CMD16X
CMD17X
D10
G1
G2
A
B
C
D
CMD21X
CMD25X
CMD35X
COMMAND DECODE
D13
7442
CM2
CM1
CM0
CMDXX0
CMDXX1
CMDXX2
CMDXX3
CMDXX4
CMDXX5
CMDXX6
CMDXX7
E15
D15
7404
TSB4
TSB3
TSB2
TSB1
TSB8
TSB7
TSB6
TSB5
CMD04X
CMDXX2
TS7D
TSB=MAR
74173
C4
B4
MARGIN REG
PROPRIETARY LEGEND
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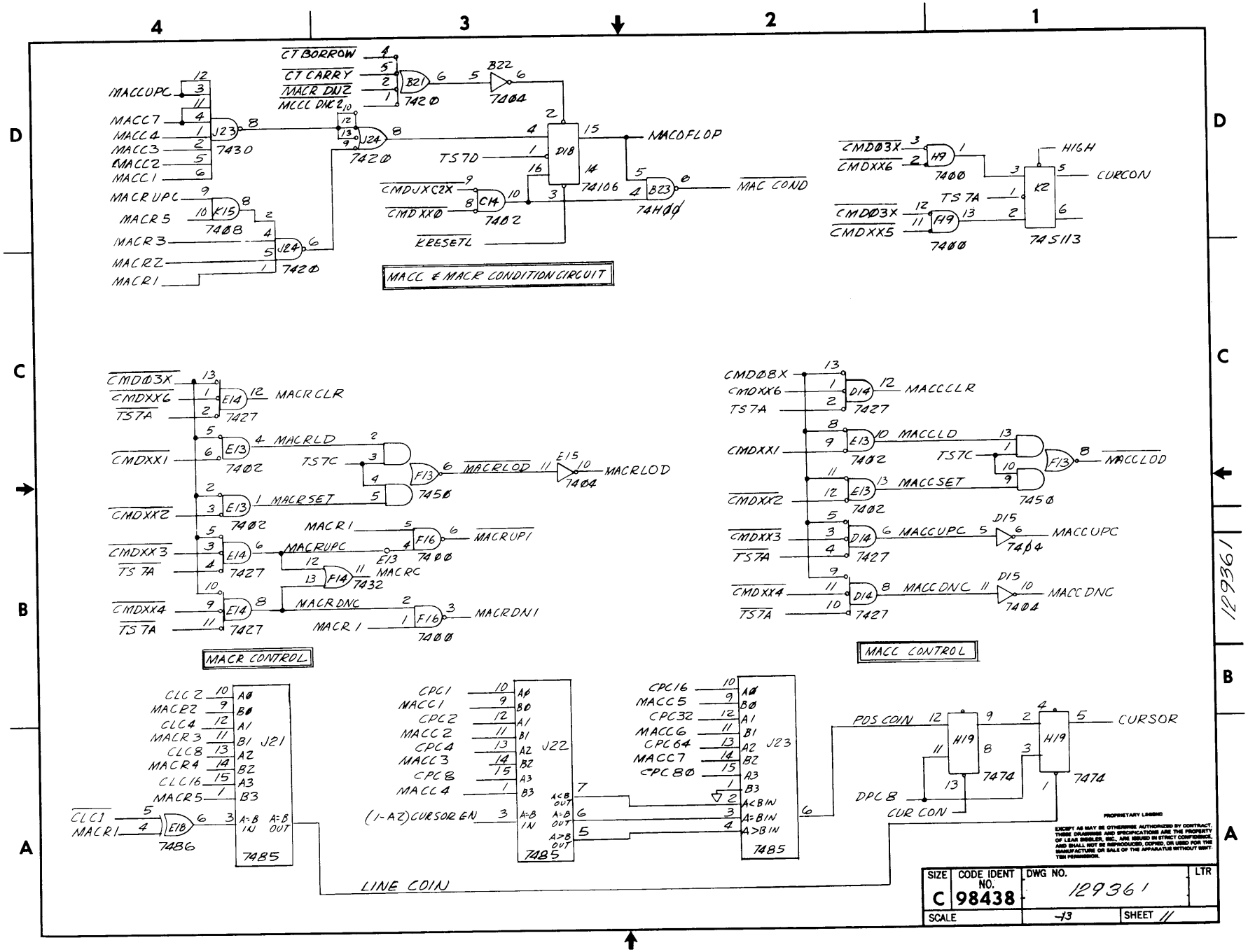
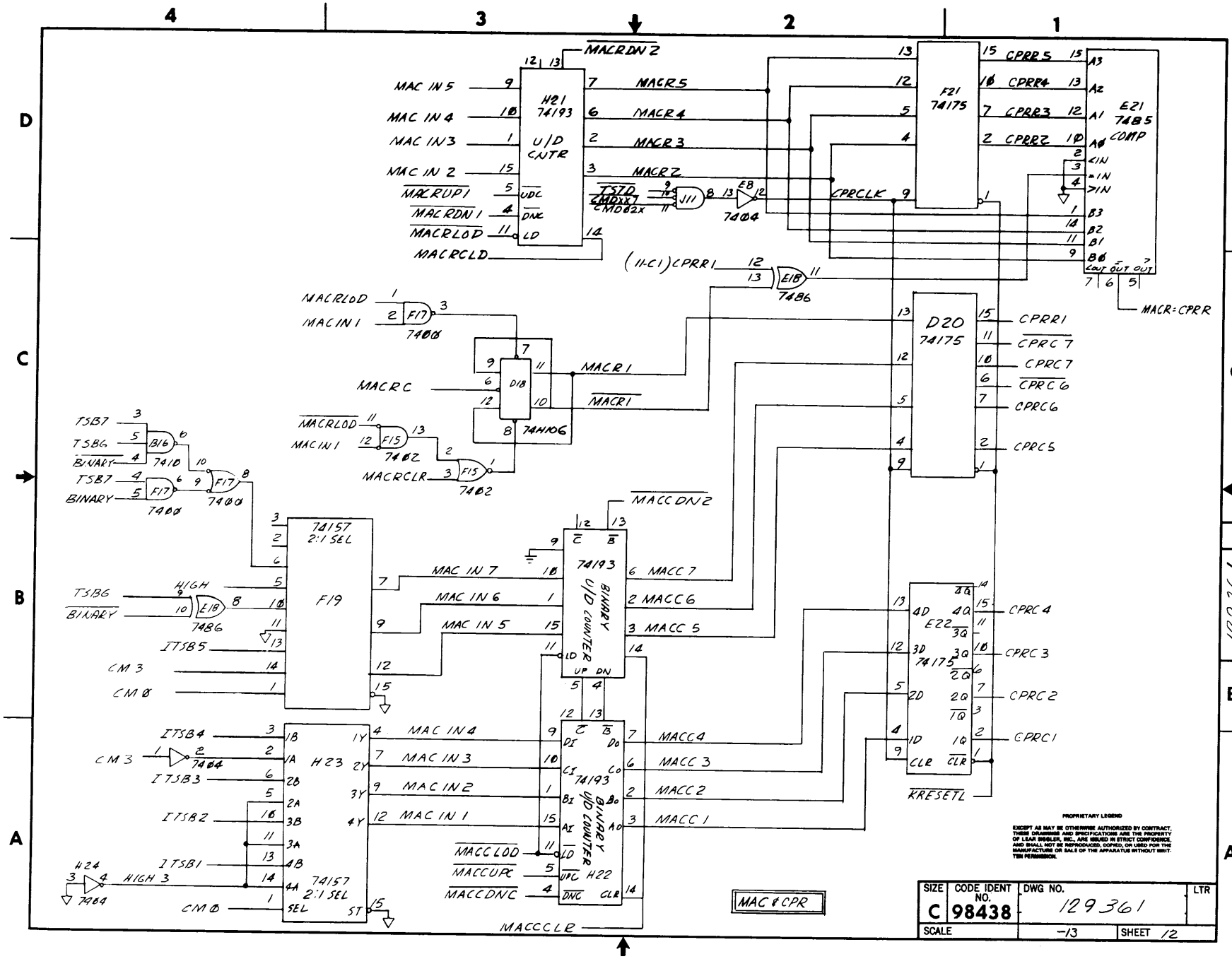
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE
-13
SHEET 10


MACC & MACR CONDITION CIRCUIT
MACR CONTROL
MACC CONTROL
MACCUPC
MACC7
MACC4
MACC3
MACC2
MACC1
MACRUPC
MACR5
MACR3
MACR2
MACR1
CT BORROW
CT CARRY
MACR DNZ
MCCC DNZ
TS7D
CMDJXC2X
CMDXX0
KRESETL
MACOFLOP
MAC COND
CMD03X
CMDXX6
HIGH
CURCON
TS7A
CMDXX5
CMD08X
MACCCLR
CMDXX1
MACCLD
TS7C
CMDXX2
MACCSET
CMDXX3
MACCUPC
CMDXX4
MACCDNC
MACRCLR
MACRLD
MACRLOD
MACRSET
MACRUPC
MACRC
MACRDNC
MACRDN1
CLC2
CLC4
CLC8
CLC16
CLC1
(1-A2)CURSOR EN
CPC1
CPC2
CPC4
CPC8
CPC16
CPC32
CPC64
CPC80
POS COIN
DPC8
CUR COIN
CURSOR
LINE COIN
PROPRIETARY LEGEND
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE -/3
SHEET //


MACRDN2
MAC IN 5
MAC IN 4
MAC IN 3
MAC IN 2
MACRUP1
MACRDN1
MACRLOD
MACRCLD
H21 74193 U/D CNTR
MACR5
MACR4
MACR3
MACR2
TST0
CMD01x
CMD02x
J11
E8
7404
CPRCLK
F21 74175
CPRR5
CPRR4
CPRR3
CPRR2
E21 7485 COMP
A>B
A=B
A<B
B3
B2
B1
B0
COUT OUT OUT
MACR=CPRR
(11-C1)CPRR1
E18
7486
MACRLOD
MACIN1
F17
7400
D18
MACR1
MACR
74H106
F15
7402
MACRCLR
TSB7
TSBG
BINARY
B16
7410
MACCDN2
74157 2:1 SEL F19
HIGH
MAC IN 7
MAC IN 6
MAC IN 5
ITSB5
CM 3
CM 0
74193 U/D BINARY COUNTER
MACC 7
MACC 6
MACC 5
D20 74175
CPRR1
CPRC 7
CPRC7
CPRC6
CPRC5
E22 74175
CPRC 4
CPRC 3
CPRC 2
CPRC 1
KRESETL
ITSB4
ITSB3
ITSB2
ITSB1
H24
HIGH 3
H23 74157 2:1 SEL
MAC IN4
MAC IN 3
MAC IN2
MAC IN 1
MACC4
MACC 3
MACC2
MACC 1
MACCLOD
MACCUP
MACCDNC
H22
MACCCLR
MAC & CPR
PROPRIETARY LEGEND
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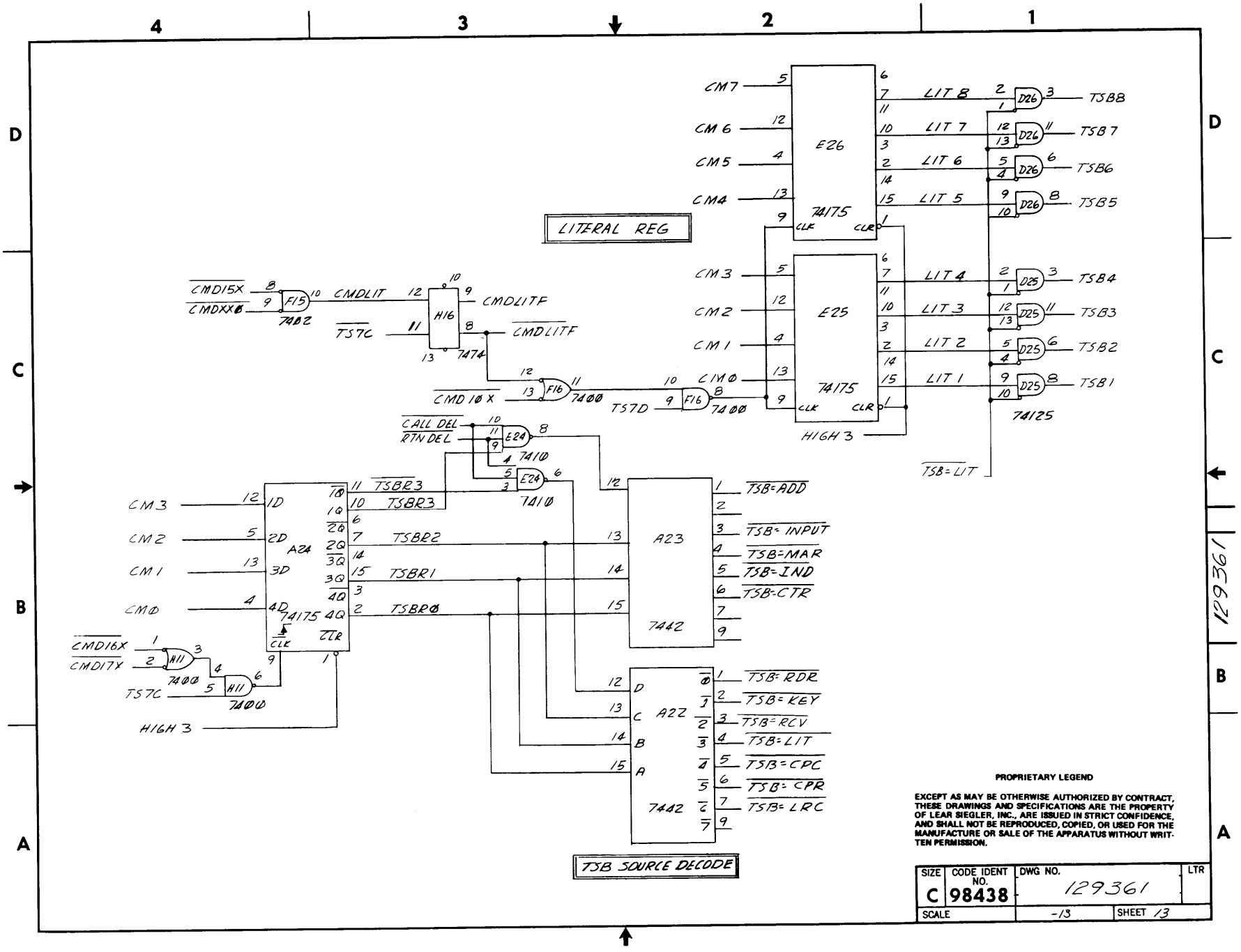
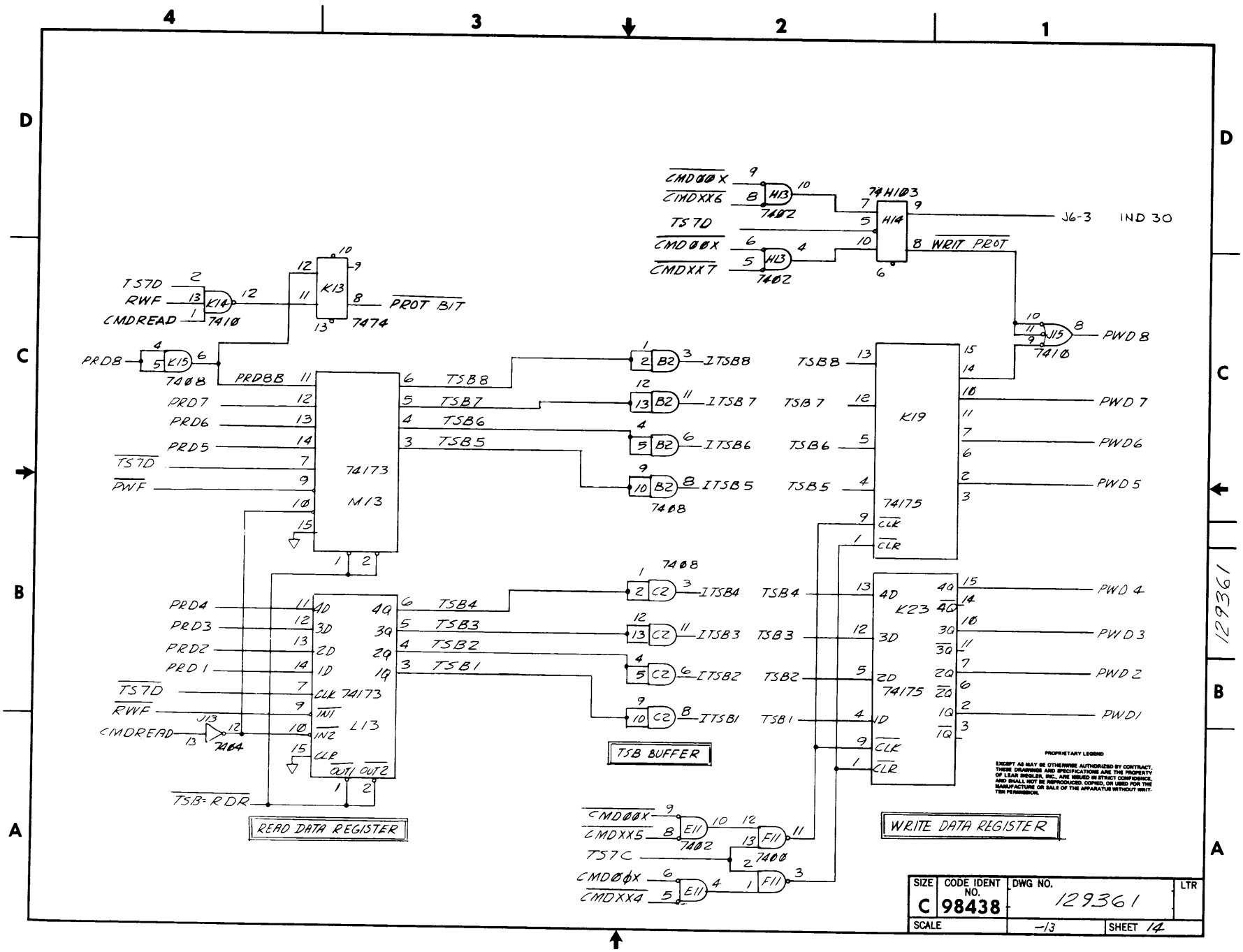
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE
-13
SHEET 12



SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE	-13	SHEET 13	


CMD00X
CMDXX6
7402
74H103
H14
J6-3 IND 30
TS7D
CMD00X
CMDXX7
8 WRIT PROT
PWD 8
TS7D
RWF
CMDREAD
7410
K13
7474
PROT BIT
PRD8
K15
7408
PRDBB
PRD7
PRD6
PRD5
TS7D
RWF
74173
M13
TSB8
TSB7
TSB6
TSB5
ITSB8
ITSB7
ITSB6
ITSB5
TSB8
TSB7
TSB6
TSB5
K19
74175
PWD 7
PWD6
PWD5
PRD4
PRD3
PRD2
PRD1
TS7D
RWF
CMDREAD
7404
L13
TSB4
TSB3
TSB2
TSB1
ITSB4
ITSB3
ITSB2
ITSB1
TSB4
TSB3
TSB2
TSB1
K23
PWD 4
PWD 3
PWD 2
PWD1
TSB=RDR
READ DATA REGISTER
TSB BUFFER
WRITE DATA REGISTER
CMD00X
CMDXX5
TS7C
CMD0ϕX
CMDXX4
E11
F11
7400
PROPRIETARY LEGEND
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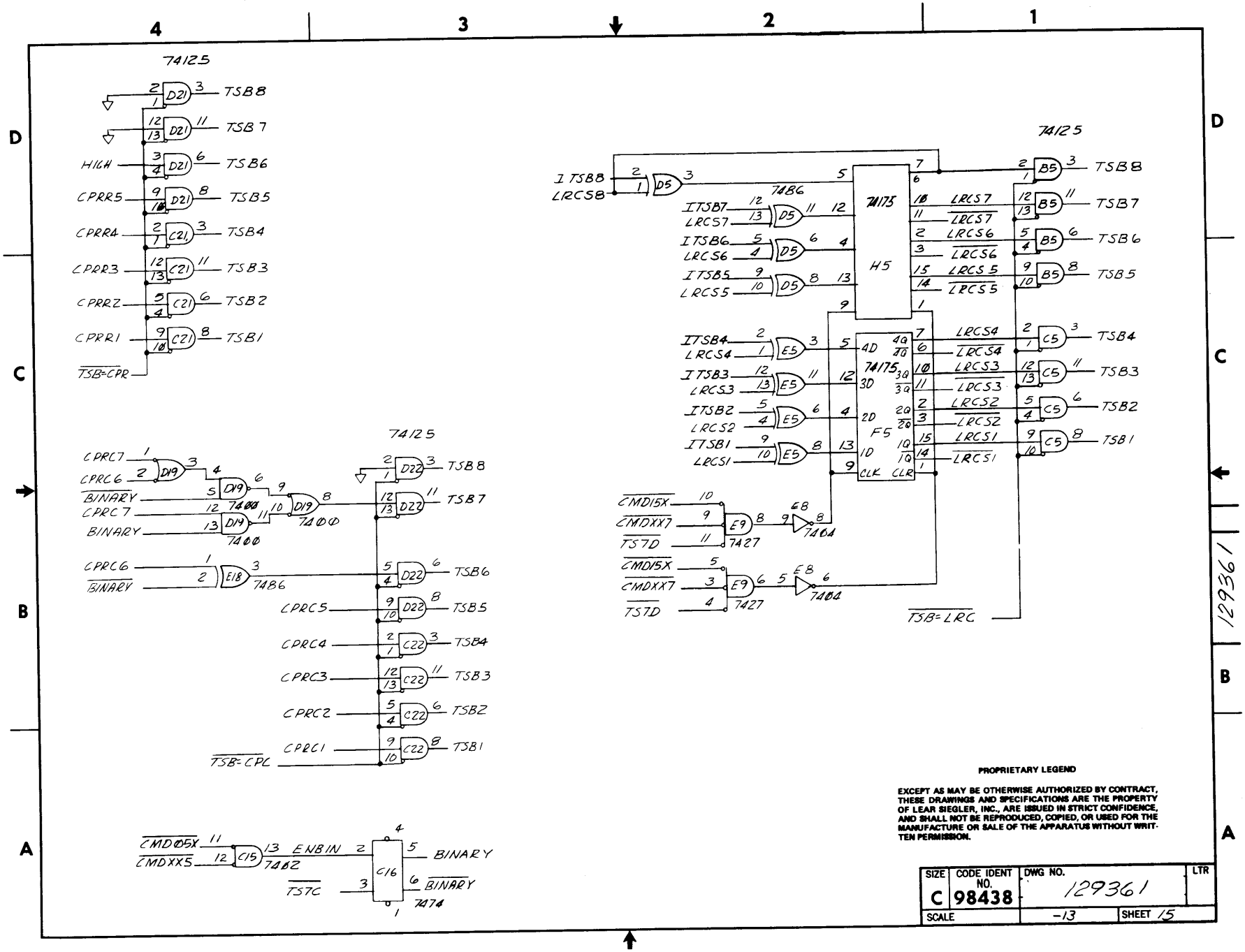
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE -13
SHEET 14


4
3
2
1
D
C
B
A
74125
TSB8
TSB7
HIGH
TSB6
CPRR5
TSB5
CPRR4
TSB4
CPRR3
TSB3
CPRR2
TSB2
CPRR1
TSB1
TSB=CPR
74125
CPRC7
CPRC6
BINARY
CPRC7
BINARY
7400
7400
CPRC6
BINARY
7486
CPRC5
CPRC4
CPRC3
CPRC2
CPRC1
TSB=CPC
CMD05X
CMDXX5
ENBIN
7402
C16
TS7C
BINARY
BINARY
7474
ITSB8
LRCS8
7486
ITSB7
LRCS7
ITSB6
LRCS6
ITSB5
LRCS5
74175
H5
ITSB4
LRCS4
ITSB3
LRCS3
ITSB2
LRCS2
ITSB1
LRCS1
4D
3D
2D
1D
CLK
4Q
3Q
2Q
1Q
CLR
F5
CMD15X
CMDXX7
TS7D
7427
7404
CMD15X
CMDXX7
TS7D
7427
7404
74125
LRCS7
LRCS6
LRCS5
LRCS4
LRCS3
LRCS2
LRCS1
TSB=LRC
PROPRIETARY LEGEND
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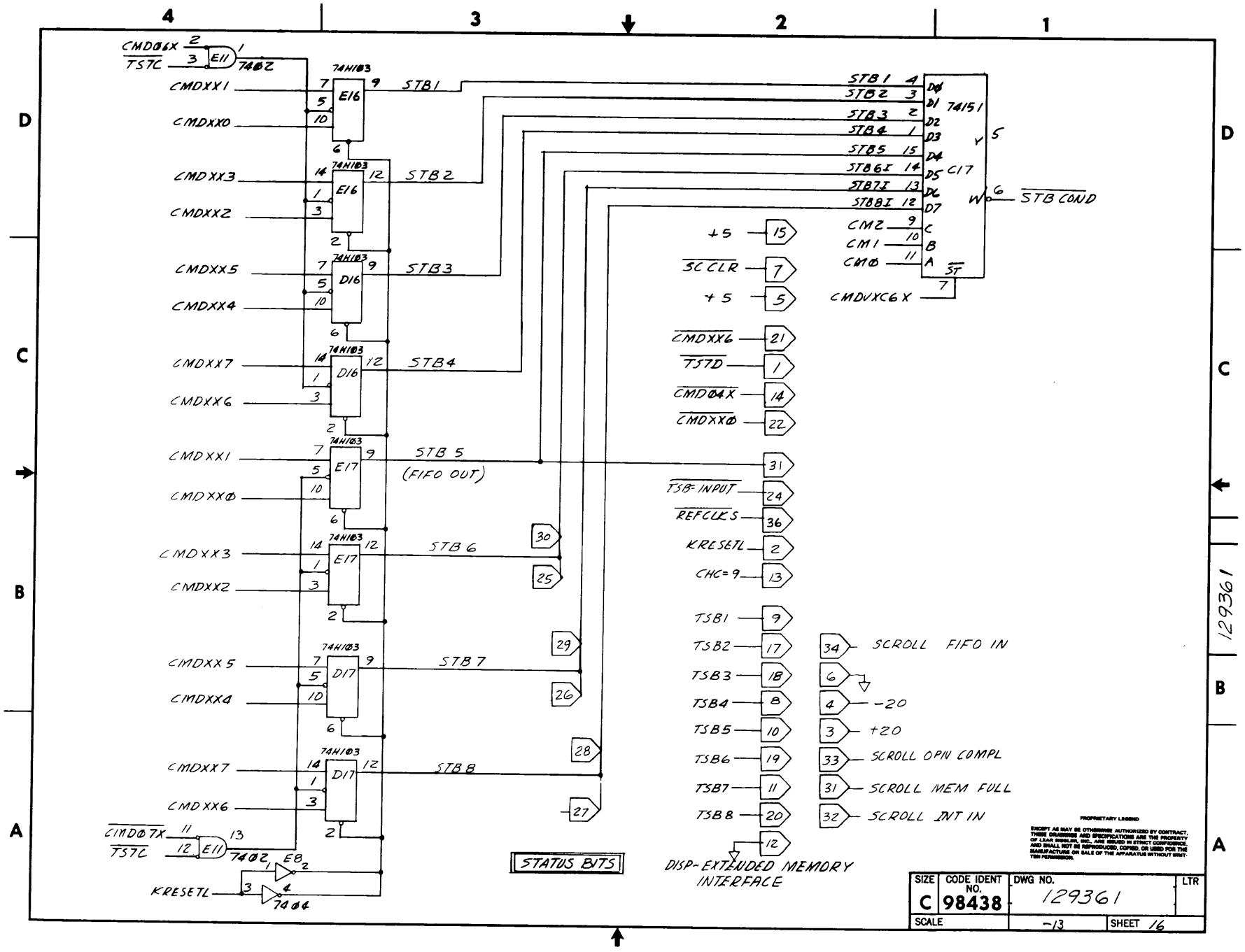
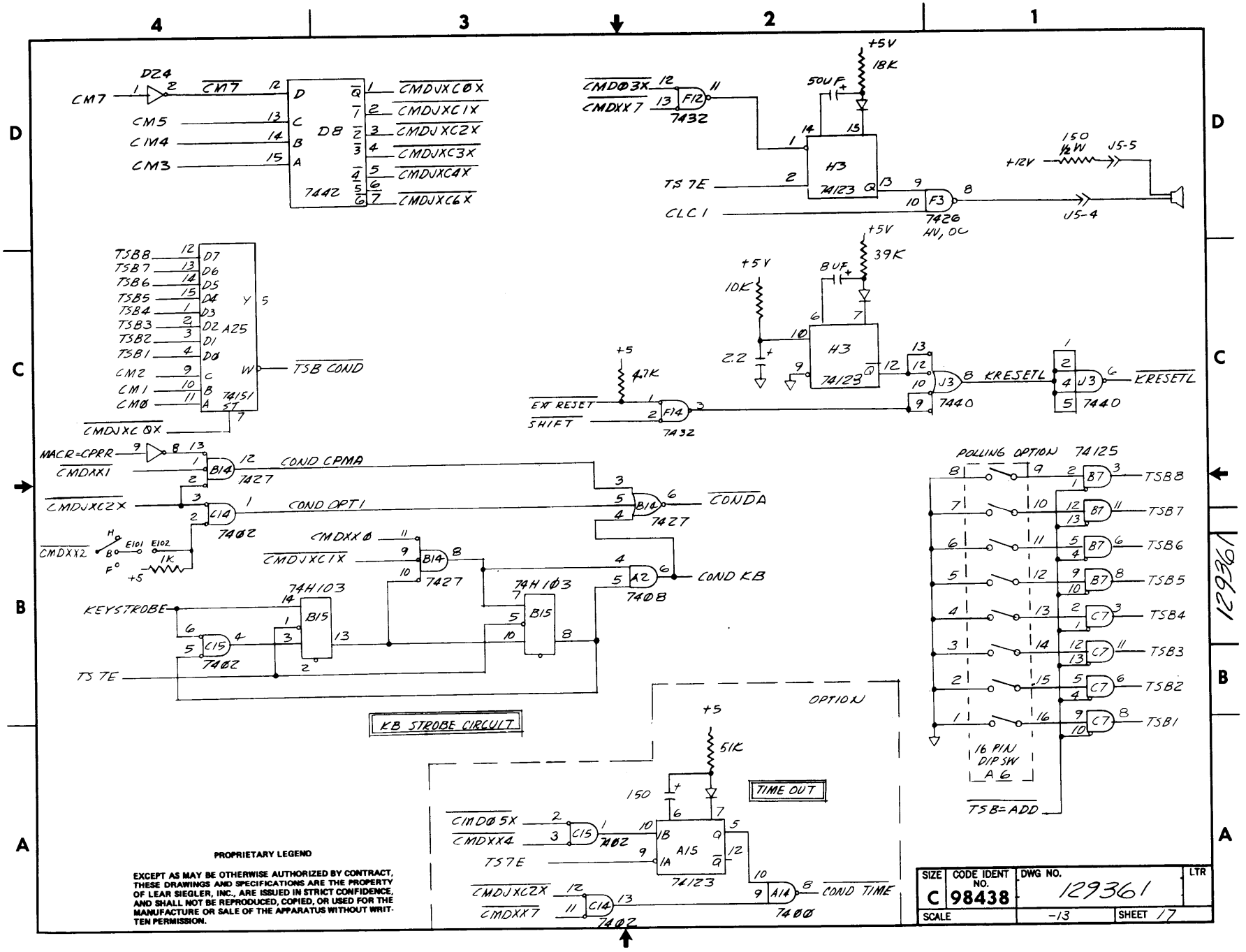
SIZE
C
CODE IDENT NO.
98438
DWG NO.
129361
LTR
SCALE
-13
SHEET 15


CMD06X
TST C
E11
74802
74H103
E16
CMDXX1
CMDXX0
STB1
CMDXX3
CMDXX2
STB2
CMDXX5
CMDXX4
D16
STB3
CMDXX7
CMDXX6
STB4
E17
STB 5
(FIFO OUT)
CMDXX3
CMDXX2
STB 6
D17
CMDXX5
CMDXX4
STB 7
CMDXX7
CMDXX6
STB 8
CMD07X
TST C
74802
E8
KRESETL
7404
STATUS BITS
STB1
STB2
STB3
STB4
STB5
STB6I
STB7I
STB8I
74151
C17
STB COND
CM2
CM1
CM0
CMDUXC6X
+5
SCCLR
+5
CMDXX6
TSTD
CMD04X
CMDXX0
TSB=INPUT
REFCLKS
KRESETL
CHC=9
TSB1
TSB2
TSB3
TSB4
TSB5
TSB6
TSB7
TSB8
SCROLL FIFO IN
-20
+20
SCROLL OPN COMPL
SCROLL MEM FULL
SCROLL INT IN
DISP-EXTENDED MEMORY INTERFACE
PROPRIETARY LEGEND
SIZE
CODE IDENT NO.
C
98438
DWG NO.
129361
LTR
SCALE
-/3
SHEET 16


4
3
2
1
D
C
B
A
D24
CM7
CM5
CM4
CM3
DB
7442
CMDJXC0X
CMDJXC1X
CMDJXC2X
CMDJXC3X
CMDJXC4X
CMDJXC6X
CMD03X
CMDXX7
7432
+5V
18K
50UF
H3
74123
TS7E
CLC1
7426
HV, OC
150
½W
+12V
J5-5
J5-4
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
CM2
CM1
CM0
A25
74151
TSB COND
CMDJXC0X
39K
10K
2.2
BUF
4.7K
EXT REJET
SHIFT
7440
KRESETL
MACR=CPRR
CMDAX1
CMDJXC2X
COND CPMA
COND OPT1
7427
7402
CONDA
CMDXX2
E101
E102
1K
CMDXX0
CMDJXC1X
74H103
74H103
KEYSTROBE
TS7E
7408
COND KB
KB STROBE CIRCUIT
OPTION
51K
150
TIME OUT
CIMD05X
CMDXX4
A15
CMDJXC2X
CMDXX7
COND TIME
7400
POLLING OPTION 74125
16 PIN DIP SW A6
TSB=ADD
PROPRIETARY LEGEND
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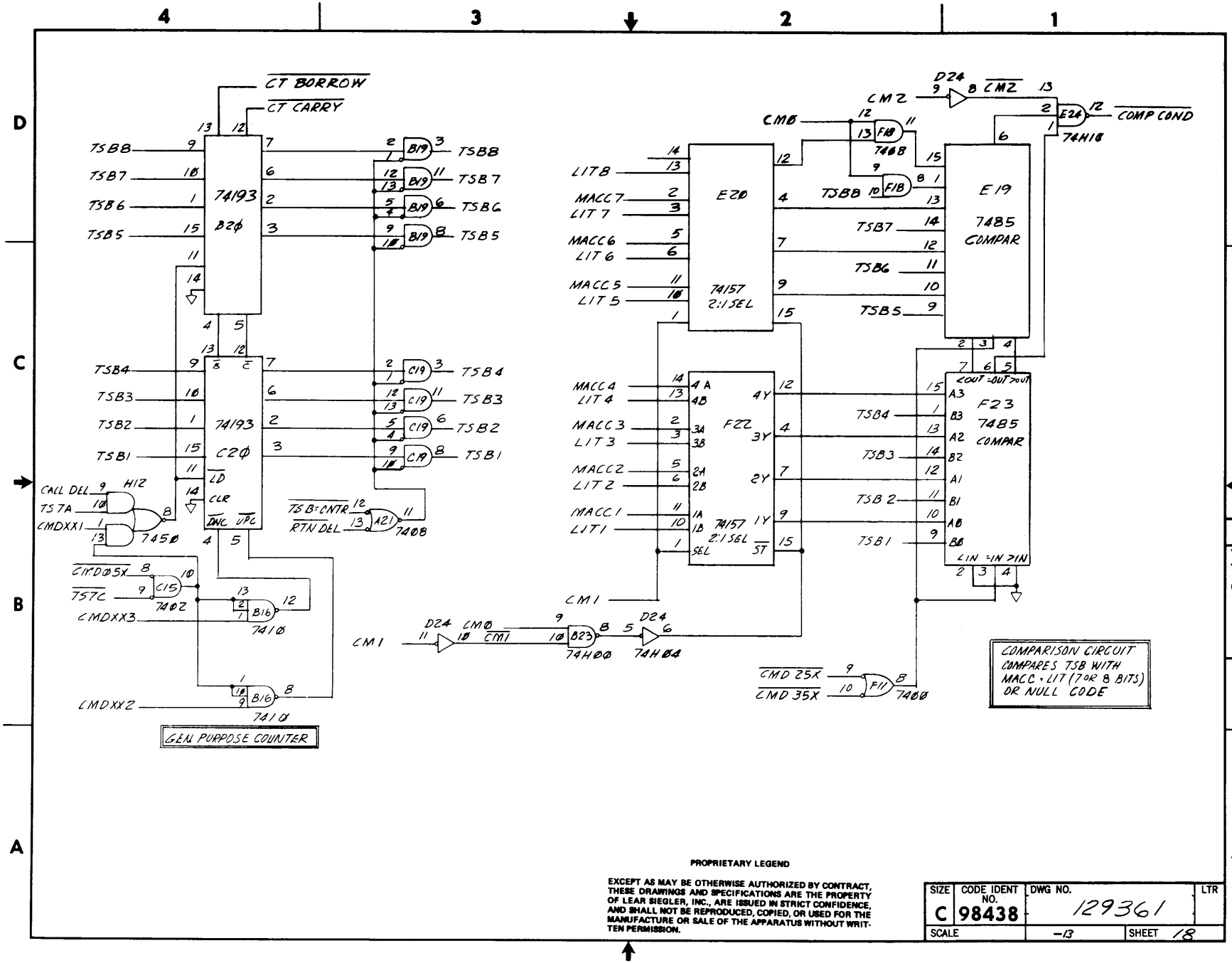
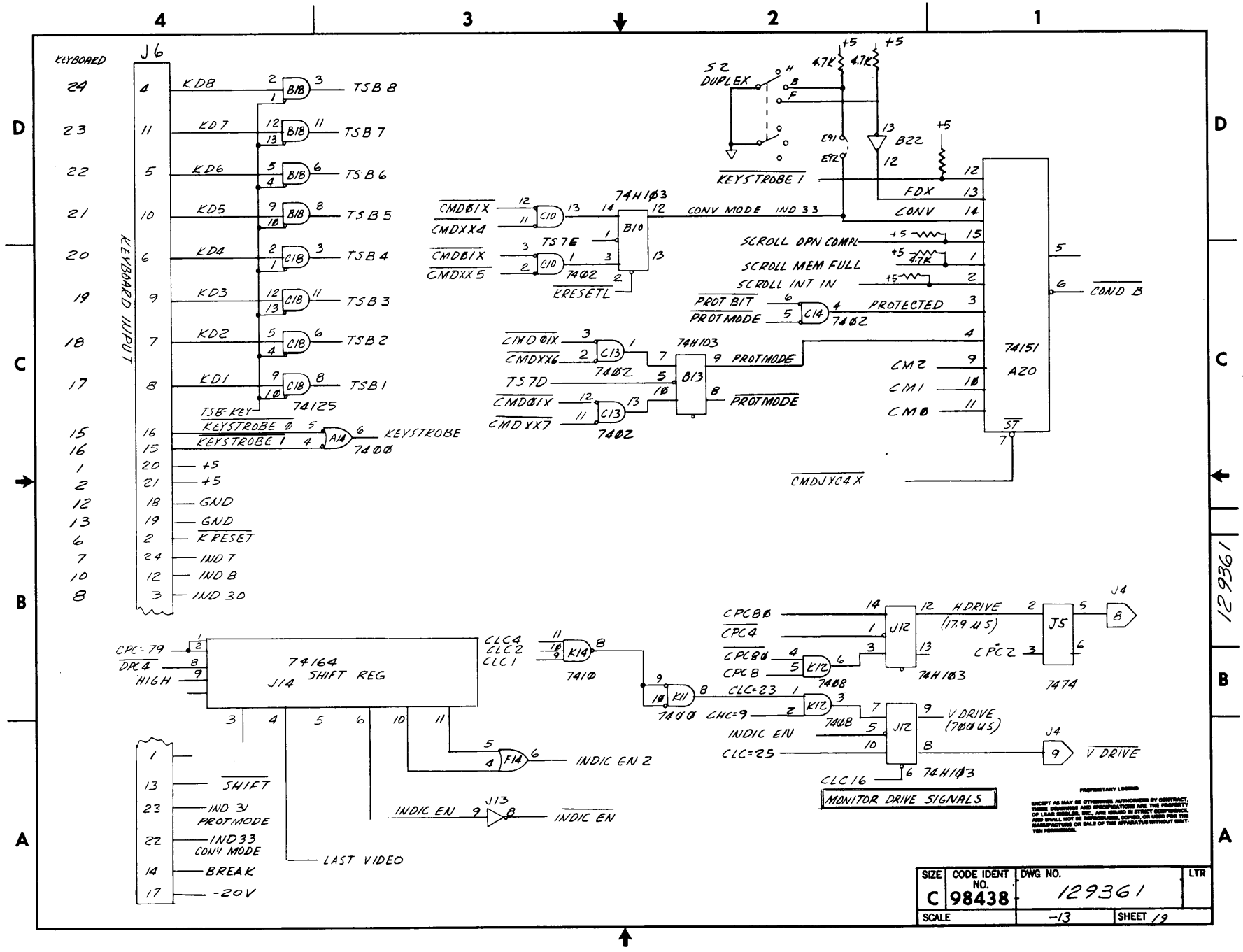
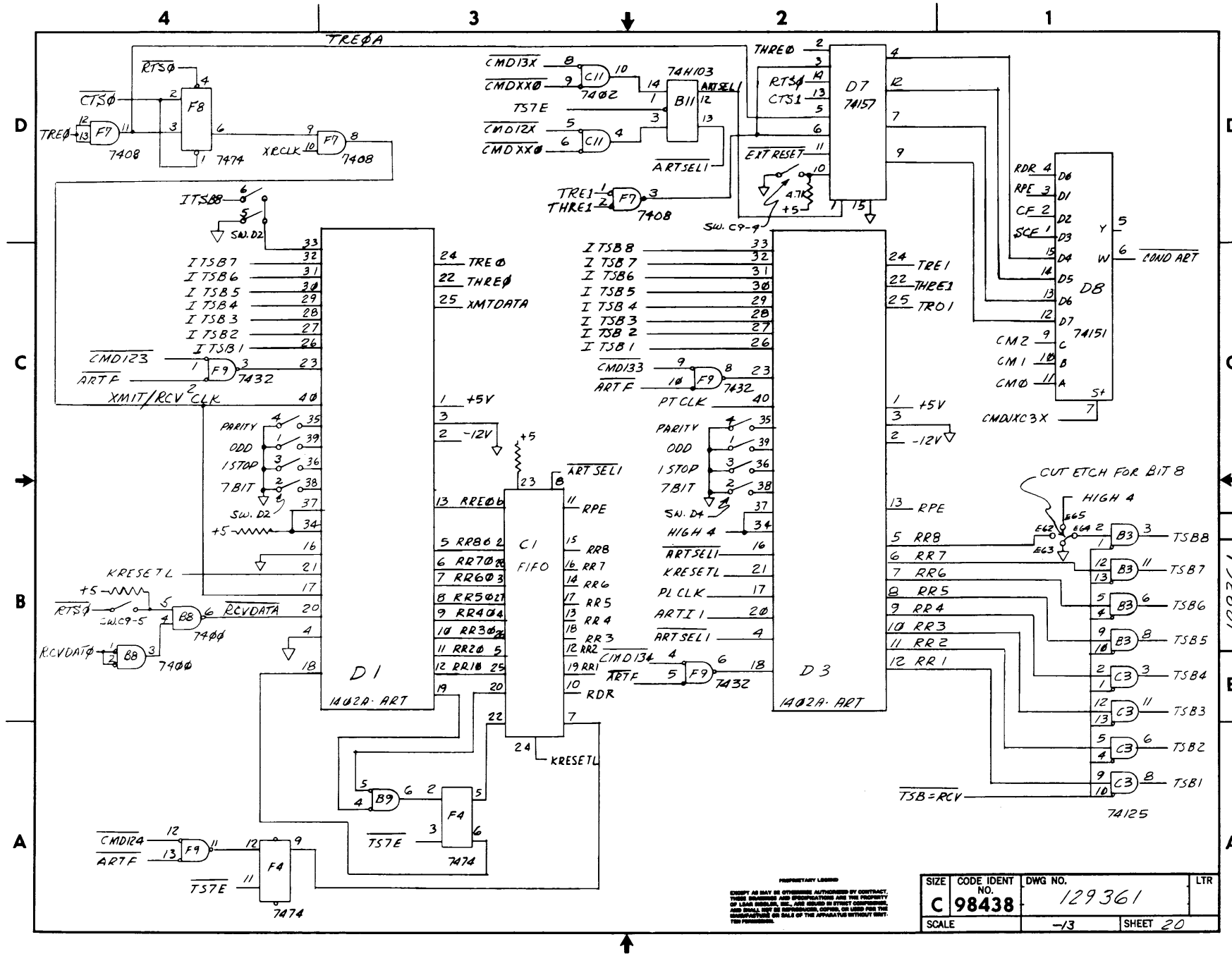
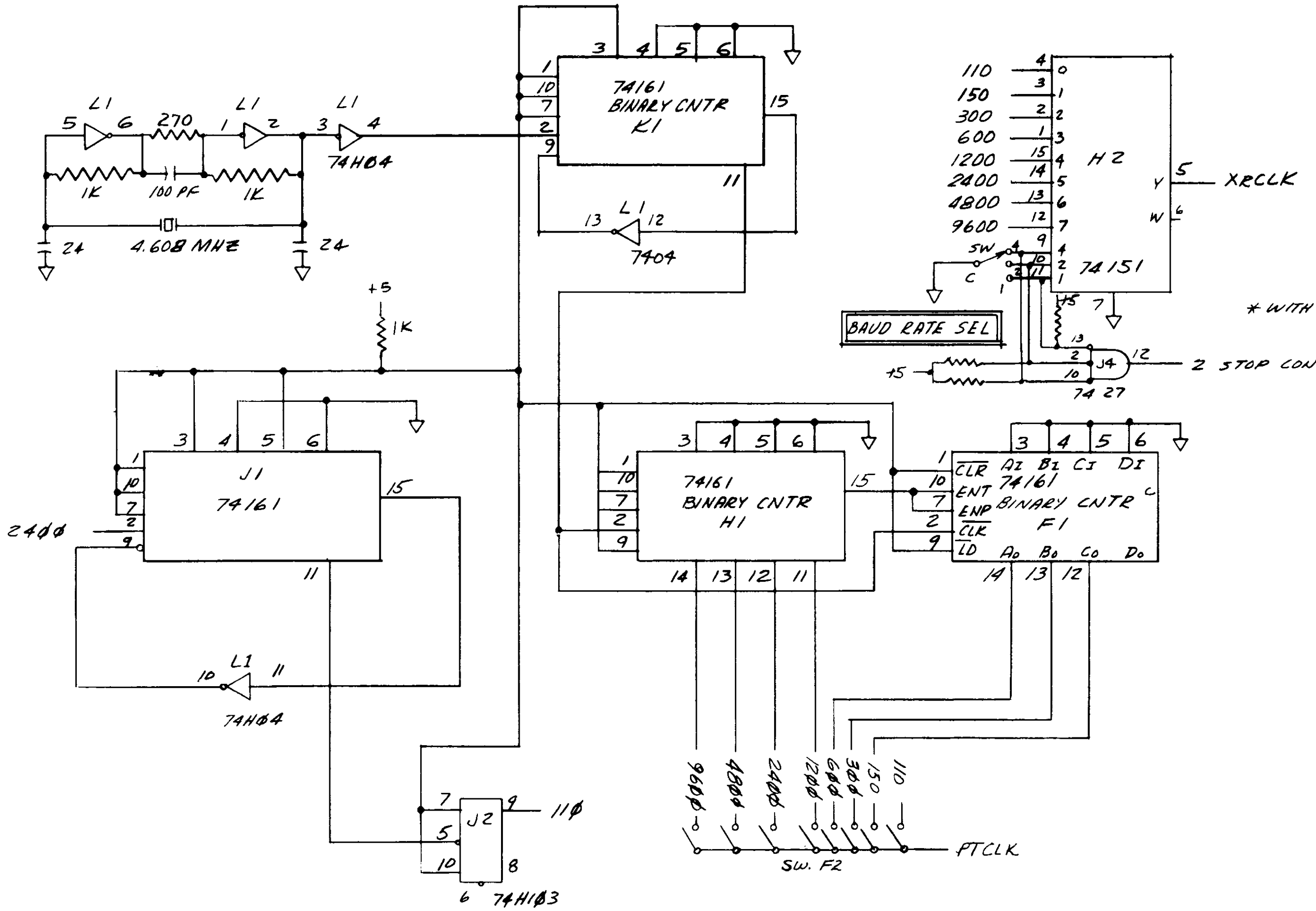
SIZE
C
CODE IDENT NO.
98438
DWG NO.
129361
LTR
SCALE
-13
SHEET 17



SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE		-13	SHEET 18


KEYBOARD
J6
KEYBOARD INPUT
KD8
KD7
KD6
KD5
KD4
KD3
KD2
KD1
TSB 8
TSB 7
TSB 6
TSB 5
TSB 4
TSB 3
TSB 2
TSB 1
74125
TSB=KEY
KEYSTROBE Ø
KEYSTROBE 1
KEYSTROBE
+5
GND
KRESET
IND 7
IND 8
IND 30
5Z DUPLEX
KEYSTROBE 1
B22
FDX
CONV
SCROLL OPN COMPL
SCROLL MEM FULL
SCROLL INT IN
PROT BIT
PROT MODE
PROTECTED
74151
A20
CMZ
CMI
CMØ
COND B
CMDJXC4X
CONV MODE IND 33
TS7E
KRESETL
TS7D
CMDXX4
CMDXX5
CMDXX6
CMDXX7
74H103
74Ø2
74Ø8
74Ø
74Ø74
74164
J14 SHIFT REG
CPC=79
DPC4
HIGH
CLC4
CLC2
CLC1
SHIFT
IND 3V PROTMODE
IND33 CONV MODE
BREAK
-20V
LAST VIDEO
INDIC EN 2
INDIC EN
CHC=9
CLC=23
CLC=25
CLC16
H DRIVE
(17.9 µS)
V DRIVE
(700 µS)
CPC2
MONITOR DRIVE SIGNALS
PROPRIETARY LEGEND
SIZE
C
CODE IDENT NO.
98438
DWG NO.
129361
LTR
SCALE
-13
SHEET 19


TREØA
RTSØ
CTSØ
TREØ
F8
F7
7408
7474
XRCLK
CMD13X
CMDXXØ
TS7E
CMD12X
CMDXXØ
C11
7402
74H103
B11
ARTSEL1
TRE1
THREI
THREØ
RTSØ
CTS1
D7
74157
EXT RESET
4.7K
+5
SW. C9-9
ITSB8
ITSB7
ITSB6
ITSB5
ITSB4
ITSB3
ITSB2
ITSB1
SW. D2
CMD123
ARTF
XMIT/RCV CLK
PARITY
ODD
1STOP
7BIT
KRESETL
RTSØ
SW. C9-5
B8
7400
RCVDATA
RCVDATØ
RCVDATA
D1
1402A-ART
TREØ
THREØ
XMTDATA
+5V
-12V
ARTSEL1
RREØ6
RPE
RR8
RR7
RR6
RR5
RR4
RR3
RR2
RR1
RDR
C1
FIFO
KRESETL
B9
F4
TS7E
7474
CMD124
ARTF
TS7E
F4
7474
ITSB8
ITSB7
ITSB6
ITSB5
ITSB4
ITSB3
ITSB2
ITSB1
CMD133
ARTF
PT CLK
PARITY
ODD
1STOP
7BIT
SW. D4
HIGH 4
ARTSEL1
KRESETL
PL CLK
ARTI1
ARTSEL1
CMD134
ARTF
F9
7432
D3
1402A-ART
TRE1
THREI
TRO1
+5V
-12V
RPE
RR8
RR7
RR6
RR5
RR4
RR3
RR2
RR1
RDR 4
RPE 3
CF 2
SCE 1
D8
74151
CM2
CM1
CMØ
CMDXC3X
CMD ART
CUT ETCH FOR BIT 8
HIGH 4
EG5
EG4
EG2
EG3
B3
C3
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
TSB=RCV
74125
PROPRIETARY LEGEND
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE -/3
SHEET 20



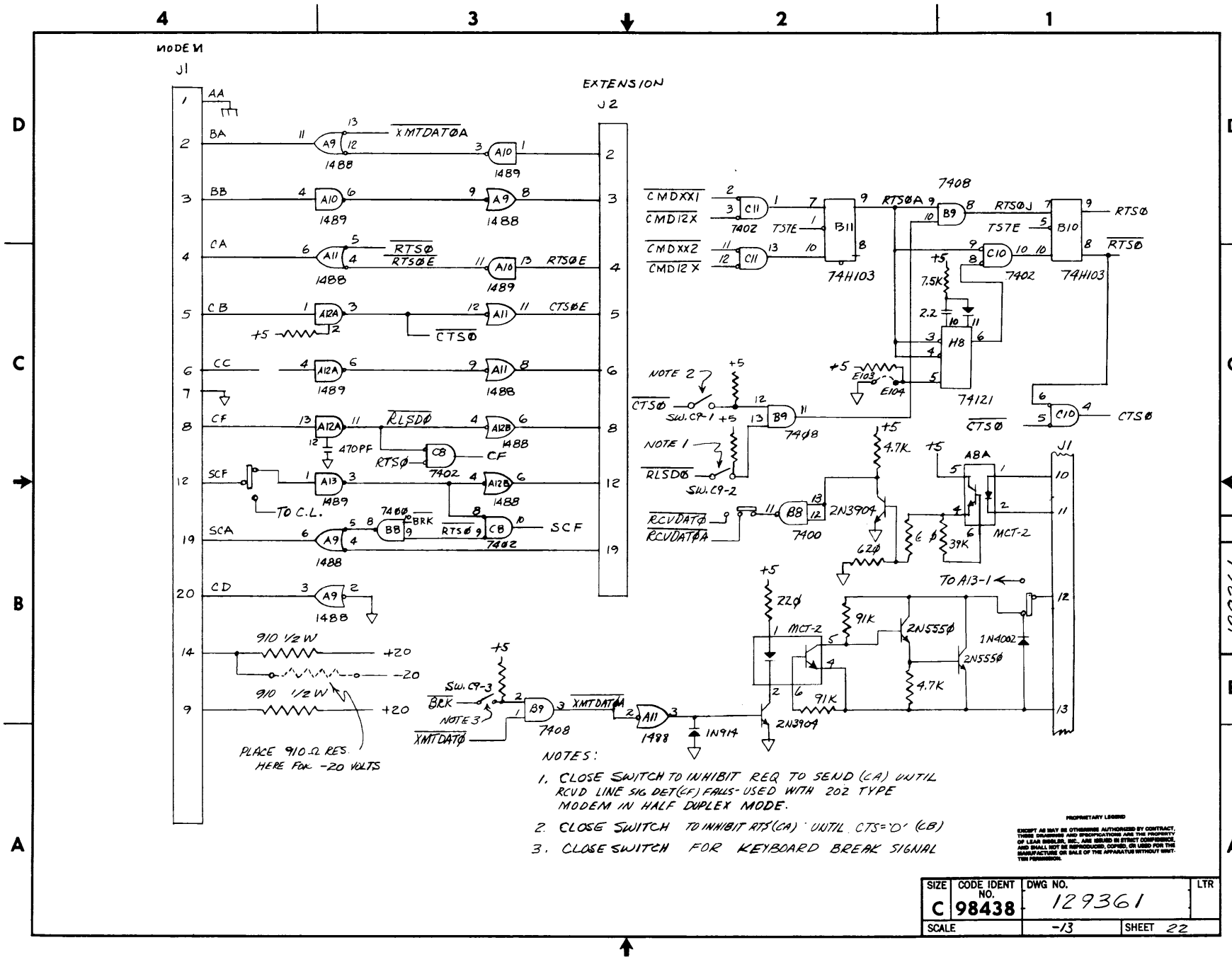
SW POS	SW CODE 1	2	4	ACT MUX	BAUD
0	1	1	1	7	9600
1	0	1	1	6	4800
2	1	0	1	5	2400
3	0	0	1	4	1200
4	1	1	0	3	600
5	0	1	0	2	300
6	1	0	0	1	150
7	0	0	0	0	110 *
8					
9					

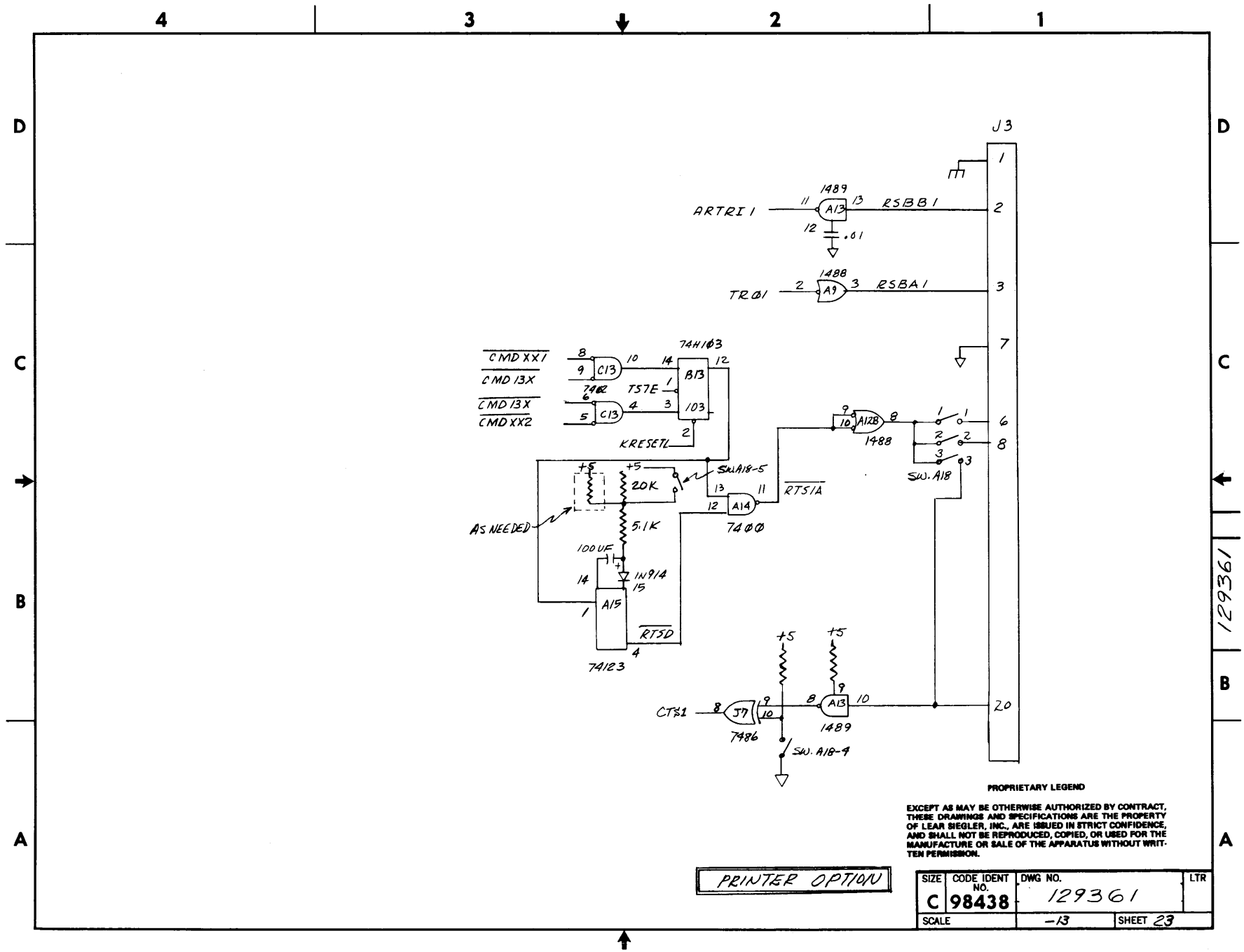
* WITH AUTOMATIC 2 STOP

E-44

129361

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129361	
SCALE		-13	SHEET 21


MODEM
J1
EXTENSION
J2
XMTDATØA
RTSØ
RTSØE
CTSØE
CTSØ
RLSDØ
470PF
CF
TO C.L.
BRK
SCF
SCA
CD
910 1/2 W
+20
-20
PLACE 910Ω RES. HERE FOR -20 VOLTS
CMDXX1
CMD12X
CMDXX2
CMD12X
7402
74H103
7408
RTSØA
RTSØJ
TSTE
7.5K
2.2
H8
74121
E103
E104
NOTE 2
SW.C9-1
NOTE 1
SW.C9-2
RLSDØ
4.7K
2N3904
RCVDATØ
RCVDATØA
7400
ABA
MCT-2
62Ø
39K
TO A13-1
22Ø
91K
2N5550
1N4002
Sw.C9-3
BRK
NOTE 3
XMTDATØ
XMTDATA
1488
1489
1N914
NOTES:
1. CLOSE SWITCH TO INHIBIT REQ TO SEND (CA) UNTIL RCVD LINE SIG DET(CF) FALLS- USED WITH 202 TYPE MODEM IN HALF DUPLEX MODE.
2. CLOSE SWITCH TO INHIBIT RTS(CA) UNTIL CTS='0' (CB)
3. CLOSE SWITCH FOR KEYBOARD BREAK SIGNAL
PROPRIETARY LEGEND
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE -13
SHEET 22


J3
ARTRI 1
1489
A13
RSBB 1
.01
TRØ1
1488
A9
RSBA 1
CMD XX1
CMD 13X
CMD 13X
CMD XX2
74H103
C13
B13
TS7E
7402
C13
103
KRESETL
SW.A18-5
20K
5.1K
AS NEEDED
100 UF
1N914
A15
RTS1A
A14
7400
RTS1D
74123
A12B
1488
SW. A18
CTS1
J7
7486
A13
1489
SW. A18-4
PROPRIETARY LEGEND
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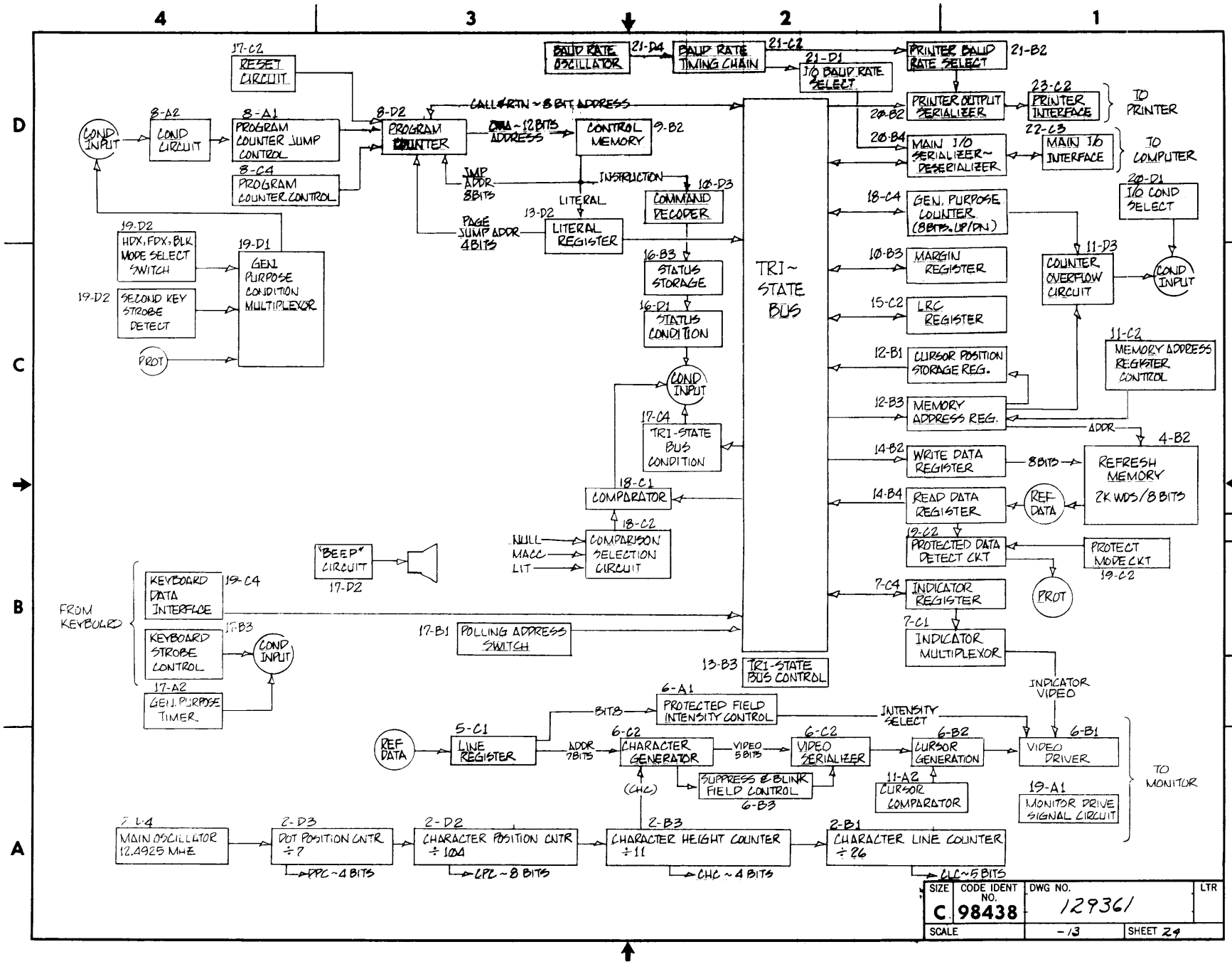
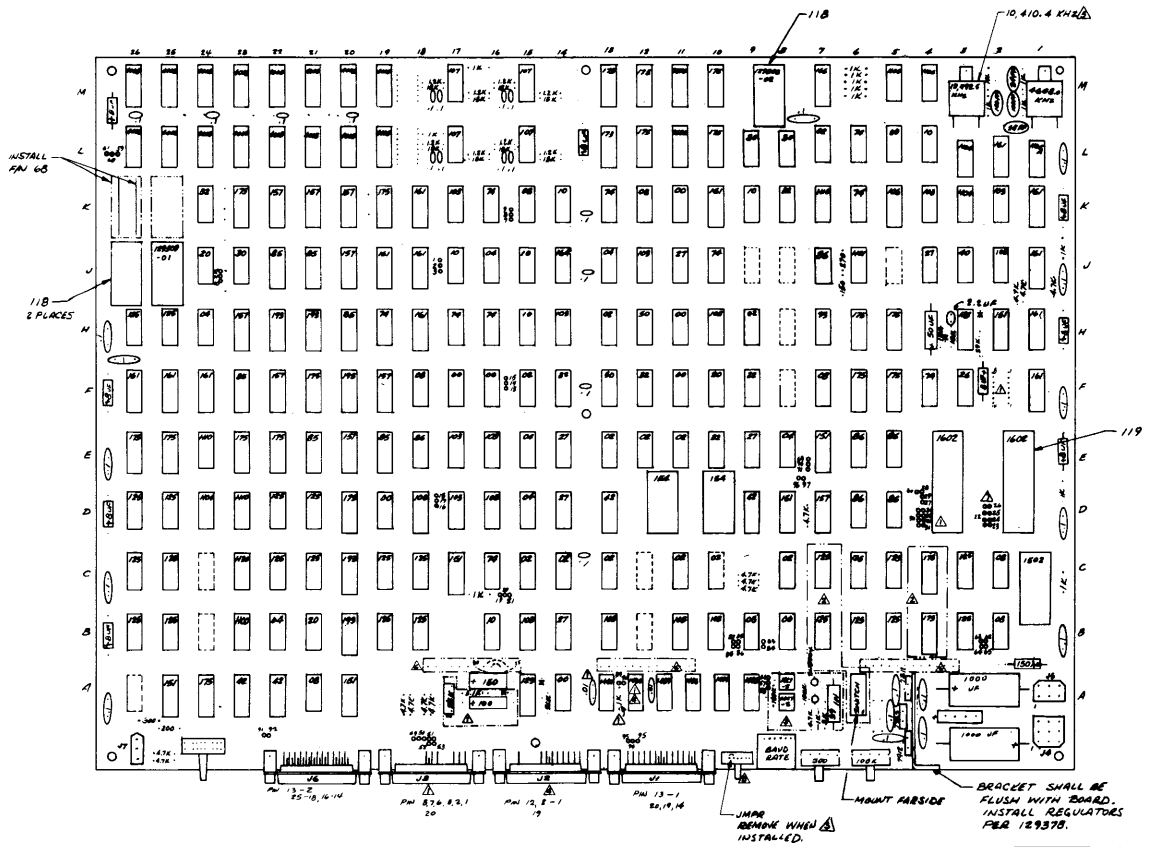
PRINTER OPTION
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE -13
SHEET 23


4
3
2
1
D
C
B
A
BAUD RATE OSCILLATOR
21-D4
BAUD RATE TIMING CHAIN
21-C2
I/O BAUD RATE SELECT
21-D1
PRINTER BAUD RATE SELECT
21-B2
17-C2
RESET CIRCUIT
8-A2
COND CIRCUIT
COND INPUT
8-A1
PROGRAM COUNTER JUMP CONTROL
8-C4
PROGRAM COUNTER CONTROL
8-D2
PROGRAM COUNTER
CALL RTN ~ 8 BIT ADDRESS
CMA ~ 12 BITS ADDRESS
9-B2
CONTROL MEMORY
IMP ADDR 8 BITS
INSTRUCTION
10-D3
COMMAND DECODER
LITERAL
13-D2
LITERAL REGISTER
PAGE JUMP ADDR 4 BITS
16-B3
STATUS STORAGE
16-D1
STATUS CONDITION
19-D2
HDX, FDX, BLK MODE SELECT SWITCH
19-D2
SECOND KEY STROKE DETECT
PROT
19-D1
GEN PURPOSE CONDITION MULTIPLEXOR
TRI-STATE BUS
20-B2
PRINTER OUTPUT SERIALIZER
23-C2
PRINTER INTERFACE
TO PRINTER
20-B4
MAIN I/O SERIALIZER-DESERIALIZER
22-C3
MAIN I/O INTERFACE
TO COMPUTER
20-D1
I/O COND SELECT
18-C4
GEN. PURPOSE COUNTER (8 BITS, UP/DN)
10-B3
MARGIN REGISTER
15-C2
LRC REGISTER
12-B1
CURSOR POSITION STORAGE REG.
12-B3
MEMORY ADDRESS REG.
11-D3
COUNTER OVERFLOW CIRCUIT
COND INPUT
11-C2
MEMORY ADDRESS REGISTER CONTROL
ADDR
4-B2
REFRESH MEMORY 2K WDS/8 BITS
14-B2
WRITE DATA REGISTER
8 BITS
14-B4
READ DATA REGISTER
REF DATA
19-C2
PROTECTED DATA DETECT CKT
PROTECT MODE CKT
19-C2
PROT
7-C4
INDICATOR REGISTER
7-C1
INDICATOR MULTIPLEXOR
INDICATOR VIDEO
17-C4
TRI-STATE BUS CONDITION
COND INPUT
18-C1
COMPARATOR
18-C2
COMPARISON SELECTION CIRCUIT
NULL
MACC
LIT
"BEEP" CIRCUIT
17-D2
FROM KEYBOARD
KEYBOARD DATA INTERFACE
19-C4
KEYBOARD STROBE CONTROL
17-B3
COND INPUT
17-A2
GEN. PURPOSE TIMER
17-B1
POLLING ADDRESS SWITCH
13-B3
TRI-STATE BUS CONTROL
6-A1
PROTECTED FIELD INTENSITY CONTROL
BITS
INTENSITY SELECT
REF DATA
5-C1
LINE REGISTER
ADDR 7 BITS
6-C2
CHARACTER GENERATOR
VIDEO 5 BITS
6-C2
VIDEO SERIALIZER
6-B2
CURSOR GENERATION
6-B1
VIDEO DRIVER
SUPPRESS & BLINK FIELD CONTROL
6-B3
(CHC)
11-A2
CURSOR COMPARATOR
19-A1
MONITOR DRIVE SIGNAL CIRCUIT
TO MONITOR
2-L4
MAIN OSCILLATOR 12.4925 MHz
2-D3
DOT POSITION CNTR ÷7
PPC ~ 4 BITS
2-D2
CHARACTER POSITION CNTR ÷104
CPC ~ 8 BITS
2-B3
CHARACTER HEIGHT COUNTER ÷11
CHC ~ 4 BITS
2-B1
CHARACTER LINE COUNTER ÷26
CLC ~ 5 BITS
SIZE C
CODE IDENT NO. 98438
DWG NO. 129361
LTR
SCALE
-13
SHEET 24

APPENDIX F: ADM-2 P.C. BOARD ASSEMBLY

REVISIONS					
SHT	ZONE	LTR	DESCRIPTION	DATE	APPROVED
		A	INC ADCN 1 SH 2 REDRAWN -5 REPLACED -3 W.J. Kelly 4-30-74	5/1/74	
		B	REMOVE 4.7K RES AT J34 & 1K AT A13 ADD JMPRS; ADD OPT 7; ADD NOTE FOR REL W.J. Kelly 5-8-74		



△PRINTER OPTION
△POLLING OPTION
△CURRENT LOOP OPTION
△RS232 EXTENSION OPTION
△50 HZ OPTION
△EXTENDED MEMORY OPTION
△WORD STRUCTURE

REF	INSTALL JUMPERS
	E1 - 2
	E8 - 9
	E10 - 11
	E14 - 15
	E17 - 18
△ 9 21	E19 - 20
	E26 - 22
△	E24 - 23
27 28 29 30	E28 - 30
△	
	E59 - 60
	E63 - 64
	E70 - 71
△ 83 84	E83 - 84
△	
△ 96 97	E96 - 97
	TERM 25 - 30
	26 - 29
	27 - 28

SH 2 IS N/A

-1 ASSY

DASH NO.	NEXT ASSY APPLICATION	USED ON
-1		

UNLESS OTHERWISE SPECIFIED
DIM. IN INCHES
TOLERANCES
X ± .1
XX ± .03
XXX ± .010
ANGLES ± 0.5°
MACH. FIN.

CONTR NO.
DR W J Kelly 2-25-74
CHK
DSGN
ENGR
PROJ
REL
APPD
APPD

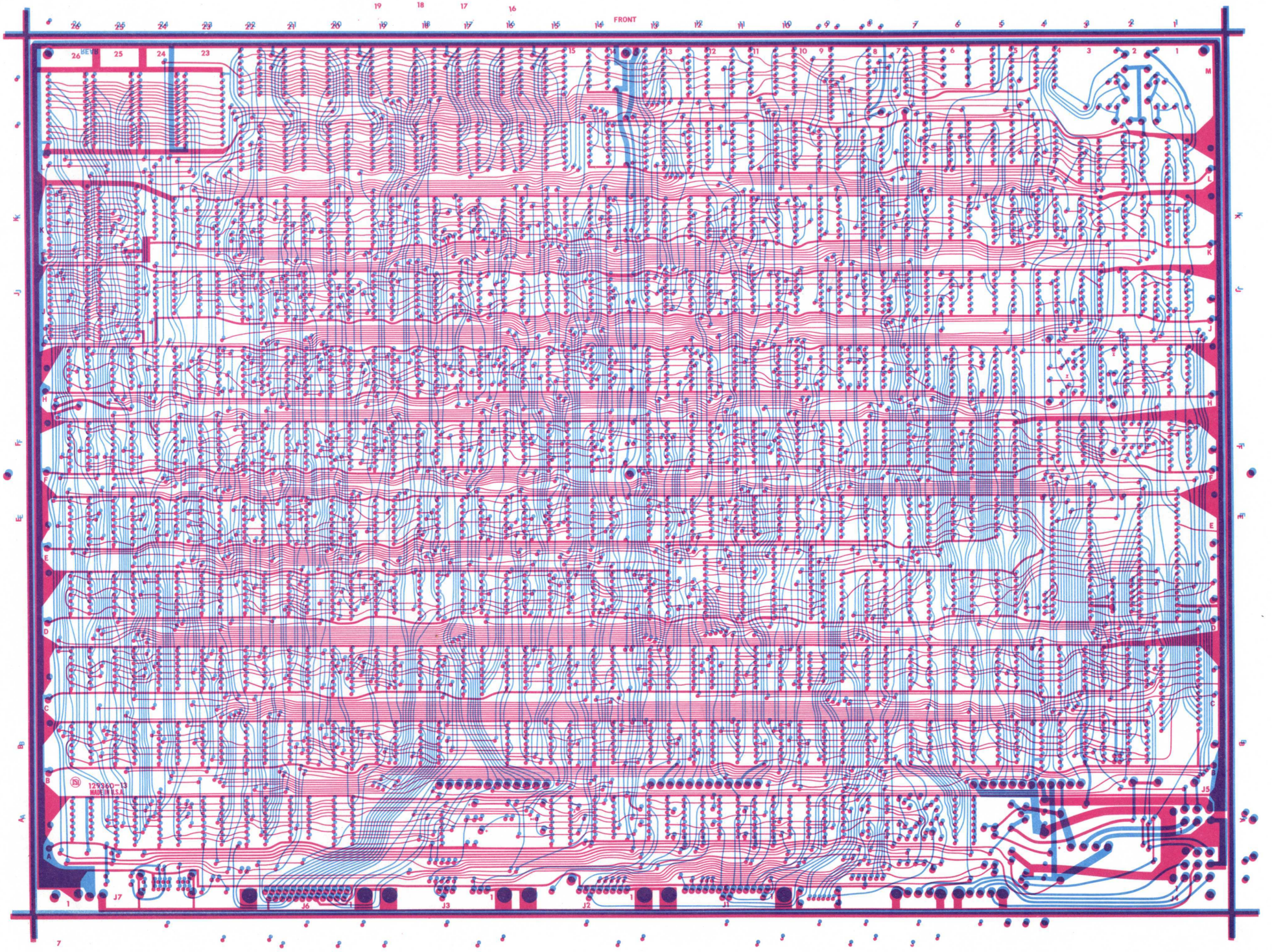
LEAR SIEGLER, INC.
ELECTRONIC INSTRUMENTATION DIVISION
ANAHEIM, CALIFORNIA 92803

PC BOARD ASSY
ADM-2

SIZE	CODE IDENT NO.	DWG NO.	LTR
D	98438	129360	B
SCALE 1/1		SHEET 1 OF 2	

129360

APPENDIX G: ADM-2 CIRCUIT BOARD


FRONT
REAR
J7
J6
J3
J2
J1
J4
J5
127360-13

OPERATOR'S QUICK REFERENCE GUIDE

ADM-2 CONTROL

FUNCTION	SEQUENCE
CURSOR ←	CTRL / H
CURSOR ↓	CTRL / J
CURSOR ↑	CTRL / K
CURSOR →	CTRL / L
HOME	HOME KEY
SKIP	CTRL / I
NEW LINE	NUMBERS KEY
PROTECT ON	ESC &
PROTECT OFF	ESC '
START WRITE PROTECT	ESC)
END WRITE PROTECT	ESC (
CLEAR ALL TO UNPROTECT SP	ESC +
SEND LINE UNPROTECT	ESC 4
SEND PAGE UNPROTECT	ESC 5
SEND LINE PROTECT	ESC 6
SEND PAGE PROTECT	ESC 7
CLEAR ALL TO NULL	ESC *
CLEAR PG TO NULL	ESC :
CLEAR PG TO SPACE	ESC ;
KEYBOARD ENABLE	ESC "
KEYBOARD DISABLE	ESC #
LOAD CURSOR	ESC =
READ CURSOR	ESC ?
ADM-2 MODE ON	ESC %
ADM-2 MODE OFF	ESC $
CHAR INSERT	ESC Q
CHAR DELETE	ESC W
LINE INSERT	ESC E
LINE DELETE	ESC R
LINE ERASE	ESC T
ERASE PAGE	ESC Y
PARTIAL SEND	ESC S
BACK TAB	ESC I
START/END BLINK FIELD	ESC ^
START/END BLANK FIELD	ESC _
SET BLOCK MODE	ESC B
SET CONVERSATION MODE	ESC C

ABSOLUTE CURSOR POSITIONING

X or Y	ASCII CODE	X or Y	ASCII CODE	X or Y	ASCII CODE
1	SPACE	28	;	55	V
2	!	29	<	56	W
3	"	30	=	57	X
4	#	31	>	58	Y
5	$	32	?	59	Z
6	%	33	@	60	[
7	&	34	A	61	\
8	'	35	B	62	]
9	(	36	C	63	^
10	)	37	D	64	_
11	*	38	E	65	`
12	+	39	F	66	a
13	,	40	G	67	b
14	–	41	H	68	c
15	.	42	I	69	d
16	/	43	J	70	e
17	0	44	K	71	f
18	1	45	L	72	g
19	2	46	M	73	h
20	3	47	N	74	i
21	4	48	O	75	j
22	5	49	P	76	k
23	6	50	Q	77	l
24	7	51	R	78	m
25	8	52	S	79	n
26	9	53	T	80	o
27	:	54	U		

TRANSMIT Y, THEN X.

BACK PAGE	ESC I	ERASE LINE TO NULL	ESC t
FORWARD PAGE	ESC K	ERASE PAGE TO NULL	ESC y
SET PAGE EDIT	ESC N	SET STATUS 1	ESC c1
CLEAR PAGE EDIT	ESC O	CLEAR STATUS 1	ESC b
PRINT PAGE	ESC P	SET STATUS 2	ESC e
UNFORMAT PRINT PAGE	ESC p	CLEAR STATUS 2	ESC d
SET PROGRAM MODE	ESC U	SET STATUS 3	ESC g
CLEAR PROGRAM MODE	ESC X	CLEAR STATUS 3	ESC f
SET COLUMN TAB	ESC V	SET STATUS 4	ESC <
		CLEAR STATUS 4	ESC >