VME-HSMEM-8/4
High-Speed Memory Board
Hardware Reference Manual

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PREFACE

This manual describes the Integrated Solutions VME-HSMEM-8/4, a VMEbus-compatible high-speed memory board. The text provided in this manual includes a product overview, specifications, and configuration information. The manual is divided into three sections:

SECTION 1: This section provides introductory material and an overview of board functions.

SECTION 2: This section lists the VME-HSMEM-8/4 specifications.

SECTION 3: This section provides information regarding the VME-HSMEM-8/4 switch and jumper configuration options.

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SECTION 1: INTRODUCTION

Integrated Solutions' (ISI) VME high-speed memory board (VME-HSMEM-8/4) is a fast-access, dual-ported memory board offering four or eight Mbytes of memory on a single board. This double-wide VMEbus-compatible board operates in a synchronous mode to provide a high-speed memory companion to ISI's VMEbus-compatible CPU boards. The VME-HSMEM-8/4 behaves in a completely synchronous fashion with all arbitration (three-way arbitration among the processor board, VMEbus, and refresh cycles) performed on the companion processor board.

1.1 High-Speed Memory Bus

All memory accesses are controlled over an ISI proprietary high-speed bus (HSMEM bus). The board supports 8-, 16-, and 32-bit transfers over the HSMEM bus. Refresh requests also arrive over the HSMEM bus, but refresh addresses are generated on the VME-HSMEM-8/4 board.

The HSMEM bus is implemented on the A and C rows of the VMEbus P2 connector in conjunction with connectors J1 and J2, which support HSMEM bus Address Bits 27–24 (HSA27–24). Some of the HSMEM bus signal specifications vary depending on which mode has been selected, i.e., the VME-HSMEM-8/4 board can be configured to operate with the VME-68K20 processor board (020 mode) or the VME-68K10 board (010 mode). The HSMEM bus signals are as follows:

HSCYC* Asserting this signal indicates the start of a memory cycle and its duration indicates the length of the active part of the cycle. The type of memory cycle (i.e., processor, VMEbus, or refresh) is determined by the status of HSMEM bus control signals HSVME* and HSREF*.

HSWRITE* Indicates whether the current memory access is a read cycle or a write cycle.

HSLWORD* This control line determines whether the HSDS1* and HSDS0* signals are to be interpreted in a 32-bit sense or in a 16-bit sense by the VME-HSMEM-8/4 memory boards (see Table 1-1 for details). Also, refer to the HSDS1* and HSDS0* signal descriptions that follow.

HSDS1* and HSDS0* These two lines are used in conjunction with HSA01 to determine the bytes accessed during a memory read or write cycle. Table 1-1 shows byte access selection for processor memory cycles (see Section 1.2), which use the HSMEM bus†.

HSREF* When asserted, this signal indicates that the memory cycle is a refresh cycle.

HSVME* When asserted, this signal indicates that the memory cycle is a VMEbus cycle.

HSPARERR* When asserted, this signal indicates a parity error on the current read access.

HSA27 - HSA01 These are the twenty-seven HSMEM bus address lines, allowing a maximum of 256 Mbytes of high-speed memory.

HSD31 - HSD00 These are the thirty-two HSMEM bus data lines.

† During VMEbus memory cycles (data is transferred directly to/from memory over the VMEbus), byte access selection is a function of VMEbus signals as shown in Table 1-2.

Table 1-1. Byte Access Selection (Processor Memory Cycle)

Longword				Logical Signal Level†				
Upper Word		Lower Word						
Byte 0 (MSB)	Byte 1	Byte 2	Byte 3 (LSB)	HSLWORD*	HSDS1*	HSDS0*	HSA01	Description
X	X			N††	1	1	0	Access upper word
		X	X	N	1	1	1	Access lower word
	X			N	0	1	0	Access Byte 1
			X	N	0	1	1	Access Byte 3
X				N	1	0	0	Access Byte 0
		X		N	1	0	1	Access Byte 2
				0	0	0	0	Illegal
				0	0	0	1	Illegal
X	X	X	X	1	0	0	N	Access longword

Table 1-2. Byte Access Selection (VMEbus Memory Cycle)

Longword				Logical Signal Level†				
Upper Word		Lower Word						
Byte 0	Byte 1	Byte 2	Byte 3	LWORD*	DS1*	DS0*	A01	Description
X	X			0	1	1	0	Access upper word
		X	X	0	1	1	1	Access lower word
	X			0	0	1	0	Access Byte 1
			X	0	0	1	1	Access Byte 3
X				0	1	0	0	Access Byte 0
		X		0	1	0	1	Access Byte 2
X	X	X	X	1	1	1	0	Access longword
	X	X		1	1	1	1	Access Bytes 1–2
	X	X	X	1	0	1	0	Access Bytes 1–3
X	X	X		1	1	0	0	Access Bytes 0–2
				1	1	0	1	Illegal
				1	0	1	1	Illegal
				0	0	0	N††	Transition state

† In Tables 1-1 and 1-2, a *1* indicates the signal is asserted and a *0* indicates the signal is not asserted. These symbols should not be confused with the signals' voltage levels.

†† An *N* indicates the logical level of the signal does not matter.

1.2 High-Speed Bus Cycles

There are three types of cycles involving the VME-HSMEM-8/4 board: processor cycles, VMEbus cycles, and refresh cycles. HSCYC* is the main timing control signal for all three cycle types and all memory timing is generated from this signal.

1.2.1 Processor Cycles

Regardless of the VME-HSMEM-8/4 mode configuration (020 or 010), all address lines and the HSWRITE* and HSLWORD* control lines must be stable at least 30ns prior to the assertion of HSCYC*. HSLWORD* must remain stable throughout the entire cycle, while HSWRITE* and the HSMEM bus address lines must remain stable until within 10ns of HSCYC* de-assertion. In addition, the HSREF* and HSVME* lines must remain inactive from at least 30ns prior to HSCYC* assertion and until within 10ns prior to HSCYC* de-assertion.

The signal timing requirements for HSCYC*, HSDS0*, and HSDS1* are dependent upon the mode configuration of the VME-HSMEM-8/4 board.

020 mode - HSCYC* must be asserted at least 120ns. The data strobe lines must be stable 30ns prior to HSCYC* assertion and must remain stable for 30ns after HSCYC* assertion.

010 mode - HSCYC* must be asserted at least 180ns. The data strobe lines must be stable within 45ns after HSCYC* assertion and must remain stable until HSCYC* de-assertion.

The VME-HSMEM-8/4 board requires a recovery time of at least 90ns between de-assertion and re-assertion of HSCYC*. It is the responsibility of the processor board to ensure this recovery time.

1.2.2 VMEbus Cycles

The HSVME* signal, asserted by the CPU, selects the manner of handling VMEbus data transfers:

- **HSVME* active:** When the processor asserts HSVME* coincident with HSCYC*, the VME-HSMEM-8/4 transfers data directly to/from the VMEbus. During VMEbus cycles, the VME-HSMEM-8/4 boards should obtain a VMEbus address, VMEbus address modifiers, and four control signals (LWORD*, DS1*, DS0*, and WRITE*) directly from the VMEbus.

  All address lines and the WRITE* and LWORD* control lines must be stable at least 30ns prior to the assertion of HSCYC* and must remain stable throughout the entire cycle. DS1* and DS0* must be stable prior to the assertion of HSCYC* and must remain stable throughout the entire cycle.

  The HSMEM bus control lines (HSWRITE*, HSLWORD*, HSDS1*, and HSDS0*) are disregarded during a VMEbus data transfer cycle.

- **HSVME* inactive:** During these cycles, the VMEbus data transfers are channeled through the processor board. All address lines and the HSWRITE* and HSLWORD* control line timings are as previously specified in the processor memory cycle description.

1.2.3 Refresh Cycles

Refresh cycles must be initiated by the processor board at least every 15.625 microseconds, but the refresh address is supplied by a counter on the VME-HSMEM-8/4 board. For refresh cycles, the HSREF* line must be asserted at least 30ns prior to assertion of HSCYC* and must remain stable until within 10ns of HSCYC* de-assertion. During a refresh cycle, the control signals HSDS1*, HSDS0*, HSWRITE*, and HSLWORD* are ignored. Additionally, since the VME-HSMEM-8/4 board generates an internal refresh address, the address on the HSMEM bus address lines is ignored.

1.3 Parity Generation and Checking

Parity generation and checking on a byte level is implemented on the VME-HSMEM-8/4 board. Correct parity is always generated on write cycles. To enable parity checking on read cycles, however, a switch must be enabled on the VME-HSMEM-8/4 board (see Section 3, Configuration).

In order for parity checking to function properly, the entire memory must be initialized prior to any read access, since byte and word reads are treated as longword accesses internally by the VME-HSMEM-8/4 board and parity is checked on all four bytes of the longword.

SECTION 2: SPECIFICATIONS

This section provides the specifications for the VME-HSMEM-8/4 memory board.

2.1 Memory Organization

The VME-HSMEM8 board provides 8192 Kbytes of memory, organized as two 1M x 36 bit banks. The VME-HSMEM4 board provides 4096 Kbytes of memory, organized as one 1M x 36 bit bank.

2.2 Form Factor

The VME-HSMEM-8/4 form factor is standard double-sized VMEbus - 160mm x 233.33mm.

2.3 Electrical Requirements

The VME-HSMEM8 board requires 4 amps (maximum) of +5 Vdc ± 5%, while the VME-HSMEM4 board requires 3.9 amps (maximum) of +5 Vdc ± 5%.

2.4 Environmental Requirements

The VME-HSMEM-8/4 environmental requirements are as follows:

Temperature:

0 to 50 degrees centigrade (operating)
-40 to 65 degrees centigrade (non-operating)

Humidity:

10 to 90 percent (non-condensing)

2.5 Indicators

A red LED (DS1) is provided to indicate that either a HSMEM bus or VMEbus cycle is in progress on the VME-HSMEM-8/4 board (LED is on). Refresh cycles do not cause DS1 to light.

2.6 Parity

The VME-HSMEM-8/4 supports on-board byte parity generation and detection.

2.7 Transfer Types

The VME-HSMEM-8/4 supports 8-, 16-, and 32-bit transfers on the HSMEM bus and 8-, 16-, or 32-bit transfers on the VMEbus.

2.8 I/O Connections

The VME-HSMEM-8/4 board has four I/O connectors. P1 and P2 are 96-pin DIN connectors. The VME-HSMEM-8/4 is connected to the VMEbus via connector P1 and Row B of connector P2.

The VME-HSMEM-8/4 is connected to the HSMEM bus via the user-defined pins (Rows A and C) of the P2 connector in conjunction with connectors J1 and J2. Connectors J1 and J2 are both 10-pin connectors which support HSMEM bus Address Bits 27–24. The purpose of two connectors is to allow the HSA27–24 lines to be easily daisy-chained from one memory board to another.

The P1, P2, and J1/J2 connector pin assignments and signal mnemonics are provided in Tables 2-1, 2-2, and 2-3, respectively.

NOTE

Each VME-HSMEM-8/4 board includes a 10-conductor ribbon cable to support HSA27–24 signal lines. When connecting the cables from the CPU board through a series of memory boards, refer to Figure 2-1 for the recommended cabling scheme. Also note that the last memory board in the chain must be terminated as described in Section 3 of this manual.

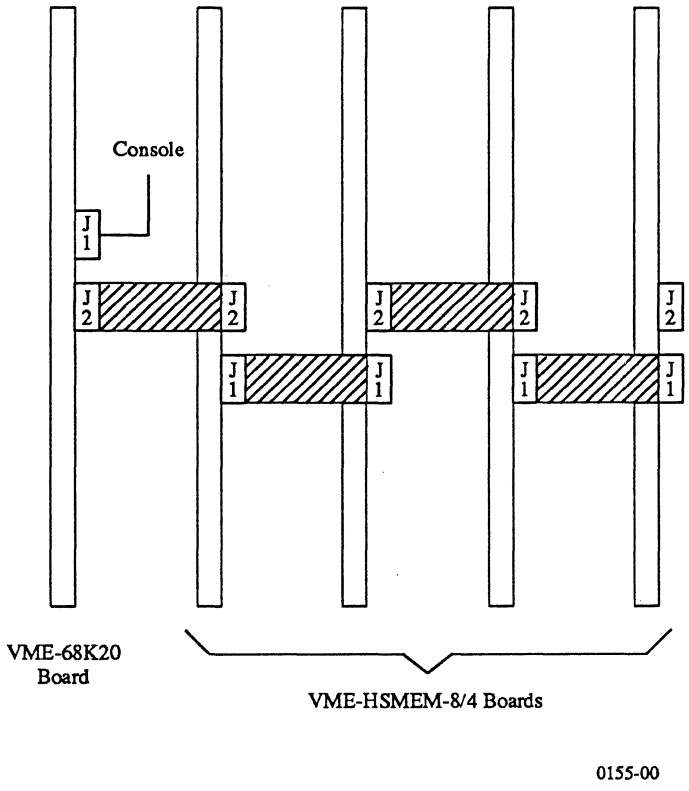


Figure 2-1. Memory Board Cabling Scheme

Table 2-1. VMEbus Connector P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*†	D08
2	D01	BCLR*†	D09
3	D02	ACFAIL*†	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK†	BG3IN*	SYSFAIL*†
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*†	SYSRESET*
13	DS0*	BR1*†	LWORD*
14	WRITE*	BR2*†	AM5
15	GND	BR3*†	A23
16	DTACK*	AM0†	A22
17	GND	AM1†	A21
18	AS*†	AM2†	A20
19	GND	AM3†	A19
20	IACK*†	GND	A18
21	IACKIN*	SERCLK†	A17
22	IACKOUT*	SERDAT†	A16
23	AM4	GND	A15
24	A07	IRQ7*†	A14
25	A06	IRQ6*†	A13
26	A05	IRQ5*†	A12
27	A04	IRQ4*†	A11
28	A03	IRQ3*†	A10
29	A02	IRQ2*†	A09
30	A01	IRQ1*†	A08
31	-12V†	+5V STDBY†	+12V†
32	+5V	+5V	+5V

NOTE

An asterisk following a signal name indicates that the signal is true when the signal is low.

† VMEbus signals, but no connection on VME-HSMEM-8/4 board.

Table 2-2. Connector P2 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	HSD07	+5 Volts	HSD15
2	HSD06	GND	HSD14
3	HSD05	n/c†	HSD13
4	HSD04	A24	HSD12
5	HSD03	A25	HSD11
6	HSD02	A26	HSD10
7	HSD01	A27†	HSD09
8	HSD00	A28†	HSD08
9	HSVME*	A29†	HSA23
10	HSA01	A30†	HSA22
11	HSA02	A31†	HSA21
12	HSA03	GND	HSA20
13	HSA04	+5 Volts	HSA19
14	HSA05	D16	HSA18
15	HSA06	D17	HSA17
16	HSA07	D18	HSA16
17	HSA08	D19	HSA15
18	HSA09	D20	HSA14
19	HSA10	D21	HSA13
20	HSA11	D22	HSA12
21	HSD31	D23	HSCYC*
22	HSD30	GND	HSDS0*
23	HSD29	D24	HSLWORD*
24	HSD28	D25	HSDS1*
25	HSD27	D26	Reserved
26	HSD26	D27	HSPARERR*
27	HSD25	D28	HSD19
28	HSD24	D29	HSD18
29	HSD23	D30	HSD17
30	HSD22	D31	HSREF*
31	HSD21	GND	HSWRITE*
32	HSD20	+5 Volts	HSD16

NOTE

The B row of connector P2 implements VMEbus address and data lines.

† Not connected (n/c) on the VME-HSMEM-8/4 board.

Table 2-3. Connectors J1 and J2 Pin Assignments

Pin Number	Signal Mnemonic	Signal Name
1	—	Reserved
2	GND	Ground
3	HSA27	High-Speed Bus Address 27
4	GND	Ground
5	HSA26	High-Speed Bus Address 26
6	GND	Ground
7	HSA25	High-Speed Bus Address 25
8	GND	Ground
9	HSA24	High-Speed Bus Address 24
10	GND	Ground

2.9 HSMEM Bus Timing Specifications

The VME-HSMEM-8/4 memory access time is 125ns, with a total cycle time of 210ns. The HSMEM bus signal specifications are as follows (also see Figure 2-2 for a timing diagram showing interface requirements and Table 2-4 for minimum and maximum timing specifications values):

HSCYC* The minimum duration for which HSCYC* is active during read and write cycles is 120ns, with a minimum recovery time of 90ns.

HSWRITE* This signal must be stable 30ns prior to HSCYC* assertion and must remain stable until within 10ns prior to HSCYC* de-assertion.

HSLWORD* This control line determines whether the HSDS1* and HSDS0* signals are to be interpreted in a 32-bit sense or in a 16-bit sense by the VME-HSMEM-8/4 memory boards. In the case of ISI's VME-68K20 companion processor board, HSLWORD* is always asserted and all memory accesses are interpreted by the memory board in a 32-bit sense. The VME-68K10 companion processor board never asserts HSLWORD* and the VME-HSMEM-8/4 board interprets all memory accesses in a 16-bit sense.

HSDS1* and HSDS0* The data strobe signal timing specifications are dependent upon which mode is selected on the VME-HSMEM-8/4 board:

020 mode - data strobe lines must be stable 30ns prior to HSCYC* assertion. These lines must remain stable 30ns after HSCYC* assertion.

010 mode - data strobe lines must be stable within 45ns after HSCYC* assertion and must remain stable until HSCYC* de-assertion.

HSREF* This signal must be stable 30ns prior to assertion of HSCYC* and must remain stable until within 10ns prior to HSCYC* de-assertion.

HSVME* This signal must be stable 30ns prior to HSCYC* assertion and must remain stable until within 10ns prior to HSCYC* de-assertion.

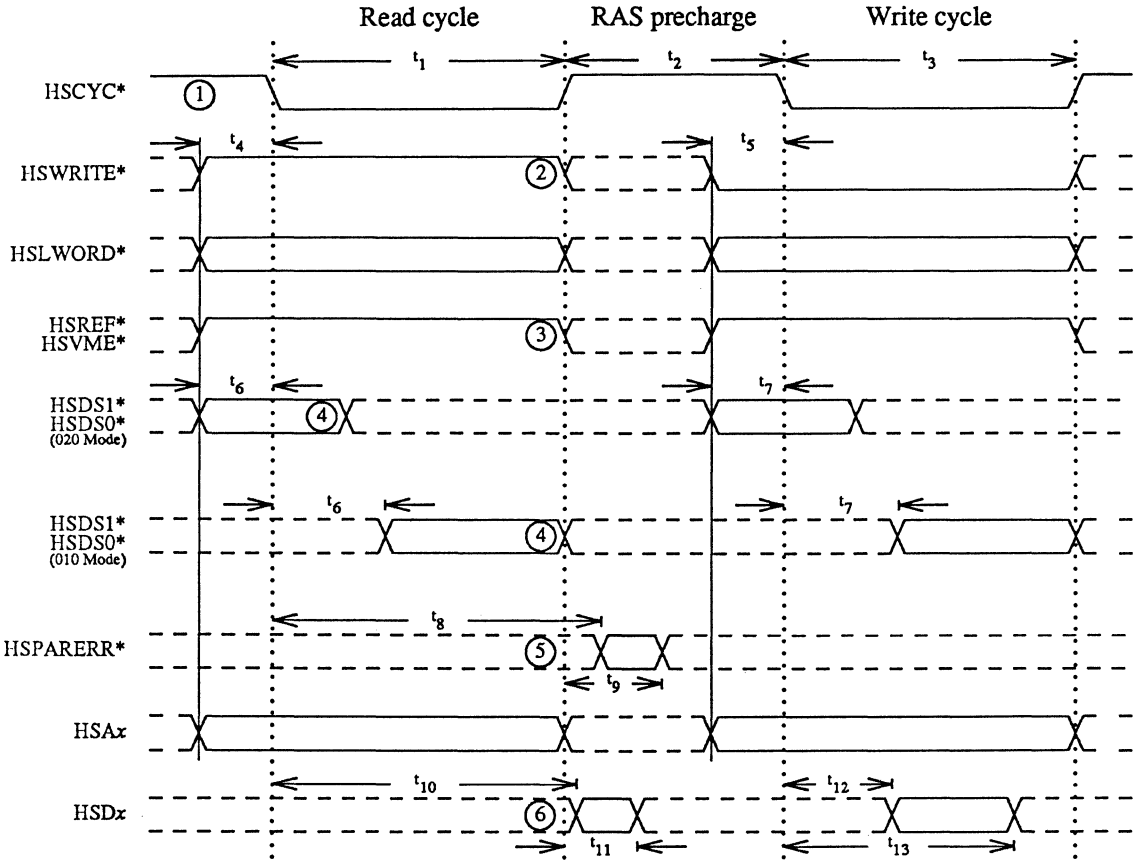
HSPARERR* This signal will be stable within 135ns after the assertion of HSCYC* and will remain stable until 50ns after HSCYC* de-assertion.

HSA27 - HSA01 Address signals must be stable 30ns prior to assertion of HSCYC* and must remain stable until within 10ns prior to HSCYC* de-assertion.

HSD31 - HSD00 On read cycles, data signals must be stable within 125ns after the assertion of HSCYC* and must remain stable until at least 40ns after de-assertion of HSCYC*. On write cycles, data signals must be stable within 30ns after assertion of HSCYC* and must remain stable 95ns after HSCYC* assertion.

Table 2-4. VME-HSMEM-8/4 Timing Specifications

Parameter		020 Mode		010 Mode	
		Min.	Max.	Min.	Max.
t_1	HSCYC*, read cycle	120ns		120ns	
t_2	HSCYC*, RAS precharge	90ns		90ns	
t_3	HSCYC*, write cycle	120ns		120ns	
t_4	HSWRITE*, HSLWORD*, HSREF*, HSVME*, HSA*x* leading edges, read cycle	30ns		30ns	
t_5	HSWRITE*, HSLWORD*, HSREF*, HSVME*, HSAx leading edges, write cycle	30ns		30ns	
t_6	HSDS1* and HSDS0* leading edge, read cycle	30ns			45ns
t_7	HSDS1* and HSDS0* leading edge, write cycle	30ns			45ns
t_8	HSPARRER* leading edge		135ns		135ns
t_9	HSPARRER* trailing edge	50ns		50ns	
t_{10}	HSD*x* leading edge, read cycle		125ns		125ns
t_{11}	HSD*x* trailing edge, read cycle	40ns		40ns	
t_{12}	HSD*x* leading edge, write cycle		30ns		30ns
t_{13}	HSD*x* trailing edge, write cycle	95ns		95ns	



(1) On VMEbus access cycles, BERR* and DTACK* timing (as related to HSCYC*) are noted below.†

(2) HSWRITE*, HSREF*, and HSA*x* must remain stable until within 10ns of HSCYC* de-assertion.

(3) HSREF* must be stable at least 30ns before HSCYC* and remain stable until within 10ns of HSCYC* de-assertion. All other HSMEM bus lines are disregarded during a refresh cycle.

(4) HSDS1* and HSDS0* must remain stable until 30ns after HSCYC* assertion for 020 mode and until HSCYC* de-assertion for 010 mode.

(5) HSPARERR* is valid within 135ns after HSCYC* is asserted on a read cycle and remains valid until 50ns after HSCYC* de-assertion.

(6) HSD*x* are valid within 125ns after HSCYC* is asserted on a read cycle and remain valid at least 40ns after HSCYC* is de-asserted. On write cycles, HSD*x* must be stable within 30ns after HSCYC* assertion and must remain stable until 95ns after HSCYC* assertion.

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Figure 2-2. VME-HSMEM-8/4 Timing Diagram

† On VMEbus write cycles, either BERR* or DTACK* is asserted 40ns after HSCYC* assertion and remains asserted until de-assertion of VMEbus signals DS1* and DS0*. On VMEbus read cycles, either BERR* or DTACK* is asserted 160ns after HSCYC* assertion and remains asserted until de-assertion of DS1* and DS0*.

SECTION 3: CONFIGURATION

This section describes how to configure the VME-HSMEM-8/4 board. There are nine sets of jumpers, one switch bank (SW2), and one rotary switch (SW1) that enable you to configure the operation of the memory board (see Figure 3-1).

The jumper sets are numbered E1 through E9 and are located as shown in Figure 3-1. SW2 is an eight-bit DIP switch, while SW1 is a 16-position rotary switch. The rotary switch has a small index mark that indicates what setting on the rotary wheel is selected. Figure 3-2 shows the location of the index mark.

The functions and configuration of these jumpers and switches are discussed in the subsections that follow.

NOTE

Factory default jumper and switch settings are shown in bold typeface.

3.1 Address Boundary Configuration (Eight-Mbyte Board)

The address boundary for the VME-HSMEM8 is set by using rotary switch SW1 in conjunction with bit switches 1 and 2 in SW2. This combination of switch settings allows easy placement of the VME-HSMEM8 board on any eight-Mbyte boundary in both the 256-Mbyte HSMEM bus address space and the lower 256-Mbyte VMEbus address space.

Switches SW2-1 and SW2-2 select which of the four 64-Mbyte regions within the 256-Mbyte address space the VME-HSMEM8 will respond to. SW1 further selects which of the eight-Mbyte segments within the 64-Mbyte region the memory board will respond to.

NOTE

Since most system configurations are expected to be less than 64-Mbytes, typically only SW1 will need alteration to select the address boundary within the 64-Mbyte region.

The rotary switch consists of a 16-position wheel marked in increments from 0 to F (hex). Each increment represents an increase in the address boundary of *four Mbytes*. Since the VME-HSMEM8 board is only capable of being configured on eight-Mbyte boundaries, positioning the wheel to any odd number has the same effect as positioning it to the previous even number. For example, wheel position 1 corresponds to the same address boundary as position 0, position 3 responds to the same address boundary as position 2, and so on. Refer to Table 3-1 for the correct memory boundary settings.

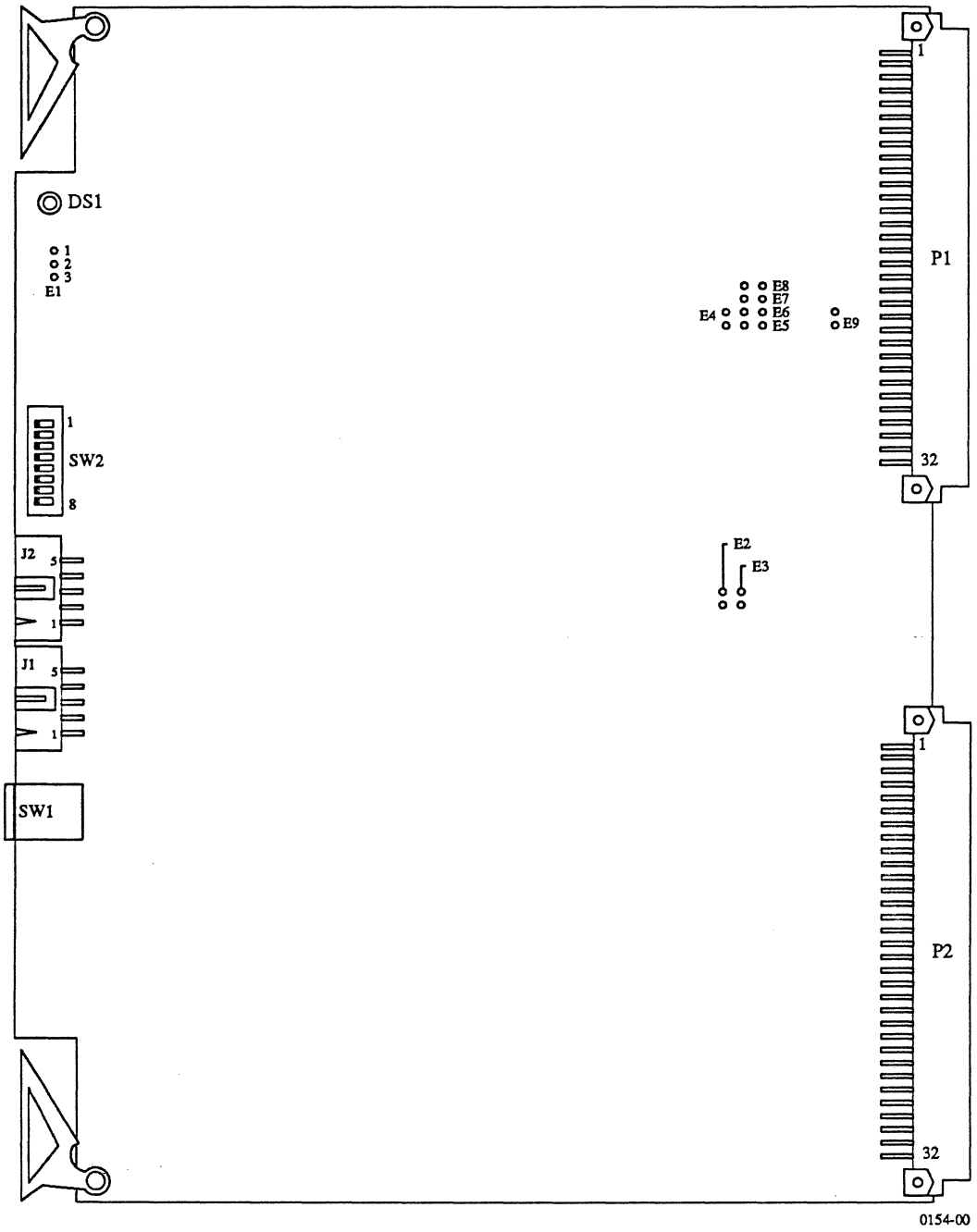

Figure 3-1. VME-HSMEM-8/4 Board Layout

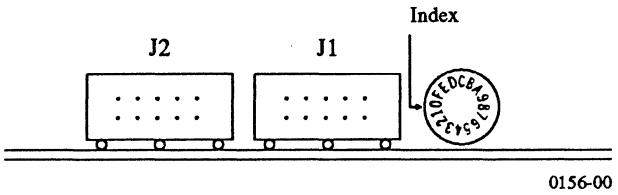

Figure 3-2. SW1 Index Mark

Table 3-1. VME-HSMEM8 Address Boundaries

64-Mbyte Region	Boundary Setting (Mbytes)	SW2-1	SW2-2	SW1	Address Range
First	**0 (default)**	**On**	**On**	**0**	**0000000 – 07FFFFF**
	8	On	On	2	0800000 – 0FFFFFF
	16	On	On	4	1000000 – 17FFFFF
	24	On	On	6	1800000 – 1FFFFFF
	32	On	On	8	2000000 – 27FFFFF
	40	On	On	A	2800000 – 2FFFFFF
	48	On	On	C	3000000 – 37FFFFF
	56	On	On	E	3800000 – 3FFFFFF
Second	64	On	Off	0	4000000 – 47FFFFF
	72	On	Off	2	4800000 – 4FFFFFF
	80	On	Off	4	5000000 – 57FFFFF
	88	On	Off	6	5800000 – 5FFFFFF
	96	On	Off	8	6000000 – 67FFFFF
	104	On	Off	A	6800000 – 6FFFFFF
	112	On	Off	C	7000000 – 77FFFFF
	120	On	Off	E	7800000 – 7FFFFFF
Third	128	Off	On	0	8000000 – 87FFFFF
	136	Off	On	2	8800000 – 8FFFFFF
	144	Off	On	4	9000000 – 97FFFFF
	152	Off	On	6	9800000 – 9FFFFFF
	160	Off	On	8	A000000 – A7FFFFF
	168	Off	On	A	A800000 – AFFFFFF
	176	Off	On	C	B000000 – B7FFFFF
	184	Off	On	E	B800000 – BFFFFFF
Fourth	192	Off	Off	0	C000000 – C7FFFFF
	200	Off	Off	2	C800000 – CFFFFFF
	208	Off	Off	4	D000000 – D7FFFFF
	216	Off	Off	6	D800000 – DFFFFFF
	224	Off	Off	8	E000000 – E7FFFFF
	232	Off	Off	A	E800000 – EFFFFFF
	240	Off	Off	C	F000000 – F7FFFFF
	248	Off	Off	E	F800000 – FFFFFFF

3.2 Address Boundary Configuration (Four-Mbyte Board)

The address boundary for the VME-HSMEM4 is set by using rotary switch SW1 in conjunction with bit switches 1 and 2 in SW2. This combination of switch settings allows easy placement of the VME-HSMEM4 board on any four-Mbyte boundary in both the 256-Mbyte HSMEM bus address space and the lower 256-Mbyte VMEbus address space.

Switches SW2-1 and SW2-2 select which of the four 64-Mbyte regions within the 256-Mbyte address space the VME-HSMEM4 will respond to. SW1 further selects which of the four-Mbyte segments within the 64-Mbyte region the memory board will respond to.

NOTE

Since most system configurations are expected to be less than 64-Mbytes, typically only SW1 will need alteration to select the address boundary within the 64-Mbyte region.

The rotary switch consists of a 16-position wheel marked in increments from 0 to F (hex). Each increment represents an increase in the address boundary by *four Mbytes*. Refer to Table 3-2 for the correct memory boundary settings.

Table 3-2. VME-HSMEM4 Address Boundaries

64-Mbyte Region	Boundary Setting (Mbytes)	SW2-1	SW2-2	SW1	Address Range
First	**0 (default)**	**On**	**On**	**0**	**0000000 – 03FFFFF**
	4	On	On	1	0400000 – 07FFFFF
	8	On	On	2	0800000 – 0BFFFFF
	12	On	On	3	0C00000 – 0FFFFFF
	16	On	On	4	1000000 – 13FFFFF
	20	On	On	5	1400000 – 17FFFFF
	24	On	On	6	1800000 – 1BFFFFF
	28	On	On	7	1C00000 – 1FFFFFF
	32	On	On	8	2000000 – 23FFFFF
	36	On	On	9	2400000 – 27FFFFF
	40	On	On	A	2800000 – 2BFFFFF
	44	On	On	B	2C00000 – 2FFFFFF
	48	On	On	C	3000000 – 33FFFFF
	52	On	On	D	3400000 – 37FFFFF
	56	On	On	E	3800000 – 3BFFFFF
	60	On	On	F	3C00000 – 3FFFFFF

(continued on next page)

Table 3-2. VME-HSMEM4 Address Boundaries (*continued*)

64-Mbyte Region	Boundary Setting (Mbytes)	SW2-1	SW2-2	SW1	Address Range
Second	64	On	Off	0	4000000 – 43FFFFF
	68	On	Off	1	4400000 – 47FFFFF
	72	On	Off	2	4800000 – 4BFFFFF
	76	On	Off	3	4C00000 – 4FFFFFF
	80	On	Off	4	5000000 – 53FFFFF
	84	On	Off	5	5400000 – 57FFFFF
	88	On	Off	6	5800000 – 5BFFFFF
	92	On	Off	7	5C00000 – 5FFFFFF
	96	On	Off	8	6000000 – 63FFFFF
	100	On	Off	9	6400000 – 67FFFFF
	104	On	Off	A	6800000 – 6BFFFFF
	108	On	Off	B	6C00000 – 6FFFFFF
	112	On	Off	C	7000000 – 73FFFFF
	116	On	Off	D	7400000 – 77FFFFF
	120	On	Off	E	7800000 – 7BFFFFF
	124	On	Off	F	7C00000 – 7FFFFFF
Third	128	Off	On	0	8000000 – 83FFFFF
	132	Off	On	1	8400000 – 87FFFFF
	136	Off	On	2	8800000 – 8BFFFFF
	140	Off	On	3	8C00000 – 8FFFFFF
	144	Off	On	4	9000000 – 93FFFFF
	148	Off	On	5	9400000 – 97FFFFF
	152	Off	On	6	9800000 – 9BFFFFF
	156	Off	On	7	9C00000 – 9FFFFFF
	160	Off	On	8	A000000 – A3FFFFF
	164	Off	On	9	A400000 – A7FFFFF
	168	Off	On	A	A800000 – ABFFFFF
	172	Off	On	B	AC00000 – AFFFFFF
	176	Off	On	C	B000000 – B3FFFFF
	180	Off	On	D	B400000 – B7FFFFF
	184	Off	On	E	B800000 – BBFFFFF
	188	Off	On	F	BC00000 – BFFFFFF

(continued on next page)

Table 3-2. VME-HSMEM4 Address Boundaries (*continued*)

64-Mbyte Region	Boundary Setting (Mbytes)	SW2-1	SW2-2	SW1	Address Range
Fourth	192	Off	Off	0	C000000 – C3FFFFF
	196	Off	Off	1	C400000 – C7FFFFF
	200	Off	Off	2	C800000 – CBFFFFF
	204	Off	Off	3	CC00000 – CFFFFFF
	208	Off	Off	4	D000000 – D3FFFFF
	212	Off	Off	5	D400000 – D7FFFFF
	216	Off	Off	6	D800000 – DBFFFFF
	220	Off	Off	7	DC00000 – DFFFFFF
	224	Off	Off	8	E000000 – E3FFFFF
	228	Off	Off	9	E400000 – E7FFFFF
	232	Off	Off	A	E800000 – EBFFFFF
	236	Off	Off	B	EC00000 – EFFFFFF
	240	Off	Off	C	F000000 – F3FFFFF
	244	Off	Off	D	F400000 – F7FFFFF
	248	Off	Off	E	F800000 – FB00000
	252	Off	Off	F	FC00000 – FFFFFFF

3.3 Extended Address Mode

The VME-HSMEM-8/4 memory board has the ability to respond to extended addresses above the 16-Mbyte boundary. In order to use this feature, the HSMEM bus address lines A27–A24 must be connected from the CPU to the memory board by a 10-conductor ribbon cable as shown in Figure 2-1. The 10-conductor cable must be installed between the CPU and memory boards. In systems with multiple memory boards, the ribbon cable must be daisy chained from the CPU board to all the memory boards.

In order to enable the memory board to respond to extended addresses, switch SW2-3 must be off (see Table 3-3). When the switch is on, the memory board disregards HSMEM bus and VMEbus address lines A27–A24. The factory default setting is extended addressing mode disabled.

Table 3-3. Extended Addressing Switch

SW2-3	Description
On	**Extended address mode disabled (default)**
Off	Extended address mode enabled

3.4 Extended Address Line Termination

Termination resistors are provided on each memory board to properly terminate the extended address lines A27–A24 for proper operation. These resistors must be connected to the address lines only on the last memory board in the daisy chain (farthest from the CPU board). Memory boards between the last memory board and the CPU (if any) must not have any termination resistor connected.

Switches SW2-5 through SW2-8 determine whether or not the termination resistors are connected. If all four positions are on, the resistors are connected. If all four positions are off, the resistors are not connected. These four switches must always be all on or all off. The factory default setting is to have all four switches on (see Table 3-4).

Table 3-4. Extended Addressing Line Termination

SW2-5 through SW2-8	Description
On	**Address line terminated (default)**
Off	Address line not terminated

3.5 Parity Checking

Parity generation and checking is implemented on the VME-HSMEM-8/4 board and is enabled and disabled with SW2-4. During write cycles, odd parity is generated for each byte written. The odd parity bit is written into a parity RAM which accompanies each group of eight data RAMs. On read accesses, parity is checked for each byte. If a parity error is detected, the parity error line is asserted. During a processor memory cycle, the parity error line is the HSMEM bus signal HSPARERR*. During a VMEbus memory cycle, the VMEbus signal BERR* is asserted when a parity error is detected. The factory default configuration is with parity checking enabled (see Table 3-5).

Table 3-5. Parity Checking

SW2-4	Description
On	**Parity checking enabled (default)**
Off	Parity checking disabled

3.6 Operating Mode

The VME-HSMEM-8/4 memory board can be configured to work with either ISI's VME-68K10 CPU board (010 mode) or the VME-68K20 CPU board (020 mode). These different operating modes are selected via jumpers E1 and E4. Jumpers E1 and E4 change the timing for latching addresses in order to accommodate the different signal timings for the two processor boards. The appropriate jumper settings are shown for each operating mode in Table 3-6. The factory default setting is for 020 mode.

Table 3-6. Operating Mode Selection

	Jumper	
CPU Board	E1	E4
VME-68K10	E1-2 to E1-3	Out
VME-68K20 (default)	**E1-1 to E1-2**	**In**

3.7 Memory Size

The VME-HSMEM-8/4 memory board has the ability to be configured as an eight-Mbyte board or as a half-populated four-Mbyte board. To use the four-Mbyte configuration, DRAMs must be inserted into locations 1B–1K, 2B–2K, 3B–3K, and 4B–4K. The other DRAM locations can either be filled or left empty for proper four-Mbyte memory operation. There are three jumpers that configure the memory board as either eight or four Mbytes as shown in Table 3-7. The factory default is set for eight Mbytes on the VME-HSMEM8 and for four Mbytes and the VME-HSMEM4.

Table 3-7. Memory Size Selection

	Jumper		
Memory Size	E2	E3	E7
4 Mbytes	In	Out	In
8 Mbytes	Out	In	Out

3.8 Factory Settings

The rest of the jumpers on the VME-HSMEM-8/4 memory board are set by the factory. They are not user configurable. Table 3-8 lists how the jumpers must be set for proper operation. In addition, switch SW2-3 is factory set to *ON* and must remain so.

Table 3-8. Factory Set Jumpers

Jumper	Setting
E5	Out
E6	In
E8	Out
E9	In

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