VME-ICP16/8

Intelligent Communications Processor

Hardware Reference Manual

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PREFACE

This manual describes the Integrated Solutions VME-ICP16/8 Intelligent Communications Processor board and contains the information necessary to configure it into a system. If you are using an Optimum V System or WorkStation, shipped complete with a VME-ICP16/8, you do not need to use this manual.

The manual is divided into four sections, which include the following:

Section 1 describes the general features and architecture of the VME-ICP16/8.

Section 2 lists the board specifications.

Section 3 provides information regarding VME-ICP16/8 configuration.

Section 4 describes the VME-ICP16/8 software interface.

In this manual, the use of an asterisk (*) following a signal name indicates that the signal is true when low.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

SECTION 1: INTRODUCTION

If you have not yet done so, please read the preface at the beginning of this manual.

Integrated Solutions' VME-ICP16/8 is an intelligent communications processor that offers eight or sixteen RS232C serial ports and one parallel printer output port on a single VME-compatible printed circuit board. The VME-ICP16/8 comes in four configurations:

- Sixteen RS232C serial ports and one Centronics-compatible parallel printer port
- Sixteen RS232C serial ports and one Dataproducts-compatible parallel printer port
- Eight RS232C serial ports and one Centronics-compatible parallel printer port
- Eight RS232C serial ports and one Dataproducts-compatible parallel printer port

NOTE

This manual does not support certain early versions of the VME-ICP8, specifically IS part number 102133. Locate the board part number on the pin side of the board. If you have one of these early boards, you can get supporting documentation through IS Customer Support. Ask for the *VME-ICP8 Specification/Configuration Summary*, IS part number 9110-102133-02 (old part number) or 490026 (new part number).

A VME-ICP8 is essentially a depopulated VME-ICP16. You can upgrade the VME-ICP8 by adding the necessary hardware to implement an additional eight serial ports; this is a field upgrade.

1.1 Features

The VME-ICP16/8 board supports eight or sixteen asynchronous programmable RS232C serial ports and one parallel printer port in a VME bus-based computer system. The VME-ICP16/8 offers these high performance features:

- Up to 16 Kbytes of on-board data cache for sustained high data transfer rates.
- Per-line programmable baud rate, character length, parity, stop bits, and transmit enable.
- Various baud rates up to 38.4K baud.
- Split receive/transmit rate pairs.

1.2 Architecture

Figure 1-1 shows the major functional elements of a fully configured VME-ICP16/8 board. These functional elements include

- Control microprocessor (Z8002)
- 16 Kbytes cache buffer
- EPROM-resident firmware
- VME interface logic (Bus Request/Grant, Address Decode, Interrupt Request)
- Eight dual-channel asynchronous receiver/transmitters with programmable baud rate

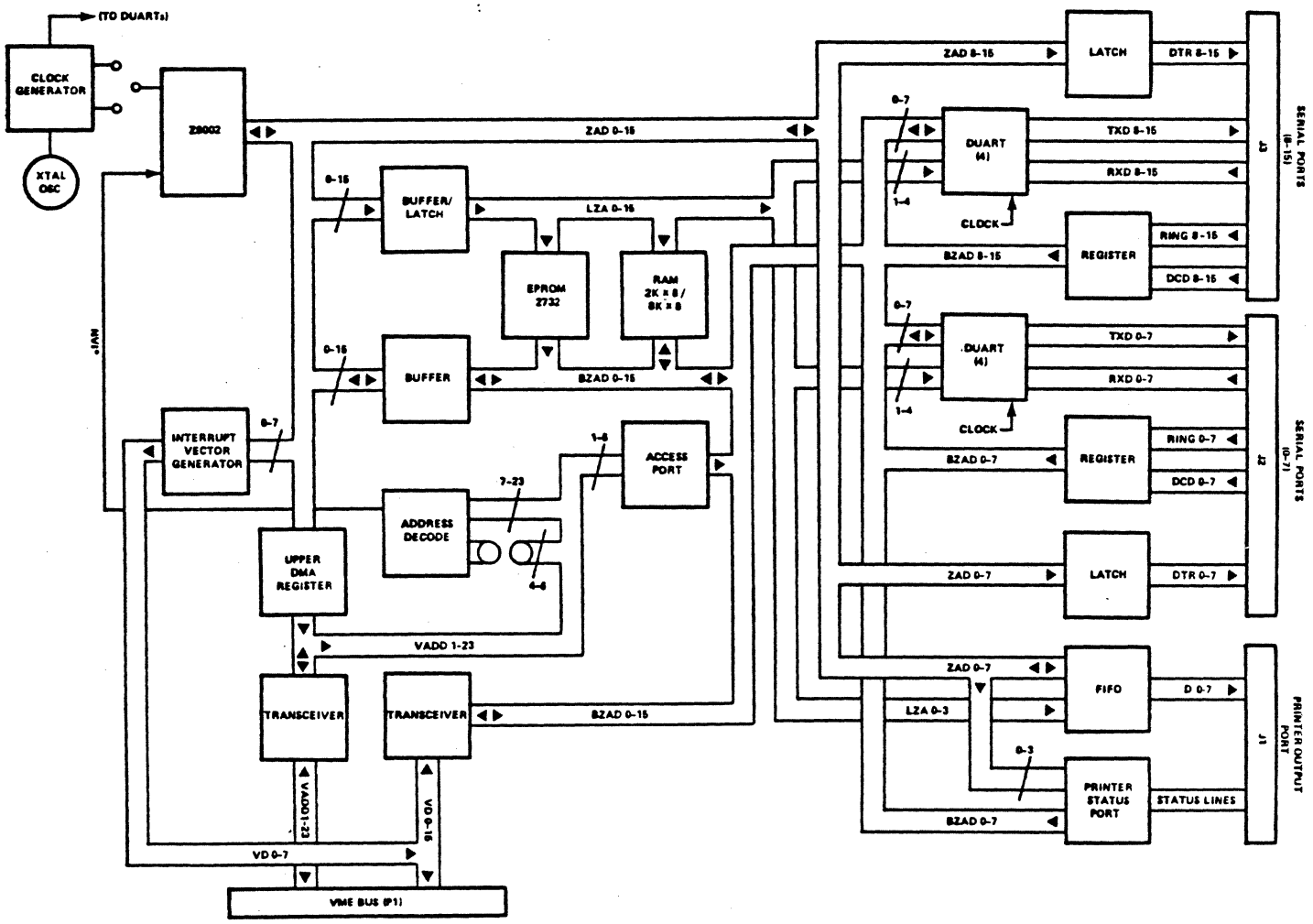

Figure 1-1. VME-ICP16/8 Block Diagram

1.2.1 Control Microprocessor

The high speed 16-bit microprocessor

- Directly controls all communications across the VME host interface
- Sets up and monitors all operations to the serial ports and to the parallel printer port

Using a 16-bit microprocessor gives the VME-ICP16/8 a higher level of functionality independent of host processor intervention than is possible with less intelligent controllers.

1.2.2 Cache Buffer

All information transfers between the peripheral devices and the VME bus memory through an on-board buffer memory. The buffer memory occupies either 2K x 8 or 8K x 8 static RAMs for a maximum of 16 Kbytes. This prevents data overruns that can occur with non-buffered controllers when they cannot acquire the host memory bus fast enough to prevent losing data due to a FIFO overflow.

At power-up, the firmware automatically determines how much RAM is present. Therefore, no firmware changes are required when going from one RAM configuration to another.

1.2.3 EPROM

All VME-ICP16/8 operations are controlled and monitored by the firmware residing in two EPROMs. The VME-ICP16/8 EPROM sockets can accommodate either 2716- or 2732-type EPROMs.

The VME-ICP16/8 factory-shipped firmware comes in two 2732-type EPROMs. These can easily be changed in the field for firmware upgrades.

1.2.4 VME Interface

The VME-ICP16/8 interfaces with the VME bus as a 24 address bit, 16 data bit master; and a 24 address bit, 16 data bit slave (as defined in the *VMEbus Specification Manual*, Motorola part number MVMEBS/D1). The VME interface logic on the VME-ICP16/8 board provides interfacing capability consistent with the VME specification for these VME-defined functional modules:

- Data Transfer Bus Requester—This is the bus acquisition interface based on a Bus Request/Bus Grant protocol. VME defines four separate sets (0–3) of these lines. Each set supports a "daisy chain propagation" priority scheme among multiple requesters within the set. Priorities also exist between sets, with highest priority going to Request 3. The VME-ICP16/8 supports all four sets.
- Data Transfer Bus Master—This is the ability to initiate data transfer cycles across the Data Transfer Bus. When granted acquisition of the bus, the VME-ICP16/8 may directly access the host memory, independent of the host CPU.
- Interrupter—The Interrupter performs three tasks:
  - — Asserts the interrupt request line
  - — Supplies a status/ID (vector) byte to the data bus when its request has been acknowledged
  - — Propagates the interrupt acknowledge daisy chain signal if it is not requesting that level of interrupt

  VME supports seven levels (1–7) of interrupt request priority, with level 7 being the highest. The VME-ICP16/8 can select one level from levels 3 through 6; levels 1, 2, and 7 are not selectable.
- Slave—This is the ability to respond to an access attempt by a master. Determination of an attempt to access is based on recognition of a certain address within a particular address range. The VME-ICP16/8 can exist on any 16-word boundary within the address range of FFF000 to FFFFC0.

1.2.5 Dual-Channel Receiver/Transmitters

The VME-ICP16/8 uses dual-channel receiver/transmitters (DUARTs) to handle heavy bursts of input with minimum risk of data loss. Received data is quadruple buffered via an architecture of holding registers and a shift register. Consequently, even during periods of host CPU unavailability, the VME-ICP16/8 receives and holds data for all channels with little risk of data overrun.

Each receiver/transmitter provides two independent, full-duplex, asynchronous channels with these programmable parameters:

- Baud rate
- Character length
- Parity
- Stop bits
- Transmit enable

1.3 Device Register Addressing

Programming of the individual ports, and of the VME-ICP16/8 itself, uses 14 device registers located at contiguous word locations on the VME bus. These device registers occupy the first 14 words on any 16-word boundary within the address range of FFF000 to FFFFC0. The remaining two words may not be assigned for other functions.

Table 1-1 defines the fourteen VME-ICP16/8 device registers.

Table 1-1. Device Registers

Register	Mnemonic
Selector Register	SEL
Interrupt Control Register	ICR
Line Enable Register	LER
Transmit Control Register	TCR
Break Register	BRK
Silo Window Register	SWR
Assert Carrier Register	ACR
Detect Carrier Register	DCR
Detect Ring Register	DRR
Parameter Register	PR
Status Register	SR
Bus Address High	BAH
Bus Address Low	BAL
Byte Count	BC

SECTION 2: SPECIFICATIONS

This section provides performance specifications and operating requirements for the VME-ICP16/8.

2.1 Form Factor

The form factor for the VME-ICP16/8 is standard, double-sized VME, 160mm x 233.33mm.

2.2 Input/Output Connections

The VME-ICP16/8 plugs into a VME bus-based system and supports either eight or sixteen RS232C serial ports and one parallel printer output port. The VME-ICP16/8 interfaces with the VME bus, as defined in the *VMEbus Specification Manual*, via one connector, P1. Table 2-1 shows the pin assignments and signal mnemonics for connector P1.

The I/O connections for the 16 serial port signal lines pass through two 50-pin connectors, J2 and J3. Tables 2-2 and 2-3 show the pin assignments and signal mnemonics for J2 and J3 respectively. The VME-ICP8 uses only J2.

A 20-pin connector, J1, on the VME-ICP16 board provides the signal interface for a parallel printer. Since the VME-ICP16 can support either a Centronics- or Dataproducts-compatible printer, J1 may have the signal interface provided in Table 2-4 (Centronics) or Table 2-5 (Dataproducts).

2.3 Addressing

The VME-ICP16/8 board uses 14 one-word VME bus address locations as device registers to support the sixteen RS232C serial ports and the parallel printer port. These device registers occupy the first 14 words on any 16-word boundary within the address range of FFF000 to FFFFC0 (hex). The last two word locations must remain available to the VME-ICP16/8 and may not be reassigned for other functions.

The VME-ICP16/8 responds to all standard supervisory and non-privileged accesses. It does not respond to short I/O or extended (32-bit address) accesses.

2.4 Interrupt Vector

The VME-ICP16/8 interrupt vector is software programmable.

Table 2-1. VME Bus Connector P1 Pin Assignments

Pin Number	Row A Signal	Row B Signal	Row C Signal
1	VMED0	BBUSY*	VMED8
2	VMED1	BCLR*	VMED9
3	VMED2	ACFAIL*†	VMED10
4	VMED3	BG0IN*	VMED11
5	VMED4	BG0OUT*	VMED12
6	VMED5	BG1IN*	VMED13
7	VMED6	BG1OUT*	VMED14
8	VMED7	BG2IN*	VMED15
9	GND	BG2OUT*	GND
10	SYSCLK†	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	VMEBERR*
12	VMEDS1*	BR0*	SYSRESET*
13	VMEDS0*	BR1*	LWRD*†
14	VMEWR*	BR2*	VMEAM5
15	GND	BR3*	VADD23
16	VMEDTACK*	VMEAM0	VADD22
17	GND	VMEAM1	VADD21
18	VMEAS*	VMEAM2	VADD20
19	GND	VMEAM3	VADD19
20	VMEIACK*	GND	VADD18
21	IACKIN*	SERCLK†	VADD17
22	IACKOUT*	SERDAT†	VADD16
23	VMEAM4	GND	VADD15
24	VADD7	IRQ7*†	VADD14
25	VADD6	IRQ6*	VADD13
26	VADD5	IRQ5*	VADD12
27	VADD4	IRQ4*	VADD11
28	VADD3	IRQ3*	VADD10
29	VADD2	IRQ2*†	VADD9
30	VADD1	IRQ1*†	VADD8
31	-12V†	+5V STDBY†	+12V
32	+5V	+5V	+5V

NOTE

The use of an asterisk (*) following the signal name indicates that the signal is true when it is low.

† VME bus signals, but no connection on VME-ICP16/8 board.

Table 2-2. I/O Port Connector J2 Pin Assignments

Pin Number	Signal Mnemonic	Signal Name	Pin Number	Signal Mnemonic	Signal Name
1	DTR0	Data Terminal Ready 0	26	GND	Ground
2	DCD0	Data Carrier Detect 0	27	TXD2	Transmit Data 2
3	DTR1	Data Terminal Ready 1	28	RING2	Ring 2
4	DCD1	Data Carrier Detect 1	29	RXD2	Receive Data 2
5	DTR2	Data Terminal Ready 2	30	GND	Ground
6	DCD2	Data Carrier Detect 2	31	TXD3	Transmit Data 3
7	DTR3	Data Terminal Ready 3	32	RING3	Ring 3
8	DCD3	Data Carrier Detect 3	33	RXD3	Receive Data 3
9	DTR4	Data Terminal Ready 4	34	GND	Ground
10	DCD4	Data Carrier Detect 4	35	TXD4	Transmit Data 4
11	DTR5	Data Terminal Ready 5	36	RING4	Ring 4
12	DCD5	Data Carrier Detect 5	37	RXD4	Receive Data 4
13	DTR6	Data Terminal Ready 6	38	GND	Ground
14	DCD6	Data Carrier Detect 6	39	TXD5	Transmit Data 5
15	DTR7	Data Terminal Ready 7	40	RING5	Ring 5
16	DCD7	Data Carrier Detect 7	41	RXD5	Receive Data 5
17	GND	Ground	42	GND	Ground
18	GND	Ground	43	TXD6	Transmit Data 6
19	TXD0	Transmit Data 0	44	RING6	Ring 6
20	RING0	Ring 0	45	RXD6	Receive Data 6
21	RXD0	Receive Data 0	46	GND	Ground
22	GND	Ground	47	TXD7	Transmit Data 7
23	TXD1	Transmit Data 1	48	RING7	Ring 7
24	RING1	Ring 1	49	RXD7	Receive Data 7
25	RXD1	Receive Data 1	50	GND	Ground

Table 2-3. I/O Port Connector J3 Pin Assignments

Pin Number	Signal Mnemonic	Signal Name	Pin Number	Signal Mnemonic	Signal Name
1	DTR8	Data Terminal Ready 8	26	GND	Ground
2	DCD8	Data Carrier Detect 8	27	TXD10	Transmit Data 10
3	DTR9	Data Terminal Ready 9	28	RING10	Ring 10
4	DCD9	Data Carrier Detect 9	29	RXD10	Receive Data 10
5	DTR10	Data Terminal Ready 10	30	GND	Ground
6	DCD10	Data Carrier Detect 10	31	TXD11	Transmit Data 11
7	DTR11	Data Terminal Ready 11	32	RING11	Ring 11
8	DCD11	Data Carrier Detect 11	33	RXD11	Receive Data 11
9	DTR12	Data Terminal Ready 12	34	GND	Ground
10	DCD12	Data Carrier Detect 12	35	TXD12	Transmit Data 12
11	DTR13	Data Terminal Ready 13	36	RING12	Ring 12
12	DCD13	Data Carrier Detect 13	37	RXD12	Receive Data 12
13	DTR14	Data Terminal Ready 14	38	GND	Ground
14	DCD14	Data Carrier Detect 14	39	TXD13	Transmit Data 13
15	DTR15	Data Terminal Ready 15	40	RING13	Ring 13
16	DCD15	Data Carrier Detect 15	41	RXD13	Receive Data 13
17	GND	Ground	42	GND	Ground
18	GND	Ground	43	TXD14	Transmit Data 14
19	TXD8	Transmit Data 8	44	RING14	Ring 14
20	RING8	Ring 8	45	RXD14	Receive Data 14
21	RXD8	Receive Data 8	46	GND	Ground
22	GND	Ground	47	TXD15	Transmit Data 15
23	TXD9	Transmit Data 9	48	RING15	Ring 15
24	RING9	Ring 9	49	RXD15	Receive Data 15
25	RXD9	Receive Data 9	50	GND	Ground

Table 2-4. Connector J1 Pin Assignments (Centronics)

Pin Number	Signal Mnemonic	Signal Name	Pin Number	Signal Mnemonic	Signal Name
1	D7	Data 7	11	CDS*	Data Strobe*
2	D6	Data 6	12	GND	Ground
3	D5	Data 5	13	ACK*	Acknowledge*
4	D4	Data 4	14	FAULT*	Fault*
5	D3	Data 3	15	SEL	Select
6	D2	Data 2	16	BUSY	Busy
7	D1	Data 1	17	PE	Paper Empty
8	D0	Data 0	18	-	Not used
9	GND	Ground	19	IP*	Input Prime*
10	GND	Ground	20	-	Not used

Table 2-5. Connector J1 Pin Assignments (Dataproducts)

Pin Number	Signal Mnemonic	Signal Name	Pin Number	Signal Mnemonic	Signal Name
1	D7	Data 7	11	DPDS	Data Strobe
2	D6	Data 6	12	GND	Ground
3	D5	Data 5	13	DEMAND	Demand
4	D4	Data 4	14	RDY	Ready
5	D3	Data 3	15	ONL	On Line
6	D2	Data 2	16	-	Not used
7	D1	Data 1	17	-	Not used
8	D0	Data 0	18	IIN	Interface In
9	GND	Ground	19	BCLR*	Buffer Clear*
10	GND	Ground	20	IOUT	Interface Out

2.5 Electrical Requirements

The electrical requirements for the VME-ICP16/8 are

- +5 volts.
- +12 volts.

2.6 Environmental Requirements

The VME-ICP16/8 environmental requirements are

- Temperature:

  0 degrees to 70 degrees centigrade (operating)

  –40 degrees to 65 degrees centigrade (non-operating)

- Humidity: 10 to 95 percent (non-condensing)

SECTION 3: CONFIGURATION

This section describes how to configure the VME-ICP16/8 controller board with jumpers.

Figure 3-1 shows the locations of the jumpers. The rest of this section describes the functions and configuration of these jumpers.

3.1 Parallel Port Interface (E1–E6 and E24–E25)

The VME-ICP16/8 parallel printer port can be set for either Centronics or Dataproducts compatibility. The parallel port interface configuration is determined by three sets of jumpers:

- Data Strobe select (E1-E3)
- Acknowledge select (E4-E6)
- Interface select (E24-E25)

Table 3-1 shows the jumper settings for each interface configuration.

Table 3-1. Parallel Port Interface Jumper Settings

Interface	Jumpers
Centronics	E2 to E3 E4 to E5 No jumper on E24 or E25
Dataproducts	E2 to E3 E5 to E6 E24 to E25

3.2 Static RAM Socket Configuration (E9–E14)

Jumpers E9–E14 configure the static RAM sockets to accommodate either 2K x 8 or 8K x 8 static RAMs (see Table 3-2). When using 2K x 8 RAMs, position the RAM chips in the sockets so that Pin 1 of the chip resides in Pin 3 of the socket.

At system power on, the on-board firmware automatically determines which size RAMs are present and adjusts itself accordingly. The VME-ICP16/8 comes with 8K x 8 RAMs.

Table 3-2. Static RAM Jumper Settings

RAM	Jumpers
2K x 8	E9 to E10 E12 to E13
8K x 8	E10 to E11 E13 to E14

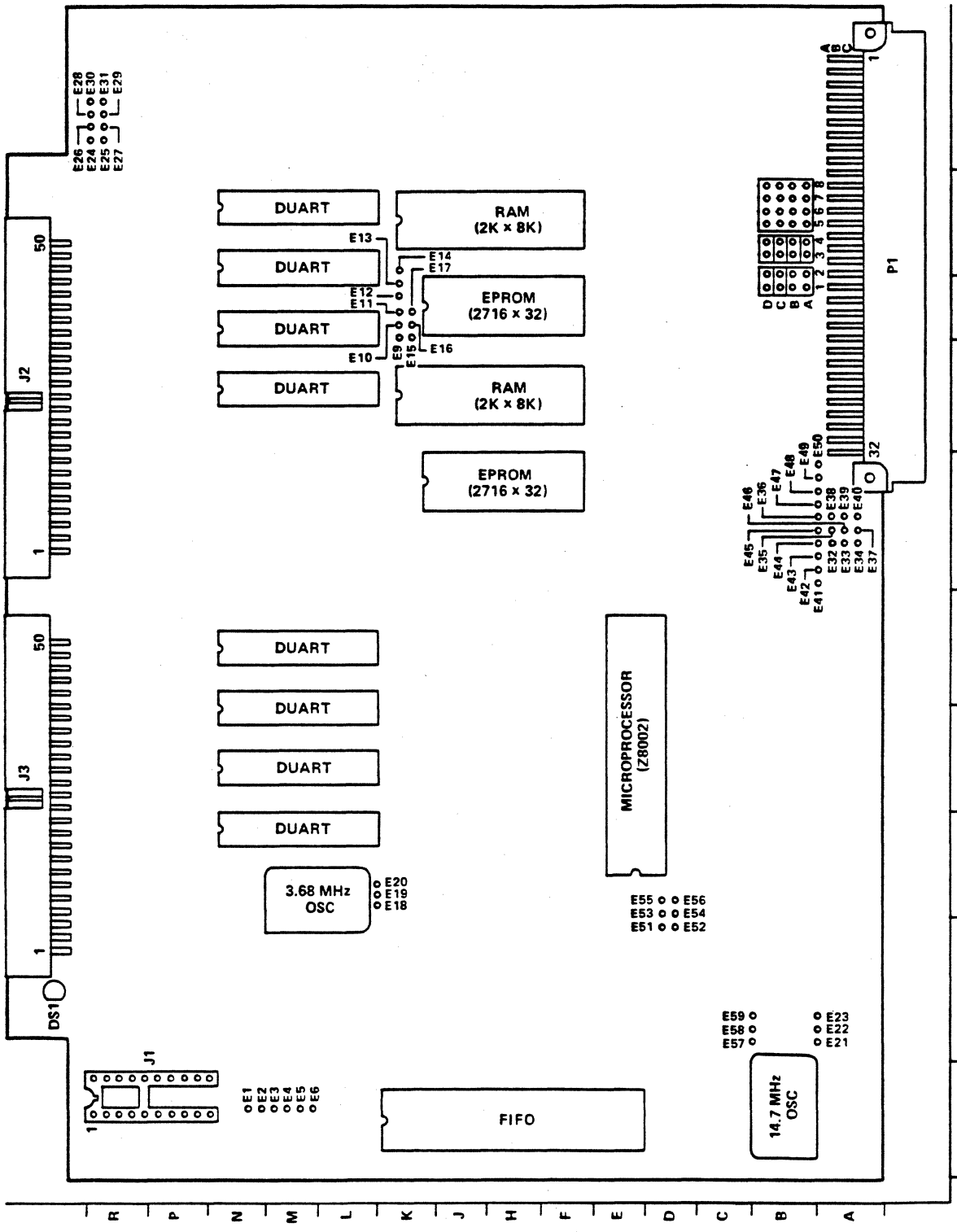

Figure 3-1. VME-ICP16/8 Board Layout

3.3 EPROM Socket Configuration (E15–E17)

Jumpers E15–E17 configure the EPROM sockets to accommodate either 2K x 8 (2716) or 4K x 8 (2732) EPROMs. Integrated Solutions' firmware is resident on two 4K x 8 EPROMs so the factory setting is E16 to E17. Table 3-3 shows the jumper settings.

Table 3-3. EPROM Jumper Settings

EPROM	Jumpers
2716	E15 to E16
2732	E16 to E17

3.4 Clock Generation Jumpers (E18–E23 and E57–E59)

The VME-ICP16/8 board can use two types of control microprocessors: a Z8002A or a Z8002B. These microprocessors use different clock rates; you must set clock generation to match.

Jumpers E18–E23 and E57–E59 support the appropriate control microprocessor as shown in Table 3-4. The VME-ICP16/8 ordinarily comes with a Z8002B.

Table 3-4. Clock Generation Jumper Settings

Microprocessor	Jumpers
Z8002A (6 MHz)	E19 to E20 E22 to E23 E58 to E59
Z8002B (10 MHz)	E19 to E20 E21 to E22 E57 to E58

3.5 Serial Line Configuration (E26-E27)

This jumper chooses between eight or sixteen serial lines on the VME-ICP16/8 board. VME-ICP8 boards have this jumper installed, limiting the serial ports to eight. See Table 3-5.

Table 3-5. Serial Line Jumper Settings

Serial Lines	Jumper
Eight lines	E26 to E27
Sixteen lines	No jumper

3.6 Access Port Jumpers (E28–E31)

These jumpers are currently factory set to open (no jumpers installed).

3.7 Address Selection (E32–E50)

Jumpers E32–E40 determine the number of word locations allocated to the VME-ICP16/8 on the VME bus. Since the board responds to 16 word locations, this jumper configuration is factory set with jumpers from E33 to E34, E35 to E36, and E38 to E39.

Jumpers E41–E50 set the VME-ICP16/8 address location on the VME bus within the address range of FFF000 (hex) and FFFFC0 (hex). Figure 3-2 shows the selectable address bits within the 24-bit address and their corresponding jumper reference designations.

Jumper post E50 is tied to ground, while E41 is tied to +5 volts. Connect posts E42–49 to either E41 or E50 to produce a logical 1 or 0, respectively. The factory default setting is wire-wrapped to FFF520 hex.

Bits	23-12	11	10	9	8	7	6	5	4	3-0
Setting	111111111111	x	x	x	x	x	x	x	x	0000
Jumper	none	E43	E45	E47	E49	E48	E46	E44	E42	none
Default	111111111111	0	1	0	1	0	0	1	0	0000

Note: x = logic level jumper selectable

Figure 3-2. Selectable Address Bits

3.8 Interrupt Request Level (E51–E56, A1–D1, and A2–D2)

The VME-ICP16/8 can select one VME interrupt level from levels 3 through 6; levels 1, 2, and 7 are not available. Set jumpers to select both the Interrupt Request line and the interrupt level code.

Table 3-6 provides the jumper configurations for each of the valid VME-ICP16/8 interrupt levels. The factory default setting is for level 4.

Table 3-6. Interrupt Level Jumper Settings

Level 3	Level 4	Level 5	Level 6
D1 to D2 E55 to E56	C1 to C2 E51 to E52 E53 to E54	B1 to B2 E53 to E54	A1 to A2 E51 to E52

3.9 VME Bus Request Level (A3–D3 and A4–D4)

Jumpers A3–D3 and A4–D4 control the VME bus request level of the VME-ICP16/8 requester. There are four levels of bus request, Bus Request 0 (BRQ0) through BRQ3.

Table 3-7 shows the jumper configurations for each request level. The factory default setting is for level 3.

Table 3-7. Bus Request Level Jumper Settings

BRQ0	BRQ1	BRQ2	BRQ3
D3 to D4	C3 to C4	B3 to B4	A3 to A4

3.10 Bus Grant Level (A5–D5, A6–D6, A7–D7, and A8–D8)

Jumpers A5–D5, A6–D6, A7–D7, and A8–D8 control the VME bus grant level of the VME-ICP16/8. There are four jumper configurations, each corresponding to one of the four Bus Grant levels, BG0 through BG3. The Bus Grant level selected must be the same as the level selected for Bus Request. For instance, if you choose BRQ3 then you must select BG3.

Table 3-8 provides the jumper configurations for each of the Bus Grant levels. The factory default setting is for level 3.

Table 3-8. Bus Grant Level Jumper Settings

BG0	BG1	BG2	BG3
A6 to A7	A6 to A7	A6 to A7	A5 to A6
B6 to B7	B6 to B7	B5 to B6	A7 to A8
C6 to C7	C5 to C6	B7 to B8	B6 to B7
D5 to D6	C7 to C8	C6 to C7	C6 to C7
D7 to D8	D6 to D7	D6 to D7	D6 to D7

SECTION 4: SOFTWARE INTERFACE

This section provides information regarding VME-ICP16/8 programming.

Programming involves placing values in VME bus addressable memory locations corresponding to the device registers on the VME-ICP16/8 board. The number, format, and meaning of the registers supported by the VME-ICP16/8 board is determined by the firmware executing on the board.

Hardware on the VME-ICP16/8 provides support for eight or sixteen asynchronous RS232C serial ports and one parallel printer output port. The rest of this section describes the format of the device registers to support this hardware.

4.1 Register Organization

The firmware supports a group of fourteen 16-bit registers. Figure 4-1 shows the structure of the registers. The last five registers are "indexed registers;" these show different information depending on the line selected in the SEL register.

Default Address	Register	Mnemonic
FFF520	Selector Register	SEL
FFF522	Interrupt Control Register	ICR
FFF524	Line Enable Register	LER
FFF526	Transmit Control Register	TCR
FFF528	Break Register	BRK
FFF52A	Silo Window Register	SWR
FFF52C	Assert Carrier Register	ACR
FFF52E	Detect Carrier Register	DCR
FFF530	Detect Ring Register	DRR
FFF532	Parameter Register	PR
FFF534	Status Register	SR
FFF536	Bus Address High	BAH
FFF538	Bus Address Low	BAL
FFF53A	Byte Count	BC

Figure 4-1. VME-ICP16/8 Device Registers

4.2 Selector Register (SEL)

SEL

Base + 0 (default FFF520)

The SEL clears the controller and selects which block of the indexed registers (PR, SR, BAH, BAL, and BC) to address. The index selection can choose between each of the serial ports, the silo, or the parallel printer port. See Figure 4-2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MC	CLK	MV	unused				Index					unused			

Figure 4-2. Selector Register

Bit definitions for SEL:

- **Bit 15:** Master Clear (MC)—When MC is set all registers return to their power-up state. The operation is not complete until this bit reads as 0.
- **Bit 14:** Clock (CLK)—On the VME-ICP16/8 board this bit must have a value of 0.
- **Bit 13:** Multi-Vector (MV)—This bit determines if the board should use one interrupt vector, or a linear sequence of vectors, one for each interrupt cause. See Section 4.3, "Interrupt Control Register (ICR)." This bit is ignored unless it is set at the same time as is MC.
- **Bits 12–9:** Unused.
- **Bits 8–4:** Index—Selects the current index for the indexed registers, with this code:
  - 0-F hex: the corresponding serial port
  - 10 hex: the silo
  - 11 hex: the parallel printer port

  Other possible values are unused.
- **Bits 3–0:** Unused.

After a Master Clear, reading the SEL can determine the controller configuration, using the format in Figure 4-3.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused								CE	LP	BR	NLINES				

Figure 4-3. Reading the SEL for the Controller Configuration

Bit definitions for SEL Read:

- **Bits 15-7:** Unused.
- **Bit 7:** Centronics Select (CE)—Set to "1" if configured for a Centronics printer interface, "0" if configured for a Dataproducts interface. **Bit 6:** Line Printer (LP)—Set to "1" if the board supports a line printer.
- **Bit 5:** Baud Rate (BR)—Shows the baud rate table being used, between the two in Table 4-1. "0" means the first table, "1" means the second. This is set at the factory.

  See Section 4.11.1, "Line Parameter Register (LPR)," to select specific baud rates.
- **Bits 4-0:** Number of Lines (NLINES)—Provides the number of terminal lines the VME-ICP16/8 board supports (8 or 16).

Table 4-1. Baud Rate Tables

LPR Speed Selection	BR=0	BR=1
0000	75 Baud	50 Baud
0001	110 Baud	110 Baud
0010	134.5 Baud	134.5 Baud
0011	150 Baud	200 Baud
0100	300 Baud	300 Baud
0101	600 Baud	600 Baud
0110	1200 Baud	1200 Baud
0111	2000 Baud	1050 Baud
1000	2400 Baud	2400 Baud
1001	4800 Baud	4800 Baud
1010	1800 Baud	7200 Baud
1011	9600 Baud	9600 Baud
1100	19.2K Baud	38.4K Baud
1101	unused	unused
1110	unused	unused
1111	unused	unused

4.3 Interrupt Control Register (ICR)

ICR Base + 2 (default FFF522)

The ICR controls the generation of interrupts by the VME-ICP16/8 and monitors their status. When writing the ICR, the lower byte is the interrupt vector and the upper byte is the interrupt enable bits. When reading the ICR, the lower byte determines the last interrupt posted, and the upper byte indicates which interrupts are pending. See Figures 4-4 and 4-5.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NIE	SIE	TIE	CIE	RIE	PIE	unused		Vector							
Interrupt enable								Interrupt vector							

Figure 4-4. Writing the Interrupt Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NI	SI	TI	CI	RI	PI	unused		NIP	SIP	TIP	CIP	RIP	PIP	unused	
Interrupt pending								Interrupt posted							

Figure 4-5. Reading the Interrupt Control Register

There are six sources of interrupts listed in order of priority. Their bit numbers and definitions are as follows:

- **Bit 15,7:** Non-existent memory error (NI)—If a VME bus error occurs while obtaining host transmission data, or while transferring the input silo to the host, a non-existent memory interrupt is set pending. This condition is a result of improper programming of the bus address or byte count fields.

- **Bit 14,6:** Silo requiring service (SI)—If a silo age time has passed since the silo was last empty or if the silo fills to or above the alarm level, then a silo service interrupt is set pending. Determine the cause by reading the Status Register (SI) of the silo.
- **Bit 13,5:** Transmitter going empty (TI)—When all the programmed characters have been transmitted on a line, a transmitter interrupt is set pending. Read the Transmit Control Register (TCR) to determine which lines are empty.
- **Bit 12,4:** Carrier state change (CI)—When there is a transition in carrier detect for an enabled line, a carrier interrupt is set pending.
- **Bit 11,3:** Ring state change (RI)—When there is a transition in ring detect for an enabled line, a ring interrupt will be set pending.
- **Bit 10,2:** Printer service (PI)—This interrupt means that the printer requires service. Read the Printer Status Register (PSR) to see what needs service.

The VME-ICP16/8 generates an interrupt under these conditions:

- Board firmware sets an interrupt pending bit
- The host controller sets the corresponding interrupt enable bit
- The interrupt posted field is **0** (no interrupts currently posted)

In issuing an interrupt, the board firmware chooses the highest priority interrupt pending bit, resets it to **0**, and sets the corresponding interrupt posted bit to **1**.

If the board was initialized in multi-vector mode, a different vector is used for each source of interrupt, as indicated in Table 4-2. The base vector, now used for NI interrupts only, is the vector defined in writing the ICR (see Figure 4-4). Otherwise, the last interrupt posted field determines the cause of the interrupt.

In any case, the host controller must read the "Interrupt Posted" field to find the source of interrupt. Reading this field resets the contents to **0**; do not read it indiscriminately.

Table 4-2. Interrupt Vectors

Interrupt	Location
Non-existent memory (NI)	Vector
Silo (SI)	Vector + 1
Transmit (TI)	Vector + 2
Carrier (CI)	Vector + 3
Ring (RI)	Vector + 4
Printer (PI)	Vector + 5

4.4 Line Enable Register (LER)

LER Base + 4 (default FFF524)

Used only in terminal support, the LER is a bit-per-line read-write register. To enable a line, the host should "or in" the appropriate bit. See Figure 4-6.

At power-up this register is 0. Any line which does not have its bit set is considered disabled and is ignored by the VME-ICP16/8.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Line Enabled															

Figure 4-6. Line Enable Register

4.5 Transmit Control Register (TCR)

TCR Base + 6 (default FFF526)

The TCR is a terminal-related bit-per-line read-write register. See Figure 4-7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Transmitter Control															

Figure 4-7. Transmit Control Register

When reading the register, the value indicates which lines have become empty since the previous read of the register. The host should read the register when servicing a transmitter interrupt to determine which lines caused the interrupt.

Reading the register resets its value to 0. The TCR should not be read indiscriminately since the state of the transmitters will be lost.

If two or more lines empty at the same time, only one interrupt is produced.

The host must service each line indicated by the value read in the TCR. To initiate a transmission line, first select the line via the SEL, then program the BAH, BAL, and BC registers with the address and length of a new data block to be transmitted. Next, write to the TCR with the appropriate bit set, starting transmission on the line.

4.6 Break Register (BRK)

BRK Base + 8 (default FFF528)

Used only in terminal support, the BRK is a bit-per-line read-write register. See Figure 4-8.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Break Bits															

Figure 4-8. Break Register

To assert a break condition on a line, the host should "or in" the appropriate bit. When a break bit is

set, the corresponding line, if enabled, transmits a break until the bit is reset by the host. At power-up this register is 0.

4.7 Silo Window Register (SWR)

SWR	Base + A (default FFF52A)

Having the format of a silo frame, the SWR is a read-write word register providing a window into the input data silo. See Figure 4-9.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDP	FE	PE	DO	Line Number				Received Character							

Figure 4-9. Silo Window Register

Byte operations are not permitted on this register. The silo can be emptied by repeatedly reading this register, or by programming the silo's BAH, BAL, and BC registers and setting either the TBI or the TS bit in the silo's SR at the appropriate time. The latter methods result in the silo frames being DMA transferred into host memory for processing. For diagnostic purposes the register can also be written, simulating the reception of a character by placing the value written into the input silo.

An interrupt can be caused without enabling any line on the VME-ICP16/8 by setting a small silo age time and writing a value in this register. After the silo ages, an interrupt is posted. This technique can be useful in the system configuration procedure.

Bit definitions for SWR:

- **Bit 15:** Valid Data Present (VDP)—This bit remains at 1 if the register reflects data which was received and placed into the silo. The bit is 0 if the register is read when there is no data in the silo; in this case the remaining bits are meaningless.
- **Bit 14:** Framing Error (FE)—This bit is set if the received character did not have a stop bit; the bit is set upon reception of a break.
- **Bit 13:** Parity Error (PE)—This bit is set if the parity of the received character does not agree with that designated for the line.
- **Bit 12:** Data Overrun (DO)—This bit is set if received characters were lost on the indicated line. The character in this frame is valid.
- **Bits 11-8:** Line Number—These bits contain the number of the line upon which the data was received.
- **Bits 7-0:** Received Character—These bits contain the received character, right justified. Unused bits are 0, and parity is not shown.

4.8 Assert Carrier Register (ACR)

ACR Base + C (default FFF52C)

The ACR is a bit-per-line read-write register used to assert carrier on a line. To assert carrier on a particular line, "or in" the corresponding bit. See Figure 4-10.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Assert Carrier															

Figure 4-10. Assert Carrier Register

4.9 Detect Carrier Register (DCR)

DCR Base + E (default FFF52E)

This is a bit-per-line read-only register used to detect carriers. If carrier is present on a particular line the corresponding bit is set. If the firmware notes a transition on any enabled line the CI bit of the ICR is set. See Figure 4-11.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Detect Carrier															

Figure 4-11. Detect Carrier Register

4.10 Detect Ring Register (DRR)

DRR Base + 10 (default FFF530)

The DRR is a bit-per-line read-only register that is used to detect carrier. If a ring condition is present on a particular line the corresponding bit is set. If the firmware notes a transition on any enabled line the RI bit of the ICR is set. See Figure 4-12.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Detect Ring															

Figure 4-12. Detect Ring Register

4.11 Parameter Registers (PR)

PR Base + 12 (default FFF532)

There are three different formats of parameter registers corresponding to

- Terminal lines (LPR)
- The input silo (SPR)

The parameter register accessed depends on the "index" value in the SEL.

4.11.1 Line Parameter Register (LPR)

The LPR is a read-write register specifying the operating parameters for a line. This register should be loaded only after the SEL has been programmed to select the line to which the parameters apply. See Figure 4-13.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused			PE	OP	TSB	CLEN		Rx Speed				Tx Speed			

Figure 4-13. Line Parameter Register

Bit definitions for LPR:

- **Bits 15-13:** Unused.
- **Bit 12:** Parity Enable (PE)—If set, parity is enabled for both transmit and receive. Characters transmitted on the line have an appropriate parity bit affixed and characters received on the line are checked for correct parity.
- **Bit 11:** Odd Parity (OP)—If PE is set then this bit determines odd or even parity checking. Setting OP generates and checks odd parity; leaving OP at 0 generates and checks even parity.
- **Bit 10:** Two Stop Bits (TSB)—If clear then one stop bit is indicated. If set with five-bit characters then 1.5 stop bits are used; otherwise two stop bits are used.
- **Bits 9-8:** Character Length (CLEN)—CLEN specifies the length of transmitted and received characters, excluding parity. See Table 4-3.

Table 4-3. CLEN Bit Codes

Bits	Length
00	5 bit
01	6 bit
10	7 bit
11	8 bit

- **Bits 7-4:** Receiver Speed—The receiver speed indicates the baud rate for received characters. Table 4-1 shows the possible values, depending on the baud rate table selected by SEL.
- **Bits 3-0:** Transmitter Speed—The transmitter speed indicates the baud rate for transmitted characters shifting onto the line. Table 4-1 shows the possible values.

4.11.2 Silo Parameter Register (SPR)

Figure 4-14 shows the SPR.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Silo Alarm Level								Silo Age Time							

Figure 4-14. Silo Parameter Register

Bit definitions for the SPR:

- **Bits 15-8:** Silo Alarm Level—If the silo contains more than the specified number of characters the ALRM bit of the SSR register is set.
- **Bits 7-0:** Silo Age Time—If the silo has not been empty for the specified amount of time, then the AGE bit of the SSR register is set.

4.12 Status Registers (SR)

SR

Base + 14 (default FFF534)

Status for both the silo and the parallel printer are available from the SR. There is no SR for the serial lines.

4.12.1 Silo Status Register (SSR)

The Silo SR is a read-write register that provides status information on the terminal input silo. See Figure 4-15.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBI	TS	ALRM	AGE	unused				Silo Fill Level							

Figure 4-15. Silo Status Register

Bit definitions for the SR:

- **Bit 15:** Transfer Silo Before Interrupt (TBI)—This bit is used to initiate the contents of the silo that should be transferred to the host before posting a silo interrupt to the host. The bit should be set by the host after the programming of the silo's BAH, BAL, and BC registers. The host can interrogate silo frames at the specified location in the silo interrupt handler.
- **Bit 14:** Transfer Silo (TS)—This bit is used to initiate and indicate completion of a block transfer of silo frames from the VME-ICP16/8 to the host. The bit should be set by the host after the programming of the silo's BAH, BAL, and BC registers to initiate the transfer of silo frames to the host. The host can then interrogate the frames after the firmware has cleared this bit.
- **Bit 13:** Silo Alarmed (ALRM)—This bit is set by the firmware if the silo reaches a depth greater than that specified in the SPR. If this bit is set, then the SI bit of the ICR will also be set. If the TBI bit of this register is set, the silo will be transferred to host memory before posting the interrupt.
- **Bit 12:** Silo Aged (AGE)—The firmware sets this bit if the oldest character in the silo has been in the silo for more than the amount of time specified in the SPR. If this bit is set then the SI bit of the ICR will also be set. If the TBI bit of this register is set, the silo will be transferred to host memory before posting the interrupt.
- **Bits 11-8:** Unused.
- **Bits 7-0:** Silo Fill Level—This shows the current level of the silo.

4.12.2 Printer Status Register (PSR)

The PSR gives the host CPU information on the printer status. This register presents different information depending on the brand of printer interface you are using. See Figure 4-16.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE	FF	RE	PS	BY	PE	unused								FL	GO

Figure 4-16. Printer Status Register

Bit definitions for the PSR:

- **Bit 15:** FIFO Empty (FE)—Used internally, to show an empty FIFO.
- **Bit 14:** FIFO Full (FF)—Used internally, to show a full FIFO.
- **Bit 13:** Printer Ready (RE)—This bit shows that the printer is ready to receive data.
- **Bit 12:** Printer Selected (PS)—This bit shows "1" when the SELECT button on the printer has been pushed.
- **Bit 11:** Printer Busy (BY)—This bit shows that the printer is currently printing.
- **Bit 10:** Paper Empty (PE)—This bit sets to 1 when the printer runs out of paper. This bit works only with Centronics printers.
- **Bits 9-2:** Unused.
- **Bit 1:** Flush (FL)—Flushes data for the printer. Not used with UNIX drivers.
- **Bit 0:** Go (GO)—Tells the printer to begin operation.

To operate the printer, set the BAH, BAL, and BC registers, then set the GO bit (Bit 0) of the PSR to "1."

4.13 Bus Address Register High (BAH)

BAH

Base + 16 (default FFF536)

The BAH holds the upper eight bits of the byte address where transmitted data resides. This register should not be programmed until the appropriate line number is selected via the SEL. The host locations containing the transmitted data should not be modified until the transmit operation is complete. See Figure 4-17.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused								Bus Address High							

Figure 4-17. Bus Address Register High

4.14 Bus Address Register Low (BAL)

BAL Base + 18 (default FFF538)

The BAL holds the lower 16 bits of the byte address where transmitted data resides. This register should not be programmed until the appropriate line number is selected via the SEL. The host locations containing the transmitted data should not be modified until the transmit operation is complete. See Figure 4-18.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bus Address Low															

Figure 4-18. Bus Address Register Low

4.15 Byte Count Register (BC)

BC Base + 1A (default FFF53A)

This is a read-write register. As with the LP, BAH, and BAL registers, this register should not be programmed without first selecting the line numbers with the "index" in the SEL. See Figure 4-19.

For terminal lines this register should be loaded with the number of characters (bytes) to output. For the silo this register should contain the maximum number of bytes of silo information to transfer to the host.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Number of Bytes															

Figure 4-19. Byte Count Register

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