Publication Number C29-531R02

UNIVERSAL CLOCK MODULE

PROGRAMMING MANUAL

PERKIN-ELMER

Computer Systems Division
2 Crescent Place
Oceanport, N.J. 07757

PAGE REVISION STATUS SHEET

PUBLICATION NUMBER 29-531

TITLE Universal Clock Module Programming Manual

REVISION R02 DATE November 1979

PAGE	REV.	DATE	PAGE	REV.	DATE	PAGE	REV.	DATE
i/ii	R01	9/78						
iii	R01	9/78						
iv	R00	2/78						
1-1/1-2	R01	9/78						
2-1	R00	2/78						
2-2	R02	11/79						
2-3	R01	9/78						
2-4	R02	11/79						
2-5	R00	2/78						
2-6	R02	11/79						
2-7/2-8	R01	9/78						
3-1	R00	2/78						
3-2	R01	9/78						
3-3/3-4	R00	2/78						
A-1	R00	2/78						
A-2	R01	9/78						
A-3 thru A-6	R00	2/78						
A-7	R01	9/78						
A-8 thru A-15	R00	2/78						

PREFACE

This manual provides the systems programmer or operator with a description of the Universal Clock Module and its operation. The user should be familiar with the 16-bit and 32-bit processors. Chapter 1 is a general introduction. Chapter 2 describes in detail the principles and operation of the precision interval clock (PIC). Chapter 3 also contains a detailed description of the principles and operation of the line frequency clock (LFC).

TABLE OF CONTENTS

APPENDICES

FIGURES

TABLE OF CONTENTS (Continued)

TABLES

CHAPTER 1
INTRODUCTION

1.1 GENERAL OVERVIEW OF THE UNIVERSAL CLOCK MODULE

The universal clock module is a versatile timer consisting of two independent clock devices:

- line frequency clock (LFC)

- precision interval clock (PIC)

Both clocks provide timer controlled processor interrupts, but have different timing mechanisms. The LFC is derived directly from the AC power line and has a fixed clock rate equal to twice the line frequency. The user has no control over the LFC other than to disable, enable, or disarm interrupts. The PIC, although derived from an 8-megahertz crystal oscillator, is dynamically variable through program control. The user can select an increment of time (resolution rate) and a count (interval count) where:

resolution rate x interval count = interval

1.1.1 Device Addresses

Both the PIC and LFC have a specified 10-bit device address. The preferred address for the PIC is a 6C (hexadecimal) and for the LFC is 6D (hexadecimal). However, if another address is assigned, it must be an even numbered address for the PIC and an odd numbered address for the LFC. The address for the LFC is always the address of the PIC plus one. The first two most-significant bits of both 10-bit addresses are always set to zero. The possible device addresses are in the range of 1 to 127 (2^8-1).

PIC's	00	0110	1100	BINARY
ADDRESS	0	6	C	HEX

LFC's	00	0110	1101	BINARY
ADDRESS	0	6	D	HEX

CHAPTER 2
OPERATION OF THE PRECISION INTERVAL CLOCK (PIC)

2.1 GENERAL PRINCIPLES

The precision interval clock (PIC) produces or queues a processor interrupt. A specified time interval determines the point at which the interrupt occurs. An interval is defined as the time between events or states. An interval starts when the previous interval expires and ends when its allotted time period expires. The duration of the interval is measured in increments of time as selected by the user. These increments of time are the resolution rates. Four resolution rates are derived from a master time base. The master time base is supplied by an 8-megahertz internal crystal oscillator that produces a 1-megahertz signal. This oscillator, however, can be disabled to allow the user to substitute his own external master time base oscillator. In addition, the number of times a specified resolution rate is to occur in an interval is called the interval count and is also specified by the user.

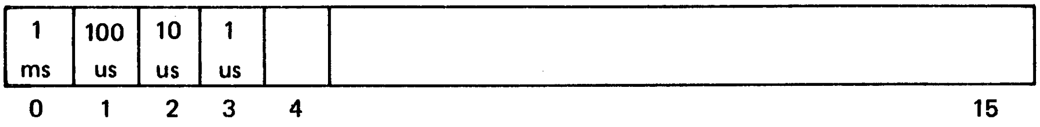
A basic structure of the PIC as shown in Figure 2-1 is explained in the following paragraphs.

2.1.1 Resolution Rate and Initial Interval Count

The four resolution rates derived from the crystal oscillator are:

1 microsecond	(1 us)
10 microseconds	(10 us)
100 microseconds	(100 us)
1 millisecond	(1 ms)

RESOLUTION RATES



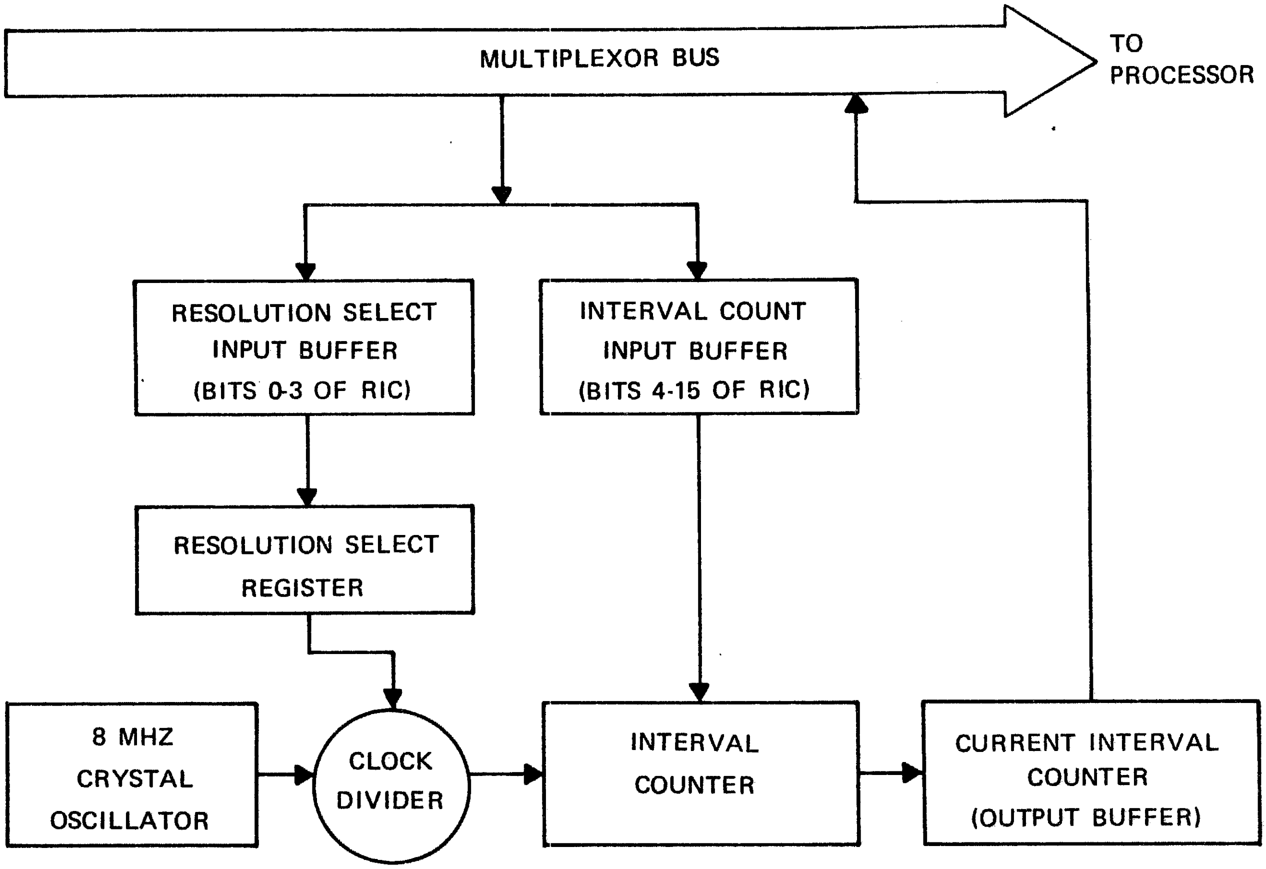

MULTIPLEXOR BUS
TO PROCESSOR
RESOLUTION SELECT INPUT BUFFER (BITS 0-3 OF RIC)
INTERVAL COUNT INPUT BUFFER (BITS 4-15 OF RIC)
RESOLUTION SELECT REGISTER
8 MHZ CRYSTAL OSCILLATOR
CLOCK DIVIDER
INTERVAL COUNTER
CURRENT INTERVAL COUNTER (OUTPUT BUFFER)

Figure 2-1 Precision Interval Clock (PIC)

If the bit that represents the desired resolution rate is set, the appropriate resolution rate is produced. If more than one bit is specified, the shortest resolution rate is used. If no bits are specified, the interval does not take place.

Once the resolution rate is selected, the desired number of times that resolution is to occur must also be specified through the interval counter. The value in the interval counter, the initial interval count, determines how many times the selected resolution rate occurs in an interval. This count must be a hexadecimal number with a decimal value in the range of 0 to 4,095 (2^{12}). The initial interval count should be specified as the desired number. If zero is specified as the count, it is ignored and a value of one is assumed. If no value is specified as the count, the initial interval count specified in the previous interval is used. Each time a cycle occurs, the value in the interval counter is decremented by one until a value of zero is reached. A value of zero generates or queues an interrupt.

The resolution rate and the initial interval count (RIC) determine the allotted time period for an interval. The resolution rate and the initial interval count form a halfword that initializes or changes the resolution select register and interval counter in the PIC. During an interval, the initial interval count in the PIC remains unchanged.

RESOLUTION RATE AND INITIAL INTERVAL COUNTER (RIC)

1 ms	100 us	10 us	1 us	INITIAL INTERVAL COUNT
0	1	2	3	4 … 15

Associated with each resolution rate is a range of interval periods that particular resolution is able to produce. These intervals are listed in Table 2-1.

NOTE

> The minimum interval, with a resolution of 1 us, is dependent on the model processor being used.

TABLE 2-1 POSSIBLE INTERVAL PERIODS

RESOLUTION RATE	INTERVAL COUNT (DECIMAL)	INTERVALS PRODUCED
1 MICROSECOND (1 us)	1 2 3 . . . 4,096	1 us 2 us 3 us . . . 4,096 us
10 MICROSECONDS (10 us)	1 2 3 . . . 4,096	10 us 20 us 30 us . . . 40,960 us
100 MICROSECONDS (100 us)	1 2 3 . . . 4,096	100 us 200 us 300 us . . . 409,600 us
1 MILLISECOND (1 ms)	1 2 3 . . . 4,096	1 ms 2 ms 3 ms . . . 4,096 ms

2.1.2 Current Interval Counter

The result of the initial interval count being decremented is called the current interval count (CIC) and is stored in a separate halfword in the PIC. Each time the initial interval count is decremented, the current interval count is replaced with a value that is one less than its previous value. Effectively, the current interval count always contains the current number of cycles remaining to be executed in an interval. The value in the CIC can be in the range of 4,095 to zero. Any time during the interval, the processor can interrogate the CIC without affecting the decrementing of the clock by issuing a read instruction (RD,RDR,RH,RHR).

CURRENT INTERVAL COUNTER

0	0	0	0	CURRENT INTERVAL COUNT	
0	1	2	3	4	15

where:

Bits 0-3 — Bits 0 through 3 are unused and always set to zero.

Bits 4-15 — Bits 4 through 15 contain the decrementing interval count.

2.1.3 Command Byte

Since the PIC produces interrupts at the conclusion of each interval, three options are available to the user to determine whether or not an interrupt is to occur at the conclusion of the interval or not at all. A fourth option allows the user to stop the clock at any point, establish a new interval, and restart the clock. These options are:

- disable interrupts
- enable interrupts
- disarm interrupts
- start clock

All four options are derived from the three most-significant bits in a byte which is called the command byte. If the bit that represents the desired interrupt mode is set, the appropriate action takes place at the conclusion of the interval. If no bits are set, the disarm mode is the default.

COMMAND BYTE

DISARM							
DISABLE	ENABLE	START	0	0	0	0	0
0	1	2	3	4	5	6	7

where:

DISABLE If bit 0 is set and the end of the interval occurs, the PIC is unable to interrupt the processor but allows the interrupts to be queued.

ENABLE If bit 1 is set and the end of the interval occurs, the PIC immediately interrupts the processor.

DISARM If both bits 0 and 1 are set and the end of the interval occurs, the PIC is unable to interrupt the processor and does not allow interrupts to be queued. In effect, all interrupts are ignored.

START If bit 2 is set at the beginning, during, or end of an interval, the clock immediately stops. The resolution select register and interval counter are loaded with new data from the input buffers and the clock restarts.

BITS 3-7 Bits 3 through 7 are unused and are always set to zero.

2.1.4 Status Byte

The status byte indicates whether or not the resolution rate and initial interval count from the input buffers have been successfully loaded into the resolution select register and interval counter. The RIC is loaded a byte at a time when a write halfword (WH,WHR) instruction is executed. If a processor interrupt occurs in the system before the second byte is loaded, the overflow bit is set. At this point, the PIC contains the four resolution bits and the four most-significant bits (bits 4-7 of byte 1) of the initial interval count. When the overflow bit is set, it should be reset by one of the following before the next interval takes place:

- execution of a sense status (SS,SSR) instruction (32-bit)

- execution of an acknowledge interrupt (AI,AIR) instruction (16-bit)

- initialization (32- and 16-bit)

Then execution of an output command (OC,OCR) sends the command byte to the PIC with the start bit set. This transfer causes the remaining value in the RIC (bits 8-15) to be loaded into the least-significant byte of the interval counter. When the second byte is loaded, the PIC starts decrementing the value currently in the interval counter.

If the overflow bit is not reset, the status byte will not be accurate for the next interval; and as a result, does not indicate whether or not the resolution select register and interval counter were successfully loaded.

2.2 BASIC PIC OPERATION

The command byte and the RIC should be defined before a write instruction is issued. First, the interrupt bit in the command byte should be set and sent to the PIC by execution of an output command. The desired interval count and one of the resolution rate bits in the RIC should then be set. A write data (WD) or write halfword (WH) instruction is then executed to load the resolution rate and initial interval count, a byte at a time, into their input buffers. They remain in the input buffers until either new data is loaded or an output command (OC,OCR) is executed. The input buffers can be loaded with new data anytime during an interval. The start bit in the command byte should then be set and sent to the PIC by execution of another output command. This process causes the clock to start decrementing. If no interrupt bits are set in the command byte, the clock starts and the interval counter begins decrementing at the selected resolution rate. Then, either bit 0 or 1 in the command byte should be set to acknowlege interrupts. Anytime during this interval, the processor can monitor the decrementing interval count by issuing a read instruction. However, the contents of the current interval counter does not change during the reading process. Also, anytime during this interval, new data can be sent to the input buffers either to immediately change the resolution rate and interval count or to wait until the current interval count terminates to start a new interval. When the current interval counter finally has a value of zero, the resolution select register and interval counter are loaded with data from the input buffers and another interval takes place. Figure 2-2 shows the flow of data at the beginning of the interval from the RIC to the CIC at the end of the interval. If it is necessary to stop the PIC during an interval, set the RIC to all zeros and issue a start command.

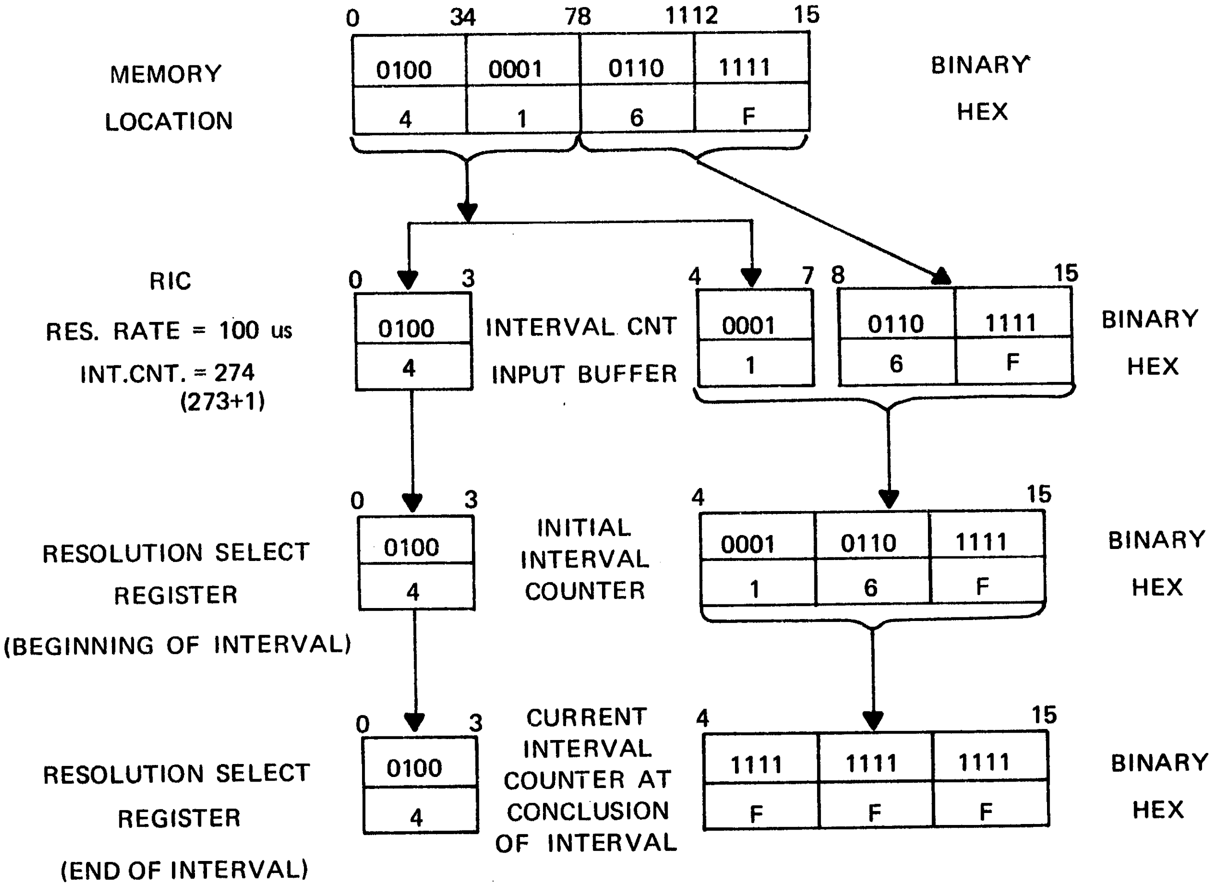


Figure 2-2 Flow of Data to PIC

2.3 INITIALIZATION

Initialization occurs when the machine is powered up or when the initialize button is pressed. It affects the PIC by setting the following locations to zeros:

- resolution select register

- initial interval counter

- resolution rate and initial interval count (RIC)

- current interval counter (CIC)

- status byte

Initialization can also occur when bits 0 and 1 are set in the command byte and an output command is issued which puts the PIC in the disarm mode.

CHAPTER 3
OPERATION OF THE LINE FREQUENCY CLOCK (LFC)

3.1 GENERAL PRINCIPLES

The line frequency clock (LFC) generates or queues a processor interrupt. The point at which the interrupt occurs is determined by a fixed clock rate that is derived from the frequency of the AC power line. The power line frequency is either 60 or 50 hertz and the clock rate is always twice the line frequency. The duration of the interval for each power line frequency is shown in Table 3-1.

TABLE 3-1 DURATION OF INTERVAL IN RELATION TO LINE FREQUENCY

POWER LINE FREQUENCY	DURATION OF INTERVAL
60 Hz	8.33 ms
50 Hz	10.00 ms

An example of the structure of the LFC is shown in Figure 3-1.

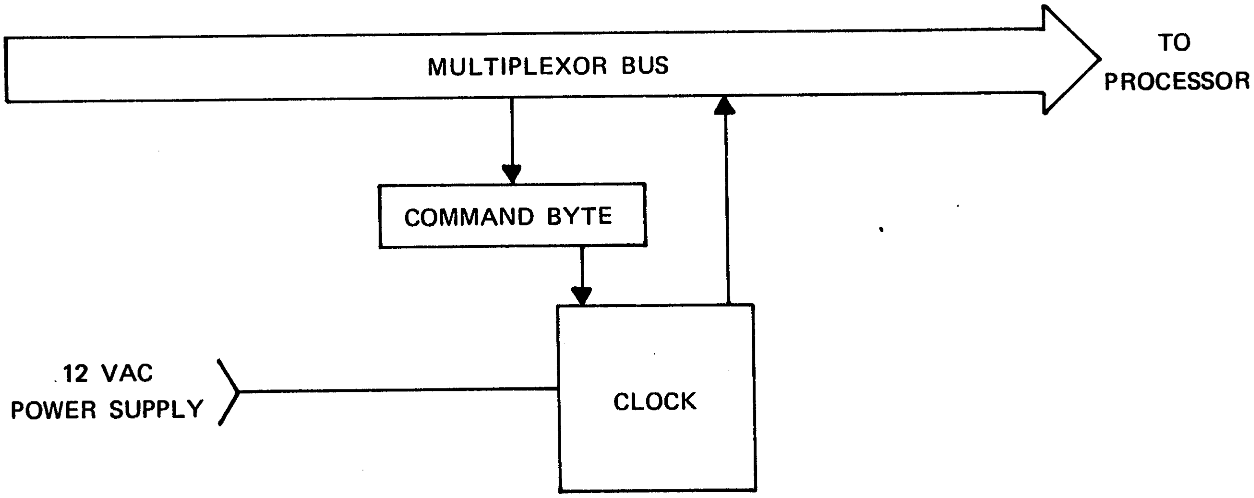


Figure 3-1 Flow of Data to LFC

3.1.1 Command Byte

Since the LFC produces interrupts at twice the line frequency, three options are available to the user to determine whether or not that interrupt is to occur at the conclusion of thé interval or not at all. These options are:

- disable interrupts

- enable interrupts

- disarm interrupts

All three options are derived from the first two most-significant bits in a byte called the command byte. If the bit that represents the desired interrupt mode is set, the appropriate action takes place at the end of one half the period of the line frequency.

COMMAND BYTE

<table>
<tr><th colspan="2">DISARM</th><th></th><th></th><th></th><th></th><th></th><th></th></tr>
<tr><td>DISABLE</td><td>ENABLE</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td></tr>
</table>

where:

DISABLE If bit 0 is set and twice the line frequency occurs, the LFC is unable to interrupt the processor but allows the interrupts to be queued.

ENABLE If bit 1 is set and twice the line frequency occurs, the LFC immediately interrupts the processor.

DISARM If both bits 0 and 1 are set and twice the line frequency occurs, the LFC is unable to interrupt the processor and does not allow interrupts to be queued. In effect, all interrupts are ignored.

BITS 2-7 Are unused and always set to zero.

When the LFC generates an interrupt, it should be serviced with one of the following:

- acknowledge interrupt instruction (16-bit)
- immediate interrupt, auto driver channel (32-bit)
- an appropriate channel command block (16- and 32-bit)

If the sense status or acknowledge interrupt instruction is executed, a status of all zeros is returned.

3.2 BASIC LFC OPERATION

The command byte should be defined to indicate the desired interrupt mode. Then, an output command (OC,OCR) is issued. Execution of an output command transfers the command byte to the clock. If interrupts are enabled, the next possible interrupt and all following interrupts are generated. If interrupts are disabled, the next possible interrupt and all following interrupts are queued. If interrupts are disarmed, all interrupts are ignored.

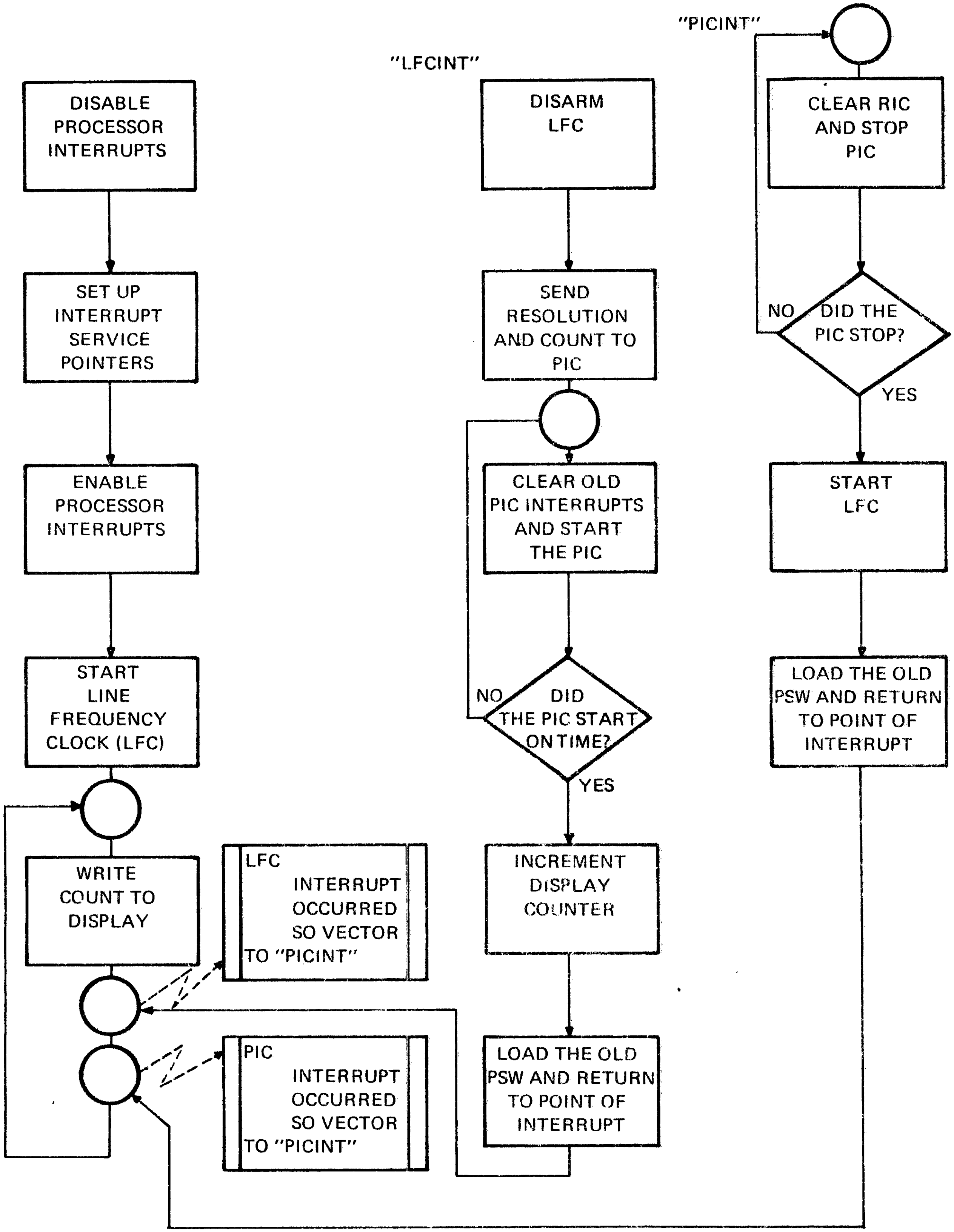
3.3 INITIALIZATION

Initialization occurs when the machine is powered up or when the initialize button is pressed. After initialization, the LFC is left in disarm mode.

Initialization can also occur when bits 0 and 1 are set in the command byte and an output command is issued which puts the LFC in disarm mode.

APPENDIX A
PROGRAMMING EXAMPLES FOR 16-BIT AND 32-BIT PROCESSORS

The following flowcharts and printouts are programming examples for the LFC and the PIC.


"PICINT"
"LFCINT"
DISABLE PROCESSOR INTERRUPTS
SET UP INTERRUPT SERVICE POINTERS
ENABLE PROCESSOR INTERRUPTS
START LINE FREQUENCY CLOCK (LFC)
WRITE COUNT TO DISPLAY
LFC INTERRUPT OCCURRED SO VECTOR TO "PICINT"
PIC INTERRUPT OCCURRED SO VECTOR TO "PICINT"
DISARM LFC
SEND RESOLUTION AND COUNT TO PIC
CLEAR OLD PIC INTERRUPTS AND START THE PIC
NO
DID THE PIC START ON TIME?
YES
INCREMENT DISPLAY COUNTER
LOAD THE OLD PSW AND RETURN TO POINT OF INTERRUPT
CLEAR RIC AND STOP PIC
NO
DID THE PIC STOP?
YES
START LFC
LOAD THE OLD PSW AND RETURN TO POINT OF INTERRUPT

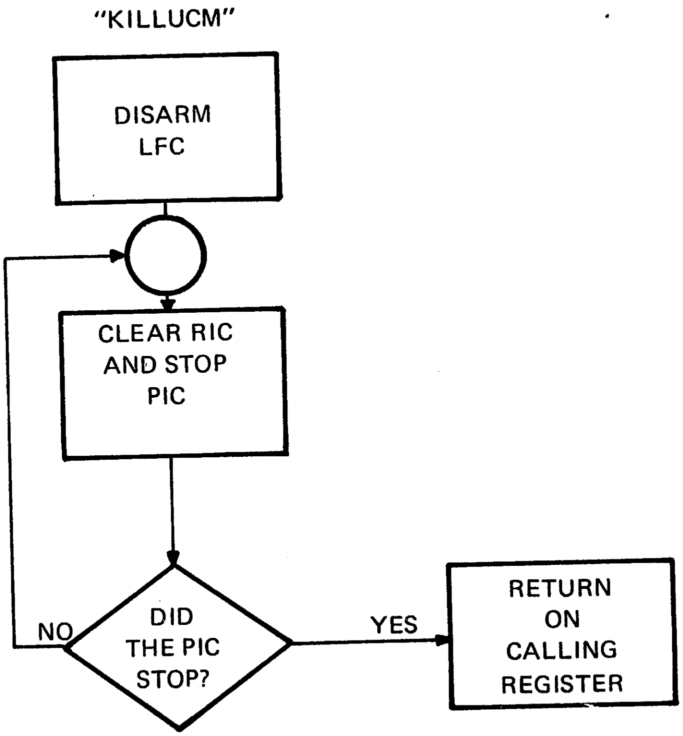
Universal Clock Module 16-Bit Interrupt Programming Example

```
            UNIVERSAL CLOCK MODULE 32 BIT INTERRUPI PROGRAM EXAMPLE   PAGE   1  10:48:05  09/28/78

PROG= *NONE*     ASSEMBLED BY CAL 03-066R05-00   (32-BIT)
                                                                                                              CPE20010
                                  1         CROSS                                                             CPE20020
                                  2         WIDTH 120                                                         CPE20030
                                  3         TARGT 32                                                          CPE20040
                                  4         PROG  UNIVERSAL CLOCK MODULE 32 BIT INTERRUPT PROGRAM EXAMPLE     CPE20050
                                  5         NORX3                                                             CPE20060
                                  6  *******************************************************************     CPE20070
                                  7  *    THIS IS A 32-BIT PROGRAMMING EXAMPLE FOR THE LINE FRLQUENCY  *     CPE20080
                                  8  *  CLOCK AND THE PRECISION INTERVAL CLOCK. THE EXAMPLE USES INTER- *     CPE20090
                                  9  *  RUPIS TO RECOGNIZE THE END OF THE INIERVALS.                    *     CPE20100
                                 10  *  THERL ARE FOUR MODULES:                                         *     CPE20110
                                 11  *            1)"CALLUCM"  THIS MODULE INITIALIZES THE INTLRRUPT    *     CPE20120
                                 12  *              HANDLER AND STARTS THE LINE FREQUENCY CLOCK.        *     CPE20130
                                 13  *            2)"LFCINT"   THIS MODULE SERVICES THE INTERRUPT THAT  *     CPE20140
                                 14  *              OCCURS AFTER THE LINE FREQUENCY CLOCK HAS WAITED    *     CPE20150
                                 15  *              ONE-HALF CYCLE OF THE AC LINE FREQUENCY.            *     CPE20160
                                 16  *              -8.33 MILLISECONDS @ 60 HZ OR 10 MILLISECONDS @50HZ*     CPE20170
                                 17  *              THEN IT STARTS THE PRECISION INTERVAL CLOCK.        *     CPE20180
                                 18  *            3)"PICINT"   THIS MODULE SERVICES THE PRECISION INT-  *     CPE20190
                                 19  *              ERVAL CLOCK INTERRUPT THAT OCCURS AFTER A PROGRAM   *     CPE20200
                                 20  *              CONTROLLED INTERVAL OF 150 MICROSECONDS. IT THEN    *     CPE20210
                                 21  *              RESTARTS THE LINE FREQUENCY CLOCK. THIS MEANS THAT *     CPE20220
                                 22  *              THE PROGRAM WILL CONTINUE TO SERVICE "LFCINT" AND   *     CPE20230
                                 23  *              "PICINT" UNTIL THE FOURTH MODULE IS CALLED.         *     CPE20240
                                 24  *            4)"KILLUCM"  THIS MODULES DISARMS LFC & PIC INTER-    *     CPE20250
                                 25  *              RUPTS  AND STOPS THE PIC.                           *     CPE20260
                                 26  *                                                                  *     CPE20270
                                 27  *******************************************************************

                                                                                                              CPE20290
            0000 0000            29  R0       EQU   0                                                         CPE20300
            0000 0001            30  R1       EQU   1                                                         CPE20310
            0000 0002            31  R2       EQU   2                                                         CPE20320
            0000 0002            32  INTDEV   EQU   2                   MICROCODE PUTS INTERRUPIING ADDRESS I CPE20330
                                 33  **                                 REGISTER 2 OF REGISTER SET 0          CPE20340
            0000 0003            34  R3       EQU   3                                                         CPE20350
            0000 0008            35  R8       EQU   8                                                         CPE20360
            0000 0009            36  R9       EQU   9                                                         CPE20370
            0000 000A            37  R10      EQU   10                                                        CPE20380
            0000 000B            38  NEXTDEV  EQU   11                                                        CPE20390
            0000 000D            39  STATUS   EQU   13                                                        CPE20400
            0000 000F            40  LINK     EQU   15

                                                                                                              CPE20420
000000I  C8A0 3000               42  DISABLL  LHI   R10,X'3000'         GET DISABLE PSW MASK                  CPE20430
000004I  958A                    43           EPSR  R8,R10              NOW UISABLE INTERRUPTS                CPE20440
000006I  2490                    44           LIS   R9,0                CLEAR R9(THE DISPLAYED COUNT REGISTR) CPE20450
000008I  41F0 801A =000026I      45           BAL   LINK,CALLUCM                                              CPE20460
00000CI  2401                    46  WRITE2   LIS   STATUS,1            LOAD STATUS WITH DISPLAT ADDRESS      CPE20470
00000EI  DED0 80A0 =000082I      47           OC    STATUS,INCRMT       PUT DISPLAY IN INCREMENTAL MODE       CPE20480
000012I  08F9                    48           LR    LINK,R9             LOAD CONTENTS OF R9 INTO LINK AND     CPE20490
000014I  94FF                    49           EXBR  LINK,LINK           WRITE VALUE ON DISPLAY PANEL
```

```
0016R  98UF                    WHR    STATUS,LINK                                             CPE00500
0018R  DED0 00D5R              OC     STATUS,NORM          PUT DISPLAY IN NORMAL MODE         CPE00510
001CR  4300 000CR        WAIT  B      WRITE2               DISPLAY COUNT UNTIL CLOCK INTERRUPTS CPE00520


0020R  D080 00DCR     CALLUCM  STM    R8,RSAVE             SAVE CURRENT USER'S REGISTERS      CPE00540
0024R  C8A0 3000               LHI    R10,X'3000'          SET DISABLE INT PSW REGISTER       CPE00550
0028R  958A                    EPSR   R8,R10               DISABLE INTERRUPTS AT PROCESSOR    CPE00560
002AR  C8A0 004ER              LHI    R10,LFCINT           GET ADDRESS OF LFC INTRPT HANDLER  CPE00570
002ER  40A0 01AA               STH    R10,X'D0'+X'DA'      STORE IT IN INTRPT SERVICE POINTER CPE00580
                      **************                  NOTE DA=2*6D HEX'6D' IS THE PREFFERRED  CPE00590
                      **************                       ADDRESS OF THE LINE FREQUENCY CLOCK CPE00600
0032R  C8A0 007ER              LHI    R10,PICINT           GET ADDRESS OF THE PIC INTRPT HANDLR CPE00610
0036R  40A0 01A8               STH    R10,X'D0'+X'D8'      STORE IT IN THE INTRPT SERVICE POINT CPE00620
                      **************                  NOTE D8=2*6C HEX'6C' IS THE PREFFERRED  CPE00630
                      **************                       ADDRESS OF THE PRECISION CLOCK     CPE00640
003AR  C8A0 4800               LHI    R10,X'4800'          SET INTRPT PSW IN REGISIER         CPE00650
003ER  958A                    EPSR   R8,R10               ENABLE INTERRUPTS AT PROCESSOR     CPE00660
0040R  4860 00CER     LFCST1   LH     NEXTDEV,LFC          GET LFC ADDRESS                    CPE00670
0044R  DE60 00D0R              OC     NEXTDEV,LFCSTCMD     START LFC                          CPE00680
0048R  D180 00DCR              LM     R8,RSAVE             RESTORE REGISTERS                  CPE00690
004CR  030F                    BR     LINK                 RETURN TO CALLING PROGRAM & WAIT FOR CPE00700
                      **************                       INTERRUPT                          CPE00710


       0000 004ER     LFCINT   EQU    *                    LFCINTERRUPT HANDLER               CPE00730
004ER  0000           OLDPSWA  DC     0                    LOCATION TO SAVE THE OLD PSW       CPE00740
0050R  0000           OLDLOCA  DC     0                    LOCATION TO SAVE THE OLD LOC       CPE00750
0052R  3000           NEWPSWA  DC     X'3000'              NEW PSW FOR INTERRUPT HANDLER      CPE00760
0054R  D000 00DCR              STM    R0,RSAVE             SAVE USER'S REGISTERS              CPE00770
0058R  4820 00CER              LH     INTDEV,LFC           GET LFC ADDRESS                    CPE00780
005CR  4860 00CCR              LH     NEXTDEV,PIC          GET PIC ADDRESS                    CPE00790
0060R  DE20 00D1R              OC     INTDEV,DISARM        STOP & DISARM LFC                  CPE00800
0064R  D860 00D6R     PICST1   WH     NEXTDEV,INTRVL       SET RESOLUTION                     CPE00810
0068R  DE60 00D2R              OC     NEXTDEV,DISARMST     CLEAR PIC INTERRUPTS & START PIC   CPE00820
006CR  DE60 00D3R              OC     NEXTDEV,ENABLE       ENABLE PIC INTERRUPTS              CPE00830
0070R  908D                    SSR    NEXTDEV,STATUS       DID THE PIC START ON TIME?         CPE00840
0072R  2087                    BTCS   8,PICST1             NO, START IT AGAIN                 CPE00850
0074R  D100 00DCR              LM     R0,RSAVE             RESTORE USER'S REGISTERS           CPE00860
0078R  2691                    AIS    R9,1                 INCREMENT COUNT REGISTER           CPE00870
007AR  C200 004ER              LPSW   OLDPSWA              AND RETURN                         CPE00880


       0000 007ER     PICINT   EQU    *                    PIC INTERRUPT HANDLER              CPE00900
007ER  0000           OLDPSWB  DC     0                    LOCATION TO SAVE THE OLD PSW       CPE00910
0080R  0000           OLDLOCB  DC     0                    LOCATION TO SAVE THE OLD LOC       CPE00920
0082R  3000           NEWPSWB  DC     X'3000'              NEW PSW FOR INTERRUPT HANDLER      CPE00930
0084R  D000 00DCR              STM    R0,RSAVE             SAVE USER'S REGISTERS              CPE00940
0088R  4820 00CCR              LH     INTDEV,PIC           GET PIC ADDRESS                    CPE00950
008CR  4860 00CER              LH     NEXTDEV,LFC          GET LFC ADDRESS                    CPE00960
0090R  D820 0008R     PICSTOP  WH     INTDEV,ZERO          YES, CLEAR RIC,                    CPE00970
0094R  DE20 00D2R              OC     INTDEV,DISARMST      AND STOP PIC                       CPE00980
```

```
     UNIVERSAL CLOCK MODULE 32 BIT INTERRUPT PROGRAM EXAMPLE   PAGE   3  10:48:05  09/28/78

0000881  D080 802C =000088I     97  KILLUCM  STM    R8,RSAVE              SAVE REGISTERS                       CPE20970
00008C1  48B0 801C =0000ACI     98           LH     NEXTDEV,LFC           GET LFC ADDRESS                      CPE20980
0000901  4820 8016 =0000AAI     99           LH     INTDEV,PIC            GET PIC ADDRESS                      CPE20990
0000941  DEB0 8017 =0000AFI    100           OC     NEXTDEV,DISARM        STOP LFC & CLEAR INTERRUPTS          CPE21000
000098I  D820 801A =0000B6I    101  PICKILL  WH     INTDEV,ZERO           CLEAR PIC RESOLUTION COUNTER         CPE21010
00009CI  DE20 8010 =0000B0I    102           OC     INTDEV,DISARMST       STOP PIC & CLEAR INTERRUPTS          CPE21020
0000A0I  9D2D                  103           SSR    INTDEV,STATUS         DID THE PIC STOP?                    CPE21030
0000A2I  2085                  104           BTBS   8,PICKILL             NO GO STOP IT                        CPE21040
0000A4I  D180 8010 =0000B8I    105           LM     R8,RSAVE              RESTORE REGISTERS AND                CPE21050
0000A8I  030F                  106           BR     LINK                  RETURN TO CALLING PROGRAM            CPE21060


                               108  **************  COMMANDS FOR THE PRECISION INTERVAL CLOCK                   CPE21080
                               109  **************  AND THE LINE FREQUENCY CLOCK                               CPE21090
0000AAI  006C                  110  PIC      DC     X'6C'                 STANDARD PIC ADDRESS                 CPE21100
0000ACI  006D                  111  LFC      DC     X'6D'                 STANDARD LFC ADDRESS                 CPE21110
0000AEI  40                    112  LFCSTCMD DB     X'40'                 LFCSTART COMMAND ENABLES INTERRUPTS  CPE21120
0000AFI  C0                    113  DISARM   DB     X'C0'                 LFC DISARMS COMMAND CLEAR INTERRUPTS CPE21130
0000B0I  E0                    114  DISARMST DB     X'E0'                 PIC DISARM AND START COMMAND         CPE21140
0000B1I  40                    115  ENABLE   DB     X'40'                 PIC ENABLE INTERRUPTS COMMAND        CPE21150
0000B2I  40                    116  INCRMT   DB     X'40'                 DISPLAY COMMAND - INCREMENTAL MODE   CPE21160
0000B3I  80                    117  NORM     DB     X'80'                 DISPLAY COMMAND - NORMAL MODE        CPE21170
0000B4I  1096                  118  INTRVL   DC     X'1096'               150 MICROSECONDS @ 1 MS RESOLUTION   CPE21180
0000B6I  0000                  119  ZERO     DC     X'0000'               ZEROES TO CLEAR RIC                  CPE21190
0000B8I                        120           ALIGN  4                     ALIGN RSAVE AREA ON FULLWORD BOUNDARY CPE21200
0000B8I                        121  RSAVE    DS     16*ADC                REGISTER SAVE AREA FOR 16 USER REGIST CPE21210
0000F8I                        122           END                                                           CPE21220
```

```
      UNIVERSAL CLOCK MODULE 16 BIT INTERRUPT PROGRAM EXAMPLE   PAGE   4  10:47:03  09/28/78
   ASSEMBLED BY CAL 03-066R05-00   (32-BIT)

   START OPTIONS:  SCR,TA=16

      NO CAL ERRORS
      NO CAL WARNINGS
       2 PASSES

    ABSTOP     0000 0000
    ADC        0000 0002       130
    CALLUCM    0000 0020R       45     54*
    DISABLE    0000 0000R       42*
    DISARM     0000 00D1R       80    109    122*
    DISARMST   0000 00D2R       82     98    111    123*
    ENABLE     0000 00D3R       83    124*
    IMPTOP     0000 00FCR
    INCRMT     0000 00D4R       47    125*
    INTDEV     0000 0002        32*    78     80     95     97     98     99    108    110    111    112
    INTRVL     0000 00D6R       81    127*
    KILLUCM    0000 00AAR      106*
    LADC       0000 0001
    LFC        0000 00CER       67     78     96    107    120*
    LFCINT     0000 004ER       57     73*
    LFCS11     0000 0040R       67*
    LFCS12     0000 009CR      101*
    LFCSICMD   0000 00D0R       68    101    121*
    LINK       0000 000F        40*    45     48     49     49     50     70    115
    NEWPSWA    0000 0052R       76*
    NEWPSWB    0000 0082R       93*
    NEXTDEV    0000 0008        38*    67     68     79     81     82     83     84     96    101    107    109
    NORM       0000 00D5R       51    126*
    OLDLOCA    0000 0050R       75*
    OLDLOCB    0000 0080R       92*
    OLDPSWA    0000 004ER       74*    88
    OLDPSWB    0000 007ER       91*   104
    PIC        0000 00CCR       79     95    108    119*
    PICINT     0000 007ER       61     90*
    PICKILL    0000 00BAR      110*   113
    PICS11     0000 0064R       81*    85
    PICSTOP    0000 0090R       97*   100
    PURETOP    0000 0000R
    R0         0000 0000        29*    77     86     94    102
    R1         0000 0001        30*
    R10        0000 000A        37*    42     43     55     56     57     58     61     62     65     66
    R2         0000 0002        31*
    R3         0000 0003        34*
    R8         0000 0008        35*    43     54     56     66     69    106    114
    R9         0000 0009        36*    44     48     87    103
    RSAVE      0000 00DCR       54     69     77     86     94    102    106    114    130*
    STATUS     0000 000D        39*    46     47     50     51     84     99    112
    WAIT       0000 001CR       52*
    WRITE2     0000 00CCR       46*    52
    ZERO       0000 00D8R       97    110    128*
```



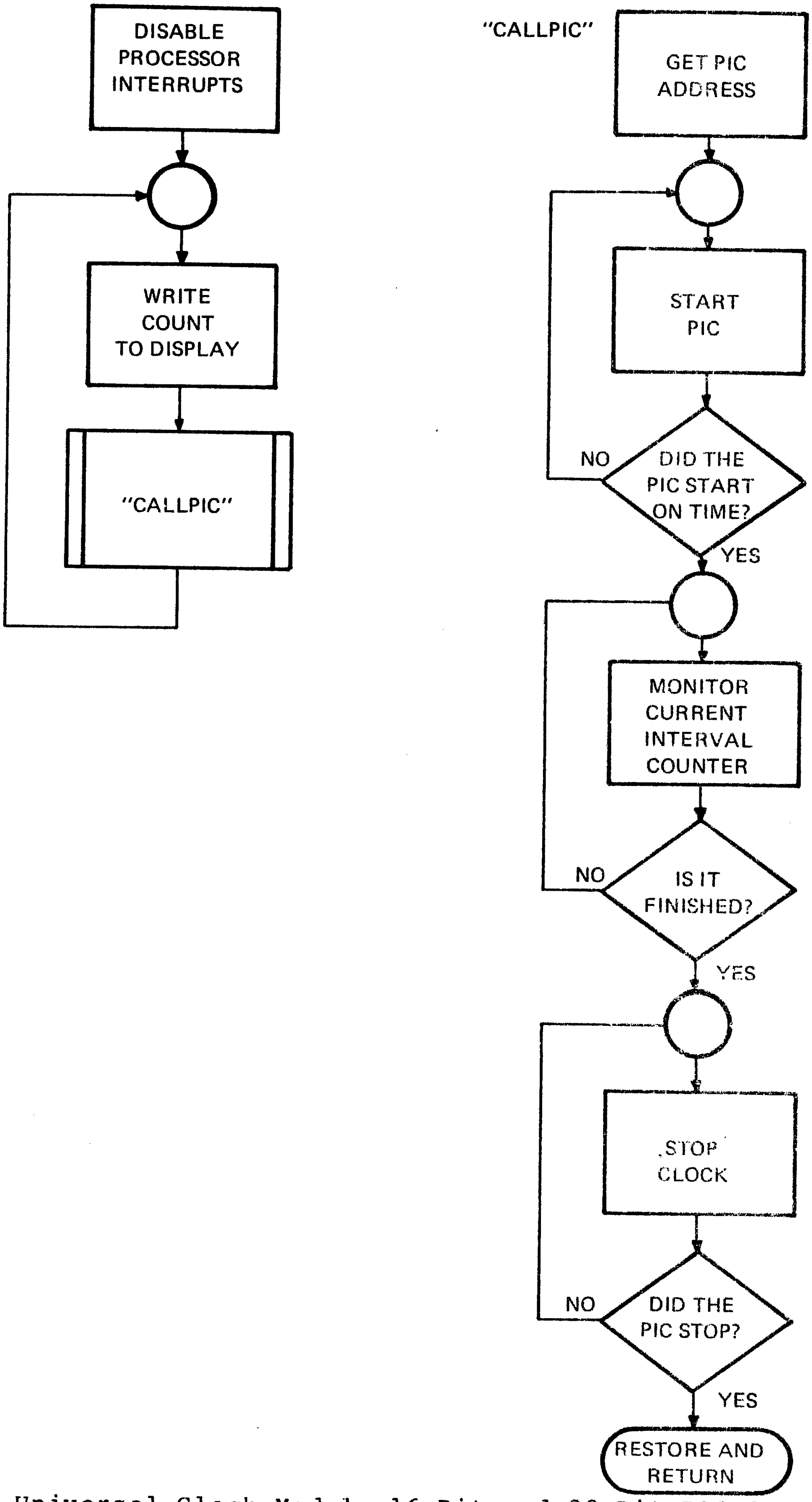
Universal Clock Module 32-Bit Interrupt Programming Example

```
UNIVERSAL CLOCK MODULE 16 BIT INTERRUPT PROGRAM EXAMPLE   PAGE   1  10:47:03  09/28/78
PROG= *NONE*     ASSEMBLED BY CAL 03-066R05-00   (32-BIT)
                                    1          CROSS                                                         CPE00010
                                    2          WIDTH 120                                                     CPE00020
                                    3          TARGT 16                                                      CPE00030
                                    4          PROG  UNIVERSAL CLOCK MODULE 16 BIT INTERRUPT PROGRAM EXAMPLE CPE00040
                                    5          NORX3                                                         CPE00050
                                    6  ******************************************************************   CPE00060
                                    7  *    THIS IS A 16-BIT PROGRAMMING EXAMPLE FOR THE LINE FREQUENCY  *   CPE00070
                                    8  *  CLOCK AND THE PRECISION INTERVAL CLOCK. THE EXAMPLE USES INTER- *   CPE00080
                                    9  *  RUPTS TO RECOGNIZE THE END OF THE INTERVALS.                    *   CPE00090
                                   10  *  THERE ARE FOUR MODULES:                                         *   CPE00100
                                   11  *            1)"CALLUCM"  THIS MODULE INITIALIZES THE INTERRUPT   *   CPE00110
                                   12  *              HANDLER AND STARTS THE LINE FREQUENCY CLOCK.       *   CPE00120
                                   13  *            2)"LFCINT"   THIS MODULE SERVICES THE INTERRUPT THAT *   CPE00130
                                   14  *              OCCURS AFTER THE LINE FREQUENCY CLOCK HAS WAITED   *   CPE00140
                                   15  *              ONE-HALF CYCLE OF THE AC LINE FREQUENCY.           *   CPE00150
                                   16  *              -8.33 MILLISECONDS @ 60 HZ OR 10 MILLISECONDS @50HZ*   CPE00160
                                   17  *              THEN IT STARTS THE PRECISION INTERVAL CLOCK.       *   CPE00170
                                   18  *            3)"PICINT"   THIS MODULE SERVICES THE PRECISION INT- *   CPE00180
                                   19  *              ERVAL CLOCK INTERRUPT THAT OCCURS AFTER A PROGRAM  *   CPE00190
                                   20  *              CONTROLLED INTERVAL OF 150 MICROSECONDS. IT THEN   *   CPE00200
                                   21  *              RESTARTS THE LINE FREQUENCY CLOCK. THIS MEANS THAT *   CPE00210
                                   22  *              THE PROGRAM WILL CONTINUE TO SERVICE "LFCINT" AND  *   CPE00220
                                   23  *              "PICINT" UNTIL THE FOURTH MODULE IS CALLED.        *   CPE00230
                                   24  *            4)"KILLUCM"  THIS MODULES DISARMS LFC & PIC INTER-   *   CPE00240
                                   25  *              RUPTS  AND STOPS THE PIC.                          *   CPE00250
                                   26  *                                                                 *   CPE00260
                                   27  ******************************************************************   CPE00270

            0000 0000              29  R0        EQU   0                                                 CPE00290
            0000 0001              30  R1        EQU   1                                                 CPE00300
            0000 0002              31  R2        EQU   2                                                 CPE00310
            0000 0002              32  INTDEV    EQU   2                  MICROCODE PUTS INTERRUPTING ADDRESS  CPE00320
                                   33  **                                 IN REGISTER 2 OF IN REGISTER SET 0   CPE00330
            0000 0003              34  R3        EQU   3                                                 CPE00340
            0000 0008              35  R8        EQU   8                                                 CPE00350
            0000 0009              36  R9        EQU   9                                                 CPE00360
            0000 000A              37  R10       EQU   10                                                CPE00370
            0000 000B              38  NEXTDEV   EQU   11                                                CPE00380
            0000 000D              39  STATUS    EQU   13                                                CPE00390
            0000 000F              40  LINK      EQU   15                                                CPE00400

    0000R   C8A0 3000              42  DISABLE   LHI   R10,X'3000'        GET DISABLE PSW MASK             CPE00420
    0004R   958A                   43            EPSR  R8,R10             NOW DISABLE INTERRUPTS           CPE00430
    0006R   2490                   44            LIS   R9,0               CLEAR R9(THE DISPLAYED COUNT REGISTR)  CPE00440
    0008R   41F0 0020R             45            BAL   LINK,CALLUCM                                        CPE00450
    000CR   2401                   46  WRITE2    LIS   STATUS,1           LOAD STATUS WITH DISPLAY ADDRESS CPE00460
    000ER   DED0 0004R             47            OC    STATUS,INCRMT      PUT DISPLAY IN INCREMENTAL MODE  CPE00470
    0012R   08F9                   48            LHR   LINK,R9            LOAD CONTENTS OF R9 INTO LINK AND  CPE00480
    0014R   94FF                   49            EXBR  LINK,LINK          WRITE VALUE ON DISPLAY PANEL     CPE00490
```

```
0000161  98DF                    50           WHR   STATUS,LINK                                                 CPE20500
0000181  34FF                    51           EXHR  LINK,LINK                                                   CPE20510
00001A1  94FF                    52           EXBR  LINK,LINK                                                   CPE20520
00001C1  98DF                    53           WHR   STATUS,LINK                                                 CPE20530
00001E1  DED0 8091 =000083I      54           OC    STATUS,NORM         PUT DISPLAY IN NORMAL MODE              CPE20540
0000221  4300 FFE6 =00000CI      55  WAIT     B     WRITE2              DISPLAY COUNT UNTIL CLOCK INTERRUPTS    CPE20550

0000261  D080 808E =000088I      57  CALLUCM  STM   R8,RSAVE            SAVE CURRENT USER'S REGISTERS           CPE20570
00002A1  C8A0 3000               58           LHI   R10,X'3000'         SET DISABLE INT PSW REGISTER            CPE20580
00002E1  958A                    59           EPSR  R8,R10              DISABLE INTERRUPTS AT PROCESSOR         CPE20590
0000301  C8A0 0054I              60           LHI   R10,LFCINT          GET ADDRESS OF LFC INTRPT HANDLER       CPE20600
0000341  40A0 01AA               61           STH   R10,X'D0'+X'DA'     STORE IT IN INTRPT SERVICE POINTER      CPE20610
                                 62  **************                NOTE DA=2*6D HEX'6D' IS THE PREFFERRED       CPE20620
                                 63  **************                     ADDRESS OF THE LINE FREQUENCY CLOCK     CPE20630
0000381  C8A0 00701              64           LHI   R10,PICINT          GET ADDRESS OF THE PIC INTRPT HANDLR    CPE20640
00003C1  40A0 01A8               65           STH   R10,X'D0'+X'D8'     STORE IT IN THE INTRPT SERVICE POINT    CPE20650
                                 66  **************                NOTE D8=2*6C HEX'6C' IS THE PREFFERRED       CPE20660
                                 67  **************                     ADDRESS OF THE PRECISION CLOCK          CPE20670
0000401  C8A0 7000               68           LHI   R10,X'7000'         SET INTRPT PSW IN REGISTER              CPE20680
0000441  958A                    69           EPSR  R8,R10              ENABLE INTERRUPTS AT PROCESSOR          CPE20690
0000461  48B0 8062 =0000ACI      70  LFCST1   LH    NEXTDEV,LFC         GET LFC ADDRESS                         CPE20700
00004A1  DEB0 8060 =0000AEI      71           OC    NEXTDEV,LFCSTCMD    START LFC                               CPE20710
00004E1  D180 8066 =000088I      72           LM    R8,RSAVE            RESTORE REGISTERS                       CPE20720
0000521  030F                    73           BR    LINK                RETURN TO CALLING PROGRAM & WAIT FOR    CPE20730
                                 74  **************                     INTERRUPT                               CPE20740

         0000 0054I              76  LFCINT   EQU   *                   LFCINTERRUPT HANDLER                    CPE20760
0000541  48B0 8052 =0000AAI      77           LH    NEXTDEV,PIC         GET PIC ADDRESS                         CPE20770
0000581  DE20 8053 =0000AFI      78           OC    INTDEV,DISARM       STOP & DISARM LFC                       CPE20780
00005C1  D8B0 8054 =000084I      79  PICST1   WH    NEXTDEV,INTRVL      SET RESOLUTION                          CPE20790
0000601  DEB0 804C =0000B01      80           OC    NEXTDEV,DISARMST    CLEAR PIC INTERRUPTS & START PIC        CPE20800
0000641  DEB0 8049 =0000B1I      81           OC    NEXTDEV,ENABLE      ENABLE PIC INTERRUPTS                   CPE20810
0000681  9DBD                    82           SSR   NEXTDEV,STATUS      DID THE PIC START ON TIME?              CPE20820
00006A1  2087                    83           BTCS  8,PICST1            NO, START IT AGAIN                      CPE20830
00006C1  2691                    84           AIS   R9,1                                                        CPE20840
00006E1  1800                    85           LPSWR R0                  AND RETURN                              CPE20850

         0000 00701              87  PICINT   EQU   *                   PIC INTERRUPT HANDLER                   CPE20870
0000701  48B0 8038 =0000ACI      88           LH    NEXTDEV,LFC         GET LFC ADDRESS                         CPE20880
0000741  D820 803E =000086I      89  PICSTOP  WH    INTDEV,ZERO         YES, CLEAR RIC.                         CPE20890
0000781  DE20 8034 =0000B0I      90           OC    INTDEV,DISARMST     AND STOP PIC                            CPE20900
00007C1  9D2D                    91           SSR   INTDEV,STATUS       DID THE PIC STOP?                       CPE20910
00007E1  2085                    92           BTBS  8,PICSTOP           NO,GO BACK AND STOP IT                  CPE20920
0000801  DEB0 802A =0000AEI      93  LFCST2   OC    NEXTDEV,LFCSTCMD    NOW START THE LFC                       CPE20930
0000841  2691                    94           AIS   R9,1                                                        CPE20940
0000861  1800                    95           LPSWR R0                  AND RETURN                              CPE20950
```

```
   UNIVERSAL CLOCK MODULE 16 BIT INTERRUPT PROGRAM EXAMPLE   PAGE   3  10:47:03  09/28/78
0098R   902D                99              SSR   INTDEV,STATUS         DID THE PIC STOP?                        CPE00990
009AR   2085               100              BTBS  8,PICSTOP             NO,GO BACK AND STOP IT                   CPE01000
009CR   DEB0  00D0R        101  LFCST2      OC    NEXTDEV,LFCSTCMD      NOW START THE LFC                        CPE01010
00A0R   D100  00DCR        102              LM    R0,RSAVE              RESTORE USER'S REGISTERS                 CPE01020
00A4R   2691               103              AIS   R9,1                  INCREMENT DISPLAY REGISTER               CPE01030
00A6R   C200  007ER        104              LPSW  OLDPSWB               AND RETURN                               CPE01040


00AAR   D080  00DCR        106  KILLUCM     STM   R8,RSAVE              SAVE REGISTERS                           CPE01060
00AER   4880  00CER        107              LH    NEXTDEV,LFC           GET LFC ADDRESS                          CPE01070
00B2R   4820  00CCR        108              LH    INTDEV,PIC            GET PIC ADDRESS                          CPE01080
00B6R   DEB0  00D1R        109              OC    NEXTDEV,DISARM        STOP LFC & CLEAR INTERRUPTS              CPE01090
00BAR   D820  00D8R        110  PICKILL     WH    INTDEV,ZERO           CLEAR PIC RESOLUTION COUNTER             CPE01100
00BER   DE20  00D2R        111              OC    INTDEV,DISARMST       STOP PIC & CLEAR INTERRUPTS              CPE01110
00C2R   902D               112              SSR   INTDEV,STATUS         DID THE PIC STOP?                        CPE01120
00C4R   2085               113              BTBS  8,PICKILL             NO STOP THE PIC                          CPE01130
00C6R   D180  00DCR        114              LM    R8,RSAVE              RESTORE REGISTERS AND                    CPE01140
00CAR   030F               115              BR    LINK                  RETURN TO CALLING PROGRAM                CPE01150


                           117  ***************  COMMANDS FOR THE PRECISION INTERVAL CLOCK                        CPE01170
                           118  ***************  AND THE LINE FREQUENCY CLOCK                                    CPE01180
00CCR   006C               119  PIC         DC    X'6C'                 STANDARD PIC ADDRESS                     CPE01190
00CER   006D               120  LFC         DC    X'6D'                 STANDARD LFC ADDRESS                     CPE01200
00D0R   40                 121  LFCSTCMD    DB    X'40'                 LFCSTART COMMAND ENABLES INTERRUPTS      CPE01210
00D1R   C0                 122  DISARM      DB    X'C0'                 LFC DISARMS COMMAND CLEAR INTERRUPTS     CPE01220
00D2R   E0                 123  DISARMST    DB    X'E0'                 PIC DISARM AND START COMMAND             CPE01230
00D3R   40                 124  ENABLE      DB    X'40'                 PIC ENABLE INTERRUPTS COMMAND            CPE01240
00D4R   40                 125  INCRMT      DB    X'40'                 DISPLAY COMMAND - INCREMENTAL MODE       CPE01250
00D5R   80                 126  NORM        DB    X'80'                 DISPLAY COMMAND - NORMAL MODE            CPE01260
00D6R   1096               127  INTRVL      DC    X'1096'               150 MICROSECONDS @ 1 MS RESOLUTION       CPE01270
00D8R   0000               128  ZERO        DC    X'0000'               ZEROES TO CLEAR RIC                      CPE01280
00DCR                      129              ALIGN 4                     ALIGN RSAVE AREA ON FULLWORD BOUNDARY    CPE01290
00DCR                      130  RSAVE       DS    16*ADC                REGISTER SAVE AREA FOR 16 USER REGIST    CPE01300
00FCR                      131              END                                                              CPE01310
```

```
   UNIVERSAL CLOCK MODULE 32 BIT INTERRUPT PROGRAM EXAMPLE   PAGE   4 10:48:05  09/28/78

ASSEMBLED BY CAL 03-066R05-00   (32-BIT)

START OPTIONS:  SCR,TA=32

   NO CAL ERRORS
   NO CAL WARNINGS
    2 PASSES

ABSTOP     0000 0000
ADC        0000 0004        121
CALLUCM    0000 0026I        45     57*
DISABLE    0000 0000I        42*
DISARM     0000 00AFI        78    100    113*
DISARMST   0000 00B0I        80     90    102    114*
ENABLE     0000 00B1I        81    115*
IMPTOP     0000 00F8I
INCRMT     0000 00B2I        47    116*
INTDEV     0000 0002         32*    78     89     90     91     99    101    102    103
INTRVL     0000 00B4I        79    118*
KILLUCM    0000 0088I        97*
LADC       0000 0002
LFC        0000 00ACI        70     88     98    111*
LFCINT     0000 0054I        60     76*
LFCST1     0000 0046I        70*
LFCST2     0000 0080I        93*
LFCSTCMD   0000 00AEI        71     93    112*
LINK       0000 000F         40*    45     48     49     49     50     51     51     52     52     53     73    106
NEXTDEV    0000 000B         38*    70     71     77     79     80     81     82     88     93     98    100
NORM       0000 00B3I        54    117*
PIC        0000 00AAI        77     99    110*
PICINT     0000 0070I        64     87*
PICKILL    0000 0098I       101*   104
PICST1     0000 005CI        79*    83
PICSTOP    0000 0074I        89*    92
PURETOP    0000 0000P
R0         0000 0000         29*    85     95
R1         0000 0001         30*
R10        0000 000A         37*    42     43     58     59     60     61     64     65     68     69
R2         0000 0002         31*
R3         0000 0003         34*
R8         0000 0008         35*    43     57     59     69     72     97    105
R9         0000 0009         36*    44     48     84     94
RSAVE      0000 00B8I        57     72     97    105    121*
STATUS     0000 000D         39*    46     47     50     53     54     82     91    103
WAIT       0000 0022I        55*
WRITE2     0000 000CI        46*    55
ZERO       0000 00B6I        89    101    119*
```



Universal Clock Module 16-Bit and 32-Bit PIC Status Programming Example

```
      PRECISION CLOCK 16 AND 32 BIT STATUS PROGRAM EXAMPLE      PAGE   1  10:46:22  09/28/78

PROG= *NONE*     ASSEMBLED BY CAL 03-066R05-00   (32-BIT)

                               1           CROSS                                                        PIC00010
                               2           WIDTH 120                                                    PIC00020
                               3           TARGT 16                                                     PIC00030
                               4           PROG  PRECISION CLOCK 16 AND 32 BIT STATUS PROGRAM EXAMPLE   PIC00040
                               5   *****************************************************************   PIC00050
                               6   *    THIS PROGRAM IS FOR THE PRECISION INTERVAL CLOCK. IT DOES NOT *   PIC00060
                               7   *USE INTERRUPTS. IT CAN BE RUN ON EITHER 16 BIT OR 32 BIT MACHINES.*   PIC00070
                               8   *IT IS CALLED AS A SUBROUTINE TO ACTIVATE THE PIC FOR A PROGRAM    *   PIC00080
                               9   *CONTROLLED INTERVAL OF 500 MILLISECONDS @ 1MILLISECOND RESOLUTION.*   PIC00090
                              10   *THE PROGRAM STAYS IN THIS ROUTINE BY CONTINUOUSLY INTERROGATING   *   PIC00100
                              11   *THE CURRENT INTERVAL COUNTER. AS SOON AS THE COUNTER RESETS TO THE*   PIC00110
                              12   *INITIAL INTERVAL VALUE THE PROGRAM RETURNS TO THE CALLING PROGRAM *   PIC00120
                              13   *ON THE REGISTER NAMED "LINK".                                     *   PIC00130
                              14   *****************************************************************   PIC00140
          0000 0000           15   R0       EQU   0                                                     PIC00150
          0000 0001           16   R1       EQU   1                                                     PIC00160
          0000 0009           17   R9       EQU   9                                                     PIC00170
          0000 000A           18   R10      EQU   10                                                    PIC00180
          0000 000B           19   PIC      EQU   11                                                    PIC00190
          0000 000C           20   OLD      EQU   12                                                    PIC00200
          0000 000D           21   NEW      EQU   13                                                    PIC00210
          0000 000E           22   STATUS   EQU   14                                                    PIC00220
          0000 000F           23   LINK     EQU   15                                                    PIC00230

 0000R    C810 030F           25   DISABLE  LHI   R1,X'030F'          GET DISABLE PSW MASK              PIC00250
 0004R    9114                26            SLHLS R1,4                SHIFT MASK                        PIC00260
 0006R    9501                27            EPSR  R0,R1               NOW DISABLE INTERRUPTS            PIC00270
 0008R    2490                28            LIS   R9,0                CLEAR R9(THE DISPLAYED COUNT REGISTR)  PIC00280
 000AR    24E1                29   WRITE2   LIS   STATUS,1            LOAD STATUS WITH DISPLAY ADDRESS  PIC00290
 000CR    DEE0 0065R          30            OC    STATUS,INCRMT       PUT DISPLAY IN INCREMENTAL MODE   PIC00300
 0010R    08F9                31            LHR   LINK,R9             LOAD CONTENTS OF R9 INTO LINK AND PIC00310
 0012R    94FF                32            EXBR  LINK,LINK           WRITE VALUE ON DISPLAY PANEL      PIC00320
 0014R    98EF                33            WHR   STATUS,LINK                                           PIC00330
 0016R    DEE0 0066R          34            OC    STATUS,NORM         PUT DISPLAY IN NORMAL MODE        PIC00340
 001AR    41F0 0024R          35   DOCOUNT  BAL   LINK,CALLPIC        START CLOCK SEQUENCE              PIC00350
 001ER    2691                36            AIS   R9,1                INCREMENT DISPLAY COUNT REGISTER  PIC00360
 0020R    4300 000AR          37            B     WRITE2              GOTO DISPLAY THE COUNT REGISTER   PIC00370

 0024R    D0A0 0068R          39   CALLPIC  STM   R10,RSAVE           SAVE REGISTERS                    PIC00390
 0028R    48B0 005ER          40            LH    PIC,PICADR          GET PIC ADDRESS                   PIC00400
 002CR    48C0 0060R          41            LH    OLD,INTRVL          GET RESOLUTION AND INTERVAL COUNT PIC00410
 0030R    C4C0 0FFF           42            NHI   OLD,X'0FFF'         MASK OFF RESOLUTION               PIC00420
 0034R    D0B0 0060R          43   PICSTART WH    PIC,INTRVL          SET PIC INTERVAL                  PIC00430
 0038R    DEB0 0064R          44            OC    PIC,DISARMST        DISARM PIC & START IT             PIC00440
 003CR    9DBE                45            SSR   PIC,STATUS          DID IT START ON TIME?             PIC00450
 003ER    4280 0034R          46            BTC   8,PICSTART          NO,START IT AGAIN                 PIC00460
 0042R    99BD                47   TIMEOUT  RHR   PIC,NEW             YES,NOW START MONITORING PIC COUNTER  PIC00470
 0044R    05CD                48            CLAR  OLD,NEW             IS IT FINISHED?                   PIC00480
 0046R    2163                49            BLS   DONE                YES,BECAUSE CIC = INTERVAL@500    PIC00490
```

```
   PRECISION CLOCK 16 AND 32 BIT STATUS PROGRAM EXAMPLE      PAGE   2  10:46:22  09/28/78
0048R  08CD                 50            LDAR  OLD,NEW           NO,SO OLD CIC=MOST RECENT CIC         PIC00500
004AR  2204                 51            BS    TIMEOUT           NOW RETURN AND CHECK THE CIC          PIC00510
004CR  40B0 0062R           52  DONE      WH    PIC,ZERO          WRITE ZEROES TO CLEAR RIC             PIC00520
0050R  DEB0 0064R           53            OC    PIC,DISARMST      STOP PIC                              PIC00530
0054R  9DBE                 54            SSR   PIC,STATUS        DID IT STOP?                          PIC00540
0056R  2085                 55            BTBS  8,DONE            NO STOP IT                            PIC00550
0058R  D1A0 0068R           56            LM    R10,RSAVE         YES FINISHED,RESTORE AND RETURN       PIC00560
005CR  030F                 57            BR    LINK              RETURN                                PIC00570


                            59  *********COMMAND & STORAGE AREA                                         PIC00590
005ER  006C                 60  PICADR    DC    X'6C'             PREFERRED PIC ADDRESS                 PIC00600
0060R  81F4                 61  INTRVL    DC    X'81F4'           500 MILLISECONDS @ 1 MSEC RESOLUTION  PIC00610
0062R  0000                 62  ZERO      DC    X'0000'           ZEROES TO CLEAR RIC                   PIC00620
0064R  E0                   63  DISARMST  DB    X'E0'             DISABLE INTRPTS & START COMMAND       PIC00630
0065R  40                   64  INCRMT    DB    X'40'             DISPLAY COMMAND - INCREMENTAL MODE    PIC00640
0066R  80                   65  NORM      DB    X'80'             DISPLAY COMMAND - NORMAL MODE         PIC00650
0068R                       66            ALIGN 4                 ALIGN RSAVE AREA ON FULLWORD BOUNDARY PIC00660
0068R                       67  RSAVE     DS    ADC*6                                                   PIC00670
0074R                       68            END                                                           PIC00680
```

```
    PRECISION CLOCK 16 AND 32 BIT STATUS PROGRAM EXAMPLE      PAGE   3  10:46:22  09/28/78

ASSEMBLED BY CAL 03-066R05-00   (32-BIT)

START OPTIONS:  SCR,TA=16

   NO CAL ERRORS
   NO CAL WARNINGS
    2 PASSES

ABSTOP     0000 0000
ADC        0000 0002        67
CALLPIC    0000 0024R       35     39*
DISABLE    0000 000OR       25*
DISARMST   0000 0064R       44     53     63*
DUCOUNT    0000 001AR       35*
DONE       0000 004CR       49     52*    55
IMPTOP     0000 0074R
INCRMT     0000 0065R       50     64*
INTRVL     0000 0060R       41     43     61*
LADC       0000 0001
LINK       0000 000F        23*    31     32     32     33     35     57
NEW        0000 000D        21*    47     48     50
NORM       0000 0066R       34     65*
OLD        0000 000C        20*    41     42     48     50
PIC        0000 000B        19*    40     43     44     45     47     52     53     54
PICADR     0000 005ER       40     60*
PICSTART   0000 0034R       43*    46
PURETOP    0000 0000R
R0         0000 0000        15*    27
R1         0000 0001        16*    25     26     27
R10        0000 000A        18*    39     56
R9         0000 0009        17*    28     31     36
RSAVE      0000 0068R       39     56     67*
STATUS     0000 000E        22*    29     30     33     34     45     54
TIMEOUT    0000 0042R       47*    51
WRITE2     0000 000AR       29*    37
ZERO       0000 0062R       52     62*
```

PUBLICATION COMMENT FORM

Please use this postage-paid form to make any comments, suggestions, criticisms, etc. concerning this publication.

From ______________________ Date ______________________

Title ______________________ Publication Title ______________________

Company______________________ Publication Number ______________________

Address ______________________

____

____

FOLD FOLD

Check the appropriate item.

□ Error Page No. ________ Drawing No. ______________

□ Addition Page No. ________ Drawing No. ______________

□ Other Page No.________ Drawing No. ______________

Explanation:

FOLD FOLI

Fold and Staple
No postage necessary if mailed in U.S.A.

CUT ALONG LINE

STAPLE

STAPLE

FOLD

FOLD

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 22 OCEANPORT, N.J.

POSTAGE WILL BE PAID BY ADDRESSEE

PERKIN-ELMER
Computer Systems Division
2 Crescent Place
Oceanport, NJ 07757

TECH PUBLICATIONS DEPT. MS 322A

FOLD

FOLD

STAPLE

STAPLE