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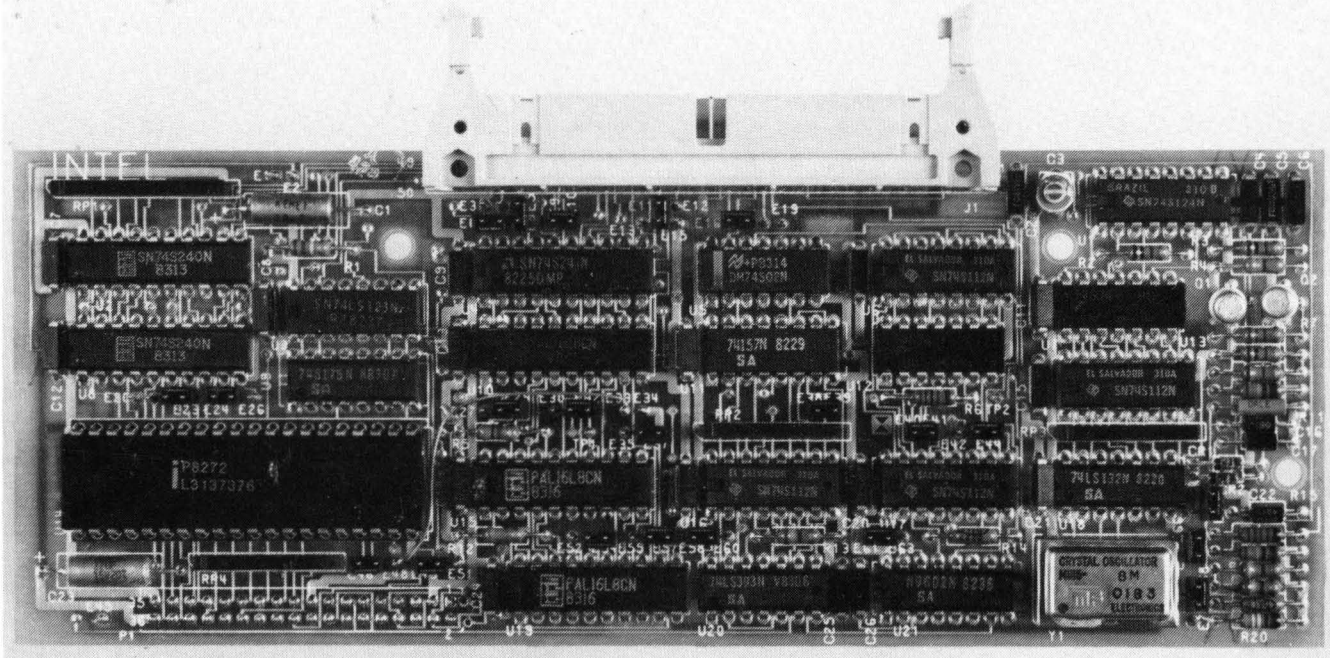
iSBX™ 218A FLEXIBLE DISKETTE CONTROLLER BOARD HARDWARE REFERENCE MANUAL



Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Order Number: 145911-001

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PREFACE

This manual provides the information you will need to configure and install the iSBX 218A board onto a host board which is equipped with an iSBX Bus connector. This manual is not intended to be a tutorial publication on the subject of disk drive interfacing techniques.

The iSBX 218A board can be used as a direct replacement for the iSBX 218 board; however, reconfiguration from the factory default mode is required for this application. The iSBX 218A board is compatible with most 8-inch floppy disk drives and most 5.25-inch floppy disk drives currently on the market.

Additional related information can be found in the following publications (available from the Intel Literature Department -- see page ii for address):

- Intel 8272 Data Sheet.
- Intel MULTIBUS® Handbook (includes iSBX™ Bus), Order Number 210883.
- iSBC® 215G Winchester Disk Controller Hardware Reference Manual, Order Number 144780.
- iSBC® 86/30 Single Board Computer Hardware Reference Manual, Order Number 144044.

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CHAPTER 1. GENERAL INFORMATION

1.1 INTRODUCTION

Intel's iSBX 218A Flexible Diskette Controller Multimodule Board is an expansion Multimodule board designed to augment Intel's iSBC microcomputer product family, and other host boards equipped with an iSBX Bus connector.

The iSBX 218A board provides for integration of flexible diskette storage by interfacing with up to four 8-inch or 5.25-inch, single/double-sided, single/double-density flexible diskette drives. This chapter contains a description of the iSBX 218A board and lists the equipment supplied, and specifications.

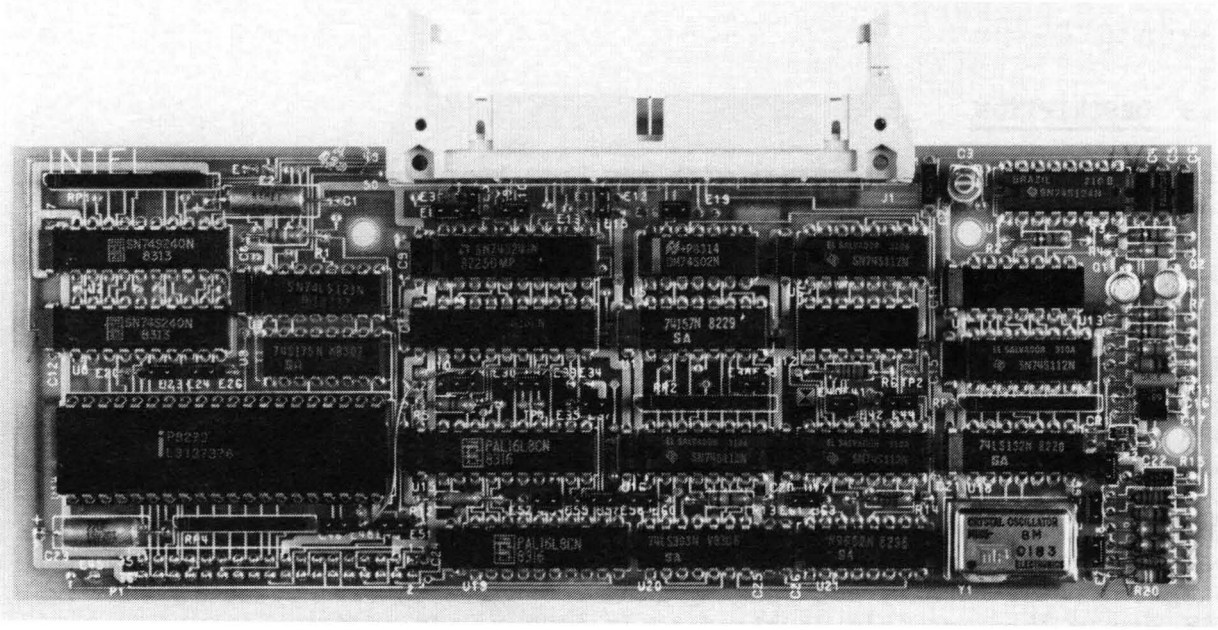


Figure 1-1. iSBX™ 218A Flexible Diskette Controller Board

1.2 BOARD FEATURES

The iSBX 218A board provides the following major features:

- Handles up to four single/double sided drives, without the use of a scrambler cable.
- Drives used may be a mixture of single or double-density types.
- Recording format is IBM-compatible, soft-sectored, in both single and double-density.
- Performs READ, WRITE, FORMAT, RE-CALIBRATE, SEEK, SENSE, & SPECIFY commands with minimal processor overhead.
- Can be operated in DMA mode or non-DMA mode, including DMA with processors which use only DMA Request (DRQ) but not DMA Acknowledge (DACK), such as the 8089 or the 80186.
- Provides programmable motor on/off control, programmable reset, and programmable terminal count (TC) capability.
- Configurable to be fully upward compatible with the iSBX 218 board.

1.3 DESCRIPTION

The iSBX 218A board interfaces with any host board equipped with an iSBX Bus connector. The only restriction is that the host board be able to support the data transfer rate of the drive attached to the iSBX 218A board. The board operates in the polled I/O mode or in direct memory access (DMA) mode.

Up to four drives of the same size (8-inch or 5.25-inch) can be controlled by the iSBX 218A board. The board interfaces to both single and double-sided drives of the same size, and allows both single-density and double-density recording formats to be used concurrently.

The iSBX 218A board supports a soft-sector format with sector sizes ranging from 128 bytes to 4096 bytes in the IBM 3740-compatible single-density format; and ranging from 256 bytes to 8192 bytes in the IBM System 34-compatible double-density format. In addition to programmable sector sizes and recording density, the head load time, head unload time and track-to-track access time (step rate) operating characteristics must be specified by the program.

A number of jumper-selectable options are provided on the iSBX 218A board to support various drive interface pin assignments and functions.

1.4 EQUIPMENT SUPPLIED

The following equipment is supplied with the iSBX 218A board:

a. Schematic Diagram
b. 6 Screws, 1/4" 6-32 nylon
c. 3 Spacers, 1/2" 6-32 nylon

1.5 SPECIFICATIONS

Specifications for the iSBX 218A Flexible Diskette Controller Multimodule Board are provided in Table 1-1.

Table 1-1. iSBX™ 218A Board Specifications

POWER REQUIREMENT	+5VDC ± 0.25V @ 1.7A max.
ENVIRONMENTAL REQUIREMENTS	
Operation Temperature	0°C to 55°C (32°F to 131°F)
Operation Humidity	To 90% without condensation
PHYSICAL CHARACTERISTICS	
Width	8.0 cm (3.15 in)
Length	19.1 cm (7.50 in)
Height	2.1 cm (0.83 in)
Height with host	2.9 cm (1.13 in)
Weight	126.0 gm (4.50 oz)

1.6 iSBX™ BUS COMPLIANCE LEVEL

All Intel iSBX Bus-compatible boards are designed around guidelines set forth in the "Intel iSBX Bus Specification." The specification requires that certain board operating characteristics, such as data bus width and employment of interlocked operation, be clearly stated in the board's printed specifications (i.e., reference manual). Used properly, this information quickly summarizes the level of compliance the board bears to the published iSBX Bus Specification. The compliance level clearly states the board's level of compatibility to the iSBX Bus structure. Refer to the INTEL iSBX BUS SPECIFICATION for additional information.

The following notation states the iSBX 218A board's level of compliance to the iSBX Bus Specification:

Drive	iSBX™ DMA Transfer	iSBX™ Non-DMA Transfer
5.25-inch	D8 DMA I	D8
8-inch	D8 DMA	D8

This notation is decoded as follows:

D8 = interfaces to 8-bit or 16/8-bit host board.

DMA = supports DMA operations.

I = requires interlocked operation.

In addition to the iSBX DMA mode transfers described in the preceding chart, several other DMA modes are available on the iSBX 218A board. Refer to Section 2.8.5 for details.

***

CHAPTER 2. INTERFACING AND CONFIGURATION

2.1 INTRODUCTION

Much of the iSBX 218A board's flexibility is obtained through the use of jumper-configurable options. This chapter explains the jumper options on the iSBX 218A board, and describes how to configure the jumpers for your application. Read Section 2.2 to get an idea of how to choose a drive which is compatible with the iSBX 218A board. In some cases you may need to modify the drive you choose for proper operation with the iSBX 218A board. Some of the areas to consider for possible drive modification are given in this chapter. Electrical interfacing requirements are also provided here. You should read this entire chapter before configuring the jumpers on your board.

2.2 CHOOSING A DRIVE AND DRIVE MODIFICATIONS

The iSBX 218A board is configured at the factory to operate with the Shugart Corporation Model 450 5.25-inch disk drive. Any equivalent 5.25-inch drive can also be used without modification. Factors to consider when choosing a drive which is not equivalent to the Shugart 450 include ready logic, motor-on control, and stepper motor power restrictions. This section also discusses some of the possible drive modifications to other drives which may be necessary to ensure a proper interface with the iSBX 218A board. Refer to your drive's reference manual for additional information.

2.2.1 READY LOGIC

Most standard-sized drives compatible with the iSBX 218A board provide a "ready" indication to the board only when the drive is selected. If the drive provides an ungated READY/ output (generally referred to as "Radial Ready"), the drive must be modified to condition the drive's READY/ output with DRIVE SELECT/. Most 5.25-inch drives do not provide a ready indication. Accordingly, when interfacing drives that do not provide a READY/ output, you must ensure that the iSBX 218A board's READY/ input is permanently enabled, or is connected to the INDEX timeout circuit (see Section 2.8.4.1).

2.2.2 DRIVE TERMINATION

When two or more drives are interfaced (daisy-chained) to the iSBX 218A board, the termination resistors/networks on the following common drive input signal lines must be removed from all but the last physical drive on the cable. Typically, these include (but are not limited to) the following input signals:

DRIVE SELECTS
DIRECTION SELECT
STEP
WRITE DATA
WRITE GATE
HEAD LOAD (if used)
LOW CURRENT (if used)
FAULT RESET (if used)
MOTOR ON (if used)
SIDE SELECT (if used)

Refer to your drive's reference manual for complete information on input signal termination.

2.2.3 DRIVE NUMBERING

Each drive must be assigned a unique drive number. Depending on the drive, this can be accomplished with wire jumpers, shorting plugs, or switch settings. Generally, drives are shipped for single drive systems (drive 0 or drive 1). If using multiple drives, refer to the drive manual to reconfigure the second, third, and fourth drives for drive addresses 1, 2, and 3 (or 2, 3, and 4).

2.2.4 MOTOR ON/ CONTROL

The spindle motor of 5.25-inch drives must be turned on long enough before READ or WRITE is made to allow the drive to reach operating speed. This can be accomplished in several ways, depending on how your particular drive controls the motor.

If the motor is controlled only by the MOTOR ON line, there are two possibilities. First, the motor can be controlled by one of the programmable latches. With this method, the motors of all connected drives are controlled together. This allows efficient copying from one disk to another. Using the Programmable Latch allows leaving the motor on during periods of frequent use rather than making each READ or WRITE wait the required motor start-up time. Typically, a software timer is used to keep the motor on for some time (e.g. 2 seconds) after each access. If another access is required within the time period, the access is made without a motor start-up delay, and the timer is reset. This method results in the best overall system performance.

The second method of using a disk drive (on which the motor is controlled only by MOTOR ON) is to drive MOTOR ON with HEAD LOAD from the 8272 controller.

Again, the motors on all connected drives will be controlled together. The HEAD LOAD TIME must be programmed to be longer than the motor start-up time. This requires every access to wait the entire motor start-up time, even if the motor was just used and hasn't yet come to a complete stop. This results in lower overall system performance than the method described above, but does not require special software.

Some drives have an option allowing the motor to be controlled by the AND (simultaneous occurrence) of MOTOR ON and DRIVE SELECT. Note than in this case, only the selected drive will have its motor activated, even if other drives are connected. MOTOR ON could either be driven by HEAD LOAD from the 8272 or simply be enabled all the time (grounded).

In either case however, the head load time would have to be programmed to be longer than the motor start-up time to assure that DRIVE SELECT occurs soon enough before the READ or WRITE occurs.

Some drives have an option allowing the motor to be controlled only by DRIVE SELECT. Just as in the case described immediately above, only the selected drive will have its motor activated. Again, even though HEAD LOAD is not used, the head load time must be programmed to be longer than the motor start-up time to assure that DRIVE SELECT occurs long enough before the READ or WRITE occurs.

2.2.5 STEPPER MOTOR POWER

Some drives use the DRIVE SELECT line to control a power down mode of the stepper motor. This type of drive cannot be used with the iSBX 218A board because the stepper motor will be powered down when it should be stepping. This is because of the way the iSBX 218A board examines the DRIVE READY status. The iSBX 218A board polls all four possible drives for a change in DRIVE READY status by cycling through the DRIVE SELECT lines. This polling continues between consecutive STEP pulses to a drive that is seeking. The DRIVE SELECT for the seeking drive is active during the step pulse itself, but not continuously between step pulses. Verify that your drive does not have this power-down mode, or if it does, ensure that the drive has an option to disable the power-down mode.

2.3 DRIVE INTERFACE CONNECTOR SIGNAL FUNCTIONS

The following list provides brief definitions of the signal functions on the drive interface connector (J1). Refer to Chapter 3 for drive cabling information.

WRITE CURRENT SWITCH/	An active-low output signal used to select low write current compensation circuitry available on some drives. This signal is enabled during read/write operations and is active when the track address is 43 or greater.
HEAD LOAD/	An active-low output signal used to load the read/write head. When the head is initially loaded, the iSBX 218A board provides a programmed delay (head load time) prior to initiating any read/write operation. Following a read/write operation, the controller delays deactivating the HEAD LOAD/ signal until after the programmed head unload time.

TWO SIDED/	An active-low status input signal that indicates the presence of a double-sided diskette. This signal is examined only during the Sense Drive Status command.
SIDE SELECT/	An active-low output control signal that selects one side of a double-sided drive. When SIDE SELECT is high, read/write operations are performed on side 0 of the drive.
INDEX/	An active-low input pulse that is coincident with the detection of the index hole in the diskette, indicating the logical beginning of a track.
READY/	An active-low input signal indicating that the drive is ready to perform an operation. The qualifications for READY/ are drive-dependent and usually include diskette in place, door closed and diskette RPM at specified speed. The iSBX 218A board uses a common READY/ input and requires that the drive provide a gated READY/ output when individually selected.
DRIVE SELECT 0/ - DRIVE SELECT 3/	Individual active-low output signals for selecting the individual drives interfaced.
DIRECTION SELECT/	An output control signal that specifies the direction in which the drive's head is stepped. This signal is only enabled during seek operations and when at a logic low level, sets the direction toward the spindle (step in).
STEP/	An active-low output pulse that causes the drive to move (step) the read/write head one track position. The direction of the step is determined by the state of the direction output signal. Like the DIRECTION/ signal, STEP/ is only enabled during seek operations.
WRITE DATA/	The serial data/clock composite write signal to the drive. The high-to-low going transition of the signal indicates a clock or data "1" bit to be written on the diskette.
WRITE GATE/	An active-low control signal that enables the drive's write circuitry, allowing data to be written on the diskette. When this signal is in its inactive state (high) the write circuitry is disabled and the drive reads data from the diskette.
TRACK 00/	An active-low input status signal that indicates the drive head is currently positioned over track 00 of the diskette. Note that this signal is examined only during a seek or recalibrate operation.

WRITE PROTECT/	An active-low input status signal that indicates the presence of a write-protected diskette. Note that this signal is only examined during a write or format operation.
READ DATA/	The composite (unseparated) data and clock input signal generated by the drive during a diskette read operation. A high-to-low going transition indicates a clock or data "1" bit.
FAULT/	An active low input status signal that indicates a write fault condition within the drive. This signal is examined only during read/write operations.
FAULT RESET/	An active-low output signal used to reset fault detection logic which may be optional in some drives. This signal is automatically generated at the beginning of every read/write operation.
MOTOR ON/	An active-low output signal which turns the drive spindle motor on and off (for DC motors only). Note that MOTOR ON/ is common to all four drives.
IN USE/	An active-low output signal used by the drive to control the "in use" or "busy" indicator on each drive. Typically, IN USE/ must be qualified by another signal (such as DRIVE SELECT/). The qualification signal is drive dependent.

2.4 DISK DRIVE INTERFACE TIMING CHARACTERISTICS

Figure 2-1 and Table 2-1 provide timing parameters for drive seek timing, head load timing, and write data timing.

Table 2-1. Drive Interface Timing Characteristics

Symbol	Parameter	Standard 8-inch Drive			5¼-inch Mini Drive			Units
		Minimum	Typical	Maximum	Minimum	Typical	Maximum	
Seek Timing								
t_{DSD}	DRIVE SELECT/ to DIRECTION/ Setup Time	19			38			µs
t_{SDS}	DRIVE SELECT/ Hold Time from STEP/	5			10			µs
t_{DS}	DIRECTION/ to STEP/ Setup Time	1			2			µs
t_{SD}	DIRECTION/ Hold Time from STEP/	24			48			µs
t_{SCY}	STEP/ Cycle Time	1		16	2		32	ms
t_{SPW}	STEP/ Pulse Width	5			10			µs
Head Load Timing								
t_{HLD}	Head Load Time	2		254	4		508	ms
t_{HUL}	Head Unload Time	16		240	32		480	ms
Write Data Timing								
t_{HBC}	Half Bit Cell		1 or 2*			2 or 4*		µs
t_{FBC}	Full Bit Cell		2 or 4*			4 or 8*		µs
t_{DPW}	Data Pulse Width	200	250		200	250		ns

*FM Mode Values.

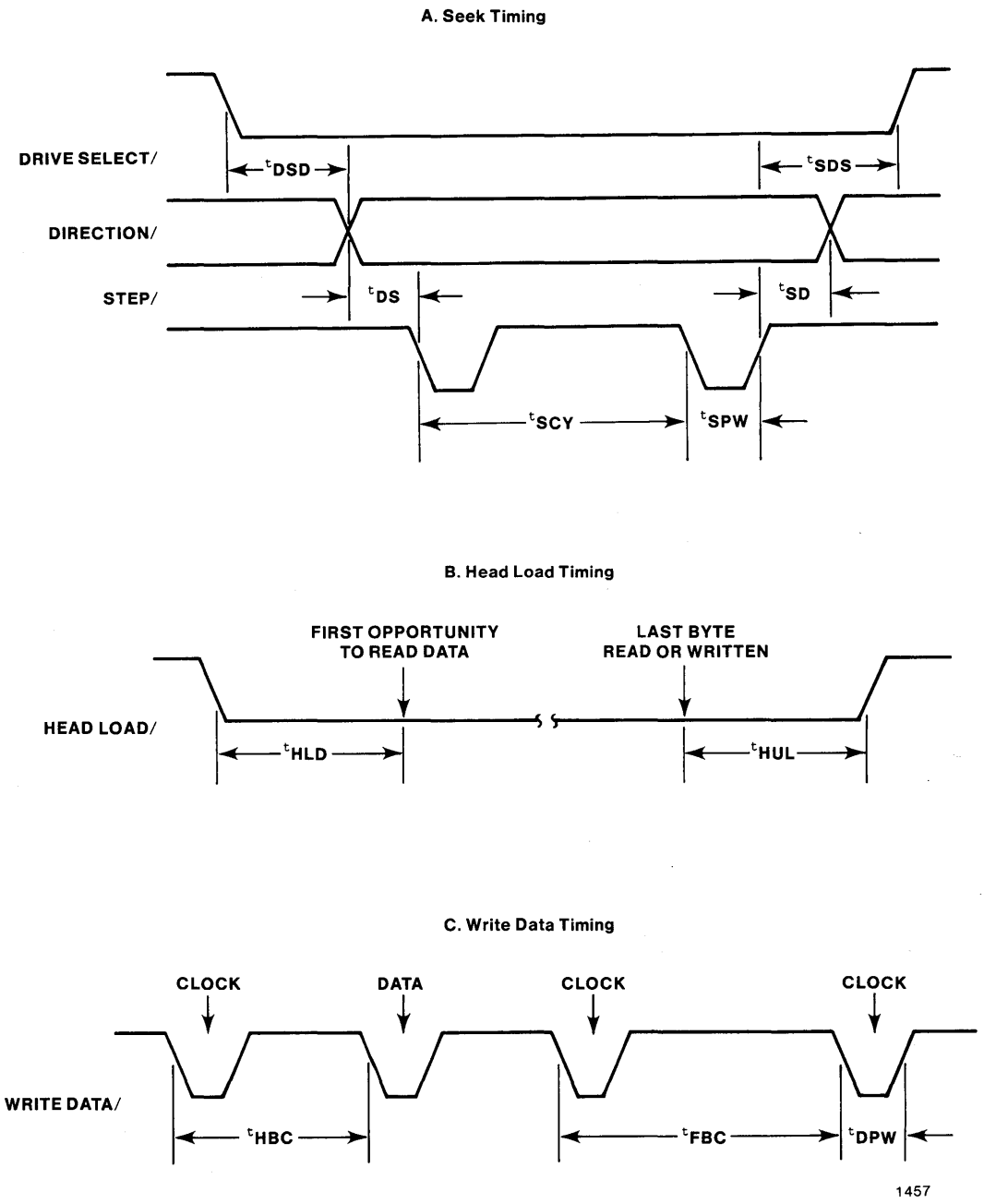


Figure 2-1. Drive Interface Timing Characteristics

2.5 DISK DRIVE INTERFACE DC LOADING CHARACTERISTICS

The current drive characteristics for all iSBX 218A board output signals are as follows:

$$I_{OL} = 64 \text{ milliamps}$$

$$I_{OH} = -15 \text{ milliamps}$$

All board inputs are terminated with a 220 ohm pull-up/330 ohm pull-down device. Refer to Chapter 3 for drive cabling information.

2.6 JUMPER CONNECTIONS OVERVIEW

Before configuring your iSBX 218A board jumpers, you need to know certain characteristics about the disk drive you will connect to the board, and the host board onto which your board will reside. Most of the information you need about the disk drive should be located in the disk drive reference manual or data sheet. You should refer to the host board hardware reference manual for information about your host board. If your host board is an iSBC 215G board (PBA number 144263-009 or higher), Section 2.8.9 outlines the required configuration information.

Figure 2-2 provides a simplified flowchart of the steps to follow when configuring your board. The flowchart summarizes the configuration questions you must answer before installing or removing jumpers. The flowchart also serves as a suggested procedure for going through the configuration process in an orderly manner.

Sections 2.8.1 through 2.8.8 of this chapter explain the purpose of each jumper choice. In some cases you must select more than one jumper connection to establish one mode of operation. Most of the jumper connections are made using push-on type jumpers. A few require wire wrap jumpers.

NOTE

The iSBX 218A board is configured at the factory to operate without modification on an iSBC 215G host board (PBA number 144263-009 or higher), and for using Shugart Corporation Model 450 5.25-inch drives (or compatible drive). However, the iSBC 215G board requires several jumper modifications. See Section 2.8.9 for details.

If you are using the iSBX 218A board in an iSBX 218 application, and must use software which was written specifically for the iSBX 218 board then you must reconfigure the iSBX 218A board. Refer to Section 2.8.10.

2.7 FACTORY DEFAULT JUMPER CONFIGURATION

The iSBX 218A board has been configured at the factory for installation into a specific system (Intel System 310, with iSBC 215G board). This configuration may not be suitable for your application. Figure 5-1 provides a numerical list of the iSBX 218A board default jumpers. In addition, the factory default jumpers are marked with a "§" symbol in the jumper tables throughout this chapter. This means that the jumpers marked are the only ones installed at the factory. The installed jumpers correspond to the jumpers shown installed on the schematic diagram in Chapter 5. Jumper connections marked with a "W" are wire-wrap connections rather than push-on jumpers. The "W" does not indicate default jumpering.

CAUTION

Do not solder jumpers in place on the iSBX 218A board. Use push-on jumpers where possible; use wire wrap jumpers elsewhere. When installing or removing push-on jumpers, use a tool designed specifically for that purpose -- do not use pliers. Pliers may cause damage to the push-on jumper.

2.8 JUMPER CONFIGURATIONS

The following sections describe the jumper options you must choose to properly configure your iSBX 218A board. The flowchart in Figure 2-2 provides a recommended procedure to follow when configuring your board. Although most of these jumpers can actually be configured in any sequence, this flowchart helps eliminate any repeated steps by showing you at a glance what needs to be considered.

2.8.1 DRIVE SIZE

With this set of jumpers you select either 8-inch drives or 5.25-inch drives. The board must be configured for one size only. The factory default configuration is for 5.25-inch drives. Table 2-2 lists the drive size jumpers.

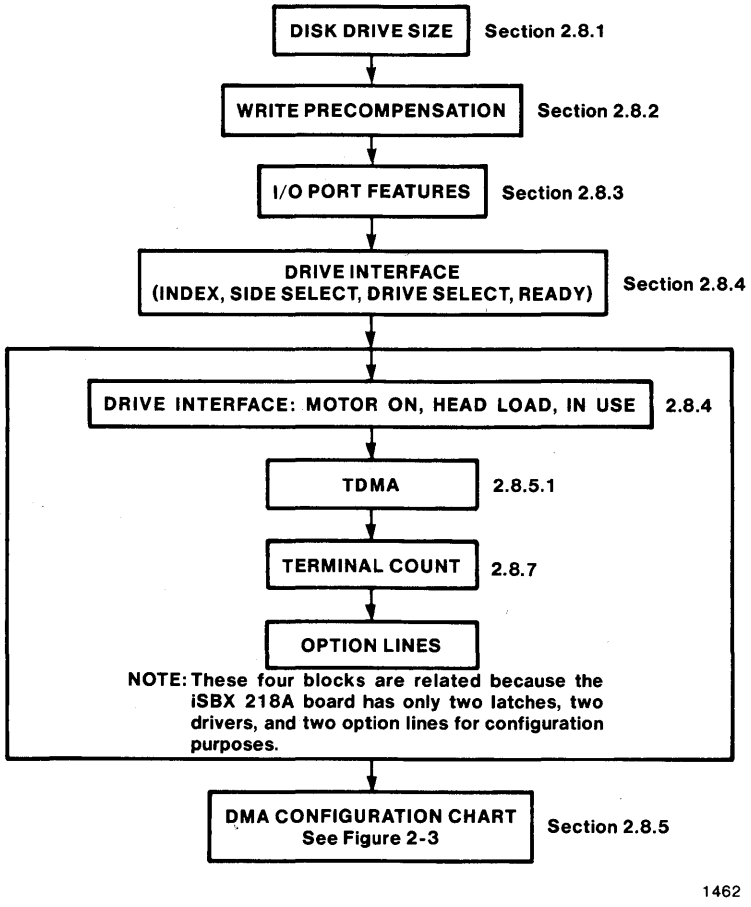


Figure 2-2. Jumper Configuration Flowchart

Table 2-2. Drive Size Jumper Configurations

Feature Selected	Jumper(s) Installed
Drive Size: 5.25-Inch	43 - 44 § 56 - 57 § 58 - 59 § 61 - 62 § 64 - 65 § 68 - 69 §
Drive Size: 8-Inch	42 - 43 55 - 56 59 - 60 62 - 63 69 - 70
Notes: § = factory default configuration. Jumper 64 - 65 must be removed for 8-inch operation.	

2.8.2 WRITE PRECOMPENSATION OPTIONS

Write precompensation is an action which the iSBX 218A board performs to compensate for the "bit shift" phenomenon which occurs in rotating memory devices such as disk drives. In simple terms, write precompensation helps ensure that the recorded data on the diskette will subsequently be read correctly. Write precompensation is a requirement for most disk drives. There are two options which are concerned with write precompensation: the amount of precompensation and the number of disk tracks on which to use precompensation.

The amount of write precompensation is either 250 nanoseconds or 125 nanoseconds. The factory default is 125 nanoseconds. This is generally the choice for most 5.25-inch drives. For 8-inch drives, 250 nanoseconds is typically selected. Refer to your drive manual if necessary. Table 2-3 lists the write precompensation jumpers.

The second option is selecting which group of tracks should receive precompensation. The choices are all tracks or inner tracks (tracks 43 and greater) only. However, for disks with only 40 tracks there is no selection required. The factory default is write precompensation on all tracks. This is generally the choice for most 5.25-inch drives. Most 8-inch drives use inner-track-only precompensation.

If, for some reason, you do not want to use write precompensation you can install a wire-wrap jumper at post 28 - 35.

Table 2-3. Write Precompensation Jumper Configurations

Feature Selected	Jumper(s) Installed
125 ns write precompensation	24 - 25 § 31 - 32 §
250 ns write precompensation	25 - 26 30 - 31
Write precompensation on all tracks	28 - 29 §
Write precompensation on inner tracks only (tracks 43 and greater)	27 - 28
No write precompensation	28 - 35 (W)

Notes: § = factory default configuration; W = wire wrap jumper.

2.8.3 I/O PORT FEATURES ENABLE OPTION

The I/O port features make the iSBX 218A board compatible with a wide variety of disk drives. These features include two programmable latches, a programmable RESET command, and a programmable DMA Acknowledge (DACK) command. All these features are jumper selectable; descriptions are located in subsequent sections of this chapter.

Although the iSBX 218A board boasts many enhancements over the iSBX 218 board, it can be used as a direct replacement for the latter. When using the "A" version for a direct replacement, you should remove jumper 49 - 50 and install jumper 50 - 51. When installed, this jumper disables the I/O port features available on the iSBX 218A board (which were not available on the iSBX 218 board). The default configuration is to have the I/O port features enabled (jumper 49 - 50 installed and 50 - 51 removed).

For a complete list of iSBX 218 board emulation jumpers, refer to Section 2.8.10. The following table outlines the I/O port feature jumper options:

Table 2-4. I/O Port Features Enable/Disable Jumpers

Feature Selected	Jumper(s) Installed
I/O Port Features Enabled	49 - 50 §
I/O Port Features Disabled (iSBX 218 Emulation)	50 - 51
Notes: § = factory default configuration; W = wire wrap jumper.	

2.8.4 DRIVE INTERFACE OPTIONS

This group of jumpers is used to configure the interface between the iSBX 218A board and the particular type of drive in use. Since drive manufacturers do not route their data and control signals over a standardized pin-out, it is necessary to provide some flexibility to the drive interface configuration. The major differences are found between 8-inch drives and 5.25-inch drives. You should consult your disk drive manual to verify the actual signals used by your drive and to verify the pin assignments on its connector. Table A-2 lists the J1 pin assignments for the iSBX 218A board. Notice that the the 8-inch drives use the 50-pin connector, while the 5.25-inch drives use only 34 of the pins. Each of the 34 pins has two numbers, depending on whether it is used for a 50-pin connection or a 34-pin connection. Throughout this manual each pin is referred to as though it were part of a 50-pin connection.

2.8.4.1 READY/ Signal Options

The iSBX 218A board requires a READY/ signal for proper operation. The READY/ signal ideally should originate in the disk drive, but can be generated on-board if necessary. The READY/ signal indicates that the drive is ready to perform a valid function. More specifically, for most 8-inch drives, READY/ means that drive power is on, a diskette is in the drive, and the drive door is closed. For other drives, the READY/ signal is generated several different ways. Consult your drive manual for more information on how READY/ is generated.

Drives which provide a READY/ signal allow the 8272 (disk controller device on the iSBX 218A board) to monitor which drives are ready for use. When used with drives which do not provide the READY/ signal, the iSBX 218A must assume that all drives are in fact ready for use. This is done by making the READY/ input to the 8272 always true. However, if you access a drive without a disk in it, the iSBX 218A board will wait indefinitely for a response. This is because the READY/ line indicates that the drive is ready, and no index pulses have occurred. Essentially the board is waiting for the non-existent disk to make one revolution, before giving up and returning an error condition.

The iSBX 218A board has a special "index timeout" circuit which eliminates this potential indefinite wait. If, during an access, no index pulses are read for about 1 second, the circuit will time-out, causing READY/ to become false. This in turn causes an interrupt and a "drive not ready" status code. During periods when no access is made, the index time-out circuit constantly indicates that READY/ is true.

This means you cannot use READY/ produced by the index time-out circuit to determine if a drive is ready or not ready. It is only useful to recover from the potentially indefinite wait situation.

As far as the iSBX 218A board is concerned, there are four ways of dealing with the READY/ signal. The board can be configured to generate its own READY/ signal at all times; or it can be configured to accept READY/ from one of two available J1 pins; or READY/ can be generated on-board as a result of an INDEX timeout. Table 2-5 summarizes the READY/ options and their corresponding jumper configurations.

Table 2-5. READY/ Signal Sources

Feature Selected	Jumper(s) Installed
READY/ from INDEX TIMEOUT (for drives without READY/ lines)	6 - 7 §
READY/ always true (for drives without READY/ lines)	3 - 7 (W)
READY/ input from J1-22 (for all 8-inch drives)	1 - 2 7 - 8
READY/ input from J1-50 (for most 5.25-inch drives with READY/ lines)	1 - 2 4 - 7

Notes: § = factory default configuration; W = wire wrap jumper.

2.8.4.2 DRIVE SELECT 3/ Signal Options

The DRIVE SELECT 3/ signal is an output from the iSBX 218A board used to select the fourth drive (if connected) in multiple drive configurations. All 8-inch drives will accept the DRIVE SELECT 3/ signal on pin 32. However, on 5.25-inch drives, this signal is accepted on pin 22 or pin 50. The DRIVE SELECT 3/ default jumper configuration is routed to pin 22. Consult Table A-2 and your drive manual to verify its requirements. Table 2-6 outlines the DRIVE SELECT 3/ options.

Table 2-6. DRIVE SELECT 3/ Options

Feature Selected	Jumper(s) Installed
DRIVE SELECT 3/ connected to J1-32	13 - 14
DRIVE SELECT 3/ connected to J1-22	5 - 8 §
DRIVE SELECT 3/ connected to J1-50	4 - 5
Notes: § = factory default configuration.	

2.8.4.3 SIDE SELECT/ Signal Options

The SIDE SELECT/ signal is an iSBX 218A board output signal. It selects one side of a double-sided drive. When SIDE SELECT/ is true (low), side 1 of the drive is selected. All double sided (DS) 8-inch drives accept this signal on line 14; all DS 5.25-inch drives accept it on pin 48. The iSBX 218A board default configuration is set for pin 14 and 48, meaning that the board sends the signal to both pins. Table 2-7 summarizes the SIDE SELECT/ jumper options.

Table 2-7. SIDE SELECT Options

Feature Selected	Jumper(s) Installed
SIDE SELECT connected to J1-14 only (for DS 8-inch drives)	none
SIDE SELECT connected to J1-14 & J1-48 (for DS 5.25-inch drives)	9 - 10 §
Notes: § = factory default configuration.	

2.8.4.4 INDEX/ Signal Options

The INDEX/ signal is an input signal to the iSBX 218A board from the selected drive. This signal is coincident with the detection of the index hole in the diskette. It indicates the logical beginning of a track on the diskette. All 8-inch drives output INDEX/ on pin 20; most 5.25-inch drives output INDEX/ on pin 24. The default configuration for this option is pin 24. Table 2-8 shows the two options available for the INDEX/ signal.

Table 2-8. INDEX/ Signal Options

Feature Selected	Jumper(s) Installed
INDEX/ on J1-20 (for 8-inch drives)	17 - 18
INDEX/ on J1-24 (for 5.25-inch drives)	16 - 17 §
Notes: § = factory default configuration.	

2.8.4.5 IN USE/ (J1-20) Signal Options

The IN USE signal is an output signal from the iSBX 218A board to the disk drive. Typically it is used to turn on the "in-use" or "busy" lamp on drives which are so equipped. Some drives, such as the Shugart Corporation Model 460, require IN USE/ to be grounded to enable the busy lamp. The iSBX 218A board offers several choices for the source of IN USE/. Table 2-9 summarizes these choices. The factory default configuration has the IN USE/ signal disconnected.

There are three ways of generating the IN USE/ signal: it can be enabled at all times; it can be generated by the 8272 device; it can be generated under program control, through one of four programmable latches or lines. Refer to Sections 4.5 and 4.6 for programming information.

Table 2-9. IN USE (J1-20) Signal Options

Feature Selected	Jumper(s) Installed
IN USE always enabled	15 - 18 (W)
IN USE enabled by 8272 HEAD LOAD	18 - 19 20 - 21
IN USE enabled by LATCH 0	18 - 19 20 - 23 (W)
IN USE enabled by LATCH 1	18 - 19 20 - 48 (W)
IN USE enabled by OPTION 0 (with inverting driver)	18 - 19 20 - 46 (W)
IN USE enabled by OPTION 0 (without driver)	18 - 46 (W)
IN USE enabled by OPTION 1 (with inverting driver)	18 - 19 20 - 45 (W)
IN USE enabled by OPTION 1 (without driver)	18 - 45 (W)

Notes: W = wire wrap jumper. § = factory default configuration.

If using IN USE/ with a driver (18 - 19) note that only one drive interface pin can be driven; however, two drivers can be connected to the same source.

2.8.4.6 MOTOR ON/ (J1-32) Signal Options

The MOTOR ON/ Signal is used by 5.25-inch drives to turn on (or off) the DC spindle motor in the drive. The iSBX 218A board offers several choices for the source of MOTOR ON/. Table 2-10 summarizes these choices. The factory default configuration has the MOTOR ON/ signal originating from LATCH 0. This latch is programmable. Therefore, in this mode, the MOTOR ON/ signal is under program control. Refer to Section 4.5 for latch programming information.

Table 2-10. MOTOR ON/ (J1-32) Signal Options

Feature Selected	Jumper(s) Installed
MOTOR ON/ always enabled	14 - 15
MOTOR ON/ enabled by LATCH 0	11 - 14 § 22 - 23 §
MOTOR ON/ enabled by LATCH 1	11 - 14 § 22 - 48 (W)
MOTOR ON/ enabled by OPTION 0 (with inverting driver)	11 - 14 § 22 - 46 (W)
MOTOR ON/ enabled by OPTION 0 (without driver)	14 - 46 (W)
MOTOR ON/ enabled by OPTION 1 (with inverting driver)	11 - 14 § 22 - 45 (W)
MOTOR ON/ enabled by OPTION 1 (without driver)	14 - 45 (W)

Notes: § = factory default configuration; W = wire wrap jumper.

If using MOTOR ON/ with a driver (11 - 14) note that only one drive interface pin can be driven; however, two drivers can be connected to the same source.

2.8.4.7 HEAD LOAD/ (J1-18) Signal Options

The HEAD LOAD/ signal is typically used by 8-inch drives. It causes the drive read/write head to move into place over the diskette, in preparation for read/write activity. If you are using an 8-inch drive, you must provide the HEAD LOAD/ signal to your drive. Some 8-inch "half-height" drives use the HEAD LOAD/ signal for motor on-off control. The iSBX 218A board offers several choices for the source of HEAD LOAD/. Table 2-11 summarizes these choices. The default configuration for the HEAD LOAD/ signal is to have it de-selected (i.e., not installed).

There are three ways of generating the HEAD LOAD/ signal: it can be enabled at all times; or it can be generated by the 8272 device; or it can be generated under program control, through one of four programmable latches or lines. Refer to Chapter 4 for programming information.

Table 2-11. HEAD LOAD/ (J1-18) Signal Options

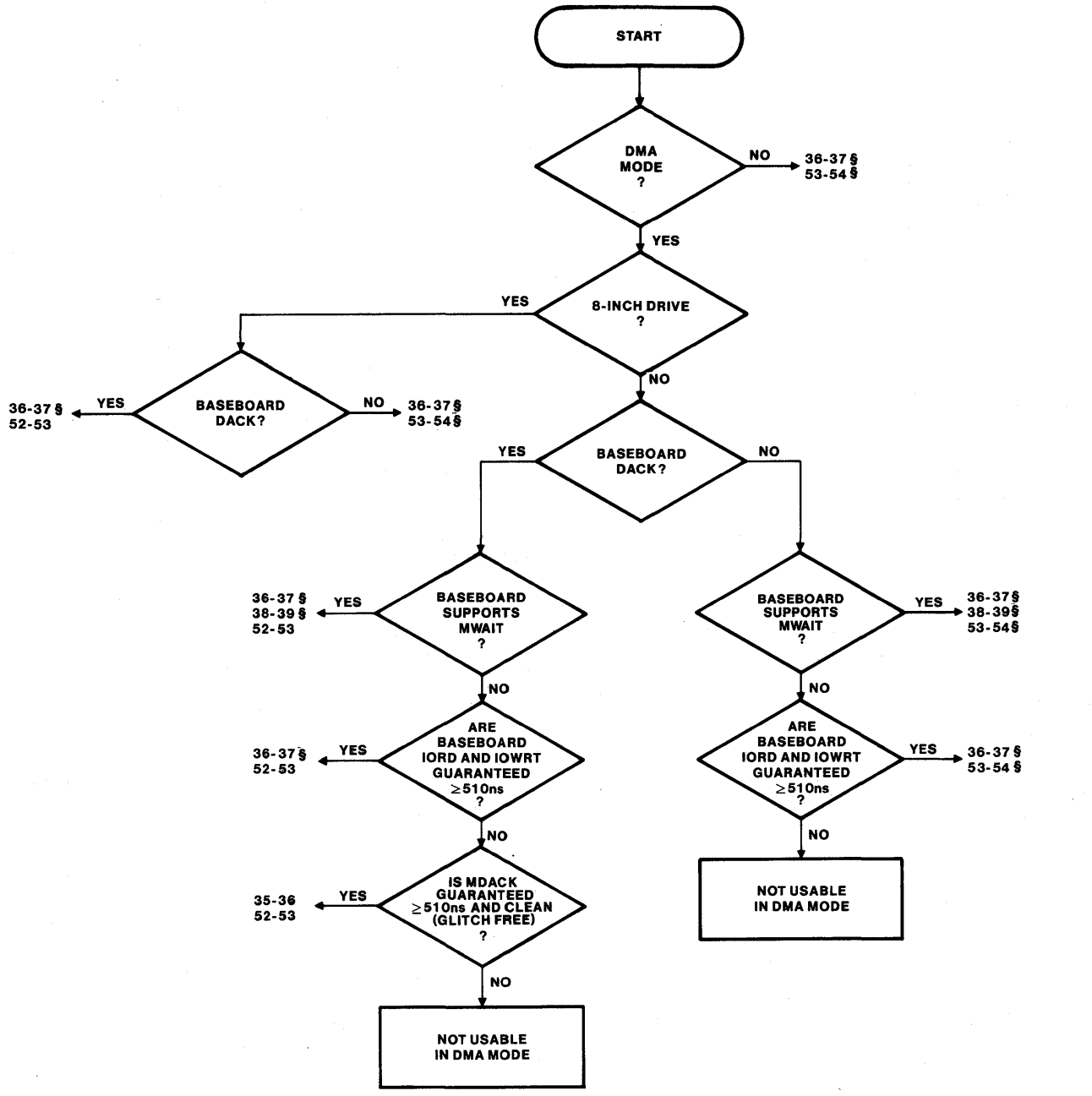
Feature Selected	Jumper(s) Installed
HEAD LOAD/ always enabled	12 - 15
HEAD LOAD/ enabled by 8272 HEAD LOAD	11 - 12 21 - 22
HEAD LOAD/ enabled by LATCH 0	11 - 12 22 - 23
HEAD LOAD/ enabled by LATCH 1	11 - 12 22 - 48 (W)
HEAD LOAD/ enabled by OPTION 0 (with driver)	11 - 12 22 - 46 (W)
HEAD LOAD/ enabled by OPTION 0 (without driver)	12 - 46 (W)
HEAD LOAD/ enabled by OPTION 1 (with driver)	11 - 12 22 - 45 (W)
HEAD LOAD/ enabled by OPTION 1 (without driver)	12 - 45 (W)

Notes: W = wire wrap jumper; § = factory default configuration.

If using HEAD LOAD/ with a driver (11 - 12) note that only one drive interface pin can be driven; however, two drivers can be connected to the same source.

2.8.5 DIRECT MEMORY ACCESS (DMA) CONFIGURATION

If your host board supports DMA operations you must configure the iSBX 218A board to ensure that the two boards are configured for the same level of DMA support. There are several ways to approach DMA operations with the iSBX 218A board and your host board. To simplify this approach, a flowchart of the suggested configuration process is shown in Figure 2-3. This flowchart explains how to configure all the iSBX 218A board jumpers which are related to DMA operations.



Note: 38-39 should be removed unless otherwise indicated. §=Indicates default jumper

Figure 2-3. DMA Configuration Process

NOTE

The iSBX 218A board is configured at the factory to operate without modification on an iSBC 215G host board (PBA number 144263-009 or higher), and for using Shugart Corporation Model 450 5.25-inch drives (or compatible drive). However, the iSBC 215G board requires several jumper modifications. See Section 2.8.9 for details.

If you choose not to use DMA or if your system does not support DMA, only two jumpers are required for this step of the configuration process (refer to Figure 2-3). However, if you elect to use DMA you must follow the configuration process outlined in Figure 2-3. In some cases your host board may not be able to provide the required signals or may not be able to provide a particular signal in the correct time frame. If your host board cannot meet these requirements, do not use DMA mode for data transfers. Instead, your system program will require a high-speed I/O loop for handling the required data transfers. The following paragraphs describe the DMA configuration process.

DMA Configuration Summary:

Before configuring your board for DMA operations study the flowchart in Figure 2-3. You need to know if your host board supplies or supports the following signals: DMA Acknowledge (DACK) and Multimodule Wait (MWAIT). The flowchart outlines what you need to know about your system before you configure the iSBX 218A board for DMA operation. In addition, you may need to know if your host board's I/O READ, I/O WRITE and DACK signals are present for at least 510 nanoseconds.

The following procedure describes the flowchart in Figure 2-3. Your DMA mode jumper configuration is complete the first time you reach a jumper configuration point. Do not go beyond the first DMA jumper configuration point you encounter.

1. Specify drive size. If you select 8-inch drives, you must know if your host board provides a DMA Acknowledge signal (DACK). If yes, install jumpers 36-37 and 52-53. If no, install jumpers 36-37 and 53-54 (these are installed at the factory).

   The remainder of this summary applies to 5.25-inch drives only.

2. Does the host board support the DMA Acknowledge (DACK) signal? No jumpers are specifically required for this step. If yes, follow the path on the left side of the figure, and go on to step 3 below; if no, follow the path on the right side to the figure and skip ahead to step 6.

3. If you answered yes to #2, (host board does support DACK), then the next step is to determine if your host board supports MWAIT. If yes, install jumpers 36-37, 38-39, and 52-53. If no, go on to step 4.

   From this point on, if you answer yes to any decision, configure the specified jumpers and stop. No further DMA configuration is required if you answer yes to a decision block.

4. If your board does not support MWAIT then it must be able to hold the I/O READ and I/O WRITE commands for at least 510 nanoseconds. If your host board can meet this requirement, install jumpers 36-37 and 52-53. If the requirement cannot be met, go on to step 5.

5. If your board cannot meet the requirements in step 4, then it must generate MDACK and be able to hold this signal true for at least 510 nanoseconds. In addition, the MDACK signal must have clean ("glitch"-free) transitions. For example, MDACK driven by a DMA controller would provide a clean signal; MDACK derived from address decoding would not provide a clean signal. If your system meets these requirements, install jumpers 35-36 and 52-53. If your system cannot meet these requirements then you cannot use DMA mode.

6. If you answered no to #2, (host board does not support DACK), then the next step is to determine if your host board supports MWAIT. If yes, install jumpers 36-37, 38-39, and 53-54. If no, go on to step 7.

7. If your board does not support MWAIT then it must be able to hold the I/O READ and I/O WRITE commands for at least 510 nanoseconds. If your host board can meet this requirement, install jumpers 36-37 and 53-54. If your system cannot meet this requirement then you cannot use DMA mode.

Although the flowchart in Figure 2-3 and the descriptions above are sufficient to configure your board for DMA, the following two sections individually describe the effects of the jumpers covered in the flowchart.

2.8.5.1 DACK And MDACK Signal Options

Typical DMA Controllers respond to a DMA REQUEST (DRQ) by sending a DMA Acknowledge (DACK) and a command, either READ or WRITE. With a controller of this type, DACK on the iSBX Bus would be used and the on-board DACK generator would not be used. The 8272 was designed to do DMA with this type of controller.

Other DMA Controllers, such as those in the 8089 and 80186, do not use DACK. They respond to a DRQ with an address, a chip select (instead of DACK) and a command. The 8272 cannot be used directly in DMA mode with this type of controller.

The on-board DACK generator provides the interface between a DRQ-only controller and the DRQ-DACK 8272. The DRQ-only controller reads from or writes to the DACK Generator Port for DMA transfers, just as a DRQ-DACK controller would access the 8272. Since data and commands are bused, the 8272 receives all the same signals (except DACK) that it would receive from a DRQ-DACK controller. The DACK Generator logic then sends DACK to the 8272. When 5.25-inch drives are used in DMA Mode, this logic also generates MWAIT to the iSBX Bus to ensure that the DACK pulse to the 8272 is at least 510 nanoseconds wide.

On host boards which support DRQ-DACK DMA operations, the DMA Acknowledge (DACK) signal is routed directly from the host board to the iSBX 218A board through the MDACK line on the iSBX connector (pin 32). DACK must be simulated on host boards without this capability, if you are using DMA transfers. Table 2-12 outlines the choices for the DACK options. When the host board MDACK signal is used it can be qualified or not qualified by commands. Table 2-13 outlines the qualification options for MDACK. Refer to Figure 2-3 for more information.

Table 2-12. DACK Signal Source Options

Feature Selected	Jumper(s) Installed
DACK from host board	52 - 53
DACK not from host board (for programmed DACK or Non-DMA mode)	53 - 54 §
Notes: § = factory default configuration.	

Table 2-13. MDACK Signal Qualification Option

Feature Selected	Jumper(s) Installed
MDACK from host board (direct input, not qualified by READ or WRITE) to 8272	35 - 36
MDACK qualified by IORD or IOWT before going to 8272	36 - 37 §
Notes: § = factory default configuration.	

2.8.5.2 MWAIT/ Signal Options

The MWAIT/ signal is an output from the iSBX 218A board (pin 34 on the iSBX connector) which causes the host board to execute wait states when asserted. You can disable the MWAIT/ signal by removing jumper 38-39. Table 2-14 outlines the MWAIT/ signal options. Refer to Figure 2-3 for more information on configuring these jumpers.

Table 2-14. MWAIT Signal Options

Feature Selected	Jumper(s) Installed
MWAIT/ enabled to connector	38 - 39 §
MWAIT/ not enabled	removed
Notes: § = factory default configuration.	

2.8.6 TERMINATE DMA (TDMA) ENABLE OPTIONS

The iSBX 218A board activates TDMA (on the iSBX Bus) to terminate a DMA transfer. Because the 8272 interrupt output produces TDMA, the signal may change states at other times in addition to assertion at DMA termination (for example, when READY changes state). According to the iSBX Bus Specification the state of TDMA is relevant only during DMA transfers. This means that the host board must ignore TDMA at other times. If a host board is not capable of masking and unmasking TDMA (such as the iSBC 215G board), a mask circuit on the iSBX 218A board can be used instead. This mask circuit has four options associated with it: always enabled, always disabled, driven by one of the programmable latches, or driven by one of the iSBX Bus Option lines. Table 2-15 outlines the different TDMA ENABLE options.

NOTE

If your host board is an iSBC 215A/215B board or an iSBC 215G board (PBA 144263-008 or lower, and you are not using DMA mode, then TDMA should be disabled.

Table 2-15. TDMA ENABLE Signal Options

Feature Selected	Jumper(s) Installed
TDMA always enabled (TDMA same as MINTR1)	33 - 34
TDMA enabled by LATCH 0	23 - 33 (W)
TDMA enabled by LATCH 1	33 - 48 § (W)
TDMA enabled by OPTION 0	33 - 46 (W)
TDMA enabled by OPTION 1	33 - 45 (W)
TDMA disabled	33 - 35 (W)
Notes: § = factory default configuration; W = wire wrap jumper.	

2.8.7 TERMINAL COUNT OPTIONS

The Terminal Count (TC) input to the 8272 device can be driven by one of the latches or by one of the Option lines. In the iSBX 218 compatibility mode this input is driven by the Option 0 line. Table 2-16 outlines the different Terminal Count input jumpers.

Table 2-16. Terminal Count Signal Options

Feature Selected	Jumper(s) Installed
Terminal Count from Latch 0	23 - 47 (W)
Terminal Count from Latch 1	47 - 48
Terminal Count from Option 0	46 - 47 §
Terminal Count from Option 1	45 - 47 (W)
Notes: § = factory default configuration; W = wire wrap jumper.	

2.8.8 OTHER JUMPERS

There are two other jumper connections on the iSBX 218A board which are used for factory test purposes only. The following jumpers should be installed at all times:

40 - 41 §
66 - 67 §

2.8.9 SPECIAL iSBC® 215/215G CONFIGURATIONS

If you are installing the iSBX 218A board on an iSBC 215G board you must first check the iSBC 215G board to see what the printed board assembly (PBA) number of the iSBC 215G board is. The PBA number is marked on the component side of the board, near device U54 (right side). If the number is 144263-008 or lower, your iSBC 215G board will not operate correctly with the iSBX 218A board in the default configuration. Similarly, the iSBC 215A board and iSBC 215B board will not operate correctly with the iSBX 218A board in the default configuration. To use any of these non-compatible host boards, you must configure your iSBX 218A board as an iSBX 218 board, and not use any of the "A" features such as motor control and DMA mode transfers (see Section 2.8.10). However, on the iSBC 215G board only, if the PBA number is 144263-009 or higher, the board is fully compatible with the iSBX 218A board.

The iSBC 215G board (PBA 144263-009 or higher) is also compatible with the iSBX 217B Cartridge Tape Drive Interface Board. If you are using the iSBX 217B board, install it on iSBX connector J3.

In all cases, install the iSBX 218A board on iSBX connector J4. Additionally, you must configure the jumpers on your iSBC 215G board for proper operation. Table 2-17 outlines the iSBC 215G board jumper changes required for each possible combination of iSBX 218A board and iSBX 217B board.

NOTE

If your host board is an iSBC 215A/215B board or an iSBC 215G board (PBA 144263-008 or lower, and you are not using DMA mode, then TDMA should be disabled. See Table 2-15.

Table 2-17. Required iSBC® 215G Jumper Modifications

W3	W4	W11	W24	J4 DMA Mode?	J3 DMA Mode?
IN	IN	1-3	X	NO	NO
IN	OUT	1-3	1-2	YES	NO
OUT	IN	1-3	1-3	NO	YES
OUT	OUT	1-3	NONE	YES	YES
			Note: X = irrelevant		

2.8.10 iSBX™ 218 BOARD EMULATION MODE

To use the iSBX 218A board in applications where it must emulate an iSBX 218 board jumper modifications are required. Install the jumpers in Table 2-18 to obtain complete hardware and software compatibility with and emulation of the iSBX 218 board.

Table 2-18. iSBX™ 218 Board Emulation Jumpers

Install the following jumpers for all applications:

1 - 2	28 - 29
7 - 8	31 - 32
11 - 12	33 - 35
13 - 14	35 - 36
17 - 18	40 - 41
21 - 22	46 - 47
24 - 25	50 - 51
66 - 67	

52 - 53 (Install only if DMA mode IS used)
53 - 54 (Install only if DMA mode IS NOT used)

Install the following jumpers for 8-inch drives only:

42 - 43	62 - 63
55 - 56	69 - 70
59 - 60	

Install the following jumpers for 5.25-inch drives only:

43 - 44	61 - 62
56 - 57	64 - 65
58 - 59	68 - 69

2.8.11 NUMERICAL LIST OF JUMPERS

Table 2-19 is a list of all jumpers on the iSBX 218A board, arranged in numerical and functional order.

Table 2-19. Numerical List Of Jumpers

READY/ input from J1-22 (for most 8-inch drives)	1 - 2 7 - 8
READY/ input from J1-50 (for most 5.25-inch drives with READY/ lines)	1 - 2 4 - 7
READY/ always true (for drives without READY/ lines)	3 - 7 (W)
DRIVE SELECT 3/ connected to J1-50	4 - 5
DRIVE SELECT 3/ connected to J1-22	5 - 8 §
READY/ from INDEX TIMEOUT (for drives without READY/ lines)	6 - 7 §
SIDE SELECT connected to J1-14 & J1-48 (for all 5.25-inch drives)	9 - 10 §
SIDE SELECT connected to J1-14 only (for all 8-inch drives)	removed
HEAD LOAD/ enabled by 8272 HEAD LOAD	11 - 12 21 - 22
HEAD LOAD/ enabled by LATCH 0	11 - 12 22 - 23
HEAD LOAD/ enabled by LATCH 1	11 - 12 22 - 48 (W)
HEAD LOAD/ enabled by OPTION 0 (with driver)	11 - 12 22 - 46 (W)
HEAD LOAD/ enabled by OPTION 1 (with driver)	11 - 12 22 - 45 (W)
MOTOR ON/ enabled by LATCH 0	11 - 14 § 22 - 23 §
MOTOR ON/ enabled by LATCH 1	11 - 14 § 22 - 48 (W)
MOTOR ON/ enabled by OPTION 0 (with driver)	11 - 14 § 22 - 46 (W)
MOTOR ON/ enabled by OPTION 1 (with driver)	11 - 14 § 22 - 45 (W)
HEAD LOAD/ always enabled	12 - 15
HEAD LOAD/ enabled by OPTION 1 (w/o driver)	12 - 45 (W)
HEAD LOAD/ enabled by OPTION 0 (w/o driver)	12 - 46 (W)
DRIVE SELECT 3/ connected to J1-32	13 - 14
MOTOR ON/ always enabled	14 - 15
MOTOR ON/ enabled by OPTION 1 (w/o driver)	14 - 45 (W)
MOTOR ON/ enabled by OPTION 0 (w/o driver)	14 - 46 (W)
IN USE always enabled	15 - 18 (W)
INDEX/ on J1-24 (for 5.25-inch drives)	16 - 17 §
INDEX/ on J1-20 (for 8-inch drives)	17 - 18

Table 2-19. Numerical List Of Jumpers (continued)

IN USE enabled by 8272 HEAD LOAD	18 - 19 20 - 21
IN USE enabled by LATCH 0	18 - 19 20 - 23 (W)
IN USE enabled by LATCH 1	18 - 19 20 - 48 (W)
IN USE enabled by OPTION 0 (with driver)	18 - 19 20 - 46 (W)
IN USE enabled by OPTION 1 (with driver)	18 - 19 20 - 45 (W)
IN USE enabled by OPTION 1 (without driver)	18 - 45 (W)
IN USE enabled by OPTION 0 (without driver)	18 - 46 (W)
TDMA enabled by LATCH 0	23 - 33 (W)
Terminal Count from Latch 0	23 - 47 (W)
125 ns write precompensation	24 - 25 §
	31 - 32 §
250 ns write precompensation	25 - 26
	30 - 31
Write precompensation on inner tracks	27 - 28
Write precompensation on all tracks	28 - 29 §
No write precompensation	28 - 35 (W)
TDMA always enabled (TDMA same as MINTR1)	33 - 34
TDMA disabled	33 - 35 (W)
TDMA enabled by OPTION 1	33 - 45 (W)
TDMA enabled by OPTION 0	33 - 46 (W)
TDMA enabled by LATCH 1	33 - 48 § (W)
MDACK from host board (direct input, not qualified by READ or WRITE) to 8272	35 - 36
MDACK qualified by IORD or IOWT before going to 8272	36 - 37 §
MWAIT/ enabled to connector	38 - 39 §
MWAIT/ disabled to connector	removed
Factory Test Jumper	40 - 41 §
Drive Size: 8-Inch	42 - 43 55 - 56 59 - 60 62 - 63 69 - 70
Drive Size: 5.25-Inch	43 - 44 § 56 - 57 § 58 - 59 § 61 - 62 § 64 - 65 § 68 - 69 §
Terminal Count from Option 1	45 - 47 (W)
Terminal Count from Option 0	46 - 47 §
Terminal Count from Latch 1	47 - 48

Notes: § = factory default configuration; W = wire wrap jumper.

Table 2-19. Numerical List Of Jumpers (continued)

I/O Port Features Enabled	49 - 50 §
I/O Port Features Disabled	50 - 51
DACK from host board	52 - 53
DACK not from host board (for programmed DACK or Non-DMA mode)	53 - 54 §
Factory Test Jumper	66 - 67 §

Note: § = factory default configuration; W = wire wrap jumper.

***

CHAPTER 3. BOARD INSTALLATION

3.1 INTRODUCTION

This chapter explains how to install the iSBX 218A board into your system. However, before installation, you should verify the jumper configurations discussed in Chapter 2. Once you have set up the jumpers according to your disk drive requirements and system requirements, proceed with the installation procedure in this chapter.

3.2 INSTALLATION CONSIDERATIONS

The iSBX 218A board is designed to interface with any host board which has an iSBX Bus connector on it. Other installation considerations such as power, cooling, mounting, and physical size requirements, are discussed in the following sections.

3.2.1 POWER REQUIREMENT

The power requirement for the Controller board is +5V (±0.25V) at 1.7A maximum. All power is provided to the iSBX 218A board from the host board via the iSBX connector.

3.2.2 COOLING REQUIREMENT

The iSBX 218A board dissipates about 8.50 watts. Adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F).

3.2.3 MOUNTING REQUIREMENTS

The iSBX 218A board mounts onto the host board via the iSBX connector and the proper mounting holes. The mounting hardware supplied as part of the iSBX 218A board includes:

a. 3 nylon spacers, 1/2" threaded, separate from the board.
b. 6 nylon screws, 1/4" 6-32, separate from the board.

3.2.4 PHYSICAL DIMENSIONS

Physical dimensions of the iSBX 218A board are as follows:

a. Width: 8.0 cm (3.15 inches)
b. Length: 19.1 cm (7.50 inches)
c. Height: 2.1 cm (0.83 inches)
d. Height with host 2.9 cm (1.13 in)

Refer to Figure 3-1 for additional dimensions.

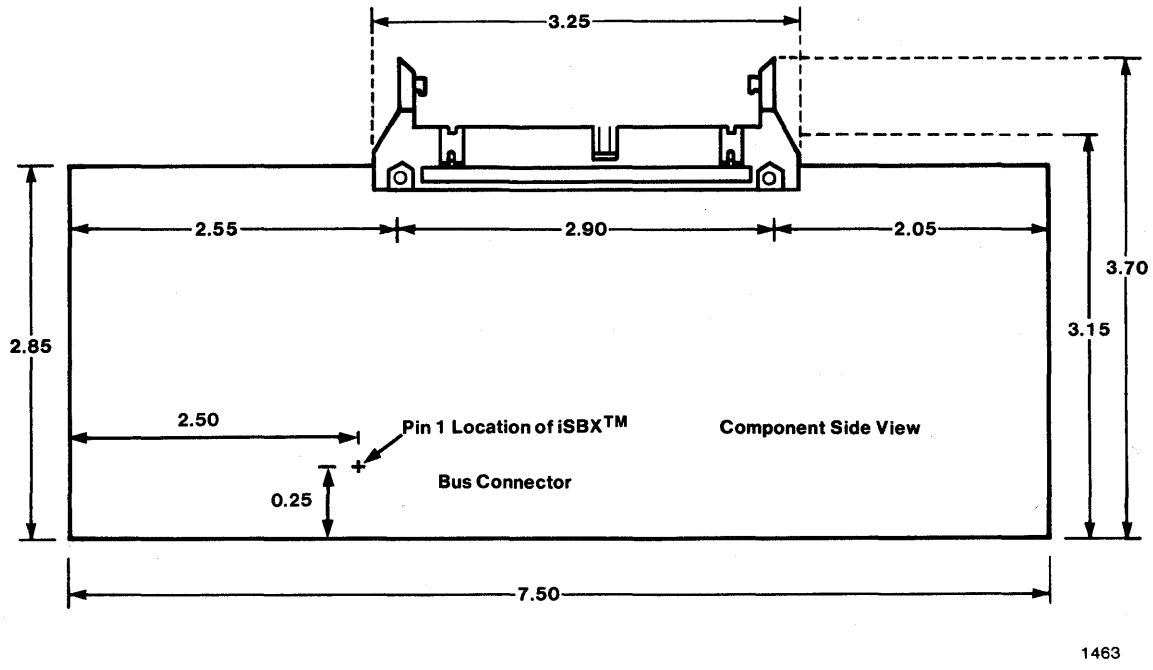


Figure 3-1. Board Dimensions (Inches)

3.2.5 ENVIRONMENTAL CONDITIONS

The board should be operated in accordance with the limits defined in Table 1-1 of this manual.

3.2.6 CONNECTOR CONFIGURATIONS

Connector P1 on the iSBX 218A board interfaces to the host board. Connector J1 on the iSBX 218A board interfaces to the diskette drives. The pin assignments for each connector are listed in Appendix A.

The location of each connector is shown in Figure 3-2. The J1 connector is used with a 50-conductor ribbon cable for one drive or for multiple drives. Notice that the conductor configuration for 5.25-inch drives is different than the 8-inch drive configuration. The 5.25-inch drives use a 34-pin cable, starting at pin 17 of the 50-pin connector. Refer to Table A-2 for pin assignments. Figure 3-3 shows the cable configuration.

NOTE

Pin 1 on the board does not correspond to the triangle symbol (usually indicating Pin 1) on the J1 connector. Use the numbers on the board for all pin assignments.

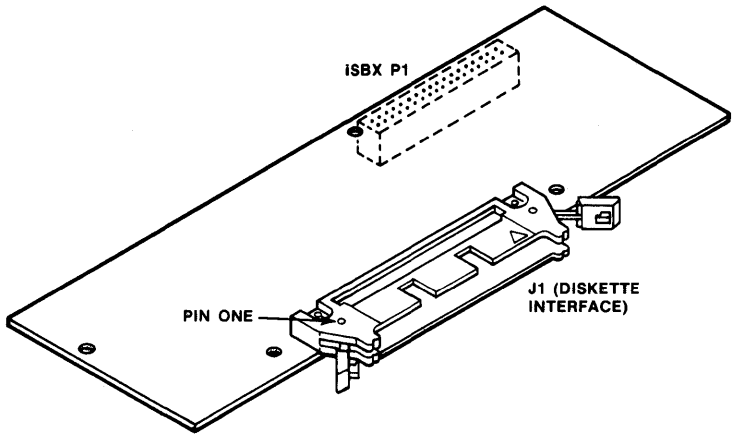


Figure 3-2. iSBX™ 218A Connector Locations

3.2.7 DRIVE CABLING

The iSBX 218A board uses a single 50-pin interface connector for both 8-inch drives and 5.25-inch drives. Typically, all 8-inch drives use the full 50-conductor flat cable or twisted pair, while the 5.25-inch drives use only 34 of these conductors. In both types, you can alter many of the individual drive interface signal pin assignments by configuring jumpers on the controller board; refer to Chapter 2.

To fabricate the drive interface cable, the cable ends are fitted with the appropriate mating connectors. When controlling multiple drives, additional drive mating connectors are inserted directly into the cable to form a daisy-chain cable.

The recommended maximum cable length between the controller and the last drive is 3 meters (10 feet); consult your drive manual specifications table for possible additional limitations. Figure 3-4 illustrates a typical daisy-chain flat ribbon cable designed to control two 8-inch drives with the iSBX 218A board.

Table 3-1 summarizes the recommended cable and connector part numbers for the iSBX 218A board:

Table 3-1. Recommended Cables And Connectors

Mating Connector To J1 on iSBX™ 218A	50-Pin Cable For 8-inch Drives	34-Pin Cable For 5.25-inch Drives
3M 3425-7050 or T&B Ansley 609-5001M	3M 3365/50 T&B Ansley 171-50 Spectra Strip (twisted pair) 455-248-50	3M 3365/34 T&B Ansley 171-34 Spectra Strip (twisted pair) 455-248-34

3.2.8 SIGNAL TERMINATION

All line terminations required on the iSBX 218A board are provided through the 220 ohm pull-up/330 ohm pull-down resistors in resistor pack RP1. This is a factory installed device and is not field-removable. Termination requirements for the diskette drive are listed in the drive manufacturer's manual. The last drive in a daisy chain string must be terminated. A typical four drive installation, showing cabling and termination location is given in Figure 3-5.

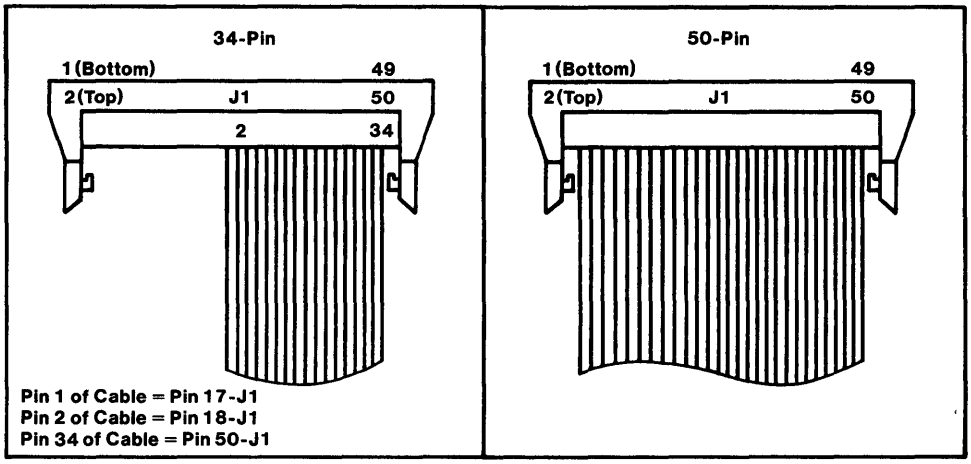


Figure 3-3. Disk Drive Cable Configuration

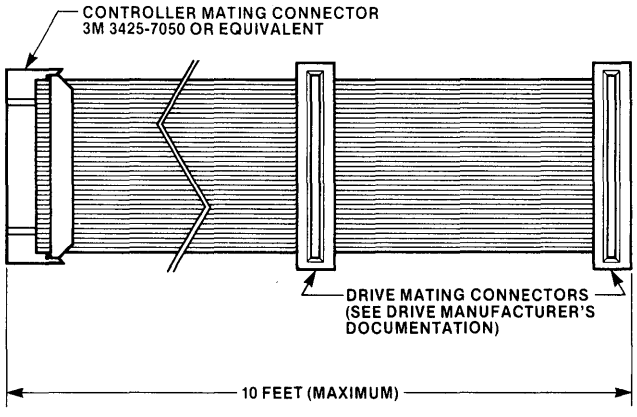


Figure 3-4. Flat Ribbon I/O Interface Cable

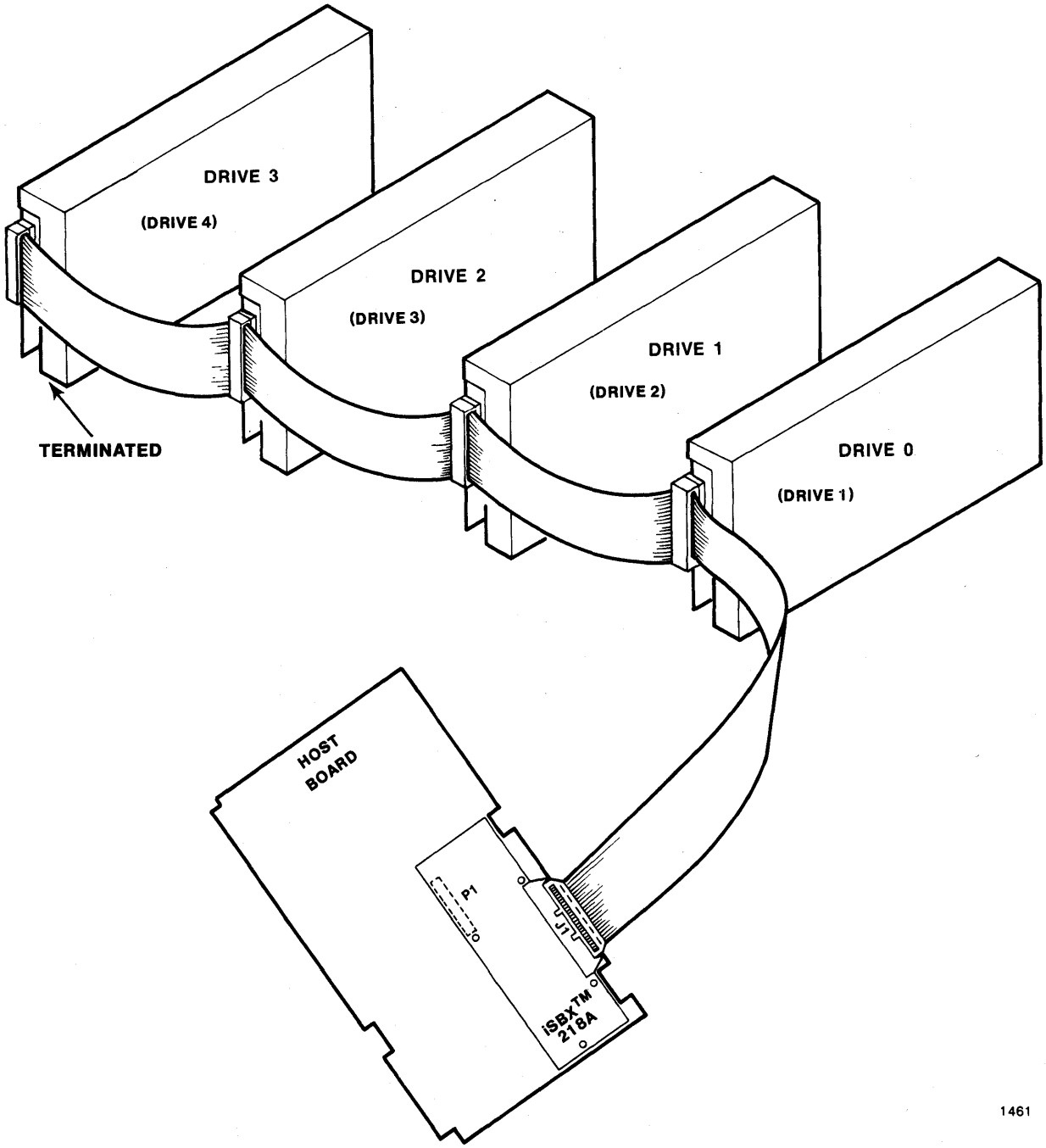


Figure 3-5. Typical Diskette Drive Installation

3.3 INSTALLATION PROCEDURE

The following procedure outlines how to install the iSBX 218A board. This procedure assumes you have already configured the board for the type of drive in your system.

1. With the 6-32 screws, secure the three 1/2 inch nylon spacers to the host board as shown in Figure 3-6.

2. Locate pin 1 on the iSBX connector (P1) on the iSBX 218A board and align it with pin 1 of the iSBX connector on the host board. If you are installing the iSBX 218A board on an iSBC 215G board, you must use the J4 iSBX Bus connector.

3. Align the iSBX 218A board mounting holes with the spacers on the host board.

4. Gently press the two boards together until the connector seats.

5. Fasten the iSBX 218A board to the spacers with the three remaining 6-32 nylon screws. See Figure 3-6.

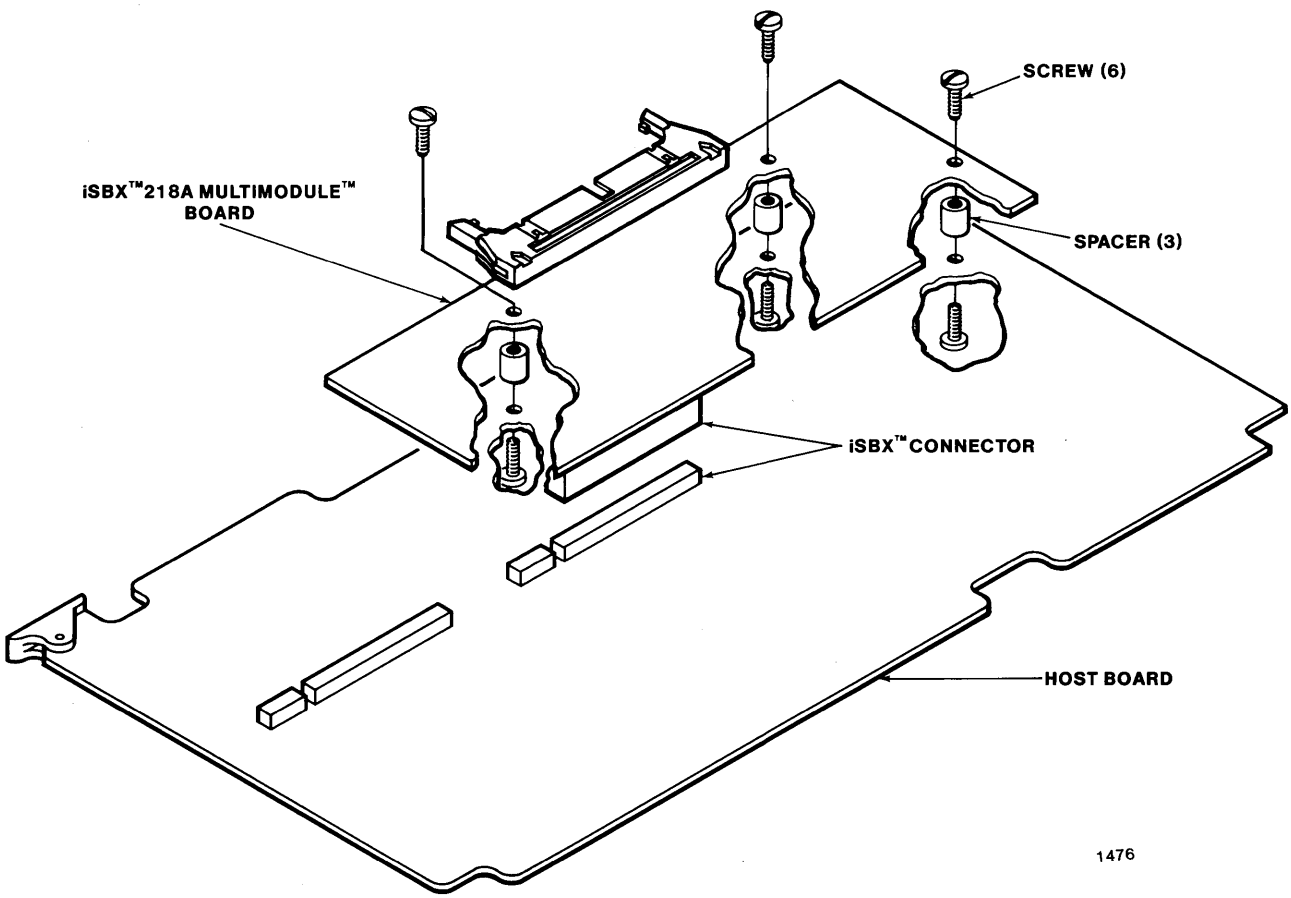


Figure 3-6. iSBX™ 218A Board Mounting Technique

CHAPTER 4. PROGRAMMING INFORMATION

4.1 INTRODUCTION

This chapter provides programming information for several special functions built into the iSBX 218A board. Board I/O addressing information is also provided in this chapter. Information on how to program and use the 8272 Flexible Disk Controller device is not covered here; refer to the 8272 data sheet or the component catalog for additional information. Special 8272 programming considerations not provided in the data sheet are given in Appendix B.

4.2 I/O ADDRESSING

In terms of programming, the host board communicates with the 8272 device and the special functions on the iSBX 218A board through an I/O addressing scheme. This addressing scheme varies depending on the addresses which your host board has reserved for its iSBX Bus connectors and the data bus width of the host board. Refer to the host board's reference manual for this information. Table 4-1 outlines the various signals which are used in conjunction with each other to produce the correct I/O address for the six iSBX 218A board I/O functions.

Table 4-1. I/O Address Signals

Function	Chip Select		Port Address	
	MCS0/	MCS1/	8-Bit Host	16-Bit Host
Read 8272 Status Register	1	0	nXX0	nXX00
Read/Write 8272 Data Register	1	0	nXX1	nXX10
Read/Write DACK Generator	0	1	n00X	n00X0
Write Reset Latch	0	1	n01X	n01X0
Read/Write Latch 0	0	1	n10X	n10X0
Read/Write Latch 1	0	1	n11X	n11X0

Notes: For MCS0 and MCS1, asserted = 1, not asserted = 0. For port address X = irrelevant. The n is host board dependent and represents all the high order port address lines. For 8-bit hosts, the n = I/O address lines A7 through A3. For 16-bit hosts, the n = I/O address lines A15 (or AF Hex) through A4. Select the host port address that combines the indicated chip select (MCS0 or MCS1) with the low order address bits shown.

As an example, Table 4-2 shows how the I/O addressing would be accomplished on an Intel iSBC 86/30 board.

Table 4-2. I/O Addressing Example With iSBC® 86/30 Board

Address (J3 Connector)	Function	
00A0	8272 Main Status Register	Read only
00A2	8272 Data Register	Read/Write
00B0	On-board DACK Generator	Read/Write
00B2	Reset Latch	Write only
00B4	Latch 0	Read/Write
00B6	Latch 1	Read/Write

Address (J4 Connector)	Function	
0080	8272 Main Status Register	Read only
0082	8272 Data Register	Read/Write
0090	On-board DACK Generator	Read/Write
0092	Reset Latch	Write only
0094	Latch 0	Read/Write
0096	Latch 1	Read/Write

4.3 ON-BOARD DACK GENERATOR

Typical DMA Controllers respond to a DMA REQUEST (DRQ) by sending a DMA Acknowledge (DACK) and a command (either READ or WRITE). With such a DMA controller, DACK on the iSBX Bus would be used and the on-board DACK generator would not be used. The 8272 was designed to operate in DMA mode with this type of controller.

Other DMA Controllers, such as those in the 8089 and 80186, do not use DACK. They respond to a DRQ with address and chip select (instead of DACK) and command. The 8272 cannot directly be used in DMA mode with this type of controller.

The on-board DACK generator provides the interface between a DRQ-only controller and the DRQ-DACK 8272. The DRQ-only controller reads from or writes to the DACK Generator Port for DMA transfers, just as a DRQ-DACK controller would access the 8272. Since data and commands are bused, the 8272 receives all the same signals (except DACK) that it would receive from a DRQ-DACK controller. The DACK Generator logic then sends DACK to the 8272. When 5.25-inch drives are used in DMA Mode, this logic also generates MWAIT to the iSBX Bus to ensure that the DACK pulse to the 8272 is at least 510 nanoseconds.

4.4 RESET LATCH

After MRESET (from the iSBX Bus) is asserted, the Reset Latch, Latch 0, Latch 1 and the 8272 are reset. Some host boards can drive MRESET under program control. The Reset Latch allows the programmer to do the same thing, even if the host board cannot drive MRESET.

The on-board reset signal is generated by writing to this port with data bit 0 set, followed by writing with data bit 0 clear. The other seven data bits are "irrelevant" bits.

The 8272 requires that the reset pulse be at least 14 clock periods, where 125 nanoseconds is the clock period for 8-inch drives and 250 nanoseconds is the clock period for 5.25-inch drives. Therefore, the programmer must ensure that the set and clear commands to the reset latch are separated by at least 1.75 microseconds for 8-inch drives or 3.5 microseconds for 5.25-inch drives.

4.5 LATCH 0 AND LATCH 1

The output of Latch 0 or Latch 1 can be set high by writing to the appropriate port with data bit 0 set (logic 1). It can be cleared by writing with data bit 0 clear (logic 0). Reading this port returns (in data bit 0) the condition of the corresponding latch. In all cases, data bits one through seven are irrelevant.

The output of Latch 0 or Latch 1 can be jumpered through an inverting driver to the MOTOR ON pin of the drive interface. Since MOTOR ON is active low at the interface, writing a one turns the motor on. Consult the disk drive manual manual to determine the motor start-up time before an access can be made. The output of Latch 0 or Latch 1 can also be jumpered through an inverting driver to the HEAD LOAD, or IN USE pins of the drive interface. Two inverting drivers are available for MOTOR ON, HEAD LOAD, or IN USE.

Latch 0 or Latch 1 can be jumpered to one of the iSBX Bus Option lines or to the TDMA mask. Writing a zero to the latch disables TDMA and keeps it inactive on the iSBX Bus, regardless of 8272 activity. The iSBX 218A board meets the guidelines in the iSBX Bus Specification, even if TDMA is enabled all the time (in this case TDMA is the same as MINTR1). However, some host boards (specifically the iSBC 215G board) require that TDMA be maskable, if the iSBX 218A board is used in DMA mode.

Jumpers are also available for Latch 0 or Latch 1 to drive Terminal Count (TC) to the 8272. Writing a one corresponds to activating TC.

4.6 OPTION LINES

Both iSBX Bus Option lines are connected to jumper posts and are available for programmer-defined use. Option 0 is easily jumperable to drive Terminal Count (TC), to enable the iSBX 218A board to be used in iSBX 218 (non-A) applications.

Option lines can also be used to drive MOTOR ON, HEAD LOAD, or IN USE (with or without inverting drivers), or the TDMA mask signal. Refer to Chapter 2 for additional information.

4.7 SPECIAL PROGRAMMING CONSIDERATIONS

In some instances, the iSBX 218A board may require special programming solutions to conditions which are not addressed in the 8272 data sheet. Refer to Appendix B for a list of these conditions and solutions.

***

CHAPTER 5. SERVICE INFORMATION

5.1 INTRODUCTION

This chapter provides a list of service diagrams and service and repair assistance instructions for the iSBX 218A board.

5.2 SERVICE DIAGRAMS

A jumper location diagram is shown in Figure 5-1. This helps you locate the jumper posts when configuring the board as described in Chapter 2. It also provides a list of the factory-installed, default jumpers. The parts location diagram and schematic diagram for the iSBX 218A board are provided in Figures 5-2 and 5-3, respectively. On the schematic diagram, a signal mnemonic that ends with a slash (e.g., ALE/) is active-low. Conversely, a signal mnemonic without a slash (e.g., ALE) is active-high.

5.3 SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance by contacting the Intel Product Service Marketing Administration in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Marketing Administration, you should have the following information available:

a. The date on which you received the product.

b. The complete model number (including dash number) and serial number for the product. These numbers are stamped onto the printed circuit boards.

c. Your shipping and billing addresses.

e. A purchase order number for billing purposes if your Intel product warranty has expired.

f. Any extended warranty agreement information, if applicable.

Use the following numbers for contacting the Intel Product Service Marketing Administration group:

Regional Telephone Numbers:

Western Region:	602-869-4951
Midwestern Region:	602-869-4392
Eastern Region:	602-869-4045
International:	602-869-4391

TWX Numbers:

910 - 951 - 1330
910 - 951 - 0687

Always contact the Product Service Marketing Administration group before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to Intel, use the original factory packing material, if possible. If this material is not available, wrap the product in cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by the Intel Product Service Marketing Administration personnel.

Factory Installed Jumpers:

05 - 08
06 - 07
09 - 10
11 - 14
16 - 17
22 - 23
24 - 25
28 - 29
31 - 32
33 - 48
36 - 37
38 - 39
40 - 41
43 - 44
46 - 47
49 - 50
53 - 54
56 - 57
58 - 59
61 - 62
64 - 65
66 - 67
68 - 69

Note: Jumper numbers are shown with an "E" prefix on the board.

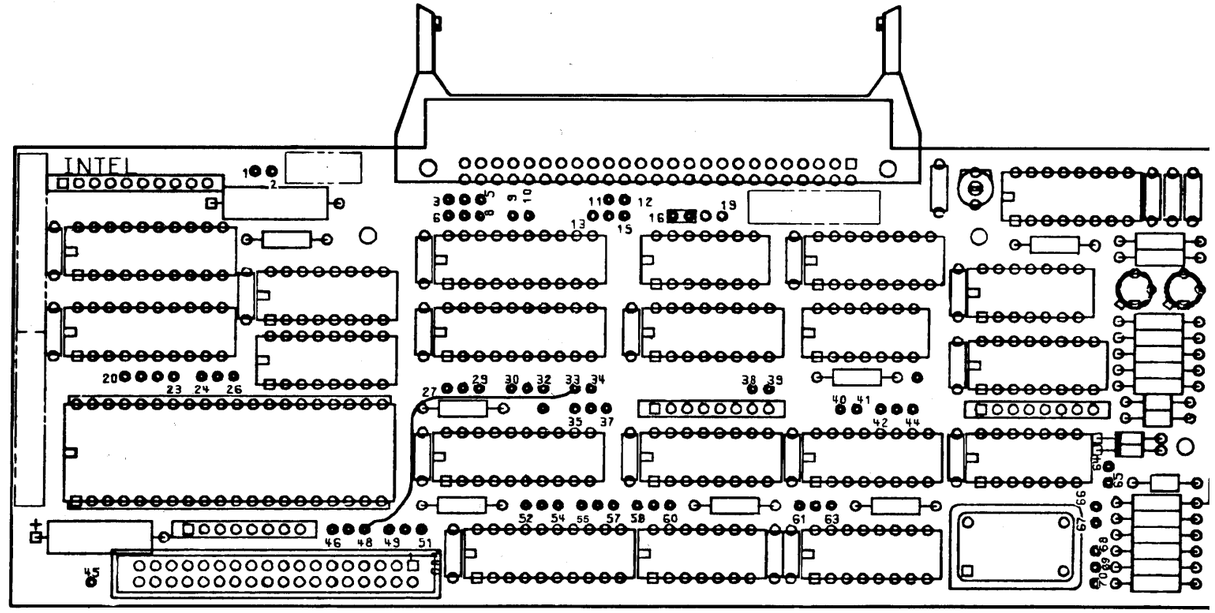


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Figure 5-1. iSBX™ 218A Jumper Post Location Diagram

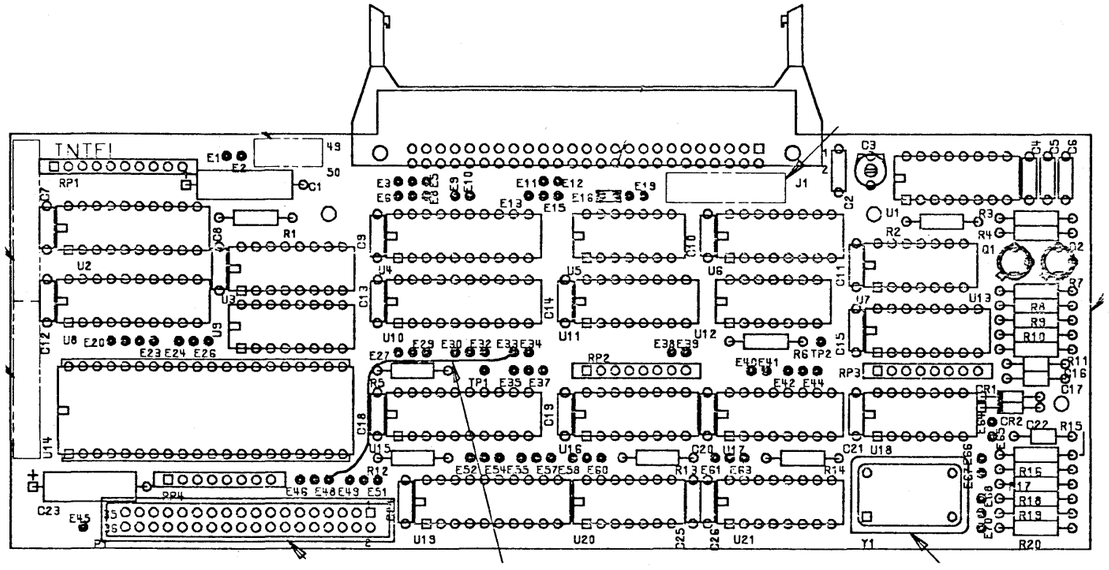

Figure 5-2. iSBX™ 218A Board Parts Location Diagram

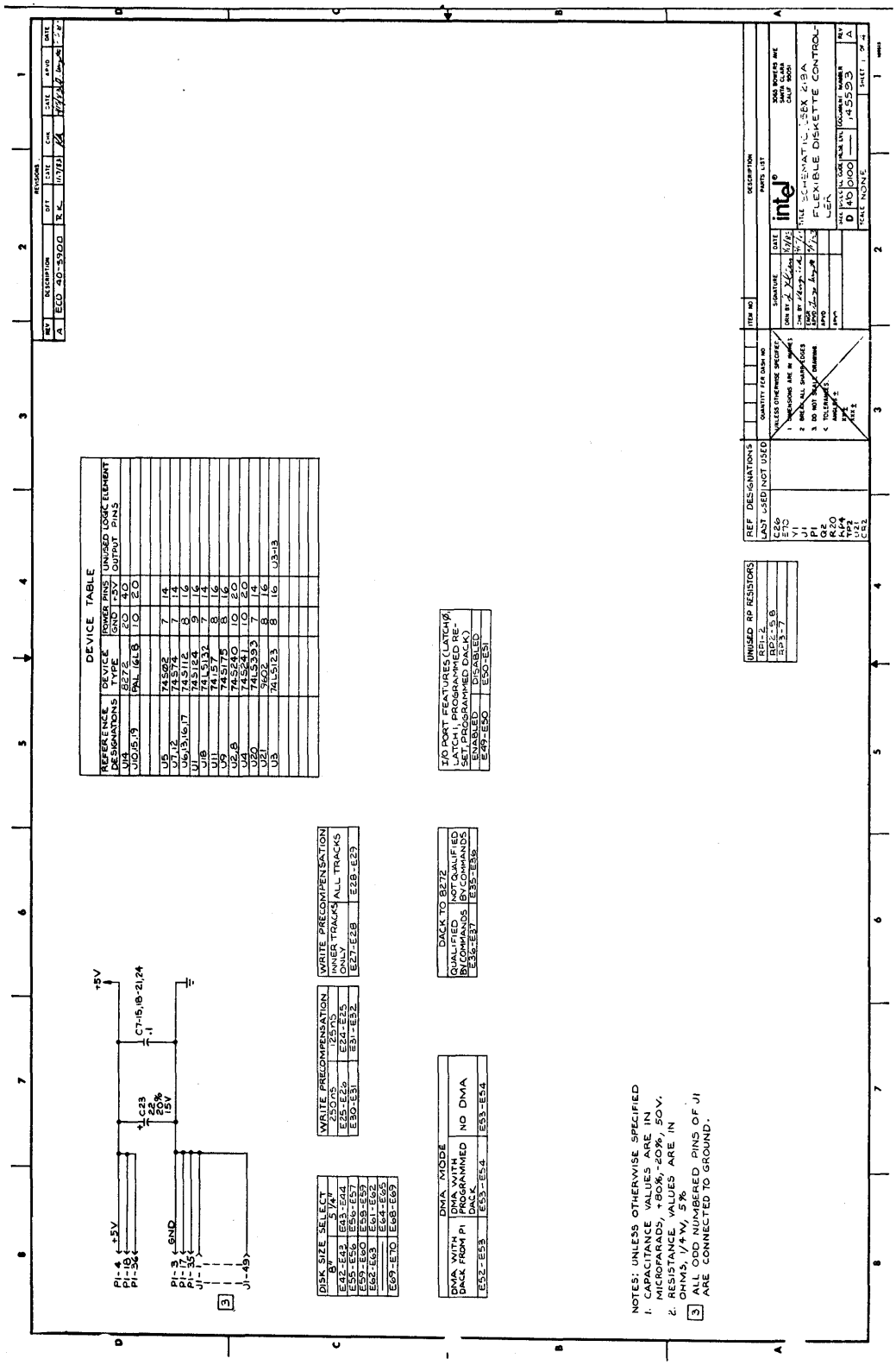

Figure 5-3. iSBX™ 218A Board Schematic Diagram (Sheet 1)

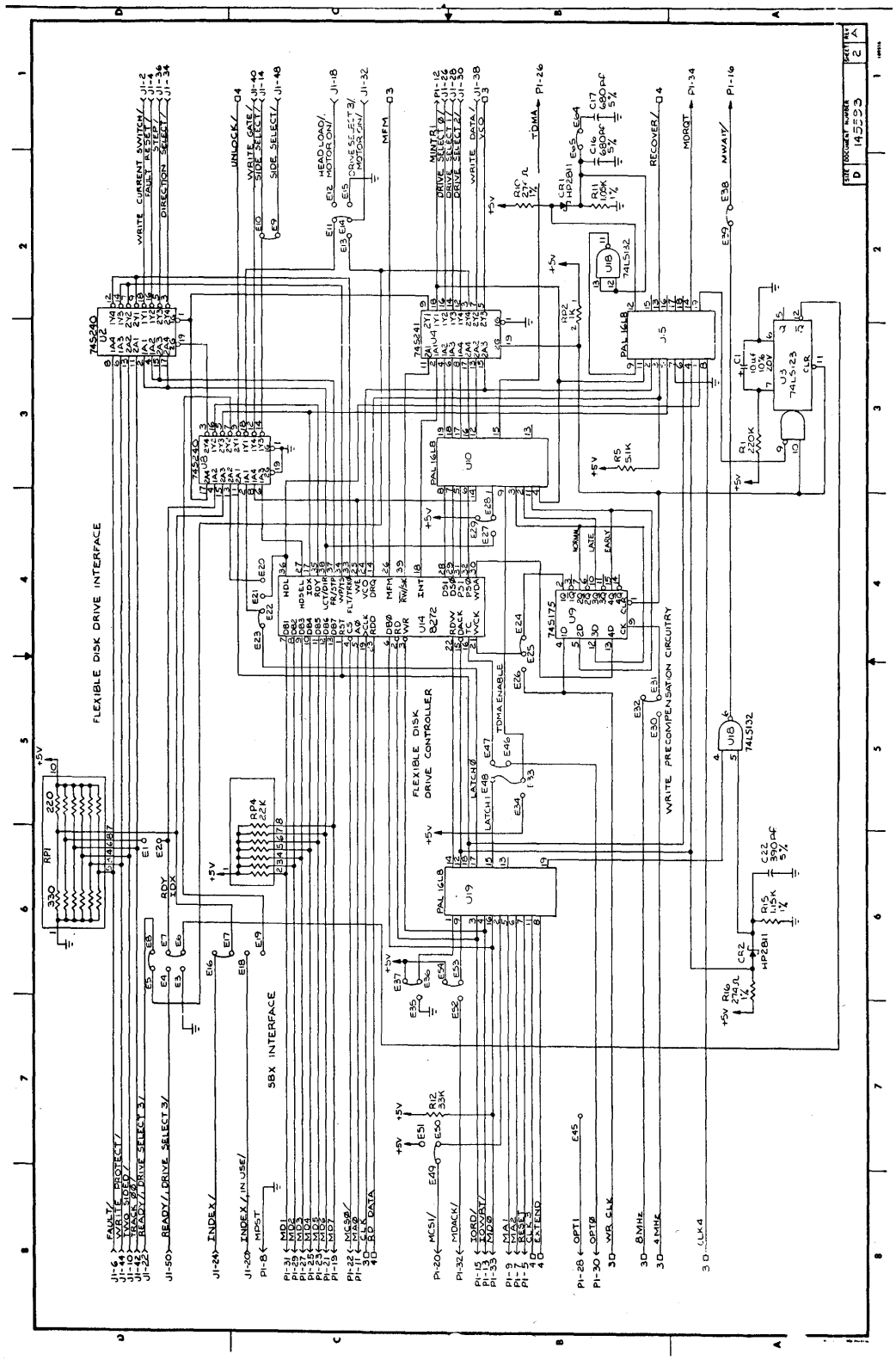

Figure 5-3. iSBX™ 218A Board Schematic Diagram (Sheet 2)

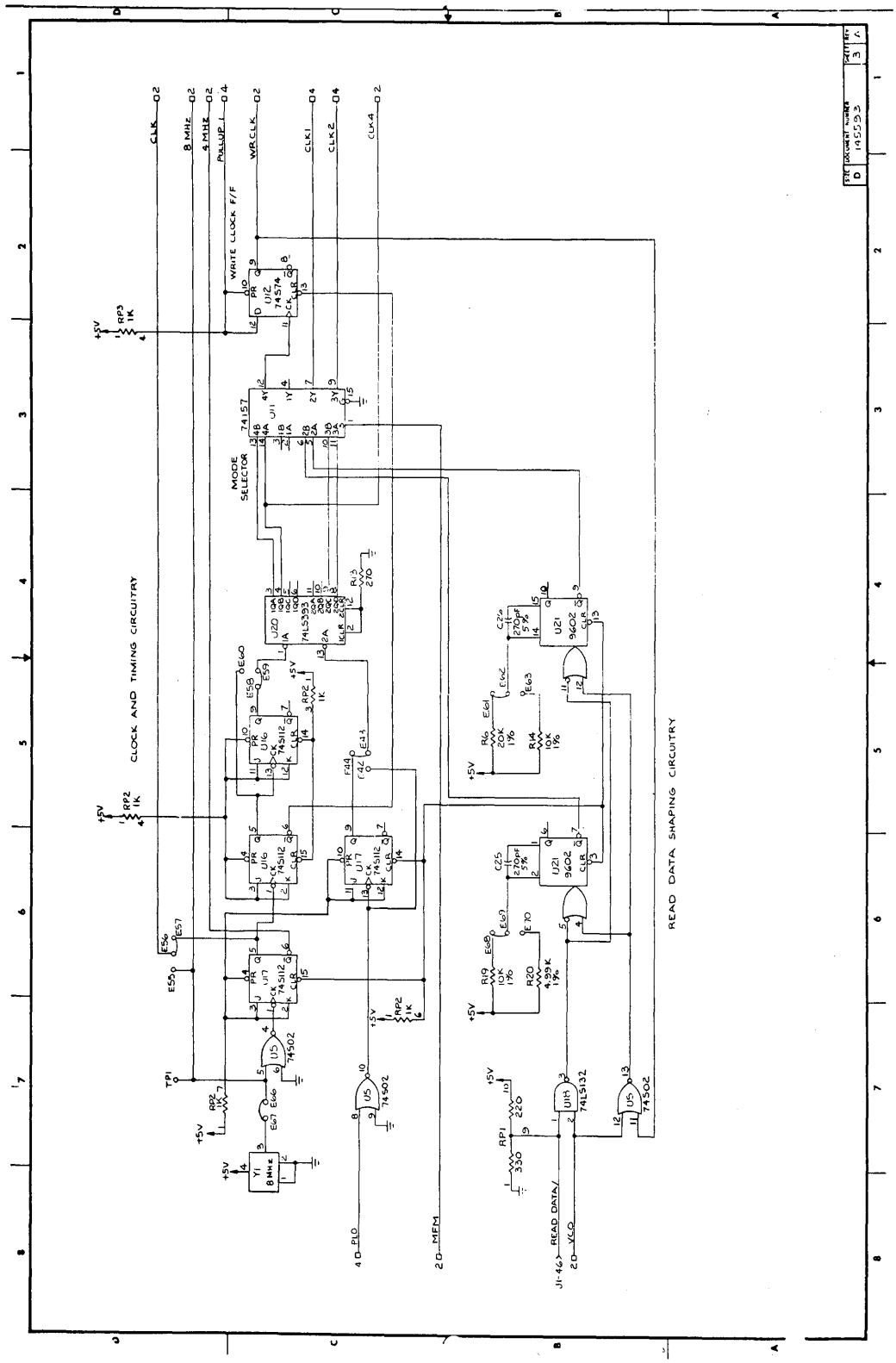

Figure 5-3. iSBX™ 218A Board Schematic Diagram (Sheet 3)

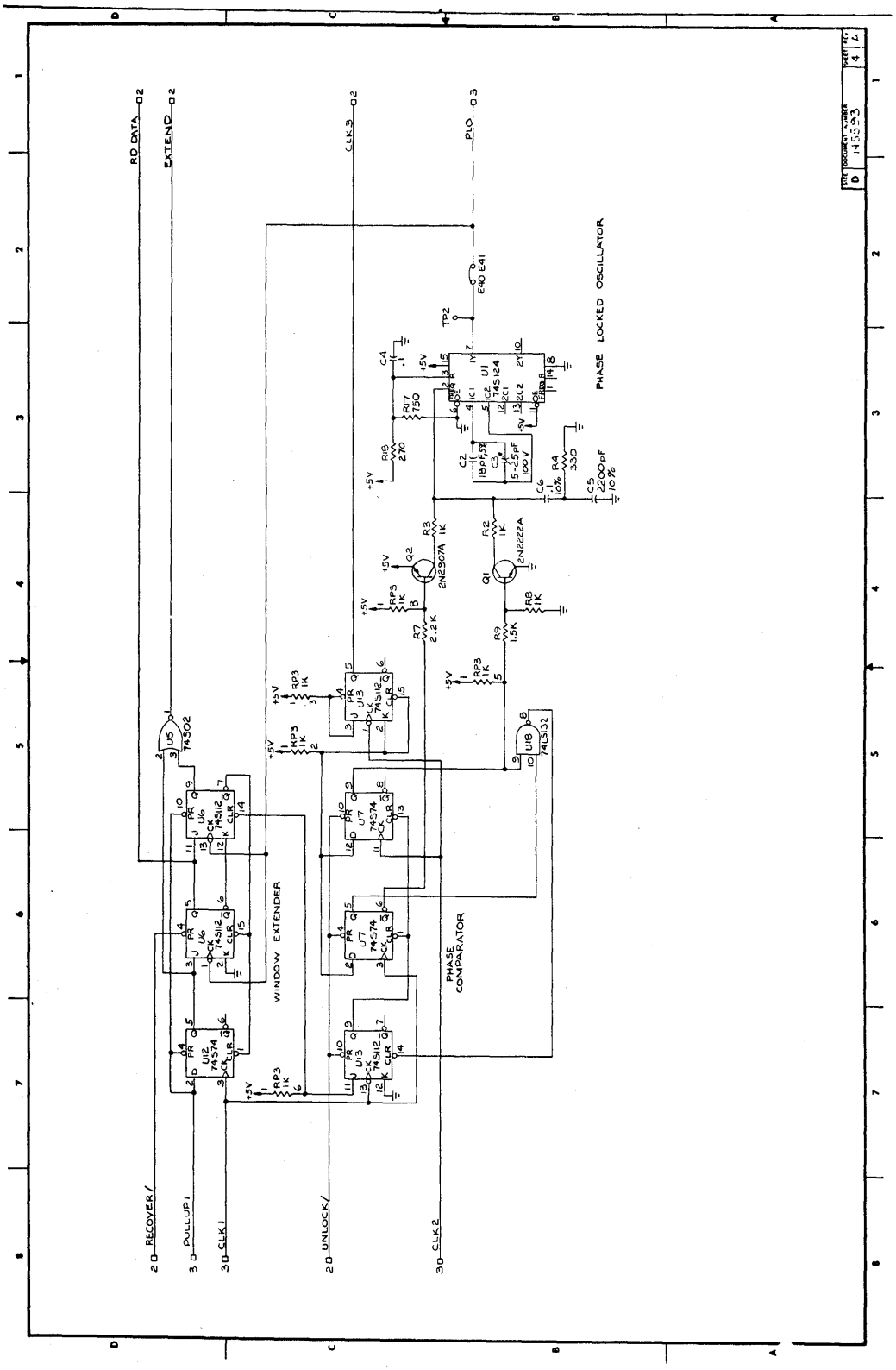

Figure 5-3. iSBX™ 218A Board Schematic Diagram (Sheet 4)

***

APPENDIX A. CONNECTOR PIN ASSIGNMENTS

This appendix provides the connector pin assignments for the iSBX Bus connector (P1) and the disk interface connector (J1). Refer to Tables A-1 and A-2.

Table A-1. iSBX™ Bus Connector Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	Not Used		2	Not Used	
3	GND	Signal Ground	4	+5V	+5 Volts
5	RESET	Reset	6	Not Used	
7	MA2	Address 2	8	MPST/	Exp. Module Present
9	MA1	Address 1	10	Not Used	
11	MA0	Address 0	12	MINTR1	Interrupt 1
13	IOWRT/	I/O Write Command	14	Not Used	
15	IORD/	I/O Read Command	16	MWAIT/	Exp. Module Wait
17	GND	Signal Ground	18	+5V	+5 Volts
19	MD7	Data Bit 7	20	MCS1/	Chip Select 1
21	MD6	Data Bit 6	22	MCS0/	Chip Select 0
23	MD5	Data Bit 5	24	Not Used	
25	MD4	Data Bit 4	26	TDMA	Terminate DMA
27	MD3	Data Bit 3	28	OPT1	Option 1
29	MD2	Data Bit 2	30	OPT0	Option 0
31	MD1	Data Bit 1	32	MDACK/	DMA Acknowledge
33	MD0	Data Bit 0	34	MDRQT	DMA Request
35	GND	Signal Ground	36	+5V	+5 Volts

Note: Signals ending with a slash (/) are active-low. Signals without a slash are active-high.

Table A-2. Disk Drive Interface Connector (J1) Pin Assignments

50-pin* Connector Numbering	34-pin* Connector Numbering	Connection** Type	Function(s)
2		D	WRITE CURRENT SWITCH
4		D	FAULT RESET
6		D	FAULT
8			Not connected
10		D	TWO SIDED
12			Not connected
14		D	SIDE SELECT
16			Not connected
18	2	J	HEAD LOAD, MOTOR ON [2]
20	4	J	INDEX, IN USE[2]
22	6	J	READY[1], DRIVE SELECT 3
24	8	J	INDEX
26	10	D	DRIVE SELECT 0
28	12	D	DRIVE SELECT 1
30	14	D	DRIVE SELECT 2
32	16	J	DRIVE SELECT 3, MOTOR ON [2]
34	18	D	DIRECTION SELECT
36	20	D	STEP
38	22	D	WRITE DATA
40	24	D	WRITE GATE
42	26	D	TRACK 00
44	28	D	WRITE PROTECT
46	30	D	READ DATA
48	32	J	SIDE SELECT
50	34	J	READY [1], DRIVE SELECT 3
1-49(ODD)	1-33(ODD)	D	Signal Ground

Notes:

* 50-pin for 8-inch drives; 34-pin for 5.25-inch drives.

** D = Dedicated. This pin can only be the indicated function.
J = Jumperable. This pin is connected to a wire wrap post. It may be jumpered to any one of the functions indicated, or left open.

1. READY to the 8272 can also be grounded or connected to the index timeout circuit for drives that do not produce READY.
2. HEAD LOAD, MOTOR ON, or IN USE can also be grounded on the board.

***

APPENDIX B. SPECIAL 8272 PROGRAMMING INFORMATION

This appendix describes several special programming conditions which may arise when using the 8272 device. These special considerations are not covered in the 8272 data sheet.

UNIVERSAL APPLICATIONS

1. If the head is on the wrong cylinder and READ A TRACK command is executed, no error interrupt will be issued. The ST0 register does not show an abnormal termination (i.e., Bit's 6 and 7 are not set to "1"). But upon reading the ST2 register the bit 4 will be set (wrong cylinder).

   SOLUTION: Thru software - read ID after seek.

2. CRC errors could occur during READ A TRACK execution and not be indicated by ST0.

   SOLUTION: Thru software - always read ST1, ST2 after READ A TRACK.

3. Setting EOT bit in the command phase is not sufficient to terminate the execution phase.

   SOLUTION: Terminal count (TC) must be sent to the device. EOT is the final sector number of a cylinder. EOT as a terminate bit is supported only in the READ A TRACK command.

4. Second step pulse can occur prematurely (0-1ms), causing a seek error.

   SOLUTION: Program step rate time at least 1ms longer than minimum time required by drive.

5. The 8272 does not perform implied seeks.

   SOLUTION: Any READ/WRITE command must be preceded by: 1) seek command; 2) sense interrupt status; and 3) read ID.

6. The three SCAN commands do not work in accordance with the data sheet.

   SOLUTION: None - do not use.

7. RQM flag in status register will remain set for 12 microseconds (with 8-inch drives) and 24 usec (with 5.25-inch drives).

   SOLUTION: Software should not attempt to read the main status register before this time because you will erroneously assume that the 8272 is ready to receive the next command/parameter.

MINI-DRIVE (5.25-INCH) APPLICATIONS

1. Gap length programmability: 8272 can program Gap 3 only. Gap 5 is fixed at 40 bytes of "FF" plus 6 bytes of "00" (Sync).

   SOLUTION: Mini-floppies do not normally use Gap 5, so Gap 3 needs to be reduced to compensate for fixed Gap 5. Correct Gap length numbers are shown in Table B-1.

2. Multiple track write is not permitted with most mini drives. This is because of the turn-off time of the erase head coils - the head switches track before erase head turns off.

   SOLUTION: After write operation, the system should wait 1.3 milliseconds before attempting to step or change side.

Table B-1. Program Values Of N And Suggested Values Of GPL

			8-Inch Drive				5.25-Inch Drive			
Mode	Bytes Per Sector	N(3)	Sectors Per Track	EOT	R/W GPL(1)	Format GPL(2)	Sectors Per Track	EOT	R/W GPL(1)	Format GPL(2)
	128	00	-	-	-	-	18	12	07	09
	128	00	26	1A	07	1B	16	10	10	19
FM	256	01	15	0F	0E	2A	8	08	18	20
SINGLE	512	02	8	08	1B	3A	4	04	46	87
DENSITY	1024	03	4	04	47	8A	2	02	C8	FF
	2048	04	2	02	C8	FF	1	01	C8	FF
	4096	05	1	01	C8	FF	-	-	-	-
	256	01	-	-	-	-	18	12	0A	0C
	256	01	26	1A	0E	36	16	10	20	21
MFM	512	02	15	0F	1B	54	8	08	2A	50
DOUBLE	1024	03	8	08	35	74	4	04	80	F0
DENSITY	2048	04	4	04	99	FF	2	02	C8	FF
	4096	05	2	02	C8	FF	1	01	C8	FF
	8192	06	1	01	C8	FF	-	-	-	-

Notes:
1. Suggested values of GPL in READ or WRITE commands to avoid splice point between data field and ID field of contiguous sectors.
2. Suggested values of GPL in Format Command.
3. N = 00 is undefined in MFM (double density) mode.
4. Hex numbers are shown in EOT, R/W GPL, and FORMAT GPL columns; decimal in all others.

***

APPENDIX C. PAL INFORMATION

The iSBX 218A board is equipped with three programmable array logic (PAL) devices (U10, U15, U19). These devices are programmed at the factory to perform a specific function. The tables in this appendix give the hex values which were used to program the PAL devices and the equations which determine the function of the devices.

Table C-1. PAL Information For U10

```
PAL16L8
PAT NO 218AU10B
PRECOMP PAL AT U10

LCT LATE NORMAL INT PS1 PS0 DS0 DS1 ENABLE GND
EARLY WRDATA SPARE13 WE TDMA DRVSEL3 DRVSEL2 DRVSEL1 DRVSEL0 VCC

IF (VCC) /WRDATA = /WE +
                   LCT * /PS0 * /PS1 * NORMAL +
                   LCT * /PS0 * PS1 * LATE +
                   LCT * PS0 * /PS1 * EARLY +
                   /LCT * NORMAL

IF (VCC) /DRVSEL0 = /DS1 * /DS0

IF (VCC) /DRVSEL1 = /DS1 * DS0

IF (VCC) /DRVSEL2 = DS1 * /DS0

IF (VCC) /DRVSEL3 = DS1 * DS0

IF (VCC)    /TDMA = /ENABLE + /INT

IF (VCC) /SPARE13 = VCC


F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F .
F F F F F F F F F F F F F F F F F F F F 5 A F F 3 C F F F F F F .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D .
D D D D D D D D D D D D D D D D D D D D D D D 5 D D D D D C D D .
9 9 1 9 1 9 9 9 9 8 9 9 9 1 9 9 9 1 9 9 9 9 9 9 9 9 9 9 9 9 9 9 .
0 8 0 8 8 8 8 8 8 8 8 8 0 8 8 8 8 0 8 8 8 8 8 8 8 8 8 8 8 8 8 8 .
8 8 0 8 8 8 8 8 8 8 8 8 8 0 8 8 0 8 8 8 8 8 8 8 8 8 8 8 8 8 0 8 .
8 8 8 0 0 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
```

Table C-2. PAL Information For U15

```
PAL16L8
PAT NO 218AU15A
DMA PAL AT U15

HDLOAD VCO DRQ DACK INDEX BDRESET SPARE7 CLK DELAY GND
INT START RECOVER MDRQT AX BX CX DX TRIGGER VCC

IF (VCC) /MDRQT = /DRQ +
                  /DACK +
                  BDRESET +
                  INT +
                  /DELAY * /MDRQT

IF (VCC)   /AX = INDEX * VCO +
                 VCO * /BDRESET * /AX

IF (VCC)   /BX = /INDEX * /AX +
                 /AX * /BDRESET * /BX

IF (VCC)   /CX = INDEX * /BX +
                 /BX * /BDRESET * /CX

IF (VCC)   /DX = /INDEX * /CX +
                 /BDRESET * VCO * /CX * /DX

IF (VCC) /RECOVER = /RECOVER * /BDRESET * VCO * /DX +
                    INDEX * /DX

IF (VCC) /START = DRQ * DACK * /BDRESET * /INT * /MDRQT

IF (VCC) /TRIGGER = INDEX * HDLOAD +
                    CLK * /HDLOAD
```

```
F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F .
F F E F F F F F F F F D A 5 F B F F F 7 F F F F F F F F F F F F .
D F F E F F F D F F F 9 F F F 3 F 1 F 7 F F F F E F F F F F F F .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F .
A F F F 7 D F B 7 F F F E F F F F 3 F F F F F 7 F F F B F F F 7 .
6 7 7 7 7 7 7 3 7 5 7 7 3 7 7 7 7 6 7 6 7 7 7 7 7 7 7 7 7 7 7 7 .
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 0 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 .
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 0 2 .
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 0 2 2 2 2 2 0 2 2 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
```

Table C-3. PAL Information For U19

```
PAL16L8
PAT NO 218AU19A
IO PORTS PAL AT U19

QUAL MCS1 IORD IOWRT MA1 MA2 MRESET EXTEND MDACK GND
CLK3 DACK RLATCH RDW ALATCH MDO MLATCH BDRESET WAIT VCC

IF (VCC) /BDRESET = /MRESET * /RLATCH

IF (VCC) /MLATCH = BDRESET +
                   /IOWRT * /MCS1 * MA2 * /MA1 * /MDO +
                   /MDO * /MLATCH +
                   IOWRT * /MLATCH +
                   MCS1 * /MLATCH +
                   /MA2 * /MLATCH +
                   MA1 * /MLATCH

IF (VCC)    /RDW = EXTEND * /CLK3 +
                   /CLK3 * /RDW +
                   /EXTEND * /RDW

IF (/MCS1 * MA2 * /IORD) /MDO = /MA1 * /MLATCH +
                                MA1 * /ALATCH

IF (VCC) /ALATCH = BDRESET +
                   /MDO * /ALATCH +
                   /IOWRT * /MCS1 * MA2 * MA1 * /MDO +
                   IOWRT * /ALATCH +
                   MCS1 * /ALATCH +
                   /MA2 * /ALATCH +
                   /MA1 * /ALATCH

IF (VCC) /RLATCH = MRESET +
                   /IOWRT * /MCS1 * /MA2 * MA1 * /MDO +
                   /MDO * /RLATCH +
                   IOWRT * /RLATCH +
                   MCS1 * /RLATCH +
                   MA2 * /RLATCH +
                   /MA1 * /RLATCH

IF (VCC)   /DACK = QUAL * /MDACK * /IORD +
                   QUAL * /MDACK * /IOWRT +
                   /QUAL * /MDACK +
                   /IORD * /MA1 * /MA2 * /MCS1 +
                   /IOWRT * /MA1 * /MA2 * /MCS1

IF (VCC)   /WAIT = MDACK * MCS1 +
                   MDACK * MA1 +
                   MDACK * MA2
```

Table C-3. PAL Information For U19 (continued)

```
F 7 F F F 7 F F F F F F F F F F 7 F F F F F F F F F F F F F F .
E F F F F F B F F F F F 7 F 7 F F F F F F F F D F F F F F F D E F F F .
D 9 D D D D D D D D 9 D D 4 9 D 9 9 D D 5 D D D D D D D D C D D D .
5 5 5 5 5 5 5 5 5 5 5 5 1 5 5 5 1 4 5 5 5 5 5 5 5 5 5 5 5 4 5 5 5 .
4 4 4 4 4 4 4 4 0 4 4 0 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 .
0 4 4 4 4 4 4 4 4 4 4 4 0 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 .
4 4 4 4 4 4 4 4 4 4 4 4 0 4 4 4 4 4 4 0 4 4 4 4 4 4 4 4 4 4 4 4 4 .
4 4 4 4 4 4 4 4 4 4 4 4 0 0 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 .
F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F .
F F 7 F F 7 E F F F F F F F F F F F F F F B F F F D F F F F 7 F D .
F B 7 F F F F F F 3 F F B F F A F B F E F F F D F F F F F 7 F D .
F E F 7 F F F F F E F F E F F A E F F F F F F D F D F B F 7 F F .
D 5 D D D 5 D D 8 D D D D 5 D D D 5 D C D D D D D D D 9 D D D D .
8 5 D D D D D D D 5 D D D 5 D D D 5 D C D D D D D D D 9 D D D D .
5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 1 4 5 4 5 5 5 5 5 5 5 1 5 5 5 5 .
5 5 5 5 5 5 5 5 5 5 5 5 5 5 0 5 5 5 5 5 4 5 5 5 5 5 5 5 1 5 5 5 5 .
```

***

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