iSBX™ 217B
MAGNETIC CARTRIDGE TAPE INTERFACE MULTIMODULE™ BOARD HARDWARE REFERENCE MANUAL

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PREFACE

This manual describes the iSBX 217B Magnetic Cartridge Tape Interface Multimodule board. The manual explains how to use the features associated with a typical tape drive installation. For additional information, the following publications are available from the Intel Literature Department:

- Intel Multibus® Specification, Order Number: 9800683
- Intel iSBX™ Bus Specification, Order Number: 142686

N O T E

Throughout this manual an asterisk (*) following a signal name means that the signal is active-low. Former Intel manuals and schematic diagrams use a slash (/) to denote active-low signals.

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CHAPTER 1. GENERAL INFORMATION

1.1 INTRODUCTION

The iSBX 217B Magnetic Cartridge Tape Interface Board is an 8-bit, single-wide, iSBX Multimodule I/O expansion board for installation on any 8-bit or 16-bit iSBC host board which has an iSBX connector. Its function is to interface industry-standard 1/4 inch magnetic cartridge tape drives to a host Multibus processor board. The iSBX 217B board supports the Archive Corporation streaming tape drive interface, and the 3M Company HCD-75 interface. Each iSBX 217B board can support up to four tape drives (of the same manufacturer).

This manual provides the installation and setup information you need to interface the iSBX 217B board with a host iSBC board and a magnetic cartridge tape drive. Required interfacing information is provided in Chapter 3, and service information is covered in Chapter 4.

1.2 DESCRIPTION

The iSBX 217B board is designed to handle the interface and transfer of data from an iSBC host board such as the iSBC 215G Winchester Disk Controller board, to a 1/4 inch magnetic tape cartridge device. The transfer may occur in one of two modes: direct memory access (DMA) mode or a high-speed programmed I/O mode.

Three types of drives can be used with the iSBX 217B board: the high-speed, 90 inch-per-second (ips) Archive Corporation drive; the 30 ips Archive Corporation drive; and the 3M Company's HCD-75 drive. To use the 90 inch-per-second (ips) Archive drive, the host board must be capable of transferring data at 100K bytes/second or faster, or have DMA capability. Using the slower, 30 ips Archive drive, or the 3M drive is possible with any Intel host board, using either DMA or programmed I/O.

As with all other iSBX Multimodule boards, the iSBX 217B board plugs directly onto the host iSBC board via the iSBX Bus connector. This enables the iSBX board to communicate directly with the host board via the internal iSBX bus. All Intel iSBC boards with an iSBX connector support the required command and status signals for proper iSBX 217B board operation. Board power (+5VDC @ 1.50 amps) is provided by the host iSBC board, via the iSBX connector.

The tape drive interfaces to the iSBX 217B board through a single 50-pin connector (J1). The board is factory-configured for the Archive tape drive interface; you can reconfigure the board for the 3M Company drive by changing the jumper matrix configuration and installing several wires.

1.3 EQUIPMENT SUPPLIED

The iSBX 217B board is shipped from the factory with several pieces of plastic mounting hardware and a schematic diagram. The mounting hardware is used to secure the iSBX board to the iSBC host board. Installation instructions are provided in Chapter 2. The schematic diagram should be saved for future reference since it may be more current than the diagram in Chapter 4. Connectors and cable pieces are not supplied with the board. Connector information is provided in Chapter 2.

1.4 SPECIFICATIONS

Board specifications are listed in Table 1-1.

Table 1-1. Board Specifications

PHYSICAL DIMENSIONS	
Width:	3.70 inches (9.4 cm)
Length:	3.07 inches (7.8 cm)
Height:	0.80 inch (2.0 cm); see Figure 2-2
Weight:	3.5 ounces (98.0 gm)
CURRENT REQUIREMENTS	+5V @ 1.5 A Maximum
ENVIRONMENTAL CHARACTERISTICS	
Operating Temperature:	0°C to 55°C
Storage Temperature:	-40°C to 85°C
Humidity:	50% to 95% non-condensing @ 25°C to 40°C
Vibration & Shock:	2G maximum through 50Hz
Minimum Airflow:	200 linear feet/minute per board position.

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CHAPTER 2. PREPARATION FOR USE

2.1 INTRODUCTION

This chapter provides installation instructions and configuration information for the iSBX 217B board. The information presented in this chapter includes unpacking and inspection instructions; installation considerations such as physical dimensions, cooling requirements, and mounting instructions; connector pin assignments; and jumper configurations.

2.2 UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment contact the Intel Product Service HOTLINE to obtain a return authorization number and further instructions (see section 5-2). A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

2.3 INSTALLATION CONSIDERATIONS

The following sections provide installation information for the iSBX 217B board.

2.3.1 PHYSICAL DIMENSIONS

Physical dimensions of the iSBX 217B board are provided in Figure 2-1. Mounting clearance detail is shown in Figure 2-2.

NOTE

In some cardcage models, two slots are used by the host iSBC and iSBX board combination.

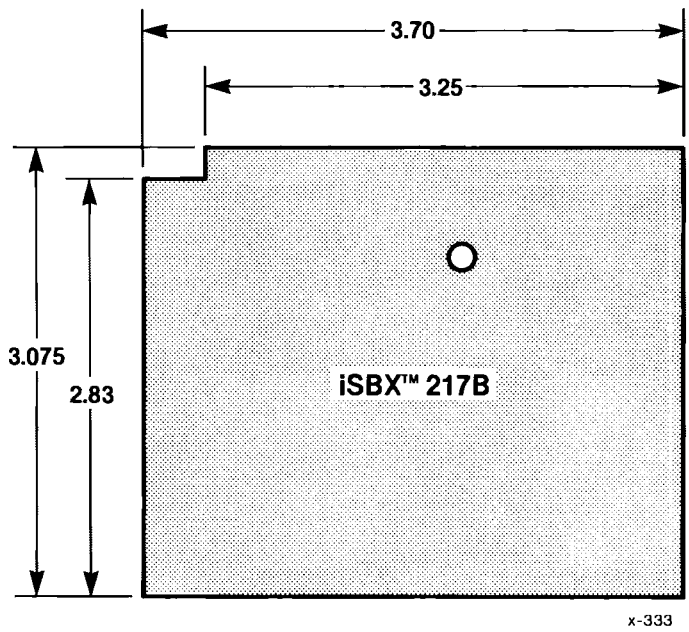

Figure 2-1. Physical Dimensions (Inches)

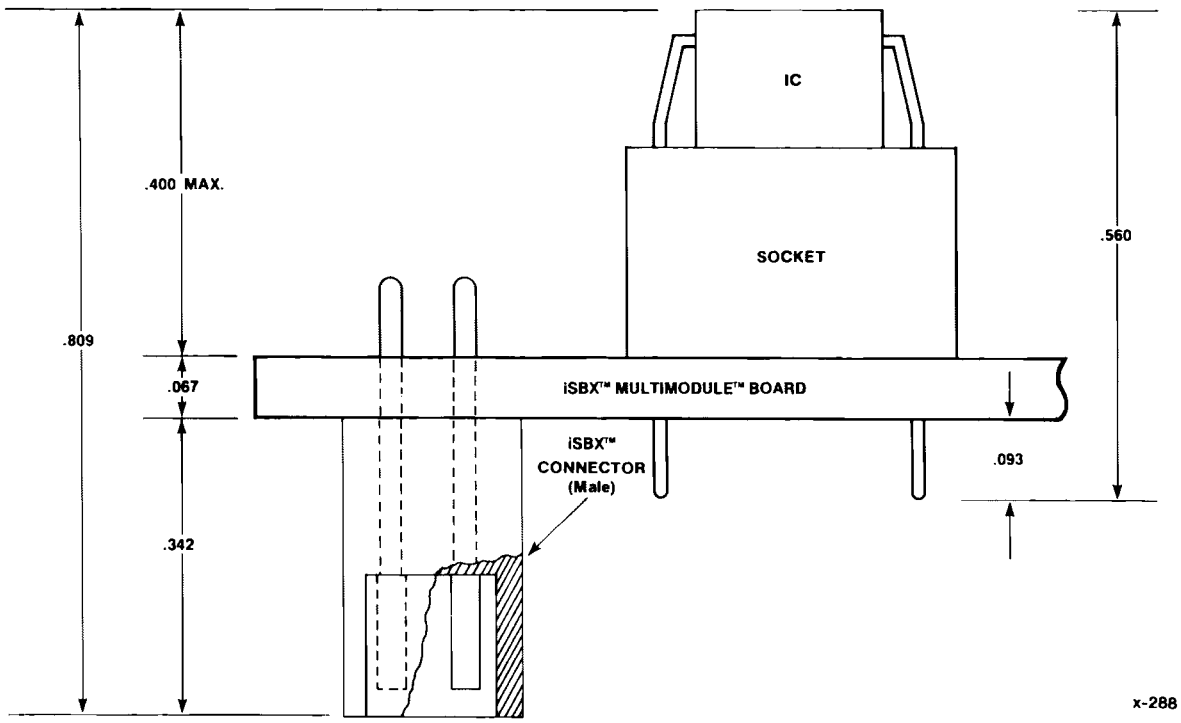

Figure 2-2. Mounting Clearances (Inches)

2.3.2 POWER REQUIREMENTS

The iSBX 217B board requires +5VDC @ 1.5A. Power is supplied by the host iSBC board, through the iSBX connector.

2.3.3 COOLING REQUIREMENTS

Sufficient cooling should be supplied to prevent a temperature rise above 55'C in the cardcage.

2.3.4 GENERAL SYSTEM REQUIREMENTS

A user-provided program, running on the host board, must be used to handle the command, status, and data exchange between the iSBX 217B board and the host board. Host boards without DMA capability must use a programmed I/O routine to read/write commands and data to/from the iSBX 217B board. A host board that supports direct memory access (DMA) operations can use either the DMA mode or the programmed I/O mode. Refer to Chapter 3 for specific programming and interfacing information.

The iSBX 217B board can be used on any host iSBC board with an iSBX Multimodule connector. However, in order to use the high-speed, 90-inch per second Archive drive, the host board must have either DMA capability, or be capable of transferring data at 100K bytes/second or faster (an 8 MHz or faster processor). If you are using the cartridge tape drive for hard disk backup or program loading onto a hard disk, then the iSBX 217B board is ideally suited for use on the iSBC 215G Winchester Disk Controller Board.

2.4 JUMPER CONFIGURATIONS

Jumpers are used to define the type of tape drive in use. Table 2-1 and Figure 2-3 summarize the jumper configuration for the Archive drive interface (factory default configuration); Table 2-2 and Figure 2-4 give the jumper configuration for the 3M drive interface.

2.4.1 CONVERSION TO 3M DRIVE INTERFACE

To convert the iSBX 217B board from the default Archive interface, to the 3M interface, follow these steps:

a. Remove all push-on header jumper connectors from the board (do not remove soldered jumpers 94-95 or 70-77).

b. Install the wire-wrap jumpers as outlined in Table 2-2.

Table 2-1. Archive Interface Jumper Configurations

Name	From	To		Comments
RP2-4	E90	E84		Connect RP
OE*	E95	E94	##	Ground OE*
D7	E11	E10		Data bit 7
D6	E13	E34		Data bit 6
D5	E31	E32		Data bit 5
D4	E17	E16		Data bit 4
D3	E67	E52		Data bit 3
D2	E35	E50		Data bit 2
D1	E33	E48		Data bit 1
D0	E72	E71		Data bit 0
RDCLK	E77	E70	##	Connect strobe to RDCLK
OUT0*	E39	E54		Connect OUT0* to ONLINE*
OUT1*	E73	E66		Connect OUT1* to REQ*
RESET*	E46	E61		Connect RESET*
XFER*	E57	E58		Connect XFER*
ACK0*	E60	E45		Connect ACK0* to ACK*
IN0*	E40	E41		Connect IN0* to RDY*
IN1*	E26	E27		Connect IN1* to EXCEPTION*
ACK1*	E83	E76		Connect ACK1* to OUT3*
Chassis GND	E8	E29		Connect Signal GND to Chassis GND

Notes: Jumper connections are made with push-on headers, except as noted with ##; ## = soldered jumpers.

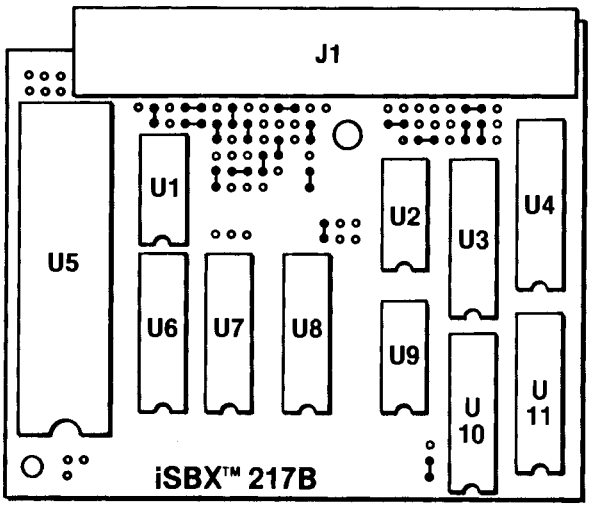

Figure 2-3. Archive Jumper Configuration

Table 2-2. 3M Interface Jumper Configurations

Name	From	To		Comments
D7	E11	E12		Connect D7 to low byte;
	E65	E50		high byte
D6	E14	E13		Connect D6 to low byte;
	E63	E48		high byte
D5	E31	E30		Connect D5 to low byte;
	E64	E71		high byte
D4	E38	E17		Connect D4 to low byte;
	E54	E53		high byte
D3	E10	E9		Connect D3 to low byte;
	E66	E67		high byte
D2	E34	E35		Connect D2 to low byte;
	E19	E18		high byte
D1	E32	E33		Connect D1 to low byte;
	E79	E80		high byte
D0	E16	E15		Connect D0 to low byte;
	E74	E72	#	high byte
RESET	E8	E7		Connect RESET* to INIT*
PAL12*	E52	E2	#	Connect U10-7 to Byte 2
	E24	E37	#	Connect U10-13 to PAL12*
PAL19*	E28	E56	#	Connect PAL 19* to U10-11
	E1	E41	#	Connect U10-9 to Byte 1
XFER*-P2	E3	E6		Connect XFER* to P2
OUT0*	E21	E39	#	Connect OUT0* to RDY
OUT1*	E25	E44		Connect OUT1* to C/D
W/$\overline{R}$	E47	E62		Connect W/$\overline{R}$ to I/O
XFER*	E23	E22		Connect XFER* to ACK
ACK0*	E60	E43	#	Connect ACK0* to REQ
ACK1*	E83	E76		Connect ACK1* to OUT3*
IN1*	E26	E43	#	Connect IN1* to REQ
IN0*	E36	E49	#	Connect IN0* to ATN
RDCLK*	E77	E70	##	Connect Strobe to RDCLK*
OE*	E95	E94	##	Connect OE*

Notes: Jumper connections are made with push-on headers, except as noted.
= Wire jumpers; ## = Soldered jumpers.

c. Insert the push-on jumpers as shown in Figure 2-4 and Table 2-2.

d. Remove resistor pack RN3 on the 3M drive. This prevents overloading the iSBX 217B data bus lines. Refer to the 3M drive manual for exact location of component.

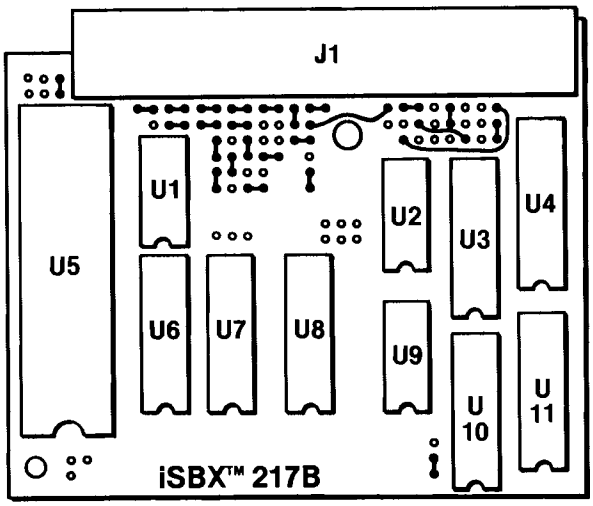

Figure 2-4. 3M Jumper Configuration

2.5 CABLE AND CONNECTOR INFORMATION

Edge connector J1 is used to connect the tape drive to the iSBX 217B board. This connector is a 3M Company 50-pin, right angle header, part number 3433. It mates to the 3M Company connector, part number 3425. Equivalent mating connectors from other vendors are available. Maximum cable length from the board to the drive is 3 meters (10 feet). A daisy chain cable must be used for multiple drives (up to four drives).

2.6 CONNECTOR J1 PIN IDENTIFICATION

This section provides a pin-out diagram and gives signal definitions for connector J1. The signals present on the J1 pins depend on the jumper configuration of the iSBX 217B board. Table 2-3 provides pin/signal names; Table 2-4 provides signal definitions, when the board is configured for the Archive interface; Table 2-5 provides signal definitions for the 3M interface.

NOTE

In the 3M configuration, ensure that pin 1 of board connector is connected to pin 50 of the drive cable. See Table 2-3.

CAUTION

Remove resistor pack RN3 on the 3M drive. This prevents overloading the iSBX 217B data bus lines. Refer to the 3M drive manual for exact location of component.

Table 2-3. Connector J1 Pin Assignments

Archive Pin	Archive Function	3M Pin	3M Function	Archive Pin	Archive Function	3M Pin	3M Function
1	GND	50	RESET	2	NC	49	IN0*
3	OPEN	48	OPEN	4	NC	47	D7 LOW
5	OPEN	46	OPEN	6	NC	45	D6 LOW
7	OPEN	44	OPEN	8	NC	43	D5 LOW
9	GND	42	GND	10	NC	41	D4 LOW
11	GND	40	GND	12	D7	39	D3 LOW
13	GND	38	GND	14	D6	37	D2 LOW
15	GND	36	GND	16	D5	35	D1 LOW
17	GND	34	GND	18	D4	33	D0 LOW
19	GND	32	GND	20	D3	31	PAL12
21	GND	30	GND	22	D2	29	D7 HIGH
23	GND	28	GND	24	D1	27	D6 HIGH
25	GND	26	GND	26	D0	25	D5 HIGH
27	GND	24	GND	28	OUT0*	23	D4 HIGH
29	GND	22	GND	30	OUT1*	21	D3 HIGH
31	GND	20	GND	32	RESET*	19	D2 HIGH
33	GND	18	GND	34	XFER*	17	D1 HIGH
35	GND	16	GND	36	ACK0*	15	D0 HIGH
37	GND	14	GND	38	IN0*	13	PAL19
39	GND	12	GND	40	IN1*	11	NC
41	GND	10	GND	42	NC	9	OUT0*
43	GND	8	GND	44	NC	7	OUT1*
45	GND	6	GND	46	NC	5	W/$\overline{R}$
47	GND	4	GND	48	NC	3	XFER*
49	GND	2	GND	50	NC	1	ACK0* and IN1*

Notes: Archive = Default configuration; NC = not connected; * = active low.

Table 2-4. Connector J1 Signal Definitions - Archive Configuration

HB0-HB7:	Bi-directional data bus. (D0-D7) HB0 is the least significant bit.
ONL:	Online (OUT0*) - iSBX 217B board generated control signal which is activated prior to transferring a Read and Write command.
REQ:	Request (OUT1*) - iSBX 217B board generated control signal which indicates that command data has been placed on the data bus in command mode or that status has been taken from the data bus in status mode.
XFER:	Transfer (XFER*) - iSBX 217B board generated control signal which indicates that data has been placed on the data bus in write mode or that data has been taken from the data bus in read mode.
ACK:	Acknowledge (ACK0*) - drive generated signal which indicates that data has been taken from the data bus in Write Mode or that data has been placed on the data bus in Read Mode.
RDY:	Ready (IN0*) - drive generated signal which indicates the following: 1) If no operation is in progress, RDY means ready to accept a command. 2) Data has been taken from the data bus in command mode. 3) Data has been placed on the data bus in status mode. 4) A buffer is ready to be filled by the host in write mode. 5) A buffer is ready to be emptied by the host in read mode. 6) A position command has been completed in position mode. 7) At the conclusion of a write file mark.
EXC:	Exception (IN1*) - drive generated signal which indicates that an error condition occurred during a file mark cycle or on reset.
RES:	Reset (RESET*) - iSBX 217B board generated signal that causes the drive to perform a power-on sequence

Note: Archive signal names shown in leftmost column; iSBX 217B signal names are shown in parenthesis.

Table 2-5. Connector J1 Signal Definitions - 3M Configuration

D0 - D7:	Data Input Bus/Data Output Bus: 16 lines for the bi-directional 3M bus. The two buses are tied together and, along with the byte 1 and byte 2 control signals, allow the 8-bit directional iSBX 217B board to control the HCD-75 tape drive.
C/D:	Command/Data (OUT1*) - a iSBX 217B board generated signal that is used to indicate (to the drive) whether information on the bus is a command to be executed or data to be written. Set high to indicate a command and low for a data transfer.
I/O:	Input/Output ($W/\overline{R}$) - a iSBX 217B board generated signal that is used to control the direction of transfers between the iSBX 217B board and the drive. Set high for direction flow to the drive and low for direction flow to the iSBX 217B board.
RDY:	Ready (OUT0*) - a iSBX 217B board generated signal that is set low when the iSBX 217B board is initiating a command, data, or status transfer.
INIT:	Initialize (RESET*) - a iSBX 217B board generated signal that, when pulsed high, resets the drive and puts the drive in a ready state.
ATN:	Attention (IN0*) - a drive generated signal which is set high to indicate an attention condition to read the drive status.
REQ:	Transfer Request (ACK0* and IN1*) - an input to the iSBX 217B board that is set low (by the drive) when the drive is ready to accept data during write operations or when data becomes valid during read operations.
ACK:	Transfer Acknowledge (XFER*) - an output from the iSBX 217B board that strobes high when valid data is on the bus during a write operation or when the host has read a byte of data during a read operation.
BYTE1:	Byte 1 Control (PAL19*) - an output from the iSBX 217B board that strobes the low byte of the drive 16-bit bus.
BYTE2:	Byte 2 Control (PAL12*) - an output from the iSBX 217B board that strobes the high byte of the drive 16-bit bus.

Note: 3M drive signals are shown in leftmost column; iSBX 217B signal names are shown in parenthesis.

2.7 iSBX™ MULTIMODULE™ CONNECTOR

Pin assignments for connector P1 (iSBX Multimodule) are listed in Table 2-6. Signals which end with a slash (/) or asterisk (*) are active-low TTL signals; signals without a slash or asterisk are active-high.

CAUTION

Ensure that MINTR1 (pin 12) is not connected on the host board.

Table 2-6. iSBX™ Bus Connector Pin Assignments

Pin	Mnemonic		Description	Pin	Mnemonic		Description
1	+12V	#	+12 Volts	2	-12V	#	-12 Volts
3	GND		Signal Ground	4	+5V		+5 Volts
5	RESET		Reset	6	MCLK		M Clock
7	MA2	#	M Address 2	8	MPST*		iSBX Bd Present
9	MA1	#	M Address 1	10	--		Reserved
11	MA0		M Address 0	12	MINTR1	#	M Interrupt 1
13	IOWRT*		IO Write Cmd	14	MINTR0		M Interrupt 0
15	IORD*		IO Read Cmd	16	MWAIT*		M Wait
17	GND		Signal Ground	18	+5V		+5 Volts
19	MD7		M Data Bit 7	20	MCS1*		M Chip Select 1
21	MD6		M Data Bit 6	22	MCS0*		M Chip Select 0
23	MD5		M Data Bit 5	24	--		Reserved
25	MD4		M Data Bit 4	26	--		Reserved
27	MD3		M Data Bit 3	28	OPT0		Option 0
29	MD2		M Data Bit 2	30	OPT1		Option 1
31	MD1		M Data Bit 1	32	--		Reserved
33	MD0		M Data Bit 0	34	--		Reserved
35	GND		Signal Ground	36	+5V		+5 Volts

Note: # = not used by iSBX 217B board.

2.8 INSTALLATION PROCEDURE

The iSBX 217B board can be easily installed without special equipment or tools. The following procedure outlines iSBX 217B board installation:

CAUTION

Host iSBC board must be removed from chassis or cardcage for proper installation of the iSBX 217B board. Turn off power before removal.

a. Some iSBC Single Board Computers have up to three iSBX Multimodule connectors. Choose the connector location which corresponds to the host I/O addressing you select. Avoid using the rightmost iSBX connector if possible; the iSBX 217B board J1 connector latch may not open correctly with some cardcage models.

   Refer to Table 3-4 or to the host board hardware reference manual for the I/O address identification.

b. Install the supplied threaded spacer on the solder side of the Multimodule Board (at the hole near connector J1). Secure the spacer by hand- tightening one of the supplied 1/4-inch screws through the component side of the iSBX 217B board (refer to Figure 2-5).

c. Locate pin 1 on the host iSBX connector. Similarly, locate pin 1 on the iSBX 217B board iSBX connector. Refer to Figure 2-6.

d. Carefully match the connectors at pin 1 and insert the iSBX 217B board into the host board iSBX connector until it is fully inserted and correctly seated. The iSBX 217B board J1 connector should be oriented in the same direction as the host board's I/O connectors.

e. Push the remaining 1/4-inch screw up through the bottom of the host board and thread it into the spacer.

f. Tighten down both screws as shown in Figure 2-5.

g. Refer to Section 2.4 for jumper connection information. If jumper connections are not required, install the host board back into its chassis.

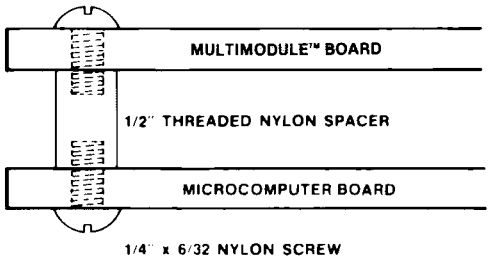

Figure 2-5. Mounting Technique

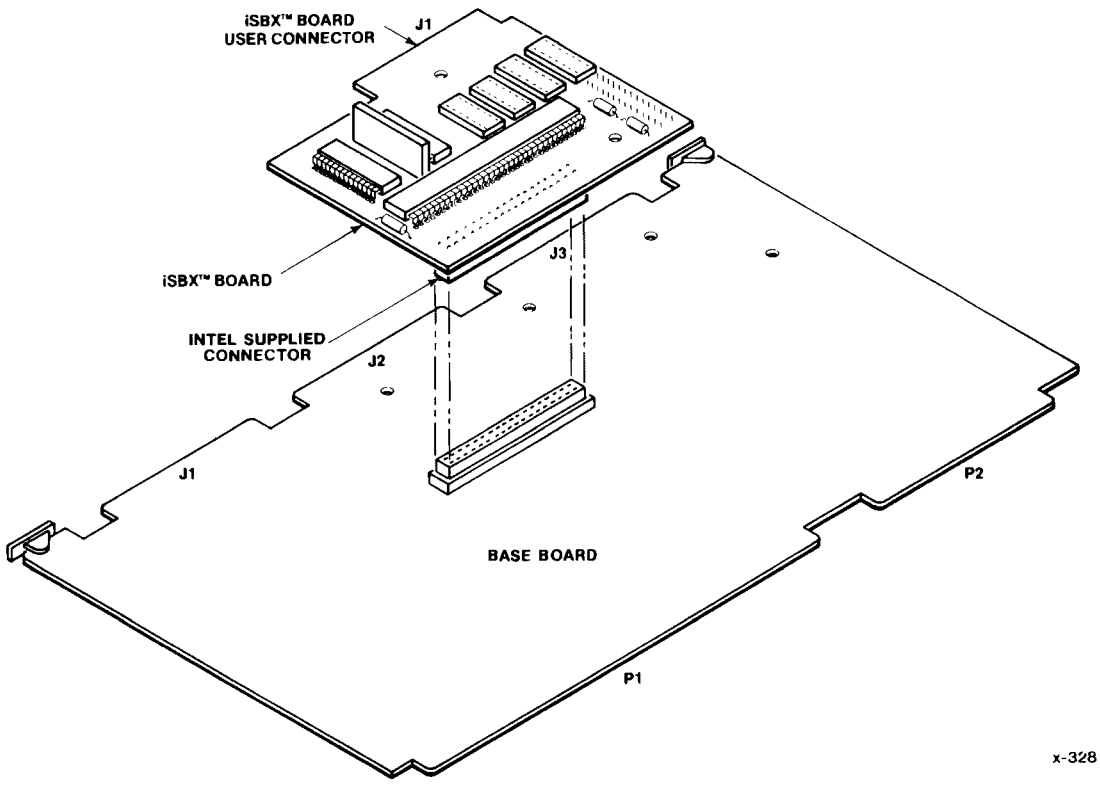

Figure 2-6. iSBX™ Board Installation

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CHAPTER 3. INTERFACING AND PROGRAMMING INFORMATION

3.1 INTRODUCTION

This chapter provides interfacing information and programming information for the iSBX 217B board. This information includes I/O addressing information, initialization information, command and command parameter instructions, host software requirements, and example flowcharts.

Throughout this chapter, abbreviations or mnemonics are used when referencing certain commands, status conditions, or common computer terms. The following table gives a brief definition of these abbreviations:

Mnemonic	Meaning In This Chapter
DMA:	Direct Memory Access.
EOT:	End Of Transfer (command).
IBF:	Input Buffer Full (status condition of UPI).
I/O:	Input/Output; here refers to mode of transfer.
OBF:	Output Buffer Full (status condition of UPI).
SOD:	Drive Ready (status of tape drive).
SOT:	Start Of Transfer (command).
UPI:	Universal Peripheral Interface (8741 microcomputer).
XFER:	Transfer (operation).

3.2 GENERAL OPERATION

There are four different operating modes in which the host and the iSBX 217B board communicate to transfer data to or from the tape drive:

a. Direct memory access (DMA) mode with Archive drive;

b. Programmed I/O mode with Archive drive;

c. DMA mode with 3M drive; and

d. Programmed I/O mode with 3M drive.

The difference between DMA and programmed I/O is illustrated by the behavior of the host board during the transfer. In general the DMA mode requires that the host transfer a byte of data when the iSBX 217B board makes a DMA request. In the programmed I/O mode the host board polls a bit in the UPI (microcomputer on the iSBX 217B board) status register. When this bit becomes true the data can be transferred. Detailed

descriptions of the modes are in the following sections: Archive DMA, Section 3.5.1; Archive programmed I/O, Section 3.5.2; 3M DMA, Section 3.5.3; and 3M programmed I/O, Section 3.5.4.

A summary of commands is given Section 3.3. Following the introduction to the commands, Sections 3.3.1 and 3.3.2 discuss the protocol for issuing commands. System operation is discussed in Section 3.5. Detailed descriptions of the commands are listed in Section 3.6.

3.3 COMMAND IMPLEMENTATION

A command must be given to the iSBX 217B board to initiate every function. Every command must be completed, i.e., the sense status bytes must be read (see Section 3.7), before a new command can be given. After a command is sent to the iSBX 217B board, the host may either poll the output buffer full (OBF) bit of the UPI, or be interrupted by Multimodule interrupt 0 (MINTR0) to signify the end of the function, before reading the sense status bytes.

All commands are followed by at least one parameter byte. Some of the commands can be used by both drive types; however, other commands are unique to one drive type only.

The iSBX 217B board utilizes three types of commands (see Table 3-1):

a. Simple Commands. These are commands which the host issues, and the iSBX 217B board executes the command and returns the status of the drive. Once the host issues a simple command, no further action is required except to receive the status. The receive status function includes waiting for the requested function to complete.

b. Data Transfer Commands. These commands cause data to be transferred to or from the tape. In this type of command the host issues the data transfer command, issues a special purpose command, transfers the data, issues a special purpose command, and receives the status. The data transfer command is not complete until the host receives the status.

c. Special Purpose Commands. These commands are used to synchronize the host and the iSBX 217B board during data transfers. The special purpose commands do not return any status. A special purpose command can be issued ONLY during the execution of a data transfer command.

Table 3-1 summarizes the complete command set. This table shows the hexadecimal code for the particular command, indicates the type of command (simple, data transfer, or special purpose), and indicates the number of parameter bytes required by the command.

The host issues commands to the iSBX 217B board by writing to specific host board I/O ports. In turn, the host reads UPI status and drive status through the same ports. Data is read or written through another set of ports. Addressing is described in more detail in Section 3.4.

Table 3-1. Command Set Summary

Hex Code	Command	Parameters Archive	Parameters 3M	Type Of CMD
00	RESET iSBX 217B BOARD	1	1	a
01	INITIALIZE DRIVE	1	1	a
02	WRITE A BLOCK	1	3	b
03	WRITE A FILE MARK	1	1	a
04	READ A BLOCK	1	3	b
05	SPACE FORWARD ONE FILE	1	N	a
06	READ STATUS	1	1	a
07	REWIND	1	N	a
08	RETENSION	1	N	a
09	ERASE TAPE	1	N	a
0C	UNLOAD TAPE	N	1	a
14	CONTINUE	N	1	a
15	WRITE RAM	N	5	b
16	READ RAM	N	5	b
17	VERIFY	N	5	a
40	START OF TRANSFER (SOT)	1	1	c
80	END OF TRANSFER (EOT)	1	1	c

Note: N = invalid command for drive; see text.

3.3.1 PROTOCOL FOR ISSUING COMMANDS

The protocol for issuing commands from the host board to the iSBX 217B board is as follows:

1. Wait for IBF to be 0.
2. Send command to iSBX 217B port.
3. Wait for IBF to be 0.
4. Send 1st parameter to parameter port.
5. Wait for IBF if second parameter is required.
6. Send next parameter, if required (3M only).
7. Repeat steps 5 and 6 for remaining parameters (3M only).

Anytime the host board waits for IBF to be 0 it must also be able to detect the end of a function, either by MINTR0 or by polling OBF. If the end of the transfer is detected then the host board should skip the rest of the issuing command protocol and go on and receive the status.

3.3.2 PROTOCOL FOR RECEIVING STATUS

The protocol for receiving status from the iSBX 217B board is as follows:

1. Wait for OBF to be 1.
2. Read sense byte 0.
3. Repeat steps 1 and 2 for the number of sense status bytes indicated in sense byte 0 (see Section 3.7).

3.4 I/O ADDRESSING

I/O port addresses vary with the particular host board in use. Table 3-2 summarizes the iSBX I/O port addresses for various host boards. To select Base 0 addresses, the signal MCS0* must be true; to select Base 1 addresses, MCS1* must be true.

The host board iSBX board connector determines the range of addresses which must be used for host/iSBX dialog. Table 3-3 summarizes iSBX 217B command, data, and status addressing.

3.5 OPERATION

The host communicates with the iSBX 217B in five basic ways to send commands, read or write data, and to check status. These ways are summarized as follows:

1. Host issues a simple command.
2. Programmed I/O read transfers.
3. Programmed I/O write transfers.
4. DMA read transfers.
5. DMA write transfers.

These five methods of operation are discussed in the following paragraphs. Notice that except for simple commands, the methods for the Archive drive are somewhat different than the methods for the 3M drive.

In a few remote cases, a breakdown in host-to-drive communication may develop, due to tape drive anomalies. Refer to Appendix A for a discussion of these drive anomalies.

Table 3-2. iSBC® Board Connector Port Assignments For iSBX™ Boards

Board	DMA	SBX Conn	CMD FUNCT/ UPI Status	CMD PARAM/ Drive Status	Data
iSBC® 215G	Yes	J3	C072/6/A/E	C070/4/8/C	C0B0 - C0BE*
		J4	C0D2/6/A/E	C0D0/4/8/C	C0E0 - C0EE*
iSBC® 589	Yes	J2	FF82/6/A/E	FF80/4/8/C	FF90 - FF9F*
		J3	FFA2/6/A/E	FFA0/4/8/C	FFB0 - FFBF*
iSBC® 208	Yes	J3	21/3/5/7	20/2/4/6	28 - 2F
iSBC® 88/45	Yes	J4	C1/3/5/7	C0/2/4/6	C8 - CF
		J5	F1/3/5/7	F0/2/4/6	F8 - FF
iSBC® 80/10B	No	J4	F1/3/5/7	F0/2/4/6	F8 - FF
iSBC® 80/16	No	J4	C1/3/5/7	C0/2/4/6	C8 - CF
		J5	F1/3/5/7	F0/2/4/6	F8 - FF
iSBC® 80/24	No	J5	C1/3/5/7	C0/2/4/6	C8 - CF
		J6	F1/3/5/7	F0/2/4/6	F8 - FF
iSBC® 88/40	No	J4	81/3/5/7	80/2/4/6	90 - 9F*
		J5	A1/3/5/7	A0/2/4/6	B0 - BF*
		J6	61/3/5/7	60/2/4/6	70 - 7F*
iSBC® 88/25	No	J3	81/3/5/7	80/2/4/6	90 - 9F*
		J4	A1/3/5/7	A0/2/4/6	B0 - BF*
iSBC® 86/05	No	J3	A2/6/A/E	A0/4/8/C	B0 - BF*
		J4	82/6/A/E	80/4/8/C	90 - 9F*
iSBC® 86/30	No	J3	A2/6/A/E	A0/4/8/C	B0 - BF*
		J4	82/6/A/E	80/4/8/C	90 - 9F*

Note: * = Use EVEN addresses only for DATA column (i.e., B0, B2, B4, B6, etc.);.

All address are shown in hexadecimal. For CMD FUNCT and CMD PARAM, the addresses shown perform the same function. For example, on the iSBC 86/30 board using J4, reading or writing to port 80 is equivalent to reading or writing to port 84, 88, or 8C. For data transfers, any address in the range performs the data operation.

Table 3-3. iSBX™ 217B Board I/O Port Addressing

iSBX™ 217B Port Address	Port Function
Base 0 @ 0, 2, 4, 6 (8-bit host) or 0, 4, 8, C (16-bit host)	Write command parameter or read drive status
Base 0 @ 1, 3, 5, 7 (8-bit host) or 2, 6, A, E (16-bit host)	Write command function or read UPI status
Base 1 @ 0 through 7 (8-bit host) or 0 through F EVEN only (16-bit host)	Write or read data

Simple Commands

In this form of operation the command and parameters are sent to the UPI and then the status is returned. The host must be able to detect the end of the operation at anytime. The sequence for a simple command is:

1. Send simple command and its parameters to UPI.
2. Receive status.

The following four sections describe how to use the iSBX 217B board with each drive type. Both methods of transfer (DMA and Programmed I/O) are given. Figure 3-1A is a flowchart of a simple command. Figure 3-1B shows the recommended sequence for issuing the command byte. Figure 3-1C shows the sequence for issuing a parameter byte. Figure 3-2A shows a data transfer operation, and Figure 3-2B shows the method of reading the returned status sense bytes.

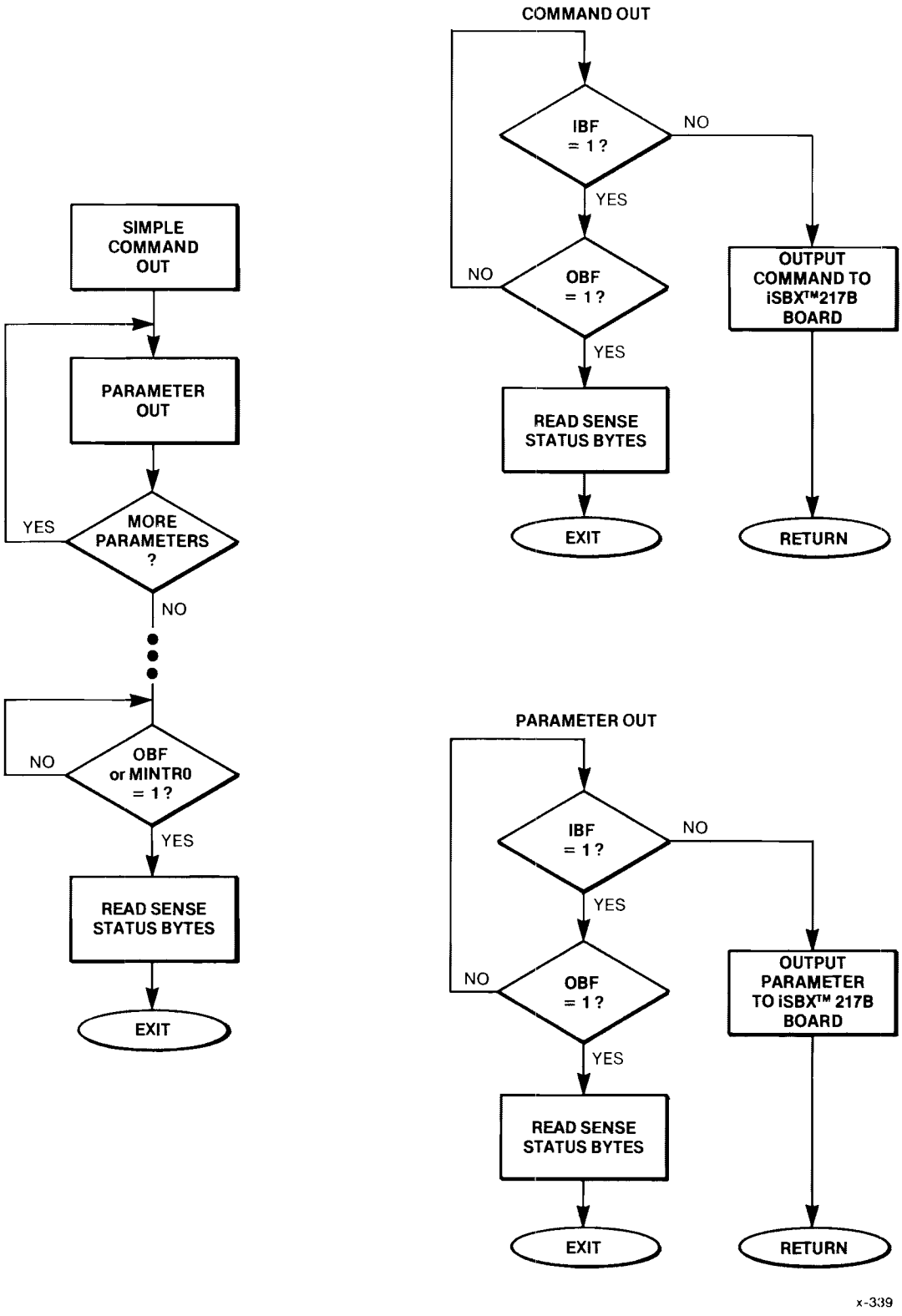


Figure 3-1. Example Flowcharts

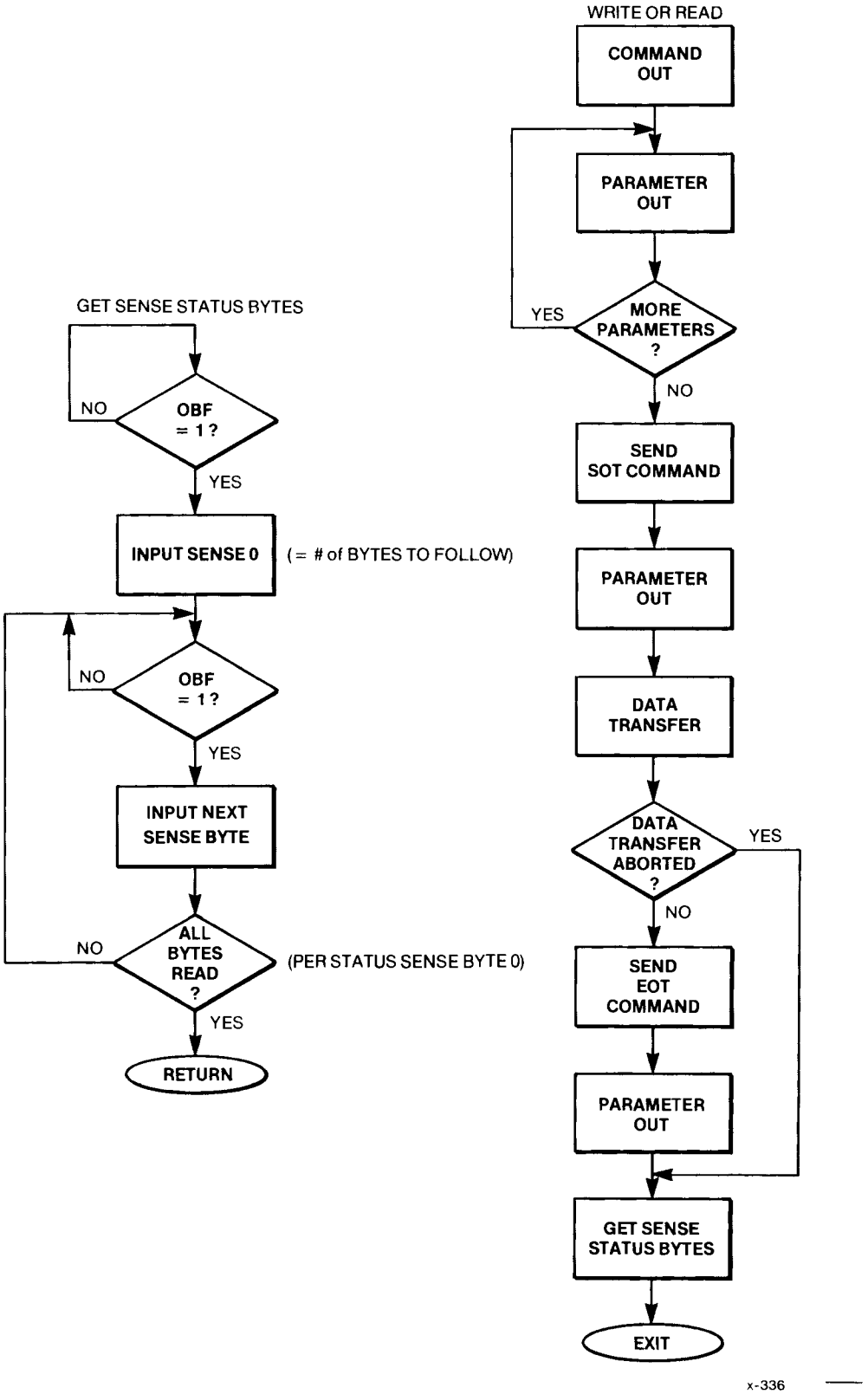


Figure 3-2. Example Flowcharts

3.5.1 ARCHIVE DRIVE USING DMA MODE

Hosts that use Direct Memory Access (DMA) capability must use DMA request (DMRQT) to synchronize data transfer. However, the use of DMA acknowledge (MDACK*) is optional. For example, the iSBC 215G Winchester Disk Drive Controller board performs data transfer with no DMA acknowledge because in reality the iSBC 215G board executes a programmed I/O transfer with the iSBX 217B board while performing DMA transfers over the Multibus system. Additionally, the DMA hardware must have the capability for an external termination (TDMA) so that in the event the drive has experienced an unrecoverable error, the iSBX 217B board can terminate operation.

The host should examine the DMA byte count register after completion of the transfer. If the full byte count has not been transferred, the drive terminated the operation and the host should examine the sense status bytes for any hard errors. Figure 3-3 shows a timing diagram of a DMA transfer with external termination caused by a hard data error.

The following procedure gives the DMA READ data transfer operation:

1. Send a read command to the UPI.
2. Set up DMA hardware and enable.
3. Send a SOT command to the UPI.
4. Transfer the data.
5. Send an EOT command to the UPI.
6. Receive sense status bytes from the UPI.

The following procedure gives the DMA WRITE data transfer operation:

1. Send a write command to the UPI.
2. Set up DMA hardware and enable.
3. Send a SOT command to the UPI.
4. Transfer the data.
5. Send an EOT command to the UPI.
6. Receive sense status bytes from UPI.

At anytime during either sequence the host board must be able to perceive the end of the operation. If the end to the operation is perceived before the host board has reached step 6, the host should go directly to step 6. DMA enable can be delayed until the end of sending the SOT command. However DMA must be enabled when the SOT command parameter is sent to the iSBX 217B board.

For hosts which have an 8089 controller (such as the iSBC 215G board) the code should be similar to the following:

```
SEND WRITE COMMAND
SET UP
WAIT FOR IBF
SEND SOT COMMAND
WAIT FOR IBF
XFER                        ;ENABLE DMA
MOVBI 217B, PARAMETER       ;SEND SOT PARAMETER
```

Notice that the actual data transfer in this mode does not begin until after the iSBX 217B board receives the SOT parameter.

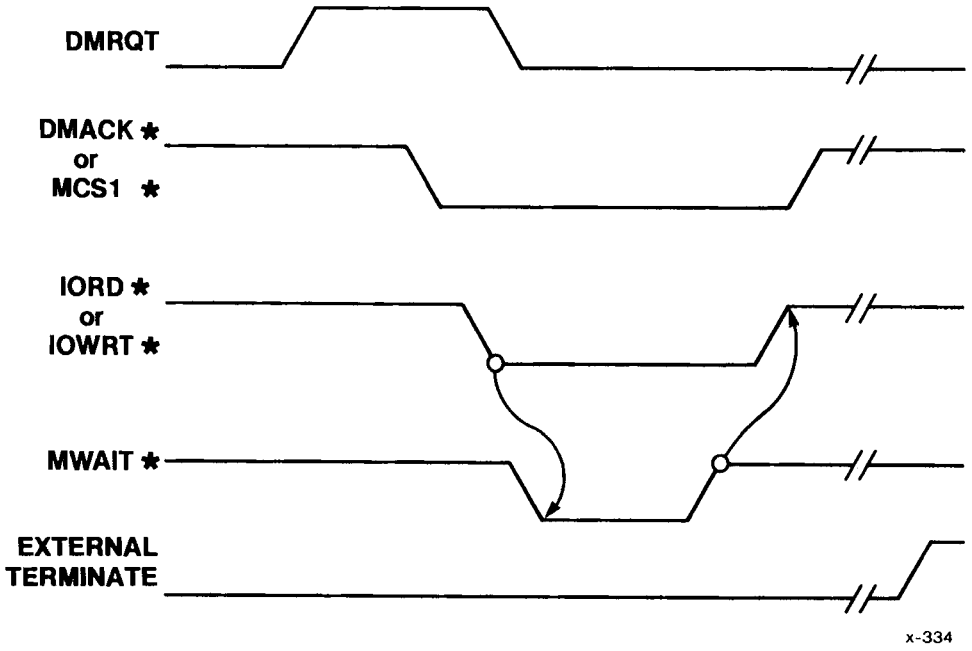


Figure 3-3. DMA Data Transfer Timing Diagram

3.5.2 ARCHIVE DRIVE USING PROGRAMMED I/O MODE

For programmed I/O transfers, the host board must support the MWAIT* line on the iSBX bus. As soon as the host has given the command sequence to the iSBX 217B board, the data transfer for a read or write function can begin.

The host board must employ a high-speed programmed I/O loop, with the loop speed controlled by MWAIT*. Figure 3-4 depicts the sequence of events. For a read or write operation, when the host board accesses (Base 1), MWAIT* will go active if either the next data byte is not available for a read operation or if the drive is not ready to receive a byte for a write operation. As long as MWAIT* is active, the host board executes wait states. When the drive is ready for data, MWAIT* becomes inactive thereby permitting instruction execution to continue. Figure 3-5 is a timing diagram of this sequence.

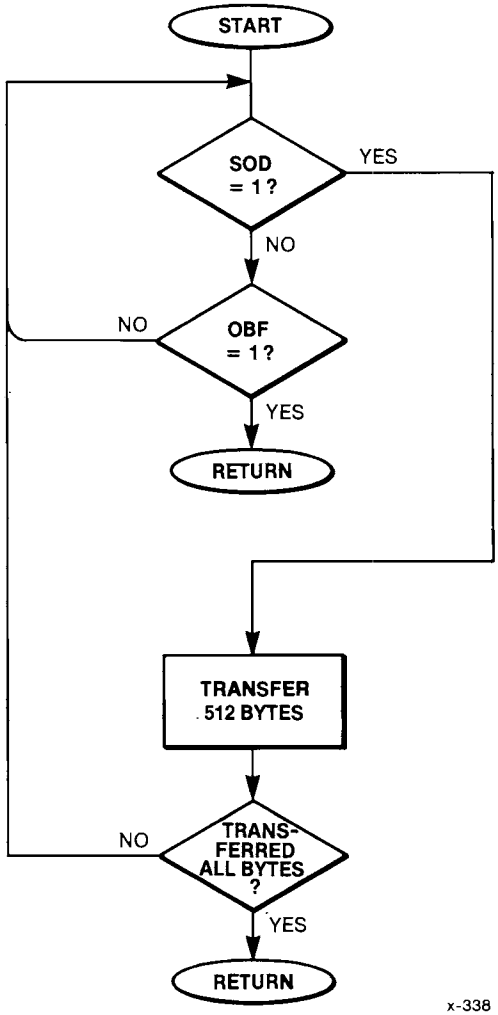


Figure 3-4. Archive Drive Programmed I/O Simplified Flow

In the event that a hard error prevents function completion, the iSBX 217B board sets OBF notifying the host that an error exists. The host board should then poll OBF and read the drive sense status bytes (see Section 3.7) to determine the type of error.

The host is required to transfer the data to and from the Archive drive at a rate greater than 100K bytes/sec, or 30K bytes/sec, depending on the drive speed.

For the Archive interface at 90 ips operation, the host must read/write a byte to the drive every 11 microseconds or less. To attain that speed, the program loop should transfer data as fast as possible by synchronizing the iSBX transfers with MWAIT*.

Since the Archive drive has three 512 byte FIFO (first-in-first-out) buffers, the drive will always transfer data in blocks of 512 bytes. Therefore, it is the responsibility of the host to stop after every 512 data bytes are transferred and wait until another buffer is ready to be serviced.

The mechanism for checking for a buffer ready is for the host to poll the UPI status port. The bit definitions for the status port are as follows:

MSB	7	6	5	4	3	2	1	0	LSB

B0: Output Buffer Full (OBF) - set to a logical one when the UPI writes to the data bus buffer. This bit is cleared when the host processor reads the data bus buffer.

B1: Input Buffer Full (IBF) - when a logical one, indicates the host has written a byte to the data bus buffer, and that the iSBX 217B board has not emptied the buffer.

B2-B6: Bits 2 through bits 6 are reserved.

B7: Buffer Ready (SOD) - when using an Archive interface with programmed I/O Control, this bit when = logical 1 tells the host that another 512 byte data block is ready to be transferred. The host should poll this bit for every block of data transferred.

If an unrecoverable error occurs, the iSBX 217B board sets MINTRO active, and the host should poll OBF and read the sense status bytes until all are read.

If the host board does not support MINTRO, the software can poll OBF and SOD at the data block boundary. If OBF = 1, this indicates (to the host) that the transfer was aborted and that the status sense bytes are ready to be read.

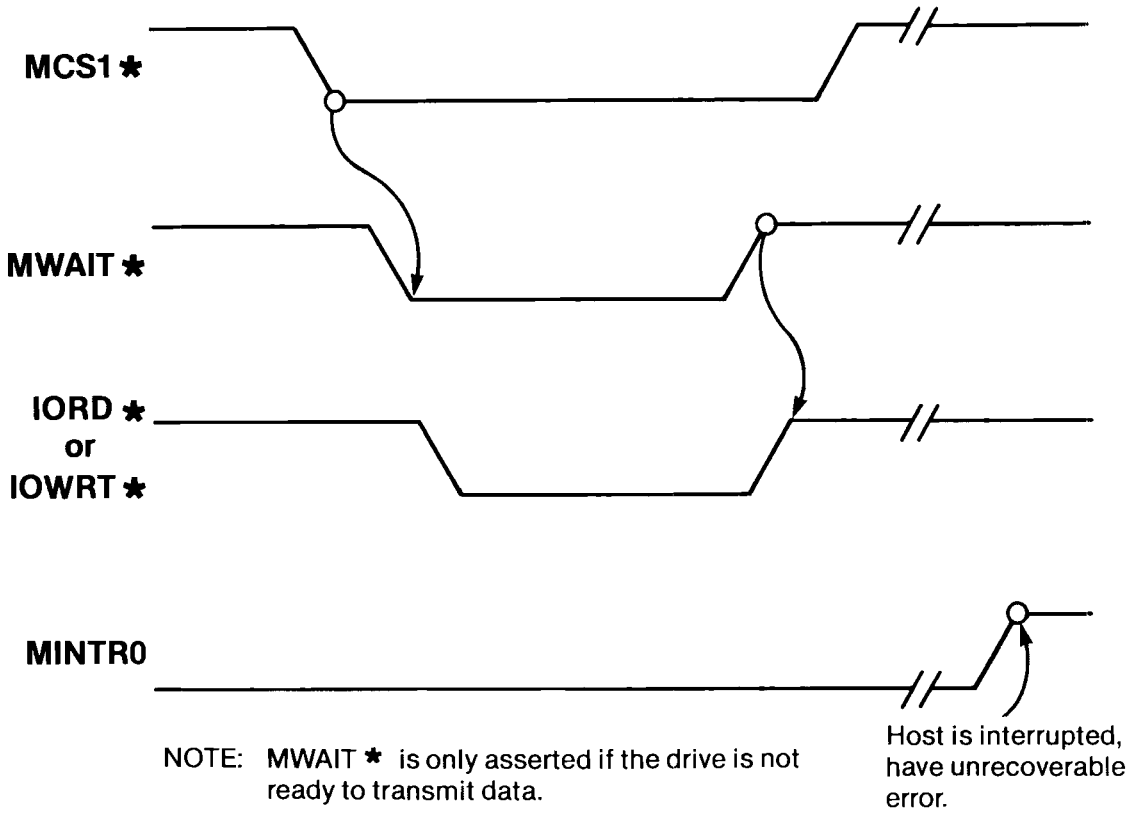


Figure 3-5. Programmed I/O Transfer Timing Diagram

The reason the buffer ready must be polled every 512 bytes, is that letting the host run free could cause MWAIT* to be active for seconds, which could seriously degrade system performance and because most processor boards that produce a timeout interrupt when the wait line is active too long.

The following paragraphs summarize the procedure for the Archive drive. Remember that all Archive drive data transfers must be in multiples of 512 bytes. Figure 3-6 is a detailed flowchart of the Archive drive programmed I/O mode READ operation. Table 3-4 is the corresponding assembly language program for this operation.

Assumes READ command and SOT command have been issued and received; and block count loaded with number of 512 byte blocks and RAM pointer loaded with the starting point of read buffer.

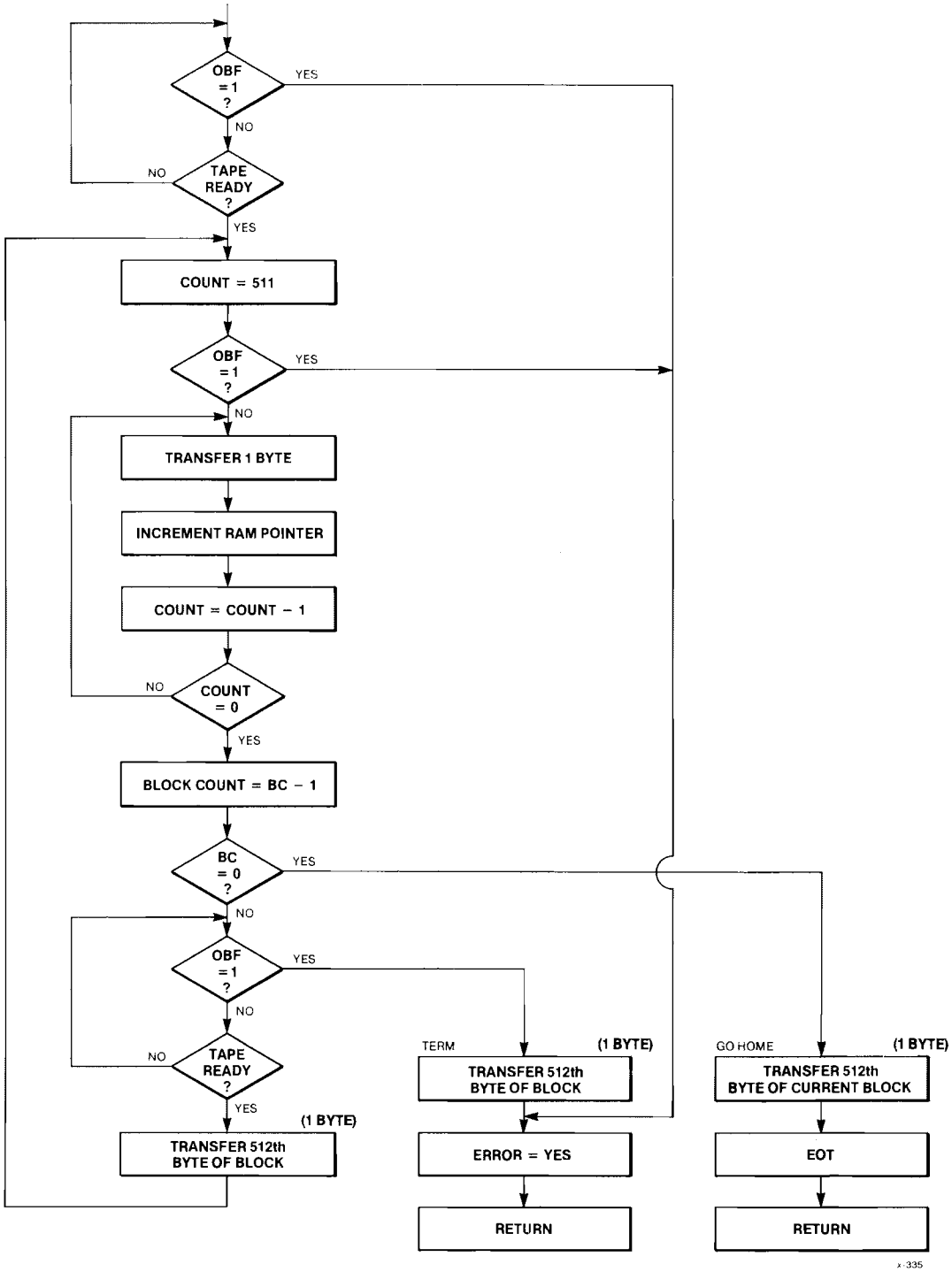


Figure 3-6. Archive Drive Detailed I/O Operation

Table 3-4. Program Example of Archive READ Operation

```
 8      NAME    QUICK_TRANSFER
 9      CGROUP  GROUP   CODE
10
11
12      EXTRN   BLOCKCOUNT:WORD                 ;CONTAINS # OF 512 BYTE BLOCKS
13      EXTRN   BUF_PTR:DWORD                   ;RAM POINTER FOR READ BUFFER
14      EXTRN   EARLY_END:BYTE                  ;INDICATION OF PREMATURE TERMINATE
15
16      PUBLIC  READ_ARCHIVE_IO
17
18      UPI_STATUS      EQU     0C1H            ;UPI-41A STATUS PORT
19      COMMAND_217     EQU     0C1H            ;UPI-41A COMMAND PORT
20      PARAM_217       EQU     0C0H            ;2178 PARAM PORT
21      DATA_217        EQU     0C8H            ;2178 DATA PORT
22      OBF_MASK        EQU     01H
23      IBF_MASK        EQU     02H
24      READY_MASK      EQU     80H             ;TAPE READY BIT MASK
25      END_XFER_217    EQU     80H             ;END XFER COMMAND
26      TRUE            EQU     0FFH            ;BOLEAN CONSTANT
27
28      ASSUME  CS:CGROUP
29      CODE    SEGMENT WORD    PUBLIC  'CODE'


33
34      ;************************ ARCHIVE I/O READ TRANSFER ****************************
35
36      ;XFERS BLOCKCOUNT*512 FROM TAPE TO RAM @ BUF_PTR
37
38      READ_ARCHIVE_IO PROC    NEAR
39      OBFCHK: IN      AL,UPI_STATUS           ;CHECK FOR OBF TERMINATION
40              RCR     AL,1
41              JC      BAIL
42              IN      AL,UPI_STATUS           ;WAIT FOR TAPE READY
43              AND     AL,READY_MASK
44              JZ      OBFCHK
45              LES     SI,DS:BUF_PTR           ;INDEX TO RAM READ BUFFER
46      FRESH:  MOV     CX,511                  ;INNER "LOOP" COUNTER
47              IN      AL,UPI_STATUS           ;CHECK FOR OBF TERMINATION
48              RCR     AL,1
49              JC      BAIL
50      TIGHTR: IN      AL,DATA_217             ;READ FROM TAPE
51              MOV     ES:[SI],AL              ;WRITE TO RAM
52              INC     SI                      ;INCREMENT RAM POINTER
53              LOOP    TIGHTR                  ;DECREMENT CX AND LOOP IF NOT ZERO
54              DEC     DS:BLOCKCOUNT           ;CHECK FOR LAST BLOCK
55              JZ      GOHOME                  ;IF SO GRAB LAST AND GO.
56      READY:  IN      AL,UPI_STATUS           ;CHECK FOR DRIVE EXCEPTION
57              RCR     AL,1
58              JC      TERM                    ;TERMinate IF OBF WHILE WAITING FOR TAPE READ
        Y
59              IN      AL,UPI_STATUS           ;WAIT FOR TAPE READY
60              AND     AL,READY_MASK
61              JZ      READY
62              IN      AL,DATA_217             ;GRAB 512th BYTE AND LOOP
63              MOV     ES:[SI],AL
64              JMP     FRESH
65
66      GOHOME: IN      AL,DATA_217             ;512th OF LAST BLOCK
67              MOV     ES:[SI],AL
68              MOV     AL,END_XFER_217         ;SEND EOT COMMAND
69              OUT     COMMAND_217,AL
70      IBFCHK: IN      AL,UPI_STATUS           ;WAIT FOR IBF=0 BEFORE SENDING PARAM
71              AND     AL,IBF_MASK
72              JNZ     IBFCHK
73              MOV     AL,0
74              OUT     PARAM_217,AL            ;SEND PARAM ASSOCIATED WITH EOT
75              RET
76
77      TERM:   IN      AL,DATA_217             ;ENTREO HERE IF OBF BETWEEN 511 AND 512
78              MOV     ES:[SI],AL
79      BAIL:   MOV     AL,TRUE                 ;BAIL OUT POINT FROM AN EXCEPTION
80              MOV     DS:EARLY_END,AL
81              RET
82      READ_ARCHIVE_IO ENDP
83
84      ;*******************************************************************************
```

3.5.2.1 Archive Drive READ Procedure In Programmed I/O Mode

The host board sequence for performing a READ operation is:

1. Send a READ command TO THE UPI.
2. Send a SOT command to the UPI.
3. Wait for SOD bit in UPI status.
4. Transfer the data. See method below.
5. Send an EOT command to the UPI.
6. Receive status from the UPI.

The method of checking for a buffer ready condition at the 512 byte boundary during a READ operation is as follows:

1. Transfer 511 bytes;
2. If more blocks are to follow, then wait for buffer ready; else go to step 5;
3. Transfer 1 byte;
4. Go to step 1;
5. Transfer 1 byte;
6. Done.

At anytime during this sequence the host board must be able to perceive the end of the operation. If the end to the operation is perceived before the host board has reached step 6, the host should go directly to step 6.

The purpose of the SOD bit is to prevent the host board from executing wait states for long periods of time while the drive searches for the next block. If the host board follows this SOD protocol, and performs the I/O transfer synchronized on DMA request (DMACK), the firmware ensures that the host board does not execute wait states for more than 1 millisecond.

3.5.2.2 Archive Drive WRITE Procedure In Programmed I/O Mode

The host board sequence for performing a WRITE operation is:

1. Send a WRITE command to the UPI.
2. Send a SOT command to the UPI.
3. Wait for SOD bit in UPI status.
4. Transfer the data. See method below.
5. Send an EOT command to the UPI.
6. Receive status from the UPI.

The method of checking for a buffer ready condition at the 512 byte boundary for a WRITE operation is as follows:

1. Transfer 512 bytes;
2. If more blocks are to follow, then wait for buffer ready; else go to step 4;
3. Go to step 1;
4. Done.

At anytime during this sequence the host board must be able to perceive the end of the operation. If the end to the operation is perceived before the host board has reached step 6, the host should go directly to step 6.

3.5.3 3M DRIVE USING DMA

The host board sequence for performing a DMA READ operation is as follows:

1. Send a read command to the UPI.
2. Set up DMA hardware and enable.
3. Send a SOT command to the UPI.
4. Wait for data transfer to complete.
5. Send an EOT command to the UPI.
6. Receive status from the UPI.

The following procedure gives the DMA WRITE data transfer operation:

1. Send a write command to the UPI.
2. Set up DMA hardware and enable.
3. Send a SOT command to the UPI.
4. Wait for data transfer to complete.
5. Send an EOT command to the UPI.
6. Receive status from UPI.

At anytime during either sequence the host board must be able to perceive the end of the operation. If the end to the operation is perceived before the host board has reached step 6, the host should go directly to step 6. DMA enable can be delayed until the end of sending the SOT command. However DMA must be enabled when the SOT command parameter is sent to the iSBX 217B board.

For hosts which have an 8089 controller (such as the iSBC 215G board) the code should be similar to the following:

```
SEND WRITE COMMAND
SET UP
WAIT FOR IBF
SEND SOT COMMAND
WAIT FOR IBF
XFER                        ;ENABLE DMA
MOVBI 217B, PARAMETER       ;SEND SOT PARAMETER
```

Notice that the actual data transfer in this mode does not begin until after the iSBX 217B board receives the SOT parameter.

3.5.4 3M DRIVE USING PROGRAMMED I/O

The programmed I/O sequence is different for the 3M interface because the HCD-75 interface does not indicate when the next buffer is available. However, because the transfer rate of the drive is only 17.5K bytes/second, the data transfer could be interrupt-driven on a byte-by-byte basis using iSBX Option Line 1 tied to an interrupt input.

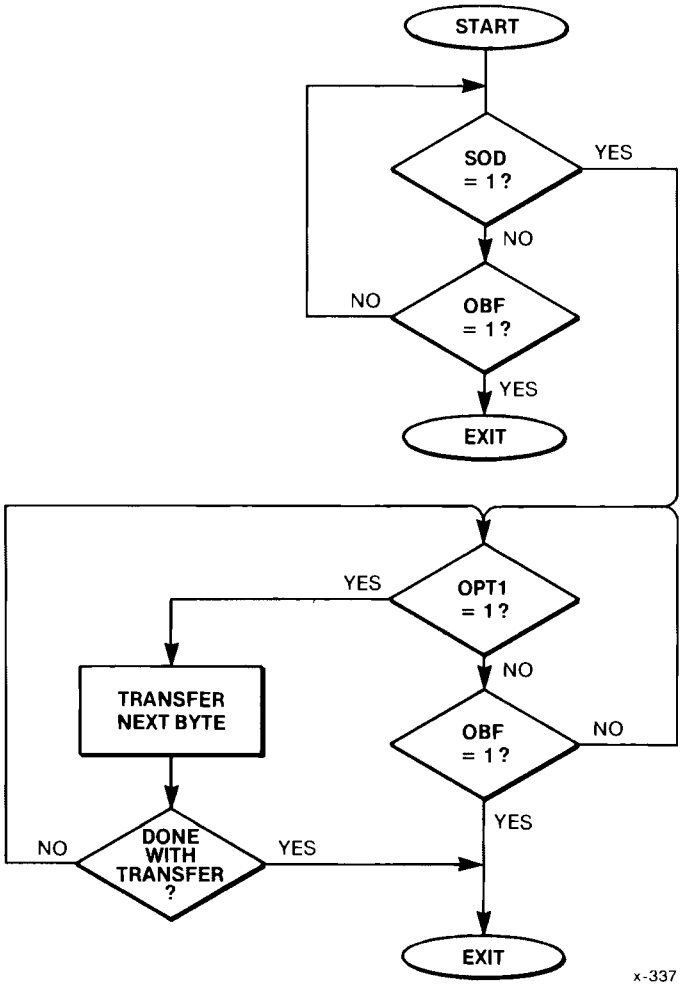


Figure 3-7. 3M Drive Programmed I/O Data Transfer

Alternatively, this line could be connected to the host board's parallel port and polled. Option line 1 is tied to MDRQT (DMA request). When this line is active (high) it indicates that the host can transfer the next data byte to or from the iSBX 217B board.

Another method could be employed by disabling the timeout on the host board, and then synchronizing the transfers with MWAIT.

The buffer ready bit (SOD) is set for the first ready buffer and stays set for the duration of the transfer. The host must not start the transfer until SOD is a 1.

The following procedure summarizes the routines for the 3M drive. All 3M drive data transfers must be in multiples of 2 bytes; this is a restriction placed on the system by the drive. Figure 3-7 is a flowchart of the read/write process on the 3M drive using OPT1 to synchronize data transfers.

The host board sequence for performing a READ operation is:

1. Send a READ command TO THE UPI.
2. Send a SOT command to the UPI.
3. Wait for SOD bit in UPI status.
4. Transfer the data.
5. Send an EOT command to the UPI.
6. Receive status from the UPI.

The host board sequence for performing a WRITE operation is:

1. Send a WRITE command to the UPI.
2. Send a SOT command to the UPI.
3. Wait for SOD bit in UPI status.
4. Transfer the data.
5. Send an EOT command to the UPI.
6. Receive status from the UPI.

At anytime during either a READ or a WRITE operation the host board must be able to perceive the end of the operation. If the end to the operation is perceived before the host board has reached step 6, the host should go directly to step 6.

Note that if the READ programmed I/O operation using MWAIT* terminates before the host has finished transferring the data, the host reads an extra byte. Therefore, the host software must be able to handle this type of termination.

3.6 COMMAND DESCRIPTIONS

All on-board functions are controlled by firmware contained in the UPI device on the iSBX 217B board. The two supported tape drive interfaces (Archive & 3M) do not require an identical number of commands. However, the iSBX 217B board supports all required commands for each drive interface. Table 3-1 summarizes the commands available on the iSBX 217B board. The table indicates whether the interface supports a particular iSBX 217B board command and if so, the table indicates the number of parameter bytes that are required with the command. The hexadecimal value for each command is also shown.

Each command is initiated by writing the specified command code to the UPI command port, followed by at least one parameter byte transferred via the UPI data port.

For every command initiated, the host must read the sense status bytes at the conclusion of that operation. The exceptions are Read, Write, and SOT commands, where the sense status bytes are automatically returned to the host after the End of Transfer command is sent. If the iSBX 217B board terminates the command, the sense status bytes are returned to the host without the EOT command.

The host can either poll the OBF (Output Buffer Full) flag in the UPI status port or the host can be interrupted by MINTRO when the drive sense status bytes require reading by the host. MINTRO stays set until the UPI reads the first sense status byte. The host must poll OBF for the remaining sense status bytes. Every command has at least one parameter byte, called parameter byte 0 (Figure 3-8).

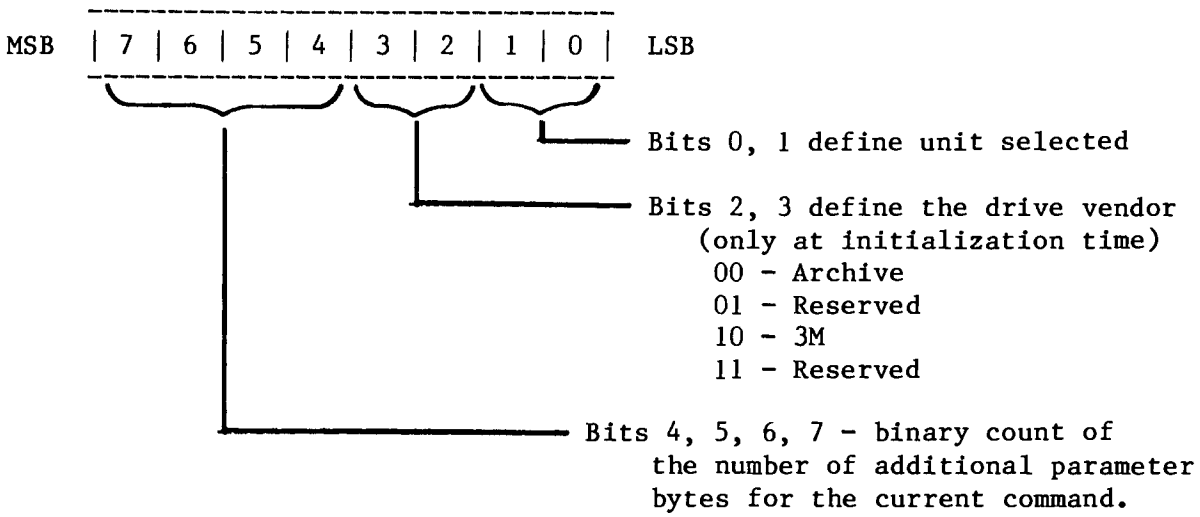


Figure 3-8. Parameter Byte 0

The two data transfer commands (WRITE and READ) must issue a Start of Transfer (SOT) command to the iSBX 217B board before starting the data transfer, and an End of Transfer command (EOT) once the data transfer is over.

If, however, the iSBX 217B board aborts the transfer, the End of Transfer command is not required. The host should instead read the sense status bytes. The following 17 subsections describe the commands available on the iSBX 217B board. The commands are listed in numerical order. Unless otherwise indicated each 3M drive command requires only one parameter byte (all Archive drive commands require only one parameter byte).

3.6.1 SOFTWARE RESET COMMAND (00H)

This command causes the iSBX 217B board to perform a checksum test on its internal ROM and to clear its internal RAM. The RESET command also initializes control port P2. The Reset command must be given as the first command after power-up. The iSBX 217B board considers all other commands invalid until the RESET command has been issued. Once the RESET command has been issued, the iSBX 217B board accepts RESET or INITIALIZATION commands only. The drive not ready bit in the sense status byte is set at the completion of the RESET command.

3.6.2 INITIALIZATION COMMAND (01H)

The INITIALIZATION command must be the second command given after power-up and/or the RESET command. The INITIALIZATION command checks to see if the drive is present, resets the drive, and reads the drive status. Additionally, this command informs the iSBX 217B board which type of drive (Archive or 3M) is attached. Following initialization, the iSBX 217B board can accept any command which the attached drive supports. Figure 3-8 shows the format of the INITIALIZATION command parameter byte.

3.6.3 WRITE COMMAND (02H)

The behavior of this command depends on the drive type attached.

Archive Drive:

The WRITE command writes a block of user data to the drive. For the Archive interface, the length of the block of data written to the drive can be any size as long as the byte count is in multiples of 512 bytes. Zeros must be appended at the end of the block if needed. Refer to the Archive Corporation drive manual for suggested data block lengths. The iSBX 217B board automatically writes a file mark on the tape after the host terminates the write function via the End of Transfer command (Archive interface only). The host may then issue another WRITE command and write another file.

3M Drive: PARAMETER BYTES: 3

For the 3M interface, data is stored on a preformatted tape with 1024 bytes per block. The host is not required to write blocks of data in 1024 byte increments, but is required to write an even number of bytes. The host must also supply the iSBX 217B board with starting block and track number (specified in parameter bytes 1 and 2). Figure 3-9 shows the format of the 2 parameter bytes.

3.6.4 WRITE FILE MARK COMMAND (03H)

The behavior of this command depends on the drive type attached.

The WRITE FILE MARK command is used to logically group data together by placing a filemark after the preceding data. One of the reasons for separating data into smaller segments is to prevent an unrecoverable loss of large data files.

Archive Drive:

In the Archive interface only, the WRITE FILE MARK command is automatically issued at the conclusion of a WRITE command. Therefore, if the host issues another such command when interfaced to the Archive drive, a double file mark would be written on the tape.

3M Drive:

In the 3M interface, the WRITE FILE MARK command writes an End Of File mark on the tape. This action uses the same amount of tape as a block of data.

3.6.5 READ COMMAND (04H)

The behavior of this command depends on the drive type attached.

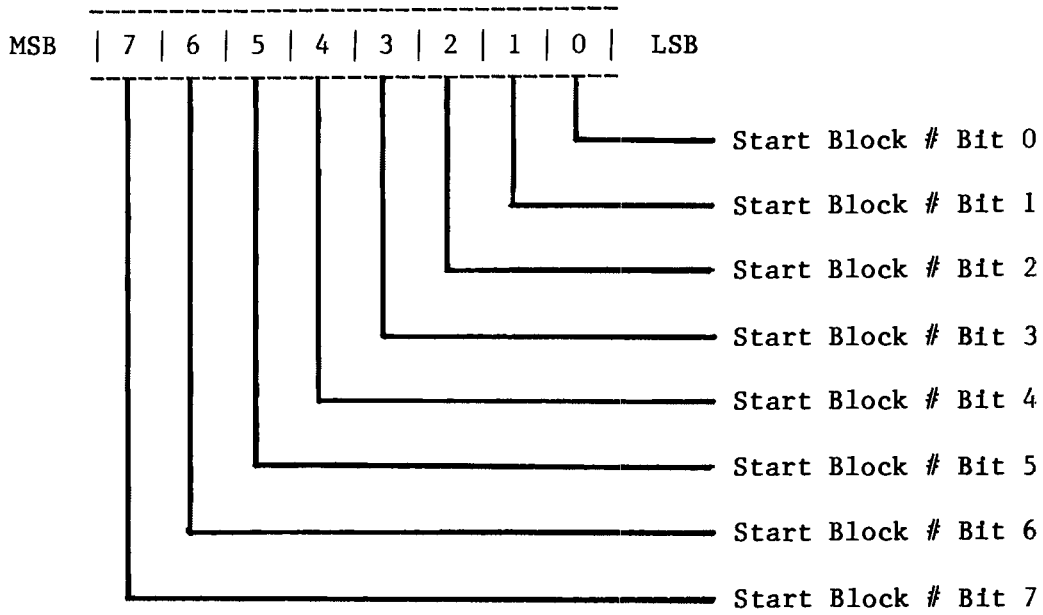
The READ command reads a block of data from the drive. Both interfaces terminate the READ command when a file mark is detected.

Archive Drive:

In the Archive interface, if the host does not read a whole file, i.e. detect a file mark, then at the completion of the End of Transfer, the tape will automatically rewind to the beginning of the tape. However, if a file mark is detected from the drive status bytes, then the host can issue another READ command and read the next file. As in the WRITE command, data must be transferred in 512 byte blocks. In the I/O read mode however, the tape ready bit (SOD) is polled between byte 511 and 512 of the block if using programmed I/O operation.

READ, WRITE COMMANDS

PARAMETER BYTE 1:



READ, WRITE COMMANDS

PARAMETER BYTE 2:

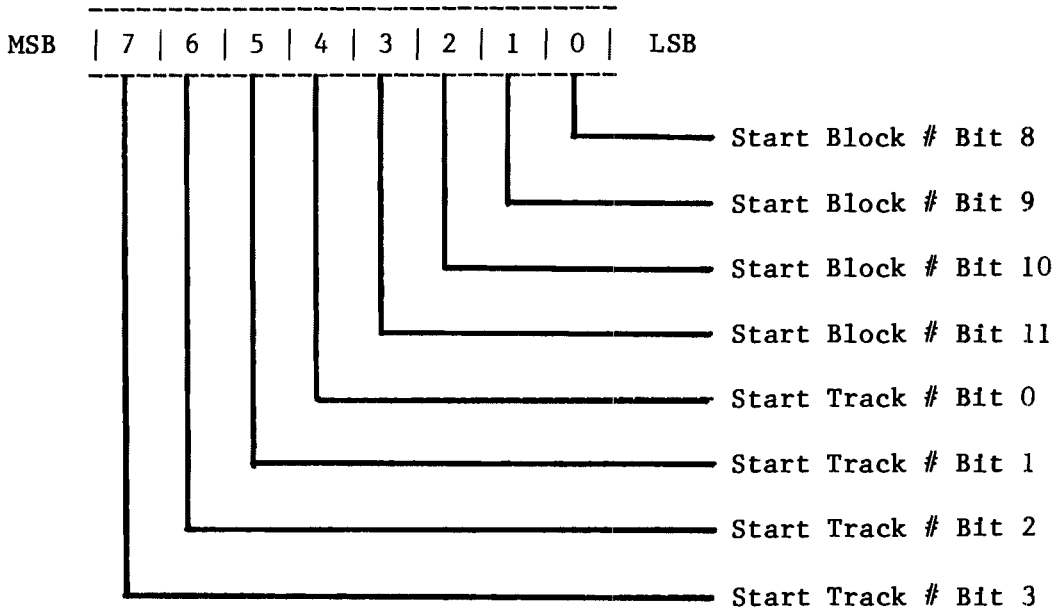


Figure 3-9. Parameter Bytes 1 and 2 For READ/WRITE/VERIFY Commands

3M Drive: PARAMETER BYTES: 3

In the 3M interface, the READ function requires a block and track number with the same format as the WRITE command. Refer to Figure 3-9. The host is not required to read the entire file; however, it must read an even number of bytes.

3.6.6 READ FILE MARK COMMAND (05H) - ARCHIVE DRIVE ONLY

This command works in conjunction with the Archive interface only. It allows the host to count file marks without transferring any data. This command allows you to position the tape to the desired file. Following the command, the tape is positioned after the next file mark.

3.6.7 READ STATUS COMMAND (06H)

This command reads the status of the drive. Refer to Section 3.7 for additional drive status information.

3.6.8 REWIND COMMAND (07H) - ARCHIVE DRIVE ONLY

This command rewinds the tape to the beginning of the tape. This command should be issued after the INITIALIZATION command. This command must also be issued prior to changing the unit number (if more than one drive is attached).

3.6.9 RETENSION COMMAND (08H) - ARCHIVE DRIVE ONLY

The RETENSION command winds the tape from beginning to end and back to the beginning. This is done to equalize the tension throughout the tape.

3.6.10 ERASE TAPE COMMAND (09H) - ARCHIVE DRIVE ONLY

Used for the Archive interface only, this command should be used when the host is ready to use a new tape or re-recording on a used tape. If the host is to use the No Data Detect bit in the sense status bytes to find where the recorded data on the tape ends, the tape must be completely erased.

3.6.11 UNLOAD TAPE COMMAND (0CH) - 3M DRIVE ONLY

Used for the 3M interface only, this command causes the cartridge to be wound to end of the tape. The Unload Tape command also unlocks the cartridge eject lever.

3.6.12 CONTINUE COMMAND (14H) - 3M DRIVE ONLY

Used for the 3M interface only, the CONTINUE command causes the write operation to continue in the next block after an unreadable header is detected. After a READ command was terminated by a file mark, a Continue command will resume the READ command.

NOTE

This command should be used ONLY under the conditions described here.

3.6.13 WRITE RAM COMMAND (15H) - 3M DRIVE ONLY PARAMETER BYTES: 5

This is a special diagnostic command used by the 3M Company HCD-75 tape drive. Refer to the 3M HCD-75 user manual for implementation information. Figure 3-10 shows the parameter byte format for the WRITE MEMORY command.

3.6.14 READ RAM COMMAND (16H) - 3M DRIVE ONLY PARAMETER BYTES: 5

This is a special diagnostic command used by the 3M Company HCD-75 tape drive. Refer to the 3M HCD-75 user manual for implementation information. Figure 3-10 shows the parameter byte format for the READ RAM command.

3.6.15 VERIFY COMMAND (17H) - 3M DRIVE ONLY PARAMETER BYTES: 5

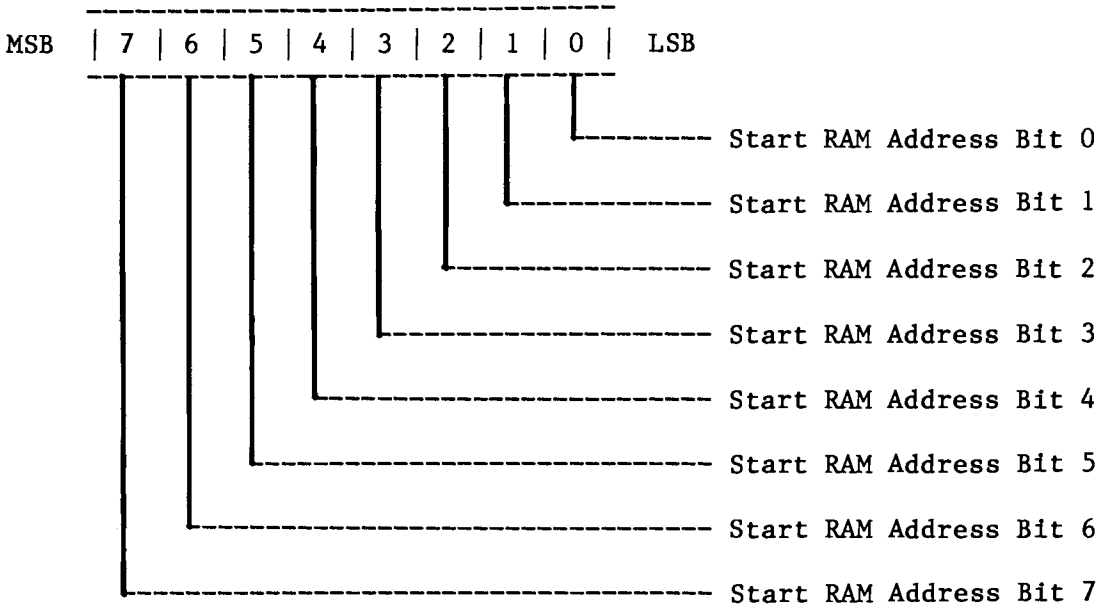
The Verify command for the HCD-75 tape drive checks for any data errors via the error detection circuitry. The verification is performed from a beginning track and block number to an ending track and block number. Refer to Figure 3-11 for the format of the VERIFY command parameter bytes.

3.6.16 START OF TRANSFER (SOT) COMMAND (40H)

This command must be issued by the host before the start of the data transfer. This action synchronizes the data transfer handshake from the host to the iSBX 217B board. The unit number used in the SOT command must match the unit number in parameter byte 0, and the EOT command.

READ RAM, WRITE RAM COMMANDS

PARAMETER BYTE 1:



READ RAM, WRITE RAM COMMANDS

PARAMETER BYTE 2:

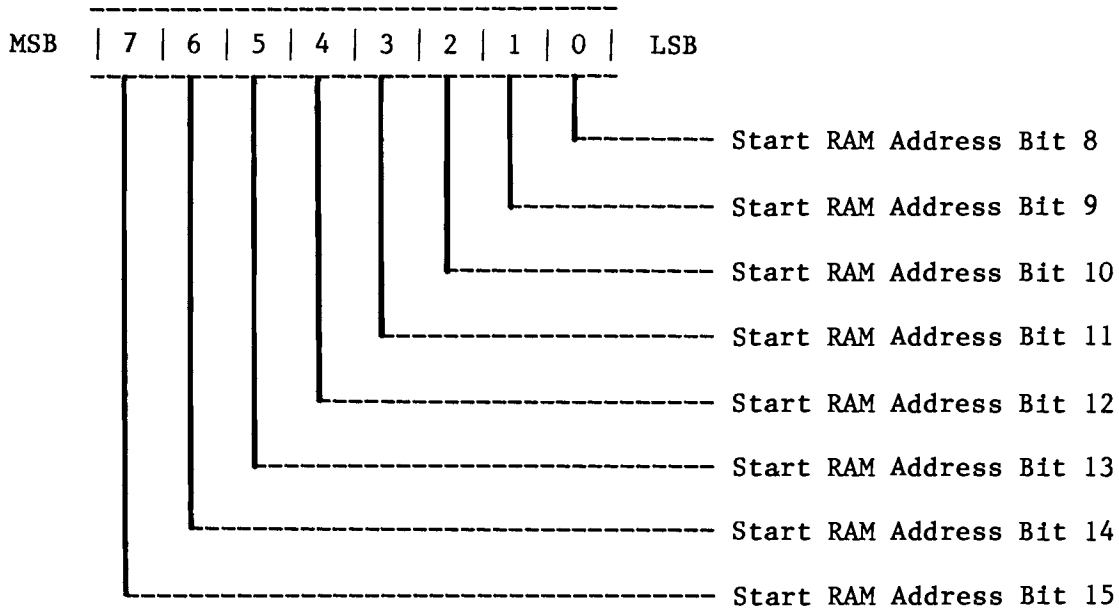
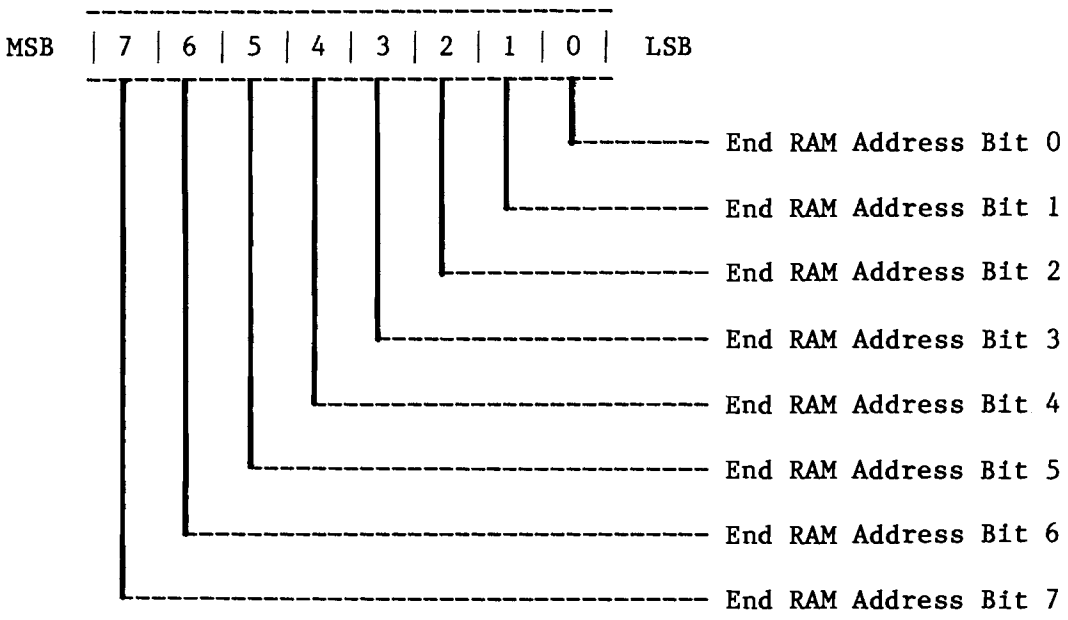


Figure 3-10. READ/WRITE RAM Parameter Bytes

READ RAM, WRITE RAM COMMANDS

PARAMETER BYTE 3:



READ RAM, WRITE RAM COMMANDS

PARAMETER BYTE 4:

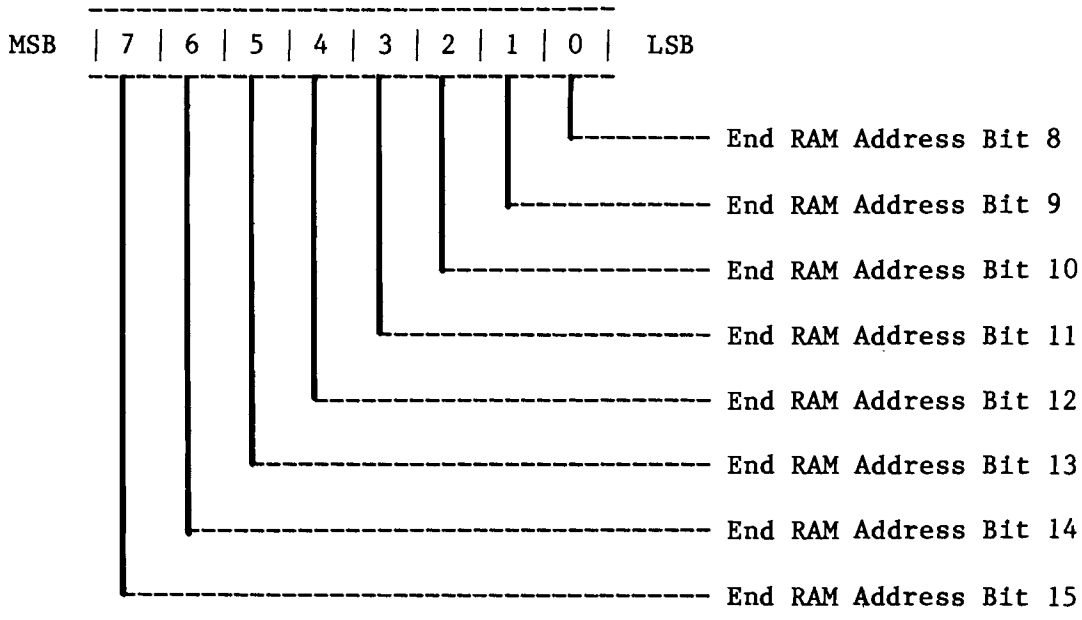
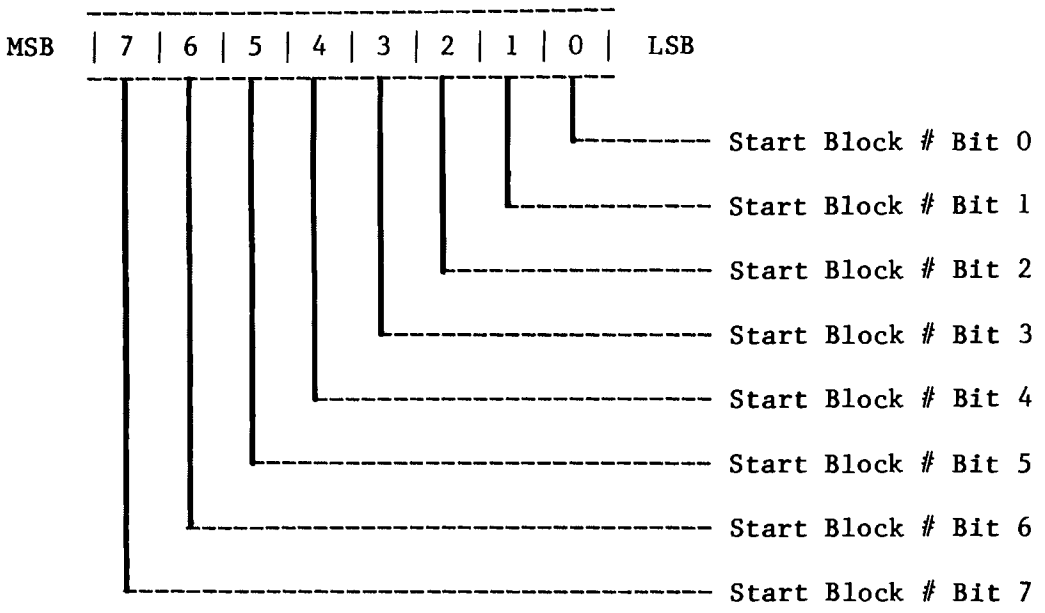


Figure 3-10. READ/WRITE RAM Parameter Bytes (continued)

VERIFY COMMAND

PARAMETER BYTE 1:



VERIFY COMMAND

PARAMETER BYTE 2:

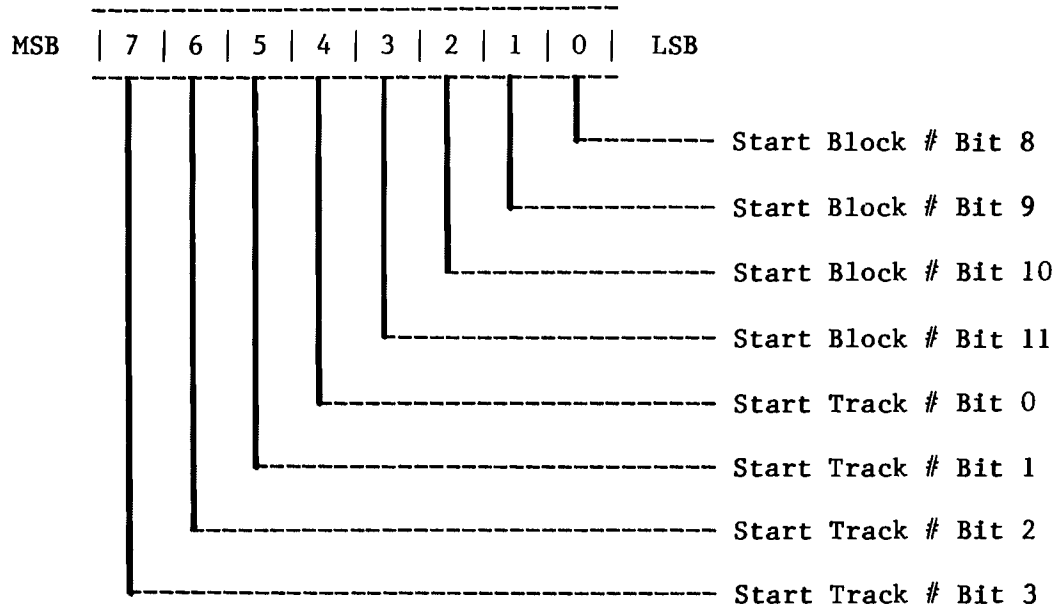
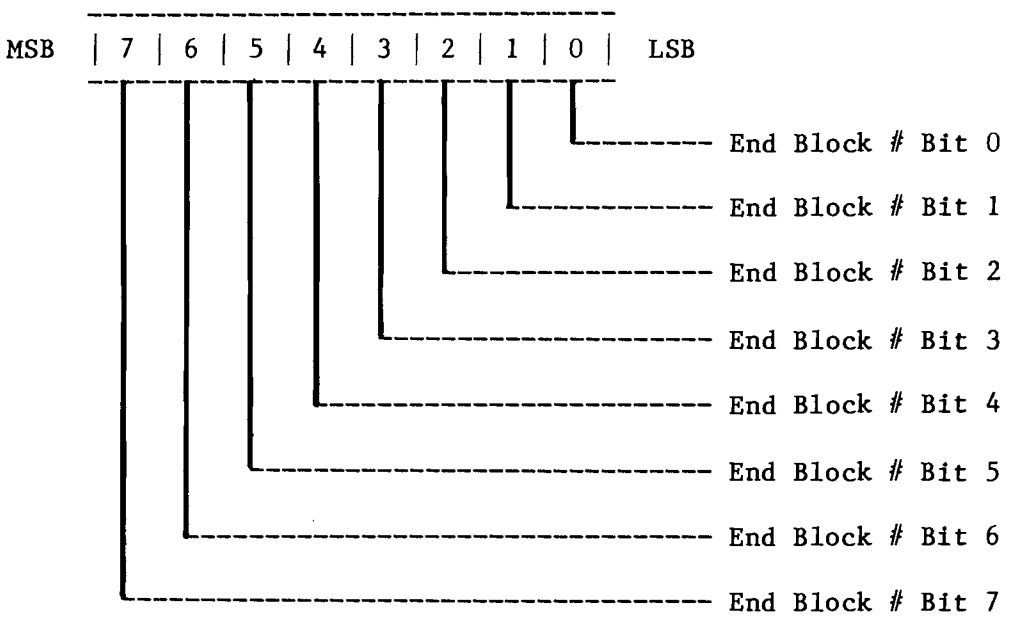


Figure 3-11. VERIFY Command Parameter Bytes

VERIFY COMMAND

PARAMETER BYTE 3:



VERIFY COMMAND

PARAMETER BYTE 4:

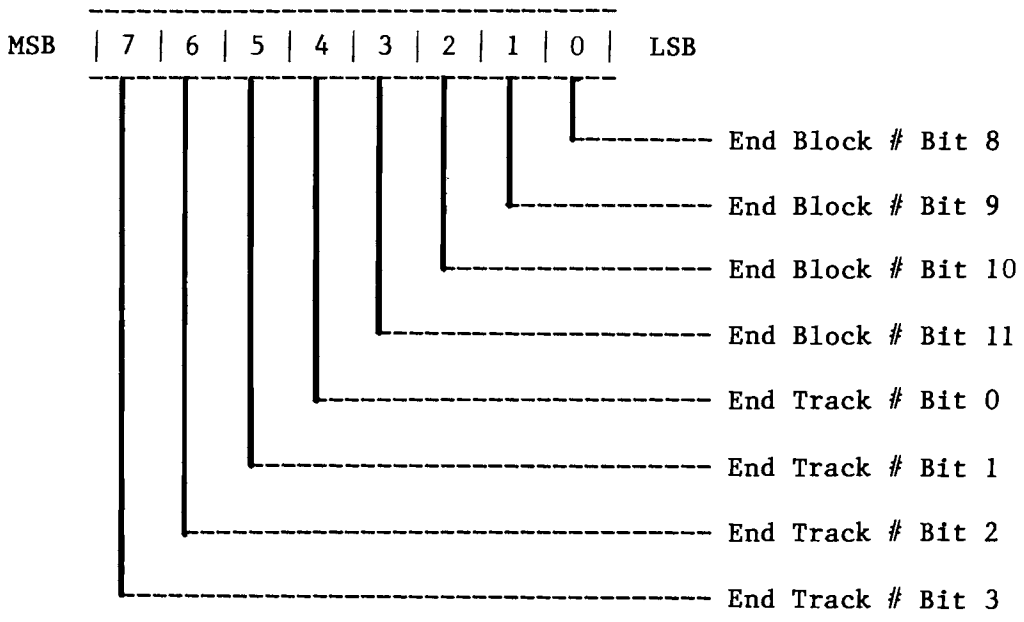


Figure 3-11. VERIFY Command Parameter Bytes (continued)

3.6.17 END OF TRANSFER (EOT) COMMAND (80H)

This command must be issued after completing the data transfer. The purpose of the END OF TRANSFER command is to inform the iSBX 217B board that the data transfer is complete. Since the iSBX 217B board does not count the number of bytes transferred during a read or write operation, it would not otherwise know the transfer had finished. The unit number used in the EOT command must match the unit number in parameter byte 0, and the SOT command.

NOTE

Do not issue the END OF TRANSFER command if the transfer was aborted by the iSBX 217B board (MINTRO or OBF detected prior to issuing SOT).

3.7 DRIVE SENSE STATUS BYTES

The sense status bytes must be read at the completion of every command. The following paragraphs discuss the status sense bytes. Figures 3-12 through 3-14 define bit functions for these bytes. These bytes are used for error checking and to monitor the results of read or write operations.

The bit definitions for the Sense Status Bytes are shown below:

SENSE BYTE 1:

B0: Checksum Error is set only for the reset command and means the internal EPROM of the UPI device on the iSBX 217B board is not functioning properly. The host should not use the iSBX 217B board when this bit is set.

B1: The drive not ready bit is set by either of the following sources:

1. The drive is not ready, or not on-line;
2. The drive has not been initialized.

B2: Hard Data Error is set during a read or write operation when an unrecoverable data error exists.

B3: Soft Data Error is set for each read after write error during a write command or for each read retry for a read command.

B4: Buffer Under-Run Error is set when the host cannot transfer the data fast enough for the Archive drive to operate continuously.

SENSE BYTE 0:

MSB	7	6	5	4	3	2	1	0	LSB

Binary count of the number of sense bytes to be read by the host after Sense Byte 0. For the Archive drive it will always be 3; for the 3M drive it will always be 3 until the INITIALIZATION command is issued; after that, it will always be 5, unless the RESET command is issued.

SENSE BYTE 1:

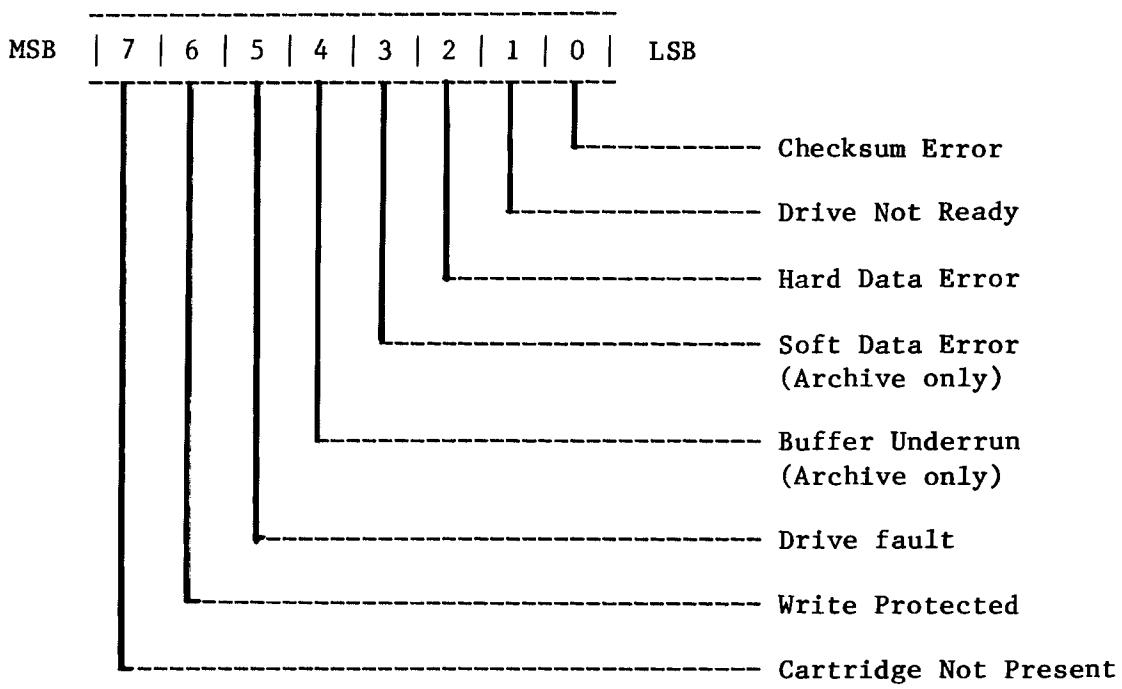
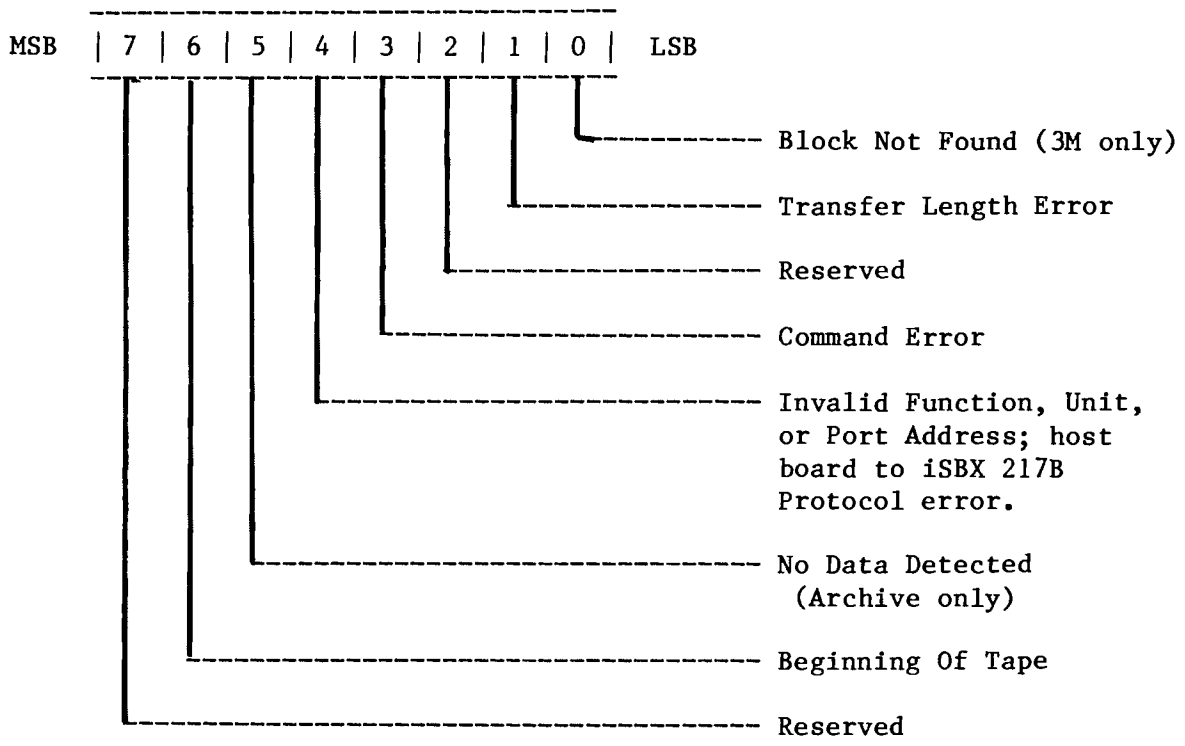


Figure 3-12. Status Sense Bytes 0 and 1

SENSE BYTE 2:



SENSE BYTE 3:

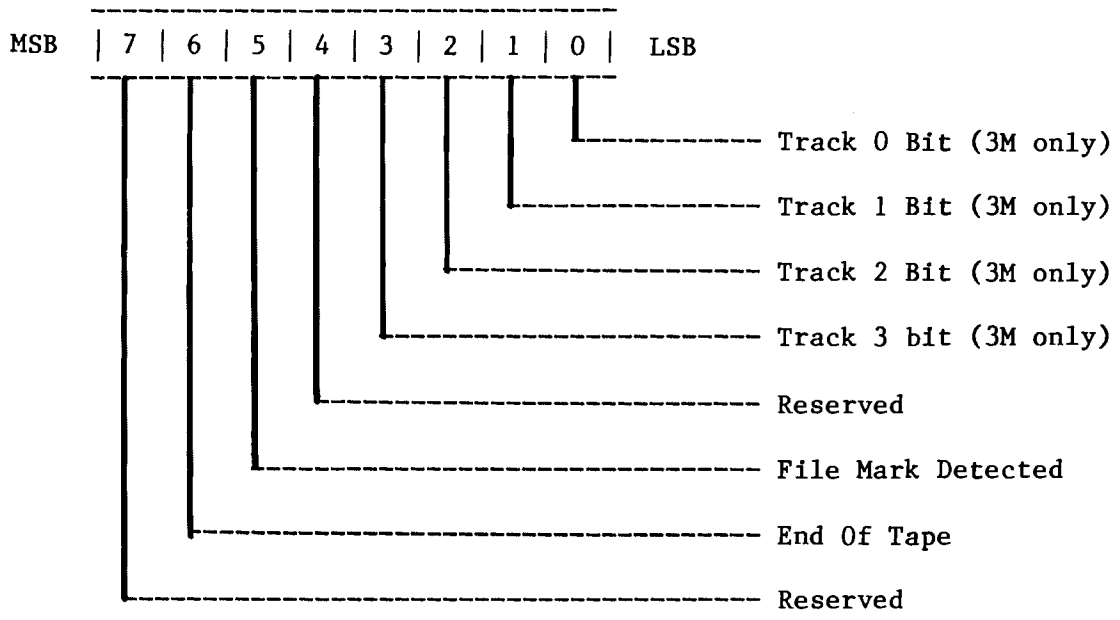
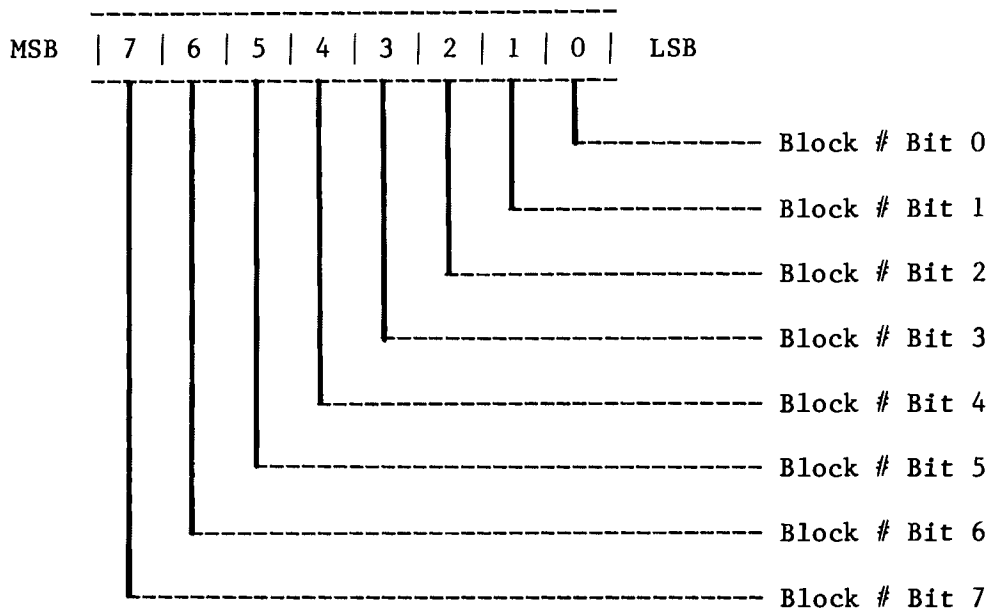


Figure 3-13. Status Sense Bytes 2 and 3

SENSE BYTE 4 (3M DRIVE ONLY):



SENSE BYTE 5 (3M DRIVE ONLY):

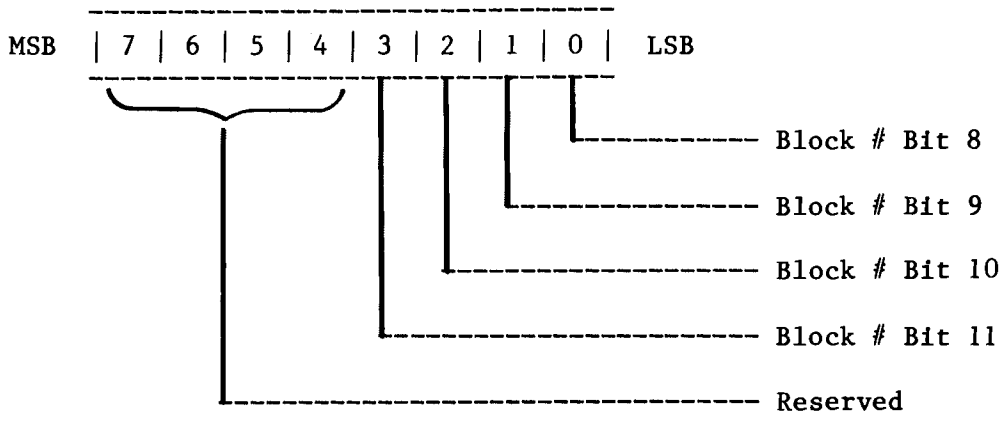


Figure 3-14. Status Sense Bytes 4 and 5

B5: The fault bit is set by any of the following faults:

1. Drive is not ready (refer to drive manual);
2. Communication failure of any type between iSBX 217B board and the host board;
3. Communication failure between iSBX 217B board and the host board when the iSBX 217B board is expecting a SOT command or EOT command, but receives another command.;

B6: Write-Protect bit is set if the drive is write-protected.

B7: Cartridge Not Present bit is set when the drive is empty.

SENSE BYTE 2:

B0: Block Not Found Error is set when the desired block and track number header key cannot be found; or if the block you are reading is not followed by a file mark or data.

B1: The length error bit is set whenever the drive terminates the data transfer rather than the host board terminating the transfer.

B2: Reserved.

B3: Command Error occurs if the drive has detected an invalid command, such as not rewinding one unit before communicating with a second unit (if multiple drives are attached).

B4: Invalid Function, Unit, or Port Address Error means the host has violated the communications protocol with the iSBX 217B board; or when an invalid command (such as issuing a 3M-only command to the Archive drive) is executed.

B5: The No-Data-Detected Error occurs when the drive fails to detect a data block or file mark and times out.

B6: Beginning Of Tape bit. For the Archive drive this bit is set when the tape is rewound and positioned at the logical beginning of tape. For the 3M drive this bit is set when the tape is rewound and positioned at the physical beginning of tape.

B7: Reserved.

SENSE BYTE 3:

B0: Track 0 Bit.

B1: Track 1 Bit.

B2: Track 2 Bit.

B3: Track 3 Bit.

B4: Reserved.

B5: The file mark bit is set when a file mark has been detected by the drive.

B6: End Of Tape bit. When set, this bit signifies the drive (Archive and 3M) has reached the logical (not physical) end of tape.

B7: Reserved.

SENSE BYTE 4:

B0 - B7: These bits are the least significant 8 bits (bits 0 - 7) of the current block after the operation is completed. During a read operation the block number is valid only if a file mark is detected.

SENSE BYTE 5:

B0 - B3: These bits are bits 8 through 11 of the current block.
B5 - B7: Reserved

***

CHAPTER 4. SERVICE INFORMATION

4.1 INTRODUCTION

This chapter provides the following service related information:

a. Service assistance information.
b. Replacement parts list and diagram.
c. Schematic diagrams.

4.2 SERVICE ASSISTANCE

United States customers can obtain service and repair assistance by contacting the Intel Product Service Center in Phoenix, Arizona. Customers outside the United States should contact your sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Center, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). This number is usually silk-screened onto the component side of the board.

c. Serial number of the product. This number is usually stamped onto the component side of the board.

d. Shipping and billing addresses.

e. Purchase order number for billing purposes if your Intel product warranty has expired.

f. Extended warranty agreement information, if applicable.

Use the following numbers for contacting the Intel Product Service Marketing Administration group:

Regional Telephone Numbers:

Western Region:	602-869-4951
Midwestern Region:	602-869-4392
Eastern Region:	602-869-4045
International:	602-869-4391

TWX Numbers:

910 - 951 - 1330
910 - 951 - 0687

Always contact the Product Service Marketing Administration group before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Product Service Center, use the original factory packing material, if possible. If this material is not available, wrap the product in cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by the Product Service Marketing Administration group personnel.

4.3 REPLACEMENT PARTS

A complete list of replacement parts is provided in Table 4-1. This list provides the part number, description and quantity of the item. Notice that each item is referenced in the parts location diagram. Some of the parts are available from any normal commercial source, and should be ordered by their generic description. Programmed parts should be ordered from Intel. Figure 4-1 shows the location of each iSBX 217B referenced part in Table 4-1.

4.4 SERVICE DIAGRAMS

Figure 4-2 provides a schematic diagram of the iSBX 217B Multimodule Board. The schematic diagrams are current when the manual is printed. However, minor revisions to the diagrams may occur between manual printings. Therefore, Intel provides photocopies of the current schematic diagrams with the board, when it is shipped from the factory. These diagrams should be inserted into this manual for future reference. In most instances, the diagrams shipped with the board will be identical to those printed in the manual.

Table 4-1. Replacement Parts

Ref Des	Description	Qty
U1	I.C., 74LS280	1
U2	I.C., 74LS32	1
U3	I.C., 74S241	1
U4	Programmed PAL (145196-001)	1
U5	Programmed 8741A (145195-001)	1
U6,7	I.C., 74LS374	2
U8	I.C., 8303	1
U9	I.C., 74LS08	1
U10	I.C., 74S240	1
U11	I.C., 74S374	1
R1-5, 11	Resistor, 470 ohm, 1/8W, 5%	6
R6-10	Resistor, 10K ohm, 1/8W, 5%	5
RP1, 2	Resistor Pack, 220/330 ohm	2
RP3	Resistor Pack 10K ohm	1
C1-3, 5, 7-9	Capacitor 0.1uf, +80-20%, 50V	7
C4	Capacitor 22pf, 5%, 50V	1
C6	Capacitor 22pf, 10%, 15V	1
Y1	Crystal 6MHz	1
P1	Connector, 36-pin	1
J1	Connector, header, 50-pin	1

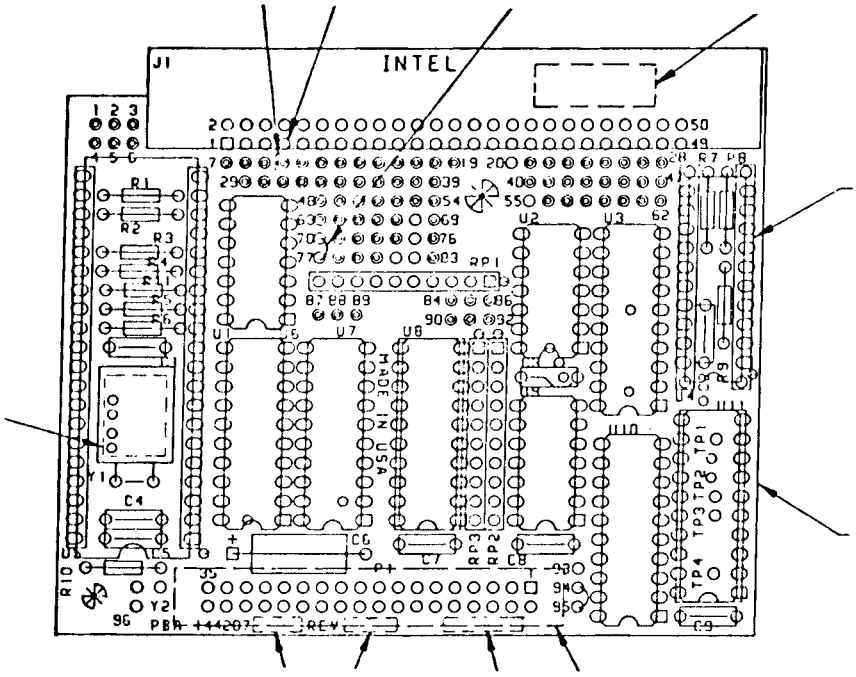
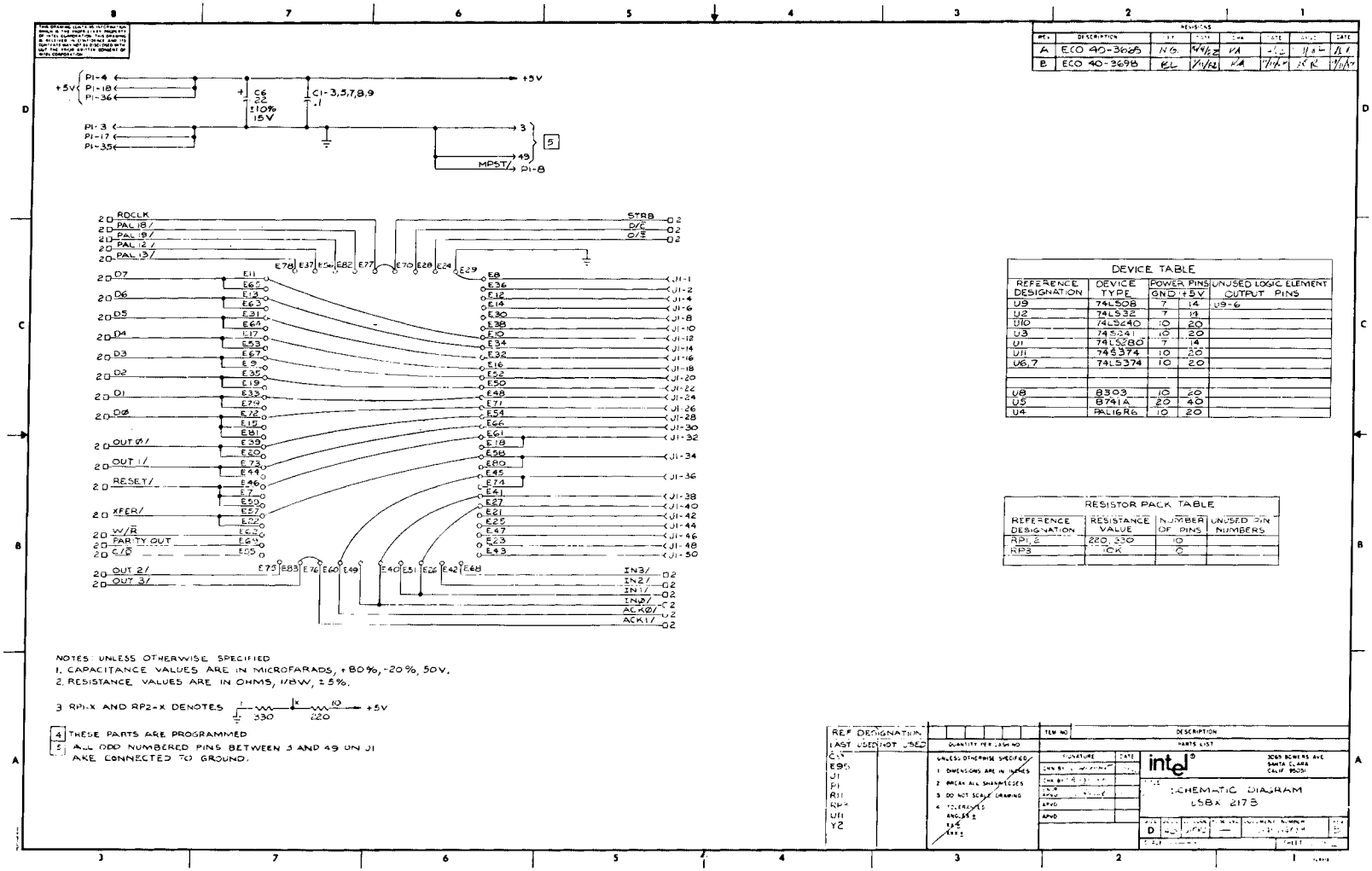


Figure 4-1. Parts Location Diagram



DEVICE TABLE

REFERENCE DESIGNATION	DEVICE TYPE	POWER PINS GND	POWER PINS +5V	UNUSED LOGIC ELEMENT OUTPUT PINS
U9	74LS08	7	14	U9-6
U2	74LS32	7	14	
U10	74LS240	10	20	
U3	74LS241	10	20	
U1	74LS280	7	14	
U11	74S374	10	20	
U6,7	74LS374	10	20	
U8	8303	10	20	
U5	8741A	20	40	
U4	PAL16R6	10	20	

RESISTOR PACK TABLE

REFERENCE DESIGNATION	RESISTANCE VALUE	NUMBER OF PINS	UNUSED PIN NUMBERS
RP1,2	220, 330	10	
RP3	10K	10	

NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITANCE VALUES ARE IN MICROFARADS, +80%,-20%, 50V.
2. RESISTANCE VALUES ARE IN OHMS, 1/8W, ±5%.
3. RP1-X AND RP2-X DENOTES 1 — 330 — X — 10 — 220 — +5V
4. THESE PARTS ARE PROGRAMMED
5. ALL ODD NUMBERED PINS BETWEEN 3 AND 49 ON J1 ARE CONNECTED TO GROUND.

REF DESIGNATION
LAST USED/NOT USED
C
E9
J1
P1
R11
RP
U11
Y2

QUANTITY PER ASSY NO

UNLESS OTHERWISE SPECIFIED
1 DIMENSIONS ARE IN INCHES
2 BREAK ALL SHARP EDGES
3 DO NOT SCALE DRAWING
4 TOLERANCES
ANG ±
XX ±
XXX ±

ITEM NO | DESCRIPTION | PARTS LIST

SIGNATURE | DATE
DRN
CHK
APVD
APVD

intel 3065 BOWERS AVE SANTA CLARA CALIF. 95051

SCHEMATIC DIAGRAM
SBX 2173

SIZE D | FSCM NO | DWG NO | REV

SCALE | SHEET

Figure 4-2. Schematic Diagram (Sheet 1)

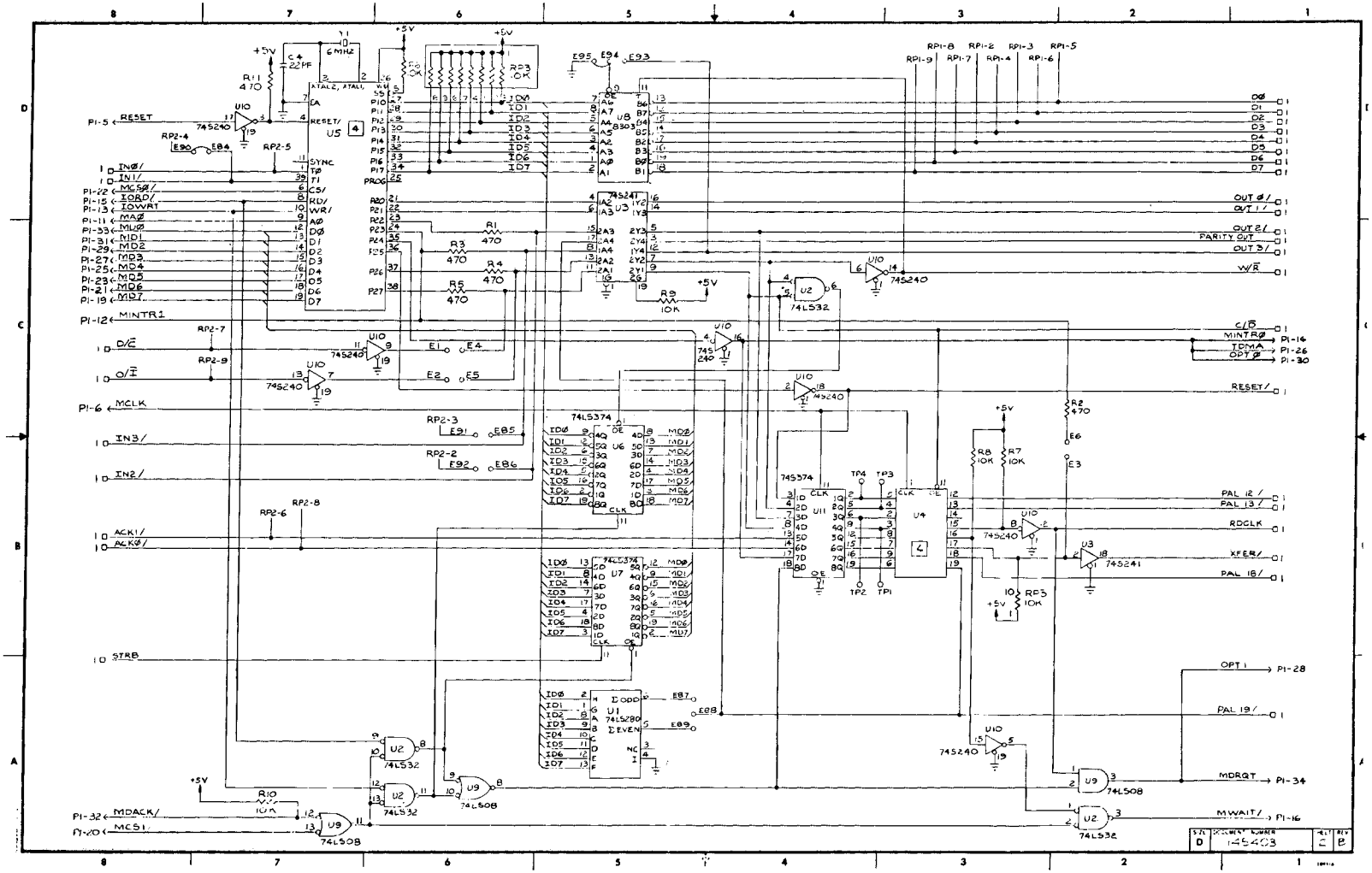


Figure 4-2. Schematic Diagram (Sheet 2)

APPENDIX A. DRIVE ANOMALIES

During the development of the iSBX 217B board, several minor drive irregularities were discovered. In most cases these drive anomalies will not present any major problems. However, the anomolies are presented here for your reference.

Archive Drive Only:

We discovered only one Archive drive anomoly requiring documentation. When reading a file of unknown length, the host should wait for 200 milliseconds before issuing the End Of Transfer (EOT) command.

3M Drive Only:

Three amomalies worthy of notation were discovered with the 3M drive.

1. If the drive terminates a read operation due to a file mark, and then the host issues a READ STATUS command for the next command, the drive returns erroneous data. This is true for single and multiple drive configurations.

2. If the host writes 100 to 1FE (hex) bytes or 300 to 3FE bytes in one block, then when reading the same block the byte count will be increased by 200. That is, (100 to 1FEH) + 200; or (300 to 3FE) + 200.

3. When writing the last block at the end of the tape (block FFFF), the drive allows up to an additional 800 (hex) bytes to be writen before the drive terminates the operation. Note that these bytes are lost and cannot be read or recovered.

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