iSBX 311™ ANALOG INPUT MULTIMODULE™ BOARD HARDWARE REFERENCE MANUAL

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PREFACE

This manual provides general information, preparation for use, programming information, principles of operation, and service information for the iSBX 311 Analog Input Multimodule Board. Supplementary information is provided in the following documents.

- Intel MCS-85 User's Manual, Order No. 9800366.
- Intel Peripheral Design Handbook, Order No. 9800676.
- Intel Multibus Specification, Order No. 9800683.
- Intel iSBX Bus Specification, Order No. 142686-001

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CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBX 311 Analog Input Multimodule Board is a member of Intel's growing family of expansion boards, designed to allow quick, easy, and inexpensive expansion for the Intel single board computer product line. The iSBX 311 Analog Input Multimodule Board (hereafter referred to as the Multimodule board) provides the ability to add analog input functions to any host iSBC board that contains an iSBX bus connector. Compatibility can also be maintained with the iCS 910 Analog Signal Conditioning/Termination Panel, since the Multimodule board contains a 50-pin edge connector with a pin assignment compatible with that of the iSBC 711 Analog Input Board. This manual contains the information required to use the Multimodule board, including chapters on general information, preparation for use, programming, principles of operation, and service information.

1-2. DESCRIPTION

The Multimodule board, shown in figure 1-1, is designed to plug onto any host iSBC microcomputer that contains an iSBX bus connector (P1). The board provides 8 differential or 16 single-ended analog input channels that may be jumper-selected as the application requires. The Multimodule board includes a user-configurable gain, and a user-selectable voltage input range (0 to +5 volts, or -5 to +5 volts).

The Multimodule board receives all power and control signals through the iSBX bus connector to initiate channel selection, sample and hold operation, and analog-to-digital conversion.

1-3. EQUIPMENT SUPPLIED

Since the Multimodule board plugs directly onto the host iSBC board, no interface cables are required for

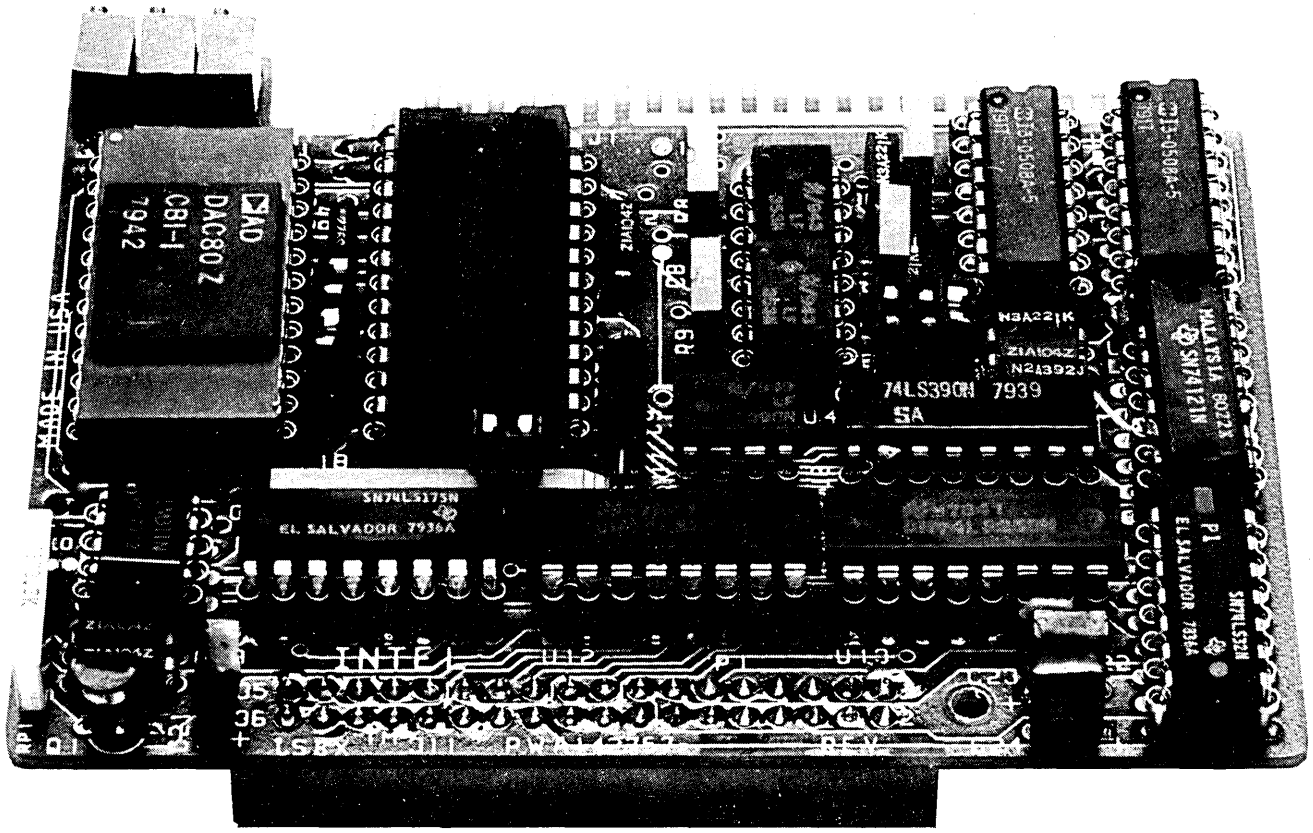


Figure 1-1. iSBX 311™ Analog Input Multimodule™ Board

the system. The following equipment is supplied with the iSBX 311 Analog Input Multimodule Board:

a. Schematic Diagram, drawing number 142820.
b. Two plastic screws, 1/4 6-32.
c. One plastic spacer, 1/2 6-32.

1-4. COMPATIBLE EQUIPMENT

The Multimodule board must be used with a host iSBC microcomputer that contains an iSBX bus connector. Multibus interfacing must be performed indirectly by means of a host iSBC microcomputer.

The input connector (J1) on the Multimodule board is compatible with the J2 and J3 connectors on the iSBC 711 Analog Board and on the iSBC 732 Combination Analog I/O Board. As a result, the Multimodule board may be used in most analog input applications satisfied by an iSBC 711 or iSBC 732 board. The Multimodule board interfaces readily to an iCS 910 Analog Input Signal Conditioning/ Termination Panel in the same manner as the iSBC 711 and 732 boards.

1-5. SPECIFICATIONS

The specifications for the iSBX 311 Analog Input Multimodule Board are listed in table 1-1.

Table 1-1. Specifications

POWER REQUIREMENTS		
V_{cc} = +5 volts (± 0.25 volts)	I_{cc} = 250mA maximum	
V_{dd} = +12 volts (± 0.6 volts)	I_{dd} = 50mA maximum	
V_{ss} =-12 volts (± 0.6 volts)	I_{ss} = 55mA maximum	
PHYSICAL CHARACTERISTICS		
Height:	2.03 cm (0.80 inch)	Multimodule board only.
	2.82 cm (1.13 inches)	Multimodule and iSBC boards.
Width:	6.35 cm (2.50 inches)	
Length:	9.40 cm (3.70 inches)	
Weight:	85 gm (2.31 ounces)	
ENVIRONMENTAL REQUIREMENTS		
Operating Temperature:	0° to 60°C (32° to 131°F).	
Relative Humidity:	To 90% (without condensation)	
INTERFACE COMPATIBILITY		
Connector P1 Interface:	Compatible with the iSBX bus interface requirements.	
Connector J1 Interface:	Analog pinout compatible with the iSBC 711 and 732 Analog Board input connector format. Connector details are contained in table 2-5.	
OPERATING CHARACTERISTICS		
Inputs:	8 differential. 16 single-ended. Jumper selectable; see table 2-2.	
Full Scale Input Voltage Range:	-5 to +5 volts (bipolar). 0 to +5 volts (unipolar). Jumper selectable; see table 2-2.	
Gain:	User-configurable through installation of two resistors at E1 to E2 and E3 to E4. Factory-configured for gain of X1 (E5 jumpered to E6); gain above 250 is possible but not recommended; see table 2-3.	
Resolution:	12 bits (11 bits plus sign for ±5 volts).	
Dynamic Error:	± 3/4 LSB (maximum) for a 10V voltage change.	

Table 1-1. Specifications (continued)

Accuracy:

Accuracy (max) at 25°C	Accuracy at 0° to 60°C
±0.035% FSR ±1/2 LSB	±0.20% FSR ±1/2 LSB, typical ±0.36% FSR ±1/2 LSB, maximum

Note: Figures are typical and are listed in percent of full scale reading (FSR) at a gain of 1. At any fixed temperature between 0° and 60°C, the accuracy is adjustable to ±0.025% ±1/2 LSB of full scale.

Gain TC (at Gain = 1):

30 PPM per degree centigrade, typical.
56 PPM per degree centigrade, maximum.

Offset TC (in percent of FCR/°C):

Gain	BIPOLAR		UNIPOLAR	
	typical	maximum	typical	maximum
1	0.0018%	0.0047%	0.0026%	0.0076%
5	0.0036%	0.015%	0.0063%	0.018%
50	0.024%	0.069%	0.048%	0.137%
250	0.116%	0.333%	0.232%	0.665%

*Offset is measured in bipolar mode and assumes that user-supplied gain resistors (10ppm) are installed for gains greater than 1.

Input Protection: 30 volts.

Input Impedance: 20 megohms (minimum).

Conversion Speed: 50 microseconds (typical).

Common Mode Rejection Ratio: 60 db (minimum).

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter of the text provides information on preparing and installing the iSBX 311 Analog Input Multimodule Board. The instructions include unpacking and inspection instructions; installation considerations, such as physical, power, cooling, and mounting requirements; jumper configuration; dc characteristics; connector assignments; jumper configuration; and installation procedures.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and the packing material for the agent's inspection.

For repair to a product damaged in shipment, contact the Intel Technical Support Center to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that the salvageable shipping cartons and packing material be saved for future use in the event that the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

Installation considerations such as power, cooling, mounting, and physical size requirements, are outlined in the following paragraphs.

NOTE

Ensure that none of the iSBX bus specifications or standards is violated if modification of the Multimodule board is required.

2-4. POWER REQUIREMENTS

The Multimodule board requires three voltages for operation; +5 volts (±0.25 volt) at 250 mA maximum, -12 volts (±0.6 volt) at 55 mA maximum, and +12 volts (±0.6 volt) at 50 mA maximum. All power for the board is drawn through the iSBX bus connector (P1) on the board.

The Multimodule board uses the -12 volt power supply voltage and components R4 and VR1 to create a -6.4 volt reference voltage and the DAC provides a +6.3 volt reference voltage from pin-24 for use with the analog circuitry.

2-5. COOLING REQUIREMENTS

The Multimodule board dissipates 35.73 gram-calories/minute (0.14 BTU/minute) of heat and adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F). The Intel Development Systems and other Intel system cardcages provide adequate air circulation for use with Multimodule boards.

2-6. MOUNTING REQUIREMENTS

Figure 2-1 shows the Multimodule board, the location of the iSBX bux connector, and the location of the mounting hole. The Multimodule will mount onto any host iSBC microcomputer containing an iSBX bus connector and the required mounting hole. The mounting hardware supplied with the Multimodule board includes:

a. 2 plastic screws, 1/4 inch 6-32, separate from board.
b. 1 plastic spacer, 1/2 inch 6-32, separate from board.
c. 36-pin connector P1, factory installed onto board.

NOTE

The Multimodule board, when installed onto a host iSBC microcomputer, occupies an additional card slot located within an iSBC 604/614 Cardcage and adjacent to the component side of the host iSBC microcomputer.

2-7. PHYSICAL DIMENSIONS

The outside dimensions of the Multimodule board are as follows:

a. Width: 6.35 cm (2.50 inches).
b. Length: 9.40 cm (3.70 inches).
c. Height: 2.03 cm (0.80 inch) Multimodule board only.
   2.82 cm (1.13 inches) Multimodule and iSBC boards.

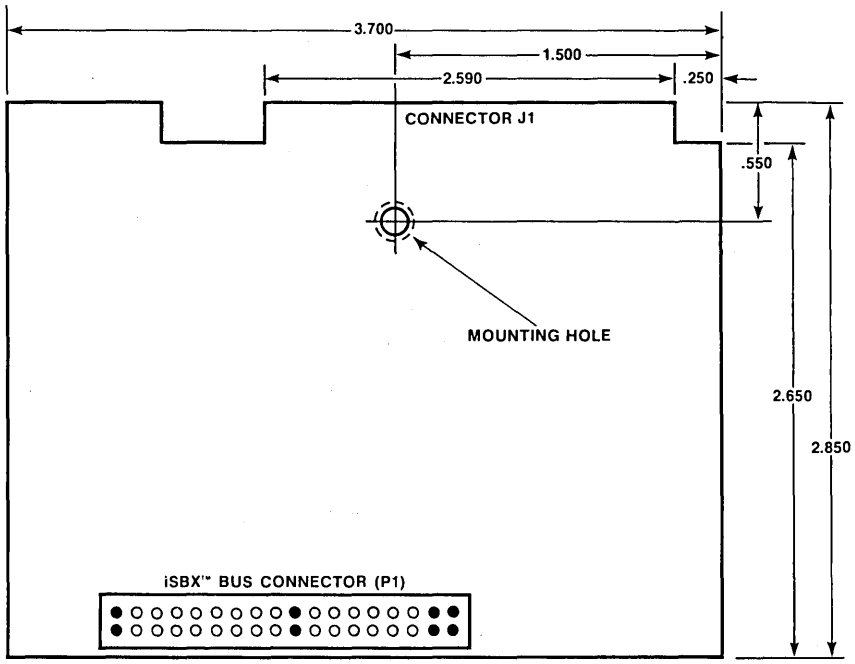


Figure 2-1. Board Dimensions (Inches)

Figure 2-1 shows the outside dimensions of the board and figure 2-2 gives the maximum height dimensions for the Multimodule board mounted onto a host iSBC microcomputer.

2-8. DC INTERFACE CHARACTERISTICS

The dc characteristics of the Multimodule board at the J1 connector are listed in table 2-1.

2-9. JUMPER CONFIGURATION

The 22 user-configured jumper positions on the iSBX 311 Analog Input Multimodule Board allow the user to select the operating mode for the input multiplexers and the DAC, and select the voltage gain for the amplifier. Table 2-2 lists the functions of the user-configurable jumpers. The Multimodule board is configued to the single ended bipolar mode of operation when shipped from the factory; this includes jumpers from E5 to E6, E8 to E9, E10 to E13, E11 to E12, E15 to E16, and E19 to E20. The

Table 2-1. DC Interface Characteristics

Output Signal	Type Drive	I_{OL} MAX (mA)	V_{OL} MAX (I_{OL} = MAX)	I_{OH} MAX (μA)	V_{OH} MIN (I_{OH} = MAX)	C_O MIN (pf)
MD0-MD7	TRI	2.0	0.5	-200	2.4	130
MINTR0	TTL	1.6	0.5	-100	2.4	40
Input Signal	**Type Receiver**	**I_{IL} MAX (V_{IL} = 0.4)**	**V_{IL} MAX**	**I_{IH} MAX (V_{IH} = 2.4)**	**V_{IH} MIN**	**C_I MAX (pF)**
MD0-MD7	TRI	-0.5	0.8	60	2.0	40
MA0	TTL	-0.5	0.8	60	2.0	40
MCS0/	TTL	-4.0	0.8	100	2.0	40
MRESET	TTL	-2.1	0.8	100	2.0	40
IOWRT/, IORD/	TTL	-1.0	0.8	100	2.0	40
MCLK	TTL	-2.0	0.8	100	100	40

TTL = Standard Totem Pole Output
TRI = Three-State

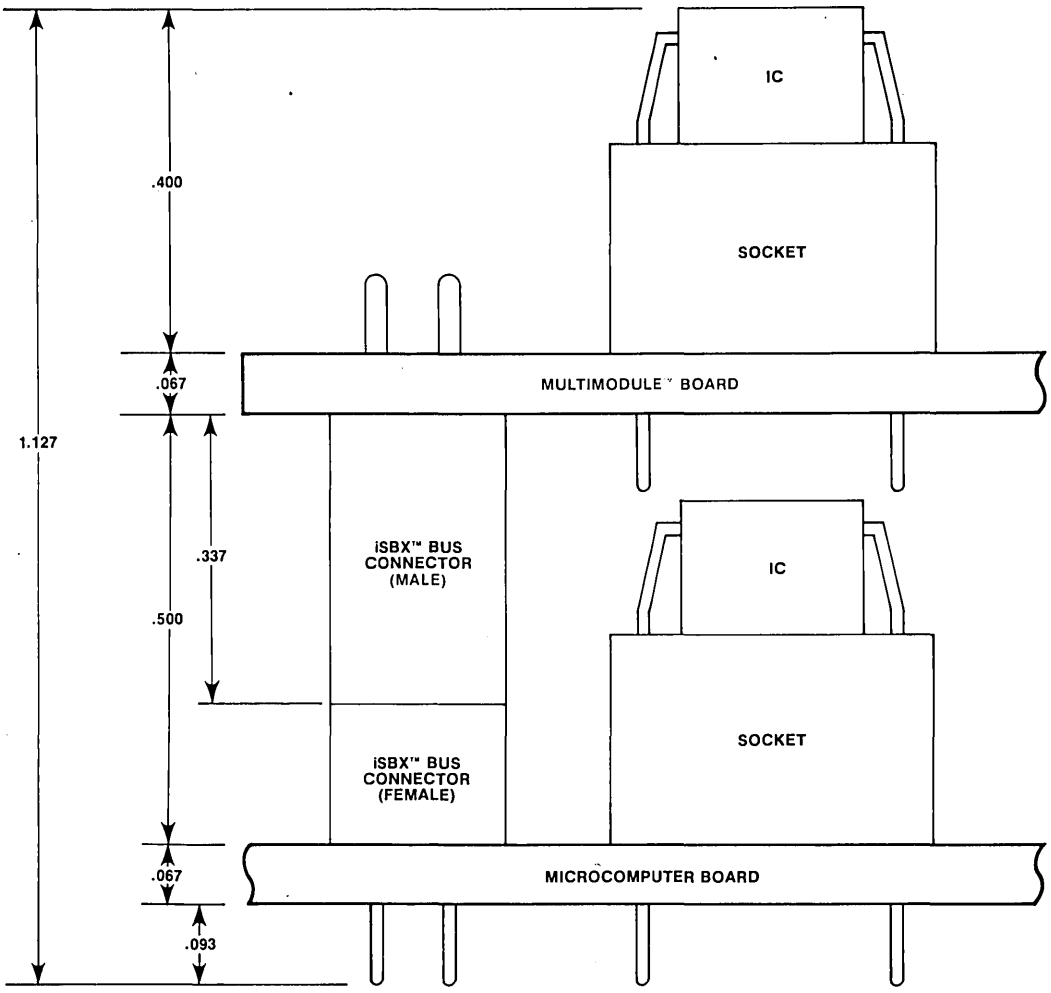


Figure 2-2. Mounting Clearances (Inches)

following paragraphs give more details on the various other jumper configurations available to the user.

INPUT MULTIPLEXER MODE SELECTION. Jumpers E19, E20, and E21 configure the multiplexer enable logic for either single-ended (connect E19 to E20) or differential (E20 to E21) operation. Single ended operation allows only one of the input multiplexers to be enabled; differential operation requires that both multiplexers be enabled to input both halves of the differential signal.

INPUT MULTIPLEXER CONFIGURATION. Jumpers E8, E9, E11, and E12 configure the Multimodule board for either single ended (connect E8 to E9 and E11 to E12) operation or differential (E9 to E12) operation. The jumper connections control which of the multiplexer outputs become amplifier inputs. For pseudo-differential mode operation, connect jumpers E8 to E9 and E12 to E13; this allows the ground reference to float with the user input signal.

DAC MODE SELECTION. The operating mode of the A-to-D converter is jumper selectable via jumpers E14, E15, E16 and E17 to either Unipolar (0 to 5 volts) input mode or Bipolar (-5 to +5 volts) input mode.

Unipolar operation (0 to 5 volts) requires a jumper from E14 to E15 and E16 to E17 to connect two internal DAC resistors in parallel into the signal path.

Bipolar operation (-5 to +5 volts) requires a jumper from E15 to E16. This configuration connects only one internal DAC resistor into the signal path and allows the DAC to be offset by 1.0 mA (half scale).

VOLTAGE GAIN SELECTION. As shipped from the factory, the Multimodule board contains a

jumper connecting E5 to E6 and no resistors from E3 to E4 and E1 to E2. This configures the board for a gain of 1. Configuration for a gain other than 1 is performed by removing the jumper connecting E5 to E6 and installing resistors at the mounting locations E1 to E2 (Rb) and E3 to E4 (Ra). Refer to table 2-3 for a list of resistor values and the voltage gains that they produce. The resistors shown in figure 2-3 must be axial 0.4 inch lead spacing to fit into the mounting positions (Ra is beneath U3, Rb is between U2 and U3). The capacitor (Cb in figure 2-3) must have 0.3 inch lead space in order to fit properly into the mounting position (E5 to E7) under the U3 socket on the board.

Table 2-2. User-Configured Jumpers

Jumper Functions	Jumper Position Number	Comments
Mode Selection for Input Multiplexers	E19, E20, E21	Connect E19 to E20*-single ended operation, 16 channels maximum. Connect E20 to E21-differential operation, 8 channels maximum.
Mode Selection for Input Multiplexers	E8, E9, E11, E12	Connect E8 to E9* and E11 to E12*-single ended. Connect E9 to E12-differential operation.
Analog Ground onto Input Returns	E10, E12, E13	Connect E10 to E13* to provide an analog ground out to the odd numbered pins of the J1 connectors. Connect E12 to E13 for pseudo-differential operation; the signal grounds float with respect to the board ground thereby eliminating ground loops. However, the ground differential must not exceed ±10V.
Mode Selection for DAC	E14, E15, E16, E17	Connect E14 to E15 and E16 to E17 -unipolar operation. Connect E9 to E10* bipolar operation.
Voltage Gain Select for Amplifier	E5, E6, E7	Connect E5 to E6*-Gain of one. Connect E5 to E7-mounting location for user-supplied capacitor to control noise.
	E1-E2, E3-E4	Install resistors into mounting locations for user-configuration of voltage gain; see table 2-3.
NOTES: * indicates the as-shipped configuration of the jumpers.		

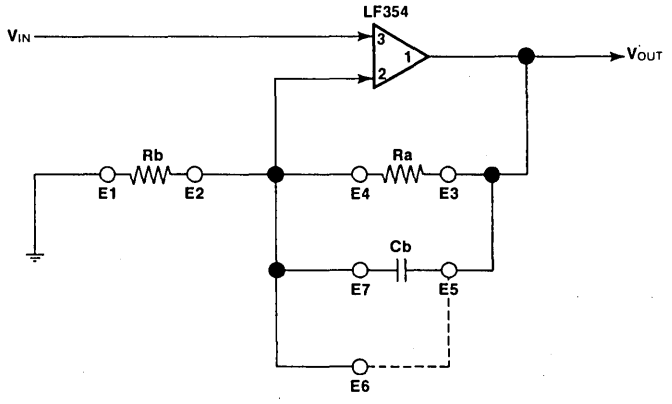


Figure 2-3. Voltage Gain Resistor Location

Table 2-3. Gain Resistor Values

GAIN	Ra VALUE	Rb VALUE
1	none	none
2	2.5K	2.5K
4	6K	2K
5	4K	1K
8	3.5K	500 ohms
10	4.5K	500 ohms
20	19K	100 ohms
50	**	50 ohms
250*	**	50 ohms

Notes: * suggested maximum gain configuration.
** choose Ra so that Rb does not exceed 50 ohms.

To choose the proper resistor values (Ra and Rb) for your application, first decide how much gain is required for the application and then calculate the resistor values as follows:

$$\text{Voltage Gain} = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{Ra}{Rb}$$

Consider these examples. If a voltage gain of 2 is required, then the resistors Ra and Rb must be chosen such that Ra = Rb. For a voltage gain of 10, Ra and Rb must be chosen such that Ra = 9Rb. Each case, however, requires that the total resistance (Ra + Rb) can be approximately 2000 ohms so that the amplifier can supply the required current output.

For higher gain applications, Rb should be 200 ohms or less to minimize noise pickup. Some configuration examples are listed in table 2-3.

NOTE

When selecting an Rb resistor value, bear in mind that the smallest possible value of Rb will provide the best possible noise immunity.

CAUTION

When installing resistors Ra and Rb, and capacitor Cb, ensure that the U3 and U4 chip sockets and surrounding traces are not contaminated with solder. Failure to do so could result in damage to the board.

The Multimodule board includes a mounting position for the user-installed capacitor (Cb in figure 2-3) under the U4 socket. The capacitor operates with Ra to increase the noise immunity of the board at the expense of reducing the bandwidth.

Capacitor Cb provides the user the ability to dampen high frequency noise at the U3 amplifier for applications using a higher gain. The capacitor works with Ra to form a time constant of approximately 1mS duration to allow time for the amplifier output to settle. The value of the capacitor is dependent on the value of resistor Ra, as shown in the following equation:

Table 2-4. iSBX™ BUS Pin Assignment

PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
35	GND	SIGNAL GROUND	36	+5V	+5V
33	MD0	M DATA BIT 0	34		Reserved
31	MD1	M DATA BIT 1	32		Reserved
29	MD2	M DATA BIT 2	30		Reserved
27	MD3	M DATA BIT 3	28		Reserved
25	MD4	M DATA BIT 4	26		Reserved
23	MD5	M DATA BIT 5	24		Reserved
21	MD6	M DATA BIT 6	22	MCS0/	M CHIP SELECT 0
19	MD7	M DATA BIT 7	20		Reserved
17	GND	SIGNAL GROUND	18	+5V	+5V
15	IORD/	IO READ COMMAND	16		Reserved
13	IOWRT/	IO WRITE COMMAND	14	MINTR0	M INTERRUPT 0
11	MA0	M ADDRESS 0	12		Reserved
9		Reserved	10		Reserved
7		Reserved	8	MPRT	M PRESENT
5	RESET	RESET	6	MCLK	M CLOCK
3	GND	SIGNAL GROUND	4	+5V	+5V
1	+12V	+12V	2	-12V	-12V

8(Ra)(Cb) = 1 mS delay, therefore,

$$\text{Capacitance (Cb)} = \frac{1 \text{ mS delay}}{8(\text{Ra})}$$

Where Ra is listed in terms of ohms and Cb in terms of farads.

NOTE

When changing channels with a Cb capacitor installed onto the Multimodule board, the first conversion should be ignored and a second conversion of the same channel should be performed 1 millisecond later to obtain correct data.

Signal Ground Isolation. The signal ground may be isolated from the Multimodule board ground by removing the jumper connecting E10 to E13 and installing one from E12 to E13. This procedure eliminates a potential ground loop problem by connecting the analog signal ground directly to the input of the amplifier.

CAUTION

Ensure that the potential on your analog signal ground does not exceed ±12 volts. Failure to do so could result in damage to the amplifiers on the board.

2-10. CONNECTOR CONFIGURATION

The Multimodule board contains two connectors, the iSBX bus connector (P1) and the I/O connector (J1). Each of these is described in the following paragraphs.

The iSBX bus connector (P1) interfaces the Multimodule board to any host iSBC microcomputer that contains an iSBX bus connector. The signals found on each pin of connector P1 are listed in table 2-4 and described in Chapter 4.

The input connector (J1) interfaces the Multimodule board to the application via user-supplied analog data lines (channels). The channel input found on each pin of connector J1 is listed in table 2-5. As the table shows, the Multimodule board provides all but four signals that are present on the J2 connector of the iSBC 711 and 732 boards; the non-supported signals include Clock Out, External Trigger In, EOC Status Out, and EOS Status Out on pins 40, 42, 44, and 46 respectively. Table 2-6 contains a list of part numbers for compatible user-supplied connectors to interface to the 50-pin J1 connector on the Multimodule board.

2-11. BOARD CONFIGURATION

The Multimodule board may be configured to operate in one of four modes; single-ended with unipolar analog to digital (A-to-D) circuitry operation, single-ended with bipolar A-to-D circuitry operation, differential with unipolar A-to-D circuitry operation, and differential with bipolar A-D circuitry operation. Figure 2-4 shows a typical configuration for the Multimodule board in a single ended input application and figure 2-5 shows a typical differential input application.

Figure 2-4 shows the input stages to the Multimodule board when configured for the single-ended operation. The single ended analog channel inputs may be used with the A-to-D circuitry operating in either the unipolar or bipolar mode. The only hardware difference between the single ended bipolar and single ended unipolar A-to-D circuitry operation is that the A-to-D converter configuration changes.

The input stages for the Multimodule board configured for differential operation are shown in figure 2-5. In this configuration, the differential analog channel inputs may be used wA-to-D circuitry operating in either the unipolar or bipolar mode.

2-12. BOARD INSTALLATION

The Multimodule board mounts directly onto a host iSBC microcomputer. Figure 2-6 shows the assembly of the boards u mounting screws and spacer. Install the board as follows:

a. With a plastic screw, 1/4 by 6-32, secure the plastic 1/2 by 6-32 spacer to the host iSBC board.

b. Locate pin 1 of the iSBX bus connector (P1) on the Multimodule board and align it with pin 1 of the iSBX bus connector on the host iSBC microcomputer.

c. Align the mounting hole on the Multimodule board with the mounting spacer installed onto the host iSBC board in the first step.

d. Gently press the two boards together until the connector seats.

e. Secure the Multimodule board to the top of the spacer with another plastic 1/4 by 6-32 screw.

NOTE

The location of an installed Multimodule board and the iSBX bus connector number on the host iSBC microcomputer may vary according to the type of host iSBC microcomputer that is used.

Table 2-5. Connector J1 Pin Assignment

PIN	SINGLE-ENDED	DIFFERENTIAL	PIN	SINGLE-ENDED	DIFFERENTIAL
1	Not Used	Not Used	2	Not Used	Not Used
3	Analog Return	Analog Return	4	Channel 0	Channel 0 High
5	Analog Return	Analog Return	6	Channel 8	Channel 0 Low
7	Analog Return	Analog Return	8	Channel 1	Channel 1 High
9	Analog Return	Analog Return	10	Channel 9	Channel 1 Low
11	Analog Return	Analog Return	12	Channel 2	Channel 2 High
13	Analog Return	Analog Return	14	Channel 10	Channel 2 Low
15	Analog Return	Analog Return	16	Channel 3	Channel 3 High
17	Analog Return	Analog Return	18	Channel 11	Channel 3 Low
19	Analog Return	Analog Return	20	Channel 4	Channel 4 High
21	Analog Return	Analog Return	22	Channel 12	Channel 4 Low
23	Analog Return	Analog Return	24	Channel 5	Channel 5 High
25	Analog Return	Analog Return	26	Channel 13	Channel 5 Low
27	Analog Return	Analog Return	28	Channel 6	Channel 6 High
29	Analog Return	Analog Return	30	Channel 14	Channel 6 Low
31	Analog Return	Analog Return	32	Channel 7	Channel 7 High
33	Analog Return	Analog Return	34	Channel 15	Channel 7 Low
35	Not Used	Not Used	36	Not Used	Not Used
37	Not Used	Not Used	38	Not Used	Not Used
39	Not Used	Not Used	40	*Not Used	*Not Used
41	Not Used	Not Used	42	*Not Used	*Not Used
43	Not Used	Not Used	44	*Not Used	*Not Used
45	Not Used	Not Used	46	*Not Used	*Not Used
47	Analog Return	Analog Return	48	Analog Return	Analog Return
49	-12v	-12v	50	+12v	+12v

Note: All odd-numbered pins (1, 3,...49) are on component side of the board. Pin 1 is the right-most pin when viewed from the component side with the board extractors at the top.

An * marks those pins that are available on the iSBC 711 and 732 board interface, but not available on the Multimodule board interface.

Table 2-6. Compatible J1 Connector Details

Function	No. Of Pairs Pins	Centers (Inches)	Connector Type	Vendor	Vendor Part No.
Parallel I/O Connector	25/50	0.1	Female Flat Crimp	3M 3M AMP ANSLEY SAE	3415-0000* WITH EARS 3415-0001 W/O EARS 88083-1 609-5015 SD6750 SERIES
Parallel* I/O Connector	25/50	0.1	Female Soldered	GTE VIKING MASTERITE	6AD01-25-1A1-D0 3KH25/9JN5 NDD8GR25-DR-H-X
Parallel I/O Connector	25/50	0.1	Female Wirewrap	TI VIKING ITT CANNON	H421011-25 3KH25/JND5 EC4A050A1A

Notes: * indicates that the connector includes screw-hold flanges that may have to be removed before installation.

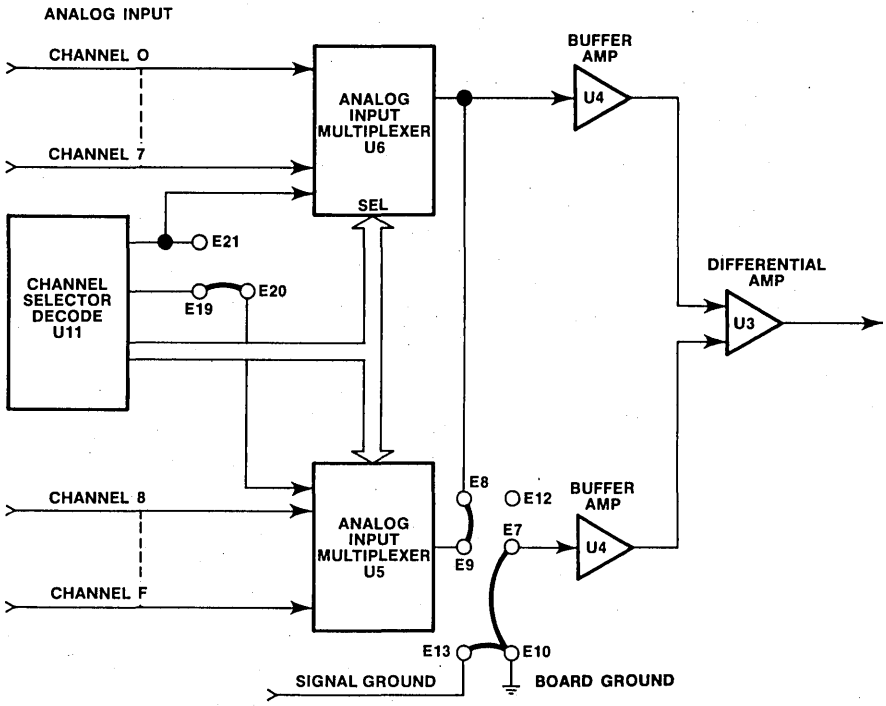


Figure 2-4. Single Ended Input Configuration

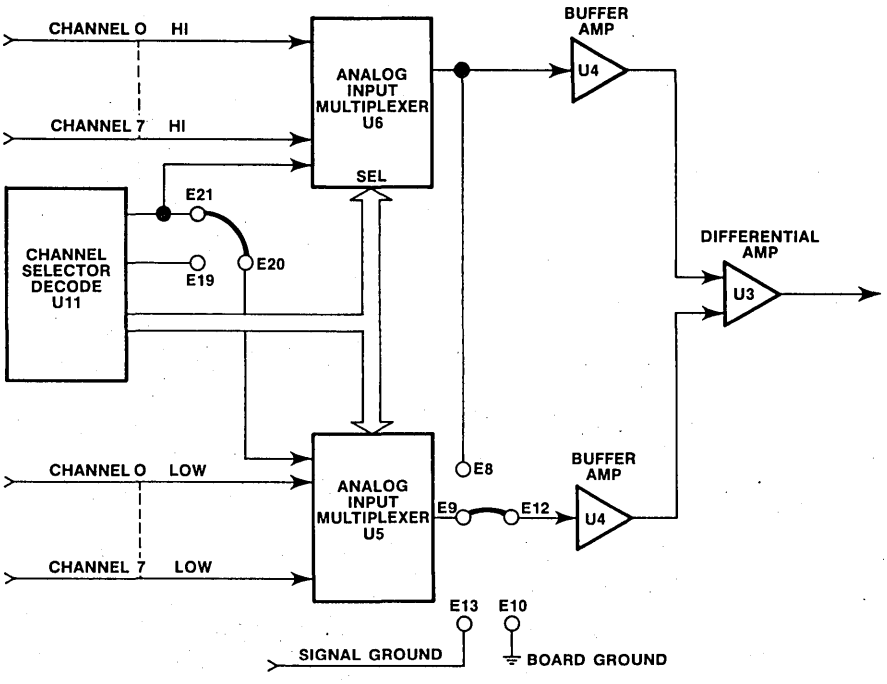


Figure 2-5. Differential Input Configuration

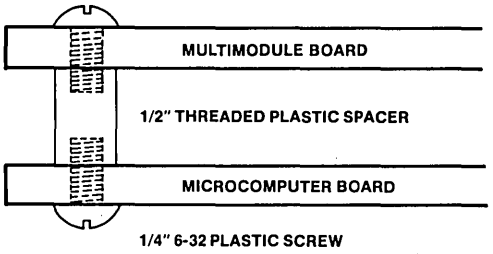


Figure 2-6. Mounting Technique

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

This chapter describes the user programming required for the iSBX 311 Analog Input Multimodule Board. Included are sections on addressing, command formats, data selection formats, interrupt servicing, and programming examples.

3-2. ADDRESSING

The Multimodule board is addressed by executing an IN or OUT instruction in the host iSBC microcomputer to one of the legal port addresses for the Multimodule board. Since some host iSBC microcomputers will accept up to three Multimodule boards, the upper address byte for each iSBX bus connector will vary, as table 3-1 shows. The port addresses vary according to whether an 8-bit board or a 16-bit board is used as the host iSBC microcomputer board.

3-3. COMMAND FORMAT

The Multimodule board is capable of responding to 2 types of commands, READ commands and WRITE commands. The READ command causes digital data (high byte, low byte, or status) to be transferred to the host iSBC microcomputer and the WRITE command transfers the channel address to the Multimodule board to select which channel will be converted. Each of the commands is issued by the host iSBC microcomputer via either an IN or an OUT instruction directed to one of the legal port addresses.

The WRITE command must select the channel on the Multimodule board which is to be converted; this consists of loading the channel selection byte into the A register before the OUT instruction is directed to one of the legal WRITE port addresses for the Multimodule board (see table 3-1). The format of the channel selection byte is shown in figure 3-1. The channel selection byte (bits C0, C1, C2, and C3) is decoded by the Multimodule board to select one of the 16 (for single ended operation) or one of 8 (for differential operation) analog input channels. The high order bits (X, X, X, X) are not used. The WRITE command is issued via an OUT instruction. When the OUT command is executed by the host iSBC microcomputer, the accumulator must contain the proper channel address, as listed in table 3-2.

When a READ command (IN instruction) is directed to one of the legal Multimodule port addresses and is decoded by the Multimodule board, the command causes converted digital data to be sent to the host iSBC microcomputer from the Multimodule board data buffers. The READ command may call for either the status of the Multimodule board, the LOW BYTE of converted data, or the HIGH BYTE of converted data. The data, recall, is the result of an analog data conversion sequence from the channel selected by the previous WRITE command. The distinction between the LOW and HIGH data bytes is performed by the port address used; refer to table 3-1.

NOTE

The RESET occurring as a result of power-on will not clear the interrupt request signal (INTRO) from the Multimodule board. Therefore, a READ HIGH BYTE command should be issued after power-up to clear the INTRO signal before starting an operation.

Table 3-1. I/O Port Addresses

FUNCTION	8-BIT PORT ADDRESS	16-BIT PORT ADDRESS	COMMENTS
READ HIGH BYTE	X0, X2, X4, or X6	X0, X4, X8, or XC	Transfer converted data from Multimodule board and resets the interrupt request line.
READ LOW BYTE and READ STATUS	X1, X3, X5, or X7	X2, X6, XA, or XE	Transfer converted data and status from Multimodule board.
WRITE CHANNEL SELECT ADDRESS	X0 through X7	X0 through XE	WRITE next channel address to Multimodule board and initiate conversion.

Note: Refer to the Hardware Reference Manual for your host iSBC microcomputer to determine the upper digit (X) of the Multimodule port address.

bit position	7	6	5	4	3	2	1	0
Channel Select Byte	X	X	X	X	C3	C2	C1	C0

Figure 3-1. Channel Selection Byte Format

bit position	7	6	5	4	3	2	1	0
LOW BYTE	D3	D2	D1	D0	0	START/	BUSY/	EOC/
HIGH BYTE	D11	D10	D9	D8	D7	D6	D5	D4

Figure 3-2. Data Format

3-4. DATA FORMAT

A READ command is issued to the multimodule board to initiate a READ operation in which converted data is sampled by the host iSBC microcomputer. The digital data created within the Multimodule board is the result of operation of the SAR, the DAC, and the comparator to transform the analog input data into 12 bits of digital data which are left-justified through two three-state multiplexers to form two 8-bit bytes of digital data. The format of the digital data bytes created by the Multimodule board is shown in figure 3-2. Bits D0 through D3 of the low byte interface to bidirectional bus lines MD4 through MD7, respectively. The low byte includes one unused bit (bit 3) and the status bits (EOC/, BUSY/, and START/ on MD0, MD1, and MD2, respectively). The high byte includes data bits D4 through D11 which are transferred on bidirectional bus lines MD0 through MD7, respectively.

3-5. STATUS FORMAT

Status for the Multimodule board is contained in the three least significant bits of the LOW BYTE of data (see figure 3-2). The status is read by the host iSBC microcomputer whenever a READ LOW BYTE command is issued by the host iSBC microcomputer to the Multimodule board. When a READ LOW BYTE command is issued, the status bits are released onto the MD0, MD1, and MD2 data lines.

The START/ status bit (bit 2) is used by the host iSBC microcomputer to determine whether or not the A-to-D converter on the Multimodule board has started data conversion. When the START/ bit is LOW, it indicates that the Multimodule board is in the process of sampling the analog data input; i.e., the A-to-D conversion is begun. When the START/ bit is HIGH, it indicates that the data sampling is completed.

Table 3-2. WRITE Commands

COMMAND*	CHANNEL** SELECTION BYTE	MODE	FUNCTION
OUT XX	00	Single Ended/Differential	Select channel 00 input.
OUT XX	01	Single Ended/Differential	Select channel 01 input.
OUT XX	02	Single Ended/Differential	Select channel 02 input.
OUT XX	03	Single Ended/Differential	Select channel 03 input.
OUT XX	04	Single Ended/Differential	Select channel 04 input.
OUT XX	05	Single Ended/Differential	Select channel 05 input.
OUT XX	06	Single Ended/Differential	Select channel 06 input.
OUT XX	07	Single Ended/Differential	Select channel 07 input.
OUT XX	08	Single Ended	Select channel 08 input.
OUT XX	09	Single Ended	Select channel 09 input.
OUT XX	0A	Single Ended	Select channel 10 input.
OUT XX	0B	Single Ended	Select channel 11 input.
OUT XX	0C	Single Ended	Select channel 12 input.
OUT XX	0D	Single Ended	Select channel 13 input.
OUT XX	0E	Single Ended	Select channel 14 input.
OUT XX	0F	Single Ended	Select channel 15 input.

Notes: * XX is any legal WRITE port address, as defined in table 3-1. Refer to the respective Hardware Reference Manual for the host iSBC microcomputer for port addresses.

** The Channel Selection Byte must be contained in the accumulator in the CPU on the host iSBC microcomputer board.

The BUSY/ status bit (bit 1) is generated by the SAR to show the condition of the successive approximation routine that occurs for each data input sequence on the Multimodule board. When the dat conversion is started, the BUSY/ signal goes LOW a maximum of 3.8 microseconds after START/ goes LOW. When the board is finished converting the analog data to digital data, BUSY/ goes HIGH, indicating that the conversion within the SAR is fully completed; i.e., data is available in the form of a HIGH BYTE and LOW BYTE.

The EOC/ status bit (bit 0) is used by the host iSBC microcomputer to determine the end of conversion when the host must determine the status of the Multimodule board by polling the status byte. The EOC/ status bit is reset by issuing a READ HIGH BYTE command to the Multimodule board. The interrupt line (INTRO) from the Multimodule board is an inverted version of the EOC/ signal and is also reset on a READ HIGH BYTE command. The interrupt line may be used to request an interrupt from the host iSBC microcomputer at the end of a conversion.

3-6. PROGRAMMING EXAMPLE

Table 3-3 contains a programming example for the Multimodule board that will read data from each of sixteen single-ended analog input channels and store the converted data in a 32-byte table in memory. A program for a differential system would be similar, with the exception that only 8 channel inputs are available. The example uses a data table to store up to 32 bytes of converted analog data input through the Multimodule board. All 16 channels are scanned, implying that the Multimodule board is configured to operate in the single ended mode. The end of a conversion cycle is sensed by polling for the EOC/ signal transition. The port addresses used in the sample program are for use with an iSBC 80/24 board (J6 Multimodule board connector) and may have to be altered if another host or another Multimodule connector is required. For proper port addresses, refer to table 3-1 of this manual.

Table 3-3. Programming Example

```
TABLE:  DS      32              ;Define data table.
HIGH    EQU     0F0H            ;High byte port
                                ;address.
LOW     EQU     0F1H            ;Low byte port
                                ;address.
ADR     EQU     0F0H            ;Channel select port
                                ;address.

ALL16:  LXI     H,TABLE + 31    ;Set data-table
                                ;pointer.
        MVI     B,15            ;Set-up channel
                                ;counter.
        IN      HIGH            ;Ensure EOC/ bit
                                ;RESET
                                ;(READ HIGH BYTE)

LOOP    MOV     A,B             ;Move next-channel
                                ;address to A.
        OUT     ADR             ;WRITE channel
                                ;address to Mtuli-
                                ;module board and
                                ;start conversion on
                                ;channel data.

INTR    IN      LOW             ;READ status byte to
                                ;check for end of
                                ;conversion.

        ANI     01H             ;Checking for EOC/
                                ;bit.
        JNZ     INTR            ;Waiting for end of
                                :conversion.
        IN      LOW             ;READ LOW BYTE of
                                ;data.
        ANI     HIGH            ;Mask off non-data
                                ;bits of low byte.

        MOV     M,A             ;Store low byte data
                                ;into table.
        DCX     H               ;Decrement memory
                                ;pointer.
        IN      HIGH            ;READ HIGH BYTE
                                ;of data from the
                                ;Multimodule board.

        MOV     M,A             ;Store high byte data
                                ;into table.
        DCR     B               ;Decrement channel
                                ;counter.
        RM                      ;Return when all 16
                                ;channels serviced.

        JMP     LOOP            ;Go to next channel.
        END
```

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a functional description of the interface signals detailing the circuit operation for the iSBX 311 Analog Input Multimodule Board. The functional description of the board includes details on the operation of each of the major components on the board, as shown in the functional block diagram in figure 4-1.

4-2. iSBX™ BUS INTERFACE SIGNAL DESCRIPTION

The Multimodule board is controlled by the signals on the iSBX bus connector. The iSBX bus signals and their functions are detailed in the following paragraphs.

RESET (Reset)—This active high signal, when asserted to the Multimodule board, clears the clock divider and interrupt request circuitry on the board. The DAC, Sample-and-Hold, and SAR devices are not directly affected by RESET.

MCLK (Clock)—This signal is derived from the host iSBC microcomputer to provide synchronous operation. MCLK is a 9 to 10 MHz clock provided by the host iSBC microcomputer. It is used by the Multimodule board to generate a 2.7 to 2.5 microsecond clock for the on-board Successive Approximation Register (SAR).

MD0-MD7 (Bidirectional data bus)—These eight bidirectional data lines provide a means of transferring commands and data to or form the Multimodule board. When not in use, the MD0-MD7 lines are held at high impedance. When both MCS0/ and IORD/ (or MCSO/ and IOWRT/) are LOW, the data lines are enabled.

IORD/ (Read Command)—This active low signal is generated by the host iSBC microcomputer as a command to the Multimodule board to input data to the host. IORD/ works with MCSO/ and MAO to enable the bidirectional data bus (MD0-MD7) for input, to reset the clock divider/interrupt request circuitry, and to select whether the low or high data byte is to be sent to the host.

IOWRT/ (Write Command)—This active low signal is generated by the host iSBC microcomputer as a command to the Multimodule board to accept data present on the bidirectional data bus. Along with MCSO/, the IOWRT/ signal causes the channel selection circuitry to be loaded with the address of the channel from which input is desired, and causes the data conversion process to begin.

MCSO/ (Select)—MCSO/ is an active low input signal to the Multimodule board to allow it to accept either an IORD/ or IOWRT/ command from the host iSBC microcomputer board. When HIGH, MCSO/ holds the bidirectional data bus in a high impedance state.

MAO (Byte Selector)—This input from the host iSBC microcomputer is used during a READ operation to select whether the data put on the bidirectional bus by the Multimodule board is to be the high or low byte of the last conversion. When MAO is LOW (along with MCSO/ and IORD/), the Multimodule board gates the HIGH BYTE (data bits D11, D10, D9, D8, D7, D6, D5, and D4) onto MD7-MD0 (respectively) to the host. When MAO is HIGH, the Multimodule board gates the LOW BYTE (data bits D3, D2, D1, D0, 0, START/, BUSY/, and INTRO/) onto MD7-MD0 (respectively); 0 indicates that the bit position is not used and may be ignored.

INTR0 (Interrupt 0)—This active high output signal provides an indication to the host iSBC microcomputer that the analog data conversion for the last channel is completed (BUSY/m0) and that service from the host iSBC microcomputer is required. The falling edge of BUSY/ advances the count in the binary counter (U8), changing the output from pin-3 to a HIGH. This output is the interrupt request signal (INTR0) from the Multimodule board and may be cleared by either a RESET pulse to U14 pin-12 or by performing a READ HIGH BYTE command decode from U14 pin-3 which is inverted to reset U8.

4-3. FUNCTIONAL DESCRIPTION

The functional description is based upon the functional block diagram shown in figure 4-1. Each functional block in the figure is explained in detail in the following paragraphs.

4-4. INPUT CHANNEL SELECTOR

Logic device U11 serves as a decoding device to determine which input chjannel to the Multimodule board is selected for output to the host iSBC

microcomputer. The channel selection byte (refer to figure 3-1) from the host is decoded into MPXA, MPXB, MPXC, MPX1, and MPX2 signals to operate the channel selector devices (U5 and U6). These signals select one of 8 differential or one of 16 single-ended analog input channels.

4-5. CHANNEL MULTIPLEXERS

The channel multiplexers (U5 and U6) receive the analog inputs from an external source. As shipped from the factory, the analog multiplexers are set up to operate in the single ended mode. In single ended mode operation, only one multiplexer is enabled on any operation to select channel data input; one of sixteen channel inputs. In differential mode operation, the Multimodule board allows both U5 and U6 to operate simultaneously in multiplexing both halves of a differential channel input signal; selection of one of eight channel inputs. As a safety feature, the multiplexers contain an internal device to protect against overvoltage surges of up to 30 volts.

4-6. OUTPUT DATA BUFFERS

The output data buffers (U12 and U13) provide an 8-bit register in which converted data for the host iSBC microcomputer can be held until requested. Depending on the command of the host, the buffers can pass either the HIGH BYTE or the LOW BYTE of the last data conversion to the host via the bidirectional bus. The buffers are held in a high impedance condition when not in use. The data in the register may be read as many times as desired, however, after reading the HIGH BYTE, the EOC/ status bit (bit 0) is reset and should be considered not valid until after the next data conversion sequence.

To pass the LOW BYTE of converted data (bits D3, D2, D1, and D0 on MD7 through MD4) and the status bits (on MD3 through MD0), the Multimodule board must sense a LOW on the IORD/ line, a LOW on MCSO/, and a HIGH on MAO. These signals enable the output buffers (U12 and U13) to operate and the MAO signal also provides the output sequencing control for the output buffers. The MAO signal is initially HIGH to select the "B" inputs to the U12 and U13 multiplexers; i.e., EOC/, BUSY/, START/, zero, D0, D1, D2, and D3 are output on data lines MD0 through MD7, respectively, to the host iSBC microcomputer.

To pass the HIGH BYTE of converted data (bits D4, D5, D6, D7, D8, D9, D10, and D11 on MD7 through MD0), the Multimodule board must sense a LOW on the IORD/ line, a LOW on MCSO/, and a LOW on MAO. When MAO goes LOW, the "A" inputs to the multiplexers (data bits D4, D5, D6, D7, D8, D9, D10, and D11) are connected to the MD0 through MD7 data lines, respectively.

4-7. SAMPLE-START PULSE GENERATOR

The monostable multivibrator (U9) is triggered at the end of the period when IOWRT/ and MCSO/ are LOW. The mutivibrator generates a 10 to 15 microsecond Sample-and-Hold (SH)pulse to sample the analog data into the Sample-and-Hold circuitry (U7) and also generates a Start-Conversion pulse (START/) to trigger the SAR to start a data conversion sequence.

4-8. BUFFER AMPLIFIERS

The two buffer amplifiers (both contained in U4) provide high impedance for the input multiplexers (U5 and U6) and for the signal source to prevent unnecessary input line lading. The buffer amplifiers also provide a low input impedance for the differential amplifier (U3).

4-9. DIFFERENTIAL AMPLIFIERS

The differential amplifier (U3) operates as a unity-gain bipolar amplifier. The amplifier provides a single-ended output that is the difference between the outputs on pin-1 and pin-7 from the buffer amplifiers (U4). The output of the amplifier feeds the gain select and offset adjust stage of U3. The amplifier includes four 0.02 percent resistors (R8, R9, R11, and R12) to provide greater than 60 db Common Mode Rejection (CMR). Capacitors C11 and C12 are included to filter high frequency noise from the data.

4-10. AMPLIFIER GAIN SELECT. The gain select is user configurable through jumper/resistor locations (E1 through E7); factory configuration includes a jumper from E5 to E6 which configures the board to a gain of one. The Multimodule board may be configured for a maximum gain of 250 by installing two resistors (Rb from E1 to E2 and Ra from E3 to E4) and removing the jumper from E5 to E6. Configuration also includes installation of filter capacitor Cb from E5 to E7 to limit the bandwidth. More jumper wiring information is contained in Chapter 2.

4-11. AMPLIFIER OFFSET ADJUST. The offset adjust resistor (R2) and resistor R10 are responsible for controlling the offset (if any) induced into the input by the two buffers, the differential amp, and the gain select circuitry. Chapter 5 of the

text includes an adjustment procedure for the offset R2). Once the offset on the channel input is corrected, the channel input is ready to be passed on to the sample-and-hold stage.

4-12. SAMPLE-AND-HOLD CIRCUITRY.

The sample-and-hold device (U7) samples the input signal on pin-3 for 15 microseconds and holds the sample for the duration of the conversion cycle. By sampling and holding the input, the Multimodule board freezes the input signal for the duration of the analog to digital (A-to-D) conversion so that a more accurate A-to-D conversion can be performed. When the sample-and-hold device senses a HIGH on pin-8 (the SH signal from U9), it samples the input on pin-3. Capacitor C9 stores the sample of the input signal voltage during the conversion.

4-13. ANALOG-TO-DIGITAL CONVERSION

The A-to-D Converter (ADC) logic on the Multimodule board consists of circuits to perform several distinct functions, including:

- a reference voltage (pin-24 of U1),
- a Digital-to-Analog Converter (U1),
- a voltage comparator (U10),
- a Successive Approximation Register—SAR (U2),
- a clock (U8),
- a DAC offset circuit (R1 and R14), and
- a Dac gain adjust circuit (R3, R5, R6, and R7).

Each of these is discussed in detail in the following paragraphs.

A voltage reference circuit of 6.3 volts within the DAC (pin-24 of U1) establishes the full-scale current reference for the DAC. More information on the DAC can be found in the data book and data sheets for the DAC device.

The DAC voltage gain adjust circuitry (R3, R5, R6, and R7) modifies the full-scale voltage reference output from the DAC by a maximum of 0.5% in order to accurately set the full-scale reading for the DAC. Chapter 5 contains a procedure for adjusting the DAC voltage gain (R3).

The DAC offset adjust circuitry (R1 and R14) establishes a true zero reading for unipolar operation or a negative full-scale reading for bipolar operation. Chapter 5 contains a procedure for adjusting the DAC offset (R1).

The SAR is a 12-bit register that sequentially tests each bit against the value in the sample and hold register. The state of each bit of the final output is successively determined by the operation of DAC, the sample-and-hold register, and the comparator circuits. The result of the operation of these ciruits builds, bit by bit, a digital data word within the SAR device. One cycle for the SAR consists of 12 successive data approximations, and each approximation determines the proper value for one data bit position within the SAR, starting with the most significant bit and ending with the least significant bit. As soon as the state of the last bit within the SAR is determined, the EOC/ signal from pin-3 of the SAR goes LOW, indicating that conversion is completed.

The voltage comparator circuitry includes some internal DAC circuitry, amplifier U10, diodes CR1 and CR2, resistor R13, and capacitor C18. For each bit of the conversion operation, the comparator circuitry compares the value held in the Sample-and-Hold register with the conversion value contained in the DAC, and with the results of the compare operations, builds a converted data word in the SAR. If U10 senses a positive current flow at pin-3, then a LOW is generated from pin-7 and fed back into the SAR on pin-11 to turn ON that particular bit of the conversion data word. Conversely, if U10 senses a negative current flow, then a HIGH is generated from pin-7 to turn OFF that bit of the conversion data word. Diodes CR1 and CR2 limit the voltage swing at the comparator in order to increase conversion speed.

4-14. CLOCK DIVIDER CIRCUITRY.

The Multimodule board includes on-board clock divider circuitry (U8) that uses the MCLK signal (9 to 10 MHz clock) from the iSBX bus connector. Device U8 divides the MCLK signal by 25 to create a CLOCK signal with a nominal 2.7 to 2.5 microsecond period. CLOCK controls the successive approximation cycle within the SAR; the nominal conversion time for one SAR cycle (12 bit approximation), including sample and hold time, is 50 microseconds.

4-15. INTERRUPT GENERATION CIRCUITRY.

When the end of conversion signal is output from the SAR device, the falling edge advances the count in U8, generating an output from pin-3 of U8 which requests an interrupt from the host iSBC microcomputer. The interrupt request from U8 remains active until cleared by reading the HIGH BYTE of data or by receiving RESET (the reset signal from the iSBX bus connector).

4-16. RESET GENERATION CIRCUITRY.

A RESET operation on the Multimodule board clears only the interrupt request line (INTRO) from U8. The RESET operation is performed through device U14 and Q1 and may be generated for the Multimodule board in one of two methods:

a. If a RESET command is issued by the host iSBC microcomputer, the command is sensed on the Multimodule board as RESET via pin-5 of the iSBX bus connector. The power-on reset will not clear the interrupt request line.

b. If a READ HIGH BYTE command is issued to the Multimodule board to input the upper byte of the data word, U14 pin-3 generates a pulse which is inverted by Q2 to reset U8, clearing the interrupt request line (INTRO) from U8. The READ HIGH BYTE command also clears the interrupt request line during initialization.

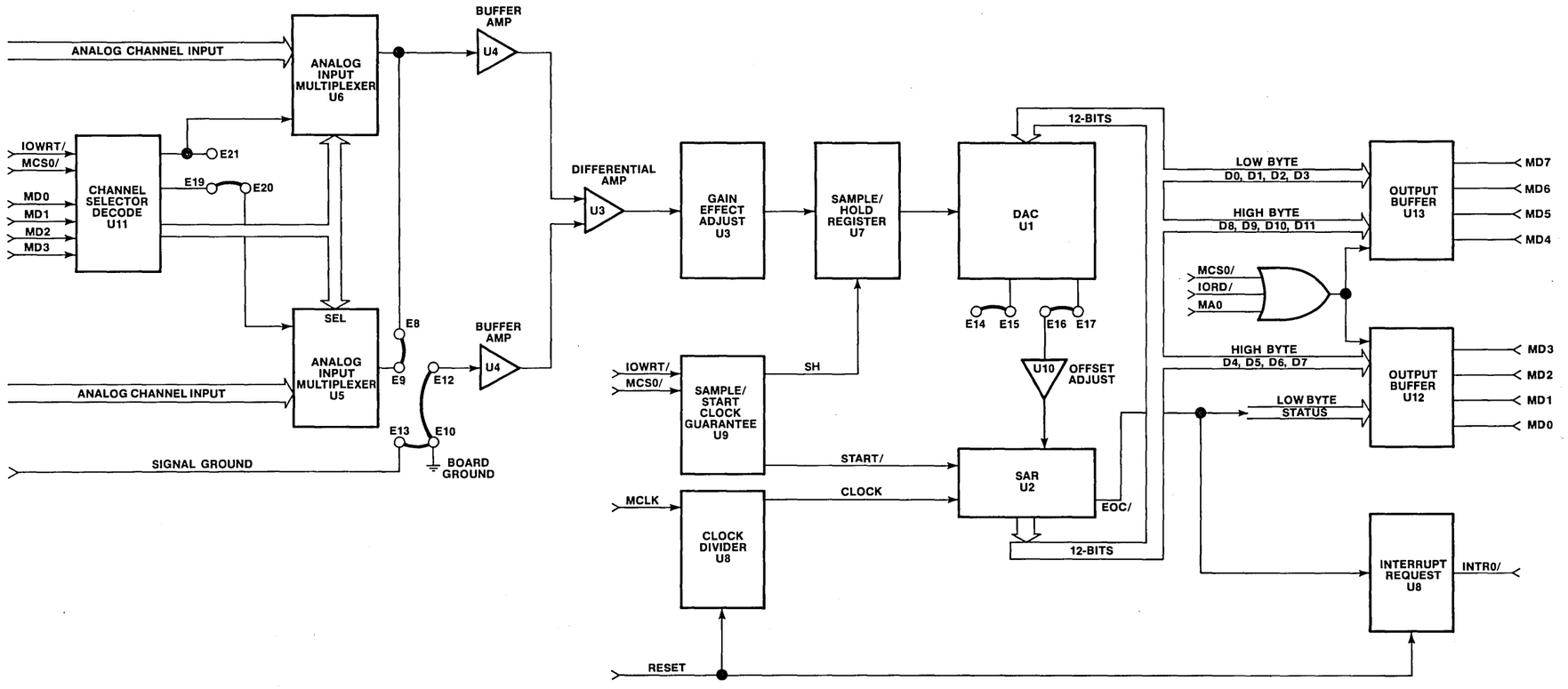


Figure 4-1. iSBX 311™ Board Functional Block Diagram (Single-Ended - Unipolar Operation)

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides a list of replaceable parts, service diagrams, adjustment procedures, and service and repair assistance instructions for the iSBX 311 Analog Input Multimodule Board.

5-2. SERVICE AND REPAIR ASSISTANCE

United States Customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Offices or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.
b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other MCSD products, it is usually stamped on a label.
c. Serial number of product. On boards, this number is usually stamped on the board. On other MCSD products, the serial number is usually stamped on a label.
d. Shipping and billing addresses.
e. If your Intel product warranty has expired, you must provide a purchase order number for billing purposes.
f. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Use the following telephone numbers for contacting the Intel Product Service Hotline:

All U.S. locations, except Alaska, Arizona & Hawaii: (800) 528-0595

All other locations: (602) 869-4600

TWX Number: (910) 951-1330

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

5-3. ADJUSTMENT PROCEDURE

The adjustments for the iSBX 311 Analog Input Multimodule Board include facilities for user-performed offset and voltage gain adjustments. The procedures are outlined in the following paragraphs. Each Multimodule board is adjusted at the factory, however, the boards should be readjusted on installation, and whenever reconfiguration occurs.

5-4. TEST EQUIPMENT REQUIRED

The test equipment required to adjust the gain and offset for the Multimodule board is as follows:

a. Digital Voltmeter with a voltage range of 0 to 15 volts and accuracy of ±0.005% or better.

b. Precision voltage source; 0 to 15 volts dc ±0.001%, continuously adjustable; source impedance less than 1.0 ohm.

5-5. PRELIMINARY PROCEDURE

Before beginning the calibration procedure, install the Multimodule board onto a host iSBC microcomputer and verify the voltage levels of the dc supply voltages as per table 5-1. If any of the voltage levels are out of tolerance, they should be readjusted before the calibration procedure is performed.

Table 5-1. Power Supply Voltage Requirements

Supply	Tolerance	Voltmeter Connection
+12	±5%	Across C23
-12	±5%	Across C24
+ 5	‖5%	Across C21
Note: Refer to figure 5-1 for capacitor locations.		

5-6. A-TO-D CONVERTER (ADC) CIRCUITRY CALIBRATION PROCEDURE. The calibration procedure for the A-to-D Converter (ADC) circuits consists of a sequence of three steps which must be performed in the following order: (1) amplifier offset adjustment, (2) ADC offset adjustment, and (3) ADC range adjustment. These adjustments are explained in the following paragraphs. However, be aware that the procedures outlined in the text assume that the calibration programs are run on a microcomputer system that includes a monitor screen and that contains a host microcomputer board within the microcomputer system, and further assumes that an ADC offset (ADCOFF) subroutine and an ADC range (ADCRNG) subroutine are in the resident program. Appendix A of this manual includes an example of typical programs to use when adjusting the ADC range and offset.

NOTE

The calibration procedures are call for adjusting the channel 0 input. Once channel 0 is adjusted properly, it may be safely assumed that the remaining channels are adjusted properly.

5-7. AMPLIFIER OFFSET ADJUST PROCEDURE. Adjust the amplifier offset as follows:

a. Short input channel 0 by connecting J2 pin 4 to J2 pin 3 (if in differential mode, also short J2 pin 6 to J2 pin 4).

b. Set the DVM to the most sensitive dc voltage scale. Then, connect the positive lead of the DVM to E22 and the negative lead to jumper post E18.

c. Call the ADCOFF subroutine and adjust the R2 resistor to give a 0 volts reading on the DVM.

5-8. ADC OFFSET ADJUSTMENT PROCEDURE. After the amplifier is adjusted, adjust the ADC offset as follows:

a. Connect the precision voltage source to the connection points required for channel 0 as listed in table 5-2.

b. Set the voltage source for the appropriate offset input as required for the ADC range being used; refer to table 5-3.

c. Call the ADCOFF subroutine and adjust the R1 resistor until the readings on the monitor alternate equally between 000 and 001, as listed in table 5-3.

Table 5-2. ADC Offset and Range Adjustment Test Input

Voltage Input	Source Connection	
	Single-ended	Differential
High	J2 pin 4	J2 pin 4
Low	J2 pin 3	J2 pin 6
Ground	J2 pin 3	J2 pin 3

Table 5-3. Voltage Source Input Required for ADC Offset and Range Adjustment

Operating Mode	Offset Adjust Reading	Range Adjust Reading
0 to +5 volts	0.00061 volts	4.9982 volts
±5 volts	-4.9988 volts	4.9963 volts

5-9. ADC RANGE ADJUST PROCEDURE. After the amplifier offset and ADC offset adjustments are made, adjust the ADC range as follows:

a. Connect a precision voltage source to the connection points for channel 0 input, as listed in table 5-2.

b. Set the precision voltage source to the appropriate range input as required for the ADC range being used; refer to table 5-3.

c. Call t he ADCRNG subroutine and adjust the R3 resistor until the readings on the monitor alternate equally between FFEH and FFFH, as listed in table 5-3.

5-10. REPLACEABLE PARTS

Table 5-4 provides a list of replaceable parts for the Multimodule board. Table 5-5 identifies and locates the manufacturers specified in the MFR CODE column of table 5-4. Intel parts that are available on the open market are listed in the MFR CODE column as "COML". Every effort should be made to procure these parts from a local (commercial) distributor.

Table 5-4. Replaceable Parts

Reference Designator	Description	Mfr. Part No.	Mfr. Code	Qty.
U9	IC, Monostable Multivibrator	74121	TI	1
U11	IC, Quad D-type Flip-Flop	74175	TI	1
U12, U13	IC, Quad 2-to-1 Multiplexer	74LS258A	TI	2
U14	IC, Quad 2-input OR	74LS32	TI	1
U8	IC, Dual 4-bit Counter	74LS390	TI	1
U5, U6	IC, 8-to-1 Analog Multiplexer	HI-3-508-A-5	TI	2
U3, U4	IC, Dual Op. Amplifier	LF353BN	NAT	2
U7	IC, Sample and Hold Register	LF398N	NAT	1
U2	IC, Successive Approx. Register	AM2504CN	ADV	1
U1	IC, Digital To Analog Converter	AD-DAC-80Z-CBI-I	ANA	1
U10	IC, Comparator	LM311N	ADV	1
R4	Resistor, 1.1K, ¼W, 5%	OBD	COML	1
R7	Resistor, 39.2K, ⅛W, 1%	OBD	COML	1
R12	Resistor, 2.5323K, 1/20W, 0.02%, 10PPM	OBD	COML	1
R13	Resistor, 3.9K, ⅛W, 5%	OBD	COML	1
R14	Resistor, 681K, ⅛W, 1%	OBD	COML	1
R15	Resistor, 150 ohm, ¼W, 5%	OBD	COML	1
R5, R6, R10	Resistor, 196K, ⅛W, 1%	OBD	COML	3
R8, R9, R11	Resistor, 2.5K, 1/20W, 0.02%, 10PPM	OBD	COML	3
R1, R2, R3	Resistor, 20K, ½W, 16 turn	3262X-203	BRN	3
RP2	Resistor Pack, 10K, 10 pin SIP, 9R	4310R-101-103	BRN	1
RP1	Resistor Pack, 1K, 6 pin SIP, 3R	4306R-102-102	BRN	1
C1	Capacitor, cer., 0.01μF, 50V, +80%, -20%	OBD	COML	1
C8	Capacitor, cer., 0.001μF, 50V, 10%	OBD	COML	1
C17	Capacitor, cer., 1800pF, 50V, 10%	OBD	COML	1
C18	Capacitor, cer., 33pF, 50V, 5%	OBD	COML	1
C22	Capacitor, cer., 0.1μF, 50V, +80%, -20%	OBD	COML	1
C25	Capacitor, dg., 0.01μF, 50V, +80%, -20%	OBD	COML	1
C5, C7, C12, C13, C16, C19, C20	Capacitor, dg., 0.1μF, 50V, +80%, -20%	OBD	COML	7
C10, C11, C14, C15	Capacitor, dg., 220pF, 50V, 10%	OBD	COML	4
C2, C3, C4, C6, C9	Capacitor, cer., 1μF, 50V, +80%, -20%	OBD	COML	5
C21	Capacitor, tant., 33μF, 10V, ±20%	OBD	COML	1
C23, C24	Capacitor, tant., 15μF, 20V, ±20%	OBD	COML	2
CR1, CR2	Diode HP2811	OBD	COML	2
VR1	Diode, zener 1N4567	OBD	COML	1
Q1	Transistor, PNP 2N4403	OBD	COML	1
	Shorting Plugs	530153-2	AMP	5
	Socket, SIP, 12-pin	7195-295-5	EMC	4
	Socket, SIP, 8-pin	7195-295-5	EMC	2
	Socket, SIP, 4-pin	7195-295-5	EMC	4
P1	Connector, 36-pin	000292-0001	VIK	1
E8-E22	Stake pins, brass	87623-1	AMP	15

Table 5-5. Manufacturer Codes

Mfr. Code	Manufacturer	Address
AMP	AMP Incorporated	Harrisburg, PA
ADV	Advanced Microdevices	Sunnyvale, CA
ANA	Analog Devices	Norwood, MA
BRN	Bourns, Inc.	Riverside, CA
EMC	EMC Technology, Inc.	Cherry Hill, NJ
HEW	Hewlett Packard	Palo Alto, CA
Intel	Intel Corporation	Santa Clara, CA
MOT	Motorola	Franklin Park, IL
TI	Texas Instruments	Dallas, TX
VIK	Viking Connectors, Inc.	Chatsworth, CA
COML	Available from any commercial distributor; Order by description (OBD).	

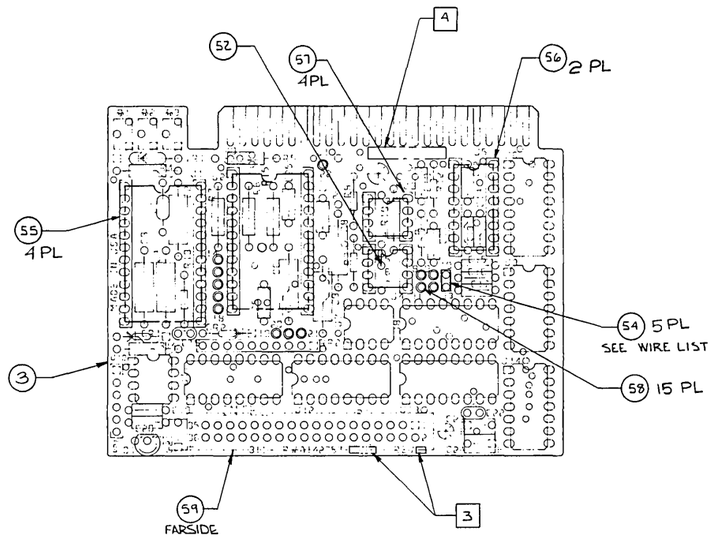
5-11. SERVICE DIAGRAMS

The parts location diagram and schematic diagrams for the Multimodule board are provided in Figures 5-1 and 5-2, respectively. On the schematic diagram, a signal mnemonic that ends with a slash (e.g., MCSO/) is active LOW. Conversely, a signal mnemonic without the slash (e.g., OPTO) is active HIGH.

DWG NO. 142757 | SH 1 | REV C

REVISIONS

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
	C	ECO 40-2167	[illegible]	[illegible]	1/15/81	[illegible]



NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PART NUMBER IS 142757-002. THIS DOCUMENT, PARTS LIST AND WIRE LIST ARE TRACKING DOCUMENTS.
2. WORKMANSHIP PER 99-0007-001.
3. MARK WITH ASSEMBLY DASH NUMBER AND REVISION LEVEL WITH PERMANENT CONTRASTING COLOR, .12 HIGH, NON-CONDUCTIVE, APPROXIMATELY WHERE SHOWN.
4. MARK VENDOR I.D. WITH PERMANENT CONTRASTING COLOR, .12 HIGH, NON-CONDUCTIVE, APPROXIMATELY WHERE SHOWN.
5. STAKE PINS ARE PREFIXED WITH "E" OMITTED DUE TO SPACE LIMITATIONS.

ITEM NO.	PART NUMBER	DESCRIPTION

PARTS LIST

QUANTITY PER DASH NO.

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES:
ANGLES ± 2°
XX ± .030
XXX ± .010
SURFACE FINISH √

SIGNATURE		DATE
DRN BY	[illegible]	9-30-80
CHK BY	[illegible]	10/31/80
ENGR APVD	[illegible]	10/1/80
APVD		
APVD		

intel® 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE
PRINTED WIRING ASSEMBLY
ANALOG INPUT MULTIMODULE

SIZE	CODE	CLASS	DWG. NO.	REV
D	40	05	142757	C

SCALE NONE SHEET 1 OF 1

NEXT ASSY | USED ON

9300021

Figure 5-1. iSBX 311™ Analog Input Multimodule™ Board Parts Location Diagram

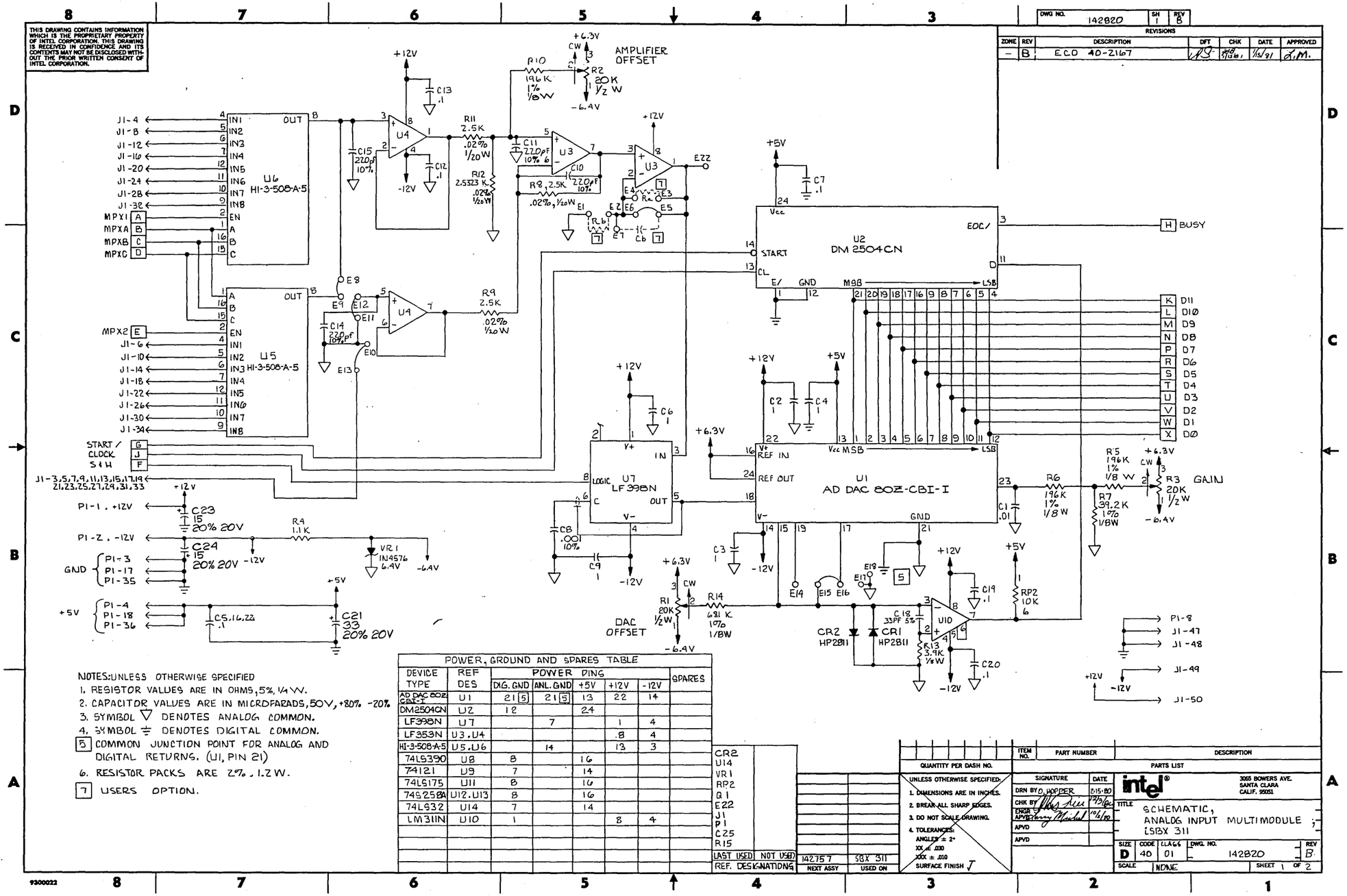


Figure 5-2. iSBX 311™ Analog Input Multimodule™ Board Schematic Diagram (Sheet 1 of 2)

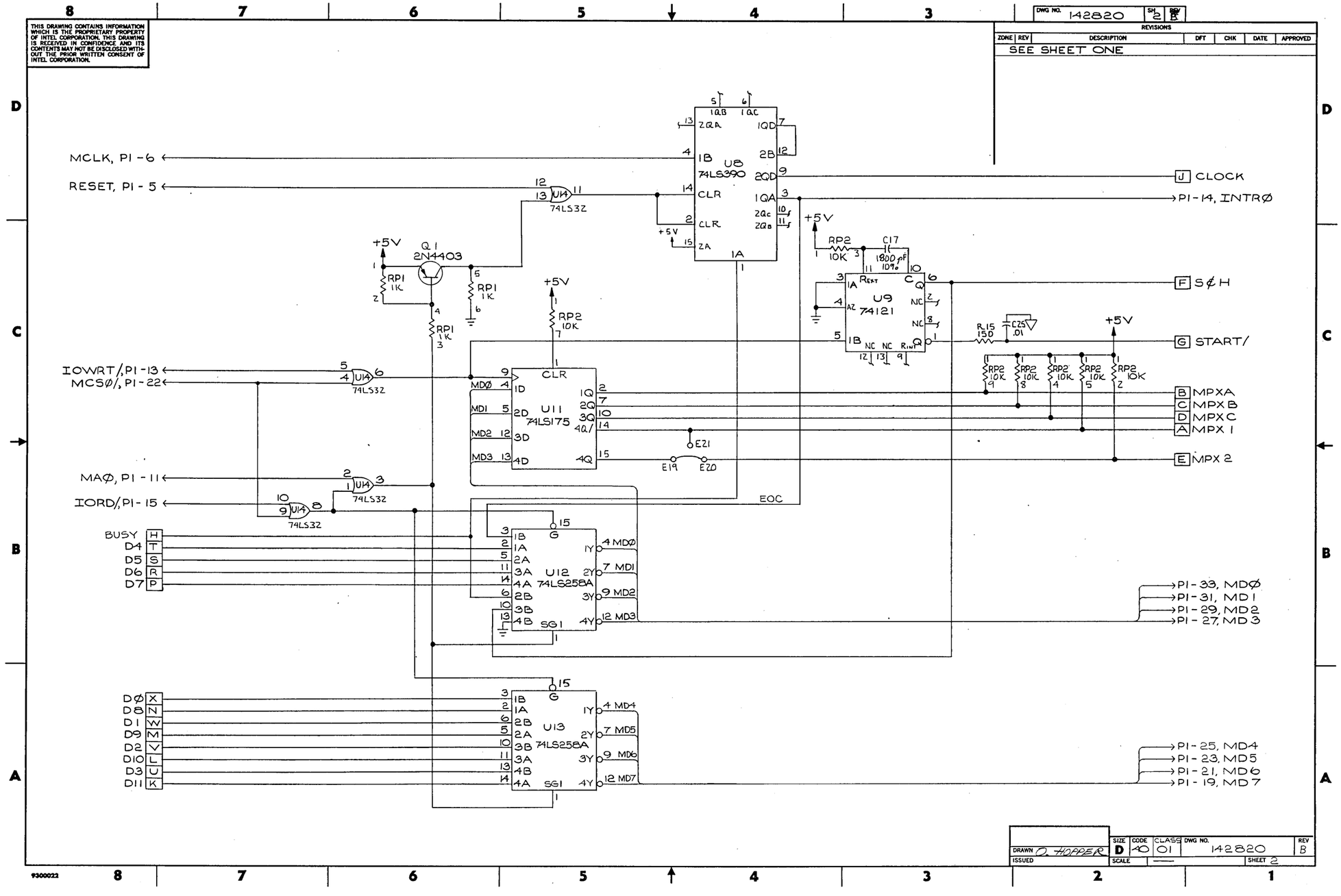


Figure 5-2. iSBX 311™ Analog Input Multimodule™ Board Schematic Diagram (Sheet 2 of 2)

APPENDIX A
CALIBRATION PROGRAMS

The calibration program presented in this appendix is intended to show a typical approach to programming the iSBX 311 Analog Input Multimodule Board when calibrating the ADC as explained in Chapter 5 of this text. The program contains port addresses that are valid for an iSBC 80/24 board with the Multimodule board mounted onto the J6 Multimodule connector. If a different configuration is required, refer to the hardware reference manual for the host iSBC microcomputer to determine the proper port addresses.

```
EXTRN     DBYTE,RXRDY
CSEL      EQU   OFOH    ;Channel select port address.
LOW       EQU   OF1H    ;LOW data byte port address.
HIGH      EQU   OF0H    ;HIGH data byte port address.
STATUS    EQU   OF1H    ;STATUS byte port address.
CSEG
ADCOFF:
ADCRNG:   MVI   A,O     ;Select channel 0.
          OUT   CSEL    ;Start conversion on channel 0.
EOC:      IN    LOW     ;READ LOW BYTE (status) from Multimodule board.
          ANI   01      ;Mask for EOC/ status bit.
          JNZ   EOC     ;Wait until EOC/.
          IN    HIGH    ;READ HIGH BYTE of data from Multimodule board.
          MOV   C,A     ;Save in C register.
          CALL  DBYTE   ;Output HIGH BYTE to console output device.
          IN    LOW     ;READ LOW BYTE of data from the Multimodule board.
          MOV   C,A     ;Save in C register.
          CALL  DBYTE   ;Output LOW BYTE to console output device.
          MVI   C,(cr)  ;Prepare a carriage return character.
          CALL  CO      ;Output carriage return to console output device.
          MVI   C,(1f)  ;Prepare a line feed character.
          CALL  CO      ;Output line feed to console output device.
          IN    CRTS    ;Check the status byte of the console device for halt request from
                        operator.
          ANI   RXRDY   ;Mask for keyboard input request.
          JZ    ADCRNG  ;No input request sensed, perform calibration test again.
          RET           ;Input request sensed from console device, exit calibration routine.
```

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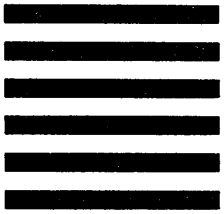

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