82077SL
CHMOS SINGLE-CHIP FLOPPY DISK CONTROLLER

- **Completely Compatible with Industry Standard 82077AA**
- **Single-Chip Laptop Desktop Floppy Disk Controller Solution**
  - **— 100% PC AT* Compatible**
  - **— 100% PS/2* Compatible**
  - **— 100% PS/2 Model 30 Compatible**
  - **— Fully Compatible with Intel's 386SL Microprocessor SuperSet**
  - **— Integrated Drive and Data Bus Buffers**
- **Power Management Features**
  - **— Application Software Transparency**
  - **— Programmable Powerdown Command**
  - **— Auto Powerdown and Wakeup Modes**
  - **— Two External Power Management Pins**
  - **— Typical Power Consumption in Power Down; Less than 95 μA**
- **High Speed Processor Interface**
- **Integrated Analog Data Separator**
  - **— 250 Kbits/sec**
  - **— 300 Kbits/sec**
  - **— 500 Kbits/sec**
  - **— 1 Mbits/sec**
- **Programmable Crystal Oscillator for On or Off**
- **Perpendicular Recording Support**
- **12 mA Host Interface Drivers, 40 mA Disk Drivers**
- **Four Fully Decoded Drive Select and Motor Signals**
- **Programmable Write Precompensation Delays**
- **Addresses 256 Tracks Directly, Supports Unlimited Tracks**
- **16 Byte FIFO**
- **68-Pin PLCC**

The 82077SL, a 24 MHz crystal, a resistor package, and a device chip select implements a complete laptop solution. All programmable options default to 82077AA compatible values. The dual PLL data separator has better performance than most board level/discrete PLL implementations. The FIFO allows better system performance in multi-master systems (e.g., Microchannel, EISA).

The 82077SL is a superset of 82077AA. The 82077SL incorporates power management features while maintaining complete compatibility with the 82077AA/8272A floppy disk controllers. It contains programmable power management features while integrating all of the logic required for floppy disk control. The power management features are transparent to any application software. There are two versions of 82077SL floppy disk controllers, the 82077SL and 82077SL-5. The only difference between the two products is that the 82077SL supports 1 Mbps data rate for the higher 4 MB density floppy disk drives and 82077SL-5 supports 500/300/250 Kbps data rate for high and low density floppy disk drives.

The 82077SL is fabricated with Intel's advanced CHMOS III technology and is available in a 68-lead PLCC (plastic) package.

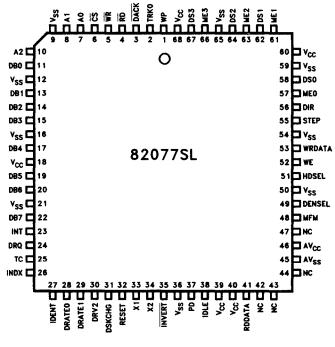

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Figure 1. 82077SL Pinout

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82077SL CHMOS Single-Chip Floppy Disk Controller

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Table 1. 82077SL Pin Description

Symbol	Pin#	I/O	Description
HOST INTERFACE			
RESET	32	I	**RESET:** A high level places the 82077SL in a known idle state. All registers are cleared except those set by the Specify command.
$\overline{CS}$	6	I	**CHIP SELECT:** Decodes base address range and qualifies $\overline{RD}$ and $\overline{WR}$ inputs.
A0 A1 A2	7 8 10	I	**ADDRESS:** Selects one of the host interface registers:

A2	A1	A0	Access Type	Register	
0	0	0	R	Status Register A	SRA
0	0	1	R	Status Register B	SRB
0	1	0	R/W	Digital Output Register	DOR
0	1	1		Reserved	
1	0	0	R	Main Status Register	MSR
1	0	0	W	Data Rate Select Register	DSR
1	0	1	R/W	Data (First In First Out)	FIFO
1	1	0		Reserved	
1	1	1	R	Digital Input Register	DIR
1	1	1	W	Configuration Control Register	CCR

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	11 13 14 15 17 19 20 22	I/O	**DATA BUS:** Data bus with 12 mA drive
$\overline{RD}$	4	I	**READ:** Control signal
$\overline{WR}$	5	I	**WRITE:** Control signal
DRQ	24	O	**DMA REQUEST:** Requests service from a DMA controller. Normally active high, but goes to high impedance in AT and Model 30 modes when the appropriate bit is set in the DOR.
$\overline{DACK}$	3	I	**DMA ACKNOWLEDGE:** Control input that qualifies the $\overline{RD}$, $\overline{WR}$ inputs in DMA cycles. Normally active low, but is disabled in AT and Model 30 modes when the appropriate bit is set in the DOR.
TC	25	I	**TERMINAL COUNT:** Control line from a DMA controller that terminates the current disk transfer. TC is accepted only while $\overline{DACK}$ is active. This input is active high in the AT, and Model 30 modes and active low in the PS/2™ mode.
INT	23	O	**INTERRUPT:** Signals a data transfer in non-DMA mode and when status is valid. Normally active high, but goes to high impedance in AT, and Model 30 modes when the appropriate bit is set in the DOR.
X1 X2	33 34		**CRYSTAL 1,2:** Connection for a 24 MHz fundamental mode parallel resonant crystal. X1 may be driven with a MOS level clock and X2 would be left unconnected.

Table 1. 82077SL Pin Description (Continued)

<table>
<tr><th>Symbol</th><th>Pin#</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE (Continued)</td></tr>
<tr><td>IDENT</td><td>27</td><td>I</td><td>IDENTITY: Upon Hardware RESET, this input (along with MFM pin) selects between the three interface modes. After RESET, this input selects the type of drive being accessed and alters the level on DENSEL. The MFM pin is also sampled at Hardware RESET, and then becomes an output again. Internal pull-ups on MFM permit a no connect.
<table>
<tr><th>IDENT</th><th>MFM</th><th>INTERFACE</th></tr>
<tr><td>1</td><td>1 or NC</td><td>AT Mode</td></tr>
<tr><td>1</td><td>0</td><td>ILLEGAL</td></tr>
<tr><td>0</td><td>1 or NC</td><td>PS/2 Mode</td></tr>
<tr><td>0</td><td>0</td><td>Model 30 Mode</td></tr>
</table>
AT MODE: Major options are: enables DMA Gate logic, TC is active high, Status Registers A & B not available.
PS/2 MODE: Major options are: No DMA Gate logic, TC is active low, Status Registers A & B are available.
MODEL 30 MODE: Major options are: enable DMA Gate logic, TC is active high, Status Registers A & B available.
After Hardware reset this pin determines the polarity of the DENSEL pin. IDENT at a logic level of "1", DENSEL will be active high for high (500 Kbps/1 Mbps) data rates (typically used for 5.25″ drives). IDENT at a logic level of "0", DENSEL will be active low for high data rates (typically used for 3.5″ drives). This assumes the $\overline{\text{INVERT}}$ pin to be tied to ground.</td></tr>
<tr><td colspan="4">DISK CONTROL (All outputs have 40 mA drive capability)</td></tr>
<tr><td>$\overline{\text{INVERT}}$</td><td>35</td><td>I</td><td>INVERT: Strapping option. Determines the polartity of all signals in this section. Should be strapped to ground when using the internal buffers and these signals become active LOW. When strapped to VCC, these signals become active high and external inverting drivers and receivers are required.</td></tr>
<tr><td>ME0
ME1
ME2
ME3</td><td>57
61
63
66</td><td>O</td><td>ME0–3: Decoded Motor enables for drives 0–3. The motor enable pins are directly controlled via the Digital Output Register.</td></tr>
<tr><td>DS0
DS1
DS2
DS3</td><td>58
62
64
67</td><td>O</td><td>DRIVE SELECT 0–3: Decoded drive selects for drives 0–3. These outputs are decoded from the select bits in the Digital Output Register and gated by ME0–3.</td></tr>
<tr><td>HDSEL</td><td>51</td><td>O</td><td>HEAD SELECT: Selects which side of a disk is to be used. An active level selects side 1.</td></tr>
<tr><td>STEP</td><td>55</td><td>O</td><td>STEP: Supplies step pulses to the drive.</td></tr>
<tr><td>DIR</td><td>56</td><td>O</td><td>DIRECTION: Controls the direction the head moves when a step signal is present. The head moves toward the center if active.</td></tr>
<tr><td>WRDATA</td><td>53</td><td>O</td><td>WRITE DATA: FM or MFM serial data to the drive. Precompensation value is selectable through software.</td></tr>
<tr><td>WE</td><td>52</td><td>O</td><td>WRITE ENABLE: Drive control signal that enables the head to write onto the disk.</td></tr>
<tr><td>DENSEL</td><td>49</td><td>O</td><td>DENSITY SELECT: Indicates whether a low (250/300 Kbps) or high (500 Kbps/1 Mbps) data rate has been selected.</td></tr>
<tr><td>DSKCHG</td><td>31</td><td>I</td><td>DISK CHANGE: This input is reflected in the Digital Input Register.</td></tr>
</table>

Table 1. 82077SL Pin Description (Continued)

Symbol	Pin#	I/O	Description
DISK CONTROL (All outputs have 40 mA drive capability) (Continued)			
DRV2	30	I	**DRIVE2:** This indicates whether a second drive is installed and is reflected in Status Register A.
TRK0	2	I	**TRACK0:** Control line that indicates that the head is on track 0.
WP	1	I	**WRITE PROTECT:** Indicates whether the disk drive is write protected.
INDX	26	I	**INDEX:** Indicates the beginning of the track.
PLL SECTION			
RDDATA	41	I	**READ DATA:** Serial data from the disk. INVERT also affects the polarity of this signal.
MFM	48	I/O	**MFM:** At Hardware RESET, aids in configuring the 82077SL. Internal pull-up allows a no connect if a "1" is required. After reset this pin becomes an output and indicates the current data encoding/decoding mode (Note: If the pin is held at logic level "0" during hardware RESET it must be pulled to "1" after reset to enable the output. The pin can be released on the falling edge of hardware RESET to enable the output). MFM is active high (MFM). MFM may be left tied low after hardware reset, in this case the MFM function will be disabled.
DRATE0 DRATE1	28 29	O	**DATARATE0–1:** Reflects the contents of bits 0,1 of the Data Rate Register. (Drive capability of +6.0 mA @ 0.4V and −4.0 mA @ 2.4V)
IDLE	38	O	**IDLE:** This pin indicates that the part is in the IDLE state and can be powered down. IDLE state is defined as MSR = 80H, INT = 0, and the head being "unloaded" (as defined in Section 6.2.6). Whenever the part is in this state, IDLE pin is active high. If the part is powered down by the Auto Mode, IDLE pin is set high and if the part is powered down by setting the DSR POWERDOWN bit, IDLE pin is set low.
PD	37	O	**POWERDOWN:** This pin is active high whenever the part is in powerdown state, either via DSR POWERDOWN bit or via the Auto Mode. This pin can be used to disable external oscillator's output.
MISCELLANEOUS			
VCC	18 39 40 60 68		**Voltage:** +5V
GND	9 12 16 21 36 50 54 59 65		**Ground**
AVCC	46		**Analog Supply**
AVSS	45		**Analog Ground**
NC	42 43 44 47		**No Connection:** These pins **MUST** be left unconnected.

1.0 INTRODUCTION

The 82077SL is a single-chip floppy disk controller for portable PC designs, PC-AT™, Microchannel™ and EISA systems. The 82077SL includes all the power management features necessary to implement a powerful laptop and notebook solution. The 82077SL is fully compatible with the 82077AA. The pin out remains the same with the exception of two new powerdown status pins, PD and IDLE. These pins will replace the LOFIL and HIFIL pins on the 82077AA that are used to connect an external capacitor.

The 82077SL, a 24 MHz crystal, a resistor package and a chip select implement a complete design. The power management features of the 82077SL are designed to be transparent to all application software. The 82077SL will seem awake to the software even when it is in powerdown mode. All drive control signals are fully decoded and have 40 mA drive buffers with selectable polarity. Signals returned from the drive are sent through on-chip input buffers with hysteresis for noise immunity. The integrated analog data separator needs no external compensation of components, yet allows for wide motor variation with exceptionally low soft error rates. The microprocessor interface has 12 mA drive buffers on the data bus plus 100% hardware register compatibility for PC-AT™ and Microchannel™ systems. The 16-byte FIFO with programmable thresholds is extremely useful in multi-master systems (Microchannel™, EISA) or systems with large bus latency.

Upon hardware reset, (Pin 32) the 82077SL defaults to 8272A functionality. Figure 1-1 is a block diagram of the 82077SL.

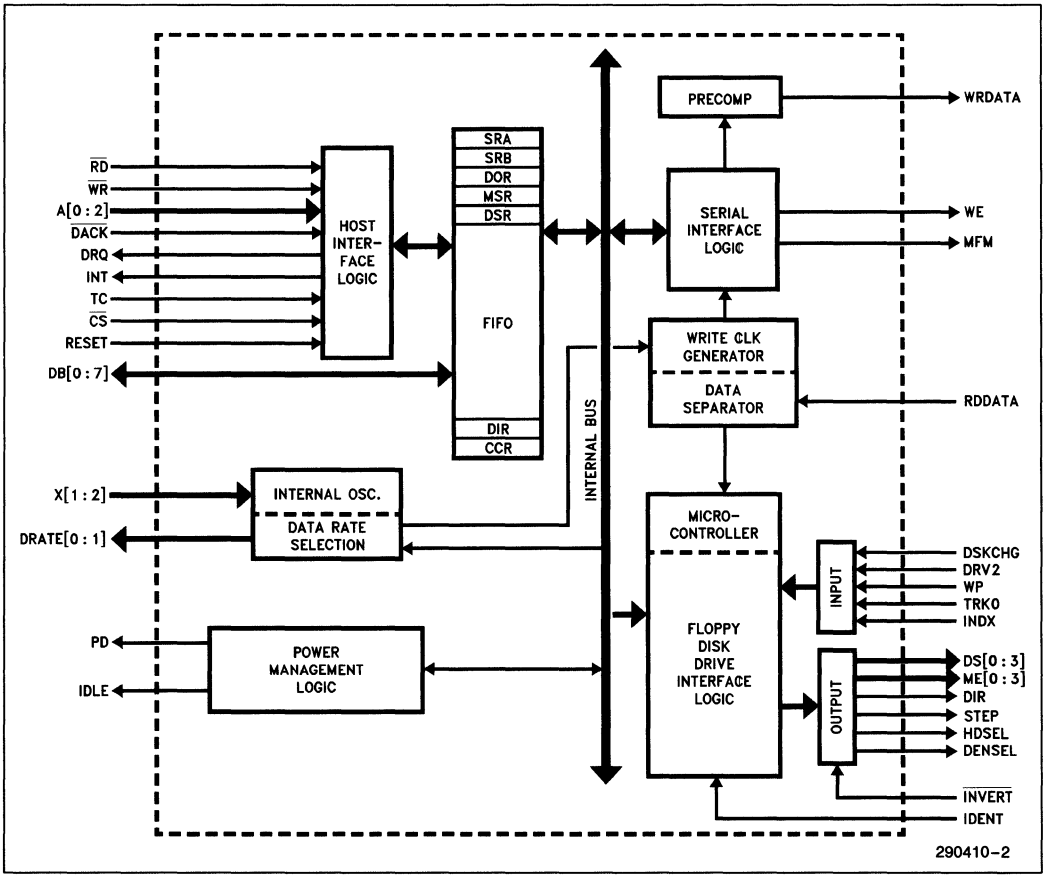


Figure 1-1. 82077SL Block Diagram

1.1 Perpendicular Recording Mode

An added capability of the 82077SL is the ability to interface directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method by orienting the magnetic bits vertically. This scheme packs in more data bits for the same area.

The 82077SL with perpendicular recording drives can read standard 3.5" floppies as well as read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the 82077SL into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires the 1 Mbps data rate of the 82077SL. At this data rate, the FIFO eases the host interface bottleneck due to the speed of data transfer to or from the disk.

1.2 Power Management Scheme

While maintaining compatibility with 82077AA, the 82077SL contains a powerful set of features for conserving power. This enables the 82077SL to play an important role in the power sensitive environment of portable personal computers. These features are transparent to any application software.

The 82077SL supports two powerdown modes—direct powerdown and automatic powerdown. Direct powerdown refers to direct action by the software to powerdown without dependence on external factors. Automatic powerdown results from 82077SL's monitoring of the current conditions according to a previously programmed mode. The 82077SL contains a new powerdown command that via programming can be used to invoke auto powerdown. 82077SL is powered down whenever a set of conditions are satisfied. Any hardware reset disables the automatic powerdown command. Software resets have no effect on the POWERDOWN command parameters.

The 82077SL also supports powerdown of its internal crystal oscillator independent of the powerdown modes described above. By setting bit 5 in DSR register, the internal oscillator is turned off. This bit has sole control of the oscillator powerdown. This allows the internal oscillator to be turned off when an external oscillator is used.

2.0 MICROPROCESSOR INTERFACE

The interface consists of the standard asynchronous signals: $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0–A2, INT, DMA control and a data bus. The address lines select between configuration registers, the FIFO and control/status registers. This interface can be switched between PC AT, Model 30, or PS/2™ normal modes. The PS/2™ register sets are a superset of the registers found in a PC-AT.

2.1 Status, Data and Control Registers

As shown below, the base address range is supplied via the $\overline{CS}$ pin. For PC-AT™ or PS/2™ designs, the primary and secondary address ranges are 3F0 Hex to 37F Hex and 370 Hex to 377 Hex respectively.

A2	A1	A0	Access Type	Register	
0	0	0	R	Status Register A	SRA
0	0	1	R	Status Register B	SRB
0	1	0	R/W	Digital Output Register	DOR
0	1	1		Reserved	
1	0	0	R	Main Status Register	MSR
1	0	0	W	Data Rate Select Register	DSR
1	0	1	R/W	Data (First In First Out)	FIFO
1	1	0		Reserved	
1	1	1	R	Digital Input Register	DIR
1	1	1	W	Configuration Control Register	CCR

In the following sections, the various registers are shown in their powerdown state. The "UC" notation stands for a value that is returned without change from the active mode. The notation " * " means that the value is reflecting the actual status of the 82077SL, but the value is determinable in the powerdown state. "N/A" reflects the values of the pins indicated. "X" indicates that the value is undefined.

2.1.1a STATUS REGISTER A (SRA, PS/2 MODE)

This register is read-only and monitors the state of the interrupt pin and several disk interface pins. This register is part of the register set, and is not accessible in PC-AT mode.

This register can be accessed during powerdown state without waking up the 82077SL from its powerdown state.

Bits	7	6°	5	4°	3	2°	1°C	0
Function	INT PENDING	$\overline{DRV2}$	STEP	$\overline{TRK0}$	HDSEL	$\overline{INDX}$	$\overline{WP}$	DIR
H/W Reset State	0	N/A	0	N/A	0	N/A	N/A	0
Auto PD State	0*	UC	0*	1	0*	1	1	0*

The INT PENDING bit is used by software to monitor the state of the 82077SL INTERRUPT pin. The bits marked with a " ° " reflect the state of drive signals on the cable and are independent of the state of the $\overline{INVERT}$ pin.

The INT PENDING bit is low by definition for 82077SL to be in powerdown. The bits reflecting the floppy disk drive input pins (TRK0, INDEX and WP) are forced to an inactive state. The floppy disk drive outputs (HDSEL, STEP, and DIR) also go to their inactive, default state.

As a read-only register, there is no default value associated with a reset other than some drive bits will change with a reset. The INT PENDING, STEP, HDSEL, and DIR bits will be low after reset.

2.1.1b STATUS REGISTER A (SRA, MODEL 30 MODE)

Bits	7	6	5	4	3	2	1	0
Function	INT PENDING	DRQ	STEP F/F	TRK0	$\overline{HDSEL}$	INDX	WP	$\overline{DIR}$
H/W Reset State	0	0	0	N/A	1	N/A	N/A	1
Auto PD State	0*	0*	0	0	1*	0	0	1*

This register has the following changes in PS/2 Model 30 Mode. Disk interface pins (Bits 0, 1, 2, 3, & 4) are inverted from PS/2 Mode. The DRQ bit monitors the status of the DMA Request pin. The STEP bit is latched with the Step output going active and is cleared with a read to the DIR register, Hardware or Software RESET.

The DRQ bit is low by definition for 82077SL to be in powerdown. The bits reflecting the floppy disk drive input pins (TRK0, INDEX and WP) are forced to reflect an inactive state. The floppy disk drive outputs (HDSEL, STEP, and DIR) also go to their inactive, default state.

2.1.2a STATUS REGISTER B (SRB, PS/2 MODE)

This register is read-only and monitors the state of several disk interface pins. This register is part of the PS/2 register set, and is not accessible in PC-AT mode.

Bits	7	6	5	4	3*	2	1	0
Function	1	1	DRIVE SEL 0	WRDATA TOGGLE	RDDATA TOGGLE	WE	MOT EN1	MOT EN0
H/W Reset State	1	1	0	0	0	0	0	0
Auto PD State	1	1	UC	0	0	0*	0	0

As the only drive input, RDDATA TOGGLE's activity is independent of the $\overline{INVERT}$ pin level and reflects the level as seen on the cable.

The two TOGGLE bits do not read back the state of their respective pins directly. Instead, the pins drive a Flip/Flop which produces a wider and more reliably read pulse. Bits 6 and 7 are undefined and always return a 1.

After any reset, the activity on the TOGGLE pins are cleared. Drive select and Motor bits cleared by the RESET pin and not software resets.

2.1.2b STATUS REGISTER B (SRB, MODEL 30 MODE)

Bits	7	6	5	4	3	2	1	0
Function	$\overline{DRV2}$	$\overline{DS1}$	$\overline{DS0}$	WRDATA F/F	RDDATA F/F	WE F/F	$\overline{DS3}$	$\overline{DS2}$
H/W Reset State	N/A	1	1	0	0	0	1	1
Auto PD State	UC	UC	UC	0	0	0	UC	UC

This register has the following changes in Model 30 Mode. Bits 0, 1, 5, and 6 return the decoded value of the Drive Select bits in the DOR register. Bits 2, 3, and 4 are set by their respective active going edges and are cleared by reading the DIR register. The WRDATA bit is triggered by raw WRDATA signals and is not gated by WE. Bits 2, 3, and 4 are cleared to a low level by either Hardware or Software RESET.

2.1.3 DIGITAL OUTPUT REGISTER (DOR)

The Digital Output Register contains the drive select and motor enable bits, a reset bit and a $\overline{DMA\ GATE}$ bit.

Bits	7	6	5	4	3	2	1	0
Function	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMA $\overline{GATE}$	$\overline{RESET}$	DRIVE SEL1	DRIVE SEL2
H/W Reset State	0	0	0	0	0	0	0	0
Auto PD State	0*	0*	0*	0*	UC	1*	UC	UC

The MOT ENx bits directly control their respective motor enable pins (ME0–3). A one means the pin is active, the $\overline{INVERT}$ pin determines the active level. The DRIVE SELx bits are decoded to provide four drive select lines and only one may be active at a time. A one is active and the $\overline{INVERT}$ pin determines the level on the cable. Standard programming practice is to set both MOT ENx and DRIVE SELx bits at the same time.

Table 2-1 lists a set of DOR values to activate the drive select and motor enable for each drive.

Table 2-1. Drive Activation Values

Drive	DOR Value
0	1CH
1	2DH
2	4EH
3	8FH

The $\overline{DMAGATE}$ bit is enabled only in PC-AT and Model 30 Modes. If $\overline{DMAGATE}$ is set low, the INT and DRQ outputs are tristated and the $\overline{DACK}$ and TC inputs are disabled. $\overline{DMAGATE}$ set high will enable INT, DRQ, TC, and $\overline{DACK}$ to the system. In PS/2 Mode $\overline{DMAGATE}$ has no effect upon INT, DRQ, TC or $\overline{DACK}$ pins and they are always active.

The DOR reset bit and the Motor Enable bits have to be inactive when the 82077SL is in powerdown. The $\overline{DMAGATE}$ and DRIVE SEL bits are unchanged. During powerdown, writing to the DOR does not awaken the 82077SL with the exception of activating any of the motor enable bits. Setting the motor enable bits active (high) will wake up the part.

This $\overline{RESET}$ bit clears the basic core of the 82077SL and the FIFO circuits when the LOCK bit is set to "0" (see Section 5.3.2 for LOCK bit definition). Once set, it remains set until the user clears this bit. This bit is set by a chip reset and the 82077SL is held in a reset state until the user clears this bit. The $\overline{RESET}$ bit has no effect upon this register.

2.1.4 DATARATE SELECT REGISTER (DSR)

Bits	7	6	5	4	3	2	1	0
Function	S/W RESET	POWER DOWN	PDOSC	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
H/W Reset State	0	0	0	0	0	0	1	0
Auto PD State	0	0	UC	UC	UC	UC	UC	UC

This register ensures backward compatibility with the 82072 floppy controller and is write-only. Changing the data rate changes the timings of the drive control signals. To ensure that drive timings are not violated when changing data rates, choose a drive timing such that the fastest data rate will not violate the timing.

This register is identical to the one used in 82077AA with the exception of bit 5. This bit in the 82077SL denoted by PDOSC is used to implement crystal oscillator power management. The internal oscillator in the 82077SL can be programmed to be either powered on or off via the PDOSC bit. This capability is independent of the chip's powerdown state. In other words, auto powerdown mode and powerdown via activating POWERDOWN bit has no effect over the power state of the oscillator.

In the default state the PDOSC bit is low and the oscillator is powered up. When this bit is programmed to a one, the oscillator is shut off. Hardware reset clears this bit to a zero. Neither of the software resets (via DOR or DSR) have any effect on this bit. When an external oscillator is used, this bit can be set to reduce power consumption. When an internal oscillator is used, this bit can be set to turn off the oscillator to conserve power. However, PDOSC must go high only when the part is in the powerdown state, otherwise the part will not function correctly and must be hardware reset once the oscillator has turned back on and stabilized. Setting the PDOSC bit has no effect on the clock input to the 82077SL (the X1 pin). The clock input is separately disabled when the part is powered down.

S/W RESET behaves the same as DOR RESET except that this reset is self clearing.

POWERDOWN bit implements direct powerdown. Setting this bit high will put the 82077SL into the powerdown state regardless of the state of the part. The part is internally reset and then put into powerdown. No status is saved and any operation in progress is aborted. Unlike the 82077AA this mode of powerdown does not turn off the internal oscillator. Any hardware or software reset will exit the 82077SL from this powerdown state.

PRECOMP 0–2 adjusts the WRDATA output to the disk to compensate for magnetic media phenomena known as bit shifting. The data patterns that are susceptible to bit shifting are well understood and the 82077SL compensates the data pattern as it is written to the disk. The amount of precompensation is dependent upon the drive and media but in most cases the default value is acceptable.

The 82077SL starts precompensating the data pattern starting on Track 0. The CONFIGURE command can change the track that precompensating starts on. Table 2-2 lists the precompensation values that can be selected and Table 2-3 lists the default precompensation values. The default value is selected if the three bits are zeros.

DRATE 0–1 select one of the four data rates as listed in Table 2-4. The default value is 250 Kbps upon a chip ("Hardware") reset. Other ("Software") Resets do not affect the DRATE or PRECOMP bits.

Table 2-2. Precompensation Delays

PRECOMP 432	Precompensation Delay
111	0.00 ns—DISABLED
001	41.67 ns
010	83.34 ns
011	125.00 ns
100	166.67 ns
101	208.33 ns
110	250.00 ns
000	DEFAULT

Table 2-3. Default Precompensation Delays

Data Rate	Precompensation Delays
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

Table 2-4. Data Rates

DRATESEL		DATA RATE	
1	0	MFM	FM
1	1	1 Mbps	Illegal
0	0	500 Kbps	250 Kbps
0	1	300 Kbps	150 Kbps
1	0	250 Kbps	125 Kbps

2.1.5 MAIN STATUS REGISTER (MSR)

Bits	7	6	5	4	3*	2	1	0
Function	RQM	DIO	NON DMA	CMD BSY	DRV3 BUSY	DRV2 BUSY	DRV1 BUSY	DRV0 BUSY
H/W Reset State	0	X	X	X	X	X	X	X
Auto PD State	1	0	0	0	0	0	0	0

The Main Status Register is a read-only register and is used for controlling command input and result output for all commands.

RQM—Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

DIO—Indicates the direction of a data transfer once RQM is set. A 1 indicates a read and a 0 indicates a write is required.

NON-DMA—This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

COMMAND BUSY—This bit is set to a one when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (SEEK, RECALIBRATE commands), this bit is returned to a 0 after the last command byte.

DRV x BUSY—These bits are set to ones when a drive is in the seek portion of a command, including seeks, and recalibrates.

2.1.6 FIFO (DATA)

All command parameter information and disk data transfers go through the FIFO. The FIFO is 16 bytes in size and has programmable threshold values. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to an 8272A compatible mode after a "Hardware" reset (Reset via pin 32). "Software" Resets (Reset via DOR or DSR register) can also place the 82077SL into 8272A compatible mode if the LOCK bit is set to "0" (See section 5.3.2 for the definition of the LOCK bit). This maintains PC-AT hardware compatibility. The default values can be changed through the CONFIGURE command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 2.5 gives several examples of the delays with a FIFO. The data is based upon the following formula:

$$\text{Threshold\#} \times \left| \frac{1}{\text{DATA RATE}} \times 8 \right| - 1.5\ \mu s = \text{DELAY}$$

Table 2-5. FIFO Service Delay

FIFO Threshold Examples	Maximum Delay to Servicing at 1 Mbps Data Rate
1 byte	$1 \times 8\ \mu s - 1.5\ \mu s = 6.5\ \mu s$
2 bytes	$2 \times 8\ \mu s - 1.5\ \mu s = 14.5\ \mu s$
8 bytes	$8 \times 8\ \mu s - 1.5\ \mu s = 62.5\ \mu s$
15 bytes	$15 \times 8\ \mu s - 1.5\ \mu s = 118.5\ \mu s$

FIFO Threshold Examples	Maximum Delay to Servicing at 500 Kbps Data Rate
1 byte	$1 \times 16\ \mu s - 1.5\ \mu s = 14.5\ \mu s$
2 bytes	$2 \times 16\ \mu s - 1.5\ \mu s = 30.5\ \mu s$
8 bytes	$8 \times 16\ \mu s - 1.5\ \mu s = 126.5\ \mu s$
15 bytes	$15 \times 16\ \mu s - 1.5\ \mu s = 238.5\ \mu s$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the 82077SL enters the command execution phase, it clears the FIFO of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC.

2.1.7a DIGITAL INPUT REGISTER (DIR, PC-AT MODE)

This register is read only in all modes. In PC-AT mode only bit 7 is driven, all other bits remain tristated.

Bits	7	6	5	4	3*	2	1	0
Function	DSK	—	—	—	—	—	—	—
H/W Reset State	N/A	—	—	—	—	—	—	—
Auto PD State	0	—	—	—	—	—	—	—

DSKCHG monitors the pin of the same name and reflects the opposite value seen on the disk cable, regardless of the value of INVERT. The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits remain tristated.

2.1.7b DIGITAL INPUT REGISTER (DIR, PS/2 MODE)

Bits	7	6	5	4	3	2	1	0
Function	DSK CHG	1	1	1	1	DRATE SEL1	DRATE SEL0	HIGH DENS
H/W Reset State	N/A	1	1	1	1	1	0	1
Auto PD State	0	1	1	1	1	UC	UC	UC

The following is changed in PS/2 Mode: Bits 6, 5, 4, and 3 return a value of "1", and the DRATE SEL1-0 return the value of the current data rate selected (see Table 2-4 for values).

HIGH DENS is low whenever the 500 Kbps or 1 Mbps data rates are selected. This bit is independent of the effects of the IDENT and INVERT pins.

The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits (as applicable) remain unchanged.

Table 2-6 shows the state of the DENSEL pin when INVERT is low.

This pin is set high after a pin RESET and is unaffected by DOR and DSR resets.

Table 2-6. DENSEL Encoding

Data Rate	IDENT*	DENSEL
1 Mbps	0	0
	1	1
500 Kbps	0	0
	1	1
300 Kbps	0	1
	1	0
250 Kbps	0	1
	1	0

*After ("Hardware") Chip Reset

2.1.7c DIGITAL INPUT REGISTER (DIR, MODEL 30 MODE)

Bits	7	6	5	4	3	2	1	0
Function	$\overline{\text{DSK}}$ $\overline{\text{CHG}}$	0	0	0	$\overline{\text{DMA}}$ $\overline{\text{GATE}}$	NOPREC	DRATE SEL1	DRATE SEL0
H/W Reset State	N/A	0	0	0	0	0	1	0
Auto PD State	1	0	0	0	UC	UC	UC	UC

The following is changed in Model 30 Mode: Bits 6, 5, and 4 return a value of "0", and Bit 7 ($\overline{\text{DSKCHG}}$) is inverted in Model 30 Mode.

The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits (as applicable) remain unchanged.

Bit 3 reflects the value of $\overline{\text{DMAGATE}}$ bit set in the DOR register.

Bit 2 reflects the value of NOPREC bit set in the CCR register.

2.1.8a CONFIGURATION CONTROL REGISTER (CCR, PC AT and PS/2 MODES)

This register sets the datarate and is write only. In the PC-AT it is named the DSR.

Bits	7	6	5	4	3	2	1	0
Function	—	—	—	—	—	—	DRATE SEL1	DRATE SEL0
H/W Reset State	—	—	—	—	—	—	1	0
Auto PD State	—	—	—	—	—	—	UC	UC

Refer to the table in the Data Rate Select Register for values. Unused bits should be set to 0.

2.1.8b CONFIGURATION CONTROL REGISTER (CCR, MODEL 30 MODE)

Bits	7	6	5	4	3	2	1	0
Function	—	—	—	—	—	NOPREC	DRATE SEL1	DRATE SEL0
H/W Reset State	—	—	—	—	—	0	1	0
Auto PD State	—	—	—	—	—	UC	UC	UC

NOPREC has no function, and is reset to "0" with a Hardware RESET only.

2.2 RESET

There are three sources of reset on the 82077SL; the RESET pin, a reset generated via a bit in the DOR and a reset generated via a bit in the DSR. All resets take the 82077SL out of the power down state.

On entering the reset state, all operations are terminated and the 82077SL enters an idle state. Activating reset while a disk write activity is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, and the 82077SL waits for a new command. Drive polling will start unless disabled by a new CONFIGURE command.

2.2.1 RESET PIN ("HARDWARE") RESET

The RESET pin is a global reset and clears all registers except those programmed by the SPECIFY command. The DOR Reset bit is enabled and must be cleared by the host to exit the reset state.

2.2.2 DOR RESET vs DSR RESET ("SOFTWARE" RESET)

These two resets are functionally the same. The DSR Reset is included to maintain 82072 compatibility. Both will reset the 8272 core which affects drive status information. The FIFO circuits will also be reset if the LOCK bit is a "0" (See Section 5.3.2 for the definition of the LOCK bit). The DSR Reset clears itself automatically while the DOR Reset requires the host to manually clear it. DOR Reset has precedence over the DSR Reset. The DOR Reset is set automatically upon a pin RESET. The user must manually clear this reset bit in the DOR to exit the reset state.

The t30a specification in the A.C. Specifications gives the minimum amount of time that the DOR reset must be held active. This amount of time that the DOR reset must be held active is dependent upon the data rate. 82077SL requires that the DOR reset bit must be held active for at least 0.5 μs at 250 Kbps. This is less than a typical ISA I/O cycle time.

2.3 DMA Transfers

DMA transfers are enabled with the SPECIFY command and are initiated by the 82077SL by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting $\overline{\text{DACK}}$ and addresses need not be valid.

3.0 DRIVE INTERFACE

The 82077SL has integrated all of the logic needed to interface to a floppy disk which use floppy interface. All drive outputs have 40 mA drive capability and all inputs use a receive buffer with hysteresis. The internal analog data separator requires no external components, yet allows for an extremely wide capture range with high levels of read-data jitter, and ISV. The designer needs only to run the 82077SL disk drive signals to the disk or tape drive connector.

3.1 Cable Interface

The $\overline{\text{INVERT}}$ pin selects between using the internal buffers on the 82077SL or user supplied inverting buffers. $\overline{\text{INVERT}}$ pulled to V_{CC} disables the internal buffers; pulled to ground will enable them. There is no need to use external buffers with the 82077SL in typical PC applications.

The polarity of the DENSEL pin is controlled through the IDENT pin, after hardware reset. For 5.25" drives a high on DENSEL tells the drive that either the 500 Kbps or 1 Mbps data rate is selected. For some 3.5" drives the polarity of DENSEL changes to a low for high data rates. See **Table 2-6 DENSEL Encoding** for $\overline{\text{IDENT}}$ pin settings.

Additionally, the two types of drives have different electrical interfaces. Generally, the 5.25" drive uses open collector drivers and the 3.5" drives (as used on PS/2) use totem-pole drivers. The output buffers on the 82077SL do not change between open collector or totem-pole, they are always totem-pole. For design information on interfacing 5.25" and 3.5" drives to a single 82077SL, refer to Section 9.

3.2 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called Data Window, is used to internally sample the serial data. One state of Data Window is used to sample the data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

To support reliable disk reads the data separator must track fluctuations in the read data frequency. Frequency errors primarily arise from two sources: motor rotation speed variation and instantaneous speed variation (ISV). A second condition, and one that opposes the ability to track frequency shifts is the response to bit jitter.

The internal data separator consists of two analog phase lock loops (PLLs) as shown in Figure 3-1. The two PLLs are referred to as the reference PLL and the data PLL. The reference PLL (the master PLL) is used to bias the data PLL (the slave PLL). The reference PLL adjusts the data PLL's operating point as a function of process, junction temperature and supply voltage. Using this architecture it was possible to eliminate the need for external trim components.

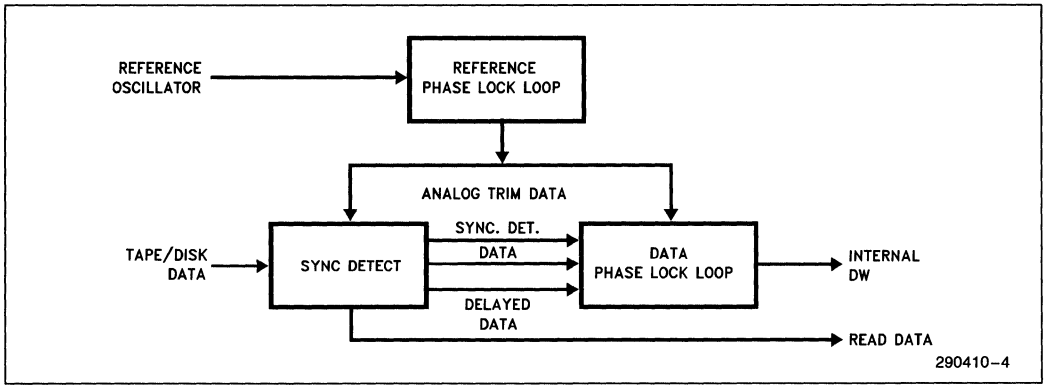


Figure 3-1. Data Separator Block Diagram

PHASE LOCK LOOP OVERVIEW

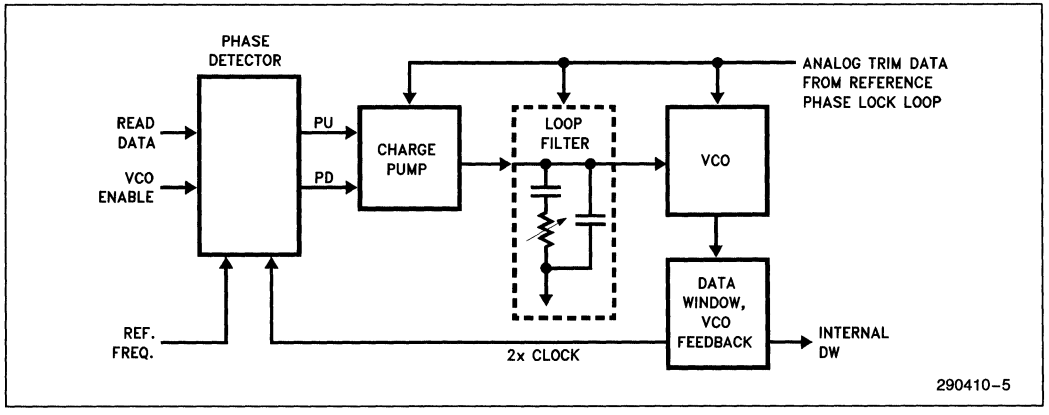


Figure 3-2. Data PLL

Figure 3-2 shows the data PLL. The reference PLL has control over the loop gain by its influence on the charge pump and the VCO. In addition the reference PLL controls the loop filter time constant. As a result the closed loop transfer function of the data PLL is controlled, and immune to the first order, to environmental factors and process variation.

Systems with analog PLLs are often very sensitive to noise. In the design of this data separator many steps were taken to avoid noise sensitivity problems. The analog section of the chip has a separate VSS pin (AVSS) which should be connected externally to a noise free ground. This provides a clean basis for VSS referenced signals. In addition many analog circuit features were employed to make the overall system as insensitive to noise as possible.

3.2.1 JITTER TOLERANCE

The jitter immunity of the system is dominated by the data PLL's response to phase impulses. This is measured as a percentage of the theoretical data window by dividing the maximum readable bit shift by a 1/4 bitcell distance. For instance, if the maximum allowable bit shift is 300 ns for a 500 Kbps data stream, the jitter tolerance is 60%. The graph in Figures 13-1 thru 13-4 of the Data Separator Characteristics sections illustrate the jitter tolerance of the 82077SL across each frequency range.

3.2.2 LOCKTIME (tLOCK)

The lock, or settling time of the data PLL is designed to be 64 bit times. This corresponds to 4 sync bytes in the FM mode and 8 sync bytes in the MFM mode. This value assumes that the sync field jitter is 5% the bit cell or less. This level of jitter should be easily achieved for a constant bit pattern, since intersymbol interference should be equal, thus nearly eliminating random bit shifting.

3.2.3 CAPTURE RANGE

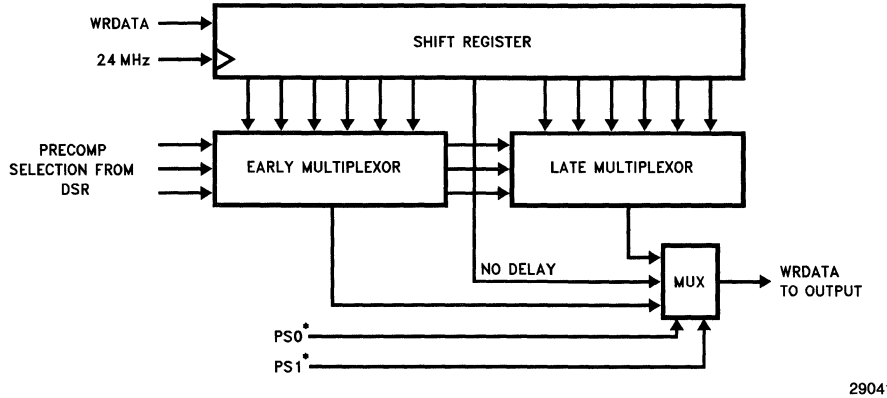
Capture Range is the maximum frequency range over which the data separator will acquire phase lock with the incoming RDDATA signal. In a floppy disk environment, this frequency variation is composed of two components: drive motor speed error and ISV. Frequency is a factor which may determine the maximum level of the ISV (Instantaneous Speed Variation) component. In general, as frequency increases the allowed magnitude of the ISV component will decrease. When determining the capture range requirements, the designer should take the maximum amount of frequency error for the disk drive and double it to account for media switching between drives.

3.3 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. The shifting of bits is a known phenomena of magnetic media and is dependent upon the disk media AND the floppy drive.

The 82077SL monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late (or not at all) relative to the surrounding bits. Figure 3-3 is a block diagram of the internal circuit.

The top block is a 13-bit shift register with the no delay tap being in the center. This allows 6 levels of early and late shifting with respect to nominal. The shift register is clocked at the main clock rate (24 MHz). The output is fed into 2 multiplexors—one for early and one for late. A final stage of multiplexors combines the early, late and normal data stream back into one which is the WRDATA output.



NOTE:
PS0,1 are 8272A control signals but are not available as outputs on the 82077SL.

Figure 3-3. Precompensation Block Diagram

4.0 POWER MANAGEMENT FEATURES

The 82077SL contains power management features that makes it ideal for design of portable personal computers. These features can be classified into power management of the part and that of the internal oscillator. The powerdown of the part is done independently of the internal oscillator in the 82077SL.

4.1 Oscillator Power Management

The 82077SL supports a built-in crystal oscillator that can be programmed to be either powered down or active, independent of the power state of the chip. This capability is implemented by the PDOSC bit in the DSR. When PDOSC is set low, the internal oscillator is on and when it is set high the internal oscillator is off. DSR powerdown does not turn off the oscillator.

When the external oscillator is used, power can be saved by turning off the internal oscillator. If the internal oscillator is used, the oscillator may be powered up (even when the rest of the chip is powered off) allowing the chip to wake up quickly and in a stable state. It is recommended to keep the internal oscillator on even when in the powerdown state. The main reason for this is that the recovery time of the oscillator during wake up may take tens of milliseconds under the worst case, which may create problems with any sensitive application software. In a typical application the internal oscillator should be on unless the system goes into a power saving or standby mode (such a mode request would be made by a system time out or by a user). In this case, the system software would take over and must turn on the oscillator sufficiently ahead of awakening the part.

In the case of the external oscillators, the power up characteristics are similar. If the external source remains active during the time the 82077SL is powered down, then the recovery time effect is minimized. The PD pin can be used to turn off the external source. While the PD pin is active 82077SL does not require a clock source. However, when the PD pin is inactive, the clocking source, once it starts oscillating, must be completely stable to ensure that the 82077SL operates properly.

4.2 Part Power Management

This section deals with the power management of the rest of the chip excluding the oscillator. This shows how powerdown modes and wake up modes are activated.

4.2.1 POWERDOWN MODES

The rest of the chip is powered down in two ways—direct powerdown and automatic powerdown. Direct powerdown results in immediate powerdown of the part without regard to the current state of the part. Automatic powerdown results when certain conditions become true within the part.

4.2.1.a Direct Powerdown

Direct powerdown is conducted via the POWERDOWN bit in the DSR register (bit 6). This mode is compatible to the 82077AA. Programming this bit high will powerdown 82077SL after the part is internally reset. All current status is lost if this type of powerdown mode is used. The part can exit powerdown from this mode via any hardware or software reset. This type of powerdown will override the automatic powerdown. If the part is in automatic powerdown when the DSR powerdown is issued then all the previous status of the part will be lost and the 82077SL will be reset to its default values.

4.2.1.b Auto Powerdown

Automatic powerdown is conducted via a "Set Powerdown Mode" command. There are four conditions required before the part will enter powerdown. All these conditions must be true for the part to initiate the powerdown sequence. These conditions are listed as follows:

1. The motor enable pins ME[0:3] must be inactive,
2. The part must be idle; this is indicated by MSR = 80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupt),
3. The head unload timer (HUT—explained in Section 6.2.6) must have expired, and
4. The auto powerdown timer must have timed out.

The command can be used to enable powerdown by setting the AUTO PD bit in the command to high. The command also provides a capability of programming a minimum power up time via the MIN DLY bit in the command. The minimum power up time refers to a minimum amount of time the part will remain powered up after being awakened or reset. An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down provided all the remaining conditions are met. Any software reset will reinitialize the timer. Changing of data rate extends the auto powerdown timer by up to 10 ms, but only if the data rate is changed during the countdown.

Disabling the auto powerdown mode cancels the timers and holds the 82077SL out of auto powerdown.

4.2.2 WAKE UP MODES

This section describes the conditions for awakening the part from both direct and automatic powerdown. Power conservation or extension of battery life is the main reason power management is required. This means that the 82077SL must be kept in powerdown state as long as possible and should be powered up as late as possible without compromising software transparency.

To keep the part in powerdown mode as late as possible implies that the part should wake up as fast as possible. However, some amount of time is required for the part to exit powerdown state and prepare the internal microcontroller to accept commands. Application software is very sensitive to such a delay and in order to maintain software transparency, the recovery time of the wake up process must be carefully controlled by the system software.

4.2.2.a Wake Up from DSR Powerdown

If the 82077SL enters the powerdown through the DSR powerdown bit, it must be reset to exit. Any form of software or hardware reset will serve, although DSR is recommended. No other register access will awaken the part, including writing to the DOR's motor enable (ME[0:3]) bits.

If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened by a software reset, the auto powerdown command (including the minimum delay timer) will once again become effective as previously programmed. If the part is awakened via a hardware reset, the auto powerdown is disabled.

After reset, the part will go through a normal sequence. The drive status will be initialized. The FIFO mode will be set to default mode on a hardware reset or on a software reset if the LOCK command has not blocked it. Finally, after a delay, the polling interrupt will be issued.

4.2.2.b Wake Up from Auto Powerdown

If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used then the part will go through the normal reset sequence. If the access is through the selected registers, then the 82077SL resumes operation as though it was never in powerdown. Besides activating the RESET pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake up the part:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not awaken the part)
2. A read from the MSR register
3. A read or write to the FIFO register

Any of these actions will wake up the part. Once awake, 82077SL will reinitiate the auto powerdown timer for 10 ms or 0.5 sec. (depending on the MIN DLY bit the auto powerdown command). The part will powerdown again when all the powerdown conditions stated in Section 4.2.1b are satisfied.

4.3 Register Behavior

The register descriptions and their values in the powerdown state were given in Section 2.1. Table 4.1 reiterates the AT and PS/2™ (including model 30) configuration registers available. It also shows the type of access permitted. In order to maintain software transparency, access to all the registers must be maintained. As Table 4.1 shows, two sets of registers are distinguished based on whether their access results in the part remaining in powerdown state or exiting it.

Access to all other registers is possible without awakening the part. These registers can be accessed during powerdown without changing the status of the part. A read from these registers will reflect the true status as shown in the register description in Section 2.1. A write to the part will result in the part retaining the data and subsequently reflecting it when the part awakens. Accessing the part during powerdown may cause an increase in the power consumption by the part. The part will revert back to its low power mode when the access has been completed.

4.4 Pin Behavior

The 82077SL is specifically designed for the portable PC systems in which the power conservation is a primary concern. This makes the behavior of the pins during powerdown very important.

The pins of 82077SL can be divided into two major categories—system interface and floppy disk drive interface. The floppy disk drive pins are disabled such that no power will be drawn through the 82077SL as a result of any voltage applied to the pin within the 82077SL's power supply range. Most of the system interface pins are left active to monitor system accesses that may wake up the part.

4.4.1 SYSTEM INTERFACE PINS

Table 4.2 gives the state of the system interface pins in the powerdown state. Pins unaffected by powerdown are labeled "UC". Input pins are "DISABLED" to prevent them from causing currents internal to the 82077SL when they have indeterminate input values.

Table 4-1. 82077SL Register Behavior

Address	Available Registers		Access Permitted
	PC-AT™	PS/2™ (Model 30)	
Access to these registers DOES NOT wake up the part			
000	—	SRA	R
001	—	SRB	R
010	DOR*	DOR*	R/W
011	—	—	—
100	DSR*	DSR*	W
110	—	—	—
111	DIR	DIR	R
111	CCR	CCR	W
Access to these registers wakes up the part			
100	MSR	MSR	R
101	FIFO	FIFO	R/W

NOTE:
*Writing to the DOR or DSR does not wake up the part, however, writing any of the motor enable bits or doing a software reset (either via DOR or DSR reset bits) will wake up the part.

Table 4-2. 82077SL System Interface Pins

System Pins	State in Power Down	System Pins	State in Power Down
Input Pins		**Output Pins**	
$\overline{CS}$	UC	DRQ	UC (Low)
$\overline{RD}$	UC	INT	UC (Low)
$\overline{WR}$	UC	PD	HIGH
A[0:2]	UC	IDLE	High (Auto PD) Low (DSR PD)
DB[0:7]	UC	DB[0:7]	UC
RESET	UC		
IDENT	UC		
$\overline{DACK}$	Disabled		
TC	Disabled		
X[1:2]	Programmable		

Two pins which can be used to indicate the status of the part are IDLE and PD. These pins have replaced the HIFIL and LOFIL pins in the 82077AA. The capacitor required on the 82077AA has been integrated on the chip. Table 4-3 shows how these pins reflect the 82077SL status.

Table 4-3. 82077SL Status Pins

PD	IDLE	MSR	Part Status
1	1	80H	Auto Powerdown
1	0	RQM = 1; MSR[6:0] = X	DSR Powerdown
0	1	80H	Idle
0	0	—	Busy

The IDLE pin indicates when the part is idle state and can be powered down. It is a combination of MSR equalling 80H, the head being unloaded and the INT pin being low. As shown in the table the IDLE pin will be low when the part is in DSR powerdown state. The PD pin is active whenever the part is in the powerdown state. It is active for either mode of powerdown. The PD pin can be used to turn off an external oscillator of other floppy disk drive interface hardware.

4.4.2 FDD INTERFACE PINS

All pins in the FDD interface which can be connected directly to the floppy disk drive itself are either DISABLED or TRISTATED. Pins used for local logic control or part programming are unaffected. Table 4-4 depicts the state of the floppy disk drive interface pins in the powerdown state.

Table 4-4. 82077SL FDD Interface Pins

FDD Pins	State in Powerdown	System Pins	State in Powerdown
Input Pins		**Output Pins**	
RDDATA	Disabled	ME[0:3]	Tristated
WP	Disabled	DS[0:3]	Tristated
TRK0	Disabled	DIR	Tristated
INDX	Disabled	STEP	Tristated
DRV2	Disabled	WRDATA	Tristated
DSKCHG	Disabled	WE	Tristated
$\overline{INVERT}$	UC	HDSEL	Tristated
		DENSEL	Tristated
		DRATE[0:1]	Tristated
		MFM	UC

5.0 CONTROLLER PHASES

For simplicity, command handling in the 82077SL can be divided into three phases: Command, Execution and Result. Each phase is described in the following secions.

When there is no command in progress, the 82077SL can be in idle, drive polling or powerdown state.

5.1 Command Phase

After a reset, the 82077SL enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the 82077SL before the command phase is complete (Please refer to Section 6.0 for the command descriptions). These bytes of data must be transferred in the order prescribed.

Before writing to the 82077SL, the host must examine the RQM and DIO bits of the Main Status Register. RQM, DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the 82077SL after each write cycle until the received byte is processed. The 82077SL asserts RQM again to request each parameter byte of the command, unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0", and the 82077SL automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to retain compatibility with the 8272A, and to provide for the proper handling of the "Invalid Command" condition.

5.2 Execution Phase

All data transfers to or from the 82077SL occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the SPECIFY command.

Each data byte is transferred by an INT or DRQ depending on the DMA mode. The CONFIGURE command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the 82077SL when service is requested from the host, and ranges from 1 to 16. The parameter FIFOTHR which the user programs is one less, and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request, for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

5.2.1 NON-DMA MODE, TRANSFERS FROM THE FIFO TO THE HOST

The INT pin and RQM bits in the Main Status Register are activated when the FIFO contains (16–<threshold>) bytes, or the last bytes of a full sector transfer have been placed in the FIFO. The INT pin can be used for interrupt driven systems and RQM can be used for polled sytems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The 82077SL will deactivate the INT pin and RQM bit when the FIFO becomes empty.

5.2.2 NON-DMA MODE, TRANSFERS FROM THE HOST TO THE FIFO

The INT pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The INT pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The INT pin will also be deactivated if TC and DACK# both go inactive. The 82077SL enters the result phase after the last byte is taken by the 82077SL from the FIFO (i.e. FIFO empty condition).

5.2.3 DMA MODE, TRANSFERS FROM THE FIFO TO THE HOST

The 82077SL activates the DRQ pin when the FIFO contains (16–<threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The 82077SL will deactivate the DRQ pin when the FIFO becomes empty. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of RD#, on the last byte, if no edge is present on DACK#). A data underrun may occur if DRQ is not removed in time to prevent an unwanted cycle.

5.2.4 DMA MODE, TRANSFERS FROM THE HOST TO THE FIFO

The 82077SL activates the DRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the DACK# and WR# pins and placing data in the FIFO. DRQ remains active until the FIFO becomes full. DRQ is again set true when the FIFO has <threshold> bytes remaining in the FIFO. The 82077SL will also deactivate the DRQ pin when TC becomes true (qualified by DACK#), indicating that no more data is required. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of WR# of the last byte, if no edge is present on DACK#). A data overrun may occur if DRQ is not removed in time to prevent an unwanted cycle.

5.2.5 DATA TRANSFER TERMINATION

The 82077SL supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer. If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the 82077SL will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the 82077SL, the internal sector count will be complete when 82077SL reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the 82077SL to read the last 16 bytes from the FIFO. The host must tolerate this delay.

5.3 Result Phase

The generation of INT determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the 82077SL before the result phase is complete. (Refer to Section 6.0 on command descriptions.) These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read from the FIFO. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared. This indicates that the 82077SL is ready to accept the next command.

6.0 COMMAND SET/DESCRIPTIONS

Commands can be written whenever the 82077SL is in the command phase. Each command has a unique set of needed parameters and status results. The 82077SL checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it was invalid, the next time the RQM bit in the MSR register is a "1" the DIO and CB bits will also be "1", indicating the FIFO must be read. A result byte of 80H will be read out of the FIFO, indicating an invalid command was issued. After reading the result byte from the FIFO the 82077SL will return to the command phase. Table 6-1 is a summary of the Command set.

Table 6-1. 82077SL Command Set

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
READ DATA										
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and system
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				
READ DELETED DATA										
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and system
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				
WRITE DATA										
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the system and FDD
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				

Table 6-1. 82077SL Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
WRITE DELETED DATA										
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior
	W					H				to Command execution
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and system
Result	R					ST 0				Status information after
	R					ST 1				Command execution
	R					ST 2				
	R					C				
	R					H				Sector ID information after
	R					R				Command execution
	R					N				
READ TRACK										
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior
	W					H				to Command execution
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and system. FDC reads all of cylinders contents from index hole to EOT
Result	R					ST 0				Status information after
	R					ST 1				Command execution
	R					ST 2				
	R					C				
	R					H				Sector ID information after
	R					R				Command execution
	R					N				
VERIFY										
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior
	W					H				to Command execution
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL/SC				
Execution										No data transfer takes place
Result	R					ST 0				Status information after
	R					ST 1				Command execution
	R					ST 2				
	R					C				
	R					H				Sector ID information after
	R					R				Command execution
	R					N				
VERSION										
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

Table 6-1. 82077SL Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
FORMAT TRACK										
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				N					Bytes/Sector
	W				SC					Sectors/Cylinder
	W				GPL					Gap 3
	W				D					Filler Byte
Execution For Each Sector Repeat:	W				C					Input Sector Parameters
	W				H					
	W				R					
	W				N					
										82077SL formats an entire cylinder
Result	R				ST 0					Status information after Command execution
	R				ST 1					
	R				ST 2					
	R				Undefined					
	R				Undefined					
	R				Undefined					
	R				Undefined					
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R				ST 0					Status information at the end of each seek operation
	R				PCN					
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT					HUT			
	W	HLT							ND	
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R				ST 3					Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				NCN					
Execution										Head is positioned over proper Cylinder on Diskette
CONFIGURE										
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL		FIFOTHR			
	W	PRETRK								
RELATIVE SEEK										
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	RCN								

Table 6-1. 82077SL Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
DUMPREG										
Command	W	0	0	0	0	1	1	1	0	*Note
Execution										Registers placed in FIFO
Result	R				PCN-Drive 0					
	R				PCN-Drive 1					
	R				PCN-Drive 2					
	R				PCN-Drive 3					
	R		SRT				HUT			
	R				HLT				ND	
	R				SC/EOT					
	R	LOCK	0	D_3	D_2	D_1	D_0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL			FIFOTHR		
	R				PRETRK					
READ ID										
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R				ST 0					Status information after Command execution
	R				ST 1					
	R				ST 2					
	R				C					
	R				H					Disk status after the Command has completed.
	R				R					
	R				N					
PERPENDICULAR MODE										
Command	W	0	0	0	1	0	0	1	0	Command Codes
	W	OW	0	D_3	D_2	D_1	D0	GAP	WGATE	
LOCK										
Command	W	LOCK	0	0	1	0	1	0	0	Command Code
Result	R	0	0	0	LOCK	0	0	0	0	
POWERDOWN MODE										
Command	W	0	0	0	1	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	MIN DLY	AUTO PD	
Result	R	0	0	0	0	0	0	MIN DLY	AUTO PD	
INVALID										
Command	W				Invalid Codes					Invalid Command Codes (NoOp — 82077SL goes into Standby State)
Result	R				ST 0					ST 0 = 80H

SC is returned if the last command that was issued was the FORMAT command. EOT is returned if the last command was a READ or WRITE.

NOTE:
These bits are used internally only. They are not reflected in the Drive Select pins. It is the users responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

PARAMETER ABBREVIATIONS

Symbol	Description
AUTO PD	Auto powerdown control. If this bit is 0, then the automatic powerdown is disabled. If it is set to 1, then the automatic powerdown is enabled.
C	Cylinder address. The currently selected cylinder address, 0 to 255.
D_0, D_1 D_2, D_3	Drive Select 0-3. Designates which drives are Perpendicular drives, a "1" indicating Perpendicular drive.
D	Data pattern. The pattern to be written in each sector data field during formatting.
DIR	Direction control. If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.
DS0, DS1	Disk Drive Select.

DS1	DS0	
0	0	drive 0
0	1	drive 1
1	0	drive 2
1	1	drive 3

DTL	Special sector size. By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.
EC	Enable Count. When this bit is "1" the "DTL" parameter of the Verify Command becomes SC (Number of sectors per track).
EFIFO	Enable FIFO. When this bit is 0, the FIFO is enabled. A "1" puts the 82077SL in the 8272A compatible mode where the FIFO is disabled.
EIS	Enable implied seek. When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.
EOT	End of track. The final sector number of the current track.
GAP	Alters Gap 2 length when using Perpendicular Mode.
GPL	Gap length. The gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	Head address. Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head load time. The time interval that 82077SL waits after loading the head and before initiating a read or write operation. Refer to the SPECIFY command for actual delays.
HUT	Head unload time. The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the SPECIFY command for actual delays.
Lock	Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be reset to their default values by a "Software Reset" (Reset made by setting the proper bit in the DSR or DOR registers).
MFM	MFM/FM mode selector. A one selects the double density (MFM) mode. A zero selects single density (FM) mode.
MIN DLY	Minimum power up time control. This bit is active only if AUTO PD bit is enabled. Setting this bit to a 0, assigns a 10 ms minimum power up time and setting this bit to a 1, assigns a 0.5 sec. minimum power up time.
MT	Multi-track selector. When set, this flag selects the multi-track operating mode. In this mode, the 82077SL treats a complete cylinder, under head 0 and 1, as a single track. The 82077SL operates as if this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the 82077SL finishes operating on the last sector under head 0.

Symbol	Description
N	Sector size code. This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the users responsibility to not select combinations that are not possible with the drive.

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

Symbol	Description
NCN	New cylinder number. The desired cylinder number.
ND	Non-DMA mode flag. When set to 1, indicates that the 82077SL is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the 82077SL operates in DMA mode, interfacing to a DMA controller by means of the DRQ and DACK# signals.
OW	The bits denoted D_0, D_1, D_2, and D_3 of the **PERPENDICULAR MODE** command can only be overwritten when the OW bit is set to "1".
PCN	Present cylinder number. The current position of the head at the completion of SENSE INTERRUPT STATUS command.
POLL	Polling disable. When set, the internal polling routine is disabled. When clear, polling is enabled.
PRETRK	Precompensation start track number. Programmable from track 00 to FFH.
R	Sector address. The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative cylinder number. Relative cylinder offset from present cylinder as used by the RELATIVE SEEK command.
SC	Number of sectors. The number of sectors to be initialized by the FORMAT command. The number of sectors to be verified during a Verify Command, when EC is set.

Symbol	Description
SK	Skip flag. When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of READ DATA. If READ DELETED is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step rate interval. The time interval between step pulses issued by the 82077SL. Programmable from 0.5 to 8 milliseconds, in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.
ST0 ST1 ST2 ST3	Status register 0–3. Registers within the 82077SL that store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write gate alters timing of WE, to allow for pre-erase loads in perpendicular drives.

6.1 Data Transfer Commands

All of the READ DATA, WRITE DATA and VERIFY type commands use the same parameter bytes and return the same results information. The only difference being the coding of bits 0–4 in the first byte.

An implied seek will be executed if the feature was enabled by the CONFIGURE command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it will be reflected in the results status normally returned for a READ/WRITE DATA command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

6.1.1 READ DATA

A set of nine (9) bytes is required to place the 82077SL into the Read Data Mode. After the READ DATA command has been issued, the 82077SL loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the SPECIFY command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the 82077SL reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one, and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the 82077SL stops sending data, but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector terminate the READ DATA Command.

N determines the number of bytes per sector (see Table 6-2 below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the 82077SL transfers the specified number of bytes to the host. For reads, it continues to read the entire 128 byte sector and checks for CRC errors. For writes it completes the 128 byte sector by filling in zeroes. If N is not set to 00 Hex, DTL should be set to FF Hex, and has no impact on the number of bytes transferred.

Table 6-2. Sector Sizes

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

The amount of data which can be handled with a single command to the 82077SL depends upon MT (multi-track) and N (Number of bytes/sector).

Table 6-3. Effects of MT and N Bits

MT	N	Max. Transfer Capacity	Final Sector Read from Disk
0	1	256 × 26 = 6,656	26 at side 0 or 1
1	1	256 × 52 = 13,312	26 at side 1
0	2	512 × 15 = 7,680	15 at side 0 or 1
1	2	512 × 30 = 15,360	15 at side 1
0	3	1024 × 8 = 8,192	8 at side 0 or 1
1	3	1024 × 16 = 16,384	16 at side 1

The Multi-Track function (MT) allows the 82077SL to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at the last sector of the same track at Side 1.

If the host terminates a read or write operation in the 82077SL, then the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 6-6. The termination must be normal.

At the completion of the READ DATA Command, the head is not unloaded until after the Head Unload Time Interval (specified in the SPECIFY command) has elapsed. If the host issues another command before the head unloads then the head settling time may be saved between subsequent reads.

If the 82077SL detects a pulse on the IDX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the 82077SL sets the IC code in Status Register 0 to "01" (Abnormal termination), and sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the READ DATA Command.

After reading the ID and Data Fields in each sector, the 82077SL checks the CRC bytes. If a CRC error occurs in the ID or data field, the 82077SL sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the READ DATA Command.

Table 6-4 below describes the affect of the SK bit on the READ DATA command execution and results.

Table 6-4. Skip Bit vs READ DATA Command

SK Bit Value	Data Address Mark Type Encountered	Results		
		Sector Read?	CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	No	Normal Termination.
0	Deleted Data	Yes	Yes	Address Not Incremented. Next Sector Not Searched For.
1	Normal Data	Yes	No	Normal Termination.
1	Deleted Data	No	Yes	Normal Termination Sector Not Read ("Skipped").

Except where noted in Table 6-4, the C or R value of the sector address is automatically incremented (see Table 6-6).

6.1.2 READ DELETED DATA

This command is the same as the READ DATA command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 6-5 describes the affect of the SK bit on the READ DELETED DATA command execution and results.

Table 6-5. Skip Bit vs READ DELETED DATA Command

SK Bit Value	Data Address Mark Type Encountered	Results		
		Sector Read?	CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	Yes	Address Not Incremented. Next Sector Not Searched For.
0	Deleted Data	Yes	No	Normal Termination.
1	Normal Data	No	Yes	Normal Termination Sector Not Read ("Skipped").
1	Deleted Data	Yes	No	Normal Termination.

Except where noted in Table 6-5 above, the C or R value of the sector address is automatically incremented (See Table 6-6).

6.1.3 READ TRACK

This command is similar to the READ DATA command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the IDX pin, the 82077SL starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the 82077SL finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The 82077SL compares the ID information read from each sector with the specified value in the command, and sets the ND flag of Status Register 1 to a "1" if there is no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (Bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors have been read. If the 82077SL does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the IDX pin, then it sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 6-6. Result Phase Table

MT	Head	Final Sector Transferred to Host	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
1	0	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	LSB	01	NC

NC: no change, the same value as the one at the beginning of command execution.
LSB: least significant bit, the LSB of H is complemented.

6.1.4 WRITE DATA

After the WRITE DATA command has been issued, the 82077SL loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the SPECIFY command), and begins reading ID Fields. When the sector address read from the diskette matches the sector address specified in the command, the 82077SL reads the data from the host via the FIFO, and writes it to the sector's data field.

After writing data into the current sector, the 82077SL computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the 82077SL continues writing to the next data field. The 82077SL continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros.

The 82077SL reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID Fields, it sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the WRITE DATA command.

The WRITE DATA command operates in much the same manner as the READ DATA command. The following items are the same. Please refer to the READ DATA Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command.
- Definition of DTL when N = 0 and when N does not = 0.

6.1.5 WRITE DELETED DATA

This command is almost the same as the WRITE DATA command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

6.1.6 VERIFY

The VERIFY command is used to verify the data stored on a disk. This command acts exactly like a READ DATA command except that no data is transferred to the host. Data is read from the disk, CRC computed and checked against the previously stored value.

Because no data is transferred to the host, TC (pin 25) cannot be used to terminate this command. By setting the EC bit to "1" an implicit TC will be issued to the 82077SL. This implicit TC will occur when the SC value has decrement to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0" DTL/SC should be programmed to 0FFH. Refer to Table 6-6 and Table 6-7 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 6-7. Verify Command Result Phase Table

MT	EC	SC/EOT Value	Termination Result
0	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

NOTE:
If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

6.1.7 FORMAT TRACK

The FORMAT command allows an entire track to be formatted. After a pulse from the IDX pin is detected, the 82077SL starts writing data on the disk including Gaps, Address Marks, ID Fields and Data Fields, per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID Field for each sector is supplied by the host; that is, four data bytes per sector are needed by the 82077SL for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the 82077SL for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the 82077SL encounters a pulse on the IDX pin again and it terminates the command.

Table 6-8 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

Table 6-8. Typical Values for Formatting

		Sector Size	N	SC	GPL1	GPL2
5.25″ Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
3.5″ Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
	MFM	256	1	0F	0E	36
		512**	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in read and write commands to avoid splice point between data field and ID field of contiguous sections.
GPL2 = suggested GPL value in FORMAT TRACK command.
*PC-AT values (typical)
**PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives.

NOTE:
All values except Sector Size are in Hex.

6.1.7.1 Format Fields

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		C	H	S	N	C	GAP 2	SYNC	DATA AM		DATA	C	GAP 3	GAP 4b
80x	12x	3x	FC	50x	12x	3x	FE	Y	D	E	O	R	22x	12x	3x	FB		R		
4E	00	C2		4E	00	A1		L		C		C	4E	00	A1	F8		C		

Figure 6-1. System 34 Format Double Density

GAP 4a	SYNC	IAM	GAP 1	SYNC	IDAM	C	H	S	N	C	GAP 2	SYNC	DATA AM	DATA	C	GAP 3	GAP 4b
40x	6x	FC	26x	6x	FE	Y	D	E	O	R	11x	6x	FB or F8		R		
FF	00		FF	00		L		C		C	FF	00			C		

Figure 6-2. System 3740 Format Single Density

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		C	H	S	N	C	GAP 2	SYNC	DATA AM		DATA	C	GAP 3	GAP 4b
80x	12x	3x	FC	50x	12x	3x	FE	Y	D	E	O	R	41x	12x	3x	FB		R		
4E	00	C2		4E	00	A1		L		C		C	4E	00	A1	F8		C		

Figure 6-3. Perpendicular Format

6.2 Control Commands

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete; READ ID, RECALIBRATE and SEEK. The other control commands do not generate an interrupt.

6.2.1 READ ID

The READ ID command is used to find the present position of the recording heads. The 82077SL stores the values from the first ID Field it is able to read into its registers. If the 82077SL does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the IDX pin, it then sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the SENSE INTERRUPT STATUS command. Otherwise, valuable interrupt status information will be lost.

6.2.2 RECALIBRATE

This command causes the read/write head within the 82077SL to retract to the track 0 position. The 82077SL clears the contents of the PCN counter, and checks the status of the TRK0 pin from the FDD. As long as the TRK0 pin is low, the DIR pin remains 0 and step pulses are issued. When the TRK0 pin goes high, the SE bit in Status Register 0 is set to "1", and the command is terminated. If the TRK0 pin is still low after 79 step pulses have been issued, the 82077SL sets the SE and the EC bits of Status Register 0 to "1", and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one RECALIBRATE command to return the head back to physical Track 0.

The RECALIBRATE command does not have a result phase. SENSE INTERRUPT STATUS command must be issued after the RECALIBRATE command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the 82077SL is in the BUSY state, but during the execution phase it is in a NON BUSY state. At this time another RECALIBRATE command may be issued, and in this manner, parallel RECALIBRATE operations may be done on up to 4 drives at once.

Upon power up, the software must issue a RECALIBRATE command to properly initialize all drives and the controller.

6.2.3 SEEK

The read/write head within the drive is moved from track to track under the control of the SEEK Command. The 82077SL compares the PCN which is the current head position with the NCN and performs the following operation if there is a difference:

—PCN < NCN: Direction signal to drive set to "1" (step in), and issues step pulses.

—PCN > NCN: Direction signal to drive set to "0" (step out), and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN, then the SE bit in Status Register 0 is set to "1", and the command is terminated.

During the command phase of the seek or recalibrate operation, the 82077SL is in the BUSY state, but during the execution phase it is in the NON BUSY state.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1)	SEEK command;	Step to the proper track
2)	SENSE INTERRUPT STATUS command;	Terminate the Seek command
3)	READ ID.	Verify head is on proper track
4)	Issue READ/WRITE command.	

The SEEK command does not have a result phase. Therefore, it is highly recommended that the SENSE INTERRUPT STATUS Command be issued after the SEEK command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return a "0". When exiting DSR POWERDOWN mode, the 82077SL clears the PCN value and the status information to zero. Prior to issuing the DSR POWERDOWN command, it is highly recommended that the user service all pending interrupts through the SENSE INTERRUPT STATUS command.

6.2.4 SENSE INTERRUPT STATUS

An interrupt signal on INT pin is generated by the 82077SL for one of the following reasons:

1. Upon entering the Result Phase of:
   a. READ DATA Command
   b. READ TRACK Command
   c. READ ID Command
   d. READ DELETED DATA Command
   e. WRITE DATA Command
   f. FORMAT TRACK Command
   g. WRITE DELETED DATA Command
   h. VERIFY Command
2. End of SEEK, RELATIVE SEEK or RECALIBRATE Command
3. 82077SL requires a data transfer during the execution phase in the non-DMA Mode

The SENSE INTERRUPT STATUS command resets the interrupt signal and via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt. If a SENSE INTERRUPT STATUS command is issued when no active interrupt condition is present, the status register ST0 will return a value of 80H (invalid command).

Table 6-9. Interrupt Identification

SE	IC	Interrupt Due To
0	11	Polling
1	00	Normal Termination of SEEK or RECALIBRATE command
1	01	Abnormal Termination of SEEK or RECALIBRATE command

The SEEK, RELATIVE SEEK and the RECALIBRATE commands have no result phase. SENSE INTERRUPT STATUS command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a SENSE INTERRUPT STATUS is not issued, the drive, will continue to be BUSY and may effect the operation of the next command.

6.2.5 SENSE DRIVE STATUS

SENSE DRIVE STATUS obtains drive status information. It has no execution phase and goes directly to the result phase from the command phase. STATUS REGISTER 3 contains the drive status information.

6.2.6 SPECIFY

The SPECIFY command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between the Head Load signal goes high and the read, write operation starts. The values change with the data rate speed selection and are documented in Table 6-10. The values are the same for MFM and FM.

Table 6-10. Drive Control Delays (ms)

	HUT				SRT			
	1M	500K	300K	250K	1M	500K	300K	250K
0	128	256	426	512	8.0	16	26.7	32
1	8	16	26.7	32	7.5	15	25	30
..	..	..	..	..	..	..	..	..
E	112	224	373	448	1.0	2	3.33	4
F	120	240	400	480	0.5	1	1.67	2

	HLT			
	1M	500K	300K	250K
00	128	256	426	512
01	1	2	3.3	4
02	2	4	6.7	8
..	..	..	..	.
7F	126	252	420	504
7F	127	254	423	508

The choice of DMA or NON-DMA operations is made by the ND bit. When this bit is "1", the NON-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signalled by the DRQ pin. Non-DMA mode uses the RQM bit and the INT pin to signal data transfers.

6.2.7 CONFIGURE

Issued to select the special features of the 82077SL. A CONFIGURE command need not be issued if the default values of the 82077SL meet the system requirements.

CONFIGURE DEFAULT VALUES:

EIS — No Implied Seeks
EFIFO — FIFO Disabled
POLL — Polling Enabled
FIFOTHR — FIFO Threshold Set to 1 Byte
PRETRK — Pre-Compensation Set to Track 0

EIS—Enable implied seek. When set to "1", the 82077SL will perform a SEEK operation before executing a read or write command. Defaults to no implied seek.

EFIFO—A "1" puts the FIFO into the 8272A compatible mode where the FIFO is disabled. This means data transfers are asked for on a byte by byte basis. Defaults to "1", FIFO disabled. The threshold defaults to one.

POLL—Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a RESET. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR—The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte "0F" selects 16 bytes.

PRETRK—Pre-compensation start track number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0, "FF" selects 255.

6.2.8 VERSION

The VERSION command checks to see if the controller is an enhanced type or the older type (8272A/765A). A value of 90 H is returned as the result byte, defining an enhanced FDD controller is in use. No interrupts are generated.

6.2.9 RELATIVE SEEK

The command is coded the same as for SEEK, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control.

DIR	Action
0	Step Head Out
1	Step Head In

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

The RELATIVE SEEK command differs from the SEEK command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The SEEK command is good for drives that support a maximum of 256 tracks. RELATIVE SEEKs cannot be overlapped with other RELATIVE SEEKs. Only one RELATIVE SEEK can be active at a time. Bit 4 of Status Register 0 (EC) will be set if RELATIVE SEEK attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks and that the host needs to read track 300 and the head is on any track (0–255). If a SEEK command was issued, the head would stop at track 255. If a RELATIVE SEEK command was issued, the 82077SL would move the head the specified number of tracks, regardless of the internal cylinder position register (but would increment the register). If the head had been on track 40 (D), the maximum track that the 82077SL could position the head on using RELATIVE SEEK, would be 296 (D), the initial track, +256 (D). The maximum count that the head can be moved with a single RELATIVE SEEK command is 256 (D).

The internal register, PCN, would overflow as the cylinder number crossed track 255 and would contain 40 (D). The resulting PCN value is thus (NCN + PCN) mod 256. Functionally, the 82077SL starts counting from 0 again as the track number goes above 255(D). It is the users responsibility to compensate 82077SL functions (precompensation track number) when accessing tracks greater than 255. The 82077SL does not keep track that it is working in an "extended track area" (greater than 255). Any command issued would use the current PCN value except for the RECALIBRATE command which only looks for the TRACK0 signal. RECALIBRATE would return an error if the head was farther than 79 due to its limitation of issuing a maximum 80 step pulses. The user simply needs to issue a second RECALIBRATE command. The SEEK command and implied seeks will function correctly within the 44 (D) track (299–255) area of the "extended track area". It is the users responsibility not to issue a new track position that would exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0–255) of tracks, a RELATIVE SEEK would be issued to cross the track 255 boundary.

A RELATIVE SEEK can be used instead of the normal SEEK but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a READ ID command to ensure that the head is physically on the track that software assumes it to be. Different 82077SL commands will return different cylinder results which may be difficult to keep track of with software without the READ ID command.

6.2.10 DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug.

6.2.11 PERPENDICULAR MODE COMMAND

The PERPENDICULAR MODE command should be issued prior to executing READ/WRITE/FORMAT commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 6-11 describes the effects of the WGATE and GAP bits for the PERPENDICULAR MODE command. Upon a reset, the 82077SL will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data rate Select Register. The user must ensure that the two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal the pre-erase head is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The format field shown in Figure 5-3 illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the 82077SL, the controller must begin synchronization at the beginning of the Sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, an approximate 2 byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the WRITE DATA case, the 82077SL activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC as shown in Figure 6-1. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP = 0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the PERPENDICULAR MODE command is invoked, 82077SL software behavior from the user standpoint is unchanged.

Table 6-11. Effects of WGATE and GAP Bits

GAP	WGATE	MODE	VCO Low Time after Index Pulse	Length of Gap2 Format Field	Portion of Gap2 Written by Write Data Operation	Gap2 VCO Low Time for Read Operations
0	0	Conventional Mode	33 Bytes	22 Bytes	0 Bytes	24 Bytes
0	1	Perpendicular Mode (500 Kbps Data Rate)	33 Bytes	22 Bytes	19 Bytes	24 Bytes
1	0	Reserved (Conventional)	33 Bytes	22 Bytes	0 Bytes	24 Bytes
1	1	Perpendicular Mode (1 Mbps Data Rate)	18 Bytes	41 Bytes	38 Bytes	43 Bytes

NOTE:
When either GAP or WGATE bit is set, the current value of precompensation in the DSR is used.

6.2.12 POWERDOWN MODE COMMAND

The POWERDOWN MODE command allows the automatic power management of the 82077SL. This especially allows the extension of battery life in portable PC systems. This command should be issued during the BIOS power on self test (POST) to enable auto powerdown.

As soon as the command is enabled, a 10 ms or a 0.5 sec minimum power up timer is initiated depending on whether the MIN DLY bit is set to 0 or 1. This timer is one of the required conditions that has to be satisfied before the part will enter auto powerdown. Any software reset will reinitialize the timer. The timer countdown is also extended by up to 10 ms if the data rate is changed during the timer's countdown. Without this timer 82077SL would have been put to sleep immediately after 82077SL is idle. The minimum delay gives software a chance to interact with 82077SL without incurring an additional overhead due to recovery time.

The results phase returns the values programmed for MIN DLY and AUTO PD. The results phase of the auto powerdown mode command has its two most significant bits set to zero to distinguish it from the 82077AA's command of the same value which returns an "Illegal Command" status of 80H. The auto powerdown mode is disabled by a hardware reset. Software results have no effect on the POWERDOWN MODE command parameters.

6.3 Command Set Enhancements

The PERPENDICULAR MODE and DUMPREG commands were enhanced along with the addition of a new LOCK command in the 82077AA. These enhancements also hold for the 82077SL and are explained in this section of the data sheet. The commands were enhanced/added in order to provide protection against older software application package which could inadvertently cause system compatibility problems. The modifications/additions are fully backward compatible with the 82077AA which do not support the enhancements.

6.3.1 PERPENDICULAR MODE

The PERPENDICULAR MODE Command is enhanced to allow the system designers to designate specific drives as Perpendicular recording drives. This enhancement is made so that the system designer does not have to worry about older application software packages which bypass their system's FDC (Floppy Disk Controller) routines. The enhancement will also allow data transfers between Conventional and Perpendicular drives without having to issue PERPENDICULAR MODE commands between the accesses of the two different drives, nor having to change write pre-compensation values. The following is an explanation of how this enhancement is implemented:

With the old implementation, the user must properly program both the PERPENDICULAR MODE command and write pre-compensation value before accessing either a Conventional or Perpendicular drive. These programmed values apply to all drives (D0–D3) which the 82077SL may access. It should also be noted that any form of RESET "Hardware" or "Software" will configure the PERPENDICULAR MODE command for Conventional mode (GAP and WGATE = "0").

With the enhanced implementation, both the GAP and WGATE bits have the same affects as the old implementation except for when they are both programmed for value of "0" (Conventional mode). For the case when both GAP and WGATE equal "0" the PERPENDICULAR MODE command will have the following effect on the 82077SL: 1) If any of the new bits D0, D1, D2, and D3 are programmed to "1" the corresponding drive will automatically be programmed for Perpendicular mode (ie: GAP2 being

Old PERPENDICULAR MODE command:

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
PERPENDICULAR MODE										
Command	W	0	0	0	1	0	0	1	0	Command
	W	0	0	0	0	0	0	GAP	WGATE	Code

NOTE:
For the definition of GAP and WGATE bits see Table 6-11 and Section 6.2.11 of the data sheet.
For the Enhanced PERPENDICULAR MODE command definition see Table 6-1.

written during a write operation, the programmed Data Rate will determine the length of GAP2.), and data will be written with 0 ns write pre-compensation. 2) any of the new bits (D0–D3) that are programmed for "0" the designated drive will be programmed for Conventional Mode and data will be written with the currently programmed write pre-compensation value. 3) Bits D0, D1, D2, and D3 can only be over written when the OW bit is written as a "1". The status of these bits can be determined by interpreting the eighth result byte of the enhanced DUMPREG Command (See Section 6.3.3). (Note: if either the GAP or WGATE bit is a "1", then bits D0–D3 are ignored.)

"Software" and "Hardware" RESET will have the following effects on the enhanced PERPENDICULAR MODE command:

1) "Software" RESETs (Reset via DOR or DSR registers) will only clear GAP and WGATE bits to "0", D3, D2, D1, and D0 will retain their previously programmed values.
2) "Hardware" RESETs (Reset via pin 32) will clear all bits (GAP, Wgate, D0, D1, D2, and D3) to "0" (All Drives Conventional Mode).

6.3.2 LOCK

In order to protect a system with long DMA latencies against older application software packages that can disable the 82077SL's FIFO the following LOCK Command has been has been retained in the 82077SL's command set: [Note: This command should only be used by the system's FDC routines, and ISVs (Independent Software Vendors) should refrain from using it. If an ISV's application calls for having the 82077SL FIFO disabled a CONFIGURE Command should be used to toggle the EFIFO (Enable FIFO) bit. ISV can determine the value of the LOCK bit by interpreting the eighth result byte of an DUMPREG Command (See Section 6.3.3).]

The LOCK command defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to a "1" all subsequent "software" RESETs by the DOR and DSR registers will not change the previously set parameter values in the CONFIGURE command. When the LOCK bit is set to a "0" "software" RESETs by the DOR or DSR registers will return these parameters to their default values (See Section 6.2.7). All "hardware" Resets by pin 32 will set the LOCK bit to a "0" value, and will return EFIFO, FIFOTHR, and PRETRK to their default values. A Status byte is returned immediately after issuing the command byte. This Status byte reflects the value of the Lock bit set by the command byte. (Note: No interrupts are generated at the end of this command.)

6.3.3 ENHANCED DUMPREG COMMAND

To accommodate the new LOCK command and enhanced PERPENDICULAR MODE command the eighth result byte of DUMPREG command has been modified in the following manner:

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
		DUMPREG								
Result	R	Eighth Result Byte — Undefined —								Old
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	Enhanced

NOTES:
1. Data bit 7 reflects the status of the new LOCK bit set by the LOCK Command.
2. Data Bits D0–D5 reflect the status for bits D3, D2, D1, D0, GAP and WGATE set by the PERPENDICULAR MODE Command.

7.0 STATUS REGISTER ENCODING

The contents of these registers are available only through a command sequence.

7.1 Status Register 0

Bit No.	Symbol	Name	Description
7, 6	IC	Interrupt Code	00-Normal termination of command. The specified command was properly executed and completed without error. 01-Abnormal termination of command. Command execution was started, but was not successfully completed. 10-Invalid command. The requested command could not be executed. 11-Abnormal termination caused by Polling.
5	SE	Seek End	The 82077SL completed a SEEK or RECALIBRATE command, or a READ or WRITE with implied seek command.
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the RECALIBRATE command. 2. The RELATIVE SEEK command causes the 82077SL to step outward beyond Track 0.
3	—	—	Unused. This bit is always "0".
2	H	Head Address	The current head address.
1, 0	DS1, 0	Drive Select	The current selected drive.

7.2 Status Register 1

Bit No.	Symbol	Name	Description
7	EN	End of Cylinder	The 82077SL tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data Command.
6	—	—	Unused. This bit is always "0".
5	DE	Data Error	The 82077SL detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the 82077SL does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3	—	—	Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. READ DATA, READ DELETED DATA command, the 82077SL did not find the specified sector. 2. READ ID command, the 82077SL cannot read the ID field without an error. 3. READ TRACK command, the 82077SL cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the 82077SL is executing a WRITE DATA, WRITE DELETED DATA, or FORMAT TRACK command.
0	MA	Missing Address Mark	Any one of the following: 1. The 82077SL did not detect an ID address mark at the specified track after encountering the index pulse from the IDX pin twice. 2. The 82077SL cannot detect a data address mark or a deleted data address mark on the specified track.

7.3 Status Register 2

Bit No.	Symbol	Name	Description
7	—	—	Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: 1. READ DATA command, the 82077SL encounters a deleted data address mark. 2. READ DELETED DATA command, the 82077SL encounters a data address mark.
5	DD	Data Error in Data Field.	The 82077SL detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82077SL.
3	—	—	Unused. This bit is always "0".
2	—	—	Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82077SL and is equal to FF hex which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The 82077SL cannot detect a data address mark or a deleted data address mark.

7.4 Status Register 3

Bit No.	Symbol	Name	Description
7	—	—	Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5	—	—	Unused. This bit is always "1".
4	T0	TRACK 0	Indicates the status of the TRK0 pin.
3	—	—	Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1, 0	DS1, 0	Drive Select	Indicates the status of the DS1, DS0 pins.

8.0 COMPATIBILITY

The 82077SL was designed with software compatibility in mind. It is a fully backwards compatible solution with the older generation 8272A and NEC765A/B disk controllers. The 82077SL also implements on-board registers for compatibility with the Personal System/2s as well as PC/AT and PC/XT floppy disk controller subsystems. The 82077SL is fully compatible with Intel's 386SL™ Microprocessor Superset. The 82077SL represents a superset of features that are available on 82077AA. Upon a hardware reset of the 82077SL, all registers, functions and enhancements default to a PS/2, PC/AT, or PS/2 Model 30 compatible operating mode depending on how the IDENT and MFM pins are sampled during Hardware Reset.

8.1 Register Set Compatibility

The register set contained within the 82077SL is a culmination of hardware registers based on the architectural growth of the IBM personal computer line. Table 8-1 indicates the registers required for compatibility based on the type of computer.

Table 8-1. 82077SL Register Support

82077SL Register	8272A	82072	PC/XT	PC/AT	PS/2	Mod 30
SRA					X	X
SRB					X	X
DOR			X	X	X	X
MSR	X	X	X	X	X	X
DSR		X				
Data (FIFO)	X	X	X	X	X	X
DIR				X	X	X
CCR		X*		X	X	X

*CCR is emulated by DSR in an 82072 PC/AT design.

8.2 PS/2 vs. AT vs. Model 30 Mode

To maintain compatibility between PS/2, PC/AT, and Model 30 environments the IDENT and MFM pins are provided. The 82077SL is placed into the proper mode of operations upon Hardware RESET with the appropriate settings of the IDENT and MFM pins. The proper settings of the IDENT and MFM pins are described in IDENT's pin description. Differences between the three modes are described in the following sections.

8.2.1 PS/2 MODE

IDENT strapped low causes the polarity of DENSEL to be active low for high (500 Kbps/1 Mbps) data rates (typically used for 3.5" drives). This polalrity of DENSEL assumes INVERT# to be low. A comprehensive description of DENSEL behavior is given in Table 2-6.

The $\overline{\text{DMAGATE}}$ bit in the Digital Output Register (DOR) will not cause the DRQ or INT output signals to tristate. This maintains consistency with the operation of the floppy disk controller subsystem in the PS/2 architecture.

TC is an active low input signal that is internally qualified by $\overline{\text{DACK}}$ being active low.

8.2.2 PC/AT MODE

IDENT strapped high causes the polarity of DENSEL to be active high for high (500 Kbps/1 Mbps) data rates (typically used for 5.25" drives). This polarity of DENSEL assumes INVERT# to be low. A comprehensive description of DENSEL behavior is given in Table 2-6.

If the $\overline{\text{DMAGATE}}$ bit is written to a "0" in the Digital Output Register (DOR), DRQ and INT will tristate. If $\overline{\text{DMAGATE}}$ is written to a "1", then DRQ and INT will be driven appropriately by the 82077SL.

TC is an active high input signal that is internally qualified by DACK# being active low.

8.2.3 MODEL 30 MODE

IDENT strapped low causes the polarity of DENSEL to be active low for high (500 Kbps/1 Mbps) data rates (typically used for 3.5" drives). This polarity of DENSEL assumes INVERT# to be low. A comprehensive description of DENSEL behavior is given in Table 2-6.

$\overline{\text{DMAGATE}}$ and TC function the same as in PC/AT Mode.

8.3 Compatibility with the FIFO

The FIFO of the 82077SL is designed to be transparent to non-FIFO disk controller software developed on the older generation 8272A standard. Operation of the 82077SL FIFO can be broken down into two tiers of compatibility. For first tier compatibility, the FIFO is left in the default disabled condition upon a "Hardware" reset (via pin 32). In this mode the FIFO operates in a byte mode and provides complete compability with non-FIFO based software. For second tier compatibility, the FIFO is enabled via the CONFIGURE command. When the FIFO is enabled, it will temporarily enter a byte mode during the command and result phase of disk controller operation. This allows for compatible operation when interrogating the Main Status Register (MSR) for the purpose of transferring a byte at a time to or from the disk controller. For normal disk controller applications, the system designer can still take advantage of the FIFO for time critical data transfers during the execution phase and not create any conflicts with non-FIFO software during the command or result phase.

In some instances, use of the FIFO in any form has conflicted with certain specialized software. An example of a compatibility conflict using the FIFO is with software that monitors the progress of a data transfer during the execution phase. If the software assumed the disk controller was operating in a single byte mode and counted the number of bytes transferred to or from the disk controller to trigger some time dependent event on the disk media (i.e. head position over a specific data field), the same software will not have an identical time relationship if the FIFO is enabled. This is because the FIFO allows data to be queued up, and then burst trans-

ferred across the host bus. To accommodate software of this type, it is recommended that the FIFO be disabled.

8.4 Drive Polling

The 82077SL supports the polling mode of the older generation 8272A. This mode is enabled upon a reset and can be disabled via the CONFIGURE command. This mode is supported for the sole purpose of providing backwards compatibility with software that expects it's presence.

The intended purpose of drive polling dates back to 8" drives as a means to monitor any change in status for each disk drive present in the system. Each of the drives is selected for a period of time and its READY signal sampled. After a delay, the next drive is selected. Since the 82077SL does not support READY in this capacity (internally tied true), the polling sequence is only simulated and does not affect the drive select lines (DS0–DS3) when it is active. If enabled, it occurs whenever the 82077SL is waiting for a command or during SEEKs and RECALIBRATEs (but not IMPLIED SEEKs). Each drive is assumed to be not ready after a reset and a "ready" value for each drive is saved in an internal register as the simulated drive is polled. An interrupt will be generated on the first polling loop because of the initial "not ready" status. This interrupt must be followed with a SENSE INTERRUPT STATUS command from the host to clear the interrupt condition for each of the four logical drives.

9.0 PROGRAMMING GUIDELINES

Programming the 82077SL is identical to any other 8272A compatible disk controller with the exception of some additional commands. For the new designer it is useful to provide some guidelines on how to program the 82077SL. A typical disk operation involves more than issuing a command and waiting for the results. The control of the floppy disk drive is a low level operation that requires software intervention at different stages. New commands and features have been added to the 82077SL to reduce the complexity of this software interface.

9.1 Command and Result Phase Handshaking

Before a command or parameter byte can be issued to the 82077SL, the Main Status Register (MSR) must be interrogated for a ready status and proper FIFO direction. A typical floppy controller device driver should contain a subroutine for sending command or parameter bytes. For this discussion, the routine will be called "Send_byte" with the flowchart shown in Figure 9-1.

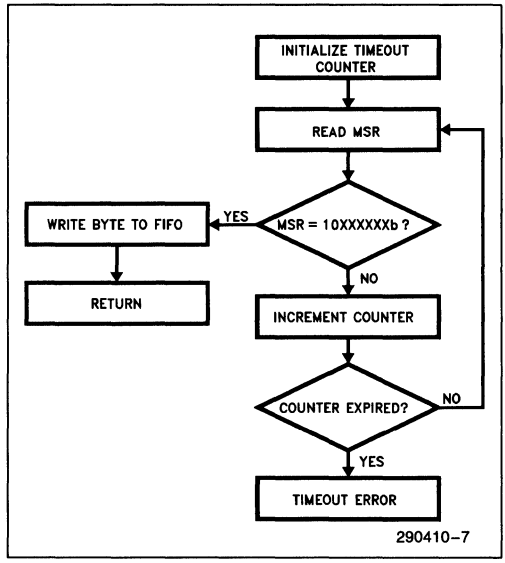


Figure 9-1. Send_Byte Routine

The routine loops until RQM is 1 and DIO is 0 indicating a ready status and FIFO direction is inward. If this condition is true, the 82077SL is ready to accept a command or parameter byte. A timeout counter is used to insure software response within a reasonable amount of time in case of no response by the 82077SL. As a note, the programmer must be careful how the maximum delay is chosen to avoid unnecessary timeouts. For example, if a new command is issued when the 82077SL is in the middle of a polling routine, the MSR will not indicate a ready status for the next parameter byte until the polling sequence completes the loop. This could cause a delay between the first and second bytes of up to 250 μs (@ 250 Kbps). If polling is disabled, this maximum delay is 175 μs. There should also be enough timeout margin to accommodate a shift of the software to a higher speed system. A timeout value that results in satisfactory operation on a 16 MHz CPU might fail when the software is moved to a system with a 25 MHz CPU. A recommended solution is to derive the timeout counter from a system hardware counter that is fixed in frequency from CPU clock to CPU clock.

For reading result bytes from the 82077SL, a similar routine is used. Figure 9-2 illustrates the flowchart for the routine "Get_byte". The MSR is polled until

RQM is 1 and DIO is 1, which indicates a ready status and outward FIFO direction. At this point, the host can read a byte from the FIFO. As in the Send_byte routine, a timout counter should be incorporated in case of a disk controller lock-up condition. For example, if a disk was not inserted into the disk drive at the time of a read operation, the controller would fail to receive the index pulse and lock-up since the index pulses are required for termination of the execution phase.

9.2 Initialization

Initializing the 82077SL involves setting up the appropriate configuration after a reset. Parameters set by the SPECIFY command are undefined after a system reset and will need to be reinitialized. CONFIGURE command parameters default to a known state after a system reset but will need to be reinitialized if the system requirements are different from the default settings. The flowchart for the recommended initialization sequence of the 82077SL is shown in Figure 9-3.

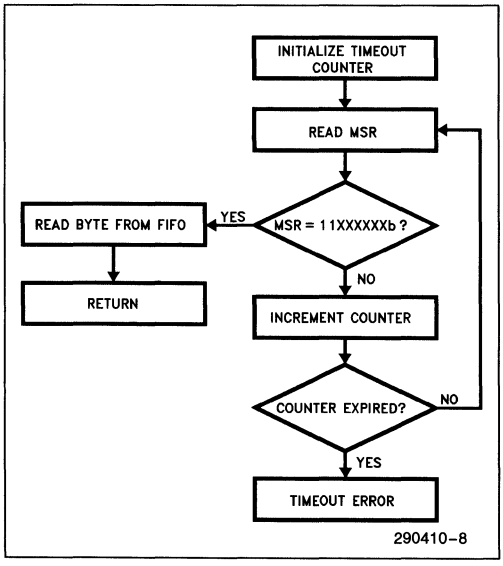


Figure 9-2. Get_Byte Routine

Following a reset of the 82077SL, the Configuration Control Register (CCR) should be reinitialized for the appropriate data rate. An external reset via the RESET pin will cause the data rate and write precompensation values to default to 250 Kbps (10b) and 125 ns (000b) respectively. Since the 125 ns write precompensation value is optimal for the 5¼" and 3½" disk drive environment, most applications will not require the value to be changed in the initialization sequence. As a note, a software reset issued via the DOR or DSR will not affect the data rate or write precompensation values. But it is recommended as a safe programming practice to always program the data rate after a reset, regardless of the type.

Since polling is enabled after a reset of the 82077SL, four SENSE INTERRUPT STATUS commands need to be issued afterwards to clear the status flags for each drive. The flowchart in Figure 9-3 illustrates how the software clears each of the four interrupt status flags internally queued by the 82077SL. It should be noted that although four SENSE INTERRUPT STATUS commands are issued, the INT pin is only active until the first SENSE INTERRUPT STATUS command is executed.

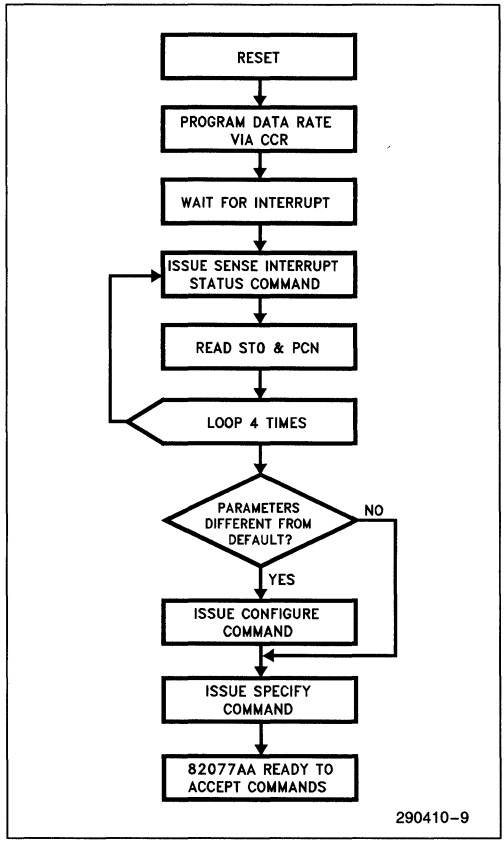


Figure 9-3. Initialization Flowchart

As a note, if the CONFIGURE command is issued within 250 μs of the trailing edge of reset (@ 1 Mbps), the polling mode of the 82077SL can be disabled before the polling initiated interrupt occurs. Since polling stops when the 82077SL enters the command phase, it is only time critical up to the first byte of the CONFIGURE command. If disabled in time, the system software no longer needs to issue the four SENSE INTERRUPT STATUS commands to clear the internal interrupt flags normally caused by polling.

The CONFIGURE command should also be issued if the system requirements are different from the default settings (as described in Section 6.2.7). For example, the CONFIGURE command can be used to enable the FIFO, set the threshold, and enable Implied Seeks.

The non-DMA mode flag, step rate (SRT), head load (HLT), and head unload times (HUT) programmed by the SPECIFY command do not default to a known state after a reset. This behavior is consistent with the 8272A and has been preserved here for compatibility. Thus, it is necessary to always issue a SPECIFY command in the initialization routine.

9.3 Recalibrates and Seeks

Commands that position the disk head are different from the typical READ/WRITE/FORMAT command in the sense that there is no result phase. Once a RECALIBRATE, SEEK, or RELATIVE SEEK command has been issued, the 82077SL will return a ready status in the Main Status Register (MSR) and perform the head positioning operation as a background task. When the seek is complete, the 82077SL will assert the INT signal to request service. A SENSE INTERRUPT STATUS command should then be asserted to clear the interrupt and read the status of the operation. Since the drive and motor enable signals are directly controlled through the Digital Output Register (DOR) on the 82077SL, a write to the DOR will need to precede the RECALIBRATE or SEEK command if the drive and motor is not already enabled. Figure 9-4 shows the flow chart for this operation.

9.4 Read/Write Data Operations

A read or write data operation requires several steps to complete successfully. The motor needs to be turned on, the head positioned to the correct cylinder, the DMA controller initialized, the read or write command initiated, and an error recovery scheme implemented. The flowchart in Figure 9-5 highlights a recommended algorithm for performing a read or write data operation.

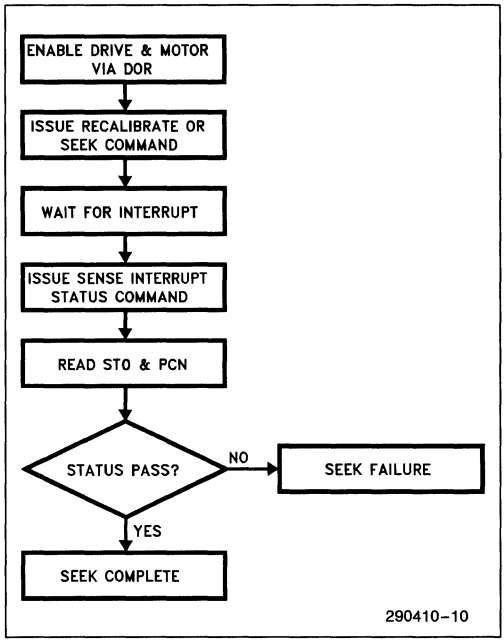


Figure 9-4. Recalibrate and Seek Operations

Before data can be transferred to or from the diskette, the disk drive motor must be brought up to speed. For most 3½" disk drives, the spin-up time is 300 ms, while the 5¼" drive usually requires about 500 ms due to the increased moment of inertia associated with the larger diameter diskette.

One technique for minimizing the motor spin-up delay in the read data case is to begin the read operation immediately after the motor is turned on. When the motor is not initially up to speed, the internal data separator will fail to lock onto the incoming data stream and report a failure in the status registers. The read operation is then repeated until successful status is obtained. There is no risk of a data integrity problem since the data field is CRC validated. But, it is not recommended to use this technique for the write data operation even though it requires successful reading of the ID field before the write takes place. The data separator performance of the 82077SL is such that locking to the data stream could take place while the motor speed variation is still significant. This could result in errors when an attempt is made to read the disk media by other disk controllers that have a narrower incoming data stream frequency bandwidth.

After the motor has been turned on, the matching data rate for the media inserted into the disk drive should then be programmed to the 82077SL via the Configuration Control Register (CCR). The 82077SL

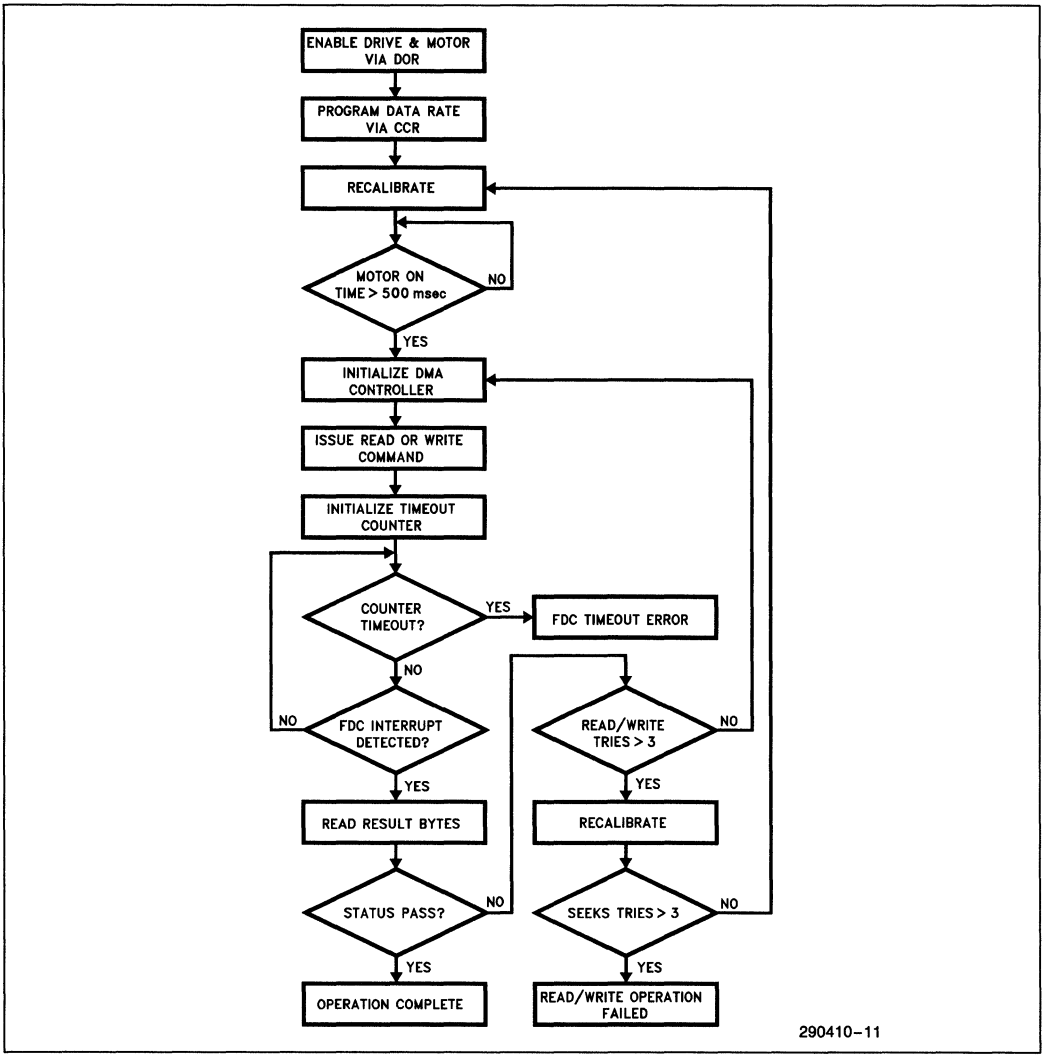


Figure 9-5. Read/Write Operation

is designed to allow a different data rate to be programmed arbitrarily without disrupting the integrity of the device. In some applications, it is required to automatically determine the recorded data rate of the inserted media. One technique for doing this is to perform a READ ID operation at each available data rate until a successful status is returned in the result phase.

If implied seeks are not enabled, the disk drive head must be positioned over the correct cylinder by executing a SEEK command. After the seek is complete, a head settling time needs to be asserted before the read or write operation begins. For most drives, this delay should be a minimum of 15 ms. When using implied seeks, the minimum head settling time can be enforced by the head load time (HLT) parameter designated in the SPECIFY command. For example, a HLT value of 8 will yield an effective head settling time of 16 ms for a programmed data rate of 500 Kbps. Of course if the head is already positioned over the correct cylinder, the head settling time does not need to be enforced.

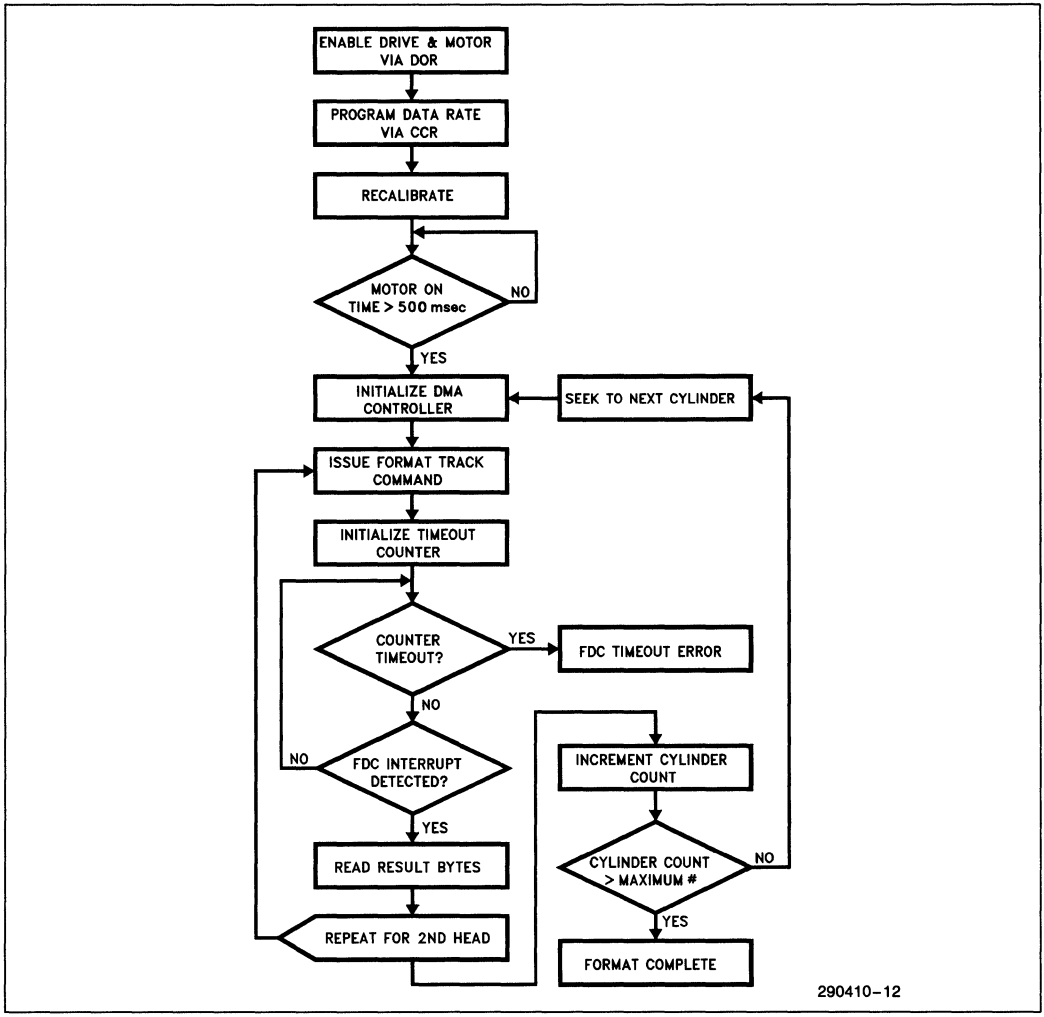


Figure 9-6 Formatting

The DMA controller is then initialized for the data transfer and the read or write command is executed. Typically the DMA controller will assert Terminal Count (TC) when the data transfer is complete. The 82077SL will then complete the current data transfer and assert the INT signal signifying it has entered the result phase. The result phase can also be entered by the 82077SL if an error is encountered or the last sector number equals the End of Track (EOT) parameter.

Based on the algorithm in Figure 9-5, if an error is encountered after reading the result bytes, two more retries are performed by reinitializing the DMA controller and re-issuing the read or write data command. A persisting failure could indicate the seek operation did not achieve proper alignment between the head and the track. The disk head should then be recalibrated and the seek repeated for a maximum of two more tries. Unsuccessful operation after this point should be reported as a disk failure to the operating system.

9.5 Formatting

The disk formatting procedure involves positioning the head on each track and creating a fixed format field used for organizing the data fields. The flowchart in Figure 9-6 highlights the typical format procedure.

After the motor has been turned on and the correct data rate programmed, the disk head is recalibrated to track 0. The disk is then allowed to come up to speed via a 500 ms delay. It is important the disk speed has stabilized before the actual formatting to avoid any data rate frequency variations. Since the format fields contain critical information used by the data separator of the disk controller for synchronization purposes, frequency stability of the data stream is imperative for media interchangeability among different systems.

The ID field data created on the disk during the format process is provided by the DMA controller during the execution phase. The DMA controller is initialized to send the C, H, R and N values for each sector ID field. For example, to format cylinder 7, on head 1, with 9 sectors, and a sector size of 2 (512 bytes), the DMA controller should be programmed to transfer 36 bytes (9 sectors x 4 bytes per sector) with the following data field: 7,1,1,2, 7,1,2,2, 7,1,3,2, ... 7,1,9,2. Since the values provided to the 82077SL during the execution phase of the format command are directly recorded as the ID fields on the disk, the data contents can be arbitrary. Some forms of copy protection have been implemented by taking advantage of this capability.

After each head for a cylinder has been formatted, a seek operation to the next cylinder is performed and the format process is repeated. Since the FORMAT TRACK command does not have implied seek capability, the SEEK command must be used. Also, as discussed in Section 9-2, the head settling time needs to be adhered to after each seek operation.

9.6 Verifies

In some applications, the sector data needs to be verified immediately after each write operation. The verify technique historically used with the 8272A or 82072 disk controller involved reinitializing the DMA controller to perform a read transfer or verify transfer (DACK# is asserted but not RD#) immediately after each write operation. A read command is then to be issued to the disk controller and the resulting status indicates if the CRC validated the previously written data. This technique has the drawback of requiring additional software intervention by having to reprogram the DMA controller between each sector write operation. The 82077SL supports this older verify technique but also provides a new VERIFY command that does not require the use of the DMA controller. This is also available in 82077AA.

To verify a write data transfer or format track operation using the VERIFY command, the software simply issues the command with the same format as a READ DATA command but without the support of the DMA controller. The 82077SL will then perform a disk read operation without a host data transfer. The CRC will be calculated for each sector read and compared against the value stored on the disk. When the VERIFY command is complete, the status register will report any detected CRC errors.

9.7 Powerdown State and Recovery

The two power management modes coupled with the internal oscillator power management forms an important consideration for programming the 82077SL. The recovery of 82077SL and the time it takes to achieve complete recovery depends on how 82077SL is powered down and how it is awakened. The following sections describe all the programming concerns and subtleties involved in using power management features of the 82077SL.

9.7.1 OSCILLATOR POWER MANAGEMENT

Section 4.1 covers the power management scheme involved in powering down of both an internal and an external oscillator. Both types of oscillators face drop out effects and require recovery times on the order of tens of milliseconds (this may be objectionable to some application software). This means that if the oscillator is powered down then it is imperative for the software to assure enough time for the oscillator to recover to a stable state. Oscillator power management must be controlled by the system software especially to maintain software transparency. In cases where the system goes into a standby mode (by user request or system timeout), the power management software can turn off the oscillator to conserve power. Complete recovery from an oscillator powerdown state requires the software to turn on the oscillator sufficiently ahead of awakening the 82077SL.

9.7.2 PART POWER MANAGEMENT

The part powerdown and wake up modes are covered in Section 4.2 in detail. This section is meant to address the programming concerns for the part (excluding the oscillator) during these modes.

9.7.2.a Powerdown Modes

For both types of powerdown modes—DSR powerdown and auto powerdown, if reset is used to exit the part from powerdown then the internal microcontroller will go through a standard sequence: register initialization followed after some delay by an interrupt.

Software transparency in auto powerdown mode is preserved by MSR retaining the value of 80H which indicates that the part is ready to receive a command. This feature allows the part to powerdown while maintaining its responsiveness to any application software.

9.7.2.b Wake Up Modes

Wake up from DSR powerdown results in the part being internally reset and all present status being lost. During DSR powerdown the RQM bit in the MSR is set. A software or hardware reset will wake up the part.

The case for wake up from auto powerdown is different. The BIOS and application software are very sensitive to delays involved in writing the first command bytes to the 82077SL. Most programs have short error timeouts in these cases. Such programs would not tolerate any floppy disk controller that was unable to receive the first byte of a command at any time. The following describes how 82077SL uniquely sustains its software transparency during wake up sequences.

Prior to writing a command to 82077SL, it is first necessary to read the MSR to ensure that the 82077SL is ready (RQM bit must be set) to receive the command. When the part detects a MSR read, it assumes that another command will follow and begins the wake up process. While the part is waking up it does not change the state of the MSR (MSR = 80H) and is able to receive the command in the FIFO. At this point one of the two following scenarios can occur.

— No other command is sent subsequent to the MSR read. The part wakes up and initializes the minimum power up timer. Upon the expiration of this timer the part is once again put in powerdown state.

— Another command follows the MSR read. If the command is send during the part's recovery from powerdown, the part remembers the command, clears the RQM bit (to prevent further bytes being written) and acts on the command once it is fully awake.

If the MSR was not checked prior to writing of a command, the part will proceed as stated above with the RQM bit cleared and the command byte held until the internal microcontroller is ready. Writing the motor enable bits in DOR active will initiate the wake up sequence with RQM set high, ready to receive any command.

As it is clear from the above discussion, the immediate access to the floppy disk controller for the first command byte is vital to software transparency. The recovery of the part from powerdown may involve a delay after the first command byte has been issued. However, all programs have tolerance for the delay after the first command byte is issued. In a powered up chip, it is possible for the microcontroller to be in its "polling loop". As a result the tolerance for this delay provides an excellent window for recovery of the part.

10.0 DESIGN APPLICATIONS

10.1 PC/AT Floppy Disk Controller

This section presents a design application of a PC/AT compatible floppy disk controller. With an 82077SL, a 24 MHz crystal, a resistor package, and a device chip select, a complete floppy disk controller can be built. The 82077SL integrates all the necessary building blocks for a reliable and low cost solution. But before we discuss the design application using the 82077SL, it is helpful to describe the architecture of the original IBM PC/AT floppy disk controller design that uses the 8272A.

10.1.1 PC/AT FLOPPY DISK CONTROLLER ARCHITECTURE

The standard IBM PC/AT floppy disk controller using the 8272A requires 34 devices for a complete solution. The block diagram in Figure 10-1 illustrates the complexity of the disk controller. A major portion of this logic involves the design of the data separator. The reliability of the disk controller is primarily dictated by the performance and stability of the data separator. Discrete board level analog phase lock loops generally offer good bit jitter margins but suffer from instability and tuning problems in the manufacturing stage if not carefully designed. While digital data separator designs offer stability and generally a lower chip count, they suffer from poor performance in the recovery of data.

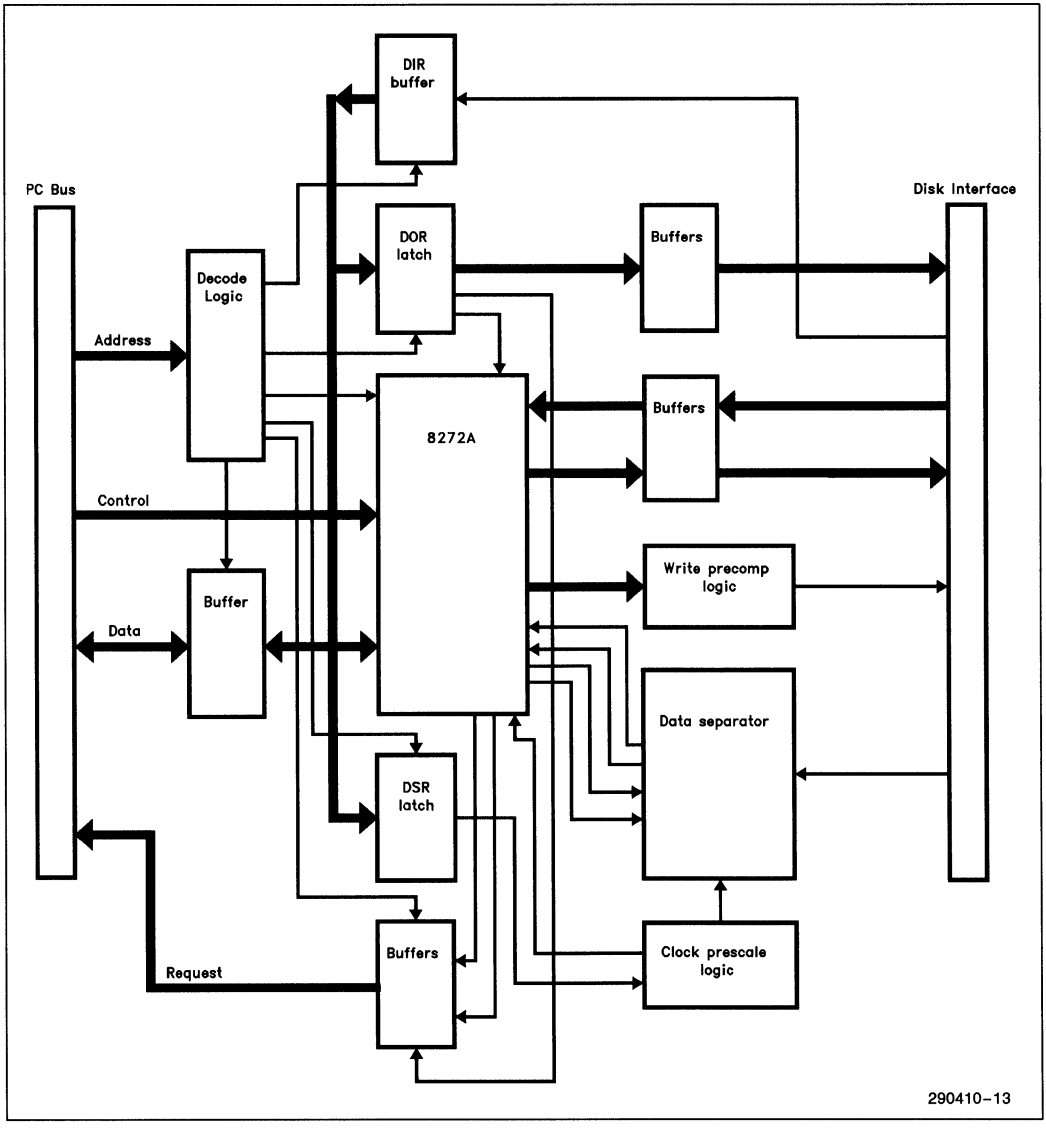


Figure 10-1. Standard IBM PC/AT Floppy Disk Controller

Table 10-1 indicates the drive and media types the IBM PC/AT disk controller can support. This requires the data separator to operate at three different data rates: 250 Kbps, 300 Kbps and 500 Kbps. Clocks to the data separator and disk controller need to be prescaled correspondingly to accommodate each of these data rates. The clock prescaling is controlled by the Data rate Select Register (DSR). Supporting all three data rates can compromise the performance of the phase lock loop (PLL) if steps are not taken in the design to adjust the performance parameters of the PLL with the data rate.

Table 10-1. Standard PC/AT Drives and Media Formats

Capacity	Drive Speed	Data Rate	Sectors	Cylinders
360 Kbyte	300 RPM	250 Kbps	9	40
*360 Kbyte	360 RPM	300 Kbps	9	40
1.2 Mbyte	360 RPM	500 Kbps	15	80

*360 Kbyte diskette in a 1.2 Mbyte drive.

The PC/AT disk controller provides direct control of the drive selects and motors via the Digital Output Register (DOR). As a result, drive selects on the 8272A are not utilized. This places drive selection and motor speed-up control responsibility with the software. The DOR is also used to perform a software reset of the disk controller and tristate the DRQ2 and IRQ6 output signals on the PC bus.

The design of the disk controller also requires address decode logic for the disk controller and register set, buffering for both the disk interface and PC bus, support for write precompensation and monitoring of the disk change signal via a separate read only register (DIR). An I/O address map of the complete register set for the PC/AT floppy disk controller is shown in Table 10-2.

Table 10-2. I/O Address Map for the PC/AT

I/O Address	Access Type	Description
3F0H	—	Unused
3F1H	—	Unused
3F2H	Write	Digital Output Register
3F3H	—	Unused
3F4H	Read	Main Status Register
3F5H	Read/Write	Data Register
3F6H	—	Unused
3F7H	Write	Data Rate Select Register
3F7H	Read	Digital Input Register

10.1.2 82077SL PC/AT SOLUTION

The 82077SL integrates the entire PC/AT controller design with the exception of the address decode on a single chip. The schematic for this solution is shown in Figure 10-2. The chip select for the 82077SL is generated by a 16L8 PAL that is programmed to decode addresses 03F0H thru 03F7H when AEN (Address Enable) is low. The programming equation for the PAL is shown in a ABEL file format in Figure 10-3. An alternative address decode solution could be provided by using a 74LS133 13 input NAND gate and 74LS04 inverter to decode A3–A14 and AEN. Although the PC/AT allows for a 64K I/O address space, decoding down to a 32K I/O address space is sufficient with the existing base of add-in cards.

A direct connection between the disk interface and the 82077SL is provided by on-chip output buffers with a 40 mA sink capability. Open collector outputs from the disk drive are terminated at the disk controller with a 150Ω resistor pack. The 82077SL disk interface inputs contain a schmitt trigger input structure for higher noise immunity. The host interface is a similar direct connection with 12 mA sink capabilities on DB0–DB7, INT and DRQ.

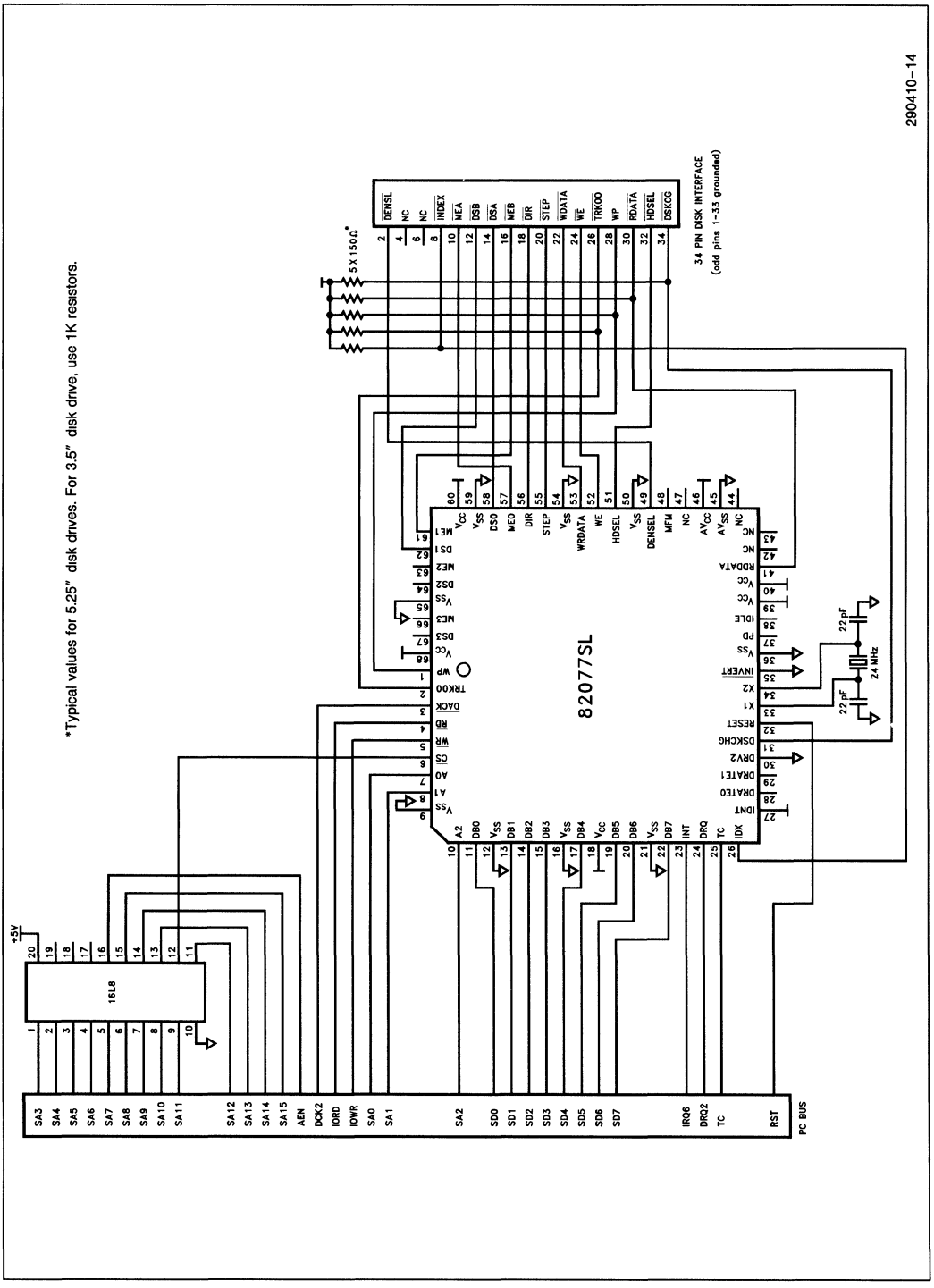


Figure 10-2. 82077SL PC/AT Floppy Disk Controller

```
MODULE PCAT077_LOGIC;

TITLE "82077SL PC/AT FLOPPY DISK CONTROLLER';
PCAT077 DEVICE "P16L8';

GND,VCC                              PIN 10,20;
SA3,SA4,SA5,SA6,SA7,SA8,SA9,SA10     PIN 1,2,3,4,5,6,7,8;
SA11,SA12,SA13,SA14,SA15,AEN         PIN 9,11,13,14,15,16;
CS077_                               PIN 12;

EQUATIONS

"" CHIP SELECT FOR THE 82077SL (3F0H -- 3F7H)

CS077_ = !(!SA15 & !SA14 & !SA13 & !SA12 & !SA11 & !SA10 &
          SA9 & SA8 & SA7 & SA6 & SA5 & SA4 & !SA3 & !AEN);

END PCAT077_LOGIC
```

Figure 10-3. PAL Equation File for a PC/AT Compatible FDC Board

10.2 3.5" Drive Interfacing

The 82077SL is designed to interface to both 3.5" and 5.25" disk drives. This is facilitated by the 82077SL by orienting IDENT to get the proper polarity of DENSEL for the disk drive being used. Typically DENSEL is active high for high (500 Kbps/ 1 Mbps) data rates on 5.25" drives. And DENSEL is typically active low for high data rates on 3.5" drives. A complete description of how to orient IDENT to get the proper polarity for DENSEL is given in Table 2-6.

10.2.1 3.5" DRIVES UNDER THE AT MODE

When interfacing the 82077SL floppy disk controller with a 3.5" disk drive in a PC/AT application, it is possible that two design changes will need to be implemented for the design discussed in Section 10.1. Most 3.5" disk drives incorporate a totem pole interface structure as opposed to open collector. Outputs of the disk drive will drive both high or low voltage levels when the drive is selected, and float only when the drive has been deselected. These totem pole outputs generally can only sink or source 4 mA of current. As a result, it is recommended to replace the 150Ω termination resistor pack with a 4.7 KΩ package to pull floating signals inactive. Some other 3.5" drives do have an open collector interface, but have limited sink capability. In these cases, the drive manufacturer manuals usually suggest a 1 KΩ termination.

A second possible change required under "AT mode" operation involves high capacity 3.5" disk drives that utilize a density select signal to switch between media recorded at a 250 Kbps and 500 Kbps data rate. The polarity of this signal is typically inverted for 3.5" drives versus 5.25" drives. Thus, an inverter can be added between the DENSEL output of the 82077SL and the disk drive interface connector when using 3.5" drives.

But drives that do not support both data rates or drives with an automatic density detection feature via an optical sensor do not require the use of the DENSEL signal.

Another method is to change the polarity of IDENT with a drive select signal. ORing RESET with the drive select signal (DS0–3) used for the 3.5" disk drive will produce the proper polarity for DENSEL (assuming INVERT# is low).

10.2.2 3.5" DRIVES UNDER THE PS/2 MODES

If IDENT is strapped to ground, the DENSEL output signal polarity will reflect a typical 3.5" drive mode of operation. That is, DENSEL will be high for 250 Kbps or 300 Kbps and low for 500 Kbps or 1 Mbps (assuming INVERT# is low). Thus the only change from the disk interface shown in Figure 10-2 is to replace the 150Ω termination resistor pack with a value of about 10 KΩ. This will prevent excessive current consumption on the CMOS inputs of the 82077SL by pulling them inactive when the drive(s) are deselected.

10.2.3 COMBINING 5.25″ AND 3.5″ DRIVES

If 5.25″ and 3.5″ drives are to be combined in a design, then steps need to be taken to avoid contention problems on the disk interface. Since 3.5″ drives do not have a large sink capability, the 150Ω termination resistor pack required by 5.25″ drives cannot be used with the 3.5″ drive. To accommodate both drives with the same disk controller, the outputs of the 3.5″ drive should be buffered before connecting to the 82077SL disk interface inputs. The 82077SL inputs are then connected to the necessary resistive termination load for the 5.25″ interface.

The block diagram in Figure 10-4 highlights how a combined interface could be designed. In this example, the 5.25″ drive is connected to drive select 0 (DS0) and the 3.5″ drive is connected to drive select 1 (DS1). DS1 is also used to enable a 74LS244 buffer on the output signals of the 3.5″ drive. The drive select logic of the 82077SL is mutually exclusive and prevents the activation of the buffer and 5.25″ drive at the same time. Since the 74LS244 has an I_{OL} of 24 mA, the termination resistor should be increased to 220Ω. This could impact the reliability of the 5.25″ drive interface if the cable lengths are greater than 5 feet.

To accommodate the polarity reversal of the DENSEL signal for 3.5″ drives, it is routed through an inverter for the 3.5″ drive interface. A 1 KΩ pull-up should be placed on the output of the inverter to satisfy the I_{OH} requirements for the 3.5″ drive when using a 74LS04.

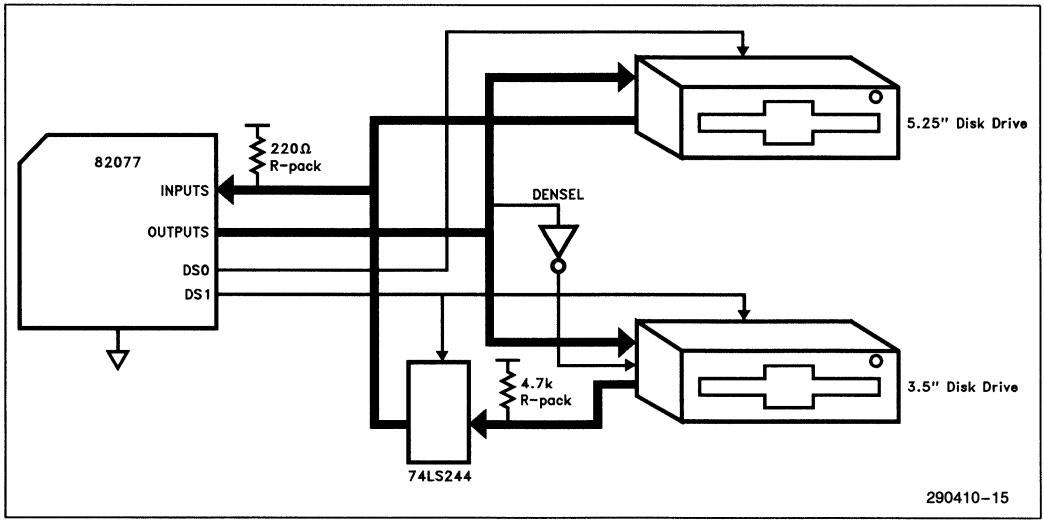


Figure 10-4. Combined 3.5″ and 5.25″ Drive Interface

11.0 D.C. SPECIFICALIFNS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

11.1 Absolute Maximum Ratings

Storage Temperature ..... −65°C to +150°C
Supply Voltage ..... −0.5 to +8.0V
Voltage on Any Input ..... GND − 2V to 6.5V
Voltage on Any Output.. GND − 0.5V to VCC+0.5V
Power Dissipation ..... 1 Watt

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

11.2 D.C. Characteristics

T_A = 0°C to = 70°C, V_{CC} = +5V ±10%, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{ILC}	Input Low Voltage, X1	−0.5	0.8	V	
V_{IHC}	Input High Voltage, X1	3.9	V_{CC} +0.5	V	
V_{IL}	Input Low Voltage (all pins except X1)	−0.5	0.8	V	
V_{IH}	Input High Voltage (all pins except X1)	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage MFM		0.4	V	I_{OL} = 2.5 mA
	DRATE0-1		0.4	V	I_{OL} = 6.0 mA
	DB0-7, INT and DRQ		0.4	V	I_{OL} = 12 mA
	ME0-3, DS0-3, DIR, STP WRDATA, WE, HDSEL and DENSEL		0.4	V	I_{OL} = 40 mA
V_{OH}	Output High Voltage MFM	3.0		V	I_{OH} = −2.5 mA
	All Other Outputs	3.0		V	I_{OH} = −4.0 mA
	All Outputs	V_{CC} − 0.4		V	I_{OH} = −100 µA
	V_{CC} Supply Current (Total)				
I_{CC1}	1 Mbps Data Rate, V_{IL} = V_{SS}, V_{IH} = V_{CC}		45	mA	(Notes 1, 2)
I_{CC2}	1 Mbps Data Rate, V_{IL} = 0.45, V_{IH} = 2.4		50	mA	(Notes 1, 2)
I_{CC3}	500 Kbps Data Rate, V_{IL} = V_{SS}, V_{IH} = V_{CC}		35	mA	(Notes 1, 2)
I_{CC4}	500 Kbps Data Rate, V_{IL} = 0.45, V_{IH} = 2.4		40	mA	(Notes 1, 2)
I_{CCSB}	I_{CC} in Powerdown				(Note 3)
I_{IL}	Input Load Current (all input pins)		10 −10	µA µA	V_{IN} = V_{CC} V_{IN} = 0V
I_{OFL}	Data Bus Output Float Leakage		±10	µA	0.45 < V_{OUT} < V_{CC}

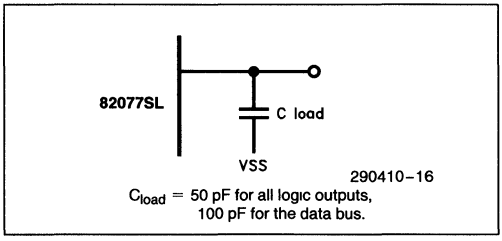
NOTES:
1. The data bus are the only inputs that may be floated.
2. Tested while reading a sync field of "00". Outputs not connected to D.C. Loads.
3. V_{IL} = V_{SS}, V_{IH} = V_{CC}; Outputs not connected to D.C. loads.

Capacitance

C_{IN}	Input Capacitance	10	pF	F = 1 MHz, T_A = 25°C
C_{IN1}	Clock Input Capacitance	20	pF	Sampled, not 100% Tested
$C_{I/O}$	Input/Output Capacitance	20	pF	

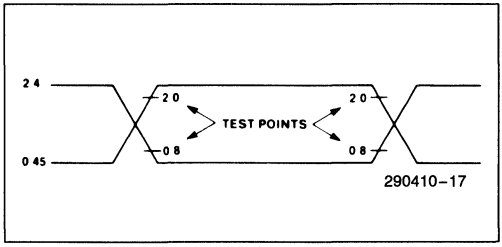
NOTE:
All pins except pins under test are tied to AC ground.

LOAD CIRCUIT



C_{load} = 50 pF for all logic outputs, 100 pF for the data bus.

A. C. TESTING INPUT, OUTPUT WAVEFORM



11.3 Oscillator

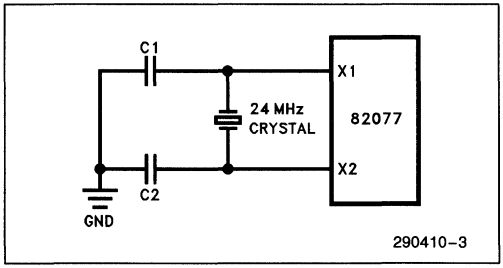


Figure 11-2. Crystal Oscillator Circuit

The 24 MHz clock can be supplied either by a crystal or a MOS level square wave. All internal timings are referenced to this clock or a scaled count which is data rate dependent.

The crystal oscillator must be allowed to run for 10 ms after VCC has reached 4.5V or exiting the POWERDOWN mode to guarantee that it is stable.

Crystal Specifications

Frequency:	24 MHz ±0.1%
Mode:	Parallel Resonant Fundamental Mode
Series Resistance:	Less than 40Ω
Shunt Capacitance:	Less than 5 pF

12.0 A.C. SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit
CLOCK TIMINGS				
t1	Clock Rise Time		10	ns
	Clock Fall Time		10	ns
t2	Clock High Time(7)	16	26	ns
t3	Clock Low Time(7)	16	26	ns
t4	Clock Period	41.66	41.66	ns
t5	Internal Clock Period(3)			
HOST READ CYCLES				
t7	Address Setup to $\overline{RD}$	5		ns
t8	$\overline{RD}$ Pulse Width	90		ns
t9	Address Hold from RD	0		ns
t10	Data Valid from $\overline{RD}$(12)		80	ns
t11	Command Inactive	60		ns
t12	Output Float Delay		35	ns
t13	INT Delay from RD		t5 + 125	ns
t14	Data Hold from $\overline{RD}$	5		ns
HOST WRITE CYCLES				
t15	Address Setup to $\overline{WR}$	5		ns
t16	$\overline{WR}$ Pulse Width	90		ns
t17	Address Hold from WR	0		ns
t18	Command Inactive	60		ns
t19	Data Setup to WR	70		ns
t20	Data Hold from WR	0		ns
t21	INT Delay from WR		t5 + 125	ns
DMA CYCLES				
t22	DRQ Cycle Period(1)	6.5		µs
t23	DACK to DRQ Inactive		75	ns
t23a	DRQ to DACK Inactive	(Note 15)		ns
t24	RD to DRQ Inactive(4)		100	ns
t25	DACK Setup to $\overline{RD}$, $\overline{WR}$	5		ns
t26	DACK Hold from RD, WR	0		ns
t27	DRQ to $\overline{RD}$, $\overline{WR}$ Active(1)	0	6	µs
t28	Terminal Count Width(10)	50		ns
t29	TC to DRQ Inactive		150	ns
RESET				
t30	"Hardware" Reset Width(5)	170		t4
t30a	"Software" Reset Width(5)	(Note 11)		ns
t31	Reset to Control Inactive		2	µs

A.C. SPECIFICATIONS (Continued)

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit
WRITE DATA TIMING				
t32	Write Data Width(6)			ns
DRIVE CONTROL				
t35	DIR Setup to STEP(14)	1.0		µs
t36	DIR Hold from STEP	10		µs
t37	STEP Active Time (High)	2.5		µs
t38	STEP Cycle Time(2)			µs
t39	INDEX Pulse Width	5		t5
t41	WE to HDSEL Change	(Note 13)		ms
READ DATA TIMING				
t40	Read Data Pulse Width	50		ns
f44	PLL Data Rate			
	82077SL		1M	bits/sec
	82077SL-5		500K	bits/sec
t44	Data Rate Period = 1/f44			
tLOCK	Lockup Time		64	t44

NOTES:

1. This timing is for FIFO threshold = 1. When FIFO threshold is N bytes, the value should be multiplied by N and subtract 1.5 µs. The value shown is for 1 Mbps, scales linearly with data rate.
2. This value can range from 0.5 ms to 8.0 ms and is dependent upon data rate and the Specify command value.
3. Many timings are a function of the selected data rate. The nominal values for the internal clock period (t5) for the various data rates are:

1 Mbps	3 x oscillator period = 125 ns
500 Kbps	6 x oscillator period = 250 ns
300 Kbps	10 x oscillator period = 420 ns
250 Kbps	12 x oscillator period = 500 ns

4. If $\overline{DACK}$ transitions before $\overline{RD}$, then this specification is ignored. If there is no transition on $\overline{DACK}$, then this becomes the DRQ inactive delay.
5. Reset requires a stable oscillator to meet the minimum active period.
6. Based on the internal clock period (t5). For various data rates, the Write Data Width minimum values are:

1 Mbps	5 x oscillator period −50 ns = 150 ns
500 Kbps	10 x oscillator period −50 ns = 360 ns
300 Kbps	16 x oscillator period −50 ns = 615 ns
250 Kbps	19 x oscillator period −50 ns = 740 ns

7. Test points for clock high time are 3.5V. Due to transitional times, clock high time max and clock low time max cannot be met simultaneously. Clock high time min and clock low time max cannot be met simultaneously.
8. Based on internal clock period (t5).
9. Jitter tolerance is defined as: $\frac{\text{Maximum bit shift from nominal position}}{\text{1/4 period of nominal data rate}} \times 100\%$

It is a measure of the allowable bit jitter that may be present and still be correctly detected. The data separator jitter tolerance is measured under dynamic conditions that jitters the bit stream according to a reverse precompensation algorithm.

10. TC width is defined as the time that both TC and DACK are active.

A.C. SPECIFICATIONS (Continued)

NOTES: (Continued)

11. The minimum reset active period for a software reset is dependent on the data rate, after the 82077SL has been properly reset using the t30 spec. The minimum software reset period then becomes:

1 Mbps	3 x t4 = 125 ns
500 Kbps	6 x t4 = 250 ns
300 Kbps	10 x t4 = 420 ns
250 Kbps	12 x t4 = 500 ns

12. Status Register's status bits which are not latched may be updated during a Host read operation.
13. The minimum MFM values for WE to HDSEL change (t41) for the various data rates are:

1 Mbps	0.5 ms + [8 x GPL]
500 Kbps	1.0 ms + [16 x GPL]
300 Kbps	1.6 ms + [26.66 x GPL]
250 Kbps	2.0 ms + [32 x GPL]

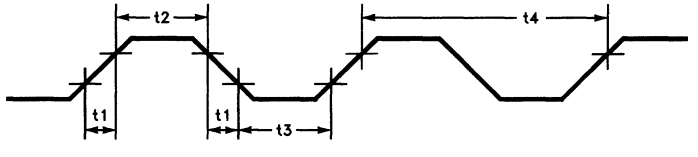
GPL is the size of gap 3 defined in the sixth byte of a Write Command.

14. This timing is a function of the selected data rate as follows:

1 Mbps	1.0 μs Min
500 Kbps	2.0 μs Min
300 Kbps	3.3 μs Min
250 Kbps	4.0 μs Min

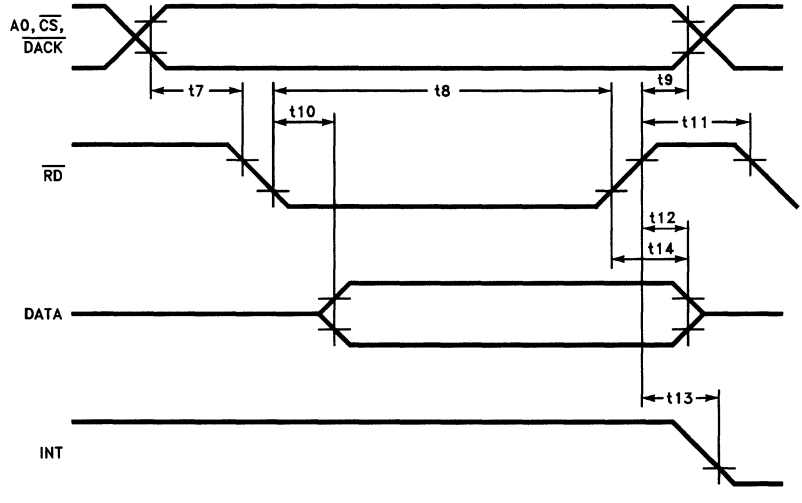
15. This timing is a function of the internal clock period (t5) and is given as (2/3) t5. The values of t5 are shown in Note 3.

CLOCK TIMINGS



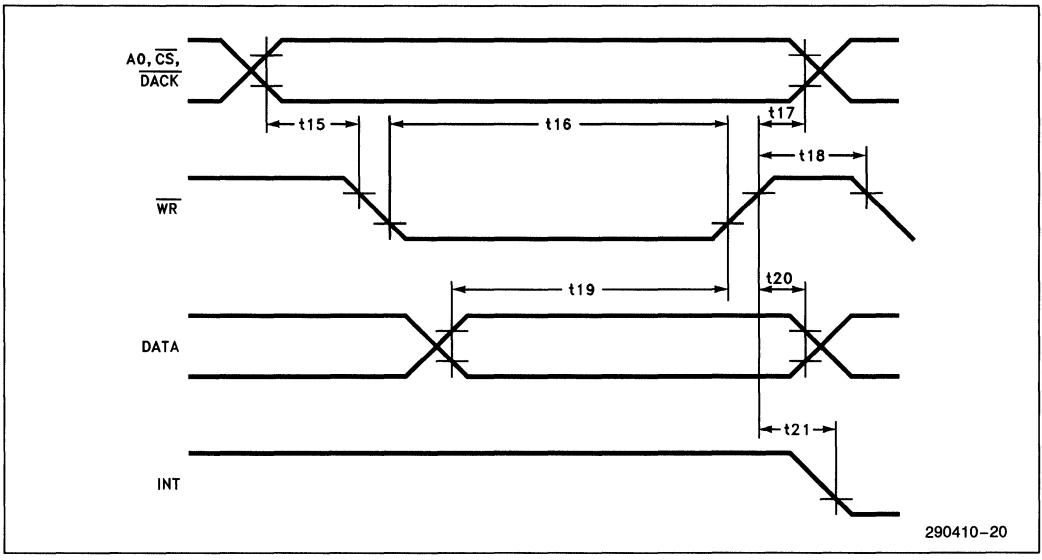
290410-18

HOST READ CYCLES

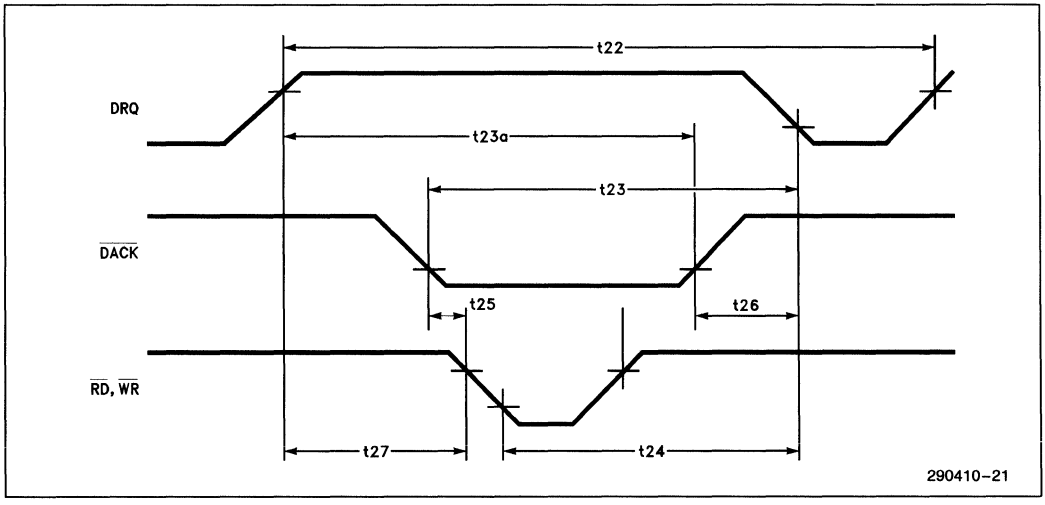


290410-19

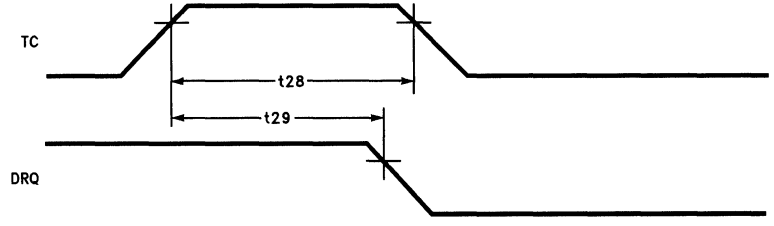
HOST WRITE CYCLES



DMA CYCLES

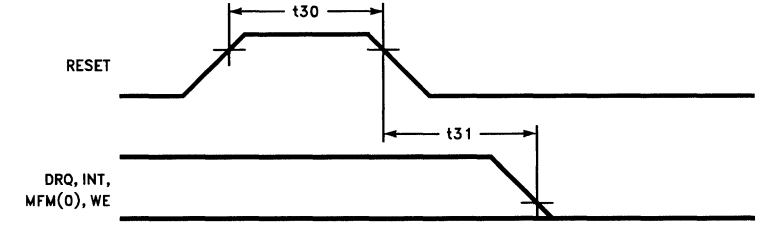


TERMINAL COUNT



290410-22

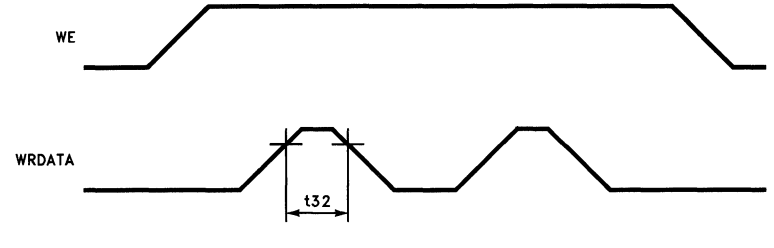
RESET



290410-23

NOTE:
MFM(0) refers to the MFM pin left open during hardware reset.

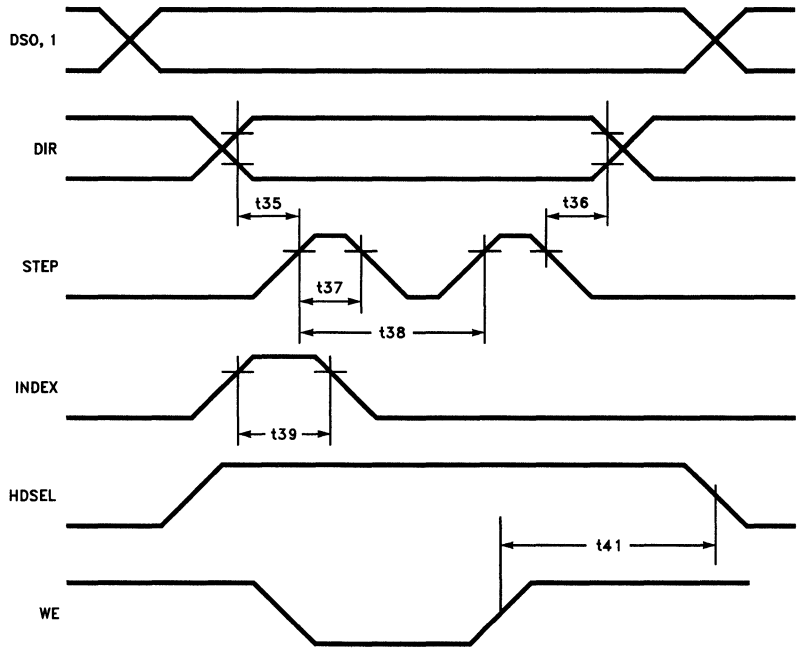
WRITE DATA TIMING



290410-24

NOTE:
Invert high.

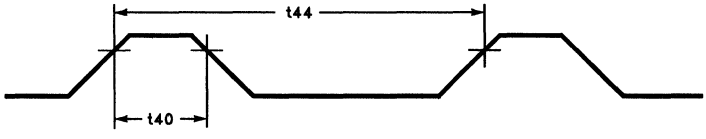
DRIVE CONTROL



290410-25

NOTE:
For overlapped seeks, only one step pulse per drive selection is issued. Non-overlapped seeks will issue all programmed step pulses. Invert high.

INTERNAL PLL



290410-26

NOTE:
Invert high.

13.0 DATA SEPARATOR CHARACTERISTICS FOR FLOPPY DISK MODE

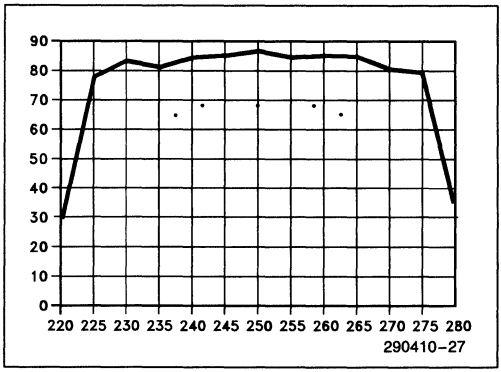


Figure 13-1. Typical Jitter Tolerance vs Data Rate (Capture Range) (250 Kbps)

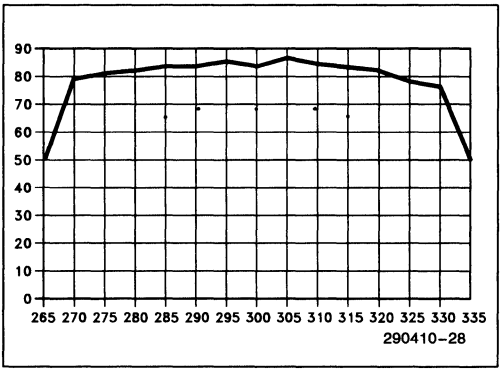


Figure 13-2. Typical Jitter Tolerance vs Data Rate (Capture Range) (300 Kbps)

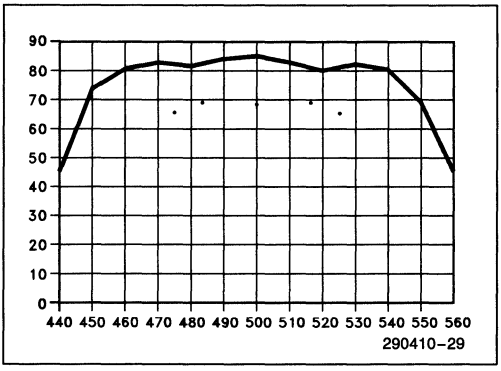


Figure 13-3. Typical Jitter Tolerance vs Data Rate (Capture Range) (500 Kbps)

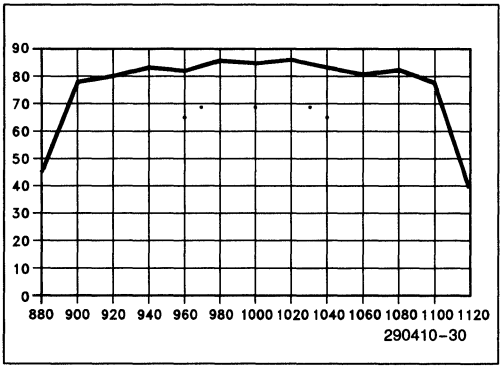


Figure 13-4. Typical Jitter Tolerance vs Data Rate (Capture Range) (1 Mbps), 82077SL-1

Jitter Tolerance measured in percent. See datasheet — Section 3.2.1 capture range expressed as a percent of data rate, i.e., ±3%.

• = Test Points:
250, 300, 500 Kbps are center, ±3% @ 68% jitter, ±5% @ 65% jitter
1 Mbps are center, ±3% @ 68% jitter, ±4% @ 63% jitter

Test points are tested at temperature and V_{CC} limits. Refer to the datasheet. Typical conditions are: room temperature, nominal V_{CC}.

14.0 82077SL 68-Lead PLCC Package Thermal Characteristics

T_A Ambient Temp. (°C)	Typical Values				θ_{ja} (°C/W)	θ_{jc} (°C/W)
	T_c (°C)	T_j (°C)	I_{cc} (mA)	V_{cc} (V)		
70	75	75	30	5.0	36	5

NOTES:
Case Temperature Formula:
$T_c = T_a + P [\theta_{ja} - \theta_{jc}]$
Junction Temperature Formula:
$T_j = T_c + p [\theta_{jc}]$
P = Power dissipated
θ_{jc} = thermal resistance from the junction to the case.
θ_{ja} = thermal resistance from the junction to the ambient.

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