INTELLEC® SERIES IV INSTALLATION AND CHECKOUT MANUAL RELEASE 2.8

Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Order Number: 121757-005

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ICE	Intellec	MULTICHANNEL	SYSTEM 2000
iCS	Intellink	MULTIMODULE	UPI
iDBP	iOSP	OpenNET	

and the combination of ICE, iCS, iRMX, iSBC, iSBX, or MCS and a numerical suffix.

REV.	REVISION HISTORY	DATE
-001	Original Release per ECO #54415.	04/83
-002	iSBC-056 Memory Board Configuration Change per ECO #54735.	07/83
-003	Revised to include new power-up diagnostic tests, new Winchester diagnostics, new Chapter 2, new Appendix B, general cleanup of the manual and to support Software Release 2.5.	11/83
-004	Revised to include new Appendix C, general cleanup of the manual and to support Software Release 2.8.	06/84
-005	Added signal names to jumper tables in Figures 4-8 thru 4-12. Made minor changes throughout the manual.	08/84

PREFACE

WARNING

Risk of electrical shock may be present on exposed metal parts unless this product is adequately grounded in accordance with the following guidelines:

A. An insulated grounding conductor, at least as suitable in size, insulation material and thickness to the building AC line circuit conductors, must be installed as part of the building wiring.

B. The grounding conductor mentioned in item A is to be grounded to the earth at a suitable building earth ground such as the steel frame or water pipe of a building if they are suitably earth grounded.

C. The wall outlets in the vicinity of this product must be of the grounding type described in item A and must be connected as described in item B.

This manual is divided into five chapters and three appendices as follows:

- Chapter 1, General information, provides a physical and functional description and relevant specifications for the system.
- Chapter 2, Installation, provides information for pre-installation requirements, and installation of the standard system.
- Chapter 3, System Operation and Verification, describes and provides procedures for the power-up and confidence tests that verify system performance.
- Chapter 4, Installing Options, provides information for installing optional boards in the system to fit a variety of configurations.
- Chapter 5, Service Information, contains basic troubleshooting information and instructions on how to obtain service and repair assistance.
- Appendix A, Test Monitor Commands, describes and provides examples for use of the confidence test commands.
- Appendix B, iMDX-434 Upgrade Kit Installation, provides installation instructions for the SPU Processor Board and the SIV/4 Operating System diskette.
- Appendix C, Second-User Terminal Installation, provides installation instructions for a second-user terminal.

Additional information on the system and a list of users manuals are provided in the *Intellec Series IV Microcomputer Development System Overview*, Order Number 121752.

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CHAPTER 1
GENERAL DESCRIPTION

1.1 Introduction

This chapter provides a basic introduction to the physical and functional characteristics of the Series IV Development System (hereafter referred to as the Series IV or just the system). It contains a physical and functional description of the system and its major subassemblies, and a summary of the physical, functional and environmental specifications. It also includes information on available options, typical system configurations and power supply loading.

1.2 Physical Description

The physical system consists of two major assemblies: the mainframe and the keyboard (see Figure 1-1).

1.2.1 Mainframe

The mainframe contains a CRT subsystem, either a 5¼-inch Winchester Disk Drive and a 5¼-inch floppy disk drive or dual 5¼-inch floppy disk drives, a multiple-output power supply, an auxiliary 5 volt power supply, a 10-slot card cage and three cooling fans. These subassemblies are contained in a high-impact

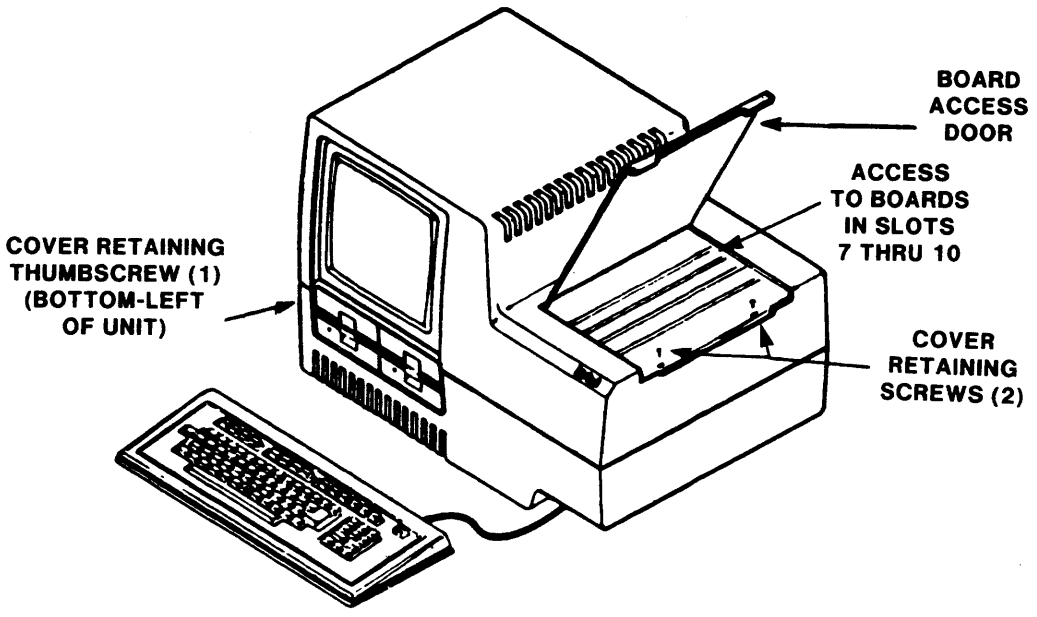


Figure 1-1. Intellec Series IV Development System

structurally strengthened plastic enclosure. A rear panel on the enclosure contains the system RESET switch, the Configuration switches, a keyboard connector, a line printer connector and two serial channel connectors. (see Figure 1-2).

1.2.2 Card Cage

The card cage includes a 10-slot motherboard that uses Multibus backplane architecture. This architecture enables more than one bus master, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. For standard configurations: card slots 1 & 2 (nearest the CRT) will contain a Central Processor I/O board (CPIO) and an ISIS Execution Unit (IEU), respectively. Optional configurations add a Slave Processor Unit (SPU) in slot 3. The first three slots are designed to accommodate 12-inch by 12-inch (30.48 by 30.48 centimeters) boards.

The remaining seven slots accommodate 6.75-inch by 12-inch (18.63 by 30.48 centimeters) boards. Slot 4 contains either an iSBC-056 (256-Kbyte) or iSBC-012 (512-Kbyte) memory board. The memory board has no bus interrupt assigned;

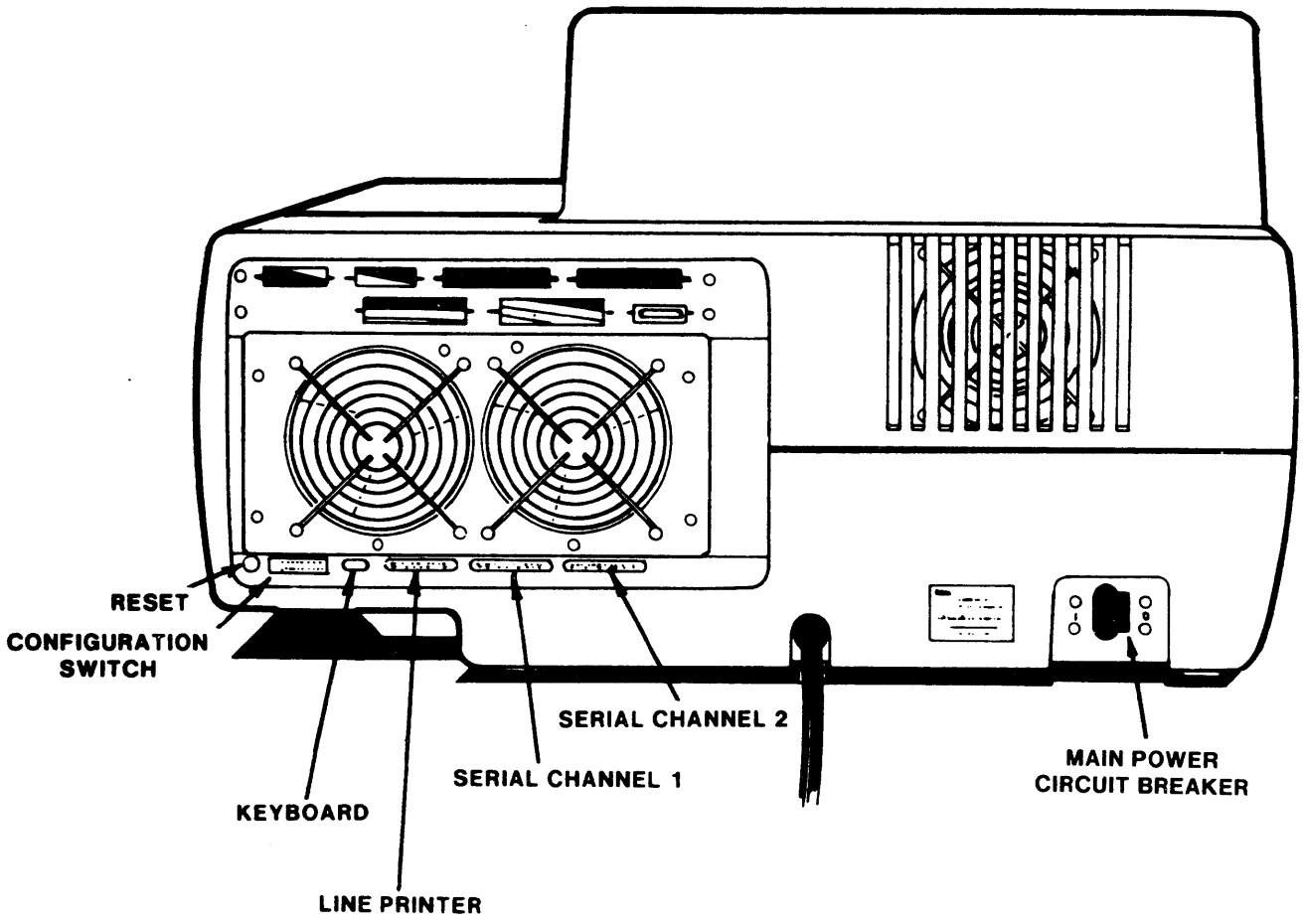


Figure 1-2. Series IV, Rear View

therefore, the bus priority of whichever slot it uses will be omitted from the listing. The remaining slots are used to accommodate options such as expansion memory boards, controller boards for peripheral disk drives, network communication boards, ISIS Cluster boards and In-Circuit Emulator (ICE) boards. Four of these slots are accessible through a hinged door over the top of the card cage; the other three can be accessed only by removing the top cover of the system.

In addition to the backplane connectors, the motherboard houses the system power distribution and I/O connectors. This includes connectors for power to the floppy and Winchester disk drives, floppy I/O, power for the CRT, input power from the multiple-output power supply, two serial I/O channels, a line printer channel and the keyboard. Also, the RESET switch is part of the motherboard.

1.3 Functional Description

The Series IV is a microcomputer development system that can be used in a standalone or network environment. This manual deals mainly with the standalone installation where the system is used as a free-standing, self-contained, data input and display computer. Various applications of the system can be enhanced and new applications added by installing options such as expansion memory and peripheral devices.

A functional block diagram of the Series IV system is shown in Figure 1-3. The function of its major modules is described in the following paragraphs.

1.3.1 Multiple-Output Power Supply

The multiple-output power supply provides the main dc power for the system. This switching type power supply receives input of 110-volts, 50/60Hz or 220-volts, 50/60Hż through a power circuit breaker switch and a line filter. For 110-volt operation, the circuit breaker is rated at 15 amperes; for 220-volt operation, 10 amperes.

The power supply provides five dc outputs as follows:

+5.1 V + or − 1% at 45.0 amperes maximum
+12.0 V + or − 5% at 1.1 amperes maximum
+12.0 V + or − 5% at 4.6 amperes maximum
−12.0 V + or − 5% at 2.0 amperes maximum
−10.0 V + or − 5% at 0.5 amperes maximum

1.3.2 Auxiliary Power Supply

The auxiliary power supply provides a voltage-controlled current source for parallel operation with the multiple-output power supply. This single-output switching power supply receives the same ac input power as the multiple-output power supply. The auxiliary power supply output is connected in parallel with the 5-volt output from the multiple-output power supply so that the output voltage level remains the same, but the output current level is increased. Output from the auxiliary power supply alone is 5.1 volts dc + 1% at 25 amperes maximum. The multiple-output and auxiliary supplies connected in parallel produce up to 70 amperes of current at 5 volts.

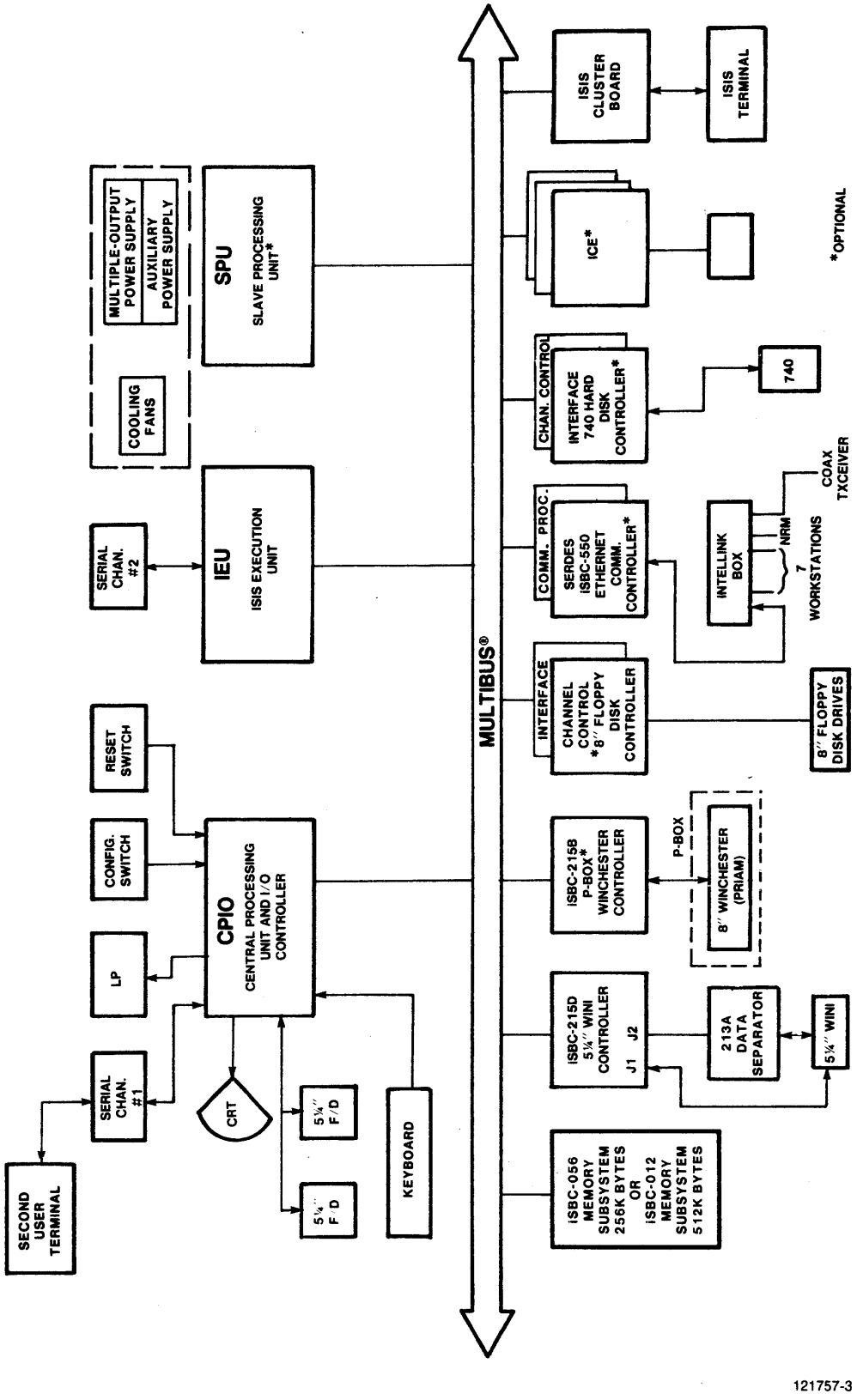


Figure 1-3. Series IV, Functional Block Diagram

1.3.3 Cooling Fans

The system employs three fans to provide cooling by circulating air over the power supplies and the card cage. When fully configured, the system can dissipate 2500 BTU per hour (725 watts) during operation. To allow for adequate cooling, the system positioning or surroundings must not prevent the natural flow of air. The card cage access door on top of the system must also remain closed when the system is turned on. One intake fan and two exhaust fans are located on the rear of the system and are connected so that they run when ac power is applied.

1.3.4 Keyboard

The keyboard provides the operator interface for entering data and control commands to the system (see Figure 1-3). This keyboard employs a standard typewriter key arrangement with additional keys for computer operation. The additional keys include an 11-key edit pad on the right, eight programmable function keys across the top that work with the CRT menu display, five additional function keys that are user defined and a BREAK key. The BREAK key allows the user to regain control of the system.

Circuits contained on the keyboard provide buffering for up to eight sequential keystrokes, and 24 additional buffers are provided by software. The CPIO board processes all keyboard input.

1.3.5 CRT Subsystem

The CRT subsystem provides a 12-inch raster scan-type monitor display with a 19.61KHz horizontal scan. The display is 80 characters wide, and is divided by software into two partitions. An upper 23 line partition provides a scrolling feature so that, when the partition is full, new data is entered on the bottom line. Previous data then moves up and the top line is lost from the display. Data cannot be scrolled backwards. The lower 2 line partition is fixed and not influenced by the scrolling partition. This fixed partition is controlled by software to provide a menu for system operation. The menu works with the eight function keys (soft keys) across the top of the keyboard. There is no visual separation between the upper and lower partitions.

Characters in either partition can be displayed, through software control, with the following attributes: overline (not underline), reverse video, blink and highlight. The cursor appears as a non-blinking reverse video rectangle, occupying the position where the next character will appear. As each new character is displayed, the cursor moves one position to the right until the 80th character is entered. The cursor does not wrap-around, but remains in the last position on top of the last character displayed. The cursor will not appear if it is in the same location as an attribute character.

Pressing the keyboard RETURN key causes the cursor to move to the first character position at the left of the display and also to move downward to the next line. Pressing the keyboard LINE FEED key also moves the cursor down one line, but the cursor remains in the same horizontal position. If the cursor is on the last line of the scrolling partition, pressing the RETURN or LINE FEED keys causes all characters in the partition to move up one line; the top line is then lost and the bottom line is blank.

A normal display is light characters on a dark background, and reverse video is dark characters on a light background. There is no background separation between character lines.

1.3.6 Floppy Disk Drive

The system contains either two 5¼-inch floppy disk drives or one 5¼-inch Winchester drive and one 5¼-inch floppy disk drive. The double-sided, double-density floppy diskettes with 80 tracks per side, provide 638K bytes of formatted storage. The soft sectored floppy drive records in Modified Frequency Modulation (MFM) with FM recording used on track 0 side 0.

Diskettes are inserted and removed through the front of the disk drives. A latch on the front of the disk drives is lifted (opened) to insert or remove diskettes. When a diskette is inserted, the latch is pressed down (closed) to lock the diskette on the spindle and position (load) the read and write heads. Do not apply or remove power to or from the system when diskettes are in the drives. Drive 0 is normally the drive on the right-hand side and drive 1 is normally on the left-hand side. The 5¼-inch (mini-floppy) diskettes are normally write enabled so that data can be transferred to the diskette. To prevent writing over existing files, a tab must be installed over the write enable slot on the side of the diskette. Always insert diskettes with the label facing upward, the write enable slot to the left, and the read/write slot to the back of the drive (see Figure 3-3).

1.3.7 5¼-Inch Winchester Disk Drive

On iMDX-431 Systems, a 5¼-inch Winchester disk drive replaces the left hand floppy disk drive. This drive has 10 Megabytes of formatted storage and records via MFM. It has 2 double-sided, metal oxide coated platters which spin at 3600 RPM. Four heads access the platters and transfer data at 5 Mbits/sec. The Winchester does not need to be unlocked for regular operation. The heads are protected automatically at "Power-on and Power-off".

1.3.8 Central Processor and I/O

The Central Processor and I/O (CPIO) board interfaces the following I/O devices:

a. Keyboard

b. CRT Monitor

c. Floppy Disk Drive(s)

d. Line Printer (Centronix parallel type)

e. Serial Channel 1 (RS232 and CCITT Rec V24)

f. Second-user Terminal via Serial Channel 1

This single board computer also provides a 5MHZ co-processor cluster that contains an 8088 microprocessor, an 8089 I/O processor, 64 Kbytes of two-ported RAM, 32 Kbytes of PROM/ROM, an interrupt subsystem with three 8259A programmable interrupt controllers, a general purpose timer with an 8253 programmable interval timer and an 8251A USART for Serial Channel 1. Since the CPIO is a bus master (able to control access to the Multibus backplane) in a system that can use more than one bus master, an on-board 8289A bus arbiter

resolves bus access conflict. The CPIO also supports the functions performed by the IEU board.

1.3.9 ISIS Execution Unit

The ISIS Execution Unit (IEU) board, a standard feature in system configurations, supports ISIS operating system application environments. This allows the system to provide a compatible code execution environment for previous users of the ISIS operating system. The IEU board also supports a serial I/O channel (Channel 2) that is compatible with the RS232 specification and CCITT Recommendation V24.

The CPU for the IEU board, a 5 MHz 8085A microprocessor, is supported by 64 Kbytes of two-ported RAM, an interrupt subsystem with two 8259A programmable interrupt controllers, a general purpose timer with an 8253 programmable interval timer and an 8251A USART for Serial Channel 2. To support its operational environment, the IEU board depends upon the assistance from the CPIO board.

1.3.10 SPU Unit (Optional)

The Slave Processor Unit (SPU), a single board computer that can be added to the system, provides greater computing power. The board provides an 8086 microprocessor, operating at 8MHz. The processor is supported with 128 Kbytes of two-ported RAM, up to 64 Kbytes of PROM/ROM, an interrupt system with two 8259A programmable interrupt controllers, and a general purpose timer with an 8253 programmable interrupt timer. Since the SPU can also function as a bus master, an on-board 8289 bus arbiter resolves bus conflicts with other bus masters.

The SPU also contains an 8206 Error Detection and Correction Unit (ECC) that works with the on-board RAM. This ECC provides greater memory system reliability by detecting and correcting all single-bit errors and detecting all double-bit and most multiple-bit errors.

1.3.11 iSBC-056/012B Memory Boards

System memory is provided by either the iSBC-056 (256 Kbytes) RAM memory board, the iSBC-012B (512 Kbytes) RAM memory board or combinations thereof. Both boards measure 7 inches by 12 inches (17.8 x 30.5 centimeters). Refer to Figure 1-6 for the system memory upgrade configurations supported. (If ISIS Cluster boards are installed in the system, refer to the *Series IV iMDX 580/582 ISIS Cluster Installation, Operation, and Service Manual,* Order no. 134650, for supported memory configurations.) Jumper information needed to operate each board type in a supported system configuration is furnished in Chapter 4 along with its respective board drawing. The board dash number specified in Figure 1-6 for a given configuration must be noted to relate to the proper jumper information given in Chapter 4. Also, whenever the memory configuration is changed, bear in mind that the IEU board jumpers must be reconfigured so that its memory occupies the top-most page of memory. In addition, as a troubleshooting aid, a parity LED is provided on each board.

1.3.12 ISIS Cluster Board (Optional)

The ISIS Cluster board is a single board computer that functions as an ISIS workstation when interfaced to a user-supplied terminal. The Cluster board uses a Series IV network workstation (equipped with software release 2.8 or higher) as a host system (Cluster workstations can only operate on a network). Each ISIS Cluster board contains an 8085A CPU, 64K of dual-port RAM, 4K of EPROM, and I/O circuitry. When installed in a Series IV, it operates independently using the iSBC-550 Communication board set to communicate with the network. It cannot access any of the Series IV peripherals. For further information on the operation and installation of ISIS Cluster boards, refer to the *Series IV iMDX 580/582 ISIS Cluster Installation, Operation, and Service Manual,* Order no. 134650.

1.4 System Configuration

The system configuration depends upon the boards contained in the card cage, the combination of 5¼-inch disk drives and whether the system is used as a standalone unit or as a communication network workstation. The standard configuration for a standalone system provides a CPIO board, an iSBC-056 or iSBC-012B RAM memory board and an IEU board. By adding boards, the system can accommodate a variety of applications. Computing power for the standard system is increased by adding an SPU board. In addition to the three 12-inch by 12-inch boards, the remaining seven slots in the card cage can contain expansion memory boards, network communications boards, ISIS Cluster boards, disk drive controller boards and In-Circuit Emulator (ICE) boards (when the Series IV is being used in single-user mode; ISIS Cluster, Multi-user and Toggle modes do not support the use of ICE). Table 1-1 lists typical system configurations and indicates required and optional boards that make up a particular system configuration.

In a Series IV equipped with software release 2.8 or higher, memory can be partitioned to support two users interactively in both standalone operation or network mode. User 1 operates in memory Partition 1 and accesses the system from the system keyboard. User 2 operates in memory Partition 2 and accesses the system via a user-supplied terminal that is connected to Serial Channel 1. After installing the terminal, the Series IV must be initialized to support the Multi-user mode of operation by executing either SYSGEN (workstation options 6–11) or the STTY and REGION CUSPs (refer to the *Series IV Operating and Programming Guide,* Order no. 121753, if the Series IV is operating in standalone mode or the *NDS-II Network Resource Manager User's Guide,* Order no. 134300, if the system is being used as a network workstation).

Some configurations of options may not be possible due to excessive current drain on the system power supplies. Refer to Tables 1-3 and 1-4 at rear of this chapter to verify that the power usage of the selected system configuration does not exceed the current capability of the power supply.

Table 1-1. Series IV, Typical Systems Configurations

System	Description
iMDX430	• CPIO Processor • IEU (ISIS Execution Unit) • iSBC-056 (256KB) or iSBC-012 RAM Board (512KB) • two 5¼″ Floppy Disk Drives
iMDX431	• CPIO Processor • IEU (ISIS Execution Unit) • iSBC-056 (256KB) or iSBC-012 RAM Board (512KB) • iSBC-215D 5¼″ Winchester Controller • 5¼″ Winchester Drive and 213A Data Separator (under Winchester drive) • 5¼″ Floppy Disk Drive
Options	**Description**
Extended Processing	iMDX 434 Upgrade kit (SPU Processor)
Workstation	iMDX 456 Upgrade Kit (Ethernet Communications to the NDS-II Network)
Peripheral Chassis	35 MB Winchester Drive and iSBC-215B Controller
Hard Disk	Model 740/743 and iSBC-206 Controller
8″ Floppy Disk Drive	Such as Intel 720 (User Supplied) for ICOPY only
ICE	In Circuit Emulator board and board sets may be added by the user (the use of ICE in combination with ISIS Cluster, Multi-user, or Toggle modes is not supported)
ISIS Cluster Workstation	iMDX 580 and 582 Upgrade Kits (User must provide a terminal; iMDX 456 must be installed)
Second-user Terminal	User must supply the terminal; cable provided with the system

1.5 System Bus Architecture

The system bus architecture is designed such that the SPU, IEU and the CPIO all have their unique local memory and yet all can access the Multibus interface. The CPIO and the SPU can also access any Multibus memory. However, the IEU, because of the limited 16-bit addressing, cannot address any other memory outside it's own local 64 Kbytes. It can, however, address system I/O.

System memory is dual-port access, in that it is local memory to the resident CPU(s) and system memory to the CPU's on other boards. The address lines are multiplexed between local and Multibus interface access.

1.6 System Memory Allocation

The Series IV software (operating system) is designed to operate within a one megabyte boundary. There is therefore a limit to the amount of functional RAM that can be added to the system. Before adding additional RAM, calculate the existing system memory and then install optional memory up to but not to exceed 872 Kbytes of total system memory.

As noted earlier, the basic Series IV system may be equipped with either an iSBC-056 (256 Kbytes) or iSBC-012B (512 Kbytes) RAM memory board. Figure 1-4 shows the basic system memory allocations when using the iSBC-056 board. Figure 1-5 shows the basic system memory allocations when using the iSBC-012B board. Bear in mind, that with either memory board installed, the IEU board memory must always occupy the top-most page of memory.

When the iSBC-056 board is used, optional memory may be added to the Series IV, above page 6 (6000:FFFF) on the standard system and above page 9 (9000:FFFF), with the iMDX-434 option installed (refer to Figure 1-4). When the iSBC-012B board is used, optional memory may be added above page A (A000:FFFF) on the standard system and above page D (D000:FFFF), with the iMDX-434 option (refer to Figure 1-5).

NOTE

To run I²ICE in the Series IV system, 512 Kbytes of contiguous user memory is required.

Additional memory boards (e.g.; iSBC-028/iSBC-064/iSBC-056/iSBC-012B) may be installed in any system provided that the IEU is not pushed above page E (E000:FFFF) and the power supply current capability is not exceeded. Refer to Figure 1-6 for some of the optional memory configurations that may be employed.

If ISIS Cluster boards are to be installed into a system that is equipped with an iSBC-012B RAM board, it may be necessary that the memory strapping on the iSBC-012B and IEU boards be changed. For more information, refer to the *Series IV iMDX 580/582 ISIS Cluster Installation, Operation, and Service Manual,* Order no. 134650.

The system memory is referenced by multiple processors on the CPIO board (8088) and the optional SPU board (8086). The 8088 and 8086 microprocessors can both address one megabyte (20-bit addressing). All three processors address the majority of memory at common addresses. Since the 8085 does not have segment registers, any address it passes as data to and from the CPIO board will have an implied segment address the same as the 8088. For compatability with existing 8085 resident applications that communicate with the Multibus backplane, IEU memory is aliased at address 0K thru 63K (page 0). This is apparent only to the 8085 processor.

Actually, a small portion of common memory is reserved and cannot be shared. The lowest 1 Kbyte of the CPIO, SPU and IEU memory is reserved for interrupt vectors and the top 32 Kbytes (992 to 1024K) of the CPIO and the top 16 Kbytes of the SPU on-board memory is the PROM (ROM) memory for each board. Expansion memory must be contiguous to both the CPIO and SPU processors.

1.7 Specifications

Table 1-2 lists the relevant specifications for the system. Additional power supply information is provided in Table 1-3 (for standard system) and Table 1-4 (optional board current demands).

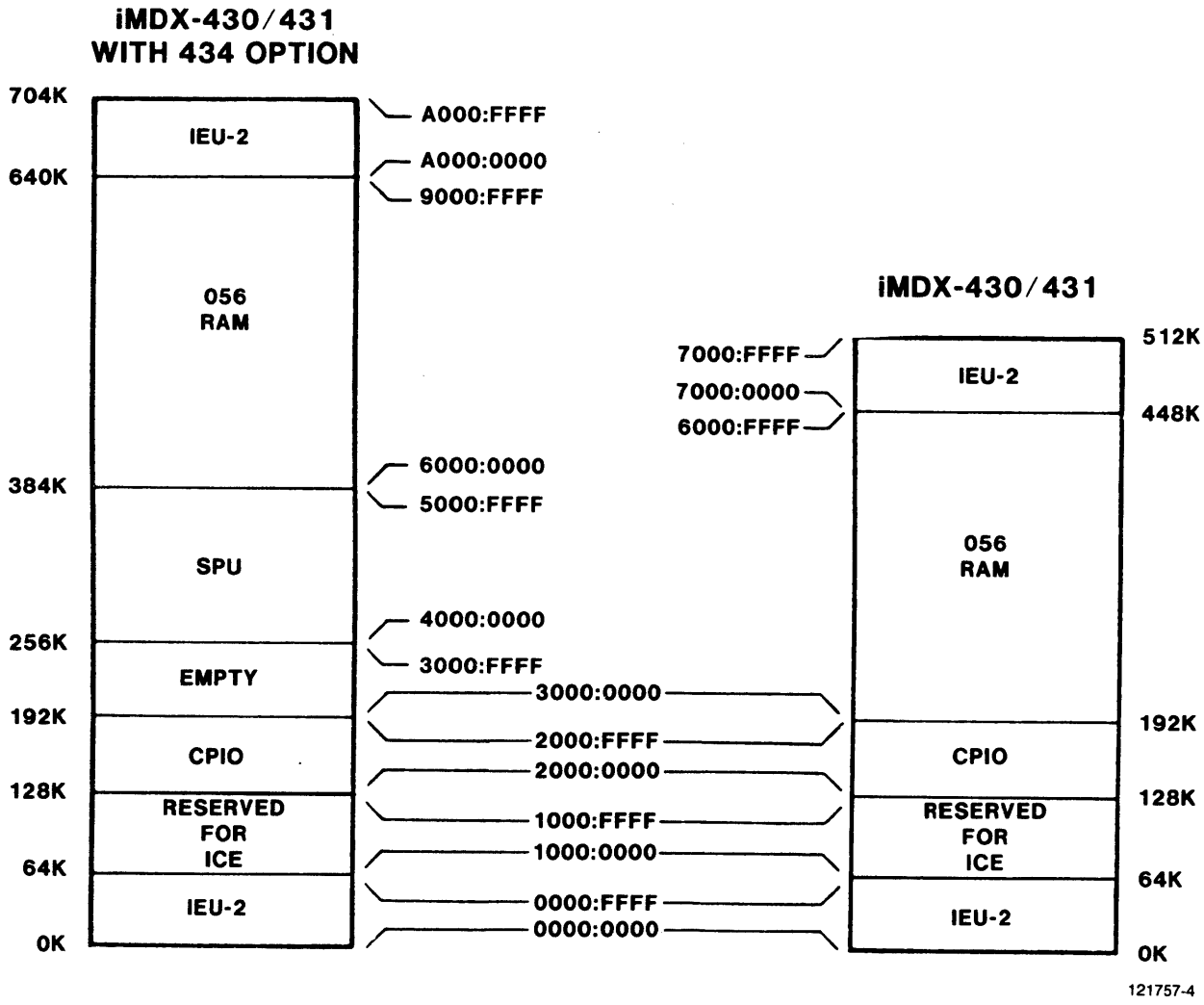


Figure 1-4. Series IV, System Memory Allocation Using iSBC-056 RAM Memory Board

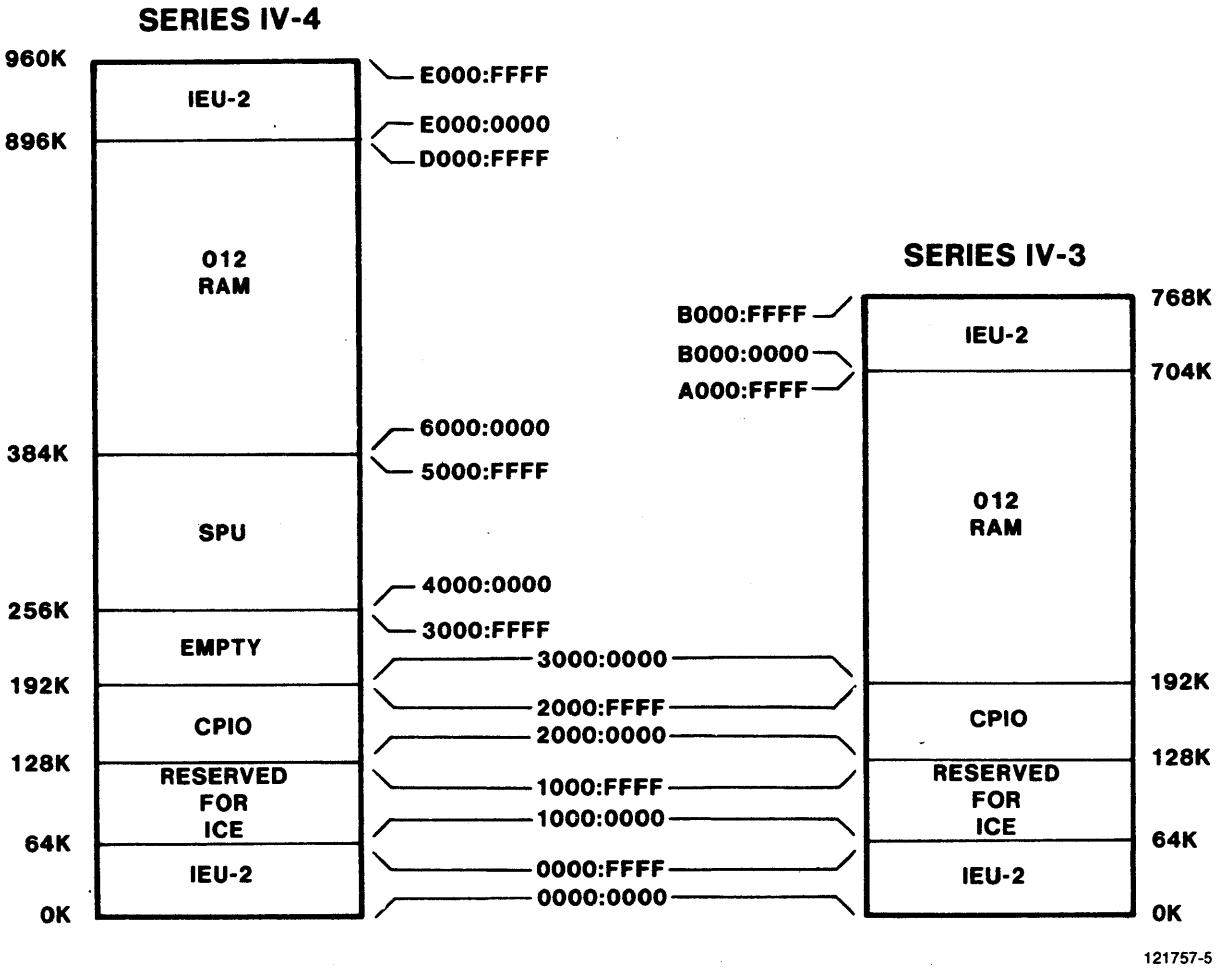
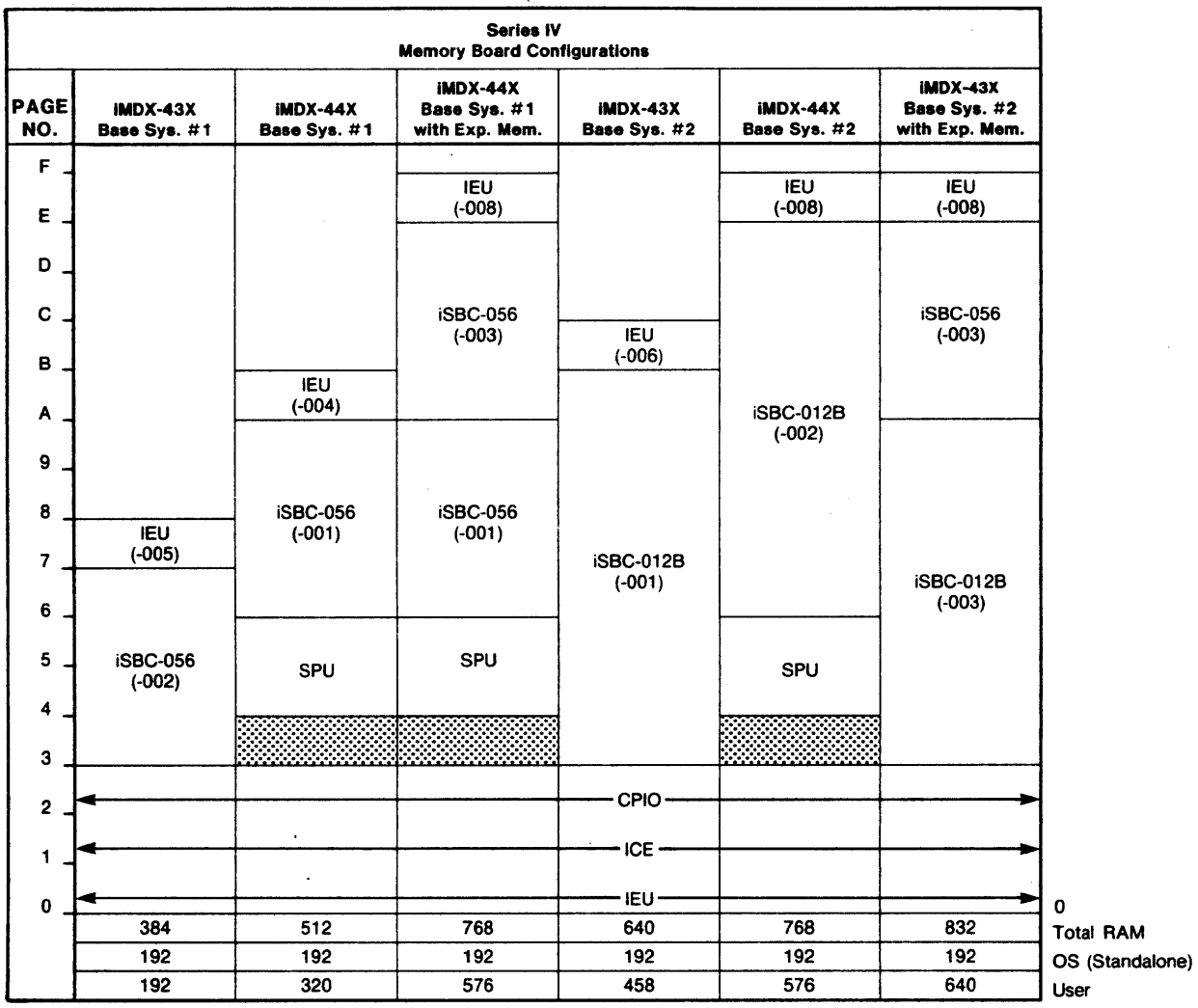


Figure 1-5. Series IV, System Memory Allocation Using iSBC-012B RAM Memory Board



NOTES:

1. **ALL TOTAL RAM, OS AND USER MEMORY FIGURES ARE KBYTES.**
2. **I^2 ICE REQUIRES 512 KBYTES OF USER MEMORY.**
3. **REFER TO RESPECTIVE BOARD DIAGRAM IN CHAPTER 4 OF THIS MANUAL FOR JUMPER DATA.**

121757-6

Figure 1-6. Series IV, System Memory Upgrade Configurations

Table 1-2. Series IV, Development System Specifications

Physical Characteristics	
Mainframe:	Width: 26.5 in. (67.31cm) Height: 16.5 in. (41.91cm) Depth: 18.5 in. (46.99cm) Weight: 66 lbs. (29.24kg)
Keyboard:	Width: 20.0 in. (50.8cm) Height: 3.0 in. (7.62cm) Depth: 8.0 in. (20.32cm) Weight: 7.0 lbs. (3.17kg)
AC Input Power Requirements	
Standard:	8.5A @ 85/170 Vac, 47-64 Hz
Optional:	4.25A @ 170/264 Vac, 47-64 Hz
Environmental Characteristics	
Operating Temperature:	
Models A & B (Amer. & Eur.)	50° to 94° F (10° to 35° C)
Model C (Japan)	50° to 104° F (10° to 40°C)
Relative Humidity:	5% to 90% without condensation
Power Supply Characteristics	
Available Outputs:	+5.1 ±1% (2), +12 ±5% (2), −12 ±5%, −10 ±5%.
Current Capacity:	Refer to Table 1-3.
Integral Floppy Disk Drive Characteristics	
Number of Drives:	One or Two
Drive Type:	5¼-inch, double-sided, double-density
Tracks per side:	80
Sector Size:	512 bytes
Storage Capacity:	638 Kbytes formatted
Media Type:	Dysan 204/2D or equivalent (certified).
Rotational Speed:	300 rpm ± 1.5%
Recording Mode:	MFM (Modified Frequency Modulation) FM (Track 0, Side 0)
Data Transfer Rate:	250K bits per second
Access Time:	10 ms maximum
Head Settling Time:	15.0 ms maximum
Power-up Delay:	0.5 seconds maximum
Integral Winchester Disk Drive Characteristics	
Rotational Speed:	3600 rpm ± 0.1%
Storage Capacity:	12.76 Megabytes unformatted; (10 Megabytes formatted)
Cylinders:	306
Tracks:	1224
Sector Size:	512 bytes
Power-up Time:	30 sec.
Head Settling Time:	15 ms.
Track Access:	3 ms.
Data Transfer Rate:	5 Mbits/sec.

Table 1-2. Series IV, Development System Specifications (Cont'd)

Integral Winchester Disk Drive Characteristics (Cont'd)	
R/W Heads:	4
Disks:	2
Encoding Method:	MFM
Display Characteristics	
CRT Screen Size:	12 inches (30.48 cm) measured diagonally
Display Color:	Green (P42 phosphor)
Display Size:	6″ x 8.25″ both ±.125 @ 12VDC 15.24cm x 20.95cm both ±.3cm @ 12 VDC
Character Size:	6 x 9 pixels (8 x 12 template)
Characters per Line:	80
Number of Lines:	25
Display Partitions (software):	Two: Top 23 lines scrolling; bottom two lines non-scrolling.
Display Modes:	Normal video, intensified video overline (not underline), reverse video and blink
Horizontal Scan Frequency:	19.61KHz
Vertical Scan Frequency:	60Hz 110Vac; 50Hz 220Vac
Horizontal Blanking/Retrace Time:	11 microsec.
Vertical Blanking/Retrace Time:	1.22ms (60Hz) or 2.45ms (50Hz)
Keyboard Characteristics	
Buffer Size:	Eight Characters
Mode:	Asynchronous
Baud Rate:	300
Scan:	Each key sensed every 12.5 ms max.
Data Transfer:	Bit serial; 10-bit frame; 1 start bit, 1 stop bit, and 8 data bits
Card Cage Characteristics	
Number of Slots:	10
Card Size:	Three 12″ x 12″ (30.48cm x 30.48cm) and seven 6.75″ x 12″ (18.63 x 30.48cm)
Architecture:	Multibus backplane (IEEE Standard P796 compatible)
Bus Priority Slots:	Priority 0 thru 9 fixed, non-rotating (see Figure 4-1)
CPIO Board Characteristics	
Board Size:	12″ x 12″ (30.48 x 30.48cm)
Processor:	8088 and 8089 co-processor cluster operating at 5MHz
RAM:	64KB two-ported
PROM/ROM:	32KB
Bus Clock Rate:	9.8304MHz
Interrupt Levels:	System, local master and local slave
Serial Channel 1:	Dedicated to :TI: and :TO: at default of 300 Baud; (User selectable via STTY command)
Line Printer Channel:	Centronics parallel interface

Table 1-2. Series IV, Development System Specifications (Cont'd)

SPU Board Characteristics	
Board Size:	12″ x 12″ (30.48 x 30.48cm)
Processor:	8086 operating at 8MHz
RAM:	128KB two-ported with Error Correction Unit (ECC)
PROM/ROM:	Up to 64KB (only 8KB used)
Interrupt Levels:	15
IEU Board Characteristics	
Board Size:	12″ x 12″ (30.48 by 30.48cm)
Processor:	8085A
RAM:	64KB two-ported
ROM:	None
Interrupt Types:	Two: system and local
Serial Channel 2:	8253-8251A Programmable Interface
Baud Rate:	64K with Ext. Clock (synchronous)
Type:	RS232 and CCITT Rec. V24 compatible

Table 1-3. Series IV, Standard System Power Supply Loading

	Power Supply Outputs				
Assembly	**+5.1V**	**+12V**	**+12V**	**−10V**	**−12V**
Power Supply Capacity (Maximum Amps)					
Multiple-Output Power Supply	45A	5.00A	3.00A	0.50A	2.00A
Auxiliary Power Supply	25A	—	—	—	—
Total Available Current	70A	5.00A	3.00A	0.50A	2.00A
Maximum Current Demand iMDX430 (Amps)					
CRT Display	—	—	1.50A	—	—
Keyboard	0.50A	—	—	—	—
Floppy Disk Drives (2)	1.40A	1.10A	—	—	—
CPIO Board	12.06A	—	0.25A	—	0.10A
IEU Board	6.82A	—	0.50A	—	0.50A
*iSBC-056 256K RAM Board	4.80A	—	0.015A	—	—
Total Current Drain	25.58A	1.10A	2.265A	—	0.60A
Available for Options	44.42A	#	0.735A	0.5A	1.40A
Maximum Current Demand iMDX431 (Amps)					
CRT Display	—	—	1.50A	—	—
Keyboard	0.50A	—	—	—	—
5¼″ Winchester, 213A Board and Floppy Drive	3.50A	2.80A	—	—	—
iSBC-215D	—	—	—	—	—
CPIO Board	12.06A	—	0.25A	—	0.10A

Table 1-3. Series IV, Standard System Power Supply Loading (Cont'd)

Assembly	Power Supply Outputs				
	+5.1V	+12V	+12V	−10V	−12V
Maximum Current Demand iMDX431 (Amps) (Cont'd)					
IEU Board	6.82A	—	0.50A	—	0.50A
*iSBC-056 256K RAM Board	4.80A	—	0.015A	—	—
Total Current Drain	27.68A	2.80A	2.265A	0.0A	0.60A
Available for Options	42.32A	#	0.75A	0.5A	1.40A

NOTES:

Not Available
* Or iSBC-012B Board

For optional device current demand refer to Table 1-4.

Table 1-4. Series IV, Optional Device Maximum Current Demand

Assembly	Power Supply			
	+5.1V	+12V	−10V	−12V
SPU Board	13.2A	0.025A	—	0.023A
iSBC-550 Communication Board Set	9.55A	0.50A	—	—
iSBC-215B Winchester Disk Controller	5.05A	—	—	—
206 Hard Disk Controller	8.14A	—	—	—
ICE 41A Emulator Board Set	8.91A	0.07A	—	—
ICE 49 Emulator Board Set	10.72A	0.07A	—	—
ICE 51 Emulator Board Set	15.47A	0.07A	—	—
ICE 85 Emulator Board Set	19.30A	0.07A	—	—
ICE 86 Emulator Board Set	21.43A	0.07A	—	—
ICE 88 Emulator Board Set	19.62A	0.07A	—	—
Multi-ICE (85+85) Emulator Board Sets	38.60A	0.14A	—	—
I²ICE Emulator System, Host Interface Board (III520)	5.00A	—	—	—
ISIS Cluster Board	4.50A	0.025A	0.023A	—

CHAPTER 2
INSTALLATION

2.1 Introduction

This chapter provides pre-installation requirements and the installation procedure used to prepare the system for operation.

2.2 Site Preparation

The physical characteristics (width, height, depth and weight) of the system are given in Table 1-2. Before the system is uncrated, determine its operating location. Ensure that the work area selected (bench, table, desk or other structure) accommodates and supports the system mainframe and keyboard. The system requires a height clearance of at least 25.5 inches (65 centimeters). Also, ensure that the wall outlet to be used to power the system is an approved grounding type having a separate grounding conductor connected to the building earth ground.

CAUTION

The Series IV unit comes equipped with a 3-prong plug for connection to the ac power source (wall outlet). The round prong of this type plug is used to ensure personnel safety by providing the unit with a common ground connection to any other equipment plugged into the ac power source and thus must never be defeated. Never alter this plug or use adapters which will defeat its purpose.

Allow a minimum clearance of 6 inches (15.25 centimeters) around the system to provide air flow for system cooling. Failure to provide adequate air flow may cause overheating and damage to sensitive electronic parts.

2.3 Installation Procedure

Refer to Figure 2-1 for a guide through the installation procedure. Assure proper installation and checkout of the Series IV system by:

1. Preparing the system operating location as defined in Paragraph 2.2.
2. Inspecting all packages for damage, unpacking the system and taking inventory (see Paragraphs 2.4, 2.5 and 2.6).
3. Setting up the system (see Paragraph 2.7).
4. Powering up the system (see Paragraph 2.8).
5. Bootloading the Supplemental Diagnostic Monitor and running the SIVDIA and SIVEXT Supplemental Tests (see Paragraphs 2.9, 2.10 and 2.11).
6. Verifying operation of the 5¼" Winchester Subsystem, if installed, by running SIVWIN Supplemental Tests (see Paragraph 2.12).

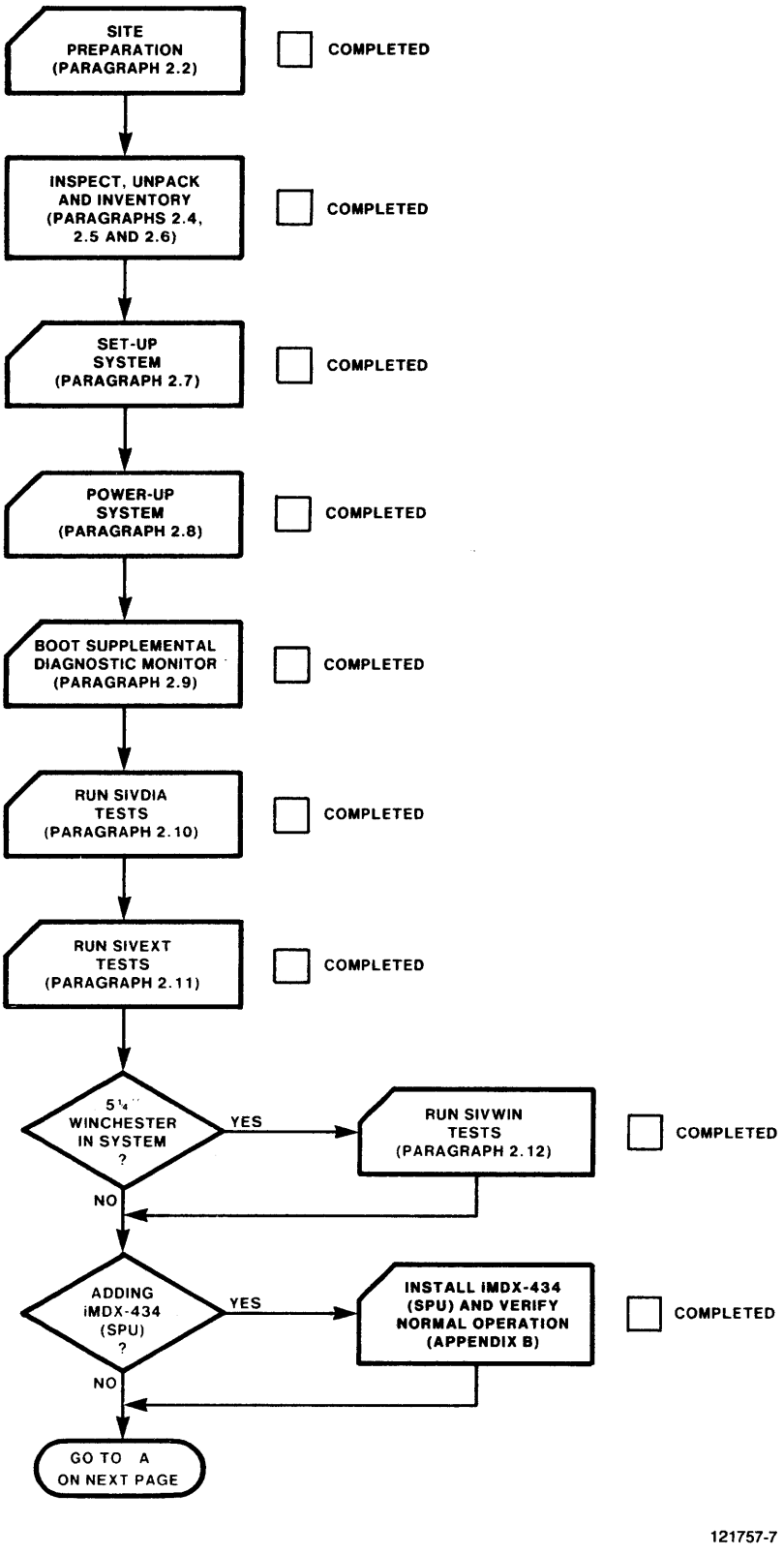


Figure 2-1. Series IV, Installation Procedure Flowchart

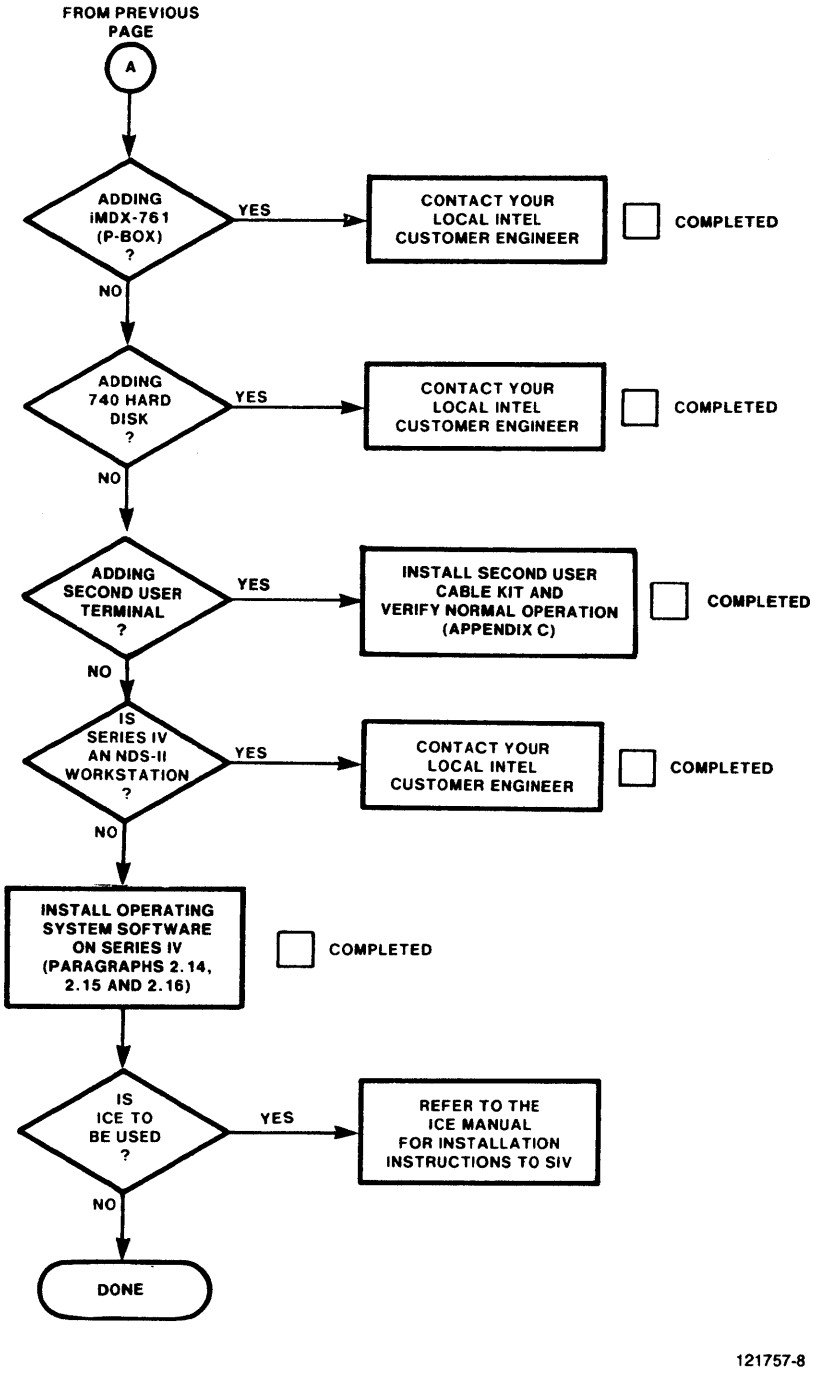


Figure 2-1. Series IV, Installation Procedure Flowchart (Cont'd)

7. Installing options and verifying their operation (see Paragraph 2.13).
8. Installing the system software (see Paragraph 2.14 through 2.16).

2.4 Incoming Inspection

Inspect the exterior of the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is damaged or water stained, request that the carrier's agent be present when the equipment is unpacked. If the carrier's agent is not present, and the equipment is damaged, keep the carton and packing material for the agents inspection.

For repairs to equipment damaged in shipment, contact Intel Technical Service Center to obtain a Return Authorization Number and further instructions. (Refer to Paragraphs 5.4 and 5.5). A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

2.5 Unpacking Procedure

NOTE

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be reshipped.

Figures 2-2 and 2-3 show the system packed in one of two approved methods (Procedure "A" or "B"). Identify the packing illustration that reflects the method used to pack your system and then, referring to that illustration, proceed as follows:

WARNING

The packed system weighs approximately 89 pounds (40.37 kilograms). To prevent injury, always use two people to lift or move the system.

1. Remove the accessory kit envelope and set it aside for use when installing options.
2. Lift the keyboard and packing material from the top of the system. Separate the keyboard from the packing material and place the keyboard aside until the mainframe is in place.
3. Use two people to lift the system mainframe onto the work area.

2.6 System Inventory

Verify that all items listed below have been received.

1. iMDX-2006 Literature Kit.
2. iMDX-2002 Kit having the following diskettes:
   - SIV/3 iNDX.S31 Operating System
   - SIV/4 iNDX.S41 Operating System

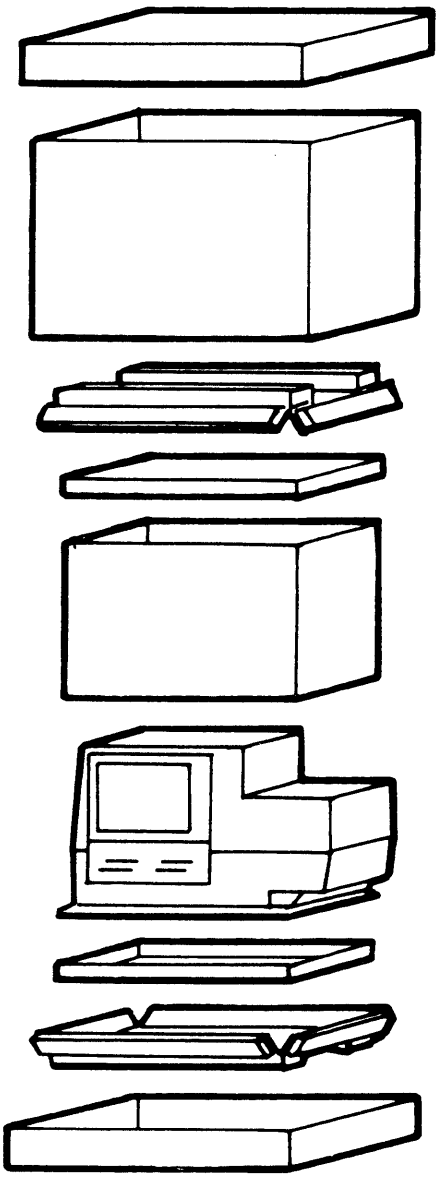


Figure 2-2. Series IV, Unpacking Procedure "A"

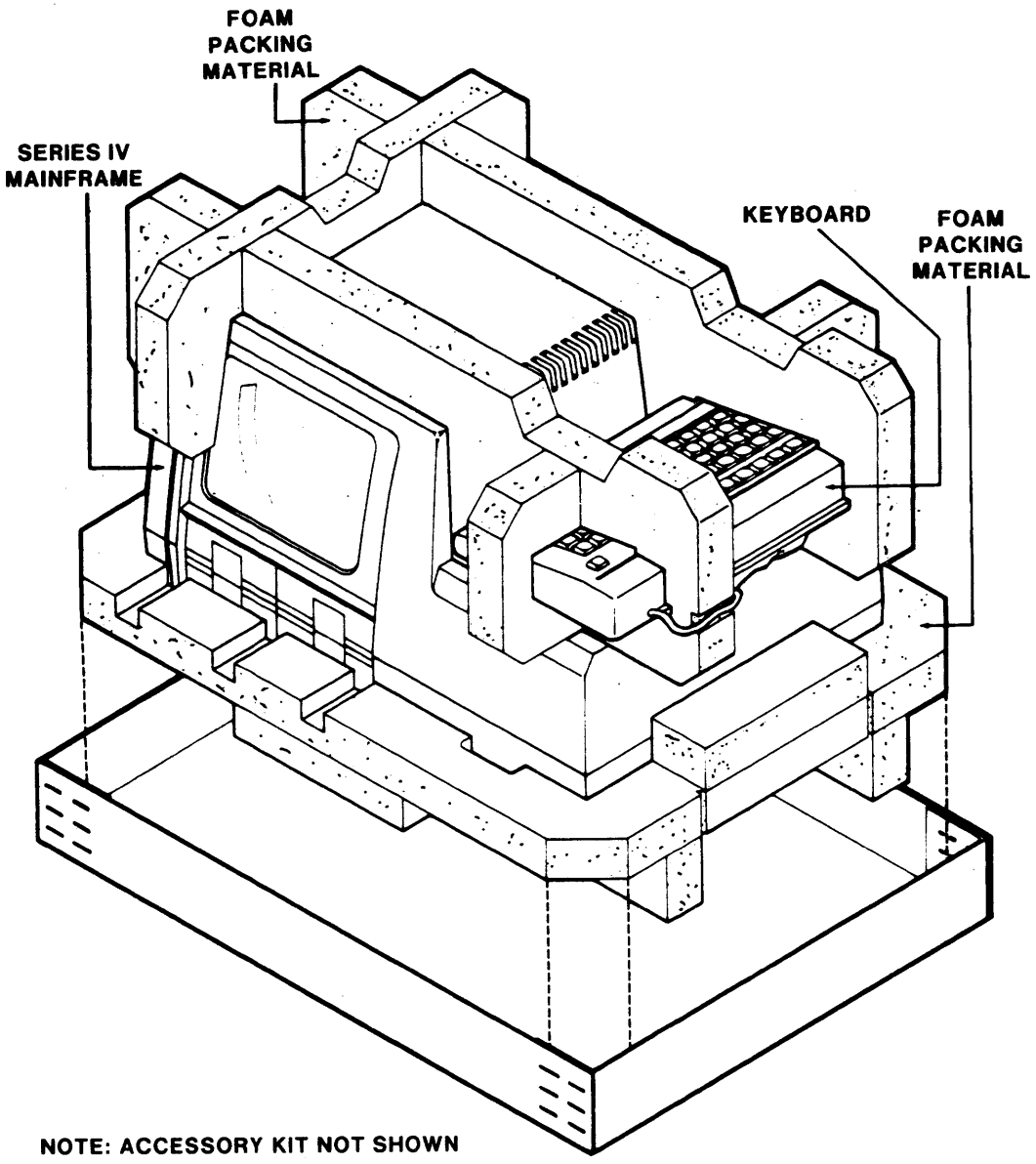


Figure 2-3. Series IV, Unpacking Procedure "B"

- SIV iNDX.CUSPS
- ISIS-IV System Software
- SIV 16-bit Standard Software
- SIV Supplemental Diagnostics
- Series IV ICE Support 1 of 2
- Series IV ICE Support 2 of 2
- Scratch Diskette
- FPORT (8-inch Diskette, Double Density)
- FPORT (8-inch Diskette, Single Density)
- iPPS PROM Programming Software

3. Accessory Kit (P/N 124480) which includes:
   - Dual Auxiliary Connector Kit (P/N 4000607)
   - Triple Auxiliary Connector Kit (P/N 124506)
   - Cable Assembly (P/N 108197)
   - Cable Connector Adapter Plate (P/N 133560)
   - Miscellaneous Hardware

2.7 System Set-Up

WARNING

The unpacked system weighs approximately 70 pounds (31.75 kilograms). To prevent injury, always use two people to lift or move the system.

Set-up the system as follows:

1. Connect the plug on the keyboard cable to the mainframe keyboard connector (see Figure 3-1). Fasten the connector to the mainframe with its two captive, slothead screws.
2. Arrange the system in its working position. Usually the keyboard sits in front of the disk drives.
3. Open the Floppy Disk Drive latch(es) and remove the shipping cardboard from the drive(s).
4. After assuring that the system power circuit breaker is in the 0 (OFF) position, connect the power cord plug to a three-conductor power outlet.

2.8 Power-Up Procedure

Power-up the system as follows:

1. Locate the Configuration Switches at the right rear of the system (see Figure 3-1) and then set the switches as shown below to select Floppy Drive #0 as the boot device.

```
ON                          X      SW 2-6 and 8 = down
 ↑      X  X  X  X  X          X   SW 7 = up
     1  2  3  4  5  6   7   8      SW 1 = up when 60 Hz ac
                                          power, down when
                                          50 Hz
```

2. Power-up the system by setting the circuit breaker (left rear of system) to the on (1) position.

3. Observe that the fans are running and, after several seconds, the following message is displayed on the CRT screen:

```
SERIES IV SYSTEM POWER-UP DIAGNOSTIC, Vx.y
CPIO PHASE I ........................................ / PASSED
CPIO PHASE II ....................................... / PASSED
FLOPPY DRIVE NOT READY
SPU ............................................. NOT INSTALLED
iSBC-550 ........................................ NOT INSTALLED
IEU ............................................. / INSTALLED

SIV Boot Vx.y
Mini-floppy dr.0
-device failure
Error 3800

Attempt to reboot from : Mon88
SERIES IV CPIO MONITOR Vx.y
.
```

(where *x.y* is the release level)

NOTE

The "FLOPPY DRIVE NOT READY" and "Error 3800" messages are normal messages when Floppy Drive #0 latch is open.

2.9 Bootload Supplemental Diagnostic Monitor

Bootload the Supplemental Diagnostic Monitor into the system by performing the following:

1. Ensure that the SIV Supplemental Diagnostic diskette is write protected by a tab covering the Write-Enable slot (see Figure 3-3).

2. Insert the SIV Supplemental Diagnostic diskette into Floppy Drive #0 (drive on right) and close the drive latch.

3. Momentarily depress the RESET switch (located at right rear of system). See Figure 3-1 for location. After approximately 40 seconds, the following message will be displayed on the CRT screen.

```
SERIES IV SYSTEM POWER-UP DIAGNOSTIC, Vx.y
CPIO PHASE I ........................................ / PASSED
CPIO PHASE II ....................................... / PASSED
SPU ............................................. NOT INSTALLED
iSBC-550 ........................................ NOT INSTALLED
IEU ............................................. / INSTALLED
```

```
SIV Boot Vx.y
Mini-floppy dr.0
```

The front panel LED of Floppy Drive #0 goes on for a few seconds and then the following message is displayed on the CRT screen.

```
SERIES IV Diagnostic Monitor, Vx.y
>
```

NOTE

If the sign-on message is not displayed, repeat step 3 twice more. If the system still does not sign on, refer to service information in Chapter 5.

2.10 Load and Run SIVDIA

The SIVDIA test suite is executed by performing the following:

1. Ensure that the Supplemental Diagnostic diskette is in Floppy Drive #0 and the Series IV Diagnostic Monitor has been loaded (Paragraph 2.9). Then load the SIVDIA test suite and the Test Monitor (TMON) by typing:

   ```
   ZSIVDIA<cr>
   ```

2. The LED on Floppy Drive #0 lights for approximately 30–40 seconds, and then the following message is displayed:

   ```
   File SIVDIA loaded

   SERIES IV CPIO, SPU DIAGNOSTIC TEST Vx.y
   *
   ```

   NOTE

   The SIVDIA test suite is now loaded into the system and will be used to test the CPIO and board and Floppy Drive #0.

3. To run the pre-selected SIVDIA tests, type:

   ```
   T<cr>
   ```

4. After approximately 30 to 40 seconds, the following message should be displayed:

```
0004H ***IGNORED ***
0005H ***IGNORED ***
0006H ***IGNORED ***
0007H ***IGNORED ***
000AH ***IGNORED ***
000CH ***IGNORED ***
000DH ***IGNORED ***
000EH ***IGNORED ***
000FH ***IGNORED ***
0010H ***IGNORED ***
0011H ***IGNORED ***
0012H ***IGNORED ***
0013H ***IGNORED ***
0014H ***IGNORED ***
0000H 8088 CPU TEST                                    PASSED
0001H CPIO 8259A INTERRUPT TEST                        PASSED
0002H 8088 SOFTWARE INTERRUPT TEST                     PASSED
0003H FAILSAFE TIMER TEST (88)                         PASSED
```

```
0008H IEU RAM REFRESH TEST                                    PASSED
0009H CPIO RAM REFRESH TEST                                   PASSED
FLOPPY DISK DRIVE(S) TO BE TESTED:
     0: DRIVE 0      1: DRIVE 1      B: BOTH DRIVES
ANSWER (0,1 OR B): *
```

5. To run the Floppy Disk Seek Test on Floppy Drive #0, type:

NOTE

This test will not destroy data contained on the Supplemental Diagnostic diskette; therefore, it can remain in the drive. If a test fails, refer to Chapter 5.

```
0<cr>
```

6. The LED on Floppy Drive #0 lights for approximately 1 minute and then the following message is displayed:

```
000BH FLOPPY DISK SEEK TEST                                   PASSED
0015H CPIO 8089 HANG CATCHER TEST                             PASSED
*
```

7. To transfer control back to the Series IV Diagnostic Monitor, type:

```
EXIT<cr>
```

8. When transfer of control to the Series IV Diagnostic Monitor has completed, the following prompt is displayed:

```
>
```

2.11 Load and Run SIVEXT

The SIVEXT test suite is executed by performing the following:

1. Ensure that the Supplemental Diagnostic diskette is in Floppy Drive #0 and the Series IV Diagnostic Monitor has been loaded (Paragraph 2.9). Then load the SIVEXT test suite and the Test Monitor (TMON) by typing:

```
ZSIVEXT<cr>
```

2. The LED on Floppy Drive #0 lights for approximately 30–40 seconds, and then the following message is displayed:

```
File SIVEXT loaded

SERIES IV IEU, EXTRA RAM DIAGNOSTIC TEST Vx.y
*
```

3. To run the pre-selected SIVDIA tests, type:

```
T<cr>
```

NOTE

The SIVEXT test suite having been loaded into the system now begins testing the IEU and extra memory boards and because of the **T<cr>** command, finishes after the tests run one time.

4. After approximately 1 to 1.5 minutes, the following message should be displayed:

```
0007H ***IGNORED ***
000DH ***IGNORED ***
000EH ***IGNORED ***
```

```
0000H 8085 RESET                                    PASSED
0001H 8085 CPU                                      PASSED
0002H FIFO CONTROL PORT                             PASSED
0003H IEU 8259A INTERRUPT                           PASSED
0004H FAILSAFE TIMER                                PASSED
0005H TIMER COUNT                                   PASSED
0006H IEU CONTROL PORT                              PASSED
0008H EXTRA RAM DATA BUS RIPPLE                     PASSED
0009H EXTRA RAM ADDRESS BUS RIPPLE                  PASSED
000AH EXTRA RAM MARCH                               PASSED
000BH EXTRA RAM REFRESH                             PASSED
000CH EXTRA RAM ADDRESS                             PASSED
*
```

NOTE

If a test fails, refer to Chapter 5.

5. To transfer control back to the Series IV Diagnostic Monitor, type:

   `EXIT<cr>`

6. When transfer of control to the Series IV Diagnostic Monitor has completed, the following prompt is displayed:

   `>`

7. If the system being tested has an integral 5¼″ Winchester Disk Drive, proceed to Paragraph 2.12; otherwise, proceed to the next step.
8. Remove the SIV Supplemental Diagnostic diskette from Floppy Drive #0.
9. Refer to Figure 2-1, Series IV Installation Procedure Flowchart, for direction as to installing any optional features and/or software.

2.12 Load and Run SIVWIN

The SIVWIN WSST86 test suite is executed by performing the following:

1. Ensure that the Supplemental Diagnostic diskette is in Floppy Drive #0 and the Series IV Diagnostic Monitor has been loaded (Paragraph 2.9). Then load the SIVWIN test suite and the Test Monitor (TMON) by typing:

   `ZSIVWIN<cr>`

2. The LED on Floppy Drive #0 lights while the test suite/TMON is being loaded into memory (approximately 30–40 seconds); upon completion, the following message is displayed:

   ```
   File SIVWIN loaded
   SERIES IV WINCHESTER/SMD SDT, Vx.y
   WSST86, Vx.y
   ```

3. After the sign-on message is displayed, a series of questions will appear on the screen as shown in Figure 2-4. The default answer will be displayed in brackets. To initialize the test in the default condition, enter a carriage return (<cr>) when prompted with an asterisk.

NOTE

Affirmative responses to the yes/no questions consist of a "Y" or "y" followed by a carriage return. Negative responses consist of a "N" or "n" followed by a carriage return. When a carriage return only is pressed, the default answer enclosed in brackets is assumed.

```
SERIES IV WINCHESTER/SMD SDT, Vx.y
WSST86, Vx.y
CURRENT WAKEUP ASSIGNMENTS
  CONTROLLER WAKEUP
  iSBC-215   2063H
  iSBC-215   2065H
  iSBC-215   2066H
  iSBC-215   2064H
DO YOU WANT TO CHANGE THE DEFAULT WAKEUP ASSIGNMENTS?(Y / [N]): *<cr>
CONTROLLER RESPONSE TEST:
 iSBC-215 ( 2063H ) ... NO RESPONSE
 iSBC-215 ( 2065H ) ... RESPONDED
 iSBC-215 ( 2066H ) ... NO RESPONSE
 iSBC-220 ( 2064H ) ... NO RESPONSE
''NO RESPONSE'' INDICATES THE CONTROLLER IS DEFECTIVE OR NOT INSTALLED.

CURRENT DRIVE CHARACTERISTICS FOR RESPONDING CONTROLLERS:

                                                    SECTORS  BYTES    TOTAL
                          TOTAL    HEADS    HEADS    PER      PER      ALTERNATE
CONTROLLER   WAKEUP  DRIVE CYLDRS   FIXED    RMVBL    TRACK    SECTOR   CYLINDERS
 iSBC-215    2065H    0    525T     5T       0T       12T      512T     10T
 iSBC-215    2065H    1    0T       0T       0T       0T       0T       0T
 iSBC-215    2065H    2    0T       0T       0T       0T       0T       0T
 iSBC-215    2065H    3    0T       0T       0T       0T       0T       0T
DO YOU WANT TO CHANGE THE DRIVE CHARACTERISTICS?(Y / [N]): *<cr>
DRIVE RESPONSE TEST:

 iSBC-215H      DRIVE 0      DRIVE 1      DRIVE 2      DRIVE 3
 2065H          RESPONDED    NOT USED     NOT USED     NOT USED

IS THE DRIVE BACKED UP? (Y / [N]: *<cr>
*
```

Figure 2-4. Default Initialization Menu for Series IV 5¼″ Winchester

4. Once the initialization is complete, the system will display an asterisk.
5. To begin testing, enter the following command:

   *T<cr>

6. At the completion of each test, the test number, test name and its status (i.e. PASSED or FAILED) will be displayed on the terminal. Those tests that are in the "default ignored condition" will be listed as *** **IGNORED** *** when testing begins. A sample output of a passing system is given in Figure 2-5.

2.13 System Options

NOTE

If none of the options listed below are to be installed, proceed to Paragraph 2.14.

```
000CH *** IGNORED ***
000FH *** IGNORED ***
0014H *** IGNORED ***
0015H *** IGNORED ***
0016H *** IGNORED ***
0017H *** IGNORED ***
0018H *** IGNORED ***
0019H *** IGNORED ***
001AH *** IGNORED ***
001BH *** IGNORED ***
001CH *** IGNORED ***
0000H RESET DISK TEST                          ''PASSED''
0001H ROM CHECKSUM TEST                        ''PASSED''
0002H RAM WINDOW TEST                          ''PASSED''
0003H RAM ADDRESS TEST                         ''PASSED''
0004H TRANSFER STATUS TEST                     ''PASSED''
0005H BUFFER I/O TEST                          ''PASSED''
0006H FORMAT DIAGNOSTICS TRACKS TEST           ''PASSED''
0007H MICRO-DIAGNOSTIC                         ''PASSED''
0008H VERIFY FORMAT/FORMAT TEST                ''PASSED''
0009H SEEK/VERIFY TEST                         ''PASSED''
000AH WORST CASE SEEK TEST                     ''PASSED''
000BH WRITE/READ/VER. DIAG. TRACK TEST         ''PASSED''
000DH PLATTER/HEAD SELECTION TEST              ''PASSED''
000EH SECTOR SELECTION TEST                    ''PASSED''
0010H ALTERNATE TRACK TEST                     ''PASSED''
0011H ZERO FILL TEST                           ''PASSED''
0012H DATA OVERRUN TEST                        ''PASSED''
0013H AUTO-INCREMENT TEST                      ''PASSED''
*
```

Figure 2-5. Sample SIVWIN WSST86 Test Output

The approved options for the Series IV system are as follows:

- iMDX-434 Enhanced Performance Option (Customer installable).
- iMDX-761 External Peripheral Chassis (8″ Winchester Disk Drive).
- 740 Hard Disk.
- iMDX-456 Workstation Option.
- Memory Upgrade.
- In-Circuit Emulator (ICE).
- Centronics Parallel Type Printer (Customer supplied).
- iMDX-580/582 ISIS Cluster Workstation (Customer installable).
- Second-User Terminal (Customer supplied).

The installation of options to the Series IV, other than the iMDX-434, iMDX-580/582 ISIS Cluster, Second-User Terminal and ICE, are technically complex procedures. These options should be installed only by an authorized Intel Customer Service Engineer.

NOTE

The use of ICE in combination with ISIS Cluster, Multi-user mode or Toggle mode has not been defined and is not supported.

Positioning of the boards in the card cage is critical. Each board must be installed in a unique position for each system configuration. Four boards CPIO, IEU, SPU and iSBC-056/iSBC-012 occupy permanent positions, slots 1 through 4 (J10-J7), and will not change with optional system configurations. The other optional boards occupy different slots, depending upon the system configuration. Figure 4-2 shows the placement of each board in the card cage for it's respective system configuration.

After determining the proper board locations (Figure 4-2), insert the board into the appropriate slot by lowering it until it touches the connector. After determining that the board is aligned in the PCB guides and meets the connector properly, firmly push the board into the connector until it securely seats. Connect all appropriate external cables, as required, to the seated board.

2.13.1 iMDX-434 Option

The addition of the iMDX-434 Extended Processing option also requires rejumpering the address lines of the IEU board and the memory board(s). Chapter 4 provides the jumper information needed to reconfigure these boards. The procedure to install and checkout the iMDX-434 option is provided in Appendix B at the rear of this manual.

2.13.2 iMDX-761 External Peripheral Chassis Option

Contact the local Intel Customer Service Engineer to install this option.

2.13.3 740 Hard Disk Option

Contact the local Intel Customer Service Engineer to install this option.

2.13.4 iMDX-456 Workstation Upgrade Kit Option

Contact the local Intel Customer Service Engineer to install this option.

2.13.5 Memory Upgrade Options

The information needed to upgrade the memory size of the Series IV is provided in Chapter 4 of this manual. Bear in mind, that whenever adding memory, rejumpering of the IEU board is required in addition to rejumpering the respective memory board(s). Refer to Figure 4-7 for the memory addressing schemes supported; note the dash number (e.g.; -002) for the boards to be in your upgraded system and then refer to the respective figures for the address jumpers to be installed for that dash number.

2.13.6 Centronics Printer Option

The Series IV interfaces to a Centronics Parallel Type Printer through the Line Printer connector on the back panel (Figure 1-2). The printer interface table (Table 2-1) defines each printer signal on the Line Printer connector.

This interface requires Cable No. 125705-003. It is suggested that a copy of *Centronics Specification* No. C332-44 Rev. A, be obtained before attempting an interface of the printer.

Table 2-1. Series IV, Centronics Printer Interface

Pin No.	Description	Centronics Signal Name
1	Line Printer Data Bit 0	LPDATA0
2	Line Printer Data Bit 1	LPDATA1
3	Line Printer Data Bit 2	LPDATA2
4	Line Printer Data Bit 3	LPDATA3
5	Line Printer Data Bit 4	LPDATA4
6	Line Printer Data Bit 5	LPDATA5
7	Line Printer Data Bit 6	LPDATA6
8	Line Printer Data Bit 7	LPDATA7
9	Logic Ground	GND
10	Logic Ground	GND
11	Logic Ground	GND
12	Logic Ground	GND
13	Fault	FAULT/
14	Data Strobe	DATA STB/
15	Logic Ground	GND
16	Acknowledge	ACKNLG/
17	Busy	BUSY
18	Logic Ground	GND
19	Prime (Reset)	PRIME/
20	No Connection	---
21	Logic Ground	GND
22	Select/	SELECT/
23	Logic Ground	GND
24*	+ 5 Volts dc	5VDC
25*	Chassis Ground	CHASSIS GND

NOTES:
1. A slash (/) following a signal name indicates an Active Low Signal.
2. The asterisk (*) indicates no wires are connected.
3. Printer Connection is Centronics Parallel Type.
4. See *Centronics Specification* C332-44 Rev. A.

2.13.7 iMDX-580/582 Option

The iMDX-580/582 ISIS Cluster Workstation option can only be installed in a Series IV that is a network workstation equipped with software release 2.8 or higher. The information needed to install the iMDX-580/582 option is provided in the *Series IV iMDX 580/582 ISIS Cluster Installation, Operation, and Service Manual,* Order No. 134650.

2.13.8 Second-User Terminal

The information needed to connect a Second-user terminal to a Series IV equipped with software release 2.8 or higher is provided in Appendix C in this manual.

2.14 iNDX System Build

The iNDX System is configured in the following manner:

NOTE

To perform the iNDX System Build, one of the following is required:

- Integral 5¼″ Winchester Disk (WM0)
- iMDX 750 8″ Winchester in P-Box (WD0)
- iMDX 740 fixed platter (HD0)

1. Ensure that the system is powered-up and the Configuration switches are set to select Floppy Drive #0 as the boot device (see Table 3-1).
2. Insert the appropriate diskette, as defined below, in Drive #0. Ensure the diskette is **NOT** write protected (no tab over the Write-Enable slot).

   iNDX.S31 diskette — Series IV without SPU (SIV/3)
   iNDX.S41 diskette — Series IV with SPU installed (SIV/4)
3. Momentarily depress the RESET switch. After the power-up diagnostic tests have completed, the operating system will be booted from the diskette and the following message will be displayed:

```
SIV Boot Vx.y
Mini-floppy dr 0

WAITING FOR WINCHESTER INIT, ...
Copyright 1982, 1983, 1984 Intel Corporation
User space has xxxK bytes
iNDX-Sx1 (Vx.y)

ENTER DATE (mm/dd/yy <cr>):
```

4. Enter the date in the requested format.
5. The system will then prompt for the time as follows:

```
ENTER TIME (hh:mm:ss <cr>):
```

   Enter the time in the 24 hour format.
6. After a few seconds, the iNDX prompt ">" is displayed on line 23 of the CRT screen. On line 25, the **"LOGON"** and **"IMPORT"** and **"EXIT"** command options are displayed in reverse video.

NOTE

Only the letters shown in upper case in the command line (line 25 on the screen) must be typed by the user when entering a command. The remainder of the word is completed by the Syntax Builder feature of the operating system. The Fill command can be used to disable or modify this feature (refer to the *Intellec Series IV Operating and Programming Manual*). In the following procedures all user input is shown in reverse video.

7. To select the **"LOGON"** command option, depress Function Key F0 and observe the following message on line 23:

```
> logon
```

8. Line 24 prompts you to "ENTER user name". To logon with a user name of SUPERUSER, type:

```
SUPERUSER<cr>
```

9. When queried for the password, enter PASSME (default password).
10. After a few seconds, another prompt, ">", is displayed on line 23 followed by seven commands in reverse video.

NOTE

You are now logged onto the system. Next, the Submit command will be used to format the System Disk and copy the system files from the diskette to the System Disk.

11. To select the Submit Command, type:

    SU (Do not depress <cr>)

12. On line 23 of the CRT observe:

    >submit

13. To complete the Submit command line and start the formatting and copying process, enter:

    /iNDX.Sx1/SYSTEM.BUILD (FL0,sdt,vrd)<cr>

    where:

iNDX.Sx1	=	volume root directory name of the source diskette (iNDX.S31 or iNDX.S41)
FL0	=	source floppy device name
sdt	=	target system disk device name; for example, — WM0 (integral 5¼" Winchester) — WD0 (8" Winchester in P-Box) — HD0 (iMDX-740 fixed platter)
vrd	=	volume root directory name being assigned to the target System Disk (e.g.; W0, MW, WINI0, SYS.DSK); the name can be up to 10 characters.

14. After a few seconds, a full screen of text will be displayed. Read through the text and ensure that the appropriate disk drive is being formatted with the Volume Root Directory Name specified in the submit command file.
15. To continue, type:

    <cr>

NOTE

The formatting and copying process will take approximately 20 to 30 minutes.

16. When copying has been completed and a single prompt, ">", is displayed on line 23, logoff from the system by typing:

    LOGOff<cr>

17. After the next prompt is displayed on line 23, remove the iNDX.S31 or iNDX.S41 Diskette from Floppy Drive #0.

NOTE

The System Disk now contains the operating system and several of the iNDX files. From this point on, you will boot from, logon and run the system from the System Disk.

18. Set the Configuration switches to select the System Disk as the boot device (refer to Table 3-1).

19. Momentarily depress the RESET switch to start booting the operating system from the System Disk.
20. When prompted, enter the DATE and then the TIME.
21. Refer to steps 7 through 9 and Logon as SUPERUSER and enter the password.

NOTE

You are now logged on the system. To copy the remainder of the iNDX command files from the iNDX.CUSPS diskette to the System Disk, proceed to Paragraph 2.15.

2.15 CUSPS Copy

1. Insert the iNDX.CUSPS Diskette into Floppy Drive #0. Select the Submit command by typing:

   `SU` (Do not depress <cr>)

2. Observe line 23 of display for the following:

   `>submit`

3. To complete the submit command line and start the CUSPs Copy process, enter the following:

   `/vrd/CUSPS.COPY (vrd)<cr>`

   where:

   vrd = the Volume Root Directory Name of the System Disk (e.g.; W0, MW, WINI0)

NOTE

The CUSPs COPY process will take approximately 5 to 10 minutes.

4. When the CUSPs Copy has completed, a single prompt will be displayed on line 23. At this time, remove the iNDX.CUSPS diskette.

NOTE

All of the iNDX Command files are now loaded on the System Disk. If you want to copy the ISIS-IV Operating System Files onto the System Disk, proceed to Paragraph 2.16.

2.16 ISIS Build

The ISIS build process is executed as follows:

1. Log onto the system and then insert the ISIS.SYS Diskette into Floppy Drive #0.
2. Select the Submit command by typing:

   `SU` (Do not depress <cr>)

3. Observe the following on line 23 of the CRT screen:

   `>submit`

4. To complete the Submit command line and start the ISIS-IV build process, enter the following:

```
/ISIS.SYS/ISIS.BUILD (ISIS.SYS,vrd)<cr>
```

where:

vrd = Volume Root Directory Name of the System Disk (e.g.; W0, MW, WINI0)

NOTE

The ISIS-IV Build process takes approximately 5 to 10 minutes.

5. When the ISIS-IV Build is complete, a single prompt will be displayed on line 23 of the CRT screen. At this time, remove the ISIS.SYS Diskette from Floppy Drive #0.
6. The system software is now completely installed and the system is ready for use.

CHAPTER 3
SYSTEM OPERATION AND VERIFICATION

3.1 Introduction

This chapter contains information concerning operating controls and indicators, power turn-on, power-up diagnostic testing, and supplemental testing. The information in this chapter is intended to familiarize the operator with the system operation, basic hardware areas and describes the tests that verify overall system performance. Power-up tests are performed automatically upon power turn-on and whenever the system is reset. The supplemental tests should be performed during initial system installation, whenever the system configuration is changed by installing options, whenever system malfunctioning is suspected and also routinely to verify system performance.

3.2 Operator's Controls

The operator's primary interface with the system is through the system keyboard and observing the system response displayed on the CRT screen. There are also several manual controls that control system operation. The following list provides the names and paragraph reference of these manual controls:

1. System Configuration Switches (Paragraph 3-3)
2. Power Circuit Breaker Switch (Paragraph 3-4)
3. Hardware RESET Switch (Paragraph 3-5)
4. CRT Brightness Control (Paragraph 3-7)
5. Drive 0, Drive 1 Latches (Paragraph 3-8)
6. Buzzer (operator programmable) (Paragraph 3-9)

3.3 System Configuration Switches

The System Configuration Switches (S2-1 thru S2-8), located on the back of the system near the RESET switch (see Figure 3-1), select the power line frequency and the device that contains the boot-up program. Unless the switches are properly set, the system will not boot-up or run correctly. Table 3-1 lists the configuration switch settings for each device type presently allowed and provides some typical settings as examples. In the listing, "0" indicates a switch in the down or OFF position; "1" indicates a switch in the up or ON position; "n" indicates a switch in either position (don't care).

NOTE

TABLE 3-1 LISTS THE SETTINGS OF THE EIGHT SYSTEMS CONFIGURATION SWITCHES. THESE SWITCHES MUST BE PROPERLY SET FOR CORRECT SYSTEM OPERATION.

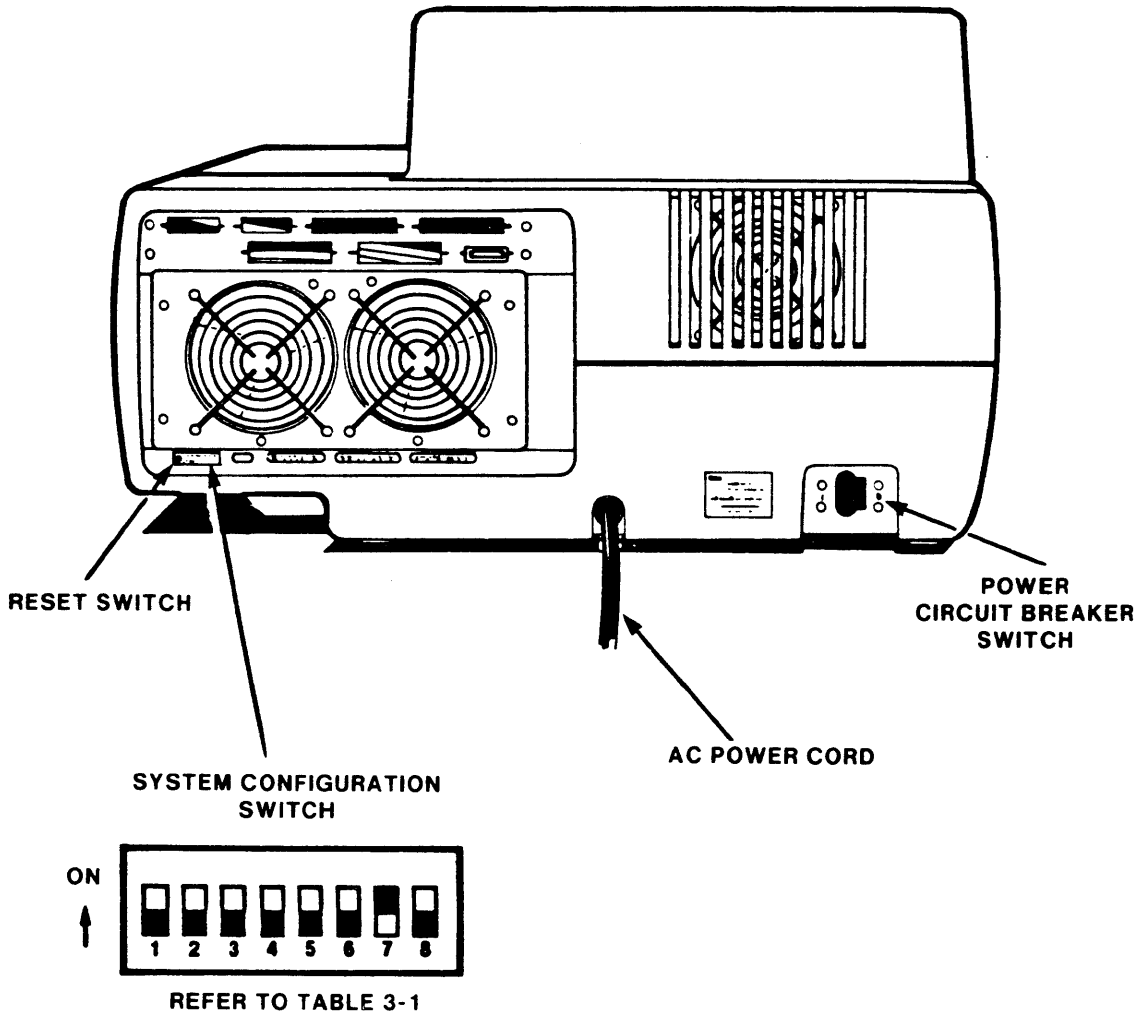


Figure 3-1. Series IV, Systems Control Locations, Rear View

Table 3-1. Series IV, System Configuration Switch Settings

Switch Number/Setting								Function Enabled
1	2	3	4	5	6	7	8	
*	n	0	0	0	0	0	0	Skip power-up test and boot system monitor.
*	n	0	0	0	0	1	0	Boot system from integral floppy disk, drive 0.
*	n	0	1	0	0	1	0	Boot system from integral floppy disk, drive 1.
*	n	0	0	0	1	0	0	Boot system from 740 Hard Disk, fixed platter.
*	n	0	1	0	1	0	0	Boot system from 740 Hard Disk, removable platter.
*	n	0	0	0	1	1	0	Boot system from external peripheral chassis.
*	n	0	0	1	0	1	0	Boot system from integral Winchester drive.
*	n	0	1	1	0	1	0	Reserved for future configurations
*	n	0	0	1	1	0	0	Reserved for future configurations
*	n	0	0	1	1	1	0	Reserved for future configurations
*	n	0	1	1	1	1	0	Reserved for future configurations
*	n	#	#	#	#	#	1	Boot workstation from network.
*	n	0	0	1	1	1	1	Reserved (special case)

NOTES:

1. "0" indicates OFF (down); "1" indicates ON (up); "n" indicates DON'T CARE.
2. Switch 1 (*) selects 60Hz when up (1) or 50Hz when down (0); for CRT scan rate only.
3. Switch 2 (n) is reserved for future configurations.
4. Switches 3 and 4 select boot device unit addresses.
5. Switch 5, 6 and 7 select boot device type.
6. Switch 8 selects network communications booting.
7. # = Bit Substitute; i.e., substitute the bit pattern that corresponds to the device from which the Operating System (OS) will be booted by default. For example, a workstation that uses a 740 fixed platter hard disk, drive 0 as a defaulted boot device, would require a switch pattern of:

   * n 0 0 0 1 0 1

   If network communications are lost, the system will boot from the device selected by switches 3–7.

EXAMPLE SETTINGS OF SYSTEM CONFIGURATION SWITCHES

1. To select a 60Hz standalone system that boots from the integral floppy disk, drive 0:

1	2	3	4	5	6	7	8	Switch Numbers
1	n	0	0	0	0	1	0	Switch Settings

2. To select a 50Hz standalone system that boots from the integral floppy disk, drive 0:

1	2	3	4	5	6	7	8	Switch Numbers
0	n	0	0	0	0	1	0	Switch Settings

3. To select a 60Hz standalone system that boots from an external peripheral chassis:

1	2	3	4	5	6	7	8	Switch Numbers
1	n	0	0	0	1	1	0	Switch Settings

3.4 Power Circuit Breaker Switch

The power circuit breaker switch is located at the left, lower rear of the system (see Figure 3-1). This switch combines an ON/OFF switch, which is used to control application of ac power to the system, with a circuit breaker, which is used for circuit protection against excessive current drain. For user safety, this switch also contains an external trip coil which will remove ac power whenever the top cover is removed. The trip coil is connected, via the top-cover interlock switch (located inside unit on side of the power supply fan), to +12 Vdc. The interlock switch has 3-positions, the down position for normal system operation with top cover installed (+12 Vdc disconnected from trip coil), the middle position which enables +12 Vdc to trip coil and removes ac power (automatically returns to this position when cover is removed), and the up position for removing +12 Vdc from trip coil and thus reapplying ac power (allows maintenance to be performed with top cover removed).

3.5 Hardware Reset Switch

The hardware RESET momentary switch, located on the back of the system (see Figure 3-1), reinitializes the system to a known set of parameters. The system subsequently executes the power-up tests and then reboots, depending upon the configuration switch settings.

3.6 Software Restart Key

The RESTART key can be used to control the running of the Powerup (and RESET) diagnostics tests and to break to the CPIO Monitor (MON88).

3.7 CRT Brightness Control

The CRT brightness control, located under the card cage portion of the mainframe and near the front (see Figure 3-2), controls the brightness of the CRT display. The brightness should be adjusted for comfortable viewing, but not so bright as to cause a halo effect on the display.

3.8 Drive 0 and Drive 1 Latches

The integral floppy disk drives have latches and indicators. These latches, located in the front center of the drives, are opened to insert and remove diskettes. The latches are closed, after a diskette is inserted, to lock the diskette in place and enable the drive to respond to program commands. To open a latch, pull outward on the bottom edge, then release. To close a latch, first insert a diskette, with the write-enable slot on the left (see Figure 3-3), and then press downward and inward on the latch until it locks in place. An LED indicator, located on the front of each drive, lights when its drive is selected and is either reading or writing data (it is not lit while heads are moving between tracks).

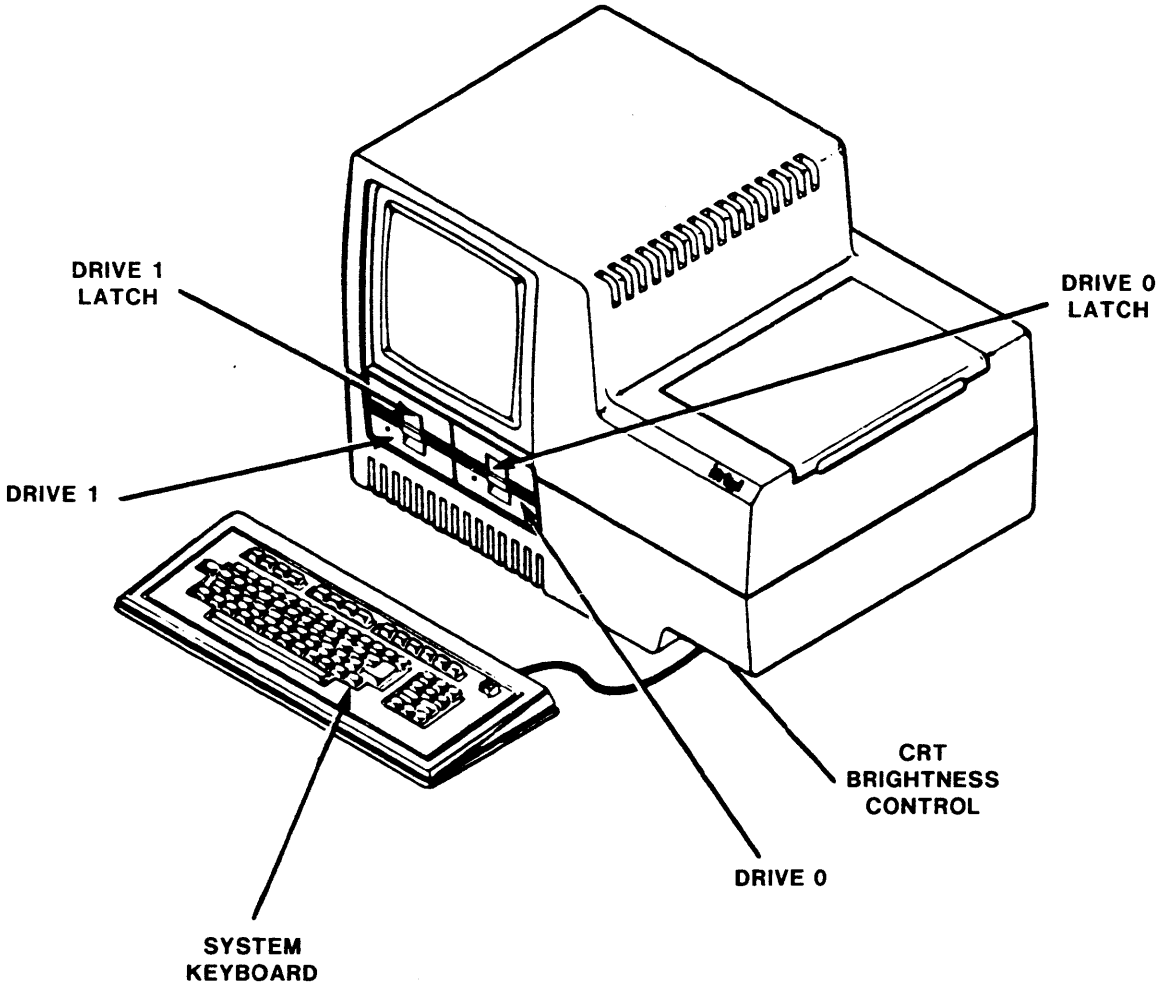


Figure 3-2. Series IV, System Control Locations, Front View

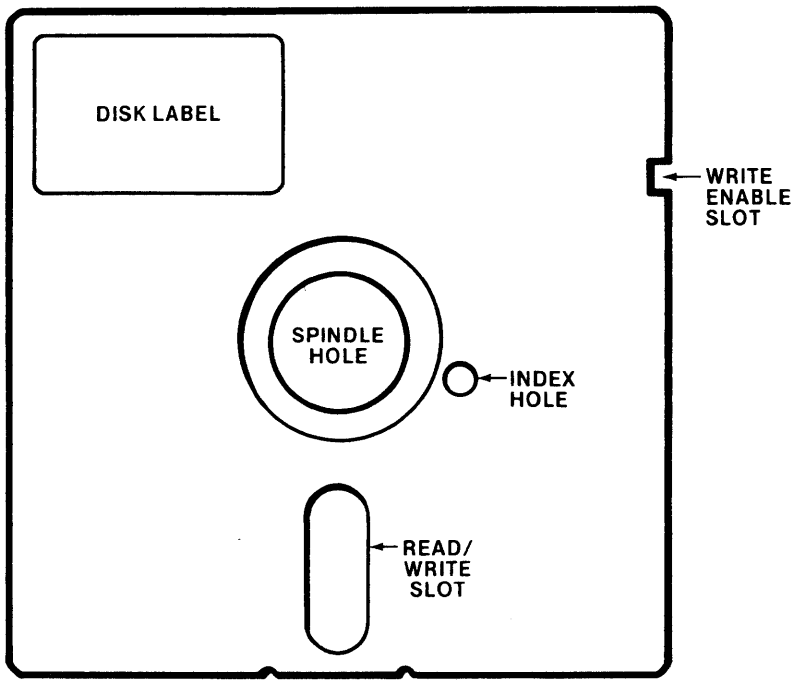
3.9 Buzzer

The buzzer provides an audible alarm to the operator when certain programmed functions occur. This audible alarm generally indicates an abnormal condition or a condition that requires the operators attention. The audible alarm alerts the operator that further action is required.

3.10 Power-Up Tests

The power-up diagnostic tests are used to verify the general operation of the CPIO board and, when installed, the SPU and Ethernet Communications Controller (iSBC-550) boards. Each board contains a PROM in which its tests reside. The power-up tests are automatically invoked each time ac power is applied to the system (power-up) or when the hardware RESET switch is pressed.

The following general discussion focuses about the CPIO since it interacts with the other system boards to report on their status. Detailed descriptions of the



NOTES:

1. **TO PREVENT WRITING ONTO A DISKETTE, COVER THE WRITE ENABLE SLOT.**
2. **TO PREVENT MEDIA DAMAGE AND SUBSEQUENT DATA LOSS, DO NOT TOUCH THE DISKETTE SURFACE IN THE READ/WRITE SLOT.**

Figure 3-3. Series IV, Floppy Diskette, 5¼-inch

power-up testing performed by the CPIO, SPU and iSBC-550 boards are presented in the following paragraphs.

For the purpose of the following discussion, it is to be assumed that the SPU and iSBC-550 optional boards are installed along with the IEU board and no diskette installed in Floppy Drive 0 (the boot device selected via the Configuration Switches). In this situation, the following message should be displayed on the CRT screen upon successful completion of all power-up tests (approx. 40 sec.).

```
SERIES IV SYSTEM POWER-UP DIAGNOSTIC,Vx.y
CPIO PHASE I ..................................................... / PASSED
CPIO PHASE II .................................................... / PASSED
FLOPPY DRIVE NOT READY SPU ....................................... / PASSED
iSBC-550 ......................................................... / PASSED
CPIO/SPU MULTIBUS TEST ........................................... / PASSED
IEU ..................................................... / INSTALLED

SIV Boot Vx.y
Mini-floppy dr.0
 -device failure
Error 3800

Attempt to reboot from : Mon88
SERIES IV CPIO MONITOR Vx.y                    (where x.y is the release level)
```

The sequence of the power-up diagnostic testing results displayed above is as follows. As stated previously, the power-up tests of each board are invoked by the system firmware when either ac power is applied to the system or the RESET switch is pressed. The CPIO begins its self-testing by running tests 1 through 5 (refer to Table 3-2 for test name and description) to ensure that the minimal hardware is operational; if these tests are successfully completed, the "CPIO PHASE I ... / PASSED" message is displayed and diagnostic testing continues. At this point in the testing, the user has the opportunity (5 seconds) to interrupt the power-up diagnostics by pressing the keyboard RESTART key. The following message will be displayed on the 25th line of the screen to indicate this option to the user.

```
WAITING 5 SECONDS FOR OPTIONAL INTERVENTION
```

If the RESTART key is hit within the 5 second period, the system breaks to the monitor; otherwise, the following message is displayed on the 25th line and the power-up diagnostics continue on to Phase II testing.

```
NO INTERVENTION DETECTED / DIAGNOSTIC PROCEEDING
```

If an error is detected and "CPIO PHASE I ... / FAILED" is displayed, the power-up diagnostics provide user friendly messages to identify the test that failed and then transfer control to the CPIO Monitor (MON88).

NOTE

The transfer to MON88 occurs whenever a "FAILED " message is displayed for any test. The user friendly messages provided are described later in this chapter under the heading: POWER-UP TESTS ERROR REPORTING.

The CPIO power-up diagnostic testing continues by invoking tests 6 thru 15. If all tests are successfully completed, the "CPIO PHASE II ... / PASSED" message is displayed. As defined in the example system, with the latch on Floppy Drive #0 open, the next message to be displayed will be "FLOPPY DRIVE NOT READY".

The CPIO then accesses the SPU to report the results of its on-board PROM testing ("SPU ... / PASSED); it then accesses the iSBC-550 board to report its status ("iSBC-550 ... / PASSED).

When the SPU is installed, proper operation of the Multibus Controller Logic on both the SPU and CPIO must also be verified. This is performed by first executing, from the CPIO firmware, an address bus ripple test on memory which resides on the SPU. Next, the SPU executes a memory address test on the CPIO memory. If both tests pass, the two tests are executed simultaneously to verify the Multibus Arbitration Logic. Upon successful completion, the message "CPIO/ SPU MULTIBUS TEST ... / PASSED" is displayed. Note that the Multibus Controller Logic is tested only when the SPU is installed and its initial power-up test was successfully completed.

The CPIO accesses the IEU simply to report on whether or not it is installed. Upon completion of testing, the power-up diagnostics transfer control to the bootload firmware.

NOTE

In the example, the system was to boot from the 5¼-inch Floppy Disk Drive #0 and the CPIO Bootload Firmware would have initiated a command for it to do so. In this instance, a "– device failure Error 3800" message, describing the boot failure is displayed. This display is correct since the selected floppy boot device does not have a diskette installed; the message is also displayed whenever the drive door is left open.

Total run time for the execution of all power-up diagnostic tests should be less than 60 seconds.

To confirm a power-up test failure, press the hardware RESET switch to reinitialize the test. If the failure is repeated, refer to Chapter 5 for service information.

Do not attempt to operate the system if the power-up test has a repeatable failure. Operating the system may induce errors in programs or damage components.

3.10.1 CPIO Board Power-Up Test Description

The CPIO tests are divided into five basic groups: 8088 processor tests, memory tests, video subsystem tests, keyboard/lineprinter/floppy disk subsystem tests, and the interrupt/timer tests. The test names and descriptions are presented in Table 3-2 in the order in which they are executed. The error message(s) that may be displayed for each test should it fail, are presented later in this chapter under the heading: CPIO Power-up Error Reporting.

In Table 3-2, there are additional tests listed (tests 16-19) that are not run during the CPIO Phase I and Phase II power-up testing. To run these tests, it is necessary to use the "T" command while in the CPIO monitor (MON88).

To run any of the CPIO power-up tests while in MON88, type the following after the dot prompt is displayed:

```
.T n<cr>
```

where:

n equals a test number listed in Table 3-2.

After receiving this command, MON88 transfers control of the system back to the CPIO power-up diagnostics to execute the selected test and loop on it repeatedly.

During the execution of the 'T' command, the test status for all tests except Test 5 will appear on the 25th line of the display as follows:

```
TEST NAME XXXX FAILS IN YYYY TRIALS
```

where:

XXXX is the number of times the test failed.
YYYY is the number of times the test ran.

A blinking "H" is displayed in the upper left corner of the CRT screen as an indicator that testing is in progress for Test 5.

To guarantee valid test results, the RESET switch should be used to exit all tests. It should be noted, that the RESET switch must be used to exit Tests 8, 12 and 14. The RESTART switch can be used to exit other tests.

Table 3-2. CPIO Power-Up Test Descriptions

Sequence	Test Name/Description
1	**8088 Basic ALU Test** — Verifies the basic operations of the 8088, including register addressing, logic, shift and rotate instructions, stack instructions, and jump and unconditional jump instructions.
2	**EPROM Checksum Test** — Generates checksums for all EPROM devices and compares the checksums to expected values (value = socket number of EPROM).
3	**CRT UPI ROM Test** — Verifies contents of the CRT UPI (8741A) ROM by performing checksum of the ROM space (expected result is '0'). Note that the UPI ROM is accessed by using the special UPI Read ROM instruction which has been dedicated for diagnostic use only.
4	**Video UPI RAM Test** — Verifies proper operation of the Video UPI RAM by invoking a firmware diagnostic routine which resides within the CRT UPI ROM.
5	**Video Counter Test** — Verifies operation of the CPIO on-board video circuitry by monitoring the video data stream and keeping count of the number of video transactions that occur between vertical retrace intervals. A video counter in the CRT subsystem is used. This test is initiated by feeding the letter 'H' through the CRT UPI subsystem and enabling the counter. After a predefined period, the counter is stopped and its contents verified. Note that during this test, the H character will be continually blinking on the left upper corner of the CRT.
6	**RAM Data Bus Ripple Test** — Verifies data lines by rippling a logic 1 across the data lines writing to test locations in each memory bank. Then data lines are checked for a fixed logical '1' state.
7	**RAM Address Bus Ripple Test** — Verifies address bus by initializing selected RAM test locations to '0' then rippling a logic 1 across the address bus and writing an alternating test pattern. Then the test locations are read to verify correct access.
8	**RAM March Test** — Marches an alternate pattern upward through memory, then marches its complement downward through memory. The pattern is read at each memory location. Takes 9 sec. for one pass.
9	**8088 Extended ALU Test** — Tests functions on the 8088 such as integer multiply and divide, indirect addressing, general arithmetic instructions using double words and unsigned and signed operands.
10	**Keyboard Reset Test** — Test is invoked by the CPIO sending KB RESET/ to the Keyboard. The Keyboard diagnostics include the RAM/ROM checksum test, FIFO test and matrix shorts test. Note: if a key is pressed while test is in progress, a FATAL KEYBOARD ERROR is likely to occur; hit RESET to start over.
11	Line Printer UPI ROM Test — Invokes the line printer subsystem 8741A ROM checksum test. The 8741A executes the test and reports status back to the 8088 CPU.
12	**Line Printer UPI RAM Test** — Invokes the line printer subsystem 8741A RAM test. The 8741A executes and reports status back to the 8088 CPU.

Table 3-2. CPIO Power-Up Test Descriptions (Cont'd)

Sequence	Test Name/Description
13	**8259A Interrupt Controller Test** — Verifies ability to access the Programmable Interrupt Controller by writing data patterns to the 8259A mask register and verifying the data patterns.
14	**8253 Programmable Interval Timer Test** — Verifies ability of the three 8253 counters to count down; also verifies ability of Counter 2 to generate Interrupt 0 upon reaching terminal count.
15	**Basic Floppy Drive Test** — Verifies the operation of the CPIO floppy drive control circuits. First, the 8089 is initialized, then the sense drive status is sent to the 8272, which causes the basic status of Drive #0 (only)to be checked.
*16	**Floppy Drive 0 Seek Test** — A worst case seek test sequence is exercised, seeking a minumum to maximun track number 11 times. The drive then seeks several other track seek combinations. The Read ID is read at each seek to ensure that the drive head is on the correct track. A formatted diskette must be used for this test.
*17	**Floppy Drive 1 Seek Test** — Same as Test 16.
*18	**Floppy Drive 0 Format/Write/Read** — Verifies the operation of the disk drive by formatting the diskette and performing read/write operations.
*19	**Floppy Drive 1 Format/Write/Read Test** — Same as Test 18.

* Denotes tests that are not run during the power-up sequence but can be run from MON88 for additional fault analysis.

3.10.2 SPU Board (Optional) Power-Up Test Descriptions

Table 3-3 lists the optional SPU board power-up tests by names and provides a brief description of each test. All numbers used for the tests and in the test descriptions are hexadecimal (H). The error messages that may be displayed for each test will be presented in this chapter under the heading: SPU Error Reporting.

Table 3-3. Series IV, SPU Power-up Tests

Test No.	Test Name	Test Description
0001H	PROM Checksum	Generates a checksum of the PROM contents and then verifies that it compares to a stored checksum.
0002H	SPU Data Bus Ripple	The error correction unit is enabled and a logic 1 is rippled across the data bus and verified.
0003H	SPU Address Bus Ripple	The error correction unit is enabled and a pattern is written to all memory locations. The locations are then read and verified, the pattern is complemented, written again and the complemented pattern is then read and verified.
0004H	SPU RAM March	The error correction is enabled and a pattern is written to all locations of the SPU memory. The pattern is then read and verified, complemented, then written, read and verified again.

Table 3-3. Series IV, SPU Power-up Tests (Cont'd)

Test No.	Test Name	Test Description
0005H	ECC Syndrome	Checks operation of the error correction unit by inputting correctable errors and reading and verifying each of the 16 bits.
0006H	Force Uncorrectable Error	Checks operation of the error correction unit by generating a two-bit error and verifying that an uncorrectable error signal results.
0007H	SPU Timer	Checks the counting capability of all three counters on the programmable interval timer.
0008H	SPU FIFO	Writes and verifies 16 different patterns for the FIFO and then repeats the process with the complement patterns.
0009H	SPU Local Interrupt Controller	Generates interrupts and checks that the correct interrupts are issued by the controller.

3.10.3 iSBC-550 Power-Up Test Descriptions

Table 3-4 lists the iSBC-550 power-up tests by names and provides a brief description of each test. All numbers used for the tests and in the test descriptions are hexadecimal (H).

Table 3-4. iSBC-550 Power-up Test Descriptions

Test No.	Test Description
	COMMUNICATION PROCESSOR BOARD
1H	**DRAM Data Ripple Test** — Verifies dynamic RAM data lines by rippling a logic 1 across the data bus during write/read cycles to on-board DRAM memory.
2H	**DRAM March Test** — Tests all 16K bytes of dynamic RAM memory by executing standard march algorithm.
3H	**SRAM Data Ripple Test** — Verifies static RAM data lines by rippling a logic 1 across the data bus during write/read cycles to on-board SRAM memory.
4H	**SRAM March Test** — Tests all 8k bytes of static RAM memory by executing standard march algorithm.
5H	**Lower PROM Checksum Test** — Generates a checksum for the low byte PROM device and compares the checksum to a stored checksum value.
6H	**Upper PROM Checksum Test** — Generates a checksum for the high byte PROM device and compares the checksum to a stored checksum value.
7H	**8255A Port B Write/Read Test** — Verifies ability of 8088 CPU to write/read 8255A Port B.
8H	**8237 Write/Read Test** — Verifies ability of 8088 CPU to write/read 8237 Channel 0 Address Register.
9H	**8259A Write/Read Test** — Verifies ability of 8088 CPU to write/read 8259A mask register, issue a clear interrupt command, and read 8259A interrupt status.
AH	**8253 Counter 0 Test** — Verifies ability of Counter 0 to generate Interrupt 5 on reaching zero.
BH	**8253 Counter 1 Test** — Verifies ability of Counter 1 to generate Interrupt 6 on reaching zero.
CH	**8253 Counter 2 Test** — Verifies ability of Counter 2 to generate Interrupt 7 on reaching zero.

Table 3-4. iSBC-550 Power-up Test Descriptions (Cont'd)

Test No.	Test Description
	SERDES BOARD
DH	**Address PROM Read/DMA Receive Channel 1 Test** — Reads SerDes board address PROM through DMA receive channel 1 to verify proper operation of read address and receive channel 1 circuits.
EH	**DMA Receive Channel 2 Test** — Reads SerDes board address PROM through DMA receive channel 2 to verify proper operation of receive channel 2.
FH	**DMA Receive Channel 3 Test** — Reads SerDes board address PROM through DMA receive channel 3 to verify proper operation of receive channel 3.
10H	**Address ROM CRC Test** — Reads SerDes board address PROM and generates a 16-bit CRC (circular ROM check) to verify contents of the address PROM.
11H	**Broadcast Packet Recognize/Receive Good CRC Test** — Controller executes an on-board verify operation with a broadcast address to test transmit, receive, and CRC circuits and ability to recognize broadcast packets.
12H	**Receive Bad CRC Test** — Controller executes an on-board verify operation while forcing a CRC error during transmission to test ability of CRC logic to detect CRC errors.
13H	**Address Recognition Circuitry Test** — Controller executes an on-board verify operation with a packet containing the controller's Ethernet address to ensure that the controller accepts packets addressed to it.
14H	**Non-Self Addressed Packet Recognition Test** — Controller executes an on-board verify operation with a packet containing a wrong Ethernet address to ensure that the controller rejects packets addressed to other controllers.
15H	**On-Board Loopback Path** — A routine used by Tests 11-14H to execute on-board verify operations.

3.10.4 CPIO/SPU Multibus Test Description

This test verifies the proper operation of the Multibus Controller Logic on both the CPIO and SPU boards. It is a three part test in which the CPIO and SPU are first directed to read and write individually to each others memory to test the others receivers and drivers and then, only upon successful completion, directed to execute the tests simultaneously to check their Multibus Arbitration Logic. The three parts of the test are futher defined as follows:

NOTE

This test is performed only when the SPU is installed and its testing passed.

1. The CPIO firmware begins the testing by executing an address bus ripple test on the second page of SPU memory (page 5) to check the CPIO Multibus drivers and receivers. During this part of the test, the following message is displayed on line 25:

   ```
   TRYING TO ACCESS SPU MEMORY
   ```

   If a failure is detected during any part of this test, the power-up diagnostics will end the test and the following message will be displayed:

   ```
   CPIO/SPU MULTIBUS TEST ..... / FAILED
   ```

   Otherwise, the test proceeds to part two.

2. The SPU executes a memory address test on the second half of page two of the CPIO memory to check the SPU Multibus drivers and receivers. If a failure is detected, control will be transferred to MON88; otherwise, the test proceeds to part three.

3. Part three of the test involves executing parts one and two again simultaneously to verify proper operation of the Multibus Arbitration Logic on both the boards. Upon successful completion, the following message is displayed:

```
CPIO/SPU MULTIBUS TEST ..... / PASSED
```

NOTE

If the keyboard RESTART key was pressed after the 5 second optional intervention message was displayed, the CPIO will report either the SPU missing or the CPIO/SPU MULTIBUS TEST ..... / FAILED depending upon when the key was pressed.

3.11 Power-Up Tests Error Reporting

Error reporting for the power-up diagnostics is divided into two groups: CPIO Power-up Error Reporting and Optional Board Power-up Error Reporting.

3.11.1 CPIO Power-Up Error Reporting

When a CPIO hardware failure is detected, one of the following fail messages will be displayed.

```
CPIO PHASE I ..... / FAILED
TEST NAME ERROR / ERROR INFORMATION
```

OR

```
CPIO PHASE II ..... / FAILED
TEST NAME ERROR / ERROR INFORMATION
```

Following the fail message will be useful error information to help the user isolate the failure. Error information pertaining to memory tests will also contain data such as address of the memory location where the fault was detected, data expected by the test, and data received by the test. The error information that may be displayed is as follows:

Test Name Error	Error Information
CPIO PHASE I	
8088 BASIC ALU	STACK ERROR AT *xxxx:yyyy*,EXP.DATA *zz*H, REC.DATA *uu*H
8088 EXTENDED ALU	MULTIPLY/DIVIDE ERROR ARITHMETIC ERROR CONVERSION ERROR TRANSLATION ERROR
PROM CHECKSUM	SOCKET NUMBER *xx*
CRT UPI ROM	None
VIDEO UPI RAM	None
VIDEO COUNTER	EXP. CNTR VALUE *xx*H, REC. CNTR VALUE *yy*H

Test Name Error	Error Information
CPIO PHASE II	
RAM DATA BUS RIPPLE	AT *xxxx:yyyy*, EXP.DATA *zz*H, REC.DATA *uu*H
RAM ADDR BUS RIPPLE	AT *xxxx:yyyy*, EXP.DATA *zz*H, REC.DATA *uu*H
RAM MARCH	AT *xxxx:yyyy*, EXP.DATA *zz*H, REC.DATA *uu*H
KEYBOARD RESET	CHECKSUM TEST FAILED FIFO TEST FAILED MATRIX SHORT
LPT UPI ROM	None
LPT UPI RAM	None
8253 TIMER	TIMER 0 FAILED TIMER 1 FAILED TIMER 2 FAILED
8259A INTERRUPT CHIPS	MASTER PIC MASK WRITE/READ FAILED SLAVE PIC MASK WRITE/READ FAILED SYSTEM PIC MASK WRITE/READ FAILED MASTER/LEVEL 0/TIMER 2 INT. FAILED SLAVE/LEVEL 0/KEYBOARD INT. FAILED SLAVE/LEVEL 2/USART INT. FAILED SLAVE/LEVEL 4/LINEPRINTER INT. FAILED SLAVE/LEVEL 6/SIGNAL INT. FAILED SLAVE/LEVEL 7/FIFO INT. FAILED SYSTEM/LEVEL *x*/MULTIBUS INT. *x* FAILED
FLOPPY SUBSYSTEM	FAILED TO INITIALIZE 8089 FLIPPY DRIVE NOT READY

3.11.2 Optional Board Power-Up Error Reporting

3.11.2.1 SPU Error Reporting

After getting the error code from the SPU result block, the CPIO power-up diagnostic decodes the received information and displays the following fail message as follows:

```
SPU  ..................................................... / FAILED
```

The above message will be followed by one of the messages below to define the nature of the error.

```
RAM DATA BUS RIPPLE ERROR / AT xxxx:yyyy, EXP.DATA zzH,
   REC.DATA uuH
RAM ADDR BUS RIPPLE ERROR / AT xxxx:yyyy, EXP.DATA zzH,
   REC.DATA uuH
RAM MARCH TEST ERROR / AT xxxx:yyyy, EXP.DATA zzH, REC.DATA uuH
ECC SYNDROME ERROR
ECC UNCORRECTABLE ERROR DETECT ERROR
EPROM CHECKSUM ERROR
SPU TIMER ERROR
SPU FIFO ERROR
LOCAL INTERRUPT ERROR
MULTIBUS INTERRUPT ERROR
```

3.11.2.2 iSBC-550 Error Reporting

If a hardware error is detected on the iSBC-550, the following message will be displayed.

```
iSBC-550 ..... / FAILED
```

The above message will be followed with one of the messages below to define the nature of the error:

```
PROCESSOR DRAM DATA RIPPLE ERROR
PROCESSOR DRAM MARCH ERROR
PROCESSOR SRAM DATA RIPPLE ERROR
PROCESSOR SRAM MARCH ERROR
PROCESSOR LOWER PROM CHECKSUM ERROR
PROCESSOR UPPER PROM CHECKSUM ERROR
PROCESSOR 8255 PORT B WRITE/READ ERROR
PROCESSOR 8237 WRITE/READ ERROR
PROCESSOR 8259 WRITE/READ ERROR
PROCESSOR 8253 COUNTER 0 ERROR
PROCESSOR 8253 COUNTER 1 ERROR
PROCESSOR 8253 COUNTER 2 ERROR
PROCESSOR DMA RECEIVE CHANNEL 1 ERROR
RECEIVE CHANNEL 2 ERROR
PROCESSOR DMA RECEIVE CHANNEL 3 ERROR
SERDES ADDRESS PROM 16-BIT CRC ERROR
SERDES BROADCAST PACKET RECOGNIZE ERROR
SERDES RECEIVE BAD CRC ERROR
SERDES ADDRESS RECOGNITION CIRCUITRY ERROR
SERDES NON SELF-ADDRESSED PACKET RECOG. ERROR
SERDES ON-BOARD LOOPBACK ERROR
```

3.11.3 CPIO/SPU Multibus Error Reporting

If a failure is detected during any part of the CPIO/SPU Multibus testing, the following message will be displayed:

```
CPIO/SPU MULTIBUS TEST ..... / FAILED
```

along with one of following messages:

```
NO RESPONSE FROM SPU/      (Part 1)

SPU MULTIBUS ERROR/        (Part 1)

CPIO MULTIBUS ERROR/       (Part 2)

FAILE IN COLLISION TST     (Part 3)
```

3.12 Power-Up Procedures

The power-up procedures describe how to properly apply power to the system and observe performance of the power-up tests. Power-up procedures are performed when the system is initially installed (refer to Chapter 2) to ensure that the system functions properly. This initial power-up should be performed before

any optional devices are installed and again after any options are installed to ensure that system performance has not been affected. Finally, power-up procedures are performed whenever power is applied to the system to ensure that the system is set up and initialized properly.

The power-up procedures may vary slightly depending upon the system configuration and application. The following procedure provides the power-up sequence.

To power-up the Series IV:

Step **Perform**

1. Set the System Configuration Switches as required to select the ac source frequency, boot device address, and boot device type (see Table 3-1). If the selected device does not contain the operating program, or the selected device is not functional, the system may transfer control back to the system monitor.

2. Observe that the ac power cord (Figure 3-2) is properly connected to a three-wire power outlet.

NOTE

If the system has an external Winchester drive, it should be powered off before the system power is turned on.

3. Turn on the power circuit breaker switch (back left of system).

NOTE

After power has been removed from the system, the user should not reapply power for 15 seconds.

4. Observe that power is applied to the system (fans running) and the system is proceeding through the power-up diagnostic testing. Before the CPIO finishes the power-up sequence, it will verify the physical presence of the IEU board. An "Error 3800" message will normally be displayed if the User has booted from the 5¼-inch Floppy Drive #0 and a diskette has not yet been inserted in that drive ("Error 3801" if booting from Floppy Drive #1).

Example of "Error 3800" display:

```
SERIES IV SYSTEM POWER-UP DIAGNOSTIC, Vx.y
CPIO PHASE I ..................................... / PASSED
CPIO PHASE II .................................... / PASSED
FLOPPY DRIVE NOT READY SPU ....................... / PASSED
iSBC-550 ......................................... / PASSED
CPIO/SPU MULTIBUS TEST ........................... / PASSED
IEU ..................................... / INSTALLED
SIV Boot Vx.y
Mini-floppy dr 0
- device failure
Error 3800
Attempt to reboot from: MON88
SERIES IV CPIO MONITOR Vx.y
```

5. Turn on power to any connected peripherals such as external peripheral chassis, lineprinters or non-system disk drives (if applicable).

3.13 Boot Loading the Supplemental Level Diagnostics

The following instructions explain how to boot the Supplemental Level Diagnostic Monitor. Note that before the system boots, it executes the power-up tests.

To boot the Supplemental Diagnostic Monitor on the Series IV system:

1. Insert a floppy diskette (5¼-inch) that contains the Supplemental Level Diagnostic Monitor, order number 134444, into the appropriate floppy disk drive (refer to Configuration Switches). Normally, Drive #0, on the right-hand side, is selected to boot the diagnostic monitor. Always insert the diskette with the write-enable slot on the left and the read/write slot to the back of the drive (refer to Figure 3-3). The diagnostic diskette should be write protected by covering over the write-enable slot.
2. Press the RESET switch (back right of system) to reinitialize the system and boot from the integral floppy disk drive. Observe that the system completes the power-up tests (less than 60 seconds), that no error messages are displayed, and that the following sign-on message is displayed:

```
SIV Boot Vx.y
Mini-floppy dr 0
SERIES IV Diagnostic Monitor, Vx.y

>
```

NOTE

If the sign-on message is not displayed, repeat step 2 twice more. If the system still does not sign on, refer to the service information in Chapter 5.

3. Observe that the system sign-on message above is displayed, then proceed to the appropriate supplemental test or system operation as applicable. The supplemental tests must be executed following initial installation, following any configuration change, when a system malfunction is suspected and routinely to assure proper operation.

3.14 Supplemental Test General Information

The supplemental tests run under the control of the CPIO board and provides five unique, dynamic subsystem and peripheral test suites called:

1. SIVDIA
2. SIVEXT
3. SIVWIN
4. SIVCOM
5. SIV740

The SIVDIA test suite exercises the CPIO and SPU boards, while the SIVEXT test suite checks the IEU and extra system RAM memory boards. The SIVWIN test suite checks the operation of the integral (5¼-inch), and peripheral chassis (8-inch) Winchester Subsystems. The SIV740 test suite checks the 740 (hard disk) drive subsystem. The SIVCOM test suite verifies the systems Ethernet Communication Network.

The remaining paragraphs in this chapter describe the supplemental tests, operating procedures, execution times and error messages. Appendix A to this manual describes and provides examples of the Test MONitor (TMON) commands used to run with the supplemental test suites.

Each of the five test suites display error codes or error messages to aid in isolating faults to a replaceable subassembly. The primary factors in isolating failures are the failing test numbers and the total system failure symptoms. Failures are typically caused by faulty printed circuit boards/subassemblies, or bad connections between subassemblies (i.e., oxidation on motherboard connectors, loose cable connector, etc.).

3.15 SIVDIA Supplemental Test Suite

3.15.1 Initiating SIVDIA

At the completion of the power-up test, the SIVDIA test suite may be initiated by performing the following:

NOTE

Make certain the Configuration switches are set to allow booting from Floppy Disk Drive No. 0.

1. Insert a copy of the Series IV Supplemental Level Diagnostic, Order No. 134444, into the floppy disk drive selected as the boot device via the Configuration Switches then close the latch and boot the Supplemental Diagnostic Monitor (Refer to Section 3.13).
2. Type "Z" and the test name "SIVDIA" into the system.
3. Define test suite parameters and start the test procedure. (see Appendix A for TMON commands).

NOTE

Operator entries are shown in reverse video and the ‹cr› indicates pressing the keyboard RETURN key.

Example of initiating SIVDIA:

```
Series IV Diagnostic Monitor, Vx.y
>ZS:VDIA‹cr›
File SIVDIA loaded (after approx. 30-40 sec.)
SERIES IV CPIO, SPU DIAGNOSTIC TEST Vx.y
*
```

4. Enter the following command to execute tests 0000H to 0003H, 0008H, 0009H, 000BH, 000DH - 0014H (if SPU installed) and 0015H:

```
*T‹cr›
```

The SIVDIA test suite, now loaded into the system, begins testing the CPIO, IEU and SPU boards, and finishes after the tests run one time. Also, test 000BH—FLOPPY DISK SEEK TEST—prompts for the drive or drives to be tested; Drive 0 was entered by the user in the example given in Figure 3-4.

As the system exercises each part, the test results are displayed on the CRT. Figure 3-4 shows the display of the CRT screen if all the SIVDIA tests have passed.

NOTE

To exit TMON and return to the diagnostic monitor so that another test suite may be loaded and exercised or testing abandoned altogether, type:

```
*EXIT<cr>
```

```
0004H *** IGNORED ***
0005H *** IGNORED ***
0006H *** IGNORED ***
0007H *** IGNORED ***
000AH *** IGNORED ***
000CH *** IGNORED ***
0000H CPIO CPU TEST                                    "PASSED"
0001H CPIO 8259A INTERRUPT TEST                        "PASSED"
0002H CPIO SOFTWARE INTERRUPT TEST                     "PASSED"
0003H CPIO FAILSAFE TIMER TEST                         "PASSED"
0008H IEU RAM REFRESH TEST                             "PASSED"
0009H CPIO RAM REFRESH TEST                            "PASSED"
FLOPPY DISK DRIVES TO BE TESTED:
     0: DRIVE 0    1: DRIVE 1    B: BOTH DRIVES
ANSWER (0,1 or B) *<cr> (User input)
000BH FLOPPY DISK SEEK TEST                            "PASSED"
000DH SPU WAKE UP TEST                                 "PASSED"
000EH SPU CPU TEST                                     "PASSED"
000FH NORMAL W/R SPU MEMORY TEST                       "PASSED"
0010H SPU CHECK BITS MEMORY MARCH TEST                 "PASSED"
0011H SPU MEMORY REFRESH                               "PASSED"
0012H SPU MEMORY REFRESH ECC OFF                       "PASSED"
0013H CPIO WAKE UP                                     "PASSED"
0014H CPIO FIFO                                        "PASSED"
0015H CPIO 8089 OPERATION TIME-OUT                     "PASSED"
*
```

Figure 3-4. Series IV, CRT Display of SIVDIA Confidence Test

3.15.2 SIVDIA Test Descriptions

Table 3-5 describes the function of each test in the SIVDIA test suite.

Table 3-5. Series IV, SIVDIA Test Descriptions

Test No.	Test Name	Test Description
0000H	8088 CPU	The 8088 microprocessor executes a sequence of assembly language instructions to verify its Arithmetic Logic Unit (ALU).
0001H	CPIO 8259A Interrupt	Generates interrupts and verifies the interrupt vectors to test the three CPIO interrupt controllers.
0002H	8088 Software	Generates and verifies all 256 software interrupts.
0003H	Failsafe Timer (88)	Verifies that the onboard failsafe timer generates an acknowledge signal to the CPU within 10ms of an access to a nonexistent memory or I/O location. **NOTE** Before executing test 0004H, install the line-printer loopback connector, No. 124270, in jack J20 (see Line Printer in Figure 1-2).

Table 3-5. Series IV, SIVDIA Test Descriptions (Cont'd)

Test No.	Test Name	Test Description
*0004H	Lineprinter Loopback	Invokes the lineprinter loopback test resident in the lineprinter subsystem controller (8741A). **NOTE** Before executing test 0005H, install the USART loopback connector, No. 123314, in jack J19 for Serial Channel 1 (see Figure 1-2).
*0005H	USART	Loopback Sets and verifies Request to Send, Clear to Send, Data Terminal Ready, Data set Ready, Transmitted Data and Received Data functions on the CPIO USART (8251).
*0006H	Reserved	Reserved for the 8087 Numeric Processor test that is to be implemented in the future.
*0007H	Keyboard	Enables a full screen display of each character typed. To advance to the next test, type CONTROL-C (press and hold CONTROL key while pressing the C key).
0008H	IEU RAM Refresh	Writes an FFH to all IEU board RAM memory locations, pauses a few seconds, and then checks for changes in data. Next, the same write, wait and check is performed with complement pattern 00H. If a failure occurs, the failed address and expected versus received values are displayed.
0009H	CPIO RAM Refresh	Same as test 0008H except for CPIO board RAM instead of IEU RAM.
		NOTE Test 000AH times out and reports FAILED when no lineprinter is attached to the Series IV.
*000AH	CPIO Lineprinter	Outputs the ASCII character set to the lineprinter five times. When a printer is attached, actual pass/fail status is based on visual inspection of the printer's output.
		NOTE 1. When executing tests 000BH and 000CH, the user is prompted, on the first pass only, to select the floppy disk drive(s) to be tested. 2. Test 000BH requires a formatted diskette installed in the floppy disk drive(s) being tested.
000BH	Floppy Disk Seek	Executes a worst case seek sequence to verify the diskette drive subsystem.
*000CH	Floppy Disk F/W/R	Formats diskette then writes to and reads from random tracks to exercise the diskette drive subsystem. The user is prompted, on the first pass only, to insert a blank diskette into the drive(s) before executing this test.
		NOTE Tests 000DH through 0012H verify the optional SPU board. These tests are performed only if an optional SPU board is installed in the system.
000DH	SPU Wake Up	Verifies communication from the CPIO board to the SPU board 8086 microprocessor.
000EH	SPU CPU	The 8086 microprocessor executes a sequence of assembly language instructions to verify that the processor is functioning properly.

Table 3-5. Series IV, SIVDIA Test Descriptions (Cont'd)

Test No.	Test Name	Test Description
000FH	Normal W/R SPU RAM	Initializes on-board RAM with 00H, verifies the data, writes FFH to RAM, and again verifies the data.
0010H	SPU Check-bits RAM March	Verifies integrity of check RAM by filling check RAM with alternating ones and zeros, verifying the pattern, complementing the pattern, and verifying the new pattern.
0011H	SPU Memory Refresh	Writes data pattern to RAM, waits, and verifies the data pattern.
0012H	SPU RAM March (ECC off)	Writes a data pattern to RAM with Error Correction Unit (ECC) disabled. Verifies the pattern, complements it, and verifies the new pattern. **NOTE** Tests 0013H and 0014H verify communications between the CPIO and SPU boards; therefore, they will only be performed if the SPU board is installed.
0013H	CPIO Wake Up	Verifies communication from the SPU board to the CPIO board 8088 microprocessor.
0014H	CPIO FIFO	Checks the CPIO board FIFO control port protocol from the SPU board 8086 microprocessor.
0015H	CPIO 8089 Operation Time-out	This test checks the 8089 Operation Time-out circuit on the CPIO board.

* Ignored at test initialization

3.15.3 SIVDIA Test Execution Times

Approximate execution times for individual tests or groups of tests are listed in Table 3-6.

Table 3-6. Series IV, SIVDIA Test Execution Time

Test No.	Execution Time
0 to 3	1 second (Combined)
4	ignored
5	ignored
6	ignored
7	ignored
8	15 seconds
9	20 seconds
A	ignored
B	3 minutes
C	ignored
D to F	2 seconds (Combined)
10	10 seconds
11	18 seconds
12	18 seconds
13 to 15	2 seconds (Combined)

3.15.4 SIVDIA Error Messages

Error messages for the SIVDIA test suite always include the failing test number and test name; the messages frequently include the error type and a result word.

The failing test number is the primary factor used to isolate failures to a replaceable subassembly. Failing test numbers and their respective subassemblies are as follows:

Test Number	Subassembly
0 to 3, 9 and 15	CPIO
4	CPIO + LP Loopback Conn.
5	CPIO + Serial Ch. Loopback Conn.
7	CPIO + Keyboard + Keyboard Cable
8	CPIO + IEU
A	CPIO + LP + LP Cable
B,C	CPIO + Floppy Drive(s) + FD Cables
D to 12	SPU
13 and 14	CPIO + SPU

The SPU RAM tests display the failing address, expected data byte, and received data byte for all RAM failures.

In most cases, the system fault may be corrected by replacing the subassembly identified as faulty by the failing test number. In the case of floppy drive test failures, replace the CPIO first. The CPIO board can be replaced quicker than the drive.

When CPIO failures occur along with SPU failures, first replace the CPIO and rerun the tests. A CPIO failure may cause tests run on other boards to fail.

Tests B and C (floppy drive tests) also provide error codes for attempted diskette operations as listed in Table 3-7.

Table 3-7. Diskette Drive Error Codes

Error Code	Error Type
0034	I/O ERROR
0039	BAD COMMAND
2052	TIMEOUT
2060	BAD INTERRUPT
2101	WRITE ERROR
2102	READ ERROR
3010	DELETED DATA ADDRESS MARK NOT FOUND
3020	DATA CRC ERROR
3040	ID CYLINDER MISCOMPARE
3080	SECTOR OUT OF BOUNDS
30A0	ID CRC ERROR
30E0	NO ID ADDRESS MARK FOUND
30F0	BAD DATA ADDRESS MARK FOUND
3100	DATA OVERRUN
3200	WRITE PROTECT
3400	DRIVE FAULT
3700	NO SECTOR FOUND
3710	BAD CYLINDER
3720	SEEK MISCOMPARE
3780	UNEXPECTED INTERRUPT
3800	DRIVE NOT READY
3C00	BAD COMMAND CODE
3C10	BLOCK OVERFLOW
3C20	INVALID COMMAND
3C40	8089 ERROR
3CF0	PROTOCOL ERROR

3.16 SIVEXT Supplemental Test Suite

3.16.1 Initiating SIVEXT

At the completion of the power-up test, the SIVEXT test suite may be initiated by performing the following:

NOTE

Make certain that the Configuration Switches are set to boot from floppy disk drive #0.

1. Insert a copy of the Series IV Supplemental Level Diagnostic, Order No. 134444, into floppy disk drive #0, close the latch and press the RESET switch. (Refer to Section 3.13.)
2. Type "Z" and the test name "SIVEXT" into the system.
3. Define the test suite parameters and start the test procedure. (See Appendix A for TMON commands).

NOTE

Operator entries are shown in reverse video and the <cr> indicates pressing the keyboard RETURN key.

Example of initiating SIVEXT

```
Series IV Diagnostic Monitor x.y
>ZSIVEXT<cr>
File SIVEXT loaded (after approx. 30-40 seconds)
SERIES IV IEU, EXTRA RAM DIAGNOSTIC TEST X.Y
*
```

4. Type the following command to execute tests 0000H–0006H and 0008H–000CH.

```
*T<cr>
```

The SIVEXT test suite, now loaded into the system, begins testing the IEU and extra memory boards, and because of the TEST<cr>, command finishes after the tests run one time.

As the tests exercise the system, the results are displayed on the CRT. Figure 3-5 shows the display of the CRT screen after all the SIVEXT tests have passed.

NOTE

To exit TMON and return to the diagnostic monitor so that another test suite may be loaded and exercised, type:

```
*EXIT<cr>
```

3.16.2 SIVEXT Test Descriptions

Table 3-8 describes the function of each individual test in the SIVEXT test suite.

```
0007H *** IGNORED ***
000DH *** IGNORED ***
000EH *** IGNORED ***
0000H 8085 RESET                                    "PASSED"
0001H 8085 CPU                                      "PASSED"
0002H FIFO CONTROL PORT                             "PASSED"
0003H IEU 8259A INTERRUPT                           "PASSED"
0004H FAILSAFE TIMER                                "PASSED"
0005H TIMER COUNT                                   "PASSED"
0006H IEU CONTROL PORT                              "PASSED"
0008H EXTRA RAM DATA BUS RIPPLE                     "PASSED"
0009H EXTRA RAM ADDRESS BUS RIPPLE                  "PASSED"
000AH EXTRA RAM MARCH                               "PASSED"
000BH EXTRA RAM REFRESH                             "PASSED"
000CH EXTRA RAM ADDRESS                             "PASSED"
*
```

Figure 3-5. Series IV, CRT Display of SIVEXT Confidence Test

Table 3-8. Series IV, SIVEXT Test Descriptions

Test No.	Test Name	Test Description
0000H	8085 Reset	Verifies that a RESET disables the IEU board 8085 microprocessor **NOTE** If test 0001H fails, failures detected in following tests may be misleading.
0001H	8085 CPU	Executes the IEU 8085 microprocessor instruction set and verifies the results. Software interrupts are also tested.
0002H	FIFO Control Port	Checks the IEU board FIFO control port protocol from the CPIO board 8088 microprocessor. FIFO interrupts are also verified.
0003H	IEU 8259A Interrupt	Checks the Multibus interrupts that invoke the IEU 8259A interrupt controller chip.
0004H	Failsafe Timer	Verifies that the IEU board failsafe timer will time out when it attempts to read a non-existant I/O port. The program will automatically seek an unused I/O port.
0005H	Timer Count	Synchronizes and compares the values of the three IEU board counters through 1900 values ranging from 0000H to FFFFH. Also verifies generation of the interrupt level 2 when counter 2 reaches its terminal count.
0006H	IEU Control Port	Verifies the following operations of the IEU board bus public control port: Override (OVRD) Interrupt Interrupt Enable SLAVE LOCK **NOTE** Before executing test 0007H, install the USART loopback connector (P/N 123314) in Serial Channel 2 (see Figure 1-2).
*0007H	USART Loopback	Sets and then verifies the following signals on the IEU USART (8251A): Request to Send, Clear to Send, Data Terminal Ready, Data Set Ready, Transmitted Data and Received Data.

Table 3-8. Series IV, SIVEXT Test Descriptions (Cont'd)

Test No.	Test Name	Test Description
0008H	Extra RAM Data Bus	A logic 1 is rippled across the data bus and data is written into a test location and verified for each 16KB of memory specified.
0009H	Extra RAM Address	A 55H is written into RAM while a Bus Ripple logic 1 is rippled across the address bus. Data are then read, complemented and read again for verification at each location.
000AH	Extra RAM March	A background pattern (55H) is marched upward through the specified memory, complemented, marched downward; each time verifying the complemented pattern.
000BH	Extra RAM Refresh	A background pattern (FFH) is written to all locations and, after a wait period, all locations are checked for changes in data. The procedure is then repeated with the complement (00H) pattern.
000CH	Extra RAM Address	The integrity of both low byte and high byte addressing is checked to locate any RAM addressing problems, such as dual addressing on writes.
*000DH	Extra RAM Walk	Each memory bank is tested separately by writing a background pattern (00H) in all locations. An FFH pattern is then written into each location one at a time. As each location is written, the previous location is complemented, and the background data is read to verify data is unchanged. This test is initially ignored and a RECOGNIZE command must be issued before it is performed.
*000EH	Extra RAM Galpat	A pattern of ones and zeros is galloped (written) through each memory bank to check for pattern sensitivity and access problems. This test is initially ignored and a RECOGNIZE command must be issued before it is performed.

*Ignored at test initialization

3.16.3 SIVEXT Test Execution Times

Table 3-9 shows the approximate execution time of each test in the SIVEXT test suite.

Table 3-9. Series IV, SIVEXT Test Execution Time

Test No.	Execution Time
0 to 6	2 seconds (combined)
7	ignored
8 to 9	2 seconds (combined)
B	50 seconds
C	1 second
D	when recognized (17 hrs/page of mem.)
E	when recognized (23 hrs/page of mem.)

Note: Page of memory equals 64K Bytes. When tests 0D & 0E are executing, the address plus offset currently under test will be displayed in the following format:

```
000DH EXTRA RAM WALK TEST
  @ 3000:25F3
```

3.16.4 SIVEXT Error Messages

When executing the SIVEXT tests and the debug equals 00, the CRT displays only that the test failed. Before setting DEBUG =FF, the CRT displays:

```
test number          test name                          FAILED <===
```

As an example, exercising test 9 would display:

```
*T 9<cr>
0009H    EXTRA RAM ADDRESS BUS RIPPLE                   FAILED <===
```

Activating the debug portion of the test monitor gives the CE more failure information. Using the same test example above and setting debug equal to FF, the CRT displays:

```
*DEBUG =FF<cr>
*T 9<cr>

0009H  EXTRA RAM ADDRESS BUS RIPPLE                     FAILED <===

      ADDR              Expected              Received
      6BA88H              0000                  0100
```

This error message explains that the word at address BA88H of page 6 of the 056 RAM board (see Figure 1-4) received data at the wrong time.

Test 0002H, with debug equal to FF, displays data transfer errors. An example of a Test 2 error is:

```
*DEBUG =FF<cr>
*T 2<cr>

0002H    FIFO CONTROL PORT    TEST (85/88)              FAILED <===

                Error Type                    Result Word
                    *                             **
```

* Error Type:

*xx*1 = IEU failed to request FIFO data
*xx*2 = IEU failed to acknowledge receipt of FIFO data
*xx*4 = CPIO to CPIO failure
*xx*8 = IEU to CPIO failure

** This "Result Word" is always zero.

In most cases, the system fault may be corrected by replacing the subassembly identified as faulty by the failing test number.

When CPIO failures occur along with IEU/RAM failures, replace the CPIO first and rerun the tests. A CPIO failure may cause tests run on the other boards to fail.

3.17 SIVWIN Supplemental Test Suite

The SIVWIN test suite verifies proper operation of the Winchester disk controller boards (iSBC-215B and iSBC-215D) along with the 8-inch Winchester disk drive in the peripheral chassis (P-Box) and/or the integral Winchester disk drive (5¼-inch Wini). The user configures and controls the test through an initialization menu and TMON test commands.

3.17.1 Initiating SIVWIN

A menu of questions will be displayed upon test initialization to allow the user to configure the test suite to match the hardware configuration. Individual tests will be initialized as either ignored or recognized based on how the user answers the menu questions.

Load the SIVWIN WSST86 test suite into memory and then initialize as described in the following procedure.

1. Insert a copy of the Series IV Supplemental Level Diagnostic tests (P/N 134444) into the boot device selected via the Configuration switches. Close the latch and press the RESET switch. The Series IV executes the power-up test sequence and loads the diagnostic test monitor from the diskette. After the power-up test is completed, the following message is displayed on the Series IV terminal:

   ```
   Series IV Diagnostic Monitor x.y
   >
   ```

2. Type "ZSIVWIN" to load the Winchester Diagnostic as shown in the following example:

   ```
   >ZSIVWIN<cr>
   ```

3. The following message is displayed on the terminal when the test suite/TMON have been loaded into memory:

   ```
   File SIVWIN loaded
   SERIES 4 WINCHESTER/SMD SDT, Vx.y
   WSST86, Vx.y
   ```

   NOTE

   Affirmative responses to the yes/no questions consist of a "Y" or "y" followed by a carriage return. Negative responses consist of a "N" or "n" followed by a carriage return. When a carriage return only is pressed, the default answer enclosed in brackets is assumed.

4. All controller board(s) and their assigned Wakeup Ports are then displayed (refer to Figure 3-6). The user is asked if he/she wants to change the current wakeup assignments. The user can respond by typing <**cr**> or **N** or **n**.

5. A controller response test is then executed on each of the current assigned wakeups. If none of the controllers respond, this step will loop forever. When at least one controller responds, this step will terminate.

6. The current drive characteristics are displayed for each drive that is connected to the controller(s) that responded in Step 5. The user is asked if he/she desires to change the drive characteristics. The user can respond by typing <**cr**> or N or **n**. Figure 3-7 shows the responses given when it is desired to change the drive characteristics.

7. A drive response test is executed on each drive that contains more than 0 cylinders as per Step 6. This step loops forever if none of the drives attached to an individual controller respond. This step terminates when at least one drive responds for every controller that responded in Step 5. If a drive is not present and it does not have 0T entered for Total Cylinders, it takes approximately 1 minute to report the NO RESPONSE message.

```
SERIES 4 WINCHESTER/SMD SDT, Vx.y
WSST86, Vx.y
COPYRIGHT INTEL CORP. 1980,1983
CURRENT WAKEUP ASSIGNMENTS
   CONTROLLER   WAKEUP
   iSBC-215      2063H
   iSBC-215      2065H
   iSBC-215      2066H
   iSBC-220      2064H
DO YOU WANT TO CHANGE THE DEFAULT WAKEUP ASSIGNMENTS?(Y / [N]): *<cr>
CONTROLLER RESPONSE TEST:

  iSBC-215 ( 2063H ) . . . NO RESPONSE
  iSBC-215 ( 2065H ) . . . RESPONDED
  iSBC-215 ( 2066H ) . . . NO RESPONSE
  iSBC-220 ( 2064H ) . . . NO RESPONSE

''NO RESPONSE'' INDICATES THE CONTROLLER IS DEFECTIVE OR NOT INSTALLED.

CURRENT DRIVE CHARACTERISTICS FOR RESPONDING CONTROLLERS:

                                                SECTORS BYTES  TOTAL
                         TOTAL  HEADS HEADS PER     PER    ALTERNATE
CONTROLLER WAKEUP DRIVE CYLDRS FIXED RMVBL TRACK   SECTOR CYLINDERS
  iSBC-215  2065H    0   306T    4T    0T    17T     512T     9T
  iSBC-215  2063H    1   0T      0T    0T     0T       0T     0T
  iSBC-215  2063H    2   0T      0T    0T     0T       0T     0T
  iSBC-215  2063H    3   0T      0T    0T     0T       0T     0T
DO YOU WANT TO CHANGE THE DRIVE CHARACTERISTICS?(Y / [N]): *<cr>
DRIVE RESPONSE TEST:

  iSBC-215H       DRIVE 0        DRIVE 1        DRIVE 2        DRIVE 3
2065H             RESPONDED      NOT USED       NOT USED       NOT USED

IS THE DRIVE BACKED UP? (Y / [N]: *<cr>
*
```

Figure 3-6. SIVWIN Default Initialization Menu for 5¼-Inch Winchester Drive

```
SERIES 4 WINCHESTER/SMD SDT, Vx.y
WSST86, Vx.y
COPYRIGHT INTEL CORP. 1980,1983
CURRENT WAKEUP ASSIGNMENTS
   CONTROLLER  WAKEUP
   iSBC-215     2063H
   iSBC-215     2065H
   iSBC-215     2066H
   iSBC-220     2064H
DO YOU WANT TO CHANGE THE DEFAULT WAKEUP ASSIGNMENTS?(Y / [N]): *<cr>
CONTROLLER RESPONSE TEST:

iSBC-215 ( 2063H ) . . . RESPONDED
iSBC-215 ( 2065H ) . . . NO RESPONSE
iSBC-215 ( 2066H ) . . . NO RESPONSE
iSBC-220 ( 2064H ) . . . NO RESPONSE

"NO RESPONSE" INDICATES THE CONTROLLER IS DEFECTIVE OR NOT INSTALLED.

CURRENT DRIVE CHARACTERISTICS FOR RESPONDING CONTROLLERS:

                                              SECTORS BYTES  TOTAL
                         TOTAL  HEADS HEADS   PER     PER    ALTERNATE
CONTROLLER WAKEUP DRIVE  CYLDRS FIXED RMVBL   TRACK   SECTOR CYLINDERS
 iSBC-215  2063H    0    525T    5T    0T     23T     512T   11T
 iSBC-215  2063H    1    525T    5T    0T     23T     512T   11T
 iSBC-215  2063H    2    525T    5T    0T     23T     512T   11T
 iSBC-215  2063H    3    525T    5T    0T     23T     512T   11T
DO YOU WANT TO CHANGE THE DRIVE CHARACTERISTICS?(Y / [N]): *Y<cr>
ENTER INPUT IN DECIMAL

iSBC-215 (2063H) DRIVE: 0
   TOTAL CYLINDERS: 525T
ENTER NEW VALUE OR RETURN TO KEEP: *<cr>
   FIXED HEADS: 5T
ENTER NEW VALUE TO KEEP: *<cr>
   REMOVABLE HEADS: 0T
ENTER NEW VALUE OR RETURN TO KEEP: *<cr>
   SECTORS PER TRACK: 23T
ENTER NEW VALUE OR RETURN TO KEEP: *<cr>
   BYTES PER SECTOR: 512T
ENTER NEW VALUE OR RETURN TO KEEP: *<cr>
TOTAL ALTERNATE CYLINDERS: 11T
ENTER NEW VALUE OR RETURN TO KEEP: *<cr>

iSBC-215 (2063H) DRIVE: 1
   TOTAL CYLINDERS: 525T
ENTER NEW VALUE OR RETURN TO KEEP: *0<cr>

iSBC-215 (2063H) DRIVE: 2
   TOTAL CYLINDERS: 525T
ENTER NEW VALUE OR RETURN TO KEEP: *0<cr>

iSBC-215 (2063H) DRIVE: 3
   TOTAL CYLINDERS: 525T
ENTER NEW VALUE OR RETURN TO KEEP: *0<cr>
```

Figure 3-7. SIVWIN Initialization Menu For 8-Inch Winchester Drive Showing Response For Changing Drive Characteristics (Sheet 1 of 2)

```
CURRENT DRIVE CHARACTERISTICS FOR RESPONDING CONTROLLERS:

                                                SECTORS BYTES   TOTAL
                          TOTAL   HEADS HEADS   PER     PER     ALTERNATE
CONTROLLER WAKEUP DRIVE   CYLDRS  FIXED RMVBL  TRACK   SECTOR  CYLINDERS
  iSBC-215 2063H    0     525T     5T    0T     23T     512T    11T
  iSBC-215 2063H    1       0T     5T    0T     23T     512T    11T
  iSBC-215 2063H    2       0T     5T    0T     23T     512T    11T
  iSBC-215 2063H    3       0T     5T    0T     23T     512T    11T
DO YOU WANT TO CHANGE THE DRIVE CHARACTERISTICS?(Y / [N]): *<cr>
DRIVE RESPONSE TEST:

 iSBC-215H       DRIVE 0         DRIVE 1         DRIVE 2         DRIVE 3
2063H            RESPONDED       NOT USED        NOT USED        NOT USED

IS THE DRIVE BACKED UP? (Y / [N]: *<cr>
*
```

Figure 3-7. SIVWIN Initialization Menu For 8-Inch Winchester Drive Showing Response For Changing Drive Characteristics (Sheet 2 of 2)

8. The user is asked if the drive(s) to be tested are backed up. A negative response does not allow any destructive tests to user data, to execute. An affirmative answer allows all tests to execute, including those that destroy user data. In the example shown in Figure 3-8, the WSST86 diagnostic has been initialized to allow destructive testing on drive 0 by responding YES to this question. Had more than one drive been installed, the following would have been displayed in place of this question.

```
ARE ANY DRIVES BACKED UP? (Y / [N]): * Y
IS iSBC-215H (2065H) DRIVE 0 BACKED UP? (Y / [N]): * Y
IS iSBC-215H (2065H) DRIVE 1 BACKED UP? (Y / [N]): * <cr>
```

In the above example, the WSST86 diagnostic has been initialized to allow destructive testing on Drive 0 by responding YES; however, it was disallowed for Drive 1 because the default value of NO was entered when asked if it was backed up.

```
SERIES 4 WINCHESTER/SMD SDT, Vx.y
WSST86, Vx.y
COPYRIGHT INTEL CORP. 1980,1983
CURRENT WAKEUP ASSIGNMENTS
   CONTROLLER   WAKEUP
   iSBC-215      2063H
   iSBC-215      2065H
   iSBC-215      2066H
   iSBC-220      2064H
DO YOU WANT TO CHANGE THE DEFAULT WAKEUP ASSIGNMENTS?(Y / [N]): *<cr>
CONTROLLER RESPONSE TEST:

  iSBC-215 ( 2063H ) . . . NO RESPONSE
  iSBC-215 ( 2065H ) . . . RESPONDED
  iSBC-215 ( 2066H ) . . . NO RESPONSE
  iSBC-220 ( 2064H ) . . . NO RESPONSE

"NO RESPONSE" INDICATES THE CONTROLLER IS DEFECTIVE OR NOT INSTALLED.

CURRENT DRIVE CHARACTERISTICS FOR RESPONDING CONTROLLERS:

                                                SECTORS BYTES  TOTAL
                         TOTAL  HEADS HEADS PER     PER    ALTERNATE
CONTROLLER WAKEUP DRIVE CYLDRS FIXED RMVBL TRACK   SECTOR CYLINDERS
  iSBC-215   2065H   0    306T    4T    0T    17T     512T     9T
  iSBC-215   2065H   1    0T      0T    0T    0T      0T       0T
  iSBC-215   2065H   2    0T      0T    0T    0T      0T       0T
  iSBC-215   2065H   3    0T      0T    0T    0T      0T       0T
DO YOU WANT TO CHANGE THE DRIVE CHARACTERISTICS?(Y / [N]): *<cr>
DRIVE RESPONSE TEST:

  iSBC-215H       DRIVE 0        DRIVE 1        DRIVE 2        DRIVE 3
2065H             RESPONDED      NOT USED       NOT USED       NOT USED

IS THE DRIVE BACKED UP? (Y / [N]): *Y<cr>
*
```

Figure 3-8. SIVWIN Initialization Menu That Will Allow Destructive Testing

3.17.2 SIVWIN Test Execution

After initializing the WSST86 diagnostic, perform the following procedure to execute the actual testing. The answers given to questions asked during the initialization procedure causes certain tests to be ignored. For example, Tests C, F and 16 will be ignored in a Series IV single drive system because they are multiple drive tests. Destructive tests, such as Tests 14, 15 and 17 are always initially ignored and can only be executed if the drive under test has been backed up.

1. The level of error messages displayed as the tests execute may be controlled with the DEBUG command. In general, the larger the value of DEBUG, the more information displayed. Table 3-10 lists the information available for different settings of DEBUG. As the DEBUG value is increased, the level of information furnished contains the specified information and also all of the information available with the lesser values. To change the DEBUG value to a setting recommended for troubleshooting, enter the following command:

```
*DEB=3<cr>
```

Table 3-10. SIVWIN DEBUG Levels

DEBUG Value	Information Available
0	Pass/Fail Information Only (Default)
1*	Test Status (see NOTE 1)
2	Encoded Error Messages
3-FFFEH**	English Error Messages
FFFFH	I/O Blocks

* Recommended setting for Burn-in.
** Recommended setting for troubleshooting.

NOTE

1. If DEBUG is set to a value greater than 0, Tests 8, A, 14, 15 and 17 will display status as they execute. This allows the user to see that the test is still executing and that the system has not locked up. The status display format is as follows:

   hxcccc

   where:

   - *h* is the head number (displayed in current base, i.e. hex, decimal, etc.)
   - *x* is either 'V', 'S', 'W', 'R' or 'F' for Verify, Seek, Write, Read or Format respectively.
   - *cccc* is the cylinder number (displayed in current base; i.e. binary (Y), octal (Q), decimal (T), hexadecimal (H) or ASCII (ASC)).

2. If the DEBUG value is greater than 2, Tests 0, 2 and 3 will display the firmware version of the controller under test in the following format:

```
0000H RESET/INITIALIZE TEST
iSBC-215H ( 2063H ) DRIVE 1 ( FIRMWARE VERSION: iSBC x.y )
0000H RESET/INITIALIZE DISK TEST                    "PASSED"
```

2. To execute all recognized tests, enter the following command:

```
*T<cr>
```

3. The system will display the test number, test name and status (i.e.; PASSED, FAILED) as each test executes as shown in Figure 3-9. Those tests that are in the "default ignored condition" will be listed as such when testing begins.

```
000CH *** IGNORED ***
000FH *** IGNORED ***
0014H *** IGNORED ***
0015H *** IGNORED ***
0016H *** IGNORED ***
0017H *** IGNORED ***
0018H *** IGNORED ***
0019H *** IGNORED ***
001AH *** IGNORED ***
001BH *** IGNORED ***
001CH *** IGNORED ***
0000H RESET DISK TEST                              "PASSED"
0001H ROM CHECKSUM TEST                            "PASSED"
0002H RAM WINDOW TEST                              "PASSED"
0003H RAM ADDRESS TEST                             "PASSED"
0004H TRANSFER STATUS TEST                         "PASSED"
0005H BUFFER I/O TEST                              "PASSED"
0006H FORMAT DIAGNOSTICS TRACKS TEST               "PASSED"
0007H MICRO-DIAGNOSTIC                             "PASSED"
0008H VERIFY FORMAT/FORMAT TEST                    "PASSED"
0009H SEEK/VERIFY TEST                             "PASSED"
000AH WORST CASE SEEK TEST                         "PASSED"
000BH WRITE/READ/VER. DIAG. TRACK TEST             "PASSED"
000DH PLATTER/HEAD SELECTION TEST                  "PASSED"
000EH SECTOR SELECTION TEST                        "PASSED"
0010H ALTERNATE TRACK TEST                         "PASSED"
0011H ZERO FILL TEST                               "PASSED"
0012H DATA OVERRUN TEST                            "PASSED"
0013H AUTO-INCREMENT TEST                          "PASSED"
*
```

Figure 3-9. SIVWIN Sample Test Output

4. To execute the utilities that are initially IGNORED, such as Tests 1B and 1C, perform the following steps:

   a. Enter the following command to allow DETMON to recognize the tests:

```
*REC 1B, 1C
```

   b. To excute Test 1B, enter the following command:

```
*T 1B
```

c. The user is queried to determine which function of the test is to be executed. An asterisk indicates that the system is waiting for user input. A sample output follows:

```
DISPLAY/EDIT DEFECT LIST: 0. RETURN TO DETMON
 1. READ DEFECT LIST FROM DISK : 3. ADD TO DEFECT LIST IN RAM
 2. DISPLAY DEFECT LIST IN RAM : 4. DELETE FROM DEFECT LIST IN RAM
                5. STORE DEFECT LIST IN RAM ONTO DISK
                6. CLEAR DEFECT LIST IN RAM
ENTER A NUMBER BETWEEN 0 AND 6: *2
CYLINDER HEAD
0066       02
0067       03
009C       02
00AE       02
013B       02
DISPLAY/EDIT DEFECT LIST: 0. RETURN TO DETMON
 1. READ DEFECT LIST FROM DISK : 3. ADD TO DEFECT LIST IN RAM
 2. DISPLAY DEFECT LIST IN RAM : 4. DELETE FROM DEFECT LIST IN RAM
                5. STORE DEFECT LIST IN RAM ONTO DISK
                6. CLEAR DEFECT LIST IN RAM
ENTER A NUMBER BETWEEN 0 AND 6: *0
001BH DISPLAY/EDIT DEFECTIVE TEST UTIL                    "PASSED"
*
```

d. To execute Test 1C, enter the following command:

```
*T 1C
```

e. The user is queried to determine which function of the test is to be executed (refer to Paragraph 3.17.6 for information on error logs). An asterisk indicates that the system is waiting for user input. A sample output follows:

```
001CH DISPLAY/CLEAR ERROR LOG UTILITY
DISPLAY/CLEAR ERROR LOG MENU :     0. RETURN TO DETMON
 1. DISPLAY ALL LOGS         :     6. CLEAR ALL LOGS
 2. DISPLAY NO RESPONSE LOG  :     7. CLEAR NO RESPONSE LOG
 3. DISPLAY HARD ERROR LOG   :     8. CLEAR HARD ERROR LOG
 4. DISPLAY EXCEPTION LOG    :     9. CLEAR EXCEPTION LOG
 5. DISPLAY SOFT ERROR LOG   :    10. CLEAR SOFT ERROR LOG
ENTER A NUMBER BETWEEN 0 AND 10: *4

EXCEPTION ERROR:
SBC WAKEUP UNIT CYLDR HD OP$STAT FUNC ERRCOD TEST TRAIL ERRCNT
215 2065H    0H   0H    0H 1H      3H   14     14H  1H    1H
OPERATION STATUS (OP$STAT) EXPLANATION:
  OPERATION COMPLETE
  NO ERRORS DETECTED
READ SECTOR ID FUNCTION (FUNC)
ERROR CODE (ERRCOD) EXPLANATION:
TEST NEEDS UNIT BACKED UP TO EXECUTE
PRESS RETURN TO CONTINUE*<cr>
DISPLAY/CLEAR ERROR LOG MENU :     0. RETURN TO DETMON
 1. DISPLAY ALL LOGS         :     6. CLEAR ALL LOGS
 2. DISPLAY NO RESPONSE LOG  :     7. CLEAR NO RESPONSE LOG
 3. DISPLAY HARD ERROR LOG   :     8. CLEAR HARD ERROR LOG
 4. DISPLAY EXCEPTION LOG    :     9. CLEAR EXCEPTION LOG
 5. DISPLAY SOFT ERROR LOG   :    10. CLEAR SOFT ERROR LOG
```

```
ENTER A NUMBER BETWEEN 0 AND 10: *0
001CH DISPLAY/CLEAR ERROR LOG UTILITY                    "PASSED"
```

5. To execute Tests 14, 15 and 17, the drive under test must first be backed up. The following procedure will allow execution of these tests.

Tests 14, 15 and 17 will destroy all user data on the drive(s) under test. Ensure that the customer's data has been backed-up before executing any of these tests.

a. Re-initialize the WSST86 diagnostic by entering the RESET command. Answer the question "IS THIS DRIVE BACKED UP?" with Y as shown in Figure 3-8. Tests 14, 15 and 17 will automatically be recognized.

b. Set the value of DEBUG to 3H to display the test status and any error messages.

```
*DEB=3H
```

c. Enter the following command to start test execution:

```
*T 14,15,17
```

d. The terminal will display the following information as the tests execute:

```
0014H WRITE ALL/READ/COMPARE TEST
hxcccc
0014H WRITE ALL/READ/COMPARE TEST                        "PASSED"
0015H RANDOM WRITE/READ/VERIFY TEST
hxcccc
0015H RANDOM WRITE/READ/VERIFY TEST                      "PASSED"
0017H FORMAT UTILITY
hxcccc
0017H FORMAT UTILITY                                     "PASSED"
*
```

e. To ignore the destructive tests, enter the following command:

```
*IGN 14,15,17
```

3.17.3 SIVWIN Test Execution Times

Approximate execution times for the individual tests for systems equipped with the 35 MB drive and/or the 12 MB drive are shown in Table 3-11.

Table 3-11. SIVWIN Test Execution Times

Test Number	35 MB Drive	12 MB Drive
0	5 seconds	7 seconds
1	1 second	1 second
2	1 minute	1 min., 12 sec.
3	5 seconds	8 seconds

Table 3-11. SIVWIN Test Execution Times (Cont'd)

Test Number	35 MB Drive	12 MB Drive
4	1 second	1 second
5	1 second	1 second
6	4 seconds	5 seconds
7	1 second	7 seconds
8	6 minutes	3 min., 14 sec.
9	1 second	1 second
A	15 minutes	12 min., 27 sec.
B	1 second	1 second
C	2 seconds	NA
D	1 second	7 seconds
E	3 seconds	9 seconds
F	1 second	NA
10	1 second	1 second
11	23 seconds	20 seconds
12	2 seconds	5 seconds
13	1 second	5 seconds
14	15 minutes	8 minutes
15	2 minutes	2 min., 15 sec.
16	1 second	NA
17	5 minutes	2 minutes

3.17.4 SIVWIN Test Variables

TMON provides user interface with up to 16 'V' variables whose content can be displayed or altered as illustrated in Figure 3-10.

The 'V' variables are used as follows:

NOTE

If the RESET command is executed, all 'V' Variable will be reset to their default values.

V(0) indicates controller type under test. It must equal either 215H or 220H.

V(1) indicates the Wakeup Port address of the controller under test.

V(2) indicates the unit number under test. The unit number is a byte that will consist of two parts. The low nibble contains the drive number under test and the high nibble contains volume under test (fixed [0] or removable [1]). Thus, this number must equal 0, 1, 2, 3, 10H, 11H, 12H or 13H.

NOTE

V(0) through V(2) are filled in during initialization. When multiple drives are being tested, Test 16 (Select Next Drive Under Test) increments these 'V' variables to test the next drive. This allows the user to determine which controller/ drive is currently under test. It also permits the user to select an individual controller and drive by changing the 'V' variables.

V(3) indicates the cylinder(s) to be exercised by Test 14. If equal to 0FFFFH (default), all cylinders will be tested.

V(4) indicates the head(s) to be exercised by Test 14. If equal to 0FFFFH (default), all heads will be tested. For example, V(3)=0 restricts Test 14, Write All/Read/Compare Test, to cylinder 0 of each head. Likewise, V(4)=2 restricts Test 14 to head 2 of each cylinder.

V(5) is the test pattern for Test 14, the Write All/Read/Compare Test. (Default = 6DB6H.)

V(6) determines the way Test 14, the Write All/Read/Compare Test, will perform. If equal to 0 (default), the test writes all sectors before reading any sector. If not equal to 0, each sector is read immediately after the write.

V(7) thru V(9) are not used.

V(A) indicates if alternates are to be assigned for defective tracks. When equal to zero (default), alternates are not assigned. When not equal to zero, alternates are assigned.

V(B) indicates if test status information is to be displayed. When set to zero (default), tests that execute for an extended length of time will periodically display status to indicate that the test is still in progress. When not set to zero, the test will display an ASCII carriage return (without linefeed). This permits the execution of tests for many hours with the printer being used to catch errors only. The ASCII carriage return is sent to allow the TMON Control+C key to function properly and thus give the user a chance to interrupt the test. It should also be understood that this variable will not influence TMON's DEBUG or ERRONLY flags.

V(C) indicates the number of retries allowed before an error is considered nonrecoverable. Both automatic retries from the controller and host initiated retries will be included in this number. In other words, the retry count is an accumulated total of both automatic retries from the controller and the number of retries initiated from the host. The default setting of this variable is 10.

V(D) indicates if tracks listed in the Defective Track List are to be tested. When set to zero (default), known defective tracks are not tested or exercised in any way. When not set to zero, all tracks are tested.

V(E) indicates if error log entries are to be echoed to the console. If set to 0 (default), all entries placed into the error log cause the error log entry to echo to the console. If not set to 0, entries placed into the error log do not echo to the console.

V(F) is not used.

1. To display the contents of all variables execute the following command:

```
*V(0),LEN 10H<cr>
V(00)=0215
V(01)=0100
V(02)=0000
V(03)=FFFF
V(04)=FFFF
V(05)=6DB6
V(06)=0000
V(07)=0000
V(08)=0000
V(09)=0000
V(0A)=0000
V(0B)=0000
V(0C)=000A
V(0D)=0000
V(0E)=0000
V(0F)=0000
*
```

2. To display the contents of one variable, execute the following command:

```
*V(05)<cr>
V(05)=6DB6
*
```

3. To change the contents of a variable and verify that the change was made, execute the following commands:

```
*V(05)=5A5A<cr>
*V(05)<cr>
V(05)=5A5A
*
```

Figure 3-10. SIVWIN Variable Manipulation

3.17.5 SIVWIN Test Descriptions

Table 3-12 describes the function of each individual test contained in the SIVWIN test suite.

Table 3-12. Series IV, SIVWIN Test Descriptions

Test No.	Test Name	Test Description
0000H	Reset	Resets the controller and initializes the Winchester Disk controller.
0001H	ROM Checksum	Checks the controller ROM by running the on-board ROM checksum test.
0002H	RAM Window	Checks 2KB bytes of controller onboard RAM by walking ones and then zeros through memory.
0003H	RAM Address	Verifies RAM address lines.
0004H	Transfer Status	Checks communication lines between controller and drive by enabling the transfer error status function.

Table 3-12. Series IV, SIVWIN Test Descriptions (Cont'd)

Test No.	Test Name	Test Description
0005H	Buffer I/O	Verifies the transfer of data between the controller and CPIO memory.
0006H	Format Diagnostic Track	Formats and verifies one diagnostic track on the Winchester drive. **NOTE** Test 7 will fail unless the diagnostic track (last cylinder, head 0) has been formatted via Test 6.
0007H	Micro-Diagnostic	Executes on-board ROM-based diagnostics to verify fundamental controller-drive functions.
0008H	Verify Format/ Format	Verifies format; if the format does not verify, formatting will be performed by Test 17 if the drive is backed up. Before formatting, a Warning message is displayed. **NOTE** Test 9 will fail unless both the diagnostic track and track 0 are formatted via Tests 6 and 17.
0009H	Seek/Verify	Checks seek and verify functions by reading the first sector on the first and last tracks of each surface.
000AH	Worst Case Seek	Checks seek and verify functions by executing a worst case seek sequence. **NOTE** Tests B and C will fail unless the diagnostic track has been formatted via Test 6.
000BH	Write/Read/Verify Diagnostic Track	Verifies write and read functions by writing/reading the diagnostic tracks and verifying that data read matches the data written.
*000CH	Drive Selection	Verifies controller access of each drive when more than one drive is operating.
000DH	Platter/Head Selection	Verifies that each platter and head can be accessed individually. **NOTE** Test E will fail unless the diagnostic track has been formatted via Test 6.
000EH	Sector Selection	Verifies that each sector of a diagnostic track can be written, read and verified.
*000FH	Overlap Seek	Verifies correct controller overlap control on more than one disk drive.
0010H	Alternate Track	Checks alternate track capability by assigning and accessing an alternate diagnostic track.
0011H	Zero Fill	Verifies controller ability to fill partial sectors with zeroes on a diagnostic track.
0012H	Data Overrun	Reads the area immediately following partial sectors on a diagnostic track to determine if extra (overrun) data is being written.
0013H	Auto-Increment	Verifies controller ability to increment to the next sector automatically. **CAUTION** Tests 14 and 15 will destroy the user data on the drive(s) under test. Therefore, the default condition is always "IGNORED". As an added safety feature, the test can only be executed on drives that are backed up.

Table 3-12. Series IV, SIVWIN Test Descriptions (Cont'd)

Test No.	Test Name	Test Description
0014H	Write All/Read/ Compare	Writes the worst case data pattern (6DB6H) to all drive sectors and verifies the pattern. Writes the complement pattern (9249H) and verifies that pattern. The 6DB6H pattern that is written is extracted from V(5). Thus, the pattern can be changed by changing the value in V(5). See 'V' variable definitions in Paragraph 3.17.4. This test can also be forced to perform a read after each write instead of writing all data first and then reading it back by setting V (6) to a non-zero value. The default value for V (6) will be 0. Additionally, V (3) and V (4) can restrict testing to a particular cylinder and/or head rather than the full drive.
0015H	Random Write/ Read/Compare	Writes a random data pattern to all drive sectors, then reads and compares the data with the original patterns.
0016H	Select Next Drive Under Test	Increments V (0) thru (2) to point at the next drive under test. **CAUTION** Test 17 destroys the user data on the drive(s) under test. Therefore, the default condition is always "IGNORED". As an added safety feature, the test can only be executed on drives that are backed up.
**0017H	Format Utility	This utility formats the drive under test. Additionally, known defective tracks are not assigned alternates unless the value in V(A) has been changed to a number other than 0 (see Paragraph 3.17.4 for more information on 'V' variables).
0018H,0019H	Spare	
**001AH	Unload Head For Shut-down Utility	Position the head over the diagnostic cylinder.
**001BH	Display/Edit Defective Track List Utility	Permits the user to see, add, change or delete entries in the Defective Track List on the last cylinder minus 1.
**001CH	Display/Clear Error Log Utility	Permits the user to view or clear the Error Log

* Ignored unless more than one drive is present and selected for testing.

** Not a test; but a tool that allows user interface.

3.17.6 Error Messages

Error messages fall into one of four groups depending upon their type; the groups are NO RESPONSE ERROR, HARD ERROR, SOFT ERROR or EXCEPTION ERROR. A No Response Error message is displayed when the controller and/or drive does not respond within its given worst case time. When the controller reports that an error condition occurred and could not be recovered after retrying the designated number of times, a Hard Error message is displayed. A Soft Error message is displayed when the controller reports that an error condition has occurred but that it has recovered. An Exception Error message occurs when the controller/drive responds and no errors are reported but something obviously is wrong (e.g.; data read differs from data written).

All but Soft Errors cause a test to fail. An exception to this is when an Exception Error is generated as a result of not being able to read the Defective Track

List. The Soft Errors incurred during testing will not cause a test to fail; however, excessive Soft Errors could indicate an impending nonrecoverable error condition.

The following paragraphs describe the four types of error messages in greater detail.

3.17.6.1 No Response Error Messages

A typical No Response Error Message has the following format:

```
NO RESPONSE ERROR: iSBC-215 (2065H) COUNT = 1T
  DRIVE FAILURE COUNT
  0       1       2       3       TEST FUNC ST$SEMA OP$STAT BUSY$1
  1       0       0       0       8H   8H   0H      0H      FFH
```

In the preceding example, a No Response Error occurred while executing Test 8 on drive 0, which was attached to the iSBC-215 board assigned to Wakeup Port 2065H. Additional information about specific fields within the controller's Channel Control Block and I/O Parameter Block is listed under the following headings:

- FUNC (function)
- ST$SEMA (status semaphore)
- OP$STAT (operation status)
- BUSY$1 (busy 1 flag)

For a detailed explanation of what these fields indicate, refer to the respective *iSBC 215 Winchester Disk Controller Hardware Reference Manual.*

3.17.6.2 Hard Error Messages

The format of a typical Hard Error Message is as follows:

```
HARD ERROR:
SBC WAKEUP UNIT CYLDR HD OP$STAT FUNC ERRSTAT TEST TRAIL ERRCNT
215 2065H  0H   0H    0H C1H     8H   400H    8H   1H    1H
OPERATION STATUS (OP$STATUS) EXPLANATION:
  OPERATION COMPLETE
  HARD ERROR
INITIATE TRACK SEEK FUNCTION (FUNC)
HARD ERROR STATUS (ERRSTAT) EXPLANATION:
  SELECTED UNIT NOT READY
```

In the preceding example, a Hard Error occurred on the iSBC-215 at Wakeup Port 2065H, unit 0, cylinder 0, head 0 while executing Test 8. The error description information is contained in OP$STAT (operation status), FUNC (function), and ERRSTAT (error status) which are fields within the I/O Parameter Block of the controller. The information contained within these fields is explained in lines 4 through 9 of the display. As shown, the operation completed with a Hard Error per the OP$STAT, the FUNC was an Initiate Track Seek function, and the ERRSTAT indicates that the selected unit was not ready. Further, the error occurred during trial 1 of test 8 and the error count (ERRCNT) is one, indicating that this is the first time this error occurred.

3.17.6.3 Soft Error Messages

A typical Soft Error message looks identical to a Hard Error message except that the heading reads 'SOFT ERROR', the ERRSTAT describes the Soft Error status, and the accumulated number of retries is displayed.

3.17.6.4 Exception Error Messages

The format of a typical Exception Error message is as follows:

```
EXCEPTION ERROR:
SBC WAKEUP UNIT CYLDR HD OP$STAT FUNC ERRCOD TEST TRAIL ERRCNT
215 2065H  0H   0H    0H 1H      1H   14     8H   1H    1H
OPERATION STATUS (OP$STAT) EXPLANATION:
  OPERATION COMPLETE
  NO ERRORS DETECTED
TRANSFER STATUS FUNCTION (FUNC)
ERROR CODE (ERRCOD) EXPLANATION:
  TEST NEEDS UNIT BACKED UP TO EXECUTE
```

In the preceding example, the existence of an exceptional condition has prevented the test from passing. In this case, the failure occurred because an incorrectly formatted track could not be re-formatted because the unit had not been backed up. The additional information shown is identical to a Hard Error display.

3.17.7 SIVWIN Error Logs

NOTE

Error Logs can be read or cleared by executing Test 1C.

A separate error log is maintained in RAM for each of the four types of errors that may occur; i.e. No Response Log, Hard Error Log, Soft Error Log, and Exception Log. The No Response Log contains information about errors that occur because the controller and/or drive would not respond within its given worst case time. The Hard Error Log contains information about hard errors; errors that are non-recoverable even after retries. The soft error log contains information about soft errors; errors that are recoverable. The Exception Log contains information about errors that are not reported as errors by the controller and/or drive.

3.17.7.1 No Response Log

This log contains the following information:

- unit number that indicates controller and drive that incurred the error
- controller response failure count
- drive response failure count

3.17.7.2 Hard Error Log

This log has 20 individual entries containing the following information regarding the hard error occurrence:

- unit, cylinder, and head numbers

- operational status
- function code
- error status
- test number
- retry count
- test trial
- error count

The unit, cylinder and head numbers identify the particular hardware involved including the controller, fixed or removable platters within the drive, and the head and cylinder numbers. The operational status indicates the status of the operation. The function code indicates what function was being performed when the error occurred, i.e. Read, Write, etc. The actual description of the hard error is found in the error status. Additional information relating to the operational status, function codes or error status may be found in the respective *iSBC 215 Winchester Disk Controller Hardware Reference Manual.*

The test executing when the error occurred is indicated by the test number. The retry count contains the number of attempts that were made to recover from an error. The test trial indicates which pass of the test the error occurred, and the error count indicates the number of times the error occurred.

3.17.7.3 Soft Error Log

This log consists of 20 individual entries in the same format as found in the Hard Error Log with exception of the error status and retry count. Refer to the respective *iSBC 215 Winchester Disk Controller Hardware Reference Manual* for more detailed information on the error status for soft errors.

3.17.7.4 Exception Log

This log consists of 20 individual entries that are identical to those in the Hard Error Log except that the error status is replaced by an error code or exception code. Exception codes are listed in Table 3-13.

Table 3-13. Series IV, SIVWIN Exception Codes

Code	Definition
1	**'TRANSFER COUNT DIFFERENT THAN EXPECTED'** — For example, 30 bytes of data were requested but the transfer count field in the I/O Parameter Block indicates that only 20 bytes were transferred.
2	**'MORE RETRIES THAN ALLOWED'** — Indicates that more soft errors happened than allowed by V(C), the retry count.
3	**'ACTUAL CYLINDER OR HEAD NO. DIFFERENT THAN EXPECTED'** — For example, a Seek was performed to an expected cylinder and head. When a Read Sector ID on the track is performed, the actual head and sector are different than what was expected.
4	**'ACTUAL SECTOR SIZE DIFFERENT THAN EXPECTED'** — Indicates that the actual sector size is different than indicated by drive characteristics that were defined during initialization.

Table 3-13. Series IV, SIVWIN Exception Codes (Cont'd)

Code	Definition
5	**'TRACK FORMAT TYPE DIFFERENT THAN EXPECTED'** — Indicates that the format type read is different than expected. For example, an assigned alternate track was found in an area that should only have data tracks or defective tracks that point to assigned alternate tracks.
6	**'PATTERN FORMATTED DIFFERENT THAN PATTERN READ'** — Indicates that the pattern read from a track does not match the pattern that was placed on the track when it was formatted.
7	**'DEFECT LIST SHOWS ALL DIAGNOSTIC TRACKS DEFECTIVE'** — Indicates that all the diagnostic tracks are listed in the Defective Track List when at least one track is needed to execute the test.
8	**'TOO MANY DEFECTIVE DIAGNOSTIC TRACKS PER DEFECT LIST'** — Indicates that all suitable diagnostic tracks are listed in the Defective Track List. For example, one of the tests requires at least two diagnostic tracks to execute but the Defective Tracks List indicates that all but one diagnostic track is defective.
9	**'PATTERN WRITTEN DIFFERENT THAN PATTERN READ'** — Indicates that the data pattern read differs from the data pattern written.
10	**'CANNOT DO TEST WITH CURRENT DEFECT LIST'** — Indicates that an illegal combination of tracks on the defective cylinder are listed in the Defective Track List. For example, the Defective Track List cannot list both diagnostic tracks 0 and 1 nor can it list the last and next to last diagnostic tracks.
11	**'ERROR DETECTED DURING OVERLAP SEEK'** — Indicates than an error was detected while executing an Overlapped Seek Operation.
12	**'PATTERN READ IS NOT PROPERLY FILLED WITH ZEROS'** — Indicates data read is not filled with zeros to match the requested transfer count.
13	**'MORE DATA TRANSFERRED THAN REQUESTED'** — Indicates that more data bytes were transferred than were requested.
14	**'TEST NEEDS UNIT BACKED UP TO EXECUTE'** — Indicates that user data must be altered in order to execute the test but the drive is not backed up according to the responses given to the question(s) asked during initialization.
15	**'TRACK 0 HAS A FAILURE THAT IS NOT ALLOWED'** — Indicates that an error has been detected on track 0. Failures are not allowed on track 0 as it is guaranteed to work at all times.
16	**'RAN OUT OF ALTERNATE TRACKS TO ASSIGN'** — Indicates that all of tracks allocated by the number of alternate cylinders have been used and at least one more alternate track is needed.
17	**'DEFECT LIST IS NOT VALID'** — Indicates that the Defective Track List is not valid. This can be caused by being unable to read any data on the appropriate track that contains the list or because the valid byte read from the list does not equal ABCDH.
18	**'TWO OR MORE DRIVES PER CONTROLLER NEEDED FOR TEST TO EXECUTE'** — Indicates that more than one drive is needed to execute the specified test. These drives must be attached to the same controller and selected for testing during initialization.
19	**'AN INTERRUPT WAS EXPECTED BUT NOT RECEIVED'** — Indicates that the controller did not generate the required interrupt.
20	**'STATUS SEMAPHORE NEVER INDICATED STATUS TO BE POSTED AS EXPECTED'** — Indicates that the controller never changed the status semaphore as expected to signal that status is posted.
21	**'HARD ERROR DETECTED WITH INIT FUNCTION'** — Indicates that a hard error was detected while the controller was initializing. This error can cause unpredictable results in other tests.
22	**'CONTROLLER DOES NOT RESPOND FROM A RESET'** — Indicates that the controller did not respond from a reset. The most likely cause of this error code is a 'dead' controller board although faulty system RAM can also cause the failure.

3.18 SIVCOM Standalone Supplemental Test

When initiated, the SIVCOM supplemental test suite verifies the operation of the optional iSBC-550 Ethernet Communications board set. The following paragraphs familiarize the user with the actual operation of the SIVCOM test suite in the Single-Station Test Mode. To run the Series IV in the Two-Station Test Mode, refer to the *NDS-II Field Service Manual* (P/N 133711).

3.18.1 Initiating SIVCOM

The following procedures offer step-by-step instructions for initializing and running the SIVCOM test suite in the single station test mode:

1. Verify that the Intellink, Ethernet Cable and iSBC-550 Ethernet Communications Board set (option) have been installed and power has been applied.
2. Verify that the Configuration Switches are set to boot from disk drive #0 then insert a copy of the Series IV Supplemental Level Diagnostic, Order No. 134444, into floppy disk drive #0, close the latch and press the "RESET" switch (refer to Section 3.13).
3. Type "Z" and the test name "SIVCOM" into the system.
4. Define the test suite parameters and start the test procedure. (see Appendix A for TMON commands).

NOTE

Operator entries are shown in reverse video and the <cr> indicates pressing the keyboard RETURN key.

Example of initiating SIVCOM

```
Series IV Diagnostic Monitor, x.y
>ZSIVCOM<cr>
File SIVCOM loaded
iSBC-550 Ethernet Controller 8086-Based Diagnostic, Vx.y
Answer ''Yes'' or ''No'' to Initialize Test Configuration
```

Answer the Initialization Menu Questions As Follows:

```
                    Execute Memory Tests Only? NO<cr>
          Connected to Transceiver (or Equivalent)? YES<cr>
                    Testing Only One Station? YES<cr>
Controller at Port xxH--Ethernet Address 00AA 00XX XXXXH
                         Firmware Diagnostic     "PASSED"
*
```

NOTE

Ethernet address 00AA 00*XX XXXX*H should be recorded in the NDS-II Ethernet Log given in the *NDS-II Installation Manual.*

To run tests 0000H and 0002H through 001DH, type:

```
*T<cr>
```

```
0001H *** IGNORED ***
001EH *** IGNORED ***
001FH *** IGNORED ***
0020H *** IGNORED ***
0021H *** IGNORED ***
0022H *** IGNORED ***
0023H *** IGNORED ***
0024H *** IGNORED ***
0025H *** IGNORED ***
0026H *** IGNORED ***
0027H *** IGNORED ***
0028H *** IGNORED ***
0029H *** IGNORED ***
0000H Processor Wake-up Ports
0000H Processor Wake-up Ports                    "PASSED"
0002H Processor Hardware Reset
0002H Processor Hardware Reset                   "PASSED"
0003H Processor Multibus Data Ripple
0003H Processor Multibus Data Ripple             "PASSED"
0004H Processor Multibus Address Ripple
0004H Processor Multibus Address Ripple          "PASSED"
0005H Processor Firmware Verify
0005H Processor Firmware Verify                  "PASSED"
0006H Processor/Host Bus Arbitration
0006H Processor/Host Bus Arbitration             "PASSED"
0007H Processor DRAM Data Ripple
0007H Processor DRAM Data Ripple                 "PASSED"
0008H Processor 8202 DRAM Bank Select
0008H Processor 8202 DRAM Bank Select            "PASSED"
0009H Processor 8202 DRAM Refresh
0009H Processor 8202 DRAM Refresh                "PASSED"
000AH Processor DRAM March Test
000AH Processor DRAM March Test                  "PASSED"
000BH Processor SRAM Data Ripple
000BH Processor SRAM Data Ripple                 "PASSED"
000CH Processor SRAM March Test
000CH Processor SRAM March Test                  "PASSED"
000DH Processor SYS/LOC Memory Access
000DH Processor SYS/LOC Memory Access            "PASSED"
000EH Processor 8255A
000EH Processor 8255A                            "PASSED"
000FH Processor 8253
000FH Processor 8253                             "PASSED"
0010H Processor 8237
0010H Processor 8237                             "PASSED"
0011H Processor 8237/SRAM Addressing
0011H Processor 8237/SRAM Addressing             "PASSED"
0012H Processor 88/8237 SRAM Contention
0012H Processor 88/8237 SRAM Contention          "PASSED"
0013H Processor 8259/RCV Request Latch
0013H Processor 8259/RCV Request Latch           "PASSED"
0014H SerDes Transmit Enable
0014H SerDes Transmit Enable                     "PASSED"
0015H SerDes Transmit Sequencing
0015H SerDes Transmit Sequencing                 "PASSED"
0016H SerDes Internal Carrier Sense
0016H SerDes Internal Carrier Sense              "PASSED"
0017H SerDes Ethernet Address PROM
0017H SerDes Ethernet Address PROM               "PASSED"
```

```
0018H SerDes Promiscuous Receive
0018H SerDes Promiscuous Receive                    "PASSED"
0019H SerDes Non-Promiscuous Receive
0019H SerDes Non-Promiscuous Receive                "PASSED"
001AH SerDes Transmit Long Packet
001AH SerDes Transmit Long Packet                   "PASSED"
001BH SerDes Interpacket Spacing
001BH SerDes Interpacket Spacing                    "PASSED"
001CH SerDes Receive CRC Circuit
001CH SerDes Receive CRC Circuit                    "PASSED"
001DH SerDes External Transmit Loopback
001DH SerDes External Transmit Loopback             "PASSED"
```

NOTE

To exit TMON and return to the diagnostic monitor so that another test suite may be loaded and exercised or testing abandoned altogether, type:

```
*EXIT<cr>
```

3.18.2 SIVCOM Test Descriptions

Table 3-14 identifies each SIVCOM test and describes its operation.

Table 3-14. Series IV, SIVCOM Test Descriptions

Test No.	Test Name	Test Description
0000H	Processor Wake-up Ports	Verifies that processor board responds to wakeup command from host.
*0001H	Processor Multibus Interrupt	Verifies ability of the processor board to generate level 6 (INT6/) system interrupt. Host responds to interrupt by resetting processor board interrupt latch.
0002H	Processor Hardware Reset	Verifies that interrupt latch, Multibus I/O latch, 8237 DMA Controller, and 8255A Programmable Peripheral Interface are reset by Select Reset (SEL RESET) command.
0003H	Processor Multibus Data Ripple	Verifies integrity of the Multibus data drivers.
0004H	Processor Multibus Address Ripple	Verifies ability to access system memory.
0005H	Processor Firmware Verify	Verifies integrity of 8Kbytes of ROM by executing a checksum test.
0006H	Processor/Host Bus Arbitration	Verifies ability to arbitrate, gain control, and release control of the Multibus interface (system bus).
0007H	Processor DRAM Data Ripple	Verifies ability to read/write its 16KB Dynamic RAM Memory.
0008H	Processor 8202A DRAM Bank Select	Verifies ability of 8202A Dynamic RAM Controller to differentiate between DRAM addresses and Multibus I/O port addresses.
0009H	Processor 8202A DRAM Refresh	Verifies ability of 8202A to DRAM refresh 16KB Dynamic RAM Memory.
000AH	Processor DRAM March	Tests all 16KB of Dynamic RAM Memory by executing standard march algorithm.
000BH	Processor SRAM Data Ripple	Verifies integrity of DMA bus data lines by writing to and reading from Static RAM Memory.

Table 3-14. Series IV, SIVCOM Test Descriptions (Cont'd)

Test No.	Test Name	Test Description
000CH	Processor SRAM March	Tests all 8KB of Static RAM Memory by executing standard march algorithm.
000DH	Processor SYS/LOC	Verifies ability of processor board to access lower 2KB (00000007FFH) in on-board DRAM and in system RAM.
000EH	Processor 8255A	Verifies ability of 8255A Programmable Peripheral Interface to latch Port B and Port C data.
000FH	Processor 8253	Verifies ability of all three 8253 Programmable Interval Timer counters to count down and to interrupt the 8088 CPU on reaching terminal count; also verifies "on-the-fly" count values while waiting for terminal count.
0010H	Processor 8237	Verifies ability of all four 8237 DMA Controller channels to (1) read/write Base and Current Address registers, (2) read/write Base and Current Word Count registers, (3) increment/decrement Current Address register, (4) increment Current Word Count register, and (5) autoinitialize Current Address and Word Count registers.
0011H	Processor 8237/SRAM Addressing	Verifies ability of 8237 DMA Controller to access all 8KB of SRAM memory.
0012H	Processor 88/8237 SRAM Contention	Verifies ability of 8088 CPU and 8237 DMA Controller to resolve arbitration of DMA bus and to access SRAM memory.
0013H	Processor 8259/RCV Request Latch	Verifies ability of the three DMA receive channels and one transmit channel to generate interrupt requests via the 8259A Programmable Interrupt Controller. SerDes board is cleared following each interrupt.
0014H	SerDes Transmit Enables	Verifies that Transmit Start (TXSRT) command initiates SerDes board transmit startup sequence and that SerDes board sets Enable Transmit Data (ENABLE TXD) status bit.
0015H	SerDes Transmit Sequencing	Verifies that the SerDes board clears Enable Transmit Data (ENABLE TXD) status bit after transmit shutdown.
0016H	SerDes Internal Carrier Sense	In both the Read Address and Verify SerDes modes, verifies that SerDes board generates Carrier Sense (CS) Signal.
0017H	SerDes Ethernet Address PROM	Verifies integrity of SerDes board Address PROM.
0018H	SerDes Promiscuous Receive	Verifies ability of SerDes board to receive broadcast and selfaddressed packets that contain good CRC data when SerDes board Promiscuous Receive bit is set.
0019H	SerDes Non-	In Verify SerDes mode, with Promiscuous Receive control bit cleared, verifies ability of SerDes board to (1) receive broadcast packets, (2) receive self-addressed packets, and (3) reject all other packets.
001AH	SerDes Transmit	Verifies that SerDes board sets Transmit Time Out (TXTO) status bit when packet exceeds maximum length. Also verifies that SerDes board does not set TXTO status bit when maximum length packet is transmitted.
001BH	SerDes Interpacket	In Verify SerDes modes, verifies that SerDes board enforces interpacket gap requirement.

Table 3-14. Series IV, SIVCOM Test Descriptions (Cont'd)

Test No.	Test Name	Test Description
001CH	SerDes Receive CRC	In Verify SerDes mode, verifies ability of SerDes board to transmit and receive data packets that contain bad CRC data and report CRC errors to processor board.
001DH	SerDes External Receive Loopback	Demonstrates send and receive capabilities by transmitting two self-addressed packets that contain random data via an external loopback path provided by the Intellink chassis or a transceiver.

3.18.3 SIVCOM Execution Times

The approximate execution times of the SIVCOM Supplemental individual or groups of tests are listed in Table 3-15.

Table 3-15. Series IV, SIVCOM Test Execution Times

Test Number	Execution Time
0	15 seconds
2	15 seconds
3 - 5	2 seconds
6	4 seconds
7 - 12	2 seconds
13	6 seconds
14 - 19	1 second
1A	8 seconds
1B	1 second
1C	45 seconds
1D	1 second

3.18.4 SIVCOM Error Messages

Error messages for the SIVCOM test suite typically display the failing test number and a descriptive error message. The failing test number identifies a faulty subassembly. Note that network failures may be due to a faulty communication controller in the NRM or a workstation, faulty Ethernet cables, a faulty Intellink chassis, tranceivers, or coaxial cables. Failing test numbers, related NRM subassemblies, and network components are as follows:

Test Number	Subassembly
0 to 13	SIV: iSBC 550 Processor
14 to 1C	SIV: iSBC 550 SerDes
1D	SIV: iSBC 550 SerDes Board
	Network: Intellink, Transceivers or Ethernet Cable

3.18.5 SIVCOM Two-Station and Network Tests

Network test mode may be used to isolate a network failure to a specific communications path quickly (i.e., the Ethernet path to one workstation is bad while

the paths to the other workstations are good). Two-station test mode may be used to test the full functionality of a suspect Ethernet path. Swapping cables between connectors at the Intellink chassis can help isolate bad Intellink channels. One-station test mode may be used to verify that a particular NRM or workstation controller is malfunctioning. To run two-station and/or network tests, refer to the *NDS-II NRM Field Service Manual* (P/N 133711).

3.19 SIV740 Test Execution

The SIV740 test suite verifies proper operation of the Model 740 Hard Disk Controller boards and the disk drive(s). The diagnostic test is divided into three test sequences; 740 controller self tests, the drive tests, and the error detection tests.

3.19.1 SIV740 Test Execution

All TMON commands may be used with the SIV740 test suite. Appendix A provides command descriptions, syntax, and example entries for TMON commands. The user may also use utility and test subroutines to execute specific drive functions. These utility and test subroutines are described in the *Model 740/743 Hard Disk System Test Field Service Manual.* Below are step-by-step instructions for executing the drive test sequence of the SIV740 test suite:

1. Verify that the Configuration Switches are set to boot from disk drive #0 then insert a copy of the Series IV Supplemental Level Diagnostic, Order No. 134444, into disk drive #0, close the latch and press the "RESET" switch (refer to Section 3.15).
2. Type "Z" and the test name "SIV740" into the system.
3. Define test suite parameters and start the test procedure. (see Appendix A for TMON commands).

NOTE

Operator entries are shown in `reverse video` and the `<cr>` indicates pressing the keyboard RETURN key.

Check that the 740 Hard Disk "READY" (up to speed) indicator is lit before proceeding with the SIV740 Tests.

Example of initiating SIV740

```
Series IV Diagnostic Monitor, x.y
>ZSIV740<cr>
File SIV740 loaded (after approx. 35 seconds)
SIV 740 TEST x.y
enter platter id's:*
```

NOTE

The SIV740 test suite is now loaded into the system.

4. Entering platter identification numbers selects the drive test sequence and the platters to be tested. The zero character (0) selects the first drive unit;

the one character (1) selects the econd drive unit. For example, enter the following character to test both platters of the first drive unit:

```
*0 <cr>
```

Type 0R<cr> to test the removable disk or type 0F<cr> to test the fixed disk of Drive 0. Type 1<cr> to test the second drive unit; type 0 1<cr> to test both drive units. The terminal displays the following message:

Make sure all drives and platters selected are ready and not write protected.
*

5. Start the test by typing:

```
*T <cr>
```

The terminal displays the message shown in Figure 3-11, when all tests pass.

```
0001H *** IGNORED ***
0002H *** IGNORED ***
0009H *** IGNORED ***
000BH *** IGNORED ***
000DH *** IGNORED ***
000EH *** IGNORED ***
000FH *** IGNORED ***
0010H *** IGNORED ***
0011H *** IGNORED ***
0012H *** IGNORED ***
0013H *** IGNORED ***
0000H Controller Status Test

controller status test

controller base word = 68H

mds-240/740 firmware level = 02H

0000H Controller Status Test                                    "PASSED"
nop test
0003H NOP Test                                                  "PASSED"
recalibrate test
0004H Recalibrate Test                                          "PASSED"
seek test
0005H Seek Test                                                 "PASSED"
drive selection test
0006H Drive Selection Test                                      "PASSED"
platter/surface selection test
0007H Platter/Surface Selection Test                            "PASSED"
sector selection test
0008H Sector Selection Test                                     "PASSED"
track verify test
0009H Track Verify Test                                         "PASSED"
drive switches test
000AH Drive Switches Test

write protect drive 0T, fixed platter
write enable all other platters
type cr when write protected
```

Figure 3-11. Series IV, CRT Display of SIV740 Confidence Test

6. Write protect the specified platter (drive unit control switches) and press the terminal RETURN key. The test provides additional messages to test the remaining combinations of switch positions. After the sequence of switch tests is complete, the display continues:

```
000AH Drive Switches Test                    "PASSED"
memory addressing test
000CH Memory Addressing Test                 "PASSED"
```

NOTE

Check the 740 Hard Disk "READY" indicator and make sure it is lit (up to speed) before proceeding with the SIV740 test.

7. Test 14 then displays the error tables. A prompt message is displayed to allow the operator to clear the error tables.
8. Press the RETURN key. The terminal displays the command prompt (*) to indicate that the program is at the TMON command level.

NOTE

To exit TMON and return to the diagnostic monitor so that another test suite may be loaded and exercised or testing abandoned altogether, type:

```
*EXIT<cr>
```

3.19.2 SIV740 Test Descriptions

Table 3-16 identifies each SIV740 test and describes the operation of each test as it exercises the 740 logic.

Table 3-16. Series IV, SIV740 Test Descriptions

Test No.	Test Name	Test Description
0000H	Controller Status	Verifies basic controller commands and displays controller ID values.
		Controller Self Tests
*0001H	Self Diagnostic	Reserved for Intel Service Personnel.
*0002H	20-Bit Self-Diagnostic	Reserved for Intel Service Personnel.
		Drive Test Sequence
0003H	NOP	Verifies handshaking ability of controller by executing NOOP function.
0004H	Recalibrate	Verifies ability to recalibrate drive by seeking track 407, then back to track 0.
0005H	Seek	Verifies ability to seek to preselected tracks.
0006H	Drive Selection	Verifies that controller can access each drive separately when more than one drive is connected to the controller.
0007H	Platter/Surface Selection	Verifies that each platter and head can be addressed individually.
0008H	Sector Selection	Verifies that each sector of a track can be addressed individually.
*0009H	Track Verify	Verifies all sectors of data on preselected tracks.

Table 3-16. Series IV, SIV740 Test Descriptions (Cont'd)

Test No.	Test Name	Test Description
000AH	Drive Switches Tests	Verifies that controller can detect status changes caused by drive READY and WRITE PROTECT switches. The user is prompted to make several changes to the switches during test.
**000BH	Overlap Seek Test	Verifies ability to perform concurrent seeks on multiple drives. This test is ignored when the user tests one drive.
000CH	Memory Addressing	Verifies ability of controller to access system RAM memory during data transfers between the system and the disk.
**000DH	Format Track	Initializes specific tracks by writing all address marks, gaps, and data fields to verify format ability of drive. The selected tracks also ensure that tracks can be addresses individually.
**000EH	Track Selection	Verifies ability to individually address disk tracks.
**000FH	Cartridge Defect	Formats and verifies all disk tracks. This test, when run before test 10H causes the test to execute faster.
**0010H	Long Data Transfer	Writes, reads, verifies, and compares data on all tracks, surfaces, and platters. Tracks are accessed in a psuedo-random order from a fixed table in memory. Controller differentiates between recoverable (successful retries) and non-recoverable errors (unsuccessful retries) and alternates between 16-bit and 20-bit addressing when accessing system memory.
**0011H	Reserved	Reserved for future use.
0012H	Verify Platter	Verifies surface integrity of selected platters without destroying user data. A decimal digit is displayed for each track verified (the sequence 0–9 is repeated 40 times).
		Error Detection Test Sequence
*0013H	Error Detection	Reserved for Intel Service Personnel.
		Utility Routine
0014H	Display Error	This utility routine displays two error tables (one for each drive test sequence) and allows the user to clear the tables.

* Test initially ignored

** Tests 000DH to 0011H are ignored at test initialization because they destroy data. Test 000BH is ignored when only one drive unit is selected for testing.

3.19.3 SIV740 Test Execution Times

Approximate execution times for individual SIV740 tests or series of tests are listed in Table 3-17.

Table 3-17. Series IV, SIV740 Test Execution Times

Drive Tests	Execution Time
0	2 seconds
3 to 9	24 seconds (Combined)
*A	65 seconds (Minimum)
**B	60 seconds (Maximum)

Table 3-17. Series IV, SIV740 Test Execution Times (Cont'd)

Drive Tests	Execution Time
C	3 seconds
D	27 seconds
E	17 seconds
F	6 minutes 45 seconds
10	6 minutes 47 seconds
11	Ignored
12	5 minutes 12 seconds

* User must configure drive unit control switches during test.

** Ignored when only one drive unit is selected for testing.

Times shown assume the following:

- Testing both platters of one drive unit (two drive units for test 000BH).
- TMON debug switch set (=1) to enable error messages.
- All tests will pass.

3.19.4 SIV740 Error Messages

The SIV740 test suite displays error codes and messages to aid in isolating a hardware fault to a replaceable subassembly. The failing test number identifies a faulty subassembly. Failing test numbers and related subassemblies are as follows:

Test Number	Subassembly
0-14	740 Controller
3 to 12H	740 Controller/Cables/Drive

Table 3-18 lists the error codes, messages, and descriptions that may be displayed during execution of the drive test sequence. These messages can help isolate a fault to the controller, cables, or drive unit(s).

Table 3-18. SIV740 Drive Sequence Error Messages

Code	Message/Description
01	ID MISCOMPARE: One of the ID fields does not match format. If failure persists, reformat drive.
02	DATA CRC ERROR: Generated data CRC does not match CRC written on drive; data is not recoverable.
04	SEEK ERROR: Head positioned over wrong track at end of seek.
08	SECTOR ADDRESS ERROR: Sector parameter received from host CPU is invalid.
0A	ID CRC ERROR: Generated ID CRC does not match CRC written on drive; not recoverable.
0B	PROTOCOL ERROR: Operation attempted with seek-in-progress; probable controller fault.
0C	ILLEGAL CYLINDER ADDRESS: Cylinder address received from host CPU is invalid.
0D	TIMEOUT: No response from controller.
0E	NO ID ADDR MARK: No ID address mark found.
0F	DATA ADDR MARK ERROR: Data address mark missing.

Table 3-18. SIV740 Drive Sequence Error Messages (Cont'd)

Code	Message/Description
10	DATA OVERRUN: Controller unable to service a transfer request from drive.
20	WRITE PROTECT: Selected platter write protected.
40	WRITE ERROR: Drive unable to write.
80	DRIVE NOT READY: Drive not in ready state.
81	BAD SUBSYSTEM STATUS: Controller bad or not present.
82	BAD CHANNEL STATUS: Controller is busy.
83	BAD CONTROLLER ID: Controller is not a Model 740.
88	SECTOR SELECT ERROR: A sector cannot be uniquely addressed.
89	FALSE INTERRUPT: Host CPU received invalid interrupt request.
8A	FORMAT ERROR: Format error.
8B	DATA ERROR: Write/read data miscompare.
8C	INVALID RESULT: Controller result byte not zero (0 = operation complete).
8D	DRIVE SELECT ERROR: A drive cannot be uniquely selected.
8E	PLAT SELECT ERROR: A platter cannot be uniquely selected.
8F	TRACK SELECT ERROR: A track cannot be uniquely selected.
90	CONTROLLER ADDR ERROR: Data read from specified address does not match data previously written.

CHAPTER 4
INSTALLING OPTIONS

4.1 Introduction

This chapter provides information on installing options. The information consists of priority resolution, instructions for installing optional printed wiring assemblies (boards) and peripherals and other information for configuring the system to fit a variety of applications. Before performing the instructions in this chapter, install and test the system as described in Chapters 2 and 3.

4.2 Card Cage Layout

Many of the options available for the system require installation of boards to be connected to a common bus (Multibus backplane). These card slots are referenced from 1 thru 10 beginning at the slot closest to the CRT and incrementing outward toward the right-hand side of the system. The backplane connectors (J1–J10) are numbered in the opposite direction (see Figure 4-1). Slots 7 thru 10 are accessible through the door on top of the system. To install boards in slots 4 thru 6, the cover must be removed from the system. To install boards in slots 1 thru 3, either an RFI shield or a hold-down bracket must be removed.

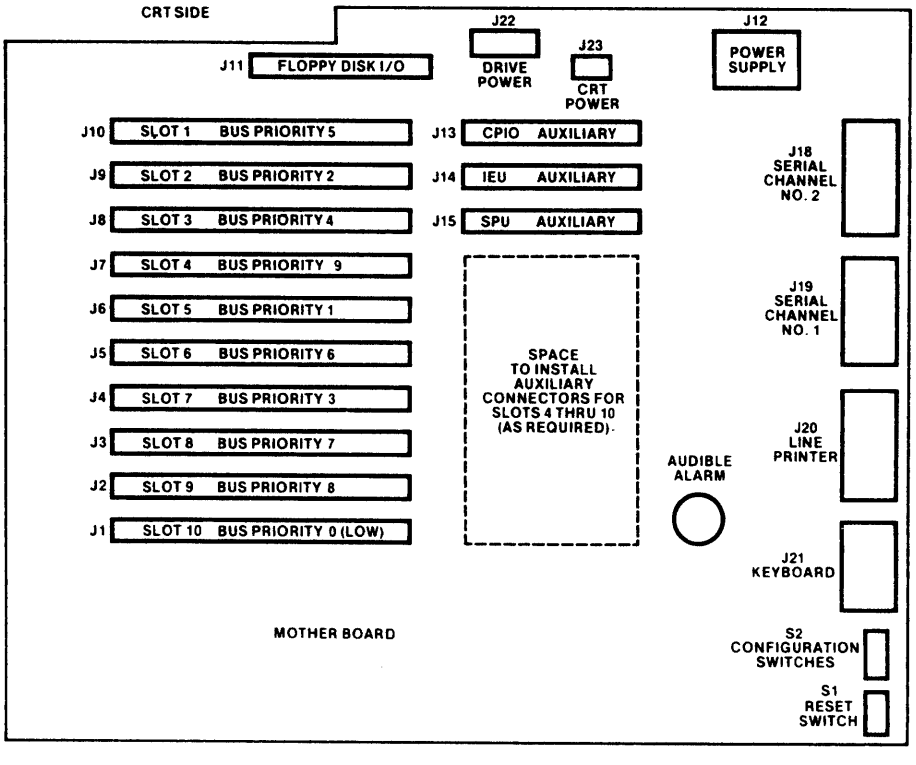


Figure 4-1. Series IV, Backplane Connectors and Slot Assignments

Connectors J13 thru J15 are auxiliary connectors that mate with the P2 connector of the boards installed in slots 1 thru 3, respectively. Space is provided for using auxiliary connectors, if they are required, on the boards installed in slots 4 thru 10. Auxiliary connectors are usually used for communication between boards that are installed in two and three board sets, such as the In-Circuit Emulator (ICE) products. Auxiliary connector assemblies with two and three connectors are supplied with the system accessory kit.

4.3 Backplane Bus Priority

Boards installed in the system backplane access the backplane bus on a priority basis depending upon their card slot location. Usually only one board in the board set will request service through the backplane bus, while other boards in the set may not affect the priority structure. Add-on memory boards do not request us service and can be inserted in any slot without changing the existing priorities. The priorities assigned to each slot are listed in Table 4-1 and shown in Figure 4-1.

Table 4-1. Series IV, Bus Priority Assignments

Bus Priority	Slot Number	Backplane Connector Designation
9 (Highest)	4	J7
8	9	J2
7	8	J3
6	6	J5
5	1	J10, J13
4	3	J8, J15
3	7	J4
2	2	J9, J14
1	5	J6
0 (Lowest)	10	J1

4.4 Installing Optional Boards

The priorities of various optional boards of the basic system are shown in Figure 4-2. Before installing options determine the exact board placement. Optional boards are installed in the mainframe card cage using the applicable procedures given in Paragraphs 4.5 thru 4.9. Before an optional board is installed, determine first what applicable procedures must be performed by answering the following:

1. What is the relative priority for the board to be installed? Refer to Figure 4-2.
2. Is an auxiliary connector required? Refer to Paragraph 4.5.
3. Does installation require an internal cable assembly to connect between a top-edge connector on the board and an external device? Refer to Paragraph 4.7.
4. What slot or slots will be used to install the board or board set? To install boards in slots 4 thru 10, refer to Paragraph 4.8; boards in slots 1 thru 3 (CPIO, IEU and SPU) refer to Paragraph 4.9.

NOTES:

1. **If the ICE, Model 740/743, iSBC550 and iMDX720 options are to be installed, the ICE Controller board must be installed in the highest priority slot followed by the iMDX720 Controller board in the next highest priority slot.**
2. **If the iMDX720 and Model 740/743 are to be installed, the iMDX720 Controller board should be given a higher priority than the Model 740/743.**
3. **ICE and ISIS Cluster boards are not defined for concurrent use. Refer to the *Series IV iMDX-580/582 ISIS Cluster Installation, Operation, and Service Manual*, Order no. 134650 for system configurations supporting ISIS Cluster.**
4. **I2ICE requires .5 MB of system memory.**

Priority	Slot	Jack	Board	Configuration Options								
5	1	J10	CPIO									
2	2	J9	IEU									
4	3	J8	SPU*									
9	4	J7	012 or 056									
1	5	J6		215D	550 or 740	215D	215D	215B	215B	215D	215D	215D
6	6	J5		550 or 740	550 or 740	215B	215B			215B	215B	215B
3	7	J4		550 or 740	ICE	550 or 740	550	550 or 740	ICE			
7	8	J3		ICE	ICE	550 or 740	550	550 or 740	ICE	550 or 740	ICE	Open
8	9	J2		ICE	ICE	ICE	740	ICE or 720	ICE	550 or 740	ICE	740 or 720
0	10	J1		ICE	ICE	ICE	740	ICE or 720	ICE	Open	ICE	740 or 720

*If present

121757-15

Figure 4-2. Series IV, Optional Board Placement

CAUTION

DO NOT remove, install, connect or disconnect any board or cable assembly while system power is on. Performing these operations with power on may cause damage to connectors and other components.

4.5 Auxiliary Connector Installation

Auxiliary connectors usually consist of two or three edge connector sockets mounted on a printed wiring assembly. They are used to provide interconnections (interface) between the P2 connectors in board sets that contain two or three boards. The ICE-85 and ICE-86 are typical options with two or three board sets that require auxiliary connectors.

One auxiliary connector with two sockets (dual-auxiliary connector) and one auxiliary connector with three sockets (triple-auxiliary connector) are shipped with the system. These connectors are also usually shipped with options that require them. To ensure proper spacing between connectors, use only auxiliary connectors with the following part numbers:

Dual-Auxiliary Connector, part number 1000515-01
Triple-Auxiliary Connector, part number 1001854-01

The auxiliary connectors cannot be installed permanently in the card cage and must be connected to the board set first and then the board set inserted, as a unit, into the appropriate slots in the card cage.

4.6 Top Cover Removal and Reinstallation

It is not always necessary to remove the top cover from the system to install boards. Card cage slots 7 thru 10 are accessible through the board access door (see Figure 4-3). To install boards into card cage slots 1 thru 6 the top cover must be removed.

WARNING

High voltage is present in the mainframe chassis. DO NOT attempt to connect power or operate the system with the cover removed. DO NOT attempt to override the safety interlock switch. DO NOT come in contact with the CRT anode connection. Failure to observe these precautions may result in serious injury.

To remove the top cover from the system, proceed as follows:

1. Turn off system power at the power circuit breaker switch and also disconnect the ac power plug from the power outlet to prevent accidental power turn-on.
2. Loosen the cover retaining thumbscrew until it is completely free from the top cover (see Figure 4-3). The thumbscrew remains captive in the base.

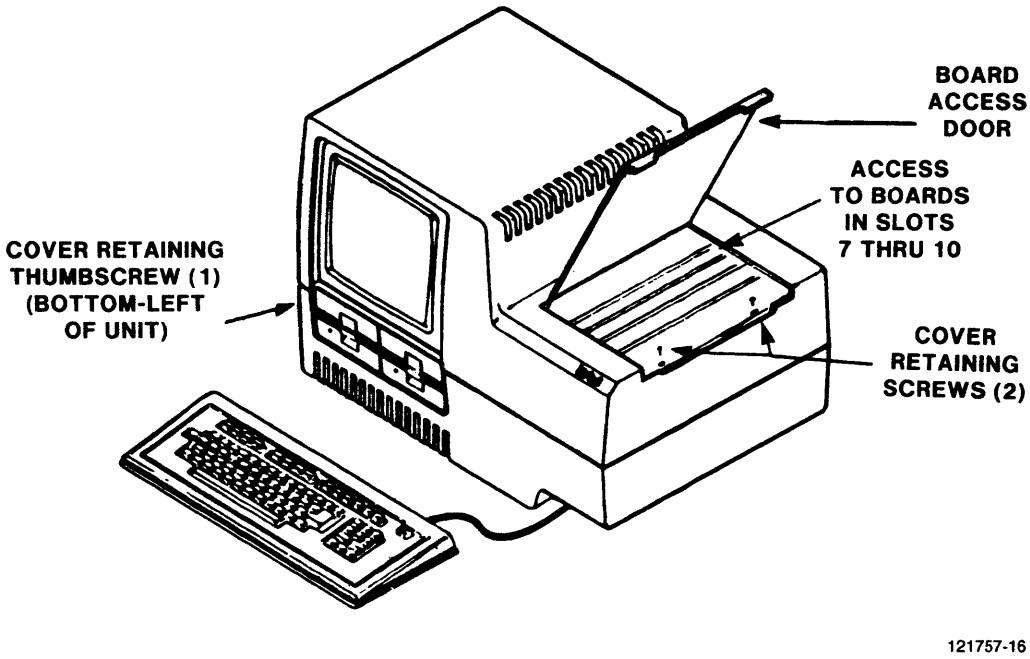


Figure 4-3. Series IV, Mainframe Board Access Door Opened

3. Lift the board access door and loosen the two cover retaining screws until the screws are completely free from the base (see Figure 4-3). The cover retaining screws remain captive in the cover.

WARNING

While handling the cover or working inside the system chassis, use extreme care not to strike the CRT neck or base. Striking the CRT neck or base could cause the CRT to implode and may cause injury, death and damage in the immediate area.

4. Close the board access door and then lift straight up on the top cover until the top cover completely clears the card cage and CRT. Set the cover aside so that the work area is kept clear.
5. Re-install the cover before resuming operation by reversing the procedure in steps 1 thru 4.

4.7 Internal Cable Assembly Installation

An internal cable assembly must be installed for boards that interface through their top-edge connector with an external device. The cable assembly and its mounting hardware are usually shipped with the board or board set that requires the external connection. Connectors at one end of the cable assemblies are mounted in the utility connector slots on the back panel (see Figure 4-4). Install any ground wires from the cable assemblies to the threaded inserts, provided on the back panel, with appropriate hardware. The other end of the cable assemblies have connectors that mate with top edge connectors on the associated boards.

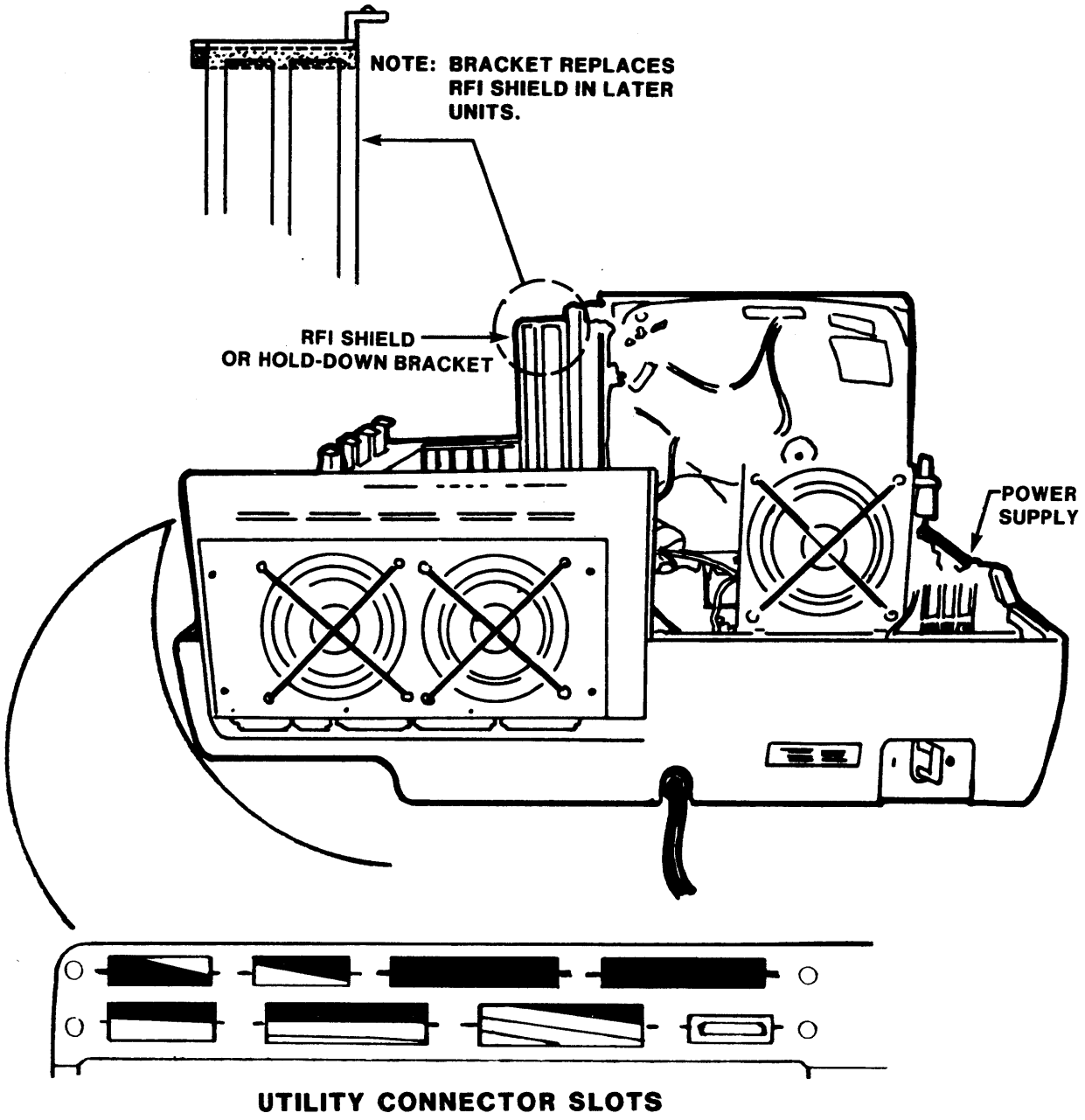


Figure 4-4. Series IV, Mainframe with Cover Removed

The mainframe top cover must be removed in order to gain access to the utility connector slots (refer to Paragraph 4.6). After the cable assembly and board installation are complete, an external cable assembly is connected between the utility connectors and the external device to complete the interface.

NOTE

ICE products use flat cable assemblies to interconnect the top-edge connectors and external buffer boxes. These flat cable assemblies are routed through the slot under the board access door. DO NOT route through the utility connectors.

4.8 Installing Boards in Slots 4 thru 10

Card cage slots 4 thru 10 accept 7 x 12 inch (17.8 x 30.5 centimeter) Multibus interface compatible boards. Four of these slots (7 thru 10) are accessible through the board access door (see Figure 4-3) and are usually reserved for boards that may be changed occasionally, need high priorities or that require easy access. Typical options that may be installed in slots 7 thru 10 are ICE and mass storage (disk) controllers (slot 9 has the second highest priority).

When installing ICE boards, route the flat cables from the top edge connectors of the boards through the access door. A slot in the access door has been provided to accommodate these cables.

Slots 4 thru 6 are accessible only when the mainframe top cover is removed, and usually contain boards that are more permanently installed, such as expansion memory boards and data communication board sets and 5¼-inch and 8-inch Winchester Controller boards.

Depending upon the option being installed, an auxiliary connector and internal cable assembly may be required. Information for installing these assemblies is provided in Paragraphs 4.5 and 4.7.

NOTE

Before installing any boards in the card cage, determine where each board fits in the priority structure (refer to Paragraph 4.3).

Install boards in slots 4 thru 10 by:

1. Turning off system power at the power circuit breaker switch and disconnecting the ac power plug from the power outlet to prevent accidental power turn-on.
2. Lifting the board access door (see Figure 4-3) to gain access to card cage slots 7 thru 10, or removing the top cover (refer to Paragraph 4.6) as required.
3. Checking the board, or board set, to be installed to determine proper jumper locations and switch settings. The information necessary for setting the board configuration is usually provided with the manuals or data sheets shipped with the board. Configuration jumper locations for commonly used boards are given in Paragraph 4.10.
4. Installing an auxiliary connector (refer to Paragraph 4.5 and an internal cable assembly (refer to Paragraph 4.7, as required. Install the auxiliary connector on the board set (see Figure 4-5).
5. Installing the board, or board set, in the card cage, making sure that the board edges line up in the card cage guide slots. When boards are lined up

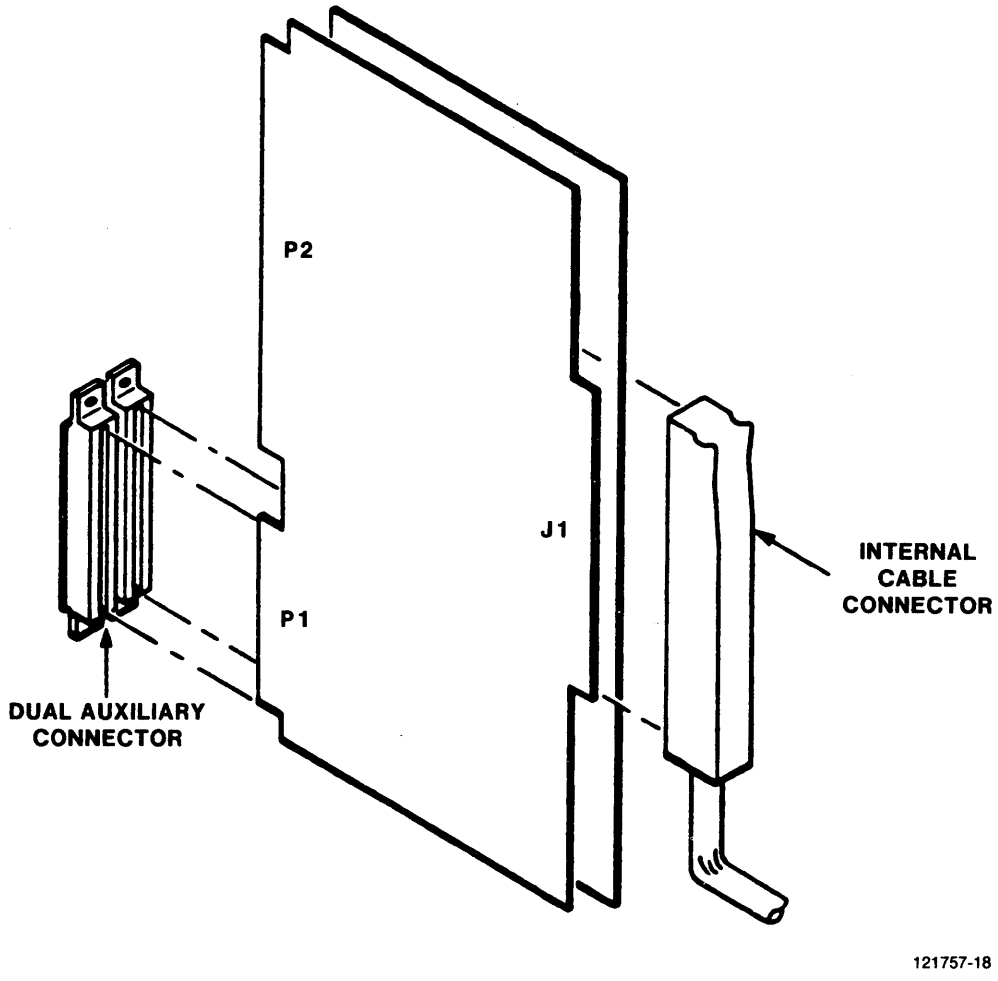


Figure 4-5. Series IV, Auxiliary Connector Installed on a Two-Board Set

and resting on the backplane bus connectors, press down firmly on the lifters at the top corners of the boards until the P1 edge connectors (see Figure 4-5) are seated in the bus connectors.

6. Re-installing the mainframe top cover (refer to Paragraph 4.6) and closing the board access door.
7. Connecting the ac power plug to the three-conductor power outlet, powering up the system and performing the test procedures given in Chapter 3 to verify that system operation has not been affected. The test procedures will check optional memory boards installed in slots 4 thru 10, but to do so, some normally ignored test(s) must be recognized.

4.9 Installing CPIO, IEU and iMDX-434 SPU Boards

The CPIO, IEU and the optional iMDX-434 SPU boards are installed in card cage slots 1, 2 and 3, respectively. Slots 1 thru 3 are accessible only after the top cover is removed from the mainframe and, depending which is installed in your system, either the Radio Frequency Interference (RFI) shield or the Board Holddown Bracket is removed from the card cage (see Figure 4-6). Slots 1 thru

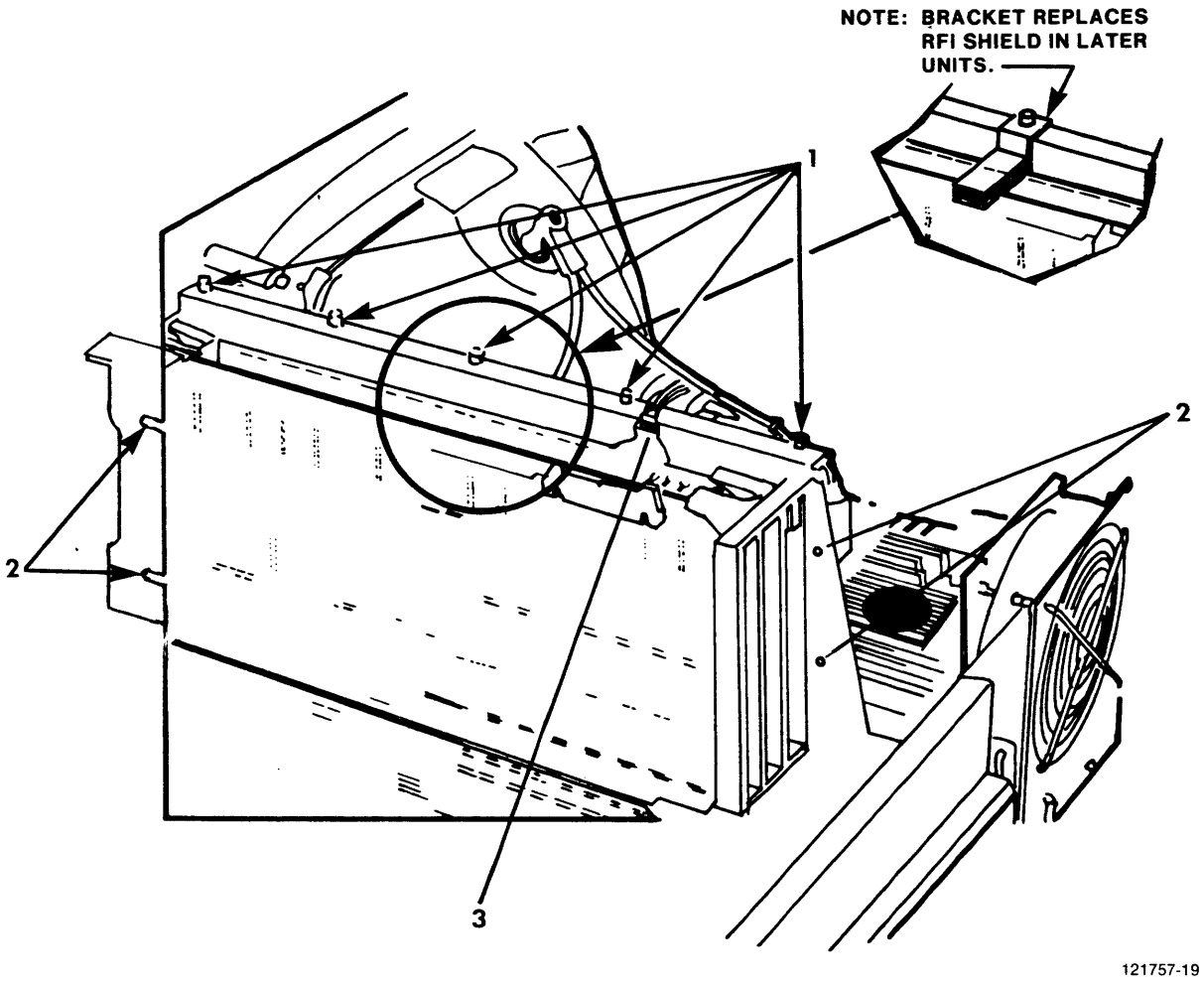


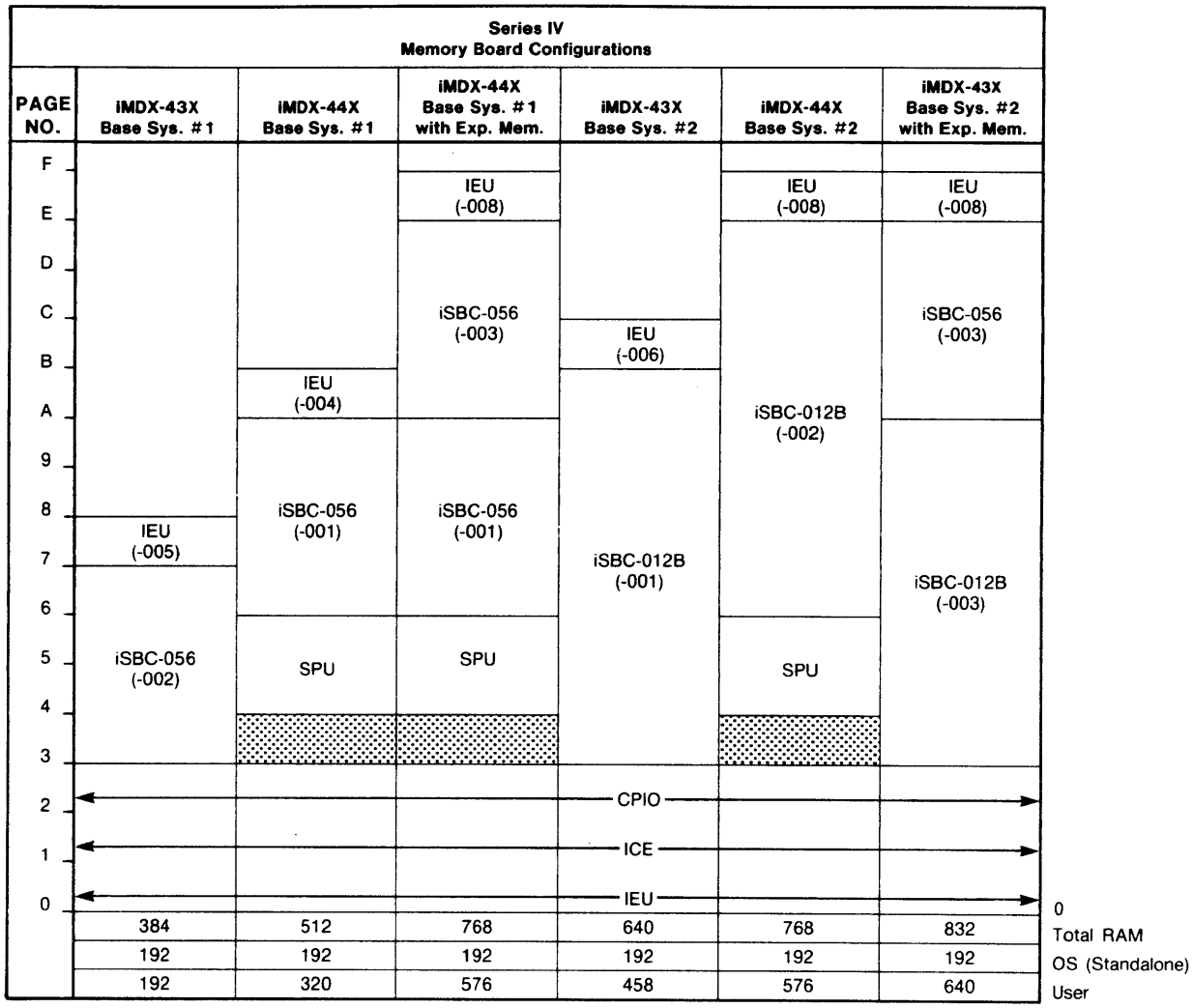
Figure 4-6. Series IV, Mainframe with Cover and RFI Shield Removed

3 accept 12 x 12 inch (30.5 x 30.5 centimeter) boards that are dedicated to system operation. The layout for these three slots is shown in Figure 4-1 and listed in Table 4-2.

Table 4-2. Series IV, Slot 1, 2 and 3 Layout

Card Slot	Board Name	Board Mnemonic	Bus Conn.	Aux. Conn.	I/O Conn.
1	Central Processor and I/O	CPIO	J10	J13	J11,J19 J20,J21
2	ISIS Execution Unit	IEU	J9	J14	J18
3	Enhanced Performance Option	SPU	J8	J15	---

The CPIO and IEU boards are currently installed in the mainframe when the unit is shipped from the factory. The optional SPU board is shipped in a separate box and must be installed by the user. Prior to attempting an SPU board installation and/or a memory upgrade, refer to Figure 4-7 for the Series IV system memory addressing schemes supported. Note that whenever an SPU board



NOTES:

1. **ALL TOTAL RAM, OS AND USER MEMORY FIGURES ARE KBYTES.**
2. **I^2 ICE REQUIRES 512 KBYTES OF USER MEMORY.**
3. **REFER TO RESPECTIVE BOARD DIAGRAM IN CHAPTER 4 OF THIS MANUAL FOR JUMPER DATA.**

121757-20

Figure 4-7. Series IV, System Memory Addressing Schemes Supported

is added, the memory address jumpers for the IEU and memory board(s) must be reconfigured as indicated for the board dash number shown on Figure 4-7; refer to the respective board diagram for jumper data. After becoming familiar with the addressing schemes, proceed on with the board installations as follows:

1. Turn off system power at the power circuit breaker switch and disconnect the ac power plug from the power outlet to prevent accidental power turn-on.
2. Remove the top cover as described in Paragraph 4.6.
3. If the RFI shield is installed in the system, perform the following:
   a. Loosen the five screws on top of the RFI shield (see item 1 of Figure 4-6). Do not remove the screws. These top screws may remain in the card cage frame.
   b. Loosen the four captive screws on the side of the RFI shield (see item 2 of Figure 4-6). These side screws (two in front and two in back) remain captive in the RFI shield.
   c. Slide the RFI shield out from under the top screws and set the RFI shield aside to keep the work area clear.
4. If the Board Hold-down Bracket is installed, remove it by removing the single screw securing it in place.

NOTE

The CRT is connected to J1 on the top of the CPIO board. J1 is the only top edge connector used in slots 1 thru 3.

5. Check the configuration jumpers and switch settings on each board to be installed. The configuration jumper locations and switch settings for the CPIO, IEU, SPU and iSBC-012/056 boards are shown in Figures 4-8 thru 4-12. Refer also to Paragraph 4.10
6. Install the board in the correct card cage slot (see Figure 4-1), making certain that the board edges line up in the appropriate card cage guide slots (see Figure 4-4). When the board is lined up and resting on the backplane bus connector, press down firmly on the lifters at the top corners of the board until the bottom edge connectors are seated in the backplane connectors.
7. Connect the CRT cable to J1 on the CPIO board (see item 3 of Figure 4-6).
8. Re-install either the RFI shield or the Board Hold-down Bracket.
9. Re-install the mainframe top cover (refer to Paragraph 4.6).
10. Apply power to the system and perform the test procedures given in Chapter 3 to verify that the system operation has not been affected.

4.10 Plug-On Jumper Options

Printed wiring assemblies (boards), to be installed in the mainframe card cage, require that plug-on jumper locations be verified to establish the proper configuration. Standard system boards are usually supplied with the plug-on jumpers installed in default locations and only verification of their installation is required. In some cases, (such as the SPU option), an optional configuration is required and jumpers must be adjusted to satisfy requirements; six extra jumpers are provided in the auxiliary kit for this purpose. Whenever the SPU option is added, the memory board(s) and IEU board jumpers must be reconfigured to reflect the new memory addressing required; refer to Figure 4-7 to determine the correct addressing scheme for your system.

For most optional boards, plug-on jumper locations are given in a technical manual provided with the board. To simplify configuring each board, the plug-on jumper locations for the more commonly used optional boards are provided along with the standard system boards in Figures 4-8 thru 4-12. The jumper locations for all boards should be checked and verified before the boards are installed in the mainframe card cage.

4.11 Down-Loading

The system accessory kit contains a cable (P/N 108197) that is used to down-load programs from external 8-inch floppy diskettes to the internal 5¼-inch floppy diskettes. The external disk drive must be controlled by a Series II or Series III development system that has an external RS-232 Serial I/O connector available.

Before connecting or disconnecting the down-load cable, be sure to power down both systems. Failure to remove power from the systems may result in damage to the cable or connector.

To connect the cable, first shut off power to both systems, then locate the serial I/O channel connectors on both systems. Connect one end of the down-load cable to the Series IV Serial Channel 2 connector (J18) and the other end to the Series II/III Serial I/O connector (J2-Serial Ch 1/TTY). The IEU board must be in slot 2 (J9). Reapply power to both systems.

With the cable connected, ISIS files can be copied to a specified location within the iNDX file structure and vice-versa using the FPORT utility program. Refer to the *Intellec Series-IV Operating and Programming Guide*, Order Number 121753, for complete instructions on the use of the FPORT utility program. When the down-loading operation is completed, power down both systems and disconnect the cable.

4.12 Connecting Optional Peripherals

Three D-type, 25-pin connectors are provided on the system back panel for connecting peripheral devices. The three connectors are hard wired to the motherboard and the controller circuits are contained on the CPIO and IEU boards. Optional peripheral devices are connected to the system with user supplied cables. One end of the cables must have a connector that mates with the system connectors. The mating connectors are Amphenol Part Number 205208-1 or equivalent.

The system provides connectors for one line printer channel (J20) and two serial channels (J19 and J18). The Line Printer Channel and Serial Channel 1 (J19) are controlled by circuits on the CPIO board. Serial Channel 2 (J18) is controlled by circuits on the IEU board. Table 4-3 provides signal names and functions, connector pin assignments and circuit loading characteristics for the Line Printer Channel.

A second-user terminal may be connected to Serial Channel 1 as instructed in Appendix C. The two serial channels are fully compatible with both the EIA Standard RS-232-C and the International Telegraph and Telephone Consultive

Committee (CCITT) Recommendation V.24 (see Table 4-4). For this manual, Data-Terminal Equipment (DTE) is defined as the Series IV system and the Data Circuit-Terminating Equipment or Data Comminication Equipment (DCE) is defined as the external peripheral device that connects to the system. Signal outputs are defined as going from the system to the external device and signal inputs are defined as going from the external device to the system. The term "signal element", as specified in the description Transmitter Signal Element Timing is defined as a binary data bit. The signal voltage levels are as follows:

1. The MARKING or OFF condition is more negative than −3Vdc.
2. The SPACING or ON condition is more positive than +3Vdc.
3. The area between −3Vdc and +3Vdc is an unspecified transition region.
4. All voltage levels are given with respect to signal ground.

Circuit loading characteristics for serial channels 1 and 2 are defined by the specification for the output and input drivers, SN75188 and SN75189. These drivers are designed to meet all requirements of the *EIA RS-232-C specification.* Table 4-3 provides connector pin assignments and signal identifications, names and descriptions for both serial channels.

Turn off system power before connecting or disconnecting peripheral cables. Failure to shut off power when connecting or disconnecting cables may cause damage to the connectors or sensitive electronic parts.

Extreme care should be taken NOT to plug a line printer cable into a serial channel connector. Safeguards have been installed but damage could still occur.

Table 4-3. Line Printer Connector J20 Pin Assignments

Pin No.	Signal	Function	Current Drive		Current Load		Termination in Ohms
			Low (I_{OL})	High (I_{OH})	Low (I_{IL})	High (I_{IH})	
1	LPDATA0	Output Data Bit 0 **NOTE** For pins 1–8, high is a binary 1 and low is a binary 0. The coding format is ASCII for characters and control functions.	24mA	−15mA	—	—	—
2	LPDATA1	Output Data Bit 1	24mA	−15mA	—	—	—
3	LPDATA2	Output Data Bit 2	24mA	−15mA	—	—	—
4	LPDATA3	Output Data Bit 3	24mA	−15mA	—	—	—
5	LPDATA4	Output Data Bit 4	24mA	−15mA	—	—	—
6	LPDATA5	Output Data Bit 5	24mA	−15mA	—	—	—
7	LPDATA6	Output Data Bit 6	24mA	−15mA	—	—	—
8	LPDATA7	Output Data Bit 7	24mA	−15mA	—	—	—
9–12	GND	Logic Ground					
13	FAULT/	Printer Error. A low (binary 0) indicates a condition such as paper empty, deselect, or platen open.	—	—	−.02mA	.02mA	470
14	DATASTB/	Data Strobe. A low to high transition clocks data from the controller to the printer.	24mA	−15mA	—	—	—
15	GND	Logic Ground					
16	ACKNLG/	Data Acknowledge. A low to high transition indicates that the current character was received or the current instruction was implemented.	—	—	−.02mA	.02mA	470
17	BUSY	Printer Busy. A high (binary 1) indicates the printer is not ready to receive new characters.	—	—	−.02mA	.02mA	470
18	GND	Logic Ground					
19	PRIME/	Printer Reset. A low to high transition resets the printer logic.	24mA	−15mA	—	—	—
20	N/C	No Connection					
21	GND	Logic Ground					
22	SELECT	Printer Select. A high (binary 1) indicates the printer switch is closed, the printer is loaded with paper, and the platen is closed.	—	—	−.02mA	.02mA	470
23	GND	Logic Ground					
24	+5Vdc	Power for logic circuits					
25	GROUND	Chassis Ground					

Table 4-4. Serial Channels 1 (J19) and 2 (J18) Pin Assignments

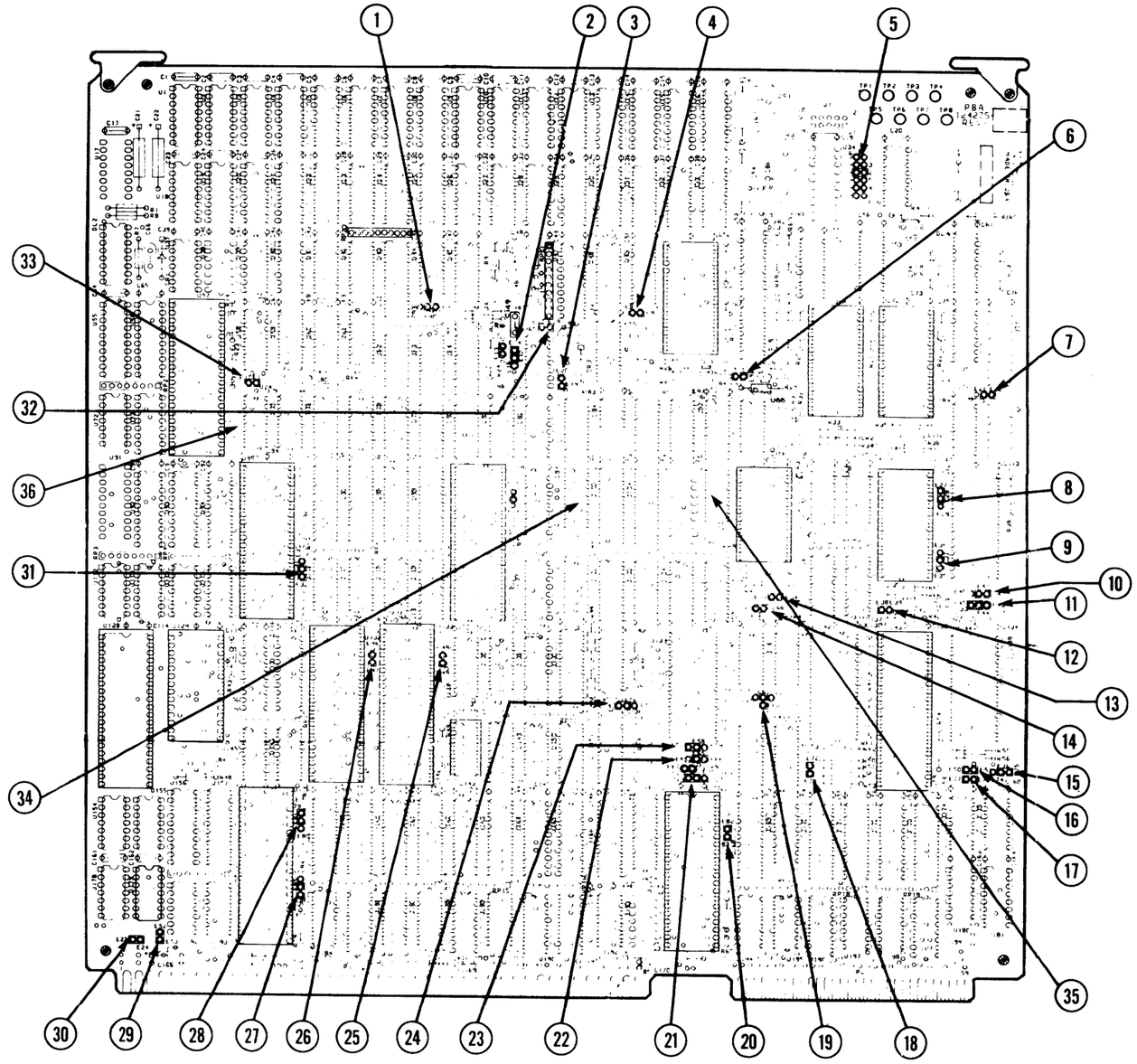
Pin No.	RS-232-C Circuit	C.C.I.T.T. Equivalent	Signal Name	Signal Description
1	AA	101	CHASSIS GROUND	Protective Ground.
2	BA	103	TRANSMITTED DATA (Data Output)	Data on this pin are normally transmitted to an external device. The line can be jumpered to configure either serial channel as a transmitter or receiver, and also to provide loop back capability.
3	BB	104	RECEIVED DATA (Data Input)	Data on this pin are normally received from an external device. The line can be jumpered to configure either serial channel as a receiver or a transmitter, and also to provide loop back capability.
4	CA	105	REQUEST TO SEND (Control Output)	A high level (ON condition) indicates data is ready to transmit. Data is not transmitted until a CLEAR TO SEND is received.
5	CB	106	CLEAR TO SEND (Control Input)	A high level (ON condition) indicates that the external device is ready to receive transmitted data. The CCITT recommendation calls this signal READY FOR SENDING. Jumper options on both serial channels allow the system to accept external clear-to-send (CTS) signals or to provide internal (self-generating) CTS signals. For Serial Channel 1, the CTS signal can be controlled by the program (software).
6	CC	107	DATA SET READY (Control Input)	A high level (ON condition) indicates that the external device is connected and ready to communicate with the system.
7	AB	102	LOGIC GROUND	Signal Ground (Common Return).
8	CF	109	RECEIVED LINE SIGNAL DETECTOR (Control Input)	This line can be activated by a jumper on Serial Channel 1 only. If activated, a high level (ON condition) indicates that no signal is being received or the received signal is unsuitable for demodulation.
9, 10	—	—	No Connection	Reserved for data set testing.
11	—	126	SELECT TRANSMIT FREQUENCY (Control Output for CCITT only)	This signal selects one of two transmit frequencies. A low level (OFF condition) selects the lower frequency and a high level (ON condition) selects the higher frequency. The signal is programmable for Serial Channel 1 and jumper selectable (normally low) for Serial Channel 2.
12	SCF	122	No Connection	Not Used.
13	SCB	121	No Connection	Not Used.
14	SBA	118	No Connection	Not Used.
15	DB	114	TRANSMIT CLOCK IN (Clock Input)	This Transmitter Signal Element Timing signal is jumper selectable to be received from the external device or an internal clock source. Serial Channels 1 and 2 are normally jumpered to accept the internal clock. In either case, a low to high level transition (OFF to ON condition) causes data to be output on the TRANSMITTED DATA LINE.
16	SBB	119	No Connection	Not Used.
17	DD	115	RECEIVE CLOCK (Clock Input for Synchronous Operation)	This Receiver Signal Element Timing signal is jumper selectable to be received from the external device or an internal clock source. Serial Channels 1 and 2 are normally jumpered to accept the internal clock. In either case, a high to low level transition (ON to OFF condition) nominally marks the center of each data bit on the RECEIVED DATA line.

Table 4-4. Serial Channels 1 (J19) and 2 (J18) Pin Assignments (Cont'd)

Pin No.	RS-232-C Circuit	C.C.I.T.T. Equivalent	Signal Name	Signal Description
18	—	—	No Connection	Unassigned.
19	SCA	120	No Connection	Not Used.
20	CD	108.2	DATA TERMINAL READY (Control Output)	A high level (ON condition) indicates the system is ready to transmit or receive data. A jumper in this line allows it to be active or inactive (unjumpered). Normally Serial Channel 1 is active and Serial Channel 2 is inactive.
21	CG	110	No Connection	Not Used.
22	CE	125	No Connection	Not Used.
23	CH	111	DATA SIGNALLING RATE SELECTOR (Control Output)	This signal selects one of two data signalling rates for a dual-rate modem. A high level (ON condition) selects the higher of the two rates, and a low level (OFF condition) selects the lower of the two rates. The signal is programmable for serial channel 1 and is jumper selectable (normally low) for Serial Channel 2.
24	DA	113	TRANSMIT CLOCK OUT (Clock Output for Synchronous Operation)	This Transmitter Signal Element Timing signal is provided by an internal clock for Serial Channel 1 and for Serial Channel 2. On this line, a high to low transition (ON to OFF condition) nominally marks the center of each data bit on the TRANSMITTED DATA line.
25	—	—	+12Vdc	Load not to exceed 50mA.

Series IV, CPIO-B1 Board Jumper Configurations

Jumper Connection	Location	Signal Name
E2 - E6	5	BUS ACK DELAY (40 NS)
E8 - E9	4	USART CLOCK
E10 - E11	33	CAS
E14 - E15	2	PROM SELECT (0FC000-0FDFFFH)
E17 - E18	32	FLOPPY CKT
E19 - E20	3	8 MHz VCO
E21 - E22	7	USART CLOCK
E23 - E24	30	C CLOCK
E27 - E28	8	PROM SELECT (0FE000-0FFFFFH)
E31 - E32	31	UPI CLOCK (10 MHz)
E33 - E34	13	OSC TO 16 MHz
E35 - E37	9	CTS
E38 - E39	12	DTR
E40 - E41	10	RXC
E43 - E44	11	TXC
E46 - E47	26	UPI CLK
E48 - E49	25	8202 CLK
E50 - E51	16	TX DATA
E52 - E53	29	B CLK
E54 - E56	24	FIFO ADR (8-BIT)
E57 - E58	23	LOC ACK (1 WAIT STATE)
E61 - E63	19	FLOPPY WRT COMPENSATION (SWTICHED AT TRK 43)
E65 - E66	22	8088 WAIT FOR TEST
E69 - E70	[illegible]	MULTIBUS ACCESS MEM ADDR (2000H)
E72 - E73	18	FLOPPY WRT CLK (8 MHz)
E75 - E76	15	REC DETECT (DISABLE)
E77 - E78	17	REC DATA
E79 - E81	28	ANY RQST
E82 - E83	20	B INTA
E85 - E86	27	CBRQ/
E87 - E88	14	8202
E90 - E91	1	LOC ACCESS MEM ADDR (0000H & 2000H)
E92 - E93	6	VCO FEEDBACK
E95 - E96	34	VIDEO CHAR WIDTH (8 DOTS)
E97 - E98	34	VIDEO CHAR WIDTH (8 DOTS)
E99 - E100	35	VIDEO CHAR WIDTH (8 DOTS)
E102 - E103	36	BUS TIMEOUT



CBA = 134688

121757-21

Figure 4-8. Series IV, CPIO Board Jumper Configurations

IEU-II Board Jumper Configurations

Jumper Connection	Location	Signal Name
E1 - E2	1	20 MHz OSC
E3 - E4	2	CAS/
E9 - E10	19	READY
E11 - E13	5	TIMER OUTPUT
E14 - E15	18	BREQ/
E16 - E17	16	USART CCK
E19 - E20	3	AACK
E22 - E23	11	TXC
E25 - E26	10	RXC
E28 - E29	9	Req To Send
E31 - E33	8	Sel USART
E34 - E35	17	CBRQ
E36 - E37	14	AACK
E40 - *	13	RXD
E41 - *	12	TXD
E44 - E45	4	RXRDY
E48 - E49	6	TXRDY
E51 - E52	15	Addressing

*PBA 124743-001:
E40-E42
E41-E43

PBA 124743-002:
E40-E43
E41-E42

WIRE-WRAP CONNECTIONS

Memory Jumper Table
(See Location 7)

Memory Address	E55-E56	E59-E60	E57-E58	E53-E54
0XXXX	X	X	X	X
1	X	X	X	
2	X	X		X
3	X	X		
4	X		X	X
5	X		X	
6	X			X
7	X			
8		X	X	X
9		X	X	
A		X		X
B		X		
C			X	X
D			X	
E				X
FXXXX				

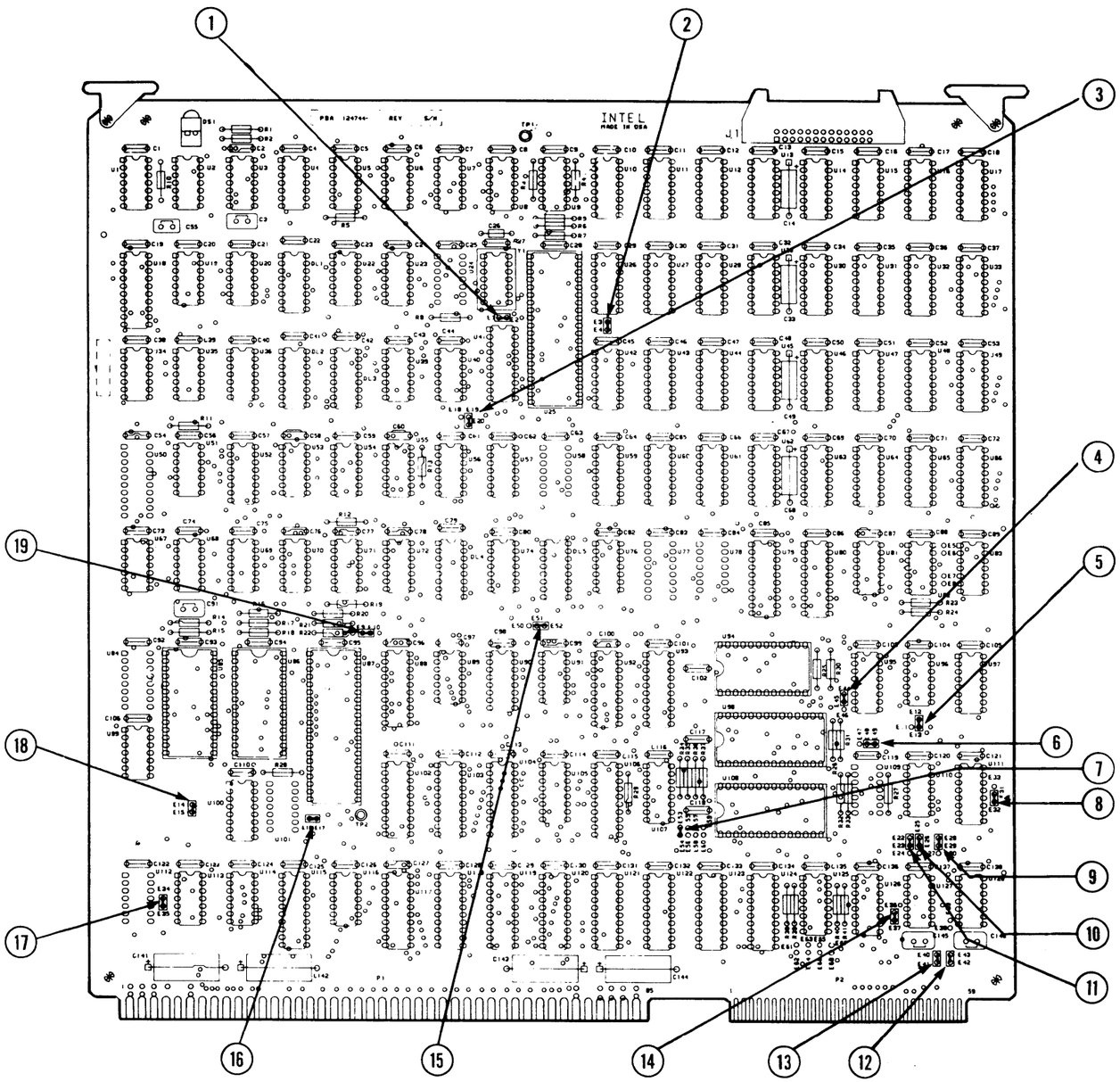
-005 iMDX-43X (07000:FFFF) → 7

-004 (0A000:FFFF) → A

-006 (0B000:FFFF) → B

-008 (0E000:FFFF) → E

X = Jumper Installed



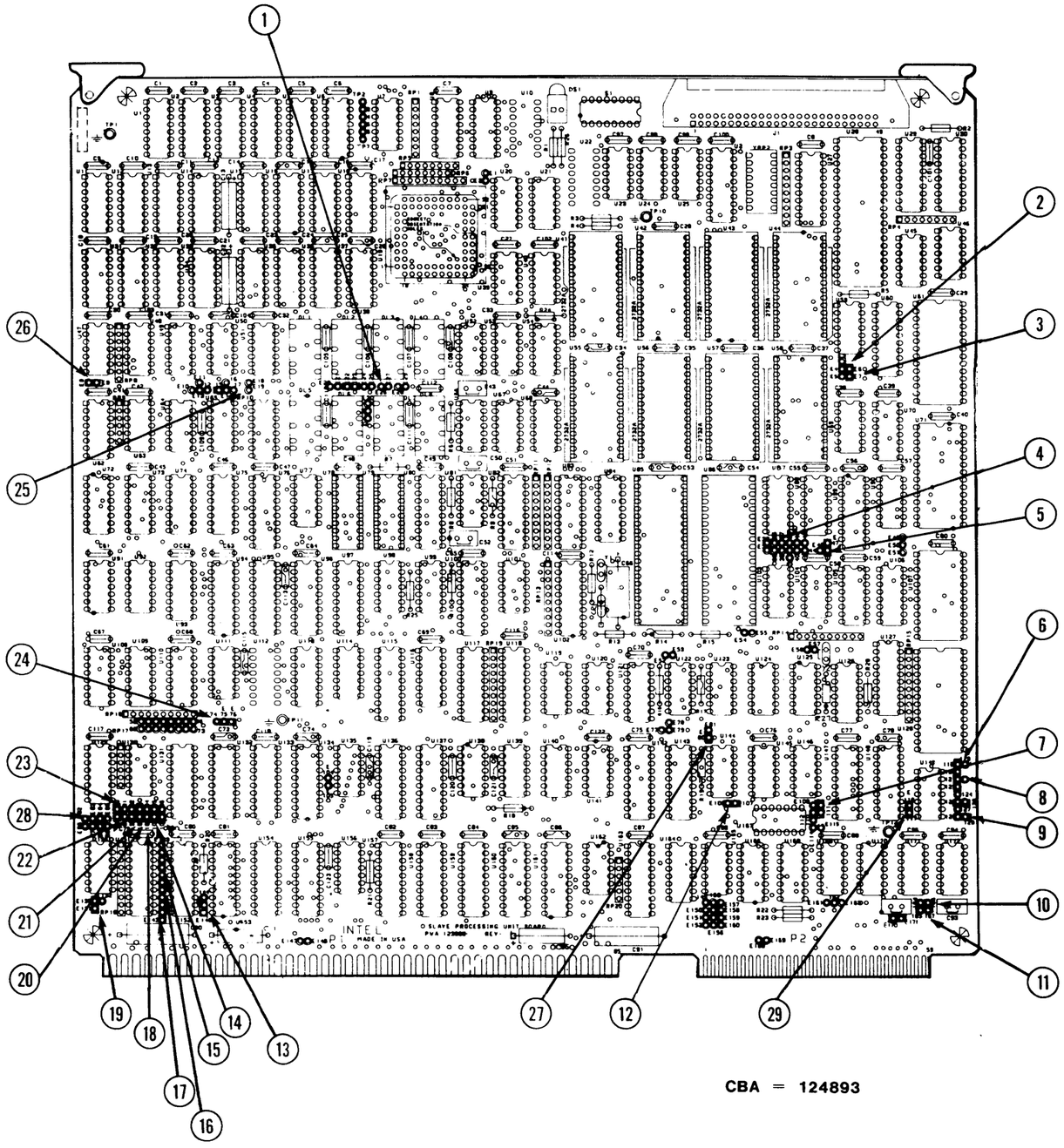
CBA = 125169

121757-22

Figure 4-9. Series IV, IEU Board Jumper Configurations

SPU Board Jumper Configurations

Jumper Connection	Location	Signal Name
E4-E5	2	ABE PROM ADDRESS
E6-E7	3	ABD PROM ADDRESS
E8-E9	26	DELAY LINE LOOP
E14-E15	25	TAP 2
E22-E23	1	160NS -RDY TWO
E35-E36	4	256-384 ONBOARD RAM ZONE
E47-E48	5	TAP 6 ONBOARD RAM RDY
E75-E76	24	I/O HIGH BYTE SELECT
E80-E81	27	RESTART/ UNCORRECTABLE ERROR
E84-E88	28	5 I/O LOW BYTE ADDRESS
E90-E97	23	11 BUS MEMORY HIGH ZONE COMPARE
E92-E99	22	13 BUS MEMORY HIGH ZONE COMPARE
E93-E100	21	14 BUS MEMORY HIGH ZONE COMPARE
E94-E101	20	15 BUS MEMORY HIGH ZONE COMPARE
E95-E102	18	16 BUS MEMORY HIGH ZONE COMPARE
E96-E103	14	17 BUS MEMORY HIGH ZONE COMPARE
E106-E107	12	9.8304 MHZ TO TIMER
E109-E111	7	READY ONE CLOCK DELAY ONBOARD RAM
E116-E117	29	WRITE ZERO/MEMORY SCRUB
E118-E120	6	CTS TO CTS
E121-E123	8	RXD SEL BY RTS
E125-E126	9	TXCI
E128-E129	9	RXC IN
E130-E131	19	ACTIVATE BUS ADR 14 TO MEMORY
E135-E136	15	ACTIVATE BUS ADR 17 TO MEMORY
E138-E139	16	ACTIVATE BUS ADR 16 TO MEMORY
E141-E142	17	ACTIVATE BUS ADR 15 TO MEMORY
E145-E146	13	CBRQ/ TO BUS
E164-E166	10	REC DATA
E165-E167	11	TRANSMIT DATA
E170-E171	11	DRIVE TO MONIT LED



121757-23

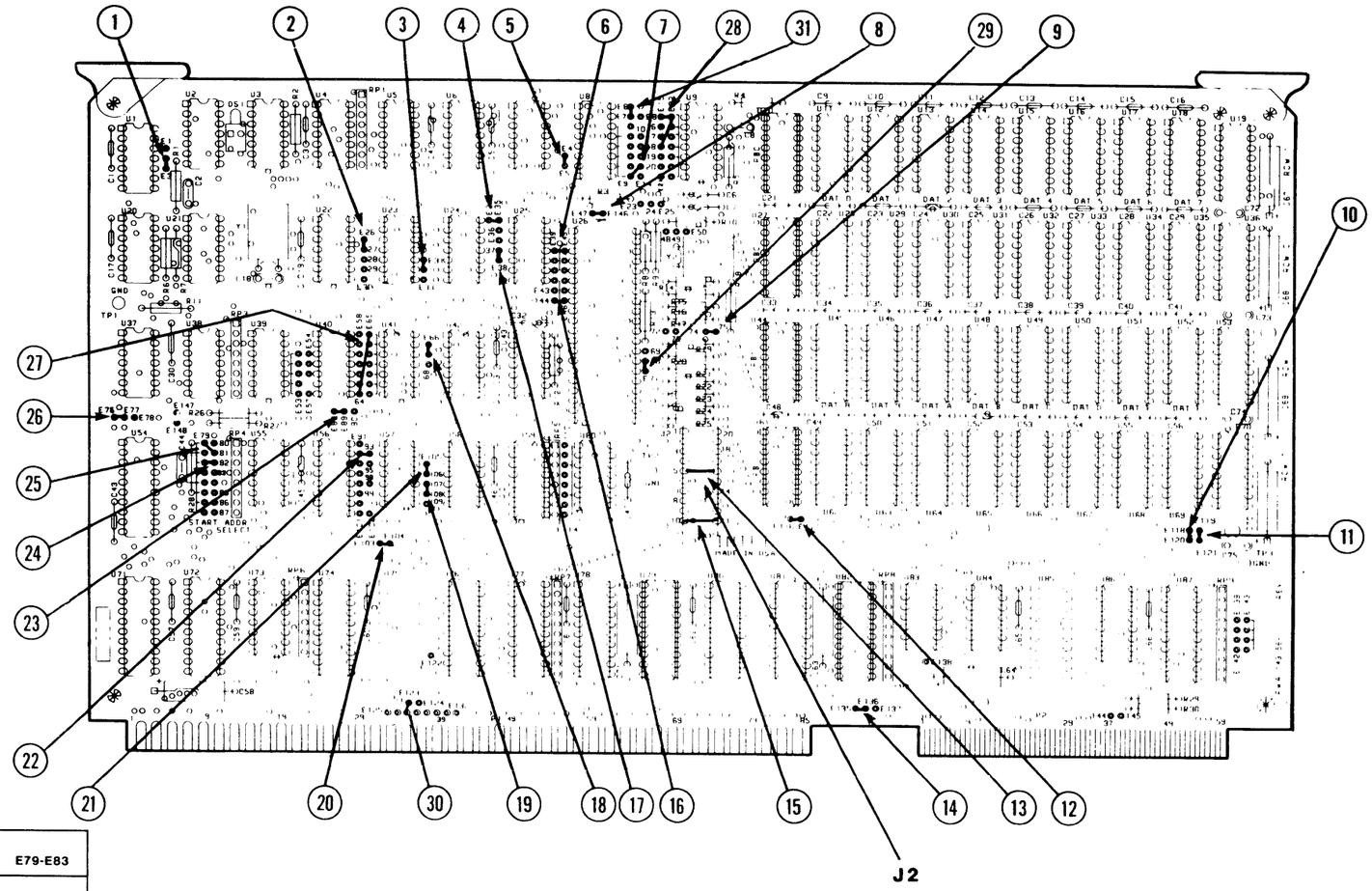
Figure 4-10. Series IV, SPU Board Jumper Configurations

iSBC 056 RAM Board Jumper Configurations

Jumper Connection	Location	Signal Name
E2-E3	1	NORMAL WRITE
E4-E5	5	PARITY FLAG MULTIBUS
E6-E7	31	GND B1/OP1 INPUT OF 8202A
E9-E13	7	ADR10-RAS2 TO 158
E15-E22	28	ADR11-B0 TO 8202A
E18-E22	28	ADR11-B0 TO 8202A
E23-EE24	7	25 MHZ TO 8202A
E26-E27	2	PARITY BANK 1 WRITE
E31-E32	3	PARITY BANK 0 WRITE
E34-E35	4	WRITE BANK SEL 0, 1
E37-E38	17	WRITE BANK SEL 0, 1
E39-E45	6	ADRE, ADRD-8202A AL0, AH0
E44-E46	16	ADRE, ADRD-8202A AL0, AH0
E47-E146	8	SUPPLY
E51-E52*	32	XACK, AACK GEN
E64-E65	27	100NS XACK DELAY-CAS
E66-E67	18	ONBOARD ERROR INDICATOR/INTERRUPT
E70-A**	29	+12V TO OP ON 8202A
E76-E77	26	PARITY PORT CS/GATING
E88-E89	23	ERROR LED GEN
E92-E93	22	MEMORY DECODE ENABLE
E94-E95	22	MEMORY DECODE ENABLE
E97-E98	22	MEMORY DECODE ENABLE
E101-E102	20	MEMORY DECODE ENABLE
E103-E104	20	PARITY ERROR CS/ENABLE
E105-E106	21	PARITY ERROR CS/ENABLE
E107-E108	19	PARITY ERROR CS/ENABLE
E116-E117	12	POWER SUPPLY
E118-E120	10	POWER SUPPLY
E119-E121	11	POWER SUPPLY
E123-E127	30	ERROR INT
E135-E136**	14	POWER SUPPLY CONFIGURATION

*JUMPER ONLY ON PBA #143514

**FOR PBA #143156-045; A=71 AND E135-E136 IS IN.
FOR PBA #143156-059; A=69 AND E135-E136 IS OUT.



Memory Jumper Table
(Locations 24 and 25)

Memory Address	E79-E80	E79-E81	E79-E82	E79-E83
0XXXX				
1				X
2			X	
3			X	X
4		X		
5		X		X
6		X	X	
7		X	X	X
8	X			
9	X			X
A	X		X	
B	X		X	X
C	X	X		
D	X	X		X
E	X	X	X	
FXXXX	X	X	X	X

-002 (03000 TO 08000:FFFF)
-001 (06000 TO 09000:FFFF)
-003 (UPGRADE) (0A000 TO 0D000:FFFF)

X = Jumper Installed

CBA = 133292

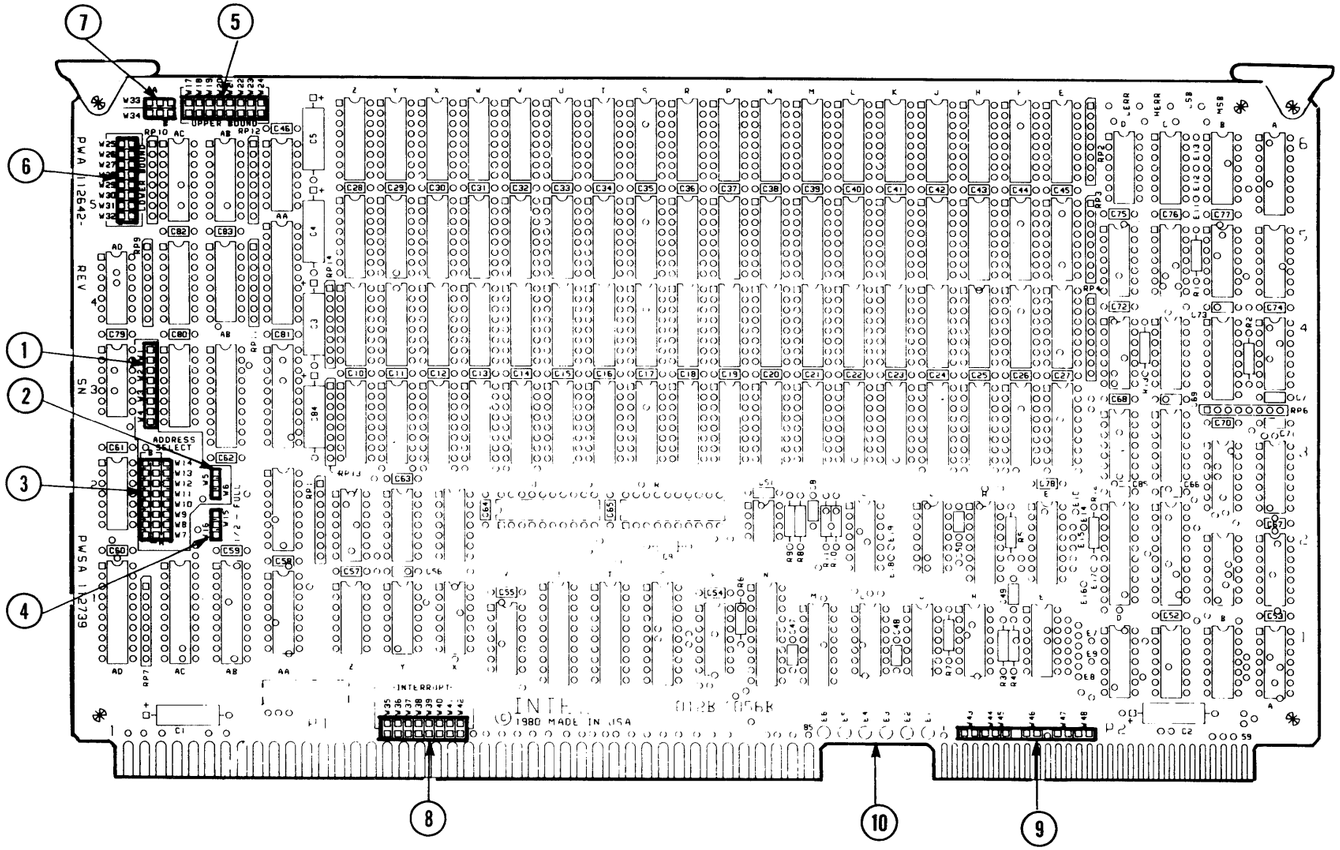
121757-24

Figure 4-11. Series IV, 056 RAM Board Jumper Configurations

iSBC-012B System Jumper Configuration

Suitcase Jumper Position	Board Location Pointer	Signal Name	System Configuration		
			-001	-002	-003
W1	1	I/O AD00	Y	Y	Y
W2	1	I/O AD01	N	N	N
W3	1	I/O AD02	N	N	N
W4	1	I/O AD03	N	N	N
W5	2	I/O AD06	N	N	N
W6	2	I/O AD06	Y	Y	Y
W7A	3	16-BIT I/O ADDRESS	Y	Y	Y
W8A	3	16-BIT I/O ADDRESS	Y	Y	Y
W9A	3	16-BIT I/O ADDRESS	Y	Y	Y
W10A	3	16-BIT I/O ADDRESS	Y	Y	Y
W11A	3	16-BIT I/O ADDRESS	Y	Y	Y
W12A	3	16-BIT I/O ADDRESS	Y	Y	Y
W13A	3	16-BIT I/O ADDRESS	Y	Y	Y
W14A	3	16-BIT I/O ADDRESS	Y	Y	Y
W15	4	FULL (512 KB)	Y	Y	Y
W16	4	1/2 (256 KB)	N	N	N
W17	5	UPPER BOUND AD0E	N	N	N
W18	5	UPPER BOUND AD0F	N	N	N
W19	5	UPPER BOUND AD10	Y	N	N
W20	5	UPPER BOUND AD11	N	Y	Y
W21	5	UPPER BOUND AD12	Y	N	Y
W22	5	UPPER BOUND AD13	N	N	N
W23	5	UPPER BOUND AD14	Y	Y	Y
W24	5	UPPER BOUND AD15	Y	Y	Y
W25	6	LOWER BOUND AD0E	Y	Y	Y
W26	6	LOWER BOUND AD0F	Y	Y	Y
W27	6	LOWER BOUND AD10	N	Y	N
W28	6	LOWER BOUND AD11	N	N	N
W29	6	LOWER BOUND AD12	Y	N	Y
W30	6	LOWER BOUND AD13	Y	Y	Y
W31	6	LOWER BOUND AD14	Y	Y	Y
W32	6	LOWER BOUND AD15	Y	Y	Y
W33A	7	BANK SELECT AD16	Y	Y	Y
W34A	7	BANK SELECT AD17	Y	Y	Y
W35	8	INT7	N	N	N
W36	8	INT6	N	N	N
W37	8	INT5	Y	Y	Y
W38	8	INT4	N	N	N
W39	8	INT3	N	N	N
W40	8	INT2	N	N	N
W41	8	INT1	N	N	N
W42	8	INT0	N	N	N
W43	9	OFF-BOARD REFRESH	N	N	N
W44	9	OFF-BOARD REFRESH	N	N	N
W45	9	OFF-BOARD REFRESH	N	N	N
W46	9	OFF-BOARD REFRESH	N	N	N
W47	9	PARITY 1	N	N	N
W48	9	PARITY 2	N	N	N

HARD WIRED JUMPERS (callout 10)
From E2 to E3 } (Normal Power)
From E5 to E6 }



NOTE

The iSBC-012 RAM memory board is received with suitcase jumpers installed in each position. Prior to installing the board into the system, make certain the suitcase jumpers are installed in (Y)/removed from (N) the board as required for the System Configuration in which it is to be used.

-001 indicates system without SPU.
address: 03000 (0H) to 0A000 (FFFFH)
-002 indicates system with SPU.
address: 06000 (0H) to 0D000 (FFFFH)
-003 indicates system being upgraded.
address: 03000 (0H) to 09000 (FFFFH)

CBA = 134198

121757-25

Figure 4-12. Series IV, 012 RAM Board Jumper Configurations

CHAPTER 5
SERVICE INFORMATION

5.1 Introduction

This chapter provides basic troubleshooting information and instructions on how to obtain service and repair assistance.

5.2 Basic Troubleshooting

When the mainframe is powered up, ac power is routed through the line filter and power circuit breaker switch to the main (multioutput) power supply, the 5 Vdc auxiliary power supply and the three cooling fans. The system normally completes the power-up tests in less than 1 minute and then displays the sign-on message. Completion of the power-up test indicates that most of the system is operational. Following either initial installation, installation of an option or a suspected malfunction, the supplemental tests should be performed to provide more thorough testing (i.e., testing circuits that were not tested by the power-up diagnostic tests). If the system should fail to boot up properly, or if any of the tests should fail, refer to the troubleshooting guide in Table 5-1.

To use Table 5-1, locate the symptom (first column) that most closely defines the error or malfunction. Then read across the table to see what the possible cause or causes could be and what corrective action is required. After performing the corrective actions, restore the system to its operating configuration (top cover in place, etc.) and repeat the failed tests. If the test continues to fail, request assistance from Intel Customer Service (refer to Paragraph 5.4).

If the power-up tests that check memory (on-board RAM) fail, the system will display an error message that contains a location number.

For example:

Test Name Error/Error Information

RAM DATA BUS RIPPLE AT *xxxx:yyyy*, EXP.DATA *zz*H, REC.DATA *uu*H

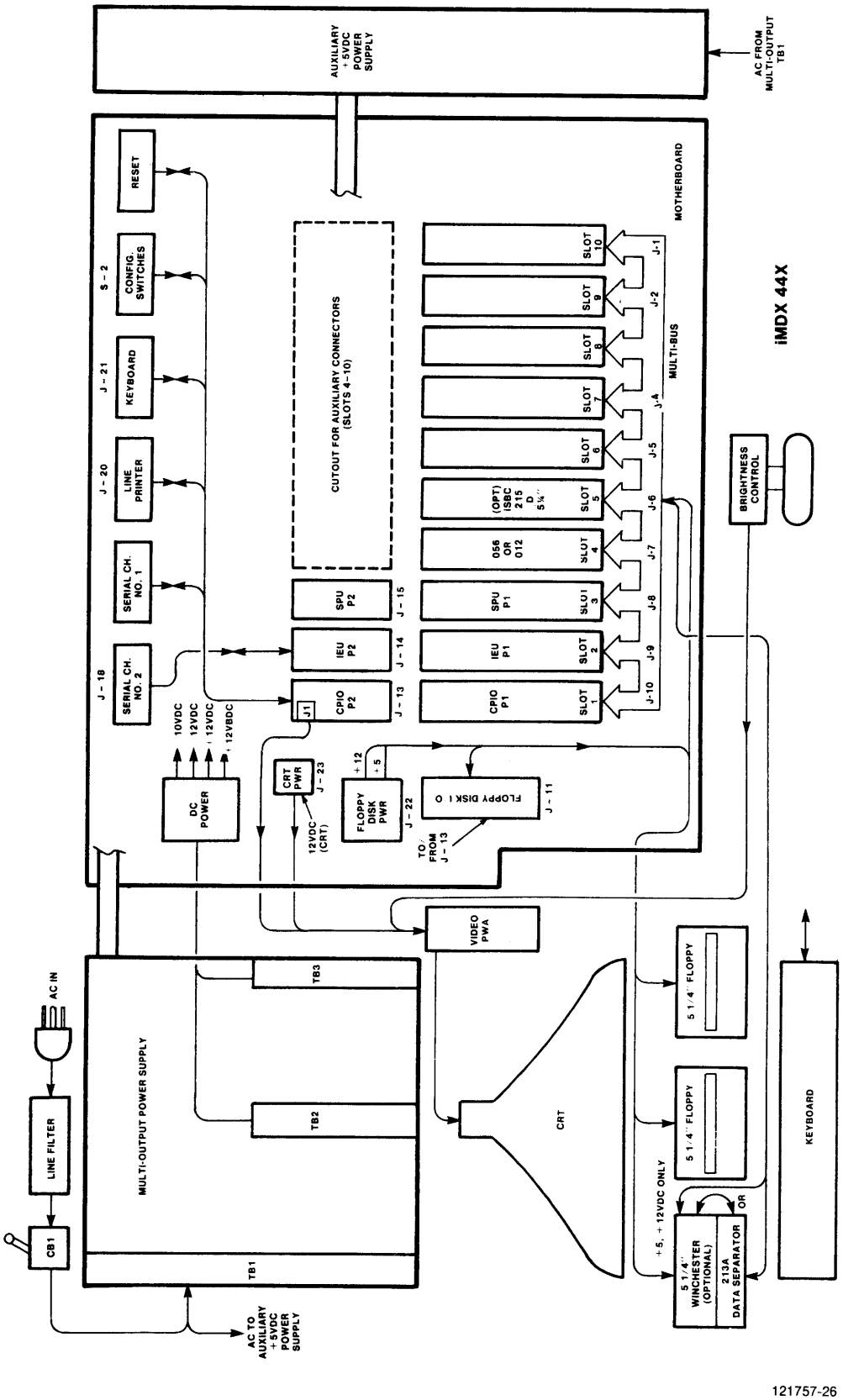
The location number, *xxxx:yyyy*, indicates the memory address where the failure occurred. This is useful information in determining the cause of failure. If assistance from Intel Customer Service is subsequently requested, be sure to include the location information in the trouble report.

Table 5-1. Series IV, Troubleshooting Guide

Symptom	Probable Cause	Corrective Action
Fans not running at power up.	No ac voltage at power outlet.	Check power outlet for proper voltage connection.
	Circuit breaker.	1. Turn circuit breaker off then on again. 2. If circuit breaker was tripped and trips a second time, disconnect the ac power plug and request assistance from Intel Customer Service (refer to Paragraph 5.4).
	Loose connections at power supply terminal TB1.	1. Turn circuit breaker off and unplug ac plug. 2. Remove top cover (refer to Paragraph 4.6). 3. Check connections to TB1 on the power supply behind the CRT (see Figures 4-4 and 5-2).
Failed power-up	CPIO failure.	1. Reseat CPIO board (refer to Paragraph 4.9).
	Board jumpers missing or in wrong place.	2. Check jumpers on CPIO board (see Figure 4-8). 3. If problem remains, request assistance from Intel Customer Service (refer to Paragraph 5.4).
Failed optional board (such as SPU) power-up.	Loose connection between optional board and motherboard	1. Reseat board that failed (refer to Paragraph 4.9). 2. If problem continues, contact the Intel Service Representative.
System will neither boot from diskette nor run supplemental tests.	Configuration switch settings not correct.	Check configuration switches (refer to Paragraph 3.3).
	Loose cable connection.	1. Turn off circuit breaker and remove ac plug from outlet. 2. Remove top cover (refer to Paragraph 4.6). 3. Check floppy disk cable connections J11 and J22 (see Figures 5-1 and 4-1). 4. Reseat CPIO board (refer to Paragraph 4.9).
CRT Blank.	CRT failure.	1. Turn off circuit breaker and remove ac power from outlet. 2. Remove top cover (refer to Paragraph 4-6). 3. Check power cable that connects between the motherboard (J23) and the video circuit board and the CPIO board (J1) top edge connector (see Figure 5-1). 4. Reseat the CPIO board (refer to Paragraph 4-9).
	Brightness Control	Adjust the brightness control.
Failed 0000H to 0003H of SIVDIA	CPIO board failure.	1. Reseat CPIO board (refer to Paragraph 4.9). 2. Check CPIO jumpers (see Figure 4-8).

Table 5-1. Series IV, Troubleshooting Guide (Cont'd)

Symptom	Probable Cause	Corrective Action
Failed Test 0007H of SIVDIA.	Keyboard failure.	Check keyboard connection to the mainframe.
Failed Test 0008H od SIVDIA	IEU board failure.	Reseat IEU board (refer to Paragraph 4.9).
Failed Test 0009H of SIVDIA	Line printer failure.	Reseat CPIO Board (refer to Paragraph 4.9).
Failed Test 000AH of SIVDIA	Line printer failure	1. Check line printer for ac power connection, power switch on and printer operation (refer to printer manual). 2. Check line printer cable connection to the mainframe (J20). 3. Reseat the CPIO board (refer to Paragraph 4.9). 4. Check CPIO board jumpers (see Figure 4-8).
Failed Test 000BH and/or 000CH of SIVDIA.	Floppy disk media or disk drive failure.	1. Turn off circuit breaker and remove ac plug from outlet. 2. Remove top cover (refer to Paragraph 4.6). 3. Check floppy disk cable connections J11 and J22 (see Figures 5-1 and 4-1). 4. Check that drive being tested has a formatted diskette inserted for Test 000BH.
Failed Test 0015H	CPIO board failure.	Reseat the CPIO board (refer to Paragraph 4.9).
Failed a Test between 0000H and 0006H of SIVEXT.	Loose connection between IEU board and motherboard.	1. Reseat the IEU board (refer to Paragraph 4.9). 2. Check IEU board jumpers (see Figure 4-9).
Failed a Test between 0008H and 000EH of SIVEXT.	Expansion (extra) memory failure.	1. Remove the failing memory board (refer to Paragraph 4.8). 2. Check failing memory board for proper jumper configuration (see Figure 4-10). 3. Reinstall and retest memory board.
Failed a Test between 000DH and 0014H of SIVDIA	SPU board failure.	1. Reseat the SPU board (refer to Paragraph 4.9). 2. Check SPU board jumpers (see Figure 4-10).
	CPIO board failure.	1. Reseat CPIO board refer to Paragraph 4.9). 2. Check CPIO board jumpers (see Figure 4-8).



121757-26

Figure 5-1. Series IV, Mainframe Internal Connections

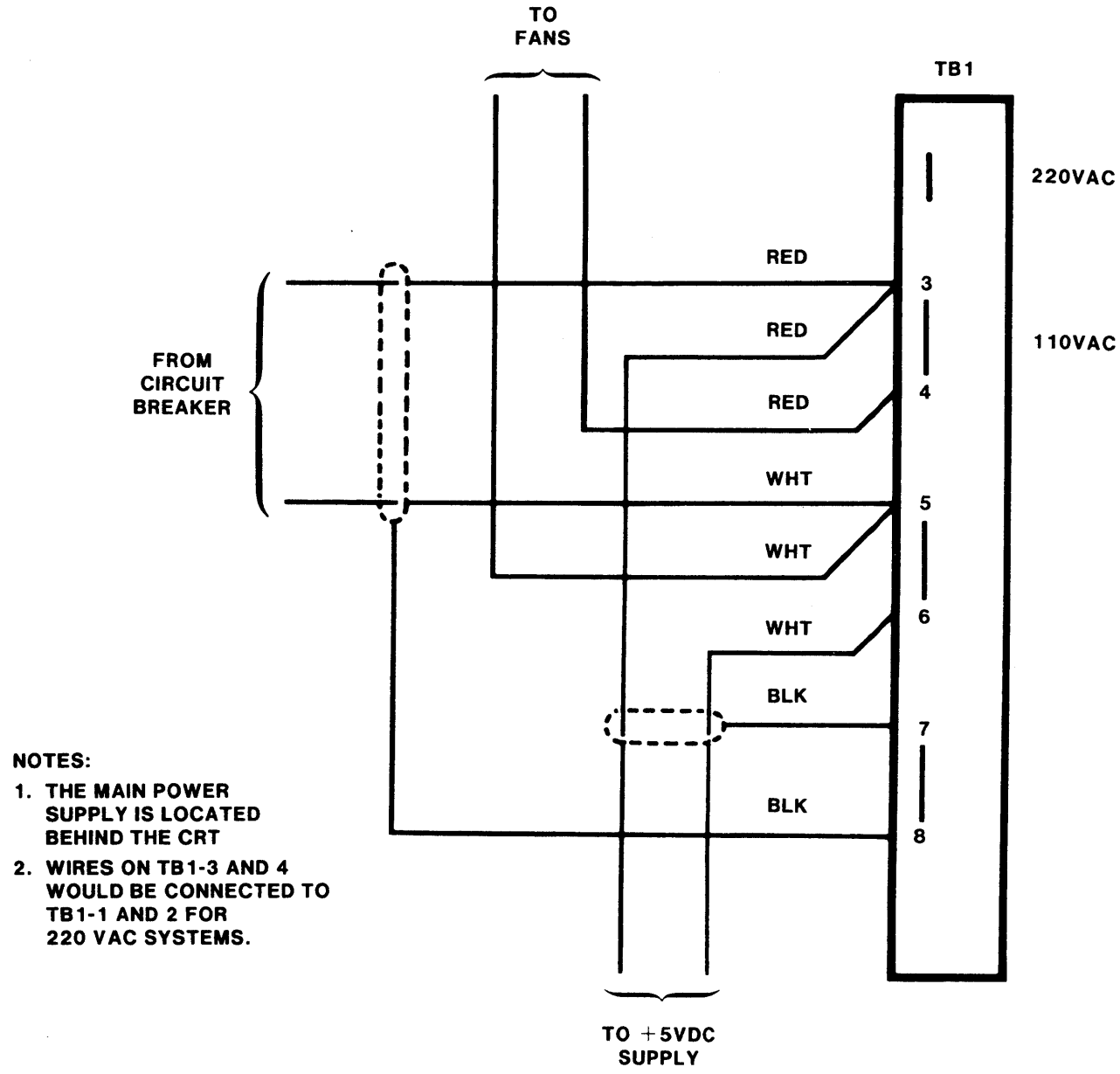


Figure 5-2. Series IV, AC Power Connections to the Main Power Supply

5.3 Preventive Maintenance

The mainframe and keyboard require the same care and maintenance given to electronic computer terminal equipment. To maintain the equipment properly, perform the following steps routinely in manufacturing environments:

1. Clean the outside of the mainframe cabinet and keyboard with any high quality (non-solvent, non-abrasive) office cleaner such as 3M Desk and Office Cleaner, Catalog No. 573 or equivalent and a soft, lint-free cloth. Use cleaners sparingly. Always apply cleaners to the cloth first and then wipe equipment.

DO NOT allow cleaners to enter mainframe or keyboard openings or get into the disk drives. If cleaners get on printed circuit boards or in the disk drive, short circuits or serious damage could occur.

2. Clean the CRT screen with any high quality, nonabrasive glass cleaner, such as Windex and a soft, lint-free cloth. Use cleaner sparingly. Always apply cleaner to the cloth first and then wipe the screen.
3. Check around the equipment for obstructions that may impede proper air circulation for cooling.
4. Perform the Supplemental Tests to ensure that all circuits are functioning (refer to Paragraphs 3.14).

5.4 Service and Repair Assistance

The best service for your Intel product will be provided by an Intel Customer Engineer. These trained professionals provide prompt, efficient on-site installation, preventive maintenance or corrective maintenance services that will keep your equipment in the best possible operating condition.

Your Intel Customer Engineer can provide the service you need through a prepaid service contract on an hourly charge basis. For further information, contact your local Intel office.

When it is impossible for you to use the services of an Intel Customer Engineer or when Intel service is not available in your local area, you can contact the Intel Service Center directly at one of the following numbers:

Telephone:

From Alaska, Arizona or Hawaii call:
(602) 869-4600

From the following U.S. areas call:

Northwest	(602) 869-4951
Southwest	(602) 869-4023
Midwest	(602) 869-4392
Northeast	(602) 869-4045
Southeast	(602) 869-4950

TWX: 910-951-1330

NOTE

Customers outside of the Continental United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.

5.5 Reshipment

Never return equipment to Intel for service or repair before you contact an Intel Customer Engineer or the Intel Service Center.

If return of your equipment is necessary, you will be given a Repair Authorization Number, shipping instructions and other important information that will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment or if the product is out of warranty, a purchase order is necessary in order for the Intel Service Center to make the repair.

Before shipping the system: recalibrate the heads by running the diagnostic test SIVDIA, Floppy Disk Seek Test 000BH. If possible protect the heads by inserting the original floppy drive head protector (cardboard insert), into the drive. Close the latch.

When preparing the product for shipment to the Service Center, use the original factory packaging material if available. If the original packaging is not available, wrap the product in a cushioning material such as Air Cap SD-240, manufactured by the Sealed Air Corporation, Hawthorne, N. J. (or equivalent) and enclose in a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling and ship it to the address specified by the Intel Service Center.

APPENDIX A
TEST MONITOR COMMAND DESCRIPTIONS

A.1 Introduction

This chapter explains the Test MONitor (TMON) commands of the DETMON syntax. TMON is the interface software between the user and the diagnostics. TMON provides a test suite, not a debug environment.

Each TMON command is described, shown with proper syntax and demonstrated with examples as actually used.

The TMON commands are:

CLEAR
DEBUG
DESCRIBE
ERRONLY
EXIT
IGNORE
RECOGNIZE
RESET
SUMMARY
TEST

A.2 Console Interface

The console interface supports the standard ISIS console commands. This section contains a table (Table A-1) of keyboard control special action characters. These commands provide the CE with error correction, display and I/O control between the keyboard and the monitor.

The symbol "∧" preceeding a term, means that the "CNTL" key must be held down before the term key is pushed.

A.3 TMON Definitions

This section contains a one page definition of each command in the TMON test suite. Each page contains a flowchart of the actual key-in language, examples of use, a description of what the command actually does and pertinent error message information.

Table A-1. Series IV, Console Control Commands

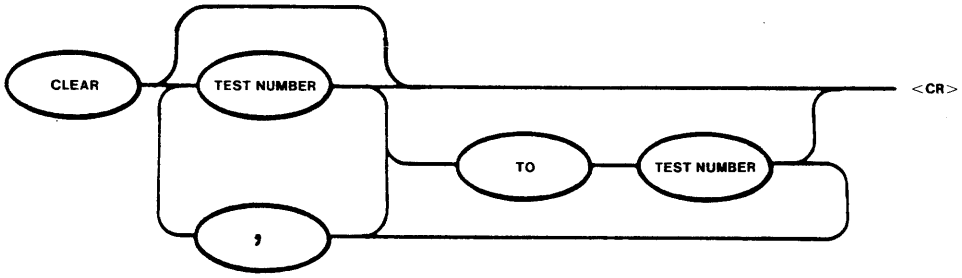
Symbol	Definition	Description
RUBOUT		Delete the previous character
∧Z	CONTROL Z	End of file
∧X	CONTROL X	Delete the entire input line
∧R	CONTROL R	Echo and correct the input line

Table A-1. Series IV, Console Control Commands (Cont'd)

Symbol	Definition	Description
∧P	CONTROL P	Input next character literally
∧C	CONTROL C	Delete input line and abort command instruction
<cr>	CARRIAGE RETURN	End of line
LF	LINE FEED	End of line
∧S	CONTROL S	Pause the display of the output
∧Q	CONTROL Q	Resume the display of the output

CLEAR

Syntax



121757-30

Examples

*CLEAR<cr>

or

*CLE<cr>

or

*CLEAR 10<cr>

Description

Clear purges the test summary table. The summary indicates the number of times the diagnostic(s) has been executed and how many times each test failed. This command destroys the old results. The Clear command will also list the numbers of all ignored tests.

Error Message

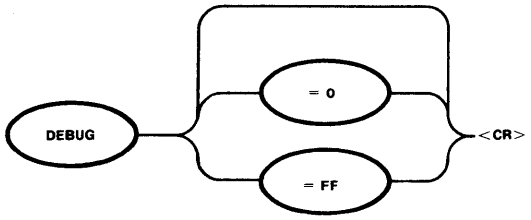
TEST OUT OF RANGE

The command specified a test outside the range of the test description table.

(*) DETMON curser, signals the user that development system will accept input from the keyboard.

DEBUG

Syntax



121757-31

Examples

1. *DEBUG<cr>
   0000H

   Displays current DEBUG status.

2. *DEB=FF<cr>

   Sets the DEBUG switch to display error messages.

3. *DEB=0<cr>

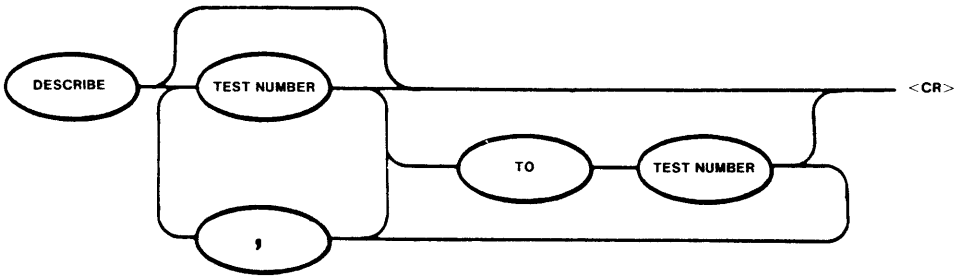
   Clears the DEBUG switch to suppress error messages.

Description

The Debug command is used to set, clear, or display the status of the Debug switch. When DEBUG=FFH, error messages are displayed. When DEBUG=00H (default), error messages are suppressed.

DESCRIBE

Syntax



121757-32

Examples

*DES<cr>

or

*DESCRIBE 0,1,2<cr>

or

*DESCRIBE 1 TO 20<cr>

Description

DESCRIBE displays the name and test number of all test programs incorporated in the diagnostic. The names of the tests indicate that portion of the circuitry being tested. This command describes all tests if no particular test(s) is specified.

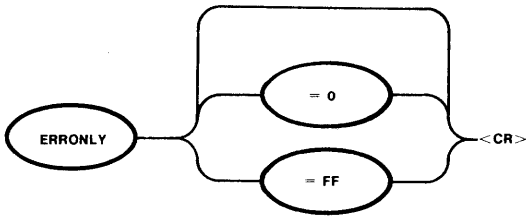
Error Message

TEST OUT OF RANGE

A specified test exceeds the top range of the test description table.

ERRONLY

Syntax



121757-33

Examples

1. *ERRONLY<cr>
   0000H

   Displays the current ERRONLY status.

2. *ERR=1<cr>

   Sets the ERRONLY switch to suppress messages for tests that pass.

3. *ERR=0<cr>

   Clears the ERRONLY switch to display messages for tests that pass.

Description

The Erronly command is used set, clear, or display the status of the Erronly switch. When ERRONLY=1, all messages for tests that pass are suppressed. When ERRONLY=0 (default), messages for tests that pass are displayed.

EXIT

Syntax

121757-34

Examples

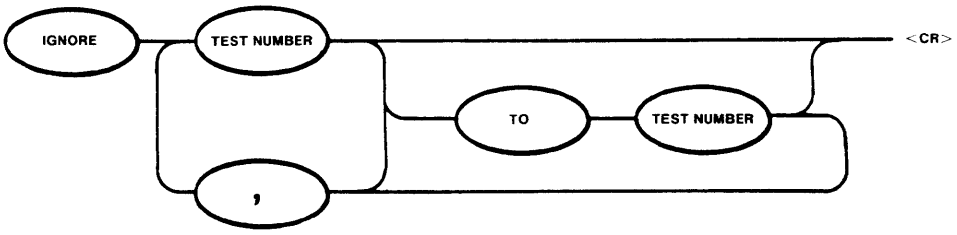
```
*EXIT<cr>
>
```

Description

This command transfers control from TMON back to the Software Diagnostic Monitor, indicated by the prompt ">". Once under the control of the Software Diagnostic Monitor, another test suite can be loaded or a directory of the test suite names can be displayed.

IGNORE

Syntax



121757-35

Examples

```
*IGNORE 2,4,12 TO 17<cr>
```

Description

Ignore disables any undesired test in the test descriptor table. The ignored test will not be tested. The "RECOGNIZE" command enables those tests previously ignored (see RECOGNIZE test.).

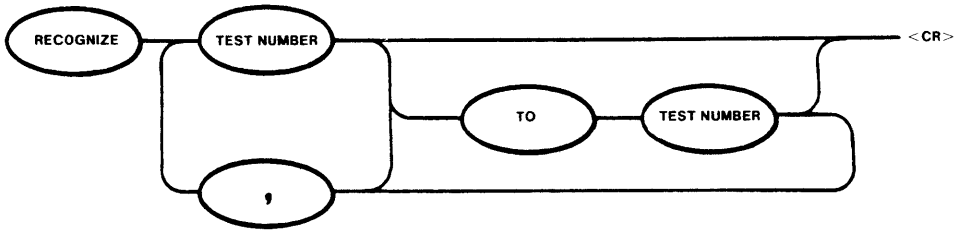
Error Message

TEST OUT OF RANGE

A test has been specified which exceeds the top range of the test description table.

RECOGNIZE

Syntax



121757-36

Examples

*REC 2, 4, 6 TO 8<cr>

*REC<cr>

Description

This command enables tests previously ignored (see IGNORE). Recognize enables all tests unless a range is specified, and then enables only those tests specified.

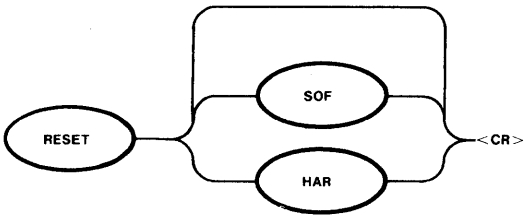
Error Message

TEST OUT OF RANGE

A test has been specified which is greater than the index of the last test in the test description table.

RESET

Syntax



121757-37

Examples

1. *RESET SOF

   Resets the software only.

2. *RESET HAR

   Resets the hardware only.

3. *RESET

   Resets both the hardware and the software.

Description

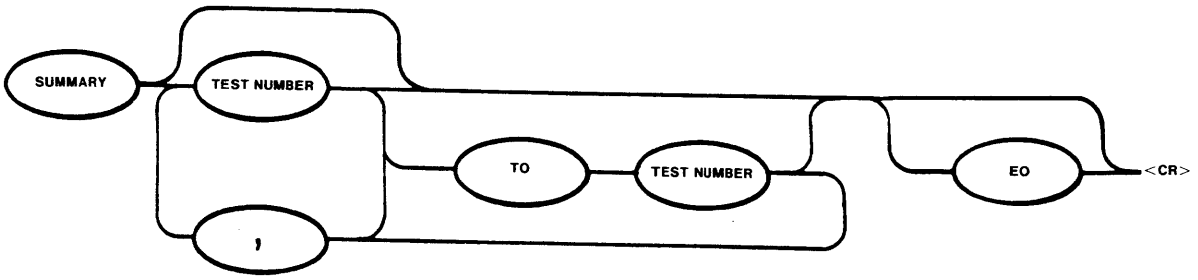
The Reset command allows the user to either reset both the hardware and software to their initial state or to specify one or the other. When Reset is typed without specifying hardware or software, the software will first be reset followed by the hardware.

NOTE

Executing this command will reset all 'V' variables to their default values.

SUMMARY

Syntax



121757-38

Examples

```
*SUMMARY EO<cr>
0001H FOO TEST                    0000H PASSED 0003 FAILED <===

*SUM 1<cr>
0001H FOO TEST                    0000H PASSED 0003 FAILED <===
```

Description

This command displays and labels both ignored and active tests. For active tests, the log indicates the number and name of the test, followed by the number of times it was tested and the number of passes and failures. Ignored tests are labeled "IGNORED".

The error only (EO) in the syntax will cause the summary to display only those tests that have failed.

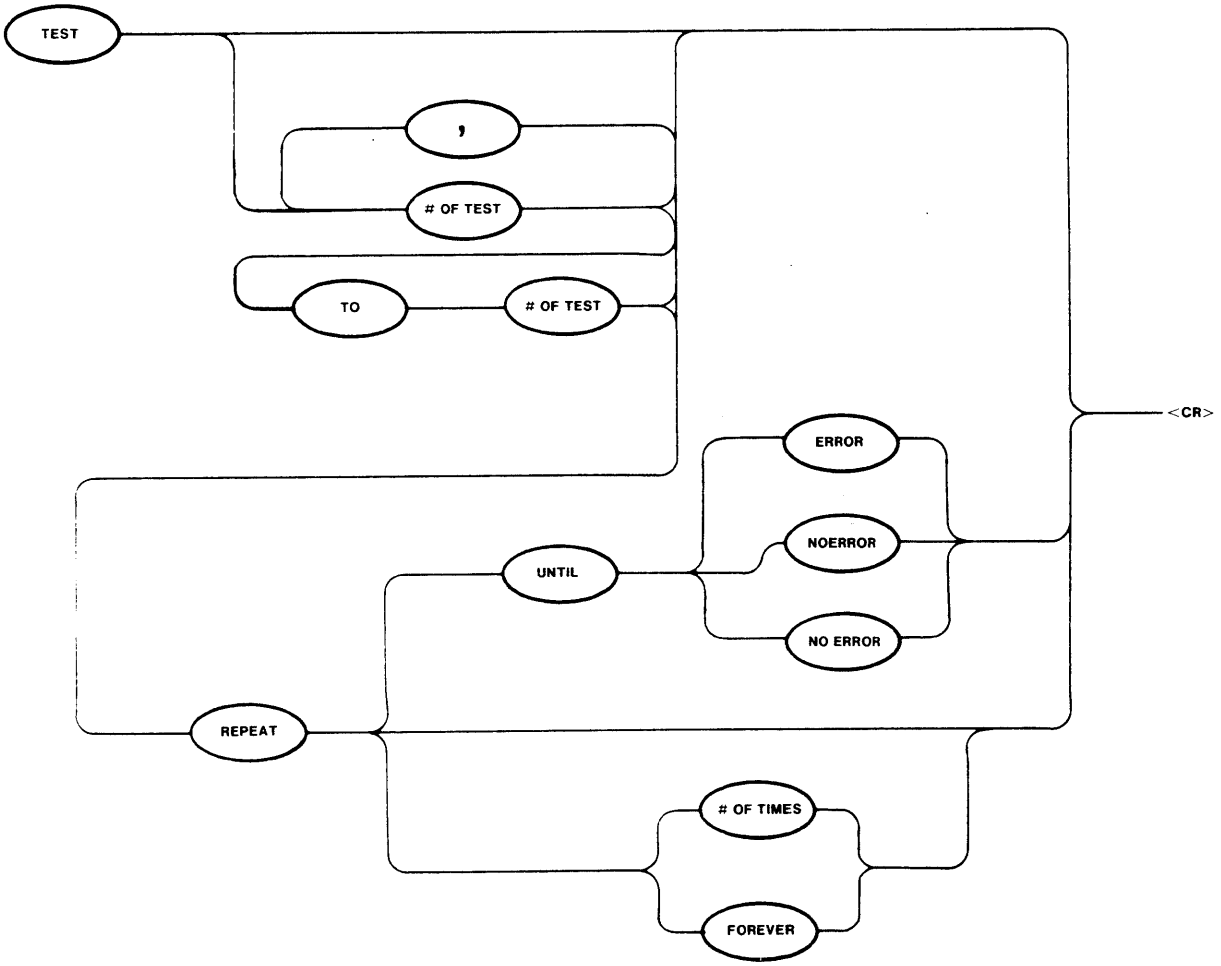
Error Message

TEST OUT OF RANGE

A test exceeding the top range of the test description table has been specified.

TEST

Syntax



121757-39

Examples

1. *T<cr>

   All non-ignored tests are tested.

2. *T 1,3 TO 40 REP FOR<cr>

   Tests 1 and 3 to 40 are displayed until interrupted by user with ^C.

3. *T 12 REP ON ERROR<cr>

   The results of Test 12 are displayed as long as it fails.

4. *T REPEAT 500T<cr>

   All non-ignored tests are executed 500 times.

Description

The test command initiates the test sequence and displays the name of the test(s) executed and the results of that testing. Tests may be activated by the "RECOGNIZE" and deactivated by the "IGNORE" command. Ignored tests are not tested.

The test range entered by the user, determines which active tests are executed.

Error Message

TEST OUT OF RANGE

A test has been specified which exceeds the top range of the test description table.

A.4 TMON Error Message

TMON displays an error message whenever the desired TMON command addresses a location outside the user defined limits. The error message interpretation is:

TEST OUT OF RANGE

A test has been specified which is greater than the last test indicated in the test description table. This error message is associated with the IGNORE, CLEAR, RECOGNIZE, SUMMARY, TEST and DESCRIBE commands.

APPENDIX B
iMDX-434 (SPU Processor Board) UPGRADE KIT INSTALLATION

B.1 Introduction

This appendix provides instructions for installing the iMDX-434 (SPU Processor Board) Upgrade Kit, P/N 133604, into the Series IV. The instructions herein apply to both an initial installation and to a previously installed system.

B.2 Unpacking and Inspection

Inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is heavily damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present, or if the carton is opened and the contents are damaged, keep the carton, contents and packing material for the agents inspection.

Inventory the contents of the upgrade kit to verify it contains:

Intel Part Number	Description
124893	SPU Processor Board
133639	iNDX.S41 (SIV/4 Operating System Diskette)

B.3 SPU Installation

The SPU is installed as follows:

1. Turn OFF the Series IV circuit breaker and disconnect the ac power plug from the wall outlet.
2. Remove the Series IV top cover (see Paragraph 4.6).
3. Remove the RFI Shield or Hold Down Bracket (see Figure 4-6).
4. The SPU board, as shipped from the factory, is ready for use in both the Series IV and NRM systems (no rejumpering required). Simply install it in Slot 3.
5. Proceed to Paragraph B.4 and reconfigure the memory as required depending upon the type memory board installed.

B.4 System Memory Address Reconfiguration

When the SPU board is installed in a Series IV system having one iSBC-056 Memory board, the system memory addressing scheme is to be reconfigured as follows:

Board	Addressing
CPIO	Page 2 (2000:0000-FFFF)
(Empty)	Page 3 (3000:0000-FFFF)
SPU	Pages 4 & 5 (4000:0000 thru 5000:FFFF)
056	Pages 6,7,8 & 9 (6000:0000 thru 9000:FFFF)
IEU	Page A (A000:0000-FFFF)

When the SPU board is installed in a Series IV system having one iSBC-012B Memory board, the system memory addressing scheme is to be reconfigured as follows:

Board	Addressing
CPIO	Page 2 (2000:0000-FFFF)
(Empty)	Page 3 (3000:0000-FFFF)
SPU	Pages 4 & 5 (4000:0000 thru 5000:FFFF)
012B	Pages 6 thru D (6000:0000 thru D000:FFFF)
IEU	Page E (E000:0000-FFFF)

The sequence in which to reconfigure the Series IV memory scheme, regardless of memory board installed, is as follows:

1. Determine which memory board is installed in your system and therefore which scheme above is to be followed throughout this procedure. Also, take into consideration any additional memory boards that have been or will be added.
2. Remove the iSBC-056 or iSBC-012B board from Slot 4. Rejumper it as required using the jumper information provided on its respective figure (Figure 4-11 for iSBC-056 and Figure 4-12 for iSBC-012B). If a second memory board has been or is to be installed, rejumper it also at this time using the jumper information provided on its respective figure.
3. Install the memory board into Slot 4. Any unused slot may be selected if a second memory board is to be used (memory boards do not have an interrupt priority).
4. Remove the IEU board from Slot 2 and rejumper it to be addressed at the first available page above the memory board(s) (see Figures 4-7 and 4-9).
5. Replace the IEU board into Slot 2.
6. Replace the RFI Shield or Hold Down Bracket removed earlier.
7. Replace the top cover.
8. Connect the ac power plug to the wall outlet and then proceed to Paragraph B.5.

B.5 Power-Up Tests

Perform the following.

1. Open the latch(es) to the floppy drive(s).
2. Set the Configuration switches to select floppy drive #0 as the boot device (see Table 3-1).
3. Power-up the system by setting the circuit breaker (left rear of system) to the on (1) position.
4. Observe that the fans are running and, after approximately 40 seconds, the following message is displayed on the CRT screen:

NOTE

The "FLOPPY DRIVE NOT READY" and "Error 3800" messages are normal messages when the floppy drive #0 latch is open.

```
SERIES IV SYSTEM POWER-UP DIAGNOSTIC, Vx.y
CPIO PHASE I ..................................... / PASSED
CPIO PHASE II .................................... / PASSED
FLOPPY DRIVE NOT READY
SPU .............................................. / INSTALLED
iSBC-550 ..................................... NOT INSTALLED
IEU .............................................. / INSTALLED
CPIO/SPU MULTIBUS TEST ........................... / PASSED

SIV Boot Vx.y
Mini-floppy dr.0
-device failure
Error 3800

Attempt to reboot from : Mon88
SERIES IV CPIO MONITOR Vx.y          (where x.y is the release level)
```

5. Proceed to Paragraph B.6.

B.6 SIVDIA Tests

The SIVDIA test suite is executed by performing the following:

1. Insert the Supplemental Diagnostic diskette in floppy drive #0 and then close the drive latch.
2. Press the RESET switch to boot the system and then observe the CRT screen for the following message:

```
SERIES IV Diagnostic Monitor, Vx.y
>
```

3. To load the SIVDIA Test Suite and the Test Monitor (TMON), type:

```
>ZSIVDIA<cr>
```

4. The LED on floppy drive #0 lights for approximately 30-40 seconds, and then the following message is displayed:

```
File SIVDIA loaded

SERIES IV CPIO, SPU DIAGNOSTIC TEST Vx.y
*
```

NOTE

The SIVDIA test suite is now loaded into the system.

5. To ignore the "FLOPPY DISK SEEK TEST", 000BH, and run the pre-selected SIVDIA tests, type:

```
*IGN B<cr>
*T<cr>
```

6. After approximately 30 to 40 seconds, the following message should be displayed:

```
0004H ***IGNORED ***
0005H ***IGNORED ***
0006H ***IGNORED ***
0007H ***IGNORED ***
000AH ***IGNORED ***
000BH ***IGNORED ***
000CH ***IGNORED ***
```

```
0000H CPIO CPU TEST                                    PASSED
0001H CPIO 8259A INTERRUPT TEST                        PASSED
0002H CPIO SOFTWARE INTERRUPT TEST                     PASSED
0003H CPIO FAILSAFE TIMER TEST                         PASSED
0008H IEU RAM REFRESH TEST                             PASSED
0009H CPIO RAM REFRESH TEST                            PASSED
000DH SPU WAKE UP TEST                                 PASSED
000EH SPU CPU TEST                                     PASSED
000FH NORMAL W/R SPU MEMORY TEST                       PASSED
0010H SPU CHECK BITS MEMORY MARCH TEST                 PASSED
0011H SPU MEMORY REFRESH                               PASSED
0012H SPU MEMORY REFRESH ECC OFF                       PASSED
0013H CPIO WAKE UP                                     PASSED
0014H CPIO FIFO                                        PASSED
0015H CPIO 8089 OPERATION TIME-OUT                     PASSED
*
```

7. To transfer control back to the Series IV Diagnostic Monitor, type:

```
*EXIT<cr>
```

8. When transfer of control to the Series IV Diagnostic Monitor has completed, the Series IV prompt will be displayed:

```
>
```

9. Proceed to Paragraph B.7.

B.7 SIVEXT Tests

The SIVEXT test suite is executed by performing the following:

1. Load both the SIVEXT test suite and the Test Monitor (TMON) by typing:

```
>ZSIVEXT<cr>
```

2. The LED on floppy drive #0 lights for approximately 30-40 seconds, and then the following message is displayed:

```
File SIVEXT loaded
SERIES IV IEU, EXTRA RAM DIAGNOSTIC TEST Vx.y
*
```

3. To run the pre-selected SIVDIA tests, type:

```
*T<cr>
```

NOTE

The SIVEXT test suite is now loaded into the system and begins testing the IEU and extra memory boards and because of the T <cr> command, finishes after the tests run one time.

4. After approximately 1 to 1.5 minutes, the following message should be displayed:

```
0007H ***IGNORED ***
000DH ***IGNORED ***
000EH ***IGNORED ***
0000H 8085 RESET                                       PASSED
0001H 8085 CPU                                         PASSED
0002H FIFO CONTROL PORT                                PASSED
0003H IEU 8259A INTERRUPT                              PASSED
```

```
0004H FAILSAFE TIMER                          PASSED
0005H TIMER COUNT                             PASSED
0006H IEU CONTROL PORT                        PASSED
0008H EXTRA RAM DATA BUS RIPPLE               PASSED
0009H EXTRA RAM ADDRESS BUS RIPPLE            PASSED
000AH EXTRA RAM MARCH                         PASSED
000BH EXTRA RAM REFRESH                       PASSED
000CH EXTRA RAM ADDRESS                       PASSED
*
```

5. Remove the SIV Supplemental Diagnostic diskette from floppy drive #0.
6. If this option was installed as part of an initial system installation, return to Figure 2-1, Series IV Installation Procedure Flowchart, for installation procedures for any other optional features and/or software. If this option was performed as an upgrade to a previously installed system, proceed to Paragraph B.8.

B.8 iNDX Operating System Copy

1. Insert the iNDX.S41 Diskette into floppy drive #0.
2. Boot the system from the iNDX.S41 Diskette and logon as SUPERUSER with a password of either PASSME or the password previously assigned by the Customer.
3. Once you are logged on, copy the iNDX.S41 software to the Winchester Drive by entering the following command:

```
SUBMIT /INDX.S41/SYSTEM.COPY (p0,sdt,vrd)<cr>
```

where:

p0	=	source system device name (FL0 or FL1)
sdt	=	target system device name (WM0, WD0 or HD0)
vrd	=	target Winchester volume name. This volume name already exists for the system device (typically W0, W, WINI0, etc.).

NOTE

The copying process will take approximately 5 to 10 minutes.

4. After the SYSTEM COPY has completed, logoff the system.
5. Set the Configuration switches to boot from the System Hard Disk Drive.
6. Boot and logon the system.
7. Use some of the iNDX commands to verify that the system is operating normally. If everything appears normal, the upgrade is complete; otherwise, recheck each step. If normal system operation cannot be achieved, refer to Chapter 5 for servicing information.

APPENDIX C
SECOND-USER TERMINAL INSTALLATION

C.1 Introduction

This appendix provides instructions for connecting a second-user terminal to Serial Channel 1 on the Series IV. With the installation of a second-user terminal, a Series IV that is equipped with software release 2.8 or higher can be partitioned to support two users interactively in either standalone or network mode. User 1 operates in memory Partition 1 and accesses the system from the system keyboard. User 2 operates in memory Partition 2 and accesses the system via the second-user terminal.

C.2 Restrictions

The following restrictions apply when operating the Series IV in Multi-user mode:

1. When User 2 is using Serial Channel 2 as a console, Serial Channel 1 can be used for any additional serial transfer requirements.
2. Either User 1 or User 2 has access to ISIS-IV, but not both. User 1 specifies which user has access to ISIS-IV when executing SYSGEN or REGION. If ISIS is assigned to User 2, the following steps must be performed to reallocate it to User 1:
   a. User 2 logs off the system by entering:

      ```
      LOGOff Exit<cr>
      ```

   b. User 1 then reassigns ISIS-IV and reselects Multi-user mode to bring up the second partition again via the REGION CUSP.
3. The use of ICE or other debugging tools in conjunction with Multi-user or Toggle modes is not supported.

C.3 Parts Required

The cable (P/N 108197) used to connect the terminal to Serial Channel 1 is supplied in the Accessory Kit (P/N 124480) shipped with the Series IV system. Refer to Table 4-4 for Serial Channel 1 pin assignments. To complete this installation, the user must supply an asynchronous terminal to be used as the second-user workstation. Refer to Appendix A of the *Intellec Series IV Operating and Programming Guide*, Order no. 121753, for information regarding the terminal requirements and configuration instructions.

C.4 Preinstallation Testing

Before connecting the second-user terminal, refer to Chapter 3 of this manual and perform the supplemental diagnostics to verify that the Series IV is operating correctly.

C.5 Installation Procedure

To connect a terminal to Serial Channel 1 on the Series IV perform the following procedure:

1. LOGOFF the Series IV.
2. Turn off the Series IV circuit breaker and disconnect the ac power plug from the power outlet to prevent accidental power turn-on.
3. Locate the Serial Channel 1 connector on the Series IV. Refer to Figure C-1.
4. Connect the J1 connector of the shielded 10-foot terminal cable (P/N 108197) supplied in the Series IV Accessory Kit to Serial Channel 1 on the Series IV. See Figure C-2 for the cable pinout.
5. Ensure that the terminal that is to be connected to the Series IV is powered down.
6. Connect the P1 connector of the terminal cable to the RS232C connector on the terminal.
7. Power up the terminal.

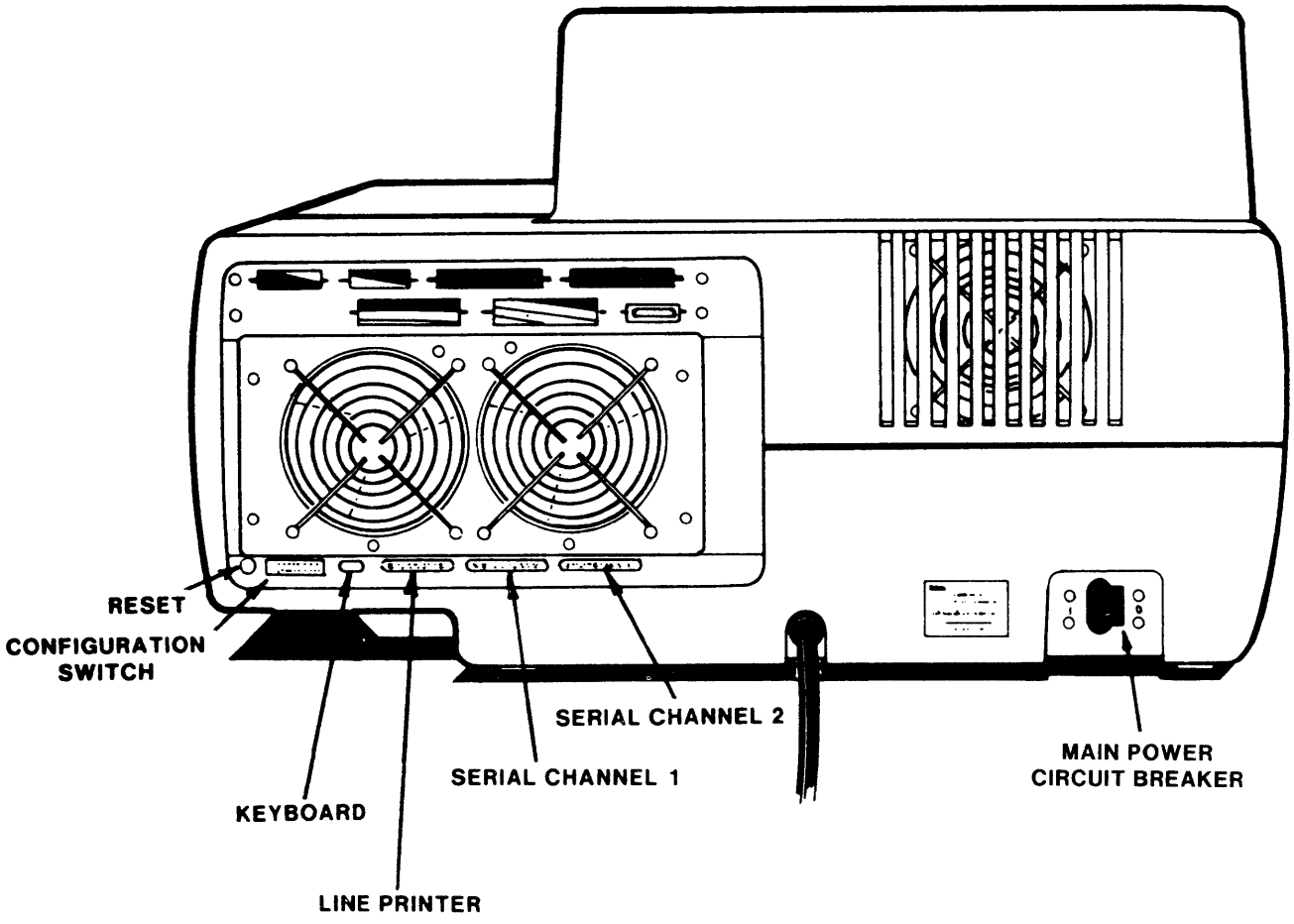


Figure C-1. Series IV, Rear View

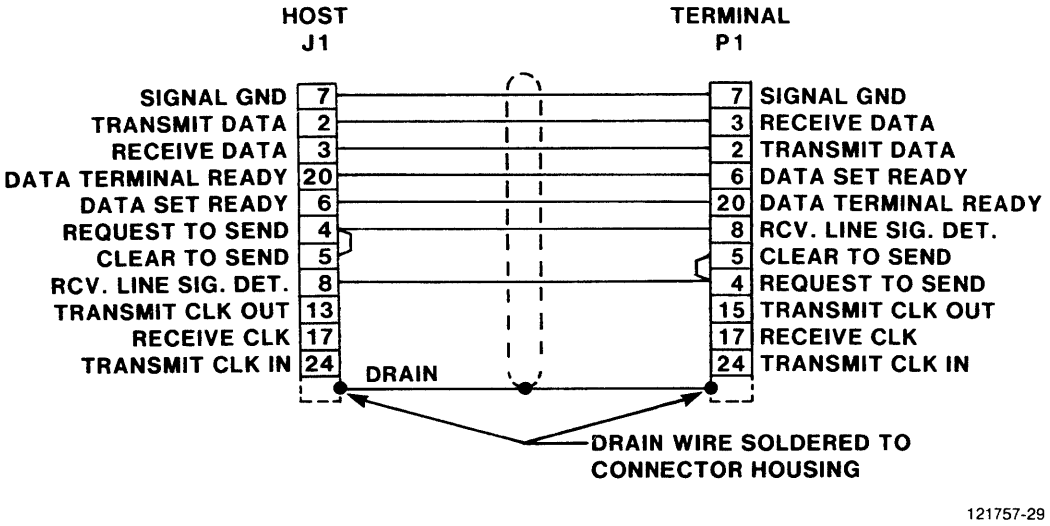


Figure C-2. Terminal Cable Pinout

8. Connect the Series IV unit ac power plug to a three-conductor power outlet, power up the system and perform the test procedures in Chapter 3 of this manual to verify that the system operation has not been affected.

9. Terminal configuration files are provided with Release 2.8 software for a number of terminals. Refer to Appendix D in the *Intellec Series IV Operating and Programming Guide*, Order no. 121753, for the list of available files. If a file is not provided for the terminal that has been installed, create a terminal configuration file as instructed in Appendix D of the *Operating and Programming Guide.*

10. Execute the STTY and REGION CUSPs or SYSGEN (workstation options 6-11). If SYSGEN is used, activate Multi-user mode in option 6 and define the terminal capabilities by specifying the terminal configuration file in option 11. Refer to the *Intellec Series IV Operating and Programming Guide* for a standalone system or the *NDS-II Network Resource Manager User's Guide*, Order no. 134300 if the Series IV is to be utilized as a network workstation.

11. If SYSGEN is executed, reset the Series IV (standalone mode) or NRM (network mode). The configuration information added during SYSGEN is not modified until the system has been rebooted. If STTY and REGION were used, it is not necessary to reset the system to enter configuration information.

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