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MCS-80 T.M.
USER'S MANUAL
(WITH INTRODUCTION TO MCS-85 T.M.)

OCTOBER 1977

8080

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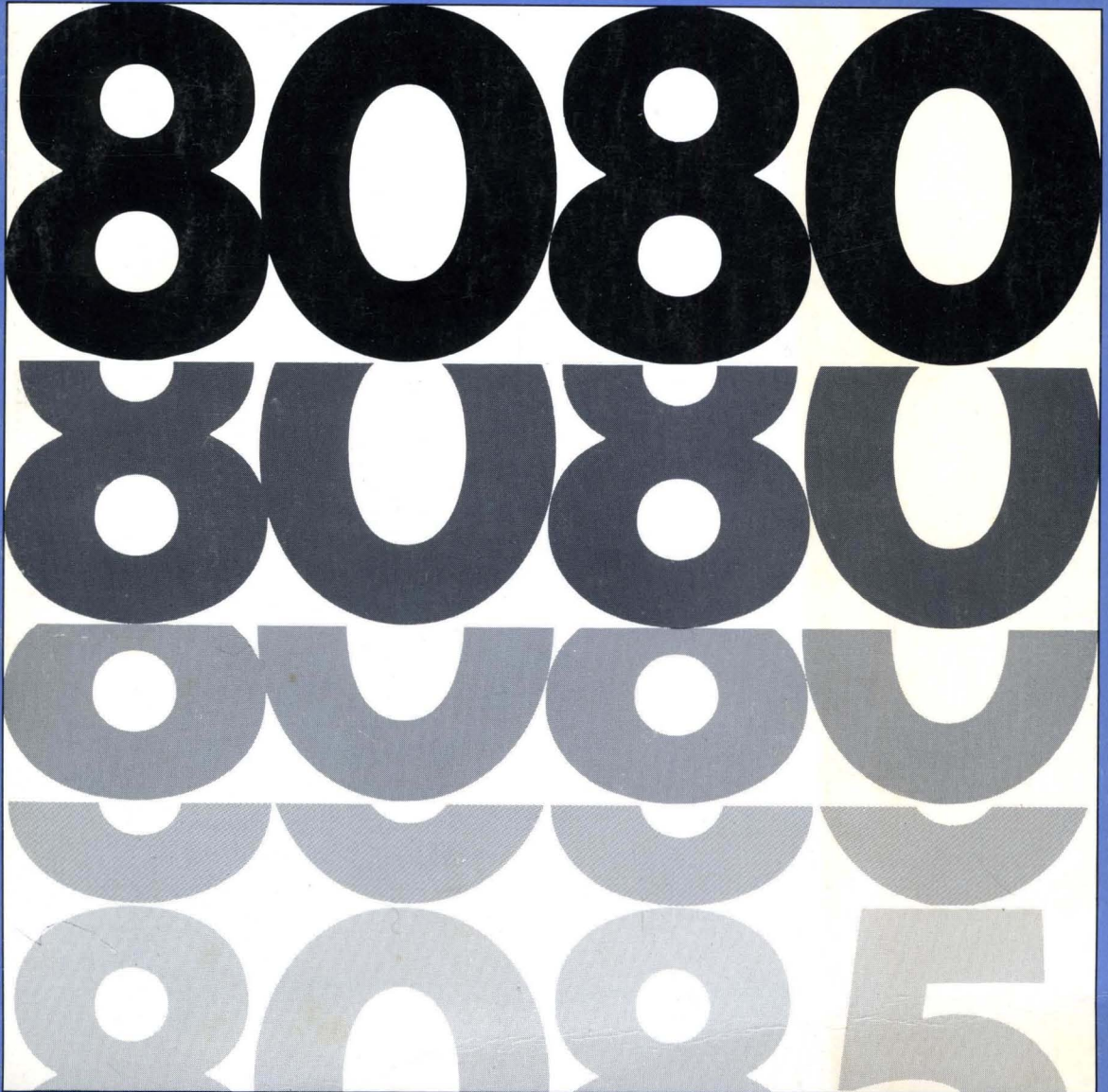
MCS-80™ USER'S MANUAL

(WITH INTRODUCTION TO MCS-85™)

The MCS-80™ family of microcomputer components has been greatly expanded since the last version of the MCS-80 manual was published in September, 1975. Over the last two years, expansion of MCS-80 family devices, coupled with the best system development support in the industry, have made Intel's 8080A the industry standard microprocessor.

Now Intel introduces the MCS-85 family, an evolutionary system based around the third generation 8085 microprocessor. MCS-85 has all the features of an MCS-80 system with higher performance and lower cost. MCS-85, the next industry standard for new designs.

Over forty microcomputer components are described in detail in this manual. Among the newest are:

8251A	Improved Programmable Communication Interface
8253	Programmable Interval Timer
8255A	Improved Programmable Peripheral Interface
8257	Programmable DMA Controller
8259	Programmable Interrupt Controller
8279	Programmable Keyboard/Display Controller
2716	2K x 8 EPROM, 5 Volt Only
2114	1K x 4 Static RAM
2116	16K x 1 Dynamic RAM
8085	5 Volt Advanced 8080 Processor
8155/56	Combination 256x8 Static RAM, 22 I/O Lines, 14-bit Counter
8355	Combination 2K x 8 ROM, 16 I/O Lines
8755	Combination 2K x 8 EPROM (5 Volt), 16 I/O Lines

intel® Microcomputers. First from the beginning.

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INTRODUCTION

INTRODUCTION

Since their inception, digital computers have continuously become more efficient, expanding into new applications with each major technological improvement. The advent of minicomputers enabled the inclusion of digital computers as a permanent part of various process control systems. Unfortunately, the size and cost of minicomputers in "dedicated" applications has limited their use. Another approach has been the use of custom built systems made up of "random logic" (i.e., logic gates, flip-flops, counters, etc.). However, the huge expense and development time involved in the design and debugging of these systems has restricted their use to large volume applications where the development costs could be spread over a large number of machines.

Today, Intel offers the systems designer a new alternative ... **the microcomputer**. Utilizing the technologies and experience gained in becoming the world's largest supplier of LSI memory components, Intel has made the power of the digital computer available at the integrated circuit level. Using the n-channel silicon gate MOS process, Intel engineers have implemented the fast (2 μs. cycle) and powerful (72 basic instructions) 8080 microprocessor on a single LSI chip. When this processor is combined with memory and I/O circuits, the computer is complete. Intel offers a variety of random-access memory (RAM), read-only memory (ROM) and shift register circuits, that combine with the 8080 processor to form the MCS-80 microcomputer system, a system that can directly address and retrieve as many as 65,536 bytes stored in the memory devices.

The 8080 processor is packaged in a 40-pin dual in-line package (DIP) that allows for remarkably easy interfacing. The 8080 has a 16-bit address bus, a 8-bit bidirectional data bus and fully decoded, TTL-compatible control outputs. In addition to supporting up to 64K bytes of mixed RAM and ROM memory, the 8080 can address up to 256 input ports and 256 output ports; thus allowing for virtually unlimited system expansion. The 8080 instruction set includes conditional branching, decimal as well as binary arithmetic,

logical, register-to-register, stack control and memory reference instructions. In fact, the 8080 instruction set is powerful enough to rival the performance of many of the much higher priced minicomputers, yet the 8080 is upward software compatible with Intel's earlier 8008 microprocessor (i.e., programs written for the 8008 can be assembled and executed on the 8080).

In addition to an extensive instruction set oriented to problem solving, the 8080 has another significant feature—SPEED. In contrast to random logic designs which tend to work in parallel, the microcomputer works by sequentially executing its program. As a result of this sequential execution, the number of tasks a microcomputer can undertake in a given period of time is directly proportional to the execution speed of the microcomputer. The speed of execution is the limiting factor of the realm of applications of the microcomputer. The 8080, with instruction times as short as 2 μsec., is an order of magnitude faster than earlier generations of microcomputers, and therefore has an expanded field of potential applications.

The architecture of the 8080 also shows a significant improvement over earlier microcomputer designs. The 8080 contains a 16-bit stack pointer that controls the addressing of an external stack located in memory. The pointer can be initialized via the proper instructions such that any portion of external memory can be used as a last in/first out stack; thus enabling almost unlimited subroutine nesting. The stack pointer allows the contents of the program counter, the accumulator, the condition flags or any of the data registers to be stored in or retrieved from the external stack. In addition, multi-level interrupt processing is possible using the 8080's stack control instructions. The status of the processor can be "pushed" onto the stack when an interrupt is accepted, then "popped" off the stack after the interrupt has been serviced. This ability to save the contents of the processor's registers is possible even if an interrupt service routine, itself, is interrupted.

	CONVENTIONAL SYSTEM	PROGRAMMED LOGIC
Product definition		Simplified because of ease of incorporating features
System and logic design	Done with logic diagrams	Can be programmed with design aids (compilers, assemblers, editors)
Debug	Done with conventional Lab Instrumentation	Software and hardware aids reduce time
PC card layout		Fewer cards to layout
Documentation		Less hardware to document
Cooling and packaging		Reduced system size and power consumption eases job
Power distribution		Less power to distribute
Engineering changes	Done with yellow wire	Change program

Table 0-1. The Advantages of Using Microprocessors

ADVANTAGES OF DESIGNING WITH MICROCOMPUTERS

Microcomputers simplify almost every phase of product development. The first step, as in any product development program, is to identify the various functions that the end system is expected to perform. Instead of realizing these functions with networks of gates and flip-flops, the functions are implemented by encoding suitable sequences of instructions (programs) in the memory elements. Data and certain types of programs are stored in RAM, while the basic program can be stored in ROM. The microprocessor performs all of the system's functions by fetching the instructions in memory, executing them and communicating the results via the microcomputer's I/O ports. An 8080 microprocessor, executing the programmed logic stored in a single 2048-byte ROM element, can perform the same logical functions that might have previously required up to 1000 logic gates.

The benefits of designing a microcomputer into your system go far beyond the advantages of merely simplifying product development. You will also appreciate the profit-making advantages of using a microcomputer in place of custom-designed random logic. The most apparent advantage is the significant savings in hardware costs. A microcomputer chip set replaces dozens of random logic elements, thus reducing the cost as well as the size of your system. In addition, production costs drop as the number of individual components to be handled decreases, and the number of complex printed circuit boards (which are difficult to layout, test and correct) is greatly reduced. Probably the most profitable advantage of a microcomputer is its flexibility for change. To modify your system, you merely re-program the memory elements; you don't have to redesign the entire system. You can imagine the savings in time and money when you want to upgrade your product. Reliability is another reason to choose the microcomputer over random logic. As the number of components decreases, the probability of a malfunctioning element likewise decreases. All

of the logical control functions formerly performed by numerous hardware components can now be implemented in a few ROM circuits which are non-volatile; that is, the contents of ROM will never be lost, even in the event of a power failure. Table 0-1 summarizes many of the advantages of using microcomputers.

MICROCOMPUTER DESIGN AIDS

If you're used to logic design and the idea of designing with programmed logic seems like too radical a change, regardless of advantages, there's no need to worry because Intel has already done most of the groundwork for you. The INTELLEC®Microcomputer Development System provides flexible, inexpensive and simplified methods for OEM product development. The INTELLEC MDS provides RAM program storage making program loading and modification easier, a display and control console for system monitoring and debugging, standard TTY and CRT interfaces, in-circuit emulation capability (ICE-80), PROM programming capability using the Universal PROM Programmer module, and a standard software package (System Monitor, Assembler and Text Editor). In addition to the standard software package available with the INTELLEC MDS Intel offers a resident PL/M compiler. Intel's Microcomputer Division is always available to provide assistance in every phase of your product development.

Intel also provides complete documentation on all their hardware and software products. In addition to this User's Manual, there are the:

- PL/M-80 Programming Manual
- 8080/8085 Assembly Language Programming Manual
- INTELLEC MDS Operator's Manual
- INTELLEC MDS Hardware Reference Manual
- ICE-80 Operator's Manual
- ICE-80 Hardware Reference Manual
- 8080 User's Program Library "Insite"

APPLICATIONS EXAMPLE

The 8080 can be used as the basis for a wide variety of calculation and control systems. The system configurations for particular applications will differ in the nature of the peripheral devices used and in the amount and the type of memory required. The applications and solutions described in this section are presented primarily to show how microcomputers can be used to solve design problems. The 8080 should not be considered limited either in scope or performance to those applications listed here.

Consider an 8080 microcomputer used within an automatic computing scale for a supermarket. The basic machine has two input devices: the weighing unit and a keyboard, used for function selection and to enter the price per unit of weight. The only output device is a display showing the total price, although a ticket printer might be added as an optional output device.

The control unit must accept weight information from the weighing unit, function and data inputs from the keyboard, and generate the display. The only arithmetic function to be performed is a simple multiplication of weight times rate.

The control unit could probably be realized with standard TTL logic. State diagrams for the various portions could be drawn and a multiplier unit designed. The whole design could then be tied together, and eventually reduced to a selection of packages and a printed circuit board layout. In effect, when designing with a logic family such as TTL, the designs are "customized" by the choice of packages and the wiring of the logic.

If, however, an 8080 microcomputer is used to realize the control unit (as shown in Figure 0-1), the only "custom" logic will be that of the interface circuits. These circuits are usually quite simple, providing electrical buffering for the input and output signals.

Instead of drawing state diagrams leading to logic, the system designer now prepares a flow chart, indicating which input signals must be read, what processing and computations are needed, and what output signals must be produced. A program is written from the flow chart. The program is then assembled into bit patterns which are loaded into the program memory. Thus, this system is customized primarily by the contents of program memory.

For this automatic scale, the program would probably reside in read-only memory (ROM), since the microcomputer would always execute the same program, the one which implements the scale functions. The processor would constantly monitor the keyboard and weighing unit, and update the display whenever necessary. The unit would require very little data memory; it would only be needed for rate storage, intermediate results, and for storing a copy of the display.

When the control portion of a product is implemented with a microcomputer chip set, functions can be changed and features added merely by altering the program in memory. With a TTL based system, however, alterations may require extensive rewiring, alteration of PC boards, etc.

The number of applications for microcomputers is limited only by the depth of the designer's imagination. We have listed a few potential applications in Table 0-2, along with the types of peripheral devices usually associated with each product.
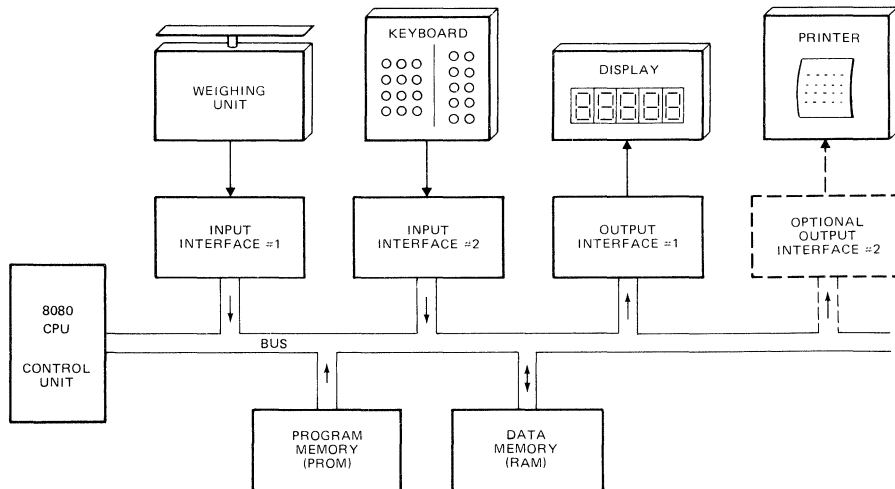
Figure 0-1. Microcomputer Application — Automatic Scale

APPLICATION	PERIPHERAL DEVICES ENCOUNTERED
Intelligent Terminals	Cathode Ray Tube Display Printing Units Synchronous and Asynchronous data lines Cassette Tape Unit Keyboards
Gaming Machines	Keyboards, pushbuttons and switches Various display devices Coin acceptors Coin dispensers
Cash Registers	Keyboard or Input Switch Array Change Dispenser Digital Display Ticket Printer Magnetic Card reader Communication interface
Accounting and Billing Machines	Keyboard Printer Unit Cassette or other magnetic tape unit "Floppy" disks
Telephone Switching Control	Telephone Line Scanner Analog Switching Network Dial Registers Class of Service Parcel
Numerically Controlled Machines	Magnetic or Paper Tape Reader Stepper Motors Optical Shaft Encoders
Process Control	Analog-to-Digital Converters Digital-to-Analog Converters Control Switches Displays

Table 0-2. Microprocessor Applications

THE FUNCTIONS OF A COMPUTER
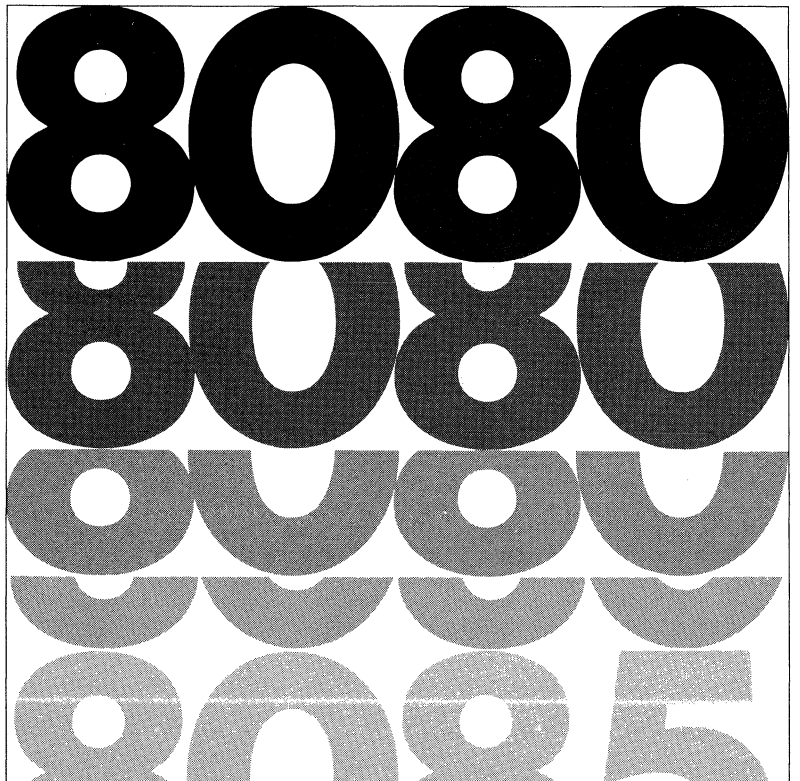
THE FUNCTIONS OF A COMPUTER

This chapter introduces certain basic computer concepts. It provides background information and definitions which will be useful in later chapters of this manual. Those already familiar with computers may skip this material, at their option.

A TYPICAL COMPUTER SYSTEM

A typical digital computer consists of:

a) A central processor unit (CPU)
b) A memory
c) Input/output (I/O) ports

The memory serves as a place to store **Instructions**, the coded pieces of information that direct the activities of the CPU, and **Data**, the coded pieces of information that are processed by the CPU. A group of logically related instructions stored in memory is referred to as a **Program**. The CPU "reads" each instruction from memory in a logically determined sequence, and uses it to initiate processing actions. If the program sequence is coherent and logical, processing the program will produce intelligible and useful results.

The memory is also used to store the data to be manipulated, as well as the instructions that direct that manipulation. The program must be organized such that the CPU does not read a non-instruction word when it expects to see an instruction. The CPU can rapidly access any data stored in memory; but often the memory is not large enough to store the entire data bank required for a particular application. The problem can be resolved by providing the computer with one or more **Input Ports**. The CPU can address these ports and input the data contained there. The addition of input ports enables the computer to receive information from external equipment (such as a paper tape reader or floppy disk) at high rates of speed and in large volumes.

A computer also requires one or more **Output Ports** that permit the CPU to communicate the result of its processing to the outside world. The output may go to a display, for use by a human operator, to a peripheral device that produces "hard-copy," such as a line-printer, to a peripheral storage device, such as a floppy disk unit, or the output may constitute process control signals that direct the operations of another system, such as an automated assembly line. Like input ports, output ports are addressable. The input and output ports together permit the processor to communicate with the outside world.

The CPU unifies the system. It controls the functions performed by the other components. The CPU must be able to fetch instructions from memory, decode their binary contents and execute them. It must also be able to reference memory and I/O ports as necessary in the execution of instructions. In addition, the CPU should be able to recognize and respond to certain external control signals, such as INTERRUPT and WAIT requests. The functional units within a CPU that enable it to perform these functions are described below.

THE ARCHITECTURE OF A CPU

A typical central processor unit (CPU) consists of the following interconnected functional units:

- Registers
- Arithmetic/Logic Unit (ALU)
- Control Circuitry

Registers are temporary storage units within the CPU. Some registers, such as the program counter and instruction register, have dedicated uses. Other registers, such as the accumulator, are for more general purpose use.

Accumulator:

The accumulator usually stores one of the operands to be manipulated by the ALU. A typical instruction might direct the ALU to add the contents of some other register to the contents of the accumulator and store the result in the accumulator itself. In general, the accumulator is both a source (operand) and a destination (result) register.

Often a CPU will include a number of additional general purpose registers that can be used to store operands or intermediate data. The availability of general purpose

registers eliminates the need to "shuffle" intermediate results back and forth between memory and the accumulator, thus improving processing speed and efficiency.

Program Counter (Jumps, Subroutines and the Stack):

The instructions that make up a program are stored in the system's memory. The central processor references the contents of memory, in order to determine what action is appropriate. This means that the processor must know which location contains the next instruction.

Each of the locations in memory is numbered, to distinguish it from all other locations in memory. The number which identifies a memory location is called its **Address**.

The processor maintains a counter which contains the address of the next program instruction. This register is called the **Program Counter**. The processor updates the program counter by adding "1" to the counter each time it fetches an instruction, so that the program counter is always current (pointing to the next instruction).

The programmer therefore stores his instructions in numerically adjacent addresses, so that the lower addresses contain the first instructions to be executed and the higher addresses contain later instructions. The only time the programmer may violate this sequential rule is when an instruction in one section of memory is a **Jump** instruction to another section of memory.

A jump instruction contains the address of the instruction which is to follow it. The next instruction may be stored in any memory location, as long as the programmed jump specifies the correct address. During the execution of a jump instruction, the processor replaces the contents of its program counter with the address embodied in the Jump. Thus, the logical continuity of the program is maintained.

A special kind of program jump occurs when the stored program "Calls" a subroutine. In this kind of jump, the processor is required to "remember" the contents of the program counter at the time that the jump occurs. This enables the processor to resume execution of the main program when it is finished with the last instruction of the subroutine.

A **Subroutine** is a program within a program. Usually it is a general-purpose set of instructions that must be executed repeatedly in the course of a main program. Routines which calculate the square, the sine, or the logarithm of a program variable are good examples of functions often written as subroutines. Other examples might be programs designed for inputting or outputting data to a particular peripheral device.

The processor has a special way of handling subroutines, in order to insure an orderly return to the main program. When the processor receives a Call instruction, it increments the Program Counter and stores the counter's contents in a reserved memory area known as the **Stack**. The Stack thus saves the address of the instruction to be executed after the subroutine is completed. Then the processor loads the address specified in the Call into its Program Counter. The next instruction fetched will therefore be the first step of the subroutine.

The last instruction in any subroutine is a **Return**. Such an instruction need specify no address. When the processor fetches a Return instruction, it simply replaces the current contents of the Program Counter with the address on the top of the stack. This causes the processor to resume execution of the calling program at the point immediately following the original Call Instruction.

Subroutines are often **Nested**; that is, one subroutine will sometimes call a second subroutine. The second may call a third, and so on. This is perfectly acceptable, as long as the processor has enough capacity to store the necessary return addresses, and the logical provision for doing so. In other words, the maximum depth of nesting is determined by the depth of the stack itself. If the stack has space for storing three return addresses, then three levels of subroutines may be accommodated.

Processors have different ways of maintaining stacks. Some have facilities for the storage of return addresses built into the processor itself. Other processors use a reserved area of external memory as the stack and simply maintain a **Pointer** register which contains the address of the most recent stack entry. The external stack allows virtually unlimited subroutine nesting. In addition, if the processor provides instructions that cause the contents of the accumulator and other general purpose registers to be "pushed" onto the stack or "popped" off the stack via the address stored in the stack pointer, multi-level interrupt processing (described later in this chapter) is possible. The status of the processor (i.e., the contents of all the registers) can be saved in the stack when an interrupt is accepted and then restored after the interrupt has been serviced. This ability to save the processor's status at any given time is possible even if an interrupt service routine, itself, is interrupted.

Instruction Register and Decoder:

Every computer has a **Word Length** that is characteristic of that machine. A computer's word length is usually determined by the size of its internal storage elements and interconnecting paths (referred to as **Busses**); for example, a computer whose registers and busses can store and transfer 8 bits of information has a characteristic word length of 8-bits and is referred to as an 8-bit parallel processor. An eight-bit parallel processor generally finds it most efficient to deal with eight-bit binary fields, and the memory associated with such a processor is therefore organized to store eight bits in each addressable memory location. Data and instructions are stored in memory as eight-bit binary numbers, or as numbers that are integral multiples of eight bits: 16 bits, 24 bits, and so on. This characteristic eight-bit field is often referred to as a **Byte**.

Each operation that the processor can perform is identified by a unique byte of data known as an **Instruction**

Code or **Operation Code**. An eight-bit word used as an instruction code can distinguish between 256 alternative actions, more than adequate for most processors.

The processor fetches an instruction in two distinct operations. First, the processor transmits the address in its Program Counter to the memory. Then the memory returns the addressed byte to the processor. The CPU stores this instruction byte in a register known as the **Instruction Register**, and uses it to direct activities during the remainder of the instruction execution.

The mechanism by which the processor translates an instruction code into specific processing actions requires more elaboration than we can here afford. The concept, however, should be intuitively clear to any logic designer. The eight bits stored in the instruction register can be decoded and used to selectively activate one of a number of output lines, in this case up to 256 lines. Each line represents a set of activities associated with execution of a particular instruction code. The enabled line can be combined with selected timing pulses, to develop electrical signals that can then be used to initiate specific actions. This translation of code into action is performed by the **Instruction Decoder** and by the associated control circuitry.

An eight-bit instruction code is often sufficient to specify a particular processing action. There are times, however, when execution of the instruction requires more information than eight bits can convey.

One example of this is when the instruction references a memory location. The basic instruction code identifies the operation to be performed, but cannot specify the object address as well. In a case like this, a two- or three-byte instruction must be used. Successive instruction bytes are stored in sequentially adjacent memory locations, and the processor performs two or three fetches in succession to obtain the full instruction. The first byte retrieved from memory is placed in the processor's instruction register, and subsequent bytes are placed in temporary storage; the processor then proceeds with the execution phase. Such an instruction is referred to as **Variable Length**.

Address Register(s):

A CPU may use a register or register-pair to hold the address of a memory location that is to be accessed for data. If the address register is **Programmable**, (i.e., if there are instructions that allow the programmer to alter the contents of the register) the program can "build" an address in the address register prior to executing a **Memory Reference** instruction (i.e., an instruction that reads data from memory, writes data to memory or operates on data stored in memory).

Arithmetic/Logic Unit (ALU):

All processors contain an arithmetic/logic unit, which is often referred to simply as the **ALU**. The ALU, as its name implies, is that portion of the CPU hardware which performs the arithmetic and logical operations on the binary data.

The ALU must contain an **Adder** which is capable of combining the contents of two registers in accordance with the logic of binary arithmetic. This provision permits the processor to perform arithmetic manipulations on the data it obtains from memory and from its other inputs.

Using only the basic adder a capable programmer can write routines which will subtract, multiply and divide, giving the machine complete arithmetic capabilities. In practice, however, most ALUs provide other built-in functions, including hardware subtraction, boolean logic operations, and shift capabilities.

The ALU contains **Flag Bits** which specify certain conditions that arise in the course of arithmetic and logical manipulations. Flags typically include **Carry, Zero, Sign,** and **Parity**. It is possible to program jumps which are conditionally dependent on the status of one or more flags. Thus, for example, the program may be designed to jump to a special routine if the carry bit is set following an addition instruction.

Control Circuitry:

The control circuitry is the primary functional unit within a CPU. Using clock inputs, the control circuitry maintains the proper sequence of events required for any processing task. After an instruction is fetched and decoded, the control circuitry issues the appropriate signals (to units both internal and external to the CPU) for initiating the proper processing action. Often the control circuitry will be capable of responding to external signals, such as an interrupt or wait request. An **Interrupt** request will cause the control circuitry to temporarily interrupt main program execution, jump to a special routine to service the interrupting device, then automatically return to the main program. A **Wait** request is often issued by a memory or I/O element that operates slower than the CPU. The control circuitry will idle the CPU until the memory or I/O port is ready with the data.

COMPUTER OPERATIONS

There are certain operations that are basic to almost any computer. A sound understanding of these basic operations is a necessary prerequisite to examining the specific operations of a particular computer.

Timing:

The activities of the central processor are cyclical. The processor fetches an instruction, performs the operations required, fetches the next instruction, and so on. This orderly sequence of events requires precise timing, and the CPU therefore requires a free running oscillator clock which furnishes the reference for all processor actions. The combined fetch and execution of a single instruction is referred to as an **Instruction Cycle**. The portion of a cycle identified

with a clearly defined activity is called a **State**. And the interval between pulses of the timing oscillator is referred to as a **Clock Period**. As a general rule, one or more clock periods are necessary for the completion of a state, and there are several states in a cycle.

Instruction Fetch:

The first state(s) of any instruction cycle will be dedicated to fetching the next instruction. The CPU issues a read signal and the contents of the program counter are sent to memory, which responds by returning the next instruction word. The first byte of the instruction is placed in the instruction register. If the instruction consists of more than one byte, additional states are required to fetch each byte of the instruction. When the entire instruction is present in the CPU, the program counter is incremented (in preparation for the next instruction fetch) and the instruction is decoded. The operation specified in the instruction will be executed in the remaining states of the instruction cycle. The instruction may call for a memory read or write, an input or output and/or an internal CPU operation, such as a register-to-register transfer or an add-registers operation.

Memory Read:

An instruction **fetch** is merely a special memory read operation that brings the instruction to the CPU's instruction register. The instruction fetched may then call for data to be read from memory into the CPU. The CPU again issues a read signal and sends the proper memory address; memory responds by returning the requested word. The data received is placed in the accumulator or one of the other general purpose registers (not the instruction register).

Memory Write:

A memory write operation is similar to a read except for the direction of data flow. The CPU issues a write signal, sends the proper memory address, then sends the data word to be written into the addressed memory location.

Wait (memory synchronization):

As previously stated, the activities of the processor are timed by a master clock oscillator. The clock period determines the timing of all processing activity.

The speed of the processing cycle, however, is limited by the memory's **Access Time**. Once the processor has sent a read address to memory, it cannot proceed until the memory has had time to respond. Most memories are capable of responding much faster than the processing cycle requires. A few, however, cannot supply the addressed byte within the minimum time established by the processor's clock.

Therefore a processor should contain a synchronization provision, which permits the memory to request a **Wait state**. When the memory receives a read or write enable signal, it places a request signal on the processor's READY line, causing the CPU to idle temporarily. After the memory has

had time to respond, it frees the processor's READY line, and the instruction cycle proceeds.

Input/Output:

Input and Output operations are similar to memory read and write operations with the exception that a peripheral I/O device is addressed instead of a memory location. The CPU issues the appropriate input or output control signal, sends the proper device address and either receives the data being input or sends the data to be output.

Data can be input/output in either parallel or serial form. All data within a digital computer is represented in binary coded form. A binary data word consists of a group of bits; each bit is either a one or a zero. **Parallel** I/O consists of transferring all bits in the word at the same time, one bit per line. **Serial** I/O consists of transferring one bit at a time on a single line. Naturally serial I/O is much slower, but it requires considerably less hardware than does parallel I/O.

Interrupts:

Interrupt provisions are included on many central processors, as a means of improving the processor's efficiency. Consider the case of a computer that is processing a large volume of data, portions of which are to be output to a printer. The CPU can output a byte of data within a single machine cycle but it may take the printer the equivalent of many machine cycles to actually print the character specified by the data byte. The CPU could then remain idle waiting until the printer can accept the next data byte. If an interrupt capability is implemented on the computer, the CPU can output a data byte then return to data processing. When the printer is ready to accept the next data byte, it can request an interrupt. When the CPU acknowledges the interrupt, it suspends main program execution and automatically branches to a routine that will output the next data byte. After the byte is output, the CPU continues with main program execution. Note that this is, in principle, quite similar to a subroutine call, except that the jump is initiated externally rather than by the program.

More complex interrupt structures are possible, in which several interrupting devices share the same processor but have different priority levels. Interruptive processing is an important feature that enables maximum untilization of a processor's capacity for high system throughput.

Hold:

Another important feature that improves the throughput of a processor is the **Hold**. The hold provision enables **Direct Memory Access** (DMA) operations.

In ordinary input and output operations, the processor itself supervises the entire data transfer. Information to be placed in memory is transferred from the input device to the processor, and then from the processor to the designated memory location. In similar fashion, information that goes

from memory to output devices goes by way of the processor.

Some peripheral devices, however, are capable of transferring information to and from memory much faster than the processor itself can accomplish the transfer. If any appreciable quantity of data must be transferred to or from such a device, then **system throughput** will be increased by having the device accomplish the transfer directly. The processor must temporarily suspend its operation during such a transfer, to prevent conflicts that would arise if processor and peripheral device attempted to access memory simultaneously. It is for this reason that a **hold** provision is included on some processors.

Chapter 2
THE 8080 CENTRAL PROCESSING UNIT
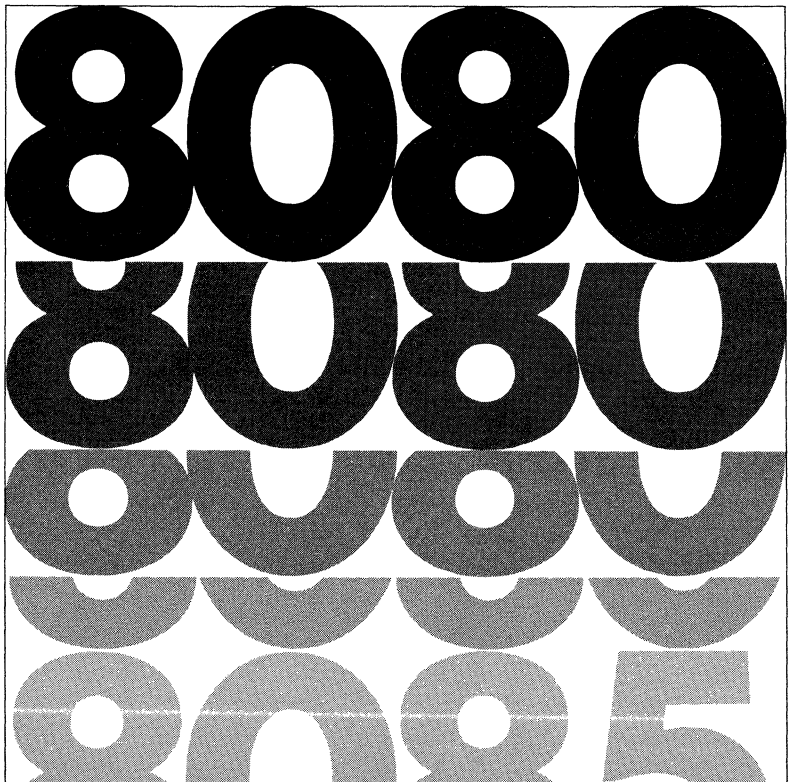
THE 8080 CENTRAL PROCESSING UNIT

The 8080 is a complete 8-bit parallel, central processor unit (CPU) for use in general purpose digital computer systems. It is fabricated on a single LSI chip (see Figure 3-1). using Intel's n-channel silicon gate MOS process. The 8080 transfers data and internal state information via an 8-bit, bidirectional 3–state Data Bus (D_0-D_7). Memory and peripheral device addresses are transmitted over a separate 16-bit 3-state Address Bus (A_0-A_{15}). Six timing and control outputs (SYNC, DBIN, WAIT, $\overline{WR}$, HLDA and INTE) emanate from the 8080, while four control inputs (READY, HOLD, INT and RESET), four power inputs (+12v, +5v, -5v, and GND) and two clock inputs (ϕ_1 and ϕ_2) are accepted by the 8080.
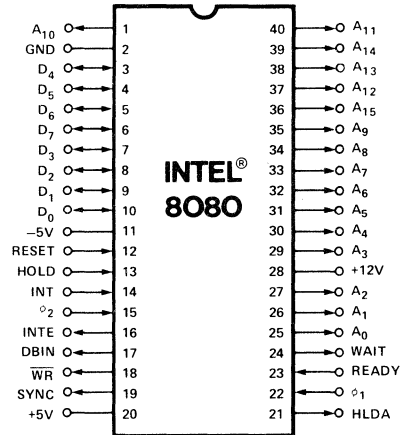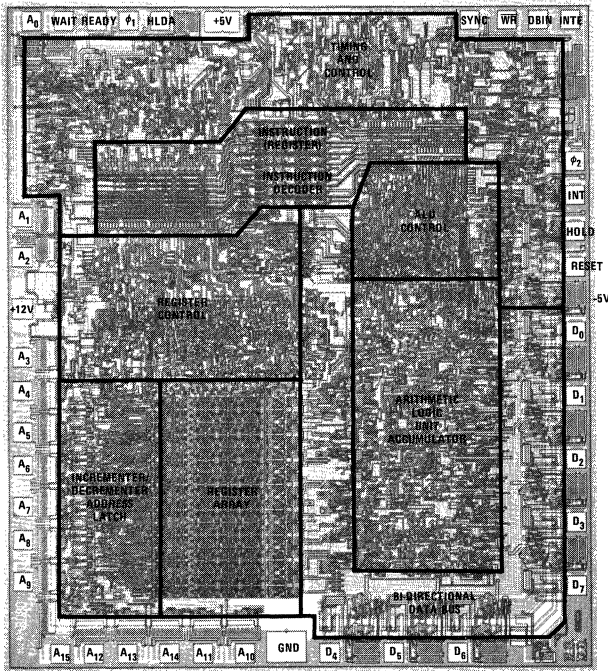
Figure 2-1. 8080 Photomicrograph With Pin Designations

ARCHITECTURE OF THE 8080 CPU

The 8080 CPU consists of the following functional units:

- Register array and address logic
- Arithmetic and logic unit (ALU)
- Instruction register and control section
- Bi-directional, 3–state data bus buffer

Figure 2-2 illustrates the functional blocks within the 8080 CPU.

Registers:

The register section consists of a static RAM array organized into six 16-bit registers:

- Program counter (PC)
- Stack pointer (SP)
- Six 8-bit general purpose registers arranged in pairs, referred to as B,C; D,E; and H,L
- A temporary register pair called W,Z

The program counter maintains the memory address of the current program instruction and is incremented auto-matically during every instruction fetch. The stack pointer maintains the address of the next available stack location in memory. The stack pointer can be initialized to use any portion of read-write memory as a stack. The stack pointer is decremented when data is "pushed" onto the stack and incremented when data is "popped" off the stack (i.e., the stack grows "downward").

The six general purpose registers can be used either as single registers (8-bit) or as register pairs (16-bit). The temporary register pair, W,Z, is not program addressable and is only used for the internal execution of instructions.

Eight-bit data bytes can be transferred between the internal bus and the register array via the register-select multiplexer. Sixteen-bit transfers can proceed between the register array and the address latch or the incrementer/decrementer circuit. The address latch receives data from any of the three register pairs and drives the 16 address output buffers (A_0-A_{15}), as well as the incrementer/decrementer circuit. The incrementer/decrementer circuit receives data from the address latch and sends it to the register array. The 16-bit data can be incremented or decremented or simply transferred between registers.
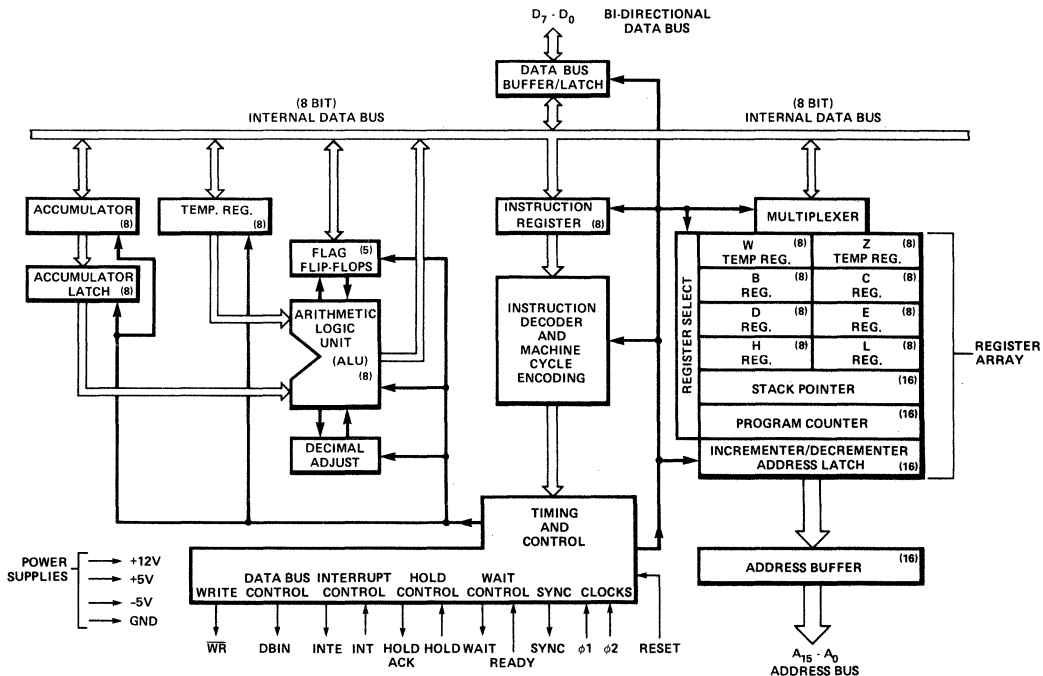
Figure 2-2. 8080 CPU Functional Block Diagram

Arithmetic and Logic Unit (ALU):

The ALU contains the following registers:

- An 8-bit accumulator

- An 8-bit temporary accumulator (ACT)

- A 5-bit flag register: zero, carry, sign, parity and auxiliary carry

- An 8-bit temporary register (TMP)

Arithmetic, logical and rotate operations are performed in the ALU. The ALU is fed by the temporary register (TMP) and the temporary accumulator (ACT) and carry flip-flop. The result of the operation can be transferred to the internal bus or to the accumulator; the ALU also feeds the flag register.

The temporary register (TMP) receives information from the internal bus and can send all or portions of it to the ALU, the flag register and the internal bus.

The accumulator (ACC) can be loaded from the ALU and the internal bus and can transfer data to the temporary accumulator (ACT) and the internal bus. The contents of the accumulator (ACC) and the auxiliary carry flip-flop can be tested for decimal correction during the execution of the DAA instruction (see Chapter 4).

Instruction Register and Control:

During an instruction fetch, the first byte of an instruction (containing the OP code) is transferred from the internal bus to the 8-bit instruction register.

The contents of the instruction register are, in turn, available to the instruction decoder. The output of the decoder, combined with various timing signals, provides the control signals for the register array, ALU and data buffer blocks. In addition, the outputs from the instruction decoder and external control signals feed the timing and state control section which generates the state and cycle timing signals.

Data Bus Buffer:

This 8-bit bidirectional 3-state buffer is used to isolate the CPU's internal bus from the external data bus (D$_0$ through D$_7$). In the output mode, the internal bus content is loaded into an 8-bit latch that, in turn, drives the data bus output buffers. The output buffers are switched off during input or non-transfer operations.

During the input mode, data from the external data bus is transferred to the internal bus. The internal bus is precharged at the beginning of each internal state, except for the transfer state (T$_3$—described later in this chapter).

THE PROCESSOR CYCLE

An **instruction cycle** is defined as the time required to fetch and execute an instruction. During the fetch, a selected instruction (one, two or three bytes) is extracted from memory and deposited in the CPU's instruction register. During the execution phase, the instruction is decoded and translated into specific processing activities.

Every instruction cycle consists of one, two, three, four or five machine cycles. A **machine cycle** is required each time the CPU accesses memory or an I/O port. The fetch portion of an instruction cycle requires one machine cycle for each byte to be fetched. The duration of the execution portion of the instruction cycle depends on the kind of instruction that has been fetched. Some instructions do not require any machine cycles other than those necessary to fetch the instruction; other instructions, however, require additional machine cycles to write or read data to/from memory or I/O devices. The DAD instruction is an exception in that it requires two additional machine cycles to complete an internal register-pair add (see Chapter 4).

Each machine cycle consists of three, four or five states. A state is the smallest unit of processing activity and is defined as the interval between two successive positive-going transitions of the ϕ_1 driven clock pulse. The 8080 is driven by a two-phase clock oscillator. All processing activities are referred to the period of this clock. The two non-overlapping clock pulses, labeled ϕ_1 and ϕ_2, are furnished by external circuitry. It is the ϕ_1 clock pulse which divides each machine cycle into states. Timing logic within the 8080 uses the clock inputs to produce a SYNC pulse, which identifies the beginning of every machine cycle. The SYNC pulse is triggered by the low-to-high transition of ϕ_2, as shown in Figure 2-3.
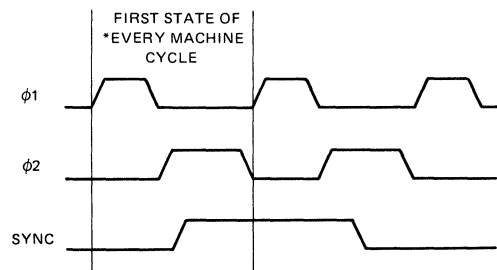
*SYNC DOES NOT OCCUR IN THE SECOND AND THIRD MACHINE CYCLES OF A DAD INSTRUCTION SINCE THESE MACHINE CYCLES ARE USED FOR AN INTERNAL REGISTER-PAIR ADD.

Figure 2-3. ϕ_1, ϕ_2 And SYNC Timing

There are three exceptions to the defined duration of a state. They are the WAIT state, the hold (HLDA) state and the halt (HLTA) state, described later in this chapter. Because the WAIT, the HLDA, and the HLTA states depend upon external events, they are by their nature of indeterminate length. Even these exceptional states, however, must

be synchronized with the pulses of the driving clock. Thus, the duration of all states are integral multiples of the clock period.

To summarize then, each **clock period** marks a **state**; three to five states constitute a machine cycle; and one to five **machine cycles** comprise an **instruction cycle**. A full instruction cycle requires anywhere from four to eighteen states for its completion, depending on the kind of instruction involved.

Machine Cycle Identification:

With the exception of the DAD instruction, there is just one consideration that determines how many machine cycles are required in any given instruction cycle: the number of times that the processor must reference a memory address or an addressable peripheral device, in order to fetch and execute the instruction. Like many processors, the 8080 is so constructed that it can transmit only one address per machine cycle. Thus, if the fetch and execution of an instruction requires two memory references, then the instruction cycle associated with that instruction consists of two machine cycles. If five such references are called for, then the instruction cycle contains five machine cycles.

Every instruction cycle has at least one reference to memory, during which the instruction is fetched. An instruction cycle must always have a fetch, even if the execution of the instruction requires no further references to memory. The first machine cycle in every instruction cycle is therefore a FETCH. Beyond that, there are no fast rules. It depends on the kind of instruction that is fetched.

Consider some examples. The add-register (ADD r) instruction is an instruction that requires only a single machine cycle (FETCH) for its completion. In this one-byte instruction, the contents of one of the CPU's six general purpose registers is added to the existing contents of the accumulator. Since all the information necessary to execute the command is contained in the eight bits of the instruction code, only one memory reference is necessary. Three states are used to extract the instruction from memory, and one additional state is used to accomplish the desired addition. The entire instruction cycle thus requires only one machine cycle that consists of four states, or four periods of the external clock.

Suppose now, however, that we wish to add the contents of a specific memory location to the existing contents of the accumulator (ADD M). Although this is quite similar in principle to the example just cited, several additional steps will be used. An extra machine cycle will be used, in order to address the desired memory location.

The actual sequence is as follows. First the processor extracts from memory the one-byte instruction word addressed by its program counter. This takes three states. The eight-bit instruction word obtained during the FETCH machine cycle is deposited in the CPU's instruction register and used to direct activities during the remainder of the instruction cycle. Next, the processor sends out, as an address,

the contents of its H and L registers. The eight-bit data word returned during this MEMORY READ machine cycle is placed in a temporary register inside the 8080 CPU. By now three more clock periods (states) have elapsed. In the seventh and final state, the contents of the temporary register are added to those of the accumulator. Two machine cycles, consisting of seven states in all, complete the "ADD M" instruction cycle.

At the opposite extreme is the save H and L registers (SHLD) instruction, which requires five machine cycles. During an "SHLD" instruction cycle, the contents of the processor's H and L registers are deposited in two sequentially adjacent memory locations; the destination is indicated by two address bytes which are stored in the two memory locations immediately following the operation code byte. The following sequence of events occurs:

(1) A FETCH machine cycle, consisting of four states. During the first three states of this machine cycle, the processor fetches the instruction indicated by its program counter. The program counter is then incremented. The fourth state is used for internal instruction decoding.

(2) A MEMORY READ machine cycle, consisting of three states. During this machine cycle, the byte indicated by the program counter is read from memory and placed in the processor's Z register. The program counter is incremented again.

(3) Another MEMORY READ machine cycle, consisting of three states, in which the byte indicated by the processor's program counter is read from memory and placed in the W register. The program counter is incremented, in anticipation of the next instruction fetch.

(4) A MEMORY WRITE machine cycle, of three states, in which the contents of the L register are transferred to the memory location pointed to by the present contents of the W and Z registers. The state following the transfer is used to increment the W,Z register pair so that it indicates the next memory location to receive data.

(5) A MEMORY WRITE machine cycle, of three states, in which the contents of the H register are transferred to the new memory location pointed to by the W,Z register pair.

In summary, the "SHLD" instruction cycle contains five machine cycles and takes 16 states to execute.

Most instructions fall somewhere between the extremes typified by the "ADD r" and the "SHLD" instructions. The input (INP) and the output (OUT) instructions, for example, require three machine cycles: a FETCH, to obtain the instruction; a MEMORY READ, to obtain the address of the object peripheral; and an INPUT or an OUTPUT machine cycle, to complete the transfer.

While no one instruction cycle will consist of more then five machine cycles, the following ten different types of machine cycles may occur within an instruction cycle:

(1) FETCH (M1)

(2) MEMORY READ

(3) MEMORY WRITE

(4) STACK READ

(5) STACK WRITE

(6) INPUT

(7) OUTPUT

(8) INTERRUPT

(9) HALT

(10) HALT • INTERRUPT

The machine cycles that actually do occur in a particular instruction cycle depend upon the kind of instruction, with the overriding stipulation that the first machine cycle in any instruction cycle is always a FETCH.

The processor identifies the machine cycle in progress by transmitting an eight-bit status word during the first state of every machine cycle. Updated status information is presented on the 8080's data lines (D_0-D_7), during the SYNC interval. This data should be saved in latches, and used to develop control signals for external circuitry. Table 2-1 shows how the positive-true status information is distributed on the processor's data bus.

Status signals are provided principally for the control of external circuitry. Simplicity of interface, rather than machine cycle identification, dictates the logical definition of individual status bits. You will therefore observe that certain processor machine cycles are uniquely identified by a single status bit, but that others are not. The M_1 status bit (D_6), for example, unambiguously identifies a FETCH machine cycle. A STACK READ, on the other hand, is indicated by the coincidence of STACK and MEMR signals. Machine cycle identification data is also valuable in the test and de-bugging phases of system development. Table 2-1 lists the status bit outputs for each type of machine cycle.

State Transition Sequence:

Every machine cycle within an instruction cycle consists of three to five active states (referred to as T_1, T_2, T_3, T_4, T_5 or T_W). The actual number of states depends upon the instruction being executed, and on the particular machine cycle within the greater instruction cycle. The state transition diagram in Figure 2-4 shows how the 8080 proceeds from state to state in the course of a machine cycle. The diagram also shows how the READY, HOLD, and INTERRUPT lines are sampled during the machine cycle, and how the conditions on these lines may modify the

basic transition sequence. In the present discussion, we are concerned only with the basic sequence and with the READY function. The HOLD and INTERRUPT functions will be discussed later.

The 8080 CPU does not directly indicate its internal state by transmitting a "state control" output during each state; instead, the 8080 supplies direct control output (INTE, HLDA, DBIN, $\overline{WR}$ and WAIT) for use by external circuitry.

Recall that the 8080 passes through at least three states in every machine cycle, with each state defined by successive low-to-high transitions of the ϕ_1 clock. Figure 2-5 shows the timing relationships in a typical FETCH machine cycle. Events that occur in each state are referenced to transitions of the ϕ_1 and ϕ_2 clock pulses.

The SYNC signal identifies the first state (T_1) in every machine cycle. As shown in Figure 2-5, the SYNC signal is related to the leading edge of the ϕ_2 clock. There is a delay (t_{DC}) between the low-to-high transition of ϕ_2 and the positive-going edge of the SYNC pulse. There also is a corresponding delay (also t_{DC}) between the next ϕ_2 pulse and the falling edge of the SYNC signal. Status information is displayed on D_0-D_7 during the same ϕ_2 to ϕ_2 interval. Switching of the status signals is likewise controlled by ϕ_2.

The rising edge of ϕ_2 during T_1 also loads the processor's address lines (A_0-A_{15}). These lines become stable within a brief delay (t_{DA}) of the ϕ_2 clocking pulse, and they remain stable until the first ϕ_2 pulse after state T_3. This gives the processor ample time to read the data returned from memory.

Once the processor has sent an address to memory, there is an opportunity for the memory to request a WAIT. This it does by pulling the processor's READY line low, prior to the "Ready set-up" interval (t_{RS}) which occurs during the ϕ_2 pulse within state T_2 or T_W. As long as the READY line remains low, the processor will idle, giving the memory time to respond to the addressed data request. Refer to Figure 2-5.

The processor responds to a wait request by entering an alternative state (T_W) at the end of T_2, rather than proceeding directly to the T_3 state. Entry into the T_W state is indicated by a WAIT signal from the processor, acknowledging the memory's request. A low-to-high transition on the WAIT line is triggered by the rising edge of the ϕ_1 clock and occurs within a brief delay (t_{DC}) of the actual entry into the T_W state.

A wait period may be of indefinite duration. The processor remains in the waiting condition until its READY line again goes high. A READY indication **must** precede the falling edge of the ϕ_2 clock by a specified interval (t_{RS}), in order to guarantee an exit from the T_W state. The cycle may then proceed, beginning with the rising edge of the next ϕ_1 clock. A WAIT interval will therefore consist of an integral number of T_W states and will always be a multiple of the clock period.

Instructions for the 8080 require from one to five machine cycles for complete execution. The 8080 sends out 8 bit of status information on the data bus at the beginning of each machine cycle (during SYNC time). The following table defines the status information.

STATUS INFORMATION DEFINITION

Symbols	Data Bus Bit	Definition
INTA*	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function ($\overline{WO} = 0$). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{WR}$ is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
INP*	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR*	D_7	Designates that the data bus will be used for memory read data.

*These three status bits can be used to control the flow of data onto the 8080 data bus.

STATUS WORD CHART

D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

Table 2-1. 8080 Status Bit Definitions
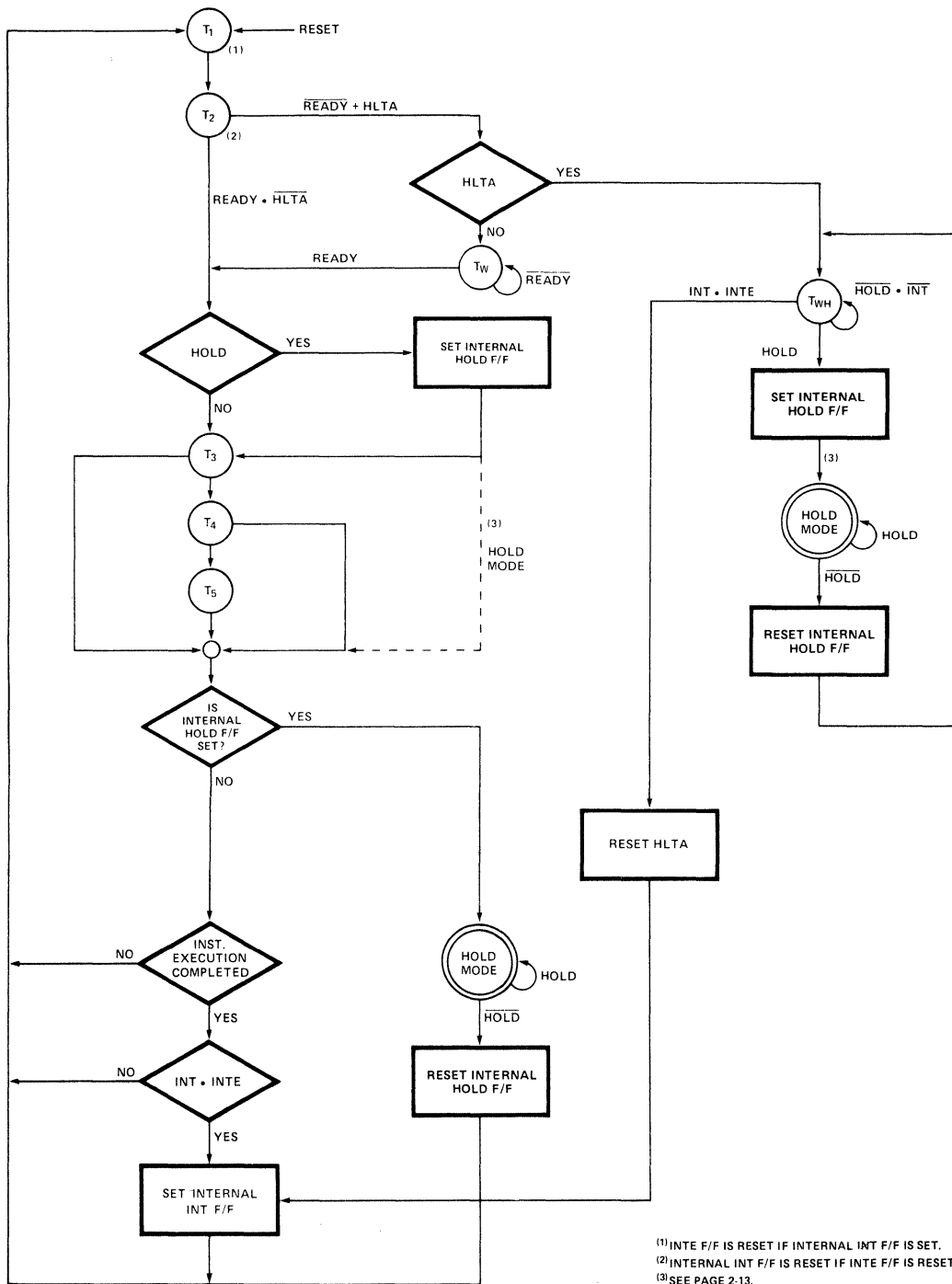
Figure 2-4. CPU State Transition Diagram

The events that take place during the T_3 state are determined by the kind of machine cycle in progress. In a FETCH machine cycle, the processor interprets the data on its data bus as an instruction. During a MEMORY READ or a STACK READ, data on this bus is interpreted as a data word. The processor outputs data on this bus during a MEMORY WRITE machine cycle. During I/O operations, the processor may either transmit or receive data, depending on whether an OUTPUT or an INPUT operation is involved.

Figure 2-6 illustrates the timing that is characteristic of a data input operation. As shown, the low-to-high transition of ϕ_2 during T_2 clears status information from the processor's data lines, preparing these lines for the receipt of incoming data. The data presented to the processor must have stabilized prior to both the "ϕ_1—data set-up" interval (t_{DS1}), that precedes the falling edge of the ϕ_1 pulse defining state T_3, and the "ϕ_2—data set-up" interval (t_{DS2}), that precedes the rising edge of ϕ_2 in state T_3. This same

data must remain stable during the "data hold" interval (t_{DH}) that occurs following the rising edge of the ϕ_2 pulse. Data placed on these lines by memory or by other external devices will be sampled during T_3.

During the input of data to the processor, the 8080 generates a DBIN signal which should be used externally to enable the transfer. Machine cycles in which DBIN is available include: FETCH, MEMORY READ, STACK READ, and INTERRUPT. DBIN is initiated by the rising edge of ϕ_2 during state T_2 and terminated by the corresponding edge of ϕ_2 during T_3. Any T_W phases intervening between T_2 and T_3 will therefore extend DBIN by one or more clock periods.

Figure 2-7 shows the timing of a machine cycle in which the processor outputs data. Output data may be destined either for memory or for peripherals. The rising edge of ϕ_2 within state T_2 clears status information from the CPU's data lines, and loads in the data which is to be output to external devices. This substitution takes place within the
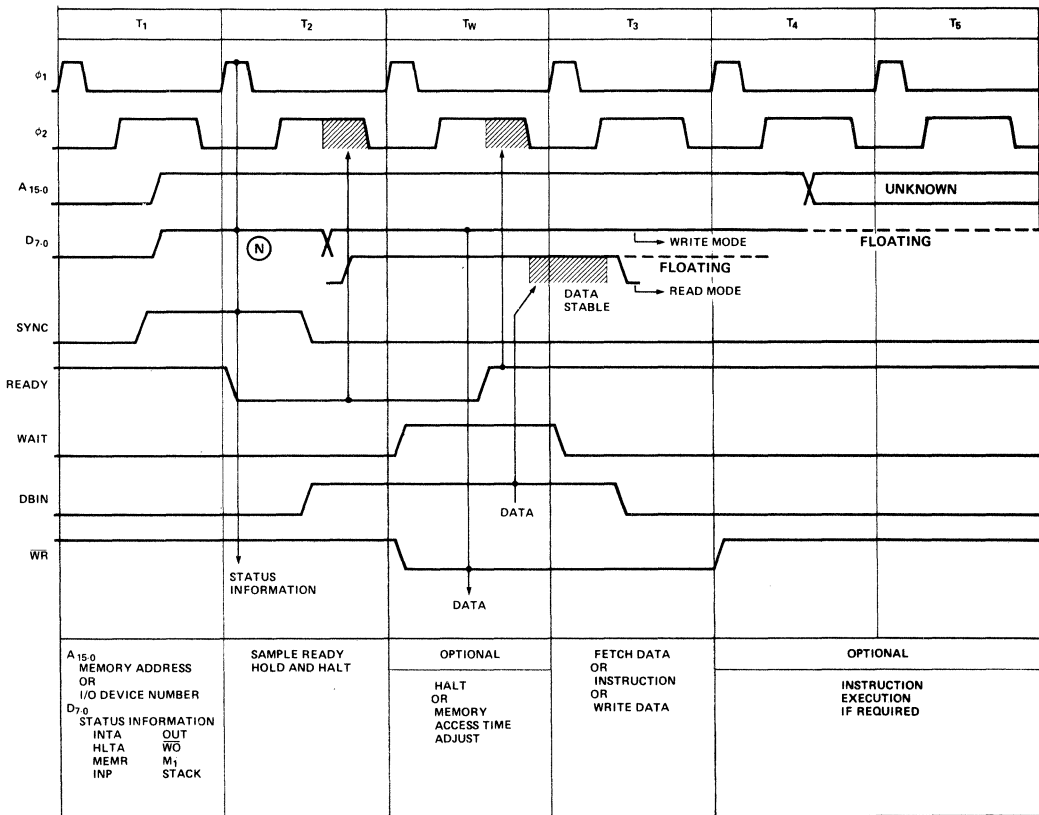
NOTE: Ⓝ Refer to Status Word Chart on Page 2-6.

Figure 2-5. Basic 8080 Instruction Cycle
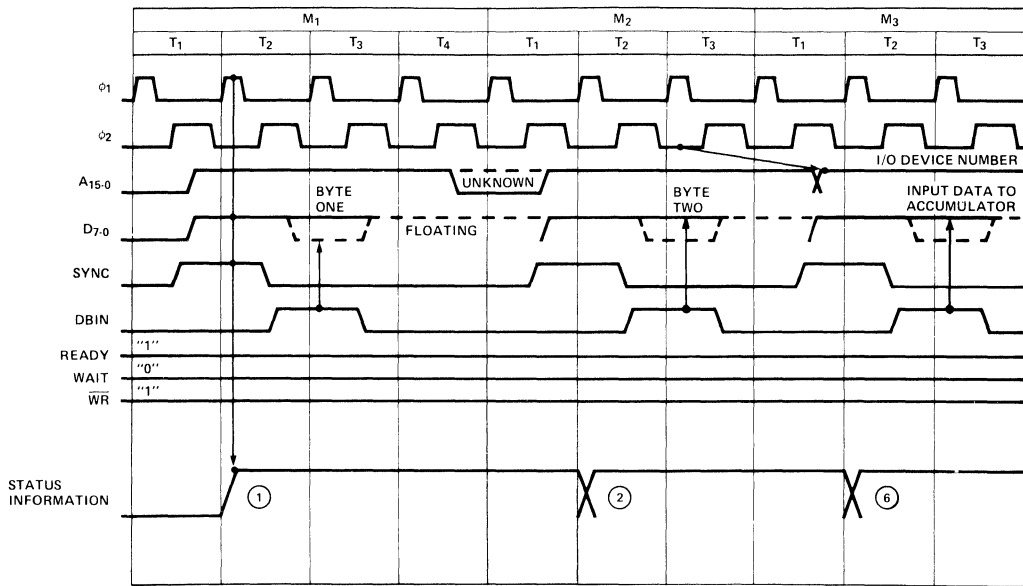
Figure 2-6. Input Instruction Cycle
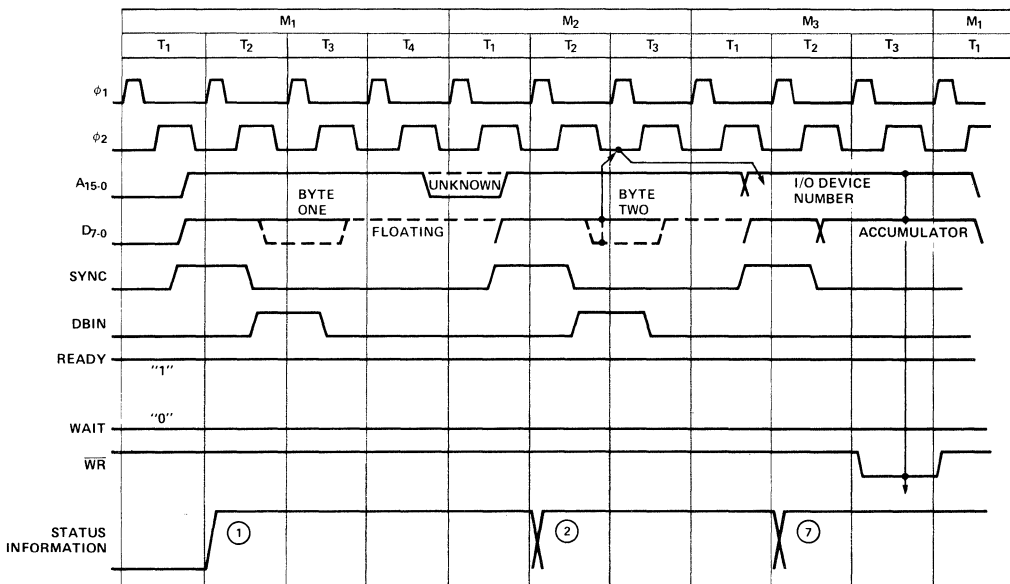
NOTE: Ⓝ Refer to Status Word Chart on Page 2-6.

Figure 2-7. Output Instruction Cycle

2-9

"data output delay" interval (t_{DD}) following the ϕ_2 clock's leading edge. Data on the bus remains stable throughout the remainder of the machine cycle, until replaced by updated status information in the subsequent T_1 state. Observe that a READY signal is necessary for completion of an OUTPUT machine cycle. Unless such an indication is present, the processor enters the T_W state, following the T_2 state. Data on the output lines remains stable in the interim, and the processing cycle will not proceed until the READY line again goes high.

The 8080 CPU generates a $\overline{WR}$ output for the synchronization of external transfers, during those machine cycles in which the processor outputs data. These include MEMORY WRITE, STACK WRITE, and OUTPUT. The negative-going leading edge of $\overline{WR}$ is referenced to the rising edge of the first ϕ_1 clock pulse following T_2, and occurs within a brief delay (t_{DC}) of that event. $\overline{WR}$ remains low until re-triggered by the leading edge of ϕ_1 during the state following T_3. Note that any T_W states intervening between T_2 and T_3 of the output machine cycle will necessarily extend $\overline{WR}$, in much the same way that DBIN is affected during data input operations.

All processor machine cycles consist of at least three states: T_1, T_2, and T_3 as just described. If the processor has to wait for a response from the peripheral or memory with which it is communicating, then the machine cycle may also contain one or more T_W states. During the three basic states, data is transferred to or from the processor.

After the T_3 state, however, it becomes difficult to generalize. T_4 and T_5 states are available, if the execution of a particular instruction requires them. But not all machine cycles make use of these states. It depends upon the kind of instruction being executed, and on the particular machine cycle within the instruction cycle. The processor will terminate any machine cycle as soon as its processing activities are completed, rather than proceeding through the T_4 and T_5 states every time. Thus the 8080 may exit a machine cycle following the T_3, the T_4, or the T_5 state and proceed directly to the T_1 state of the next machine cycle.

STATE	ASSOCIATED ACTIVITIES
T_1	A memory address or I/O device number is placed on the Address Bus (A_{15-0}); status information is placed on Data Bus (D_{7-0}).
T_2	The CPU samples the READY and HOLD inputs and checks for halt instruction.
TW (optional)	Processor enters wait state if READY is low or if HALT instruction has been executed.
T3	An instruction byte (FETCH machine cycle), data byte (MEMORY READ, STACK READ) or interrupt instruction (INTERRUPT machine cycle) is input to the CPU from the Data Bus; or a data byte (MEMORY WRITE, STACK WRITE or OUTPUT machine cycle) is output onto the data bus.
T_4 T_5 (optional)	States T_4 and T_5 are available if the execution of a particular instruction requires them; if not, the CPU may skip one or both of them. T_4 and T_5 are only used for internal processor operations.

Table 2-2. State Definitions

INTERRUPT SEQUENCES

The 8080 has the built-in capacity to handle external interrupt requests. A peripheral device can initiate an interrupt simply by driving the processor's interrupt (INT) line high.

The interrupt (INT) input is asynchronous, and a request may therefore originate at any time during any instruction cycle. Internal logic re-clocks the external request, so that a proper correspondence with the driving clock is established. As Figure 2-8 shows, an interrupt request (INT) arriving during the time that the interrupt enable line (INTE) is high, acts in coincidence with the ϕ_2 clock to set the internal interrupt latch. This event takes place during the last state of the instruction cycle in which the request occurs, thus ensuring that any instruction in progress is completed before the interrupt can be processed.

The INTERRUPT machine cycle which follows the arrival of an enabled interrupt request resembles an ordinary FETCH machine cycle in most respects. The M_1 status bit is transmitted as usual during the SYNC interval. It is accompanied, however, by an INTA status bit (D_0) which acknowledges the external request. The contents of the program counter are latched onto the CPU's address lines during T_1, but the counter itself is not incremented during the INTERRUPT machine cycle, as it otherwise would be.

In this way, the pre-interrupt status of the program counter is preserved, so that data in the counter may be restored by the interrupted program after the interrupt request has been processed.

The interrupt cycle is otherwise indistinguishable from an ordinary FETCH machine cycle. The processor itself takes no further special action. It is the responsibility of the peripheral logic to see that an eight-bit interrupt instruction is "jammed" onto the processor's data bus during state T_3. In a typical system, this means that the data-in bus from memory must be temporarily disconnected from the processor's main data bus, so that the interrupting device can command the main bus without interference.

The 8080's instruction set provides a special one-byte call which facilitates the processing of interrupts (the ordinary program Call takes three bytes). This is the RESTART instruction (RST). A variable three-bit field embedded in the eight-bit field of the RST enables the interrupting device to direct a Call to one of eight fixed memory locations. The decimal addresses of these dedicated locations are: 0, 8, 16, 24, 32, 40, 48, and 56. Any of these addresses may be used to store the first instruction(s) of a routine designed to service the requirements of an interrupting device. Since the (RST) is a call, completion of the instruction also stores the old program counter contents on the STACK.
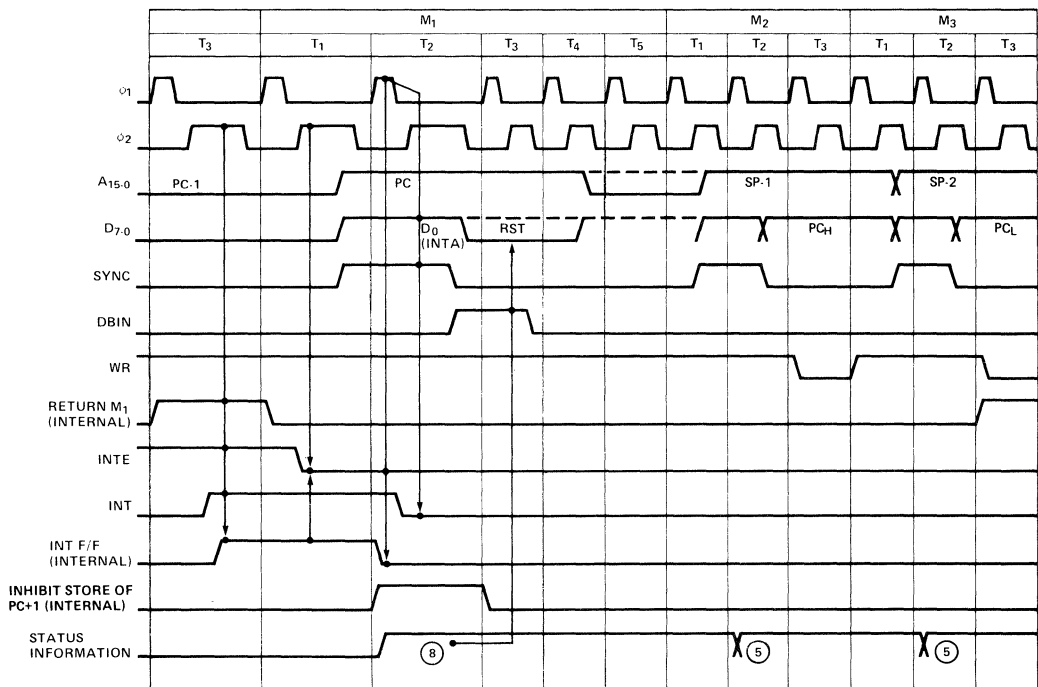
NOTE: (N) Refer to Status Word Chart on Page 2-6.

Figure 2-8. Interrupt Timing
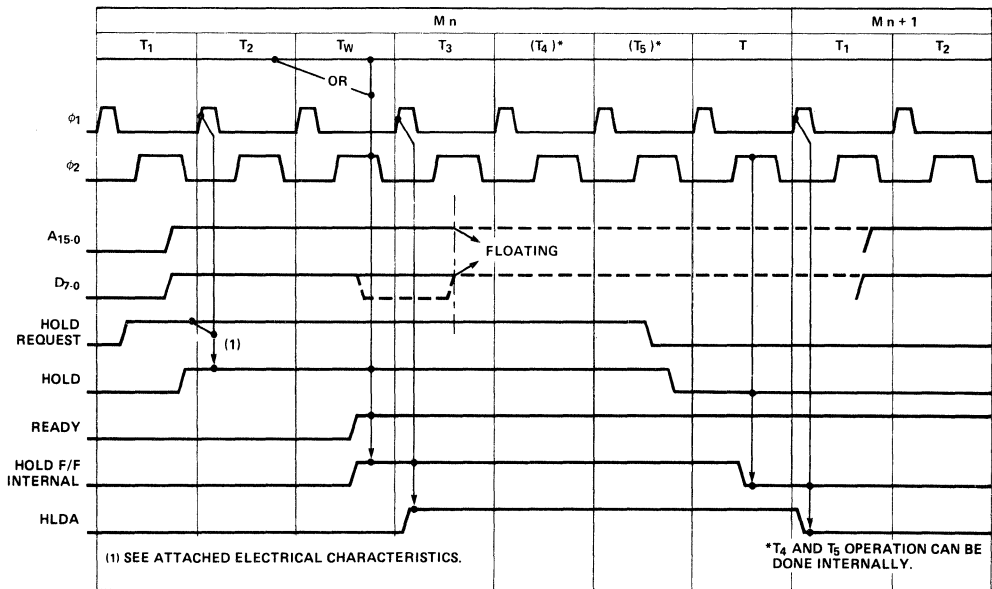
Figure 2-9. HOLD Operation (Read Mode)
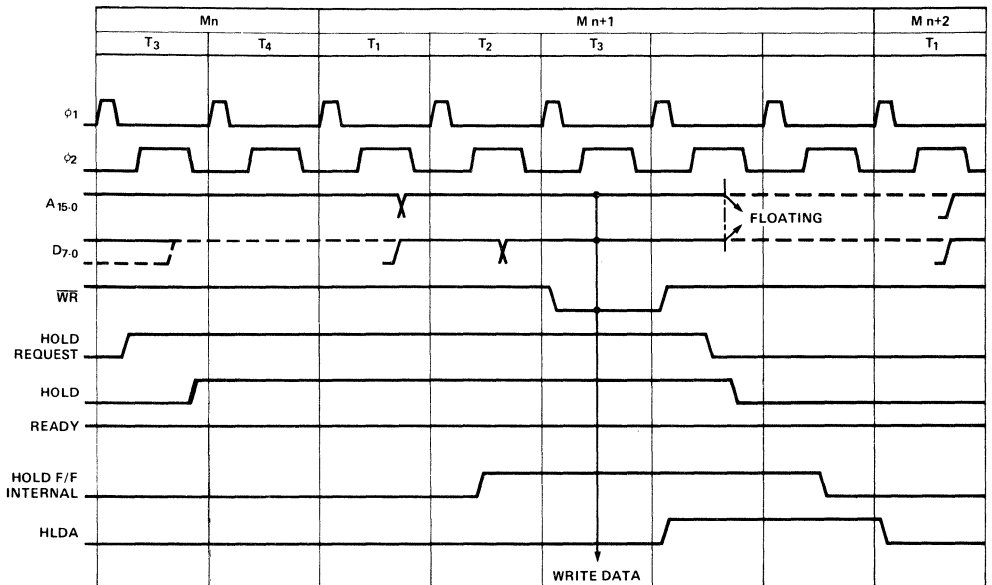
Figure 2-10. HOLD Operation (Write Mode)

HOLD SEQUENCES

The 8080A CPU contains provisions for Direct Memory Access (DMA) operations. By applying a HOLD to the appropriate control pin on the processor, an external device can cause the CPU to suspend its normal operations and relinquish control of the address and data busses. The processor responds to a request of this kind by floating its address to other devices sharing the busses. At the same time, the processor acknowledges the HOLD by placing a high on its HLDA outpin pin. During an acknowledged HOLD, the address and data busses are under control of the peripheral which originated the request, enabling it to conduct memory transfers without processor intervention.

Like the interrupt, the HOLD input is synchronized internally. A HOLD signal must be stable prior to the "Hold set-up" interval (t_{HS}), that precedes the rising edge of ϕ_2.

Figures 2-9 and 2-10 illustrate the timing involved in HOLD operations. Note the delay between the asynchronous HOLD REQUEST and the re-clocked HOLD. As shown in the diagram, a coincidence of the READY, the HOLD, and the ϕ_2 clocks sets the internal hold latch. Setting the latch enables the subsequent rising edge of the ϕ_1 clock pulse to trigger the HLDA output.

Acknowledgement of the HOLD REQUEST precedes slightly the actual floating of the processor's address and data lines. The processor acknowledges a HOLD at the beginning of T_3, if a read or an input machine cycle is in progress (see Figure 2-9). Otherwise, acknowledgement is deferred until the beginning of the state following T_3 (see Figure 2-10). In both cases, however, the HLDA goes high within a specified delay (t_{DC}) of the rising edge of the selected ϕ_1 clock pulse. Address and data lines are floated within a brief delay after the rising edge of the next ϕ_2 clock pulse. This relationship is also shown in the diagrams.

To all outward appearances, the processor has suspended its operations once the address and data busses are floated. Internally, however, certain functions may continue. If a HOLD REQUEST is acknowledged at T_3, and if the processor is in the middle of a machine cycle which requires four or more states to complete, the CPU proceeds through T_4 and T_5 before coming to a rest. Not until the end of the machine cycle is reached will processing activities cease. Internal processing is thus permitted to overlap the external DMA transfer, improving both the efficiency and the speed of the entire system.

The processor exits the holding state through a sequence similar to that by which it entered. A HOLD REQUEST is terminated asynchronously when the external device has completed its data transfer. The HLDA output returns to a low level following the leading edge of the next ϕ_1 clock pulse. Normal processing resumes with the machine cycle following the last cycle that was executed.

HALT SEQUENCES

When a halt instruction (HLT) is executed, the CPU enters the halt state (T_{WH}) after state T_2 of the next machine cycle, as shown in Figure 2-11. There are only three ways in which the 8080 can exit the halt state:

- A high on the RESET line will always reset the 8080 to state T_1; RESET also clears the program counter.
- A HOLD input will cause the 8080 to enter the hold state, as previously described. When the HOLD line goes low, the 8080 re-enters the halt state on the rising edge of the next ϕ_1 clock pulse.
- An interrupt (i.e., INT goes high while INTE is enabled) will cause the 8080 to exit the Halt state and enter state T_1 on the rising edge of the next ϕ_1 clock pulse. NOTE: The interrupt enable (INTE) flag **must** be set when the halt state is entered; otherwise, the 8080 will only be able to exit via a RESET signal.

Figure 2-12 illustrates halt sequencing in flow chart form.

START-UP OF THE 8080 CPU

When power is applied initially to the 8080, the processor begins operating immediately. The contents of its program counter, stack pointer, and the other working registers are naturally subject to random factors and cannot be specified. For this reason, it will be necessary to begin the power-up sequence with RESET.

An external RESET signal of three clock period duration (minimum) restores the processor's internal program counter to zero. Program execution thus begins with memory location zero, following a RESET. Systems which require the processor to wait for an explicit start-up signal will store a halt instruction (EI, HLT) in the first two locations. A manual or an automatic INTERRUPT will be used for starting. In other systems, the processor may begin executing its stored program immediately. Note, however, that the RESET has no effect on status flags, or on any of the processor's working registers (accumulator, registers, or stack pointer). The contents of these registers remain indeterminate, until initialized explicitly by the program.
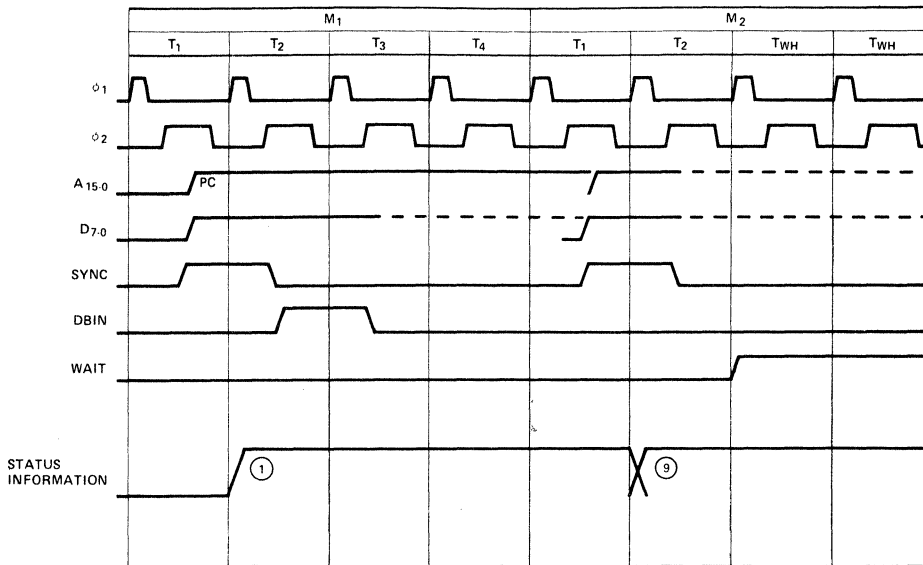
NOTE: (N) Refer to Status Word Chart on Page 2-6

Figure 2-11. HALT Timing
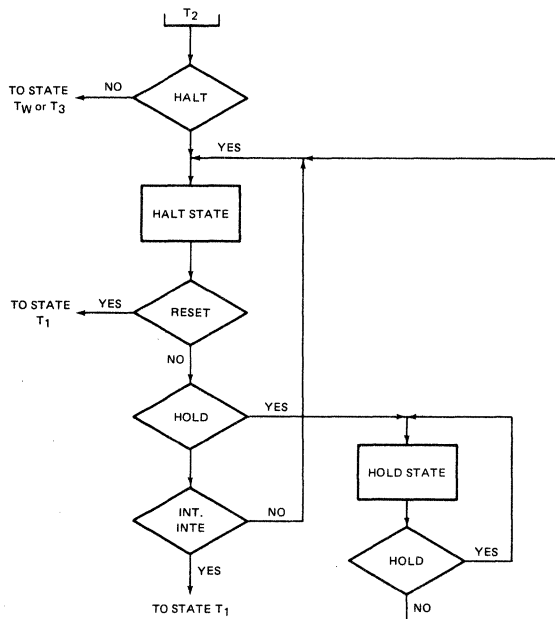
Figure 2-12. HALT Sequence Flow Chart.
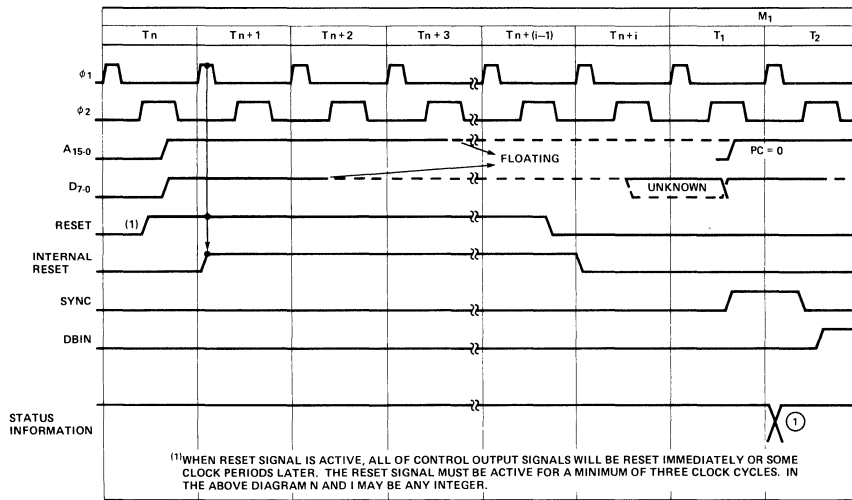
Figure 2-13. Reset.

(1) WHEN RESET SIGNAL IS ACTIVE, ALL OF CONTROL OUTPUT SIGNALS WILL BE RESET IMMEDIATELY OR SOME CLOCK PERIODS LATER. THE RESET SIGNAL MUST BE ACTIVE FOR A MINIMUM OF THREE CLOCK CYCLES. IN THE ABOVE DIAGRAM N AND I MAY BE ANY INTEGER.
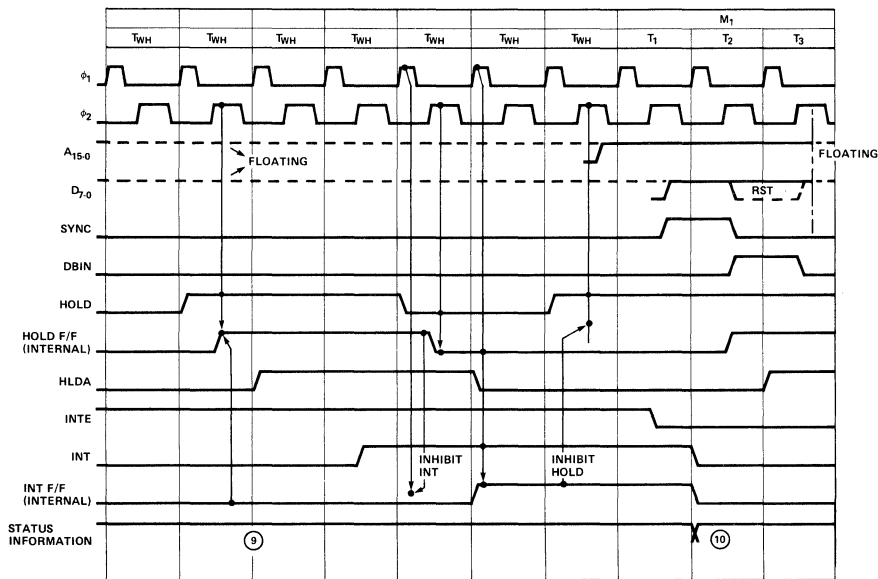
NOTE: (N) Refer to Status Word Chart on Page 2-6.

Figure 2-14. Relation between HOLD and INT in the HALT State.

NOTE: (N) Refer to Status Word Chart on Page 2-6.

MNEMONIC	OP CODE		M1[1]					M2		
	$D_7 D_6 D_5 D_4$	$D_3 D_2 D_1 D_0$	T1	T2[2]	T3	T4	T5	T1	T2[2]	T3
MOV r1, r2	0 1 D D	D S S S	PC OUT STATUS	PC = PC +1	INST→TMP/IR	(SSS)→TMP	(TMP)→DDD			
MOV r, M	0 1 D D	D 1 1 0				X[3]		HL OUT STATUS[6]		DATA→DDD
MOV M, r	0 1 1 1	0 S S S				(SSS)→TMP		HL OUT STATUS[7]		(TMP)→DATA BUS
SPHL	1 1 1 1	1 0 0 1				(HL) ———————→SP				
MVI r, data	0 0 D D	D 1 1 0				X		PC OUT STATUS[6]		B2→DDDD
MVI M, data	0 0 1 1	0 1 1 0				X				B2→TMP
LXI rp, data	0 0 R P	0 0 0 1				X			PC = PC + 1	B2→r1
LDA addr	0 0 1 1	1 0 1 0				X			PC = PC + 1	B2→Z
STA addr	0 0 1 1	0 0 1 0				X			PC = PC + 1	B2→Z
LHLD addr	0 0 1 0	1 0 1 0				X			PC = PC + 1	B2→Z
SHLD addr	0 0 1 0	0 0 1 0				X		PC OUT STATUS[6]	PC = PC + 1	B2→Z
LDAX rp[4]	0 0 R P	1 0 1 0				X		rp OUT STATUS[6]		DATA→A
STAX rp[4]	0 0 R P	0 0 1 0				X		rp OUT STATUS[7]		(A)→DATA BUS
XCHG	1 1 1 0	1 0 1 1				(HL)↔(DE)				
ADD r	1 0 0 0	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)→A	
ADD M	1 0 0 0	0 1 1 0				(A)→ACT		HL OUT STATUS[6]		DATA→TMP
ADI data	1 1 0 0	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1	B2→TMP
ADC r	1 0 0 0	1 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)+CY→A	
ADC M	1 0 0 0	1 1 1 0				(A)→ACT		HL OUT STATUS[6]		DATA→TMP
ACI data	1 1 0 0	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1	B2→TMP
SUB r	1 0 0 1	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)-(TMP)→A	
SUB M	1 0 0 1	0 1 1 0				(A)→ACT		HL OUT STATUS[6]		DATA→TMP
SUI data	1 1 0 1	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1	B2→TMP
SBB r	1 0 0 1	1 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)-(TMP)-CY→A	
SBB M	1 0 0 1	1 1 1 0				(A)→ACT		HL OUT STATUS[6]		DATA→TMP
SBI data	1 1 0 1	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1	B2→TMP
INR r	0 0 D D	D 1 0 0				(DDD)→TMP (TMP) + 1→ALU	ALU→DDD			
INR M	0 0 1 1	0 1 0 0				X		HL OUT STATUS[6]	DATA→TMP (TMP)+1→ALU	
DCR r	0 0 D D	D 1 0 1				(DDD)→TMP (TMP)+1→ALU	ALU→DDD			
DCR M	0 0 1 1	0 1 0 1				X		HL OUT STATUS[6]	DATA→TMP (TMP)-1→ALU	
INX rp	0 0 R P	0 0 1 1				(RP) + 1 ————→RP				
DCX rp	0 0 R P	1 0 1 1				(RP) – 1 ————→RP				
DAD rp[8]	0 0 R P	1 0 0 1				X		(rl)→ACT	(L)→TMP, (ACT)+(TMP)→ALU	ALU→L, CY
DAA	0 0 1 0	0 1 1 1				DAA→A, FLAGS[10]				
ANA r	1 0 1 0	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)→A	
ANA M	1 0 1 0	0 1 1 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	(A)→ACT		HL OUT STATUS[6]		DATA→TMP

M3			M4			M5				
T1	T2[2]	T3	T1	T2[2]	T3	T1	T2[2]	T3	T4	T5
HL OUT STATUS[7]	(TMP) ——→ DATA BUS									
PC OUT STATUS[6]	PC = PC + 1 B3 —→ rh									
	PC = PC + 1 B3 —→ W		WZ OUT STATUS[6]	DATA ———→ A						
	PC = PC + 1 B3 —→ W		WZ OUT STATUS[7]	(A) ————→ DATA BUS						
	PC = PC + 1 B3 —→ W		WZ OUT STATUS[6]	DATA ———→ L WZ = WZ + 1		WZ OUT STATUS[6]	DATA—→ H			
PC OUT STATUS[6]	PC = PC + 1 B3 —→ W		WZ OUT STATUS[7]	(L) ———→ DATA BUS WZ = WZ + 1	DATA BUS	WZ OUT STATUS[7]	(H) ——→ DATA BUS			
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)+CY→A									
[9]	(ACT)+(TMP)+CY→A									
[9]	(ACT)–(TMP)→A									
[9]	(ACT)–(TMP)→A									
[9]	(ACT)–(TMP)–CY→A									
[9]	(ACT)–(TMP)–CY→A									
HL OUT STATUS[7]	ALU —→ DATA BUS									
HL OUT STATUS[7]	ALU —→ DATA BUS									
(rh)→ACT	(H)→TMP (ACT)+(TMP)+CY→ALU	ALU→H, CY								
[9]	(ACT)+(TMP)→A									

MNEMONIC	OP CODE		M1[1]					M2		
	$D_7 D_6 D_5 D_4$	$D_3 D_2 D_1 D_0$	T1	T2[2]	T3	T4	T5	T1	T2[2]	T3
ANI data	1 1 1 0	0 1 1 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	(A)→ACT		PC OUT STATUS[6]	PC = PC + 1	B2 →TMP
XRA r	1 0 1 0	1 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)+(TPM)→A	
XRA M	1 0 1 0	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →TMP	
XRI data	1 1 1 0	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1	B2 →TMP
ORA r	1 0 1 1	0 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)+(TMP)→A	
ORA M	1 0 1 1	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →TMP	
ORI data	1 1 1 1	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1	B2 →TMP
CMP r	1 0 1 1	1 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)−(TMP), FLAGS	
CMP M	1 0 1 1	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →TMP	
CPI data	1 1 1 1	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1	B2 →TMP
RLC	0 0 0 0	0 1 1 1				(A)→ALU ROTATE		[9]	ALU→A, CY	
RRC	0 0 0 0	1 1 1 1				(A)→ALU ROTATE		[9]	ALU→A, CY	
RAL	0 0 0 1	0 1 1 1				(A), CY→ALU ROTATE		[9]	ALU→A, CY	
RAR	0 0 0 1	1 1 1 1				(A), CY→ALU ROTATE		[9]	ALU→A, CY	
CMA	0 0 1 0	1 1 1 1				(Ā)→A				
CMC	0 0 1 1	1 1 1 1				C̄Y→CY				
STC	0 0 1 1	0 1 1 1				1→CY				
JMP addr	1 1 0 0	0 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1	B2 →Z
J cond addr[17]	1 1 C C	C 0 1 0				JUDGE CONDITION		PC OUT STATUS[6]	PC = PC + 1	B2 →Z
CALL addr	1 1 0 0	1 1 0 1				SP = SP − 1		PC OUT STATUS[6]	PC = PC + 1	B2 →Z
C cond addr[17]	1 1 C C	C 1 0 0				JUDGE CONDITION IF TRUE, SP = SP − 1		PC OUT STATUS[6]	PC = PC + 1	B2 →Z
RET	1 1 0 0	1 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1	DATA →Z
R cond addr[17]	1 1 C C	C 0 0 0			INST→TMP/IR	JUDGE CONDITION[14]		SP OUT STATUS[15]	SP = SP + 1	DATA →Z
RST n	1 1 N N	N 1 1 1			φ→W INST→TMP/IR	SP = SP − 1		SP OUT STATUS[16]	SP = SP − 1	(PCH) →DATA BUS
PCHL	1 1 1 0	1 0 0 1			INST→TMP/IR	(HL) ————→ PC				
PUSH rp	1 1 R P	0 1 0 1				SP = SP − 1		SP OUT STATUS[16]	SP = SP − 1	(rh) →DATA BUS
PUSH PSW	1 1 1 1	0 1 0 1				SP = SP − 1		SP OUT STATUS[16]	SP = SP − 1	(A) →DATA BUS
POP rp	1 1 R P	0 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1	DATA →r1
POP PSW	1 1 1 1	0 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1	DATA →FLAGS
XTHL	1 1 1 0	0 0 1 1				X		SP OUT STATUS[15]	SP = SP + 1	DATA →Z
IN port	1 1 0 1	1 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1	B2 →Z, W
OUT port	1 1 0 1	0 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1	B2 →Z, W
EI	1 1 1 1	1 0 1 1				SET INTE F/F				
DI	1 1 1 1	0 0 1 1				RESET INTE F/F				
HLT	0 1 1 1	0 1 1 0				X		PC OUT STATUS	HALT MODE[20]	
NOP	0 0 0 0	0 0 0 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	X				

M3			M4			M5				
T1	T2[2]	T3	T1	T2[2]	T3	T1	T2[2]	T3	T4	T5
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)→A									
[9]	(ACT)–(TMP); FLAGS									
[9]	(ACT)–(TMP); FLAGS									
PC OUT STATUS[6]	PC = PC + 1	B3 →W				WZ OUT STATUS[11]		(WZ) + 1 → PC		
PC OUT STATUS[6]	PC = PC + 1	B3 →W				WZ OUT STATUS[11,12]		(WZ) + 1 → PC		
PC OUT STATUS[6]	PC = PC + 1	B3 →W	SP OUT STATUS[16]	(PCH) SP = SP – 1	→DATA BUS	SP OUT STATUS[16]		(PCL)→ DATA BUS	WZ OUT STATUS[11]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1	B3 →W[13]	SP OUT STATUS[16]	(PCH) SP = SP – 1	→DATA BUS	SP OUT STATUS[16]		(PCL)→ DATA BUS	WZ OUT STATUS[11,12]	(WZ) + 1 → PC
SP OUT STATUS[15]	SP = SP + 1	DATA →W				WZ OUT STATUS[11]		(WZ) + 1 → PC		
SP OUT STATUS[15]	SP = SP + 1	DATA →W				WZ OUT STATUS[11,12]		(WZ) + 1 → PC		
SP OUT STATUS[16]	(TMP = 00NNN000) →Z (PCL) →DATA BUS					WZ OUT STATUS[11]		(WZ) + 1 → PC		
SP OUT STATUS[16]	(rl) →DATA BUS									
SP OUT STATUS[16]	FLAGS →DATA BUS									
SP OUT STATUS[15]	SP = SP + 1	DATA →rh								
SP OUT STATUS[15]	SP = SP + 1	DATA →A								
SP OUT STATUS[15]	DATA →W		SP OUT STATUS[16]	(H)	→DATA BUS	SP OUT STATUS[16]		(L)→ DATA BUS	(WZ)→HL	
WZ OUT STATUS[18]	DATA →A									
WZ OUT STATUS[18]	(A) →DATA BUS									

NOTES:

1. The first memory cycle (M1) is always an instruction fetch; the first (or only) byte, containing the op code, is fetched during this cycle.

2. If the READY input from memory is not high during T2 of each memory cycle, the processor will enter a wait state (TW) until READY is sampled as high.

3. States T4 and T5 are present, as required, for operations which are completely internal to the CPU. The contents of the internal bus during T4 and T5 are available at the data bus; this is designed for testing purposes only. An "X" denotes that the state is present, but is only used for such internal operations as instruction decoding.

4. Only register pairs rp = B (registers B and C) or rp = D (registers D and E) may be specified.

5. These states are skipped.

6. Memory read sub-cycles; an instruction or data word will be read.

7. Memory write sub-cycle.

8. The READY signal is not required during the second and third sub-cycles (M2 and M3). The HOLD signal is accepted during M2 and M3. The SYNC signal is not generated during M2 and M3. During the execution of DAD, M2 and M3 are required for an internal register-pair add; memory is not referenced.

9. The results of these arithmetic, logical or rotate instructions are not moved into the accumulator (A) until state T2 of the next instruction cycle. That is, A is loaded while the next instruction is being fetched; this overlapping of operations allows for faster processing.

10. If the value of the least significant 4-bits of the accumulator is greater than 9 or if the auxiliary carry bit is set, 6 is added to the accumulator. If the value of the most significant 4-bits of the accumulator is now greater than 9, or if the carry bit is set, 6 is added to the most significant 4-bits of the accumulator.

11. This represents the first sub-cycle (the instruction fetch) of the next instruction cycle.

12. If the condition was met, the contents of the register pair WZ are output on the address lines (A_{0-15}) instead of the contents of the program counter (PC).

13. If the condition was not met, sub-cycles M4 and M5 are skipped; the processor instead proceeds immediately to the instruction fetch (M1) of the next instruction cycle.

14. If the condition was not met, sub-cycles M2 and M3 are skipped; the processor instead proceeds immediately to the instruction fetch (M1) of the next instruction cycle.

15. Stack read sub-cycle.

16. Stack write sub-cycle.

17. CONDITION

CONDITION		CCC
NZ —	not zero (Z = 0)	000
Z —	zero (Z = 1)	001
NC —	no carry (CY = 0)	010
C —	carry (CY = 1)	011
PO —	parity odd (P = 0)	100
PE —	parity even (P = 1)	101
P —	plus (S = 0)	110
M —	minus (S = 1)	111

18. I/O sub-cycle: the I/O port's 8-bit select code is duplicated on address lines 0-7 (A_{0-7}) and 8-15 (A_{8-15}).

19. Output sub-cycle.

20. The processor will remain idle in the halt state until an interrupt, a reset or a hold is accepted. When a hold request is accepted, the CPU enters the hold mode; after the hold mode is terminated, the processor returns to the halt state. After a reset is accepted, the processor begins execution at memory location zero. After an interrupt is accepted, the processor executes the instruction forced onto the data bus (usually a restart instruction).

SSS or DDD	Value	rp	Value
A	111	B	00
B	000	D	01
C	001	H	10
D	010	SP	11
E	011		
H	100		
L	101		

Chapter 3
INTERFACING THE 8080
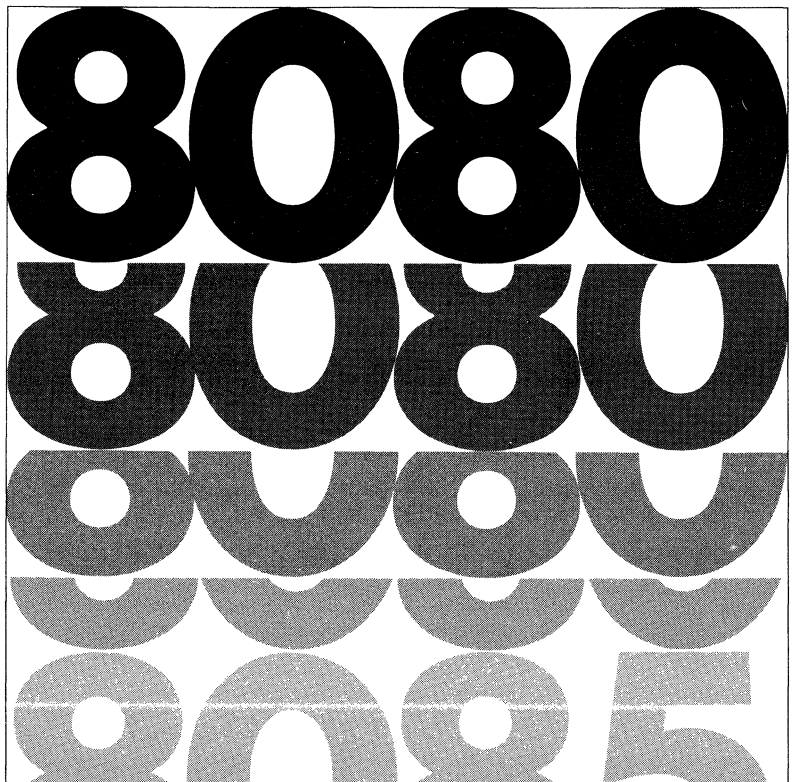
INTERFACING THE 8080

This chapter will illustrate, in detail, how to interface the 8080 CPU with Memory and I/O. It will also show the benefits and tradeoffs encountered when using a variety of system architectures to achieve higher throughput, decreased component count or minimization of memory size.

8080 Microcomputer system design lends itself to a simple, modular approach. Such an approach will yield the designer a reliable, high performance system that contains a minimum component count and is easy to manufacture and maintain.

The overall system can be thought of as a simple block diagram. The three (3) blocks in the diagram represent the functions common to **any** computer system.

CPU Module* Contains the Central Processing Unit, system timing and interface circuitry to Memory and I/O devices.

Memory Contains Read Only Memory (ROM) and Read/Write Memory (RAM) for program and data storage.

I/O Contains circuitry that allows the computer system to communicate with devices or structures existing outside of the CPU or Memory array.

for example: Keyboards, Floppy Disks, Paper Tape, etc.

There are three busses that interconnect these blocks:

Data Bus† A bi-directional path on which data can flow between the CPU and Memory or I/O.

Address Bus A uni-directional group of lines that identify a particular Memory location or I/O device.

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*"Module" refers to a functional block, it does not reference a printed circuit board manufactured by INTEL.

†"Bus" refers to a set of signals grouped together because of the similarity of their functions.

Control Bus A uni-directional set of signals that indicate the type of activity in current process.

Type of activities: 1. Memory Read
2. Memory Write
3. I/O Read
4. I/O Write
5. Interrupt Acknowledge
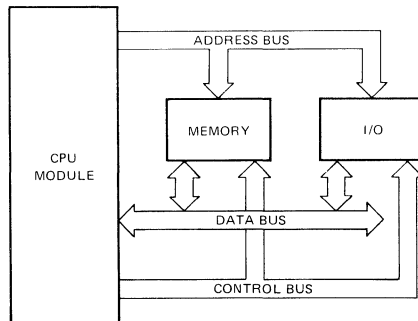
Figure 3-1. Typical Computer System Block Diagram

Basic System Operation

1. The CPU Module issues an activity command on the Control Bus.

2. The CPU Module issues a binary code on the Address Bus to identify which particular Memory location or I/O device will be involved in the current process activity.

3. The CPU Module receives or transmits data with the selected Memory location or I/O device.

4. The CPU Module returns to ① and issues the next activity command.

It is easy to see at this point that the CPU module is the central element in any computer system.

The following pages will cover the detailed design of the CPU Module with the 8080. The three Busses (Data, Address and Control) will be developed and the interconnection to Memory and I/O will be shown.

Design philosophies and system architectures presented in this manual are consistent with product development programs underway at INTEL for the MCS-80.[TM] Thus, the designer who uses this manual as a guide for his total system engineering is assured that all new developments in components and software for MCS-80 from INTEL will be compatible with his design approach.

CPU Module Design

The CPU Module contains three major areas:

1. The 8080 Central Processing Unit
2. A Clock Generator and High Level Driver
3. A bi-directional Data Bus Driver and System Control Logic

The following will discuss the design of the three major areas contained in the CPU Module. This design is presented as an alternative to the Intel® 8224 Clock Generator and Intel 8228 System Controller. By studying the alternative approach, the designer can more clearly see the considerations involved in the specification and engineering of the 8224 and 8228. Standard TTL components and Intel general purpose peripheral devices are used to implement

the design and to achieve operational characteristics that are as close as possible to those of the 8224 and 8228. Many auxiliary timing functions and features of the 8224 and 8228 are too complex to practically implement in standard components, so only the basic functions of the 8224 and 8228 are generated. Since significant benefits in system timing and component count reduction can be realized by using the 8224 and 8228, this is the preferred method of implementation.

1. 8080 CPU

The operation of the 8080 CPU was covered in previous chapters of this manual, so little reference will be made to it in the design of the Module.

2. Clock Generator and High Level Driver

The 8080 is a dynamic device, meaning that its internal storage elements and logic circuitry require a timing reference (Clock), supplied by external circuitry, to refresh and provide timing control signals.

The 8080 requires two (2) such Clocks. Their waveforms must be non-overlapping, and comply with the timing and levels specified in the 8080 A.C. and D.C. Characteristics, page 5-15.

Clock Generator Design

The Clock Generator consists of a crystal controlled,
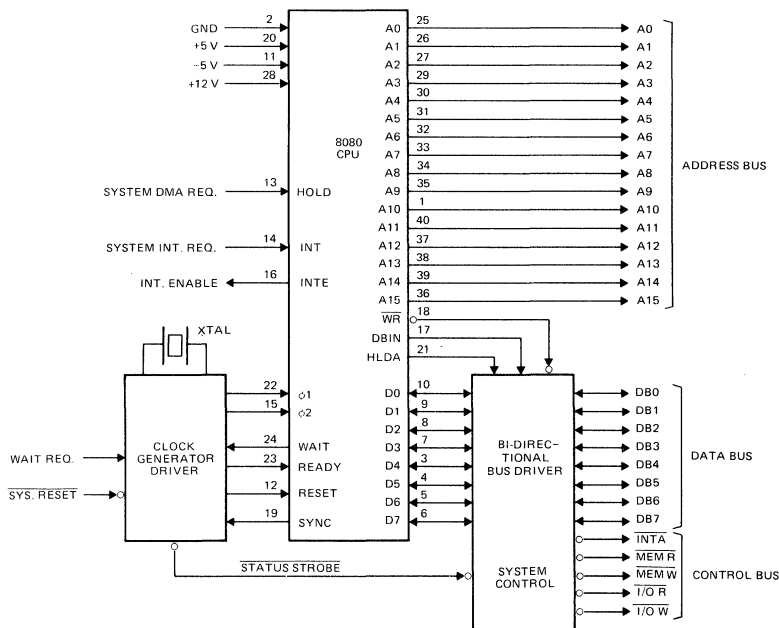
Figure 3-2. 8080 CPU Interface

OSCILLATOR

20 MHz

330   330

74S04

74S04   680 pF   74S04

OSC

CLOCK GENERATOR

CLK
DA   QA
V_{CC}
DB   QB
74163
DC   QC
GND
DD   QD
$\overline{CLR}$ LD

7486   74H00

$\overline{\phi1}$ (TTL)

7486   74H00

$\overline{\phi2}$ (TTL)

V_{CC}

74H00

AUXILIARY FUNCTIONS

SYNC

74H00
D
74S74
CLK $\overline{Q}$

$\overline{STSTB}$

$\phi1A$ (TTL)

WAIT REQ
D   Q
74S74
CLK

READY

WAVEFORMS

$\overline{\phi1}$

100 ns | 100 ns ← 50ns

$\overline{\phi2}$ 250ns

50ns ←   → 50ns

$\phi1A$ 250ns

SYNC

$\overline{STSTB}$

DMA REQ
D   Q
74S74
CLK

HOLD
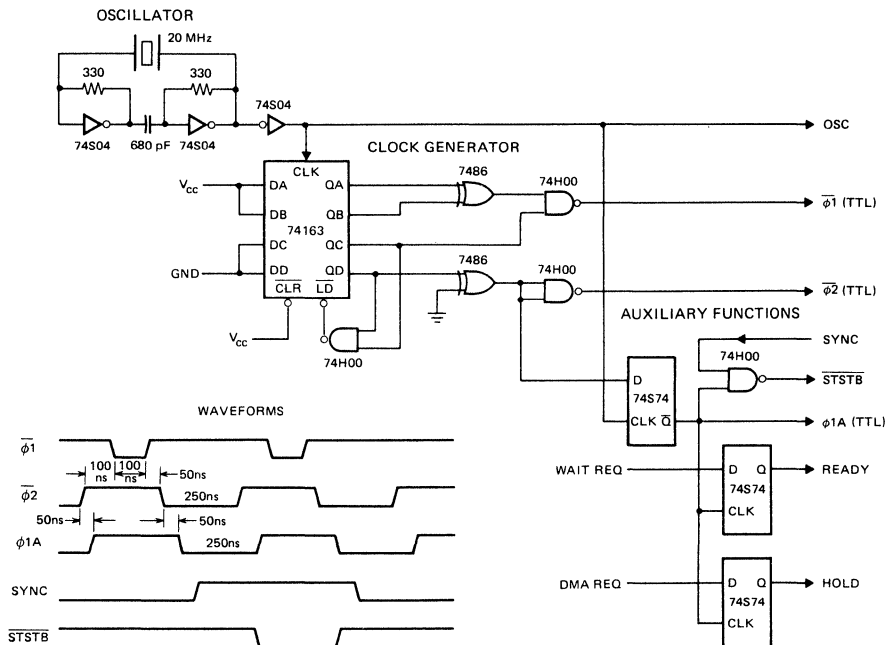
Figure 3-3. 8080 Clock Generator

20 MHZ oscillator, a four bit counter, and gating circuits.

The oscillator provides a 20 MHZ signal to the input of a four (4) bit, presettable, synchronous, binary counter. By presetting the counter as shown in figure 3-3 and clocking it with the 20 MHZ signal, a simple decoding of the counters outputs using standard TTL gates, provides proper timing for the two (2) 8080 clock inputs.

Note that the timing must actually be measured at the output of the High Level Driver to take into account the added delays and waveform distortions within such a device.

High Level Driver Design

The voltage level of the clocks for the 8080 is not TTL compatible like the other signals that input to the 8080. The voltage swing is from .6 volts (V_{ILC}) to 11 volts (V_{IHC}) with risetimes and falltimes under 50 ns. The Capacitive Drive is 20 pf (max.). Thus, a High Level Driver is required to interface the outputs of the Clock Generator (TTL) to the 8080.

The two (2) outputs of the Clock Generator are capacitivity coupled to a dual- High Level clock driver. The driver must be capable of complying with the 8080 clock input specifications, page 5-15. A driver of this type usually has little problem supplying the

positive transition when biased from the 8080 V_{DD} supply (12V) but to achieve the low voltage specification (V_{ILC}) .8 volts Max. the driver is biased to the 8080 V_{BB} supply (–5V). This allows the driver to swing from GND to V_{DD} with the aid of a simple resistor divider.

A low resistance series network is added between the driver and the 8080 to eliminate any overshoot of the pulsed waveforms. Now a circuit is apparent that can easily comply with the 8080 specifications. In fact rise and falltimes of this design are typically less than 10 ns.

+12V
6
680 pF
$\overline{\phi1}$ (TTL)   2   7   47Ω $\phi1$ (8080 PIN 22)
MH0026
OR
EQUIV.
680 pF
$\overline{\phi2}$ (TTL)   4   5   47Ω $\phi2$ (8080 PIN 15)
3
1N4002
.68 μF   15K   15K
100 Ω
–5V
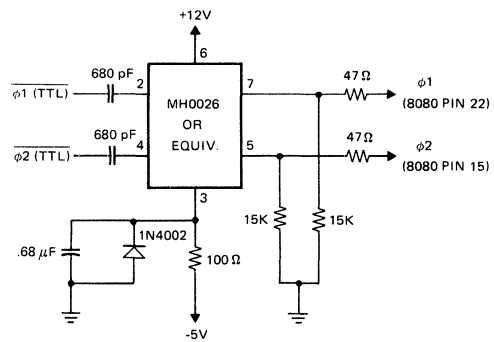
Figure 3-4. High Level Driver

Auxiliary Timing Signals and Functions

The Clock Generator can also be used to provide other signals that the designer can use to simplify large system timing or the interface to dynamic memories.

Functions such as power-on reset, synchronization of external requests (HOLD, READY, etc.) and single step, could easily be added to the Clock Generator to further enhance its capabilities.

For instance, the 20 MHZ signal from the oscillator can be buffered so that it could provide the basis for communication baud rate generation.

The Clock Generator diagram also shows how to generate an advanced timing signal (ϕ1A) that is handy to use in clocking "D" type flipflops to synchronize external requests. It can also be used to generate a strobe ($\overline{STSTB}$) that is the latching signal for the status information which is available on the Data Bus at the beginning of each machine cycle. A simple gating of the SYNC signal from the 8080 and the advanced (ϕ1A) will do the job. See Figure 3-3.

3. Bi-Directional Bus Driver and System Control Logic

The system Memory and I/O devices communicate with the CPU over the bi-directional Data Bus. The system Control Bus is used to gate data on and off the Data Bus within the proper timing sequences as dictated by the operation of the 8080 CPU. The data lines of the 8080 CPU, Memory and I/O devices are 3-state in nature, that is, their output drivers have the ability to be forced into a high-impedance mode and are, effectively, removed from the circuit. This 3-state bus technique allows the designer to construct a system around a single, eight (8) bit parallel, bi-directional Data Bus and simply gate the information on or off this bus by selecting or deselecting (3-stating) Memory and I/O devices with signals from the Control Bus.

Bi-Directional Data Bus Driver Design

The 8080 Data Bus (D7-D0) has two (2) major areas of concern for the designer:

1. Input Voltage level (V_{IH}) 3.3 volts minimum.

2. Output Drive Capability (I_{OL}) 1.7 mA maximum.
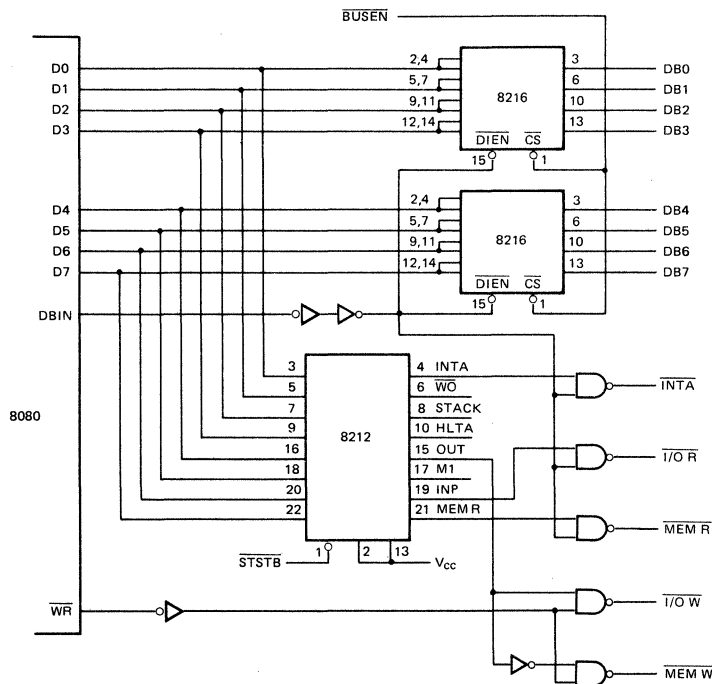
Figure 3-5. 8080 System Control

The input level specification implies that any semi-conductor memory or I/O device connected to the 8080 Data Bus must be able to provide a minimum of 3.3 volts in its high state. Most semiconductor memories and standard TTL I/O devices have an output capability of between 2.0 and 2.8 volts, obviously a direct connection onto the 8080 Data Bus would require pullup resistors, whose value should not affect the bus speed or stress the drive capability of the memory or I/O components.

The 8080A output drive capability (I_{OL}) 1.9mA max. is sufficient for small systems where Memory size and I/O requirements are minimal and the entire system is contained on a single printed circuit board. Most systems however, take advantage of the high-performance computing power of the 8080 CPU and thus a more typical system would require some form of buffering on the 8080 Data Bus to support a larger array of Memory and I/O devices which are likely to be on separate boards.

A device specifically designed to do this buffering function is the INTEL® 8216, a (4) four bit bi-directional bus driver whose input voltage level is compatible with standard TTL devices and semiconductor memory components, and has output drive capability of 50 mA. At the 8080 side, the 8216 has a "high" output of 3.65 volts that not only meets the 8080 input spec but provides the designer with a worse case 350 mV noise margin.

A pair of 8216's are connected directly to the 8080 Data Bus (D7-D0) as shown in figure 3-5. Note that the DBIN signal from the 8080 is connected to the direction control input ($\overline{DIEN}$) so the correct flow of data on the bus is maintained. The chip select ($\overline{CS}$) of the 8216 is connected to BUS ENABLE ($\overline{BUSEN}$) to allow for DMA activities by deselecting the Data Bus Buffer and forcing the outputs of the 8216's into their high impedance (3-state) mode. This allows other devices to gain access to the data bus (DMA).

System Control Logic Design

The Control Bus maintains discipline of the bi-directional Data Bus, that is, it determines what type of device will have access to the bus (Memory or I/O) and generates signals to assure that these devices transfer Data with the 8080 CPU within the proper timing "windows" as dictated by the CPU operational characteristics.

As described previously, the 8080 issues Status information at the beginning of each Machine Cycle on its Data Bus to indicate what operation will take place during that cycle. A simple (8) bit latch, like an INTEL® 8212, connected directly to the 8080 Data Bus (D7-D0) as shown in figure 3-5 will store the

Status information. The signal that loads the data into the Status Latch comes from the Clock Generator, it is Status Strobe ($\overline{STSTB}$) and occurs at the start of each Machine Cycle.

Note that the Status Latch is connected onto the 8080 Data Bus (D7-D0) before the Bus Buffer. This is to maintain the integrity of the Data Bus and simplify Control Bus timing in DMA dependent environments.

As shown in the diagram, a simple gating of the outputs of the Status Latch with the DBIN and $\overline{WR}$ signals from the 8080 generate the (4) four Control signals that make up the basic Control Bus.

These four signals: 1. Memory Read ($\overline{MEM\ R}$)

2. Memory Write ($\overline{MEM\ W}$)

3. I/O Read ($\overline{I/O\ R}$)

4. I/O Write ($\overline{I/O\ W}$)

connect directly to the MCS-80™ component "family" of ROMs, RAMs and I/O devices.

A fifth signal, Interrupt Acknowledge ($\overline{INTA}$) is added to the Control Bus by gating data off the Status Latch with the DBIN signal from the 8080 CPU. This signal is used to enable the Interrupt Instruction Port which holds the RST instruction onto the Data Bus.

Other signals that are part of the Control Bus such as $\overline{WO}$, Stack and M1 are present to aid in the testing of the System and also to simplify interfacing the CPU to dynamic memories or very large systems that require several levels of bus buffering.

Address Buffer Design

The Address Bus (A15-A0) of the 8080, like the Data Bus, is sufficient to support a small system that has a moderate size Memory and I/O structure, confined to a single card. To expand the size of the system that the Address Bus can support a simple buffer can be added, as shown in figure 3-6. The INTEL® 8212 or 8216 is an excellent device for this function. They provide low input loading (.25 mA), high output drive and insert a minimal delay in the System Timing.

Note that BUS ENABLE ($\overline{BUSEN}$) is connected to the buffers so that they are forced into their high-impedance (3-state) mode during DMA activities so that other devices can gain access to the Address Bus.

INTERFACING THE 8080 CPU TO MEMORY AND I/O DEVICES

The 8080 interfaces with standard semiconductor Memory components and I/O devices. In the previous text the proper control signals and buffering were developed which will produce a simple bus system similar to the basic system example shown at the beginning of this chapter.

In Figure 3-6 a simple, but exact 8080 typical system is shown that can be used as a guide for **any** 8080 system, regardless of size or complexity. It is a "three bus" architecture, using the signals developed in the CPU module.

Note that Memory and I/O devices interface in the same manner and that their isolation is only a function of the definition of the Read-Write signals on the Control Bus. This allows the 8080 system to be configured so that Memory and I/O are treated as a single array (memory mapped I/O) for small systems that require high thruput and have less than 32K memory size. This approach will be brought out later in the chapter.

ROM INTERFACE

A ROM is a device that stores data in the form of Program or other information such as "look-up tables" and is only read from, thus the term Read Only Memory. This type of memory is generally non-volatile, meaning that when the power is removed the information is retained.

This feature eliminates the need for extra equipment like tape readers and disks to load programs initially, an important aspect in small system design.

Interfacing standard ROMs, such as the devices shown in the diagram is simple and direct. The output Data lines are connected to the bi-directional Data Bus, the Address inputs tie to the Address bus with possible decoding of the most significant bits as "chip selects" and the $\overline{MEMR}$ signal from the Control Bus connected to a "chip select" or data buffer. Basically, the CPU issues an address during the first portion of an instruction or data fetch (T1 & T2). This value on the Address Bus selects a specific location within the ROM, then depending on the ROM's delay (access time) the data stored at the addressed location is present at the Data output lines. At this time (T3) the CPU Data Bus is in the "input Mode" and the control logic issues a Memory Read command ($\overline{MEMR}$) that gates the addressed data on to the Data Bus.

RAM INTERFACE

A RAM is a device that stores data. This data can be program, active "look-up tables," temporary values or external stacks. The difference between RAM and ROM is that data can be written into such devices and are in essence, Read/Write storage elements. RAMs do not hold their data when power is removed so in the case where Program or "look-up tables" data is stored a method to load
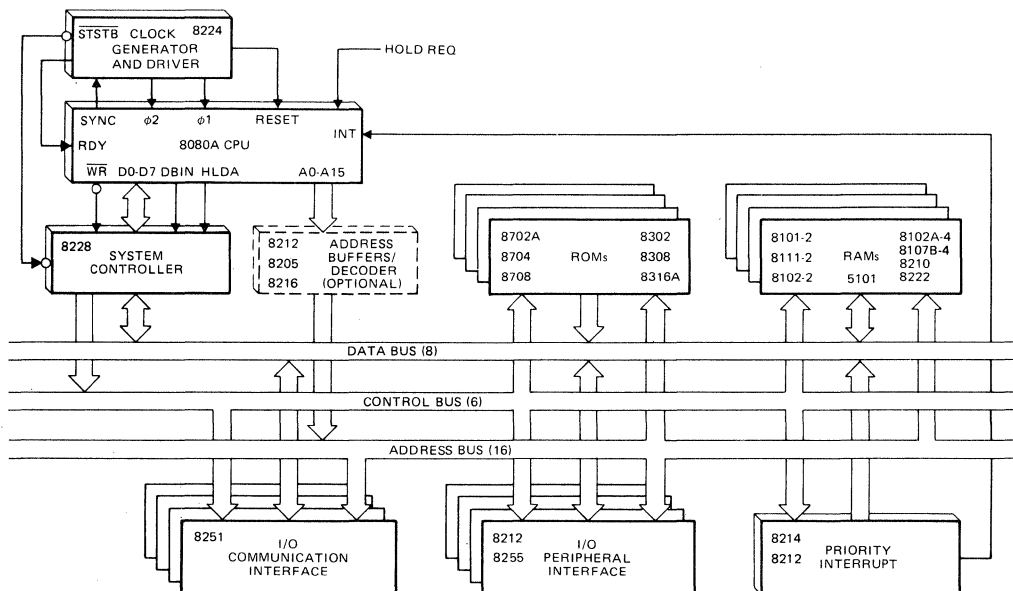
Figure 3-6. Microcomputer System

RAM memory must be provided, such as: Floppy Disk, Paper Tape, etc.

The CPU treats RAM in exactly the same manner as ROM for addressing data to be read. Writing data is very similar; the RAM is issued an address during the first portion of the Memory Write cycle (T1 & T2) in T3 when the data that is to be written is output by the CPU and is stable on the bus an $\overline{MEMW}$ command is generated. The $\overline{MEMW}$ signal is connected to the R/W input of the RAM and strobes the data into the addressed location.

In Figure 3-7 a typical Memory system is illustrated to show how standard semiconductor components interface to the 8080 bus. The memory array shown has 8K bytes (8 bits/byte) of ROM storage, using four Intel®8216As and 512 bytes of RAM storage, using Intel 8111 static RAMs. The basic interface to the bus structure detailed here is common to almost any size memory. The only addition that might have to be made for larger systems is more buffers (8216/8212) and decoders (8205) for generating "chip selects."

The memories chosen for this example have an access time of 850 nS (max) to illustrate that slower, economical devices can be easily interfaced to the 8080 with little effect on performance. When the 8080 is operated from a clock generator with a tCY of 500 nS the required memory access time is Approx. 450-550 nS. See detailed timing specification Pg. 5-16. Using memory devices of this speed such as Intel®8308, 8102A, 8107A, etc. the READY input to the 8080 CPU can remain "high" because no "wait" states are required. Note that the bus interface to memory shown in Figure 3-7 remains the same. However, if slower memories are to be used, such as the devices illustrated (8316A, 8111) that have access times slower than the minimum requirement a simple logic control of the READY input to the 8080 CPU will insert an extra "wait state" that is equal to one or more clock periods as an access time "adjustment" delay to compensate. The effect of the extra "wait" state is naturally a slower execution time for the instruction. A single "wait" changes the basic instruction cycle to 2.5 microSeconds.
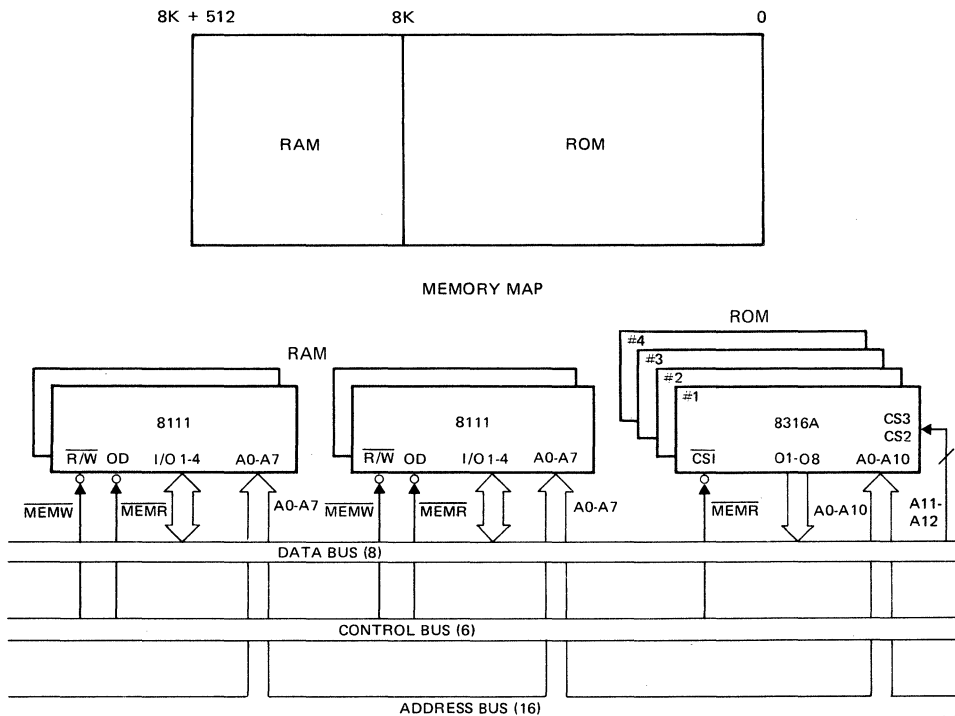
Figure 3-7. Typical Memory Interface

3-7

I/O INTERFACE

General Theory

As in any computer based system, the 8080 CPU must be able to communicate with devices or structures that exist outside its normal memory array. Devices like keyboards, paper tape, floppy disks, printers, displays and other control structures are used to input information into the 8080 CPU and display or store the results of the computational activity.

Probably the most important and strongest feature of the 8080 Microcomputer System is the flexibility and power of its I/O structure and the components that support it. There are many ways to structure the I/O array so that it will "fit" the total system environment to maximize efficiency and minimize component count.

The basic operation of the I/O structure can best be viewed as an array of single byte memory locations that can be Read from or Written into. The 8080 CPU has special instructions devoted to managing such transfers (IN, OUT). These instructions generally isolate memory and I/O arrays so that memory address space is not effected by the I/O structure and the general concept is that of a simple transfer to or from the Accumulator with an addressed "PORT". Another method of I/O architecture is to treat the I/O structure as part of the Memory array. This is generally referred to as "Memory Mapped I/O" and provides the designer with a powerful new "instruction set" devoted to I/O manipulation.
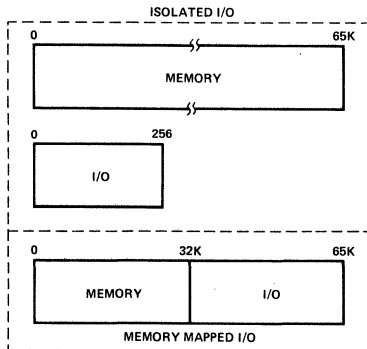
Figure 3-8. Memory/I/O Mapping.

### Isolated I/O

In Figure 3-9 the system control signals, previously detailed in this chapter, are shown. This type of I/O architecture separates the memory address space from the I/O address space and uses a conceptually simple transfer to or from Accumulator technique. Such an architecture is easy to understand because I/O communicates only with the Accumulator using the IN or OUT instructions. Also because of the isolation of memory and I/O, the full address space (65K) is uneffected by I/O addressing.
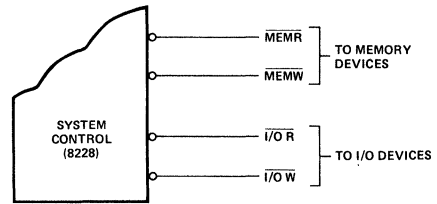
Figure 3-9. Isolated I/O.

Memory Mapped I/O

By assigning an area of memory address space as I/O a powerful architecture can be developed that can manipulate I/O using the same instructions that are used to manipulate memory locations. Thus, a "new" instruction set is created that is devoted to I/O handling.

As shown in Figure 3-10, new control signals are generated by gating the $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ signals with A_{15}, the most significant address bit. The new I/O control signals connect in exactly the same manner as Isolated I/O, thus the system bus characteristics are unchanged.

By assigning A_{15} as the I/O "flag", a simple method of I/O discipline is maintained:

If A_{15} is a "zero" then Memory is active.
If A_{15} is a "one" then I/O is active.

Other address bits can also be used for this function. A_{15} was chosen because it is the most significant address bit so it is easier to control with software and because it still allows memory addressing of 32K.

I/O devices are still considered addressed "ports" but instead of the Accumulator as the only transfer medium any of the internal registers can be used. All instructions that could be used to operate on memory locations can be used in I/O.

Examples:

MOVr, M	(Input Port to any Register)
MOV M, r	(Output any Register to Port)
MVI M	(Output immediate data to Port)
LDA	(Input to ACC)
STA	(Output from ACC to Port)
LHLD	(16 Bit Input)
SHLD	(16 Bit Output)
ADD M	(Add Port to ACC)
ANA M	("AND" Port with ACC)

It is easy to see that from the list of possible "new" instructions that this type of I/O architecture could have a drastic effect on increased system throughput. It is conceptually more difficult to understand than Isolated I/O and it does limit memory address space, but Memory Mapped I/O can mean a significant increase in overall speed and at the same time reducing required program memory area.
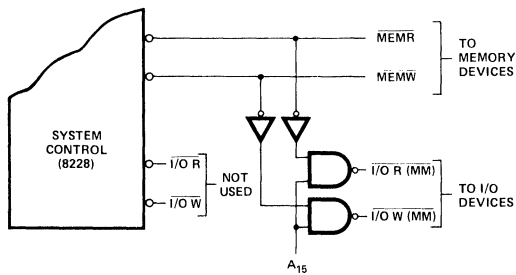
Figure 3-10. Memory Mapped I/O.

I/O Addressing

With both systems of I/O structure the addressing of each device can be configured to optimize efficiency and reduce component count. One method, the most common, is to decode the address bus into exclusive "chip selects" that enable the addressed I/O device, similar to generating chip-selects in memory arrays.

Another method is called "linear select". In this method, instead of decoding the Address Bus, a singular bit from the bus is assigned as the exclusive enable for a specific I/O device. This method, of course, limits the number of I/O devices that can be addressed but eliminates the need for extra decoders, an important consideration in small system design.

A simple example illustrates the power of such a flexible I/O structure. The first example illustrates the format of the second byte of the IN or OUT instruction using the Isolated I/O technique. The devices used are Intel®8255 Programmable Peripheral Interface units and are linear selected. Each device has three ports and from the format it can be seen that six devices can be addressed without additional decoders.

EXAMPLE #1

ADDRESSES — 6 — 8255s
(18 PORTS — 144 BITS)
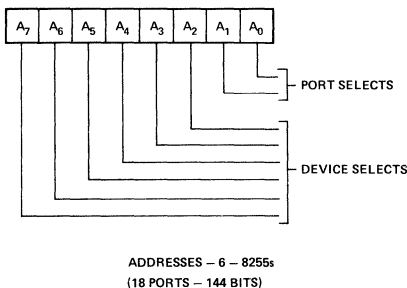
Figure 3-11. Isolated I/O — (Linear Select) (8255)

The second example uses Memory Mapped I/O and linear select to show how thirteen devices (8255) can be addressed without the use of extra decoders. The format shown could be the second and third bytes of the LDA or STA instructions or any other instructions used to manipulate I/O using the Memory Mapped technique.

It is easy to see that such a flexible I/O structure, that can be "tailored" to the overall system environment, provides the designer with a powerful tool to optimize efficiency and minimize component count.

EXAMPLE #2

ADDRESSES — 13 — 8255s
(39 PORTS — 312 BITS)
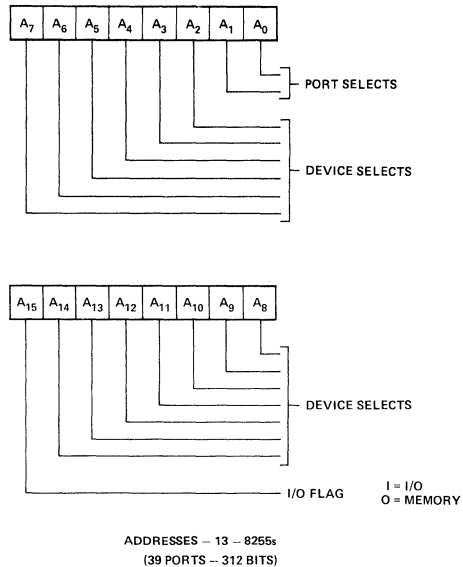
Figure 3-12. Memory Mapped I/O — (Linear Select (8255)

I/O Interface Example

In Figure 3-16 a typical I/O system is shown that uses a variety of devices (8212, 8251 and 8255). It could be used to interface the peripherals around an intelligent CRT terminals; keyboards, display, and communication interface. Another application could be in a process controller to interface sensors, relays, and motor controls. The limitation of the application area for such a circuit is solely that of the designers imagination.

The I/O structure shown interfaces to the 8080 CPU using the bus architecture developed previously in this chapter. Either Isolated or Memory Mapped techniques can be used, depending on the system I/O environment.

The 8251 provides a serial data communication interface so that the system can transmit and receive data over communication links such as telephone lines.
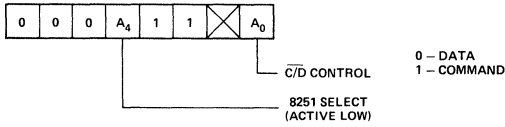
Figure 3-13. 8251 Format.

The two (2) 8255s provide twenty four bits each of programmable I/O data and control so that keyboards, sensors, paper tape, etc., can be interfaced to the system.
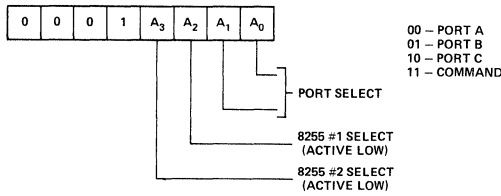
Figure 3-14. 8255 Format.

The three 8212s can be used to drive long lines or LED indicators due to their high drive capability. (15mA)
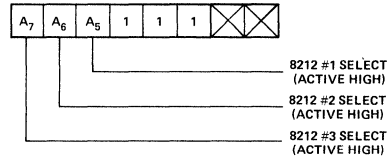
Figure 3-15. 8212 Format.

Addressing the structure is described in the formats illustrated in Figures 3-13, 3-14, 3-15. Linear Select is used so that no decoders are required thus, each device has an exclusive "enable bit".

The example shows how a powerful yet flexible I/O structure can be created using a minimum component count with devices that are all members of the 8080 Microcomputer System.
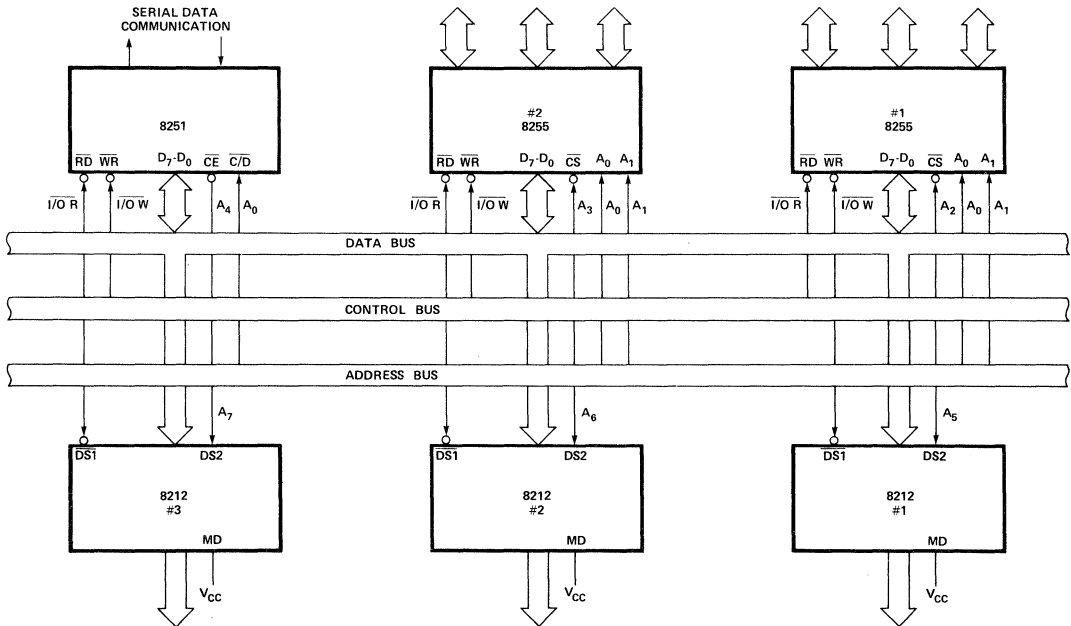
Figure 3-16. Typical I/O Interface.

Chapter 4
INSTRUCTION SET
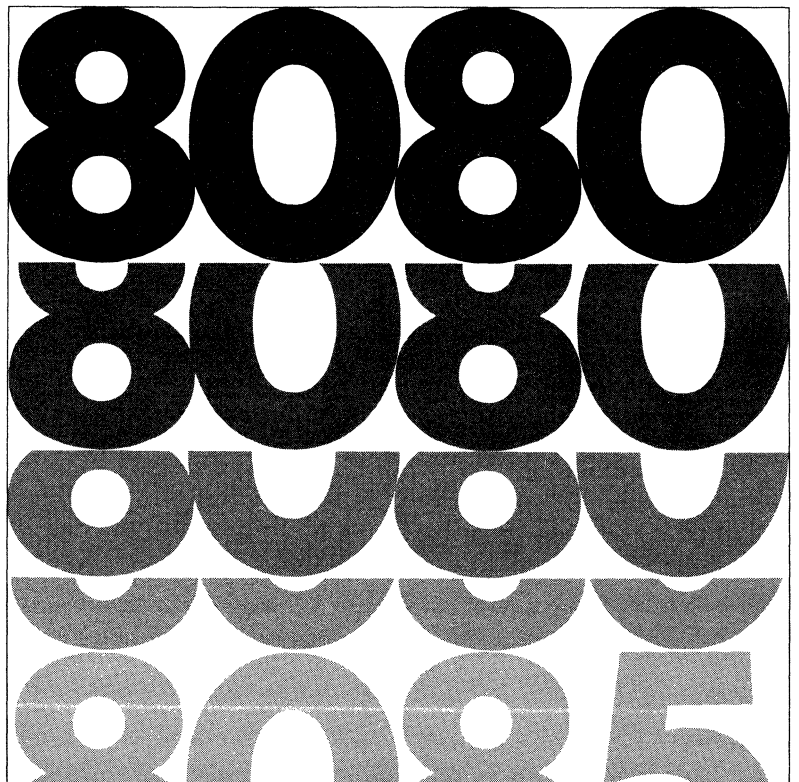
INSTRUCTION SET

A computer, no matter how sophisticated, can only do what it is "told" to do. One "tells" the computer what to do via a series of coded instructions referred to as a **Program**. The realm of the programmer is referred to as **Software**, in contrast to the **Hardware** that comprises the actual computer equipment. A computer's software refers to all of the programs that have been written for that computer.

When a computer is designed, the engineers provide the Central Processing Unit (CPU) with the ability to perform a particular set of operations. The CPU is designed such that a specific operation is performed when the CPU control logic decodes a particular instruction. Consequently, the operations that can be performed by a CPU define the computer's **Instruction Set**.

Each computer instruction allows the programmer to initiate the performance of a specific operation. All computers implement certain arithmetic operations in their instruction set, such as an instruction to add the contents of two registers. Often logical operations (e.g., OR the contents of two registers) and register operate instructions (e.g., increment a register) are included in the instruction set. A computer's instruction set will also have instructions that move data between registers, between a register and memory, and between a register and an I/O device. Most instruction sets also provide **Conditional Instructions**. A conditional instruction specifies an operation to be performed only if certain conditions have been met; for example, jump to a particular instruction if the result of the last operation was zero. Conditional instructions provide a program with a decision-making capability.

By logically organizing a sequence of instructions into a coherent program, the programmer can "tell" the computer to perform a very specific and useful function.

The computer, however, can only execute programs whose instructions are in a binary coded form (i.e., a series of 1's and 0's), that is called **Machine Code**. Because it would be extremely cumbersome to program in machine code, programming languages have been developed. There are programs available which convert the programming language instructions into machine code that can be interpreted by the processor.

One type of programming language is **Assembly Language**. A unique assembly language mnemonic is assigned to each of the computer's instructions. The programmer can write a program (called the **Source Program**) using these mnemonics and certain operands; the source program is then converted into machine instructions (called the **Object Code**). Each assembly language instruction is converted into one machine code instruction (1 or more bytes) by an **Assembler** program. Assembly languages are usually machine dependent (i.e., they are usually able to run on only one type of computer).

THE 8080 INSTRUCTION SET

The 8080 instruction set includes five different types of instructions:

- **Data Transfer Group** — move data between registers or between memory and registers
- **Arithmetic Group** — add, subtract, increment or decrement data in registers or in memory
- **Logical Group** — AND, OR, EXCLUSIVE-OR, compare, rotate or complement data in registers or in memory
- **Branch Group** — conditional and unconditional jump instructions, subroutine call instructions and return instructions
- **Stack, I/O and Machine Control Group** — includes I/O instructions, as well as instructions for maintaining the stack and internal control flags.

Instruction and Data Formats:

Memory for the 8080 is organized into 8-bit quantities, called Bytes. Each byte has a unique 16-bit binary address corresponding to its sequential position in memory.

The 8080 can directly address up to 65,536 bytes of memory, which may consist of both read-only memory (ROM) elements and random-access memory (RAM) elements (read/write memory).

Data in the 8080 is stored in the form of 8-bit binary integers:

DATA WORD

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB   LSB
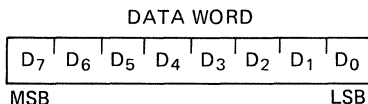
When a register or data word contains a binary number, it is necessary to establish the order in which the bits of the number are written. In the Intel 8080, BIT 0 is referred to as the **Least Significant Bit (LSB)**, and BIT 7 (of an 8 bit number) is referred to as the **Most Significant Bit (MSB)**.

The 8080 program instructions may be one, two or three bytes in length. Multiple byte instructions must be stored in successive memory locations; the address of the first byte is always used as the address of the instructions. The exact instruction format will depend on the particular operation to be executed.

Single Byte Instructions

| D_7 | | | | | | | D_0 | Op Code |

Two-Byte Instructions

Byte One | D_7 | | | | | | | D_0 | Op Code

Byte Two | D_7 | | | | | | | D_0 | Data or Address

Three-Byte Instructions

Byte One | D_7 | | | | | | | D_0 | Op Code

Byte Two | D_7 | | | | | | | D_0 | Data or Address

Byte Three | D_7 | | | | | | | D_0 |
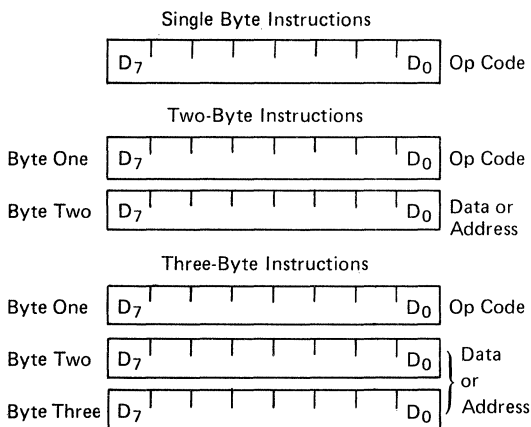
Addressing Modes:

Often the data that is to be operated on is stored in memory. When multi-byte numeric data is used, the data, like instructions, is stored in successive memory locations, with the least significant byte first, followed by increasingly significant bytes. The 8080 has four different modes for addressing data stored in memory or in registers:

- Direct — Bytes 2 and 3 of the instruction contain the exact memory address of the data item (the low-order bits of the address are in byte 2, the high-order bits in byte 3).

- Register — The instruction specifies the register or register-pair in which the data is located.

- Register Indirect — The instruction specifies a register-pair which contains the memory address where the data is located (the high-order bits of the address are in the first register of the pair, the low-order bits in the second).

- Immediate — The instruction contains the data itself. This is either an 8-bit quantity or a 16-bit quantity (least significant byte first, most significant byte second).

Unless directed by an interrupt or branch instruction, the execution of instructions proceeds through consecutively increasing memory locations. A branch instruction can specify the address of the next instruction to be executed in one of two ways:

- Direct — The branch instruction contains the address of the next instruction to be executed. (Except for the 'RST' instruction, byte 2 contains the low-order address and byte 3 the high-order address.)

- Register indirect — The branch instruction indicates a register-pair which contains the address of the next instruction to be executed. (The high-order bits of the address are in the first register of the pair, the low-order bits in the second.)

The RST instruction is a special one-byte call instruction (usually used during interrupt sequences). RST includes a three-bit field; program control is transferred to the instruction whose address is eight times the contents of this three-bit field.

Condition Flags:

There are five condition flags associated with the execution of instructions on the 8080. They are Zero, Sign, Parity, Carry, and Auxiliary Carry, and are each represented by a 1-bit register in the CPU. A flag is "set" by forcing the bit to 1; "reset" by forcing the bit to 0.

Unless indicated otherwise, when an instruction affects a flag, it affects it in the following manner:

Zero: If the result of an instruction has the value 0, this flag is set; otherwise it is reset.

Sign: If the most significant bit of the result of the operation has the value 1, this flag is set; otherwise it is reset.

Parity: If the modulo 2 sum of the bits of the result of the operation is 0, (i.e., if the result has even parity), this flag is set; otherwise it is reset (i.e., if the result has odd parity).

Carry: If the instruction resulted in a carry (from addition), or a borrow (from subtraction or a comparison) out of the high-order bit, this flag is set; otherwise it is reset.

Auxiliary Carry: If the instruction caused a carry out of bit 3 and into bit 4 of the resulting value, the auxiliary carry is set; otherwise it is reset. This flag is affected by single precision additions, subtractions, increments, decrements, comparisons, and logical operations, but is principally used with additions and increments preceding a DAA (Decimal Adjust Accumulator) instruction.

Symbols and Abbreviations:

The following symbols and abbreviations are used in the subsequent description of the 8080 instructions:

SYMBOLS	MEANING
accumulator	Register A
addr	16-bit address quantity
data	8-bit data quantity
data 16	16-bit data quantity
byte 2	The second byte of the instruction
byte 3	The third byte of the instruction
port	8-bit address of an I/O device
r,r1,r2	One of the registers A,B,C,D,E,H,L
DDD,SSS	The bit pattern designating one of the registers A,B,C,D,E,H,L (DDD=destination, SSS= source):

DDD or SSS	REGISTER NAME
111	A
000	B
001	C
010	D
011	E
100	H
101	L

rp   One of the register pairs:

B represents the B,C pair with B as the high-order register and C as the low-order register;

D represents the D,E pair with D as the high-order register and E as the low-order register;

H represents the H,L pair with H as the high-order register and L as the low-order register;

SP represents the 16-bit stack pointer register.

RP   The bit pattern designating one of the register pairs B,D,H,SP:

RP	REGISTER PAIR
00	B-C
01	D-E
10	H-L
11	SP

rh   The first (high-order) register of a designated register pair.

rl   The second (low-order) register of a designated register pair.

PC   16-bit program counter register (PCH and PCL are used to refer to the high-order and low-order 8 bits respectively).

SP   16-bit stack pointer register (SPH and SPL are used to refer to the high-order and low-order 8 bits respectively).

r_m Bit m of the register r (bits are number 7 through 0 from left to right).

Z,S,P,CY,AC   The condition flags:
Zero,
Sign,
Parity,
Carry,
and Auxiliary Carry, respectively.

( )   The contents of the memory location or registers enclosed in the parentheses.

◄───   "Is transferred to"

∧   Logical AND

∀   Exclusive OR

∨   Inclusive OR

+   Addition

−   Two's complement subtraction

*   Multiplication

◄──►   "Is exchanged with"

‾‾   The one's complement (e.g., $(\overline{A})$)

n   The restart number 0 through 7

NNN   The binary representation 000 through 111 for restart number 0 through 7 respectively.

Description Format:

The following pages provide a detailed description of the instruction set of the 8080. Each instruction is described in the following manner:

1. The MAC 80 assembler format, consisting of the instruction mnemonic and operand fields, is printed in **BOLDFACE** on the left side of the first line.

2. The name of the instruction is enclosed in parenthesis on the right side of the first line.

3. The next line(s) contain a symbolic description of the operation of the instruction.

4. This is followed by a narative description of the operation of the instruction.

5. The following line(s) contain the binary fields and patterns that comprise the machine instruction.

6. The last four lines contain incidental information about the execution of the instruction. The number of machine cycles and states required to execute the instruction are listed first. If the instruction has two possible execution times, as in a Conditional Jump, both times will be listed, separated by a slash. Next, any significant data addressing modes (see Page 4-2) are listed. The last line lists any of the five Flags that are affected by the execution of the instruction.

Data Transfer Group:

This group of instructions transfers data to and from registers and memory. **Condition flags are not affected** by any instruction in this group.

MOV r1, r2   (Move Register)

(r1) ← (r2)

The content of register r2 is moved to register r1.

0	1	D	D	D	S	S	S
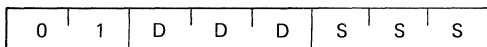
Cycles: 1
States: 5
Addressing: register
Flags: none

MOV r, M   (Move from memory)

(r) ← ((H) (L))

The content of the memory location, whose address is in registers H and L, is moved to register r.

0	1	D	D	D	1	1	0
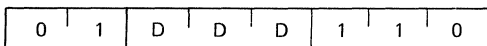
Cycles: 2
States: 7
Addressing: reg. indirect
Flags: none

MOV M, r   (Move to memory)

((H) (L)) ← (r)

The content of register r is moved to the memory location whose address is in registers H and L.

0	1	1	1	0	S	S	S
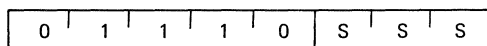
Cycles: 2
States: 7
Addressing: reg. indirect
Flags: none

MVI r, data   (Move Immediate)

(r) ← (byte 2)

The content of byte 2 of the instruction is moved to register r.

0	0	D	D	D	1	1	0
data							
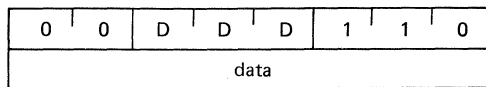
Cycles: 2
States: 7
Addressing: immediate
Flags: none

MVI M, data   (Move to memory immediate)

((H) (L)) ← (byte 2)

The content of byte 2 of the instruction is moved to the memory location whose address is in registers H and L.

0	0	1	1	0	1	1	0
data							
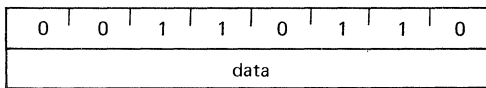
Cycles: 3
States: 10
Addressing: immed./reg. indirect
Flags: none

LXI rp, data 16   (Load register pair immediate)

(rh) ← (byte 3),

(rl) ← (byte 2)

Byte 3 of the instruction is moved into the high-order register (rh) of the register pair rp. Byte 2 of the instruction is moved into the low-order register (rl) of the register pair rp.

0	0	R	P	0	0	0	1
low-order data							
high-order data							
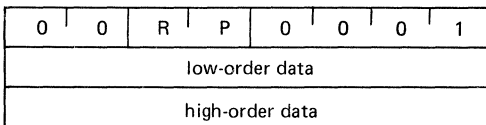
Cycles: 3
States: 10
Addressing: immediate
Flags: none

LDA addr   (Load Accumulator direct)

(A) ← ((byte 3)(byte 2))

The content of the memory location, whose address is specified in byte 2 and byte 3 of the instruction, is moved to register A.

0	0	1	1	1	0	1	0
low-order addr							
high-order addr							
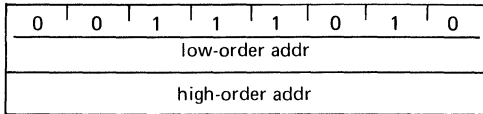
Cycles: 4
States: 13
Addressing: direct
Flags: none

STA addr   (Store Accumulator direct)

((byte 3)(byte 2)) ← (A)

The content of the accumulator is moved to the memory location whose address is specified in byte 2 and byte 3 of the instruction.

0	0	1	1	0	0	1	0
low-order addr							
high-order addr							
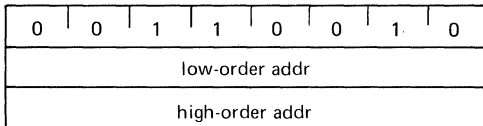
Cycles: 4
States: 13
Addressing: direct
Flags: none

LHLD addr   (Load H and L direct)

(L) ← ((byte 3)(byte 2))

(H) ← ((byte 3)(byte 2) + 1)

The content of the memory location, whose address is specified in byte 2 and byte 3 of the instruction, is moved to register L. The content of the memory location at the succeeding address is moved to register H.

0	0	1	0	1	0	1	0
low-order addr							
high-order addr							
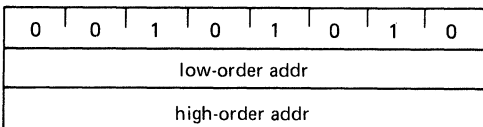
Cycles: 5
States: 16
Addressing: direct
Flags: none

SHLD addr   (Store H and L direct)

((byte 3)(byte 2)) ← (L)

((byte 3)(byte 2) + 1) ← (H)

The content of register L is moved to the memory location whose address is specified in byte 2 and byte 3. The content of register H is moved to the succeeding memory location.

0	0	1	0	0	0	1	0
low-order addr							
high-order addr							
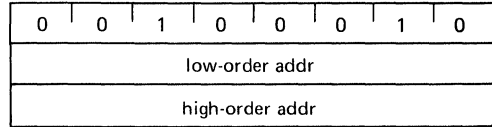
Cycles: 5
States: 16
Addressing: direct
Flags: none

LDAX rp   (Load accumulator indirect)

(A) ← ((rp))

The content of the memory location, whose address is in the register pair rp, is moved to register A. Note: only register pairs rp=B (registers B and C) or rp=D (registers D and E) may be specified.

0	0	R	P	1	0	1	0
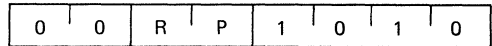
Cycles: 2
States: 7
Addressing: reg. indirect
Flags: none

STAX rp   (Store accumulator indirect)

((rp)) ← (A)

The content of register A is moved to the memory location whose address is in the register pair rp. Note: only register pairs rp=B (registers B and C) or rp=D (registers D and E) may be specified.

0	0	R	P	0	0	1	0
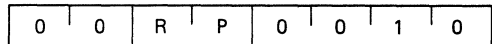
Cycles: 2
States: 7
Addressing: reg. indirect
Flags: none

XCHG   (Exchange H and L with D and E)

(H) ↔ (D)

(L) ↔ (E)

The contents of registers H and L are exchanged with the contents of registers D and E.

1	1	1	0	1	0	1	1
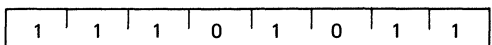
Cycles: 1
States: 4
Addressing: register
Flags: none

Arithmetic Group:

This group of instructions performs arithmetic operations on data in registers and memory.

Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Carry, and Auxiliary Carry flags according to the standard rules.

All subtraction operations are performed via two's complement arithmetic and set the carry flag to one to indicate a borrow and clear it to indicate no borrow.

ADD r   (Add Register)

(A) ◀— (A) + (r)

The content of register r is added to the content of the accumulator. The result is placed in the accumulator.

1	0	0	0	0	S	S	S
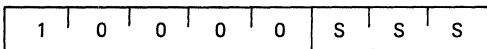
Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

ADD M   (Add memory)

(A) ◀— (A) + ((H) (L))

The content of the memory location whose address is contained in the H and L registers is added to the content of the accumulator. The result is placed in the accumulator.

1	0	0	0	0	1	1	0
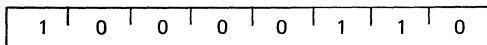
Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

ADI data   (Add immediate)

(A) ◀— (A) + (byte 2)

The content of the second byte of the instruction is added to the content of the accumulator. The result is placed in the accumulator.

1	1	0	0	0	1	1	0
data							
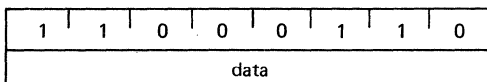
Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

ADC r   (Add Register with carry)

(A) ◀— (A) + (r) + (CY)

The content of register r and the content of the carry bit are added to the content of the accumulator. The result is placed in the accumulator.

1	0	0	0	1	S	S	S
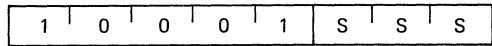
Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

ADC M   (Add memory with carry)

(A) ◀— (A) + ((H) (L)) + (CY)

The content of the memory location whose address is contained in the H and L registers and the content of the CY flag are added to the accumulator. The result is placed in the accumulator.

1	0	0	0	1	1	1	0
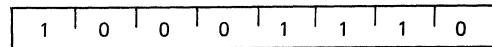
Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

ACI data   (Add immediate with carry)

(A) ◀— (A) + (byte 2) + (CY)

The content of the second byte of the instruction and the content of the CY flag are added to the contents of the accumulator. The result is placed in the accumulator.

1	1	0	0	1	1	1	0
data							
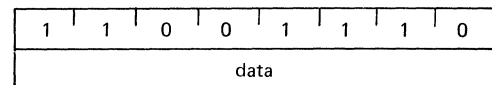
Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

SUB r   (Subtract Register)

(A) ◀— (A) − (r)

The content of register r is subtracted from the content of the accumulator. The result is placed in the accumulator.

1	0	0	1	0	S	S	S
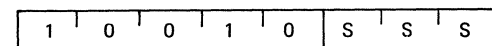
Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

SUB M (Subtract memory)

(A) ← (A) − ((H) (L))

The content of the memory location whose address is contained in the H and L registers is subtracted from the content of the accumulator. The result is placed in the accumulator.

1	0	0	1	0	1	1	0

Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

SUI data (Subtract immediate)

(A) ← (A) − (byte 2)

The content of the second byte of the instruction is subtracted from the content of the accumulator. The result is placed in the accumulator.

1	1	0	1	0	1	1	0
data							

Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

SBB r (Subtract Register with borrow)

(A) ← (A) − (r) − (CY)

The content of register r and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

1	0	0	1	1	S	S	S

Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

SBB M (Subtract memory with borrow)

(A) ← (A) − ((H) (L)) − (CY)

The content of the memory location whose address is contained in the H and L registers and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

1	0	0	1	1	1	1	0

Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

SBI data (Subtract immediate with borrow)

(A) ← (A) − (byte 2) − (CY)

The contents of the second byte of the instruction and the contents of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

1	1	0	1	1	1	1	0
data							

Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

INR r (Increment Register)

(r) ← (r) + 1

The content of register r is incremented by one. Note: All condition flags **except CY** are affected.

0	0	D	D	D	1	0	0

Cycles: 1
States: 5
Addressing: register
Flags: Z,S,P,AC

INR M (Increment memory)

((H) (L)) ← ((H) (L)) + 1

The content of the memory location whose address is contained in the H and L registers is incremented by one. Note: All condition flags **except CY** are affected.

0	0	1	1	0	1	0	0

Cycles: 3
States: 10
Addressing: reg. indirect
Flags: Z,S,P,AC

DCR r (Decrement Register)

(r) ← (r) − 1

The content of register r is decremented by one. Note: All condition flags **except CY** are affected.

0	0	D	D	D	1	0	1
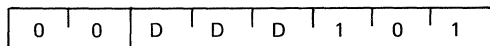
Cycles: 1
States: 5
Addressing: register
Flags: Z,S,P,AC

DCR M   (Decrement memory)

$((H) (L)) \leftarrow ((H) (L)) - 1$

The content of the memory location whose address is contained in the H and L registers is decremented by one. Note: All condition flags **except CY** are affected.

0	0	1	1	0	1	0	1
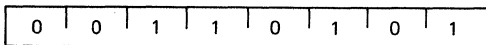
Cycles: 3
States: 10
Addressing: reg. indirect
Flags: Z,S,P,AC

INX rp   (Increment register pair)

$(rh) (rl) \leftarrow (rh) (rl) + 1$

The content of the register pair rp is incremented by one. Note: **No condition flags are affected.**

0	0	R	P	0	0	1	1
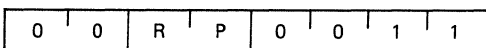
Cycles: 1
States: 5
Addressing: register
Flags: none

DCX rp   (Decrement register pair)

$(rh) (rl) \leftarrow (rh) (rl) - 1$

The content of the register pair rp is decremented by one. Note: **No condition flags are affected.**

0	0	R	P	1	0	1	1
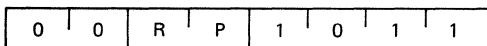
Cycles: 1
States: 5
Addressing: register
Flags: none

DAD rp   (Add register pair to H and L)

$(H) (L) \leftarrow (H) (L) + (rh) (rl)$

The content of the register pair rp is added to the content of the register pair H and L. The result is placed in the register pair H and L. Note: **Only the CY flag is affected.** It is set if there is a carry out of the double precision add; otherwise it is reset.

0	0	R	P	1	0	0	1
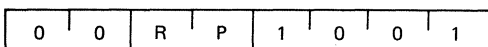
Cycles: 3
States: 10
Addressing: register
Flags: CY

DAA   (Decimal Adjust Accumulator)

The eight-bit number in the accumulator is adjusted to form two four-bit Binary-Coded-Decimal digits by the following process:

1. If the value of the least significant 4 bits of the accumulator is greater than 9 **or** if the AC flag is set, 6 is added to the accumulator.

2. If the value of the most significant 4 bits of the accumulator is now greater than 9, **or** if the CY flag is set, 6 is added to the most significant 4 bits of the accumulator.

NOTE: All flags are affected.

0	0	1	0	0	1	1	1
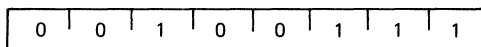
Cycles: 1
States: 4
Flags: Z,S,P,CY,AC

Logical Group:

This group of instructions performs logical (Boolean) operations on data in registers and memory and on condition flags.

Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Auxiliary Carry, and Carry flags according to the standard rules.

ANA r   (AND Register)

$(A) \leftarrow (A) \wedge (r)$

The content of register r is logically anded with the content of the accumulator. The result is placed in the accumulator. **The CY flag is cleared.**

| 1	0	1	0	0	S	S	S
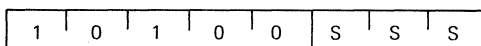
Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

ANA M   (AND memory)

$(A) \leftarrow (A) \wedge ((H) (L))$

The contents of the memory location whose address is contained in the H and L registers is logically anded with the content of the accumulator. The result is placed in the accumulator. **The CY flag is cleared.**

1	0	1	0	0	1	1	0
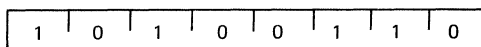
Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

ANI data   (AND immediate)

(A) ← (A) ∧ (byte 2)

The content of the second byte of the instruction is logically anded with the contents of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**

1	1	1	0	0	1	1	0
data							
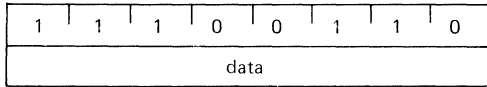
        Cycles: 2
        States: 7
    Addressing: immediate
        Flags: Z,S,P,CY,AC

XRA r   (Exclusive OR Register)

(A) ← (A) ∀ (r)

The content of register r is exclusive-or'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**

1	0	1	0	1	S	S	S
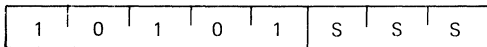
        Cycles: 1
        States: 4
    Addressing: register
        Flags: Z,S,P,CY,AC

XRA M   (Exclusive OR Memory)

(A) ← (A) ∀ ((H) (L))

The content of the memory location whose address is contained in the H and L registers is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**

1	0	1	0	1	1	1	0
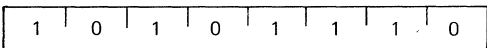
        Cycles: 2
        States: 7
    Addressing: reg. indirect
        Flags: Z,S,P,CY,AC

XRI data   (Exclusive OR immediate)

(A) ← (A) ∀ (byte 2)

The content of the second byte of the instruction is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**

1	1	1	0	1	1	1	0
data							
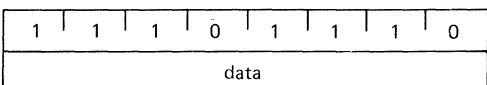
        Cycles: 2
        States: 7
    Addressing: immediate
        Flags: Z,S,P,CY,AC

ORA r   (OR Register)

(A) ← (A) V (r)

The content of register r is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**

1	0	1	1	0	S	S	S
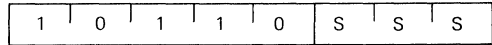
        Cycles: 1
        States: 4
    Addressing: register
        Flags: Z,S,P,CY,AC

ORA M   (OR memory)

(A) ← (A) V ((H) (L))

The content of the memory location whose address is contained in the H and L registers is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**

1	0	1	1	0	1	1	0
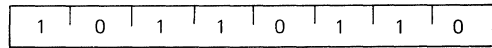
        Cycles: 2
        States: 7
    Addressing: reg. indirect
        Flags: Z,S,P,CY,AC

ORI data   (OR Immediate)

(A) ← (A) V (byte 2)

The content of the second byte of the instruction is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**

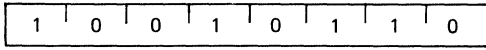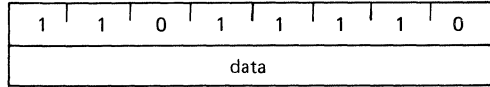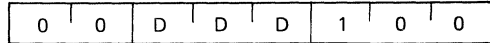| 1	1	1	1	0	1	1	0
data							
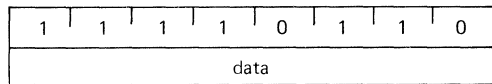
        Cycles: 2
        States: 7
    Addressing: immediate
        Flags: Z,S,P,CY,AC

CMP r   (Compare Register)

(A) − (r)

The content of register r is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. **The Z flag is set to 1 if (A) = (r). The CY flag is set to 1 if (A) < (r).**

1	0	1	1	1	S	S	S
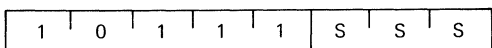
        Cycles: 1
        States: 4
    Addressing: register
        Flags: Z,S,P,CY,AC

CMP M   (Compare memory)

(A) − ((H) (L))

The content of the memory location whose address is contained in the H and L registers is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. The Z flag is set to 1 if (A) = ((H) (L)). The CY flag is set to 1 if (A) $<$ ((H) (L)).

1	0	1	1	1	1	1	0
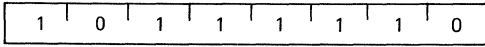
Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

CPI data   (Compare immediate)

(A) − (byte 2)

The content of the second byte of the instruction is subtracted from the accumulator. The condition flags are set by the result of the subtraction. The Z flag is set to 1 if (A) = (byte 2). The CY flag is set to 1 if (A) $<$ (byte 2).

1	1	1	1	1	1	1	0
data							
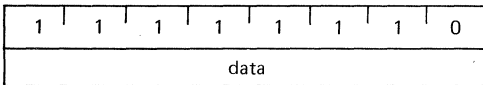
Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

RLC   (Rotate left)

$(A_{n+1}) \leftarrow (A_n)$; $(A_0) \leftarrow (A_7)$
$(CY) \leftarrow (A_7)$

The content of the accumulator is rotated left one position. The low order bit and the CY flag are both set to the value shifted out of the high order bit position. **Only the CY flag is affected**.

0	0	0	0	0	1	1	1
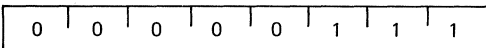
Cycles: 1
States: 4
Flags: CY

RRC   (Rotate right)

$(A_n) \leftarrow (A_{n+1})$; $(A_7) \leftarrow (A_0)$
$(CY) \leftarrow (A_0)$

The content of the accumulator is rotated right one position. The high order bit and the CY flag are both set to the value shifted out of the low order bit position. **Only the CY flag is affected**.

0	0	0	0	1	1	1	1
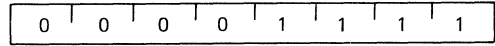
Cycles: 1
States: 4
Flags: CY

RAL   (Rotate left through carry)

$(A_{n+1}) \leftarrow (A_n)$; $(CY) \leftarrow (A_7)$
$(A_0) \leftarrow (CY)$

The content of the accumulator is rotated left one position through the CY flag. The low order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the high order bit. **Only the CY flag is affected.**

0	0	0	1	0	1	1	1
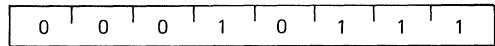
Cycles: 1
States: 4
Flags: CY

RAR   (Rotate right through carry)

$(A_n) \leftarrow (A_{n+1})$; $(CY) \leftarrow (A_0)$
$(A_7) \leftarrow (CY)$

The content of the accumulator is rotated right one position through the CY flag. The high order bit is set to the CY flag and the CY flag is set to the value shifted out of the low order bit. **Only the CY flag is affected.**

0	0	0	1	1	1	1	1
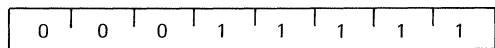
Cycles: 1
States: 4
Flags: CY

CMA   (Complement accumulator)

(A) $\leftarrow$ $\overline{(A)}$

The contents of the accumulator are complemented (zero bits become 1, one bits become 0). **No flags are affected.**

0	0	1	0	1	1	1	1
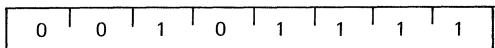
Cycles: 1
States: 4
Flags: none

CMC (Complement carry)

(CY) ← $(\overline{CY})$

The CY flag is complemented. **No other flags are affected.**

0	0	1	1	1	1	1	1
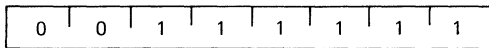
Cycles: 1
States: 4
Flags: CY

STC (Set carry)

(CY) ← 1

The CY flag is set to 1. **No other flags are affected.**

0	0	1	1	0	1	1	1
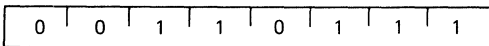
Cycles: 1
States: 4
Flags: CY

Branch Group:

This group of instructions alter normal sequential program flow.

Condition flags are not affected by any instruction in this group.

The two types of branch instructions are unconditional and conditional. Unconditional transfers simply perform the specified operation on register PC (the program counter). Conditional transfers examine the status of one of the four processor flags to determine if the specified branch is to be executed. The conditions that may be specified are as follows:

CONDITION		CCC
NZ	— not zero (Z = 0)	000
Z	— zero (Z = 1)	001
NC	— no carry (CY = 0)	010
C	— carry (CY = 1)	011
PO	— parity odd (P = 0)	100
PE	— parity even (P = 1)	101
P	— plus (S = 0)	110
M	— minus (S = 1)	111

JMP addr (Jump)

(PC) ← (byte 3) (byte 2)

Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.

1	1	0	0	0	0	1	1
low-order addr							
high-order addr							
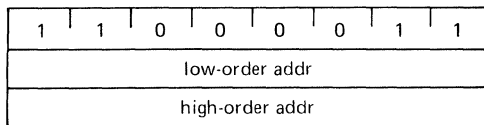
Cycles: 3
States: 10
Addressing: immediate
Flags: none

Jcondition addr (Conditional jump)

If (CCC),

(PC) ← (byte 3) (byte 2)

If the specified condition is true, control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction; otherwise, control continues sequentially.

1	1	C	C	C	0	1	0
low-order addr							
high-order addr							
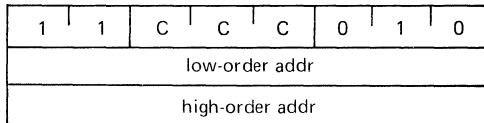
Cycles: 3
States: 10
Addressing: immediate
Flags: none

CALL addr (Call)

((SP) − 1) ← (PCH)

((SP) − 2) ← (PCL)

(SP) ← (SP) − 2

(PC) ← (byte 3) (byte 2)

The high-order eight bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order eight bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.

1	1	0	0	1	1	0	1
low-order addr							
high-order addr							
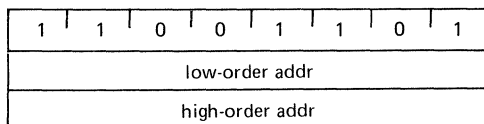
Cycles: 5
States: 17
Addressing: immediate/reg. indirect
Flags: none

Ccondition addr   (Condition call)

    If (CCC),

        ((SP) − 1) ◄— (PCH)

        ((SP) − 2) ◄— (PCL)

        (SP) ◄— (SP) − 2

        (PC) ◄— (byte 3) (byte 2)

If the specified condition is true, the actions specified in the CALL instruction (see above) are performed; otherwise, control continues sequentially.

1	1	C	C	C	1	0	0
low-order addr								
high-order addr								
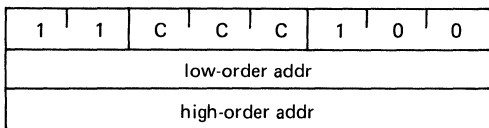
        Cycles: 3/5
        States: 11/17
    Addressing: immediate/reg. indirect
        Flags: none

RET   (Return)

    (PCL) ◄— ((SP));

    (PCH) ◄— ((SP) + 1);

    (SP) ◄— (SP) + 2;

The content of the memory location whose address is specified in register SP is moved to the low-order eight bits of register PC. The content of the memory location whose address is one more than the content of register SP is moved to the high-order eight bits of register PC. The content of register SP is incremented by 2.

1	1	0	0	1	0	0	1
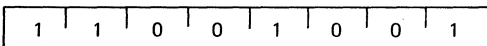
        Cycles: 3
        States: 10
    Addressing: reg. indirect
        Flags: none

Rcondition   (Conditional return)

    If (CCC),

        (PCL) ◄— ((SP))

        (PCH) ◄— ((SP) + 1)

        (SP) ◄— (SP) + 2

If the specified condition is true, the actions specified in the RET instruction (see above) are performed; otherwise, control continues sequentially.

1	1	C	C	C	0	0	0
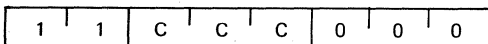
        Cycles: 1/3
        States: 5/11
    Addressing: reg. indirect
        Flags: none

RST n   (Restart)

    ((SP) − 1) ◄— (PCH)

    ((SP) − 2) ◄— (PCL)

    (SP) ◄— (SP) − 2

    (PC) ◄— 8 * (NNN)

The high-order eight bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order eight bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two. Control is transferred to the instruction whose address is eight times the content of NNN.

1	1	N	N	N	1	1	1

        Cycles: 3
        States: 11
    Addressing: reg. indirect
        Flags: none

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	N	N	N	0	0	0
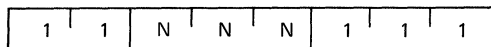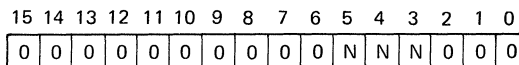
Program Counter After Restart

PCHL   (Jump H and L indirect — move H and L to PC

    (PCH) ◄— (H)

    (PCL) ◄— (L)

The content of register H is moved to the high-order eight bits of register PC. The content of register L is moved to the low-order eight bits of register PC.

1	1	1	0	1	0	0	1
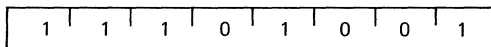
        Cycles: 1
        States: 5
    Addressing: register
        Flags: none

Stack, I/O, and Machine Control Group:

This group of instructions performs I/O, manipulates the Stack, and alters internal control flags.

Unless otherwise specified, **condition flags are not affected by any instructions in this group.**

FLAG WORD

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z	0	AC	0	P	1	CY

PUSH rp (Push)

$((SP) - 1) \leftarrow (rh)$
$((SP) - 2) \leftarrow (rl)$
$(SP) \leftarrow (SP) - 2$

The content of the high-order register of register pair rp is moved to the memory location whose address is one less than the content of register SP. The content of the low-order register of register pair rp is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. **Note: Register pair rp = SP may not be specified.**

1	1	R	P	0	1	0	1

Cycles: 3
States: 11
Addressing: reg. indirect
Flags: none

PUSH PSW (Push processor status word)

$((SP) - 1) \leftarrow (A)$
$((SP) - 2)_0 \leftarrow (CY)$, $((SP) - 2)_1 \leftarrow 1$
$((SP) - 2)_2 \leftarrow (P)$, $((SP) - 2)_3 \leftarrow 0$
$((SP) - 2)_4 \leftarrow (AC)$, $((SP) - 2)_5 \leftarrow 0$
$((SP) - 2)_6 \leftarrow (Z)$, $((SP) - 2)_7 \leftarrow (S)$
$(SP) \leftarrow (SP) - 2$

The content of register A is moved to the memory location whose address is one less than register SP. The contents of the condition flags are assembled into a processor status word and the word is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two.

1	1	1	1	0	1	0	1

Cycles: 3
States: 11
Addressing: reg. indirect
Flags: none

POP rp (Pop)

$(rl) \leftarrow ((SP))$
$(rh) \leftarrow ((SP) + 1)$
$(SP) \leftarrow (SP) + 2$

The content of the memory location, whose address is specified by the content of register SP, is moved to the low-order register of register pair rp. The content of the memory location, whose address is one more than the content of register SP, is moved to the high-order register of register pair rp. The content of register SP is incremented by 2. **Note: Register pair rp = SP may not be specified.**

1	1	R	P	0	0	0	1

Cycles: 3
States: 10
Addressing: reg. indirect
Flags: none

POP PSW (Pop processor status word)

$(CY) \leftarrow ((SP))_0$
$(P) \leftarrow ((SP))_2$
$(AC) \leftarrow ((SP))_4$
$(Z) \leftarrow ((SP))_6$
$(S) \leftarrow ((SP))_7$
$(A) \leftarrow ((SP) + 1)$
$(SP) \leftarrow (SP) + 2$

The content of the memory location whose address is specified by the content of register SP is used to restore the condition flags. The content of the memory location whose address is one more than the content of register SP is moved to register A. The content of register SP is incremented by 2.

1	1	1	1	0	0	0	1

Cycles: 3
States: 10
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

XTHL   (Exchange stack top with H and L)

(L) ←→ ((SP))

(H) ←→ ((SP) + 1)

The content of the L register is exchanged with the content of the memory location whose address is specified by the content of register SP. The content of the H register is exchanged with the content of the memory location whose address is one more than the content of register SP.

1	1	1	0	0	0	1	1
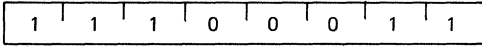
Cycles: 5
States: 18
Addressing: reg. indirect
Flags: none

SPHL   (Move HL to SP)

(SP) ← (H) (L)

The contents of registers H and L (16 bits) are moved to register SP.

1	1	1	1	1	0	0	1
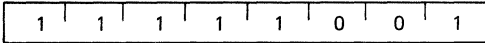
Cycles: 1
States: 5
Addressing: register
Flags: none

IN port   (Input)

(A) ← (data)

The data placed on the eight bit bi-directional data bus by the specified port is moved to register A.

1	1	0	1	1	0	1	1
port							
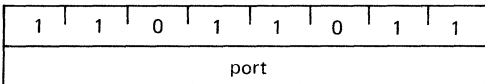
Cycles: 3
States: 10
Addressing: direct
Flags: none

OUT port   (Output)

(data) ← (A)

The content of register A is placed on the eight bit bi-directional data bus for transmission to the specified port.

1	1	0	1	0	0	1	1
port							
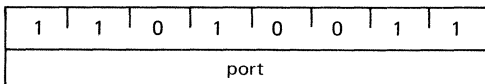
Cycles: 3
States: 10
Addressing: direct
Flags: none

EI   (Enable interrupts)

The interrupt system is enabled **following the execution of the next instruction.**

1	1	1	1	1	0	1	1
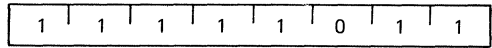
Cycles: 1
States: 4
Flags: none

DI   (Disable interrupts)

The interrupt system is disabled **immediately following the execution of the DI instruction.**

1	1	1	1	0	0	1	1
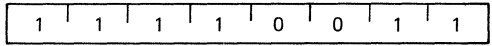
Cycles: 1
States: 4
Flags: none

HLT   (Halt)

The processor is stopped. The registers and flags are unaffected.

0	1	1	1	0	1	1	0
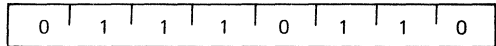
Cycles: 1
States: 7
Flags: none

NOP   (No op)

No operation is performed. The registers and flags are unaffected.

0	0	0	0	0	0	0	0
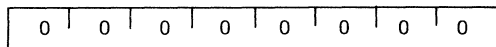
Cycles: 1
States: 4
Flags: none

8080 INSTRUCTION SET

Summary of Processor Instructions

Mnemonic	Description	D7	D6	D5	D4	D3	D2	D1	D0	Clock[2] Cycles
MOVE, LOAD, AND STORE										
MOVr1,r2	Move register to register	0	1	D	D	D	S	S	S	5
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10

Mnemonic	Description	D7	D6	D5	D4	D3	D2	D1	D0	Clock[2] Cycles
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	11
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10

NOTES: 1. DDD or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.
2. Two possible cycle times. (6/12) indicate instruction cycles dependent on condition flags.

*All mnemonics copyright
^cIntel Corporation 1977

8080 INSTRUCTION SET

Summary of Processor Instructions (Cont.)

Mnemonic	Description	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	7

NOTES: 1. DDD or SSS: B=000, C=001, D=010, E=011, H=100, L=101, Memory=110, A=111.
2. Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags.

Chapter 5
INTRODUCTION TO MCS-85™
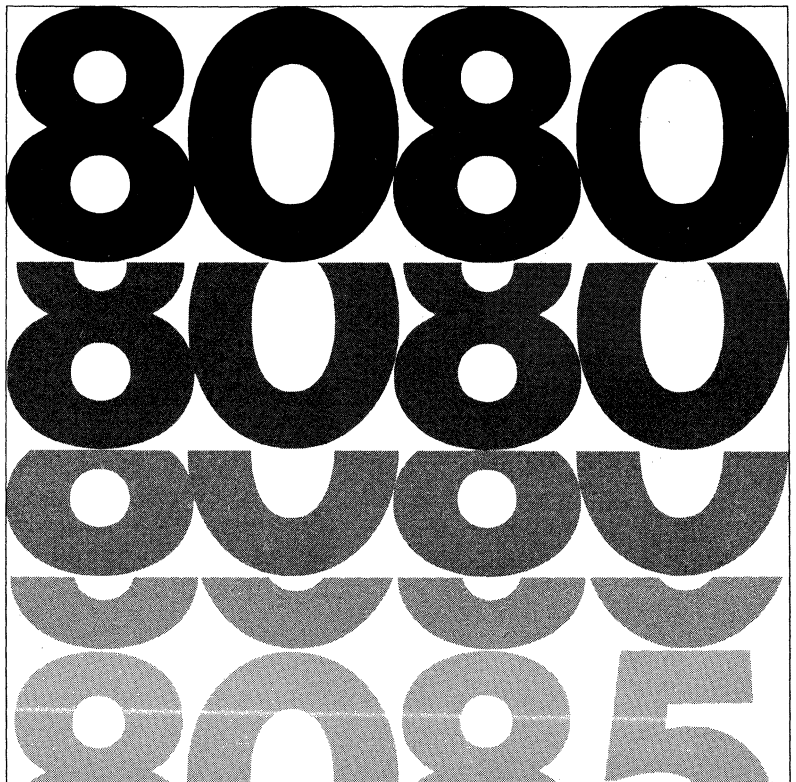
INTRODUCTION TO MCS-85™

EVOLUTION

In December 1971, Intel introduced the first general purpose, 8-bit microprocessor, the 8008. It was implemented in P-channel MOS technology and was packaged in a single 18 pin, dual in-line package (DIP). The 8008 used standard semiconductor ROM and RAM and, for the most part, TTL components for I/O and general interface. It immediately found applications in byte-oriented end products such as terminals and computer peripherals where its instruction execution (20 micro-seconds), general purpose organization and instruction set matched the requirements of these products. Recognizing that hardware was but a small part in the overall system picture, Intel developed both hardware and software tools for the design engineer so that the transition from prototype to production would be as simple and fast as possible. The commitment of providing a total systems approach with the 8008 microcomputer system was actually the basis for the sophisticated, comprehensive development tools that Intel has available today.

THE 8080A MICROPROCESSOR

With the advent of high-production N-channel RAM memories and 40 pin DIP packaging, Intel designed the 8080A microprocessor. It was designed to be software compatible with the 8008 so that the existing users of the 8008 could preserve their investment in software and at the same time provide dramatically increased performance (2 micro-second instruction execution), while reducing the amount of components necessary to implement a system. Additions were made to the basic instruction set to take advantage of this increased performance and large system-type features were included on-chip such as DMA, 16-bit addressing and external stack memory so that the total spectrum of application could be significantly increased. The 8080 was first sampled in December 1973. Since that time it has become the standard of the industry and is accepted as the primary building block for more microcomputer based applications than all other microcomputer systems combined.

A TOTAL SYSTEMS COMMITMENT

The Intel® 8080A Microcomputer System encompasses a total systems commitment to the user to fully support his needs both in developing prototype systems and reliable, high volume production. From complex MOS/LSI peripheral components to resident high level systems language (PL/M) the Intel® 8080 Microcomputer System provides the most comprehensive, effective solution to today's system problems.
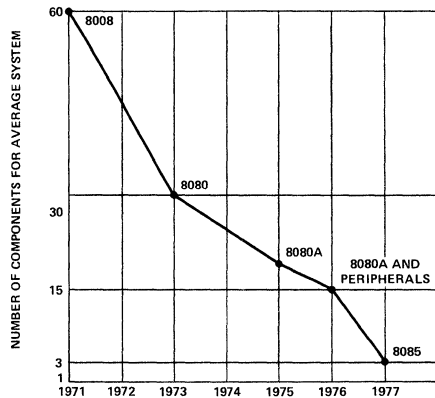
8-BIT SYSTEM COMPONENT COUNT 1971 – 1977
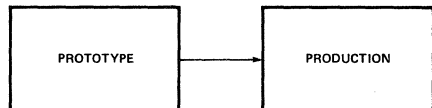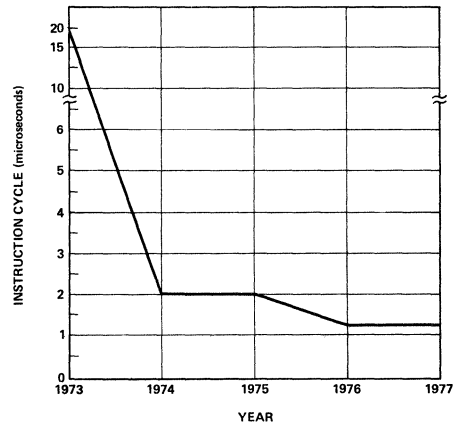
THE MCS-85™ MICROCOMPUTER SYSTEM

The basic philosophy behind the MCS-85 microcomputer system is one of logical, evolutionary advance in technology without the waste of discarding existing investments in hardware and sotware. The MCS-85 provides the existing 8080 user with an increase in performance, a decrease in the component count, a single 5 volt operation and still preserves 100% of his existing software investment. For the new microcomputer user, the MCS-85 represents the refinement of the most popular microcomputer in the industry, the Intel 8080, along with a wealth of supporting software, documentation and peripheral components to speed the cycle from prototype to production. The identical development tools that Intel has produced to support the 8080 microcomputer system can be used for the MCS-85, and additional add-on features are available to optimize system development for MCS-85.

This section of the MCS-85 User's Manual will briefly detail the basic differences between the MCS-85 and MCS-80™ families. It will illustrate both the hardware and software compatibilities and also reveal some of the engineering trade-offs that were met during the design of MCS-85. More detailed discussion of the MCS-85 bus operation and component specifications are available in Sections: 2,3,4, but the information provided in this section, Section 1, will be extremely helpful in understanding the basic concepts and philosophies behind the MCS-85.

It is important for the reader of the MCS-85 User's Manual to have a solid understanding of the 8080 microcomputer system. Most of the terms and procedures that are used in the MCS-85 User's Manual are based on information in the MCS-80™ User's Manual. Please refer to the MCS-80™ User's Manual as required.

8085 CPU	STANDARD RAM - ROM 8212 LATCH (1)	COMBINATION 8155/56 - RAM - I/O 8355 - ROM - I/O	GENERAL PERIPHERALS 825X
8271 FLOPPY DISK	8273 SLDC	8275 CRT	8279 KYBD/DISPLAY
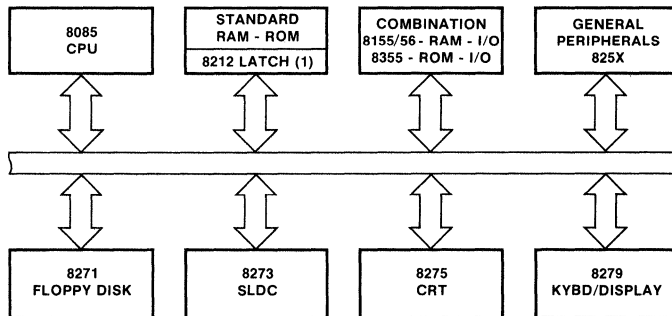
MCS-85™ TOTAL SYSTEM

SYSTEM INTEGRATION

The MCS-85 integrates many of the functions that are auxiliary to an 8080A based system. Functions such as: clock generation, system control and interrupt prioritizing are integrated into on-chip features of the 8085 Central Processor. The 8085 is, of course, the central element in the MCS-85 family. It coordinates all bus transfers and operations and executes the instruction set. The 8085 CPU is designed to be the controlling master of a unique, multiplexed bus system. This bus structure will be discussed in detail later in the manual but basically, the information provided on the data bus is time-multiplexed and contains both data and the lower 8 address bits (A7-A0). The address bus contains the remaining 8-bits (A8-A15). The 8085 CPU generates signals that tell peripheral devices what type of information is on the multiplexed bus (Address/Data) and from that point on the operation is almost identical to the MCS-80™ CPU Group. The multiplexed bus structure was chosen because it had no detrimental effect on system performance, allowed complete compatibility to existing peripheral components, provided improved timing margins and access requirements and freed device pins so that more functions could be integrated on the 8085 and other components of the family.

To enhance the system integration of MCS-85, several special components with combined memory and I/O were designed. These new devices have been designed to directly interface to the multiplexed bus of the 8085. It is interesting to note that the pin locations of the 8085 and the special peripheral components were assigned to minimize PC board area and allow for a smooth, efficient layout. The details on the new peripheral components will be discussed later in the manual.

MCS-80 CPU GROUP
(BASIC FUNCTIONS)

MCS-80™ CPU GROUP (BASIC FUNCTIONS)

MCS-85 CPU/8085
(BASIC FUNCTIONS)

MCS-85™ CPU/8085 (BASIC FUNCTIONS)

DATA/ADDRESS BUS

ADDRESS A_7-A_0

DATA IN OR OUT D_7-D_0
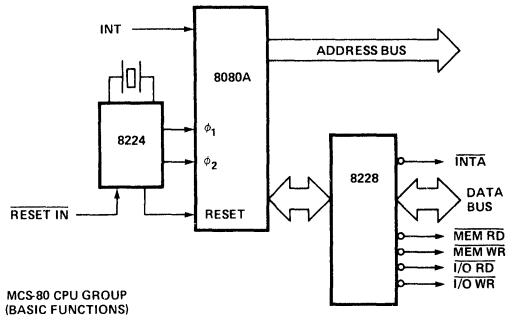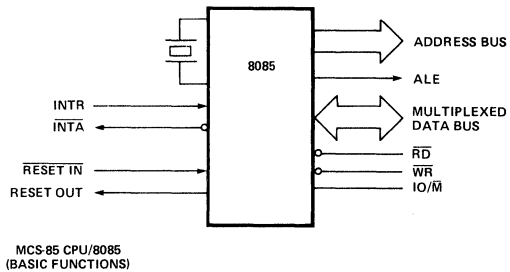
TIME MULTIPLEX DATA BUS
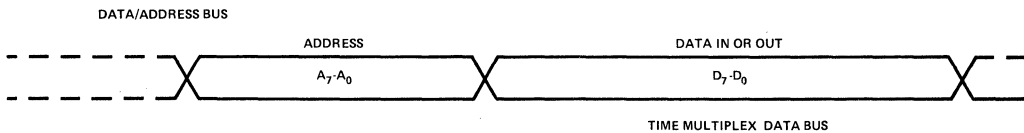
MULTIPLEXED BUS TIMING

SOFTWARE COMPATIBILITY

As with any computer system the cost of software development far outweighs those of hardware. A microcomputer-based system is traditionally a very cost-sensitive application and the development of software is one of the key areas where success or failure of the cost objectives is vital.

```
┌─────────────┐         ┌─────────────┐
│   8080A     │ ──────▶ │    8085     │
│  PROGRAMS   │         │   SYSTEM    │
└─────────────┘         └─────────────┘
```
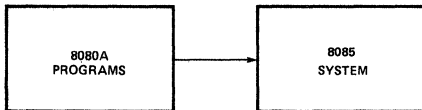
The 8085 CPU is 100% software compatible with the Intel® 8080A CPU. The compatibility is at the object or "machine code" level so that existing programs written for 8080A execution will run on the 8085 as is. This becomes even more evident to the user who has mask programmed ROMs and wishes to update his system without the need for new masks.

PROGRAMMER TRAINING

A cost which is often forgotten is that of programmer training. A new, or modified instruction set, would require programmers to relearn another set of mnemomics and greatly effect the productivity during development. The 100% compatibility of the 8085 CPU assures that no re-training effort will be required.

For the new microcomputer user, the software compatibility between the 8085 and 8080A means that all of the software development tools that are available for the 8080A and all software libraries for 8080A will operate with the new design and thus save immeasurable cost in development and debug.

```
┌────────────────┐      ┌────────────────┐
│     8080A      │      │     8080A      │
│  DEVELOPMENT   │      │    PROGRAM     │
│     TOOLS      │      │   LIBRARIES    │
└────────────────┘      └────────────────┘
         \                    /
          \                  /
           ┌────────────────┐
           │   MCS-85™      │
           │                │
           └────────────────┘
```
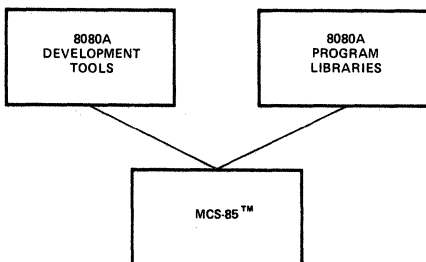
The 8085 CPU does however add two instructions to initialize and maintain hardware features of the 8085. Two of the unused opcodes of the 8080A instruction set were designated for the addition so that 100% compatibility could be maintained.

As mentioned previously, the MCS-85 is designed to be a logical, evolutionary advance that solves problems in the most efficient, cost effective manner available. 100% software compatibility fulfills one of the most important aspects of the overall MCS-85 system philosophy.

HARDWARE COMPATIBILITY

The integration of auxiliary 8080A functions, such as clock generation, system control and interrupt prioritization, dramatically reduces the amount of components necessary for most systems. In addition to integrating some of the MCS-80™ system functions, the MCS-85 operates off a single +5 volt power supply to further simplify hardware development and debug. A close examination of the AC/DC specifications of the MCS-85 systems components shows that each is specified to supply a maximum of 400 micro Amps of source current and a full TTL load of sink current so that a very substantial system can be constructed without the need for extra TTL buffers or drivers. Input and output voltage levels are also specified so that a minimum of 400 microvolts noise margin is provided for reliable, high-performance operation.

PC BOARD CONSIDERATIONS

The 8085 CPU and the 8080A are not pin-compatible due to the reduction in power supplies and the addition of integrated auxiliary features. However the pinouts of the MCS-85 system components were carefully assigned to minimize PC board area and thus yield a smooth, efficient layout. For new designs this incompatibility of pinouts presents no problems and for upgrades of existing designs the reduction of components and board area will far offset the incompatibility.

MCS-85™ SPECIAL PERIPHERAL COMPONENTS

The MCS-85 was designed to minimize the amount of components required for most systems. Intel designed several new peripheral components that combine memory, I/O and timer functions to fulfill this requirement. These new peripheral devices directly interface to the multiplexed MCS-85 bus structure and provide new levels in system integration for today's designer.

*: 8155 = $\overline{CE}$, 8156 = CE
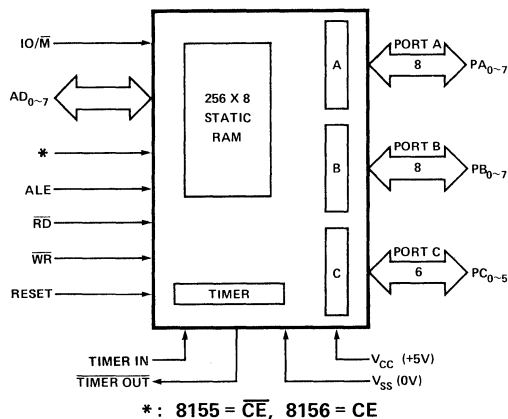
8155/8156 RAM, I/O and Timer

256 bytes RAM
2- 8-bit ports
1- 6-bit port (programmable)
1- 14-bit programmable interval timer
Single +5 volt supply operation
40 pin DIP plastic or cerdip package
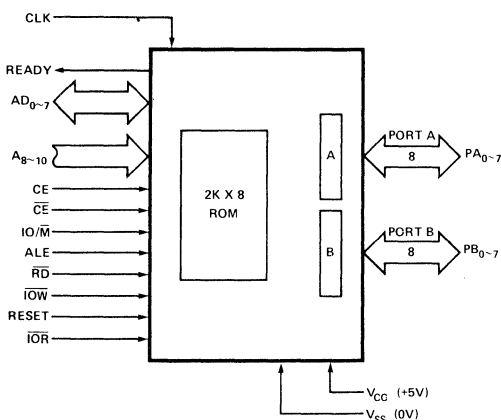
8355 ROM and I/O

2K bytes ROM
2- 8-bit ports (direction programmable)
Single +5 volt supply operation
40 pin DIP plastic or cerdip package
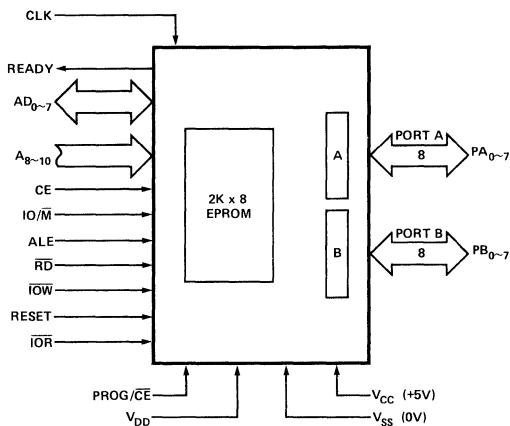
8755 EPROM and I/O

Socket compatible with 8355
2K bytes EPROM
2- 8-bit ports (direction programmable)
Single +5 volt supply read operation
U.V. Erasable
40 pin DIP package

8755/8355

One of the most important advances made with the MCS-85 is the socket-compatibility of the 8355 and 8755 components. This allows the systems designer to develop and debug in erasable PROM and then, when satisfied, switch over to mask-programmed ROM 8355 with no performance degradation or board relayout. It also allows quick prototype production for market impact without going to a "kluge" solution.
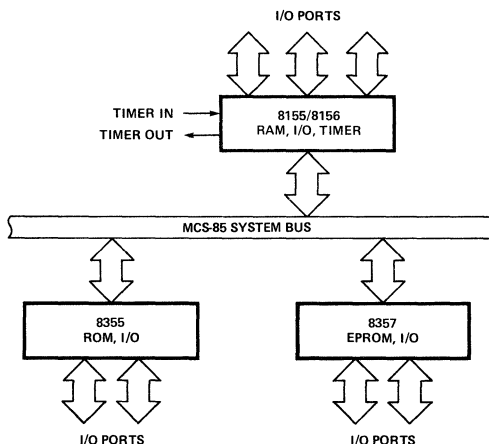
SYSTEM EXPANSION

Each of these peripheral components has features that allow a small to medium system to be constructed without the addition of buffers and decoders to further reduce the component count.

MCS-85™ BASIC SYSTEM
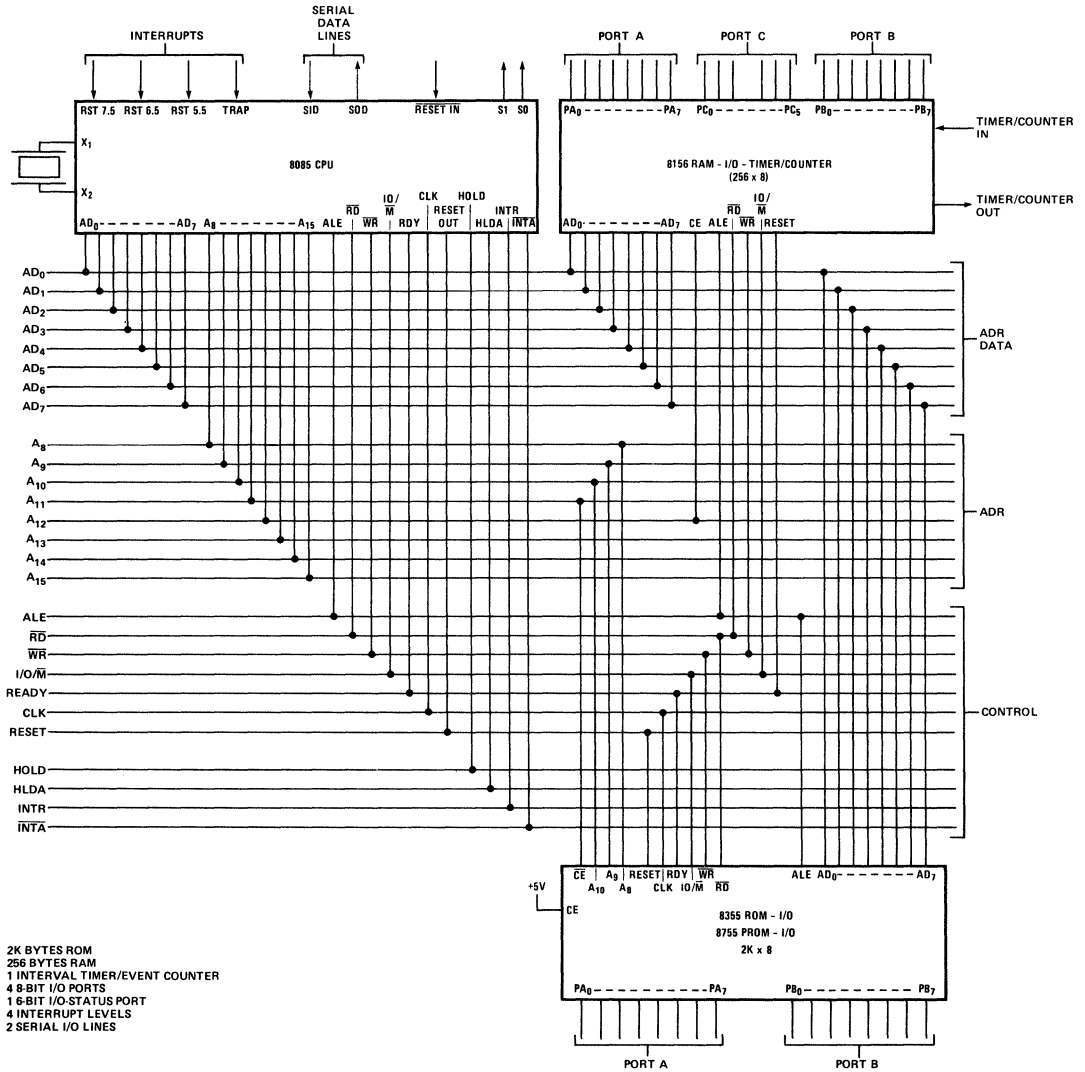
INTERFACING TO MCS-80™ PERIPHERAL COMPONENTS

The MCS-80 has a wide range of peripheral components that solve system problems and provide the designer with a great deal of flexibility in his I/O, Interrupt and DMA structures. The MCS-85 is directly compatible with these peripherals, and, with the exception of the 8257 DMA controller, needs no additional circuitry for their interface. The 8257 DMA controller uses an 8212 latch and some gating to support the multiplexed bus of MCS-85.

MULTIPLEX BUS

To understand the exact interface between the MCS-85 and the MCS-80™ peripheral components, recall that the 8080A CPU issues the address of the I/O device on its 16-bit address bus. The I/O address appears on both the upper and lower 8-bits of the address bus. The 8085 CPU utilizes a multiplexed bus structure where the address bus contains only the upper 8-bits of information. The data bus contains both data and the lower 8-bits of information of the address. Since the read/write control signals are only issued when there is data on the bus and the address bus contains the I/O device address, then all of the MCS-80 peripherals will interface directly with no hardware or software problems. In fact, due to the manner in which the 8085 control signals were implemented, memory-mapped I/O becomes simpler to use than with MCS-80 and combinations of memory-mapped and standard I/O techniques will provide the designer with new flexibilities to maximize system efficiency.
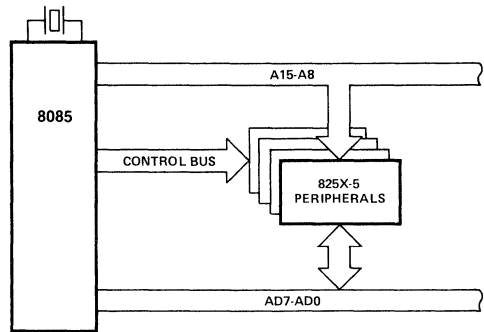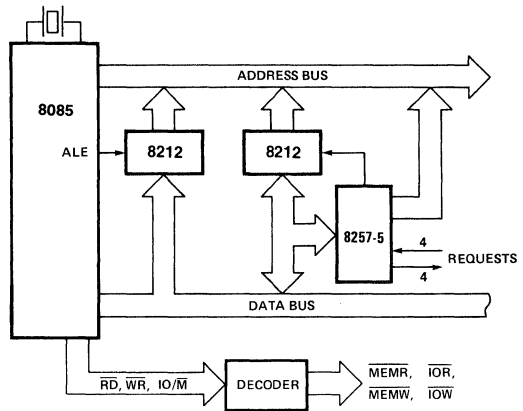
MCS-80™ PERIPHERALS

To interface 825X peripherals to 8085 bus at 3MHz, the user must use a set of MCS-80 peripherals, called, **"825X-5"**. It includes 8251A, 8253-5, 8255A-5, 8257-5 and 8259-5 as shown below:

8251A   Programmable Communications
            Interface
8253-5   Programmable Interval Timer
8255A-5 Programmable Peripheral Interface
8257-5   Programmable DMA Controller
8259-5   Programmable Interrupt Controller

This compatibility also assures the designer that all new peripheral components from Intel will interface to the MCS-85 bus structure to further expand the application spectrum of MCS-85.
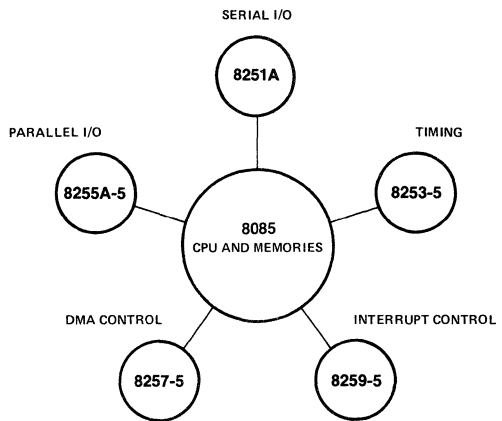
INTERFACING TO STANDARD MEMORY

The MCS-85 was designed to support the full range of system configurations from small 3 chip applications to large memory and I/O applications. The 8085 CPU issues advanced timing signals (S0 & S1) so that, in the case of large systems, these signals could be used to simplify bus arbitration logic and dynamic RAM refresh circuitry.

The multiplexed bus structure of the MCS-85 provides direct interface to MCS-80™ peripheral components, but in large, memory intensive systems, standard ROM and RAM memory will be present due to the economies of such devices when used in large quantities per system. In most memory intensive systems I/O requirements do not generally track memory space. Thus standard memory is a more cost effective solution for these applications than the special 8155, 8355 devices.
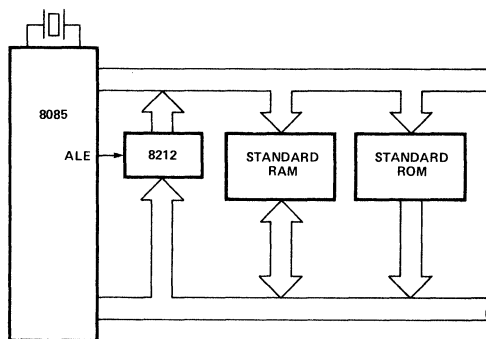
DEMULTIPLEXING THE BUS

In order to interface standard memory components such as Intel® 8102A, 8101A, 8111A, 8316A, 8308, 2104 and 2116 the MCS-85 bus must be "de-multiplexed". This is accomplished by connecting an Intel® 8212 latch to the data bus and strobing the latch with the ALE signal from the 8085 CPU. The ALE signal is issued to indicate that the information on the data bus is actually the lower 8-bits of the address bus, and the 8212 simply latches this information so that a full 16-bit address is now available to interface standard memory components.

USE OF 8212

The additional component may at first seem wasteful but large, memory intensive systems are usually multi-card implementations and require some form of TTL buffering to provide necessary current and voltage levels. Therefore, the additional 8212 will probably be required for the buffering task and the de-multiplexing of the data bus is incidental.

SYSTEM PERFORMANCE

The true benchmark of any microcomputer-based system is the amount of tasks that can be assigned to the software execution and still meet the overall product performance requirements. Speed of CPU instruction execution has been the common approach to system through-put problems but this puts a greater strain on the memory access requirement and bus operation than is usually practical for most applications. A much more desirable method would be to distribute the task-load to peripheral devices and free the systems software to simply initializing and maintaining these devices on a regular basis.

DISTRIBUTED PROCESSING

The concept of distributed task processing is not new to the computer designer, but until recently little if any task distribution was available to the microcomputer user. The MCS-85 is fully supported by Intel's MCS-80™ peripheral components. All are programmable and each can relieve the systems software of many of the bookkeeping I/O and timing tasks common to any system.

INSTRUCTION CYCLE/ACCESS

The basic instruction cycle of the 8085 is 1.3 microseconds. It is the same speed as the 8080A-1 and a closer look at the MCS-85 bus operation shows that the access requirement for this speed is only 450 nanoseconds. The MCS-80™ access requirements for this speed would be under 300 nanoseconds to illustrate the efficiency and improved timing margins of the MCS-85 bus structure.

THROUGHPUT/COST

When a total system through-put analysis is taken, the MCS-85 with its programmable peripheral components will yield the most cost-effective, reliable and producible system available.

FOR MORE INFORMATION

Data Sheets on the 8085, 8155/56, 8355, and 8755 are provided later in this manual.

More detailed information on MCS-85 is available in the Intel® MCS-85 User's Manual.
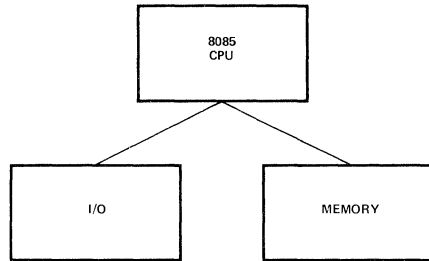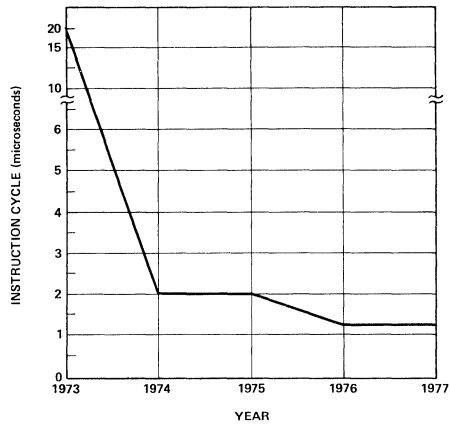
Chapter 6

MICROCOMPUTER SYSTEM
COMPONENT DATA SHEETS

CPU Group

CPU Group

intel®

8080A

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

- **TTL Drive Capability**

- **2 μs Instruction Cycle**

- **Powerful Problem Solving Instruction Set**

- **Six General Purpose Registers and an Accumulator**

- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**

- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**

- **Decimal, Binary and Double Precision Arithmetic**

- **Ability to Provide Priority Vectored Interrupts**

- **512 Directly Addressed I/O Ports**

The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/ retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.

8080A CPU FUNCTIONAL BLOCK DIAGRAM

8080A FUNCTIONAL PIN DEFINITION

The following describes the function of all of the 8080A I/O pins. Several of the descriptions refer to internal timing periods.

A_{15}-A_0 (output three-state)

ADDRESS BUS; the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A_0 is the least significant address bit.

D_7-D_0 (input/output three-state)

DATA BUS; the data bus provides bi-directional communication between the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the 8080A outputs a status word on the data bus that describes the current machine cycle. D_0 is the least significant bit.

SYNC (output)

SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output)

DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080A data bus from memory or I/O.

READY (input)

READY; the READY signal indicates to the 8080A that valid memory or input data is available on the 8080A data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080A does not receive a READY input, the 8080A will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU.

WAIT (output)

WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.

$\overline{WR}$ (output)

WRITE; the $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active low ($\overline{WR}$ = 0).

HOLD (input)

HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080A address and data bus as soon as the 8080A has completed its use of these buses for the current machine cycle. It is recognized under the following conditions:
- the CPU is in the HALT state.
- the CPU is in the T2 or TW state and the READY signal is active.
As a result of entering the HOLD state the CPU ADDRESS BUS (A_{15}-A_0) and DATA BUS (D_7-D_0) will be in their high impedance state. The CPU acknowledges its state with the HOLD AC-KNOWLEDGE (HLDA) pin.

HLDA (output)

HOLD ACKNOWLEDGE; the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus
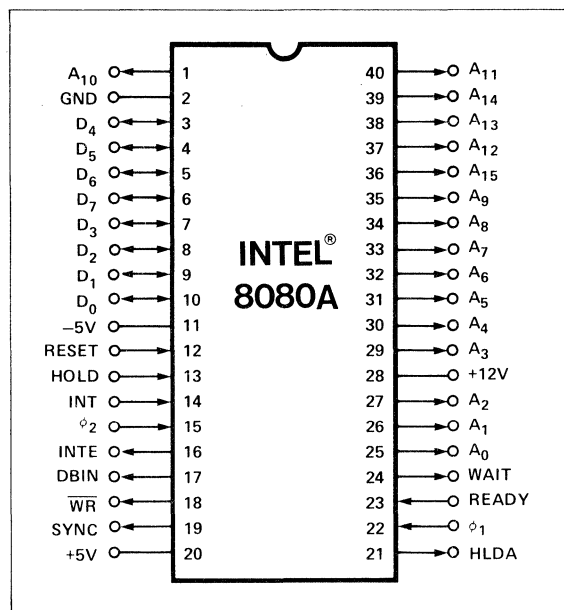
Pin Configuration

will go to the high impedance state. The HLDA signal begins at:
- T3 for READ memory or input.
- The Clock Period following T3 for WRITE memory or OUTPUT operation.

In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.

INTE (output)

INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.

INT (input)

INTERRUPT REQUEST; the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input) [1]

RESET; while the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

V_{SS}	Ground Reference.
V_{DD}	+12 ± 5% Volts.
V_{CC}	+5 ± 5% Volts.
V_{BB}	-5 ±5% Volts (substrate bias).
ϕ_1, ϕ_2	2 externally supplied clock phases. (non TTL compatible)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . 0°C to +70°C
Storage Temperature . . . . -65°C to +150°C
All Input or Output Voltages
   With Respect to V_{BB} . . . . -0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB} -0.3V to +20V
Power Dissipation 1.5W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = 0°C$ to 70°C, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IHC}	Clock Input High Voltage	9.0		$V_{DD}+1$	V	
V_{IL}	Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IH}	Input High Voltage	3.3		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = −150μA.
$I_{DD(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	
$I_{CC(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	Operation
$I_{BB(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	T_{CY} = .48 μsec
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			−100 −2.0	μA mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}+0.8V$ $V_{SS}+0.8V \leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 −100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS} + 0.45V$

CAPACITANCE

$T_A = 25°C$ $V_{CC} = V_{DD} = V_{SS} = 0V$, $V_{BB} = -5V$

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = −0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED. [3]

DATA BUS CHARACTERISTIC DURING DBIN

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY} [3]	Clock Period	0.48	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi2}$	ϕ_2 Pulse Width	220		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	70		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		nsec	
t_{DA} [2]	Address Output Delay From ϕ_2		200	nsec	$C_L = 100$pf
t_{DD} [2]	Data Output Delay From ϕ_2		220	nsec	
t_{DC} [2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		120	nsec	$C_L = 50$pf
t_{DF} [2]	DBIN Delay From ϕ_2	25	140	nsec	
t_{DI} [1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		nsec	

TIMING WAVEFORMS [14] (Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)

A.C. CHARACTERISTICS (Continued)

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = –5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	150		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	120		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	140		nsec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	120		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	C_L = 100pf: Address, Data C_L = 50pf: $\overline{WR}$, HLDA, DBIN
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	–20		nsec	

NOTES:
1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.

3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 480$ns.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE

Δ CAPACITANCE (pf)
($C_{ACTUAL} - C_{SPEC}$)

4. The following are relevant when interfacing the 8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2 t_{CY} - t_{D3} - t_{r\phi2} - 140$nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$nsec.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns
10. Data in must be stable for this period during DBIN ·T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the 8080A. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the 8080A instruction set.

The following special instruction group completes the 8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

Data in the 8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

$$\boxed{D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0}$$
DATA WORD
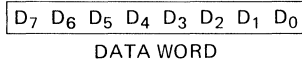
The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

$\boxed{D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0}$ OP CODE

Two Byte Instructions

$\boxed{D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0}$ OP CODE
$\boxed{D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0}$ OPERAND

Three Byte Instructions

$\boxed{D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0}$ OP CODE
$\boxed{D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0}$ LOW ADDRESS OR OPERAND 1
$\boxed{D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0}$ HIGH ADDRESS OR OPERAND 2
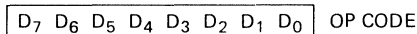
TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions
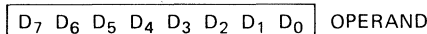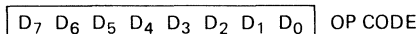
Immediate mode or I/O instructions
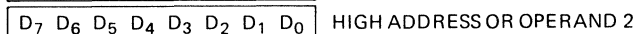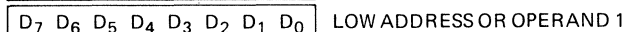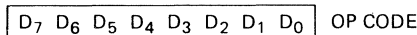
Jump, call or direct load and store instructions

For the 8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.
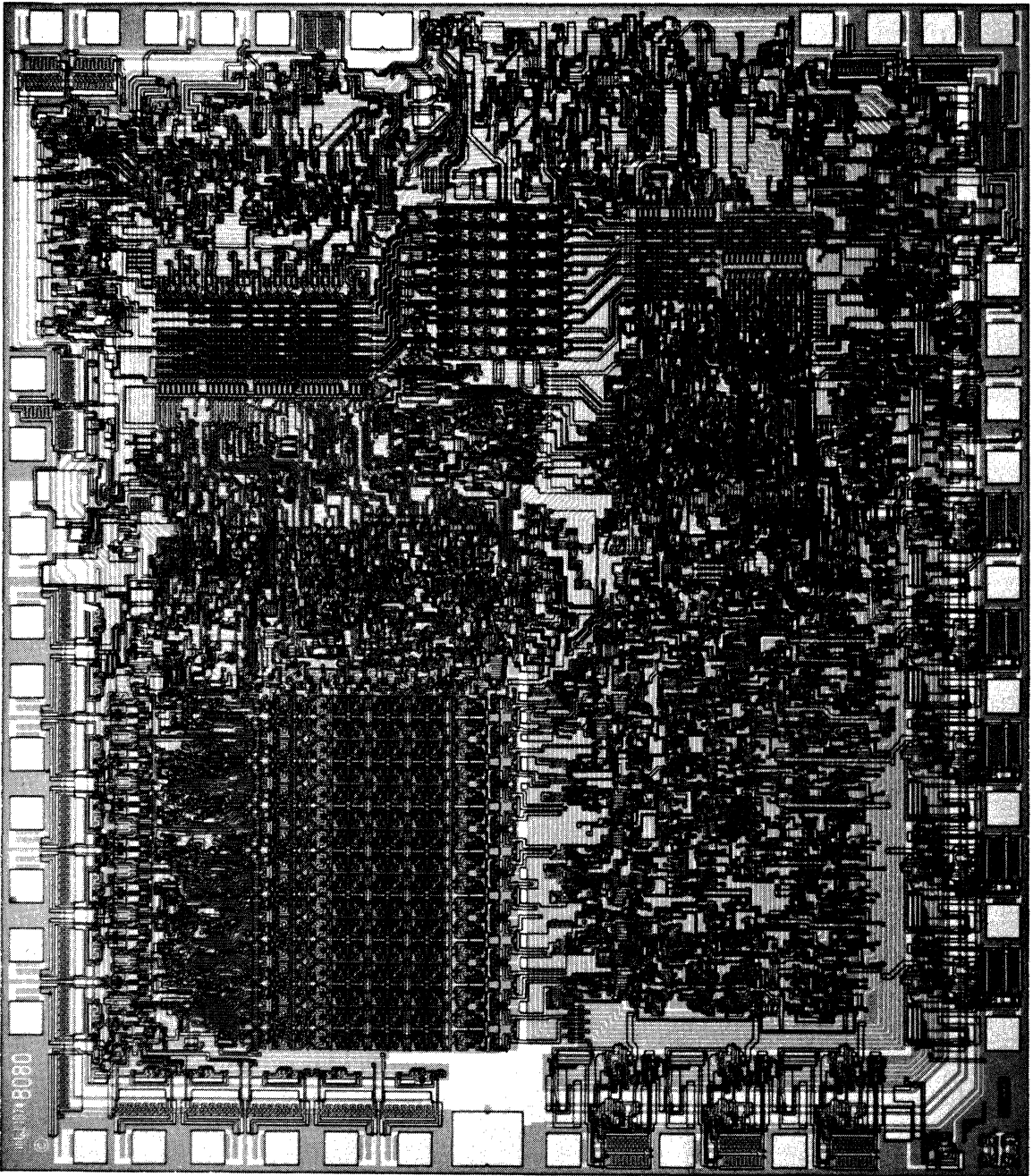
intel®

8080A-1
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

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- **1.3 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**

- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
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The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

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8080A CPU FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . 0°C to +70°C
Storage Temperature . . . . −65°C to +150°C
All Input or Output Voltages
    With Respect to V_{BB} . . . . −0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB} −0.3V to +20V
Power Dissipation 1.5W

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IHC}	Clock Input High Voltage	9.0		$V_{DD}+1$	V	
V_{IL}	Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IH}	Input High Voltage	3.3		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150µA.
$I_{DD(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	
$I_{CC(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	Operation
$I_{BB(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	T_{CY} = .32µsec
I_{IL}	Input Leakage			±10	µA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	µA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			−100 −2.0	µA mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}+0.8V$ $V_{SS}+0.8V \leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 −100	µA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS} + 0.45V$

CAPACITANCE

$T_A = 25°C$ $V_{CC} = V_{DD} = V_{SS} = 0V$, $V_{BB} = -5V$

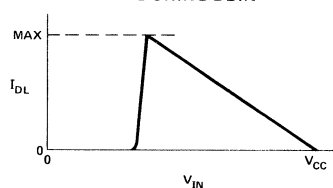| Symbol	Parameter	Typ.	Max.	Unit	Test Condition
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C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT$_A$ = −0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED. [3]
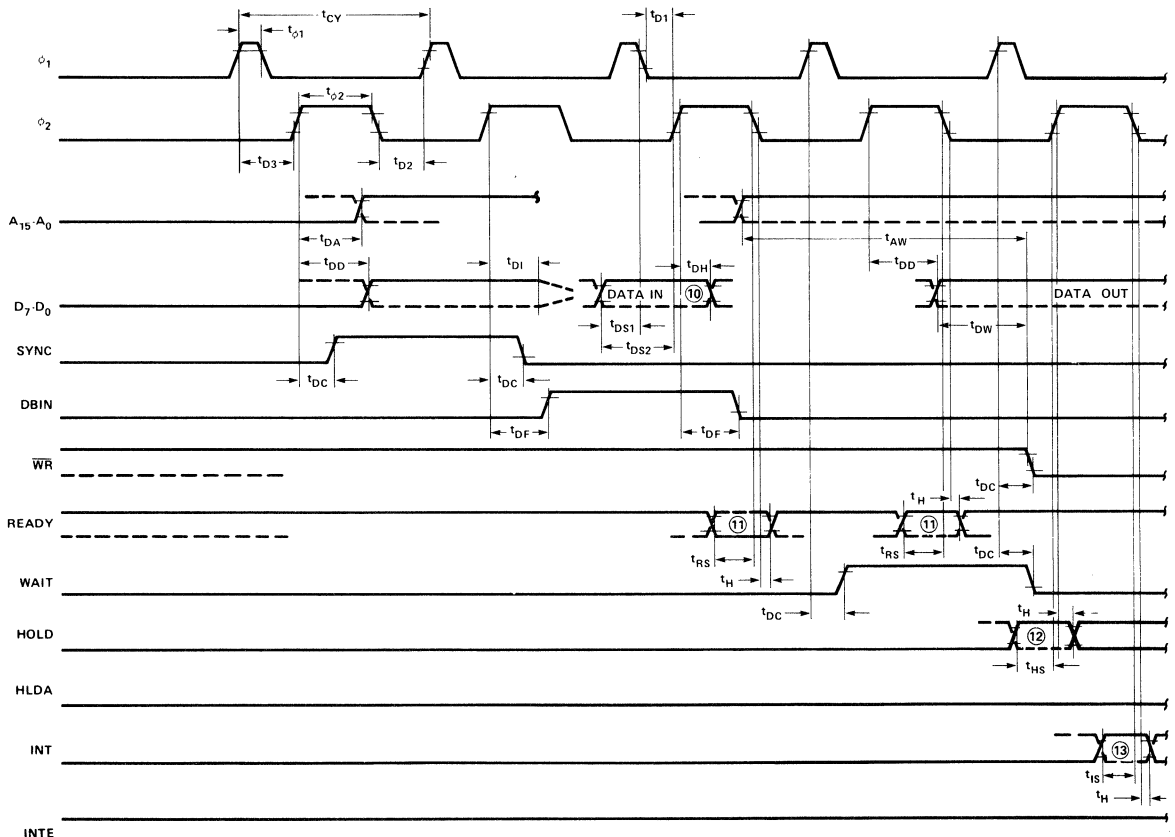

DATA BUS CHARACTERISTIC DURING DBIN

A.C. CHARACTERISTICS

CAUTION: When operating the 8080A-1 at or near full speed, care must be taken to assure precise timing compatibility between 8080A-1, 8224 and 8228.

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = –5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	.32	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	25	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	50		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	145		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	60		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	60		nsec	
t_{DA}[2]	Address Output Delay From ϕ_2		150	nsec	C_L = 50pf
t_{DD}[2]	Data Output Delay From ϕ_2		180	nsec	
t_{DC}[2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		110	nsec	C_L = 50pf
t_{DF}[2]	DBIN Delay From ϕ_2	25	130	nsec	
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	10		nsec	

TIMING WAVEFORMS[14]

(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)
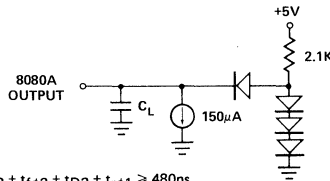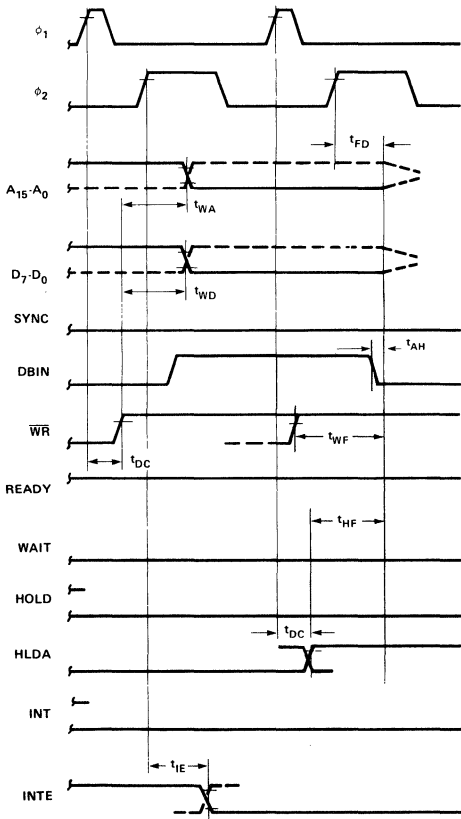
A.C. CHARACTERISTICS (Continued)

$T_A = 0°C$ to $70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted

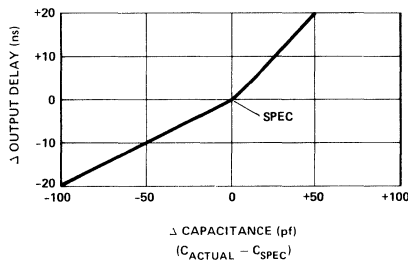| Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	120		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	$C_L = 50pf$
t_{RS}	READY Setup Time During ϕ_2	90		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	120		nsec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	100		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	$C_L = 50pf$: Address, Data
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	$C_L = 50pf$: $\overline{WR}$, HLDA, DBIN
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	–20		nsec	

NOTES:
1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. $t_{DH} = 50$ ns or t_{DF}, whichever is less.
2. Load Circuit.

3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 320ns$.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE
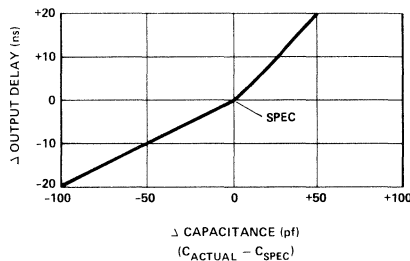
Δ CAPACITANCE (pf)
$(C_{ACTUAL} - C_{SPEC})$

4. The following are relevant when interfacing the 8080A to devices having $V_{IH} = 3.3V$:
    a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
    b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
    c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L >$ C$_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L <$ C$_{SPEC}$.
5. $t_{AW} = 2$ t_{CY} $-t_{D3}$ $-t_{r\phi2}$ $-110nsec$.
6. $t_{DW} = t_{CY}$ $-t_{D3}$ $-t_{r\phi2}$ $-150nsec$.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2}$ +10ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2}$ $-50ns$.
9. $t_{WF} = t_{D3} + t_{r\phi2}$ $-10ns$
10. Data in must be stable for this period during DBIN $\cdot T_3$. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

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8080A-2
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

- **TTL Drive Capability**
- **1.5 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**

- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.

8080A CPU FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . 0°C to +70°C
Storage Temperature . . . . -65°C to +150°C
All Input or Output Voltages
   With Respect to V_{BB} . . . . -0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB} -0.3V to +20V
Power Dissipation 1.5W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = –5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IHC}	Clock Input High Voltage	9.0		$V_{DD}+1$	V	
V_{IL}	Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IH}	Input High Voltage	3.3		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150µA.
$I_{DD(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation
$I_{CC(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	T_{CY} = .38µsec
$I_{BB(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	µA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	µA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			−100 −2.0	µA mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}+0.8V$ $V_{SS}+0.8V \leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 −100	µA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS} + 0.45V$

CAPACITANCE

T_A = 25°C V_{CC} = V_{DD} = V_{SS} = 0V, V_{BB} = –5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = –0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED. [3]

DATA BUS CHARACTERISTIC DURING DBIN

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY} [3]	Clock Period	.38	2.0	μ sec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	175		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	70		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	70		nsec	
t_{DA} [2]	Address Output Delay From ϕ_2		175	nsec	C_L = 100pf
t_{DD} [2]	Data Output Delay From ϕ_2		200	nsec	
t_{DC} [2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		120	nsec	C_L = 50pf
t_{DF} [2]	DBIN Delay From ϕ_2	25	140	nsec	
t_{DI} [1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	20		nsec	

TIMING WAVEFORMS[14] (Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)

A.C. CHARACTERISTICS (Continued)

$T_A = 0°C$ to $70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	130		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	$C_L = 50pf$
t_{RS}	READY Setup Time During ϕ_2	90		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	120		nsec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	100		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	$C_L = 100pf$: Address, Data
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	$C_L = 50pf$: $\overline{WR}$, HLDA, DBIN
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	

NOTES:
1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. $t_{DH} = 50$ ns or t_{DF}, whichever is less.
2. Load Circuit.

3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 380ns$.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE

Δ CAPACITANCE (pf)
$(C_{ACTUAL} - C_{SPEC})$

4. The following are relevant when interfacing the 8080A to devices having $V_{IH} = 3.3V$:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L >$ C_{SPEC}, subtract .3ns/pF (from modified delay) if $C_L <$ C_{SPEC}.
5. $t_{AW} = 2 t_{CY} - t_{D3} - t_{r\phi2} - 130nsec.$
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170nsec.$
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10ns$. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50ns$.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10ns$
10. Data in must be stable for this period during DBIN $\cdot T_3$. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

intel®

M8080A

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

The M8080A is functionally compatible with the Intel® 8080.

- **Full Military Temperature Range −55°C to +125°C**
- **±10% Power Supply Tolerance**
- **2 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**

- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**
- **TTL Drive Capability**

The Intel® M8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The M8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The M8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/ retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the M8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the M8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.

M8080A CPU FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . –55°C to +125°C
Storage Temperature . . . . –65°C to +150°C
All Input or Output Voltages
   With Respect to V_{BB} . . . . –0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB} –0.3V to +20V
Power Dissipation 1.7W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = –55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = –5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IHC}	Clock Input High Voltage	8.5		$V_{DD}+1$	V	
V_{IL}	Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IH}	Input High Voltage	3.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs, I_{OH} = 150μA.
V_{OH}	Output High Voltage	3.7			V	
$I_{DD(AV)}$	Avg. Power Supply Current (V_{DD})		50	80	mA	Operation T_{CY} = .48 μsec
$I_{CC(AV)}$	Avg. Power Supply Current (V_{CC})		60	100	mA	
$I_{BB(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			–100 / –2.0	μA / mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}+0.8V$ / $V_{SS}+0.8V \leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 / –100	μA	$V_{ADDR/DATA} = V_{CC}$ / $V_{ADDR/DATA} = V_{SS} + 0.45V$

CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = –5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = –0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED. [3]

DATA BUS CHARACTERISTIC DURING DBIN

A.C. CHARACTERISTICS

T_A = –55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = –5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	0.48	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	80		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		nsec	
t_{DA} [2]	Address Output Delay From ϕ_2		200	nsec	
t_{DD} [2]	Data Output Delay From ϕ_2		220	nsec	
t_{DC} [2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		140	nsec	C_L = 50pf
t_{DF} [2]	DBIN Delay From ϕ_2	25	150	nsec	
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		nsec	

TIMING WAVEFORMS[14]
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 7.0V, "0" = 1.0V; INPUTS "1" = 3.0V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)
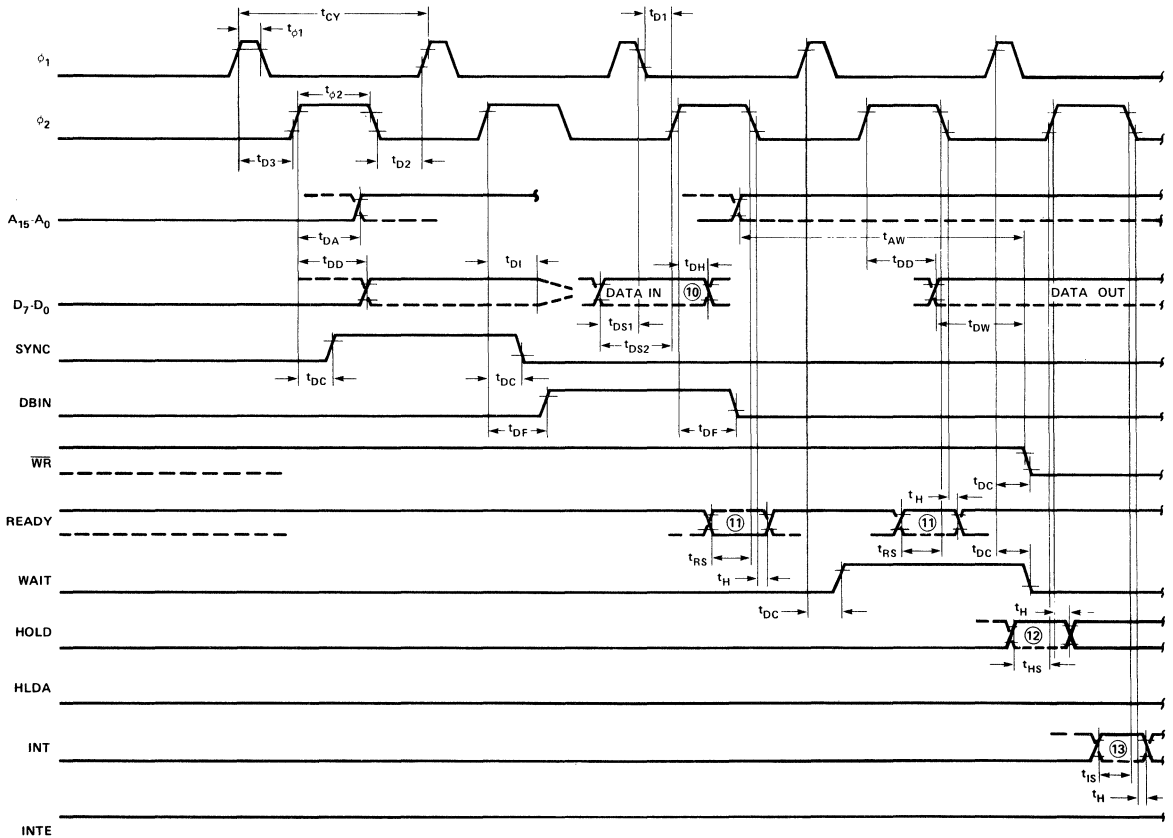
A.C. CHARACTERISTICS (Continued)

$T_A = -55°C$ to $+125°C$, $V_{DD} = +12V \pm 10\%$, $V_{CC} = +5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	130		n sec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		n sec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	n sec	$C_L = 50pf$
t_{RS}	READY Setup Time During ϕ_2	120		n sec	
t_{HS}	HOLD Setup Time to ϕ_2	140		n sec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	120		n sec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		n sec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		130	n sec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		n sec	
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		n sec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		n sec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		n sec	$C_L = 50pf$
t_{HF} [2]	HLDA to Float Delay	[8]		n sec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		n sec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	−20		n sec	

NOTES:
1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. $t_{DH} = 50$ ns or t_{DF}, whichever is less.
2. Load Circuit.

3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 480ns$.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE

Δ CAPACITANCE (pf)
$(C_{ACTUAL} - C_{SPEC})$

4. The following are relevant when interfacing the M8080A to devices having $V_{IH} = 3.3V$:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L >$ SPEC, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2 t_{CY} - t_{D3} - t_{r\phi2} - 140nsec$.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170nsec$.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10ns$. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50ns$.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10ns$.
10. Data in must be stable for this period during DBIN ·T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

intel®

8224

CLOCK GENERATOR AND DRIVER
FOR 8080A CPU

- **Single Chip Clock Generator/Driver for 8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**

- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**

The 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer, to meet a variety of system speed requirements.

Also included are circuits to provide power-up reset, advance status strobe and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

PIN CONFIGURATION

BLOCK DIAGRAM

PIN NAMES

RESIN	RESET INPUT	XTAL 1	{	CONNECTIONS
RESET	RESET OUTPUT	XTAL 2	{	FOR CRYSTAL
RDYIN	READY INPUT	TANK		USED WITH OVERTONE XTAL
READY	READY OUTPUT	OSC		OSCILLATOR OUTPUT
SYNC	SYNC INPUT	ϕ_2 (TTL)		ϕ_2 CLK (TTL LEVEL)
STSTB	STATUS STB (ACTIVE LOW)	Vcc		+5V
		VDD		+12V
ϕ_1	{ 8080	GND		0V
ϕ_2	{ CLOCKS			

6-20

FUNCTIONAL DESCRIPTION

General

The 8224 is a single chip Clock Generator/Driver for the 8080A CPU. It contains a crystal-controlled oscillator, a "divide by nine" counter, two high-level drivers and several auxiliary logic functions.

Oscillator

The oscillator circuit derives its basic operating frequency from an external, series resonant, fundamental mode crystal. Two inputs are provided for the crystal connections (XTAL1, XTAL2).

The selection of the external crystal frequency depends mainly on the speed at which the 8080A is to be run at. Basically, the oscillator operates at 9 times the desired processor speed.

A simple formula to guide the crystal selection is:

$$\text{Crystal Frequency} = \frac{1}{t_{CY}} \text{ times } 9$$

Example 1:   (500ns t_{CY})
2mHz times 9 = 18mHz*

Example 2:   (800ns t_{CY})
1.25mHz times 9 = 11.25mHz

Another input to the oscillator is TANK. This input allows the use overtone mode crystals. This type of crystal generally has much lower "gain" than the fundamental type so an external LC network is necessary to provide the additional "gain" for proper oscillator operation. The external LC network is connected to the TANK input and is AC coupled to ground. See Figure 4.

The formula for the LC network is:

$$F = \frac{1}{2\pi \sqrt{LC}}$$

The output of the oscillator is buffered and brought out on ⊖SC (pin 12) so that other system timing signals can be derived from this stable, crystal-controlled source.

*When using crystals above 10mHz a small amount of frequency "trimming" may be necessary to produce the exact desired frequency. The addition of a small selected capacitance (3pF - 10pF) in series with the crystal will accomplish this function.

Clock Generator

The Clock Generator consists of a synchronous "divide by nine" counter and the associated decode gating to create the waveforms of the two 8080A clocks and auxiliary timing signals.

The waveforms generated by the decode gating follow a simple 2-5-2 digital pattern. See Figure 2. The clocks generated; phase 1 and phase 2, can best be thought of as consisting of "units" based on the oscillator frequency. Assume that one "unit" equals the period of the oscillator frequency. By multiplying the number of "units" that are contained in a pulse width or delay, times the period of the oscillator frequency, the approximate time in nanoseconds can be derived.

The outputs of the clock generator are connected to two high level drivers for direct interface to the 8080A CPU. A TTL level phase 2 is also brought out $\phi 2$ (TTL) for external timing purposes. It is especially useful in DMA dependant activities. This signal is used to gate the requesting device onto the bus once the 8080A CPU issues the Hold Acknowledgement (HLDA).

Several other signals are also generated internally so that optimum timing of the auxiliary flip-flops and status strobe (STSTB) is achieved.
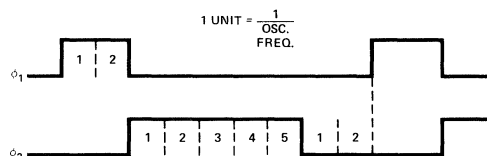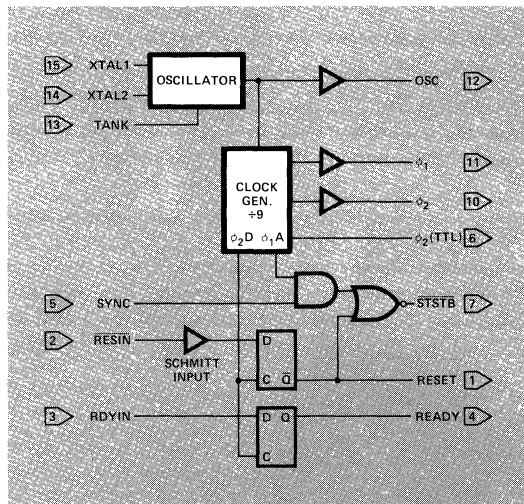
EXAMPLE: (8080 t_{CY} = 500ns)
OSC = 18mHz/55ns
ϕ_1 = 110ns (2 x 55ns)
ϕ_2 = 275ns (5 x 55ns)
ϕ_2-ϕ_1 = 110ns (2 x 55ns)

STSTB (Status Strobe)

At the beginning of each machine cycle the 8080A CPU issues status information on its data bus. This information tells what type of action will take place during that machine cycle. By bringing in the SYNC signal from the CPU, and gating it with an internal timing signal (ϕ1A), an active low strobe can be derived that occurs at the start of each machine cycle at the earliest possible moment that status data is stable on the bus. The $\overline{\text{STSTB}}$ signal connects directly to the 8228 System Controller.

The power-on Reset also generates $\overline{\text{STSTB}}$, but of course, for a longer period of time. This feature allows the 8228 to be automatically reset without additional pins devoted for this function.

Power-On Reset and Ready Flip-Flops

A common function in 8080A Microcomputer systems is the generation of an automatic system reset and start-up upon initial power-on. The 8224 has a built in feature to accomplish this feature.

An external RC network is connected to the $\overline{\text{RESIN}}$ input. The slow transition of the power supply rise is sensed by an internal Schmitt Trigger. This circuit converts the slow transition into a clean, fast edge when its input level reaches a predetermined value. The output of the Schmitt Trigger is connected to a "D" type flip-flop that is clocked with ϕ2D (an internal timing signal). The flip-flop is synchronously reset and an active high level that complies with the 8080A input spec is generated. For manual switch type system Reset circuits, an active low switch closing can be connected to the $\overline{\text{RESIN}}$ input in addition to the power-on RC net-network.

The READY input to the 8080A CPU has certain timing specifications such as "set-up and hold" thus, an external synchronizing flip-flop is required. The 8224 has this feature built-in. The RDYIN input presents the asynchronous "wait request" to the "D" type flip-flop. By clocking the flip-flop with ϕ2D, a synchronized READY signal at the correct input level, can be connected directly to the 8080A.

The reason for requiring an external flip-flop to synchronize the "wait request" rather than internally in the 8080 CPU is that due to the relatively long delays of MOS logic such an implementation would "rob" the designer of about 200ns during the time his logic is determining if a "wait" is necessary. An external bipolar circuit built into the clock generator eliminates most of this delay and has no effect on component count.
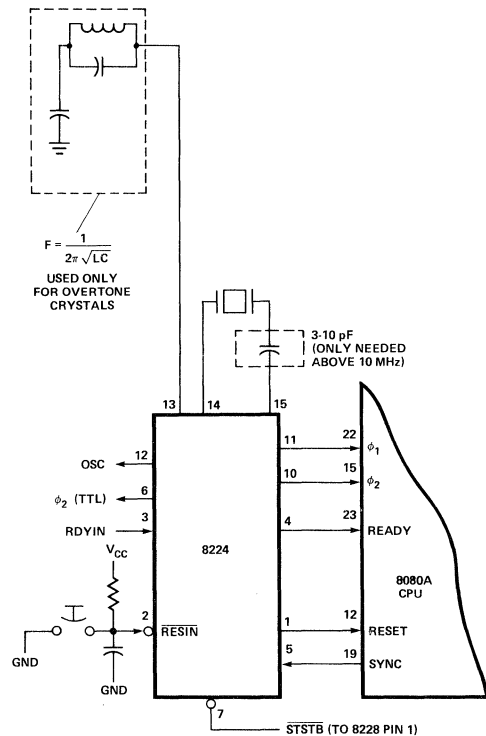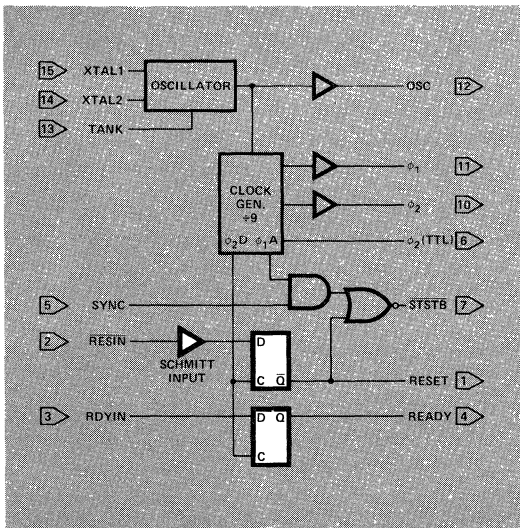
D.C. Characteristics

T_A = 0°C to 70°C; V_{CC} = +5.0V ±5%; V_{DD} = +12V ±5%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Current Loading			–.25	mA	V_F = .45V
I_R	Input Leakage Current			10	μA	V_R = 5.25V
V_C	Input Forward Clamp Voltage			1.0	V	I_C = –5mA
V_{IL}	Input "Low" Voltage			.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.6 2.0			V	Reset Input All Other Inputs
V_{IH}-V_{IL}	REDIN Input Hysteresis	.25			mV	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage			.45	V	(ϕ_1,ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} =2.5mA
				.45	V	All Other Outputs I_{OL} = 15mA
V_{OH}	Output "High" Voltage ϕ_1 , ϕ_2 READY, RESET All Other Outputs	9.4 3.6 2.4			V V V	I_{OH} = –100μA I_{OH} = –100μA I_{OH} = –1mA
I_{SC}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	–10		–60	mA	V_O = 0V V_{CC} = 5.0V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Note: 1. Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

CRYSTAL REQUIREMENTS

Tolerance: .005% at 0°C –70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

*With tank circuit use 3rd overtone mode.

A.C. Characteristics

$V_{CC} = +5.0V \pm 5\%$; $V_{DD} = +12.0V \pm 5\%$; $T_A = 0°C$ to $70°C$

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	**Typ.**	**Max.**		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\dfrac{2tcy}{9} - 20ns$			ns	$C_L = 20pF$ to $50pF$
$t_{\phi 2}$	ϕ_2 Pulse Width	$\dfrac{5tcy}{9} - 35ns$				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\dfrac{2tcy}{9} - 14ns$				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\dfrac{2tcy}{9}$		$\dfrac{2tcy}{9} + 20ns$		
t_R	ϕ_1 and ϕ_2 Rise Time			20		
t_F	ϕ_1 and ϕ_2 Fall Time			20		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	ϕ_2TTL,CL=30 R_1=300Ω R_2=600Ω
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\dfrac{6tcy}{9} - 30ns$		$\dfrac{6tcy}{9}$		$\overline{STSTB}$,CL=15pF R_1 = 2K R_2 = 4K
t_{PW}	$\overline{STSTB}$ Pulse Width	$\dfrac{tcy}{9} - 15ns$				
t_{DRS}	RDYIN Setup Time to Status Strobe	$50ns - \dfrac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\dfrac{4tcy}{9}$				
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	$\dfrac{4tcy}{9} - 25ns$				Ready & Reset CL=10pF R_1=2K R_2=4K
t_{CLK}	CLK Period		$\dfrac{tcy}{9}$			
f_{max}	Maximum Oscillating Frequency	18.432			MHz	
C_{in}	Input Capacitance			8	pF	V_{CC}=+5.0V V_{DD}=+12V V_{BIAS}=2.5V f=1MHz

TEST CIRCUIT

WAVEFORMS

VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

EXAMPLE:

A.C. Characteristics (For t_{CY} = 488.28 ns)

T_A = 0°C to 70°C; V_{CC} = +5V ± 5%; V_{DD} = +12V ± 5%

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY}=488.28ns
$t_{\phi 2}$	ϕ_2 Pulse Width	236			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	95			ns	ϕ_1 & ϕ_2 Loaded to
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		129	ns	C_L = 20 to 50pF
t_r	Output Rise Time			20	ns	
t_f	Output Fall Time			20	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	−5		+15	ns	
t_{PW}	Status Strobe Pulse Width	40			ns	
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	−167			ns	Ready & Reset Loaded to 2mA/10pF
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	All measurements
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	referenced to 1.5V unless specified otherwise.
f	Oscillator Frequency			18.432	MHz	

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M8224
CLOCK GENERATOR AND DRIVER
FOR 8080A CPU

- **Single Chip Clock Generator/Driver for M8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**
- **Full Military Temperature Range -55°C to +125°C**

- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**

The M8224 is a single chip clock generator/driver for the M8080A CPU. It is controlled by a crystal, selected by the designer, to meet a variety of system speed requirements.

Also included are circuits to provide power-up reset, advance status strobe and synchronization of ready.

The M8224 provides the designer with a significant reduction of packages used to generate clocks and timing for M8080A.

PIN CONFIGURATION

M8224 BLOCK DIAGRAM

PIN NAMES

RESIN	RESET INPUT	XTAL 1	CONNECTIONS
RESET	RESET OUTPUT	XTAL 2	FOR CRYSTAL
RDYIN	READY INPUT	TANK	USED WITH OVERTONE XTAL
READY	READY OUTPUT	OSC	OSCILLATOR OUTPUT
SYNC	SYNC INPUT	ϕ_2 (TTL)	ϕ_2 CLK (TTL LEVEL)
STSTB	STATUS STB (ACTIVE LOW)	V_{CC}	+5V
ϕ_1	8080	V_{DD}	+12V
ϕ_2	CLOCKS	GND	0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . −55°C to 125°C
Storage Temperature . . . . −65°C to 150°C
Supply Voltage, V_{CC} . . . . −0.5V to +7V
Supply Voltage, V_{DD} . . . . −0.5V to +13.5V
Input Voltage . . . . −1.0V to +7V
Output Current 100mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = −55°C to 125°C; V_{CC} = +5.0V ±10%; V_{DD} = +12V ±10%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Current Loading			−.25	mA	V_F = .45V
I_R	Input Leakage Current			10	μA	V_R = 5.5V
V_C	Input Forward Clamp Voltage			−1.2	V	I_C = −5mA
V_{IL}	Input "Low" Voltage			.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage RESIN All Other Inputs	2.6 2.0			V	
V_{IH}-V_{IL}	RESIN Input Hysteresis	.25			V	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage OSC, $\phi2$ (TTL) All Other Outputs			.45 .45	V V	I_{OL} = 10mA I_{OL} = 2.5mA
V_{OH}	Output "High" Voltage ϕ_1 , ϕ_2 READY, RESET OSC, $\phi2$ (TTL), STSTB	9.0 3.3 2.4			V V V	I_{OH} = −100μA I_{OH} = −100μA I_{OH} = −1mA
I_{OS}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	−10		−60	mA	V_O = 0V V_{CC} = 5.0V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Note: 1. Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

CRYSTAL REQUIREMENTS

Tolerance: .005% at −55°C to 125°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

*With tank circuit use 3rd overtone mode.

A.C. CHARACTERISTICS

$V_{CC} = +5.0 \pm 10\%$; $V_{DD} = +12.0V \pm 10\%$; $T_A = -55^{\circ}C$ to $+125^{\circ}C$

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9} - 20ns$			ns	$C_L = 20pF$ to $50pF$
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9} - 45ns$				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9} - 25ns$				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9} + 40ns$		
t_R	ϕ_1 and ϕ_2 Rise Time			25		
t_F	ϕ_1 and ϕ_2 Fall Time			25		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		$+15$	ns	ϕ_2TTL,CL$=30pF$ $R_1=300\Omega$ $R_2=600\Omega$
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6tcy}{9} - 30ns$		$\frac{6tcy}{9}$		$\overline{STSTB}$,CL$=15pF$ $R_1 = 2K$ $R_2 = 4K$
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{tcy}{9} - 23ns$				
t_{DRS}	RDYIN Setup Time to Status Strobe	$50ns - \frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\frac{4tcy}{9}$				
t_{DR}	READY or RESET to ϕ_2 Delay	$\frac{4tcy}{9} - 25ns$				CL$=10pF$ $R_1=2K$ $R_2=4K$
t_{CLK}	CLK Period		$\frac{tcy}{9}$			
f_{max}	Maximum Oscillating Frequency	18.432			MHz	
C_{in}	Input Capacitance			8	pF	$V_{CC}=+5.0V$ $V_{DD}=+12V$ $V_{BIAS}=2.5V$ $f=1MHz$

TEST CIRCUIT

WAVEFORMS

VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 7.0V. READY, RESET Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

Example:

A.C. CHARACTERISTICS (For t_{CY} = 488.28 ns.)

T_A = -55°C to 125°C; V_{DD} = +5V ±10%; V_{DD} = +12V ±10%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY}=488.28ns
$t_{\phi 2}$	ϕ_2 Pulse Width	226			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	84			ns	ϕ_1 & ϕ_2 Loaded to
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		149	ns	C_L = 20 to 50pF
t_r	Output Rise Time			25	ns	
t_f	Output Fall Time			25	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	31			ns	Ready & Reset Loaded
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	to 2mA/10pF
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	All measurements referenced to 1.5V
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	unless specified otherwise.

8801
CLOCK GENERATOR CRYSTAL
FOR 8224/8080A

- Specifically Selected For Intel® 8224
- 18.432 MHz for 1.95 µs 8080A Cycle
- Simple Generation of All Standard Communication Baud Rates

- Frequency Deviation ±.005%
- Frequency Mode-Fundamental
- 0 - 70°C Operating Temperature

The 8801 is a quartz crystal specifically selected to operate with the 8224 clock generator and 8080A. It resonates in the fundamental frequency mode at 18.432 MHz. This frequency allows the 8080A at full speed ($T_{CY} = 488$ ns) to have a cycle of 1.95 µs and also simplifies the generation of all standard communication baud rates. The 8801 crystal is exactly matched to the requirements of the 8080A/8224 and provides both high-performance and system flexibility for the microcomputer designer.

8801 INTERFACE
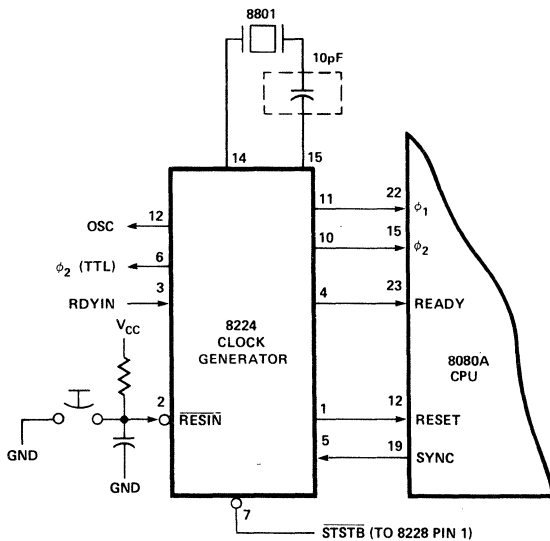
PACKAGING INFORMATION
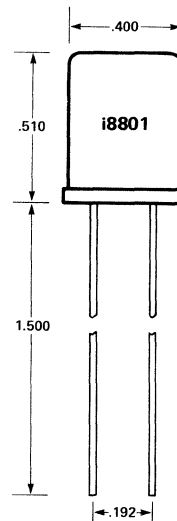
APPLICATIONS

The selection of 18.432 MHz provides the 8080A with clocks whose period is 488ns. This allows the 8080A to operate at very close to its maximum specified speed (480 ns). The 8224, when used with the 8801, outputs a signal on its OSC pin that is an approximately symetrical square wave at a frequency of 18.432 MHz. This frequency signal can be easily divided down to generate an accurate, stable baud rate clock that can be connected directly to the transmitter or receiver clocks of the 8251 USART. This feature allows the designer to support most standard communication interfaces with a minimum of extra hardware.

The chart below (Fig. 1) shows the equivalent baud rates that are generated with the corresponding dividers.

BLOCK DIAGRAM
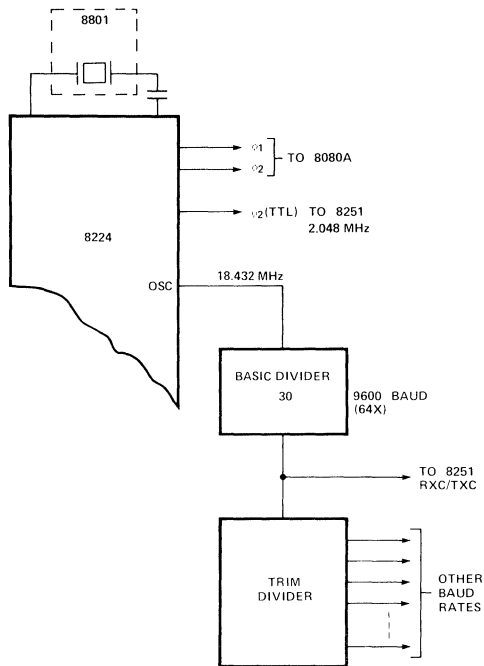
BAUD RATE 64x	BAUD RATE 16x	FREQUENCY	BASIC DIVIDER	PLUS TRIM DIVIDER
9600		614.4 KH	÷30	—
4800	19.2K	307.2 KH	÷30	÷2
2400	9600	153.6 KH	÷30	÷4
1200	4800	76.8 KH	÷30	÷8
600	2400	38.4 KH	÷30	÷16
300	1200	19.2 KH	÷30	÷32
	600	9.6 KH	÷30	÷64
	300	4.8 KH	÷30	÷128
*109.1		6.982 KH	÷30	÷88

*For 109.1 (64x) Baud rate divide 1200 Baud Frequency (76.8 KH) by 11.

Figure 1. Baud Rate Chart

ELECTRICAL CHARACTERISTICS

Recommended Drive Level 5mW
Type of Resonance . . . . Series
Equivalent Resistance . . . . 20 ohms
Maximum Shunt Capacity 7pF
Maximum Frequency Deviation
       $0° - 70°C$ . . . . ±.005%
     $-55°- 125°C$ . . . . ±.002%

ORDERING INFORMATION

Intel Products may be ordered from either your local Intel sales office or stocking Intel distributor.

intel®

8228/8238
SYSTEM CONTROLLER AND BUS DRIVER
FOR 8080A CPU

- **Single Chip System Control for MCS-80™ Systems**
- **Built-in Bi-Directional Bus Driver for Data Bus Isolation**
- **Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**

- **User Selected Single Level Interrupt Vector (RST 7)**
- **28 Pin Dual In-Line Package**
- **Reduces System Package Count**
- ***8238 Has Advanced $\overline{\text{IOW}}/\overline{\text{MEMW}}$ for Large System Timing Control**

The 8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bi-directional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems deisgner to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an INTERRUPT ACKNOWLEDGE by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION

$\overline{\text{STSTB}}$	1	28	V_{CC}
HLDA	2	27	$\overline{\text{I/OW}}$
$\overline{\text{WR}}$	3	26	$\overline{\text{MEMW}}$
DBIN	4	25	$\overline{\text{I/OR}}$
DB4	5	24	$\overline{\text{MEMR}}$
D4	6	23	$\overline{\text{INTA}}$
DB7	7	22	$\overline{\text{BUSEN}}$
D7	8	21	D6
DB3	9	20	DB6
D3	10	19	D5
DB2	11	18	DB5
D2	12	17	D1
DBØ	13	16	DB1
GND	14	15	DØ

8228/8238

8228/8238 BLOCK DIAGRAM
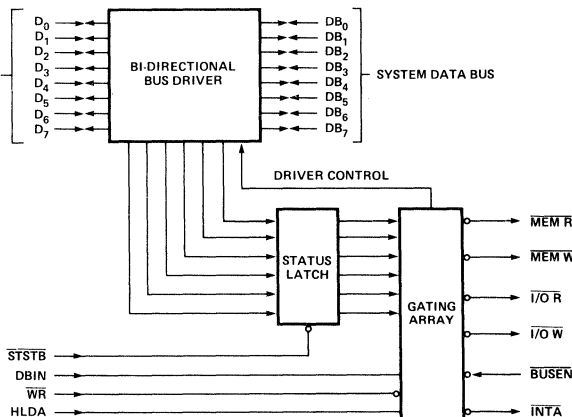
PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	INTA	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
$\overline{\text{I/OR}}$	I/O READ	$\overline{\text{WR}}$	WR (FROM 8080)
$\overline{\text{I/OW}}$	I/O WRITE	$\overline{\text{BUSEN}}$	BUS ENABLE INPUT
$\overline{\text{MEMR}}$	MEMORY READ	$\overline{\text{STSTB}}$	STATUS STROBE (FROM 8224)
$\overline{\text{MEMW}}$	MEMORY WRITE	V_{CC}	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

FUNCTIONAL DESCRIPTION

General

The 8228 and 8238 are single chip System Controllers and Data Bus drivers for the 8080 Microcomputer System. They generate all control signals required to directly interface MCS-80™ family RAM, ROM, and I/O components.

Schottky Bipolar technology is used to maintain low delay times and provide high output drive capability to support small to medium systems.

Bi-Directional Bus Driver

An eight bit, bi-directional bus driver is provided to buffer the 8080 data bus from Memory and I/O devices. The 8080A data bus has an input requirement of 3.3 volts (min) and can drive (sink) a maximum current of 1.9mA. The 8228/38 data bus driver assures that these input requirements will be not only met but exceeded for enhanced noise immunity. Also, on the system side of the driver adequate drive current is available (10mA Typ.) so that a large number of Memory and I/O devices can be directly connected to the bus.

The Bi-Directional Bus Driver is controlled by signals from the Gating Array so that proper bus flow is maintained and its outputs can be forced into their high impedance state (3-state) for DMA activities.

Status Latch

At the beginning of each machine cycle the 8080 CPU issues "status" information on its data bus that indicates the type of activity that will occur during the cycle. The 8228/38 stores this information in the Status Latch when the $\overline{STSTB}$ input goes "low". The output of the Status Latch is connected to the Gating Array and is part of the Control Signal generation.

Gating Array

The Gating Array generates control signals ($\overline{MEM\ R}$, $\overline{MEM\ W}$, $\overline{I/O\ R}$, $\overline{I/O\ W}$ and $\overline{INTA}$) by gating the outputs of the Status Latch with signals from the 8080 CPU (DBIN, $\overline{WR}$, and HLDA).

The "read" control signals ($\overline{MEM\ R}$, $\overline{I/O\ R}$ and $\overline{INTA}$) are derived from the logical combination of the appropriate Status Bit (or bits) and the DBIN input from the 8080 CPU.

The "write" control signals from the 8228 ($\overline{MEM\ W}$, $\overline{I/O\ W}$) are derived from the logical combination of the appropriate Status Bit (or bits) and the $\overline{WR}$ input from the 8080 CPU. The write signals coming from the 8238 are advanced for large system timing control.

All Control Signals are "active low" and directly interface to MCS-80 family RAM, ROM and I/O components.

The $\overline{INTA}$ control signal is normally used to gate the "interrupt instruction port" onto the bus. It also provides a special feature in the 8228/38. If only one basic vector is needed in the interrupt structure, such as in small systems, the 8228/38 can automatically insert a RST 7 instruction onto the bus at the proper time. To use this option, simply connect the $\overline{INTA}$ output of the 8228/38 (pin 23) to the +12 volt supply through a series resistor (1K ohms). The voltage is sensed internally by the 8228/38 and logic is "set-up" so that when the DBIN input is active a RST 7 instruction is gated on to the bus when an interrupt is acknowledged. This feature provides a single interrupt vector with no additional components, such as an interrupt instruction port.

When using CALL as an Interrupt instruction the 8228/38 will generate an $\overline{INTA}$ pulse for each of the three bytes.

The $\overline{BUSEN}$ (Bus Enable) input to the Gating Array is an asynchronous input that forces the data bus output buffers and control signal buffers into their high-impedance state if it is a "one". If $\overline{BUSEN}$ is a "zero" normal operation of the data buffer and control signals take place.
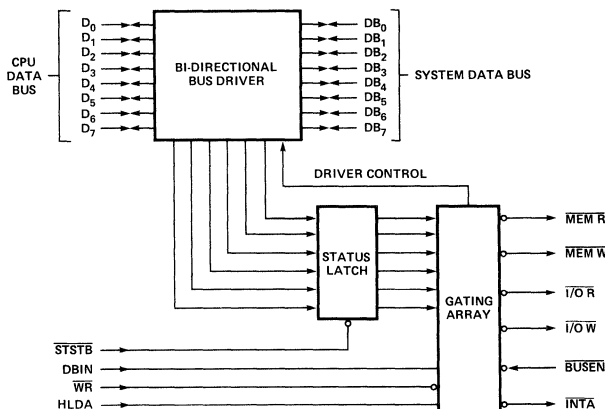
8228/38 BLOCK DIAGRAM
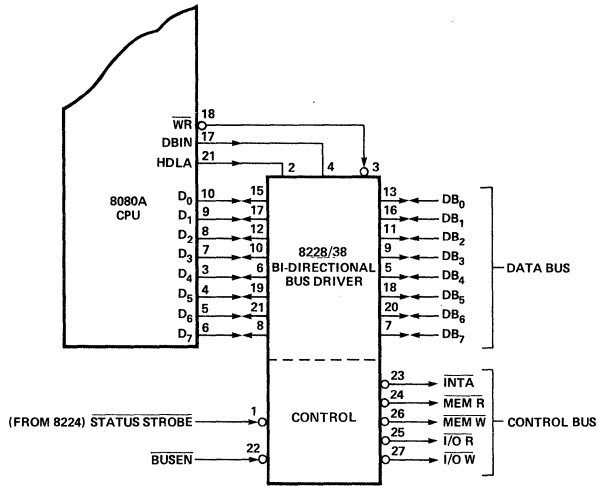
STATUS WORD CHART

DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH ①	MEMORY READ ②	MEMORY WRITE ③	STACK READ ④	STACK WRITE ⑤	INPUT READ ⑥	OUTPUT WRITE ⑦	INTERRUPT ACKNOWLEDGE ⑧	HALT ACKNOWLEDGE ⑨	INTERRUPT ACKNOWLEDGE WHILE HALT ⑩
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

TYPE OF MACHINE CYCLE

Ⓝ STATUS WORD

CONTROL SIGNALS:
$\overline{INTA}$
(NONE)
$\overline{INTA}$
$\overline{I/O\ W}$
$\overline{I/O\ R}$
$\overline{MEM\ W}$
$\overline{MEM\ R}$
$\overline{MEM\ W}$
$\overline{MEM\ R}$
$\overline{MEM\ R}$

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . −0°C to 70°C
Storage Temperature . . . . −65°C to 150°C
Supply Voltage, V_{CC} . . . . −0.5V to +7V
Input Voltage . . . . −1.5V to +7V
Output Current 100mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage, All Inputs		.75	−1.0	V	V_{CC}=4.75V; I_C=−5mA
I_F	Input Load Current, $\overline{STSTB}$			500	μA	V_{CC} = 5.25V
	D_2 & D_6			750	μA	V_F =0.45V
	D_0, D_1, D_4, D_5, & D_7			250	μA	
	All Other Inputs			250	μA	
I_R	Input Leakage Current $\overline{STSTB}$			100	μA	V_{CC}=5.25V
	DB_0-DB_7			20	μA	V_R = 5.25V
	All Other Inputs			100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8		2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		140	190	mA	V_{CC}=5.25V
V_{OL}	Output Low Voltage, D_0-D_7			.45	V	V_{CC}=4.75V; I_{OL}=2mA
	All Other Outputs			.45	V	I_{OL} = 10mA
V_{OH}	Output High Voltage, D_0-D_7	3.6	3.8		V	V_{CC}=4.75V; I_{OH}=−10μA
	All Other Outputs	2.4			V	I_{OH} = −1mA
I_{OS}	Short Circuit Current, All Outputs	15		90	mA	V_{CC}=5V
$I_{O(off)}$	Off State Output Current, All Control Outputs			100	μA	V_{CC}=5.25V; V_O=5.25
				−100	μA	V_O=.45V
I_{INT}	INTA Current			5	mA	(See Figure below)

Note 1: Typical values are for T_A = 25ºC and nominal supply voltages.

WAVEFORMS
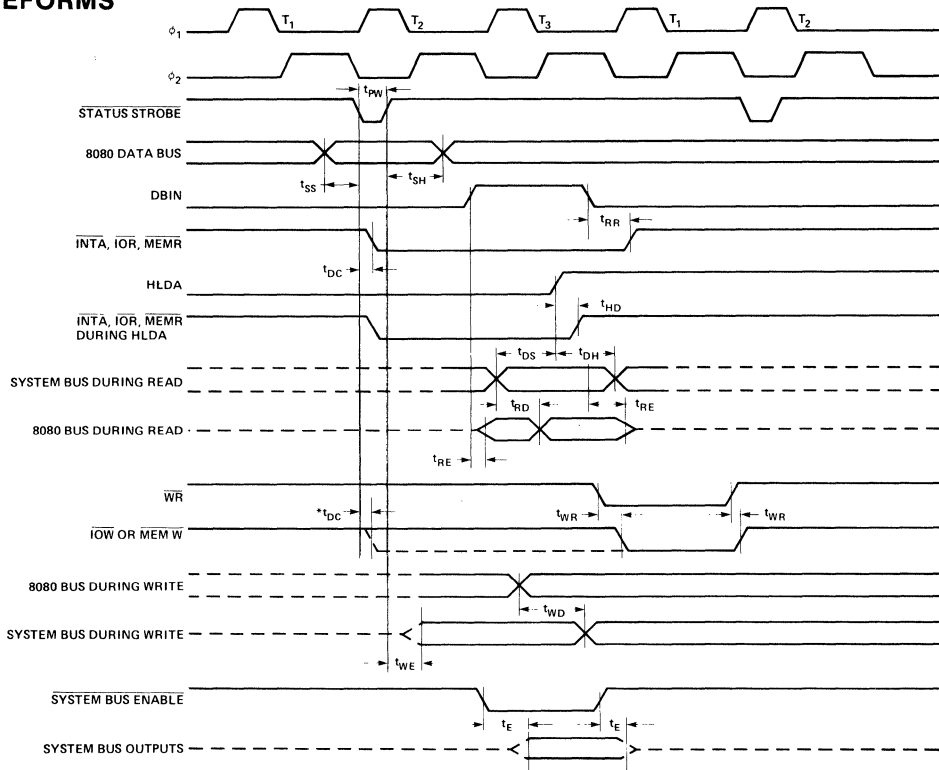
VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*ADVANCED $\overline{\text{IOW}}$/$\overline{\text{MEMW}}$ FOR 8238 ONLY.

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$.

Symbol	Parameter	Limits Min.	Limits Max.	Units	Condition
t_{PW}	Width of Status Strobe	22		ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from $\overline{\text{STSTB}}$ to any Control Signal	20	60	ns	C_L = 100pF
t_{RR}	Delay from DBIN to Control Outputs		30	ns	C_L = 100pF
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	C_L = 25pF
t_{RD}	Delay from System Bus to 8080 Bus during Read		30	ns	C_L = 25pF
t_{WR}	Delay from $\overline{\text{WR}}$ to Control Outputs	5	45	ns	C_L = 100pF
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after $\overline{\text{STSTB}}$		30	ns	C_L = 100pF
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	C_L = 100pF
t_E	Delay from $\overline{\text{System Bus Enable}}$ to System Bus DB_0-DB_7		30	ns	C_L = 100pF
t_{HD}	HLDA to Read Status Outputs		25	ns	
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	C_L = 100pF

CAPACITANCE

This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25^\circ C$, $f = 1MHz$.

Note 2: For D_0-D_7: $R_1 = 4K\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.

INTA Test Circuit (for RST 7)
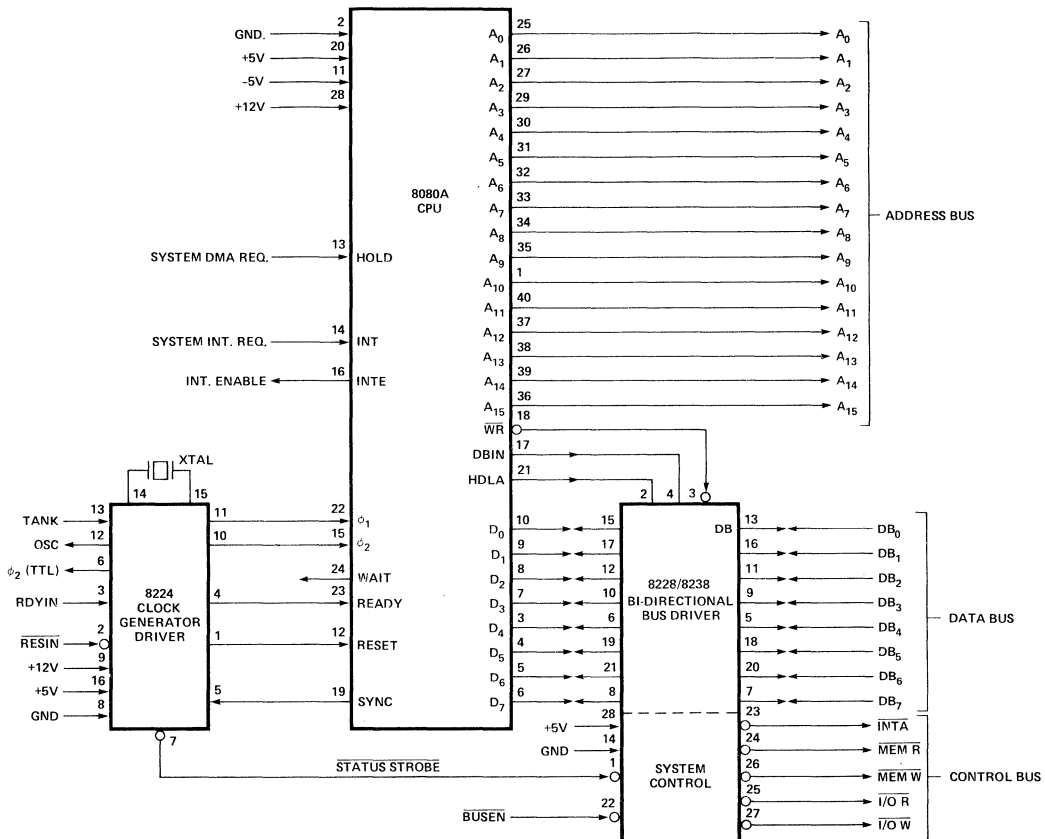
CPU Standard Interface

intel®

M8228/M8238
SYSTEM CONTROLLER AND BUS DRIVER
FOR M8080A CPU

- **Single Chip System Control for MCS™-80 Systems**
- **Built-in Bi-Directional Bus Driver for Data Bus Isolation**
- **Allows the use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **M8238 has Advanced IOW/MEMW for Large System Timing Control**

- **User Selected Single Level Interrupt Vector (RST 7)**
- **28 Pin Dual In-Line Package**
- **Reduces System Package Count**
- **Full Military Temperature Range -55°C to +125°C**
- **±10% Power Supply Tolerance**

The M8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bi-directional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The M8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an INTERRUPT ACKNOWLEDGE by the M8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The M8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION
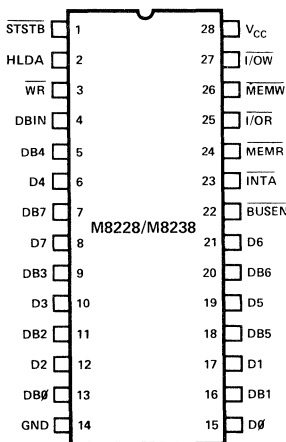
M8228/M8238 BLOCK DIAGRAM

PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	INTA	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
I/OR	I/O READ	WR	WR (FROM 8080)
I/OW	I/O WRITE	BUSEN	BUS ENABLE INPUT
MEMR	MEMORY READ	STSTB	STATUS STROBE (FROM 8224)
MEMW	MEMORY WRITE	Vcc	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . -55°C to 125°C

Storage Temperature . . . . -65°C to 150°C

Supply Voltage, V_{CC} . . . . -0.5V to +7V

Input Voltage . . . . -1.0V to +7V

Output Current 100mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS T_A = -55°C to 125°C; V_{CC} = 5V ±10%.

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
V_C	Input Clamp Voltage, All Inputs		-1.2	V	I_C = -5mA
I_F	Input Load Current, $\overline{STSTB}$		500	μA	
	D_2, D_6		750	μA	V_F = 0.4V
	D_0, D_1, D_4, D_5, D_7		250	μA	
	All Other Inputs		250	μA	
I_R	Input Leakage Current $DB_0 - D_7$		20	μA	V_R = 5.5V
	All Other Inputs		100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8	2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		210	mA	
V_{OL}	Output Low Voltage, $D_0 - D_7$		.5	V	I_{OL} = 2mA
	All Other Outputs		.5	V	I_{OL} = 10mA
V_{OH}	Output High Voltage, $D_0 - D_7$	3.3		V	I_{OH} = -10μA
	All Other Outputs	2.4		V	I_{OH} = -1mA
I_{OS}	Short Circuit Current, All Outputs	15	90	mA	V_{CC} = 5V
$I_{O (Off)}$	Off State Output Current, All Controls Outputs		100	μA	V_O = 5.5V
			-100	μA	V_O = .45V
I_{INT}	$\overline{INTA}$ Current		5	mA	(See Figure on page 3)

Note 1:   Typical values are for T_A = 25°C and nominal supply voltages.

CAPACITANCE This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25^\circ C$, $f = 1MHz$.

Note 2: For D_0-D_7: $R_1 = 4K\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.

TEST CIRCUIT[2]

OUTPUT PIN

C_L

V_{CC}

R_1

R_2

GND

GND

M8228/M8238

INTA 23

$1K\Omega \pm 10\%$

+12V

I

I_{INT}

INTA Test Circuit (for RST 7)

A.C. CHARACTERISTICS $T_A = -55^\circ C$ to $125^\circ C$; $V_{CC} = 5V \pm 10\%$.

Symbol	Parameter	Limits		Units	Condition
		Min.	Max.		
t_{PW}	Width of Status Strobe	25		ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	75	ns	$C_L = 100pF$
t_{RR}	Delay from DBIN to Control Outputs		30	ns	$C_L = 100pF$
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	$C_L = 25pF$
t_{RD}	Delay from System Bus to 8080 Bus during Read		45	ns	$C_L = 25pF$
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	60	ns	$C_L = 100pF$
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$		30	ns	$C_L = 100pF$
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	$C_L = 100pF$
t_E	Delay from $\overline{System Bus Enable}$ to System Bus DB_0-DB_7		30	ns	$C_L = 100pF$
t_{HD}	HLDA to Read Status Outputs		25	ns	$C_L = 100pF$
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	

WAVEFORMS
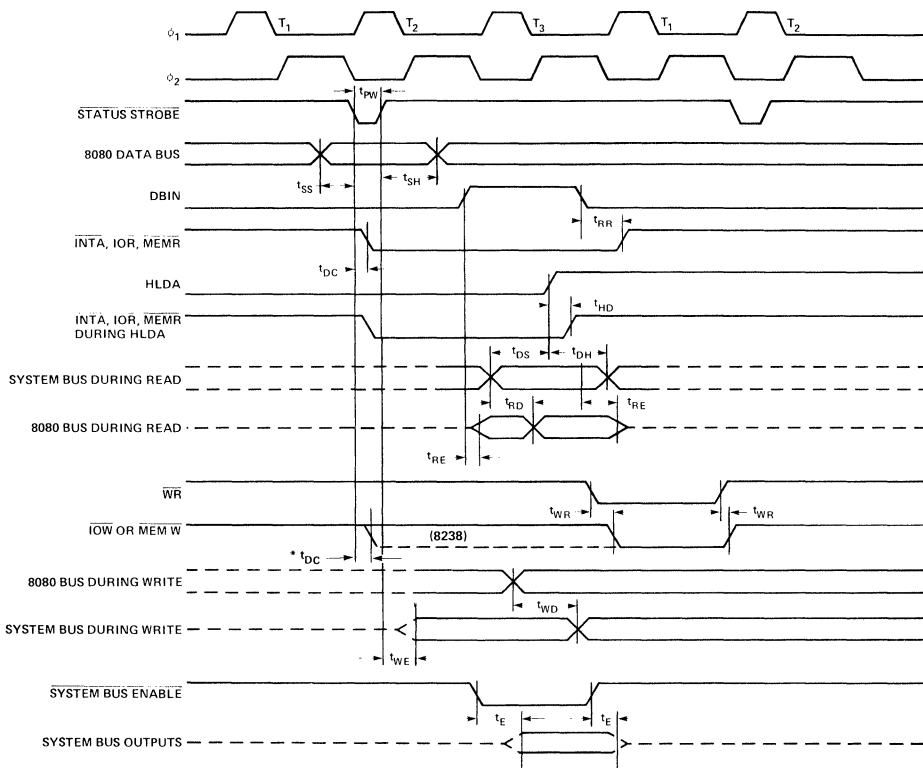
VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*Advanced $\overline{IOW}/\overline{MEMW}$ for M8238 only.

M8080A CPU Interface

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH (1)	MEMORY READ (2)	MEMORY WRITE (3)	STACK READ (4)	STACK WRITE (5)	INPUT READ (6)	OUTPUT WRITE (7)	INTERRUPT ACKNOWLEDGE (8)	HALT ACKNOWLEDGE (9)	INTERRUPT ACKNOWLEDGE WHILE HALT (10)
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

(N) STATUS WORD

CONTROL SIGNALS

- $\overline{INTA}$
- (NONE)
- $\overline{INTA}$
- $\overline{I/O\ W}$
- $\overline{I/O\ R}$
- $\overline{MEM\ W}$
- $\overline{MEM\ R}$
- $\overline{MEM\ W}$
- $\overline{MEM\ R}$
- $\overline{MEM\ R}$

Status Word Chart

intel®

8085
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

- **Single +5V Power Supply**
- **100% Software Compatible with 8080A**
- **1.3 µs Instruction Cycle**
- **On-Chip Clock Generator (with External Crystal or RC Network)**
- **On-Chip System Controller**

- **Four Vectored Interrupts (One is non-Maskable)**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64K Bytes of Memory**

The Intel® 8085 is a new generation, complete 8 bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's: 8085 (CPU), 8156 (RAM) and 8355/8755 (ROM/PROM).

The 8085 incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080, thereby offering a high level of system integration.

The 8085 uses a multiplexed Data Bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8355/8755 memory products allows a direct interface with 8085.

**8085 CPU FUNCTIONAL
BLOCK DIAGRAM**
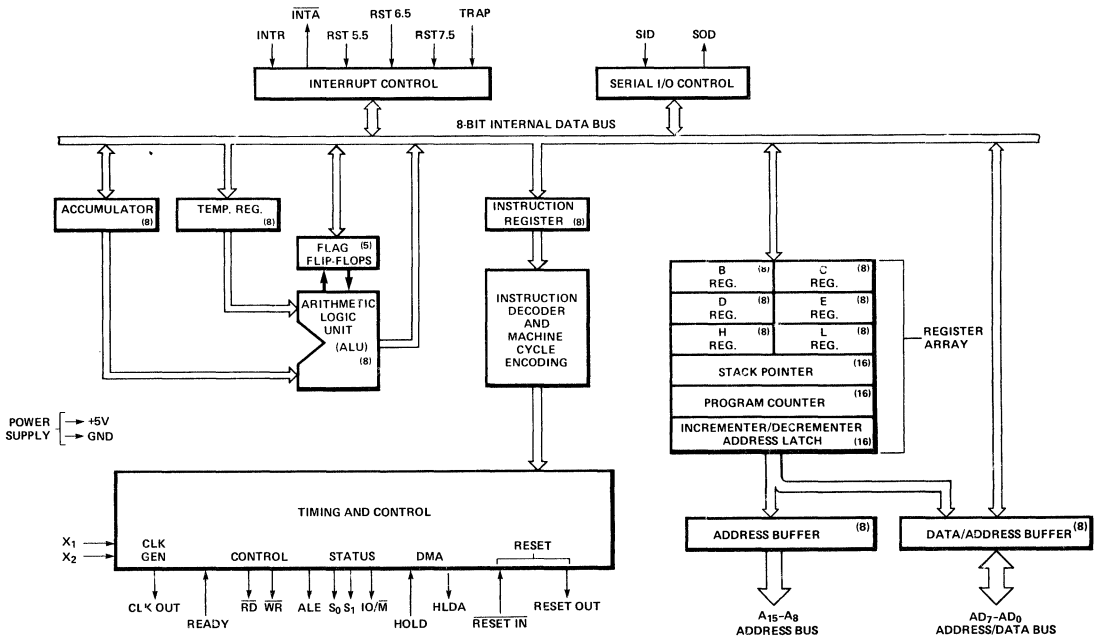
8085 FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

A_8-A_{15} (Output 3-State)

Address Bus; The most significant 8-bits of the memory address or the 8-bits of the I/O address, 3-stated during Hold and Halt modes.

AD_{0-7} (Input/Output 3-state)

Multiplexed Address/Data Bus; Lower 8-bits of the memory address (or I/O address) appear on the bus during the first clock cycle of a machine state. It then becomes the data bus during the second and third clock cycles.

3-stated during Hold and Halt modes.

ALE (Output 3-state)

Address Latch Enable: It occurs during the first clock cycle of a machine state and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. ALE can also be used to strobe the status information. 3-stated during Hold and Halt modes.

S0, S1 (Output)

Data Bus Status. Encoded status of the bus cycle:

S_1	S_0	
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

S_1 can be used as an advanced $R/\overline{W}$ status.

$\overline{RD}$ (Output 3-state)

READ; indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. Tri-stated during Hold and Halt.

$\overline{WR}$ (Output 3-state)

WRITE; indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. Tri-stated during Hold and Halt modes.

READY (Input)

If Ready is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.

HOLD (Input)

HOLD; indicates that another Master is requesting the use of the Address and Data Buses. The CPU, upon receiving the Hold request, will relinquish the use of buses as soon as the completion of the current machine cycle. Internal processing can continue. The processor can regain the buses only after the Hold is removed. When the Hold is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, and ALE lines are tri-stated.

HLDA (Output)

HOLD ACKNOWLEDGE; indicates that the CPU has received the Hold request and that it will relinquish the
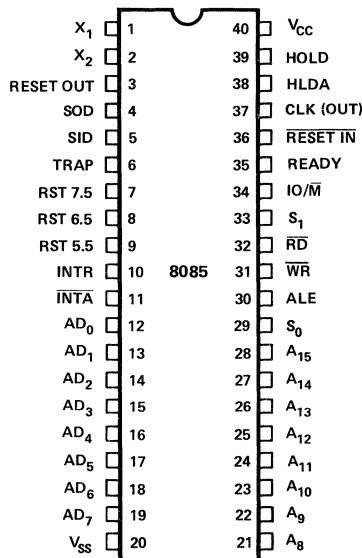
Figure 1. 8085 PINOUT DIAGRAM

buses in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the buses one half clock cycle after HLDA goes low.

INTR (Input)

INTERRUPT REQUEST; is used as a general purpose interrupt. It is sampled only during the last clock cycle of the instruction. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

$\overline{INTA}$ (Output)

INTERRUPT ACKNOWLEDGE; is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.

RST 5.5
RST 6.5 — (Inputs)
RST 7.5

RESTART INTERRUPTS; These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.

RST 7.5 → Highest Priority
RST 6.5
RST 5.5 → Lowest Priority

The priority of these interrupts is ordered as shown above. These interrupts have a higher priority than the INTR.

TRAP (Input)

Trap interrupt is a nonmaskable restart interrupt. It is recognized at the same time as INTR. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.

RESET IN (Input)

Reset sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. None of the other flags or registers (except the instruction register) are affected. The CPU is held in the reset condition as long as Reset is applied.

RESET OUT (Output)

Indicates CPU is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

X_1, X_2 (Input)

Crystal or R/C network connections to set the internal clock generator. X1 can also be an external clock input instead of a crystal.

CLK (Output)

Clock Output for use as a system clock when a crystal or R/C network is used as an input to the CPU.

IO/$\overline{M}$ (Output)

IO/$\overline{M}$ indicates whether the Read/Write is to memory or I/O. Tri-stated during Hold and Halt modes.

SID (Input)

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

SOD (output)

Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

V_{CC}

+5 volt supply.

V_{SS}

Ground Reference.

FUNCTIONAL DESCRIPTION

The 8085 is a complete 8 bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz thus improving on the present 8080's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU, a RAM/IO, and a ROM or PROM/IO chip.

The 8085 uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first cycle the address is sent out. The lower 8-bits are latched into the peripherals by the Address Latch Enable (ALE). During the rest of the machine cycle the Data Bus is used for memory or I/O data.

The 8085 provides $\overline{RD}$, $\overline{WR}$, and IO/$\overline{Memory}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. Hold, Ready, and all Interrupts are synchronized. The 8085 also provides serial input data (SID) and serial output data (SOD) lines for simple serial interface.

In addition to these features, the 8085 has three maskable, restart interrupts and one nonmaskable trap interrupt.

8085 vs. 8080

The 8085 includes the following features on-chip in addition to all of the 8080 functions.

a. Internal clock generator
b. Clock output
c. Fully synchronized Ready
d. Schmitt action on $\overline{RESET\ IN}$
e. RESET OUT pin
f. $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ Bus Control Signals
g. Encoded Status information
h. Multiplexed Address and Data
i. Direct Restarts and nonmaskable Interrupt
j. Serial Input/Output lines.

The internal clock generator requires an external crystal or R-C network. It will oscillate at twice the basic CPU operating frequency. A 50% duty cycle, two phase, nonoverlapping clock is generated from this oscillator internally and one phase of the clock ($\phi2$) is available as an external clock. The 8085 directly provides the external RDY synchronization previously provided by the 8224. The $\overline{RESET\ IN}$ input is provided with a Schmitt action input so that power-on reset only requires a resistor and capacitor. RESET OUT is provided for System RESET.

The 8085 provides $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ signals for Bus control. An $\overline{INTA}$ which was previously provided by the 8228 in 8080 system is also included in 8085.

STATUS INFORMATION

Status information is directly available from the 8085. *ALE serves as a status strobe*. The status is partially encoded, and provides the user with advanced timing of the type of bus transfer being done. IO/$\overline{M}$ cycle status signal is provided directly also. Decoded S_0, S_1 carries the following status information:

	S_1	S_0
HALT	0	0
WRITE	0	1
READ	1	0
FETCH	1	1

S1 can be interpreted as R/$\overline{W}$ in all bus transfers.

In the 8085 the 8 LSB of address are multiplexed with the data instead of status. The ALE line is used as a strobe to enter the lower half of the address into the memory or peripheral address latch. This also frees extra pins for expanded interrupt capability.

INTERRUPT AND SERIAL I/O

The 8085 has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080 INT. Each of three RESTART inputs, 5.5, 6.5, 7.5, has a programmable mask. TRAP is also a RESTART interrupt except it is non-maskable.

The three RESTART interrupts cause the internal execution of RST (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RST independent of the state of the interrupt enable or masks.

Name	RESTART Address (Hex)
TRAP	24_{16}
RST 5.5	$2C_{16}$
RST 6.5	34_{16}
RST 7.5	$3C_{16}$

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip flop which generates the internal interrupt request. The RST 7.5 request flip flop remains set until the request is serviced. Then it is reset automatically. This flip flop may also be reset by using the SIM instruction or by issuing a RESET IN to the 8085. The RST 7.5 internal flip flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and RESET IN.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP - highest priority, RST 7.5, RST 6.5, RST 5.5, INTR - lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt a RST 7.5 routine if the interrupts were re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic errors such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and
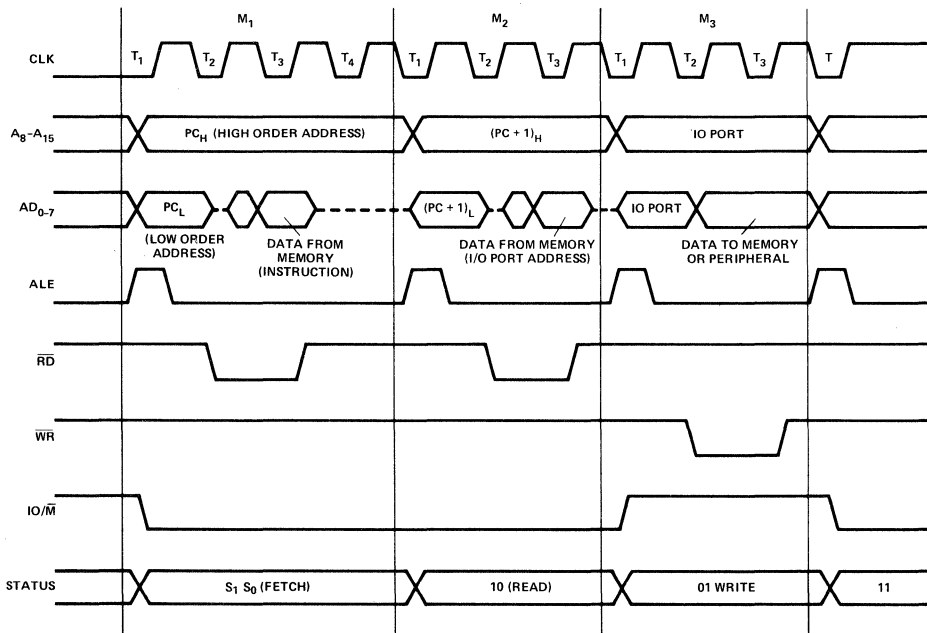
FIGURE 2. 8085 BASIC SYSTEM TIMING.

remain high to be acknowledged, but will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches.

The following diagram illustrates the TRAP interrupt request circuitry within the 8085.
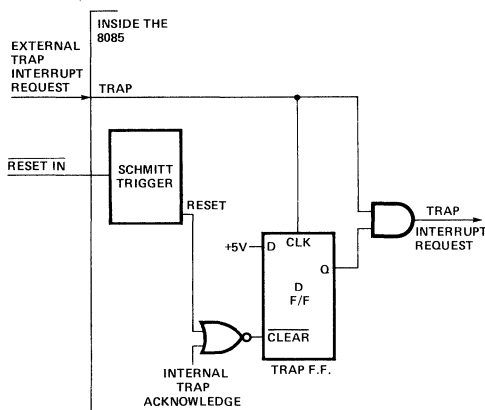
Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

Since a TRAP interrupt can occur and disable the other interrupts whether they were previously enabled or not, it is not possible to restore the previous interrupt enable status following a TRAP.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

BASIC SYSTEM TIMING

The 8085 has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 2 shows an instruction fetch, memory read and I/O write cycle (OUT). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085 can be used with slow memory. Hold causes the CPU to relinguish the bus when it is through with it by floating the Address and Data Buses.

SYSTEM INTERFACE

8085 family includes memory components, which are directly compatible to the 8085 CPU. For example, a system consisting of the three chips, 8085, 8156, and 8355 will have the following features:

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 3.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 4 shows the system configuration of Memory Mapped I/O using 8085.

The 8085 CPU can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8212 (8-bit latch) as shown in Figure 5.
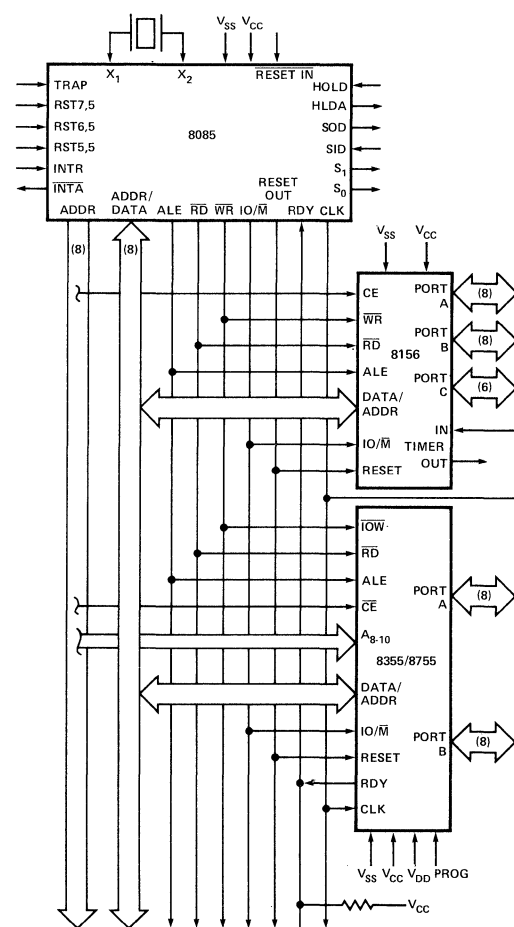
FIGURE 3. 8085 MINIMUM SYSTEM (STANDARD I/O TECHNIQUE)
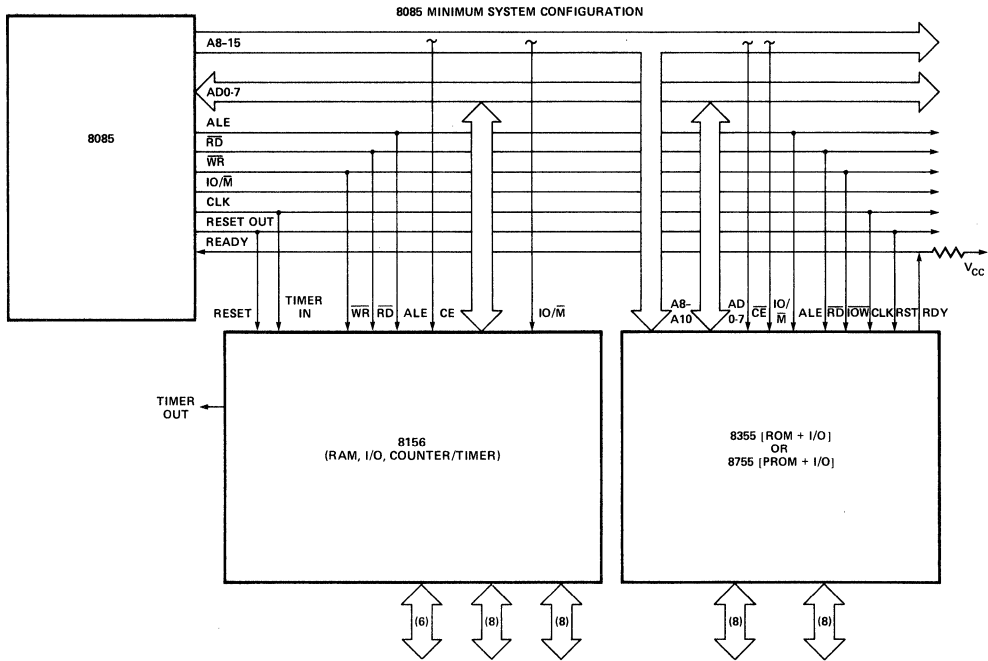
FIGURE 4. MCS-85™ MINIMUM SYSTEM (MEMORY MAPPED I/O)
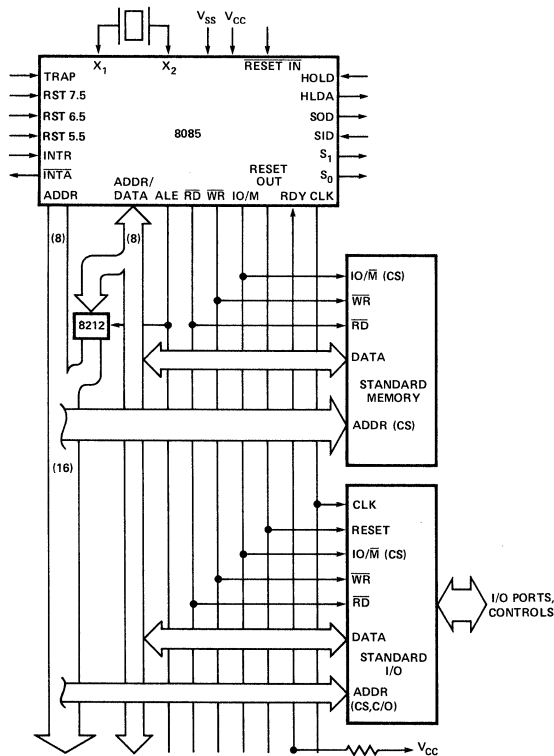
FIGURE 5. MCS-85™ SYSTEM (USING STANDARD MEMORIES)

DRIVING THE X_1 AND X_2 INPUTS

The user may drive the X_1 and X_2 inputs of the 8085 with a crystal, an external clock source or an RC network as shown below:

**1-6 MHz
INPUT FREQUENCY**

**≈ 3 MHz
INPUT FREQUENCY**
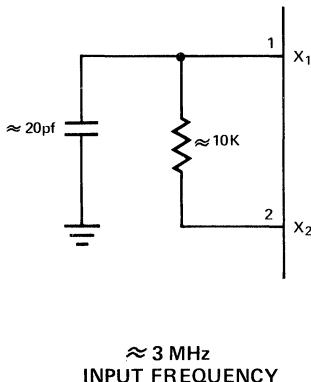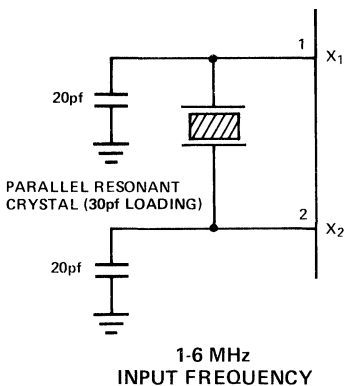
RC Mode causes a large drift in clock frequency because of the variation in on-chip timing generation parameters. Use of RC Mode should be limited to an application, which can tolerate a wide frequency variation.

**1-6 MHz
INPUT FREQUENCY**
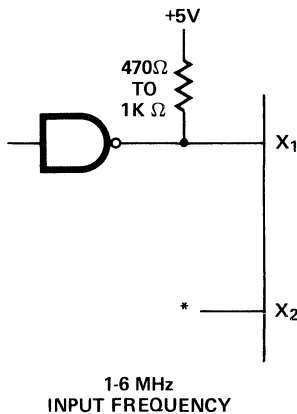
**(DUTY CYCLE AT 6MHz: 25 ~ 50%)
*WITH AN EXTERNAL CLOCK SOURCE
X_2 SHOULD BE LEFT FLOATING.**

**~6 MHz
INPUT FREQUENCY**
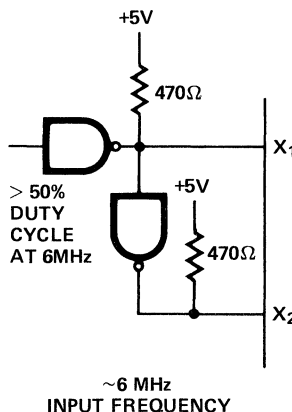
This circuit may be used when the clock input has > 50% duty cycle at 6MHz.

FIGURE 6. DRIVING THE CLOCK INPUTS (X1 AND X2) OF 8085

GENERATING 8085 WAIT STATE

The following circuit may be used to insert one WAIT state in each 8085 machine cycle.

The D flip flops should be chosen such that
- CLK is rising edge triggered
- CLEAR is low-level active.
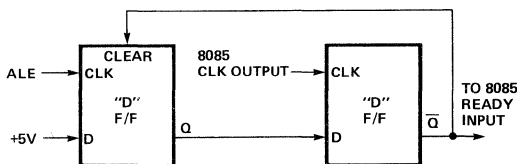
FIGURE 7. GENERATION OF A WAIT STATE FOR 8085 CPU

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . –65°C to +150°C
Voltage on Any Pin
   With Respect to Ground . . . . -0.3 to +7V
Power Dissipation . . . . 1.5 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	–0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –400µA
I_{CC}	Power Supply Current		170	mA	
I_{IL}	Input Leakage		±10	µA	V_{in} = V_{CC}
I_{LO}	Output Leakage		±10	µA	0.45V ≤ V_{out} ≤ V_{CC}
V_{ILR}	Input Low Level, RESET	–0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC} +0.5	V	
V_{HY}	Hysteresis, RESET	0.25		V	

Bus Timing Specification as a T_{CYC} Dependent

t_{AL}	—	(1/2) T – 50	MIN
t_{LA}	—	(1/2) T – 60	MIN
t_{LL}	—	(1/2) T – 40	MIN
t_{LCK}	—	(1/2) T – 60	MIN
t_{LC}	—	(1/2) T – 30	MIN
t_{AD}	—	(5/2 + N) T – 225	MAX
t_{RD}	—	(3/2 + N) T – 200	MAX
t_{RAE}	—	(1/2) T – 60	MIN
t_{CA}	—	(1/2) T – 40	MIN
t_{DW}	—	(3/2 + N) T – 60	MIN
t_{WD}	—	(1/2) T – 80	MIN
t_{CC}	—	(3/2 + N) T – 80	MIN
t_{CL}	—	(1/2) T – 110	MIN
t_{ARY}	—	(3/2) T – 260	MAX
t_{HACK}	—	(1/2) T – 50	MIN
t_{HABF}	—	(1/2) T + 30	MAX
t_{HABE}	—	(1/2) T + 30	MAX
t_{AC}	—	(2/2) T – 50	MIN
t_1	—	(1/2) T – 80	MIN
t_2	—	(1/2) T – 40	MIN
t_{RV}	—	(3/2) T – 80	MIN
t_{INS}	—	(1/2) T + 200	MIN

NOTE: N is equal to the total WAIT states.

      T = t_{CYC}.

A.C. CHARACTERISTICS $(T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$; $V_{SS} = 0V)$

Symbol	Parameter	Min.	Max.	Units	Test Conditions
T_{CYC}	CLK Cycle Period	320	2000	ns	See notes 1, 2, 3, 4, 5
t_1	CLK Low Time	80		ns	
t_2	CLK High Time	120		ns	
t_r, t_f	CLK Rise and Fall Time		30	ns	
t_{AL}	Address Valid Before Trailing Edge of ALE	110		ns	
t_{LA}	Address Hold Time After ALE	100		ns	
t_{LL}	ALE Width	120		ns	
t_{LCK}	ALE Low During CLK High	100		ns	
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		ns	
t_{AFR}	Address Float After Leading Edge of READ ($\overline{INTA}$)		0	ns	
t_{AD}	Valid Address to Valid Data In		575	ns	
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		280	ns	
t_{RDH}	Data Hold Time After $\overline{READ}$ ($\overline{INTA}$)	0		ns	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	120		ns	
t_{CA}	Address (A8–A15) Valid After Control	120		ns	$T_{CYC} = 320ns$;
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		ns	$C_L = 150$ pF
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	80		ns	
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	400		ns	
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		ns	
t_{ARY}	READY Valid From Address Valid		220	ns	
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		ns	
t_{RYH}	READY Hold Time	0		ns	
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		ns	
t_{HABF}	Bus Float After HLDA		190	ns	
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		ns	
t_{AC}	Address Valid to Leading Edge of Control	270		ns	
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		ns	
t_{HDH}	HOLD Hold Time	0		ns	
t_{INS}	INTR Setup Time to Leading Edge of CLK (M1, T1 only). Also RST and TRAP	360		ns	
t_{INH}	INTR Hold Time	0		ns	

NOTES:
1. A8-15 Address Specs apply to $IO/\overline{M}$, S0 and S1.
2. For all output timing where $C_L \neq 150pf$ use the following correction factors:
   $25pf \leqslant C_L < 150pf$: $-.10$ ns/pf
   $150pf < C_L \leqslant 300pf$: $+.30$ ns/pf
3. Output timings are measured with purely capacitive load.
4. All timings are measured at output voltage $V_L = .8V$, $V_H = 2.0V$, and 1.5V with 20ns rise and fall time on inputs.
5. To calculate timing specifications at other values of T_{CYC} use the table in Table 2.
6. L.E. = Leading Edge   T.E. = Trailing Edge

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

FIGURE 8. CLOCK TIMING WAVEFORM

READ OPERATION

WRITE OPERATION

FIGURE 9. 8085 BUS TIMING

HOLD OPERATION

FIGURE 10. 8085 HOLD TIMING

*IO/M̄ IS ALSO FLOATING DURING THIS TIME

FIGURE 11. 8085 INTERRUPT AND HOLD TIMING
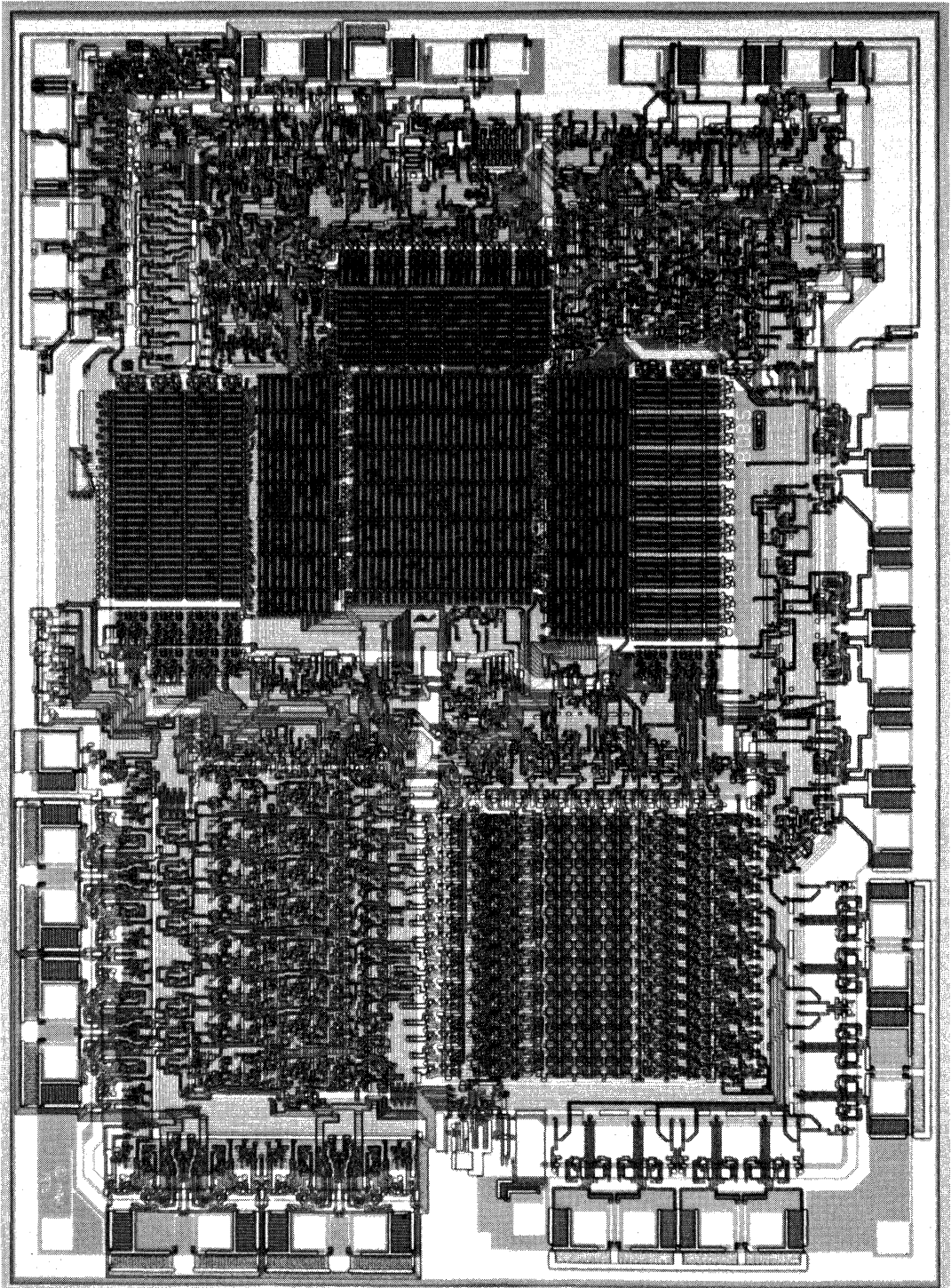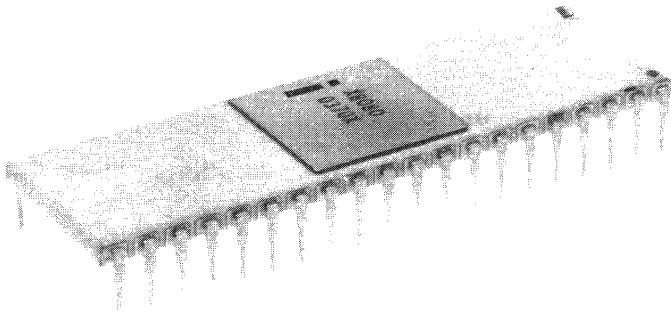
EPROMs and ROMs

EPROMs and ROMs

intel®

8708
8192 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

1024x8 Organization

- **Fast Programming —**
  Typ. 100 sec. For All 8K Bits
- **Low Power During Programming**
- **Access Time — 450 ns**
- **Standard Power Supplies —**
  +12V, ±5V

- **Static — No Clocks Required**
- **Inputs and Outputs TTL**
  Compatible During Both Read
  and Program Modes
- **Three-State Output — OR-Tie**
  Capability

The Intel® 8708 is a high speed 8192 bit erasable and electrically reprogrammable ROM (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

The 8708 is packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

A pin for pin mask programmed ROM, the Intel® 8308, is available for large volume production runs of systems initially using the 8708.

The 8708 is fabricated with the time proven N-channel silicon gate technology.

PIN CONFIGURATION

Pin			Pin
A_7	1	24	V_{CC}
A_6	2	23	A_8
A_5	3	22	A_9
A_4	4	21	V_{BB}
A_3	5	20	$\overline{CS}$/WE
A_2	6	19	V_{DD}
A_1	7	18	PROGRAM
A_0	8	17	O_8
O_1	9	16	O_7
O_2	10	15	O_6
O_3	11	14	O_5
V_{SS}	12	13	O_4

(8708)

BLOCK DIAGRAM

DATA OUTPUT $O_1 \cdot O_8$

$\overline{CS}$/WE → CHIP SELECT LOGIC

A_0 A_9 ADDRESS INPUTS

Y DECODER

X DECODER

OUTPUT BUFFERS

Y GATING

64 X 128 ROM ARRAY
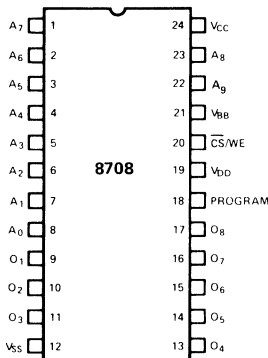
PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT
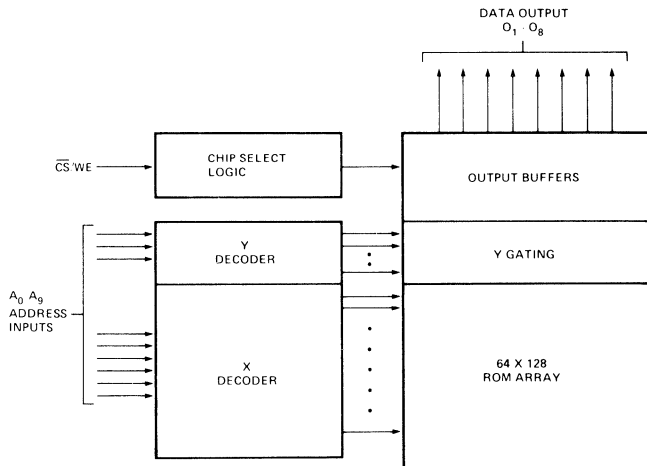
PIN CONFIGURATION DURING READ OR PROGRAM

MODE	PIN NUMBER						
	9-11, 13-17	12	18	19	20	21	24
READ	D_{OUT}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
PROGRAM	D_{IN}	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

PROGRAMMING

The programming specifications are identical to those of the 2708. (See ROM and PROM Programming Instructions, page 6-74).

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . –25°C to +85°C
Storage Temperature . . . .–65°C to +125°C
V_{DD} With Respect to V_{BB} . . . . +20V to –0.3V
V_{CC} and V_{SS} With Respect to V_{BB} . . . . . . +15V to –0.3V
All Input or Output Voltages With
    Respect to V_{BB} During Read . . . . +15V to –0.3V
$\overline{CS}$/WE Input With Respect to V_{BB}
    During Programming . . . . +20V to –0.3V
Program Input With Respect to V_{BB} . . . . . +35V to –0 3V
Power Dissipation 1.5W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to 70°C, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = –5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Sink Current		1	10	µA	$V_{IN} = 5.25$ V or $V_{IN} = V_{IL}$
I_{LO}	Output Leakage Current		1	10	µA	$V_{OUT} = 5.25V$, $\overline{CS}$/WE = 5V
I_{DD} [2]	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC} [2]	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB} [2]	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; $T_A = 0°C$
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 1.6mA$
V_{OH1}	Output High Voltage	3.7			V	$I_{OH} = –100µA$
V_{OH2}	Output High Voltage	2.4			V	$I_{OH} = –1mA$
P_D	Power Dissipation			800	mW	$T_A = 70°C$

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. The total power dissipation of the 8708 is specified at 800 mW. It is not calculable by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

TYPICAL D.C. CHARACTERISTICS
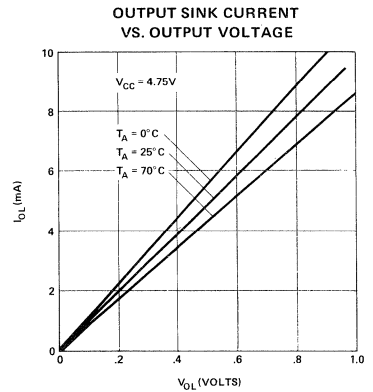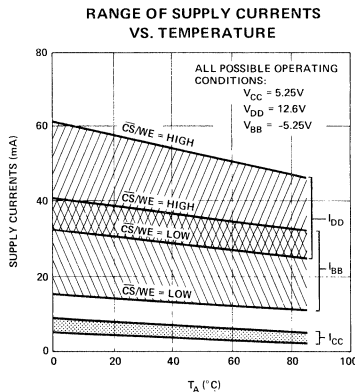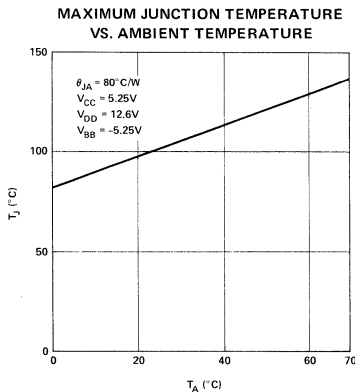
MAXIMUM JUNCTION TEMPERATURE VS. AMBIENT TEMPERATURE

RANGE OF SUPPLY CURRENTS VS. TEMPERATURE

OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
$t_{\overline{CO}}$	Chip Select to Output Delay		60	120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

CAPACITANCE $T_A = 25°C$, f = 1MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note . This parameter is periodically sampled and not 100% tested.

A.C. TEST CONDITIONS

Output Load: 1 TTL gate and $C_L = 100pF$
Input Rise and Fall Times: ≤20ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs
Input Pulse Levels: 0.65V to 3.0V

WAVEFORMS
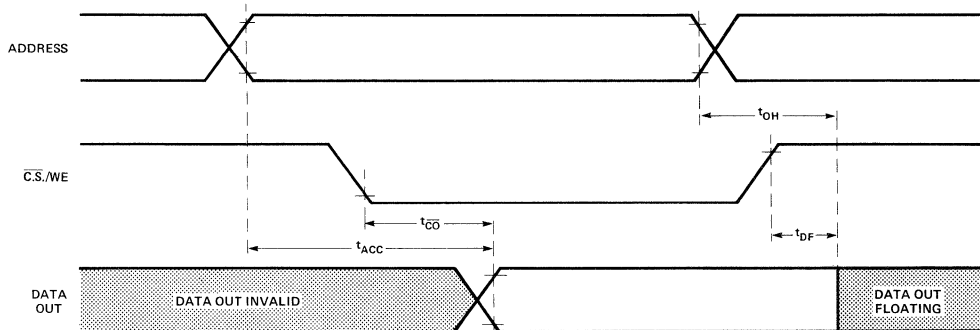
ERASURE CHARACTERISTICS

The erasure characteristics of the 8708 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level flourescent lighting could erase the typical 8708 in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8708 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8708 window to prevent unintentional erasure.

The recommended erasure procedure (see page 3-55) for the 8708 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000µW/cm² power rating. The 8708 should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

intel®

2716
16K (2K×8) UV ERASABLE PROM

- Single +5V Power Supply

- Simple Programming Requirements
  Single Location Programming
  Programs With One 50ms Pulse

- Low Power Dissipation
  525mW Max. Active Power
  132mW Max. Standby Power

- Pin Compatible To Intel 2316E ROM

- Fast Access Time: 450ns Max.

- Inputs and Outputs TTL
  Compatible During Read
  And Program

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static power down mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. For production quantities, the 2716 user can convert rapidly to Intel's new pin-for-pin compatible 16K ROM, the 2316E.

Since the 450-nsec 2716 operates from a single 5-volt supply, it is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8048. The 2716 is also the first EPROM with a static power down mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Now, it is possible to program on-board, in the system, in the field. Program any location at any time — either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION

```
      A7 ⊏ 1      24 ⊐ VCC
      A6 ⊏ 2      23 ⊐ A8
      A5 ⊏ 3      22 ⊐ A9
      A4 ⊏ 4      21 ⊐ VPP
      A3 ⊏ 5      20 ⊐ CS
      A2 ⊏ 6      19 ⊐ A10
      A1 ⊏ 7      18 ⊐ PD/PGM
      A0 ⊏ 8      17 ⊐ O7
      O0 ⊏ 9      16 ⊐ O6
      O1 ⊏ 10     15 ⊐ O5
      O2 ⊏ 11     14 ⊐ O4
     GND ⊏ 12     13 ⊐ O3
```
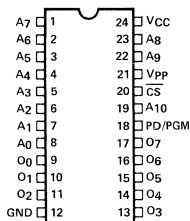
PIN NAMES

A_0–A_{10}	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O_0–O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM
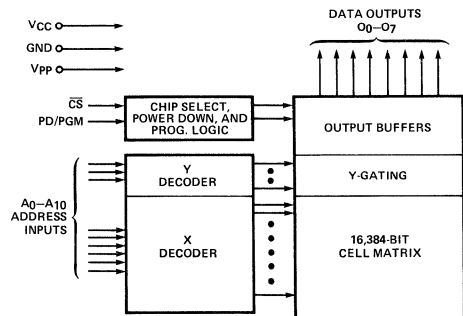
PRELIMINARY

PROGRAMMING

The programming specifications are described in the PROM/ROM Programming Instructions on page 6-74.

Absolute Maximum Ratings*

Temperature Under Bias . . . . –10°C to +80°C
Storage Temperature . . . . –65°C to +125°C
All Input or Output Voltages with
   Respect to Ground . . . . +6V to –0.3V
V_{PP} Supply Voltage with Respect
   to Ground . . . . +28V to –0.3V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC}^{[1,2]} = +5V \pm 5\%$, $V_{PP}^{[2]} = V_{CC} \pm 0.6V^{[3]}$

| Symbol | Parameter | Limits | | | Unit | Conditions |
		Min.	Typ.[4]	Max.		
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.25V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.25V$
$I_{PP1}^{[2]}$	V_{PP} Current			5	mA	$V_{PP} = 5.85V$
$I_{CC1}^{[2]}$	V_{CC} Current (Standby)		10	25	mA	PD/PGM = V_{IH}, $\overline{CS} = V_{IL}$
$I_{CC2}^{[2]}$	V_{CC} Current (Active)		57	100	mA	$\overline{CS}$ = PD/PGM = V_{IL}
V_{IL}	Input Low Voltage	–0.1		0.8	V	
V_{IH}	Input High Voltage	2.2		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400 \mu A$

NOTES:
1. V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
2. Vpp may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. The tolerance of 0.6V allows the use of a driver circuit for switching the Vpp supply pin from V_{CC} in read to 25V for programming.
4. Typical values are for $T_A = 25°C$ and nominal supply voltages.
5. This parameter is only sampled and is not 100% tested.
6. t_{ACC2} is referenced to PD/PGM or the addresses, whichever occurs last.

Typical Characteristics

ICC CURRENT
vs.
TEMPERATURE
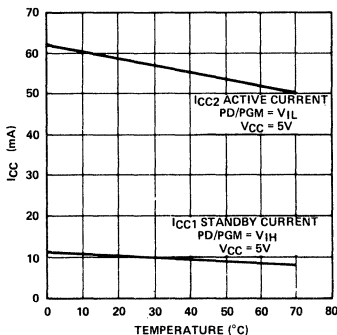
ACCESS TIME
vs.
CAPACITANCE

ACCESS TIME
vs.
TEMPERATURE

PRELIMINARY
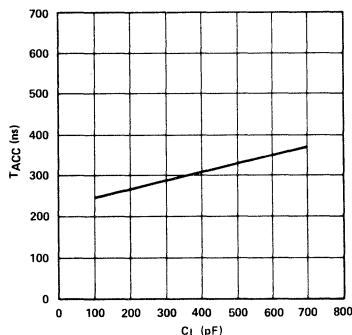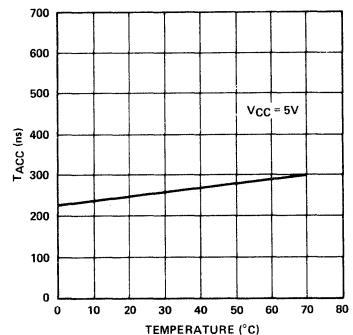
A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC}[1] = +5V \pm 5\%$, $V_{PP}[2] = V_{CC} \pm 0.6V[3]$

Symbol	Parameter	Min.	Typ.[4]	Max.	Unit	Test Conditions
t_{ACC1}	Address to Output Delay		250	450	ns	PD/PGM = $\overline{CS}$ = V_{IL}
t_{ACC2}	PD/PGM to Output Delay		280	450	ns	$\overline{CS}$ = V_{IL}
t_{CO}	Chip Select to Output Delay			120	ns	PD/PGM = V_{IL}
t_{PF}	PD/PGM to Output Float	0		100	ns	$\overline{CS}$ = V_{IL}
t_{DF}	Chip Deselect to Output Float	0		100	ns	PD/PGM = V_{IL}
t_{OH}	Address to Output Hold	0			ns	PD/PGM = $\overline{CS}$ = V_{IL}

Capacitance[5] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

NOTE: Please refer to page 2 for notes.

A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
  Inputs   1V and 2V
  Outputs   0.8V and 2V

WAVEFORMS

A. Read Mode
PD/PGM = V_{IL}

B. Standby Mode
$\overline{CS}$ = V_{IL}

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.
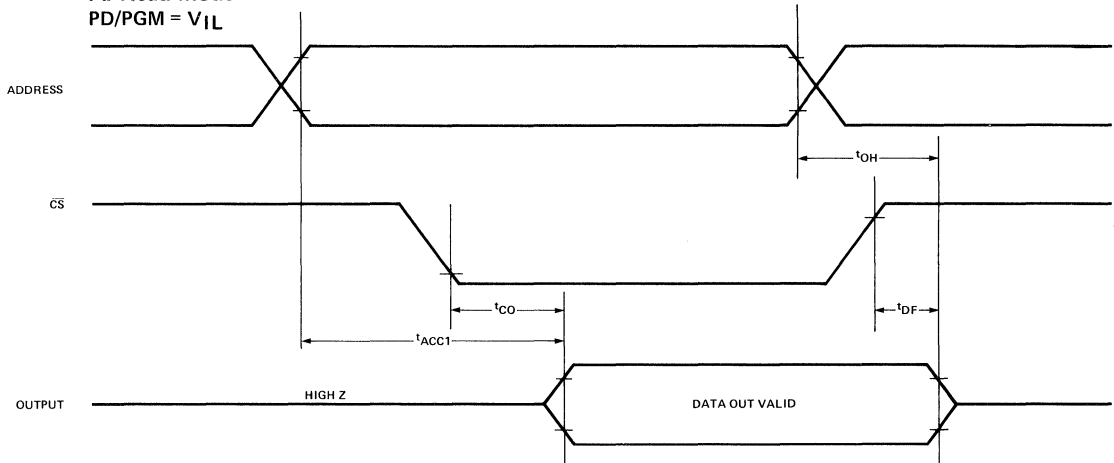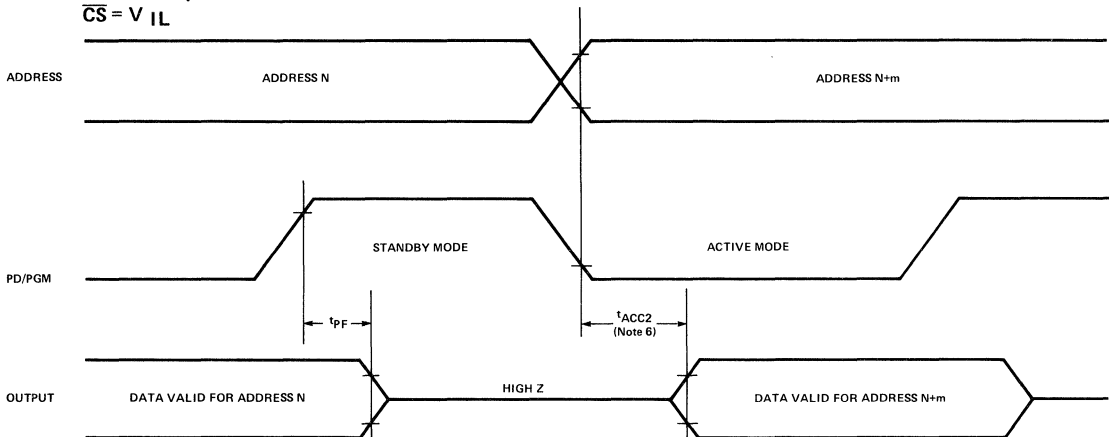
ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure (see page 3-55) for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The six modes of operation of the 2716 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other three modes.

TABLE I. MODE SELECTION

PINS / MODE	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

Data is available at the outputs in the read mode. Data is available 450 ns (t_{ACC}) from stable addresses with $\overline{CS}$ low or 120 ns (t_{CO}) from $\overline{CS}$ with addresses stable.

DESELECT MODE

The outputs of two or more 2716s may be OR-tied together on the same data bus. Only one 2716 should have its outputs selected ($\overline{CS}$ low) to prevent data bus contention between 2716s in this configuration. The outputs of the other 2716s should be deselected with the $\overline{CS}$ input at a high TTL level.

POWER DOWN MODE

The 2716 has a power down mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. Power down is achieved by applying a TTL high signal to the PD/PGM input. In power down the outputs are in a high impedance state, independent of the $\overline{CS}$ input.

PROGRAMMING

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{CS}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the addresses and data are stable, a 50 msec, active high, TTL program pulse is applied to the PD/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the PD/PGM input.

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the PD/PGM input programs the paralleled 2716s.

PROGRAM INHIBIT

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for PD/PGM, all like inputs (including $\overline{CS}$) of the parallel 2716s may be common. A TTL level program pulse applied to a 2716's PD/PGM input with V_{PP} at 25V will program that 2716. A low level PD/PGM input inhibits the other 2716s from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed wth V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

intel®

8308
8192 BIT STATIC MOS READ ONLY MEMORY

- **Fast Access Time: 450 ns**
- **Standard Power Supplies: +12V, ±5V**
- **TTL Compatible: All Inputs and Outputs**
- **Programmable Chip Select Input for Easy Memory Expansion**

- **Three-State Output: OR-Tie Capability**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Pin Compatible to 8708 PROM**

The Intel® 8308 is a 8192 bit static MOS read only memory organized as 1024 words by 8-bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are TTL compatible. The chip select input (CS2/$\overline{CS2}$) is programmable. An active high or low level chip select input can be defined by the designer and the desired chip select logic level is fixed at Intel during the masking process. The programmable chip select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion. The pin compatible UV erasable 8708 PROM is available for initial system prototyping.

The 8308 read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

PIN CONFIGURATION

A_7	1	24	V_{CC}
A_6	2	23	A_8
A_5	3	22	A_9
A_4	4	21	V_{BB}
A_3	5	20	$\overline{CS1}$
A_2	6	19	V_{DD}
A_1	7	18	CS2/$\overline{CS2}$[1]
A_0	8	17	O_8
O_1	9	16	O_7
O_2	10	15	O_6
O_3	11	14	O_5
V_{SS}	12	13	O_4

8308

BLOCK DIAGRAM

DATA OUTPUT
$O_1 \cdot O_8$

$\overline{CS1}$ → CHIP SELECT LOGIC
CS2/$\overline{CS2}$ →

OUTPUT BUFFERS

A_9, A_8, A_7, A_6 → Y DECODER

Y GATING

$A_0 \cdot A_9$ ADDRESS INPUTS

A_5, A_4, A_3, A_2, A_1, A_0 → X DECODER

64 X 128 ROM ARRAY
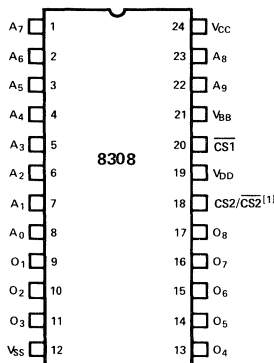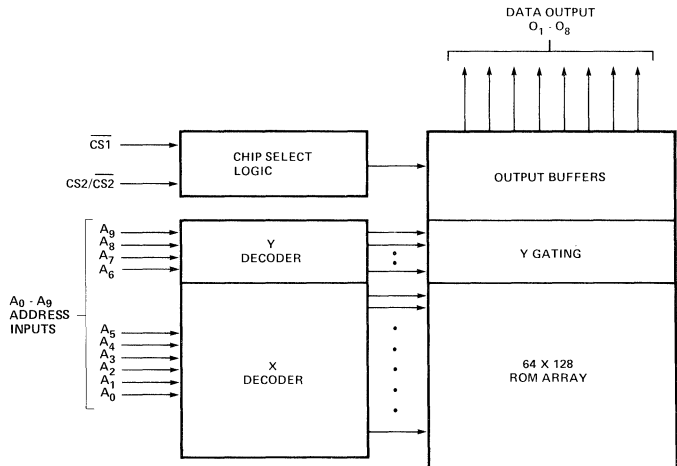
PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS1}$	CHIP SELECT INPUT
CS2/$\overline{CS2}$[1]	PROGRAMMABLE CHIP SELECT INPUT

NOTE 1. The CS2/$\overline{CS2}$ LOGIC LEVELS MUST BE SPECIFIED BY THE USER AS EITHER A LOGIC 1 (V_{IH}) OR LOGIC 0 (V_{IL}). A LOGIC 0 SHOULD BE SPECIFIED IN ORDER TO BE COMPATIBLE WITH THE 8708.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . . –25°C to +85°C
Storage Temperature . . . . –65°C to +150°C
Voltage On Any Pin With Respect
    To V_{BB} . . . . –0.3V to 20V
Power Dissipation . . . . 1.0 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PROGRAMMING

The programming specifications are described in the PROM/ROM Programming Instructions on page 6-74.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±5%; V_{DD} = 12V ±5%, V_{BB} = –5V ±5%, V_{SS} = 0V Unless Otherwise Specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins Except $\overline{CS}_1$)			±10	μA	V_{IN} = 0 to 5.25V
I_{LCL}	Input Load Current on $\overline{CS}_1$			–1.6	mA	V_{IN} = 0.45V
I_{LPC}	Input Peak Load Current on $\overline{CS}_1$			–4	mA	V_{IN} = 0.8V to 3.3V
I_{LKC}	Input Leakage Current on $\overline{CS}_1$			10	μA	V_{IN} = 3.3V to 5.25V
I_{LO}	Output Leakage Current			10	μA	Chip Deselected
V_{IL}	Input "Low" Voltage	V_{SS}–1		0.8V	V	
V_{IH}	Input "High" Voltage	3.3		V_{CC}+1.0	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2mA
V_{OH1}	Output "High" Voltage	2.4			V	I_{OH} = –4mA
V_{OH2}	Output "High" Voltage	3.7			V	I_{OH} = –1mA
I_{CC}	Power Supply Current V_{CC}		10	15	mA	
I_{DD}	Power Supply Current V_{DD}		32	60	mA	
I_{BB}	Power Supply Current V_{BB}		10μA	1	mA	
P_D	Power Dissipation		460	840	mW	

NOTE 1: Typical values for T_A = 25°C and nominal supply voltage

D.C. OUTPUT CHARACTERISTICS

D.C. OUTPUT CHARACTERISTICS

A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$; $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Specified.

Symbol	Parameter	Limits[2]			Unit
		Min.	Typ.	Max.	
t_{ACC}	Address to Output Delay Time		200	450	ns
t_{CO1}	Chip Select 1 to Output Delay Time		85	160	ns
t_{CO2}	Chip Select 2 to Output Delay Time		125	220	ns
t_{DF}	Chip Deselect to Output Data Float Time		125	220	ns

NOTE 2: Refer to conditions of Test for A.C. Characteristics. Add 50 nanoseconds (worst case) to specified values at
$V_{OH} = 3.7V$ @ $I_{OH} = -1mA$, $C_L = 100pF$.

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . . 1 TTL Gate, and $C_{LOAD} = 100pF$
Input Pulse Levels . . . . .65V to 3.3V
Input Pulse Rise and Fall Times . . . . 20 nsec
Timing Measurement Reference Level
. . . . 2.4V V_{IH}, V_{OH}; 0.8V V_{IL}, V_{OL}

CAPACITANCE $T_A = 25°C$, f = 1 MHz, $V_{BB} = -5V$, V_{DD}, V_{CC} and all other pins tied to V_{SS}.

Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	Input Capacitance		6pF
C_{OUT}	Output Capacitance		12pF
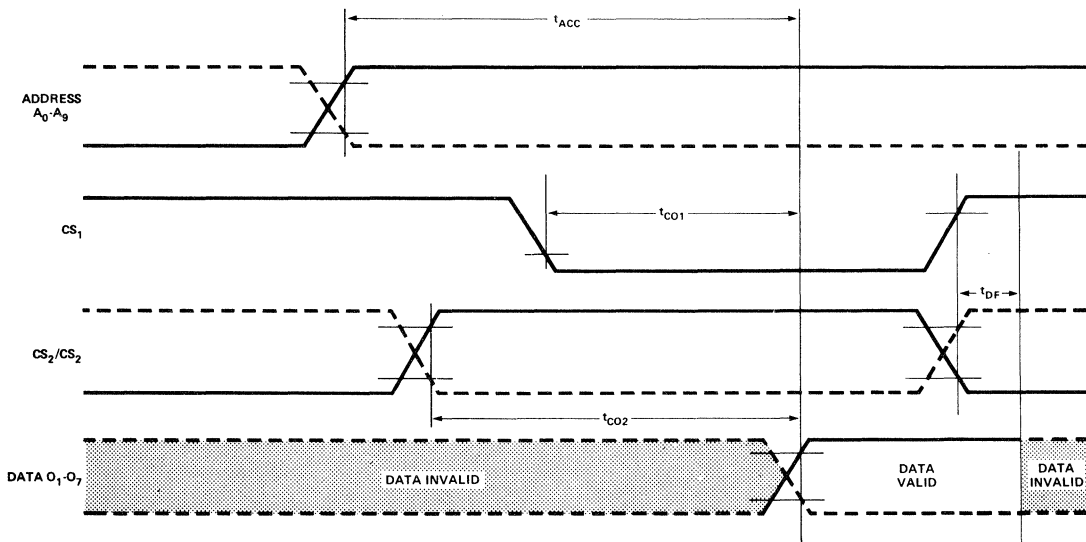
TYPICAL CHARACTERISTICS (Nominal supply voltages unless otherwise noted.)

I_{DD} VS. TEMPERATURE
(NORMALIZED)
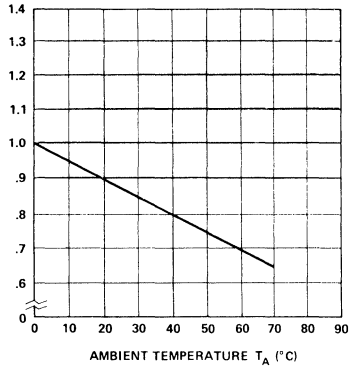
Δ OUTPUT CAPACITANCE
VS. Δ OUTPUT DELAY
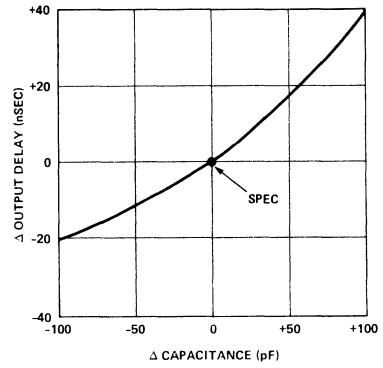
$\overline{CS}_1$ INPUT
CHARACTERISTICS
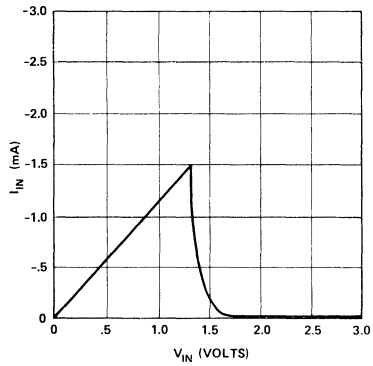
T_{ACC} VS. TEMPERATURE
(NORMALIZED)

intel®
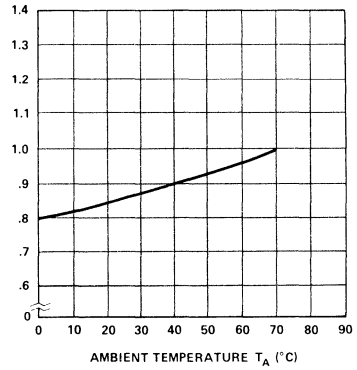
8316A
16,384 BIT STATIC MOS READ ONLY MEMORY
Organization—2048 Words x 8 Bits
Access Time-850 ns max

- ■ **Single +5 Volts Power Supply Voltage**
- ■ **Directly TTL Compatible — All Inputs and Outputs**
- ■ **Low Power Dissipation of 31.4 μW/Bit Maximum**
- ■ **Three Programmable Chip Select Inputs for Easy Memory Expansion**

- ■ **Three-State Output — OR-Tie Capability**
- ■ **Fully Decoded — On Chip Address Decode**
- ■ **Inputs Protected — All Inputs Have Protection Against Static Charge**

The Intel® 8316A is a 16,384-bit static MOS read only memory organized as 2048 words by 8 bits. This ROM is designed for microcomputer memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and the desired chip select code is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitate easy memory expansion.

The 8316A read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible.

PIN CONFIGURATION
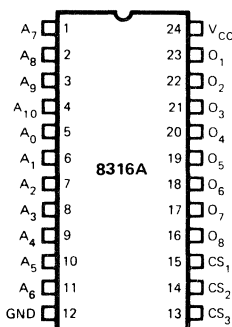
BLOCK DIAGRAM
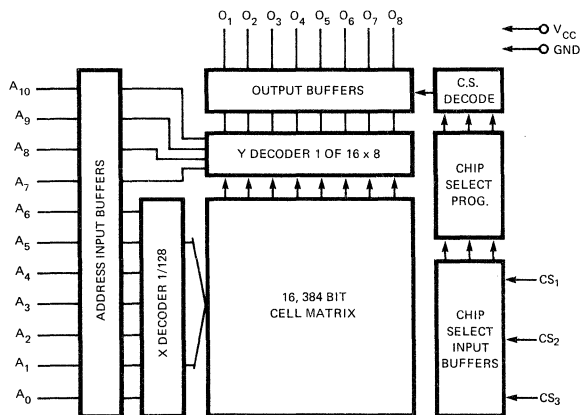
PIN NAMES

A_0- A_{10}	ADDRESS INPUTS
O_1- O_8	DATA OUTPUTS
CS_1- CS_3	PROGRAMMABLE CHIP SELECT INPUTS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... $-10°C$ to $80°C$
Storage Temperature .... $-65°C$ to $+150°C$
Voltage on Any Pin
   With Respect to Ground .... $-0.5V$ to $+7V$
Power Dissipation 1.0W

PROGRAMMING: *The programming specifications are in the ROM and PROM Programming Instructions (see page 6-74).*

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.[1]	MAX.		
I_{LI}	Input Load Current (All Input Pins)		1	10	μA	$V_{IN} = 0$ to 5.25V
I_{LOH}	Output Leakage Current			10	μA	$CS = 2.2V$, $V_{OUT} = 4.0V$
I_{LOL}	Output Leakage Current			-20	μA	$CS = 2.2V$, $V_{OUT} = 0.45V$
I_{CC}	Power Supply Current		40	98	mA	All inputs 5.25V Data Out Open
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		$V_{CC}+1.0V$	V	
V_{OL}	Output "Low" Voltage			0.45	V	$I_{OL} = 2.0$ mA
V_{OH}	Output "High" Voltage	2.2			V	$I_{OH} = -100 \mu A$

(1) Typical values for $T_A = 25°C$ and nominal supply voltage.

TYPICAL D.C. CHARACTERISTICS

V_{IN} LIMITS VS. TEMPERATURE
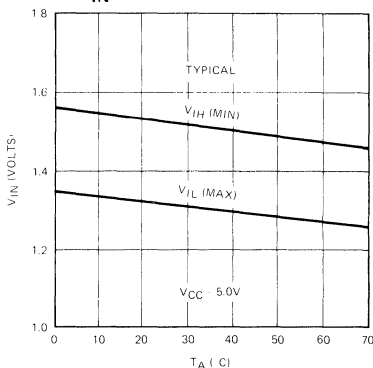
STATIC I_{CC} VS. AMBIENT TEMPERATURE WORST CASE
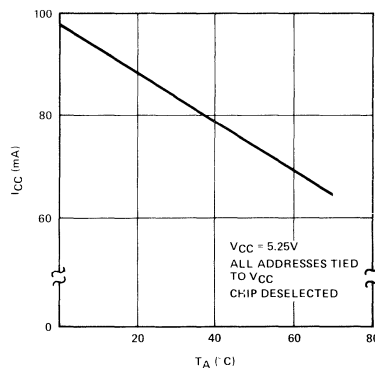
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE
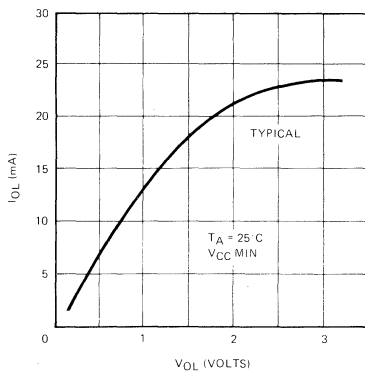
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE
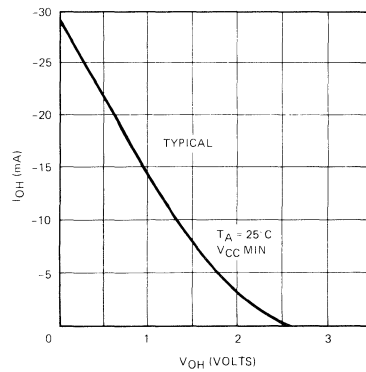
A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.[1]	MAX.	
t_A	Address to Output Delay Time		400	850	nS
t_{CO}	Chip Select to Output Enable Delay Time			300	nS
t_{DF}	Chip Deselect to Output Data Float Delay Time	0		300	nS

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . 1 TTL Gate, and C_{LOAD} = 100 pF
Input Pulse Levels . . . . 0.8 to 2.0V
Input Pulse Rise and Fall Times . (10% to 90%) 20 nS
Timing Measurement Reference Level
    Input 1.5V
    Output . . . . 0.45V to 2.2V

CAPACITANCE [2] T_A = 25°C, f = 1 MHz

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C_{IN}	All Pins Except Pin Under Test Tied to AC Ground	4 pF	10 pF
C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground	8 pF	15 pF

(2) This parameter is periodically sampled and is not 100% tested.

A.C. WAVEFORMS
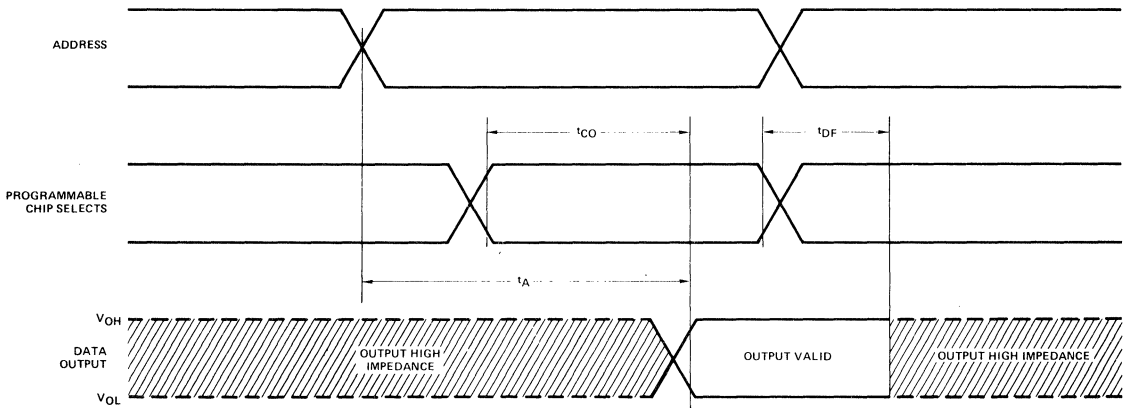
TYPICAL A.C. CHARACTERISTICS
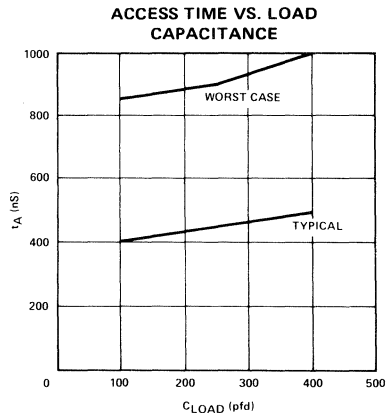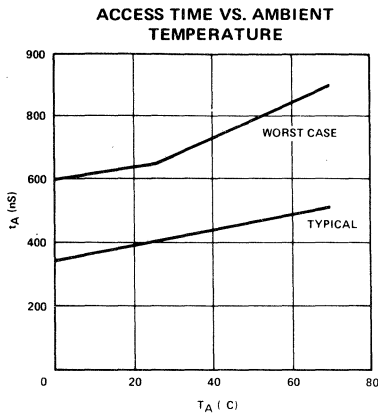
ACCESS TIME VS. AMBIENT TEMPERATURE

ACCESS TIME VS. LOAD CAPACITANCE

intel®

2316E
16,384 BIT STATIC ROM

- **Fast Access Time—450 ns Max.**

- **Single +5V ± 10% Power Supply**

- **Intel MCS 80 and 85 Compatible**

- **Three Programmable Chip Selects for Simple Memory Expansion and System Interface**

- **EPROM/ROM Pin Compatible for Cost-Effective System Development**

- **Completly Static Operation**

- **Inputs and Outputs TTL Compatible**

- **Three-State Output for Direct Bus Interface**

The Intel® 2316E is a 16,384-bit static, N-channel MOS read only memory (ROM) organized as 2048 words by 8 bits. Its high bit density is ideal for large, non-volatile data storage applications such as program storage. The three-state outputs and TTL input/output levels allow for direct interface with common system bus structures. The 2316E single +5V power supply and 450 ns access time are both ideal for usage with high performance microcomputers such as the Intel MCS™-80 and MCS™-85 devices.

A cost-effective system development program may be implemented by using the pin compatible Intel 2716 16K UV EPROM for prototyping and the lower cost 2316E ROM for production. The 2716 is fully compatible to the 2316E in all respects. The three 2316E programmable chip selects may be defined by the user and are fixed during the masking process. To simplify the conversion from 2716 prototyping to 2316E production, it is recommended that the 2316E programmable chip select logic levels be defined the same as that shown in the below data sheet pin configuration. This pin configuration and these chip select logic levels are the same as the 2716.

PIN CONFIGURATION

A_7 — 1	24 — V_{CC}
A_6 — 2	23 — A_8
A_5 — 3	22 — A_9
A_4 — 4	21 — CS_3
A_3 — 5	20 — $\overline{CS}_1$
A_2 — 6	19 — A_{10}
A_1 — 7	18 — CS_2
A_0 — 8	17 — D_7
D_0 — 9	16 — D_6
D_1 — 10	15 — D_5
D_2 — 11	14 — D_4
GND — 12	13 — D_3
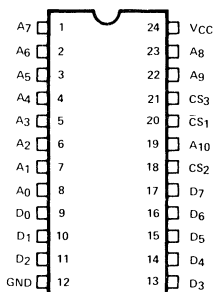
PIN NAMES

A_0–A_{10}	ADDRESS INPUTS
D_7–D_0	DATA OUTPUTS
CS_1–CS_3	CHIP SELECT INPUTS

BLOCK DIAGRAM

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . . . -10°C to 80°C
Storage Temperature . . . . -65°C to $+150^\circ$C
Voltage On Any Pin With Respect
  to Ground . . . . -0.5V to $+7$V
Power Dissipation . . . . 1.0 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
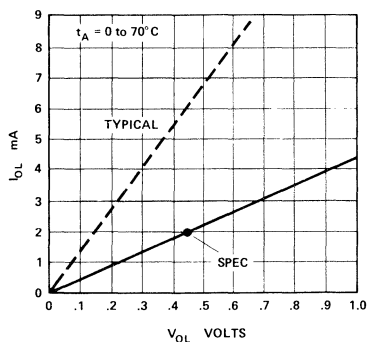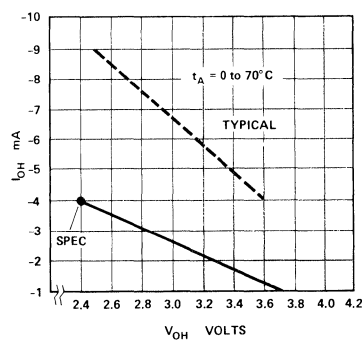
D.C. AND OPERATING CHARACTERISTICS

$T_A = 0^\circ$C to $+70^\circ$C, $V_{CC} = 5$V $\pm10\%$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	$V_{IN} = 0$ to 5.25V
I_{LOH}	Output Leakage Current			10	μA	Chip Deselected, $V_{OUT} = 4.0$V
I_{LOL}	Output Leakage Current			-20	μA	Chip Deselected, $V_{OUT} = 0.4$V
I_{CC}	Power Supply Current		70	120	mA	All Inputs 5.25V Data Out Open
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.4		$V_{CC}+1.0$V	V	
V_{OL}	Output "Low" Voltage			0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output "High" Voltage	2.4			V	$I_{OH} = -400\,\mu$A

NOTE: 1. Typical values for $T_A = 25^\circ$C and nominal supply voltage.

A.C. CHARACTERISTICS

$T_A = 0^\circ$C to $+70^\circ$C, $V_{CC} = +5$V $\pm10\%$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
t_A	Address to Output Delay Time		450	ns
t_{CO}	Chip Select to Output Enable Delay Time		120	ns
t_{DF}	Chip Deselect to Output Data Float Delay Time	10	100	ns

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . . 1 TTL Gate and $C_L = 100$ pF
Input Pulse Levels . . . . 0.8 to 2.4V
Input Pulse Rise and Fall Times (10% to 90%) . . . . . 20 ns
Timing Measurement Reference Level
  Input . . . . 1V and 2.2V
  Output . . . . 0.8V and 2.0V

CAPACITANCE(2) $T_A = 25^\circ$C, f = 1 MHz

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C_{IN}	All Pins Except Pin Under Test Tied to AC Ground	5 pF	10 pF
C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground	10 pF	15 pF

NOTE: 2. This parameter is periodically sampled and is not 100% tested.

PRELIMINARY

A.C. Waveforms
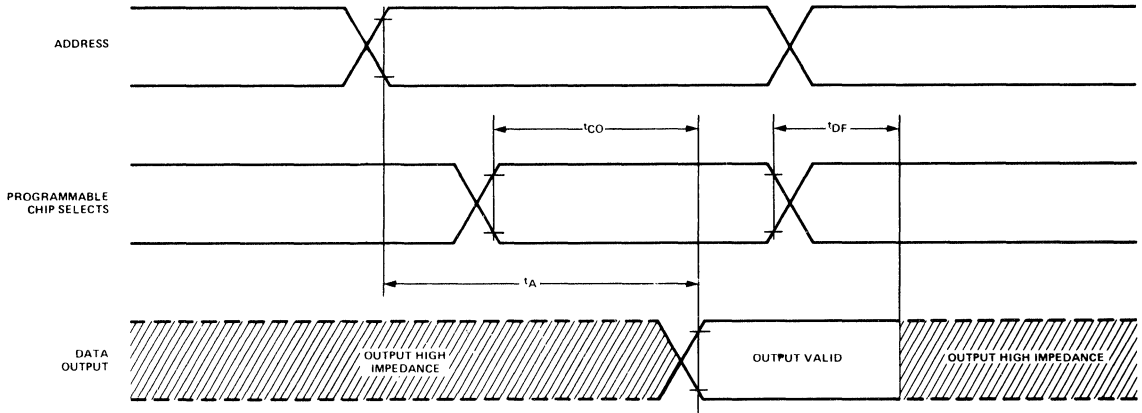
Typical System Application (8K × 8 ROM Memory)
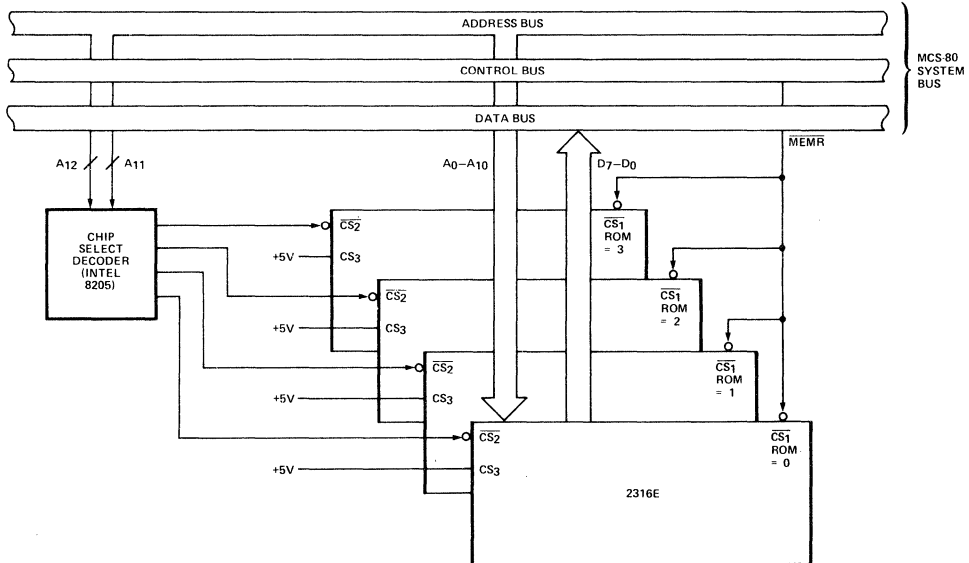
PROM AND ROM PROGRAMMING INSTRUCTIONS

TABLE OF CONTENTS

I. PROM AND ROM INPUT FORMATS

A. General Information

Intel can accept programming and masking information for PROMs, EPROMs, or ROMs in the form of punched paper tape, a master device from which to copy, or computer punched cards. The allowable paper tape and computer punched card formats are given in Table I. The preferred formats are the Intel Intellec Hex and BPNF since these formats are defined to allow detection of errors.

It is desirable that two, preferably different, input media for each customer code be sent so Intel can perform a code verification to detect any errors between the two inputs. This procedure, if followed, can avoid errors due to a mispunched tape/card or sending a defective or improper master device.

All orders must be accompanied by a customer PROM/ROM order form. A copy of the form is contained in this section and additional copies are available from Intel Literature Department, 3065 Bowers Ave., Santa Clara, California 95051.

Table I. Acceptable Paper Tape and Computer Card Formats

Paper Tape	Computer Card
Intellec Hex BPNF Hex	Intellec Hex PN

B. Paper Tape Format

The paper tape which should be used is 1" wide paper using 7 or 8-bit ASCII code (such as a Model 33 ASR Teletype produces). The three paper tape formats which should be sent are described in Sections B1 through B3.

B1. Intellec Hex Paper Tape Format

In the Intel Intellec Hex Format, a data field can contain either 8 or 4-bit data. *Two* ASCII hexadecimal characters must be used to represent *both* 8 and 4-bit data. In the case of 4-bit data, only one of the characters is meaningful and must be specified on the Intel PROM/ROM Order Form.

Preceding the first data field and following the last data field there must be a leader/trailer length of at least 25 null characters. Comments (except for a colon) may be placed on the tape leader.

The format described below is readily generated by the Intel Intellec Microcomputer Development System or by systems programmed by the user.

1. RECORD MARK FIELD: Frame 0

   The ASCII code for a colon (:) is used to signal the start of a record.

2. RECORD LENGTH FIELD: Frames 1 and 2

   The number of data bytes in the record is representated by two ASCII hexadecimal digits in this field. The high-order digit is in frame 1. The maximum number of data bytes in a record is 255 (FF in hexadecimal). An end-of-file record contains two ASCII zeros in this field.

3. LOAD ADDRESS FIELD: Frames 3–6

   The four ASCII hexadecimal digits in frames 3–6 give the address at which the data is loaded. The high-order digit is in frame 3, the lower-order digit in frame 6. The first data byte is stored in the location indicated by the load address; successive bytes are stored in successive memory locations. This field in an end-of-file record contains zeros or the starting address of the program.

4. RECORD TYPE FIELD: Frames 7 and 8

   The two ASCII hexadecimal digits in this field specify the record type. The high-order digit is in frame 7. All data records are type 0; end-of-file records are type 1. Other possible values for this field are reserved for future expansion.

5. DATA FIELD: Frames 9 to 9+2*(record length)–1

   A data byte is represented by two frames containing the ASCII characters 0–9 or A–F, which represent a hexadecimal value between 0 and FF (0 and 255 decimal). The high-order digit is in the first frame of each pair. If the data is 4-bit, then either the high or low-order digit represents the data and the other digit of the pair may be any ASCII hexadecimal digit. There are no data bytes in an end-of-file record.

6. CHECKSUM FIELD: Frames 9+2*(record length) to 9+2*(record length)+1

The checksum field contains the ASCII hexadecimal representation of the two's complement of the 8-bit sum of the 8-bit bytes that result from converting each pair of ASCII hexadecimal digits to one byte of binary, from the record length field to and including the last byte of the data field. Therefore, the sum of all the ASCII pairs in a record after converting to binary, from the record length field to and including the checksum field, is zero.

Intellec Hex Example:

```
: 10310000311A320E03117E31CD40003A9231B7C2EE
: 1031100060310E00117031CD40003A9231B7C2607B
: 10312000312A7E31227A310E03117E31CD40003AB0
: 103130009231B7C260312A8C317CB5CA50310E044D
: 10314000118831CD40003A9231B7C26031C3273186
: 103150000E01117A31CD40000E09119031CD4000A1
: 103160000E0C119231CD40000E09119031CD40006E
: 0A3170007E3196310100000092311B
: 10317C0092310100963180008C31923100009631F1
: 04318E0092319231B7
: 0231940092319231B7
: 00310001CE
```

B2. BPNF Paper Tape Format

The format requirements are as follows:

1. All data fields are to be punched in consecutive order, starting with data field 0 (all addresses low). There must be exactly N data fields for a N x 8 or N x 4 device organizations.

2. Each data field must begin with the start character B and end with the stop character F. There must be exactly 8 or 4 data characters between the B and F for a N x 8 or N x 4 organization, respectively.

   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A DATA FIELD. If in preparing a tape an error is made, the entire data field, including the B and F must be rubbed out. Within the data field, a P results in a high level output, and an N results in a low level output.

3. Preceding the first data field and following the last data field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes) or null characters.

4. Between data fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") after each 72 characters. When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.

5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the device pattern number.

6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

Example of BPNF 2048 x 8 format (N = 2048):
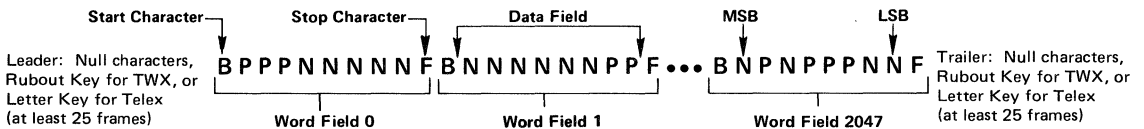
Example of 512 x 4 format (N = 512):
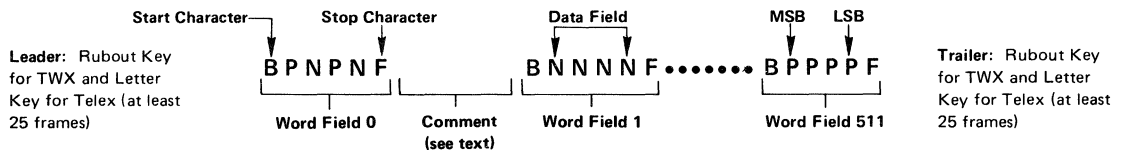
B3. Non-Intellec Hex Paper Tape Format

For the non-Intellec Hex Format, a data field can contain either 8 or 4-bit data. *Two* ASCII hexadecimal characters must be used to represent *both* 8 and 4-bit data. In the case of 4-bit data, only one of the characters is meaningful and must be specified on the Intel PROM/ROM Order Form.

Parity is allowed; however, it is not checked. Preceding the first data field and following the last data field there must be a leader/trailer length of at least 25 null characters or rubout punches.

The format requirements are as follows:

1. The start of the first data field is indicated by a colon. After the last data field, a semicolon must be punched to indicate the end. All data fields are to be punched in consecutive order, starting with data field 00_H (all addresses low).

2. *Two* hex characters must be used to represent the data field of both N word x 8-bit and N word x 4-bit devices. For an 8-bit data field, the high order data is represented by the left justified character of the pair. Either character of the pair may be used to represent the word field of a N word x 4-bit device, however, it must be consistent throughout the word field. The other character may be any hex character.

   A field of "don't care" data is allowed. Data after a field of "don't care" will be programmed starting at an address location enclosed in parentheses. In the following example, data is entered in addresses 00_H to 05_H, followed with "don't care" from addresses 06_H to 25_H, data being entered again starting at address location 26_H, and followed with "don't care" data to the last address location.

   | Start Character | Data Fields from Address 00_H to 05_H | Address Location where Data is to be Programmed | Data Fields from Address 26_H to $2A_H$ | End Character |
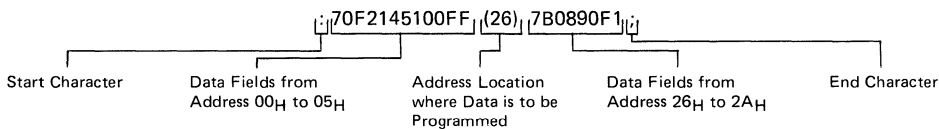
3. The x character may be used to rubout any erroneous character(s). The # character may be used to rubout an entire line up to the previous carriage return.

4. Spaces are allowed only between *separate* word fields.

5. After each 72 characters, a carriage return followed by a line feed should be punched to allow a print-out of the tape.

6. Comments must be placed only between the tape leader and the start of the first data field.

C. Computer Punched Card Format

The following general format is applicable to the programming information sent on computer punched cards:

1. An 80 column Hollerith card (interpreted) punched on an IBM 026 or 029 keypunch should be submitted.

2. A single deck must consist of a Title Card followed by the data cards. There will be N/8 or N/14 data cards for N words x 8-bit and N words x 4-bit devices, respectively, in the PN format.

   For the Intellec Hex format, there will be N/32 data cards for both N words x 8-bit and N words x 4-bit devices, and one end of file card.

C1. Intellec Hex Computer Punched Card Format

Two hex characters must be used to represent data for both a N word x 8-bit and N word x 4-bit device. For the latter, only one of the characters is meaningful and must be specified on the Intel PROM/ROM Order Form. The entire data field for all bits must be punched even if it is "don't care".

Column	Data
1	Punch a T
2–3	Blank
4–28	Customer Company Name
29–30	Blank
31–50	Customer's Company Division or location
51–52	Blank
53–61	Customer Part Number
62–63	Blank
64–72	Punch the Intel 4-digit basic part number and in ( ) the number of output bits; e.g., 2708 (8), 2316 (8), or 3605 (4)
73–74	Blank
75–76	Chip number for ROMs with programmable chip select inputs. If not applicable, leave blank.
77–78	Blank
79–80	Punch a 2-digit decimal number to indicate truth table number. The first truth table will be 00, second 01, third 02, etc.

a. N word x 8-bit device

Column	Data
1	Record mark: A colon is used to signal the start of a record.
2–3	Record length: This is the count of the actual data bytes in the record. Column 2 contains the high order digit of the count, Column 3 contains the low order digit. A record length of zero indicates end of file. All frames containing data will have a maximum record length of 10_{Hex} bytes (32 decimal).
4–7	Load address: The four characters starting addresses at which the following data will be loaded. The high order digit of the load address is in Column 4 and the low order digit is in Column 7. The first data byte is stored in the location indicated by the load address. Successive data bytes are stored in successive memory locations. ROMs containing more than 32 bytes of data will use two or more records or cards to transmit the data. Although the load address for the beginning record need not be 0000, each subsequent load address should be "10_H" (32 decimals) greater than the last.
8–9	Record type: A 2-digit code in this field specifies the type of this record. The high order digit of this code is located in Column 8. Currently, all data records are type 0. End-of-file records will be type 1; they are distinguished by a zero RECORD LENGTH field (see above). Other possible values for this field are reserved for future expansion.
10–73	Data
75–75	Checksum: Same as paper tape format.
76–78	Blank
79–80	Punch same 2-digit decimal number as in Title Card.

b. N word x 4-bit device

This format is identical to the previously documented 8-bit hexadecimal format with the following exceptions:

Column	Data
10–73	Each memory location is represented by two columns containing the characters 0–9, A–F. Since this is 4-bit data, the user must indicate which character of each pair is to be used as valid data. A single deck must be submitted without mixing first and second characters of the pair.

C2. PN Computer Punched Card Format

A word field consists of only P's and N's. A punched P will result in an output high level and a punched N in an output low level. The B and F characters, unlike the paper tape format, are illegal characters. The entire data field for all bits must be punched even if it is "don't care". The data field must begin in consecutive order, starting with address 0 (all addresses logically low).

DECIMAL NUMBER INDICATING
THE TRUTH TABLE NUMBER
NO. OF OUTPUTS
4 or 8
INTEL
P/N

TITLE CARD
DESIGNATION
CUSTOMER'S COMPANY NAME
CUSTOMER'S DIVISION OR LOCATION
CUSTOMER'S P/N

Column	Data
1	Punch a T
2–3	Blank
4–28	Customer Company Name
29–30	Blank
31–50	Customer's Company Division or location
51–52	Blank
53–61	Customer Part Number
62–63	Blank
64–72	Punch the Intel 4-digit basic part number and in ( ) the number of output bits; e.g., 2708 (8), 2316 (8), or 3605 (4)
73–74	Blank
75–76	Chip number for ROMs with programmable chip select inputs. If not applicable, leave blank.
77–78	Blank
79–80	Punch a 2-digit decimal number to indicate truth table number. The first truth table will be 00, second 01, third 02, etc.

Title Card Format.

For a N words × 4-bit organization only, cards 2 and those following should be punched as shown. Each card specifies the 4-bit output of 14 words.

LSB
MSB
DECIMAL WORD ADDRESS BEGINNING EACH CARD
14 DATA FIELDS
DECIMAL NUMBER INDICATING THE TRUTH TABLE NUMBER

Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., 00000, 00014, 00028, etc.
6	Blank
7-10	Data Field
11	Blank
12-15	Data Field
16	Blank
17-20	Data Field
21	Blank
22-25	Data Field
26	Blank
27-30	Data Field
31	Blank
32-35	Data Field
36	Blank
37-40	Data Field
41	Blank
42-45	Data Field
46	Blank
47-50	Data Field
51	Blank
52-55	Data Field
56	Blank
57-60	Data Field
61	Blank
62-65	Data Field
66	Blank
67-70	Data Field
71	Blank
72-75	Data Field
76-78	Blank
79-80	Punch same 2 digit decimal number as in title card.

For a N words X 8-bit organization only, cards 2 and those following should be punched as shown. Each card specifies the 8-bit output of 8 words.

Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., $\emptyset\emptyset\emptyset\emptyset\emptyset$, $\emptyset\emptyset\emptyset\emptyset$8, $\emptyset\emptyset\emptyset$16, etc.
6	Blank
7-14	Data Field
15	Blank
16-23	Data Field
24	Blank
25-32	Data Field
33	Blank
34-41	Data Field
42	Blank
43-50	Data Field
51	Blank
52-59	Data Field
60	Blank
61-68	Data Field
69	Blank
70-77	Data Field
78	Blank
79-80	Punch same 2 digit decimal number as in title card.

DECIMAL WORD ADDRESS BEGINNING EACH CARD — MSB — LSB — 8 DATA FIELDS — DECIMAL NUMBER INDICATING THE TRUTH TABLE NUMBER

D.   Custom PROM/ROM Order Forms

All orders for PROMs/ROMs which are to be electrically or mask programmed at Intel must be submitted with the order forms shown on the following pages. Additional forms are available from Intel Literature Department, 3065 Bowers Ave., Santa Clara, California 95051. The ROM Order Forms for the 4001 and 4308 are shown on pages 8-97 and 8-108, respectively.

The order forms for the individual PROMs/ROMs are listed in Table II below.

Table II

PROM/ROM Part Number	Order Form Number
MOS EPROMs	A
8748, 8755	A
2316E, 8316A, 8316AL	B
8048	C
8308	D
8355	E
Bipolar PROMs/ROMs	F

<div align="center">

**CUSTOMER EPROM
ORDER FORM
A**

</div>

<div align="right">

**1702A/4702A/8702A Family
2708/8708/2704 Family
2716, 8748, 8755**

</div>

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Intel Device P/N _____

All custom MOS EPROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

The marking will consist of the Intel Logo, the product and package type (B1702A), the 4-digit Intel pattern number (WWWW), an internal manufacturing traceability code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.

**1702A MARKING
EXAMPLE**

1

□ B1702A

XXYY

WWWW
Z....Z

CUSTOMER PART NUMBER

Customer P/N (Please Fill-In)	**Intel Pattern Number** (Please Do Not Use)
1 �	1 ⌊⌋
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19

CUSTOMER 16K ROM
ORDER FORM
B

Company _____ Phone # _____	For Intel Use Only
Company Contact _____ Date _____	S# _____
P.O. # _____ Intel P/N & Pkg _____	STD _____
	APP _____

A custom 16K ROM order must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

Date _____

MARKING

The marking will consist of the Intel Logo, the product and package type (P2316E), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.
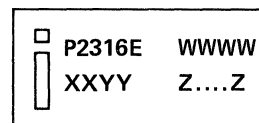
```
┌─────────────────────┐
│ □  P2316E   WWWW     │
│ ▯  XXYY     Z....Z   │
└─────────────────────┘
   1
```

P2316E MARKING EXAMPLE

IMPORTANT MASK OPTION SPECIFICATION

The chip select inputs are mask programmable and must be specified by the user. The chip select logic levels must be specified with one of the below Chip Numbers. The Chip Number will be coded in terms of positive logic where a logic "1" is a high level input. It should be noted that Chip Number 4 for the 2316E is compatible to Intel's 2716 EPROM.

Chip Number	CS3	CS2	CS1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

CUSTOMER PART NUMBER

Customer P/N (Please Fill-In)	Chip Number (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1 |_|_|_|_|_|_|_|_|_|	1 |_|_|_|_|_|_|_|_|_|	1 |_|_|_|_|_|_|_|_|_|
2 |_|_|_|_|_|_|_|_|_|	2 |_|_|_|_|_|_|_|_|_|	2 |_|_|_|_|_|_|_|_|_|
3 |_|_|_|_|_|_|_|_|_|	3 |_|_|_|_|_|_|_|_|_|	3 |_|_|_|_|_|_|_|_|_|
4 |_|_|_|_|_|_|_|_|_|	4 |_|_|_|_|_|_|_|_|_|	4 |_|_|_|_|_|_|_|_|_|
5 |_|_|_|_|_|_|_|_|_|	5 |_|_|_|_|_|_|_|_|_|	5 |_|_|_|_|_|_|_|_|_|
6 |_|_|_|_|_|_|_|_|_|	6 |_|_|_|_|_|_|_|_|_|	6 |_|_|_|_|_|_|_|_|_|
7 |_|_|_|_|_|_|_|_|_|	7 |_|_|_|_|_|_|_|_|_|	7 |_|_|_|_|_|_|_|_|_|
8 |_|_|_|_|_|_|_|_|_|	8 |_|_|_|_|_|_|_|_|_|	8 |_|_|_|_|_|_|_|_|_|
9 |_|_|_|_|_|_|_|_|_|	9 |_|_|_|_|_|_|_|_|_|	9 |_|_|_|_|_|_|_|_|_|
10 |_|_|_|_|_|_|_|_|_|	10 |_|_|_|_|_|_|_|_|_|	10 |_|_|_|_|_|_|_|_|_|
11 |_|_|_|_|_|_|_|_|_|	11 |_|_|_|_|_|_|_|_|_|	11 |_|_|_|_|_|_|_|_|_|

CUSTOMER 8308 ROM
ORDER FORM
D

		For Intel Use Only
Company _____	Phone # _____	S# _____
Company Contact _____	Date _____	STD _____
P.O. # _____	Intel P/N & Pkg _____	APP _____
		Date _____

All custom 8308 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking will consist of the Intel logo, the product type (C8308), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and a maximum 9-digit number (Z....Z) which is specified by the user. The 9-digit number may be a part number or the 8308 chip number.
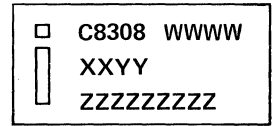
```
☐  C8308  WWWW
☐  XXYY
☐  ZZZZZZZZZ
```
1

C8308 MARKING EXAMPLE

IMPORTANT MASK OPTION SPECIFICATION

The CS_2 chip select input is mask programmable and must be specified by the user. The chip select logic level must be specified with one of the below Chip Numbers. The Chip Number will be coded in terms of positive logic where a "1" is a high level input.

Chip Number	$\overline{CS_1}$ (non-programmable)	CS_2 (programmable)
0	0	0
1	0	1

CUSTOMER PART NUMBER

Customer P/N (Please Fill-In)	Chip Number (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
14	14	14

CUSTOMER 8355 ROM
ORDER FORM
E

	For Intel Use Only
Company _____ Phone # _____	S# _____
Company Contact _____ Date _____	STD _____
P.O. # _____ Package Type: ☐ Plastic ☐ Cerdip	APP _____
	Date _____

All custom 8355 orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats described in the Programming Instruction sectin of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

All devices will be marked as shown at the right figure. The marking will consist of the Intel Logo, the product and package type (P8355), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.
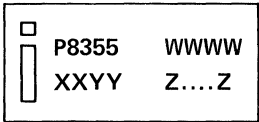
```
┌──────────────────────┐
│ ☐                     │
│ │  P8355    WWWW      │
│ │  XXYY     Z....Z    │
│ └                     │
└──────────────────────┘
            1
P8355 MARKING EXAMPLE
```

CUSTOMER PART NUMBER

Customer P/N
(Please Fill-In)

1 └┴┴┴┴┴┴┴┴┴┘
2 └┴┴┴┴┴┴┴┴┴┘
3 └┴┴┴┴┴┴┴┴┴┘
4 └┴┴┴┴┴┴┴┴┴┘
5 └┴┴┴┴┴┴┴┴┴┘
6 └┴┴┴┴┴┴┴┴┴┘
7 └┴┴┴┴┴┴┴┴┴┘
8 └┴┴┴┴┴┴┴┴┴┘
9 └┴┴┴┴┴┴┴┴┴┘
10 └┴┴┴┴┴┴┴┴┴┘
11 └┴┴┴┴┴┴┴┴┴┘
12 └┴┴┴┴┴┴┴┴┴┘
13 └┴┴┴┴┴┴┴┴┴┘
14 └┴┴┴┴┴┴┴┴┴┘
15 └┴┴┴┴┴┴┴┴┴┘
16 └┴┴┴┴┴┴┴┴┴┘
17 └┴┴┴┴┴┴┴┴┴┘
18 └┴┴┴┴┴┴┴┴┴┘
19 └┴┴┴┴┴┴┴┴┴┘
20 └┴┴┴┴┴┴┴┴┴┘

Intel Pattern Number
(Please Do Not Use)

1 └┴┴┴┴┴┴┴┴┴┘
2 └┴┴┴┴┴┴┴┴┴┘
3 └┴┴┴┴┴┴┴┴┴┘
4 └┴┴┴┴┴┴┴┴┴┘
5 └┴┴┴┴┴┴┴┴┴┘
6 └┴┴┴┴┴┴┴┴┴┘
7 └┴┴┴┴┴┴┴┴┴┘
8 └┴┴┴┴┴┴┴┴┴┘
9 └┴┴┴┴┴┴┴┴┴┘
10 └┴┴┴┴┴┴┴┴┴┘
11 └┴┴┴┴┴┴┴┴┴┘
12 └┴┴┴┴┴┴┴┴┴┘
13 └┴┴┴┴┴┴┴┴┴┘
14 └┴┴┴┴┴┴┴┴┴┘
15 └┴┴┴┴┴┴┴┴┴┘
16 └┴┴┴┴┴┴┴┴┴┘
17 └┴┴┴┴┴┴┴┴┴┘
18 └┴┴┴┴┴┴┴┴┴┘
19 └┴┴┴┴┴┴┴┴┴┘
20 └┴┴┴┴┴┴┴┴┴┘

II. MOS EPROMs

A. Erasure Procedure

As stated in the EPROM related data sheets, the recommended erasure procedure to use with EPROMs is to illuminate the window with a UV lamp which has a wavelength of 2537 Angstroms (Å). The data sheets specify a distance of 1 inch and erase times of 10–45 minutes, depending on the type of device and UV lamp. Actually, the amount of time required to erase a device can be concisely stated in terms of the amount of UV energy incident to the window, expressed in Watt-seconds per square centimeter (W-sec/cm^2). Table III lists the required integrated dosgae (UV intensity × exposure time) for the EPROMs currently in production by Intel.

Table III. Required Erase Energy for Device Types

Device Type	2537Å Erase Energy
1702A/4702A	6 W-sec/cm^2
2708/8708	15 W-sec/cm^2
2716	15 W-sec/cm^2
8748	15 W-sec/cm^2
8755	15 W-sec/cm^2

The erase energy expressed in Table III includes a guardband to ensure complete erasure of all bits. *It is not sufficient to monitor "first bit" erasure to determine erasure time, as some other bits in the array may not be erased.*

A1. UV Sources

There are several models of UV lamps that can be used to erase EPROMs (see Table IV). The model numbers in the table refer to lamps manufactured by Ultra Violet Products of San Gabriel, California. In addition, there are several other manufacturers, including Data I/O (Issaquah, Wash.), PROLOG (Monterey, Calif.). Prometrics (Chicago, Ill.), and Turner Designs (Mt. View, Calif.). The individual manufacturers should be consulted for detailed product descriptions. Also shown in the table are typical erase times for various combinations of Intel PROMs and lamp intensities.

Table IV.

Model	Power Rating	Minimum Erase Time for Indicated Dosage Without a Filter Over the Bulb	
		6 W-sec 1702A, 4702A	15 W-sec 2708, 8708, 8755 2716, 8748
R-52	13000 μW/cm^2	7.7 min	19.2 min
S-52	12000 μW/cm^2	8.3 min	20.7 min
S-68	12000 μW/cm^2	8.3 min	20.7 min
UVS-54	5700 μW/cm^2	17.5 min	43.8 min
UVS-11	5500 μW/cm^2	18.2 min	45.6 min

According to the manufacturers, the output of the UV lamp bulbs decrease with age. The output of the lamp should be verified periodically to ensure that adequate intensities are maintained. If this is not done, bits may be partially erased which will interfere with later programming and/or operation at high temperature.

For lamps other than those listed, the erase time can be determined by using a UV intensity meter, such as the Ultra Violet Products Model J-225. When a meter is used, the intensity should be measured at the same position (distance from the lamp) as the EPROMs to be erased. This will require careful positioning to insure that the sensor will receive the same amount of UV light that the window of the EPROM will receive.

The sensors used with most UV intensity meters show reduced output with constant exposure to UV light. Therefore, they should not be permanently placed inside the erasure enclosure, they should only be used for periodic measurements.

B. 2708/2704 Family Programming

Initially, and after each erasure, all 8192/4096 bits of the 2708/2704 are in the "1" state (output high). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for programming operation by raising the CS/WE input (pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8 bits in parallel, to the data output lines (O_1-O_8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up, one program pulse per address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to N x t_{PW} $\geq$ 100 ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{PW} = 1 ms) to greater than 1000 (t_{PW} = 0.1 ms). There must be N successive loops throuhg all 1024 addresses. *It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.* Caution should be observed regarding the end of a program sequence. The CS/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small amount of current (I_{ILL}) when CS/WE is at V_{IHW} (12V) and the program pulse is at V_{ILP}.

Programming Examples (Using N x t_{PW} $\geq$ 100 ms)

Example 1: All 8096 bits are to be programmed with a 0.5 ms program pulse width.

The minimum number of program loops is 200. One program loop consists of words 0 to 1023.

Example 2: Words 0 to 100 and 500 to 600 are to be programmed. All other bits are "don't care". The program pulse width is 0.75 ms.

The minimum number of program loops is 133. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1's.

Example 3: Same requirements as example 2, but the PROM is now to be *updated* to include data for words 750 to 770.

The minimum number of program loops is 133. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1's. Addresses 0 to 100 and 500 to 600 must be re-programmed with their original data pattern.

2704, 2708
PROGRAM CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V ±5%, V_{DD} = +12V ±5%, V_{BB} = –5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

D.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Address and $\overline{CS}$/WE Input Sink Current			10	μA	V_{IN} = 5.25V
I_{IPL}	Program Pulse Source Current			3	mA	
I_{IPH}	Program Pulse Sink Current			20	mA	
I_{DD}	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Level (except Program)	V_{SS}		0.65	V	
V_{IH}	Input High Level for all Addresses and Data	3.0		V_{CC}+1	V	
V_{IHW}	$\overline{CS}$/WE Input High Level	11.4		12.6	V	Referenced to V_{SS}
V_{IHP}	Program Pulse High Level	25		27	V	Referenced to V_{SS}
V_{ILP}	Program Pulse Low Level	V_{SS}		1	V	$V_{IHP} - V_{ILP}$ = 25V min.

A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	10			μs
t_{CSS}	$\overline{CS}$/WE Setup Time	10			μs
t_{DS}	Data Setup Time	10			μs
t_{AH}	Address Hold Time	1			μs
t_{CH}	$\overline{CS}$/WE Hold Time	.5			μs
t_{DH}	Data Hold Time	1			μs
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns
t_{DPR}	Program To Read Delay			10	μs
t_{PW}	Program Pulse Width	.1		1.0	ms
t_{PR}	Program Pulse Rise Time	.5		2.0	μs
t_{PF}	Program Pulse Fall Time	* .5		2.0	μs

NOTE: Intel's standard product warranty applies only to devices programmed to specifications described herein.

2704, 2708
Programming Waveforms
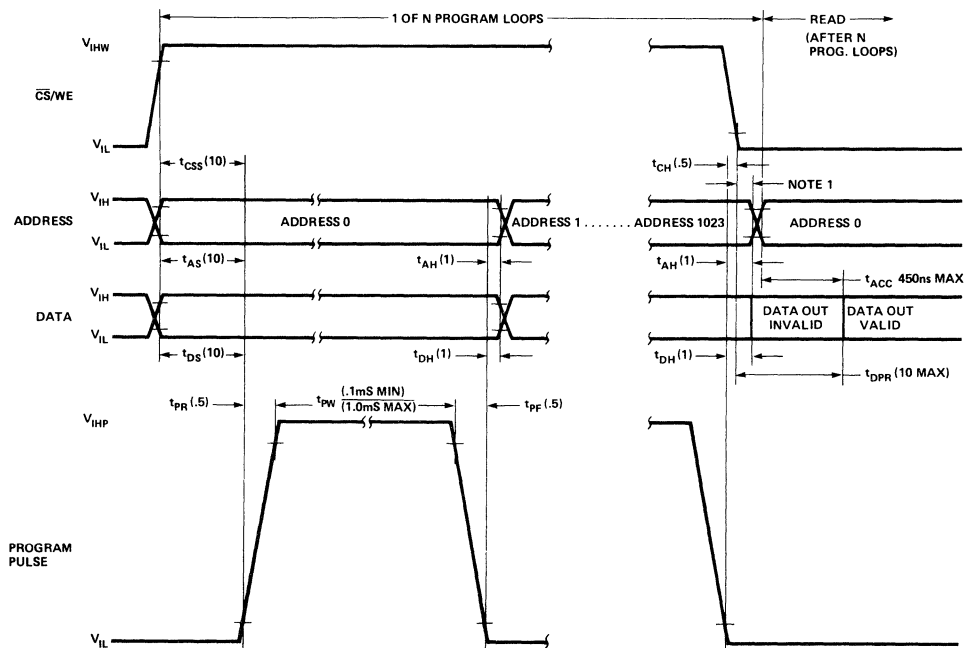
NOTE 1. THE $\overline{CS}$/WE TRANSITION MUST OCCUR AFTER THE PROGRAM PULSE TRANSITION AND BEFORE THE ADDRESS TRANSITION.

NOTE 2. NUMBERS IN ( ) INDICATE MINIMUM TIMING IN μs UNLESS OTHERWISE SPECIFIED.

C. 2716 Programming

Initially, and after each erasure, all 16,384 bits of the 2716 are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 2716 is programmed by applying a 50 ms, TTL programming pulse to the PD/PGM pin with the $\overline{CS}$ input high and the V_{PP} supply at 25V ±1V. Any location may be programmed at any time — either individually, sequentially, or randomly. The programming time for a single bit is only 50 ms and for all 16,384 bits is approximately 100 sec. The detailed programming specifications and timing waveforms are given in the following tables and figures.

CAUTION: The V_{CC} and V_{PP} supplies must be sequenced on and off such that V_{CC} is applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} to prevent damage to the 2716. The maximum allowable voltage during programming which may be applied to the V_{PP} with respect to ground is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding the 26-volt maximum specification. For convenience in programming, the 2716 may be verified with the V_{PP} supply at 25V ±1V. During normal read operation, however, V_{PP} must be at V_{CC}.

2716 PROGRAM CHARACTERISTICS[1]

$T_A = 25°C ±5°C$, $V_{CC}[2] = 5V ±5\%$, $V_{PP}[2,3] = 25V ±1V$

D.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Current (for Any Input)			10	μA	$V_{IN} = 5.25V/0.45$
I_{PP1}	V_{PP} Supply Current			5	mA	PD/PGM = V_{IL}
I_{PP2}	V_{PP} Supply Current During Programming Pulse			30	mA	PD/PGM = V_{IH}
I_{CC}	V_{CC} Supply Current			100	mA	
V_{IL}	Input Low Level	−0.1		0.8	V	
V_{IH}	Input High Level	2.2		V_{CC}+1	V	

A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	
t_{AS}	Address Setup Time	2			μs	
t_{CSS}	$\overline{CS}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{CSH}	$\overline{CS}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns	PD/PGM = V_{IL}
t_{CO}	Chip Select to Output Delay			120	ns	PD/PGM = V_{IL}
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

NOTES: 1. Intel's standard product warranty applies only to devices programmed to specifications described herein.
   2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The 2716 must not be inserted into or removed from a board with V_{PP} at 25 ±1V to prevent damage to the device.
   3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.

A.C. Conditions of Test:

V_{CC} .... 5V ±5%
V_{PP} .... 25V ±1V
Input Rise and Fall Times (10% to 90%) .... 20 ns

Input Pulse Levels .... 0.8V to 2.2V
Input Timing Reference Level .... 1V and 2V
Output Timing Reference Level .... 0.8V and 2V

PROGRAMMING WAVEFORMS

V_{PP} = 25V ±1V, V_{CC} = 5V ±5%
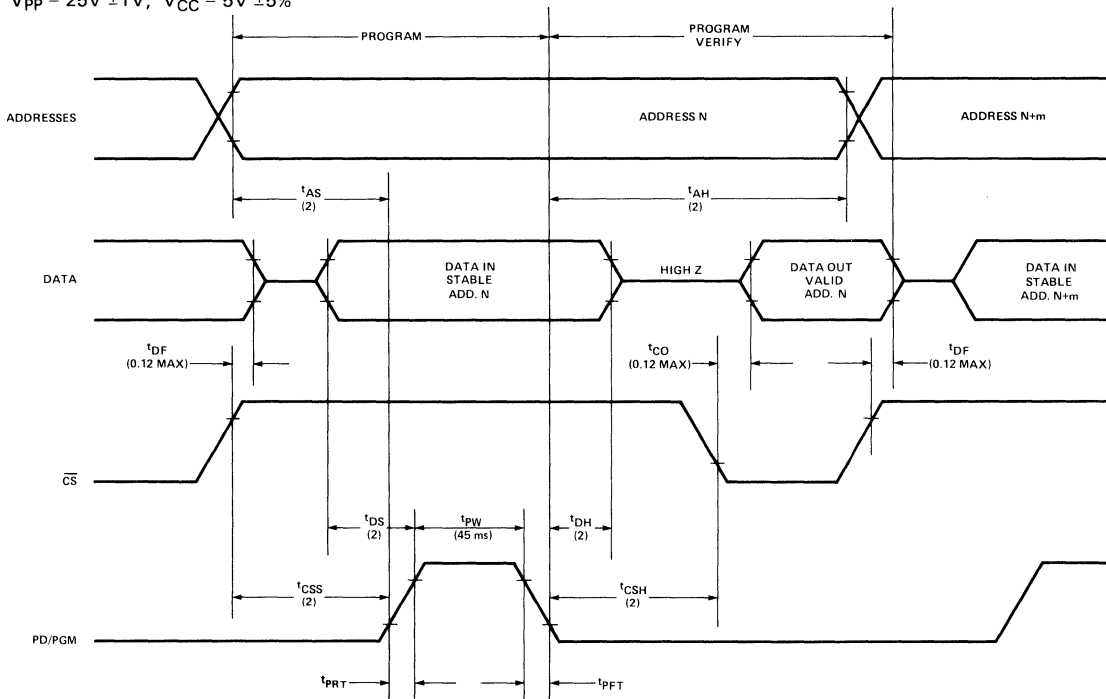
NOTE: ALL TIMES SHOWN IN PARENTHESES ARE MINIMUM TIMES AND ARE μSEC UNLESS OTHERWISE NOTED.

D. 8748/8755 Programming

Initially, and after each erasure, all bits of the EPROM portions of the 8748 and 8755 are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The EPROM portions of the 8748 and 8755 are programmed on the Intel® Universal PROM Programmer (UPP). The UPP and its related personality cards for the 8748 and 8755 are described beginning on page 7-15 of this catalog.

2316E 16K ROM
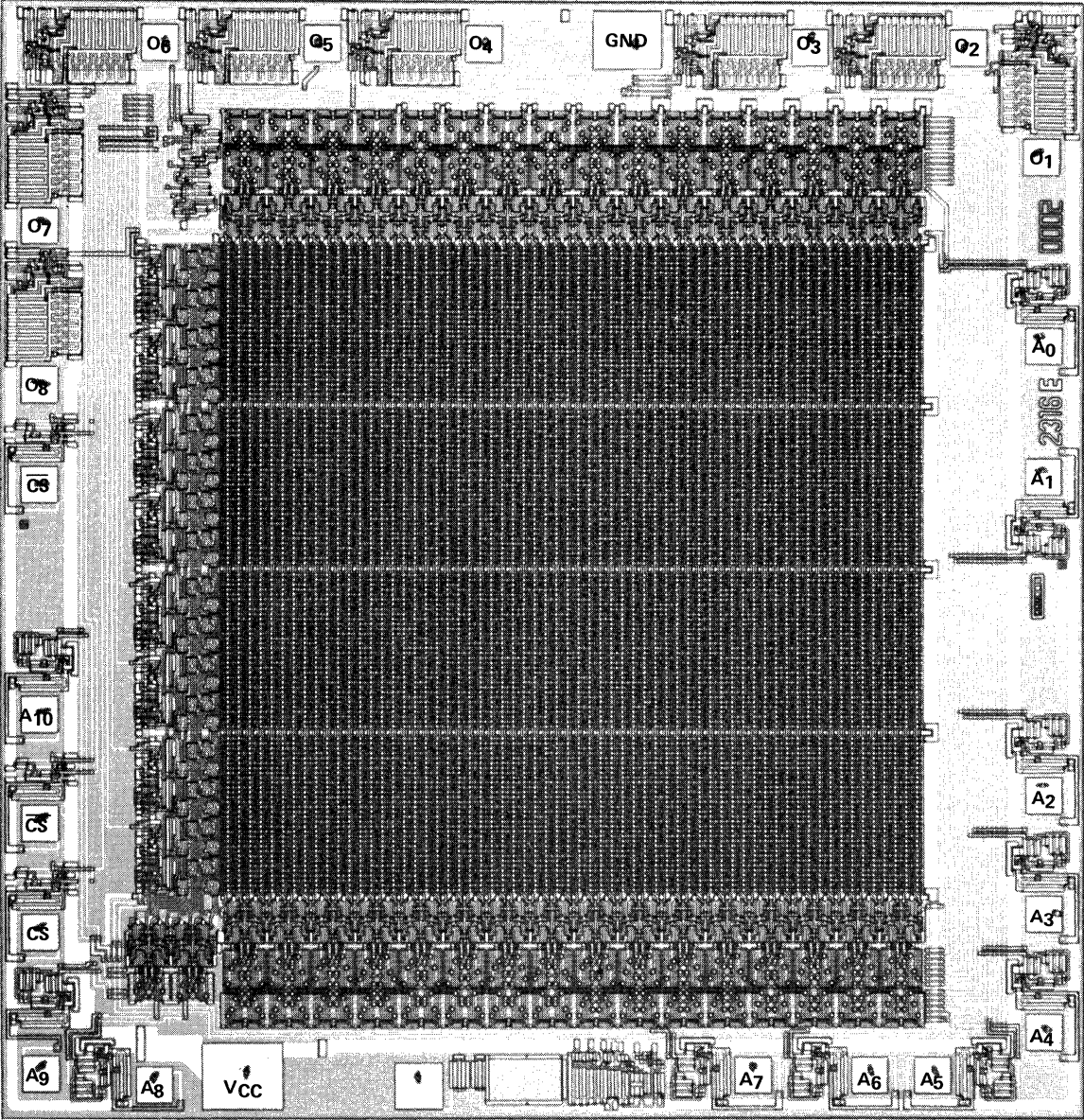
2708 8K UV EPROM

2716 16K EPROM

RAMs

RAMs

intel®

8101A-4
1024 BIT STATIC MOS RAM
WITH SEPARATE I/O

* 450 nsec Access Time Maximum
* 256 Word by 4 Bit Organization

- ■ Single +5V Supply Voltage
- ■ Directly TTL Compatible: All Inputs and Outputs
- ■ Static MOS: No Clocks or Refreshing Required
- ■ Simple Memory Expansion: Chip Enable Input

- ■ Powerful Output Drive Capability
- ■ Low Cost Packaging: 22 Pin Plastic Dual In-Line Configuration
- ■ Low Power: Typically 150mW
- ■ Three-State Output: OR-Tie Capability
- ■ Output Disable Provided for Ease of Use in Common Data Bus Systems

The Intel® 8101A-4 is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 8101A-4 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bi-directional logic in a common I/O system.

The Intel® 8101A-4 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION	LOGIC SYMBOL	BLOCK DIAGRAM

PIN NAMES

DI_1-DI_4	DATA INPUT	CE_2	CHIP ENABLE 2
A_0-A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT	DO_1-DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . $-10°C$ to $80°C$

Storage Temperature . . . . $-65°C$ to $+150°C$

Voltage On Any Pin
 With Respect to Ground . . . . $-0.5V$ to $+7V$

Power Dissipation . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current		1	10	μA	$V_{IN} = 0$ to $5.25V$
I_{LOH}	I/O Leakage Current[2]		1	10	μA	Output Disabled, $V_{OUT} = 4.0V$
I_{LOL}	I/O Leakage Current[2]		-1	-10	μA	Output Disabled, $V_{OUT} = 0.45V$
I_{CC1}	Power Supply Current		35	55	mA	$V_{IN} = 5.25V$, $I_O = 0mA$ $T_A = 25°C$
I_{CC2}	Power Supply Current			60	mA	$V_{IN} = 5.25V$, $I_O = 0mA$ $T_A = 0°C$
V_{IL}	Input "Low" Voltage	-0.5		$+0.8$	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			$+0.45$	V	$I_{OL} = 2.0mA$
V_{OH}	Output "High" Voltage	2.4			V	$I_{OH} = -400\mu A$

TYPICAL D.C. CHARACTERISTICS

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE

OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
 2. Input and Output tied together.

A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	(See Below)
t_{DF} [2]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	(See Below)
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

A.C. CONDITIONS OF TEST

t_r, t_f . . . . 20 ns
Input Levels . . . . 0.8V or 2.0V
Timing Reference 1.5V
Load . . . . 1 TTL Gate and $C_L = 100$ pF

CAPACITANCE [3] $T_A = 25°C$, f = 1 MHz

Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8
C_{OUT}	Output Capacitance $V_{OUT} = 0V$	8	12

WAVEFORMS

READ CYCLE
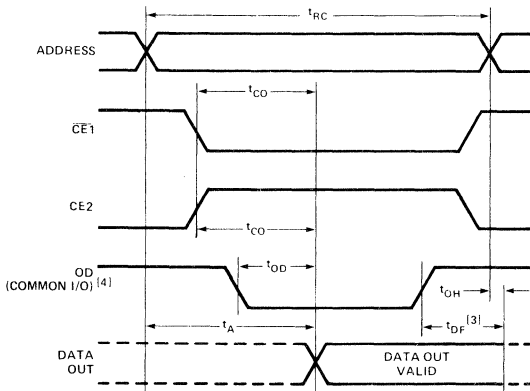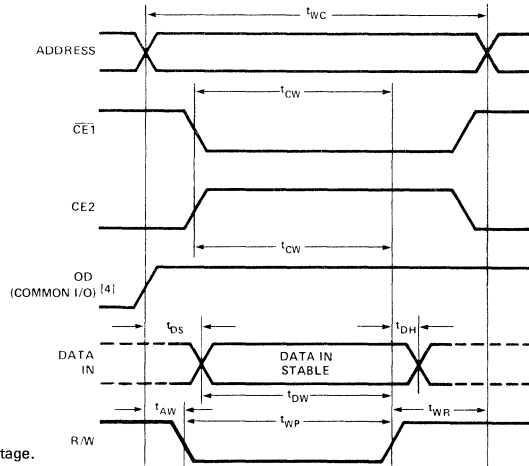
WRITE CYCLE

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.
3. This parameter is periodically sampled and is not 100% tested.
4. OD should be tied low for separate I/O operation.

intel®

8102A-4

1024 BIT FULLY DECODED STATIC MOS
RANDOM ACCESS MEMORY

- **Access Time — 450 ns Max.**
- **Single +5 Volts Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**

- **Simple Memory Expansion — Chip Enable Input**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 16 Pin Plastic Dual-In-Line Configuration**

The Intel®8102A-4 is a 1024 word by one bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 8102A-4 is designed for microcomputer memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel 8102A-4 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

PIN CONFIGURATION   LOGIC SYMBOL   BLOCK DIAGRAM
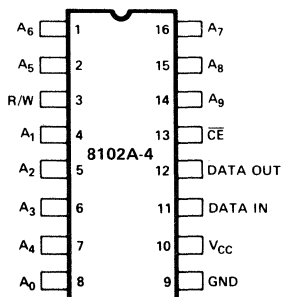
PIN NAMES

D_{IN}	DATA INPUT	$\overline{CE}$	CHIP ENABLE
A_0- A_9	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias $-10°C$ to $80°C$

Storage Temperature $-65°C$ to $+150°C$

Voltage On Any Pin
  With Respect To Ground $-0.5V$ to $+7V$

Power Dissipation   1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.[1]	MAX.		
I_{LI}	INPUT LOAD CURRENT (ALL INPUT PINS)			10	μA	$V_{IN} = 0$ to 5.25V
I_{LOH}	OUTPUT LEAKAGE CURRENT			5	μA	$\overline{CE} = 2.0V$, $V_{OUT} = 2.4$ to V_{CC}
I_{LOL}	OUTPUT LEAKAGE CURRENT			-10	μA	$\overline{CE} = 2.0V$, $V_{OUT} = 0.4V$
I_{CC1}	POWER SUPPLY CURRENT		30	50	mA	ALL INPUTS = 5.25V DATA OUT OPEN $T_A = 25°C$
I_{CC2}	POWER SUPPLY CURRENT			55	mA	ALL INPUTS = 5.25V DATA OUT OPEN $T_A = 0°C$
V_{IL}	INPUT "LOW" VOLTAGE	-0.5		0.8	V	
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V_{CC}	V	
V_{OL}	OUTPUT "LOW" VOLTAGE			0.4	V	$I_{OL} = 2.1mA$
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.4			V	$I_{OH} = -100\mu A$

(1)   Typical values are for $T_A = 25°C$ and nominal supply voltage.

TYPICAL D.C. CHARACTERISTICS

POWER SUPPLY CURRENT VS.
AMBIENT TEMPERATURE

POWER SUPPLY CURRENT VS.
SUPPLY VOLTAGE

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit
READ CYCLE					
t_{RC}	Read Cycle	450			ns
t_A	Access Time			450	ns
t_{CO}	Chip Enable to Output Time			230	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns
WRITE CYCLE					
t_{WC}	Write Cycle	450			ns
t_{AW}	Address to Write Setup Time	20			ns
t_{WP}	Write Pulse Width	300			ns
t_{WR}	Write Recovery Time	0			ns
t_{DW}	Data Setup Time	300			ns
t_{DH}	Data Hold Time	0			ns
t_{CW}	Chip Enable to Write Setup Time	300			ns

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CONDITIONS OF TEST

Input Pulse Levels: 0.8 Volt to 2.0 Volt
Input Rise and Fall Times: 10nsec
Timing Measurement Inputs: 1.5 Volts
Reference Levels Output: 0.8 and 2.0 Volts
Output Load: 1 TTL Gate and C_L = 100 pF

CAPACITANCE [2] T_A = 25°C, f = 1 MHz

SYMBOL	TEST	TYP.[1]	MAX.
		LIMITS (pF)	
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

NOTE: 2. This parameter is periodically sampled and is not 100% tested.

WAVEFORMS

READ CYCLE

① 1.5 VOLTS
② 2.0 VOLTS
③ 0.8 VOLTS
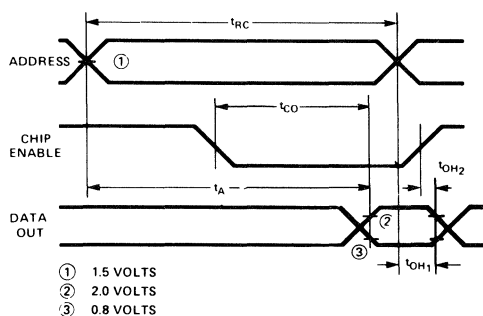
WRITE CYCLE
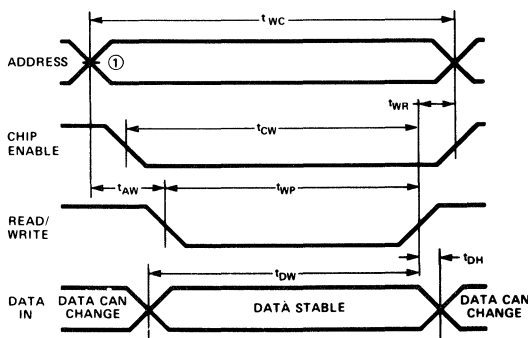
TYPICAL D.C. AND A.C. CHARACTERISTICS

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE
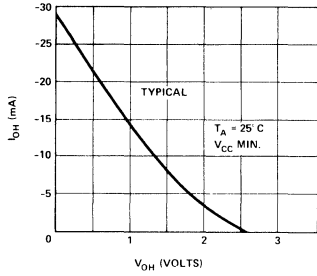
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE
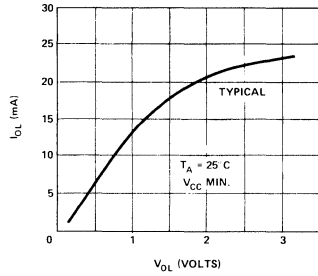
V_{IN} LIMITS VS. TEMPERATURE
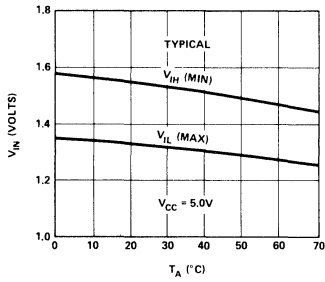
ACCESS TIME VS. V_{CC} NORMALIZED TO V_{CC} = 5.0V

ACCESS TIME VS. AMBIENT TEMPERATURE

ACCESS TIME VS. LOAD CAPACITANCE

intel®
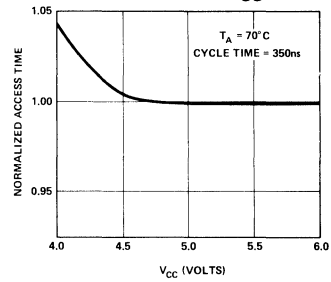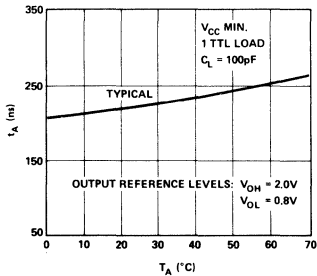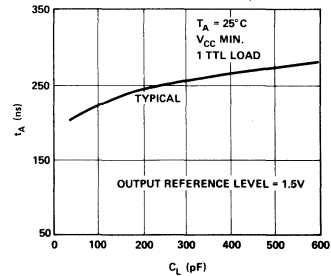
8111A-4
1024 BIT STATIC MOS RAM
WITH COMMON I/O

* 450 nsec Access Time Maximum
* 256 Word by 4 Bit Organization

- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Static MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**

- **Powerful Output Drive Capability**
- **Low Cost Packaging: 18 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150mW**
- **Three-State Output: OR-Tie Capability**
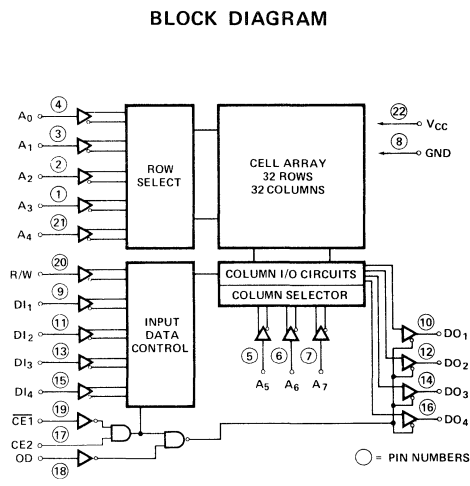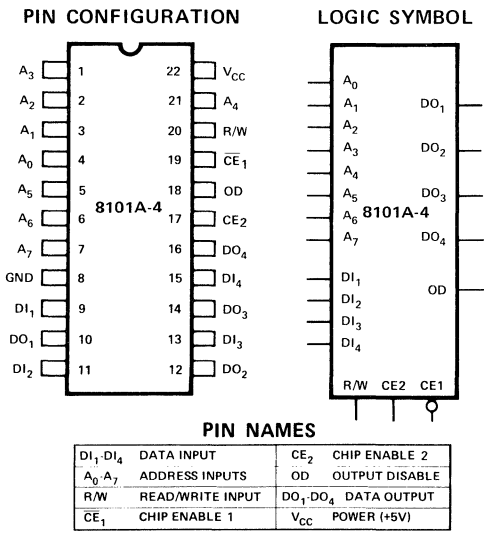- **Output Disable Provided for Ease of Use in Common Data Bus Systems**

The Intel® 8111A-4 is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 8111A-4 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

The Intel® 8111A-4 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION

A_3	1	18	V_{CC}
A_2	2	17	A_4
A_1	3	16	R/W
A_0	4	15	$\overline{CE}_1$
A_5	5	14	I/O_4
A_6	6	13	I/O_3
A_7	7	12	I/O_2
GND	8	11	I/O_1
OD	9	10	$\overline{CE}_2$

8111A-4

LOGIC SYMBOL
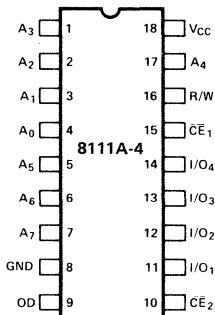
BLOCK DIAGRAM

PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT
$\overline{CE}_1$	CHIP ENABLE 1
$\overline{CE}_2$	CHIP ENABLE 2
I/O_1- I/O_4	DATA INPUT/OUTPUT

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . –10°C to 80°C

Storage Temperature . . . . –65°C to +150°C

Voltage On Any Pin
  With Respect to Ground . . . . –0.5V to +7V

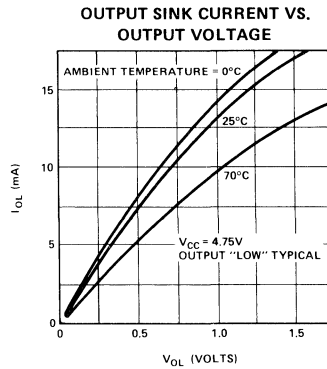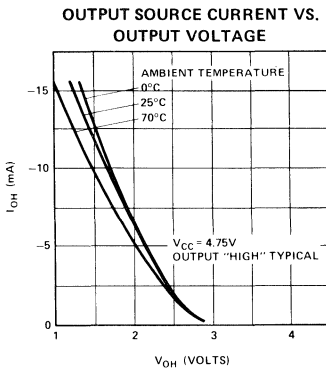Power Dissipation . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to 70°C, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10	μA	$V_{IN} = 0$ to 5.25V
I_{LOH}	I/O Leakage Current		1	10	μA	Output Disabled, $V_{I/O} = 4.0V$
I_{LOL}	I/O Leakage Current		–1	–10	μA	Output Disabled, $V_{I/O} = 0.45V$
I_{CC1}	Power Supply Current		35	55	mA	$V_{IN} = 5.25V$ $I_{I/O} = 0mA, T_A = 25°C$
I_{CC2}	Power Supply Current			60	mA	$V_{IN} = 5.25V$ $I_{I/O} = 0mA, T_A = 0°C$
V_{IL}	Input Low Voltage	–0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.0mA$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400\mu A$

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE

OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.

A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	(See Below)
t_{DF} [2]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	(See Below)
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

A.C. CONDITIONS OF TEST

t_r, t_f .... 20 ns
Input Levels .... 0.8V or 2.0V
Timing Reference 1.5V
Load .... 1 TTL Gate and $C_L = 100$ pF

CAPACITANCE [3] $T_A = 25°C$, $f = 1$ MHz

Symbol	Test	Limits (pF) Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O} = 0V$	10	15

WAVEFORMS

READ CYCLE
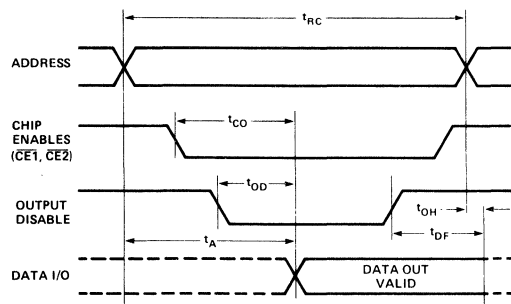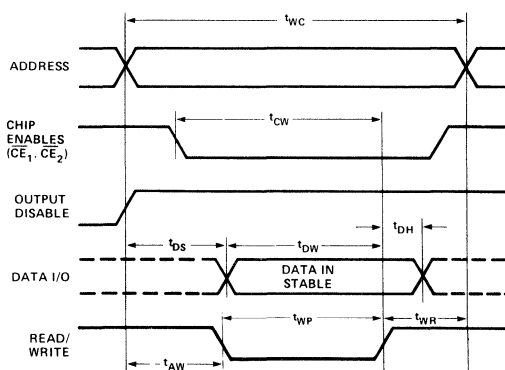
WRITE CYCLE

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.
3. This parameter is periodically sampled and is not 100% tested.

intel®

5101 FAMILY
256 X 4 BIT STATIC CMOS RAM

P/N	Typ. Current @ 2V (µA)	Typ. Current @ 5V (µA)	Max Access (ns)
5101L	0.14	0.2	650
5101L-1	0.14	0.2	450
5101L-3	0.70	1.0	650
5101-8	——	10.0	800

- **Single +5V Power Supply**
- **Ideal for Battery Operation (5101L)**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Three-State Output**

The Intel® 5101 is an ultra-low power 1024-bit (256 words X 4 bits) static RAM fabricated with an advanced ion-implanted silicon gate CMOS technology. The device has two chip enable inputs. Minimum standby current is drawn by this device when CE2 is at a low level. When deselected the 5101 draws from the single 5-volt supply only 10 microamps. This device is ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

The 5101 uses fully DC stable (static) circuitry; it is not necessary to pulse chip select for each address transition. The data is read out non-destructively and has the same polarity as the input data. All inputs and outputs are directly TTL compatible. The 5101 has separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire OR-ed for use in common data I/O systems.

The 5101L has the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.

A pin compatible N-channel static RAM, the Intel® 2101A, is also available for low cost applications where a 256 X 4 organization is needed.

The Intel ion-implanted, silicon gate, Complementary MOS (CMOS) process allows the design and production of ultra-low power, high performance memories.

PIN CONFIGURATION

LOGIC SYMBOL

BLOCK DIAGRAM

○ = PIN NUMBERS

TRUTH TABLE

$\overline{CE}_1$	CE₂	OD	R/W	D$_{IN}$	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D$_{IN}$	Write
L	H	L	H	X	D$_{OUT}$	Read

Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . . . –10°C to 80°C

Storage Temperature . . . . –65°C to +150°C

Voltage On Any Pin

   With Respect to Ground . . . . –0.3V to V_{CC} +0.3V

Maximum Power Supply Voltage . . . . +7.0V

Power Dissipation . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
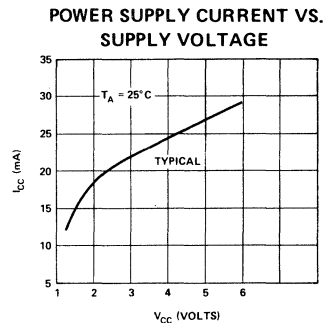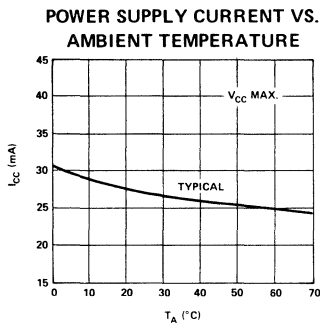
D. C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	5101L and 5101L-1 Limits Min.	Typ.[1]	Max.	5101L-3 Limits Min.	Typ.[1]	Max.	5101-8 Limits Min.	Typ.[1]	Max.	Units	Test Conditions
I_{L2}[2]	Input Current		5			5			5		nA	
I_{LO}[2]	Output Leakage Current			1			1			2	µA	$\overline{CE1}$=2.2V, V_{OUT}= 0 to V_{CC}
I_{CC1}	Operating Current		9	22		9	22		11	25	mA	$V_{IN}=V_{CC}$, Except $\overline{CE1}$ ⩽ 0.65V, Outputs Open
I_{CC2}	Operating Current		13	27		13	27		15	30	mA	V_{IN}=2.2V, Except $\overline{CE1}$ ⩽ 0.65V, Outputs Open
I_{CCL}[2]	Standby Current			10			200			500	µA	CE2 ⩽ 0.2V, T_A= 70°C
V_{IL}	Input Low Voltage	-0.3		0.65	-0.3		0.65	-0.3		0.65	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.4	V	I_{OL}=2.0 mA
V_{OH}	Output High Voltage	2.4			2.4			2.4			V	I_{OH}= –1.0 mA

Low V_{CC} Data Retention Characteristics (For 5101L, 5101L-1 and 5101L-3) T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V		
I_{CCDR1}	5101L or 5101L-1 Data Retention Current		0.14	10	µA	CE2 ⩽ 0.2V	V_{DR}=2.0V, T_A=70°C
I_{CCDR2}	5101L-3 Data Retention Current		0.70	200	µA		V_{DR}=2.0V, T_A=70°C
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[3]			ns		

NOTES:

1. Typical values are T_A = 25°C and nominal supply voltage.
2. Current through all inputs and outputs included in I_{CCL} measurement.
3. t_{RC} = Read Cycle Time.

Low V$_{CC}$ Data Retention Waveform

① 4.75V
② V$_{DR}$
③ V$_{IH}$
④ 0.2V
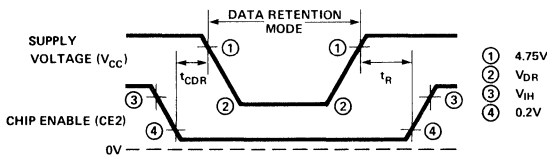
Typical I$_{CCDR}$ Vs. Temperature
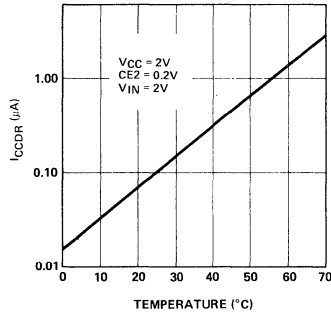
A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

READ CYCLE

Symbol	Parameter	5101L-1 Limits (ns) Min.	Max.	5101L and 5101L-3 Limits (ns) Min.	Max.	5101-8 Limits (ns) Min.	Max.
t$_{RC}$	Read Cycle	450		650		800	
t$_A$	Access Time		450		650		800
t$_{CO1}$	Chip Enable ($\overline{CE\ 1}$) to Output		400		600		800
t$_{CO2}$	Chip Enable (CE 2) to Output		500		700		850
t$_{OD}$	Output Disable to Output		250		350		450
t$_{DF}$	Data Output to High Z State	0	130	0	150	0	200
t$_{OH1}$	Previous Read Data Valid with Respect to Address Change	0		0		0	
t$_{OH2}$	Previous Read Data Valid with Respect to Chip Enable	0		0		0	

WRITE CYCLE

Symbol	Parameter	5101L-1 Min.	Max.	5101L and 5101L-3 Min.	Max.	5101-8 Min.	Max.
t$_{WC}$	Write Cycle	450		650		800	
t$_{AW}$	Write Delay	130		150		200	
t$_{CW1}$	Chip Enable ($\overline{CE\ 1}$) to Write	350		550		650	
t$_{CW2}$	Chip Enable (CE 2) to Write	350		550		650	
t$_{DW}$	Data Setup	250		400		450	
t$_{DH}$	Data Hold	50		100		100	
t$_{WP}$	Write Pulse	250		400		450	
t$_{WR}$	Write Recovery	50		50		100	
t$_{DS}$	Output Disable Setup	130		150		200	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20 nsec

Timing Measurement Reference Level: 1.5 Volt

Output Load: 1 TTL Gate and C$_L$ = 100 pF

Capacitance [2] $T_A = 25°C$, f = 1 MHz

Symbol	Test	Limits (pF) Typ.	Max.
C$_{IN}$	Input Capacitance (All Input Pins) V$_{IN}$ = 0V	4	8
C$_{OUT}$	Output Capacitance V$_{OUT}$ = 0V	8	12

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
        2. This parameter is periodically sampled and is not 100% tested.
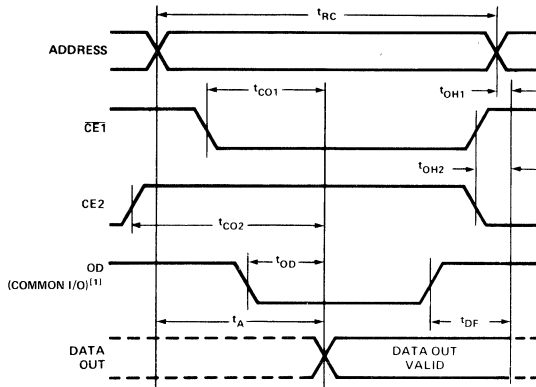
Waveforms

READ CYCLE

WRITE CYCLE

NOTES:
1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

intel®
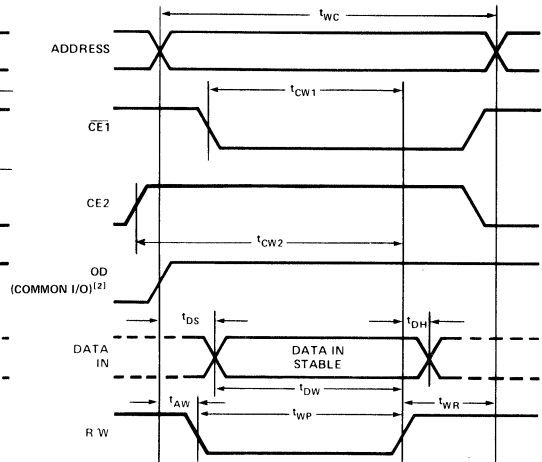
M5101-4, M5101L-4
256 x 4 BIT STATIC CMOS RAM

- **Military Temperature Range: −55°C to +125°C**
- **Ultra Low Standby Current: 200 nA/Bit**

- **Fast Access Time—800ns**
- **Single +5V Power Supply**
- **CE2 Controls Unconditional Standby Mode**
- **Three-State Output**

The Intel® M5101 is an ultra-low power 256 × 4 CMOS RAM specified over the −55°C to +125°C temperature range. The RAM uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. When deselected with CE2 low, the M5101 draws from the single 5-volt supply only 200 microamps at 125°C.

The Intel® M5101 is fabricated with an ion-implanted, silicon gate, Complementary MOS (CMOS) process. This technology allows the design and production of ultra-low power, high performance memories.

PIN CONFIGURATION
5101

A_3	1		22	V_{CC}
A_2	2		21	A_4
A_1	3		20	R/W
A_0	4		19	CE1
A_5	5		18	OD
A_6	6		17	CE2
A_7	7		16	DO_4
GND	8		15	DI_4
DI_1	9		14	DO_3
DO_1	10		13	DI_3
DI_2	11		12	DO_2

LOGIC SYMBOL
5101

Inputs: A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, DI_1, DI_2, DI_3, DI_4, OD, R/W, CE2, CE1
Outputs: DO_1, DO_2, DO_3, DO_4
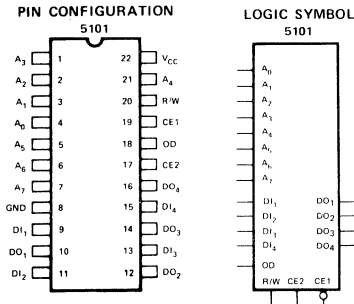
PIN NAMES

DI_1, DI_4	DATA INPUT	OD	OUTPUT DISABLE
A_0 – A_7	ADDRESS INPUTS	DO_1 – DO_4	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
CE1, CE2	CHIP ENABLE		

Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . −65°C to 135°C
Storage Temperature . . . . −65°C to +150°C
Voltage On Any Pin
    With Respect to Ground . . . . −0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage . . . . +7.0V
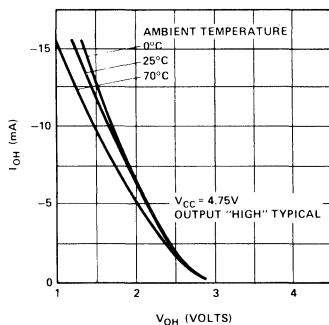Power Dissipation . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
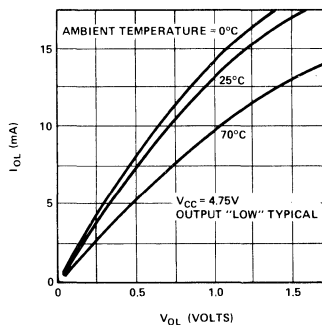
D. C. and Operating Characteristics for M5101-4, M5101L-4

T_A = −55°C to 125°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}[2]	Input Current		8		nA	V_{IN} = 0 to 5.25V
I_{LOH}[2]	Output High Leakage			2	µA	$\overline{CE1}$=2.2V, V_{OUT} = V_{CC}
I_{LOL}[2]	Output Low Leakage			2	µA	$\overline{CE1}$=2.2V, V_{OUT}=0.0V
I_{CC1}	Operating Current		11	25	mA	V_{IN} = V_{CC} Except $\overline{CE1}$ ⩽0.01V Outputs Open
I_{CC2}	Operating Current		20	32	mA	V_{IN} =2.2V Except $\overline{CE1}$ ⩽0.5V Outputs Open
I_{CCL}[2]	Standby Current		2	200	µA	V_{IN} =0 to V_{CC}, Except CE2 ⩽ 0.2V
V_{IL}	Input "Low" Voltage	−0.3		0.5	V	
V_{IH}	Input "High" Voltage	V_{CC}−2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	V_{CC}−2.0			V	I_{OH} = 1.0mA

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage.   2. Current through all inputs and outputs included in I_{CCL}.

Low V$_{CC}$ Data Retention Characteristics (For M5101L-4) T$_A$ = –55°C to 125°C

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions	
V$_{DR}$	V$_{CC}$ for Data Retention	2.0			V	CE2 ≤ 0.2V	V$_{DR}$ = 2.0V
I$_{CCDR}$	Data Retention Current		2	200	µA		
t$_{CDR}$	Chip Deselect to Data Retention Time	0			ns		
t$_R$	Operation Recovery Time	t$_{RC}$[2]			ns		

NOTES: 1. Typical values are T$_A$ = 25°C and nominal supply voltage.
         2. t$_{RC}$ = Read Cycle Time.

A.C. Characteristics for M5101-4, M5101L-4

READ CYCLE T$_A$ = –55°C to 125°C, V$_{CC}$ = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t$_{RC}$	Read Cycle	800			ns	
t$_A$	Access Time			800	ns	
t$_{CO1}$	Chip Enable ($\overline{CE1}$) to Output			700	ns	
t$_{CO2}$	Chip Enable (CE2) to Output			850	ns	(See below)
t$_{OD}$	Output Disable To Output			350	ns	
t$_{DF}$	Data Output to High Z State	0		150	ns	
t$_{OH1}$	Previous Read Data Valid with Respect to Address Change	0			ns	
t$_{OH2}$	Previous Read Data Valid with Respect to Chip Enable	0			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t$_{WC}$	Write Cycle	800			ns	
t$_{AW}$	Write Delay	150			ns	
t$_{CW1}$	Chip Enable ($\overline{CE1}$) To Write	550			ns	
t$_{CW2}$	Chip Enable (CE2) To Write	550			ns	(See below)
t$_{DW}$	Data Setup	400			ns	
t$_{DH}$	Data Hold	100			ns	
t$_{WP}$	Write Pulse	400			ns	
t$_{WR}$	Write Recovery	50			ns	
t$_{DS}$	Output Disable Setup	150			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: 0.5 Volt to V$_{CC}$–2.0 Volt

Input Pulse Rise and Fall Times: 20 nsec

Timing Measurement Reference Level: 1.5 Volt

Output Load: 1 TTL Gate and C$_L$ = 100 pF

Capacitance[3] T$_A$ = 25°C, f = 1 MHz

Symbol	Test	Limits (pF)	
		Typ.	Max.
C$_{IN}$	Input Capacitance (All Input Pins) V$_{IN}$ = 0V	4	8
C$_{OUT}$	Output Capacitance V$_{OUT}$ = 0V	8	12

NOTE: 3. This parameter is periodically sampled and is not 100% tested.
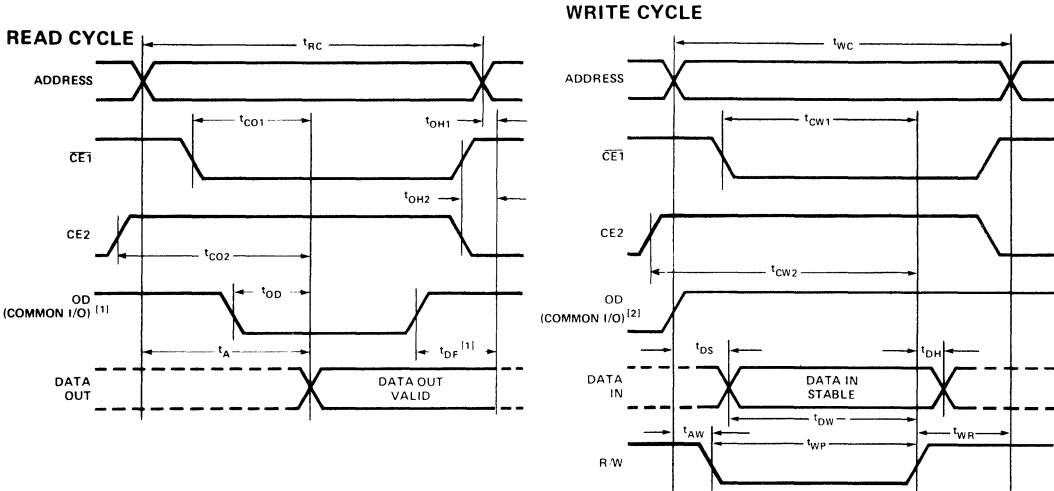
Waveforms

READ CYCLE

WRITE CYCLE

NOTES: 1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

Low V$_{CC}$ Data Retention

①	4.75V
②	V$_{DR}$
③	V$_{IH}$
④	0.2V
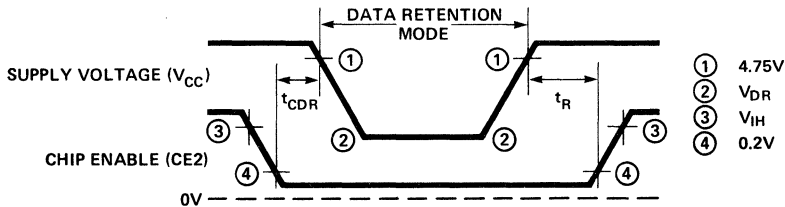
2114
1024 X 4 BIT STATIC RAM

	2114-2	2114-3	2114	2114L3	2114L
Max. Access Time (ns)	200	300	450	300	450
Max. Power Dissipation (mw)	710mw	710mw	710mw	370mw	370mw

- **High Density 18 Pin Package**
- **Identical Cycle and Access Times**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**

- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **Pin-Out Compatible with 3605 and 3625 Bipolar PROMs**

The Intel® 2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The 2114 is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

The 2114 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

PIN CONFIGURATION   **LOGIC SYMBOL**   **BLOCK DIAGRAM**
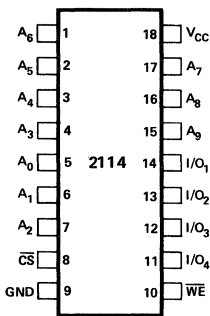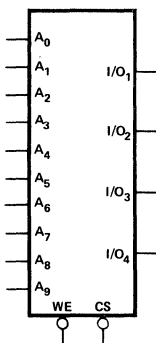
PIN NAMES

A_0-A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
$I/O_1-I/O_4$	DATA INPUT/OUTPUT	
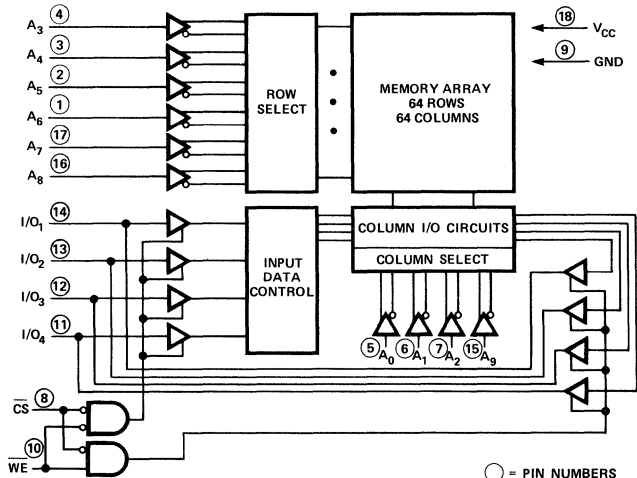
PRELIMINARY

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . -10°C to 80°C

Storage Temperature . . . . -65°C to $+150^\circ$C

Voltage on Any Pin

  With Respect to Ground . . . . -0.5V to $+7$V

Power Dissipation 1.0W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0^\circ$C to 70°C, $V_{CC} = 5$V $\pm 5\%$, unless otherwise noted.

SYMBOL	PARAMETER	2114-2, 2114-3, 2114			2114L3, 2114L			UNIT	CONDITIONS
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{LI}	Input Load Current (All Input Pins)			10			10	μA	$V_{IN} = 0$ to 5.25V
$|I_{LO}|$	I/O Leakage Current			10			10	μA	$\overline{CS} = 2.4$V, $V_{I/O} = 0.4$V to V_{CC}
I_{CC1}	Power Supply Current		80	120			65	mA	$V_{IN} = 5.25$V, $I_{I/O} = 0$ mA, $T_A = 25^\circ$C
I_{CC2}	Power Supply Current		90	135			70	mA	$V_{IN} = 5.25$V, $I_{I/O} = 0$ mA, $T_A = 0^\circ$C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}	2.4		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V_{CC}	2.4		V_{CC}	V	$I_{OH} = -1.0$ mA

CAPACITANCE

$T_A = 25^\circ$C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O} = 0$V
C_{IN}	Input Capacitance	5	pF	$V_{IN} = 0$V

NOTE: This parameter is periodically sampled and not 100% tested.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	2114-2 Min.	2114-2 Max.	2114-3, 2114L3 Min.	2114-3, 2114L3 Max.	2114, 2114L Min.	2114, 2114L Max.	UNIT
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{CO}	Chip Selection to Output Valid		70		100		100	ns
t_{CX}	Chip Selection to Output Active	0		0		0		ns
t_{OTD}	Output 3–state from Deselection	0	40	0	80	0	100	ns
t_{OHA}	Output Hold from Address Change	10		10		10		ns

WRITE CYCLE [2]

SYMBOL	PARAMETER	2114-2 Min.	2114-2 Max.	2114-3, 2114L3 Min.	2114-3, 2114L3 Max.	2114, 2114L Min.	2114, 2114L Max.	UNIT
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Time	100		150		200		ns
t_{WR}	Write Release Time	20		0		0		ns
t_{OTW}	Output 3–state from Write	0	40	0	80	0	100	ns
t_{DW}	Data to Write Time Overlap	100		150		200		ns
t_{DH}	Data Hold From Write Time	0		0		0		ns

NOTES: 1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

A.C. CONDITIONS OF TEST

Input Pulse Levels . . . . 0.8 Volt to 2.4 Volt

Input Rise and Fall Times . . . . 10 nsec

Input and Output Timing Levels . . . . 1.5 Volts

Output Load . . . . 1 TTL Gate and $C_L = 50$ pF

PRELIMINARY

WAVEFORMS
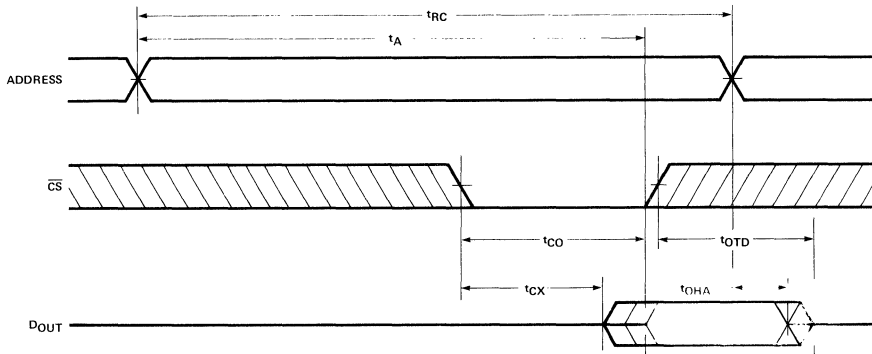
READ CYCLE ①

WRITE CYCLE
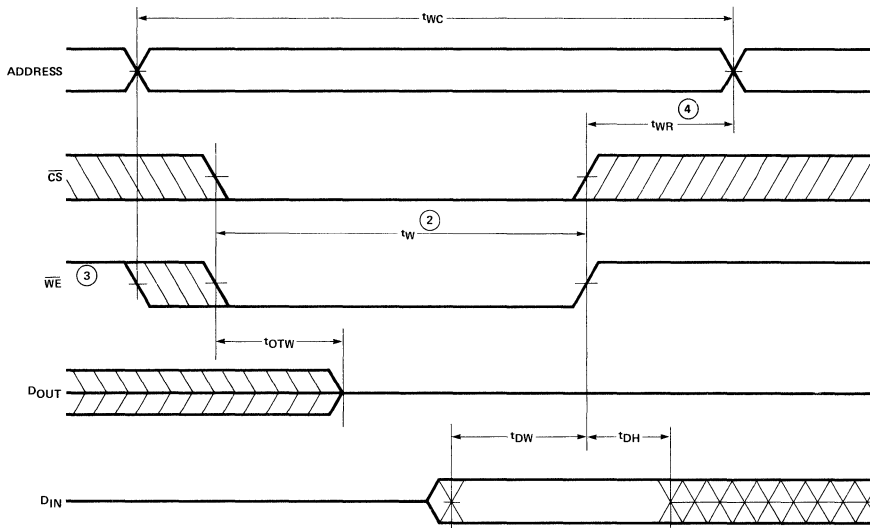
NOTES:
① $\overline{WE}$ is high for a Read Cycle.
② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to $\overline{WE}$ going high.
③ $\overline{WE}$ must be high during all address transitions.
④ t_{WR} is referenced to the high transition of $\overline{WE}$.

DATA STORAGE

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{WE}$ remains high, the data stored cannot be affected by the address, Chip Select, or data I/O voltage levels and timing transitions. The block diagram also shows data storage cannot be affected by $\overline{WE}$, the addresses, nor the I/O ports as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ by itself — or in conjunction with the other — can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during a Write time — defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. To prevent the loss of data, the addresses must be properly established during the entire Write time plus t_{WR}.

Internal delays on the 2114 are established such that address decoding propagates ahead of data inputs (keyed by the Write time). Therefore, it is permissable to establish the addresses coincident to the selection of a Write time, but no later. If the Write time precedes the addresses, the data in the previously addressed locations, or some other location, may be inadvertently changed.

While it is important that the addresses remain stable for the entire Write cycle, the data inputs are not required to remain stable. Appropriate voltage levels will be written into the cells as long as the data is stable for t_{DW} at the end of the Write time.

intel®

2142
1024 X 4 BIT STATIC RAM

	2142-2	2142-3	2142	2142L2	2142L3	2142L
Max. Access Time (ns)	200	300	450	200	300	450
Max. Power Dissipation (mw)	525	525	525	370	370	370

- **High Density 20 Pin Package**
- **Access Time Selections From 200-450ns**
- **Identical Cycle and Access Times**
- **Low Operating Power Dissipation .1mW/Bit Typical**
- **Single +5V Supply**

- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**

The Intel® 2142 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2142 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply.

The 2142 is placed in a 20-pin package. Two Chip Selects ($\overline{CS}_1$ and CS_2) are provided for easy and flexible selection of individual packages when outputs are OR-tied. An Output Disable is included for direct control of the output buffers.

The 2142 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

PIN CONFIGURATION   LOGIC SYMBOL
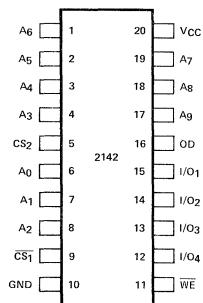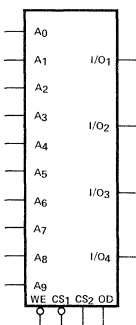
BLOCK DIAGRAM

PIN NAMES

A_0–A_9	ADDRESS INPUTS	OD	OUTPUT DISABLE
$\overline{WE}$	WRITE ENABLE	VCC	POWER (+5V)
$\overline{CS}_1$, CS_2	CHIP SELECT	GND	GROUND
I/O_1–I/O_4	DATA INPUT/OUTPUT		

ADVANCE INFORMATION

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... -10°C to 80°C
Storage Temperature ....-65°C to $+150^{\circ}$C
Voltage on Any Pin
  With Respect to Ground .... -0.5V to $+7$V
Power Dissipation 1.0W
D.C. Output Current 10mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0^{\circ}$C to 70°C, $V_{CC} = 5$V $\pm 5\%$, unless otherwise noted.

SYMBOL	PARAMETER	2142-2, 2142-3, 2142			2142L2, 2142L3, 2142L			UNIT	CONDITIONS
		Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins)			10			10	μA	$V_{IN} = 0$ to 5.25V
$|I_{LO}|$	I/O Leakage Current			10			10	μA	$\overline{CS} = 2.4$V, $V_{I/O} = 0.4$V to V_{CC}
I_{CC1}	Power Supply Current		80	95			65	mA	$V_{IN} = 5.25$V, $I_{I/O} = 0$ mA, $T_A = 25^{\circ}$C
I_{CC2}	Power Supply Current			100			70	mA	$V_{IN} = 5.25$V, $I_{I/O} = 0$ mA, $T_A = 0^{\circ}$C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	2.1	6.0		2.1	6.0		mA	$V_{OL} = 0.4$V
I_{OH}	Output High Current		-1.4	-1.0		-1.4	-1.0	mA	$V_{OH} = 2.4$V
I_{OS}[2]	Output Short Circuit Current			40			40	mA	$V_{I/O} =$ GND to V_{CC}

NOTE: 1. Typical values are for $T_A = 25^{\circ}$C and $V_{CC} = 5.0$V.
       2. Duration not to exceed 30 seconds.

CAPACITANCE

$T_A = 25^{\circ}$C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O} = 0$V
C_{IN}	Input Capacitance	5	pF	$V_{IN} = 0$V

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels .... 0.8 Volt to 2.4 Volt

Input Rise and Fall Times .... 10 nsec

Input and Output Timing Levels .... 1.5 Volts

Output Load .... 1 TTL Gate and $C_L = 100$ pF

ADVANCE INFORMATION

Characteristics are subject to change without notice

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	2142-2, 2142L2 Min. Max.		2142-3, 2142L3 Min. Max.		2142, 2142L Min. Max.		UNIT
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{OD}	Output Enable to Output Valid		70		100		120	ns
t_{ODX}	Output Enable to Output Active	20		20		20		ns
t_{CO}	Chip Selection to Output Valid		70		100		120	ns
t_{CX}	Chip Selection to Output Active	20		20		20		ns
t_{OTD}	Output 3-state from Disable		60		80		100	ns
t_{OHA}	Output Hold from Address Change	50		50		50		ns

WRITE CYCLE [2]

SYMBOL	PARAMETER	2142-2, 2142L2 Min. Max.		2142-3, 2142L3 Min. Max.		2142, 2142L Min. Max.		UNIT
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Time	120		150		200		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTD}	Output 3-state from Disable		60		80		100	ns
t_{DW}	Data to Write Time Overlap	120		150		200		ns
t_{DH}	Data Hold From Write Time	0		0		0		ns

NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

WAVEFORMS

READ CYCLE [3]
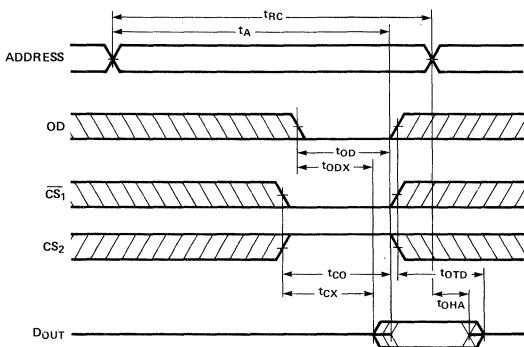
WRITE CYCLE

NOTES:
3. $\overline{WE}$ is high for a Read Cycle.
4. $\overline{WE}$ must be high during all address transitions.

TYPICAL D.C. AND A.C. CHARACTERISTICS

ADVANCE INFORMATION

NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE
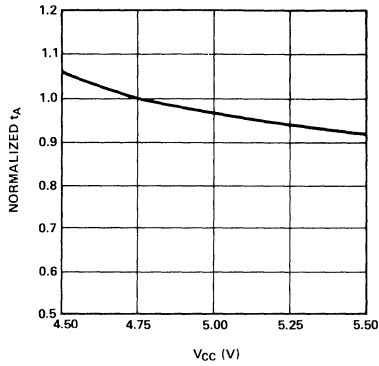
NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE
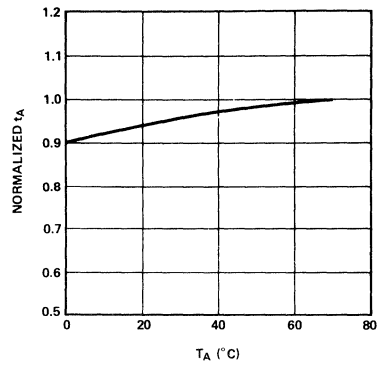
NORMALIZED ACCESS TIME VS.
OUTPUT LOAD CAPACITANCE
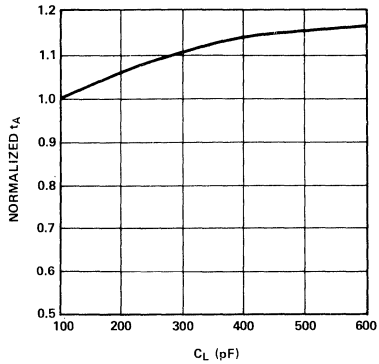
NORMALIZED POWER SUPPLY CURRENT
VS. AMBIENT TEMPERATURE
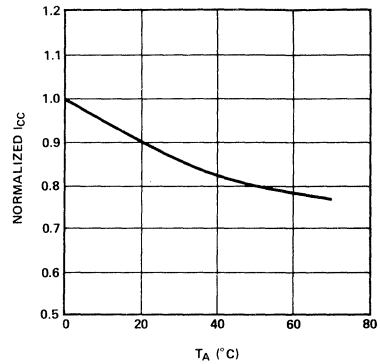
OUTPUT SOURCE CURRENT
VS. OUTPUT VOLTAGE

OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE

intel®
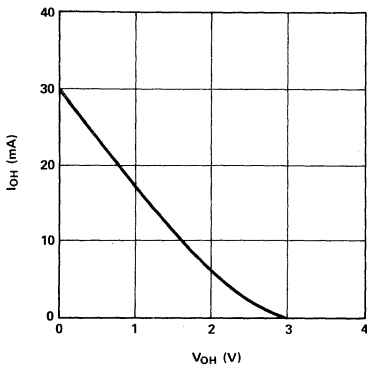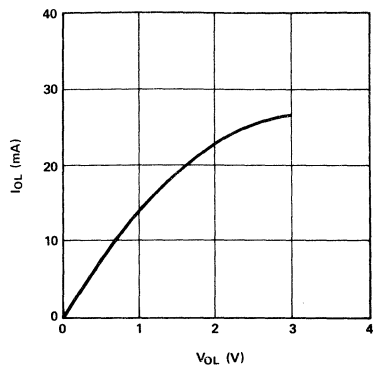
2104A FAMILY
4096 x 1 BIT DYNAMIC RAM

	2104A-1	2104A-2	2104A-3	2104A-4
Max. Access Time (ns)	150	200	250	300
Read, Write Cycle (ns)	320	320	375	425
Max. IDD (mA)	35	32	30	30

- **Highest Density 4K RAM Industry Standard 16 Pin Package**
- **Low Power 4K RAM**
- **All Inputs Including Clocks TTL Compatible**
- **±10% Tolerance on All Power Supplies +12V, +5V, -5V**

- **Refresh Period: 2 ms**
- **On-Chip Latches for Addresses, Chip Select and Data In**
- **Simple Memory Expansion: Chip Select**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**
- **Compatible with Intel® 2116 16K RAM**

The Intel® 2104A is a 4096 word by 1 bit MOS RAM fabricated with N-channel silicon gate technology for high performance and high functional density.

The efficient design of the 2104A allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2104A on 6 address input pins. The two 6 bit address words are latched into the 2104A by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

A new unique dynamic storage cell provides high speed along with low power dissipation and wide voltage margins. The memory cell requires refreshing for data retention. Refreshing is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2 milliseconds.

The 2104A is designed for page mode operation, "$\overline{RAS}$-only refreshing," and "$\overline{CAS}$-only deselection." Thus it is compatible with the Intel® 2116, 16K RAM.

PIN CONFIGURATION   LOGIC DIAGRAM   BLOCK DIAGRAM
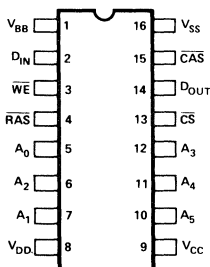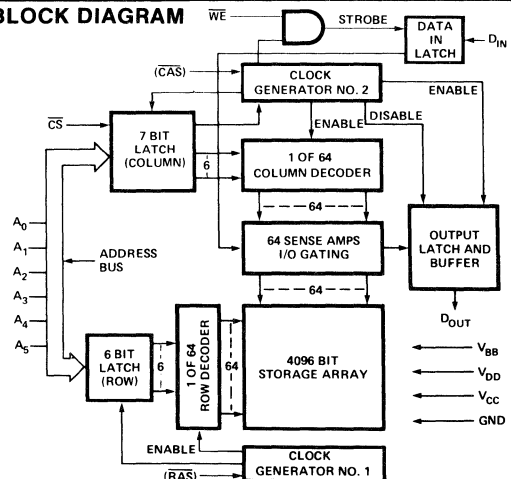
PIN NAMES

$A_0 \cdot A_5$	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... $-10°$C to $+80°$C
Storage Temperature .... $-65°$C to $+150°$C
Voltage on any Pin Relative to V_{BB}
   ($V_{SS} - V_{BB} \geqslant 4.5V$) .... $-0.3V$ to $+20V$
Power Dissipation 1.0W
Data Out Current .... 50 mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

$T_A = 0°$ to $70°$C, $V_{DD} = +12V \pm 10\%$, $V_{CC} = +5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.(2)	Max.		
I_{LI}	Input Load Current (any input)			10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
$|I_{LO}|$	Output Leakage Current for High Impedance State			10	μA	Chip deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} $V_{OUT} = 0$ to 5.5V
I_{DD1} [3]	V_{DD} Standby Current		0.7	2	mA	$V_{DD} = 13.2V$ — $\overline{CAS}$ and $\overline{RAS}$ at V_{IH}. Chip deselected prior to measurement. See Note 5.
			0.7	1.5	mA	$V_{DD} = 12.6V$
I_{BB1}	V_{BB} Standby Current		5	50	μA	$V_{DD} = 13.2V$
I_{DD2} [3]	Operating V_{DD} Current (Device Selected)		24	35	mA	2104A-1 $t_{CYC} = 320$ ns
			22	32	mA	2104A-2 $t_{CYC} = 320$ ns
			20	30	mA	2104A-3, 4 $t_{CYC} = 375$ ns
I_{BB2}	Operating V_{BB} Current		160	400	μA	Device Selected. Min cycle time.
I_{CC1} [4]	V_{CC} Supply Current when Deselected			10	μA	
I_{DD3}	Operating V_{DD} Current ($\overline{RAS}$-only cycle)		12	25	mA	2104A-1, 2 $t_{CYC} = 320$ ns
			10	22	mA	2104A-3, 4 $t_{CYC} = 375$ ns
V_{IL}	Input Low Voltage (any input)	-1.0		0.8	V	
V_{IH}	Input High Voltage	2.4		7.0	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	$I_{OL} = 3.2$ mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	$I_{OH} = -5$ mA

CAPACITANCE[6] $T_A = 25°$C

Symbol	Test	Typ.	Max.	Unit	Conditions
C_{I1}	Input Capacitance $(A_0\text{-}A_5)$, D_{IN}, $\overline{CS}$	3	7	pF	$V_{IN} = V_{SS}$
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{WRITE}$	3	7	pF	$V_{IN} = V_{SS}$
C_0	Output Capacitance (D_{OUT})	4	7	pF	$V_{OUT} = 0V$
C_{I3}	Input Capacitance $\overline{CAS}$	6	7	pF	$V_{IN} = V_{SS}$

Notes:
1. All voltages referenced to V_{SS}. The only requirement for the sequence of applying voltages to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycles containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.
2. Typical values are for $T_A = 25°$C and nominal power supply voltages.
3. The I_{DD} current flows to V_{SS}.
4. When chip is selected V_{CC} supply current is dependent on output loading. V_{CC} is connected to output buffer only.
5. The chip is deselected; i.e., output is brought to high impedance state by $\overline{CAS}$-only cycle or by a read cycle with $\overline{CS}$ at V_{IH}.
6. Capacitance measured with Boonton Meter.

A.C.CHARACTERISTICS[1]

$T_A = 0°C$ to $70°C, V_{DD} = 12V \pm 10\%, V_{CC} = 5V \pm 10\%, V_{BB} = -5V \pm 10\%, V_{SS} = 0V$, unless otherwise noted.

READ, WRITE, AND READ MODIFY WRITE CYCLES

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{REF}	Time Between Refresh		2		2		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	100		115		115		125		ns
t_{CP}	$\overline{CAS}$ Precharge Time	60		80		110		110		ns
t_{RCL}[2]	$\overline{RAS}$ to $\overline{CAS}$ Leading Edge Lead Time	20	50	25	70	35	110	80	135	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	100		130		140		165		ns
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		300		ns
t_{AR}	$\overline{RAS}$ to Address or $\overline{CS}$ Hold Time	95		120		160		215		ns
t_{ASR}	Row Address Set-Up Time	0		0		0		0		ns
t_{ASC}	Column Address or $\overline{CS}$ Set-Up Time	–5		0		0		0		ns
t_{RAH}	Row Address Hold Time	20		25		35		80		ns
t_{CAH}	Column Address or $\overline{CS}$ Hold Time	45		50		50		80		ns
t_T	Rise or Fall Time		50		50		50		50	ns
t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	60	0	60	0	80	ns
t_{CAC}[3]	Access Time From $\overline{CAS}$		100		130		140		165	ns
t_{RAC}[3]	Access Time From $\overline{RAS}$		150		200		250		300	ns

READ CYCLE

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	320		320		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	150	32000	200	32000	250	32000	300	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	100		130		140		165		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns
t_{RCH}	Read Command Hold Time	0		0		0		0		ns
t_{DOH}	Data Out Hold Time	32		32		32		32		μs

WRITE CYCLE[4]

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	320		320		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	150	32000	200	32000	250	32000	300	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	100		130		140		165		ns
t_{WCS}	Write Command Set-Up Time	0		0		0		0		ns
t_{WCH}	Write Command Hold Time	55		75		75		80		ns
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	105		145		185		215		ns
t_{WP}	Write Command Pulse Width	45		55		75		80		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	100		130		140		150		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		130		140		150		ns
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns
t_{DH}	Data-In Hold Time	55		75		75		80		ns
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	105		145		185		215		ns

Notes:
1. All voltages referenced to V_{SS}. Minimum timings do not allow for t_T or skews.
2. $\overline{CAS}$ must remain at V_{IH} a minimum of t_{RCL} MIN after $\overline{RAS}$ switches to V_{IL}. To achieve the minimum guaranteed access time (t_{RAC}), $\overline{CAS}$ must switch to V_{IL} at or before t_{RCL} of $t_{RAC} - t_T - t_{CAC}$ as described in the Applications Information on page 2-45. t_{RCL} MAX is given for reference only as $t_{RAC} - t_{CAC}$.
3. Load = 2 TTL and 100 pF. See Applications Information.
4. In a write cycle D_{OUT} latch will contain data written into cell. In a read-modify-write cycle D_{OUT} latch will contain data read from cell. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} is indeterminate.

WAVEFORMS

READ CYCLE
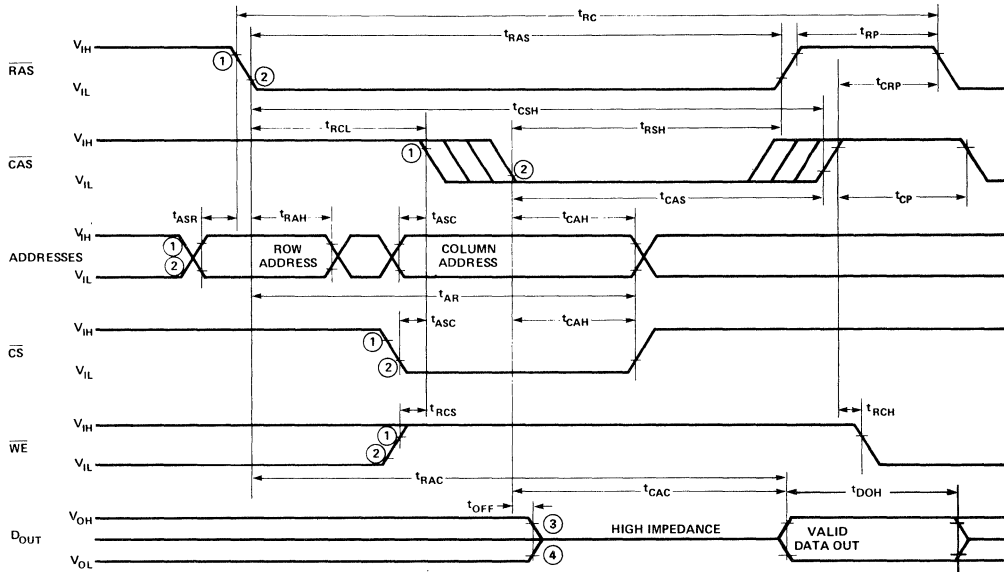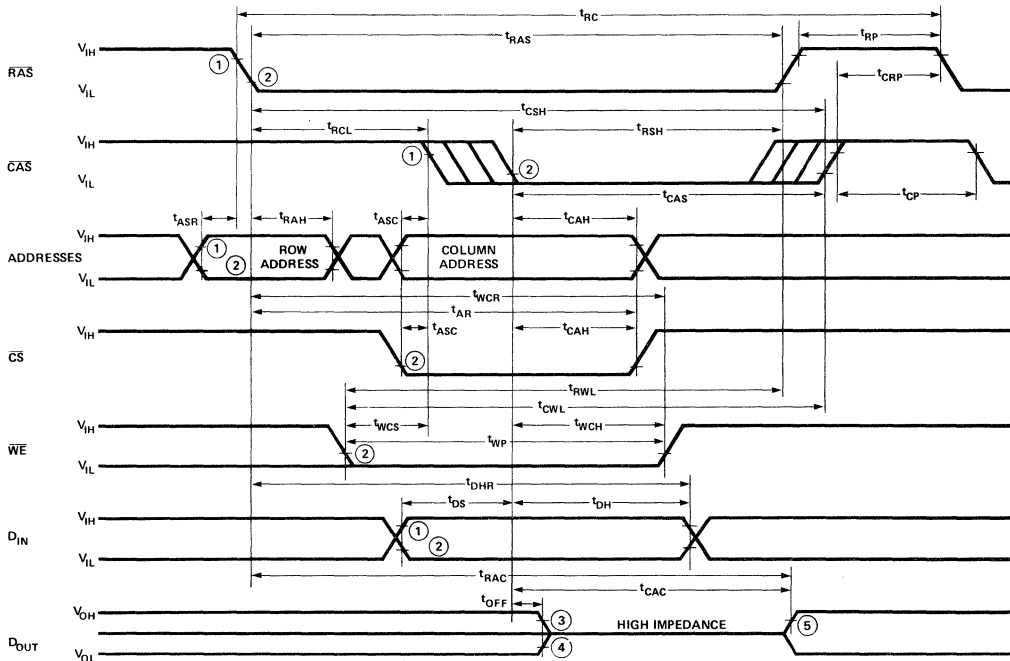
WRITE CYCLE

(See page 2-44 for notes)

A.C.CHARACTERISTICS[1]

$T_A = 0°$ to $70°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RWC}	Read Modify Write Cycle Time[2]	350		445		505		575		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	200		260		280		315		ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	250		330		390		450		ns
t_{RWL}	RMW Cycle $\overline{RAS}$ Lead Time	100		130		140		150		ns
t_{CWH}	RMW Cycle $\overline{CAS}$ Hold Time	250		330		390		450		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		130		140		150		ns
t_{WP}	Write Command Pulse Width	45		55		75		80		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns
t_{MOD}	Modify Time	0	10	0	10	0	10	0	10	μs
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns
t_{DH}	Data-In Hold Time	55		75		75		80		ns

Notes: 1. All voltages referenced to V_{SS}.
2. The minimum cycle timing does not allow for t_T or skews.

WAVEFORMS

READ-MODIFY-WRITE CYCLE
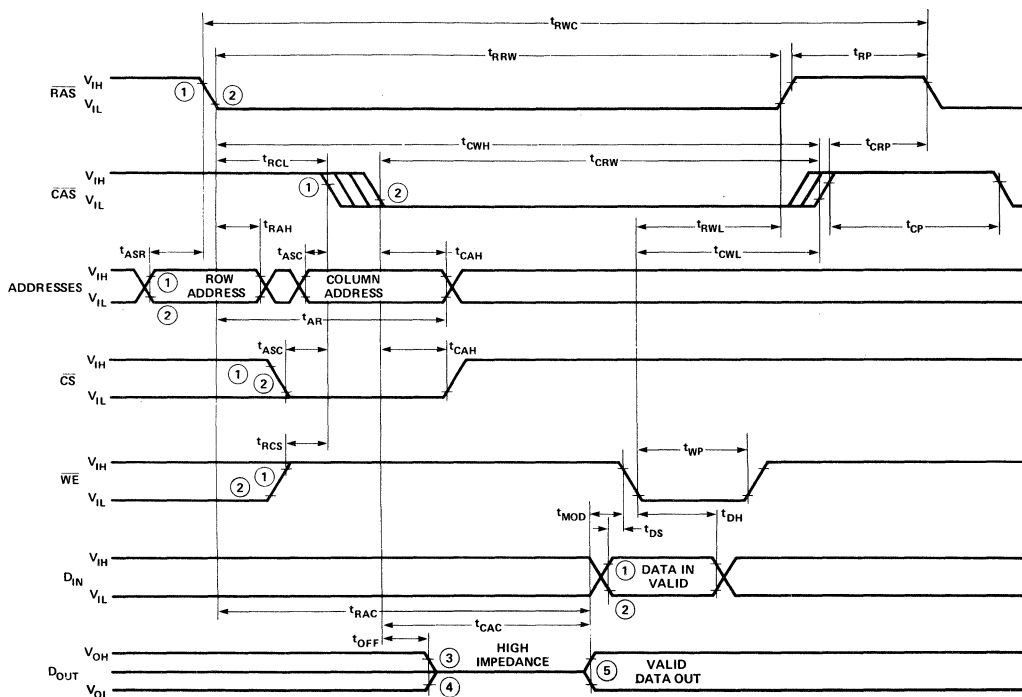
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. In a write cycle D_{OUT} latch will contain data written into cell. In a read-modify-write cycle D_{OUT} latch will contain data read from cell. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} is indeterminate.

TYPICAL CHARACTERISTICS

TYPICAL I_{BB2} AND I_{DD2} VS. TEMPERATURE

V_{DD}	= 12.0V
V_{BB}	= –5.0V
t_{CYCLE}	= 375 ns
t_{RCL}	= 60 ns
t_{RP}	= 125 ns
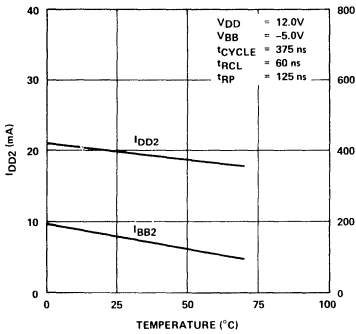
I_{DD2}

I_{BB2}

TYPICAL I_{BB2} AND I_{DD2} VS. CYCLE TIME

V_{DD}	= 12.0V
V_{BB}	= –5.0V
T_A	= 25°C
t_{CAS}	= 165 ns
t_{RCL}	= 80 ns

I_{DD2}

I_{BB2}
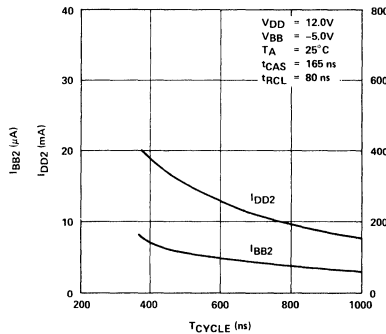
TYPICAL ACCESS TIME VS. TEMPERATURE

V_{DD}	= 10.8V
V_{BB}	= –5.5V

t_{RCL} = 110 ns

t_{RCL} = 60 ns

t_{RCL} = 25 ns
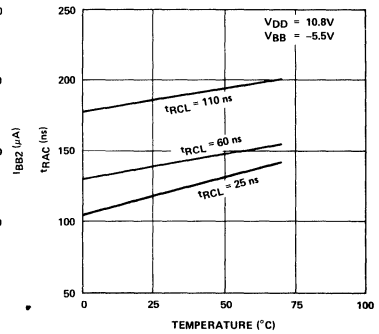
APPLICATIONS

ADDRESSING

Two externally applied negative going TTL clocks, Row Address Strobe ($\overline{RAS}$), and Column Address Strobe ($\overline{CAS}$), are used to strobe the two sets of 6 addresses into internal address buffer registers. The first clock, $\overline{RAS}$, strobes in the six low order addresses (A_0-A_5) which selects one of 64 rows and begins the timing which enables the column sense amplifiers. The second clock, $\overline{CAS}$, strobes in the six high order addresses (A_6-A_{11}) to select one of 64 column sense amplifiers and Chip Select ($\overline{CS}$) which enables the data out buffer.

An address map of the 2104A is shown below. Address "0" corresponds to all addresses at V_{IL}. All addresses are sequentially located on the chip.

2104A Address Map

```
4032                0
              ┌───┐
              │ R │
     ARRAY    │ O │
   (DATA IN)  │ W │
              │   │
              │ D │
              │ E │
              │ C │
4095            63 │ O │
              │ D │
              │ E │
              │ R │
  SENSE AMPLIFIER

  COLUMN DECODER
```
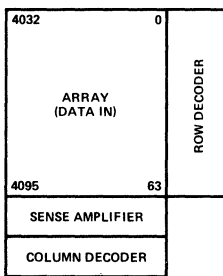
DATA CYCLES/TIMING

A memory cycle begins with addresses stable and a negative transition of $\overline{RAS}$. See the waveforms on page 4. It is not necessary to know whether a Read or Write cycle is to be performed until $\overline{CAS}$ becomes valid.

Note that Chip Select ($\overline{CS}$) does not have to be valid until the second clock, $\overline{CAS}$. It is, therefore, possible to start a memory cycle before it is known which device must be selected. This can result in a significant improvement in

system access time since the decode time for chip select does not enter into the calculation for access time.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks are TTL compatible and do not require level shifting and driving at high voltage MOS levels. Buffers internal to the 2104A convert the TTL level signals to MOS levels inside the device. Therefore, the delay associated with external TTL-MOS level converters is not added to the 2104A system access time.

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during $\overline{CAS}$. The output pin of a selected device will unconditionally go to a high impedance state immediately following the leading edge of $\overline{CAS}$ and remain in this state until valid data appears at the output at access time. The selected output data is internally latched and will remain valid until a subsequent $\overline{CAS}$ is given to the device by a Read, Write, Read-Modify-Write, $\overline{CAS}$ only or Refresh cycle. Data-out goes to a high impedance state for all non-selected devices.

Device access time, t_{ACC}, is the longer of two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR   2. $t_{ACC} = t_{RCL} + t_T + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe lead time, t_{RCL}, and transition time, t_T, are system dependent timing parameters. For example, substituting the device parameters of the 2104A-4 and assuming a TTL level transition time of 5 ns yields:

3. $t_{ACC} = t_{RAC} = 300ns$ for $80\,nsec \leqslant t_{RCL} \leqslant 130nsec$

OR

4. $t_{ACC} = t_{RCL} + t_T + t_{CAC} = t_{RCL} + 170ns$ for $t_{RCL} > 130ns$.

Note that if 80 nsec$\leqslant$$t_{RCL}$$\leqslant$130 nsec, device access time is determined by equation 3 and is equal to t_{RAC}. If t_{RCL}>130 nsec, access time is determined by equation 4. This 50ns interval (shown in the t_{RCL} inequality in equation 3) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$. This allowance for a t_{RCL} skew is designed in at the device level to allow minimum access times to be achieved in practical system designs.

WRITE CYCLE

A Write Cycle is generally performed by bringing Write Enable ($\overline{WE}$) low before $\overline{CAS}$. D_{OUT} will be the data written into the cell addressed. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} will be indeterminate.

READ-MODIFY-WRITE CYCLE

A Read-Modify-Write Cycle is performed by bringing Write Enable ($\overline{WE}$) low after access time, t_{RAC}, with $\overline{RAS}$ and $\overline{CAS}$ low. Data in must be valid at or before the falling edge of $\overline{WE}$. In a read-modify-write cycle D_{OUT} is data read and does not change during the modify-write portion of the cycle.

$\overline{CAS}$ ONLY (DESELECT) CYCLE

In some applications, it is desirable to be able to deselect all memory devices without running a regular memory cycle. This may be accomplished with the 2104A by performing a $\overline{CAS}$-Only Cycle. Receipt of a $\overline{CAS}$ without $\overline{RAS}$ deselects the 2104A and forces the Data Output to the high-impedance state. This places the 2104A in its lowest power, standby condition. I_{DD} will be about twice I_{DD1} for the first cycle of $\overline{CAS}$-only deselection and I_{DD1} for any additional $\overline{CAS}$-only cycles. The cycle timing and $\overline{CAS}$ timing should be just as if a normal $\overline{RAS}/\overline{CAS}$ cycle was being performed.

CHIP SELECTION/DESELECTION

The 2104A is selected by driving $\overline{CS}$ low during a Read,

Write, or Read-Modify-Write cycle. A device is deselected by 1) driving $\overline{CS}$ high during a Read, Write, or Read-Modify-Write cycle or 2) performing a $\overline{CAS}$ Only cycle independent of the state of $\overline{CS}$.

REFRESH CYCLES

Each of the 64 rows internal to the 2104A must be refreshed every 2 msec to maintain data. Any data cycle (Read, Write, Read-Modify-Write) refreshes the entire selected row (defined by the low order row addresses). The refresh operation is independent of the state of chip select. It is evident, of course, that if a Write or Read-Modify-Write cycle is used to refresh a row, the device should be deselected ($\overline{CS}$ high) if it is desired not to change the state of the selected cell.

RAS/$\overline{CAS}$ TIMING

The device clocks, $\overline{RAS}$ and $\overline{CAS}$, control operation of the 2104A. The timing of each clock and the timing relationships of the two clocks must be understood by the user in order to obtain maximum performance in a memory system.

The $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle must not begin until the minimum precharge time, t_{RP}, has been met.

PAGE MODE OPERATION

The 2104A is designed for page mode operation and is presently being characterized for that mode. Specifications will be available at a later date.

POWER SUPPLY

Typical power supply current waveforms versus time are shown below for both a $\overline{RAS}/\overline{CAS}$ cycle and a $\overline{CAS}$ only cycle. I_{DD} and I_{BB} current surges at $\overline{RAS}$ and $\overline{CAS}$ edges make adequate decoupling of these supplies important. Due to the high frequency noise component content of the current waveforms, the decoupling capacitors should be low inductance, ceramic units selected for their high frequency performance.

It is recommended that a 0.1 μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1 μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10 μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

A 0.01 μF ceramic capacitor is recommended between V_{CC} and V_{SS} at every eighth device to prevent noise coupling to the V_{CC} line which may affect the TTL peripheral logic in the system.
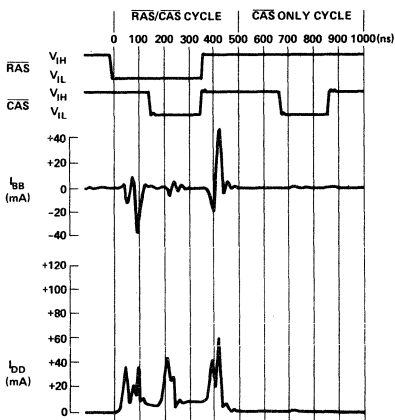
TYPICAL SUPPLY CURRENTS VS. TIME

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double-sided circuit boards with noise performance equal to or better than multi-layered circuit boards.
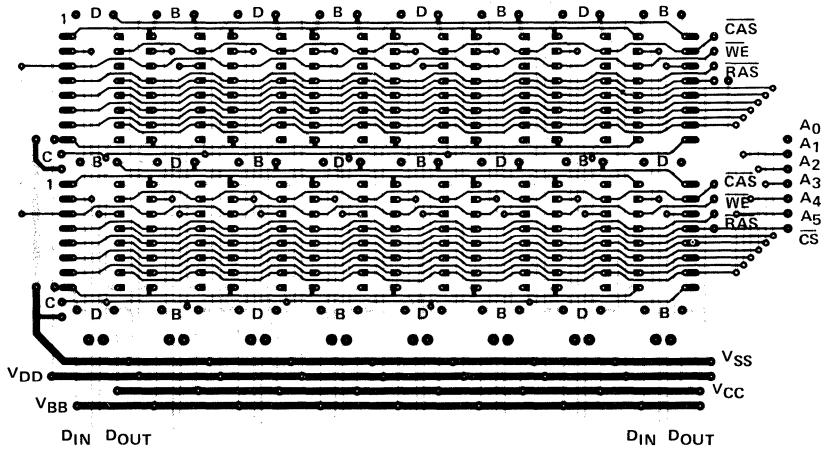
DECOUPLING CAPACITORS
D = 0.1 μF to V_{DD} TO V_{SS}
B = 0.1 μF V_{BB} TO V_{SS}
C = 0.01 μF V_{CC} TO V_{SS}

intel®

2107B

4096 BIT DYNAMIC RAM

	2107B	2107B-4	2107B-5
Access Time	200ns	270ns	300ns
Read,Write Cycle	400ns	470ns	590ns
RMW Cycle	520ns	590ns	750ns

- Low Cost Per Bit
- Low Standby Power
- Easy System Interface
- Only One High Voltage Input Signal — Chip Enable
- TTL Compatible — All Address, Data, Write Enable, Chip Select Inputs
- Refresh Period—2ms for 2107B, 2107B-4, 1ms for 2107B-5 @70°C

- Address Registers Incorporated on the Chip
- Simple Memory Expansion — Chip Select Input Lead
- Fully Decoded — On Chip Address Decode
- Output is Three State and TTL Compatible
- Industry Standard 22-Pin Configuration

The Intel®2107B is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 2107B uses dynamic circuitry which reduces the standby power dissipation.

Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107B is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 2107B uses a single transistor cell to achieve high speed and low cost. It is a replacement for the 2107A.

PIN CONFIGURATION
2107B

V_{BB} 1	22 V_{SS}
A_9 2	21 A_8
A_{10} 3	20 A_7
A_{11} 4	19 A_6
$\overline{CS}$ 5	18 V_{DD}
D_{IN} 6	17 CE
$\overline{D_{OUT}}$ 7	16 NC
A_0 8	15 A_5
A_1 9	14 A_4
A_2 10	13 A_3
V_{CC} 11	12 $\overline{WE}$
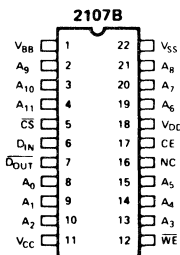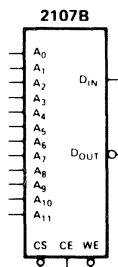
PIN NAMES

$A_0 \cdot A_{11}$	ADDRESS INPUTS*	V_{BB}	POWER (-5V)
CE	CHIP ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	V_{DD}	POWER (+12V)
D_{IN}	DATA INPUT	V_{SS}	GROUND
$\overline{D_{OUT}}$	DATA OUTPUT	$\overline{WE}$	WRITE ENABLE
NC	NOT CONNECTED		

*Refresh Address $A_0 \cdot A_5$.
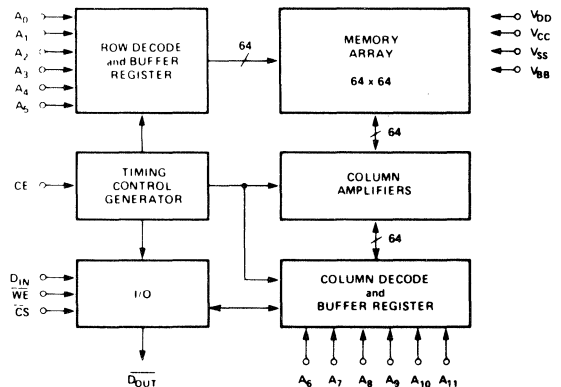
LOGIC SYMBOL
2107B

BLOCK DIAGRAM

Absolute Maximum Ratings*

Temperature Under Bias . . . . 0°C to 70°C

Storage Temperature . . . . −65°C to +150°C

All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} . . . . +25V to −0.3V

Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} . . . . +20V to −0.3V

Power Dissipation 1.25W

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±10%, V_{BB}[1] = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}[6]	Input Load Current (all inputs except CE)		.01	50	µA	V_{IN} = $V_{IL\,MIN}$ to $V_{IH\,MAX}$ CE = V_{ILC} or V_{IHC}
I_{LC}	Input Load Current		.01	2	µA	V_{IN} = $V_{IL\,MIN}$ to $V_{IH\,MAX}$
$|I_{LO}|$	Output Leakage Current for high impedance state		.01	10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		110	200[5]	µA	CE = −1V to +.6V
I_{DD2}	V_{DD} Supply Current during CE on			60	mA	CE = V_{IHC}, $\overline{CS}$ = V_{IL}
$I_{DD\,AV}$	Average V_{DD} Current		38	54	mA	$\overline{CS}$ = V_{IL}; T_A = 25°C; Min cycle time, Min t_{CE}
I_{CC1}[4]	V_{CC} Supply Current during CE off		.01	10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
I_{BB}	V_{BB} Supply Current		5	400	µA	
V_{IL}	Input Low Voltage	−1.0		0.6	V	t_T = 20ns, V_{ILC} = +1.0V
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	t_T = 20ns
V_{ILC}	CE Input Low Voltage	−1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}−1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = −2.0mA

NOTES:
1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V or more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.
5. Maximum I_{DD1} for 2107B-5 is 250 µA.
6. During CE high a current of 0.5mA typical, 1.5mA maximum will be drawn from any address pin which is switched from low to high.

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	2107B		2107B-4		2107B-5		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Time Between Refresh		2		2		1	ms	7
t_{AC}	Address to CE Set Up Time	0		0		10		ns	3
t_{AH}	Address Hold Time	100		100		100		ns	
t_{CC}	CE Off Time	130		130		200		ns	
t_T	CE Transition Time	10	40	10	40	10	40	ns	
t_{CF}	CE Off to Output High Impedance State	0		0		0		ns	

READ CYCLE

Symbol	Parameter	2107B		2107B-4		2107B-5		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	400		470		590		ns	4
t_{CE}	CE On Time	230	4000	300	4000	350	3000	ns	
t_{CO}	CE Output Delay		180		250		280	ns	5
t_{ACC}	Address to Output Access		200		270		300	ns	6
t_{WL}	CE to $\overline{WE}$	0		0		0		ns	
t_{WC}	$\overline{WE}$ to CE On	0		0		0		ns	

WRITE CYCLE

Symbol	Parameter	2107B		2107B-4		2107B-5		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	400		470		590		ns	4
t_{CE}	CE On Time	230	4000	300	4000	350	3000	ns	
t_W	$\overline{WE}$ to CE Off	125		150		200		ns	
t_{CW}	CE to $\overline{WE}$	150		150		150		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		0		0		ns	1
t_{DH}	D_{IN} Hold Time	0		0		0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		50		75		ns	
t_{WW}	$\overline{WE}$ Delay	75		75		75		ns	

Capacitance[2] $T_A = 25°C$

Symbol	Test	Plastic And Ceramic Pkg. Typ.	Max.	Unit	Conditions
C_{AD}	Address Capacitance, $\overline{CS}$	4	6	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	17	25	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	5	7	pF	$V_{OUT} = 0V$
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	8	10	pF	$V_{IN} = V_{SS}$

Notes: 1. If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.
2. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation.
$C = \frac{I\Delta t}{\Delta V}$ with the current equal to a constant 20mA.

3. t_{AC} is measured from end of address transition.
4. $t_T = 20ns$
5. $C_{LOAD} = 50pF$, Load = One TTL Gate, Ref = 2.0V.
6. $t_{ACC} = t_{AC} + t_{CO} + 1t_T$
7. $t_{REF} = 2ms$ at $T_A = 55°C$ for the 2107B-5.

Read and Refresh Cycle [1]

Write Cycle

NOTES: 1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} −2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Read Modify Write Cycle[1]

Symbol	Parameter	2107B		2107B-4		2107B-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RWC}	Read Modify Write (RMW) Cycle Time	520		590		750		ns
t_{CRW}	CE Width During RMW	350	4000	420	4000	510	3000	ns
t_{WC}	$\overline{WE}$ to CE on	0		0		0		ns
t_W	$\overline{WE}$ to CE off	150		150		200		ns
t_{WP}	$\overline{WE}$ Pulse Width	50		50		100		ns
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		0		0		ns
t_{DH}	D_{IN} Hold Time	0		0		0		ns
t_{CO}	CE to Output Delay		180		250		280	ns
t_{ACC}	Access Time $(t_{ACC} = t_{AC} + t_{CO} + 1t_T)$		200		270		300	ns
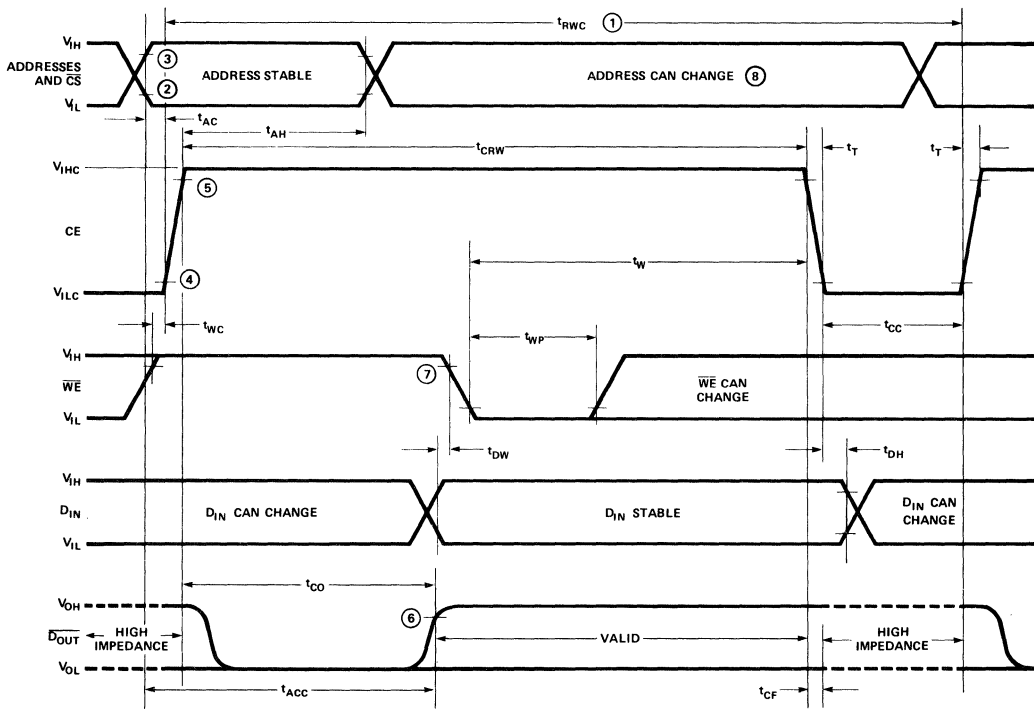
NOTES:
1. Minimum cycle timing is based on t_T of 20ns.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} −2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$. C_{LOAD} = 50pF. Load = One TTL Gate.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.
8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Typical Characteristics

Fig. 1. I_{DD} AV VS. TEMPERATURE
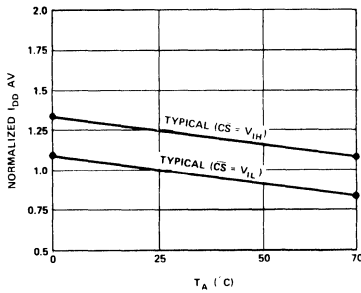
Fig. 2. TYPICAL I_{DD} AVERAGE VS. CYCLE TIME
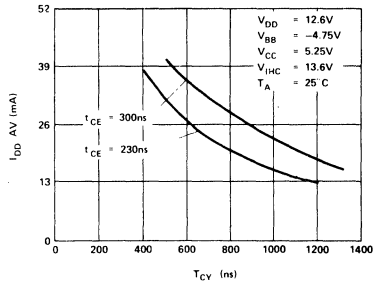
Fig. 3. I_{DD2} VS. TEMPERATURE
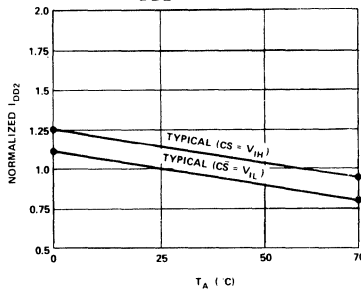
Fig. 4. TYPICAL V_{IL} MAX VS. CE RISE TIME
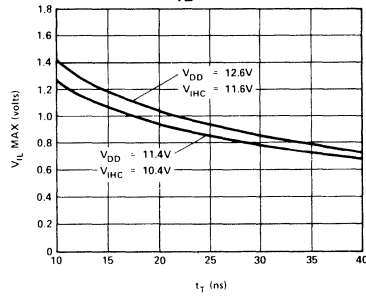
Typical Current Transients vs. Time
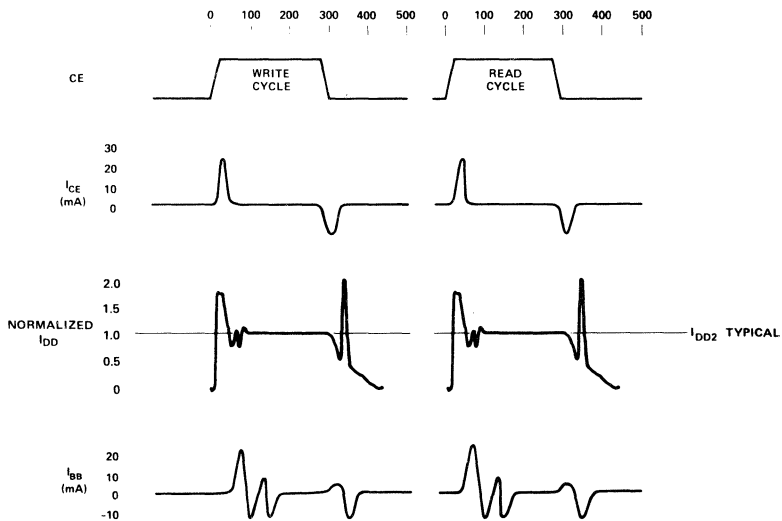
For additional typical characteristics and applications information please refer to Intel Application Note AP-10, "Memory System Design With the Intel 2107B 4K RAM" or Intel's Memory Design Handbook.

intel®

2116 FAMILY

16,384 X 1 BIT DYNAMIC RAM

	2116-2	2116-3	2116-4
Max. Access Time (ns)	200	250	300
Read, Write Cycle (ns)	350	375	425
Read-Modify-Write Cycle (ns)	400	525	595

- **Highest Density 16K RAM: Industry Standard 16 Pin Package**
- **Low Standby Power**
- **All Inputs Including Clocks TTL Compatible**
- **±10% Tolerance on all Power Supplies +12V, +5V, −5V**

- **On-Chip Latches for Address and Data In**
- **Only 64 Refresh Cycles Required Every 2 ms**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**

The Intel® 2116 is a 16,384 word by 1 bit MOS RAM fabricated with two layer polysilicon N-MOS technology — a production-proven process for high performance, high reliability, and high functional density. The 2116 uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 2116 allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment. The 2116 is designed to facilitate upgrading of 2104A-type 4K RAM systems to 16K capabilities.

The use of the 16 pin package is made possible by multiplexing the 14 address bits (required to address 1 of 16,384 bits) into the 2116 on 7 address input pins. The two 7 bit address words are latched into the 2116 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires re-freshing for data retention. Refreshing can be accomplished every 2 ms by any one of the three following methods: (1) $\overline{CAS}$ before $\overline{RAS}$ cycles on 64 addresses, A_0–A_5, (2) $\overline{RAS}$-only cycles on 128 address, A_0–A_6, or (3) normal read or write cycles on 128 addresses, A_0–A_6. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed. The output is brought to a high impedance state by a $\overline{CAS}$-only cycle or by a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

PIN CONFIGURATION

V_{BB}	1	16	V_{SS}
D_{IN}	2	15	$\overline{CAS}$
$\overline{WE}$	3	14	D_{OUT}
$\overline{RAS}$	4	13	A_6
A_0	5	12	A_3
A_2	6	11	A_4
A_1	7	10	A_5
V_{DD}	8	9	V_{CC}

2116

LOGIC SYMBOL

A_0
A_1
A_2
A_3 D_{IN}
A_4
A_5
A_6 D_{OUT}
RAS
CAS
WE
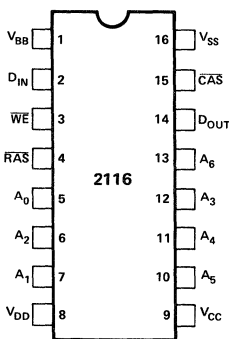
BLOCK DIAGRAM

PIN NAMES

$A_0 \cdot A_6$	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND
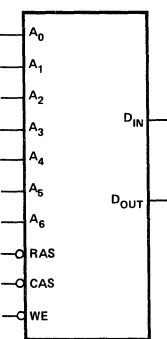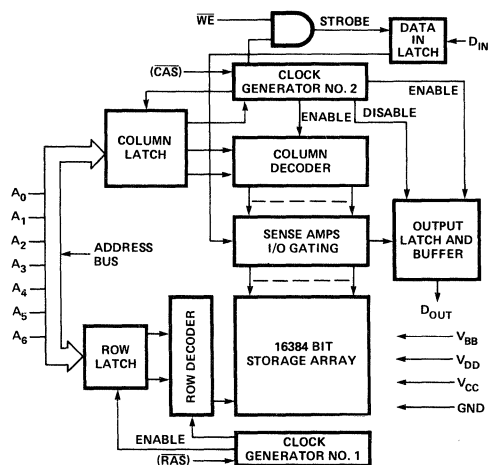
Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . –10°C to +80°C
Storage Temperature . . . . –65°C to +150°C
Voltage on any Pin Relative to V_{BB}
  ($V_{SS} - V_{BB} \geqslant$ 4V) . . . . –0.3V to +20V
Power Dissipation 1.25W

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics [1],[2]

T_A = 0°C to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = –5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions	
		Min.	Typ.(3)	Max.			
I_{LI}	Input Load Current (any input)			10	μA	$V_{IN} = V_{IL\,MIN}$ to $V_{IH\,MAX}$	
$|I_{LO}|$	Output Leakage Current for high impedance state		0.1	10	μA	Chip deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current		1.2	2	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH} or $\overline{CAS}$-only cycle. Chip deselected prior to measurement. See Note 5.	
I_{BB1}	V_{BB} Supply Current		1	50	μA		
I_{DD2} [4]	Operating V_{DD} Current		53	69	mA	2116-2 t_{CYC} = 350 ns	T_A = 25°C Device selected. See Note 6.
			51	68	mA	2116-3 t_{CYC} = 375 ns	
			49	65	mA	2116-4 t_{CYC} = 425 ns	
I_{BB2}	Operating V_{BB} Current		120	400	μA	Device selected	
I_{CC1} [7]	V_{CC} Supply Current when deselected			10	μA		
V_{IL}	Input Low Voltage (any input)	–1.0		0.8	V		
V_{IH}	Input High Voltage (any input)	2.4		V_{CC}+1	V		
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 4.1 mA (Read Cycle Only)	
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = –5 mA (Read Cycle Only)	

Capacitance [8] T_A = 25°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = –5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{I1}	Address, Data In & $\overline{WE}$ Capacitance	4	7	pF	$V_{IN} = V_{SS}$
C_{I2}	$\overline{RAS}$ Capacitance	3	5	pF	$V_{IN} = V_{SS}$
C_{I3}	$\overline{CAS}$ Capacitance	6	10	pF	$V_{IN} = V_{SS}$
C_O	Data Output Capacitance	3	7	pF	V_{OUT} = 0V

Notes:
1. All voltages referenced to V_{SS}. No power supply sequencing is required but V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}.
2. To avoid self-clocking, $\overline{RAS}$ should not be allowed to float.
3. Typical values are for T_A = 25°C and nominal power supply voltages.
4. For $\overline{RAS}$-only refresh I_{DD} = 0.78 I_{DD2}. For $\overline{CAS}$-before-$\overline{RAS}$ (64 cycle refresh) I_{DD} = 0.96 I_{DD2}.
5. The chip is deselected (i.e., output is brought to high impedance state) by $\overline{CAS}$-only cycle or by $\overline{CAS}$-before-$\overline{RAS}$ cycle. The current flowing in a selected (i.e., output on) chip with $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} is approximately twice I_{DD1}.
6. See Page 2-98 for typical I_{DD} characteristics under other conditions.
7. When chip is selected V_{CC} supply current is dependent on output loading; V_{CC} is connected to output buffer only.
8. Capacitance measured with Boonton Meter.

Typical Characteristics

I_{BB2} AND I_{DD2} VS. TEMPERATURE

Figure 1.

I_{DD2} VS. CYCLE TIME
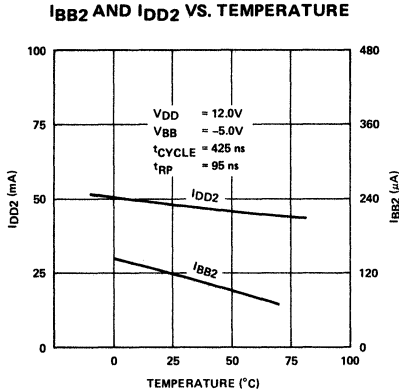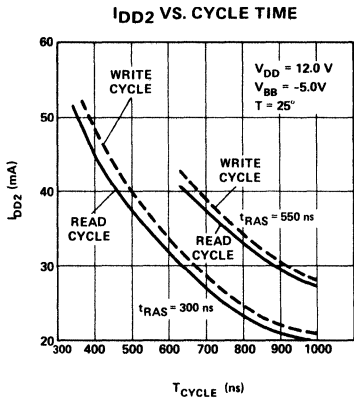
Figure 2.

Standby Power Calculations:

$$P_{REF} = P_{OP} \left(N\frac{t_{CYC}}{t_{REF}}\right) + P_{SB}\left(1 - N\frac{t_{CYC}}{t_{REF}}\right) \text{ where}$$

P_{OP} = Power dissipation (continuous operation) $\cong V_{DD} \times I_{DD2}$.

N = Number of refresh cycles (64 or 128)

t_{CYC} = Cycle time for a refresh cycle.

t_{REF} = Time between refreshes

P_{SB} = Standby power dissipation = $V_{DD} \times I_{DD1} + |V_{BB}| \times I_{BB}$

Note that I_{DD2} depends upon refresh as follows:

1. For 128 cycle ($\overline{RAS}$ before $\overline{CAS}$) use I_{DD2} from Figures 1 and 2.

2. For 64 cycle ($\overline{CAS}$ before $\overline{RAS}$) multiply I_{DD2} determined in (1) by 0.96.

3. For 128 cycle ($\overline{RAS}$ only) multiply I_{DD2} determined in (1) by 0.78.

Examples of typical calculations for V_{BB} = –5.0V, V_{DD} = 12.0V, T_A = 25°C, t_{CYC} = 0.425 μs, t_{RAS} = 0.3 μs. t_{REF} = 2000 μs:

1. 128 cycle ($\overline{RAS}$ before $\overline{CAS}$): P_{OP} = 12.0V x 43 mA = 516 mW

$$P_{REF} = 516 \left(128 \frac{0.425}{2000}\right) + (12 \times 1.2 + 5 \times 0.001)\left(1 - 128 \frac{0.425}{2000}\right)$$

$$P_{REF} = 28.0 \text{ mW}$$

2. 64 cycle ($\overline{CAS}$ before $\overline{RAS}$); P_{OP} = 12.0V x 43 (0.96) mA = 495 mW.

$$P_{REF} = 495 \left(64 \frac{0.425}{2000}\right) + (12 \times 1.2 + 5 \times 0.001)\left(1 - 64 \frac{0.425}{2000}\right) =$$

$$P_{REF} = 20.9 \text{ mW}$$

3. 128 cycle ($\overline{RAS}$ only): P_{OP} = 12.0V x 43 (0.78) mA = 402 mW

$$P_{REF} = 25.0 \text{ mW}$$
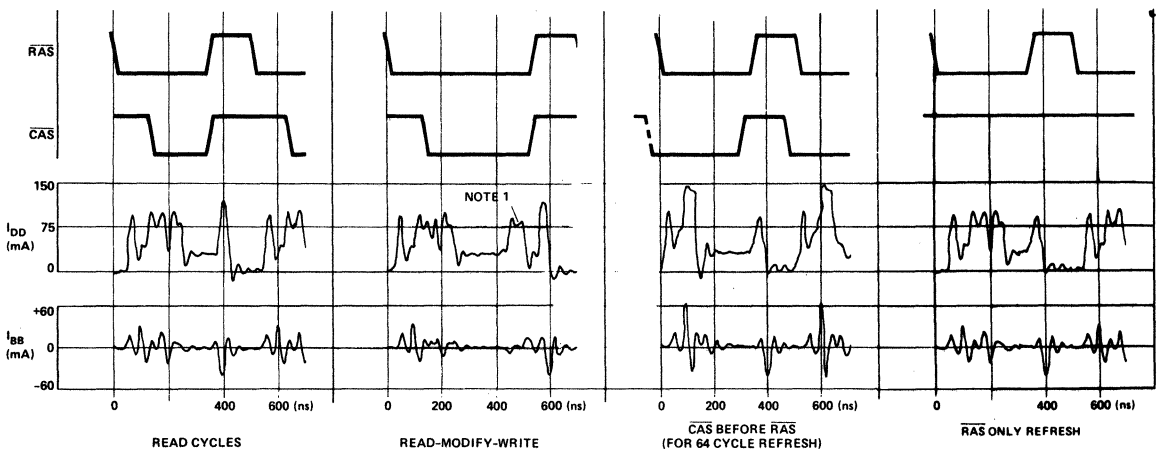
Note 1: Increase in current due to $\overline{WE}$ going low. Width of this current pulse is independent of $\overline{WE}$ pulse width.

Figure 3. Supply Current Waveforms.

A.C. Characteristics [1]

T_A=0°C to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=−5V ±10%, V_{SS}=0V, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2116-2		2116-3		2116-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{REF}	Time Between Refresh		2		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	75		75		95		ns
t_{CP}	$\overline{CAS}$ Precharge Time	100		125		125		ns
t_{RCL} [2]	$\overline{RAS}$ to $\overline{CAS}$ Leading Edge Lead Time	45	75	50	110	60	110	ns
t_{CRP} [3]	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	160		200		220		ns
t_{CSH}	$\overline{CAS}$ Hold Time	200		250		300		ns
t_{ASR}	Row Address Set-Up Time	0		0		0		ns
t_{ASC}	Column Address Set-Up Time	−10		−10		−10		ns
t_{AH}	Address Hold Time	45		50		60		ns
t_T	Transition Time (Rise and Fall)		50		50		50	ns
t_{OFF}	Output Buffer Turn Off Delay	0	60	0	60	0	80	ns
t_{CAC} [4]	Access Time From $\overline{CAS}$		125		150		190	ns
t_{RAC} [4]	Access Time From $\overline{RAS}$		200		250		300	ns

READ AND REFRESH CYCLES

Symbol	Parameter	2116-2		2116-3		2116-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC} [5]	Random Read Cycle Time	350		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	275	32000	300	32000	330	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	125	10000	150	10000	190	10000	ns
t_{CH}	$\overline{CAS}$ Hold Time for $\overline{RAS}$-Only Refresh	30		30		30		ns
t_{CPR}	$\overline{CAS}$ Precharge for 64 Cycle Refresh	30		30		30		ns
t_{RCH}	Read Command Hold Time	20		20		20		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		ns
t_{DOH}	Data-Out Hold Time	32		32		32		µs

WRITE CYCLE

Symbol	Parameter	2116-2		2116-3		2116-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC} [5]	Random Write Cycle Time	350		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	275	32000	300	32000	330	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	125	10000	150	10000	190	10000	ns
t_{WCH}	Write Command Hold Time	75		100		100		ns
t_{WP}	Write Command Pulse Width	50		100		100		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	125		200		200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		150		160		ns
t_{DS} [6]	Data-In Set-Up Time	0		0		0		ns
t_{DH} [6]	Data-In Hold Time	100		100		125		ns

Notes:
1. All voltages referenced to V_{SS}.
2. $\overline{CAS}$ must remain at V_{IH} a minimum of $t_{RCL\ MIN}$ after $\overline{RAS}$ switches to V_{IL}. To achieve the minimum guaranteed access time (t_{RAC}), $\overline{CAS}$ must switch to V_{IL} at or before t_{RCL} (MAX) = t_{RAC} −t_{CAC}. Device operation is not guaranteed for t_{RCL}>2 µs.
3. The t_{CRP} specification is less restrictive than the t_{CRL} range which was specified in the 2116 preliminary data sheet.
4. Load = 1 TTL and 50 pF.
5. The minimum cycle timing does not allow for t_T or skews.
6. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

Waveforms

READ CYCLE

WRITE CYCLE

Notes:
1,2. V_{IH} MIN and V_{IL} MAX are reference levels for measuring timing of input signals.
3,4. V_{OH} MIN and V_{OL} MAX are reference levels for measuring timing of D_{OUT}.
5. D_{OUT} follows D_{IN} when writing, with $\overline{WE}$ before $\overline{CAS}$.
6. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{OFF} is measured to $I_{OUT} \leqslant |I_{LO}|$.

A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2116-2		2116-3		2116-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RMW}	Read-Modify-Write Cycle Time	400		525		595		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	225	10000	310	10000	350	10000	ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	325	32000	450	32000	500	32000	ns
t_{RWH}	RMW Cycle $\overline{RAS}$ Hold Time	250		350		390		ns
t_{CWH}	RMW Cycle $\overline{CAS}$ Hold Time	300		410		460		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	125		200		200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		160		160		ns
t_{WP}	Write Command Pulse Width	50		100		100		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		ns
t_{MOD}	Modify Time	0	10	0	10	0	10	μs
t_{DS}	Data-In Set-Up Time	0		0		0		ns
t_{DHM}	Data-In Hold Time (RMW Cycle)	50		100		125		ns

Waveforms
READ MODIFY WRITE CYCLE
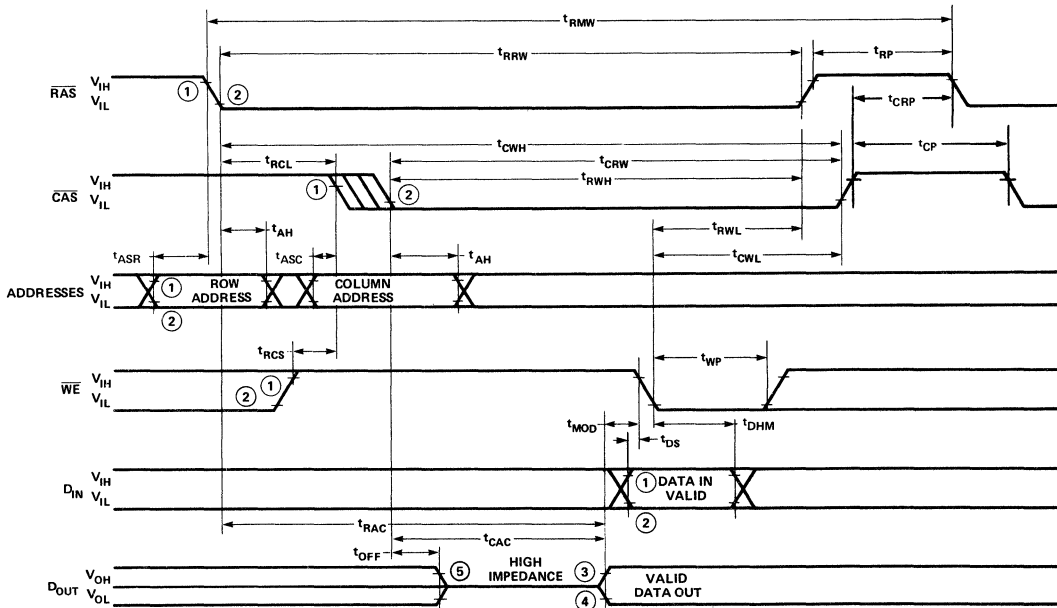
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

Refresh Cycle Waveforms

$\overline{CAS}$ BEFORE $\overline{RAS}$ CYCLES. (64 CYCLE REFRESH)
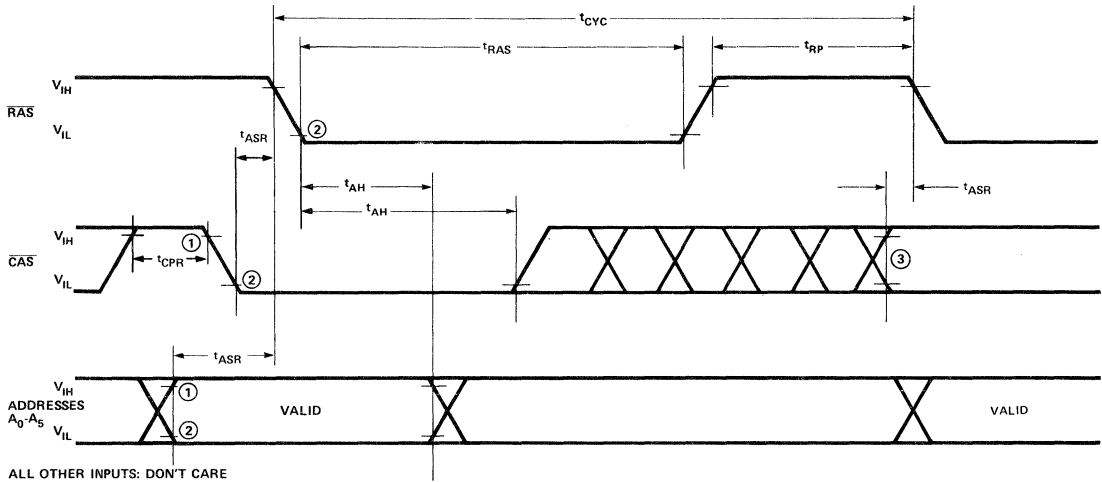
$\overline{RAS}$ ONLY CYCLES (128 CYCLE REFRESH)
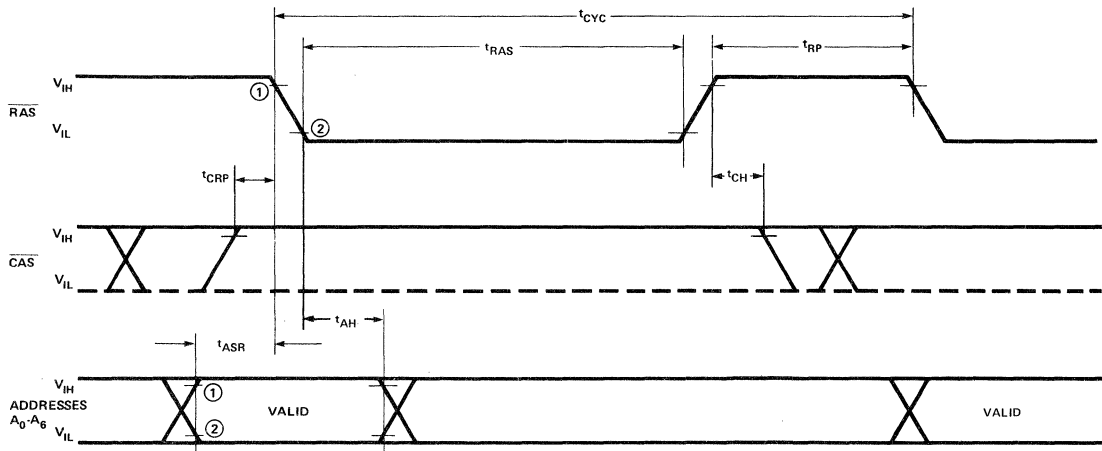
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
 3. $\overline{CAS}$ must be high or low as appropriate for the next cycle.

Applications Information

REFRESH MODES

The 2116 may be refreshed in any of three modes. Read/Refresh cycles and $\overline{RAS}$-only cycles refresh the row addressed by A_0 through A_6 and therefore require 128 cycles to refresh the stored data. Assuming a 500 nsec system cycle time, the refresh operations require 64 μsec out of each 2.0 msec refresh period or 3.2% of the available memory time. The third 2116 refresh mode, $\overline{CAS}$-before-$\overline{RAS}$, allows refresh of the stored data in only 64 cycles and requires only 32 μsec or 1.6% of the available memory time

(equal to the 64-cycle refresh 4K RAMs). While some 2116 aplications would not be impacted by the 3.2% memory lockout time using 128 cycle refresh, most large mainframe memory applications would suffer throughput degradation in that refresh mode. Intel designed the 2116 to allow either 128-cycle or 64-cycle refresh, allowing the system designer to choose the refresh mode which fits his system needs. In addition to allowing higher memory throughput, the $\overline{CAS}$-before-RAS 64-cycle refresh mode dissipates approximately 14% less power than the 128-cycle $\overline{RAS}$-only mode and 23% less power than the 128-cycle Read/Refresh mode (refer to the Standby Power Calculation section).

POWER SUPPLY DECOUPLING/DISTRIBUTION

Power supply current waveforms for the 2116 are shown in Figure 3. The V_{DD} supply provides virtually all of the operating current for the 2116. The V_{DD} supply current, I_{DD}, has two components: transient current peaks when the clocks change state and a DC component while the clocks are active (low). When selecting the decoupling capacitors for the V_{DD} supply, the characteristics of capacitors as well as the current waveform must be considered. Suppression of transient or pulse currents require capacitors with small physical size and low inherent inductance. Monolithic and other ceramic capacitors exhibit these desirable characteristics. When the current waveform indicates a DC component, bulk capacity must be located near the current load to supply the load power. Inductive effects of PC board traces and bus bars preclude supplying the DC component from bulk capacitors at the periphery of a memory matrix without voltage droop during the active portion of a memory cycle. This means that some bulk capacity in the form of electrolytic or large ceramic capacitors should be distributed around or within the memory matrix.

The V_{BB} supply current, I_{BB}, has high transient current peaks, with essentially no DC component (less than 400 microamperes). The V_{BB} capacitors should be selected for transient suppression characteristics. The following capacitance values and locations are recommended for the 2116:

1. A 0.33 μF ceramic capacitor between V_{DD} and V_{SS} (ground) at every other device.

2. A 0.1 μF ceramic capacitor between V_{BB} and V_{SS} at every other device (preferably alternate devices to the V_{DD} decoupling above).

3. A 4.7 μF electrolytic capacitor between V_{DD} and V_{SS} for each eight devices and located adjacent to the devices.

The V_{CC} supply is connected only to the 2116 output buffer and is not used internally. The load current from the V_{CC} supply is dependent only upon the output loading and is usually only the input high level current to a TTL gate and the output leakage currents of any OR-tied 2116s (typically 100 μA or less total). Intel recommends that a 0.1 or 0.01 μF ceramic capacitor be connected between V_{CC} and V_{SS} for every eight devices to preclude coupled noise from affecting the TTL devices in the system.

Intel recommends a power supply distribution system such that each power supply is grided both horizontally and vertically at each memory device. This technique minimizes the power distribution system impedance and enhances the effect of the decoupling capacitors.

OUTPUT DATA LATCH

The 2116 contains an output data latch eliminating the need for an external system data latch and the timing circuitry required to strobe an external latch. The 2116 output latch operates identically to the output latch found on all industry standard 16-pin, 4K RAMs and enhances the system compatibility of the 16K and 4K devices.

Operation of the output latch is controlled by $\overline{CAS}$. The data output will go to the high-impedance state immediately following the $\overline{CAS}$ leading edge during each data cycle and will either go to valid data at access time on selected devices (devices receiving both $\overline{RAS}$ and $\overline{CAS}$) or will remain in the high impedance state on unselected devices (devices receiving only $\overline{CAS}$). During $\overline{RAS}$-only refresh cycles, the data output remains in the state it was prior to the $\overline{RAS}$-only cycle. This unique feature of latched output RAMs allows a refresh cycle to be hidden among data cycles without impacting data availability. For instance, a $\overline{RAS}$-only refresh cycle could follow each data cycle in a microprocessor system but the accessed data would remain at the device output and the microprocessor could take the data at any time within the cycle. Non-latched output devices do not provide this type of hidden refresh capability since their data output would go to the high impedance state at the end of the data cycle.

PAGE MODE OPERATION

The 2116 is designed for page mode operation and is presently being characterized for that mode. Specifications will be available at a later date.

intel®

3222

REFRESH CONTROLLER FOR 4K DYNAMIC RANDOM ACCESS MEMORIES

- **Ideal for use in 2107A, 2107B Systems**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 22-Pin DIP**

- **Adjustable Refresh Timing Oscillator**
- **6-Bit Address Multiplexer**
- **6-Bit Refresh Address Counter**
- **Refresh Cycle Controller**

The Intel® 3222 is a refresh controller for dynamic RAMs requiring refresh of up to 6 input addresses (or 4K bits for 64 x 64 organization). The device contains an accurate refresh timer (whose frequency can be set by an external resistor and capacitor), plus all necessary control and I/O circuitry to provide for the refresh requirements of dynamic RAMs. The chip's high performance makes it especially suitable for use with high speed N-channel RAMs like the Intel® 2107B. The 3222 is well suited for asynchronous dynamic memory systems.

The 3222 operates from a single +5 volt power supply and is specified for operation over a 0°C to 75°C ambient temperature range. It is fabricated by means of Intel's highly reliable Schottky bipolar process.

PIN CONFIGURATION
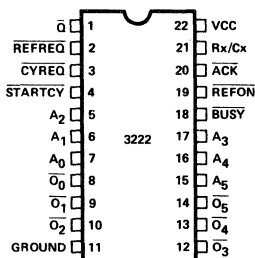
PIN NAMES

$A_0 - A_5$	ADDRESS INPUTS	$\bar{O}_0 \cdot \bar{O}_5$	ADDRESS OUTPUTS
$\overline{ACK}$	ACKNOWLEDGE OUTPUT	$\bar{Q}$	INTERNAL REFRESH REQUEST LATCH OUTPUT
$\overline{BUSY}$	BUSY INPUT	$\overline{REFON}$	REFRESH ON OUTPUT
$\overline{CYREQ}$	CYCLE REQUEST INPUT	$\overline{REFREQ}$	REFRESH REQUEST INPUT
		$RxCx$	RC TIE POINT
		$\overline{STARTCY}$	START CYCLE OUTPUT
		V_{CC}	+5V SUPPLY

BLOCK DIAGRAM

Absolute Maximum Ratings*

Temperature Under Bias . . . . −65° to +125°C
Storage Temperature . . . . −65° to +160°C
All Input, Output or Supply Voltages . . . . − 0.5V to +7V
All Input Voltages . . . . −1.0V to +5.5V
Output Currents . . . . 100 mA
Power Dissipation . . . . 1 W

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C.

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
		Min.	Typ.[1]	Max.		
I_{FB}	Input Load Current $\overline{BUSY}$		0.40	1	mA	V_{IN} = 0.45V
I_{FO}	Input Load Current All Other Inputs		0.05	0.25	mA	V_{IN} = 0.45V
I_{RB}	Input Leakage Current $\overline{BUSY}$		<1	50	μA	V_{IN} = V_{CC}
I_{RO}	Input Leakage Current All Other Inputs		<1	20	μA	V_{IN} = 5.25V
V_{CLAMP}	Input Clamp Voltage		−0.76	−1	V	I_C = −5.0mA
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{CC}	Power Supply Current		91	120	mA	V_{CC} = 5.25V
I_{SC}	Output High Short Circuit Current		−48	−70	mA	V_{OUT} = 0V V_{CC} = 5.25V
V_{OL}	Output Low Voltage		0.32	0.45	V	I_{OL} = 5mA
V_{OH}	Output High Voltage ($\overline{O}_0$-$\overline{O}_5$)	2.6	3.1		V	I_{OH} = −1mA V_{CC} = 4.75V
V_{OH1}	Output High Voltage (All Other Outputs)	2.4	3.0		V	I_{OH} = −1mA V_{CC} = 4.75V

Note 1: Typical values are for T_A = 25°C and nominal power supply voltages.

Capacitance[2] , T_A = 25°C

| Symbol | Test | Limits (pF) | | Conditions |
		Typ.	Max.	
C_{IN} (Address)	Input Capacitance	5	10	V_{bias} = 2.0V
C_{IN} ($\overline{CYREQ}$)	Input Capacitance	6	10	V_{CC} = 0V
C_{IN} ($\overline{BUSY}$)	Input Capacitance	20	30	f = 1 MHz

Note 2: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C. Load = 1 TTL, C_L = 15pF.

Conditions of Test: Input pulse amplitude: 3V, Input rise and fall times: 5ns between 1V and 2V. Measurements are made at 1.5V.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
t_{AA}	Address In to Address Out		7	12	ns	$\overline{BUSY}$ = V_{IH}
t_{BAM}	$\overline{BUSY}$ In to Address Out		21	28	ns	
t_{BAR}	$\overline{BUSY}$ In to Counter Out		18	27	ns	
t_{BK}	$\overline{BUSY}$ In to $\overline{ACK}$ Out		14	20	ns	$\overline{REFREQ}$ = V_{IH}, $\overline{CYREQ}$ = V_{IL}
t_{BR}	$\overline{BUSY}$ In to $\overline{REFON}$ Out		15	24	ns	
t_{BS}	$\overline{BUSY}$ In to $\overline{STARTCY}$ Out	4	7	14	ns	$\overline{CYREQ}$ = V_{IL}
t_{HOLD}	$\overline{BUSY}$ Hold Time	50			ns	External Delay between $\overline{STARTCY}$ and $\overline{BUSY}$
t_{RH}	$\overline{CYREQ}$ or $\overline{REFREQ}$ Hold Time	0			ns	External Delay after $\overline{BUSY}$
t_{RR}	$\overline{REFREQ}$ to $\overline{REFON}$		18	26	ns	$\overline{CYREQ}$ and $\overline{BUSY}$ = V_{IH}, No priority contention between $\overline{REFREQ}$ and $\overline{CYREQ}$
t_{RRC}	$\overline{REFREQ}$ to $\overline{REFON}$		33	45	ns	$\overline{BUSY}$ = V_{IH}
t_{RS}	$\overline{CYREQ}$ or $\overline{REFREQ}$ In to $\overline{STARTCY}$ Out	9	14	21	ns	$\overline{BUSY}$ = V_{IH}
t_{Setup}	$\overline{BUSY}$ Setup Time	120			ns	$\overline{BUSY}$ = V_{IL} During Refresh

Note 1: Typical values are for T_A = 25°C and nominal power supply voltages.

A. SYSTEM MEMORY CYCLE WITH MEMORY NOT BUSY
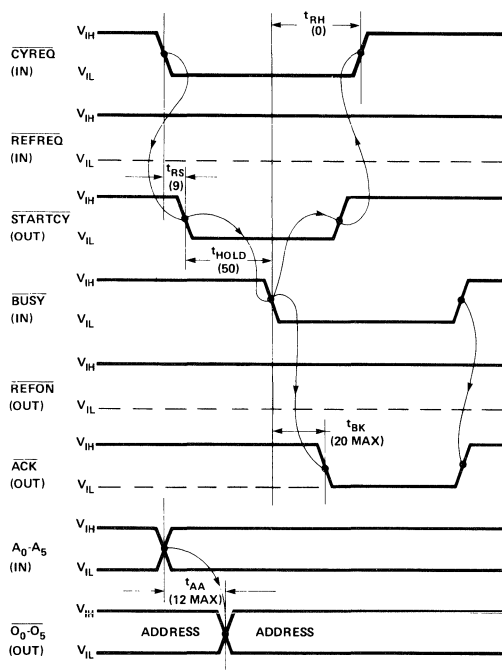
B. SYSTEM MEMORY CYCLE WITH MEMORY BUSY (FOLLOWING REFRESH CYCLE)

(Numbers in parentheses are minimum values in ns unless otherwise specified.)
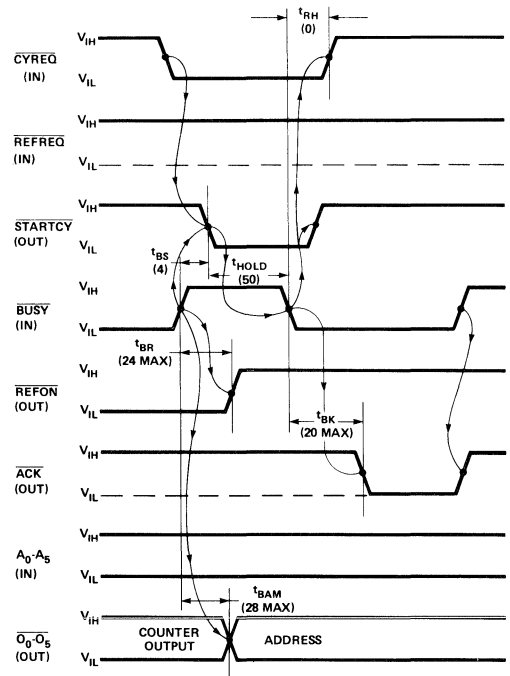
C. REFRESH MEMORY CYCLE WITH MEMORY NOT BUSY

D. REFRESH MEMORY CYCLE WITH MEMORY BUSY (FOLLOWING SYSTEM CYCLE)

(Numbers in parentheses are minimum values in ns unless otherwise specified.)
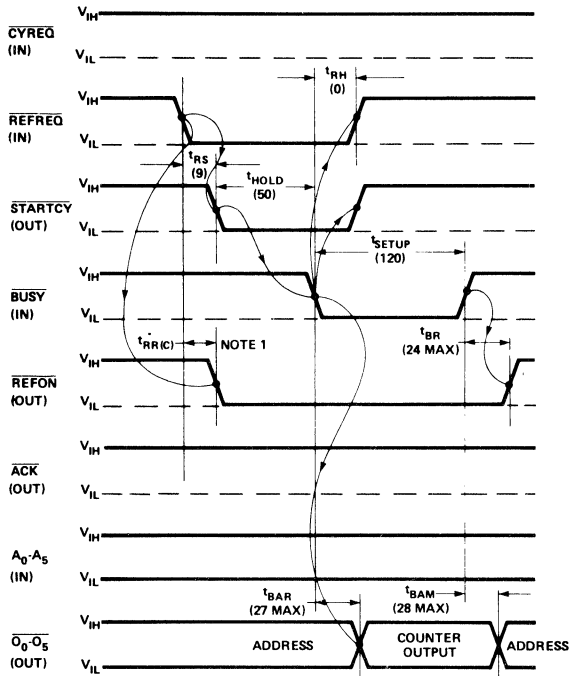
NOTE 1: t_{RR} (26ns MAX) IF PRIORITY CONTENTION IS ELIMINATED; t_{RRC}
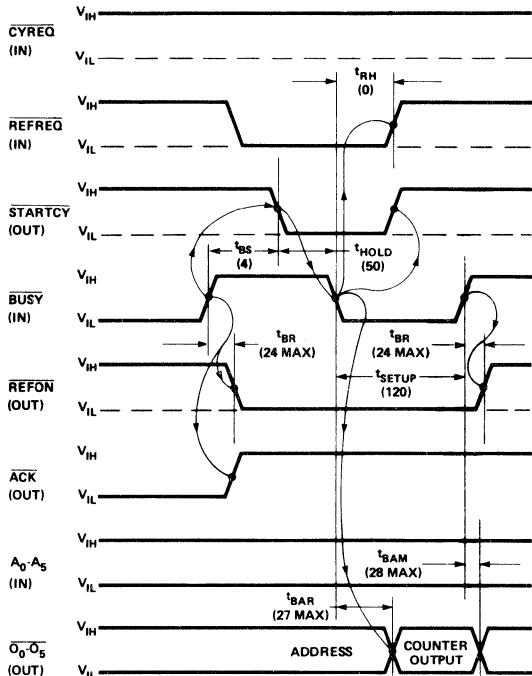
E. TYPICAL APPLICATION OF 3222 REFRESH CONTROLLER IN A 2107B SYSTEM
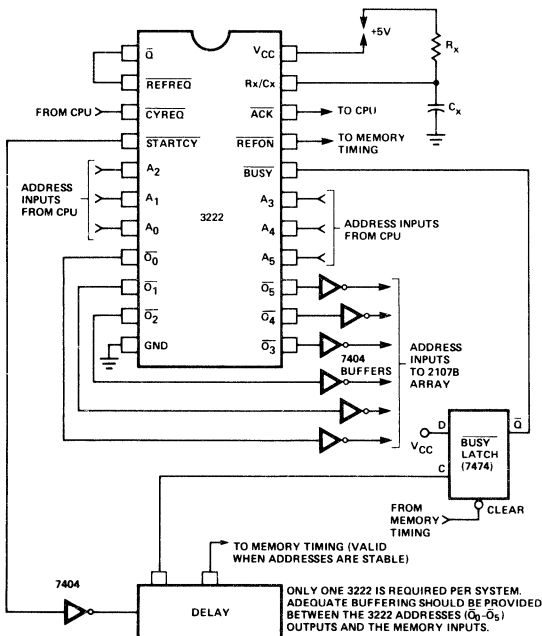
F. USE OF 3222 FOR REFRESH TIMING AND CONTROL IN A 2104A SYSTEM

ONLY ONE 3222 IS REQUIRED PER SYSTEM. ADEQUATE BUFFERING SHOULD BE PROVIDED BETWEEN THE 3222 ADDRESSES ($\overline{O}_0$-$\overline{O}_5$) OUTPUTS AND THE MEMORY INPUTS.

PIN NAMES AND FUNCTIONS

Pin No.	Pin Name	Function
1	$\overline{Q}$	Output of the internal Refresh Request latch. This pin may be connected to the Refresh Request input ($\overline{REFREQ}$) directly for asynchronous sequential mode refresh or indirectly through control logic for burst mode or synchronous mode refresh (see text).
2	$\overline{REFREQ}$	Refresh Request input (active when low). The request is honored only if the memory is not presently executing a cycle ($\overline{BUSY}$ high) and if a system cycle request did not occur first.
3	$\overline{CYREQ}$	System Memory Cycle Request input (active when low). The request is honored only if the memory is not presently executing a cycle ($\overline{BUSY}$ high) and if a refresh request did not occur first.
4	$\overline{STARTCY}$	Output signal indicating to external circuitry that a memory cycle (system or refresh) is to begin. See text for timing considerations for a refresh cycle.
5-7 15-17	A_0-A_5	Low order system address inputs. These addresses are multiplexed to the address output pins ($\overline{O}_0$-$\overline{O}_5$) during a system cycle.
8-10	$\overline{O}_0$-$\overline{O}_5$	Low order memory address outputs. During a system cycle these outputs give the low order (A_0-A_5) address of a memory access. During a refresh cycle these outputs give the refresh address (generated internal to the 3222).
11	GROUND	Ground.
18	$\overline{BUSY}$	An externally generated signal which the 3222 monitors to determine memory system status. If $\overline{BUSY}$ is high the memory is not busy and a system or refresh cycle may begin. If $\overline{BUSY}$ is low the memory is being accessed for a data I/O or refresh cycle and no other cycle may begin.
19	$\overline{REFON}$	The 3222 output which when low indicates the memory system is either ready to begin or is in a refresh cycle (Refresh On).
20	$\overline{ACK}$	The 3222 output which when low indicates the memory system is either ready to begin or is in a system cycle (system cycle request accepted and acknowledged).

Pin No.	Pin Name	Function
21	RX/CX	Connection point for the RC network which determines the refresh period for sequential refresh mode. (See Refresh Control section).
22	V_{CC}	+5 volt supply.

FUNCTIONAL DESCRIPTION

The Intel® 3222 performs the four basic functions of a refresh controller by:

1. Providing a refresh timing oscillator.
2. Generating six bit refresh addresses.
3. Multiplexing refresh and system addresses to the six low order address inputs ($\overline{O}_0$-$\overline{O}_5$).
4. Providing control signals for both refresh and memory cycle accesses.

As shown in the pin configuration figure, the 3222 has as inputs the six low order (A_0-A_5) system addresses. These addresses are internally multiplexed with six internally generated refresh addresses. The output of these multiplexers provide the six low order addresses to the memory array.

The block diagram shows the four main circuit categories of the 3222. An explanation of the workings of each of these categories is given in the Device Operation section from a users point of view.

DEVICE OPERATION

Operation of the Intel® 3222 Refresh Controller is most easily explained by considering five conditions presented by the three input control lines Cycle Request ($\overline{CYREQ}$), Refresh Request ($\overline{REFREQ}$), and System Busy ($\overline{BUSY}$). These conditions are:

1. System memory cycle request — memory not busy ($\overline{BUSY}$ = High)
2. System memory cycle request — memory busy ($\overline{BUSY}$ = Low)
3. Refresh cycle request — memory not busy ($\overline{BUSY}$ = High)
4. Refresh cycle request — memory busy ($\overline{BUSY}$ = Low)
5. Simultaneous system memory cycle and refresh cycle requests.

Condition 5 is actually a subset of the four previous conditions and is included for completeness.

As is implied in the five conditions, the response of the 3222 to both refresh and memory cycles is dependent on the state of the $\overline{BUSY}$ input. The $\overline{BUSY}$ signal is generated externally to the 3222 and, when low, defines the time when the memory is performing a cycle (refresh or memory access). It is important to assure that $\overline{BUSY}$ is low for the *entire* memory cycle time. Interference may occur in asynchronous memory systems if the $\overline{BUSY}$ input goes high prematurely. (An asynchronous memory system is one in which the refresh and memory cycle requests occur independent of each other.)

System Memory Cycle Request — Memory Not Busy

This section details operation of the 3222 when the memory is not busy and a request for a system memory cycle is made (See Figure A for timing sequences). The request for a memory cycle is made by the $\overline{CYREQ}$ input going low. The Start Cycle output $\overline{STARTCY}$ goes low at t_{RS} after $\overline{CYREQ}$. $\overline{STARTCY}$ is used for two purposes:

1. To set the external $\overline{BUSY}$ latch. (See Figure E.)
2. To initiate memory system timing (after appropriate delay).

The required delay time depends on system configuration and associated delay paths for both Chip Enable (2107B input signal) and system addresses.

The low going $\overline{BUSY}$ input causes the internally generated Start Cycle output to go high and the Acknowledge output $\overline{ACK}$ to go low (after t_{BK} time). The Acknowledge output confirms that the requested system memory cycle has been accepted by the 3222. Note that the cycle request input may be returned to the high state when the $\overline{BUSY}$ input goes low. However, at the designer's discretion, the cycle request line may remain low until "just prior" to $\overline{BUSY}$ returning high. (If $\overline{BUSY}$ goes high before $\overline{CYREQ}$ goes high, another memory access may inadvertently be started.)

When the memory is not busy and a cycle request has been made, the low order system address delay through the 3222 is t_{AA} nsec. When the 3222 is not busy, the low order system addresses (A_0-A_5) are gated through to the output ($\overline{O}_0$-$\overline{O}_5$) independent of any other input.

System Memory Cycle Request — Memory Busy

The major differences between a system memory cycle request when the system is busy and when it is not busy (as previously described) are:

1. The Start Cycle output $\overline{STARTCY}$ does not go low until t_{BS} after the rising edge of the $\overline{BUSY}$ input. (Even though the $\overline{CYREQ}$ input is low.)
2. Output addresses $\overline{O}_0$-$\overline{O}_5$ change at or before t_{AA} time if the previous cycle was a system cycle request and change at or before t_{BAM} if the previous cycle was a Refresh Cycle request. (Note that the longer delay is after a refresh cycle.) See Figure B for definition of terms.

Note that for a system memory cycle following a refresh cycle, the refresh on output $\overline{REFON}$ goes high at or before t_{BR} relative to $\overline{BUSY}$ going high. Since the Acknowledge output $\overline{ACK}$ can not go low until after t_{HOLD} there is no ambiguity between $\overline{REFON}$ and $\overline{ACK}$. The memory is always defined as being in a refresh cycle, system cycle or no cycle.

Refresh Cycle — Memory Not Busy

Operation of the 3222 for a refresh request with the memory not busy (see Figure C) is similar to a system cycle request under the same condition. A refresh cycle is initiated by the Refresh Request input ($\overline{REFREQ}$) going low. This low going input causes both the Start Cycle output, $\overline{STARTCY}$, and Refresh On output, $\overline{REFON}$, to go low at t

and t_{RRC} (or t_{RR}) time respectively. The low going edge of $\overline{STARTCY}$ is used to set the external $\overline{BUSY}$ latch low. As in the previous two cases, the $\overline{BUSY}$ input must remain low for the entire cycle required by the memory. As in the previous two cases, the low going $\overline{BUSY}$ drives the $\overline{STARTCY}$ output high.

Refresh Cycle — Memory Busy

For this condition, it is assumed that the previous cycle was a system access cycle. Timing conditions for this operation are shown in Figure D. Here, the $\overline{STARTCY}$ input goes low t_{BS} after $\overline{BUSY}$ returns high from the previous cycle. As before, $\overline{REFON}$ goes low t_{BR} after $\overline{BUSY}$ goes high. After t_{HOLD}, relative to $\overline{STARTCY}$, BUSY again goes low and places the low order refresh addresses on the address outputs ($\overline{O}_0$-$\overline{O}_5$) after t_{BAR} time. Internal refresh timing is performed in a manner identical to that described in Refresh Cycle-Memory Not Busy section.

Simultaneous Refresh and Memory System Cycle Request

The simultaneous request for a refresh and memory system access is almost a certainty in asynchronous systems. It is, therefore, necessary to have circuitry in any refresh controller capable of resolving the attendant ambiguity with minimum additional delay. The Intel® 3222 Refresh Controller has just such a circuit. (All timing parameters specified for asynchronous operation assume that a refresh and memory system request can occur at the same time.) A latch internal to the 3222 decides which signal ($\overline{CYREQ}$ or $\overline{REFREQ}$) it will accept if both occur simultaneously, and conditions the other control circuits appropriately. If a refresh cycle was accepted, $\overline{REFON}$ will go low at the appropriate time. If a memory system access was accepted then $\overline{ACK}$ will go low at the appropriate time.

Refresh Control

The 3222 controls both burst and distributed refresh modes. The burst refresh mode requires that $\overline{REFREQ}$ be generated externally to the 3222 since refresh is completed in 64 consecutive cycles every 2ms. A system requiring distributed refresh timing, however can be controlled either by the 3222 or by external circuitry. If refresh timing is to be controlled by the 3222 the output $\overline{Q}$ is tied to the $\overline{REFREQ}$ input. Timing is controlled by an oscillator internal to the 3222. The desired refresh timing interval is determined by:

1. $t_{REF} = .63 \, R_x C_x$
   r

   Where:
   t_{REF} = the total time between refreshes (e.g. 2msec) in msec.
   r = the number of rows to be refreshed on the memory device (for the 2107B r = 64).
   R_x = external timing resistance in $K\Omega$ (3K to 10K)
   C_x = external timing capacitance in μf. (0.005μf to 0.02μf)

The 3222's oscillator stability is guaranteed to be ±2% for a given part and ±6% from part to part, both over the ranges $0°C \leqslant T_A \leqslant 75°C$ and V_{CC} = 5.0V ±5%.

Figure F shows how the 3222 may be used to control refresh in a 2104A system.

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3232

ADDRESS MULTIPLEXER AND REFRESH COUNTER FOR 4K DYNAMIC RAMs

- **Ideal For 2104A**

- **Simplifies System Design**

- **Reduces Package Count**

- **Standard 24-Pin DIP**

- **Address Input to Output Delay: 9ns Maximum Driving 15pF, 25ns Maximum Driving 250pF**

- **Suitable For Either Distributed Or Burst Refresh**

- **Single Power Supply: +5 Volts ±10%**

The Intel® 3232 contains an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of up to 6 input addresses (or 4K bits for 64 x 64 organization). It multiplexes twelve bits of system supplied address to six output address pins. The device also contains a 6 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3232 makes it especially suitable for use with high speed N-channel RAMs like the 2104A.

The 3232 operates from a single +5 volt power supply and is specified for operation over a 0 to +75°C ambient temperature range.

PIN CONFIGURATION

$\overline{COUNT}$	1	24 V_{CC}
REFRESH ENABLE	2	23 ROW ENABLE
A_1	3	22 A_5
A_7	4	21 A_{11}
A_2	5	20 A_4
A_8	6 3232	19 A_{10}
A_0	7	18 A_3
A_6	8	17 A_9
$\overline{O}_0$	9	16 $\overline{O}_3$
$\overline{O}_2$	10	15 $\overline{O}_4$
$\overline{O}_1$	11	14 $\overline{O}_5$
GND	12	13 ZERO DETECT
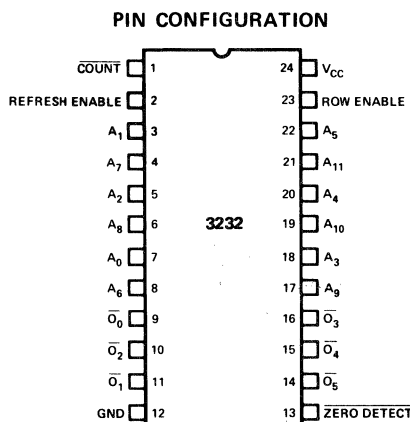
NOTE: A_0 THROUGH A_5 ARE ROW ADDRESSES.
A_6 THROUGH A_{11} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_5)
L	L	COLUMN ADDRESS (A_6 THROUGH A_{11})

$\overline{COUNT}$ – ADVANCES INTERNAL REFRESH COUNTER.
ZERO DETECT – INDICATES A ZERO IN THE REFRESH ADDRESS (USED IN BURST REFRESH MODE).

LOGIC DIAGRAM

6-148

Absolute Maximum Ratings*

Temperature Under Bias .... -65° to +125°C
Storage Temperature .... -65° to +160°C
All Input, Output, or
  Supply Voltages ....-0.5V to +7 Volts
Output Currents 100mA
Power Dissipation 1W

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

All Limits Apply for $V_{CC} = 5.0V \pm 10\%$, $T_A = 0°C$ to $+75°C$

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. (1)	MAX.		
I_F	Input Load Current		-0.04	-0.25	mA	$V_{IN} = 0.45V$
I_R	Input Leakage Current		0	10	μA	$V_{IN} = 5.5V$
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OL}	Output Low Voltage		0.25	0.40	V	$I_{OL} = 5mA$
V_{OH}	Output High Voltage ($\overline{O}_0$-$\overline{O}_5$)	2.8	4.0		V	$I_{OH} = -1mA$
V_{OH1}	Output High Voltage ($\overline{\text{Zero Detect}}$)	2.4	3.3		V	$I_{OH} = -1mA$
I_{CC}	Power Supply Current		100	150	mA	$V_{CC} = 5.5V$

Note 1.   Typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

A.C. Characteristics

All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to 75°C, Load = 1 TTL, C_L = 250pF, Unless Otherwise Specified.

SYMBOL	PARAMETER	MIN.	TYP.[1]	MAX.	UNIT	CONDITIONS
t_{AO}	Address Input to Output Delay		6	9	ns	Refresh Enable = Low [1] [2]
t_{AOI}	Address Input to Output Delay		16	25	ns	Refresh Enable = Low
t_{OO}	Row Enable to Output Delay	7	12	27	ns	Refresh Enable = Low [1] [2]
t_{OOI}	Row Enable to Output Delay	12	28	41	ns	Refresh Enable = Low
t_{EO}	Refresh Enable to Output Delay	7	14	27	ns	Note 1, 2
t_{EOI}	Refresh Enable to Output Delay	12	30	45	ns	
t_{CO}	$\overline{\text{Count}}$ to Output	15	40	60	ns	Refresh Enable = High [1] [2]
t_{COI}	$\overline{\text{Count}}$ to Output	20	55	80	ns	Refresh Enable = High
f_C	Counting Frequency	5			MHz	
t_{CPW}	$\overline{\text{Count}}$ Pulse Width	35			ns	
t_{CZ}	$\overline{\text{Count}}$ to $\overline{\text{Zero Detect}}$	15		70	ns	Note 2

Note 1: V_{CC} = 5.0V, T_A = 25°C
2: C_L = 15pF

A.C. TIMING WAVEFORMS (Typically used with 2104A)

NORMAL CYCLE
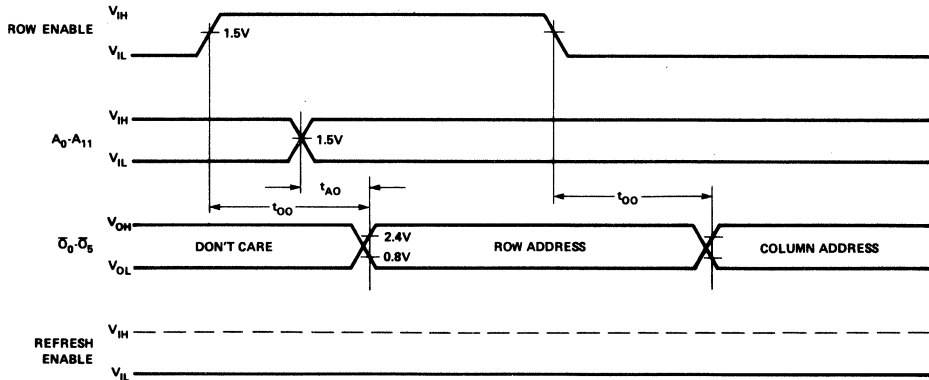
REFRESH CYCLE
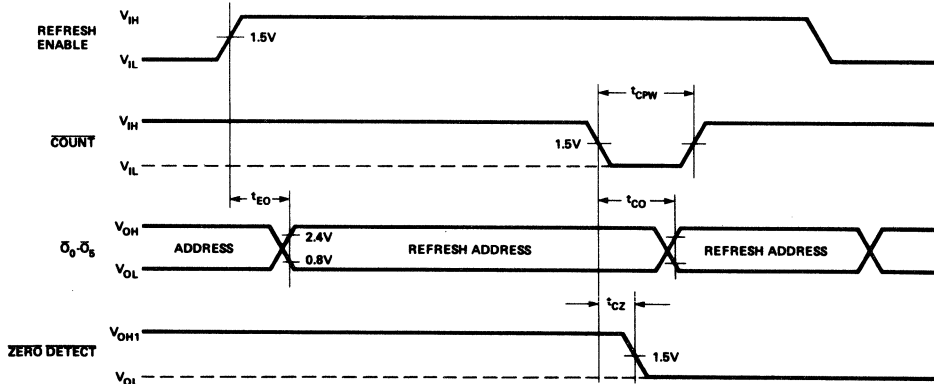
PIN NAMES AND FUNCTIONS

Pin. No.	Pin Name	Function
1	Count Input	Active low input increments internal six bit counter by one for each count pulse in.
2	Refresh Enable Input	Active high input which determines whether the 3232 is in refresh mode (H) or address enable (L).
7,3,5,18, 20,22	A_0-A_5 Inputs	Row Address inputs.
8,4,6,17, 19,21	A_6-A_{11} Inputs	Column address inputs.
9,11,10, 16,15,14	$\overline{O}_0$-$\overline{O}_5$ Outputs	Address outputs to memories. Inverted with respect to address inputs.
12	GND	Power supply ground.
13	Zero Detect Output	Active low output which senses that all six bits of refresh address in the counter are zero. Can be used in the burst mode to sense refresh completion.
23	Row Enable Input	High input selects row, low input selects column addresses of the driven memories.
24	V_{CC}	+5V power supply input.

DEVICE OPERATION

The Intel® 3232 Address Multiplexer/Refresh Counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh.

These functions are controlled by two signals: Refresh Enable and Row Enable, both of which are active high TTL

inputs. The truth table on page 1 shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter)
2. Row addresses (A_0 through A_5)
3. Column addresses (A_6 through A_{11})

Burst Refresh Mode

When refresh is requested, the refresh enable input is high. This input is ANDed with the 6 outputs of the internal 6 bit counter. At each Count pulse the counter increments by one, sequencing the outputs ($\overline{O}_0$-$\overline{O}_5$) through all 64 row addresses. When the counter sequences to all zeros, the Zero Detect output goes low signaling the end of the refresh sequence. Due to counter decoding spikes, the Zero Detect output is valid only after t_{CZ} following the low going edge of Count.

Distributed Refresh Mode

In the distributed refresh mode, one row is selected for refresh each ($t_{REFRESH}/n$) time where n = number of rows in the device and $t_{REFRESH}$ is the specified refresh rate for the device. For the 2104A $t_{REFRESH}$ = 2msec and n = 64, therefore one row is refreshed each 31 μsec. Following the refresh cycle at row n_x, the Count input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n_{x+1}. The Count input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address

All twelve system address lines are applied to the inputs of the 3232. When Refresh Enable is low and Row Enable is high, input addresses A_0-A_5 are gated to the outputs and applied to the driven memories. Conversely, when Row Enable is low (with Refresh Enable still low), input addresses A_6-A_{11} are gated to the outputs and applied to the driven memories.

Figure 1 shows a typical connection between the 3232 and the 2104A 4K dynamic RAM. When the memory devices are driven directly by the 3232, the address applied to the memory devices is the inverse of the address at the 3232 inputs due to the inverted outputs of the 3232. This should be remembered when checking out the memory system.

Figure 1. Typical Connection of 3232 and 2104 Memories.

intel®

3242
ADDRESS MULTIPLEXER AND REFRESH
COUNTER FOR 16K DYNAMIC RAMs

- **Ideal For 2116**

- **Simplifies System Design**

- **Reduces Package Count**

- **Standard 28-Pin DIP**

- **Suitable For Either Distributed Or Burst Refresh**

- **Single Power Supply: +5 Volts ±10%**

- **Address Input to Output Delay: 9ns Driving 15 pF, 25ns Driving 250pF**

The Intel® 3242 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of 64 or 128 cycles. It multiplexes 14 bits of system supplied address to 7 output address pins. The device also contains a 7 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3242 makes it especially suitable for use with high speed N-channel RAMs like the 2116.

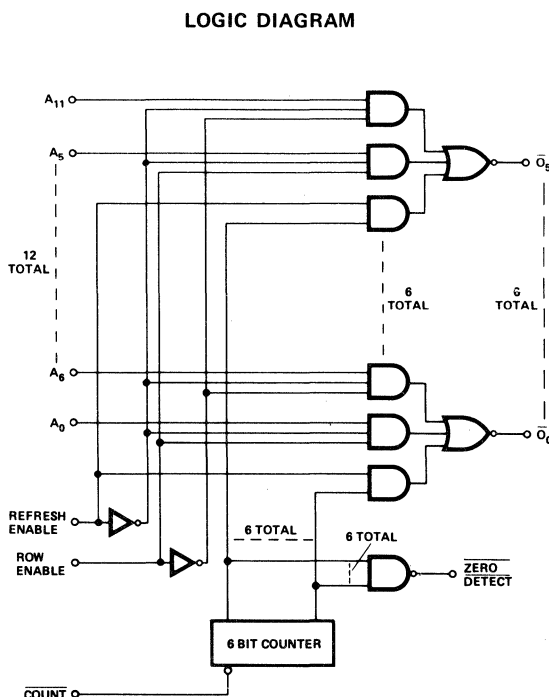The 3242 operates from a single +5 volt power supply and is specified for operation over a 0 to +75°C ambient temperature range. It is fabricated by means of Intel's highly reliable Schottky bipolar process and is packaged in a hermetically sealed 28 pin Type D package.

PIN CONFIGURATION

Pin	Signal		Pin	Signal
1	$\overline{COUNT}$		28	V_{CC}
2	REFRESH ENABLE		27	A_6
3	ROW ENABLE		26	A_{13}
4	N.C.		25	A_5
5	A_1		24	A_{12}
6	A_8		23	A_4
7	A_2		22	A_{11}
8	A_9		21	A_3
9	A_0		20	A_{10}
10	A_7		19	$\overline{O}_6$
11	$\overline{O}_0$		18	$\overline{O}_3$
12	$\overline{O}_2$		17	$\overline{O}_4$
13	$\overline{O}_1$		16	$\overline{O}_5$
14	GND		15	ZERO DETECT

(device center labeled 3242)

NOTE: A_0 THROUGH A_6 ARE ROW ADDRESSES.
A_7 THROUGH A_{13} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_6)
L	L	COLUMN ADDRESS (A_7 THROUGH A_{13})

$\overline{COUNT}$ – ADVANCES INTERNAL REFRESH COUNTER.
ZERO DETECT – INDICATES ZERO IN THE FIRST 6 SIGNIFICANT REFRESH COUNTER BITS (USED IN BURST REFRESH MODE)
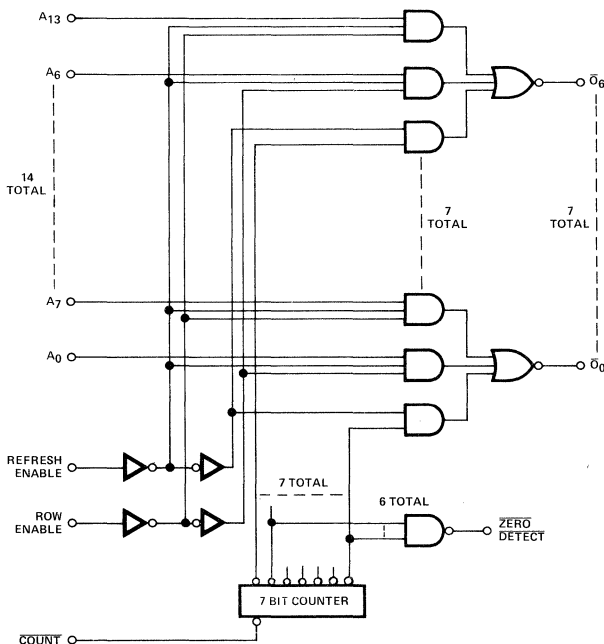
LOGIC DIAGRAM

A.C. Characteristics

All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to 75°C, Load = 1 TTL, C_L = 250pF, Unless Otherwise Specified.

SYMBOL	PARAMETER	MIN.	TYP.[1]	MAX.	UNIT	CONDITIONS
t_{AO}	Address Input to Output Delay		6	9	ns	Refresh Enable = Low[2][3]
t_{AO1}	Address Input to Output Delay		16	25	ns	Refresh Enable = Low
t_{OO}	Row Enable to Output Delay	7	12	27	ns	Refresh Enable = Low[2][3]
t_{OO1}	Row Enable to Output Delay	12	28	41	ns	Refresh Enable = Low
t_{EO}	Refresh Enable to Output Delay	7	14	27	ns	Notes 2, 3
t_{EO1}	Refresh Enable to Output Delay	12	30	45	ns	
t_{CO}	$\overline{\text{Count}}$ to Output	15	40	60	ns	Refresh Enable = High[2][3]
t_{CO1}	$\overline{\text{Count}}$ to Output	20	55	80	ns	Refresh Enable = High
f_C	Counting Frequency			5	MHz	
t_{CPW}	$\overline{\text{Count}}$ Pulse Width	35			ns	
t_{CZ}	$\overline{\text{Count}}$ to $\overline{\text{Zero Detect}}$	15		70	ns	Note 3

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

2. T_A = 25°C, V_{CC} = 5.0V.

3. C_L = 15 pF.

A.C. TIMING WAVEFORMS (Typically used with 2116)

NORMAL CYCLE
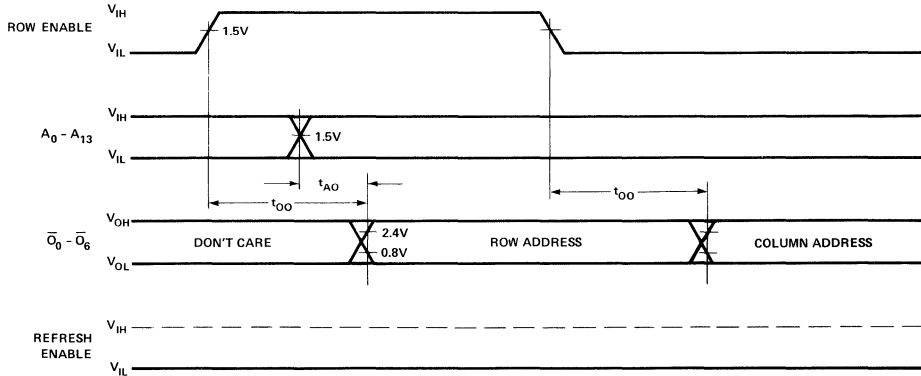
REFRESH CYCLE
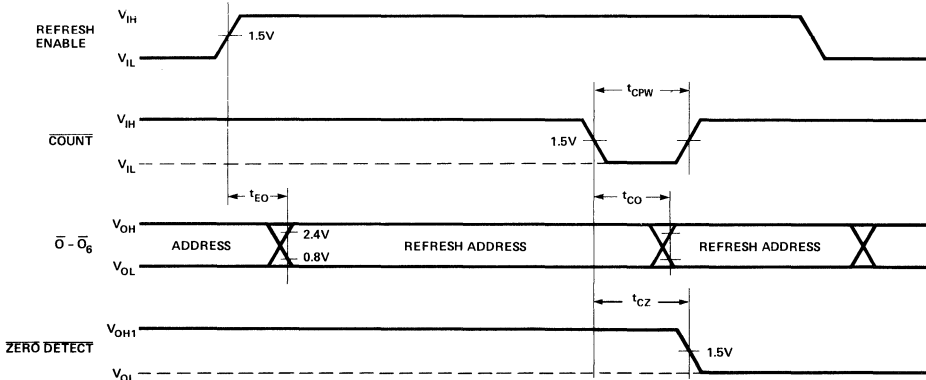
Absolute Maximum Ratings*

Temperature Under Bias .... -10° to +85°C
Storage Temperature .... -65° to +150°C
All Input, Output, or
    Supply Voltages .... -0.5V to +7 Volts
Output Currents 100mA
Power Dissipation 1W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

All Limits Apply for V_{CC} = 5.0V ±10%, T_A = 0°C to + 75°C

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. (1)	MAX.		
I_F	Input Load Current		-0.04	-0.25	mA	V_{IN} = 0.45V, Note 2
I_R	Input Leakage Current		0.01	10	μA	V_{IN} = 5.5V
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OL}	Output Low Voltage		0.25	0.40	V	I_{OL} = 8mA
V_{OH}	Output High Voltage ($\overline{O}_0 - \overline{O}_6$)	3.0	4.0		V	I_{OH} = −1mA
V_{OHI}	Output High Voltage ($\overline{Zero}\ \overline{Detect}$)	2.4	3.3		V	I_{OH} = −1mA
I_{CC}	Power Supply Current		105	165	mA	V_{CC} = 5.5V

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Inputs are high impedance, TTL compatible, and suitable for bus operation.

PIN NAMES AND FUNCTIONS

Pin No.	Pin Name	Function
1	$\overline{\text{Count}}$ Input*	Active low input increments internal 7-bit counter by one for each count pulse in.
2	Refresh Enable Input*	Active high input which determines whether the 3242 is in refresh mode (H) or address enable (L).
9,5,7,21, 23,25,27	A_0-A_6 Inputs*	Row address inputs.
10,6,8,20, 22,24,26	A_7-A_{13} Inputs*	Column address inputs.
11,13,12, 18,17,16, 19	$\overline{O}_0-\overline{O}_6$ Outputs	Address outputs to memories. Inverted with respect to address inputs.
14	GND	Power supply ground.
15	$\overline{\text{Zero}}$ $\overline{\text{Detect}}$ Output	Active low output which senses that the six low order bits of refresh address in the counter are zero. Can be used in the burst mode to sense refresh completion.
3	Row Enable Input*	High input selects row, low input selects column addresses of the driven memories.
28	V_{CC}	+5V power supply input.

*The inputs are high impedance, TTL compatible, and suitable for bus operation.

DEVICE OPERATION

The Intel® 3242 Address Multiplexer/Refresh Counter performs the following functions:

1. Row, Column and Refresh Address multiplexing.
2. Address Counting for burst or distributed refresh.

These functions are controlled by two signals: Refresh Enable and Row Enable, both of which are active high TTL inputs. The truth table on page 1 shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter).
2. Row addresses (A_0 through A_6).
3. Column addresses (A_7 through A_{13}).

Burst Refresh Mode

When refresh is requested, the refresh enable input is high. This input is ANDed with the seven outputs of the internal 7-bit counter. At each $\overline{\text{Count}}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0-\overline{O}_6$) through 128 row addresses. When the first six significant bits of the counter sequence to all zeros, the $\overline{\text{Zero Detect}}$ output goes low, signaling the end of the refresh sequence. Due to counter decoding spikes, the $\overline{\text{Zero Detect}}$ output is valid only after t_{CZ} following the low-going edge of $\overline{\text{Count}}$. The $\overline{\text{Zero Detect}}$ output used in this manner signals the completion of 64 refresh cycles. To use the 128-cycle burst refresh mode, an external flip-flop must be driven by the $\overline{\text{Zero Detect}}$.

Distributed Refresh Mode

In the distributed refresh mode, one row is selected for refresh each ($t_{REFRESH}/n$) time where n = number of refresh cycles required for the device and $t_{REFRESH}$ is the specified refresh rate for the device. For the 2116 $t_{REFRESH}$ = 2 msec and n = 128 or 64, therefore, one row is refreshed each 15.5 or 31 μsec, respectively. Following the refresh cycle at row n_x, the $\overline{\text{Count}}$ input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n_{x+1}. The $\overline{\text{Count}}$ input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address

All 14 system address lines are applied to the inputs of the 3242. When Refresh Enable is low and Row Enable is high, input addresses A_0-A_6 are gated to the outputs and applied to the driven memories. Conversely, when Row Enable is low (with Refresh Enable still low), input addresses A_7-A_{13} are gated to the outputs and applied to the driven memories. Figure 1 shows a typical connection between the 3242 and the 2116 16K dynamic RAM. When the memory devices are driven directly by the 3242, the address applied to the memory devices is the inverse of the address at the 3242 inputs due to the inverted outputs of the 3242. This should be remembered when checking out the memory system.
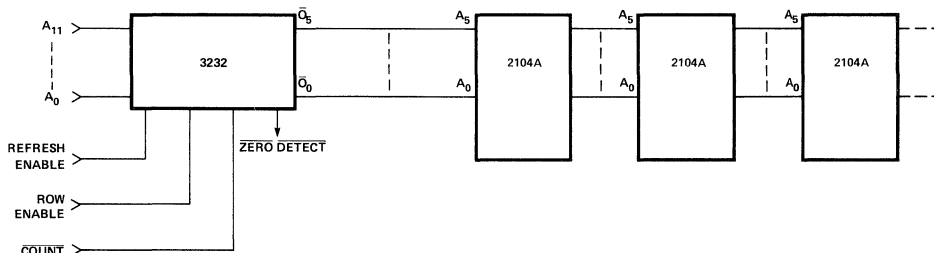
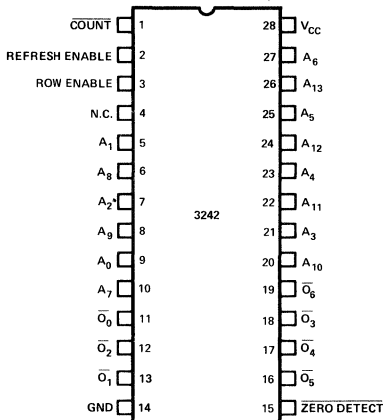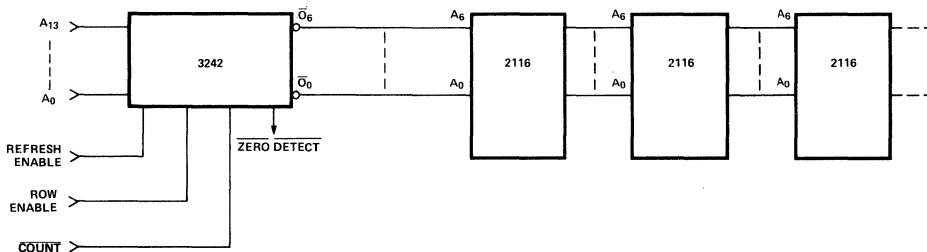

Figure 1. Typical Connection of 3242 and 2116 Memories.

PERIPHERALS and SUPPORT CIRCUITS

PERIPHERALS and SUPPORT CIRCUITS

intel®
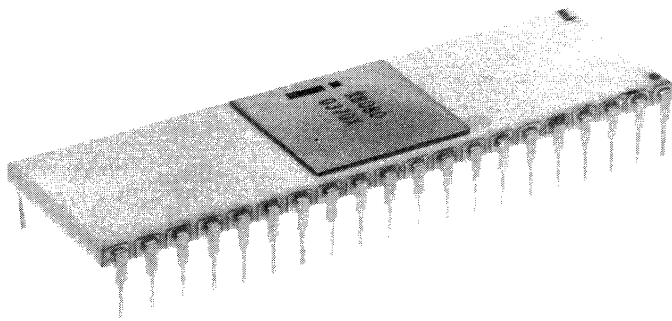
8205

HIGH SPEED 1 OUT OF 8 BINARY DECODER

- **I/O Port or Memory Selector**
- **Simple Expansion — Enable Inputs**
- **High Speed Schottky Bipolar Technology — 18ns Max. Delay**
- **Directly Compatible with TTL Logic Circuits**

- **Low Input Load Current — .25 mA max., 1/6 Standard TTL Input Load**
- **Minimum Line Reflection — Low Voltage Diode Input Clamp**
- **Outputs Sink 10 mA min.**
- **16-Pin Dual-In-Line Ceramic or Plastic Package**

The 8205 decoder can be used for expansion of systems which utilize input ports, output ports, and memory components with active low chip select input. When the 8205 is enabled, one of its eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 8205 allow easy system expansion. For very large systems, 8205 decoders can be cascaded such that each decoder can drive eight other decoders for arbitrary memory expansions.

The Intel®8205 is packaged in a standard 16 pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION

A_0	1	16	V_{CC}
A_1	2	15	O_0
A_2	3	14	O_1
E_1	4	13	O_2
E_2	5	12	O_3
E_3	6	11	O_4
O_7	7	10	O_5
GRD	8	9	O_6

8205

LOGIC SYMBOL

8205

Inputs: A_0, A_1, A_2, E_1, E_2, E_3
Outputs: O_0, O_1, O_2, O_3, O_4, O_5, O_6, O_7
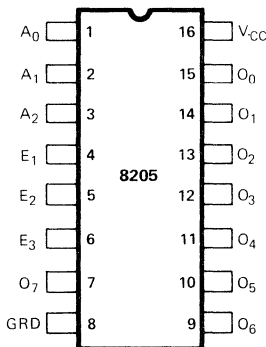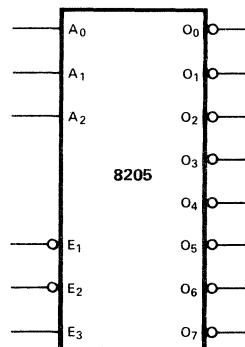
PIN NAMES

$A_0 \cdot A_2$	ADDRESS INPUTS
$\overline{E_1} \cdot \overline{E_3}$	ENABLE INPUTS
$\overline{O_0} \cdot \overline{O_7}$	DECODED OUTPUTS

ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

FUNCTIONAL DESCRIPTION

Decoder

The 8205 contains a one out of eight binary decoder. It accepts a three bit binary code and by gating this input, creates an exclusive output that represents the value of the input code.

For example, if a binary code of 101 was present on the A0, A1 and A2 address input lines, and the device was enabled, an active low signal would appear on the $\overline{O5}$ output line. Note that all of the other output pins are sitting at a logic high, thus the decoded output is said to be exclusive. The decoders outputs will follow the truth table shown below in the same manner for all other input variations.

Enable Gate

When using a decoder it is often necessary to gate the outputs with timing or enabling signals so that the exclusive output of the decoded value is synchronous with the overall system.

The 8205 has a built-in function for such gating. The three enable inputs ($\overline{E1}$, $\overline{E2}$, E3) are ANDed together and create a single enable signal for the decoder. The combination of both active "high" and active "low" device enable inputs provides the designer with a powerfully flexible gating function to help reduce package count in his system.

ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

APPLICATIONS OF THE 8205

The 8205 can be used in a wide variety of applications in microcomputer systems. I/O ports can be decoded from the address bus, chip select signals can be generated to select memory devices and the type of machine state such as in 8008 systems can be derived from a simple decoding of the state lines (S0, S1, S2) of the 8008 CPU.

I/O Port Decoder

Shown in the figure below is a typical application of the 8205. Address input lines are decoded by a group of 8205s (3). Each input has a binary weight. For example, A0 is assigned a value of 1 and is the LSB; A4 is assigned a value of 16 and is the MSB. By connecting them to the decoders as shown, an active low signal that is exclusive in nature and represents the value of the input address lines, is available at the outputs of the 8205s.

This circuit can be used to generate enable signals for I/O ports or any other decoder related application.

Note that no external gating is required to decode up to 24 exclusive devices and that a simple addition of an inverter or two will allow expansion to even larger decoder networks.

Chip Select Decoder

Using a very similar circuit to the I/O port decoder, an array of 8205s can be used to create a simple interface to a 24K memory system.
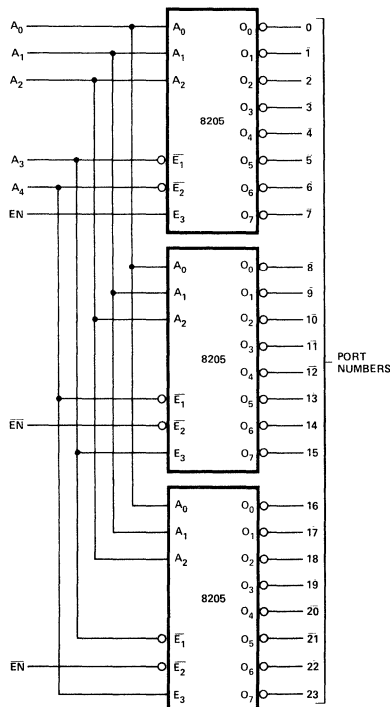
The memory devices used can be either ROM or RAM and are 1K in storage capacity. 8308s and 8102s are the devices typically used for this application. This type of memory device has ten (10) address inputs and an active "low" chip select ($\overline{CS}$). The lower order address bits A0-A9 which come from the microprocessor are "bussed" to all memory elements and the chip select to enable a specific device or group of devices comes from the array of 8205s. The output of the 8205 is active low so it is directly compatible with the memory components.

Basic operation is that the CPU issues an address to identify a specific memory location in which it wishes to "write" or "read" data. The most significant address bits A10-A14 are decoded by the array of 8205s and an exclusive, active low, chip select is generated that enables a specific memory device. The least significant address bits A0-A9 identify a specific location within the selected device. Thus, all addresses throughout the entire memory array are exclusive in nature and are non-redundant.

This technique can be expanded almost indefinitely to support even larger systems with the addition of a few inverters and an extra decoder (8205).

I/O Port Decoder
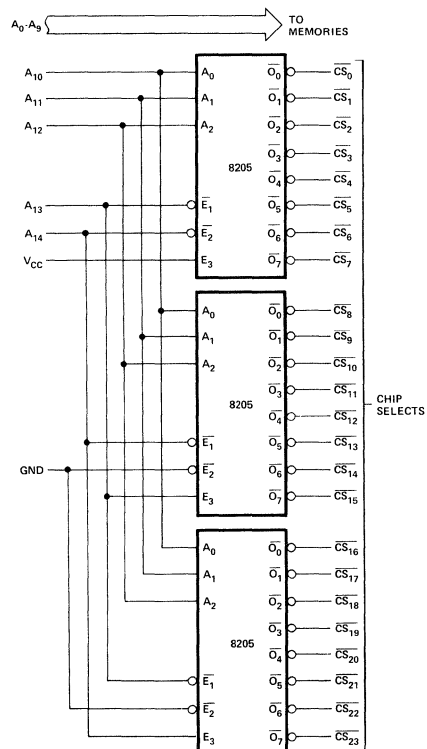
24K Memory Interface

Logic Element Example

Probably the most overlooked application of the 8205 is that of a general purpose logic element. Using the "on-chip" enabling gate, the 8205 can be configured to gate its decoded outputs with system timing signals and generate strobes that can be directly connected to latches, flip-flops and one-shots that are used throughout the system.

An excellent example of such an application is the "state decoder" in an 8008 CPU based system. The 8008 CPU issues three bits of information (S0, S1, S2) that indicate the nature of the data on the Data Bus during each machine state. Decoding of these signals is vital to generate strobes that can load the address latches, control bus discipline and general machine functions.

In the figure below a circuit is shown using the 8205 as the "state decoder" for an 8008 CPU that not only decodes the S0, S1, S2 outputs but gates these signals with the clock (phase 2) and the SYNC output of the 8008 CPU. The $\overline{T1}$

and $\overline{T2}$ decoded strobes can connect directly to devices like 8212s for latching the address information. The other decoded strobes can be used to generate signals to control the system data bus, memory timing functions and interrupt structure. RESET is connected to the enable gate so that strobes are not generated during system reset, eliminating accidental loading.

The power of such a circuit becomes evident when a single decoded strobe is logically broken down. Consider $\overline{T1}$ output, the boolean equation for it would be:

$$\overline{T1} = (\overline{S0 \cdot S1 \cdot S2}) \cdot (\overline{SYNC \cdot Phase\ 2 \cdot Reset})$$

A six input NAND gate plus a few inverters would be needed to implement this function. The seven remaining outputs would need a similar circuit to duplicate their function, obviously a substantial savings in components can be achieved when using such a technique.
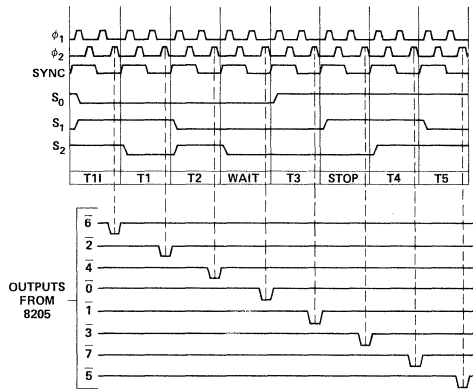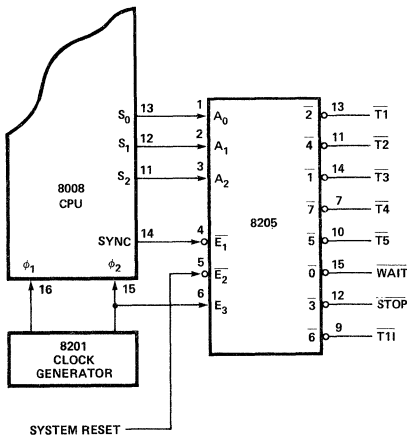
State Control Coding

S0	S1	S2	STATE
0	1	0	T1
0	1	1	T1I
0	0	1	T2
0	0	0	WAIT
1	0	0	T3
1	1	0	STOP
1	1	1	T4
1	0	1	T5

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias: Ceramic   −65°C to +125°C

                        Plastic   −65°C to +75°C

Storage Temperature   −65°C to +160°C

All Output or Supply Voltages   −0.5 to +7 Volts

All Input Voltages   −1.0 to +5.5 Volts

Output Currents   125 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS $T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$

8205

SYMBOL	PARAMETER	LIMIT MIN.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_F	INPUT LOAD CURRENT		−0.25	mA	$V_{CC} = 5.25V$, $V_F = 0.45V$
I_R	INPUT LEAKAGE CURRENT		10	µA	$V_{CC} = 5.25V$, $V_R = 5.25V$
V_C	INPUT FORWARD CLAMP VOLTAGE		−1.0	V	$V_{CC} = 4.75V$, $I_C = -5.0$ mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	$V_{CC} = 4.75V$, $I_{OL} = 10.0$ mA
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	$V_{CC} = 4.75V$, $I_{OH} = -1.5$ mA
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	$V_{CC} = 5.0V$
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	$V_{CC} = 5.0V$
I_{SC}	OUTPUT HIGH SHORT CIRCUIT CURRENT	−40	−120	mA	$V_{CC} = 5.0V$, $V_{OUT} = 0V$
V_{OX}	OUTPUT "LOW" VOLTAGE @ HIGH CURRENT		0.8	V	$V_{CC} = 5.0V$, $I_{OX} = 40$ mA
I_{CC}	POWER SUPPLY CURRENT		70	mA	$V_{CC} = 5.25V$

TYPICAL CHARACTERISTICS

OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE

OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE

DATA TRANSFER FUNCTION
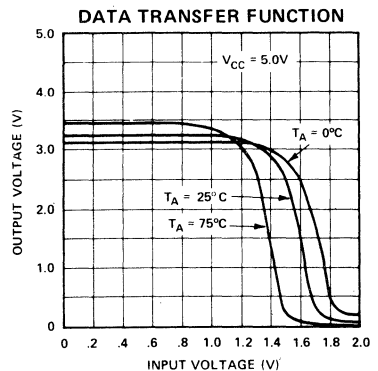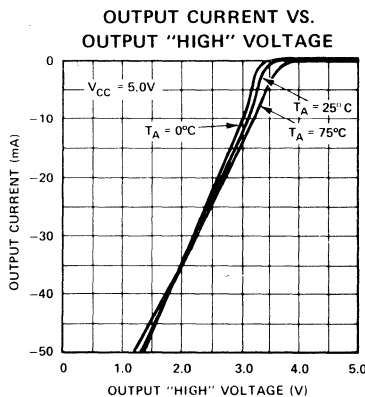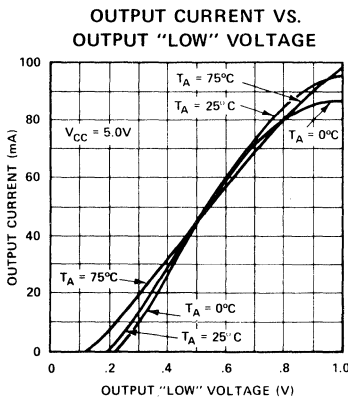
SWITCHING CHARACTERISTICS

CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec between 1V and 2V

Measurements are made at 1.5V

TEST LOAD:

V_{CC}

390 Ω

C_L 2K
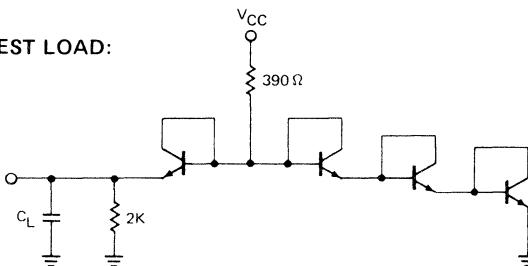
All Transistors 2N2369 or Equivalent. C_L = 30 pF

TEST WAVEFORMS

ADDRESS OR ENABLE
INPUT PULSE

t_{+-}, t_{++} t_{-+}, t_{--}
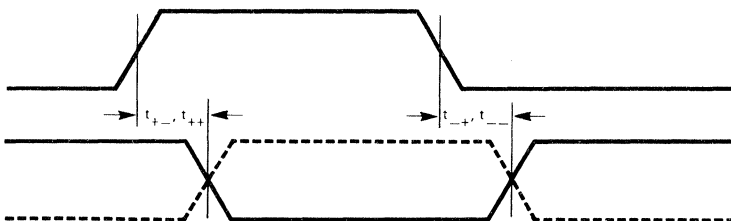
OUTPUT

A.C. CHARACTERISTICS T_A = 0°C to +75°C, V_{CC} = 5.0V ±5% unless otherwise specified.

SYMBOL	PARAMETER		MAX. LIMIT	UNIT	TEST CONDITIONS
t_{++}	ADDRESS OR ENABLE TO OUTPUT DELAY		18	ns	
t_{-+}			18	ns	
t_{+-}			18	ns	
t_{--}			18	ns	
C_{IN} [1]	INPUT CAPACITANCE	P8205	4(typ.)	pF	f = 1 MHz, V_{CC} = 0V
		C8205	5(typ.)	pF	V_{BIAS} = 2.0V, T_A = 25°C

1. This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

ADDRESS OR ENABLE TO OUTPUT
DELAY VS. LOAD CAPACITANCE

V_{CC} = 5.0V
T_A = 25°C

t_{+-}, t_{--}
t_{-+}
t_{++}

ADDRESS OR ENABLE TO OUTPUT DELAY (ns)

LOAD CAPACITANCE (pF)
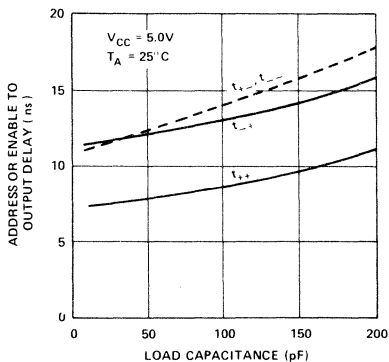
ADDRESS OR ENABLE TO OUTPUT
DELAY VS. AMBIENT TEMPERATURE
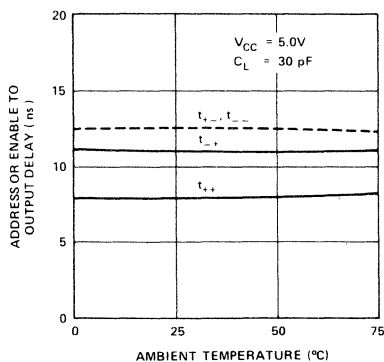
V_{CC} = 5.0V
C_L = 30 pF

t_{+-}, t_{--}
t_{-+}
t_{++}

ADDRESS OR ENABLE TO OUTPUT DELAY (ns)

AMBIENT TEMPERATURE (°C)

intel®

8212

EIGHT-BIT INPUT/OUTPUT PORT

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current — .25 mA Max.
- Three State Outputs
- Outputs Sink 15 mA

- 3.65V Output High Voltage for Direct Interface to 8080 CPU or 8008 CPU
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

PIN CONFIGURATION

PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM
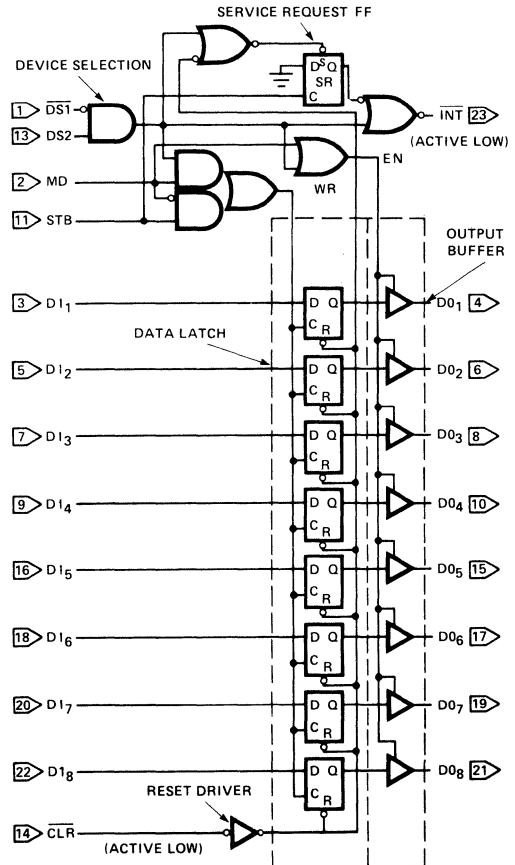
FUNCTIONAL DESCRIPTION

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state)

This high-impedance state allows the designer to connect the 8212 directly onto the microprocessor bi-directional data bus.

Control Logic

The 8212 has control inputs $\overline{DS1}$, DS2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS1}$, DS2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS1}$ is low and DS2 is high ($\overline{DS1} \cdot DS2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS1} \cdot DS2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS1} \cdot DS2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

This input is used as the clock (C) to the data latch for the input mode MD = 0 and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The (SR) flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS1} \cdot DS2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.
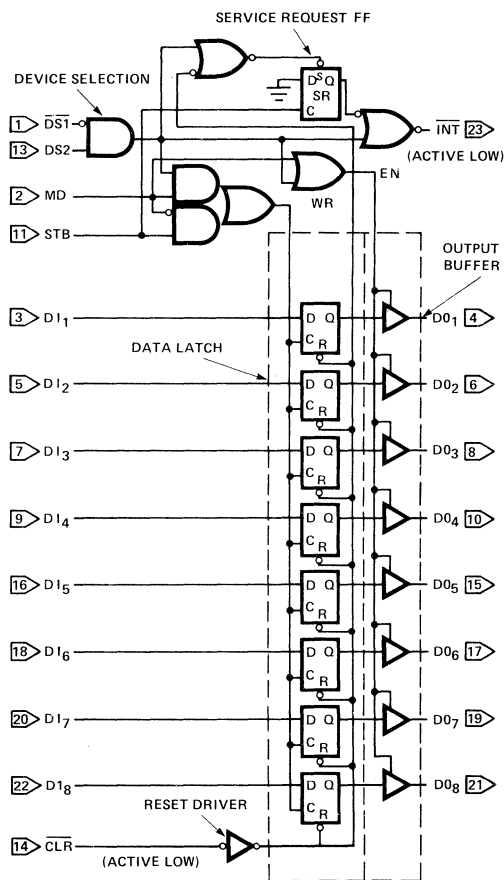
STB	MD	($\overline{DS1} \cdot DS2$)	DATA OUT EQUALS
0	0	0	3-STATE
1	0	0	3-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

CLR	($\overline{DS1} \cdot DS2$)	STB	*SR	INT
0	0	0	1	1
0	1	0	1	0
1	0	⌐	0	0
1	1	0	0	0
1	0	0	1	1
1	1	⌐	1	0

*INTERNAL SR FLIP-FLOP

$\overline{CLR}$ — RESETS DATA LATCH
  SETS SR FLIP-FLOP
  (NO EFFECT ON OUTPUT BUFFER)

Applications Of The 8212 -- For Microcomputer Systems

I	Basic Schematic Symbol	VII	8080 Status Latch
II	Gated Buffer	VIII	8008 System
III	Bi-Directional Bus Driver	IX	8080 System:
IV	Interrupting Input Port		8 Input Ports
V	Interrupt Instruction Port		8 Output Ports
VI	Output Port		8 Level Priority Interrupt

I. Basic Schematic Symbols

Two examples of ways to draw the 8212 on system schematics—(1) the top being the detailed view showing pin numbers, and (2) the bottom being the symbolic view showing the system input or output as a system bus (bus containing 8 parallel lines). The output to the data bus is symbolic in referencing 8 parallel lines.

BASIC SCHEMATIC SYMBOLS
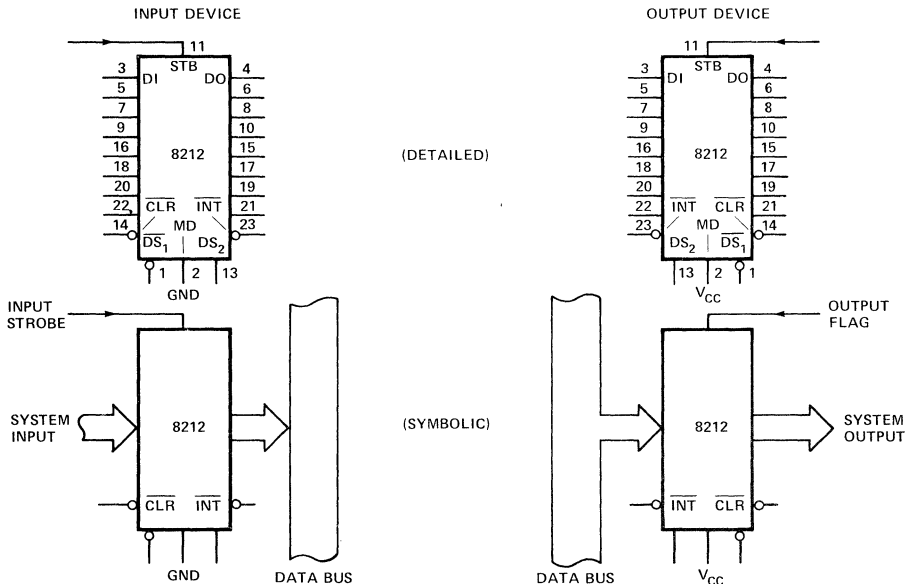
II. Gated Buffer (3 - STATE)

The simplest use of the 8212 is that of a gated buffer. By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS1}$ and DS2.

When the device selection logic is false, the outputs are 3-state.

When the device selection logic is true, the input data from the system is directly transferred to the output. The input data load is 250 micro amps. The output data can sink 15 milli amps. The minimum high output is 3.65 volts.

GATED BUFFER
3-STATE
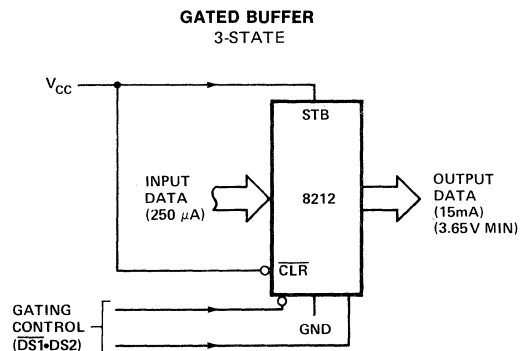
III. Bi-Directional Bus Driver

A pair of 8212's wired (back-to-back) can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS1}$ on the first 8212 and to DS2 on the second. One device is active, and acting as a straight through buffer the other is in 3-state mode. This is a very useful circuit in small system design.

BI-DIRECTIONAL BUS DRIVER
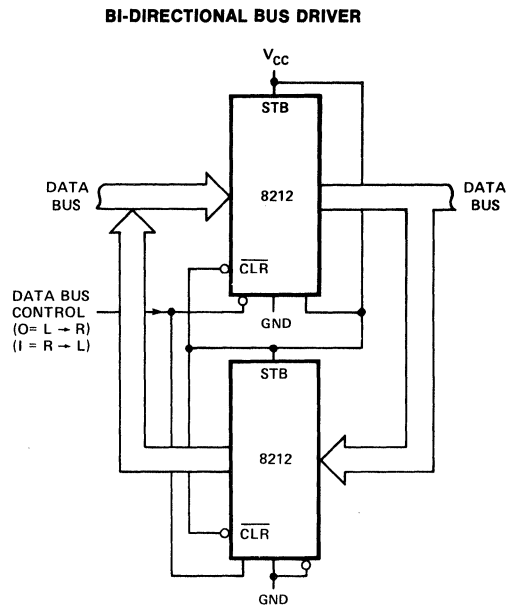
IV. Interrupting Input Port

This use of an 8212 is that of a system input port that accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true — enabling the system input data onto the data bus.

INTERRUPTING INPUT PORT
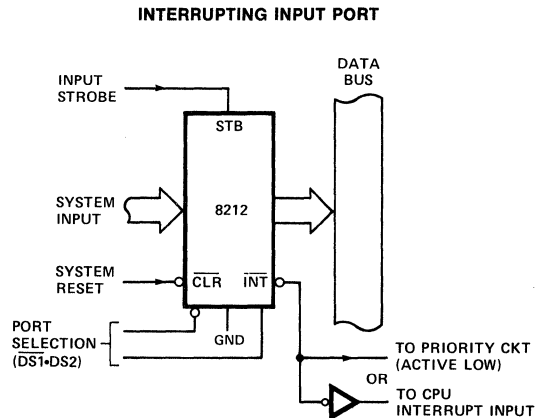
V. Interrupt Instruction Port

The 8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus).

INTERRUPT INSTRUCTION PORT
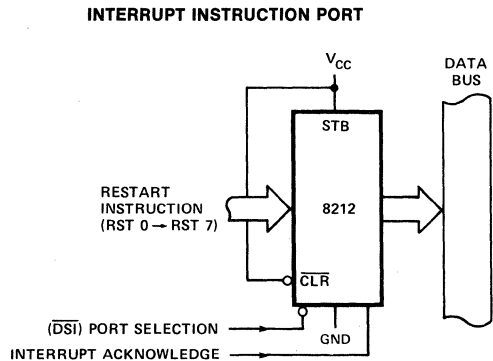
VI. Output Port (With Hand-Shaking)

The 8212 can be used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of data. The selection of the port comes from the device selection logic. ($\overline{DS1} \cdot DS2$)

OUTPUT PORT (WITH HAND-SHAKING)
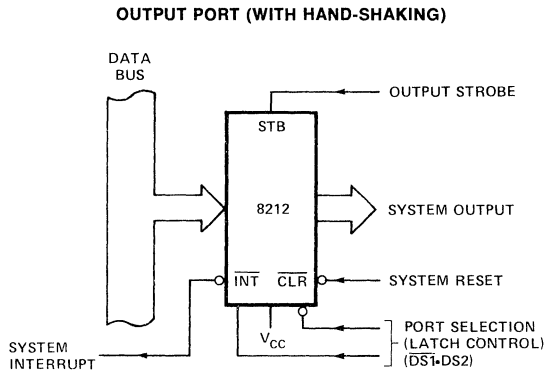
VII. 8080 Status Latch

Here the 8212 is used as the status latch for an 8080 microcomputer system. The input to the 8212 latch is directly from the 8080 data bus. Timing shows that when the SYNC signal is true, which is connected to the DS2 input and the phase 1 signal is true, which is a TTL level coming from the clock generator; then, the status data will be latched into the 8212.

Note: The mode signal is tied high so that the output on the latch is active and enabled all the time.

It is shown that the two areas of concern are the bidirectional data bus of the microprocessor and the control bus.

8080 STATUS LATCH
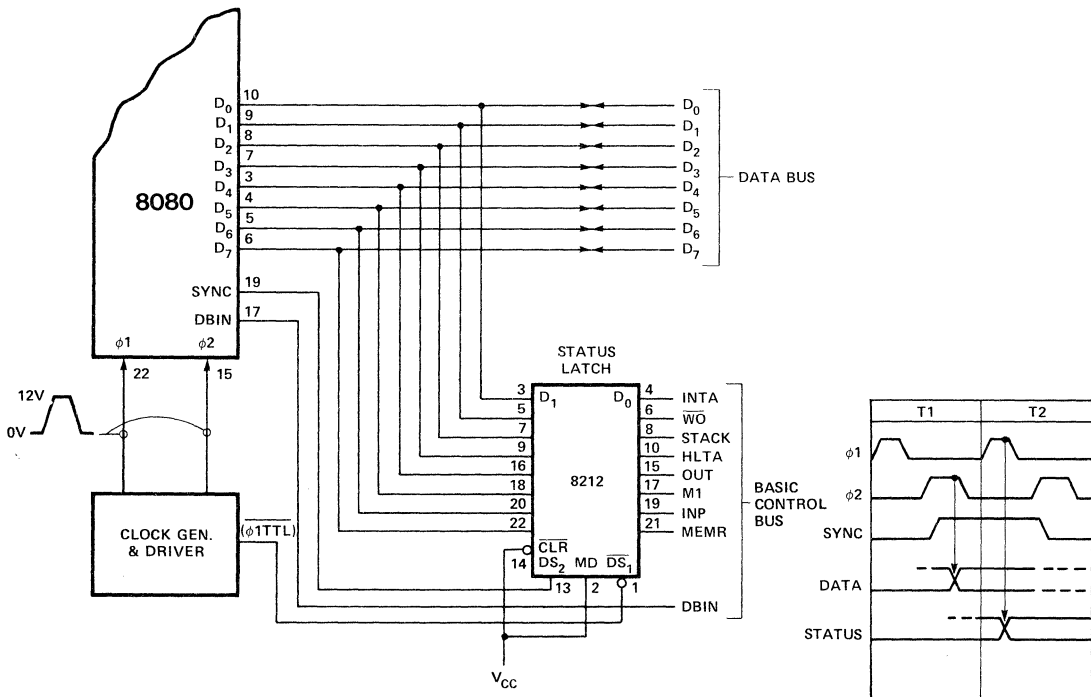
ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias Plastic . . $-65°C$ to $+75°C$

Storage Temperature . . . . $-65°C$ to $+160°C$

All Output or Supply Voltages . . . . -0.5 to $+7$ Volts

All Input Voltages . . . . -1.0 to 5.5 Volts

Output Currents . . . . 125 mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = 0°C$ to $+75°C$ $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current ACK, DS_2, CR, DI_1-DI_8 Inputs			$-.25$	mA	$V_F = .45V$
I_F	Input Load Current MD Input			$-.75$	mA	$V_F = .45V$
I_F	Input Load Current DS_1 Input			-1.0	mA	$V_F = .45V$
I_R	Input Leakage Current ACK, DS, CR, DI_1-DI_8 Inputs			10	μA	$V_R = 5.25V$
I_R	Input Leakage Current MO Input			30	μA	$V_R = 5.25V$
I_R	Input Leakage Current DS_1 Input			40	μA	$V_R = 5.25V$
V_C	Input Forward Voltage Clamp			-1	V	$I_C = -5$ mA
V_{IL}	Input "Low" Voltage			.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	$I_{OL} = 15$ mA
V_{OH}	Output "High" Voltage	3.65	4.0		V	$I_{OH} = -1$ mA
I_{SC}	Short Circuit Output Current	-15		-75	mA	$V_O = 0$ V
$|I_O|$	Output Leakage Current High Impedance State			20	μA	$V_O = .45V/5.25V$
I_{CC}	Power Supply Current		90	130	mA	

TYPICAL CHARACTERISTICS

INPUT CURRENT VS. INPUT VOLTAGE
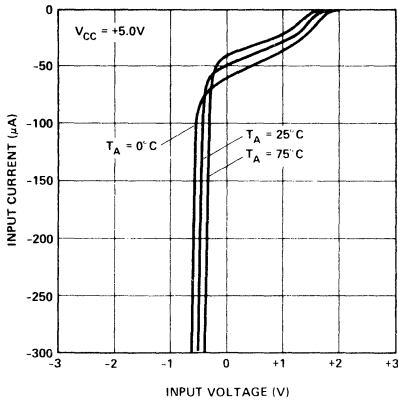
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE
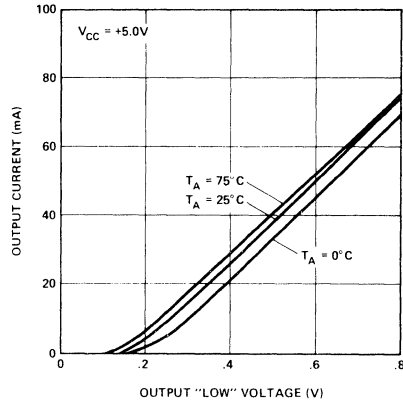
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE
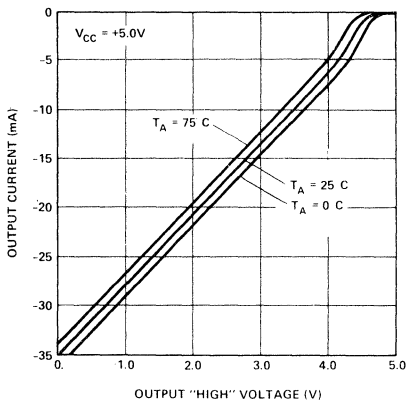
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE
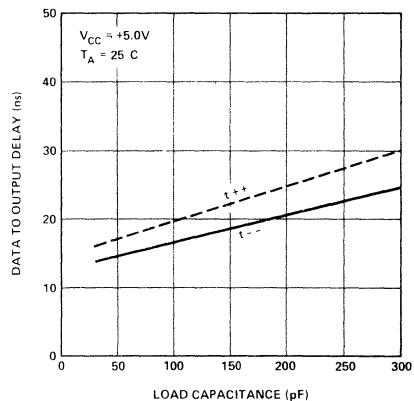
DATA TO OUTPUT DELAY VS. TEMPERATURE
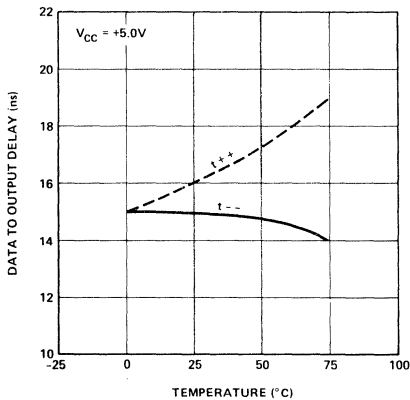
WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE

TIMING DIAGRAM

DATA

STB or $\overline{DS}_1 \cdot DS_2$

t_{PW} t_H

1.5V 1.5V

t_{WE}

OUTPUT

1.5V

$\overline{DS}_1 \cdot DS_2$

1.5V 1.5V

t_E (SEE NOTE BELOW) t_D

.5V

OUTPUT

V_{OH}

t_{PW}

V_{OL}

$\overline{CLR}$

1.5V 1.5V

.5V

t_C

DO

1.5V

DATA

1.5V 1.5V

t_{SET} t_H

STB or $\overline{DS}_1 \cdot DS_2$

1.5V

t_{PD}

OUTPUT

1.5V

STB

1.5V

t_{PW}

$\overline{DS}_1 \cdot DS_2$

1.5V

t_{PW} t_S

$\overline{INT}$

1.5V
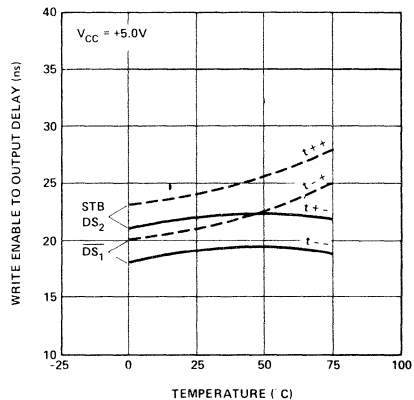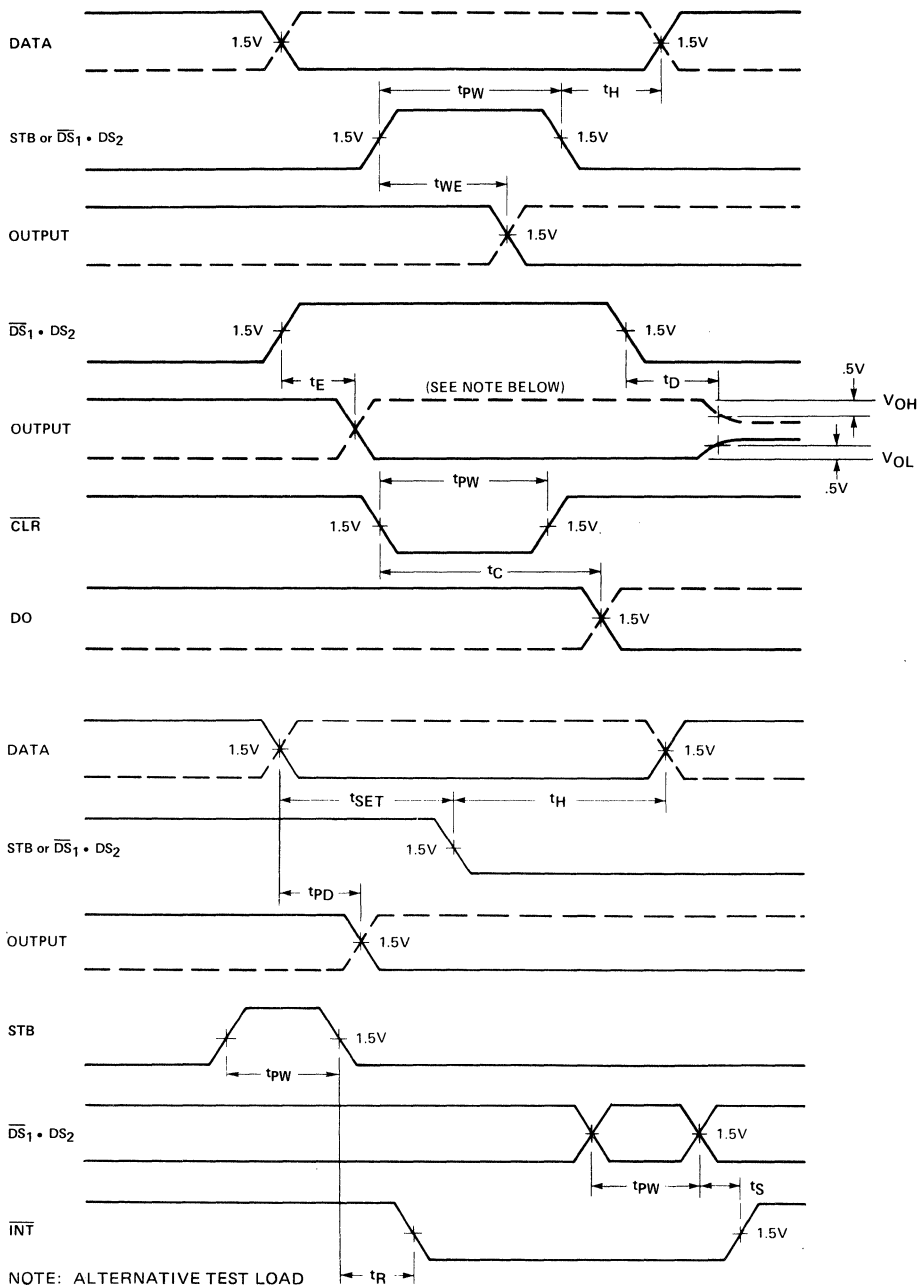
NOTE: ALTERNATIVE TEST LOAD
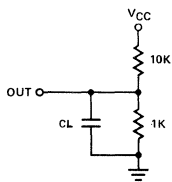
t_R

V_{CC}

10K

OUT

C_L 1K

A.C. CHARACTERISTICS

$T_A = 0°C$ to $+75°C$ $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{pw}	Pulse Width	30			ns	
t_{pd}	Data To Output Delay			30	ns	
t_{we}	Write Enable To Output Delay			40	ns	
t_{set}	Data Setup Time	15			ns	
t_h	Data Hold Time	20			ns	
t_r	Reset To Output Delay			40	ns	
t_s	Set To Output Delay			30	ns	
t_e	Output Enable/Disable Time			45	ns	
t_c	Clear To Output Delay			55	ns	

CAPACITANCE* $F = 1\,MHz$ $V_{BIAS} = 2.5V$ $V_{CC} = +5V$ $T_A = 25°C$

Symbol	Test	LIMITS	
		Typ.	Max.
C_{IN}	DS_1 MD Input Capacitance	9 pF	12 pF
C_{IN}	DS_2, CK, ACK, DI_1-DI_8 Input Capacitance	5 pF	9 pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8 pF	12 pF

*This parameter is sampled and not 100% tested.

SWITCHING CHARACTERISTICS

CONDITIONS OF TEST

Input Pulse Amplitude = 2.5 V
Input Rise and Fall Times 5 ns
Between 1V and 2V Measurements made at 1.5V
with 15 mA & 30 pF Test Load

TEST LOAD

15 mA & 30 pF

V_{CC}

300

TO D.U.T.

*30 pF

600
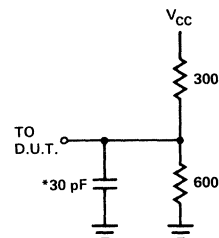
* INCLUDING JIG & PROBE CAPACITANCE

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M8212
EIGHT-BIT INPUT/OUTPUT PORT

- **Fully Parallel 8-Bit Data Register and Buffer**
- **Service Request Flip-Flop for Interrupt Generation**
- **Low Input Load Current: .25 mA Max.**
- **Three-State Outputs**
- **Full Military Temperature Range -55°C To +125°C**

- **3.4V Output High Voltage for Direct Interface to M8080A CPU**
- **Asynchronous Register Clear**
- **Replaces Buffers, Latches and Multiplexers in Microcomputer Systems**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**
- **24-Pin Dual In-Line Package**

The M8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

PIN CONFIGURATION

$\overline{DS}_1$	1	24	V_{CC}
MD	2	23	$\overline{INT}$
DI_1	3	22	DI_8
DO_1	4	21	DO_8
DI_2	5	20	DI_7
DO_2	6	19	DO_7
DI_3	7	18	DI_6
DO_3	8	17	DO_6
DI_4	9	16	DI_5
DO_4	10	15	DO_5
STB	11	14	$\overline{CLR}$
GND	12	13	DS_2

M8212

PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS}_1$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . −55°C to +125°C

Storage Temperature . . . . −65°C to +160°C

All Output or Supply Voltages . . . . −0.5 to +7 Volts

All Input Voltages . . . . −1.0 to 5.5 Volts

Output Currents . . . . 125 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = −55°C to +125°C V_{CC} = +5V ±10%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current ACK, DS_2, CR, DI_1-DI_8 Inputs			−.25	mA	V_F = .45V
I_F	Input Load Current MD Input			−.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			−1.0	mA	V_F = .45V
I_R	Input Leakage Current ACK, DS, CR, DI_1-DI_8 Inputs			10	μA	V_R = V_{CC}
I_R	Input Leakage Current MD Input			30	μA	V_R = V_{CC}
I_R	Input Leakage Current DS_1 Input			40	μA	V_R = V_{CC}
V_C	Input Forward Voltage Clamp			−1.2	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			.80	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 10mA
V_{OH}	Output "High" Voltage	3.4	4.0		V	I_{OH} = −.5mA
I_{OS}	Short Circuit Output Current	−15		−75	mA	V_{CC} = 5.0V
$\lvert I_O \rvert$	Output Leakage Current High Impedance State			20	μA	V_O = .45V to V_{CC}
I_{CC}	Power Supply Current		90	145	mA	

A.C. CHARACTERISTICS

$T_A = -55°C$ to $+125°C$ $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
t_{PW}	Pulse Width	40		ns	
t_{PD}	Data To Output Delay		30	ns	NOTE 1
t_{WE}	Write Enable To Output Delay		50	ns	NOTE 1
t_{SET}	Data Setup Time	20		ns	
t_H	Data Hold Time	30		ns	
t_R	Reset To Output Delay		55	ns	NOTE 1
t_S	Set To Output Delay		35	ns	NOTE 1
t_E	Output Enable/Disable Time		50	ns	NOTE 1
t_C	Clear To Output Delay		65	ns	NOTE 1

CAPACITANCE $F = 1MHz$ $V_{BIAS} = 2.5V$ $V_{CC} = +5V$ $T_A = 25°C$

Symbol	Test	LIMITS	
		Typ.	Max.
C_{IN}	$\overline{DS}_1$, MD Input Capacitance	9 pF	12 pF
C_{IN}	DS_2, $\overline{CLR}$, STB, DI_1-DI_8 Input Capacitance	5 pF	9 pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8 pF	12 pF

SWITCHING CHARACTERISTICS

CONDITIONS OF TEST
Input Pulse Amplitude = 2.5V
Input Rise and Fall Times: 5 ns between 1V and 2V

TEST LOAD
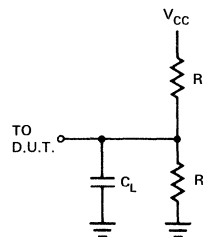
NOTE 1:	TEST	C_L	R_1	R_2
	t_{PD}, t_{WE}, t_R, t_S, t_C	30pF	300Ω	600Ω
	t_E, ENABLE↑	30pF	10KΩ	1KΩ
	t_E, ENABLE↓	30pF	300Ω	600Ω
	t_E, DISABLE↑	5pF	300Ω	600Ω
	t_E, DISABLE↓	5pF	10KΩ	1KΩ

TIMING DIAGRAM

TYPICAL CHARACTERISTICS

INPUT CURRENT VS. INPUT VOLTAGE

$V_{CC} = +5.0V$

INPUT CURRENT (μA)

$T_A = 0\ C$ $T_A = 25\ C$ $T_A = 75\ C$

INPUT VOLTAGE (V)

OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE

$V_{CC} = +5.0V$

OUTPUT CURRENT (mA)

$T_A = 75\ C$ $T_A = 25\ C$ $T_A = 0\ C$

OUTPUT "LOW" VOLTAGE (V)

OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE

$V_{CC} = +5.0V$

OUTPUT CURRENT (mA)

$T_A = 75\ C$ $T_A = 25\ C$ $T_A = 0\ C$

OUTPUT "HIGH" VOLTAGE (V)

DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE

$V_{CC} = +5.0V$
$T_A = 25\ C$

DATA TO OUTPUT DELAY (ns)

$t + +$ $t - -$

LOAD CAPACITANCE (pF)

DATA TO OUTPUT DELAY VS. TEMPERATURE

$V_{CC} = +5.0V$

DATA TO OUTPUT DELAY (ns)

$t + +$ $t - -$

TEMPERATURE (°C)

WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE

$V_{CC} = +5.0V$

WRITE ENABLE TO OUTPUT DELAY (ns)

$t + +$ $t - +$ $t + -$ $t - -$

STB
DS_2

$\overline{DS_1}$

TEMPERATURE (C)

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8214
PRIORITY INTERRUPT CONTROL UNIT

- ■ Eight Priority Levels
- ■ Current Status Register
- ■ Priority Comparator

- ■ Fully Expandable
- ■ High Performance (50ns)
- ■ 24-Pin Dual In-Line Package

The 8214 is an eight level priority interrupt control unit designed to simplify interrupt driven microcomputer systems.

The PICU can accept eight requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue an interrupt to the system along with vector information to identify the service routine.

The 8214 is fully expandable by the use of open collector interrupt output and vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt driven microcomputer systems.

PIN CONFIGURATION

LOGIC DIAGRAM

PIN NAMES

INPUTS	
$\overline{R_0}\text{-}\overline{R_7}$	REQUEST LEVELS (R₇ HIGHEST PRIORITY)
$\overline{B_0}\text{-}\overline{B_2}$	CURRENT STATUS
$\overline{SGS}$	STATUS GROUP SELECT
$\overline{ECS}$	ENABLE CURRENT STATUS
INTE	INTERRUPT ENABLE
$\overline{CLK}$	CLOCK (INT F-F)
$\overline{ELR}$	ENABLE LEVEL READ
ETLG	ENABLE THIS LEVEL GROUP
OUTPUTS:	
$\overline{A_0}\text{-}\overline{A_2}$	REQUEST LEVELS ⎤ OPEN
$\overline{INT}$	INTERRUPT (ACT. LOW) ⎦ COLLECTOR
ENLG	ENABLE NEXT LEVEL GROUP

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . 0°C to 70°C
Storage Temperature . . . . -65°C to +150°C
All Output and Supply Voltages . . . . -0.5V to +7V
All Input Voltages . . . . -1.0V to +5.5V
Output Currents . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$.

Symbol	Parameter		Min.	Typ.[1]	Max.	Unit	Conditions
V_C	Input Clamp Voltage (all inputs)				-1.0	V	I_C=-5mA
I_F	Input Forward Current:	ETLG input		-.15	-0.5	mA	V_F=0.45V
		all other inputs		-.08	-0.25	mA	
I_R	Input Reverse Current:	ETLG input			80	μA	V_R=5.25V
		all other inputs			40	μA	
V_{IL}	Input LOW Voltage:	all inputs			0.8	V	V_{CC}=5.0V
V_{IH}	Input HIGH Voltage:	all inputs	2.0			V	V_{CC}=5.0V
I_{CC}	Power Supply Current			90	130	mA	See Note 2.
V_{OL}	Output LOW Voltage:	all outputs		.3	.45	V	I_{OL}=15mA
V_{OH}	Output HIGH Voltage:	ENLG output	2.4	3.0		V	I_{OH}=-1mA
I_{OS}	Short Circuit Output Current: ENLG output		-20	-35	-55	mA	V_{OS}=0V, V_{CC}=5.0V
I_{CEX}	Output Leakage Current: $\overline{INT}$ and $\overline{A_0}$-$\overline{A_2}$				100	μA	V_{CEX}=5.25V

NOTES:
1. Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.
2. B_0-B_2, $\overline{SGS}$, CLK, $\overline{R_0}$-$\overline{R_4}$ grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit
t_{CY}	$\overline{CLK}$ Cycle Time	80	50		ns
t_{PW}	$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	25	15		ns
t_{ISS}	INTE Setup Time to $\overline{CLK}$	16	12		ns
t_{ISH}	INTE Hold Time after $\overline{CLK}$	20	10		ns
t_{ETCS}[2]	ETLG Setup Time to $\overline{CLK}$	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After $\overline{CLK}$	20	10		ns
t_{ECCS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	80	50		ns
t_{ECCH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECRS}[3]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	110	70		ns
t_{ECRH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECSS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	75	70		ns
t_{ECSH}[2]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{DCS}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{CLK}$	70	50		ns
t_{DCH}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{CLK}$	0			ns
t_{RCS}[3]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{CLK}$	90	55		ns
t_{RCH}[3]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{CLK}$	0			ns
t_{ICS}	$\overline{INT}$ Setup Time to $\overline{CLK}$	55	35		ns
t_{CI}	$\overline{CLK}$ to $\overline{INT}$ Propagation Delay		15	25	ns
t_{RIS}[4]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{INT}$	10	0		ns
t_{RIH}[4]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{INT}$	35	20		ns
t_{RA}	$\overline{R_0}$-$\overline{R_7}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		80	100	ns
t_{ELA}	$\overline{ELR}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		40	55	ns
t_{ECA}	$\overline{ECS}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		100	120	ns
t_{ETA}	ETLG to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		35	70	ns
t_{DECS}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{ECS}$	15	10		ns
t_{DECH}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{ECS}$	15	10		ns
t_{REN}	$\overline{R_0}$-$\overline{R_7}$ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	25	ns
t_{ECRN}	$\overline{ECS}$ to ENLG Propagation Delay		85	90	ns
t_{ECSN}	$\overline{ECS}$ to ENLG Propagation Delay		35	55	ns

CAPACITANCE[5]

Symbol	Parameter	Min.	Typ.[1]	Max	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		7	12	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5V$, $T_A = 25°C$, f = 1 MHz

NOTE 5. This parameter is periodically sampled and not 100% tested.

WAVEFORMS
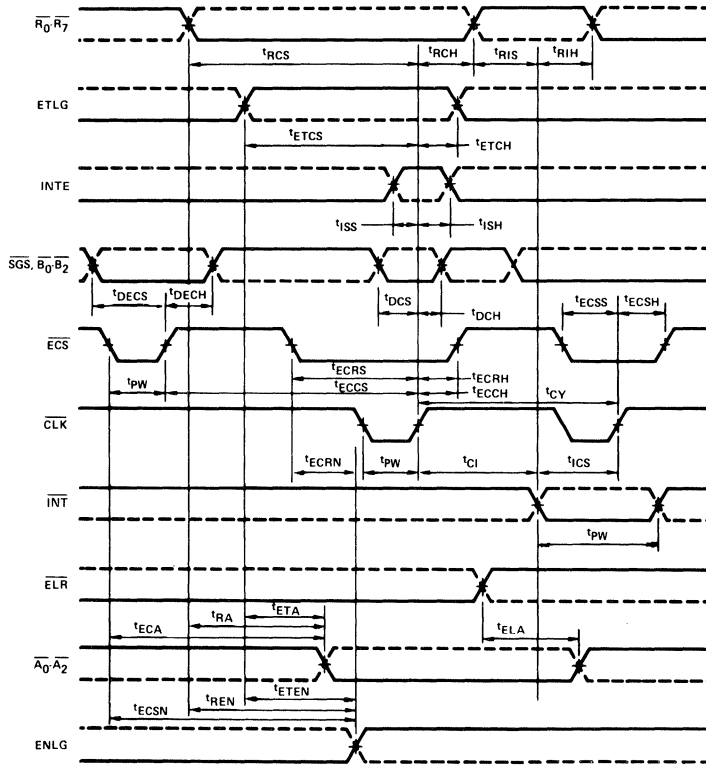
NOTES:

(1) Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.

(2) Required for proper operation if ISE is enabled during next clock pulse.

(3) These times are not required for proper operation but for desired change in interrupt flip-flop.

(4) Required for new request or status to be properly loaded.

TEST CONDITIONS:

Input pulse amplitude: 2.5 volts.

Input rise and fall times: 5 ns between 1 and 2 volts.

Output loading of 15 mA and 30 pf.

Speed measurements taken at the 1.5V levels.

TEST LOAD CIRCUIT

intel®
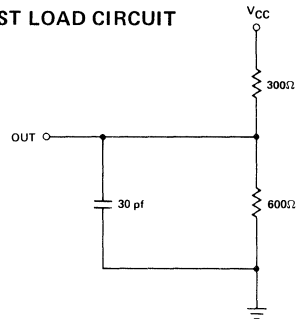
M8214
PRIORITY INTERRUPT CONTROL UNIT

- Eight Priority Levels
- Fully Expandable
- Current Status Register
- Priority Comparator

- 24-Pin Dual In-Line Package
- Full Military Temperature Range -55°C To +125°C
- ±10% Power Supply Tolerance

The M8214 is an eight level priority interrupt control unit designed to simplify interrupt driven micro-computer systems.

The PICU can accept eight requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue an interrupt to the system along with vector informa-tion to identify the service routine.

The M8214 is fully expandable by the use of open collector interrupt output and vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt driven microcomputer systems.

PIN CONFIGURATION

LOGIC DIAGRAM

PIN NAMES

INPUTS	
$\overline{R_0}$-$\overline{R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS
$\overline{SGS}$	STATUS GROUP SELECT
$\overline{ECS}$	ENABLE CURRENT STATUS
INTE	INTERRUPT ENABLE
$\overline{CLK}$	CLOCK (INT F-F)
$\overline{ELR}$	ENABLE LEVEL READ
ETLG	ENABLE THIS LEVEL GROUP
OUTPUTS:	
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS ⎫ OPEN
$\overline{INT}$	INTERRUPT (ACT. LOW) ⎰ COLLECTOR
ENLG	ENABLE NEXT LEVEL GROUP

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . −55°C to +125°C
Storage Temperature . . . . −65°C to +160°C
All Output and Supply Voltages . . . . −0.5V to +7V
All Input Voltages . . . . −1.0V to +5.5V
Output Currents . . . . 100 mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

T_A = 55°C to 125°C V_{CC} = 5V ±10%

Symbol	Parameter		Limits			Unit	Conditions
			Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage (all inputs)				-1.2	V	I_C=-5mA
I_F	Input Forward Current:	ETLG input		−.15	-0.5	mA	V_F=0.45V
		all other inputs		−.08	-0.25	mA	
I_R	Input Reverse Current:	ETLG input			80	μA	V_R=5.5V
		all other inputs			40	μA	
V_{IL}	Input LOW Voltage:	all inputs			0.8	V	V_{CC}=5.0V
V_{IH}	Input HIGH Voltage:	all inputs	2.0			V	V_{CC}=5.0V
I_{CC}	Power Supply Current			90	130	mA	See Note 2.
V_{OL}	Output LOW Voltage:	all outputs		.3	.45	V	I_{OL}=10mA
V_{OH}	Output HIGH Voltage:	ENLG output	2.4	3.0		V	I_{OH}=−1mA
I_{OS}	Short Circuit Output Current: ENLG output		-15	-35	-55	mA	V_{CC}=5.0V
I_{CEX}	Output Leakage Current: $\overline{INT}$, $\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$				100	μA	V_{CEX}=5.5V

NOTES:
1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.
2. B_0-B_2, $\overline{SGS}$, CLK, $\overline{R_0}$-$\overline{R_4}$ grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS T_A = –55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit
t_{CY}	$\overline{CLK}$ Cycle Time	85			ns
t_{PW}	$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	25	15		ns
t_{ISS}	INTE Setup Time to $\overline{CLK}$	16	12		ns
t_{ISH}	INTE Hold Time after $\overline{CLK}$	20	10		ns
t_{ETCS}[2]	ETLG Setup Time to $\overline{CLK}$	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After $\overline{CLK}$	20	10		ns
t_{ECCS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	85	25		ns
t_{ECCH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECRS}[3]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	110	70		ns
t_{ECRH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECSS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	85	70		ns
t_{ECSH}[2]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{DCS}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{CLK}$	90	50		ns
t_{DCH}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{CLK}$	0			ns
t_{RCS}[3]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{CLK}$	100	55		ns
t_{RCH}[3]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{CLK}$	0			ns
t_{ICS}	$\overline{INT}$ Setup Time to $\overline{CLK}$	55	35		ns
t_{CI}	$\overline{CLK}$ to $\overline{INT}$ Propagation Delay		15	30	ns
t_{RIS}[4]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{INT}$	10	0		ns
t_{RIH}[4]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{INT}$	35	20		ns
t_{RA}	$\overline{R_0}$-$\overline{R_7}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		80	100	ns
t_{ELA}	$\overline{ELR}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		40	55	ns
t_{ECA}	$\overline{ECS}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		100	130	ns
t_{ETA}	ETLG to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		35	70	ns
t_{DECS}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{ECS}$	20	10		ns
t_{DECH}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{ECS}$	20	10		ns
t_{REN}	$\overline{R_0}$-$\overline{R_7}$ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	30	ns
t_{ECRN}	$\overline{ECS}$ to ENLG Propagation Delay		85	110	ns
t_{ECSN}	$\overline{ECS}$ to ENLG Propagation Delay		35	55	ns

WAVEFORMS (See 8214 Waveforms, page 10-131)

CAPACITANCE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		7	12	pF

TEST CONDITIONS: V_{BIAS} = 2.5V, V_{CC} = 5V, T_A = 25°C, f = 1 MHz

intel®

8216/8226
4-BIT PARALLEL BI-DIRECTIONAL BUS DRIVER

- **Data Bus Buffer Driver for 8080 CPU**
- **Low Input Load Current — .25 mA Maximum**
- **High Output Drive Capability for Driving System Data Bus**

- **3.65V Output High Voltage for Direct Interface to 8080 CPU**
- **Three State Outputs**
- **Reduces System Package Count**

The 8216/8226 is a 4-bit bi-directional bus driver/receiver.

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50mA I_{OL} capability.

A non-inverting (8216) and an inverting (8226) are available to meet a wide variety of applications for buffering in microcomputer systems.

PIN CONFIGURATION

$\overline{CS}$	1	16	V_{CC}
DO_0	2	15	$\overline{DIEN}$
DB_0	3	14	DO_3
DI_0	4	13	DB_3
DO_1	5	12	DI_3
DB_1	6	11	DO_2
DI_1	7	10	DB_2
GND	8	9	DI_2

8216/8226
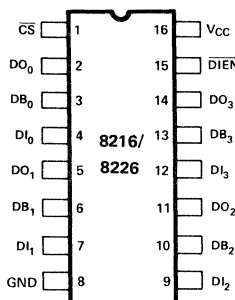
PIN NAMES

DB_0-DB_3	DATA BUS BI-DIRECTIONAL
DI_0-DI_3	DATA INPUT
DO_0-DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT
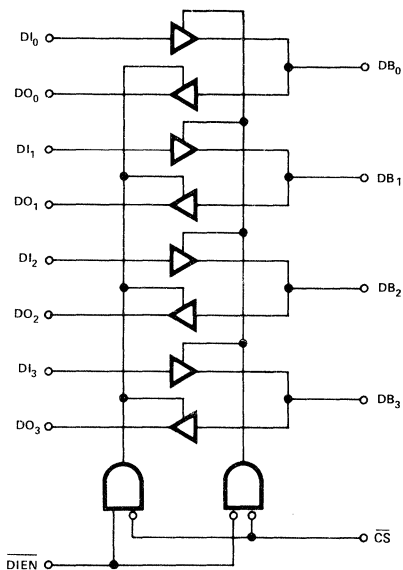
LOGIC DIAGRAM 8216

LOGIC DIAGRAM 8226
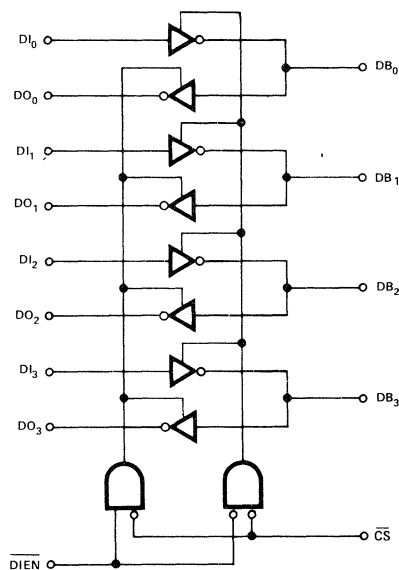
FUNCTIONAL DESCRIPTION

Microprocessors like the 8080 are MOS devices and are generally capable of driving a single TTL load. The same is true for MOS memory devices. While this type of drive is sufficient in small systems with few components, quite often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The 8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bi-Directional Driver

Each buffered line of the four bit driver consists of two separate buffers that are tri-state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is direct TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080 Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080 and 8008 CPUs is achieved with an adequate amount of noise immunity (350mV worst case).

Control Gating $\overline{\text{DIEN}}$, $\overline{\text{CS}}$

The $\overline{\text{CS}}$ input is actually a device select. When it is "high" the output drivers are all forced to their high-impedance state. When it is at "zero" the device is selected (enabled) and the direction of the data flow is determined by the $\overline{\text{DIEN}}$ input.

The $\overline{\text{DIEN}}$ input controls the direction of data flow (see Figure 1) for complete truth table. This direction control is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

The 8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.
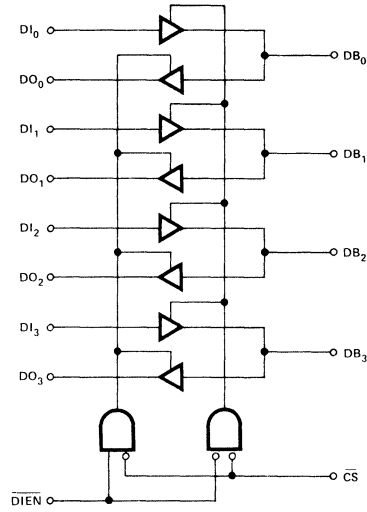
(a) 8216
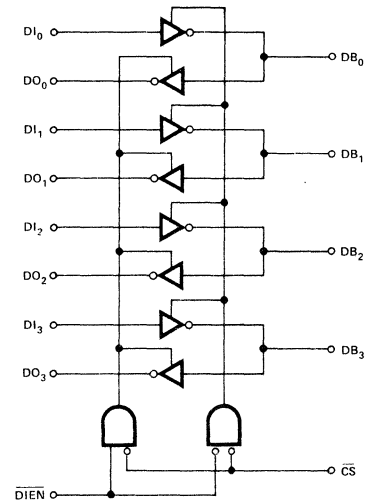
(b) 8226

DIEN	CS	
0	0	DI → DB
1	0	DB → DO
0	1	⎤ HIGH IMPEDANCE
1	1	⎦

Figure 1. 8216/8226 Logic Diagrams

APPLICATIONS OF 8216/8226

8080 Data Bus Buffer

The 8080 CPU Data Bus is capable of driving a single TTL load and is more than adequate for small, single board systems. When expanding such a system to more than one board to increase I/O or Memory size, it is necessary to provide a buffer. The 8216/8226 is a device that is exactly fitted to this application.

Shown in Figure 2 are a pair of 8216/8226 connected directly to the 8080 Data Bus and associated control signals. The buffer is bi-directional in nature and serves to isolate the CPU data bus.

On the system side, the DB lines interface with standard semiconductor I/O and Memory components and are completely TTL compatible. The DB lines also provide a high drive capability (50mA) so that an extremely large system can be dirven along with possible bus termination networks.

On the 8080 side the DI and DO lines are tied together and are directly connected to the 8080 Data Bus for bi-directional operation. The DO outputs of the 8216/8226 have a high voltage output capability of 3.65 volts which allows direct connection to the 8080 whose minimum input voltage is 3.3 volts. It also gives a very adequate noise margin of 350mV (worst case).

The $\overline{\text{DIEN}}$ inputs to 8216/8226 is connected directly to the 8080. $\overline{\text{DIEN}}$ is tied to DBIN so that proper bus flow is maintained, and $\overline{\text{CS}}$ is tied to $\overline{\text{BUSEN}}$ so that the system side Data Bus will be 3-stated when a Hold request has been acknowledged during a DMA activity.

Memory and I/O Interface to a Bi-directional Bus

In large microcomputer systems it is often necessary to provide Memory and I/O with their own buffers and at the same time maintain a direct, common interface to a bi-directional Data Bus. The 8216/8226 has separated data in and data out lines on one side and a common bi-directional set on the other to accomodate such a function.

Shown in Figure 3 is an example of how the 8216/8226 is used in this type of application.

The interface to Memory is simple and direct. The memories used are typically Intel® 8102, 8102A, 8101 or 8107B-4 and have separate data inputs and outputs. The DI and DO lines of the 8216/8226 tie to them directly and under control of the $\overline{\text{MEMR}}$ signal, which is connected to the $\overline{\text{DIEN}}$ input, an interface to the bi-directional Data Bus is maintained.

The interface to I/O is similar to Memory. The I/O devices used are typically Intel® 8255s, and can be used for both input and output ports. The $\overline{\text{I/O R}}$ signal is connected directly to the $\overline{\text{DIEN}}$ input so that proper data flow from the I/O device to the Data Bus is maintained.

The 8216/8226 can be used in a wide variety of other buffering functions in microcomputer systems such as Address Bus Drivers, Drivers to peripheral devices such as printers, and as Drivers for long length cables to other peripherals or systems.
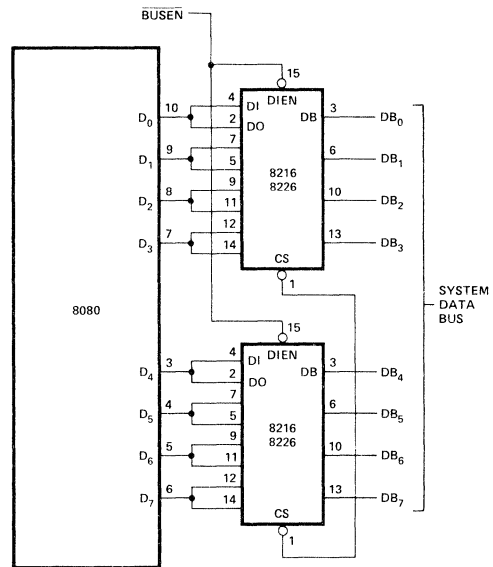
Figure 2. 8080 Data Bus Buffer.
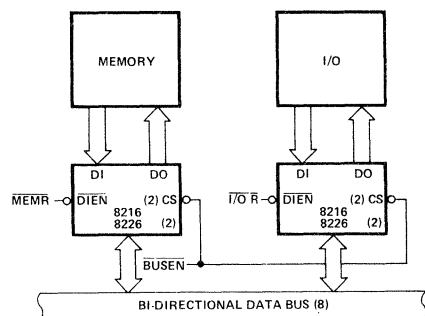
Figure 3. Memory and I/O Interface to a Bi-Directional Bus.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . 0°C to 70°C
Storage Temperature . . . . –65°C to +150°C
All Output and Supply Voltages . . . . –0.5V to +7V
All Input Voltages . . . . –1.0V to +5.5V
Output Currents . . . . 125 mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

T_A = 0°C to +70°C, V_{CC}=+5V ±5%

Symbol	Parameter		Limits			Unit	Conditions
			Min.	Typ.	Max.		
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$			–0.15	–.5	mA	V_F = 0.45
I_{F2}	Input Load Current All Other Inputs			–0.08	–.25	mA	V_F = 0.45
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$				20	μA	V_R = 5.25V
I_{R2}	Input Leakage Current DI Inputs				10	μA	V_R = 5.25V
V_C	Input Forward Voltage Clamp				–1	V	I_C = –5mA
V_{IL}	Input "Low" Voltage				.95	V	
V_{IH}	Input "High" Voltage		2.0			V	
$|I_O|$	Output Leakage Current (3-State)	DO DB			20 100	μA	V_O = 0.45V/5.25V
I_{CC}	Power Supply Current	8216		95	130	mA	
		8226		85	120	mA	
V_{OL1}	Output "Low" Voltage			0.3	.45	V	DO Outputs I_{OL}=15mA DB Outputs I_{OL}=25mA
V_{OL2}	Output "Low" Voltage	8216		0.5	.6	V	DB Outputs I_{OL}=55mA
		8226		0.5	.6	V	DB Outputs I_{OL}=50mA
V_{OH1}	Output "High" Voltage		3.65	4.0		V	DO Outputs I_{OH} = –1mA
V_{OH2}	Output "High" Voltage		2.4	3.0		V	DB Outputs I_{OH} = –10mA
I_{OS}	Output Short Circuit Current		–15 –30	–35 –75	–65 –120	mA mA	DO Outputs $V_O \cong$ 0V, DB Outputs V_{CC}=5.0V

NOTE: Typical values are for T_A = 25°C, V_{CC} = 5.0V.

WAVEFORMS
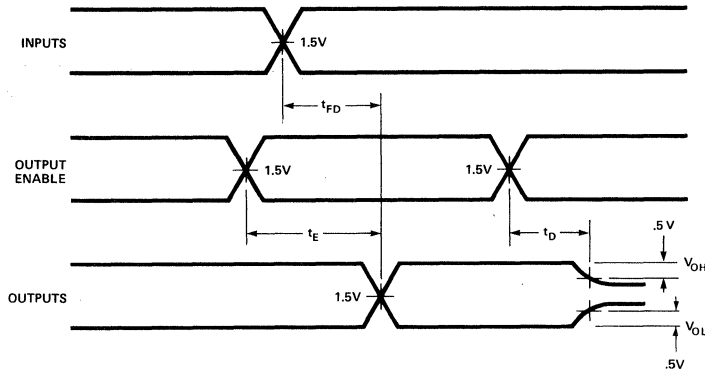
A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	$C_L=30pF$, $R_1=300\Omega$ $R_2=600\Omega$
T_{PD2}	Input to Output Delay DB Outputs					$C_L=300pF$, $R_1=90\Omega$ $R_2 = 180\Omega$
	8216		20	30	ns	
	8226		16	25	ns	
T_E	Output Enable Time					
	8216		45	65	ns	(Note 2)
	8226		35	54	ns	(Note 3)
T_D	Output Disable Time		20	35	ns	(Note 4)

TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT
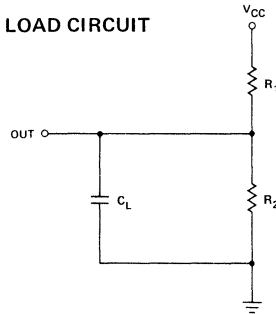
CAPACITANCE [5]

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
C_{IN}	Input Capacitance		4	8	pF
C_{OUT1}	Output Capacitance		6	10	pF
C_{OUT2}	Output Capacitance		13	18	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, $f = 1$ MHz.

NOTES:
1. Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.
2. DO Outputs, $C_L = 30pF$, $R_1 = 300/10$ KΩ, $R_2 = 180/1$KΩ; DB Outputs, $C_L = 300pF$, $R_1 = 90/10$ KΩ, $R_2 = 180/1$ KΩ.
3. DO Outputs, $C_L = 30pF$, $R_1 = 300/10$ KΩ, $R_2 = 600/1$K; DB Outputs, $C_L = 300pF$, $R_1 = 90/10$ KΩ, $R_2 = 180/1$ KΩ.
4. DO Outputs, $C_L = 5pF$, $R_1 = 300/10$KΩ, $R_2 = 600/1$ KΩ; DB Outputs, $C_L = 5pF$, $R_1 = 90/10$ KΩ, $R_2 = 180/1$ KΩ.
5. This parameter is periodically sampled and not 100% tested.

intel®

M8216
4-BIT PARALLEL BI-DIRECTIONAL BUS DRIVER

- ■ **Data Bus Buffer Driver for 8080 CPU**
- ■ **Low Input Load Current: .25 mA Maximum**
- ■ **High Output Drive Capability for Driving System Data Bus**
- ■ **16-Pin Dual In-Line Package**

- ■ **3.40V Output High Voltage for Direct Interface to 8080 CPU**
- ■ **Three-State Outputs**
- ■ **Full Military Temperature Range -55°C To +125°C**
- ■ **±10% Power Supply Tolerance**

The M8216 is a 4-bit bi-directional bus driver/receiver.

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.40V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50mA I_{OL} capability.

The M8216 is used to meet a wide variety of applications for buffering in microcomputer systems.

PIN CONFIGURATION

$\overline{CS}$	1		16	V_{CC}
DO_0	2		15	$\overline{DIEN}$
DB_0	3		14	DO_3
DI_0	4	M8216	13	DB_3
DO_1	5		12	DI_3
DB_1	6		11	DO_2
DI_1	7		10	DB_2
GND	8		9	DI_2
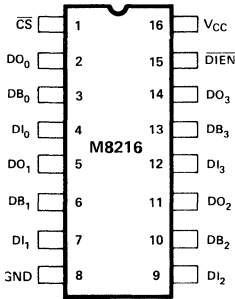
PIN NAMES

DB_0-DB_3	DATA BUS BI-DIRECTIONAL
DI_0-DI_3	DATA INPUT
DO_0-DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT

LOGIC DIAGRAM
8216

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . −55°C to +125°C

Storage Temperature . . . . −65°C to +150°C

All Output and Supply Voltages . . . . −0.5V to +7V

All Input Voltages . . . . −1.0V to +5.5V

Output Currents . . . . 125 mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

T_A = −55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter		Limits			Unit	Conditions
			Min.	Typ.	Max.		
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$			−0.15	−.5	mA	V_F = 0.45
I_{F2}	Input Load Current All Other Inputs			−0.08	−.25	mA	V_F = 0.45
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$				20	μA	V_R = 5.5V
I_{R2}	Input Leakage Current DI Inputs				10	μA	V_R = 5.5V
V_C	Input Forward Voltage Clamp				−1.2	V	I_C = −5mA
V_{IL}	Input "Low" Voltage				.95	V	V_{CC} = 5V
V_{IH}	Input "High" Voltage		2.0			V	V_{CC} = 5V
$|I_O|$	Output Leakage Current DO (3-State) DB				20 100	μA	V_O = .45V to V_{CC}
I_{CC}	Power Supply Current			95	130	mA	
V_{OL1}	Output "Low" Voltage			0.3	.45	V	DO Outputs I_{OL}=15mA DB Outputs I_{OL}=25mA
V_{OL2}	Output "Low" Voltage			0.5	.6	V	DB Outputs I_{OL}=50mA
V_{OH1}	Output "High" Voltage		3.4	3.8		V	DO Outputs I_{OH} = −.5mA
V_{OH2}	Output "High" Voltage		2.4	3.0		V	DO Outputs I_{OH} = −2mA DB Outputs I_{OH} = −5.0mA
I_{OS}	Output Short Circuit Current		−15 −30	−35 −75	−65 −120	mA mA	DO Outputs V_{CC} = 5.0V DB Outputs V_{CC} = 5.0V
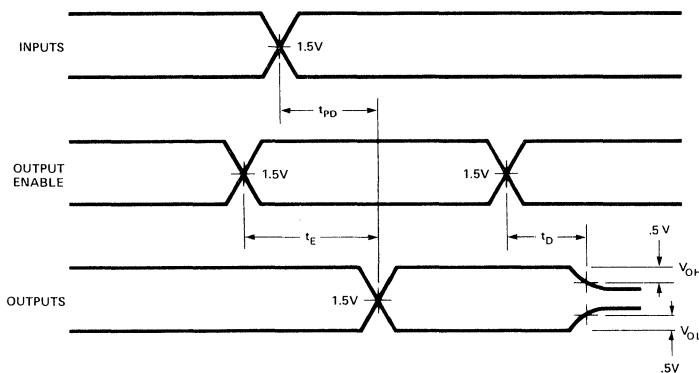
NOTE: Typical values are for T_A = 25°C, V_{CC} = 5.0V.

WAVEFORMS

A.C. CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	(NOTE 2)
T_{PD2}	Input to Output Delay DB Outputs		20	33	ns	(NOTE 2)
T_E	Output Enable Time		45	75	ns	(NOTE 2)
T_D	Output Disable Time		20	40	ns	(NOTE 2)

TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.

TEST LOAD CIRCUIT
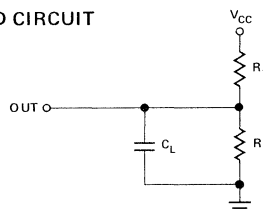
CAPACITANCE

Symbol	Parameter		Limits			Unit
			Min.	Typ.[1]	Max.	
C_{IN}	Input Capacitance			4	6	pF
C_{OUT1}	Output Capacitance	DO Outputs		6	10	pF
C_{OUT2}	Output Capacitance	DB Outputs		13	18	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, $f = 1$ MHz.

NOTES: 1. Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.
2.

TEST	C_L	R_1	R_2
T_{PD1}	30pF	300Ω	600Ω
T_{PD2}	300pF	90Ω	180Ω
T_E, (DO, ENABLE↑)	30pF	10KΩ	1KΩ
T_E, (DO, ENABLE↓)	30pF	300Ω	600Ω
T_E, (DB, ENABLE↑)	300pF	10KΩ	1KΩ
T_E, (DB, ENABLE↓)	300pF	90Ω	180Ω
T_D, (DO, DISABLE↑)	5pF	300Ω	600Ω
T_D, (DO, DISABLE↓)	5pF	10KΩ	1KΩ
T_D, (DB, DISABLE↑)	5pF	90Ω	180Ω
T_D, (DB, DISABLE↓)	5pF	10KΩ	1KΩ

intel®

8251A
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
  - **Synchronous:**
    5-8 Bit Characters
    Internal or External Character
    Synchronization
    Automatic Sync Insertion
  - **Asynchronous:**
    5-8 Bit Characters
    Clock Rate — 1, 16 or 64 Times
    Baud Rate
    Break Character Generation
    1, 1½, or 2 Stop Bits
    False Start Bit Detection
    Automatic Break Detect
    and Handling

- **Baud Rate —DC to 64k Baud**
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080/8085 CPU**
- **28-Pin DIP Package**
- **All Inputs and Outputs Are TTL Compatible**
- **Single 5 Volt Supply**
- **Single TTL Clock**

The 8251A is the enhanced version of the industry standard, Intel® 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's new high performance family of microprocessors such as the 8085. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is constructed using N-channel silicon gate technology.
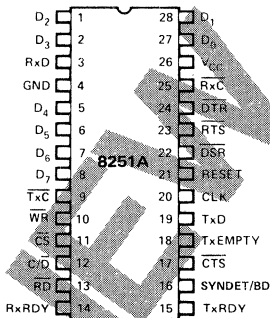
PIN CONFIGURATION

BLOCK DIAGRAM
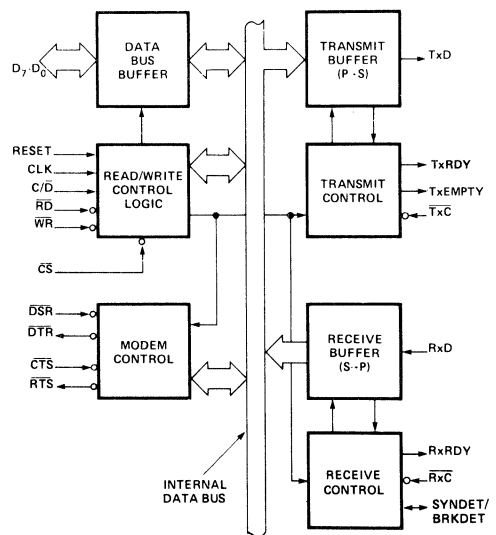
Pin Name	Pin Function
D$_7$-D$_0$	Data Bus (8 bits)
C/$\overline{D}$	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Select
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for CPU)
TxRDY	Transmitter Ready (ready for char. from CPU)

Pin Name	Pin Function
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET/BD	Sync Detect/ Break Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxEMPTY	Transmitter Empty
V$_{CC}$	+5 Volt Supply
GND	Ground

PRELIMINARY

8251A BASIC FUNCTIONAL DESCRIPTION

General

The 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 80/85 Microcomputer Systems. Like other I/O devices in a Microcomputer System, its functional configuration is programmed by the system's software for maximum flexibility. The 8251A can support virtually any serial data technique currently in use (including IBM "bi-sync").

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer. The command status and data in, and data out are separate 8-bit registers to provide double buffering.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

RESET (Reset)

A "high" on this input forces the 8251A into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6 t_{CY} (clock must be running).

CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the 8224 Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

$\overline{WR}$ (Write)

A "low" on this input informs the 8251A that the CPU is writing data or control words to the 8251A.

$\overline{RD}$ (Read)

A "low" on this input informs the 8251A that the CPU is reading data or status information from the 8251A.

C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the 8251A that the word on the Data Bus is either a data character, control word or status information.
1 = CONTROL/STATUS   0 = DATA

$\overline{CS}$ (Chip Select)

A "low" on this input selects the 8251A. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.
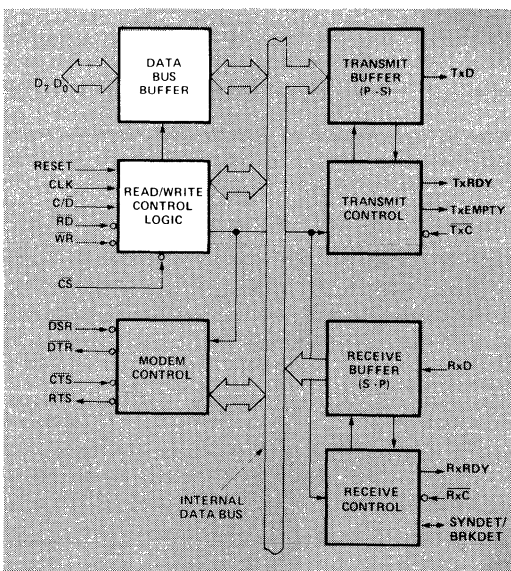
C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251A DATA ⇒ DATA BUS
0	1	0	0	DATA BUS ⇒ 8251A DATA
1	0	1	0	STATUS ⇒ DATA BUS
1	1	0	0	DATA BUS ⇒ CONTROL
X	1	1	0	DATA BUS ⇒ 3-STATE
X	X	X	1	DATA BUS ⇒ 3-STATE

Modem Control

The 8251A has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The Modem control signals are general purpose in nature and can be used for functions other than Modem control, if necessary.

PRELIMINARY

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is a general purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test Modem conditions such as Data Set Ready.

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for Modem control such as Data Terminal Ready or Rate Select.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for Modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send)

A "low" on this input enables the 8251A to transmit serial data if the Tx Enable bit in the Command byte is set to a "one." If either a Tx Enable off or CTS off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx Disable command before shutting down.

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of $\overline{TxC}$. The transmitter will begin transmission upon being enabled if $\overline{CTS}$ = 0. The TxD line will be held in the marking state immediately upon a master Reset or when Tx Enable/ $\overline{CTS}$ off or TxEMPTY.

Transmitter Control

The transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by Tx Disabled, or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the CPU.

Note that when using the Polled operation, the TxRDY status bit is *not* masked by Tx Enabled, but will only indicate the Empty/Full Status of the Tx Data Input Register.

TxE (Transmitter Empty)

When the 8251A has no characters to transmit, the TxEMPTY output will go "high". It resets automatically upon receiving a character from the CPU. TxEMPTY can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode. TxEMPTY is independent of the Tx Enable bit in the Command instruction.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being transmitted automatically as "fillers". TxEMPTY does not go low when the SYNC characters are being shifted out.
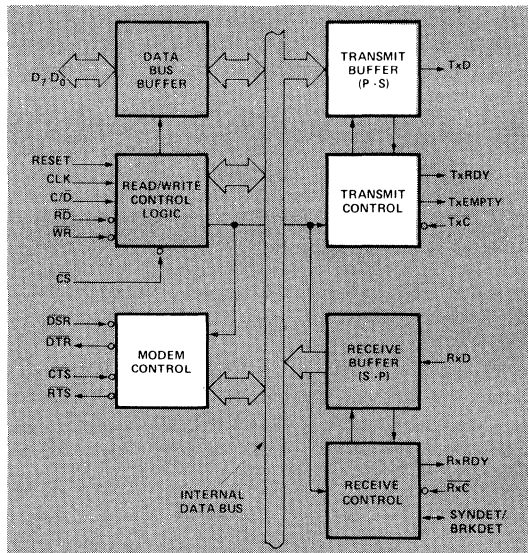
$\overline{TxC}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous transmission mode the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{TxC}$.

For Example:

    If Baud Rate equals 110 Baud,
    $\overline{TxC}$ equals 110 Hz (1x)
    $\overline{TxC}$ equals 1.76 kHz (16x)
    $\overline{TxC}$ equals 7.04 kHz (64x). ·

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251A.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to RxD pin, and is clocked in on the rising edge of $\overline{RxC}$.

Receiver Control

This functional block manages all receiver-related activities which consist of the following features:

The RxD initialization circuit prevents the 8251A from mistaking an unused input line for an active low data line in the "break condition". Before starting to receive serial characters on the RxD line, a valid "1" must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (Start bit) is enabled. This feature is only active in the asynchronous mode, and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts due to a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

The Parity Toggle F/F and Parity Error F/F circuits are used for parity error detection and set the corresponding status bit.

The Framing Error Flag F/F is set if the Stop bit is absent at the end of the data byte (asynchronous mode), and also sets the corresponding status bit.

RxRDY (Receiver Ready)

This output indicates that the 8251A contains a character that is ready to be input to the CPU. Rx RDY can be connected to the interrupt structure of the CPU or, for Polled operation, the CPU can check the condition of RxRDY using a Status Read operation.

Rx Enable off both masks and holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be Enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, overrun error will be set and the old character will be lost.

$\overline{RxC}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor; 1, 1/16 or 1/64 the $\overline{RxC}$.

For Example:

Baud Rate equals 300 Baud, if
$\overline{RxC}$ equals 300 Hz (1x)
$\overline{RxC}$ equals 4800 Hz (16x)
$\overline{RxC}$ equals 19.2 kHz (64x).

Baud Rate equals 2400 Baud, if
$\overline{RxC}$ equals 2400 Hz (1x)
$\overline{RxC}$ equals 38.4 kHz (16x)
$\overline{RxC}$ equals 153.6 kHz (64x).

Data is sampled into the 8251A on the rising edge of $\overline{RxC}$.

NOTE: In most communications systems, the 8251A will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect)/BRKDET (Break Detect)

This pin is used in SYNChronous Mode for SYNDET and may be used as either input or output, programmable through the Control Word. It is reset to output mode low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251A has located the SYNC character in the Receive mode. If the 8251A is programmed to use double Sync characters (bi-sync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.
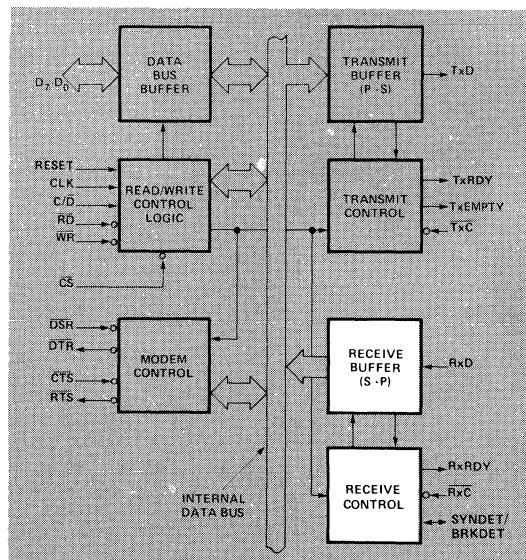
When used as an input (external SYNC detect mode), a positive going signal will cause the 8251A to start assembling data characters on the rising edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. the period of $\overline{RxC}$. When External SYNC Detect is programmed, the Internal SYNC Detect is disabled.

Break Detect (Async Mode Only)

This output will go high whenever an all zero word of the programmed length (including start bit, data bit, parity bit, and *one* stop bit) is received. Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.
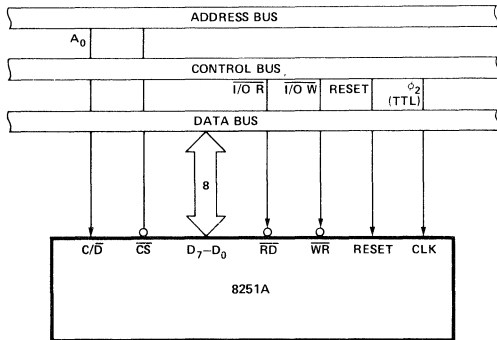
8251A Interface to 8080 Standard System Bus

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251A is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the 8251A to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD/OFF PARITY, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251A is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251A is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251A. On the other hand, the 8251A receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised "high" to signal the CPU that the 8251A has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The 8251A cannot begin transmission until the Tx Enable (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon Reset.

Programming the 8251A

Prior to starting data transmission or reception, the 8251A must be loaded with a set of control words generated by the CPU. These control words define the complete functional definition of the 8251A and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

This format defines the general operational characteristics of the 8251A. It must follow a Reset operation (internal or external). Once the Mode Instruction has been written into the 8251A by the CPU, SYNC characters or Command Instructions may be inserted.

Command Instruction

This format defines a status word that is used to control the actual operation of the 8251A.

Both the Mode and Command Instructions must conform to a specified sequence for proper device operation. The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251A for data communication.

All control words written into the 8251A after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251A at any time in the data block during the operation of the 8251A. To return to the Mode Instruction format, the master Reset bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251A back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.
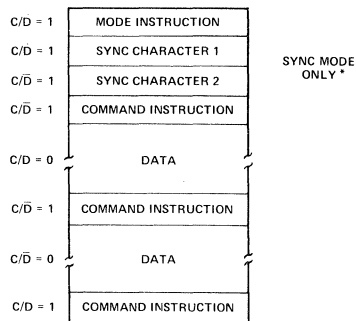
Typical Data Block

PRELIMINARY

Mode Instruction Definition

The 8251A can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251A, the designer can best view the device as two separate components sharing the same package, one Asynchronous the other Synchronous. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.

NOTE: When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant Data Bus bits will hold the data; unused bits are "don't care" when writing data to the 8251A, and will be "zeros" when reading the data from the 8251A.

Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the 8251A automatically adds a Start bit (low level) followed by the data bits (least significant bit first), and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the 8251A the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed.

Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16X or 64X mode only). If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. Note that the *receiver* requires only *one* stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the 8251A. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the 8251A.

Mode Instruction Format, Asynchronous Mode

BAUD RATE FACTOR

0	1	0	1
0	0	1	1
SYNC MODE	(1X)	(16X)	(64X)

CHARACTER LENGTH

0	1	0	1
0	0	1	1
5 BITS	6 BITS	7 BITS	8 BITS

PARITY ENABLE
1 = ENABLE   0 = DISABLE

EVEN PARITY GENERATION/CHECK
1 = EVEN   0 = ODD

NUMBER OF STOP BITS

0	1	0	1
0	0	1	1
INVALID	1 BIT	1½ BITS	2 BITS

(ONLY EFFECTS Tx; Rx NEVER REQUIRES MORE THAN ONE STOP BIT)
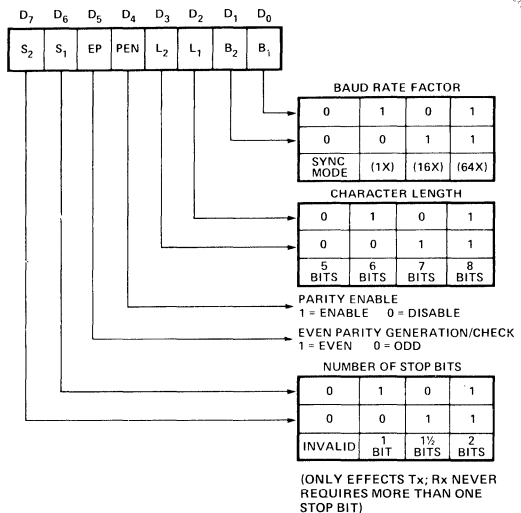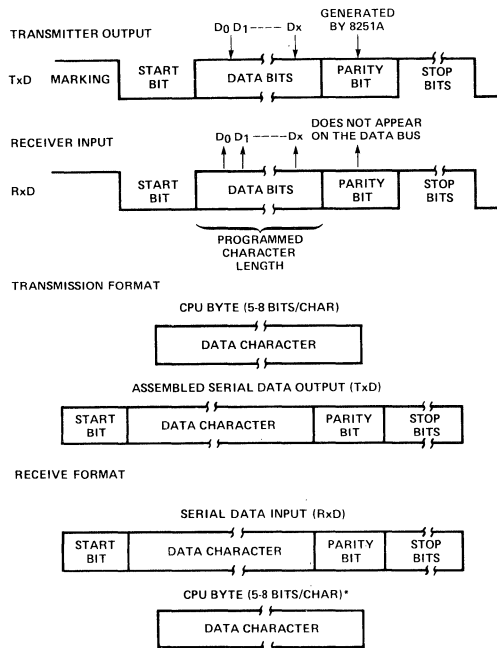
Asynchronous Mode

*NOTE: IF CHARACTER LENGTH IS DEFINED AS 5, 6 OR 7 BITS THE UNUSED BITS ARE SET TO "ZERO".

PRELIMINARY

Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the 8251A which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at the TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the 8251A with a data character before the 8251A Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the 8251A is empty and SYNC characters are being sent out. TxEMPTY does not go low when the SYNC is being shifted out (see figure below). The TxEMPTY pin is internally reset by a data character being written into the 8251A.

TxD: DATA | DATA | SYNC 1 | SYNC 2 | DATA — — — — —

AUTOMATICALLY INSERTED BY USART

TxEMPTY — FALLS UPON CPU WRITING A CHARACTER TO THE USART

NOMINAL CENTER OF LAST BIT
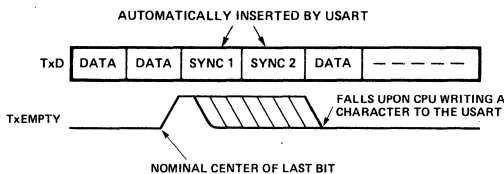
Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the SYNC mode has been programmed, ENTER HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled in on the rising edge of $\overline{RxC}$. The content of the Rx buffer is compared at every bit boundary with the first SYNC character until a match occurs. If the 8251A has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit instead of the middle of the last data bit.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the 8251A out of the HUNT mode. The high level can be removed after one $\overline{RxC}$ cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode. Parity is checked when not in Hunt, regardless of whether the Receiver is enabled or not.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost. This will also set all the used character bits in the buffer to a "one", thus preventing a possible false SYNDET caused by data that happens to be in the Rx Buffer at ENTER HUNT time. Note that the SYNDET F/F is reset at each Status Read, regardless of whether internal or external SYNC has been programmed. This does not cause the 8251A to return to the HUNT mode. When in SYNC mode, but not in HUNT, Sync Detection is still functional, but only occurs at the "known" word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character sync has been programmed, then both sync characters have been contiguously received to gate a SYNDET indication.) When external SYNDET mode is selected, internal Sync Detect is disabled, and the SYNDET F/F may be set at any bit boundary.

Mode Instruction Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SCS	ESD	EP	PEN	L_2	L_1	0	0

CHARACTER LENGTH

0	1	0	1
0	0	1	1
5 BITS	6 BITS	7 BITS	8 BITS

PARITY ENABLE
(1 = ENABLE)
(0 = DISABLE)

EVEN PARITY GENERATION/CHECK
1 = EVEN
0 = ODD

EXTERNAL SYNC DETECT
1 = SYNDET IS AN INPUT
0 = SYNDET IS AN OUTPUT

SINGLE CHARACTER SYNC
1 = SINGLE SYNC CHARACTER
0 = DOUBLE SYNC CHARACTER
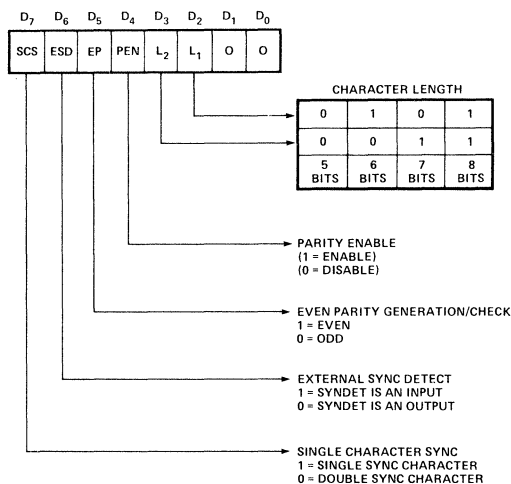
NOTE: IN EXTERNAL SYNC MODE, PROGRAMMING DOUBLE CHARACTER SYNC WILL AFFECT ONLY THE Tx.

Data Format, Synchronous Mode
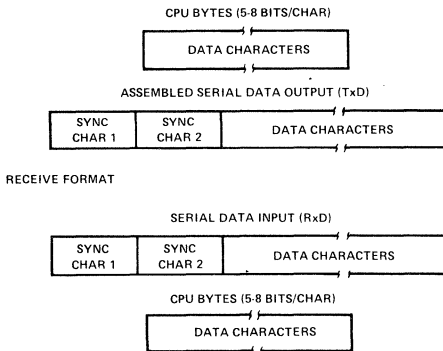
CPU BYTES (5-8 BITS/CHAR)

DATA CHARACTERS

ASSEMBLED SERIAL DATA OUTPUT (TxD)

| SYNC CHAR 1 | SYNC CHAR 2 | DATA CHARACTERS |

RECEIVE FORMAT

SERIAL DATA INPUT (RxD)

| SYNC CHAR 1 | SYNC CHAR 2 | DATA CHARACTERS |

CPU BYTES (5-8 BITS/CHAR)

DATA CHARACTERS

PRELIMINARY

COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251A has been programmed by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251A and Sync characters inserted, if necessary, then all further "control writes" (C/$\overline{D}$ = 1) will load a Command Instruction. A Reset Operation (internal or external) will return the 8251A to the Mode Instruction format.

STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251A has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. (The status update is inhibited during status read).

A normal "read" command is issued by the CPU with C/$\overline{D}$ = 1 to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251A can be used in a completely Polled environment or in an interrupt driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.

Note: Error Reset must be performed whenever RxEnable and Enter Hunt are programmed.

Command Instruction Format
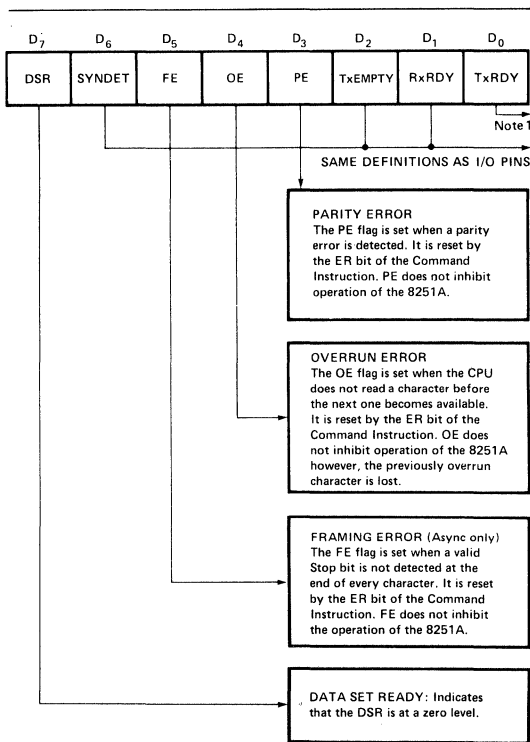
Status Read Format

Note 1: TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by $\overline{CTS}$ and TxEN; the latter is conditioned by both $\overline{CTS}$ and TxEN.
i.e. TxRDY status bit = DB Buffer Empty
TxRDY pin out = DB Buffer Empty · (CTS=0) · (TxEN=1)

PRELIMINARY

APPLICATIONS OF THE 8251A
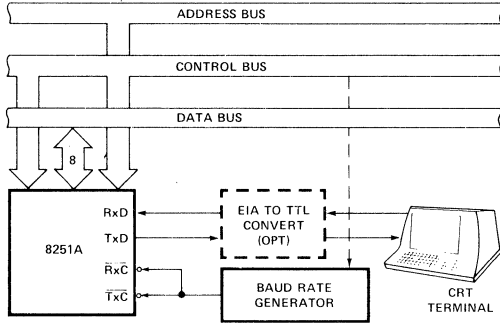
Asynchronous Serial Interface to CRT Terminal, DC-9600 Baud

Asynchronous Interface to Telephone Lines
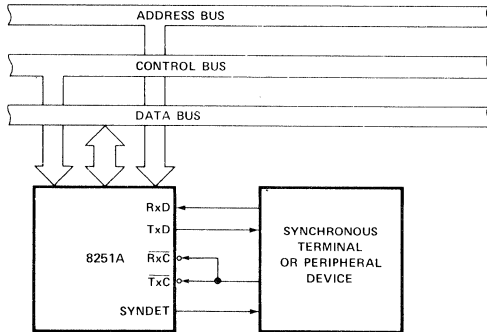
Synchronous Interface to Terminal or Peripheral Device
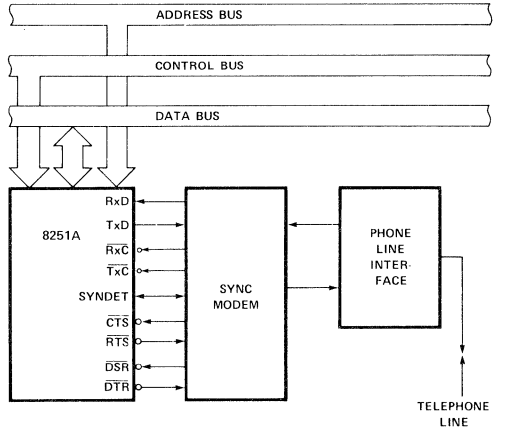
Synchronous Interface to Telephone Lines

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 0°C to 70°C
Storage Temperature . . . . −65°C to +150°C
Voltage On Any Pin
   With Respect to Ground . . . . −0.5V to +7V
Power Dissipation . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.2$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400 \mu A$
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ TO 0.45V
I_{IL}	Input Leakage		±10	μA	$V_{IN} = V_{CC}$ TO 0.45V
I_{CC}	Power Supply Current		100	mA	All Outputs = High

CAPACITANCE

$T_A = 25°C$; $V_{CC} = $ GND = 0V

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND

TEST LOAD CIRCUIT:

Figure 1.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE (dB)

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.
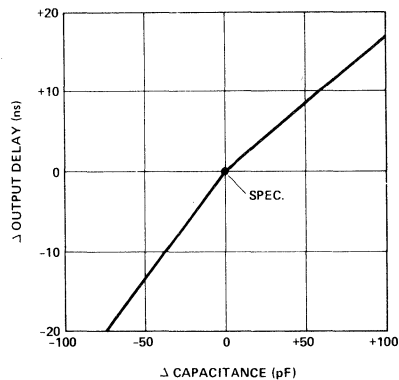
A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V

BUS PARAMETERS: (Note 1)

READ CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RR}	$\overline{READ}$ Pulse Width	250		ns	
t_{RD}	Data Delay from $\overline{READ}$		200	ns	3, C_L = 150 pF
t_{DF}	$\overline{READ}$ to Data Floating	10	100	ns	

WRITE CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AW}	Address Stable Before $\overline{WRITE}$	0		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	0		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	250		ns	
t_{DW}	Data Set Up Time for $\overline{WRITE}$	150		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	0		ns	
t_{RV}	Recovery Time Between WRITES	6		t_{CY}	Note 4

NOTES: 1. AC timings measured V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.
2. Chip Select ($\overline{CS}$) and Command/Data (C/$\overline{D}$) are considered as Addresses.
3. Assumes that Address is valid before $\overline{RD}\downarrow$.
4. This recovery time is for Mode Initialization only. Write Data is allowed only when TxRDY = 1.
   Recovery Time between Writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.

INPUT waveforms for AC tests:
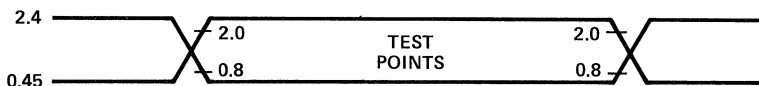
OTHER TIMINGS:

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{CY}	Clock Period	320	1.35	μs	Notes 5, 6
t_ϕ	Clock High Pulse Width	120	t_{CY-90}	ns	
$t_{\overline{\phi}}$	Clock Low Pulse Width	90		ns	
t_R, t_F	Clock Rise and Fall Time	5	20	ns	
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	μs	
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2		μs	
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2		μs	
f_{Tx}	Transmitter Input Clock Frequency				
	1x Baud Rate	DC	64	kHz	
	16x Baud Rate	DC	310	kHz	
	64x Baud Rate	DC	615	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1x Baud Rate	DC	64	kHz	
	16x Baud Rate	DC	310	kHz	
	64x Baud Rate	DC	615	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
t_{TxRDY}	TxRDY Pin Delay from Center of last Bit		8	t_{CY}	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY ↓ from Leading Edge of $\overline{WR}$		150	ns	Note 7
t_{RxRDY}	RxRDY Pin Delay from Center of last Bit		24	t_{CY}	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY ↓ from Leading Edge of $\overline{RD}$		150	ns	Note 7
t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$		24	t_{CY}	Note 7
t_{ES}	External SYNDET Set-Up Time Before Falling Edge of $\overline{RxC}$		16	t_{CY}	Note 7
$t_{TxEMPTY}$	TxEMPTY Delay from Center of Data Bit		20	t_{CY}	Note 7
t_{WC}	Control Delay from Rising Edge of WRITE (TxEn, $\overline{DTR}$, $\overline{RTS}$)		8	t_{CY}	Note 7
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		20	t_{CY}	Note 7

5. The TxC and RxC frequencies have the following limitations with respect to CLK.
    For 1x Baud Rate, f_{Tx} or $f_{Rx} \leqslant 1/(30\ t_{CY})$
    For 16x and 64x Baud Rate, f_{Tx} or $f_{Rx} \leqslant 1/(4.5\ t_{CY})$

6. Reset Pulse Width = 6 t_{CY} minimum; System Clock must be running during Reset.

7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

SYSTEM CLOCK INPUT

CLOCK ϕ

t_f t_r t_ϕ $t_{\bar\phi}$ t_{cy}

TRANSMITTER CLOCK & DATA

$\overline{TxC}$ (1x MODE)

t_{TPW} t_{TPD}

$\overline{TxC}$ (16x MODE)

Tx DATA

t_{DTX} t_{DTX}

RECEIVER CLOCK & DATA
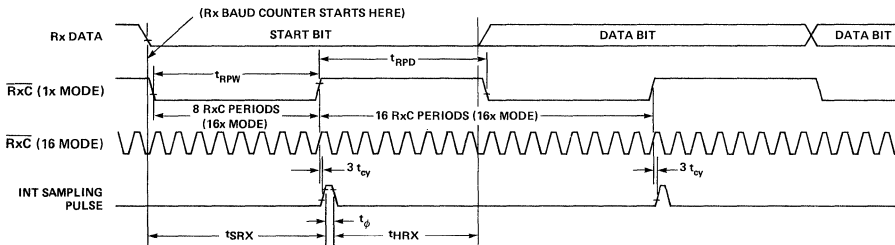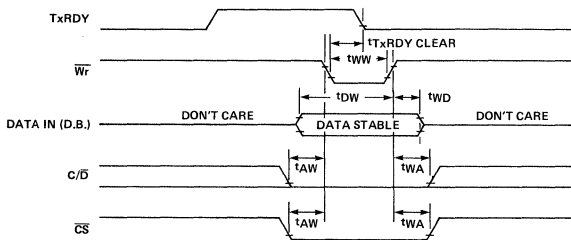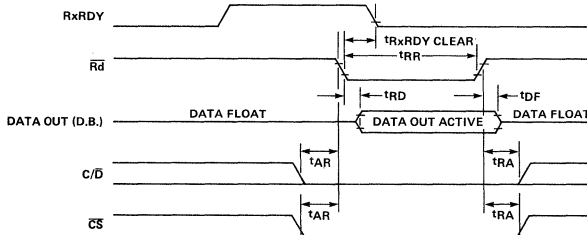
Rx DATA

(Rx BAUD COUNTER STARTS HERE)

START BIT | DATA BIT | DATA BIT

$\overline{RxC}$ (1x MODE)

t_{RPW} t_{RPD}

8 RxC PERIODS (16x MODE) | 16 RxC PERIODS (16x MODE)

$\overline{RxC}$ (16 MODE)

INT SAMPLING PULSE

$3\,t_{cy}$ $3\,t_{cy}$

t_{SRX} t_ϕ t_{HRX}

WRITE DATA CYCLE (CPU → USART)

TxRDY

t_{TxRDY} CLEAR

$\overline{Wr}$

t_{WW}

t_{DW} t_{WD}

DATA IN (D.B.)

DON'T CARE | DATA STABLE | DON'T CARE

C/$\overline{D}$

t_{AW} t_{WA}

$\overline{CS}$

t_{AW} t_{WA}

READ DATA CYCLE (CPU ← USART)

RxRDY

t_{RxRDY} CLEAR

$\overline{Rd}$

t_{RR}

t_{RD} t_{DF}

DATA OUT (D.B.)

DATA FLOAT | DATA OUT ACTIVE | DATA FLOAT

C/$\overline{D}$

t_{AR} t_{RA}

$\overline{CS}$

t_{AR} t_{RA}

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

WRITE CONTROL OR OUTPUT PORT CYCLE (CPU → USART)
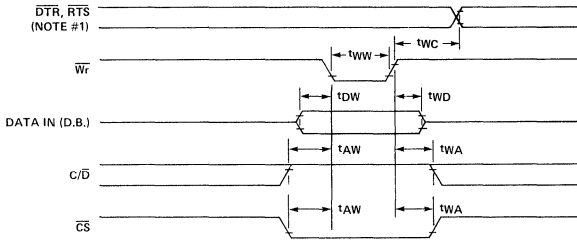
READ CONTROL OR INPUT PORT (CPU ← USART)
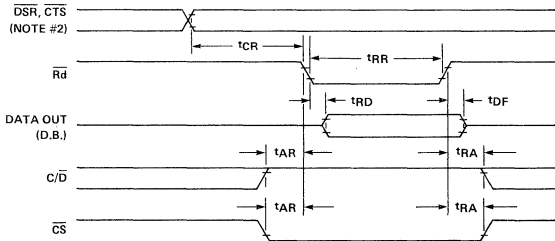
NOTE #1: T_{WC} INCLUDES THE RESPONSE TIMING OF A CONTROL BYTE.
NOTE #2: T_{CR} INCLUDES THE EFFECT OF CTS ON THE TxENBL CIRCUITRY.

TRANSMITTER CONTROL & FLAG TIMING (ASYNC MODE)
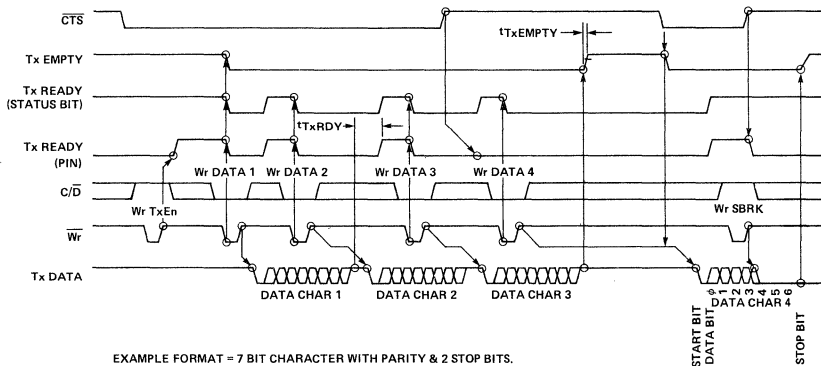
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

RECEIVER CONTROL & FLAG TIMING (ASYNC MODE)
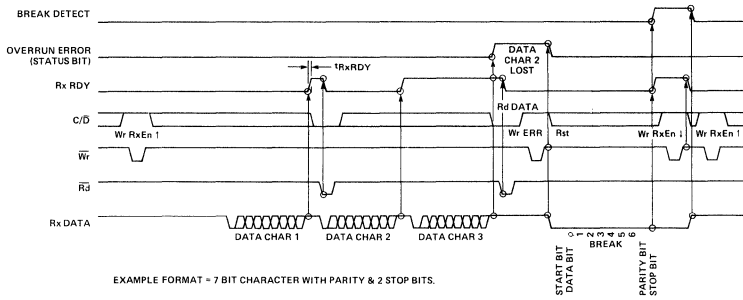
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

TRANSMITTER CONTROL & FLAG TIMING (SYNC MODE)
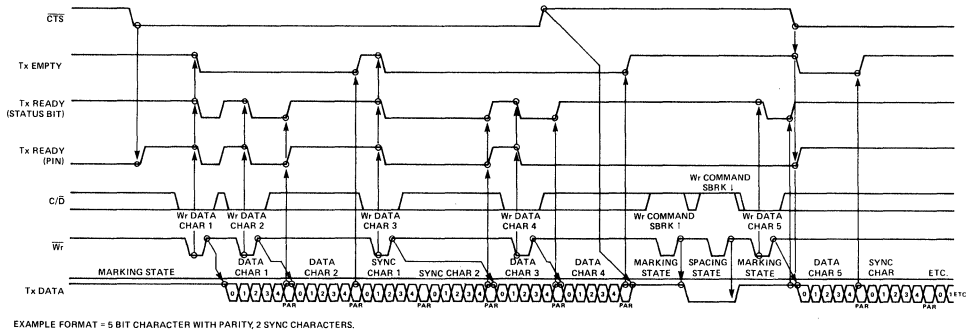
EXAMPLE FORMAT = 5 BIT CHARACTER WITH PARITY, 2 SYNC CHARACTERS.

RECEIVER CONTROL & FLAG TIMING (SYNC MODE)
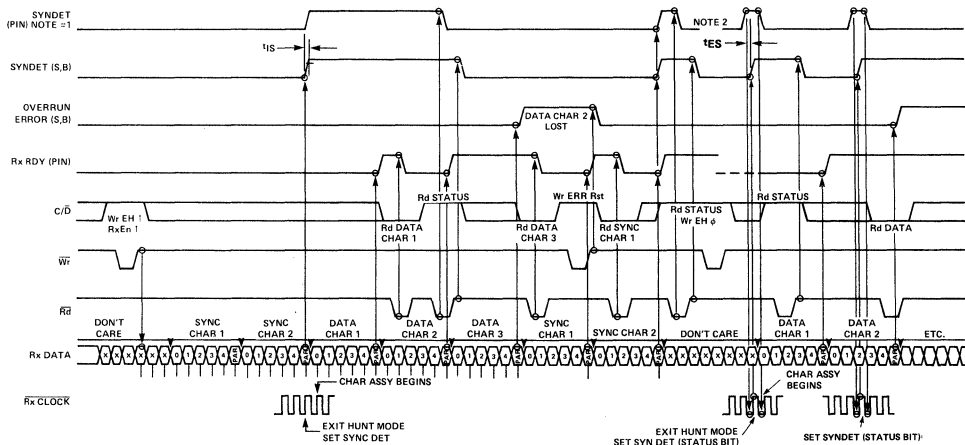
NOTE #1: INTERNAL SYNC, 2 SYNC CHARACTERS, 5 BITS, WITH PARITY
NOTE #2: EXTERNAL SYNC, 5 BITS, WITH PARITY

intel®

M8251
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
  - **Synchronous:**
    5-8 Bit Characters
    Internal or External Character Synchronization
    Automatic Sync Insertion
  - **Asynchronous:**
    5-8 Bit Characters
    Clock Rate — 1, 16 or 64 Times Baud Rate
    Break Character Generation
    1, 1½, or 2 Stop Bits
    False Start Bit Detection

- **Baud Rate — DC to 56k Baud (Sync Mode)**
  DC to 8.1k Baud (Async Mode)
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080 CPU**
- **All Inputs and Outputs Are TTL Compatible**
- **Full Military Temperature Range -55°C to +125°C**
- **±10% Power Supply Tolerance**

The M8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology.
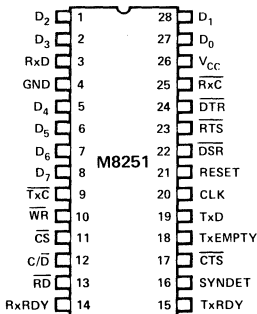
PIN CONFIGURATION

M8251 BLOCK DIAGRAM

Pin Name	Pin Function
D7-D0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
Vcc	+5 Volt Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . –55°C to +125°C

Storage Temperature . . . .–65°C to +150°C

Voltage On Any Pin
    With Respect to GND . . . . –0.5V to +7V

Power Dissipation . . . . 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = -55°C$ to $+125°C$; $V_{CC} = 5.0V \pm 10\%$; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	–.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 1.6mA$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -100\mu A$
I_{DL}	Data Bus Leakage			–50	μA	$V_{OUT} = .45V$
				10	μA	$V_{OUT} = V_{CC}$
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.5V$
I_{CC}	Power Supply Current		45	80		

CAPACITANCE

$T_A = 25°C$; $V_{CC} = $ GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

TEST LOAD CIRCUIT:
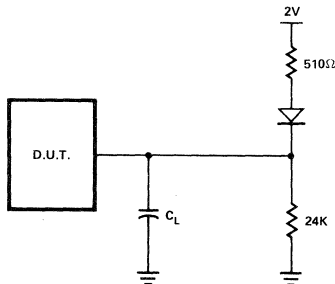
Figure 1.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE (dB)
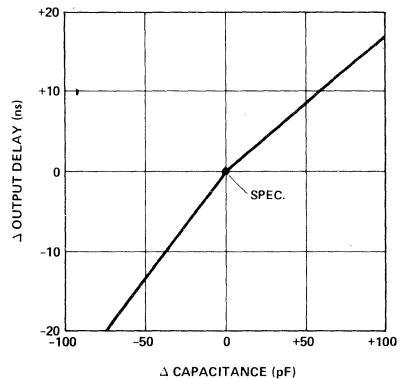
A.C. CHARACTERISTICS [2]

T_A = -55°C to +125°C; V_{CC} = 5.0V ±10% ; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{CY}	Clock Period	.420		1.35	μs	
$t_{\phi W}$	Clock Pulse Width	220			ns	
t_R, t_F	Clock Rise and Fall Time	0		50	ns	
t_{WR}	$\overline{WRITE}$ Pulse Width	400			ns	
t_{DS}	Data Set-Up Time for $\overline{WRITE}$	200			ns	
t_{DH}	Data Hold Time for $\overline{WRITE}$	40			ns	
t_{AW}	Address Stable before $\overline{WRITE}$	20			ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	20			ns	
t_{RD}	READ Pulse Width	430			ns	
t_{DD}	Data Delay from $\overline{READ}$			350	ns	
t_{DF}	$\overline{READ}$ to Data Floating [3]	25		200	ns	C_L=15pF to 100pF
t_{AR}	Address (CE, C/$\overline{D}$) Stable before $\overline{READ}$	50			ns	
t_{RA}	Address (CE, C/$\overline{D}$) Hold Time for $\overline{READ}$	5			ns	
t_{DTx}	TxD Delay from Falling Edge of TxC			1	μs	
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2			μs	
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2			μs	
f_{Tx} [1]	Transmitter Clock Frequency					
	1X Baud Rate	DC		56	KHz	
	16X and 64X Baud Rate	DC		529	KHz	
f_{Rx} [1]	Receiver Clock Frequency					
	1X Baud Rate	DC		56	KHz	
	16X and 64X Baud Rate	DC		529	KHz	
t_{Tx}	TxRDY Delay from Center of Data Bit			16	CLK Period	
t_{Rx}	RxRDY Delay from Center of Data Bit	15		20	CLK Period	
t_{IS}	Internal Syndet Delay from Center of Data Bit	20		25	CLK Period	
t_{ES}	External Syndet Set-Up Time before Falling Edge of RxC			16	CLK Period	

Note 1: The TxC and RxC frequencies have the following limitation with respect to CLK.

  For ASYNC Mode, t_{Tx} or $t_{Rx} \geqslant$ 4.5 t_{CY}

  For SYNC Mode, t_{Tx} or $t_{Rx} \geqslant$ 30 t_{CY}

  2. AC timings are measured at V_{OH} = 2.0V, V_{OL} = 0.8V, and load circuit of Figure 1.

  3. Float timings are measured at V_{OH} = 2.48V, V_{OL} = 2.08V

Figure 1. Test Load Circuit.
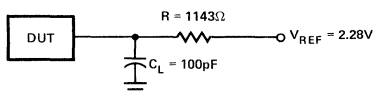
intel®

8253, 8253-5
PROGRAMMABLE INTERVAL TIMER

- **MCS-85™ Compatible 8253-5**
- **3 Independent 16-Bit Counters**
- **DC to 2 MHz**
- **Programmable Counter Modes**

- **Count Binary or BCD**
- **Single +5V Supply**
- **24 Pin Dual-In-Line Package**

The 8253 is a programmable counter/timer chip designed for use as an Intel Microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as three independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

PIN CONFIGURATION

D_7	1	24	V_{CC}
D_6	2	23	$\overline{WR}$
D_5	3	22	$\overline{RD}$
D_4	4	21	$\overline{CS}$
D_3	5	20	A_1
D_2	6	19	A_0
D_1	7	18	CLK 2
D_0	8	17	OUT 2
CLK 0	9	16	GATE 2
OUT 0	10	15	CLK 1
GATE 0	11	14	GATE 1
GND	12	13	OUT 1

8253
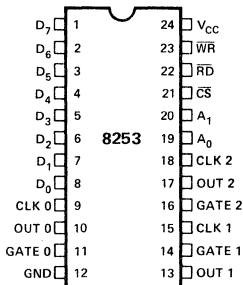
PIN NAMES

D_7-D_0	DATA BUS (8-BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
$\overline{RD}$	READ COUNTER
$\overline{WR}$	WRITE COMMAND OR DATA
$\overline{CS}$	CHIP SELECT
A_0-A_1	COUNTER SELECT
V_{CC}	+5 VOLTS
GND	GROUND

BLOCK DIAGRAM
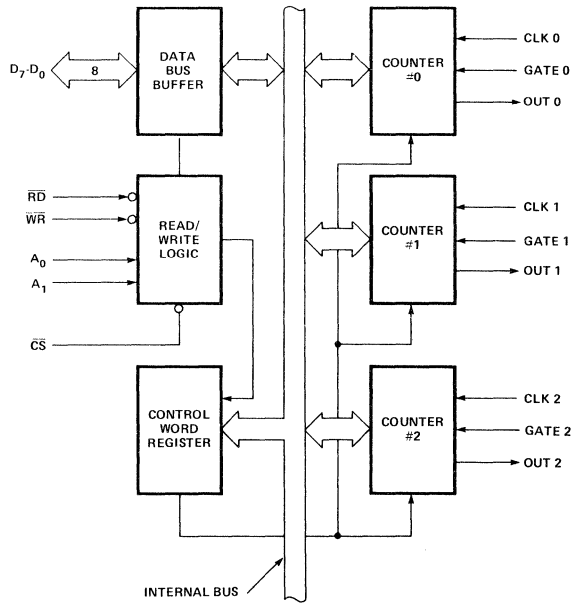
8253 BASIC FUNCTIONAL DESCRIPTION

General

The 8253 is a programmable interval timer/counter specifically designed for use with the Intel™ Micro-computer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.
- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

$\overline{WR}$ (Write)

A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counters.
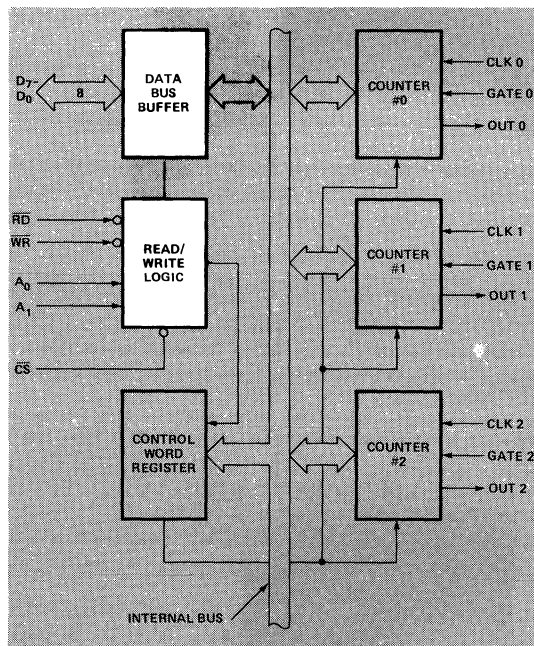
8253 BLOCK DIAGRAM

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

8253 SYSTEM INTERFACE

The 8253 is a component of the Intel™ Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel® 8205 for larger systems.

8253 BLOCK DIAGRAM
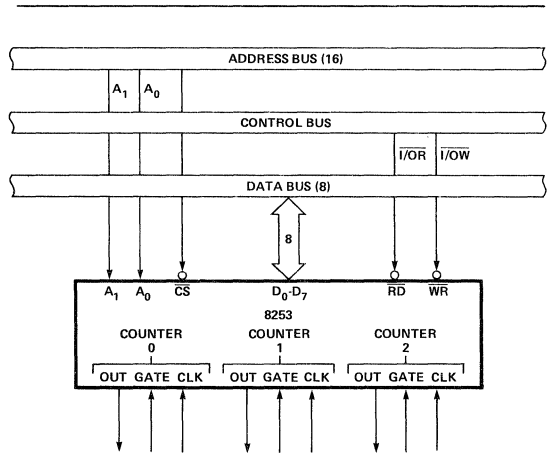
8253 SYSTEM INTERFACE

8253 DETAILED OPERATIONAL DESCRIPTION

General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11)

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control Fields

SC-Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL-Read/Load

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE Procedure Section)
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M-MODE

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

MODE Definition

MODE 0: Interrupt on terminal count.
The OUTput will be initially low after the Mode set operation. After the count is loaded into the selected count register, the OUTput will remain low and the counter will count. When terminal count is reached the OUTput will go high and remain high until the selected count register is reloaded with the Mode.

Reloading a counter register during counting results in the following:

(1) Load 1st byte stops the current counting.

(2) Load 2nd byte starts the new count.

The GATE input will enable the counting when high and inhibit counting when low.

MODE 1: Programmable One-Shot.
The OUTput will go low on the count following the rising edge of the GATE input.

The OUTput will go high on the terminal count. If a new count value is loaded while the OUTput is low it will not affect the duration of the One-Shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator

Divide by N counter. The OUTput will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The GATE input, when low, will force the OUTput high. When the GATE input goes high, the counter will start from the initial count. Thus, the GATE input can be used to synchronize the counter.

When this MODE is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator.

Similar to MODE 2 except that the OUTput will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. If the count is odd, the OUTput will be high for (N+1)/2 counts and low for (N-1)/2 counts.

If the counter register is reloaded with a new value during counting, this new value will be reflected immediately after the output transition of the current count.

MODE 4: Software triggered strobe.

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

MODE 5: Hardware triggered strobe.

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

GATE Pin Operations Summary

Modes	Low Or Going Low	Rising	High
0	Disables counting	——	Enables counting
1	——	1) Initiates counting 2) Resets output after next clock	——
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	——	Enables counting
5	——	Initiates counting	——

MODE 0

CLOCK

$\overline{WR}$ n

OUTPUT (INTERRUPT)   4 3 2 1 0

(n = 4) ⟵ n ⟶

$\overline{WR}$ m

GATE

OUTPUT (INTERRUPT)   5 4   3 2 1 0

(m = 5)

A   B

A + B = m

MODE 1

CLOCK

$\overline{WR}$ n

TRIGGER

OUTPUT   4 3 2 1 0

(n = 4)

TRIGGER

OUTPUT   4 3 2 4 3 2 1 0

MODE 2

CLOCK

$\overline{WR}$ n   n = 4   n = 3

OUTPUT   4 3 2 1 0(4) 3 2 1 0(3) 2 1 0

OUTPUT (n = 3)   0(3)   3 2 1 0(3) 2 1 0(3) 2 1

RESET

MODE 3

CLOCK

OUTPUT (n = 4)   0(4) 3 2 1 0(4) 3 2 1 0(4) 3 2 1

OUTPUT (n = 5)   0(5) 4 3 2 1 0(5) 4 3 2 1 0(5) 4 3

OUTPUT (n = 4)   4 3 2 1 0(4) 3 2 1

RESET

MODE 4

CLOCK

$\overline{WR}$ n = 4

OUTPUT   4 3 2 1 0

LOAD n   n = 4

GATE

OUTPUT   4   4 3 2 1 0

MODE 5

CLOCK

GATE

OUTPUT (n = 4)   4 3 2 1 0

GATE

OUTPUT (n = 4)   4 3 4 3 2 1 0

8253 TIMING DIAGRAMS

8253 READ/WRITE PROCEDURE

Write Operations

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1)

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it must be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

Programming Format

MODE Control Word Counter n	
LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Alternate Programming Formats

Example:

			A1	A0
No. 1		MODE Control Word Counter 0	1	1
No. 2		MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	1	0
No. 7	MSB	Count Register Byte Counter 2	1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

8253 READ/WRITE PROCEDURE

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0, A1-11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter <u>must be inhibited</u> either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

first I/O Read contains the least significant byte (LSB).

second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the 8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read then two bytes <u>must</u> be read before any loading WR command can be sent to the same counter.

Read Operation Chart

A1	A0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

Reading While Counting

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register is available.

MODE Register for Latching Count

A0, A1 = 11

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1,SC0 — specify counter to be latched.

D5,D4   — 00 designates counter latching operation.

X   — don't care.

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed.

MCS-85™ Clock Interface*
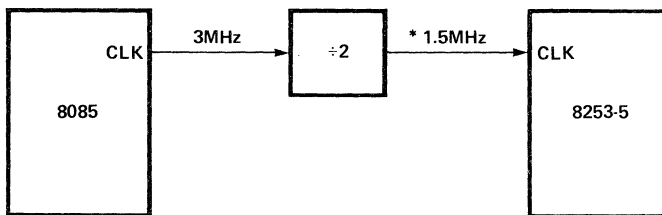
*If an 8085 clock output is to drive an 8253-5 clock input, it must be reduced to 2MHz or less.

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .... 0°C to 70°C
Storage Temperature .... −65°C to +150°C
Voltage On Any Pin
  With Respect to Ground .... −0.5 V to +7 V
Power Dissipation .... 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}+.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V
I_{CC}	V_{CC} Supply Current		1.40	mA	

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

BUS PARAMETERS: (Note 1)

READ CYCLE

SYMBOL	PARAMETER	8253		8253-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{AR}	Address Stable Before $\overline{READ}$	50		50		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		5		ns
t_{RR}	$\overline{READ}$ Pulse Width	400		300		ns
t_{RD}	Data Delay From $\overline{READ}$ [2]		300		200	ns
t_{DF}	$\overline{READ}$ to Data Floating	25	125	25	100	ns

WRITE CYCLE

SYMBOL	PARAMETER	8253		8253-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{AW}	Address Stable Before $\overline{WRITE}$	50		50		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	30		30		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		300		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		250		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		30		ns
t_{RV}	Recovery Time Between $\overline{WRITES}$	1		1		μs

Notes: 1. AC timings measured at V_{OH} = 2.2, V_{OL} = 0.8, and with load circuit of Figure 1.
2. Test Conditions: 8253, C_L = 100pF; 8253-5: C_L = 150pF.

WRITE TIMING
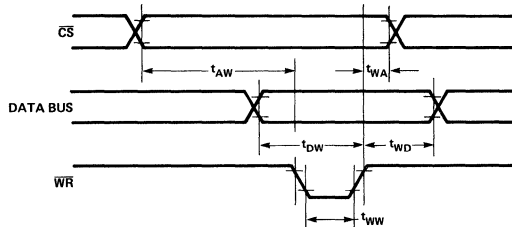
READ TIMING

INPUT WAVEFORMS FOR A.C. TESTS:

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.
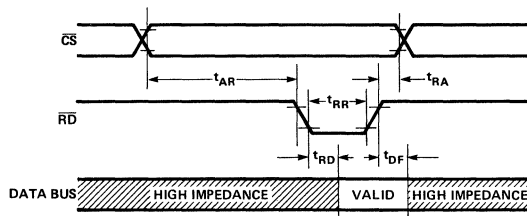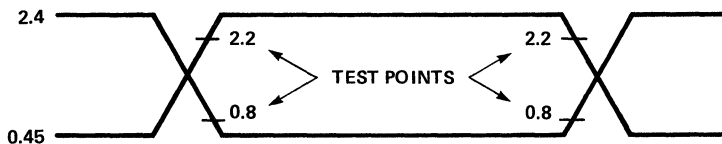
A.C. CHARACTERISTICS (Cont'd): $T_A = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V

CLOCK AND GATE TIMING

SYMBOL	PARAMETER	8253		8253-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{CLK}	Clock Period	380	dc	380	dc	ns
t_{PWH}	High Pulse Width	230		230		ns
t_{PWL}	Low Pulse Width	150		150		ns
t_{GW}	Gate Width High	150		150		ns
t_{GL}	Gate Width Low	100		100		ns
t_{GS}	Gate Set Up Time to CLK↑	100		100		ns
t_{GH}	Gate Hold Time After CLK↑	50		50		ns
t_{OD}	Output Delay From CLK↓[1]		400		400	ns
t_{ODG}	Output Delay From Gate↓[1]		300		300	ns

Note 1:   Test Conditions: 8253: $C_L = 100pF$; 8253-5: $C_L = 150pF$.
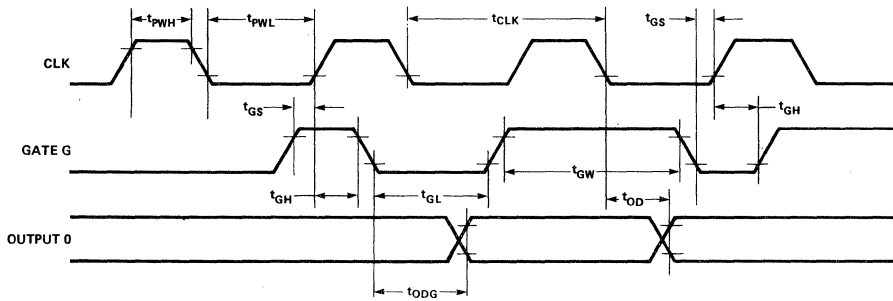
int_el®

8255A, 8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- **MCS-85™ Compatible 8255A-5**
- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Fully Compatible with Intel Microprocessor Families**
- **Improved Timing Characteristics**

- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **40 Pin Dual-In-Line Package**
- **Reduces System Package Count**
- **Improved DC Driving Capability**

The 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bi-directional Bus mode which uses 8 lines for a bi-directional bus, and five lines, borrowing one from the other group, for handshaking.

PIN CONFIGURATION

```
PA3  [ 1      40 ] PA4
PA2  [ 2      39 ] PA5
PA1  [ 3      38 ] PA6
PA0  [ 4      37 ] PA7
RD   [ 5      36 ] WR
CS   [ 6      35 ] RESET
GND  [ 7      34 ] D0
A1   [ 8      33 ] D1
A0   [ 9      32 ] D2
PC7  [ 10     31 ] D3
PC6  [ 11     30 ] D4    8255A
PC5  [ 12     29 ] D5
PC4  [ 13     28 ] D6
PC0  [ 14     27 ] D7
PC1  [ 15     26 ] VCC
PC2  [ 16     25 ] PB7
PC3  [ 17     24 ] PB6
PB0  [ 18     23 ] PB5
PB1  [ 19     22 ] PB4
PB2  [ 20     21 ] PB3
```

8255A BLOCK DIAGRAM

PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	Ø VOLTS

8255 BASIC FUNCTIONAL DESCRIPTION

General

The 8255 is a Programmable Peripheral Interface (PPI) device designed for use in Intel Microcomputer Systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255 is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state, bi-directional, eight bit buffer is used to interface the 8255 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions by the CPU. Control Words and Status information are also transferred through the Data Bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select: A "low" on this input pin enables the communication between the 8255 and the CPU.

($\overline{RD}$)

Read: A "low" on this input pin enables the 8255 to send the Data or Status information to the CPU on the Data Bus. In essence, it allows the CPU to "read from" the 8255.

($\overline{WR}$)

Write: A "low" on this input pin enables the CPU to write Data or Control words into the 8255.

(A_0 and A_1)

Port Select 0 and Port Select 1: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the Control Word Register. They are normally connected to the least significant bits of the Address Bus (A_0 and A_1).

8255 BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A $\Rightarrow$ DATA BUS
0	1	0	1	0	PORT B $\Rightarrow$ DATA BUS
1	0	0	1	0	PORT C $\Rightarrow$ DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS $\Rightarrow$ PORT A
0	1	1	0	0	DATA BUS $\Rightarrow$ PORT B
1	0	1	0	0	DATA BUS $\Rightarrow$ PORT C
1	1	1	0	0	DATA BUS $\Rightarrow$ CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS $\Rightarrow$ 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS $\Rightarrow$ 3-STATE
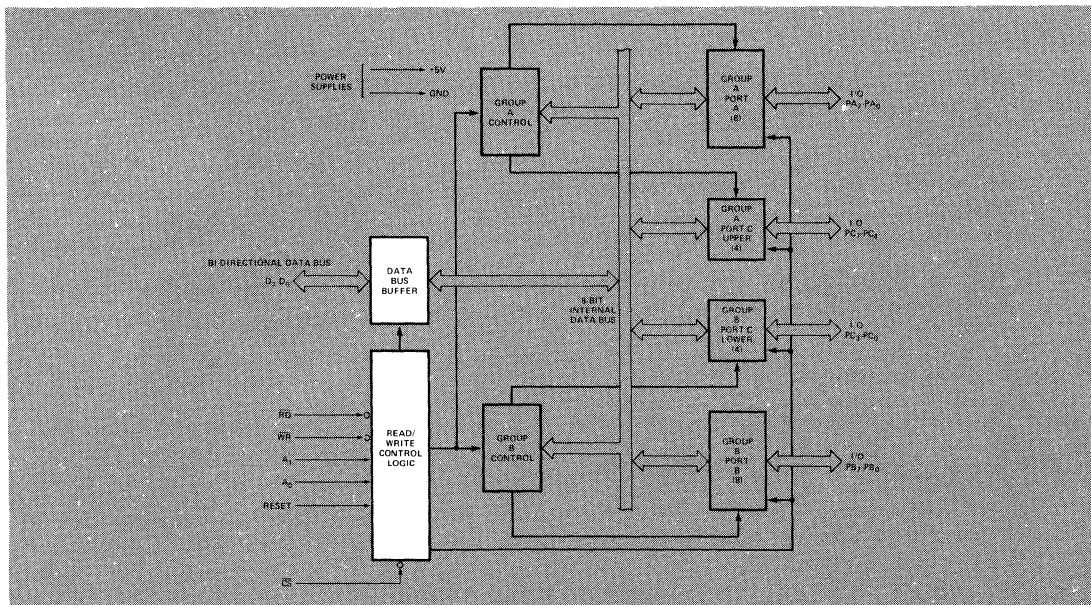
8255 Block Diagram

(RESET)

Reset: A "high" on this input clears all internal registers including the Control Register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255. The control word contains information such as "mode", "bit set", "bit reset" etc. that initializes the functional configuration of the 8255.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A — Port A and Port C upper (C7-C4)
Control Group B — Port B and Port C lower (C3-C0)

The Control Word Register can **Only** be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255 contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255.

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B.

8255 BLOCK DIAGRAM

PIN CONFIGURATION

PIN NAMES

$D_7 - D_0$	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255 DETAILED OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

    Mode 0 — Basic Input/Output
    Mode 1 — Strobed Input/Output
    Mode 2 — Bi-Directional Bus

When the RESET input goes "high" all ports will be set to the Input mode (i.e., all 24 lines will be in the high impedance state). After the RESET is removed the 8255 can remain in the Input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single OUTput instruction. This allows a single 8255 to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.
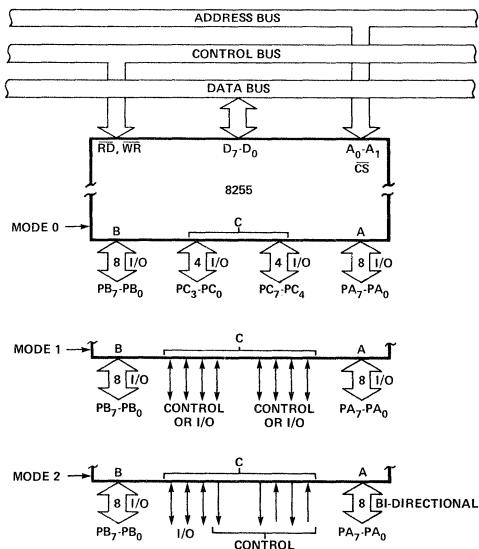
Basic Mode Definitions and Bus Interface
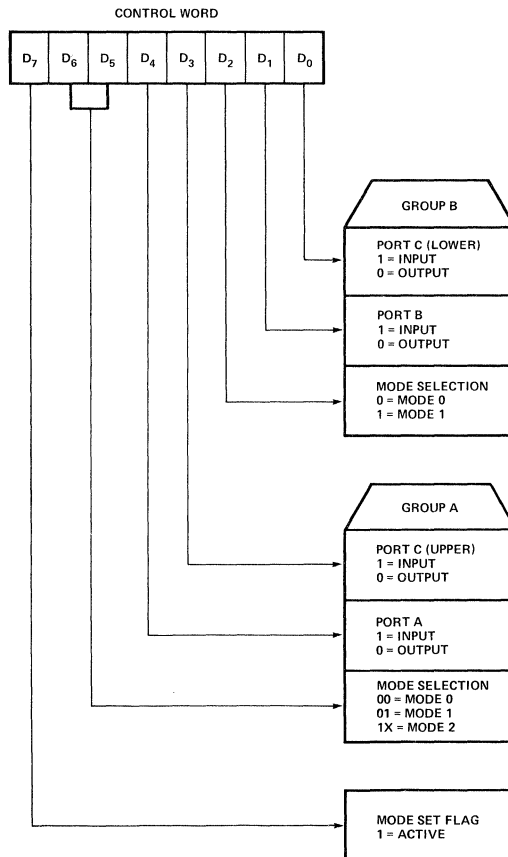
Mode Definition Format

The Mode definitions and possible Mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255 has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

CONTROL WORD

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

x x x

DON'T CARE

BIT SET/RESET
1 = SET
0 = RESET

BIT SELECT

	0	1	2	3	4	5	6	7	
	0	1	0	1	0	1	0	1	B_0
	0	0	1	1	0	0	1	1	B_1
	0	0	0	0	1	1	1	1	B_2

BIT SET/RESET FLAG
0 = ACTIVE

Bit Set/Reset Format
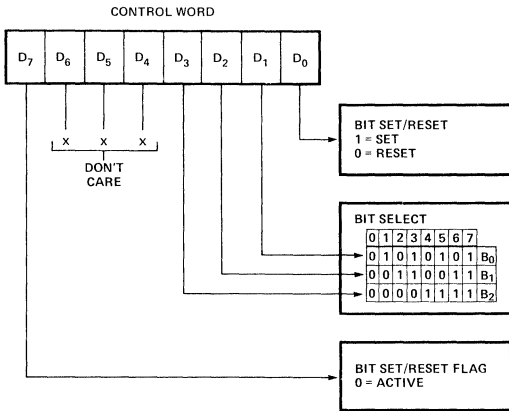
When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255 is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the Bit set/reset function of Port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) — INTE is SET — Interrupt enable
(BIT-RESET) — INTE is RESET — Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes
Mode 0 (Basic Input/Output)

This functional configuration provides simple Input and Output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:
- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.
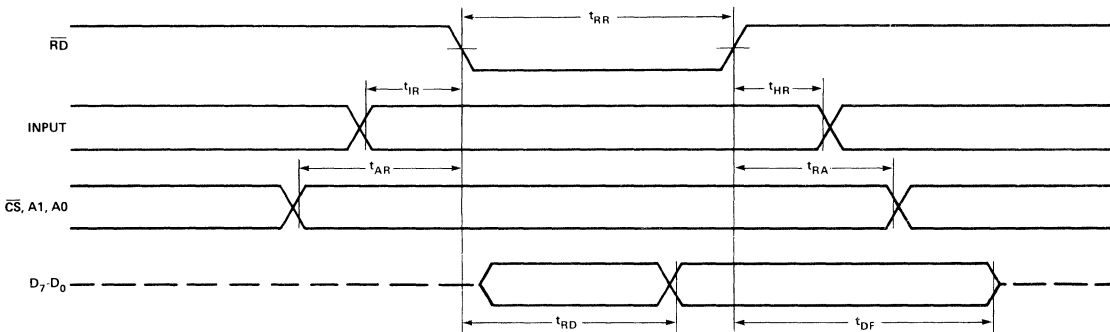
Mode 0 (Basic Input)
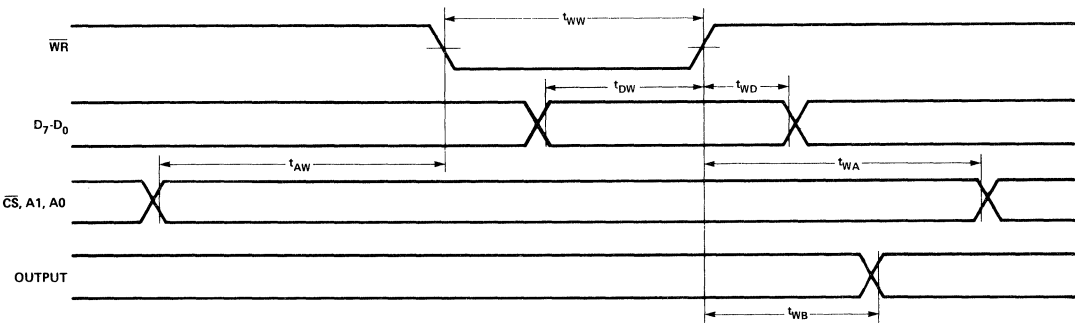
Mode 0 (Basic Output)

MODE 0 PORT DEFINITION CHART

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 CONFIGURATIONS
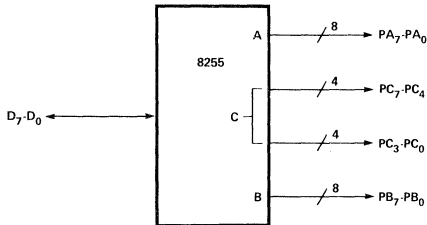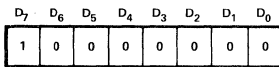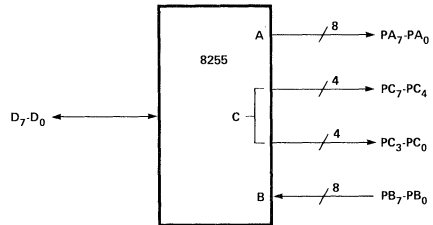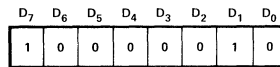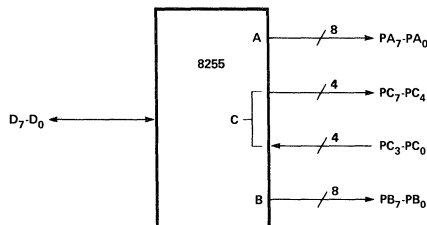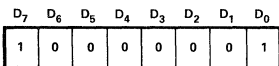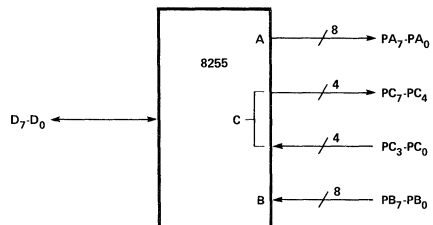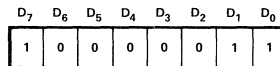
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0
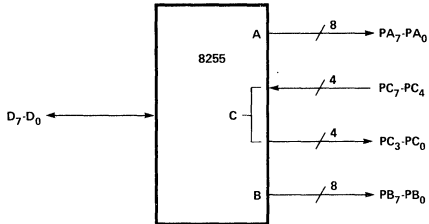
CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0
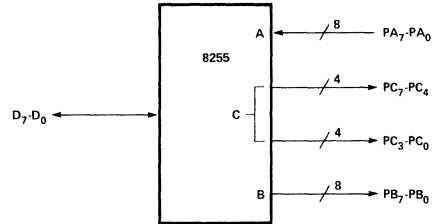
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1
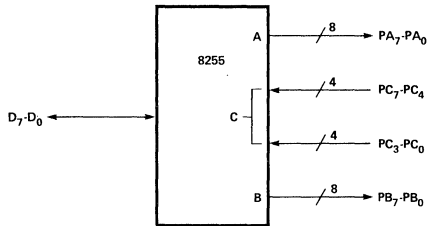
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1
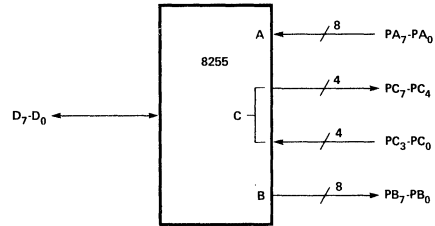
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0
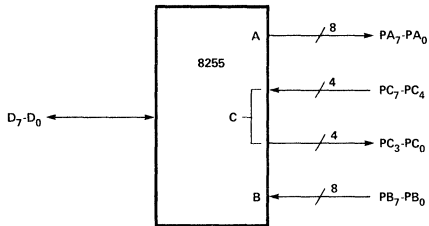
CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0
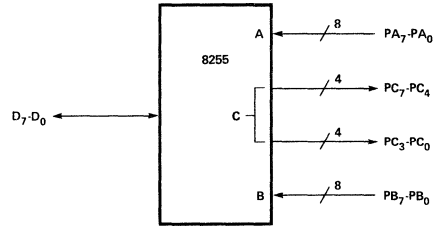
CONTROL WORD #7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1
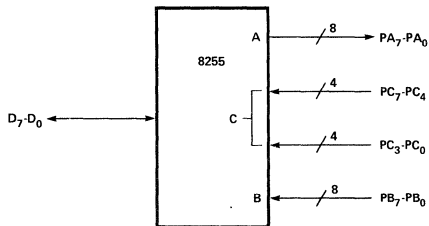
CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1
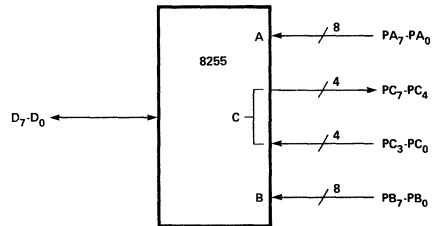
CONTROL WORD #12

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	0
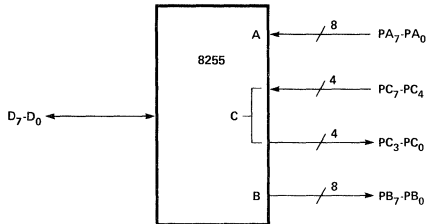
CONTROL WORD #14

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	1	0
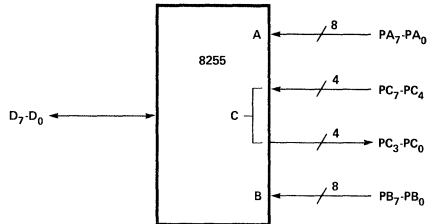
CONTROL WORD #13

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	1
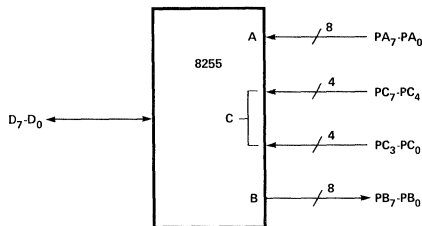
CONTROL WORD #15

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	1	1
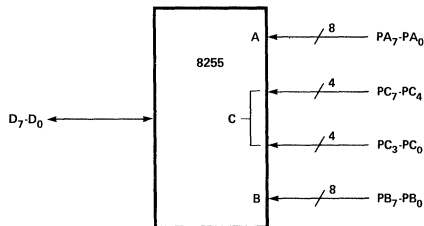
Operating Modes

Mode 1 (Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

STB (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the STB is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of RD. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

MODE 1 (PORT A)

CONTROL WORD

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

| 1 | 0 | 1 | 1 | 1/0 | | | |

$PC_{6,7}$
1 = INPUT
0 = OUTPUT

PA_7-PA_0 8

INTE A PC_4 ← $\overline{STB}_A$

PC_5 → IBF_A

PC_3 → $INTR_A$

$PC_{6,7}$ 2 I/O

$\overline{RD}$

MODE 1 (PORT B)

CONTROL WORD

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

| 1 | | | | | 1 | 1 | |

PB_7-PB_0 8

INTE B PC_2 ← $\overline{STB}_B$

PC_1 → IBF_B

PC_0 → $INTR_B$

$\overline{RD}$
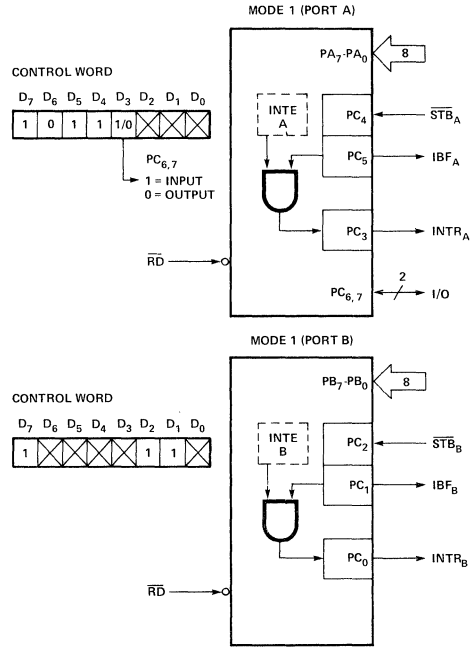
Mode 1 Input
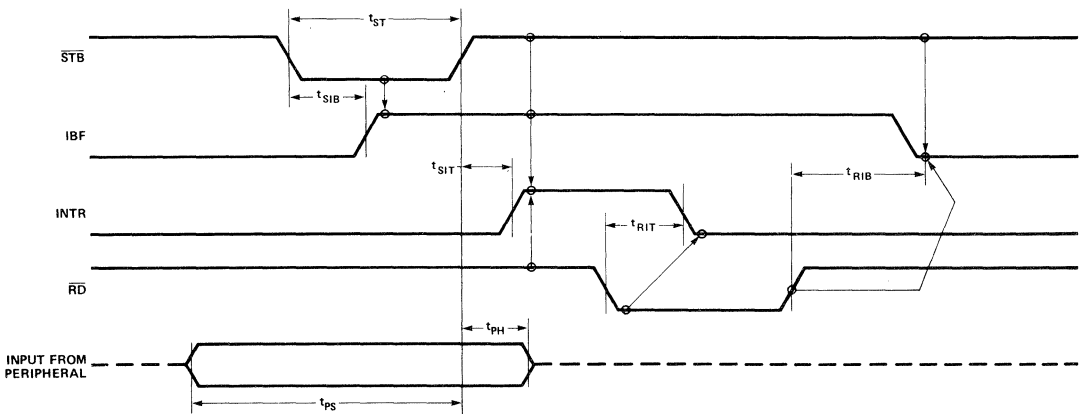
Mode 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ (Acknowledge Input)

A "low" on this input informs the 8255 that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.
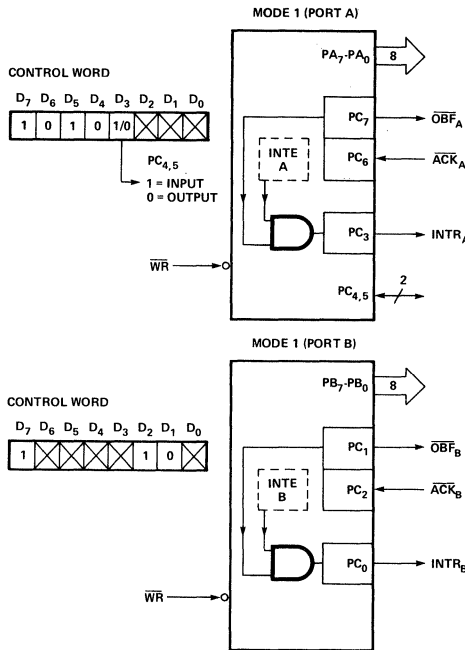
Mode 1 Output
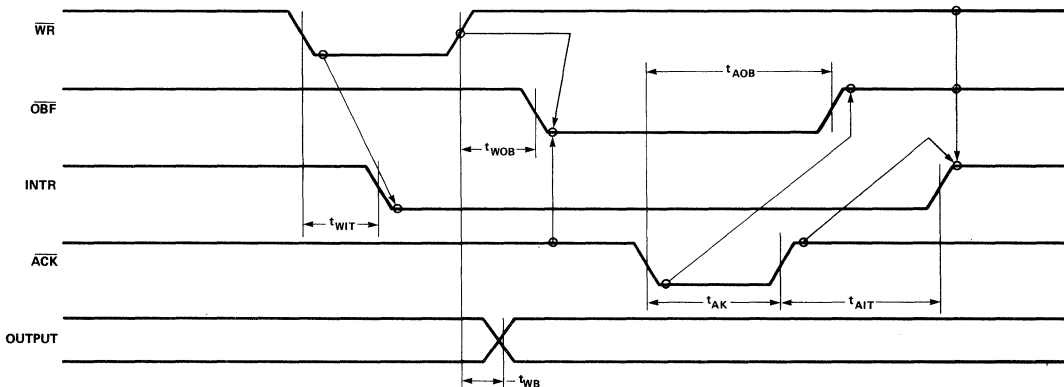
Mode 1 (Strobed Output)

Combinations of Mode 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

CONTROL WORD

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	1/0	1	0	X

$PC_{6,7}$
1 = INPUT
0 = OUTPUT

PORT A – (STROBED INPUT)
PORT B – (STROBED OUTPUT)

CONTROL WORD

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	1/0	1	1	X

$PC_{4,5}$
1 = INPUT
0 = OUTPUT

PORT A – (STROBED OUTPUT)
PORT B – (STROBED INPUT)
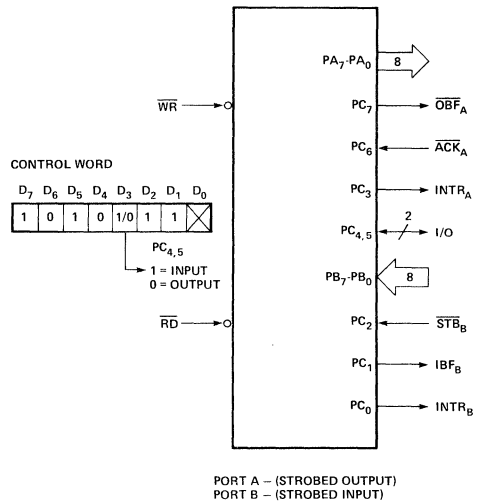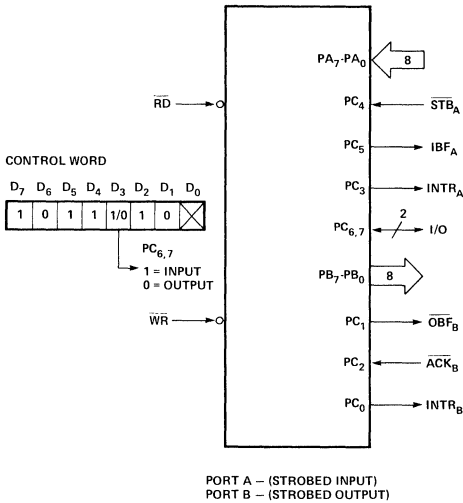
Operating Modes

Mode 2 (Strobed Bi-Directional Bus I/O)

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:
- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bi-Directional Bus I/O Control Signal Definition

INTR (Interrupt Request)

A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to Port A.

$\overline{ACK}$ (Acknowledge)

A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high-impedance state.

INTE 1 (The INTE Flip-Flop associated with $\overline{OBF}$)

Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop associated with IBF)

Controlled by bit set/reset of PC_4.
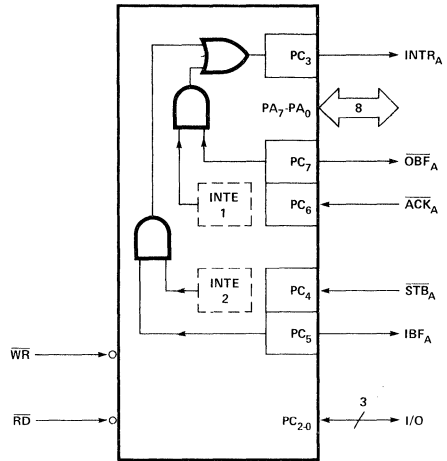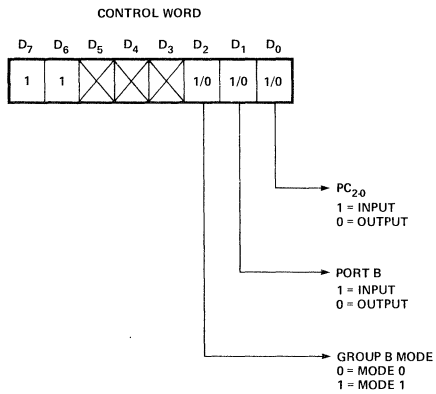
CONTROL WORD

Mode 2 Control Word

Mode 2
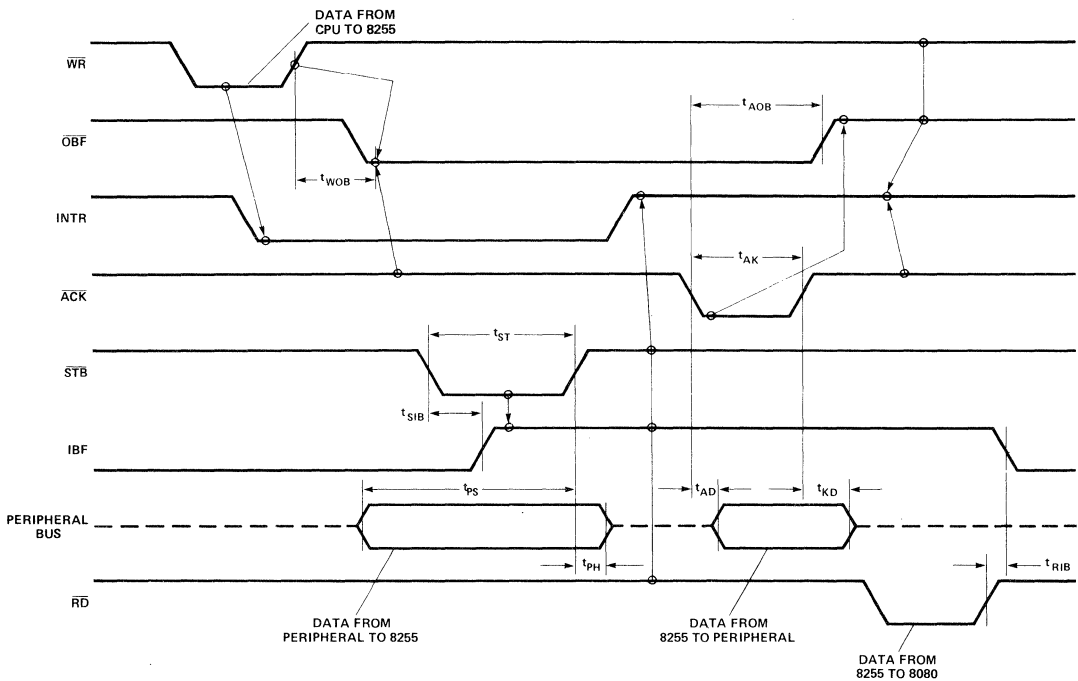
Mode 2 (Bi-directional)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

MODE 2 AND MODE 0 (INPUT)

PC$_3$	→ INTR$_A$
PA$_7$-PA$_0$	⟷ 8
PC$_7$	→ $\overline{OBF}_A$
PC$_6$	← $\overline{ACK}_A$
PC$_4$	← $\overline{STB}_A$
PC$_5$	→ IBF$_A$
PC$_{2-0}$	3 → I/O
PB$_7$-PB$_0$	← 8

CONTROL WORD

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	1	✕	✕	0	1	1/0	

PC$_{2-0}$
1 = INPUT
0 = OUTPUT

$\overline{RD}$ →

$\overline{WR}$ →

MODE 2 AND MODE 0 (OUTPUT)

PC$_3$	→ INTR$_A$
PA$_7$-PA$_0$	⟷ 8
PC$_7$	→ $\overline{OBF}_A$
PC$_6$	← $\overline{ACK}_A$
PC$_4$	← $\overline{STB}_A$
PC$_5$	→ IBF$_A$
PC$_{2-0}$	3 → I/O
PB$_7$-PB$_0$	→ 8

CONTROL WORD

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	1	✕	✕	0	0	1/0	

PC$_{2-0}$
1 = INPUT
0 = OUTPUT

$\overline{RD}$ →

$\overline{WR}$ →

MODE 2 AND MODE 1 (OUTPUT)

PC$_3$	→ INTR$_A$
PA$_7$-PA$_0$	⟷ 8
PC$_7$	→ $\overline{OBF}_A$
PC$_6$	← $\overline{ACK}_A$
PC$_4$	← $\overline{STB}_A$
PC$_5$	→ IBF$_A$
PB$_7$-PB$_0$	→ 8
PC$_1$	→ $\overline{OBF}_B$
PC$_2$	← $\overline{ACK}_B$
PC$_0$	→ INTR$_B$

CONTROL WORD

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	1	✕	✕	1	0	✕	

$\overline{RD}$ →

$\overline{WR}$ →

MODE 2 AND MODE 1 (INPUT)

PC$_3$	→ INTR$_A$
PA$_7$-PA$_0$	⟷ 8
PC$_7$	→ $\overline{OBF}_A$
PC$_6$	← $\overline{ACK}_A$
PC$_4$	← $\overline{STB}_A$
PC$_5$	→ IBF$_A$
PB$_7$-PB$_0$	← 8
PC$_2$	← $\overline{STB}_B$
PC$_1$	→ IBF$_B$
PC$_0$	→ INTR$_B$

CONTROL WORD

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	1	✕	✕	1	1	✕	

$\overline{RD}$ →

$\overline{WR}$ →

Mode 2 Combinations

MODE DEFINITION SUMMARY TABLE

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	GROUP A ONLY
PA_0	IN	OUT	IN	OUT	←——→
PA_1	IN	OUT	IN	OUT	←——→
PA_2	IN	OUT	IN	OUT	←——→
PA_3	IN	OUT	IN	OUT	←——→
PA_4	IN	OUT	IN	OUT	←——→
PA_5	IN	OUT	IN	OUT	←——→
PA_6	IN	OUT	IN	OUT	←——→
PA_7	IN	OUT	IN	OUT	←——→
PB_0	IN	OUT	IN	OUT	——
PB_1	IN	OUT	IN	OUT	——
PB_2	IN	OUT	IN	OUT	——
PB_3	IN	OUT	IN	OUT	——
PB_4	IN	OUT	IN	OUT	——
PB_5	IN	OUT	IN	OUT	——
PB_6	IN	OUT	IN	OUT	——
PB_7	IN	OUT	IN	OUT	——
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

(Right side bracket for PB rows and PC rows: MODE 0 OR MODE 1 ONLY)

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs —
All input lines can be accessed during a normal Port C read.

If Programmed as Outputs —
Bits in C upper (PC_7-PC_4) must be individually accessed using the bit set/reset function.

Bits in C lower (PC_3-PC_0) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

Source Current Capability on Port B and Port C

Any set of **eight** output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C

allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

INPUT CONFIGURATION

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$

GROUP A   GROUP B

OUTPUT CONFIGURATION

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$

GROUP A   GROUP B

Mode 1 Status Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	╳	╳	╳

GROUP A   GROUP B

(DEFINED BY MODE 0 OR MODE 1 SELECTION)
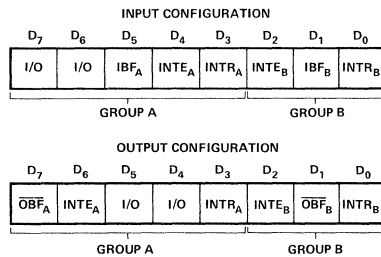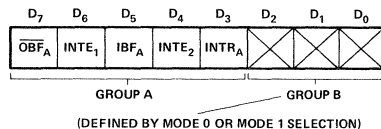
Mode 2 Status Word Format

APPLICATIONS OF THE 8255

The 8255 is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255 is programmed by the I/O service routine and becomes an extension of the systems software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the Detailed Operational Description, a control word can easily be developed to initialize the 8255 to exactly "fit" the application. Here are a few examples of typical applications of the 8255.
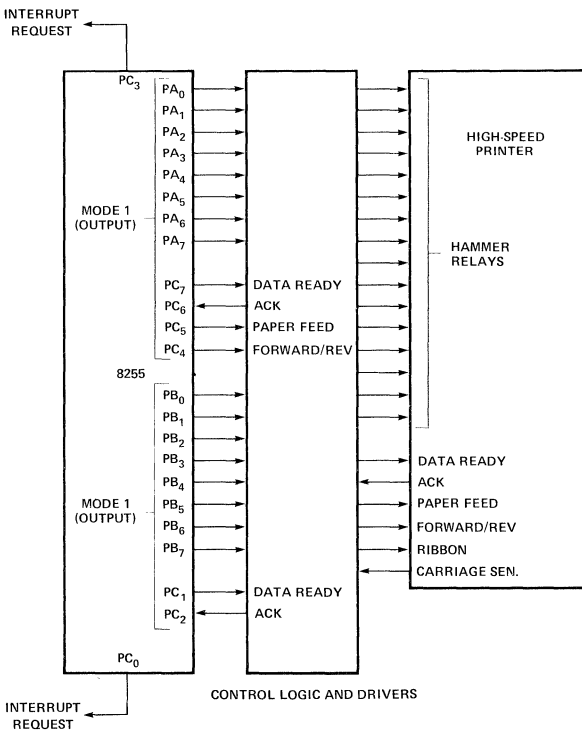
Printer Interface
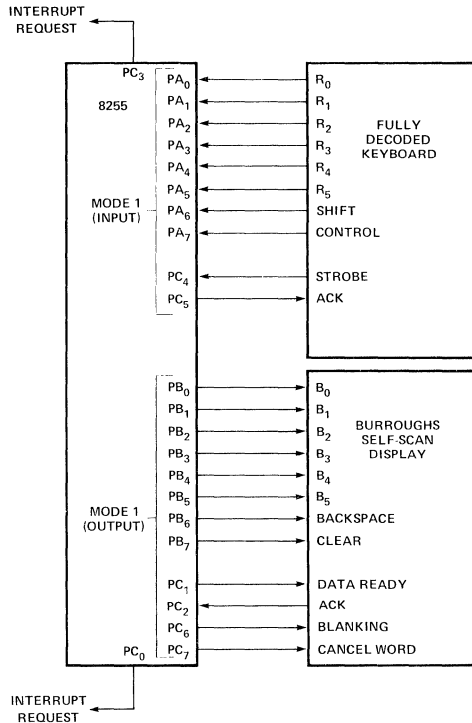
Keyboard and Display Interface
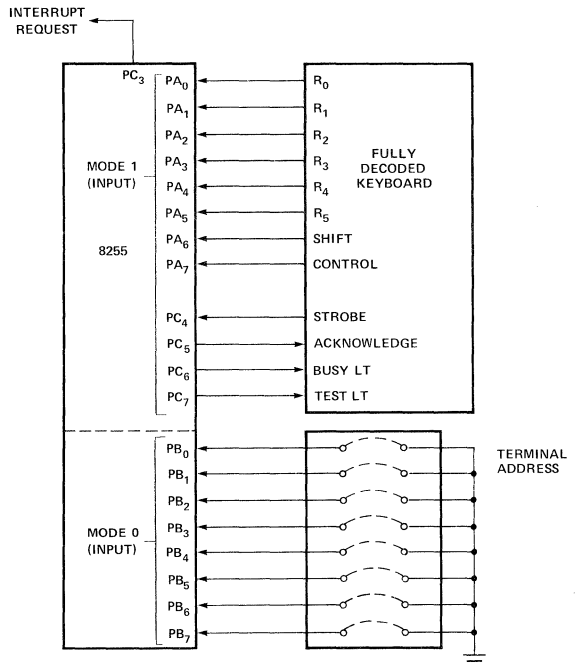
Keyboard and Terminal Address Interface

INTERRUPT REQUEST

MODE 0 (OUTPUT)

PA₀ PA₁ PA₂ PA₃ PA₄ PA₅ PA₆ PA₇ PC₄ PC₅ PC₆ PC₇

LSB

12-BIT D-A CONVERTER (DAC) → ANALOG OUTPUT

MSB

8255

BIT SET/RESET

PC₀ PC₁

STB DATA OUTPUT EN

PC₂ PC₃

SAMPLE EN STB

MODE 0 (INPUT)

PB₀ PB₁ PB₂ PB₃ PB₄ PB₅ PB₆ PB₇

LSB 8-BIT A-D CONVERTER (ADC) ← ANALOG INPUT MSB
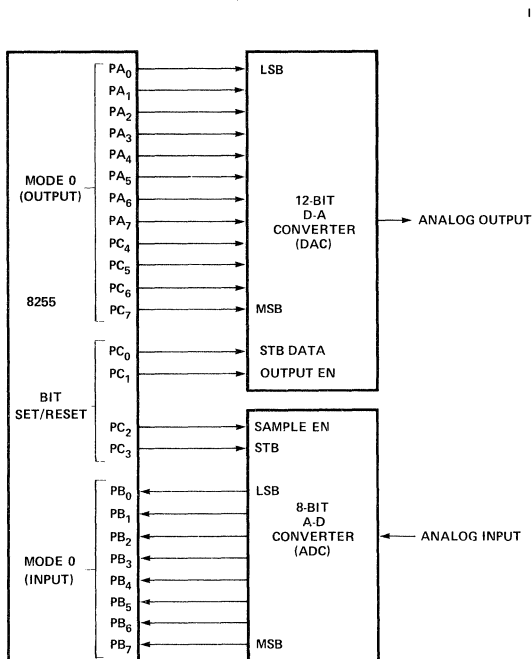
Digital to Analog, Analog to Digital

PC₃

INTERRUPT REQUEST

MODE 2

PA₀ PA₁ PA₂ PA₃ PA₄ PA₅ PA₆ PA₇

D₀ D₁ D₂ D₃ D₄ D₅ D₆ D₇

FLOPPY DISK CONTROLLER AND DRIVE

PC₄ PC₅ PC₇ PC₆

DATA STB ACK (IN) DATA READY ACK (OUT)

8255

PC₂ PC₀ PC₁

TRACK "0" SENSOR SYNC READY INDEX

MODE 0 (OUTPUT)

PB₀ PB₁ PB₂ PB₃ PB₄ PB₅ PB₆ PB₇

ENGAGE HEAD FORWARD/REV. READ ENABLE WRITE ENABLE DISC SELECT ENABLE CRC TEST BUSY LT
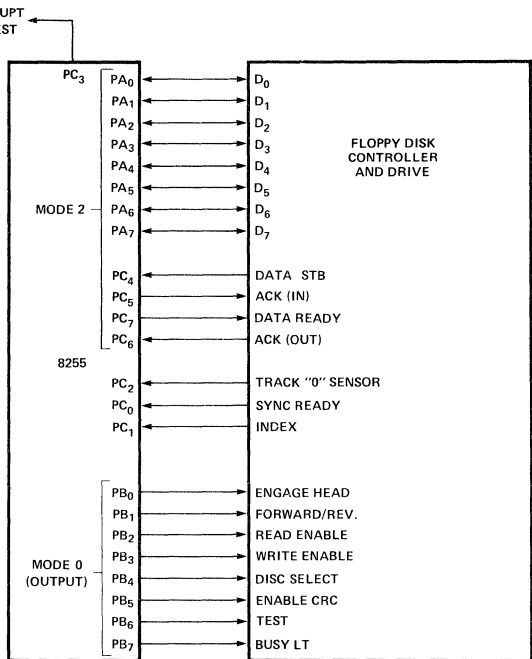
Basic Floppy Disc Interface

INTERRUPT REQUEST

PC₃

MODE 1 (OUTPUT)

PA₀ PA₁ PA₂ PA₃ PA₄ PA₅ PA₆ PA₇

R₀ R₁ R₂ R₃ R₄ R₅ SHIFT CONTROL

CRT CONTROLLER
• CHARACTER GEN.
• REFRESH BUFFER
• CURSOR CONTROL

PC₇ PC₆ PC₅ PC₄

DATA READY ACK BLANKED BLACK/WHITE

8255

PC₂ PC₁ PC₀

ROW STB COLUMN STB CURSOR H/V STB

MODE 0 (OUTPUT)

PB₀ PB₁ PB₂ PB₃ PB₄ PB₅ PB₆ PB₇

CURSOR/ROW/COLUMN ADDRESS H & V
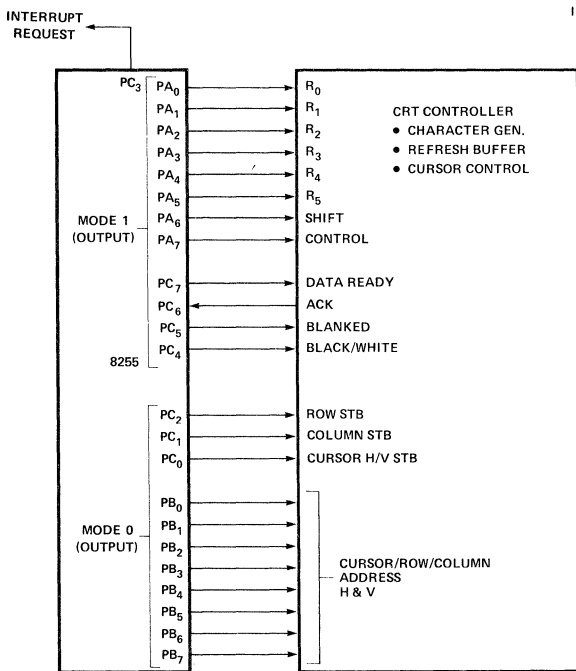
Basic CRT Controller Interface

INTERRUPT REQUEST

PC₃

MODE 1 (INPUT)

PA₀ PA₁ PA₂ PA₃ PA₄ PA₅ PA₆ PA₇

R₀ R₁ R₂ R₃ R₄ R₅ R₆ R₇

8 LEVEL PAPER TAPE READER

PC₄ PC₅ PC₆

STB̄ ACK̄ STOP/GO

8255

MACHINE TOOL

MODE 0 (INPUT)

PC₀ PC₁ PC₂

START/STOP LIMIT SENSOR (H/V) OUT OF FLUID

MODE 0 (OUTPUT)

PB₀ PB₁ PB₂ PB₃ PB₄ PB₅ PB₆ PB₇

CHANGE TOOL LEFT/RIGHT UP/DOWN HOR. STEP STROBE VERT. STEP STROBE SLEW/STEP FLUID ENABLE EMERGENCY STOP
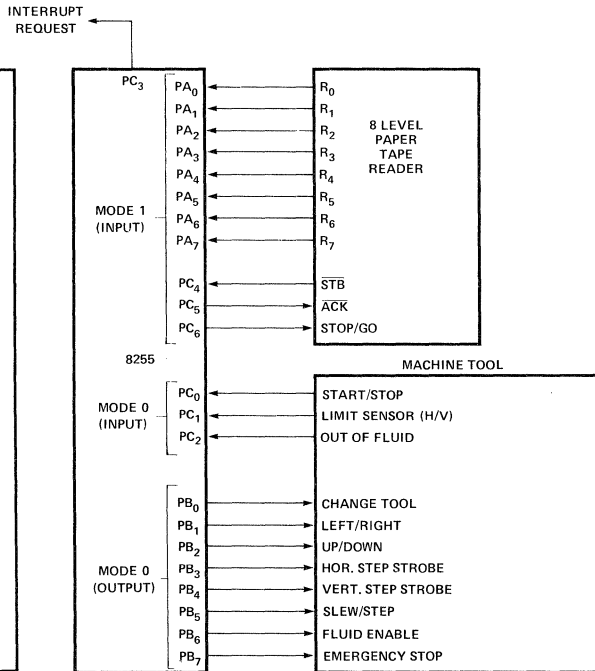
Machine Tool Controller Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . .—65°C to +150°C
Voltage on Any Pin
   With Respect to Ground. . . . .—0.5V to +7V
Power Dissipation . . . . 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = +5V$ ±5%; GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45	V	$I_{OL} = 2.5mA$
V_{OL}(PER)	Output Low Voltage (Peripheral Port)		0.45	V	$I_{OL} = 1.7mA$
V_{OH}(DB)	Output High Voltage (Data Bus)	2.4		V	$I_{OH} = -400\mu A$
V_{OH}(PER)	Output High Voltage (Peripheral Port)	2.4		V	$I_{OH} = -200\mu A$
I_{DAR}[1]	Darlington Drive Current	−1.0	−4.0	mA	$R_{EXT} = 750\Omega$; $V_{EXT} = 1.5V$
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		±10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ to 0V

Note 1:   Available on any 8 pins from Port B and C.

CAPACITANCE $T_A = 25°C$; $V_{CC} = GND = 0V$

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

TEST LOAD CIRCUIT (FOR DB)
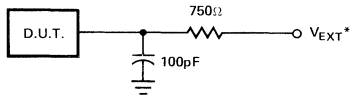
* V_{EXT} IS SET AT VARIOUS VOLTAGES DURING TESTING TO GUARANTEE THE SPECIFICATION.

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$; GND = 0V

BUS PARAMETERS:

READ:

SYMBOL	PARAMETER	8255A		8255A-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{AR}	Address Stable Before READ	0		0		ns
t_{RA}	Address Stable After READ	0		0		ns
t_{RR}	READ Pulse Width	300		300		ns
t_{RD}	Data Valid From READ[1]		250		200	ns
t_{DF}	Data Float After READ	10	150	10	100	ns
t_{RV}	Time Between READs and/or WRITEs	850		850		ns

WRITE:

SYMBOL	PARAMETER	8255A		8255A-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{AW}	Address Stable Before WRITE	0		0		ns
t_{WA}	Address Stable After WRITE	20		20		ns
t_{WW}	WRITE Pulse Width	400		300		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		100		ns
t_{WD}	Data Valid After WRITE	30		30		ns

OTHER TIMINGS:

SYMBOL	PARAMETER	8255A		8255A-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WB}	WR = 1 to Output[1]		350		350	ns
t_{IR}	Peripheral Data Before RD	0		0		ns
t_{HR}	Peripheral Data After RD	0		0		ns
t_{AK}	ACK Pulse Width	300		300		ns
t_{ST}	STB Pulse Width	500		500		ns
t_{PS}	Per. Data Before T.E. of STB	0		0		ns
t_{PH}	Per. Data After T.E. of STB	180		180		ns
t_{AD}	ACK = 0 to Output[1]		300		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	20	250	ns
t_{WOB}	WR = 1 to OBF = 0[1]		650		650	ns
t_{AOB}	ACK = 0 to OBF = 1[1]		350		350	ns
t_{SIB}	STB = 0 to IBF = 1[1]		300		300	ns
t_{RIB}	RD = 1 to IBF = 0[1]		300		300	ns
t_{RIT}	RD = 0 to INTR = 0[1]		400		400	ns
t_{SIT}	STB = 1 to INTR = 1[1]		300		300	ns
t_{AIT}	ACK = 1 to INTR = 1[1]		350		350	ns
t_{WIT}	WR = 0 to INTR = 0[1]		850		850	ns

Notes: 1. Test Conditions: 8255A: C_L = 100pF; 8255A-5: C_L = 150pF.
2. Period of Reset pulse must be at least 50µs during or after power on.
Subsequent Reset pulse can be 500 ns min.

2.4

2.0 — TEST POINTS — 2.0

0.45

0.8 — — 0.8

Input Waveforms For A.C. Tests

$\overline{RD}$

t_{RR}

INPUT

t_{IR}

t_{HR}

$\overline{CS}$, A1, A0

t_{AR}

t_{RA}

D_7-D_0

t_{RD}

t_{DF}

Mode 0 (Basic Input)

$\overline{WR}$

t_{WW}

D_7-D_0

t_{DW}

t_{WD}

$\overline{CS}$, A1, A0

t_{AW}

t_{WA}

OUTPUT

t_{WB}
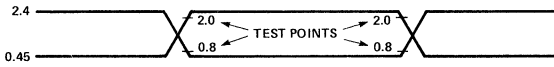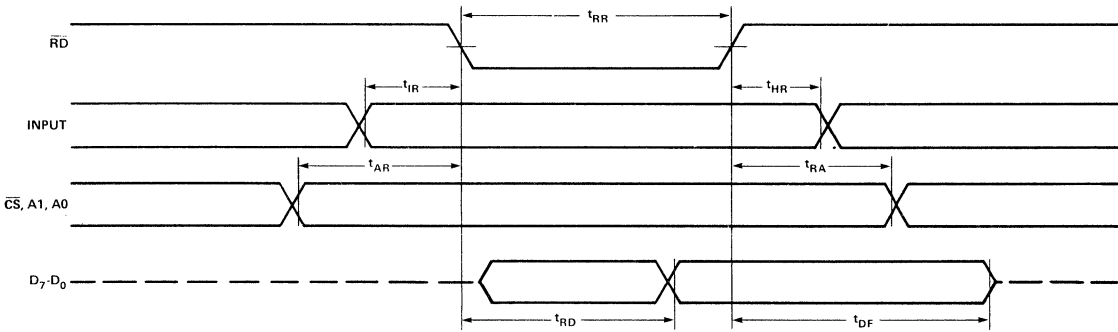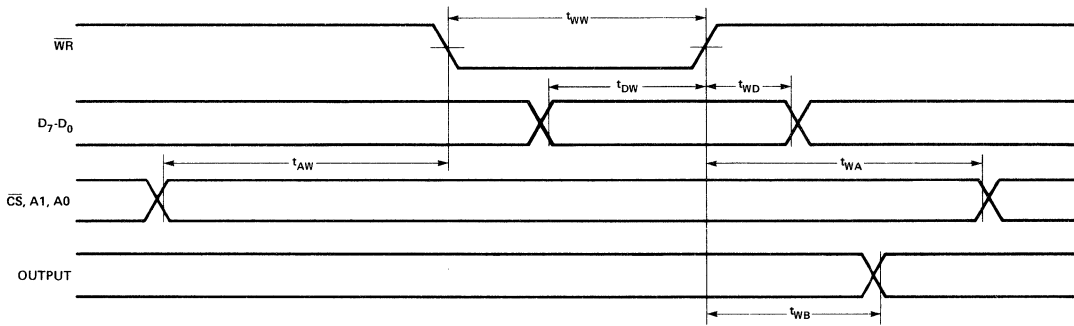
Mode 0 (Basic Output)
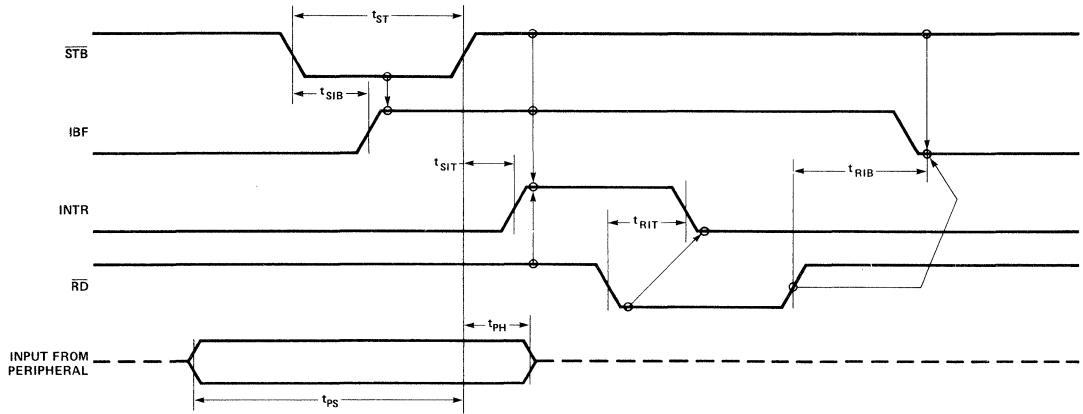
Mode 1 (Strobed Input)
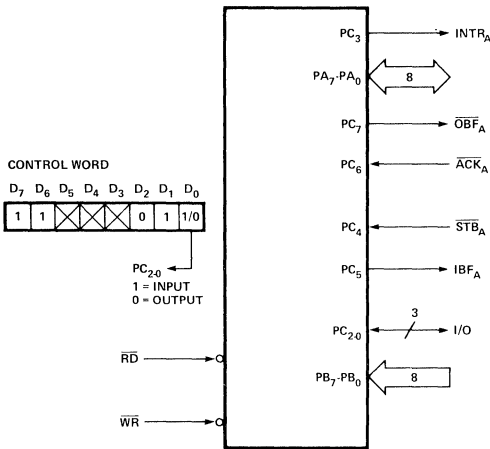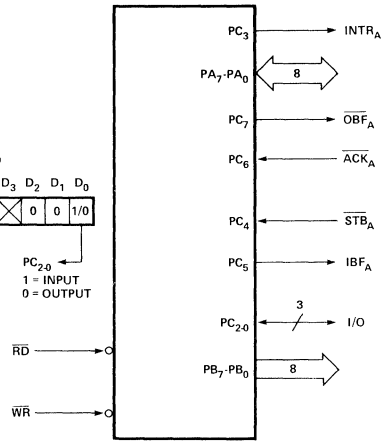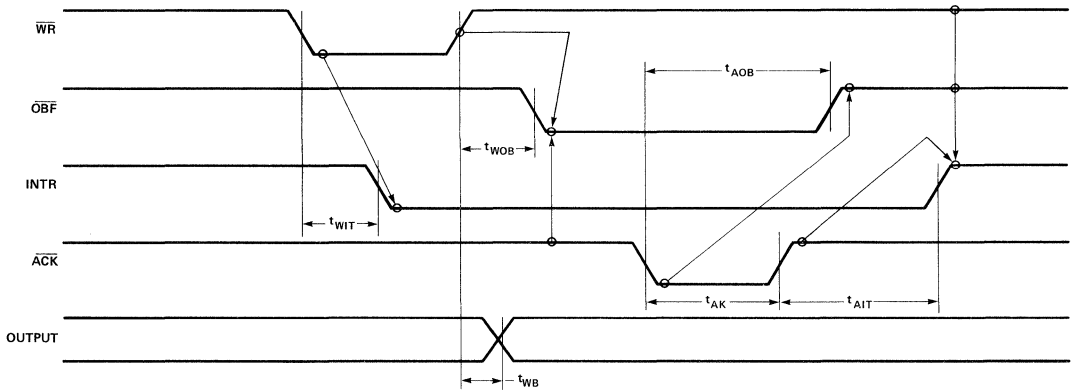
Mode 1 (Strobed Output)
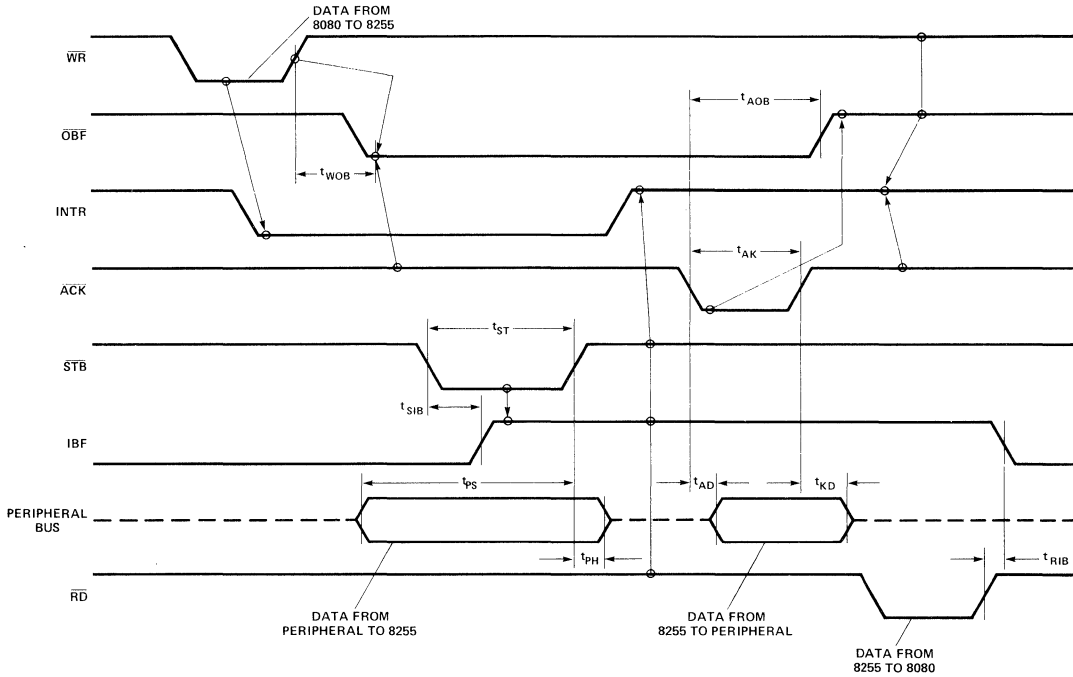
Mode 2 (Bi-directional)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF $\cdot$ $\overline{MASK}$ $\cdot$ $\overline{STB}$ $\cdot$ $\overline{RD}$ + $\overline{OBF}$ $\cdot$ $\overline{MASK}$ $\cdot$ $\overline{ACK}$ $\cdot$ $\overline{WR}$)

intel®

M8255A
PROGRAMMABLE PERIPHERAL INTERFACE

- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Fully Compatible with MCS™-80 Microprocessor Family**
- **Full Military Temperature Range -55°C to +125°C**

- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **40 Pin Dual In-Line Package**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**

The M8255A is a general purpose programmable I/O device designed for use with microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bi-directional Bus mode which uses 8 lines for a bi-directional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the M8255A include bit set and reset capability and the ability to source 1 mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

PIN CONFIGURATION

M8255A BLOCK DIAGRAM

PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . –55°C to +125°C
Storage Temperature . . . .–65°C to +150°C
Voltage On Any Pin
   With Respect to GND . . . . –0.5V to +7V
Power Dissipation . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS $T_A = -55°C$ to $+125°C; V_{CC} = +5V \pm 10\%; GND = 0V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	–.5		.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			.45	V	$I_{OL} = 1.7mA$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -50\mu A$ (–100μA for D.B. Port)
$I_{OH}^{[1]}$	Darlington Drive Current	1.0		4.0	mA	$V_{OH} = 1.5V$, $R_{EXT} = 750\Omega$
I_{CC}	Power Supply Current			120	mA	
I_{IL}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
$|I_{OFL}|$	Output Float Leakage			10	μA	$V_{OUT} = 0.45V/V_{CC}$

NOTE:
1. Available on 8 pins only.

A.C. CHARACTERISTICS $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%; GND = 0V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
t_{WP}	Pulse Width of $\overline{WR}$			400	ns	
t_{DW}	Time D.B. Stable Before $\overline{WR}$	50			ns	
t_{WD}	Time D.B. Stable After $\overline{WR}$	35			ns	
t_{AW}	Time Address Stable Before $\overline{WR}$	20			ns	
t_{WA}	Time Address Stable After $\overline{WR}$	20			ns	
t_{CW}	Time $\overline{CS}$ Stable Before $\overline{WR}$	20			ns	
t_{WC}	Time $\overline{CS}$ Stable After $\overline{WR}$	35			ns	
t_{WB}	Delay From $\overline{WR}$ To Output			500	ns	$C_L = 50pF$
t_{RP}	Pulse Width of $\overline{RD}$	405			ns	
t_{IR}	$\overline{RD}$ Set-Up Time	0			ns	
t_{HR}	Input Hold Time	0			ns	
t_{RD}	Delay From $\overline{RD} = 0$ To System Bus			295	ns	$C_L = 100pF$
t_{OD}	Delay From $\overline{RD} = 1$ To System Bus	10		150	ns	$C_L = 15pF/100pF$
t_{AR}	Time Address Stable Before $\overline{RD}$	50			ns	
t_{CR}	Time $\overline{CS}$ Stable Before $\overline{RD}$	50			ns	
t_{AK}	Width Of $\overline{ACK}$ Pulse	500			ns	
t_{ST}	Width Of $\overline{STB}$ Pulse	500			ns	
t_{PS}	Set-Up Time For Peripheral	60			ns	
t_{PH}	Hold Time For Peripheral	180			ns	
t_{RA}	Hold Time for A_1, A_0 After $\overline{RD} = 1$	0			ns	

A.C. CHARACTERISTICS (Continued)

t_{RC}	Hold Time For CS After $\overline{RD}$ = 1	0			ns	
t_{AD}	Time From $\overline{ACK}$ = 0 To Output (Mode 2)			400	ns	C_L = 50pF
t_{KD}	Time From $\overline{ACK}$ = 1 To Output Floating	20		300	ns	C_L = 15pF/50pF
t_{WO}	Time From $\overline{WR}$ = 1 To $\overline{OBF}$ = 0			700	ns	
t_{AO}	Time From $\overline{ACK}$ = 0 To $\overline{OBF}$ = 1			450	ns	C_L = 50pF
t_{SI}	Time From $\overline{STB}$ = 0 To IBF = 1			450	ns	
t_{RI}	Time From $\overline{RD}$ = 1 To IBF = 0			360	ns	

CAPACITANCE T_A = 25°C, V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

TEST LOAD CIRCUIT:
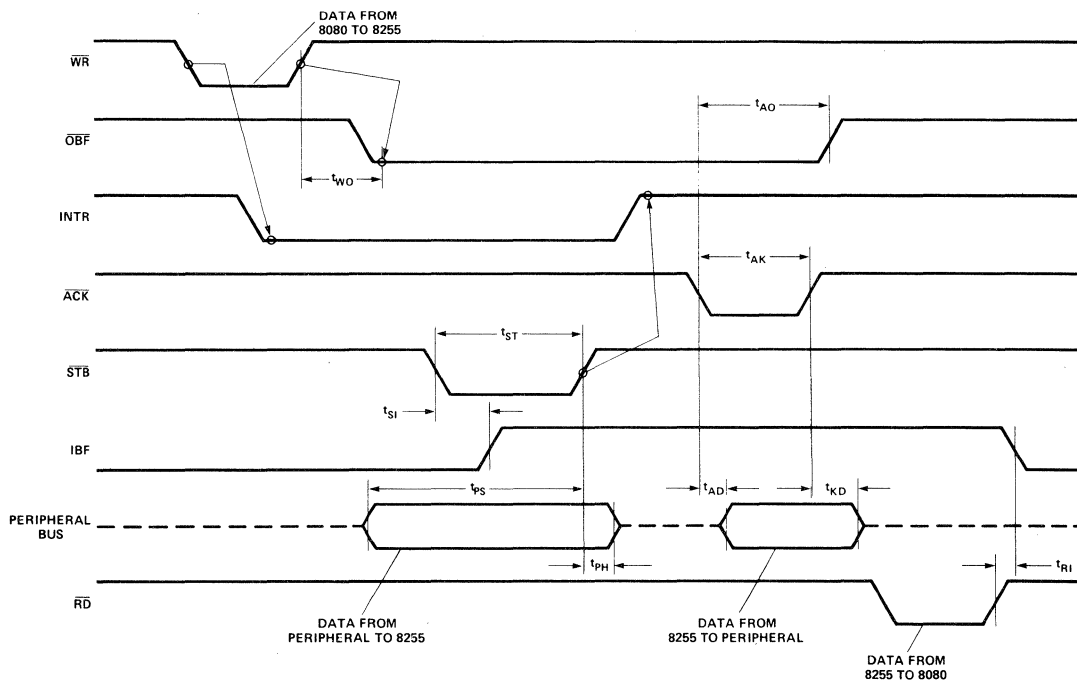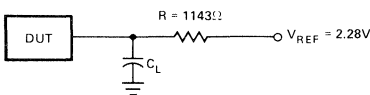
Mode 2 (Bi-directional)

intel®

8257, 8257-5
PROGRAMMABLE DMA CONTROLLER

- ■ **MCS-85™ Compatible 8257-5**
- ■ **Four Channel DMA Controller**
- ■ **Priority DMA Request Logic**
- ■ **Channel Inhibit Logic**
- ■ **Terminal Count and Modulo 128 Outputs**

- ■ **Auto Load Mode**
- ■ **Single TTL Clock**
- ■ **Single +5V Supply**
- ■ **Expandable**
- ■ **40 Pin Dual-In-Line Package**

The 8257 is a four-channel Direct Memory Access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel® Microcomputer Systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus is accomplished via the CPU's HOLD function. The 8257 has priority logic that resolves the peripherals requests and issues a composite HOLD request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers and expansion to other 8257 devices for systems that require more than four channels of DMA controlled transfer. The 8257 represents a significant savings in component count for DMA-based microcomputer systems and greatly simplifies the transfer of data at high speed between peripherals and memories.

PIN CONFIGURATION

$\overline{I/OR}$	1		40	A_7
$\overline{I/OW}$	2		39	A_6
$\overline{MEM\ R}$	3		38	A_5
$\overline{MEM\ W}$	4		37	A_4
MARK	5		36	TC
READY	6		35	A_3
HLDA	7		34	A_2
ADDSTB	8		33	A_1
AEN	9	8257	32	A_0
HRQ	10		31	V_{CC}
$\overline{CS}$	11		30	D_0
CLK	12		29	D_1
RESET	13		28	D_2
$\overline{DACK\ 2}$	14		27	D_3
$\overline{DACK\ 3}$	15		26	D_4
DRQ 3	16		25	$\overline{DACK\ 0}$
DRQ 2	17		24	$\overline{DACK\ 1}$
DRQ 1	18		23	D_5
DRQ 0	19		22	D_6
GND	20		21	D_7
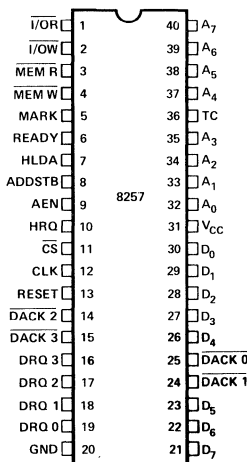
PIN NAMES

D_7-D_0	DATA BUS		AEN	ADDRESS ENABLE
A_7-A_0	ADDRESS BUS		ADSTB	ADDRESS STROBE
$\overline{I/OR}$	I/O READ		TC	TERMINAL COUNT
$\overline{I/OW}$	I/O WRITE		MARK	MODULO 128 MARK
$\overline{MEMR}$	MEMORY READ		DRQ_3-DRQ_0	DMA REQUEST INPUT
$\overline{MEMW}$	MEMORY WRITE		$\overline{DACK_3}$-$\overline{DACK_0}$	DMA ACKNOWLEDGE OUT
CLK	CLOCK INPUT			
RESET	RESET INPUT		$\overline{CS}$	CHIP SELECT
READY	READY		V_{CC}	+5 VOLTS
HRQ	HOLD REQUEST (TO 8080A)		GND	GROUND
HLDA	HOLD ACKNOWLEDGE (FROM 8080A)			

BLOCK DIAGRAM
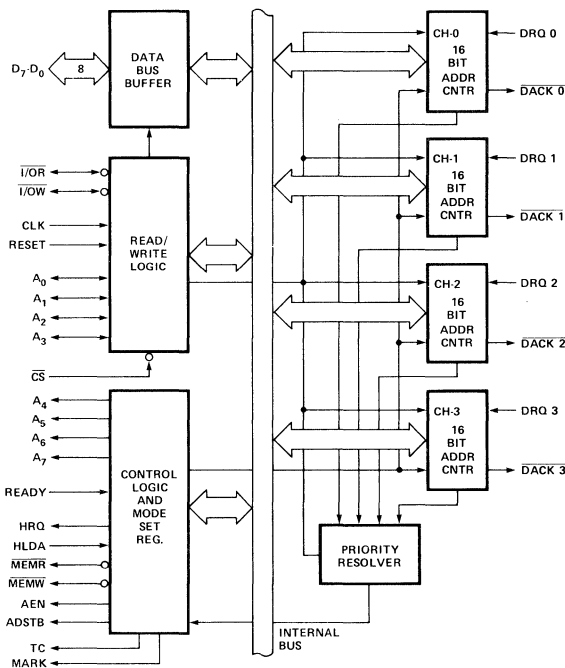
8257 BASIC FUNCTIONAL DESCRIPTION

General

The 8257 is a programmable, Direct Memory Access (DMA) device which, when coupled with a single Intel® 8212 I/O port device, provides a complete four-channel DMA controller for use in Intel® microcomputer systems. After being initialized by software, the 8257 can transfer a block of data, containing up to 16,384 bytes, between memory and a peripheral device directly, without further intervention required of the CPU. Upon receiving a DMA transfer request from an enabled peripheral, the 8257:
8257:

- Acquires control of the system bus.

- Acknowledges that requesting peripheral which is connected to the highest priority channel.

- Outputs the least significant eight bits of the memory address onto system address lines A_0-A_7, outputs the most significant eight bits of the memory address to the 8212 I/O port via the data bus (the 8212 places these address bits on lines A_8-A_{15}, and

- Generates the appropriate memory and I/O read/write control signals that cause the peripheral to receive or deposit a data byte directly from or to the addressed location in memory.

The 8257 will retain control of the system bus and repeat the transfer sequence, as long as a peripheral maintains its DMA request. Thus, the 8257 can transfer a block of data to/from a high speed peripheral (e.g., a sector of data on a floppy disk) in a single "burst". When the specified number of data bytes have been transferred, the 8257 activates its Terminal Count (TC) output, informing the CPU that the operation is complete.

The 8257 offers three different modes of operation: (1) DMA read, which causes data to be transferred from memory to a peripheral; (2) DMA write, which causes data to be transferred from a peripheral to memory; and (3) DMA verify, which does not actually involve the transfer of data. When an 8257 channel is in the DMA verify mode, it will respond the same as described for transfer operations, except that no memory or I/O read/write control signals will be generated, thus preventing the transfer of data. The 8257, however, will gain control of the system bus and will acknowledge the peripheral's DMA request for each DMA cycle. The peripheral can use these acknowledge signals to enable an internal access of each byte of a data block in order to execute some verification procedure, such as the accumulation of a CRC (Cyclic Redundancy Code) checkword. For example, a block of DMA verify cycles might follow a block of DMA read cycles (memory to peripheral) to allow the peripheral to verify its newly acquired data.

Block Diagram Description

1. DMA Channels

The 8257 provides four separate DMA channels (labeled CH-0 to CH-3). Each channel includes two sixteen-bit registers: (1) a DMA address register, and (2) a terminal count register. Both registers must be initialized before a channel is enabled. The DMA address register is loaded with the address of the first memory location to be accessed. The value loaded into the low-order 14-bits of the terminal count register specifies the number of DMA cycles minus one before the Terminal Count (TC) output is activated. For instance, a terminal count of 0 would cause the TC output to be active in the first DMA cycle for that channel. In general, if N = the number of desired DMA cycles, load the value N-1 into the low-order 14-bits of the terminal count register. The most significant two bits of the terminal count register specify the type of DMA operation for that channel:
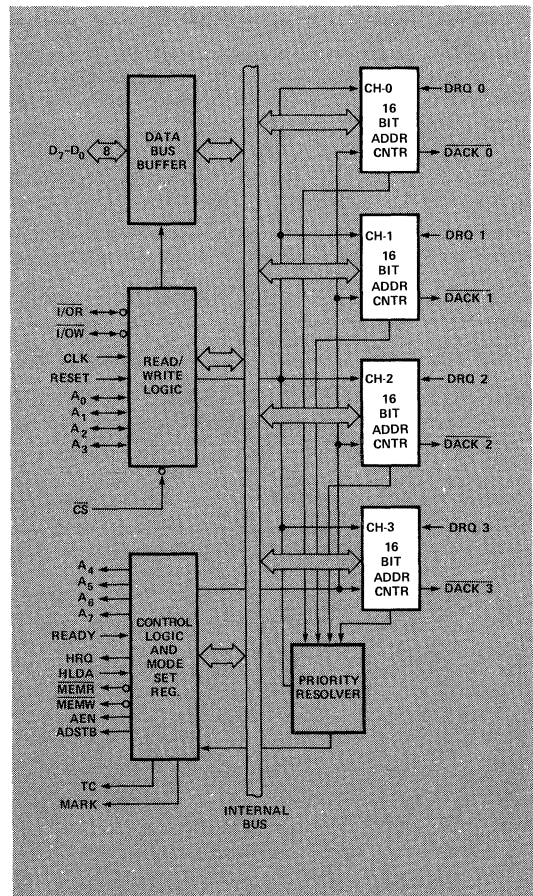
8257 BLOCK DIAGRAM

These two bits are not modified during a DMA cycle, but can be changed between DMA blocks.

Each channel accepts a DMA Request (DRQn) input and provides a DMA Acknowledge (DACKn) output:

(DRQ 0 - DRQ 3)

DMA Request: These are individual asynchronous channel request inputs used by the peripherals to obtain a DMA cycle. If not in the rotating priority mode then DRQ 0 has the highest priority and DRQ 3 has the lowest. A request can be generated by raising the request line and holding it high until DMA acknowledge. For multiple DMA cycles (Burst Mode) the request line is held high until the DMA acknowledge of the last cycle arrives.

(DACK 0 - DACK 3)

DMA Acknowledge: An active low level on the acknowledge output informs the peripheral connected to that channel that it has been selected for a DMA cycle.

BIT 15	BIT 14	TYPE OF DMA OPERATION
0	0	Verify DMA Cycle
0	1	Write DMA Cycle
1	0	Read DMA Cycle
1	1	(Illegal)

2. Data Bus Buffer

This three-state, bi-directional, eight bit buffer interfaces the 8257 to the system data bus:

(D$_0$-D$_7$)

Data Bus Lines: These are bi-directional three-state lines. When the 8257 is being programmed by the CPU, eight-bits of data for a DMA address register, a terminal count register or the Mode Set register are received on the data bus. When the CPU reads a DMA address register, a terminal count register or the Status register, the data is sent to the CPU over the data bus. During DMA cycles (when the 8257 is the bus master), the 8257 will output the most significant eight-bits of the memory address (from one of the DMA address registers) to the 8212 latch via the data bus. These address bits will be transferred at the beginning of the DMA cycle; the bus will then be released to handle the memory data transfer during the balance of the DMA cycle.
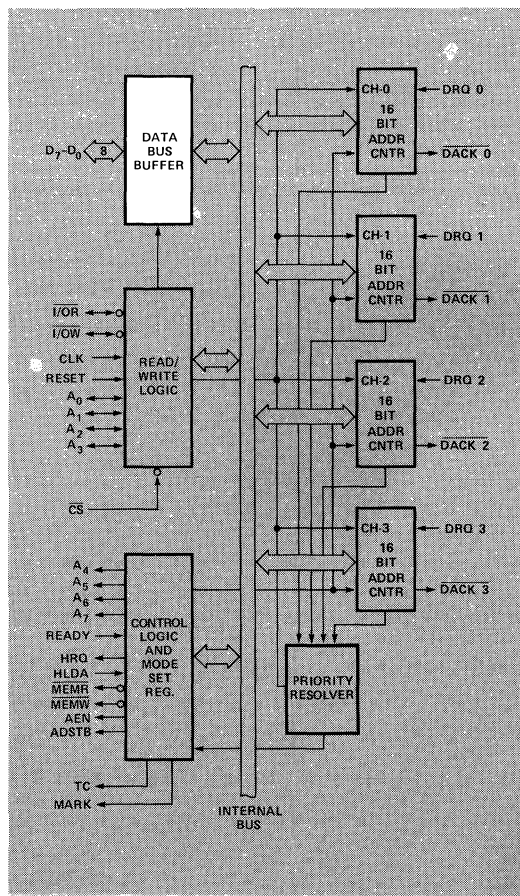
8257 BLOCK DIAGRAM

3. Read/Write Logic

When the CPU is programming or reading one of the 8257's register (i.e., when the 8257 is a "slave" device on the system bus), the Read/Write Logic accepts the I/O Read ($\overline{I/OR}$) or I/O Write ($\overline{I/OW}$) signal, decodes the least significant four address bits, (A_0-A_3), and either writes the contents of the data bus into the addressed register (if $\overline{I/OW}$ is true) or places the contents of the addressed register onto the data bus (if $\overline{I/OR}$ is true).

During DMA cycles (i.e., when the 8257 is the bus "master"), the Read/Write Logic generates the I/O read and memory write (DMA write cycle) or I/O Write and memory read (DMA read cycle) signals which control the data link with the peripheral that has been granted the DMA cycle.

Note that during DMA transfers Non-DMA I/O devices should be de-selected (disabled) using "AEN" signal to inhibit I/O device decoding of the memory address as an erroneous device address.

($\overline{I/OR}$)

I/O Read: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the 8-bit status register or the upper/lower byte of a 16-bit DMA address register or terminal count register to be read. In the "master" mode, $\overline{I/OR}$ is a control output which is used to access data from a peripheral during the DMA write cycle.

($\overline{I/OW}$)

I/O Write: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the contents of the data bus to be loaded into the 8-bit mode set register or the upper/lower byte of a 16-bit DMA address register or terminal count register. In the "master" mode, $\overline{I/OW}$ is a control output which allows data to be output to a peripheral during a DMA read cycle.

(CLK)

Clock Input: Generally from an Intel® 8224 Clock Generator device. (ϕ2 TTL)

(RESET)

Reset: An asynchronous input (generally from an 8224 device) which clears all registers and control lines.

(A_0-A_3)

Address Lines: These least significant four address lines are bi-directional. In the "slave" mode they are inputs which select one of the registers to be read or programmed. In the "master" mode, they are outputs which constitute the least significant four bits of the 16-bit memory address generated by the 8257.

($\overline{CS}$)

Chip Select: An active-low input which enables the I/O Read or I/O Write input when the 8257 is being read or programmed in the "slave" mode. In the "master" mode, $\overline{CS}$ is automatically disabled to prevent the chip from selecting itself while performing the DMA function.
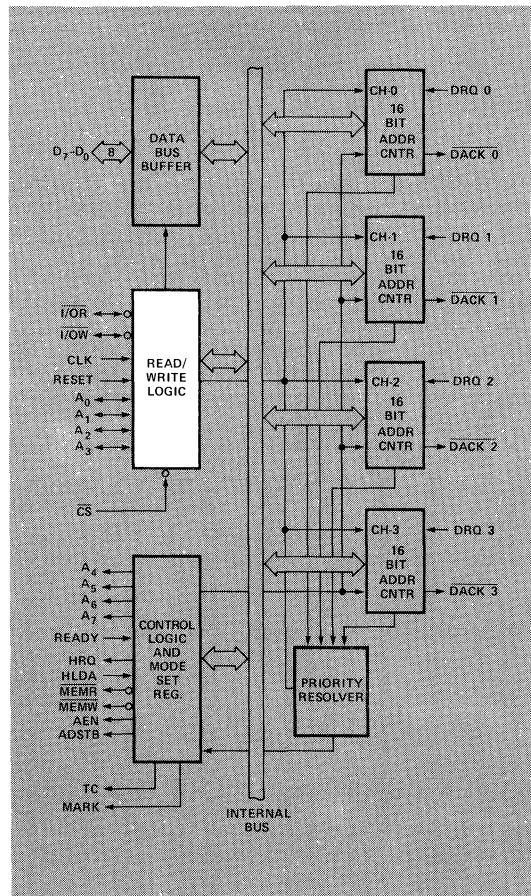
8257 BLOCK DIAGRAM

4. Control Logic

This block controls the sequence of operations during all DMA cycles by generating the appropriate control signals and the 16-bit address that specifies the memory location to be accessed.

(A_4-A_7)

Address Lines: These four address lines are three-state outputs which constitute bits 4 through 7 of the 16-bit memory address generated by the 8257 during all DMA cycles.

(READY)

Ready: This asynchronous input is used to elongate the memory read and write cycles in the 8257 with wait states if the selected memory requires longer cycles.

(HRQ)

Hold Request: This output requests control of the system bus. In systems with only one 8257, HRQ will normally be applied to the HOLD input on the CPU.

(HLDA)

Hold Acknowledge: This input from the CPU indicates that the 8257 has acquired control of the system bus.

($\overline{\text{MEMR}}$)

Memory Read: This active-low three-state output is used to read data from the addressed memory location during DMA Read cycles.

($\overline{\text{MEMW}}$)

Memory Write: This active-low three-state output is used to write data into the addressed memory location during DMA Write cycles.

(ADSTB)

Address Strobe: This output strobes the most significant byte of the memory address into the 8212 device from the data bus.

(AEN)

Address Enable: This output is used to disable (float) the System Data Bus and the System Control Bus. It may also be used to disable (float) the System Address Bus by use of an enable on the Address Bus drivers in systems to inhibit non-DMA devices from responding during DMA cycles. It may be further used to isolate the 8257 data bus from the System Data Bus to facilitate the transfer of the 8 most significant DMA address bits over the 8257 data I/O pins without subjecting the System Data Bus to any timing constraints for the transfer. When the 8257 is used in an I/O device structure (as opposed to memory mapped), this AEN output should be used to disable the selection of an I/O device when the DMA address is on the address bus. The I/O device selection should be determined by the DMA acknowledge outputs for the 4 channels.

(TC)

Terminal Count: This output notifies the currently selected peripheral that the present DMA cycle should be the last cycle for this data block. If the TC STOP bit in the Mode Set register is set, the selected channel will be automatically disabled at the end of that DMA cycle. TC is activated when the 14-bit value in the selected channel's terminal count register equals zero. Recall that the low-order 14-bits of the terminal count register should be loaded with the values (n-1), where n = the desired number of the DMA cycles.

(MARK)

Modulo 128 Mark: This output notifies the selected peripheral that the current DMA cycle is the 128th cycle since the previous MARK output. MARK always occurs at 128 (and all multiples of 128) cycles from the end of the data block. Only if the total number of DMA cycles (n) is evenly divisable by 128 (and the terminal count register was loaded with n-1), will MARK occur at 128 (and each succeeding multiple of 128) cycles from the beginning of the data block.
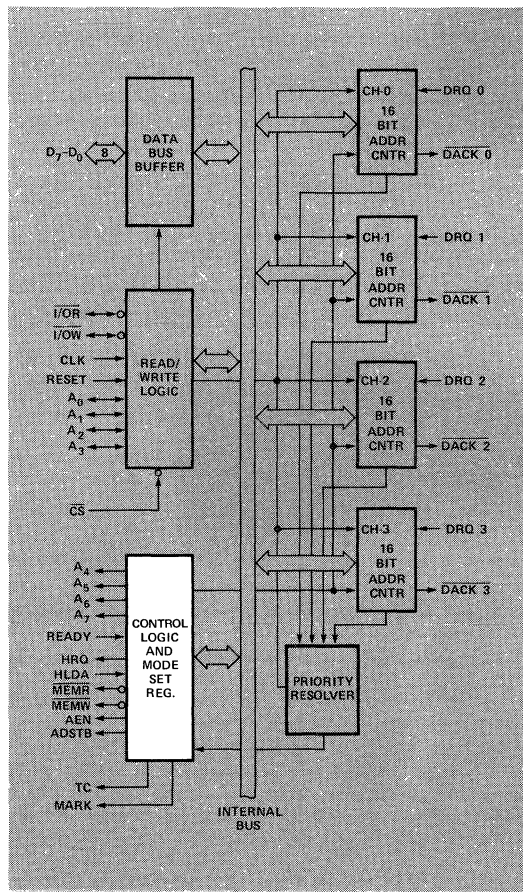
8257 BLOCK DIAGRAM

5. Mode Set Register

When set, the various bits in the Mode Set register enable each of the four DMA channels, and allow four different options for the 8257:
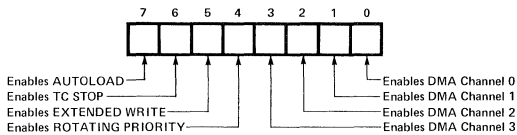
The Mode Set register is normally programmed by the CPU after the DMA address register(s) and terminal count register(s) are initialized. The Mode Set Register is cleared by the RESET input, thus disabling all options, inhibiting all channels, and preventing bus conflicts on power-up. A channel should not be left enabled unless its DMA address and terminal count registers contain valid values; otherwise, an inadvertent DMA request (DRQn) from a peripheral could initiate a DMA cycle that would destroy memory data.

The various options which can be enabled by bits in the Mode Set register are explained below:

Rotating Priority Bit 4

In the Rotating Priority Mode, the priority of the channels has a circular sequence. After each DMA cycle, the priority of each channel changes. The channel which had just been serviced will have the lowest priority.
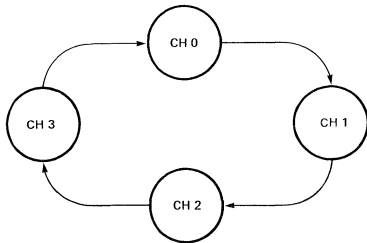
If the ROTATING PRIORITY bit is not set (set to a zero), each DMA channel has a fixed priority. In the fixed priority mode, Channel 0 has the highest priority and Channel 3 has the lowest priority. If the ROTATING PRIORITY bit is set to a one, the priority of each channel changes after each DMA cycle (not each DMA request). Each channel moves up to the next highest priority assignment, while the channel which has just been serviced moves to the lowest priority assignment:

	CHANNEL→ JUST SERVICED	CH-0	CH-1	CH-2	CH-3
Priority → Assignments	Highest ↕ Lowest	CH-1 CH-2 CH-3 CH-0	CH-2 CH-3 CH-0 CH-1	CH-3 CH-0 CH-1 CH-2	CH-0 CH-1 CH-2 CH-3

Note that rotating priority will prevent any one channel from monopolizing the DMA mode; consecutive DMA cycles will service different channels if more than one channel is enabled and requesting service. All DMA operations began with Channel 0 initially assigned to the highest priority for the first DMA cycle.

Extended Write Bit 5

If the EXTENDED WRITE bit is set, the duration of both the $\overline{MEMW}$ and $\overline{I/OW}$ signals is extended by activating them earlier in the DMA cycle. Data transfers within microcomputer systems proceed asynchronously to allow use of various types of memory and I/O devices with different access times. If a device cannot be accessed within a specific amount of time it returns a "not ready" indication to the 8257 that causes the 8257 to insert one or more wait states in its internal sequencing. Some devices are fast enough to be accessed without the use of wait states, but if they generate their READY response with the leading edge of the $\overline{I/OW}$ or $\overline{MEMW}$ signal (which generally occurs late in the transfer sequence), they would normally cause the 8257 to enter a wait state because it does not receive READY in time. For systems with these types of devices, the Extended Write option provides alternative timing for the I/O and memory write signals which allows the devices to return an early READY and prevents the unnecessary occurrence of wait states in the 8257, thus increasing system throughput.

TC Stop Bit 6

If the TC STOP bit is set, a channel is disabled (i.e., its enable bit is reset) after the Terminal Count (TC) output goes true, thus automatically preventing further DMA operation on that channel. The enable bit for that channel must be re-programmed to continue or begin another DMA operation. If the TC STOP bit is not set, the occurrence of the TC output has no effect on the channel enable bits. In this case, it is generally the responsibility of the peripheral to cease DMA requests in order to terminate a DMA operation.

Auto Load Bit 7

The Auto Load mode permits Channel 2 to be used for repeat block or block chaining operations, without immediate software intervention between blocks. Channel 2 registers are initialized as usual for the first data block; Channel 3 registers, however, are used to store the block re-initialization parameters (DMA starting address, terminal count and DMA transfer mode). After the first block of DMA cycles is executed by Channel 2 (i.e., after the TC output goes true), the parameters stored in the Channel 3 registers are transferred to Channel 2 during an "update" cycle. Note that the TC STOP feature, described above, has no effect on Channel 2 when the Auto Load bit is set.

If the Auto Load bit is set, the initial parameters for Channel 2 are automatically duplicated in the Channel 3 registers when Channel 2 is programmed. This permits repeat block operations to be set up with the programming of a single channel. Repeat block operations can be used in applications such as CRT refreshing. Channels 2 and 3 can still be loaded with separate values if Channel 2 is loaded before loading Channel 3. Note that in the Auto Load mode, Channel 3 is still available to the user if the Channel 3 enable bit is set, but use of this channel will change the values to be auto loaded into Channel 2 at update time. All that is necessary to use the Auto Load feature for chaining operations is to reload Channel 3 registers at the conclusion of each update cycle with the new parameters for the next data block transfer.

Each time that the 8257 enters an update cycle, the update flag in the status register is set and parameters in Channel 3 are transferred to Channel 2, non-destructively for Channel 3. The actual re-initialization of Channel 2 occurs at the beginning of the next channel 2 DMA cycle after the TC cycle. This will be the first DMA cycle of the new data block for Channel 2. The update flag is cleared at the conclusion of this DMA cycle. For chaining operations, the update flag in the status register can be monitored by the CPU to determine when the re-initialization process has been completed so that the next block parameters can be safely loaded into Channel 3.

6. Status Register

The eight-bit status register indicates which channels have reached a terminal count condition and includes the update flag described previously.
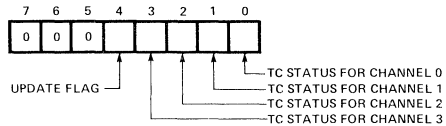
The TC status bits are set when the Terminal Count (TC) output is activated for that channel. These bits remain set until the status register is read or the 8257 is reset. The UPDATE FLAG, however, is not affected by a status register read operation. The UPDATE FLAG can be cleared by resetting the 8257, by changing to the non-auto load mode (i.e., by resetting the AUTO LOAD bit in the Mode Set register) or it can be left to clear itself at the completion of the update cycle. The purpose of the UPDATE FLAG is to prevent the CPU from inadvertently skipping a data block by overwriting a starting address or terminal count in the Channel 3 registers before those parameters are properly auto-loaded into Channel 2.
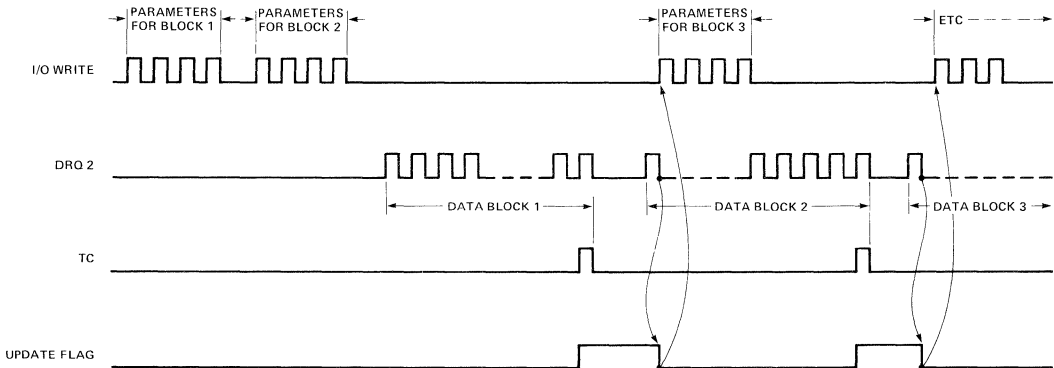
AUTOLOAD TIMING

8257 DETAILED OPERATIONAL SUMMARY

Programming and Reading the 8257 Registers

There are four pairs of "channel registers": each pair consisting of a 16-bit DMA address register and a 16-bit terminal count register (one pair for each channel). The 8257 also includes two "general registers": one 8-bit Mode Set register and one 8-bit Status register. The registers are loaded or read when the CPU executes a write or read instruction that addresses the 8257 device and the appropriate register within the 8257. The 8228 generates the appropriate read or write control signal (generally I/OR or I/OW while the CPU places a 16-bit address on the system address bus, and either outputs the data to be written onto the system data bus or accepts the data being read from the data bus. All or some of the most significant 12 address bits A_4-A_{15} (depending on the systems memory, I/O configuration) are usually decoded to produce the chip select ($\overline{CS}$) input to the 8257. An I/O Write input (or Memory Write in memory mapped I/O configurations, described below) specifies that the addressed register is to be programmed, while an I/O Read input (or Memory Read) specifies that the addressed register is to be read. Address bit 3 specifies whether a "channel register" ($A_3 = 0$) or the Mode Set (program only)/Status (read only) register ($A_3 = 1$) is to be accessed.

The least significant three address bits, A_0-A_2, indicate the specific register to be accessed. When accessing the Mode Set or Status register, A_0-A_2 are all zero. When accessing a channel register bit A_0 differentiates between the DMA address register ($A_0 = 0$) and the terminal count register ($A_0 = 1$), while bits A_1 and A_2 specify one of the

CONTROL INPUT	$\overline{CS}$	$\overline{I/OW}$	$\overline{I/OR}$	A3
Program Half of a Channel Register	0	0	1	0
Read Half of a Channel Register	0	1	0	0
Program Mode Set Register	0	0	1	1
Read Status Register	0	1	0	1

four channels. Because the "channel registers" are 16-bits, two program instruction cycles are required to load or read an entire register. The 8257 contains a first/last (F/L) flip flop which toggles at the completion of each channel program or read operation. The F/L flip flop determines whether the upper or lower byte of the register is to be accessed. The F/L flip flop is reset by the RESET input and whenever the Mode Set register is loaded. To maintain proper synchronization when accessing the "channel registers" all channel command instruction operations should occur in pairs, with the lower byte of a register always being accessed first. Do not allow $\overline{CS}$ to clock while either $\overline{I/OR}$ or $\overline{I/OW}$ is active, as this will cause an erroneous F/L flip flop state. In systems utilizing an interrupt structure, interrupts should be disabled prior to any paired programming operations to prevent an interrupt from splitting them. The result of such a split would leave the F/L F/F in the wrong state. This problem is particularly obvious when other DMA channels are programmed by an interrupt structure.

8257 REGISTER SELECTION

REGISTER	BYTE	ADDRESS INPUTS				F/L	*BI-DIRECTIONAL DATA BUS							
		A_3	A_2	A_1	A_0		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CH-0 DMA Address	LSB	0	0	0	0	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
	MSB	0	0	0	0	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
CH-0 Terminal Count	LSB	0	0	0	1	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
	MSB	0	0	0	1	1	Rd	Wr	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8
CH-1 DMA Address	LSB	0	0	1	0	0	Same as Channel 0							
	MSB	0	0	1	0	1								
CH-1 Terminal Count	LSB	0	0	1	1	0								
	MSB	0	0	1	1	1								
CH-2 DMA Address	LSB	0	1	0	0	0	Same as Channel 0							
	MSB	0	1	0	0	1								
CH-2 Terminal Count	LSB	0	1	0	1	0								
	MSB	0	1	0	1	1								
CH-3 DMA Address	LSB	0	1	1	0	0	Same as Channel 0							
	MSB	0	1	1	0	1								
CH-3 Terminal Count	LSB	0	1	1	1	0								
	MSB	0	1	1	1	1								
MODE SET (Program only)	—	1	0	0	0	0	AL	TCS	EW	RP	EN3	EN2	EN1	EN0
STATUS (Read only)	—	1	0	0	0	0	0	0	0	UP	TC3	TC2	TC1	TC0

*A_0-A_{15}: DMA Starting Address, C_0-C_{13}: Terminal Count value (N-1), Rd and Wr: DMA Verify (00), Write (01) or Read (10) cycle selection, AL: Auto Load, TCS: TC STOP, EW: EXTENDED WRITE, RP: ROTATING PRIORITY, EN3-EN0: CHANNEL ENABLE MASK, UP: UPDATE FLAG, TC3-TC0: TERMINAL COUNT STATUS BITS.

DMA Operation

Internal 8257 operations may proceed through seven different states. The duration of a state is defined by the clock input. When the 8257 is not executing a DMA cycle, it is in the idle state, S_I. A DMA cycle begins when one or more DMA Request (DRQn) lines become active. The 8257 then enters state S_0, sends a Hold Request (HRQ) to the CPU and waits for as many S_0 states as are necessary for the CPU to return a Hold Acknowledge (HLDA). For each S_0 state, the DMA Request lines are again sampled and DMA priority is resolved (according to the fixed or rotating priority scheme). When HLDA is received, the DMA Acknowledge ($\overline{DACKn}$) line for the highest priority requesting channel is activated, thus selecting that channel and its peripheral for the DMA cycle. The 8257 then proceeds to state S_1. Note that the DMA Request (DRQn) input should remain high until either $\overline{DACKn}$ is received for a single DMA cycle service, or until both the $\overline{DACKn}$ and TC outputs are received when transferring an entire data block in a "burst" mode. If the 8257 should lose control of the system bus (i.e., if HLDA goes false), the DMA Acknowledge will be removed after the current DMA cycle is completed and no more DMA cycles will occur until the 8257 again acquires control of the system bus.

Each DMA cycle will consist of at least four internal states: S_1, S_2, S_3, and S_4. If the access time for the memory or I/O devices involved is not fast enough to return the required READY response and complete a byte transfer within the specified amount of time, one or more wait states (SW) are inserted between states S_3 and S_4. Recall that in certain cases the Extended Write option can eliminate the need for a wait state. Note that a READY response is not required during DMA verify cycles. Specified minimum/maximum values for READY setup time (t_{RS}), write data setup time (t_{DW}), read data access time (t_{RD}) and HLDA setup time (t_{QS}) are listed under A.C. CHARACTERISTICS and are illustrated in the accompanying timing diagrams.

During DMA write cycles, the I/O Read ($\overline{I/OR}$) output is generated at the beginning of state S_2 and the Memory Write ($\overline{MEMW}$) output is generated at the beginning of S_3. During DMA read cycles, the Memory Read ($\overline{MEMR}$) output is generated at the beginning of state S_2 and the I/O Write (I/OW) output goes true at the beginning of of state S_3. Recall that no read or write control signals are generated during DMA verify cycles. Extended $\overline{WR}$ for MEM and I/O will be generated in S_2.

DMA OPERATION STATE DIAGRAM

Memory Mapped I/O Configurations

The 8257 can be connected to the system bus as a memory device instead of as an I/O device for memory mapped I/O configurations by connecting the system memory control lines to the 8257's I/O control lines and the system I/O control lines to the 8257's memory control lines.

This configuration permits use of the 8080's considerably larger repertoire of memory instructions when reading or loading the 8257's registers. Note that with this connection, the programming of the Read (bit 15) and Write (bit 14) bits in the terminal count register will have a different meaning:
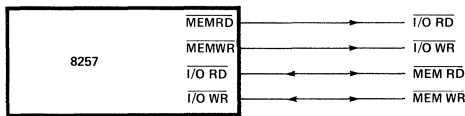
SYSTEM INTERFACE FOR MEMORY MAPPED I/O

BIT 15 READ	BIT 14 WRITE	
0	0	DMA Verify Cycle
0	1	DMA Read Cycle
1	0	DMA Write Cycle
1	1	Illegal

TC REGISTER FOR MEMORY MAPPED I/O ONLY

DETAILED SYSTEM INTERFACE SCHEMATIC
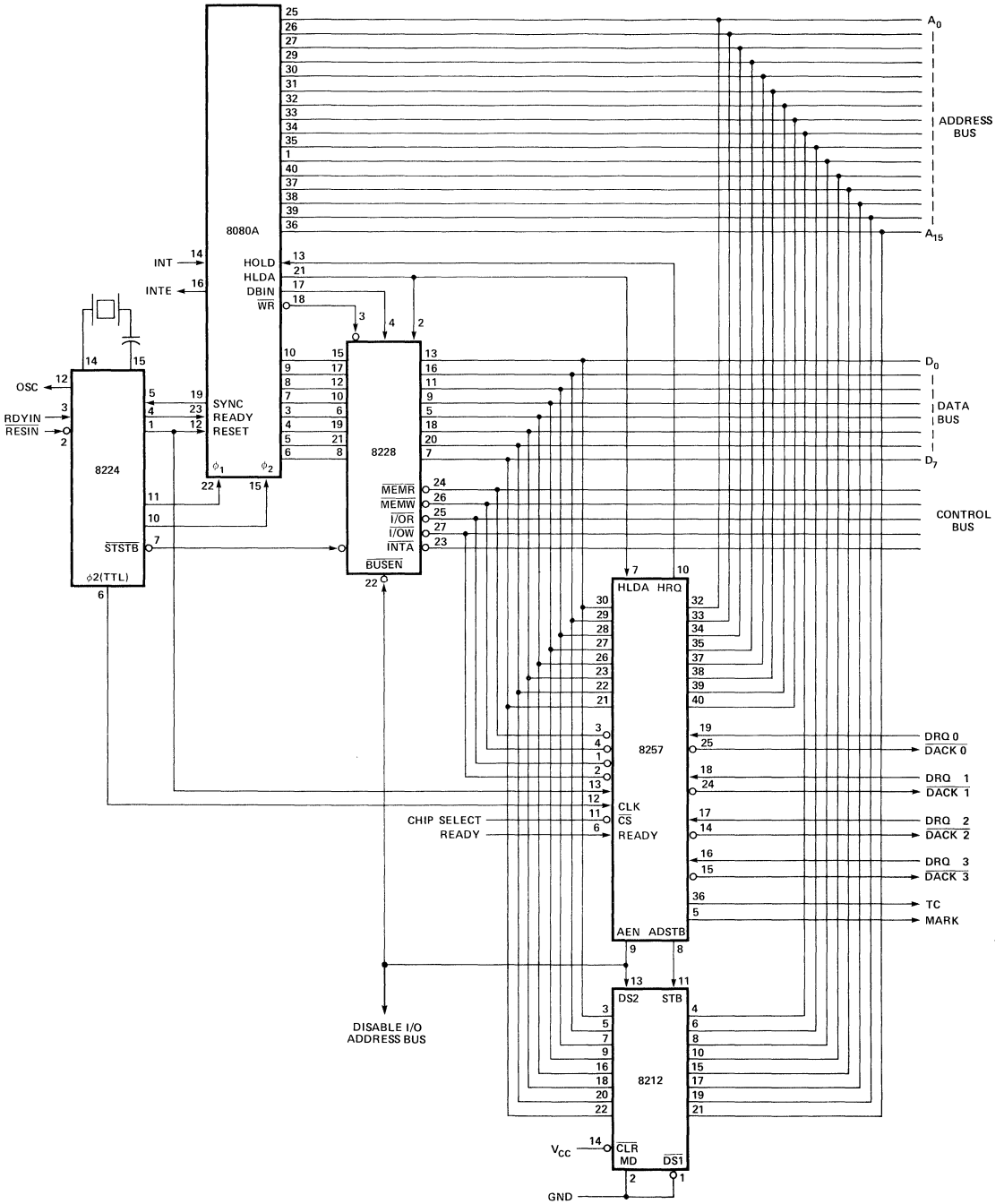
DETAILED SYSTEM INTERFACE SCHEMATIC
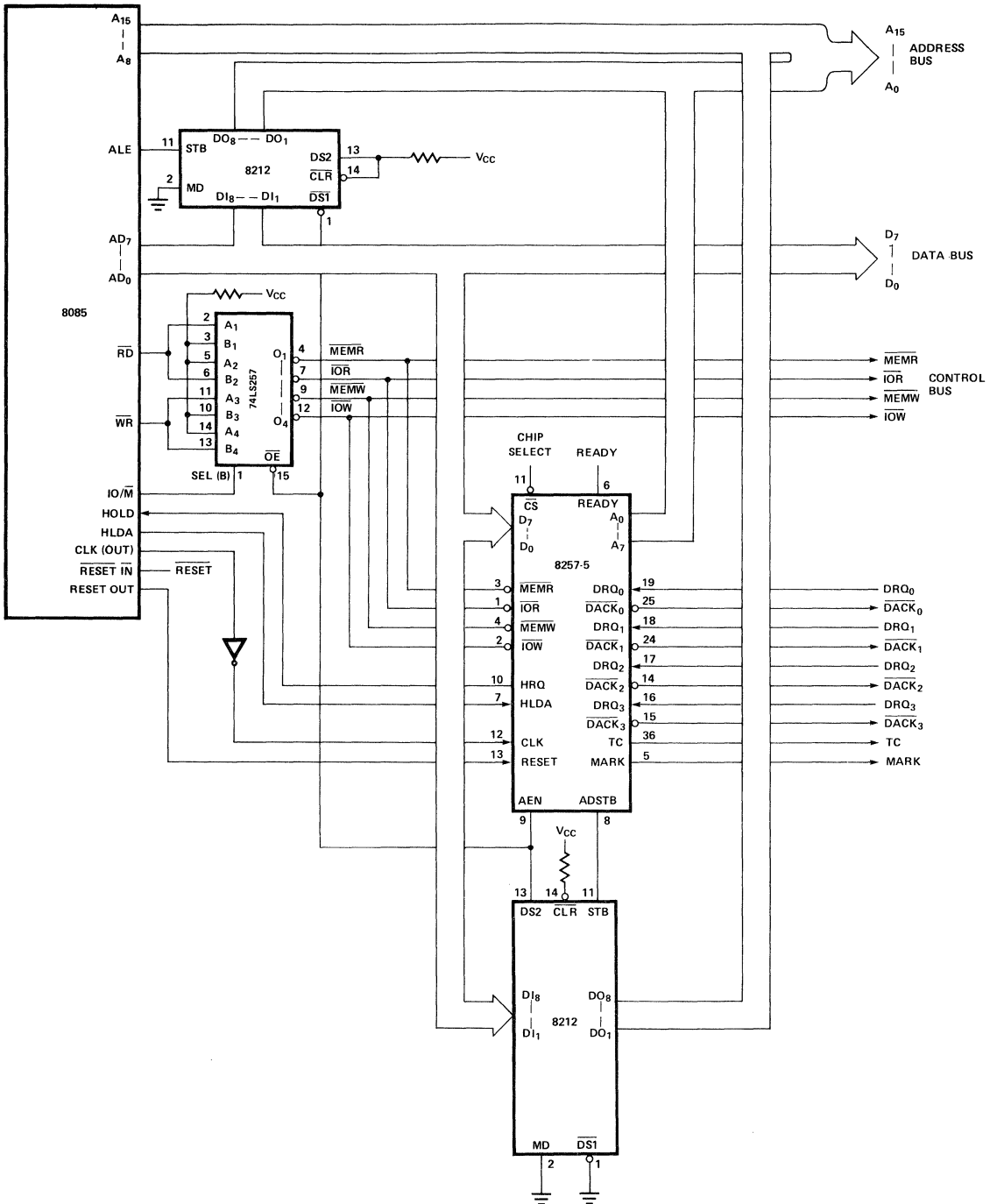
SYSTEM APPLICATION EXAMPLES

ADDRESS BUS

CONTROL BUS

I/OW   I/OR

DATA BUS

| 8257 AND 8212 | | DISK 1 | SYSTEM RAM MEMORY |

DRQ 0
DACK 0
DRQ 1
DACK 1
DRQ 2
DACK 2
DRQ 3
DACK 3

DISK 1
DISK 2
DISK 3
DISK 4

8257 AND 8212

DMA CONTROLLER

SYSTEM RAM MEMORY
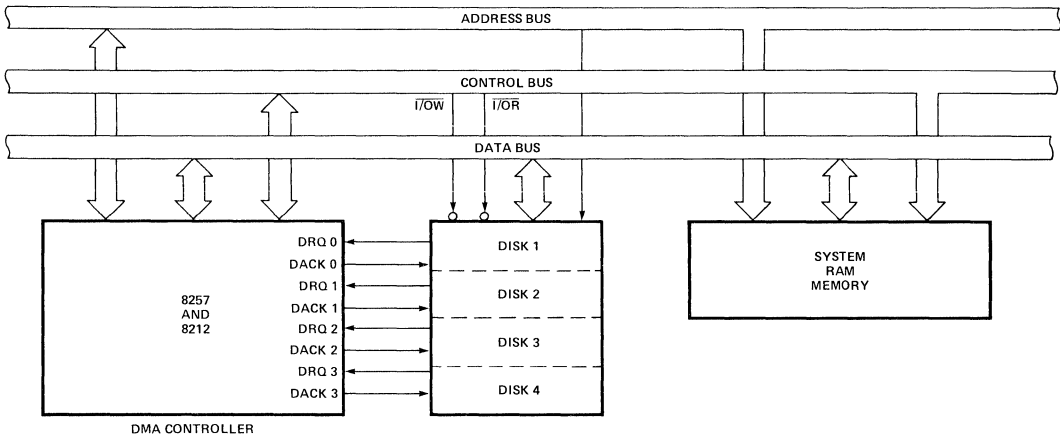
FLOPPY DISK CONTROLLER (4 DRIVES)

ADDRESS BUS

CONTROL BUS

DATA BUS

8257 AND 8212

DRQ
DACK

8251 USART

SYSTEM RAM MEMORY

MODEM

TELEPHONE LINES
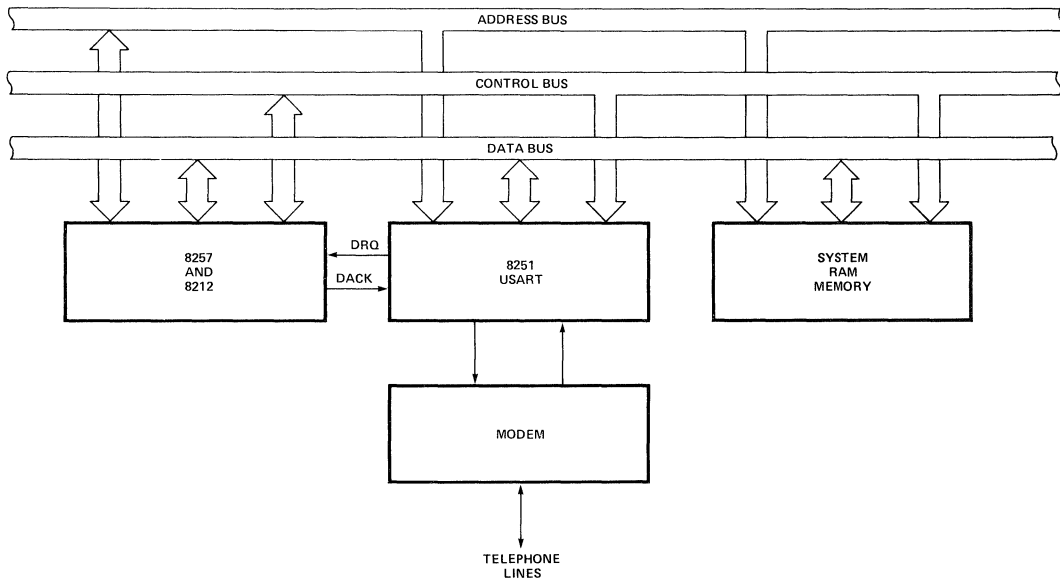
HIGH-SPEED COMMUNICATION CONTROLLER

DMA MODE WAVEFORMS
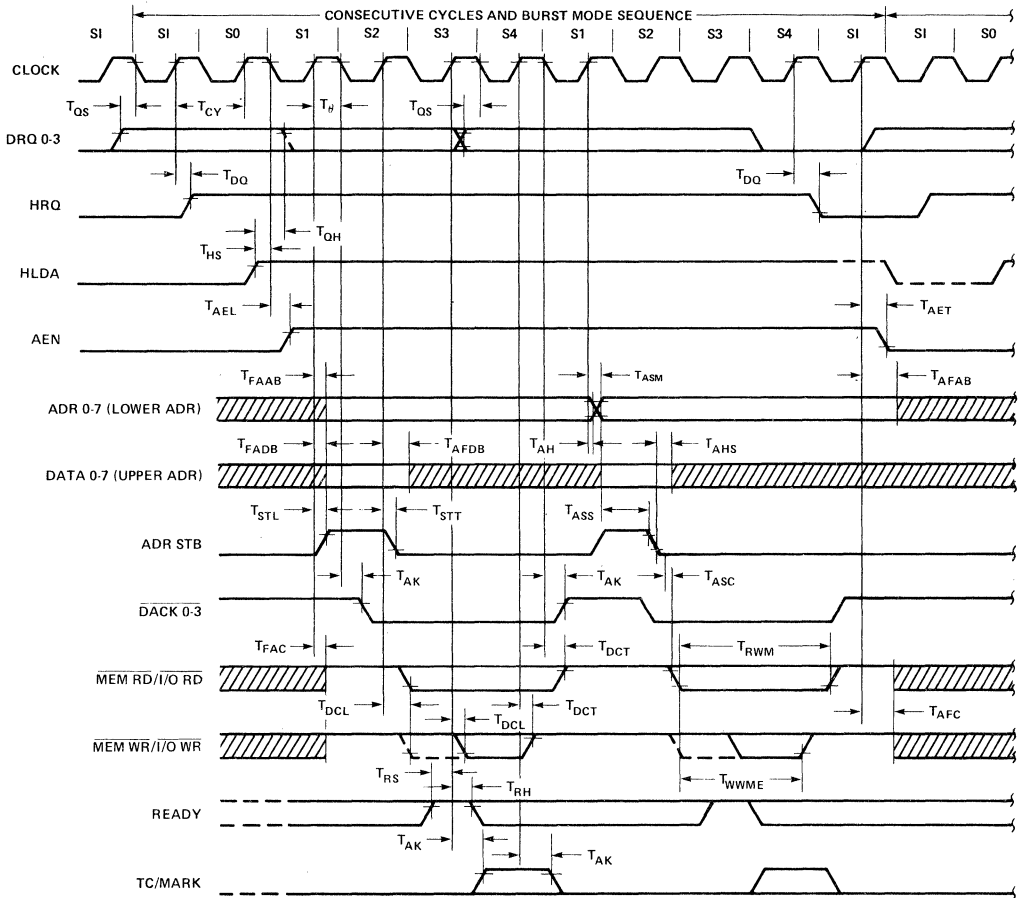
PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.
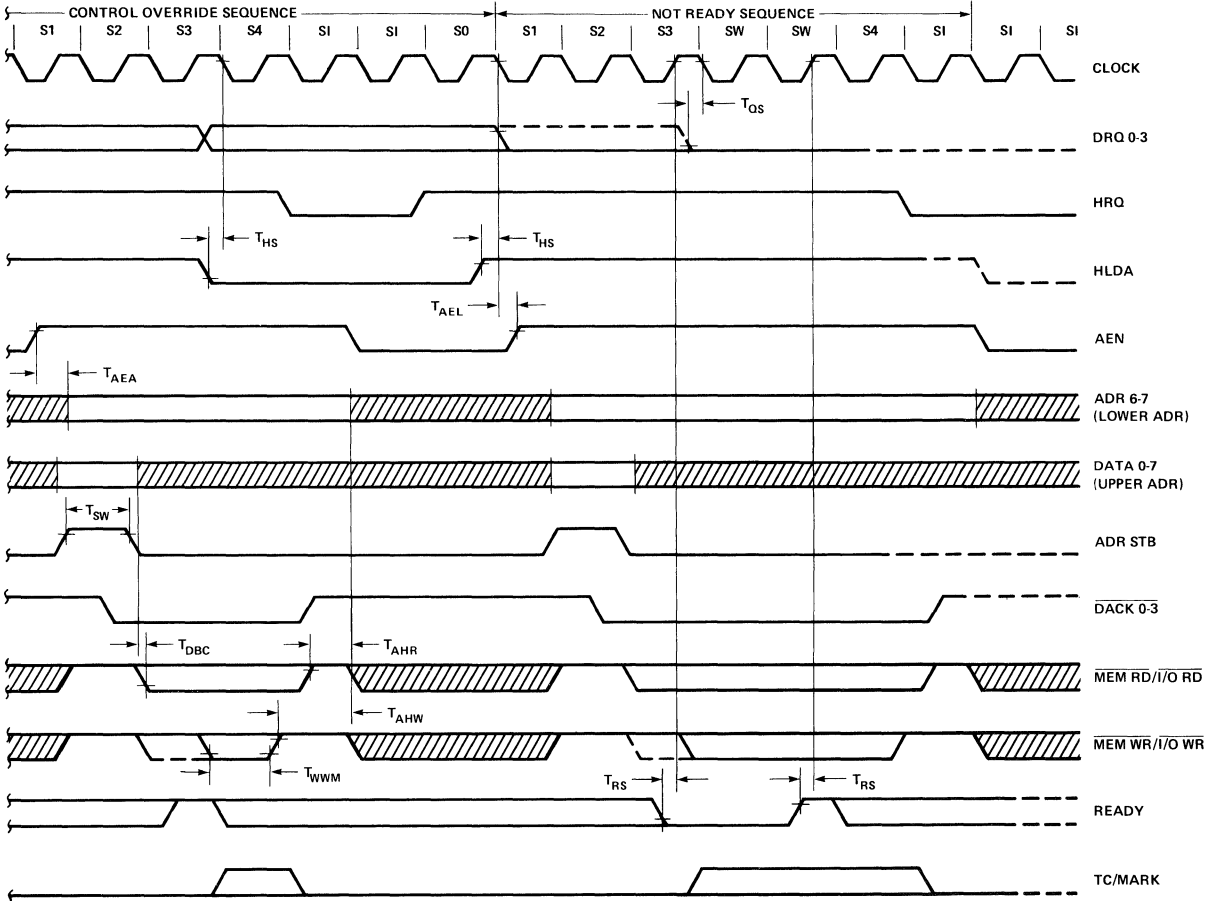
= HIGH IMPEDANCE

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . –65°C to +150°C
Voltage on Any Pin
   With Respect to Ground . . . . –0.5V to +7V
Power Dissipation . . . . 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	–0.5	0.8	Volts	
V_{IH}	Input High Voltage	2.0	V_{CC}+.5	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	Volts	I_{OH}=–150μA for AB, DB and AEN I_{OH}=–80μA for others
V_{HH}	HRQ Output High Voltage	3.3	V_{CC}	Volts	I_{OH} = –80μA
I_{CC}	V_{CC} Current Drain		120	mA	
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Leakage During Float		±10	μA	V_{OUT} = V_{CC} to 0V

CAPACITANCE

$T_A = 25°C$; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. CHARACTERISTICS: PERIPHERAL (SLAVE) MODE

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm5\%$; GND = 0V (Note 1).

8080 BUS PARAMETERS:
READ CYCLE

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{AR}	Adr or $\overline{CS}\downarrow$ Setup to $\overline{RD}\downarrow$	0		0		ns	
T_{RA}	Adr or $\overline{CS}\uparrow$ Hold from $\overline{RD}\uparrow$	0		0		ns	
T_{RD}	Data Access from $\overline{RD}\downarrow$	0	300	0	200	ns	(Note 2)
T_{DF}	DB→Float Delay from $\overline{RD}\uparrow$	20	150	20	100	ns	
T_{RR}	$\overline{RD}$ Width	250		250		ns	

WRITE CYCLE:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{AW}	Adr Setup to $\overline{WR}\downarrow$	20		20		ns	
T_{WA}	Adr Hold from $\overline{WR}\uparrow$	0		0		ns	
T_{DW}	Data Setup to $\overline{WR}\uparrow$	200		200		ns	
T_{WD}	Data Hold from $\overline{WR}\uparrow$	0		0		ns	
T_{WW}	$\overline{WR}$ Width	200		200		ns	

OTHER TIMING:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{RSTW}	Reset Pulse Width	300		300		ns	
T_{RSTD}	Power Supply↑ (V_{CC}) Setup to Reset↓	500		500		μs	
T_r	Signal Rise Time		20		20	ns	
T_f	Signal Fall Time		20		20	ns	
T_{RSTS}	Reset to First $\overline{IOWR}$	2		2		t_{CY}	

Notes: 1. All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V
2. 8257: $C_L = 100pF$, 8257-5: $C_L = 150pF$. Output "1" at 2.0V, "0" at 0.8V

8257 PERIPHERAL MODE TIMING DIAGRAM

WRITE TIMING:
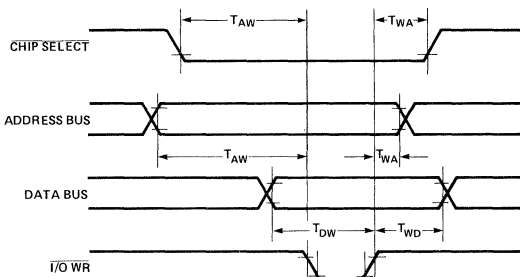
READ TIMING:
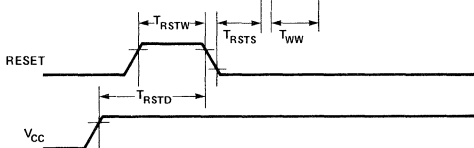
RESET TIMING:
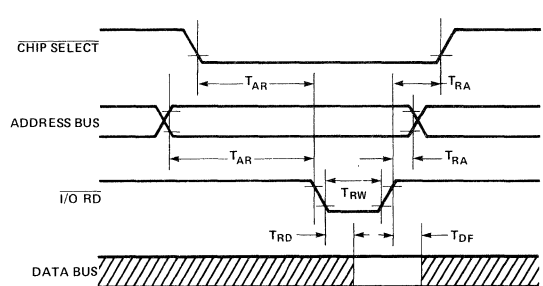
INPUT WAVEFORM FOR A.C. TESTS:

8257, 8257-5

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. CHARACTERISTICS: DMA (MASTER) MODE $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, GND $= 0V$

SYMBOL	PARAMETER	8257 MIN.	8257 MAX.	8257-5 MIN.	8257-5 MAX.	UNIT
T_{CY}	Cycle Time (Period)	320	4	320	4	μs
$T\theta$	Clock Active (High)	120	$.8T_{CY}$	80	$.8T_{CY}$	ns
T_{QS}	DRQ↑ Setup to θ↓(SI,S4)	120		120		
T_{QH}	DRQ↓ Hold from HLDA↑[4]	0		0		
T_{DQ}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 2.0V)[1]		160		160	ns
T_{DQ1}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 3.3V)[3]		250		250	ns
T_{HS}	HLDA↑ or ↓Setup to θ↓(SI,S4)	100		100		ns
T_{AEL}	AEN↑ Delay from θ↓(S1)[1]		300		300	ns
T_{AET}	AEN↓ Delay from θ↑(SI)[1]		200		200	ns
T_{AEA}	Adr(AB)(Active) Delay from AEN↑(S1)[4]	20		20		ns
T_{FAAB}	Adr(AB)(Active) Delay from θ↑(S1)[2]		250		250	ns
T_{AFAB}	Adr(AB)(Float) Delay from θ↑(SI)[2]		150		150	ns
T_{ASM}	Adr(AB)(Stable) Delay from θ↑(S1)[2]		250		250	ns
T_{AH}	Adr(AB)(Stable) Hold from θ↑(S1)[2]	T_{ASM}-50		T_{ASM}-50		
T_{AHR}	Adr(AB)(Valid) Hold from $\overline{Rd}$↑(S1,SI)[4]	60		60		ns
T_{AHW}	Adr(AB)(Valid) Hold from $\overline{Wr}$↑(S1,SI)[4]	300		300		ns
T_{FADB}	Adr(DB)(Active) Delay from θ↑(S1)[2]		300		300	ns
T_{AFDB}	Adr(DB)(Float) Delay from θ↑(S2)[2]	T_{STT}+20	250	T_{STT}+20	170	ns
T_{ASS}	Adr(DB) Setup to AdrStb↓(S1-S2)[4]	100		100		ns
T_{AHS}	Adr(DB)(Valid) Hold from AdrStb↓(S2)[4]	50		50		ns
T_{STL}	AdrStb↑ Delay from θ↑(S1)[1]		200		200	ns
T_{STT}	AdrStb↓ Delay from θ↑(S2)[1]		140		140	ns
T_{SW}	AdrStb Width (S1-S2)[4]	T_{CY}-100		T_{CY}-100		ns
T_{ASC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from AdrStb↓(S2)[4]	70		70		ns
T_{DBC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from Adr(DB) (Float)(S2)[4]	20		20		ns
T_{AK}	DACK↑ or ↓Delay from θ↓(S2,S1) and TC/Mark↑ Delay from θ↑(S3) and TC/Mark↓ Delay from θ↑(S4)[1,5]		250		250	ns
T_{DCL}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from θ↑(S2) and $\overline{Wr}$↓ Delay from θ↑(S3)[2,6]		200		200	ns
T_{DCT}	$\overline{Rd}$↑ Delay from θ↓(S1,SI) and $\overline{Wr}$↑ Delay from θ↑(S4)[2,7]		200		200	ns
T_{FAC}	$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑(S1)[2]		300		300	ns
T_{AFC}	$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑(SI)[2]		150		150	ns
T_{RWM}	$\overline{Rd}$ Width (S2-S1 or SI)[4]	$2T_{CY} + T_\theta$-50		$2T_{CY} + T_\theta$-50		ns
T_{WWM}	$\overline{Wr}$ Width (S3-S4)[4]	T_{CY}-50		T_{CY}-50		ns
T_{WWME}	$\overline{Wr}$(Ext) Width (S2-S4)[4]	$2T_{CY}$-50		$2T_{CY}$-50		ns
T_{RS}	READY Set Up Time to θ↑(S3, Sw)	30		30		ns
T_{RH}	READY Hold Time from θ↑(S3, Sw)	20		20		ns

Notes: 1. Load = 1 TTL. 2. Load = 1 TTL + 50pF. 3. Load = 1 TTL + (R$_L$ = 3.3K), V_{OH} = 3.3V. 4. Tracking Specification. 5. $\Delta T_{AK} < 50$ ns. 6. $\Delta T_{DCL} < 50$ ns. 7. $\Delta T_{DCT} < 50$ ns.

intel®

8259, 8259-5
PROGRAMMABLE INTERRUPT CONTROLLER

- MCS-85™ Compatible 8259-5
- Eight Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Modes

- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- 28 Pin Dual-In-Line Package
- Fully Compatible with Intel CPUs

The 8259 handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts, without additional circuitry. It will be packaged in a 28-pin plastic DIP, uses nMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259 is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

PIN CONFIGURATION
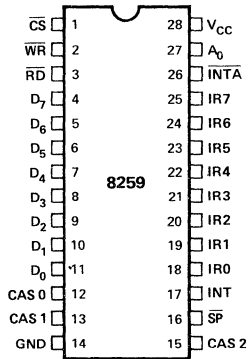
PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
$\overline{CS}$	CHIP SELECT
CAS1–CAS0	CASCADE LINES
$\overline{SP}$	SLAVE PROGRAM INPUT
INT	INTERRUPT OUTPUT
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE INPUT
IR0–IR7	INTERRUPT REQUEST INPUTS

BLOCK DIAGRAM
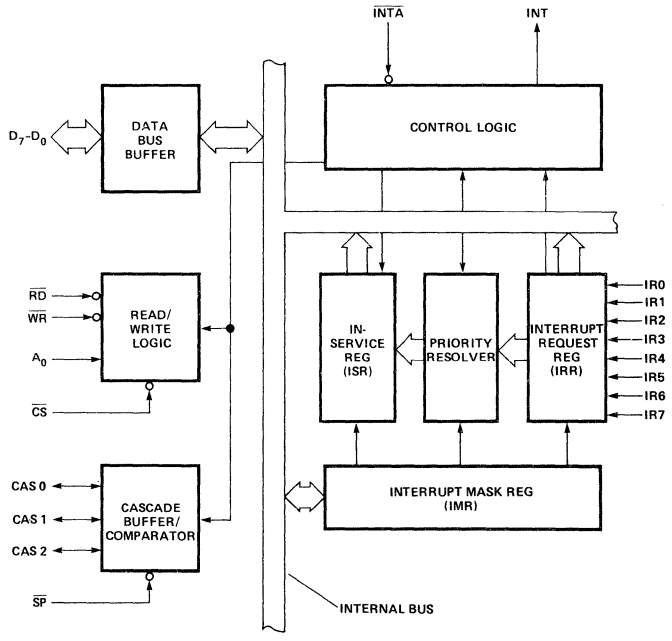
INTERRUPTS IN MICROCOMPUTER SYSTEMS

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient method so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the **Polled** approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuence polling cycle and that such a method would have a serious, detrimental effect on system throughput thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desireable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete however the processor would resume exactly where it left off.

This method is called **Interrupt**. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced and issues an Interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. The PIC does this by providing the CPU with a 3-byte CALL instruction.
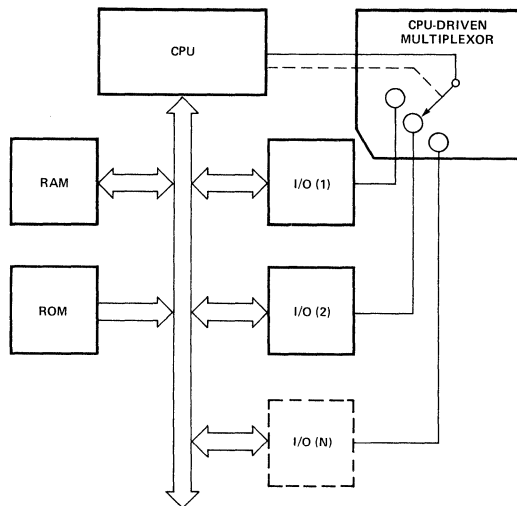
POLLED METHOD
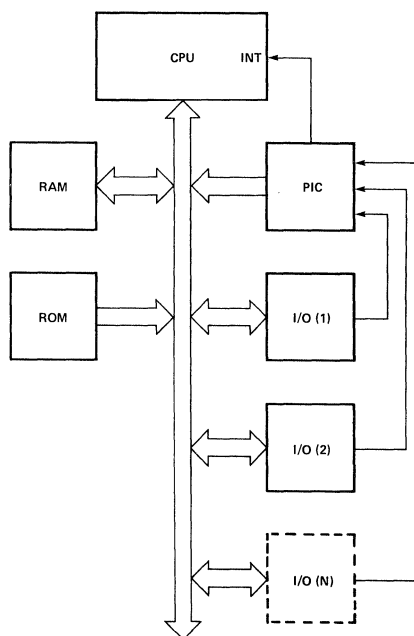
INTERRUPT METHOD

8259 BASIC FUNCTIONAL DESCRIPTION

General

The 8259 is a device specifically designed for use in real time, interrupt driven, microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259s (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 8259 can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080 input level.

$\overline{INTA}$ (Interrupt Acknowledge)

Three $\overline{INTA}$ pulses will cause the 8259 to release a 3-byte CALL instruction onto the Data Bus.

Interrupt Mask Register (IMR)

The IMR stores the bits of the interrupt lines to be masked. The IMR operates on the ISR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.
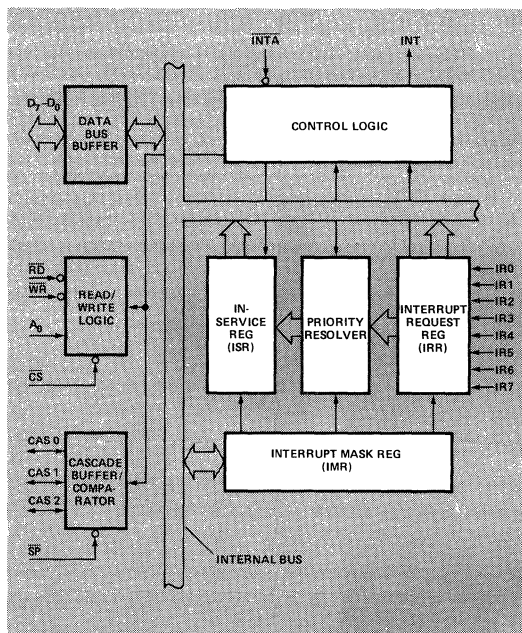
8259 BLOCK DIAGRAM
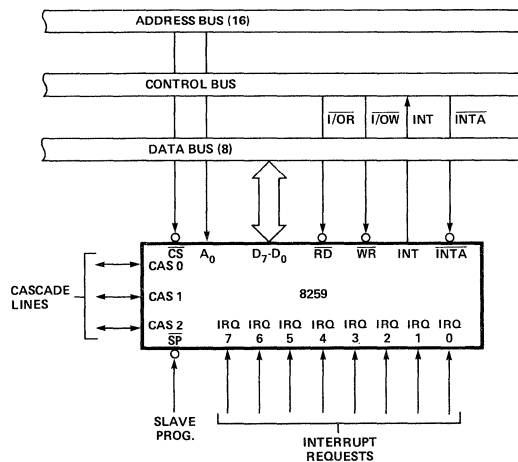
8259 INTERFACE TO STANDARD SYSTEM BUS

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8259 to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259 to be transferred onto the Data Bus.

C̄S̄ (Chip Select)

A "low" on this input enables the 8259. No reading or writing of the chip will occur unless the device is selected.

W̄R̄ (Write)

A "low" on this input enables the CPU to write control words (ICWs and OCWs) to the 8259.

R̄D̄ (Read)

A "low" on this input enables the 8259 to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR) or the BCD of the Interrupt level on to the Data Bus.

A0

This input signal is used in conjunction with W̄R̄ and R̄D̄ signals to write commands into the various command registers as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.
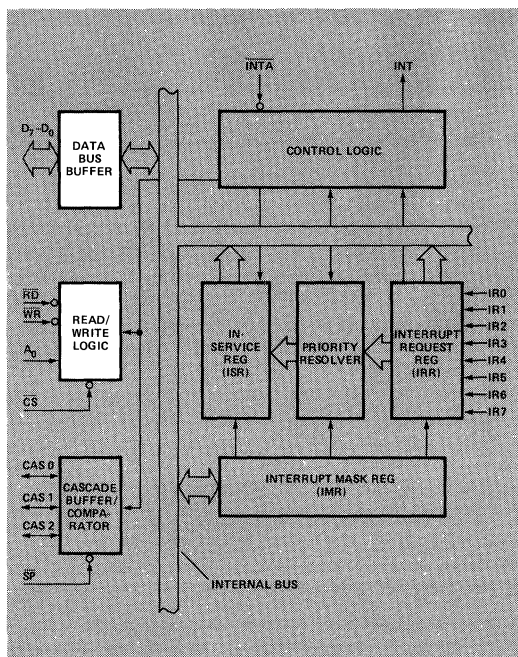
8259 BLOCK DIAGRAM

8259 BASIC OPERATION

A_0	D_4	D_3	R̄D̄	W̄R̄	C̄S̄	INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or Interrupting Level ⇒ DATA BUS (Note 1)
1			0	1	0	IMR ⇒ DATA BUS
						OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	DATA BUS ⇒ OCW2
0	0	1	1	0	0	DATA BUS ⇒ OCW3
0	1	X	1	0	0	DATA BUS ⇒ ICW1
1	X	X	1	0	0	DATA BUS ⇒ OCW1, ICW2, ICW3 (Note 2)
						DISABLE FUNCTION
X	X	X	1	1	0	DATA BUS ⇒ 3-STATE
X	X	X	X	X	1	DATA BUS ⇒ 3-STATE

Note 1: Selection of IRR, ISR or Interrupting Level is based on the content of OCW3 written before the READ operation.
Note 2: On-chip sequencer logic queues these commands into proper sequence.

$\overline{SP}$ (Slave Program)

More than one 8259 can be used in the system to expand the priority interrupt scheme up to 64 levels. In such case, one 8259 acts as the master, and the others act as slaves. A "high" on the $\overline{SP}$ pin designates the 8259 as the master, a "low" designates it as a slave.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all 8259 used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259 is used as a master ($\overline{SP}$ = 1), and are inputs when the 8259 is used as a slave ($\overline{SP}$ = 0). As a master, the 8259 sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine addressed onto the Data Bus during next two consecutive $\overline{INTA}$ pulses. (See section "Cascading the 8259".)
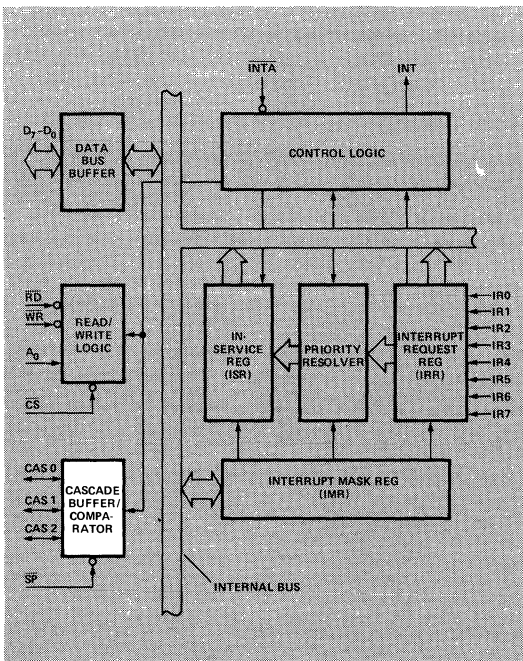
8259 BLOCK DIAGRAM

8259 DETAILED OPERATIONAL SUMMARY

General

The powerful features of the 8259 in a microcomputer system are its programmability and its utilization of the CALL instruction to jump into any address in the memory map. The normal sequence of events that the 8259 interacts with the CPU is as follows:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The 8259 accepts these requests, resolves the priorities, and sends an INT to the CPU.

3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259 will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.
5. This CALL instruction will initiate two more $\overline{INTA}$ pulses to be sent to the 8259 from the CPU group.
6. These two $\overline{INTA}$ pulses allow the 8259 to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the 8259. ISR bit is not reset until the end of the subroutine when an EOI (End of interrupt) command is issued to the 8259.

Programming The 8259

The 8259 accepts two types of command words generated by the CPU:

1. Initialization Command Words (ICWs):
   Before normal operation can begin, each 8259 in the system must be brought to a starting point — by a sequence of 2 or 3 bytes timed by $\overline{WR}$ pulses. This sequence is described in Figure 1.
2. Operation Command Words (OCWs):
   These are the command words which command the 8259 to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 8259 at anytime after initialization.
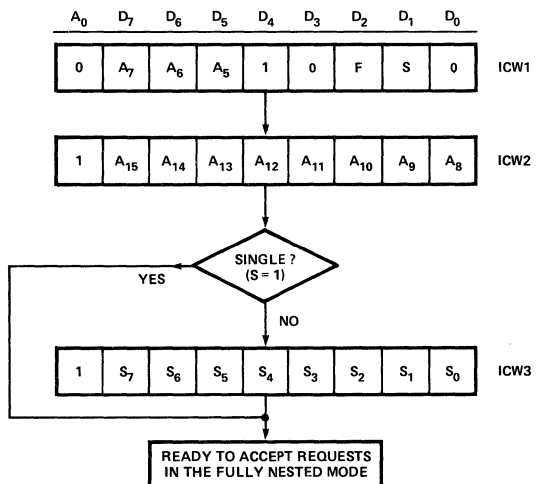
FIGURE 1. INITIALIZATION SEQUENCE

Initialization Command Words 1 and 2: (ICW1 and ICW2)

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1), and initiates the initialization sequence. During this sequence, the following occur automatically:

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low to high transition to generate an interrupt.

b. The interrupt Mask Register is cleared.

c. IR 7 input is assigned priority 7.

d. Special Mask Mode Flip-flop and status Read Flip-flop are reset.

The 8 requesting devices have 8 addresses equally spaced in memory. The addresses can be programmed at intervals of 4 or 8 bytes; the 8 routines thus occupying a page of 32 or 64 bytes respectively in memory.

The address format is:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

DEFINED BY D_{5-7} OF ICW1   AUTOMATICALLY INSERTED BY 8259

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

DEFINED BY ICW2
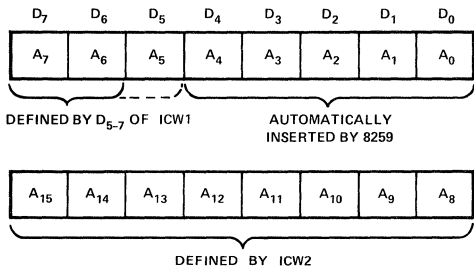
A0-4 are automatically inserted by the 8259, while A15-6 are programmed by ICW1 and ICW2. When interval = 8, A5 is fixed by the 8259. If interval = 4, A5 is programmed in ICW1. Thus, the interrupt service routines can be located anywhere in the memory space. The 8 byte interval will maintain compatibility with current 8080 RESTART instruction software, while the 4 byte interval is best for compact jump table.

The address format inserted by the 8259 is described in Table 1.

The bits F and S are defined by ICW1 as follows:

F: Call address interval. F = 1, then interval = 4; F = 0, then interval = 8.

S: Single. S = 1 means that this is the only 8259 in the system. It avoids the necesity of programming ICW3.

		INTERVAL = 4							INTERVAL = 8						
					LOWER MEMORY ROUTINE ADDRESS										
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
IR 7		A7	A6	A5	1	1	1	0	0	A7	A6	1	1	1	0	0	0
IR 6		A7	A6	A5	1	1	0	0	0	A7	A6	1	1	0	0	0	0
IR 5		A7	A6	A5	1	0	1	0	0	A7	A6	1	0	1	0	0	0
IR 4		A7	A6	A5	1	0	0	0	0	A7	A6	1	0	0	0	0	0
IR 3		A7	A6	A5	0	1	1	0	0	A7	A6	0	1	1	0	0	0
IR 2		A7	A6	A5	0	1	0	0	0	A7	A6	0	1	0	0	0	0
IR 1		A7	A6	A5	0	0	1	0	0	A7	A6	0	0	1	0	0	0
IR 0		A7	A6	A5	0	0	0	0	0	A7	A6	0	0	0	0	0	0

TABLE 1.

Example of Interrupt Acknowledge Sequence

Assume the 8259 is programmed with F = 1 (CALL address interval = 4), and IR5 is the interrupting level. The 3 byte sequence released by the 8259 timed by the $\overline{INTA}$ pulses is as follows:

	D7	D6	D5	D4	D3	D2	D1	D0	
1st $\overline{INTA}$	1	1	0	0	1	1	0	1	CALL CODE
2nd $\overline{INTA}$	A7	A6	A5	1	0	1	0	0	LOWER ROUTINE ADDRESS
3rd $\overline{INTA}$	A15	A14	A13	A12	A11	A10	A9	A8	HIGHER ROUTINE ADDRESS

Initialization Command Word 3 (ICW3)

This will load the 8-bit slave register. The functions of this register are as follows:

a. If the 8259 is the master, a "1" is set for each slave in the system. The master then will release byte 1 of the CALL sequence and will enable the corresponding slave to release bytes 2 and 3, through the cascade lines.

b. If the 8259 is a slave, bits 2 - 0 identify the slave. The slave compares its CAS0-2 inputs (sent by the master) with these bits. If they are equal, bytes 2 and 3 of the CALL sequence are released.

If bit S is set in ICW1, there is no need to program ICW3.

ICW1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	A_7	A_6	A_5	1	0	F	S	0

- 1 = SINGLE
  0 = NOT SINGLE
- CALL ADDRESS INTERVAL
  1 = INTERVAL IS 4
  0 = INTERVAL IS 8
- A_{7-5} OF LOWER ROUTINE ADDRESS

ICW2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

- UPPER ROUTINE ADDRESS

ICW3 (MASTER DEVICE)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

- 1 = IR INPUT HAS A SLAVE
  0 = IR INPUT DOES NOT HAVE A SLAVE

ICW3 (SLAVE DEVICE)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	ID_2	ID_1	ID_0

| X | X | X | X | X |

DON'T CARE

SLAVE ID[1]

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

NOTE 1: SLAVE ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT.

INITIALIZATION COMMAND WORD FORMAT

Operation Command Words (OCWs)

After the Initialization Command Words (ICWs) are programmed into the 8259, the chip is ready to accept interrupt requests at its input lines. However, during the 8259 operation, a selection of algorithms can command the 8259 to operate in various modes through the Operation Command Words (OCWs). These various modes and their associated OCWs are described below.

Interrupt Masks

Each Interrupt Request input can be masked individually by the Interrupt Masked Register (IMR) programmed through OCW1.

The IMR operates on the In-Service Register. Note that if an interrupt is already acknowledged by the 8259 (an INTA pulse has occurred), then the Interrupting level, although masked, will inhibit the lower priorities. To enable these lower priority interrupts, one can do one of two things: (1) Write an End of Interrupt (EOI) command (OCW2) to reset the IST bit or (2) Set the special mask mode using OCW3 (as will be explained later in the special mask mode.)

Fully Nested Mode

The 8259 will operate in the fully nested mode after the execution of the initialization sequence without any OCW being written. In this mode, the interrupt requests are ordered in priorities from 0 through 7. When an interrupt is acknowledged, the highest priority request is determined and its address vector placed on the bus. In addition, a bit of the Interrupt service register (IS 7-0) is set. This bit remains set until the CPU issues an End of Interrupt (EOI) command immediately before returning from the service routine. While the IS bit is set, all further interrupts of lower priority are inhibited, while higher levels will be able to generate an interrupt (which will only be acknowledged if the CPU has enabled its own interrupt input through software).

After the Initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained in the rotating priority mode.

Rotating Priority Commands

There are two variations of rotating priority: auto rotate and specific rotate.

1. Auto Rotate — Executing the Rotate-at-EOI (Auto) command, resets the highest priority ISR bit and assigns that input the lowest priority. Thus, a device requesting an interrupt will have to wait, in the worst case, until 7 other devices are serviced at most once each, i.e., if the priority and "in-service" status is:

BEFORE ROTATE	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	1	0	0	0	0

	LOWEST PRIORITY				HIGHEST PRIORITY			
PRIORITY STATUS	7	6	5	4	3	2	1	0

AFTER ROTATE	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	0	0	0	0	0

	LOWEST PRIORITY				HIGHEST PRIORITY			
PRIORITY STATUS	4	3	2	1	0	7	6	5

In this example, the In-Service FF corresponding to line 4 (the highest priority FF set) was reset and line 4 became the lowest priority, while all the other priorities rotated correspondingly.

The Rotate command is issued in OCW2, where: R = 1, EOI = 1, SEOI = 0.

2. Specific Rotate — The programmer can change priorities by programming the bottom priority, and by doing this, to fix the highest priority: i.e., if IR5 is programmed as the bottom priority device, the IR6 will have the highest one. This command can be used with or without resetting the selected ISR bit.

The Rotate command is issued in OCW2 where: R = 1, SEOI = 1. L2, L1, L0 are the BCD priority level codes of the bottom priority device. If EOI = 1 also, the ISR bit selected by L2-L0 is reset.

Observe that this mode is independent of the End of Interrupt Command and priority changes can be executed during EOI command or independently from the EOI command.

End of Interrupt (EOI) and Specific End of Interrupt (SEOI)

An End of Interrupt command word must be issued to the 8259 before returning from a service routine, to reset the appropriate IS bit.

There are two forms of EOI command: Specific and non-Specific. When the 8259 is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a non-Specific EOI command is issued the 8259 will automatically reset the highest IS bit of those that are set, since in the nested mode, the highest IS level was necessarily the last level acknowledged and will necessarily be the next routine level returned from.

However, when a mode is used which may disturb the fully nested structure, such as in the rotating priority case, the 8259 may no longer be able to determine the last level acknowledged. In this case, a specific EOI (SEOI) must be issued which includes the IS level to be reset as part of the command. The End of the Interrupt is issued whenever EOI = "1" in OCW2. For specific EOI, SEOI = "1", and EOI = 1. L2, L1, L0 is then the BCD level to be reset. As explained in the Rotate Mode earlier, this can also be the bottom priority code. Note that although the Rotate command can be issued during an EOI = 1, it is not necessarily tied to it.

OCW1

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0

INTERRUPT MASK
1 = MASK SET
0 = MASK RESET

OCW2

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	R	SEOI	EOI	0	0	L2	L1	L0

BCD LEVEL TO BE RESET
OR PUT INTO LOWEST PRIORITY

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

NON-SPECIFIC END OF INTERRUPT
1 = RESET THE HIGHEST PRIORITY
BIT OF ISR
0 = NO ACTION

SPECIFIC END OF INTERRUPT
1 = L_2, L_1, L_0 BITS ARE USED
0 = NO ACTION

ROTATE PRIORITY
1 = ROTATE
0 = NOT ROTATE

OCW3

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	—	ESMM	SMM	0	1	P	ERIS	RIS

DON'T CARE

READ IN-SERVICE REGISTER

0	1	0	1
0	0	1	1
NO ACTION		READ IR REG ON NEXT RD PULSE	READ IS REG ON NEXT RD PULSE

POLLING
A HIGH ENABLES THE NEXT RD PULSE
TO READ THE BCD CODE OF THE HIGH-
EST LEVEL REQUESTING INTERRUPT.

SPECIAL MASK MODE

0	1	0	1
0	0	1	1
NO ACTION		RESET SPECIAL MASK	SET SPECIAL MASK

OPERATION COMMAND WORD FORMAT

Special Mask Mode (SMM)

This mode is useful when some bit(s) are set (masked) by the Interrupt Mask Register (IMR) through OCW1. If, for some reason, we are currently in an interrupt service routine which is masked (this could happen when the subroutine intentionally mask itself off), it is still possible to enable the lower priority lines by setting the Special Mask mode. In this mode the lower priority lines are enabled until the SMM is reset. The higher priorities are not affected.

The special mask mode FF is set by OCW3 where ESMM = 1, SMM = 1, and reset where: ESSM = 1 and SMM = 0.

Polled Mode

In this mode, the CPU must disable its interrupt input. Service to device is achieved by programmer initiative by a Poll command.

The poll command is issued by setting P = "1" in OCW3 during a $\overline{WR}$ pulse.

The 8259 treats the next $\overline{RD}$ pulse as an interrupt acknowledge, sets the appropriate IS Flip-flop, if there is a request, and reads the priority level.

For polling operation, an OCW3 must be written before every read.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	–	–	–	–	W2	W1	W0
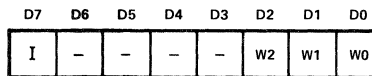
W0 — 2: BCD code of the highest priority level requesting service.
I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine common to several levels — so that the $\overline{INTA}$ sequence is not needed (and this saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

SUMMARY OF OPERATION COMMAND WORD PROGRAMMING

	A0	D4	D3				
OCW1	1			M7-M0		IMR (Interrupt Mask Register). $\overline{WR}$ will load it while status can be read with $\overline{RD}$.	
OCW2	0	0	0	R	SEOI	EOI	
				0	0	0	No Action.
				0	0	1	Non-specific End of Interrupt.
				0	1	0	No Action.
				0	1	1	Specific End of Interrupt. L2, L1, L0 is the BCD level to be reset.
				1	0	0	No Action.
				1	0	1	Rotate priority at EOI. (Auto Mode)
				1	1	0	Rotate priority, L2, L1, L0 becomes bottom priority without Ending of Interrupt.
				1	1	1	Rotate priority at EOI (Specific Mode), L2, L1, L0 becomes bottom priority, and its corresponding IS FF is reset.
OCW3	0	0	1	ESMM	SMM		
				0	0		Special Mask not Affected.
				0	1		
				1	0		Reset Special Mask.
				1	1		Set Special Mask.
				ERIS	RIS		
				0	0		No Action.
				0	1		
				1	0		Read IR Register Status.
				1	1		Read IS Register Status.

Note: The CPU interrupt input must be disabled during:
1. Initialization sequence for all the 8259 in the system.
2. Any control command execution.

Reading 8259 Status

The input status of several internal registers can be read to update the user information on the system. The following registers can be read by issuing a suitable OCW3 and reading with $\overline{RD}$.

Interrupt Requests Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR).

In Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when prior to the $\overline{RD}$ pulse, an $\overline{WR}$ pulse is issued with OCW3, and ERIS = 1, RIS = 0.

The ISR can be read in a similar mode, when ERIS = 1, RIS = 1.

There is no need to write an OCW3 before every status read operation as long as the status read corresponds with the previous one, i.e. the 8259 "remembers" whether the IRR or ISR has been previously selected by the OCW3.

For reading the IMR, a $\overline{WR}$ pulse is not necessary to preceed the $\overline{RD}$. The output data bus will contain the IMR whenever $\overline{RD}$ is active and A0 = 1.

Polling overrides status read when P = 1, ERIS = 1 in OCW3.

Cascading

The 8259 can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

A typical system is shown in Figure 2. The master controls, through the 3 line cascade bus, which one of the slaves will release the corresponding address.

As shown in Figure 2, the slaves interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will release the 8080 CALL code during byte 1 of $\overline{INTA}$ and will enable the corresponding slave to release the device routine address during bytes 2 and 3 of $\overline{INTA}$.

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first $\overline{INTA}$ pulse to the trailing edge of the third pulse. It is obvious that each 8259 in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select ($\overline{CS}$) input of each 8259. The slave program pin ($\overline{SP}$) must be at a "low" level for a slave (and then the cascade lines are inputs) and at a "high" level for a master (and then the cascade lines are outpus).
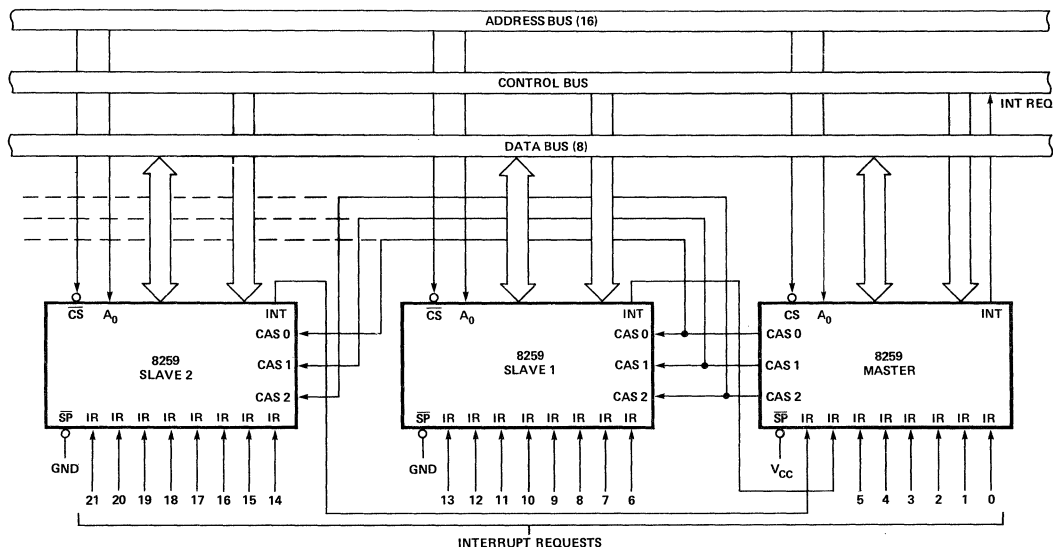
FIGURE 2. CASCADING THE 8259

8259 INSTRUCTION SET

INST. NO.		A0	D7	D6	D5	D4	D3	D2	D1	D0	OPERATION DESCRIPTION
1	ICW1 A	0	A7	A6	A5	1	0	1	1	0	Byte 1 initialization, format = 4, single.
2	ICW1 B	0	A7	A6	A5	1	0	1	0	0	Byte 1 initialization, format = 4, not single.
3	ICW1 C	0	A7	A6	A5	1	0	0	1	0	Byte 1 initialization, format = 8, single.
4	ICW1 D	0	A7	A6	A5	1	0	0	0	0	Byte 1 initialization, format = 8, not single.
5	ICW2	1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization (Address No. 2)
6	ICW3 M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization — master.
7	ICW3 S	1	0	0	0	0	0	S2	S1	S0	Byte 3 initialization — slave.
8	OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask reg, read mask reg.
9	OCW2 E	0	0	0	1	0	0	0	0	0	Non specific EOI.
10	OCW2 SE	0	0	1	1	0	0	L2	L1	L0	Specific EOI. L2, L1, L0 code of IS FF to be reset.
11	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate at EOI (Auto Mode).
12	OCW2 RSE	0	1	1	1	0	0	L2	L1	L0	Rotate at EOI (Specific Mode). L2, L1, L0, code of line to be reset and selected as bottom priority.
13	OCW2 RS	0	1	1	0	0	0	L2	L1	L0	L2, L1, L0 code of bottom priority line.
14	OCW3 P	0	—	0	0	0	1	1	0	0	Poll mode.
15	OCW3 RIS	0	—	0	0	0	1	0	1	1	Read IS register.
16	OCW3 RR	0	—	0	0	0	1	0	1	0	Read requests register.
17	OCW3 SM	0	—	1	1	0	1	0	0	0	Set special mask mode.
18	OCW3 RSM	0	—	1	0	0	1	0	0	0	Reset special mask mode.

Notes:
1. In the master mode $\overline{SP}$ pin = 1, in slave mode $\overline{SP}$ = 0.
2. (—) = do not care.

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .... $0°$ C to $70°$ C
Storage Temperature .... $-65°$ C to $+150°$ C
Voltage On Any Pin
  With Respect to Ground .... -0.5 V to $+7$ V
Power Dissipation .... 1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS $(T_A = 0°$C to $70°$C; $V_{CC} = 5$V $\pm5\%)$

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	$-.5$	$.8$	V	
V_{IH}	Input High Voltage	2.0	$V_{CC}+.5$V	V	
V_{OL}	Output Low Voltage		$.45$	V	$I_{OL} = 2$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA
V_{OH-INT}	Interrupt Output High Voltage	2.4		V	$I_{OH} = -400$ μA
		3.5		V	$I_{OH} = -50$ μA
$I_{IL(IR_{0-7})}$	Input Leakage Current		-300	μA	$V_{IN} = 0$V
	for IR_{0-7}		10	μA	$V_{IN} = V_{CC}$
I_{IL}	Input Leakage Current		10	μA	$V_{IN} = V_{CC}$ to 0V
	for Other Inputs				
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = 0.45$V to V_{CC}
I_{CC}	V_{CC} Supply Current		100	mA	

CAPACITANCE $T_A = 25°$C; $V_{CC} = $ GND $ = 0$V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	$fc = 1$ MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. CHARACTERISTICS $(T_A = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$, GND = 0V)

BUS PARAMETERS

READ

SYMBOL	PARAMETER	8259		8259-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{AR}	$\overline{CS}/A_0$ Stable Before $\overline{RD}$ or $\overline{INTA}$	50		50		ns
t_{RA}	$\overline{CS}/A_0$ Stable After $\overline{RD}$ or $\overline{INTA}$	5		30		ns
t_{RR}	$\overline{RD}$ Pulse Width	420		300		ns
t_{RD}	Data Valid From $\overline{RD}/\overline{INTA}$[1]		300		200	ns
t_{DF}	Data Float After $\overline{RD}/\overline{INTA}$	20	200	20	100	ns

WRITE

SYMBOL	PARAMETER	8259		8259-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{AW}	A_0 Stable Before $\overline{WR}$	50		50		ns
t_{WA}	A_0 Stable After $\overline{WR}$	20		30		ns
t_{WW}	$\overline{WR}$ Pulse Width	400		300		ns
t_{DW}	Data Valid to $\overline{WR}$ (T.E.)	300		250		ns
t_{WD}	Data Valid After $\overline{WR}$	40		30		ns

OTHER TIMINGS

SYMBOL	PARAMETER	8259		8259-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{IW}	Width of Interrupt Request Pulse	100		100		ns
t_{INT}	INT ↑ After IR ↑	400		350		ns
t_{IC}	Cascade Line Stable After $\overline{INTA}$ ↑	400		400		ns

Note 1: 8259: $C_L = 100pF$, 8259-5: $C_L = 150pF$.

INPUT WAVEFORMS FOR A.C. TESTS
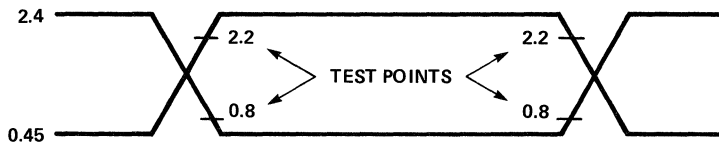
PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

WAVEFORMS

READ TIMING
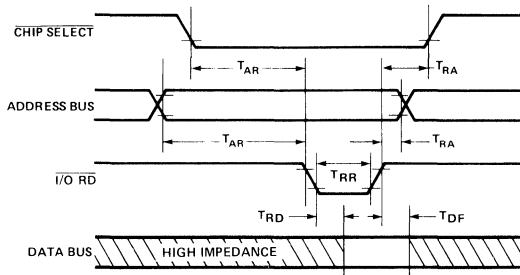
WRITE TIMING
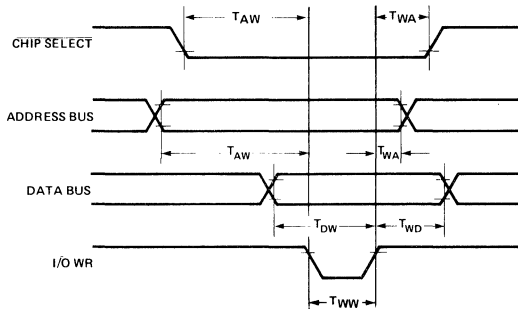
OTHER TIMING
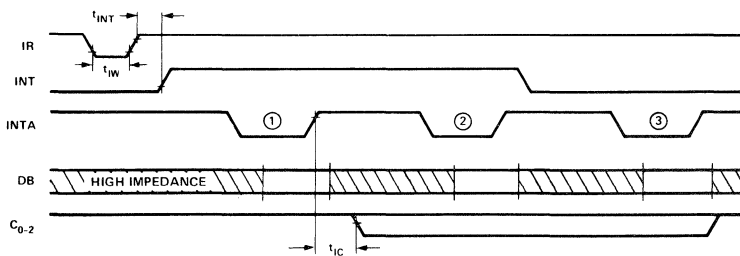
Note: Interrupt Request must remain "HIGH" (at least) until leading edge of first INTA.

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

READ STATUS/POLL MODE
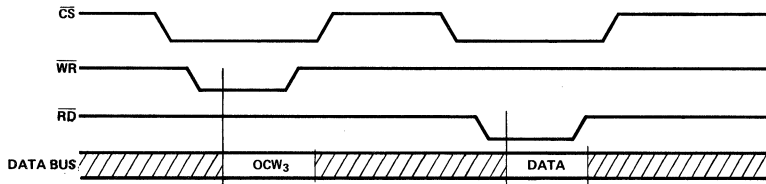
intel®

8271
PROGRAMMABLE FLOPPY DISK CONTROLLER

- ■ **IBM 3740 Soft Sectored Format Compatible**
- ■ **Programmable Record Lengths**
- ■ **Multi-Sector Capability**
- ■ **Maintain Dual Drives with Minimum Software Overhead Expandable to 4 Drives**
- ■ **Automatic Read/Write Head Positioning and Verification**

- ■ **Internal CRC Generation and Checking**
- ■ **Programmable Step Rate, Settle-Time, Head Load Time, Head Unload Index Count**
- ■ **Single +5Volt Supply**
- ■ **40 Pin Package**

The 8271 Floppy Disk Controller (FDC) is an LSI Component designed to interface one to four floppy disk drives to an 8-bit microcomputer system. Its powerful control functions minimize both hardware and software overhead normally associated with floppy disk controllers.

PIN CONFIGURATION

Pin	Signal	Pin	Signal
1	FAULT RESET/OPO	40	V_{CC}
2	SELECT 0	39	LOW CURRENT
3	4 MHz CLK	38	LOAD HEAD
4	RESET	37	DIRECTION
5	READY 1	36	SEEK/STEP
6	SELECT 1	35	WR ENBLE
7	DACK	34	INDEX
8	DRQ	33	WR PROTECT
9	RD	32	READY 0
10	WR	31	TRK0
11	INT	30	COUNT/OPI
12	DB0	29	WR DATA
13	DB1	28	FAULT
14	DB2	27	UNSEP DATA
15	DB3	26	DATA WINDOW
16	DB4	25	PLO/SS
17	DB5	24	CS
18	DB6	23	PLOC
19	DB7	22	A_1
20	GND	21	A_0
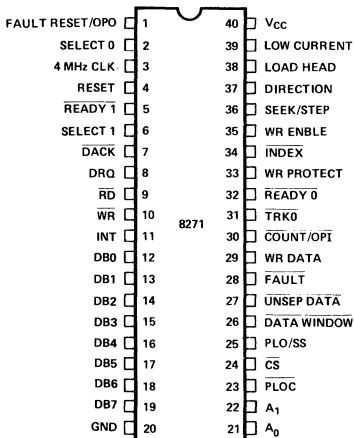
8271

BLOCK DIAGRAM
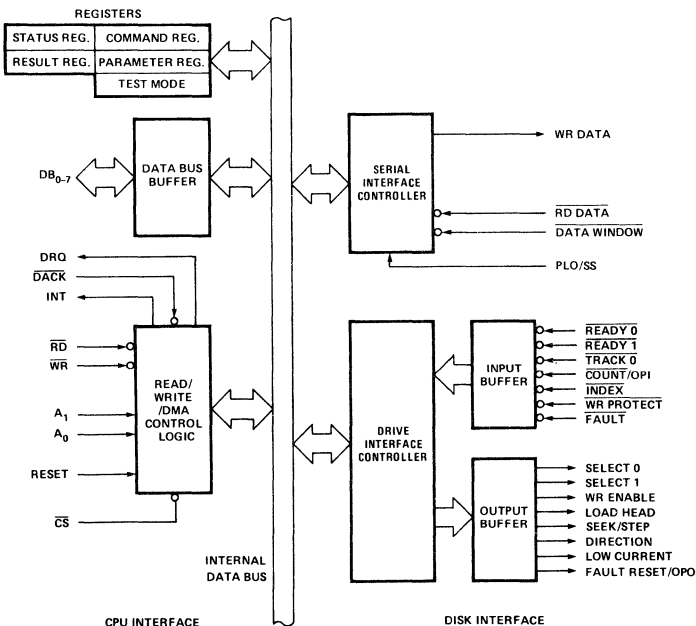
8271 BASIC FUNCTIONAL DESCRIPTION

General

The FDC supports a soft sectored format that is IBM 3740 compatible. This component is a high level controller that relieves the CPU (and user) of many of the control tasks associated with implementing a floppy disk interface. The FDC supports a variety of high level instructions which allow the user to store and retrieve data on a floppy disk without dealing with the low level details of the disk operation.

In addition to the standard read/write commands a scan command is supported. The scan command allows the user program to specify a data pattern and instruct the FDC to search for that pattern on a track. Any application that is required to search the disk (such as point of sale price lookup, disk directory search, etc.) for information may use the scan command to reduce the CPU overhead. Once the scan operation is initiated, no CPU intervention is required.

Hardware Description

The 8271 is packaged in a 40 pin DIP. The following is a functional description of each pin.

Pin Name	I/O	Description
V_{cc}		+5V supply
GND		Ground
4MHz Clock	I	A 4MHz square wave clock
Reset	I	A high signal on the reset input will force the 8271 to an idle state. The 8271 will remain idle until a command is issued by the CPU. The drive interface output signals are forced low.
$\overline{CS}$	I	The I/O Read and I/O Write inputs are enabled by the chip select signal.
DB_7-DB_0	I/O	The Data Bus lines are bidirectional three-state lines.
$\overline{WR}$	I	The Write signal is used to signal the control logic that a transfer of data from the data bus to the 8271 is required.
$\overline{RD}$	I	The Read signal is used to signal the control logic that a transfer of data from the 8271 to the data bus is required.
INT	O	The interrupt signal indicates that the 8271 requires service.

Pin Name	I/O	Description
A_1-A_0	I	These two lines are used to select the destination of source of data to be accessed by the control logic.
DRQ	O	The DMA request signal is used to request a transfer of data between the 8271 and memory.
$\overline{DACK}$	I	The DMA ACK signal notifies the 8271 that a DMA cycle has been granted.
Select 1– Select 0	O	These lines are used to specify the selected drive.
Fault Reset/ OPO	O	The fault reset line is used to reset an error condition which is latched by the drive, otherwise the pin is a user specified optional output.
Write Enable	O	This signal enables the drive write logic.
Seek/Step	O	This multi-function line is used during drive seeks.
Direction	O	The direction line specifies the seek direction.
Load Head	O	The load head line causes the drive to load the Read/Write head load pad against the diskette.
Low Current	O	This line notifies the drive that track 43 or greater is selected.
$\overline{Ready\ 1}$, $\overline{Ready\ 0}$	I	These two lines indicate that the specified drive is ready.
$\overline{Fault}$	I	This line is used by the drive to specify a file unsafe condition.
$\overline{Count/OPI}$	I	If the seek / direction / count seek mode is selected, the count pin is pulsed for each track. Otherwise this pin is user specified optional input.
$\overline{Write\ Protect}$	I	This signal is used to specify if the drive/diskette may be written.
$\overline{TRK0}$	I	This signal indicates when the R/W head is positioned over track zero.
$\overline{Index}$	I	The index signal gives an indication of the relative position of the diskette.
$\overline{PLO/SS}$	I	This pin is used to specify the type of data separator used.
Write Data	O	Composite write data.
$\overline{Unseparated\ Data}$	I	This input is the unseparated data and clocks.
$\overline{Data\ Window}$	I	This is a data window established by the single-shot or phase-locked oscillator data separator.
$\overline{PLOC}$	O	This line is low when the 8271 is searching for input data sync.

Principles of Operation

The 8271 is fully compatible with Intel microprocessors. It accepts commands from the CPU, executes these Commands and provides a Result at the end of execution.

Communication with the CPU are through the activating of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ pins. The A_1,A_0 select the appropriate registers on chip:

A_3	A_3	CS RD	CS WR
0	0	Status Reg	Command Reg
0	1	Result Reg	Parameter Reg

The FDC chip operation is composed of the following general sequence of events:

The Command Phase

During the Command Phase, the CPU issues a command byte to the 8271. The command byte provides a general description of the type of operation requested. Many operations require more detailed information about the comand. In such case, from zero to five parameters are written following the command byte to provide such information. The various commands that the 8271 can recognize are listed in the Software Operation Section.

The Execution Phase

Soon as the last parameter is written into the 8271, the FDC enters the Execution Phase. During this phase there is no need for CPU involvement. The FDC may optionally interface with the 8257 (DMA controller) for high speed data transfers (See System Diagram).

The Result Phase

During the Result Phase, the FDC chip notified the CPU of the outcome of the command execution. This phase may be initiated by:

1. The successful completion of an operation.
2. An error detected during an operation.
3. An illegal command or parameter detected during the Command Phase.

In the Result Phase, the CPU Reads the Status Register which provides the following information:

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

```
                              0  0
COMMAND BUSY ─┘              │  │  └─ NON-DMA MODE
COMMAND REG FULL ───────────┘  └──── INTERRUPT REQ
PARAMETER REG FULL ──────────────── RESULT REG FULL
```
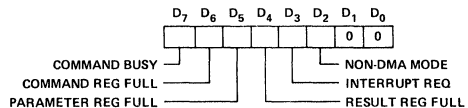
After reading the Status Register, the CPU then Reads the Result Register for more information.

COMMAND PHASE	CPU WRITES THE COMMAND AND PARAMETERS INTO THE 8271 COMMAND AND PARAMETER REGISTERS.
EXECUTION PHASE	THE 8271 IS ON ITS OWN TO CARRY OUT THE COMMANDS.
RESULT PHASE	THE 8271 SIGNALS THE CPU THAT THE EXECUTION HAS FINISHED. THE CPU WILL PERFORM A READ OPERATION OF ONE OR MORE OF THE REGISTERS.
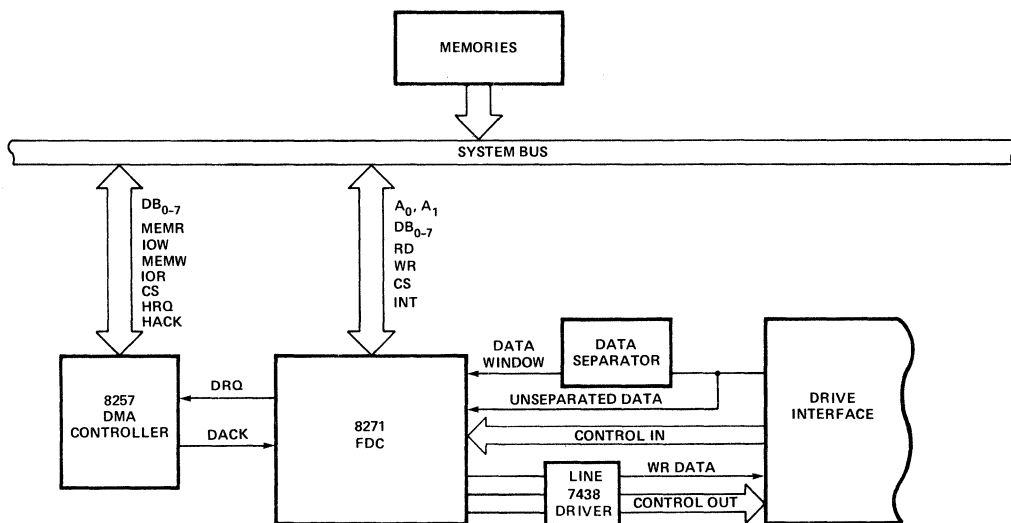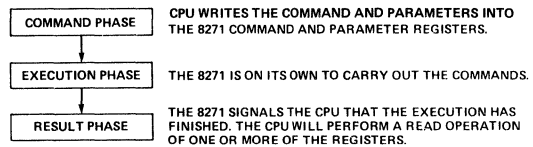
8271 SYSTEM DIAGRAM

Software Operation

The 8271 can accept many powerful commands from the CPU. The following is a list of Basic Commands (associated Parameters not shown).

SCAN DATA

SCAN DATA AND DELETED DATA

WRITE DATA

WRITE DATA AND DELETED DATA

READ DATA

READ DATA AND DELETED DATA

READ ID

VERIFY DATA AND DELETED DATA

FORMAT

SEEK

READ DRIVE STATUS

SPECIFY

RESET

As an example, the SPECIFY command is associated with 4 parameters:

	A_1 A_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	
SPECIFY COMMAND	0 0	0 0 1 1 0 1 1 1	
PARAMETER 0	0 1	0 0 0 0 1 1 0 1	SELECT SPECIFY INITIALIZATION
PARAMETER 1	0 1		STEP RATE (0-255ms IN STEPS OF 1ms)
PARAMETER 2	0 1		STEP SETTLE TIME 0-255ms, IN STEPS OF 1ms
PARAMETER 3	0 1		HEAD LOAD TIME (0-60ms IN STEPS OF 4ms) / HEAD UNLOAD INDEX COUNT (0-14)
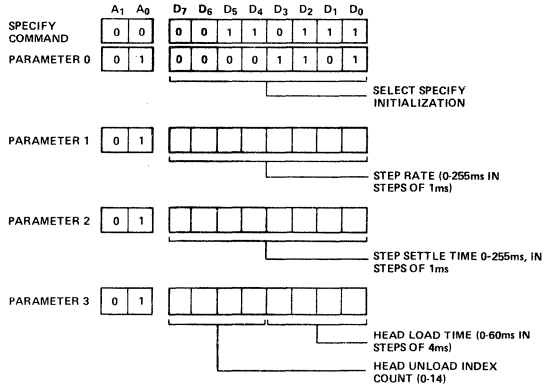
EXECUTION PHASE BASIC CHARACTERISTICS

The following table summarizes the various commands with corresponding execution phase characteristics.

COMMANDS	1 Deleted Data	2 Head	3 Ready	4 Write/ Protect	5 Seek	6 Seek Check	7 Result	8 Completion Interrupt
SCAN DATA	SKIP	LOAD	√	x	YES	YES	YES	YES
SCAN DATA AND DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
WRITE DATA	x	LOAD	√	√	YES	YES	YES	YES
WRITE DEL DATA	XFER	LOAD	√	√	YES	YES	YES	YES
READ DATA	SKIP	LOAD	√	x	YES	YES	YES	YES
READ DATA AND DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
READ ID	x	LOAD	√	x	YES	NO	YES	YES
VERIFY DATA AND DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
FORMAT	x	LOAD	√	√	YES	NO	YES	YES
SEEK	x	–	x	x	YES	NO	YES	YES
READ DRIVE STAT	x	–	x	x	NO	NO	YES	NO
SPECIFY	x	–	x	x	NO	NO	NO	NO
RESET	x	UNLOAD	x	x	NO	NO	NO	NO

Note: 1. "x" → DON'T CARE
2. "√" → check
3. "–" → No change

intel®

8273
SDLC PROTOCOL CONTROLLER

- IBM (SDLC) Compatible
- Full Duplex Operation—56K BAUD
- SDLC Loop Operation
- User Programmable Modem Control Ports
- Programmable NRZI Encode/Decode
- N-Bit Reception Capability

- Digital Phase Locked Loop—Clock Recovery
- Minimum CPU Overhead
- Single +5Volt Supply
- 40 Pin Package

The 8273 SDLC (Synchronous Data Link Control) Protocol controller is a single chip device designed to support the SDLC protocol within a microcomputer system environment. Its internal supervisory instruction set is oriented to frame level (SDLC) functions with a minimum of CPU overhead.

PIN CONFIGURATION

FLAG DET	1		40	Vcc
Tx INT	2		39	$\overline{PB_4}$
0 CLK	3		38	$\overline{PB_3}$
RESET	4		37	$\overline{PB_2}$
$\overline{TxDACK}$	5		36	$\overline{PB_1}$
TxDRQ	6		35	$\overline{RTS}$
$\overline{RxDACK}$	7		34	$\overline{PA_4}$
RxDRQ	8		33	$\overline{PA_3}$
$\overline{RD}$	9		32	$\overline{PA_2}$
$\overline{WR}$	10	8273 SDLC	31	$\overline{CD}$
Rx INT	11		30	$\overline{CTS}$
DB0	12		29	TxD
DB1	13		28	$\overline{TxC}$
DB2	14		27	$\overline{RxC}$
DB3	15		26	RxD
DB4	16		25	32xC
DB5	17		24	$\overline{CS}$
DB6	18		23	$\overline{DPLL}$
DB7	19		22	A_1
GND	20		21	A_0

BLOCK DIAGRAM

REGISTERS

Tx	REG	COMMAND REG
Rx	REG	PARAMETER REG
TEST MODE		STATUS REG
		RESULT REG
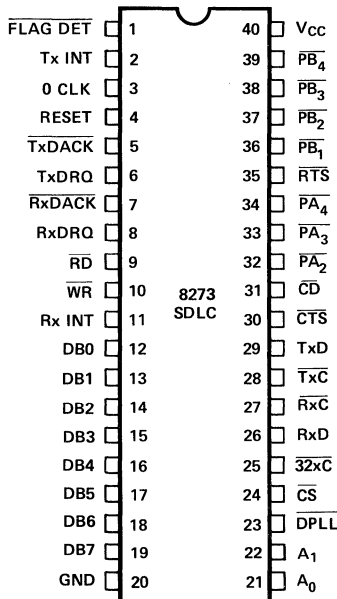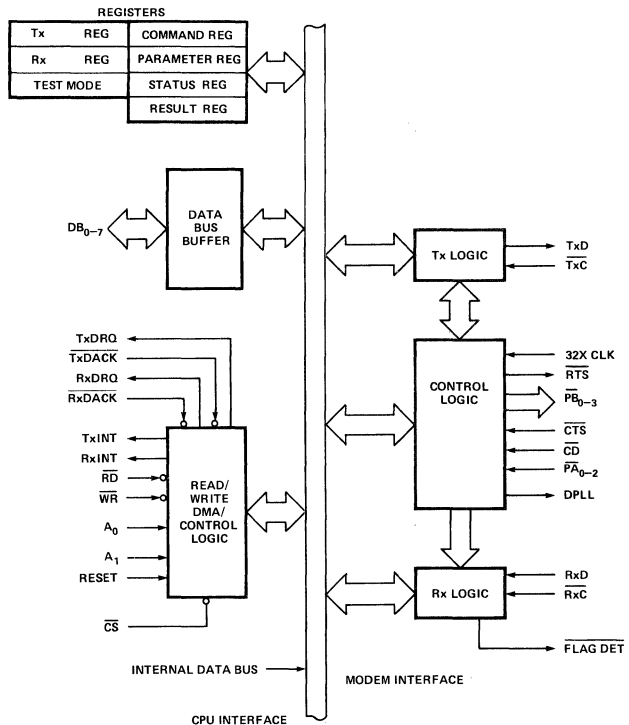
General

The IBM Synchronous Data Link Control (SDLC) communication protocol is a bit oriented communication protocol vs the BI-SYNC protocol which is character or code oriented. The SDLC protocol greatly reduces the overall CPU software on one hand and increases the throughput on the other because of its ability to go full-duplexed mode.

The 8273 SDLC chip is designed to handle the IBM SDLC protocol with minimum CPU software. The 8273 handles the zero-insertion technique used in SDLC protocol, as well as performing NRZI encoding and decoding for the data. Modem handshake signals are provided so that the CPU intervention is minimized. The FCS (Frame check sequence) is also generated and checked by the SDLC chip as well as Flags (01111110) and Idle characters.

One implementation of SDLC is the Loop-configuration typified by IBM 3650 Retail Store System which can also be handled by the 8273 by going into 1-bit delay mode. In such configuration a two wire pair can be effectively used for data transfer between controllers and loop stations. Digital phase Locked Loop pin-out can be used by the loop station without the presence of an accurate 1X clock.

Hardware Description

The 8273 is packaged in a 40 pin DIP. The following is a functional description of each pin.

Pin Name	I/O	Description
Vcc		+5V supply
GND		Ground
RESET	I	A high signal on this pin will force the 8273 to an idle state. The 8273 will remain idle until a command is issued by the CPU. The modem interface output signals are forced high.
$\overline{CS}$	I	The I/O Read and I/O Write inputs are enabled by the chip.
DB$_7$-DB$_0$	I/O	The Data Bus lines are bidirectional three-state lines.
$\overline{WR}$	I	The Write signal is used to control the transfer of either a command or data from CPU to the 8273.
$\overline{RD}$	I	The Read signal is used to control the transfer of either a data byte or a status word from the 8273 to the CPU.
TxINT	O	The Transmitter interrupt signal indicates that the transmitter logic requires service.
RxINT	O	The Receiver interrupt signal indicates that the Receiver logic requires service.

Pin Name	I/O	Description
TxDRQ	O	The Transmitter DMA Request signal indicates the transmitter Buffer is empty and is ready to transmit another data byte.
RxRDQ	O	The Receiver DMA Request signal indicates the Receiver Buffer is full.
$\overline{TxDACK}$	I	The Transmitter DMA acknowledge signal notifies the 8273 that the TxDMA cycle has been granted.
$\overline{RxDACK}$	I	The Receiver DMA acknowledge signal notifies the 8273 that the RxDMA cycle has been granted.
A$_1$-A$_0$	I	These two lines are used to select the destination or source of data to be accessed by the control logic.
TxD	O	The NRZI encoded data are transmitted through the TxD line.
$\overline{TxC}$	I	The transmitter clock controls the TxD BAUD rate.
RxD	I	The Receiver Data line receives the NRZI encoded data from the communication data channel.
$\overline{RxC}$	I	The Receiver clock is the 1X BAUD rate that RxD is received.
$\overline{32X\ CLK}$	I	The 32X clock is used to provide clock recovery when Asynchronous modem is used. In loop configuration the loop station can run without an accurate 1X clock by using the 32X CLK.
$\overline{DPLL}$	O	Digital Phase Locked Loop output can be tied to RxC and/or TxC when 1X clock is not available. DPLL is used with 32X CLK.
$\overline{FLAG\ DET}$	O	Flag Detect signals that a flag (01111110) has been detected.
$\overline{RTS}$	O	Request to send signals the terminal is ready to transmit Data.
$\overline{CTS}$	I	Clear to send signals that the modem is ready to accept data for transmission.
$\overline{CD}$	I	Carrier Detect signals that the line transmission has started and the 8273 may begin sample data on RxD line.
$\overline{PA}_{0-2}$	I	General Purpose input Ports. The logic levels on these lines can be Read by the CPU through the Data Bus Buffer.
$\overline{PB}_{0-3}$	O	General Purpose output Ports. The CPU can write these output lines through Data Bus Buffer.
ϕ CLK	I	A 4 MHz Square Wave Clock.

Principles of Operation

The 8273 is fully compatible with Intel microprocessors. It accepts commands from the CPU, executes these Commands and provides a Result at the end of execution. Communication with CPU is through the activating of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ pins. The A_1A_0 select the appropriate registers on chip:

A1	A0	CS•RD	CS•WR
0	0	Status Reg	Command Reg
0	1	Result Reg	Parameter Reg
1	0	TX Reg	—
1	1	RX Reg	—

The SDLC chip operation is composed of the following general sequence of events:

The Command Phase

During the Command Phase, the CPU issues a command byte to the 8273. The command byte provides a general description of the type of operation requested. Many operations require more detailed information about the command. In such case, from zero to four parameters are written following the command byte to provide such information. The various commands that the 8273 can recognize are listed in the Software Operation Section.

The Execution Phase

After the last parameter is written into the 8273, the SDLC chip enters the Execution Phase. During this phase there is no need for CPU involvement. The system might interface with the 8257 (DMA controller) if programmed to do so, for high speed data transfers (see System Diagram). On the other hand for low speed data rate communication TxINT and RxINT can be used.

The Result Phase

During the Result Phase, the SDLC chip notifies the CPU of the outcome of the command execution. This phase may be initiated by:

1. The successful completion of an operation.
2. An error detected during an operation.

In the Result Phase, the CPU Reads the Status Register which provides the following information.

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

- RX INTERRUPT RESULT AVAILABLE
- TX INTERRUPT RESULT AVAILABLE
- RX INTERRUPT
- TX INTERRUPT
- COMMAND RESULT BUFFER FULL
- COMMAND PARAMETER BUFFER FULL
- COMMAND BUFFER FULL
- COMMAND BUSY
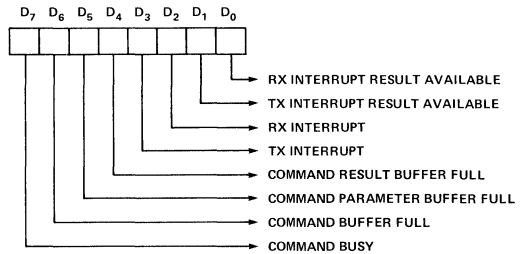
Based on the status of the Status Register, the CPU may Read the Tx Reg, Rx Reg, or Result Register, if more information is needed.

Software Operation

The 8273 can accept many powerful commands from the CPU. The following is a list of such commands (associated parameters not shown).

General Receive
Selective Receive
Selective Loop Receive
End of Polling Search
Receive Disable
Transmit Frame
Loop Transmit
Transparent Transmit
Abort Tx Frame
Abort Loop Tx
Abort Transparent Tx
Read Port A
Read Port B
Set/Reset 1 Bit Delay
Set/Reset Serial I/O
Set/Reset Operating Mode
Set/Reset Port A/B Bit
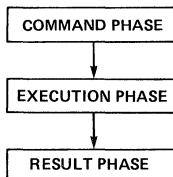
COMMAND PHASE — CPU WRITES COMMAND AND PARAMETERS INTO THE 8273 COMMAND AND PARAMETER REGISTERS.

EXECUTION PHASE — THE 8273 IS ON ITS OWN TO CARRY OUT THE COMMAND.

RESULT PHASE — THE 8273 SIGNALS THE CPU THAT THE EXECUTION HAS FINISHED. THE CPU WILL PERFORM A READ OPERATION OF ONE OR MORE OF THE REGISTERS.
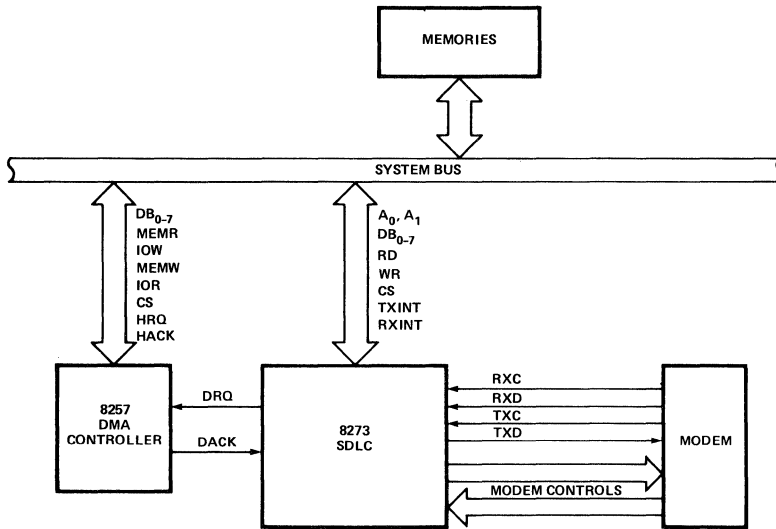
8273 SYSTEM DIAGRAM
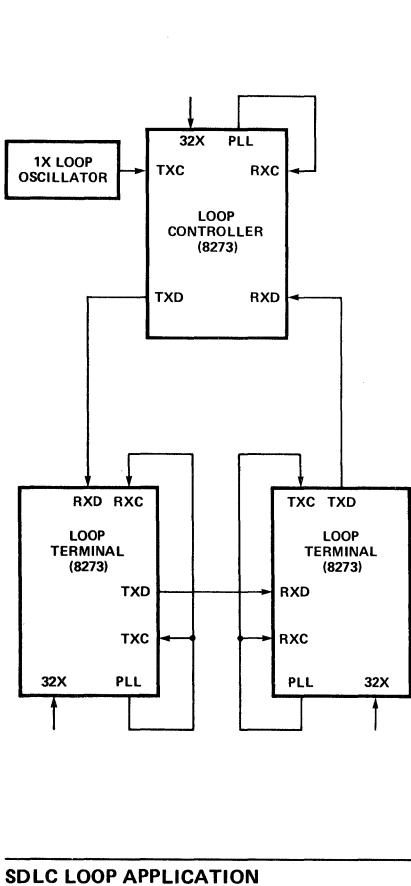
SDLC LOOP APPLICATION

SYNCHRONOUS MODEM – DUPLEX OR HALF DUPLEX OPERATION
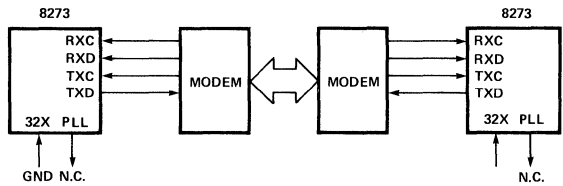
ASYNCHRONOUS MODEMS – DUPLEX OPERATION
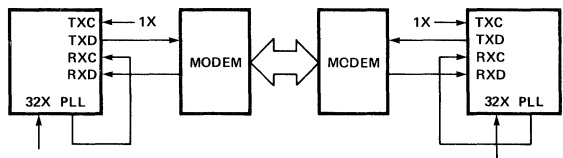
ASYNCHRONOUS MODEMS – HALF DUPLEX OPERATION
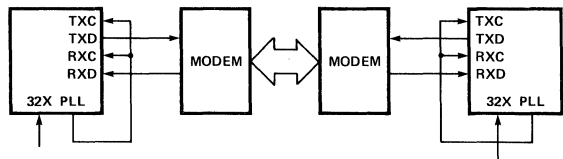
ASYNCHRONOUS OPERATION – NO MODEMS – DUPLEX OR HALF DUPLEX
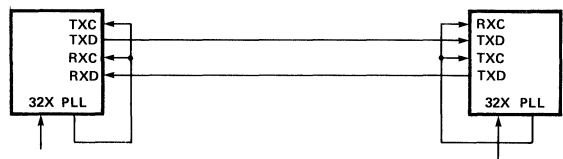
8273 MODEM OPERATION

intel®

8275
PROGRAMMABLE CRT CONTROLLER

- **Programmable Screen and Character Formats**

- **Six Indepependent Visual Field Attributes**

- **Eleven Visual Character Attributes (Graphic Capability)**

- **Cursor Control (4 Types)**

- **Light Pen Detection and Registers**

- **Dual Row Buffers**

- **Programmable DMA Burst Mode**

- **Single +5 Volt Supply**

- **40 Pin Package**

The 8275 Programmable CRT Controller is a single chip device to interface CRT Raster Scan Displays with Intel® Microcomputer Systems. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the 8275 will allow simple interface to almost any Raster Scan CRT Display with a minimum of external hardware and software overhead.

PIN CONFIGURATION

LC_3	1	40	V_{CC}
LC_2	2	39	LA_0
LC_1	3	38	LA_1
LC_0	4	37	LTEN
DRQ	5	36	RVV
$\overline{DACK}$	6	35	VSP
HRTC	7	34	GPA_1
VRTC	8	33	GPA_0
$\overline{RD}$	9	32	HLGT
$\overline{WR}$	10	31	IRQ
LPEN	11	30	CCLK
DB_0	12	29	CC_6
DB_1	13	28	CC_5
DB_2	14	27	CC_4
DB_3	15	26	CC_3
DB_4	16	25	CC_2
DB_5	17	24	CC_1
DB_6	18	23	CC_0
DB_7	19	22	CS
GND	20	21	A_0
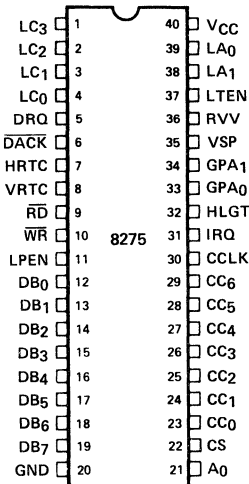
8275

BLOCK DIAGRAM
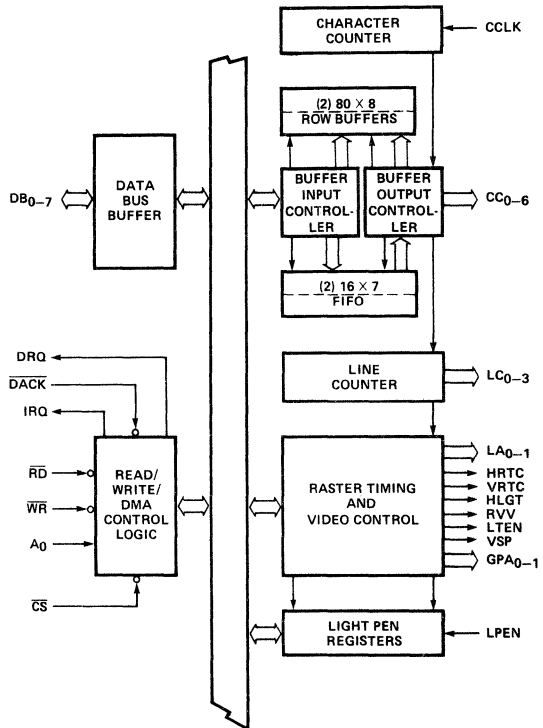
General

The CRT Controller (8275) is a single chip, programmable, NMOS-LSI device which is designed to provide an interface for microcomputers to a large class of CRT character displays. The chip provides the display row buffering, raster timing, cursor timing, light pen detection and visual attribute decoding. It is programmable to a large number of different display formats. The controller can be interfaced to standard character generator ROMs for dot matrix decoding.

The controller can generate a screen format size of from 1 to 80 characters per row, 1 to 64 rows per screen and from 1 to 16 horizontal lines per character row.

The device has 7 character code address bits allowing 6 or 7 bit ASCII capability or can be used with other 7 bit codes to generate up to 128 characters.

Hardware Description

The 8275 is Packaged in a 40 pin DIP. The following is a functional description of each pin.

Pin Name	I/O	Description
V_{cc}	—	+5V power supply
GND	—	Ground
CCLK	I	Character Clock (from dot/timing logic)
DB_7-DB_0	I/O	Bi-directional three-state data bus lines. The outputs are enabled during a read of the C or P ports.
$\overline{CS}$	I	Chip select. The read and write are enabled by $\overline{CS}$.
$\overline{RD}$	I	Read input. A control signal to read registers.
$\overline{WR}$	I	Write input. A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
A_0	I	Port Address. A high input on A_0 selects the "C" port or command registers and a low input selects the "P" port or parameter registers.
INT	O	Interrupt request.
DRQ	O	DMA request. Output signal to the 8257 DMA controller requesting a DMA cycle.
$\overline{DACK}$	I	DMA acknowledge. Input signal from the 8257 DMA controller acknowledging that the requested DMA cycle has been granted.
LPEN	I	Light pen. Input Signal from the CRT system signifying that a light pen signal has been detected.
HRTC	O	Horizontal retrace. Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.

Pin Name	I/O	Description
VRTC	O	Vertical retrace. Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
LC0-LC3	O	Line count. Output from the line counter which is used to address the character generator for the line positions on the screen.
CC0-CC6	O	Character codes. Output from the row buffers used for character selection in the character generator.
GPA0, GPA1	O	General purpose attribute codes. Outputs which are enabled by the general purpose field attribute codes.
LA0, LA1	O	Line attribute codes. These attribute codes have to be decoded externally by the dot/timing logic to generate the horizontal and vertical line combinations for the graphic displays specified by the character attribute codes.
HLGT	O	Highlight. Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.
RVV	O	Reverse video. Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
LTEN	O	Light enable. Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by the character attribute codes during generation of graphics display.
VSP	O	Video suppression. Output signal used to blank the video signal to the CRT. This output is active: — during the horizontal and vertical retrace intervals. — at the top and bottom lines of rows if the number of lines/row are greater than or equal to 9. — when an end of row or end of screen code is detected. — when a DMA underrun occurs. — at regular intervals (1/16 frame frequency for cursor, 1/32 frame frequency for character and field attributes)—to create blinking displays as specified by cursor, character attribute, or field attribute programming.

Principles of Operation

The basic elements of the CRT controller are the two row buffers (80X8), cursor position, light pen position, and visual attribute decode and control logic. The CRT controller is used with the DMA chip (8257) to provide the high speed controlling function of a CRT.

Two row buffers are utilized to provide display row refresh. Each buffer is alternately loaded from main memory and then used to provide characters to the external character generator and internal visual attribute decode logic during row display. Each buffer is loaded from main memory by DMA cycles which are requested by the CRT controller at programmable intervals. The controller can also be programmed to request a single DMA at a time or bursts of 2, 4, or 8 bytes.

Raster Control and Timing

The raster logic provides the proper video scan timing for the CRT. The various parameters of the raster timing are programmable at controller reset. Raster timing is derived from the basic character interval clock which is provided to the controller from the external dot timing logic. The following count functions are performed by the raster logic:

> Character Count
>
> Horizontal Retrace Interval Count
>
> Line Count
>
> Row Count
>
> Vertical Retrace Interval Count
>
> Blink Timing

Cursor

The cursor location is determined by the cursor line and character position registers which are loaded by command to the controller. The cursor can be programmed to appear on the display as 1) a blinking underline, 2) a blinking reverse video block, 3) a non-blinking underline, or 4) a non-blinking reverse video block.

Light Pen

When the controller detects a light pen signal, the row and character position coordinates of the raster are stored in a pair of registers. On command to the controller, these registers can be read by the microprocessor. The registers are loaded on the 0-1 transition of the light pen input which is internally synchronized with the character clock. The horizontal address will be off three character positions (more if external delays are present) and has to be corrected in the software. In addition, the controller has a status flag to indicate that the light pen signal was detected.

Visual Attributes

Visual attributes are generated and timed by the CRT controller without the intervention of the external character generator. They are actuated and controlled by special code combinations. These attribute codes can affect the display for just the character position in which they appear (character type) or they may affect a field of characters (field type).

Field Attributes

The field attributes are control codes which will affect the visual characteristics for a field of characters starting at the character following the field attribute code up to the character which precedes the next field attribute code. A field attribute code does not have to occupy a display position. Any of the following field display can be independently selected for a field:

> Blink
>
> Highlight
>
> Reverse Video
>
> Underline

Character Attributes

A character attribute generates a graphics symbol in the character position without the use of an external character generator. A character attribute is generated through the Line Attribute outputs together with the Video Suppress and Light Enable outputs. The external logic then can generate the proper symbol. Character attributes can be programmed to blink or be highlighted.

Software Operation

The 8275 can accept commands from the CPU at any time to perform the CRT controlling functions. A command (A_0=1) from the CPU to the 8275 chip may be followed by up to 4 bytes of parameters (A_0=0). The list of commands and their associated parameters are summarized below:

C/$\overline{P}$	DB	
1	0 0 0 X X X X X	RESET & STOP DISPLAY
0	S H H H H H H H	SCREEN COMPOSITION #1
0	V V R R R R R R	SCREEN COMPOSITION #2
0	U U U U L L L L	SCREEN COMPOSITION #3
0	D F C C Z Z Z Z	SCREEN COMPOSITION #4
1	0 0 1 S S S B B	START DISPLAY
1	0 1 0 X X X X X	STOP DISPLAY
1	0 1 1 X X X X X	READ LIGHT PEN (*2 $\overline{RD}$)
1	1 0 0 X X X X X	LOAD CURSOR POSITION
0	X C C C C C C C	CURSOR X-POSITION
0	X X C C C C C C	CURSOR Y-POSITION
1	1 0 1 X X X X X	ENABLE INTERRUPT
1	1 1 0 X X X X X	DISABLE INTERRUPT

MEMORIES

SYSTEM BUS

DB_{0-7}
$\overline{MEMR}$
$\overline{IOW}$
$\overline{MEMW}$
$\overline{IOR}$
$\overline{CS}$
HRQ
HACK

A_0
DB_{0-7}
$\overline{WR}$
$\overline{RD}$
$\overline{CS}$
IRQ

CHARACTER
GENERATOR
128 x 7 x 9

LC_{0-3}

8257
DMA
CONTROLLER

DRQ

$\overline{DACK}$

8275
CRT
CONTROLLER

CC_{0-6}

CHAR. CLK

HIGH
SPEED
DOT
TIMING
AND
INTERFACE

VIDEO SIGNAL

HORIZONTAL SYNC

VERTICAL SYNC

INTENSITY

VIDEO CONTROLS
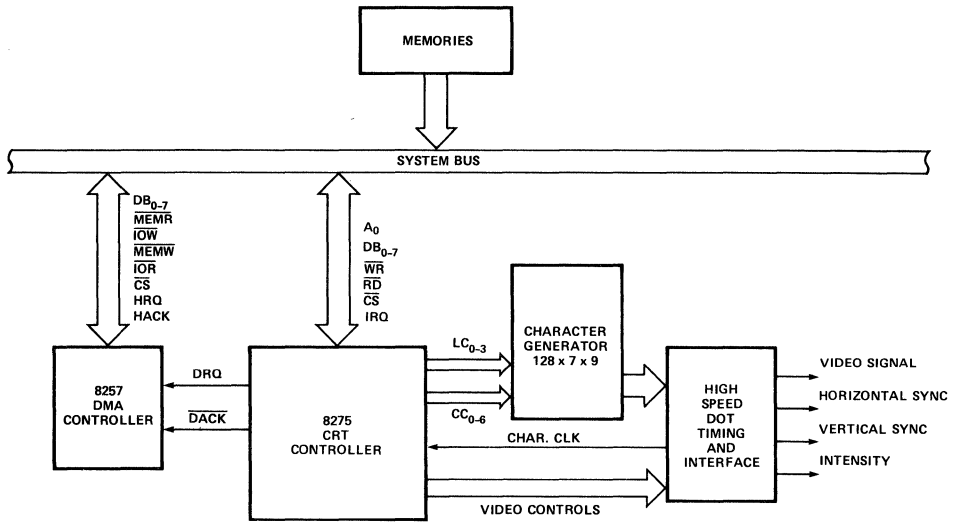
8275 SYSTEM DIAGRAM

intɘl®

8279, 8279-5
PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- **MCS-85™ Compatible 8279-5**
- **Simultaneous Keyboard Display Operations**
- **Scanned Keyboard Mode**
- **Scanned Sensor Mode**
- **Strobed Input Entry Mode**
- **8 Character Keyboard FIFO**
- **2 Key Lockout or N Key Rollover with Contact Debounce**

- **Dual 8 or 16 Numerical Display**
- **Single 16 Character Display**
- **Right or Left Entry 16 Byte Display RAM**
- **Mode Programmable from CPU**
- **Programmable Scan Timing**
- **Interrupt Output on Key Entry**

The 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel® microprocessors. The keyboard portion can provide a scanned interface to a 64 contact key matrix which can be expanded to 128. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the Hall effect and Ferrite variety. Key depressions can be 2 key lockout or N key rollover. Keyboard entries are debounced and strobed in an 8 character FIFO. If more than 8 characters are entered, over run status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has a 16 x 8 display RAM which can be organized into a dual 16 x 4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

PIN CONFIGURATION

RL$_2$	1		40	V$_{CC}$
RL$_3$	2		39	RL$_1$
CLK	3		38	RL$_0$
IRQ	4		37	CNTL/STB
RL$_4$	5		36	SHIFT
RL$_5$	6		35	SL$_3$
RL$_6$	7		34	SL$_2$
RL$_7$	8		33	SL$_1$
RESET	9	8279	32	SL$_0$
$\overline{RD}$	10		31	OUT B$_0$
$\overline{WR}$	11		30	OUT B$_1$
DB$_0$	12		29	OUT B$_2$
DB$_1$	13		28	OUT B$_3$
DB$_2$	14		27	OUT A$_0$
DB$_3$	15		26	OUT A$_1$
DB$_4$	16		25	OUT A$_2$
DB$_5$	17		24	OUT A$_3$
DB$_6$	18		23	BD
DB$_7$	19		22	CS
V$_{SS}$	20		21	A$_0$
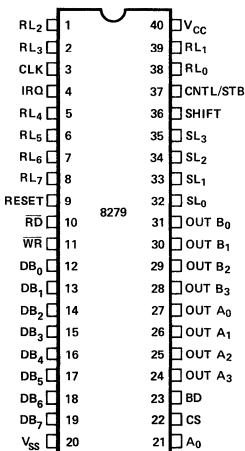
PIN NAMES

NAME	I/O	FUNCTION
DB$_{0-7}$	I/O	DATA BUS (BI-DIRECTIONAL)
CLK	I	CLOCK INPUT
RESET	I	RESET INPUT
$\overline{CS}$	I	CHIP SELECT
$\overline{RD}$	I	READ INPUT
$\overline{WR}$	I	WRITE INPUT
A$_0$	I	BUFFER ADDRESS
IRQ	O	INTERRUPT REQUEST OUTPUT
SL$_{0-3}$	O	SCAN LINES
RL$_{0-7}$	I	RETURN LINES
SHIFT	I	SHIFT INPUT
CNTL/STB	I	CONTROL/STROBE INPUT
OUT A$_{0-3}$	O	DISPLAY (A) OUTPUTS
OUT B$_{0-3}$	O	DISPLAY (B) OUTPUTS
$\overline{BD}$	O	BLANK DISPLAY OUTPUT

LOGIC SYMBOL

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.
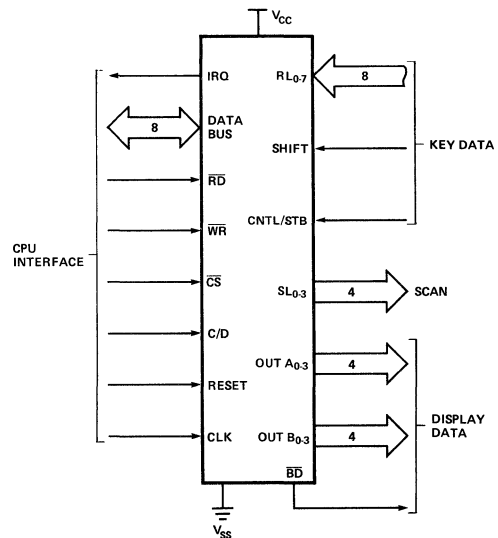
8279 BASIC FUNCTIONAL DESCRIPTION

Introduction

Since data input and display are an integral part of many microprocessor designs, the system designer needs an interface that can control these functions without placing a large load on the CPU. The 8279 provides this function for 8-bit microprocessors.

The 8279 has two sections: keyboard and display. The keyboard section can interface to regular typewriter style keyboards or random toggle or thumb switches. The display section drives alphanumeric displays or a bank of indicator lights. Thus the CPU is relieved from scanning the keyboard or refreshing the display.

The 8279 is designed to directly connect to the microprocessor bus. The CPU can program all operating modes for the 8279. These modes include:

Input Modes

- Scanned Keyboard — with encoded (8 x 8 x 4 key keyboard) or decoded (4 x 8 x 4 key keyboard) scan lines. A key depression generates a 6-bit encoding of key position. Position and shift and control status are stored in the FIFO. Keys are automatically debounced with 2-key lockout or N-key rollover.

- Scanned Sensor Matrix — with encoded (8 x 8 matrix switches) or decoded (4 x 8 matrix switches) scan lines. Key status (open or closed) stored in RAM addressable by CPU.

- Strobed Input — Data on return lines during control line strobe is transferred to FIFO.

Output Modes

- 8 or 16 character multiplexed displays that can be organized as dual 4-bit or single 8-bit.

- Right entry or left entry display formats.

Other features of the 8279 include:

- Mode programming from the CPU.

- Programmable clock to match the 8279 scan times to the CPU cycle time.

- Interrupt output to signal CPU when there is keyboard or sensor data available.

- An 8 byte FIFO to store keyboard information.

- 16 byte internal Display RAM for display refresh. This RAM can also be read by the CPU.

FIGURE 1. 8279 BLOCK DIAGRAM

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Hardware Description

The 8279 is packaged in a 40 pin DIP. The following is a functional description of each pin.

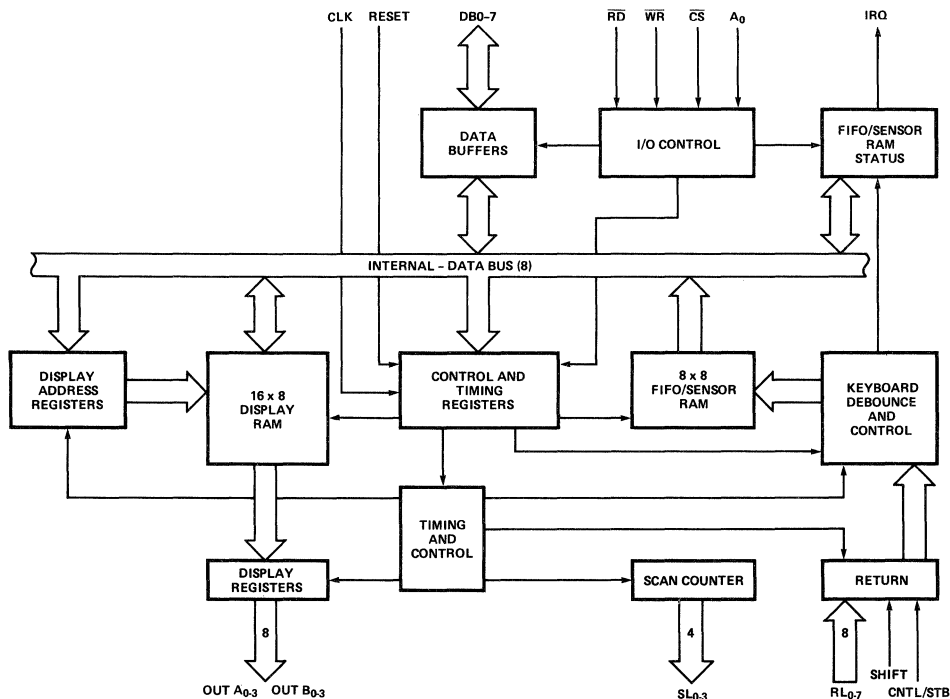| No. Of Pins	Designation	Function
8	DB_0-DB_7	Bi-directional data bus. All data and commands between the CPU and the 8279 are transmitted on these lines.
1	CLK	Clock from system used to generate internal timing.
1	RESET	A high signal on this pin resets the 8279.
1	$\overline{CS}$	Chip Select. A low on this pin enables the interface functions to receive or transmit.
1	A_0	Buffer Address. A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.
2	$\overline{RD}$, $\overline{WR}$	Input/Output read and write. These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
1	IRQ	Interrupt Request. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
2	V_{SS}, V_{CC}	Ground and power supply pins.
4	SL_0-SL_3	Scan Lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
8	RL_0-RL_7	Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.
1	SHIFT	The shift input status is stored along with the key position on key closure in the Scanned

No. Of Pins	Designation	Function
		Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.
1	CNTL/STB	For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in the Strobed Input mode. (Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low.
4	OUT A_0-OUT A_3	These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL_0-SL_3) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be considered as one 8 bit port.
4	OUT B_0-OUT B_3	
1	$\overline{BD}$	Blank Display. This output is used to blank the display during digit switching or by a display blanking command.

Principles of Operation

The following is a description of the major elements of the 8279 Programmable Keyboard/Display interface device. Refer to the block diagram in Figure 1.

I/O Control and Data Buffers

The I/O control section uses the $\overline{CS}$, A_0, $\overline{RD}$ and $\overline{WR}$ lines to control data flow to and from the various internal registers and buffers. All data flow to and from the 8279 is enabled by $\overline{CS}$. The character of the information, given or desired by the CPU, is identified by A_0. A logic one means the information is a command or status. A logic zero means the information is data. $\overline{RD}$ and $\overline{WR}$ determine the direction of data flow through the Data Buffers. The Data Buffers are bi-directional buffers that connect the internal bus to the external bus. When the chip is not selected ($\overline{CS}$ = 1), the devices are in a high impedance state. The drivers input during WR • $\overline{CS}$ and output during RD • $\overline{CS}$.

Control and Timing Registers and Timing Control

These registers store the keyboard and display modes and other operating conditions programmed by the CPU. The modes are programmed by presenting the proper command on the data lines with A_0 = 1 and then sending a $\overline{WR}$. The command is latched on the rising edge of $\overline{WR}$.

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The command is then decoded and the appropriate function is set. The timing control contains the basic timing counter chain. The first counter is a $\div N$ prescaler that can be programmed to match the CPU cycle time to the internal timing. The prescaler is software programmed to a value between 2 and 31. A value which yields an internal frequency of 100 kHz gives a 5.1 ms keyboard scan time and a 10.3 ms debounce time. The other counters divide down the basic internal frequency to provide the proper key scan, row scan, keyboard matrix scan, and display scan times.

Scan Counter

The scan counter has two modes. In the encoded mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the keyboard and display. In the decoded mode, the scan counter decodes the least significant 2 bits and provides a decoded 1 of 4 scan. Note than when the keyboard is in decoded scan, so is the display. This means that only the first 4 characters in the Display RAM are displayed.

In the encoded mode, the scan lines are active high outputs. In the decoded mode, the scan lines are active low outputs.

Return Buffers and Keyboard Debounce and Control

The 8 return lines are buffered and latched by the Return Buffers. In the keyboard mode, these lines are scanned, looking for key closures in that row. If the debounce circuit detects a closed switch, it waits about 10 msec to check if the switch remains closed. If it does, the address of the switch in the matrix plus the status of SHIFT and CONTROL are transferred to the FIFO. In the scanned Sensor Matrix modes, the contents of the return lines is directly transferred to the corresponding row of the Sensor RAM (FIFO) each key scan time. In Strobed Input mode, the contents of the return lines are transferred to the FIFO on the rising edge of the CNTL/STB line pulse.

FIFO/Sensor RAM and Status

This block is a dual function 8 x 8 RAM. In Keyboard or Strobed Input modes, it is a FIFO. Each new entry is written into successive RAM positions and each is then read in order of entry. FIFO status keeps track of the number of characters in the FIFO and whether it is full or empty. Too many reads or writes will be recognized as an error. The status can be read by an $\overline{RD}$ with $\overline{CS}$ low and A_0 high. The status logic also provides an IRQ signal when the FIFO is not empty. In Scanned Sensor Matrix mode, the memory is a Sensor RAM. Each row of the Sensor RAM is loaded with the status of the corresponding row of sensor in the sensor matrix. In this mode, IRQ is high if a change in a sensor is detected.

Display Address Registers and Display RAM

The Display Address Registers hold the address of the word currently being written or read by the CPU and the two 4-bit nibbles being displayed. The read/write addresses are programmed by CPU command. They also can be set to auto increment after each read or write. The Display RAM can be directly read by the CPU after the correct mode and address is set. The addresses for the A and B nibbles are automatically updated by the 8279 to match data entry by the CPU. The A and B nibbles can be entered independently or as one word, according to the mode that is set by the CPU. Data entry to the display can be set to either left or right entry. See Interface Considerations for details.

Software Operation

8279 Commands

The following commands program the 8279 operating modes. The commands are sent on the Data Bus with $\overline{CS}$ low and A_0 high and are loaded to the 8279 on the rising edge of $\overline{WR}$.

Keyboard/Display Mode Set

Code:

MSB							LSB
0	0	0	D	D	K	K	K

Where DD is the Display Mode and KKK is the Keyboard Mode.

DD

0	0	8 8-bit character display — Left entry
0	1	16 8-bit character display — Left entry*
1	0	8 8-bit character display — Right entry
1	1	16 8-bit character display — Right entry

For description of right and left entry, see Interface Considerations. Note that when decoded scan is set in keyboard mode, the display is reduced to 4 characters independent of display mode set.

KKK

0	0	0	Encoded Scan Keyboard — 2 Key Lockout
0	0	1	Decoded Scan Keyboard — 2-Key Lockout
0	1	0	Encoded Scan Keyboard — N-Key Rollover
0	1	1	Decoded Scan Keyboard — N-Key Rollover
1	0	0	Encoded Scan Sensor Matrix
1	0	1	Decoded Scan Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

Program Clock

Code:

0	0	1	P	P	P	P	P

Where PPPPP is the prescaler value 2 to 31. The programmable prescaler divides the external clock by PPPPP to get the basic internal frequency. Choosing a divisor that yields 100 KHz will give the specified scan and debounce times. Default after a reset pulse (but not a program clear) is 31.

Read FIFO/Sensor RAM

Code:

0	1	0	AI	X	A	A	A

X = Don't Care

Where AI is the Auto-Increment flag for the Sensor RAM and AAA is the row that is going to be read by the CPU. AI and AAA are used only if the mode is set to Sensor Matrix. This command is used to specify that the source of data reads ($\overline{CS} \bullet RD \bullet \overline{A_0}$) by the CPU is the FIFO/Sensor RAM. No additional commands are necessary as long as

Default after reset.

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data is desired from the FIFO/Sensor RAM. Another command is necessary if reading is desired from a different row than has been selected. If AI is a one, the row select counter will be incremented after each read so the next read will be from the next Sensor RAM row.

In the Auto Increment mode for reading data from the FIFO/Sensor RAM, each read advances the address by one so that the next read is from the next character. This Auto Incrementing has no effect on the display.

Read Display RAM

Code:

0	1	1	AI	A	A	A	A

Where AI is the Auto-Increment flag for the Display RAM and AAAA is the character that the CPU is going to read next. Since the CPU uses the same counter for reading and writing, this command also sets the next write location and Auto-Increment mode. This command is used to specify the display RAM as the data source for CPU data reads. If AI is set, the character address will be incremented after each read (or write) so that the next read (or write) will be from (to) the next character.

Write Display RAM

Code:

1	0	0	AI	A	A	A	A

Where AI is the Auto-Increment flag for the Display RAM and AAAA is the character that the CPU is going to write next. The addressing and Auto-Increment are identical to Read Display RAM. The difference is that Write Display RAM does not affect the source of CPU reads. The CPU will read from whichever RAM (Display or FIFO/Sensor) was last specified. This command will, however, change the location the next Display RAM read will be from if that source was specified.

Display Write Inhibit/Blanking

Code:

1	0	1	X	IW	IW	BL	BL
				A	B	A	B

Where IW is Inhibit Writing (nibble A or B) and BL is Blanking (nibble A or B). If the display is being used as a dual 4-bit display, then it is necessary to mask one of the 4-bit halves so that entries to the Display from the CPU do not affect the other half. The IW flags allow the programmer to do this. It is also useful to be able to blank either half when that half is not to be displayed. The BL flags blank the display. The next command sets the output code to be used as a "blank". Default after reset is all zeros. Note that to blank a display formatted as a single 8-bit output, it is necessary to set both BL flags to entirely blank the display. A "1" sets the flag. Reissuing the command with a "0" resets the flag.

Clear

Code:

1	1	0	C_D	C_D	C_D	C_F	C_A

Where C_D is Clear Display, C_F is Clear FIFO Status (including interrupt), and C_A is Clear All. C_D is used to

clear all positions of the Display RAM to a programmable code. All ones, all zeros and hexadecimal 20 are possible. The 2 least significant bits of C_D are also used to specify the blanking code (see below).

$$C_D \ C_D \ C_D$$

0	X	All Zeros (X = Don't Care)
1	0	AB = Hex 20 (0010 0000)
1	1	All Ones

Enable clear display when = 1 (or by C_A = 1)
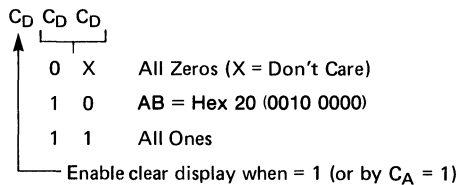
Clearing the display takes one display scan. During this time the CPU cannot write to the Display RAM. The MSB of the FIFO status word will be set during this time.

C_F set the FIFO status to empty and resets the interrupt output line. After execution of a clear command with C_F set, the Sensor Matrix mode RAM pointer will be set to row 0.

C_A has the combined effect of C_D and C_F. C_A uses the C_D clearing code to determine how to clear the Display RAM. C_A also resets the internal timing chain to resynchronize it.

End Interrupt/Error Mode Set

Code:

1	1	1	E	X	X	X	X

X = Don't care.

For the sensor matrix modes this command lowers the IRQ line and enables further writing into RAM. (The IRQ line would have been raised upon the detection of a change in a sensor value. This would have also inhibited further writing into the RAM until reset).

For the N-key rollover mode — if the E bit is programmed to "1" the chip will operate in the special Error mode. (For further details, see Interface Considerations Section.)

Status Word

The status word contains the FIFO status, error, and display unavailable signals. This word is read by the CPU when A_0 is high and $\overline{CS}$ and $\overline{RD}$ are low. See Interface Considerations for more detail on status word.

Data Read

Data is read when A_0, $\overline{CS}$ and $\overline{RD}$ are all low. The source of the data is specified by the Read FIFO or Read Display commands. The trailing edge of $\overline{RD}$ will cause the address of the RAM being read to be incremented if the Auto-Increment flag is set. FIFO reads always increment (if no error occurs) independent of AI.

Data Write

Data that is written with A_0, $\overline{CS}$ and $\overline{WR}$ low is always written to the Display RAM. The address is specified by the latest Read Display or Write Display command. Auto-Incrementing on the rising edge of $\overline{WR}$ occurs if AI set by the latest display command.

INTERFACE CONSIDERATIONS

A. Scanned Keyboard Mode, 2-Key Lockout

There are three possible combinations of conditions that can occur during debounce scanning. When a key is depressed, the debounce logic is set. A full scan of the keyboard is ignored, then other depressed keys are looked for. If none are encountered, it is a single key depression and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If the FIFO was empty, IRQ will be set to signal the CPU that there is an entry in the FIFO. If the FIFO was full, the key will not be entered and the error flag will be set. If another closed switch is encountered, no entry to the FIFO can occur. If all other keys are released before this one, then it will be entered to the FIFO. If this key is released before any other, it will be entirely ignored. A key is entered to the FIFO only once per depression, no matter how many keys were pressed along with it or in what order they were released. If two keys are depressed within the debounce cycle, it is a simultaneous depression. Neither key will be recognized until one key remains depressed alone. The last key will be treated as a single key depression.

B. Scanned Keyboard Mode, N-Key Rollover

With N-key Rollover each key depression is treated independently from all others. When a key is depressed, the debounce circuit waits 2 keyboard scans and then checks to see if the key is still down. If it is, the key is entered into the FIFO. Any number of keys can be depressed and another can be recognized and entered into the FIFO. If a simultaneous depression occurs, the keys are recognized and entered according to the order the keyboard scan found them.

C. Scanned Keyboard — Special Error Modes

For N-key rollover mode the user can program a special error mode. This is done by the "End Interrupt/Error Mode Set" command. The debounce cycle and key-validity check are as in normal N-key mode. If during a single debounce cycle, two keys are found depressed, this is considered a simultaneous multiple depression, and sets an error flag. This flag will prevent any further writing into the FIFO and will set interrupt (if not yet set). The error flag could be read in this mode by reading the FIFO STATUS word. (See "FIFO STATUS" for further details.) The error flag is reset by sending the normal CLEAR command with $C_F = 1$.

D. Sensor Matrix Mode

In Sensor Matrix mode, the debounce logic is inhibited. The status of the sensor switch is inputted directly to the Sensor RAM. In this way the Sensor RAM keeps an image of the state of the switches in the sensor matrix. Although debouncing is not provided, this mode has the advantage that the CPU knows how long the sensor was closed and when it was released. A keyboard mode can only indicate a validated closure. To make the software easier, the designer should functionally group the sensors by row since this is the format in which the CPU will read them.

The IRQ line goes high if any sensor value change is detected at the end of a sensor matrix scan. The IRQ line is cleared by the first data read operation if the Auto- Increment flag is set to zero, or by the End Interrupt command if the Auto-Increment flag is set to one.

Note: Multiple changes in the matrix Addressed by (SL_{0-3} = 0) may cause multiple interrupts. (SL_0 = 0 in the Decoded Mode). Reset may cause the 8279 to see multiple changes.

E. Data Format

In the Scanned Keyboard mode, the character entered into the FIFO corresponds to the position of the switch in the keyboard plus the status of the CNTL and SHIFT lines. CNTL is the MSB of the character and SHIFT is the next most significant bit. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to which return line the key was connected.

MSB				LSB
CNTL	SHIFT	SCAN	RETURN	

SCANNED KEYBOARD DATA FORMAT
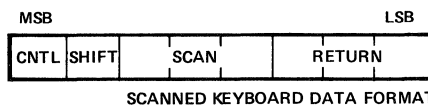
In Sensor Matrix mode, the data on the return lines is entered directly in the row of the Sensor RAM that corresponds to the row in the matrix being scanned. Therefore, each switch postion maps directly to a Sensor RAM position. The SHIFT and CNTL inputs are ignored in this mode. Note that switches are not necessarily the only thing that can be connected to the return lines in this mode. Any logic that can be triggered by the scan lines can enter data to the return line inputs. Eight multiplexed input ports could be tied to the return lines and scanned by the 8279.

MSB							LSB
RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0
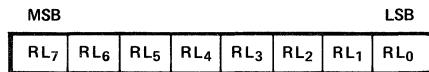
In Strobed Input mode, the data is also entered to the FIFO from the return lines. The data is entered by the rising edge of a CNTL/STB line pulse. Data can come from another encoded keyboard or simple switch matrix. The return lines can also be used as a general purpose strobed input.

MSB							LSB
RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0
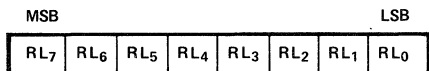
F. Display

Left Entry

Left Entry mode is the simplest display format in that each display position directly corresponds to a byte (or nibble) in the Display RAM. Address 0 in the RAM is the left-most display character and address 15 (or address 7 in 8 character display) is the right most display character. Entering characters from position zero causes the display to fill from the left. The 17th (9th) character is entered back in the left most position and filling again proceeds from there.

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Notice: This is not a final specification. Some parametric limits are subject to change.

LEFT ENTRY MODE
(AUTO INCREMENT)

1st entry — Display RAM Address 0 1 ... 14 15: [1]

2nd entry — 0 1 ... 14 15: [1][2]

16th entry — 0 1 ... 14 15: [1][2] ... [15][16]

17th entry — 0 1 ... 14 15: [17][2] ... [15][16]

18th entry — 0 1 ... 14 15: [17][18] ... [15][16]

1st entry — Display RAM Address 0 1 2 3 4 5 6 7: [1]

2nd entry — 0 1 2 3 4 5 6 7: [1][2]

Command 10010101 — 0 1 2 3 4 5 6 7: [1][2]

Enter next at Location 5 Auto Increment

3rd entry — 0 1 2 3 4 5 6 7: [1][2] [3]

4th entry — 0 1 2 3 4 5 6 7: [1][2] [3][4]

LEFT ENTRY MODE
(AUTO INCREMENT)

Right Entry

Right entry is the method used by most electronic calculators. The first entry is placed in the right most display character. The next entry is also placed in the right most character after the display is shifted left one character. The left most character is shifted off the end and is lost.

1st entry — Display RAM Address 1 2 ... 14 15 0: [ ][1]

2nd entry — 2 3 ... 15 0 1: [1][2]

3rd entry — 3 4 ... 0 1 2: [1][2][3]

16th entry — 0 1 ... 13 14 15: [1][2] ... [14][15][16]

17th entry — 1 2 ... 14 15 0: [2][3] ... [15][16][17]

18th entry — 2 3 ... 15 0 1: [3][4] ... [16][17][18]

RIGHT ENTRY MODE
(AUTO INCREMENT)

Note that now the display position and register address do not correspond. Consequently, entering a character to an arbitrary position in the Auto Increment mode may have unexpected results. Entry starting at Display RAM address 0 with sequential entry is recommended.

Auto Increment

In the Left Entry mode, Auto Incrementing causes the address where the CPU will next write to be incremented by one and the character appears in the next location. With non-Auto Incrementing the entry is both to the same RAM address and display position. Entry to an arbitrary address in the Auto Increment mode has no undesirable side effects and the result is predictable:

In the Right Entry mode, Auto Incrementing and non Incrementing have the same effect as in the Left Entry except if the address sequence is interrupted:

1st entry — Display RAM Address 1 2 3 4 5 6 7 0: [1]

2nd entry — 2 3 4 5 6 7 0 1: [1][2]

Command 10010101 — 2 3 4 5 6 7 0 1: [1][2]

Enter next at Location 5 Auto Increment

3rd entry — 3 4 5 6 7 0 1 2: [3] [1][2]

4th entry — 4 5 6 7 0 1 2 3: [3][4] [1][2]

RIGHT ENTRY MODE
(AUTO INCREMENT)

Starting at an arbitrary location operates as shown below:

Command 10010101 — Display RAM Address 0 1 2 3 4 5 6 7: [ ]

Enter next at Location 5 Auto Increment

1st entry — 1 2 3 4 5 6 7 0: [1]

2nd entry — 2 3 4 5 6 7 0 1: [1][2]

8th entry — [4][5][6][7][8][1][2][3]

9th entry — [5][6][7][8][9][2][3][4]

RIGHT ENTRY MODE
(AUTO INCREMENT)

Entry appears to be from the initial entry point.

8/16 Character Display Formats

If the display mode is set to an 8 character display, the on duty-cycle is double what it would be for a 16 character display (e.g., 5.1 ms scan time for 8 characters vs. 10.3 ms for 16 characters with 100 kHz internal frequency).
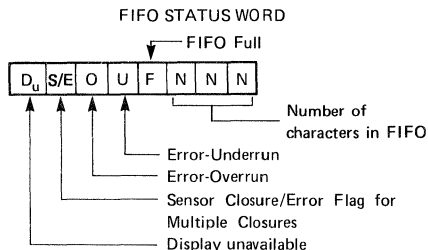
G. FIFO Status

FIFO status is used in the Keyboard and Strobed Input modes to indicate the number of characters in the FIFO and to indicate whether an error has occurred. There are two types of errors possible: overrun and underrun. Overrun occurs when the entry of another character into a full FIFO is attempted. Underrun occurs when the CPU tries to read an empty FIFO.

The FIFO status word also has a bit to indicate that the Display RAM was unavailable because a Clear Display or Clear All command had not completed its clearing operation.

In a Sensor Matrix mode, a bit is set in the FIFO status word to indicate that at least one sensor closure indication is contained in the Sensor RAM.

In Special Error Mode the S/E bit is showing the error flag and serves as an indication to whether a simultaneous multiple closure error has occurred.

FIFO STATUS WORD
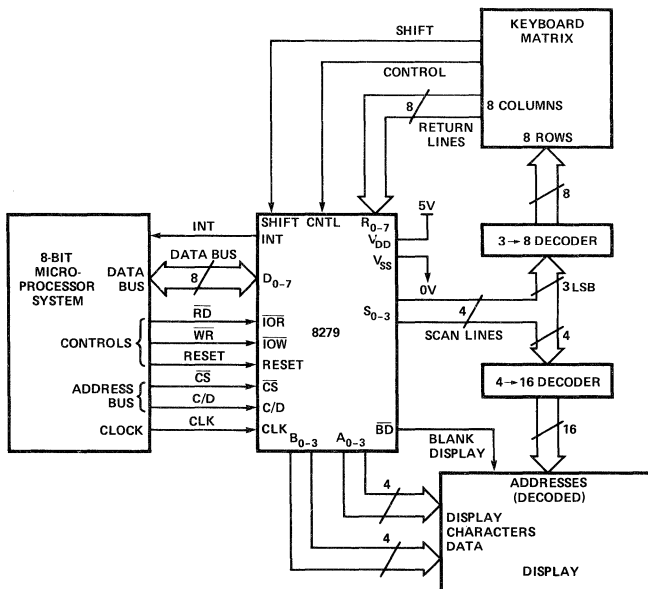
| D_u | S/E | O | U | F | N | N | N |

- FIFO Full
- Number of characters in FIFO
- Error-Underrun
- Error-Overrun
- Sensor Closure/Error Flag for Multiple Closures
- Display unavailable

APPLICATIONS

FIGURE 2. GENERAL BLOCK DIAGRAM

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature . . . . 0°C to 70°C
Storage Temperature . . . . -65°C to 125°C
Voltage on any Pin with
  Respect to Ground . . . . -0.5V to +7V
Power Dissipation . . . . .1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS $T_A = 0°C$ to 70°C, $V_{SS} = 0V$, Note 1

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL1}	Input Low Voltage for Shift Control and Return Lines	-0.5	1.4	V	
V_{IL2}	Input Low Voltage for All Others	-0.5	0.8	V	
V_{IH1}	Input High Voltage for Shift, Control and Return Lines	2.2		V	
V_{IH2}	Input High Voltage for All Others	2.0		V	
V_{OL}	Output Low Voltage		0.45	V	Note 2
V_{OH}	Output High Voltage on Interrupt Line	3.5		V	Note 3
I_{IL1}	Input Current on Shift, Control and Return Lines		+10 / -100	μA / μA	$V_{IN} = V_{CC}$ / $V_{IN} = 0V$
I_{IL2}	Input Leakage Current on All Others		±10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ to 0V
I_{CC}	Power Supply Current		120	mA	

Notes:
1. 8279, $V_{CC} = +5V \pm 5\%$; 8279-5, $V_{CC} = +5V \pm 10\%$.
2. 8279, $I_{OL} = 1.6mA$; 8279-5, $I_{OL} = 2.2mA$.
3. 8279, $I_{OH} = -100\mu A$; 8279-5, $I_{OH} = -400\mu A$.

CAPACITANCE

SYMBOL	TEST	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{in}	Input Capacitance	5	10	pF	$V_{in} = V_{CC}$
C_{out}	Output Capacitance	10	20	pF	$V_{out} = V_{CC}$

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{SS} = 0V$, (Note 1)

BUS PARAMETERS

READ CYCLE:

Symbol	Parameter	8279		8279-5		Unit
		Min.	Max.	Min.	Max.	
t_{AR}	Address Stable Before $\overline{READ}$	50		0		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		0		ns
t_{RR}	$\overline{READ}$ Pulse Width	420		250		ns
t_{RD}[2]	Data Delay from $\overline{READ}$		300		150	ns
t_{AD}[2]	Address to Data Valid		450		250	ns
t_{DF}	$\overline{READ}$ to Data Floating	10	100	10	100	ns
t_{RCY}	Read Cycle Time	1		1		μs

WRITE CYCLE:

Symbol	Parameter	8279		8279-5		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Stable Before $\overline{WRITE}$	50		0		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	20		0		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		250		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		150		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		0		ns

Notes:
1. 8279, $V_{CC} = +5V \pm 5\%$; 8279-5, $V_{CC} = +5V \pm 10\%$.
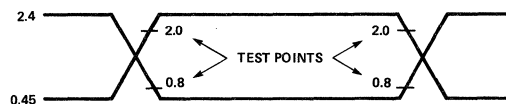2. 8279, $C_L = 100pF$; 8279-5, $C_L = 150pF$.

OTHER TIMINGS:

Symbol	Parameter	8279		8279-5		Unit
		Min.	Max.	Min.	Max.	
$t_{\phi W}$	Clock Pulse Width	230		120		nsec
t_{CY}	Clock Period	500		320		nsec

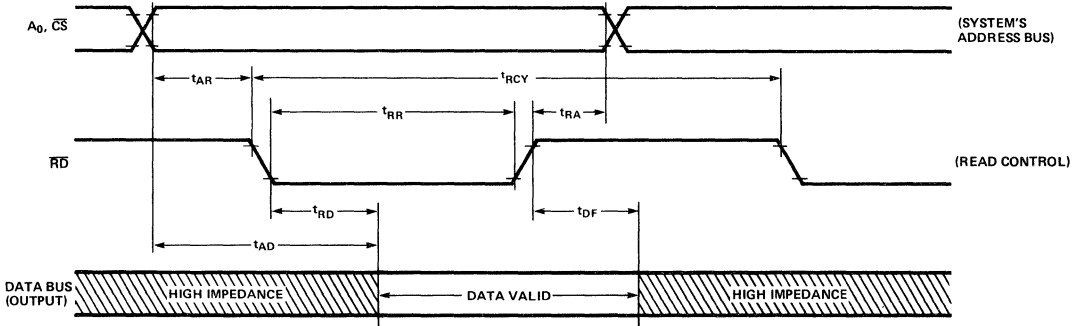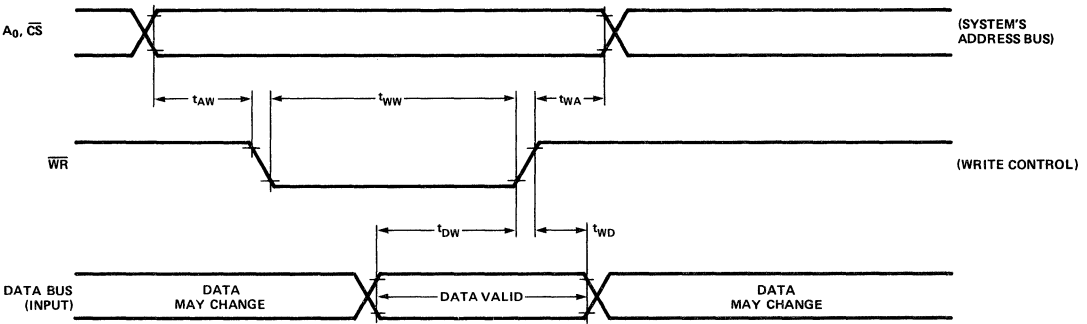|			
Keyboard Scan Time:	5.1 msec	Digit-on Time:	480 μsec
Keyboard Debounce Time:	10.3 msec	Blanking Time:	160 μsec
Key Scan Time:	80 μsec	Internal Clock Cycle:	10 μsec
Display Scan Time:	10.3 msec		

INPUT WAVEFORMS FOR A.C. TESTS:

PRELIMINARY

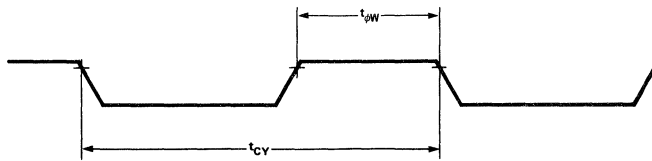Notice: This is not a final specification. Some parametric limits are subject to change.
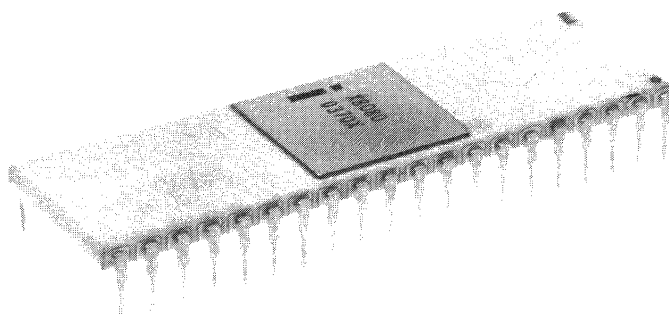
WAVEFORMS

1. Read Operation

2. Write Operation

3. Clock Input

MEMORY and I/O EXPANDERS FOR MCS-85™

MEMORY and I/O EXPANDERS FOR MCS-85™

intel®

8155/8156
2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

8155 — Active Low Chip Enable ($\overline{CE}$)
8156 — Active High Chip Enable (CE)

### ∗Directly Compatible With 8085 CPU

- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports

- 1 Programmable 6 Bit I/O Port
- Programmable 14 Bit Binary Counter/Timer
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 8156 are RAM and I/O chips to be used in the MCS-85™ microcomputer system. The RAM portion is designed with 2K bit static cells organized as 256 x 8. They have a maximum access time of 400ns to permit use with no wait states in 8085 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14 bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system. It operates in binary countdown mode, and its timer modes are programmable.

PIN CONFIGURATION
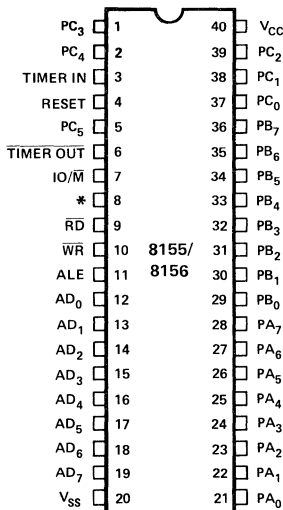
BLOCK DIAGRAM
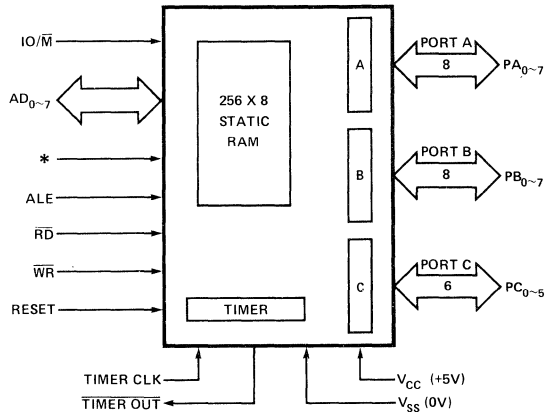
∗ : 8155 = $\overline{CE}$, 8156 = CE

8155/8156 FUNCTIONAL PIN DEFINITION

The following describes the functions of all of the 8155/8156 pins.

Symbol	Function
RESET	The Reset signal is a pulse provided by the 8085 to initialize the system. Input high on this line resets the chip and initializes the three I/O ports to **input mode. The width of RESET pulse should typically be 600 nsec. (Two 8085 clock cycle times).**
AD_{0-7}	These are 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch on the falling edge of the ALE. The address can be either for the memory section or the I/O section depending on the polarity of the $IO/\overline{M}$ input signal. The 8-bit data is either written into the chip or Read from the chip depending on the status of $\overline{WRITE}$ or $\overline{READ}$ input signal.
CE or $\overline{CE}$	Chip Enable: On the 8155, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$	Input low on this line with the Chip Enable active enables the AD_{0-7} buffers. If $IO/\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port will be read to the AD bus.
$\overline{WR}$	Input low on this line with the Chip Enable active causes the data on the AD lines to be written to the RAM or I/O ports depending on the polarity of $IO/\overline{M}$.
ALE	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and $IO/\overline{M}$ into the chip at the falling edge of ALE.
$IO/\overline{M}$	$IO/\overline{Memory}$ Select: This line selects the memory if low and selects the IO if high.

Symbol	Function
$PA_{0-7}(8)$	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status Register.
$PB_{0-7}(8)$	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status Register.
$PC_{0-5}(6)$	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the C/S Register. When PC_{0-5} are used as control signals, they will provide the following: $PC0$ — A INTR (Port A Interrupt) $PC1$ — A BF (Port A Buffer full) $PC2$ — $\overline{A STB}$ (Port A Strobe) $PC3$ — B INTR (Port B Interrupt) $PC4$ — B BF (Port B Buffer Full) $PC5$ — $\overline{B STB}$ (Port B Strobe)
TIMER IN	This is the input to the counter timer.
$\overline{\text{TIMER OUT}}$	This pin is the timer output. This output can be either a square wave or a pulse depending on the timer mode.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

OPERATIONAL DESCRIPTION

The 8155/8156 includes the following operational features:

- 2K Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit binary down counter

The I/O portion contains four registers (Command/Status, PA_{0-7}, PB_{0-7}, PC_{0-5}). The IO/M (IO/Memory Select) pin selects the I/O or the memory (RAM) portion. Detailed descriptions of memory, I/O ports and timer functions will follow.

The 8-bit address on the AD lines, the Chip Enable input, and IO/$\overline{M}$ are all latched on chip at the falling edge of ALE. A low on the IO/$\overline{M}$ must be provided to select the memory section.
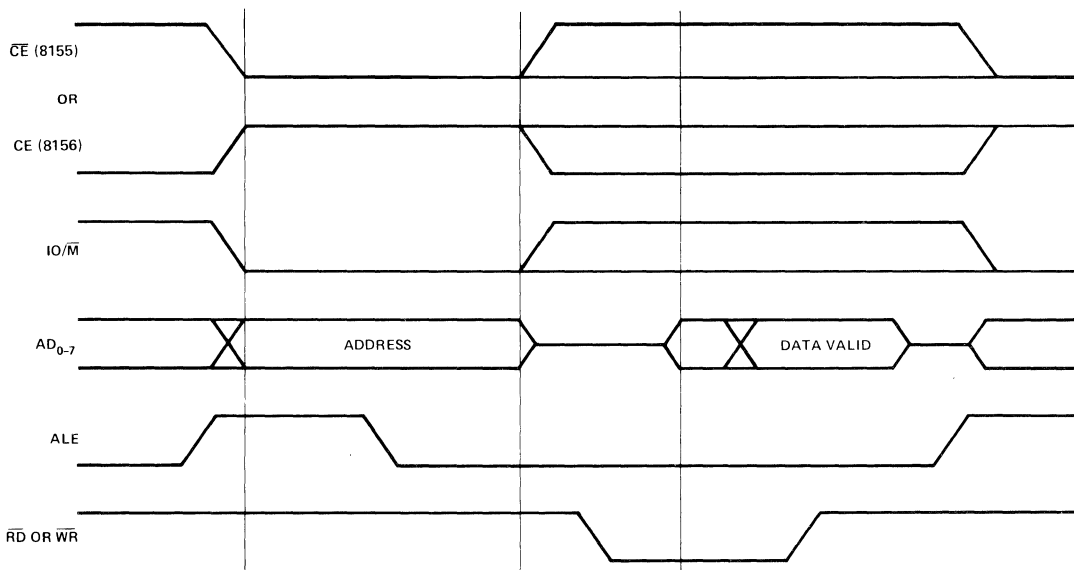
NOTE: FOR DETAILED TIMING DIAGRAM INFORMATION, SEE FIGURE 7 AND A.C. CHARACTERISTICS.

FIGURE 1. MEMORY READ/WRITE CYCLE.

PROGRAMMING OF THE COMMAND/STATUS REGISTER

The command register consists of eight latches one for each bit. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The C/S register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation. The meaning of each bit of the command byte is defined as follows:

READING THE COMMAND/STATUS REGISTER

The status register consists of seven latches one for each bit; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the C/S Register (Address XXXXX000). Status word format is shown below:
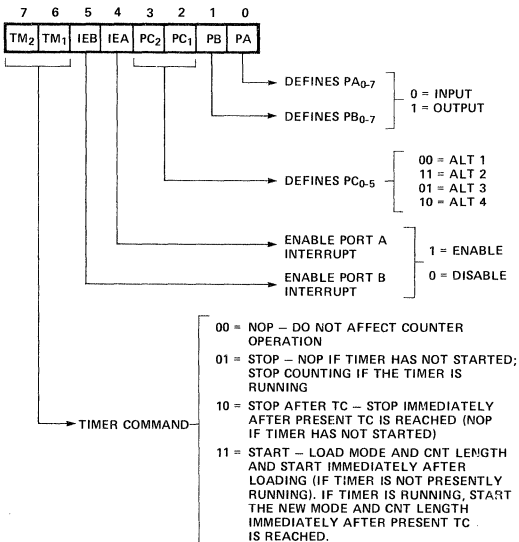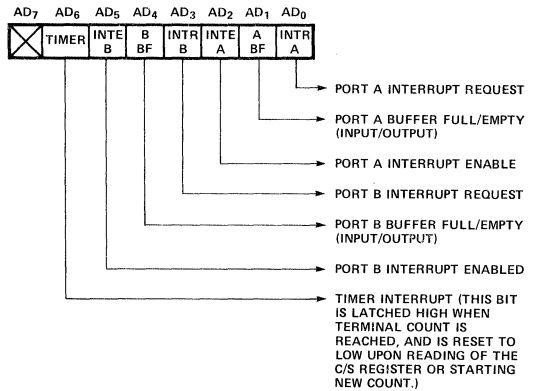

FIGURE 2. COMMAND/STATUS REGISTER BIT ASSIGNMENT.

FIGURE 3. COMMAND/STATUS REGISTER STATUS WORD FORMAT.

INPUT/OUTPUT SECTION

The I/O section of the 8155/8156 consists of four registers as described below.

- **Command/Status Register (C/S)** — This register is assigned the address XXXXX000. The C/S address serves the dual purpose.

    When the C/S register is selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins.

    When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer become available on the AD_{0-7} lines.

- **PA Register** — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.

- **PB Register** — This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010.

- **PC Register** — This register has the address XXXXX011 and contains only 6-bits. The 6-bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S register.

    When PC_{0-5} is used as a control port, 3-bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the 8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. See Table 1.

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

The following diagram shows how I/O PORTS A and B are structured within the 8155 and 8156:

8155/8156
ONE BIT OF PORT A OR PORT B

NOTES:
(1) OUTPUT MODE
(2) SIMPLE INPUT   } MULTIPLEXER CONTROL
(3) STROBED INPUT

(4) = 1 FOR OUTPUT MODE
    = 0 FOR INPUT MODE

READ PORT = (IO/$\overline{M}$=1) • ($\overline{RD}$=0) • (CE ACTIVE) • (PORT ADDRESS SELECTED)
WRITE PORT = (IO/$\overline{M}$=1) • ($\overline{WR}$=0) • (CE ACTIVE) • (PORT ADDRESS SELECTED)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the 8155/56 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

TABLE 1. TABLE OF PORT CONTROL ASSIGNMENT.

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{STB}$ (Port A Strobe)	A $\overline{STB}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{STB}$ (Port B Strobe)

The set and reset of INTR and BF with respect to $\overline{STB}$, $\overline{WR}$ and $\overline{RD}$ timing is shown in Figure 8.

To summarize, the registers' assignments are:

Address	Pinouts	Functions	No. of Bits
XXXXX000	Internal	Command/Status Register	8
XXXXX001	PA_{0-7}	General Purpose I/O Port	8
XXXXX010	PB_{0-7}	General Purpose I/O Port	8
XXXXX011	PC_{0-5}	General Purpose I/O Port or Control Lines	6

TIMER SECTION

The timer is a 14-bit counter that counts the 'timer input' pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register.

The timer addresses serve a dual purpose. During WRITE operation, a COUNT LENGTH REGISTER (CLR) with a count length (bits 0-13) and a timer mode (bits 14-15) are loaded. During READ operation the contents of the counter (the present count) and the mode bits are read.

To be sure that the right content of the counter is read, it is preferable to stop counting, read it, and then load it again and continue counting.

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 will specify the length of the next count and bits 14-15 will specify the timer output mode.

There are four modes to choose from:

0. Puts out low during second half of count.
1. Square wave
2. Single pulse upon TC being reached
3. Repetitive single pulse everytime TC is readied and automatic reload of counter upon TC being reached, until instructed to stop by a new command loaded into C/S.

Bits 6-7 of Command/Status Register Contents are used to start and stop the counter. There are four commands to choose from:

Note: See the further description on Command/Status Register.

C/S7	C/S6	
0	0	NOP — Do not affect counter operation.
0	1	STOP — NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC — Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START — Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

TIMER MODE **MSB OF CNT LENGTH**

LSB OF CNT LENGTH
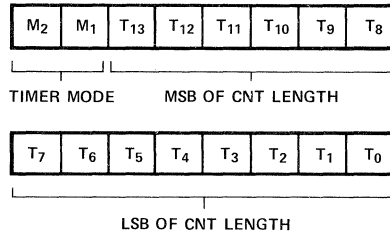
FIGURE 4. TIMER FORMAT

$M2$ $M1$ defines the timer mode as follows:

M2	M1	
0	0	Puts out low during second half of count.
0	1	Square wave, i.e., the period of the square wave equals the count length programmed with automatic reload at terminal count.
1	0	Single pulse upon TC being reached.
1	1	Automatic reload, i.e., single pulse everytime TC is reached.

Note: In case of an asymmetric count, i.e. 9, larger half of the count will be high, the larger count will stay active as shown in Figure 5.
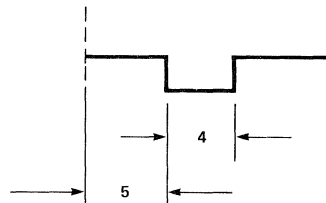
Note: 5 and 4 refer to the number of clock cycles in that time period.

FIGURE 5. ASYMMETRIC COUNT.

The timer in the 8155 is not initialized to any particular mode when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until the desired mode and count length and START command are issued.

8085 MINIMUM SYSTEM CONFIGURATION

Figure 6 shows that a minimum system is possible using only three chips:

- 256 Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 4 Interrupt Levels

FIGURE 6. 8085 MINIMUM SYSTEM CONFIGURATION.
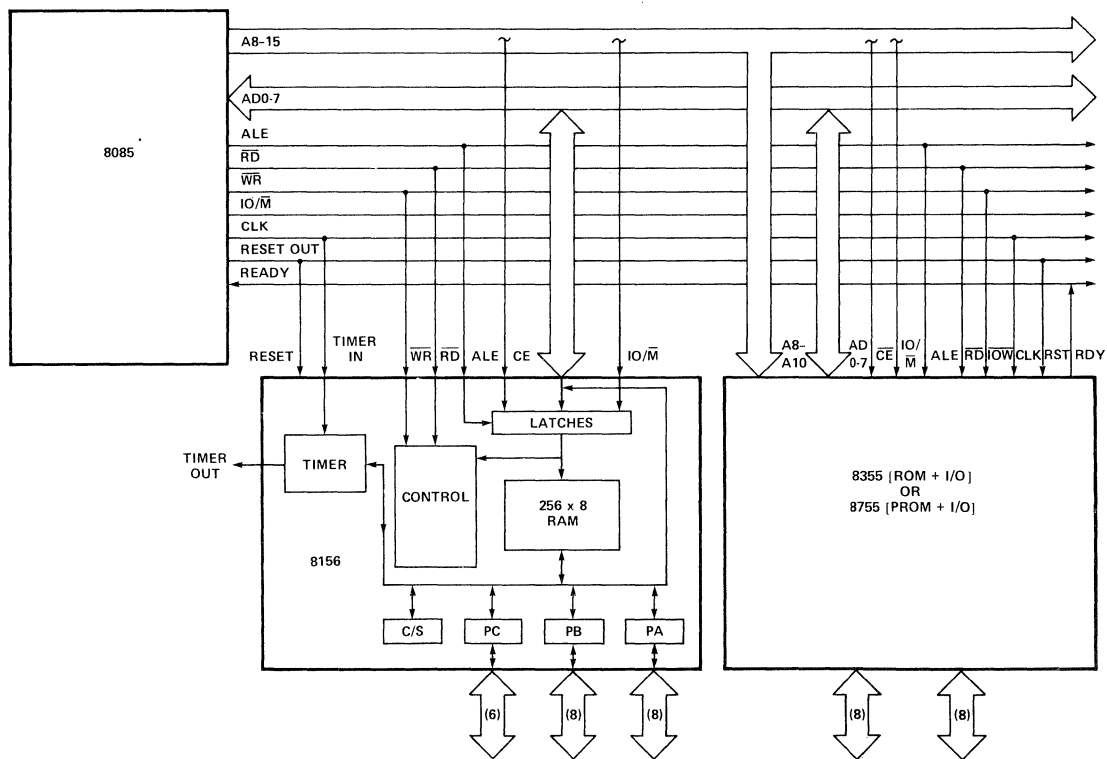
ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... 0°C to +70°C
Storage Temperature .... -65°C to +150°C
Voltage on Any Pin
  With Respect to Ground .... -0.3V to +7V
Power Dissipation 1.5W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA
I_{IL}	Input Leakage		10	µA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	µA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS $(T_A = 0°C \text{ to } 70°C; V_{CC} = 5V \pm 5\%)$

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{AL}	Address to Latch Set Up Time	50		ns	
t_{LA}	Address Hold Time after Latch	80		ns	
t_{LC}	Latch to READ/WRITE Control	100		ns	
t_{RD}	Valid Data Out Delay from READ Control		150	ns	
t_{AD}	Address Stable to Data Out Valid		400	ns	
t_{LL}	Latch Enable Width	100		ns	
t_{RDF}	Data Bus Float After READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		ns	
t_{CC}	READ/WRITE Control Width	250		ns	
t_{DW}	Data In to WRITE Set Up Time	150		ns	
t_{WD}	Data In Hold Time After WRITE	0		ns	
t_{RV}	Recovery Time Between Controls	300		ns	
t_{WP}	WRITE to Port Output		400	ns	
t_{PR}	Port Input Setup Time	50		ns	
t_{RP}	Port Input Hold Time	50		ns	150 pF Load
t_{SBF}	Strobe to Buffer Full		400	ns	
t_{SS}	Strobe Width	200		ns	
t_{RBE}	READ to Buffer Empty		400	ns	
t_{SI}	Strobe to INTR On		400	ns	
t_{RDI}	READ to INTR Off		400	ns	
t_{PSS}	Port Setup Time to Strobe Strobe	50		ns	
t_{PHS}	Port Hold Time After Strobe	100		ns	
t_{SBE}	Strobe to Buffer Empty		400	ns	
t_{WBF}	WRITE to Buffer Full		400	ns	
t_{WI}	WRITE to INTR Off		400	ns	
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low	400		ns	
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High	400		ns	
t_{RDE}	Data Bus Enable from READ Control	10		ns	

Note: For Timer Input Specification, see Figure 10.

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

A. READ CYCLE
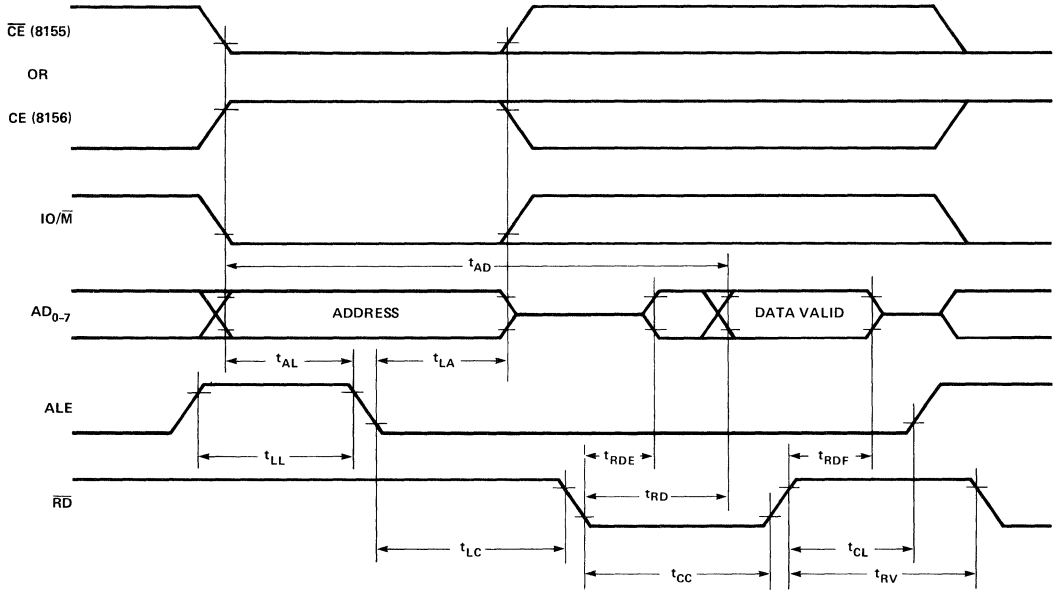
B. WRITE CYCLE
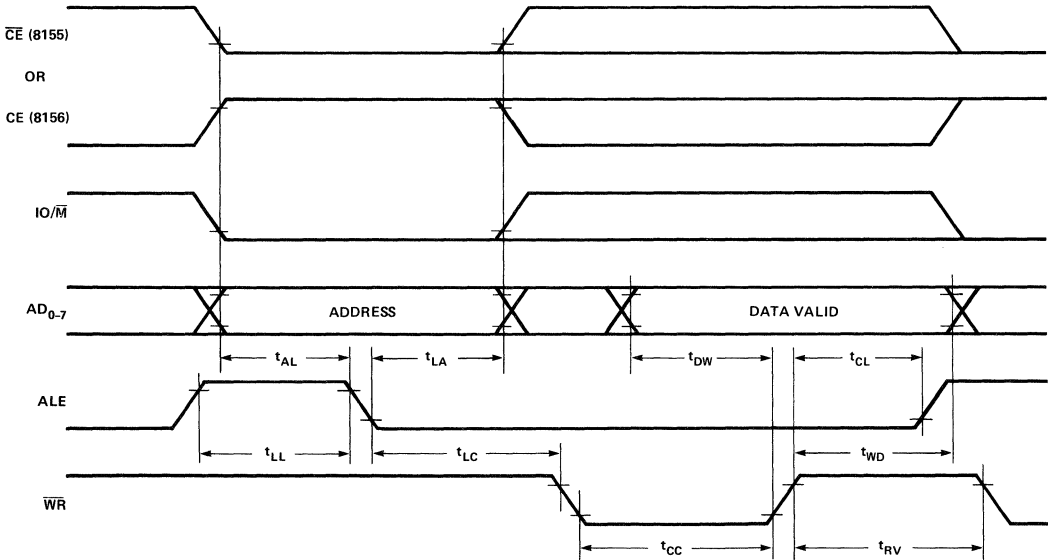
FIGURE 7. 8155/8156 READ/WRITE TIMING DIAGRAMS.

A. STROBED INPUT MODE
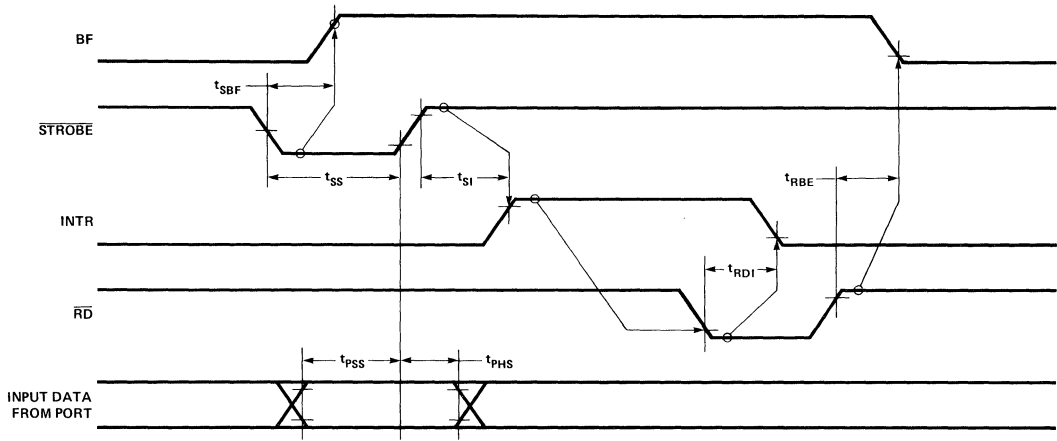
B. STROBED OUTPUT MODE
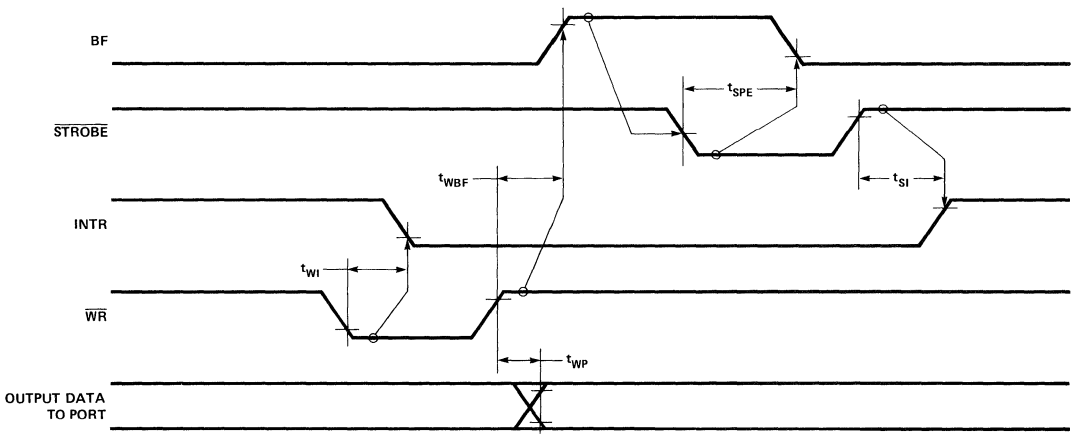
FIGURE 8. STROBED I/O TIMING.

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

A. BASIC INPUT MODE

t_{RP}

$\overline{RD}$

t_{PR}

INPUT
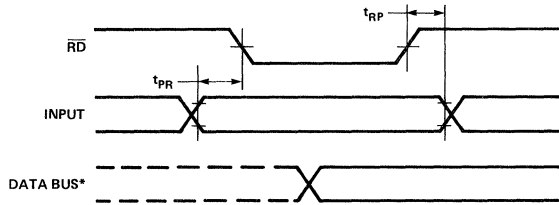
DATA BUS*

B. BASIC OUTPUT MODE

$\overline{WR}$

DATA BUS*

t_{WP}
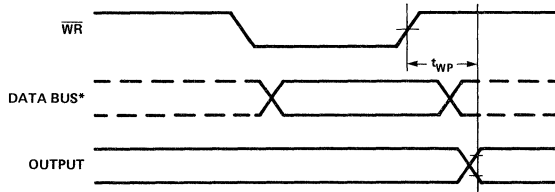
OUTPUT

*DATA BUS TIMING IS SHOWN IN FIGURE 7.

FIGURE 9. BASIC I/O TIMING WAVEFORM.

LOAD COUNTER FROM CLR

RELOAD COUNTER FROM CLR

COUNT | 0 | 3 | 2 | 1 | 0 | 3 | 2 |

t_f

t_2

TIMER-IN

t_r

t_1

TIMER-OUT (PULSE)

t_{CYC}

t_{TL}

TIMER-OUT (SQ. WAVE)

t_{TL}

t_{TH}

COUNTDOWN FROM 3 TO 0

t_{CYC}	320 ns MIN.
t_{RISE} & t_{FALL}	30 ns MAX.
t_1	80 ns MIN.
t_2	120 ns MIN.
t_{TL}	TIMER-IN TO $\overline{TIMER\text{-}OUT}$ LOW (TO BE DEFINED).
t_{TH}	TIMER-IN TO $\overline{TIMER\text{-}OUT}$ HIGH (TO BE DEFINED).
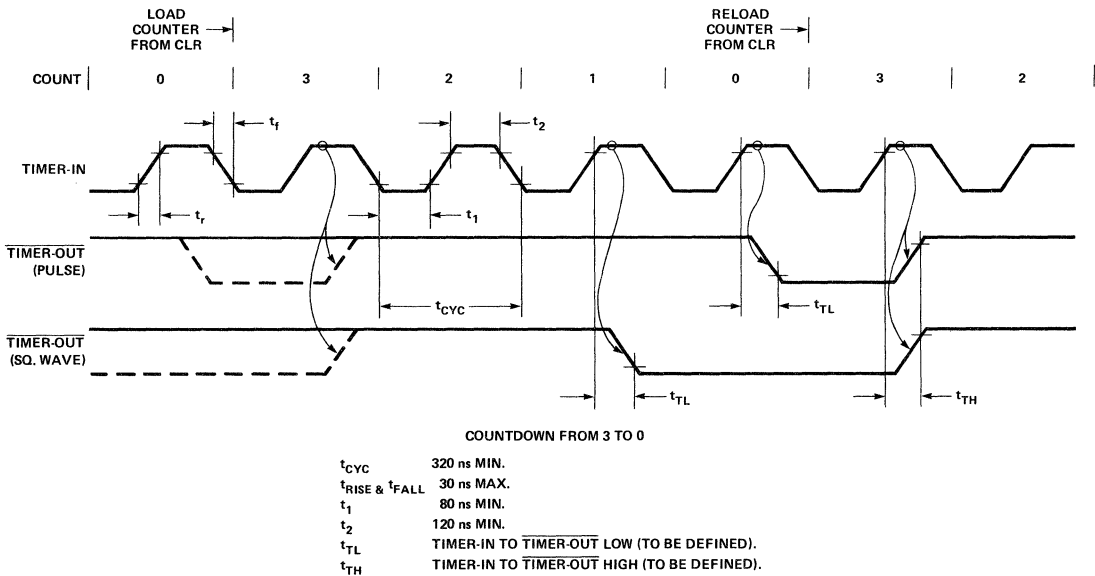
FIGURE 10. TIMER OUTPUT WAVEFORM.

intel®

8355
16,384 BIT ROM WITH I/O

*Directly Compatible With 8085 CPU

- **2048 Words x 8 Bits**
- **Single +5V Power Supply**
- **Internal Address Latch**

- **2 General Purpose 8 Bit I/O Ports**
- **Each I/O Port Line Individually Programmable as Input or Output**
- **Multiplexed Address and Data Bus**
- **40 Pin DIP**

The 8355 is a ROM and I/O chip to be used in the MCS-85™ microcomputer system. The ROM portion is organized as 2048 x 8. It has maximum access time of 400 ns to permit use with no wait states in 8085 CPU.

The I/O portion consists of two general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

PIN CONFIGURATION
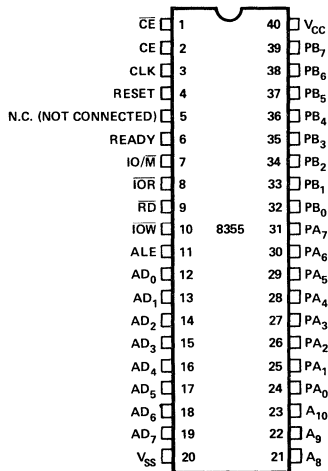
BLOCK DIAGRAM

8355 FUNCTIONAL PIN DEFINITION

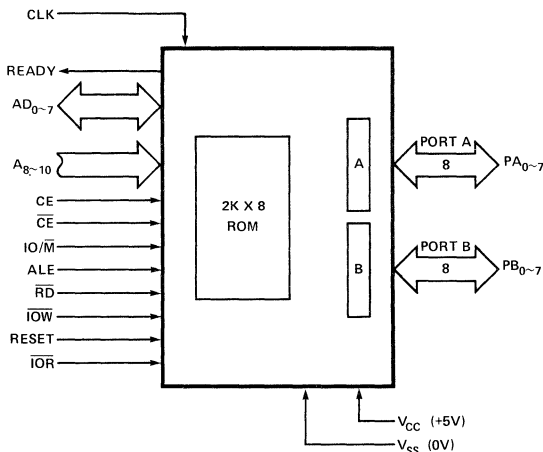| Symbol	Function
ALE	When ALE (Address Latch Enable) is high, AD_{0-7}, $IO/\overline{M}$, A_{8-10}, CE, and $\overline{CE}$ enter address latched. The signals (AD, $IO/\overline{M}$, A_{8-10}, CE, $\overline{CE}$) are latched in at the trailing edge of ALE.
AD_{0-7}	Bi-directional Address/Data bus. The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high.
	During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when latched Chip Enables are active, the output buffers present data on the bus.
A_{8-10}	These are the high order bits of the ROM address. They do not affect I/O operations.
$\overline{CE}$ CE	Chip Enable Inputs: $\overline{CE}$ is active low and CE is active high. The 8355 can be accessed only when BOTH Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD_{0-7} and READY outputs will be in a high impedance state.
$IO/\overline{M}$	If the latched $IO/\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the ROM.
$\overline{RD}$	If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected ROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are tri-stated.
$\overline{IOW}$	If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of $IO/\overline{M}$ is ignored.

Symbol	Function
CLK	The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE}$ low, CE high and ALE high.
READY	Ready is a tri-state output controlled by $\overline{CE}$, CE, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK (see Figure 4).
PA_{0-7}	These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0.
	Read operation is selected by $\overline{IOR}$ low when the Chip is enabled and AD_0 low.
	Alternately, $IO/\overline{M}$ high and $\overline{RD}$ low may be used in place of $\overline{IOR}$ when the chip is enabled and AD_0 is low to allow reading from a port.
PB_{0-7}	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0.
RESET	An input high on RESET causes all pins in Ports A and B to assume input mode.
$\overline{IOR}$	When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination $IO/\overline{M}$ high and $\overline{RD}$ low.
V_{CC}	+5 volt supply.
V_{SS}	0 volt supply.

FUNCTIONAL DESCRIPTION

ROM Section

The ROM section of the chip is addressed by an 11-bit address and the Chip Enables. The address and levels on the Chip Enable pins are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the ROM location addressed by the latched address are put out through AD_{0-7} output buffers.

I/O Section

The I/O section of the chip is addressed by the latched value of AD_{0-1}. Two 8-bit Data Direction Registers in 8355 determine the input/output status of each pin in the corresponding ports. A 0 specifies an input mode, and a 1 specifies an output mode. The table summarizes port and DDR designation. *DDR's cannot be read.*
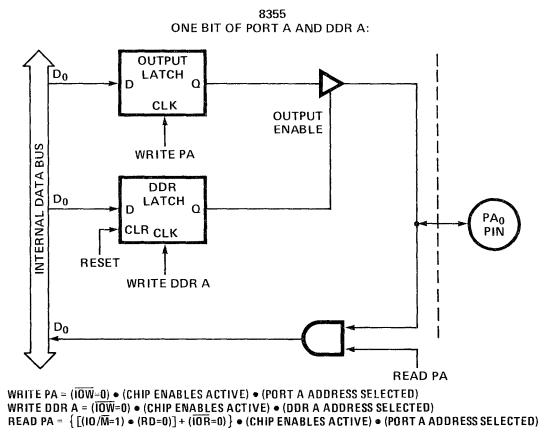
AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD_{0-7} is written into I/O port selected by the latched value of AD_{0-1}.

During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high (glitch free output).

A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7}.

To clarify the function of the I/O ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.

Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the output latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

System Interface with 8085

A system using the 8355 can use either one of the two I/O Interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE and $\overline{CE}$. By using a combination of unused address lines A_{11-15} and the Chip Enable inputs, the 8085 system can use up to 5 each 8355's without requiring a CE decoder. See Figure 1.

If a memory mapped I/O approach is used the 8355 will be selected by the combination of both the Chip Enables and IO/$\overline{M}$ using the AD_{8-15} address lines. See Figure 2.
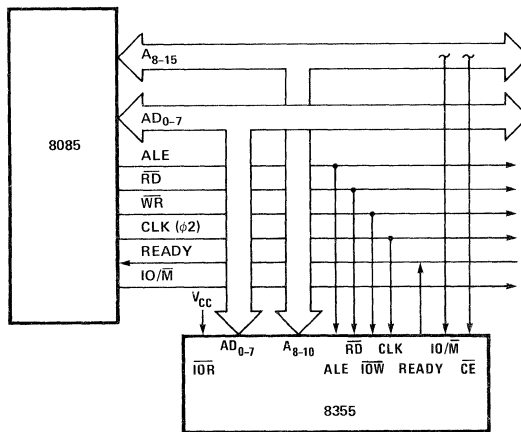
FIGURE 2. 8355 IN 8085 SYSTEM (MEMORY-MAPPED I/O).

8355
ONE BIT OF PORT A AND DDR A:

WRITE PA = ($\overline{IOW}$=0) • (CHIP ENABLES ACTIVE) • (PORT A ADDRESS SELECTED)
WRITE DDR A = ($\overline{IOW}$=0) • (CHIP ENABLES ACTIVE) • (DDR A ADDRESS SELECTED)
READ PA = {[(IO/$\overline{M}$=1) • ($\overline{RD}$=0)] + ($\overline{IOR}$=0)} • (CHIP ENABLES ACTIVE) • (PORT A ADDRESS SELECTED)
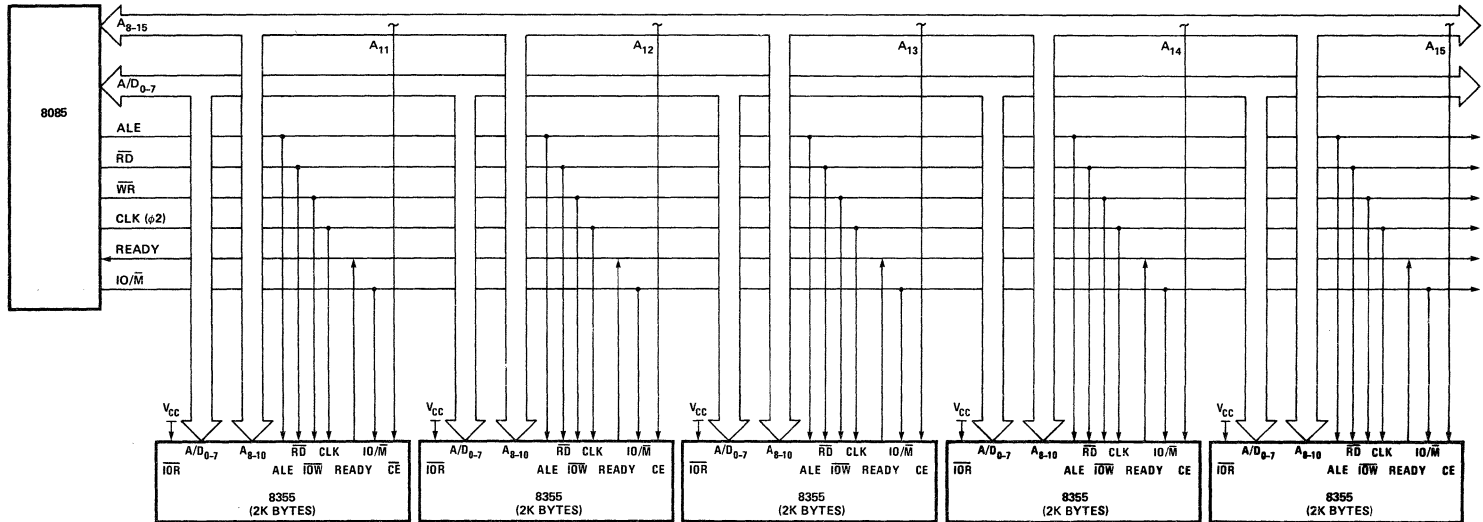
Note: Use $\overline{CE}$ for the first 8355 in the system, and CE for the other 8355's. Permits up to 5 ea. 8355's in a system without CE decoder.

FIGURE 1. 8355 IN 8085 SYSTEM (STANDARD I/O).

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... 0°C to +70°C
Storage Temperature .... -65°C to +150°C
Voltage on Any Pin
  With Respect to Ground .... -0.3V to +7V
Power Dissipation 1.5W

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA
I_{IL}	Input Leakage		10	µA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	µA	0.45V $\leqslant V_{OUT} \leqslant V_{CC}$
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

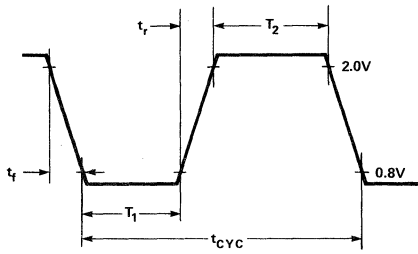| SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CYC}	Clock Cycle Time	320		ns	
T_1	CLK Pulse Width	80		ns	C_{LOAD} = 150 pF
T_2	CLK Pulse Width	120		ns	(See Figure 3)
t_f, t_r	CLK Rise and Fall Time		30	ns	
t_{AL}	Address to Latch Set Up Time	50		ns	
t_{LA}	Address Hold Time after Latch	80		ns	
t_{LC}	Latch to READ/WRITE Control	100		ns	
t_{RD}	Valid Data Out Delay from READ Control		150	ns	
t_{AD}	Address Stable to Data Out Valid		400	ns	150 pF Load
t_{LL}	Latch Enable Width	100		ns	
t_{RDF}	Data Bus Float after READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		ns	
t_{CC}	READ/WRITE Control Width	250		ns	
t_{DW}	Data In to WRITE Set Up Time	150		ns	
t_{WD}	Data In Hold Time After WRITE	0		ns	
t_{WP}	WRITE to Port Output		400	ns	
t_{PR}	Port Input Set Up Time	50		ns	
t_{RP}	Port Input Hold Time	50		ns	
t_{RYH}	READY HOLD TIME	0	120	ns	
t_{ARY}	ADDRESS (CE) to READY		160	ns	
t_{RV}	Recovery Time between Controls	300		ns	
t_{RDE}	Data Out Delay from READ Control	10		ns	

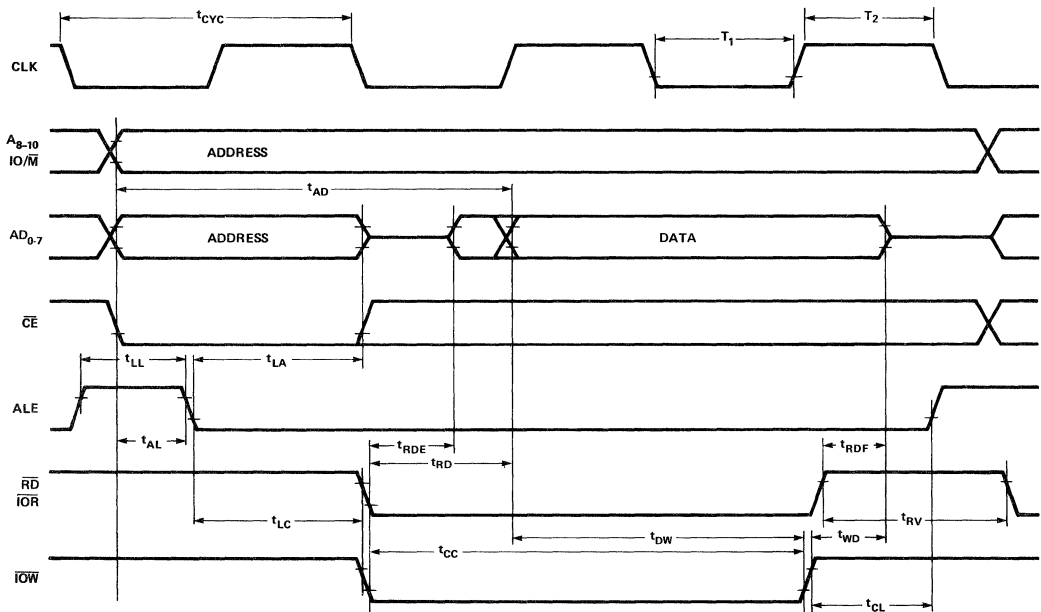**FIGURE 4. CLOCK SPECIFICATION FOR 8355.**

FIGURE 5. ROM READ AND I/O READ AND WRITE.

PRELIMINARY

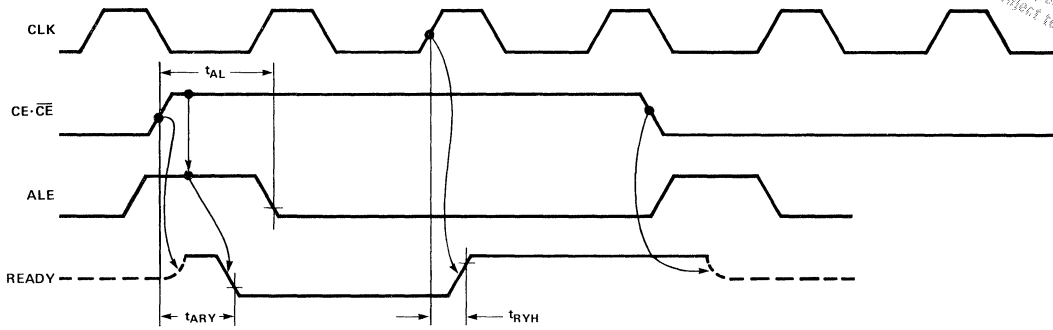Notice: This is not a final specification. Some parametric limits are subject to change.

FIGURE 6. WAIT STATE TIMING (READY = 0).

A. INPUT MODE
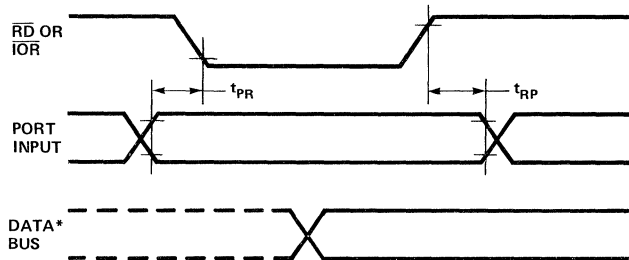
B. OUTPUT MODE
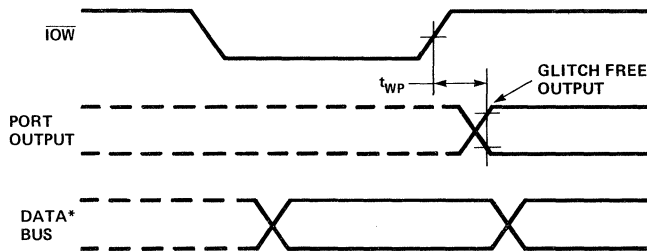
*DATA BUS TIMING IS SHOWN IN FIGURE 3.

FIGURE 7. I/O PORT TIMING.

intel®

8755
16,384 BIT EPROM WITH I/O

*Directly Compatible With 8085 CPU

- **2048 Words x 8 Bits**
- **Single +5V Power Supply (V$_{CC}$)**
- **U.V. Erasable and Electrically Reprogrammable**
- **Internal Address Latch**

- **2 General Purpose 8 bit I/O Ports**
- **Each I/O Port Line Individually Programmable as Input or Output**
- **Multiplexed Address and Data Bus**
- **40 Pin DIP**

The 8755 is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the MCS-85™ microcomputer system. The PROM portion is organized as 2048 x 8. It has maximum access time of 400 ns to permit use with no wait states in 8085 CPU.

The I/O portion consists of two general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

PIN CONFIGURATION

PROG AND $\overline{CE}$	1	40	V$_{CC}$
CE	2	39	PB$_7$
CLK	3	38	PB$_6$
RESET	4	37	PB$_5$
V$_{DD}$	5	36	PB$_4$
READY	6	35	PB$_3$
IO/$\overline{M}$	7	34	PB$_2$
$\overline{IOR}$	8	33	PB$_1$
$\overline{RD}$	9	32	PB$_0$
$\overline{IOW}$	10	31	PA$_7$
ALE	11	30	PA$_6$
AD$_0$	12	29	PA$_5$
AD$_1$	13	28	PA$_4$
AD$_2$	14	27	PA$_3$
AD$_3$	15	26	PA$_2$
AD$_4$	16	25	PA$_1$
AD$_5$	17	24	PA$_0$
AD$_6$	18	23	A$_{10}$
AD$_7$	19	22	A$_9$
V$_{SS}$	20	21	A$_8$

(device: 8755)
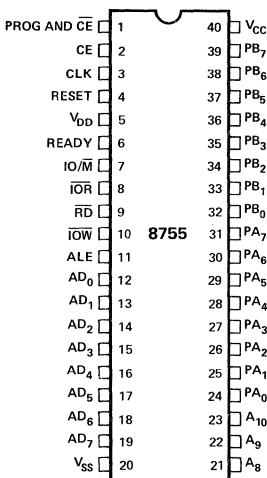
BLOCK DIAGRAM
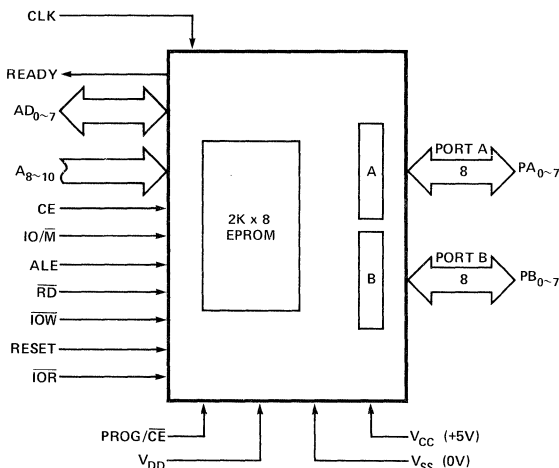
8755 FUNCTIONAL PIN DESCRIPTION

Symbol	Function
ALE	When Address Latch Enable is high, AD_{0-7}, $IO/\overline{M}$, A_{8-10}, CE, and $\overline{CE}$ enter the address latches. The signals (AD, IO/M, A_{8-10}, CE) are latched in at the trailing edge of ALE.
AD_{0-7}	Bi-directional Address/Data bus. The lower 8-bits of the PROM or I/O address are applied to the bus lines when ALE is high.
	During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched Chip Enables are active, the output buffers present data on the bus.
A_{8-10}	These are the high order bits of the PROM address. They do not affect I/O operations.
$\overline{CE}$/PROG CE	CHIP ENABLE INPUTS: $\overline{CE}$ is active low and CE is active high. Both chip enables must be active to permit accessing the PROM. $\overline{CE}$ is also used as a programming pin (see section on programming).
$IO/\overline{M}$	If the latched $IO/\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the PROM.
$\overline{RD}$	If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected PROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are tri-stated.
$\overline{IOW}$	If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of $IO/\overline{M}$ is ignored.
CLK	The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE}$ low, CE high, and ALE high.
READY	READY is a 3-state output controlled by CE, $\overline{CE}$, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK (see Figure 2.).
PA_{0-7}	These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0.

Symbol	Function
	Read operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD_0 low, or $IO/\overline{M}$ high, $\overline{RD}$ low, active Chip Enables, and AD_0 low.
PB_{0-7}	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0.
RESET	In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).
$\overline{IOR}$	When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination of $IO/\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} ("1").
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.
V_{DD}	V_{DD} is a programming voltage, and it is normally grounded.
	For programming, a high voltage is supplied with V_{DD}, = 25V, typical.

FUNCTIONAL DESCRIPTION

PROM Section

The 8755 contains an 8-bit address latch which allows it to interface directly to MCS-48 and MCS-85 Microcomputers without additional hardware.

The PROM section of the chip is addressed by the 11-bit address and CE. The address, $\overline{CE}$ and CE are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and $IO/\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the PROM location addressed by the latched address are put out on the AD_{0-7} lines.

I/O Section

The I/O section of the chip is addressed by the latched value of AD_{0-1}. Two 8-bit Data Direction Registers determine the input/output status of each pin in the corresponding port. A 0 specifies an input mode, and a 1 specifies an output mode. The table summarizes port and DDR designation. Contents of the DDR's cannot be read.

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD   is written into I/O port selected by the latched value of AD_{0-1}. During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high. (glitch free output).

A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7}.

To clarify the function of the I/O Ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.

8755
ONE BIT OF PORT A AND DDR A:

WRITE PA = ($\overline{IOW}$=0) • (CHIP ENABLES ACTIVE) • (PORT A ADDRESS SELECTED)
WRITE DDR A = ($\overline{IOW}$=0) • (CHIP ENABLES ACTIVE) • (DDR A ADDRESS SELECTED)
READ PA = { [(IO/$\overline{M}$=1) • (RD=0)] + ($\overline{IOR}$=0) } • (CHIP ENABLES ACTIVE) • (PORT A ADDRESS SELECTED)

Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the Output Latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

ERASURE CHARACTERISTICS

The erasure characteristics of the 8755 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level flourescent lighting could erase the typical 8755 in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8755 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8755 window to prevent unintentional erasure.

The recommended erasure procedure (see page 3-55) for the 8755 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000μW/cm^2 power rating. The 8755 should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

PROGRAMMING

Initially, and after each erasure, all bits of the EPROM portions of the 8755 are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 8755 is programmed on the Intel® Universal PROM Programmer (UPP). The UPP and its related personality cards for the 8755 are described beginning on page 13-45 of the 1977 Intel Data Catalog.

PRELIMINARY

SYSTEM APPLICATIONS
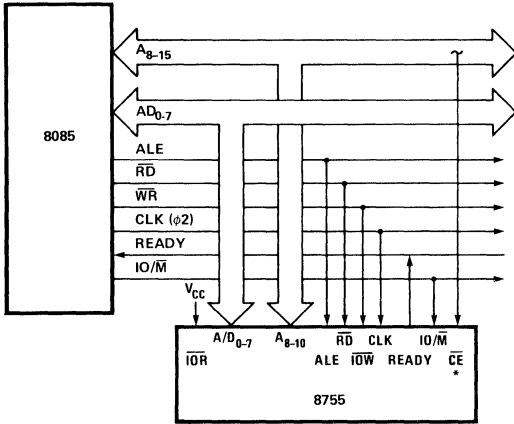
*USE $\overline{CE}$ FOR FIRST 8755 IN SYSTEM, AND CE FOR OTHERS.
BY CONNECTING CE OF EACH 8755 CHIP TO EACH OF A_{11}
THROUGH A_{15}, THE MINIMUM SYSTEM CAN USE 5-8755's
(10K BYTES) WITHOUT REQUIRING CE DECODER.

**FIGURE 1. 8755 IN 8085 SYSTEM
(STANDARD I/O).**
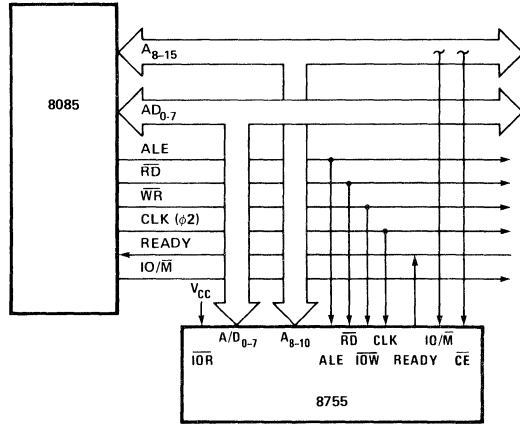
**FIGURE 2. 8755 IN 8085 SYSTEM
(MEMORY-MAPPED I/O).**

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... -10°C to +70°C
Storage Temperature .... -65°C to +150°C
Voltage on Any Pin
  With Respect to Ground .... -0.5V to +7V
Power Dissipation 1.5W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS $(T_A = 0°C$ to $70°C; V_{CC} = 5V \pm 5\%)$

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V ·	I_{OH} = -400μA
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$ to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V $\leqslant V_{OUT} \leqslant V_{CC}$
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS $(T_A = 0°C$ to $70°C; V_{CC} = 5V \pm 5\%)$

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CYC}	Clock Cycle Time	320		ns	
T_1	CLK Pulse Width	80		ns	C_{LOAD} = 150 pF
T_2	CLK Pulse Width	120		ns	(See Figure 3)
t_f, t_r	CLK Rise and Fall Time		30	ns	
t_{AL}	Address to Latch Set Up Time	50		ns	
t_{LA}	Address Hold Time after Latch	80		ns	
t_{LC}	Latch to READ/WRITE Control	100		ns	
t_{RD}	Valid Data Out Delay from READ Control		150	ns	
t_{AD}	Address Stable to Data Out Valid		400	ns	150 pF Load
t_{LL}	Latch Enable Width	100		ns	
t_{RDF}	Data Bus Float after READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		ns	
t_{CC}	READ/WRITE Control Width	250		ns	
t_{DW}	Data In to WRITE Set Up Time	150		ns	
t_{WD}	Data In Hold Time After WRITE	0		ns	
t_{WP}	WRITE to Port Output		400	ns	
t_{PR}	Port Input Set Up Time	50		ns	
t_{RP}	Port Input Hold Time	50		ns	
t_{RYH}	READY HOLD TIME	0	120	ns	
t_{ARY}	ADDRESS (CE) to READY		160	ns	
t_{RV}	Recovery Time between Controls	300		ns	
t_{RDE}	Data Out Delay from READ Control	10		ns	

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

FIGURE 3. CLOCK SPECIFICATION FOR 8755
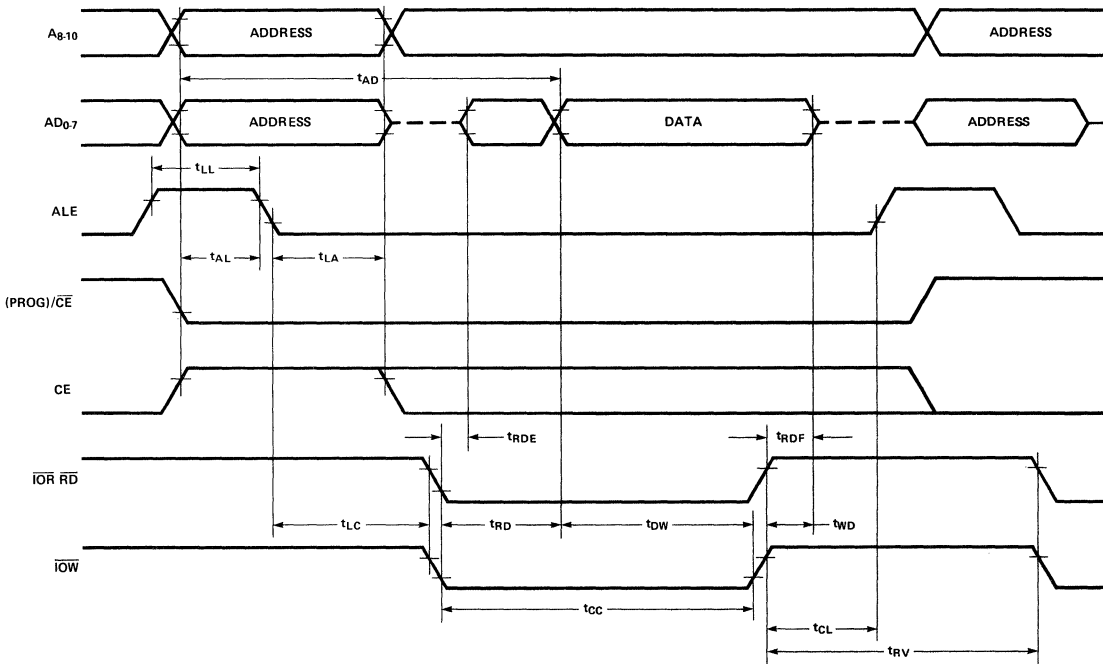
FIGURE 4. PROM READ, I/O READ, AND WRITE TIMING.

Please note that $\overline{CE1}$ must remain low for the entire cycle. This is due to the fact that the programming enable function common to this pin will disrupt internal data bus levels if $\overline{CE1}$ is taken high during the read.

A. INPUT MODE

RD OR
IOR

PORT
INPUT

t_{PR}

t_{RP}

DATA*
BUS

B. OUTPUT MODE

IOW

t_{WP}

GLITCH FREE
OUTPUT
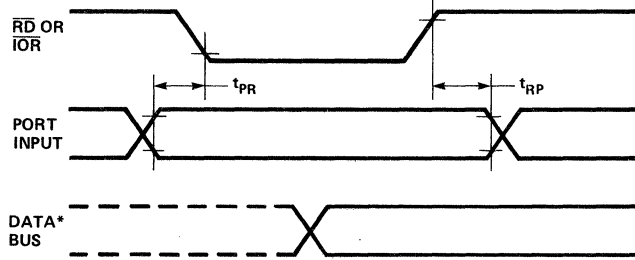
PORT
OUTPUT
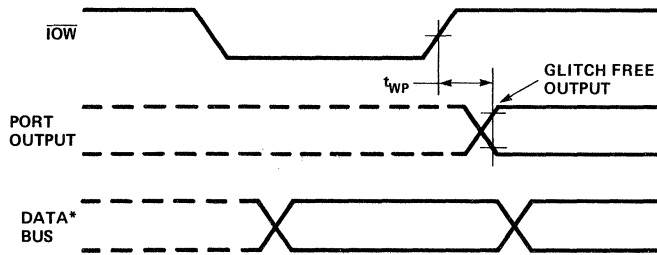
DATA*
BUS

*DATA BUS TIMING IS SHOWN IN FIGURE 4.

FIGURE 5. I/O PORT TIMING.

CLK

t_{AL}

CE·CE

ALE

READY

t_{ARY}

t_{RYH}

FIGURE 6. WAIT STATE TIMING (READY = 0).

Chapter 7

SUPPORT PRODUCTS
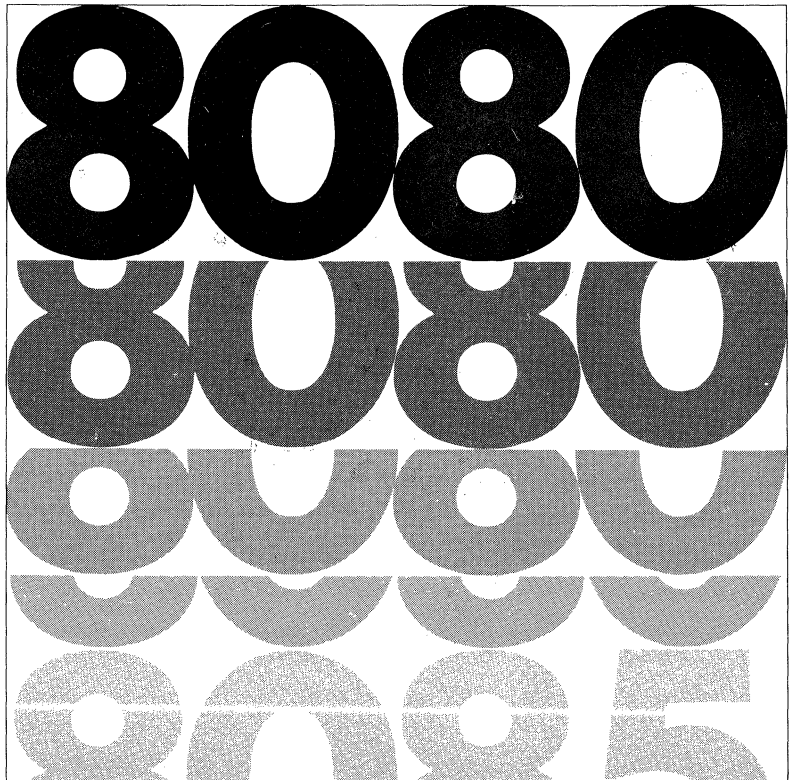
PROMPT 80 DESIGN AID
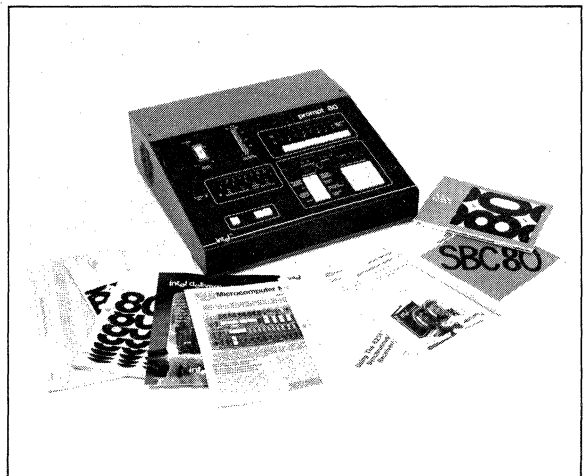
INTELLEC® PROMPT 80™·

8080 MICROCOMPUTER DESIGN AID

Simplifies microcomputing

Enter, run, debug and save machine language programs with calculator-like ease

Complete, fully-assembled microcomputer, including:

CPU   Standard 8080A on popular SBC 80/10 Single Board Computer

Memory   1K byte RAM, 3K byte ROM, and two spare 1K byte 8708 EPROMs

I/O   24 programmable parallel I/O (TTL) lines, including two:
8-bit ports, fully implemented switches, displays
Programmable serial I/O interfaces directly with most terminals

Power   Only 110 or 230 VAC required

Low Cost

PROM Programmer for 8708/2708/2704 UV Erasable, Electrically Reprogrammable ROMs (EPROMs)

Integral keyboard and 16-digit display (no teletypewriter or CRT terminal required)

Extensive system monitor software in ROM:
Examine/Display/Modify
Registers and Memory
Enter, Run, Test, Single-Step programs
Hex Calculator
Move, Search Memory Blocks

Self-programmable — user can add functions
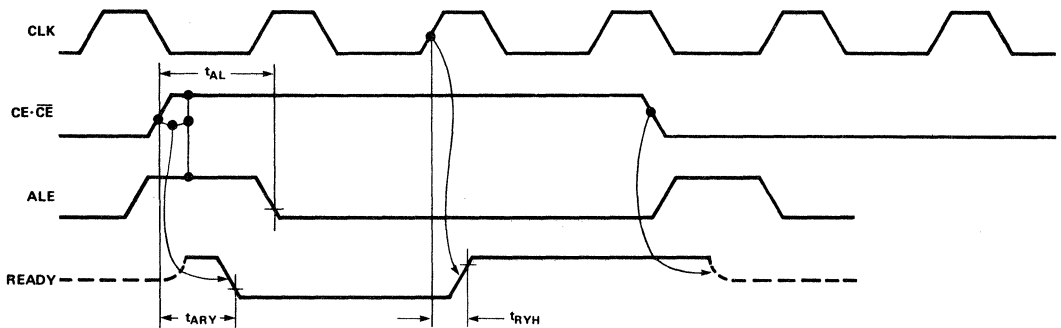
Comprehensive design library

Intellec® PROMPT 80™ is a low-cost, fully assembled microcomputer design aid. PROMPT 80 simplifies the programming of SBC 80 and System 80 microcomputers, as well as 8080 processors, 8708/2708/2704 EPROMs and 8255/8251 programmable I/O devices. 8080 programs can be entered and debugged with calculator-like ease on the large, informative display and keyboard panel. The comprehensive design library with tutorial manual is ideal for newcomers to microcomputing.

PROMPT 80's SBC 80/10 can be expanded using the SBC modular cardcage. And PROMPT 80 can serve as an economical 8708 Specialized PROM Programmer (SPP) peripheral in Intellec Microcomputer Development Systems.

PROMPT SIMPLIFIES MICROCOMPUTING

Intellec PROMPT 80 simplifies the programming of 8080 processors, SBC 80 and System 80 microcomputers, as well as 8708 EPROMs and 8255/8251 programmable I/O devices.

PROMPT is a low-cost programming tool. It is a micro-computer design aid — not a development system with sophisticated software and peripherals.

PROMPT encourages the preparation and verification of small, modular routines which together may comprise sizable programs. These are written in assembly language, then entered in machine language and debugged with calculator-like ease on the large, informative display and keyboard panel.

Many 8080 operations can be specified with only two key strokes. Once entered, programs can be exercised one instruction (single step) or many instructions at a time. And, any of the 8080 registers can be watched while single-stepping.

Programs are readily saved and instantly reloaded via UV Erasable, Electrically Reprogrammable ROMs (EPROMs). PROMPT 80 can program the popular 8708 EPROMs in small blocks, so routines can be debugged and saved incrementally. Several programs are pre-recorded as examples on PROMPT's spare 8708 EPROMs.

PROMPT 80 is a complete, fully assembled and powered 8080 microcomputer, including RAM, I/O, and system monitor in ROM. Twenty-four lines of programmable, TTL-compatible, parallel I/O are easily accessed on a panel connector. Two 8-bit ports are fully implemented, one with displays for output, the other with displays and switches for input. PROMPT's programmable serial I/O interfaces directly with most terminals. A teletypewriter or CRT can be used, but neither is required because of PROMPT's built-in keyboard and display.

The PROMPT 80 manual includes chapters for the reader with little or no programming experience. Topics treated range from the 'number system to microcomputer hard-ware design. A novel, unifying set of tutorial diagrams — MICROMAP™ — simplify microcomputer concepts.
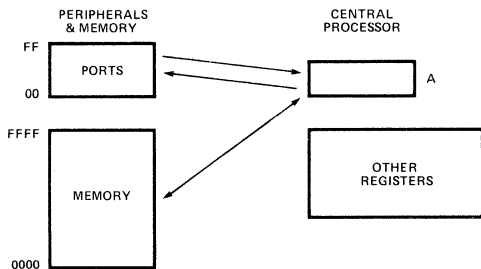
PROMPT's handy, pocket-sized reference cardlet can be affixed to the mainframe. Programming pads aid in the organization and documentation of programs. These features, plus a comprehensive design library of manuals, articles, and applications notes, make Intellec PROMPT 80 ideal for the newcomer to microcomputing.

A COMPLETE COMPUTER

The heart of PROMPT 80 is the popular SBC 80/10 Single Board Computer, a complete computer on a single printed circuit board. The SBC 80/10 includes an 8080A, 1K bytes of static RAM memory, and sockets for 4K bytes of EPROM memory. Signals to the SBC 80/10 include 48 programmable, parallel I/O lines with sockets for inter-changeable line drivers and terminators, a programmable serial channel, a multi-source single level interrupt net-work, and bus drivers for memory and I/O expansion. Read-only-memory may be added in 1K byte increments using Intel 8708 EPROMs or 8308 ROMs.

The central processor for PROMPT's SBC 80/10 is Intel's powerful 8-bit n-channel MOS 8080A CPU. The 8080A contains six 8-bit general-purpose registers and an accumulator. The six general-purpose registers may be addressed individually or in pairs, providing both single and double precision operations.

The 8080A has a 16-bit address bus which allows direct addressing of up to 64K bytes of memory. An external stack, located anywhere in read/write memory, may be used as a last-in/first-out store. The contents of the pro-gram counter, accumulator, flags, and all of the general-prupose registers are stacked using a 16-bit pointer. Sub-routine nesting is bounded only by memory size.

EXPANDING PROMPT 80™
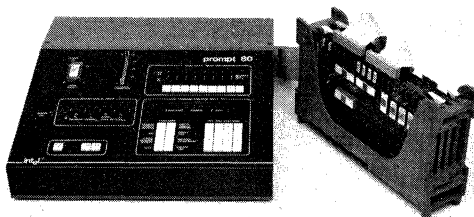
PROMPT 80's SBC 80/10 can be expanded via the SBC 604 Modular Cardcage. The cardcage houses the SBC 80/10 and up to three expansion boards. Memory and I/O can be added in various combinations. Additional power may be required.
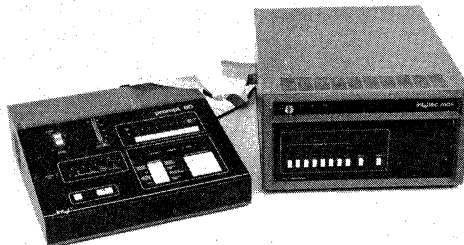
A Specialized PROM Programmer kit, the PROMPT-SPP, allows PROMPT 80 to serve as an economical 8708 Spe-cialized PROM Programmer peripheral in Intellec Micro-computer Development Systems. The PROMPT-SPP cable plugs directly into the rear panel of the Intellec Micro-computer Development System.

PROM PROGRAMMER

8708 UV Erasable, Electrically Reprogrammable ROMs (EPROMs) can be easily programmed, compared, and transferred to RAM using the zero-insertion force socket on the panel. A new technique allows 8708 to be partially programmed in multiple blocks of 16 bytes. Thus, small, modular routines can be entered, tested, and readily saved using EPROM.

EPROMs can also be conveniently duplicated. The master (original) device plugs into the SBC 80/10 inside PROMPT 80, and can be copied to the panel programming socket.

REGISTER/DISPLAY GROUP

All 8080 registers can be displayed, even while single-stepping programs. The registers are shown in three rows:

first row:	B	C	D	E
second row:	H	L	Flags	A
third row:	Program Counter		Stack Pointer	

One register row is visible at a time. Three small LEDs to the left of these rows indicate which row is displayed. The SCROLL REGISTER DISPLAY command displays the next row (first, second, third, etc.)

RESET, INTERRUPTS

SYS RST resets the system, initializes the PROMPT 80 registers and enters the monitor. MON INT interrupts a user program and enters the monitor saving the user registers. USR INT is a user interrupt which traps PROMPT 80 to location $3C02_{16}$.

MONITOR

A comprehensive system monitor resides in three 1K ROMs. It drives PROMPT's keyboard, displays, and responds to COMMANDS and FUNCTIONS. The monitor is modular, organized so that the third ROM may be removed if F FUNCTIONS are not required. This allows sizable user routines — as much as 2K ROM/EPROM and nearly 1K RAM — to be exercised.
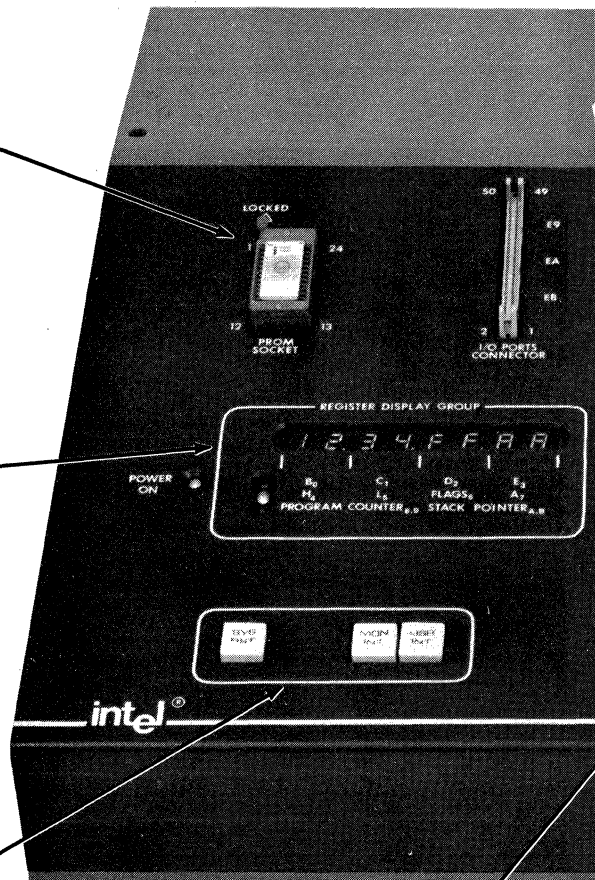
COMMANDS

PROMPT 80 commands are compatible with those used by Intel's SDK, SBC, and Intellec monitors.

You can EXAMINE/MODIFY a REGISTER, or DISPLAY/MODIFY MEMORY. Then either the NEXT or PREVIOUS register and memory locations can be opened with one button.

The GO command executes programs, allowing multiple, optional breakpoints. Or a program can be SINGLE STEPped, executed one instruction at a time.

The SCROLL REGISTER DISPLAY command displays the next row of the REGISTER/DISPLAY GROUP.

INPUT/OUTPUT GROUP

The INPUT/OUTPUT (I/O) GROUP features two fully implemented 8-bit ports, both with displays, and with latch switches for the input port E9. The port addresses are clearly marked E8 and E9. Those two ports and a third, at EA, are easily accessible on the I/O PORTS CONNECTOR. Negative true logic is used throughout the I/O GROUP and PORTS CONNECTOR to enhance noise immunity and allow wire-ANDing.

PARALLEL I/O

The I/O PORTS CONNECTOR provides easy access to 24 parallel, TTL-compatible lines. These lines are addressed as three ports (each 8 lines), port E8, E8, and EA.

These ports can be defined to be input or output by software. Defining control words, tabulated in "Specifications", are sent OUT to port EB, the control word register.

SERIAL I/O

PROMPT's programmable serial I/O readily interfaces with most terminals. Jumpers select either 20 mA teletypewriter (TTY) current loop or RS-232C operation, and the appropriate communications frequency. Asynchronous or synchronous transmission, data format, control characters, parity, and transmission rate can be programmed.

A serial cable kit, PROMPT-SER, connects PROMPT to either a teletypewriter or RS-232C standard (CRT) terminal through a rear chassis access slot. Teletypewriters may require minor reader control modifications.

COMMAND/FUNCTION DISPLAYS

The COMMAND/FUNCTION displays show addresses and data when DISPLAYing MEMORY, and parameters for COMMANDS and FUNCTIONS are entered.

FUNCTIONS

Eight FUNCTIONS are provided by PROMPT. Others may be added by the user. Pressing a HEX DATA/FUNCTIONS key (0—7) starts a function.

⓪	is	F0	Read Paper Tape
①	is	F1	Write Paper Tape
②	is	F2	Program EPROM, Compare
③	is	F3	Compare EPROM
④	is	F4	Transfer EPROM to RAM
⑤	is	F5	Move Block Memory
⑥	is	F6	Hexadecimal Calculator, +, −
⑦	is	F7	Byte Search Memory, optional mask
⑧	is	F8	Word Search Memory, optional mask

Commands are entered naturally, like phrases in a sentence: the NEXT parameters are separated by commas ⊡ and command sentences end with ⊡ EXECUTE/END.

The commands do what makes sense. For example:

GO ☐ ① ⓪ ⓪ ⊡ EXECUTE/END
starts the program at address 100.

GO ☐ ① ⓪ ⓪ ⊡ NEXT ② ⓪ ⓪ ⊡ EXECUTE/END
starts the program at 100, but stops if you get to 200, a breakpoint.

GO ☐ ⊡ EXECUTE/END
starts the program where you last stopped.

SPECIFICATIONS

WORD SIZE
Instruction: 8, 16, or 24 bits
Data: 8 bits

TIMING
Basic Instruction: 1.95 μsec
Cycle Time: $t_{CY} = 488$ nsec
Clock: 2.058 MHz ± 0.1%

MEMORY BYTES

	Addressing	On Board	Monitor Uses
ROM/PROM	$0-0FFF_{16}$	4096	2048 or 3072
RAM	$3C00-3FFF_{16}$	1024	114

Up to 48K bytes may be added using optional RAM, ROM, or PROM expansion boards and the SBC 604 Cardcage.

I/O ADDRESSING
Ports E4 to E7 are dedicated to PROMPT's display/keyboard groups. Ports E8 to EB drive the panel I/O PORTS CONNECTOR and PROM SOCKET.

	Dedicated to Display/Keyboard				I/O Ports Connector/ PROM Socket				Serial I/O USART	
	A	B	C	Control	A	B	C	Control	Data	Control
PORT	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED

PARALLEL I/O
The panel I/O ports can be defined input or output by OUTputting control words to port address EB.

HEX Control Word (OUT this to EB)	Port E8 Bits 7–0	Port E9 Bits 7–0	Port EA Bits 7–4	Port EA Bits 3–0
80	OUTPUT	OUTPUT	OUTPUT	OUTPUT
81	OUTPUT	OUTPUT	OUTPUT	INPUT
82	OUTPUT	INPUT	OUTPUT	OUTPUT
83	OUTPUT	INPUT	OUTPUT	INPUT
84 or 86	OUTPUT	STROBED OUTPUT	OUTPUT	Bits 2, 1, 0 are strobes
85 or 87	OUTPUT	STROBED INPUT	OUTPUT	

All input ports are TTL-compatible. Ports E8 and EA are one-load fully TTL-compatible as output. Port E9 is ordinarily used as input. When used as output, E9 can sink at least one low-power TTL load.

SERIAL I/O
The serial I/O port is defined by software and jumpers. PROMPT is configured at the factory for 20 mA current loop TTY interface, but can easily be jumpered for RS-232C levels.

Asynchronous or synchronous transmission, data format, control characters, parity and transmission rate can be programmed.

INTERRUPTS
PROMPT 80 provides a panel user interrupt to $3C02_{16}$. The SBC 80/10 supports single level vectoring to location 38_{16}. Requests may originate from user-specified I/O (2), the parallel ports (2), or serial port (2).

EPROM PROGRAMMING
8708/2708/2704 EPROMs can be programmed in multiple blocks of 16 bytes. Starting and ending memory address need only differ by a multiple of 16, and starting EPROM address end XX0 hexadecimal (X = don't care). Programming time is 115 sec for 1K byte, 3 sec for 16 bytes.

The 8708 may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (UV intensity × exposure time) is 10 W-sec/cm^2.

SYSTEM MONITOR
Resides in three 8308 ROMs, 0 to $3FF_{16}$, 400_{16} to $7FF_{16}$, and 800_{16} to BFF_{16}. The third ROM implements F FUNCTIONS, and can be removed. PROMPT has an unused ROM/EPROM socket at address $C00_{16}$ to FFF_{16}.

COMMANDS
Examine/Modify Register   Display/Modify Memory
Go (with optional breakpoints)   Single Step
Scroll Register Display   Open Previous/Clear Entry
Next [.]   [.] Execute/end

FUNCTIONS
[0] Read Tape
[1] Write Tape
[2] Program EPROM, Compare
[3] Compare EPROM
[4] Transfer EPROM to RAM
[5] Move Block Memory
[6] Hexadecimal Calculator, +, –
[7] Byte Search Memory, optional mask
[8] Word Search Memory, optional mask

SOFTWARE DRIVERS
Panel Keyboard Input   Panel Display Output
Console Terminal Input   Console Terminal Output
TTY Reader Input   TTY Punch Output

CONNECTORS
PROMPT Panel I/O Ports   3M 3425 Flat
SBC 80/10 Parallel I/O   3M 3415 Flat
SBC 80/10 Serial I/O   3M 3462 Flat
SBC 80/10 Bus   CDC VPB01E43D00A1
SBC 80/10 Auxiliary Bus   TI H312130

EQUIPMENT SUPPLIED
PROMPT 80 mainframe with SBC 80/10, display/keyboard, PROM Programmer, power supply, cabinet, and ROM-based system monitor
(2) 8708 EPROMs with pre-recorded example programs
110 VAC power cable, 110 or 220 VAC fuse
PROMPT 80 User's Manual, PROMPT 80 Monitor Listing
PROMPT 80 Reference Cardlist, PROMPT 80 Programming Pads
8080 Systems User's Guide, 8080 Assembly Language Manual
System 80/10 Hardware Reference Manual
Design Library of Application Notes, Article Reprints
PROMPT 80 Schematics

ORDERING INFORMATION, COMPATIBLE EQUIPMENT
PROMT-80 – Complete PROMPT 80 set 110 VAC
PROMT-80-220V – Complete PROMPT 80 set 220 VAC
PROMT-SER – Serial Cable connects PROMPT to TTY, CRT
PROMT-SPP – Specialized PROM Programmer Kit connects PROMPT 80 to Intellec® Microcomputer Development Systems for 8708 EPROM programming.
All SBC products (additional memory, I/O, wire-wrap, and other boards) are compatible with PROMPT's SBC 80/10.
Additional PROMPT 80 Programming Pads can be ordered from Intel Literature Department.

PHYSICAL CHARACTERISTICS
Maximum Height: 13.5 cm   (5.3 in.)
Width: 43.2 cm   (17 in.)
Maximum Depth: 43.2 cm   (17 in.)
Weight: 9.6 kg   (21 lb)

ELECTRICAL REQUIREMENTS
Either 115 or 230 VAC (±10%) may be switch-selected on the mainframe. 1.8 amps max current (at 125 VAC)
Frequency is 47–63 Hz.

Voltage	Internal PROMPT 80 Supply	PROMPT 80 Requires
+26.5	0.1A	0.03A
+12	1.2A	0.5A
+ 5	6.0A	5.0A
– 5	0.3A	0.1A
–12	0.3A	0.2A

Fixed over-voltage protect on 5V supply 6.2–6.7 volts.

ENVIRONMENTAL
Operating Temperature: 10°C to 40°C
Non-operating Temperature: –20°C to 65°C

INTELLEC
MICROCOMPUTER DEVELOPMENT SYSTEM

Modular microcomputer development system for development and implementation of MCS™-80 and Series 3000 Microcomputer Systems

Intel® 8080 microprocessor, with 2 µs cycle time and 78 instructions, controls all Intellec MDS functions

16K bytes RAM memory expandable to 64K bytes

2K bytes ROM memory expandable to 14K bytes

Hardware interfaces and software drivers provided for TTY, CRT, line printer, high-speed paper tape reader, high-speed paper tape punch, and Universal PROM Programmer

Universal bus structure with multiprocessor and DMA capabilities

Eight level nested, maskable, priority interrupt system

Optional PROM programmer peripheral capable of programming all Intel PROMs

ICE (In-Circuit Emulator) options extend Intellec MDS diagnostic capabilities into user configured system allowing real-time emulation of user processors

Optional I/O modules expandable in groups of four 8-bit input and output ports to a maximum of 88 ports (all TTL compatible)

ROM resident system monitor includes all necessary functions for program loading, debugging, and execution

RAM resident macro assembler used to assemble all 8080 machine instructions with full macro and conditional assembly capabilities

RAM resident text editor with powerful string search, substitution, insertion, and deletion commands

The Intellec® MDS is a modular microcomputer development system containing all necessary hardware and software to develop and implement Intel MCS™-80 and Series 3000 microcomputer systems. The addition of MDS options and peripherals provides the user with a complete in-circuit microcomputer development system, supporting product design from program development through prototype debug, to production and field test.

INTELLEC HARDWARE

The standard Intellec® MDS consists of four microcomputer modules (CPU, 16K RAM Memory, Front Panel Control, and Monitor), an interconnecting printed circuit motherboard, power supplies, fans, a chassis, and a front panel. Modular expansion capability is provided by 14 additional sockets on the motherboard.

The CPU module uses Intel's powerful NMOS 8-bit 8080 microprocessor. The 8080's 2 μs cycle time, 78 instructions, unlimited subroutine nesting, vectored interrupt, and DMA capabilities are fully utilized by the Intellec MDS. Bus control logic resolves bus contention conflicts between the CPU module and other modules capable of acquiring control of the bus. The CPU module interfaces with a sixteen line address bus and a bidirectional eight line data bus. 8080 status signals are decoded and utilized for memory and I/O operations. An eight-level, nested interrupt priority system, complete with an interrupt priority push-down stack, resolves contention for 8080 interrupt servicing.

The RAM memory module contains 16K bytes of Intel 2107A dynamic RAM which operates at full processor speed. All necessary address decoding and refresh logic is contained on the module.

The front panel control module provides system initialization, priority arbitration, and real time clock functions. System initialization routines reside in a 256 byte, PROM resident, bootstrap loader. An eight-level priority arbitration network resolves bus contention requests among potential bus masters. A 1 ms interrupt request generator, which can be disabled under program control, provides real time clock functions. A 10 ms automatic time-out feature is also provided to force an interrupt request if nonexistent memory or I/O is addressed.

The Monitor module contains the Intellec MDS system monitor and all Intellec MDS peripheral interface hardware. The system monitor resides in a 2K byte Intel 8316 ROM. The module contains all necessary control and data transfer circuitry to interface with the following Intellec MDS peripherals:

- Teletype
- CRT
- High Speed Paper Tape Reader
- High Speed Paper Tape Punch
- PROM Programmer
- Line Printer

The Intellec MDS universal bus structure enables several CPU and DMA devices to share the bus by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal which is derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure contains provisions for up to 16-bit address and data transfers and is not limited to any one Intel microcomputer family.

The Intellec MDS front panel is intended to augment the primary user interaction medium, the system console. The simplicity of the front panel coupled with the power of the system monitor provides an efficient user/Intellec interface. The front panel contains eight interrupt request **switches** with corresponding indicators, CPU RUN and HALT **status**

indicators, a bootstrap loader switch, RESET switch, and a POWER ON switch and indicator.

The basic Intellec MDS capabilities may be significantly enhanced by the addition of the following optional features.

ICE (In-Circuit Emulator) extends Intellec MDS diagnositc capabilities into user configured systems. The Intellec MDS resident ICE processor operates in conjunction with the MDS host CPU and interfaces to the user system via an external cable. The ICE processor replaces the user system processor providing real time emulation capability. MDS resident memory and I/O may be substituted for equivalent user system elements, allowing the hardware designer to sequentially develop his system by integrating MDS and user system hardware. MDS display and debug hardware eliminate the need for specially constructed user system equivalents. Augmenting these capabilities are such powerful ICE debug functions as setting breakpoints, tracing program flow, single stepping, examining and altering CPU registers and memory locations.

The Universal PROM Programmer is an Intellec MDS peripheral capable of programming and verifying the following Intel PROMs: 1702A, 2704, 2708, 3601, 3604, 3624, 8702A, 8704, and 8708. Programming and verification operations are initiated from the Intellec MDS system console and are controlled by programs resident in the Intellec MDS and Universal PROM Programmer.

The addition of a single or dual drive Diskette Operating System significantly reduces program development time. An intelligent controller, constructed around Intel's powerful Series 3000 computing elements, provides diskette interface and control. Intel's software operating system (IDOS) in conjunction with the diskette operating system hardware provides a highly efficient and easy to use method of assembling, editing, and executing programs.

Customized user I/O requirements may be satisfied by adding I/O modules. Each I/O module contains four 8-bit input ports (latched or unlatched), four 8-bit latched output ports (with adjustable strobe pulses), and eight system interrupt lines. All inputs and outputs are TTL compatible. Optional I/O may be expanded to a maximum of 44 input and 44 output ports.

Memory may be expanded by adding RAM or PROM modules in user defined combinations. Up to 64K bytes of RAM may be added in 16K byte increments. PROM (Intel 8702A) may be added in 256 byte increments by adding PROM modules with socket capacity for 6K bytes and populating each module with the desired number of PROMs. Maximum PROM capacity is 12K bytes. RAM/PROM memory overlap is resolved by giving PROM priority.

DMA (direct memory access) modules work in conjunction with the Intellec MDS universal bus to maximize the efficiency of data transfers between MDS memory and selected I/O devices. Each module contains all the necessary control and data transfer logic to implement a complete DMA channel.

A ROM simulator composed of high speed bipolar RAM emulates Series 3000 bipolar microprogram ROM memory. Each ROM simulator module may be used in 512 X 16 or 1024 X 8 configurations.

INTELLEC SOFTWARE

Resident software provided with the Intellec MDS includes the system monitor, 8080 macro assembler and text editor. Used together, these three programs simplify program preparation and speed the debugging task.

The system monitor provides complete control over operation of the Intellec MDS. All necessary functions for program loading and execution are provided. Additional commands provide extensive debug facilities and PROM programming functions. System peripherals may be dynamically assigned either via monitor commands or through calls to the system monitor's I/O subroutines.

Programs may be loaded from the reader device in either BNPF or hexadecimal format. Utility commands which aid in the execution and checkout of programs include:

- initialize memory to a constant
- move a block of memory to another location
- display memory
- modify RAM memory
- examine and modify CPU registers
- set breakpoints
- initiate execution at any given address
- perform hexadecimal arithmetic
- examine and modify the interrupt mask

The Intellec MDS System Monitor contains a powerful and easily expandable input/output system, which is built around four logical device types; console device, reader device, punch device and list device. Associated with each logical device may be any one of four physical devices. The user controls physical device assignment to each logical device through a System command.

Drivers are provided in the system monitor for the Universal PROM Programmer, ASR 33 teletype, high speed paper tape reader, high speed paper tape punch, line printer, and CRT. The user may write his own drivers for other peripheral devices and easily link them to the system monitor.

All system peripherals may be accessed simply by calling I/O subroutines in the system monitor. In addition, the user may dynamically reconfigure his system by monitor commands or by calling system subroutines which can assign a different physical device to each logical device. The user may also determine the current system peripheral configuration, check I/O status and determine the size of available memory.

The monitor is written in 8080 Assembly Language and resides in 2K bytes of ROM memory.

The Intellec MDS Resident Assembler translates symbolic 8080 assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation.

Conditional assembly permits the assembler to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

The assembler performs its function in three passes. The first pass builds the symbol table. The second pass produces a source listing and provides error diagnostics. The third pass produces the object code. If the punch and list devices are separate (e.g. a high speed punch or printer is available) passes 2 and 3 may be combined into one pass.

Object code produced by the assembler is in hexadecimal format. It may be loaded directly into the Intellec MDS for execution and debugging or may be converted by the system monitor to BNPF format for ROM programming.

The assembler is written in PL/M$^{T.M.}$-80, Intel's high level systems programming language. It occupies 12K bytes of RAM memory including space for over 800 symbols. The symbol table size may be expanded to a maximum of 6500 symbols by adding RAM memory. All I/O in the assembler is done through the system monitor, enabling the assembler to take advantage of the monitor's I/O system. The assembler is shipped in hexadecimal object format on paper tape or diskette and is standard with each Intellec MDS.

The Intellec MDS editor is a comprehensive tool for the entry and correction of assembly language programs for the Intel 8080 microcomputer. Its command set allows manipulation of either entire lines of text or individual characters within a line.

Programs may be entered directly from the console keyboard or from the system reader device. Text is stored internally in the editor's workspace, and may be edited with the following commands:

- string insertion or deletion
- string search
- string substitution

To facilitate the use of these editing commands, utility commands are used to change positions in the workspace. These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

The contents of the workspace may be listed to the system console or written to the system list or punch device for future use.

The text editor is written in PL/M$^{T.M.}$-80. It occupies 8K bytes of RAM memory, including over 4500 bytes of workspace. The workspace may be expanded to a maximum of 58K bytes by adding RAM memory. All I/O in the editor is done through the system monitor, enabling the editor to take advantage of the monitor's I/O system. The editor is shipped in hexadecimal object format on paper tape or diskette and is standard with each Intellec MDS.
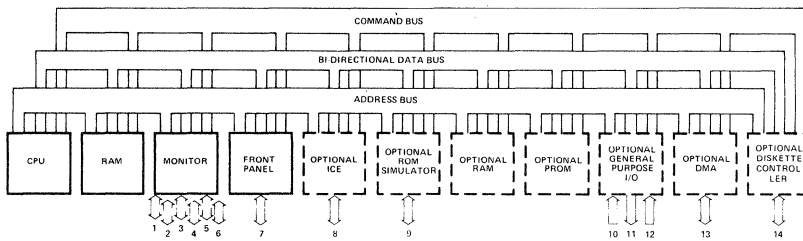
NOTES:
1. PROM PROGRAMMER DATA/STATUS/COMMANDS
2. HIGH SPEED PUNCH DATA/STATUS/COMMANDS
3. HIGH SPEED READER DATA/STATUS/COMMANDS
4. PRINTER DATA/STATUS/COMMANDS
5. CRT DATA/STATUS/COMMANDS
6. TTY DATA/STATUS/COMMANDS
7. FRONT PANEL STATUS/SWITCH INPUTS
8. USER SYSTEM CPU OR MCU PIN SIGNALS
9. USER SYSTEM ROM PIN SIGNALS
10. EIGHT INTERRUPT LINES
11. FOUR 8-BIT OUTPUT PORTS
12. FOUR 8-BIT INPUT PORTS
13. DMA DEVICE DATA/STATUS/COMMANDS
14. DISKETTE DRIVE DATA/STATUS/COMMANDS

HARDWARE SPECIFICATIONS

WORD SIZE
Host Processor (Intel 8080)
    Data: 8 bits
    Instruction, 8, 16, or 24 bits

MEMORY SIZE
RAM: 16K bytes expandable to 64K bytes using optional modules.

ROM: 2K bytes expandable to 14K bytes in 256 byte increments using optional PROM modules.

PROM: 256 bytes expandable to 12K bytes using optional modules.

Total: RAM, ROM and PROM may be combined in user defined configurations up to a maximum of 64K bytes.

MACHINE CYCLE TIME
Host Processor (Intel 8080): 2.0 μS

BUS TRANSFER RATE
Maximum bus transfer rate of 5 MHz.

SYSTEM CLOCKS
Host Processor (Intel 8080) Clock: Crystal controlled at 2 MHz ±0.1%.
Bus Clock: Crystal controlled at 9.8304 MHz ±0.1%.

I/O INTERFACES
CRT:
    Baud Rates: 110/300/600/1200/2400/4800/9600 (selectable).
    Code Format: 7–12 level code (programmable).
    Parity: Odd/even (programmable).
    Interface: TTL/RS232C (selectable).

TTY:
    Baud Rate: 110
    Code Format:
        Input: 10 level or greater.
        Output: 11 level.
        Parity: Odd.
        Interface: 20 mA current loop.

High Speed Paper Tape Reader:
    Transfer Rate: 200 cps.
    Control: 2-bit output.
               1-bit input.
    Data: 8-bit byte
    Interface: TTL

Punch:
    Transfer Rate: 75 cps
    Control: 2-bit output
               1-bit input
    Data: 8-bit byte
    Interface: TTL

Printer:
    Transfer Rate: 165 cps
    Control: 2-bit status input
               1-bit output
    Data: ASCII
    Interface: TTL

PROM Programmer:
    Control: 3 strobes for multiplexed output data.
    Data: 8-bit bidirectional
    Interface: TTL

GENERAL PURPOSE I/O (OPTIONAL)
Input Ports: 8-bit TTL compatible (latched or unlatched); expandable in 4 port increments to 44 input ports.
Output Ports: 8-bit TTL compatible (latched); expandable in 4 port increments to 44.
Interrupts: 8 TTL compatible interrupt lines.

INTERRUPT
8-level, maskable, nested priority interrupt network initiated from front panel or user selected devices.

DIRECT MEMORY ACCESS
Standard capability on Intellec bus; implemented for user selected DMA devices through optional DMA module — maximum transfer rate of 2 MHz.

MEMORY ACCESS TIME
RAM: 450 ns
PROM: 1.3 μs using Intel 8708A PROM.

PHYSICAL CHARACTERISTICS
Dimensions: 8.5″ X 19″ X 17″
               21.6 cm X 48.3 cm X 43.2 cm
Weight: 65 lb (29.5 kg)

ELECTRICAL CHARACTERISTICS

DC POWER SUPPLY (Volts)	POWER SUPPLY CURRENT (Amps)	BASIC SYSTEM CURRENT REQUIREMENTS (Amps)	
		Maximum	Typical
+ 5 ±5%	35.0	9.0	6.6
+12 ±5%	3.0	0.7	0.4
−10 ±5%	3.0	0.2	0.2
−12 ±5%	0.5	—	—

AC POWER REQUIREMENTS
50–60 Hz; 115/230 VAC; 150 Watts

ENVIRONMENTAL CHARACTERISTICS
Operating Temperature: 0 to 55°C

SOFTWARE SPECIFICATIONS

CAPABILITIES

System Monitor:
  Devices supported include:
    ASR 33 teletype
    Intel high speed paper tape reader
    Paper tape punch
    CRT
    Printer
    Universal PROM programmer
    4 logical devices recognized
    16 physical devices maximum allowed

Macro Assembler:
  800 symbols in standard system; automatically expandable with additional RAM memory to 6500 symbols maximum.

  Assembles all seventy-eight 8080 machine instructions plus 10 pseudo-operators.

Text Editor:
  12K bytes of workspace in standard system; automatically expandable with additional RAM memory to 58K bytes.

OPERATIONAL ENVIRONMENTAL

System Monitor:
  Required hardware:
    Intellec MDS
    331 bytes RAM memory
    2K bytes ROM memory
    System console

Macro Assembler:
  Required hardware:
    Intellec MDS
    12K bytes RAM memory
    System console
    Reader device
    Punch device
    List device
  Required software:
    System monitor

Text Editor:
  Required hardware:
    Intellec MDS
    8K bytes RAM memory
    System console
    Reader device
    Punch device
  Required software:
    System monitor

Tape Format:
  Hexadecimal object format.

MDS OPTIONS
MDS-016   16K Dynamic RAM
MDS-406   6K PROM (sockets and logic)
MDS-501   DMA Channel Controller
MDS-504   General Purpose I/O Module
MDS-600   Prototype Module
MDS-610   Extender Module
MDS-620   Rack Mounting Kit

MDS EMULATORS/SIMULATOR
MDS-ICE-30   3001 In-Circuit Emulator
MDS-ICE-80   8080 In-Circuit Emulator
MDS-SIM-100   Bipolar ROM Simulator

MDS PERIPHERALS
MDS-UPP   Universal PROM Programmer
MDS-PTR   High Speed Paper Tape Reader
MDS-DOS   Diskette Operating System

MDS INTERFACE CABLES/CONNECTORS
MDS-900   CRT Interface Cable
MDS-910   Line Printer Interface Cable
MDS-915   High Speed Reader Interface Cable
MDS-920   High Speed Punch Interface Cable
MDS-930   Peripheral Extension Cable
MDS-940   DMA Cable
MDS-950   General Purpose I/O Cable
MDS-960   25-pin Connector Pair
MDS-970   37-pin Connector Pair
MDS-980   60-pin Motherboard Auxiliary Connector
MDS-985   86-pin Motherboard Main Connector
MDS-990   100-pin Connector Hood

EQUIPMENT SUPPLIED
Central Processor Module
RAM Memory Module
Monitor Module (System I/O)
Front Panel Control Module
Chassis with Motherboard
Power Supplies
Finished Cabinet
Front Panel
ROM Resident System Monitor
RAM Resident Macro Assembler
RAM Resident Text Editor
Hardware Reference Manual
Reference Schematics
Operator's Manual
8080 Assembly Language Programming Manual
System Monitor Source Listing
8080 Assembly Language Reference Card
TTY Cable
European AC Adapter
AC Cord

ICE-80 8080
IN-CIRCUIT EMULATOR

Connects Intellec® MDS to user configured system via an external cable and 40-pin plug, replacing the user 8080

Allows real-time (2 MHz) emulation of the user system 8080

Allows user configured system to share Intellec® MDS RAM, ROM and PROM memory and Intellec® MDS I/O facilities

Checks for up to three hardware and four software break conditions

Offers full symbolic debugging capabilities

Eliminates the need for extraneous debugging tools residing in the user system

Provides address, data and 8080 status information on last 44 machine cycles emulated

Provides capability to examine and alter CPU registers, main memory, pin and flag values

Integrates hardware and software development efforts

Available in diskette or paper tape versions

The Intellec® MDS In-Circuit Emulator/80 (ICE-80) is an Intellec® MDS resident module that interfaces to any user configured 8080 system. With ICE-80 as a replacement for a prototype system 8080, the designer can emulate the system's 8080 in real time, single-step the system's program, and substitute Intellec® MDS memory and I/O for user system equivalents. Powerful Intellec® MDS debug functions are extended into the user system. For the first time the designer may examine and modify his sytem with symbolic references instead of absolute values.
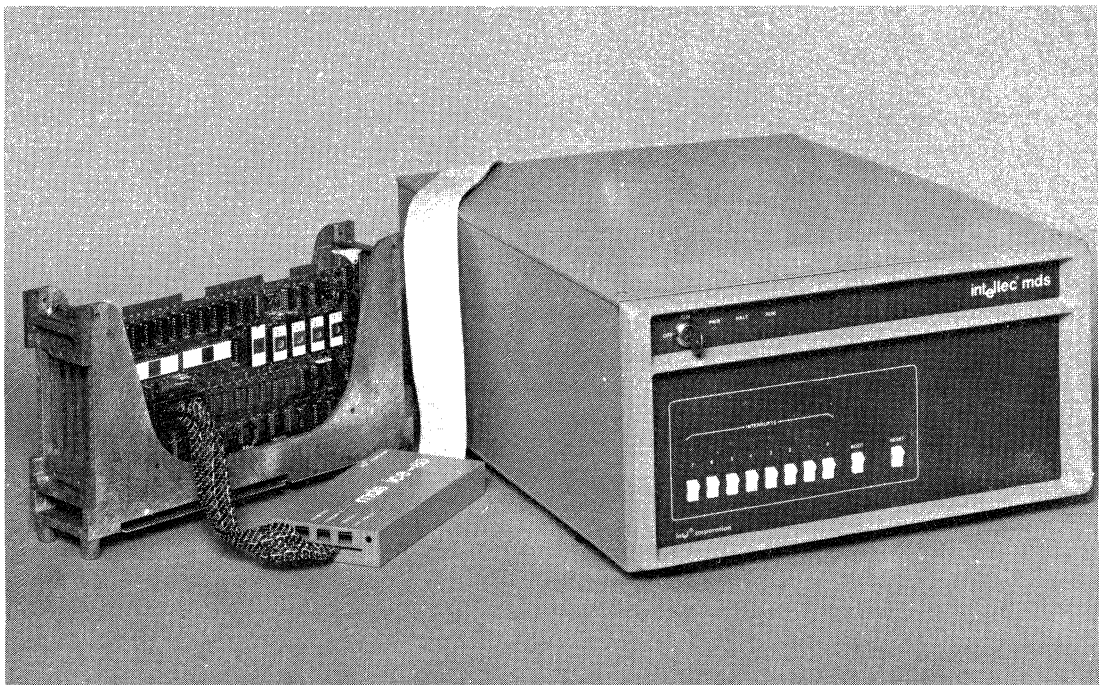
INTEGRATED HARDWARE/ SOFTWARE DEVELOPMENT

The user prototype need consist of no more than an 8080 CPU socket and a user bus to begin integration of software and hardware development efforts. Through ICE-80 mapping capabilities, MDS equivalents can be accessed for missing prototype hardware. Hardware designs can be tested using the system software which will drive the final product.

The system integration phase, which can be so costly and frustrating when attempting to mesh completed hardware and software products, becomes a convenient two-way debug tool when begun early in the design cycle.

SYMBOLIC DEBUGGING

ICE-80 allows the user to make symbolic references to memory addresses and data in his program. Symbols may be substituted for numeric values in any of the ICE-80 commands. The user is relieved from looking up addresses of variables or program subroutines.

The user symbol table generated along with the object file during a PL/M compilation or a MAC80 or MDS assembly, is loaded to MDS memory along with the user program which is to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables that are found useful during system debugging. By referring to symbolic memory addresses, the user can be assured of examining, changing, or breaking at the intended location.

ICE-80 provides symbolic definition of all 8080 registers, flags, and selected pins. The following symbolic references are also provided for user convenience: TIMER, a 16-bit register containing the number of ϕ_2 clock pulses elapsed during emulation; ADDRESS, the address of the last instruction emulated; INTERRUPTENABLED, the user 8080 interrupt mechanism status; and UPPERLIMIT, the highest MDS RAM address that can be occupied by user memory.

DEBUG CAPABILITY INSIDE USER SYSTEM

ICE-80 provides the user with the ability to debug a full prototype or production system without introducing extraneous hardware or software test tools.

ICE-80 connects to the user system through the socket provided for the user 8080 in the user system. Intellec® MDS memory is used for the execution of the ICE-80 software, while MDS I/O provides the user with the ability to communicate with ICE-80 and receive information on the operation of the user system.

MEMORY AND I/O MAPPING

Memory and I/O for the user system can be resident in the user system or "borrowed" from the MDS through ICE-80's mapping capability.

ICE-80 separates user memory into 16 4K blocks. User I/O is divided into 16 16-port blocks. Each block of memory or I/O can be defined independently. The user may assign MDS equivalents to take the place of devices not yet designed for the user system during prototyping. In addition, proven MDS memory or I/O can be accessed in place of suspect user system devices during prototype or production checkout.

The user can also designate a block of memory or I/O as nonexistent. ICE-80 issues error messages when memory or I/O designated as nonexistent is accessed by the user program.
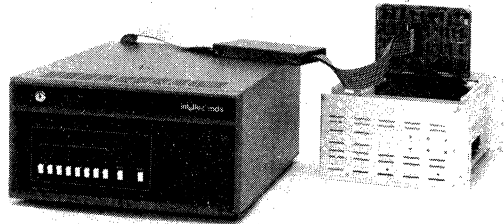
ICE-80 INSTALLED IN USER SYSTEM

REAL TIME TRACE

ICE-80 captures valuable trace information while the user is executing programs in real time. The 8080 status, the user memory or port addressed, and the data read or written (snap data), is stored for the last 44 machine cycles executed. This provides ample data for determining how the user system was reacting prior to emulation break. It is available whether the break was user initiated or the result of an error condition.

For detailed information on the actions of CPU registers, flags, or other system operations, the user may operate in single or multiple-step sequences tailored to system debug needs.

HARDWARE

The heart of ICE-80 is a microcomputer system utilizing Intel's 8080 microprocessor as its nucleus. This system communicates with the Intellec® MDS host processor via I/O commands. Host processor commands and ICE-80 status are interchanged through registers on the ICE-80 Trace Board. ICE-80 and the MDS also communicate through a Control Block resident in the Intellec® MDS main memory which contains detailed configuration and status information transmitted at an emulation break.

ICE-80 hardware consists of two PC boards, the Processor and Trace Boards, residing in the Intellec® MDS chassis, and a 6-foot cable which interfaces to the user system. The Trace and Processor Boards communicate with the MDS on the MDS bus, and also with each other on a separate ICE-80 bus. ICE-80 connects to the user system through a cable that plugs directly into the socket provided for the user's 8080.

TRACE BOARD

The Trace Board talks to the MDS as a peripheral device. It receives MDS commands to ICE-80 and returns ICE-80 responses.

While ICE-80 is executing the user program, the Trace Board collects data for each machine cycle emulated (snap data). The information is continuously stored in high-speed bipolar memory.

The Trace Board also contains two 24-bit hardware breakpoint registers which can be loaded by the user. While in emulation mode, a hardware comparitor is constantly monitoring address and status lines for a match which will terminate an emulation. A user probe is also available which can be attached to any user signal. When this signal goes true a break condition is recognized.

The Trace Board signals the Processor Board when an MDS command to ICE-80 or a break condition has been detected. The ICE-80 CPU then sends data stored on the Trace Board to the Control Block in MDS memory. Snap data, along with information on 8080 registers and pin status, and the reason for the emulation break are then available for access during interrogation mode. Error conditions, if present, are transmitted and automatically displayed for the user.

PROCESSOR BOARD

An 8080 CPU resides on the Processor Board. During emulation it executes instructions from the user's program. At all other times it executes instructions from the control program in the Trace Module's ROM.

The Processor Board contains an internal Clock Generator that provides the clocks to the user emulation CPU at 2 MHz. The CPU can alternately be driven by a clock derived from user system signal lines. The clock source is selected by a jumper option on the board. A timer on the Trace Board counts the ϕ_2 clock pulses during emulation and can provide the user with the exact timing of the emulation.

The Processor Board turns on an emulation when ICE-80 has received a RUN command from the MDS. It terminates emulation when a break condition is detected on the Trace Board, or the user's program attempts to access memory or I/O ports designated as nonexistent in the user system, or the user 8080 is inactive for a quarter of a second.

The Address Map located on the Processor Board stores the assigned location of each user memory or I/O block. During emulation the Processor Board determines whether to send/receive information on the MDS or User bus by consulting the Address Map. The Processor Board allows the ICE-80 CPU to gain access to the MDS bus as a master to "borrow" MDS facilities. At an emulation break, the Processor Board stores the status of specified 8080 input and output signals, disables all interaction with the user bus, and commands the Trace Board to send stored information to a Control Block in MDS memory for access during interrogation mode.

CABLE CARD

The Cable Card is included for cable driving. It transmits address and data bus information to the user system through a 40-pin connector which plugs into the user system in the socket designed for the 8080 when enabled by the Processor Module's user bus control logic.

SOFTWARE

The ICE-80 software driver (ICE80SD) is an MDS RAM-based program which provides the user with easy-to-use English language commands for defining breakpoints, initiating emulation, and interrogating and altering user system status recorded during emulation. ICE-80 commands are configured with a broad range of modifiers which provide the user with maximum flexibility in describing the operation to be performed.

ICE80SD is available in both paper tape and diskette-based versions. The diskette-based version, which is supplied on a System Diskette for operation with the Intellec® MDS Diskette Operating System, provides expanded capabilities for retrieving and storing user programs, as well as the standard MDS peripherals available in the paper tape version.

EMULATION COMMANDS:

GO
: Initiates real-time emulation and allows user to specify breakpoints, data retrieval, and conditions under which emulation should be reinitiated.

STEP
: Initiates emulation in single or multiple instruction increments. User may specify a register dump or tailor diagnostic activity to his needs following each step, and define conditions under which stepping should continue.

RANGE
: Delimits blocks of instructions for which register dump or tailored diagnostics are to occur.

CONTINUE
: Resume real-time emulation.

CALL
: Emulate user system interrupt.

INTERROGATION COMMANDS:

BASE
: Establish mode of display for output data.

DISPLAY
: Print contents of memory, 8080 registers, input ports, 8080 flags, 8080 pins, snap data, symbol table, or other diagnostic data on list device. Can also be used for base-to-base conversion, or addition or subtraction in any base.

CHANGE
: Alter contents of memory, register, output port, or 8080 flag.

XFORM
: Define memory and I/O status.

SEARCH
: Look through memory range for specified value.

UTILITY COMMANDS:

LOAD
: Fetch user symbol table and object code from input device.

SAVE
: Send user symbol table and object code to output device.

EQUATE
: Enter symbol name and value to user symbol table.

FILL
: Fill memory range with specified value.

MOVE
: Move block of memory data to another area of memory.

TIMEOUT
: Enable/disable user CPU 1/4 second wait state timeout.

LIST
: Define list device (diskette-based version only).

EXIT
: Return program control to MDS monitor.
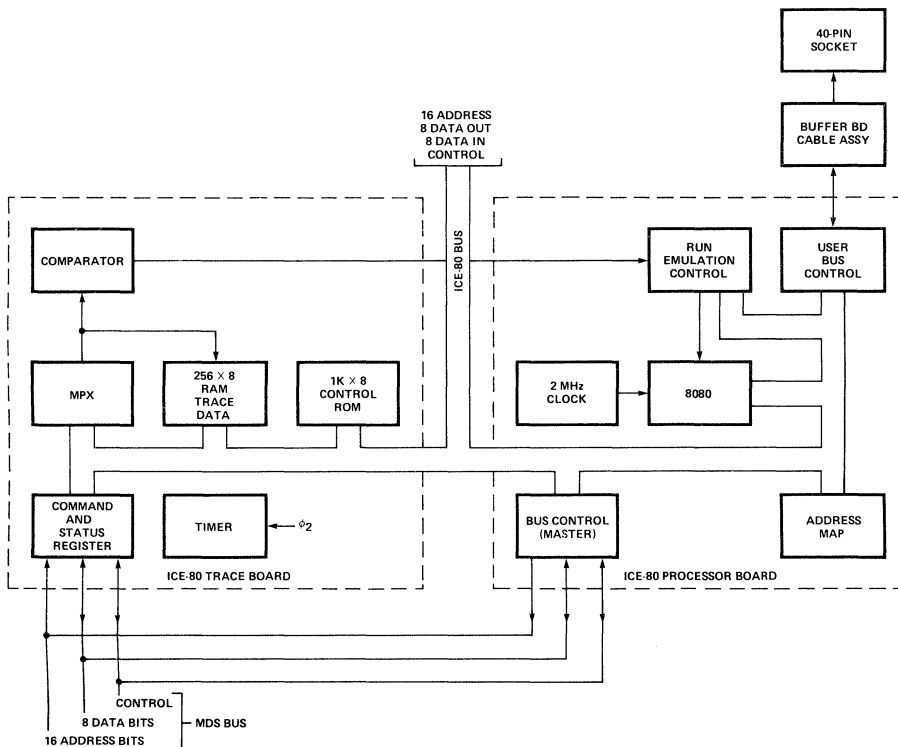
FUNCTIONAL BLOCK DIAGRAM OF ICE-80 MODULE

SAMPLE, ICE-80 DEBUG SESSION

ISIS 8080 MACRO ASSEMBLER, V1.0   PAGE 1

```
                      ; USER PROGRAM TO OUTPUT A SERIES OF
                      ; CHARACTERS TO SDK-80 CONSOLE DEVICE
                      ;
1320                      ORG    1320H
01E3      CO          EQU    1E3H    ; SDK-80 CONSOLE OUT DRIVER
                      ;
1320 0601  START: MVI    B,1      ; SET UP B VALUE
1322 3A3613        LDA    DAT1     ; LOAD A WITH DAT1 VALUE
1325 4F    LOOP:  MOV    C,A
1326 CDE301        CALL   CO       ; SEND C VALUE TO CONSOLE
1329 79            MOV    A,C      ; RESTORE A
132A 93            SBB    B        ; SUBTRACT B FROM A
132B 323713        STA    RSLT     ; STORE RESULT IN RSLT
132E FE40          CPI    40H      ; LAST VALUE TO PRINT
1330 C22513        JNZ    LOOP     ; LOOP AGAIN IF A>40H
1333 C32013        JMP    START    ; ELSE RESTART WHOLE PROCEDURE
                      ;
1336 5A    DAT1:  DB     5AH
1337       RSLT:  DS     1
0000              END
```

```
ISIS, V1.0      INITIAL ICE-80 SESSION
–ICE80          (Note: The SDK-80 Monitor has already been used to initialize the SDK-80 Board)
ISIS ICE-80, V1.0
① **XFORM MEMORY 0 TO 1 U
   *XFORM IO 0FH U
② *LOAD PROG. HEX
   ERR=067
   STAT=11H TYPE=06H CMND=07H ADDR=1320H GOOD=06H BAD=04H
   *CHANGE MEMORY 1321H=FFH
   ERR=067
   STAT=11H TYPE=06H CMND=07H ADDR=1321H GOOD=FFH BAD=FDH
   *LOAD PROG. HEX
③ *GO FROM START UNTIL RSLT WRITTEN
   EMULATION BEGUN
④ ERR=067
   STAT=11H TYPE=07H CMND=02H
⑤ *DISPLAY CYCLES 5

   STAT=A2H ADDR=1326H DATA=CDH
   STAT=82H ADDR=1327H DATA=E3H
   STAT=82H ADDR=1328H DATA=01H
   STAT=04H ADDR=FFFFH DATA=13H
   STAT=04H ADDR=FFFEH DATA=29H
⑥ *CHANGE DOUBLE REGISTER SP=13FFH
   *BASE HEX
   *EQUATE STOP=1333H
⑦ *GO FROM START UNTIL STOP EXECUTED THEN DUMP
   EMULATION BEGUN
   B=01H C=41H D=00H E=00H H=00H L=00H F=56H A=40H P=1320H *=1333H S=13FFH
   EMULATION TERMINATED AT 1333H
⑧ *EXIT
   *FFFF
```

1. Set up user memory and I/O. The program is set up to execute in block 1 (1000H–1FFFH) of user memory, and requires access to the SDK-80 monitor (block 0) and I/O ports in block 0FH. Both ports and memory are defined as available to the user system. All other memory and I/O is initialized by ICE-80 as nonexistent (guarded).

2. A load command generates an error. The type and command numbers indicate that a data mismatch occurred on a write to memory command. The data to be written to address 1320H should have been 06H. When ICE-80 read the data after writing it, a 04H was detected. A change command to a different memory address hints that bit 1 does not go to 1 anywhere in this memory block. Examination indicates that a pin was shorted on the RAM located at 1300H–13FFH in the prototype system. The problem is fixed and a subsequent load succeeds.

3. A real-time emulation is begun. The program is executed FROM 'START' (1320H) and continues UNTIL 'RSLT' is written (in location 1328H, the contents of the accumulator is stored in (written into) 'RSLT').

4. An error condition results: TYPE 07, CMND 02 indicate the program accessed a guarded area.

5. The last 5 machine cycles executed are displayed. The last instruction executed was a call (CDH). The fourth and fifth cycles are a push operation (designated by status 04H) to store the program counter before executing the call. The stack pointer was not initialized in the program and is accessing memory location FFFFH.

6. After making a note to initialize the stack pointer in the next assembly, a temporary fix is effected by setting the stack pointer to the top of user available memory.

7. After setting the base for displays to hex and adding the symbol 'STOP' to the symbol table, emulation is started which will terminate when the instruction at 1333H ('STOP') is executed. When emulation terminates, a DUMP of the contents of user 8080 registers is requested. One can see that the value of the accumulator is set at 40H, the stack pointer is set at 13FFH, the last address executed (*) is 1333H, and the program counter has been set to 1320H.

8. EXIT returns control to the MDS monitor.

ICE80SD OPERATING ENVIRONMENT

Paper Tape-Based ICE80SD

Required Hardware:
   Intellec® MDS
   System console
   MDS Reader device
   MDS Punch device
   ICE-80

Required Software:
   System monitor

Diskette-Based ICE80SD

Required Hardware:
   Intellec® MDS
   32K bytes RAM memory
   System console
   MDS-DOS Diskette Operating System
   ICE-80

Required Software:
   System monitor
   ISIS

EQUIPMENT SUPPLIED

Printed Circuit Modules (2)
Interface Cables and Buffer Board
Hardware Reference Manual
Operator's Manual
Schematic Diagram
ICE-80 Software Driver, paper tape version
   (ICE-80 Software Driver, disketted-based version is
   supplied with MDS Diskette Operating System)

SYSTEM CLOCK

Crystal controlled 2.185 MHz ±0.01%. May be replaced by user clock through jumper selection.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 8.00 lb (3.64 kg)

ELECTRICAL CHARACTERISTICS

DC Power:
   V_{CC} = +5V, ±5%
   I_{CC} = 9.81A maximum; 6.90A typical
   V_{DD} = +12V, ±5%
   I_{DD} = 79 mA maximum; 45 mA typical
   V_{BB} = –9V, ±5%
   I_{BB} = 1 mA maximum; 1 μA typical

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0°C to 40°C
Operating Humidity: Up to 95% relative humidity without condensation

CONNECTORS

Edge Connector: CDC VPB01E32A00A1

ORDERING INFORMATION

Part Number	Description
MDS-80-ICE	8080 CPU In-Circuit Emulator. Cable Assembly and Interactive Software included

UPP UNIVERSAL PROM PROGRAMMER

Intellec® MDS peripheral capable of programming the following Intel® PROMs: 1702A, 2704, 2708, 3601, 3604, 3624, 8702A, 8704 and 8708

Personality cards used for specific Intel® PROM programming requirements

Zero insertion force sockets for both 16-pin and 24-pin PROMs

Flexible power source for system logic and programming pulse generation

PROM programming verification facility

Stand-alone or rack-mountable

The Universal PROM Programmer is an Intellec MDS peripheral capable of programming and verifying the following Intel PROMs: 1702A, 2704, 2708, 3601, 3604, 3624, 8702A, 8704, and 8708. Programming and verification operations are initiated from the Intellec MDS system console and are controlled by programs resident in the Intellec MDS and Universal PROM Programmer.

The basic MDS-UPP consists of a controller module, two personality card sockets, front panel, power supplies, chassis, and an Intellec MDS interconnection cable. An Intel 4040 based intelligent controller monitors the Intellec MDS interface and controls the command generation and data transfer interface between the selected PROM personality card and the Intellec MDS. The 4040 CPU operates in conjunction with a fixed central control program residing in an Intel 4001 ROM. Each Intel PROM to be programmed is driven by a unique personality card which contains the appropriate pulse generation functions and driver circuitry. Hence, programming and verifying any Intel PROM may be accomplished by selecting and plugging in the appropriate personality card option. The front panel contains a power-on switch and indicator, reset switch, and two zero-force insertion sockets (one 16-pin and one 24-pin or two 24-pin). A central power supply provides regulated power for system logic and ±40 and +70 volts for PROM programming pulse generation.

PROM programming commands are initiated from the Intellec MDS system console and are implemented by programs in the Intellec MDS. The desired PROM image is loaded into Intellec MDS RAM through a user selected input medium (e.g., TTY, diskette drive, high speed paper tape reader). Next, the PROM programming command is issued specifying the location of the programming data, the socket option, the "nibble" option (upper or lower four bits of an 8-bit RAM data byte), and PROM starting address. The PROM programming algorithm programs each specified PROM location, compares the resulting PROM word with the source data, and regenerates program pulses when necessary. The Intellec MDS system monitor contains a compare feature which allows specified sections of programmed PROM to be compared with MDS resident RAM. A transfer feature which can be used to copy the contents of a PROM to MDS RAM for PROM duplication is also included.

The Universal PROM Programmer may be used as a table top unit or mounted in a standard 19" RETMA cabinet.
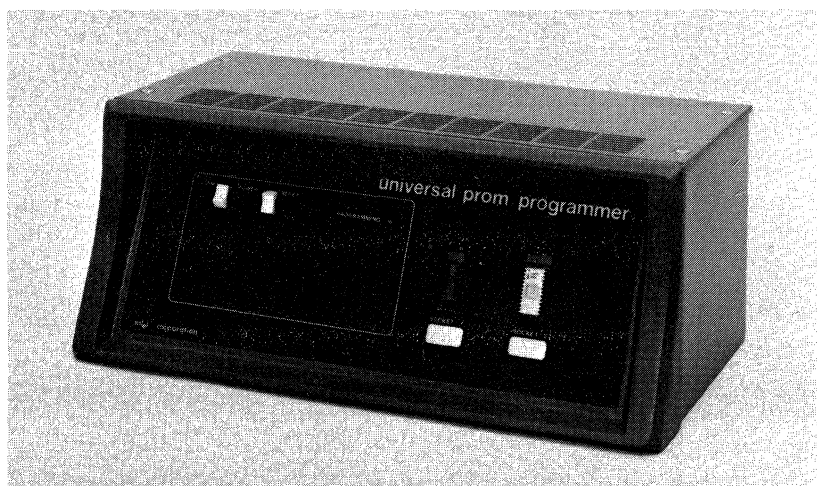
SPECIFICATIONS

INTERFACE
Data: Two 8-bit unidirectional buses
Commands: 3 Write Commands
2 Read Commands
Initiate Command

AVERAGE PROGRAMMING TIME
1702A/8702A: 40 seconds
2708/8708: 5 minutes
3601: 2 seconds
3604: 10 seconds
3624: 10 seconds
2704/8704: 2.5 minutes

PHYSICAL CHARACTERISTICS
Dimensions: 6" X 7" X 17"
14.7 cm X 17.2 cm X 41.7 cm
Weight: 18 lb (8.2 kg)

ELECTRICAL CHARACTERISTICS
DC Power Supplies:

Voltage	Current
5V	2.5A
−10V	0.75A
±40V	0.5A
70V	0.4A

AC Power Requirements:
50−60 Hz; 115/230 VAC; 80 Watts

ENVIRONMENTAL CHARACTERISTICS
Operating Temperature: 0° to 70°C.

OPTIONS
Personality Cards:
MDS-UPP-361:3601 Personality Card
MDS-UPP-864:8604/3604/3624 Personality Card
MDS-UPP-872:8702A/1702A Personality Card
MDS-UPP-878:8708/8704/2708/2704 Personality Card

PROM Programming Sockets:
MDS-UPP-501: 16-pin/24-pin pair
MDS-UPP-502: 24-pin/24-pin pair

EQUIPMENT SUPPLIED
Cabinet
Power Supplies
4040 Intelligent Controller Module
Specified Zero Insertion Force Socket Pair
Intellec MDS Interface Cable
Hardware Reference Manual
Reference Schematics

μSCOPE™ 820
MICROPROCESSOR SYSTEM CONSOLE

Provides an interface to microcomputer systems for troubleshooting system problems

Monitors, displays, and alters register, memory and I/O values for system under test

Executes diagnostic routines from μScope 820 console overlay memory

Executes instrument resident software patch routines even when microcomputer system is ROM-based

Provides a 32-bit hardware breakpoint with bit masking and a 256-word trace memory

Is a stand-alone, self-contained, rugged portable unit

Human engineered with easy to read 9-segment hexadecimal displays and extensive operator prompting

Gives complete control over microprocessor including single step, run with display, or run real-time capability

Designed to support many different microprocessors

Has built-in, self-test operation

The μScope™ 820 Microprocessor System Console is a portable, self-contained instrument designed to provide the control, monitoring, and interaction necessary to effectively and quickly evaluate and debug 8-bit microcomputer-based systems in the lab, on the production line, or in the field. Connection to the user's system is through a personality probe that is plugged into the microprocessor socket. Each personality probe is unique to each microprocessor type. The instrument features many different operating and control modes which allow the operator to carry out a number of functional checks on the microcomputer System Under Test (SUT).

The unit has been specificially designed to ease the task of microcomputer system check-out for the lab, production line, and field technician. It also provides the more powerful analytical capabilities necessary to troubleshoot difficult problems by the more experienced, sophisticated user. Preprogrammed test routines resident in front panel PROMs, dedicated high level command keys, visual prompting, and simplified data entry sequences all ease the check-out of microcomputer hardware. For more rigorous diagnostic tasks, the unit provides a 32-bit maskable hardware breakpoint with optional course of action after a breakpoint match, a 256 × 32-bit trace memory and a 128 × 8 overlay RAM that allows real-time entry of test routines via the μScope 820 Microprocessor System Console keyboard.

CPU CONTROL

The instrument provides complete control over the operation of the microprocessor in the System Under Test (SUT). The user CPU can be forced to HALT, SINGLE STEP, RESET, RUN REAL TIME, or RUN WITH DISPLAY. All of the above CPU commands can be issued without impacting other operational parameters or diagnostic sequences that have been set up.

RESET/SELF-TEST

The RESET and SELF-TEST features of the unit allow the operator to either initialize the instrument to a known state or quickly verify that the instrument is operating correctly. When the console is RESET, the breakpoint and overlay memory are disabled, the display registers are cleared and the specific examine modes are aborted.

When the operator initiates the SELF-TEST of the unit, a sequence of operations take place which serve to confirm proper operation of a majority of the instrument.

BREAKPOINT CONTROL

The hardware breakpoint of the instrument allows the operator to alter the normal program flow of the SUT. Breakpoint logic is implemented in hardware, thereby eliminating any throughput degradation of the SUT. All 32 bits of the breakpoint condition word are maskable in order to allow the breakpoint condition to be as specific or as general as may be desired.

The occurrence of a breakpoint match can cause an unconditional halt, incrementing of the pass counter, calling of a subroutine, or the recording of a single cycle of trace data. All of these options are selectable via the EXAM ACTION key prior to enabling the breakpoint.

TRACE MEMORY

The console has a full 32-bit word trace memory that records 256 cycles of SUT operation without causing any delays. The trace memory provides information about CPU operation just prior to a CPU halt or just prior to the initiation of a panel freeze via the trace DISPLAY key.

The operator can alternatively elect to have data recorded on all SUT microprocessor cycles or only when program execution of the SUT microprocessor generates a breakpoint match. Once the data is recorded, sequential examination of the data can be accomplished simply by depressing the EXAM NEXT or EXAM LAST keys.

OVERLAY MEMORY

A unique feature of the unit is the ability to map its memory onto the SUT memory space. Using the overlay memory allows the operator to insert patch, exercise, or diagnostic subroutines at any location or point of execution in the SUT program. The subroutine can either be entered via the front panel hexadecimal keypad or via the front panel's ROM/PROM socket.

By using the unit's overlay memory, the operator can quickly set up the SUT to execute special maintenance or troubleshooting programs that permit rapid evaluation of system operation.

ADDRESS DISPLAY/SELECT

A dedicated, 4-digit hexadecimal address display allows the following address information to be displayed:

- The address of any memory location.
- The I/O port number of any I/O port.
- The address of any overlay memory location.
- The address of the overlay memory origin assignment.
- The address at which the breakpoint is to occur.
- The address portion of the breakpoint mask.
- The address of the given trace record element.

An additional feature of the address display/select logic is that once the operator has initiated a given memory, trace, or I/O examination, it is possible to continue the examination in a sequential fashion either in an ascending or descending address value.
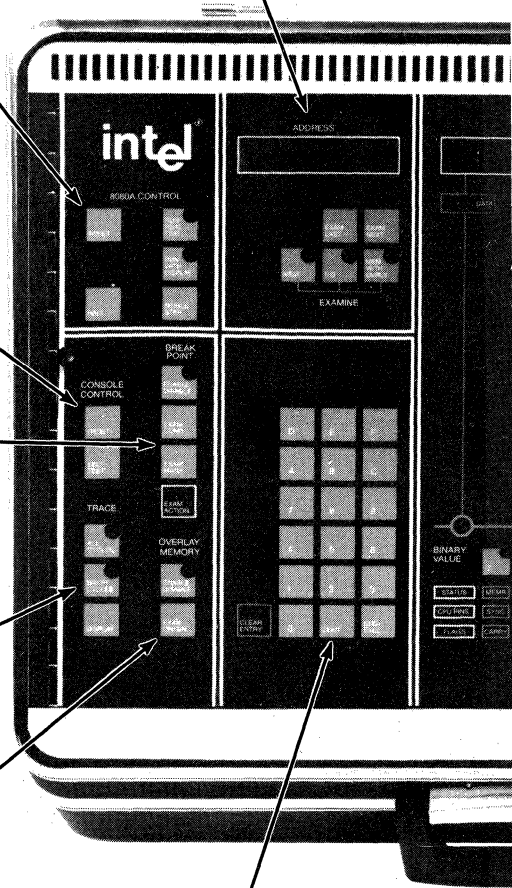
ADDRESS, DATA, AND CONTROL ENTRY

The address, data, and control variable entry into the instrument is accomplished via the conveniently located hexadecimal keypad.

For selection of the information to be displayed or modified the operator enters the hexadecimal value of the desired address, I/O port number or label assigned to each of the registers. Once this entry is made, the operator can then elect to either CONTINUE data entry if modification is desired or press the END/EXECUTE key if examination only is desired. For all data entry sequences that potentially require multiple value entry, the μScope^{TM} 820 Microprocessor System Console provides operator prompting to indicate the specific information expected.

VALUE DISPLAY/SELECT

The value displays provide clear and easy to use information. Together with the address display, they provide simultaneous readout of trace vectors, breakpoint conditions and breakpoint mask values, memory contents and I/O port contents. In addition, the display allows readout of all single and double byte register values, the state of CPU pins and flags, information regarding the course of action following the occurrence of a breakpoint, as well as information regarding the breakpoint pass count.

The information displayed by the 4-digit hexadecimal value readouts is selected via the hexadecimal keypad in conjunction with any of the instrument's 11 dedicated examine keys. Further, the information is either displayed statically or is continually updated 10 times/sec if the unit is in the run with display mode.

PROM/ROM SOCKET

A front panel socket is provided for mounting 2K PROMs or ROMs that serve as storage for preprogrammed test subroutines. The actual useable program space of the PROM/ROM is 1920 bytes. The remaining 128 bytes of storage, shadowed by RAM, are used by the unit to identify up to 16 separate subroutines in the PROM/ROM and to define the specific instrument states and conditions under which the subroutine will be called. Each of the separate subroutines is uniquely enabled by the SUBR SELECT key and the hex keypad.

POWER SUPPLY

The system console is complete with its own fully regulated DC power supply that provides all the DC power required by the unit itself, as well as that which is required by the associated microprocessor probe. The supply is completely self-contained, including its own AC on/off switch, line fuse, line filter and power cord. An additional feature of the power supply is that it has been designed to permit line voltage selection in the field to facilitate operation with a wide range of AC line voltages and frequencies.

BREAKPOINT ACTION

Following the occurrence of a breakpoint match, the operator has the flexibility to execute a number of different diagnostic operations. The selection of these alternate courses of action is accomplished by pushing the EXAM ACTION key and then entering the assigned value of the specific action desired via the hex keypad. Further keypad entries specify the parametric value of the action selected such as the number of breakpoint pass counts or the start address of a subroutine call following a breakpoint.

PROBE CONNECTION

The instrument is intended to work with many of the microprocessors that are available today. This is accomplished by standardized interface logic which transmits and receives various address, data, and control signals between the system console and the circuitry of the particular probe. The interconnect circuitry between the instrument and probe has been designed to drive a 6-foot cable that permits convenient positioning of the panel and the SUT.

In addition, a board edge connector has been provided for a personality ROM that provides front panel definition and interpretation of specific control signals for different types of microprocessors. This personality ROM is supplied with each probe kit.

FRONT PANEL

The front panel of the μScope™ 820 Microprocessor System Console has been designed to be rugged and durable as well as easy to use and understand. A plastic overlay that employs membrane switch contacts provides long lasting durability as well as protection from accidental spills. Audio and tactile feedback for the membrane switches is provided for operator convenience.

Ease of use of the front panel has been further enhanced by human engineering with functional grouping of switches as well as LEDs that prompt the operator during data entry sequences. Graphics have also been added to reinforce the functional switch groupings as well as data entry procedures.

BINARY DATA DISPLAY/MODIFICATION

All 8-bit values can be displayed in binary format on the instrument. The binary display operates in parallel with the hexadecimal display and it is provided for those instances where operator recognition is enhanced by binary presentation. The selection procedure for the binary data display is identical to that for the hexadecimal value display. Once the selection has been made, the operator can alter the value by means of further hex keypad entries or by changing the binary state of any of the data bits via the 8 binary data switches.
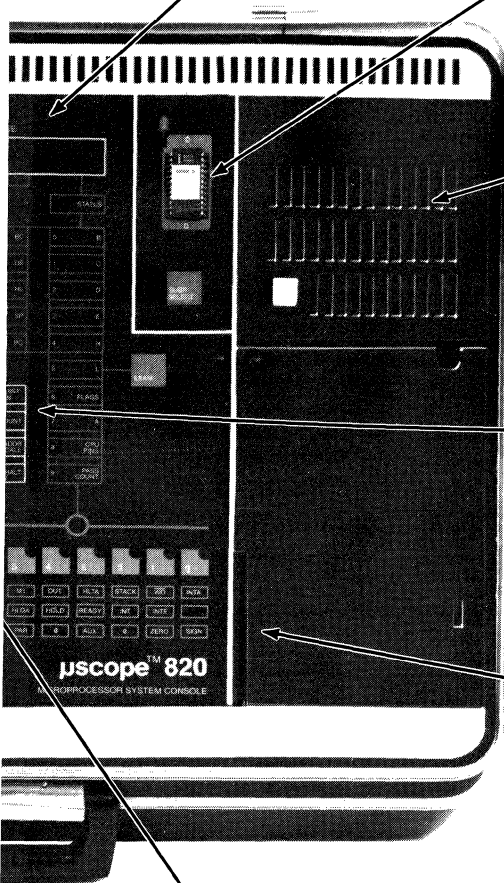
CHARACTERISTICS

COMMANDS

Reset	Examine/Modify Memory
Self Test	Examine/Modify I/O
CPU Reset	Examine/Modify Overlay Memory
Run Real Time	Examine/Modify Next Location
Run with Display	Examine/Modify Last Location
Halt	Examine/Modify Breakpoint
Single Step	Condition
Enable/Disable Breakpoint	Examine/Modify Breakpoint
Enable/Disable Overlay	Mask
Enable Trace All Cycles	Examine/Modify Breakpoint
Enable Trace at Breakpoint	Action
Examine/Modify Value	Examine/Modify Overlay Origin
— Single Registers	Display Trace Data
— Double Registers	Clear Entry
— CPU States	Continue
— Breakpoint Pass	End/Execute
Count	Subroutine Select

CPU CONTROLS

User-selectable commands permit one of four possible CPU operating modes:

1. *Run Real Time* — User's CPU runs at full speed set by user clock. No wait states or cycle stealing are required.

2. *Run with Display* — User's CPU runs at full speed, except that 10 times/sec the instrument halts user's CPU temporarily to acquire display data. Worse case throughput is 95% of real time operation.

3. *Halt* — User CPU halted at next opcode fetch. DMA activity is permitted during HALT.

4. *Single Step* — User CPU executes one instruction then halts.

BREAKPOINT

The breakpoint condition is set by a 32-bit word (16-bit address, 8-bit data, 8-bit status). The breakpoint mask is also set by a 32-bit word which is bit-selectable. There are three courses of action following a breakpoint match:

1. Halt on first opcode fetch following breakpoint match.

2. Halt on first opcode fetch following Nth breakpoint match $1 \leqslant N \leqslant 256$.

3. Execute subroutine beginning at first opcode fetch following breakpoint match.

All breakpoint actions following a match is controlled by the breakpoint enable/disable switch except for trace recording and the sync trigger output. The sync output is a positive true TTL output that occurs whenever a breakpoint match occurs.

    Pulse Width = 50 nsec typ
    Output High = 2.5V min, −1.2 mA
    Output Low = 0.5V max, 24.0 mA

TRACE

The trace memory is a 256-word memory with each word consisting of 16 address bits, 8 data bits and 8 status bits. The memory is a circular buffer which records the last 256 cycles (words) prior to a user CPU halt or DISPLAY TRACE command. Trace data can be recorded on all CPU cycles or only when breakpoint matches occur (independent of breakpoint enable/disable status). In addition, the operator can initiate a panel freeze which temporarily stops all trace data recording, and allows display of previously recorded data without halting the user CPU.

DATA ENTRY

All single and double byte items can be entered via the front panel hexadecimal keypad. In addition, all single byte items can be optionally entered via eight binary input keys.

MEMORY OVERLAY

The μScope^TM 820 Microprocessor System Console allows memory read/writes of the user CPU in any assigned 1K or 2K block to be made to the instrument's overlay memory. For 1K block assignments, the first 128 bytes reside in the instrument's RAM memory while the remaining 896 bytes reside in the interchangeable front panel ROM/EPROM (either Intel's 2716 EPROM or Intel's 2316E ROM). For 2K block assignments, again the first 128 bytes are from RAM and the remaining 1920 bytes are from the front panel 2716/-2316E.

DATA DISPLAY

Eight hexadecimal 0.5 in. LEDs are provided for the simultaneous display of 4 bytes of information. The displays are physically separated into two groups. The first group displays 2 bytes of address, while the second group displays CPU data, status, single and double byte register values, or single and double byte breakpoint values. In addition, eight binary displays are used to provide quick recognition of single byte binary data patterns.

SELF TEST

The necessary hardware and software has been incorporated into the instrument to facilitate the self-checking of the majority of its operations. Included in these self tests are:

- Bit tests of all breakpoint condition and mask latches.
- Bit tests of all RAM.
- Verifies checksum on all operating system ROMs.
- Clears trace memory and performs bit test on trace RAM.
- Checks miscellaneous I/O ports and peripheral components.
- Lights all front panel displays for user verification.

CONNECTION

Four external connections to the μScope 820 Microprocessor System Console are provided:

- 50-pin board edge connector for the microprocessor probe cable.
- 20-pin board edge connector for the probe personality PROM.
- 24-pin zero force insertion sockets for overlay EPROM/ROM.
- One recessed pin for breakpoint sync output.

PHYSICAL CHARACTERISTICS

Width:	479 mm	(18-7/8 in.)
Length:	394 mm	(15-1/2 in.)
Height (top closed):	168 mm	(6-5/8 in.)
Height (top removed):	117 mm	(4-5/8 in.)
Weight:	9.1 kg	(20 lb)

ELECTRICAL REQUIREMENTS

Voltage: 100, 120, 220, 240 − 10% +5%, 110VA max
Frequency: 48—63 Hz

ENVIRONMENTAL CONDITIONS

Operating Temperature: 0°C to 55°C (32°F to 130°F)
Storage Temperature: −40°C to 75°C (−40°F to 167°F)
Humidity: 95% RH, 15°C to 40°C (59°F to 104°F)
                non condensing

ACCESSORIES SUPPLIED

One 2.3m (7.5 ft) power cord
One Operator's Manual
One Hardware Reference Manual

ORDERING INFORMATION

Part Number	Description
USC-820	Microprocessor System Console

μSCOPE™ PROBE 8080A

Provides interconnection for 8080A Microprocessor-based Systems to the μScope™ 820 Microprocessor System Console

Comes complete with cable, buffer box, personality ROM, and μScope 820 system console overlay

Has user system interconnect cable with integral ground plane for low noise operation

Includes a 6-foot cable for convenient positioning of μScope 820 console

Operates over a broad range of environmental conditions

Provides complete control over the system under test, yet causes minimal interference with system under test operation

Fits securely in the console carrying case during transit

Provides complete protection for plug pins during transit

The probe 8080A provides the μScope 820 console with the ability to interact with 8080A Microcomputer-based Systems. The purpose of the probe is to interface the μScope 820 console to the CPU of the System Under Test (SUT). All of the interface signals and the associated circuitry have been designed to be effectively transparent to the SUT. CPU data, address, and clock lines are sensed by the probe 8080A, with only the CPU control lines being switched. In addition, all SUT loading and timing degradations have been minimized by specially designed buffer circuitry.

The mechanical design of the probe is compact, rugged, and allows proper operation of the probe and the console over the full ambient range specified. The buffer circuitry and the ground plane design of the interconnect cable provide low noise electrical signals while allowing the SUT to be 6 feet from the system console.
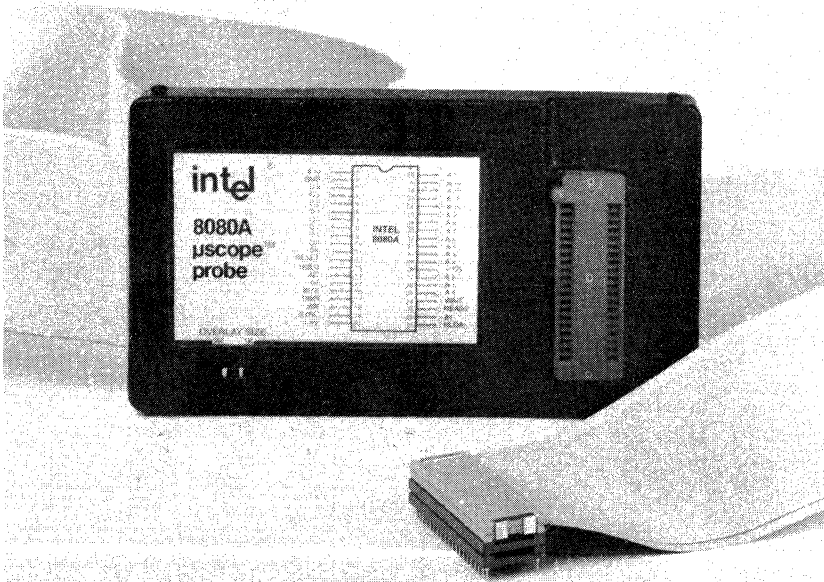
GENERAL

μSCOPE 820 CONSOLE INTERCONNECT

The probe interconnection to the μScope 820 console is accomplished via a 1.8 m (6 ft) flat cable. 50-pin mating connectors plug into a board edge connector in the power cord compartment of the instrument and into a flat cable connector on the buffer box.

SYSTEM UNDER TEST (SUT) INTERCONNECT

Interconnection from the buffer box to the SUT is accomplished with a 305 mm (12 in.) flat cable, complete with an integral ground plane, which is terminated with a low profile 40-pin DIP connector. The DIP connector is inserted into the SUT 8080A socket and the 8080A itself is plugged into the 40-pin socket provided on the probe buffer box.

μSCOPE 820 CONSOLE CONFIGURATION

Several features of the console are directly determined by the probe being used with it. The instrument features that are determined by the 8080A interface probe are:

- Single Registers: A, B, C, D, E, H, L
- Double Registers: BC, DE, HL, PC, SP
- CPU States: Flags, CPU pins (SYNC, RESET, HLDA, HOLD, READY, INT, INTE)
- Trace/Breakpoint Word Size: 32 bits with 16 bits of address, 8 bits of data and 8 bits of CPU status.

ELECTRICAL SPECIFICATIONS

All DC specifications are in addition to user system parameters. All capacitance values include cables and connectors.

Non-Intercepted Signals

$\phi 1, \phi 2$	$\pm 10\ \mu A$ max; 55 pF typical
$A_{15}-A_0, D_7-D_0$	-0.25 mA max @ 0.45V; 10 μA max @ 5.25V; 45 pF typical
+12V Supply	15 μA max
WAIT	35 pF typical (capacitive loading only)

Intercepted Signals

Outputs to user system:

SYNC	20 mA min @ 0.5V; -1 mA min @ 2.7V; 40 pF typical
HOLDA, INTE, DBIN, and $\overline{WR}$	4 mA min @ 0.4V; -0.2 mA min @ 2.7V; 40 pF typical

Inputs from user system:

INT, READY, RESET	40 μA max @ 2.7V; -0.72 mA max @ 0.4V; 50 pF typical
HOLD	60 μA max @ 2.7V; -1.08 mA max @ 0.4V; 50 pF typical

CONNECTIONS

Three external connections to the probe are provided:

- 50-pin flat cable connector on buffer box
- 40-pin zero insertion socket for the 8080A
- 40-pin low profile replaceable IC DIP connector for connection to SUT

CHARACTERISTICS

PHYSICAL CHARACTERISTICS

Probe Buffer Box:

Height:	19 mm	(3/4 in.)
Length:	184 mm	(7-1/4 in.)
Width:	95 mm	(3-3/4 in.)

User System Interconnect Cable:

Width:	57 mm	(2-1/4 in.)
Length:	381 mm	(15 in.) flat cable

μScope 820 Console Personality ROM PC Card:

Height:	19 mm	(3/4 in.)
Width:	57 mm	(2-1/4 in.)
Length:	86 mm	(3-1/4 in.)

POWER REQUIREMENTS

Power supplied by μScope™ 820 Microprocessor System Console.

ENVIRONMENTAL CONDITIONS

Operating Temperature:	0° to 55°C (32° to 130°F)
Storage Temperature:	-40°C to 75°C (-40° to 167°F)
Humidity:	95% RH, 15° to 40°C (59° to 104°F) noncondensing

ACCESSORIES SUPPLIED

One μScope 820 System Console Overlay
One Personality ROM
One Hardware Reference Manual

ORDERING INFORMATION

Part Number	Description
PRB-80	8080A Interface Probe

Chapter 8
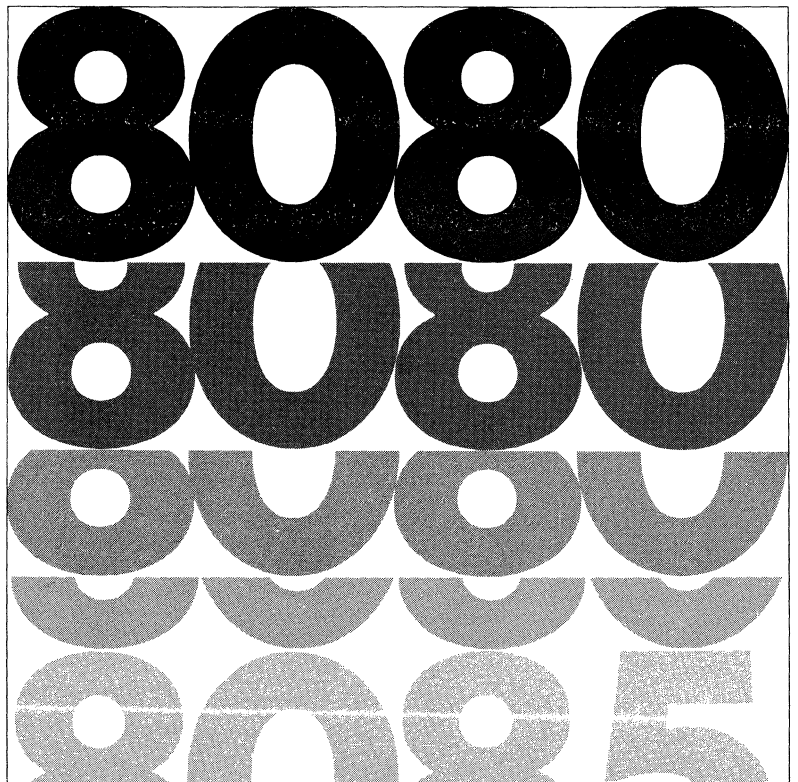
GENERAL INFORMATION

Semiconductor components are identified as follows:

Example:

| M | C | 5 | 1 | 0 | 1 | | L | — | 4 |

Four or five characters per device type

Up to three character modifier for power, speed, processing, etc.

Package Type
B — Hermetic Package, Type B
C — Hermetic Package, Type C
D — Hermetic Package, Type D
M — Metal Can Package
P — Plastic Package
X — Unpackaged Device
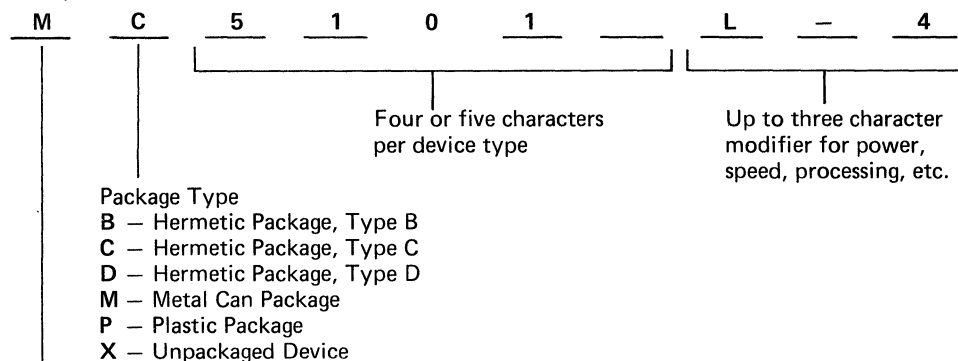
M — Indicates Military Operating Temperature Range

Examples:

P5101L CMOS 256 X 4 RAM, low power selection, plastic package, commercial temperature range.

C8080A2 8080A Microprocessor with 1.5 μs cycle time, hermetic package Type C, commercial temperature range.

MD3604/C 512 X 8 PROM, hermetic package Type D, military temperature range, MIL-STD-883 Level C processing.*

MC8080A/B 8080A Microprocessor, hermetic package Type C, military temperature range, MIL-STD-883 Level B processing.*

Kits, boards and systems may be ordered using the part number designations in this catalog.

The latest Intel OEM price book should be consulted for availability of various options. These may be obtained from your local Intel representative or by writing directly to Intel Corporation, 3065 Bowers Avenue, Santa Clara, CAlifornia 95051.

On military temperature devices, B suffix indicates MIL-STD-883 Level B processing. Suffix C indicates MIL-STD-883 Level C processing. "S" number suffixes must be specified when entering any order for military temperature devices. All orders requesting source inspection will be rejected by Intel.

PLASTIC DUAL IN-LINE PACKAGE TYPE P

16-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

.840 (21.336)
.820 (20.826)

PIN 1

.260 (6.604)
.240 (6.096)

.200 (5.080) MAX.

.140 (3.556)
.130 (3.302)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.015 MIN. (0.381)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 TYP (0.813)

.023 (0.584)
.014 (0.356)

.325 MAX. (8.255)

.015 (0.381)
.008 (0.203)

0°
15°

.400
.330

(10.160)
(8.382)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

.910 (23.114)
.890 (22.098)

PIN 1

.260 (6.604)
.240 (6.096)

.200 (5.080) MAX.

.140 (3.556)
.130 (3.302)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.015 MIN. (0.381)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 TYP (0.813)

.023 (0.584)
.014 (0.356)

.325 MAX. (8.255)

.015 (0.381)
.008 (0.203)

0°
15°

.400
.330

(10.160)
(8.382)

22-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

1.110 (28.194)
1.090 (27.686)

PIN 1

.360 (9.144)
.340 (8.636)

.200 (5.080) MAX.

.155 (3.937)
.145 (3.683)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.015 MIN. (0.381)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 TYP (0.813)

.023 (0.584)
.014 (0.356)

.425 MAX. (10.795)

.015 (0.381)
.008 (0.203)

0°
15°

.510
.450

(12.954)
(11.430)

PLASTIC DUAL IN-LINE PACKAGE TYPE P

24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

1.250 (31.750)
1.230 (31.442)

PIN 1

.550 (13.970)
.530 (13.462)

.200 (5.080) MAX.

.160 (4.064)
.150 (3.810)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 TYP (0.813)

.023 (0.584)
.014 (0.356)

.015 MIN. (0.381)

.015 (0.381)
.008 (0.203)

.625 MAX. (15.875)

0°
15°

.700
.630
(17.780)
(16.002)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

1.460 (37.084)
1.440 (36.576)

PIN 1

.550 (13.970)
.530 (13.462)

.200 (5.080) MAX.

.160 (4.064)
.150 (3.810)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 TYP (0.813)

.023 (0.584)
.014 (0.356)

.015 MIN. (0.381)

.015 (0.381)
.008 (0.203)

.625 MAX. (15.875)

0°
15°

.700
.630
(17.780)
(16.002)

40-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

2.060 (52.324)
2.040 (51.816)

PIN 1

.550 (13.970)
.530 (13.462)

.200 (5.080) MAX.

.175 (4.445)
.165 (4.191)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 TYP (0.813)

.023 (0.584)
.014 (0.356)

.015 MIN. (0.381)

.015 (0.381)
.008 (0.203)

.625 MAX. (15.875)

0°
15°

.700
.630
(17.780)
(16.002)

CERAMIC DUAL IN-LINE PACKAGE TYPE D

16-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

.780 (19.812)
.740 (18.796)

PIN 1

.300 (7.620)
.260 (6.604)

.200 (5.080) MAX.

.160 (4.064)
.145 (3.683)

.322 MAX. (8.178)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 (0.813) TYP.

.015 MIN. (0.381)

.023 (0.584)
.014 (0.356)

.015 (0.381)
.008 (0.203)

.400
.330

0°
15°

(10.160)
(8.382)

18-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

.905 (22.987)
.875 (22.225)

PIN 1

.300 (7.620)
.260 (6.604)

.200 (5.080) MAX.

.160 (4.064)
.145 (3.683)

.322 MAX. (8.178)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 (0.813) TYP

.015 MIN. (0.381)

.023 (0.584)
.014 (0.356)

.015 (0.381)
.008 (0.203)

.400
.330

0°
15°

(10.160)
(8.382)

22-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

1.085 (27.559)
1.055 (26.797)

PIN 1

.400 (10.16)
.350 (8.89)

.200 (5.080) MAX.

.180 (4.572)
.140 (3.556)

.425 MAX. (10.795)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 (0.813) TYP

.015 MIN. (0.381)

.023 (0.584)
.014 (0.356)

.015 (0.381)
.008 (0.203)

.510
.440

0°
15°

(12.954)
(11.176)

CERAMIC DUAL IN-LINE PACKAGE TYPE D

24-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

1.270 (32.258)
1.230 (31.242)

PIN 1

.530 (13.462)
.510 (12.954)

.220 (5.588) MAX.

.175 (4.445)
.150 (3.810)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 TYP (0.813)

.015 MIN. (0.381)

.023 (0.584)
.014 (0.356)

.625 MAX. (15.875)

.015 (0.381)
.008 (0.203)

0°
15°

.700
.630

(17.780)
(16.002)

28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

1.470 (37.338)
1.430 (36.322)

PIN 1

.530 (13.462)
.510 (12.954)

.220 (5.588) MAX.

.175 (4.445)
.150 (3.810)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.065 (1.651)
.040 (1.016)

.110 (2.794)
.090 (2.286)

.032 TYP (0.813)

.015 MIN. (0.381)

.023 (0.584)
.014 (0.356)

.625 MAX. (15.875)

.015 (.381)
.008 (.203)

0°
15°

.700
.630

(17.780)
(16.002)

40-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

2.070 (52.578)
2.030 (51.562)

PIN 1

.530 (13.462)
.510 (12.954)

.220 (5.588) MAX.

.175 (4.445)
.150 (3.810)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 TYP (0.813)

.015 MIN. (0.381)

.023 (0.584)
.014 (0.356)

.625 MAX. (15.875)

.015 (0.381)
.008 (0.203)
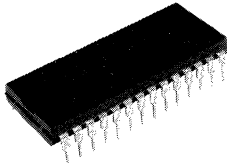
0°
15°

.700
.630

(17.780)
(16.002)

CERAMIC DUAL IN-LINE PACKAGE TYPE C

16-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE C

.820 (20.820)
.780 (19.812)

PIN 1 MARK
PIN 1

.310 (7.874)
.270 (6.858)

.200 (5.080) MAX.
.096 (2.413)
.070 (1.778)

.130 (3.302)
.080 (2.032)

SEATING PLANE

.015 MIN. (0.381)
.015 (0.381)
.008 (0.203)

0°
10°

.100 (2.540)
.165 (4.191)

.065 (1.65)
.040 (1.016)

.023 (0.584)
.014 (0.356)

.380
.280

.110 (2.794)
.090 (2.286)

.032 TYP. (0.813)

(9.652)
(7.112)

18-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE C

.920 (20.820)
.880 (19.812)

PIN 1 MARK
PIN 1

.310 (7.874)
.270 (6.858)

.200 (5.080) MAX.
.095 (2.413)
.070 (1.778)

.130 (3.302)
.080 (2.032)

SEATING PLANE

.015 MIN (0.381)
.015 (0.381)
.008 (0.203)

0°
10°

.100 (2.540)
.165 (4.191)

.065 (1.651)
.040 (1.016)

.023 (0.584)
.014 (0.356)

.380
.280

.110 (2.794)
.090 (2.286)

.032 TYP. (0.813)

(9.652)
(7.112)

22-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE C

1.095 (27.813)
1.055 (26.797)

PIN 1 MARK
PIN 1

.400 (10.160)
.380 (9.652)

.200 (5.080) MAX.
.100 (2.540)
.070 (1.774)

.130 (3.302)
.080 (2.032)

SEATING PLANE

.015 MIN. (0.381)
.015 (0.381)
.008 (0.203)

0°
10°

.100 (2.540)
.165 (4.191)

.065 (1.651)
.040 (1.016)

.023 (0.584)
.014 (0.356)

.480
.390

.110 (2.794)
.090 (2.286)

.032 TYP. (0.813)

(12.192)
(9.906)

CERAMIC DUAL IN-LINE PACKAGE TYPE C

24-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE C
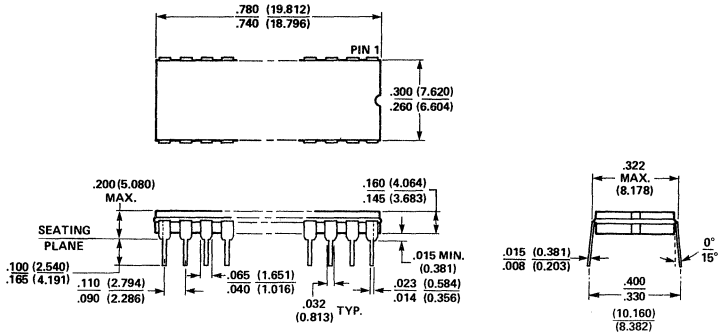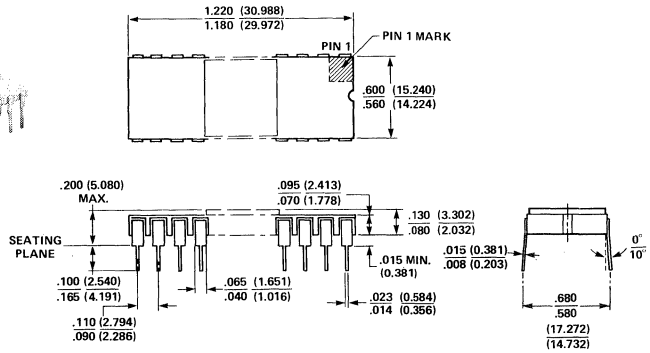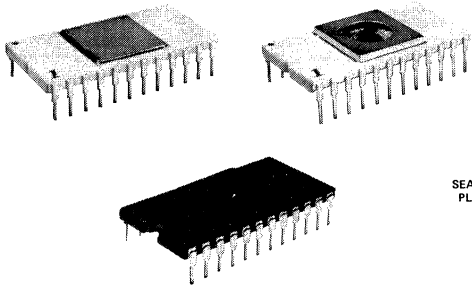
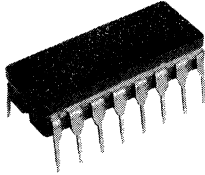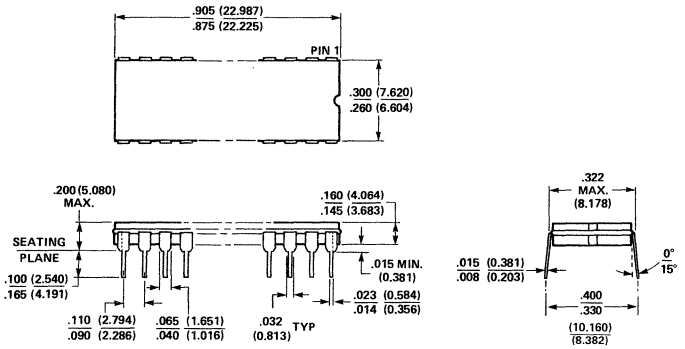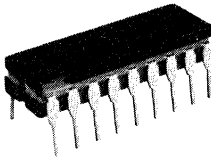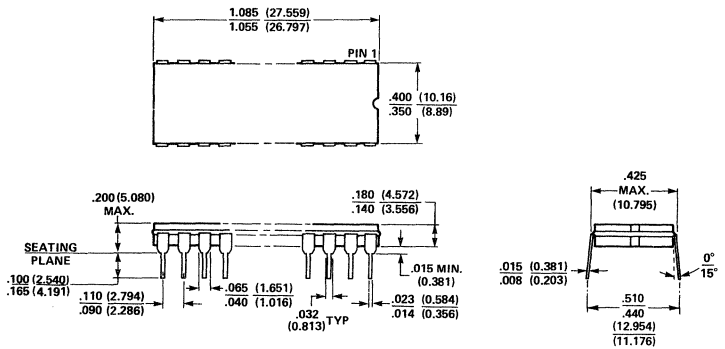## 28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE C
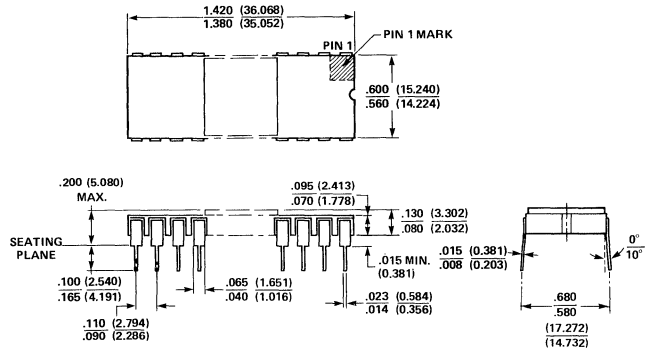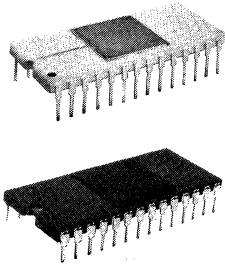
40-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE C
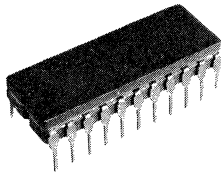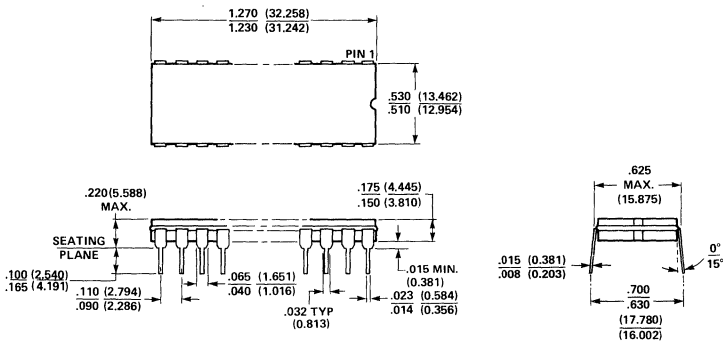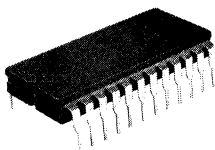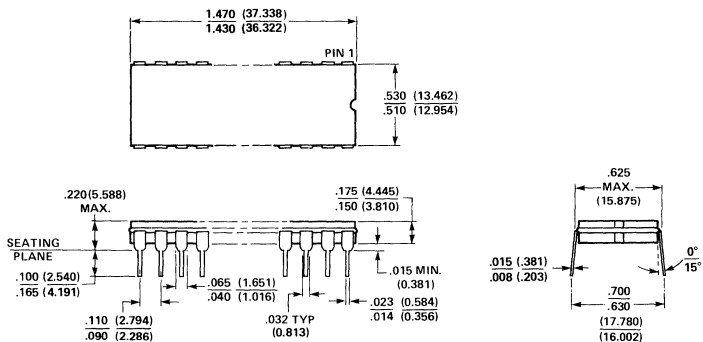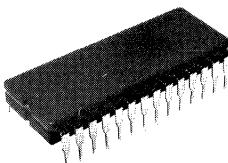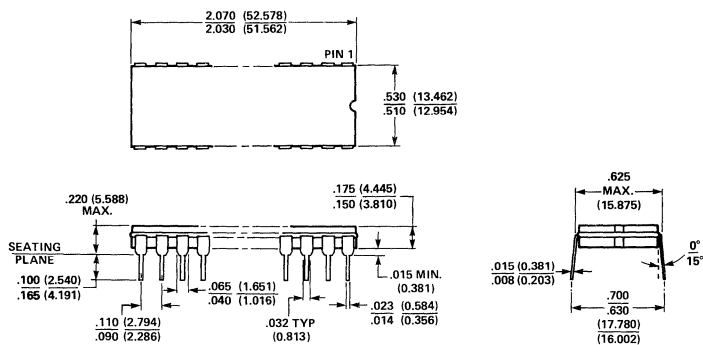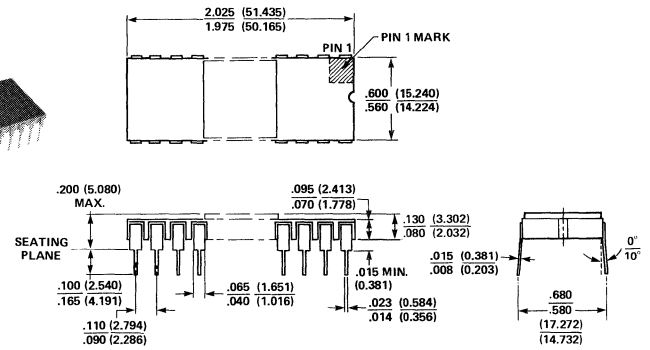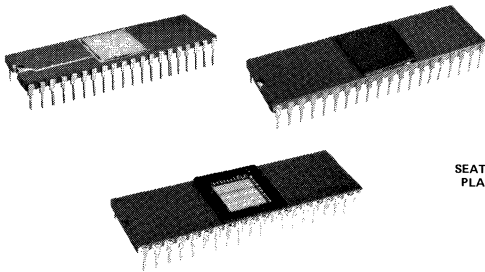
CERAMIC DUAL IN-LINE PACKAGE TYPE B

22-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE B

1.085 (27.559)
1.065 (27.051)

PIN 1

.385 (9.779)
.370 (9.398)

.200 (5.080) MAX.

.140 (3.556)
.120 (3.048)

.175 (4.445)
.155 (3.937)

SEATING PLANE

.100 (2.540)
.165 (4.119)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 TYP.
(0.831)

.015 MIN.
(0.381)

.023 (0.584)
.014 (0.356)

.425 MAX.
(10.795)

(0.381) .015
(0.203) .008

0°
15°

.510
.450
(12.454)
(11.430)

24-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE B

1.270 (32.258)
1.230 (31.242)

PIN 1

.530 (13.462)
.510 (12.954)

.220 (5.558) MAX.

.150 (3.810)
.110 (2.794)

.190 (4.826)
.125 (3.175)

SEATING PLANE

.100 (2.540)
.165 (4.191)

.110 (2.794)
.090 (2.286)

.065 (1.651)
.040 (1.016)

.032 TYP
(0.813)

.015 MIN.
(0.381)

.023 (0.584)
.014 (0.356)

.625 MAX.
(15.875)

.015 (0.381)
.008 (0.203)

0°
15°

.700
.630
(17.780)
(16.002)

INTEL MILITARY PRODUCTS
IC 38510 PROGRAM

Intel offers selected products in full conformance with requirements for military components. Effort is underway by agencies of the Department of Defense with full Intel cooperation to establish "JAN" standards for several of our products. Intel has led these standards by emulating the anticipated "JAN" processing and lot acceptance requirements with the Intel in-house IC 38510 Program. Intel Specifications are available which document general and detailed requirements for each of the military products. Detail specifications are organized by generic family and provide all information necessary for non-standard parts submissions in accordance with MIL-STD-749, Step I, Step II, and Step III. These documents are available from your local Intel Sales Office or authorized Intel Distributor.

Three levels of product assurance are offered: Level B, Level C, and Military Temperature Only.

The Military Temperature level products have guaranteed operating characteristics over the specified temperature range and have undergone Intel's rigid product assurance requirements.

Level C and Level B products are in conformance with MIL-STD-883, Method 5004 requirements, and in addition, have a specified maximum rebond criteria (10%) and a specified burn-in PDA (10%), all documented in the detail specifications, consistent with 38510 requirements. Lot conformance tests are performed in accordance with MIL-STD-883A, Method 5005.

Available now.	Qualification in progress. Check with local Intel Sales Office or Distributor for availability.
MC8080A	MD8238
MB8101A	MD8253
MD8102A-4	MD8259
MD8111A	MD8316E
MD8212	MC8748
MD8214	MC8755
MD8216	
MD8224	
MD8226	
MD8228	
MD8251	
MD8255	
MD8316A	
MC8702A	
MC8708	

LEVEL B AND C
MILITARY PRODUCTS MANUFACTURING FLOW

Wafers

- Incoming QC Raw Material Inspection
- Incoming QC Silicon Wafer Inspection
- Wafer Fabrication

  Optical Inspections
  Contamination Checks
  Particle Counts
  Critical Dimensions

- Optical Inspection
- Wafer Sort

  QA Wafer Inspection
  and Die Count

- Scribe and Break
- DI Water Die Clean
- Post Break Chip Inspection —
  MIL-STD-883A, Method 2010
  Condition B

  QA Post Break Chip
  Inspection, MIL-STD-
  883A, Method 2010
  Condition B

Lead Frame
and Base

- Lead Frame Attach
- Visual Inspection for Alignment
  and Glass Flow
- Die Attach: Jumper Chip Attach

  Visual Inspection of
  Die Attached Units.
  Monitor of Die Attach
  Machines.

- Aluminum Ultrasonic Wire Bond

  Bond Pull Acceptance to
  Monitor Bond Strengths per
  MIL-STD-883A, Method 2011

- Die Attach and Bond Inspection
  per MIL-STD-883A, Method 2010
  Condition B

  QA Die Attach and Bond
  Inspection per MIL-STD-883A,
  Method 2010 Condition B
  AQL = 1%

Cap

- Cap Seal

  QA Seal Monitor. Cap
  Alignment and Glass Flow

  Stabilization Bake,
  150°C, 24 Hours

- Temperature Cycle, per MIL-STD-883A,
  Method 1010 Condition C, 10 cycles
- Centrifuge, per MIL-STD-883A, Method
  2001, Condition E, Y_1 Axis, 30KG
- Hermeticity Testing: Fine Leak — Helium
  or Kr 85 to 5×10^{-8} cc/sec.

  Gross Leak — Fluorocarbon,
  Condition C_2, 100% MIL-STD-
  883A, Method 1014

- Tin Plate

  QA Tin Thickness Monitor
  Thickness Spec 200–700
  Microinches

- Trim Tie Bar

  Hermeticity Lot Acceptance
  AQL = 1%

Final Visual — Package, Seal Date Code, Country of Origin, and Lead Inspection

Final Visual Lot Acceptance, AQL = 1%

Plant Outgoing Inspection*

Mark, Tube Load and Opens and Shorts Testing

Ship to USA

Stabilization Bake — 150°C, 24 Hours

Incoming Inspection of Foreign Assembly Plant Shipments**. LTPD Dependent Upon Test

25°C Interim Electrical Tests, Level B Products Only per MIL-STD-883A

Burn-In (Level B Products Only) per MIL-STD-883A, Method 1015, Condition C or F

100% Electrical Tests at 25°C (AC, DC, Function)

100% Electrical Test at -55°C (AC, DC, Function) Level B Product Only

100% Electrical Tests at +125°C (AC, DC, Function) Level B Product Only

Mark Customer Number

Final QA Visual and Electrical Tests at 25°C, -55°C, and 125°C LTPD = 5 (AC, DC and Function) (-55°C and +125°C Testing On Levels B and C Product Only)

Group B Tests Performed per MIL-STD-883A, Method 5005, for Lot Conformance. (Levels B and C Only)

Group C and D Tests Performed per MIL-STD-883A, Method 5005, for Lot Conformance. (Levels B and C Only)

Ship to Customer

PIECE PARTS ⬡	◯ MANUFACTURING OPERATION	△ QA MONITOR
	⊘ MANUFACTURING INSPECTION OR TEST	☐ QA LOT ACCEPTANCE

*Outgoing Acceptance (Plant Clearance) Inspections:

Test	LTPD	ACC
1. Hermeticity	5	2
2. Centrifuge	5	2
3. X-Ray	7	1
4. Lead Fatigue	20	0
5. Acoustic (Loose Particles) AQL = .04%		

**Incoming Inspection Testing:

Test	LTPD	ACC
1. X-Ray, Die Attach and Seal Quality	7	1
2. External Visual	7	1
3. Opens and Shorts	7	1
4. Hermeticity	7	1
5. Lead Fatigue	20	0
6. Internal Visual	10	0
7. Bond Pull	7	1
8. Acoustic (1000 Particles) AQL = .04%		

INSTRUCTION SET

Summary of Processor Instructions

Mnemonic	Description	D7	D6	D5	D4	D3	D2	D1	D0	Clock[2] Cycles
MOV r1,r2	Move register to register	0	1	D	D	D	S	S	S	5
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4

NOTES: 1. DDD or SSS — 000 B — 001 C — 010 D — 011 E — 100 H — 101 L — 110 Memory — 111 A.

2. Two possible cycle times, (5/11) indicate instruction cycles dependent on condition flags.

INSTRUCTION SET

Summary of Processor Instructions
By Alphabetical Order

Mnemonic	Description	D7	D6	D5	D4	D3	D2	D1	D0	Clock[2] Cycles
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	0	1	7
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
ANA r	And register with A	1	0	1	0	0	S	S	S	4
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CMA	Compliment A	0	0	1	0	1	1	1	1	4
CMC	Compliment carry	0	0	1	1	1	1	1	1	4
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
HLT	Halt	0	1	1	1	0	1	1	0	7
IN	Input	1	1	0	1	1	0	1	1	10
INR M	Increment memory	0	0	1	1	0	1	0	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
LDA	Load A direct	0	0	1	1	1	0	1	0	13
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MOV M, r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r, M	Move memory to register	0	1	D	D	D	1	1	0	7
MOV r1,r2	Move register to register	0	1	D	D	D	S	S	S	5
NOP	No-operation	0	0	0	0	0	0	0	0	4
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
OUT	Output	1	1	0	1	0	0	1	1	10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RET	Return	1	1	0	0	1	0	0	1	10
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RST	Restart	1	1	A	A	A	1	1	1	11
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
STA	Store A direct	0	0	1	1	0	0	1	0	13
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
STC	Set carry	0	0	1	1	0	1	1	1	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18

NOTES: 1. DDD or SSS — 000 B — 001 C — 010 D — 011E — 100H — 101L — 110 Memory — 111 A.
2. Two possible cycle times, (5/11) indicate instruction cycles dependent on condition flags.

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Tel: (203) 762-0361
Harvey Electronics
112 Main Street
Norwalk 06851
Tel: (203) 853-1515

FLORIDA
Cramer/E.W. Hollywood
4035 No. 29th Avenue
Hollywood 33020
Tel: (305) 921-7878
†*Hamilton/Avnet Electronics
6800 Northwest 20th Ave.
Ft. Lauderdale 33309
Tel: (305) 971-2900
Cramer/EW Orlando
345 No. Graham Ave.
Orlando 32814
Tel: (305) 894-1511
Pioneer
6220 S. Orange Blossom Trail
Suite 412
Orlando 32809
Tel: (305) 859-3600

GEORGIA
†Cramer
6456 Warren Drive
Norcross 30071
Tel: (404) 448-9050

**Note New Telephone Number

GEORGIA (cont.)
†*Hamilton/Avnet Electronics
6700 I 85, Access Road, #11
Norcross 30071
Tel: (404) 448-0800

ILLINOIS
†Cramer/Chicago
1911 So. Busse Rd.
Mt. Prospect 60056
Tel: (312) 593-8230
†*Hamilton/Avnet Electronics
3901 No. 25th Ave.
Schiller Park 60176
Tel: (312) 678-6310
Pioneer/Chicago
1551 Carmen Drive
Elk Grove Village 60006
Tel: (312) 437-9680

INDIANA
†Pioneer/Indiana
6408 Castleplace Drive
Indianapolis 46250
Tel: (317) 849-7300
Sheridan Sales
8790 Purdue Road
Indianapolis 46268
Tel: (317) 297-3146

KANSAS
†*Hamilton/Avnet Electronics
9219 Quivira Road
Overland Park 66215
Tel: (913) 888-8900

MARYLAND
†Cramer/EW Washington
16021 Industrial Drive
Gaithersburg 20760
Tel: (301) 948-0110
†*Hamilton Avnet
7235 Standard Drive
Hanover 21076
Tel: (301) 796-5000
†Pioneer/Washington
9100 Gaither Road
Gaithersburg 20760
Tel: (301) 948-0710
TWX: 710-828-0545

MASSACHUSETTS
†Cramer Electronics Inc.
85 Wells Avenue
Newton 02159
Tel: (617) 969-7700
†*Hamilton/Avnet Electronics
100 E. Commerce Way
Woburn 01801
Tel: (617) 933-8000

MICHIGAN
†Sheridan Sales Co.
24543 Indoplex Circle
Farmington Hills 48024
Tel: (313) 477-3800
†Pioneer/Michigan
13485 Stamford
Livonia 48150
Tel: (313) 525-1800
†*Hamilton/Avnet Electronics
32487 Schoolcraft Road
Livonia 48150
Tel: (313) 522-4700
TWX: 810-242-8775

MINNESOTA
†Industrial Components
5280 West 74th Street
Minneapolis 55435
Tel: (612) 831-2666
†Cramer/Bonn
7275 Bush Lake Road
Edina 55435
Tel: (612) 835-7811
†*Hamilton/Avnet Electronics
7683 Washington Avenue So.
Edina 55435
Tel: (612) 941-3801

MISSOURI
†*Hamilton/Avnet Electronics
396 Brookes Lane
Hazelwood 63042
Tel: (314) 731-1144
Sheridan Sales
110 S. Hwy. 67, Suite 10
Florissant 63031
Tel: (314) 837-5200

NEW JERSEY
Cramer/Pennsylvania, Inc.
12 Springdale Road
Cherry Hill Industrial Center
Cherry Hill 08034
Tel: (609) 424-5993
TWX: 710-896-0908
†*Hamilton/Avnet Electronics
218 Little Falls Road
Cedar Grove 07009
Tel: (201) 239-0800
TWX: 710-994-5787
Cramer/New Jersey
1 Cardinal Drive
Little Falls 07424
Tel: (201) 785-4300

NEW JERSEY (cont.)
†Harvey Electronics
389 Passaic Avenue
Fairfield 07006
Tel: (201) 227-1262
†*Hamilton/Avnet Electronics
113 Gaither Drive
East Gate Industrial Park
Mt. Laurel 08057
Tel: (609) 234-2133
TWX: 710-897-1405

NEW MEXICO
†*Hamilton/Avnet Electronics
2524 Baylor Drive, S.E.
Albuquerque 87119
Tel: (505) 765-1500

NEW YORK
†Cramer/Rochester
3000 Winton Road South
Rochester 14623
Tel: (716) 275-0300
†*Hamilton/Avnet Electronics
167 Clay Road
Rochester 14623
Tel: (716) 442-7820
Cramer/Syracuse
6716 Joy Road
East Syracuse 13057
Tel: (315) 437-6671
†*Hamilton/Avnet Electronics
6500 Joy Road
E. Syracuse 13057
Tel: (315) 437-2641
†Cramer/Long Island
129 Oser Avenue
Hauppauge, L.I. 11787
Tel: (516) 231-5600
TWX: 510-227-9863
†*Hamilton/Avnet Electronics
70 State Street
Westbury, L.I. 11590
Tel: (516) 333-5800
TWX: 510-222-8237
†Harvey Electronics
60 Crossways Park West
Woodbury 11797
Tel: (516) 921-8700

NORTH CAROLINA
†Cramer Electronics
938 Burke Street
Winston-Salem 27102
Tel: (919) 725-8711
Pioneer/Carolina
2906 Baltic Avenue
Greensboro 27406
Tel: (919) 273-4441
TWX: 510-925-1114
Hamilton/Avnet Electronics, Inc.
2803 Industrial Drive
Raleigh 27609
Tel: (919) 829-8030

OHIO
†Sheridan Sales Co.
2501 Neff Road
Dayton 45414
Tel: (513) 223-3332
†Cramer/Cleveland
5835 Harper Road
Cleveland 44139
Tel: (216) 248-8400
†*Hamilton/Avnet Electronics
954 Senate Drive
Dayton 45459
Tel: (513) 433-0610
TWX: 810-450-2531
†Pioneer/Dayton
1900 Troy Street
Dayton 45404
Tel: (513) 236-9900
†Sheridan Sales Co.
10 Knollcrest Drive
Cincinnati 45222
Tel: (513) 761-5432
TWX: 810-461-2670
†Pioneer/Cleveland
4800 E. 131st Street
Cleveland 44105
Tel: (216) 587-3600
†*Hamilton/Avnet Electronics
761 Beta Drive, Suite E
Cleveland 44143
Tel: (216) 461-1400
†Sheridan Sales Co.
23224 Commerce Park Road
Beachwood 44122
Tel: (216) 831-0130

OKLAHOMA
†Components Specialties, Inc.
7920 E. 40th Street
Tulsa 74145
Tel: (918) 664-2820

OREGON
†Almac/Stroum Electronics
4475 S.W. Scholls Ferry Rd.
Portland 97225
Tel: (503) 292-3534

PENNSYLVANIA
†Sheridan Sales Co.
1717 Penn Avenue, Suite 5009
Pittsburgh 15221
Tel: (412) 244-1640
Pioneer/Pittsburgh
560 Alpha Drive
Pittsburgh 15238
Tel: (412) 782-2300

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Pioneer/Delaware
141 Gibraltar Road
Horsham 19044
Tel: (215) 674-4000
TWX: 510-665-6778

TENNESSEE
Sheridan Sales Co.
6900 Office Park Circle
Knoxville 37919
Tel: (615) 588-5386

TEXAS
Component Specialties Inc.
8330 Burnett Road, Suite 101
Austin 78758
Tel: (512) 459-3308
†Cramer Electronics
13740 Midway Road
Dallas 75240
Tel: (214) 661-9300
†*Hamilton/Avnet Electronics
4445 Sigma Road
Dallas 75240
Tel: (214) 661-8661
†*Hamilton/Avnet Electronics
3939 Ann Arbor
Houston 77083
Tel: (713) 780-1771
†Component Specialties, Inc.
10907 Shady Trail, Suite 101
Dallas 75220
Tel: (214) 357-6511
†Component Specialties, Inc.
8585 Commerce Park Drive, Suite 590
Houston 77036
Tel: (713) 771-7237

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†*Hamilton/Avnet Electronics
1585 West 2100 South
Salt Lake City, 84119
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WASHINGTON
†*Hamilton/Avnet Electronics
13407 Northrup Way
Bellevue 98005
Tel: (206) 746-8750
†Almac/Stroum Electronics
5811 Sixth Ave. South
Seattle 98108
Tel: (206) 763-2300
†Liberty Electronics
1750 132nd Avenue NE
Bellevue 98005
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2975 Moorland Road
New Berlin 53151
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TWX: 610-492-8867
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1735 Courtwood Cresc.
Ottawa K2C 3J2
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141 Catherine Street
Ottawa, Ontario K2P 1C3
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99 Norfinch Dr.
Downsview, Ontario M3N 1W8
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†*Hamilton/Avnet Electronics
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