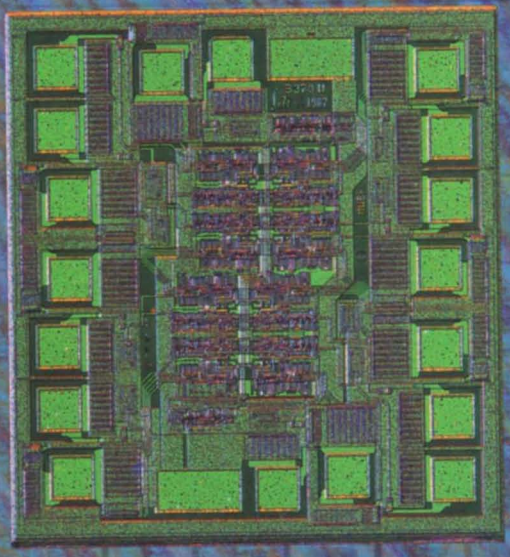
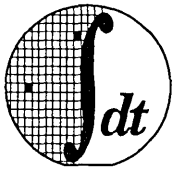
1990/91 DATABOOK

LOGIC



Integrated Device Technology, Inc.



Integrated Device Technology, Inc.

1990-91
LOGIC DATA BOOK

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GENERAL INFORMATION

CONTENTS OVERVIEW

Historically, Integrated Device Technology has presented our product offerings entirely under one cover. For ease of use for our customers, we have divided the products into four separate data books — Logic, Specialized Memory, RISC and Static RAM.

IDT's 1990 Logic Data Book is comprised of new and revised data sheets and application notes for both the Complex Logic and Standard Logic product lines. Also included is a current, complete packaging section for all product groups. This section will be updated in each subsequent data book with the latest available packages.

The Logic Data Book's Table of Contents is a listing of the products contained in the 1990 Logic Data Book, as well as those products which we believe will be in the remaining three data books, to be published later in the year. The numbering scheme is slightly different from the past. The number in the bottom center of the page denotes the section number and the sequence of the data sheet within that section, (i.e., 5.5 would be the fifth data sheet in the fifth section). The number in the lower right-hand corner is the page number of that particular data sheet.

Integrated Device Technology, a recognized leader in high-speed CMOS technology, produces a broad line of products, enabling us to provide a complete CMOS solution to designers of high-performance digital systems. Our products include industry standard devices, as well as products with speed, lower power, package and/or architectural benefits that allow the designer to achieve significantly improved system performance.

Use this book to find ordering information: Start with the Ordering Information chart at the back of each data sheet, or for the Complex Logic product line, the Cross Reference Guide (page 1.6), then reference the Package Outline Index (page 4.2), to compose the complete IDT part number. Reference data on our Technology Capabilities and Quality Commitments are included in separate sections (2 and 3, respectively).

Use this book to find product data: Start with the Table of Contents, organized by product line (page 1.3), or with the Numeric Table of Contents across all product lines (page 1.4). These indices will direct you to the page on which the complete technical data sheet can be found. Data sheets may be of the following type:

ADVANCE INFORMATION — contain initial descriptions, subject to change, for products that are in development, including features and block diagrams.

PRELIMINARY — contain descriptions for products soon to be released or recently released to production, including features, pinouts and block diagrams. Timing data are based on imulation or initial characterization and are subject to change upon full characterization.

FINAL — contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New products, product performance enhancements, additional package types and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types and product availability.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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APPLICATION AND TECHNICAL NOTES

IDT SALES OFFICE, REPRESENTATIVE AND DISTRIBUTOR LOCATIONS

SPECIALIZED MEMORY DATA BOOK

The following is a list of data sheets expected to be included in the Specialized Memory Data Book due for publication 4Q90. Until its release, please refer to your 1989 Data Book Supplement.

ECL PRODUCTS

IDT10484	4K x 4 ECL 10K SRAM
IDT100484	4K x 4 ECL 100K SRAM
IDT101484	4K x 4 ECL 101K SRAM
IDT10490	64K x 1 ECL 10K SRAM
IDT100490	64K x 1 ECL 100K SRAM
IDT101490	64K x 1 ECL 101K SRAM
IDT10494	16K x 4 ECL 10K SRAM
IDT100494	16K x 4 ECL 100K SRAM
IDT101494	16K x 4 ECL 101K SRAM
IDT10496LL	16K x 4 Self-Timed Latch Input, Latch Output
IDT100496LL	16K x 4 Self-Timed Latch Input, Latch Output
IDT101496LL	16K x 4 Self-Timed Latch Input, Latch Output
IDT10496RL	16K x 4 Self-Timed Reg Input, Latch Output
IDT100496RL	16K x 4 Self-Timed Reg Input, Latch Output
IDT101496RL	16K x 4 Self-Timed Reg Input, Latch Output
IDT10497	16K x 4 Synchronous Write, Latch Output
IDT100497	16K x 4 Synchronous Write, Latch Output
IDT101497	16K x 4 Synchronous Write, Latch Output
IDT10498	16K x 4 Conditional Write, Latch Output
IDT100498	16K x 4 Conditional Write, Latch Output
IDT101498	16K x 4 Conditional Write, Latch Output
IDT10504	64K x 4 ECL 10K SRAM
IDT100504	64K x 4 ECL 100K SRAM
IDT101504	64K x 4 ECL 100K SRAM
IDT10506LL	64K x 4 Self-Timed Latch Input, Latch Output
IDT100506LL	64K x 4 Self-Timed Latch Input, Latch Output
IDT101506LL	64K x 4 Self-Timed Latch Input, Latch Output
IDT10506RLA	64K x 4 Self-Timed Reg Input, Latch Output
IDT100506RLA	64K x 4 Self-Timed Reg Input, Latch Output
IDT101506RLA	64K x 4 Self-Timed Reg Input, Latch Output
IDT10507	64K x 4 Synchronous Write, Latch Output
IDT100507	16K x 4 Synchronous Write, Latch Output
IDT101507	16K x 4 Synchronous Write, Latch Output
IDT10508	64K x 4 Conditional Write, Latch Output
IDT100508	64K x 4 Conditional Write, Latch Output
IDT101508	64K x 4 Conditional Write, Latch Output
IDT10509	32K x 9 ECL 10K SRAM
IDT100509	32K x 9 ECL 100K SRAM
IDT101509	32K x 9 ECL 101K SRAM

FIFO PRODUCTS

IDT7200	256 x 9-Bit Parallel FIFO
IDT7201	512 x 9-Bit Parallel FIFO
IDT7202	1024 x 9-Bit Parallel FIFO
IDT7203	2K x 9-Bit Parallel FIFO
IDT7204	4K x 9-Bit Parallel FIFO
IDT7205	8K x 9-Bit Parallel FIFO
IDT7206	16K x 9-Bit Parallel FIFO
IDT72021	1K x 9-Bit Parallel FIFO w/ Flags and $\overline{OE}$
IDT72031	2K x 9-Bit Parallel FIFO w/Flags and $\overline{OE}$

FIFO PRODUCTS (CONTINUED)

IDT72041	4K x 9-Bit Parallel FIFO w/Flags and $\overline{OE}$
IDT72103	2K x 9-Bit Configurable Parallel-Serial FIFO
IDT72104	4K x 9-Bit Configurable Parallel-Serial FIFO
IDT72105	256 x 16-Bit Parallel-to-Serial FIFO
IDT72115	512 x 16-Bit Parallel-to-Serial FIFO
IDT72125	1024 x 16-Bit Parallel-to-Serial FIFO
IDT72131	2048 x 9-Bit Parallel-to-Serial FIFO
IDT72141	4096 x 9-Bit Parallel-to-Serial FIFO
IDT72132	2048 x 9-Bit Serial-to-Parallel FIFO
IDT72142	2048 x 9-Bit Serial-to-Parallel FIFO
IDT72200	256 x 8-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72210	512 x 8-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72420	64 x 8-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72201	256 x 9-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72211	512 x 9-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72421	64 x 9-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72215A	512 x 18-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72225A	1024 x 18-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72220	1K x 8-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72230	2K x 8-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72240	4K x 8-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72221	1K x 9-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72231	2K x 9-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72241	4K x 9-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72235	2K x 18-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72245	4K x 18-Bit Parallel SyncFIFO™ (Clocked FIFO)
IDT72401	64 x 4 FIFO
IDT72402	64 x 5 FIFO
IDT72403	64 x 4 FIFO w/$\overline{OE}$
IDT72404	64 x 5 FIFO w/$\overline{OE}$
IDT72413	64 x 5 FIFO (w/Flags)
IDT7251	512 x 18-Bit — 1K x 9-Bit BiFIFO
IDT7252	1K x 18-Bit — 2K x 9-Bit BiFIFO
IDT72510	512 x 18-Bit — 1K x 9-Bit BiFIFO
IDT72520	1K x 18-Bit — 2K x 9-Bit BiFIFO
IDT72511	512 x 18-Bit BiFIFO
IDT72521	1K x 18-Bit BiFIFO
IDT72605	256 x 18-Bit Synchronous BiFIFO (SyncBiFIFO™)
IDT72615	512 x 18-Bit Synchronous BiFIFO (SyncBiFIFO™)

SPECIALTY MEMORY PRODUCTS

IDT7130	8K (1K x 8) Dual-Port RAM (MASTER)
IDT7140	8K (1K x 8) Dual-Port RAM (SLAVE)
IDT7030	8K (1K x 8) Dual-Port RAM (MASTER)
IDT7040	8K (1K x 8) Dual-Port RAM (SLAVE)
IDT7010	9K (1K x 9) Dual-Port RAM (MASTER)
IDT70104	9K (1K x 9) Dual-Port RAM (SLAVE)
IDT70101	9K (1K x 9) Dual-Port RAM (MASTER w/Interrupts)
IDT70105	9K (1K x 9) Dual-Port RAM (SLAVE w/Interrupts)
IDT7132	16K (2K x 8) Dual-Port RAM (MASTER)
IDT7142	16K (2K x 8) Dual-Port RAM (SLAVE)
IDT7032	16K (2K x 8) Dual-Port RAM (MASTER)
IDT7042	16K (2K x 8) Dual-Port RAM (SLAVE)
IDT71321	16K (2K x 8) Dual-Port RAM (MASTER w/Interrupts)

SPECIALTY MEMORY PRODUCTS (CONTINUED)

IDT71421	16K (2K x 8) Dual-Port RAM (SLAVE w/Interrupts)
IDT71322	16K (2K x 8) Dual-Port RAM (w/Semaphores)
IDT7012	18K (2K x 9) Dual-Port RAM
IDT70121	18K (2K x 9) Dual-Port RAM (MASTER w/Interrupts)
IDT70125	18K (2K x 9) Dual-Port RAM (SLAVE w/Interrupts)
IDT7133	32K (2K x 16) Dual-Port RAM (MASTER)
IDT7143	32K (2K x 16) Dual-Port RAM (SLAVE)
IDT7134	32K (4K x 8) Dual-Port RAM
IDT71342	32K (4K x 8) Dual-Port RAM (w/Semaphores)
IDT7014	32K (4K x 9) Dual-Port RAM
IDT7024	64K (4K x 16 Dual-Port RAM
IDT7005	64K (8K x 8) Dual-Port RAM
IDT7025	128K (8K x 16) Dual-Port RAM
IDT7006	128K (16K x 8) Dual-Port RAM
IDT7044	144K (4K x 36) Dual-Port RAM
IDT7050	8K (1K x 8) FourPort™ RAM
IDT7052	16K (2K x 8) FourPort™ RAM

SUBSYSTEMS PRODUCTS

MULTI-PORT MODULES

IDT7M134	8K x 8 Master Dual-Port SRAM Module
IDT7M144	8K x 8 Slave Dual-Port SRAM Module
IDT7M135	16K x 8 Master Dual-Port SRAM Module
IDT7M145	16K x 8 Slave Dual-Port SRAM Module
IDT7M137	32K x 8 Master Dual-Port SRAM Module
IDT7M1003	64K x 8 Dual-Port SRAM Module
IDT7M1001	128K x 8 Dual-Port SRAM Module
IDT7M1004	8K x 8 Dual-Port SRAM Module
IDT7M1005	16K x 9 Dual-Port SRAM Module
IDT7MB6056	32K x 16 Dual-Port (Shared Memory) SRAM Module
IDT7MB1008	32K x 16 Dual-Port SRAM Module
IDT7MB1006	64K x 16 Dual-Port SRAM Module
IDT7MB6046	64K x 16 Dual-Port (Shared Memory) SRAM Module
IDT7MB6036	128K x 16 Dual-Port (Shared Memory) SRAM Module
IDT7MB6156	32K x 18 Dual-Port (Shared Memory) SRAM Module
IDT7MB6146	64K x 18 Dual-Port (Shared Memory) SRAM Module
IDT7MB6136	128K x 18 Dual-Port (Shared Memory) SRAM Module
IDT7M1002	16K x 32 Dual-Port SRAM Module
IDT7M1041	8K x 8 FourPort™ SRAM Module
IDT7M1042	4K x 8 FourPort™ SRAM Module
IDT7M1043	4K x 16 FourPort™ SRAM Module
IDT7M1044	2K x 16 FourPort™ SRAM Module

FIFO MODULES

IDT7M205	8K x 9-Bit CMOS FIFO Module
IDT7MP2005	8K x 9-Bit FIFO Module
IDT7M206	16K x 9-Bit CMOS FIFO Module
IDT7MP2011	16K x 9 Bit FIFO Module
IDT7M207	32K x 9-Bit CMOS FIFO Module
IDT7MP2010	16K x 18-Bit FIFO Module
IDT7MP2009	32K x 18-Bit FIFO Module

SRAM MODULES

IDT7MC4001	1M x 1 CMOS Static RAM Module
IDT7M4042	256K x 4 CMOS Static RAM Module
IDT7M812	64K x 8 CMOS Static RAM Module
IDT8M824	128K x 8 CMOS Static RAM Module
IDT8MP824	128K x 8 CMOS Static RAM Module
IDT7MP4034	256K x 8 CMOS Static RAM Module
IDT7M4048	512K x 8 CMOS Static RAM Module
IDT7MP4008	512K x 8 CMOS Static RAM Module
IDT7M912	64K x 9 CMOS Static RAM Module
IDT7MC4005	16K x 16 CMOS Static RAM Module
IDT7MB4009	2(16K x 16) CMOS Static RAM Module
IDT8M612	32K x 16 CMOS Static RAM Module
IDT8MP612	32K x 16 CMOS Static RAM Module
IDT7M624	64K x 16 CMOS Static RAM Module
IDT8M624	64K x 16 CMOS Static RAM Module
IDT8MP624	64K x 16 CMOS Static RAM Module
IDT7M4016	256K x 16 CMOS Static RAM Module
IDT7MP4047	512K x 16 CMOS Static RAM Module
IDT7MC4032	16K x 32 CMOS Static RAM Module w/Separate Data I/O
IDT7MP4031	16K x 32 CMOS Static RAM Module
IDT7M4003	32K x 32 CMOS Static RAM Module
IDT7M4017	64K x 32 CMOS Static RAM Module
IDT7MP4036	64K x 32 CMOS Static RAM Module
IDT7MP4045	256K x 32 CMOS Static RAM Module

CACHE MODULES

IDT7MB6064	Dual (4K x 60) Data/Instruction Cache Module for IDT79R3000 CPU
IDT7MB6044	Dual (4K x 64) Data/Instruction Cache Module for IDT79R3000 CPU
IDT7MB6043	Dual (8K x 64) Data/Instruction Cache Module for IDT79R3000 CPU
IDT7MB6051	Dual (8K x 64) Data/Instruction Cache Module for IDT79R3000 CPU (Multiprocessor)
IDT7MB6039	Dual (16K x 60) Data/Instruction Cache Module for IDT79R3000 CPU
IDT7MB6049	Dual (16K x 60) Data/Instruction Cache Module for IDT79R3000 CPU (Multiprocessor)
IDT7MB6040	Dual (16K x 64) Data/Instruction Cache Module for General CPUs
IDT7MB6061	Dual (16K x 60) Data/Instruction w/Resettable Instruction Tag

WRITABLE CONTROL STORE MODULES

IDT7M6032	16K x 32 Writable Control Store Static RAM Module
IDT7MB6042	8K x 112 Writable Control Store Static RAM Module
Flexi-Pak Module Family	Various Combinations of Four SRAMs, EPROMs and EEPROMs Packaged in 32-Lead JEDEC LCCs Mounted on PGA-Type Substrate

RISC DATA BOOK

The following is a list of data sheets expected to be included in the RISC Data Book due for publication 4Q90. Until its release, please refer to your 1980 Data Book Supplement.

RISC MICROPROCESSOR PRODUCTS

RISC COMPONENTS

IDT79R3000	RISC CPU Processor
IDT79R3001	32-Bit RISController™
IDT79R3010	RISC Floating-Point Accelerator
IDT79R3020	RISC CPU Write Buffer
IDT79R4000	Third Generation RISC Processor

RISC DEVELOPMENT SYSTEMS

RS1210	RISComputer™ Development System
RC2030	RISComputer™ Development System
RC3240	RISComputer™ Development System
RC3260	RISComputer™ Development System

M/2000 RISComputer™ Development System

RISC DEVELOPMENT SOFTWARE

3106 Ada	Ada Compiler
3120C-SRC (SPP)	System Programmer's Package
3123C-SRC (SPP/e)	System Programmer's Package/e
3178C-SRC (ASAPP)	Ada Stand-alone Programmer's Package

RISC SUBSYSTEM PRODUCTS

RISC CPU MODULES

IDT7RS101	R3000 Module w/64K I-Cache, 64K D-Cache, 4 Word Read Buffer and 1 Word Write Buffer
IDT7RS101F	R3000, R3010 Module w/64K I-Cache, 64K D-Cache, 4 Word Read Buffer and 1 Word Write Buffer
IDT7RS102	R3000 Module w/16K I-Cache, 16K D-Cache, 1 Word Read Buffer and 1 Word Write Buffer
IDT7RS102F	R3000, R3010 Module w/16K I-Cache, 16K D-Cache, 1 Word Read Buffer and 1 Word Write Buffer
IDT7RS103	R3000 Module w/16K I-Cache and 16K D-Cache
IDT7RS103F	R3000, R3010 Module w/16K I-Cache and16K D-Cache
IDT7RS104	R3001 Module w/ 128K I-Cache, 128K D-Cache, 1 Word Read Buffer and 1 Word Write Buffer
IDT7RS104F	R3001, R3010 Module w/128K I-Cache, 128K D-Cache, 1 Word Read Buffer and 1 Word Write Buffer
IDT7RS105	R3000 Module w/32K I-Cache, 16K D-Cache, 1 Word Read Buffer, 1 Word Write Buffer and IDT Bus
IDT7RS105F	R3000, R3010 Module w/32K I-Cache, 16K D-Cache, 1 Word Read Buffer, 1 Word Write Buffer and IDT Bus
IDT7RS107F	R3000, R3010 Module w/64K I-Cache, 64K D-Cache, 0R3020 and 1 Word Read Buffer

RISC TargetSystems

IDT7RS301	TargetSystem™ for IDT7RS101
IDT7RS302	TargetSystem™ for IDT7RS102
IDT7RS303	TargetSystem™ for IDT7RS103
IDT7RS304	TargetSystem™ for IDT7RS104
IDT7RS305	TargetSystem™ for IDT7RS105
IDT7RS307	TargetSystem™ for IDT7RS107

RISC SUBSYSTEM PRODUCTS (CONTINUED)

SUPPORT PRODUCTS

IDT7RS201	Nubus Board
IDT7RS202	Nubus Board, Supports Nubus Memory
IDT7RS203	Nubus Board, Supports Onboard Memory
IDT7RS340	System Board
IDT7RS341	Personality Board for IDT7RS101
IDT7RS342	Personality Board for IDT7RS102
IDT7RS343	Personality Board for IDT7RS103
IDT7RS347	Personality Board for IDT7RS107
IDT7RS353-B	JMI C-Executive™ Binary Code
IDT7RS353-MB	JMI C-Executive™ Maintenance for Binary Code
IDT7RS353-S	JMI C-Executive™ SourceCode
IDT7RS353-MS	JMI C-Executive™ Maintenance for Source Code
IDT7RS355-B	Floating Point Library Binary Code
IDT7RS355-MB	Floating Point Library Maintenance for Binary Code
IDT7RS355-S	Floating Point Library Source Code
IDT7RS355-MS	Floating Point Library Maintenance for Source Code
IDT7RS356-2B	R3000 C-Compiler Binary Code for 80286, 80386 IDT7RS356-2MB R3000 C-Compiler Maintenance for Binary Code for 80286, 80386 PC-DOS
IDT7RS356-3B	R3000 C-Compiler Binary Code for PC SCO XENIX
IDT7RS356-3MB	R3000 C-Compiler Maintenance for Binary Code SCO XENIX
IDT7RS357-1B	R3000 Macro Assembler Binary Code for 8086, 8088 PC-DOS
IDT7RS357-1MB	R3000 Macro Assembler Maintenance for Binary Code 8086, 8088
IDT7RS357-2B	R3000 Macro Assembler Binary Code for 80286, 80386 PC-DOS
IDT7RS357-2MB	R3000 Macro Assembler Maintenance for Binary Code 80286, 80386
IDT7RS357-3B	R3000 Macro Assembler Binary Code for PC SCO XENIX
IDT7RS357-3MB	R3000 Macro Assembler Maintenance for Binary Code SCO XENIX
IDT7RS361-B	IDT PROM Monitor Binary Code
IDT7RS361-MB	IDT PROM Monitor Maintenance for Binary Code
IDT7RS361-E	IDT PROM Monitor Binary Code — in 4 EPROMs
IDT7RS361-S	IDT PROM Monitor Source Code
IDT7RS361-MS	IDT PROM Monitor Maintenance for Source Code
IDT7RS363-1	R3000 PGA Breakout Board and HP 16500A Logic Analyzer Set-up Software
IDT7RS363-2	R3000 PGA Breakout Board and HP 16500A Logic Analyzer Set-up Software and 5 HP Adapters
IDT7RS364	HP 16500A Logic Analyzer Disassembler Software for 7RS300 Series TargetSystems™
IDT7RS365	R3000 Flatpack Version
IDT7RS366	R3001 PGA Version
IDT7RS382	R3000 Evaluation Board
IDT7RS383	R3001 Evaluation Board

MacStation™ DEVELOPMENT SYSTEM

IDT7RS501-1	MacStation™ Development System w/IDT7RS201 Nubus Board, IDT/ux and C-Compiler
IDT7RS501-1D	MacStation™ Development System Documentation
IDT7RS501-1M	MacStation™ Development System Maintenance
IDT7RS501-2	MacStation™ Development System w/150MB External Hard Disk, 40MB External Tape Drive, IDT7RS201 Nubus Board, IDT/ux and C-Compiler
IDT7RS501-3	Complete IDT7RS501 MacStation™ Development System w/MAC II Computer, 8MB RAM, 150MB Hard Disk, 40MB External Tape Drive, IDT7RS201 Nubus Board, IDT/ux and C-Compiler
IDT7RS501-4	4MB SIMM Module for MAC II
IDT7RS501-5	IDT7RS501 MacStation™ Development System w/150MB External Hard Disk, IDT7RS201 Nubus Board, IDT/ux and C-Compiler

RISC SUBSYSTEM PRODUCTS (CONTINUED)
MacStation™ DEVELOPMENT SYSTEM (CONTINUED)

IDT7RS501-6	IDT7RS501 MacStation™ Development System w/40MB External Tape Drive, IDT7RS201 Nubus Board, IDT/ux and C-Compiler
IDT7RS502-1	MacStation™ Development System w/IDT7RS202 Nubus Board, 8MB Nubus RAM Board, IDT/ux and C-Compiler
IDT7RS502-1D	MacStation™ Development System Documentation
IDT7RS502-1M	MacStation™ Development System Maintenance
IDT7RS502-2	IDT7RS502 MacStation™ Development System w/150MB External Hard Disk, 40MB External Tape Drive, IDT7RS202 Nubus Board, IDT/ux and C-Compiler
IDT7RS502-3	Complete IDT7RS502 MacStation™ Development System w/MAC II Computer, 8MB RAM, 150MB Hard Disk, 40MB External Tape Drive, IDT7RS202 Nubus Board, IDT/ux and C-Compiler
IDT7RS502-4	4MB SIMM Module for MAC II
IDT7RS502-5	IDT7RS502 MacStation™ Development System w/150MB External Hard Disk, IDT7RS202 Nubus Board, IDT/ux and C-Compiler
IDT7RS502-6	IDT7RS502 MacStation™ Development System w/40MB External Tape Drive, IDT7RS202 Nubus Board, IDT/ux and C-Compiler
IDT7RS503-1	MacStation™ Development System w/16MB RAM, IDT/ux and C-Compiler
IDT7RS503-1D	MacStation™ Development System Documentation
IDT7RS503-1M	MacStation™ Development System Maintenance
IDT7RS551-1B	IDT/ux — UNIX Operating System for MacStations™
IDT7RS571-1S	MIPS SPP for the MAC
IDT7RS572-1S	MIPS SPP/e for the MAC
IDT7RS573-1B	MIPS Fortran for the MAC
IDT7RS573-1MB	Maintenance for MIPS Fortran for the MAC

STATIC RAM DATA BOOK

The following is a list of data sheets expected to be included in the Static RAM Data Book due for publication 1Q91. Until its release, please refer to your 1980 Data Book Supplement.

STATIC RAM PRODUCTS

IDT6167	16K x 1 w/Power-Down
IDT6168	4K x 4 w/Power-Down
IDT6177	4K x 4 Cache-Tag w/Open Drain and Power-Down
IDT6178	4K x 4 Cache-Tag w/Power-Down
IDT61970	4K x 4 w/Output Enable and Power-Down
IDT71681	4K x 4 w/Separate I/O and Power-Down
IDT71682	4K x 4 w/Separate I/O and Power-Down
IDT6116	2K x 8 w/Power-Down
IDT7187	64K x 1 w/Power-Down
IDT6198	16K x 4 w/Output Enable and Power-Down
IDT7188	16K x 4 w/Power-Down
IDT7198	16K x 4 w/Output Enable, 2 Chip Selects and Power-Down
IDT61B98	16K x 4 BiCEMOS™ w/Output Enable
IDT71981	16K x 4 w/Separate I/O and Power Down
IDT71982	16K x 4 w/Separate I/O and Power Down
IDT71B88	16K x 4 BiCEMOS™
IDT71B98	16K x 4 BiCEMOS w/Output Enable and 2 Chip Selects
IDT7164	8K x 8 w/Power-Down
IDT7165	8K x 8 Resettable Power-Down
IDT7174	8K x 8 Cache-Tag w/Power-Down
IDT71B64	8K x 8 BiCEMOS™
IDT71B65	8K x 8 BiCEMOS™ Resettable
IDT71B74	8K x 8 BiCEMOS™ Cache-Tag
IDT7186	4K x 16 w/Power-Down
IDT71586	4K x 16 w/Address Latch and Power-Down
IDT7169	8K x 9 w/Power-Down
IDT71569	8K x 9 w/Address Latch and Power-Down
IDT71B569	8K x 9 BiCEMOS™ w/Address Latch
IDT71B69	8K x 9 BiCEMOS™
IDT71B79	8K x 9 BiCEMOS™ Cache-Tag
IDT71220	4K x 18 x 2 w/Single Address Latch and Power-Down
IDT71222	4K x 18 x 2 w/Dual Address Latches and Power-Down
IDT71270	4K x 18 x 2 Cache-Tag and Power-Down
IDT71257	256K x 1 w/Power-Down
IDT61298	64K x 4 w/Output Enable and Power-Down
IDT71258	64K x 4 w/Power-Down
IDT61B298	64K x 4 BiCEMOS™ w/Output Enable
IDT71281	64K x 4 w/Separate I/O and Power-Down
IDT71282	64K x 4 w/Separate I/O and Power-Down
IDT71B258	64K x 4 BiCEMOS™
IDT71256	32K x 8 w/Power-Down
IDT71B256	32K x 8 BiCEMOS™
IDT71B556	32K x 8 BiCEMOS™ w/Address Latch
IDT71259	32K x 9 w/Power-Down
IDT71509	32K x 9 w/Address Latch, Parity and Power-Down
IDT71559	32K x 9 w/Address Latch and Power-Down
IDT71589	32K x 9 Burst Mode w/Power-Down
IDT71027	1 Meg x 1 w/Power-Down
IDT71028	256K x 4 w/Power-Down
IDT71024	128K x 8 w/Power-Down

NUMERICAL TABLE OF CONTENTS

NUMERICAL TABLE OF CONTENTS (CONTINUED)

NUMERICAL TABLE OF CONTENTS (CONTINUED)

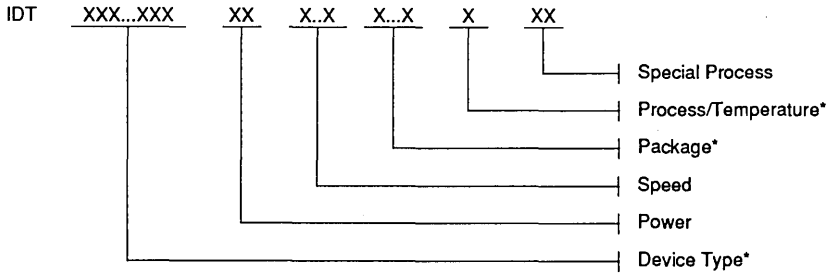
IDT PACKAGE MARKING DESCRIPTION

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, for ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "S" or "SA" is used for the standard product's power.
   "L" or "LA" is used for lower power than the standard product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or radiation tolerance (RT).

Example:



* Field Identifier Applicable To All Products

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ASSEMBLY LOCATION DESIGNATOR

IDT uses various locations for assembly. These are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

A = Anam, Korea
I = USA
P = Penang, Malaysia

MIL-STD-883C COMPLIANT DESIGNATOR

IDT ships military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.

Integrated Device Technology, Inc.

DIGITAL SIGNAL PROCESSING CROSS REFERENCE GUIDE

ANALOG DEVICES	IDT
ADSP-1009	**7209**
ADSP-1012	**7212**
ADSP-1010	**7210**
ADSP-1016	**7216**

CYPRESS	IDT
7C510	7210
7C510-45DC	7210L45D
7C510-45GC	7210L45G
7C510-45LC	7210L45L
7C510-45PC	7210L45P
7C510-55DC	7210L55D
7C510-55DMB	7210L55DB
7C510-55GC	7210L55G
7C510-55GMB	7210L55GB
7C510-55LC	7210L55L
7C510-55LMB	7210L55LB
7C510-55PC	7210L55P
7C510-65DC	7210L65D
7C510-65DMB	7210L65DB
7C510-65GC	7210L65G
7C510-65GMB	7210L65GB
7C510-65LC	7210L65L
7C510-65LMB	7210L65LB
7C510-65PC	7210L65P
7C516	7216
7C516-38DC	7216L35D
7C516-38GC	7216L35G
7C516-38LC	7216L35L
7C516-38PC	7216L35P
7C516-42DMB	7216L40DB
7C516-42GMB	7216L40GB
7C516-42LMB	7216L40LB
7C516-45DC	7216L45D
7C516-45GC	7216L45G
7C516-45LC	7216L45L
7C516-45PC	7216L45P
7C516-55DC	7216L55D
7C516-55DMB	7216L55DB
7C516-55GC	7216L55G
7C516-55GMB	7216L55GB
7C516-55LC	7216L55L
7C516-55LMB	7216L55LB
7C516-55PC	7216L55P
7C516-65DC	7216L65D
7C516-65DMB	7216L65DB
7C516-65GC	7216L65G
7C516-65GMB	7216L65GB
7C516-65LC	7216L65L
7C516-65LMB	7216L65LB
7C516-65PC	7216L65P
7C517	7217
7C517-45DC	7217L45D
7C517-45GC	7217L45G
7C517-45LC	7217L45L
7C517-45PC	7217L45P
7C517-55DC	7217L55D
7C517-55DMB	7217L55DB
7C517-55GC	7217L55G
7C517-55GMB	7217L55GB
7C517-55LC	7217L55L
7C517-55LMB	7217L55LB
7C517-55PC	7217L55P
7C517-65DC	7217L65D
7C517-65DMB	7217L65DB
7C517-65GC	7217L65G
7C517-65GMB	7217L65GB
7C517-65LC	7217L65L
7C517-65LMB	7217L65LB
7C517-65PC	7217L65P

LOGIC DEVICES	IDT
LMA1009	**7209**
LMA1009DC-45	7209L45C
LMA1009GC-45	7209L45G
LMA1009DMB-55	7209L55CB
LMA1009GMB-55	7209L55GB
LMA1009DC-75	7209L65C
LMA1009GC-75	7209L65G
LMA1009DC-90	7209L65C
LMA1009GC-90	7209L65G
LMA1009DMB-95	7209L75CB
LMA1009GMB-95	7209L75GB
LMA1009DMB-115	7209L75CB
LMA1009GMB-115	7209L75GB
LMA2009	**7209**
LMA2009KC-45	7209L45L
LMA2009KMB-55	7209L55LB
LMA2009KC-55	7209L45L
LMA2009KMB-65	7209L55LB
LMA2009KC-75	7209L65L
LMA2009KC-90	7209L65L
LMA2009KMB-95	7209L75LB
LMA2009KMB-115	7209L75LB
LMA1010	**7210**
LMA1010PC-45	7210L45P
LMA1010DC-45	7210L45C
LMA1010GC-45	7210L45G
LMA1010PC-55	7210L55P
LMA1010DC-55	7210L55C
LMA1010GC-55	7210L55G
LMA1010DBM-55	7210L55CB
LMA1010GMB-55	7210L55GB
LMA1010PC-65	7210L65P
LMA1010DC-65	7210L65C
LMA1010GC-65	7210L65G

LOGIC DEVICES (Con't)	IDT
LMA1010DMB-65	7210L65CB
LMA1010GMB-65	7210L65GB
LMA2010	**7210**
LMA2010JC-45	7210L45J
LMA2010KC-45	7210L45L
LMA2010JC-55	7210L55J
LMA2010KC-55	7210L55L
LMA2010KMB-55	7210L55LB
LMA2010JC-65	7210L65J
LMA2010KC-65	7210L65L
LMA2010KMB-65	7210L65LB
LMU12	**7212**
LMU12DC-45	7212L45C
LMU12DMB-55	7212L55CB
LMU12DC-65	7212L45C
LMU12DMB-75	7212L55CB
LMU12DC	7212L70C
LMU12DMB	7212L90CB
LMU16	**7216**
LMU16PC-45	7216L45P
LMU16DC-45	7216L45C
LMU16GC-45	7216L45G
LMU16PC-55	7216L55P
LMU16DC-55	7216L55C
LMU16GC-55	7216L55G
LMU16DMB-55	7216L55CB
LMU16GMB-55	7216L55GB
LMU16PC-65	7216L65P
LMU16DC-65	7216L65C
LMU16GC-65	7216L65G
LMU16DMB-65	7216L55CB
LMU16GMB-65	7216L55GB
LMU16PC	7216L65P
LMU16DC	7216L65C
LMU16GC	7216L65G
LMU216	**7216**
LMU216JC-45	7216L45J
LMU216KC-45	7216L45L
LMU216JC-55	7216L55J
LMU216KC-55	7216L55L
LMU216KMB-55	7216L55LB
LMU216JC-65	7216L65J
LMU216KC-65	7216L65L
LMU216KMB-65	7216L65LB
LMU17	**7217**
LMU17PC-45	7217L45P
LMU17DC-45	7217L45C
LMU17GC-45	7217L45G
LMU17PC-55	7217L55P
LMU17DC-55	7217L55C
LMU17GC-55	7217L55G
LMU17DMB-55	7217L55CB
LMU17GMB-55	7217L55GB
LMU17PC-65	7217L65P
LMU17DC-65	7217L65C

CYPRESS (Con't)	IDT
LMU17GC-65	7217L65G
LMU17DMB-65	7217L55CB
LMU17GMB-65	7217L55GB
LMU17PC	7217L65P
LMU17DC	7217L65C
LMU17GC	7217L65G
LMU217	**7217**
LMU217JC-45	7217L45J
LMU217KC-45	7217L45L
LMU217JC-55	7217L55J
LMU217KC-55	7217L55L
LMU217KMB-55	7217L55LB
LMU217JC-65	7217L65J
LMU217KC-65	7217L65L
LMU217KMB-65	7217L65LB
TRW	**IDT**
MPY012	**7212**
MPY016	**7216**
MPY016KJ1A	7216L45CB
MPY016KJ1A1	7216L45CB
MPY016KJ1C	7216L45C
MPY016KJ1C1	7216L35C
MPY016KJ1G	7216L45C
MPY016KJ1G1	7216L35C
TMC216H	**7216**
TDC1009	**7209**
TDC1010	**7210**
TMC2009	**7209**
TMC2010	**7210**
TMC2110	**7210**

IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the 80's and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CEMOS™ technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, IDT's product strategy has been to apply the advantages of it's extremely fast CEMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost weight and size. Many of the company's innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Producing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance fast SRAM , FCT logic family, high-density modules, FIFOs, complex logic products, specialty memories, ECL I/O BiCEMOS™ memories, RISC subsystems, and the 32-bit RISC microprocessor family complement each other to provide high-speed CMOS solutions to a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families and additional product lines will be introduced. Contact your IDT field representative or factory marketing engineer to determine the latest product offerings. If you're building state-of-the-art equipment, IDT wants to help you solve some of your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance Static RAMs, FCT Logic Family, Complex Logic (CLP), FIFOs, Specialty Memories (SMP), ECL I/O BiCMOS Memories, 32-bit RISC Microprocessor, RISC Subsystems and high-density Subsystems Modules product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Most of these product lines offer Class B products which are fully compliant to the latest revision of MIL-STD-883, Paragraph 1.2.1. In addition, IDT offers Radiation Tolerant (RT), as well as Radiation Enhanced (RE), products.

IDT has an active program with the Defense Electronic Supply Center (DESC) to list all of IDT's military compliant devices on Standard Military Drawings (SMD). The SMD program allows standardization of militarized products and reduction of the proliferation of non-standard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 88 devices which are listed or pending listing. The devices are from IDT's SRAM, FCT Logic family, Complex Logic (CLP), FIFOs and Specialty Memories (SMP) product families. IDT expects to add another 20 devices to the SMD program in the near future. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
84036/D	6116
5962-88740	6116LA
84132/B	6167
5962-86015/A	7187
5962-86859	6198/7198/7188
5962-86705/A	6168
5962-85525/A	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-88681/A	71258S
5962-88545	71258L
5962-88544	71257L
5962-88725/A	71257S
5962-89690	6116
5962-89691	7164
5962-89692	7188
5962-89712	71982
SMP	**IDT**
5962-86875/A	7130/7140
5962-87002/A	7132/7142
5962-88610/A	7133S/7143S
5962-88665/A	7133L/7143L
FIFO	**IDT**
5962-87531	7201LA
5962-86846/A	72404
5962-88669	7203S
5962-89568	7204L
5962-89536	7202L
5962-89863	7201S
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L

SMD	
LOGIC	**IDT**
5962-87630/B	54FCT244/A
5962-87629/C	54FCT245/A
5962-86862/A	54FCT299/A
5962-87644/A	54FCT373/A
5962-87628/C	54FCT374/A
5962-87627	54FCT377/A
5962-87654/A	54FCT138/A
5962-87655	54FCT240/A
5962-87656/A	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543/A	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	54FCT520A/B
5962-88775	54FCT646A/B
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88652	54FCT182/A
5962-88653	54FCT645A/B
5962-88654	54FCT640A/B
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-88675	54FCT845A/B
5962-89730	54FCT543/A

SMD	
CLP	**IDT**
5962-87708/A	39C10B & C
5962-88535	39C01
5962-88533/A	49C460A
5962-88613	39C60A
5962-88643	49C410
5962-88743	75C48S
5962-XXXXX	75C58
5962-XXXXX	75C458S
5962-89517	49C402/A
5962-86893	7216L
5962-87686	7217L
5962-88733	7210
5962-XXXXX	49C402L
5962-XXXXX	7320L
5962-XXXXX	7321L
5962-XXXXX	7383L
5962-XXXXX	7209L

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RADIATION HARDENED TECHNOLOGY

IDT manufactures and supplies radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices are able to survive in hostile radiation environments. In total dose, dose rate and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply all its products on these processes. Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an on-going research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/ processes.

IDT LEADING EDGE CEMOS TECHNOLOGY

HIGH-PERFORMANCE CEMOS

From IDT's beginnings in 1980, it has had a belief in and a commitment to CMOS. The company developed a high-performance version of CMOS, called enhanced CMOS (CEMOS), that allows the design and manufacture of leading-edge components. It incorporates the best characteristics of traditional CMOS, including low power, high noise immunity and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL. The last decade has seen development and production of four "generations" of IDT's CEMOS technology with process improvements which have reduced IDT's electrical effective (Leff) gate lengths by more than 50 percent from 1.3 microns (millionths of a meter) in 1981 to 0.6 microns in 1989.

	CEMOS I	CEMOS II		CEMOS III	CEMOS V	CEMOS VI
		A	C			
Calendar Year	**1981**	**1983**	**1985**	**1987**	**1989**	**1990**
Drawn Feature Size	2.5μ	1.7μ	1.3μ	1.2μ	1.0μ	0.8μ
Leff	1.3μ	1.1μ	0.9μ	0.8μ	0.6μ	0.45μ
Basic Proces Enhancements	Dual-well, Wet Etch, Projection Aligned	Dry Etch, Stepper	Shrink, Spacer	Silicide, BPSG, BiCEMOS I	BiCEMOS II	BiCEMOS III

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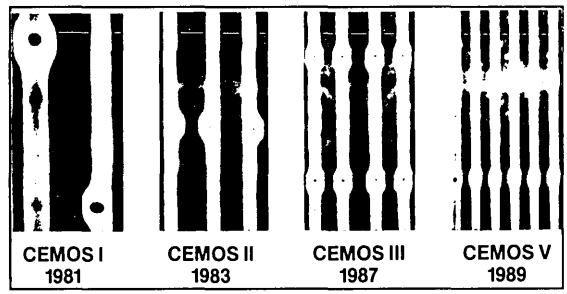
CEMOS IV = CEMOS III – scaled process optimized for high-speed logic.

Figure 1.

Continual advancement of CEMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits. In addition, the fundamental process technology has been extended to add bipolar elements to the CEMOS platform. IDT's BiCEMOS process combines the ultra-high speeds of bipolar devices with the lower power and cost of CMOS, allowing us to build even faster components than straight CMOS at a slightly higher cost.



SEM photos (miniaturization) 2514 drw 02

Figure 2. Fifteen-Hundred-Power Magnification Scanning Electron Microscope (SEM) Photos of the Four Generations of IDT's CEMOS Technology

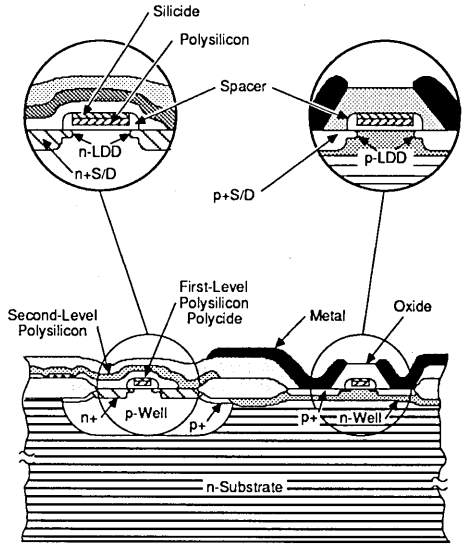


Figure 3. IDT CEMOS Device Cross Section

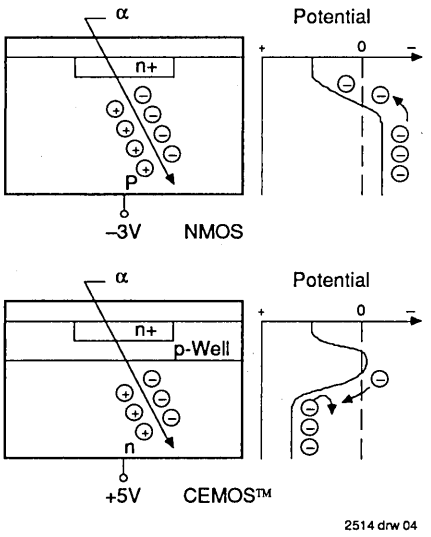


Figure 4. IDT CEMOS Built-In High Alpha Particle Immunity

ALPHA PARTICLES

Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Traveling with high energy levels, alpha particles penetrate deep into an integrated chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake.

The cause of alpha particles is well documented and understood in the industry. IDT has considered various techniques to protect the cells from this hazardous occurrence. These techniques include dual-well structures (Figures 3 and 4) and a polymeric compound for die coating. Presently, a polymeric compound is used in many of IDT's SRAMs; however, the specific techniques used may vary and change from one device generation to the next as the industry and IDT improve the alpha particle protection technology.

LATCHUP IMMUNITY

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes (Figure 5). The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than this.

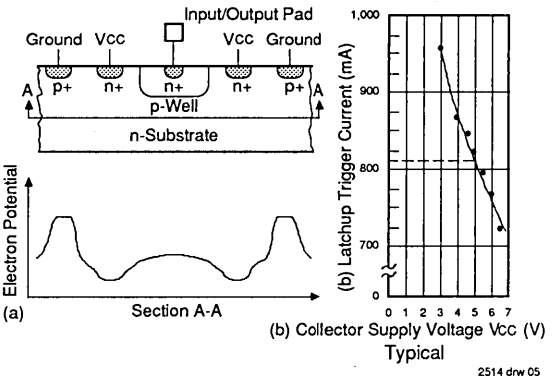


Figure 5. IDT CEMOS Latchup Suppression

SURFACE MOUNT TECHNOLOGY

To take full advantage of the low-power aspect of CMOS, and obtain two to three times the space savings, CMOS products should be used as SMDs (surface mount devices). However, most integrated circuits sold today are still packaged in the traditional DIP (dual in-line package) configuration because there is a tremendous support industry to handle thru-board assembly.

Determined to utilize CMOS advantages, IDT re-invented the DIP. This was accomplished by developing multilayered substrates (either co-fired ceramics or glass filled epoxy FR-4) with dual in-line (DIP) or single in-line (SIP) pins. An advanced IR (InfraRed) reflow and vapor phase reflow surface mount technology was also developed to produce the most reliable solder connections available.

Products that are to be interconnected to form larger electronic elements are electrically tested, environmentally screened, performance selected and then thermally matched to the appropriate ceramic or glass filled epoxy substrates. After modular assembly, the finished product is 100% re-tested to ensure that it completely performs to the specifications required.

As a result, IDT produces extraordinarily dense, high-speed combinations of monolithic ICs as complex subsystem modular assemblies. These modules convert SMDs to user-friendly DIPs/SIPs providing customers with the density advantages of surface mount in a format compatible with their extensive, thru-board, assembly expertise.

STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa, California — the heart of the "Silicon Valley." The company's operations are housed in seven facilities totaling over 500,000 square feet. These facilities house all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test and administration. In-house capabilities include scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), plastic and hermetic packaging, military and commercial testing, burn-in, life test and a full complement of environmental screening equipment.

The over-200,000-square-foot corporate headquarters campus is composed of four buildings. The largest facility on this site is a 100,000 square foot, two-building complex. The first building, a 60,000 square foot facility, is dedicated to the Complex Logic, Standard Logic and RISC Microprocessor product lines, as well as hermetic and plastic package assembly, logic products' test, burn-in, mark and QA, and a reliability/failure analysis lab.

IDT's Packaging and Assembly Process Development teams are located here. To keep pace with the development of new products and to enhance the IDT philosophy of "Innovation," these teams have ultra modern, integrated and correspondingly sophisticated equipment and environments at their disposal. All manufacturing is completed in dedicated clean room areas (Class 10K minimum), with all preseal operations accomplished under Class 100 laminar flow hoods.

Development of assembly materials, processes and equipment is accomplished under a fully operational production environment to ensure reliability and repeatable product. The Hermetic Manufacturing and Process Development team is currently producing custom products to the strict requirements of MIL-STD-883. The fully automated plastic facility is currently producing high volumes of USA-manufactured product, while developing state-of-the-art surface mount technology patterned after MIL-STD-883.

The second building of the complex houses sales, marketing, finance and MIS.

The RISC Subsystems and Subsystems Modules Divisions are located behind the two-building complex in a 54,000 square foot facility. Also located at this facility are Quality Assurance and wafer fabrication services.

Directly across the street from the two-building complex is a newly acquired 50,000 square foot facility that houses administrative services, Northwest Area Sales, Human Resources, International Planning and Shipping and Receiving functions.

IDT's largest and newest facility, opened in 1990 in San Jose, California, is a multi-purpose 150,000 square foot, ultra modern technology development center. This facility houses a 25,000 square foot, combined Class 1 (a maximum of one particle per cubic foot of 0.2 micron or larger), sub-half-micron R&D fabrication facility and a wafer fabrication area. This fab supports both production volumes of IDT products, including some next generation SRAMs, and the R&D efforts of the technology development staff. Technology development efforts targeted for the center include advanced silicon processing and wafer fabrication techniques. A test area to support both production and research is located on-site. The building is also the new home of the FIFO and ECL product lines.

IDT's second largest facility is located in Salinas, California, about an hour away from Santa Clara. This 95,000 square foot facility, located on 14 acres, is the Static RAM Division and Specialty Memory product line. Constructed in 1985, this facility houses an ultra-modern 25,000 square foot high-volume wafer fabrication area measured at Class 2-to-3 (a maximum of 2 to 3 particles per cubic foot of 0.2 micron or larger) clean room conditions. Careful design and construction of this fabrication area created a clean room environment far beyond the 1985 average for U.S. fab areas. This made possible the production of large volumes of high-density submicron geometry, fast static RAMs. This facility also houses shipping areas for IDT's leadership family of CMOS static RAMs. This site will expand to accommodate a 250,000 square foot complex.

To extend these philosophies while maintaining strict control of our processes, IDT has an operational Assembly and Test facility located in Penang, Malaysia. This facility assembles product to USA standards, with all assemblies done under laminar flow conditions (Class 100) until the silicon is encased in its final packaging. All products in this facility are manufactured to the quality control requirements of MIL-STD-883.

All of IDT's facilities are aimed at increasing our manufacturing productivity to supply ever larger volumes of high-performance, cost-effective leadership CMOS products.

SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing – as opposed to being "tested-in" later – in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-M-38510, as defined by Paragraph 1.2.1 of MIL-STD-883.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

QUALITY AND RELIABILITY

QSP–QUALITY, SERVICE AND PERFORMANCE

Quality from the beginning, is the foundation for IDT's commitment to supply consistently high-quality products to our customers. IDT's quality commitment is embodied in its all pervasive Constant Quality Improvement (CQI) program. Everyone who influences the quality of the product–from the designer to the shipping clerk–is committed to constantly improving the product quality.

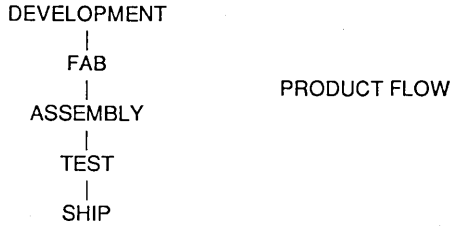
LOGIC PRODUCTS DIVISION'S FOCUS

"To make quantitative constant improvement in the quality of our actions that result in the supply of leadership products in conformance to the requirements of our customers."

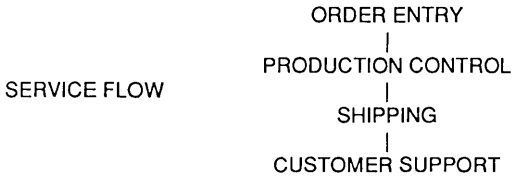
IDT's Logic Products Division has dedicated its efforts to constant quantitative improvements in quality. The result, a supply of leadership products that conform to the requirements of our customers.

LOGIC PRODUCTS DIVISION'S PRODUCT ASSURANCE STRATEGY FOR CQI

Measurable standards are essential to the success of CQI. All the processes contributing to the final quality of the product need to be monitored, measured and improved upon through the use of statistical tools.



Our customers receive the benefit of our optimized systems. Installed to enhance quality and reliability, these systems provide accurate and timely reporting on the effectiveness of manufacturing controls and the reliability and quality performance of IDT logic products and services.



These systems and controls concentrate on CQI by focusing on the following key elements:

Statistical Techniques
Using statistical techniques, including Statistical Process Control (SPC) to determine whether the product/ processes are under control.

Standardization
Implementing policies, procedures and measurement techniques that are common across different operational areas.

Documentation
Documenting and training in policies, procedures, measurement techniques and updating through characterization/ capability studies.

Productivity Improvement
Using constant improvement teams made up from employees at all levels of the organization.

Leadership
Focusing on quality as a key business parameter and strategic strength.

Total Employee Participation
Incorporating the CQI program into the IDT Corporate Culture.

Customer Service
Supporting the customer, as a partner, through performance review and pro-active problem solving.

People Excellence
Committing to growing, motivating and retaining people through training, goal setting, performance measurement and review.

PRODUCT FLOW

Product quality starts here. IDT has mechanisms and procedures in place that monitor and control the quality of our development activities. From the calibration of design capture libraries through process technology and product characterization that establish whether the performance, ratings and reliability criteria have been met. This includes failure analysis of parts that will improve the prototype product.

At the pre-production stage once again in-house qualification tests assure the quality and reliability of the product. All specifications and manufacturing flows are established and personnel trained before the product is placed into production.

Manufacturing

To make CQI during the manufacturing stage, control items are determined for major manufacturing conditions. Data is gathered and statistical techniques are used to control specific manufacturing processes that affect the quality of the product.

In-process and final inspections are fed back to earlier processes to improve product quality. All product is burned-in (where applicable) before 100% inspection of electrical characteristics takes place.

Products which pass final inspection are then subject to Quality Assurance and Reliability Tests. This data is used to improve manufacturing processes and provide reliability predictions of field applications.

Inventory and Shipping

Controls in shipping focus on ensuring parts are identified and packaged correctly. Care is also taken to see that the correct paperwork is present and the product being shipped was processed correctly.

SERVICE FLOW

Quality not only applies to the product but to the quality -of -service we give our customers. Services is also constantly improved.

Order Procedures

Checks are made at the order entry stage to ensure the correct processing of the Customer's product. After verification and data entry the Acknowledgements (sent to Customers) are again checked to ensure details are correct. As part of the CQI program, the results of these verifications are analyzed using statistical techniques and corrective actions are taken.

Production Control

Production Control (P.C.) is responsible for the flow and logistics of material as it moves through the manufacturing processes. The quality of the actions taken by P.C. greatly impinges on the quality of service the customer receives. Because many of our customers have implemented Just-in-Time (JIT) manufacturing practices, IDT as a supplier also has to adopt these same disciplines. As a result, employees receive extensive training and the performance level of key actions are kept under constant review. These key actions include:

Quotation response and accuracy.
Scheduling response and accuracy.
Response and accuracy of Expedites.
Inventory, management, and effectiveness.
On time delivery.

Customer Support

IDT has a worldwide network of sales offices and Technical Development Centers. These provide local customer support on business transactions, and in addition, support customers on applications information, technical services, benchmarking of hardware solutions, and demonstration of various Development Workstations.

The key to CQI is the timely resolution of defects and implementation of the corrective actions. This is no more important than when product failures are found by a customer. When failures are found at the customer's incoming inspection, in the production line, or the field application, the Logic Products Division Quality Assurance group is the focal point for the investigation of the cause of failure and implementation of the corrective action. IDT constantly improves the level of support we give our customers by monitoring the response time to customers that have detected a product failure. Providing the customer with an analysis of the failure, including corrective actions and the statistical analysis of defects, brings CQI full circle–full support of our customers and their designs with high-quality products.

SUMMARY

In 1990, IDT made the commitment to *"Leadership through Quality, Service, and Performance Products"*.

We believe by following that credo IDT and our cusotmers will be successful in the coming decade. With the implementation of the CQI strategy within the Logic Products Division, we will satisfy our goal...

"Leadership through Quality, Service and Performance Products".

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic and modular assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-38510 as defined by paragraph 1.2.1 of MIL-STD-883 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

Monolithic Hermetic Package Processing Flow[1]

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die-Sort Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT-defined internal criteria.

3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.

6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.

7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.

8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in as applicable to the same conditions as Military Grade devices.

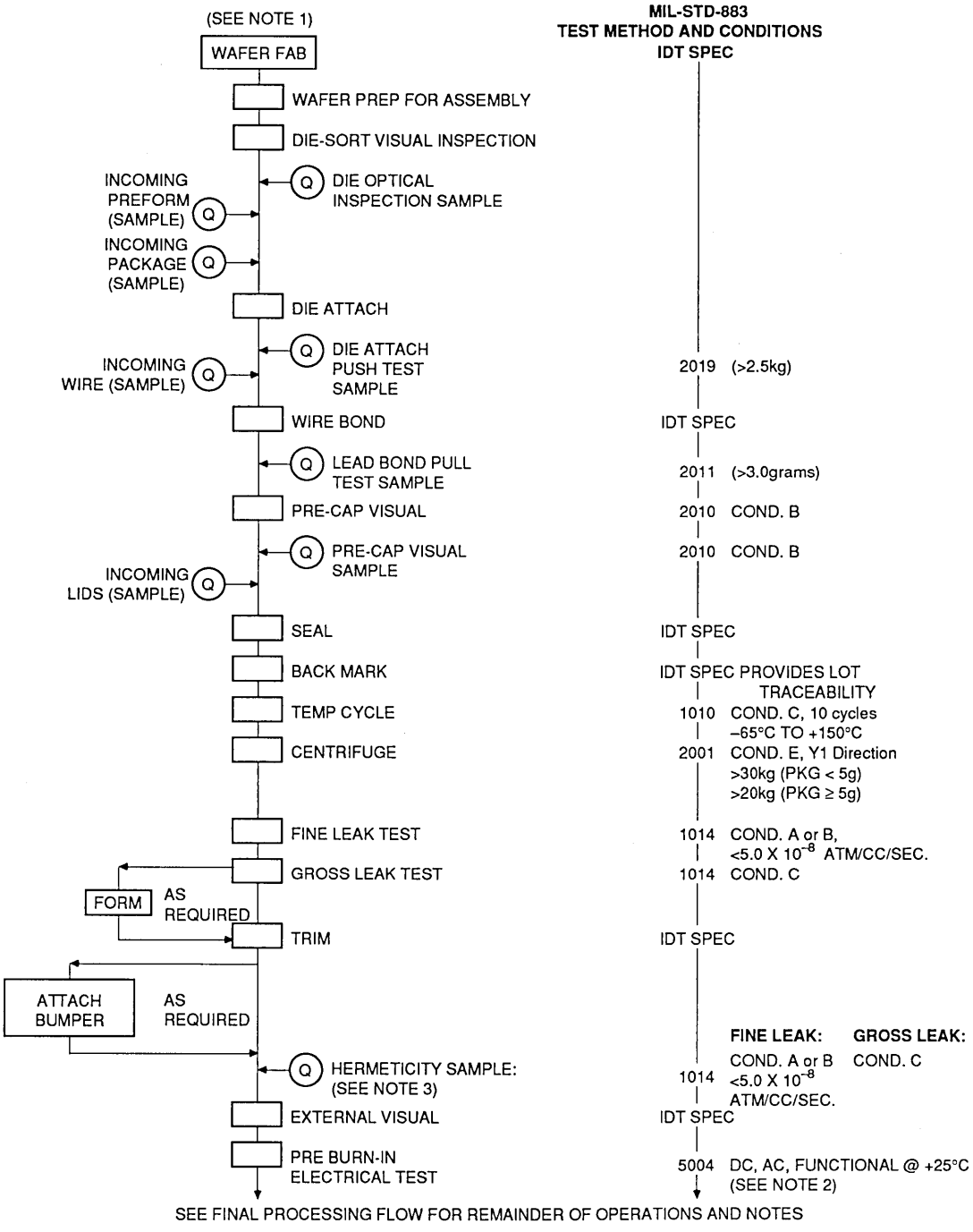
10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the –55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.

11. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.

12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

NOTE:
1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

Monolithic Hermetic Package Processing Flow



2502 drw 01

SUMMARY

Monolithic Plastic Package Processing Flow

Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is all applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die-Sort Visual Inspection:** Wafers are 100% visually inspected to strict IDT defined internal criteria.

3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests.

4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull tests to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the package is molded, 100% of the product is visually inspected to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure:** Plastic encapsulated devices are baked to ensure an optimum plastic seal so as to enhance moisture barrier characteristics.

7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

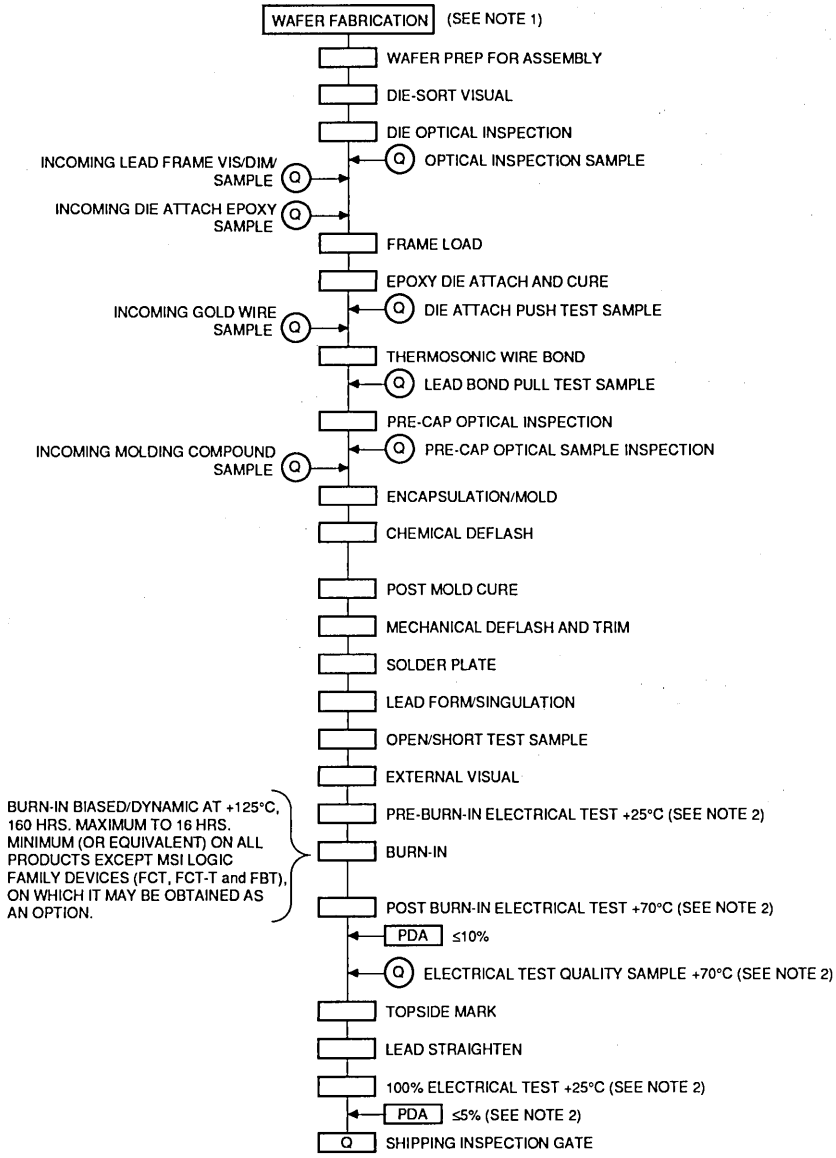
8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in 16 hours at +125°C (or equivalent), utilizing the same burn-in conditions as the Military Grade product.

9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.

10. **Mark:** All product is marked with product type and lot code identifiers.

11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to the 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated, the test methods are patterned after MIL-STD-883 criteria.

Monolithic Plastic Package Processing Flow



NOTE:
1. All screens are 100% unless otherwise noted.
2. All electrical test programs are per the applicable IDT test specification.
3. IDT performs a 100% electrical test at +25°C with a 5% PDA limit at this point.
4. (Q) = Quality sample inspection.

2502 drw 02

Monolithic Hermetic Package Final Processing Flow

Operation	MIL-STD-883 Test Method	Military Compliant Class B	Commercial	
			Military Temp. Range	Commercial Temp. Range
Burn-In	1015/D at +125°C Min. or Equivalent	100% 160 Hours	100% 16 to 160 Hours	100% 16to160 Hours
Post Burn-In Electrical: Static (DC), Functional and Switching (AC)[2]	IDT Spec.	100% +25, -55 and +125°C	100% +125°C	100% +70°C
Percent Defective Allowed (PDA)[4]	5004 or IDT Spec.	5%	10%	10%
Group A Electrical: Static (DC), Functional and Switching (AC)[2]	5005 and IDT Spec.	Sample -55 and +125°C	Sample +125°C	Sample +70°C
Mark/Lead Straighten	IDT Spec.	100%	100%	100%
+25°C Electrical[2]	IDT Spec.	100%[5]	100%	100%
Final Visual/Pack	IDT Spec.	100%	100%	100%
Quality Conformance Inspection	5005 (Group B, C, D)	Yes	—	—
Quality Shipping Inspection (Visual/Plant Clearance)	IDT Spec.	Sample	Sample	Sample

2505 tbl 01

NOTES:
1. All screens are 100% unless otherwise noted.
2. All electrical test programs are per the applicable IDT test specification.
3. This hermeticity sample is performed after all lead finish operations.
4. If a lot fails the 5% PDA but is ≤10%, the lot may be resubmitted to burn-in one time only to the same time and temperature conditions as first submission. The subsequent post burn-in electrical test at +25°C will be performed to a PDA of 3%.
5. IDT performs a 100% electrical test at +25°C with a 2% PDA limit at this point to satisfy group A requirements, and considers this to be equivalent to the group A requirement of an LTPD of 2, with an accept number of 0. If a lot fails the 2% PDA limit, it may be rescreened one time only to a tightened PDA limit of 1.5%.
6. (Q) = Quality sample inspection.

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The low power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS (SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by the devices in the system due to a pulse event, and is measured in RADS (SI) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is either created through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

Radiation Category	Primary Particle	Source	Effect
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

2510 drw 01

Figure 1.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as Error Detection and Correction (EDC) circuitry, since the occurrence of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes, IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

RADIATION HARDNESS CATEGORIES

Radiation Enhanced ('RE) or Radiation Tolerant ('RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level via ARACOR X-Ray radiation. This Total Dose Test plan qualifies each 'RE or 'RT wafer to a Total Dose level. Only wafers with sampled die that pass Total Dose level tests are assembled and used for orders (consult factory for more details on Total Dose sample testing). With regard to Total Dose testing, clarifications/exceptions to MIL-STD-883, Methods 5005 and 1019 are required. Consult factory for more details.

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance or radiation "hardness".

- Radiation Enhanced process uses Epi wafers and is able to provide Logic devices that can be Total Dose qualified to 10K RADs (Si) or greater by IDT's ARACOR X-Ray Total Dose sample die test plan (Total Dose levels require negotiation, consult factory for more details).
- Radiation Tolerant Logic product uses standard wafer/ process material that is qualified to 10K RADs (Si) Total Dose by IDT's ARACOR X-Ray Total Dose sample die test plan.

Integrated Device Technology can provide Radiation Tolerant/Enhanced versions of all Logic product types (some speed grades may not be available as 'RE).

Please contact your IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications.Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

PACKAGE DIAGRAM OUTLINES

THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CEMOS™ process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (T_J), it becomes increasingly important to maintain a low (T_J).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_O \exp \left[\frac{Ea}{k} \left(\frac{1}{T_O} - \frac{1}{T_J} \right) \right]$$

where

- t_A = lifetime at elevated junction (T_J) temperature
- t_O = normal lifetime at normal junction (T_O) temperature
- Ea = activation energy (ev)
- k = Boltzmann's constant (8.617×10^{-5}ev/k)

i.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CEMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.
4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883 to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelop (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package cavity size and die attach integrity. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (T_J), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degree celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

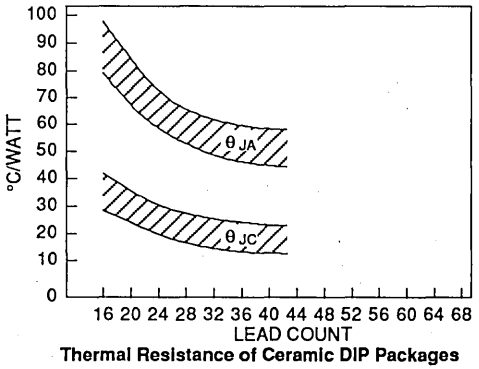
$$\theta_{JA} = [T_J - T_A]/P$$
$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

where

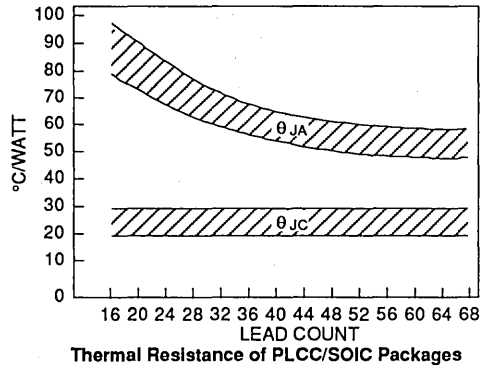
$$\frac{\theta_{JC} = T_J - T_C}{P} \qquad \frac{\theta_{CA} = T_C - T_A}{P}$$

- θ = Thermal resistance
- J = Junction
- P = Operational power of device (dissipated)
- T_A = Ambient temperature in degree celsius
- T_J = Temperature of the junction
- T_C = Temperature of case/package
- θ_{CA} = Case to Ambient, thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
- θ_{JC} = Junction to Case, thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on the package material properties and package geometry.)
- θ_{JA} = Junction to Ambient, thermal resistance—usually measured with respect to the temperature of a specified volume of still air. (Dependent on θ_{JC} + θ_{JA} which includes the influence of area and environmental condition.)

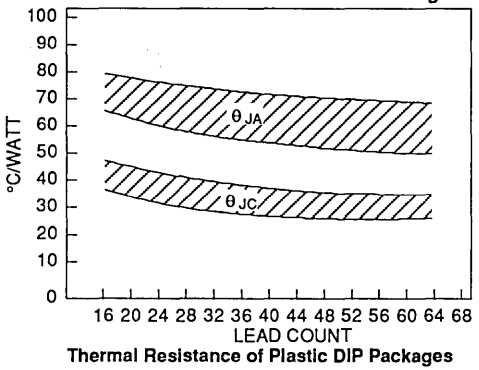
Ref. MIL-STD-883C, Method 1012.1
JEDEC ENG. Bulletin No. 20, January 1975
1986 Semi. Std., Vol. 4, Test Methods G30–86, G32–86.



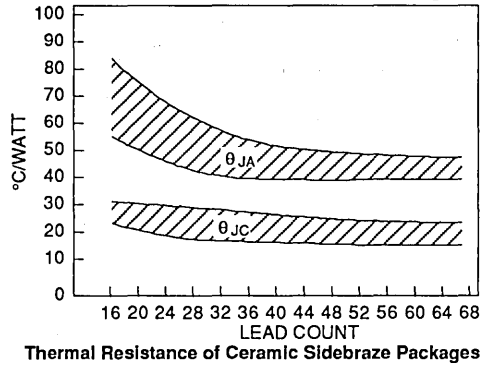
Thermal Resistance of Ceramic DIP Packages



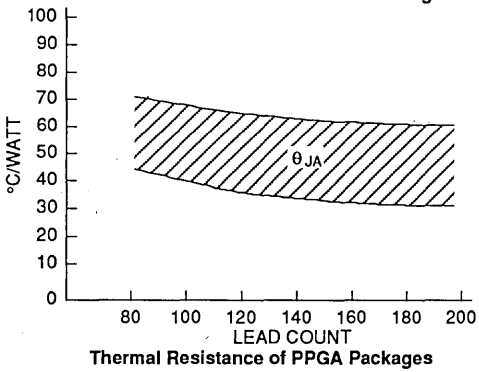
Thermal Resistance of PLCC/SOIC Packages



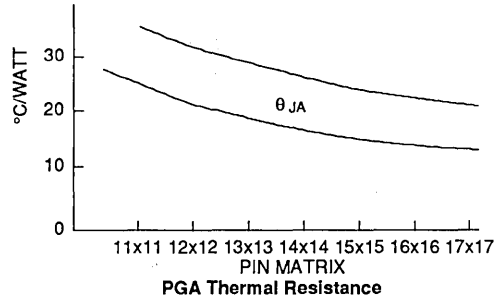
Thermal Resistance of Plastic DIP Packages



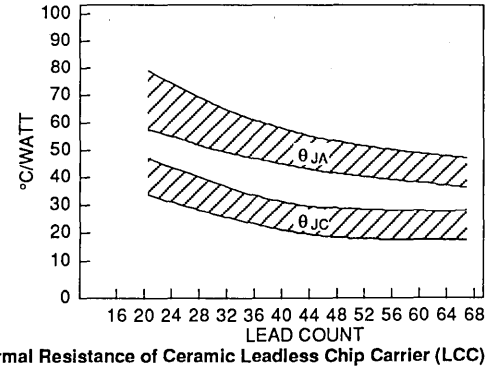
Thermal Resistance of Ceramic Sidebraze Packages



Thermal Resistance of PPGA Packages



PGA Thermal Resistance



Thermal Resistance of Ceramic Leadless Chip Carrier (LCC) Packages

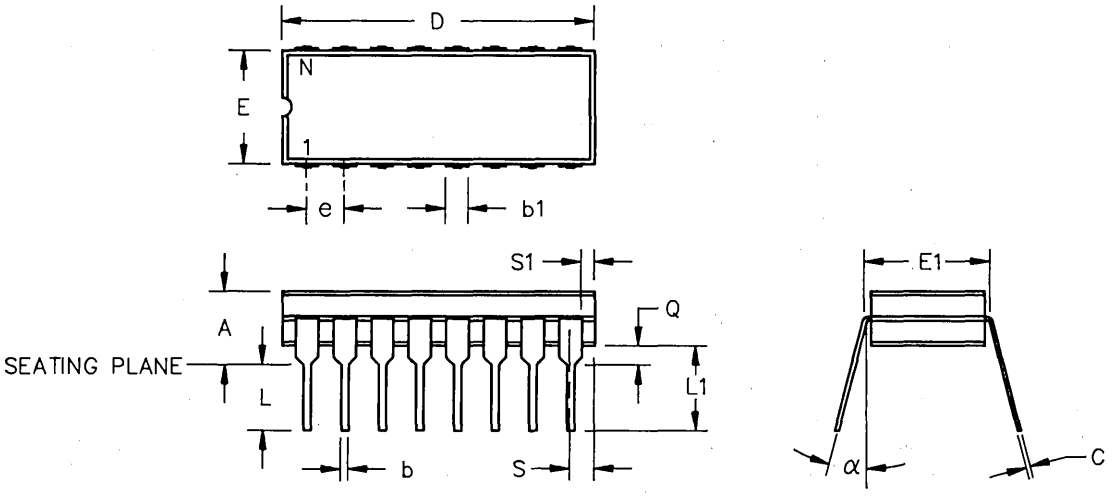
2512 drw 01

PACKAGE DIAGRAM OUTLINE INDEX

Integrated Device Technology, Inc.

PACKAGE DIAGRAM OUTLINES

DUAL IN–LINE PACKAGES



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. THE MINIMUM LIMIT FOR DIMENSION b1 MAY BE .023 FOR CORNER LEADS.

16–28 LEAD CERDIP (300 MIL)

DWG #	D16–1		D18–1		D20–1		D22–1		D24–1		D28–3	
# OF LDS (N)	16		18		20		22		24		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.105	.175	.105	.175	.105	.175	.105	.175	.105	.175	.105	.175
b	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021
b1	.038	.060	.038	.060	.038	.060	.038	.060	.045	.065	.045	.065
C	.009	.012	.009	.012	.009	.012	.009	.012	.009	.014	.009	.014
D	.750	.830	.880	.930	.935	1.060	1.050	1.080	1.240	1.280	1.440	1.490
E	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320	.300	.320	.300	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.025	.055	.025	.055	.025	.060	.015	.060	.015	.060	.015	.060
S	.045	.080	.045	.080	.045	.080	.020	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

24-40 LEAD CERDIP (600 MIL)

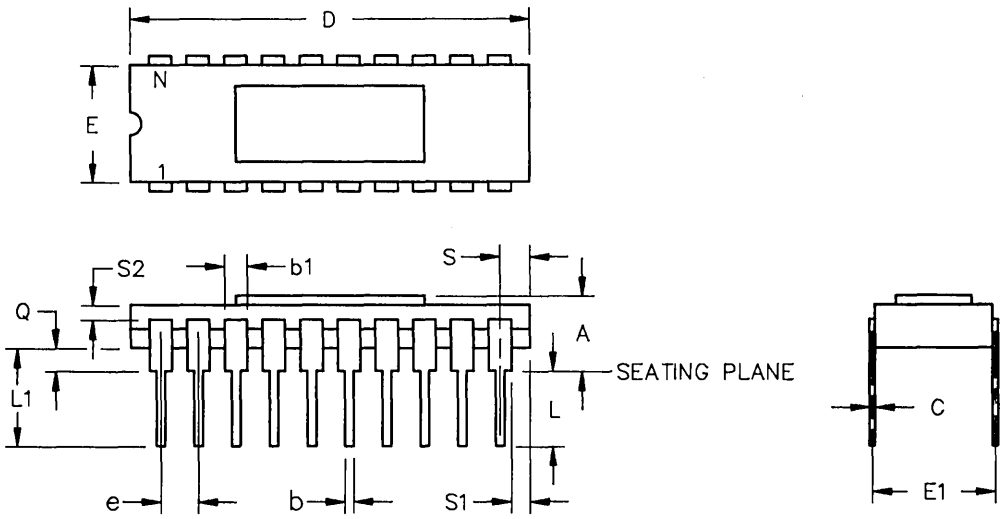
DWG #	D24-2		D28-1		D40-1	
# OF LDS (N)	24		28		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.190	.090	.200	.160	.220
b	.014	.023	.014	.023	.014	.023
b1	.038	.060	.038	.065	.038	.065
C	.008	.012	.008	.014	.008	.014
D	1.230	1.290	1.440	1.490	2.020	2.070
E	.500	.610	.510	.545	.510	.545
E1	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–
Q	.015	.060	.020	.060	.020	.060
S	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°

28-40 LEAD CERDIP (WIDE BODY)

DWG #	D28-2		D32-1		D40-2	
# OF LDS (N)	28		32		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.120	.210	.160	.220
b	.014	.023	.014	.023	.014	.023
b1	.038	.065	.038	.065	.038	.065
C	.008	.014	.008	.014	.008	.014
D	1.440	1.490	1.625	1.675	2.020	2.070
E	.570	.600	.570	.600	.570	.600
E1	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–
Q	.020	.060	.020	.060	.020	.060
S	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

20-32 LEAD SIDE BRAZE (300 MIL)

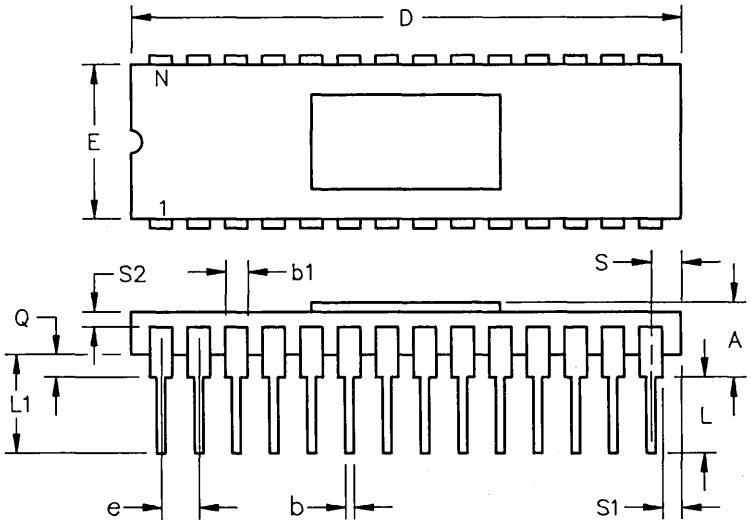


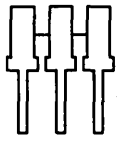
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C20-1		C22-1		C24-1		C28-1		C32-3	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.100	.200	.090	.200	.090	.200	.090	.200
b	.014	.023	.014	.023	.015	.023	.014	.023	.014	.023
b1	.040	.060	.040	.060	.040	.060	.040	.060	.040	.060
C	.008	.015	.008	.015	.008	.015	.008	.015	.008	.014
D	.970	1.060	1.040	1.120	1.180	1.230	1.380	1.420	1.580	1.640
E	.220	.310	.260	.310	.220	.310	.220	.310	.280	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200	.125	.200	.100	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.015	.060	.015	.060	.030	.060
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–

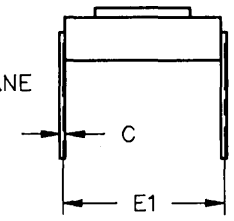
DUAL IN-LINE PACKAGES (Continued)

28-48 LEAD SIDE BRAZE (400 MIL)





48 LEAD OPTION

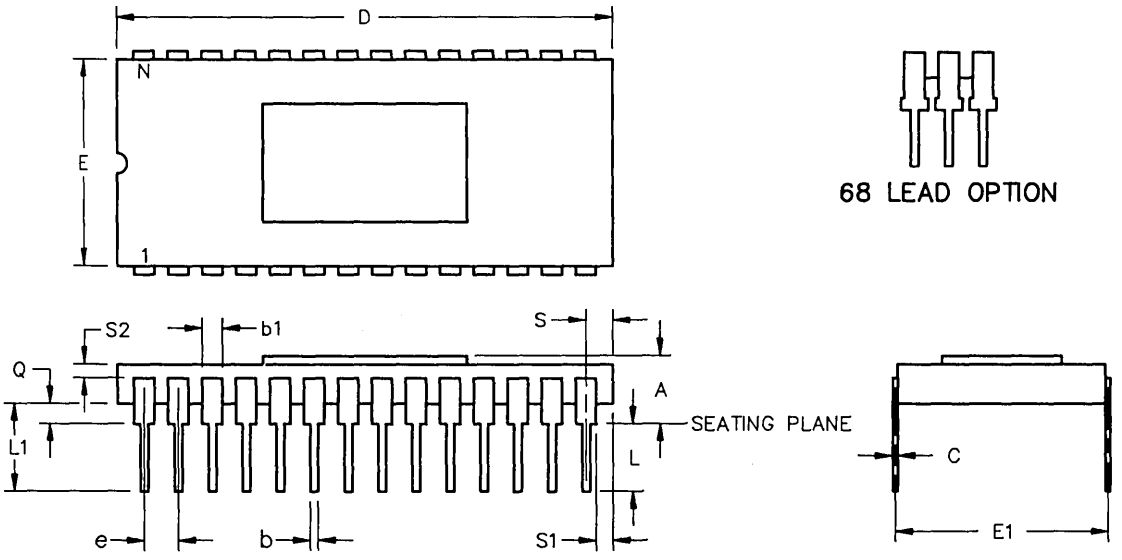


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C28-2		C32-2		C48-1	
# OF LDS (N)	28		32		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.090	.200	.085	.190
b	.014	.023	.014	.023	.014	.023
b1	.040	.060	.040	.060	.040	.060
C	.008	.014	.008	.014	.008	.014
D	1.380	1.420	1.580	1.640	1.690	1.730
E	.380	.420	.380	.410	.380	.410
E1	.390	.420	.390	.420	.390	.420
e	.100 BSC		.100 BSC		.070 BSC	
L	.100	.175	.100	.175	.125	.175
L1	.150	–	.150	–	.150	–
Q	.030	.060	.030	.060	.020	.070
S	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

24-68 LEAD SIDE BRAZE (600 MIL)

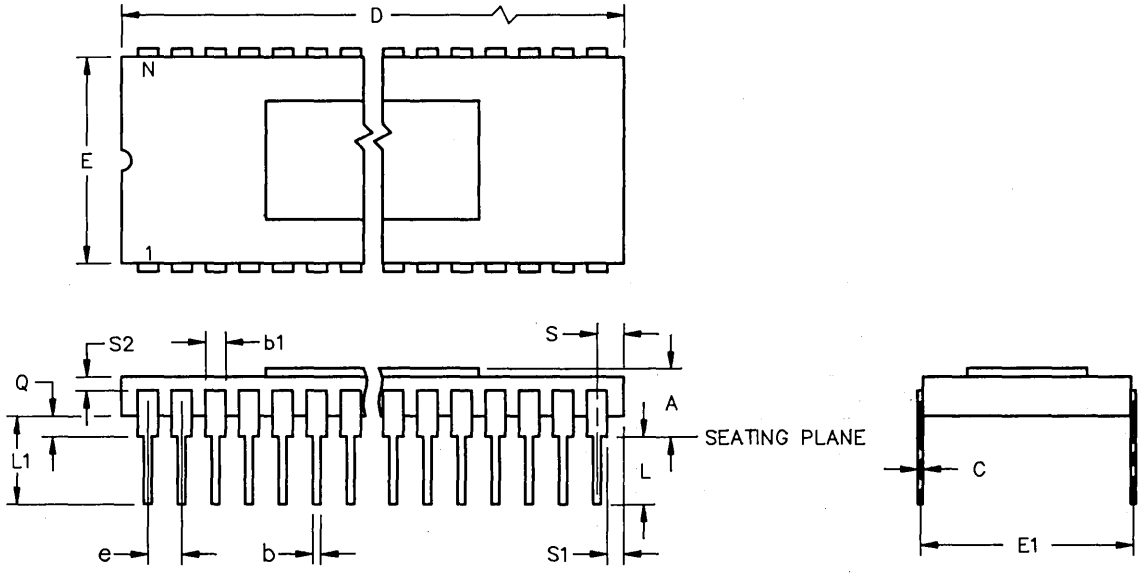


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C24-2		C28-3		C32-1		C40-1		C48-2		C68-1	
# OF LDS (N)	24		28		32		40		48		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.190	.085	.190	.100	.190	.085	.190	.100	.190	.085	.190
b	.015	.023	.015	.022	.015	.023	.015	.023	.015	.023	.015	.023
b1	.040	.060	.038	.060	.040	.060	.038	.060	.040	.060	.040	.060
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.180	1.220	1.380	1.430	1.580	1.640	1.980	2.030	2.370	2.430	2.380	2.440
E	.575	.610	.580	.610	.580	.610	.580	.610	.550	.610	.580	.610
E1	.595	.620	.595	.620	.590	.620	.595	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.070 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.020	.060	.020	.065	.020	.060	.020	.060	.020	.060	.020	.070
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.010	–	.010	–	.005	–	.010	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

64 LEAD SIDE BRAZE (900 MIL)

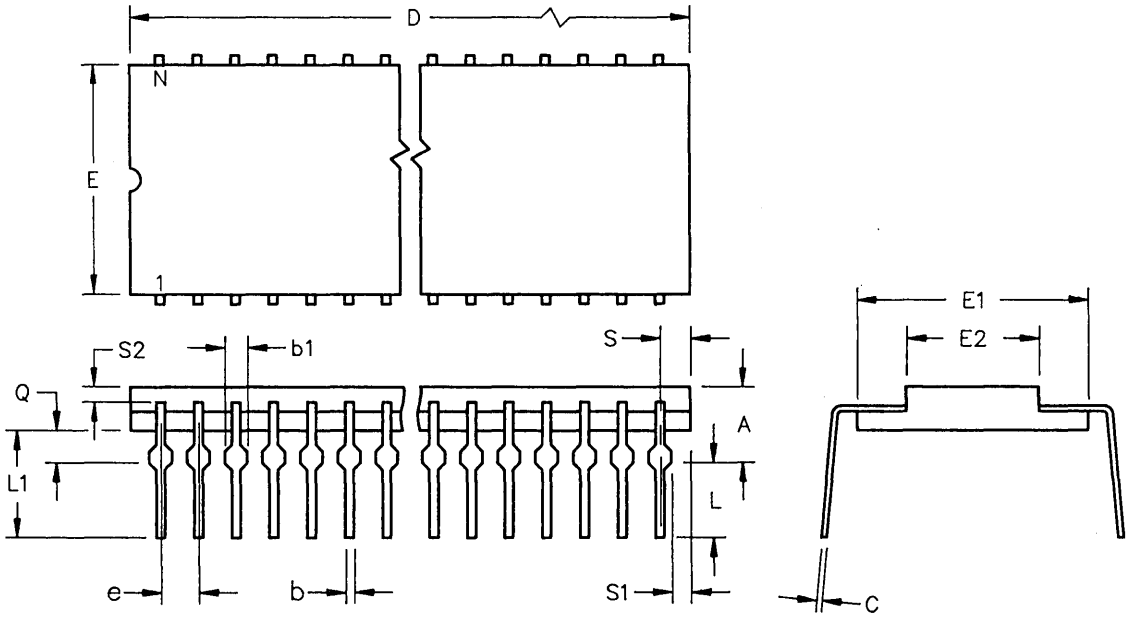


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C64-1	
# OF LDS (N)	64	
SYMBOL	MIN	MAX
A	.110	.190
b	.014	.023
b1	.040	.060
C	.008	.015
D	3.160	3.240
E	.884	.915
E1	.890	.920
e	.100 BSC	
L	.125	.200
L1	.150	–
Q	.015	.070
S	.030	.065
S1	.005	–
S2	.005	–

DUAL IN-LINE PACKAGES (Continued)

64 LEAD TOP BRAZE (900 MIL)

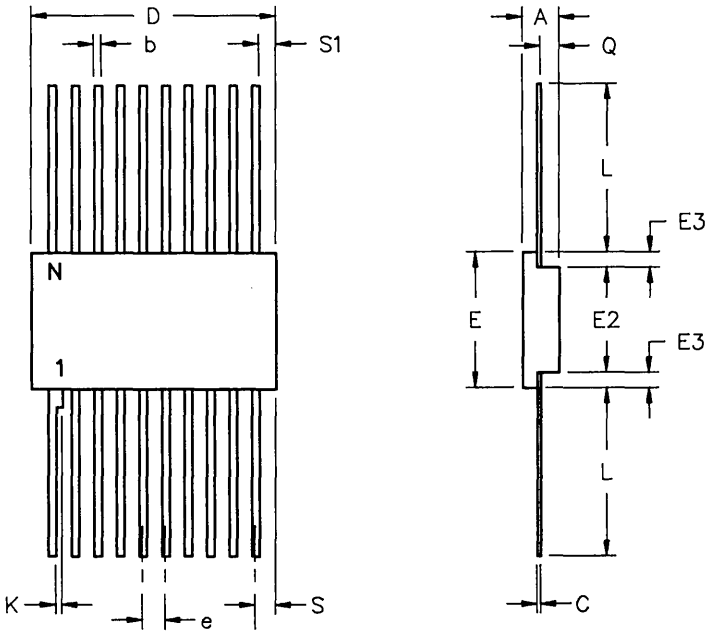


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C64-2	
# OF LDS (N)	64	
SYMBOL	MIN	MAX
A	.120	.180
b	.015	.021
b1	.040	.060
C	.009	.012
D	3.170	3.240
E	.790	.810
E1	.880	.815
E2	.640	.660
e	.100 BSC	
L	.125	.160
L1	.150	–
Q	.020	.100
S	.030	.065
S1	.005	–
S2	.005	–

FLATPACKS

20–28 LEAD FLATPACK

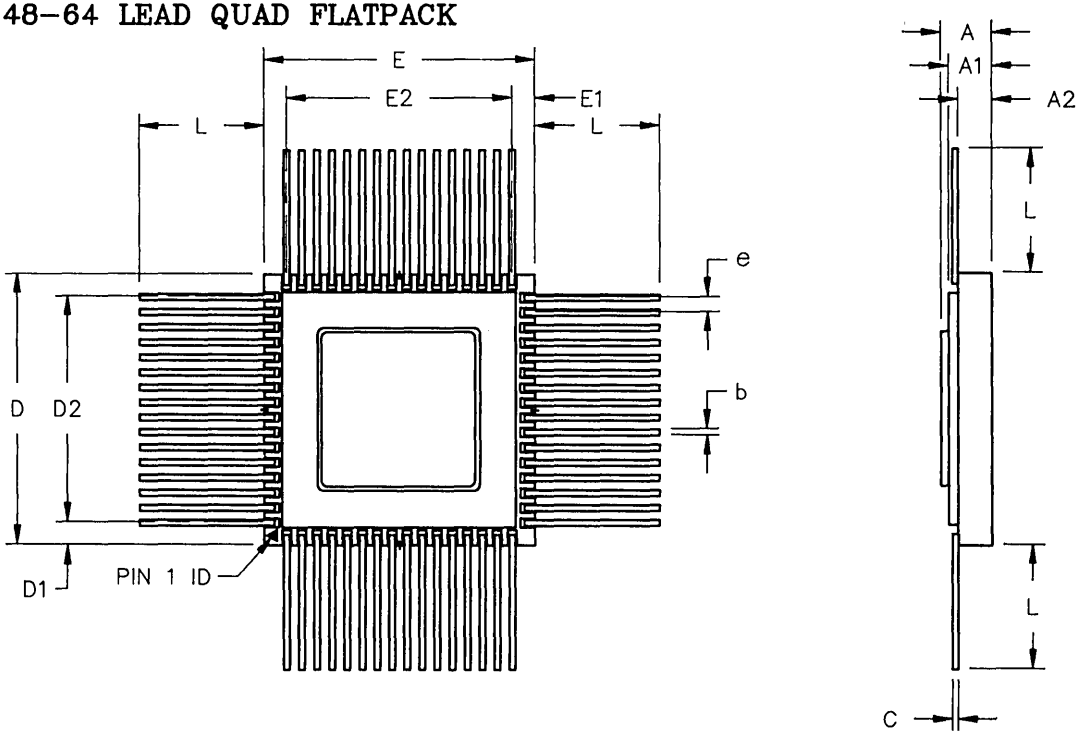


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F20–1		F20–2		F24–1		F28–1		F28–2	
# OF LDS (N)	20		20 (.295 BODY)		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.045	.092	.045	.092	.045	.090	.045	.090	.045	.115
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.003	.006	.003	.006	.003	.006	.004	.007	.003	.007
D	–	.540	–	.540	–	.640	.710	.740	.710	.740
E	.340	.360	.245	.303	.360	.420	.480	.520	.460	.520
E2	.130	–	.130	–	.180	–	.180	–	.180	–
E3	.030	–	.030	–	.030	–	.040	–	.040	–
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.010	.040	.010	.040	.010	.040	.010	.045	.010	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–	.005	–	.005	–

FLATPACKS (Continued)

48–64 LEAD QUAD FLATPACK

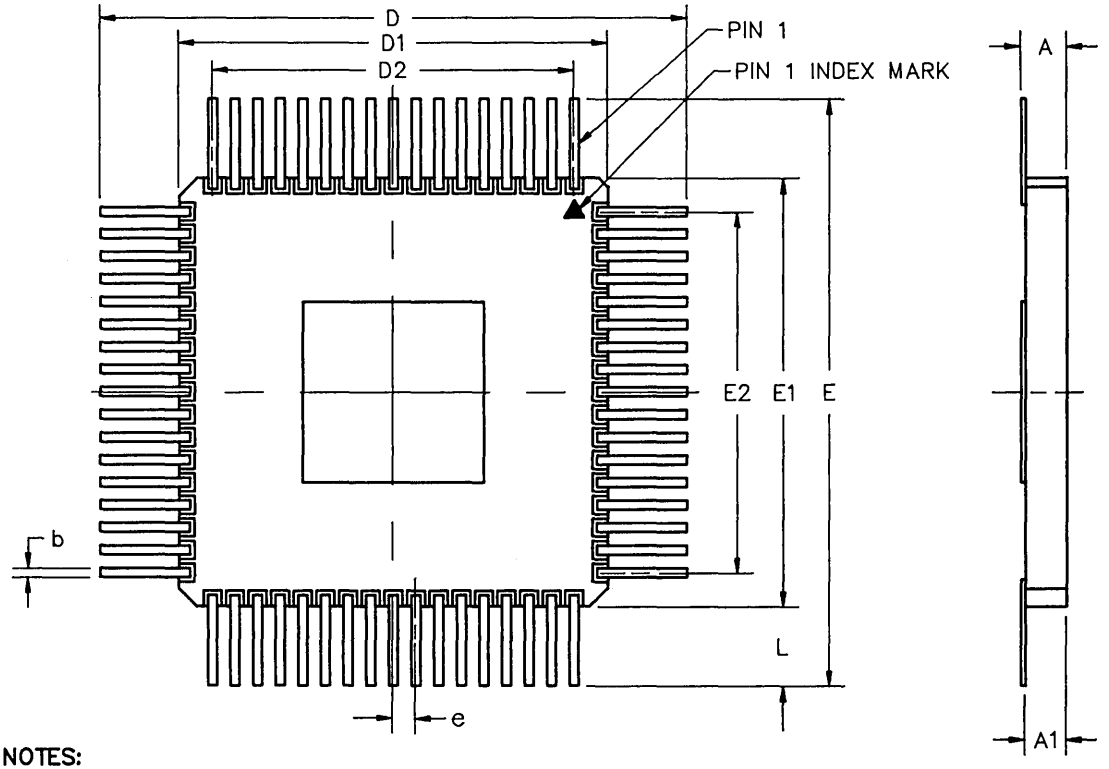


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F48–1		F64–1	
# OF LDS (N)	48		64	
SYMBOL	MIN	MAX	MIN	MAX
A	.089	.108	.070	.090
A1	.079	.096	.060	.078
A2	.058	.073	.030	.045
b	.018	.022	.016	.020
C	.008	.010	.009	.012
D/E	–	.750	.885	.915
D1/E1	.100 REF		.075 REF	
D2/E2	.550 BSC		.750 BSC	
e	.050 BSC		.050 BSC	
L	.350	.450	.350	.450
ND/NE	12		16	

FLATPACKS (Continued)

68 LEAD QUAD FLATPACK

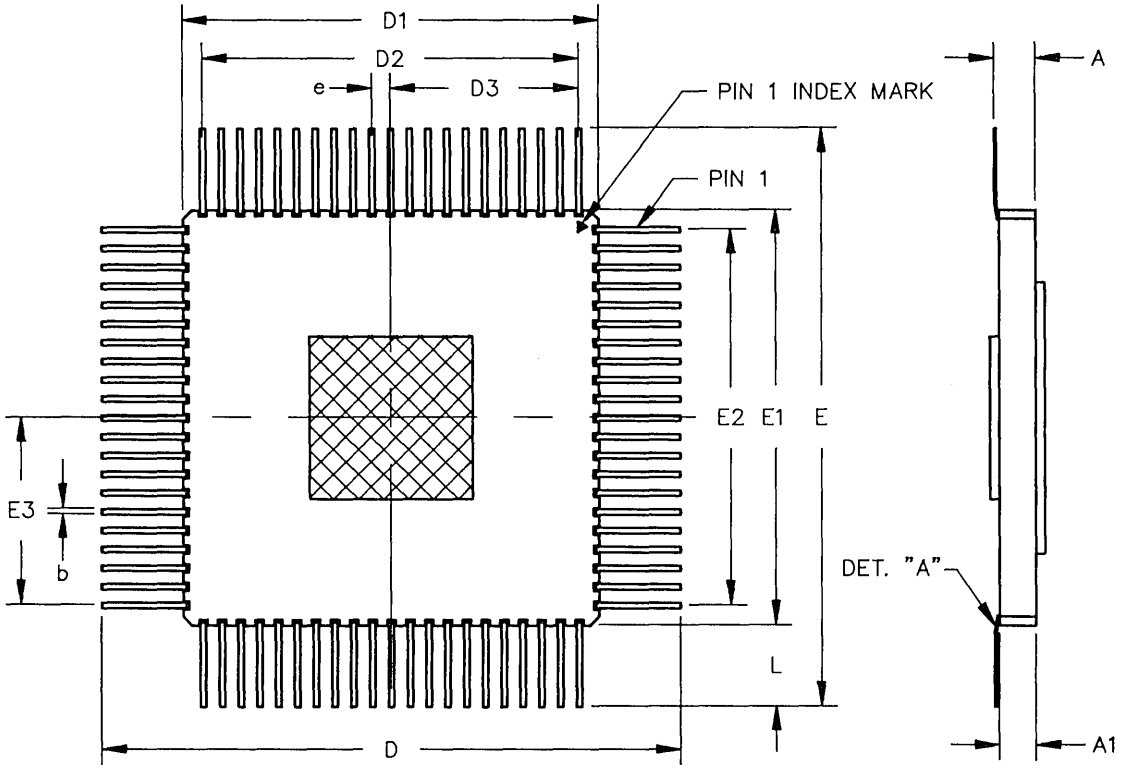


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F68–1	
# OF LDS (N)	68	
SYMBOL	MIN	MAX
A	.080	.145
A1	.070	.090
b	.014	.021
C	.008	.012
D/E	1.640	1.870
D1/E1	.926	.970
D2/E2	.800 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	17	

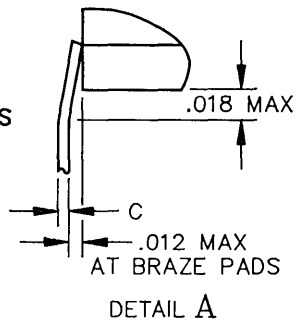
FLATPACKS (Continued)

84 LEAD QUAD FLATPACK (CAVITY DOWN)



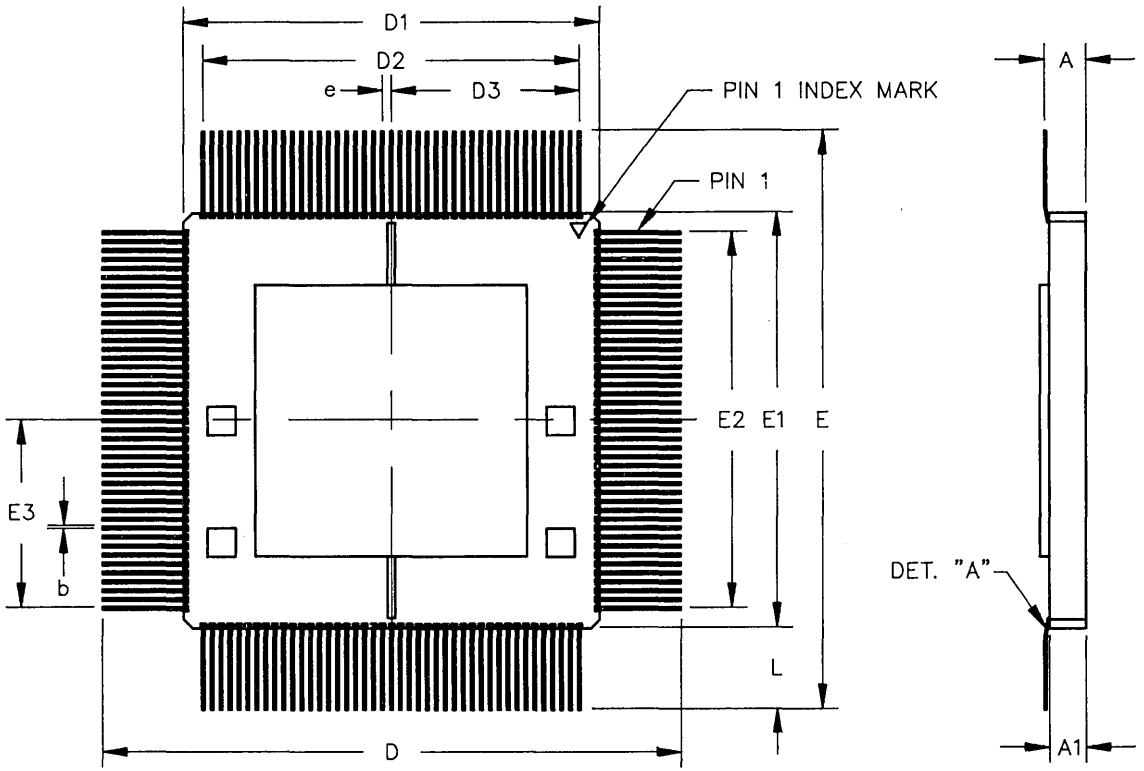
DWG #	F84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	–	.140
A1	–	.105
b	.014	.020
C	.007	.013
D/E	1.485	1.615
D1/E1	1.130	1.170
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	21	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.



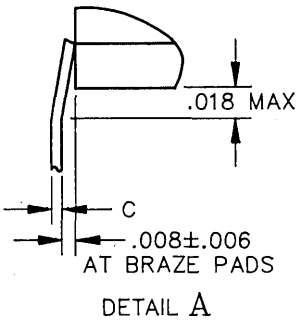
FLATPACKS (Continued)

172 LEAD QUAD FLATPACK (MIPS)



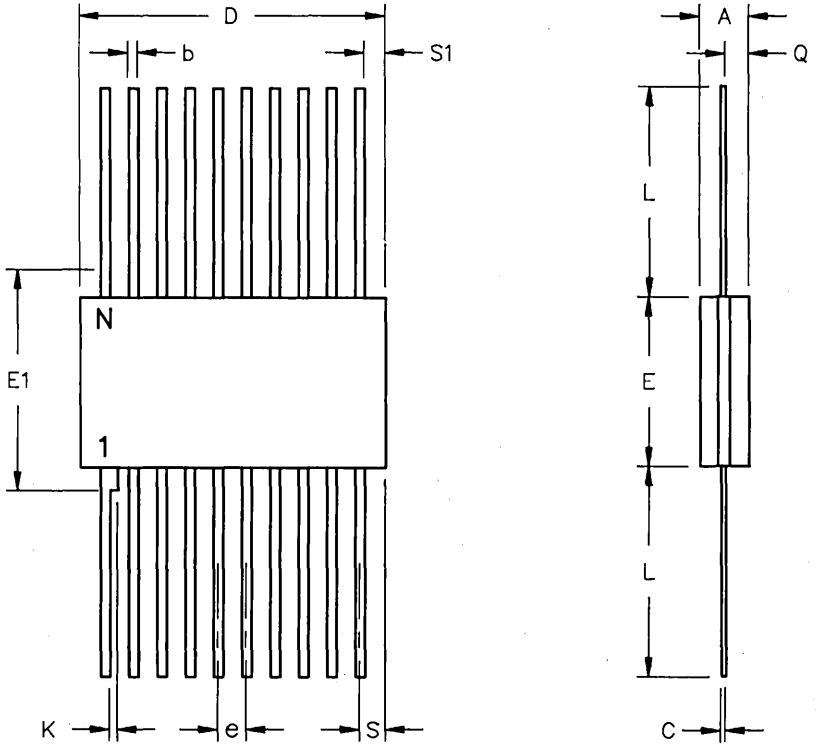
DWG #	F172-1	
# OF LDS (N)	172	
SYMBOL	MIN	MAX
A	–	.130
A1	–	.105
b	.006	.010
C	.004	.008
D/E	1.580	1.620
D1/E1	1.135	1.165
D2/E2	1.050 BSC	
D3/E3	.525 BSC	
e	.025 BSC	
L	.220	.230
ND/NE	43	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.



CERPACKS

16–28 LEAD CERPACK

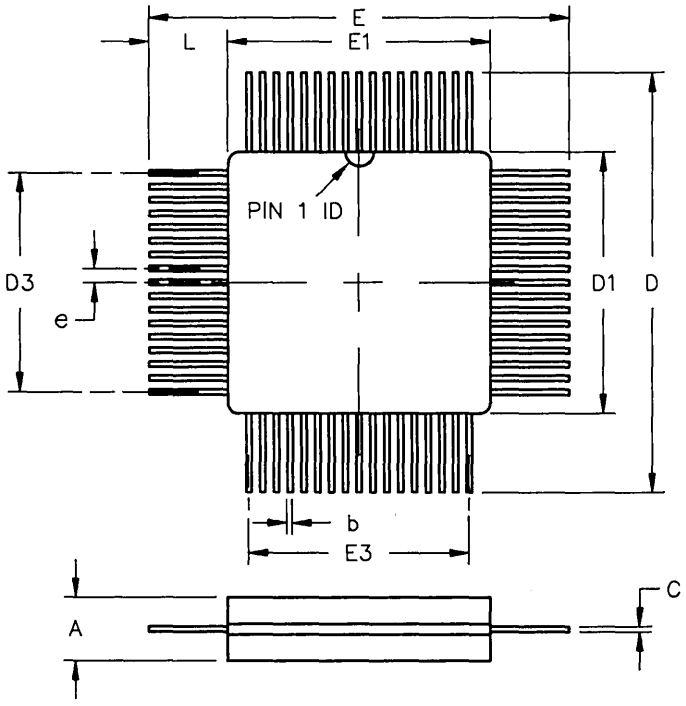


NOTES:
1. ALL DIMENSION ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	E16–1		E20–1		E24–1		E28–1		E28–2	
# OF LDS (N)	16		20		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.085	.045	.092	.045	.090	.045	.115	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.0045	.006	.0045	.006	.0045	.006	.0045	.009	.0045	.006
D	.370	.430	–	.540	–	.640	–	.740	–	.740
E	.245	.285	.245	.300	.300	.420	.460	.520	.340	.380
E1	–	.305	–	.305	–	.440	–	.550	–	.400
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.026	.040	.026	.040	.026	.040	.026	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–	.005	–	.005	–

CERQUADS

68 LEAD CERQUAD (STRAIGHT LEADS)

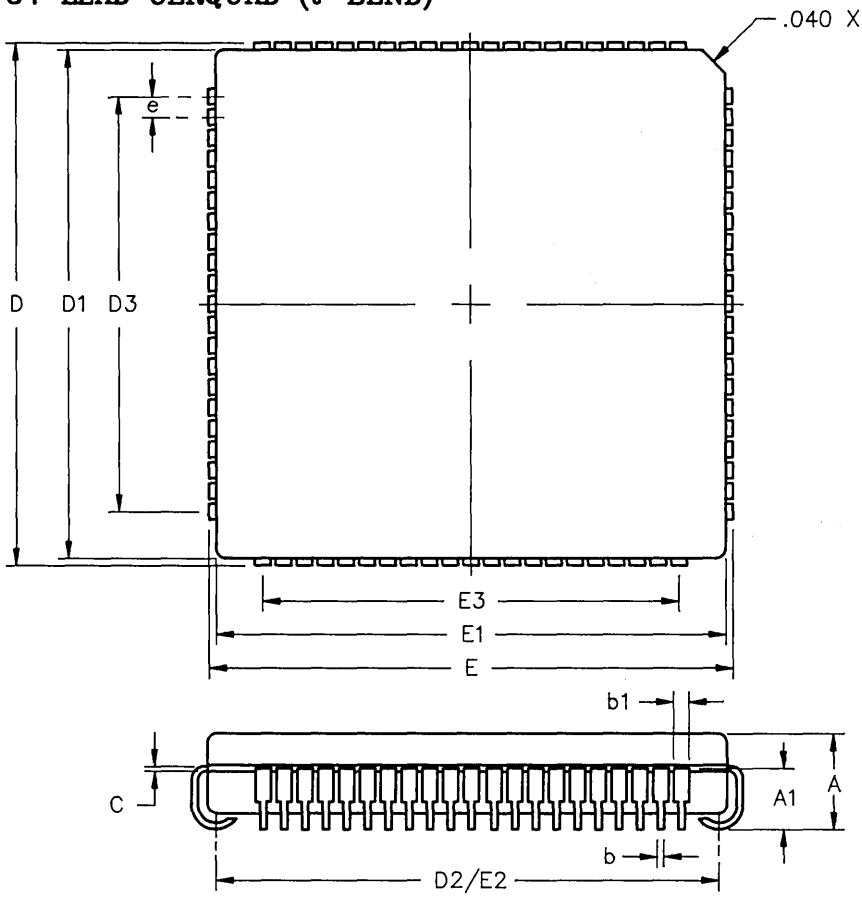


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	CQ68-1	
# OF LDS (N)	68	
SYMBOL	MIN	MAX
A	.115	.165
b	.008	.013
C	.0045	.008
D/E	.860	1.100
D1/E1	.460	.500
D3/E3	.400 REF	
e	.025 BSC	
L	.200	.300
ND/NE	17	

CERQUADS (Continued)

84 LEAD CERQUAD (J-BEND)

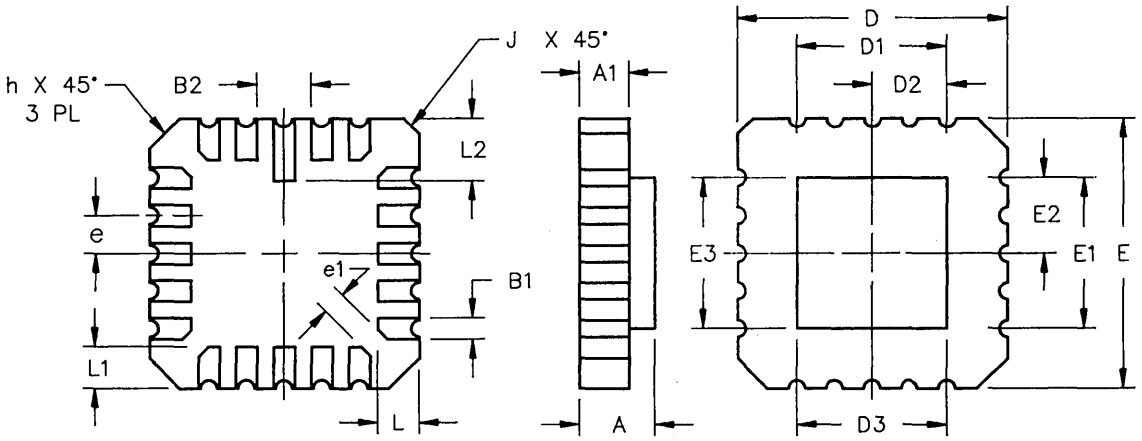


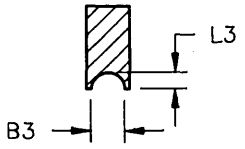
DWG #	CQ84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	.155	.200
A1	.090	.120
b1	.022	.032
b	.013	.023
C	.006	.013
D/E	1.170	1.190
D1/E1	1.138	1.162
D2/E2	1.100	.1.150
D3/.E3	1.000 BSC	
e	.050 BSC	
ND/NE	21	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

LEADLESS CHIP CARRIERS





NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–48 LEAD LCC (SQUARE)

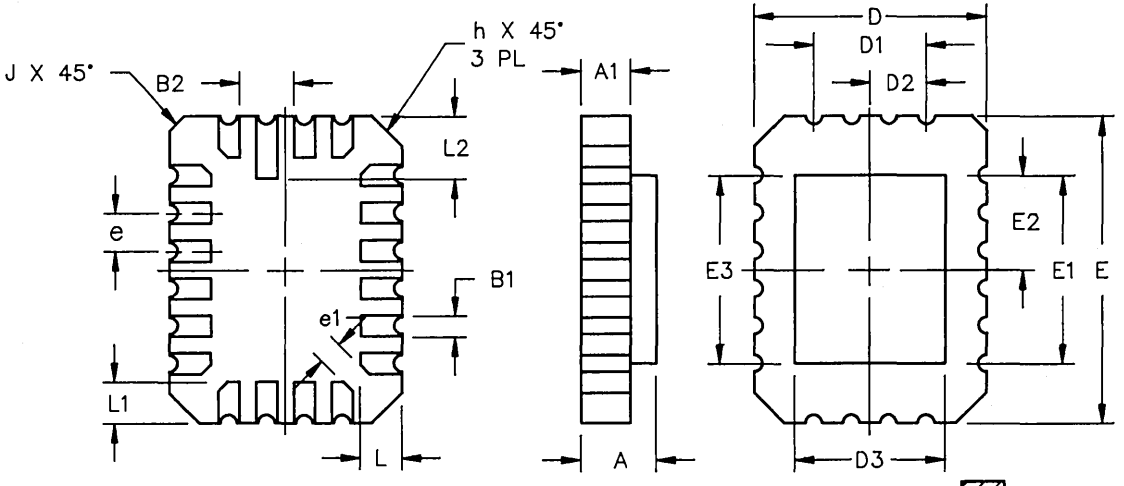
DWG #	L20–2		L28–1		L44–1		L48–1	
# OF LDS (N)	20		28		44		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120	.055	.120
A1	.054	.066	.050	.088	.054	.088	.045	.090
B1	.022	.028	.022	.028	.022	.028	.017	.023
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.342	.358	.442	.460	.640	.660	.554	.572
D1/E1	.200 BSC		.300 BSC		.500 BSC		.440 BSC	
D2/E2	.100 BSC		.150 BSC		.250 BSC		.220 BSC	
D3/E3	–	.358	–	.460	–	.560	.500	.535
e	.050 BSC		.050 BSC		.050 BSC		.040 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.012 RADIUS	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.033	.047
L1	.045	.055	.045	.055	.045	.055	.033	.047
L2	.077	.093	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	5		7		11		12	

LEADLESS CHIP CARRIERS (Continued)

52–68 LEAD LCC (SQUARE)

DWG #	L52–1		L52–2		L68–2		L68–1	
# OF LDS (N)	52		52		68		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.061	.087	.082	.120	.082	.120	.065	.120
A1	.051	.077	.072	.088	.072	.088	.055	.075
B1	.022	.028	.022	.028	.022	.028	.008	.014
B2	.072	REF	.072	REF	.072	REF	.072	REF
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.739	.761	.739	.761	.938	.962	.554	.566
D1/E1	.600	BSC	.600	BSC	.800	BSC	.400	BSC
D2/E2	.300	BSC	.300	BSC	.400	BSC	.200	BSC
D3/E3	–	.661	–	.661	–	.862	–	.535
e	.050	BSC	.050	BSC	.050	BSC	.025	BSC
e1	.015	–	.015	–	.015	–	.015	–
h	.040	REF	.040	REF	.040	REF	.040	REF
J	.020	REF	.020	REF	.020	REF	.020	REF
L	.045	.055	.045	.055	.045	.055	.045	.055
L1	.045	.055	.045	.055	.045	.055	.045	.055
L2	.077	.093	.075	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	13		13		17		17	

LEADLESS CHIP CARRIERS (Continued)



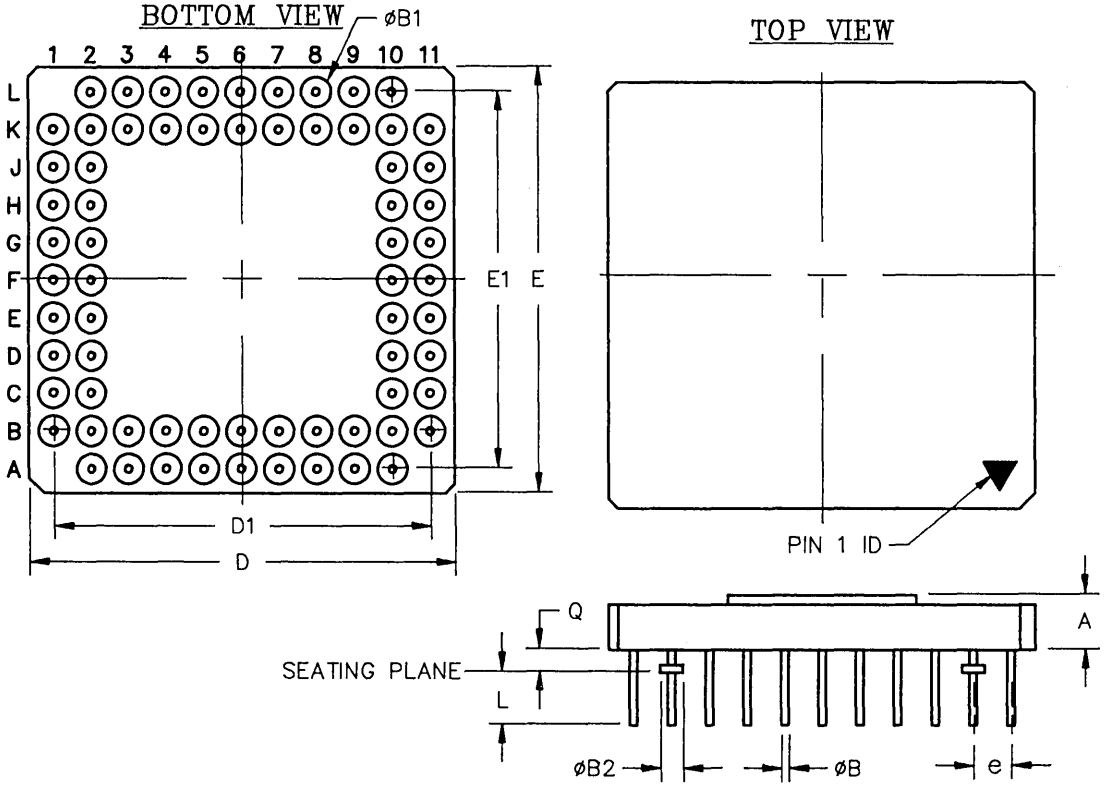
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–32 LEAD LCC (RECTANGULAR)

DWG #	L20–1		L22–1		L24–1		L28–2		L32–1	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.060	.075	.064	.100	.064	.120	.060	.120	.060	.120
A1	.050	.065	.054	.063	.054	.066	.050	.088	.050	.088
B1	.022	.028	.022	.028	.022	.028	.022	.028	.022	.028
B2	.072 REF		.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022	.006	.022
D	.284	.296	.284	.296	.292	.308	.342	.358	.442	.458
D1	.150 BSC		.150 BSC		.200 BSC		.200 BSC		.300 BSC	
D2	.075 BSC		.075 BSC		.100 BSC		.100 BSC		.150 BSC	
D3	–	.280	–	.280	–	.308	–	.358	–	.458
E	.420	.435	.480	.496	.392	.408	.540	.560	.540	.560
E1	.250 BSC		.300 BSC		.300 BSC		.400 BSC		.400 BSC	
E2	.125 BSC		.150 BSC		.150 BSC		.200 BSC		.200 BSC	
E3	–	.410	–	.480	–	.408	–	.558	–	.558
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
e1	.015	–	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.012 RADIUS		.025 REF		.040 REF		.040 REF	
J	.020 REF		.012 RADIUS		.015 REF		.020 REF		.020 REF	
L	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L1	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L2	.080	.095	.083	.097	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015	.003	.015
ND	4		4		5		5		7	
NE	6		7		7		9		9	

PIN GRID ARRAYS

68 PIN PGA (CAVITY UP)

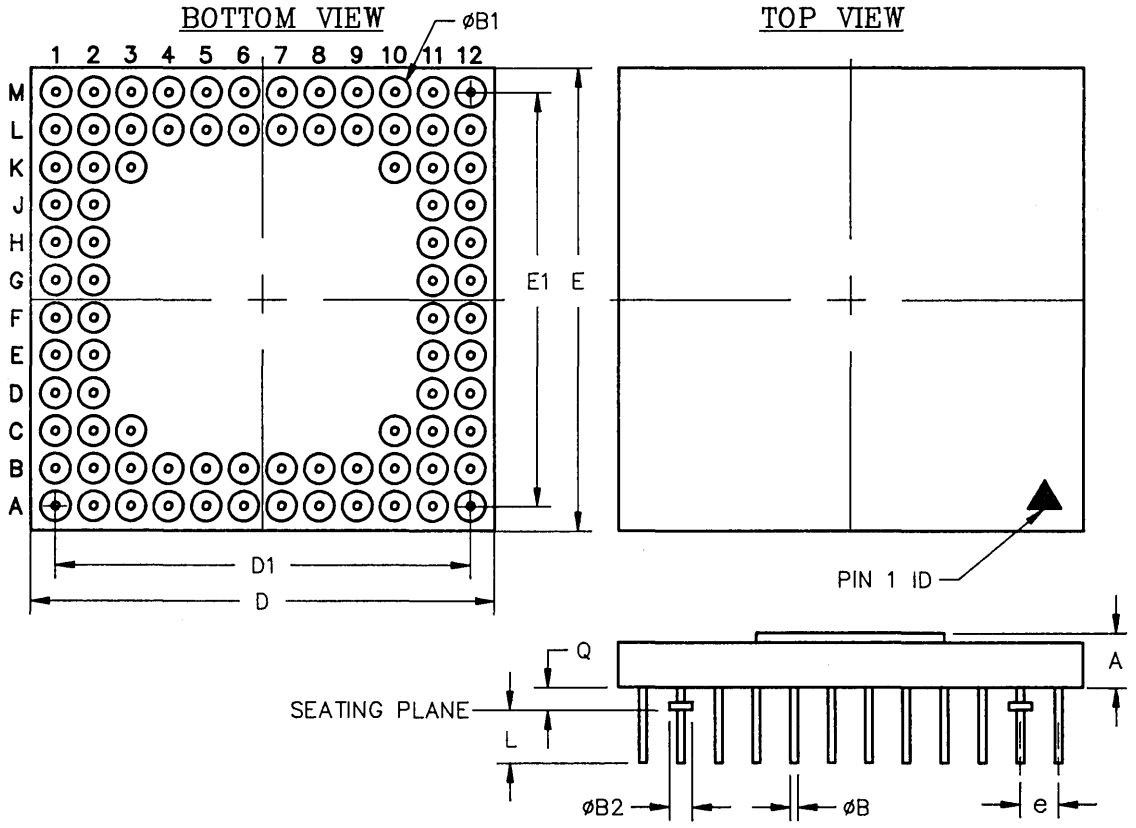


DWG #	G68-1	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.140	1.180
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY UP – 12 X 12 GRID)

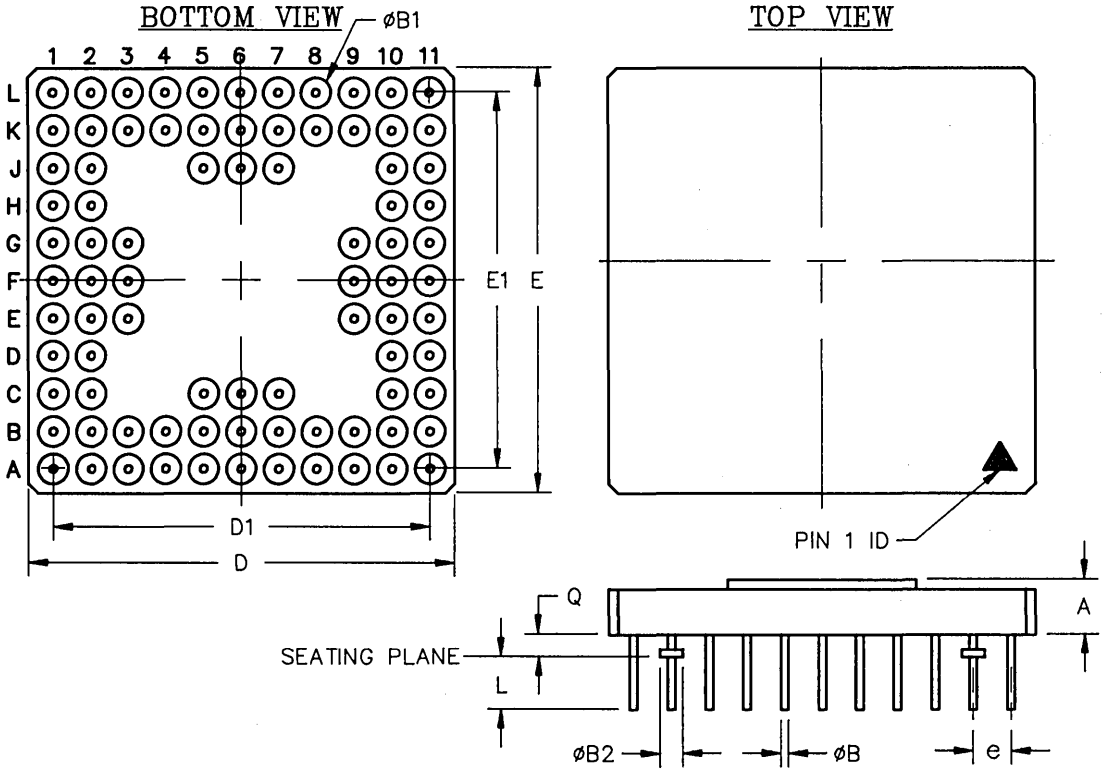


DWG #	G84–1	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
øB	.016	.020
øB1	.040	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY UP – 11 X 11 GRID)

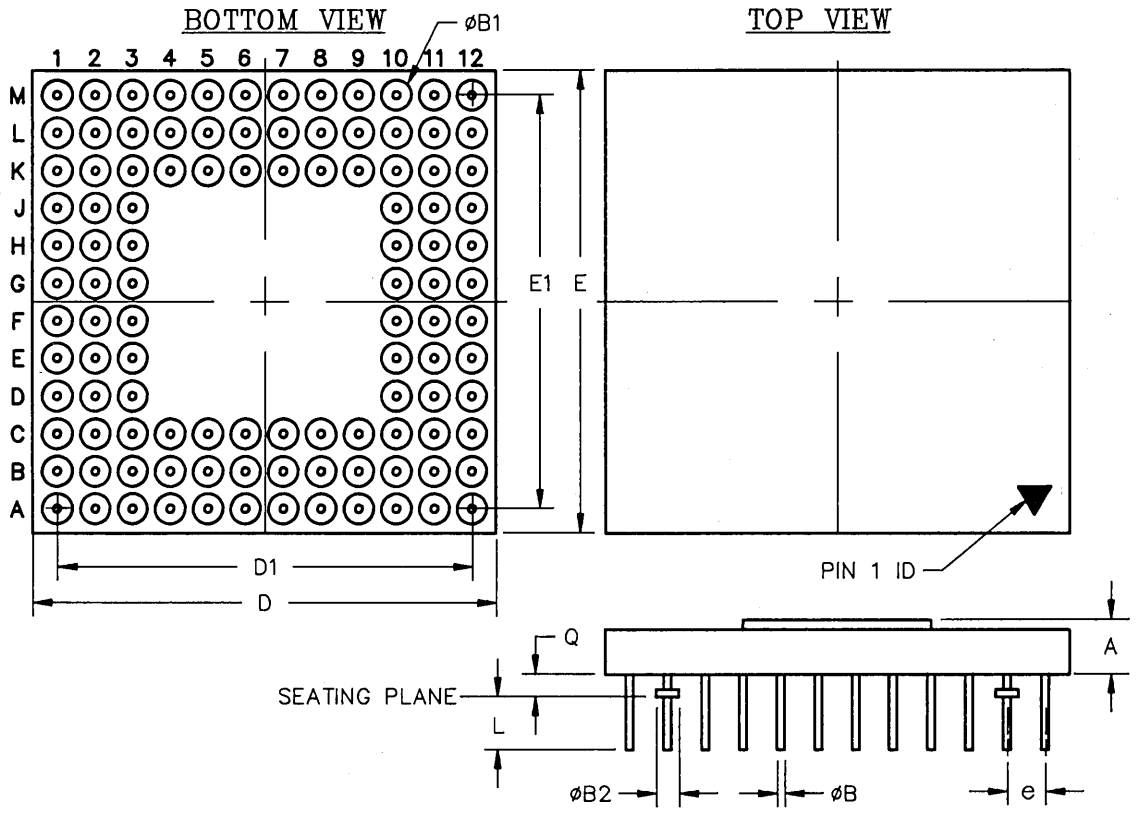


DWG #	G84–3	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.080	1.120
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

108 PIN PGA (CAVITY UP)

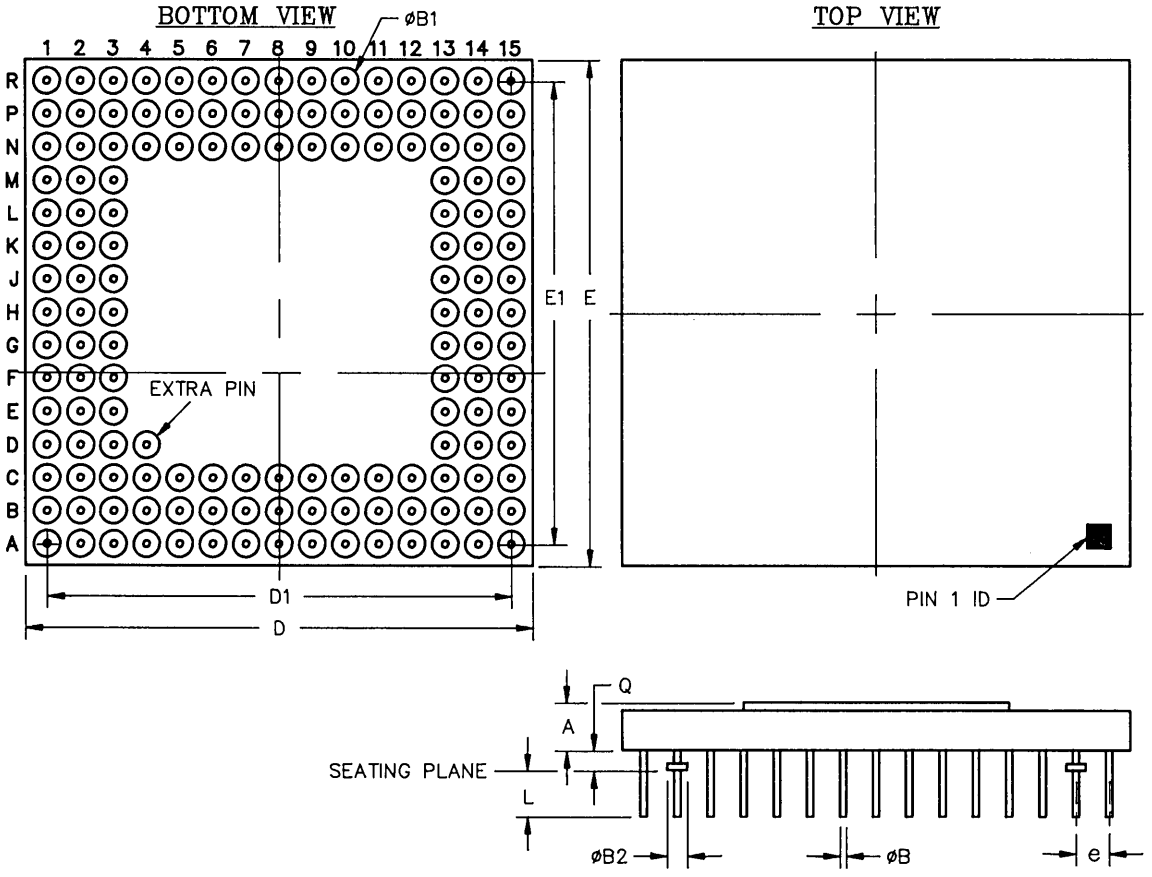


DWG #	G108-1	
# OF PINS (N)	108	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.188	1.212
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY UP)

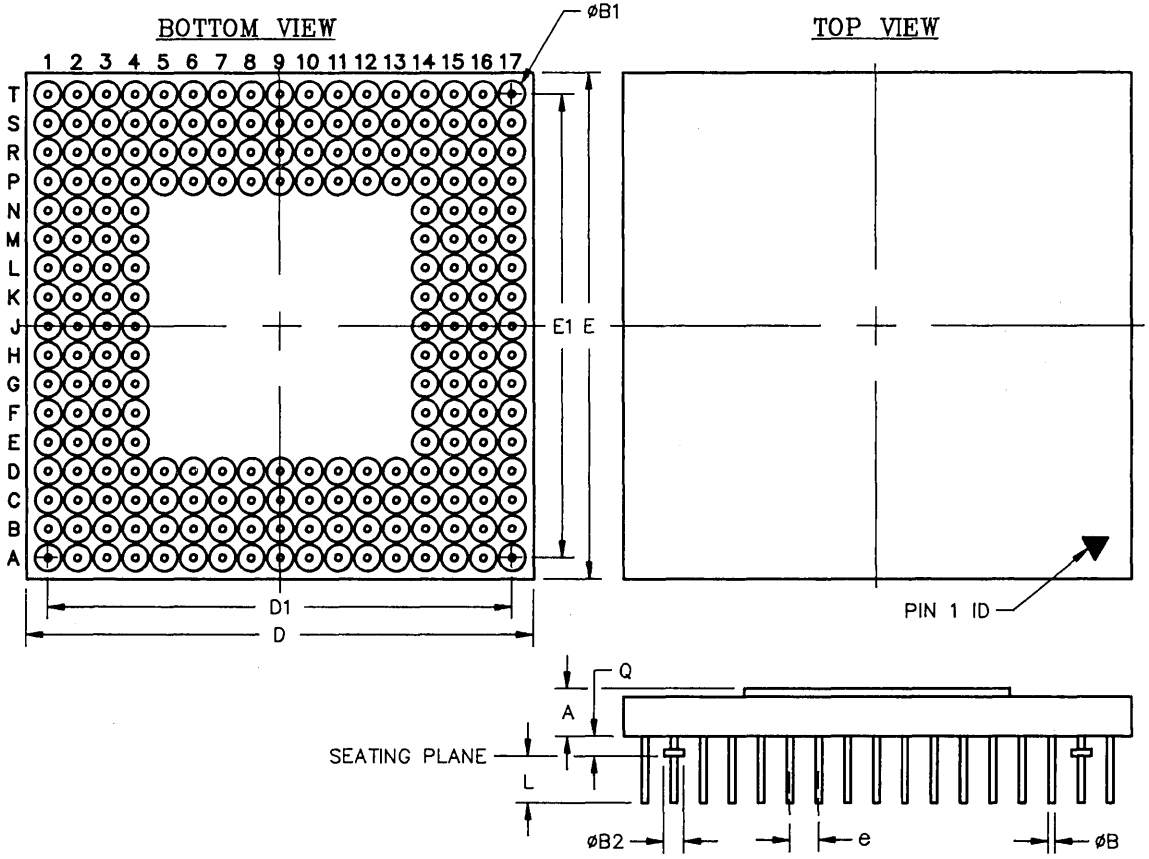


DWG #	G144-2	
# OF PINS (N)	145	
SYMBOL	MIN	MAX
A	.082	.125
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. EXTRA PIN (D–4) ELECTRICALLY CONNECTED TO D–3.

PIN GRID ARRAYS (Continued)

208 PIN PGA (CAVITY UP)

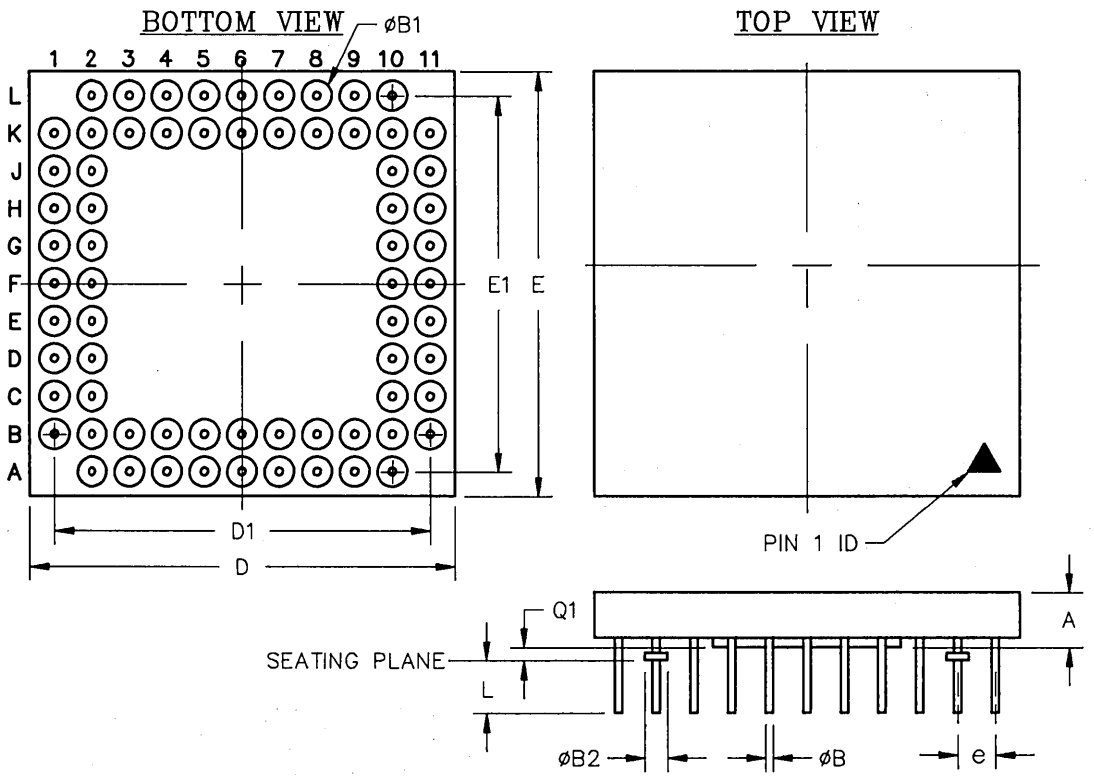


DWG #	G208-1	
# OF PINS (N)	208	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.732	1.780
D1/E1	1.600 BSC	
e	.100 BSC	
L	.125	.140
M	17	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

68 PIN PGA (CAVITY DOWN)

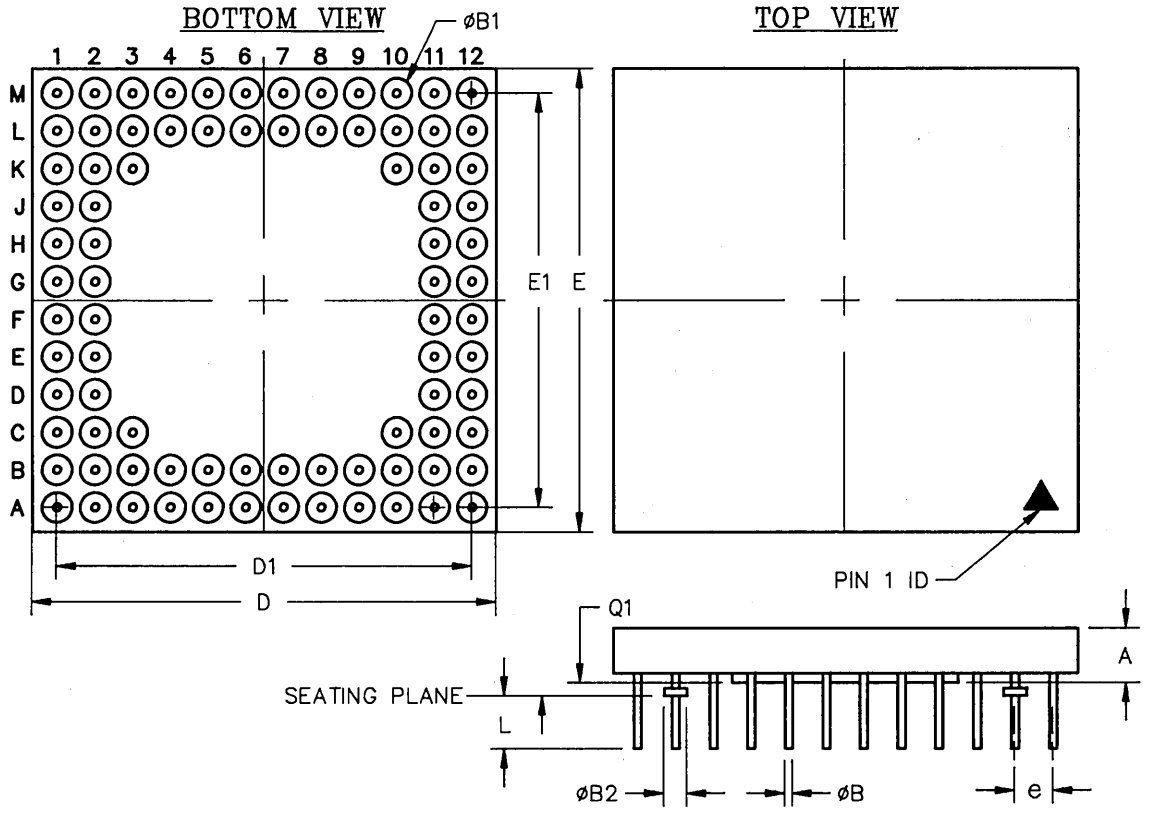


DWG #	GU68-2	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.077	.095
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.098	1.122
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY DOWN)

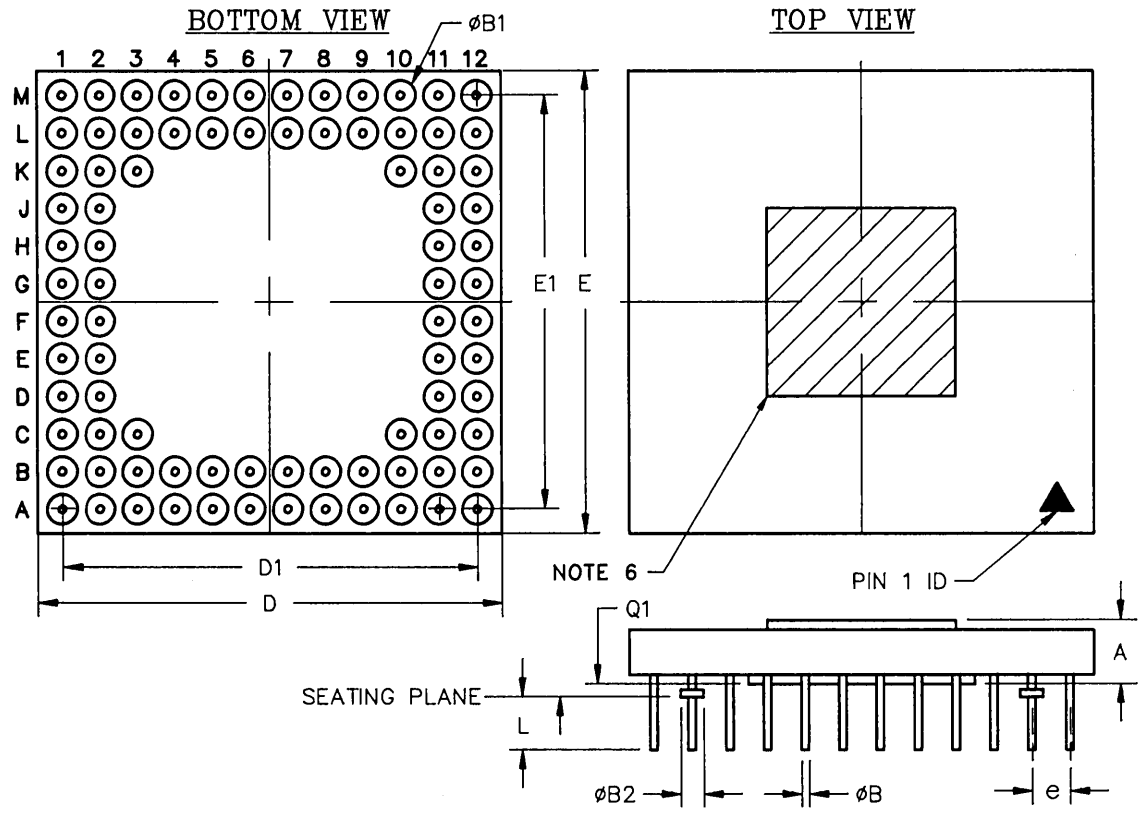


DWG #	G84-2	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.100	.120
M	12	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY DOWN – MIPS)

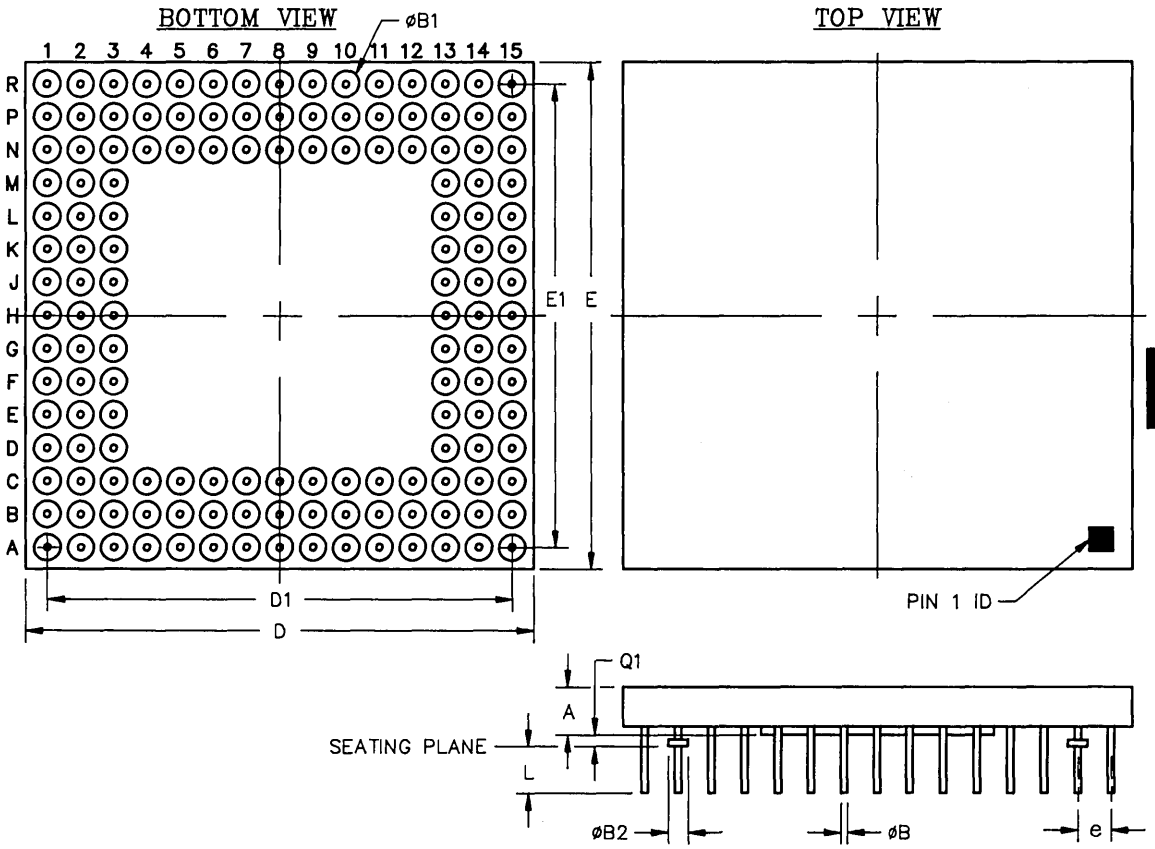


DWG #	G84-4	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. CROSS HATCHED AREA INDICATES INTEGRALL METALLIC HEAT SINK.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY DOWN)

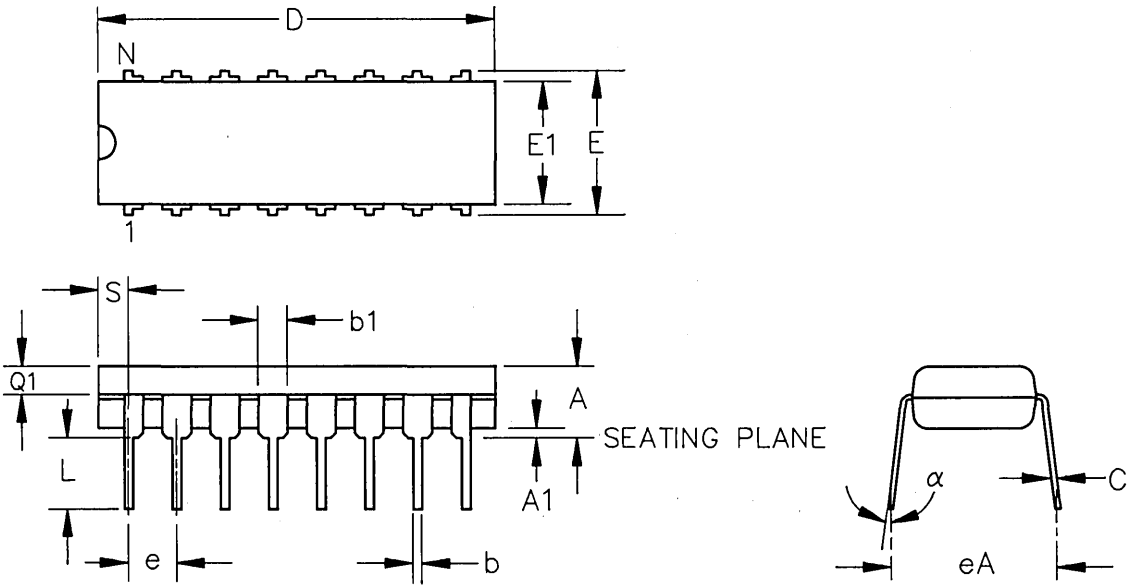


DWG #	G144-1	
# OF PINS (N)	144	
SYMBOL	MIN	MAX
A	.082	.100
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PLASTIC DUAL IN-LINE PACKAGES

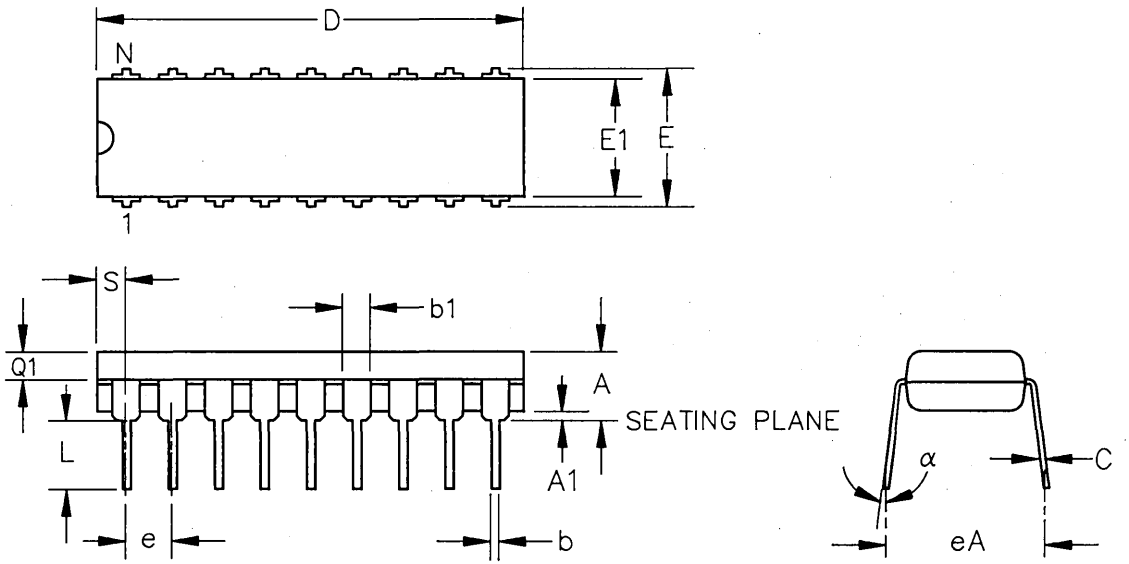
16-32 LEAD PLASTIC DIP (300 MIL)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P16-1		P22-1		P28-2		P32-2	
# OF LDS (N)	16		22		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.180	.145	.180
A1	.015	.035	.015	.035	.015	.030	.015	.030
b	.015	.022	.015	.022	.015	.022	.016	.022
b1	.050	.070	.050	.065	.045	.065	.045	.060
C	.008	.012	.008	.012	.008	.015	.008	.015
D	.745	.760	1.050	1.060	1.345	1.375	1.545	1.585
E	.300	.325	.300	.320	.300	.325	.300	.325
E1	.247	.260	.240	.270	.270	.295	.275	.295
e	.090	.110	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.400	.310	.400
L	.120	.150	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°
S	.015	.035	.020	.040	.020	.042	.020	.060
Q1	.050	.070	.055	.075	.055	.065	.055	.065

PLASTIC DUAL IN-LINE PACKAGES (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

18-24 LEAD PLASTIC DIP (300 MIL - FULL LEAD)

DWG #	P18-1		P20-1		P24-1	
# OF LDS (N)	18		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.165
A1	.015	.035	.015	.035	.015	.035
b	.015	.020	.015	.020	.015	.020
b1	.050	.070	.050	.070	.050	.065
C	.008	.012	.008	.012	.008	.012
D	.885	.910	1.022	1.040	1.240	1.255
E	.300	.325	.300	.325	.300	.320
E1	.247	.260	.240	.280	.250	.275
e	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.370
L	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°
S	.040	.060	.025	.070	.055	.075
Q1	.050	.070	.055	.075	.055	.070

PLASTIC DUAL IN-LINE PACKAGES (Continued)

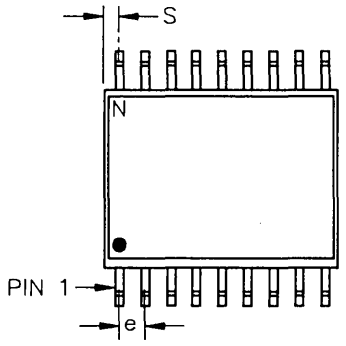
24-48 LEAD PLASTIC DIP (600 MIL)

DWG #	P24-2		P28-1		P32-1		P40-1		P48-1	
# OF LEADS (N)	24		28		32		40		48	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.160	.185	.160	.185	.170	.190	.160	.185	.170	.200
A1	.015	.035	.015	.035	.015	.050	.015	.035	.015	.035
b	.015	.020	.015	.020	.016	.020	.015	.020	.015	.020
b1	.050	.065	.050	.065	.045	.055	.050	.065	.050	.065
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.240	1.260	1.420	1.460	1.645	1.655	2.050	2.070	2.420	2.450
E	.600	.620	.600	.620	.600	.625	.600	.620	.600	.620
E1	.530	.550	.530	.550	.530	.550	.530	.550	.530	.560
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
eA	.610	.670	.610	.670	.610	.670	.610	.670	.610	.670
L	.120	.150	.120	.150	.125	.135	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	.060	.080	.055	.080	.070	.080	.070	.085	.060	.075
Q1	.060	.080	.060	.080	.065	.075	.060	.080	.060	.080

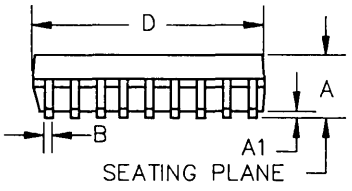
64 LEAD PLASTIC DIP (900 MIL)

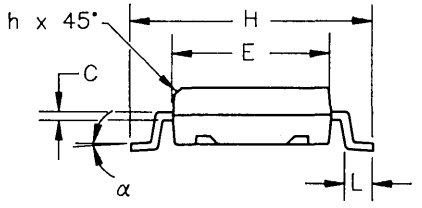
DWG #	P64-1	
# OF LEADS (N)	64	
SYMBOLS	MIN	MAX
A	.180	.230
A1	.015	.040
b	.015	.020
b1	.050	.065
C	.008	.012
D	3.200	3.220
E	.900	.925
E1	.790	.810
e	.090	.110
eA	.910	1.000
L	.120	.150
α	0°	15°
S	.045	.065
Q1	.080	.090

SMALL OUTLINE IC



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, ULESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.



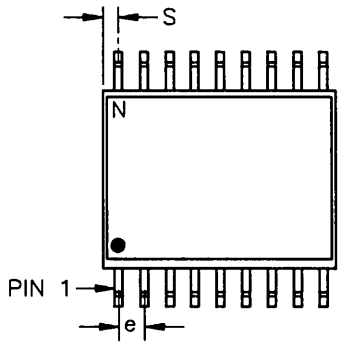


4

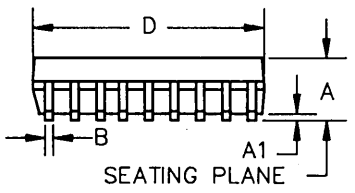
16–24 LEAD SMALL OUTLINE (GULL WING)

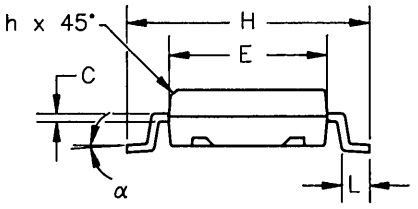
DWG #	SO16–1		SO18–1		SO20–2		SO24–2		SO24–3	
# OF LDS (N)	16 (.300)		18 (.300)		20 (.300")		24 (.300")		24 (.300")	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.095	.1043	.095	.1043	.095	.1043	.095	.1043	.110	.120
A1	.005	.0118	.005	.0118	.005	.0118	.005	.0118	.005	.0118
B	.014	.020	.014	.020	.014	.020	.014	.020	.014	.020
C	.0091	.0125	.0091	.0125	.0091	.0125	.0091	.0125	.007	.011
D	.403	.413	.447	.462	.497	.511	.600	.614	.620	.630
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
E	.292	.2992	.292	.2992	.292	.2992	.292	.2992	.295	.305
h	.010	.020	.010	.020	.010	.020	.010	.020	.012	.020
H	.400	.419	.400	.419	.400	.419	.400	.419	.406	.419
L	.018	.045	.018	.045	.018	.045	.018	.045	.028	.045
α	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°
S	.023	.035	.023	.035	.023	.035	.023	.035	.032	.043

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.





28 LEAD SMALL OUTLINE (GULL WING)

DWG #	SO28–2		SO28–3	
# OF LDS (N)	28 (.300")		28 (.330")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.1043	.110	.120
A1	.005	.0118	.005	.014
B	.014	.020	.014	.019
C	.0091	.0125	.006	.010
D	.700	.712	.718	.728
e	.050 BSC		.050 BSC	
E	.292	.2992	.340	.350
h	.010	.020	.012	.020
H	.400	.419	.462	.478
L	.018	.045	.028	.045
α	0°	8°	0°	8°
S	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)

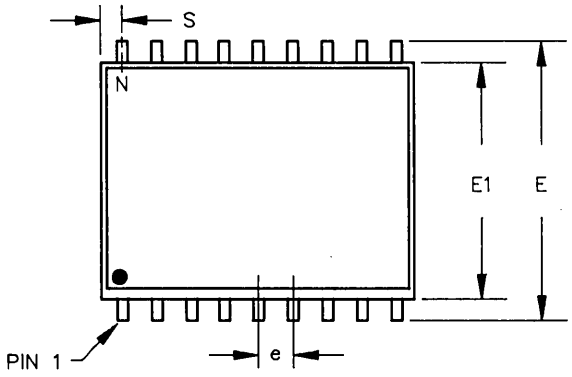
16–24 LEAD SMALL OUTLINE (EIAJ – .0315 PITCH)

DWG #	SO16–5		SO20–5		SO24–5	
# OF LDS (N)	16		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.057	.071	.069	.083	.069	.083
A1	.002 TYP		.002 TYP		.002 TYP	
B	.012	.020	.012	.020	.012	.020
C	.006	.010	.006	.010	.006	.010
D	.248	.271	.331	.354	.382	.405
E	.165	.180	.205	.220	.205	.220
e	.0315 BSC		.0315 BSC		.0315 BSC	
H	.232	.256	.295	.319	.295	.319
L	.010	–	.010	–	.010	–
α	0°	8°	0°	8°	0°	8°

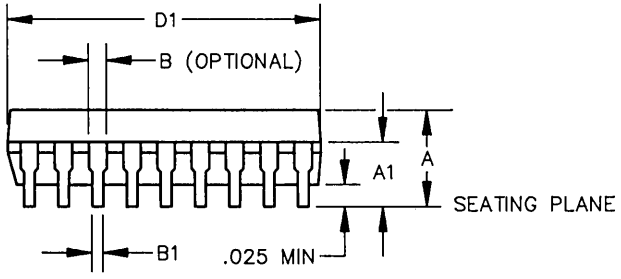
16–28 LEAD SMALL OUTLINE (EIAJ – .050 PITCH)

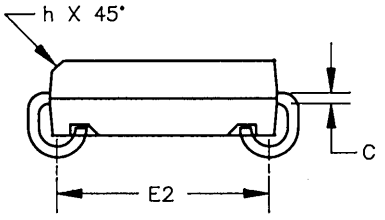
DWG #	SO16–6		SO18–6		SO20–6		SO24–6		SO28–6	
# OF LDS (N)	16		18		20		24		28	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.057	.071	.069	.083	.069	.083	.069	.083	.083	.098
A1	.002 TYP		.002 TYP		.002 TYP		.002 TYP		.002 TYP	
B	.012	.020	.012	.020	.012	.020	.012	.020	.012	.020
C	.006	.010	.006	.010	.006	.010	.006	.010	.006	.010
D	.382	.406	.437	.453	.480	.504	.580	.603	.720	.740
E	.165	.180	.205	.220	.205	.220	.205	.220	.290	.300
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
H	.232	.256	.295	.319	.295	.319	.295	.319	.378	.402
L	.010	–	.010	–	.010	–	.010	–	.010	–
α	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE

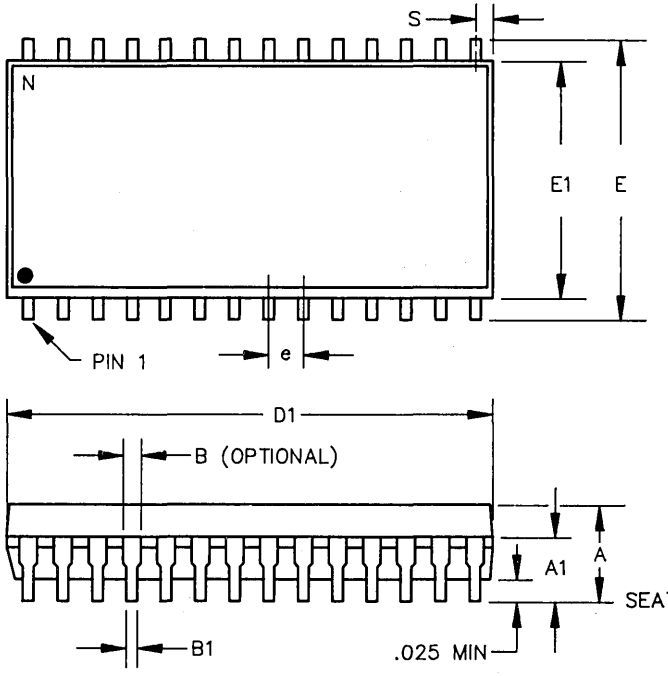




16–24 LEAD SMALL OUTLINE (J–BEND)

DWG #	SO16–2		SO20–1		SO24–4	
# OF LDS (N)	16 LD (.300")		20 LD (.300")		24 LD (.300")	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.120	.140	.130	.148
A1	.078	.095	.078	.095	.082	.095
B	.020	.024	.020	.024	.026	.032
B1	.014	.020	.014	.020	.015	.020
C	.008	.013	.008	.013	.007	.011
D1	.400	.412	.500	.512	.620	.630
E	.335	.347	.335	.347	.335	.345
E1	.292	.300	.292	.300	.295	.305
E2	.262	.272	.262	.272	.260	.280
e	.050 BSC		.050 BSC		.050 BSC	
h	.010	.020	.010	.020	.010	.020
S	.023	.035	.023	.035	.032	.043

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

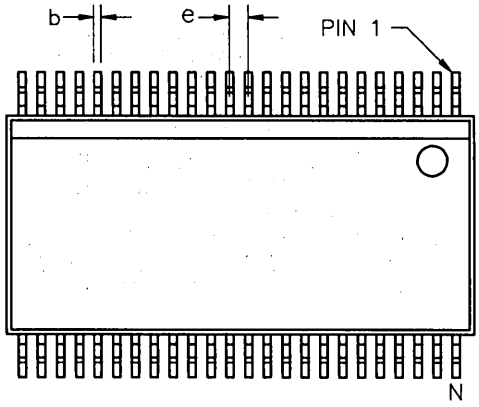
4

28–32 LEAD SMALL OUTLINE (J–BEND)

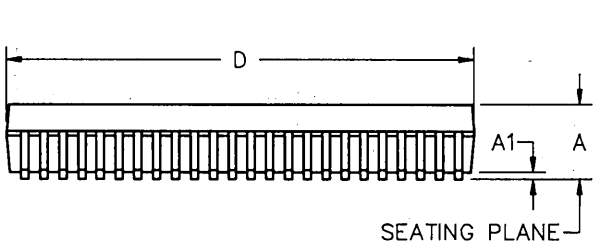
DWG #	SO28–5		SO28–4		SO32–2	
# OF LDS (N)	28 LD (.300")		28 LD (.350")		32 LD (.300")	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.130	.148	.130	.148
A1	.078	.095	.082	.095	.082	.095
B	.020	.024	.026	.032	.026	.032
B1	.014	.020	.016	.020	.016	.020
C	.008	.013	.007	.011	.008	.013
D1	.700	.712	.720	.730	.820	.830
E	.335	.347	.380	.390	.330	.340
E1	.292	.300	.345	.355	.295	.305
E2	.262	.272	.310	.330	.260	.275
e	.050 BSC		.050 BSC		.050 BSC	
h	.012	.020	.012	.020	.012	.020
S	.023	.035	.023	.035	.032	.043

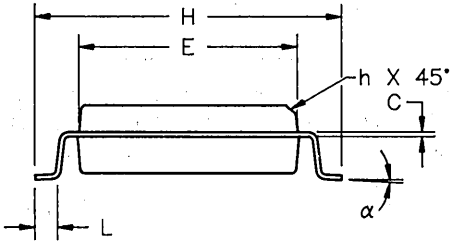
SMALL OUTLINE IC (Continued)

48 & 56 LEAD SMALL OUTLINE (SSOP – GULL WING)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

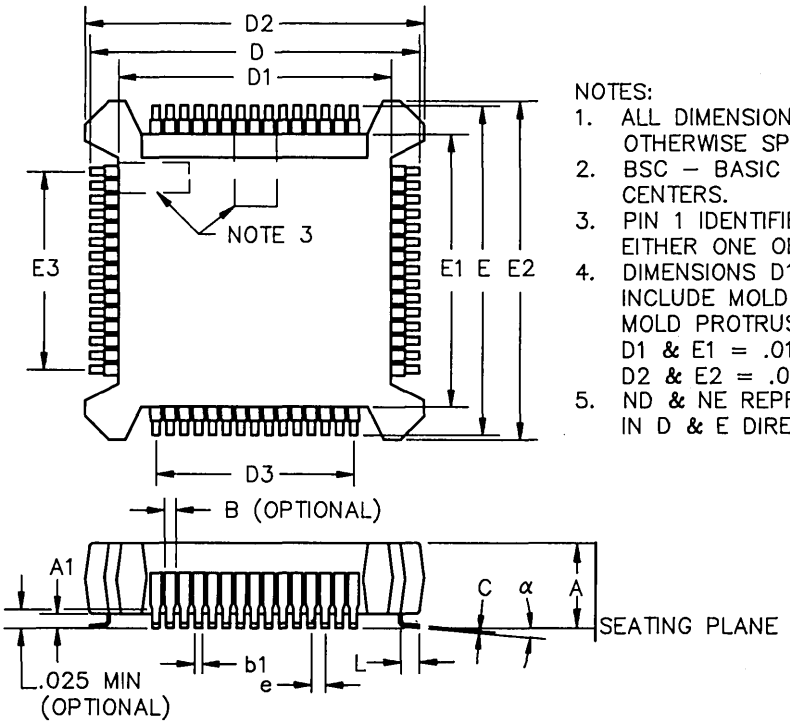




DWG #	SO48–1		SO56–1	
# OF LDS (N)	48 (.300")		56 (.300")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.110	.095	.110
A1	.008	.016	.008	.016
b	.008	.012	.008	.012
C	.005	.009	.005	.009
D	.620	.630	.720	.730
E	.291	.299	.291	.299
e	.025 BSC		.025 BSC	
H	.395	.420	.395	.420
h	.015	.025	.015	.025
L	.020	.040	.020	.040
α	0°	8°	0°	8°

PLASTIC QUAD FLATPACKS

100–132 LEAD PLASTIC QUAD FLATPACK (JEDEC)



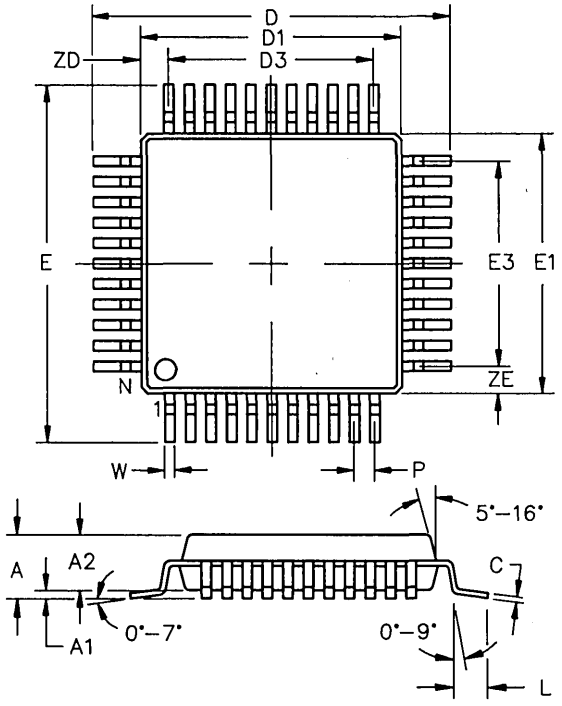
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. PIN 1 IDENTIFIER CAN BE POSITIONED AT EITHER ONE OF THESE TWO LOCATIONS.
4. DIMENSIONS D1, D2, E1, AND E2 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE MOLD PROTRUSIONS ARE AS FOLLOWS:
   D1 & E1 = .010 MAX.
   D2 & E2 = .007 MAX.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

4

DWG #	PQ100–1		PQ132–1	
# OF LDS (N)	100		132	
SYMBOLS	MIN	MAX	MIN	MAX
A	.160	.180	.160	.180
A1	.020	.040	.020	.040
B	.008	.016	.008	.016
b1	.008	.012	.008	.012
C	.0055	.008	.0055	.008
D	.875	.885	1.075	1.085
D1	.747	.753	.947	.953
D2	.897	.903	1.097	1.103
D3	.600 REF		.800 REF	
e	.025 BSC		.025 BSC	
E	.875	.885	1.075	1.085
E1	.747	.753	.947	.953
E2	.897	.903	1.097	1.103
E3	.600 REF		.800 REF	
L	.020	.030	.020	.030
α	0°	8°	0°	8°
ND/NE	25/25		33/33	

PLASTIC QUAD FLATPACKS (Continued)

80–128 LEAD PLASTIC QUAD FLATPACK (EIAJ)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .010 PER SIDE.
4. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

DWG #	PQ80–2		PQ100–2		PQ120–2		PQ128–2	
# OF LDS (N)	80		100		120		128	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.110	.124	.110	.124	.136	.156	.136	.156
A1	.010	–	.010	–	.010	–	.010	–
A2	.100	.120	.100	.120	.125	.144	.125	.144
C	.005	.008	.005	.008	.005	.008	.005	.008
D	.909	.917	.909	.917	1.224	1.232	1.224	1.232
D1	.783	.791	.783	.791	1.098	1.106	1.098	1.106
D3	.724 REF		.742 REF		.913 REF		.976 REF	
E	.673	.681	.673	.681	1.224	1.232	1.224	1.232
E1	.547	.555	.547	.555	1.098	1.106	1.098	1.106
E3	.472 REF		.486 REF		.913 REF		.976 REF	
L	.026	.037	.026	.037	.026	.037	.026	.037
ND/NE	16/24		20/30		30/30		32/32	
P	.0315 BSC		.026 BSC		.026 BSC		.0315 BSC	
W	.010	.018	.012	.018	.012	.018	.012	.018
ZD	.032		.023		.094		.063	
ZE	.039		.032		.094		.063	

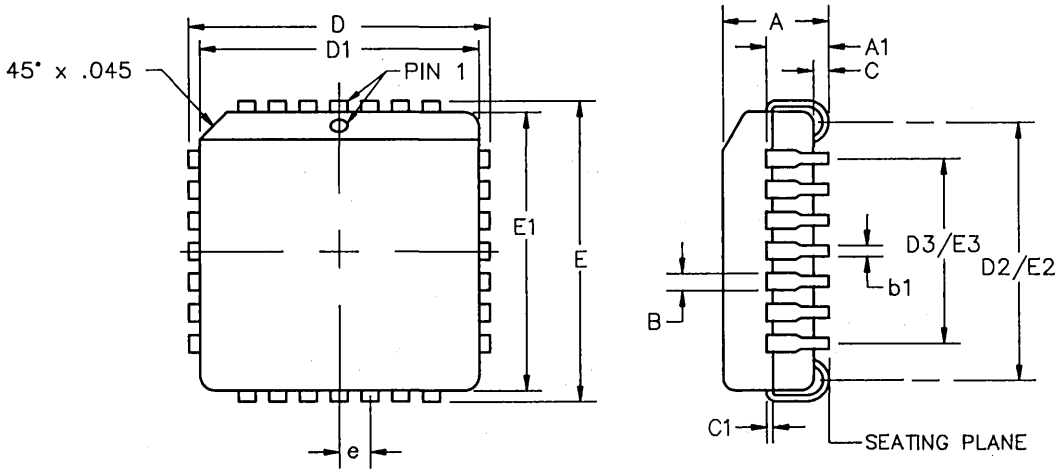
PLASTIC QUAD FLATPACKS (Continued)

144–208 LEAD PLASTIC QUAD FLATPACK (EIAJ)

DWG #	PQ144–2		PQ160–2		PQ184–2		PQ208–2	
# OF LDS (N)	144		160		184		208	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.136	.156	.136	.156	.136	.156	.136	.156
A1	.010	–	.010	–	.010	–	.010	–
A2	.125	.144	.125	.144	.125	.144	.125	.144
C	.005	.008	.005	.008	.005	.008	.005	.008
D	1.224	1.232	1.224	1.232	1.224	1.232	1.224	1.232
D1	1.098	1.106	1.098	1.106	1.098	1.106	1.098	1.106
D3	.896 RF		.998 REF		.886 REF		1.004 REF	
E	1.224	1.232	1.224	1.232	1.224	1.232	1.224	1.232
E1	1.098	1.106	1.098	1.106	1.098	1.106	1.098	1.106
E3	.896 REF		.998 REF		.886 REF		1.004 REF	
L	.026	.037	.026	.037	.026	.037	.026	.037
ND/NE	36/36		40/40		46/46		52/52	
P	.026 BSC		.026 BSC		.020 BSC		.020 BSC	
W	.009	.014	.009	.014	.009	.014	.009	.014
ZD	.103		.052		.108		.049	
ZE	.103		.052		.108		.049	

PLASTIC LEADED CHIP CARRIERS

20–84 LEAD PLCC (SQUARE)



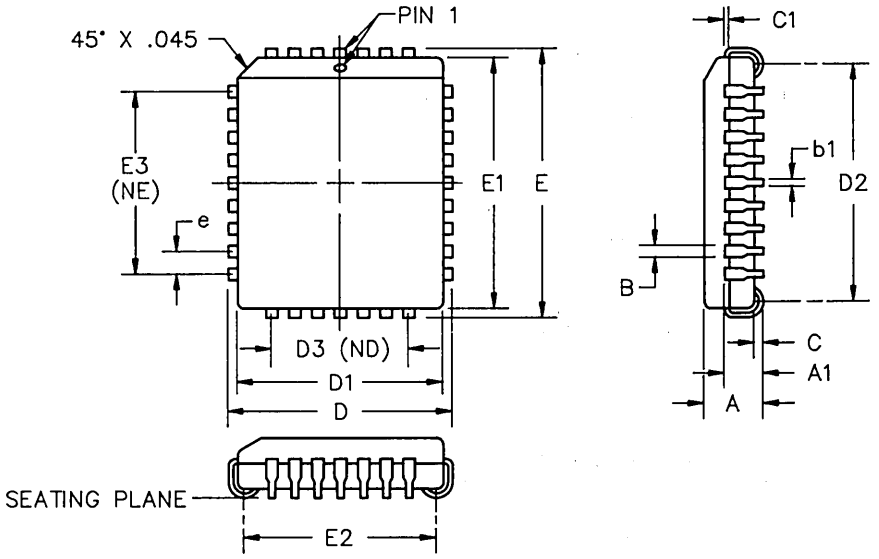
NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PKG.

DWG #	J20–1		J28–1		J44–1		J52–1		J68–1		J84–1	
# OF LDS	20		28		44		52		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180
A1	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115
B	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032
b1	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021
C	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040
C1	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
D1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
D2/E2	.290	.330	.390	.430	.590	.630	.690	.730	.890	.930	1.090	1.130
D3/E3	.200 REF		.300 REF		.500 REF		.600 REF		.800 REF		1.000 REF	
E	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
E1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
ND/NE	5		7		11		13		17		21	

PLASTIC LEADED CHIP CARRIERS (Continued)

18–32 LEAD PLCC (RECTANGULAR)

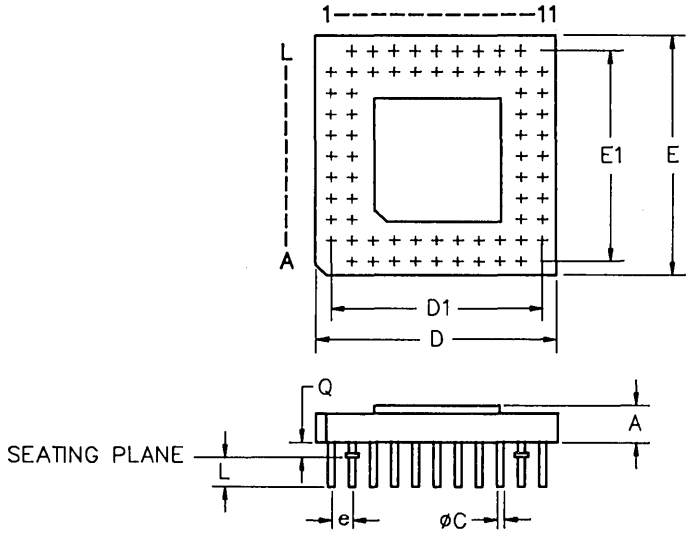


DWG #	J18–1		J32–1	
# OF LDS	18		32	
SYMBOL	MIN	MAX	MIN	MAX
A	.120	.140	.120	.140
A1	.075	.095	.075	.095
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.015	.040	.015	.040
C1	.008	.012	.008	.012
D	.320	.335	.485	.495
D1	.289	.293	.449	.453
D2	.225	.265	.390	.430
D3	.150 REF		.300 REF	
E	.520	.535	.585	.595
E1	.489	.493	.549	.553
E2	.422	.465	.490	.530
E3	.200 REF		.400 REF	
e	.050 BSC		.050 BSC	
ND/NE	4 / 5		7 / 9	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED MEASURED FROM THE BOTTOM OF THE PACKAGE.

PLASTIC PIN GRID ARRAYS

68–208 PIN PGA (CAVITY UP)



NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC PIN SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
5. DIM. "A" INCLUDES BOTH THE PKG BODY & THE LID. IT DOES NOT INCLUDE HEATSINK OR OTHER ATTACHED FEATURES.
6. PIN DIAMETER "C" EXCLUDES SOLDER DIP OR OTHER LEAD FINISH.
7. PIN TIPS MAY HAVE RADIUS OR CHAMFER.

DWG No.	PG 68–2		PG 84–2		PG 208–2	
# OF PINS (N)	68 PIN		84 PIN		208 PIN	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.115	.160	.115	.160	.115	.160
C	.016	.020	.016	.020	.016	.020
D	1.140	1.180	1.140	1.180	1.740	1.780
D1	1.000 BSC		1.000 BSC		1.600 BSC	
E	1.140	1.180	1.140	1.180	1.740	1.780
E1	1.000 BSC		1.000 BSC		1.600 BSC	
e	.100 BSC		.100 BSC		.100 BSC	
L	.100	.160	.100	.160	.100	.160
M	11		11		17	
Q	.040	.070	.040	.070	.040	.070

GENERAL INFORMATION

TECHNOLOGY AND CAPABILITIES

QUALITY AND RELIABILITY

PACKAGE DIAGRAM OUTLINES

COMPLEX LOGIC PRODUCTS

5

STANDARD LOGIC PRODUCTS

APPLICATION AND TECHNICAL NOTES

COMPLEX LOGIC PRODUCTS

The need for high performance building blocks of ever increasing complexity is the basis for many of today's innovative design solutions. IDT's Complex Logic product line addresses this need by combining IDT's sub-micron CEMOS process with highly sophisticated design tools to produce VLSI building blocks that satisfy the most demanding system requirements. IDT's Complex Logic products are divided into four functional areas:

Error Detection and Correction
Graphics
Read-Write Buffers
DSP and Microslice

Error Detection and Correction (EDC)

Today's high performance systems are becoming increasingly DRAM intensive. IDT has developed a range of high performance CEMOS EDC devices that eliminate the performance penalties once associated with these circuits while assuring the designer of the continuous, error free operation necessary in such systems. IDT's family of EDC products offers the designer a choice of 16, 32, or 64 bit devices with either single bus or flow through operation. These devices are capable of detecting and correcting errors in as little as 20ns.

Graphics

The demand for performance intensive graphics in applications like 3D modelling, high performance workstations, X-Windows terminals, and multimedia screens requires designs using high performance graphics building blocks. IDT offers a range of products in this area from PaletteDAC's running at up to 165 MHz for true and pseudo-color displays to video speed flash A/D converters. IDT intends to release future building blocks that will enable a designer to easily implement all the functions necessary to gain a competitive edge in graphics systems.

Read-Write Buffers

The current generation of RISC and CISC microprocessors depend on secondary cache memory for their best performance. IDT's newly released 73200 family of write buffers provide the designer with a flexible approach to meeting these requirements in his system.

DSP and Microslice Processors

Digital signal processing applications have always demanded extremely high performance building blocks. IDT continues to offer a selection of the world's fastest fixed point DSP elements including multipliers, multiplier/accumulators, ALU's and microslice processors. These components enable the construction of customized, high performance architectures and instruction sets.

Quality

All IDT Complex Logic products are manufactured on a MIL-STD-883, Class B compliant manufacturing line. IDT military products offer: a number of DESC qualified product options; radiation tolerant and radiation enhanced versions; package options including hermetic DIP, LCC and flatpack.

All IDT commercial products are manufactured using the same military qualified production line and adhere to strict quality requirements developed during IDT's long history of supply to military customers. IDT commercial products are available in a variety of packages including through hole and surface mount configurations.

The Future

IDT's Complex Logic product line will continue to upgrade the performance of existing products while at the same time developing the products and architectural enhancements that will facilitate the design of the systems of the future. Our goal is to provide the designer with components of the highest performance, integration level, and functionality possible.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

4-BIT CMOS MICROPROCESSOR SLICE

IDT39C01C
IDT39C01D
IDT39C01E

FEATURES:

- Low-power CEMOS™
  - Icc (max.)
    Military: 35mA
    Commercial: 30mA
  Fast
  - IDT39C01C — meets 2901C speeds
  - IDT39C01D — 20% speed upgrade
  - IDT39C01E — 40% speed upgrade
- Eight-function ALU
  - Performs addition, two subtraction operations and five logic functions on two source operands
- Expandable
  - Longer word lengths achieved through cascading any number of IDT39C01s
- Four status flags
  - Carry, overflow, negative and zero
- Pin-compatible and functionally equivalent to all versions of the 2901
- Available in 40-pin DIP and 44-pin LCC
- Military product available compliant to MIL-STD-883 and DESC Standard Military Drawing (SMD) 5962-88535

DESCRIPTION:

The IDT39C01s are high-speed, cascadable ALUs which can be used to implement CPUs, peripheral controllers and programmable microprocessors. The IDT39C01's microinstruction flexibility allows for easy emulation of most digital computers.

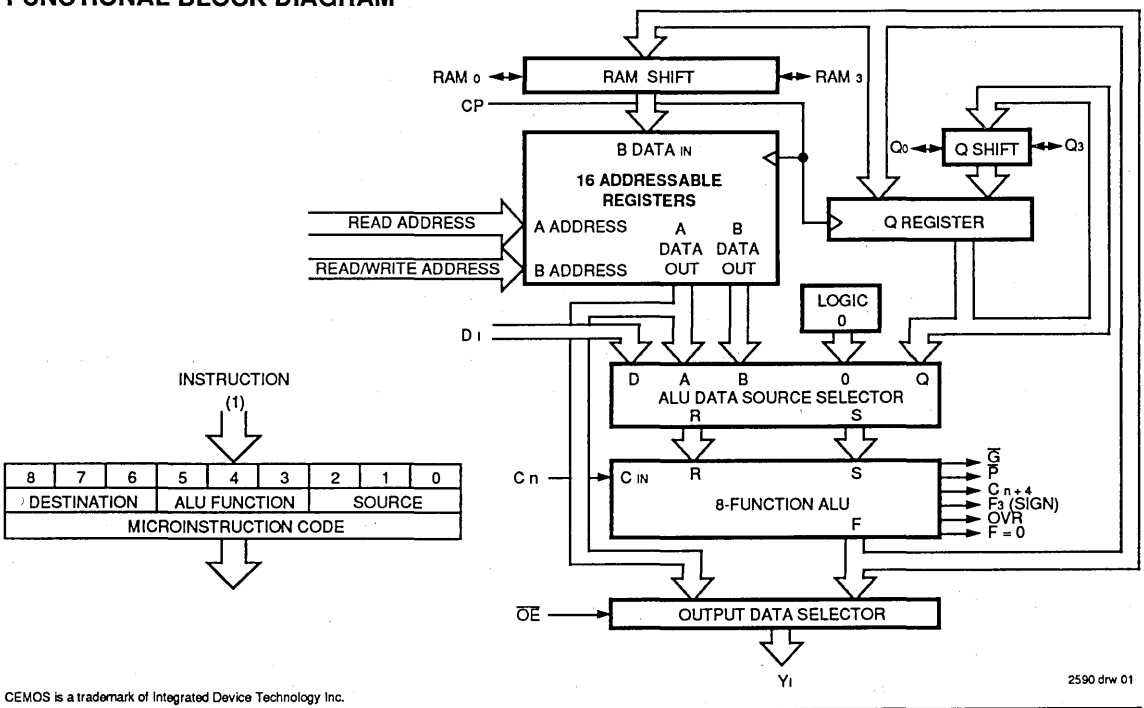
This extremely low-power yet high-speed ALU consists of a 16-word-by-4-bit dual-port RAM, a high-speed ALU and the required shifting, decoding and multiplexing logic. It is expandable in 4-bit increments, contains a flag output along with three-state data outputs, and can easily use either a ripple carry or full lookahead carry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU destination register, ALU source operands and the ALU function.

The IDT39C01 is fabricated using CEMOS™, a CMOS technology designed for high-performance and high-reliability. It is a pin-compatible, performance-enhanced, functional replacement for all versions of the 2901.

Military grade product is manufactured in compliance with the latest version of MIL-STD-883, Class B.

5

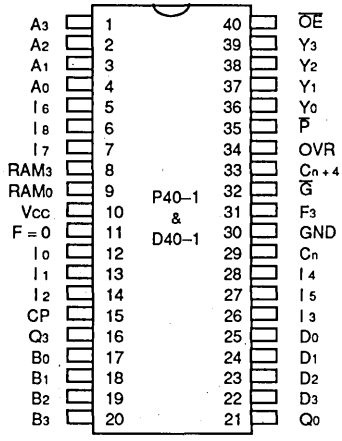
FUNCTIONAL BLOCK DIAGRAM



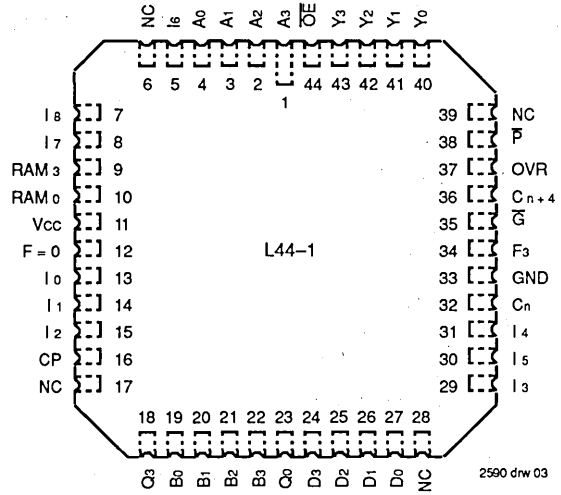
2590 drw 01

CEMOS is a trademark of Integrated Device Technology Inc.

PIN CONFIGURATION



DIP
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_0 - A_3	I	Four address inputs to the register file which select one register and displays its contents through the A port.
B_0 - B_3	I	Four address inputs to the register file which select one of the registers in the file, the contents of which is displayed through the B port. They also select the location into which new data can be written when the clock goes LOW.
I_0 - I_8	I	Nine instruction control lines which determine what data source will be applied to the ALU $I_{(0, 1, 2)}$, what function the ALU will perform $I_{(3, 4, 5)}$ and what data is to be deposited in the Q Register or the register file $I_{(6, 7, 8)}$.
D_0 - D_3	I	Four-bit direct data inputs which are the data source for entering external data into the device. D_0 is the LSB.
Y_0 - Y_3	O	Four three-state output lines which, when enabled, display either the four outputs of the ALU or the data on the A port of the register stack. This is determined by the destination code $I_{(6, 7, 8)}$.
F_3	O	Most significant ALU output bit (sign-bit).
F = 0	O	Open drain output which goes HIGH if the F_0 - F_3 ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+4}	O	Carry-out of the internal ALU.
Q_3 RAM_3	I/O	Bidirectional lines controlled by $I_{(6, 7, 8)}$. Both are three-state output drivers connected to the TTL-compatible CMOS inputs. When the destination code on $I_{(6, 7, 8)}$ indicates an up shift, the three-state outputs are enabled, the MSB of the Q Register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_3 and RAM_3 lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable on which, when pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{G}$, $\overline{P}$	O	Carry generate and carry propagate output of the ALU. These are used to perform a carry lookahead operation.
OVR	O	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.
CP	I	Clock input. LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 16 x 4 RAM which comprises the master latches of the register file. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.

2590 tbl 01

ALU SOURCE OPERAND CONTROL

Mnemonic	Microcode				ALU Source Operands	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

2590 tbl 02

ALU FUNCTION CONTROL

Mnemonic	Microcode				ALU Function	Symbol
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S – R
SUBS	L	H	L	2	R Minus S	R – S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EX-OR S	R ∇ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \nabla S}$

2590 tbl 03

DEVICE ARCHITECTURE:

The IDT39C01 CMOS bit-slice microprocessor is configured four bits wide and is cascadable to any number of bits (4, 8, 12, 16, etc.). Key elements which make up this four-bit microprocessor slice are: 1) the register file (16 x 4 dual-port RAM) with shifter; 2) ALU and 3) Q Register and shifter.

REGISTER FILE — RAM data is read from the A port as controlled by the 4-bit A address field input. Data, as defined by the B address field input, can be simultaneously read from the B port of the RAM. This same code can be applied to the A select and B select field with the identical data appearing at both the RAM A port and B port outputs, simultaneously. New data is written into the file (word) defined by the B address field of the RAM when activated by the RAM write enable. The RAM data input field is driven by a 3-input multiplexer that is used to shift the ALU output data (F). It is capable of shifting the data up one position, down one position or not shifting at all. The other inputs to the multiplexer are from the RAM_3 and RAM_0 I/O pins. For a shift up operation, the RAM_3 output buffer is enabled and the RAM_0 multiplexer input is enabled. During a shift down operation, the RAM_0 output buffer is enabled and the RAM_3 multiplexer input is enabled. Four-bit latches hold the RAM data while the clock is LOW, with the A port output and B port output each driving separate latches. The data to be written into the RAM is applied from the ALU F output.

ALU — The ALU can perform three binary arithmetic and five logic operations on the two 4-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer, with both having an inhibit capability. Both multiplexers are controlled by the I_0, I_1, I_2 inputs. This multiplexer configuration enables the user to select various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs (I_3, I_4, I_5) are used to select the ALU function. This high-speed ALU also incorporates a carry-in (C_n) input, carry propagate ($\overline{P}$) output, carry generate ($\overline{G}$) output and carry-out (C_{n+4}) all aimed at accelerating arithmetic operations by the use of carry look ahead logic. The overflow output pin (OVR) will be HIGH when arithmetic operations exceed the two's complement number range. The ALU data outputs (F_0, F_1, F_2, F_3) are routed to the RAM, Q Register inputs and the Y outputs under control of the I_6, I_7, I_8 control signal inputs. The MSB of the ALU is output as F_3 so the user can examine the sign-bit without enabling the three-state outputs. An open drain output, F = 0, is HIGH when $F_0 = F_1 = F_2 = F_3 = 0$ so the user can determine when the ALU output is zero by wire-ORing these outputs together.

Q REGISTER — The Q Register is a separate 4-bit file intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q Register. In either the shift-up or shift-down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_3, which operate comparably to the RAM shifter. They are controlled by the I_6, I_7, I_8 inputs.

The clock input of the IDT39C01 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and RAM EN is enabled, new data will be written into the RAM file defined by the B address field.

5

ALU DESTINATION CONTROL(1)

Mnemonic	Microcode				RAM Function		Q Register Function		Y Output	RAM Shifter		Q Shifter	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	$F \rightarrow Q$	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	$F \rightarrow B$	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	$F \rightarrow B$	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	$F/2 \rightarrow B$	DOWN	$Q/2 \rightarrow Q$	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	$F/2 \rightarrow B$	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	$2F \rightarrow B$	UP	$2Q \rightarrow Q$	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	$2F \rightarrow B$	X	NONE	F	IN_0	F_3	X	Q_3

NOTE:

2590 tbl 04

1. X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
   B = Register Addressed by B inputs.
   UP is toward MSB; DOWN is toward LSB.

SOURCE OPERAND AND ALU FUNCTION MATRIX(1)

Octal $I_{5,4,3}$	ALU Function	$I_{2,1,0}$ Octal 0	1	2	3	4	5	6	7
		ALU Source A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C_n = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C_n = L S Minus R	Q − A − 1	B − A − 1	Q − 1	B − 1	A − 1	A − D − 1	Q − D − 1	−D − 1
	C_n = H	Q − A	B − A	Q	B	A	A − D	Q − D	−D
2	C_n = L R Minus S	A − Q − 1	A − B − 1	−Q − 1	−B − 1	−A − 1	D − A − 1	D − Q − 1	D − 1
	C_n = H	A − Q	A − B	−Q	−B	−A	D − A	D − Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∇ Q	A ∇ B	Q	B	A	D ∇ A	D ∇ Q	D
7	R EX-NOR S	$\overline{A \nabla Q}$	$\overline{A \nabla B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \nabla A}$	$\overline{D \nabla Q}$	$\overline{D}$

NOTE:

2590 tbl 05

1. + = Plus; − = Minus; ∧ = AND; ∇ = EX-OR; ∨ = OR.

ALU LOGIC MODE FUNCTIONS

Octal		Group	Function
$I_{5,4,3}$	$I_{2,1,0}$		
4	0	AND	$A \wedge Q$
4	1		$A \wedge B$
4	5		$D \wedge A$
4	6		$D \wedge Q$
3	0	OR	$A \vee Q$
3	1		$A \vee B$
3	5		$D \vee A$
3	6		$D \vee Q$
6	0	EX–OR	$A \nabla Q$
6	1		$A \nabla B$
6	5		$D \nabla A$
6	6		$D \nabla Q$
7	0	EX–NOR	$\overline{A \nabla Q}$
7	1		$\overline{A \nabla B}$
7	5		$\overline{D \nabla A}$
7	6		$\overline{D \nabla Q}$
7	2	INVERT	$\overline{Q}$
7	3		$\overline{B}$
7	4		$\overline{A}$
7	7		$\overline{D}$
6	2	PASS	Q
6	3		B
6	4		A
6	7		D
3	2	PASS	Q
3	3		B
3	4		A
3	7		D
4	2	"ZERO"	0
4	3		0
4	4		0
4	7		0
5	0	MASK	$\overline{A} \wedge Q$
5	1		$\overline{A} \wedge B$
5	5		$\overline{D} \wedge A$
5	6		$\overline{D} \wedge Q$

2590 tbl 06

ALU ARITHMETIC MODE FUNCTIONS

Octal		$C_n = L$		$C_n = H$	
$I_{5,4,3}$	$I_{2,1,0}$	Group	Function	Group	Function
0	0	ADD	A + Q	ADD plus one	A + Q + 1
0	1		A + B		A + B + 1
0	5		D + A		D + A + 1
0	6		D + Q		D + Q + 1
0	2	PASS	Q	Increment	Q + 1
0	3		B		B + 1
0	4		A		A + 1
0	7		D		D + 1
1	2	Decrement	Q – 1	PASS	Q
1	3		B – 1		B
1	4		A – 1		A
2	7		D – 1		D
2	2	1's Comp.	–Q – 1	2's Comp. (Negate)	–Q
2	3		–B – 1		–B
2	4		–A – 1		–A
1	7		–D – 1		–D
1	0	Subtract (1's Comp)	Q – A – 1	Subtract (2's Comp)	Q – A
1	1		B – A – 1		B – A
1	5		A – D – 1		A – D
1	6		Q – D – 1		Q – D
2	0		A – Q – 1		A – Q
2	1		A – B – 1		A – B
2	5		D – A – 1		D – A
2	6		D – Q – 1		D – Q

2590 tbl 07

DEFINITIONS(1)

$P_0 = R_0 + S_0$
$P_1 = R_1 + S_1$
$P_2 = R_2 + S_2$
$P_3 = R_3 + S_3$
$G_0 = R_0S_0$
$G_1 = R_1S_1$
$G_2 = R_2S_2$
$G_3 = R_3S_3$
$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

NOTE:
1. + = OR

2590 tbl 08

LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+4} AND OVR (1)

$I_{5,4,3}$	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \nabla C_4$
1	S – R	Same as R + S equations, but substitute $\overline{R}_i$ for R_i in definitions			
2	R – S	Same as R + S equations, but substitute $\overline{S}_i$ for S_i in definitions			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R} \wedge S$	LOW	Same as R ∨ S equations, but substitute $\overline{R}_i$ for R_i in definitions		
6	R ∇ S	Same as $R \vee S$ equations, but substitute $\overline{R}_i$ for R_i in definitions			
7	$\overline{R \nabla S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0 (G_0 + C_n)}$	(2)

NOTES:
1. + = OR.
2. $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \nabla [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{C}_n]$

2590 tbl 09

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to Ground	−0.5 to V_{CC} +0.5	−0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE: 2590 tbl 10

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2590 tbl 26

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions		Min.	Typ.(3)	Max.	Unit
I_{IH}	Input HIGH Current (All Inputs)	V_{CC} = Max. V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current (All Inputs)	V_{CC} = Max. V_{IN} = GND		–	−0.1	−5	µA
V_{OH}	Output High Voltage	V_{CC} = Min.	I_{OH} = −1.0mA (MIL.)	2.4	4.3	–	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA (COM'L.)	2.4	4.3	–	
V_{OL}	Output Low Voltage	V_{CC} = Min.	I_{OL} = 16mA (MIL.)	–	0.3	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA (COM'L.)	–	0.3	0.5	
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level(1)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level(1)		–	–	0.8	V
I_{OZ}	Output Leakage Current	V_{CC} = Max.	V_{OUT} = 0V	–	−0.1	−10	µA
			V_{OUT} = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Max. V_{OUT} = 0V(2)		−30	–	–	mA

2590 tbl 11

NOTES:

1. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
2. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
3. V_{CC} = 5.0V at T_A +25°C.

DC ELECTRICAL CHARACTERISTICS (Cont'd.)

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = VCC –0.2V

Symbol	Parameter	Test Conditions[1]			Min.	Typ. [3]	Max.	Unit
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = H			–	0.5	5.0	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = L			–	0.5	5.0	mA
I_{CCT}	Quiescent Input Power Supply[4] Current (per Input @ TTL High)	V_{CC} = Max., V_{IH} = 3.4V f_{CP} = 0			–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L		MIL. COM'L.	– –	1.5 1.0	2.5 2.0	mA/ MHz
I_{CC}	Total Power Supply Current[5]	V_{CC} = Max.. Outputs Open, $\overline{OE}$ = L CP = 50 % Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ 50% Data Duty Cycle	IDT39C01C f_{CP} = 10MHz	MIL. COM'L.	– –	– –	30 25	mA
			IDT39C01D f_{CP} = 15MHz	MIL. COM'L.	– –	– –	35 30	
			IDT39C01E f_{CP} = 17.5MHz	MIL. COM'L.	– –	– –	40 35	
		V_{CC} = Max.. Outputs Open, $\overline{OE}$ = L CP = 50 % Duty Cycle V_{IH} = 3.4V, V_{IL} = 0.4V 50% Data Duty Cycle	IDT39C01C f_{CP} = 10MHz	MIL. COM'L.	– –	– –	35 30	
			IDT39C01D f_{CP} = 15MHz	MIL. COM'L.	– –	– –	40 35	
			IDT39C01E f_{CP} = 17.5MHz	MIL. COM'L.	– –	– –	45 40	

NOTES:

2590 tbl 12

1. These input levels should only be static tested in a noise-free environment.
2. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
3. V_{CC} = 5.0V at T_A +25°C.
4. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
5. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   $I_{CC} = I_{CCQH}(C_{DH}) + I_{CCQL}(1 - C_{DH}) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$
   C_{DH} = Clock duty cycle high period
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
   N_T = Number of dynamic inputs driven at TTL levels
   f_{CP} = Clock input frequency

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large Vcc current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

5

AC ELECTRICAL CHARACTERISTICS
IDT39C01C

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01C over the –55°C to +125°C and 0°C to +70°C temperature ranges. VCC is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil.	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	32	31	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	31	32	MHz
Minimum Clock LOW Time	15	15	ns
Minimum Clock HIGH Time	15	15	ns
Minimum Clock Period	32	31	ns

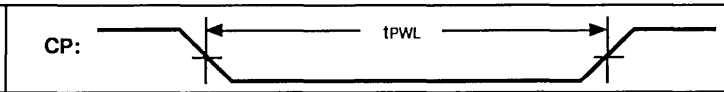
2590 tbl 13

COMBINATIONAL PROPAGATION DELAYS[1] C_L = 50pF

	To Output																
	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3		
From Input	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Address	48	40	48	40	48	40	44	37	48	40	48	40	48	40	–	–	ns
D	37	30	37	30	37	30	34	30	40	38	37	30	37	30	–	–	ns
C_n	25	22	25	22	21	20	–	–	28	25	25	22	28	25	–	–	ns
$I_{0,1,2}$	40	35	40	35	40	35	44	37	44	37	40	35	40	35	–	–	ns
$I_{3,4,5}$	40	35	40	35	40	35	40	35	40	38	40	35	40	35	–	–	ns
$I_{6,7,8}$	29	25	–	–	–	–	–	–	–	–	–	–	29	26	29	26	ns
A Bypass ALU (I = 2XX)	40	35	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ∫	40	35	40	35	40	35	40	35	40	35	40	35	40	35	33	28	ns

2590 tbl 14

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)



Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	15	15	2	1 (3)	30,15 + tPWL (4)		2	1	ns
B Destination Address	15	15	Do not change (2)				2	1	ns
D	– (1)	–	–	–	25	25	0	0	ns
C_n	–	–	–	–	20	20	0	0	ns
$I_{0,1,2}$	–	–	–	–	30	30	0	0	ns
$I_{3,4,5}$	–	–	–	–	30	30	0	0	ns
$I_{6,7,8}$	10	10	Do not change (2)				0	0	ns
$RAM_{0,3}$, $Q_{0,3}$	–	–	–	–	12	12	0	0	ns

NOTES:
2590 tbl 15

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.

OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	25	23	25	23

2590 tbl 16

5

AC ELECTRICAL CHARACTERISTICS
IDT39C01D

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01D over the –55°C to +125°C and 0°C to +70°C temperature ranges. VCC is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil.	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	27	23	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	37	43	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period	27	23	ns

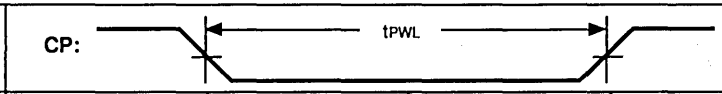
2590 tbl 17

COMBINATIONAL PROPAGATION DELAYS[1] C_L = 50pF

	To Output																
	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3		
From Input	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Address	33	30	33	30	33	30	33	30	33	30	33	30	33	30	–	–	ns
D	24	21	23	20	23	20	21	20	25	24	24	21	25	22	–	–	ns
C_n	18	17	17	16	14	14	–	–	19	18	17	16	19	18	–	–	ns
$I_{0,1,2}$	28	26	27	25	26	24	28	24	29	25	27	24	27	25	–	–	ns
$I_{3,4,5}$	27	26	27	24	26	24	26	24	27	26	26	24	27	26	–	–	ns
$I_{6,7,8}$	18	16	–	–	–	–	–	–	–	–	–	–	21	21	21	21	ns
A Bypass ALU (I = 2XX)	26	24	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ∫	27	24	26	23	26	23	25	23	27	24	26	24	27	24	20	19	ns

2590 tbl 18

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)



Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	11	10	0	0 (3)	24, 11 + tPWL (4)	21, 10 + tPWL (4)	2	1	ns
B Destination Address	11	10	Do not change (2)				2	1	ns
D	– (1)	–	–	–	16	16	0	0	ns
C_n	–	–	–	–	13	13	0	0	ns
$I_{0,1,2}$	–	–	–	–	19	19	0	0	ns
$I_{3,4,5}$	–	–	–	–	19	19	0	0	ns
$I_{6,7,8}$	7	7	Do not change (2)				0	0	ns
$RAM_{0,3}$, $Q_{0,3}$	–	–	–	–	9	9	0	0	ns

2590 tbl 19

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.

OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	16	14	18	16

2590 tbl 20

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AC ELECTRICAL CHARACTERISTICS
IDT39C01E

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01E over the –55°C to +125°C and 0°C to +70°C temperature ranges. VCC is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil.	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	21	20	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	46	50	MHz
Minimum Clock LOW Time	10	8	ns
Minimum Clock HIGH Time	10	8	ns
Minimum Clock Period	21	20	ns

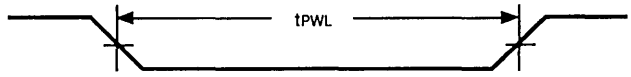
2590 tbl 21

COMBINATIONAL PROPAGATION DELAYS (1) C_L = 50pF

	To Output																
	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3		
From Input	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Address	26	22	26	22	26	22	26	21	29	25	26	22	26	22	–	–	ns
D	18	16	17	15	17	15	16	15	22	20	18	16	19	16	–	–	ns
Cn	13	13	13	12	10	10	–	–	16	15	13	12	14	13	–	–	ns
$I_{0,1,2}$	21	20	20	19	19	18	21	18	25	21	20	18	20	19	–	–	ns
$I_{3,4,5}$	20	20	20	18	19	18	19	18	23	23	19	18	20	20	–	–	ns
$I_{6,7,8}$	13	12	–	–	–	–	–	–	–	–	–	–	16	16	16	16	ns
A Bypass ALU (I = 2XX)	26	24	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ∫	20	18	19	17	19	17	19	17	25	22	19	18	20	18	15	15	ns

2590 tbl 22

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)



Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	8	7	0	0 (3)	18, 8 + tPWL (4)	15, 7 + tPWL (4)	2	1	ns
B Destination Address	8	7	Do not change (2)				2	1	ns
D	– (1)	–	–	–	12	12	0	0	ns
C_n	–	–	–	–	10	10	0	0	ns
$I_{0,1,2}$	–	–	–	–	14	14	0	0	ns
$I_{3,4,5}$	–	–	–	–	14	14	0	0	ns
$I_{6,7,8}$	5	5	Do not change (2)				0	0	ns
$RAM_{0,3}$, $Q_{0,3}$	–	–	–	–	9	9	0	0	ns

2590 tbl 23

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.

OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	14	10	12	12

2590 tbl 24

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 4

2590 tbl 25

Test	Switch
Open Drain Disable Low Enable Low	Closed
All other Tests	Open

2590 tbl 27

INPUT/OUTPUT INTERFACE CIRCUIT

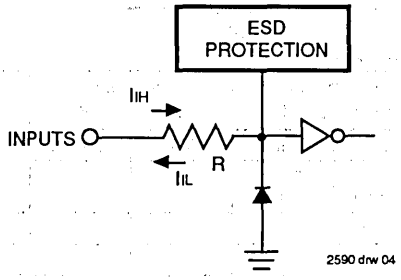


Figure 1. Input Structure (All Inputs)

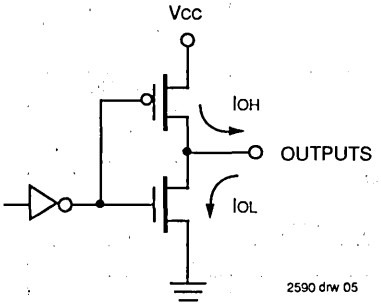


Figure 2. Outputs Structure (All Outputs Except F=0)

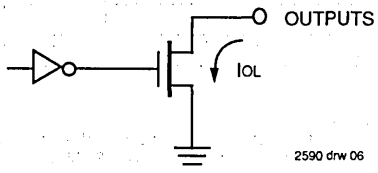
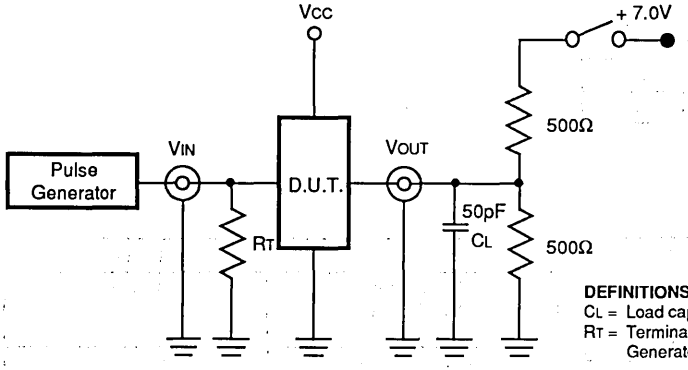


Figure 3. Output Structure (F=0 Only)

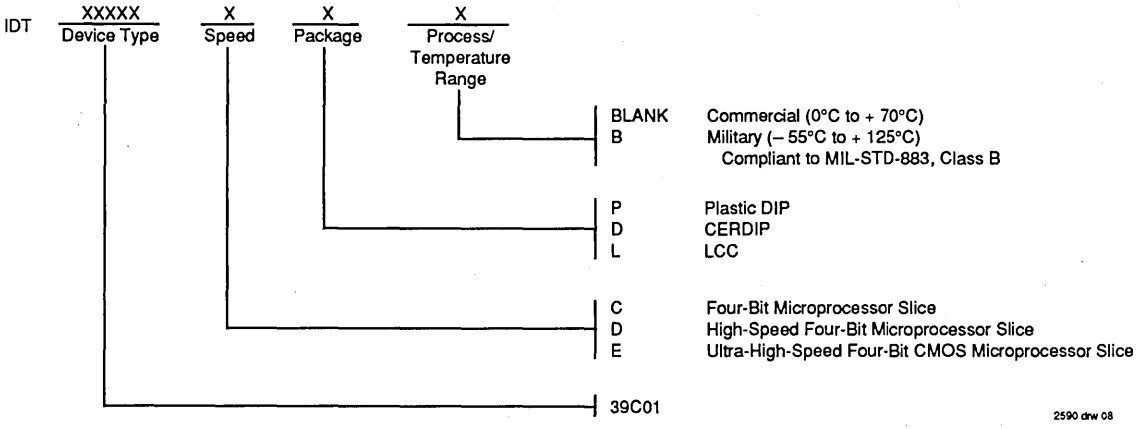
TEST CIRCUIT LOAD



DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator

Figure 4. Switching Test Circuits

ORDERING INFORMATION



5

Integrated Device Technology, Inc.

12-BIT CMOS MICROPROGRAM SEQUENCER

IDT39C10B
IDT39C10C

FEATURES:

- Low-power CEMOS™
  - — Icc (max.)
    Military: 90mA
    Commercial: 75mA
- Fast
  - — IDT39C10B matches 2910A speeds
  - — IDT39C10C 30% speed upgrade
- 33-Deep stack
  - — Accommodates highly nested loops and subroutines
- 12-bit address width
- 12-bit internal loop counter
- 16 powerful microinstructions
- Three output enables control 3-way branch
- Available in 40-pin DIP and 44-pin LCC/PLCC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87708 is listed on this function. Refer to Section 2/page 2-4.

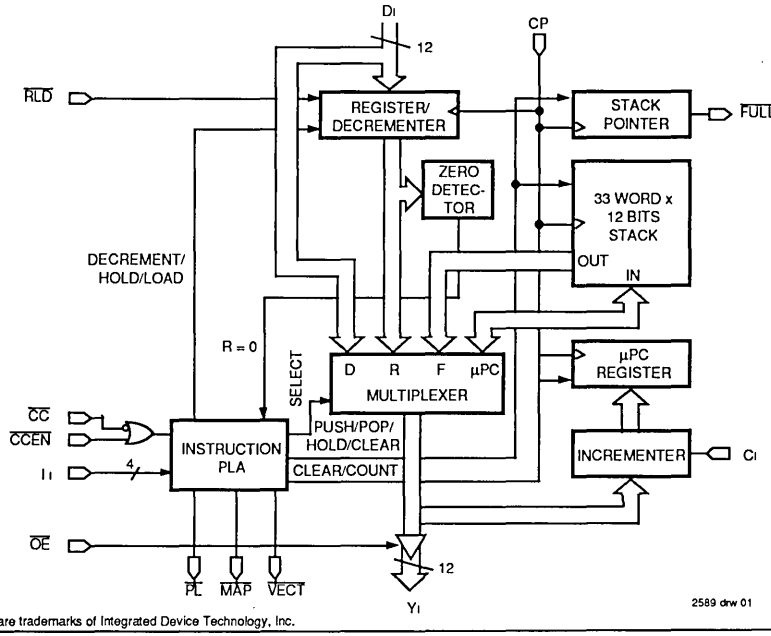
DESCRIPTION:

The IDT39C10 microprogram sequencers are designed for use in high-performance microprogram state machines. These microprogram sequencers are intended for use in controlling the sequence of microinstructions executed in the microprogram memory. The IDT39C10s provide several conditional branch instructions that allow branching to any microinstruction within the 4K microword address space. A 33-deep last-in/first-out stack provides for a very powerful microprogram subroutine return linkage and looping capability. With this depth of a microprogram return stack, the microprogrammer has maximum flexibility in nesting subroutines and loops. The counter contained in the IDT39C10s provides for microinstruction loop counts of up to 4096, in terms of total count length.

The IDT39C10s provide a 12-bit address to the microprogram memory. This microprogram sequencer selects one of four sources for the address. These are (1) the microprogram address register, (2) external direct input, (3) internal register counter and (4) the 33-deep LIFO stack. The microprogram counter usually contains an address that is one greater than the microinstruction currently being executed in the microprogram pipeline register.

The IDT39C10s are fabricated using CEMOS, a CMOS technology designed for high-performance and high-reliability. The devices are pin-compatible, performance-enhanced, functional replacements for the 2910A.

FUNCTIONAL BLOCK DIAGRAM



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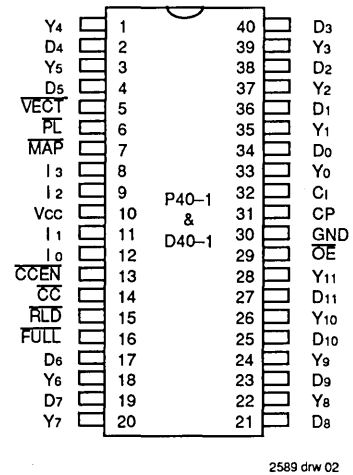
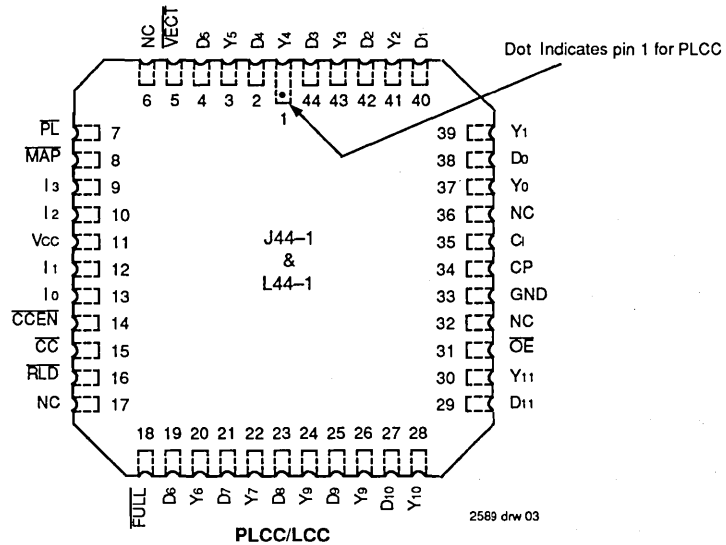
PIN CONFIGURATIONS



DIP
TOP VIEW



PLCC/LCC
TOP VIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
DI	I	Direct input to register/counter and multiplexer D0 is LSB.
II	I	Selects one-of-sixteen instructions.
$\overline{CC}$	I	Used as test criterion. Past test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	I	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the operates as though $\overline{CC}$ were true (LOW).
CI	I	Low order carry input to incrementer for microprogram counter.
$\overline{RLD}$	I	When LOW forces loading of register/ counter regardless of instruction or condition.
$\overline{OE}$	I	Three-state control of YI outputs.
CP	I	Triggers all internal state changes at LOW-to-HIGH edge.
YI	O	Address to microprogram memory. Y0 is LSB, Y11 is MSB.
$\overline{FULL}$	O	Indicates that 33 items are on the stack.
$\overline{PL}$	O	Can select #1 source (usually Pipeline Register) as direct input source.
$\overline{MAP}$	O	Can select #2 source (usually Mapping PROM or PLA) as direct input source.
$\overline{VECT}$	O	Can select #3 source (for example, Interrupt Starting Address) as direct input source.

2589 tbl 01

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PRODUCT DESCRIPTION

The IDT39C10s are high-performance CMOS microprogram sequencers that are intended for use in very high-speed microprogrammable microprocessor applications. The sequencers allow for direct control of up to 4K words of microprogram.

The heart of the microprogram sequencers is a 4-input multiplexer that is used to select one of four address sources to select the next microprogram address. These address sources include the register/counter, the direct input, the microprogram counter or the stack as the source for the address of the next microinstruction.

The register/counter consists of twelve D-type flip-flops which can contain either an address or a count. These edge-triggered flip-flops are under the control of a common clock enable, as well as the four microinstruction control inputs. When the load control (RLD) is LOW, the data at the D inputs is loaded into this register on the LOW-to-HIGH transition of the clock. The output of the register/counter is available at the multiplexer as a possible next address source for the microcode. Also, the terminal count output associated with the register/counter is available at the internal instruction PLA to be used as condition code input for some of the microinstructions. The IDT39C10s contain a microprogram counter that usually contains the address of the next microinstruction compared to that currently being executed. The microprogram counter actually consists of a 12-bit incrementer followed by a 12-bit register. The microprogram counter will increment the address coming out of the sequencer going to the microprogram memory if the carry-in input to this counter is HIGH; otherwise, this address will be loaded into the microprogram counter. Normally, this carry-in input is set to the logic HIGH state so that the incrementer will be active. Should the carry-in input be set LOW, the same address is loaded into the microprogram counter. This is a technique that can be used to allow execution of the same microinstruction several times.

There are twelve D-inputs on the IDT39C10s that go directly to the address multiplexer. These inputs are used to provide a branch address that can come directly from the microcode or some other external source. The fourth input available to the multiplexer for next address control is the 33-deep, 12-bit wide LIFO stack. The LIFO stack provides return address linkage for subroutines and loops. The IDT39C10s contain a built-in stack pointer that always points to the last stack location written. This allows for stack reference operations, usually called loops, to be performed without popping the stack.

The stack pointer internal to the IDT39C10s is actually an up/down counter. During the execution of microinstructions one, four and five, the PUSH operation may occur depending on the state of the condition code input. This causes the stack pointer to be incremented by one and the stack to be written with the required return linkage (the value contained in the microprogram counter). On the microprogram cycle following the PUSH, this new return linkage data that was in the microprogram counter is now at the new location pointed to by the stack pointer. Thus, any time the multiplexer looks at the stack, it will see this data on the top of the stack.

During five different microinstructions, a pop operation associated with the stack may occur. If the pop occurs, the stack pointer is decremented at the next LOW-to-HIGH transition of the clock. A pop decrements the stack pointer which is the equivalent of removing the old information from the top of the stack.

The IDT39C10s are designed so that the stack pointer linkage allows any sequence of pushes, pops or stack references to be used. The depth of the stack can grow to a full 33 locations. After a depth of 33 is reached, the $\overline{\text{FULL}}$ output goes LOW. If further PUSHes are attempted when the stack is full, the stack information at the top of the stack will be destroyed but the stack pointer will not end around. It is necessary to initialize the stack pointer when power is first turned on. This is performed by executing a RESET instruction (Instruction 0). This sets the stack pointer to the stack empty position — the equivalent depth of zero. Similarly, a pop from an empty stack may place unknown data on the Y outputs, but the stack pointer is designed not to end around. Thus, the stack pointer will remain at the 0 or stack empty location if a pop is executed while the stack is already empty.

The IDT39C10s' internal 12-bit register/counter is used during microinstructions eight, nine and fifteen. During these instructions, the 12-bit counter acts as a down counter and the terminal count (count = 0) is used by the internal instruction PLA as an input to control the microinstruction branch test capability. The design of the internal counter is such that, if it is preloaded with a number N and then this counter is used in a microprogram loop, the actual sequence in the loop will be executed N + 1 times. Thus, it is possible to load the counter with a count of 0 and this will result in the microcode being executed one time. The 3-way branch microinstruction, Instruction 15, uses both the loop counter and the external condition code input to control the final source address from the Y outputs of the microprogram sequencer. This 3-way branch may result in the next address coming from the D inputs, the stack or the microprogram counter.

The IDT39C10s provide a 12-bit address at the Y outputs that are under control of the $\overline{\text{OE}}$ input. Thus, the outputs can be put in the three-state mode, allowing the writable control store to be loaded or certain types of external diagnostics to be executed.

In summary, the IDT39C10s are the most powerful microprogram sequencers currently available. They provide the deepest stack, the highest performance and the lowest power dissipation for today's microprogrammed machine design.

IDT39C10 OPERATION

The IDT39C10s are CMOS pin-compatible implementations of the Am2910 and 2910A microprogram sequencers. The IDT39C10's microprogram is functionally identical except that it provides a 33-deep stack to give the microprogrammer more capability in terms of microprogram subroutines and microprogram loops. The definition of each microprogram instruction is shown in the table of instructions. This table

shows the results of each instruction in terms of controlling the multiplexer, which determines the Y outputs, and in controlling the signals that can be used to enable various branch address sources ($\overline{PL}$, $\overline{MAP}$, $\overline{VECT}$). The operation of the register/counter and the 33-deep stack after the next LOW-to-HIGH transition of the clock. The internal multiplexer is used to select which of the internal sources is used to drive the Y outputs. The actual value loaded into the microprogram counter is either identical to the Y output or the Y output value is incremented by 1 and placed in the microprogram counter. This function is under the control of the carry inputs. For each of the microinstruction inputs, only one of the three outputs ($\overline{PL}$, $\overline{MAP}$, or $\overline{VECT}$) will be LOW. Note that this function is not determined by any of the possible condition code inputs. These outputs can be used to control the three-state selection of one of the sources for the microprogram branches.

Two inputs, $\overline{CC}$ and $\overline{CCEN}$, can be used to control the conditional instructions. These are fully defined in the table of instructions. The $\overline{RLD}$ input can be used to load the internal register/counter at any time. When this input is LOW, the data at the D inputs will be loaded into this register/counter on the LOW-to-HIGH transition of the clock. Thus, the $\overline{RLD}$ input overrides the internal hold or decrement operations specified by the various microinstructions. The $\overline{OE}$ input is normally LOW and is used as the three-state enable for the Y outputs. The internal stack in the IDT39C10s is a last-in/first-out memory that is 12-bits in width and 33 words deep. It has a stack pointer that addresses the stack and always points to the value currently on the top of the stack. When instruction 0 (RESET) is executed, the stack pointer is initialized to the top of the stack which is, by definition, the stack empty condition. Thus, the contents of the top of the stack are undefined until the forced PUSH occurs. A pop performed while the stack is empty will not change the stack pointer in any way; however, it will result in unknown data at the Y outputs.

By definition, the stack is full any time 33 more pushes than pops have occurred since the stack was last empty. When this happens, the Full Flag will go LOW. This signal first goes LOW on the microcycle after the 33 pushes occur. When this signal is LOW, no additional pushes should be attempted or the information on the top of the stack will be lost.

THE IDT39C10 INSTRUCTION SET

This data sheet contains a block diagram of the IDT39C10 microprogram sequencers. As can be seen, the devices are controlled by a 4-bit microinstruction word (I_3 - I_0). Normally, this word is supplied from one 4-bit field of the microinstruction word associated with the entire state machine system. These four bits provide for the selection of one of the sixteen powerful instructions associated with selecting the address of the next microinstruction. Unused Y outputs can be left open; however, the corresponding most significant D inputs should be tied to ground for smaller microwords. This is necessary to make sure the internal operation of the counter is proper should less than 4K of microcode be implemented. As shown in the block diagram, the internal instruction PLA uses the four instruction inputs as well as the $\overline{CC}$, $\overline{CCEN}$ and the internal counter = 0 line for controlling the sequencer. This internal instruction PLA provides all of the necessary internal control signals to control each particular part of the microprogram sequencer. The next address at the Y outputs of the IDT39C10s can be from one of four sources. These include the internal microprogram counter, the last-in/first-out stack, the register/counter and the direct inputs.

The following paragraphs will describe each instruction associated with the IDT39C10s. As a part of the discussion, an example of each instruction is shown in Figure 1. The purpose of the examples is to show microprogram flow. Thus, in each example the microinstruction currently being executed has a circle around it. That is, this microinstruction is assumed to be the contents of the pipeline register at the output of the microprogram memory. In these drawings, each of the dots refers to the time that the contents of the microprogram memory word would be in the pipeline register and is currently being executed.

INSTRUCTION 0 – JUMP 0 (JZ)

This instruction is used at power up time or at any restart sequence when the need is to reset the stack pointer and jump to the very first address in microprogram memory. The Jump 0 instruction does not change the contents of the register/counter.

INSTRUCTION 1 – CONDITIONAL JUMP TO SUBROUTINE (CJS)

The Conditional Jump to Subroutine Instruction is the one used to call microprogram subroutines. The subroutine address will be contained in the pipeline register and presented at the D inputs. If the condition code test is passed, a branch is taken to the subroutine. Referring to the flow diagram for the IDT39C10s shown in Figure 1, we see that the content of the microprogram counter is 68. This value is pushed onto the stack and the top of stack pointer is incremented. If the test is failed, this Conditional Jump to Subroutine instruction behaves as a simple continue. That is, the content of microinstruction address 68 is executed next.

INSTRUCTION 2 – JUMP MAP (JMAP)

This sequencer instruction can be used to start different microprogram routines based on the machine instruction opcode. This is typically accomplished by using a mapping PROM as an input to the D inputs on the microprogram sequencer. The JMAP instruction branches to the address appearing on the D inputs. In the flow diagram shown in Figure 1, we see that the branch actually will be the contents of microinstruction 85 and this instruction will be executed next.

INSTRUCTION 3 – CONDITIONAL JUMP PIPELINE (CJP)

The simplest branching control available in the IDT39C10 microprogram sequencers is that of conditional jump to address. In this instruction, the jump address is usually contained in the microinstruction pipeline register and presented to the D inputs. If the test is passed, the jump is

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taken. If the test fails, this instruction executes as a simple continue. In the example shown in the flow diagram of Figure 1, we see that if the test is passed, the next microinstruction to be executed is the content of address 25. If the test is failed, the microcode simply continues to the contents of the next instruction.

INSTRUCTION 4 –
PUSH/CONDITIONAL LOAD COUNTER (PUSH)

With this instruction, the counter can be conditionally loaded during the same instruction that pushes the current value of the microprogram counter on to the stack. Under any condition independent of the conditional testing, the microprogram counter is pushed on to the stack. If the conditional test is passed, the counter will be loaded with the value on the D inputs to the sequencer. If the test fails, the contents of the counter will not change. The PUSH/Conditional Load Counter instruction is used in conjunction with the loop instruction (Instruction 13), the repeat file based on the counter instruction (Instruction 9) or the 3-way branch instruction (Instruction 15).

INSTRUCTION 5 –
CONDITIONAL JUMP TO SUBROUTINE R/PL (JSRP)

Subroutines may be called by a Conditional Jump Subroutine from the internal register or from the external pipeline register. In this instruction, the contents of the microprogram counter are pushed on the stack and the branch address for the subroutine call will taken from either the internal register/counter or the external pipeline register presented to the D inputs. If the conditional test is passed, the subroutine address will be taken from the pipeline register. If the conditional test fails, the branch address is taken from the internal register/counter. An example of this is shown in the flow diagram of Figure 1.

INSTRUCTION 6 –
CONDITIONAL JUMP VECTOR (CJV)

The Conditional Jump Vector instruction is similar to the Jump Map instruction in that it allows a branch operation to a microinstruction as defined from some external source, except that it is conditional. The Jump Map instruction is unconditional. If the conditional test is passed, the branch is taken to the new address on the D inputs. If the conditional test is failed, no branch is taken but rather the microcode simply continues to the next sequential microinstruction. When this instruction is executed, the $\overline{\text{VECT}}$ output is LOW unconditionally. Thus, an external 12-bit field can be enabled on to the D inputs of the microprogram sequencer.

INSTRUCTION 7 –
CONDITIONAL JUMP R/PL (JRP)

The Conditional Jump register/counter or external pipeline register always causes a branch in microcode. This jump will be to one of two different locations in the microcode address space. If the test is passed, the jump will be to the address presented on the D inputs to the microprogram sequencer. If the conditional test fails, the branch will be to the address contained in the internal register/counter.

INSTRUCTION 8 –
REPEAT LOOP COUNTER NOT EQUAL TO 0 (RFCT)

This instruction utilizes the loop counter and the stack to implement microprogrammed loops. The start address for the loop would be initialized by using the PUSH/Conditional Load Counter instruction. Then, when the repeat loop instruction is executed, if the counter is not equal to 0, the next microword address will be taken from the stack. This will cause a loop to be executed as shown in the Figure 1 flow diagram. Each time the microcode sequence goes around the loop, the counter is decremented. When the counter reaches 0, the stack will be popped and the microinstruction address will be taken from the microprogram counter. This instruction performs a timed wait or allows a single sequence to be executed the desired number of times. Remember, the actual number of loops performed is equal to the value in the counter plus 1.

INSTRUCTION 9 –
REPEAT PIPELINE COUNTER NOT EQUAL TO 0 (RPCT)

This instruction is another technique for implementing a loop using the counter. Here, the branch address for the loop is contained in the pipeline register. This instruction does not use the stack in any way as a part of its implementation. As long as the counter is not equal to 0, the next microword address will be taken from the D inputs of the microprogram sequencer. When the counter reaches 0, the internal multiplexer will select the address source from the microprogram counter, thus causing the microcode to continue on and leave the loop.

INSTRUCTION 10 –
CONDITIONAL RETURN (CRTN)

The Conditional Return instruction is used for terminating subroutines. The fact that it is conditional allows the subroutine either to be ended or to continue. If the conditional test is passed, the address of the next microinstruction will be taken from the stack and it will be popped. If the conditional test fails, the next microinstruction address will come from the internal microprogram counter. This is depicted in the flow diagram of Figure 1. It is important to remember that every subroutine call must somewhere be followed by a return from subroutine call in order to have an equal number of pushes and pops on the stack.

INSTRUCTION 11 –
CONDITIONAL JUMP PIPELINE AND POP (CJPP)

The Conditional Jump Pipeline and Pop instruction is a technique for exiting a loop from within the middle of the loop. This is depicted fully in the flow diagram for the IDT39C10s as shown in Figure 1. The conditional test input for this instruction results in a branch being taken if the test is passed. The address selected will be that on the D inputs to the microprogram sequencer and, since the loop is being terminated, the stack will be popped. Should the test be failed on the conditional test inputs, the microprogram will simply continue to the next address as taken from the microprogram counter. The stack will not be affected if the conditional test input is failed.

INSTRUCTION 12 –
LOAD COUNTER AND CONTINUE (LDCT)

The Load Counter and Continue instruction is used to place a value on the D inputs in the register/counter and continue to the next microinstruction.

INSTRUCTION 13 –
TEST END OF LOOP (LOOP)

The Test End of Loop instruction is used as a last instruction in a loop associated with the stack. During this instruction, if the conditional test input is failed, the loop branch address will be that on the stack. Since we may go around the loop a number of times, the stack is not popped. If the conditional test input is passed, then the loop is terminated and the stack is popped. Notice that the loop instruction requires a PUSH to be performed at the instruction immediately prior to the loop return address. This is necessary so as to have the correct address on the stack before the loop operation. It is for this reason that the stack pointer always points to the last thing written on the stack.

INSTRUCTION 14 –
CONTINUE (CONT)

Continue is a simple instruction where the address for the microinstruction is taken from the microprogram counter. This instruction simply causes sequential program flow to the next microinstruction in microcode memory.

INSTRUCTION 15 –
THREE WAY BRANCH (TWB)

The Three-Way Branch instruction is used for looping while waiting for a conditional event to come true. If the event does not come true after some number of microinstructions, then a branch is taken to another microprogram sequence. This is depicted in Figure 1 showing the IDT39C10's flow diagram and is also described in full detail in the IDT39C10's instruction operational summary. Operation of the instruction is such that any time the external conditional test input is passed, the next microinstruction will be that associated with the program counter and the loop will be left. The stack is also popped. Thus, the external test input overrides the other possibilities. Should the external conditional test input not be true, the rest of the operation is controlled by the internal counter. If the counter is not equal to 0, the loop is taken by selecting the address on the top of the stack as the address out of the Y outputs of the IDT39C10s. In addition, the counter is decremented. Should the external conditional test input be failed and the counter also have counted to 0, this instruction "times out". The result is that the stack is popped and a branch is taken to the address presented to the D inputs of the IDT39C10 microprogram sequencers. This address is usually provided by the external pipeline register.

CONDITIONAL TEST

Throughout this discussion we have talked about microcode passing the conditional test. There are actually two inputs associated with the conditional test input. These include the $\overline{CCEN}$ and the $\overline{CC}$ inputs. The $\overline{CCEN}$ input is a condition code enable. Whenever the $\overline{CCEN}$ input is HIGH, the $\overline{CC}$ input is ignored and the device operates as though the $\overline{CC}$ input were true (LOW). Thus, a fail of the external test condition can defined as $\overline{CCEN}$ equals LOW and $\overline{CC}$ equals HIGH. A pass condition is defined as a $\overline{CCEN}$ equal to HIGH or a $\overline{CC}$ equal to LOW. It is important to recognize the full function of the condition code enable and the condition code inputs in order to understand when the test is passed or failed.

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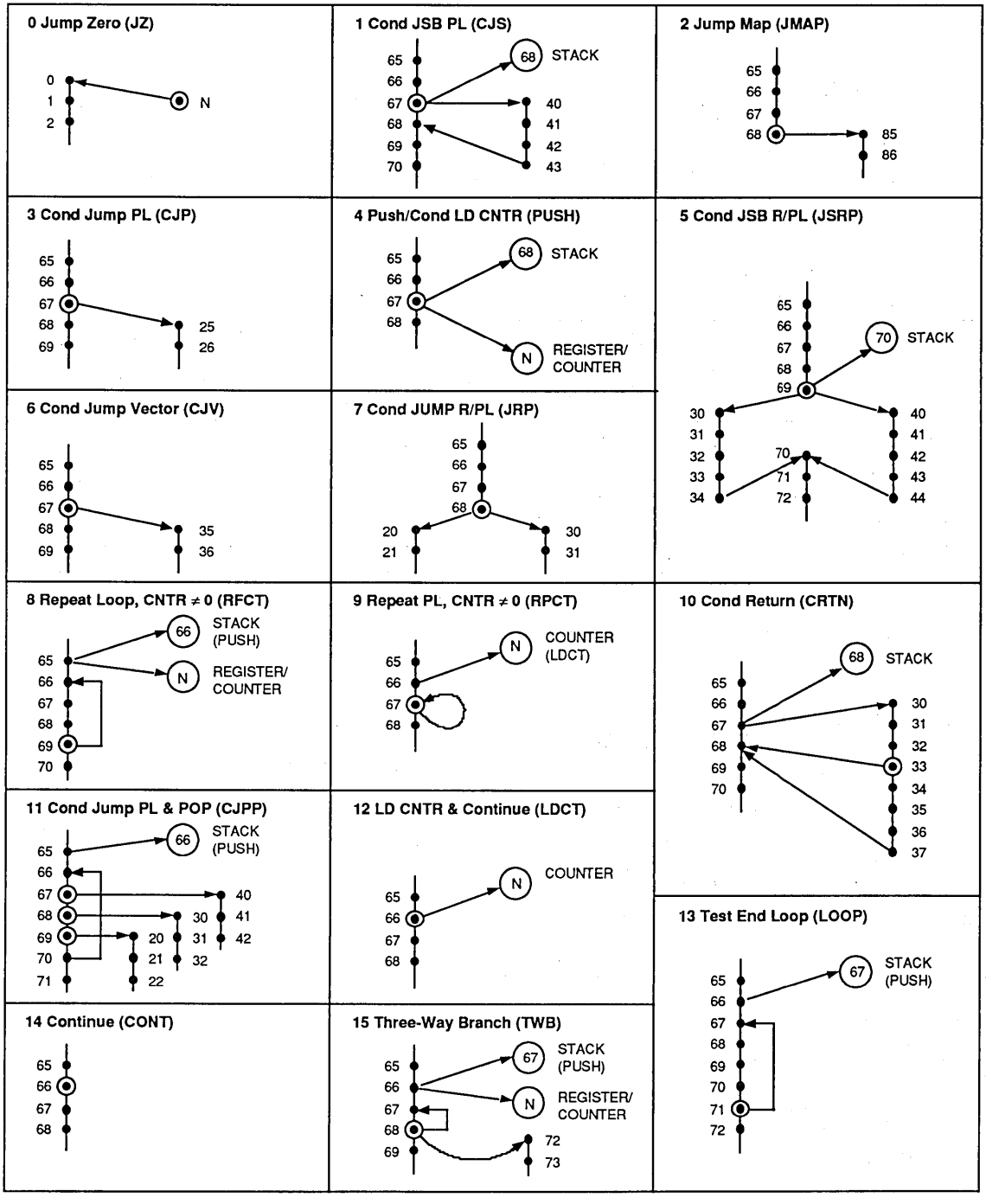
IDT39C10 INSTRUCTION OPERATIONAL SUMMARY

$I_3 - I_0$	Mnemonic	CC	Counter Test	Stack	Address Source	Register/ Counter	Enable Select
0	JZ	X	X	CLEAR	0	NC	$\overline{PL}$
1	CJS	PASS FAIL	X X	PUSH NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
2	JMAP	X	X	NC	D	NC	$\overline{MAP}$
3	CJP	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
4	PUSH	PASS FAIL	X X	PUSH PUSH	PC PC	LOAD NC	$\overline{PL}$ $\overline{PL}$
5	JSRP	PASS FAIL	X X	PUSH PUSH	D R	NC NC	$\overline{PL}$ $\overline{PL}$
6	CJV	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{VECT}$ $\overline{VECT}$
7	JRP	PASS FAIL	X X	NC NC	D R	NC NC	$\overline{PL}$ $\overline{PL}$
8	RFCT	X X	= 0 NOT = 0	POP NC	PC STACK	NC DEC	$\overline{PL}$ $\overline{PL}$
9	RPCT	X X	= 0 NOT = 0	NC NC	PC D	NC DEC	$\overline{PL}$ $\overline{PL}$
10	CRTN	PASS FAIL	X X	POP NC	STACK PC	NC NC	$\overline{PL}$ $\overline{PL}$
11	CJPP	PASS FAIL	X X	POP NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
12	LDCT	X	X	NC	PC	LOAD	$\overline{PL}$
13	LOOP	PASS FAIL	X X	POP NC	PC STACK	NC NC	$\overline{PL}$ $\overline{PL}$
14	CONT	X	X	NC	PC	NC	$\overline{PL}$
15	TWB	PASS PASS FAIL FAIL	= 0 NOT = 0 = 0 NOT = 0	POP POP POP NC	PC PC D STACK	NC DEC NC DEC	$\overline{PL}$ $\overline{PL}$ $\overline{PL}$ $\overline{PL}$

NC = No Charge; DEC = Decrement

2589 tbl 02



2551 drw 05

Figure 1. IDT39C10B Flow Diagrams

IDT39C10 INSTRUCTIONS

$I_3 - I_0$	Mnemonic	Name	Reg/ Cntr Con- tents	FAIL $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH and $\overline{CC}$ = LOW		Reg/ Cntr	Enable
				Y	Stack	Y	Stack		
0	JZ	Jump Zero	X	0	CLEAR	0	CLEAR	HOLD	$\overline{PL}$
1	CJS	Cond JSP PL	X	PC	HOLD	D	PUSH	HOLD	$\overline{PL}$
2	JMAP	Jump Map	X	D	HOLD	D	HOLD	HOLD	$\overline{MAP}$
3	CJP	Cond Jump PL	X	PC	HOLD	D	HOLD	HOLD	$\overline{PL}$
4	PUSH	PUSH/Cond Ld Cntr	X	PC	PUSH	PC	PUSH	(1)	$\overline{PL}$
5	JSRP	Cond JSB R/PL	X	R	PUSH	D	PUSH	HOLD	$\overline{PL}$
6	CJV	Cond Jump Vector	X	PC	HOLD	D	HOLD	HOLD	$\overline{VECT}$
7	JRP	Cond Jump R/PL	X	R	HOLD	D	HOLD	DEC	$\overline{PL}$
8	RFCT	Repeat Loop, CNTR ≠ 0	≠ 0	F	HOLD	F	HOLD	DEC	$\overline{PL}$
			= 0	PC	POP	PC	POP	HOLD	$\overline{PL}$
9	RPCT	Repeat PL, CNTR ≠ 0	≠ 0	D	HOLD	D	HOLD	DEC	$\overline{PL}$
			= 0	PC	HOLD	PC	HOLD	HOLD	$\overline{PL}$
10	CRTN	Cond RTN	X	PC	HOLD	F	POP	HOLD	$\overline{PL}$
11	CJPP	Cond Jump PL & POP	X	PC	HOLD	D	POP	HOLD	$\overline{PL}$
12	LDCT	LD Contr & Continue	X	PC	HOLD	PC	HOLD	LOAD	$\overline{PL}$
13	LOOP	Test End Loop	X	F	HOLD	PC	POP	HOLD	$\overline{PL}$
14	CONT	Continue	X	PC	HOLD	PC	HOLD	HOLD	$\overline{PL}$
15	TWB	Three-Way Branch	≠ 0	F	HOLD	PC	POP	DEC	$\overline{PL}$
			= 0	D	POP	PC	POP	HOLD	$\overline{PL}$

NOTE: 2589 tbl 03
1. If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold; else load. X = Don't Care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to V_{CC} + 0.5	−0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE: 2589 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2589 tbl 05
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level[4]		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level[4]		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–0.1	–5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	–	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA Mil.	2.4	4.3	–	
			I_{OH} = –15mA Com'l.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA	–	GND	V_{LC}	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA Mil.	–	0.3	0.5	
			I_{OL} = 24mA Com'l.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	–0.1	–10	µA
			V_O = V_{CC} (max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V[3]		–30	–	–	mA
I_{CCQH}	Quiescent Power Supply Current CP = H	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = H		–	35	50	mA
I_{CCQL}	Quiescent Power Supply Current CP = L	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = L		–	35	50	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max., V_{IH} = 3.4V, f_{CP} = 0		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max.	MIL.	–	1.0	3.0	mA/
		$V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	COM'L.	–	1.0	1.5	MHz
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{CP} = 10MHz	MIL.	–	45	80	mA
		Outputs Open, $\overline{OE}$ = L CP = 50 % Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	COM'L.	–	45	65	
		V_{CC} = Max., f_{CP} = 10MHz	MIL.	–	50	90	
		Outputs Open, $\overline{OE}$ = L CP = 50 % Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	COM'L.	–	50	75	

2589 tbl 06

NOTES:
1. For conditions shown as Max. or Min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, + 25°C ambient and maximum loading, not production tested.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels should only be static tested in a noise-free environment.
5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock input frequency

5

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large Vcc current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

IDT39C10C AC ELECTRICAL CHARACTERISTICS

I. MINIMUM SET-UP AND HOLD TIMES

	t(S)		t(H)		
Inputs	Com'l.	Mil.	Com'l.	Mil.	Unit
$D_I \rightarrow R$	6	7	0	0	ns
$D_I \rightarrow PC$	13	15	0	0	ns
I_{0-3}	23	25	0	0	ns
$\overline{CC}$	15	18	0	0	ns
$\overline{CCEN}$	15	18	0	0	ns
CI	6	7	0	0	ns
$\overline{RLD}$	11	12	0	0	ns

2589 tbl 07

II. MAXIMUM COMBINATIONAL DELAYS

	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		
Inputs	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
D_{0-11}	12	15	–	–	–	–	ns
I_{0-3}	20	25	13	15	–	–	ns
$\overline{CC}$	16	20	–	–	–	–	ns
$\overline{CCEN}$	16	20	–	–	–	–	ns
CP	28	33	–	–	22	25	ns
$\overline{OE}$ (1)	10/10	13/13	–	–	–	–	ns

NOTE: 2589 tbl 08

1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF. Tested at C_L = 50pF, correlated to 5pF.

III. CLOCK REQUIREMENTS

	Com'l.	Mil.	Unit
Minimum Clock LOW Time	18	20	ns
Minimum Clock HIGH Time	17	20	ns
Minimum Clock Period	35	40	ns

2589 tbl 09

IDT39C10B AC ELECTRICAL CHARACTERISTICS

I. MINIMUM SET-UP AND HOLD TIMES

	t(S)		t(H)		
Inputs	Com'l.	Mil.	Com'l.	Mil.	Unit
$D_I \rightarrow R$	16	16	0	0	ns
$D_I \rightarrow PC$	30	30	0	0	ns
I_{0-3}	35	38	0	0	ns
$\overline{CC}$	24	35	0	0	ns
$\overline{CCEN}$	24	35	0	0	ns
CI	18	18	0	0	ns
$\overline{RLD}$	19	20	0	0	ns

2589 tbl 10

II. MAXIMUM COMBINATIONAL DELAYS

	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		
Inputs	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
D_{0-11}	20	25	–	–	–	–	ns
I_{0-3}	35	40	30	35	–	–	ns
$\overline{CC}$	30	36	–	–	–	–	ns
$\overline{CCEN}$	30	36	–	–	–	–	ns
CP	40	46	–	–	31	35	ns
$\overline{OE}$ (1)	25/27	25/30	–	–	–	–	ns

NOTE: 2589 tbl 11

1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF. Tested at C_L = 50pF, correlated to 5pF.

III. CLOCK REQUIREMENTS

	Com'l.	Mil.	Unit
Minimum Clock LOW Time	20	25	ns
Minimum Clock HIGH Time	20	25	ns
Minimum Clock Period	50	51	ns

2589 tbl 12

IDT39C10B INPUT/OUTPUT INTERFACE CIRCUIT

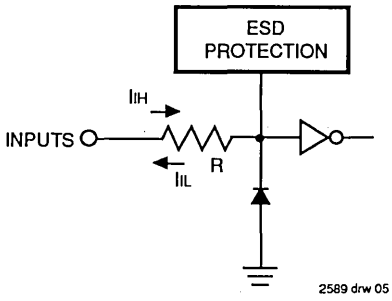


Figure 2. Input Structure

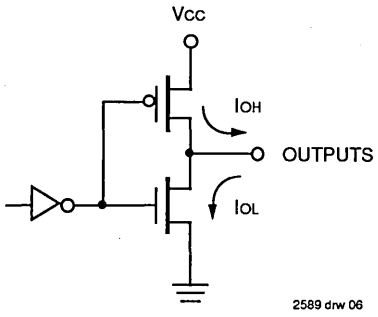


Figure 3. Output Structure

TEST LOAD CIRCUIT

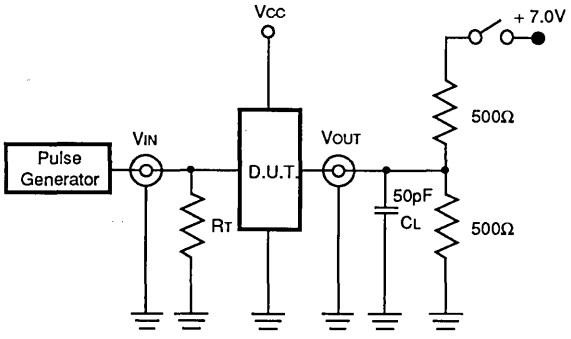


Figure 4. Switching Test Circuits

Test	Switch
Open Drain Disable Low Enable Low	Closed
All other Tests	Open

2589 tbl 14

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 4

2589 tbl 13

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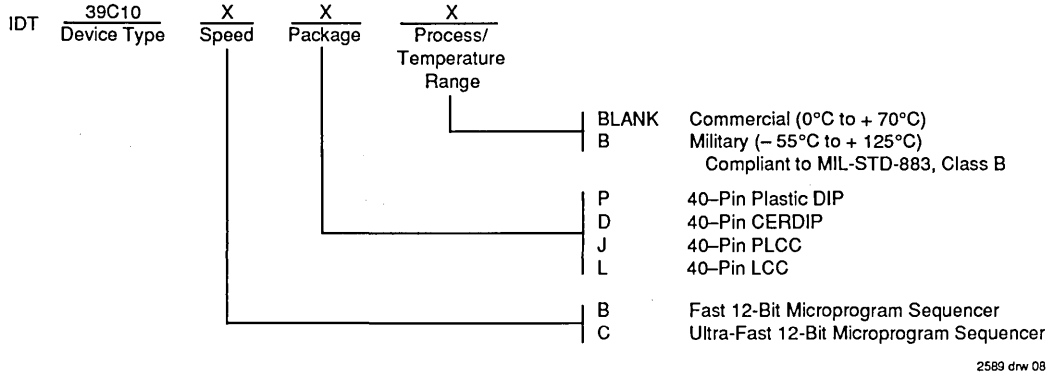
ORDERING INFORMATION



2589 drw 08

Integrated Device Technology, Inc.

16-BIT CMOS MICROPROCESSOR SLICE

IDT49C402
IDT49C402A
IDT49C402B

FEATURES:

- Functionally equivalent to four 2901s and one 2902
- IDT49C402B is 60% faster than four 2901Cs and one 2902A
- Expanded two-address architecture with independent, simultaneous access to two 64 x 16 register files
- Expanded destination functions with 8 new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- Clamp diodes on all inputs provide noise suppression
- Fully cascadable
- 68-pin ceramic PGA, Plastic Leaded Chip Carrier (PLCC), and Ceramic Flatpack (25 mil centers)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C402s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

The IDT49C402s include all of the normal functions associated with standard 2901 bit-slice operation: a) a 3-bit instruction field (I_0, I_1, I_2) which controls the source operand selection for the ALU; b) a 3-bit microinstruction field (I_3, I_4, I_5) used to control the eight possible functions of the ALU; c) eight destination control functions which are selected by the microcode inputs (I_6, I_7, I_8); and d) a tenth microinstruction input, I_9, offering eight additional destination control functions. This I_9 input, in conjunction with I_6, I_7 and I_8, allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU, and having the RAM A data output port available at the Y output pins of the device.

Also featured is an on-chip dual-port RAM that contains 64-words-by-16 bits – four times the number of working registers in a 2901.

The IDT49C402s are fabricated using CEMOS™, a CMOS technology designed for high performance and high reliability. These performance-enhanced devices feature both bipolar speed and bipolar output drive capabilities, while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

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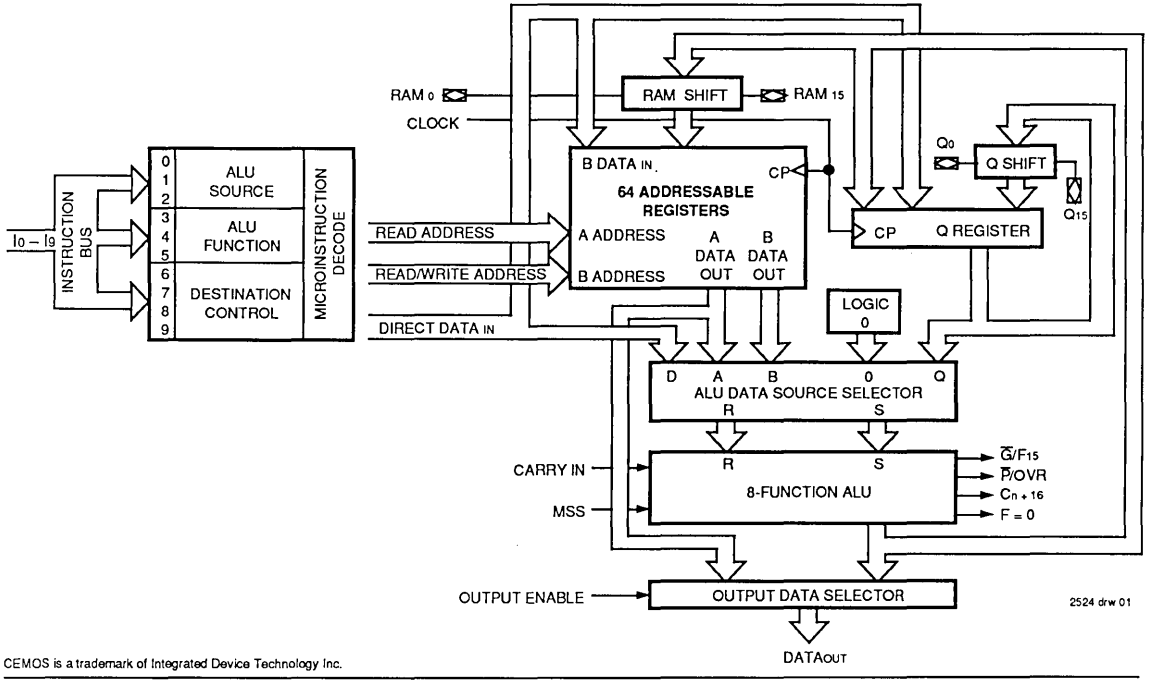
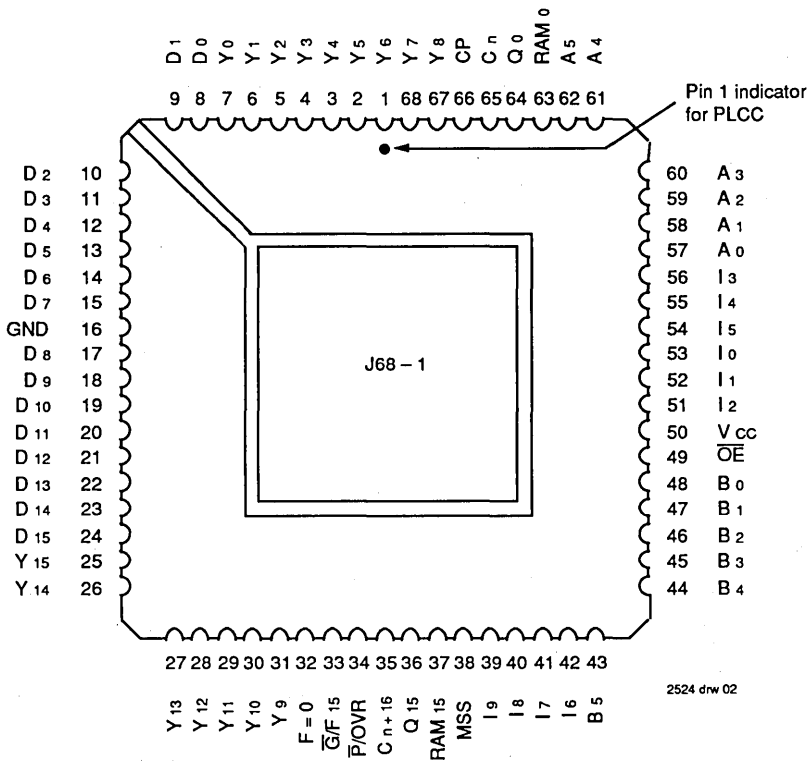
FUNCTIONAL BLOCK DIAGRAM

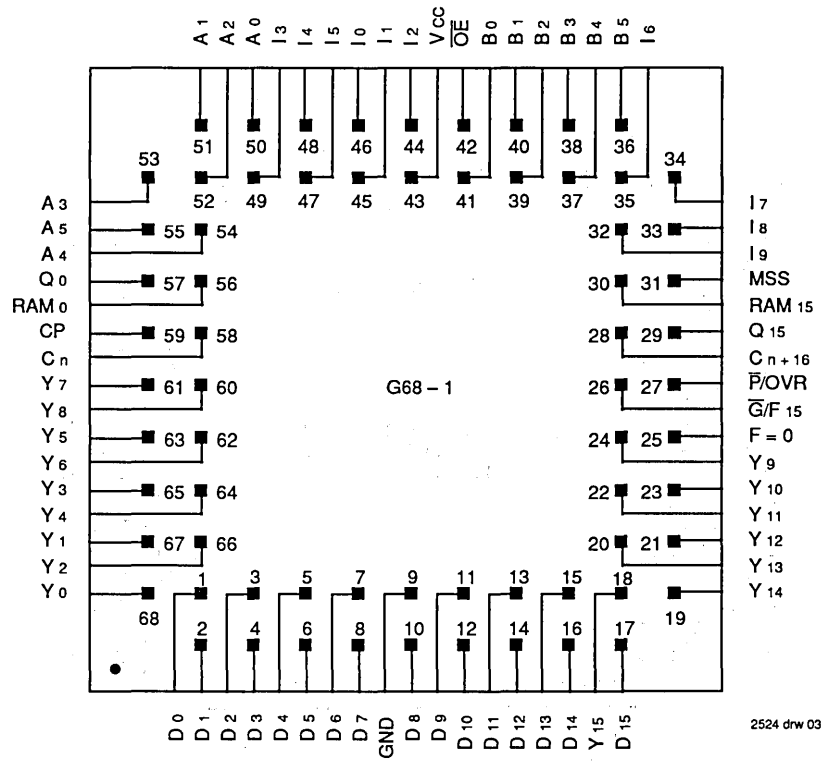


CEMOS is a trademark of Integrated Device Technology Inc.

PIN CONFIGURATIONS

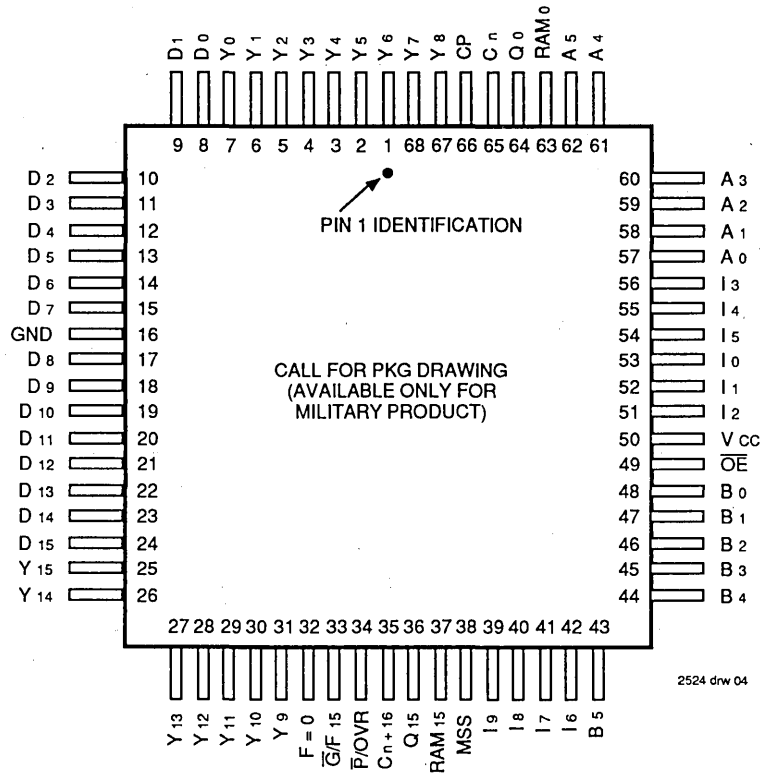


PLCC
TOP VIEW



PGA
TOP VIEW

5



FLATPACK
TOP VIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_0 - A_5	I	Six address inputs to the register file which selects one register and displays its contents through the A port.
B_0 - B_5	I	Six address inputs to the register file which selects one of the registers in the file, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the clock goes LOW.
I_0 - I_9	I	Ten instruction control lines which determine what data source will be applied to the ALU $I_{(0, 1, 2)}$, what function the ALU will perform $I_{(3, 4, 5)}$ and what data is to be deposited in the Q Register or the register file $I_{(6, 7, 8, 9)}$. Original 2901 destinations are selected if I_9 is disconnected in this mode, proper I_9 bias is controlled by an internal pullup resistor to Vcc.
D_0 - D_{15}	I	Sixteen-bit direct data inputs which are the data source for entering external data into the device ALU, Q Register or RAM. D_0 is the LSB.
Y_0 - Y_{15}	O	Sixteen three-state output lines which, when enabled, display either the sixteen outputs of the ALU or the data on the A port of the register stack. This is determined by the destination code $I_{(6, 7, 8, 9)}$.
$\overline{G}/F_{15}$	O	A multipurpose pin which indicates the carry generate ($\overline{G}$) function at the least significant and intermediate slices or as F_{15}, the most significant ALU output (sign bit). $\overline{G}/F_{15}$ selection is controlled by the MSS pin. If MSS = HIGH, F_{15} is enabled. If MSS = LOW, $\overline{G}$ is enabled.
F = 0	O	Open drain output which goes HIGH if the F_0 - F_{15} ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+16}	O	Carry-out of the ALU.
Q_{15} RAM_{15}	I/O	Bidirectional lines controlled by $I_{(6, 7, 8, 9)}$. Both are three-state output drivers connected to the TTL-compatible inputs. When the destination code on $I_{(6, 7, 8, 9)}$ indicates an up shift, the three-state outputs are enabled, the MSB of the Q Register is available on the Q_{15}, pin and the MSB of the ALU output is available on the RAM_{15} pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_{15} and RAM_{15} lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable. When pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{P}$/OVR	O	A multipurpose pin which indicates the carry propagate ($\overline{P}$) output for performing a carry lookahead operation or overflow (OVR) the Exclusive-OR of the carry-in and carry-out of the ALU MSB. OVR, at the most significant end of the word, indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. $\overline{P}$/OVR selection is controlled by the MSS pin. If MSS = HIGH, OVR is enabled. If MSS = LOW, $\overline{P}$ is enabled.
CP	I	The clock input LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 64 x 16 RAM. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.
MSS	I	When HIGH, enables OVR and F_{15} on the $\overline{P}$/OVR and $\overline{G}/F_{15}$ pins. When LOW, enables $\overline{G}$ and $\overline{P}$ on these pins. If left open, internal pullup resistor to Vcc provides declaration that the device is the most significant slice.

2524 tbl 01

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DEVICE ARCHITECTURE

The IDT49C402 CMOS bit-slice microprocessor is configured sixteen bits wide and is cascadable to any number of bits (16, 32, 48, 64). Key elements which make up this 16-bit microprocessor slice are the 1) register file (64 x 16 dual-port RAM) with shifter; 2) ALU and 3) Q Register and shifter.

REGISTER FILE — A 16-bit data word from one of the 64 RAM registers can read from the A port as selected by the 6-bit A address field. Simultaneously, the same data word, or any other word from the 64 RAM registers, can be read from the B port as selected by the 6-bit B address field. New data is written into the RAM register location selected by the B address field during the clock (CP) LOW time. Two sixteen-bit latches hold the RAM A port and B port during the clock (CP) LOW time, eliminating any data races. During clock HIGH, these latches are transparent, reading the data selected by the A and B addresses. The RAM data input field is driven from a four-input multiplexer that selects the ALU output or the D inputs. The ALU output can be shifted up one position, down one position or not shifted. Shifting data operations involves the RAM_{15} and RAM_0 I/O pins. For a shift up operation, the RAM shifter MSB is connected to an enabled RAM_{15} I/O output, while the RAM_0 I/O input is selected as the input to the LSB. During a shift down operation, the RAM shifter LSB is connected to an enabled RAM_0 I/O output, while the RAM_{15} I/O input is selected as the input to the MSB.

ALU — The ALU can perform three binary arithmetic and five logic operations on the two 16-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer, with both having a zero source operand. Both multiplexers are controlled by the $I_{(0, 1, 2)}$ inputs. This multiplexer configuration enables the user to select the various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs $I_{(3, 4, 5)}$ are used to select the ALU function. This high-speed ALU cascades to any word length, providing carry-in (C_n), carry-out (C_{n+16}) and an open-drain (F = 0) output. When all bits of the ALU are zero, the pull-down device of F = 0 is off, allowing a wire-OR of this pin over all cascaded devices. Multipurpose pins $\overline{G}/F_{15}$ and $\overline{P}/OVR$ are aimed at accelerating arithmetic operations. For intermediate and least significant slices, the MSS pin is programmed LOW, selecting the carry-generate ($\overline{G}$) and carry propagate ($\overline{P}$) output functions to be used by carry lookahead logic. For the most significant slice, MSS is programmed HIGH, selecting the sign-bit (F_{15}) and the two's complement overflow (OVR) output functions. The sign bit (F_{15}) allows the ALU sign bit to be monitored without enabling the three-state ALU outputs. The overflow (OVR) output is high when the two's complement arithmetic operation has overflowed into the sign bit, as logically determined from the Exclusive -OR of the carry-in and carry-out of the most significant bit of the ALU. The ALU data outputs are available at the three-state outputs $Y_{(0\text{-}15)}$ or as inputs to the RAM register file and Q register under control of the $I_{(6, 7, 8, 9)}$ instruction inputs.

Q REGISTER — The Q Register is a separate 16-bit file intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 4-input multiplexer. In the no-shift mode, the multiplexer enters the ALU F output or Direct Data into the Q Register. In either the shift up or shift down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_{15}, which operate comparably to the RAM shifter. They are controlled by the $I_{(6, 7, 8, 9)}$ inputs.

The clock input of the IDT49C402 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and $I_{(6, 7, 8, 9)}$ define the RAM as the destination, new data will be written into the RAM file defined by the B address field.

ALU SOURCE OPERAND CONTROL

Mnemonic	Microcode				ALU Source Operands	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

2524 tbl 02

ALU FUNCTION CONTROL

Mnemonic	Microcode				ALU Function	Symbol
	I_2	I_1	I_0	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S – R
SUBS	L	H	L	2	R Minus S	R – S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EX-OR S	R ∇ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R}$ ∇ $\overline{S}$

2524 tbl 04

ALU ARITHMETIC MODE FUNCTIONS

Octal		C_n = L		C_n = H	
$I_{5,4,3}$	$I_{2,1,0}$	Group	Function	Group	Function
0	0	ADD	A + Q	ADD plus one	A + Q + 1
0	1		A + B		A + B + 1
0	5		D + A		D + A + 1
0	6		D + Q		D + Q + 1
0	2	PASS	Q	Increment	Q + 1
0	3		B		B + 1
0	4		A		A + 1
0	7		D		D + 1
1	2	Decrement	Q – 1	PASS	Q
1	3		B – 1		B
1	4		A – 1		A
2	7		D – 1		D
2	2	1's Comp.	–Q – 1	2's Comp. (Negate)	–Q
2	3		–B – 1		–B
2	4		–A – 1		–A
1	7		–D – 1		–D
1	0	Subtract (1's Comp)	Q – A – 1	Subtract (2's Comp)	Q – A
1	1		B – A – 1		B – A
1	5		A – D – 1		A – D
1	6		Q – D – 1		Q – D
2	0		A – Q – 1		A – Q
2	1		A – B – 1		A – B
2	5		D – A – 1		D – A
2	6		D – Q – 1		D – Q

2524 tbl 03

ALU LOGIC MODE FUNCTIONS

Octal		Group	Function
$I_{5,4,3}$	$I_{2,1,0}$		
4	0	AND	A ∧ Q
4	1		A ∧ B
4	5		D ∧ A
4	6		D ∧ Q
3	0	OR	A ∨ Q
3	1		A ∨ B
3	5		D ∨ A
3	6		D ∨ Q
6	0	EX–OR	A ∇ Q
6	1		A ∇ B
6	5		D ∇ A
6	6		D ∇ Q
7	0	EX–NOR	$\overline{A}$ ∇ $\overline{Q}$
7	1		$\overline{A}$ ∇ $\overline{B}$
7	5		$\overline{D}$ ∇ $\overline{A}$
7	6		$\overline{D}$ ∇ $\overline{Q}$
7	2	INVERT	$\overline{Q}$
7	3		$\overline{B}$
7	4		$\overline{A}$
7	7		$\overline{D}$
6	2	PASS	Q
6	3		B
6	4		A
6	7		D
3	2	PASS	Q
3	3		B
3	4		A
3	7		D
4	2	"ZERO"	0
4	3		0
4	4		0
4	7		0
5	0	MASK	$\overline{A}$ ∧ Q
5	1		$\overline{A}$ ∧ B
5	5		$\overline{D}$ ∧ A
5	6		$\overline{D}$ ∧ Q

2524 tbl 05

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SOURCE OPERAND AND ALU FUNCTION MATRIX(1)

Octal	ALU	$I_{2,1,0}$ Octal							
		0	1	2	3	4	5	6	7
Octal	ALU	ALU Source							
$I_{5,4,3}$	Function	A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	$C_n = L$ R Plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	$C_n = H$	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	$C_n = L$ S Minus R	Q − A − 1	B − A − 1	Q − 1	B − 1	A − 1	A − D − 1	Q − D − 1	−D − 1
	$C_n = H$	Q − A	B − A	Q	B	A	A − D	Q − D	−D
2	$C_n = L$ R Minus S	A − Q − 1	A − B − 1	−Q − 1	−B − 1	−A − 1	D − A − 1	D − Q − 1	D − 1
	$C_n = H$	A − Q	A − B	−Q	−B	−A	D − A	D − Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∇ Q	A ∇ B	Q	B	A	D ∇ A	D ∇ Q	D
7	R EX-NOR S	$\overline{A}$ ∇ $\overline{Q}$	$\overline{A}$ ∇ $\overline{B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D}$ ∇ $\overline{A}$	$\overline{D}$ ∇ $\overline{Q}$	$\overline{D}$

NOTE:
1. + = Plus; − = Minus; ∧ = AND; ∇ = EX-OR; ∨ = OR.

2524 tbl 06

ALU DESTINATION CONTROL(1)

	Microcode					RAM Function		Q Register Function			RAM Shifter		Q Shifter		
Mnemonic	I_9	I_8	I_7	I_6	Hex Code	Shift	Load	Shift	Load	Y Output	RAM_0	RAM_{15}	Q_0	Q_{15}	
OREG	H	L	L	L	8	X	NONE	NONE	F → Q	F	X	X	X	X	Existing 2901
NOP	H	L	L	H	9	X	NONE	X	NONE	F	X	X	X	X	Functions
RAMA	H	L	H	L	A	NONE	F → B	X	NONE	A	X	X	X	X	
RAMF	H	L	H	H	B	NONE	F → B	X	NONE	F	X	X	X	X	
RAMQD	H	H	L	L	C	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_{15}	Q_0	IN_{15}	
RAMD	H	H	L	H	D	DOWN	F/2 → B	X	NONE	F	F_0	IN_{15}	Q_0	X	
RAMQU	H	H	H	L	E	UP	2F → B	UP	2Q → Q	F	IN_0	F_{15}	IN_0	Q_{15}	
RAMU	H	H	H	H	F	UP	2F → B	X	NONE	F	IN_0	F_{15}	X	Q_{15}	
DFF	L	L	L	L	0	NONE	D → B	NONE	F → Q	F	X	X	X	X	New Added
DFA	L	L	L	H	1	NONE	D → B	NONE	F → Q	A	X	X	X	X	IDT49C402
FDF	L	L	H	L	2	NONE	F → B	NONE	D → Q	F	X	X	X	X	Functions
FDA	L	L	H	H	3	NONE	F → B	NONE	D → Q	A	X	X	X	X	
XQDF	L	H	L	L	4	X	NONE	DOWN	Q/2 → Q	F	X	X	Q_0	IN_{15}	
DXF	L	H	L	H	5	NONE	D → B	X	NONE	F	X	X	Q_0	X	
XQUF	L	H	H	L	6	X	NONE	UP	2Q → Q	F	X	X	IN_0	Q_{15}	
XDF	L	H	H	H	7	X	NONE	NONE	D → Q	F	X	X	X	Q_{15}	

NOTE:
1. X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the impedance state.
   B = Register Addressed by B inputs.
   UP is toward MSB; DOWN is toward LSB.

2524 tbl 07

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to Ground	−0.5 to V_{CC} + 0.5	−0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2524 tbl 08

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2524 tbl 09

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ. (2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic High Level (4)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level (4)		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	−0.1	−5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −300µA (5)	–	–	–	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL.	2.4	4.3	–	
			I_{OH} = −8mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA (5)	–	–	–	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA MIL.	–	0.3	0.5	
			I_{OL} = 10mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	−0.1	−10	µA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V (3)		−15	−30	–	mA

NOTES: 2524 tbl 10

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels should only be static tested in a noise-free environment.
5. Guaranteed by design, not production tested.

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DC ELECTRICAL CHARACTERISTICS (IDT49C402 STANDARD POWER) VERSION (Cont'd)

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = VCC – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQH}	Quiescent Power Supply Current	V_{CC} = Max.	MIL.	–	150	265	mA
	CP = H (CMOS Inputs)	$V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	COM'L.	–	150	215	
		f_{CP} = 0, CP = H					
I_{CCQL}	Quiescent Power Supply Current	V_{CC} = Max.	MIL.	–	80	135	mA
	CP = L (CMOS Inputs)	$V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	COM'L.	–	80	110	
		f_{CP} = 0, CP = L					
I_{CCT}	Quiescent Input Power Supply[6]	V_{CC} = Max., V_{IH} = 3.4V, f_{CP} = 0	MIL.	–	0.3	0.5	mA/
	Current (per Input @ TTL High)		COM'L.	–	0.3	0.5	Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max.	MIL.	–	2.0	3.0	mA/
		$V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	COM'L.	–	2.0	2.5	MHz
		Outputs Open, $\overline{OE}$ = L					
I_{CC}	Total Power Supply Current[7]	V_{CC} = Max., f_{CP} = 10MHz	MIL.	–	135	255	mA
		Outputs Open, $\overline{OE}$ = L	COM'L.	–	135	190	
		CP = 50 % Duty cycle					
		$V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$					
		V_{CC} = Max., f_{CP} = 10MHz	MIL.	–	145	265	
		Outputs Open, $\overline{OE}$ = L	COM'L.	–	145	200	
		CP = 50 % Duty cycle					
		V_{IH} = 3.4V, V_{IL} = 0.4V					

2524 tbl 11

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
5. Guaranteed by design, not production tested.
6. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
7. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   $I_{CC} = I_{CCQH} (CD_H) + I_{CCQL} (1 - CD_H) + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{CP})$
   CD_H = Clock duty cycle high period
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
   N_T = Number of dynamic inputs driven at TTL levels
   f_{CP} = Clock input frequency

DC ELECTRICAL CHARACTERISTICS (IDT49C402 LOW POWER) VERSION (Cont'd)

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQH}	Quiescent Power Supply Current	V_{CC} = Max.	MIL.	–	–	10	mA
	CP = H (CMOS Inputs)	$V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	COM'L.	–	–	10	
		f_{CP} = 0, CP = H					
I_{CCQL}	Quiescent Power Supply Current	V_{CC} = Max.	MIL.	–	–	10	mA
	CP = L (CMOS Inputs)	$V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	COM'L.	–	–	10	
		f_{CP} = 0, CP = L					
I_{CCT}	Quiescent Input Power Supply[6]	V_{CC} = Max., V_{IH} = 3.4V, f_{CP} = 0	MIL.	–	–	1.2	mA/
	Current (per Input @ TTL High)		COM'L.	–	–	0.85	Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max.	MIL.	–	–	7.5	mA/
		$V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	COM'L.	–	–	4.5	MHz
		Outputs Open, $\overline{OE}$ = L					
I_{CC}	Total Power Supply Current[7]	V_{CC} = Max.., f_{CP} = 10MHz	MIL.	–	–	85	mA
		Outputs Open, $\overline{OE}$ = L	COM'L.	–	–	55	
		CP = 50 % Duty cycle					
		$V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$					
		V_{CC} = Max.., f_{CP} = 10MHz	MIL.	–	–	130	
		Outputs Open, $\overline{OE}$ = L	COM'L.	–	–	95	
		CP = 50 % Duty cycle					
		V_{IH} = 3.4V, V_{IL} = 0.4V					

2524 tbl 12

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
5. Guaranteed by design, not production tested.
6. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
7. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   $I_{CC} = I_{CCQH}(C_{DH}) + I_{CCQL}(1 - C_{DH}) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$
   C_{DH} = Clock duty cycle high period
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
   N_T = Number of dynamic inputs driven at TTL levels
   f_{CP} = Clock input frequency

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic testing environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.

5

AC ELECTRICAL CHARACTERISTICS IDT49C402 STANDARD AND LOW POWER VERSION

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402 over the –55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil. (6)	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	50	48	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)	20	21	MHz
Minimum Clock LOW Time	30	30	ns
Minimum Clock HIGH Time	20	20	ns
Minimum Clock Period	50	48	ns

2524 tbl 13

MAXIMUM COMBINATIONAL PROPAGATION DELAYS(1) C_L = 50pF

From Input	To Output: Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		(MSS = H) OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Address	52	47	47	42	52	47	47	42	38	34	52	47	44	40	–	–	ns
D	35	32	34	31	35	32	34	31	27	25	35	32	28	26	–	–	ns
C_n	29	26	–	–	29	26	27	25	20	18	29	26	23	21	–	–	ns
$I_{0,1,2}$	41	37	30	27	41	37	38	35	29	26	41	37	30	27	–	–	ns
$I_{3,4,5}$	40	36	28	26	40	36	37	34	27	25	40	36	28	26	–	–	ns
$I_{6,7,8,9}$	26	24	–	–	–	–	–	–	–	–	–	–	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ∫	42	38	41	37	42	38	41	37	30	27	42	38	41	37	25	23	ns

2524 tbl 14

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

	CP:								
	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		
Input	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Source Address	20	18	2 (3)	1 (3)	50	50	2	1	ns
B Destination Address	20	18	Do not change (2)				2	1	ns
D	– (1)	–	–	–	30/40 (5)	26/36 (5)	2	1	ns
C_n	–	–	–	–	35	32	0	0	ns
$I_{0,1,2}$	–	–	–	–	45	41	0	0	ns
$I_{3,4,5}$	–	–	–	–	45	41	0	0	ns
$I_{6,7,8,9}$	12	11	Do not change (2)				0	0	ns
$RAM_{0,15}$, $Q_{0,15}$	–	–	–	–	12	11	0	0	ns

2524 tbl 15

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

5

AC ELECTRICAL CHARACTERISTICS IDT49C402A STANDARD AND LOW POWER VERSION

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402A over the –55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil.(6)	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)(6)	23	22	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)(6)	35	41	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period(6)	36	31	ns

2524 tbl 16

MAXIMUM COMBINATIONAL PROPAGATION DELAYS(1) CL = 50pF

From Input	To Output: Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		(MSS = H) OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Address	41	37	39	35	41	37	41	37	37	34	41	37	40	36	–	–	ns
D	32	29	29	26	29	26	31	28	27	25	32	29	28	26	–	–	ns
C_n	28	25	–	–	26	24	25	23	20	18	29	26	23	21	–	–	ns
$I_{0,1,2}$	35	32	30	27	35	32	34	31	29	26	35	32	30	27	–	–	ns
$I_{3,4,5}$	35	32	28	26	34	31	34	31	27	25	35	32	28	26	–	–	ns
$I_{6,7,8,9}$	25	23	–	–	–	–	–	–	–	–	–	–	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ∫	34	31	31	28	33	30	34	31	30	27	34	31	34	31	25	23	ns

2524 tbl 17

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

	CP: 								
	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		
Input	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Source Address	11	10	2 (3)	1 (3)	25	21	2	1	ns
B Destination Address	11	10	Do not change (2)				2	1	ns
D	– (1)	–	–	–	12/22 (5)	10/20 (5)	2	1	ns
C_n	–	–	–	–	17	15	0	0	ns
$I_{0,1,2}$	–	–	–	–	28	25	0	0	ns
$I_{3,4,5}$	–	–	–	–	28	25	0	0	ns
$I_{6,7,8,9}$	11	10	Do not change (2)				0	0	ns
$RAM_{0,15}$, $Q_{0,15}$	–	–	–	–	12	11	0	0	ns

2524 tbl 18

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

5

AC ELECTRICAL CHARACTERISTICS IDT49C402B LOW POWER VERSION

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402B over the –55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil.(6)	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)(6)	22	19	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)(6)	52	60	MHz
Minimum Clock LOW Time	11	9	ns
Minimum Clock HIGH Time	11	9	ns
Minimum Clock Period(6)	24	20	ns

2524 tbl 19

MAXIMUM COMBINATIONAL PROPAGATION DELAYS(1) C_L = 50pF

From Input	To Output: Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		(MSS = H) OVR		C_{n+16}		F = 0		RAM0 RAM15		Q0 Q15		
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Address	33	28	31	26	31	28	31	28	28	26	31	28	32	29	–	–	ns
D	26	23	23	21	23	21	25	22	22	20	26	23	24	23	–	–	ns
C_n	22	20	–	–	20	18	19	17	15	14	22	20	18	17	–	–	ns
$I_{0,1,2}$	28	26	24	22	28	26	27	25	23	21	28	26	26	24	–	–	ns
$I_{3,4,5}$	28	26	22	21	27	25	27	25	22	20	28	26	25	23	–	–	ns
$I_{6,7,8,9}$	20	18	–	–	–	–	–	–	–	–	–	–	16	14	16	14	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	24	22	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ↓	27	25	25	22	26	24	27	25	–	–	27	25	27	25	–	–	ns

2524 tbl 20

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	10	9	2(3)	1(3)	20	18	2	1	ns
B Destination Address	10	9	Do not change(2)				2	1	ns
D	–(1)	–	–	–	12/22(5)	10/20(5)	2	1	ns
C_n	–	–	–	–	16	14	0	0	ns
$I_{0,1,2}$	–	–	–	–	26	24	0	0	ns
$I_{3,4,5}$	–	–	–	–	26	24	0	0	ns
$I_{6,7,8,9}$	10	9	Do not change(2)				0	0	ns
$RAM_{0,15}$, $Q_{0,15}$	–	–	–	–	12	10	0	0	ns

2524 tbl 21

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

IDT49C402B
MAX. OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)
Tested at C_L = 50pF, correlated to 5pF

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	18	16	15	13

2524 tbl 22

IDT49C402A
MAX. OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)
Tested at C_L = 50pF, correlated to 5pF

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	22	20	20	18

2524 tbl 23

IDT49C402
MAX. OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)
Tested at C_L = 50pF, correlated to 5pF

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	25	23	25	23

2524 tbl 24

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2524 tbl 25

CRITICAL SPEED PATH ANALYSIS

Critical speed paths are for the IDT49C402B versus the equivalent bipolar circuit implementation using four 2901Cs and one 2902A is shown below.

The IDT49C402B operates faster than the theoretically achievable values of the discrete bipolar implementation. Actual speed values for the discrete bipolar circuit will increase due to on-chip/off-chip circuit board delays.

TIMING COMPARISION: IDT49C402B vs 2901C w/2902A

16–Bit µP System	Data Path (Com'l.)		Data Path (Mil.)		Unit
	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	
Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	≥ 83.5	ns
IDT49C402B	28	23	31	25	ns
Speed Savings	43	48	52	55	ns

2524 tbl 26

TIMING COMPARISION: IDT49C402A vs 2901C w/2902A

16–Bit µP System	Data Path (Com'l.)		Data Path (Mil.)		Unit
	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	
Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	≥ 83.5	ns
IDT49C402A	37	36	41	25	ns
Speed Savings	34	35	42.5	43.5	ns

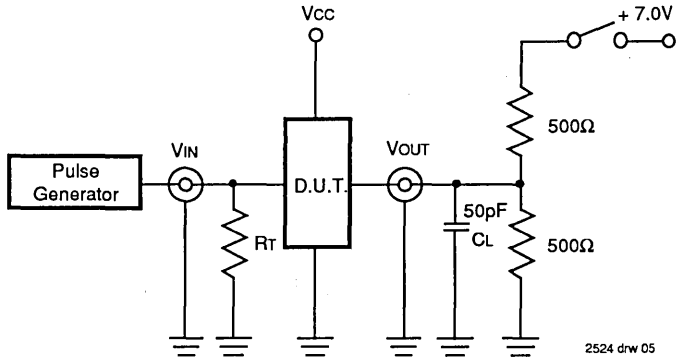
2524 tbl 27

TIMING COMPARISION: IDT49C402 vs 2901C w/2902A

16–Bit µP System	Data Path (Com'l.)		Data Path (Mil.)		Unit
	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	
Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	≥ 83.5	ns
IDT49C402A	47	40	52	44	ns
Speed Savings	24	31	31.5	39.5	ns

2524 tbl 28

TEST CIRCUIT LOAD



DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_L = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 1. Switching Test Circuit (All Outputs)

INPUT/OUTPUT INTERFACE CIRCUIT

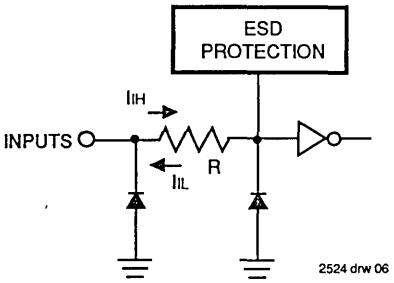


Figure 2. Input Structure (All Inputs)

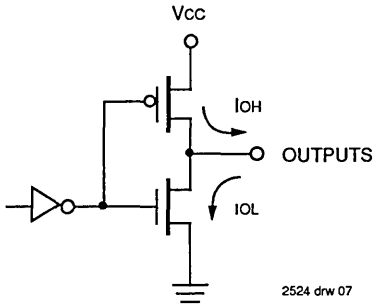


Figure 3. Outputs Structure (All Outputs Except F = 0)

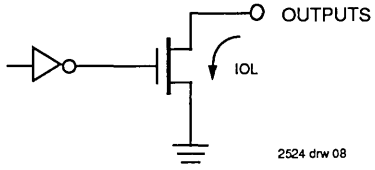
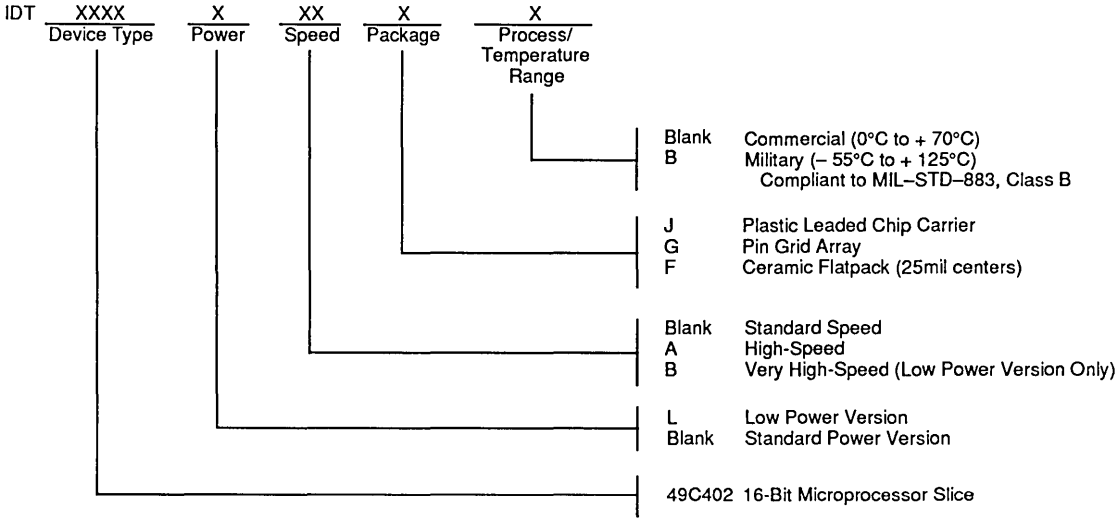


Figure 4. Outputs Structure (F = 0)

5

ORDERING INFORMATION



2524 drw 09

Integrated Device Technology, Inc.

16-BIT CMOS MICROPROGRAM SEQUENCER

IDT49C410
IDT49C410A

FEATURES:

- 16-bit wide address path
  - — Address up to 65,536 words of microprogram memory
- 16-bit loop counter
  - — Pre-settable down-counter for counting loop iterations and repeating instructions
- Low-power CEMOS™
  - — Icc (max.)
    Military: 90mA
    Commercial: 75 mA
- Fast
  - — IDT49C410 meets 2910A speeds
  - — IDT49C410A is a 30% speed upgrade
- 33-deep stack
  - — Accommodates highly nested microcode
- 16 powerful microinstructions
- Available in 48-pin, 600 mil plastic and sidebraze DIP, 52-pin PLCC and 48-pin Flatpack
- Three enables control branch address sources
- Four address sources
- 2910A instruction compatibility
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88643 is listed for this function

DESCRIPTION:

The IDT49C410s are architecture and function code compatible to the 2910A with an expanded 16-bit address path, thus allowing for programs up to 65,536 words in length. They are microprogram address sequencers intended for controlling the sequence of execution of microinstructions stored in the microprogram memory. Besides the capability of sequential access, they provide conditional branching to any microinstruction within their 65,536 microword range.

The 33-deep stack provides microsubroutine return linkage and looping capability. The deep stack can be used for highly nested microcode applications. Microinstruction loop count control is provided with a count capability of 65,536.

During each microinstruction, the microprogram controller provides a 16-bit address from one of four sources: 1) the microprogram address register (µPC), which usually contains an address one greater than the previous address; 2) an external (direct) input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a last-in/first-out stack (F).

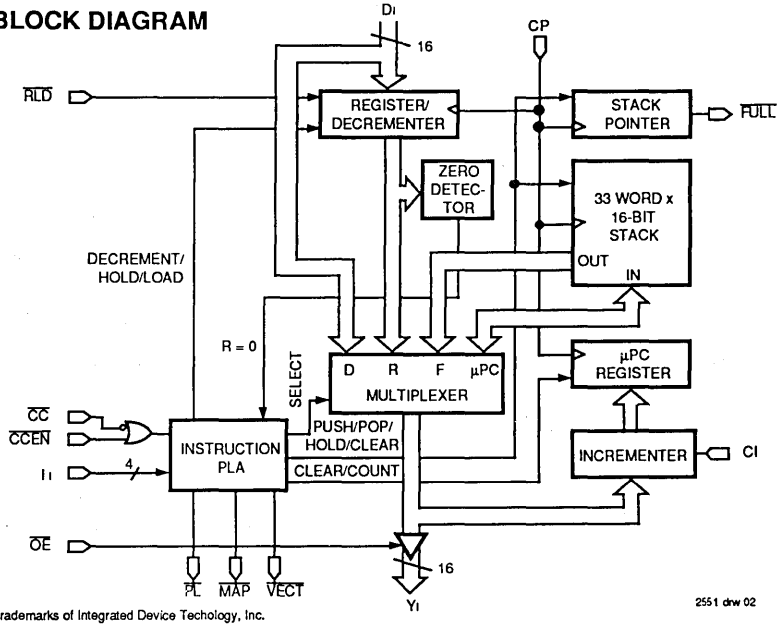
The IDT49C10s are fabricated using CEMOS, a CMOS technology designed for high-performance and high-reliability.

The IDT49C410s are pin-compatible, performance-enhanced, easily upgradable versions of the 2910A.

The IDT49C410s are available in 48-pin DIP (600 mil x 100 mil centers), 52-pin PLCC and 48-pin flatpack.

5

FUNCTIONAL BLOCK DIAGRAM



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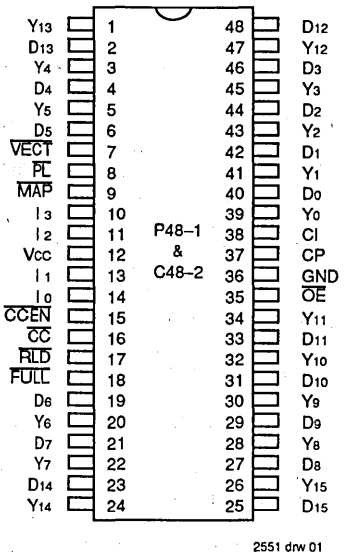
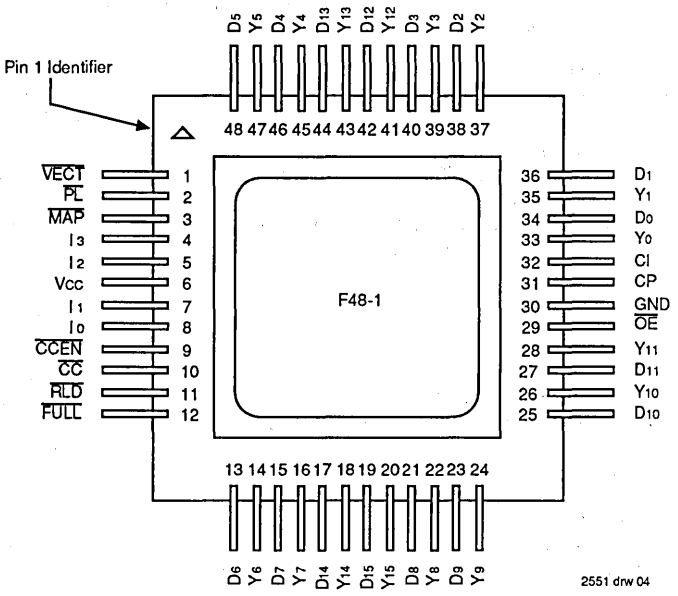
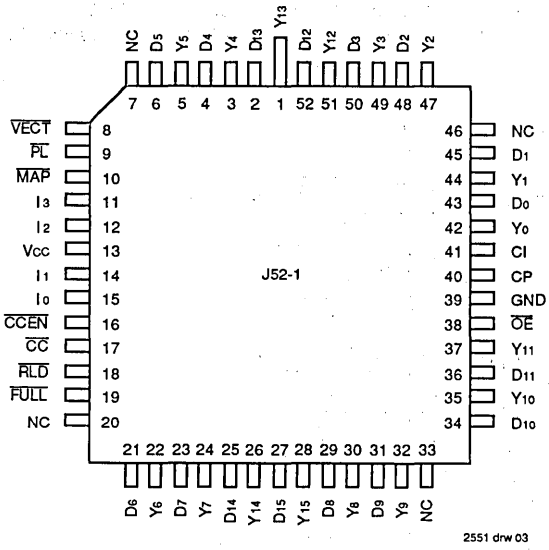
PIN CONFIGURATIONS



DIP
TOP VIEW



FLATPACK
TOP VIEW



PLCC
TOP VIEW

IDT49C410 PIN DESCRIPTIONS

Pin Name	I/O	Description
DI	I	Direct input to register/counter and multiplexer D0 is LSB.
I1	I	Selects one-of-sixteen instructions.
$\overline{CC}$	I	Used as test criterion. Past test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	I	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	I	Low order carry input to incrementer for microprogram counter.
$\overline{RLD}$	I	When LOW forces loading of register/counter regardless of instruction or condition.
$\overline{OE}$	I	Three-state control of YI outputs.
CP	I	Triggers all internal state changes at LOW-to-HIGH edge.
YI	O	Address to microprogram memory. Y0 is LSB, Y15 is MSB.
$\overline{FULL}$	O	Indicates that 33 items are on the stack.
$\overline{PL}$	O	Can select #1 source (usually Pipeline Register) as direct input source.
$\overline{MAP}$	O	Can select #2 source (usually Mapping PROM or PLA) as direct input source.
$\overline{VECT}$	O	Can select #3 source (for example, Interrupt Starting Address) as direct input source.

2551 tbl 01

PRODUCT DESCRIPTION

The IDT49C410s are high-performance CMOS microprogram sequencers that are intended for use in very high-speed microprogrammable microprocessor applications. The sequencers allow for direct control of up to 64K words of microprogram.

The heart of the microprogram sequencers is a 4-input multiplexer that is used to select one of four address sources to select the next microprogram address. These address sources include the register/counter, the direct input, the microprogram counter or the stack as the source for the address of the next microinstruction.

The register/counter consists of sixteen D-type flip-flops which can contain either an address or a count. These edge-triggered flip-flops are under the control of a common clock enable, as well as the four microinstruction control inputs. When the load control ($\overline{RDL}$) is LOW, the data at the D inputs is loaded into this register on the LOW-to-HIGH transition of the clock. The output of the register/counter is available at the multiplexer as a possible next address source for the microcode. Also, the terminal count output associated with the register/counter is available at the internal instruction PLA to be used as condition code input for some of the microinstructions. The IDT49C410s contain a microprogram counter that usually contains the address of the next microinstruction compared to that currently being executed. The microprogram counter actually consists of a 16-bit incrementer followed by a 16-bit register. The microprogram counter will increment the address coming out of the sequencer going to the microprogram memory if the carry-in input to this counter is HIGH; otherwise, this address will be loaded into the microprogram counter. Normally, this carry-in input is set to the logic HIGH state so that the incrementer will be active. Should the carry-in input be set LOW, the same address is loaded into the microprogram counter. This is a technique that can be used to allow execution of the same microinstruction several times.

There are sixteen D-inputs on the IDT49C410s that go directly to the address multiplexer. These inputs are used to provide a branch address that can come directly from the microcode or some other external source. The fourth input available to the multiplexer for next address control is the 33-deep, 16-bit wide LIFO stack. The LIFO stack provides return address linkage for subroutines and loops. The IDT49C410s contain a built-in stack pointer that always points to the last stack location written. This allows for stack reference operations, usually called loops, to be performed without popping the stack.

The stack pointer internal to the IDT49C410s is actually an up/down counter. During the execution of microinstructions one, four and five, the PUSH operation may occur depending on the state of the condition code input. This causes the stack pointer to be incremented by one and the stack to be written with the required return linkage (the value contained in the microprogram counter). On the microprogram cycle following the PUSH, this new return linkage data that was in the microprogram counter is now at the new location pointed to by the stack pointer. Thus, any time the multiplexer looks at the stack, it will see this data on the top of the stack.

During five different microinstructions, a pop operation associated with the stack may occur. If the pop occurs, the stack pointer is decremented at the next LOW-to-HIGH transition of the clock. A pop decrements the stack pointer which is the equivalent of removing the old information from the top of the stack.

The IDT49C410s are designed so that the stack pointer linkage allows any sequence of pushes, pops or stack references to be used. The depth of the stack can grow to a full 33 locations. After a depth of 33 is reached, the $\overline{FULL}$ output goes LOW. If further PUSHes are attempted when the stack is full, the stack information at the top of the stack will be destroyed but the stack pointer will not end around. It is necessary to initialize the stack pointer when power is first turned on. This is performed by executing a RESET instruction (Instruction 0). This sets the stack pointer to the stack empty position — the equivalent depth of zero. Similarly, a pop from an empty stack may place unknown data on the Y outputs, but the stack pointer is designed not to end around. Thus, the stack pointer will remain at the 0 or stack empty location if a pop is executed while the stack is already empty.

The IDT49C410's internal 16-bit register/counter is used during microinstructions eight, nine and fifteen. During these instructions, the 16-bit counter acts as a down counter and the terminal count (count = 0) is used by the internal instruction PLA as an input to control the microinstruction branch test capability. The design of the internal counter is such that, if it is preloaded with a number N and then this counter is used in a microprogram loop, the actual sequence in the loop will be executed N + 1 times. Thus, it is possible to load the counter with a count of 0 and this will result in the microcode being executed one time. The 3-way branch microinstruction, instruction 15, uses both the loop counter and the external condition code input to control the final source address from the Y outputs of the microprogram sequencer. This 3-way branch may result in the next address coming from the D inputs, the stack or the microprogram counter.

The IDT49C410s provide a 16-bit address at the Y outputs that are under control of the $\overline{OE}$ input. Thus, the outputs can be put in the three-state mode, allowing the writable control store to be loaded or certain types of external diagnostics to be executed.

In summary, the IDT49C410s are the most powerful microprogram sequencers currently available. They provide the deepest stack, the highest performance and lowest power dissipation for today's microprogrammed machine design.

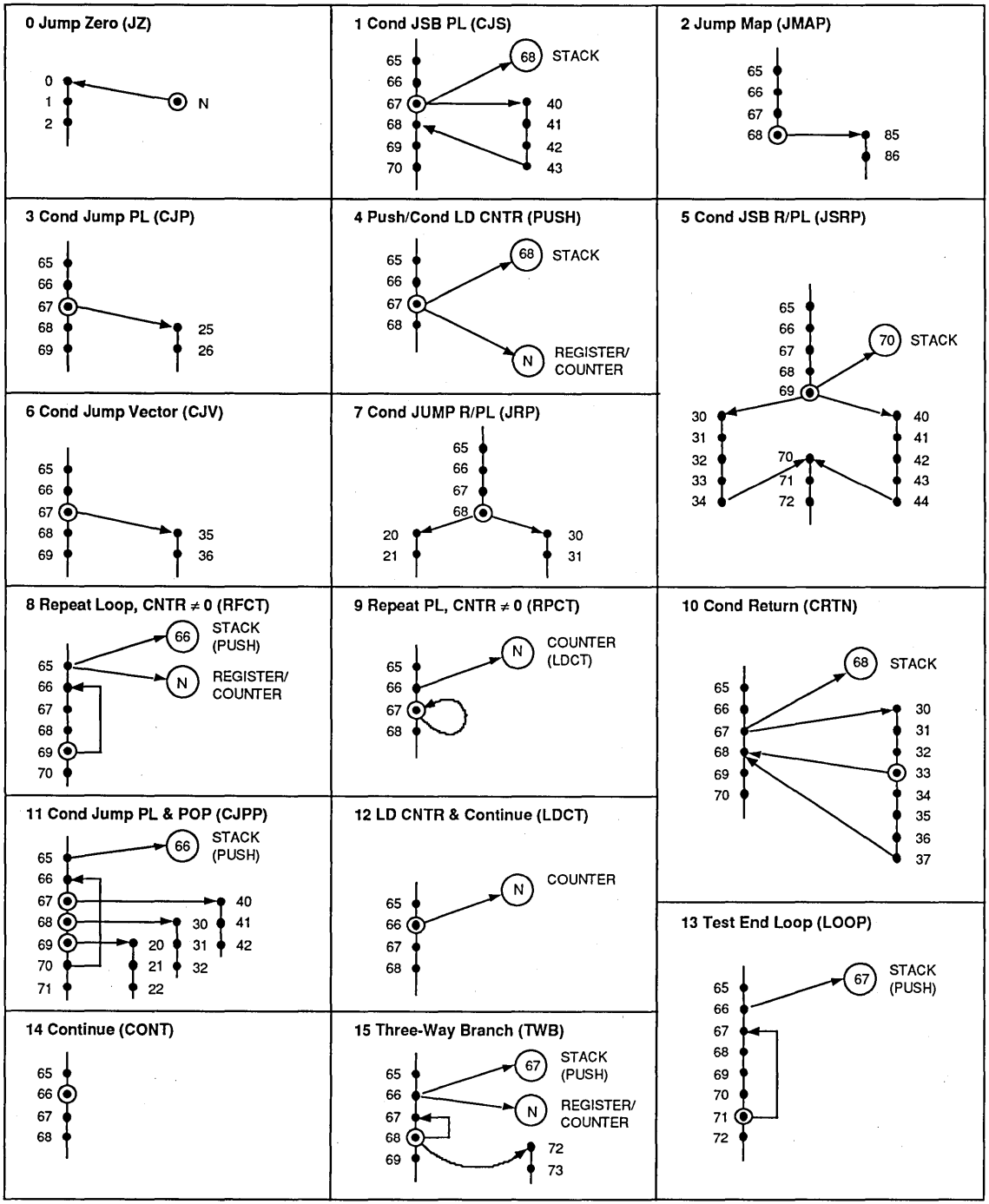


Figure 1. IDT49C410 Flow Diagrams

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IDT49C410 OPERATION

The IDT49C410s are CMOS pin-compatible implementations of the Am2910 and 2910A microprogram sequencers. The IDT49C410 sequencers are functionally identical except that they are 16 bits wide and provide a 33-deep stack to give the microprogrammer more capability in terms of microprogram subroutines and microprogram loops. The definition of each microprogram instruction is shown in the table of instructions. This table shows the results of each instruction in terms of controlling the multiplexer, which determines the Y outputs, and in controlling the signals that can be used to enable various branch address sources ($\overline{PL}$, $\overline{MAP}$, $\overline{VECT}$). The operation of the register/counter and the 33-deep stack after the next LOW-to-HIGH transition of the clock are also shown. The internal multiplexer is used to select which of the internal sources is used to drive the Y outputs. The actual value loaded into the microprogram counter is either identical to the Y output or the Y output value is incremented by 1 and placed in the microprogram counter. This function is under the control of the carry inputs. For each of the microinstruction inputs, only one of the three outputs ($\overline{PL}$, $\overline{MAP}$ or $\overline{VECT}$) will be LOW. Note that this function is not determined by any of the possible condition code inputs. These outputs can be used to control the three-state selection of one of the sources for the microprogram branches.

Two inputs, $\overline{CC}$ and $\overline{CCEN}$, can be used to control the conditional instructions. These are fully defined in the table of instructions. The $\overline{RLD}$ input can be used to load the internal register/counter at any time. When this input is LOW, the data at the D inputs will be loaded into this register/counter on the LOW-to-HIGH transition of the clock. Thus, the $\overline{RLD}$ input overrides the internal hold or decrement operations specified by the various microinstructions. The $\overline{OE}$ input is normally LOW and is used as the three-state enable for the Y outputs. The internal stack in the IDT49C410s is a last-in/first-out memory that is 16-bits in width and 33 words deep. It has a stack pointer that addresses the stack and always points to the value currently on the top of the stack. When instruction 0 (RESET) is executed, the stack pointer is initialized to the top of the stack which is, by definition, the stack empty condition. Thus, the contents of the top of the stack are undefined until the forced PUSH occurs. A pop performed while the stack is empty will not change the stack pointer in any way; however, it will result in unknown data at the Y outputs.

By definition, the stack is full any time 33 more PUSHes than pops have occurred since the stack was last empty. When this happens, the $\overline{FULL}$ Flag will go LOW. This signal first goes LOW on the microcycle after the 33 pushes occur. When this signal is LOW, no additional pushes should be attempted or the information on the top of the stack will be lost.

THE IDT49C410 INSTRUCTION SET

This data sheet contains a block diagram of the IDT49C410 microprogram sequencers. As can be seen, the devices are controlled by a 4-bit microinstruction word (I_3 - I_0). Normally, this word is supplied from one 4-bit field of the microinstruction word associated with the entire state machine system. These four bits provide for the selection of one of the sixteen powerful instructions associated with selecting the address of the next microinstruction. Unused Y outputs can be left open; however, the corresponding most significant D inputs should be tied to ground for smaller microwords. This is necessary to make sure the internal operation of the counter is proper should less than 64K of microcode be implemented. As shown in the block diagram, the internal instruction PLA uses the four instruction inputs as well as the $\overline{CC}$, $\overline{CCEN}$ and the internal counter = 0 line for controlling the sequencer. This internal instruction PLA provides all of the necessary internal control signals to control each particular part of the microprogram sequencer. The next address at the Y outputs of the IDT49C410s can be from one of four sources. These include the internal microprogram counter, the last-in/first-out stack, the register/counter and the direct inputs.

The following paragraphs will describe each instruction associated with the IDT49C410s. As a part of the discussion, an example of each instruction is shown in Figure 1. The purpose of the examples is to show microprogram flow. Thus, in each example the microinstruction currently being executed has a circle around it. That is, this microinstruction is assumed to be the contents of the pipeline register at the output of the microprogram memory. In these drawings, each of the dots refers to the time that the contents of the microprogram memory word would be in the pipeline register and is currently being executed.

INSTRUCTION 0 – JUMP 0 (JZ)

This Conditional Jump is used at power-up time or at any restart sequence when the need is to reset the stack pointer and jump to the very first address in microprogram memory. The Jump 0 instruction does not change the contents of the register/counter.

INSTRUCTION 1 – CONDITIONAL JUMP TO SUBROUTINE (CJS)

The Conditional Jump to Subroutine instruction is the one used to call microprogram subroutines. The subroutine address will be contained in the pipeline register and presented at the D inputs. If the condition code test is passed, a branch is taken to the subroutine. Referring to the flow diagram for the IDT49C410s shown in Figure 1, we see that the content of the microprogram counter is 68. This value is pushed onto the stack and the top of stack pointer is incremented. If the test is failed, this Conditional Jump to Subroutine instruction behaves as a simple continue. That is, the content of microinstruction address 68 is executed next.

INSTRUCTION 2 – JUMP MAP (JMAP)

This sequencer instruction can be used to start different microprogram routines based on the machine instruction opcode. This is typically accomplished by using a mapping PROM as an input to the D inputs on the microprogram sequencer. The JMAP instruction branches to the address appearing on the D inputs. In the flow diagram shown in Figure 1, we see that the branch actually will be the contents of microinstruction 85 and this instruction will be executed next.

IDT49C410 INSTRUCTION OPERATIONAL SUMMARY

$I_3 - I_0$	Mnemonic	CC	Counter Test	Stack	Address Source	Register Counter	Enable Select
0	JZ	X	X	CLEAR	0	NC	$\overline{PL}$
1	CJS	PASS FAIL	X X	PUSH NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
2	JMAP	X	X	NC	D	NC	$\overline{MAP}$
3	CJP	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
4	PUSH	PASS FAIL	X X	PUSH PUSH	PC PC	LOAD NC	$\overline{PL}$ $\overline{PL}$
5	JSRP	PASS FAIL	X X	PUSH PUSH	D R	NC NC	$\overline{PL}$ $\overline{PL}$
6	CJV	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{VECT}$ $\overline{VECT}$
7	JRP	PASS FAIL	X X	NC NC	D R	NC NC	$\overline{PL}$ $\overline{PL}$
8	RFCT	X X	= 0 NOT = 0	POP NC	PC STACK	NC DEC	$\overline{PL}$ $\overline{PL}$
9	RPCT	X X	= 0 NOT = 0	NC NC	PC D	NC DEC	$\overline{PL}$ $\overline{PL}$
10	CRTN	PASS FAIL	X X	POP NC	STACK PC	NC NC	$\overline{PL}$ $\overline{PL}$
11	CJPP	PASS FAIL	X X	POP NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
12	LDCT	X	X	NC	PC	LOAD	$\overline{PL}$
13	LOOP	PASS FAIL	X X	POP NC	PC STACK	NC NC	$\overline{PL}$ $\overline{PL}$
14	CONT	X	X	NC	PC	NC	$\overline{PL}$
15	TWB	PASS PASS FAIL FAIL	= 0 NOT = 0 = 0 NOT = 0	POP POP POP NC	PC PC D STACK	NC DEC NC DEC	$\overline{PL}$ $\overline{PL}$ $\overline{PL}$ $\overline{PL}$

NC = No Charge; DEC = Decrement

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INSTRUCTION 3 – CONDITIONAL JUMP PIPELINE (CJP)

The simplest branching control available in the IDT49C410 microprogram sequencers is that of conditional jump to address. In this instruction, the jump address is usually contained in the microinstruction pipeline register and presented to the D inputs. If the test is passed, the jump is taken while, if the test fails, this instruction executes as a simple continue. In the example shown in the flow diagram of Figure 1, we see that if the test is passed, the next microinstruction to be executed is the content of address 25. If the test is failed, the microcode simply continues to the contents of the next instruction.

INSTRUCTION 4 – PUSH/CONDITIONAL LOAD COUNTER (PUSH)

With this instruction, the counter can be conditionally loaded during the same instruction that pushes the current value of the microprogram counter on to the stack. Under any condition independent of the conditional testing, the microprogram counter is pushed on to the stack. If the conditional test is passed, the counter will be loaded with the value on the D inputs to the sequencer. If the test fails, the contents of the counter will not change. The PUSH/Conditional Load Counter instruction is used in conjunction with the loop instruction (Instruction 13), the repeat file based on the counter instruction (Instruction 9) or the 3-way branch instruction (Instruction 15).

INSTRUCTION 5 – CONDITIONAL JUMP TO SUBROUTINE R/PL (JSRP)

Subroutines may be called by a Conditional Jump Subroutine from the internal register or from the external pipeline register. In this instruction the contents of the microprogram counter are pushed on the stack and the branch address for the subroutine call will be taken from either the internal register/counter or the external pipeline register presented to the D inputs. If the conditional test is passed, the subroutine address will be taken from the pipeline register. If the conditional test fails, the branch address is taken from the internal register/counter. An example of this is shown in the flow diagram of Figure 1.

INSTRUCTION 6 – CONDITIONAL JUMP VECTOR (CJV)

The Conditional Jump Vector instruction is similar to the Jump Map instruction in that it allows a branch operation to a microinstruction as defined from some external source,

except that it is conditional. The Jump Map instruction is unconditional. If the conditional test is passed, the branch is taken to the new address on the D inputs. If the conditional test is failed, no branch is taken but rather the microcode simply continues to the next sequential microinstruction. When this instruction is executed, the $\overline{VECT}$ output is LOW unconditionally. Thus, an external 12-bit field can be enabled on to the D inputs of the microprogram sequencer.

INSTRUCTION 7 –
CONDITIONAL JUMP R/PL (JRP)

The Conditional Jump register/counter or external pipeline register always causes a branch in microcode. This jump will be to one of two different locations in the microcode address space. If the test is passed, the jump will be to the address presented on the D inputs to the microprogram sequencer. If the conditional test fails, the branch will be to the address contained in the internal register/counter.

INSTRUCTION 8 –
REPEAT LOOP COUNTER NOT EQUAL TO 0 (RFCT)

This instruction utilizes the loop counter and the stack to implement microprogrammed loops. The start address for the loop would be initialized by using the PUSH/Conditional Load Counter instruction. Then, when the repeat loop instruction is executed, if the counter is not equal to 0, the next microword address will be taken from the stack. This will cause a loop to be executed as shown in the Figure 1 flow diagram. Each time the microcode sequence goes around the loop, the counter is decremented. When the counter reaches 0, the stack will be popped and the microinstruction address will be taken from the microprogram counter. This instruction performs a timed wait or allows a single sequence to be executed the desired number of times. Remember, the actual number of loops performed is equal to the value in the counter plus 1.

INSTRUCTION 9 –
REPEAT PIPELINE, COUNTER NOT EQUAL TO 0 (RPCT)

This instruction is another technique for implementing a loop using the counter. Here, the branch address for the loop is contained in the pipeline register. This instruction does not use the stack in any way as a part of its implementation. As long as the counter is not equal to 0, the next microword address will be taken from the D inputs of the microprogram sequencer. When the counter reaches 0, the internal multiplexer will select the address source from the microprogram counter, thus causing the microcode to continue on and leave the loop.

INSTRUCTION 10 –
CONDITIONAL RETURN (CRTN)

The Conditional Return instruction is used for terminating subroutines. The fact that it is conditional allows the subroutine either to be ended or to continue. If the conditional test is passed, the address of the next microinstruction will be taken from the stack and it will be popped. If the conditional test fails, the next microinstruction address will come from the internal microprogram counter. This is depicted in the flow diagram of Figure 1. It is important to remember that every subroutine call must somewhere be followed by a return from subroutine call in order to have an equal number of pushes and pops on the stack.

INSTRUCTION 11 –
CONDITIONAL JUMP PIPELINE AND POP (CJPP)

The Conditional Jump Pipeline and Pop instruction is a technique for exiting a loop from within the middle of the loop. This is depicted fully in the flow diagram for the IDT49C410s, as shown in Figure 1. The conditional test input for this instruction results in a branch being taken if the test is passed. The address selected will be that on the D inputs to the microprogram sequencer and, since the loop is being terminated, the stack will popped. Should the test be failed on the conditional test inputs, the microprogram will simply continue to the next address as taken from the microprogram counter. The stack will not be affected if the conditional test input is failed.

INSTRUCTION 12 –
LOAD COUNTER AND CONTINUE (LDCT)

The Load Counter and Continue instruction is used to place a value on the D inputs in the register/counter and continue to the next microinstruction.

INSTRUCTION 13 –
TEST END OF LOOP (LOOP)

The Test End of Loop instruction is used as a last instruction in a loop associated with the stack. During this instruction, if the conditional test input is failed, the loop branch address will be that on the stack. Since we may go around the loop a number of times, the stack is not popped. If the conditional test input is passed, then the loop is terminated and the stack is popped. Notice that the loop instruction requires a PUSH to be performed at the instruction immediately prior to the loop return address. This is necessary so as to have the correct address on the stack before the loop operation. It is for this reason that the stack pointer always points to the last thing written on the stack.

INSTRUCTION 14 –
CONTINUE (CONT)

The Continue instruction is a simple instruction whereby the address for the microinstruction is taken from the microprogram counter. This instruction simply causes sequential program flow to the next microinstruction in microcode memory.

INSTRUCTION 15 –
THREE WAY BRANCH (TWB)

The Three Way Branch instruction is used for looping while waiting for a conditional event to come true. If the event does not come true after some number of microinstructions, a branch is taken to another microprogram sequence. This is depicted in Figure 1 showing the IDT49C410 flow diagrams and is also described in full detail in the IDT49C410's instruction operational summary. Operation of the instruction is such that any time the external conditional test input is passed, the next microinstruction will be that associated with the program counter and the loop will be left. The stack is also popped. Thus, the external test input overrides the other possibilities. Should the external test input not be true, the rest of the operation is controlled by the internal counter. If the counter

is not equal to 0, the loop is taken by selecting the address on the top of the stack as the address out of the Y outputs of the IDT49C410. In addition, the counter is decremented. Should the external conditional test input be failed and the counter also have counted to 0, this instruction "times out". The result is that the stack is popped and a branch is taken to the address presented to the D inputs of the IDT49C410 microprogram sequencer. This address is usually provided by the external pipeline register.

CONDITIONAL TEST

Throughout this discussion we have talked about microcode passing the conditional test. There are actually two inputs associated with the conditional test input. These include the $\overline{CCEN}$ and the $\overline{CC}$ inputs. The $\overline{CCEN}$ input is a condition code enable. Whenever the $\overline{CCEN}$ input is HIGH, the $\overline{CC}$ input is ignored and the device operates as though the $\overline{CC}$ input were true (LOW). Thus, a fail of the external test condition can be defined as $\overline{CCEN}$ equals LOW and $\overline{CC}$ equals HIGH. A pass condition is defined as a $\overline{CCEN}$ equal to HIGH or a $\overline{CC}$ equal to LOW. It is important to recognize the full function of the condition code enable and the condition code inputs in order to understand when the test is passed or failed.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE: 2551 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2551 tbl 04

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%; Military: T_A = – 55°C to + 125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions [1]		Min.	Typ. [2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level [4]		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level [4]		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	– 0.1	– 5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{HC}	–	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12 mA MIL	2.4	4.3	–	
			I_{OH} = –15 mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA	–	GND	V_{LC}	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 mA MIL	–	0.3	0.5	
			I_{OL} = 24 mA COM'L	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	– 0.1	– 10	µA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V [3]		– 30	–	–	mA

NOTES:
1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels should only be static tested in a noise-free environment.

2551 tbl 05

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DC ELECTRICAL CHARACTERISTICS (Cont'd.)

Commercial: T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%; Military: T_A = – 55°C to + 125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions [1]		Min.	Typ. [2]	Max.	Unit
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = H		–	35	50	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = L		–	35	50	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High) [5]	V_{CC} = Max., V_{IH} = 3.4V, f_{CP} = 0		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL COM'L	– –	1.0 1.0	3.0 1.5	mA/ MHz
I_{CC}	Total Power Supply Current [6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50 % Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	MIL COM'L	– –	45 45	80 65	mA
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50 % Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL COM'L	– –	50 50	90 75	

NOTES: 2551 tbl 06

5. I_{CCQT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input frequency

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large Vcc current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

IDT49C410A
AC ELECTRICAL CHARACTERISTICS
I. SET-UP AND HOLD TIMES

Inputs	t (S)		t (H)		Unit
	Com'l.	Mil.	Com'l.	Mil.	
DI → R	6	7	0	0	ns
DI → PC	13	15	0	0	ns
I 0–3	23	25	0	0	ns
$\overline{CC}$	15	18	0	0	ns
$\overline{CCEN}$	15	18	0	0	ns
CI	6	7	0	0	ns
$\overline{RLD}$	11	12	0	0	ns

2551 tbl 07

II. COMBINATIONAL DELAYS

Inputs	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		Unit
	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
D0–11	12	15	–	–	–	–	ns
I 0–3	20	25	13	15	–	–	ns
$\overline{CC}$	16	20	–	–	–	–	ns
$\overline{CCEN}$	16	20	–	–	–	–	ns
CP	28	33	–	–	22	25	ns
$\overline{OE}$ (1)	10/10	13/13	–	–	–	–	ns

2551 tbl 08

NOTE:
1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF. Tested at C_L = 50pF, correlated to 5pF.

III. CLOCK REQUIREMENTS

	Com'l.	Mil.	Unit
Minimum Clock LOW Time	18	20	ns
Minimum Clock HIGH Time	17	20	ns
Minimum Clock Period	35	40	ns

2551 tbl 09

IDT49C410
AC ELECTRICAL CHARACTERISTICS
I. SET-UP AND HOLD TIMES

Inputs	t (S)		t (H)		Unit
	Com'l.	Mil.	Com'l.	Mil.	
DI → R	16	16	0	0	ns
DI → PC	30	30	0	0	ns
I 0–3	35	38	0	0	ns
$\overline{CC}$	24	35	0	0	ns
$\overline{CCEN}$	24	35	0	0	ns
CI	18	18	0	0	ns
$\overline{RLD}$	19	20	0	0	ns

2551 tbl 10

II. COMBINATIONAL DELAYS

Inputs	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		Unit
	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
D0–11	20	25	–	–	–	–	ns
I 0–3	35	40	30	35	–	–	ns
$\overline{CC}$	30	36	–	–	–	–	ns
$\overline{CCEN}$	30	36	–	–	–	–	ns
CP	40	46	–	–	31	35	ns
$\overline{OE}$ (1)	25/27	25/30	–	–	–	–	ns

2551 tbl 11

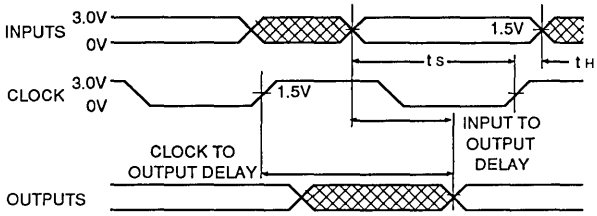
NOTE:
1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF. Tested at C_L = 50pF, correlated to 5pF.

III. CLOCK REQUIREMENTS

	Com'l.	Mil.	Unit
Minimum Clock LOW Time	20	25	ns
Minimum Clock HIGH Time	20	25	ns
Minimum Clock Period	50	51	ns

2551 tbl 12

SWITCHING WAVEFORMS



2551 drw 06

IDT49C410 INPUT/OUTPUT INTERFACE CIRCUITRY

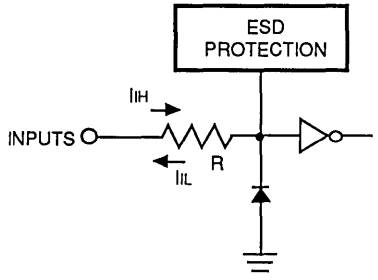


Figure 2. Input Structure

2551 drw 07

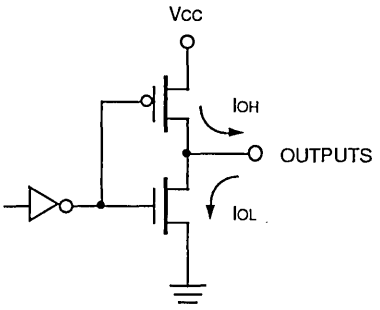
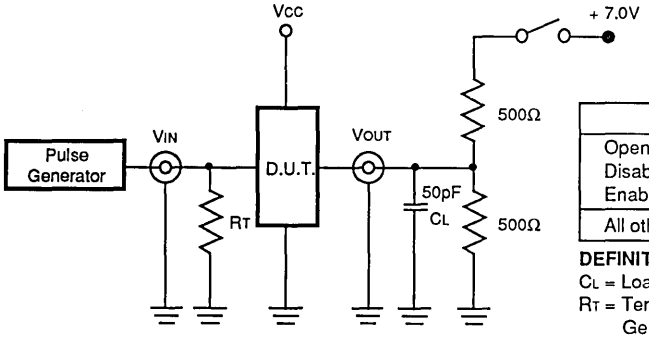


Figure 3. Output Structure

2551 drw 08

TEST LOAD CIRCUIT



Test	Switch
Open Drain Disable Output from Low Enable Output to Low	Closed
All other Outputs	Open

2551 tbl 13

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 4. Switching Test Circuits

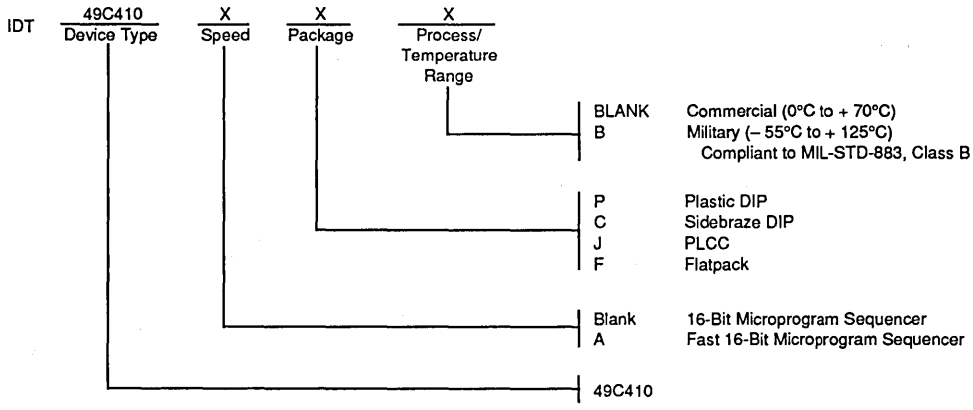
2551 drw 09

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 3

2551 tbl 14

ORDERING INFORMATION



2551 drw 10

5

Integrated Device Technology, Inc.

16 x 16 PARALLEL CMOS MULTIPLIER-ACCUMULATOR

IDT7210L

FEATURES:

- 16 x 16 parallel multiplier-accumulator with selectable accumulation and subtraction
- High-speed: 25ns multiply-accumulate time
- IDT7210 features selectable accumulation, subtraction, rounding and preloading with 25-bit result
- IDT7210 is pin and functionally compatible with the TRW TDC1010J
- Performs subtraction and double precision addition and multiplication
- Produced using advanced CEMOS™ high-performance technology
- TTL-compatible
- Available in plastic and topbraze DIP, PLCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88733 is listed on this function

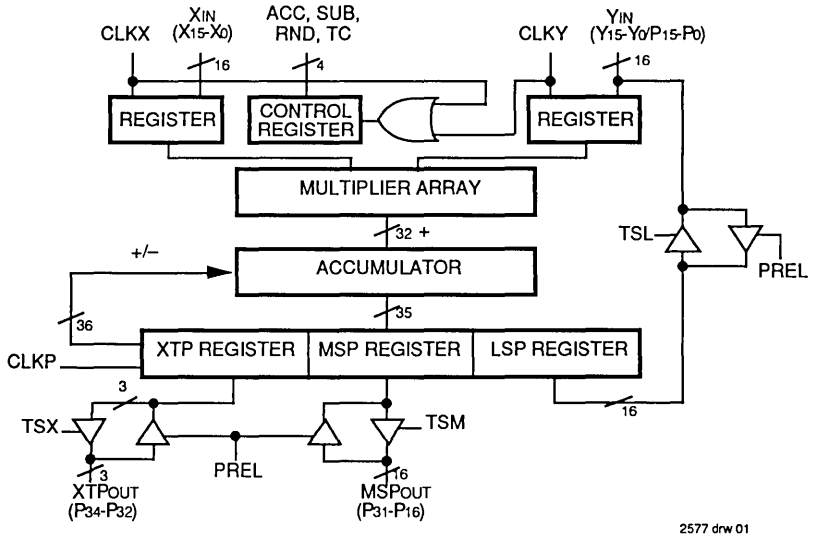
DESCRIPTION:

The IDT7210 is a high-speed, low-power 16 x 16-bit parallel multiplier-accumulator that is ideally suited for real-time digital signal processing applications. Fabricated using CEMOS silicon gate technology, this device offers a very low-power alternative to existing bipolar and NMOS counterparts, with only 1/7 to 1/10 the power dissipation and exceptional speed (25ns maximum) performance.

A pin and functional replacement for TRW's TDC1010J the IDT7210 operates from a single 5 volt supply and is compatible with standard TTL logic levels. The architecture of the IDT7210 is fairly straightforward, featuring individual input and output registers with clocked D-type flip-flop, a preload capability which enables input data to be preloaded into the output registers, individual three-state output ports for the Extended Product (XTP) and Most Significant Product (MSP) and a Least Significant Product output (LSP) which is multiplexed with the Y input.

The X_{IN} and Y_{IN} data input registers may be specified through the use of the Two's Complement input (TC) as either a two's complement or an unsigned magnitude, yielding a full-precision 32-bit result that may be accumulated to a full 35-bit result. The three output registers – Extended Product (XTP), Most Most Significant Product (MSP) and Least Significant Product (LSP) – are controlled by the respective TSX, TSM and TSL input lines. The LSP output can be routed through Y_{IN} ports.

FUNCTIONAL BLOCK DIAGRAM



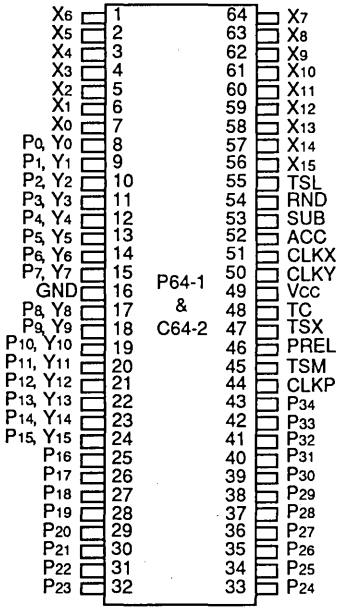
IDT7210

CEMOS is a trademark of Integrated Device Technology, Inc.

DESCRIPTION (Continued)

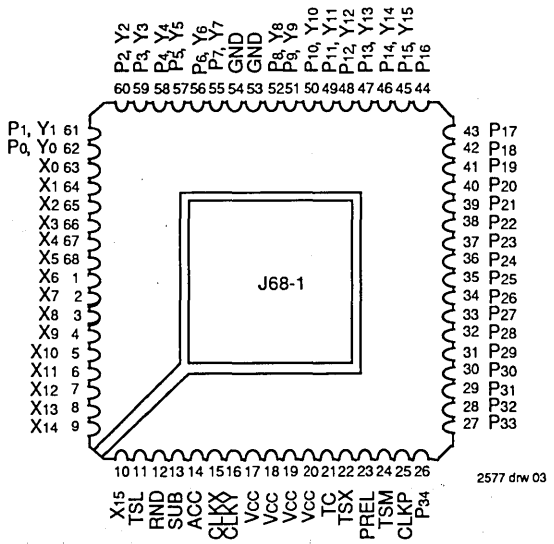
The Accumulate input (ACC) enables the device to perform either a multiply or a multiply-accumulate function. In the multiply-accumulate mode, output data can be added to or subtracted from subsequent results. When the Subtraction (SUB) input is active simultaneously with an active ACC, a subtraction can be performed. The double precision accumulated result is rounded down to either a single precision or single precision plus 3-bit extended result. In the multiply mode, the Extended Product output (XTP) is sign extended in the two's complement mode or set to zero in the unsigned mode. The Round (RND) control rounds up the Most Significant Product (MSP) and the 3-bit Extended Product (XTP) outputs. When Preload input (PREL) is active, all the output buffers are forced into a high-impedance state (see Preload truth table) and external data can be loaded into the output register by using the TSX, TSL and TSM signals as input controls.

PIN CONFIGURATIONS



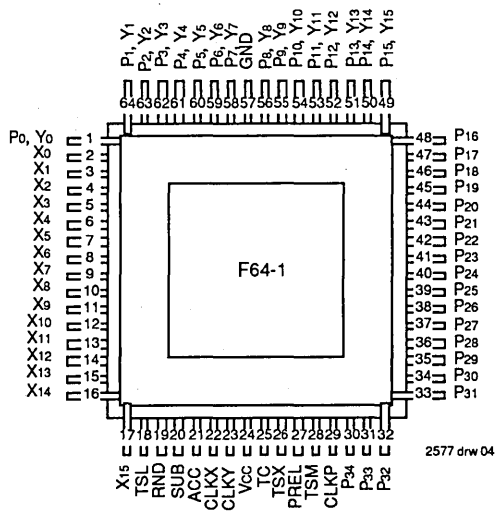
DIP
TOP VIEW

2577 drw 02



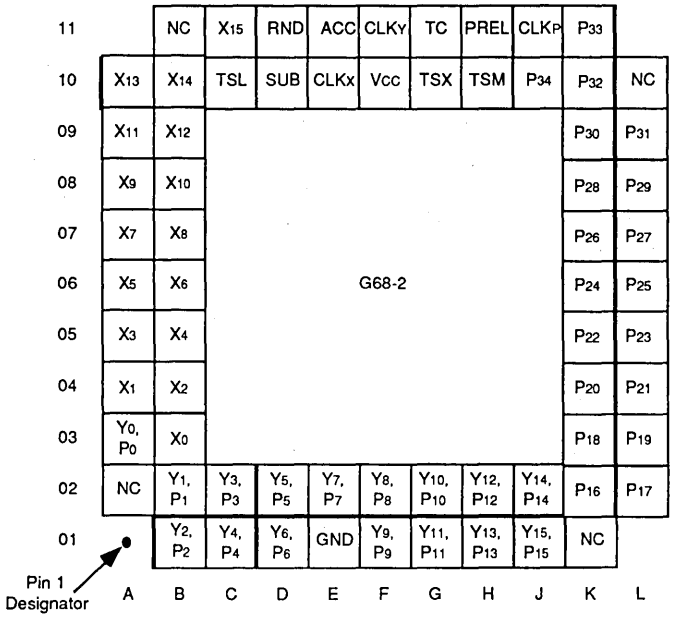
2577 drw 03

PLCC
TOP VIEW



2577 drw 04

FLATPACK
TOP VIEW



PGA
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VCC	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
VTERM	Terminal Voltage with Respect to GND	–0.5 to VCC +0.5V	–0.5 to VCC +0.5V	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2577 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	12	pF

NOTE: 2577 tbl 07

1. This parameter is measured at characterization and not 100%tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C TO +125°C)

Symbol	Parameter	Test Conditions	Commercial			Military			Unit
			Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.	
V_{IH}	Input High Voltage		2.0	—	—	2.0	—	—	V
V_{IL}	Input Low Voltage		—	—	0.8	—	—	0.8	V
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	10	—	—	10	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	—	45	90	—	45	110	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	50	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ –0.2V, $V_{IN} \leq$ 0.2V	—	4	10	—	4	12	mA
I_{CC}/f(2,3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10 MHz	—	—	6	—	—	8	mA/ MHz
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}(4)	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	—	0.4	—	—	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_O GND	-20	—	—	-20	—	—	mA

NOTES: 2577 tbl 03

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 90+ 6(f –10)mA, where f = operating frequency in MHz. For the military range, I_{CC} = 110 + 8(f –10). f = operating frequency in MHz, f = 1/t_{MA}.
3. For frequencies greater than 10MHz, guaranteed by design, not production tested.
4. I_{OL} = 8mA for t_{MA} = 20ns to 55ns.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0° to +70°C)

Symbol	Parameter	7210L25		7210L35		7210L45		7210L55		7210L65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MA}	Multiply-Accumulate Time	–	25	–	35	–	45	–	55	–	65	ns
t_D	Output Delay	–	20	–	25	–	25	–	30	–	35	ns
t_{ENA}	3-State Enable Time	–	20	–	25	–	25	–	30	–	30	ns
t_{DIS}	3-State Disable Time(1)	–	20	–	25	–	25	–	30	–	30	ns
t_S	Input Register Set-up Time	12	–	12	–	15	–	20	–	25	–	ns
t_H	Input Register Hold Time	3	–	3	–	3	–	3	–	3	–	ns
t_{PW}	Clock Pulse Width	10	–	10	–	15	–	20	–	25	–	ns

NOTES: 2577 tbl 04

1. Transition is measured ±500mV from steady state voltage.

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = –55° to +125°C)

Symbol	Parameter	7210L30		7210L40		7210L55		7210L65		7210L75		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MA}	Multiply-Accumulate Time	–	30	–	40	–	55	–	65	–	75	ns
t_D	Output Delay	–	20	–	25	–	30	–	35	–	35	ns
t_{ENA}	3-State Enable Time	–	20	–	25	–	30	–	30	–	35	ns
t_{DIS}	3-State Disable Time(1)	–	20	–	25	–	30	–	30	–	30	ns
t_S	Input Register Set-up Time	12	–	15	–	20	–	25	–	25	–	ns
t_H	Input Register Hold Time	3	–	3	–	3	–	3	–	3	–	ns
t_{PW}	Clock Pulse Width	10	–	15	–	20	–	25	–	25	–	ns

NOTES: 2577 tbl 05

1. Transition is measured ±500mV from steady state voltage.

SIGNAL DESCRIPTION

INPUTS

X_{IN} (X_{15} through X_0) — Multiplicand Data Inputs

Y_{IN} (Y_{15} through Y_0) — Multiplier Data Inputs.

INPUT CLOCKS

CLKX, CLKY — Input data is loaded on the rising edge of these clocks.

CONTROLS

ACC (Accumulate) — When ACC is high, the contents of the XTP, MSP and LSP registers are added to or subtracted from the multiplier output. When ACC is low, the device acts as a simple multiplier with no accumulation being performed and the next product generated will be stored directly into the output registers. The ACC signal is loaded on the rising edge of the CLKX or CLKY and must be valid for the duration of the data input.

SUB (Subtract) — When the ACC and SUB signals are both high, the contents of the output register are subtracted from the next product generated and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is high and SUB is low, an addition instead of a subtraction is performed. Like the ACC signal, the SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY and must be valid over the same period as the input data is valid. When the ACC is low, SUB acts as a "don't care" input.

TC (Two's Complement) — When the TC control is high, it makes both the X and Y input two's complement inputs. When the TC control is low, it makes both inputs, X and Y, unsigned magnitude inputs.

RND (Round)—A high level at this input adds a "1" to the most significant bit of the LSP to round up the XTP and MSP data. RND, like ACC and SUB, is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

PREL (Preload) — When the PREL input is high, the output is driven to a high impedance state. When the TSX, TSL and TSM inputs are also high, the contents of the output register can be preset to the preload data applied to the output pins at the rising edge of CLKP. The PREL, TSM, TSL and TSX inputs must be valid over the same period that the preload input is valid.

Y_{IN}/LSP Output — Shares functions between 16-bit data input (Y_{IN}) and the least significant product output (LSP).

TSX, TSL, TSM (Three-State Output Controls) — The XTP, MSP and LSP registers are controlled by direct non-registered control signals. These output drivers are at high impedance (disabled) when control signals TSX, TSM and TSL are high and are enabled when TSX, TSM and TSL are low.

OUTPUT CLOCK

CLKP — Output data is loaded into the output register on the rising edge of this clock.

OUTPUTS

XTP ($P_{34} - P_{32}$) — Extended Product Output (3-bits)

MSP ($P_{31} - P_{16}$) — Most Significant Product

LSP ($P_{15} - P_0$) — Least Significant Product shared with Y_{IN} input

NOTES ON TWO'S COMPLEMENT FORMATS

1. In two's complement notation, the location of the binary point that signifies the separation of the fractional and integer fields is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer field is provided to extend the utility of the accumulator. In the case of the output notation, the output binary point is located between the 2^0 and 2^{-1} bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number field can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.
2. When in the non-accumulating mode, the first four bits (P^{34} to P^{31}) will all indicate the sign of the product. Additionally, the P^{30} term will also indicate the sign with one exception, when multiplying -1×-1. With the additional bits that are available in this multiplier, the -1×-1 is a valid operation that yields a +1 product.
3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond that available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 35-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2577 tbl 06

PRELOAD TRUTH TABLE

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi Z
0	0	1	0	Q	Hi Z	Q
0	0	1	1	Q	Hi Z	Hi Z
0	1	0	0	Hi Z	Q	Q
0	1	0	1	Hi Z	Q	Hi Z
0	1	1	0	Hi Z	Hi Z	Q
0	1	1	1	Hi Z	Hi Z	Hi Z
1	0	0	0	Hi Z	Hi Z	Hi Z
1	0	0	1	Hi Z	Hi Z	PL
1	0	1	0	Hi Z	PL	Hi Z
1	0	1	1	Hi Z	PL	PL
1	1	0	0	PL	Hi Z	Hi Z
1	1	0	1	PL	Hi Z	PL
1	1	1	0	PL	PL	Hi Z
1	1	1	1	PL	PL	PL

NOTES: 2577 tbl 08

Hi Z = Output buffers at high impedance (output disabled)
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
PL = Output buffers at high impedance or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.

5

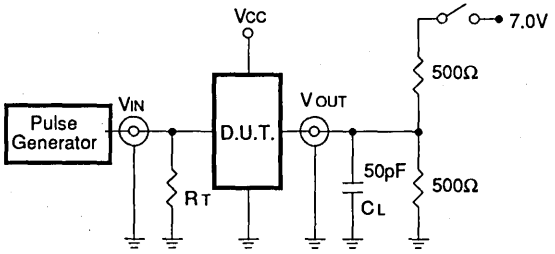


Figure 1. AC Test Load Circuit

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2577 tbl 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

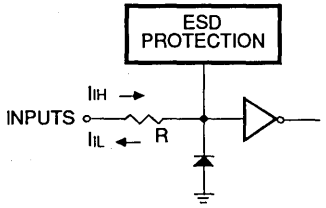


Figure 2. Input Interface Circuit

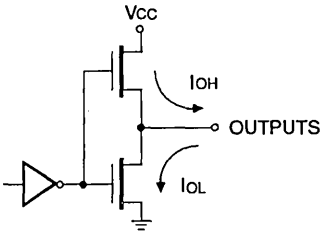


Figure 3. Output Interface Circuit

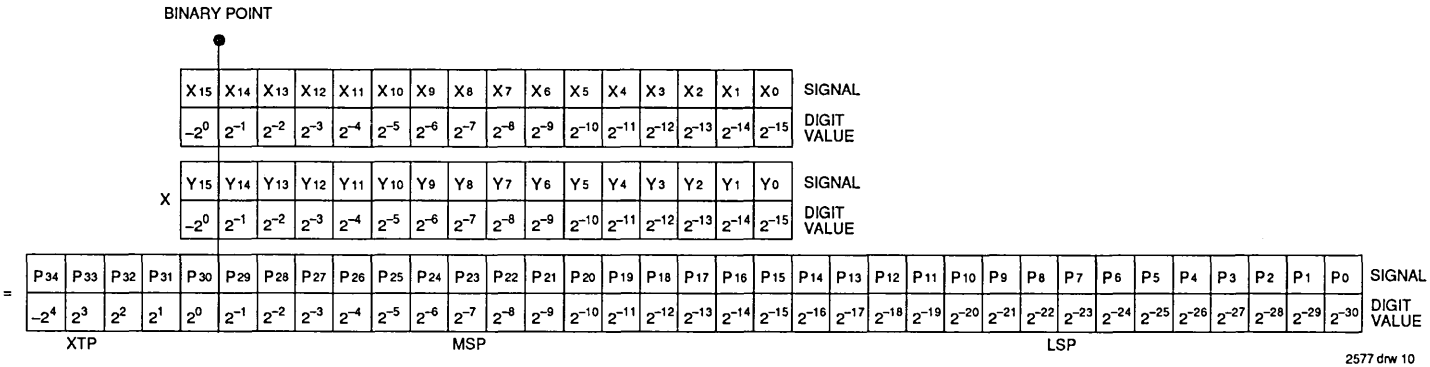


Figure 4. Franctional Two's Complement Notation.

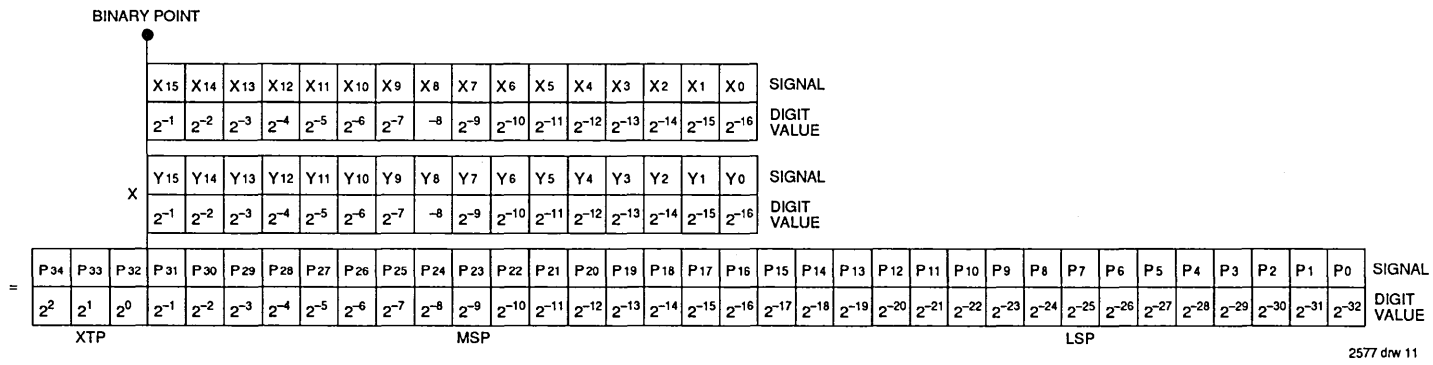


Figure 5. Fractional Unsigned Magnitude Notation

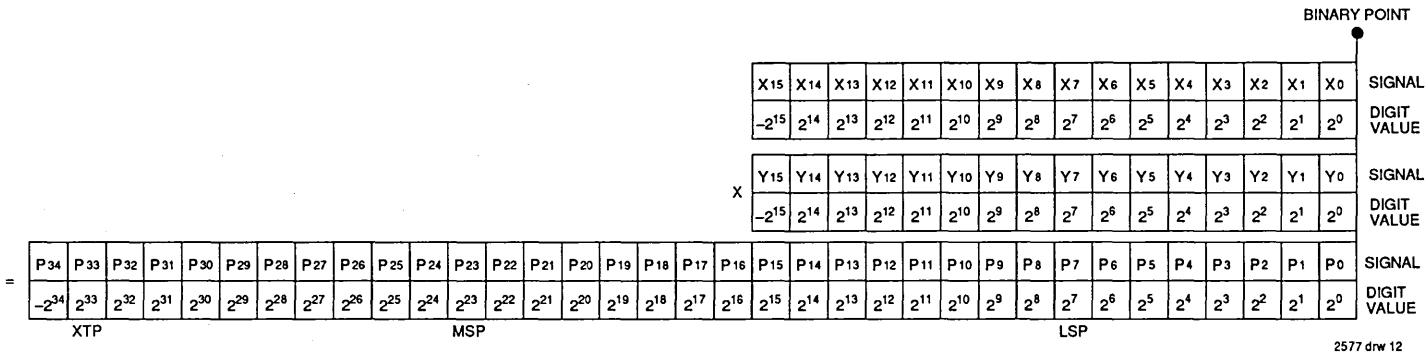


Figure 6. Integer Two's Complement Notation

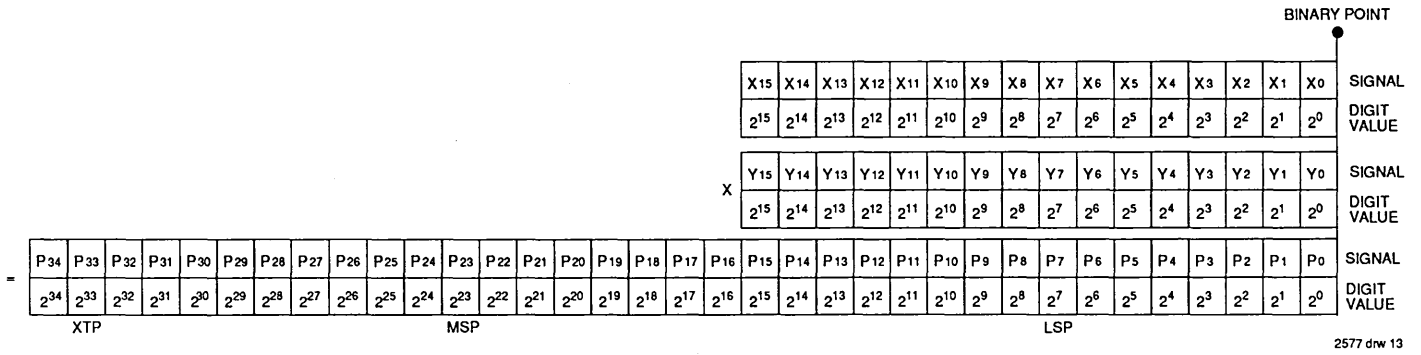
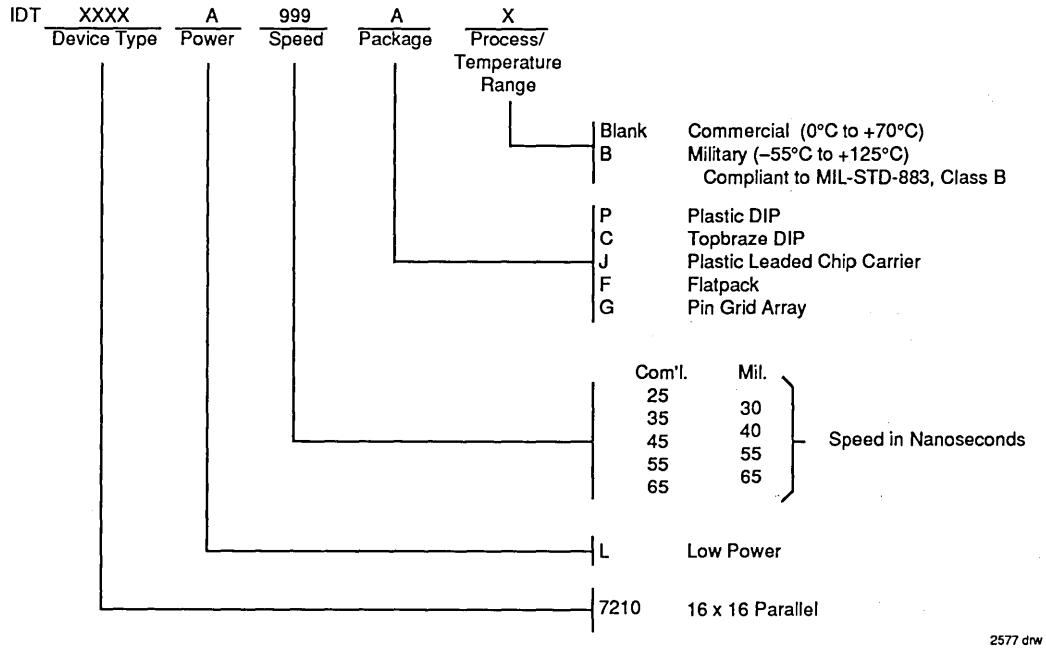


Figure 7. Integer Unsigned Magnitude Notation

ORDERING INFORMATION



5

Integrated Device Technology, Inc.

16 x 16 PARALLEL CMOS MULTIPLIERS

IDT7216L
IDT7217L

FEATURES:

- 16 x 16 parallel multiplier with double precision product
- 20ns clocked multiply time
- Low power consumption: 120mA
- Produced with advanced submicron CEMOS™ high performance technology
- IDT7216L is pin- and functionally-compatilble with TRW MPY016H/K and AMD Am29516
- IDT7217L requires only single clock with register enables making it pin- and functionally-compatible with AMD Am29517
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Input and output directly TTL-compatible
- Three-state output
- Available in plastic and Top Braze, DIP, PLCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing # 5962-86873 is listed on this function for IDT7216 and Standard Military Drawing #5962-87686 is listed for this function for IDT7217.

DESCRIPTION:

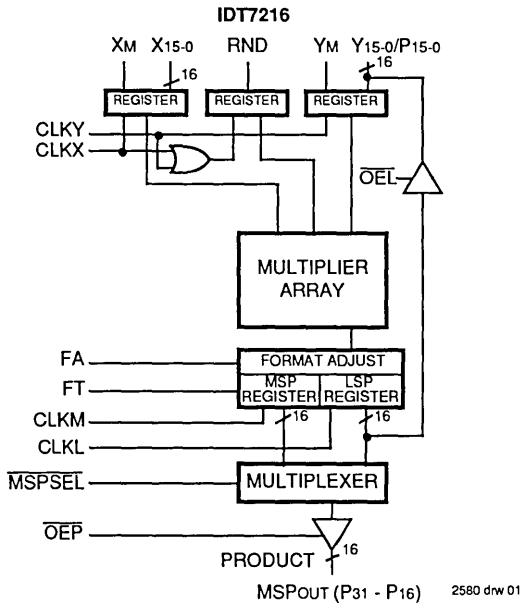
The IDT7216/IDT7217 are high-speed, low-power 16 x 16-bit multipliers ideal for fast, real time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, submicron CEMOS technology, has achieved speeds comparable to bipolar (20ns max.), at 1/10 the power consumption.

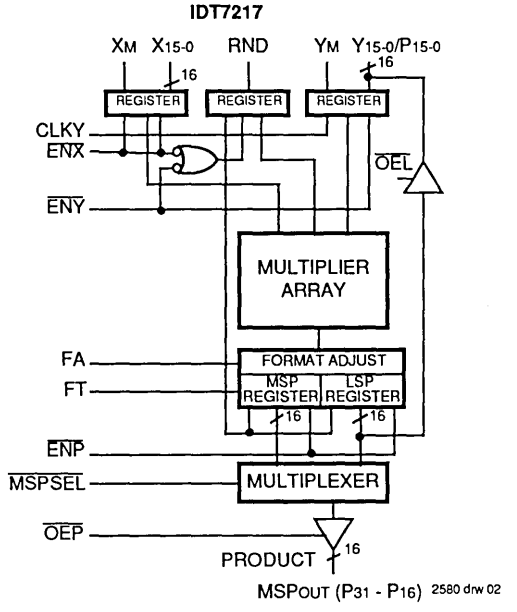
The IDT7216/IDT7217 are ideal for applications requiring high-speed multiplication such as fast Fourier transform analysis, digital filtering, graphic display systems, speed synthesis and recognition and in any system requirement where multiplication speeds of a mini/microcomputer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge-triggered D-type flip-flop. In the IDT7216, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7217 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

The IDT7216/IDT7217 offer additional flexibility with the FA control and $\overline{MSPSEL}$ functions. The FA control formats the output for two's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. The

FUNCTIONAL BLOCK DIAGRAMS





CEMOS is a trademark of Integrated Device Technology, Inc.

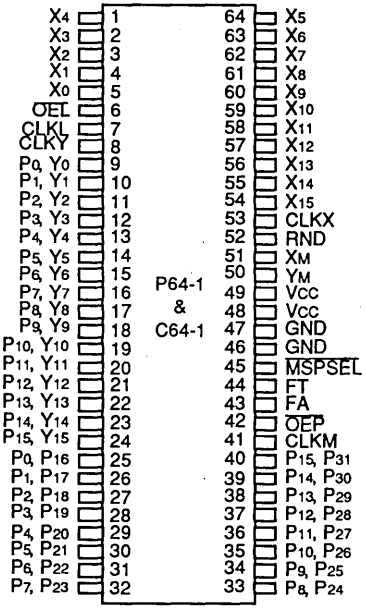
DESCRIPTION (Cont'd.)

$\overline{\text{MSPSEL}}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the TRW MPY016H.

The IDT7216/IDT7217 multipliers are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS

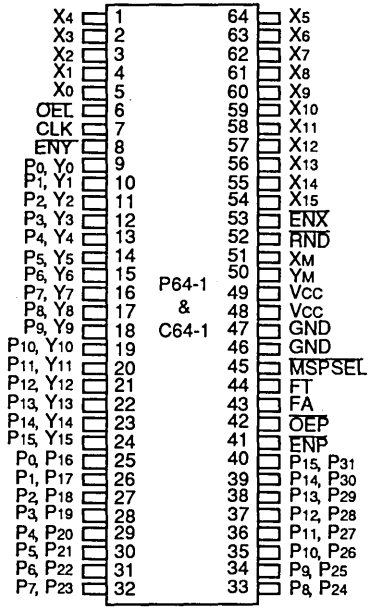
IDT7216



2580 drw 03

64-PIN DIP
TOP VIEW

IDT7217



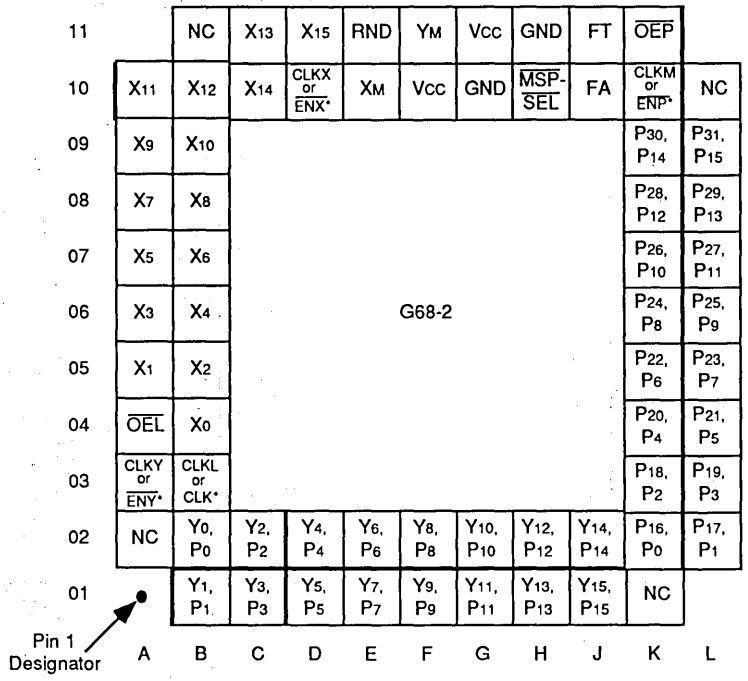
2580 drw 04

64-PIN DIP
TOP VIEW

5

PIN CONFIGURATIONS (Cont'd.)

IDT7216/IDT7217



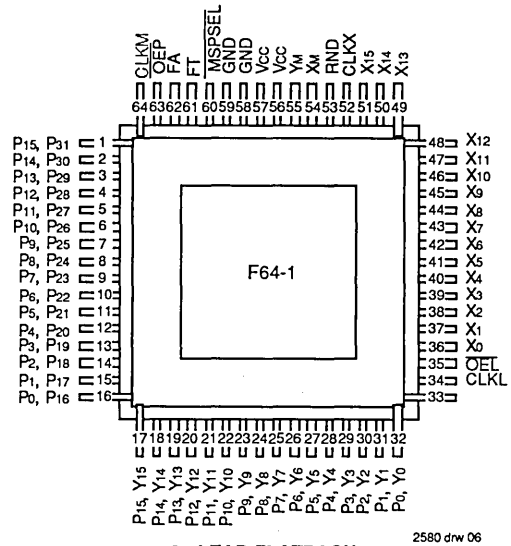
*Pin designation for IDT7217

2580 drw 05

PGA
TOP VIEW

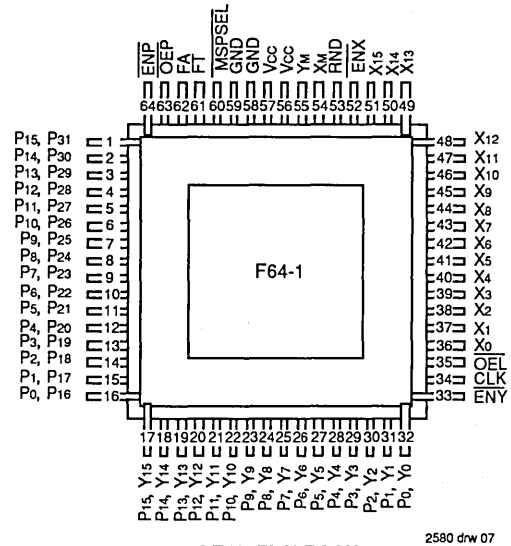
PIN CONFIGURATIONS (Cont'd.)

IDT7216



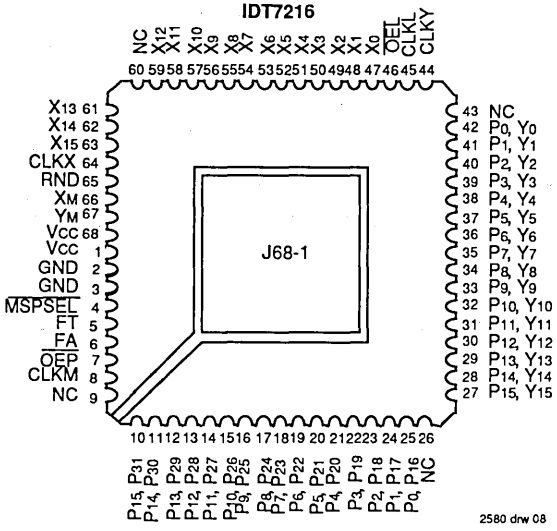
64-LEAD FLATPACK
TOP VIEW

IDT7217



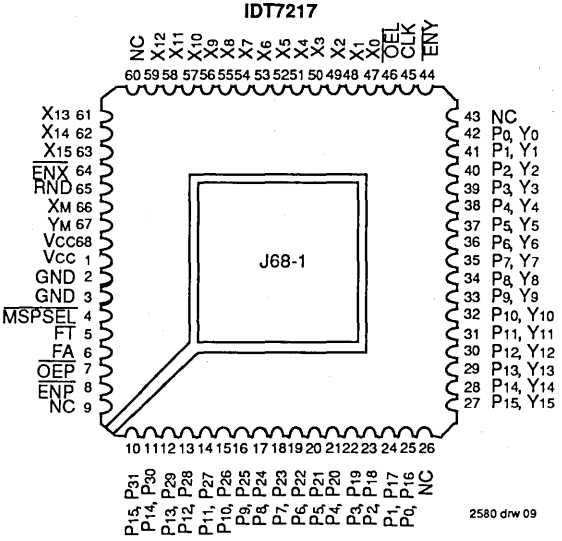
64-LEAD FLATPACK
TOP VIEW

IDT7216



PLCC
TOP VIEW

IDT7217



PLCC
TOP VIEW

5

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	V_{CC} + .05	V_{CC} + .05	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2580 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2580 tbl 04

1. This parameter is measured at characterization and not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter(1)	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage/7216	—	—	0.8	V
V_{IL}	Input Low Voltage/7217	—	—	0.4	V

2580 tbl 02

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C) for Commercial clocked multiply times of 20, 25, 35, 45, 55, 65ns or Military, 25, 30, 40, 55, 65, 75ns

			Commercial			Military			
Symbol	Parameter	Test Conditions(1)	Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.	Unit
V_{IH}	Input High Voltage		2.0	—	—	2.0	—	—	V
V_{IL}	Input Loow Voltage		—	—	0.8	—	—	0.8	V
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	10	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	10	—	—	20	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	—	40	80	—	40	100	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	40	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ – 0.2V, $V_{IN} \leq$ 0.2V	—	4	20	—	4	25	mA
I_{CC}/f(2,3)	Increase in Power Supply Current MHz	V_{CC} = Max., f > 10 MHz	—	—	4	—	—	6	mA/ MHz
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}(4)	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	—	0.4	—	—	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_O = GND	-20	—	—	-20	—	—	mA

NOTES: 2580 tbl 03

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. Icc is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: Icc = 80+ 4(f –10)mA; for the military range, Icc = 100 + 6(f –10). f = operating frequency in MHz, f = 1/t_{MUC} for IDT7216 and f = 1/t_{MC} for IDT7217.
3. For frequencies greater than 10MHz, guaranteed by design, not production tested.
4. I_{OL} = 8mA for t_{MC} = 20 to 55ns

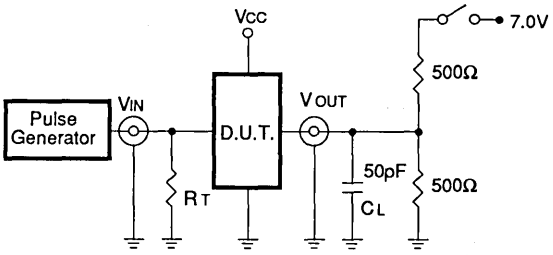


Figure 1. AC Test Load Circuit

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2580 tbl 08

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2580 tbl 09

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

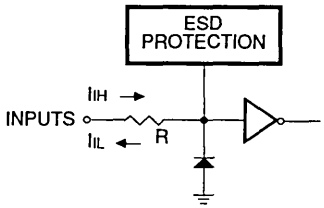


Figure 2. Input Interface Circuit

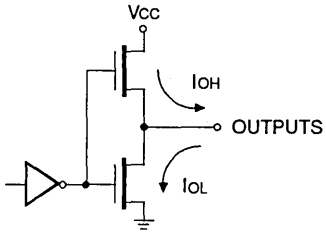


Figure 3. Output Interface Circuit

5

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0° to +70°C)

Symbol	Parameter	7216L20/25 7217L20/25 Min.	7216L20/25 7217L20/25 Max.	7216L35/45 7217L35/45 Min.	7216L35/45 7217L35/45 Max.	7216L55/65 7217L55/65 Min.	7216L55/65 7217L55/65 Max.	Unit
t_{MUC}	Unclocked Multiply Time	—	30/38	—	55/65	—	75/85	ns
t_{MC}	Clocked Multiply Time	—	20/25	—	35/45	—	55/65	ns
t_S	X, Y, RND Set-up Time	11/12	—	12/15	—	20	—	ns
t_H	X, Y, RND Hold Time	1/2	—	3	—	3	—	ns
t_{PWH}	Clock Pulse Width High	9/10	—	10/15	—	15	—	ns
t_{PWL}	Clock Pulse Width Low	9/10	—	10/15	—	20	—	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out	—	18/20	—	25	—	25/30	ns
t_{PDP}	Output Clock to P	—	18/20	—	25	—	30	ns
t_{PDY}	Output Clock to Y	—	18/20	—	25	—	30	ns
t_{ENA}	3-State Enable Time	—	18/20	—	25	—	30/35	ns
t_{DIS}	3-State Enable Time[2]	—	18/20	—	22	—	25	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	—	10	—	10	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	0/2	—	3	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	ns

NOTES:
2580 tbl 06

1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage.
3. Guaranteed by design, not production tested.

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = −55° to +125°C)

Symbol	Parameter	7216L25/30 7217L25/30 Min.	7216L25/30 7217L25/30 Max.	7216L40/55 7217L40/55 Min.	7216L40/55 7217L40/55 Max.	7216L65/75 7217L65/75 Min.	7216L65/75 7217L65/75 Max.	Unit
t_{MUC}	Unclocked Multiply Time	—	38/43	—	60/75	—	85/95	ns
t_{MC}	Clocked Multiply Time	—	25/30	—	40/55	—	65/75	ns
t_S	X, Y, RND Set-up Time	12	—	15/20	—	25	—	ns
t_H	X, Y, RND Hold Time	2	—	3	—	3	—	ns
t_{PWH}	Clock Pulse Width High	10	—	15	—	15	—	ns
t_{PWL}	Clock Pulse Width Low	10	—	15	—	15	—	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out	—	20	—	25/30	—	35	ns
t_{PDP}	Output Clock to P	—	20	—	25/30	—	30/35	ns
t_{PDY}	Output Clock to Y	—	20	—	25/30	—	30/35	ns
t_{ENA}	3-State Enable Time	—	20	—	25	—	35/40	ns
t_{DIS}	3-State Enable Time[2]	—	22	—	25	—	25	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	—	12/15	—	15	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	2	—	3	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	ns

NOTES:
2580 tbl 07

1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage.
3. Guaranteed by design, not production tested.

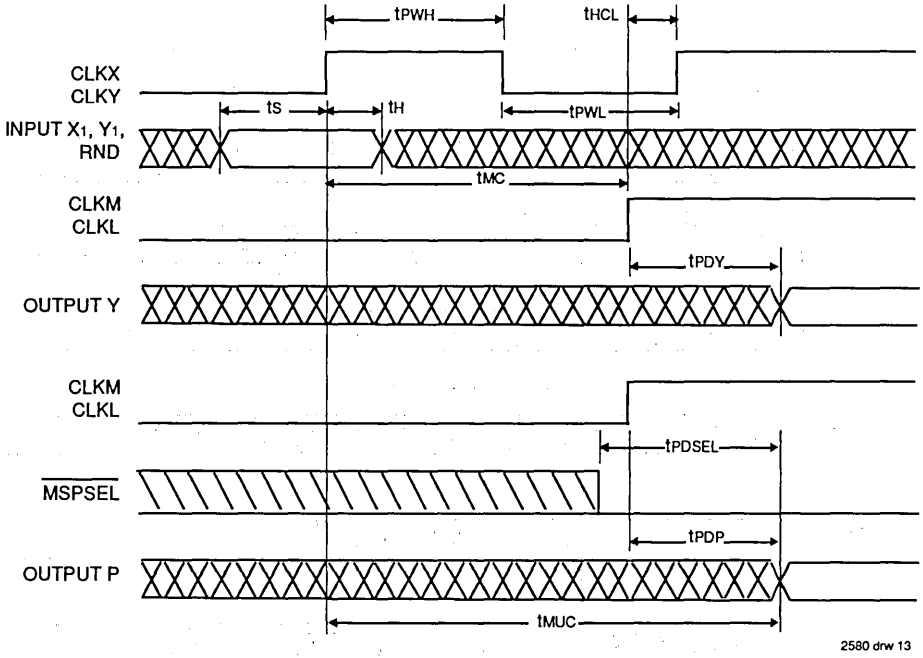


Figure 4. IDT7216 Timing Diagram

5

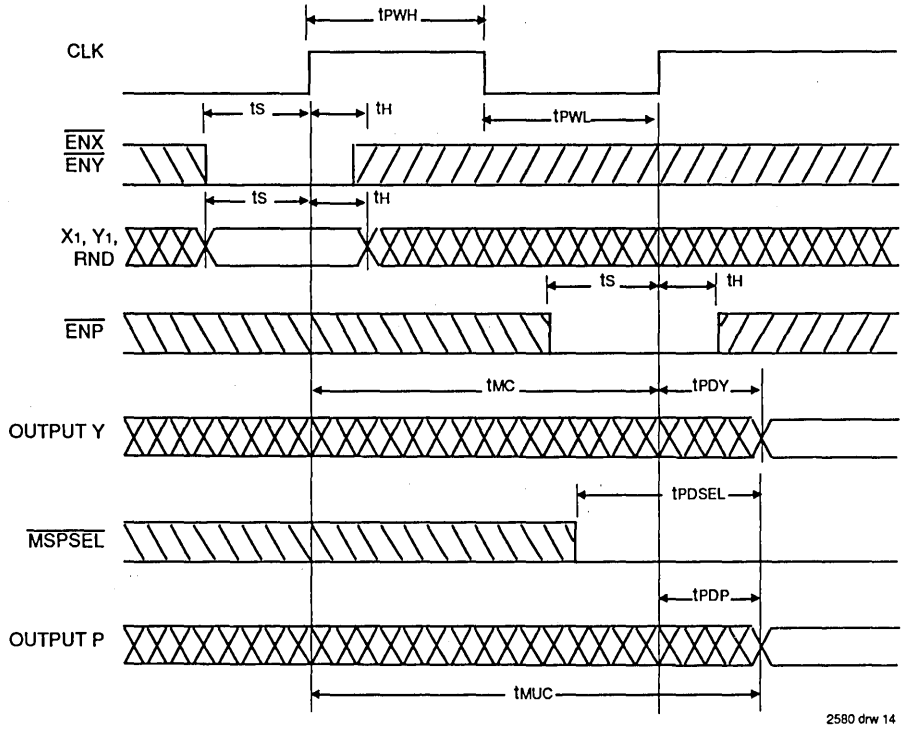


Figure 5. IDT7217 Timing Diagram

SIGNAL DESCRIPTION:

INPUTS:

X_{IN} (X_{15} through X_0)
Sixteen multiplicand data inputs

Y_{IN} (Y_{15} through Y_0)
Sixteen multiplier data inputs. (This is also an output port for P_{15-0})

INPUT CLOCKS (IDT7216 ONLY)

CLKX
The rising edge of this clock loads the X_{15-0} data input register along with the X mode and round registers.

CLKY
The rising edge of this clock loads the Y_{15-0} data input register along with the Y mode and round registers.

CLKM
The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL
The rising edge of this clock loads the Least Significant Product (LSP) register.

INPUT CLOCKS (IDT7217 ONLY)

CLK
The rising edge of this clock loads all registers.

$\overline{ENX}$
Register enable for the X_{15-0} data input register along with the X mode and round registers.

$\overline{ENY}$
Register enable for the Y_{15-0} data input register along with the Y mode and round registers.

$\overline{ENP}$
Register enable for the Most Significant Product (MSP) and Least Significant Product (LSP).

CONTROLS

X_M, Y_M (TCX, TCY)[1]
Mode control inputs for each data word. A LOW input designates unsigned data input and a HIGH input designates two's complement.

FA (RS)[1]
When the format adjust control is HIGH, a full 32-bit product is selected. When this control is LOW, a left-shifted 31-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional two's complement applications (see Multiplier Input/Output Formats).

FT
When this control is HIGH, both the Most Significant Product (MSP) and Least Significant Product (LSP) registers are transparent.

$\overline{OEL}$
Three-state enable for routing LSP through Y_{IN}/LSP_{OUT} port.

$\overline{OEP}$
Three-state enable for the product output port.

RND
Round control for the rounding of the Most Significant Product (MSP). When this control is HIGH, a one is added to the Most Significant Bit (MSB) of the Least Significant Product (LSP). Note that this bit depends on the state of the format adjust (FA) control. If FA is LOW when RND is HIGH, a one will be added to the 2^{-16} bit (P_{14}). If FA is HIGH when RND is HIGH, a one will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

$\overline{MSPSEL}$
When the $\overline{MSPSEL}$ is LOW, the Most Significant Product (MSP) is selected. When HIGH, the Least Significant Product (LSP) is available at the product output port.

OUTPUTS

MSP (P_{31} through P_{16})
Most Significant Product output.

LSP (P_{15} through P_0)
Least Significant Product output.

Y_{15-0} /LSPOUT (Y_{15} through Y_0 or P_{15} through P_0)
Least Significant Product (LSP) output available when $\overline{OEL}$ is LOW. This is also an output port for Y_{15-0}.

5

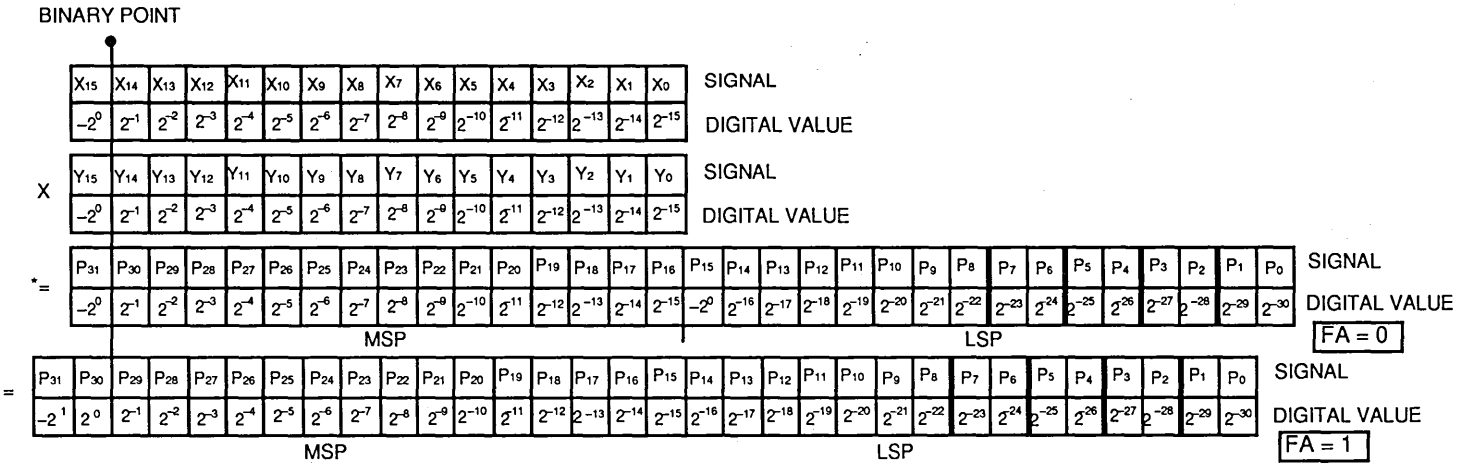


Figure 6. Fractional Two's Complement Notation

2580 drw 16

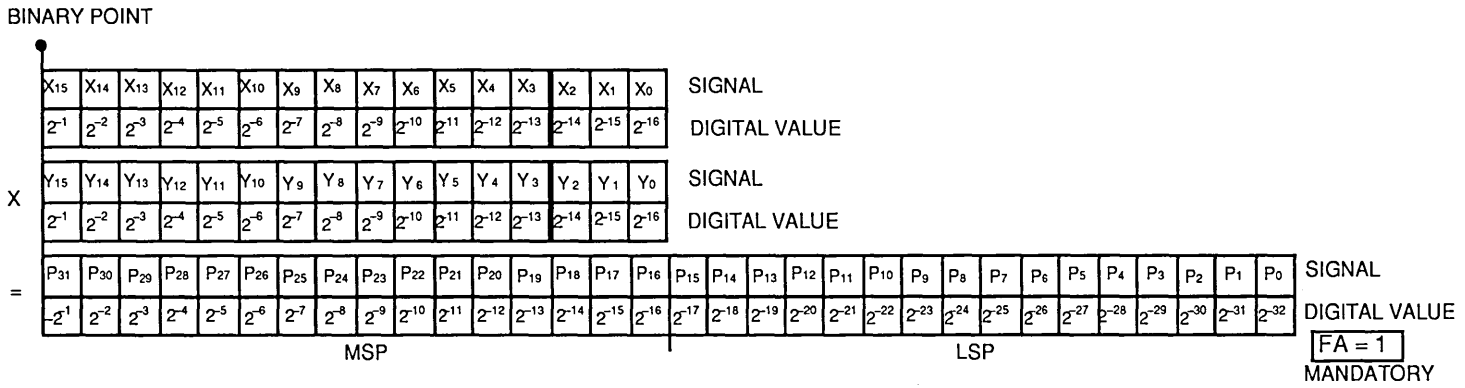


Figure 7. Fractional Unsigned Magnitude Notation

2580 drw17

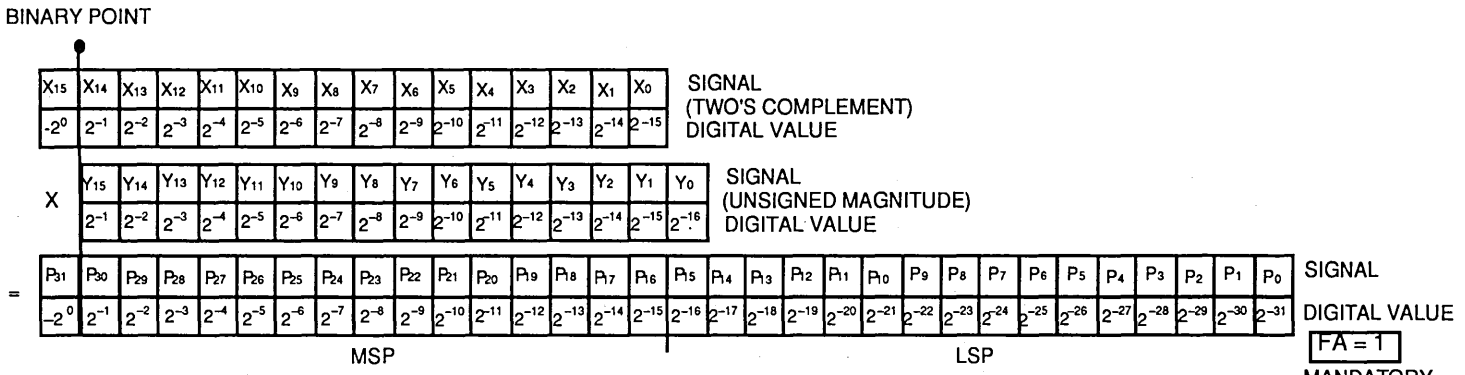


Figure 8. Fractional Mixed Mode Notation

2580 drw 18

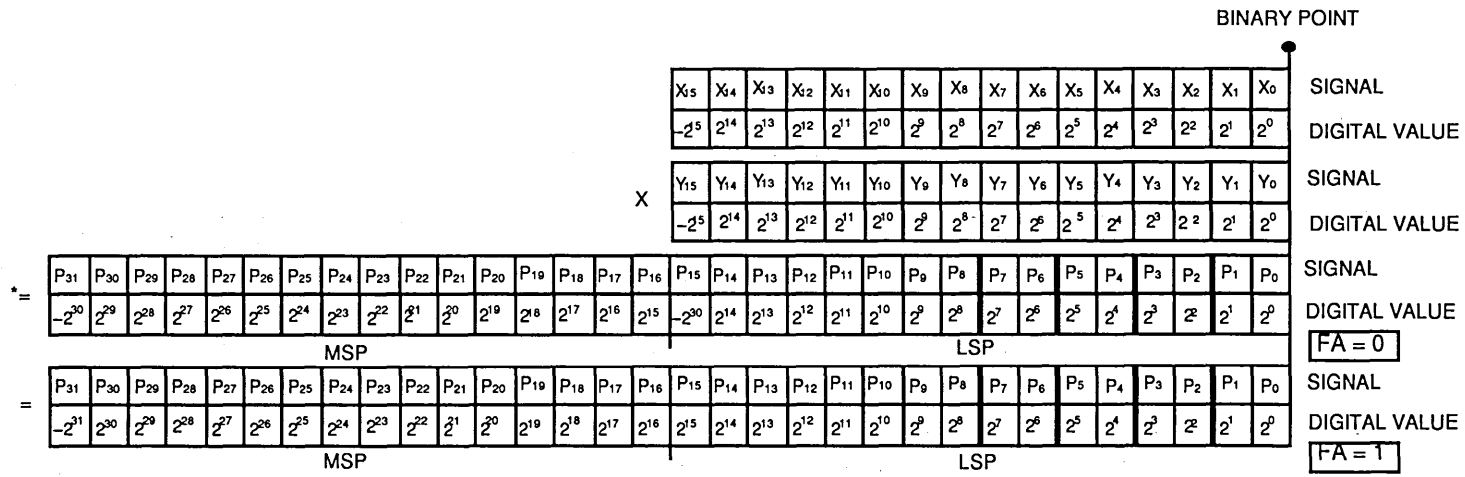


Figure 9. Integer Two's Complement Notation

2580 drw 19

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000.0 yielding an erroneous product of –1 in the fraction case and -2^{30} in the integer case.

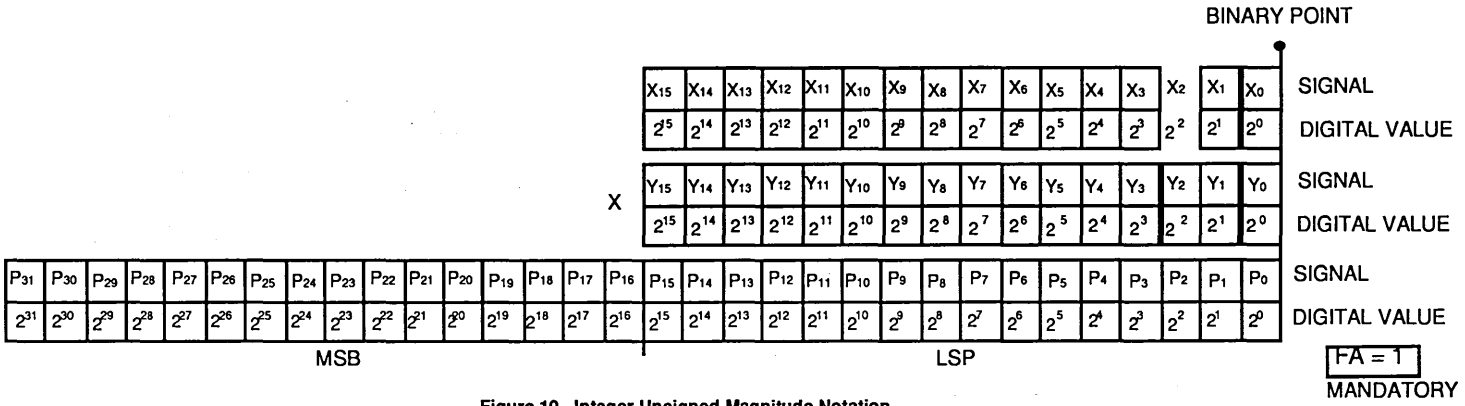


Figure 10. Integer Unsigned Magnitude Notation

2580 drw 20

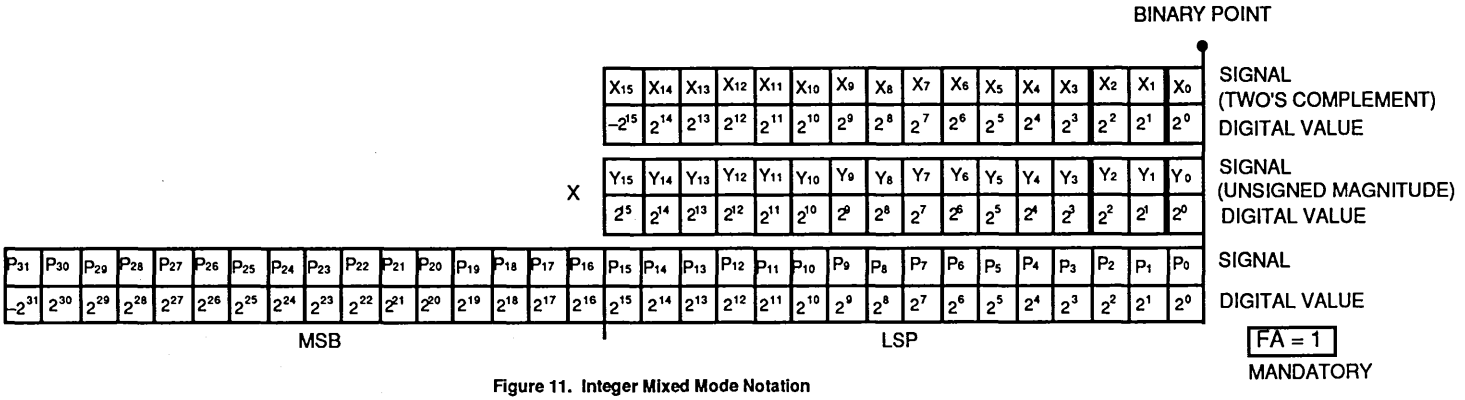
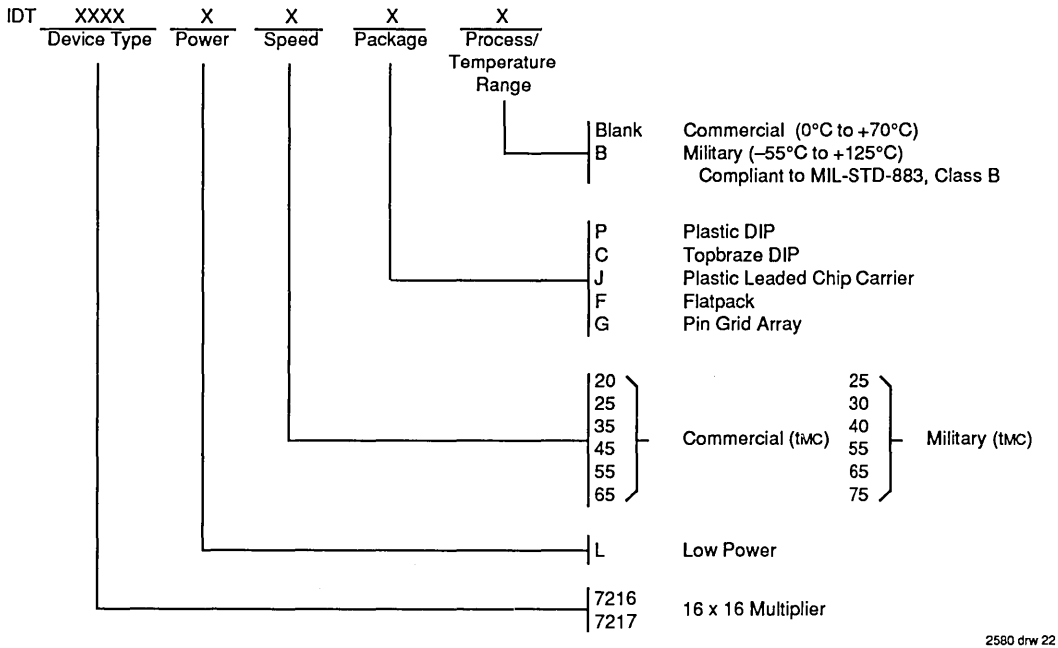


Figure 11. Integer Mixed Mode Notation

2580 drw 21

ORDERING INFORMATION



5

Integrated Device Technology, Inc.

16-BIT CMOS CASCADABLE ALU

IDT7381
IDT7383

FEATURES:

- High-performance 16-bit Arithmetic Logic Unit (ALU)
- 20ns to 55ns clocked ALU operations
- Ideal for radar, sonar or image processing applications
- IDT7381:
  - — 54/74S381 instruction set (8 functions)
  - — Replaces Gould S614381 or Logic Devices L4C381
  - — Cascadable with or without carry look-ahead
- IDT7383:
  - — 32 advanced ALU functions
  - — Cascadable without carry look-ahead
- Pipeline or flow-through modes
- Internal feedback path for accumulation
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CEMOS™ high-performance technology
- Available in 68-lead PGA and 68-pin surface mount PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7381 and IDT7383 are high-speed cascadable Arithmetic Logic Unit (ALUs). Both three-bus devices have two input registers, ultra-fast 16-bit ALUs and 16-bit output registers. With IDT's high-performance CEMOS technology, the IDT7381/7383 can do arithmetic or logic operations in 20ns. The IDT7381 functionally replaces four 54/74S381 four-bit ALUs in a 68-pin package.

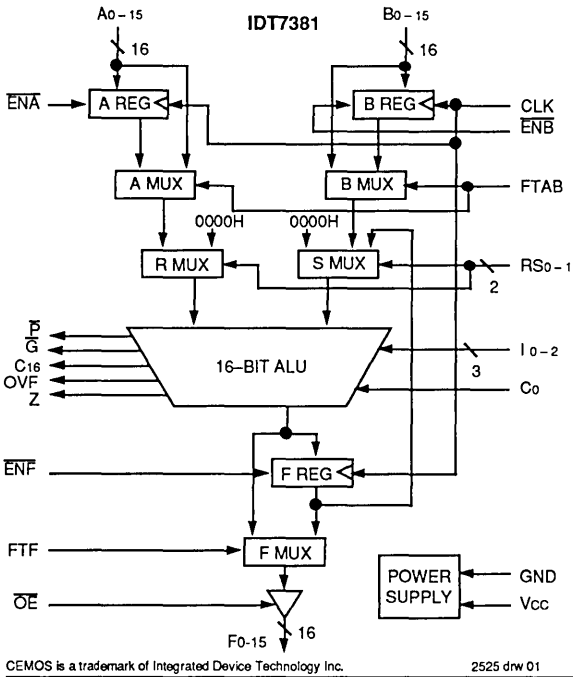
The two input operands, A and B, can be clocked or fed through for flexible pipelining. The F output can also be set into clocked or flow-through mode. An output enable is provided for three-state control of the output port on a bus.

The IDT7381 has three function pins to select 1 of 8 arithmetic or logic operations. The two R and S selection pins determine whether A, B, F or 0 are fed into the ALU. This ALU has carry-out, propagate and generate outputs for cascading using carry look-ahead.

The IDT7383 has five function pins to select 1 of 32 arithmetic or logic operations and the R, S input selections to the ALU. The R and S ALU inputs can be A, B, F, 0 or all 1s. This ALU has a carry-out pin for cascading.

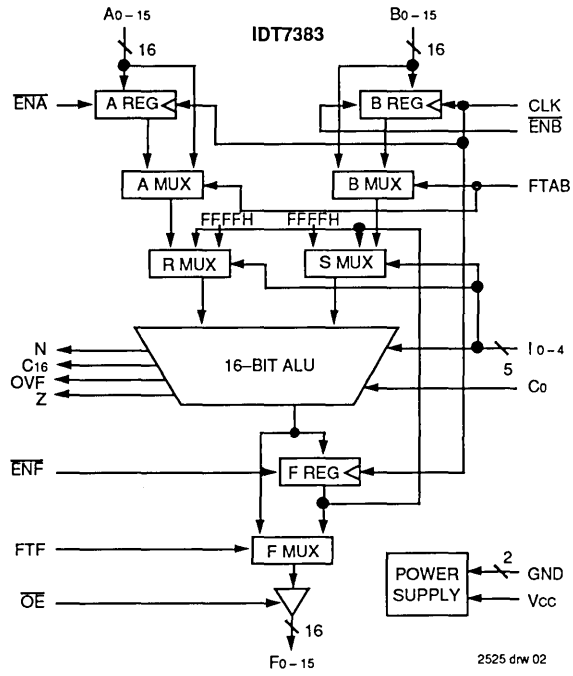
The IDT7381 and IDT7383 are available in 68-pin PLCC or PGA packages. Military grade product is manufactured in compliant with the latest revision of MIL-STD-883, Class B, for high reliability systems.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology Inc.

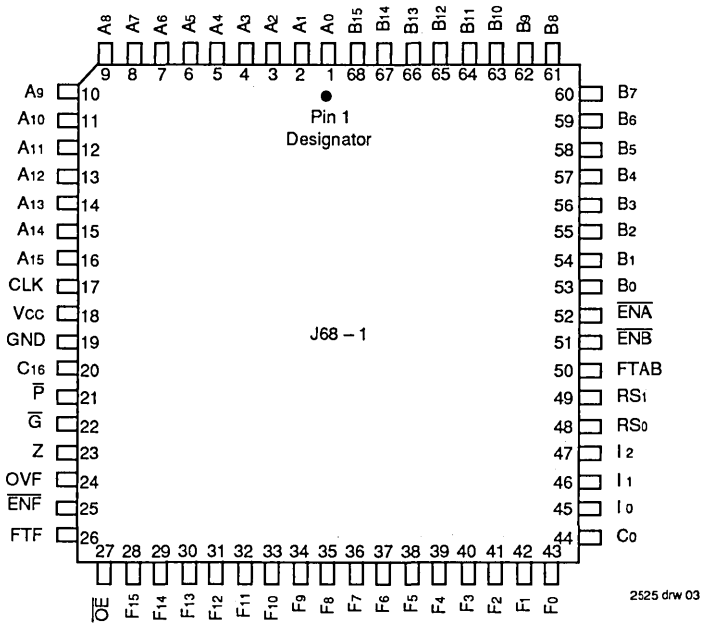
2525 drw 01



2525 drw 02

PIN CONFIGURATION

IDT7381



PLCC
TOPVIEW

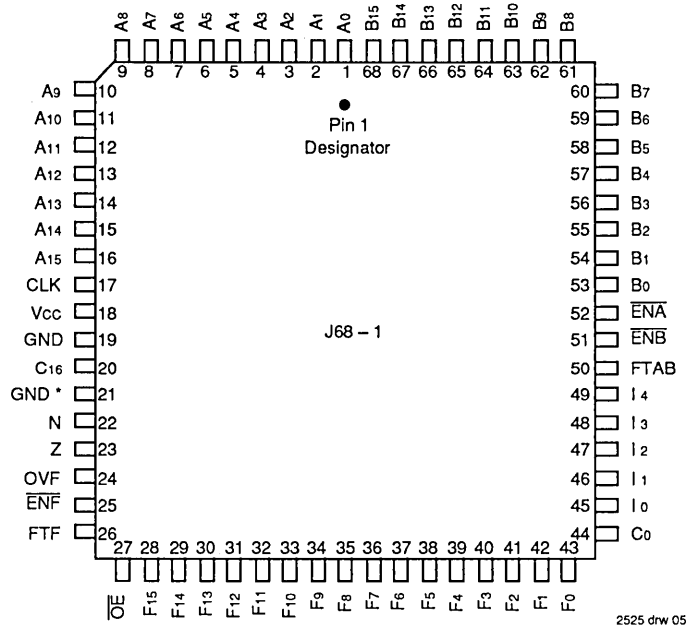
11		B7	B6	B4	B2	B0	ENB	RS1	I2	I0	
10	B9	B8	B5	B3	B1	ENA	FTAB	RS0	I1	C0	F0
09	B11	B10								F2	F1
08	B13	B12								F4	F3
07	B15	B14								F6	F5
06	A1	A0				G68 – 1				F8	F7
05	A3	A2								F10	F9
04	A5	A4								F12	F11
03	A7	A6								F14	F13
02	A8	A9	A11	A13	A15	VCC	C16	G	OVF	OE	F15
01		A10	A12	A14	CLK	GND	P	Z	ENF	FTF	
		A	B	C	D	E	F	G	H	J	K	L

Pin 1
Designator

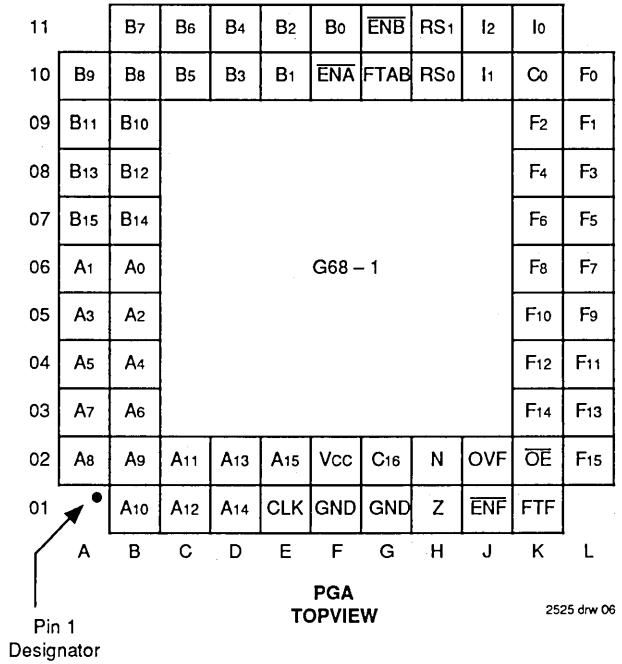
PGA
TOPVIEW

2525 drw 04

IDT7383



PLCC
TOPVIEW



PGA
TOPVIEW

PIN DESCRIPTIONS

IDT7381 AND IDT7383 PINS

Pin Name	I/O	Description
A_0 - A_{15}	I	Sixteen–bit data input port.
B_0 - B_{15}	I	Sixteen–bit data input port.
$\overline{ENA}$	I	Register enable for the A input port; active low pin.
$\overline{ENB}$	I	Register enable for the B input port; active low pin.
FTAB	I	Flow–through control pin. When this pin is high, both register A and B are transparent.
F_0 – F_{15}	O	Sixteen–bit data output port.
$\overline{ENF}$	I	Register enable for the F output port; active low pin.
FTF	I	Flow–through control pin. When this pin is high, the F register is transparent.
CLK	I	Clock input.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port F is in a high impedance state. When low, the output port F is active.
C_0	I	Carry input. This pin receives arithmetic carries from less significant ALU components in a cascade configuration.
C_{16}	O	Carry output. This pin produces arithmetic carries to more significant ALU components in a cascaded configuration.
OVF	O	This pin indicates a two's complement arithmetic overflow, when high.
Z	O	This pin indicates a zero output result, when high.
V_{CC}		Power supply pin, 5V.
GND		Ground pin, 0V. There are two ground pins on the IDT7383.

2525 tbl 01

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IDT7381 PINS

Pin Name	I/O	Description
RS_0 – RS_{15}	I	Two control pins used to select input operands for the R and S multiplexers.
I_0 - I_2	I	Three control pins to select the ALU function performed.
$\overline{P}$	O	Indicates the carry propagate output state to the ALU.
$\overline{G}$	O	Indicates the carry generate output state to the ALU.

2525 tbl 02

IDT7381 R AND S MUX TABLE

RS_0	RS_1	R Mux	S Mux
0	0	A	F
0	1	A	0
1	0	0	B
1	1	A	B

2525 tbl 03

IDT7381 ALU FUNCTION TABLE

I_2	I_1	I_0	Function
0	0	0	F = 0
0	0	1	$F = \overline{R} + S + C_0$
0	1	0	$F = R + \overline{S} + C_0$
0	1	1	$F = R + S + C_0$
1	0	0	F = R xor S
1	0	1	F = R or S
1	1	0	F = R and S
1	1	1	F = all 1's

2525 tbl 04

PIN DESCRIPTIONS (Continued)

IDT7383 PINS

Pin Name	I/O	Description
$I_0 - I_4$	I	Five control pins to select the ALU function performed.
N	O	The sign bit of an ALU operation.

2525 tbl 05

IDT7383 ALU FUNCTION TABLE

I_4	I_3	I_2	I_1	I_0	Function
0	0	0	0	0	F = A + B + Co
0	0	0	0	1	F = A or B
0	0	0	1	0	F = A - B
0	0	0	1	1	$F = \overline{A} + B + Co$
0	0	1	0	0	F = A + Co
0	0	1	0	1	$F = \overline{A}$ or F
0	0	1	1	0	F = A – 1 + Co
0	0	1	1	1	$F = \overline{A} + Co$
0	1	0	0	0	F = A + F + Co
0	1	0	0	1	F = A or F
0	1	0	1	0	$F = A + \overline{F} + Co$
0	1	0	1	1	$F = \overline{A} + F + Co$
0	1	1	0	0	F = F + B + Co
0	1	1	0	1	$F = \overline{A}$ or B
0	1	1	1	0	$F = F + \overline{B} + Co$
0	1	1	1	1	$F = \overline{F} + B + Co$
1	0	0	0	0	F = A xor B
1	0	0	0	1	F = A and B
1	0	0	1	0	$F = \overline{A}$ and B
1	0	0	1	1	F = A xnor B
1	0	1	0	0	F = A xor F
1	0	1	0	1	F = A and F
1	0	1	1	0	$F = \overline{A}$ and F
1	0	1	1	1	F = all 1's + Co
1	1	0	0	0	F = B + Co
1	1	0	0	1	$F = A$ and $\overline{B}$
1	1	0	1	0	$F = \overline{B} + Co$
1	1	0	1	1	F = B – 1 + Co
1	1	1	0	0	F = F + Co
1	1	1	0	1	$F = A$ or $\overline{B}$
1	1	1	1	0	F = F – 1 + Co
1	1	1	1	1	$F = \overline{F} + Co$

2525 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	−0.5 to V_{CC} + 0.5	−0.5 to V_{CC} + 0.5	V
V_{CC}	Power Supply Voltage	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2525 tbl 07

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Under no circumstances should an input of an I/O Pin be greater than V_{CC} + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2525 tbl 09

1. This parameter is sampled at initial characterization and is not production tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5V		—	—	−10	µA
I_{OS}(3)	Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−20	—	−100	mA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.5V	—	−0.1	−20	µA
			V_O = 2.7V	—	−0.1	20	
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −4mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4mA MIL.	—	—	0.5	V
			I_{OL} = 8mA COM'L.				

NOTES: 2525 tbl 08

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = V_{CC} = −0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{CC} = Max.	COM'L.	—	2	10	mA
	TTL Inputs HIGH	V_{IN} = V_{LC} or V_{HC}	MIL.	—	2	15	
I_{CCQT}[3]	Quiescent Power Supply Current	V_{CC} = Max.	COM'L.	—	15	45	mA
	TTL Inputs HIGH	V_{IN} = 3.4V	MIL.	—	15	55	
I_{CCD1}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Disabled $\overline{OE}$ = HIGH f_{CP} = 10MHz 50% Duty Cycle $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$	COM'L.	—	10	35	mA
			MIL.	—	10	55	
I_{CCD2}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Disabled $\overline{OE}$ = HIGH f_{CP} = 20MHz 50% Duty Cycle $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$	COM'L.	—	30	60	mA
			MIL.	—	30	80	

2525 tbl 10

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C)

Maximum Combinational Propagation Delays

From Input	IDT7381L20 IDT7383L20				IDT7381L25 IDT7383L25				IDT7381L30 IDT7383L30				Unit
	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	
FTAB = 0, FTF = 0													
CLK	11	20	20	20	13	22	26	22	20	28	30	28	ns
C_0	—	—	14	14	—	—	16	16	—	—	20	20	ns
I_{0-4}, RS_0, RS_1	—	18	20	18	—	22	22	22	—	28	28	28	ns
FTAB = 0, FTF = 1													
CLK	20	20	20	20	27	22	26	22	33	28	30	28	ns
C_0	18	—	14	14	22	—	16	16	28	—	20	20	ns
I_{0-4}, RS_0, RS_1 (1)	20	18	20	18	22	22	22	22	28	28	28	28	ns
FTAB = 1, FTF = 0													
A_0–A_{15}, B_0–B_{15}	—	16	20	17	—	18	25	22	—	24	30	28	ns
CLK	11	—	—	—	13	—	—	—	19	—	—	—	ns
C_0	—	—	14	14	—	—	16	16	—	—	20	20	ns
I_{0-4}, RS_0, RS_1 (1)	—	18	20	18	—	22	22	22	—	28	28	28	ns
FTAB = 1, FTF = 1													
A_0–A_{15}, B_0–B_{15}	20	16	20	17	26	18	25	22	32	24	30	28	ns
C_0	18	—	14	14	22	—	16	16	28	—	20	20	ns
I_{0-4}, RS_0, RS_1 (1)	20	18	20	18	22	22	22	22	28	28	28	28	ns

2525 tbl 11

5

Maximum Combinational Propagation Delays

From Input	IDT7381L40 IDT7383L40				IDT7381L55 IDT7383L55				Unit
	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z, OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z, OVF	C_{16}	
FTAB = 0, FTF = 0									
CLK	26	30	44	32	32	38	53	36	ns
C_0	—	—	28	20	—	—	34	22	ns
I_{0-4}, RS_0, RS_1	—	32	34	35	—	42	42	42	ns
FTAB = 0, FTF = 1									
CLK	46	30	44	32	56	38	53	36	ns
C_0	30	—	28	20	37	—	34	22	ns
I_{0-4}, RS_0, RS_1 (1)	40	32	34	35	55	42	42	42	ns
FTAB = 1, FTF = 0									
A_0–A_{15}, B_0–B_{15}	—	30	40	32	—	36	46	37	ns
CLK	26	—	—	—	32	—	—	—	ns
C_0	—	—	28	20	—	—	34	22	ns
I_{0-4}, RS_0, RS_1 (1)	—	32	34	35	—	42	42	42	ns
FTAB = 1, FTF = 1									
A_0–A_{15}, B_0–B_{15}	40	30	40	32	55	36	46	37	ns
C_0	30	—	28	20	37	—	34	22	ns
I_{0-4}, RS_0, RS_1 (1)	40	32	34	35	55	42	42	42	ns

2525 tbl 12

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C) - (Cont'd.)

Minimum Set-up and Hold Times Relative to Clock (CLK)

Input	IDT7381L20 IDT7383L20		IDT7381L25 IDT7383L25		IDT7381L30 IDT7383L30		IDT7381L40 IDT7383L40		IDT7381L55 IDT7383L55		Unit
	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	
FTAB = 0, FTF = X											
A_0–A_{15}, B_0–B_{15}	5	0	6	0	6	0	6	0	8	0	ns
C_0 (2)	12	0	16	0	16	0	16	0	21	0	ns
I_{0-4}, RS_0, RS_1 (1) (2)	15	0	24	0	29	0	32	0	44	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	5	0	6	0	6	0	6	0	8	0	ns
FTAB = 1, FTF = 0											
A_0–A_{15}, B_0–B_{15}	14	0	16	0	25	0	28	0	35	0	ns
C_0	12	0	16	0	16	0	16	0	21	0	ns
I_{0-4}, RS_0, RS_1 (1)	15	0	24	0	29	0	32	0	44	0	ns
$\overline{ENF}$	5	0	6	0	6	0	6	0	8	0	ns

2525 tbl 13

Minimum Clock Cycle Times and Pulse Widths

Parameter	IDT7381L20 IDT7383L20	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L40 IDT7383L40	IDT7381L55 IDT7383L55	Unit
Clock LOW Time	5	6	8	10	14	ns
Clock HIGH Time	5	6	8	10	14	ns
Clock Period	18	20	25	34	43	ns

2525 tbl 14

Maximum Output Enable/Disable Times

Parameter	IDT7381L20 IDT7383L20	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L40 IDT7383L40	IDT7381L55 IDT7383L55	Unit
Enable Time	8	10	15	18	20	ns
Disable Time	8	10	15	18	20	ns

2525 tbl 15

NOTES:
1. For IDT7381, pins I_0 – I_2, RS_0, RS_1 apply. For IDT7383, pins I_0 – I_4 apply.
2. Only for FTF = 0.

AC ELECTRICAL CHARACTERISTICS — MILITARY (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C)

Maximum Combinational Propagation Delays

From Input	IDT7381L25 IDT7383L25				IDT7381L30 IDT7383L30				IDT7381L35 IDT7383L35				Unit
	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	
FTAB = 0, FTF = 0													
CLK	14	24	24	24	26	28	34	28	27	32	45	32	ns
C_0	—	—	18	18	—	—	22	22	—	—	30	23	ns
I_{0-4}, RS_0, RS_1 (1)	—	22	24	22	—	28	28	28	—	34	34	34	ns
FTAB = 0, FTF = 1													
CLK	25	24	24	24	34	28	34	28	45	32	40	32	ns
C_0	21	—	18	18	26	—	22	22	30	—	30	23	ns
I_{0-4}, RS_0, RS_1 (1)	25	22	24	22	30	28	28	28	40	34	34	34	ns
FTAB = 1, FTF = 0													
A_0–A_{15}, B_0–B_{15}	—	20	25	22	—	28	28	28	—	30	35	32	ns
CLK	14	—	—	—	26	—	—	—	27	—	—	—	ns
C_0	—	—	18	18	—	—	22	22	—	—	30	23	ns
I_{0-4}, RS_0, RS_1 (1)	—	22	24	22	—	28	28	28	—	34	34	34	ns
FTAB = 1, FTF = 1													
A_0–A_{15}, B_0–B_{15}	25	22	25	22	30	28	28	28	40	30	30	32	ns
C_0	21	—	18	18	26	—	22	22	30	—	30	23	ns
I_{0-4}, RS_0, RS_1 (1)	25	22	24	22	30	28	28	28	40	34	34	34	ns

2525 tbl 16

Maximum Combinational Propagation Delays

From Input	IDT7381L45 IDT7383L45				IDT7381L65 IDT7383L65				Unit
	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z, OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z, OVF	C_{16}	
FTAB = 0, FTF = 0									
CLK	28	34	50	34	37	44	63	45	ns
C_0	—	—	32	23	—	—	42	25	ns
I_{0-4}, RS_0, RS_1 (1)	—	38	38	38	—	48	48	48	ns
FTAB = 0, FTF = 1									
CLK	56	34	50	34	68	44	63	45	ns
C_0	32	—	32	23	42	—	42	25	ns
I_{0-4}, RS_0, RS_1 (1)	46	38	38	38	66	48	48	48	ns
FTAB = 1, FTF = 0									
A_0–A_{15}, B_0–B_{15}	—	32	46	36	—	44	56	44	ns
CLK	28	—	—	—	37	—	—	—	ns
C_0	—	—	32	23	—	—	42	25	ns
I_{0-4}, RS_0, RS_1 (1)	—	38	38	38	—	48	48	48	ns
FTAB = 1, FTF = 1									
A_0–A_{15}, B_0–B_{15}	45	32	46	36	65	44	56	44	ns
C_0	32	—	32	23	42	—	42	25	ns
I_{0-4}, RS_0, RS_1 (1)	46	38	38	38	66	48	48	48	ns

2525 tbl 17

5

AC ELECTRICAL CHARACTERISTICS — MILITARY (Vcc = 5V ± 10%, TA = −55°C to +125°C) - (Cont'd)

Minimum Set-up and Hold Times Relative to Clock (CLK)

Input	IDT7381L25 IDT7383L25		IDT7381L30 IDT7383L30		IDT7381L35 IDT7383L35		IDT7381L45 IDT7383L45		IDT7381L65 IDT7383L65		Unit
	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	
FTAB = 0, FTF = X											
A_0–A_{15}, B_0–B_{15}	7	0	8	0	8	0	8	0	10	0	ns
C_0 (2)	14	0	18	0	19	0	20	0	25	0	ns
I_{0-4}, RS_0, RS_1 (1) (2)	19	0	30	0	32	0	36	0	50	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	7	0	8	0	8	0	8	0	10	0	ns
FTAB = 1, FTF = 0											
A_0–A_{15}, B_0–B_{15}	14	0	27	0	30	0	33	0	43	0	ns
C_0	14	0	18	0	19	0	20	0	25	0	ns
I_{0-4}, RS_0, RS_1 (1)	19	0	30	0	34	0	36	0	50	0	ns
$\overline{ENF}$	7	0	8	0	8	0	8	0	10	0	ns

2525 tbl 18

Minimum Clock Cycle Times and Pulse Widths

Parameter	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L35 IDT7383L35	IDT7381L45 IDT7383L45	IDT7381L65 IDT7383L65	Unit
Clock LOW Time	8	12	13	15	20	ns
Clock HIGH Time	8	12	13	15	20	ns
Clock Period	20	26	30	38	52	ns

2525 tbl 19

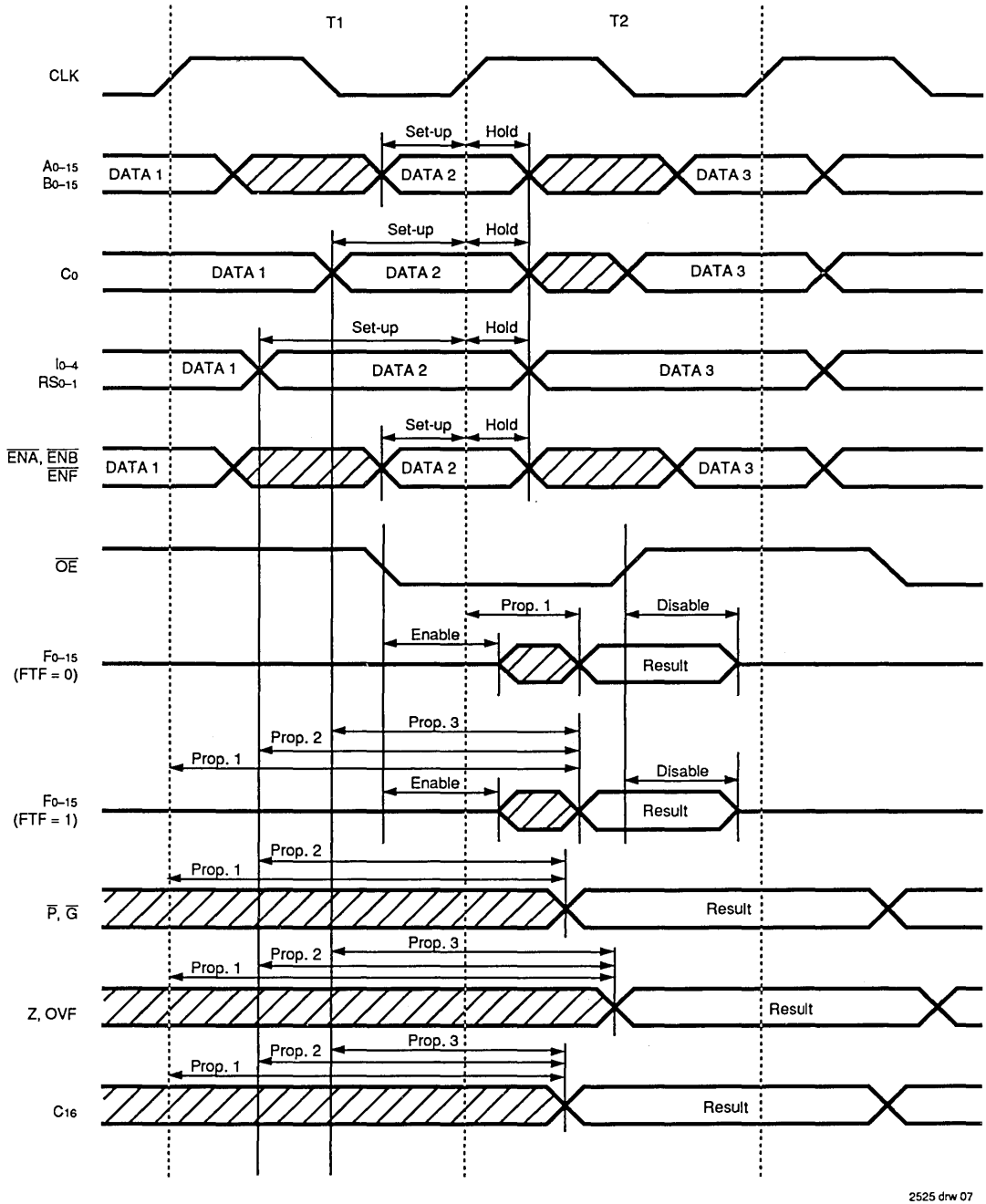
Maximum Output Enable/Disable Times

Parameter	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L35 IDT7383L35	IDT7381L45 IDT7383L45	IDT7381L65 IDT7383L65	Unit
Enable Time	14	18	19	20	22	ns
Disable Time	14	18	19	20	22	ns

2525 tbl 20

NOTES:
1. For IDT7381, pins I_0 – I_2, RS_0, RS_1 apply. For IDT7383, pins I_0 – I_4 apply.
2. Only for FTF = 0.

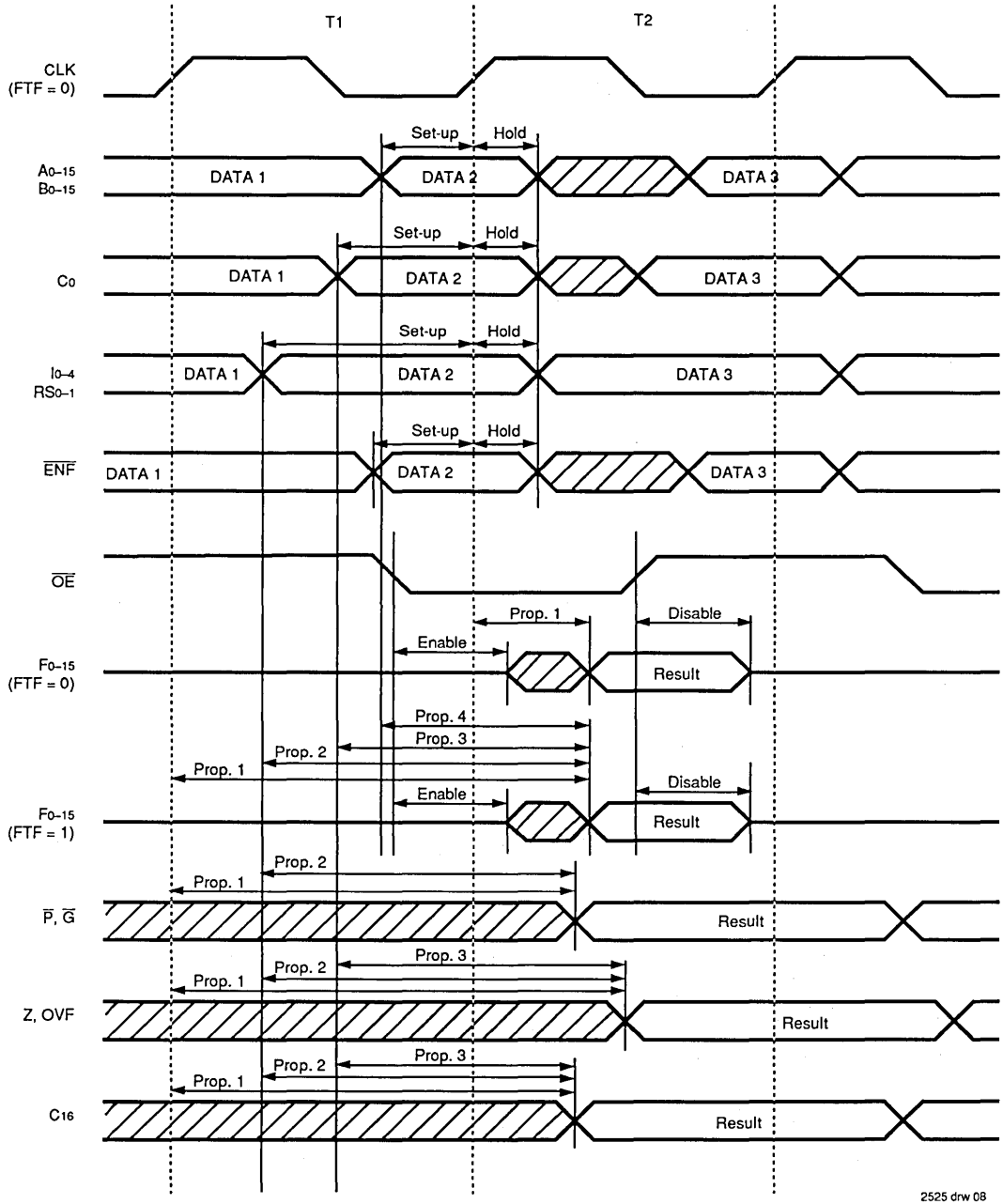
WAVEFORMS FOR FTAB = 0, FTF = X



2525 drw 07

Prop. 1: Propagation delay with respect to the CLK.
Prop. 2: Propagation delay with respect to I_{0-4}, RS_{0-2}.
Prop. 3: Propagation delay with respect to C_0.

WAVEFORMS FOR FTAB = 1, FTF = X



Prop. 1: Propagation delay with respect to the CLK.
Prop. 2: Propagation delay with respect to I0-4, RS0-2.
Prop. 3: Propagation delay with respect to C0.
Prop. 4: Propagation delay with respect to A, B.

PROPAGATION DELAY CALCULATIONS FOR TWO IDT7381/7383s

From Input	To Output		To Set PUT Time
	F_{0-15}	Flags [2]	Relative to Clock (CLK)
FTAB = 0, FTF = 0			
CLK	As in 16-bit case	(Clk → C_{16}) + (C_0 → flag)	....
C_0	....	(C_0 → C16) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-4}, RS_{0-1} [1]	....	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	....	....	As in 16-bit case
ENA, ENB,ENF	....	....	As in 16-bit case
FTAB = 0, FTF = 1			
CLK	(Clk → C_{16}) + (C_0 → F_{0-15})	(Clk → C_{16}) + (C_0 → flag)	....
C_0	(C_0 → C_{16}) + (C_0 → F_{0-15})	(C_0 → C_{16}) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-4}, RS_{0-1} [1]	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → F_{0-15})	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	....	....	As in 16-bit case
ENA, ENB,ENF	....	....	As in 16-bit case
FTAB = 1, FTF = 0			
CLK	As in 16-bit case	....	....
C_0	....	(C_0 → C_{16}) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-4}, RS_{0-1} [1]	....	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	....	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → flag)	As in 16-bit case
ENA, ENB,ENF	....	....	As in 16-bit case
FTAB = 0, FTF = 1			
CLK	Don't care condition	Don't care condition	....
C_0	(C_0 → C_{16}) + (C_0 → F_{0-15})	(C_0 → C_{16}) + (C_0 → flag)	....
I_{0-4}, RS_{0-1} [1]	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → F_{0-15})	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	....
A_{0-15}, B_{0-15}	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → F_{0-15})	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → flag)	....
ENA, ENB,ENF	....	....	....

NOTES:
1. For IDT7381, pins I_{0-2}, RS_{0-2} apply. For IDT7383, pins I_{0-4} apply.
2. Flags are $\overline{P}$, $\overline{G}$, OVF, Z, C_{16} for IDT7381. Flags are N, OVF, Z C_{16} for IDT7383.

2525 tbl 22

5

CASCADING THE IDT7381/3

Some applications require 32-bit or wider input operands. Cascading is the hardware solution. It provides a high speed alternative in handling more than 16-bit wide operands.

This section is divided in three parts:

1. Cascading the IDT7381
2. Cascading the IDT7383
3. Time delay considerations

1. Cascading the IDT7381

Cascading to 32-bit wide operands takes only two IDT7381s and no external hardware. However, cascading to data widths greater than 32-bit can be done in two ways: without external hardware (slow method) or by using a carry look ahead generator like the IDT39C02A or the FCT182 (fast method).

a) Cascading the IDT7381 without a carry-look-ahead generator: (Figures 2 and 3)

1. Connect the C_{16} output of the least significant device into the C_0 input of the next most significant device.
2. Common lines to all devices are: RS_{0-1}, I_{0-2}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
3. Take OVF, C_{16}, $\overline{P}$, $\overline{G}$ of the most significant device as valid.
4. The system's zero flag (Z) is obtained by ANDing all zero flag results.

b) Cascading three or more IDT7381s with carry-look-ahead (CLA) generator: (Figure 4)

1. Connect the $\overline{P}$ and $\overline{G}$ outputs of each device to the CLA generator's corresponding inputs.
2. Take the CLA generator outputs into the C_0 inputs of each device (except for the least significant one).
3. Common lines to all devices are: RS_{0-1}, I_{0-2}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
4. Take OVF, C_{16}, $\overline{P}$, $\overline{G}$ of the most significant device as valid.
5. Carry-in to the system should be connected to the C_0 input of the least significant device and also to the CLA generator.

2. Cascading the IDT7383

(Figures 5 and 6)

1. Connect the C_{16} output of the least significant device into the C_0 input of the next most significant device.
2. Common lines to all devices are: I_{0-4}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
3. Take OVF, C_{16}, N of the most significant device as valid.
4. The system's zero flag (Z) is obtained by ANDing all zero flag results.

3. Time Delay Considerations

Once cascading has taken place, time delays may become critical in high performance systems. Our main interest here is focused on "propagation delays", i.e. calculating the time required for an input signal to propagate through several cascaded devices up to a specific output in another device within the cascaded system.

Propagation Delay

The propagation delay *for two devices* between the input and output of interest (input to output delay) is done as follows:

1. Calculate delay between the input and C_{16} in the first device.
2. Calculate delay between C_0 and the output in the second device.
3. Add both results.

The following table is an example on how to build a propagation delay table for all inputs in a 32-bit IDT7381/3 cascaded system.

Propagation delay calculations can be extended to *n–cascaded* devices as the sum of the delays in all devices between the input and output of interest. That is:

$(Input)_1 \rightarrow (C_{16})_1 = t_1$

...

$(C_0)_i \rightarrow (C_{16})_i = t_i$

$(C_0)_{i+1} \rightarrow (C_{16})_{i+1} = t_{i+1}$

...

$(C_0)_n \rightarrow (Output)_n = t_n$

Where the subscript i denotes the device number and the arrow (→) represents the delay in between. Notice that i + 1 is the immediate upper device from device i. Adding the delays t_i we get:

Propagation delay = $t_1 + t_2 + ... + t_i + t_{i+1} + ... + t_n$

Total Delay

As seen from Figure 11, the propagation delay is within the IDT7381/3 devices only. A complete analysis should also include the delay associated with the transmission line Li (which depends on the line length and its impedance). This line delay should then be added to the propagation delay to obtain the total delay for the cascaded system:

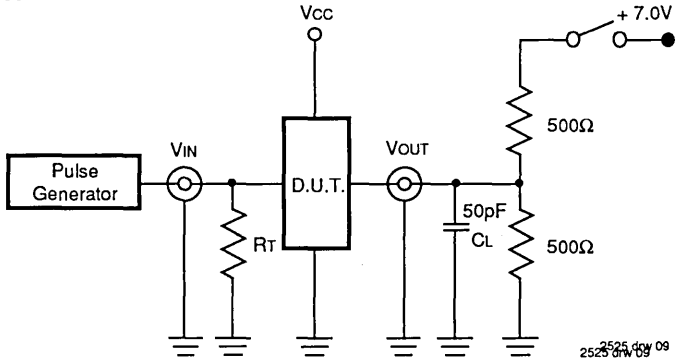
Total delay = Propagation delay + Transmission line delay

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

TEST LOAD CIRCUIT



DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_L = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 1. AC Test Load Circuit

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2525 tbl 21

Test	Switch
Open Drain Disable Low Enable Low	Closed
All other Outputs	Open

2525 tbl 23

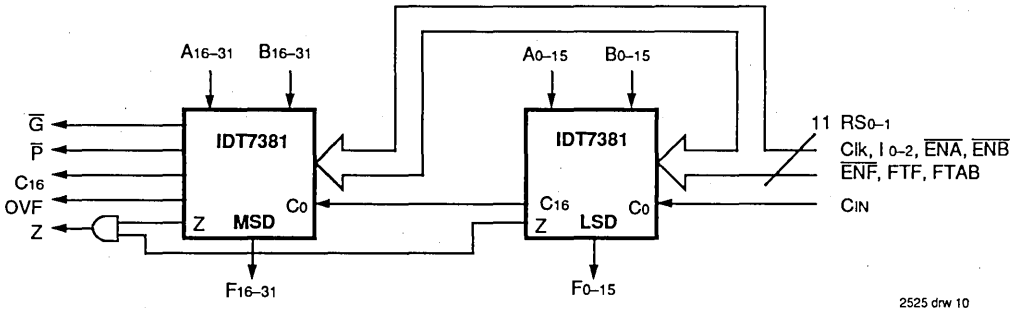


Figure 2. Cascading Two IDT7381s to 32 Bits

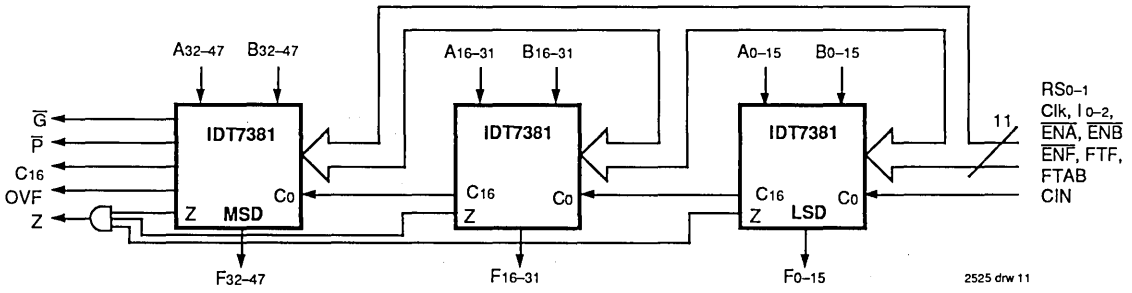


Figure 3. Cascading Three IDT7381s to 48 Bits Wide without a Carry-lookahead Generator

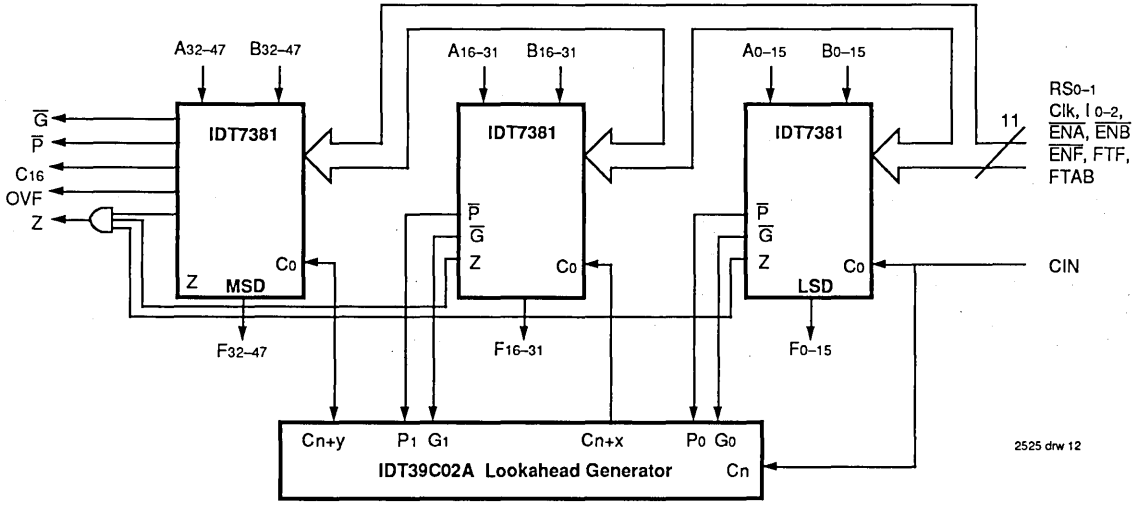


Figure 4. Cascading Three IDT7381s to 48 Bits Wide with a Carry-lookahead Generator

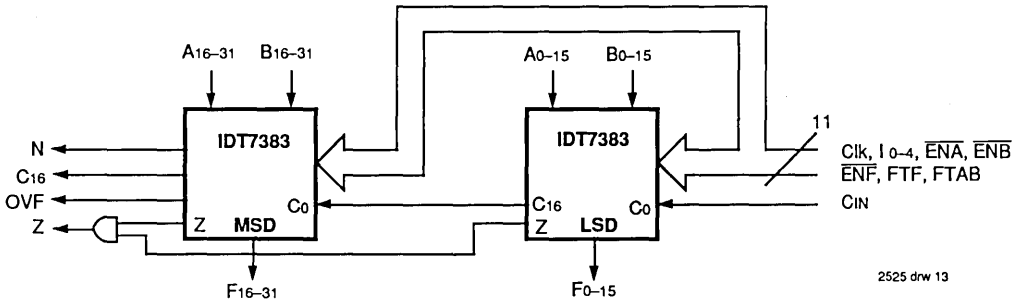


Figure 5. Cascading Two IDT7383s to 32 Bits

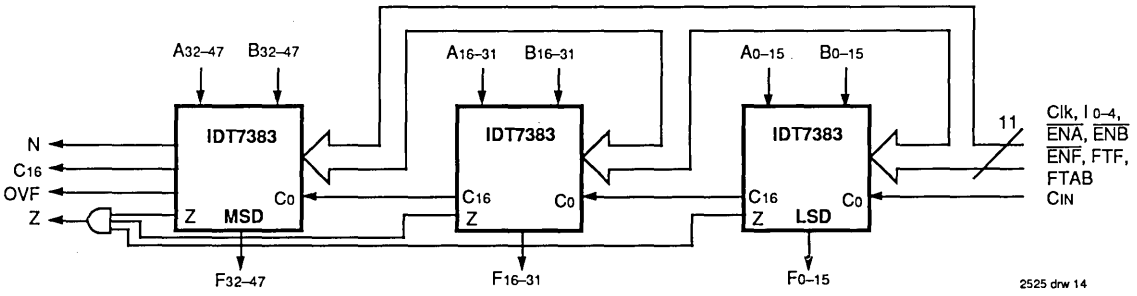


Figure 6. Cascading Three IDT7383s to 48 Bits

5

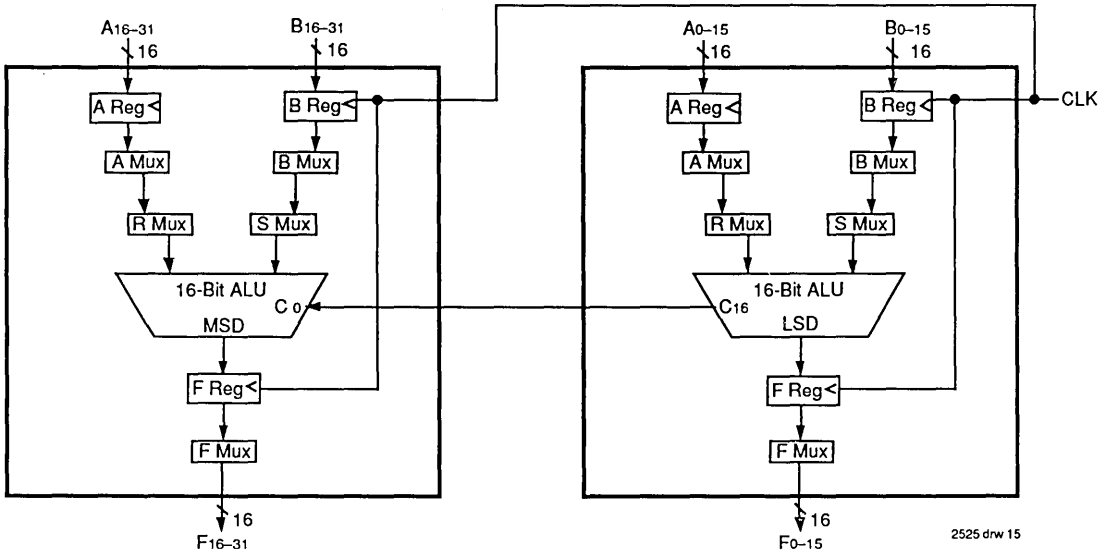


Figure 7. 32-Bit Configuration for FTAB = 0, FTF = 0

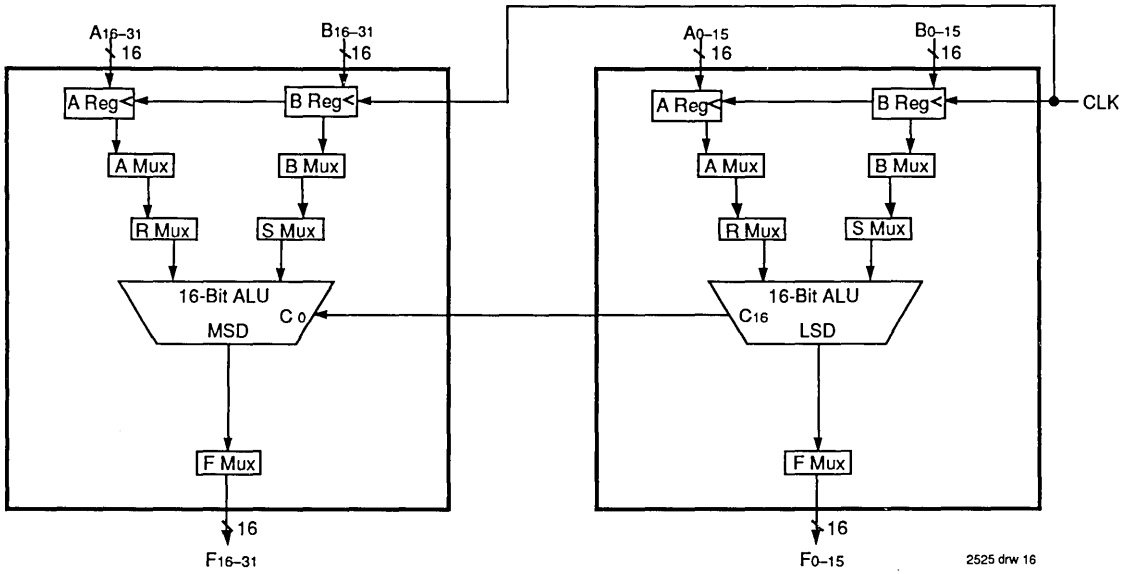


Figure 8. 32-Bit Configuration for FTAB = 0, FTF = 1

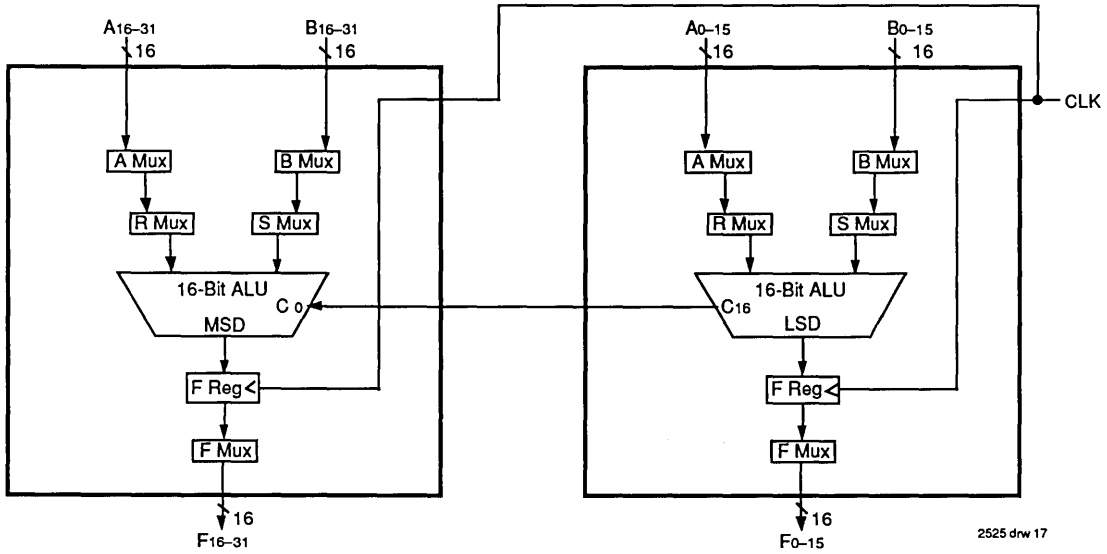


Figure 9. 32-Bit Configuration for FTAB = 1, FTF = 0

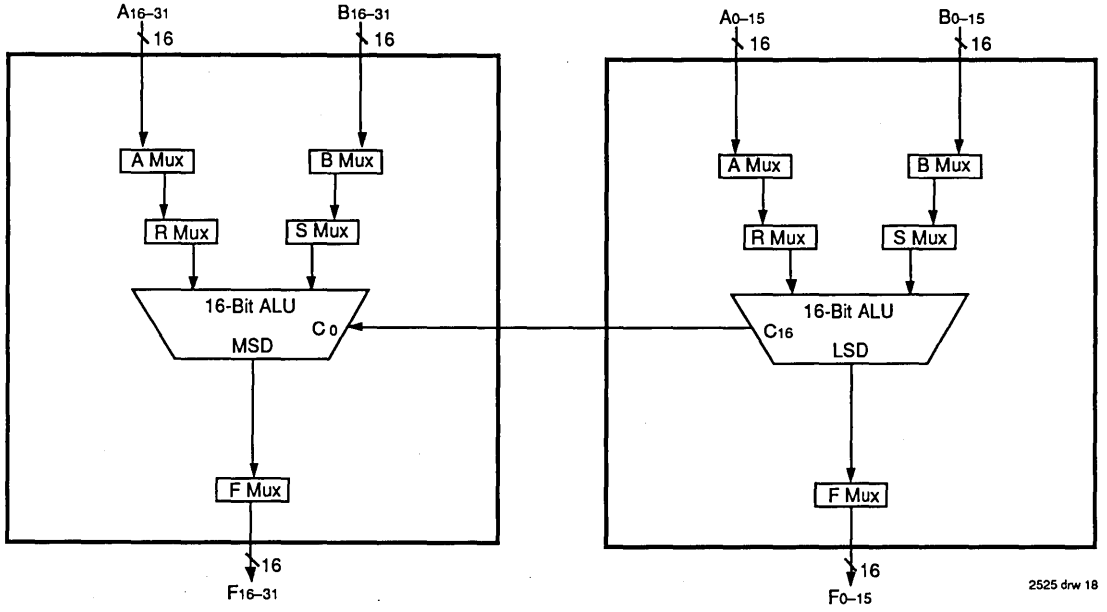


Figure 10. 32-Bit Configuration for FTAB = 1, FTF = 1

5

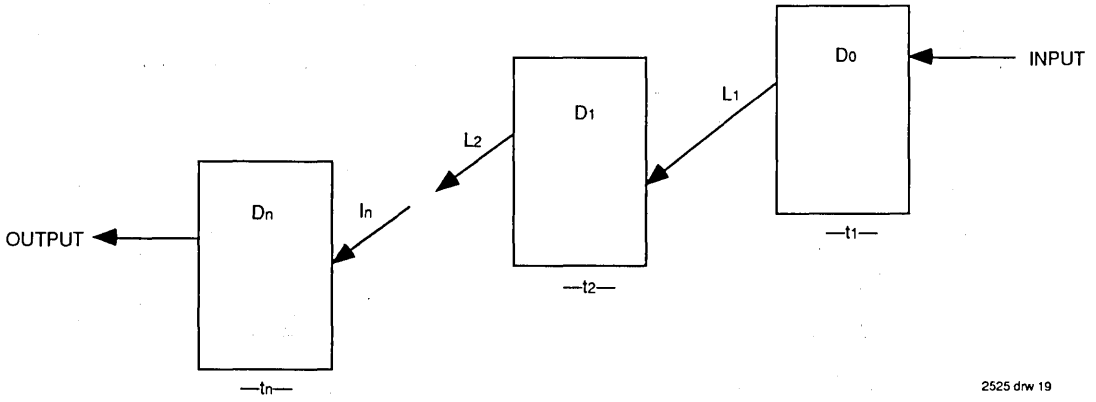
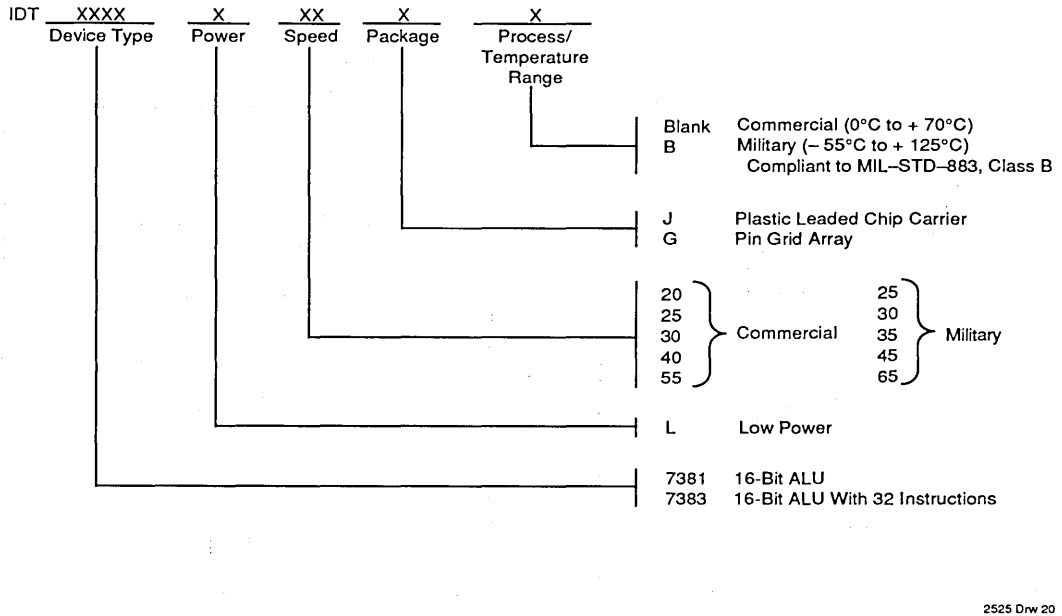


Figure 11. Propagation Delay = t1 + t2 + . . . + tn N-Cascaded Devices

ORDERING INFORMATION



Integrated Device Technology, Inc.

16-BIT CMOS MULTILEVEL PIPELINE REGISTERS

IDT73200
IDT73201

FEATURES:

- IDT73200: Eight 16-bit high-speed pipeline registers
- IDT73201: Seven 16-bit high-speed pipeline registers plus a direct feed-through path
- 12ns to 20ns access time
- Programmable multilevel register configurations
- Powerful instruction set: transfer, hold, load directly
- Functionally replaces four Am29520s
- Read/Write buffer for 32-bit RISC/CISC microprocessors
- Applications as temporary address storage or programmable pipeline registers for DSP products
- Coefficient storage for FIR filters
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CEMOS™ high-performance technology
- Available in 48-pin plastic and ceramic DIP and 52-pin surface mount PLCC and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT73200 and IDT73201 are mutilevel pipeline registers. With IDT's high-performance CEMOS™ technology, the IDT73200 and IDT73201 have access times of 12ns.

The IDT73200 contains eight 16-bit registers which can be configured as one 8-level, two 4-level , four 2-level or eight 1-level pipeline registers.

The IDT73201 contains seven 16-bit registers and a direct feed-through path. The seven registers can be configured as one 7-level, a 4-level plus a 3-level, three 2-level or seven 1-level pipeline registers.

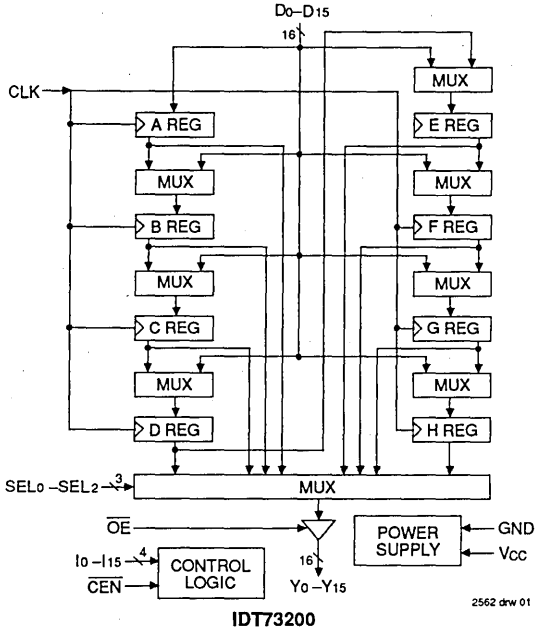
An eight-to-one output multiplexer allows data to be read from any one of the registers or from the feed-through path on the IDT73201. Three input control pins (SEL_0–SEL_2) select which of the multiplexer inputs are directed to the output (Y_0–Y_{15}).

These pipeline registers are ideal for high throughput, vector-oriented operations such as those in digital signal processing (DSP). The IDT73200 and IDT73201 can also be used as quick access scratch pad registers for general purpose computing.

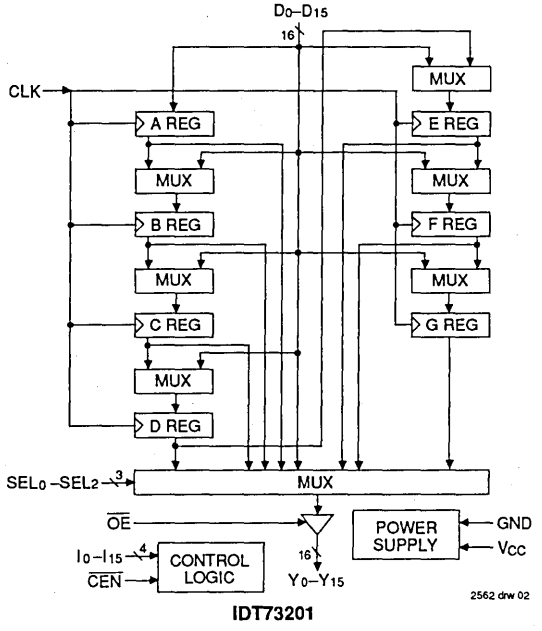
The two pipeline registers are packaged in 48-pin plastic and ceramic DIPs for through–hole designs as well as 52-pin PLCC and LCC for surface mount designs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

5

FUNCTIONAL BLOCK DIAGRAMS



IDT73200



IDT73201

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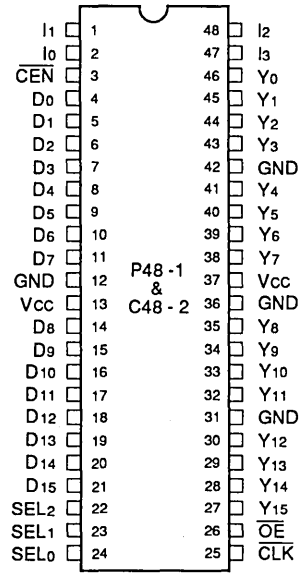
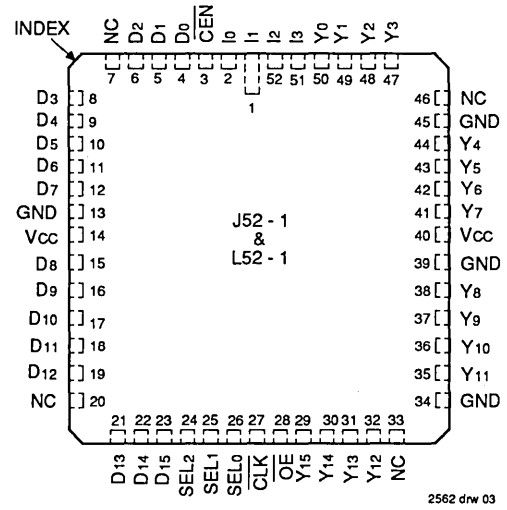
PIN CONFIGURATIONS



DIP
TOP VIEW



PLCC/LCC
TOP VIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
$D_0 - D_{15}$	I	Sixteen-bit data input port.
$Y_0 - Y_{15}$	O	Sixteen-bit data output port.
$I_0 - I_3$	I	Four control pins to select the register operation performed.
$SEL_0 - SEL_2$	I	Three control pins to select the register appearing at the output.
CLK	I	Clock input.
$\overline{CEN}$	I	Clock enable control pin. When this pin is low, the instruction I_0–I_3 is performed on the registers. When high, no register operation occurs.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port Y is in a high impedance state. When low, the output port Y is active.
V_{CC}		Power supply pin, 5V.
GND		Ground pins, 0V.

2562 tbl 01

IDT73200 OUTPUT SELECTION

SEL_2	SEL_1	SEL_0	Y Output
0	0	0	$A \rightarrow Y_0 - Y_{15}$
0	0	1	$B \rightarrow Y_0 - Y_{15}$
0	1	0	$C \rightarrow Y_0 - Y_{15}$
0	1	1	$D \rightarrow Y_0 - Y_{15}$
1	0	0	$E \rightarrow Y_0 - Y_{15}$
1	0	1	$F \rightarrow Y_0 - Y_{15}$
1	1	0	$G \rightarrow Y_0 - Y_{15}$
1	1	1	$H \rightarrow Y_0 - Y_{15}$

2562 tbl 02

IDT73201 OUTPUT SELECTION

SEL_2	SEL_1	SEL_0	Y Output
0	0	0	$A \rightarrow Y_0 - Y_{15}$
0	0	1	$B \rightarrow Y_0 - Y_{15}$
0	1	0	$C \rightarrow Y_0 - Y_{15}$
0	1	1	$D \rightarrow Y_0 - Y_{15}$
1	0	0	$E \rightarrow Y_0 - Y_{15}$
1	0	1	$F \rightarrow Y_0 - Y_{15}$
1	1	0	$G \rightarrow Y_0 - Y_{15}$
1	1	1	$D_0 - D_{15} \rightarrow Y_0 - Y_{15}$

2562 tbl 03

IDT73200 INSTRUCTION TABLE

I_3	I_2	I_1	I_0	Mnemonic	Function	Pipeline Levels
0	0	0	0	LDA	$D_0 - D_{15} \rightarrow A$	1
0	0	0	1	LDB	$D_0 - D_{15} \rightarrow B$	1
0	0	1	0	LDC	$D_0 - D_{15} \rightarrow C$	1
0	0	1	1	LDD	$D_0 - D_{15} \rightarrow D$	1
0	1	0	0	LDE	$D_0 - D_{15} \rightarrow E$	1
0	1	0	1	LDF	$D_0 - D_{15} \rightarrow F$	1
0	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
0	1	1	1	LDH	$D_0 - D_{15} \rightarrow H$	1
1	0	0	0	LSHAH	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow F \rightarrow G \rightarrow H$	8
1	0	0	1	LSHAD	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D$	4
1	0	1	0	LSHEH	$D_0 - D_{15} \rightarrow E \rightarrow F \rightarrow G \rightarrow H$	4
1	0	1	1	LSHAB	$D_0 - D_{15} \rightarrow A \rightarrow B$	2
1	1	0	0	LSHCD	$D_0 - D_{15} \rightarrow C \rightarrow D$	2
1	1	0	1	LSHEF	$D_0 - D_{15} \rightarrow E \rightarrow F$	2
1	1	1	0	LSHGH	$D_0 - D_{15} \rightarrow G \rightarrow H$	2
1	1	1	1	HOLD	Hold All Registers	—

2562 tbl 04

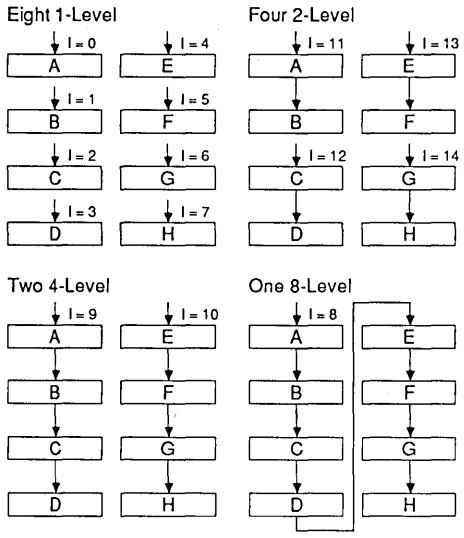
IDT73201 INSTRUCTION TABLE

I_3	I_2	I_1	I_0	Mnemonic	Function	Pipeline Levels
0	0	0	0	LDA	$D_0 - D_{15} \rightarrow A$	1
0	0	0	1	LDB	$D_0 - D_{15} \rightarrow B$	1
0	0	1	0	LDC	$D_0 - D_{15} \rightarrow C$	1
0	0	1	1	LDD	$D_0 - D_{15} \rightarrow D$	1
0	1	0	0	LDE	$D_0 - D_{15} \rightarrow E$	1
0	1	0	1	LDF	$D_0 - D_{15} \rightarrow F$	1
0	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
0	1	1	1	HOLD	Hold All Registers	—
1	0	0	0	LSHAG	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow F \rightarrow G$	7
1	0	0	1	LSHAD	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D$	4
1	0	1	0	LSHEG	$D_0 - D_{15} \rightarrow E \rightarrow F \rightarrow G$	3
1	0	1	1	LSHAB	$D_0 - D_{15} \rightarrow A \rightarrow B$	2
1	1	0	0	LSHCD	$D_0 - D_{15} \rightarrow C \rightarrow D$	2
1	1	0	1	LSHEF	$D_0 - D_{15} \rightarrow E \rightarrow F$	2
1	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
1	1	1	1	HOLD	Hold All Registers	—

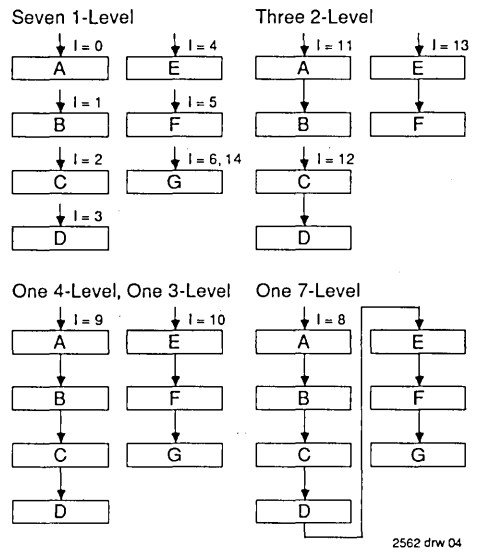
2562 tbl 05

5

IDT73200 PIPELINE CONFIGURATIONS



IDT73201 PIPELINE CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VCC	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
VTERM	Terminal Voltage with Respect to GND	–0.5 to VCC + 0.5	–0.5 to VCC + 0.5	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
IOUT	DC Output Current	50	50	mA

2562 tbl 06

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	12	pF

2562 tbl 07

NOTE:

1. This parameter is sampled at initial characterization and is not 100% tested.

TEST CIRCUIT

Test	Switch
tPLZ	Closed
tPZL	Closed
Open Drain	Closed
All Other Tests	Open

2562 tbl 10

DEFINITIONS:

CL = Load capacitance includes jig and probe capacitance.
RT = Termination should be equal to ZOUT of the pulse generator. (Typically 50Ω)
VIN = 0V to 3.0V
INPUT: tr = tf = 2.5ns (10% to 90%) unless otherwise specified

DC ELECTRICAL CHARACTERISTICS

Commercial: 0°C to +70°C, 5V ± 5%; Military: –55°C to +125°C, 5V ± 10%

Symbol	Parameter	Test Condition		Min.	Max	Unit
V_{IH}	High-Level Input Voltage	—		2.0	—	V
V_{IL}	Low-Level Input Voltage	—		—	0.8	V
I_{IH}	High Level Input Current	V_{CC} = Max.	V_I = V_{CC}	—	10	µA
I_{IL}	Low-Level Input Current	V_{CC} = Max.	V_I = GND	—	–10	µA
V_{OH}	High-Level Output Voltage	V_{CC} = Min., I_{OH} = -8mA(COM'L.), –6mA(MIL.)		2.4	—	V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min., I_{OL} = 16mA(COM'L.), 12mA(MIL.)		—	0.4	V
V_{IK}	Input Clamp Voltage	I_I = –18mA		—	–1.2	V
I_{OS}	Short Circuit Output Current[2]	V_{CC} = Max., V_O = GND V_I = V_{CC} or GND		–20	—	mA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_I = V_{CC}	—	20	µA
I_{OZL}	Low Impedance Output Current	V_{CC} = Max.	V_I = GND	—	–20	µA

NOTES:
1. For conditions shown as Min. or Max., use appropriate value based on temperature range.
2. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed 100 milliseconds.

2562 tbl 08

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{CC} = Max. V_I = V_{LC} or V_{HC}		—	2	10	mA
I_{CCQT}[3]	Quiescent Power Supply Current Inputs HIGH	V_{CC} = Max. V_I = 3.4V		—	15	45	mA
I_{CCD1}[4]	Dynamic Power Supply Current	V_{CC} = Max. Outputs Disabled, $\overline{OE}$ = HIGH f_{CP} = 10MHz, 50% Duty Cycle $V_I \leq V_{HC}$, $V_I \geq V_{LC}$	COM'L.	—	10	30	mA
			MIL.	—	10	40	
I_{CCD1}[4]	Dynamic Power Supply Current	V_{CC} = Max. Outputs Disabled, $\overline{OE}$ = HIGH f_{CP} = 40MHz, 50% Duty Cycle $V_I \leq V_{HC}$, $V_I \geq V_{LC}$	COM'L.	—	10	60	mA
			MIL.	—	10	80	

NOTES:
1. For conditions shown as Min. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. This parameter is not directly testable but is derived for use in the total power supply calculation.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CCQC} + (I_{CCQT} \times D_H \times N_T) + I_{CCD}$
   I_{CCQC} = Quiescent Current
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for each TTL Input High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Charge moved by an input transition pair (HLH or LHL)
   All currents are in milliamps and all frequencies are in megahertz.

2562 tbl 09

5

AC ELECTRICAL CHARACTERISTICS

Commerical: T_A = 0°C to +70°C, V_{CC} = 5V ±5%; Military: T_A = −55°C to +125°C, V_{CC} = 5V ±10%

Parameter	Commercial				Military				Unit
	73200L12 73201L12		73200L15 73201L15		73200L15 73201L15		73200L20 73201L20		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CLK to Y_0–Y_{15} Propagation Delay	—	12	—	15	—	15	—	20	ns
SEL_0–SEL_2 to Y_0–Y_{15} Propagation Delay	—	12	—	15	—	15	—	20	ns
D_0–D_{15} to CLK Set-up Time	3	—	4	—	4	—	5	—	ns
D_0–D_{15} to CLK Hold Time	1	—	2	—	2	—	3	—	ns
I_0–I_3 to CLK Set-up Time	4	—	5	—	5	—	6	—	ns
I_0–I_3 to CLK Hold Time	2	—	2	—	2	—	3	—	ns
CEN to CLK Set-up Time	4	—	5	—	5	—	6	—	ns
CEN to CLK Hold Time	2	—	2	—	2	—	3	—	ns
$\overline{OE}$ Enable Time[1]	—	9	—	10	—	10	—	13	ns
$\overline{OE}$ Disable Time[1]	—	8	—	9	—	9	—	13	ns
CLK Pulse Width HIGH	5	—	5	—	5	—	6	—	ns
CLK Pulse Width LOW	5	—	5	—	5	—	6	—	ns
CLK Period	—	12	—	15	—	15	—	20	ns
Data In to Data Out Flowthrough[2]	—	12	—	15	—	-15	—	20	ns

NOTES:
1. Output Enable and Disable times measured to 500mV change of output voltage level.
2. 73201 only.

2562 tbl 11

AC TEST CONDITIONS

Input Pulse Levels	GND to 4.0V
Input Rise/Fall Times	4ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2562 tbl 12

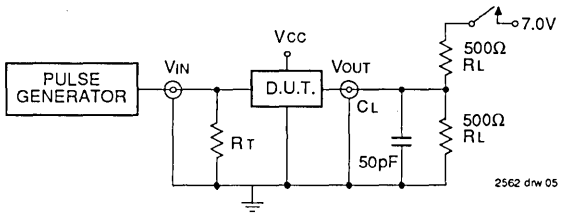


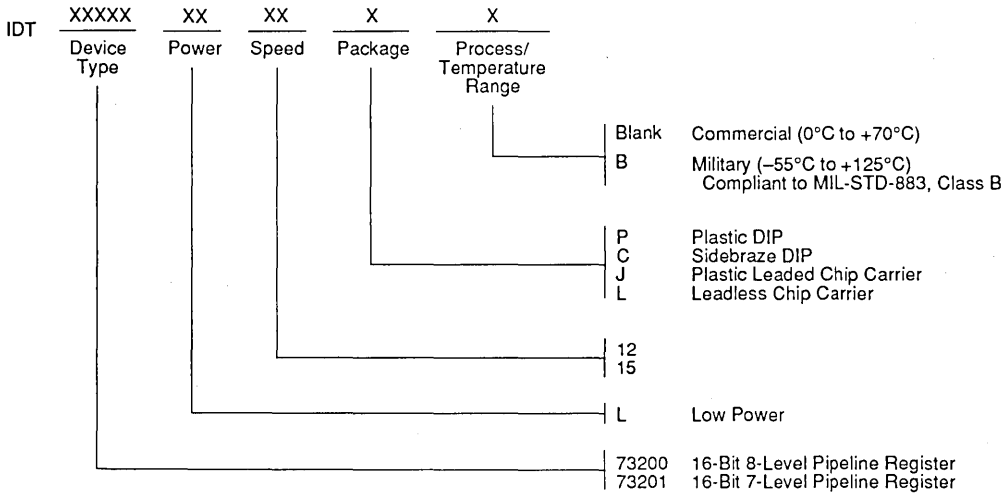
Figure 1. AC Output Test Circuit

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscilliate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

ORDERING INFORMATION



2562 drw 06

5

Integrated Device Technology, Inc.

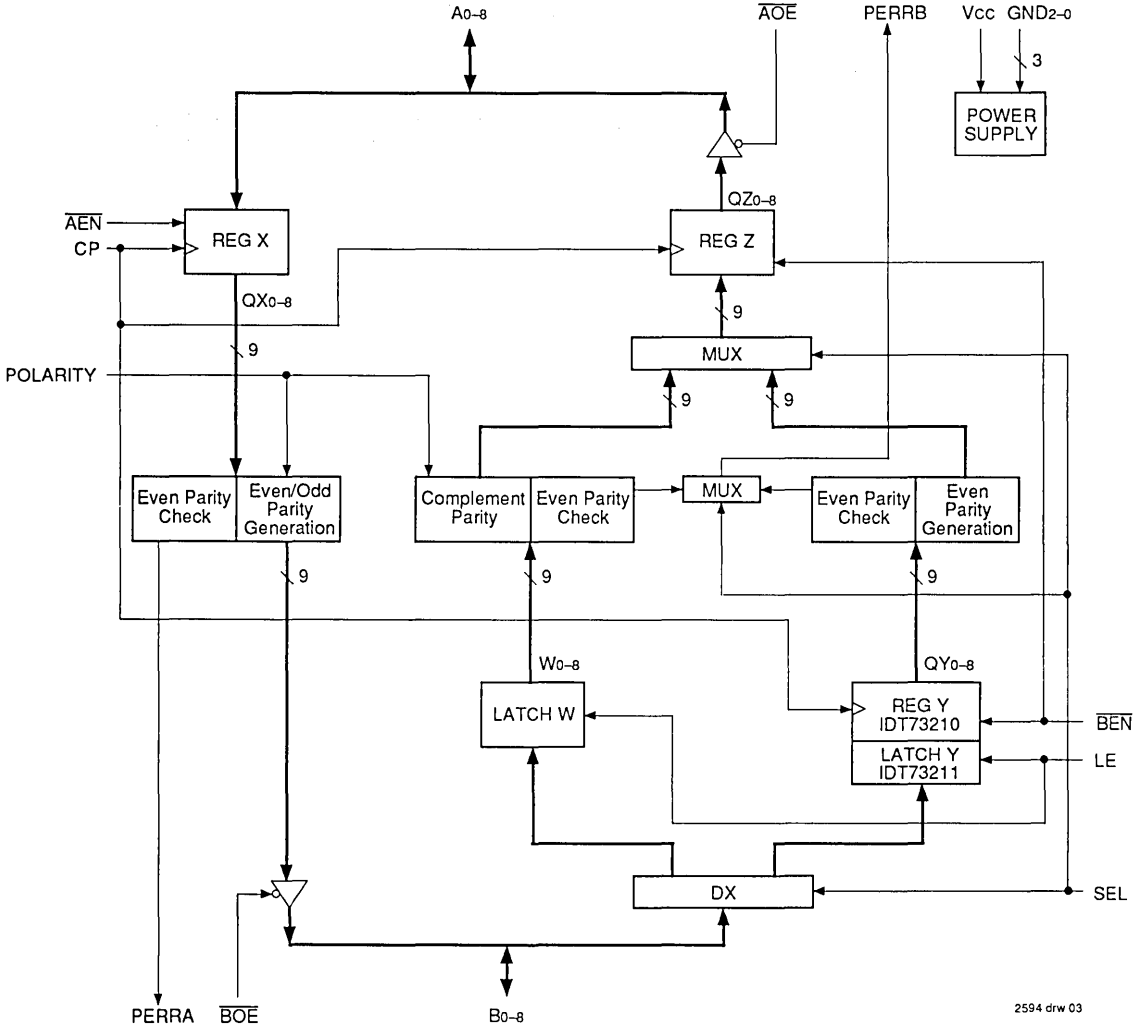
FAST CMOS OCTAL REGISTER TRANSCEIVER WITH PARITY

PRELIMINARY
IDT73210
IDT73211

FEATURES

- Two bidirectional interfacing ports
- Single-level pipeline register for one port and one-level (73211) or two-level (73210) pipeline register for the other port
- 8-bit wide interface ports plus parity bit
- Even parity checking in both directions
- Even/odd parity generation from Port A to Port B
- Even parity generation from Port B to Port A
- Parity polarity control
- High output drive capability: 64/48mA (commercial/ military)
- Available in 32-pin, 300 mil plastic DIP and sidebraze DIP, surface mount 32-pin SOJ and LCC packages
- High-speed, low-power, CEMOS™ process technology
- Military product compliant to MIL-STD-883, Class B

FUNCTIONAL BLOCK DIAGRAM



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APPLICATIONS

- Cache memory bus interface
- Read and write buffers for RISC microprocessor system
- Registered transceiver with parity

FUNCTIONAL DESCRIPTION

The IDT73210/1 Octal Register Transceivers are high-speed, low-power data interface with data integrity checking capability.

They are designed for high-performance systems requiring bidirectional data transfer between two buses and maintaining error checking via parity.

In any RISC or CISC microprocessor system, the IDT73210/1 can be used to interface cache memory with main memory. Data integrity is ensured through parity checking. Control features allow dynamic reconfiguration of check/generate and odd/even parity options.

DETAILED FUNCTIONAL DESCRIPTION

Port A to Port B Path (IDT73210 and IDT73211) is comprised of a register (X), an even/odd parity generator and an even parity checker. The input data is on the A_{0-8} lines. When $\overline{AEN}$ is low, A_{0-8} is latched into Register X on the low-to-high CP transition. Even parity of the latched data is checked. If PERRA goes high, a parity error has occurred. A new parity bit, B_8, is generated. The output data bus is B_{0-8} and is enabled when $\overline{BOE}$ is low.

Port B to Port A Path (IDT73210) is comprised of a latch (W), two registers (Y and Z), an even parity generator/checker and a parity bit latch complementor. The input data bus is on the B_{0-8} lines.

When SEL is high, the incoming data is latched into Latch W. When LE is high, Latch W is transparent; when LE is low, Latch W is closed. The parity bit, B_8, can be complemented by the POLARITY pin. If POLARITY is low, the parity sense remains the same. If POLARITY is high, the parity sense is complemented. Parity is not generated in this path. Even parity of latched data is checked. If PERRB goes high, a parity error has occurred. When $\overline{BEN}$ is low, W_{0-8} is latched into Register Z on the low-to-high CP transition. The previous contents are held in Register Z if $\overline{BEN}$ is high or if there is no low-to-high CP transition. The output data bus is A_{0-8} and is enabled when $\overline{AOE}$ is low. When SEL is high, there is only a one clock cycle latency.

When SEL is low, the incoming data is latched into Register Y on the low-to-high CP transition, when $\overline{BEN}$ is low. Even parity of the registered data is checked. If PERRB goes high, a parity error has occurred. Even parity (QY_8) is generated on the contents in Register Y. When $\overline{BEN}$ is low, the contents of register Y are transferred to Register Z on the low-to-high CP transition. When $\overline{BOE}$ is low, the content of Register Z is made available at output Port A. When SEL is low, there is a two clock cycle latency.

Port B to Port A Path (IDT73211) is comprised of a latch (W), two registers (Y and Z), an even parity generator/checker and a parity bit latch complementor. The input data bus is on the B_{0-8} lines.

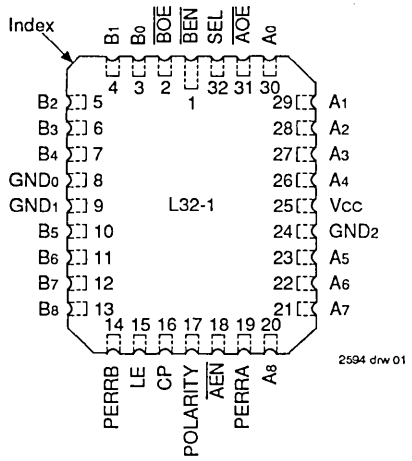
When SEL is high, the incoming data is latched into Latch W. When LE is high, Latch W is transparent; when LE is low, Latch W is closed. The parity bit, B_8, can be complemented by the POLARITY pin. If POLARITY is low, the parity sense remains the same. If POLARITY is high, the parity sense is complemented. Parity is not generated in this path. Even parity of latched data is checked. If PERRB goes high, a parity error has occurred. When $\overline{BEN}$ is low, W_{0-8} is latched into Register Z on the low-to-high CP transition. The previous contents are held in Register Z if $\overline{BEN}$ is high or if there is no low-to-high CP transition. The output data bus is A_{0-8} and is enabled when $\overline{AOE}$ is low. When SEL is high, there is only a one clock cycle latency.

When SEL is low, the incoming data is latched into Latch Y when LE is high. Latch Y is closed when LE is low. Even parity of latched data is checked. If PERRB goes high, a parity error has occurred. Even parity (QY_8) is generated on the contents in Latch Y. When $\overline{BEN}$ is low, the contents of Latch Y are transferred to Register Z on the low-to-high CP transition. When $\overline{BOE}$ is low, the content of Register Z is made available at output Port A. When SEL is low, there is a one clock cycle latency.

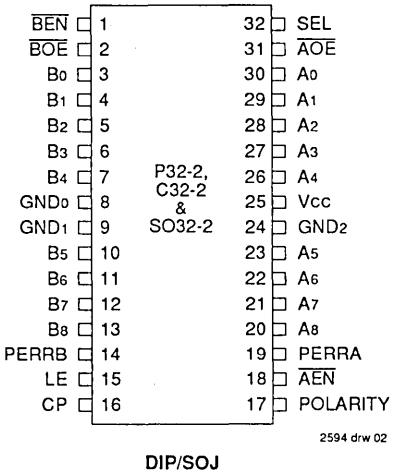
The power pins are Vcc and GND_{0-2}. GND_0 is internal quiet ground, GND_1 is Port B ground and GND_2 is Port A ground.

5

PIN CONFIGURATIONS[1]



LCC
TOP VIEW



DIP/SOJ
TOP VIEW

NOTE:
1. GND_0 is internal quiet ground
   GND_1 is B Port ground
   GND_2 is A Port ground

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_{0-8}	I/O	Data Port A.
$\overline{AEN}$	I	Clock enable (active low) for the register X.
$\overline{AOE}$	I	3-state output enable for Port A.
B_{0-8}	I/O	Data Port B.
$\overline{BEN}$	I	Clock enable (active low) for the registers Y and Z.
$\overline{BOE}$	I	3-state output enable for Port B.
LE	I	Latch enable input for Latch Y/Latch W of Port B. The Latch Y/Latch W is open when LE is high. Data is latched on the high-to-low transition of LE.
SEL	I	Input selection for Port B. SEL = 0 Register Y; SEL = 1 Latch Y
POLARITY	I	Polarity selection input. **Polarity** / **A to B Direction** / **B to A Direction** 0 / EVEN / Pass Parity 1 / ODD / Complement Parity
PERRA	O	Parity output error for Port A.
PERRB	O	Parity output error for Port B.
CP	I	Input clock.
Vcc		+5 volts.
GND_{0-2}		Ground.

2594 tbl 01

OPERATING MODES SUMMARY

IDT73210/1 A TO B DIRECTION

Input	Reg. X	PERRA	Output	
			(B_8)	B_{0-8}
A_{0-8}	$A_{0-8} \rightarrow QX_{0-8}$ ($\overline{CP}$ = Lo to Hi) ($\overline{AEN}$ = 0)	Result of even parity check	Even/odd parity bit B_8 = POLARITY XOR Even parity generate from QX_{0-7}	$QX_{0-8} \rightarrow B_{0-8}$ ($\overline{BOE}$ = 0)

2594 tbl 02

IDT73210/1 B TO A DIRECTION WHEN SEL = 1

Input	Latch W	PERRB	Reg. Z		Output	
			(QZ_8)	QZ_{0-8}	(A_8)	A_{0-8}
B_{0-8}	$B_{0-8} \rightarrow W_{0-8}$ (LE = 1)	Result of even parity check	Bit complemented by POLARITY (Even/odd parity translation)	$W_{0-8} \rightarrow QZ_{0-8}$ ($\overline{CP}$ = Lo to Hi) ($\overline{BEN}$ = 0)	A_8 = POLARITY XOR W_8	$QZ_{0-8} \rightarrow A_{0-8}$ ($\overline{AOE}$ = 0)

2594 tbl 03

IDT73210 B TO A DIRECTION WHEN SEL = 0

Input	Reg. Y	PERRB	Reg. Z		Output	
			(QZ_8)	QZ_{0-8}	(A_8)	A_{0-8}
B_{0-8}	$B_{0-8} \rightarrow QY_{0-8}$ ($\overline{CP}$ = Lo to Hi) ($\overline{BEN}$ = 0)	Result of even parity check	Even parity generated bit	$QY_{0-8} \rightarrow QZ_{0-8}$ ($\overline{CP}$ = Lo to Hi) ($\overline{BEN}$ = 0)	A_8 = Even parity generated from QY_{0-7}	$QZ_{0-8} \rightarrow A_{0-8}$ ($\overline{BOE}$ = 0)

2594 tbl 04

IDT73211 B TO A DIRECTION WHEN SEL = 0

Input	Latch Y	PERRB	Reg. Z		Output	
			(QZ_8)	QZ_{0-8}	(A_8)	A_{0-8}
B_{0-8}	$B_{0-8} \rightarrow QY_{0-8}$ (LE = 1)	Result of even parity check	Even parity generated bit	$QY_{0-8} \rightarrow QZ_{0-8}$ ($\overline{CP}$ = Lo to Hi) ($\overline{BEN}$ = 0)	A_8 = Even parity generated from QY_{0-7}	$QZ_{0-8} \rightarrow A_{0-8}$ ($\overline{BOE}$ = 0)

2594 tbl 05

5

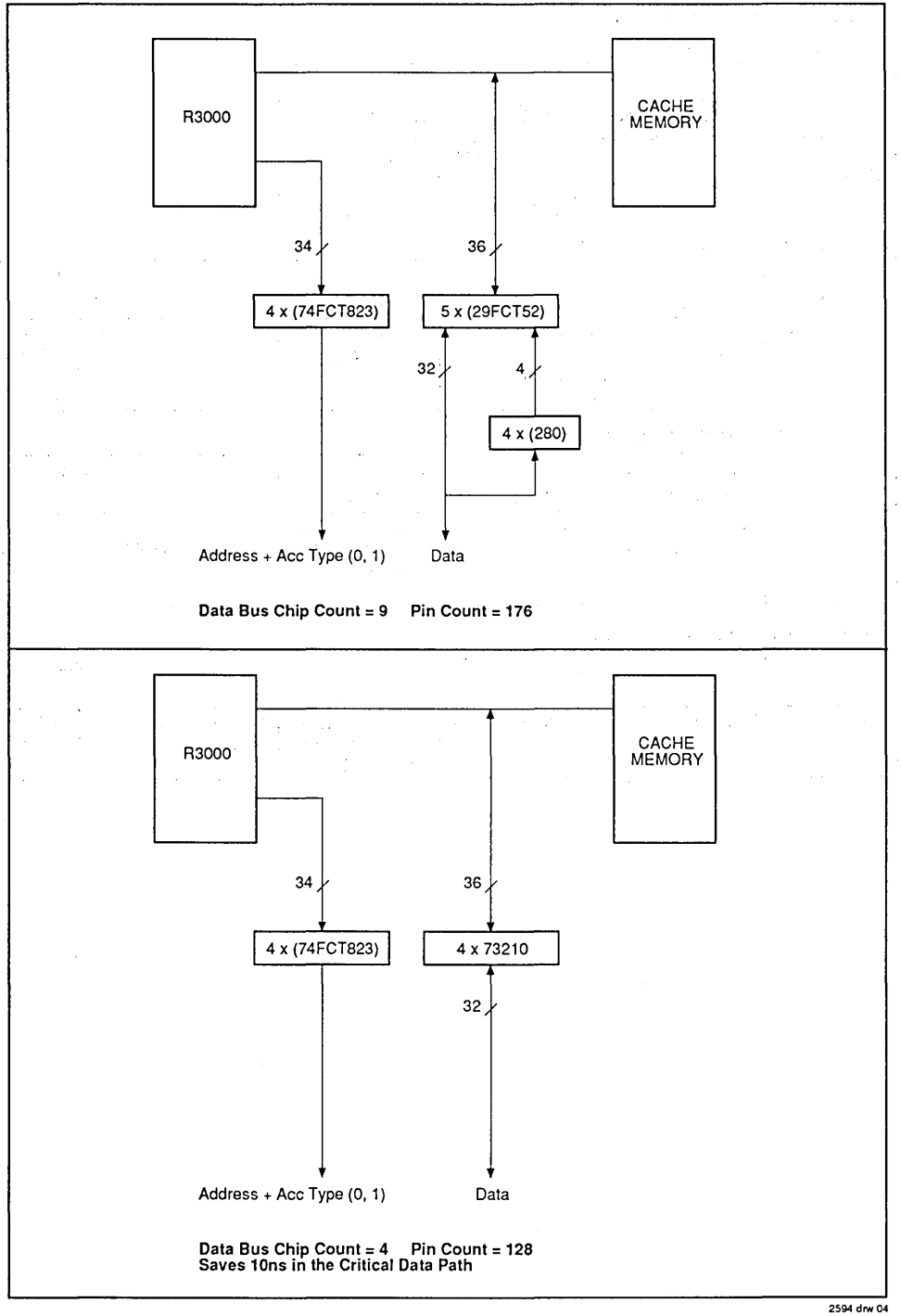


Figure 1. R3000 System with No Parity Support in Main Memory

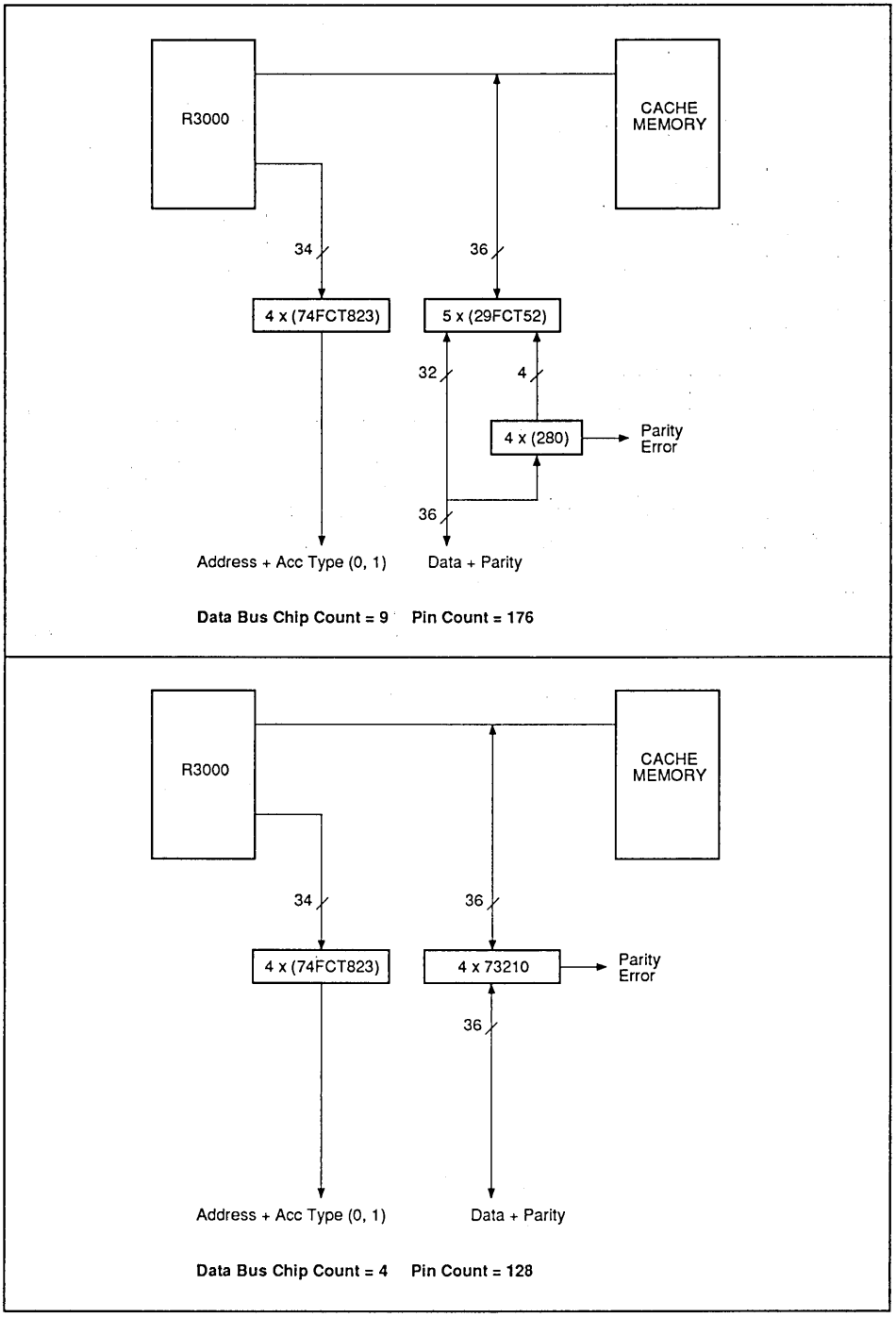


Figure 2. R3000 System with Parity Support in Main Memory

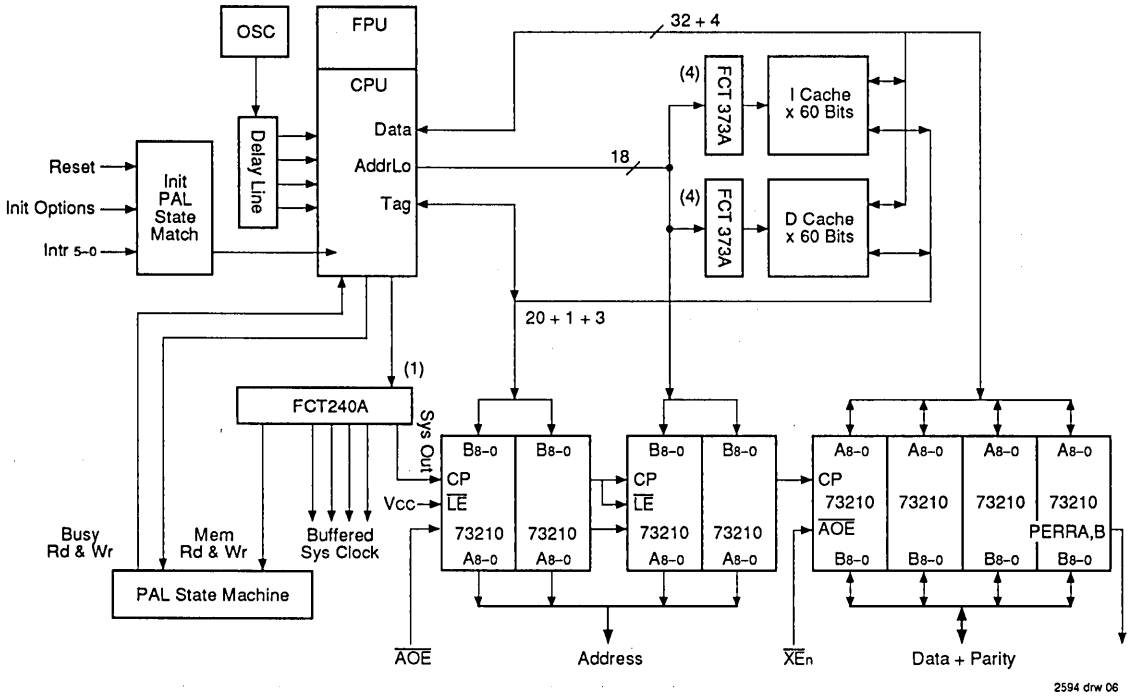


Figure 3. Read and Write Buffers Using Eight IDT73210/1

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to Ground	–0.5 to VCC + 0.5	–0.5 to VCC + 0.5	V
VCC	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.2	1.5	W
IOUT	Total Output Current	200	250	mA

NOTE: 2594 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	5	pF
COUT	Output Capacitance	VOUT = 0V	7	pF
CI/O	Input – Output Capacitance	VOUT = 0V	7	pF

NOTE: 2594 tbl 07

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:
Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%; Military: TA = –55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)			Min.	Typ.(2)	Max.	Unit
VIH	Input HIGH Level	Guaranteed Logic HIGH Level			2.0	—	—	V
VIL	Input LOW Level	Guaranteed Logic LOW Level			—	—	0.8	V
IIH	Input HIGH Current	VCC = Max.		Except I/O	—	—	10	µA
		VI = 2.7V		I/O pins	—	—	20	
IIL	Input LOW Current	VCC = Max.		Except I/O	—	—	-10	µA
		VI = 0.5V		I/O pins	—	—	-20	
VIK	Clamp Diode Voltage	VCC = Min., IN = –18mA			—	-0.7	-1.2	V
IOS	Short Circuit Current	VCC = Max.(3), VO = GND		PERRA, PERRB	-30	—	-150	mA
				A0-8, B0-8	-20	—	-75	
VOH	Output HIGH Voltage	VCC = Min.		IOH = –12mA MIL.	2.4	3.3	—	V
		VIN = VIH or VIL		IOH = –15mA COM'L.				
VOL	Output LOW Voltage	VCC = Min.	A0-8	IOL = 48mA MIL.	—	0.3	0.5	V
		VIN = VIH or VIL	B0-8	IOL = 64mA COM'L.				
		VCC = Min.	PERRA	IOL = 20mA MIL.				
		VIN = VIH or VIL	PERRB	IOL = 24mA COM'L.				
VH	Input Hysteresis for CP only	VCC = 5V			—	200	—	mV

NOTES: 2594 tbl 09

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient, not production tested.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed 100 millisecond.

5

POWER SUPPLY CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4[3]	COM'L.	—	3	10	mA
			MIL.	—	3	15	
I_{CCD1}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Disabled f_{CP} = 10MHz 50% Duty Cycle f_i = 5MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	6.0	15	mA
I_{CCD2}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Disabled f_{CP} = 40MHz 50% Duty Cycle f_i = 20MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	24	60	mA

2594 tbl 08

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. This parameter is not directly testable but is derived for use in the total power supply calculation.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CCQC} + I_{CCQT} D_H N_T + I_{CCD}$
   I_{CCQC} = Quiescent Current
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

T_A = 0°C to +70°C; V_{CC} = 5V ± 5%
C_L = 50pF; R_L = 500Ω

Parameter	Description	Min.	Typ.(1)	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Clock to A_{0-8} ($\overline{AOE}$ = Low) Clock to B_{0-8} ($\overline{BOE}$ = Low)	—	—	10.0	ns
t_{PHL}	Propagation Delay CP to PERRA, PERRB	—	—	8.5	ns
t_{PHL}	Propagation Delay POLARITY to B_{0-8}	—	—	7.0	ns
t_{PHL}	Propagation Delay B_{0-8} to PERRB LE = High	—	—	8.5	ns
t_S	Set-up Time A_{0-8}, B_{0-8}, POLARITY, SEL to CP	2.0	—	—	ns
t_H	Hold Time A_{0-8}, B_{0-8}, POLARITY, SEL to CP	1.5	—	—	ns
t_S	Set-up Time $\overline{AEN}$, $\overline{BEN}$ to CP Low-to-High	2.0	—	—	ns
t_H	Hold Time $\overline{AEN}$, $\overline{BEN}$ to CP Low-to-High	1.5	—	—	ns
t_S	Set-up Time B_{0-8} to LE	2.0	—	—	ns
t_H	Hold Time B_{0-8} to LE	1.5	—	—	ns
t_S	Set-up Time B_{0-8} to CP to Low-to-High; LE = High	3.0	—	—	ns
t_H	Hold Time B_{0-8} to CP to Low-to-High; LE = High	1.5	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	—	—	7.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	—	—	6.5	ns
t_{PWH}	Clock Pulse Width High	7.0	5.0	—	ns
t_{PWL}	Clock Pulse Width Low	7.0	5.0	—	ns

NOTE:
1. Typical values are at Vcc = 5.0V and +25°C ambient, not production tested.

2594 tbl 10

5

SWITCHING CHARACTERISTICS OVER MILITARY OPERATING RANGE

T_A = -55°C to +125°C; V_{CC} = 5V ± 10%
C_L = 50pF; R_L = 500Ω

Parameter	Description	Min.	Typ.[1]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Clock to A_{0-8} ($\overline{AOE}$ = Low) Clock to B_{0-8} ($\overline{BOE}$ = Low)	—	—	12.2	ns
t_{PHL}	Propagation Delay CP to PERRA, PERRB	—	—	10.6	ns
t_{PHL}	Propagation Delay POLARITY to B_{0-8}	—	—	7.0	ns
t_{PHL}	Propagation Delay B_{0-8} to PERRB LE = High	—	—	10.6	ns
t_S	Set-up Time A_{0-8}, B_{0-8}, POLARITY, SEL to CP	2.0	—	—	ns
t_H	Hold Time A_{0-8}, B_{0-8}, POLARITY, SEL to CP	1.5	—	—	ns
t_S	Set-up Time $\overline{AEN}$, $\overline{BEN}$ to CP Low-to-High	2.0	—	—	ns
t_H	Hold Time $\overline{AEN}$, $\overline{BEN}$ to CP Low-to-High	1.5	—	—	ns
t_S	Set-up Time B_{0-8} to LE	2.0	—	—	ns
t_H	Hold Time B_{0-8} to LE	1.5	—	—	ns
t_S	Set-up Time B_{0-8} to CP to Low-to-High; LE = High	3.0	—	—	ns
t_H	Hold Time B_{0-8} to CP to Low-to-High; LE = High	1.5	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	—	—	7.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	—	—	6.5	ns
t_{PWH}	Clock Pulse Width High	8	6	—	ns
t_{PWL}	Clock Pulse Width Low	8	6	—	ns

NOTE:
1. Typical values are at V_{CC} = 5.0V and +25°C ambient.

2594 tbl 11

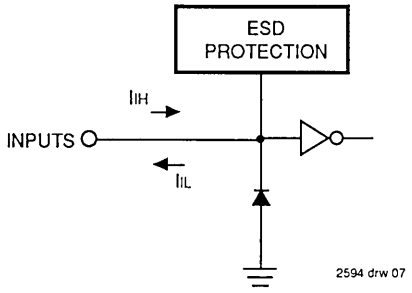


Figure 4. Input Interface Circuit

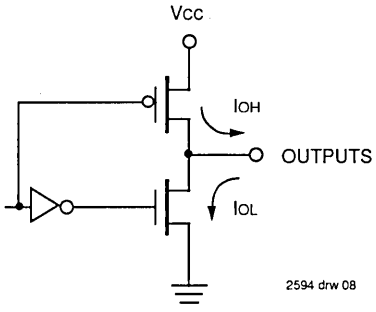
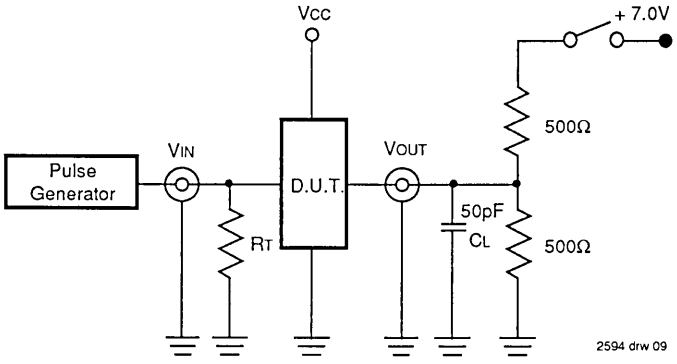


Figure 5. Output Interface Circuit



DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance
RL = Termination resistance: should be equal to ZOUT of the Pulse Generator

Figure 6. AC Test Load Circuit

AC TEST CONDITIONS

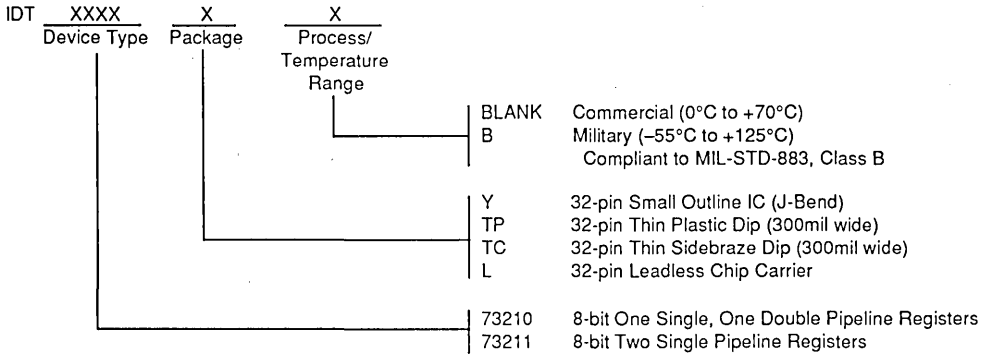
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 6

2594 tbl 12

Test	Switch
Open Drain Disable Low Enable Low	Closed
All other Tests	Open

2594 tbl 13

ORDERING INFORMATION



2594 drw 10

Integrated Device Technology, Inc.

16-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT39C60
IDT39C60–1
IDT39C60A
IDT39C60B

FEATURES

- Low-power CEMOS™
  - — Military: 100mA (max.)
  - — Commercial: 85mA (max.)
- Fast
  - — Data in to Error Detect
    IDT39C60B: 16ns (max.), IDT39C60A: 20ns (max.)
    IDT39C60–1: 25ns (max.), IDT39C60: 32ns (max.)
  - — Data in to Corrected Data out
    IDT39C60B: 25ns (max.), IDT39C60A: 30ns (max.)
    IDT39C60–1: 52ns (max.), IDT39C60: 65ns (max.)
- Improves system memory reliability
  - — Corrects all single-bit errors, detects all double and some triple-bit errors
- Cascadable
  - — Data words up to 64 bits
- Built-in diagnostics
  - — Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - — Fast byte writes possible with separate byte enables
- Available in 48-pin DIP, 52-pin PLCC and LCC
- Pin-compatible to all versions of the AMD2960
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88613 available for this function

DESCRIPTIONS

The IDT39C60 family are high-speed, low-power, 16-bit Error Detection and Correction Units which generate check-bits on a 16-bit data field according to a modified Hamming Code and correct the data word when checkbits are supplied. When performing a read operation from memory, the IDT39C60s will correct 100% of all single bit errors, will detect all double bit errors and some triple bit errors.

The IDT39C60s are easily cascadable from 16 bits up to 64 bits. Sixteen-bit systems use 6 check bits, 32-bit systems use 7 check bits and 64-bit systems use 8 check bits. For all three configurations, the error syndrome is made available.

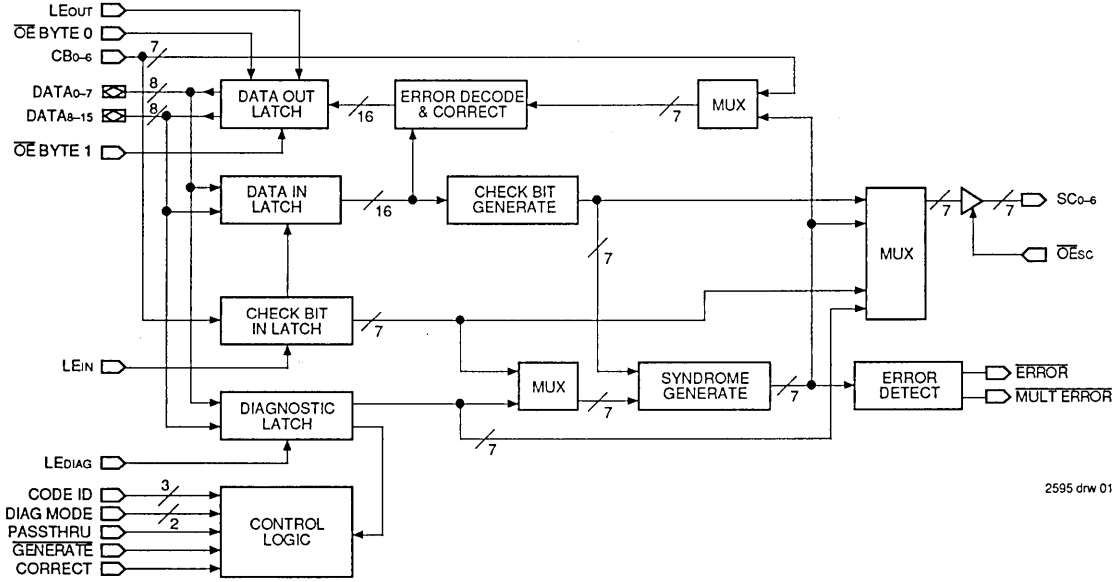
All parts incorporate 2 built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

The IDT39C60s are pin-compatible, performance-enhanced functional replacements for all versions of the 2960. They are fabricated using CEMOS, a CMOS technology designed for high-performance and high-reliability. The devices are packaged in either 48-pin DIPs and 52-pin PLCC and LCCs.

Military grade product is manufactured in compliance to the latest revision of MIL-STD-883, Class B.

5

FUNCTIONAL BLOCK DIAGRAM



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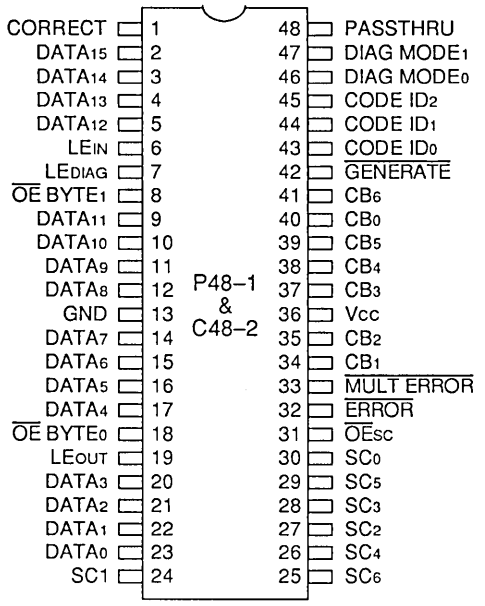
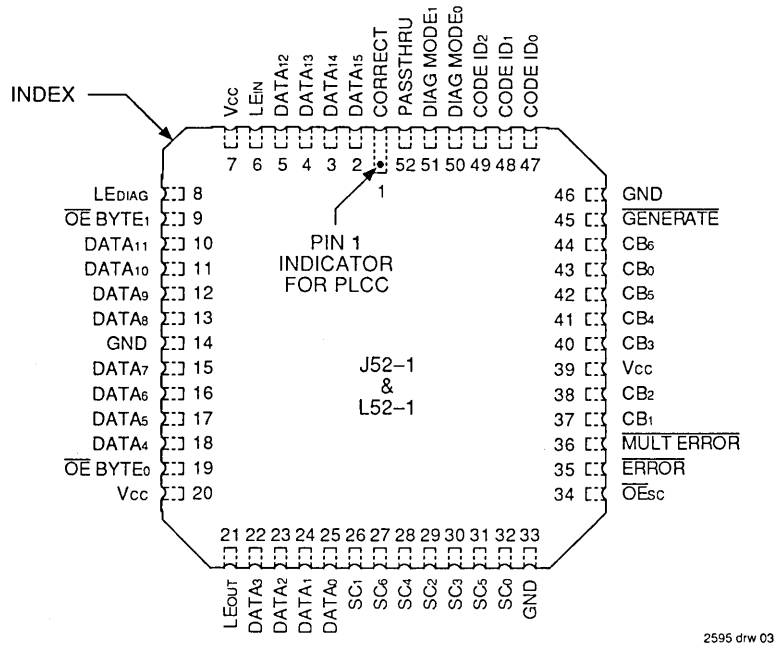
PIN CONFIGURATION



2595 drw 02

DIP
TOP VIEW
(600 mil x 100 mil Centers)



2595 drw 03

PLCC/LCC
TOP VIEW
(750 mil x 750 mil Centers)

PIN DESCRIPTIONS

Pin Name	I/O	Description
$DATA_{0-15}$	I/O	16 bidirectional data lines provide input to the Data Input Latch and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.
CB_{0-6}	I	Seven check bit input lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32- and 64-bit configurations.
LE_{IN}	I	Latch Enable — Data Input Latch. Controls latching of the input data. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.
$\overline{GENERATE}$	I	Generate Check Bits input. When this input is LOW, the EDC is in the Check Bit Generate mode. When HIGH, the EDC is in the Detect mode or Correct mode. In the Generate mode, the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. In the Detect or Correct modes the EDC detects single and multiple errors and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct mode, single-bit errors are also automatically corrected — corrected data is placed at the input of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates, in a coded form, the number of errors and the bit-in-error.
SC_{0-6}	O	Syndrome/Check Bit outputs hold the check/partial check bits when the EDC is in Generate mode and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct modes. These are 3-state outputs.
$\overline{OE}_{SC}$	I	Output Enable — Syndrome/Check Bits. When LOW, the 3-state output lines SC_{0-6} are enabled. When HIGH, the SC outputs are in the high impedance state.
$\overline{ERROR}$	O	Error Detected output. When the EDC is in Detect or Correct mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate mode, $\overline{ERROR}$ is forced HIGH. (In a 64-bit configuration, $\overline{ERROR}$ must be implemented externally.)
$\overline{MULT\ ERROR}$	O	Multiple Errors Detected output. When the EDC is in Detect or Correct mode this output, if LOW, indicates that there are two or more bit errors that have been detected. If HIGH, this indicates that either one or no errors have been detected. In Generate mode, $\overline{MULT\ ERROR}$ is forced HIGH. (In a 64-bit configuration, $\overline{MULT\ ERROR}$ must be implemented externally.)
CORRECT	I	Correct input. When HIGH, this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.
LE_{OUT}	I	Latch Enable — Data Output Latch. Controls the latching of the Data Output Latch. When LOW, the Data Output Latch is latched to its previous state. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are disabled with its contents unchanged if the EDC is in Generate mode.
$\overline{OE}\ BYTE_0$ $\overline{OE}\ BYTE_1$	I	Output Enable — Bytes 0 and 1, Data Output Latch controls the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW, these lines enable the Data Output Latch and, when HIGH, these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output at a time.
PASSTHRU	I	PASSTHRU input, when HIGH, forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC_{0-6}) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.
DIAG $MODE_{0-1}$	I	Diagnostic Mode Select controls the initialization and diagnostic operation of the EDC.
CODE ID_{0-2}	I	Code Identification inputs identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32, and 64 bits and their respective modified Hamming Codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID_2, ID_1, ID_0) is also used to instruct the EDC that the signals CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASSTHRU are to be taken from the diagnostic latch rather than the control lines.
LE_{DIAG}	I	Latch Enable — Diagnostic Latch. The Diagnostic Latch follows the 16-bit data on the input lines when HIGH. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASSTHRU.

2595 tbl 01

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PRODUCT DESCRIPTION

The IDT39C60 EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics. As shown in the Functional Block Diagram, the device consists of the following:

- — Data Input Latch
- — Data Output Latch
- — Diagnostic Latch
- — Check Bit Input Latch
- — Check Bit Generation Logic
- — Syndrome Generation Logic
- — Error Detection Logic
- — Error Correction Logic
- — Control Logic

DATA INPUT/OUTPUT/DIAGNOSTIC LATCHES

The LE_{IN}, Latch Enable input, controls the Data Input which can load 16 bits of data from the bidirectional DATA lines. The input data is used for either check bit generation or error detection/correction.

The 16 bits of data from the DATA lines can be loaded into the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in the other byte. The Diagnostic Latch is used when in Internal Control mode or in one of the Diagnostics modes.

The Data Output Latch is split into two bytes and enabled onto the DATA lines through separate byte control lines. The Data Output Latch stores the result of an error correction operation or is loaded directly from the Data Input Latch under control of the Latch Enable Out (LE_{OUT}). The PASSTHRU control input determines which data is loaded.

CHECK BIT GENERATION LOGIC

This block of combinational logic generates 7 check bits using a modified Hamming Code from the 16 bits of data input from the Data Input Latch.

SYNDROME GENERATION LOGIC

This logic compares the check bits generated through the Check Bit Generator with either the check bits in the Check Bit Input Latch or 7 bits assigned in the Diagnostic Latch.

Syndrome bits are produced by an exclusive-OR of the two sets of bits. A match indicates no errors. If errors occur, the syndrome bits can be decoded to indicate the bit in error, whether 2 errors were detected or 3 or more errors.

ERROR DETECTION/CORRECTION LOGIC

The syndrome bits generated by the Syndrome Logic are decoded and used to control the $\overline{\text{ERROR}}$ and $\overline{\text{MULTERROR}}$ outputs. If one or more errors are detected, $\overline{\text{ERROR}}$ goes low. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ go low. Both outputs remain high when there are no errors detected.

For single bit errors, the correction logic will complement (correct) the bit in error, which can then be loaded into the Data Out Latches under the LE_{OUT} control. If check bit errors need to be corrected, then the device must be operated in the Generate mode.

CONTROL LOGIC

The control logic determines the specific mode of operation, usually from external control signals. However, the Internal Control mode allows these signals to be provided from the Diagnostic Latch.

DETAILED PRODUCT DESCRIPTION

The IDT39C60 EDC unit contains the logic necessary to generate check bits on a 16-bit data input according to a modified Hamming Code. The EDC can compare internally generated check bits against those read with the 16-bit data to allow correction of any single bit data error and detection of all double and some triple bit errors. The IDT39C60 can be used for 16-bit data words (6 check bits), 32-bit data words (7 check bits) or 64-bit data words (8 check bits).

CODE AND BYTE SELECTION

The 3 code identification pins, ID_{0-2}, are used to determine the data word size from 16, 32 or 64 bits and the byte position of each 16-bit IDT39C60 EDC device.

Code 16/22 refers to a 16-bit data field with 6 check bits.
Code 32/39 refers to a 32-bit data field with 7 check bits.
Code 64/72 refers to a 64-bit data field with 8 check bits.

The ID_{0-2} of 001 is used to place the device in the Internal Control mode as described later in this section.

Table 1 defines all possible identification codes.

CHECK AND SYNDROME BITS

The IDT39C60 provides either check bits or syndrome bits on the three-state output pins, SC_{0-6}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an Exclusive-OR of the check bits generated from read data with the read check bits stored with the data. Syndrome bits can be decoded to determine the single bit-in-error or that a double error was detected. Some triple bit errors are also detected. The check bits are labeled:

C_0, C_1, C_2, C_3, C_4	for the 8-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5$	for the 16-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5, C_6$	for the 32-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$	for the 64-bit configuration

Syndrome bits are similarly labeled S_0 through S_7.

CONTROL MODE SELECTION

Tables 2 and 3 describe the 9 operating modes of the IDT39C60. The Diagnostic mode pins, DIAG $MODE_{0-1}$, define 4 basic areas of operation, with $\overline{GENERATE}$, CORRECT and PASSTHRU, further dividing operation into 8 functions with the ID_{0-2} defining the ninth mode as the Internal mode.

Generate mode is used to display the check bits on the outputs SC_{0-6}. The Diagnostic Generate mode displays check bits as stored in the Diagnostic Latch.

Detect mode provides an indication of errors or multiple errors on the outputs $\overline{ERROR}$ and $\overline{MULTERROR}$. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC_{0-6}. For the Diagnostic Detect mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct mode is similar to the Detect mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latch. Again, the Diagnostic Correct mode will correct single bit errors as determined by syndrome bits generated from the Data Input and contents of the Diagnostic Latch.

The Initialize mode provides check bits for all zero bit data. Data In Latch is set and latched to a logic zero and made available as input to the Data Out Latch.

The Internal mode disables the external control pins DIAG $MODE_{0-1}$, CORRECT, PASSTHRU and CODE ID to be defined by the Diagnostic Latch. When in the internal control mode, the data loaded into the diagnostic latch should have the CODE ID different from 001 as this would represent an invalid operation.

CODE ID_2	CODE ID_1	CODE ID_0	Hamming Code and Slice Selected
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Byte 0 and 1
0	1	1	Code 32/39, Byte 2 and 3
1	0	0	Code 64/72, Byte 0 and 1
1	0	1	Code 64/72, Byte 2 and 3
1	1	0	Code 64/72, Byte 4 and 5
1	1	1	Code 64/72, Byte 6 and 7

2595 tbl 02

Table 1. Hamming Code and Slice Identification

DIAG $MODE_1$	DIAG $MODE_2$	Diagnostic Mode Selected
0	0	**Non-diagnostic mode.** The EDC functions normally in all modes.
0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate mode. The EDC functions normally in the Detect or Correct modes.
1	0	**Diagnostic Detect/Correct.** In the Detect or Correct mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate mode.
1	1	**Initialize.** The outputs of the Data Input Latch are forced to zeroes and the check bits generated correspond to the all zero data. The latch is not reset, a functional difference from the Am2960.

2595 tbl 03

Table 2. Diagnostic Mode Control

5

Operating Mode	DM_1	DM_0	$\overline{GENERATE}$	CORRECT	PASS-THRU	$DATA_{OUT}$ Latch (LE_{OUT} = High)	SC_{0-6} ($\overline{OE}_{SC}$ = Low)	$\overline{ERROR}$ $\overline{MULT\ ERROR}$
Generate	0	0	0	X	0	—	Check Bits Generated from $DATA_{IN}$ Latch	High
	1	0						
Detect	0	0	1	0	0	$DATA_{IN}$ Latch	Syndrome Bits $DATA_{IN}$/ Check Bit Latch	Error Dep[1]
	0	1						
Correct	0	0	1	1	0	$DATA_{IN}$ Latch with Single Bit Correction	Syndrome Bits $DATA_{IN}$/ Check Bit Latch	Error Dep
	0	1						
PASSTHRU	0	0	X	X	1	$DATA_{IN}$ Latch	Check Bit Latch	High
	0	1						
	1	0						
Diagnostic Generate	0	1	0	X	0	—	Check Bits from Diagnostic Latch	High
Diagnostic Detect	1	0	1	0	0	$DATA_{IN}$ Latch	Syndrome Bits $DATA_{IN}$/ Diagnostic Latch	Error Dep
Diagnostic Correct	1	0	1	1	0	$DATA_{IN}$ Latch with Single Bit Correction	Syndrome Bits $DATA_{IN}$/ Diagnostic Latch	Error Dep
Initialization Mode	1	1	X	X	X	$DATA_{IN}$ Latch Set to 0000	Check Bits Generated from $DATA_{IN}$ Latch (0000)	—
Internal Mode	ID_{0-2} = 001 (Control Signals ID_{0-2}, $DIAG\ MODE_{0-1}$, CORRECT and PASSTHRU are taken from the Diagnostic Latch)							

NOTE: 2595 tbl 04

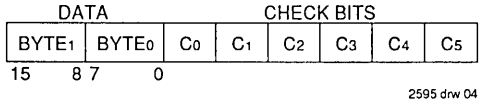
1. ERROR DEP (Error Dependent): $\overline{ERROR}$ will be low for single or multiple errors, with $\overline{MULT\ ERROR}$ low for double or multiple errors. Both signals are high for no errors.

Table 3. IDT39C60 Operating Modes

16-BIT DATA WORD CONFIGURATION

Figure 1 indicates the 22-bit data format for two bytes of data and 6 check bits.

A single IDT39C60 EDC unit, connected as shown in Figure 2, provides all the logic needed for single bit error correction and double bit error detection of a 16-bit data field. The identification code 16/22 indicates 6 check bits are required. The CB_6 pin is, therefore, a "Don't Care" and ID_2, ID_1, ID_0 = 000.



Uses Modified Hamming Code 16/22
16 Data Bits with 6 Check Bits

Figure 1. 16-Bit Data Format

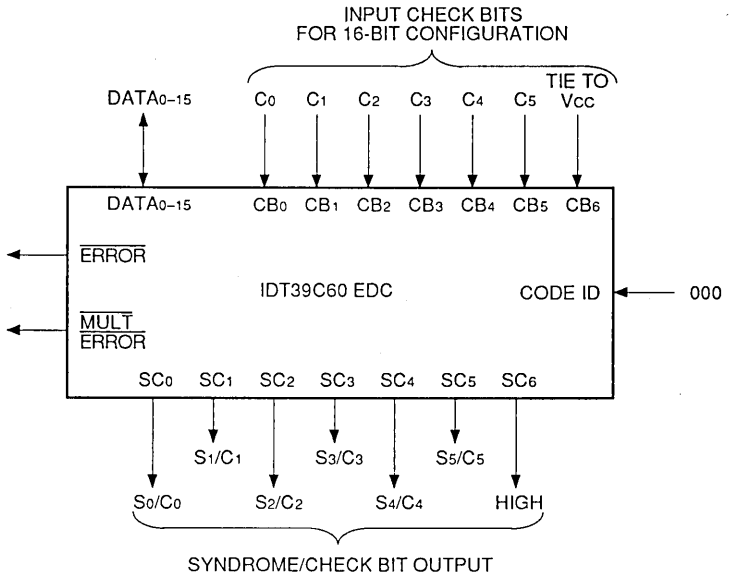


Figure 2. 16-Bit Configuration

Table 3 describes the operating modes available. The output pin SC_6, is forced high for either syndrome or check bits since only 6 check bits are used for the 16/22 code.

Table 4 indicates the data bits participating in the check bit generation. For example, check bit C_0 is the Exclusive-OR function of the 8 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate Mode.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 5 indicates the decoding of the six syndrome bits to indicate the bit-in-error for a single bit error, or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 6 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-5} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Generated Check Bits	Participating Data Bits[1]															
	Parity	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X

NOTE:
1. The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

2595 tbl 05

Table 4. 16-Bit Modified Hamming Code — Check Bit Encode Chart

					Hex	0	1	2	3
	Syndrome Bits				S_5	0	0	1	1
					S_4	0	1	0	1
Hex	S_3	S_2	S_1	S_0					
0	0	0	0	0		*	C4	C5	T
1	0	0	0	1		C0	T	T	14
2	0	0	1	0		C1	T	T	M
3	0	0	1	1		T	2	8	T
4	0	1	0	0		C2	T	T	15
5	0	1	0	1		T	3	10	T
6	0	1	1	0		T	4	9	T
7	0	1	1	1		M	T	T	M
8	1	0	0	0		C3	T	T	M
9	1	0	0	1		T	5	11	T
A	1	0	1	0		T	6	12	T
B	1	0	1	1		1	T	T	M
C	1	1	0	0		T	7	13	T
D	1	1	0	1		M	T	T	M
E	1	1	1	0		0	T	T	M
F	1	1	1	1		T	M	M	T

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

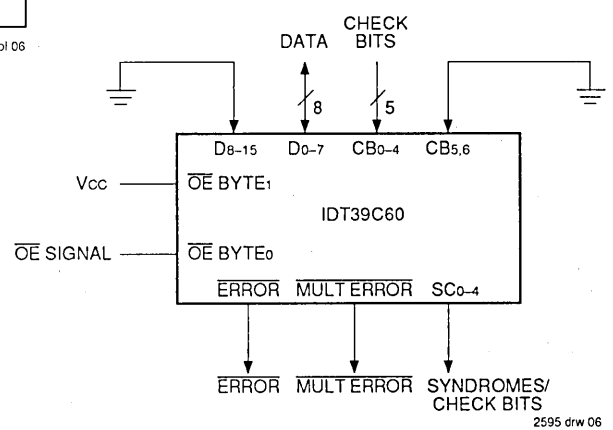
2595 tbl 06

Table 5. Syndrome Decode to Bit-In-Error (16-Bit Configuration)

Data Bit	Internal Function
0	Diagnostic Check Bit0
1	Diagnostic Check Bit1
2	Diagnostic Check Bit2
3	Diagnostic Check Bit3
4	Diagnostic Check Bit4
5	Diagnostic Check Bit5
6, 7	Don't Care
8	CODE ID0
9	CODE ID1
10	CODE ID2
11	DIAG MODE0
12	DIAG MODE1
13	CORRECT
14	PASSTHRU
15	Don't Care

2595 tbl 07

Table 6. Diagnostic Latch Loading — 16-Bit Format



2595 drw 06

Figure 3. 8-Bit Configuration

32-BIT DATA WORD CONFIGURATION

Two IDT39C60 EDC units, connected as shown in Figure 5, provide all the logic needed for single bit error correction and double bit error detection of a 32-bit data field. The identification code 32/39 indicates 7 check bits are required. Table 1 gives the ID2, ID1, ID0 values needed for distinguishing the byte 0/1 from byte 2/3. Valid syndrome, check bits and the $\overline{\text{ERROR}}$ and $\overline{\text{MULTERROR}}$ signal come from the byte 2/3 unit. Control signals not indicated are connected to both units in parallel. The $\overline{\text{OE}}$sc always enables the SC0-6 outputs of byte 0/1, but must be used to select data check bits or syndrome bits fed back from the byte 2/3 for data correction modes.

Data In bits 0 through 15 are connected to the same numbered inputs of the byte 0/1 EDC unit, while Data In bits 16 through 31 are connected to byte 2/3 Data Inputs 0 to 15, respectively.

Figure 4 indicates the 39-bit data format for 4 bytes of data and 7 check bits. Check bits are input to the byte 0/1 unit through a tri-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 32-bit configuration requires a feedback of sydrome bits from byte 2/3 into the byte 0/1 unit. The MUX shown on the functional block diagram is used to select the CB0-6 pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating mode available for the 32/39 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, Sn is the XOR of check bits Cn from those read with those generated. Table 7 indicates the decoding of the seven syndrome bits to determine the bit-in-error for a single bit error, or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 8 in relating a single IDT39C60 EDC with the two cascaded units of Figure 5. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

Table 9 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC0-6 outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Table 10 indicates the data bits participating in the check bit generation. For example, check bit C0 is the Exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate Mode.

					Hex	0	1	2	3	4	5	6	7
	Syndrome Bits				S6	0	0	0	0	1	1	1	1
					S5	0	0	1	1	0	0	1	1
					S4	0	1	0	1	0	1	0	1
Hex	S_3	S_2	S_1	S_0									
0	0	0	0	0		*	C4	C5	T	C6	T	T	30
1	0	0	0	1		C0	T	T	14	T	M	M	T
2	0	0	1	0		C1	T	T	M	T	2	24	T
3	0	0	1	1		T	18	8	T	M	T	T	M
4	0	1	0	0		C2	T	T	15	T	3	25	T
5	0	1	0	1		T	19	9	T	M	T	T	31
6	0	1	1	0		T	20	10	T	M	T	T	M
7	0	1	1	1		M	T	T	M	T	4	26	M
8	1	0	0	0		C3	T	T	M	T	5	27	T
9	1	0	0	1		T	21	11	T	M	T	T	M
A	1	0	1	0		T	22	12	T	1	T	T	M
B	1	0	1	1		17	T	T	M	T	6	28	T
C	1	1	0	0		T	23	13	T	M	T	T	M
D	1	1	0	1		M	T	T	M	T	7	29	T
E	1	1	1	0		16	T	T	M	T	M	M	T
F	1	1	1	1		T	M	M	T	0	T	T	M

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

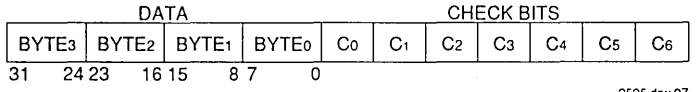
2595 tbl 08

Table 7. Syndrome Decode to Bit-In-Error (32-Bit Configuration)

32-Bit Propagation Delay		Component Delay From IDT39C60
From	To	AC Specifications
DATA	Check Bits Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	Corrected DATAOUT	(DATA to SC) + (CB to SC, CODE ID 011) + CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	$\overline{\text{ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{ERROR}}$, CODE ID011)
DATA	$\overline{\text{MULT ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 011)

2595 tbl 09

Table 8. Key AC Calculations for the 32-Bit Configuration



Uses Modified Hamming Code 32/39
32 Data Bits with 7 Check Bits

Figure 4. 32-Bit Data Format

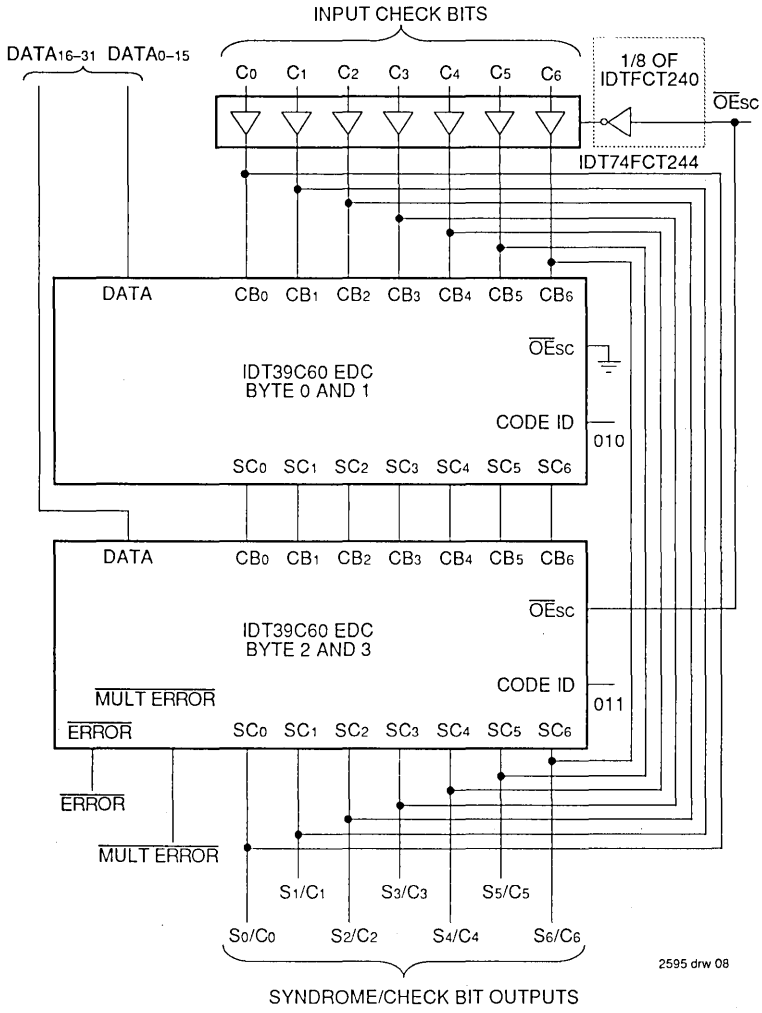


Figure 5. 32-Bit Configuration

Data Bit	Internal Function
0	Diagnostic Check Bit0
1	Diagnostic Check Bit1
2	Diagnostic Check Bit2
3	Diagnostic Check Bit3
4	Diagnostic Check Bit4
5	Diagnostic Check Bit5
6	Diagnostic Check Bit6
7	Don't Care
8	Slice 0/1 — CODE ID0
9	Slice 0/1 — CODE ID1
10	Slice 0/1 — CODE ID2
11	Slice 0/1 — DIAG MODE0
12	Slice 0/1 — DIAG MODE1
13	Slice 0/1 — CORRECT
14	Slice 0/1 — PASSTHRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 — CODE ID0
25	Slice 2/3 — CODE ID1
26	Slice 2/3 — CODE ID2
27	Slice 2/3 — DIAG MODE0
28	Slice 2/3 — DIAG MODE1
29	Slice 2/3 — CORRECT
30	Slice 2/3 — PASSTHRU
31	Don't Care

2595 tbl 10

Table 9. Diagnostic Latch Loading — 32-Bit Format

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C0	Even (XOR)	X				X		X	X	X	X		X			X	
C1	Even (XOR)	X	X	X		X		X		X		X		X			
C2	Odd (XNOR)	X			X	X			X		X	X			X		X
C3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C5	Even (XOR)									X	X	X	X	X	X	X	X
C6	Even (XOR)	X	X	X	X	X	X	X	X								

2595 tbl 11

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C0	Even (XOR)		X	X	X		X					X		X	X		X
C1	Even (XOR)	X	X	X		X		X		X		X		X			
C2	Odd (XNOR)	X			X	X			X		X	X			X		X
C3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C5	Even (XOR)									X	X	X	X	X	X	X	X
C6	Even (XOR)									X	X	X	X	X	X	X	X

2595 tbl 12

Table 10. 32-Bit Modified Hamming Code — Check Bit Encode Chart

64-BIT DATA WORD CONFIGURATION

The IDT39C60 EDC units connected with the MSI gates, as shown in Figure 6, provide all the logic needed for single bit error detection and double bit error detection of a 64-bit data field. The Identification code 64/72 is used, indicating 8 check bits are required. Check bits and Syndrome bits are generated external to the IDT39C60 EDC using Exclusive-OR gates. For error correction, the syndrome bits must be fed back to the CB_{0-6} inputs. Thus, external tri-state buffers are used to select between the check bits read in from memory and the syndrome bits being fed back.

The $\overline{ERROR}$ signal is low for one or more errors detected. From any of the 4 devices, $\overline{MULTERROR}$ is low for some double bit errors and for all three bit errors. Both are high otherwise. The DOUBLE ERROR signal is high only when a double bit error is detected.

Figure 6 indicates the 72-bit data format of 8 bytes of data and 8 check bits. Check bits are input to the various units through a tri-state buffer such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits as generated external to the IDT39C60 EDC. The MUX shown on the functional block diagram is used to select the CB_{0-6} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 64/72 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 11 indicates the decoding of the 8 syndrome bits to determine the bit-in-error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

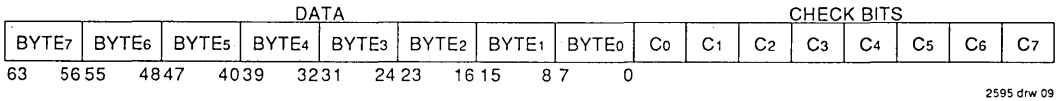
In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 12 in relating a single IDT39C60 EDC with the four units of Figure 7. Delay through the Exclusive-OR gates and the 3-state buffer must be included.

Table 13 indicates the Data Bits participating in the check bit generation. For example, check bit C_0 is the Exclusive-OR function of the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. In the PASSTHRU mode, the contents of the check bit latch are passed through the external Exclusive-OR gates and appear inverted at the outputs C_0 to C_7.

Table 14 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic Check Bits to determine syndrome bits or to pass as check bits to the SC_{0-6} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Some multiple errors will cause a data bit to be inverted. For example, in the 16-bit mode where bits 8 and 13 are in error, the syndrome 111100 (S_0, S_1, S_2, S_3, S_4, S_5) is produced. The bit-in-error decoder receives the syndrome 11100 (S_0, S_1, S_2, S_3, S_4) which it decodes as a single error in data bit 0 and inverts that bit. Figure 8 indicates a method for inhibiting correction when a multiple error occurs.



2595 drw 09

Uses Modified Hamming Code 64/72
32 Data Bits with 8 Check Bits

Figure 6. 64-Bit Data Format

					Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
					S_7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
					S_6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	Syndrome Bits				S_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Hex	S_3	S_2	S_1	S_0																	
0	0	0	0	0		*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1		C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0		C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1		T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0		C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1		T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0		T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1		M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0		C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1		T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0		T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1		17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0		T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1		M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0		16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1		T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

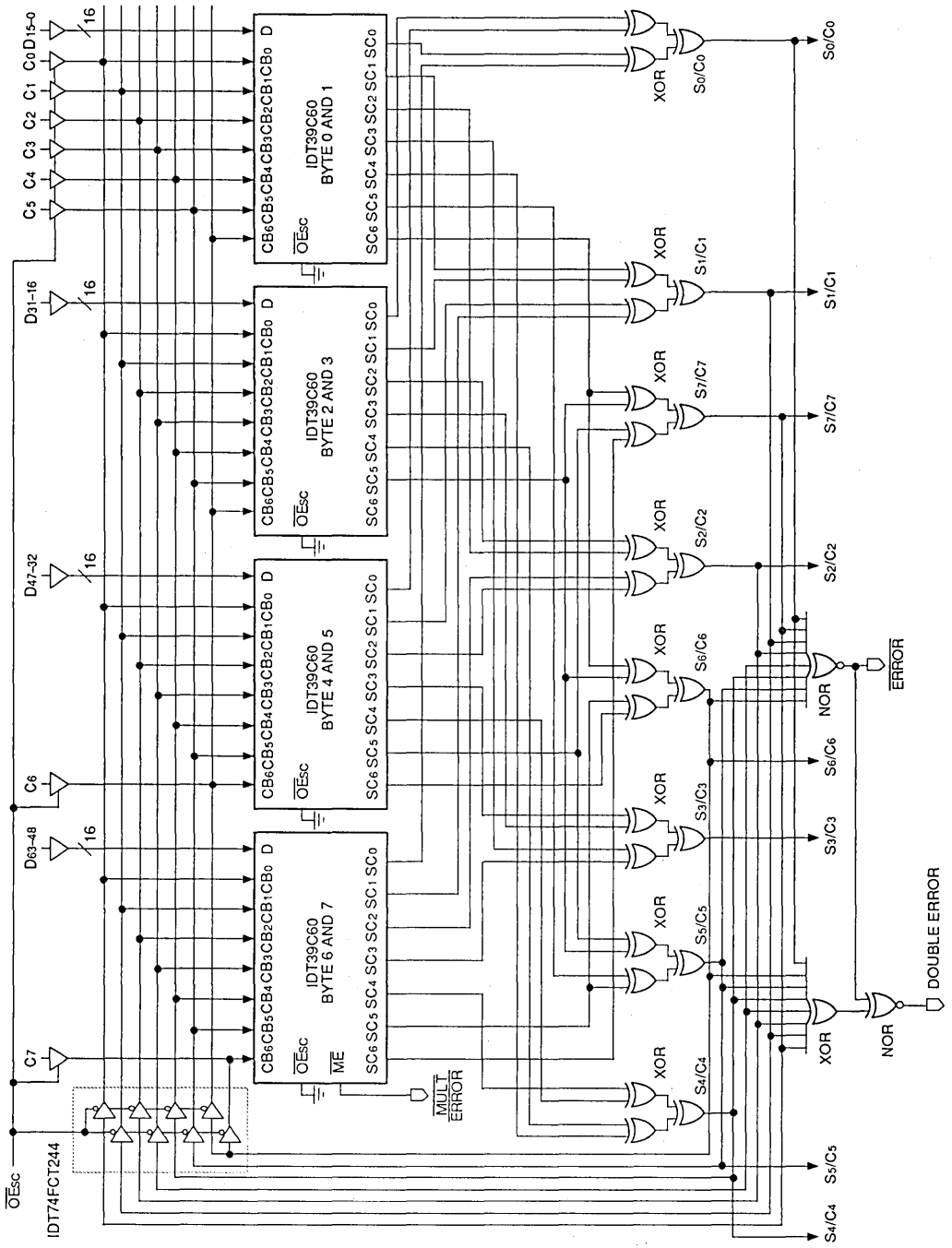
2595 tbl 13

Table 11. Syndrome Decode to Bit-In-Error (64-Bit Configuration)

64-Bit Propagation Delay		Component Delay From IDT39C60
From	To	AC Specifications
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA	Corrected $DATA_{OUT}$	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	$\overline{ERROR}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	$\overline{MULT\ ERROR}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to $\overline{MULT\ ERROR}$, CODE ID 1xx)
DATA	DOUBLE ERROR for 64 Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

2595 tbl 14

Table 12. Key AC Calculations for the 64-Bit Configuration



NOTES:
1. In PASSTHRU mode the contents of the Check Latch appears on the XOR outputs inverted.
2. In Diagnostic Generate mode the contents of the Diagnostic Latch appear on the XOR outputs inverted.

Figure 7. 64-Bit Configuration

Generated Check Bits	Parity	Participating Data Bits[1]															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

2595 tbl 15

Generated Check Bits	Parity	Participating Data Bits[1]															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)									X	X	X	X	X	X	X	X

2595 tbl 16

Generated Check Bits	Parity	Participating Data Bits[1]															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)									X	X	X	X	X	X	X	X

2595 tbl 17

Generated Check Bits	Parity	Participating Data Bits[1]															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

NOTE:
1. The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

2595 tbl 18

Table 13. 64-Bit Modified Hamming Code — Check Bit Encode Chart

Data Bit	Internal Function
0	Diagnostic Check Bit0
1	Diagnostic Check Bit1
2	Diagnostic Check Bit2
3	Diagnostic Check Bit3
4	Diagnostic Check Bit4
5	Diagnostic Check Bit5
6, 7	Don't Care
8	Slice 0/1 — CODE ID0
9	Slice 0/1 — CODE ID1
10	Slice 0/1 — CODE ID2
11	Slice 0/1 — DIAG MODE0
12	Slice 0/1 — DIAG MODE1
13	Slice 0/1 — CORRECT
14	Slice 0/1 — PASSTHRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 — CODE ID0
25	Slice 2/3 — CODE ID1
26	Slice 2/3 — CODE ID2
27	Slice 2/3 — DIAG MODE0
28	Slice 2/3 — DIAG MODE1
29	Slice 2/3 — CORRECT
30	Slice 2/3 — PASSTHRU

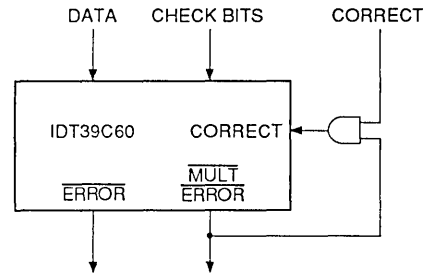
2595 tbl 19

Data Bit	Internal Function
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit6
39	Don't Care
40	Slice 4/5 — CODE ID0
41	Slice 4/5 — CODE ID1
42	Slice 4/5 — CODE ID2
43	Slice 4/5 — DIAG MODE0
44	Slice 4/5 — DIAG MODE1
45	Slice 4/5 — CORRECT
46	Slice 4/5 — PASSTHRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit7
56	Slice 6/7 — CODE ID0
57	Slice 6/7 — CODE ID1
58	Slice 6/7 — CODE ID2
59	Slice 6/7 — DIAG MODE0
60	Slice 6/7 — DIAG MODE1
61	Slice 6/7 — CORRECT
62	Slice 6/7 — PASSTHRU
63	Don't Care

2595 tbl 20

Table 14. Diagnostic Latch Loading — 64-Bit Format

Some multiple errors will cause a data bit to be inverted. For example, in the 16-bit mode where bits 8 and 13 are in error, the syndrome 111100 (S_0, S_1, S_2, S_3, S_4, S_5) is produced. The bit-in-error decoder receives the syndrome 11100 (S_0, S_1, S_2, S_3, S_4) which it decodes as a single error in data bit 0 and inverts that bit. Figure 8 indicates a method for inhibiting correction when a multiple error occurs.



2595 drw 11

Figure 8. Inhibition of Data Modification

FUNCTIONAL EQUATIONS

The following equations and tables describe in detail how the output values of the IDT39C60 EDC are determined as a function of the value of the inputs and the internal states. Be sure to carefully read the following definitions of symbols before examining the tables.

DEFINITIONS

$D_I \leftarrow$ DATAI if $\overline{LE_{IN}}$ is HIGH or the output of bit I of the Data Input Latch if $\overline{LE_{IN}}$ is LOW
$C_I \leftarrow$ CB_I if $\overline{LE_{IN}}$ is HIGH or the output of bit I of the Check Bit Latch if $\overline{LE_{IN}}$ is LOW
$DL_I \leftarrow$ Output of bit I of the Diagnostic Latch
$S_I \leftarrow$ Internally generated syndromes (same as outputs of SC_I if outputs enabled)

$PA \leftarrow D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12}$

$PB \leftarrow D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7$

$PC \leftarrow D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14}$

$PD \leftarrow D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15}$

$PE \leftarrow D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13}$

$PF \leftarrow D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_{14} \oplus D_{15}$

$PG_1 \leftarrow D_1 \oplus D_4 \oplus D_6 \oplus D_7$

$PG_2 \leftarrow D_1 \oplus D_2 \oplus D_3 \oplus D_5$

$PG_3 \leftarrow D_8 \oplus D_9 \oplus D_{11} \oplus D_{14}$

$PG_4 \leftarrow D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15}$

Error Signals

$\overline{ERROR} \leftarrow (\overline{S6} \cdot \overline{(ID_1 + ID_2)}) \cdot \overline{S5} \cdot \overline{S4} \cdot \overline{S3} \cdot \overline{S2} \cdot \overline{S1} \cdot \overline{S0}$ + GENERATE + INITIALIZE + PASSTHRU

$\overline{MULT\ ERROR}$:
(16 and 32-Bit Modes) $\leftarrow \overline{((S6 \cdot ID_1) \oplus S5 \oplus S4 \oplus S3 \oplus S2 \oplus S1 \oplus S0)\ (ERROR)}$ + TOME + GENERATE + PASSTHRU + INITIALIZE

$\overline{MULT\ ERROR}$: (64-Bit Modes) $\leftarrow$ $\overline{TOME}$ + GENERATE + PASSTHRU + INITIALIZE

		Hex	0		1		2		3		4		5		6		7	
		S_6	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		S_5	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	Syndrome[1,2] Bits	S_4	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		S_3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Hex	S_2 S_1 S_0																	
0 8	0 0 0									1		1	1		1			1
1 9	0 0 1			1			1			1	1	1	1		1		1	1
2 A	0 1 0				1				1	1	1						1	1
3 B	0 1 1	1							1	1	1						1	1
4 C	1 0 0		1							1	1	1						1
5 D	1 0 1	1	1							1	1	1						1
6 E	1 1 0	1			1		1	1	1	1			1		1	1		
7 F	1 1 1	1			1		1	1	1	1			1		1	1	1	

NOTES: 2595 tbl 21

1. S_6, S_5, ... S_0 are internal syndromes except in Modes 010, 100, 101, 110, 111 (CODE ID_2, ID_1, ID_0). In these modes, the syndromes are input over the check bit lines. $S_6 \leftarrow C_6$, $S_5 \leftarrow C_5$, ... $S_1 \leftarrow C_1$, $S_0 \leftarrow C_0$.
2. The S_6 internal syndrome is always forced to 0 in CODE ID 000.

Table 15. TOME (Three or More Errors)

Generate Mode (Check Bits)	CODE ID_{0-2}						
	000	010	011	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_3$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	PA	PA	$PA \oplus CB_1$	PA	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD}$	$\overline{PD}$	$PD \oplus CB_2$	$\overline{PD}$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE}$	$\overline{PE}$	$PE \oplus CB_3$	$\overline{PE}$	PE	PE	PE
$SC_4 \leftarrow$	PF	PF	$PF \oplus CB_4$	PF	PF	PF	PF
$SC_5 \leftarrow$	PC	PC	$PC \oplus CB_5$	PC	PC	PC	PC
$SC_6 \leftarrow$	1	PB	$PC \oplus CB_6$	PB	PB	PB	PB

2595 tbl 22

Table 16. Generate Mode (Check Bits)

Detect and Correct Modes (Syndromes)	CODE ID_{0-2}						
	000	010	011 (1)	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus C_0$	$PG_1 \oplus PG_3 \oplus C_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus C_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus C_1$	$PA \oplus C_1$	$PA \oplus CB_1$	$PA \oplus C_1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus C_2$	$\overline{PD} \oplus C_2$	$PD \oplus CB_2$	$\overline{PD} \oplus C_2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus C_3$	$\overline{PE} \oplus C_3$	$PE \oplus CB_3$	$\overline{PE} \oplus C_3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus C_4$	$PF \oplus C_4$	$PF \oplus CB_4$	$PF \oplus C_4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus C_5$	$PC \oplus C_5$	$PC \oplus CB_5$	$PC \oplus C_5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus C_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus C_6$	$PB \oplus C_6$

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

2595 tbl 23

Table 17. Detect and Correct Modes (Syndromes)

Diagnostic Detect and Correct Mode	CODE ID_{0-2}						
	000	010	011 (1)	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_1 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus DL_1$	$PA \oplus DL_1$	$PA \oplus CB_1$	$PA \oplus DL_1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus DL_2$	$\overline{PD} \oplus DL_2$	$PD \oplus CB_2$	$\overline{PD} \oplus DL_2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus DL_3$	$\overline{PE} \oplus DL_3$	$PE \oplus CB_3$	$\overline{PE} \oplus DL_3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus DL_4$	$PF \oplus DL_4$	$PF \oplus CB_4$	$PF \oplus DL_4$	PF	PF	PF
$SC_5 \leftarrow$	$PDL \oplus DL_5$	$PC \oplus DL_5$	$PC \oplus CB_5$	$PC \oplus DL_5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus DL_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus DL_6$	$PB \oplus DL_7$

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

2595 tbl 24

Table 18. Diagnostic Detect and Correct Mode

Diagnostic Generate Mode	CODE ID_{0-2}						
	000	010	011 (1)	100	101	110	111
$SC_0 \leftarrow$	DL_0	DL_0	CB_0	DL_0	1	1	1
$SC_1 \leftarrow$	DL_1	DL_1	CB_1	DL_1	1	1	1
$SC_2 \leftarrow$	DL_2	DL_2	CB_2	DL_2	1	1	1
$SC_3 \leftarrow$	DL_3	DL_3	CB_3	DL_3	1	1	1
$SC_4 \leftarrow$	DL_4	DL_4	CB_4	DL_4	1	1	1
$SC_5 \leftarrow$	DL_5	DL_5	CB_5	DL_5	1	1	1
$SC_6 \leftarrow$	1	DL_6	CB_6	1	1	DL_6	DL_7

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

2595 tbl 25

Table 19. Diagnostic Generate Mode

PASSTHRU Mode	CODE ID_{0-2}						
	000	010	011 (1)	100	101	110	111
$SC_0 \leftarrow$	C_0	C_0	CB_0	C_0	1	1	1
$SC_1 \leftarrow$	C_1	C_1	CB_1	C_1	1	1	1
$SC_2 \leftarrow$	C_2	C_2	CB_2	C_2	1	1	1
$SC_3 \leftarrow$	C_3	C_3	CB_3	C_3	1	1	1
$SC_4 \leftarrow$	C_4	C_4	CB_4	C_4	1	1	1
$SC_5 \leftarrow$	C_5	C_5	CB_5	C_5	1	1	1
$SC_6 \leftarrow$	1	C_6	CB_6	1	1	C_6	C_6

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

2595 tbl 26

Table 20. PASSTHRU Mode

		S_5	0	0	0	0	1	1	1	1
		S_4	0	0	1	1	0	0	1	1
S_2	S_1	S_3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE: 2595 tbl 27
1. Unlisted S combinations are no correction.

Table 21. CODE ID_{2-0} = 000

		C_6	0	0	0	0	1	1	1	1
		C_5	1	1	1	1	0	0	0	0
		C_4	0	0	1	1	0	0	1	1
C_2	C_1	C_3	0	1	0	1	0	1	0	1
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

NOTE: 2595 tbl 28
1. Unlisted C_n combinations are no correction.

Table 22. CODE ID_{2-0} = 010

		S_6	0	0	0	0	1	1	1	1
		S_5	0	0	0	0	1	1	1	1
		S_4	0	0	1	1	0	0	1	1
S_2	S_1	S_3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE: 2595 tbl 29
1. Unlisted S combinations are no correction.

Table 23. CODE ID_{2-0} = 011

		C_0	0	0	0	0	1	1	1	1
		C_6	0	0	0	0	1	1	1	1
		C_5	1	1	1	1	0	0	0	0
		C_4	0	0	1	1	0	0	1	1
C_2	C_1	C_3	0	1	0	1	0	1	0	1
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

NOTE: 2595 tbl 30
1. Unlisted C_n combinations are no correction.

Table 24. CODE ID_{2-0} = 100

		C_0	0	0	0	0	1	1	1	1
		C_6	0	0	0	0	1	1	1	1
		C_5	0	0	0	0	1	1	1	1
		C_4	0	0	1	1	0	0	1	1
C_2	C_1	C_3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE: 2595 tbl 31
1. Unlisted C_n combinations are no correction.

Table 25. CODE ID_{2-0} = 101

		C_0	0	0	0	0	1	1	1	1
		C_6	1	1	1	1	0	0	0	0
		C_5	0	0	0	0	1	1	1	1
		C_4	0	0	1	1	0	0	1	1
C_2	C_1	C_3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE: 2595 tbl 32
1. Unlisted C_n combinations are no correction.

Table 26. CODE ID_{2-0} = 110

		C_0	0	0	0	0	1	1	1	1
		C_6	1	1	1	1	0	0	0	0
		C_5	1	1	1	1	0	0	0	0
		C_4	0	0	1	1	0	0	1	1
C_2	C_1	C_3	0	1	0	1	0	1	0	1
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

NOTE: 2595 tbl 33
1. Unlisted C_n combinations are no correction.

Table 27. CODE ID_{2-0} = 111

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to Ground	−0.5 to VCC + 0.5	−0.5 to VCC + 0.5	V
VCC	Power Supply Voltage	−0.5 to +7.0	−0.5 to +7.0	V
TA	Operating Temperature	0 to +70	−55 to +125	°C
TBIAS	Temperature Under Bias	−55 to +125	−65 to +135	°C
TSTG	Storage Temperature	−55 to +125	−65 to +150	°C
IOUT	DC Output Current	30	30	mA

NOTE: 2595 tbl 34

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	5	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

NOTE: 2595 tbl 35

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%; Military: TA = −55°C to +125°C, VCC = 5.0V ± 10%
VLC = 0.2V; VHC = VCC − 0.2V

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
VIH	Input HIGH Level	Guaranteed Logic HIGH Level(4)		2.0	—	—	V
VIL	Input LOW Level	Guaranteed Logic LOW Level(4)		—	—	0.8	V
IIH	Input HIGH Current	VCC = Max., VIN = VCC		—	0.1	10	µA
IIL	Input LOW Current	VCC = Max., VIN = GND		—	−0.1	−10	µA
VOH	Output HIGH Voltage	VCC = Min.	IOH = −300µA	VHC	VCC	—	V
			IOH = −6mA MIL.	2.4	4.3	—	
			IOH = −6mA COM'L.	2.4	4.3	—	
VOL	Output LOW Voltage	VCC = Min.	IOL = 300µA	—	GND	VLC	V
			IOL = 8mA MIL.	—	0.3	0.5	
			IOL = 8mA COM'L.	—	0.3	0.5	
IOZ	Off State (High Impedance) Output Current	VCC = Max.	VO = 0V	—	−0.1	−20	µA
			VO = VCC (Max.)	—	0.1	20	
IOS	Output Short Circuit Current	VCC = Max., VOUT = 0V(3)		−20	—	—	mA

NOTES: 2595 tbl 36

1. For conditions shown as Max. or Min. use appropriate value specified under DC Electrical Characteristics.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels should only be static tested in a noise-free environment. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS (Cont'd.)

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 2.0V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current (CMOS) Inputs	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{OP} = 0		—	3.0	5.0	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High)[3]	V_{CC} = Max., V_{IN} = 3.4V, f_{OP} = 0		—	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	—	5.0	8.5	mA/ MHz
			COM'L.	—	5.0	7.0	
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty Cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	—	53	90	mA
			COM'L.	—	53	75	
		V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty Cycle V_{IN} = 3.4V, V_{IN} = 0.4V	MIL.	—	60	100	
			COM'L.	—	60	85	

2595 tbl 37

NOTES:
1. For conditions shown as Max. or Min. use appropriate value specified under DC Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
4. Total Supply Current is the sum of the Quiescent Current and the Dynamic Current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   $I_{CC} = I_{CCQ} + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{OP})$
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
   N_T = Number of dynamic inputs driven at TTL levels
   f_{OP} = Operating frequency

5

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.

IDT 39C60B AC ELECTRICAL CHARACTERISTICS

Temperature range: –55°C to +125°C; VCC = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

MAXIMUM PROPAGATION DELAYS C_L = 50pF

	From Input		To Output SC0–7	To Output DATA0–31	To Output ERROR	To Output MULT ERROR	Unit
	DATA0–15		22	30(1)	22	25	ns
	CB0–7 (CODE ID1, 0 = 00, 11)		14	26	20	24	ns
	CB0–7 (CODE ID1, 0 = 10)		14	19	20	24	ns
	$\overline{\text{GENERATE}}$	↘	15	—	↗↘ 14	↗↘ 19	ns
	CORRECT Not Internal Control Mode		—	20	—	—	ns
	DIAG MODE and PASSTHRU Not Internal Control Mode		24	26	19	21	ns
	CODE ID 1, 0		24	29	26	29	ns
	LEIN From latched to transparent	↗	24	34	24	26	ns
	LEOUT From latched to transparent	↗	—	13	—	—	ns
	LEDIAG From latched to transparent	↗	24	34	24	26	ns
Internal Control Mode	LEDIAG From latched to transparent	↗	29	40	29	32	ns
Internal Control Mode	DATA0–15 Via Diagnostic Latch		29	40	29	32	ns

2595 tbl 38

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)	Set-up Time	Hold Time	Unit
DATA0–15	↘	LEIN	6	4	ns
CB0–7 (not applic. to CODE ID1, 0 = 11)	↘		6	4	ns
DATA0–15	↘	LEOUT	29	2	ns
CB0–7 (CODE ID 00, 11)	↘		25	0	ns
CB0–7 (CODE ID 10)	↘		25	0	ns
CORRECT	↗ ↘		26	—	ns
DIAG MODE	↘		26	0	ns
CODE ID1, 0	↘		30	0	ns
LEIN	↗ ↘		34	—	ns
DATA0–15		LEDIAG	6	4	ns

2595 tbl 39

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

From Input	Enable	Disable	To Output	Enable Max.	Disable Max.	Unit
$\overline{\text{OE}}$ Byte00-3	↘	↗	DAT0–15	15	12	ns
$\overline{\text{OESC}}$	↘	↗	SC0–7	15	12	ns

2595 tbl 40

MINIMUM PULSE WIDTHS

			Min.	
LEIN, LEOUT, LEDIAG	↗↘	(Positive-going pulse)	10	ns

2595 tbl 41

5

IDT39C60B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60B over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS C_L = 50pF

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	18	25 (1)	18	20
CB_{0-6} ($CODE\ ID_{2-0}$ 000, 011)	12	22	17	20
CB_{0-6} ($CODE\ ID_{2-0}$ 010, 100, 101, 110, 111)	12	16	17	20
$\overline{GENERATE}$	13	—	—	—
CORRECT (Not Internal Control Mode)	—	17	—	—
DIAG MODE (Not Internal Control Mode)	20	22	16	19
PASSTHRU (Not Internal Control Mode)	20	22	16	19
$CODE\ ID_{1-0}$	20	22	22	24
LE_{IN} (From latched to transparent)	20	28	20	22
LE_{OUT} (From latched to transparent)	—	11	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	20	28	20	22
Internal Control Mode: LE_{DIAG} (From latched to transparent)	24	33	24	27
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	24	33	24	27

NOTE: 2595 tbl 42

1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	24	2
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	21	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	21	0
CORRECT	LE_{OUT}	22	0
DIAG MODE	LE_{OUT}	22	0
PASSTHRU	LE_{OUT}	22	0
$CODE\ ID_{2-0}$	LE_{OUT}	25	0
LE_{IN}	LE_{OUT}	28	0
$DATA_{0-15}$	LE_{DIAG}	5	3

2595 tbl 43

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

Input	Output	Enable Max.	Disable Max.
$\overline{OE}\ BYTE_0$, $\overline{OE}\ BYTE_1$	$DATA_{0-15}$	12	10
$\overline{OE}_{SC}$	SC_{0-6}	12	10

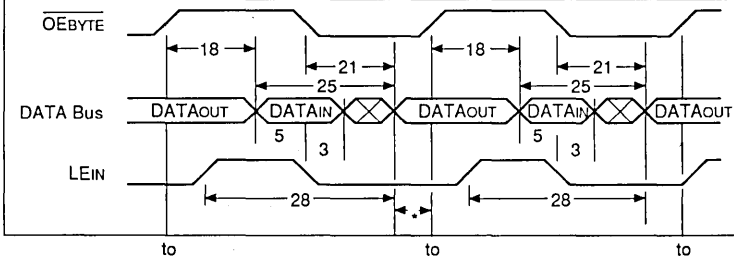
2595 tbl 44

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	8

2595 tbl 45

IDT39C60B COMMERCIAL — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 51ns (fMAX = 19.6MHz)

Timing Parameter From	To	Min./ Max.
OEBYTE = High to DATAOUT Disabled		Max.
OEBYTE = Low to DATAOUT Enabled		Max.
DATAIN to Corrected DATAOUT		Max.
DATAIN Set-up to LEIN = Low		Min.
DATAIN Hold to LEIN = Low		Min.
LEIN = High to DATAOUT		Max.
* = (Memory/System dependent)		

2595 drw 12

5

IDT39C60A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60A over the commercial operating range of 0°C to +70°C, with Vcc from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS C_L = 50pF

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{Error}$	$\overline{MULT}$ $\overline{ERROR}$
$DATA_{0-15}$	20	30[1]	20	23
CB_{0-6} ($CODE\ ID_{2-0}$ 000, 011)	14	25	20	23
CB_{0-6} ($CODE\ ID_{2-0}$ 010, 100, 101, 110, 111)	14	18	20	23
$\overline{GENERATE}$	15	—	—	—
CORRECT (Not Internal Control Mode)	—	20	—	—
DIAG MODE (Not Internal Control Mode)	22	25	18	21
PASSTHRU (Not Internal Control Mode)	22	25	18	21
$CODE\ ID_{2-0}$	23	28	25	28
LE_{IN} (From latched to transparent)	22	32	22	25
LE_{OUT} (From latched to transparent)	—	13	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	22	32	22	25
Internal Control Mode: LE_{DIAG} (From latched to transparent)	28	38	28	31
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	28	38	28	31

NOTE: 2595 tbl 46

1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	24	2
CB_{0-6} ($CODE\ ID$ 000, 011)	LE_{OUT}	21	0
CB_{0-6} ($CODE\ ID$ 010, 100, 101, 110, 111)	LE_{OUT}	21	0
CORRECT	LE_{OUT}	22	0
DIAG MODE	LE_{OUT}	22	0
PASSTHRU	LE_{OUT}	22	0
$CODE\ ID_{2-0}$	LE_{OUT}	25	0
LE_{IN}	LE_{OUT}	28	0
$DATA_{0-15}$	LE_{DIAG}	5	3

2595 tbl 47

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

Input	Output	Enable	Disable
$\overline{OE}\ BYTE_0$, $\overline{OE}\ BYTE_1$	$DATA_{0-15}$	24	21
$\overline{OE}_{SC}$	SC_{0-6}	24	21

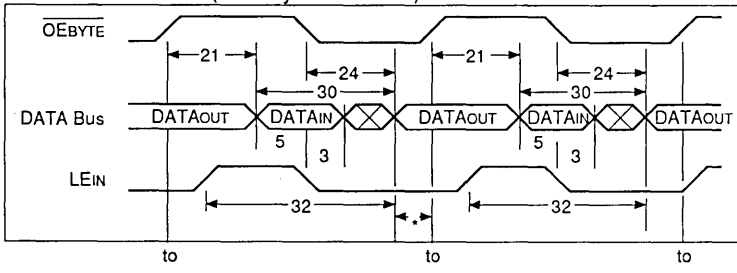
2595 tbl 48

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

2595 tbl 49

IDT39C60A COMMERCIAL — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 61ns (fMAX = 16.4MHz)

Timing Parameter From	To	Min./ Max.
OEBYTE	DATAOUT Disabled	Max.
OEBYTE	DATAOUT Enabled	Max.
DATAIN	Corrected DATAOUT	Max.
DATAIN Set-up	LEIN = Low	Min.
DATAIN Hold	LEIN = Low	Min.
LEIN	DATAOUT	Max.

* = (Memory/System dependent)

2595 drw 13

5

IDT39C60A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60A over the military operating range of –55°C to +125°C, with Vcc from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS C_L = 50pF

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	22	35[1]	24	27
CB_{0-6} ($CODE\ ID_{2-0}$ 000, 011)	17	28	24	27
CB_{0-6} ($CODE\ ID_{2-0}$ 010, 100, 101, 110, 111)	17	20	24	27
$\overline{GENERATE}$	20	—	—	—
CORRECT (Not Internal Control Mode)	—	25	—	—
DIAG MODE (Not Internal Control Mode)	25	28	21	24
PASSTHRU (Not Internal Control Mode)	25	28	21	24
$CODE\ ID_{2-0}$	26	31	28	31
LE_{IN} (From latched to transparent)	24	37	26	29
LE_{OUT} (From latched to transparent)	—	16	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	24	37	26	29
Internal Control Mode: LE_{DIAG} (From latched to transparent)	30	43	32	35
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	30	43	32	35

NOTE:

1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

2595 tbl 50

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	27	2
CB_{0-6} ($CODE\ ID$ 000, 011)	LE_{OUT}	24	0
CB_{0-6} ($CODE\ ID$ 010, 100, 101, 110, 111)	LE_{OUT}	24	0
CORRECT	LE_{OUT}	25	0
DIAG MODE	LE_{OUT}	25	0
PASSTHRU	LE_{OUT}	25	0
$CODE\ ID_{2-0}$	LE_{OUT}	28	0
LE_{IN}	LE_{OUT}	30	0
$DATA_{0-15}$	LE_{DIAG}	5	3

2595 tbl 51

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

Input	Output	Enable	Disable
$\overline{OE}\ BYTE_0$, $\overline{OE}\ BYTE_1$	$DATA_{0-15}$	28	25
$\overline{OE}_{SC}$	SC_{0-6}	28	25

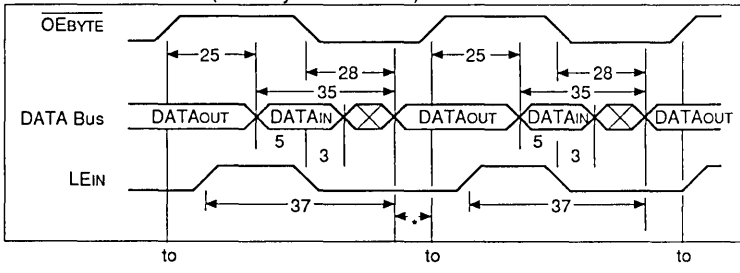
2595 tbl 52

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

2595 tbl 53

IDT39C60A MILITARY — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 70ns (fMAX = 14.3MHz)

Timing Parameter From	To	Min./ Max.
OEBYTE = High to DATAOUT Disabled		Max.
OEBYTE = Low to DATAOUT Enabled		Max.
DATAIN to Corrected DATAOUT		Max.
DATAIN Set-up to LEIN = Low		Min.
DATAIN Hold to LEIN = Low		Min.
LEIN = High to DATAOUT		Max.
* = (Memory/System dependent)		

2595 drw 14

5

IDT39C60-1 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60-1 over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS C_L = 50pF

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	28	52[1]	25	50
CB_{0-6} ($CODE\ ID_{2-0}$ 000, 011)	23	50	23	47
CB_{0-6} ($CODE\ ID_{2-0}$ 010, 100, 101, 110, 111)	28	34	29	34
$\overline{GENERATE}$	35	—	—	—
CORRECT (Not Internal Control Mode)	—	45	—	—
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASSTHRU (Not Internal Control Mode)	36	44	29	46
$CODE\ ID_{2-0}$	61	90	60	80
LE_{IN} (From latched to transparent)	39	72	39	59
LE_{OUT} (From latched to transparent)	—	31	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE_{DIAG} (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

NOTE:

1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

2595 tbl 54

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	6	7
CB_{0-6}	LE_{IN}	5	6
$DATA_{0-15}$	LE_{OUT}	34	5
CB_{0-6} ($CODE\ ID$ 000, 011)	LE_{OUT}	35	0
CB_{0-6} ($CODE\ ID$ 010, 100, 101, 110, 111)	LE_{OUT}	27	0
CORRECT	LE_{OUT}	26	1
DIAG MODE	LE_{OUT}	69	0
PASSTHRU	LE_{OUT}	26	0
$CODE\ ID_{2-0}$	LE_{OUT}	81	0
LE_{IN}	LE_{OUT}	51	5
$DATA_{0-15}$	LE_{DIAG}	6	8

2595 tbl 55

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

Input	Output	Enable	Disable
$\overline{OE}\ BYTE_0$, $\overline{OE}\ BYTE_1$	$DATA_{0-15}$	30	30
$\overline{OE}_{SC}$	SC_{0-6}	30	30

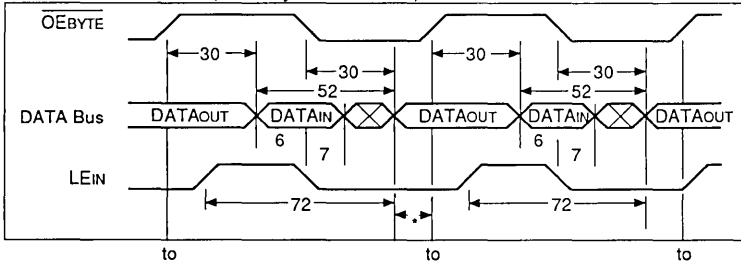
2595 tbl 56

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

2595 tbl 57

IDT39C60–1 COMMERCIAL — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 92ns (fMAX = 10.9MHz)

Timing Parameter From	To	Min./ Max.
OEBYTE	DATAOUT Disabled	Max.
OEBYTE	DATAOUT Enabled	Max.
DATAIN	Corrected DATAOUT	Max.
DATAIN Set-up	LEIN = Low	Min.
DATAIN Hold	LEIN = Low	Min.
LEIN = High	DATAOUT	Max.

* = (Memory/System dependent)

2595 drw 15

5

IDT39C60-1 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60-1 over the military operating range of –55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS C_L = 50pF

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	31	59(1)	28	56
CB_{0-6} ($CODE\ ID_{2-0}$ 000, 011)	25	55	25	50
CB_{0-6} ($CODE\ ID_{2-0}$ 010, 100, 101, 110, 111)	30	38	31	37
$\overline{GENERATE}$	38	—	—	—
CORRECT (Not Internal Control Mode)	—	49	—	—
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASSTHRU (Not Internal Control Mode)	39	51	34	54
$CODE\ ID_{2-0}$	69	100	68	90
LE_{IN} (From latched to transparent)	39	82	43	66
LE_{OUT} (From latched to transparent)	—	33	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	50	88	49	72
Internal Control Mode: LE_{DIAG} (From latched to transparent)	75	106	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106	74	96

2595 tbl 58

NOTE:

1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	7	7
CB_{0-6}	LE_{IN}	5	7
$DATA_{0-15}$	LE_{OUT}	39	5
CB_{0-6} ($CODE\ ID$ 000, 011)	LE_{OUT}	38	0
CB_{0-6} ($CODE\ ID$ 010, 100, 101, 110, 111)	LE_{OUT}	30	0
CORRECT	LE_{OUT}	28	1
DIAG MODE	LE_{OUT}	84	0
PASSTHRU	LE_{OUT}	30	0
$CODE\ ID_{2-0}$	LE_{OUT}	89	0
LE_{IN}	LE_{OUT}	59	5
$DATA_{0-15}$	LE_{DIAG}	7	9

2595 tbl 59

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

Input	Output	Enable	Disable
$\overline{OE}\ BYTE_0$, $\overline{OE}\ BYTE_1$	$DATA_{0-15}$	35	35
$\overline{OE}_{SC}$	SC_{0-6}	35	35

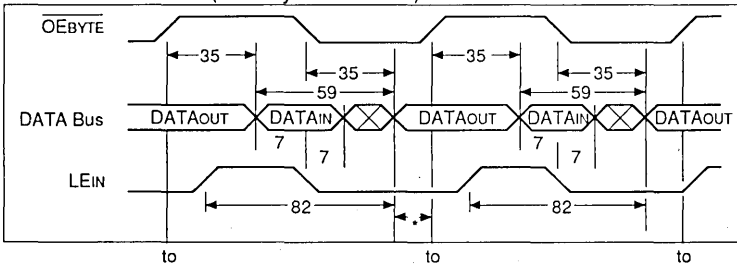
2595 tbl 60

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

2595 tbl 61

IDT39C60–1 MILITARY — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 104ns (fMAX = 9.6MHz)

Timing Parameter From To	Min./ Max.
OEBYTE = High to DATAOUT Disabled	Max.
OEBYTE = Low to DATAOUT Enabled	Max.
DATAIN to Corrected DATAOUT	Max.
DATAIN Set-up to LEIN = Low	Min.
DATAIN Hold to LEIN = Low	Min.
LEIN = High to DATAOUT	Max.
* = (Memory/System dependent)	

2595 drw 16

5

IDT39C60 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60 over the commercial operating range of 0°C to +70°C, with Vcc from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS C_L = 50pF

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	32	65[1]	32	50
CB_{0-6} ($CODE\ ID_{2-0}$ 000, 011)	28	56	29	47
CB_{0-6} ($CODE\ ID_{2-0}$ 010, 100, 101, 110, 111)	28	45	29	34
$\overline{GENERATE}$	35	—	—	—
CORRECT (Not Internal Control Mode)	—	45	—	—
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASSTHRU (Not Internal Control Mode)	36	44	29	46
$CODE\ ID_{2-0}$	61	90	60	80
LE_{IN} (From latched to transparent)	39	72	39	59
LE_{OUT} (From latched to transparent)	—	31	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE_{DIAG} (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

NOTE: 2595 tbl 62

1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	6	7
CB_{0-6}	LE_{IN}	5	6
$DATA_{0-15}$	LE_{OUT}	44	5
CB_{0-6} ($CODE\ ID$ 000, 011)	LE_{OUT}	35	0
CB_{0-6} ($CODE\ ID$ 010, 100, 101, 110, 111)	LE_{OUT}	27	0
CORRECT	LE_{OUT}	26	1
DIAG MODE	LE_{OUT}	69	0
PASSTHRU	LE_{OUT}	26	0
$CODE\ ID_{2-0}$	LE_{OUT}	81	0
LE_{IN}	LE_{OUT}	51	5
$DATA_{0-15}$	LE_{DIAG}	6	8

2595 tbl 63

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

Input	Output	Enable	Disable
$\overline{OE}\ BYTE_0$, $\overline{OE}\ BYTE_1$	$DATA_{0-15}$	30	30
$\overline{OE}_{SC}$	SC_{0-6}	30	30

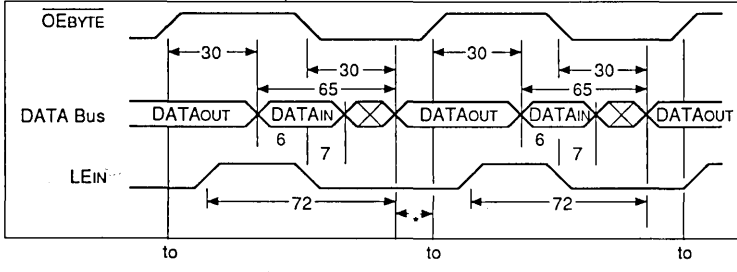
2595 tbl 64

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

2595 tbl 65

IDT39C60 COMMERCIAL — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 105ns (fMAX = 9.5MHz)

Timing Parameter From To	Min./ Max.
OEBYTE = High to DATAOUT Disabled	Max.
OEBYTE = Low to DATAOUT Enabled	Max.
DATAIN to Corrected DATAOUT	Max.
DATAIN Set-up to LEIN = Low	Min.
DATAIN Hold to LEIN = Low	Min.
LEIN = High to DATAOUT	Max.
* = (Memory/System dependent)	

2595 drw 17

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IDT39C60 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60 over the military operating range of –55°C to +125°C, with Vcc from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS C_L = 50pF

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT}$ $\overline{ERROR}$
$DATA_{0-15}$	35	73[1]	36	56
CB_{0-6} ($CODE\ ID_{2-0}$ 000, 011)	30	61	31	50
CB_{0-6} ($CODE\ ID_{2-0}$ 010, 100, 101, 110, 111)	30	50	31	37
$\overline{GENERATE}$	38	—	—	—
CORRECT (Not Internal Control Mode)	—	49	—	—
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASSTHRU (Not Internal Control Mode)	39	51	34	54
$CODE\ ID_{2-0}$	69	100	68	90
LE_{IN} (From latched to transparent)	44	82	43	66
LE_{OUT} (From latched to transparent)	—	33	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	50	88	49	72
Internal Control Mode: LE_{DIAG} (From latched to transparent)	75	106	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106	74	96

NOTE: 2595 tbl 66

1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	7	7
CB_{0-6}	LE_{IN}	5	7
$DATA_{0-15}$	LE_{OUT}	50	5
CB_{0-6} ($CODE\ ID$ 000, 011)	LE_{OUT}	38	0
CB_{0-6} ($CODE\ ID$ 010, 100, 101, 110, 111)	LE_{OUT}	30	0
CORRECT	LE_{OUT}	28	1
DIAG MODE	LE_{OUT}	84	0
PASSTHRU	LE_{OUT}	30	0
$CODE\ ID_{2-0}$	LE_{OUT}	89	0
LE_{IN}	LE_{OUT}	59	5
$DATA_{0-15}$	LE_{DIAG}	7	9

2595 tbl 67

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

Input	Output	Enable	Disable
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	35	35
$\overline{OE}_{SC}$	SC_{0-6}	35	35

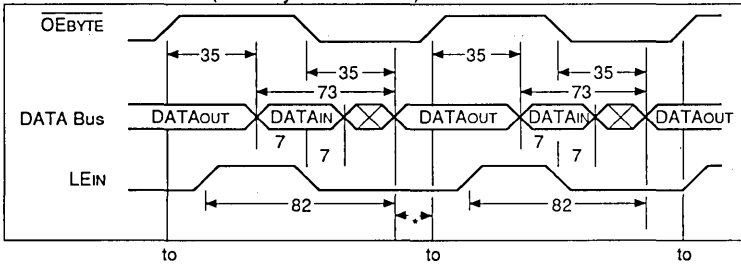
2595 tbl 68

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

2595 tbl 69

IDT39C60 MILITARY — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 118ns (fMAX = 8.5MHz)

Timing Parameter From	To	Min./ Max.
OEBYTE = High to DATAOUT Disabled		Max.
OEBYTE = Low to DATAOUT Enabled		Max.
DATAIN to Corrected DATAOUT		Max.
DATAIN Set-up to LEIN = Low		Min.
DATAIN Hold to LEIN = Low		Min.
LEIN = High to DATAOUT		Max.
* = (Memory/System dependent)		

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 12

2595 tbl 70

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2595 tbl 71

IDT39C60 INPUT/OUTPUT INTERFACE CIRCUIT

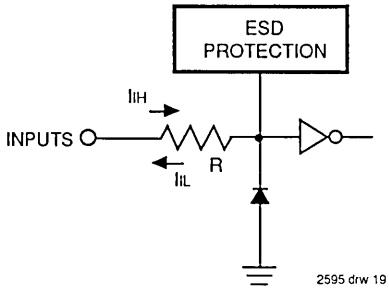


Figure 10. Input Structure (All Inputs)

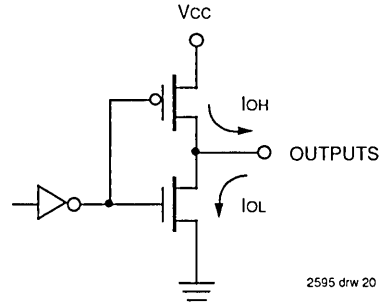
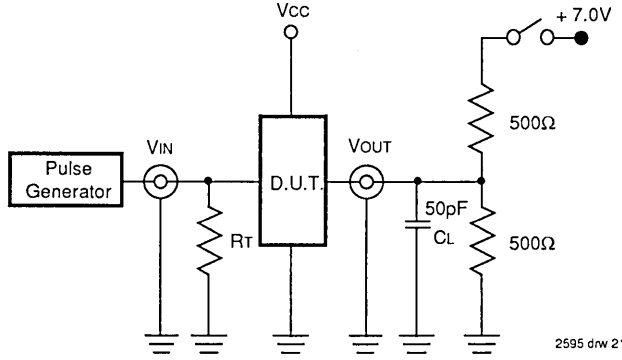


Figure 11. Output Structure

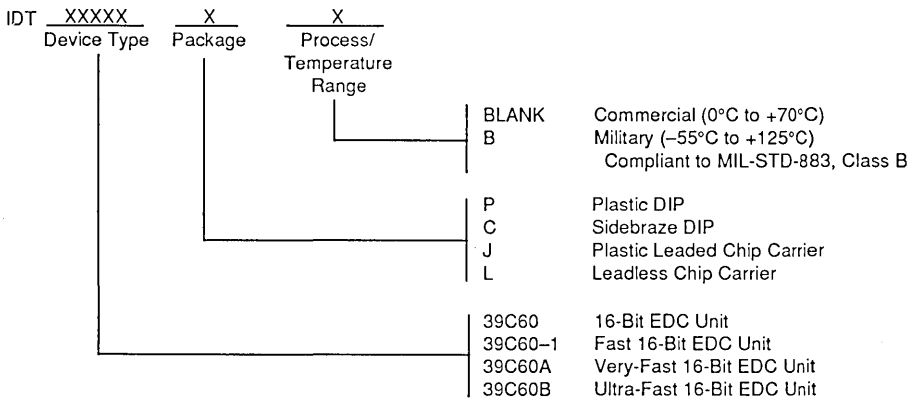
TEST CIRCUIT LOAD



DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance
RL = Termination resistance: should be equal to ZOUT of the Pulse Generator

Figure 12.

ORDERING INFORMATION



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5

Integrated Device Technology, Inc.

32-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT49C460
IDT49C460A
IDT49C460B
IDT49C460C
IDT49C460D

FEATURES:

- Fast

	Detect	Correct
— IDT49C460D	12ns (max.)	18ns (max.)
— IDT49C460C	16ns (max.)	24ns (max.)
— IDT49C460B	25ns (max.)	30ns (max.)
— IDT49C460A	30ns (max.)	36ns (max.)
— IDT49C460	40ns (max.)	49ns (max.)

- Low-power CMOS
  - — Commercial: 95mA (max.)
  - — Military: 125mA (max.)
- Improves system memory reliability
  - — Corrects all single bit errors, detects all double and some triple-bit errors
- Cascadable
  - — Data words up to 64-bits
- Built-in diagnostics
  - — Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - — Fast byte writes possible with separate byte enables
- Functional replacement for 32- and 64-bit configurations of the 2960
- Available in PGA, PLCC and Ceramic Flatpack
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962–88533

DESCRIPTION:

The IDT49C460s are high-speed, low-power, 32-bit Error Detection and Correction Units which generate check bits on a 32-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. The IDT49C460s are performance-enhanced functional replacements for 32-bit versions of the 2960. When performing a read operation from memory, the IDT49C460s will correct 100% of all single bit errors and will detect all double bit errors and some triple bit errors.

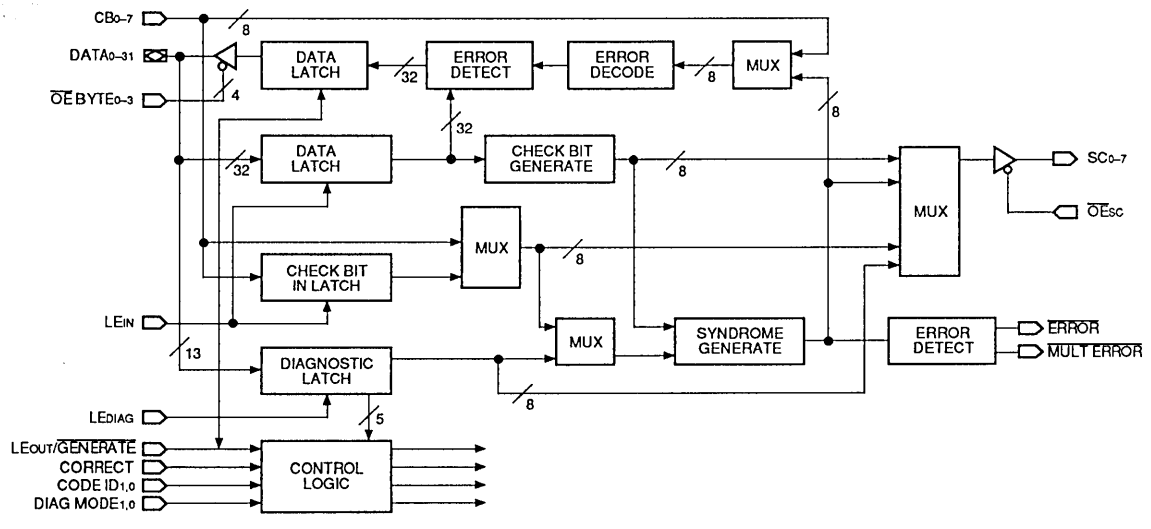
The IDT49C460s are easily cascadable to 64-bits. Thirty-two-bit systems use 7 check bits and 64-bit systems use 8 check bits. For both configurations, the error syndrome is made available.

The IDT49C460s incorporate two built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostics functions.

They are fabricated using CEMOS™, a CMOS technology designed for high-performance and high-reliability. The devices are packaged in a 68-pin ceramic PGA, PLCC and Ceramic Flatpack.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

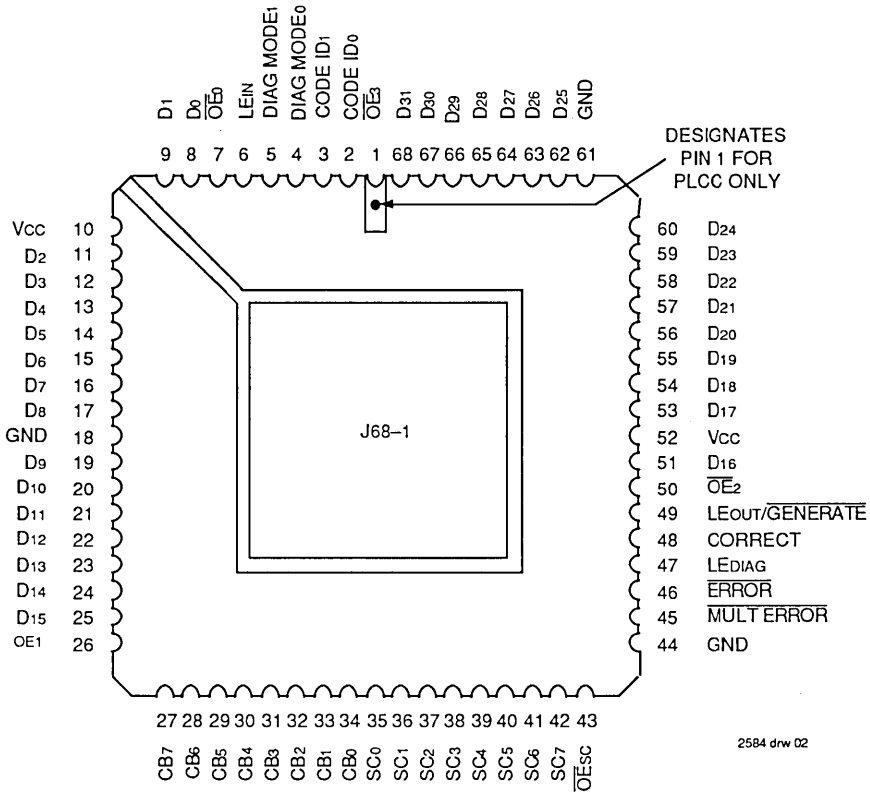
FUNCTIONAL BLOCK DIAGRAM



2584 drw 01

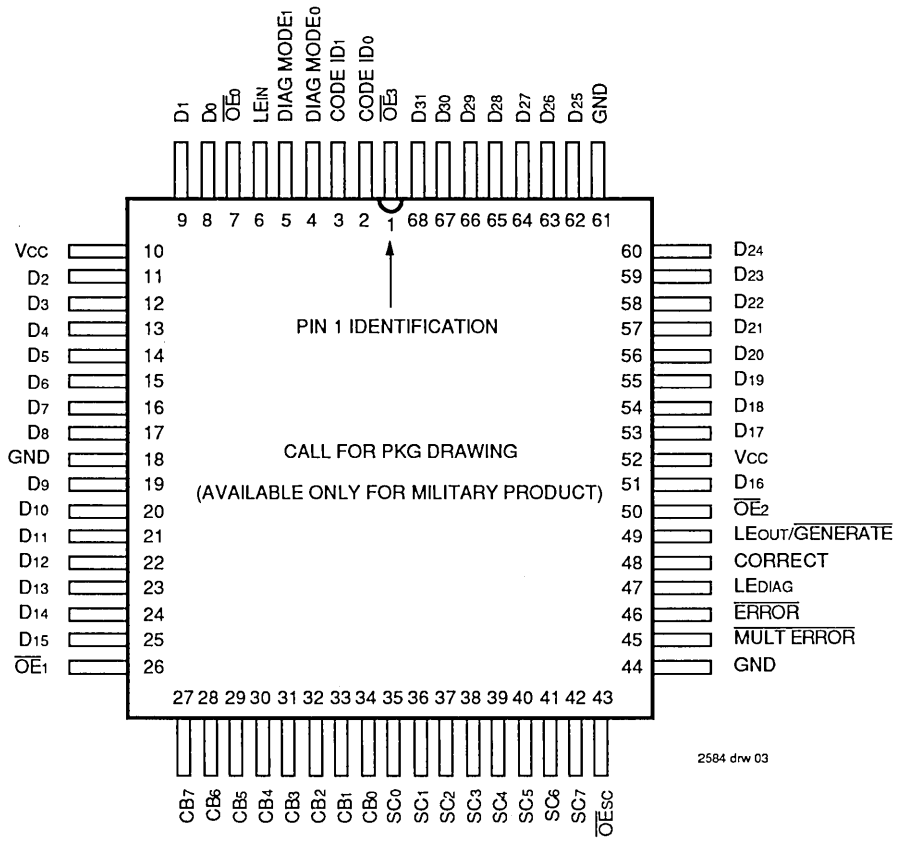
CEMOS is a trademark of Integrated Device Technology Inc.

PIN CONFIGURATION

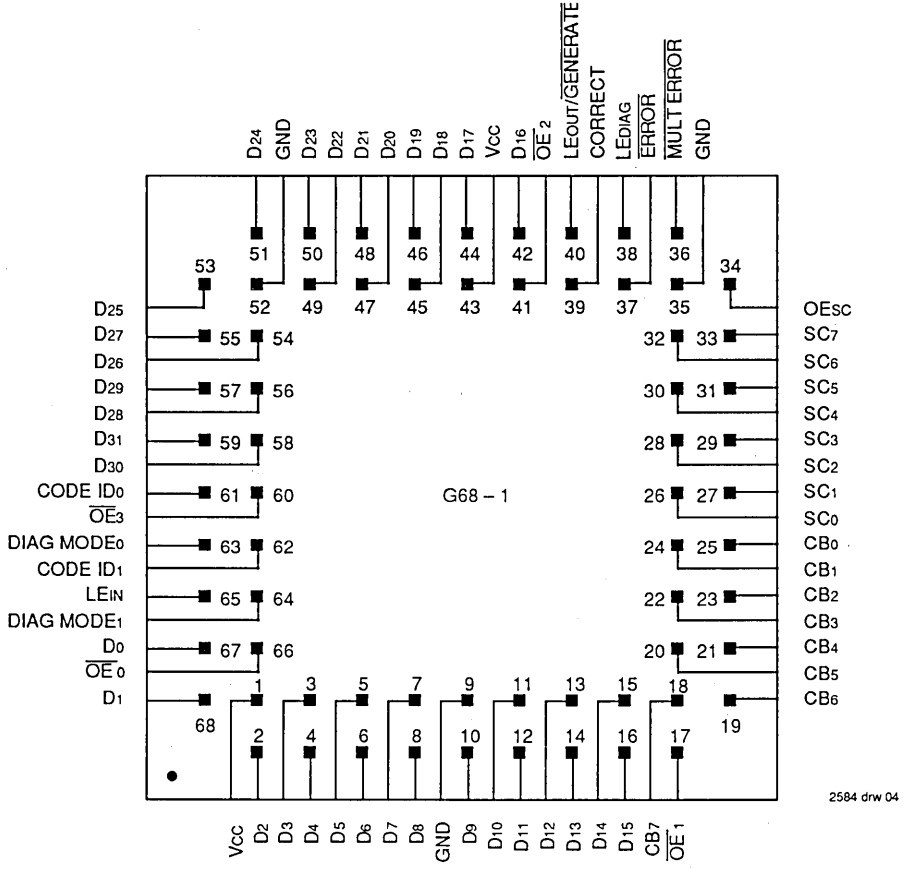


PLCC
TOPVIEW

5



FLATPACK
TOPVIEW



PGA
TOPVIEW

5

PIN DESCRIPTIONS

Pin Name	I/O	Description
$DATA_{0-31}$	I/O	32 bidirectional data lines provide input to the Data Input Latch and Diagnostic Latch and also receive output from the Data Output Latch. $DATA_0$ is the LSB; $DATA_{31}$ is the MSB.
CB_{0-7}	I	Eight check bit input lines input check bits for error detection and also used to input syndrome bits for error correction in 64-bit applications.
LE_{IN}	I	Latch Enable is for the Data Input Latch. Controls latching of the input data. Data Input Latch and Check Bit Input Latch are latched to their previous state when LOW. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits.
LE_{OUT}/ $\overline{GENERATE}$		A multifunction pin which, when LOW, is in the Check Bit Generate Mode. In this mode, the device generates the check bits or GENERATE partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. Also, when LOW, the Data Out Latch is latched to its previous state. When HIGH, the device is in the Detect or Correct Mode. In this mode, the device detects single and multiple errors and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In the Correct Mode, single bit errors are also automatically corrected and the corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the specific bit-in-error. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single bit errors are corrected by the network before being loaded into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The Data Output Latch is disabled, with its contents unchanged, if the EDC is in the Generate Mode.
SC_{0-7}	O	Syndrome Check Bit outputs. Eight outputs which hold the check bits and partial check bits when the EDC is in the Generate Mode and will hold the syndrome/partial syndrome bits when the device is in the Detect or Correct modes. All are 3-state outputs.
$\overline{OE_{SC}}$	I	Output Enable—Syndrome Check Bits. In the HIGH condition, the SC outputs are in the high impedance state. When LOW, all SC output lines are enabled.
$\overline{ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if one or more data or check bits contain an error. When HIGH, no errors have been detected. This pin is forced HIGH in the Generate Mode.
$\overline{MULT}$ $\overline{ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if two or more bit errors have been detected. A HIGH level indicates that either one or no errors have been detected. This pin is forced HIGH in the Generate Mode.
CORRECT	I	The correct input which, when HIGH, allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the device will drive data directly from the Data Input Latch to the Data Output Latch without correction.
$\overline{OE}$ $BYTE_{0-3}$	I	Output Enable—Bytes 0, 1, 2, 3. Data Output Latch. Control the three-state output buffers for each of the four bytes of the Data Output Latch. When LOW, they enable the output buffer of the Data Output Latch. When HIGH, they force the Data Output Latch buffer into the high impedance mode. One byte of the Data Output Latch is easily activated by separately selecting the four enable lines.
DIAG $MODE_{1,0}$	I	Select the proper diagnostic mode. They control the initialization, diagnostic and normal operation of the EDC.
CODE $ID_{1,0}$	I	These two code identification inputs identify the size of the total data word to be processed. The two allowable data word sizes are 32 and 64 bits and their respective modified Hamming Codes are designated 32/39 and 64/72. Special CODE $ID_{1,0}$, input 01 is also used to instruct the EDC that the signals CODE $ID_{1,0}$, DIAG $MODE_{1,0}$ and CORRECT are to be taken from the Diagnostic Latch rather than from the input control lines.
LE_{DIAG}	I	This is the Latch Enable for the Diagnostic Latch. When HIGH, the Diagnostic Latch follows the 32-bit data on the input lines. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for CODE $ID_{1,0}$, DIAG $MODE_{1,0}$ and CORRECT.

2584 tbl 01

EDC ARCHITECTURE SUMMARY

The IDT49C460s are high-performance cascadable EDCs used for check bit generation, error detection, error correction and diagnostics. The function blocks for this 32-bit device consist of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

DATA INPUT/OUTPUT LATCH

The Latch Enable Input, LE_{IN}, controls the loading of 32 bits of data to the Data In Latch. The data from the DATA lines can be loaded in the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in another byte. The Diagnostic Latch is used in the Internal Control Mode or in one of the diagnostic modes. The Data Output Latch has buffers that place data on the DATA lines. These buffers are split into four 8-bit buffers, each having their own output enable controls. This feature facilitates byte read and byte modify operations.

CHECK BIT GENERATION LOGIC

This generates the appropriate check bits for the 32 bits of data in the Data Input Latch. The modified Hamming Code is the basis for generating the proper check bits.

SYNDROME GENERATION LOGIC

In both the Detect and Correct modes, this logic does a comparison on the check bits read from memory against the newly generated set of check bits produced for the data read in from memory. Matching sets of check bits mean no error was detected. If there is a mismatch, one or more of the data or check bits is in error. Syndrome bits are produced by an exclusive-OR of the two sets of check bits. Identical sets of check bits mean the syndrome bits will be all zeros. If an error results, the syndrome bits can be decoded to determine the number of errors and the specific bit-in-error.

ERROR DETECTION LOGIC

This part of the device decodes the syndrome bits generated by the Syndrome Generation Logic. With no errors in either the input data or check bits, both the $\overline{\text{ERROR}}$ and $\overline{\text{MULTERROR}}$ outputs are HIGH. $\overline{\text{ERROR}}$ will go low if one error is detected. $\overline{\text{MULTERROR}}$ and $\overline{\text{ERROR}}$ will both go low if two or more errors are detected.

ERROR CORRECTION LOGIC

In single error cases, this logic complements (corrects) the single data bit-in-error. This corrected data is loaded into the Data Output Latch, which can then be read onto the bidirectional data lines. If the error is resulting from one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed, the EDC must be switched to the Generate Mode.

DATA OUTPUT LATCH AND OUTPUT BUFFERS

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE_{OUT}. The Data Output Latch may also be directly loaded from the Data Input Latch in the PASSTHRU mode. The Data Output Latch buffer is split into 4 individual buffers which can be enabled by $\overline{OE}_{0-3}$ separately for reading onto the bidirectional data lines.

DIAGNOSTIC LATCH

The diagnostic latch is loadable under control of the Diagnostic Latch Enable, LE_{DIAG}, from the bidirectional data lines. Check bit information is contained in one byte while the other byte contains the control information. The Diagnostic Latch is used for driving the device when in the Internal Control Mode, or for supplying check bits when in one of the diagnostic modes.

CONTROL LOGIC

Specifies in which mode the device will be operating in. Normal operation is when the control logic is driven by external control inputs. In the Internal Control Mode, the control signals are read from the Diagnostic Latch. Since LE_{OUT} and $\overline{\text{GENERATE}}$ are controlled by the same pin, the latching action (LE_{OUT} from high to low) of the Data Output Latch causes the EDC to go into the Generate Mode.

5

DETAILED PRODUCT DESCRIPTION

The IDT49C460 EDC units contain the logic necessary to generate check bits on 32 bits of data input according to a modified Hamming Code. The EDC can compare internally generated check bits against those read with the 32-bit data to allow correction of any single bit data error and detection of all double (and some triple) bit errors. The IDT49C460s can be used for 32-bit data words (7 check bits) and 64-bit (8 check bits) data words.

WORD SIZE SELECTION

The two code identification pins, CODE $ID_{1,0}$, are used to determine the data word size that is 32 or 64 bits. They also select the Internal Control Mode. Table 5 defines all possible slice identification codes.

CHECK AND SYNDROME BITS

The IDT49C460s provide either check bits or syndrome bits on the three-state output pins, SC_{0-7}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an exclusive-OR of the check bits generated from read data with the read check bits stored with the data. Syndrome bits can be decoded to determine the single bit in error or that a double (some triple) error was detected. The check bits are labeled:

$C_0, C_1, C_2, C_3, C_4, C_5, C_6$ for the 32-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$ for the 64-bit configuration

Syndrome bits are similarly labeled S_0 through S_7.

Correct	Diag $Mode_1$	Diag $Mode_2$	Diagnostic Mode Selected
X	0	0	**Non-diagnostic Mode.** Normal EDC function in this mode.
X	0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes.
X	1	0	**Diagnostic Detect/Correct.** In either mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	1	**Initialize.** The Data Input Latch outputs are forced to zeros and latched upon removal of Initialize Mode.
0	1	1	**PASSTHRU.**

2584 tbl 02

Table 2. Diagnostic Mode Control

Operating Mode	DM_1	DM_2	Generate	Correct	$DATA_{OUT}$ Latch	SC_{0-7} ($\overline{OE}_{SC}$ = LOW)	$\overline{ERROR}$ / $\overline{MULT\ ERROR}$
Generate	0 1	0 0	0	X	LE_{OUT} = LOW (1)	Check Bits Generated from $DATA_{IN}$ Latch	High
Detect	0 0	0 1	1	0	$DATA_{IN}$ Latch	Syndrome Bits $DATA_{IN}$/ Check Bit Latch	Error Dep (2)
Correct	0 0	0 1	1	1	$DATA_{IN}$ Latch w/ Single Bit Correction	Syndrome Bits $DATA_{IN}$/ Check Bit Latch	Error Dep
PASSTHRU	1	1	1	0	$DATA_{IN}$ Latch	Check Bit Latch	High
Diagnostic Generate	0	1	0	X	—	Check Bits from Diagnostic Latch	High
Diagnostic Detect	1	0	1	0	$DATA_{IN}$ Latch	Syndrome Bits $DATA_{IN}$/ Diagnostic Latch	Error Dep
Diagnostic Correct	1	0	1	1	$DATA_{IN}$ Latch w/ Single Bit Correction	Syndrome Bits $DATA_{IN}$/ Diagnostic Latch	Error Dep
Initialization	1	1	1	1	$DATA_{IN}$ Latch Set to 0000 (3)	—	—
Internal	CODE $ID_{1,0}$ = 01 (Control Signals CODE $ID_{1,0}$, DIAG $MODE_{1,0}$ and CORRECT are taken from Diagnostic Latch.)						

NOTES: 2584 tbl 03

1. In Generate Mode, data is read into the EDC unit and the check bits are generated. The same data is written to memory along with the check bits. Since the $DATA_{OUT}$ Latch is not used in the Generate Mode, LE_{OUT} (being LOW since it is tied to Generate) does not affect the writing of check bits.
2. Error Dep (Error Dependent): $\overline{ERROR}$ will be low for single or multiple errors, with $\overline{MULT\ ERROR}$ low for double or multiple errors. Both signals are high for no errors.
3. LE_{IN} is LOW.

Table 3. IDT49C460 Operating Modes

OPERATING MODE SELECTION

Tables 2 and 3 describe the nine operating modes of the IDT49C460s. The Diagnostic Mode pins — DIAG MODE$_{0,1}$ — define four basic areas of operation. $\overline{\text{GENERATE}}$ and CORRECT further divide operation into 8 functions, with CODE ID$_{1,0}$ defining the ninth mode as the Internal Mode.

Generate Mode is used to display the check bits on the outputs SC$_{0-7}$. The Diagnostic Generate Mode displays check bits as stored in the Diagnostic Latch.

Detect Mode provides an indication of errors or multiple errors on the outputs $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC$_{0-7}$. For the Diagnostic Detect Mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct Mode is similar to the Detect Mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latches. Again, the Diagnostic Correct Mode will correct single bit errors as determined by syndrome bits generated from the data input and contents of the diagnostic latches.

The Initialize Mode provides check bits for all zero bit data. Data Input Latches are set, latched to a logic zero and made available as input to the Data Out Latches.

The Internal Mode disables the external control pins DIAG MODE$_{0,1}$ and CORRECT to be defined by the Diagnostic Latch. Even CODE ID$_{1,0}$, although externally set to the 01 code, can be redefined from the Diagnostic Latch data.

Code ID$_1$	Code ID$_0$	Slice Selected
0	0	32-Bit
0	1	Internal Control Mode
1	0	64-Bit, Lower 32-Bit (0–31)
1	1	64-Bit, Upper 32-Bit (32–63)

2584 tbl 04

Table 5. Slice Identification

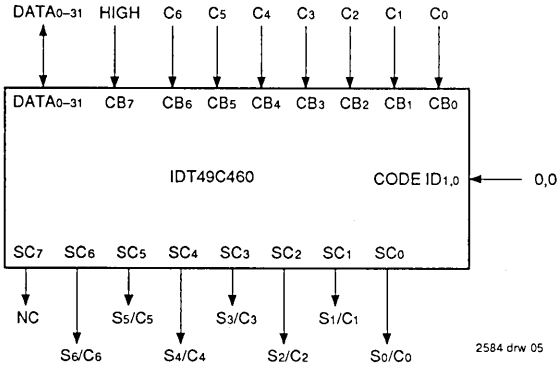


Figure 1. 32-Bit Configuration

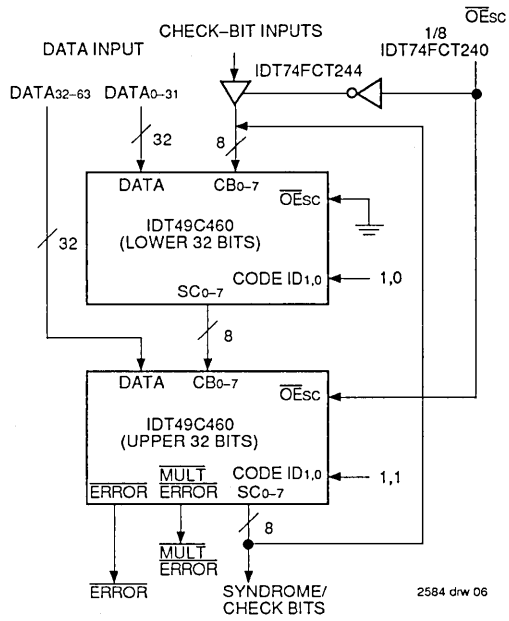


Figure 2. 64-Bit Configuration

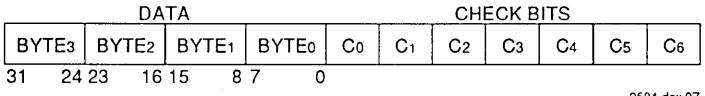


Figure 3. 32-Bit Data Format

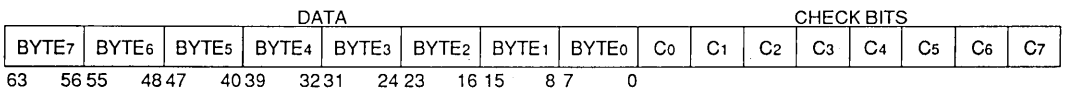


Figure 4. 64-Bit Data Format

32-BIT DATA WORD CONFIGURATION

A single IDT49C460 EDC unit, connected as shown in Figure 1, provides all the logic needed for single bit error correction and double bit error detection of a 32-bit data field. The identification code indicates 7 check bits are required. The CB7 pin should be HIGH.

Figure 3 indicates the 39-bit data format for two bytes of data and 7 check bits. Table 3 describes the operating mode available.

Table 6 indicates the data bits participating in the check bit generation. For example, check bit C_0 is the exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits from the respective latch are passed, unchanged, in the PASSTHRU or Diagnostic Generate Mode.

Syndrome bits are generated by an exclusive-OR or the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 7 indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single bit error, or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 4 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

BIT 0	CB_0 DIAGNOSTIC
BIT 1	CB_1 DIAGNOSTIC
BIT 2	CB_2 DIAGNOSTIC
BIT 3	CB_3 DIAGNOSTIC
BIT 4	CB_4 DIAGNOSTIC
BIT 5	CB_5 DIAGNOSTIC
BIT 6	CB_6 DIAGNOSTIC
BIT 7	CB_7 DIAGNOSTIC
BIT 8	CODE ID_0
BIT 9	CODE ID_1
BIT 10	DIAG $MODE_0$
BIT 11	DIAG $MODE_1$
BIT 12	CORRECT
BIT 13–31	DON'T CARE

2584 drw 05

Table 4. 32-Bit Diagnostic Latch Coding Format

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)	X				X		X	X	X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								

2584 tbl 06

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X					X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X

2584 tbl 07

Table 6. 32–Bit Modified Hamming Code–Check Bit Encode Chart

Hex	Syndrome Bits S3	S2	S1	S0	Hex	0	1	2	3	4	5	6	7
					S6	0	0	0	0	1	1	1	1
					S5	0	0	1	1	0	0	1	1
					S4	0	1	0	1	0	1	0	1
0	0	0	0	0		*	C4	C5	T	C6	T	T	30
1	0	0	0	1		C0	T	T	14	T	M	M	T
2	0	0	1	0		C1	T	T	M	T	2	24	T
3	0	0	1	1		T	18	8	T	M	T	T	M
4	0	1	0	0		C2	T	T	15	T	3	25	T
5	0	1	0	1		T	19	9	T	M	T	T	31
6	0	1	1	0		T	20	10	T	M	T	T	M
7	0	1	1	1		M	T	T	M	T	4	26	T
8	1	0	0	0		C3	T	T	M	T	5	27	T
9	1	0	0	1		T	21	11	T	M	T	T	M
A	1	0	1	0		T	22	12	T	1	T	T	M
B	1	0	1	1		17	T	T	M	T	6	28	T
C	1	1	0	0		T	23	13	T	M	T	T	M
D	1	1	0	1		M	T	T	M	T	7	29	T
E	1	1	1	0		16	T	T	M	T	M	M	T
F	1	1	1	1		T	M	M	T	0	T	T	M

NOTES:
1. * = No errors detected
2. Number = The number of the single bit-in-error
3. T = Two errors detected
4. M = Three or more errors detected

2584 tbl 08

Table 7. Syndrome Decode to Bit-in-Error (32-Bit)

64-BIT DATA WORD CONFIGURATION

Two IDT49C460 EDC units, connected as shown in Figure 2, provide all the logic needed for single bit error detection and double bit error detection of a 64-bit data field. Table 5 gives the CODE $ID_{1,0}$ values needed for distinguishing the upper 32 bits from the lower 32 bits. Valid syndrome, check bits and the $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ signals come from the IC with the CODE $ID_{1,0}$ = 11. Control signals not indicated are connected to both units in parallel. The EDC with the CODE $ID_{1,0}$ = 10 has the $\overline{OE}_{SC}$ grounded. The $\overline{OE}_{SC}$ selects the syndrome bits from the EDC with CODE $ID_{1,0}$ = 11 and also controls the check bit buffers from memory.

Data In bits 0 through 31 are connected to the same numbered inputs of the EDC unit with CODE $ID_{1,0}$ = 10, while Data In bits 32 through 63 are connected to Data Inputs 0 to 31, respectively, for the EDC unit with CODE $ID_{1,0}$ = 11.

Figure 4 indicates the 72-bit data format of 8 bytes of data and 8 check bits. Check bits are input to the EDC unit with CODE $ID_{1,0}$ = 10 through a three-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits from the upper EDC unit to the lower EDC unit. The MUX shown on the functional block diagram is used to select the CB_{0-7} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 64/72 configuration.

Table 11 indicates the data bits participating in the check bit generation. For example, check bit Co is the exclusive-OR function of the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization modes. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate modes.

Syndrome bits are generated by an exclusive-OR of the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 9 indicates the decoding of the 8 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Tables 8A and 8B define the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic Check Bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Performance data is provided in Table 10, relating a single IDT49C460 EDC with the two cascaded units of Figure 2. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

Bit	Internal Function
0	CB_0 DIAGNOSTIC
1	CB_1 DIAGNOSTIC
2	CB_2 DIAGNOSTIC
3	CB_3 DIAGNOSTIC
4	CB_4 DIAGNOSTIC
5	CB_5 DIAGNOSTIC
6	CB_6 DIAGNOSTIC
7	CB_7 DIAGNOSTIC
8	CODE ID_0 LOWER 32-BIT
9	CODE ID_1 LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13–31	DON'T CARE
32–39	DON'T CARE
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45–63	DON'T CARE

2584 tbl 09

Table 8A. 64-Bit Diagnostic Latch–Coding Format (Diagnostic and Correct Mode)

5

Bit	Internal Function
0–7	DON'T CARE
8	CODE ID_0 LOWER 32-BIT
9	CODE ID_1 LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13–31	DON'T CARE
32	CB_0 DIAGNOSTIC
33	CB_1 DIAGNOSTIC
34	CB_2 DIAGNOSTIC
35	CB_3 DIAGNOSTIC
36	CB_4 DIAGNOSTIC
37	CB_5 DIAGNOSTIC
38	CB_6 DIAGNOSTIC
39	CB_7 DIAGNOSTIC
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45–63	DON'T CARE

2584 tbl 10

Table 8B. 64-Bit Diagnostic Latch–Coding Format (Diagnostic and Correct Mode)

					Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
					S_7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Syndrome Bits				S_6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Hex	S_3	S_2	S_1	S_0																	
0	0	0	0	0		*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1		C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0		C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1		T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0		C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1		T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0		T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1		M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0		C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1		T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0		T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1		17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0		T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1		M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0		16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1		T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

2584 tbl 11

Table 9. Syndrome Decode to Bit–In–Error (64–Bit Configuration)

64–Bit Propagation Delay		Component Delay for IDT49C460 AC Specifications
From	To	
DATA	Check Bits Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	Corrected DATA$_{OUT}$	(DATA TO SC) + (CB TO SC, CODE ID 11) + (CB TO DATA, CODE ID 10)
DATA	Syndromes Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	$\overline{\text{ERROR}}$ for 64 Bits	(DATA TO SC) + (CB TO $\overline{\text{ERROR}}$, CODE ID 11)
DATA	$\overline{\text{MULT ERROR}}$ for 64 Bits	(DATA TO SC) + (CB TO $\overline{\text{MULT ERROR}}$, CODE ID 11)

2584 tbl 12

Table 10. Key Calculations for the 64–Bit Configuration

5

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

2584 tbl 13

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)									X	X	X	X	X	X	X	X

2584 tbl 14

Generated Check Bits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)									X	X	X	X	X	X	X	X

2584 tbl 15

Generated Check Bits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

NOTE:
1. The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

2584 tbl 16

Table 11. 64-Bit Modified Hamming Code–Check Bit Encoding

SC OUTPUTS

The tables below indicate how the SC0–7 outputs are generated in each control mode of various CODE IDs (Internal Control Mode not applicable).

Generate	CODE ID1,0		
	00	10	11
SC0 ←	PH0	PH1	PH2 ⊕ CB0
SC1 ←	PA	PA	PA ⊕ CB1
SC2 ←	PB	PB	PB ⊕ CB2
SC3 ←	PC	PC	PC ⊕ CB3
SC4 ←	PD	PD	PD ⊕ CB4
SC5 ←	PE	PE	PE ⊕ CB5
SC6 ←	PF	PF	PF ⊕ CB6
SC7 ←	—	PF	PG ⊕ CB7
	Final Check Bits	Partialß Check Bits	Final Check Bits

2584 tbl 17

Correct/ Detect	CODE ID1,0		
	00	10	11
SC0 ←	PH0 ⊕ C0	PH1 ⊕ C0	PH2 ⊕ CB0
SC1 ←	PA ⊕ C1	PA ⊕ C1	PA ⊕ CB1
SC2 ←	PB ⊕ C2	PB ⊕ C2	PB ⊕ CB2
SC3 ←	PC ⊕ C3	PC ⊕ C3	PC ⊕ CB3
SC4 ←	PD ⊕ C4	PD ⊕ C4	PD ⊕ CB4
SC5 ←	PE ⊕ C5	PE ⊕ C5	PE ⊕ CB5
SC6 ←	PF ⊕ C6	PF ⊕ C6	PF ⊕ CB6
SC7 ←	—	PF ⊕ C7	PG ⊕ CB7
	Final Syndrome	Partial Syndrome	Final Syndrome

2584 tbl 19

Diagnostic Generate	CODE ID1,0		
	00	10	11
SC0 ←	DL0	DL0	DL32
SC1 ←	DL1	DL1	DL33
SC2 ←	DL2	DL2	DL34
SC3 ←	DL3	DL3	DL35
SC4 ←	DL4	DL4	DL36
SC5 ←	DL5	DL5	DL37
SC6 ←	DL6	DL6	DL38
SC7 ←	—	DL7	DL39
	Final Check Bits	Partial Check Bits	Final Check Bits

2584 tbl 18

Diagnostic Correct/ Detect	CODE ID1,0		
	00	10	11
SC0 ←	PH0 ⊕ DL0	PH1 ⊕ DL0	PH2 ⊕ CB0
SC1 ←	PA ⊕ DL1	PA ⊕ DL1	PA ⊕ CB1
SC2 ←	PB ⊕ DL2	PB ⊕ DL2	PB ⊕ CB2
SC3 ←	PC ⊕ DL3	PC ⊕ DL3	PC ⊕ CB3
SC4 ←	PD ⊕ DL4	PD ⊕ DL4	PD ⊕ CB4
SC5 ←	PE ⊕ DL5	PE ⊕ DL5	PE ⊕ CB5
SC6 ←	PF ⊕ DL6	PF ⊕ DL6	PF ⊕ CB6
SC7 ←	—	PF ⊕ DL7	PG ⊕ CB7
	Final Syndrome	Partial Syndrome	Final Syndrome

2584 tbl 20

PASSTHRU	CODE ID1,0		
	00	10	11
SC0 ←	C0	C0	CB0
SC1 ←	C1	C1	CB1
SC2 ←	C2	C2	CB2
SC3 ←	C3	C3	CB3
SC4 ←	C4	C4	CB4
SC5 ←	C5	C5	CB5
SC6 ←	C6	C6	CB6
SC7 ←	—	C7	CB7

2584 tbl 21

5

DATA CORRECTION

The tables below indicate which data output bits are corrected depending upon the syndromes and the CODE $ID_{1,0}$ position. The syndromes that determine data correction are, in some cases, syndromes input externally via the CB inputs and, in some cases, syndromes input externally by that EDC (S_i are the internal syndromes and are the same as the value of the SC_i output of that EDC if enabled).

SYNDROME DECODE TO BIT CORRECTED (32-BIT CONFIGURATION) CODE ID_{1-0} = 00

					Hex	0	1	2	3	4	5	6	7
	Syndrome Bits				S_6	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1
Hex	S_3	S_2	S_1	S_0									
0	0	0	0	0		–	–	–	–	–	–	–	30
1	0	0	0	1		–	–	–	14	–	–	–	–
2	0	0	1	0		–	–	–	–	–	2	24	–
3	0	0	1	1		–	18	8	–	–	–	–	–
4	0	1	0	0		–	–	–	15	–	3	25	–
5	0	1	0	1		–	19	9	–	–	–	–	31
6	0	1	1	0		–	20	10	–	–	–	–	–
7	0	1	1	1		–	–	–	–	–	4	26	–
8	1	0	0	0		–	–	–	–	–	5	27	–
9	1	0	0	1		–	21	11	–	–	–	–	–
A	1	0	1	0		–	22	12	–	1	–	–	–
B	1	0	1	1		17	–	–	–	–	6	28	–
C	1	1	0	0		–	23	13	–	–	–	–	–
D	1	1	0	1		–	–	–	–	–	7	29	–
E	1	1	1	0		16	–	–	–	–	–	–	–
F	1	1	1	1		–	–	–	–	0	–	–	–

NOTE:
1. S_7 = 1 in CODE $ID_{1,0}$ = 00

2584 tbl 22

FUNCTIONAL EQUATIONS

The equations below describe the IDT49C460 output values as defined by the value of the inputs and internal states.

DEFINITIONS

$PA = D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{20} \oplus D_{22} \oplus D_{24} \oplus D_{26} \oplus D_{28}$

$PB = D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{19} \oplus D_{20} \oplus D_{23} \oplus D_{25} \oplus D_{26} \oplus D_{29} \oplus D_{31}$

$PC = D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{16} \oplus D_{17} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{27} \oplus D_{28} \oplus D_{29}$

$PD = D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{14} \oplus D_{15} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{30} \oplus D_{31}$

$PE = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$

$PF = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$

$PG = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23}$

$PH0 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$

$PH1 = D_1 \oplus D_2 \oplus D_3 \oplus D_5 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{24} \oplus D_{25} \oplus D_{27} \oplus D_{30}$

$PH2 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{20} \oplus D_{22} \oplus D_{23} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$

SYNDROME DECODE TO BIT CORRECTED (64–BIT CONFIGURATION)

					Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
					S_7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Syndrome Bits				S_6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Hex	S_3	S_2	S_1	S_0																	
0	0	0	0	0		*	C4	C5	–	C6	–	–	62	C7	–	–	46	–	–	–	–
1	0	0	0	1		C0	–	–	14	–	–	–	–	–	–	–	–	–	–	–	30
2	0	0	1	0		C1	–	–	–	–	34	56	–	–	50	40	–	–	–	–	–
3	0	0	1	1		–	18	8	–	–	–	–	–	–	–	–	–	–	2	24	–
4	0	1	0	0		C2	–	–	15	–	35	57	–	–	51	41	–	–	–	–	31
5	0	1	0	1		–	19	9	–	–	–	–	63	–	–	–	47	–	3	25	–
6	0	1	1	0		–	20	10	–	–	–	–	–	–	–	–	–	–	4	26	–
7	0	1	1	1		–	–	–	–	–	36	58	–	–	52	42	–	–	–	–	–
8	1	0	0	0		C3	–	–	–	–	37	59	–	–	53	43	–	–	–	–	–
9	1	0	0	1		–	21	11	–	–	–	–	–	–	–	–	–	–	5	27	–
A	1	0	1	0		–	22	12	–	33	–	–	–	49	–	–	–	–	6	28	–
B	1	0	1	1		17	–	–	–	–	38	60	–	–	54	44	–	1	–	–	–
C	1	1	0	0		–	23	13	–	–	–	–	–	–	–	–	–	–	7	29	–
D	1	1	0	1		–	–	–	–	–	39	61	–	–	55	45	–	–	–	–	–
E	1	1	1	0		16	–	–	–	–	–	–	–	–	–	–	–	0	–	–	–
F	1	1	1	1		–	–	–	–	32	–	–	–	48	–	–	–	–	–	–	–

2584 tbl 23

5

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to V_{CC} + 0.5V	−0.5 to V_{CC} + 0.5V	V
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
I_{OUT}	DC Output Current	30	30	mA

NOTE: 2584 tbl 24

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = + 25°C, f = 1.0MHz)

Symbol	Parameter [1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2584 tbl 25

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} − 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions [1]		Min.	Typ. [2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	0.1	10.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	−0.1	−10.0	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = 300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = −12mA Mil.	2.4	4.3	—	
			I_{OH} = −15mA Com'l.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 12mA Mil.	—	0.3	0.5	
			I_{OL} = 16mA Com'l.	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	—	−0.1	−20.0	µA
			V_O = V_{CC} (Max.)	—	0.1	20.0	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V [3]		−30.0	—	—	mA

NOTES: 2584 tbl 26

1. For conditions shown as Max. or Min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, + 25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd.)

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = VCC – 0.2V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max.; All Inputs $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{OP} = 0; Outputs Disabled		—	3.0	10	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High) (5)	V_{CC} = Max., V_{IN} = 3.4V, f_{OP} = 0		—	0.3	0.75	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max.	MIL.	—	6	10	mA/ MHz
		$V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	COM'L.	—	6	7	
I_{CC}	Total Power Supply Current (6)	V_{CC} = Max., f_{OP} = 10MHz	MIL.	—	60	110	mA
		Outputs Open, $\overline{OE}$ = L 50 % Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	COM'L.	—	60	80	
		V_{CC} = Max., f_{OP} = 10MHz	MIL.	—	70	125	
		Outputs Open, $\overline{OE}$ = L 50 % Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	COM'L.	—	70	95	

NOTES:

2584 tbl 27

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   $I_{CC} = I_{CCQ} + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{OP})$
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
   N_T = Number of dynamic inputs driven at TTL levels.
   f_{OP} = Operating frequency in Megahertz.

5

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.

IDT49C460D AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, V_{CC} = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
	$DATA_{0-31}$		14	18 [2]	12	15	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 00, 11)		11	16	10	12	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 10)		12	12	—	—	ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	9	↓ 7	↓ 8	ns
		↓	14	—	↑ 7	↑ 8	ns
	CORRECT Not Internal Control Mode		—	12	—	—	ns
	DIAG MODE Not Internal Control Mode		12	20	10	15	ns
	CODE $ID_{1,0}$		14 [6]	18	13	16	ns
	LE_{IN} From latched to Transparent		17	21	14	17	ns
	LE_{DIAG} From latched to Transparent	↑	12 [6]	18	12	14	ns
Internal Control Mode	LE_{DIAG} From latched to Transparent	↑	12 [6]	17	12	14	ns
	$DATA_{0-31}$ Via Diagnostic Latch	↑	12	19 [2]	10	12	ns

2584 tbl 28

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$ [4]		↓	LE_{IN}	3	3	ns
CB_{0-7} [4]		↓	LE_{IN}	2	3	ns
$DATA_{0-31}$ [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	5 [15]	0	ns
CB_{0-7} (CODE ID 00, 11) [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	11	0	ns
CB_{0-7} (CODE ID 10) [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	6	0	ns
CORRECT [4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	6	0	ns
DIAG MODE [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	13	0	ns
$CODE\ ID_{1,0}$ [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	8	0	ns
LE_{IN} [4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	14	0	ns
$DATA_{0-31}$ [4, 6]			LE_{DIAG}	3	3	ns

NOTE: (15) above applies to correction path. 2584 tbl 29

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE\ Byte_{0-3}}$	↓	↑	$DATA_{0-31}$	0	8	0	10	ns
$\overline{OE_{SC}}$	↓	↑	SC_{0-7}	0	8	0	10	ns

2584 tbl 30

MINIMUM PULSE WIDTHS[6]

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive–going pulse)	5		ns

NOTES: 2584 tbl 31
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

IDT49C460D AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, V_{CC} = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULTERROR}$	Unit
	$DATA_{0-31}$		17	22 [2]	16	18	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 00, 11)		13	17	12	14	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 10)		13	14	—	—	ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	10	↓ 8	↓ 8	ns
		↓	15	—	↑ 8	↑ 9	ns
	CORRECT Not Internal Control Mode		—	13	—	—	ns
	DIAG MODE Not Internal Control Mode		14	22	12	17	ns
	CODE $ID_{1,0}$		16 [6]	20	15	18	ns
	LE_{IN} From latched to Transparent		18	24	16	19	ns
	LE_{DIAG} From latched to Transparent	↑	14 [6]	20	13	16	ns
Internal Control Mode	LE_{DIAG} From latched to Transparent	↑	14 [6]	19	14	16	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch	↑	14	22 [2]	11	14	ns

2584 tbl 32

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$ [4]		↓	LE_{IN}	3	3	ns
CB_{0-7} [4]		↓	LE_{IN}	2	3	ns
$DATA_{0-31}$ [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	6 [15]	0	ns
CB_{0-7} (CODE ID 00, 11) [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	12	0	ns
CB_{0-7} (CODE ID 10) [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	8	0	ns
CORRECT [4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	7	0	ns
DIAG MODE [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	14	0	ns
CODE $ID_{1,0}$ [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	9	0	ns
LE_{IN} [4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	16	0	ns
$DATA_{0-31}$ [4, 6]			LE_{DIAG}	3	3	ns

NOTE: (15) above applies to correction path.

2584 tbl 33

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE}$ $Byte_{0-3}$	↓	↑	$DATA_{0-31}$	0	10	0	12	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	0	10	0	12	ns

2584 tbl 34

MINIMUM PULSE WIDTHS[6]

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive–going pulse)	5		ns

2584 tbl 35

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5F.
6. Not production tested, guaranteed by characterization.

IDT49C460C AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, V_{CC} = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS(1)

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULTERROR}$	Unit
	$DATA_{0-31}$		19	24 (2)	16	20	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 00, 11)		14	21	12	16	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 10)		14	16	—	—	ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	12	↓ 9	↓ 11	ns
		↓	18	—	↑ 9	↑ 11	ns
	CORRECT Not Internal Control Mode		—	16	—	—	ns
	DIAG MODE Not Internal Control Mode		16	26	11	20	ns
	CODE $ID_{1,0}$		18 (6)	23	17	21	ns
	LE_{IN} From latched to Transparent		22	28	19	22	ns
	LE_{DIAG} From latched to Transparent	↑	15 (6)	24	15	19	ns
Internal Control Mode	LE_{DIAG} From latched to Transparent	↑	16 (6)	22	15	18	ns
	$DATA_{0-31}$ Via Diagnostic Latch	↑	15	25 (2)	13	16	ns

2584 tbl 36

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$ (4)		↓	LE_{IN}	3	4	ns
CB_{0-7} (4)		↓	LE_{IN}	2	4	ns
$DATA_{0-31}$ (4, 6)		↓	$LE_{OUT}/\overline{GENERATE}$	6 (16)	0	ns
CB_{0-7} (CODE ID 00, 11) (4, 6)		↓	$LE_{OUT}/\overline{GENERATE}$	14	0	ns
CB_{0-7} (CODE ID 10) (4, 6)		↓	$LE_{OUT}/\overline{GENERATE}$	8	0	ns
CORRECT (4, 6)	↑	↓	$LE_{OUT}/\overline{GENERATE}$	8	0	ns
DIAG MODE (4, 6)		↓	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
$CODE\ ID_{1,0}$ (4, 6)		↓	$LE_{OUT}/\overline{GENERATE}$	10	0	ns
LE_{IN} (4, 6)	↑	↓	$LE_{OUT}/\overline{GENERATE}$	19	0	ns
$DATA_{0-31}$ (4, 6)			LE_{DIAG}	3	3	ns

NOTE: (16) above applies to correction path.

2584 tbl 37

OUTPUT ENABLE/DISABLE TIMES(5)

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE}\ Byte_{0-3}$	↓	↑	$DATA_{0-31}$	0	10	0	12	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	0	10	0	12	ns

2584 tbl 38

MINIMUM PULSE WIDTHS(6)

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive–going pulse)	6		ns

2584 tbl 39

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

IDT49C460C AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, V_{CC} = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
	$DATA_{0-31}$		22	29 [2]	21	24	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 00, 11)		17	23	16	18	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 10)		17	18	—	—	ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	13	↓ 10	↓ 12	ns
		↓	20	—	↑ 10	↑ 12	ns
	CORRECT Not Internal Control Mode		—	17	—	—	ns
	DIAG MODE Not Internal Control Mode		18	29	12	23	ns
	CODE $ID_{1,0}$		21 [6]	26	20	24	ns
	LE_{IN} From latched to Transparent		24	32	21	25	ns
	LE_{DIAG} From latched to Transparent	↑	18 [6]	27	17	21	ns
Internal Control Mode	LE_{DIAG} From latched to Transparent	↑	19 [6]	25	18	21	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch	↑	18	29 [2]	14	18	ns

2584 tbl 40

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$ [4]		↓	LE_{IN}	3	4	ns
CB_{0-7} [4]		↓	LE_{IN}	2	4	ns
$DATA_{0-31}$ [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	7 [19]	3	ns
CB_{0-7} (CODE ID 00, 11) [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	16	0	ns
CB_{0-7} (CODE ID 10) [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	10	0	ns
CORRECT [4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	9	0	ns
DIAG MODE [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	19	0	ns
$CODE\ ID_{1,0}$ [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	12	0	ns
LE_{IN} [4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	21	0	ns
$DATA_{0-31}$ [4, 6]			LE_{DIAG}	3	3	ns

Note: (19) above applies to correction path.

2584 tbl 41

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE}\ Byte_{0-3}$	↓	↑	$DATA_{0-31}$	0	12	0	14	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	0	12	0	14	ns

2584 tbl 42

MINIMUM PULSE WIDTHS[6]

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive–going pulse)	6		ns

2584 tbl 43

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5F.
6. Not production tested, guaranteed by characterization.

IDT49C460B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, V_{CC} = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
	$DATA_{0-31}$		25	30 [2]	25	27	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 00, 11)		14	30	17	20	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 10)		16	18	—	—	ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	12	↓ 23	↓ 23	ns
		↓	21	—	↑ 23	↑ 23	ns
	CORRECT Not Internal Control Mode		—	23	—	—	ns
	DIAG MODE Not Internal Control Mode		17	26	20	24	ns
	CODE $ID_{1,0}$		18 [6]	26	21	26	ns
	LE_{IN} From latched to Transparent		27	38	30	3	ns
	LE_{DIAG} From latched to Transparent	↑	15 [6]	29	19	22	ns
Internal Control Mode	LE_{DIAG} From latched to Transparent	↑	16 [6]	32	19	24	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch	↑	16	32 [2]	20	25	ns

2584 tbl 44

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)	Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$ [4]	↓	LE_{IN}	4	4	ns
CB_{0-7} [4]	↓	LE_{IN}	4	4	ns
$DATA_{0-31}$ [4, 6]	↓	$LE_{OUT}/\overline{GENERATE}$	19	0	ns
CB_{0-7} (CODE ID 00, 11) [4, 6]	↓	$LE_{OUT}/\overline{GENERATE}$	15	0	ns
CB_{0-7} (CODE ID 10) [4, 6]	↓	$LE_{OUT}/\overline{GENERATE}$	15	0	ns
CORRECT [4, 6]	↑	$LE_{OUT}/\overline{GENERATE}$	11	0	ns
DIAG MODE [4, 6]	↓	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
CODE $ID_{1,0}$ [4, 6]	↓	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
LE_{IN} [4, 6]	↑	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
$DATA_{0-31}$ [4, 6]		LE_{DIAG}	4	3	ns

2584 tbl 45

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE\ Byte_{0-3}}$	↓	↑	$DATA_{0-31}$	0	12	0	14	ns
$\overline{OE_{SC}}$	↓	↑	SC_{0-7}	0	12	0	14	ns

2584 tbl 46

MINIMUM PULSE WIDTHS

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive–going pulse)	9		ns

2584 tbl 47

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

IDT49C460B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, V_{CC} = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
	$DATA_{0-31}$		28	33[2]	28	30	ns
	CB_{0-7} ($CODE\ ID_{1,0}$ = 00, 11)		17	33	20	23	ns
	CB_{0-7} ($CODE\ ID_{1,0}$ = 10)		19	23	—	—	ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	15	↓ 26	↓ 26	ns
		↓	24	—	↑ 26	↑ 26	ns
	CORRECT Not Internal Control Mode		—	26	—	—	ns
	DIAG MODE Not Internal Control Mode		20	29	23	27	ns
	$CODE\ ID_{1,0}$		21	29	24	29	ns
	LE_{IN} From latched to Transparent		30	41	33	36	ns
	LE_{DIAG} From latched to Transparent	↑	18	32	22	25	ns
Internal Control Mode	LE_{DIAG} From latched to Transparent	↑	19	35	22	27	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch	↑	19	35[2]	23	28	ns

2584 tbl 56

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$ [4]		↓	LE_{IN}	4	4	ns
CB_{0-7} [4]		↓	LE_{IN}	4	4	ns
$DATA_{0-31}$ [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	23	0	ns
CB_{0-7} ($CODE\ ID$ 00, 11) [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	18	0	ns
CB_{0-7} ($CODE\ ID$ 10) [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	18	0	ns
CORRECT [4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	14	0	ns
DIAG MODE [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
$CODE\ ID_{1,0}$ [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
LE_{IN} [4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	23	0	ns
$DATA_{0-31}$ [4, 6]			LE_{DIAG}	4	3	ns

2584 tbl 57

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE}\ Byte_{0-3}$	↓	↑	$DATA_{0-31}$	0	12	0	14	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	0	12	0	14	ns

2584 tbl 58

MINIMUM PULSE WIDTHS

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive-going pulse)	12		ns

2584 tbl 59

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to 70°C, V_{CC} = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
	$DATA_{0-31}$		27	36[2]	30	33	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 00, 11)		16	34	19	23	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 10)		16	20	—	—	ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	12	↓ 25	↓ 25	ns
		↓	21	—	↑ 25	↑ 25	ns
	CORRECT Not Internal Control Mode		—	23	—	—	ns
	DIAG MODE Not Internal Control Mode		17	26	20	24	ns
	CODE $ID_{1,0}$		18	26	21	26	ns
	LE_{IN} From latched to Transparent		27	38	30	33	ns
	LE_{DIAG} From latched to Transparent	↑	15	29	19	22	ns
Internal Control Mode	LE_{DIAG} From latched to Transparent	↑	16	32	29	24	ns
	$DATA_{0-31}$ Via Diagnostic Latch	↑	16	32[2]	20	25	ns

2584 tbl 52

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$ [4]		↓	LE_{IN}	5	4	ns
CB_{0-7} [4]		↓	LE_{IN}	5	4	ns
$DATA_{0-31}$ [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	23	0	ns
CB_{0-7} (CODE ID 00, 11) [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	15	0	ns
CB_{0-7} (CODE ID 10) [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	15	0	ns
CORRECT [4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	11	0	ns
DIAG MODE [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
$CODE\ ID_{1,0}$ [4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
LE_{IN} [4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	25	0	ns
$DATA_{0-31}$ [4, 6]			LE_{DIAG}	5	3	ns

2584 tbl 53

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE}\ Byte_{0-3}$	↓	↑	$DATA_{0-31}$	0	12	0	14	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	0	12	0	14	ns

2584 tbl 54

MINIMUM PULSE WIDTHS

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive-going pulse)	9		ns

2584 tbl 55

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, Vcc = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: ERROR		To Output: MULT ERROR		Unit
	DATA0–31		30	39[2]	33		36		ns
	CB0–7 (CODE ID1,0 = 00, 11)		19	37	22		26		ns
	CB0–7 (CODE ID1,0 = 10)		19	23	—		—		ns
	LEOUT/GENERATE	↑	—	15	↓	28	↓	28	ns
		↓	24	—	↑	28	↑	28	ns
	CORRECT Not Internal Control Mode		—	26	—		—		ns
	DIAG MODE Not Internal Control Mode		20	29	23		27		ns
	CODE ID1,0		21	29	24		29		ns
	LEIN From latched to Transparent		30	41	33		36		ns
	LEDIAG From latched to Transparent	↑	18	32	22		25		ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	19	35	22		27		ns
Internal Control Mode	DATA0–31 Via Diagnostic Latch	↑	19	35[2]	23		28		ns

2584 tbl 52

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
DATA0–31 [4]		↓	LEIN	5	4	ns
CB0–7 [4]		↓	LEIN	5	4	ns
DATA0–31 [4, 6]		↓	LEOUT/GENERATE	27	0	ns
CB0–7 (CODE ID 00, 11) [4, 6]		↓	LEOUT/GENERATE	18	0	ns
CB0–7 (CODE ID 10) [4, 6]		↓	LEOUT/GENERATE	18	0	ns
CORRECT [4, 6]	↑	↓	LEOUT/GENERATE	14	0	ns
DIAG MODE [4, 6]		↓	LEOUT/GENERATE	20	0	ns
CODE ID1,0 [4, 6]		↓	LEOUT/GENERATE	20	0	ns
LEIN [4, 6]	↑	↓	LEOUT/GENERATE	28	0	ns
DATA0–31 [4, 6]			LEDIAG	5	3	ns

2584 tbl 53

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0–3	↓	↑	DATA0–31	0	12	0	14	ns
OESC	↓	↑	SC0–7	0	12	0	14	ns

2584 tbl 54

MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive-going pulse)	12		ns

2584 tbl 31

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, Vcc = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0-7	To Output: DATA0-31	To Output: ERROR		To Output: MULT ERROR		Unit
	DATA0-31		37	49[2]	40		45		ns
	CB0-7 (CODE ID1,0 = 00, 11)		22	46	26		31		ns
	CB0-7 (CODE ID1,0 = 10)		22	30	—		—		ns
	LEOUT/GENERATE	↗	—	17	↘	30	↘	30	ns
		↘	29	—	↗	30	↗	30	ns
	CORRECT Not Internal Control Mode		—	31	—		—		ns
	DIAG MODE Not Internal Control Mode		23	35	27		33		ns
	CODE ID1,0		25	35	29		35		ns
	LEIN From latched to Transparent		37	51	41		45		ns
	LEDIAG From latched to Transparent	↗	21	38	26		30		ns
Internal Control Mode	LEDIAG From latched to Transparent	↗	22	42	26		33		ns
Internal Control Mode	DATA0-31 Via Diagnostic Latch	↗	22	42[2]	27		34		ns

2584 tbl 60

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
DATA0-31 [4]		↘	LEIN	6	4	ns
CB0-7 [4]		↘	LEIN	5	4	ns
DATA0-31 [4, 6]		↘	LEOUT/GENERATE	30	0	ns
CB0-7 (CODE ID 00, 11) [4, 6]		↘	LEOUT/GENERATE	20	0	ns
CB0-7 (CODE ID 10) [4, 6]		↘	LEOUT/GENERATE	20	0	ns
CORRECT [4, 6]	↗	↘	LEOUT/GENERATE	16	0	ns
DIAG MODE [4, 6]		↘	LEOUT/GENERATE	23	0	ns
CODE ID1,0 [4, 6]		↘	LEOUT/GENERATE	23	0	ns
LEIN [4, 6]	↗	↘	LEOUT/GENERATE	31	0	ns
DATA0-31 [4, 6]			LEDIAG	6	3	ns

2584 tbl 61

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0-3	↘	↗	DATA0-31	0	15	0	17	ns
OESC	↘	↗	SC0-7	0	15	0	17	ns

MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↗↘ (Positive-going pulse)	12		ns

2584 tbl 63

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, V_{CC} = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: ERROR		To Output: MULTERROR		Unit
	DATA0–31		40	52[2]	44		48		ns
	CB0–7 (CODE ID1,0 = 00, 11)		25	49	29		34		ns
	CB0–7 (CODE ID1,0 = 10)		25	33	—		—		ns
	LEOUT/GENERATE	↑	—	20	↓	33	↓	33	ns
		↓	32	—	↑	33	↑	33	ns
	CORRECT Not Internal Control Mode		—	34	—		—		ns
	DIAG MODE Not Internal Control Mode		26	38	30		36		ns
	CODE ID1,0		28	38	32		38		ns
	LEIN From latched to Transparent		40	54	44		48		ns
	LEDIAG From latched to Transparent	↑	24	42	29		33		ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	25	47[2]	29		36		ns
	DATA0–31 Via Diagnostic Latch	↑	25	47	30		37		ns

2584 tbl 64

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
DATA0–31 [4]		↓	LEIN	6	4	ns
CB0–7 [4]		↓	LEIN	5	4	ns
DATA0–31 [4, 6]		↓	LEOUT/GENERATE	36	0	ns
CB0–7 (CODE ID 00, 11) [4, 6]		↓	LEOUT/GENERATE	24	0	ns
CB0–7 (CODE ID 10) [4, 6]		↓	LEOUT/GENERATE	24	0	ns
CORRECT [4, 6]	↑	↓	LEOUT/GENERATE	20	0	ns
DIAG MODE [4, 6]		↓	LEOUT/GENERATE	28	0	ns
CODE ID1,0 [4, 6]		↓	LEOUT/GENERATE	28	0	ns
LEIN [4, 6]	↑	↓	LEOUT/GENERATE	37	0	ns
DATA0–31 [4, 6]			LEDIAG	6	3	ns

2584 tbl 66

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE}$ Byte0–3	↓	↑	DATA0–31	0	15	0	17	ns
$\overline{OE}$SC	↓	↑	SC0–7	0	15	0	17	ns

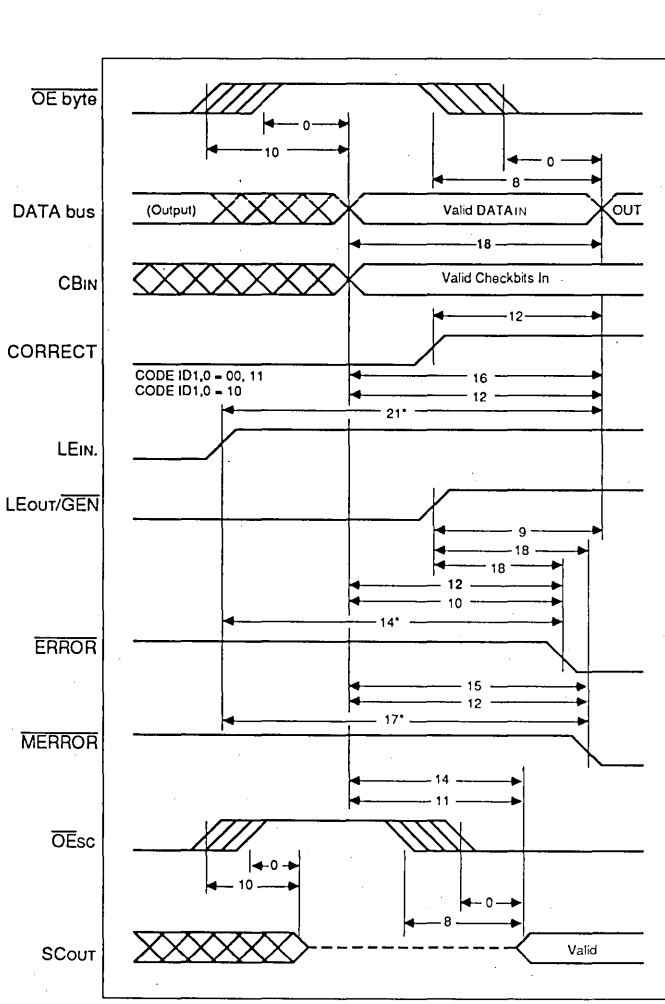
MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive-going pulse)	15		ns

2584 tbl 67

NOTES:
1. CI = 5pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with CI = 5pF and measured to 0.5V change of output level. Testing is performed at CI = 50pF and correlated to CI = 5pF.
6. Not production tested, guaranteed by characterization.

DETECT OR CORRECTION MODE (FROM GENERATE MODE)



Propagation Delay From To	Min./Max.
$\overline{OE}$ byte = High to DATAOUT Disabled	Min.
$\overline{OE}$ byte = High to DATAOUT Disabled	Max.
$\overline{OE}$ byte = Low to DATAOUT Enabled	Min.
$\overline{OE}$ byte = Low to DATAOUT Enabled	Max.
(Corrected DATA if Correct Mode) (DATAIN if Detect Mode)	
DATAIN to DATAOUT	**Max.**
CORRECT = High to DATAOUT	Max.
CBIN to DATAOUT	Max.
CBIN to DATAOUT	Max.
*LEIN = High to DATAOUT	Max.
LEOUT/$\overline{GEN}$ = High to DATAOUT	Max.
LEOUT/$\overline{GEN}$ = High to $\overline{MERROR}$ = Low	Max.
LEOUT/$\overline{GEN}$ = High to $\overline{ERROR}$ = Low	Max.
DATAIN to $\overline{ERROR}$ = Low	**Max.**
CBIN to $\overline{ERROR}$ = Low	Max.
LEIN = High to $\overline{ERROR}$ = Low	Max.
(Low = Error)	
DATAIN to $\overline{MERROR}$ = Low	Max.
CBIN to $\overline{MERROR}$ = Low	Max.
LEIN = High to $\overline{MERROR}$ = Low	Max.
(Low = Error)	
DATAIN to SCOUT	Max.
CBIN to SCOUT	Max.
$\overline{OE}$SC = High to SCOUT Disabled	Min.
$\overline{OE}$SC = High to SCOUT Disabled	Max.
$\overline{OE}$SC = Low to SCOUT Enabled	Min.
$\overline{OE}$SC = Low to SCOUT Enabled	Max.
(Syndrome Bits Come Out)	

NOTES:
1. **BOLD** indicates critical parameters.
* Assumes "CBIN" and/or "DATAIN" are valid at least 4ns before "LEIN" goes high.

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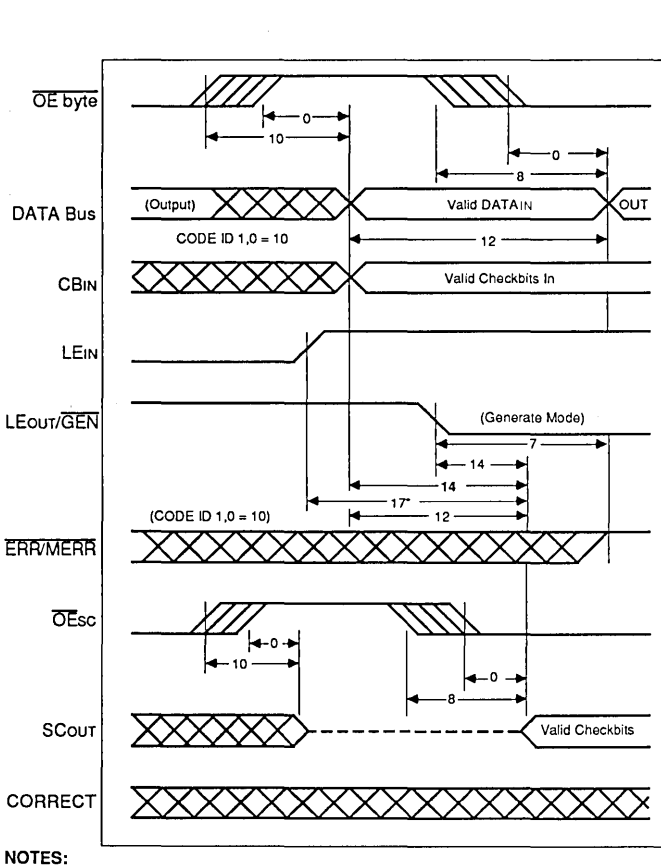
GENERATE MODE (FROM DETECT OR CORRECTION MODE)



Propagation Delay From	To	Min./Max.
$\overline{OE}$ byte = High	to DATAOUT Disabled	Min.
$\overline{OE}$ byte = High	to DATAOUT Disabled	Max.
$\overline{OE}$ byte = Low	to DATAOUT Enabled	Min.
$\overline{OE}$ byte = Low	to DATAOUT Enabled	Max.
CBIN	to DATAOUT	Max.
LEOUT/$\overline{GENERATE}$ = Low	to $\overline{ERROR}$ = High	Max.
LEOUT/$\overline{GENERATE}$ = Low	to SCOUT	Max.
DATAIN	**to SCOUT**	**Max.**
*LEIN = High	to SCOUT*	Max.
CBIN	to SCOUT (Forced High)	Max.
$\overline{OE}$SC = High	to SCOUT Disabled	Min.
$\overline{OE}$SC = High	to SCOUT Disabled	Max.
$\overline{OE}$SC = Low	to SCOUT Enabled	Min.
$\overline{OE}$SC = Low	to SCOUT Enabled (Check Bits Exit)	Max.
	(Don't Care)	

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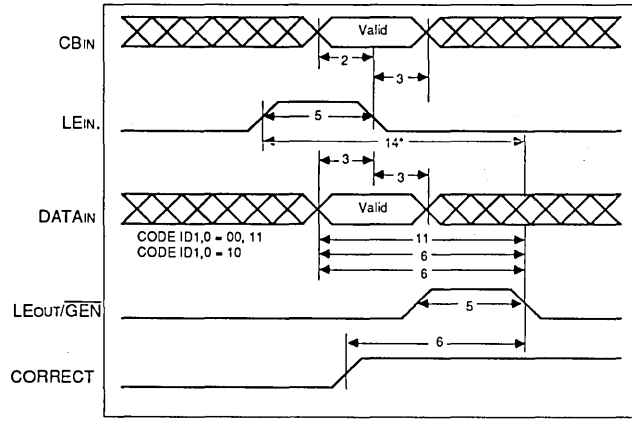
NOTES:
1. **BOLD** indicates critical parameters.
2. Valiid "DATA" and valid CBIN" are shown to occur simultaneously, since both buses are latched and opened by the "LEIN" input.
* Assumes DATA bus becomes input 4ns before LEIN goes high.

5

SET-UP AND HOLD TIMES AND MENIMUM PULSE WIDTHS



Set-up/Hold Time Of	With Respect To	Min./Max.
CBIN	LEIN = Low	Min.
CBIN	LEIN = Low	Min.
LEIN		Min.
*LEIN = High	to LEOUT/$\overline{GEN}$ = Low*	Min.
DATA	LEIN = Low	Min.
DATA	LEIN = Low	Min.
CBIN	LEOUT/$\overline{GEN}$ = Low	Min.
CBIN	LEOUT/$\overline{GEN}$ = Low	Min.
DATA	LEOUT/$\overline{GEN}$ = Low	Min.
LEOUT/$\overline{GENERATE}$		Min.
CORRECT	LEOUT/$\overline{GEN}$ = Low	Min.

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NOTES:

1. **BOLD** indicates critical parameters.
* Enable to enable timing requirement to ensure that the last DATA word applied to "DATAIN" is made available as DATAOUT"; assumes that "DATAIN" is valid at least 4ns before "LEIN" goes high.

INPUT/OUTPUT INTERFACE CIRCUIT

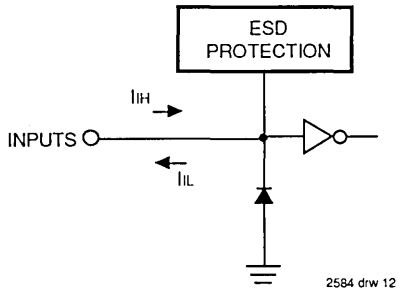


Figure 5. Input Structure (All Inputs)

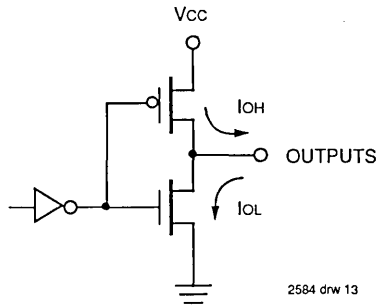
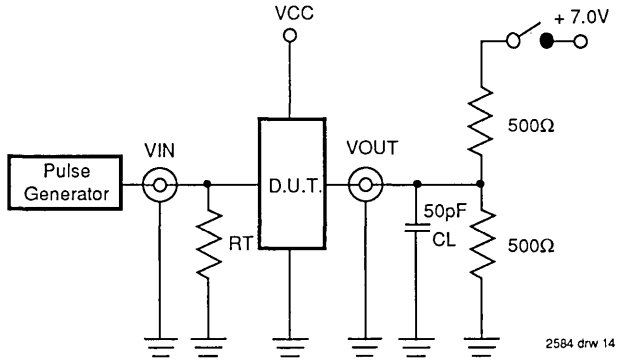


Figure 6. Out put Structure

TEST LOAD CIRCUIT



DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance
RL = Termination resistance: should be equal to ZOUT of the Pulse Generator

Figure 7.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 7

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Test	Switch
Open Drain Disable Low Enable Low	Closed
All other Outputs	Open

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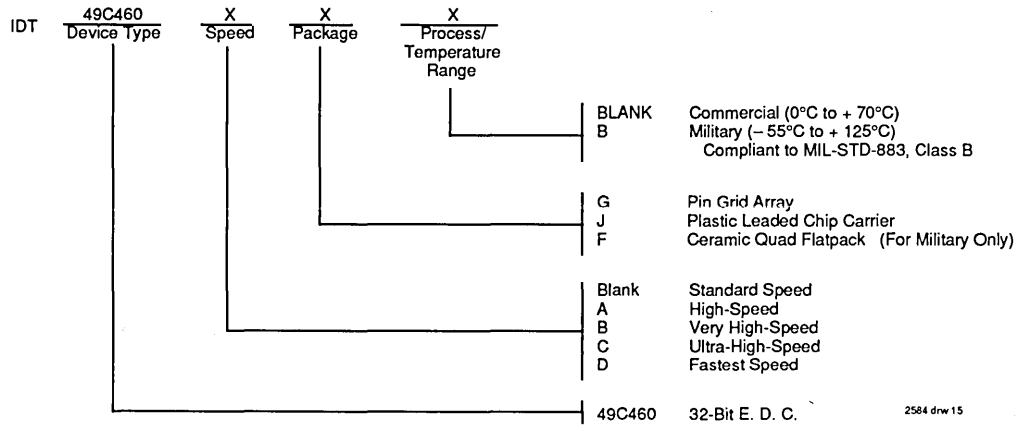
ORDERING INFORMATION



Integrated Device Technology, Inc.

32-BIT FLOW-THRU ERROR DETECTION AND CORRECTION UNIT

PRELIMINARY
IDT49C465

FEATURES

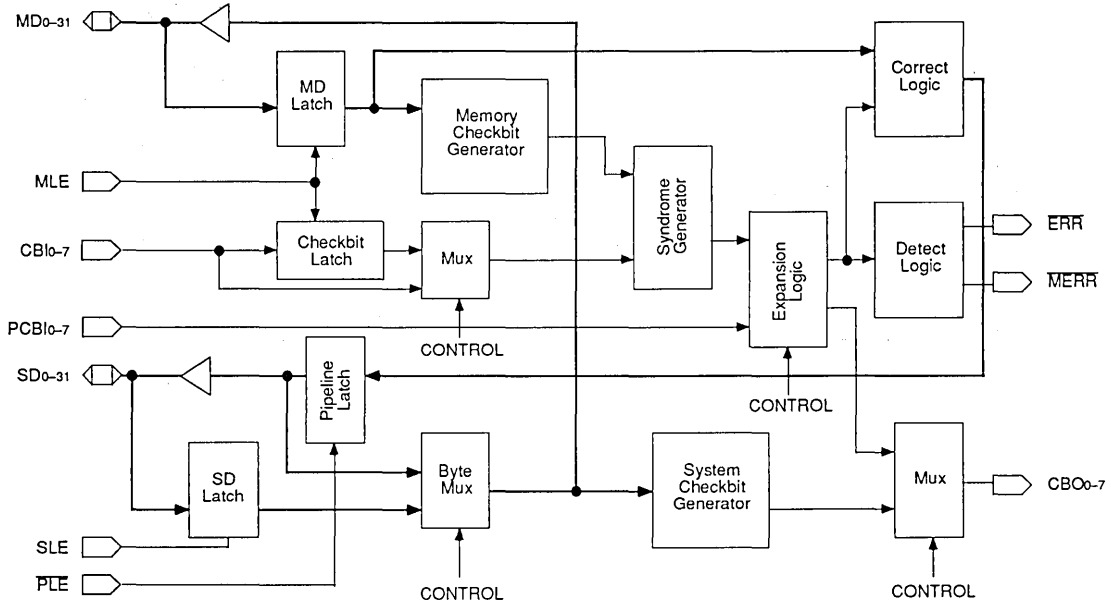
- 32-bit wide Flow-thruEDC™ unit
- Expandable to 64 bits
- Single-chip 64-bit Generate Mode
- Separate system and memory buses
- On-chip pipeline latch with external control
- Supports bi-directional and common I/O memories
- Corrects all single-bit errors
- Detects all double-bit errors, some multiple-bit errors
- Error Detection Time — 15ns
- Error Correction Time — 20ns
- Internal syndrome register
- Four-bit error counter and error-data register on-chip
- Parity generation and checking on system data bus
- Low power CMOS — 100mA typical
- 144-pin PGA package
- Military product compliant to MIL-STD 883, Class B

DESCRIPTION

The IDT49C465 is a 32-bit, two-data bus, Flow-thruEDC unit. The chip provides single-error correction and multiple-error detection of both hard and soft memory errors. It can be expanded to 64-bit widths by cascading 2 units, without the need for additional external logic. The Flow-thruEDC has been optimized for speed and simplicity of control.

The EDC unit has been designed to be used in either of two configurations in an error correcting memory system. The bi-directional configuration is most appropriate for systems using bi-directional memory buses. A second system configuration utilizes external octal buffers and is particularly well suited for systems using memory with separate I/O buses.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



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Flow-thruEDC™ is a trademark of Integrated Device Technology Inc.

PIN CONFIGURATION

	A	B	C	D	E	F	G	H		J	K	L	M	N	P	Q
15	VCC	SD 2	PCBI 6	PCBI 5	PCBI 3	CODE ID 1	CODE ID 0	MODE 1	$\overline{\text{MERR}}$	$\overline{\text{ERR}}$	SYO 5	SYO 3	SYO 1	MD 1	VCC
14	SD 6	SD 4	SD 1	PCBI 7	PCBI 4	PCBI 1	PCBI 0	MODE 0	SYO 6	SYO 4	SYO 2	MD 0	MD 2	VCC	MD 5
13	SD 9	SD 5	BE 0	SD 3	SD 0	PCBI 2	GND	GND	SYO 7	GND	SYO 0	VCC	MD 3	MD 6	MD 9
12	SD11	SD 7	VCC										MD 4	MD 8	GND
11	SD12	SD10	SD 8										MD 7	MD 10	MD 11
10	SD15	BE 1	GND										MD 12	MD 13	MD 15
9	SLE	SD13	SD14										$\overline{\text{MOE}}$	MD 14	MLE
8	$\overline{\text{SOE}}$	$\overline{\text{PLE}}$	GND				G144-1						GND	MD 17	MD 16
7	SD17	SD19	SD16										MD 20	MD 21	MD 18
6	SD18	BE 2	SD20										GND	MD 23	MD 19
5	SD21	SD22	SD25										MD 27	MD 25	MD 22
4	GND	SD24	BE 3										VCC	MD 28	MD 24
3	SD23	SD26	SD28	VCC	CBO 0	$\overline{\text{CBOE}}$	CBO 7	GND	GND	$\overline{\text{SCLK}}$ $\overline{\text{EN}}$	GND	CBI 6	CBI 7	MD 30	MD 26
2	SD27	VCC	SD29	SD31	CBO 2	CBO 4	CBO 6	P3	MODE 2	SYN-CLK	CBI 0	CBI 3	CBI 4	MD 31	MD 29
1	VCC	SD30	CBO 1	CBO 3	CBO 5	PSEL	$\overline{\text{PERR}}$	P2	P1	P0	$\overline{\text{CLEAR}}$	CBI 1	CBI 2	CBI 5	VCC

Reference Square

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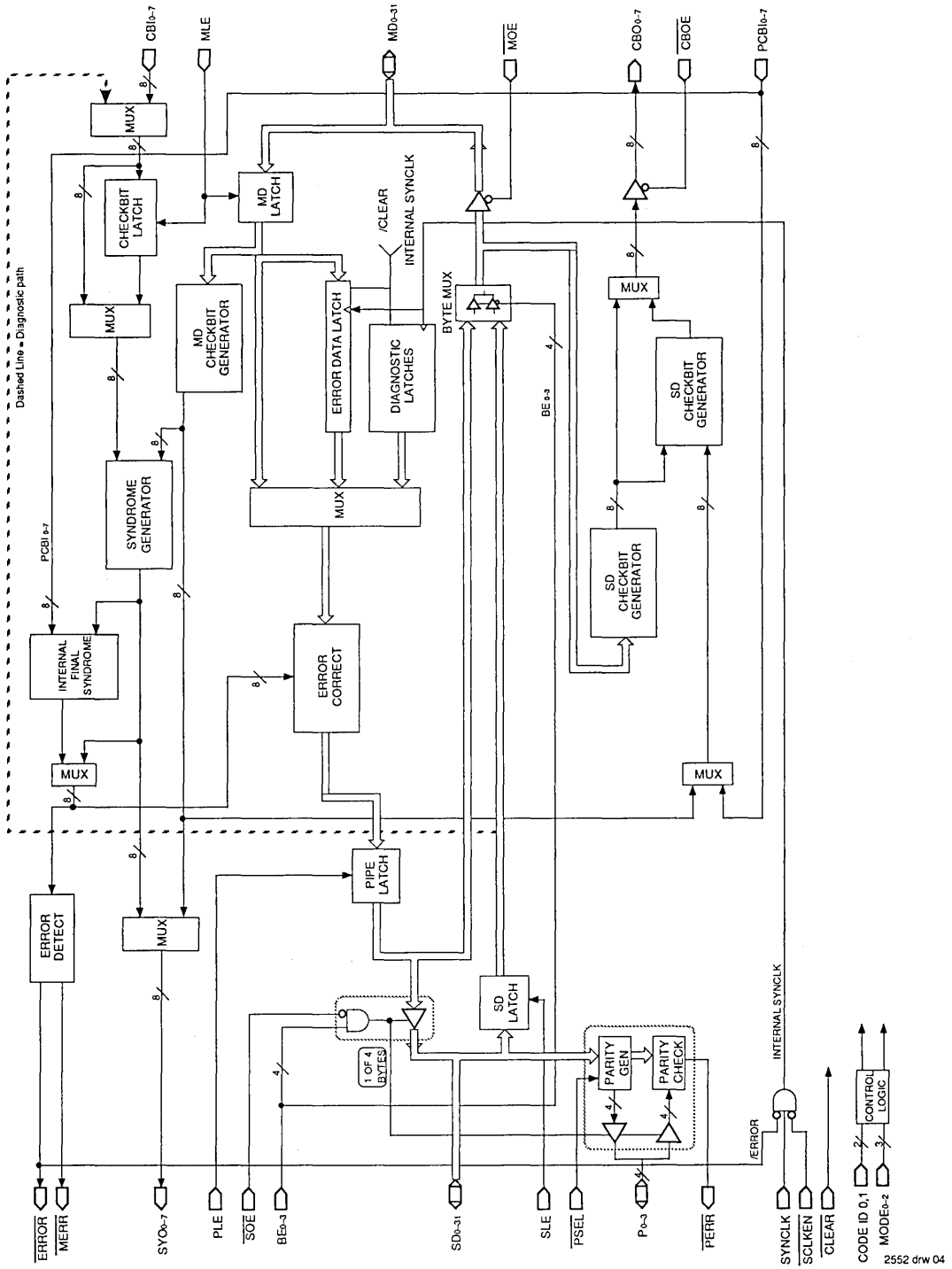
PGA
TOP VIEW

DETAILED FUNCTIONAL BLOCK DIAGRAM



5

SYSTEM CONFIGURATIONS

The IDT49C465 EDC unit can be used in various configurations in an EDC system. The basic configurations are shown below.

Figure 1 illustrates a bi-directional configuration, which is most appropriate for systems using bi-directional memory buses. It is the simplest configuration to understand and use. During a correction cycle, the corrected data word can be simultaneously output on both the system bus and memory bus. Logically, no other parts are required for the correction function. During partial-word-write operations, the new bytes are internally combined with the corrected old bytes for checkbit generation and writing to memory.

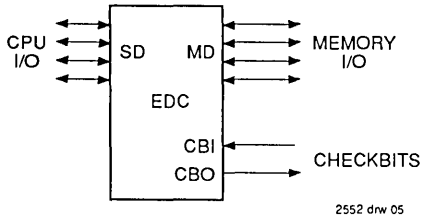


Figure 1. Bi-Directional Configuration

Figure 2 illustrates a separate I/O configuration. This is appropriate for systems using separate I/O memory buses. This configuration allows separate input and output memory buses to be used. Corrected data is output on the SD outputs for the system and for re-write to memory. Partial word-write bytes are combined externally for writing and checkbit generation.

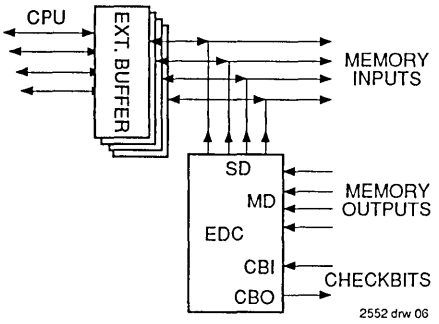


Figure 2. Separate I/O Configuration

Figure 3 illustrates a third configuration which utilizes external buffers and is also well suited for systems using memory with separate I/O buses. Since data from memory does not need to pass through the part on every cycle, the EDC system may operate in "bus-watch" mode. As in the separate I/O configuration, corrected data is output on the SD outputs.

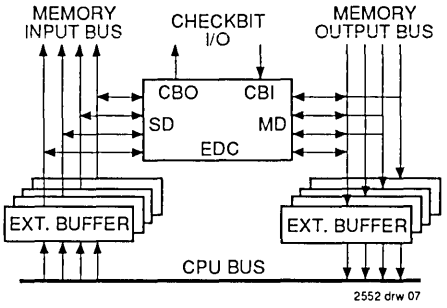


Figure 3. Bypassed Separate I/O Configuration

Figure 4 illustrates the single-chip generate-only mode for very fast 64-bit checkbit generation in systems that use separate checkbit-generate and detect-correct units. If this is not desired, 64-bit checkbit generation and correction can be done with just 2 EDC units. 64-bit correction is also straightforward, fast and requires no extra hardware for the expansion.

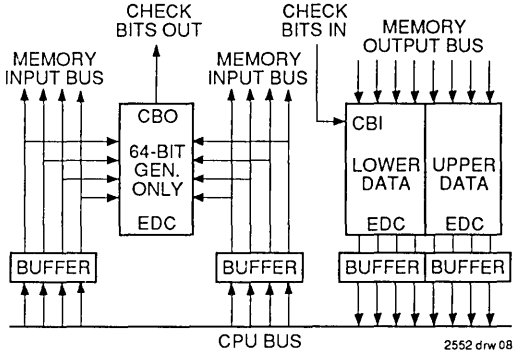


Figure 4. Separate Generate/Correction Units with 64-Bit Checkbit Generation

FUNCTIONAL DESCRIPTION

The error detection/correction codes consist of a modified Hamming code; it is identical to that used on the IDT49C460.

32-BIT MODE (CODE ID 1,0=00)

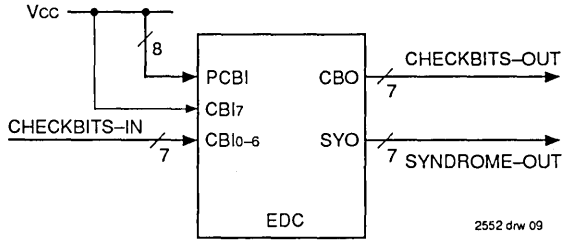


Figure 5. 32-Bit Mode

64-BIT MODE (CODE ID 1,0=10 & 11)

The expansion bus topology is shown in Figure 6. This topology allows the syndrome bits used by the correction logic to be generated simultaneously in both parts used in the expansion. During a 64-bit detection or correction operation, "Partial-Checkbit" data and "Partial-Syndrome" data is simultaneously exchanged between the two EDC units in opposite directions on dedicated expansion buses. This results in very short 64-bit detection and correction times.

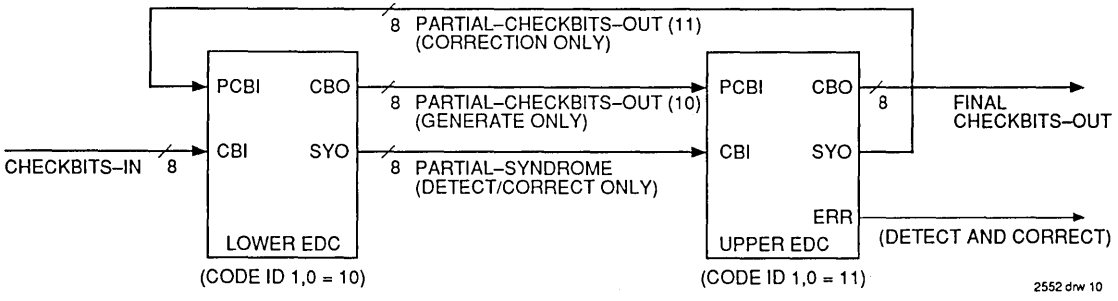


Figure 6. 64-Bit Mode — 2 Cascaded IDT49C465 Devices

64-BIT GENERATE-ONLY MODE (CODE ID 1,0=01)

If the Identity pins CODE ID 1,0 = 01, a single EDC is placed in the 64-bit "Generate-only" mode. In this mode, the lower 32 bits of the 64-bit data word enter the device on the SD_{0-31} inputs. This provides the device with the full 64-bit word from memory. The resultant generated checkbits are output on the CBO_{0-7} outputs. The generate time is less than that resulting from using a 2-chip cascade.

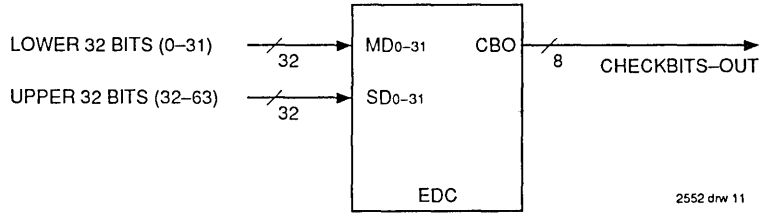


Figure 7. 64-Bit "Generate-Only" Mode (Single Chip)

PIN DESCRIPTIONS

Symbol	I/O		Name and Function
I/O Buses and Controls			
SD_{0-7} SD_{8-15} SD_{16-23} SD_{24-31}	I/O		**System Data Bus:** Data from MD_{0-31} appears at these pins corrected if MODE 2-0 = x11, or uncorrected in the other modes. The BE_n inputs must be high and the $\overline{SOE}$ pin must be low to enable the SD output buffers during a read cycle. (Also, see diagnostic section.) **Separate I/O memory systems:** In a write or partial-write cycle, the byte not-to-be-modified is output on SD_n to n+7 for re-writing to memory, if BE_n is high and $\overline{SOE}$ is low. The new bytes to be written to memory are input on the SD_n pins, for writing checkbits to memory, if BE_n is low. **Bi-directional memory systems:** In a write or partial-write cycle, the byte not-to-be-modified is re-directed to the MD I/O pins, if BE_n is high, for checkbit generation and rewriting to memory via the MD I/O pins. $\overline{SOE}$ must be high to avoid enabling the output drivers to the system bus in this mode. The new bytes to be written are input on the SD_n pins for checkbit generation and writing to memory. BE_n must be low to direct input data from the System Data bus to the MD I/O pins for checkbit generation and writing to the checkbit memory.
SLE	I		**System Latch Enable:** SLE is an input used to latch data at the SD inputs. The latch is transparent when SLE is high; the data is latched when SLE is low.
$\overline{PLE}$	I		**Pipeline Latch Enable:** $\overline{PLE}$ is an input which controls a pipeline latch, which controls data to be output on the SD bus and the MD bus during byte merges. Use of this latch is optional. The latch is transparent when $\overline{PLE}$ is low; the data is latched when $\overline{PLE}$ is high.
$\overline{SOE}$	I		**System Output Enable:** When low, enables System output drivers and Parity output drivers if corresponding Byte Enable inputs are high.
BE_{0-3}	I		**Byte Enables:** In systems using separate I/O memory buses, BE_n is used to enable the SD and Parity outputs for byte n. The BE_n pins also control the "Byte mux". When BE_n is high, the corrected or uncorrected data from the Memory Data latch is directed to the MD I/O pins and used for checkbit generation for byte n. This is used in partial-word-write operations or during correction cycles. When BE_n is low, the data from the System Data latch is directed to the MD I/O pins and used for checkbit generation for byte n. BE_0 controls SD_{0-7} BE_2 controls SD_{16-23} BE_1 controls SD_{8-15} BE_3 controls SD_{24-31}
MD_{0-31}	I/O		**Memory Data Bus:** These I/O pins accept a 32-bit data word from main memory for error detection and/or correction. They also output corrected old data or new data to be written to main memory when the EDC unit is used in a bi-directional configuration.
MLE	I		**Memory Latch Enable:** MLE is used to latch data from the MD inputs and checkbits from the CBI inputs. The latch is transparent when MLE is high; data is latched when MLE is low. When identified as the upper slice in a 64-bit cascade, the checkbit latch is bypassed.
$\overline{MOE}$	I		**Memory Output Enable:** $\overline{MOE}$ enables Memory Data Bus output drivers when low.
P_{0-3}	I/O		**Parity I/O:** The parity I/O pins for Bytes 0 to 3. These pins output the parity of their respective bytes when that byte is being output on the SD bus. These pins also serve as parity inputs and are used in generating the Parity ERRor ($\overline{PERR}$) signal under certain conditions (see Byte Enable definition). The parity is odd or even depending on the state of the Parity SELect pin (PSEL).
PSEL	I		**Parity SELect:** If the Parity SELect pin is low, the parity is even. If the Parity SELect pin is high, the parity is odd.
Inputs			
CBI_{0-7}	I		**CheckBits-In** (00) CheckBits-In-1 (10) Partial-Syndrome-In (11): In a single EDC system or in the lower slice of a cascaded EDC system, these inputs accept the checkbits from the checkbit memory. In the upper slice in a cascaded EDC system, these inputs accept the "Partial-Syndrome" from the lower slice (Detect/Correct path).
$PCBI_{0-7}$	I		**Partial-CheckBits-In** (10) Partial-CheckBits-In (11): In a single EDC system, these inputs are unused but should not be allowed to float. In a cascaded EDC system, the "Partial-Checkbits" used by the lower slice are accepted by these inputs (Correction path only). In the upper slice of a cascaded EDC system, "Partial-Checkbits" generated by the lower slice are accepted by these inputs (Generate path).
$CODE\ ID_{1,0}$	I		**CODE IDentity:** Inputs which identify the slice position/ functional mode of the IDT49C465. (00) Single 32-bit EDC unit (10) Lower slice of a 64-bit cascade (01) 64-bit "Checkbit-generate-only" unit (11) Upper slice of a 64-bit cascade

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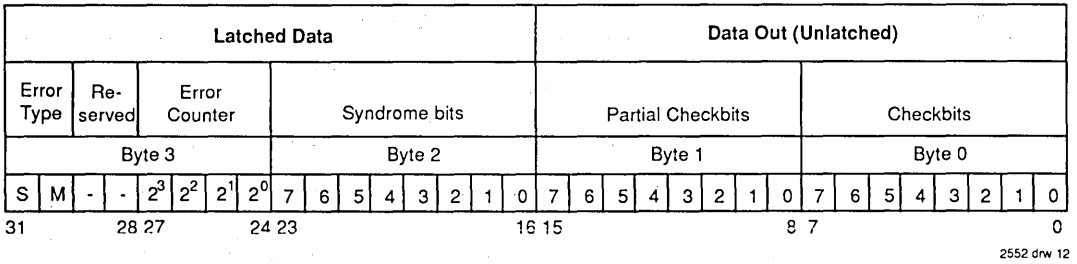
PIN DESCRIPTIONS (Con't.)

Symbol	I/O		Name and Function
Inputs (Con't.)			
$MODE_{2-0}$	I		**MODE select:** Selects one of four operating modes.
		(x11)	**"Normal" Mode:** Normal EDC operation (Flow-thru correction and generation).
		(x10)	**"Generate-Detect" Mode:** In this mode, error correction is disabled. Error generation and detection are normal.
		(000)	**"Error-Data-Output" Mode:** Allows the uncorrected data captured from an error event by the Error-Data Register to be read by the system for diagnostic purposes. The Error-Data Register is cleared by toggling $\overline{CLEAR}$ low. The Syndrome Register and Error-Data Register record the syndrome and uncorrected data from the first error that occurs after they are reset by the $\overline{CLEAR}$ pin. The Syndrome Register and Error-Data Register are updated when there is a positive edge on SYNCLK, an error condition is indicated ($\overline{ERROR}$ = low), and the Error Counter indicates zero. **All-Zero-Data Source:** In Error-Data-Output Mode, clearing the Error-Data Register provides a source of all-zero-data for hardware initialization of memory, if this desired.
		(x01)	**Diagnostic-Output Mode:** In this mode, the contents of the Syndrome Register , Error Counter and Error-Type Register are output on the SD bus. This allows the syndrome bytes for an indicated error to be read by the system for error-logging purposes. The Syndrome Register and the Error-Data Register are updated when there is a positive edge on SYNCLK, an error condition is indicated and the Error Counter indicates zero errors. Thus, the Syndrome Register saves the syndrome that was present when the first error occurred after the Error Counter was cleared. The Syndrome Register and the Error Counter are cleared by toggling $\overline{CLEAR}$ low. The Error Counter lets the system tell if more than one error has occurred since the last time the Syndrome Register or Error-Data Register was read.
		(100)	**Checkbit-Injection Mode:** In the "Checkbit-Injection" Mode, diagnostic checkbits may be input on System Data Bus bits 0-7 (see Diagnostic Features - Detailed Description).
$\overline{CLEAR}$	I		**CLEAR:** When the $\overline{CLEAR}$ pin is taken low, the Error-Data Register, the Syndrome Register, the Error Counter and the Error-Type Register are cleared.
SYNCLK	I		**SYNdrome CLocK:** If $\overline{ERROR}$ is low, and the Error Counter indicates zero errors, syndrome bits are clocked into the Syndrome Register and data from the outputs of the Memory Data input latch are clocked into the Error-Data Register on the low-to-high edge of SYNCLK. If $\overline{ERROR}$ is low, the Error Counter will increment on the low-to-high edge of SYNCLK, unless the Error Counter indicates fifteen errors.
$\overline{SCLKEN}$	I		**SynCLK ENable:** The $\overline{SCLKEN}$ enables the SYNCLK signal. SYNCLK is ignored if $\overline{SCLKEN}$ is high.
Outputs and Enables			
CBO_{0-7}	O		**CheckBits-Out** (00, 01) Partial-CheckBits-Out (10) Checkbits-Out (11): In a single EDC system, the checkbits are output to the checkbit memory on these outputs. In the lower slice in a cascaded EDC system, the "Partial-checkbits" used by the upper slice are output by these outputs (Generate path only). In the upper slice in a cascade, the "Final-Checkbits" appear at these outputs (Generate path only).
$\overline{CBOE}$	I		**CheckBits Out Enable:** Enables CheckBit Output drivers when low.
SYO_{0-7}	O		**SYndrome-Out** (00) Partial-SYndrome-Out (10) Partial-Checkbits-Out (11): In a 32-bit EDC system, the syndrome bits are output on these pins. In the lower slice in a 64-bit cascaded system, the "Partial-Syndrome" bits appear at these outputs (Detect/ Correct path). In the upper slice in a cascaded EDC system, the "Partial-Checkbits" appear at these outputs (Correct path only). In a 64-bit cascaded system, the "Final-Syndrome" may be accessed in the "Diagnostic-Output" Mode from either the lower or the upper slice since the final syndrome is contained in both.
$\overline{ERR}$	O		**ERROR:** When in "Normal" and "Detect only" modes, a low on this pin indicates that one or more errors have been detected. $\overline{ERR}$ is not gated or latched internally.
$\overline{MERR}$	O		**Multiple ERRor:** When in "Normal" and "Detect only" modes, a low on this pin indicates that two or more errors have been detected. $\overline{MERR}$ is not gated or latched internally.
$\overline{PERR}$	O		**Parity ERRor:** A low on this pin indicates a parity error which has resulted from the active bytes defined by the 4 Byte Enable pins. Parity ERRor ($\overline{PERR}$) is not gated or latched internally (see Byte Enable definition).
Power Supply Pins			
$V_{CC\ 1-10}$	P		+5 Volts
GND_{1-12}	P		Ground

2552 tbl 02

5

DIAGNOSTIC DATA FORMAT (SYSTEM BUS)



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DIAGNOSTIC FEATURES — DETAILED DESCRIPTION

Mode 2-0	
x11	**"NORMAL" Mode** In this mode, operation is "Normal" or non-diagnostic.
x10	**"GENERATE-DETECT" Mode** When the EDC unit is in the **"Generate-Detect" Mode**, data is not corrected or altered by the error correction network. (Also referred to as the "Detect-only" Mode.)
000	**"ERROR-DATA-OUTPUT" Mode** In this mode, the 32-bit data from the Error-Data Register is output on the SD bus. **Error Data Register**: The uncorrected data from the Memory Data bus input latch is stored in the Error-Data Register if the error counter contents indicates "0" and there is a positive transition on the SYNCLK input when the $\overline{\text{ERROR}}$ signal is low. Thus, the Error-Data Register contains memory data corresponding to the first error to occur since the register was cleared. This register is cleared by pulling the $\overline{\text{CLEAR}}$ input low. The register is read via the System Data bus by entering the **"Error-Data-Output"** Mode and enabling the System Data bus output drivers. **All-Zero-Data**: The Error-Data Register can be used as an "all-zero-data" data source for memory initialization in systems where the initialization process is to be done entirely by hardware.
x01	**"DIAGNOSTIC-OUTPUT" Mode** In this mode, data from the diagnostic registers, the PCBI bus and the CBI bus is output on the SD bus. **Direct Checkbit Readback**: Internal data paths allow both the "Partial-CheckBit-Input" bus and the data in the "CheckBit-Input" latch to be read directly by the system bus for diagnostic purposes. Both the Checkbit Input Bus and the Partial Checkbit Input Bus are read via the System Data bus by entering the **"Diagnostic-Output" Mode** and enabling the System Data bus output drivers. The checkbits are output on System Data bus bits 0-7; the Partial Checkbits are output on bits 8-15. **Syndrome Register:** After an error has been detected, the syndrome bits generated are clocked into the internal Syndrome Register if the error counter contents indicates "0" and there is a positive transition on the SYNCLK input when the $\overline{\text{ERROR}}$ signal is low. This register is cleared by pulling the $\overline{\text{CLEAR}}$ input low. The register is read via the System Data bus by entering the **"Diagnostic-Output" Mode** and enabling the System Data bus outputs. This data is output on SD bits 16-23. **Error Counter**: The 4-bit on-board error counter is incremented if the error counter contents do not indicate FF HEX, which corresponds to a count of 15, and there is a positive transition on the SYNCLK input when the $\overline{\text{ERROR}}$ signal is low. This counter is cleared by pulling the $\overline{\text{CLEAR}}$ input low. The counter is read via the System Data bus by entering the **"Diagnostic-Output" Mode** and enabling the System Data bus output drivers. This data is output on System Data bus bits 24-27. **Test Register**: These 2 bits are reserved for factory diagnostics only and must not be used by system software. This data is output on System Data bus bits 28-29. **Error-Type Register**: The Error-Type Register, clocked by the SYNCLK input, saves 2 bits which indicate whether a recorded error was a single or a multiple-bit error. This register holds only the first error type to occur after the last Clear operation. This data is output on System Data bus bits 30-31.
100	**Direct Read-Path Checkbit Injection**: In the **"Checkbit-Injection" Mode**, bits 0-7 of the System Data input latch are presented to the inputs of the Checkbit Input latch. If MLE is strobed, the checkbit latch will be loaded with this value in place of the checkbits from memory. By inserting various checkbit values, operation of the correction function of the EDC can be verified "on-board". Except for the "Checkbit-Injection" function, operation in this mode is identical to "Normal" Mode operation.

2552 tbl 03

OPERATING MODE CHARTS

SLICE IDENTIFICATION

CODE ID 1	CODE ID 0	Slice Definition
0	0	32-bit Flow-Thru EDC
0	1	64-bit GENERATE Only EDC
1	0	64-bit EDC- Lower 32 bits (0-31)
1	1	64-bit EDC- Upper 32 bits (32-63)

2552 tbl 04

SLICE POSITION CONTROL

CODE ID	Slice Position/ Functional Operation	SOE	SD Bus	MOE	MD Bus	Checkbit Buses: PCBI Bus	CBI Bus	CBO Bus	SYO Bus	P Bus	PERR
1 0	Width =		32		32	8	8	8	8	4	1
0 0	Single 32-bit EDC unit										
	Generate[1]	1	Sys. 0–31	0	Sys. Byte Mux	—	—	CBs out	—	P in	active
	Detect/Correct[2]	0	Pipe. latch	1	MD 0–31	—	CBs in	—	Syn. out	P out	—
0 1	"64-bit Generate-only"	1	Sys. 32–63	1	Sys. 0–31	—	—	CBs out	—	—	—
1 0	Lower word, 64-bit bus										
	Generate[1]	1	Sys. 0–31	0	MD 0–31	—	—	PCBs out	—	P in	active
	Detect/Correct[2]	0	Pipe. latch	1	MD 0–31	U-SYOout	CBs in	—	Par.Synd	P out	—
1 1	Upper word, 64-bit bus										
	Generate[1]	1	Sys. 32–63	0	MD 32–63	L-CBOout	—	F.CBs out	—	P in	active
	Detect/Correct[2]	0	Pipe. latch	1	MD 32–63	—	L-SYOout	—	Par.Cbits	P out	—

NOTES:
1. Checkbits generated from the data in the SD Latch.
2. Corrected data residing in the Pipeline Latch.

2552 tbl 05

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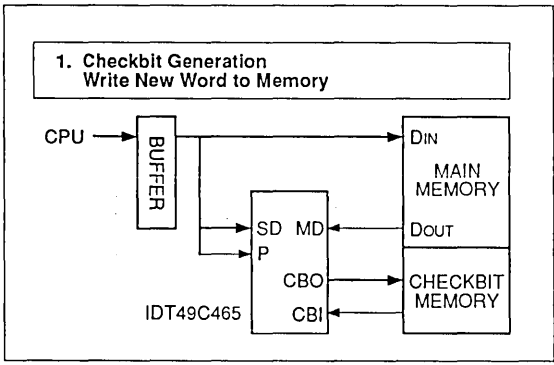
FUNCTIONAL MODE CONTROL

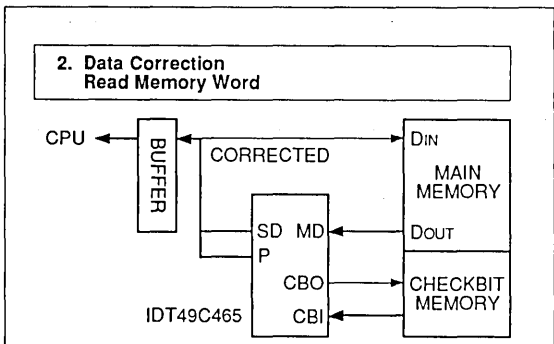
MODE 2	MODE 1	MODE 0	Functional Mode of SD Bus	SOE	SD Bus	MOE	MD Bus	Checkbit Buses: PCBI Bus	CBI Bus	CBO Bus	SYO Bus	P Bus	PERR
			Width =		32		32	8	8	8	8	4	1
x	1	1	**"Normal"**										
			Generate	1	CPU Data	0	Pipe. latch	—	—	CB out	—	P in	active
			Correct	0	Pipe. latch	1	RAM Data	—	CB in	—	—	P out	—
x	1	0	**"Generate-Detect"**										
			Generate	1	CPU Data	0	Pipe. latch	—	—	CB out	—	P in	active
			Detect	0	Pipe. latch	1	RAM Data	—	CB in	—	—	P out	—
0	0	0	**"Error-Data-Output"**	0	Err. D. latch	—	—	—	—	—	—	—	—
x	0	1	**"Diagnostic-Output"**	0	CBin latch PCBIin bus Syn. register Err. counter Er. type reg.	—	—	PCBI in	CB in	—	—	—	—
1	0	0	**"Checkbit-Injection"**										
			Generate	1	SDin latch	0	Pipe. latch	—	—	CB out	—	P in	active
			Inject Checkbits	1	SD0–7 in	0	Pipe. latch	—	—	—	—	—	—
			Correct	0	Pipe. latch	1	RAM Data	—	CB in	—	—	P out	—

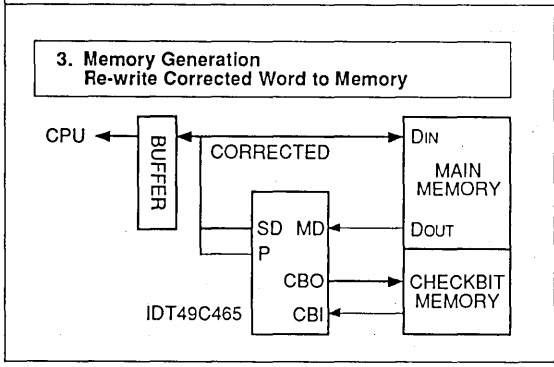
2552 tbl 06

PRIMARY DATA PATH vs. MEMORY CONFIGURATION

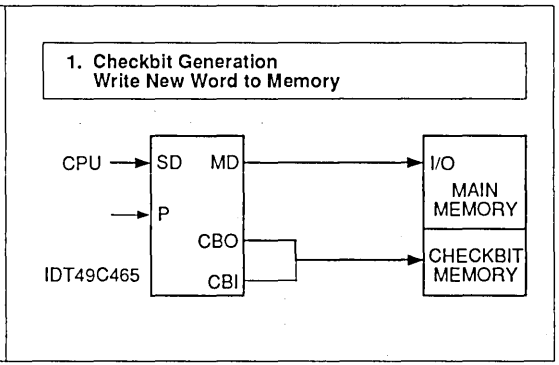
SEPARATE I/O MEMORIES:

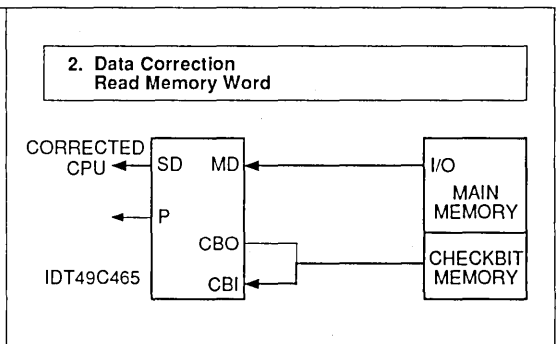


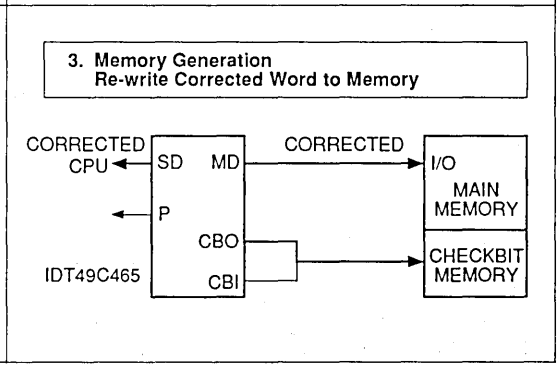




COMMON I/O MEMORIES:



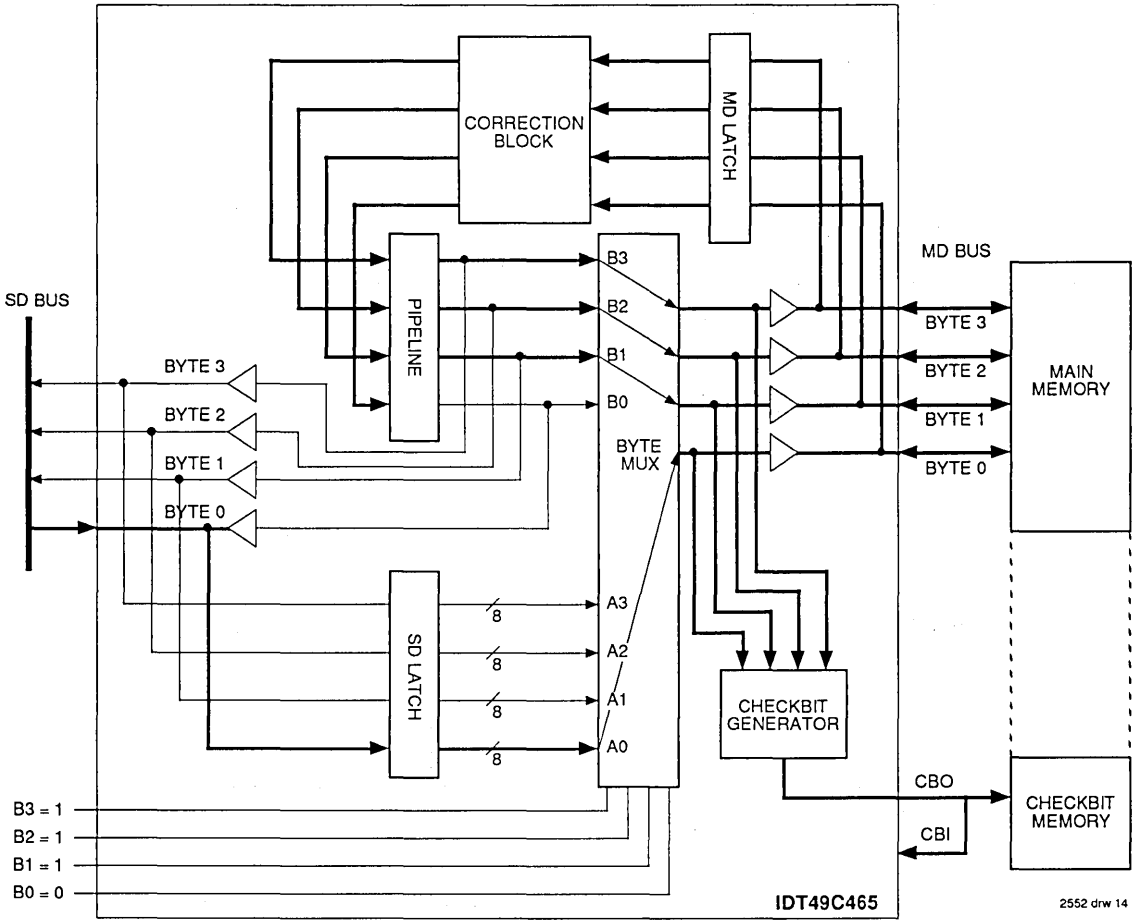




2552 drw 13

PARTIAL-WORD-WRITE OPERATIONS

FOR COMMON I/O MEMORIES:



In order to perform a partial-word-write operation, the complete word in question must be read from memory. This must be done in order to correct any error which may have occurred in the old word. Once the complete, corrected word is available, with all the bytes verified, the new word may be assembled in the byte mux and the new checkbits generated.

The example shown above illustrates the case of combining 3 bytes from an old word with a new lower order byte to form a new word. The new word, along with the new checkbits, may now be written to memory.

In the separate I/O memory configuration, the situation is similar except that the new word is output on the SD Bus instead of the MD Bus (refer to previous page).

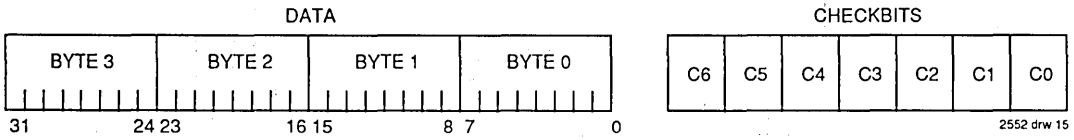
32-BIT DATA WORD CONFIGURATION

A single IDT49C465 EDC unit, connected as shown below, provides all the logic needed for single-bit error correction, and double-bit error detection, of a 32-bit data field. The identification code (00) indicates 7 checkbits are required. The CBI7 pin should be tied high.

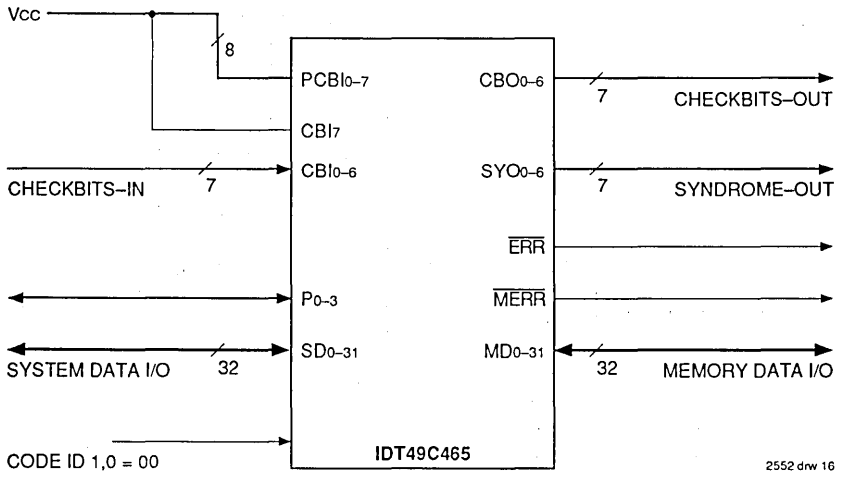
The 39-bit data format for four bytes of data and 7 checkbits is indicated below.

Syndrome bits are generated by an exclusive-OR of the generated checkbits with the checkbits read from memory. For example, Sn is the XOR of checkbits from those read with those generated. During Data Correction, the syndrome bits are used to complement (correct) single-bit errors in the data bits.

32-BIT DATA FORMAT



32-BIT HARDWARE CONFIGURATION



64-BIT DATA WORD CONFIGURATION

Two IDT49C465 EDC units, connected as shown below, provide all the logic needed for single-bit error correction, and double-bit error detection, of a 64-bit data field. The "Slice Identification" Table gives the CODE ID1,0 values needed for distinguishing the upper 32 bits from the lower 32 bits. Final generated checkbits, $\overline{\text{ERROR}}$ and $\overline{\text{MULTIPLE ERROR}}$ signals come from the upper slice, the IC with CODE ID1,0=11. Control signals not shown are connected to both units in parallel.

Data-In bits 0 through 31 are connected to the same numbered inputs of the EDC with CODE ID1,0=10, while Data-In bits 32 through 63 are connected to data inputs 0 to 31, respectively, for the EDC unit with CODE ID1,0=11.

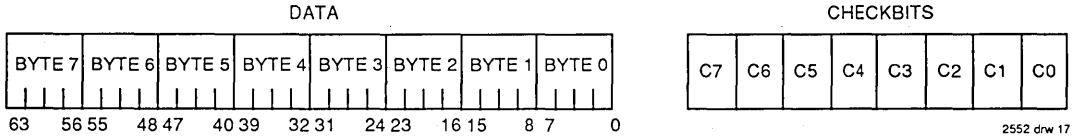
The 72-bit data format of data and checkbits is indicated below.

Correction of single-bit errors in the 64-bit configuration requires a simultaneous exchange of partial checkbits and partial syndrome bits between the upper and lower units.

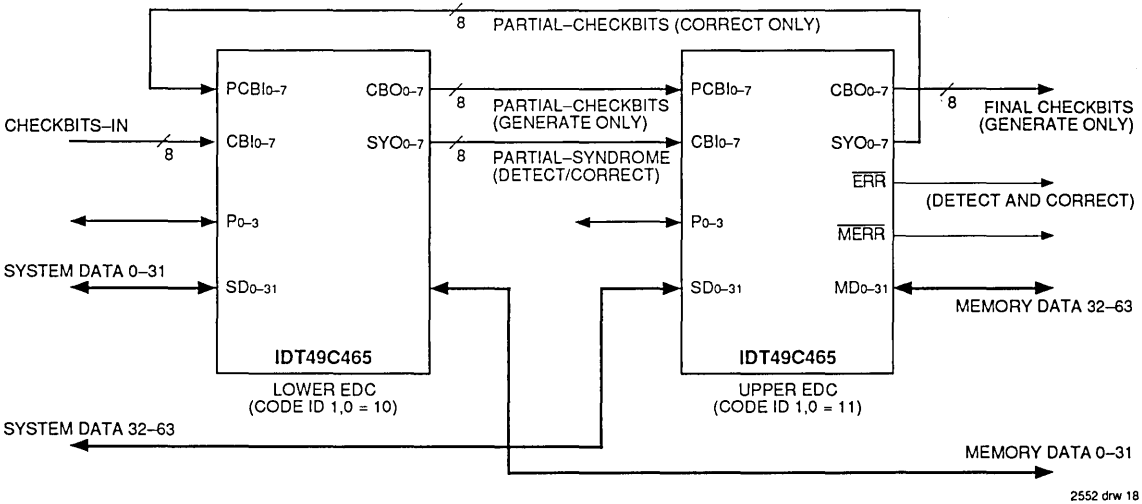
Syndrome bits are generated by an exclusive-OR of the generated checkbits with the checkbits read from memory. For example, Sn is the XOR of checkbits read and checkbits generated. During data correction, the syndrome bits are used to complement (correct) single-bit errors in the data bits. For double or multiple-bit error detection, the data available as output by the Pipeline Latch is not defined.

Critical AC performance data is provided in the Table "Key AC Calculations", which illustrates the delays that are critical to 64-bit cascaded performance. As indicated, a summation of propagation delays is required when cascading these units.

64-BIT DATA FORMAT



64-BIT HARDWARE CONFIGURATION



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DEFINITIONS OF TERMS:

$D_0 - D_{31}$ = System Data and/or Memory Data Inputs
$CBI_0 - CBI_7$ = Checkbit Inputs
$PCBI_0 - PCBI_7$ = Partial Checkbit Inputs
$FS_0 - FS_7$ = Final Internal Syndrome bits

FUNCTIONAL EQUATIONS:

The equations below describe the terms used in the IDT49C465 to determine the values of the partial checkbits, checkbits, partial syndromes and final internal syndromes. NOTE: All "⊕" symbols below represent the "EXCLUSIVE-OR" function.

$$PA = D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{20} \oplus D_{22} \oplus D_{24} \oplus D_{26} \oplus D_{28}$$

$$PB = D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{19} \oplus D_{20} \oplus D_{23} \oplus D_{25} \oplus D_{26} \oplus D_{29} \oplus D_{31}$$

$$PC = D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{16} \oplus D_{17} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{27} \oplus D_{28} \oplus D_{29}$$

$$PD = D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{14} \oplus D_{15} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{30} \oplus D_{31}$$

$$PE = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$$

$$PF = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$$

$$PG = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23}$$

$$PH_0 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$$

$$PH_1 = D_1 \oplus D_2 \oplus D_3 \oplus D_5 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{24} \oplus D_{25} \oplus D_{27} \oplus D_{30}$$

$$PH_2 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{20} \oplus D_{22} \oplus D_{23} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$$

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.

DETAILED DESCRIPTION — CHECKBIT AND SYNDROME GENERATION vs. CODE ID

LOGIC EQUATIONS FOR THE CBO OUTPUTS

Checkbit Generation	CODE ID 1,0		
	00	10	11
	Final Chkbits	Partial Checkbits	Final Checkbits
CBO_0	PH_0	PH_1	$PH_2 \oplus PCBI_0$
CBO_1	PA	PA	$PA \oplus PCBI_1$
CBO_2	$\overline{PB}$	$\overline{PB}$	$PB \oplus PCBI_2$
CBO_3	$\overline{PC}$	$\overline{PC}$	$PC \oplus PCBI_3$
CBO_4	PD	PD	$PD \oplus PCBI_4$
CBO_5	PE	PE	$PE \oplus PCBI_5$
CBO_6	PF	PF	$PF \oplus PCBI_6$
CBO_7	—	PF	$PG \oplus PCBI_7$

2552 tbl 07

LOGIC EQUATIONS FOR THE SYO OUTPUTS

Checkbit/ Syndrome Generation	CODE ID 1,0		
	00	10	11
	Final Syndrome	Partial Syndrome	Partial Checkbits
SYO0	PH0 ⊕ CBI0	PH1 ⊕ CBI0	PH2
SYO1	PA ⊕ CBI1	PA ⊕ CBI1	PA
SYO2	$\overline{PB}$ ⊕ CBI2	$\overline{PB}$ ⊕ CBI2	PB
SYO3	$\overline{PC}$ ⊕ CBI3	$\overline{PC}$ ⊕ CBI3	PC
SYO4	PD ⊕ CBI4	PD ⊕ CBI4	PD
SYO5	PE ⊕ CBI5	PE ⊕ CBI5	PE
SYO6	PF ⊕ CBI6	PF ⊕ CBI6	PF
SYO7	—	PF ⊕ CBI7	PG

2552 tbl 08

LOGIC EQUATIONS FOR THE FINAL SYNDROME (FSn)

Final Syndrome Generation	CODE ID 1,0	
	00	10, 11
	Final Syndrome	Final Internal Syndrome
FS_0	$PH_0 \oplus CBI_0$	PH_1 (L) ⊕ PH_2 (U) ⊕ CBI_0
FS_1	$PA \oplus CBI_1$	PA (L) ⊕ PA (U) ⊕ CBI_1
FS_2	$\overline{PB} \oplus CBI_2$	PB (L) ⊕ PB (U) ⊕ CBI_2
FS_3	$\overline{PC} \oplus CBI_3$	PC (L) ⊕ PC (U) ⊕ CBI_3
FS_4	$PD \oplus CBI_4$	PD (L)⊕ PD (U) ⊕ CBI_4
FS_5	$PE \oplus CBI_5$	PE (L) ⊕ PE (U) ⊕ CBI_5
FS_6	$PF \oplus CBI_6$	PF (L) ⊕ PF (U) ⊕ CBI_6
FS_7	—	PF (L) ⊕ PG (U)⊕ CBI_7

2552 tbl 09

32-BIT SYNDROME DECODE TO BIT-IN-ERROR (1)

					HEX	0	1	2	3	4	5	6	7
					S6	0	0	0	0	1	1	1	1
				Syndrome	S5	0	0	1	1	0	0	1	1
				Bits	S4	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0									
0	0	0	0	0		*	C4	C5	T	C6	T	T	30
1	0	0	0	1		C0	T	T	14	T	M	M	T
2	0	0	1	0		C1	T	T	M	T	2	24	T
3	0	0	1	1		T	18	8	T	M	T	T	M
4	0	1	0	0		C2	T	T	15	T	3	25	T
5	0	1	0	1		T	19	9	T	M	T	T	31
6	0	1	1	0		T	20	10	T	M	T	T	M
7	0	1	1	1		M	T	T	M	T	4	26	T
8	1	0	0	0		C3	T	T	M	T	5	27	T
9	1	0	0	1		T	21	11	T	M	T	T	M
A	1	0	1	0		T	22	12	T	1	T	T	M
B	1	0	1	1		17	T	T	M	T	6	28	T
C	1	1	0	0		T	23	13	T	M	T	T	M
D	1	1	0	1		M	T	T	M	T	7	29	T
E	1	1	1	0		16	T	T	M	T	M	M	T
F	1	1	1	1		T	M	M	T	0	T	T	M

NOTES: 2552 tbl 12

1. The table indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected. The all-zero case indicates no error detected.
   * = No errors detected
   # = The number of the single bit-in-error
   T = Two errors detected
   M = Three or more errors detected

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DETAILED DESCRIPTION — 32-BIT CONFIGURATION

32-BIT MODIFIED HAMMING CODE — CHECKBIT ENCODING CHART[1]

Generated Checkbits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	Even (XOR)	X				X		X	X	X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								

2552 tbl 10

Generated Checkbits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0	Even (XOR)		X	X	X		X					X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X

NOTE:

2552 tbl 11

1. The table indicates the data bits participating in the checkbit generation. For example, checkbit C0 is the Exclusive-OR function of the 16 data input bits marked with an X.

DETAILED DESCRIPTION — 64-BIT CONFIGURATION

64-BIT MODIFIED HAMMING CODE - CHECKBIT ENCODING CHART[1, 2]

Generated Checkbits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X			X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

2552 tbl 13

Generated Checkbits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)									X	X	X	X	X	X	X	X

2552 tbl 14

Generated Checkbits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)									X	X	X	X	X	X	X	X

2552 tbl 15

Generated Checkbits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

2552 tbl 16

NOTES:
1. The table indicates the data bits participating in the checkbit generation. For example, checkbit C0 is the Exclusive-OR function of the 32 data input bits marked with an X.
2. The checkbit is generated as either an XOR or an XNOR of the 32 data bits noted by an "X" in the table.

DETAILED DESCRIPTION — 64-BIT CONFIGURATION (Con't.)

32-BIT SYNDROME DECODE TO BIT-IN-ERROR(1)

				HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				S6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	Syndrome			S5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	Bits			S4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0																
0	0	0	0	0	*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1	C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0	C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1	T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0	C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1	T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0	T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1	M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0	C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1	T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0	T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1	17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0	T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1	M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0	16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1	T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES: 2552 tbl 17

1. The table indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected. The all-zero case indicates no error detected.
   * = No errors detected
   # = The number of the single bit-in-error
   T = Two errors detected
   M = Three or more detected

KEY AC CALCULATIONS — 64-BIT CASCADED CONFIGURATION

	64-Bit Propagation Delay		Total AC Delay for IDT49C465 in 64-bit Mode
Mode	From	To	(L) = Lower slice (U) = Upper slice
Generate	SD Bus	Checkbits out	SD to CBO(L) + PCBI to CBO(U) t SC(L) + t PCC(U)
Detect	MD Bus	$\overline{\text{ERROR}}$ for 64-bits	MD to SYO(L) + CBI to $\overline{\text{ERR}}$ (U) t MSY(L) + t CE (U)
	MD Bus	$\overline{\text{M ERROR}}$ for 64-bits	MD to SYO(L) + CBI to $\overline{\text{M ERR}}$ t MSY(L) + t CME (U)
Correct	MD Bus	Corrected data out	MD to SYO(L) + CBI to SD(U) t MSY(L) + t CS (U) (or) → MD to SYO(U) + PCBI to SD(L) t MSY(U) + t PCS(L)

NOTE: 2552 tbl 18

1. (or) = Whichever is worse.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{CC}	Power Supply Voltage	−0.5 to +7.0	−0.5 to +7.0	°C
V_{TERM}	Terminal Voltage with Respect to Ground	−0.5 to V_{CC} + 0.5	−0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
I_{OUT}	DC Output Current	30	30	mA

NOTE: 2552 tbl 19

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Ratings for extended periods of time may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2552 tbl 20

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)			Min.	Typ.(2)	Max.	Unit
V_{IH}	Input High Level(4)	Guaranteed Logic High	Normal Inputs		2.0	—	—	V
			Hysteresis Inputs		3.0	—	—	
V_{IL}	Input Low Level(4)	Guaranteed Logic Low			—	—	0.8	V
I_{IH}	Input High Current	V_{CC} = Max., V_{IN} = V_{CC}			—	—	5.0	µA
I_{IL}	Input Low Current	V_{CC} = Max., V_{IN} = GND			—	—	−5.0	µA
I_{OZ}	Off State (Hi-Z)	V_{CC} = Max.	V_O = 0V		—	—	−10	µA
			V_O = 3V		—	—	10	
I_{OS}	Short Circuit Current	V_{CC} = Max.(3)			−20	—	−100	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −6mA	COM'L.	2.0	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = −4mA	MIL.	2.4	—	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8mA	COM'L.	—	—	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 6mA	MIL.	—	—	0.5	
V_H	Hysteresis	$\overline{CLEAR}$, MLE, $\overline{PLE}$, SLE, $\overline{SYNCLK}$, $\overline{SCLKEN}$			—	200	—	mV

NOTES: 2552 tbl 21

1. For conditions shown as min. or max., use appropriate value specified above for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient temperature and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Con't.)

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%
$V_{HC} = V_{CC} - 0.2V$, $V_{LC} = V_{CC} + 0.2V$

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current CMOS Input Levels	$V_{IN} = V_{HC}$, $V_{IL} = V_{LC}$ V_{CC} = Max. All Inputs Outputs Disabled		—	—	5	mA
I_{CCQT}	Quiescent Power Supply Current TTL Input Levels	V_{IH} = 3.4V, V_{IL} = 0V V_{CC} = Max. All Inputs Outputs Disabled		—	—	160	mA
I_{CCD1}	Dynamic Power Supply Current f = 10MHz	f_{CP} = 10MHz, 50% Duty Cycle $V_{IH} = V_{HC}$, $V_{IL} = V_{LC}$ All Inputs, Outputs Disabled	COM'L.	—	—	230	mA
			MIL.	—	—	300	
I_{CCD2}	Dynamic Power Supply Current f = 20MHz	f_{CP} = 20MHz, 50% Duty Cycle $V_{IH} = V_{HC}$, $V_{IL} = V_{LC}$ All Inputs, Outputs Disabled	COM'L.	—	—	300	mA
			MIL.	—	—	350	

2552 tbl 22

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified above for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient temperature, and maximum loading.
3. Total supply current is the sum of the Quiescent current and the dynamic current and is calculated as follows:
   $I_{CCT} = I_{CCQC} (N_{QC}) + I_{CCQC} \times (N_{DC} \times D_C) + I_{CCDC} \times (N_{DC} \times f_{OP}) + I_{CCQT} (N_{QT}) + I_{CCQT} (N_{DT} \times D_T) + I_{CCDC} \times (N_{DC} \times f_{OP})$
   where: N_{DC} = Total # of dynamically switching CMOS inputs
   N_{DT} = Total # of dynamically switching TTL inputs
   N_{QC} = Total # of quiescent CMOS inputs
   N_{QT} = Total # of quiescent TTL inputs
   D_C = AC Duty cycle – % of time high (CMOS)
   D_T = AC Duty cycle – % of time high (TTL)
   f_{OP} = Operating frequency

AC PARAMETERS

PROPAGATION DELAY TIMES (PRELIMINARY)

Parameter Name	Parameter Description: From Input (edge)	Parameter Description: To Output (edge)	32-bit System Standalone Slice CODE ID=00 Com. Max.	32-bit System Standalone Slice CODE ID=00 Mil. Max.	64-bit "Generate only" Slice CODE ID=01 Com. Max.	64-bit "Generate only" Slice CODE ID=01 Mil. Max.	64-bit System Lower Slice CODE ID=10 Com. Max.	64-bit System Lower Slice CODE ID=10 Mil. Max.	64-bit System Upper Slice CODE ID=11 Com. Max.	64-bit System Upper Slice CODE ID=11 Mil. Max.	Unit	Refer to Timing Diagram Figure
GENERATE (WRITE) PARAMETERS												
t_{BC}	BEN	CBO	20	25	—	—	20	25	20	25	ns	—
t_{BM}	BEN	MDOUT	20	25	—	—	20	25	20	25	ns	—
t_{MC}	**MDIN**	**CBO**	—	—	**15**	**20**	—	—	—	—	ns	10
t_{PCC}	**PCBI**	**CBO**	—	—	—	—	—	—	**15**	**20**	ns	7
t_{PPE}	PXIN	PERR	15	20	—	—	15	20	15	20	ns	—
t_{SC}		**CBO**	**15**	**20**	**15**	**20**	**15**	**20**	**15**	**20**	ns	7
t_{SM}	**SDIN**	MDOUT	15	20	—	—	15	20	15	20	ns	7
t_{SPE}		PERR	15	20	—	—	15	20	15	20	ns	—
DETECT (READ) PARAMETERS												
t_{CE}		**ERROR** Low	15	20	—	—	—	—	**15**	**20**	ns	8,10
t_{CME}	**CBI**	MULT ERR=Low	20	24	—	—	—	—	20	24	ns	8,10
t_{CSY}		SYO	15	20	—	—	10	15	15	20	ns	8,10
t_{ME}		**ERROR**	**15**	**20**	—	—	—	—	15	20	ns	8,10
t_{MME}	**MDIN**	MULT ERR	20	24	—	—	—	—	20	24	ns	8,10
t_{MSY}		**SYO**	15	20	—	—	**10**	**15**	**15**	**20**	ns	8,10
CORRECT (READ) PARAMETERS												
t_{CS}	**CBI**	**SDOUT**	20	24	—	—	—	—	**20**	**24**	ns	8,11
t_{MP}		Px	30	36	—	—	30	36	30	36	ns	8,11
t_{MS}	**MDIN**	**SDOUT**	**20**	**25**	—	—	—	—	—	—	ns	8,11
t_{MSY}		**SYO**	15	20	—	—	10	**15**	**15**	**20**	ns	8,11
t_{PCS}	**PCBI**	**SDOUT**	—	—	—	—	**15**	**20**	—	—	ns	11
DIAGNOSTIC PARAMETERS												
t_{CLR}	CLEAR = Low	SDOUT	20	24	—	—	20	24	20	24	ns	15
t_{MIS}	MODE ID	SDOUT	20	24	—	—	20	24	20	24	ns	15

NOTES:
1. Where "edge" is not specified, both high and low edges are implied.
2. **BOLD** indicates critical system parameters.

2552 tbl 23

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AC PARAMETERS

PROPAGATION DELAY TIMES FROM LATCH ENABLES (PRELIMINARY)

Parameter Name	Parameter Description: From Input (edge)	To Output (edge)	Com.'l. Max.	Mil. Max.	Unit	Refer to Timing Diagram Figure
tMLC		CBO *	20	24	ns	13
tMLE		ERROR *	15	20	ns	8, 10, 11
tMLME	MLE = High	MULT ERR *	20	24	ns	8
tMLP		Px *	30	36	ns	8, 11
tMLS		SDOUT *	20	24	ns	8, 10, 11
tMLSY		SYO *	18	22	ns	8, 10
tPLS	$\overline{PLE}$ = Low	SDOUT *	10	12	ns	8, 11
tPLP	$\overline{PLE}$ = Low	Px *	20	22	ns	8, 11
tSLC	$\overline{SLE}$ = High	CBO *	20	24	ns	7, 9
tSLM	SLE = High	MDOUT *	15	20	ns	7, 9

NOTE: 2552 tbl 24

"*" = Both high and low edges are implied.

ENABLE AND DISABLE TIMES (PRELIMINARY)

Parameter Name	Parameter Description: From Input (edge)	To Output (edge)	Com'l. Min.	Com'l. Max.	Mil. Min.	Mil. Max.	Unit	Refer to Timing Diagram Figure
tBESZx	BEN = High	SDOUT *	2	15	1	18	ns	8, 10, 11
tBESxZ	Low	Hi – Z	—	15	—	18	ns	
tBEPZx	BEN = High	POUT *	2	15	1	18	ns	8, 11
tBEPxZ	Low	Hi – Z	—	15	—	18	ns	
tCECZx	$\overline{CBOE}$ = Low	CBO *	2	15	1	18	ns	7, 9
tCECxZ	High	Hi – Z	—	15	—	18	ns	
tMEMZx	$\overline{MOE}$ = Low	MDOUT *	2	15	1	18	ns	7, 9
tMEMxZ	High	Hi – Z	—	15	—	18	ns	8, 10
tSESZx	$\overline{SOE}$ = Low	SDOUT *	2	15	1	18	ns	8, 10
tSESxZ	High	Hi – Z	—	15	—	18	ns	7, 9

NOTE: 2552 tbl 25

"*" = Delay to both edges.

SET-UP AND HOLD TIMES (PRELIMINARY)

Parameter Name	Parameter Description: From Input (edge)	To Output (edge)	Com.'l. Min.	Mil. Min.	Unit	Refer to Timing Diagram Figure
tCMLS	CBI Set-up *	before MLE = Low	4	5	ns	8, 10, 11
tCMLH	CBI Hold *	after MLE = Low	4	5	ns	8, 10, 11
tMMLS	MDIN Set-up *	before MLE = Low	4	5	ns	8, 10, 11
tMMLH	MDIN Hold *	after MLE = Low	4	5	ns	8, 10, 11
tSSLS	SDIN Set-up *	before SLE = Low	4	5	ns	7, 9
tSSLH	SDIN Hold *	after SLE = Low	4	5	ns	7, 9
tCPLS	CBI Set-up *	before $\overline{PLE}$ = High	18	22	ns	—
tCPLH	CBI Hold *	after $\overline{PLE}$ = High	0	0	ns	—
tMPLS	MDIN Set-up *	before $\overline{PLE}$ = High	18	22	ns	—
tMPLH	MDIN Hold *	after $\overline{PLE}$ = High	0	0	ns	—
tPCPLS	PCBI Set-up *	before $\overline{PLE}$ = High	18	22	ns	—
tPCPLH	PCBI Hold *	after $\overline{PLE}$ = High	0	0	ns	—

DIAGNOSTIC SET-UP AND HOLD TIMES

tCSCS	CBI Set-up *		25	30	ns	15
tMSCS	MDIN Set-up *	before SYNCLK=High	25	30	ns	15
tMLSCS	MLE Set-up = High		25	30	ns	15
tSESCS	SCLKEN Set-up =Low		4	5	ns	15
tSESCH	SCLKEN Hold =Low	after SYNCLK =High	4	5	ns	15

NOTE:
"*" = Where "edge" is not specified, both high and low edges are implied.

2552 tbl 26

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MINIMUM PULSE WIDTH (PRELIMINARY)

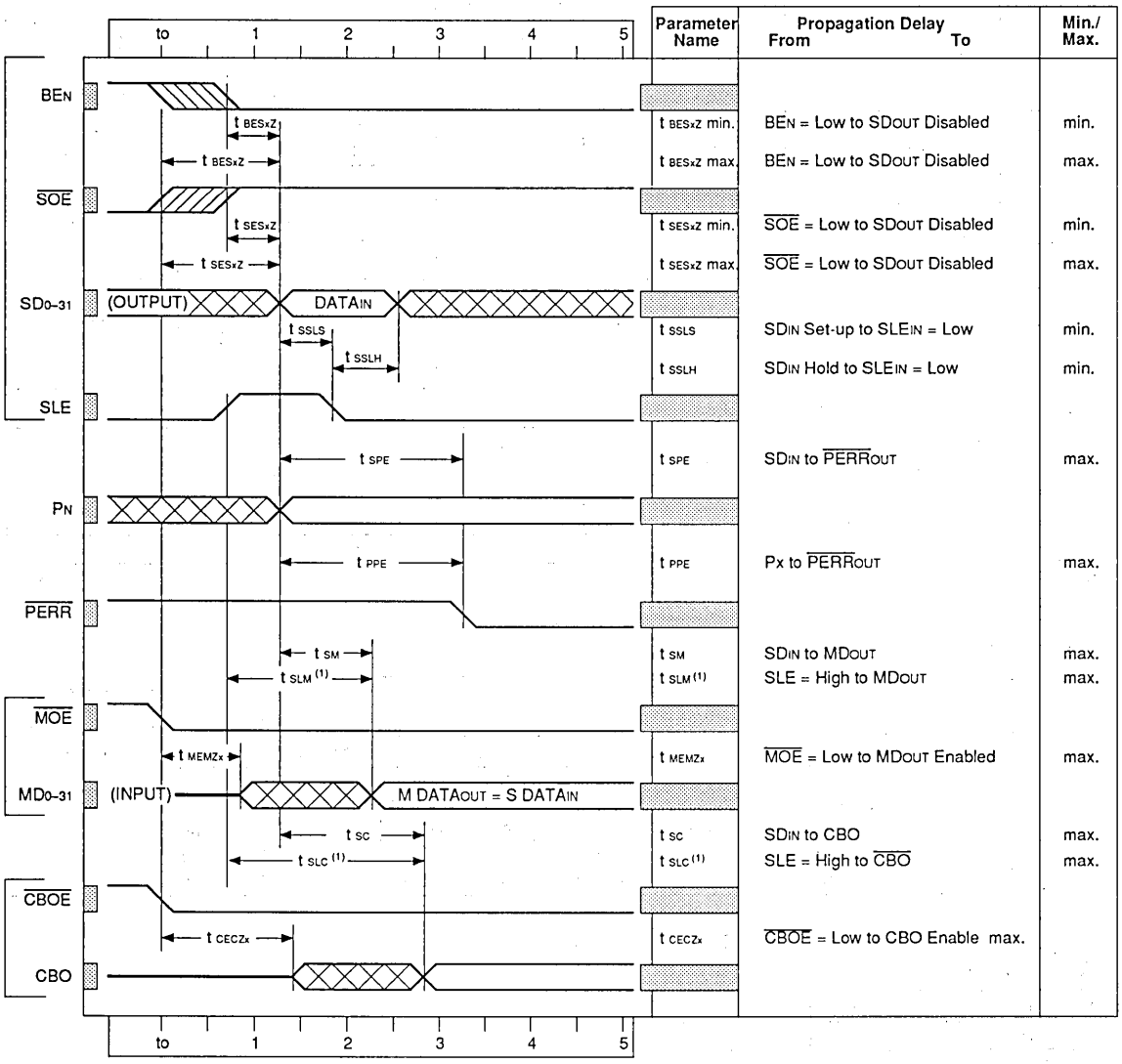
Parameter Name	Minimum Pulse Width Input		Conditions	Com'l. Min.	Mil. Min.	Unit	Refer to Timing Diagram Figure
tCLR	Min. $\overline{CLEAR}$ low time	to clear diag. registers	Data = Valid	5	6	ns	14
tMLE	Min. MLE high time	to strobe new data	MD, CBI = Valid	5	6	ns	—
tPLE	Min. $\overline{PLE}$ low time	to strobe new data	SD = Valid	5	6	ns	—
tSLE	Min. SLE high time	to strobe new data	SD = Valid	5	6	ns	—
tSYNCLK	Min. SYNCLK high time	to clock in new data	SCKEN = Low	5	6	ns	14

2552 tbl 27

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 18

2552 tbl 28

AC TIMING DIAGRAMS — 32-BIT CONFIGURATION

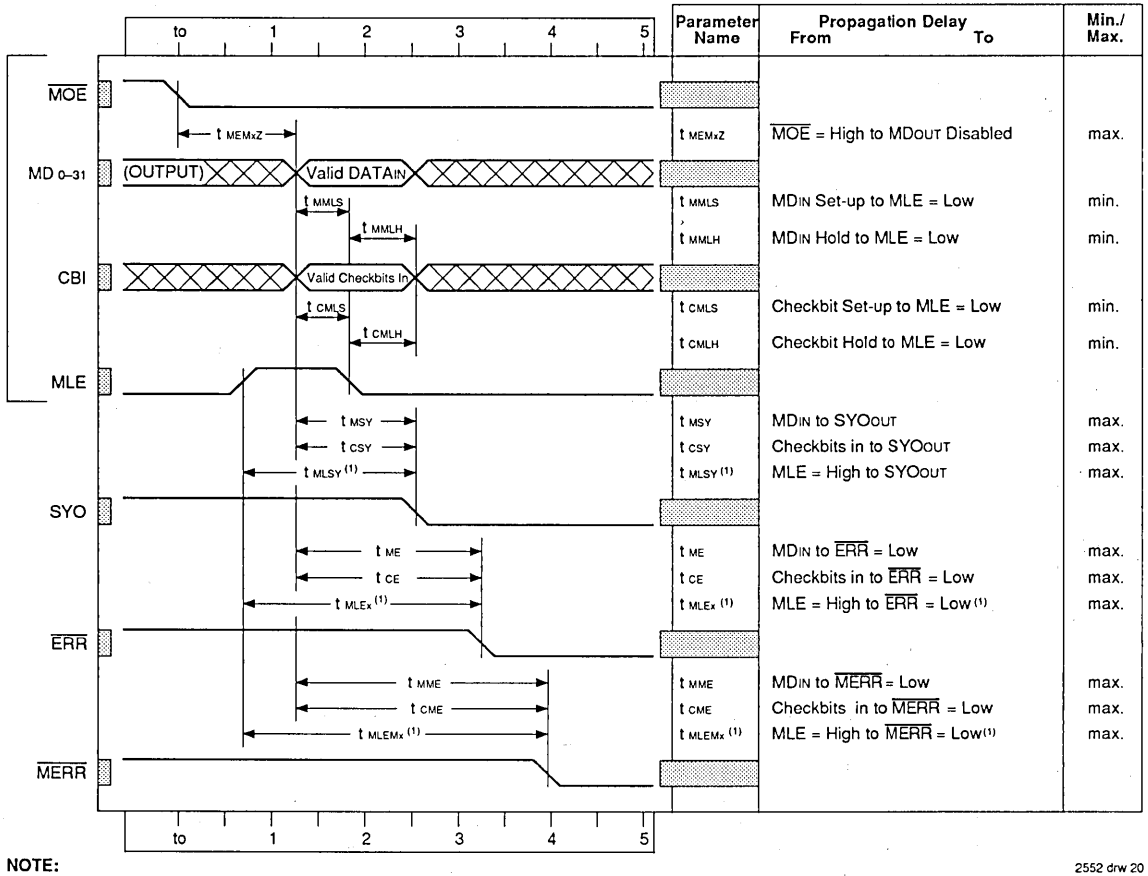


NOTE:
1. Assumes that System Data is valid at least 4ns before SLE goes high.

2552 drw 19

Figure 7. 32-Bit Generate Timing

AC TIMING DIAGRAMS — 32-BIT CONFIGURATION



Parameter Name	Propagation Delay From	To	Min./ Max.
t MEMxZ	$\overline{MOE}$ = High to MDOUT Disabled		max.
t MMLS	MDIN Set-up to MLE = Low		min.
t MMLH	MDIN Hold to MLE = Low		min.
t CMLS	Checkbit Set-up to MLE = Low		min.
t CMLH	Checkbit Hold to MLE = Low		min.
t MSY	MDIN to SYOOUT		max.
t CSY	Checkbits in to SYOOUT		max.
t MLSY (1)	MLE = High to SYOOUT		max.
t ME	MDIN to $\overline{ERR}$ = Low		max.
t CE	Checkbits in to $\overline{ERR}$ = Low		max.
t MLEx (1)	MLE = High to $\overline{ERR}$ = Low (1)		max.
t MME	MDIN to $\overline{MERR}$ = Low		max.
t CME	Checkbits in to $\overline{MERR}$ = Low		max.
t MLEMx (1)	MLE = High to $\overline{MERR}$ = Low (1)		max.

NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 4ns before MLE goes high.

2552 drw 20

Figure 8. 32-Bit Detect Timing

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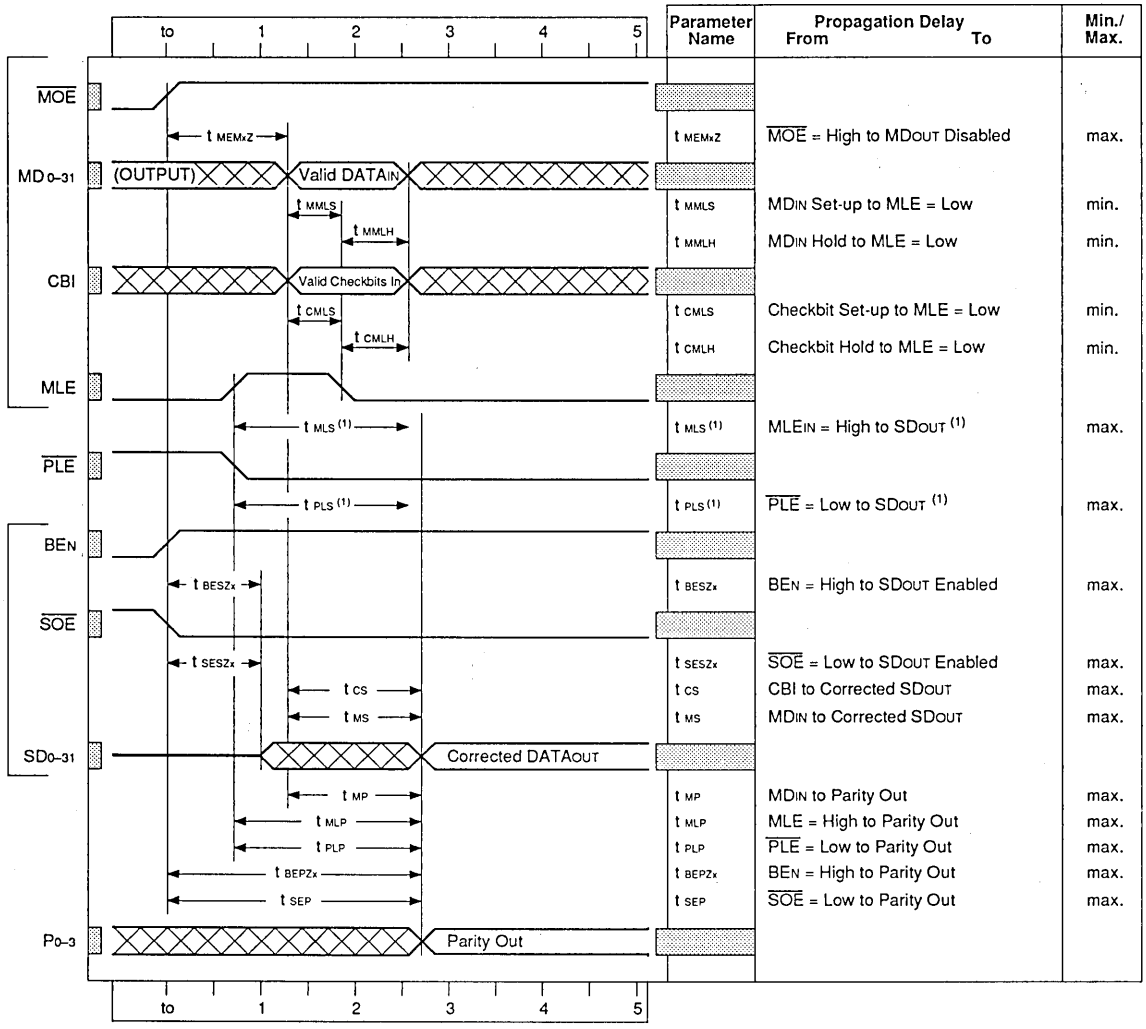
AC TIMING DIAGRAMS — 32-BIT CONFIGURATION



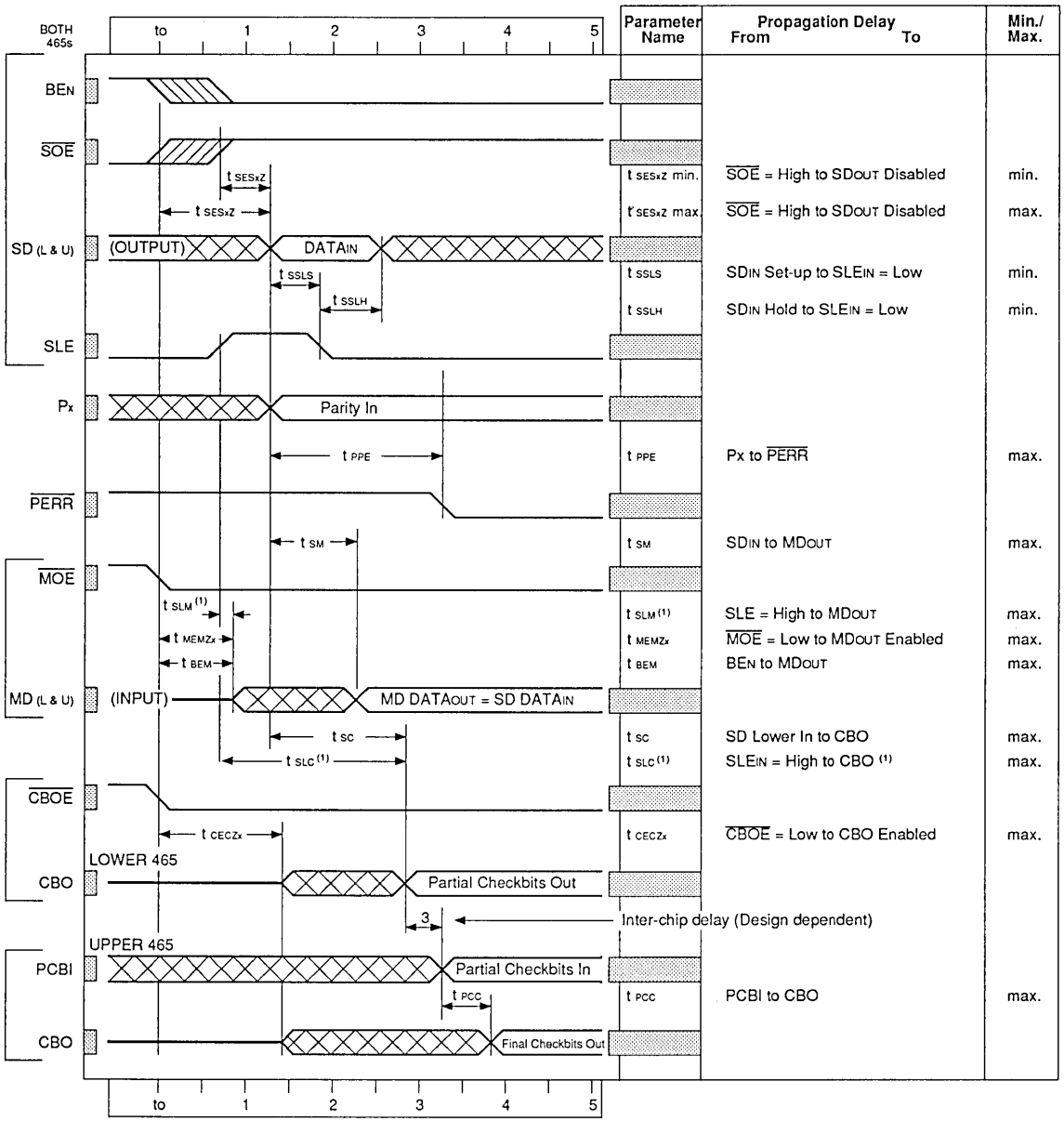
Parameter Name	Propagation Delay From To	Min./ Max.
t MEMxZ	$\overline{MOE}$ = High to MDOUT Disabled	max.
t MMLS	MDIN Set-up to MLE = Low	min.
t MMLH	MDIN Hold to MLE = Low	min.
t CMLS	Checkbit Set-up to MLE = Low	min.
t CMLH	Checkbit Hold to MLE = Low	min.
t MLS (1)	MLEIN = High to SDOUT (1)	max.
t PLS (1)	$\overline{PLE}$ = Low to SDOUT (1)	max.
t BESZx	BEN = High to SDOUT Enabled	max.
t SESZx	$\overline{SOE}$ = Low to SDOUT Enabled	max.
t CS	CBI to Corrected SDOUT	max.
t MS	MDIN to Corrected SDOUT	max.
t MP	MDIN to Parity Out	max.
t MLP	MLE = High to Parity Out	max.
t PLP	$\overline{PLE}$ = Low to Parity Out	max.
t BEPZx	BEN = High to Parity Out	max.
t SEP	$\overline{SOE}$ = Low to Parity Out	max.

NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 4ns before MLE goes high.

2552 drw 21

Figure 9. 32-Bit Correct Timing

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION

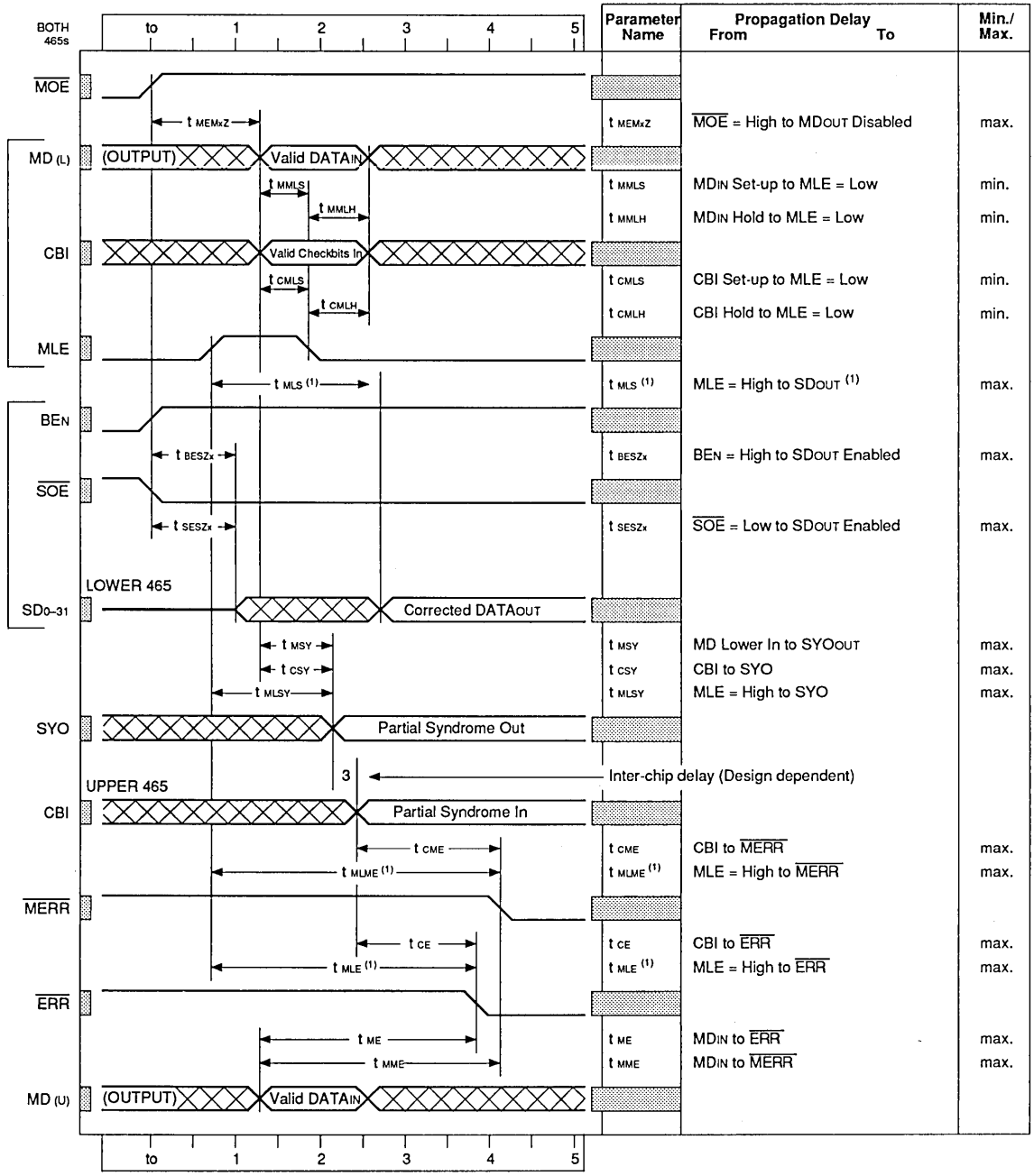


NOTE:
1. Assumes that System Data is valid at least 4ns before SLE goes high.

2552 drw 22

Figure 10. 64-Bit Generate Timing — (64-Bit Cascading System)

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION

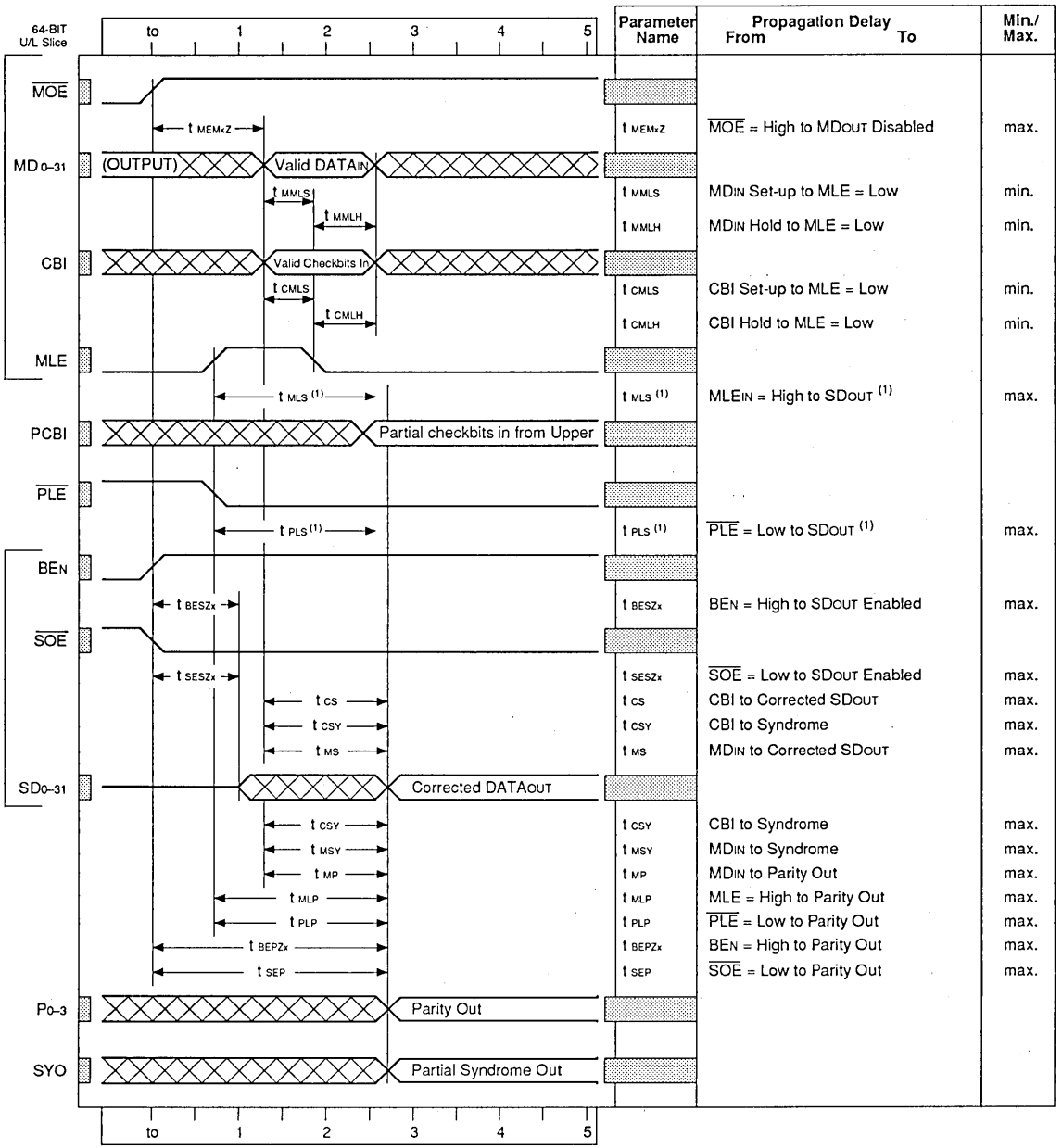


NOTE:
1. Assumes that System Data is valid at least 4ns before SLE goes high.

2552 drw 23

Figure 11. 64-Bit Detect Timing

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION



Parameter Name	Propagation Delay From To	Min./ Max.
t MEMxZ	$\overline{MOE}$ = High to MDOUT Disabled	max.
t MMLS	MDIN Set-up to MLE = Low	min.
t MMLH	MDIN Hold to MLE = Low	min.
t CMLS	CBI Set-up to MLE = Low	min.
t CMLH	CBI Hold to MLE = Low	min.
t MLS (1)	MLEIN = High to SDOUT (1)	max.
t PLS (1)	$\overline{PLE}$ = Low to SDOUT (1)	max.
t BESZx	BEN = High to SDOUT Enabled	max.
t SESZx	$\overline{SOE}$ = Low to SDOUT Enabled	max.
t CS	CBI to Corrected SDOUT	max.
t CSY	CBI to Syndrome	max.
t MS	MDIN to Corrected SDOUT	max.
t CSY	CBI to Syndrome	max.
t MSY	MDIN to Syndrome	max.
t MP	MDIN to Parity Out	max.
t MLP	MLE = High to Parity Out	max.
t PLP	$\overline{PLE}$ = Low to Parity Out	max.
t BEPZx	BEN = High to Parity Out	max.
t SEP	$\overline{SOE}$ = Low to Parity Out	max.

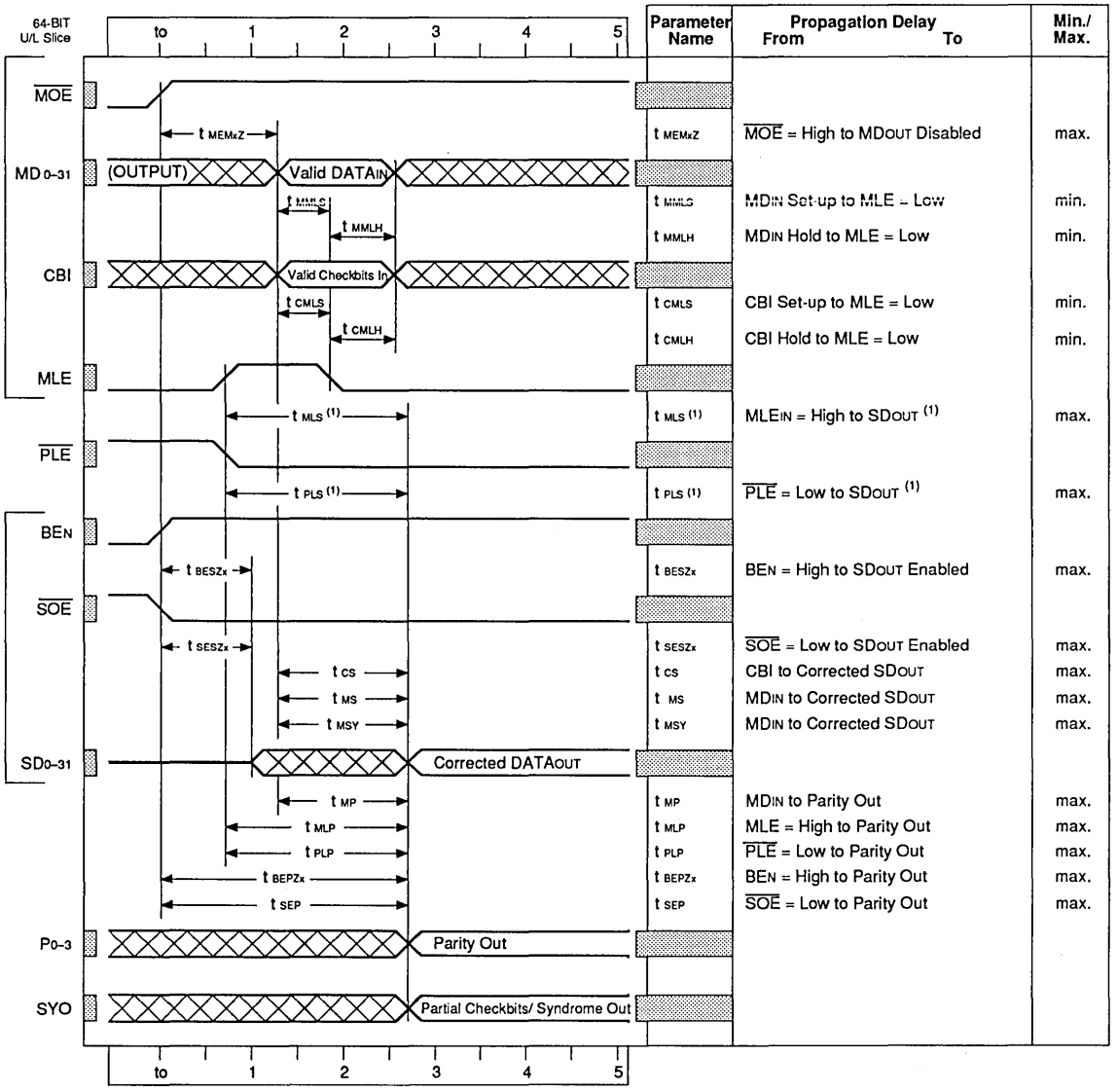
NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 4ns before MLE goes high.

2552 drw 24

Figure 12. 64-Bit Correct Timing (Lower Slice)

5

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION

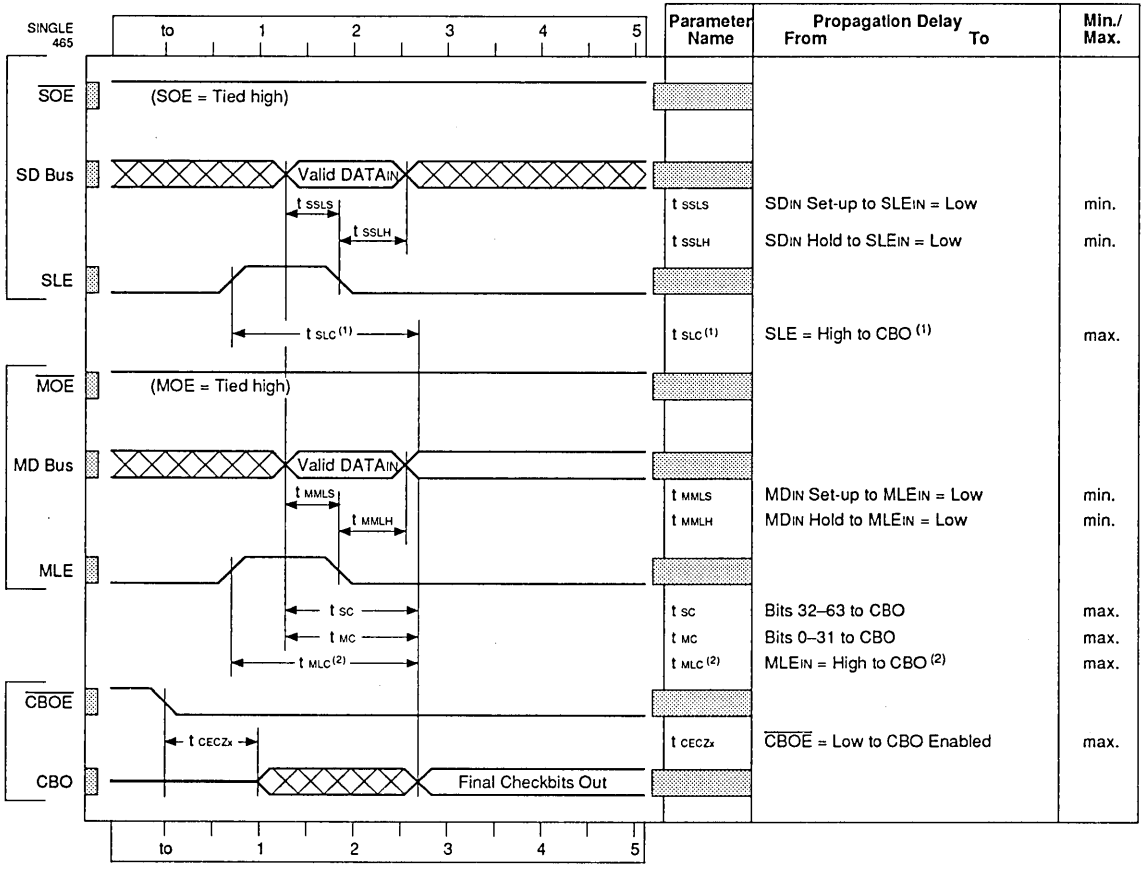


NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 4ns before MLE goes high.

2552 drw 25

Figure 13. 64-Bit Correct Timing (Upper Slice)

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION



NOTE:
1. Assumes that System Data is valid at least 4ns before SLE goes high.
2. Assumes that Memory Data is valid at least 4ns before MLE goes high.

2552 drw 26

Figure 14. 64-Bit Single Chip "Generate Only" Timing

5

AC TIMING DIAGRAMS — DIAGNOSTIC TIMING

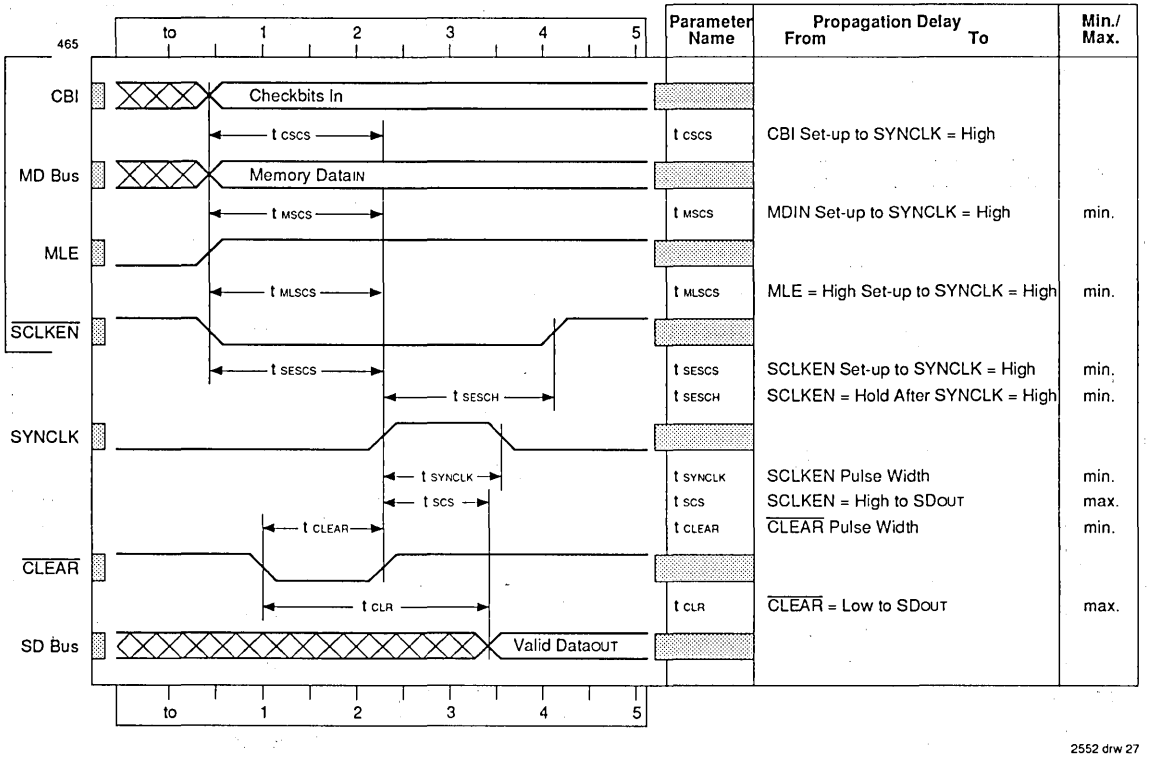


Figure 15. 32-Bit Diagnostic Timing

INPUT/OUTPUT INTERFACE CIRCUITS

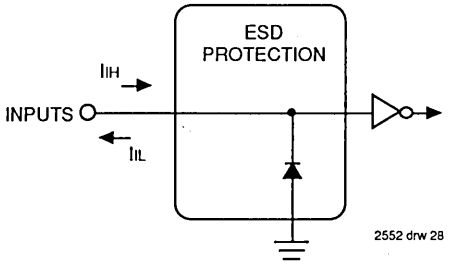


Figure 16. Input Structure (All Inputs)

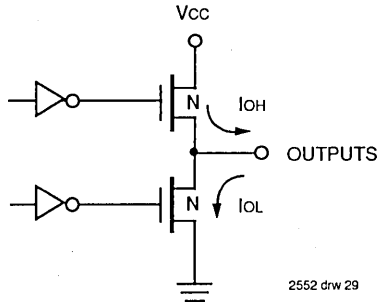
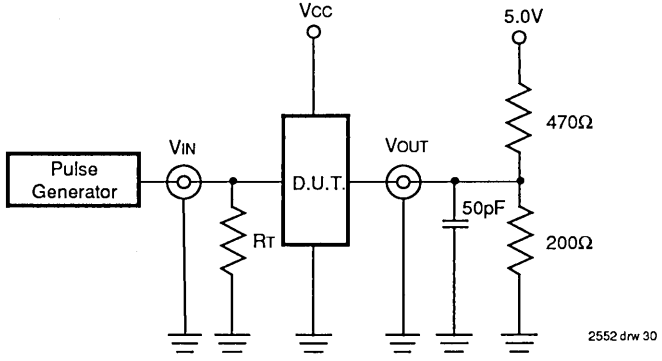


Figure 17. Output Structure

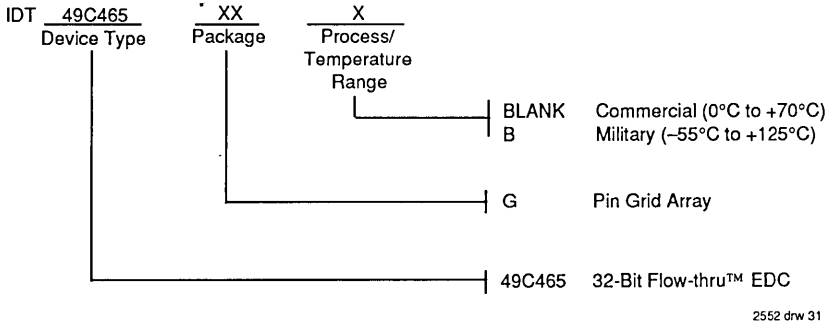
AC TEST CIRCUIT



DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance
RL = Termination resistance: should be equal to ZOUT of the Pulse Generator

Figure 18.

ORDERING INFORMATION



Integrated Device Technology, Inc.

Flow-thruEDC™ ERROR DETECTION AND CORRECTION UNIT

ADVANCE INFORMATION
IDT49C466

FEATURES:

- 64-bit wide Flow-thruEDC Error Detection and Correction Unit
- Separate System and Memory Data Input/Output Buses
- 64-bit Error Detect Time - 20ns;
  Error Correct Time - 25ns
- Corrects all single bit errors; Detects all double bit errors
- Configurable 16-deep system bus read/write buffer with flag indicators
- Simultaneous check bit generation and data correction of memory data
- Supports partial word writes on byte boundaries
- 8mA output drive current to drive small memory arrays directly
- Sophisticated error diagnostics and error logging
- Parity generation on system data bus
- 208 pin Pin Grid Array and Plastic Quad Flatpack (PQFP)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C466 64-bit Flow-thruEDC is a high speed error detection and correction unit to ensure data integrity in high reliability memory systems. The flow-thru architecture with separate system and memory data buses is ideally suited for pipelined memory systems.

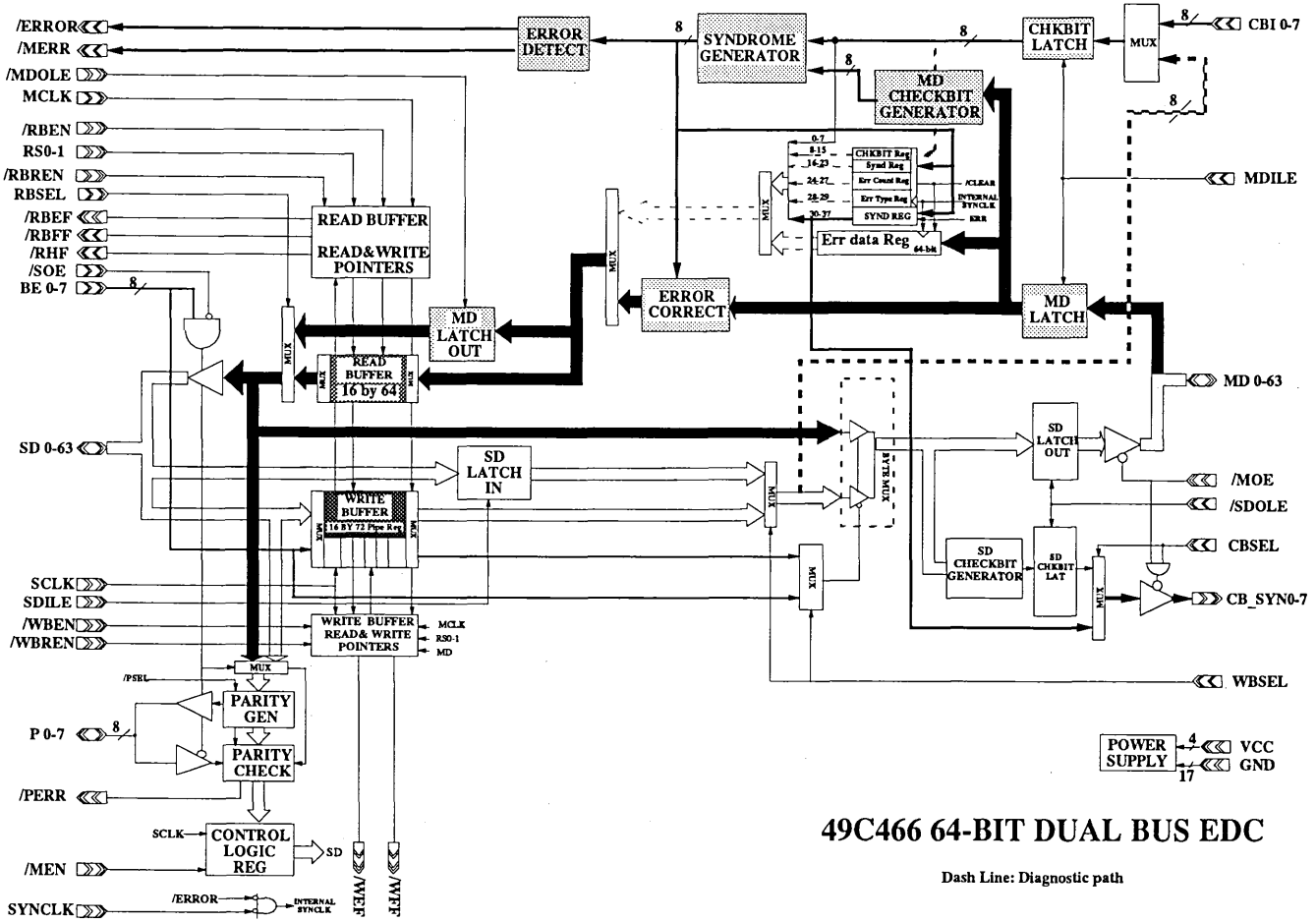
Implementing a Hamming code in the 8-bit wide check bit bus, the IDT49C466 corrects all single bit hard and soft errors, and detects all double bit errors. The read/write buffer can store up to sixteen 64-bit words until the system bus is ready (during reads) or until the system bus is released (during writes). Full and empty flags indicate whether additional data can be written to the EDC.

The simultaneous check bit generation and data correction of memory data eliminates the separate correction and generation modes found on other EDC units. Check bit generation for partial word writes on byte boundaries is supported on the IDT49C466.

Diagnostics features include a syndrome latch from which the error bit can be decoded, a four bit error counter which counts up to 15 errors, and an error data latch which stores the complete error data word. Parity can be generated and checked on the system bus by the IDT49C466.

Military product is available compliant with the latest revision of MIL-STD-883, Class B, for those systems operating in extreme environments.

Flow-thruEDC is a trademark of Integrated Device Technology Inc.



49C466 64-BIT DUAL BUS EDC

Dash Line: Diagnostic path

EDC IDT49C466 007

PIN CONFIGURATION

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	
17	MD_10	MD_8	MD_2	MD_1	MERRORB	CBIN_6	CBIN_1	RBENB	RBSEL	RBHFB	SD_2	SD_3	BE0	SD_9	SD_10	SD_12	SD_15	17
16	MD_13	MD_9	MD_6	MD_3	ERRORB	CBIN_3	CBIN_2	RBRENB	RBEFB	RBFFB	SD_1	SD_4	SD_6	SD_8	SD_13	SD_16	SD_17	16
15	MD_17	MD_12	MD_11	MD_5	MD_4	CBIN_7	CBIN_4	CBIN_0	GND_Q	SD_0	P0	SD_7	P1	BE1	SD_14	SD_19	SD_21	15
14	MD_18	MD_19	MD_15	GND_N	MD_7	MD_0	CBIN_5	GND_N	VCC_Q	GND_N	SD_5	SD_11	GND_N	GND_N	P2	BE2	SD_20	14
13	MD_23	MD_20	MD_14	VCC_N										SD_18	SD_22	SD_24	SD_25	13
12	MD_25	MD_22	MD_21	MD_16										SD_23	SD_26	SD_28	SD_27	12
11	MD_27	MD_28	MD_24	GND_N										P3	BE3	SD_30	SD_29	11
10	MD_31	MD_30	MD_29	MD_26										SD_31	SOEB	SDILE	SCLK	10
9	MOLEB	MOEB	MILE	GND_N				G208-1						MDOLEB	GND_N	MENB	RS_0	9
8	MD_33	MD_32	MD_34	MD_35										GND_N	SD_33	MCLK	RS_1	8
7	MD_37	MD_36	MD_39	MD_40										SD_37	SD_34	SD_32	PERRB	7
6	MD_41	MD_38	MD_42	MD_45										SD_42	SD_38	P4	SD_35	6
5	MD_43	MD_44	MD_46	MD_52										GND_N	P5	BE4	SD_36	5
4	MD_48	MD_49	MD_50	GND_N	GND_N	MD_61	CBO_4	VCC_2	GND_N	SD_61	GND_N	SD_54	SD_49	VCC_N	SD_43	SD_39	SD_40	4
3	MD_47	MD_51	MD_56	MD_60	MD-59	CBO_6	GND_N	GND_Q	WBENB	SD_62	SD_59	SD_57	SD_53	SD_51	SD_45	SD_44	SD_41	3
2	MD_53	MD_54	MD_57	CBO_7	CBO_5	CBO_2	CBO_0	WBRENB	SYNCLK	WBEFB	SD_60	BE7	SD_55	BE6	SD_50	SD_47	BE5	2
1	MD_55	MD_58	MD_62	MD_63	CBO_3	CBO_1	WBSEL	SYNSEL	WBFFB	SD_63	P7	SD_58	SD_56	P6	SD_52	SD_48	SD_46	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	

Pin 1 reference

PIN DESCRIPTION

Pin Name	I/O	Description
Data Buses		
SD_{0-63}	I/O	System Data Bus is a bidirectional 64-bit bus interfacing to the system or CPU. When System Output Enable, $\overline{SOE}$, is high or Byte Enable, BE_{0-7}, is low, data is input. The data is latched into the system data (SD) latch when the System Data Input Latch Enable (SDILE) is low. The System Data Bus is an output of the corrected memory data during a read operation. Corrected data can come from the memory data (MD) output latch or the content of the read buffer. When the Read Buffer Select (RDSEL) pin is low, the MD latch is selected. When RDSEL is high, the read buffer contents are selected. When System Output Enable, $\overline{SOE}$, is low and Byte Enable, BE_{0-7}, is high, the SD bus output drivers are enabled.
MD_{0-63}	I/O	Memory Data Bus is a bidirectional 64-bit bus interfacing to the memory. During a read cycle, memory data is input for error detection and correction. The data is latched in the memory data (MD) input latch when the Memory Data Input Latch Enable (MDILE) is low. Data from the SD output latch or the read buffer is is output on the Memory Data Bus on a memory write cycle.
CBI_{0-7}	I	Check Bit Inputs interface to the check bit memory.
$\overline{CBSYN}_{0-7}$	I	Check Bit or Syndrome Output, when $\overline{MOE}$ is low, is enabled. When CBSEL is high, the check bits are selected. When CBSEL is low, the syndrome bits are selected.
P_{0-7}	I/O	Parity input/output for bytes 0 to 7. Byte parity is generated from the system data bus data word and output on the P_{0-7} pins. These pins are parity inputs when the corresponding Byte Enable (BE) is low, and are used to generate the parity error signal ($\overline{PERR}$). The parity select bit (PSEL) of the mode register selects odd or even parity.
Control Inputs		
$\overline{SOE}$	I	System Output Enable enables system data output drivers if the corresponding Byte Enable (BE_{0-7}) is high.
BE_{0-7}	I	Byte Enable is used to enable the System Data outputs for a particular byte in systems using separate I/I memories. For example, if BE_1 is high, the System data outputs for byte 1 (SD_{8-15}) are enabled. In systems using common I/O memories, the BE_{0-7} pins also control the data byte mux. If a particular BE is high, data is feed back to the memory data bus and used for check bit generation of that byte. This is used during partial word write operations and rewriting corrected data to the memory. If a particular BE is low, data from the system data latch is directed to the memory data bus and used for check bit generation of that byte, used in writing new data during a partial word write operation. BE is buffered with the data in the write buffer.
$\overline{MOE}$	I	Memory Output Enable, when low, enables the output buffers of the memory data bus (MD) and the check bit output bus (CBO).
MILE	I	Memory Input Latch Enable on the high to low transition latches data at the MD inputs and the checkbits at the CBI inputs. The latch is transparent when MILE is high.
$\overline{MOLE}$	I	Memory Output Latch Enable latches both the data at the output of the byte mux and the output of the checkbit generator on the low to high transition of $\overline{MOLE}$. The latch is transparent when $\overline{MOLE}$ is low.
WBSEL	I	Write Buffer Select, when high, the output of the write buffer is selected. The WBSEL is low, the SD input latch is selected.
SDILE	I	System Data Input Latch Enable latches data on the system data bus (SD) into the SD input latch on the low to high transition. When SDILE is high, the SD input latch is transparent.
$\overline{WBEN}$	I	Write Buffer Enable allows system data (SD) input to be written to the write buffer.
$\overline{WBREN}$	I	Write Buffer Read Enable, when low, the output of the write buffer is enabled.
RS_{0-1}	I	Reset and FIFO Select pins set both read and write buffer FIFOs. RS_{0-1} Function 00 Reset 16-deep FIFO or first 8-deep FIFO 10 Reset second 8-deep FIFO 01 Select 16-deep FIFO or first 8-deep FIFO 11 Select second 8-deep FIFO
RBSEL	I	Read Buffer Select when high the output of the read buffer is selected. When low, the MD latch output is selected.

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5

PIN DESCRIPTION (Cont.'d)

Pin Name	I/O	Description
$\overline{RBEN}$	I	Read Buffer Enable when low allows data to be written into the read buffer on the low to high transition of the memory clock.
$\overline{RBREN}$	I	Read Buffer Enable, when low, the output of the read buffer is selected.
CBSEL	I	Checkbit Select, when high, selects the checkbits at the $\overline{CB}SYN_{0-7}$ output. When CBSEL is low, the syndrome bits are selected.
Clock Inputs		
MCLK	I	Memory Clock. On the low to high transition of MCLK, data is written to the read buffer when $\overline{RBEN}$ is low.
SCLK	I	System Clock. On the low to high transition of the system clock, data is read from the read buffer when $\overline{RBREN}$ is low. Data on the system data bus is written into the write buffer when $\overline{WBEN}$ is low on the low to high transition of SCLK.
Status Outputs		
$\overline{WBEF}$	O	Write Buffer Empty Flag, when Low, indicates that there is only one more data word at the output of the write buffer. Further read operations are then inhibited. At reset, the $\overline{WBEF}$ is set low.
$\overline{WBFF}$	O	Write Buffer Full Flag, when low, inhibits further write operations to the buffer and indicates that the write buffer is full. After a reset, $\overline{WBFF}$ is high, and remains high until for 16 consecutive write operations without any read operations in the 16-deep configuration; or 8 consecutive write operations in the dual 8-deep configuration.
$\overline{RBEF}$	O	Read Buffer Empty Flag, when low, indicates that there is only one more data word at the output of the read buffer. Further read operations are then inhibited. At reset, the $\overline{RBEF}$ is set low.
$\overline{RBHF}$	O	Read Buffer Half-full Flag, when low, indicates that there are eight or more data words (in the 16-deep configuration) or four or more data words (in the dual 8-deep configuration) in the read buffer. The flag will return high when less than eight (or four) data words are in the buffer.
$\overline{RBFF}$	O	Read Buffer Full Flag, when low, inhibits further write operations to the buffer and indicates that the read buffer is full. After a reset, RBFF is high, and remains high until for 16 consecutive write operations without any read operations in the 16-deep configuration; or 8 consecutive write operations in the dual 8-deep configuration.
$\overline{ERR}$	O	Error Flag. In normal mode (Mode 3), when $\overline{ERR}$ is low, a data error is indicated. The $\overline{ERR}$ is not latched internally.
$\overline{MERR}$	O	Multiple Error. In normal mode (Mode 3), when $\overline{MERR}$ is low, a multiple data error is indicated. The $\overline{MERR}$ is not latched internally.
$\overline{PERR}$	O	Parity Error. Parity error signal, when low, indicates a parity error on the system data bus input.
Power Supply		
V_{CC}	P	Power Supply Voltage, +5 volts.
GND	P	Ground.

2617 tbl 01

Integrated Device Technology, Inc.

CMOS SINGLE 8-BIT PaletteDAC™ FOR TRUE COLOR APPLICATIONS

PRELIMINARY
IDT75C457

FEATURES

- 165/135/125/110/80 MHz operating speeds
- Pin- and function-compatible with Brooktree Bt 457
- Fixed pipeline delay: No external circuitry required
- 50ns read access time
- Integral and differential linearity < 1/2 LSB
- Single 8-bit DAC
- 256 x 8 Dual-Ported Color Palette RAM
- 4 x 8 Dual-Ported Overlay Palette RAM
- Multiplexed TTL pixel and overlay inputs
- RS-343A compatible output
- Single 5 volt power supply
- 84-pin PGA and PLCC packages
- Typical power dissipation: 1000mW
- CEMOS™ Monolithic construction
- Military product is compliant with MIL-STD-883, Class B

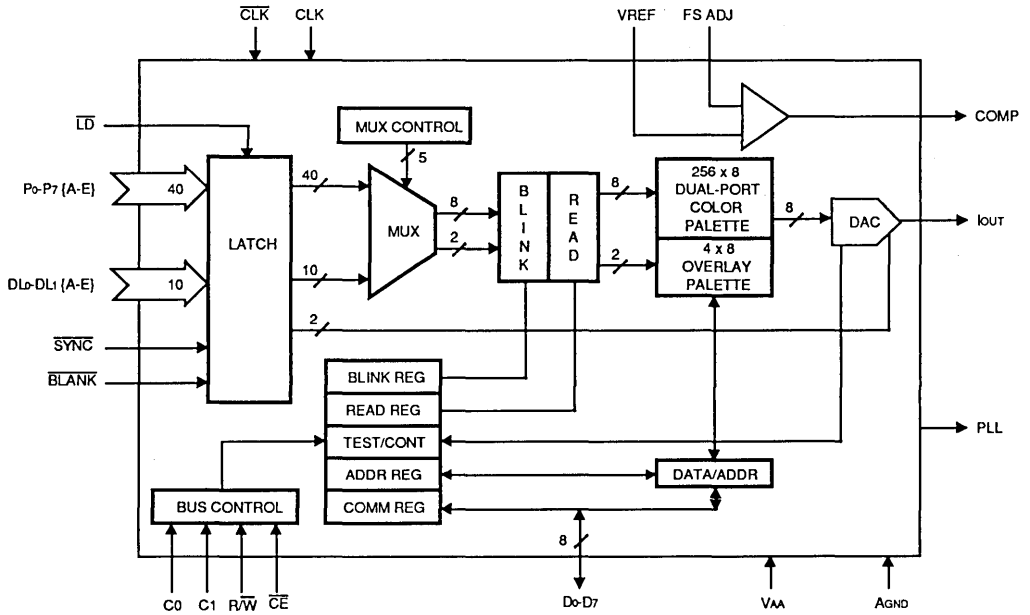
DESCRIPTION

The IDT75C457 is a single channel 8-bit video DAC with on-chip, dual-ported color palette memory. This chip is specifically designed for the display of true-color, high resolution graphics. The architecture eliminates the ECL pixel interface by providing multiple TTL-compatible pixel ports and by multiplexing the pixel data on-chip.

Features included on-chip are programmable blink rates, bit plane masking and blinking, as well as color overlay capability. The IDT75C457 generates an RS-343A compatible video output that is capable of driving a doubly terminated 75 ohm coaxial cable directly. A PLL current output enables synchronization of three IDT75C457s, thus allowing display of true-color images.

The IDT75C457 military PaletteDACs are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest levels of performance and reliability.

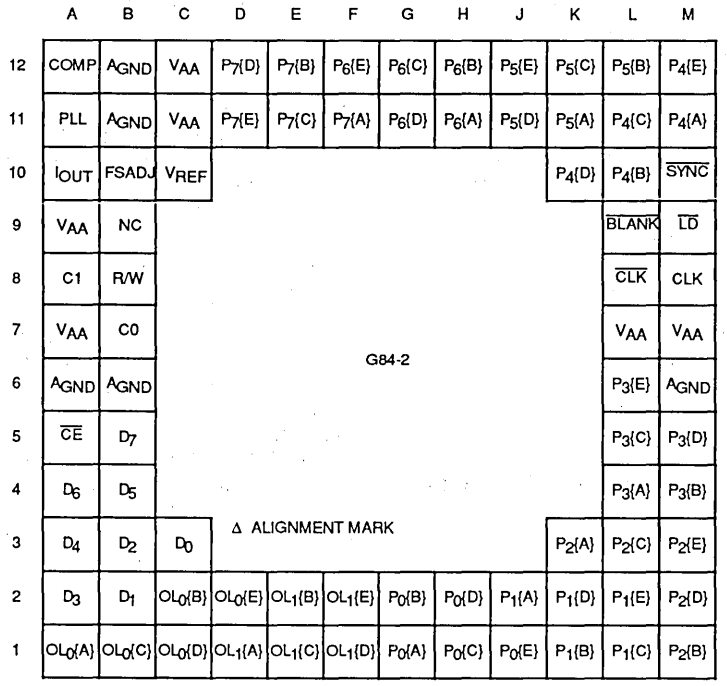
FUNCTIONAL BLOCK DIAGRAM



2523 drw 01

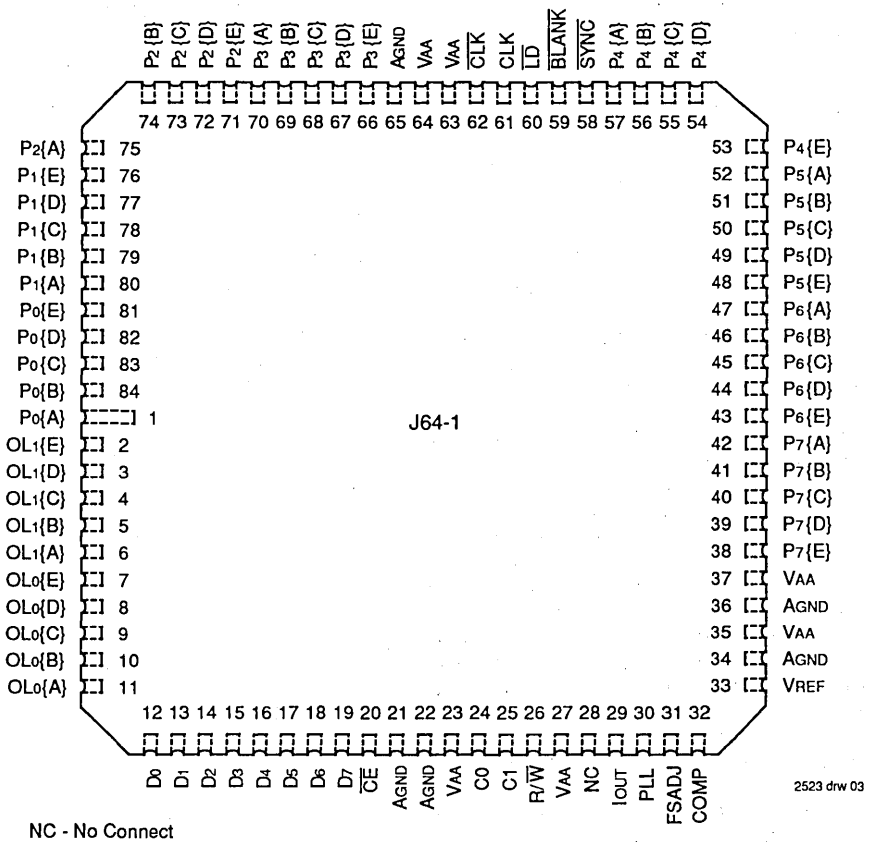
CEMOS and PaletteDAC are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



PGA
TOP VIEW

2523 drw 02



NC - No Connect

PLCC
TOP VIEW

GENERAL INFORMATION

The IDT75C457 triple 8-bit PaletteDAC is a highly integrated building block which interfaces a relatively low bandwidth frame buffer memory to analog RS-343A high bandwidth output.

The IDT75C457 includes a look-up table for updating color information and other graphics applications. The basic functional blocks are the microprocessor bus interface, the frame buffer memory interface and multiplexer, a dual-port RAM with one R/$\overline{W}$ port, one high-speed R/O port and one 8-bit video speed DAC.

MICROPROCESSOR BUS INTERFACE

The IDT75C457 supports a standard microprocessor bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and overlay registers allow color updating without contention with the display refresh process.

The bus interface consists of eight bidirectional data pins, D_0-D_7, with two control inputs, C0 and C1, a read/write direction input, R/$\overline{W}$, and a clock input, $\overline{CE}$. All data and control information are latched on the falling edge of $\overline{CE}$, as shown in Figure 3. All accesses to the chip are controlled by the data in the address register combined with the control inputs C0, C1 and R/$\overline{W}$, depicted in the Truth Table (Table 1).

An access to a control register requires writing a 4 through 7 into the address register (C0 = C1 = 0) and then writing or reading data to the selected register (C0 = 0, C1 = 1). When accessing the control registers, the address register is not changed, facilitating read-modify-write operations. If an invalid address is loaded into the address register, data written is ignored or invalid data is read out.

It is also possible to access the color palette information. The palette is organized as 256 address with 8 bits of red, blue or green information. Additionally, there are two extra addresses assigned to overlay information, yielding a total memory size of 260 x 8.

There are two modes of accessing palette entries on the IDT75C457, "Normal", and "RGB".

In Normal mode, writing color data entails the MPU loading the address register with the address of the color palette location or the overlay palette location to be modified. The MPU performs a color write cycle, using C0 and C1 to select either the color palette or the overlay palette. The address register then increments to the next address location which the MPU may modify simply by writing another color. Reading color data is similar to writing, except the MPU executes read cycles.

Normal mode is useful if a 24-bit data bus is available, as 24 bits of color information (eight bits each of red, green, and blue) may be read or written to three IDT75C457s in a single MPU cycle. In this application the $\overline{CE}$ inputs of all three IDT75C457s are connected together. If only an eight-bit data bus is available, the $\overline{CE}$ inputs must be individually selected during the appropriate color read or write cycle (red $\overline{CE}$ during red write cycle, blue during blue write cycle, etc.). When accessing the color palette the address register resets to $00 after a read or write cycle to location $FF. When accessing the overlay palette, the address register increments to $04 following a read or write cycle to overlay color three.

In RGB mode, writing color data entails the MPU loading the address register with the address of the color palette location or overlay palette location to be modified. The MPU performs three successive write cycles (eight bits each of red, green or blue), using C0 or C1 to select either the color palette or the overlay palette. After the blue write cycle, the address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green or blue data. Reading color data is similar to writing except the MPU executes the read cycles.

RGB mode is useful if only an eight-bit data bus is available. Each IDT75C457 is programmed to be red, green or blue PaletteDAC, and will respond only to the assigned read or write cycle. In this application, the IDT75C457s share a common eight-bit data bus. The $\overline{CE}$ inputs of all three IDT75C457s must be asserted simultaneously only during color read/write cycles and address register write cycles.

Address Register Data	C1	C0	Access
X	0	0	Address Register
$00-$FF	0	1	Color Palette
$00	1	1	Overlay Color 0
$01	1	1	Overlay Color 1
$02	1	1	Overlay Color 2
$03	1	1	Overlay Color 3
$04	1	0	Read Mask Register
$05	1	0	Blink Mask Register
$06	1	0	Command Register
$07	1	0	Test Register

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Table 1. Truth Table for MPU Operations

When accessing the color palette, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay palette, the address register increments to location $04 following a blue read or write cycle to overlay color three. To keep track of the red, green and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count module three. They are reset to 0 when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other eight bits of the address register (ADDR 0-7) are accessible to the MPU.

FRAME BUFFER INTERFACE

The frame buffer interface consists of five 8-bit input ports which correspond to five consecutive pixels. In addition, there are two extra bits per port which may be used for overlay information. To reduce the bandwidth requirements for the pixel data, the IDT75C457 latches 4 or 5 pixels (the multiplex factor is programmable to 4 or 5 by bit 7 of the command register) on each rising edge of $\overline{LD}$. The color and overlay information is internally multiplexed at the pixel clock frequency,

CLK, and sequentially output. This arrangement allows pixel data to be transferred at a rate 4 or 5 times slower than the pixel clock. Typically, $\overline{LD}$ is the pixel clock divided by 4 or 5 and is used to clock data out of the frame buffer memory.

As shown in Figure 2, sync, blank, color and overlay information are latched on the rising edge of $\overline{LD}$. Up to 40 bits of color information are input through P_0-P_7{A-E} and up to 10 bits of overlay information are input through OL_0-OL_1{A-E}. Both sync and blank have separate inputs, $\overline{SYNC}$ and $\overline{BLANK}$, respectively. The IDT75C457 outputs color information on each clock cycle. Four or five pixels are output sequentially, beginning with the {A} information, then the {B} information, until the cycle is completed with the {D} or {E} information. In this configuration, sync and blank are limited to multiples of four or five clock cycles.

The multiplexing factor, 4:1 or 5:1, is programmable from the command register, bit 7. In the 4:1 mode, the {E} color and overlay inputs are not used and the $\overline{LD}$ clock should be CLOCK divided by 4. The {E} color and overlay inputs must be connected to a valid logic level.

The overlay inputs (OL_0-OL_1) have the same timing as the pixel inputs (P_0-P_7). It is possible to use additional bit planes or external logic to control the overlay selection for cursor generation.

5

INTERNAL MULTIPLEXING

$\overline{LD}$ is typically CLK divided by four or five and it latches color and overlay information on every rising edge, independent of CLK. A digital PLL allows $\overline{LD}$ to be phase independent of CLK. The only restriction is that only one rising edge of $\overline{LD}$ is allowed to occur per four (4:1 multiplexing) or five (5:1 multiplexing) CLK cycles.

Color Palette

On the rising edge of each CLK cycle, eight bits of color information (P_0-P_7) and two bits of overlay information (OL_0-OL_1) for each pixel are processed by the read mask, blink mask and command registers. This information provides the address to the dual-port color palette RAM. Note that P_0 is the LSB when addressing the color palette RAM. The value stored at a selected address determines the displayed color. Through the use of the control register, individual bit planes may be enabled or disabled for display and/or blinked at one of four blink rates and duty cycles.

The blink timing is based on vertical retrace intervals which are defined by at least 256 $\overline{LD}$ cycles since the last falling edge of $\overline{BLANK}$. The color changes during this normally blanked time.

The processed pixel data is then used to select which color palette entry or overlay register is used to provide color information. Table 2 illustrates the truth table used for color selection.

CR_6[1]	OL_1	OL_0	P_7-P_0	Palette Entry
1	0	0	$00	Color Palette Entry $00
1	0	0	$01	Color Palette Entry $01
	.			.
	.			.
	.			.
1	0	0	$FF	Color Palette Entry $FF
0	0	0	$xx	Overlay Color 0
x	0	1	$xx	Overlay Color 1
x	1	0	$xx	Overlay Color 2
x	1	1	$xx	Overlay Color 3

NOTE: 2523 tbl 02

1. CR_6 is bit 6 of the Command Register.

Table 2. Palette and Overlay Select

Video Generation, DACs

On every CLK cycle, the selected 8 bits of color information from the Color Palette RAM are presented to the 8-bit D/A converters. The IDT75C457 uses a 5 x 3 segmented approach where the five MSBs of the input data are decoded into a parallel "Thermometer" code which produces thirty two "coarse" output levels. The remaining three LSBs of input data drive three binary weighted current switches with a total contribution of one-thirty second of full scale. The MSB and LSB currents are summed at the output to produce 256 levels.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs are pipelined to maintain synchronization with the pixel data. Both inputs drive appropriately weighted current switches which are summed at the output of the DACs to produce the specific output levels required by RS-343, as shown in Figure 3. Table 3 details the output levels associated with $\overline{SYNC}$, $\overline{BLANK}$ and data.

Monitor Interface

The analog outputs of the IDT75C457 are high-impedance current sources which are capable of directly driving a doubly terminated 75Ω coaxial cable to standard video levels. A typical output circuit is shown in Figure 4.

Description	S	B	DAC Data	I_{OUT} (mA)
WHITE	1	1	$FF	26.67
DATA	1	1	Data	Data + 9.05
DATA and SYNC	0	1	Data	Data + 1.44
BLACK	1	1	$0	9.05
BLACK and SYNC	0	1	$0	1.44
BLANK	1	0	X	7.62
SYNC	0	0	X	0

NOTE: 2523 tbl 03

1. Typical values with full scale I_{OUT} = 26.67mA, R_{SET} = 523Ω, V_{REF} = 1.235V, S is SYNC, B is BLANK.

Table 3. Video Output Truth Table

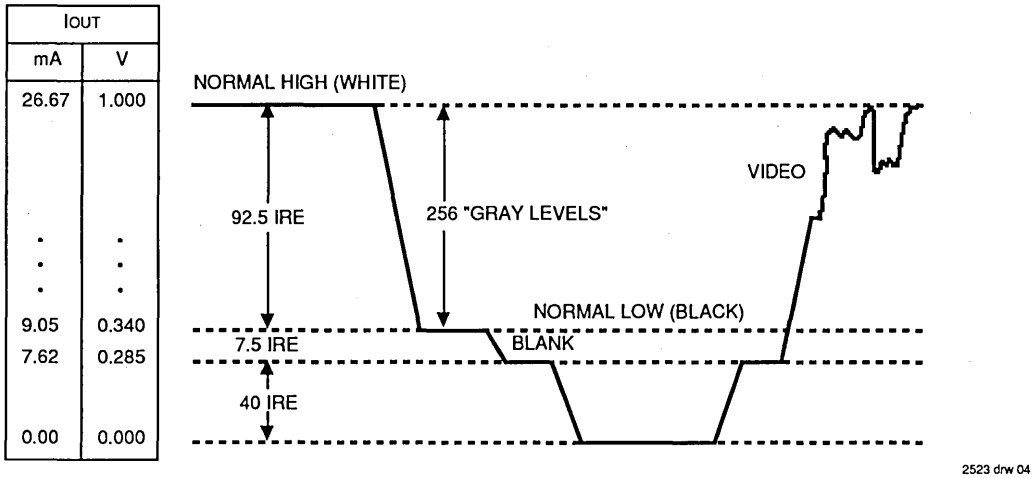


Figure 1. Composite Video Output Waveform

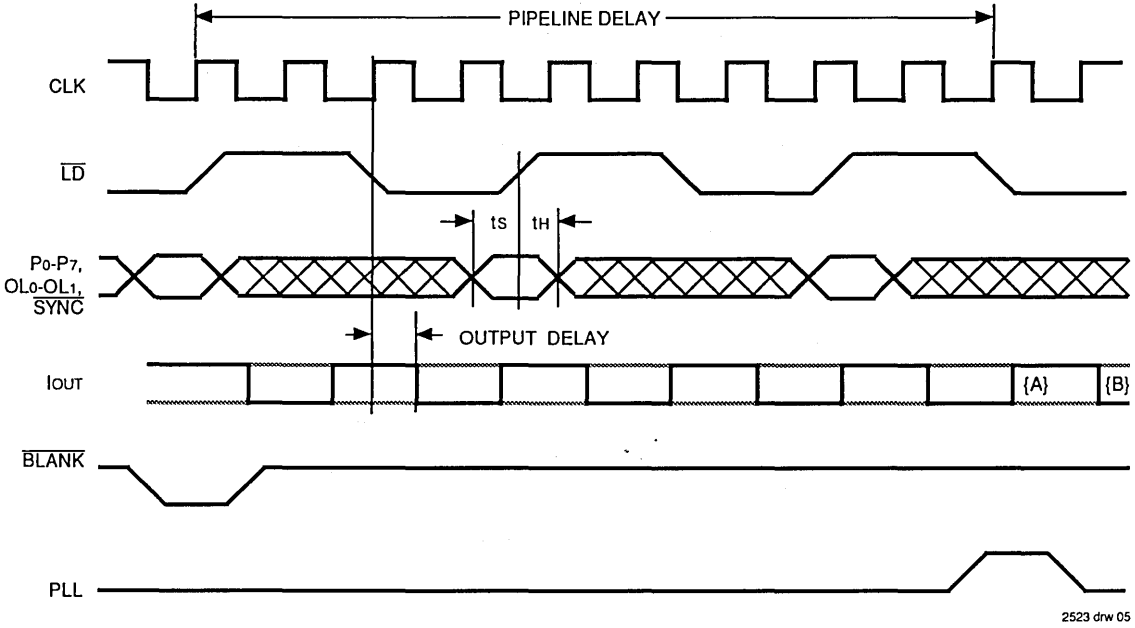


Figure 2. Pixel Timing

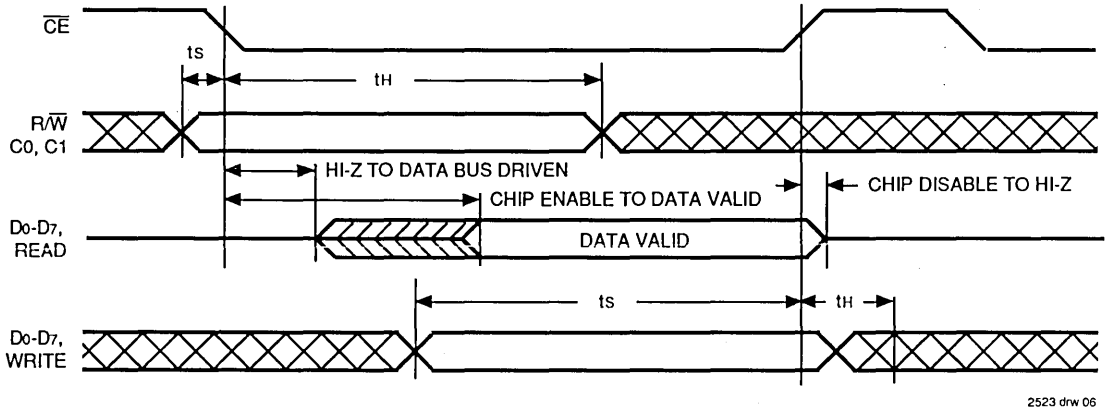


Figure 3. Data Bus Timing

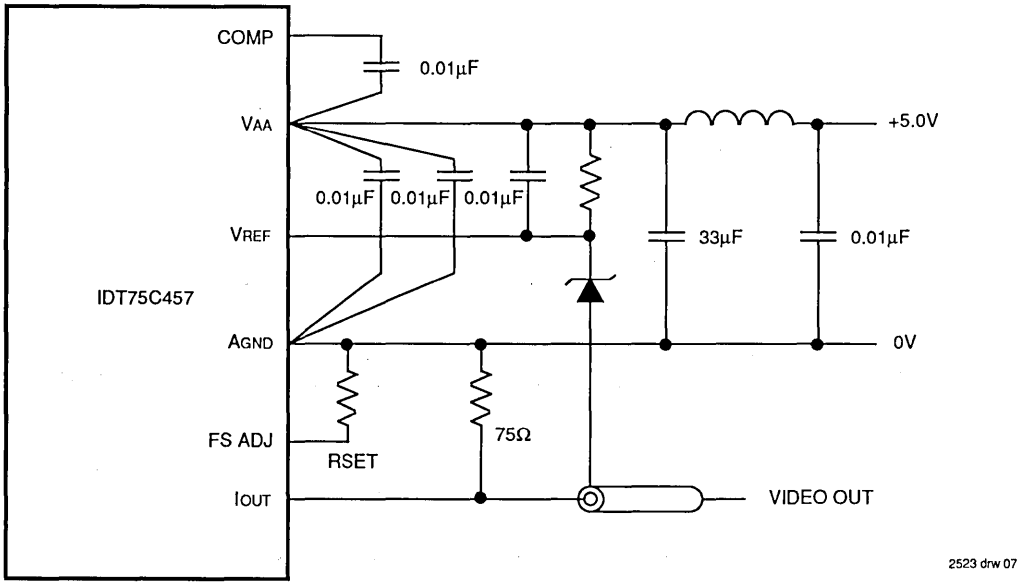


Figure 4. Typical Application

PIN DESCRIPTIONS

Pin Name	Description
Data Bus	
D_0-D_7	8-bit, bidirectional data bus. Data is input and output over this bus and the flow is controlled by R/$\overline{W}$ and $\overline{CE}$. D_7 is the most significant bit.
$\overline{CE}$	Chip Enable Input. The chip is enabled when this control pin is LOW. During a write cycle (R/$\overline{W}$ LOW), the data present on D_0-D_7 is internally latched on the LOW-to-HIGH transition of this pin.
R/$\overline{W}$	Read/Write Control input. The Read/Write input is latched on the HIGH-to-LOW transition of $\overline{CE}$ and determines the direction of the bidirectional data bus, D_0-D_7. If R/$\overline{W}$ is HIGH during the falling edge of $\overline{CE}$, a read cycle occurs. If R/$\overline{W}$ is LOW during the falling edge of $\overline{CE}$, a write cycle occurs and, additionally, D_0-D_7 are latched on the rising edge of $\overline{CE}$.
C0, C1	Register Control inputs. C0 and C1 determine which register or palette entry is accessed during a read or write cycle. These inputs are latched on the HIGH-to-LOW transition of $\overline{CE}$.
Pixel	
CLK, $\overline{CLK}$	Pixel Clock Inputs. These inputs are differential and may be driven by ECL operating from a +5V supply. The clock frequency is normally the system pixel clock rate.
$\overline{LD}$	Load Clock input. The Load Clock is normally CLK divided by 4 or 5 (determined by the Control Register bit 7). The pixel data, P_0-P_7 {A-E} and OL_0-OL_1 {A-E}, $\overline{BLANK}$ and $\overline{SYNC}$ are internally latched on the LOW-to-HIGH transition of $\overline{LD}$.
P_0-P_7 {A-E}	Pixel Input Data. These inputs provide the address input to the color palette RAM. The data stored at a particular address is the color output by the DAC. Four or five consecutive pixels, as determined by bit 7 in the Command Register, are internally latched on the LOW-to-HIGH transition of $\overline{LD}$. The pixels are output sequentially, first {A} then {B}. After all four or five pixels have been output, the cycle repeats. Unused inputs must be connected to a valid logic level.
OL_0-OL_1{A-E}	Pixel Overlay Inputs. The Overlay inputs have the same timing as P_0-P_7 and select between either the color palette or the overlay palette. When the overlay palette is selected, the pixel information P_0-P_7 {A-E} is ignored. Bit 6 of the command register determines if Overlay = 0 displays overlay color 0 or the color palette entry. See Table 2 for details.
$\overline{BLANK}$	Composite Blank Input. A LOW on this input forces the analog outputs (I_{OUT}) to the blanking level. The $\overline{BLANK}$ input is internally latched on the LOW-to-HIGH transition of $\overline{LD}$. This input overrides all other pixel information.
$\overline{SYNC}$	Composite Sync Input. A LOW on this input subtracts approximately 7mA from the I_{OG} analog output and overrides no other pixel information. For the correct $\overline{SYNC}$ level, this input should be LOW only when $\overline{BLANK}$ is also LOW. The $\overline{SYNC}$ input is internally latched on the LOW-to-HIGH transition of $\overline{LD}$.
Analog	
A_{GND}	Analog Ground Power Supply, 0V.
V_{AA}	Analog Power Supply, 5V.
V_{REF}	Voltage Reference Input, 1.235V. This input supplies a reference voltage for the DAC circuitry. Care must be taken to correctly decouple this voltage because noise on this pin will couple directly to the DAC outputs.
FS ADJ	Full-Scale Adjust Input. The current flowing from this pin to A_{GND} is directly proportional to the full-scale analog output current. Normally, a resistor is connected between this pin and A_{GND}. The voltage on this pin is approximately equal to V_{REF}. The relationship I_{OUT} (mA) = 11.294 x V_{REF} (V)/RSET (KΩ).
I_{OUT}	DAC current output.
COMP	Compensation Input. This pin provides the ability to compensate the internal reference operational amplifier.
PLL	Phase Lock Loop Current Output. This high impedance current source is used to enable multiple IDT75C457s to be synchronized with sub-pixel resolution when used with an external PLL. A logic one on the $\overline{BLANK}$ input results in no current being output onto this pin, while a logic zero results in the following current being output: PLL (mA) = 3227 * V_{REF} (V)/RSET (ohm). If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a register up to 150 ohms).

2523 tbl 04

5

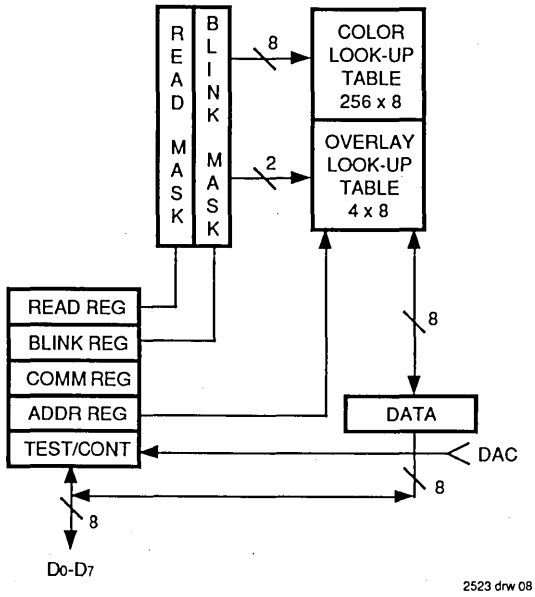


Figure 5. IDT75C457 Register Block Diagram

Command Register

The Command Register is accessed by reading or writing with the Address Register = $06, C0 = 0 and C1 = 1 (see Table 1). It internally ANDs the pixel information with a bit from the register before the color palette selection, effectively enabling (HIGH) or disabling (LOW) the entire pixel plane. The Read Mask Register may be read or written at any time. RMR7 (Read Mask Register bit 7) corresponds to D7 (Data Bus bit 7).

CR0 — OL0 Display Enable. This bit is ANDed internally with the data from OL0 prior to the palette selection. If CR0 is LOW, the internal OL0 bits are set LOW, allowing only overlay colors 0 and 2 to be selected.

CR1 — OL1 Display Enable. This bit is ANDed internally with the data from OL1 prior to the palette selection. If CR1 is LOW, the internal OL1 bits are set LOW, allowing only overlay colors 0 and 1 to be selected.

CR2 — OL0 Blink Enable. If this bit is set HIGH, the OL0 bit is internally switched between the value input and 0 at the rate specified by the CR4 and CR5 bits. CR0 must be set HIGH for this function.

CR3 — OL1 Blink Enable. If this bit is set HIGH, the OL1 bit is internally switched between the value input and 0 at the rate specified by the CR4 and CR5 bits. CR1 must be set HIGH for this function.

CR4, CR5 — Blink Rate Select. These bits select blink rates based on Vertical Sync cycles, defined as more than 256 $\overline{LD}$ cycles during BLANK.

CR6 — Color Palette RAM Enable. This bit specifies whether to use the Color Palette or the Overlay Palette when OL0 = OL1 = LOW.

CR7 — Multiplex Select. This bit selects between 4:1 (CR7 = 0) or 5:1 (CR7 = 1) multiplexing. When using 4:1 multiplexing the {E} inputs are never used and must be connected to a valid logic level.

Read Mask Register

The Read Mask Register is accessed by reading or writing with the Address Register = $04, C0 = 0 and C1 = 1 (see Table 1). It internally ANDs the pixel information with a bit from the register before the color palette selection, effectively enabling (HIGH) or disabling (LOW),the entire pixel plane. The Read Mask Register may be read or written at any time. RMR7 (Read Mask Register bit 7) corresponds to D7 (Data Bus bit 7).

Blink Mask Register

The Blink Mask Register is accessed by reading or writing with the Address Register = $05, C0 = 0 and C1 = 1 (see Table 1). Each register bit causes the corresponding pixel bit (P0-P7) to internally switch between the input value and 0 at the blink rate specified in the Command Register. For this function to work, the corresponding enable bit in the Read Mask Register must be set HIGH. The Blink Mask Register may be read or written at any time. BMR7 (Blink Mask Register bit 7) corresponds to D7 (Data Bus bit 7).

Test/Control Register

The Test/Control Register is accessed by reading or writing with the Address Register = $07, C0 = 0 and C1 = 1 (see Table 1). This register allows the MPU to read the 8 input bits of the DAC. It may be written to or read by the MPU at any time, and is not initialized. The register bits are defined as follows:

D7-D4	DAC input data (one nibble)
D3	Upper (LOW) or Lower (HIGH) nibble select
D2	Blue enable
D1	Green enable
D0	Red enable

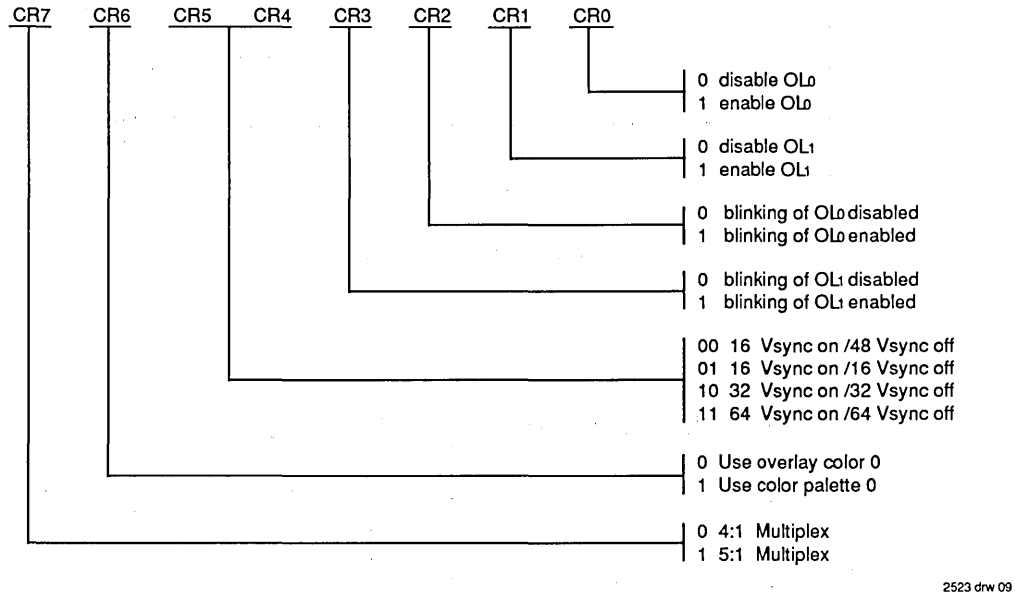
2523 tbl 05

When writing to the register, upper four bits (D4-D7) are ignored.

To use the test/control register, the MPU writes to it, specifying the upper or lower nibble of the 8-bit input information to the DAC. When the MPU reads the register, the four bits of color information from the DAC inputs are contained in the upper four bits of the register, and the lower four bits contain whatever was previously written to the register. Note that either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

The red, green and blue enable bits are also used to specify the mode of writing color data to, and reading color data from, the IDT75C457. If all three enable bits are a logic zero, each write cycle to the color palette or the overlay palette loads eight bits of color data. During each read cycle of the color palette or the overlay palette, eight bits of color data are output onto the data bus. If a 24-bit data bus is available, this enables three IDT75C457 to be accessed simultaneously.

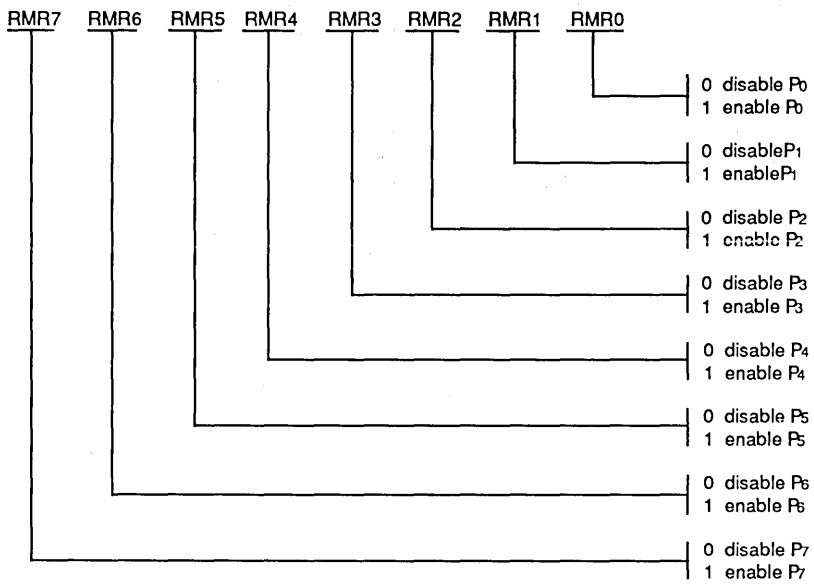
If any of the red, green, blue bits are a logic one, the IDT75C457 assumes the MPU is reading or writing color information using red, green, blue cycles, such as are used on the IDT75C458. Setting the appropriate enable bit configures the IDT75C457 to output or input color data only for the color read/write cycle corresponding to the enabled color. Thus, if the green enable bit is a logic one, and a red, green, blue write cycle occurred, the IDT75C457 would input data only during the green write cycle. If a red, green, blue read cycle occurred, the IDT75C457 would output data only during the green read cycle. Note that $\overline{CE}$ must be a logic zero during each of the red, green, blue cycles. One, and only one, of the enable bits must be a logic one. This mode of operation is useful where only an 8-bit data bus is available and the software drivers are written for RGB operation.



2523 drw 09

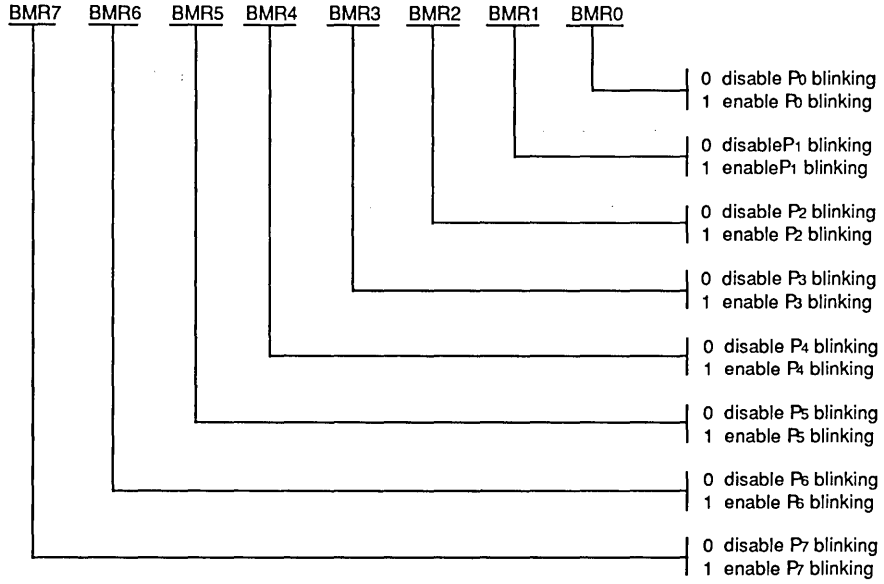
Figure 6. Command Register Designations

5



2523 drw 010

Figure 7. Read Mask Register Designations



2523 drw 11

Figure 8. Blink Mask Register Designations

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
Power Supplies			
V_{AA}	Measured to AGND	−0.5 to +7.0	V
Input Voltage			
Applied Voltage (2)	Measured to AGND	−0.5 to V_{AA} +0.5	V
Output			
Applied Voltage (2)	Measured to AGND	−0.5 to V_{AA} +0.5	V
Applied Current (2, 3, 4)	Externally forced	−1.0 to +6.0	mA
Analog Output Short Circuit Duration	Analog output High to AGND	Indef	s
Temperature			
Operating	Military	−55 to +125	°C
Ambient	Commercial	0 to +70	°C
Storage	Military	−65 to +150	°C
	Commercial	−55 to +125	°C

2523 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

5

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{AA}	Power Supply	Measured to AGND	4.75	5.0	5.25	V
I_{AA}	Power Supply Current	V_{AA} = Typ., Static	–	120	–	mA
V_{IH} (1)	Input Voltage HIGH		2.0	–	V_{AA} + 0.5	V
V_{IL} (1)	Input Voltage LOW		AGND - 0.5	–	0.8	V
V_{CIH}	Clock Input Voltage HIGH		V_{AA} - 1.0	–	V_{AA} + 0.5	V
V_{CIL}	Clock Input Voltage LOW		AGND - 0.5	–	V_{AA} - 0.6	V
I_{IH}	Input Current HIGH	V_{IN} = 2.4V	–	–	1	µA
I_{IL}	Input Current LOW	V_{IN} = 0.4V	–	–	-1	µA
V_{OH}	Output Voltage HIGH	V_{AA} = Min., I_{OH} = -800µA	2.4	–	–	V
V_{OL}	Output Voltage LOW	V_{AA} = Min., I_{OL} = 6.4mA	–	–	0.4	V
I_{OZ}	Output 3-State Current		–	–	10	µA

NOTE:
1. All digital inputs except CLK and $\overline{CLK}$.

2523 tbl 07

AC ELECTRICAL CHARACTERISTICS

Following conditions apply unless otherwise specified:
T_A = 0°C to +70°C (Commercial Temperature Range)
T_A = -55°C to +125°C (Military Temperature Range)
V_{AA} = 5.0V ±5%
TTL Inputs, V_{IL} = 0V, V_{IH} = 3V, rise/fall time <5ns
CLK Inputs, V_{IH} = V_{AA} - 1.0V, V_{IL} = V_{AA} - 1.6V, rise/fall time <2ns
Timing reference points at 50% of signal swing

		'75C457-165(1)		'75C457-135(1)		'75C457-125		'75C457-110		'75C457-80		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
F_{CLK}	Clock Frequency	–	165	–	135	–	125	–	110	–	80	MHz
F_{CLD}	$\overline{LD}$ Clock Frequency	–	41	–	34	–	32	–	28	–	20	MHz
t_{CS}	Control Set-up Time, C0, C1, R/$\overline{W}$	0	–	0	–	0	–	0	–	0	–	ns
t_{CH}	Control Hold Time, C0, C1, R/$\overline{W}$	15	–	15	–	15	–	15	–	15	–	ns
t_{CEH}	$\overline{CE}$ HIGH Time	20	–	20	–	25	–	25	–	25	–	ns
t_{CEL}	$\overline{CE}$ LOW Time	30	–	30	–	50	–	50	–	50	–	ns
t_{CEZO}	$\overline{CE}$ to Data Bus Driven	10	–	10	–	10	–	10	–	10	–	ns
t_{CED}	$\overline{CE}$ to Data Valid	–	30	–	30	–	50	–	50	–	75	ns
t_{CEOZ}	$\overline{CE}$ to Data Bus Hi-Z	–	15	–	15	–	15	–	15	–	15	ns
t_{WDS}	Write Data Set-Up Time	30	–	30	–	35	–	35	–	50	–	ns
t_{WDH}	Write Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
t_{CLKCY}	Clock Cycle Time	6	–	7.4	–	8	–	9	–	12	–	ns
t_{CLKPL}	Clock Pulse Width LOW	2.8	–	3.0	–	3.2	–	4	–	5	–	ns
t_{CLKPH}	Clock Pulse Width HIGH	2.8	–	3.0	–	3.2	–	4	–	5	–	ns
t_{LDCY}	$\overline{LD}$ Cycle Time	24	–	29	–	31	–	35	–	50	–	ns
t_{LDPH}	$\overline{LD}$ Pulse Width HIGH	10	–	12	–	13	–	15	–	20	–	ns
t_{LDPL}	$\overline{LD}$ Pulse Width LOW	10	–	12	–	13	–	15	–	20	–	ns
t_{PS}	Pixel Data Set-up Time	2	–	3	–	3	–	3	–	4	–	ns
t_{PH}	Pixel Data Hold Time	1	–	2	–	2	–	2	–	2	–	ns
I_{AAD}	Dynamic Supply Current Commercial Temp.	–	270	–	250	–	230	–	210	–	190	mA
I_{AAD}	Dynamic Supply Current Military Temp.	–	–	–	–	–	260	–	240	–	220	mA

NOTE:
1. 165 and 135 specification over commercial temperature only.

2523 tbl 08

ANALOG OUTPUT DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Res	Resolution			–	8	–	bits
I_{LSB}	LSB Current Size			–	69.1	–	µA
LI			1 LSB Version	–	1/2	±1	LSB
			1/2 LSB Version	–	1/4	±1/2	LSB
LD			1 LSB Version	–	1/2	±1	LSB
			1/2 LSB Version	–	1/4	±1/2	LSB
V_{OC}	Output Compliance Voltage			-1.0	–	1.2	V
R_{AOUT} (2)	Output Impedance				50		kΩ
C_{AOUT} (2)	Output Capacitance	f = 1MHz, I_{OUT} = 0mA			8	12	pF
I_{REF}	V_{REF} Input Current				10		µA
EM	Matching Error (DAC to DAC)			–	2	5	%
PSRR	Power Supply Rejection Ratio			–	50	–	dB
I_W (1)	White Current	Measured to Blank		17.69	19.05	20.40	mA
I_B (1)	Black Current	Measured to Blank		0.95	1.44	1.90	mA
I_{BLANK}	Blank Current I_{OR}, I_{OB}			0	5	50	µA
I_{BLANK} (1)	Blank Current I_{OG}			6.29	7.62	8.96	mA
I_{SYNC}	Sync Current I_{OG}			0	5	50	µA

NOTES:
1. R_{SET} = 523Ω, V_{REF} = 1.235V
2. This parameter is guaranteed but not tested in production.

2523 tbl 09

5

ANALOG OUTPUT AC ELECTRICAL CHARACTERISTICS

Following conditions apply unless otherwise specified:
T_A = 0°C to +70°C (Commercial Temperature Range)
T_A = -55°C to +125°C (Military Temperature Range)
V_{AA} = 5.0V ±5%
TTL Inputs, V_{IL} = 0.8V, V_{IH} = 2.0V, rise/fall time <5ns
CLK Inputs, V_{IH} = V_{AA} - 1.0V, V_{IL} = V_{AA} - 1.6V, rise/fall time <2ns
Timing reference points at 50% of signal swing

		'75C457-165 (3)			'75C457-135 (3)			'75C457-125			'75C457-110			'75C457-80			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
F_{CLK}	Clock Frequency	–	–	165	–	–	135	–	–	125	–	–	110	–	–	80	MHz
t_{VD}	Video Output Delay Time	–	15	–	–	15	–	–	15	–	–	15	–	–	15	–	ns
t_{VT}	Video Output Transition Time	–	1.5	–	–	1.7	–	–	1.8	–	–	2	–	–	2	–	ns
t_S	Video Output Skew	–	0	<2	–	0	<2	–	0	<2	–	0	<2	–	0	<2	ns
t_S	Video Ouput Setting Time	–	6	–	–	7	–	–	8	–	–	8	–	–	12	–	ns
FT	Clock and Data Feedthrough	–	50	–	–	50	–	–	50	–	–	50	–	–	50	–	pV-s
GE	Glitch Energy	–	50	–	–	50	–	–	50	–	–	50	–	–	50	–	pV-s
CT	Crosstalk, DAC to DAC	–	100	–	–	100	–	–	100	–	–	100	–	–	100	–	pV-s
t_{VP}	Pipeline Delay	9	–	9	9	–	9	9	–	9	9	–	9	9	–	9	clock
t_{PLL}	PLL Delay Time	–	15	–	–	15	–	–	15	–	–	15	–	–	15	–	ns

NOTES:
1. C_L = 10pF, 10%-90% points.
2. This parameter is guaranteed but not tested in production.
3. 165 and 135 MHz over commercial temperature range only.

2523 tbl 10

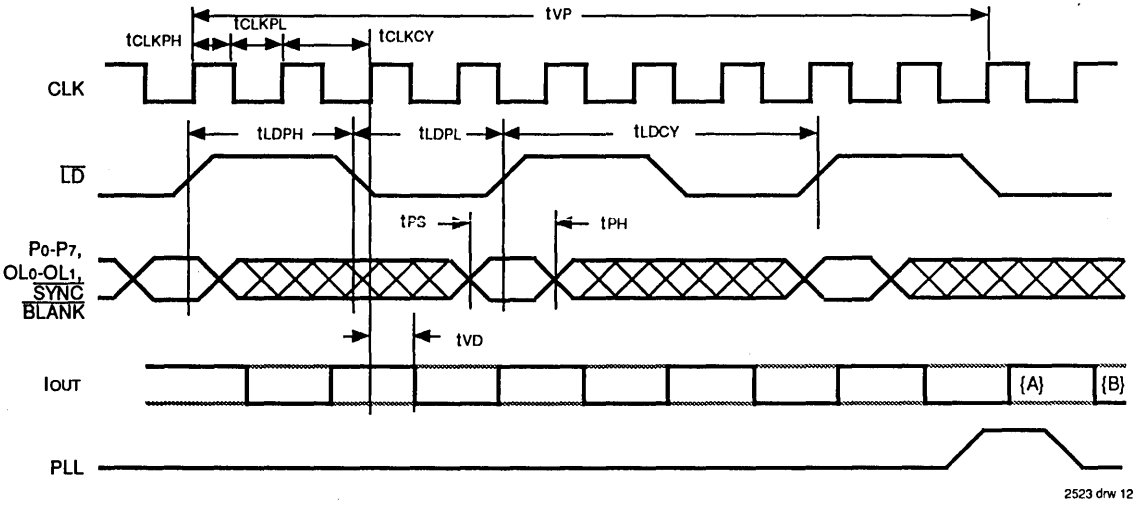


Figure 9. Video I/O Timing Diagram

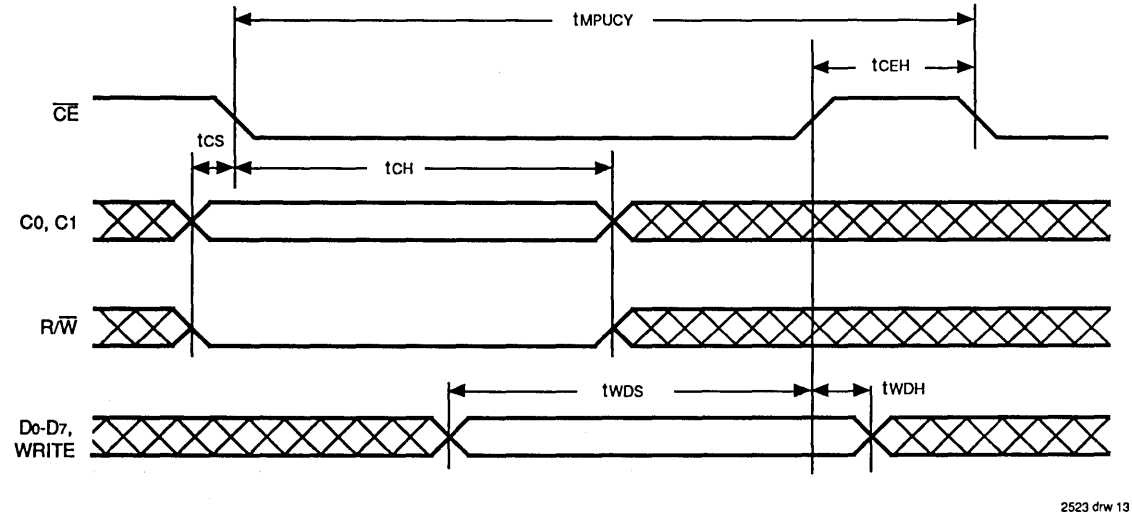


Figure 10. MPU WRITE Timing Diagram

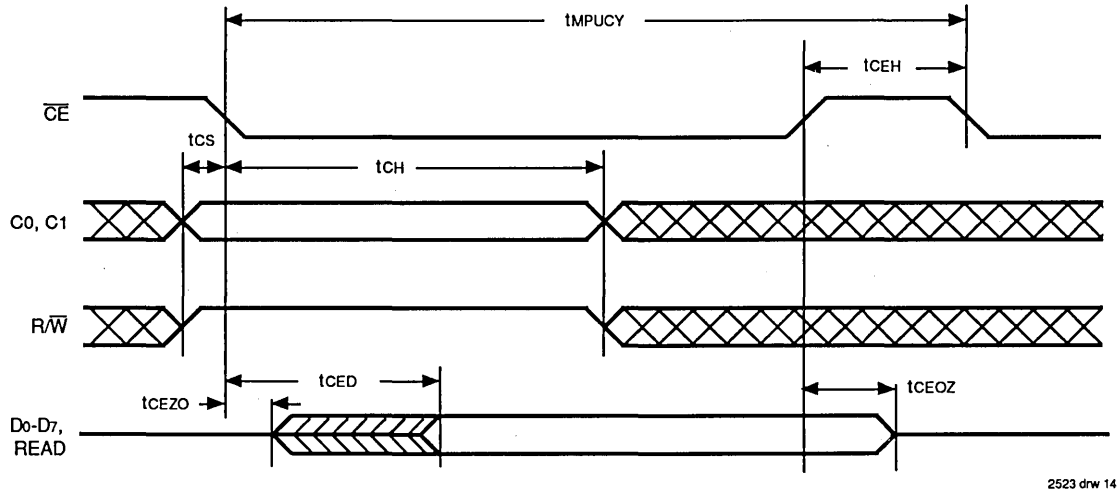
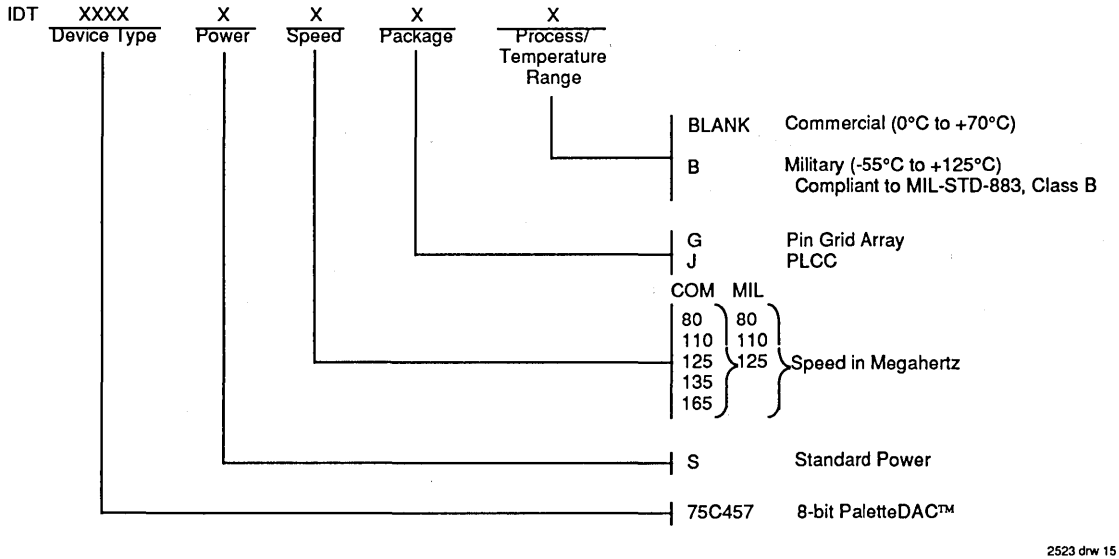


Figure 11. MPU READ Timing Diagram

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS TRIPLE 8-BIT PALETTEDAC™

IDT 75C458

FEATURES:

- 165/135/125/110/80MHz operating speed
- Fixed pipeline delay: 9 clock cycles
- 50ns read access time
- Integral and differential linearity < 1/2LSB
- Triple 8-bit DACs
- 256 x 24 Dual-Ported Color Palette RAM
- 4 x 24 Dual-Ported Overlay Palette RAM
- Multiplexed TTL pixel and overlay inputs
- RS-343A compatible RGB outputs
- CEMOS ™ monolithic construction
- Single 5V power supply
- 84-pin PGA and PLCC packages
- Typical power dissipation: 1000mW
- Pin- and function-compatible with Brooktree BT458
- Military product is compliant to MIL-STD-883, Class B

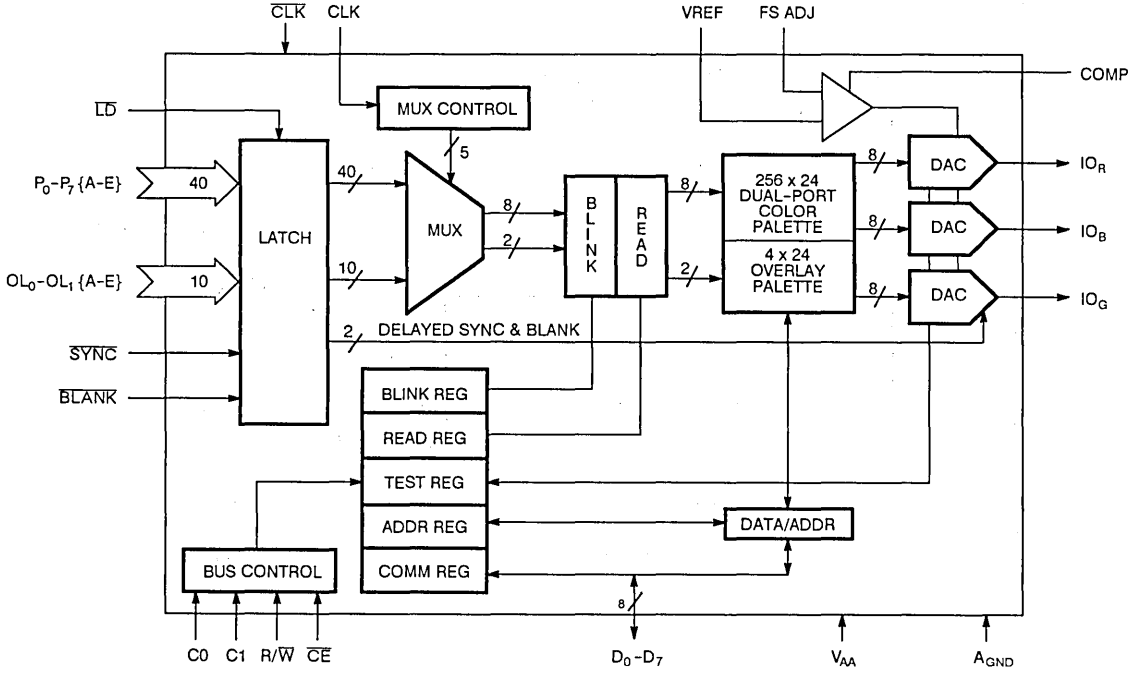
DESCRIPTION:

The IDT75C458 is a triple 8-bit video DAC with on-chip, dual-ported color palette memory. This chip is specifically designed for the display of high resolution color graphics. The architecture eliminates the ECL pixel interface by providing multiple TTL-compatible pixel ports and by multiplexing the pixel data on-chip.

The IDT75C458 supports up to 259 simultaneous colors from a palette of 16.8 million. Other features included on-chip are programmable blink rates, bit plane masking and blinking as well as a color overlay capability. The IDT75C458 generates RS-343A compatible red, green, and blue video outputs which are capable of directly driving a doubly terminated 75Ω coaxial cable.

The IDT75C458 military DACs are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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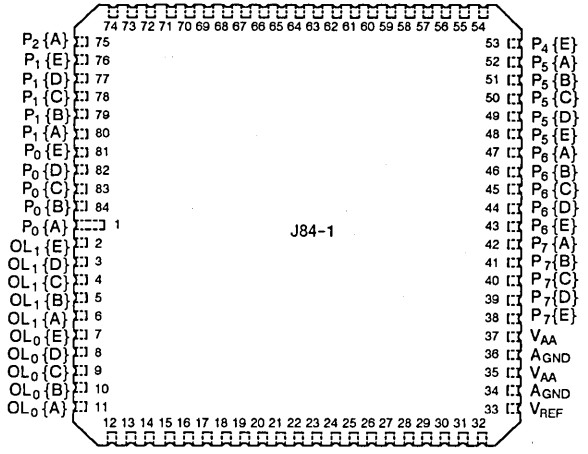
PIN CONFIGURATIONS

	A	B	C	D	E	F	G	H	J	K	L	M
12	COMP	A_{GND}	V_{AA}	$P_7\{D\}$	$P_7\{B\}$	$P_6\{E\}$	$P_6\{C\}$	$P_6\{B\}$	$P_5\{E\}$	$P_5\{C\}$	$P_5\{B\}$	$P_4\{E\}$
11	IO_B	A_{GND}	V_{AA}	$P_7\{E\}$	$P_7\{C\}$	$P_7\{A\}$	$P_6\{D\}$	$P_6\{A\}$	$P_5\{D\}$	$P_5\{A\}$	$P_4\{C\}$	$P_4\{A\}$
10	IO_G	FSADJ	V_{REF}							$P_4\{D\}$	$P_4\{B\}$	$\overline{SYNC}$
9	V_{AA}	IO_R									$\overline{BLANK}$	$\overline{LD}$
8	C1	R/$\overline{W}$									$\overline{CLK}$	CLK
7	V_{AA}	C0									V_{AA}	V_{AA}
6	A_{GND}	A_{GND}					G84-2				$P_3\{E\}$	A_{GND}
5	$\overline{CE}$	D_7									$P_3\{C\}$	$P_3\{D\}$
4	D_6	D_5									$P_3\{A\}$	$P_3\{B\}$
3	D_4	D_2	D_0	△ ALIGNMENT MARK						$P_2\{A\}$	$P_2\{C\}$	$P_2\{E\}$
2	D_3	D_1	$OL_0\{B\}$	$OL_0\{E\}$	$OL_1\{B\}$	$OL_1\{E\}$	$P_0\{B\}$	$P_0\{D\}$	$P_1\{A\}$	$P_1\{D\}$	$P_1\{E\}$	$P_2\{D\}$
1	$OL_0\{A\}$	$OL_0\{C\}$	$OL_0\{D\}$	$OL_1\{A\}$	$OL_1\{C\}$	$OL_1\{D\}$	$P_0\{A\}$	$P_0\{C\}$	$P_0\{E\}$	$P_1\{B\}$	$P_1\{C\}$	$P_2\{B\}$

PGA
TOP VIEW



PLCC
TOP VIEW

GENERAL INFORMATION:

The IDT75C458 triple 8-bit PaletteDAC is a highly integrated building block which interfaces a relatively low bandwidth frame buffer memory to an analog RS-343A, high bandwidth output. To decrease the frame buffer memory requirements, the IDT75C458 has a color lookup table (dual-port RAM) included on-chip.The basic functional blocks are the microprocessor bus interface, the frame buffer memory interface and multiplexer, a dual-port RAM with one R/W port and one high-speed R/O port and three 8-bit video speed DACs.

MICROPROCESSOR BUS INTERFACE

The IDT75C458 supports a standard microprocessor bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and overlay registers allow color updating without contention with the display refresh process.

The bus interface consists of eight bidirectional data pins, D_0 - D_7, with two control inputs, C0 and C1, a read/write direction input, R/$\overline{W}$, and a clock input, $\overline{CE}$. All data and control information are latched on the falling edge of $\overline{CE}$, as shown in Figure 3. All accesses to the chip are controlled by the data in the address register combined with the control inputs C0, C1 and R/$\overline{W}$, depicted in the Truth Table (Table 1).

An access to a control register requires writing a 4 through 7 into the address register (C0 = C1 = 0) and then writing or reading data to the selected register (C0 = 0, C1 = 1). When accessing the control registers, the address register is not changed, facilitating read-modify-write operations. If an invalid address is loaded into the address register, data written is ignored or invalid data is read out.

It is also possible to access the color palette information. The palette is organized as 256 addresses with 8 bits of red, blue and green information. Additionally, there are four extra addresses assigned to overlay information, yielding a total memory size of 260 x 24.

Access to the palette entries is, again, through the address register. The desired palette address is loaded into the address register, C0 and C1 are modified to point to the color palette or overlay and the information is read or written. In this case, however, an internal counter is used to access the red, green or blue color information. The first color palette or overlay access reads or writes red. The next access is for green, while the third access is for blue. After the third access, the address register is incremented, allowing the reading or writing of the red information of the next palette address. When writing, red and green information is temporarily stored in registers and, during the blue cycle, all 24 bits are written.

The internal counter is reset by an access to the address or any of the control registers. After setting the address register, it is possible to read or write the entire palette without accessing the address register again. Some care is needed; only continuous reads or writes are allowed and it is not possible to switch between the color palette and overlay.

The color palette RAM and overlay registers are dual-ported which allows simultaneous access from the MPU port (D_0 - D_7) and the pixel port (P_0 - P_7 {A-E}). If the pixel port is reading the same palette entry as the MPU is writing, it is possible that the DAC output may be invalid. It is recommended that the palette and overlay entries be updated during the blanking time.

ADDRESS REGISTER DATA	C1	C0	ACCESS
X	0	0	Address Register
$00-$FF	0	1	Color Palette
$00	1	1	Overlay Color 0
$01	1	1	Overlay Color 1
$02	1	1	Overlay Color 2
$03	1	1	Overlay Color 3
$04	1	0	Read Mask Register
$05	1	0	Blink Mask Register
$06	1	0	Command Register
$07	1	0	Test Register

NOTE:

Control input C0 = 1 enables the internal counter which accesses the red, green and blue colors individually and increments the address counter after the blue access. C0 = 0 disables auto-increment of the address register allowing read-modify-write operations.

Table 1. Truth Table for MPU Operations

FRAME BUFFER INTERFACE

The frame buffer interface consists of five 8-bit input ports which correspond to five consecutive pixels. In addition, there are two extra bits per port which may be used for overlay information. To reduce the bandwidth requirements for the pixel data, the IDT75C458 latches 4 or 5 pixels (the multiplex factor is programmable to 4 or 5 by bit 7 of the command register) on each rising edge of $\overline{LD}$. The color and overlay information is internally multiplexed at the pixel clock frequency, CLK, and sequentially output. This arrangement allows pixel data to be transferred at a rate 4 or 5 times slower than the pixel clock. Typically, $\overline{LD}$ is the pixel clock divided by 4 or 5 and is used to clock data out of the frame buffer memory.

As shown in Figure 2, sync, blank, color and overlay information are latched on the rising edge of $\overline{LD}$. Up to 40 bits of color information are input through P_0 - P_7 {A-E} and up to 10 bits of overlay information are input through OL_0 - OL_1 {A-E}. Both sync and blank have separate inputs, $\overline{SYNC}$ and $\overline{BLANK}$, respectively. The IDT75C458 outputs color information on each clock cycle. Four or five pixels are output sequentially, beginning with the {A} information, then the {B} information, until the cycle is completed with the {D} or {E} information. In this configuration, sync and blank times are limited to multiples of four or five clock cycles.

The multiplexing factor, 4:1 or 5:1, is programmable from the command register, bit 7. In the 4:1 mode, the {E} color and overlay inputs are not used and the $\overline{LD}$ clock should be CLOCK divided by 4. The {E} color and overlay inputs must be connected to a valid logic level.

The overlay inputs (OL_0 - OL_1) have the same timing as the pixel inputs (P_0 - P_7). It is possible to use additional bit planes or external logic to control the overlay selection for cursor generation.

INTERNAL MULTIPLEXING

$\overline{LD}$ is typically CLK divided by four or five and it latches color and overlay information on every rising edge, independent of CLK. A digital PLL allows $\overline{LD}$ to be phase independent of CLK. The only restriction is that only one rising edge of $\overline{LD}$ is allowed to occur per four (4:1 multiplexing) or five (5:1 multiplexing) CLK cycles.

Color Palette

On the rising edge of each CLK cycle, eight bits of color information (P_0 - P_7) and two bits of overlay information (OL_0 - OL_1) for each pixel are processed by the read mask, blink mask and command registers. This information provides the address to the dual-port color palette RAM. Note that P_0 is the LSB when addressing the color palette RAM. The value stored at a selected address determines the displayed color. In this way, 8 bits of information can select from a palette of over 16 million with 256 simultaneous displayed colors (plus 3 overlay colors). Through the use of the control register, individual bit planes may be enabled or disabled for display and/or blinked at one of four blink rates and duty cycles.

The blink timing is based on vertical retrace intervals which are defined by at least 256 $\overline{LD}$ cycles since the last falling edge of $\overline{BLANK}$. The color changes during this normally blanked time.

The processed pixel data is then used to select which color palette entry or overlay register is used to provide color information. Table 2 illustrates the truth table used for color selection.

CR6	OL_1	OL_0	$P_7 - P_0$	PALETTE ENTRY
1	0	0	$00	Color palette entry $00
1	0	0	$01	Color palette entry $01
	.		.	.
	.		.	.
	.		.	.
1	0	0	$FF	Color palette entry $FF
0	0	0	$xx	Overlay color 0
x	0	1	$xx	Overlay color 1
x	1	0	$xx	Overlay color 2
x	1	1	$xx	Overlay color 3

NOTE:
CR6 is bit 6 of the Command Register.

Table 2. Palette and Overlay Select

Video Generation, DACs

On every CLK cycle, the selected 24 bits of color information (8 bits each of red, green and blue) from the Color Palette RAM are presented to the three 8-bit D/A converters. The IDT75C458 uses a 5 x 3 segmented approach where the five MSBs of the input data are decoded into a parallel "Thermometer" code which produces thirty two "course" output levels. The remaining three LSBs of input data drive three binary weighted current switches with a total contribution of one-thirty second of full scale. The MSB and LSB currents are summed at the output to produce 256 levels.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs are pipelined to maintained synchronization with the pixel data. Both inputs drive appropriately weighted current switches which are summed at the output of the DACs to produce the specific output levels required by RS-343, as shown in Figure 3. Note that the sync information is only available at the IO_G (green) output and that the input data to the DAC sums with the sync current. Table 3 details the output levels associated with $\overline{SYNC}$, $\overline{BLANK}$ and data.

Monitor Interface

The analog outputs of the IDT75C458 are high-impedance current sources which are capable of directly driving a doubly terminated 75Ω coaxial cable to standard video levels. A typical output circuit is shown in Figure 4.

Description	S	B	DAC data	IO_G(mA)	IO_R, IO_B (mA)
WHITE	1	1	$FF	26.67	19.05
DATA	1	1	data	data+9.05	data+1.44
DATA & SYNC	0	1	data	data+1.44	data+1.44
BLACK	1	1	$0	9.05	1.44
BLACK & SYNC	0	1	$0	1.44	1.44
BLANK	1	0	X	7.62	0
SYNC	0	0	X	0	0

NOTE:
Typical values with full scale IOG = 26.67mA. RSET = 523Ω, VREF = 1.235V. S is $\overline{SYNC}$, B is $\overline{BLANK}$.

Table 3. Video Output Truth Table

IO_R, IO_B		IO_G	
mA	V	mA	V
19.05	0.714	26.67	1.000
•	•	•	•
•	•	•	•
•	•	•	•
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

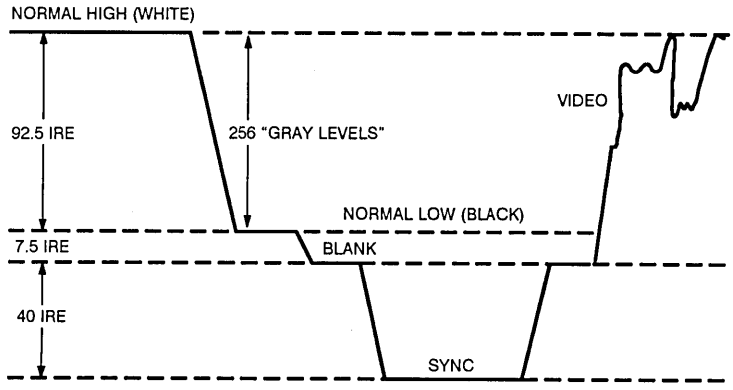


Figure 1. Composite Video Output Waveform

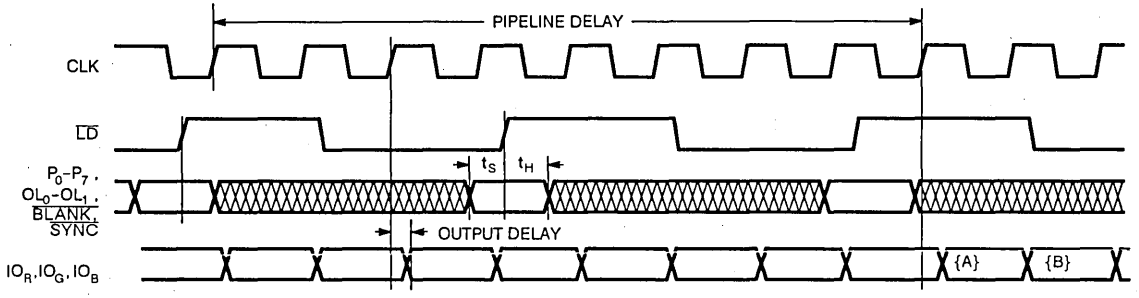


Figure 2. Pixel Timing

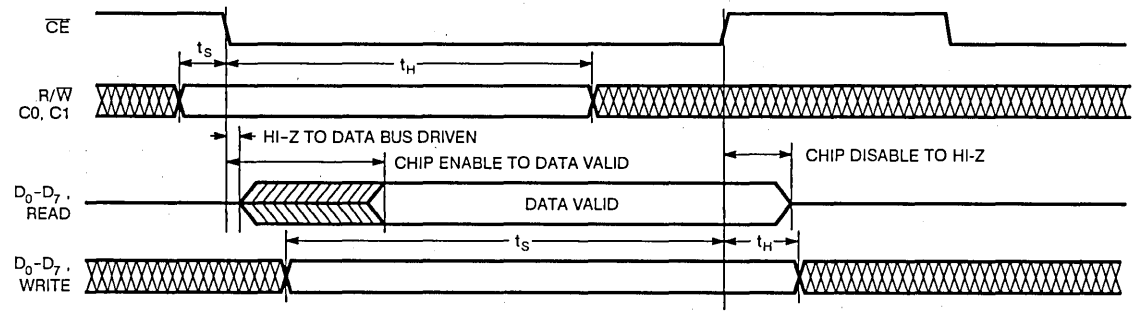


Figure 3. Data Bus Timing

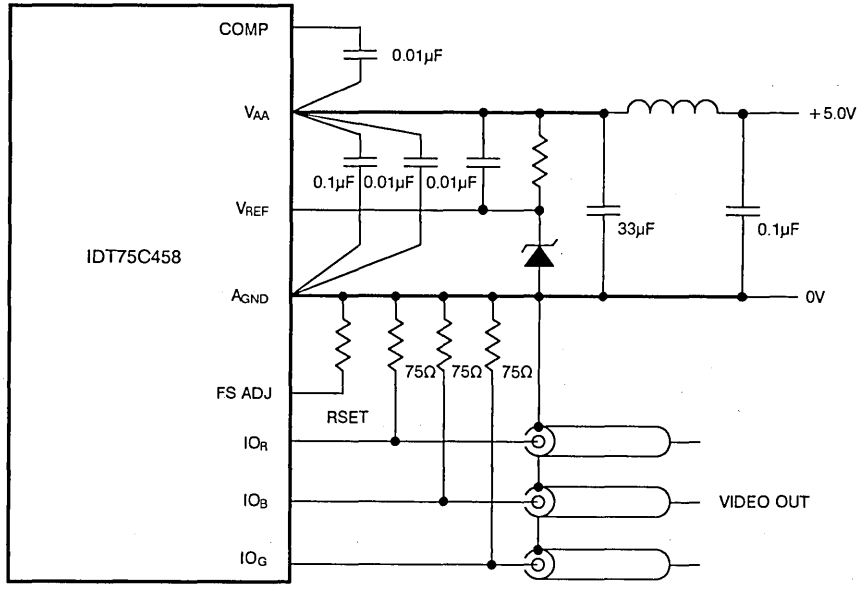


Figure 4. Typical Application

PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
DATA BUS	
D_0 - D_7	8-bit, bidirectional data bus. Data is input and output over this bus and the flow is controlled by R/$\overline{W}$ and $\overline{CE}$. D_7 is the most significant bit.
$\overline{CE}$	Chip Enable input. The chip is enabled when this control pin is LOW. During a write cycle (R/$\overline{W}$ LOW), the data present on D_0 - D_7 is internally latched on the LOW-to-HIGH transition of this pin.
R/$\overline{W}$	Read/Write Control input. The Read/Write input is latched on the HIGH-to-LOW transition of $\overline{CE}$ and determines the direction of the bidirectional data bus D_0 - D_7. If R/$\overline{W}$ is HIGH during the falling edge of $\overline{CE}$, a read cycle occurs. If R/$\overline{W}$ is LOW during the falling edge of $\overline{CE}$, a write cycle occurs and, additionally, D_0 - D_7 are latched on the rising edge of $\overline{CE}$.
C0, C1	Register Control inputs. C0 and C1 determine which register or palette entry is accessed during a read or write cycle. These inputs are latched on the HIGH-to-LOW transition of $\overline{CE}$.
PIXEL	
CLK, $\overline{CLK}$	Pixel Clock inputs. These inputs are differential and may be driven by ECL operating from a +5V supply. The clock frequency is normally the system pixel clock rate.
$\overline{LD}$	Load Clock input. The Load Clock is normally CLK divided by 4 or 5 (determined by the Control Register, bit 7). The pixel data, P_0 - P_7 {A-E} and OL_0 - OL_1 {A-E}, $\overline{BLANK}$ and $\overline{SYNC}$ are internally latched on the LOW-to-HIGH transition of $\overline{LD}$.
P_0 - P_7 {A-E}	Pixel Input Data. These inputs provide the address input to the color palette RAM. The data stored at a particular address is the color output by the DAC. Four or five consecutive pixels, as determined by bit 7 in the Command Register, are internally latched on the LOW-to-HIGH transition of $\overline{LD}$. The pixels are output sequentially, first {A} then {B}. After all four or five pixels have been output, the cycle repeats. Unused inputs must be connected to a valid logic level.
OL_0 - OL_1 {A-E}	Pixel Overlay Inputs. The Overlay inputs have the same timing as P_0 - P_7 and select between either the color palette or the overlay palette. When the overlay palette is selected, the pixel information P_0 - P_7 {A-E} is ignored. Bit 6 of the command register determines if Overlay = 0 displays overlay color 0 or the color palette entry. See Table 2 for details.
$\overline{BLANK}$	Composite Blank Input. A LOW on this input forces the analog outputs (IO_R, IO_G, IO_B) to the blanking level. The $\overline{BLANK}$ input is internally latched on the LOW-to-HIGH transition of $\overline{LD}$. This input overrides all other pixel information.
$\overline{SYNC}$	Composite Sync Input. A LOW on this input subtracts approximately 7mA from the IO_G analog output and overrides no other pixel information. For the correct SYNC level, this input should be LOW only when $\overline{BLANK}$ is also LOW. The $\overline{SYNC}$ input is internally latched on the LOW-to-HIGH transition of $\overline{LD}$.
ANALOG	
A_{GND}	Analog Ground Power Supply, 0V.
V_{AA}	Analog Power Supply, 5V.
V_{REF}	Voltage Reference Input, 1.235V. This input supplies a reference voltage for the DAC circuitry. Care must be taken to correctly decouple this voltage because noise on this pin will couple directly to the DAC outputs.
FS ADJ	Full-Scale Adjust Input. The current flowing from this pin to A_{GND} is directly proportional to the full-scale analog output current. Normally, a resistor is connected between this pin and A_{GND}. The voltage on this pin is approximately equal to V_{REF}. The relationship between the full-scale output current and RSET is: IO_G (mA) = 11.294 x V_{REF} (V)/RSET (KΩ) IO_R, IO_B (mA) = 8.067 x V_{REF} (V)/RSET (KΩ)
IO_G, IO_R, IO_B	Green, Red and Blue DAC current outputs.
COMP	Compensation Input. This pin provides the ability to compensate the internal reference operational amplifier.

5

INTERNAL REGISTERS

Command Register

The Command Register is accessed by reading or writing with the Address Register = $06, C0 = 0 and C1 = 1 (see Table 1). It provides control over multiplexing and blink rate selection. The Command Register may be read or written at any time. CR7 (Command Register bit 7) corresponds to D7 (Data Bus bit 7).

CR0 — OL_0 display enable. This bit is ANDed internally with the data from OL_0 prior to the palette selection. If CR0 is LOW, the internal OL_0 bits are set LOW allowing only overlay colors 0 and 2 to be selected.

CR1 — OL_1 display enable. This bit is ANDed internally with the data from OL_1 prior to the palette selection. If CR1 is LOW, the internal OL_1 bits are set LOW allowing only overlay colors 0 and 1 to be selected.

CR2 — OL_0 blink enable. If this bit is set HIGH, the OL_0 bit is internally switched between the value input and 0 at the rate specified by the CR4 and CR5 bits. CR0 must be set HIGH for this function.

CR3 — OL_1 blink enable. If this bit is set HIGH, the OL_1 bit is internally switched between the value input and 0 at the rate specified by the CR4 and CR5 bits. CR1 must be set HIGH for this function.

CR4, CR5 — Blink Rate Select. These bits select blink rates based on Vertical Sync cycles, defined as more than 256 $\overline{LD}$ cycles during BLANK.

CR6 — Color Palette RAM enable. This bit specifies whether to use the Color Palette or the Overlay Palette when $OL_0 = OL_1 = LOW$.

CR7 — Multiplex Select. This bit selects between 4:1 (CR7 = 0) or 5:1 (CR7 = 1) multiplexing. When using 4:1 multiplexing, the {E} inputs are never used and must be connected to a valid logic level.

Read Mask Register

The Read Mask Register is accessed by reading or writing with the Address Register = $04, C0 = 0 and C1 = 1 (see Table 1). It internally ANDs the pixel information with a bit from the register before the color palette selection, effectively enabling (HIGH) or disabling (LOW) the entire pixel plane. The Read Mask Register may be read or written at any time. RMR7 (Read Mask Register bit 7) corresponds to D7 (Data Bus bit 7).

Blink Mask Register

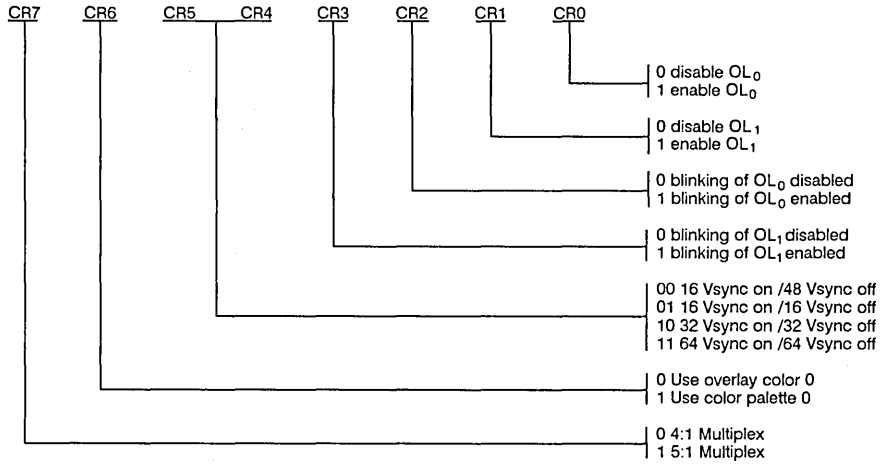
The Blink Mask Register is accessed by reading or writing with the Address Register = $05, C0 = 0 and C1 = 1 (see Table 1). Each register bit causes the corresponding pixel bit (P_0 - P_7) to internally switch between the input value and 0 at the blink rate specified in the Command Register. For this function to work, the corresponding enable bit in the Read Mask Register must be set HIGH. The Blink Mask Register may be read or written at any time. BMR7 (Blink Mask Register bit 7) corresponds to D_7 (Data Bus bit 7).

Test Register

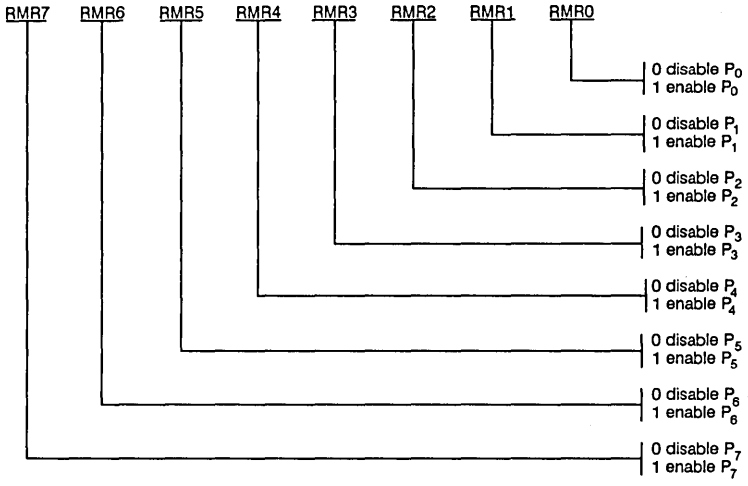
The Test Register is accessed by reading or writing with the Address Register = $07, C0 = 0 and C1 = 1 (see Table 1). This register allows the MPU to read the 24 input bits of the DACs. The register bits are defined below.

TR7-TR4	Read data (one nibble of red, blue or green)
TR3	Upper (LOW) or Lower (HIGH) nibble select
TR2	Blue enable
TR1	Green enable
TR0	Red enable

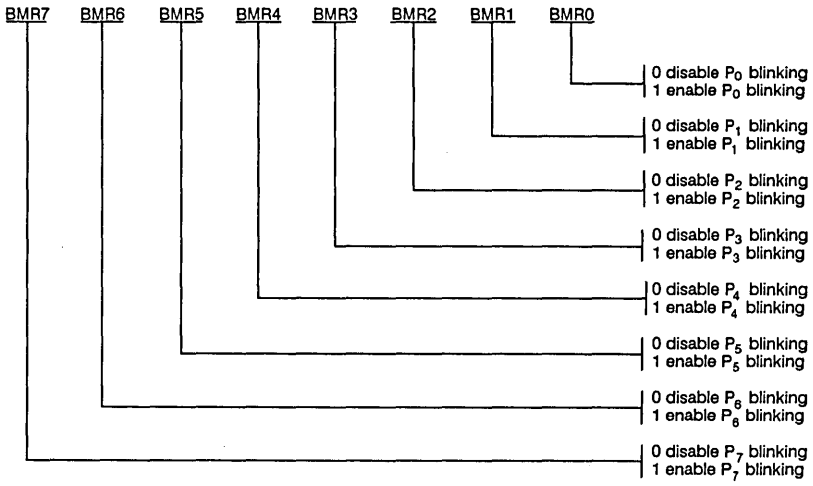
The desired DAC is selected by setting only one color enable bit (D_0 - D_2) HIGH and the upper or lower nibble is selected with D_3. After this write operation, a subsequent read yields the DAC data on D_7 - D_4 and the previously written enable data on D_0 - D_3. For a correct read, pixel and overlay data must remain constant for the entire MPU read cycle. When $\overline{BLANK}$ is asserted, the Test Register information D_7 - D_4 will be forced to zero. TR7 (Test Register bit 7) corresponds to D_7 (Data Bus bit 7).



COMMAND REGISTER DESIGNATIONS



READ MASK REGISTER DESIGNATIONS



BLINK MASK REGISTER DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLIES			
V_{AA}	Measured to A_{GND}	-0.5 to +7.0	V
INPUT VOLTAGE			
Applied Voltage(2)	Measured to A_{GND}	-0.5V to V_{AA} + 0.5	V
OUTPUT			
Applied Voltage(2)	Measured to A_{GND}	-0.5V to V_{AA} + 0.5	V
Applied Current(2,3,4)	Externally forced	-1.0 to + 6.0	mA
Short Circuit Duration	Single output High to A_{GND}	Indefinite	–
TEMPERATURE			
Operating, Ambient	Military	-55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	-65 to +150	°C
	Commercial	-55 to +125	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{AA}	Power Supply	Measured to A_{GND}	4.75	5.0	5.25	V
I_{AA}	Power Supply Current	V_{AA} = Typ., Static	–	200	–	mA
V_{IH}(1)	Input Voltage HIGH		2.0	–	V_{AA} +0.5	V
V_{IL}(1)	Input Voltage LOW		A_{GND} -0.5	–	0.8	V
V_{CIH}	Clock Input Voltage HIGH		V_{AA} -1.0	–	V_{AA} +0.5	V
V_{CIL}	Clock Input Voltage LOW		A_{GND} -0.5	–	V_{AA} -1.6	V
I_{IH}	Input Current HIGH	V_{IN} = 2.4V	–	–	1	µA
I_{IL}	Input Current LOW	V_{IN} = 0.4V	–	–	-1	µA
V_{OH}	Output Voltage HIGH	V_{AA} = Min., I_{OH} = -800µA	2.4	–	–	V
V_{OL}	Output Voltage LOW	V_{AA} = Min., I_{OL} = 6.4mA	–	–	0.4	V
I_{OZ}	Output 3-State Current		–	–	10	µA

NOTE:
1. All digital inputs except CLK and $\overline{CLK}$.

AC ELECTRICAL CHARACTERISTICS

Following conditions apply unless otherwise specified:
T_A = 0°C to +70°C (Commercial Temperature Range)
T_A = -55°C to +125°C (Military Temperature Range)
V_{AA} = 5.0V ±5%
TTL Inputs, V_{IL} = 0V, V_{IH} = 3.0V, rise/fall time <5ns
CLK Inputs, V_{IH} = V_{AA} -1.0V, V_{IL} = V_{AA} -1.6V, rise/fall time <2ns
Timing reference points at 50% of signal swing
Analog Output Load ≤ 10pF
D_0 - D_7 Output Load ≤ 50pF

		IDT75C458-165(1)		IDT75C458-135(1)		IDT75C458-125		IDT75C458-110		IDT75C458-80		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT
F_{CLK}	Clock Frequency	–	165	–	135	–	125	–	110	–	80	MHz
F_{LD}	$\overline{LD}$ Clock Frequency	–	41	–	34	–	32	–	28	–	20	MHz
t_{CS}	Control Set-up Time; C0, C1, R/$\overline{W}$	0	–	0	–	0	–	0	–	0	–	ns
t_{CH}	Control Hold Time; C0, C1, R/$\overline{W}$	15	–	15	–	15	–	15	–	15	–	ns
t_{CEH}	$\overline{CE}$ HIGH Time	20	–	20	–	25	–	25	–	25	–	ns
t_{CEL}	$\overline{CE}$ LOW Time	30	–	30	–	50	–	50	–	50	–	ns
t_{CEZO}	$\overline{CE}$ to Data Bus Driven	10	–	10	–	10	–	10	–	10	–	ns
t_{CED}	$\overline{CE}$ to Data Valid	–	30	–	30	–	50	–	50	–	75	ns
t_{CEOZ}	$\overline{CE}$ to Data Bus HI-Z	–	15	–	15	–	15	–	15	–	15	ns
t_{WDS}	Write Data Set-up Time	30	–	30	–	35	–	35	–	50	–	ns
t_{WDH}	Write Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
t_{CLKCY}	Clock Cycle Time	6	–	7.4	–	8	–	9	–	12	–	ns
t_{CLKPL}	Clock Pulse Width LOW	2.8	–	3.0	–	3.2	–	4	–	5	–	ns
t_{CLKPH}	Clock Pulse Width HIGH	2.8	–	3.0	–	3.2	–	4	–	5	–	ns
t_{LDCY}	$\overline{LD}$ Cycle Time	24	–	29	–	31	–	35	–	50	–	ns
t_{LDPH}	$\overline{LD}$ Pulse Width HIGH	10	–	12	–	13	–	15	–	20	–	ns
t_{LDPL}	$\overline{LD}$ Pulse Width LOW	10	–	12	–	13	–	15	–	20	–	ns
t_{PS}	Pixel Data Set-up Time	2	–	3	–	3	–	3	–	4	–	ns
t_{PH}	Pixel Data Hold Time	1	–	2	–	2	–	2	–	2	–	ns
t_{AAD}	Dynamic Supply Current Commercial Temp.	–	450	–	425	–	400	–	380	–	360	mA
t_{AAD}	Dynamic Supply Current Military Temp.	–	–	–	–	–	450	–	430	–	410	mA

NOTE:
1. 165 and 135 MHz specified over commercial temperature only.

5

ANALOG OUTPUT DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Res	Resolution			–	8	–	bits
I_{LSB}	LSB Current Size			–	69.1	–	µA
L_I			1 LSB VERSION	–	1/2	±1	LSB
			1/2 LSB VERSION	–	1/4	±1/2	LSB
L_D			1 LSB VERSION	–	1/2	±1	LSB
			1/2 LSB VERSION	–	1/4	±1/2	LSB
V_{OC}	Output Compliance Voltage			-1.0	–	1.2	V
R_{AOUT}(2)	Output Impedance				50		kΩ
C_{AOUT}(2)	Output Capacitance	f = 1MHz, I_{OUT} = 0mA			8	12	pF
I_{REF}	V_{REF} Input Current				10		µA
E_M	Matching Error (DAC to DAC)			–	2	5	%
PSRR	Power Supply Rejection Ratio			–	50	–	dB
I_W(1)	White Current	Measured to Blank		17.69	19.05	20.40	mA
I_W(1)	White Current	Measured to Black		16.74	17.62	18.50	mA
I_B(1)	Black Current	Measured to Blank		0.95	1.44	1.90	mA
I_{BLANK}	Blank Current IO_R, IO_B			0	5	50	µA
I_{BLANK}(1)	Blank Current IO_G			6.29	7.62	8.96	mA
I_{SYNC}	Sync Current IO_G			0	5	50	µA

NOTE:
1. R_{SET} = 523Ω, V_{REF} = 1.235V
2. This parameter is guaranteed but not tested in production.

ANALOG OUTPUT AC ELECTRICAL CHARACTERISTICS

Following conditions apply unless otherwise specified:
T_A = 0°C to +70°C (Commercial Temperature Range)
T_A = -55°C to +125°C (Military Temperature Range)
V_{AA} = 5.0V ±5%
TTL Inputs, V_{IL} = 0.8V, V_{IH} = 2.0V, rise/fall time < 5ns
CLK Inputs, V_{IH} = V_{AA} -1.0V, V_{IL} = V_{AA} -1.6V, rise/fall time < 2ns
Timing reference points at 50% of signal swing

		IDT75C458-165(3)			IDT75C458-135(3)			IDT75C458-125			IDT75C458-110			IDT75C458-80			
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
F_{CLK}	Clock Frequency	–	–	165	–	–	135	–	–	125	–	–	110	–	–	80	MHz
t_{VD}	Video Output Delay Time	–	15	–	–	15	–	–	15	–	–	15	–	–	15	–	ns
t_{VT}	Video Output Transition Time	–	1.5	–	–	1.7	–	–	1.8	–	–	2	–	–	2	–	ns
t_S	Video Output Skew(1)	–	0	<2	–	0	<2	–	0	<2	–	0	<2	–	0	<2	ns
t_{SI}(2)	Video Output Settling Time	–	6	–	–	7	–	–	8	–	–	8	–	–	12	–	ns
FT(2)	Clock and Data Feedthrough	–	50	–	–	50	–	–	50	–	–	50	–	–	50	–	pV-s
G_E(2)	Glitch Energy	–	50	–	–	50	–	–	50	–	–	50	–	–	50	–	pV-s
CT(2)	Crosstalk, DAC to DAC	–	100	–	–	100	–	–	100	–	–	100	–	–	100	–	pV-s
t_{VP}	Pipeline Delay	9	–	9	9	–	9	9	–	9	9	–	9	9	–	9	clock

NOTES:
1. C_L = 10pF, 10%-90% points
2. This parameter is guaranteed but not tested in production.
3. 165 and 135 MHz specified over commercial temperature range only.

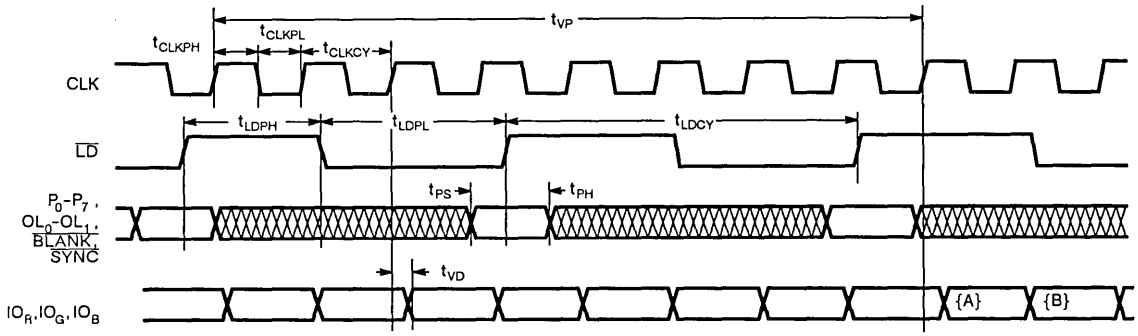


Figure 5. Video I/O Timing Diagram

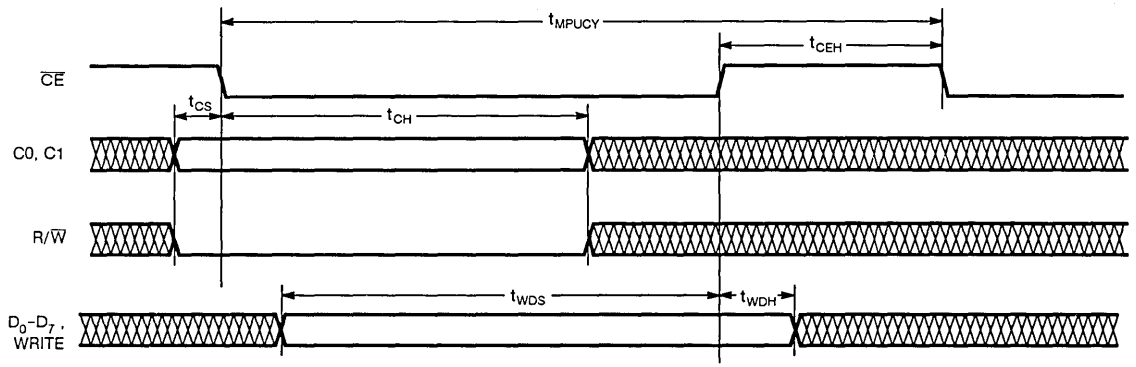


Figure 6. MPU WRITE Timing Diagram

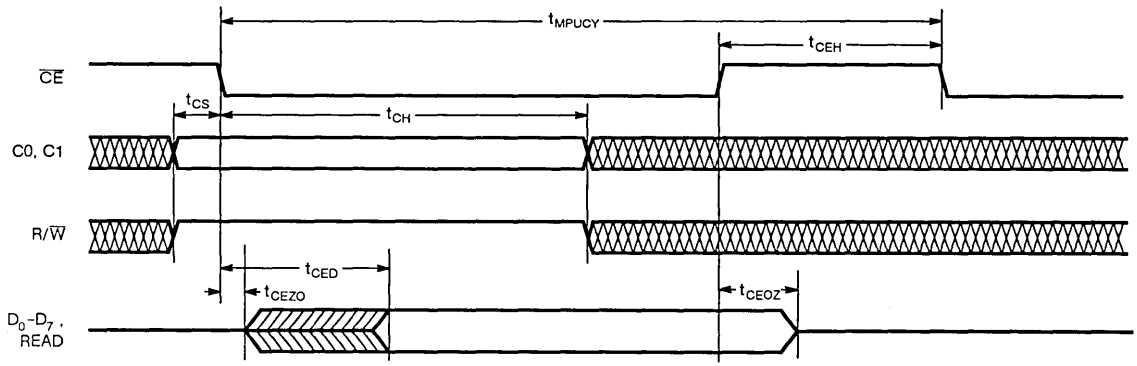
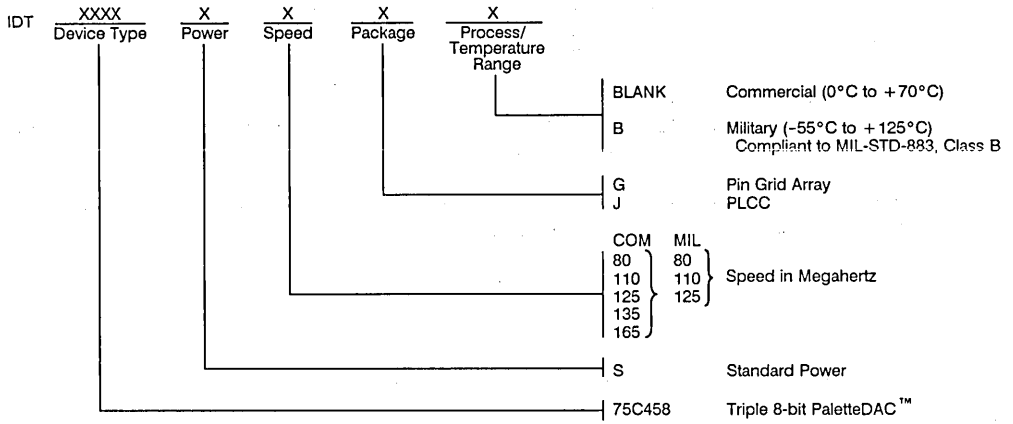


Figure 7. MPU READ Timing Diagram

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS FLASH A/D CONVERTER

IDT75C48

FEATURES:

- 8-bit resolution
- 30 MSPS conversion rate
- Guaranteed no missing codes
- Pin- and function-compatible with TRW 1048
- Low power consumption: 500mW
- Extended analog input range
- On-chip EDC (Error Detection and Correction)
- Improved output logic HIGH drive, no pull-up needed
- No sample and hold required
- Differential Phase < 1 Degree
- Differential Gain < 2%
- Selectable output formats
- TTL-compatible
- Available in 28-pin CERDIP and LCC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88743 is listed for this function

DESCRIPTION:

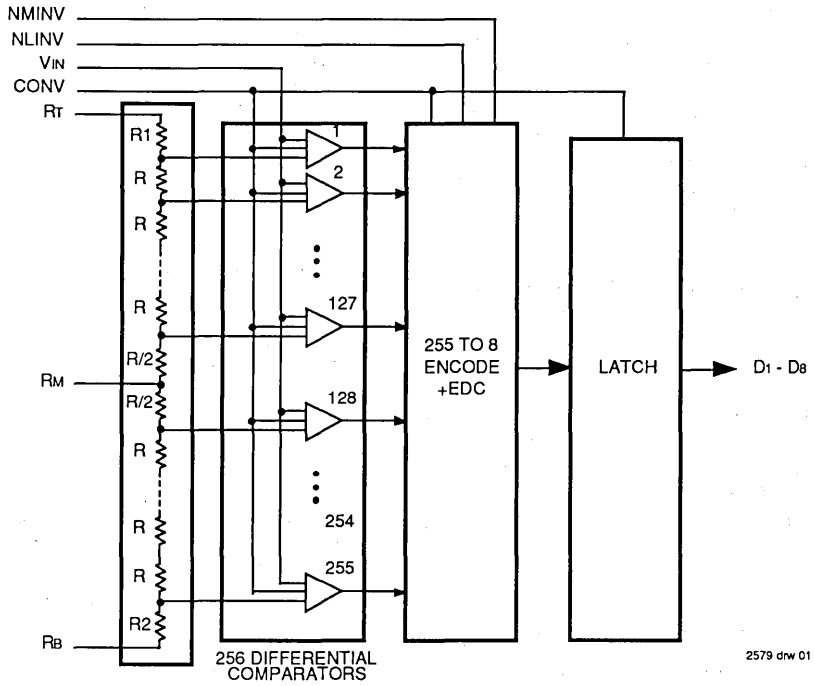
The IDT75C48 is a 30 MegaSample per Second (MSPS), fully parallel, 8-bit Flash Analog to Digital Converter. The wide input analog bandwidth of 10MHz permits the conversion of analog input signals with full-power frequency components up to this limit with no input sample and hold. Low power consumption due to CEMOS™ processing, virtually eliminates thermal considerations. The IDT75C48 is available in 28-pin plastic and hermetic DIPs and a 28-pin LCC.

The IDT75C48 consists of a reference voltage generator, 255 comparators, encoding and EDC (Error Detection and Correction) logic and an output data register. A single clock starts the conversion process and controls all internal operations. Two control inputs allow the output coding format to be programmed for straight binary or offset two's complement in either the true or inverted form.

The IDT75C48 military Flash A/D Converters are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

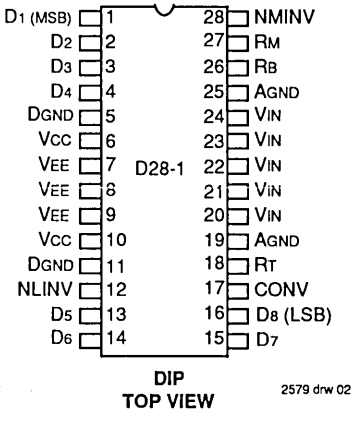
5

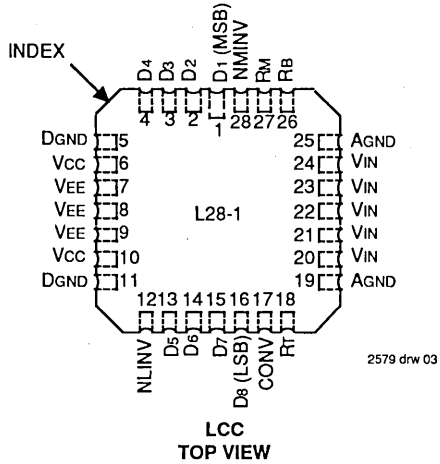
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS





GENERAL INFORMATION

The IDT75C48 has four functional sections: a comparator array, a reference voltage generator, encoding logic with EDC and output logic. The comparator array compares the input signal with 255 reference voltages to produce an N - of - 255 code. This is sometimes called a "Thermometer" code because all of the comparators with their reference voltage less than the input signal will be "on" while those with their reference above the input will be "off".

The reference voltage generator consists of a string of precisely matched resistors which generate the 255 voltages needed by the comparators. The voltages at the ends of the resistor string set the maximum and minimum conversion range and are typically 0V and –2V, respectively.

The encoding logic converts the "Thermometer" code into binary or offset two's complement numbers and can invert either code. Included in the encoding function is Error Detection and Correction logic which ensures that a corrupted Thermometer code is correctly encoded.

The output logic latches and holds the data constant between samples. The output timing is designed for an easy interface to external latches or memories using the same clock as the ADC.

POWER

The IDT75C48 requires two power supply voltages, V_{CC} and V_{EE}. Typically, V_{EE} = –5.2V and V_{CC} = +5.0V. Two separate grounds are provided, AGND and DGND, the analog and digital grounds. The difference between AGND and DGND must not exceed ± 0.1V and all power and ground pins must be connected.

REFERENCE

The IDT75C48 converts analog input signals that are within the range of the reference ($V_{RB} \leq V_{IN} \leq V_{RT}$) into digital form. V_{RB} (Reference Bottom) and V_{RT} (Reference Top) are applied across the reference resistor chain and both must be within the range of +2.1V to –2.1V. In addition, the voltage applied across the reference resistor chain (V_{RT}–V_{RB}) must be between 1.8V and 2.2V, with V_{RT} more positive than V_{RB}. Nominally, V_{RT} = 0.0V and V_{RB} = –2.0V.

The IDT75C48 provides a midpoint tap, RM, which allows the converter to be adjusted for optimum linearity or a non-linear transfer function. Adjustment of RM is not necessary to meet the linearity specification. Figure 5 shows a circuit which will provide approximately 1/2 LSB adjustment of the midpoint. The characteristic impedance of RM is about 170Ω and this node should be driven from a low impedance source. Any noise introduced at this point will couple directly into the resistor chain, seriously affecting performance.

Due to the unavoidable coupling with the clock and the input signal, RT and RB should provide low AC impedance to ground. For applications with a fixed reference, a bypass capacitor is recommend.

CONTROL

The IDT75C48 provides two function control pins, NMINV and NLINV. These controls are for steady state use and are usually tied to the appropriate voltages. They control the output coding format in either straight binary or offset two's complement. In addition, both formats may be either true or inverted. These pins are active low and perform the functions shown in Figure 1.

CONVERT

The IDT75C48 begins a conversion with every rising edge of the convert signal, CONV. The analog input signal is sampled on the rising edge of CONV, while the outputs of the comparators are encoded on the falling edge. The next rising edge latches the encoder output which is presented on the output pins.

The input sample is taken within 15ns of the rising edge of CONV. This is called t_{STO} or the Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a

function of temperature, but the short term uncertainty or jitter is less than 60ps.

If the maximum CONV pulse width HIGH time (tPWH) is exceeded, the accuracy of the input sample may be impaired. The maximum CONV pulse width LOW time (tPWL) may be exceeded, but the digital output data for the sample taken by the previous rising edge of CONV will be meaningless. It is recommended that CONV be held LOW during longer periods of inactivity.

The digital output data is presented at tD, the Digital Output Delay Time, after the next rising edge of CONV. Previous output data is held for the tHO (Output Hold Time) after the rising edge of CONV to allow for non-critical timing in the external circuitry. This means that the data for samples N is acquired while the converter is taking sample N + 2.

ANALOG INPUT

The IDT75C48 uses strobed, auto-zeroing, latching comparators. All five analog input pins must be connected together as close to the package as possible.

If the analog input signal is within the reference voltage range, the output will be a binary number between 0 and 255. An input signal above VRT will yield a full-scale positive output while an input below VRB will cause a full-scale negative output.

Step	Range		Binary		Offset Two's	
	–2.0000V FS 7.8431mV/Step	–2.0480V FS 8.000mV/Step	*NMINV=1 NLINV=1	NMINV=0 NLINV=0	NMINV=0 NLINV=1	NMINV=1 NLINV=0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	–0.0078V	–0.0080V	00000001	11111110	10000001	01111110
⋮	⋮	⋮	⋮	⋮	⋮	⋮
127	–0.9961V	–0.0160V	01111111	10000000	11111111	00000000
128	–1.0039V	–1.0240V	10000000	01111111	00000000	11111111
129	–1.0118V	–1.0320V	10000001	01111110	00000001	11111110
⋮	⋮	⋮	⋮	⋮	⋮	⋮
254	–1.9921V	–2.0320V	11111110	00000001	01111110	10000001
255	–2.0000V	–2.0400V	11111111	00000000	01111111	10000000

*When NMINV and NLINV are both high a 1KΩ series resistor must be inserted between NMINV and Vcc.

2579 drw 04

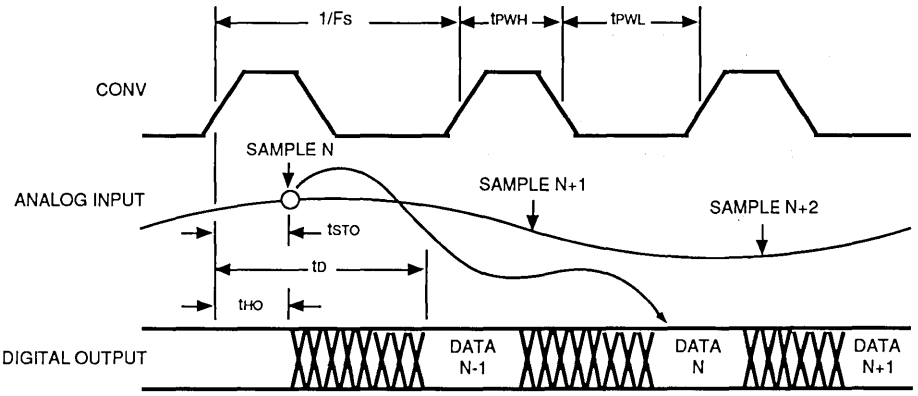


Figure 2. Timing Diagram

2579 drw 05

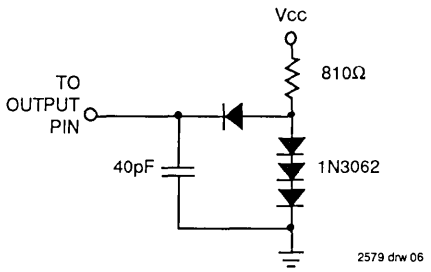


Figure 3. Output Load 1

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
Power Supply			
V_{CC}	Measured to D_{GND}	–0.5 to +7.0	V
V_{EE}	Measured to A_{GND}	+0.5 to –7.0	V
A_{GND}	Measured to D_{GND}	–0.5 to +0.5	V
Input Voltage			
CONV, NMINV, NLINV	Measured to D_{GND}	–0.5 to V_{CC} +0.5	V
V_{IN}, V_{RT}, V_{RB}	Measured to A_{GND}	V_{CC} to V_{EE}	V
V_{RT}	Measured to V_{RB}	–4.0 to +4.0	V
Output			
Applied Voltage (2)	Measured to D_{GND}	–0.5 to V_{CC} +0.5	V
Applied Current (2, 3, 4)	Externally forced	–20.0 to +20.0	mA
Short Circuit Duration	Single output High to D_{GND}	1.0	S
Temperature			
Operating Ambient	Military	–55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	–65 to +150	°C
	Commercial	–55 to +125	°C

2579 tbl 01

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Temperature Range						Unit
			Commercial			Military			
			Min.	Nom.	Max.	Min.	Nom.	Max.	
Power Supply									
V_{CC}	Positive Power Supply		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Power Supply		–4.9	–5.2	–5.5	–4.9	–5.2	–5.5	V
V_{AGND}	Analog Ground Voltage (ref D_{GND})		–0.1	0	+0.1	–0.1	0	+0.1	V
I_{CC}	Positive Supply Current	V_{CC} = Max., Static[1]	—	50	70	—	60	80	mA
I_{EE}	Negative Supply Current	V_{EE} = Max., Static[1]	—	–25	–35	—	–25	–35	mA
Digital Inputs (CONV, NMINV, NLINV)									
V_{IL}	Input Voltage, Logic LOW[4]		–0.5	—	0.8	–0.5	—	0.8	V
V_{IH}	Input Voltage, Logic HIGH[4]		2.0	—	V_{CC} +.1	2.0	—	V_{CC} +.1	V
I_{IL}	Input Current, Logic LOW	V_{CC} = Max., V_{IL} = 0.5V	—	—	±10	—	—	±10	µA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max., V_{IH} = 2.4V	—	—	±10	—	—	±10	µA
I_I	Input Current, Max. Input Voltage	V_{CC} = Max., V_I = V_{CC}	—	—	50	—	—	50	µA
C_I	Digital Input Capacitance[4]	T_A = +25°C, F = 1MHz	—	—	15	—	—	15	pF
Digital Outputs									
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min., I_{OL} = 4.0mA	—	—	0.5	—	—	0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min., I_{OH} = 4.0mA	2.4	—	—	2.4	—	—	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max.[2]	—	—	–50	—	—	–50	mA
Reference									
V_{RT}	Most Positive Reference Voltage[3]		–0.1	0	+0.1	–0.1	0	+0.1	V
V_{RB}	Most Negative Reference Voltage[3]		–1.9	–2.0	–2.1	–1.9	–2.0	–2.1	V
V_{RT}–V_{RB}	Reference Voltage Range		1.8	2.0	2.2	1.8	2.0	2.2	V
I_{REF}	Reference Current (R_T to R_B)	V_{RT}, V_{RB} = Nom.	—	5	9	—	6	10	mA
R_{REF}	Reference Current (R_T to R_B)	V_{RT}, V_{RB} = Nom.	250	400	—	200	330	—	Ohm
Analog Input									
V_{IN}	Input Voltage Range		V_{RB}	—	V_{RT}	V_{RB}	—	V_{RT}	V
R_{IN}	Equiv. Input Resistance[4]	V_{RT}, V_{RB}= Nom., V_{IN} = V_{RB}	100	—	—	100	—	—	KOhm
C_{IN}	Equiv. Input Capacitance[4]	V_{RT}, V_{RB}= Nom., V_{IN} = V_{RB}	—	—	50	—	—	50	pF
I_{CB}	Input Const. Bias Current	V_{EE} = Max.	—	—	10	—	—	10	µA
T_A	Ambient Temperature, Still Air		0	—	70	—	—	—	°C
T_C	Case Temperature		—	—	—	–55	—	+125	°C

NOTES:
2579 tbl 02

1. Worst case, all digital inputs and outputs LOW.
2. Output HIGH, one pin to ground, one second duration.
3. V_{RT} must be more positive than V_{RB} and the voltage reference must be within the specified range. Although the device is specified and tested with the reference equal to 0V and –2V, the part will operate with V_{RT} up to +2.1V. Likewise, the reference range may vary from 1.2V to 2.6V.
4. This parameter is guaranteed but not tested in production.

5

AC ELECTRICAL CHARACTERISTICS FOR IDT75C48SX20 (20MHz Version)

Specifications over the DC Electrical range unless otherwise stated.

Symbol	Parameter	Test Conditions	Temperature Range						Unit
			Commercial			Military			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
FS	Conversion Rate	VCC = Min., VEE = Min.	20	30	—	20	30	—	MSPS
tPWL	CONV, Pulse Width LOW(3)		18	—	100,000	18	—	100,000	ns
tPWH	CONV, Pulse Width HIGH(3)		22	—	20,000	22	—	20,000	ns
tSTO	Sampling Time Offset	VCC = Min., VEE = Min.	0	—	10	0	—	15	ns
EAP	Aperture Error(4)		—	—	60	—	—	60	ps
tD	Digital Output Delay	VCC = Min., VEE = Min., Load 1	—	—	30	—	—	35	ns
tHO	Digital Output Hold Time	VCC = Min., VEE = Min., Load 1	5	—	—	5	—	—	ns
ELI	Linearity Error, Integral	VRT, 1/2 LSB(2)	—	—	0.2	—	—	0.2	%FS
		VRB = Nom. 3/4 LSB(2)	—	—	0.3	—	—	0.3	%FS
ELD	Linearity Error, Differential	VRT, VRB = Nom.	—	—	0.2	—	—	0.2	%FS
CS	Code Size(1)		25	100	175	25	100	175	%Nom
EOT	Offset Error, Top	VIN = midpoint code 0	—	10	45	—	10	45	mV
EOB	Offset Error, Bottom	VIN = midpoint code 255	—	–10	–30	—	–10	–30	mV
TCO	Offset Error, Temperature Coefficient(4)	VIN = VRB	—	—	±20	—	—	±20	µV/°C
BW	Bandwidth, Full Power Input		7	12	—	5	10	—	MHz
TTR	Transient Response, Full Scale(5)		—	—	20	—	—	20	nS
SNR	Signal to Noise Ratio	20 MSPS Conversion Rate, 10 MHz Bandwidth							
	Peak Signal/RMS Noise	1.248 MHz Input	54	56	—	53	55	—	dB
		2.438 MHz Input	53	56	—	52	55	—	dB
	RMS Signal/RMS Noise	1.248 MHz Input	45	47	—	44	46	—	dB
		2.438 MHz Input	44	47	—	43	46	—	dB
NPR	Noise Power Ratio	DC to 8 MHz White Noise Bandwidth 4 Sigma Loading 1.248 MHz Slot 20 MSPS Conversion Rate	36.5	39	—	36.5	39	—	dB
DP	Differential Phase Error	FS = 4 x NTSC	—	.5	1	—	.5	1	Degree
DG	Differential Gain Error	FS = 4 x NTSC	—	1	2	—	1	2	%

NOTES:

2579 tbl 03

1. Guarantees no missing codes.
2. See the ordering information section regarding the part number designation.
3. No damage to the part will occur if the Max. times are exceeded. See the Convert section for more information about the Conv Max. time limitations.
4. This parameter is guaranteed but not tested in production.

AC ELECTRICAL CHARACTERISTICS FOR IDT75C48SX30 (30MHz Version)

Specifications over the DC Electrical range unless otherwise stated.

Symbol	Parameter	Test Conditions	Temperature Range						Unit
			Commercial			Military			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
FS	Conversion Rate	VCC = Min., VEE = Min.	30	40	—	30	40	—	MSPS
tPWL	CONV, Pulse Width LOW		14	—	100,000	14	—	100,000	ns
tPWH	CONV, Pulse Width HIGH		14	—	20,000	14	—	20,000	ns
tSTO	Sampling Time Offset	VCC = Min., VEE = Min.	0	—	10	0	—	15	ns
EAP	Aperture Error[4]		—	—	60	—	—	60	ps
tD	Digital Output Delay	VCC = Min., VEE = Min., Load 1	—	—	25	—	—	28	ns
tHO	Digital Output Hold Time	VCC = Min., VEE = Min., Load 1	5	—	—	5	—	—	ns
ELI	Linearity Error, Integral	VRT, 3/4 LSB[2]	—	—	0.3	—	—	0.3	%FS
		VRB = Nom. 1 LSB[2]	—	—	0.4	—	—	0.4	%FS
ELD	Linearity Error, Differential	VRT, VRB = Nom.	—	—	0.2	—	—	0.2	%FS
CS	Code Size[1]		25	100	175	25	100	175	%Nom
EOT	Offset Error, Top	VIN = midpoint code 0	—	10	45	—	10	45	mV
EOB	Offset Error, Bottom	VIN = midpoint code 255	—	–10	–30	—	–10	–30	mV
TCO	Offset Error, Temperature Coefficient[4]	VIN = VRB	—	—	±20	—	—	±20	µV/°C
BW	Bandwidth, Full Power Input		10	13	—	8	10	—	MHz
TTR	Transient Response, Full Scale[4]		—	—	20	—	—	20	nS
SNR	Signal to Noise Ratio	30 MSPS Conversion Rate, 15 MHz Bandwidth							
	Peak Signal/RMS Noise	5 MHz Input	44	48	—	44	48	—	dB
		10 MHz Input	44	48	—	44	48	—	dB
	RMS Signal/RMS Noise	5 MHz Input	35	39	—	35	39	—	dB
		10 MHz Input	35	39	—	35	39	—	dB
NPR	Noise Power Ratio	DC to 15 MHz White Noise Bandwidth 4 Sigma Loading 5 MHz Slot 30 MSPS Conversion Rate	—	—	—	—	—	—	dB
DP	Differential Phase Error	FS = 4 x NTSC	—	.5	1	—	.5	1	Degree
DG	Differential Gain Error	FS = 4 x NTSC	—	1	2	—	1	2	%

NOTES:

2579 tbl 04

1. Guarantees no missing codes.
2. See the ordering information section regarding the part number designation.
4. No damage to the part will occur if the Max. times are exceeded. See the Convert section for more information about the Conv Max. time limitations.
5. This parameter is guaranteed but not tested in production.

5

CALIBRATION

The calibration of the IDT75C58 involves the setting of the 1st and 255th comparator thresholds to the desired voltages. This is done be varying the top and bottom voltages on the reference resistor chain, V_{RT} and V_{RB}, to compensate for any internal offsets. Assuming a nominal 0V to –2V reference range, apply –0.0039V (1/2 LSB from 0V) to the analog input, continuously strobe the device and adjust V_{RT} until the OVFL output toggles between 0 and 1. To adjust the first comparator, apply –1.996V (1/2 LSB from –2V) to the analog input and adjust V_{RB} until the converter output toggles between the codes 0 and 1.

The offset errors are caused by the parasitic resistance between the package pins and the actual resistor chain on-chip and are shown as R1 and R2 in the Functional Block Diagram. The offset errors, E_{OT} and E_{OB}, are specified in the AC Electrical Characteristics and indicate the degree of adjustment needed.

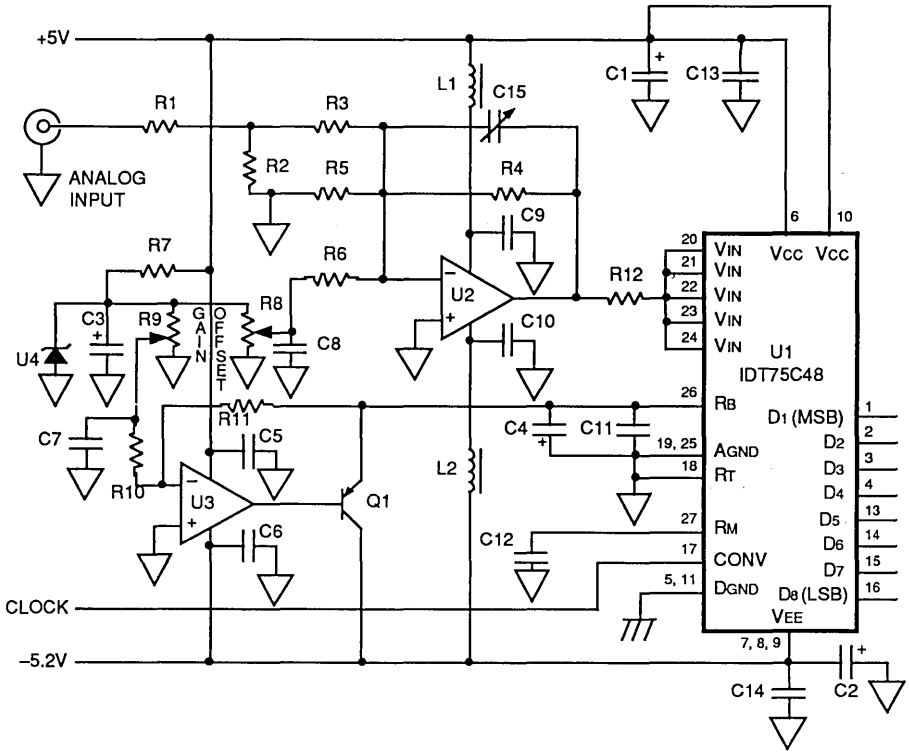
The previously described calibration scheme requires that both ends of the reference resistor chain be adjustable, i.e. be driven by operational amplifiers. A simpler method is to connect the top of the resistor chain, R_T, to analog ground or 0V and to adjust this end of the range with the input buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error which can be compensated for by varying the voltage applied to R_B. This is a preferred method for gain adjustment since it is not the input signal path. See Figure 5 for a detailed circuit diagram of this method.

TYPICAL INTERFACE

Figure 5 shows a typical application example for the IDT75C58. The analog input amplifier is a bipolar wideband operational amplifier whose low impedance output directly drives the A/D Converter. The input buffer amplifier is configured with a gain of minus two which will convert a standard video input signal (1V p–p) to the recommended 2V converter input range. Both V_{IN} pins are connected together as close to the package as possible and the input buffer feedback loop is closed at this point. Bipolar inputs, as well as the calibration of the reference top, are accomplished using the offset control. A band-gap reference is used to provide a stable voltage for both the offset and gain control. A variable capacitor in the input buffer feedback loop allows optimization of either the step or the frequency response and may be replaced by a fixed value in the final version of the printed circuit board.

To ensure operation to the rated specifications, proper decoupling is needed. The bypass capacitors should be located close to the chip with the shortest lead lengths possible. Massive ground planes are recommended. If separate digital and ground planes are used, they should be connected together at one point close to the IDT75C58.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier buffered by a PNP transistor. The transistor provides a low impedance source and is necessary to provide the current flowing through the resistor chain. The bottom reference voltage may be adjusted to cancel the gain error introduced by the offset voltage, E_{OB}, as discussed in the calibration section.



PARTS LIST

R1	0.0Ω
R2	80.7Ω
R3	1KΩ
R4	2KΩ
R5	220Ω
R6	2KΩ
R7	1KΩ
R8	2KΩ
R9	2KΩ
R10	10KΩ
R11	20KΩ
R12	27Ω
C1-C4	10µF
C5-C14	0.1µF
C15	1-6pF Variable
U1	IDT75C48
U2	HA-2539-5
U3	uA741C
U4	LM313
Q1	2N2907
L1, L2	Ferrite Bead

Figure 4. Application Example

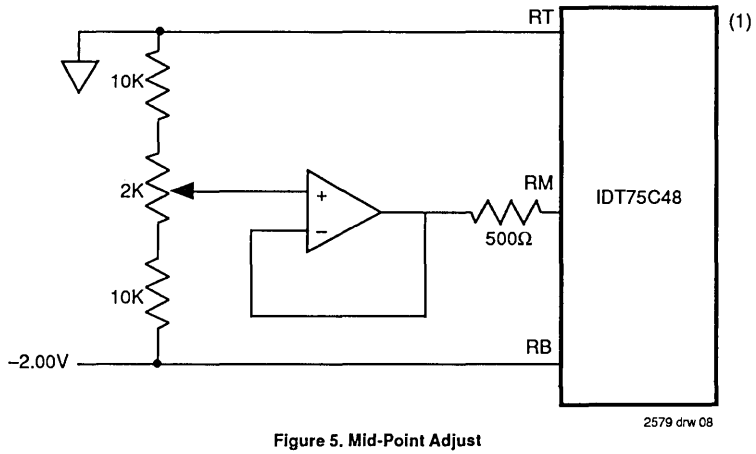
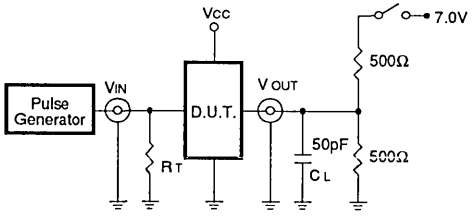


Figure 5. Mid-Point Adjust

NOTE:
1. When NMINV and NLINV are both HIGH a 1KΩ series register must be inserted between NMINV and Vcc.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



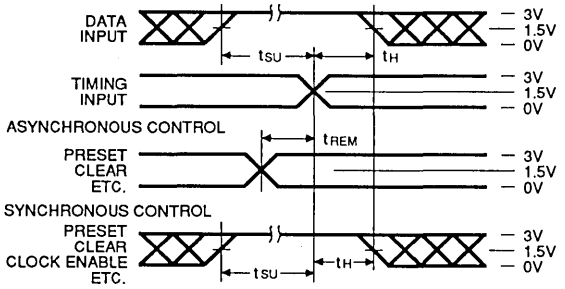
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

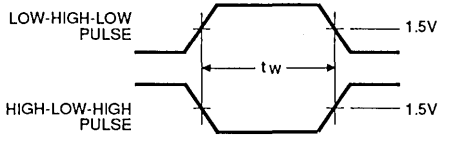
DEFINITIONS: 2578 tbl 6

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

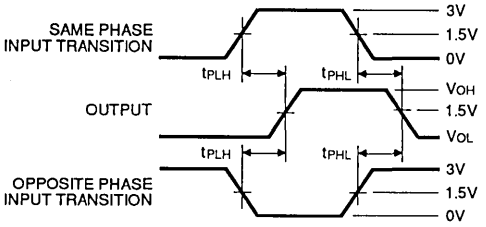
SET-UP, HOLD AND RELEASE TIMES



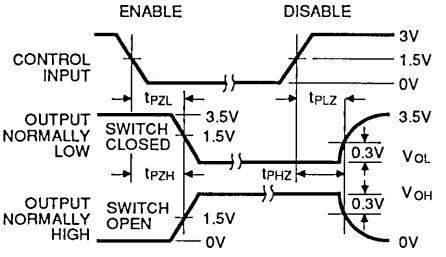
PULSE WIDTH



PROPAGATION DELAY



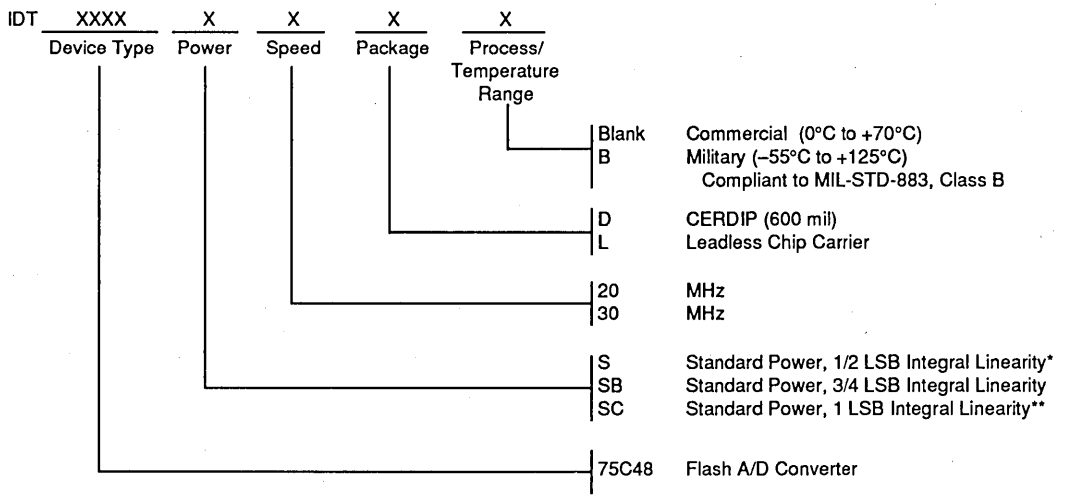
ENABLE AND DISABLE TIMES



NOTES 2578 drw 12

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2579 drw 09

* 20 MHz Version only
** 30 MHz Version only

5

Integrated Device Technology, Inc.

CMOS FLASH A/D CONVERTER

IDT75C58

FEATURES:

- 8-bit resolution
- 30 MSPS conversion rate
- Overflow output
- Low power consumption: 500mW
- Guaranteed no missing codes
- Power-Down mode
- Extended analog input range
- On-chip EDC (Error Detection and Correction)
- Tri-state outputs
- Improved output logic HIGH drive, no pull-up needed
- No sample and hold required
- Differential Phase = 1 Degree
- Differential Gain = 2%
- TTL-compatible
- Available in 28-pin CERDIP or LCC
- Military product compliant to MIL-STD-883, Class B

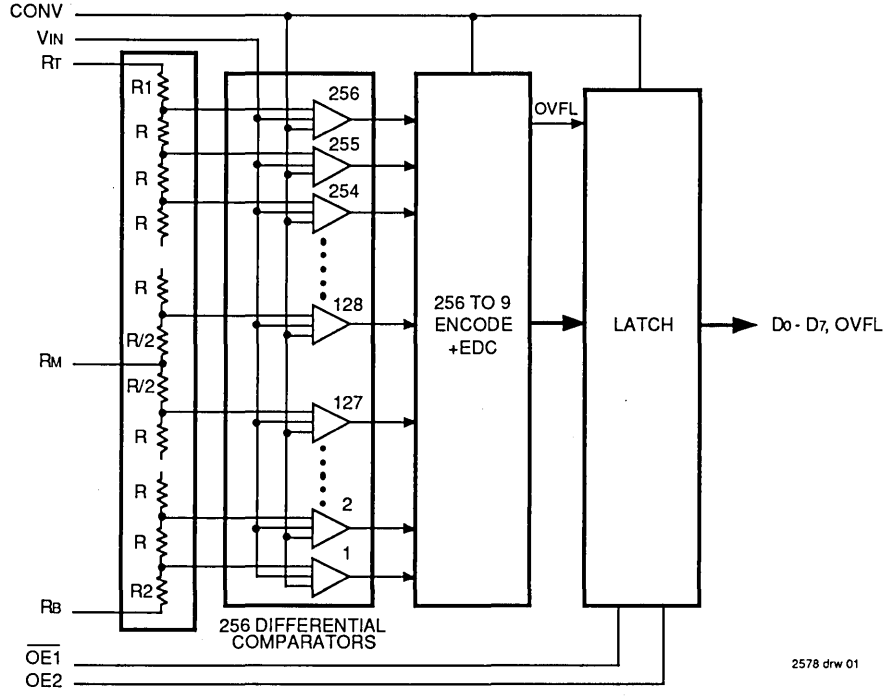
DESCRIPTION:

The IDT75C58 is a 30 MegaSample per Second (MSPS), fully parallel, 8-bit Flash Analog to Digital Converter. The wide input analog bandwidth of 10MHz permits the conversion of analog input signals with full-power frequency components up to this limit with no input sample and hold. Low power consumption, due to CEMOS™ processing, virtually eliminates thermal considerations. The IDT75C58 is available in 28-pin plastic and hermetic DIPs and a 28-pin LCC.

The IDT75C58 consists of a reference voltage generator, 256 comparators, encoding and EDC (Error Detection and Correction) logic and an output data register. A single clock starts the conversion process and controls all internal operations. An additional comparator detects an Overflow condition (V_{IN} more positive than Full-Scale +1LSB) and activates the OVFL output. This output, together with two output enable inputs ($\overline{OE1}$ and OE2), allow the stacking of two IDT75C58s for 9-bit resolution with no external components.

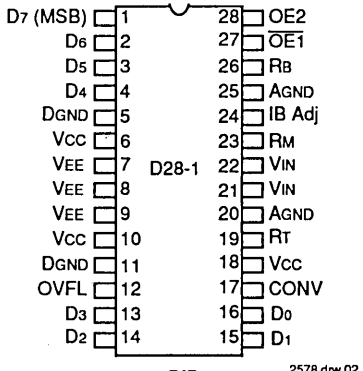
The IDT75C58 military Flash A/D Converters are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

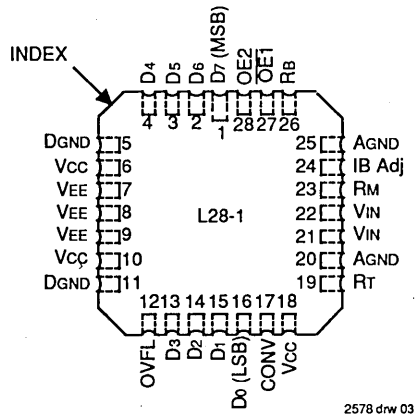


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

GENERAL INFORMATION

The IDT75C58 has four functional sections: a comparator array, a reference voltage generator, encoding logic with EDC and output logic. The comparator array compares the input signal with 256 reference voltages to produce an N - of - 256 code. This is sometimes called a "Thermometer" code because all of the comparators with their reference voltage less than the input signal will be "on" while those with their reference above the input will be "off".

The reference voltage generator consists of a string of precisely matched resistors which generate the 256 voltages needed by the comparators. The voltages at the ends of the resistor string set the maximum and minimum conversion range and are typically 0V and –2V, respectively.

Included in the encoding function is Error Detection and Correction logic which ensures that a corrupted Thermometer code is correctly encoded.

The output logic latches and holds the data constant between samples. The output timing is designed for an easy interface to external latches or memories using the same clock as the ADC.

POWER

The IDT75C58 requires two power supply voltages, V_{CC} and V_{EE}. Typically, V_{EE} = –5.0V and V_{CC} = +5.0V. Two separate grounds are provided, AGND and DGND, the analog and digital grounds. The difference between AGND and DGND must not exceed ± 0.1V and all power and ground pins must be connected.

REFERENCE

The IDT75C58 converts analog input signals that are within the range of the reference ($V_{RB} \leq V_{IN} \leq V_{RT}$) into digital form. V_{RB} (Reference Bottom) and V_{RT} (Reference Top) are applied across the reference resistor chain and both must be within the range of +2.1V to –2.1V. In addition, the voltage applied across the reference resistor chain (V_{RT}–V_{RB}) must be between 1.8V and 2.2V, with V_{RT} more positive than V_{RB}. Nominally, V_{RT} = 0.0V and V_{RB} = –2.0V.

The IDT75C58 provides a midpoint tap, RM, which allows the converter to be adjusted for optimum linearity or a non-linear transfer function. Adjustment of RM is not necessary to meet the linearity specification. Figure 6 shows a circuit which will provide approximately 1/2 LSB adjustment to the midpoint. The characteristic impedance of RM is about 170Ω and this node should be driven from a low impedance source. Any noise introduced at this point will couple directly into the resistor chain, seriously affecting performance.

Due to the unavoidable coupling with the clock and the input signal, RT and RB should provide low AC impedance to ground. For applications with a fixed reference, a bypass capacitor is recommended.

CONTROL

Two function control pins, $\overline{OE1}$ and OE2, control the outputs with the function shown in Table 1.

IB Adj

An analog control pin, IB Adj, controls the bias current in the comparators. Normally, this pin is connected to analog ground. To reduce the quiescent current, a "power-down" mode, IB Adj, may be connected to VEE. For somewhat better analog performance at higher input frequencies, IB Adj may be connected to a voltage between AGND and VCC.

CONVERT

The IDT75C58 begins a conversion with every rising edge of the convert signal, CONV. The analog input signal is sampled on the rising edge of CONV, while the outputs of the comparators are encoded on the falling edge. The next rising edge latches the encoder output which is presented on the output pins.

5

The input sample is taken within 15ns of the rising edge of CONV. This is called tSTO or the Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short term uncertainty or jitter is less than 60ps. The maximum CONV pulse width LOW time (tPWL) may be exceeded, but the digital output data for the sample taken by the previous rising edge of CONV will be meaningless. It is recommended that CONV be held LOW during longer periods of inactivity.

The digital output data is presented at tD, the Digital Output Delay Time, after the next rising edge of CONV. Previous output data is held for the tHO (Output Hold Time) after the rising edge of CONV to allow for non-critical timing in the external circuitry. This means that the data for sample N is acquired while the converter is taking sample N + 2.

ANALOG INPUT

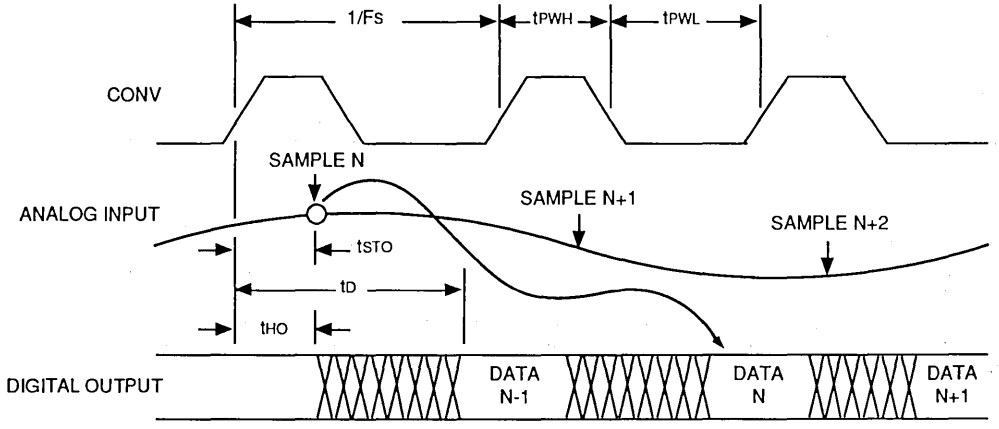
The IDT75C58 uses strobed, auto-zeroing, latching comparators. Both analog input pins must be connected together as close the package as possible. The input signal must remain within the range of VCC to VEE to prevent damage to the device.

If the analog input signal is within the reference voltage range, the output will be a binary number between 0 and 255. An input signal below VRB will yield a full-scale (all outputs low) output while an input above VRT will cause OVFL output.

Step	Range		Output	OVFL
	-2.0000V FS 7.8125mV/Step	-2.0480V FS 8.000mV/Step		
256	0.0000V	0.0000V	11111111	1
255	-0.0078V	-0.0080V	11111111	0
254	-0.0156V	-0.0160V	11111110	0
•	•	•	•	•
129	-0.9961V	-0.0160V	10000000	0
128	-1.0039V	-1.0240V	01111111	0
127	-1.0118V	-1.0320V	01111110	0
•	•	•	•	•
001	-1.9921V	-2.040V	00000001	0
000	-2.0000V	-2.048V	00000000	0

2578 drw 04

Figure 1. Output Coding



2578 drw 05

Figure 2. Timing Diagram

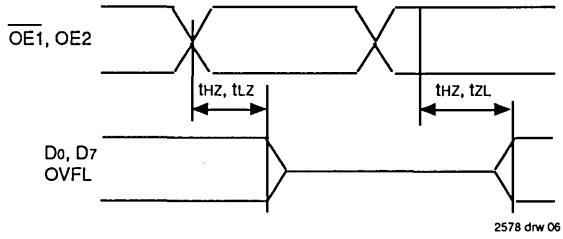


Figure 3. Output, Enable/Disable Timing

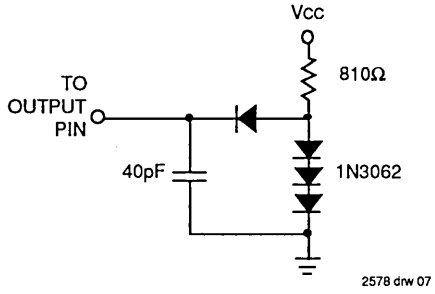


Figure 4. Output Load 1

$\overline{OE1}$	OE2	D0 - D7	OVFL
0	1	Valid	Valid
1	1	High Z	Valid
X	0	High Z	High Z

2578tbl01

Table 1. Function Control

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
Power Supply			
VCC	Measured to DGND	–0.5 to +7.0	V
VEE	Measured to AGND	–0.5 to –7.0	V
AGND	Measured to DGND	–0.5 to +0.5	V
Input Voltage			
CONV, $\overline{OE1}$, OE2	Measured to DGND	–0.5 to VCC +0.5	V
VIN, VRT, VRB	Measured to AGND	VCC to VEE	V
VRT	Measured to VRB	–4.0 to +4.0	V
Output			
Applied Voltage (2)	Measured to DGND	–0.5 to VCC +0.5	V
Applied Current (2, 3, 4)	Externally forced	–3.0 to +6.0	mA
Short Circuit Duration	Single output High to DGND	1.0	S
Temperature			
Operating, Ambient	Military	–55 to +125	°C
	Commercial	–0 to +70	°C
Storage	Military	–65 to +150	°C
	Commercial	–55 to +125	°C

2578 tbl 02

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

5

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Temperature Range						Unit
			Commercial			Military			
			Min.	Nom.	Max.	Min.	Nom.	Max.	
Power Supply									
V_{CC}	Positive Power Supply		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Power Supply		–4.75	–5.2	–5.5	–4.5	–5.2	–5.5	V
V_{AGND}	Analog Ground Voltage (ref D_{GND})		–0.1	0	+0.1	–0.1	0	+0.1	V
I_{CC}	Positive Supply Current	V_{CC} = Max., Static[1]	—	50	70	—	60	80	mA
I_{EE}	Negative Supply Current	V_{EE} = Max., Static[1]	—	–15	–25	—	–15	–25	mA
Digital Inputs (CONV, NMINV, NLINV)									
V_{IL}	Input Voltage, Logic LOW[4]		–0.5	—	0.8	–0.5	—	0.8	V
V_{IH}	Input Voltage, Logic HIGH[4]		2.0	—	V_{CC} +.1	2.0	—	V_{CC} +.1	V
I_{IL}	Input Current, Logic LOW	V_{CC} = Max., V_{IL} = 0.5V	—	—	±10	—	—	±10	µA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max., V_{IH} = 2.4V	—	—	±10	—	—	±10	µA
I_I	Input Current, Max. Input Voltage	V_{CC} = Max., V_I = V_{CC}	—	—	50	—	—	50	µA
C_I	Digital Input Capacitance[4]	T_A = +25°C, F = 1MHz	—	—	15	—	—	15	pF
Digital Outputs									
I_{OL}	Output Current, Logic LOW	V_{CC} = Min., V_O = 0.4V	—	—	4.0	—	—	4.0	mA
I_{OH}	Output Current, Logic HIGH	V_{CC} = Min., V_O = 2.4V	—	—	–2	—	—	–2	mA
I_{OZ}	Output HIGH Z Current[4]	V_{CC} = Max.	—	5	—	—	5	—	µA
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min., I_{OH} = Max.	2.4	—	—	2.4	—	—	V
V_{OL}	Output Voltage, Logic Low	V_{CC} = Min., I_{OL} = Max.	—	—	0.5	—	—	0.5	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max.[2]	—	—	–50	—	—	–50	mA
Reference									
V_{RT}	Most Positive Reference Voltage[3]		–0.1	0	+0.1	–0.1	0	+0.1	V
V_{RB}	Most Negative Reference Voltage[3]		–1.9	–2.0	–2.1	–1.9	–2.0	–2.1	V
V_{RT}–V_{RB}	Reference Voltage Range		1.8	2.0	2.2	1.8	2.0	2.2	V
I_{REF}	Reference Current (R_T to R_B)	V_{RT}, V_{RB} = Nom.	—	5	9	—	6	10	mA
R_{REF}	Reference Current (R_T to R_B)	V_{RT}, V_{RB} = Nom.	250	400	—	220	330	—	Ohm
Analog Input									
V_{IN}	Input Voltage Range		V_{RB}	—	V_{RT}	V_{RB}	—	V_{RT}	V
R_{IN}	Equiv. Input Resistance[4]	V_{RT}, V_{RB}= Nom., V_{IN} = V_{RB}	100	—	—	100	—	—	KOhm
C_{IN}	Equiv. Input Capacitance[4]	V_{RT}, V_{RB}= Nom., V_{IN} = V_{RB}	—	—	50	—	—	50	pF
I_{CB}	Input Const. Bias Current	V_{EE} = Max.	—	—	10	—	—	10	µA
T_A	Ambient Temperature, Still Air		0	—	70	—	—	—	°C
T_C	Case Temperature		—	—	—	–55	—	+125	°C

NOTES:

2578 tbl 03

1. Worst case, all digital inputs and outputs LOW.
2. Output HIGH, one pin to ground, one second duration.
3. V_{RT} must be more positive than V_{RB} and the voltage reference must be within the specified range. Although the device is specified and tested with the reference equal to 0V and –2V, the part will operate with V_{RT} up to +2.1V. Likewise, the reference range may vary from 1.2V to 2.6V.
4. This parameter is guaranteed but not tested in production.

AC ELECTRICAL CHARACTERISTICS FOR IDT75C58X20 (20MHz Version)

Specifications over the DC Electrical range unless otherwise stated.

Symbol	Parameter	Test Conditions	Temperature Range						Unit
			Commercial			Military			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
FS	Conversion Rate	VCC = Min., VEE = Min.	20	30	—	20	30	—	MSPS
tPWL	CONV, Pulse Width LOW(4)		18	—	100,000	18	—	100,000	ns
tPWH	CONV, Pulse Width HIGH(4)		22	—	20,000	22	—	20,000	ns
tSTO	Sampling Time Offset	VCC = Min., VEE = Min.	0	—	10	0	—	15	ns
EAP	Aperture Error(5)		—	—	60	—	—	60	ps
tD	Digital Output Delay	VCC = Min., VEE = Min., Load 1	—	—	30	—	—	35	ns
tHO	Digital Output Hold Time	VCC = Min., VEE = Min., Load 1	5	—	—	5	—	—	ns
tHZ	Output Disable Time from HIGH(5)	VCC = Min., VEE = Min., Load 1	—	5	10	—	5	10	ns
tLZ	Output Disable Time from LOW(5)	VCC = Min., VEE = Min., Load 1	—	5	10	—	5	10	ns
tZH	Output Enable Time to HIGH(5)	VCC = Min., VEE = Min., Load 1	—	12	18	—	12	—	ns
tZL	Output Enable Time to LOW(5)	VCC = Min., VEE = Min., Load 1	—	12	18	—	12	18	ns
ELI	Linearity Error, Integral	VRT, 1/2 LSB(2)	—	—	0.2	—	—	0.2	%FS
		VRB = Nom. 3/4 LSB(2)	—	—	0.3	—	—	0.3	%FS
ELD	Linearity Error, Differential	VRT, VRB = Nom.	—	—	0.2	—	—	0.2	%FS
CS	Code Size(1)		25	100	175	25	100	175	%Nom
EOT	Offset Error, Top	VIN = Midpoint Code 255	—	10	20	—	10	20	mV
EOB	Offset Error, Bottom	VIN = Midpoint Code 0	—	–10	–20	—	–10	–20	mV
EOO	Offset Error, OVFL(3)	VIN = VRT	–6	0	6	–6	0	6	mV
TCO	Offset Error, Temperature Coefficient(5)	VIN = VRB	—	—	±20	—	—	±20	µV/°C
BW	Bandwidth, Full Power Input		7	12	—	5	10	—	MHz
TTR	Transient Response, Full Scale(5)		—	—	20	—	—	20	ns
SNR	Signal to Noise Ratio	20 MSPS Conversion Rate, 10MHz Bandwidth							
	Peak Signal/RMS Noise	1.248MHz Input	54	56	—	53	55	—	dB
		2.438MHz Input	53	56	—	52	55	—	dB
	RMS Signal/RMS Noise	1.248MHz Input	45	47	—	44	46	—	dB
		2.438MHz Input	44	47	—	43	46	—	dB
NPR	Noise Power Ratio	DC to 10MHz White Noise Bandwidth 4 Sigma Loading 1.248MHz Slot 20 MSPS Conversion Rate	36.5	39	—	36.5	39	—	dB
DP	Differential Phase Error	FS = 4 x NTSC	—	.5	1	—	.5	1	Degree
DG	Differential Gain Error	FS = 4 x NTSC	—	1	2	—	1	2	%

NOTES:

2578 tbl 04

1. Guarantees no missing codes.
2. See the ordering information section regarding the part number designation.
3. A 0mV offset means 1 LSB above the 255th code threshold.
4. No damage to the part will occur if the Max. times are exceeded. See the Convert section for more information about the Conv Max. time limitations.
5. This parameter is guaranteed but not tested in production.

AC ELECTRICAL CHARACTERISTICS FOR IDT75C58X30 (30MHz Version)

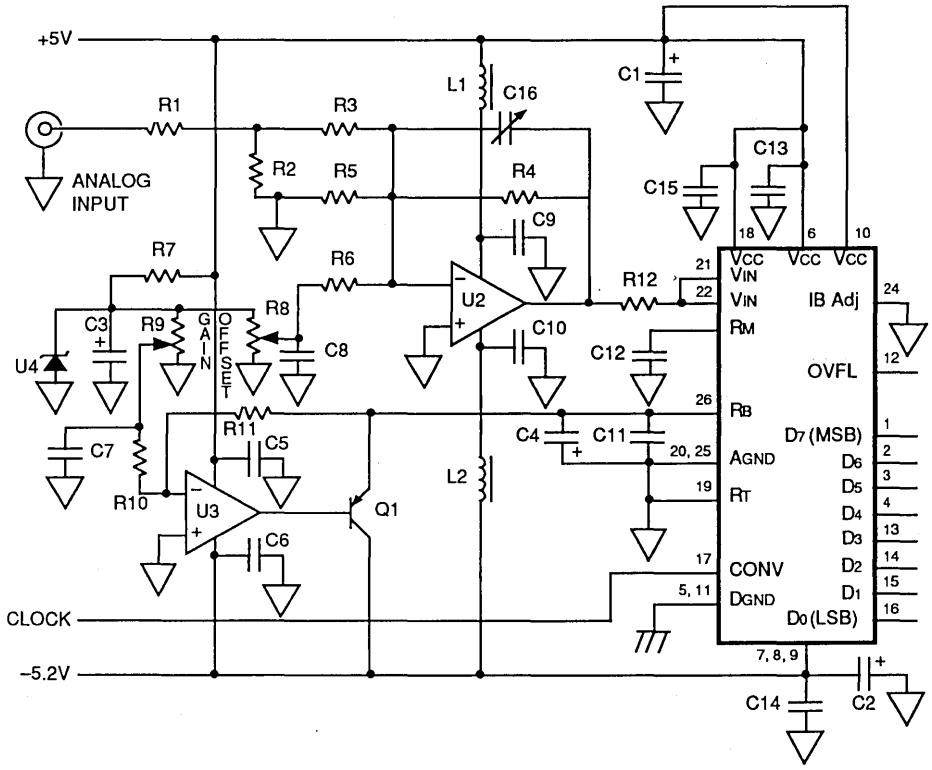
Specifications over the DC Electrical range unless otherwise stated.

Symbol	Parameter	Test Conditions	Temperature Range						Unit
			Commercial			Military			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
FS	Conversion Rate	VCC = Min., VEE = Min.	30	40	—	30	40	—	MSPS
tPWL	CONV, Pulse Width LOW(4)		14	—	100,000	14	—	100,000	ns
tPWH	CONV, Pulse Width HIGH(4)		14	—	20,000	14	—	20,000	ns
tSTO	Sampling Time Offset	VCC = Min., VEE = Min.	0	—	10	0	—	15	ns
EAP	Aperture Error(5)		—	—	60	—	—	60	ps
tD	Digital Output Delay	VCC = Min., VEE = Min., Load 1	—	—	25	—	—	28	ns
tHO	Digital Output Hold Time	VCC = Min., VEE = Min., Load 1	5	—	—	5	—	—	ns
tHZ	Output Disable Time from HIGH(5)	VCC = Min., VEE = Min., Load 1	—	5	—	—	5	—	ns
tLZ	Output Disable Time from LOW(5)	VCC = Min., VEE = Min., Load 1	—	5	—	—	5	—	ns
tZH	Output Enable Time to HIGH(5)	VCC = Min., VEE = Min., Load 1	—	12	—	—	12	—	ns
tZL	Output Enable Time to LOW(5)	VCC = Min., VEE = Min., Load 1	—	12	—	—	12	—	ns
ELI	Linearity Error, Integral	VRT, 3/4 LSB(2)	—	—	0.3	—	—	0.3	%FS
		VRB = Nom. 1 LSB(2)	—	—	0.4	—	—	0.4	%FS
ELD	Linearity Error, Differential	VRT, VRB = Nom.	—	—	0.2	—	—	0.2	%FS
CS	Code Size(1)		25	100	175	25	100	175	%Nom
EOT	Offset Error, Top	VIN = Midpoint Code 255	—	10	45	—	45	20	mV
EOB	Offset Error, Bottom	VIN = Midpoint Code 0	—	–10	–30	—	–30	–20	mV
EOO	Offset Error, OVFL(3)	VIN = VRT	–6	0	6	–6	0	6	mV
TCO	Offset Error, Temperature Coefficient(5)	VIN = VRB	—	—	±20	—	—	±20	µV/°C
BW	Bandwidth, Full Power Input		10	13	—	8	10	—	MHz
TTR	Transient Response, Full Scale(5)		—	—	20	—	—	20	ns
SNR	Signal to Noise Ratio	30 MSPS Conversion Rate, 15MHz Bandwidth							
	Peak Signal/RMS Noise	5MHz Input	44	48	—	44	48	—	dB
		10MHz Input	44	48	—	44	48	—	dB
	RMS Signal/RMS Noise	5MHz Input	35	39	—	35	39	—	dB
		10MHz Input	35	39	—	35	39	—	dB
NPR	Noise Power Ratio	DC to 15MHz White Noise Bandwidth 4 Sigma Loading 5MHz Slot 30 MSPS Conversion Rate	—	—	—	—	—	—	dB
DP	Differential Phase Error	FS = 4 x NTSC	—	.5	1	—	.5	1	Degree
DG	Differential Gain Error	FS = 4 x NTSC	—	1	2	—	1	2	%

NOTES:

2578 tbl 05

1. Guarantees no missing codes.
2. See the ordering information section regarding the part number designation.
3. A 0mV offset means 1 LSB above the 255th code threshold.
4. No damage to the part will occur if the Max. times are exceeded. See the Convert section for more information about the Conv Max. time limitations.
5. This parameter is guaranteed but not tested in production

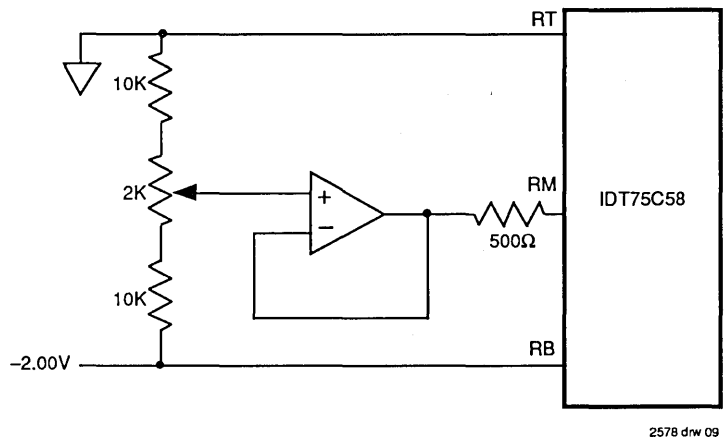


PARTS LIST

R1	0.0Ω
R2	80.7Ω
R3	1KΩ
R4	2KΩ
R5	22Ω
R6	2KΩ
R7	1KΩ
R8	2KΩ
R9	2KΩ
R10	10KΩ
R11	20KΩ
R12	27Ω
C1-C4	10µF
C5-C15	0.1µF
C16	1-6pF Variable
U1	IDT75C58
U2	HA-2539-5
U3	uA741C
U4	LM313
Q1	2N2907
L1, L2	Ferrite Bead

2578 drw 08

Figure 5. Application Example



2578 drw 09

Figure 6. Mid-Point Adjust

CALIBRATION

The calibration of the IDT75C58 involves the setting of the 1st and 255th comparator thresholds to the desired voltages. This is done by varying the top and bottom voltages on the reference resistor chain, V_{RT} and V_{RB}, to compensate for any internal offsets. Assuming a nominal 0V to –2V reference range, apply –0.0039V (1/2 LSB from 0V) to the analog input, continuously strobe the device and adjust V_{RT} until the OVFL output toggles between 0 and 1. To adjust the first comparator, apply –1.996V (1/2 LSB from –2V) to the analog input and adjust V_{RB} until the converter output toggles between the codes 0 and 1.

The offset errors are caused by the parasitic resistance between the package pins and the actual resistor chain on-chip and are shown as R1 and R2 in the Functional Block Diagram. The offset errors, E_{OT} and E_{OB}, are specified in the AC Electrical Characteristics and indicate the degree of adjustment needed.

The previously described calibration scheme requires that both ends of the reference resistor chain be adjustable, i.e. be driven by operational amplifiers. A simpler method is to connect the top of the resistor chain, R_T, to analog ground or 0V and to adjust this end of the range with the input buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error which can be compensated for by varying the voltage applied to R_B. This is a preferred method for gain adjustment since it is not the input signal path. See Figure 5 for a detailed circuit diagram of this method.

TYPICAL INTERFACE

Figure 5 shows a typical application example for the IDT75C58. The analog input amplifier is a bipolar wideband operational amplifier whose low impedance output directly drives the A/D Converter. The input buffer amplifier is configured with a gain of minus two which will convert a standard video input signal (1V p–p) to the recommended 2V converter input range. Both V_{IN} pins are connected together as close to the package as possible and the input buffer feedback loop is closed at this point. Bipolar inputs, as well as the calibration of the reference top, are accomplished using the offset control. A band-gap reference is used to provide a stable voltage for both the offset and gain control. A variable capacitor in the input buffer feedback loop allows optimization of either the step or the frequency response and may be replaced by a fixed value in the final version of the printed circuit board.

To ensure operation to the rated specifications, proper decoupling is needed. The bypass capacitors should be located close to the chip with the shortest lead lengths possible. Massive ground planes are recommended. If separate digital and ground planes are used, they should be connected together at one point close to the IDT75C58.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier buffered by a PNP transistor. The transistor provides a low impedance source and is necessary to provide the current flowing through the resistor chain. The bottom reference voltage may be adjusted to cancel the gain error introduced by the offset voltage, E_{OB}, as discussed in the calibration section.

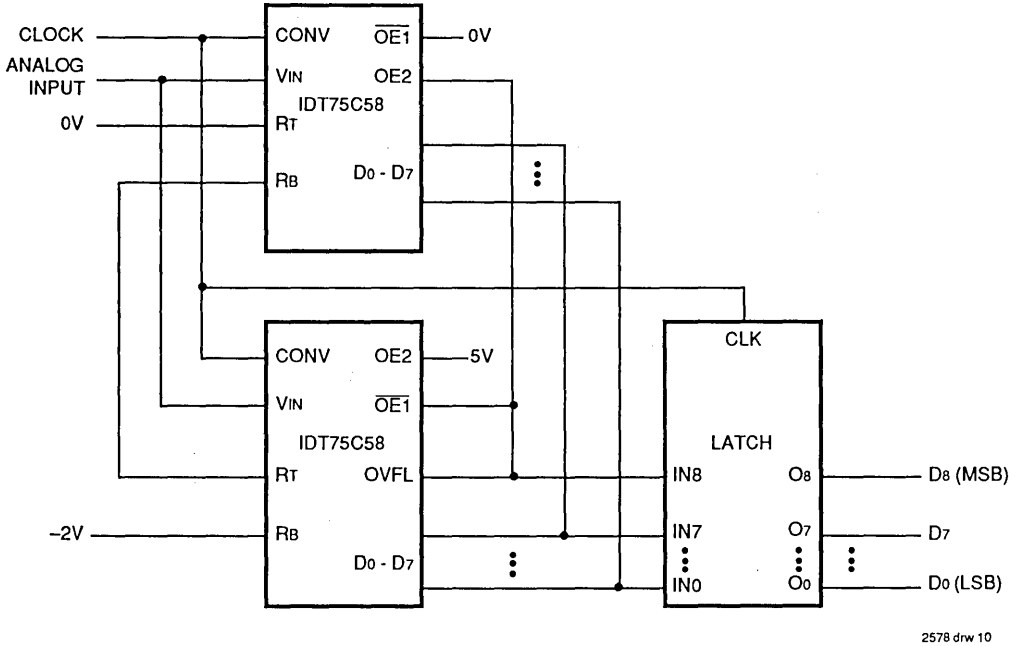
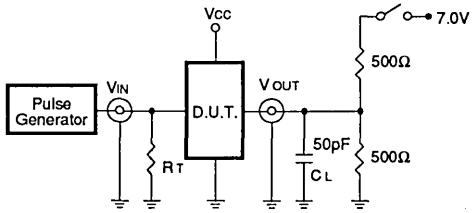


Figure 7. Simplified 9-Bit Application

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



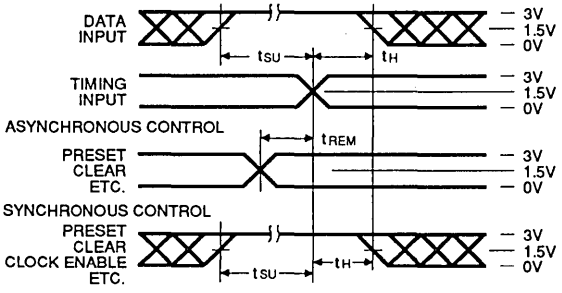
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

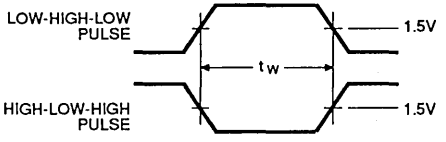
DEFINITIONS: 2578 tbl 6

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

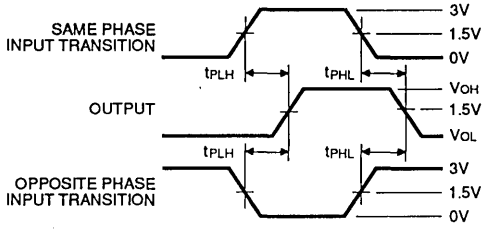
SET-UP, HOLD AND RELEASE TIMES



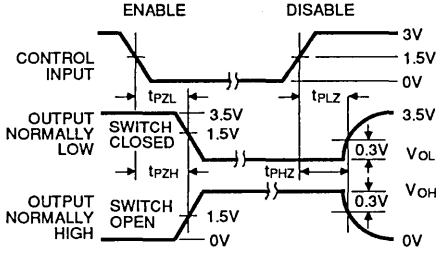
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

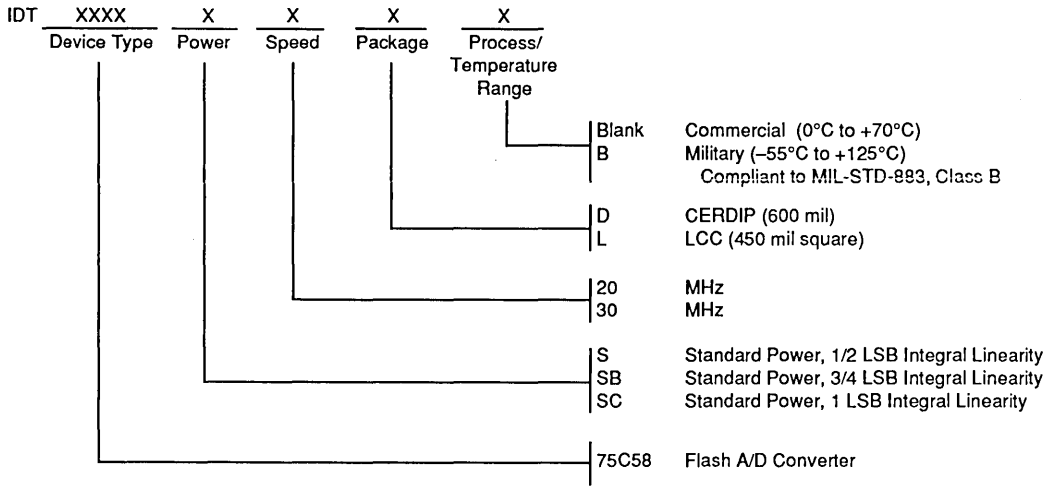


NOTES 2578 drw 12

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tF ≤ 2.5ns; tR ≤ 2.5ns.

5

ORDERING INFORMATION



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GENERAL INFORMATION

TECHNOLOGY AND CAPABILITIES

QUALITY AND RELIABILITY

PACKAGE DIAGRAM OUTLINES

COMPLEX LOGIC PRODUCTS

STANDARD LOGIC PRODUCTS

6

APPLICATION AND TECHNICAL NOTES

STANDARD LOGIC PRODUCTS

The demand for high-performance systems continues to push the need for faster and faster clock frequencies that exceed the capabilities of ASICs and older generation logic families such as FAST™ and FACT™. The use of high-speed MSI logic building blocks in the "speed-critical" processor/memory interface has allowed designers to produce the highest performance 25/33MHz microprocessor-based systems. The use of MSI logic with the fastest speed and lowest switching noise characteristics, as realized by the FCT-CT devices, has become all pervasive in today's high-performance systems.

The Standard Logic Product Line represents families of Memory and Bus Interface Devices that take advantage of two different IDT technology platforms.

The FCT and FCT-T (Fast CEMOS™ TTL-compatible) logic families have taken advantage of the pioneering IDT has done in CMOS technologies. Today's technology utilizes state-of-the-art sub-micron and double-layer metal processing.

The FBT (Fast BiCEMOS™ TTL-compatible) logic family is manufactured using an advanced dual metal BiCMOS technology that combines the most advanced sub-micron CMOS technology with high-performance bipolar processing.

THE FCT & FCT-T LOGIC FAMILY

This logic family was designed to allow easy upgrade of older bipolar 54/74F and Am29000 series designs to their performance equivalents in CMOS. The FCT family comes in two versions. There is the standard switching noise version (FCT) and a low switching noise version called FCT-T. Each version has various speed grades. Key features of these families are:

- FCT/FCT-T is a direct replacement of the FAST family of products.
- FCT/FCT-T is a direct replacement of the Am29000 family of products.
- FCT-A series is up to 25% faster than FCT speeds with standard switching noise.
- FCT-AT series is equivalent to FCT-A speeds with low switching noise.
- FCT-C series is up to 50% faster than FCT, with standard switching noise.
- FCT-CT series is equivalent to FCT-C speeds with low switching noise.
- High output drive to 64mA (commercial) and 48mA (military).
- Substantially lower input current levels (5μA maximum).
- Consistent with JEDEC Standard No. 18.
- Excellent ESD and latch-up immunity.

THE FBT LOGIC FAMILY

This logic family is manufactured using an advanced BiCEMOS, dual metal technology. This technology provides the highest device speeds while minimizing simultaneous switching noise and maintaining CMOS power levels. The FBT family comes in various speed grades. Key features of this family are:

- FBT series is equivalent to BCT speeds with ultra-low switching noise.
- FBT-A series is up to 30% faster than BCT speeds, with low switching noise.
- FBT-C series is up to 45% faster than BCT speeds with low switching noise.
- Output drive to 64mA (commercial) and 48mA (military) (non-resistor parts).
- CMOS power levels (5μW typical static).
- TTL-compatible input and output levels.
- High-impedance in power-off state.
- Some devices have 25Ω series resistor outputs.
- JEDEC standard pinout for DIP, SOIC and LCC packages.

A series of memory driver functions ave been designed using the BiCEMOS process. These functions include a 25Ω series resistor on the output driver, acting as a series termination. This results in a greater ability to drive transmission lines with high-capacitance loads such as large banks of memory.

All IDT logic devices are manufactured and assembled on a MIL-STD-883, Class B compliant line. Key features of the military products include:

- Fully compliant to MIL-STD-883, Class B.
- Offer numerous devices to DESC drawings.
- Available in Radiation Tolerant and Radiation Enhanced versions.
- Packages include hermetic DIP, LCC and CERPACK.

Commercial products are manufactured using the same production line and stringent quality requirements acquired from building military products. All commercial products are available in dual in-line as well as surface mount packages.

6

PRODUCT MATRIX

NOISE			
Standard		FCT-A	
Improved			FCT
Low	FCT-CT	FCT-AT	FCT-T
Ultra-Low	FBT-C	FBT	
SPEED	Very High-Speed	High-Speed	FAST

TABLE OF CONTENTS

Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTERED TRANSCEIVERS

IDT29FCT52AT/BT/CT
IDT29FCT53AT/BT/CT

FEATURES:

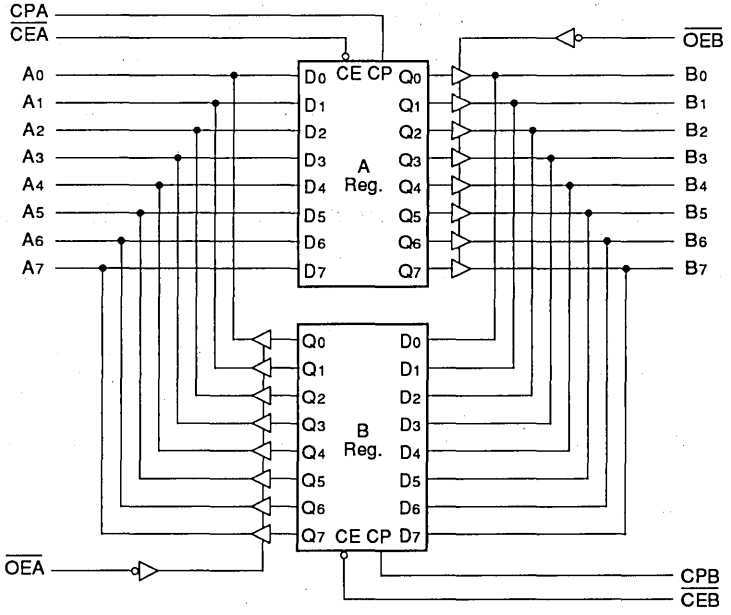
- Equivalent to AMD's Am2952/53 and Fairchild's 29F52/53 in pinout/function
- IDT29FCT52AT/53AT equivalent to FAST™ speed
- **IDT29FCT52BT/53BT 25% faster than FAST™**
- **IDT29FCT52CT/53CT 37% faster than FAST™**
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (2.5mW typ. static)
- TTL input and output level compatible
- I_{OFF} feature ideal for hot switching of backplane drivers
- Available in 24-pin DIP, SOIC, 28-pin LCC and PLCC with JEDEC standard pinout
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT52AT/BT/CT and IDT29FCT53AT/BT/CT are 8-bit registered transceivers manufactured using advanced CEMOS™, a dual metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

The IDT29FCT52AT/BT/CT is a non-inverting option of the IDT29FCT53AT/BT/CT.

FUNCTIONAL BLOCK DIAGRAM

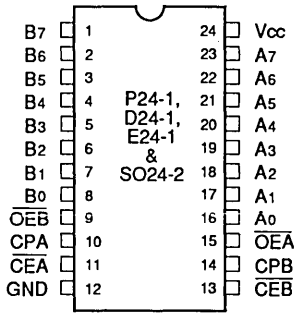


2629 drw 01

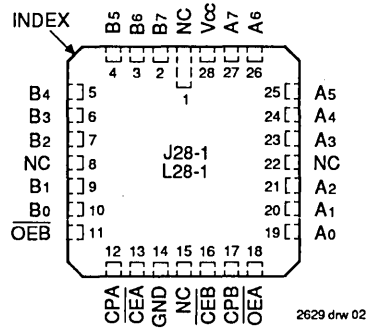
NOTE:
1. IDT29FCT52 function is shown.

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
A0-7	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B0-7	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents, regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the B0-7 lines. When $\overline{OEB}$ is HIGH, the B0-7 outputs are in the high impedance state.
CPB	I	Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents, regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the A0-7 lines. When $\overline{OEA}$ is HIGH, the A0-7 outputs are in the high impedance state.

2629 tbl 05

REGISTER FUNCTION TABLE[1]
(Applies to A or B Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

2629 tbl 06

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition

OUTPUT CONTROL[1]

	Internal	Y-Outputs		
$\overline{OE}$	Q	52	53	Function
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

2629 tbl 07

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2529 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2640 tbl 02

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max., V_I = 2.7V	Except I/O Pins	—	—	5	µA
			I/O Pins	—	—	15	
I_{IL}	Input LOW Current	Vcc = Max., V_I = 0.5V	Except I/O Pins	—	—	-5	µA
			I/O Pins	—	—	-15	
I_I	Input HIGH Current	Vcc = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		-60	-120	-225	mA
I_{OFF}	Power Down Disable	Vcc = GND, V_O = 4.5V		—	—	100	µA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL. I_{OH} = -8mA COM'L.	2.4	3.3	—	V
			I_{OH} = -12mA MIL. I_{OH}= -15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.(4) I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	Vcc = Max. V_{IN} = GND or Vcc		—	0.5	1.5	mA

NOTES: 2629 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously.Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ or $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	2.0	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.5	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.3	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.5	16.8[5]	

NOTES:

2629 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at DH
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT29FCT52AT/53AT				IDT29FCT52BT/53BT				IDT29FCT52CT/53CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CPA, CPB to An, Bn	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	2.0	6.3	—	7.3	ns
tPZH tPZL	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	1.5	7.0	—	8.0	ns
tPHZ tPLZ	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	1.5	6.5	—	7.5	ns
tSU	Set-up Time HIGH or LOW An, Bn to CPA, CPB		2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Hold Time HIGH or LOW An, Bn to CPA, CPB		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	Pulse Width HIGH[3] or LOW CPA or CPB		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns

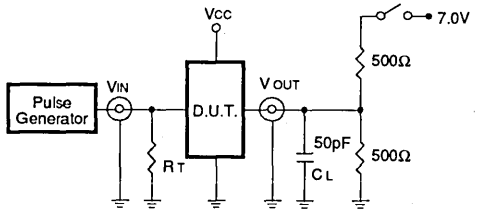
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2629 tbl 08

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

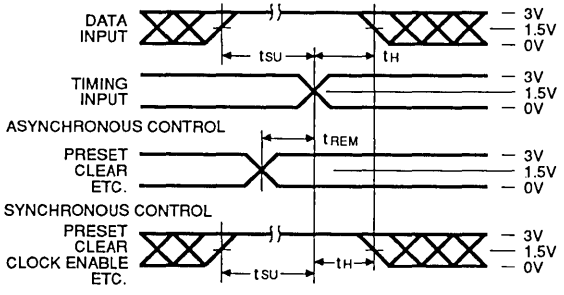
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2629 tbl 08

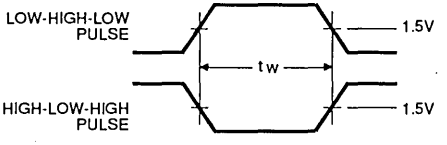
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

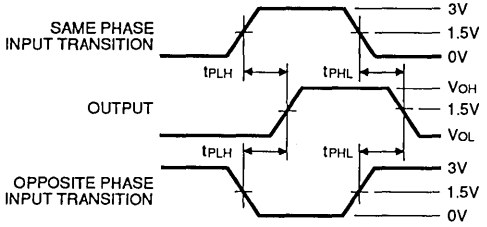
SET-UP, HOLD AND RELEASE TIMES



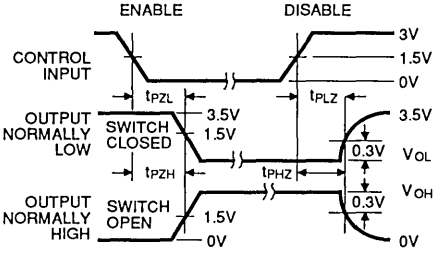
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

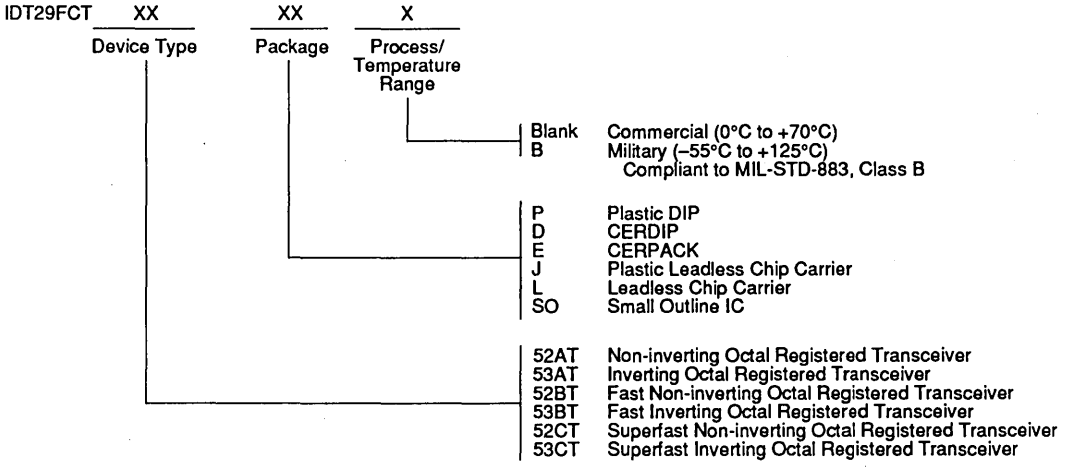


2629 drw 04

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2629 drw 03

6

Integrated Device Technology, Inc.

MULTILEVEL PIPELINE REGISTERS

IDT29FCT520AT/BT/CT
IDT29FCT521AT/BT/CT

FEATURES:

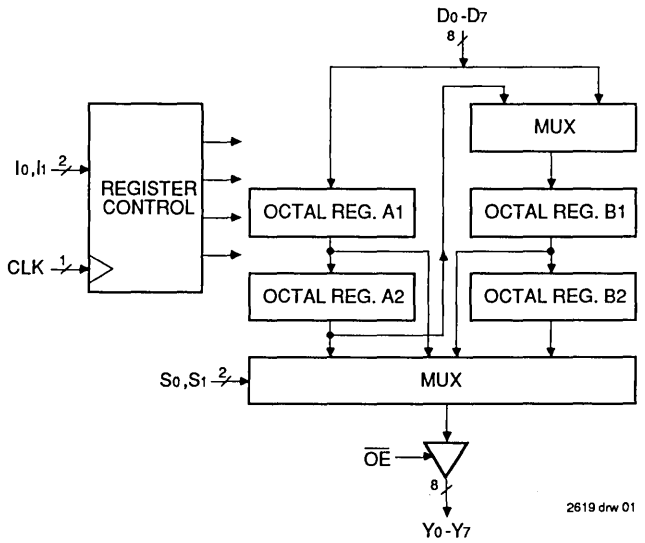
- Equivalent to AMD's Am29520/521 bipolar Multilevel Pipeline Registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- Four 8-bit high-speed registers
- Dual two-level or single four-level push-only stack operation
- All registers available at multiplexed output
- Hold, transfer and load instructions
- Provides temporary address or data storage
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than AMD's bipolar (5µA typ.)
- True TTL input and output levels
- Manufactured using advanced CEMOS™ processing
- Available in 300 mil plastic and hermetic DIP, as well as LCC, SOIC and CERPACK
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT520AT/BT/CT and IDT29FCT521AT/ BT/CT each contain four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

These devices differ only in the way data is loaded into and between the registers in 2-level operation. The difference is illustrated in Figure 1. In the IDT29FCT520AT/BT/CT when data is entered into the first level (I = 2 or I = 1), the existing data in the first level is moved to the second level. In the IDT29FCT521AT/BT/CT, these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0). This transfer also causes the first level to change. In either part I=3 is for hold.

FUNCTIONAL BLOCK DIAGRAM



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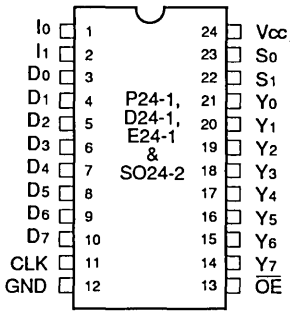
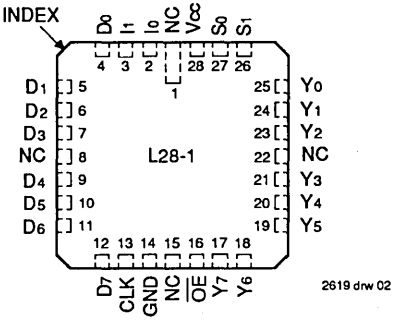
PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

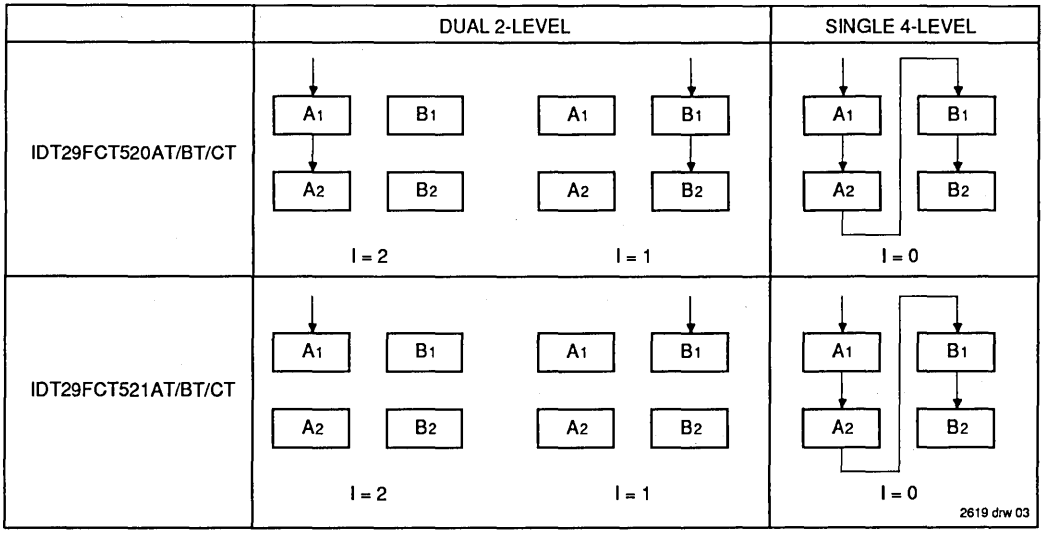
Pin Names	Description
D_n	Register input Port.
CLK	Clock input. Enter data into registers on LOW-to-HIGH transitions.
I_0, I_1	Instruction inputs. See Figure 1 and instruction Control Tables.
S_0, S_1	Multiplexer select. Inputs either register A_1, A_2, B_1 or B_2 data to be available at the output port.
$\overline{OE}$	Output enable for 3-state output port.
Y_n	Register output port.

2619 tbl 01

REGISTER SELECTION

S_1	S_0	Register
0	0	B_2
0	1	B_1
1	0	A_2
1	1	A_1

2619 tbl 02



NOTE:
1. I = 3 for hold.

Figure 1. Data Loading in 2-Level Operation

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2619 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2619 tbl 04

1. This parameter is measured at characterization data but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	Vcc = Max.	V_I = 0.5V	—	—	-5	µA
I_{OZH}	High Impedance Output Current	Vcc = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	-10	
I_I	Input HIGH Current	Vcc = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.[3], V_O = GND		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL. I_{OH} = -8mA COM'L.	2.4	3.3	—	V
			I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.0	3.0	—	
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	Vcc = Max. V_{IN} = GND or Vcc		—	0.2	1.5	mA

NOTES: 2619 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current, TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	7.0	12.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

2619 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL HIgh Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT520AT/521AT				FCT520BT/521BT				FCT520CT/521CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PHL} t_{PLH}	Propagation Delay CLK to Y_n	C_L = 50pF R_L = 500Ω	2.0	14.0	2.0	16.0	2.0	7.5	2.0	8.0	2.0	6.0	2.0	7.0	ns
t_{PHL} t_{PLH}	Propagation Delay S_0 or S_1 to Y_n		2.0	13.0	2.0	15.0	2.0	7.5	2.0	8.0	2.0	6.0	2.0	7.0	ns
t_{SU}	Set-up Time HIGH or LOW D_n to CLK		5.0	—	6.0	—	2.5	—	2.8	—	2.5	—	2.8	—	ns
t_H	Hold Time HIGH or LOW D_n to CLK		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{SU}	Set-up Time HIGH or LOW I_0 or I_1 to CLK		5.0	—	6.0	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
t_H	Hold Time HIGH or LOW I_0 or I_1 to CLK		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	12.0	1.5	13.0	1.5	7.0	1.5	7.5	1.5	6.0	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	15.0	1.5	16.0	1.5	7.5	1.5	8.0	1.5	6.0	1.5	7.0	ns
t_W	Clock Pulse Width HIGH or LOW		7.0	—	8.0	—	5.5	—	6.0	—	5.5	—	6.0	—	ns

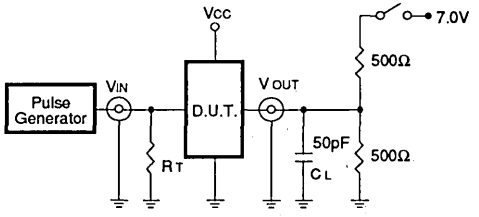
NOTES:

2619 tbl 07

1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



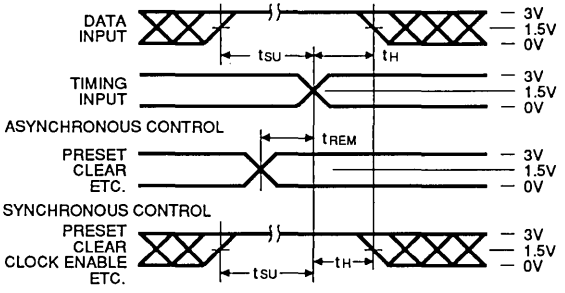
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

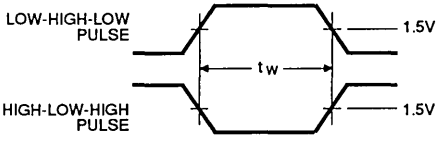
DEFINITIONS: 2619 tbl 08

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

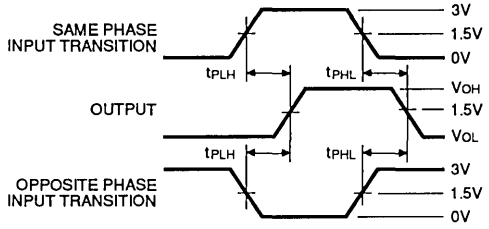
SET-UP, HOLD AND RELEASE TIMES



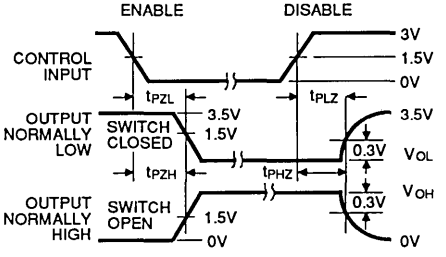
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES 2619 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tF ≤ 2.5ns; tR ≤ 2.5ns.

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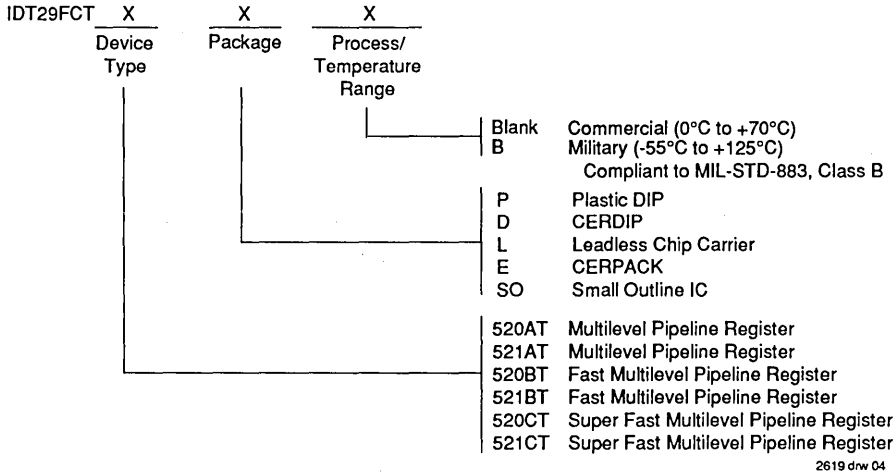
ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS 1-OF-8 DECODER

IDT54/74FCT138T
IDT54/74FCT138AT
IDT54/74FCT138CT

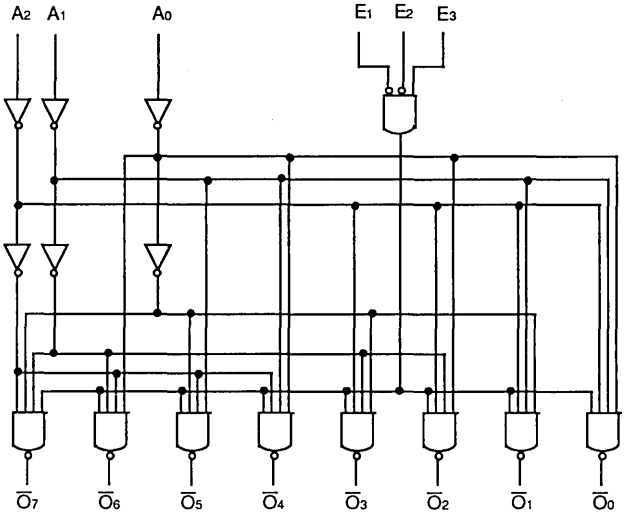
FEATURES:

- IDT54/74FCT138T equivalent to FAST™ speed
- **IDT54/74FCT138AT 35% faster than FAST™**
- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- True TTL input and output levels
- Substantially lower input current levels than FAST™ (5μA max.)
- 1-of-8 decoder with enables
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

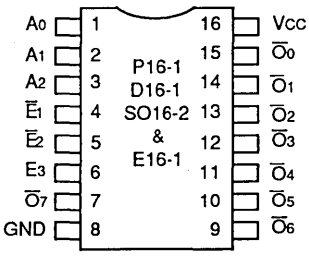
The IDT54/74FCT138T/AT/CT are 1-of-8 decoders built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT138T/AT/CT accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The IDT54/74FCT138T/AT/CT features three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74FCT138T/AT/CT devices and one inverter.

FUNCTIONAL BLOCK DIAGRAM



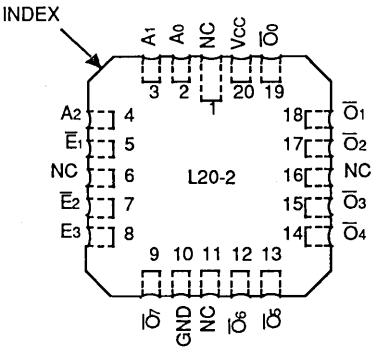
2570 cnv* 03

PIN CONFIGURATIONS



2570 drw 01

DIP/SOIC/CERPACK
TOP VIEW



2570 drw 02

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0$–$\overline{O}_7$	Outputs (Active LOW)

2570 tbl 06

FUNCTION TABLE

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

2570 tbl 07

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2570 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2570 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:

2570 tbl 03

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open Toggle $\overline{E}_1$, $\overline{E}_2$ or E_3	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.5	mA
		50% Duty Cycle f_O = 10MHz One Output Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	

NOTES:

2570 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_O N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

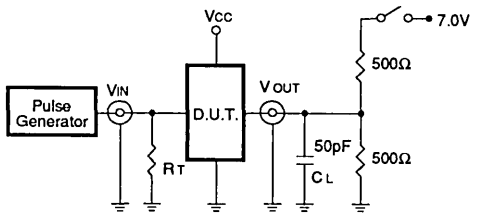
Symbol	Parameter	Condition[1]	IDT54/74FCT138T				IDT54/74FCT138AT				IDT54/74FCT138CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	12.0	1.5	5.8	1.5	7.8	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	—	—	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2570 tbl 08

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



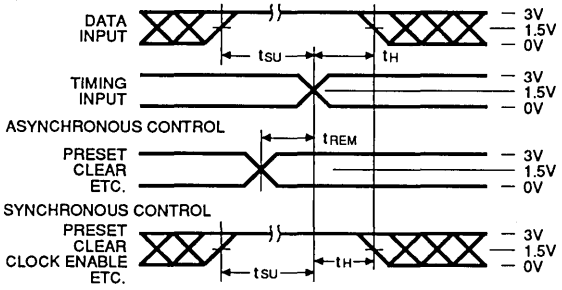
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

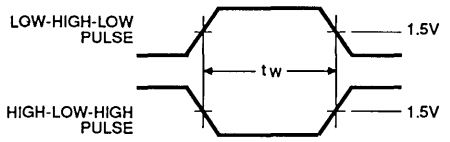
DEFINITIONS: 2570 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

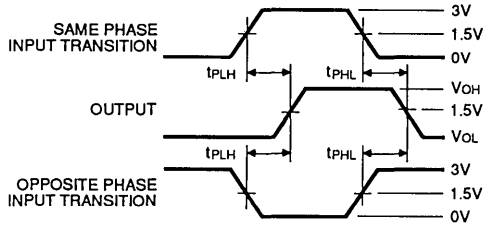
SET-UP, HOLD AND RELEASE TIMES



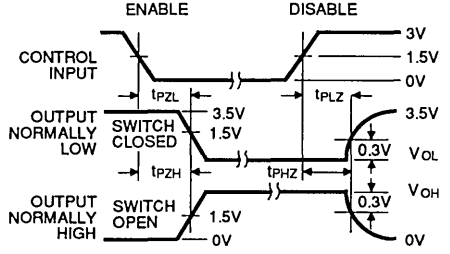
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

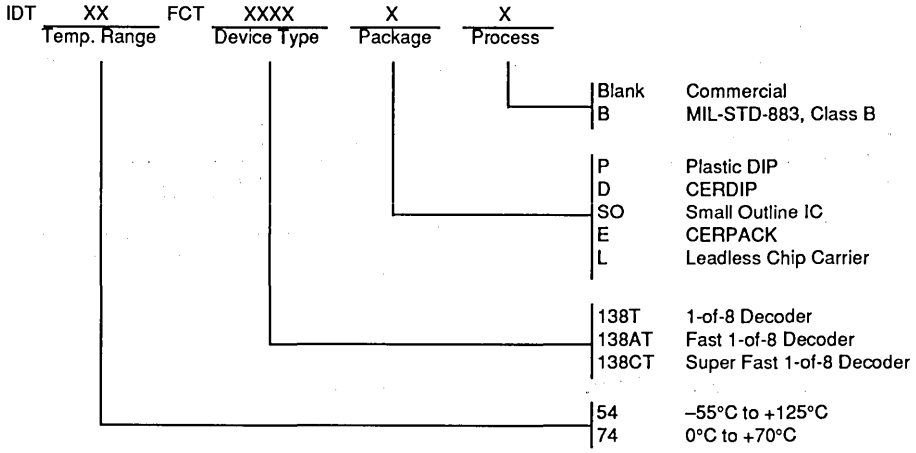


NOTES 2570 drw 10

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_O \leq 50\Omega$; $t_F \leq 2.5$ns; $t_R \leq 2.5$ns.

6

ORDERING INFORMATION



2570 cnv* 09

Integrated Device Technology, Inc.

FAST CMOS DUAL 1-OF-4 DECODER

IDT54/74FCT139T
IDT54/74FCT139AT
IDT54/74FCT139CT

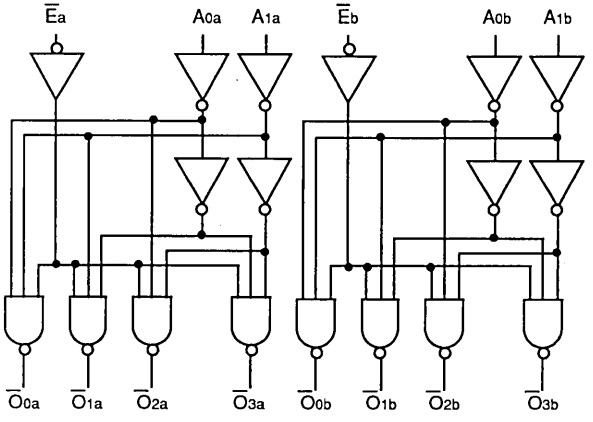
FEATURES

- IDT54/74FCT139T equivalent to FAST™ speed
- **IDT54/74FCT139AT 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST™ (5µA max.)
- Dual 1-of-4 decoder with enable
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

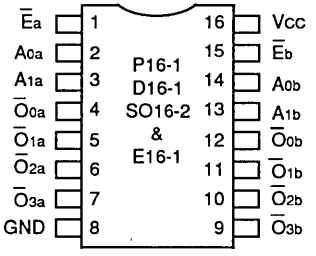
The IDT54/74FCT139T/AT/CT are dual 1-of-4 decoders built using advanced CEMOS™, a dual metal CMOS technology. These devices have two independent decoders, each of which accept two binary weighted inputs (A_0-A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

FUNCTIONAL BLOCK DIAGRAM



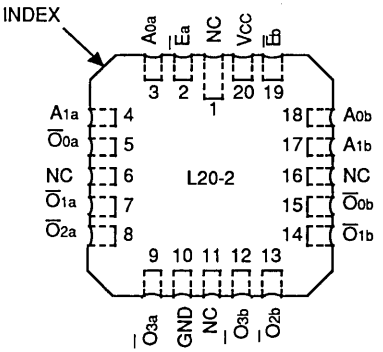
2566 cnv* 03

PIN CONFIGURATIONS



2566 cnv* 01

DIP/SOIC/CERPACK
TOP VIEW



2566 cnv* 02

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
A_0, A_1	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
$\overline{O_0}$ - $\overline{O_3}$	Outputs (Active LOW)

2566 tbl 07

TRUTH TABLE[1]

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

NOTES:

2566 tbl 06

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

2566 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

2566 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	−5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		−60	−120	−225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL. I_{OH} = −8mA COM'L.	2.4	3.3	—	V
			I_{OH} = −12mA MIL. I_{OH} = −15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2566 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_O = 10MHz 50% Duty Cycle One Output Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	
		V_{CC} = Max. Outputs Open f_O = 10MHz 50% Duty Cycle One Output Toggling on Each Decoder	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	7.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	3.7	9.5[5]	

NOTES:
2566 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_O N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

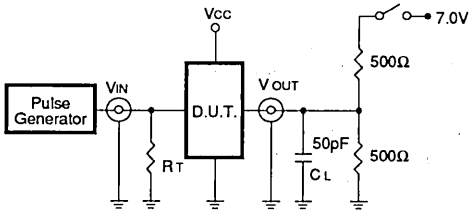
			IDT54/74FCT139T				IDT54/74FCT139AT				IDT54/74FCT139CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Parameter	Description	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{On}$	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	12.0	1.5	5.9	1.5	7.8	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{On}$		1.5	8.0	1.5	9.0	1.5	5.5	1.5	7.2	—	—	—	—	ns

NOTES:
2566 tbl 08

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



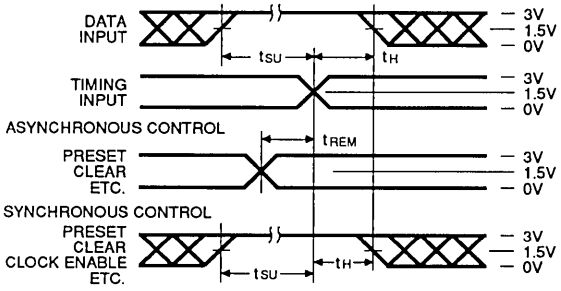
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

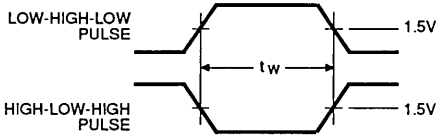
DEFINITIONS: 2566 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

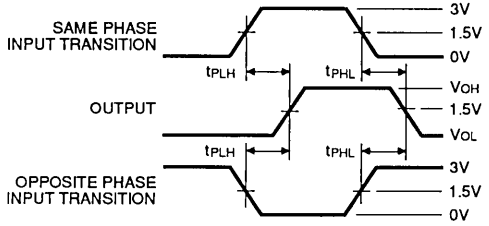
SET-UP, HOLD AND RELEASE TIMES



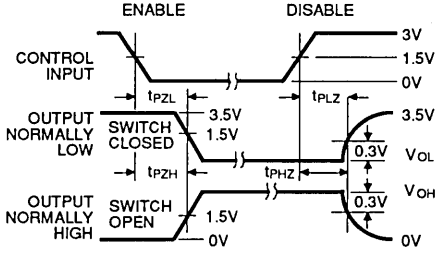
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

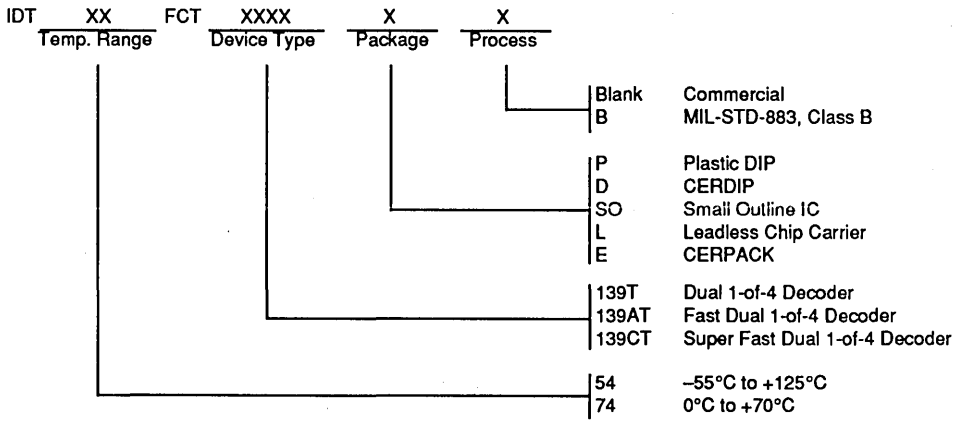


NOTES 2566 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2566 cnv* 09

Integrated Device Technology, Inc.

FAST CMOS 8-INPUT MULTIPLEXER

IDT54/74FCT151T/AT/CT
IDT54/74FCT251T/AT/CT

FEATURES:

- IDT54/74FCT151T/251T equivalent to FAST™ speed and drive
- **IDT54/74FCT151AT/251AT 25% faster than FAST™**
- **IDT54/74FCT151CT/251CT 50% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- TTL input and output level compatible
  - — V_{OH} = 3.3V (typ.)
  - — V_{OL} = 0.3V (typ.)
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

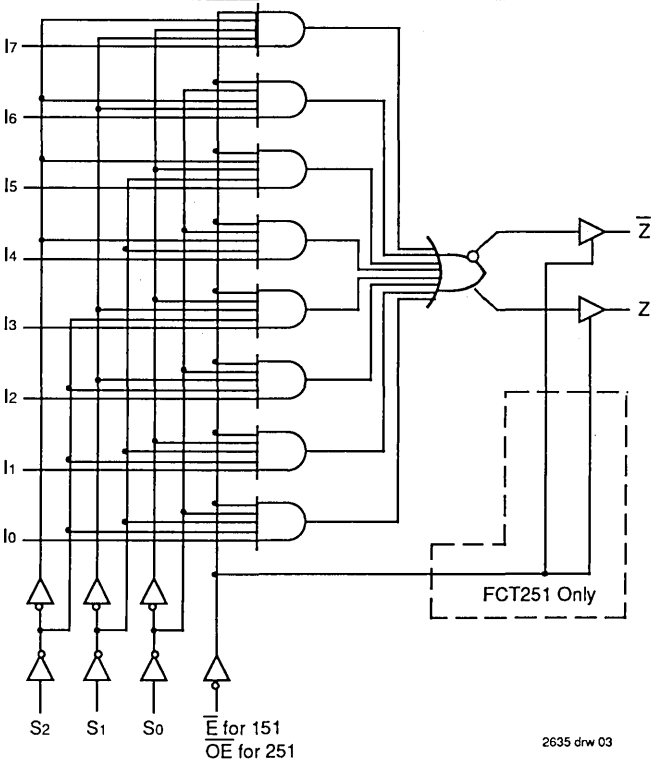
DESCRIPTION:

The IDT54/74FCT151T/AT/CT and IDT54/74FCT251T/AT/CT are high-speed 8-input multiplexers built using advanced CEMOS™, a dual metal CMOS technology. They select one bit of data from up to eight sources under the control of three select inputs. Both assertion and negation outputs are provided.

The IDT54/74FCT151T/AT/CT has a common active-LOW enable ($\overline{E}$) input. When $\overline{E}$ is LOW, data from one of eight inputs is routed to the complementary outputs according to the 3-bit code applied to the Select (S_0-S_2) inputs. A common application of the 'FCT151 is data routing from one of eight sources.

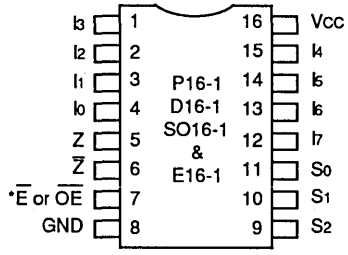
The IDT54/74FCT251T/AT/CT has a common active-LOW Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, data from one of eight inputs is routed to the complementary outputs. When $\overline{OE}$ is HIGH, both outputs are in the high impedance state. This feature allows multiplexer expansion by tying several outputs together.

FUNCTIONAL BLOCK DIAGRAM



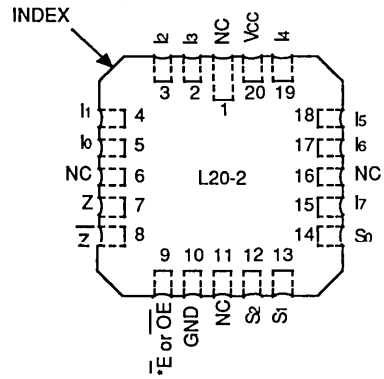
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor, Inc.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

2635 drw 01



LCC
TOP VIEW

2635 drw 02

*$\overline{E}$ for 151 only. $\overline{OE}$ for 251 only.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

2635 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2635 tbl 04

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
I0 - I7	Data Inputs
S0 - S2	Selects Inputs
$\overline{E}$	Enable Input (Active LOW)-FCT151
$\overline{OE}$	Output Enable Input (Active LOW)-FCT251
Z	Data Output
$\overline{Z}$	Inverted Data Output

2635 tbl 01

FUNCTION TABLE(2)

Inputs				Outputs	
S2	S1	S0	$\overline{E}/\overline{OE}$(1)	Z	$\overline{Z}$
X	X	X	H	L(151)	H(151)
X	X	X	H	Z(251)	Z(251)
L	L	L	L	I0	$\overline{I0}$
L	L	H	L	I1	$\overline{I1}$
L	H	L	L	I2	$\overline{I2}$
L	H	H	L	I3	$\overline{I3}$
H	L	L	L	I4	$\overline{I4}$
H	L	H	L	I5	$\overline{I5}$
H	H	L	L	I6	$\overline{I6}$
H	H	H	L	I7	$\overline{I7}$

2635 tbl 02

NOTES:
1. $\overline{E}$ for 151, $\overline{OE}$ for 251.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't care, Z = High Impedance.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:
2635 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	QuiescentPower Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	3.5	7.5	

NOTES:
2635 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_O = Number of Outputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FCT151T/AT/CT

Symbol	Parameter	Condition[1]	IDT54/74FCT151T				IDT54/74FCT151AT				IDT54/74FCT151CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay SN to $\overline{Z}$	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.6	1.5	7.4	1.5	5.6	1.5	6.2	ns
tPLH tPHL	Propagation Delay SN to Z		1.5	10.5	1.5	11.5	1.5	6.8	1.5	7.6	1.5	5.8	1.5	6.5	ns
tPLH tPHL	Propagation Delay $\overline{E}$ to $\overline{Z}$		1.5	7.0	1.5	7.5	1.5	5.6	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPLH tPHL	Propagation Delay $\overline{E}$ to Z		1.5	9.5	1.5	11.0	1.5	5.8	1.5	6.6	1.5	5.0	1.5	5.7	ns
tPLH tPHL	Propagation Delay IN to $\overline{Z}$		1.5	6.5	1.5	7.5	1.5	5.2	1.5	5.8	1.5	4.4	1.5	4.9	ns
tPLH tPHL	Propagation Delay IN to Z		1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.1	1.5	4.7	1.5	5.2	ns

2635 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FCT251T/AT/CT

Symbol	Parameter	Condition[1]	IDT54/74FCT251T				IDT54/74FCT251AT				IDT54/74FCT251CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay SN to $\overline{Z}$	CL = 50pF RL = 500Ω	1.5	9.0	1.5	9.5	1.5	6.6	1.5	7.4	1.5	5.6	1.5	6.2	ns
tPLH tPHL	Propagation Delay SN to Z		1.5	11.0	1.5	14.0	1.5	6.8	1.5	7.6	1.5	5.8	1.5	6.5	ns
tPLH tPHL	Propagation Delay IN to $\overline{Z}$		1.5	7.0	1.5	8.0	1.5	5.2	1.5	5.8	1.5	4.4	1.5	4.9	ns
tPLH tPHL	Propagation Delay IN to Z		1.5	7.0	1.5	8.0	1.5	5.5	1.5	6.1	1.5	4.7	1.5	5.2	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to $\overline{Z}$		1.5	9.0	1.5	10.0	1.5	6.7	1.5	7.4	1.5	5.7	1.5	6.3	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to $\overline{Z}$		1.5	7.5	1.5	8.5	1.5	6.0	1.5	6.4	1.5	5.0	1.5	5.4	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to Z		1.5	9.0	1.5	10.0	1.5	6.7	1.5	7.6	1.5	5.7	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Z		1.5	7.0	1.5	7.0	1.5	6.0	1.5	6.3	1.5	5.0	1.5	5.2	ns

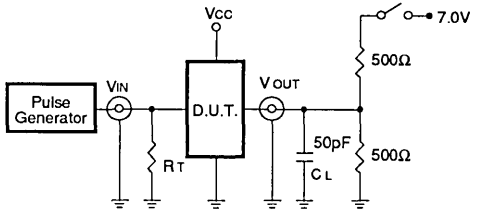
NOTES:

2635 tbl 08

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



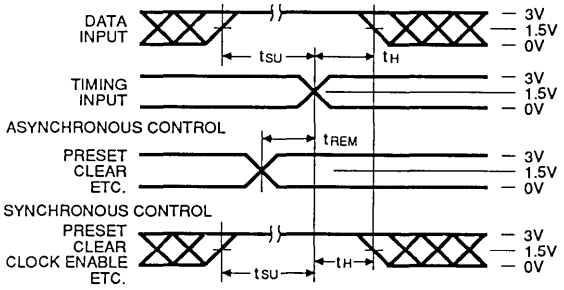
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

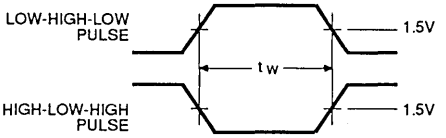
DEFINITIONS: 2635 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

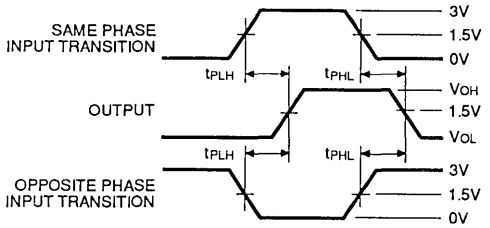
SET-UP, HOLD AND RELEASE TIMES



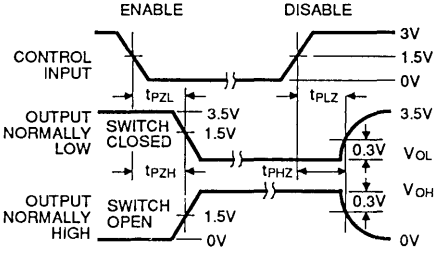
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

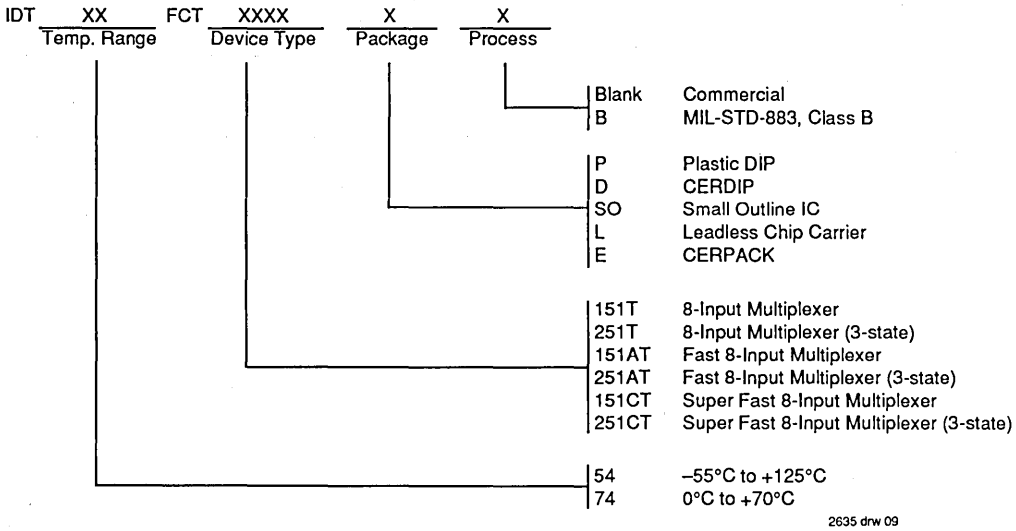


NOTES 2635 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS QUAD 2-INPUT MULTIPLEXER

IDT54/74FCT157T/AT/CT
IDT54/74FCT257T/AT/CT

FEATURES:

- IDT54/74FCT157T/257T equivalent to FAST™ speed and drive
- **IDT54/74FCT157AT/257AT 25% faster than FAST™**
- **IDT54/74FCT157CT/257CT 50% faster than FAST™**
- TTL input and output level compatible
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Product available in Radiation Tolerant and Radiation Enhanced Versions
- Military product compliant to MIL-STD-883, Class B and DESC listed

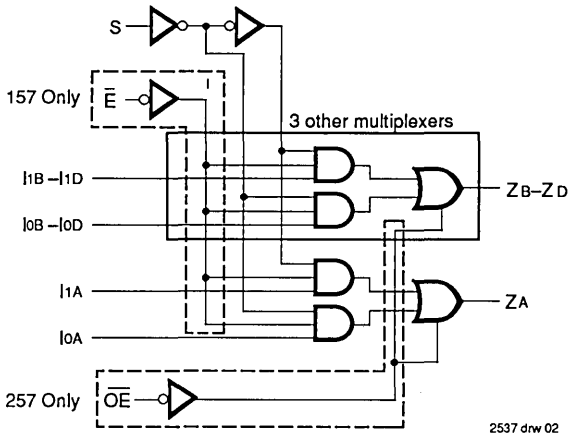
DESCRIPTION:

The IDT54/74FCT157T/AT/CT and IDT54/74FCT257T/AT/CT are high-speed quad 2-input multiplexers built using advanced CEMOS™, a dual metal CMOS technology. Four bits of data from two sources can be selected using the common select input. The four buffered outputs present the selected data in the true (non-inverting) form.

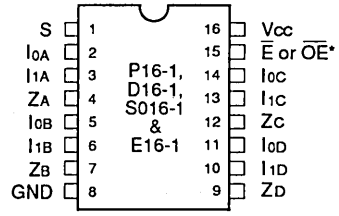
The IDT54/74FCT157T/AT/CT has a common, active-LOW, enable input. When the enable input is not active, all four outputs are held LOW. A common application of 'FCT157T is to move data from two different groups of registers to a common bus. Another application is as a function generator. The 'FCT157T can generate any four of the 16 different functions of two variables with one variable common.

The IDT54/74FCT257T/AT/CT has a common Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, all outputs are switched to a high-impedance state allowing the outputs to interface directly with bus-oriented systems.

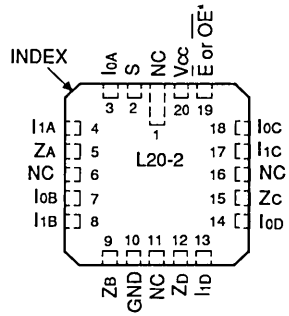
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

2537 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a registered trademark of National Semiconductor Co.

* $\overline{E}$ for FCT157, $\overline{OE}$ for FCT257.

PIN DESCRIPTION

Pin Names	Description
I_{0A}–I_{0D}	Source 0 Data Inputs
I_{1A}–I_{1D}	Source 1 Data Inputs
$\overline{E}$	Enable Input (Active LOW)–FCT157T
$\overline{OE}$	Output Enable (Active LOW)–FCT257T
S	Select Input
Z_A–Z_D	Outputs

2537 tbl 05

FUNCTION TABLE[1]

Inputs				Output Z_N	
$\overline{E}/\overline{OE}$	S	I_0	I_1	157	257
H	X	X	X	L	Z
L	H	X	L	L	L
L	H	X	H	H	H
L	L	L	X	L	L
L	L	H	X	H	H

NOTES:
2537 tbl 06

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:
2537 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
2537 tbl 02

1. This parameter is guaranteed but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2537 tbl 03

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{IN} = Vcc Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND Four Bits Toggling	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	2.7	8.0[5]	

2537 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - FCT157T/AT/CT

Symbol	Parameter	Condition[1]	54/74FCT157T				54/74FCT157AT				54/74FCT157CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay In to Zn	CL = 50 pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	5.0	1.5	5.8	1.5	4.3	1.5	5.0	ns
tPLH tPHL	Propagation Delay $\overline{E}$ to Zn		1.5	10.5	1.5	12.0	1.5	6.0	1.5	7.4	1.5	4.8	1.5	5.9	ns
tPLH tPHL	Propagation Delay S to Zn		1.5	10.5	1.5	12.0	1.5	7.0	1.5	8.1	1.5	5.2	1.5	6.0	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - FCT257T/AT/CT

Symbol	Parameter	Condition[1]	54/74FCT257T				54/74FCT257AT				54/74FCT257CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay In to Zn	CL = 50 pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	5.0	1.5	5.8	1.5	4.3	1.5	5.0	ns
tPLH tPHL	Propagation Delay S to Zn		1.5	10.5	1.5	12.0	1.5	7.0	1.5	8.1	1.5	5.2	1.5	6.0	ns
tPZH tPZL	Output Enable Time		1.5	8.5	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.0	1.5	6.8	ns
tPHZ tPLZ	Output Disable Time		1.5	6.0	1.5	8.0	1.5	5.5	1.5	5.8	1.5	5.0	1.5	5.3	ns

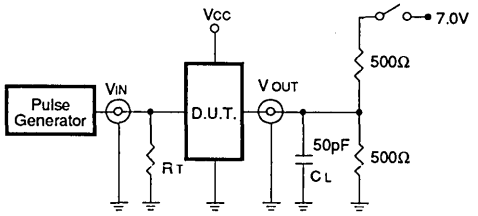
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2537 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



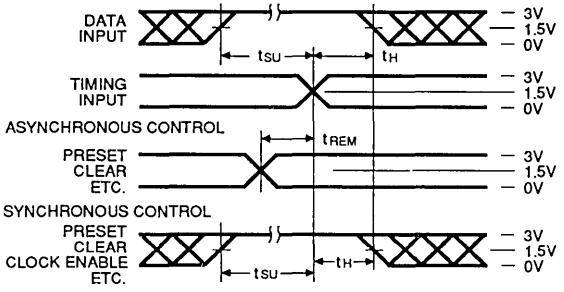
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

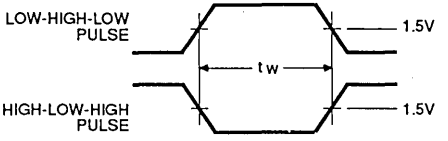
DEFINITIONS: 2537 tbl 03

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

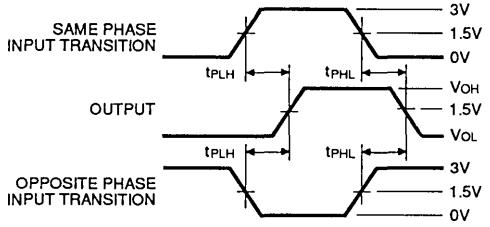
SET-UP, HOLD AND RELEASE TIMES



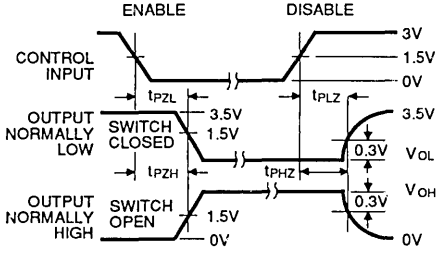
PULSE WIDTH



PROPAGATION DELAY



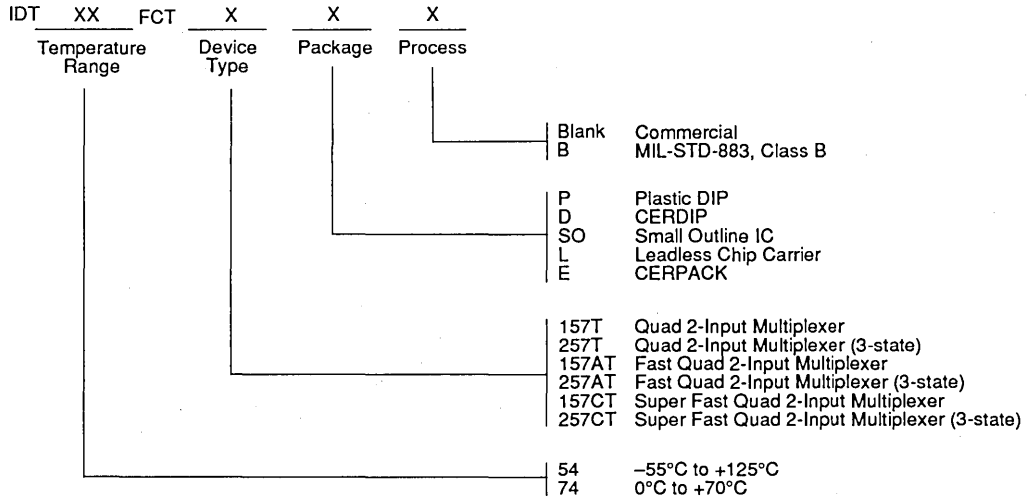
ENABLE AND DISABLE TIMES



NOTES 2537 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2537 drw 03

6

Integrated Device Technology, Inc.

FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54/74FCT161T
IDT54/74FCT161AT
IDT54/74FCT163T
IDT54/74FCT163AT

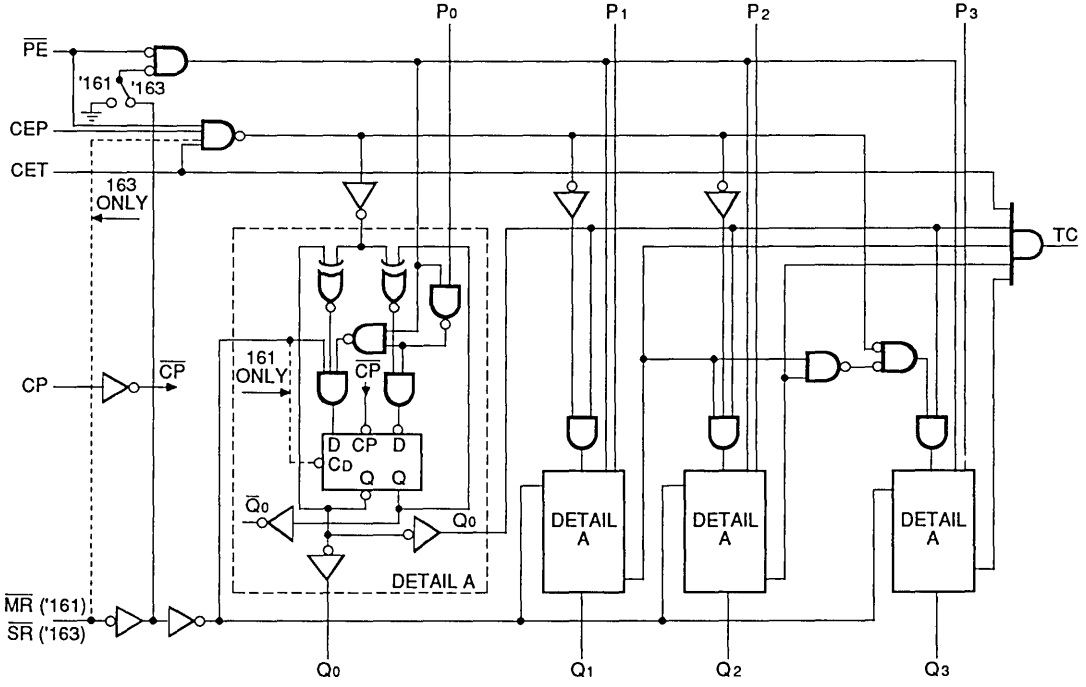
FEATURES:

- IDT54/74FCT161T/163T equivalent to FAST™ speed
- **IDT54/74FCT161AT/163AT 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- True TTL input and output levels
- Substantially lower input current levels than FAST™ (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT161T/163T and IDT54/74FCT161AT/163AT are high-speed synchronous modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-stage counters. The IDT54/74FCT161T and IDT54/74FCT161AT have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54/74FCT163T and IDT54/74FCT163AT have Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

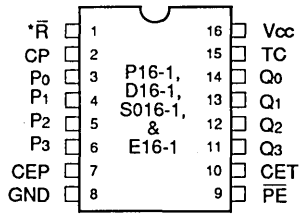
FUNCTIONAL BLOCK DIAGRAM



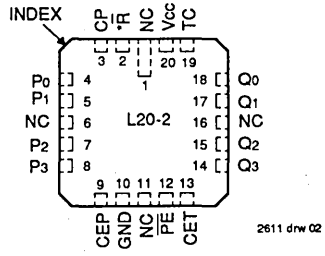
2611 drw 01

CEMOS is a trademark of Integrated Device Techology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

*$\overline{MR}$ for '161
*$\overline{SR}$ for '163

PIN DESCRIPTION

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)
P0-3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q0-3	Flip-Flop Outputs
TC	Terminal Count Output

FUNCTION TABLE[2]

$\overline{SR}$[1]	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge(s)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (Pn→Qn)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES: 2611 tbl 06
1. For FCT163/163A only.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care.

2611 tbl 05

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
VTERM[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES: 2611 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE: 2611 tbl 02
1. This parameter is guaranteed at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	-5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL. I_{OH} = -8mA COM'L.	2.4	3.3	—	V
			I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL}= 32mA MIL. I_{OL}= 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2611 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open Load Mode $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	12.8[5]	

2611 tbl 04

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

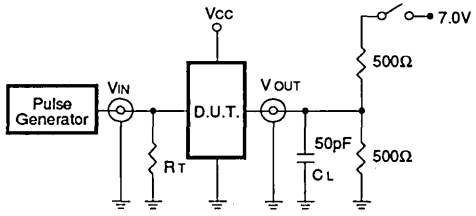
Symbol	Parameter	Condition[1]	IDT54/74FCT161T/163T				IDT54/74FCT161AT/163AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Qn ($\overline{PE}$ Input HIGH)	CL = 50pF RL = 500Ω	2.0	11.0	2.0	11.5	2.0	7.2	2.0	7.5	ns
tPLH tPHL	Propagation Delay CP to Qn ($\overline{PE}$ Input LOW)		2.0	9.5	2.0	10.0	2.0	6.2	2.0	6.5	ns
tPLH tPHL	Propagation Delay CP to TC		2.0	15.0	2.0	16.5	2.0	9.8	2.0	10.8	ns
tPLH tPHL	Propagation Delay CET to TC		1.5	8.5	1.5	9.0	1.5	5.5	1.5	5.9	ns
tPHL	Propagation Delay $\overline{MR}$ to Qn ('161)		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.1	ns
tPHL	Propagation Delay $\overline{MR}$ to TC ('161)		2.0	11.5	2.0	12.5	2.0	7.5	2.0	8.2	ns
tSU	Set-up Time, HIGH or LOW Pn to CP		5.0	—	5.5	—	4.0	—	4.5	—	ns
tH	Hold Time, HIGH or LOW Pn to CP		1.5	—	2.0	—	1.5	—	2.0	—	ns
tSU	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		11.5	—	13.5	—	9.5	—	11.5	—	ns
tH	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time, HIGH or LOW CEP or CET to CP		11.5	—	13.0	—	9.5	—	11.0	—	ns
tH	Hold Time, HIGH or LOW CEP or CET to CP		0	—	0	—	0	—	0	—	ns
tW	Clock Pulse Width (Load) HIGH or LOW		5.0	—	5.0	—	4.0[3]	—	4.0[3]	—	ns
tW	Clock Pulse Width (Count) HIGH or LOW		7.0	—	8.0	—	6.0	—	7.0	—	ns
tW	$\overline{MR}$ Pulse Width, LOW ('161)		5.0	—	5.0	—	4.0[3]	—	4.0[3]	—	ns
tREM	Recovery Time $\overline{MR}$ to CP ('161)		6.0	—	6.0	—	5.0	—	5.0	—	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2611 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



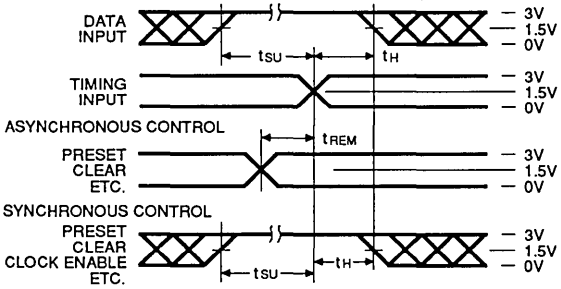
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

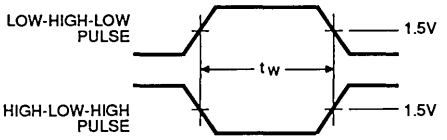
DEFINITIONS: 2611 tbl 08

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

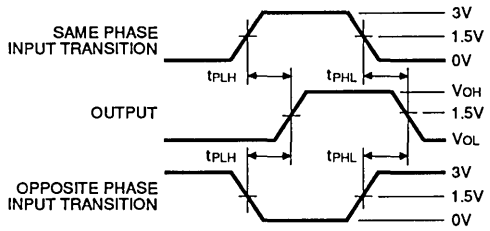
SET-UP, HOLD AND RELEASE TIMES



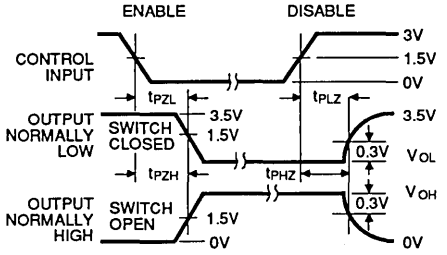
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

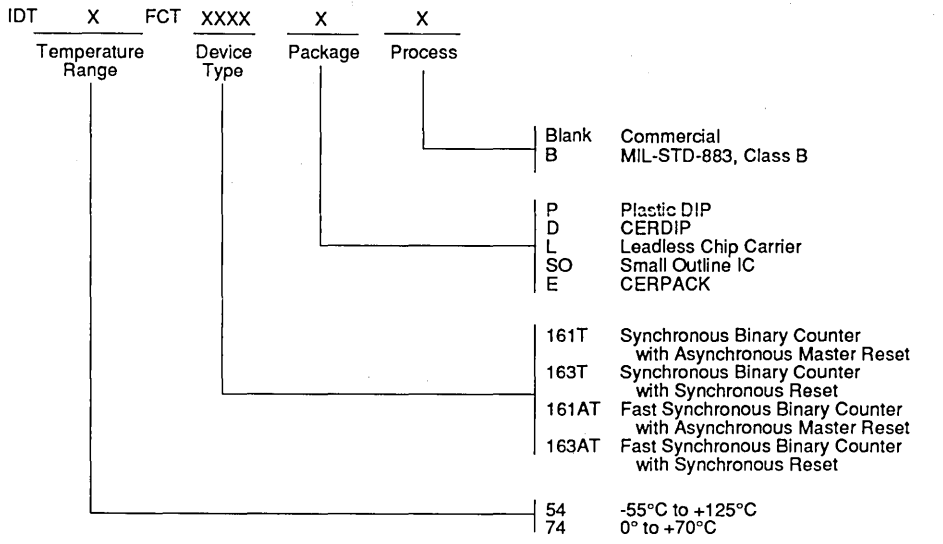


NOTES 2611 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tF ≤ 2.5ns; tR ≤ 2.5ns.

6

ORDERING INFORMATION



2611 drw 03

Integrated Device Technology, Inc.

FAST CMOS UP/DOWN BINARY COUNTER

IDT54/74FCT191T
IDT54/74FCT191AT

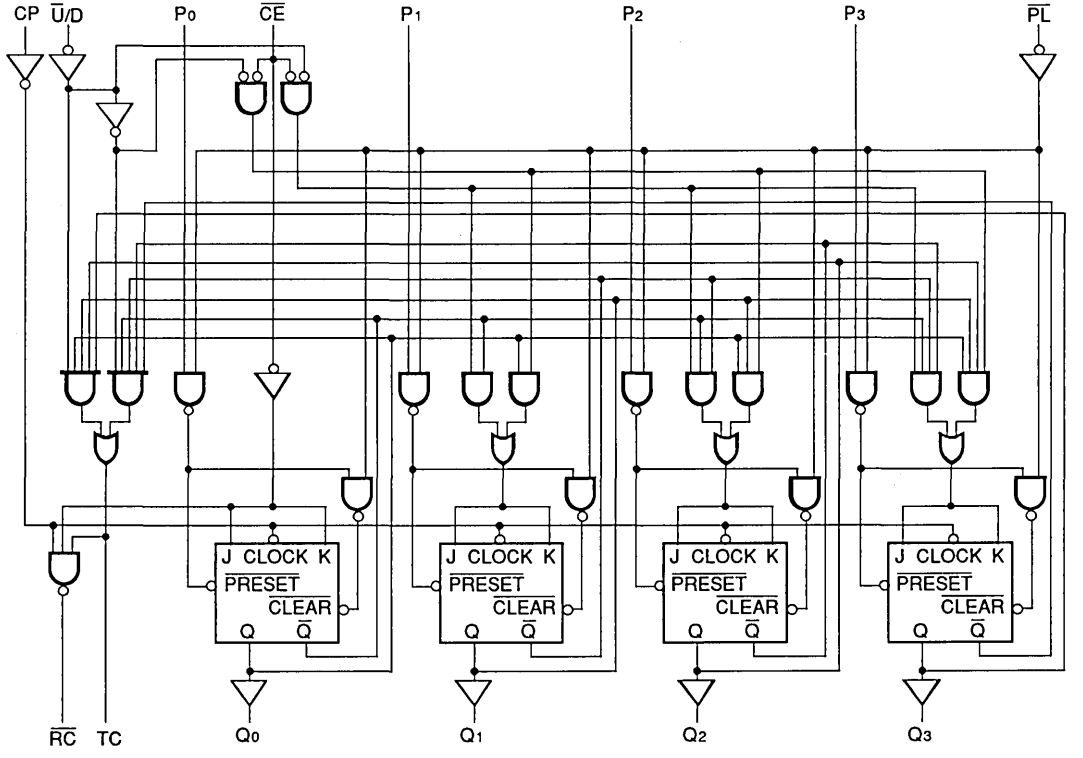
FEATURES:

- IDT54/74FCT191T equivalent to FAST™ speed
- **IDT54/74FCT191AT 35% faster than FAST**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- True TTL input and output levels
- Substantially lower input current levels than FAST (5μA max.)
- JEDEC standard pinout for DIP, LCC and SOIC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT191T and IDT54/74FCT191AT are reversible modulo-16 binary counters, featuring synchronous counting and asynchronous presetting and are built using advanced CEMOS™, a dual metal CMOS technology. The preset feature allows the IDT54/74FCT191T and IDT54/74FCT191AT to be used in programmable dividers. The count enable input, terminal count output and ripple clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

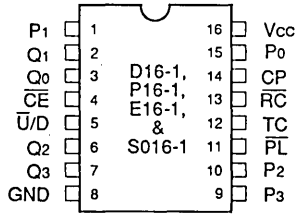
FUNCTIONAL BLOCK DIAGRAM



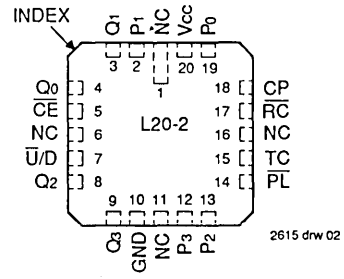
2615 drw 01

CEMOS is a trademark of Integrated Device Techology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P0-3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}$/D	Up/Down Count Control Input
Q0-3	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Count Output (Active HIGH)

2615 tbl 05

$\overline{RC}$ FUNCTION TABLE[2]

Inputs		Outputs	
$\overline{CE}$	CP	TC[1]	$\overline{RC}$
L	⊓	H	⊓
H	X	X	H
X	X	L	H

2615 tbl 06

MODE SELECT FUNCTION TABLE[2]

Inputs				
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	Mode
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asynchronous)
H	H	X	X	No Change (Hold)

2615 tbl 07

NOTES:
1. TC is generated internally.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2615 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2615 tbl 02

1. This parameter is guaranteed at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	-5	
I_I	Input HIGH Current	Vcc = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.[3], V_O = GND		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL. I_{OH} = -8mA COM'L.	2.4	3.3	—	V
			I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	Vcc = Max. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	Vcc = Max. V_{IN} = GND or Vcc		—	0.2	1.5	mA

NOTES: 2615 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.0	2.8	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.2	3.8	
		V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	4.2	10.5[5]	

2615 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at VCC or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT191T				IDT54/74FCT191AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	2.5	12.0	1.5	16.0	2.5	7.8	1.5	10.5	ns
tPLH tPHL	Propagation Delay CP to TC		3.0	14.0	2.0	16.0	3.0	11.8	2.0	12.2	ns
tPLH tPHL	Propagation Delay CP to $\overline{RC}$		2.5	8.5	1.5	12.5	2.5	8.5	1.5	10.0	ns
tPLH tPHL	Propagation Delay $\overline{CE}$ to $\overline{RC}$		2.0	8.0	2.0	8.5	2.0	7.2	2.0	8.0	ns
tPLH tPHL	Propagation Delay $\overline{U}$/D to $\overline{RC}$		4.0	20.0	4.0	22.5	4.0	13.0	4.0	14.7	ns
tPLH tPHL	Propagation Delay $\overline{U}$/D to TC		3.0	11.0	3.0	13.0	3.0	7.2	3.0	8.5	ns
tPLH tPHL	Propagation Delay P_n to Q_n		2.0	14.0	1.5	16.0	2.0	9.1	1.5	10.4	ns
tPLH tPHL	Propagation Delay $\overline{PL}$ to Q_n		3.0	13.0	3.0	14.0	3.0	8.5	3.0	9.1	ns
tSU	Set-up Time, HIGH or LOW P_n to $\overline{PL}$		5.0	—	6.0	—	4.0	—	5.0	—	ns
tH	Hold Time, HIGH or LOW P_n to $\overline{PL}$		1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time LOW $\overline{CE}$ to CP		10.0	—	10.5	—	9.0	—	9.5	—	ns
tH	Hold Time LOW $\overline{CE}$ to CP		0	—	0	—	0	—	0	—	ns
tSU	Set-up Time, HIGH or LOW $\overline{U}$/D to CP		12.0	—	12.0	—	10.0	—	10.0	—	ns
tH	Hold Time, HIGH or LOW $\overline{U}$/D to CP		0	—	0	—	0	—	0	—	ns
tW	$\overline{PL}$ Pulse Width LOW		6.0	—	8.5	—	5.5	—	8.0	—	ns
tW	Clock Pulse Width HIGH or LOW		5.0	—	7.0	—	4.0[3]	—	6.0	—	ns
tREM	Recovery Time $\overline{PL}$ to CP		6.0	—	7.5	—	5.0	—	6.5	—	ns

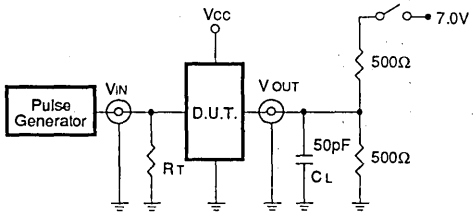
NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2615 tbl 08

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



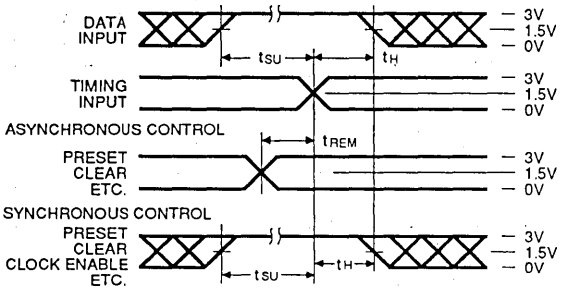
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

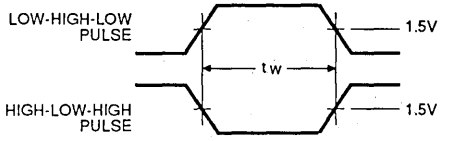
DEFINITIONS: 2615 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

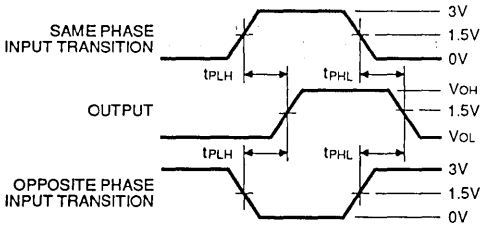
SET-UP, HOLD AND RELEASE TIMES



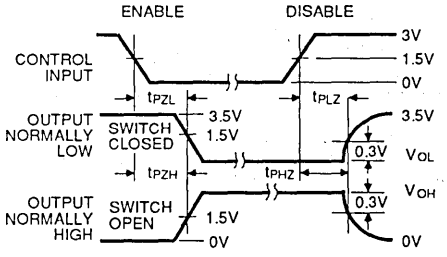
PULSE WIDTH



PROPAGATION DELAY



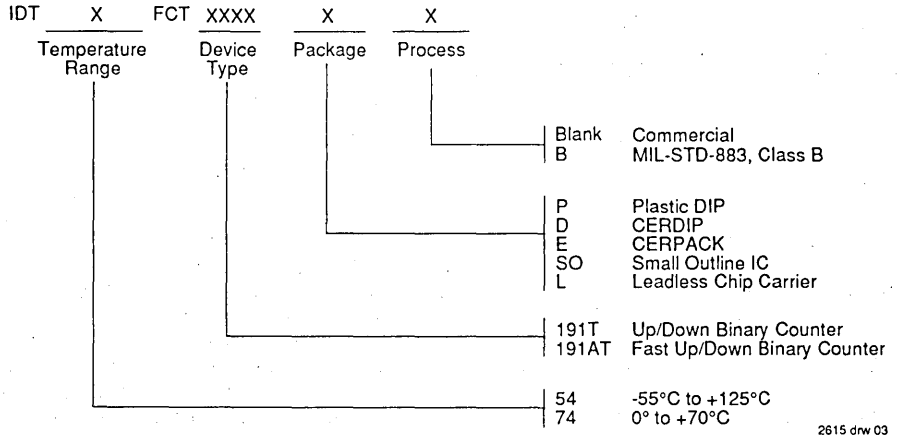
ENABLE AND DISABLE TIMES



NOTES 2615 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_O \leq 50\Omega$; $t_F \leq 2.5$ns; $t_R \leq 2.5$ns.

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

FAST CMOS UP/DOWN BINARY COUNTERS

IDT54/74FCT193T
IDT54/74FCT193AT

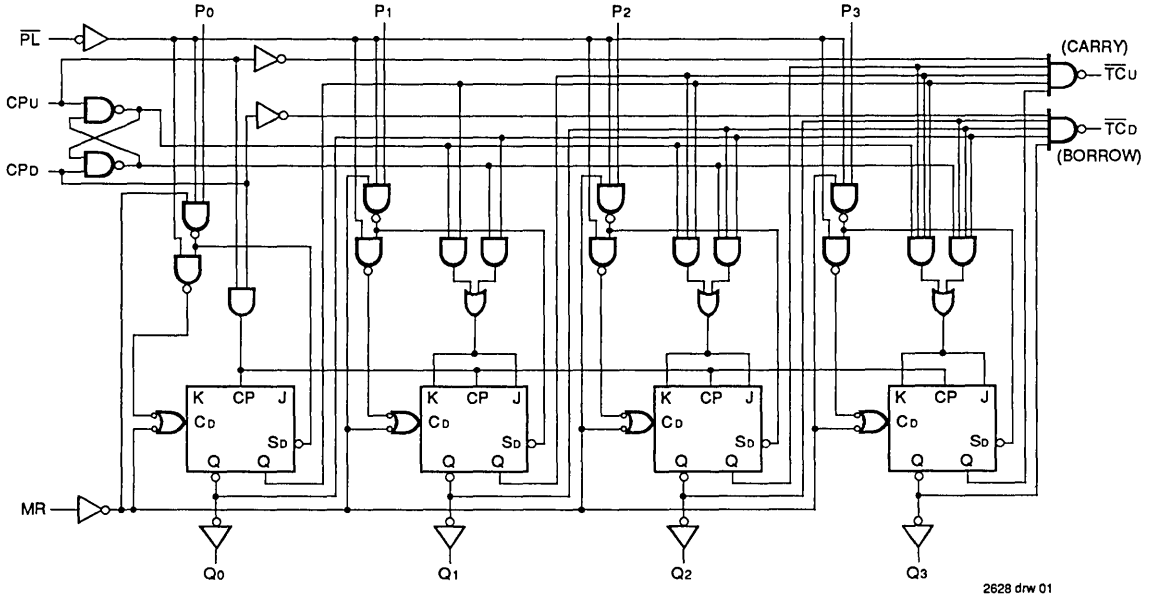
FEATURES:

- IDT54/74FCT193T equivalent to FAST™ speed
- **IDT54/74FCT193AT 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

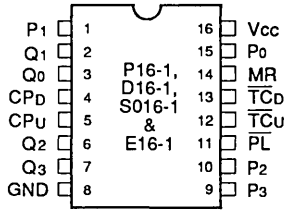
The IDT54/74FCT193T and IDT54/74FCT193AT are up/down modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. Separate count-up and count-down clocks are used and, in either counting mode, the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate terminal count-up and terminal count-down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

FUNCTIONAL BLOCK DIAGRAM

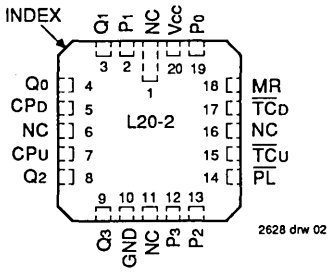


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
CPU	Count Up Clock Input (Active Rising Edge)
CPD	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
Pn	Parallel Data Inputs
Qn	Flip-flop Outputs
$\overline{TC_D}$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC_U}$	Terminal Count Up (Carry) Output (Active LOW)

2628 tbl 05

FUNCTION TABLE[1]

MR	$\overline{PL}$	CPU	CPD	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↑	Count Down

NOTES: 2628 tbl 06
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2628 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2628 tbl 02
1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	-5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL. I_{OH} = -8mA COM'L.	2.4	3.3	—	V
			I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2628 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND One Bit Toggling at f_i = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	4.2	10.5[5]	

2629 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

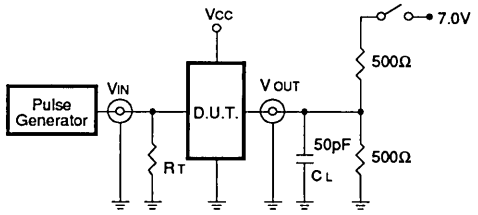
Symbol	Parameter	Condition[1]	IDT54/74FCT193T				IDT54/74FCT193AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CPU or CPD to $\overline{TC_U}$ or $\overline{TC_D}$	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	10.5	2.0	6.5	2.0	6.9	ns
tPLH tPHL	Propagation Delay CPU or CPD to Qn		2.0	13.5	2.0	14.0	2.0	8.8	2.0	9.1	ns
tPLH tPHL	Propagation Delay Pn to Qn		2.0	15.5	2.0	16.5	2.0	10.1	2.0	10.8	ns
tPLH tPHL	Propagation Delay $\overline{PL}$ to Qn		2.0	14.0	2.0	13.5	2.0	8.8	2.0	9.1	ns
tPHL	Propagation Delay MR to Qn		3.0	15.5	3.0	16.0	3.0	10.1	3.0	10.4	ns
tPLH	Propagation Delay MR to $\overline{TC_U}$		3.0	14.5	3.0	15.0	3.0	9.4	3.0	9.8	ns
tPHL	Propagation Delay MR to $\overline{TC_D}$		3.0	15.5	3.0	16.0	3.0	10.1	3.0	10.4	ns
tPLH tPHL	Propagation Delay $\overline{PL}$ to $\overline{TC_U}$ or $\overline{TC_D}$		3.0	16.5	3.0	18.5	3.0	10.8	3.0	12.0	ns
tPLH tPHL	Propagation Delay Pn to $\overline{TC_U}$ or $\overline{TC_D}$		3.0	15.5	3.0	16.5	3.0	10.1	3.0	10.8	ns
tSU	Set-up Time, HIGH or LOW Pn to $\overline{PL}$		5.0	—	6.0	—	4.0	—	5.0	—	ns
tH	Hold Time, HIGH or LOW Pn to $\overline{PL}$		2.0	—	2.0	—	1.5	—	1.5	—	ns
tW	$\overline{PL}$ Pulse Width LOW		6.0	—	7.5	—	5.0	—	6.5	—	ns
tW	CPU or CPD Pulse Width HIGH or LOW		5.0	—	7.0	—	4.0[3]	—	6.0	—	ns
tW	CPU or CPD Pulse Width LOW (Change of Direction)		10.0	—	12.0	—	8.0	—	10.0	—	ns
tW	MR Pulse Width HIGH		6.0	—	6.0	—	5.0	—	5.0	—	ns
tREM	Recovery Time $\overline{PL}$ to CPU or CPD		6.0	—	8.0	—	5.0	—	7.0	—	ns
tREM	Recovery Time MR to CPU or CPD		4.0	—	4.5	—	3.0	—	3.5	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2628 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



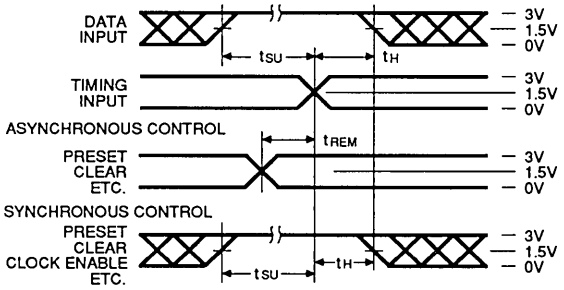
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

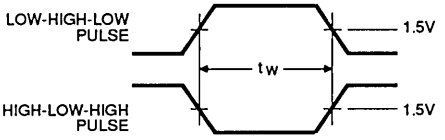
DEFINITIONS: 2628 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

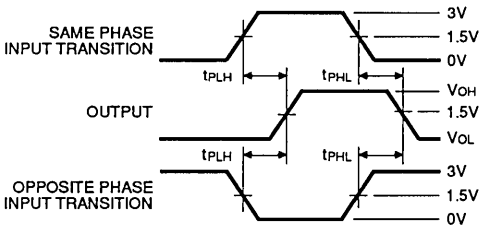
SET-UP, HOLD AND RELEASE TIMES



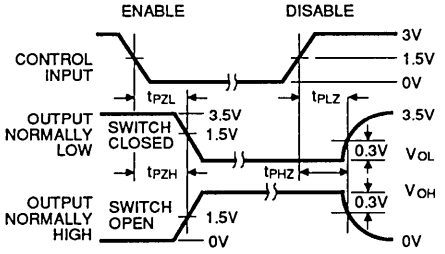
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

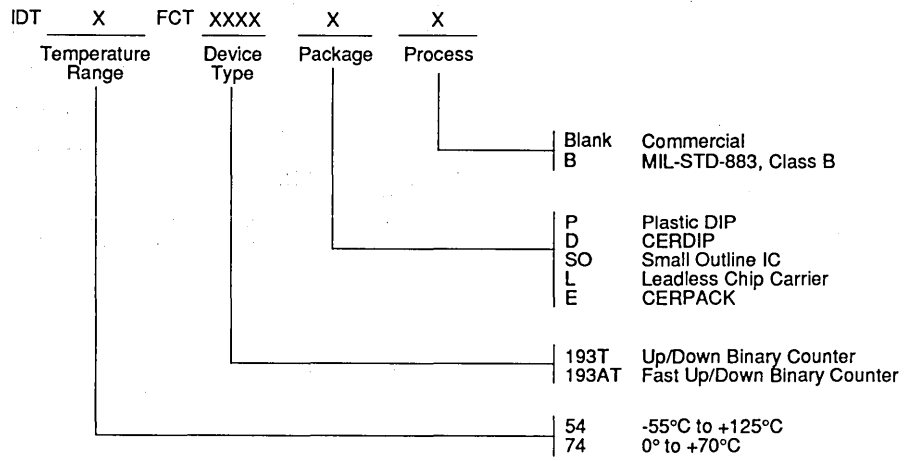


NOTES 2628 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2628 drw 03

Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT240T/AT/CT
IDT54/74FCT241T/AT/CT
IDT54/74FCT244T/AT/CT
IDT54/74FCT540T/AT/CT
IDT54/74FCT541T/AT/CT

FEATURES:

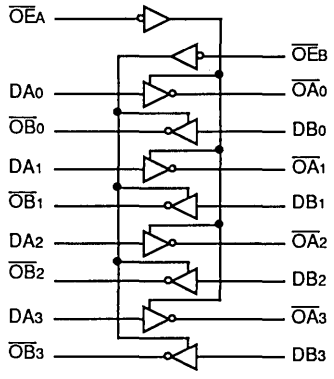
- IDT54/74FCT240T/241T/244T/540T/541T equivalent to FAST™ speed and drive
- **IDT54/74FCT240AT/241AT/244AT/540AT/541AT 25% faster than FAST™**
- **IDT54/74FCT240CT/241CT/244CT/540CT/541CT up to 55% faster than FAST™**
- True TTL input and output compatible
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications

DESCRIPTION:

The IDT octal buffer/line drivers are built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT240T/AT/CT, IDT54/74FCT241T/AT/CT and IDT54/74FCT244T/AT/CT are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitter/receivers which provide improved board density.

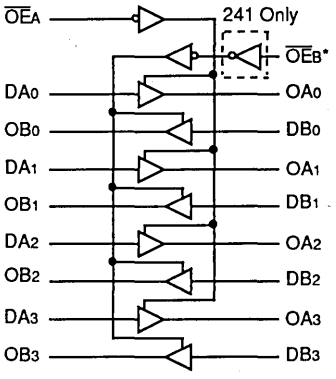
The IDT54/74FCT540T/AT/CT and IDT54/74FCT541T/AT/CT are similar in function to the IDT54/74FCT240T/AT/CT and IDT54/74FCT244T/AT/CT, respectively, except that the inputs and outputs are on opposite sides of the package. This pinout arrangement makes these devices especially useful as output ports for microprocessors and as backplane drivers, allowing ease of layout and greater board density.

FUNCTIONAL BLOCK DIAGRAMS



IDT54/74FCT240T

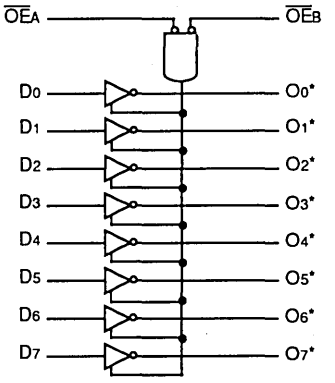
2565 cnv* 01



IDT54/74FCT241T/244T

*$\overline{OE}_B$ for 241T, $\overline{OE}_B$ for 244T

2565 cnv* 02



IDT54/74FCT540T/541T

*Logic diagram shown for 'FCT540T. 'FCT541T is the non-inverting option.

2565 cnv* 03

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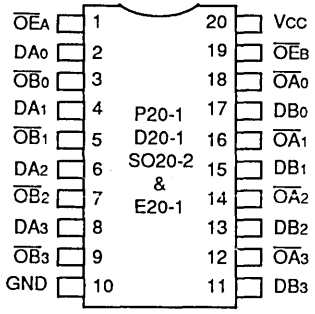
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

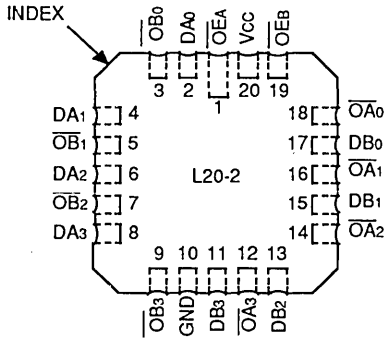
PIN CONFIGURATIONS

IDT54/74FCT240T



DIP/SOIC/CERPACK
TOP VIEW

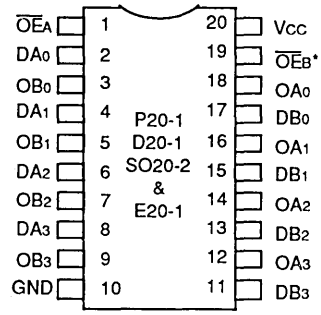
2565cnv* 04



LCC
TOP VIEW

2565cnv* 07

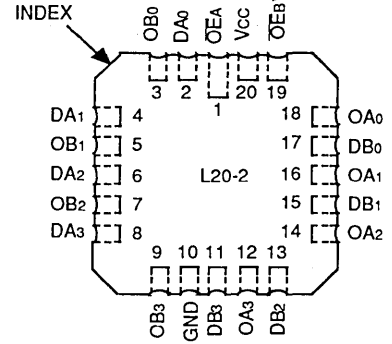
IDT54/74FCT241T/244T



DIP/SOIC/CERPACK
TOP VIEW

*OEB for 241T, OEB for 244T

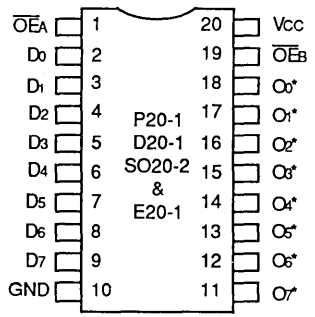
2565cnv* 05



LCC
TOP VIEW

2565cnv* 08

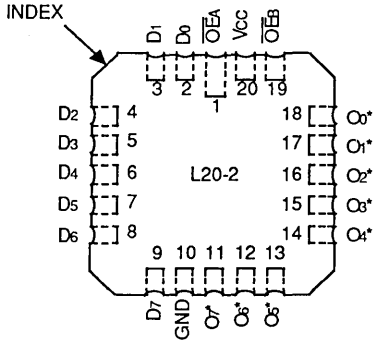
IDT54/74FCT540T/541T



DIP/SOIC/CERPACK
TOP VIEW

*OEB for 241T, OEB for 244T

2565cnv* 06



LCC
TOP VIEW

2565cnv* 09

PIN DESCRIPTION

Pin Names	Description
$\overline{OE_A}$, $\overline{OE_B}$	3–State Output Enable Inputs (Active LOW)
OE_B[1]	3–State Output Enable Input (Active HIGH)
Dxx	Inputs
Oxx	Outputs

NOTES: 2565 tbl 04
1. OE_B for 241 only

FUNCTION TABLE

Inputs[1]				Outputs[1]				
$\overline{OE_A}$	$\overline{OE_B}$	OE_B[2]	D	240	241	244	540	541
L	L	H	L	H	L	L	H	L
L	L	H	H	L	H	H	L	H
H	H	L	X	Z	Z	Z	Z	Z

NOTE: 2565 tbl 05
1. H = High Voltage Level
   X = Don't Care
   L = Low Voltage Level
   Z = High Impedance
2. OE_B for 241 only.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2565 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2565 tbl 02
1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ. (2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2565 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_A}$ = $\overline{OE_B}$ = GND or $\overline{OE_A}$ = GND, OE_B = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		$\overline{OE_A}$ = $\overline{OE_B}$ = GND or $\overline{OE_A}$ = GND, OE_B = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
		$\overline{OE_A}$ = $\overline{OE_B}$ = GND or $\overline{OE_A}$ = GND, OE_B = V_{CC} Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2565 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT240T

			54/74FCT240T				54/74FCT240AT				54/74FCT240CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.0	1.5	5.7	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	4.5	1.5	4.6	ns

2565 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT241T AND FCT244T

			54/74FCT241T/244T				54/74FCT241AT/244AT				54/74FCT241CT/244CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
tPZH tPZL	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

2565 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT540T AND FCT541T

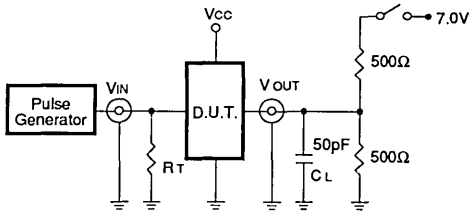
			54/74FCT540T/541T				54/74FCT540AT/541AT				54/74FCT540CT/541CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay DN to ON IDT54/74FCT540T	CL = 50pF RL = 500Ω	1.5	8.5	1.5	9.5	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
tPLH tPHL	Propagation Delay DN to ON IDT54/74FCT541T		1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

NOTES:
2565 tbl 09

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



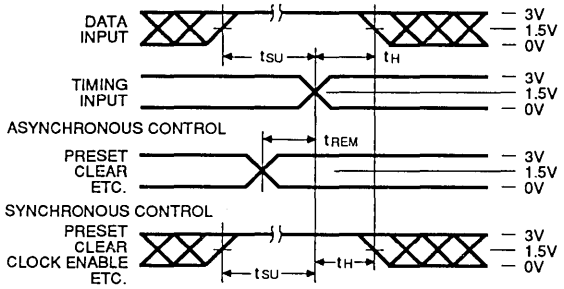
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

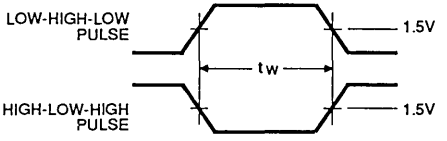
DEFINITIONS: 2565 tbl 10

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

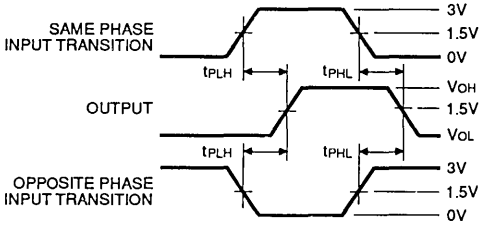
SET-UP, HOLD AND RELEASE TIMES



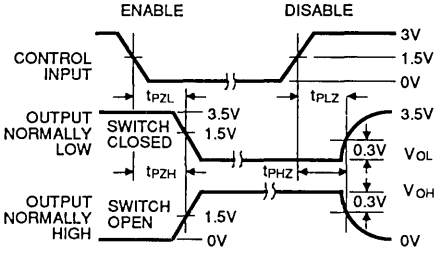
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

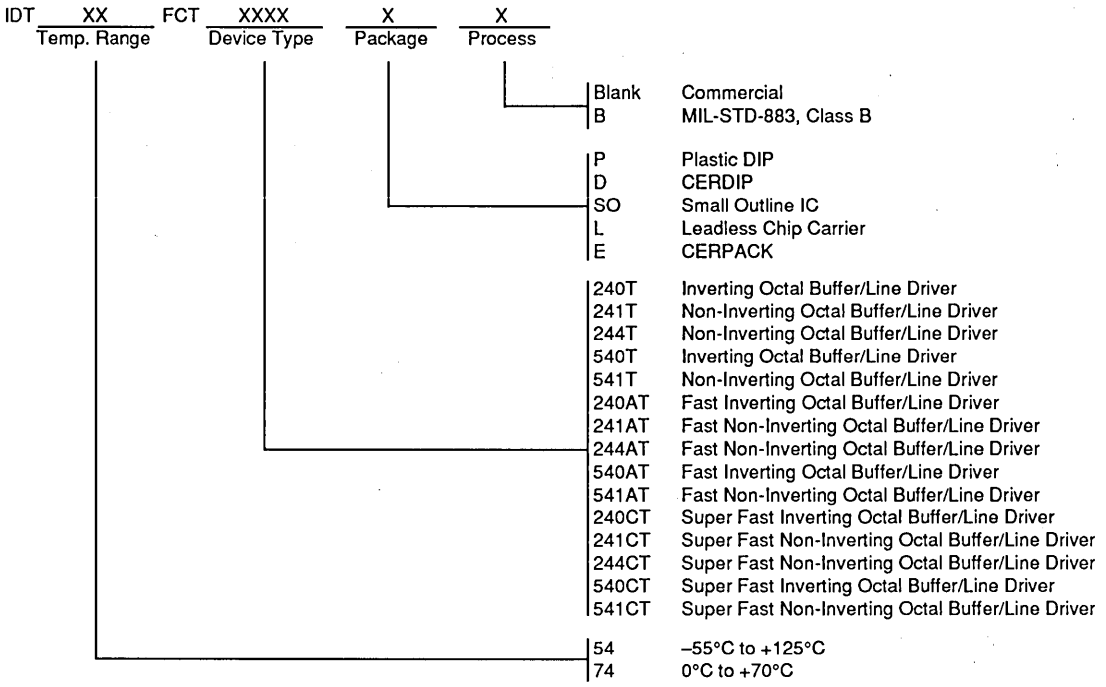


NOTES 2565 drw 10

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2565 cnv* 15

Integrated Device Technology, Inc.

FAST CMOS OCTAL BIDIRECTIONAL TRANSCEIVERS

IDT54/74FCT245T/AT/CT
IDT54/74FCT640T/AT/CT
IDT54/74FCT645T/AT/CT

FEATURES:

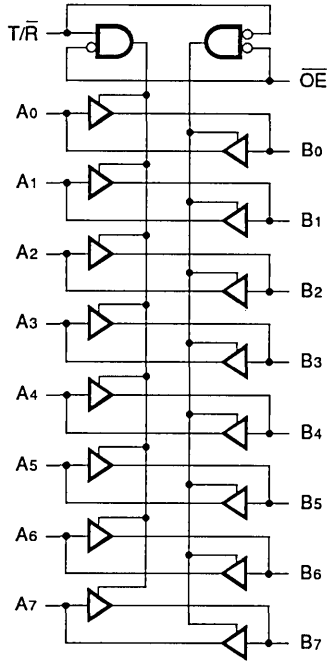
- IDT54/74FCT245T/640T/645T equivalent to FAST™ speed and drive
- **IDT54/74FCT245AT/640AT/645AT 25% faster than FAST™**
- **IDT54/74FCT245CT/640CT/645CT 40% faster than FAST™**
- True TTL input and output compatibility
  — V_{OH} = 3.3V (typ.)
  — V_{OL} = 0.3V (typ.)
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (2.5mW typical static)
- Direction control and over-riding 3-state control
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed
- Meets or exceeds JEDEC Standard 18 specifications

DESCRIPTION:

The IDT octal bidirectional transceivers are built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT245T/AT/CT, IDT54/74FCT640T/AT/CT and IDT54/74FCT645T/AT/CT are designed for asynchronous two-way communication between data buses. The transmit/receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The IDT54/74FCT245T/AT/CT and IDT54/74FCT645T/AT/CT transceivers have non-inverting outputs. The IDT54/74FCT640T/AT/CT has inverting outputs.

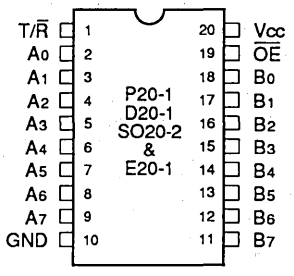
FUNCTIONAL BLOCK DIAGRAM



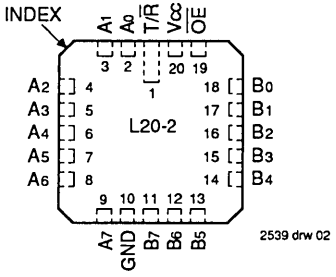
2539 drw 01

FCT245T, 645T are non-inverting options.
FCT640T is the inverting option.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-State Outputs
B_0–B_7	Side B Inputs or 3-State Outputs

2539 tbl 05

FUNCTION TABLE[2]

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A[1]
L	H	Bus A Data to Bus B[1]
H	X	High Z State

NOTE: 2539 tbl 06

1. 640 is inverting from input to output.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES: 2539 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2539 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max	Except I/O Pins	—	—	5	µA
		V_I = 2.7V	I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max	Except I/O Pins	—	—	–5	µA
		V_I = 0.5V	I/O Pins	—	—	–15	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –6mA Mil.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA Com'l.				
			I_{OH} = –12mA Mil.	2.0	3.0	—	
			I_{OH} = –15mA Com'l.				
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 48mA Mil.	—	0.3	0.55	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA Com'l.				
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = V_{CC} or GND		—	0.5	1.5	mA

2539 tbl 03

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = T/$\overline{R}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = T/$\overline{R}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.0	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.3	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = T/$\overline{R}$ = GND Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.5	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.5	14.5[5]	

2539 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT245T/AT/CT

Symbol	Parameter	Conditions[1]	54/74FCT245T				54/74FCT245AT				54/74FCT245CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	1.5	4.1	1.5	4.5	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

2534 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT640T/AT/CT

Symbol	Parameter	Conditions[1]	54/74FCT640T				54/74FCT640AT				54/74FCT640CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	2.0	7.0	2.0	8.0	1.5	5.0	1.5	5.3	1.5	4.4	1.5	4.7	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		2.0	13.0	2.0	16.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		2.0	10.0	2.0	12.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to A or B[3]		2.0	13.0	2.0	16.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		2.0	10.0	2.0	12.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

2534 tbl 08

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT645T/AT/CT

Symbol	Parameter	Conditions[1]	54/74FCT645T				54/74FCT645AT				54/74FCT645CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	1.5	9.5	1.5	11.0	1.5	4.6	1.5	4.9	1.5	4.1	1.5	4.5	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		1.5	11.0	1.5	12.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		1.5	12.0	1.5	13.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	11.0	1.5	12.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	12.0	1.5	13.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

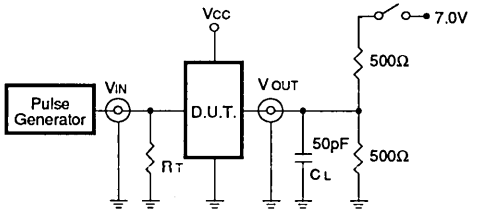
2534 tbl 09

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



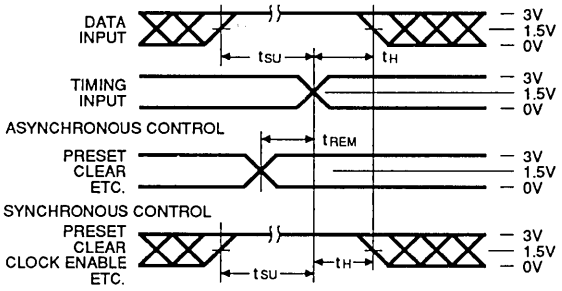
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

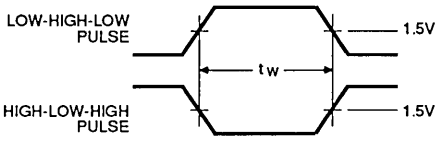
DEFINITIONS: 2539 tbl 10

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

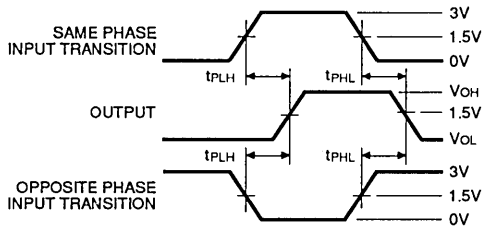
SET-UP, HOLD AND RELEASE TIMES



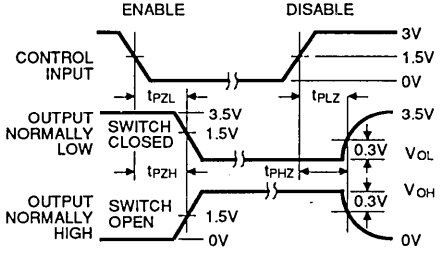
PULSE WIDTH



PROPAGATION DELAY



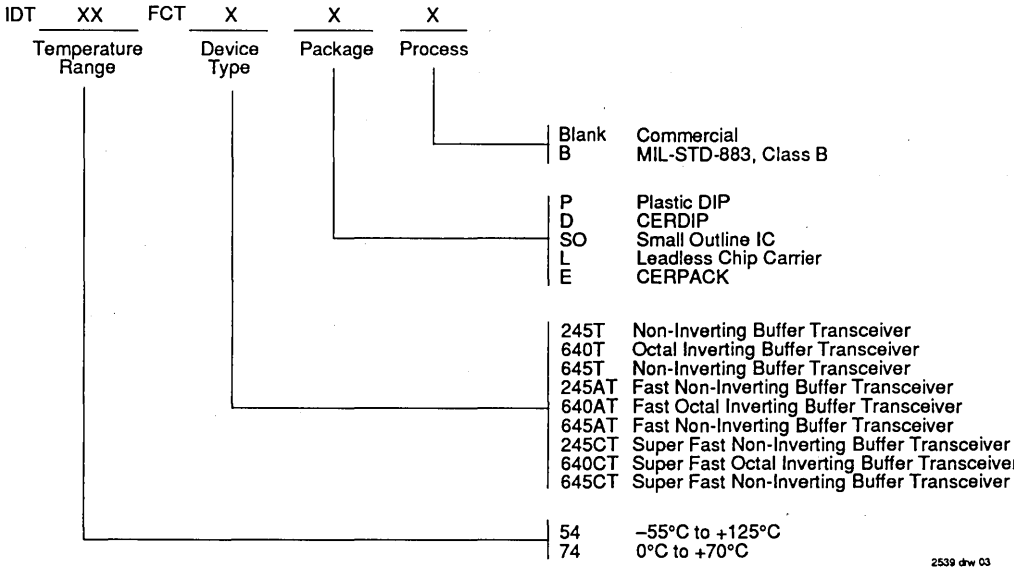
ENABLE AND DISABLE TIMES



NOTES 2539 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH MASTER RESET

IDT54/74/FCT273T
IDT54/74FCT273AT
IDT54/74FCT273CT

FEATURES:

- IDT54/74FCT273T equivalent to FAST™ speed
- **IDT54/74FCT273AT 45% faster than FAST™**
- **IDT54/74FCT273CT 55% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- True TTL input and output levels
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal D flip-flop with Master Reset
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

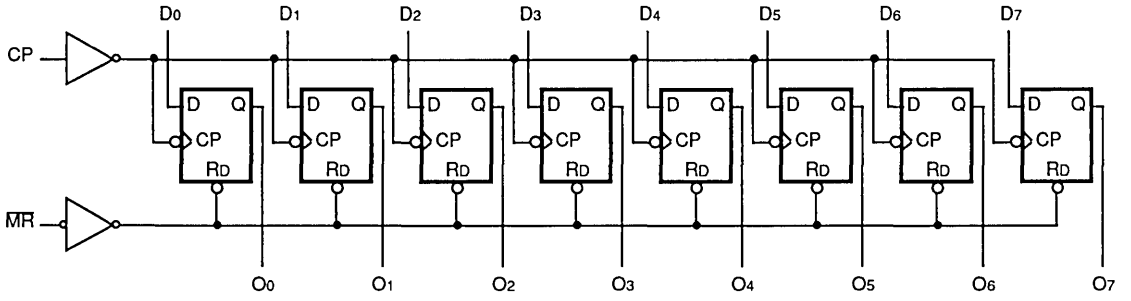
DESCRIPTION:

The IDT54/74FCT273T/AT/CT are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT273T/AT/CT have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

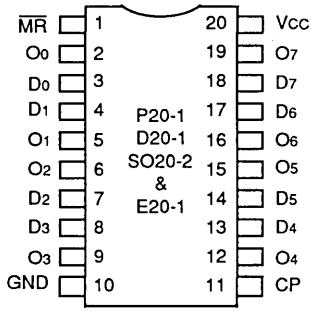
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

FUNCTIONAL BLOCK DIAGRAM



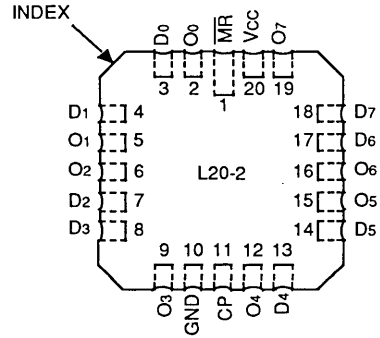
2568 cnv* 03

PIN CONFIGURATIONS



2568 cnv* 01

DIP/SOIC/CERPACK
TOP VIEW



2568 cnv* 02

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
D_N	Data Inputs
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
O_N	Data Outputs

2568 tbl 05

FUNCTION TABLE[1]

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

2568 tbl 06

NOTE:
1. H = HIGH voltage level steady state
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
   L = LOW voltage level steady state
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2568 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2568 tbl 02

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2568 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{MR}$ = Vcc One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle $\overline{MR}$ = Vcc One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle $\overline{MR}$ = Vcc Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2568 tbl 07

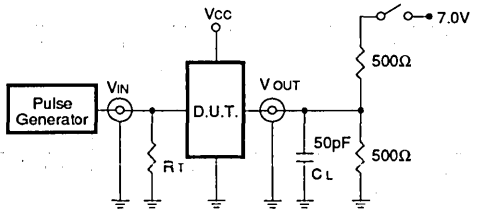
NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



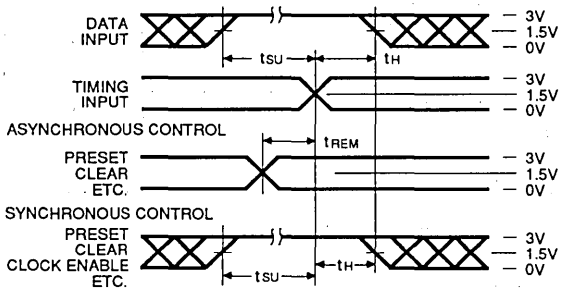
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

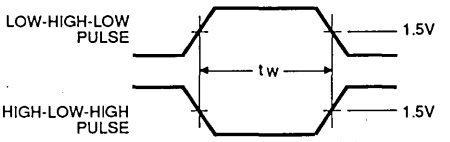
DEFINITIONS: 2568 tbl 07

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

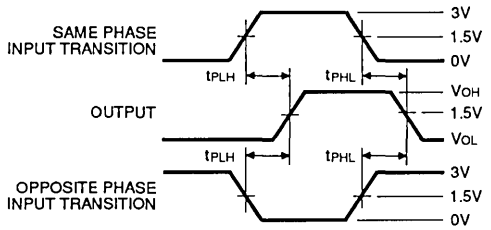
SET-UP, HOLD AND RELEASE TIMES



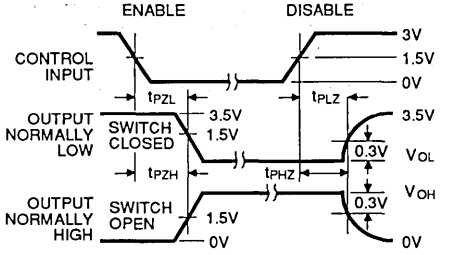
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES 2568 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

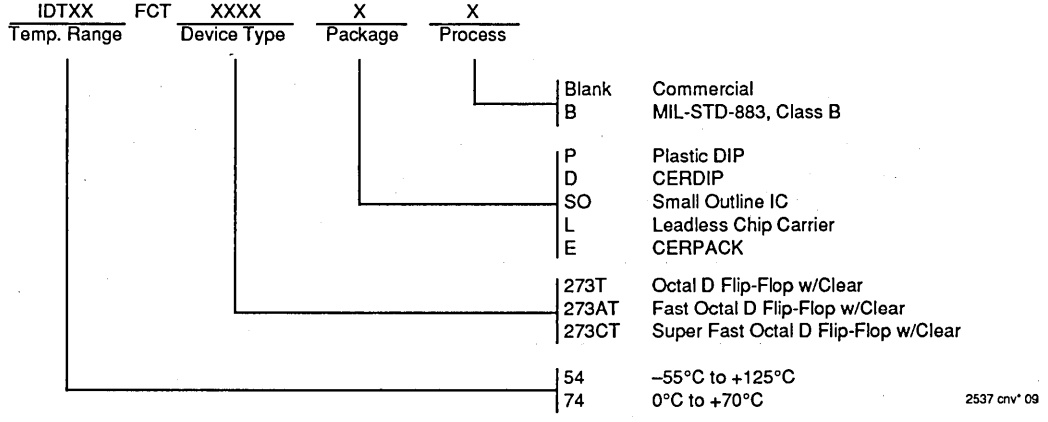
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT273T				IDT54/74FCT273AT				IDT54/74FCT273CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to On	CL = 50pF RL = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.8	2.0	6.5	ns
tPHL	Propagation Delay $\overline{MR}$ to On		2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	6.1	2.0	6.8	ns
tSU	Set-up Time HIGH or LOW Dn to CP		3.0	—	3.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Dn to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tREM	Recovery Time $\overline{MR}$ to CP		4.0	—	5.0	—	2.0	—	2.5	—	2.0	—	2.5	—	ns

NOTES:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2568 tbl 08

ORDERING INFORMATION



2537 cnv* 09

6

Integrated Device Technology, Inc.

FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74/FCT299T
IDT54/74/FCT299AT

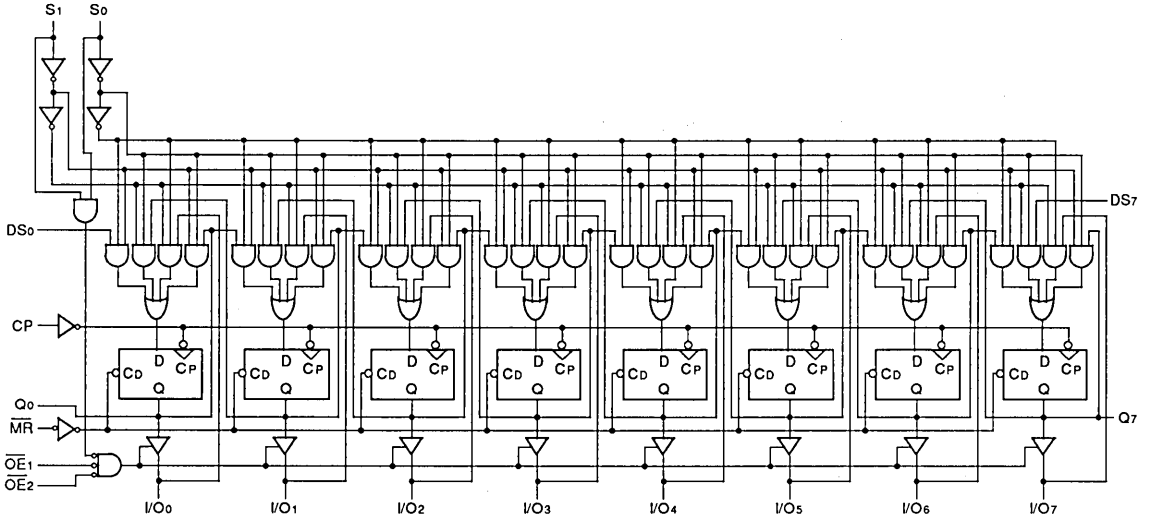
FEATURES:

- IDT54/74FCT299T equivalent to FAST™ speed
- **IDT54/74FCT299AT 25% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 8-input universal shift register
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT299T and IDT54/74FCT299AT are built using advanced CEMOS™, a dual-metal CMOS technology. The IDT54/74FCT299T and IDT54/74FCT299AT are 8-input universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

FUNCTIONAL BLOCK DIAGRAM



2632 drw 01

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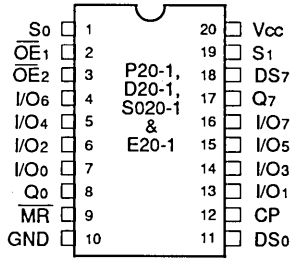
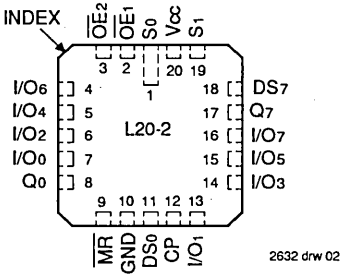
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
CP	Clock Pulse Input (Active Edge Rising)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O_0–I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
O_0, O_7	Serial Outputs

2632 tbl 01

FUNCTION TABLE[1]

Inputs				
$\overline{MR}$	S_1	S_0	CP	Response
L	X	X	X	Asynchronous Reset Q_0–Q_7 = LOW
H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

NOTE: 2632 tbl 02
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2632 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5 unless otherwise noted.
2. Inputs and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2632 tbl 04
1. This parameter is guaranteed by characterization data and not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V	Except I/O Pins	—	—	5	µA
			I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V	Except I/O Pins	—	—	-5	µA
			I/O Pins	—	—	-15	
I_I	Input HIGH Current	V_{CC} = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.,[3] V_O = GND		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL. I_{OH} = -8mA COM'L.	2.4	3.3	—	V
			I_{OH} = -12mA MIL. I_{OH}= -15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or Vcc		—	0.2	1.5	mA

NOTES:
2632 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = Vcc S_0 = S_1 = Vcc DS_0 = DS_1 = GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = Vcc S_0 = S_1 = Vcc DS_0 = DS_7 = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = Vcc S_0 = S_1 = Vcc DS_0 = DS_7 = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2632 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

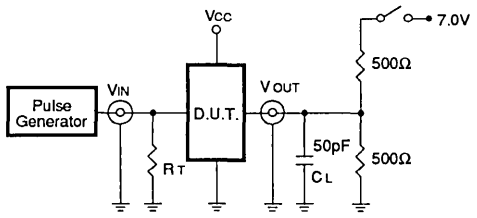
Symbol	Parameter	Condition[1]	IDT54/74FCT299T				IDT54/74FCT299AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Q_0 or Q_7	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	14.0	2.0	7.2	2.0	9.5	ns
tPLH tPHL	Propagation Delay CP to I/O_n		2.0	12.0	2.0	12.0	2.0	7.2	2.0	9.5	ns
tPHL	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		2.0	10.0	2.0	10.5	2.0	7.2	2.0	9.5	ns
tPHL	Propagation Delay $\overline{MR}$ to I/O_n		2.0	15.0	2.0	15.0	2.0	8.7	2.0	11.5	ns
tPZH tPZL	Output Enable Time $\overline{OE}_n$ to I/O_n		1.5	11.0	1.5	15.0	1.5	6.5	1.5	7.5	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}_n$ to I/O_n		1.5	7.0	1.5	9.0	1.5	5.5	1.5	6.5	ns
tSU	Set-up Time HIGH or LOW S_0 or S_1 to CP		7.5	—	7.5	—	3.5	—	4.0	—	ns
tH	Hold Time HIGH or LOW S_0 or S_1 to CP		1.0	—	1.0	—	1.0	—	1.0	—	ns
tSU	Set-up Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		5.5	—	5.5	—	4.0	—	4.5	—	ns
tH	Hold Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns
tW	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns
tREM	Recovery Time $\overline{MR}$ to CP		7.0	—	7.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2632 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



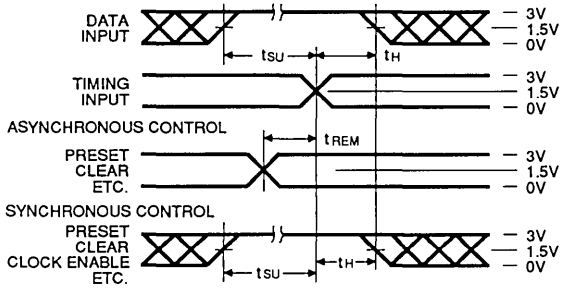
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

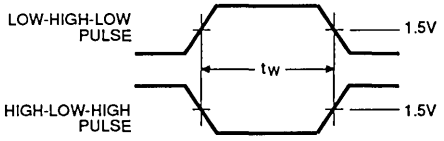
DEFINITIONS: 2632 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

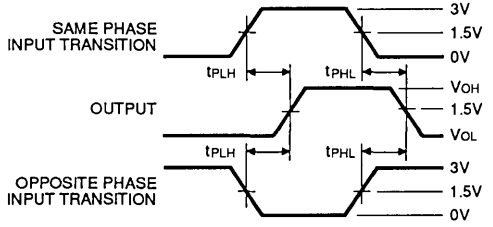
SET-UP, HOLD AND RELEASE TIMES



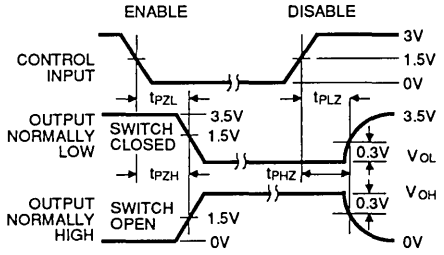
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

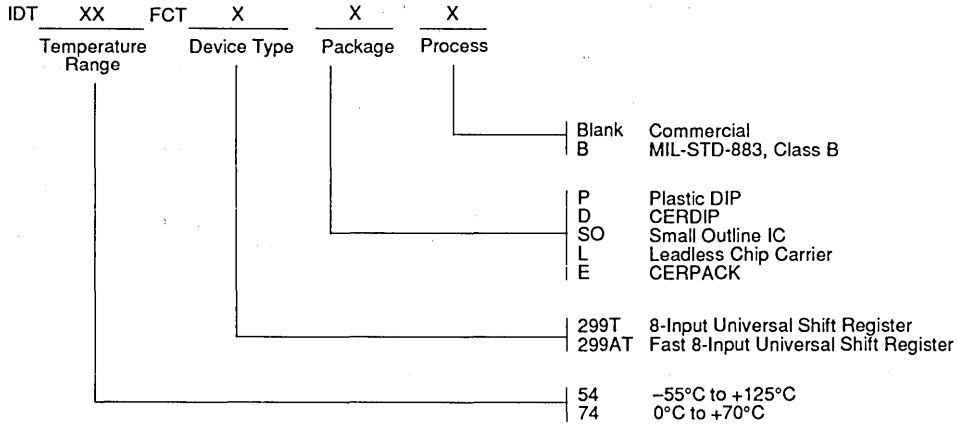


NOTES 2632 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCHES

IDT54/74FCT373T/AT/CT
IDT54/74FCT533T/AT/CT
IDT54/74FCT573T/AT/CT

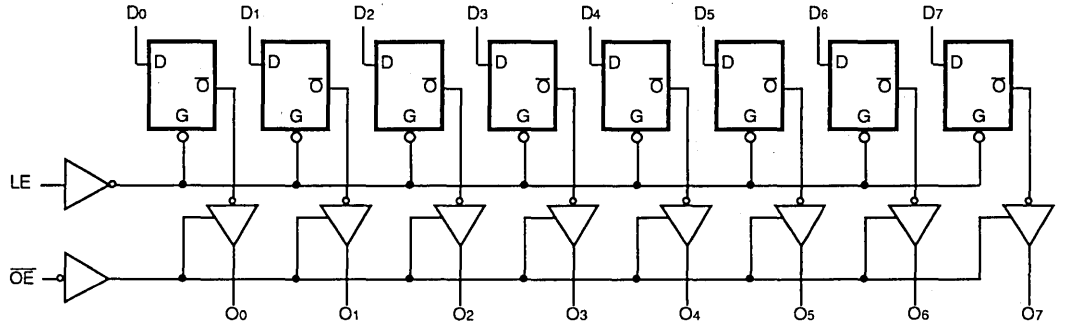
FEATURES

- IDT54/74FCT373T/533T/573T equivalent to FAST™ speed and drive
- **IDT54/74FCT373AT/533AT/573AT up to 30% faster than FAST™**
- **IDT54/74FCT373CT/533CT/573CT up to 40% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- CMOS devices with TRUE TTL input and output compatibility
  - — V_{OH} = 3.3V (typ.)
  - — V_{OL} = 0.3V (typ.)
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Octal transparent latch with 3-state output control
- JEDEC Standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

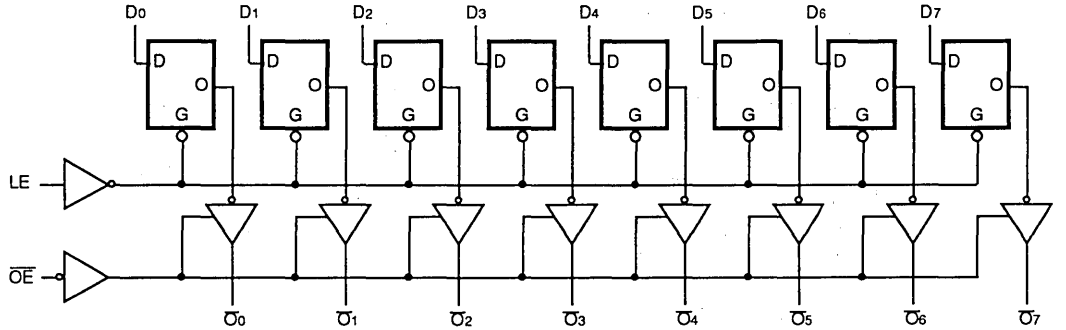
DESCRIPTION

The IDT54/74FCT373T/AT/CT, IDT54/74FCT533T/AT/CT and IDT54/74FCT573T/AT/CT are octal transparent latches built using advanced CEMOS™, a dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT373T/AT/CT AND IDT54/74FCT573T/AT/CT



FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT533T/AT/CT



2564cnv* 01

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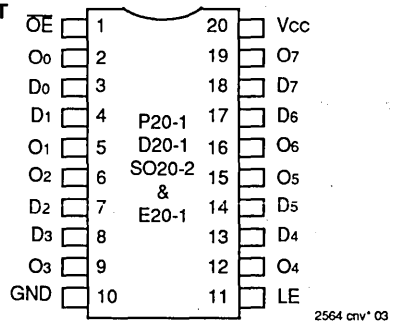
FAST is trademark of National Semiconductor

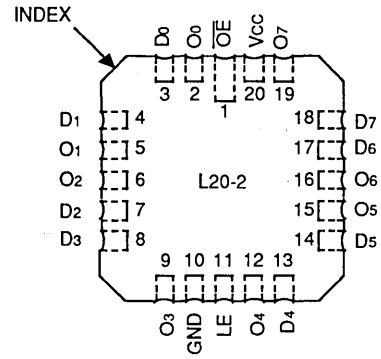
2564 cnv* 02

PIN CONFIGURATIONS

IDT54/74FCT373T

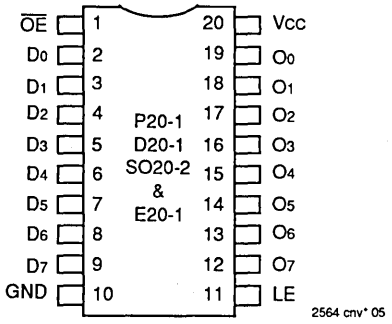


DIP/SOIC/CERPACK
TOP VIEW

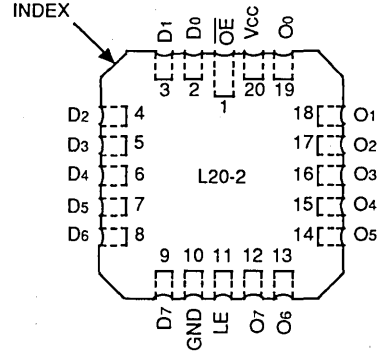


LCC
TOP VIEW

IDT54/74FCT573T

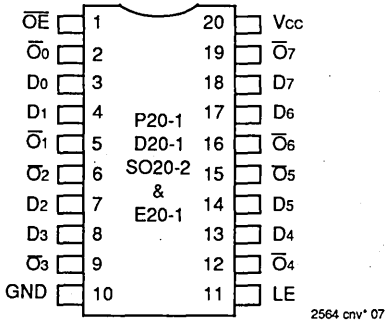


DIP/SOIC/CERPACK
TOP VIEW

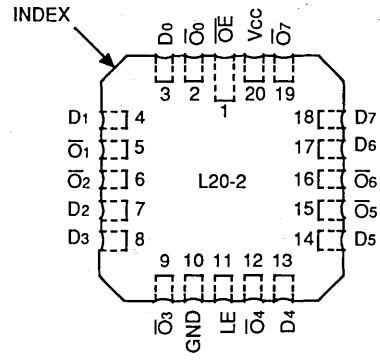


LCC
TOP VIEW

IDT54/74FCT533T



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTION TABLE (FCT533)[1]

Inputs			Outputs
D_N	LE	$\overline{OE}$	$\overline{O}_N$
H	H	L	L
L	H	L	H
X	X	H	Z

2564 tbl 05

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance

FUNCTION TABLE (FCT373 and FCT573)[1]

Inputs			Outputs
D_N	LE	$\overline{OE}$	O_N
H	H	L	H
L	H	L	L
X	X	H	Z

2564 tbl 06

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
D_N	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_N	3-State Outputs
$\overline{O}_N$	Complementary 3-State Outputs

2564 tbl 07

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2564 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2564 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = –55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	Vcc = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	Vcc = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	Vcc = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	Vcc = Max. V_{IN} = GND or Vcc		—	0.2	1.5	mA

NOTES: 2564 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = Vcc One Bit Toggling	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = Vcc Eight Bits Toggling	V_{IN} = Vcc V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2564 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT373T/AT/CT/FCT573T/AT/CT

			FCT373T/573T				FCT373AT/573AT				FCT373CT/573CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Conditions[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay Dn to On	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	1.5	4.2	1.5	5.1	ns
tPLH tPHL	Propagation Delay LE to On		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	2.0	5.5	2.0	8.0	ns
tPZH tPZL	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
tPHZ tPLZ	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
tSU	Set-up Time HIGH or LOW, Dn to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, Dn to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

2564 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT533T/AT/CT

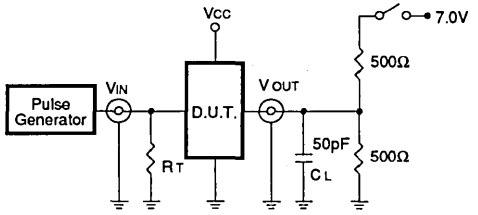
			FCT533T				FCT533AT				FCT533CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Conditions[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay Dn to $\overline{On}$	CL = 50pF RL = 500Ω	1.5	10.0	1.5	12.0	1.5	5.2	1.5	5.6	1.5	4.2	1.5	5.1	ns
tPLH tPHL	Propagation Delay LE to $\overline{On}$		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.8	2.0	5.5	2.0	8.0	ns
tPZH tPZL	Output Enable Time		1.5	11.0	1.5	12.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
tPHZ tPLZ	Output Disable Time		1.5	7.0	1.5	8.5	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
tSU	Set-up Time HIGH or LOW, Dn to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, Dn to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:
2564 tbl 09

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

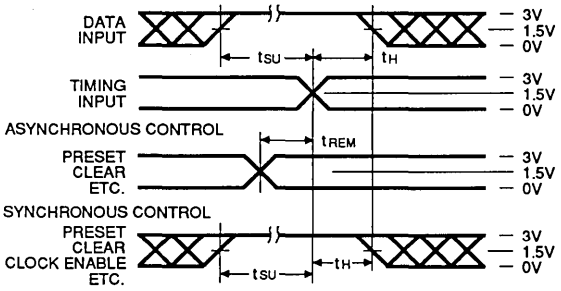
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2564 tbl 10

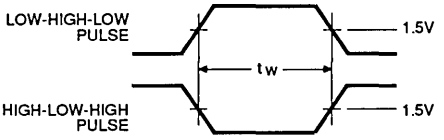
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

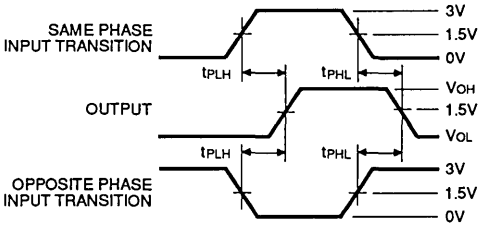
SET-UP, HOLD AND RELEASE TIMES



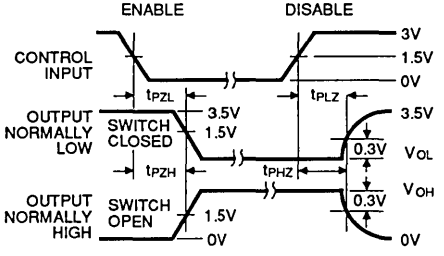
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



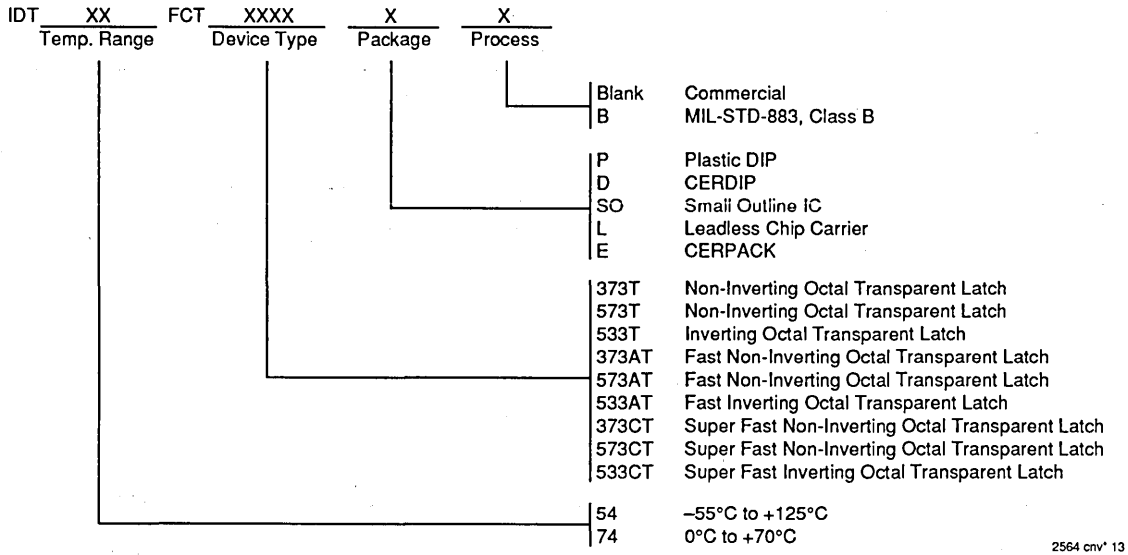
2564 drw 14

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2564 cnv* 13

Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTERS (3-STATE)

IDT54/74FCT374T/AT/CT
IDT54/74FCT534T/AT/CT
IDT54/74FCT574T/AT/CT

FEATURES

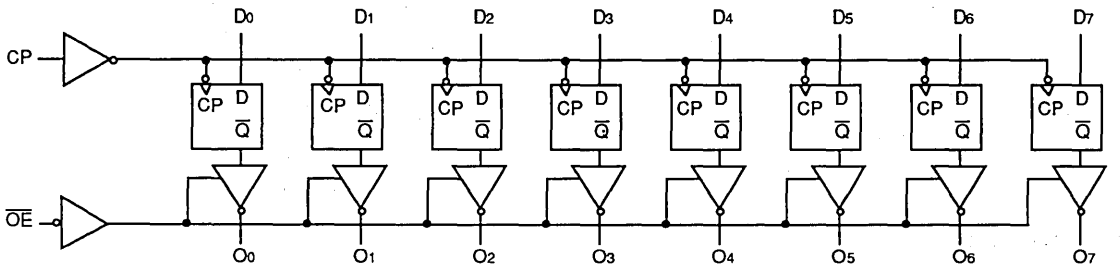
- IDT54/74FCT374T/534T/574T equivalent to FAST™ speed and drive
- **IDT54/74FCT374AT/534AT/574AT up to 30% faster than FAST™**
- **IDT54/74FCT374CT/534CT/574CT up to 50% faster than FAST™**
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Edge triggered master/slave, D-type flip-flops
- Buffered common clock and buffered common three-state control
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications

DESCRIPTION

The IDT54/74FCT374T/AT/CT, IDT54/74FCT534T/AT/CT and IDT54/74FCT574T/AT/CT are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high-impedance state.

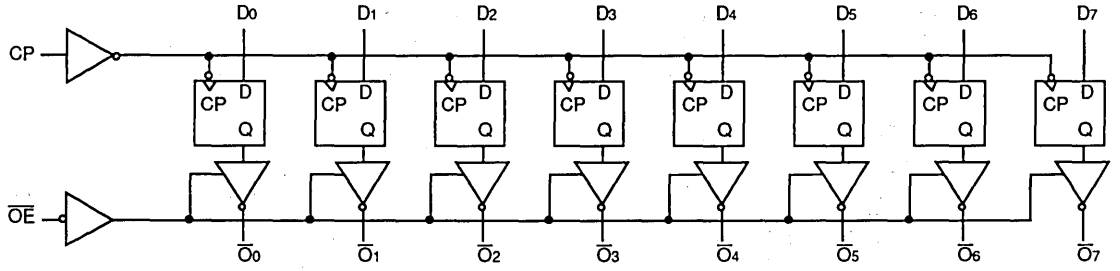
Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT374T AND IDT54/74FCT574T



2569 drw 01

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT534T

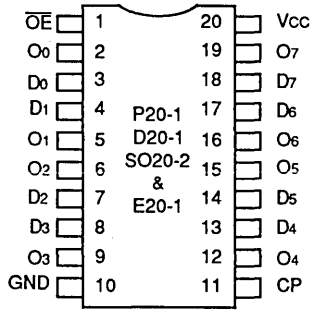


2569 drw 02

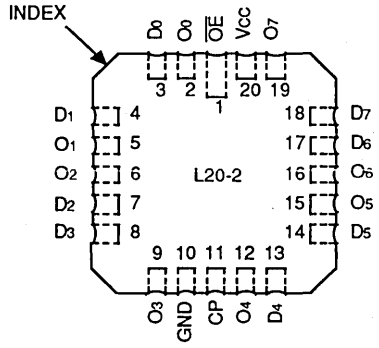
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor

PIN CONFIGURATIONS

IDT54/74FCT374T



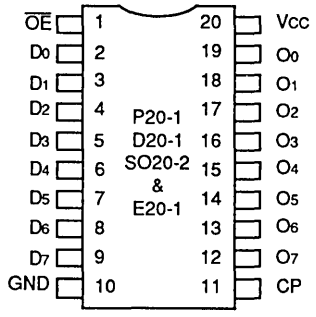
DIP/SOIC/CERPACK
TOP VIEW



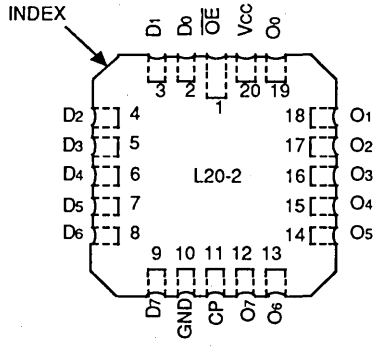
2569 drw 03

LCC
TOP VIEW

IDT54/74FCT574T



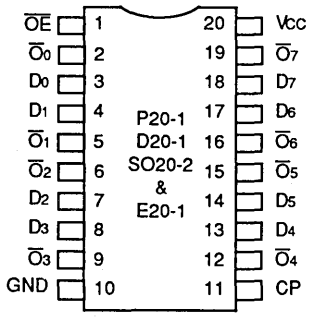
DIP/SOIC/CERPACK
TOP VIEW



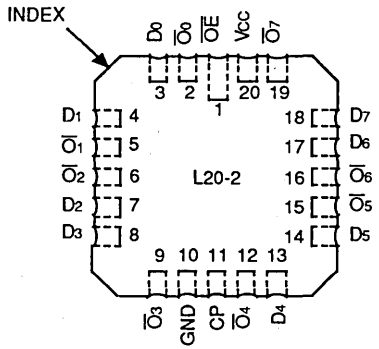
2569 drw 04

LCC
TOP VIEW

IDT54/74FCT534T



DIP/SOIC/CERPACK
TOP VIEW



2569 drw 05

LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
D_N	D flip-flop data inputs
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition.
O_N	3-state outputs, (true)
$\overline{O_N}$	3-state outputs, (inverted)
$\overline{OE}$	Active LOW 3-state Output Enable input

2569 tbl 06

FUNCTION TABLE[1]

	Inputs			FCT534		FCT374/574	
				Outputs	Internal	Outputs	Internal
Function	$\overline{OE}$	CP	D_N	$\overline{O_N}$	Q_N	O_N	$\overline{Q_N}$
HI-Z	H	L	X	Z	NC	Z	NC
	H	H	X	Z	NC	Z	NC
LOAD REGISTER	L	↑	L	H	L	L	H
	L	↑	H	L	H	H	L
	H	↑	L	Z	L	Z	H
	H	↑	H	Z	H	Z	L

NOTE: 2569 tbl 05

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance
   NC = No Change
   ↑ = LOW-to-HIGH transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2569 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2569 tbl 02

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2569 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		$\overline{OE}$ = GND f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
		$\overline{OE}$ = GND Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2569 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

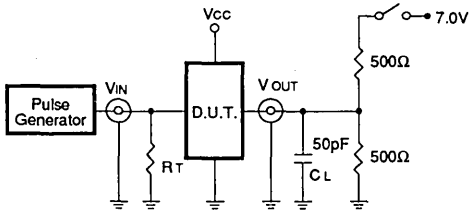
Symbol	Parameter	Conditions[1]	FCT374T/534T/574T				FCT374AT/534AT/574AT				FCT374CT/534CT/574CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to On[3]	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	2.0	5.2	2.0	6.2	ns
tPZH tPZL	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.7	ns
tSU	Set-up Time HIGH or LOW, Dn to CP		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, Dn to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. On for FCT374 and FCT574, $\overline{On}$ for FCT534.

2569 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



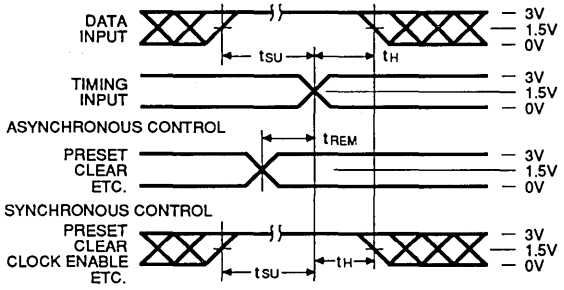
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

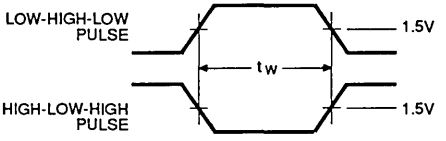
DEFINITIONS: 2569 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

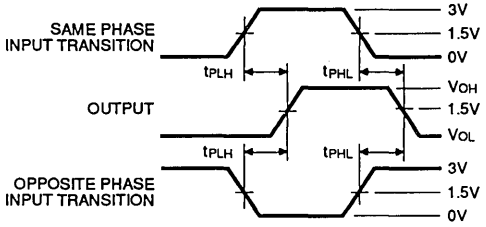
SET-UP, HOLD AND RELEASE TIMES



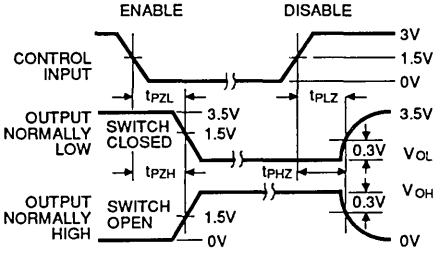
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

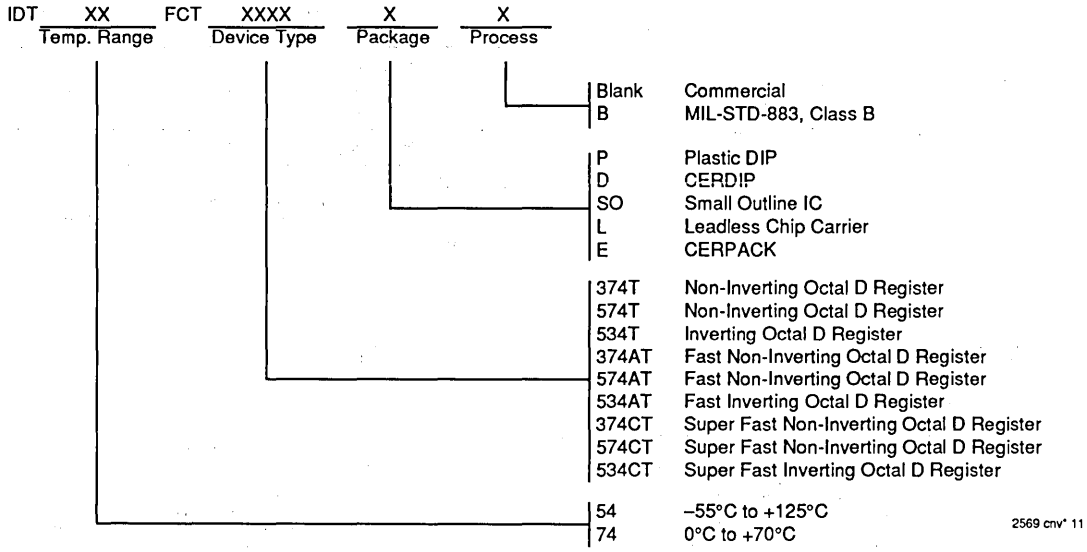


NOTES 2569 drw 06

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74FCT377T
IDT54/74FCT377AT
IDT54/74FCT377CT

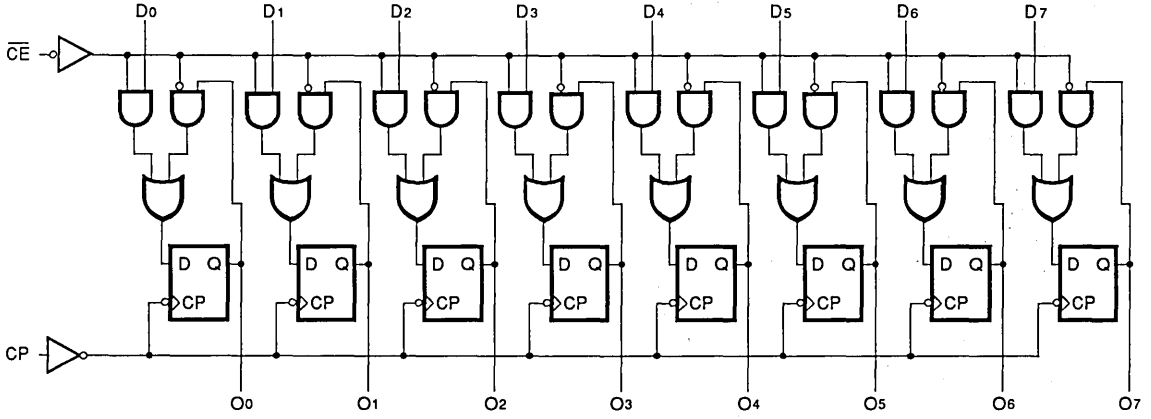
FEATURES:

- IDT54/74FCT377T equivalent to FAST™ speed
- **IDT54/74FCT377AT 25% faster than FAST™**
- **IDT54/74FCT377CT 40% faster than FAST™**
- True TTL input and output compatibility:
  - — V_{OH} = 3.3V (typ.)
  - — V_{OL} = 0.3V (typ.)
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Octal D flip-flop with clock enable
- Meets or exceeds JEDEC Standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

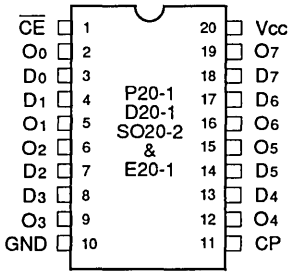
The IDT54/74FCT377T/AT/CT are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT377T/AT/CT have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

FUNCTIONAL BLOCK DIAGRAM

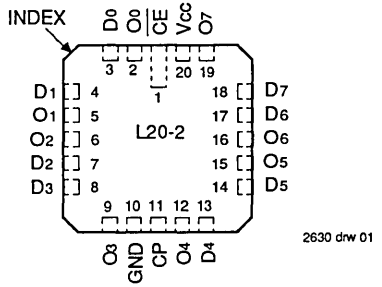


2630 drw 02

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2630 drw 01

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
$D_0 - D_7$	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
$O_0 - O_7$	Data Outputs
CP	Clock Pulse Input

2630 tbl 05

FUNCTION TABLE[1]

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D	O
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	H	H	X	No Change

2630 tbl 06

NOTE:
1. H = HIGH Voltage Level
   h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
   L = LOW Voltage Level
   l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
   X = Immaterial
   ↑ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

2630 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2630 tbl 02

NOTE:
1. This parameter is guaranteed but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	-5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL. I_{OH} = -8mA COM'L.	2.4	3.3	—	V
			I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2630 tbl 03

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{CE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		$\overline{CE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
		$\overline{CE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

NOTES: 2630 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

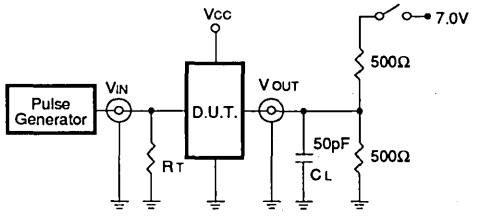
			IDT54/74FCT377T				IDT54/74FCT377AT				IDT54/74FCT377CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	C_L = 50pF R_L = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.2	2.0	5.5	ns
t_{SU}	Set-up Time HIGH or LOW D_n to CP		2.5	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_n to CP		2.0	—	2.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time HIGH or LOW $\overline{CE}$ to CP		4.0	—	4.0	—	3.5	—	3.5	—	3.5	—	3.5	—	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width, HIGH or LOW		7.0	—	7.0	—	6.0	—	7.0	—	6.0	—	7.0	—	ns

NOTES: 2630 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



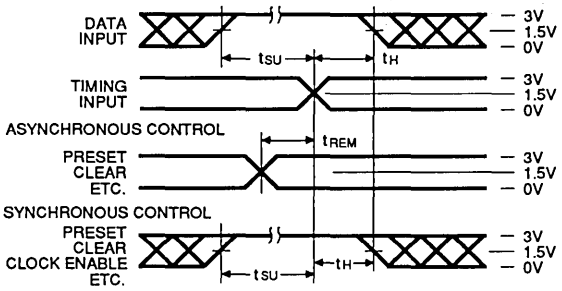
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

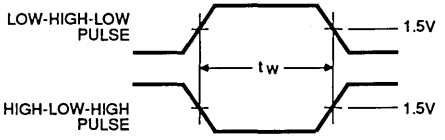
DEFINITIONS: 2630 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

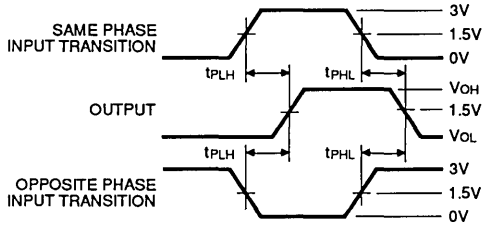
SET-UP, HOLD AND RELEASE TIMES



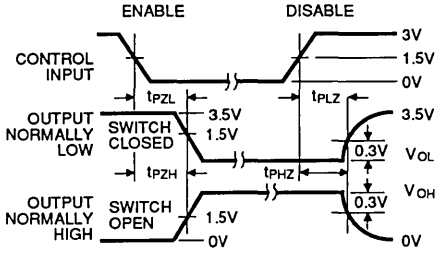
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

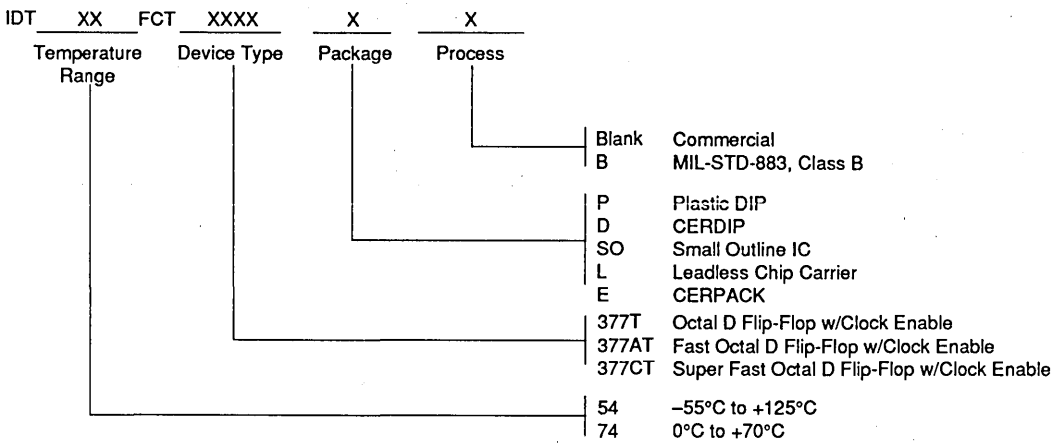


NOTES 2630 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS QUAD DUAL-PORT REGISTER

IDT54/74FCT399T
IDT54/74FCT399AT

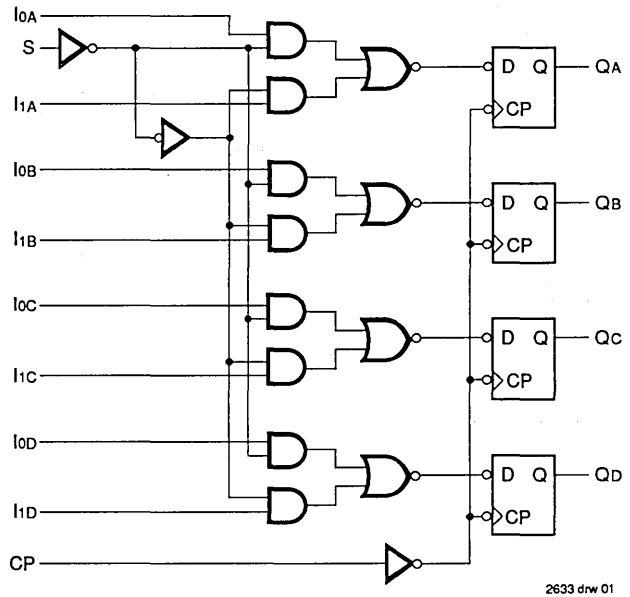
FEATURES:

- IDT54/74FCT399T equivalent to FAST™ speed
- **IDT54/74FCT399AT 30% faster than FAST™**
- Equivalent to FAST™ pinout/function and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Available in 16-pin DIP and SOIC, and 20-pin LCC
- Product avilable in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

Both these devices are high-speed quad dual-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0X}, I_{1X}) and Select input (S) must be stable only one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input for predictable operation.

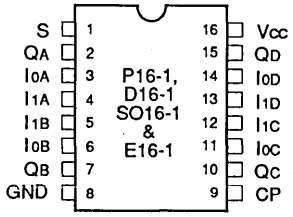
FUNCTIONAL BLOCK DIAGRAM



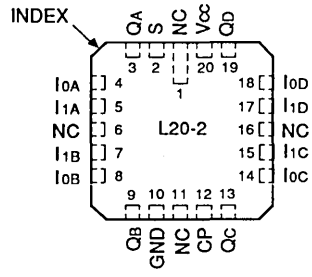
6

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2633 drw 02

LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
S	Common Select Input
CP	Clock Pulse Input (Active Rising Edge)
I_{0A} – I_{0D}	Data Inputs from Source 0
I_{1A} – I_{1D}	Data Inputs from Source 1
Q_A – Q_D	Register True Outputs

2633 tbl 05

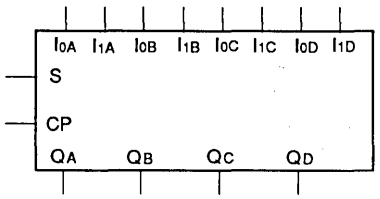
FUNCTION TABLE[1]

Inputs			Outputs
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

2633 tbl 06

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
   l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
   X = Immaterial

LOGIC SYMBOL



2633 drw 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2633 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2633 tbl 02

1. This parameter is measured at characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	Vcc = Max.	V_I = 0.5V	—	—	-5	µA
I_I	Input HIGH Current	Vcc = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	Vcc = Max(3)., V_O = GND		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL. I_{OH} = -8mA COM'L.	2.4	3.3	—	V
			I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	Vcc = Max. V_{IN} = GND or Vcc		—	0.2	1.5	mA

NOTES: 2633 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		One Bit Toggling at f_i = 5MHz 50% Duty Cycle S = Steady State	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
		Four Bits Toggling at f_i = 5MHz 50% Duty Cycle S = Steady State	V_{IN} = 3.4V V_{IN} = GND	—	5.2	12.8[5]	

NOTES:

2633 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FCT399T				IDT54/74FCT399AT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	3.0	10.0	3.0	11.5	2.5	7.0	2.5	7.5	ns
t_{SU}	Set-up Time HIGH or LOW I_n to CP		4.0	—	4.5	—	3.5	—	4.0	—	ns
t_H	Hold Time HIGH or LOW I_n to CP		1.0	—	1.5	—	1.0	—	1.0	—	ns
t_{SU}	Set-up Time HIGH or LOW S to CP		9.0	—	9.5	—	8.5	—	9.0	—	ns
t_H	Hold Time HIGH or LOW S to CP		0	—	0	—	0	—	0	—	ns
t_W	CP Pulse Width HIGH or LOW		5.0	—	7.0	—	5.0	—	6.0	—	ns

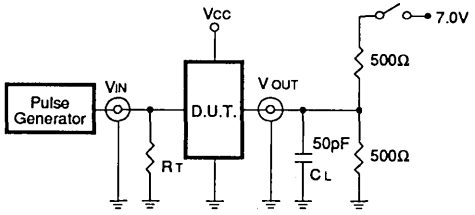
NOTES:

2633 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

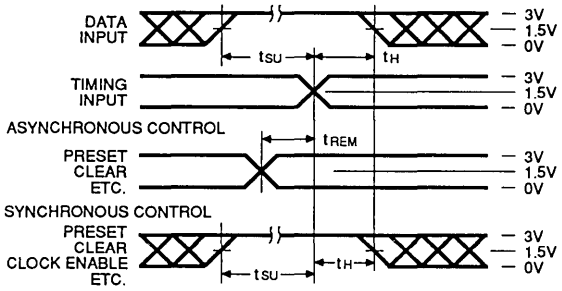
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2633 tbl 08

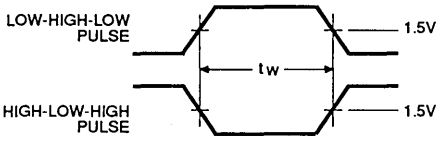
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

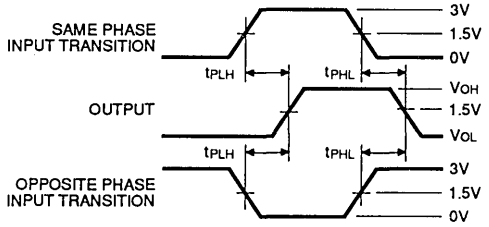
SET-UP, HOLD AND RELEASE TIMES



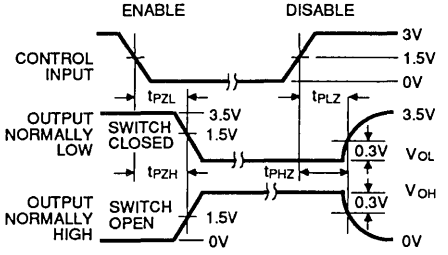
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



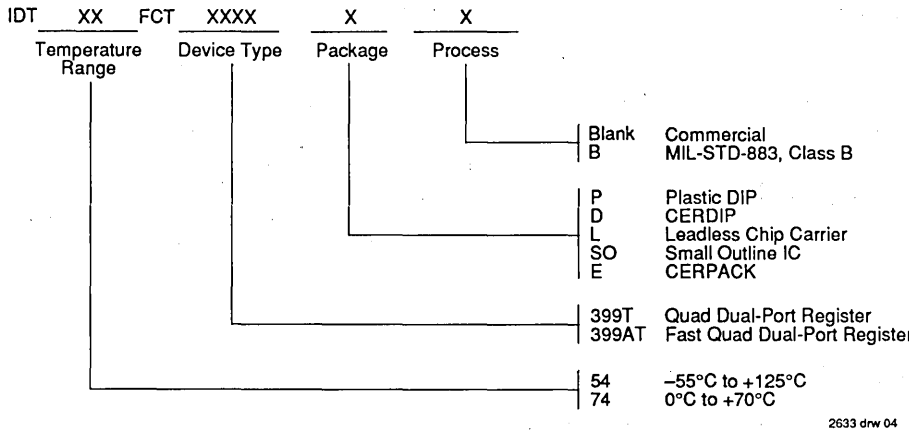
2633 drw 05

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS 8-BIT IDENTITY COMPARATOR

IDT54/74FCT521T
IDT54/74FCT521AT
IDT54/74FCT521BT
IDT54/74FCT521CT

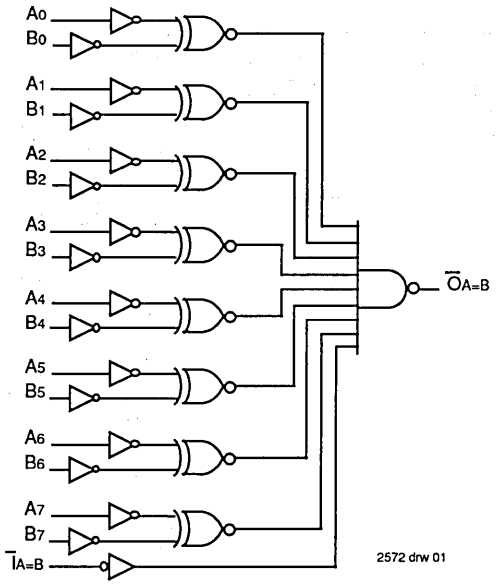
FEATURES:

- IDT54/74FCT521T equivalent to FAST™ speed
- **IDT54/74FCT521AT 35% faster than FAST™**
- **IDT54/74FCT521BT 50% faster than FAST™**
- **IDT54/74FCT521CT 60% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), and 32mA (military)
- CMOS power levels (1mW typ. static)
- True TTL input and output levels
- Substantially lower input current levels than FAST™ (5μA max.)
- 8-bit Identitiy Comparator
- Product available in Radiation Tolerant and Radiation Enhanced versions
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT521T/AT/BT/CT are 8-bit identity comparators built using advanced CEMOS™, a dual metal CMOS technology. These devices compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

FUNCTIONAL BLOCK DIAGRAM



6

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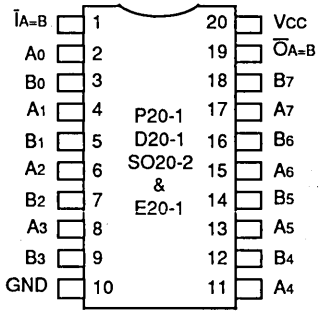
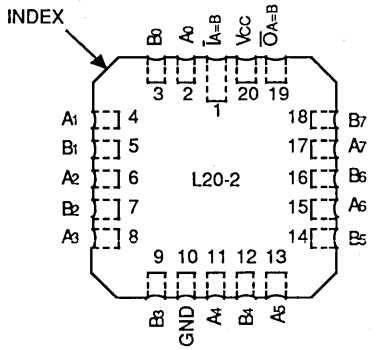
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



2572 drw 02

DIP/SOIC/CERPACK
TOP VIEW



2572 drw 03

LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
A0 - A7	Word A Inputs
B0 - B7	Word B Inputs
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active LOW)

2572 tbl 05

FUNCTION TABLE[1]

Inputs		Output
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

2572 tbl 06

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   *A0 = B0, A1 = B1, A2 = B2, etc.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
VTERM[3]	Terminal Voltage with Respect to GND	–0.5 to VCC	–0.5 to VCC	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES: 2572 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
2. Input and VCC terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE: 2572 tbl 02
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:
2572 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		f_i = 10MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	

NOTES:
2572 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

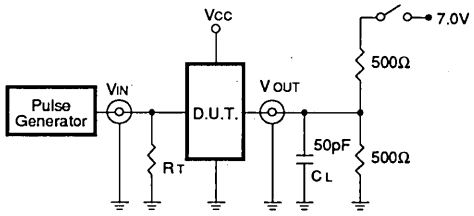
Symbol	Parameter	Condition[1]	IDT54/74FCT521T				IDT54/74FCT521AT				IDT54/74FCT521BT				IDT54/74FCT521CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay An or Bn to $\overline{O}_{A=B}$	CL = 50pF RL = 500Ω	1.5	11.0	1.5	15.0	1.5	7.2	1.5	9.5	1.5	5.5	1.5	7.3	1.5	4.5	1.5	5.1	ns
tPLH tPHL	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$		1.5	10.0	1.5	9.0	1.5	6.0	1.5	7.8	1.5	4.6	1.5	6.0	1.5	4.1	1.5	4.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2572 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

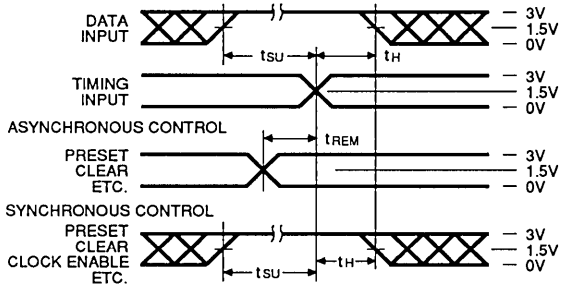
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2572 tbl 08

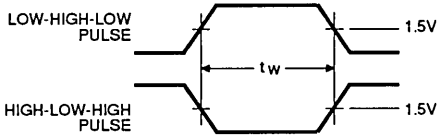
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

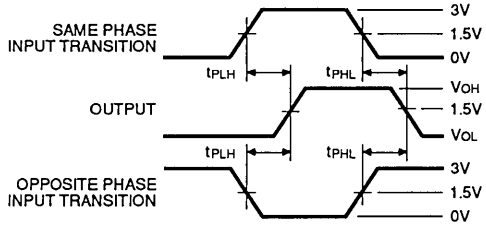
SET-UP, HOLD AND RELEASE TIMES



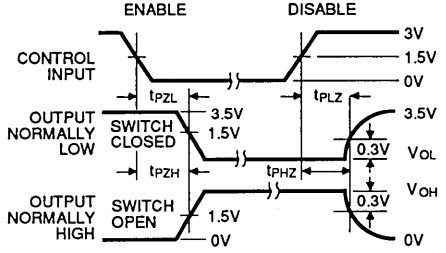
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



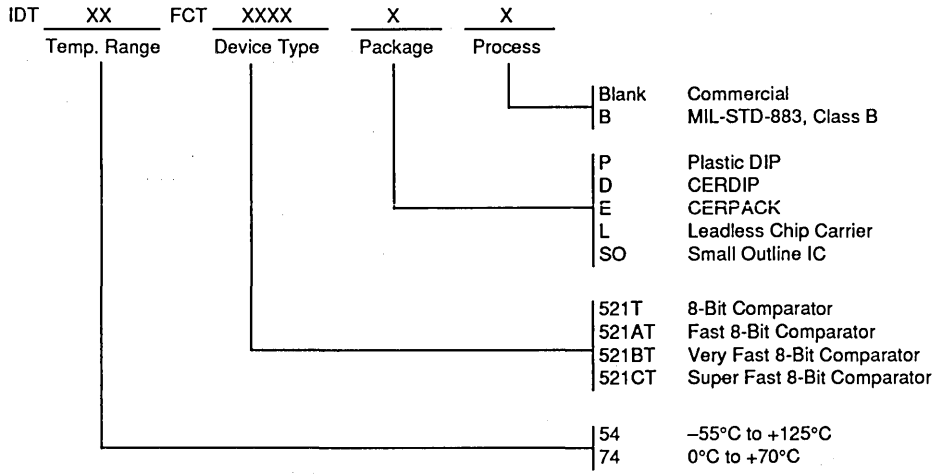
2572 drw 04

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2572 cnv* 08

Integrated Device Technology, Inc.

FAST CMOS OCTAL LATCHED TRANSCEIVER

IDT54/74FCT543T
IDT54/74FCT543AT

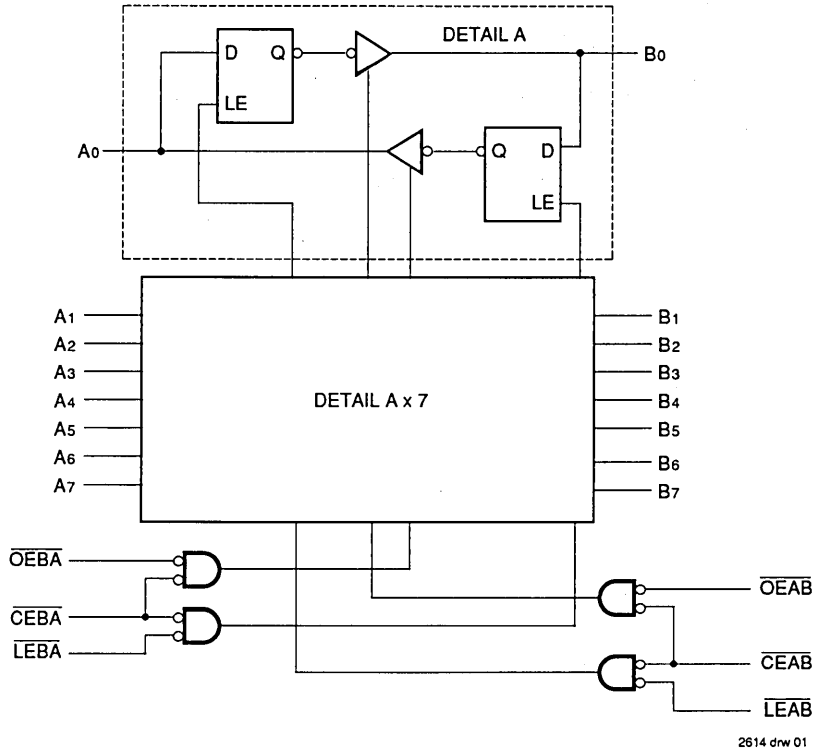
FEATURES:

- IDT54/74FCT543T equivalent to FAST™ speed
- **IDT54/74FCT543AT 25% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial), 48mA (military)
- 8-bit octal latched transceiver
- Separate controls for data flow in each direction
- Back-to-back latches for storage
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than FAST™ (5µA max.)
- True TTL input and output levels
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

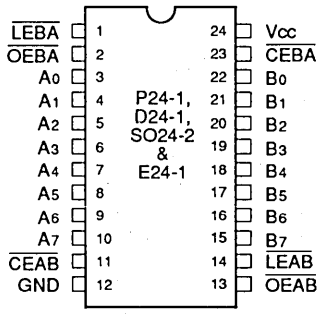
The IDT54/74FCT543T/AT are non-inverting octal transceivers built using advanced CEMOS™, a dual metal CMOS technology. These devices contain two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0–A_7 or to take data from B_0–B_7, as indicated in the Function Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

FUNCTIONAL BLOCK DIAGRAM

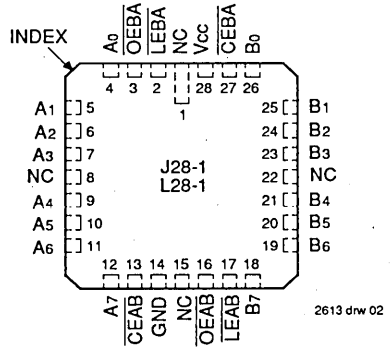


CEMOS is a trademark of Integrated Device Techology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A0–A7	A-to-B Data Inputs or B-to-A 3-State Outputs
B0–B7	B-to-A Data Inputs or A-to-B 3-State Outputs

2613 tbl 02

FUNCTION TABLE(1, 2)

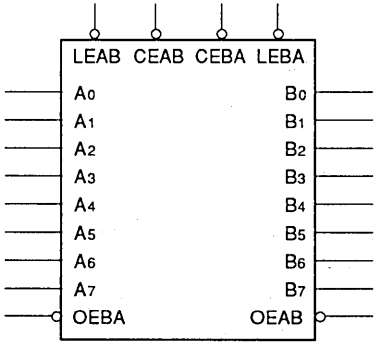
For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B0–B7
H	—	—	Storing	High Z
—	H	—	Storing	—
—	—	H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

2513 tbl 01

NOTES:
1. * Before $\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   — = Don't Care or Irrelevant
2. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

LOGIC SYMBOL



2613 drw 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2614 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2614 tbl 04

1. This parameter is guaranteed by characterization and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	Except I/O Pins	—	—	5	µA
		V_I = 2.7V	I/O Pins	—	—	15	
I_{IL}	Input LOW Current	Vcc = Max.	Except I/O Pins	—	—	-5	µA
		V_I = 0.5V	I/O Pins	—	—	-15	
I_I	Input HIGH Current	Vcc = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.[3], V_O = GND		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min.	I_{OH} = -6mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA COM'L.				
			I_{OH} = -12mA MIL.	2.0	3.0	—	V
			I_{OH} = -15mA COM'L.				
V_{OL}	Output LOW Voltage	Vcc = Min.	I_{OL} = 48mA MIL.[4]	—	0.3	0.55	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA COM'L.				
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	Vcc = Max. V_{IN} = GND or Vcc		—	0.2	1.5	mA

NOTES: 2613 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = Vcc One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = Vcc One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = Vcc Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	7.0	12.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

2613 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at VCC or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT543T				IDT54/74FCT543AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparent Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	2.5	8.5	2.5	10.0	2.5	6.5	2.5	7.5	ns
tPLH tPHL	Propagation Delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn		2.5	12.5	2.5	14.0	2.5	8.0	2.5	9.0	ns
tPZH tPZL	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		2.0	12.0	2.0	14.0	2.0	9.0	2.0	10.0	ns
tPHZ tPLZ	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		2.0	9.0	2.0	13.0	2.0	7.5	2.0	8.5	ns
tSU	Set-up Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		3.0	—	3.0	—	2.0	—	2.0	—	ns
tH	Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	ns

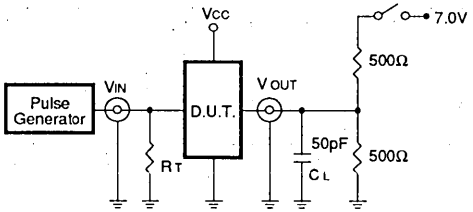
NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2513 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



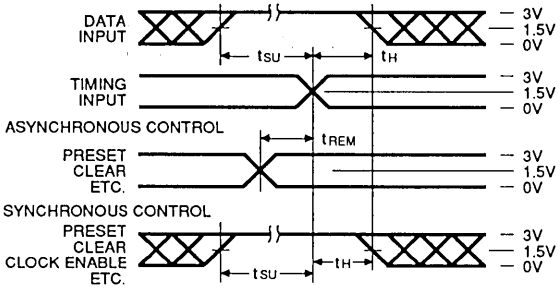
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

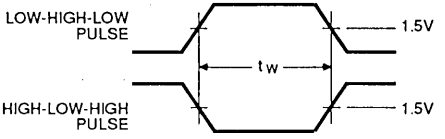
DEFINITIONS: 2613 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

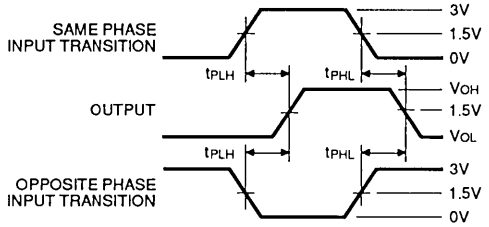
SET-UP, HOLD AND RELEASE TIMES



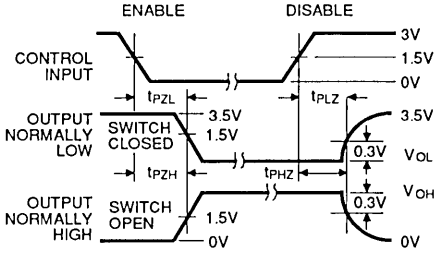
PULSE WIDTH



PROPAGATION DELAY



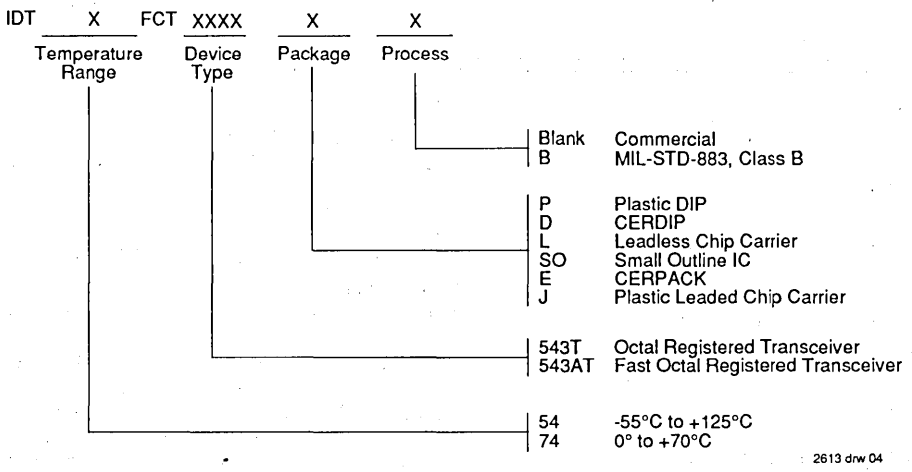
ENABLE AND DISABLE TIMES



NOTES 2613 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTERS (3-STATE)

IDT54/74FCT646T/AT/CT
IDT54/74FCT648T/AT/CT
IDT54/74FCT651T/AT/CT
IDT54/74FCT652T/AT/CT

FEATURES:

- IDT54/74FCT646T/648T/651T/652T equivalent to FAST™ speed
- **IDT54/74FCT646AT/648AT/651AT/652AT 30% faster than FAST™**
- **IDT54/74FCT646CT/648CT/651CT/652CT 40% faster than FAST™**
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of true and inverting data paths
- I_{OL} = 64mA (commercial), 48mA (military)
- CMOS power levels
- TTL input and output level compatible
- Available in 24-pin (300 mil) CERDIP, plastic DIP, SOIC, CERPACK, 28-pin LCC and PLCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

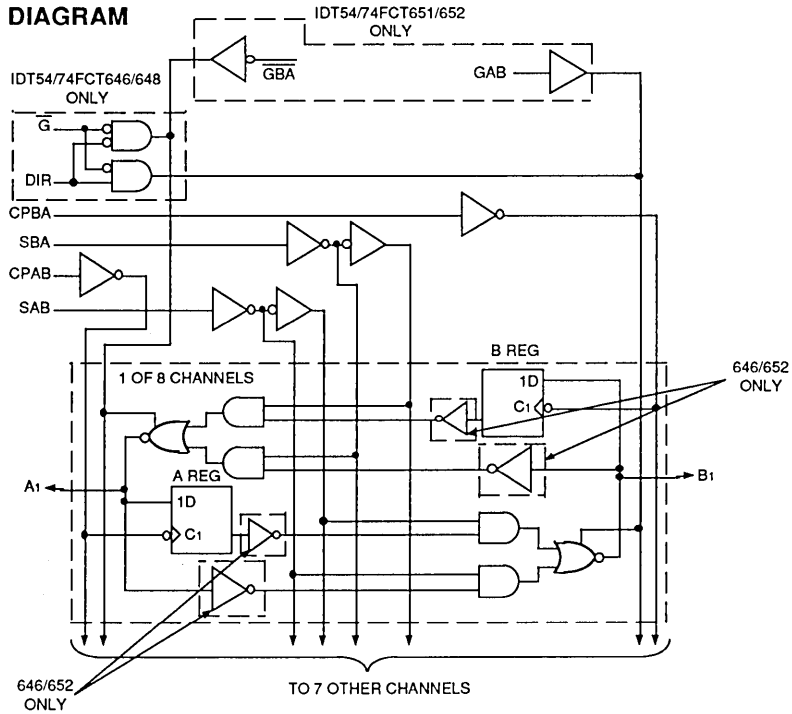
The IDT54/74FCT646/648T/AT/CT and IDT54/74FCT651/652T/AT/CT consist of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

The '651/652 utilize GAB and $\overline{GBA}$ signals to control the transceiver functions. The '646/648 utilize the enable control ($\overline{G}$) and direction (DIR) pins to control the transceiver functions.

SAB and SBA control pins are provided to select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

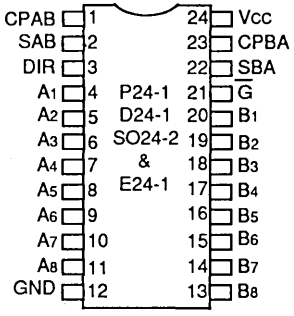
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor, Inc.

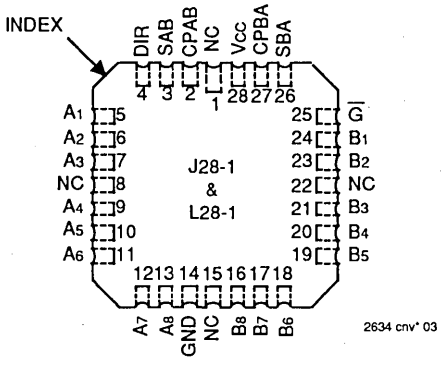
PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

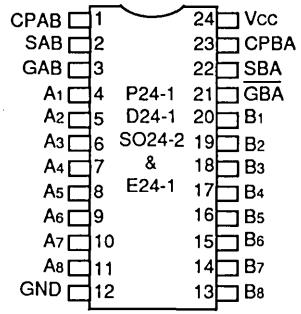
IDT54/74FCT646T/648T

2634 cnv* 02



2634 cnv* 03

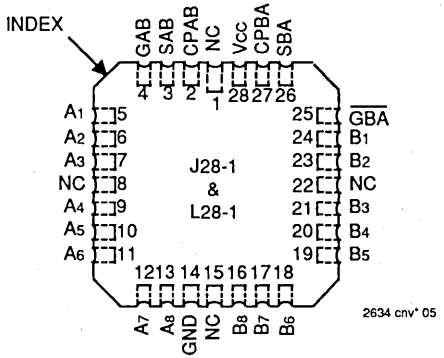
LCC/PLCC
TOP VIEW



DIP/SOIC/CERPACK
TOP VIEW

IDT54/74FCT651T/652T

2634 cnv* 04

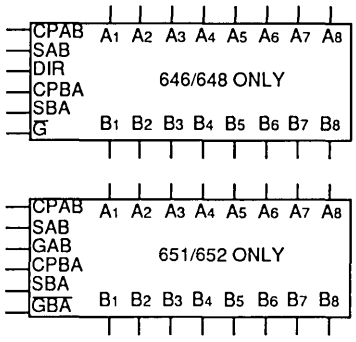


2634 cnv* 05

LCC/PLCC
TOP VIEW

6

LOGIC SYMBOLS



2634 cnv* 05

PIN DESCRIPTION

Pin Names	Description
A1 - A8	Data Register A Inputs Data Register B Outputs
B1 - B8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs (646/648)
GAB, $\overline{GBA}$	Output Enable Inputs (651/652)

2634 tbl 01

FUNCTION TABLE IDT54/74FCT646/648T/AT/CT

Inputs						Data I/O[1]		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	IDT54/74FCT646T	IDT54/74FCT648T
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

2634 tbl 02

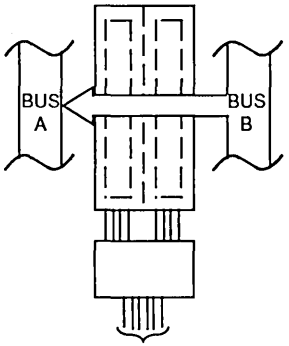
FUNCTION TABLE IDT54/74FCT651/652T/AT/CT

Inputs						Data I/O		Operation or Function	
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	IDT54/74FCT651T	IDT54/74FCT652T
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified[1]	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X[2]	X	Input	Output	Store A in Both Registers[3]	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified[1]	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X[2]	Output	Input	Store B in Both Registers[4]	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

2634 tbl 03

NOTES:

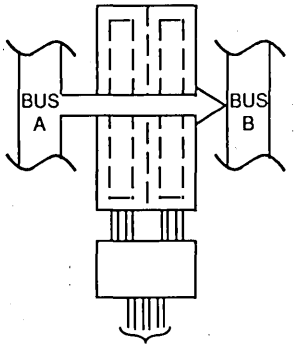
1. The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = HIGH, L = LOW, X = Don't Care, ≠ = LOW-to-HIGH transition.
3. $\overline{A}$ in B Register.
4. $\overline{B}$ in A Register.



651/652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
646/648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A

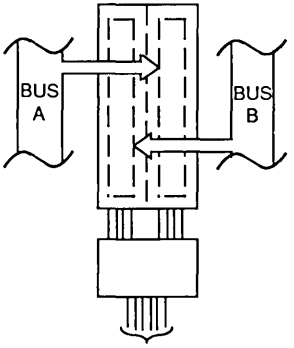
2634 cnv* 07



651/652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	H	X	X	L	X
646/648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X

REAL-TIME TRANSFER BUS A TO B

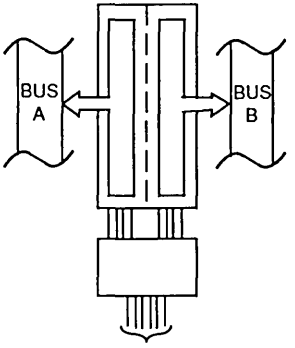
2634 cnv* 08



651/652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X
646/648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X

STORAGE FROM A AND/OR B

2634 cnv* 09



651/652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	L	H or L	H or L	H	H
646/648[1]	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or L	X	H
	H	L	H or L	X	H	X

TRANSFER STORES DATA TO A AND/OR B

2634 cnv* 10

NOTE:
1. 646/648 cannot transfer data to A bus and B bus simultaneously.

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2634 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
2. Input and VCC terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2634 tbl 05

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	−5	µA
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = 2.7V	—	—	15	µA
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	—	—	−15	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		−60	−120	−225	mA
I_{OFF}	Power Down Disable	V_{CC} = GND V_O = 4.5V		—	—	100	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL. I_{OH} = −8mA COM'L.	2.4	3.3	—	V
			I_{OH} = −12mA MIL. I_{OH} = −15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.	—	0.3	0.55	V
			I_{OL} = 64mA COM'L.[4]	—	0.3	0.55	
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:
2634 tbl 06

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These are maximum I_{OL} values per output for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{GAB}$ = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{GAB}$ = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{GAB}$ = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	7.0	12.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

NOTES:

2634 tbl 07

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Outputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	646T/648T/651T/652T				646AT/648AT/651AT/652AT				646CT/648CT/651CT/652CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	5.4	1.5	6.0	ns
tPZH tPZL	Output Enable Time, $\overline{G}$, DIR to Bus[3]		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	1.5	7.8	1.5	8.9	ns
tPHZ tPLZ	Output Disable Time, $\overline{G}$, DIR to Bus[3]		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	6.3	1.5	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	1.5	5.7	1.5	6.3	ns
tPLH tPHL	Propagation Delay SBA or SAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	1.5	6.2	1.5	7.0	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width, HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

NOTES:

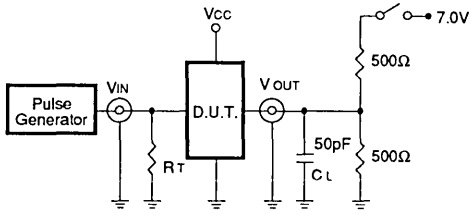
2634 tbl 08

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. GAB, $\overline{GBA}$ to Bus for 651, 652.

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

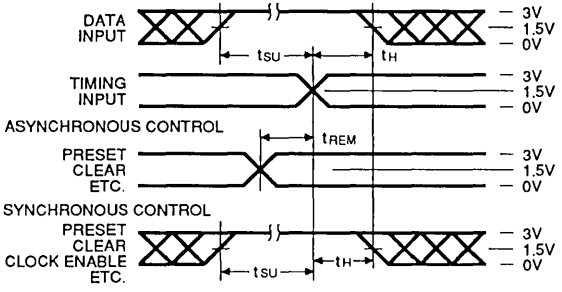
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2537 tbl 08

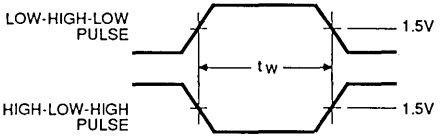
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

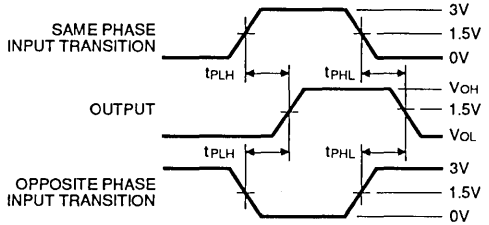
SET-UP, HOLD AND RELEASE TIMES



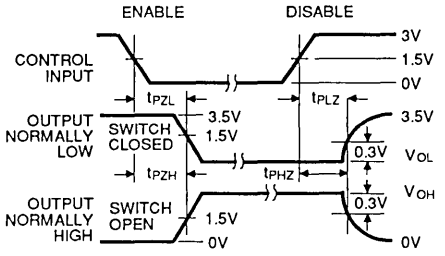
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

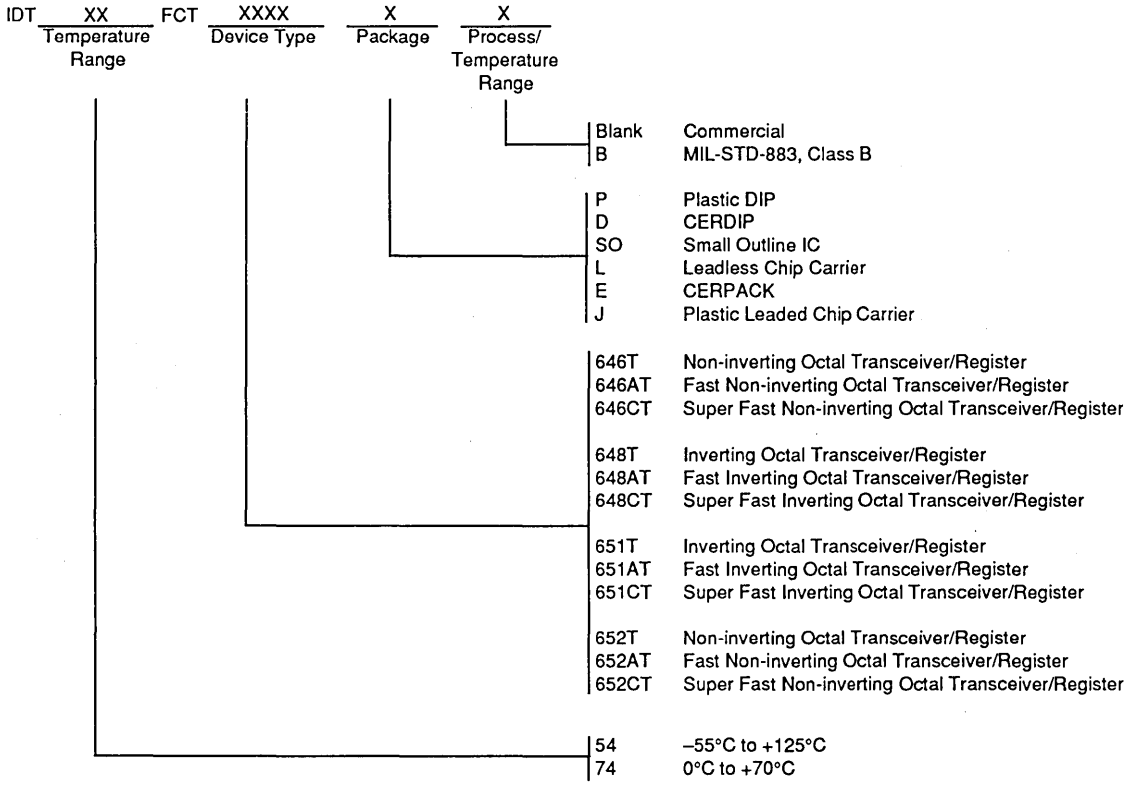


NOTES

2634 drw 15

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_O \leq 50\Omega$; $t_F \leq 2.5$ns; $t_R \leq 2.5$ns.

ORDERING INFORMATION



2634 cnv 16

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL BUS TRANSCEIVERS (3-STATE)

IDT54/74FCT620T/AT/CT
IDT54/74FCT623T/AT/CT

FEATURES

- IDT54/74FCT620T/623T equivalent to FAST™ speed
- **IDT54/74FCT620AT/623AT 25% faster than FAST™**
- **IDT54/74FCT620CT/623CT 45% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- CMOS devices with TRUE TTL input and output compatibility
  - — V_{OH} = 3.3V (typ.)
  - — V_{OL} = 0.3V (typ.)
- Substantially lower input current levels than FAST™ (5µA max.)
- Power Down Disable feature
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

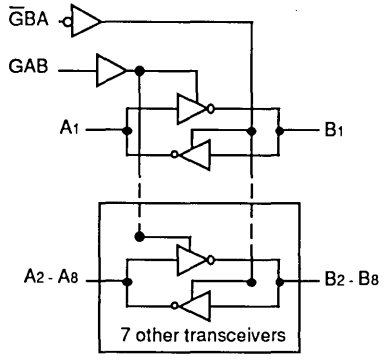
The IDT54/74FCT623T/AT/CT is a non-inverting octal transceiver with 3-state bus-driving outputs in both the send and receive directions. The B bus outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

One important feature of the IDTFCT620T/AT/CT and IDTFCT623T/AT/CT is the Power Down Disable capability. When the GAB and $\overline{GBA}$ inputs are conditioned to put the device in high-Z state, the I/O ports will maintain high impedance during power supply ramps and when Vcc = 0V. This is a desirable feature in back-plane applications where it may be necessary to perform "hot" insertion and disinsertion of cards for on-line maintenance. It is also a benefit in systems with multiple redundancy where one or more redundant cards may be powered-off.

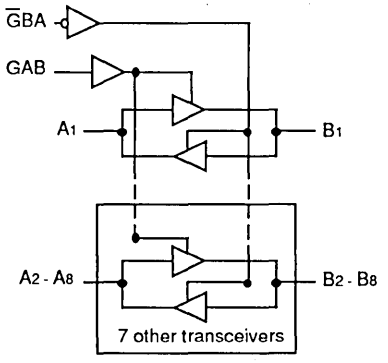
The IDTFCT620T/AT/CT is the inverting option of the IDTFCT623T/AT/CT.

FUNCTIONAL BLOCK DIAGRAMS



FCT620T/AT/CT

2563 cnv* 01

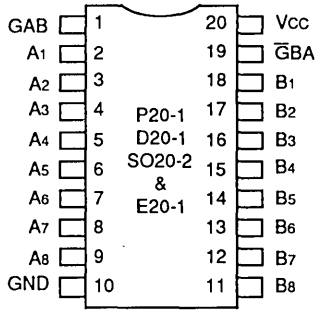


FCT623T/AT/CT

2563 cnv* 02

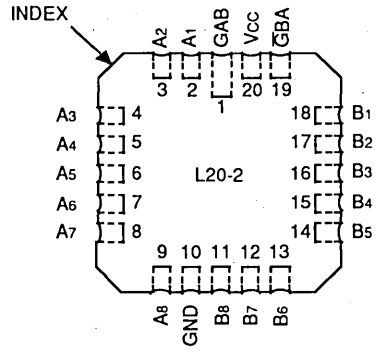
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



2563 cnv* 03

DIP/SOIC/CERPACK
TOP VIEW



2563 cnv* 04

LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
$\overline{GBA}$, GAB	Enable Inputs
A1 - A8	A Bus Inputs or 3-State Outputs
B1 - B8	B Bus Inputs or 3-State Outputs

2563 tbl 01

FUNCTION TABLE(1)

Enable Inputs		Outputs	
$\overline{GBA}$	GAB	FCT620	FCT623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus $\overline{A}$ data to B bus	B data to A bus A data to B bus

NOTES:
1. H = HIGH Voltage Level
2. L = LOW Volage Level
3. Z = HIGH-Impedance (OFF) state

2563 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
VTERM(3)	Terminal Voltage with Respect to GND	–0.5 to VCC	–0.5 to VCC	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES:

2563 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
CI/O	I/O Capacitance	VOUT = 0V	8	12	pF

NOTE:

2563 tbl 04

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	Except I/O Pins	—	—	5	µA
		V_I = 2.7V	I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max.	Except I/O Pins	—	—	−5	µA
		V_I = 0.5V	I/O Pins	—	—	−15	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		−60	−120	−225	mA
I_{OFF}	Power Down Disable	V_{CC} = GND, V_O = 4.5V		—	—	100	µA
V_{OH}	Output HIGH Voltage (A and B Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL. I_{OH} = −8mA COM'L.	2.4	3.3	—	V
			I_{OH} = −12mA MIL. I_{OH} = −15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage (A Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.[4] I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_{OL}	Output LOW Voltage (B Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.[4] I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2563 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{G}BA$ = GAB = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		50% Duty Cycle $\overline{G}BA$ = GAB = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
		50% Duty Cycle $\overline{G}BA$ = GAB = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2563 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT620T/AT/CT

Symbol	Parameter	Condition[1]	54/74FCT620T				54/74FCT620AT				54/74FCT620CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay $\overline{A}$n to Bn	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	5.2	1.5	6.0	1.5	4.5	1.5	5.1	ns
tPLH tPHL	Propagation Delay $\overline{B}$n to An		1.5	7.0	1.5	8.0	1.5	5.2	1.5	6.0	1.5	4.5	1.5	5.1	ns
tPZH tPZL	Output Enable Time $\overline{G}$BA to An		1.5	9.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time $\overline{G}$BA to An		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns
tPZH tPZL	Output Enable Time GAB to Bn		1.5	9.0	1.5	10.5	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time GAB to Bn		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns

2563 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT623T/AT/CT

Symbol	Parameter	Condition[1]	54/74FCT623T				54/74FCT623AT				54/74FCT623CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay An to Bn	CL = 50pF RL = 500Ω	1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPLH tPHL	Propagation Delay Bn to An		1.5	7.5	1.5	9.5	1.5	5.5	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPZH tPZL	Output Enable Time $\overline{G}$BA to An		1.5	9.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time $\overline{G}$BA to An		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns
tPZH tPZL	Output Enable Time GAB to Bn		1.5	9.0	1.5	10.5	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time GAB to Bn		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns

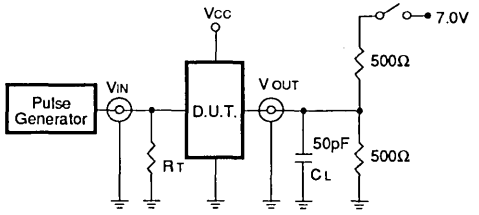
NOTES:

2563 tbl 08

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

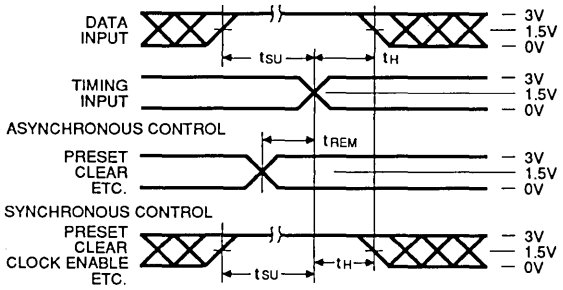
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2563 tbl 09

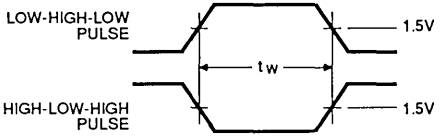
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

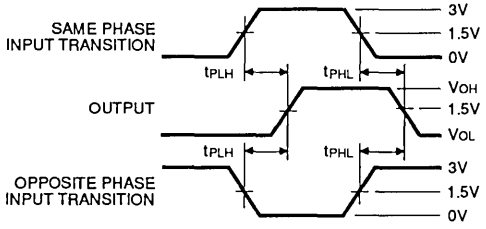
SET-UP, HOLD AND RELEASE TIMES



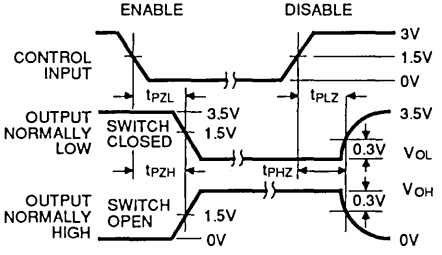
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



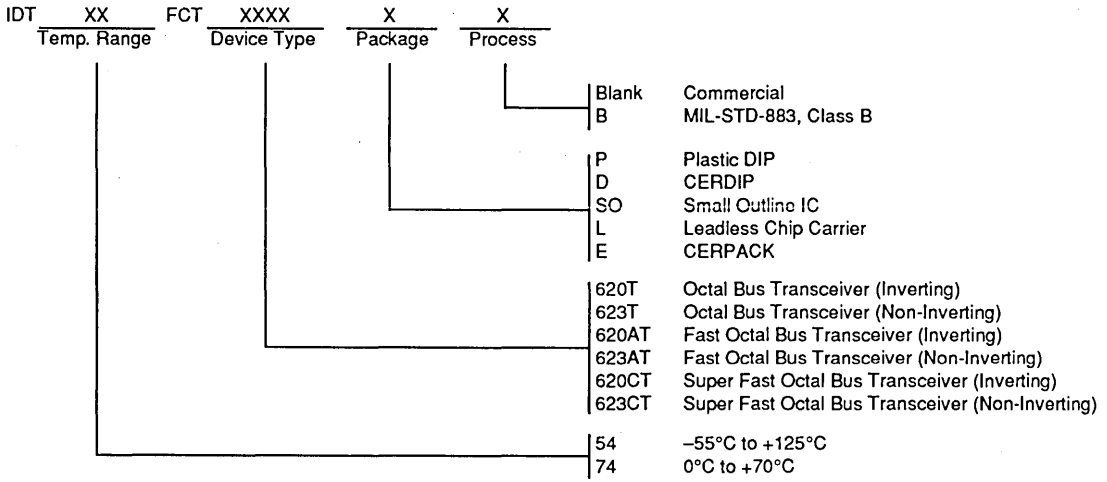
2563 drw 05

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2563 cnv* 10

Integrated Device Technology, Inc.

FAST CMOS OCTAL BUS TRANSCEIVER (OPEN DRAIN)

IDT54/74FCT621T/AT
IDT54/74FCT622T/AT

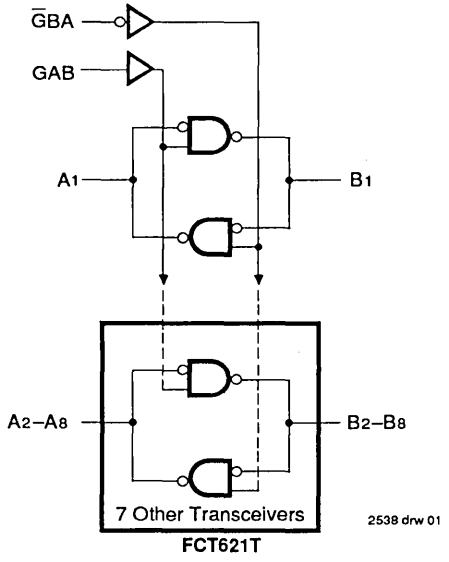
FEATURES:

- IDT54/74FCT621T/622T equivalent to FAST™ speed
- **IDT54/74FCT621AT/622AT 25% faster than FAST™ speed**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- **Power Down Disable feature**
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT621T/AT is an octal transceiver with non-inverting Open-Drain bus compatible outputs in both send and receive directions. The B bus outputs are capable of sinking 64mA providing very good capacitive drive characteristics. These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing. The IDT54/74FCT622T/AT is the inverting option of the '621.

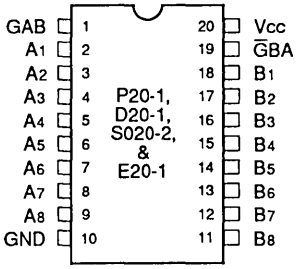
FUNCTIONAL BLOCK DIAGRAM (1)



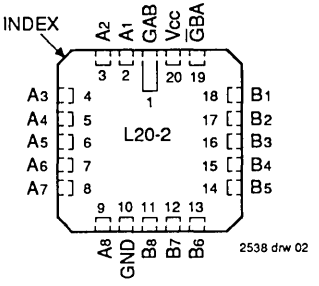
FCT621T

NOTE:
1. The FCT622T is the inverting option of FCT621T.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
$\overline{G}BA$, GAB	Enable Inputs
$A_1 - A_8$	A Inputs or Open-drain Outputs
$B_1 - B_8$	B Inputs or Open-drain Outputs

2538 tbl 05

FUNCTION TABLE[1]

Enable Inputs		Function	
$\overline{G}BA$	GAB	'FCT621T	'FCT622T
L	L	B data to A bus	$\overline{B}$ data to A bus
H	H	A data to B bus	$\overline{A}$ data to B bus
H	L	OFF	OFF
L	H	B data to A bus A data to B bus	$\overline{B}$ data to A bus $\overline{A}$ data to B bus

NOTE: 2538 tbl 06

1. H = HIGH Voltage Level.
   L = LOW Voltage Level.
   OFF = HIGH if pull-up resistor is connected to Open-Drain output.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2538 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2538 tbl 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max	Except I/O Pins	—	—	5	µA
		V_I = 2.7V	I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max	Except I/O Pins	—	—	–5	µA
		V_I = 0.5V	I/O Pins	—	—	–15	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OFF}	Power Down Disable	V_{CC} = GND V_O = 4.5V		—	—	100	µA
I_{OH}	Output HIGH Current	V_{CC} = Max. V_{IN} = V_{IH} or V_{IL}	V_{OH} = V_{CC} (Max.)	—	—	20	µA
V_{OL}	Output LOW Voltage (B Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.[4] I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_{OL}	Output LOW Voltage (A Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.[4] I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current[3]	V_{CC} = max., V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2538 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. This test is performed with outputs preconditioned to the low state. I_{CC} with outputs preconditioned to the high state is guaranteed when the outputs are forced to V_{CC} or GND.
4. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{GBA}$ = GAB = GND or V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6,7]	V_{CC} = Max. Outputs Open $\overline{GBA}$ = GAB = GND or V_{CC} One Bit Toggling at f_i = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open $\overline{GBA}$ = GAB = GND or V_{CC} Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2538 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
7. This test is performed with outputs tied to GND through a pull-down resistor.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FCT621T/AT

Symbol	Parameter	Condition[1]	IDT54/74FCT621T				IDT54/74FCT621AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH	Propagation Delay A to B	C_L = 50pF	5.5	13.0	5.5	13.5	5.5	12.0	5.5	12.5	ns
tPHL		R_L = 500Ω	1.5	8.5	1.5	9.5	1.5	6.8	1.5	7.6	
tPLH	Propagation Delay B to A		5.5	12.5	5.5	13.0	5.5	12.0	5.5	12.5	ns
tPHL			1.5	8.0	1.5	9.0	1.5	6.4	1.5	7.2	
tPLH	Propagation Delay $\overline{G}$BA to A		5.5	14.0	5.5	14.5	5.5	13.0	5.5	13.5	ns
tPHL			1.5	8.5	1.5	9.5	1.5	6.8	1.5	7.6	
tPLH	Propagation Delay GAB to B		5.5	14.0	5.5	14.5	5.5	13.0	5.5	13.5	ns
tPHL			1.5	8.0	1.5	9.0	1.5	6.4	1.5	7.2	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FCT622T/AT

Symbol	Parameter	Condition[1]	IDT54/74FCT622T				IDT54/74FCT622AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH	Propagation Delay $\overline{A}$ to B	C_L = 50pF	5.5	13.5	5.5	14.0	5.5	12.0	5.5	12.5	ns
tPHL		R_L = 500Ω	1.5	8.0	1.5	9.5	1.5	6.0	1.5	7.0	
tPLH	Propagation Delay $\overline{B}$ toA		5.5	12.5	5.5	13.0	5.5	12.0	5.5	12.5	ns
tPHL			1.5	8.0	1.5	9.5	1.5	5.5	1.5	6.5	
tPLH	Propagation Delay $\overline{G}$BA to A		5.5	12.5	5.5	13.0	5.5	11.5	5.5	12.0	ns
tPHL			1.5	10.0	1.5	11.5	1.5	7.0	1.5	8.5	
tPLH	Propagation Delay GAB to B		6.0	12.5	6.0	13.0	6.0	11.5	6.0	12.0	ns
tPHL			1.5	9.5	1.5	11.0	1.5	6.5	1.5	7.5	

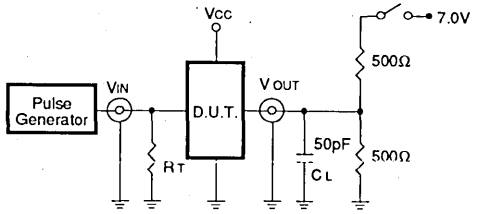
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2538 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

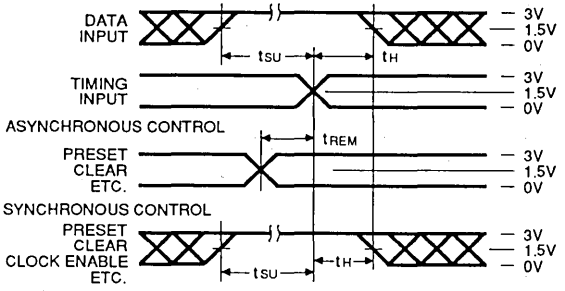
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2538 tbl 08

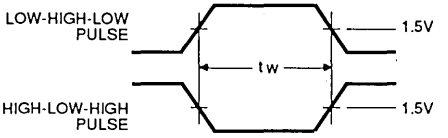
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

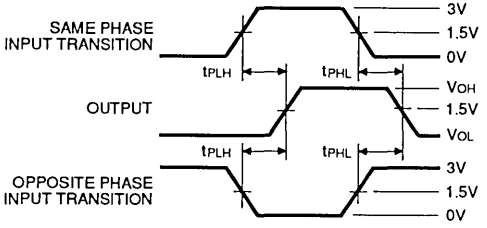
SET-UP, HOLD AND RELEASE TIMES



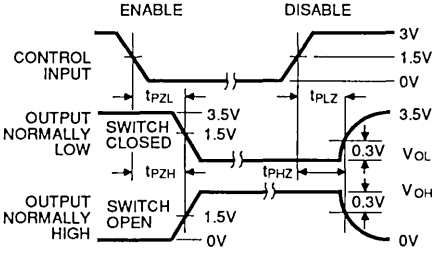
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

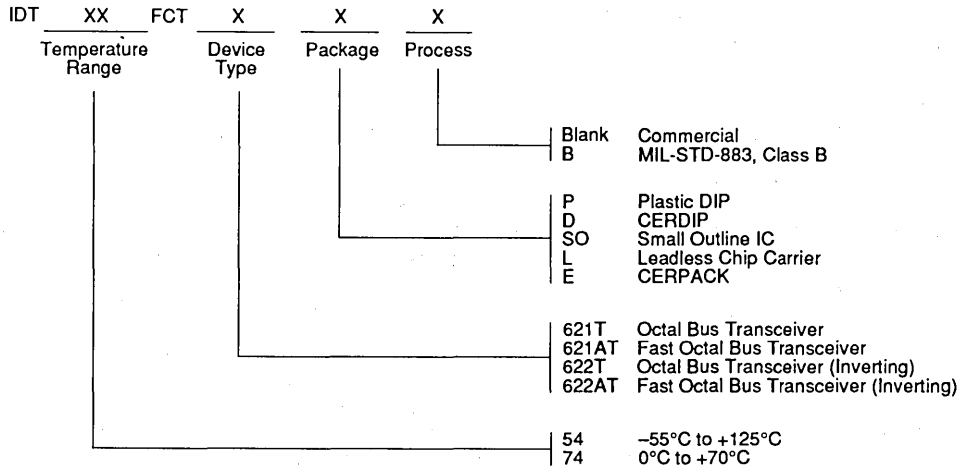


NOTES

2538 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2538 drw 03

6

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT54/74FCT821AT/BT/CT
IDT54/74FCT823AT/BT/CT
IDT54/74FCT825AT/BT/CT

FEATURES:

- IDT54/74FCT821AT/823AT/825AT equivalent to FAST™ speed and drive
- **IDT54/74FCT821BT/823BT/825BT up to 30% faster than FAST™**
- **IDT54/74FCT821CT/823CT/825CT up to 50% faster than FAST™**
- Equivalent to AMD's Am29821-25 bipolar registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meet or exceed JEDEC Standard 18 specifications

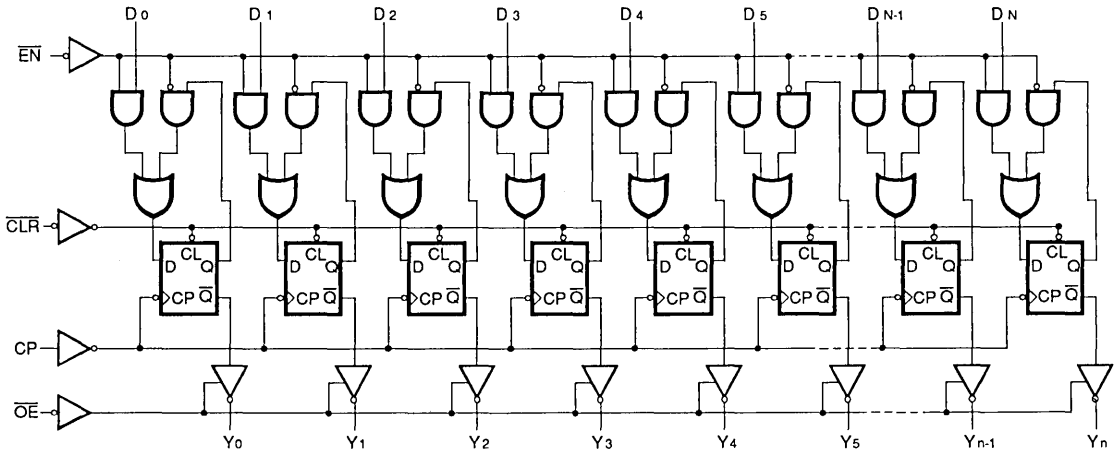
DESCRIPTION:

The IDT54/74FCT800AT/BT/CT series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT821AT/BT/CT are buffered, 10-bit wide versions of the popular '374 function. The IDT54/ 74FCT823AT/BT/CT are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825AT/BT/CT are 8-bit buffered registers with all the '823 controls plus multiple enables ($\overline{OE1}$, $\overline{OE2}$, $\overline{OE3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and $\overline{RD}/\overline{WR}$. They are ideal for use as an output port requiring high IOL/IOH.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high impedance state.

FUNCTIONAL BLOCK DIAGRAM

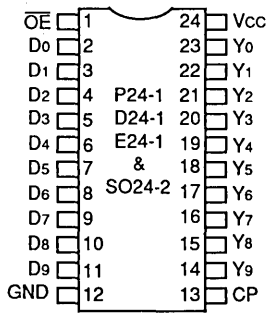


2567 drw 01

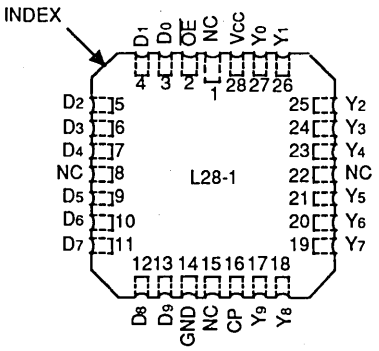
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

PIN CONFIGURATIONS

IDT54/74FCT821T 10-BIT REGISTER

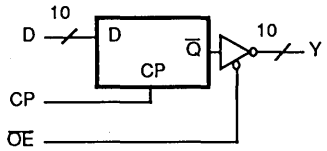


DIP/SOIC/CERPACK
TOP VIEW



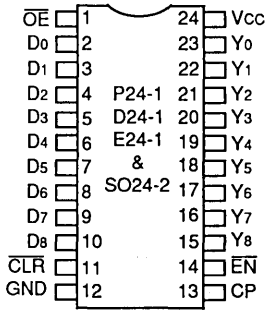
LCC
TOP VIEW

LOGIC SYMBOLS

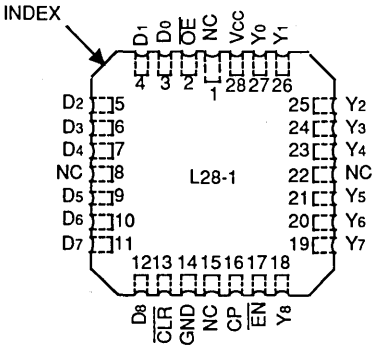


2567 cnv* 02

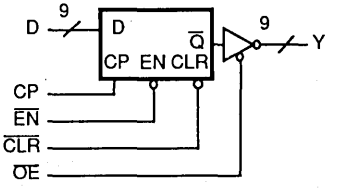
IDT54/74FCT823T 9-BIT REGISTER



DIP/SOIC/CERPACK
TOP VIEW

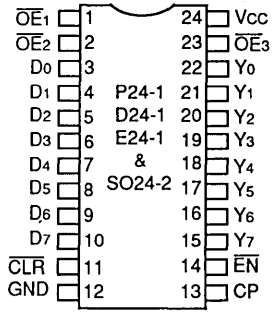


LCC
TOP VIEW

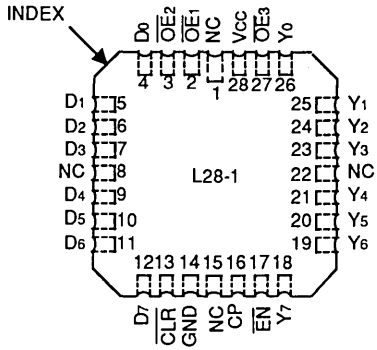


2567 cnv* 03

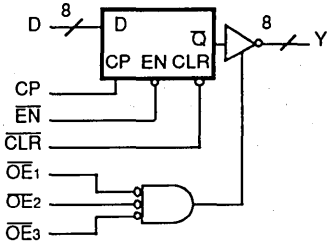
IDT54/74FCT825T 8-BIT REGISTER



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW



2567 cnv* 04

6

PIN DESCRIPTION

Names	I/O	Description
D_I	I	The D flip-flop data inputs.
$\overline{CLR}$	I	When the clear input is LOW and $\overline{OE}$ is LOW, the Q_I outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_I	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_I input is transferred to the Q_I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_I outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_I outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_I outputs.

2567 tbl 02

FUNCTION TABLE[1]

Inputs					Internal/ Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	Function
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE: 2567 tbl 03

1. H = HIGH
   L = LOW
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition
   Z = HIGH-impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2567 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2567 tbl 05

1. This parameter is measured at characterization but not tested.

PRODUCT SELECTOR GUIDE

Device		
10-Bit	9-Bit	8-Bit
54/74FCT821AT/BT/CT	54/74FCT823AT/BT/CT	54/74FCT825AT/BT/CT

2567 tbl 01

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:
2567 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = $\overline{EN}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0	mA
		$\overline{OE}$ = $\overline{EN}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	4.0	7.8[5]	
		$\overline{OE}$ = $\overline{EN}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

NOTES:

2567 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions[1]	IDT54/74FCT821AT-825AT				IDT54/74FCT821BT-825BT				IDT54/74FCT821CT-825CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Y i ($\overline{OE}$ = LOW)	CL = 50pF RL = 500Ω	—	10.0	—	11.5	—	7.5	—	8.5	—	6.0	—	7.0	ns
		CL = 300pF[3] RL = 500Ω	—	20.0	—	20.0	—	15.0	—	16.0	—	12.5	—	13.5	
tSU	Set-up Time HIGH or LOW D i to CP	CL = 50pF RL = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW D i to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW $\overline{EN}$ to CP		4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $\overline{EN}$ to CP		2.0	—	2.0	—	0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, $\overline{CLR}$ to Yi		—	14.0	—	15.0	—	9.0	—	9.5	—	8.0	—	8.5	ns
tREM	Recovery Time $\overline{CLR}$ to CP		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	$\overline{CLR}$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to Yi	CL = 50pF RL = 500Ω	—	12.0	—	13.0	—	8.0	—	9.0	—	7.0	—	8.0	ns
		CL = 300pF[3] RL = 500Ω	—	23.0	—	25.0	—	15.0	—	16.0	—	12.5	—	13.5	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Yi	CL = 5pF[3] RL = 500Ω	—	7.0	—	8.0	—	6.5	—	7.0	—	6.2	—	6.2	ns
		CL = 50pF RL = 500Ω	—	8.0	—	9.0	—	7.5	—	8.0	—	6.5	—	6.5	

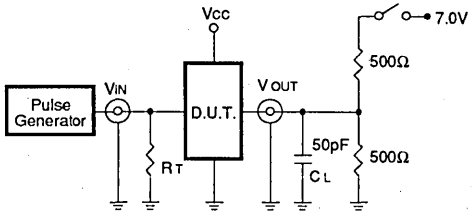
NOTES:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This paramter is guaranteed but not tested.

2567 tbl 09

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



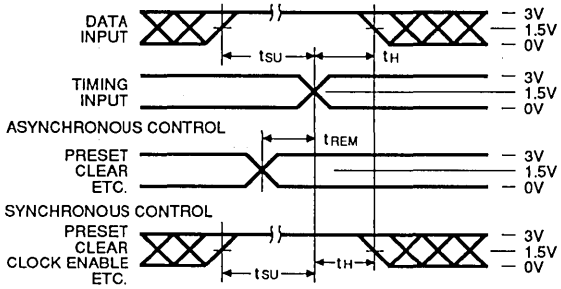
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

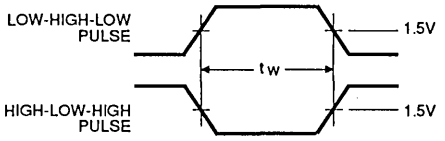
DEFINITIONS: 2567 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

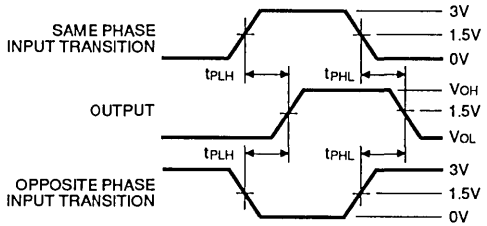
SET-UP, HOLD AND RELEASE TIMES



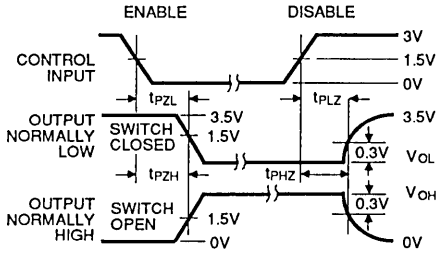
PULSE WIDTH



PROPAGATION DELAY



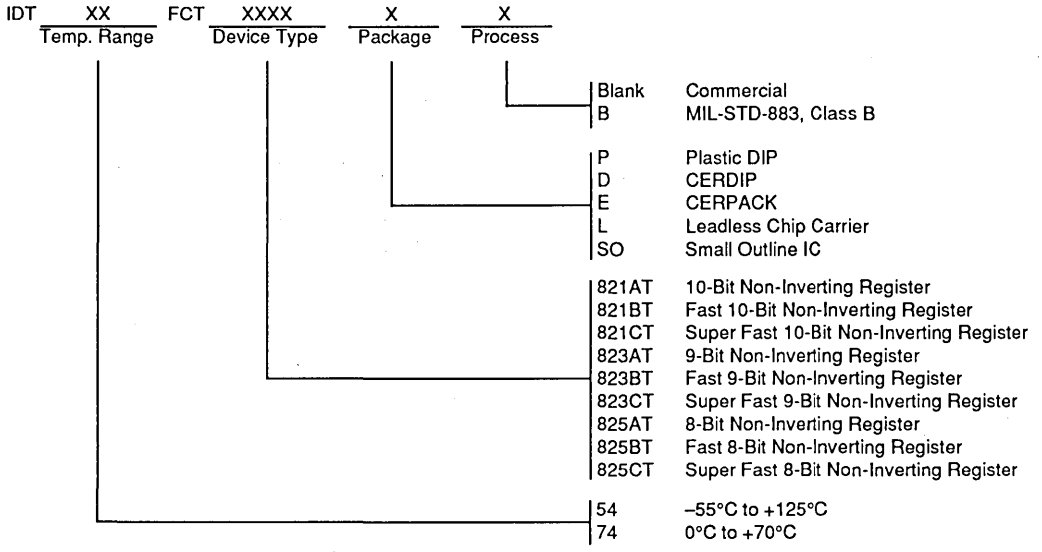
ENABLE AND DISABLE TIMES



NOTES 2567 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2567 cnv* 10

6

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUFFERS

IDT54/74FCT827AT/BT/CT
IDT54/74FCT828AT/BT/CT

FEATURES:

- **Faster than AMD's Am29827-28 series**
- Equivalent to AMD's Am29827-28 bipolar buffers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- IDT54/74FCT827/828AT equivalent to FAST™ speed
- **IDT54/74FCT827/828BT 35% faster than FAST™**
- **IDT54/74FCT827/828CT 45% faster than FAST™**
- I_{OL} = 48mA (commercial), and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- True TTL input and output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

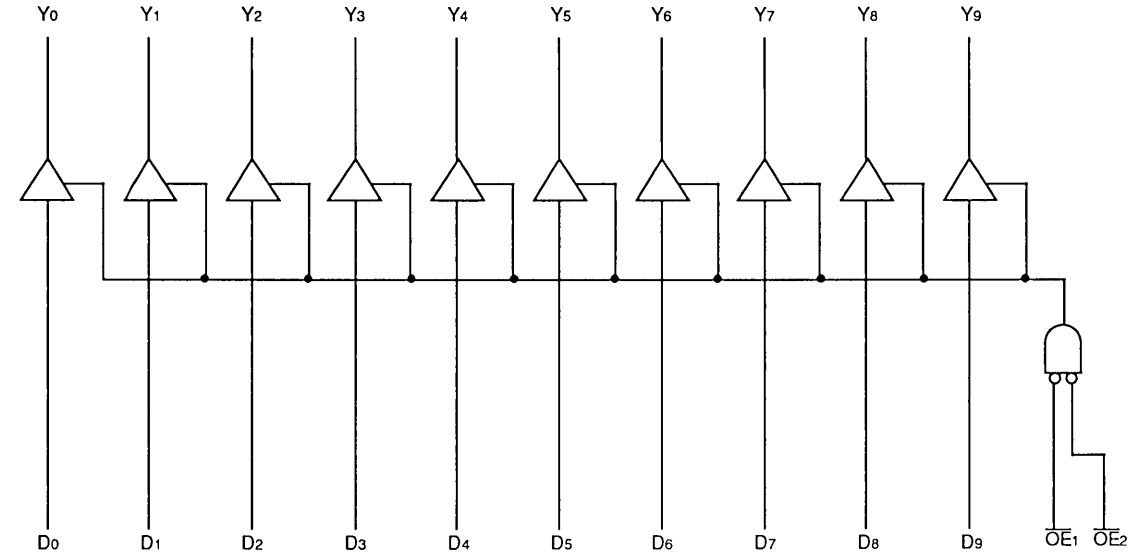
The IDT54/74FCT800AT/BT/CT series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT827AT/BT/CT and IDT54/74FCT828-AT/BT/CT 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high impedance state.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT827AT/BT/CT/828AT/BT/CT 10-BIT BUFFERS



2573 cnv* 01

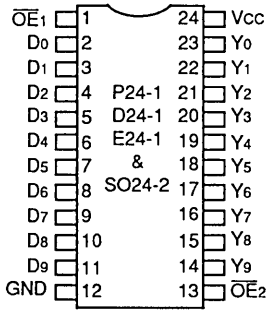
PRODUCT SELECTOR GUIDE

	10-Bit Buffer
Non-inverting	IDT54/74FCT827AT/BT/CT
Inverting	IDT54/74FCT828AT/BT/CT

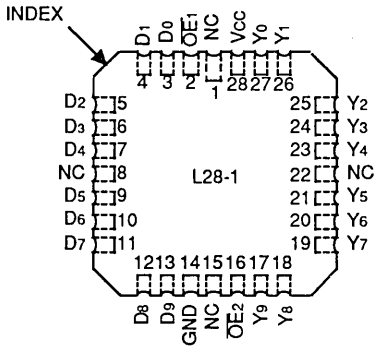
2573 tbl 01

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

PIN CONFIGURATIONS

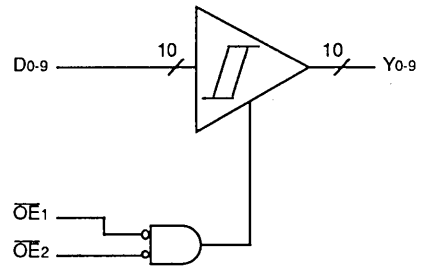


DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



2573 cnv* 02-04

PIN DESCRIPTION

Names	I/O	Description
$\overline{OE}_I$	I	When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

2573 tbl 02

FUNCTION TABLES

IDT54/74FCT827AT/BT/CT (NON-INVERTING)(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High-Impedance

2573 tbl 03

IDT54/74FCT828AT/BT/CT (INVERTING)(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High-Impedance

2573 tbl 04

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2573 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2573 tbl 06

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = −55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	Vcc = Max.	V_I = 0.5V	—	—	−5	µA
I_{OZH}	High Impedance Output Current	Vcc = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	−10	
I_I	Input HIGH Current	Vcc = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		−60	−120	−225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL. I_{OH} = −8mA COM'L.	2.4	3.3	—	V
			I_{OH} = −12mA MIL. I_{OH} = −15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	Vcc = Max. V_{IN} = GND or Vcc		—	0.2	1.5	mA

NOTES: 2573 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_1$ = $\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}_1$ = $\overline{OE}_2$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}_1$ = $\overline{OE}_2$ = GND Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

NOTES:

2573 tbl 08

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	IDT54/74FCT827AT-828AT				IDT54/74FCT827BT-828BT				IDT54/74FCT827CT-828CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	—	8.0	—	9.0	—	5.0	—	6.5	—	4.4	—	5.0	ns
	IDT54/74FCT827T (Non-inverting)	CL = 300pF[3] RL = 500Ω	—	15.0	—	17.0	—	13.0	—	14.0	—	10.0	—	11.0	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	—	9.0	—	10.0	—	5.5	—	6.5	—	4.4	—	5.0	ns
	IDT54/74FCT828T (Inverting)	CL = 300pF[3] RL = 500Ω	—	14.0	—	16.0	—	13.0	—	14.0	—	10.0	—	11.0	
tPZH tPZL	Output Enable Time $\overline{OE}$I to YI	CL = 50pF RL = 500Ω	—	12.0	—	13.0	—	8.0	—	9.0	—	7.0	—	8.0	ns
		CL = 300pF[3] RL = 500Ω	—	23.0	—	25.0	—	15.0	—	16.0	—	14.0	—	15.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$I to YI	CL = 5pF[3] RL = 500Ω	—	9.0	—	9.0	—	6.0	—	7.0	—	5.7	—	6.7	ns
		CL = 50pF RL = 500Ω	—	10.0	—	10.0	—	7.0	—	8.0	—	6.0	—	7.0	

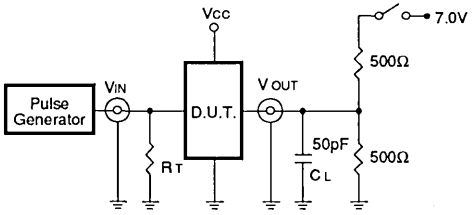
NOTES:

2573 tbl 10

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



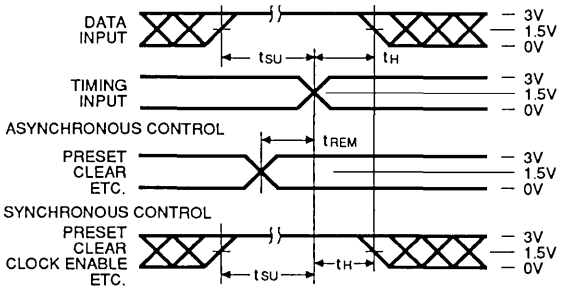
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

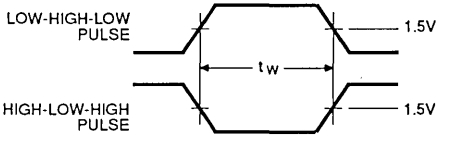
DEFINITIONS: 2573 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

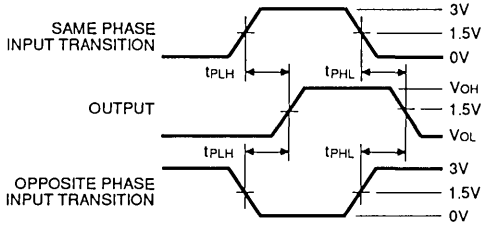
SET-UP, HOLD AND RELEASE TIMES



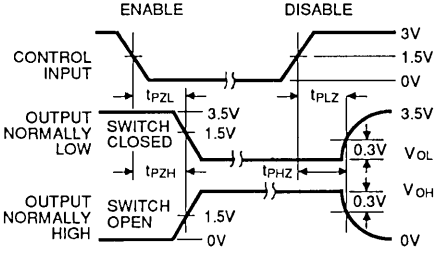
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

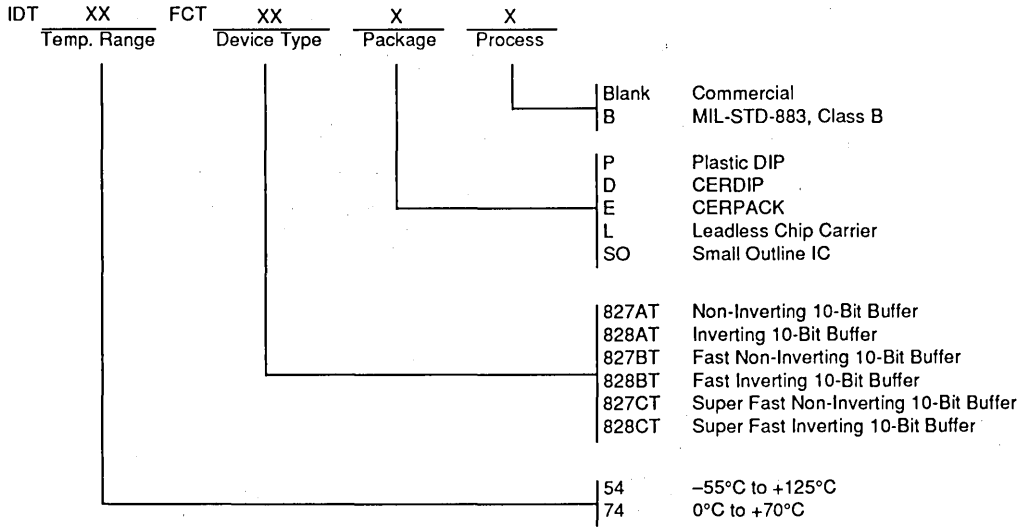


NOTES 2573 drw 11

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2573 cnv* 10

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT54/74FCT841AT/BT/CT
IDT54/74FCT843AT/BT/CT
IDT54/74FCT845AT/BT/CT

FEATURES:

- IDT54/74FCT841AT/843AT/845AT equivalent to FAST™ speed
- **IDT54/74FCT841BT/843BT/845BT up to 30% faster than FAST™**
- **IDT54/74FCT841CT/843CT/845CT up to 50% faster than FAST™**
- TRUE TTL input and output compatible
  - V_{OH} = 3.3V (typ)
  - V_{OL} = 0.3V (typ).
- Equivalent to AMD's Am29841-45 bipolar registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meet or exceed JEDEC Standard 18 specifications

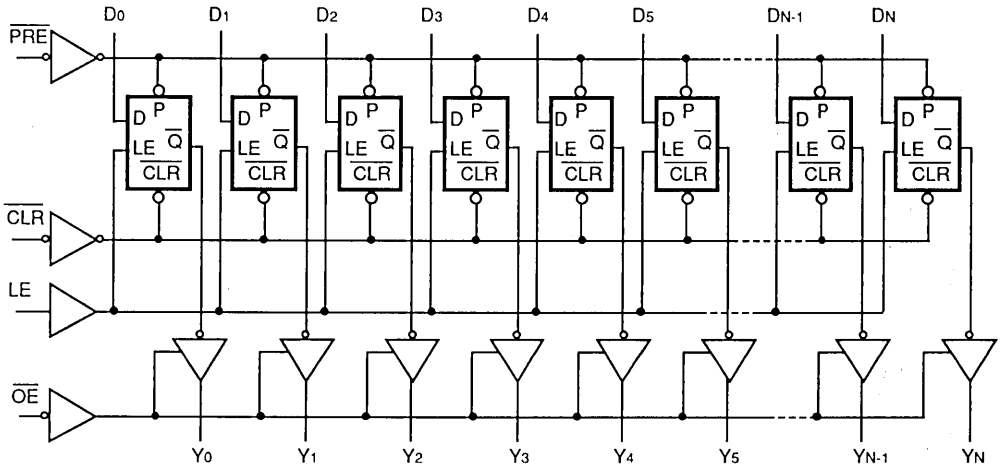
DESCRIPTION:

The IDT54/74FCT800AT/BT/CT series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841AT/BT/CT are buffered, 10-bit wide versions of the popular '373 function. The IDT54/74FCT843AT/BT/CT are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance systems. The IDT54/74FCT845AT/BT/CT are 8-bit buffered latches with all the '843 controls, plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high impedance state.

FUNCTIONAL BLOCK DIAGRAM



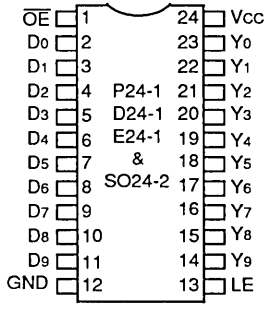
PRODUCT SELECTOR GUIDE

Device		
10-Bit	9-Bit	8-Bit
IDT54/74FCT841 AT/BT/CT	IDT54/74FCT843 AT/BT/CT	IDT54/74FCT845 AT/BT/CT

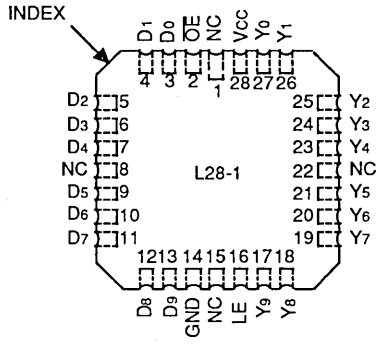
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS

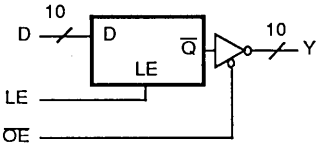
IDT54/74FCT841T 10-BIT LATCH



DIP/CERPACK/SOIC
TOP VIEW

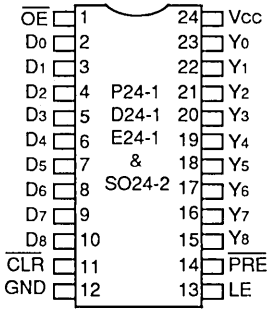


LCC
TOP VIEW

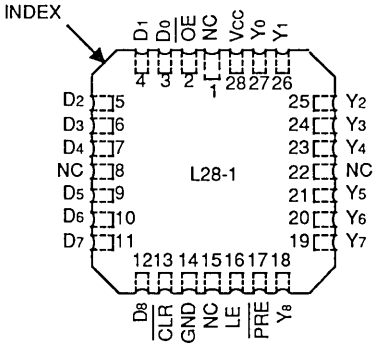


2571 cnv* 02,03,08

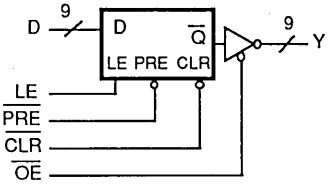
IDT54/74FCT843T 9-BIT LATCH



DIP/CERPACK/SOIC
TOP VIEW

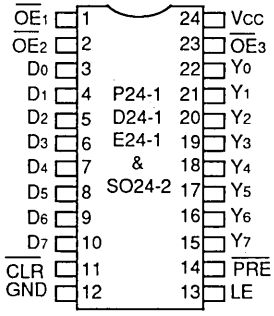


LCC
TOP VIEW

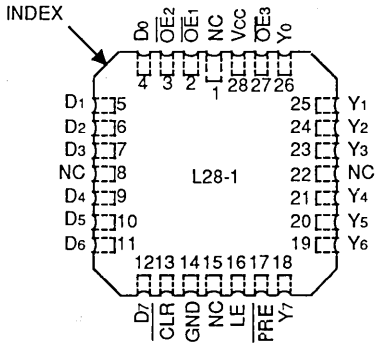


2571 cnv* 04,05,09

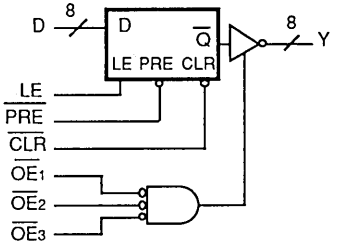
IDT54/74FCT845T 8-BIT LATCH



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



2571 cnv* 06,07,10

PIN DESCRIPTION

Name	I/O	Description
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
DI	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
YI	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y I are in high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

2571 tbl 02

FUNCTION TABLE[1]

Inputs					Inter-nal	Output	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	DI	QI	YI	Function
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE: 2571 tbl 03
1. H = HIGH, L = LOW, X = Don't Care, NC = No Charge, Z = High-Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
VTERM[3]	Terminal Voltage with Respect to GND	–0.5 to VCC	–0.5 to VCC	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTE: 2571 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE: 2571 tbl 05
1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	−5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	−10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		−60	−120	−225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL. I_{OH} = −8mA COM'L.	2.4	3.3	—	V
			I_{OH} = −12mA MIL. I_{OH} = −15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2571 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = Vcc One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = Vcc One Bit Toggling	V_{IN} = Vcc V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	1.7 2.0	4.0 5.0	mA
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = Vcc Eight Bits Toggling	V_{IN} = Vcc V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	3.2 5.2	6.5[5] 14.5[5]	

2571 tbl 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

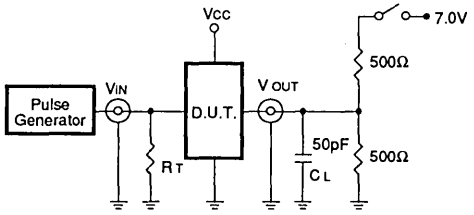
Symbol	Parameter		Test Conditions[1]	IDT54/74FCT841AT-845AT				IDT54/74FCT841BT-845BT				IDT54/74FCT841CT-845CT				Unit
				Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)		CL = 50pF RL = 500Ω	—	9.0	—	10.0	—	6.5	—	7.5	—	5.5	—	6.3	ns
			CL = 300pF[3] RL = 500Ω	—	13.0	—	15.0	—	13.0	—	15.0	—	13.0	—	15.0	
tSU	Data to LE Set-up Time		CL = 50pF	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Data to LE Hold Time		RL = 500Ω	2.5	—	3.0	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tPLH tPHL	Propagation Delay LE to YI		CL = 50pF RL = 500Ω	—	12.0	—	13.0	—	8.0	—	10.5	—	6.4	—	6.8	ns
			CL = 300pF[3] RL = 500Ω	—	16.0	—	20.0	—	15.5	—	18.0	—	15.0	—	16.0	
tPLH	Propagation Delay, $\overline{PRE}$ to YI		CL = 50pF	—	12.0	—	14.0	—	8.0	—	10.0	—	7.0	—	9.0	ns
tREM	Recovery Time $\overline{PRE}$ to YI		RL = 500Ω	—	14.0	—	17.0	—	10.0	—	13.0	—	9.0	—	12.0	ns
tPHL	Propagation Delay, $\overline{CLR}$ to YI			—	13.0	—	14.0	—	10.0	—	11.0	—	9.0	—	10.0	ns
tREM	Recovery Time $\overline{CLR}$ to YI			—	14.0	—	17.0	—	10.0	—	10.0	—	9.0	—	9.0	ns
tW	LE Pulse Width[3]	HIGH		4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tW	$\overline{PRE}$ Pulse Width[3]	LOW		5.0	—	7.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tW	$\overline{CLR}$ Pulse Width[3]	LOW		4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI		CL = 50pF RL = 500Ω	—	11.5	—	13.0	—	8.0	—	8.5	—	6.5	—	7.3	ns
			CL = 300pF[3] RL = 500Ω	—	23.0	—	25.0	—	14.0	—	15.0	—	12.0	—	13.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI		CL = 5pF[3] RL = 500Ω	—	7.0	—	9.0	—	6.0	—	6.5	—	5.7	—	6.0	ns
			CL = 50pF RL = 500Ω	—	8.0	—	10.0	—	7.0	—	7.5	—	6.0	—	6.3	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

2571 tbl 09

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



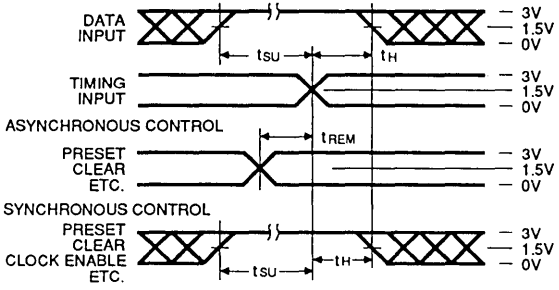
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

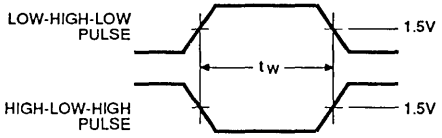
DEFINITIONS: 2571 tbl 10

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

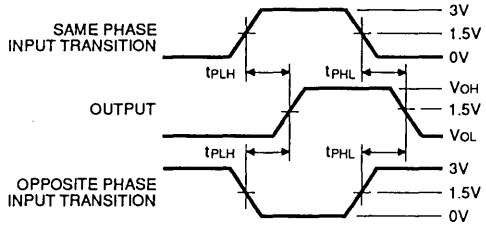
SET-UP, HOLD AND RELEASE TIMES



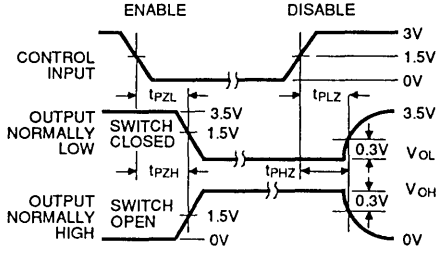
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

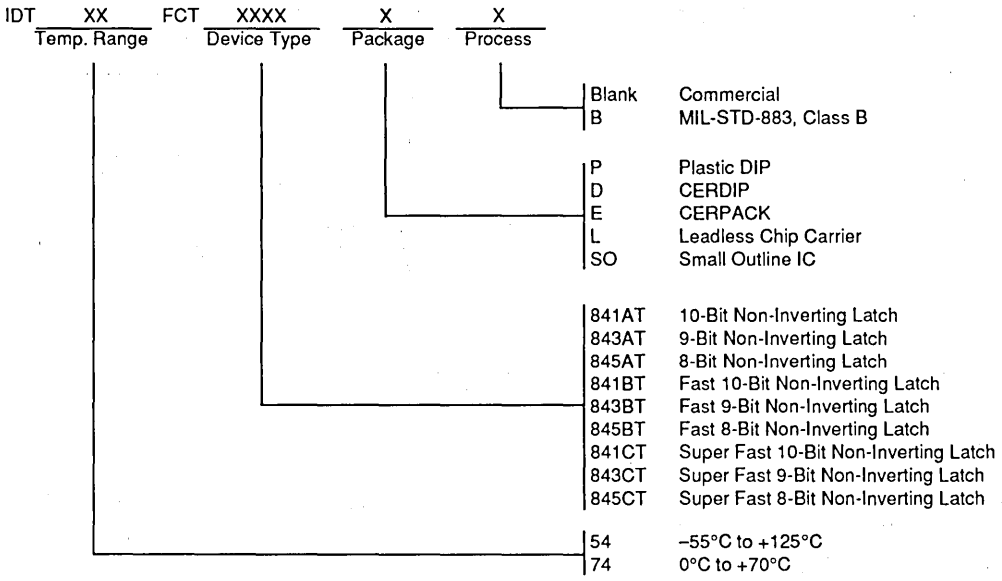


NOTES 2571 drw 11

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tF ≤ 2.5ns; tR ≤ 2.5ns.

6

ORDERING INFORMATION



2571 cnv* 16

Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTERED TRANSCEIVERS

IDT29FCT52A/B/C
IDT29FCT53A/B/C

FEATURES:

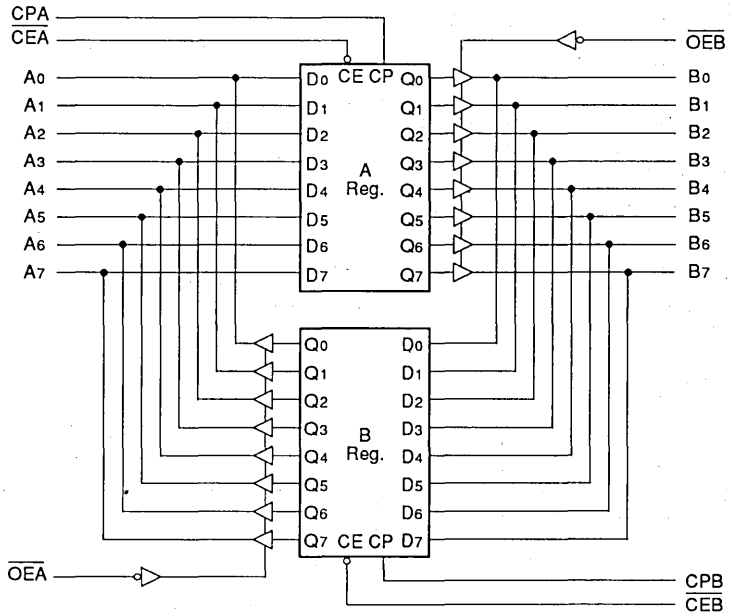
- Equivalent to AMD's Am2952/53 and National's 29F52/53 in pinout/function
- IDT29FCT52A/53A equivalent to FAST™ speed
- **IDT29FCT52B/53B 25% faster than FAST™**
- **IDT29FCT52C/53C 37% faster than FAST™**
- I_{OL} = 64mA (commercial) and 48mA (military)
- I_{IH} and I_{IL} only 5μA max.
- CMOS power levels (2.5mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin DIP, SOIC, 28-pin LCC and PLCC with JEDEC standard pinout
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT52A/B/C and IDT29FCT53A/B/C are 8-bit registered transceivers manufactured using advanced CEMOS™, a dual-metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

The IDT29FCT52A/B/C is a non-inverting option of the IDT29FCT53A/B/C.

FUNCTIONAL BLOCK DIAGRAM[1]



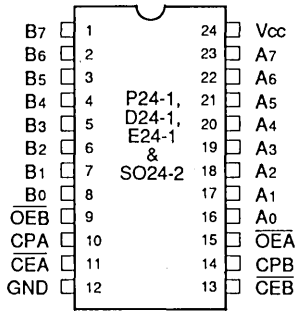
2533 drw 01

NOTE:
1. IDT29FCT52 function is shown.

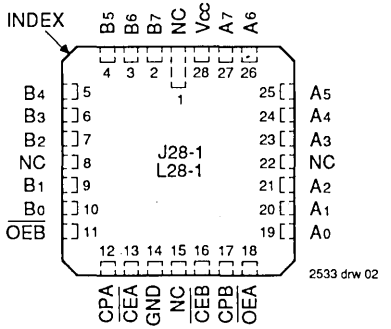
6

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
A_{0-7}	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B_{0-7}	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents, regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the B_{0-7} lines. When $\overline{OEB}$ is HIGH, the B_{0-7} outputs are in the high impedance state.
CPB	I	Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents, regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the A_{0-7} lines. When $\overline{OEA}$ is HIGH, the A_{0-7} outputs are in the high impedance state.

2533 tbl 05

REGISTER FUNCTION TABLE[1]
(Applies to A or B Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

2533 tbl 06

OUTPUT CONTROL[1]

	Internal	Y-Outputs		
$\overline{OE}$	Q	52	53	Function
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

2533 tbl 07

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2533 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2533 tbl 02

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = Vcc – 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	Vcc = Max.	V_I = Vcc	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current (Except I/O Pins)		V_I = 0.5V	—	—	–5(4)	
			V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current (I/O Pins Only)	Vcc = Max.	V_I = Vcc	—	—	15	µA
			V_I = 2.7V	—	—	15(4)	
I_{IL}	Input LOW Current (I/O Pins Only)		V_I = 0.5V	—	—	–15(4)	
			V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	Vcc	—	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	Vcc	—	
			I_{OH} = –15mA MIL.	2.4	4.0	—	
			I_{OH} = –24mA COM'L.	2.4	4.0	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}(4)	
			I_{OL} = 48mA MIL.(5)	—	0.3	0.55	
			I_{OL} = 64mA COM'L.(5)	—	0.3	0.55	

NOTES: 2533 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.5	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OEA}$ or $\overline{OEB}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OEA}$ or $\overline{OEB}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	2.0	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.5	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OEA}$ or $\overline{OEB}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.3	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.5	16.8[5]	

2533 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT29FCT52A/53A				IDT29FCT52B/53B				IDT29FCT52C/53C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CPA, CPB to An, Bn	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	2.0	6.3	2.0	7.3	ns
tPZH tPZL	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to An or Bn		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	1.5	7.0	1.5	8.0	ns
tPHZ tPLZ	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to An or Bn		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	1.5	6.5	1.5	7.5	ns
tSU	Set-up Time HIGH or LOW An, Bn to CPA, CPB		2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Hold Time HIGH or LOW An, Bn to CPA, CPB		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	Pulse Width, HIGH[3] or LOW CPA or CPB		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns

NOTES:

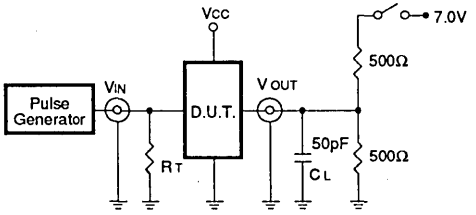
2533 tbl 08

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



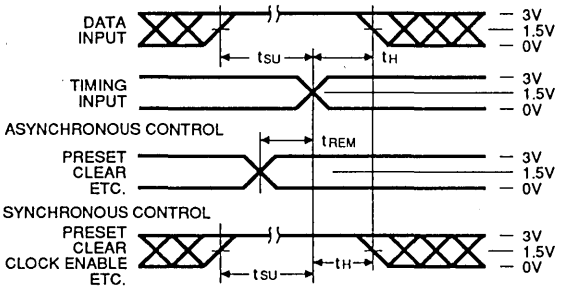
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

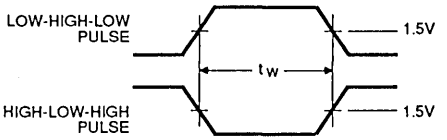
DEFINITIONS: 2533 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

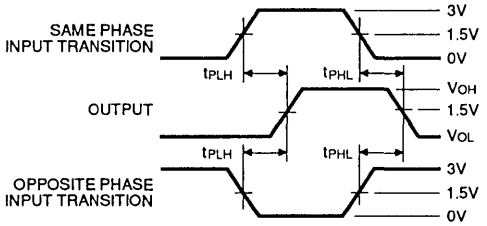
SET-UP, HOLD AND RELEASE TIMES



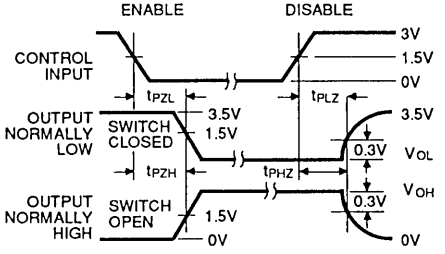
PULSE WIDTH



PROPAGATION DELAY



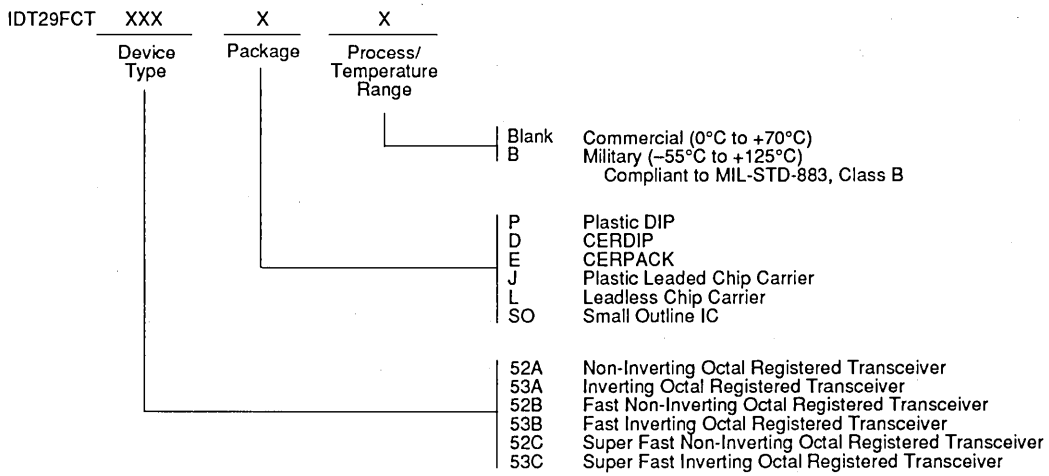
ENABLE AND DISABLE TIMES



NOTES 2533 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2533 drw 03

6

Integrated Device Technology, Inc.

MULTILEVEL PIPELINE REGISTER

IDT29FCT520A
IDT29FCT520B
IDT29FCT520C

FEATURES:

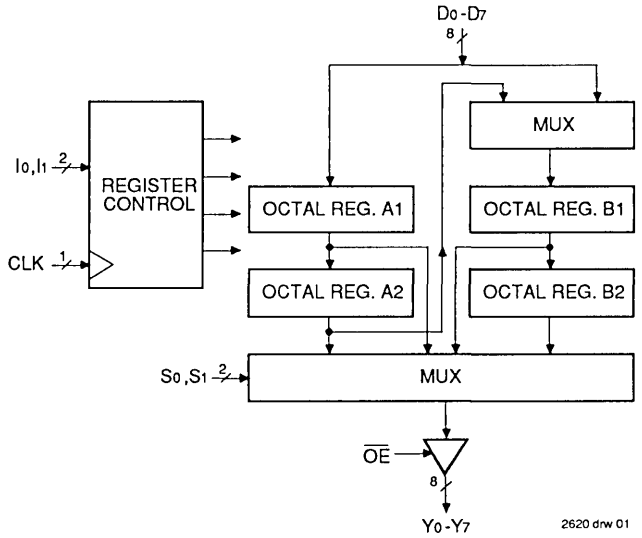
- Equivalent to AMD's Am29520 bipolar Multilevel Pipeline Register in pinout/function, speed and output drive over full temperature and voltage supply extremes
- Four 8-bit high-speed registers
- Dual two-level or single four-level push-only stack operation
- All registers available at multiplexed output
- Hold, transfer and load instructions
- Provides temporary address or data storage
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than AMD's bipolar (5μA typ.)
- TTL input and output level compatible
- CMOS output level compatible
- Manufactured using advanced CEMOS™ processing
- Available in 300 mil plastic and hermetic DIP, as well as LCC, SOIC and CERPACK
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT520A/B/C contains four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

In the IDT29FCT520A/B/C when data is entered into the first level (I = 2 or I = 1), the existing data in the first level is moved to the second level. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0). This transfer also causes the first level to change.

FUNCTIONAL BLOCK DIAGRAM



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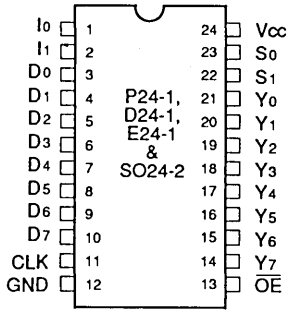
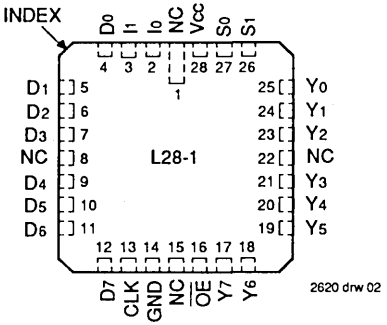
PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

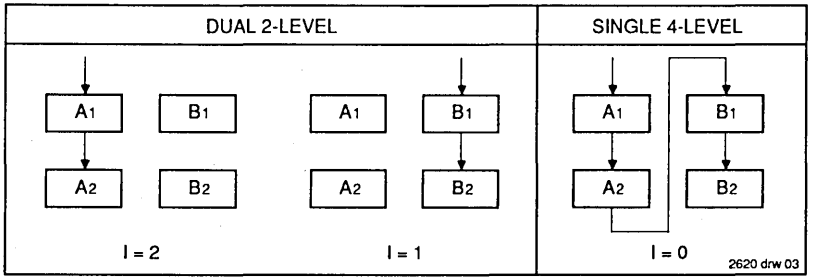
Pin Names	Description
D_n	Register input port.
CLK	Clock input. Enter data into registers on LOW-to-HIGH transitions.
I_0, I_1	Instruction inputs. See Figure 1 and Instruction Control Tables.
S_0, S_1	Multiplexer select. Inputs either register A_1, A_2, B_1 or B_2 data to be available at the output port.
$\overline{OE}$	Output enable for 3-state output port
Y_n	Register output port.

2620 tbl 01

REGISTER SELECTION

S_1	S_0	Register
0	0	B_2
0	1	B_1
1	0	A_2
1	1	A_1

2620 tbl 02



NOTE:
1. I = 3 for hold.

Figure 1. Data Loading in 2-Level Operation

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2620 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2620 tbl 04

1. This parameter is measured at characterization data but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V, V_{HC} = Vcc - 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = Vcc	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	-5(4)	
			V_I = GND	—	—	-5	
I_{OZH}	Off State (High Impedance) Output Current	Vcc = Max.	V_O = Vcc	—	—	10	µA
			V_O = 2.7V	—	—	10(4)	
I_{OZL}			V_O = 0.5V	—	—	-10(4)	
			V_O = GND	—	—	-10	
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	Vcc	—	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	Vcc	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}(4)	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2620 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current, TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		$\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz, 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	7.0	12.8[5]	
		$\overline{OE}$ = GND Eight Bits Toggling at f_i = 5MHz, 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

2620 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at VCC or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL HIgh Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT520A				IDT54/74FCT520B				IDT54/74FCT520C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPHL tPLH	Propagation Delay CLK to Yn	CL = 50pF RL = 500Ω	2.0	14.0	2.0	16.0	2.0	7.5	2.0	8.0	2.0	6.0	2.0	7.0	ns
tPHL tPLH	Propagation Delay S0 or S1 to Yn		2.0	13.0	2.0	15.0	2.0	7.5	2.0	8.0	2.0	6.0	2.0	7.0	ns
tSU	Set-up Time HIGH or LOW Dn to CLK		5.0	—	6.0	—	2.5	—	2.8	—	2.5	—	2.8	—	ns
tH	Hold Time HIGH or LOW Dn to CLK		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tSU	Set-up Time HIGH or LOW I0 or I1 to CLK		5.0	—	6.0	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
tH	Hold Time HIGH or LOW I0 or I1 to CLK		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tPHZ tPLZ	Output Disable Time		1.5	12.0	1.5	13.0	1.5	7.0	1.5	7.5	1.5	6.0	1.5	6.0	ns
tPZH tPZL	Output Enable Time		1.5	15.0	1.5	16.0	1.5	7.5	1.5	8.0	1.5	6.0	1.5	7.0	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	8.0	—	5.5	—	6.0	—	5.5	—	6.0	—	ns

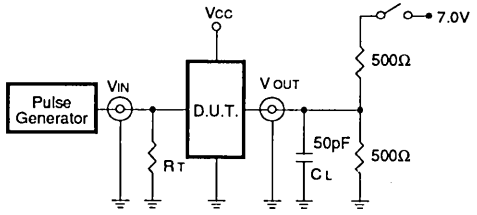
NOTES:

2620 tbl 07

1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

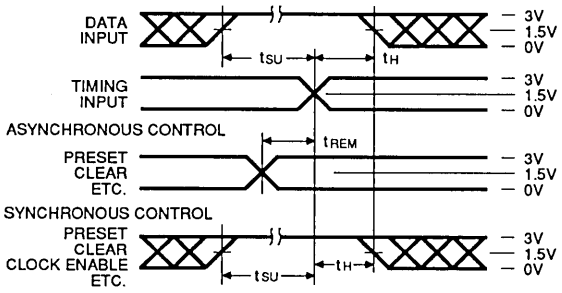
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2620 tbl 08

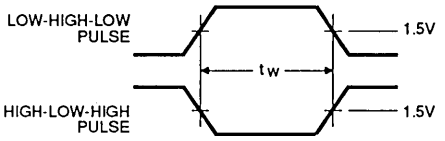
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

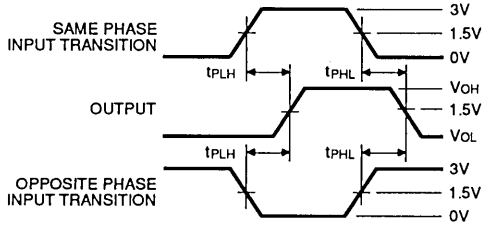
SET-UP, HOLD AND RELEASE TIMES



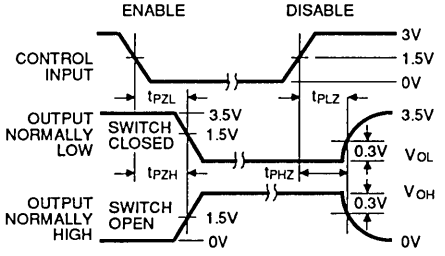
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



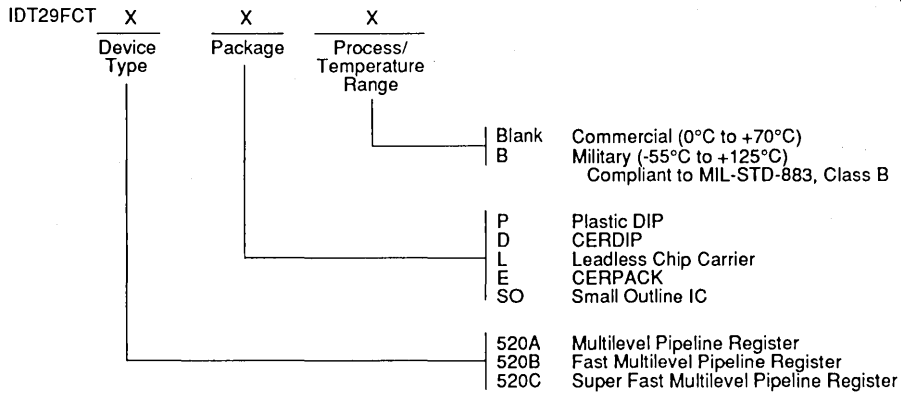
2620 drw 05

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2620 drw 04

Integrated Device Technology, Inc.

HIGH-SPEED 16-BIT SYNCHRONOUS BINARY COUNTER

ADVANCE INFORMATION
IDT49FCT661

FEATURES:

- 16-bit synchronous up/down counter, synchronously programmable
- Maximum frequency of 50MHz commercial
- Clock to Y-bus of 15ns commercial
- Both synchronous and asynchronous clear inputs
- Three-state counter outputs interface directly with bus-organized systems
- Ripple carry output for cascading
- Clocked carry output for convenient modulo configuration
- Latched inputs provide for modulo load function or interface to a processor
- Latched readback path for interface to a processor
- I_{OL} = 48mA commercial and 32mA military
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Available in 48-pin Shrink-DIP, 52-pin PLCC and LCC
- Product Available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

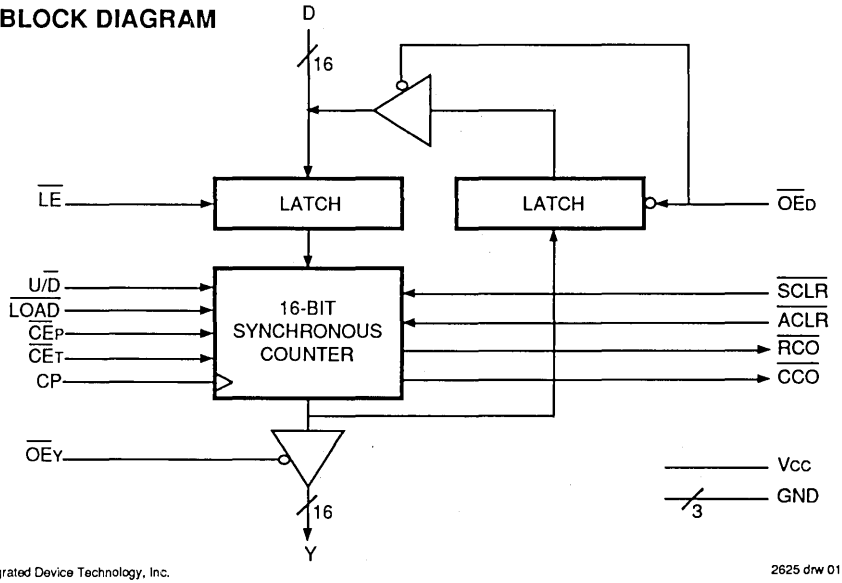
DESCRIPTION:

The IDT49FCT661 is a programmable 16-bit synchronous up/down binary counter which is conveniently organized for operation in a standalone configuration, as well as interfaced with a processor. All operations except latch, output enable and asynchronous clear happen on the rising edge of the Clock Input ($\overline{CP}$).

With a $\overline{LOAD}$ input LOW, the counter will load the value at the output of the input latch. The input latch is transparent when $\overline{LE}$ is LOW, allowing for easy connection to processor address decode and strobe logic. The D-Bus Output Enable ($\overline{OE_D}$) is used for reading back the state of the counter in processor-based applications. When $\overline{OE_D}$ is LOW, the latch is closed and the D bus is driven with the contents of the latch; otherwise the output buffer is in a high-impedance state when $\overline{OE_D}$ is HIGH. Counting is enabled only when $\overline{CE_P}$ and $\overline{CE_T}$ are LOW and $\overline{LOAD}$ is HIGH. The Up/Down Input ($U/\overline{D}$) controls direction of the count. Internal carry look-ahead logic and an active LOW on Ripple Carry Output ($\overline{RCO}$) allow for counting and cascading. During up-count, the $\overline{RCO}$ is LOW at binary 65K and upon down-count is LOW at binary 0. Normal cascade operations require only the $\overline{RCO}$ to be connected to the succeeding block at $\overline{CE_T}$. When counting, the Clock Carry Output ($\overline{CCO}$) provides a HIGH-LOW-HIGH pulse for a duration equal to the clock LOW time of the input clock only when the $\overline{RCO}$ is LOW. Two active LOW resets are available: synchronous clear ($\overline{SCLR}$) and Master Asynchronous Clear ($\overline{ACLR}$). The output control ($\overline{OE_Y}$) input forces the output to high impedance when HIGH, otherwise the Y-bus reflects the output of the counter.

6

FUNCTIONAL BLOCK DIAGRAM



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2625 drw 01

Integrated Device Technology, Inc.

HIGH-SPEED TRI-PORT BUS MULTIPLEXER

PRELIMINARY
IDT49FCT804A
IDT49FCT804C

FEATURES:

- High-speed, 10 bit x 3 port Bus Multiplexer
- Allows bidirectional communication between any 2 ports
- 10 bits provide extra addressing capability
- Latched inputs for asynchronous storage of incoming data
- Controls designed for shared memory applications
- I_{OL} = 48mA (Commercial), 32mA (Military)
- CMOS Power Levels (1mW typ. static)
- TTL input and output level compatible
- Available in DIP, PLCC, LCC and Flatpack
- Military product compliant to MIL-STD-883, Class B
- Product available in Radiation Tolerant and Radiation Enhanced versions

DESCRIPTION:

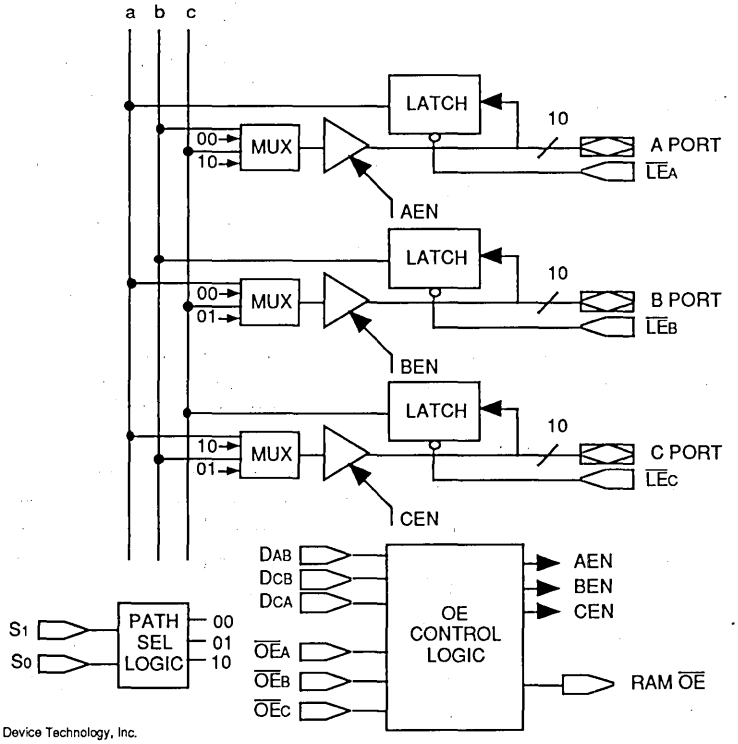
The Busmux is a multiport device intended for inter-bus communication in a multiprocessing, DSP, Array processing or networking environment. It offers significant space savings and performance benefit over discrete implementations of the function.

The architecture consists of 3 I/O ports. The input of each port has a transparent latch controlled by a Latch Enable input ($\overline{LE}$). The output of each latch is connected to an internal bus. The output of each port consists of a multiplexer and a tri-state buffer. The multiplexer will select one of the other two busses under control of Path Select Logic inputs (S_1, S_0).

The direction of signal flow is determined by Direction Control inputs (Dxx). The output enable pins of each port ($\overline{OE}$x) provide independent tri-state control. In addition, when both Path Select Logic inputs (S_1, S_0) are high, all three ports are in a high impedance state.

For shared memory applications the device is configured to use ports A and C for 2 system busses and port B for the shared memory bus. The RAM output enable (RAM $\overline{OE}$) output is asserted when the signal path is from B to A or B to C. It is disasserted under all other conditions.

FUNCTIONAL BLOCK DIAGRAM



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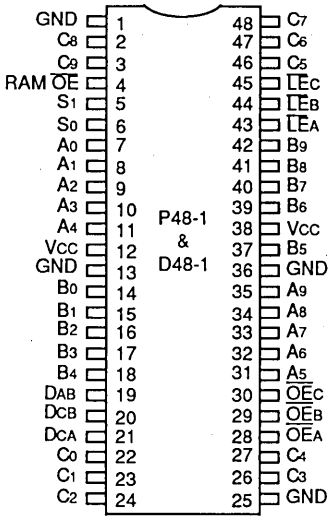
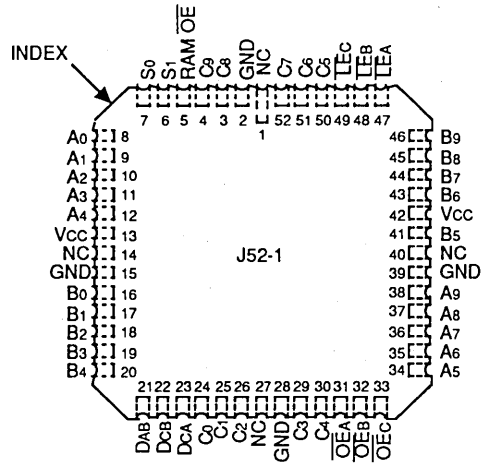
2622 drw 01

PIN CONFIGURATIONS



DIP
TOP VIEW

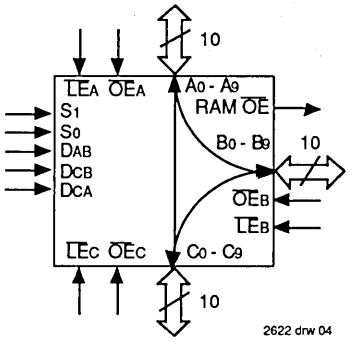
2622 drw 02



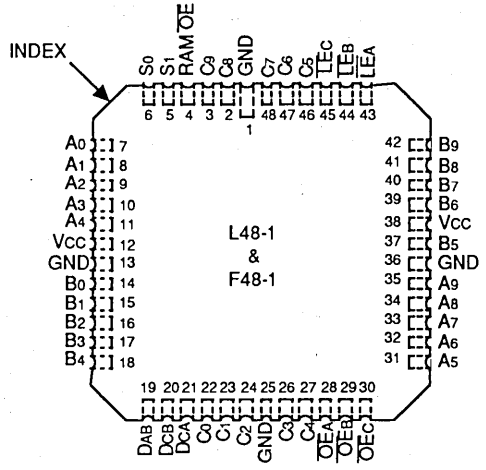
PLCC
TOP VIEW

2622 drw 03

LOGIC SYMBOL



2622 drw 04



PLCC
TOP VIEW

2622 drw 05

6

PIN DESCRIPTION

Name	Type	Description
A_0 - A_9	I/O	A port I/O
B_0 - B_9	I/O	B port I/O
C_0 - C_9	I/O	C port I/O
RAM $\overline{OE}$	O	Asserted (LOW) when B to A or B to C paths are enabled
$\overline{LE_A}$	I	Active low enable for A port input latch
$\overline{LE_B}$	I	Active low enable for B port input latch
$\overline{LE_C}$	I	Active low enable for C port input latch
S_0 - S_1	I	Path selection inputs
DAB	I	Direction control for AB path
DCB	I	Direction control for CB path
DCA	I	Direction control for CA path
$\overline{OE_A}$	I	Output enable control for A port
$\overline{OE_B}$	I	Output enable control for B port
$\overline{OE_C}$	I	Output enable control for C port
GND 1-3	PWR	One ground for each port (Noisy ground)
GND 4	PWR	Signal ground (Quiet ground)
VCC 1-2	PWR	+5V power supply

2622 tbl 01

FUNCTION TABLE – BUS CONTROL

$\overline{OE}$ = 0 $\overline{LE}$ = 0								
S_1	S_0	DAB	DCB	DCA	A PORT	B PORT	C PORT	RAM $\overline{OE}$
0	0	0	X	X	O	I	Z	L
0	0	1	X	X	I	O	Z	H
0	1	X	1	X	Z	O	I	H
0	1	X	0	X	Z	I	O	L
1	0	X	X	0	I	Z	O	H
1	0	X	X	1	O	Z	I	H
1	1	X	X	X	Z	Z	Z	H

NOTE: 2622 tbl 02
1. H = HIGH, L = LOW, I = IN, O = Out, Z = High Impedance, X = Don't Care

LATCH OPERATION

$\overline{LE}$	Operation
0	Transparent
1	Port Data Latched

2622 tbl 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2622 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2622 tbl 05
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: TA = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: TA = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	—	—	15	µA
			V_I = 2.7V	—	—	15[4]	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	—	—	–15[4]	
			V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	
V_H	Input Hysteresis	—		—	200	—	mV

NOTES:
2622 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

VLC = 0.2V; VHC = VCC – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_X$ = $\overline{LE}_X$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		50% Duty Cycle $\overline{OE}_X$ = $\overline{LE}_X$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
		50% Duty Cycle $\overline{OE}_X$ = $\overline{LE}_X$ = GND Ten Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	6.5	17.8[5]	

2622 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT49FCT804A				IDT49FCT804C				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPHL tPLH	Propagation Delay Port to Port	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	7.2	1.5	8.2	ns
tPHL tPLH	Propagation Delay $\overline{LE}$x to Port		1.5	12.0	1.5	13.0	1.5	8.7	1.5	10.2	ns
tPHL tPLH	Propagation Delay S0 or S1 to port		1.5	9.5	1.5	10.5	1.5	8.2	1.5	9.2	ns
tPHL tPLH	Propagation Delay S0 or S1 to RAM $\overline{OE}$		1.5	10.5	1.5	11.5	1.5	9.2	1.5	10.2	ns
tPHL tPLH	Propagation Delay Dxx to RAM $\overline{OE}$		1.5	9.0	1.5	10.0	1.5	7.2	1.5	8.2	ns
tPZL tPZH	Output Enable Time Dxx or $\overline{OE}$x to Port[3]		1.5	11.5	1.5	13.0	1.5	8.0	1.5	9.5	ns
tPLZ tPHZ	Output Disable Time Dxx or $\overline{OE}$x to Port[3]		1.5	9.0	1.5	11.0	1.5	7.7	1.5	9.2	ns
tSU	Set-up Time Port Data to $\overline{LE}$x		2.0	—	2.5	—	2.0	—	2.5	—	ns
tH	Hold time Port Data to $\overline{LE}$x		2.0	—	2.5	—	2.0	—	2.5	—	ns
tW	$\overline{LE}$x Pulse Width LOW		6.0	—	6.0	—	6.0	—	6.0	—	ns

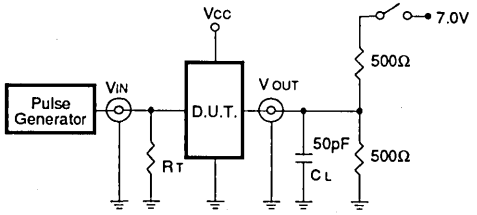
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Dxx to port guaranteed but not tested.

2604 tbl 08

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



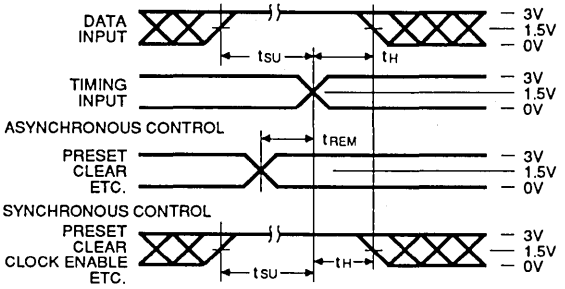
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

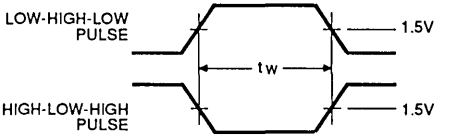
DEFINITIONS: 2622 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

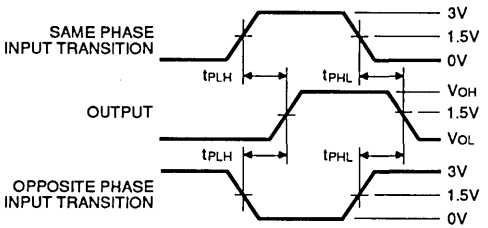
SET-UP, HOLD AND RELEASE TIMES



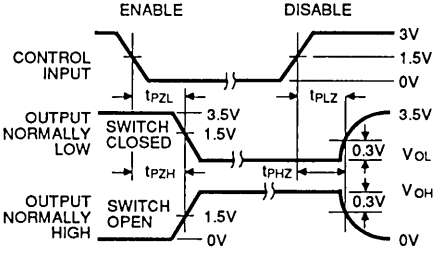
PULSE WIDTH



PROPAGATION DELAY



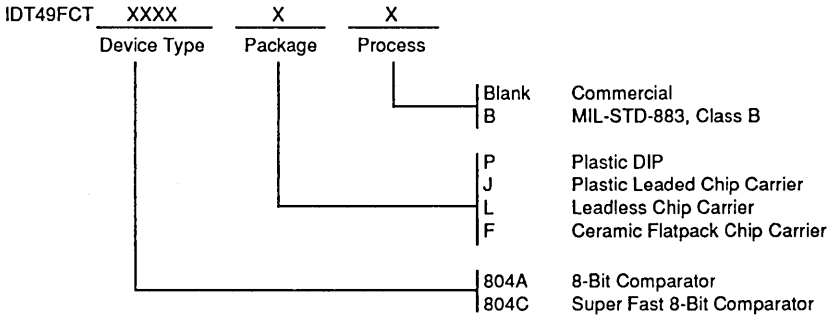
ENABLE AND DISABLE TIMES



NOTES 2622 drw 07

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2622 drw 11

6

Integrated Device Technology, Inc.

FAST CMOS BUFFER/CLOCK DRIVER

PRELIMINARY
IDT49FCT805/A
IDT49FCT806/A

FEATURES

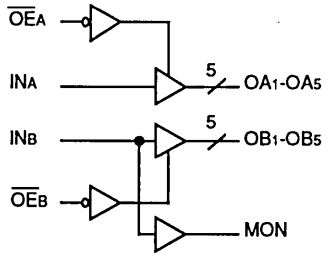
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Two independent groups of buffers with 3-state control 5:1 fanout (1 in - 5 out) per group
- True and inverting options
- 'Heartbeat' monitor output
- Guaranteed low skew
- Pinout designed for minimum skew and ground bounce
- Clock busing with 3-state control
- 20 pin DIP, SOIC, CERPACK and LCC
- Meets or exceeds JEDEC Standard 18 specifications
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

The IDT49FCT805/A and IDT49FCT806/A are clock drivers built using advanced CEMOS™, a dual metal CMOS technology. The IDT49FCT805A is a non-inverting clock driver and the IDT49FCT806A is an inverting clock driver. Each clock driver consists of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible CMOS input.

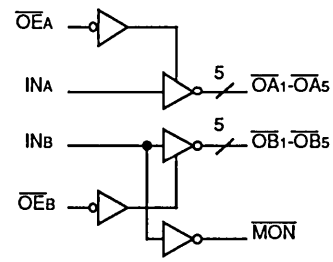
FUNCTIONAL BLOCK DIAGRAMS

IDT49FCT805



2574 drw 03

IDT49FCT806



2574 drw 06

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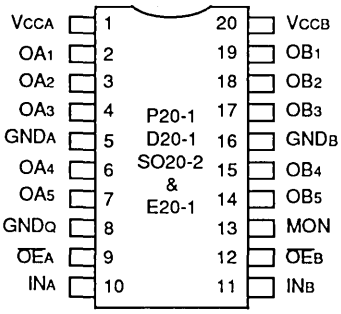
FAST is a trademark of National Semiconductor Co.

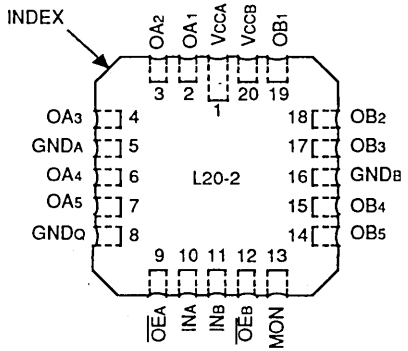
PIN CONFIGURATIONS

IDT49FCT805



DIP/SOIC/CERPACK
TOP VIEW

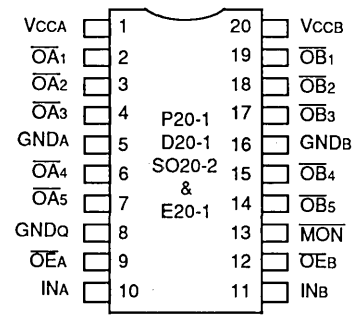
2574 drw 01



LCC
TOP VIEW

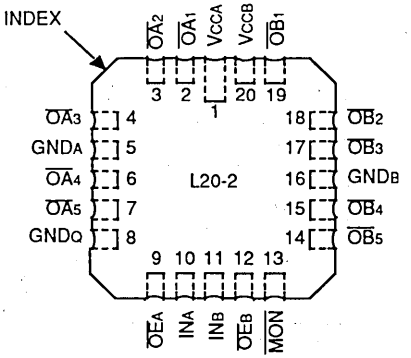
2574 drw 02

IDT49FCT806



DIP/SOIC/CERPACK
TOP VIEW

2574 drw 04



LCC
TOP VIEW

2574 drw 05

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
O_An, O_Bn	Clock Outputs
MON	Monitor Output

2574 tbl 05

FUNCTION TABLE[1]

Inputs		Outputs			
		49FCT805		49FCT806	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	O_An, O_Bn	MON	$\overline{O}_An$, $\overline{O}_Bn$	$\overline{MON}$
L	L	L	L	H	H
L	H	H	H	L	L
H	L	Z	L	Z	H
H	H	Z	H	Z	L

NOTE:
1. H = HIGH, L = LOW, Z = High Impedance

2574 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2574 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2574 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: TA = 0°C to +70°C; VCC = 5.0V ± 5%, Military: TA = –55°C to +125°C; VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = Vcc	—	—	5	µA
I_{IL}	Input LOW Current	Vcc = Max.	V_I = GND	—	—	–5	µA
I_{OZH}	Off State (HIGH Z)	Vcc = Max.	V_O = Vcc	—	—	10	µA
I_{OZL}	Output Current		V_O = GND	—	—	–10	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	3.6	4.3	—	V
			I_{OH} = –24mA MIL. I_{OH} = –24mA COM'L.	2.4	3.8	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis for all inputs	Vcc = 5V		—	200	—	mV

NOTES: 2574 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND Per Output Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f i = 10MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Five Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	7.7	14.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	8.0	15.0	
		V_{CC} = Max. Outputs Open f i = 2.5MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eleven Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	4.3	8.4[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	4.8	10.4[5]	

NOTES:

2574 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_O = Number of Outputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

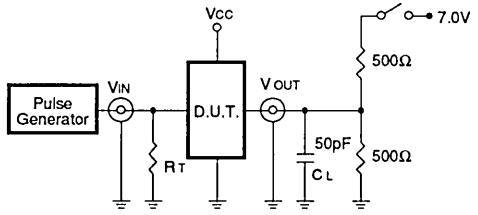
Symbol	Parameter	Condition[1]	IDT49FCT805/806				IDT49FCT805A/806A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay INA to OAn, INB to OBn	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	5.5	1.5	6.0	ns
tPZL tPZH	Output Enable Time $\overline{OE}_A$ to OAn, $\overline{OE}_B$ to OBn		1.5	8.0	1.5	8.5	1.5	8.0	1.5	8.5	ns
tPLZ tPHZ	Output Disable Time $\overline{OE}_A$ to OAn, $\overline{OE}_B$ to OBn		1.5	7.0	1.5	7.5	1.5	7.0	1.5	7.5	ns
Tskew(o)[3]	Skew between two outputs of same package (same transition)		—	0.5	—	0.6	—	0.5	—	0.6	ns
Tskew(t)[3]	Skew between opposite transitions (tPHL-tPLH) of same output		—	0.6	—	0.7	—	0.6	—	0.7	ns
Tskew(p)[3]	Skew between two outputs of different package at same temerature (same transition)		—	1.0	—	1.2	—	1.0	—	1.2	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse case temperature (max. temp.).

2574 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



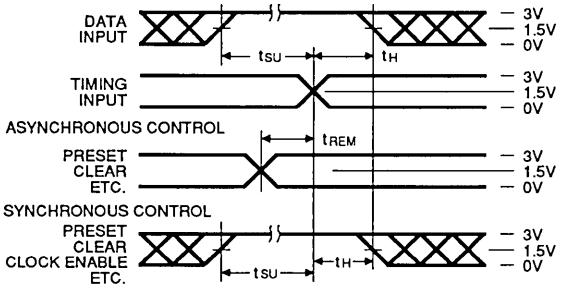
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

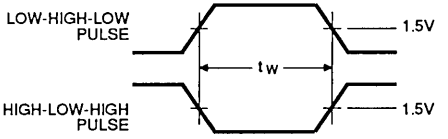
DEFINITIONS: 2574 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

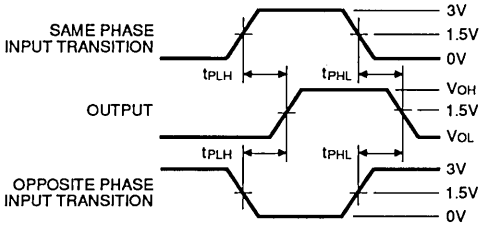
SET-UP, HOLD AND RELEASE TIMES



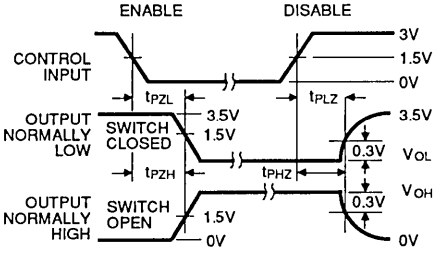
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

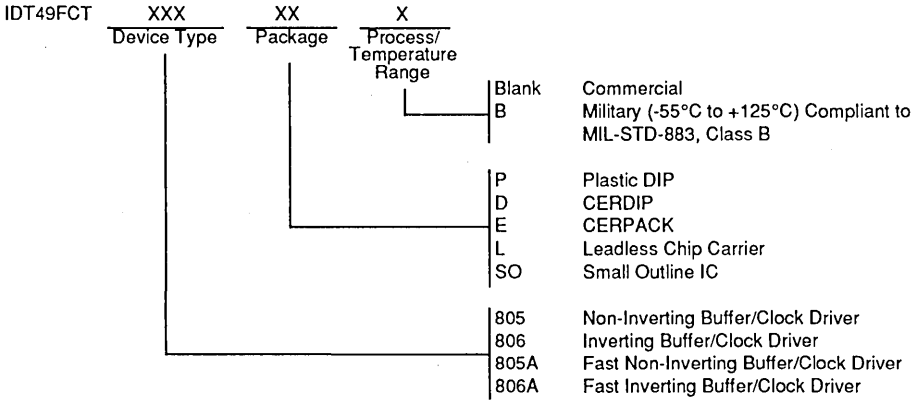


NOTES 2574 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2574 drw 07

Integrated Device Technology, Inc.

HIGH-SPEED OCTAL REGISTER WITH SPC™

PRELIMINARY
IDT49FCT818
IDT49FCT818A

FEATURES:

- High-speed, non-inverting 8 bit parallel register for any data path, control path or pipelining application
- New, unique command capability which allows for multiplicity of diagnostic functions
- High-speed Serial Protocol Channel (SPC™) provides
  - Controllability:
    - Serially scan in new machine state
    - Load new machine state "on the fly"
    - Temporarily force Y output bus
    - Temporarily force data out the D input bus (as in loading WCS)
  - Observability:
    - Directly observe D and Y buses
    - Serially scan out current machine state
    - Capture machine state "on the fly"
- I_{OL} = 32mA (commercial) and 24mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than 29818 and 54/74AS818 (5µA max.)
- Available in plastic and sidebraze DIP, SOIC, LCC and CERPACK
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

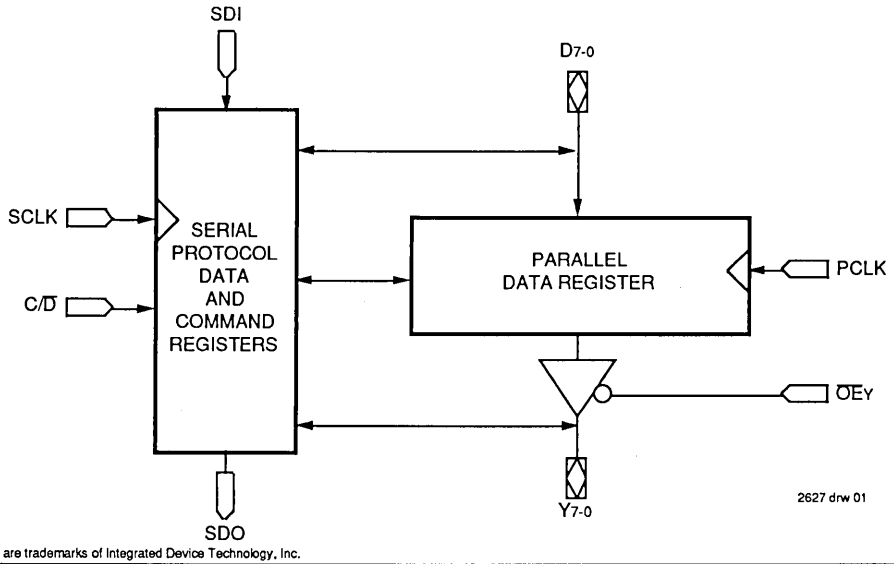
The IDT49FCT818 is a high-speed, general purpose octal register with Serial Protocol Channel (SPC). The D-to-Y path of the octal register provides a data path that is designed for normal system operation wherever a high-speed clocked register is required.

The SPC command and data registers are used to observe and control the octal data register for diagnostic purposes. The SPC command and data registers can be accessed while the system is performing normal system function. Diagnostic operations can then be performed "on the fly", synchronous with the system clock, or can be performed in the "single step" environment. The SPC port utilizes serial data in and out pins (a concept originated at IBM) which can participate in a serial scan loop throughout the system. Here normal data, address, status and control registers are replaced with the IDT49FCT818. The loop can be used to scan in a complete test routine starting point (data, address, etc). Then, after a specified number of clock cycles, the data can be clocked out and compared with expected results.

As well as diagnostic operations, SPC can be used for initializing at power-on time functions such as Writable Control Store (WCS).

6

FUNCTIONAL BLOCK DIAGRAM



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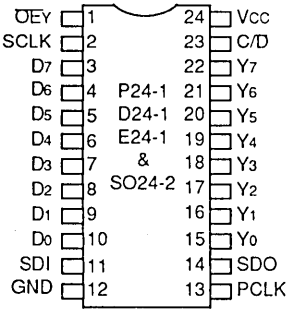
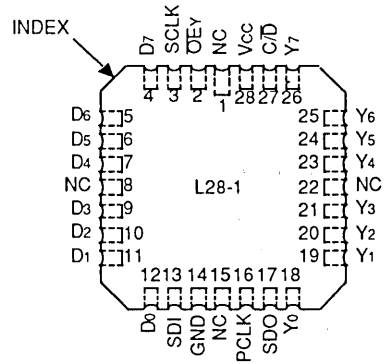
PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

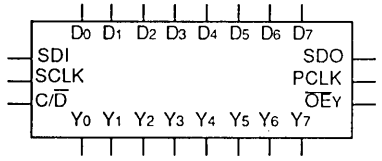
2627 drw 02



LCC
TOP VIEW

2627 drw 03

LOGIC SYMBOL



2627 drw 04

FUNCTION TABLE(1)

C/D	SCLK	PCLK	OEY	D	Y	Function
X	X	X	H	X	High Z	Tri-state Y
X	X	∫	L	H	H	Clock D to Y
X	X	∫	L	L	L	Clock D to Y
H	∫	X	X	X	X	Shift Bit into SPC Command Register
L	∫	X	X	X	X	Shift Bit into SPC Data Register
↯	∫	H or L (Static)	X	X	X	Excute SPC Command during time Between C/D & SCLK

NOTES: 2627 tbl 01

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't care
   Z = High Impedance
   ↯ = Transition, High-to-Low or Low-to-High

PIN DESCRIPTION

Pin Names	I/O	Description
PCLK	I	Parallel Data Register Clock
D7-0	I/O	Parallel Data Register Input Pins (D0 = LSB, D7 = MSB)
Y7-0	I/O	Parallel Data Register Output Pins (Y0 = LSB, Y7 = MSB)
OEY	I	Output Enable for Y Bus (Overidden by SPC Inst. 8 and 14)
SDI	I	Serial Data In for SPC Operation, Data and Command Shifts in the Least Significant Bit First
SDO	O	Serial Data Out for SPC Operation, Data and Command Shifts Out the Least Significant Bit First
C/D	I	Mode Control for SPC
SCLK	I	Serial Shift Clock for SPC Operations

2627tbl02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2627 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2627 tbl 04
1. This parameter is guaranteed by characterization and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = Vcc − 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = −55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	Vcc = Max.	V_I = Vcc	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	−5(4)	
			V_I = GND	—	—	−5	
I_{IH}	Input HIGH Current (I/O pins only)	Vcc = Max.	V_I = Vcc	—	—	15	µA
			V_I = 2.7V	—	—	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	—	—	−15(4)	
			V_I = GND	—	—	−15	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		−60	−120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = −32µA		V_{HC}	Vcc	—	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300µA	V_{HC}	Vcc	—	
			I_{OH} = −12mA MIL.	2.4	4.3	—	
			I_{OH} = −15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}(4)	
			I_{OL} = 24mA MIL.	—	0.3	0.5	
			I_{OL} = 32mA COM'L.	—	0.3	0.5	

NOTES: 2627 tbl 05
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_Y$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_Y$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		One Bit Toggling at f_i = 5MHz 50% Duty Cycle SCLK = C/$\overline{D}$ = V_{CC} SDI = V_{CC}	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_Y$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
		Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle SCLK = C/$\overline{D}$ = V_{CC} SDI = V_{CC}	V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

NOTES:

2627 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

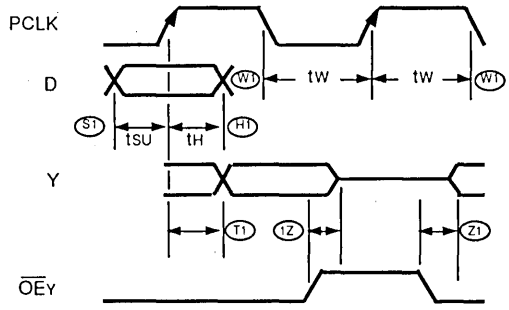
Symbol		Parameter	Condition[1]	IDT54/74FCT818				IDT54/74FCT818A				Unit
				Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPHL	T1	PCLK ≠ to Y	CL = 50pF	3.0	12.5	3.0	14.0	3.0	9.0	3.0	10.0	ns
tPLH	T2	SCLK ≠ to SDO	RL = 500Ω	3.0	20.0	3.0	22.0	3.0	14.0	3.0	15.0	
	T3	SDI to SDO (in stub mode)		3.0	20.0	3.0	22.0	3.0	14.0	3.0	15.0	
	T4	C/D Øto Y (OEY = Low Inst. 8 & 14)		3.0	16.0	3.0	18.0	3.0	13.0	3.0	14.0	
	T5	SCLK ≠ to Y (OEY = Low, Inst. 8 & 14)		3.0	20.0	3.0	22.0	3.0	13.0	3.0	14.0	
	T6	C/D to SDO (Inst. 0, 1, 2 & 4)		3.0	12.5	3.0	14.0	3.0	10.0	3.0	11.0	
tSU	S1	D to PCLK ≠		2.5	—	3.0	—	2.5	—	3.0	—	ns
	S2	C/D to SCLK ≠		12.0	—	14.0	—	12.0	—	14.0	—	
	S3	SDI to SCLK ≠		4.0	—	5.0	—	4.0	—	5.0	—	
	S4	Y or D to C/D Ø (Inst. 0, 2 & 4)		2.0	—	2.5	—	2.0	—	2.5	—	
	S5	C/D (Low) to PCLK ≠ (Inst. 3 & 13)		8.0	—	9.0	—	8.0	—	9.0	—	
	S6	Y to PCLK ≠ (Inst. 3)		1.0	—	1.5	—	1.0	—	1.5	—	
tH	H1	D to PCLK ≠		2.0	—	2.5	—	2.0	—	2.5	—	ns
	H2	C/D to SCLK Ø		12.0	—	14.0	—	12.0	—	14.0	—	
	H3	SDI to SCLK ≠		1.0	—	1.0	—	1.0	—	1.0	—	
	H4	Y or D to C/D Ø (Inst. 0, 2 & 4)		2.0	—	2.5	—	2.0	—	2.5	—	
	H5	SCLK (Low) to PCLK ≠ (Inst. 3 & 13)		2.0	—	2.5	—	2.0	—	2.5	—	
	H6	C/D (Low) to PCLK ≠ (Inst. 3 & 13)		2.0	—	2.5	—	2.0	—	2.5	—	
	H7	Y to PCLK ≠ (Inst. 3)		4.5	—	5.0	—	4.5	—	5.0	—	
tPHZ	1Z	OEY to Y		3.0	10.0	3.0	11.0	3.0	8.0	3.0	9.0	ns
tPLZ	2Z	SCLK ≠ to D (Inst. 5 & 9)		3.0	13.0	3.0	14.0	3.0	10.0	3.0	11.0	
	3Z	C/D ≠ to D (Inst. 5 & 9)		3.0	13.0	3.0	14.0	3.0	10.0	3.0	11.0	
	4Z	SCLK ≠ to Y (OEY = High Inst. 8 & 14)		3.0	13.0	3.0	14.0	3.0	10.0	3.0	11.0	
	5Z	C/D ≠ to Y (OEY = High Inst. 14)		3.0	13.0	3.0	14.0	3.0	10.0	3.0	11.0	
tPZH	Z1	OEY to Y		3.0	11.0	3.0	12.0	3.0	9.0	3.0	10.0	ns
tPZL	Z2	C/D Øto D (Inst. 5 & 9)		3.0	14.0	3.0	15.0	3.0	10.0	3.0	11.0	
	Z3	C/D Øto Y (OEY = High Inst. 14)		3.0	14.0	3.0	15.0	3.0	10.0	3.0	11.0	
tW	W1	PCLK (High & Low)		7.0	—	8.0	—	7.0	—	8.0	—	ns
	W2	SCLK (High & Low)		25.0	—	25.0	—	25.0	—	25.0	—	
	W3	C/D (High)		25.0	—	25.0	—	25.0	—	25.0	—	

NOTES:

2627 tbl 07

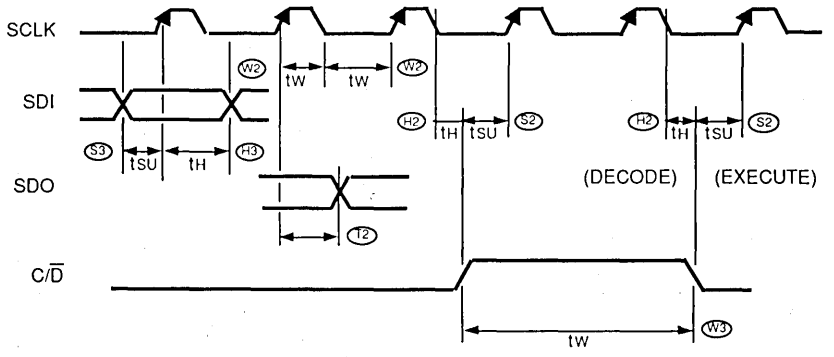
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

GENERAL AC WAVEFORMS FOR PARALLEL INPUTS AND OUTPUTS



2627 drw 05

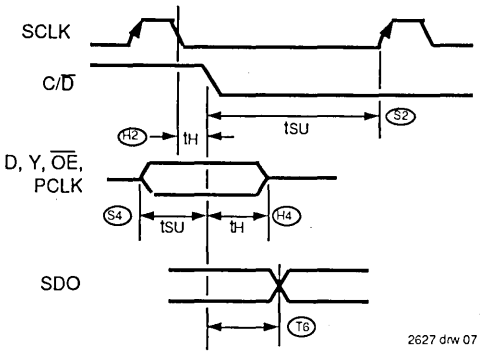
GENERAL AC WAVEFORMS FOR SERIAL PROTOCOL INPUTS AND OUTPUTS



2627 drw 06

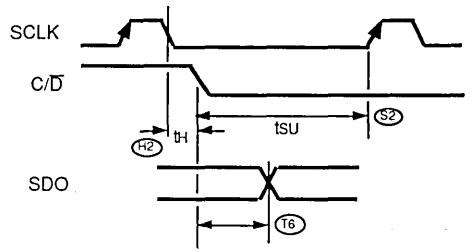
DETAILED WAVEFORMS FOR SERIAL PROTOCOL OPERATIONS

Y ⟶ SPC Data (Inst. 0)
D ⟶ SPC Data (Inst. 2)
Status ⟶ SPC Data (Inst. 4)



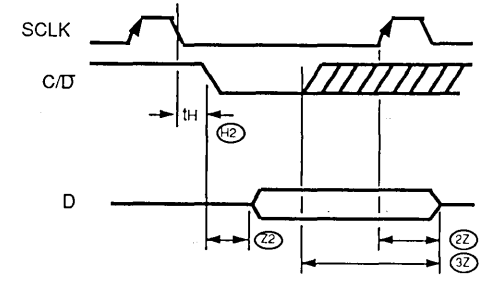
2627 drw 07

PARALLEL DATA REGISTER ⟶ SPC Data (Inst. 1)
SET SERIAL MODE (Inst. 11)
SET STUB MODE (Inst. 12)



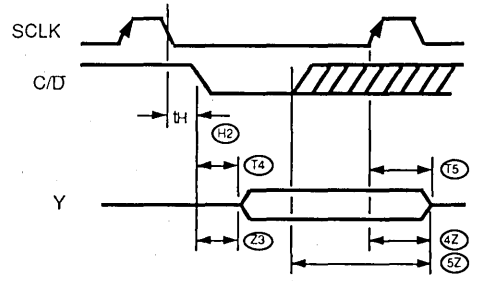
2627 drw 08

CONNECT Y TO D (Inst. 5)
SPC Data ⟶ D (Inst. 9)



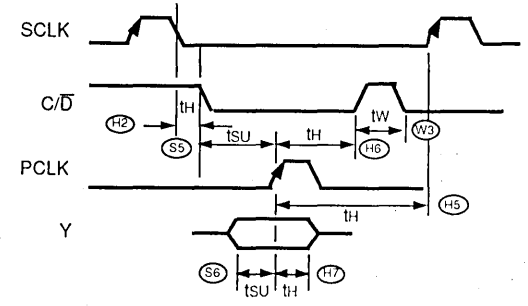
2627 drw 09

SPC Data ⟶ PARALLEL DATA REGISTER (Inst. 10)
SPC Data ⟶ Y (Inst. 8)
CONNECT D TO Y (Inst. 14)



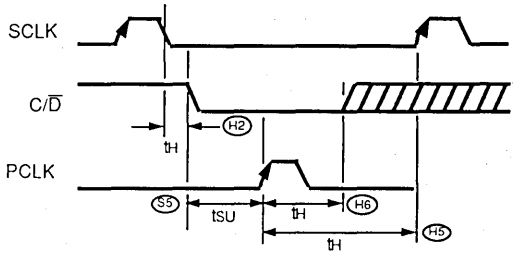
2627 drw 10

Y ⟶ SPC Data SYNCHRONOUS W/PCLK (Inst. 3)



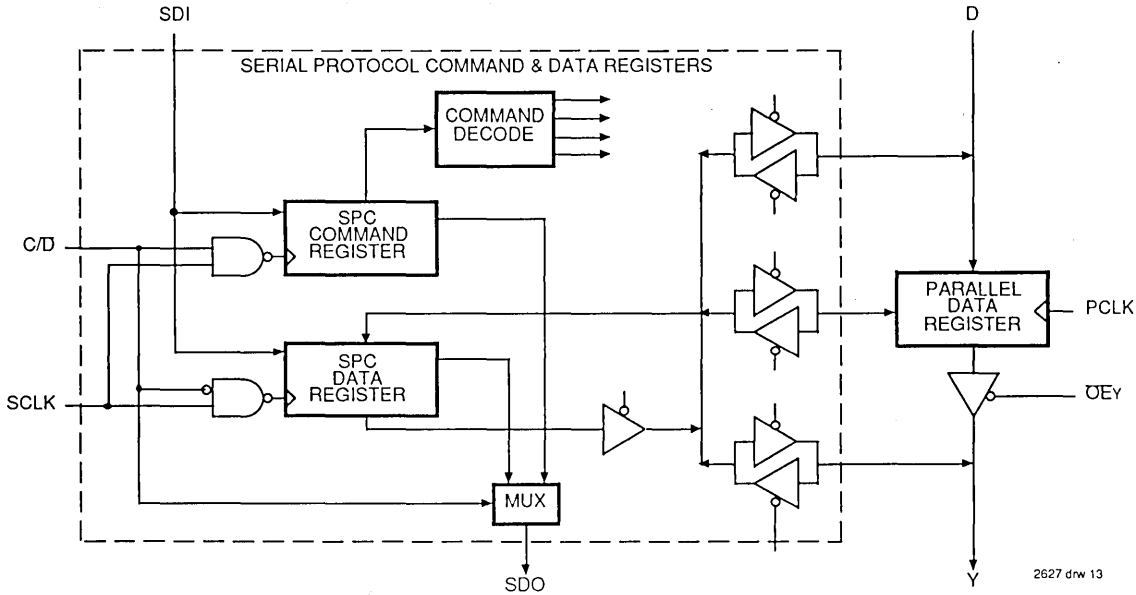
2627 drw 11

SPC Data ⟶ PARALLEL DATA REGISTER SYNCHRONOUS W/ PCLK (Inst. 13)

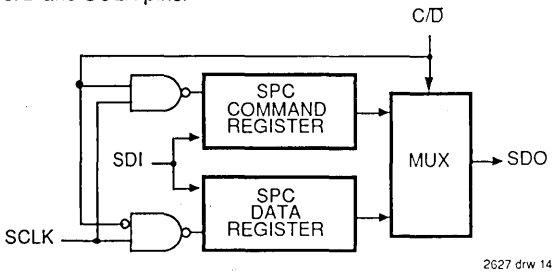


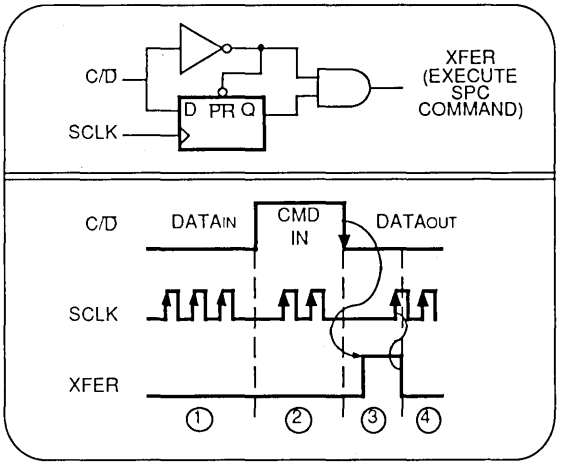
2627 drw 12

DETAILED FUNCTIONAL BLOCK DIAGRAM



The detailed block diagram consists of two main elements: the parallel data register and the SPC data /command registers. The main data path is from the D inputs down to the data register and through the Y outputs. This path is typically used during standard operations. For diagnostic or systems initialization, the internal SPC data path is used. This path allows access between the SPC data and command registers and the standard data path, pins and data register. The SPC data and command registers are accessed via the SDI, SDO, C/$\overline{D}$ and SCLK pins.





SPC FUNCTIONAL DESCRIPTION

The Serial Protocol Channel (SPC) has been optimized for the minimum number of pins and the maximum flexibility. The data is passed in on a Serial Data Input pin (SDI) and out on a Serial Data Output pin (SDO). The transfer of the data is controlled by a Serial Clock (SCLK) and a Command/Data mode input (C/$\overline{D}$). These four pins are the basic SPC pins. To the outside, the SPC appears as two serial shift registers in parallel – one for command and the other data. The serial clock shifts data and the Command/Data (C/$\overline{D}$) line selects which register is being shifted. The command register is used to control loading of data to and from the data register with other storage elements in the device.

With respect to executing an SPC command, there are four distinct phases: (1) data is shifted in, (2) followed by the command, (3) the command is executed, and (4) data is shifted out. During the data mode, data is simultaneously shifted into the serial data register while the data in the register is shifted out. During the command mode, opcode-type information is shifted through the serial ports. The command

is executed when the last bit is shifted in and the C/$\overline{D}$ line is brought LOW. The execution phase is ended with the next serial clock edge.

SPC data and commands are shifted in through the SDI pin, which is a serial input pin, and out through the SDO pin, which is a serial output pin. Data and commands are shifted in Least Significant Bit first; Most Significant Bit last (Y_0 = LSB, Y_7 = MSB). Execution of SPC commands is performed by stopping the shift clock, SCLK, and lowering the C/$\overline{D}$ line from HIGH-to-LOW. Later SCLK may then be transitioned from LOW-to-HIGH. SPC commands and data can be shifted anytime without regard for operation. During the execution phase, care must be taken that there is no conflict between the SPC operation and parallel operation. This means that if the SPC operation attempts to load the parallel data register (opcode 10) while PCLK is in transition, the results are undefined. In general, it is required that PCLK be static during SPC operations. The synchronous commands (opcode 3 and 13), however, allow PCLK to run. In these operations, the HIGH-to-LOW transition of the C/$\overline{D}$ line takes on the function of an arm signal in preparation for the next LOW-to-HIGH transition of PCLK.

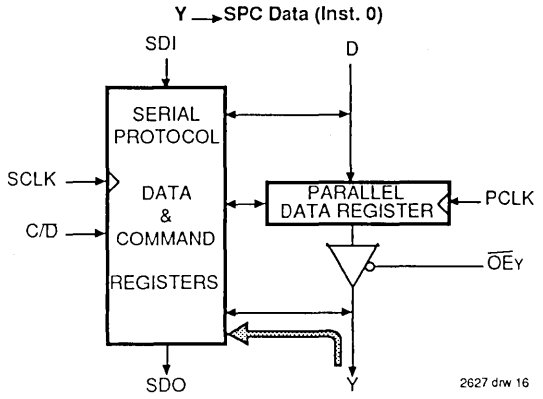
SPC COMMANDS

There are 16 possible SPC opcodes. Fourteen of these are utilized, the other two are reserved and perform NO-OP functions. The top eight opcodes, 0 through 7, are reserved for transferring data into the SPC data register for shifting out. The lower eight opcodes, 8 through 15, are used for transferring data from the SPC data register to other parts of the device. Two of the commands are also used for connecting the data in and out pins.

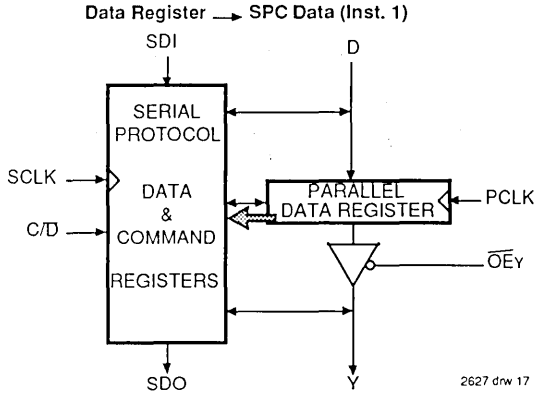
Opcode	SPC Command
0	Y to SPC Data Register
1	Parallel Data Register to SPC Data Register
2	D to SPC Data Register
3	Y to SPC Data Register Synchronous w/PCLK
4	Status ($\overline{OE}_Y$, PCLK) to SPC Data Register
5	Connect Y to D
6-7	Reserved (NO-OP)
8	SPC Data to Y ($\overline{OE}_Y$ is Overidden)
9	SPC Data to D
10	SPC Data to Parallel Data Register
11	Select Serial Mode
12	Select Stub Mode
13	SPC Data to Parallel Data Register Synchronous w/PCLK
14	Connect D to Y ($\overline{OE}_Y$ is Overidden)
15	NO-OP

2627 tbl 08

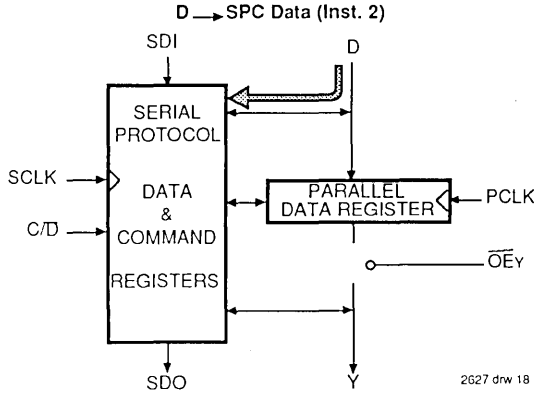
Opcode 0 is used for transferring data from the Y output pins into the SPC data register. Opcode 1 transfers data from the output of the parallel data register, before the tri-state gate, into the SPC data register. Opcode 2 transfers data from the D input pins into the SPC data register.



2627 drw 16



2627 drw 17

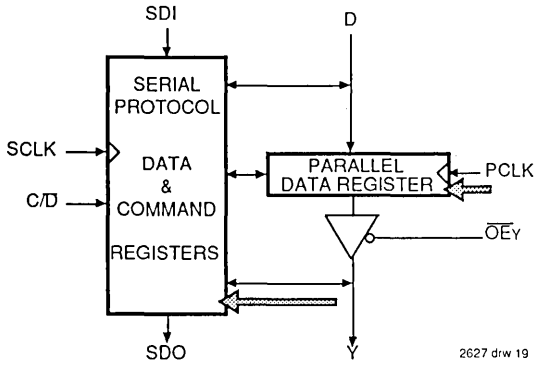


2627 drw 18

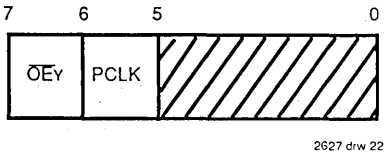
6

Opcode 3 transfers data on the Y pins to the SPC data register on the next PCLK, thus achieving a synchronous observation of the Y data pins in real time. This operation can be forced to repeat without shifting in a new command by pulsing C/$\overline{D}$ LOW-HIGH-LOW after each PCLK. As soon as data is shifted out using SCLK, the command is terminated and must be loaded in again.

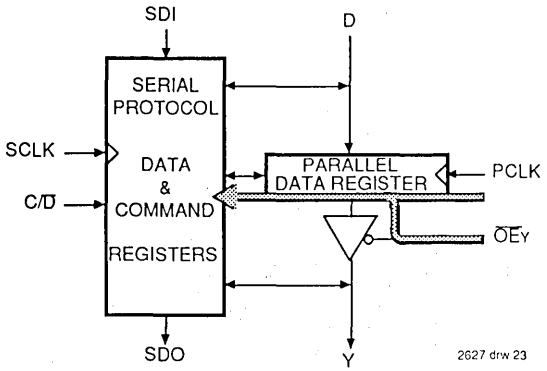
Y ⟶ SPC Data Synchronous w/PCLK (Inst. 3)



Opcode 4 is used for loading status into the SPC data register. The format of bits is shown below.

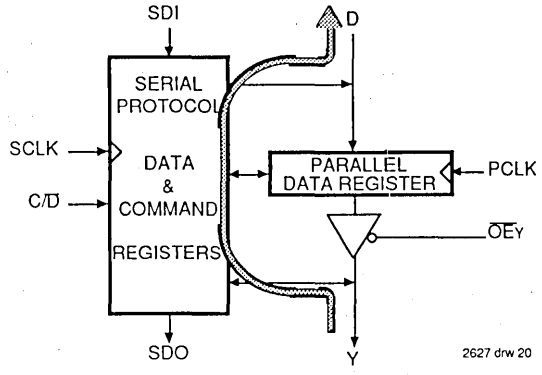


Status ⟶ SPC Data (Inst. 4)

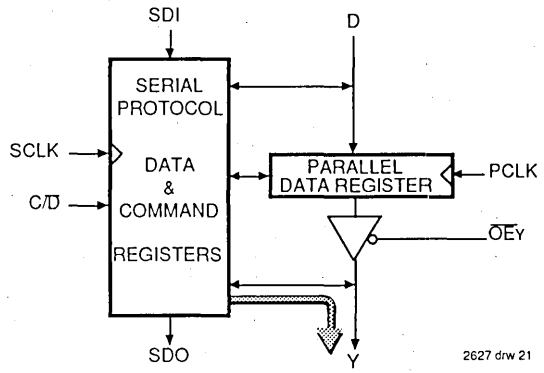


Opcode 5 connects Y to D. Opcodes 6 and 7 are reserved, hence designated NO-OP.

Connect Y to D (Inst. 5)

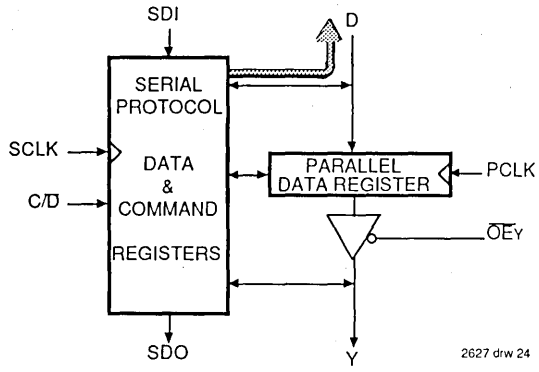


SPC Data ⟶ Y (Inst. 8)



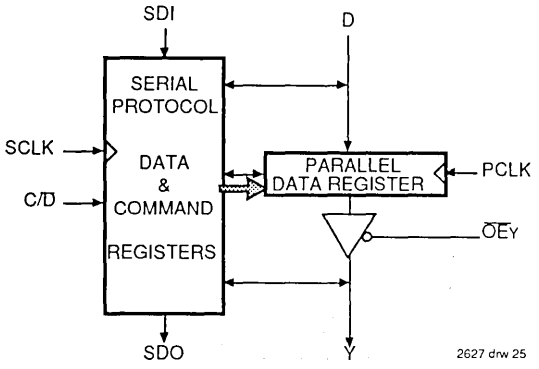
Opcode 8 is used for transferring SPC data directly to the Y pins. When executing opcode 8, the state of $\overline{OE}_Y$ is a "do not care"; that is, data will be output even if $\overline{OE}_Y$ = HIGH. Opcode 9 is used for transferring SPC data to the D pins. Operands 8 and 9 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering C/$\overline{D}$. As soon as SCLK completes its LOW-to-HIGH transition, the command is terminated.

SPC Data ⟶ D (Inst. 9)



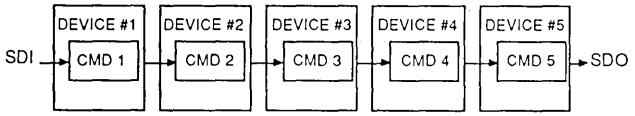
Opcode 10 is used for transferring data from the SPC data register into the parallel data register, irrespective of the state of PCLK. However, PCLK must be static between C/D going HIGH-to-LOW and SCLK going LOW-to-HIGH.

SPC Data ⟶ Parallel Data Register (Inst. 10)



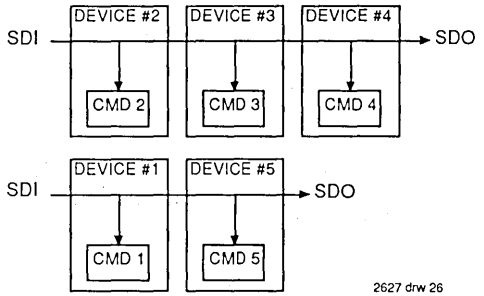
Opcodes 11 and 12 are used to set Serial and Stub Mode, respectively. After executing one of these opcodes, the device remains in this mode until programmed otherwise. The Serial mode is the default mode that the IDT49FCT818 powers up in. In Serial mode, commands are shifted through the SPC command register and then to the SDO pin. This is the typical mode used when several varieties of devices that utilize the SPC access method are employed on one serial ring.

SERIAL MODE



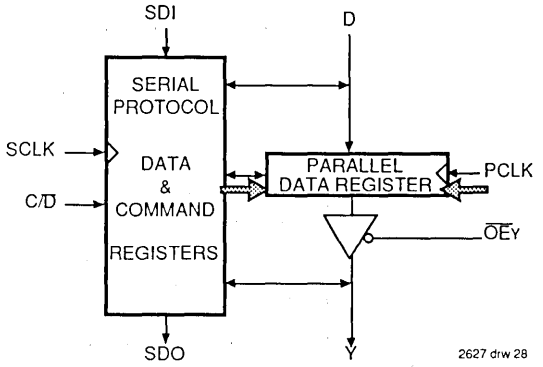
In Stub mode, SDI is connected directly to SDO. In this way, the same diagnostic command can be loaded into multiple devices of like type. For example, in four clock cycles the same command could be loaded into 8 IDT49FCT818s (64-bit pipeline register). Dissimilar devices must be segregated into serial scan loops of similar type, as shown below. During the command phase, the serial shift clock must be slowed down to accommodate the delay from SDI to SDO through all of the devices. The slower clock is typically a small tradeoff compared to the reduced number of clock cycles.

STUB MODE



Opcode 13 transfers data from the SPC data register to the parallel data register on the next PCLK. Opcode 14 connects the D bus to the Y. Operation 14 can be temporarily suspended by raising the C/D input and resumed by lowering the C/D input again. The operation is terminated by SCLK.

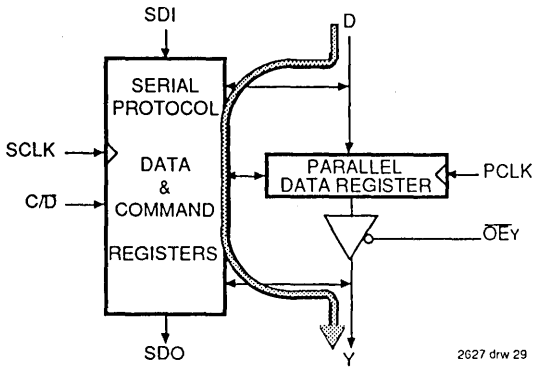
SPC Data ⟶ Parallel Data Register Synchronous w/PCLK (Inst. 13)



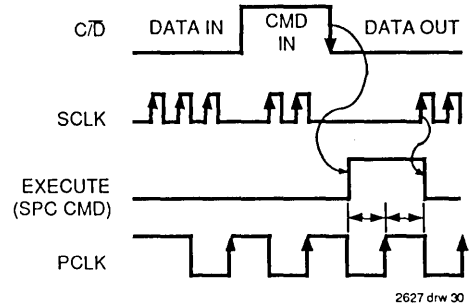
6

Opcodes 3 and 13 transfer data synchronous to PCLK which means that the HIGH-to-LOW on the C/$\overline{D}$ input is an arm signal. The data and command can be shifted in while PCLK is running. The C/$\overline{D}$ line is dropped prior to the desired PCLK edge and raised before the next edge. Instruction 13 can be repeated over many times by leaving the C/$\overline{D}$ line LOW during multiple transitions of PCLK while not clocking SCLK. PCLK cycles can even be skipped by raising the C/$\overline{D}$ input during the desired clock periods. Instruction 3 can be repeated by pulsing C/$\overline{D}$ high after each PCLK. The ability to continuously execute a synchronous command can provide major benefits. For example, the synchronous read (Instruction 3, Y to SPC data) instruction could be clocked into the SPC command register. Then, it could be continuously executed by pulsing the C/$\overline{D}$ line HIGH. When the whole system is stopped (PCLK quiescent), the serial data register will contain the next to the last state of the parallel data register. That value can be shifted out and the current state of the parallel register can then be observed, allowing for the observation of two states of the parallel register (the current and the previous).

Connect D to Y (Inst. 14)

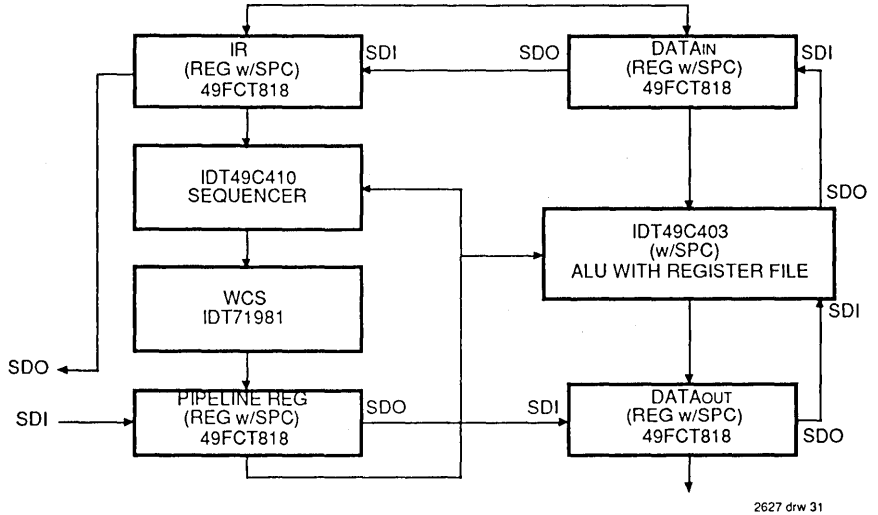


2627 drw 29



2627 drw 30

TYPICAL MICROPROGRAM APPLICATION WITH SPC™



2627 drw 31

TYPICAL APPLICATION

In the block diagram of the typical application, the SPC data register is shown being used with a writable control store in a microprogrammed design. The control store can be initialized through the diagnostic path. The SPC data register is used for the instruction register going into the IDT49C410, as well as for data registers around the IDT49C403. In this way, the designer may use the SPC data register to observe and modify the microcode coming out of the writable control store, as well as observing and being able to modify data and instructions in the overall machine. The IDT49C403 is a 16-bit version of the 2903A/203 which inciudes an SPC port for diagnostic and break point purposes.

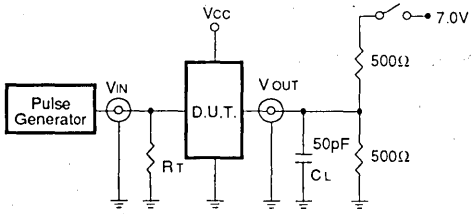
The block diagram of the diagnostics ring shows how devices with diagnostics are hooked together in a serial ring via the SDI and SDO signals. The diagnostics signals may be generated through registers which are hooked up to a microprocessor. This microprocessor could conceivably be an IBM PC.

As companies like IDT continue to integrate more onto each device and put each device into smaller packages such as surface mount devices, the board level testing becomes more complex for the designer and the manufacturing divisions of companies. To help this situation, serial diagnostics was invented. This allows for observation of critical signals deep within the system. During system test when an error is observed, these signals may be modified in order to zero in on the fault in the system.

Serial diagnostics is primarily a scheme utilizing only a few pins (4) to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults. It can be used at many points in the life of a product: design debug and verification, manufacturing test and field service. This document describes a serial diagnostic scheme which was developed at IDT and will be used in future VLSI logic devices designed by IDT.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

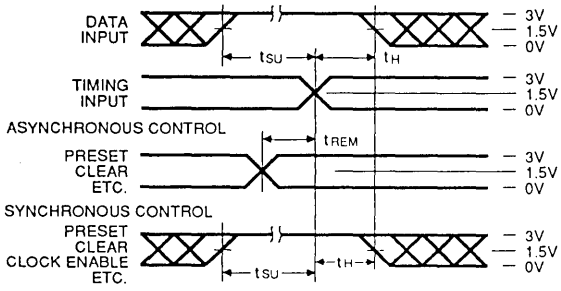
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2627 tbl 08

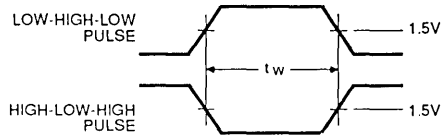
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

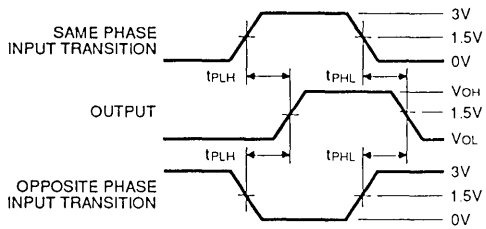
SET-UP, HOLD AND RELEASE TIMES



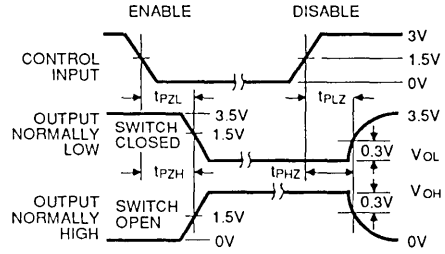
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



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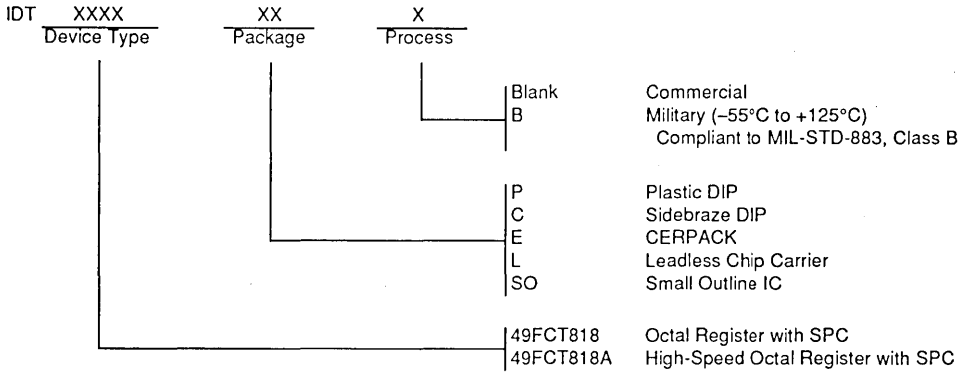
NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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6

Integrated Device Technology, Inc.

CMOS MICROCYCLE LENGTH CONTROLLER

IDT49C25
IDT49C25A

FEATURES:

- Similar function to AMD's Am2925 bipolar controller with improved speeds and output drive over full temperature and voltage supply extremes
- Four microcode-controlled clock outputs allow clock cycle length control for 15 to 30% increase in system throughput. Microcode selects one of eight clock patterns from 3 to 10 oscillator cycles in length
- System controls for $\overline{RUN}/\overline{HALT}$ and Single Step
  — Switch-debounced inputs provide flexible halt controls
- Low input/output capacitance
  — 6pF inputs (typ.)
  — 8pF outputs (typ.)
- CMOS power levels (1mW typ. static)
- Available in 300 mil 24-pin plastic and ceramic THINDIP, 28-pin LCC and PLCC packages and CERPACK
- Both CMOS and TTL output compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

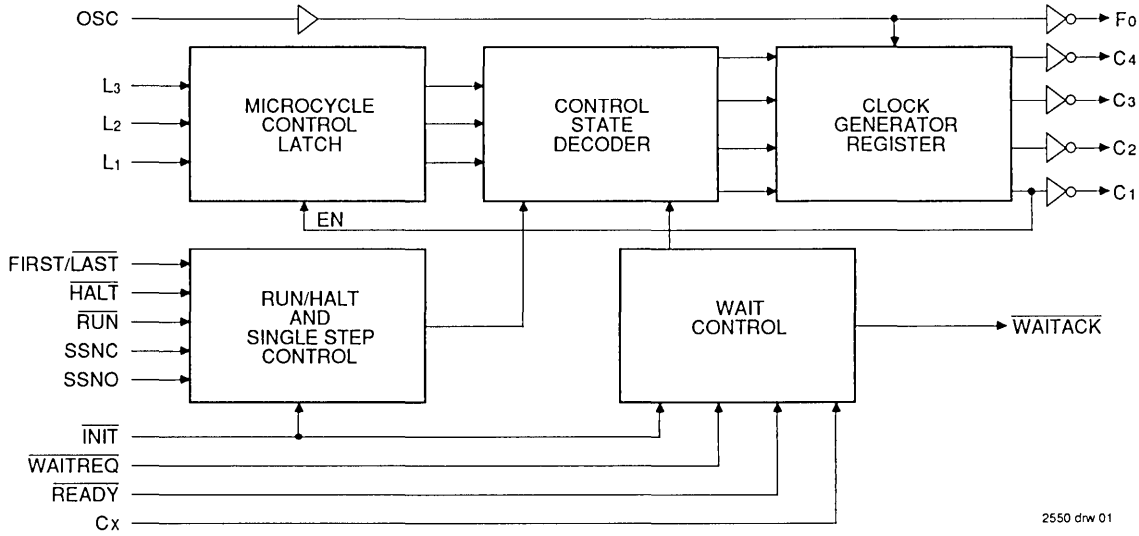
The IDT49C25/A are single-chip general purpose clock generator/drivers built using IDT's advanced CEMOS™, a dual metal CMOS technology. It has microprogrammable clock cycle length to provide significant speed-up over fixed clock cycle approaches and meets a variety of system speed requirements.

The IDT49C25/A generate four different simultaneous clock out-put waveforms tailored to meet the needs of the IDT3900 CMOS family and other MOS and bipolar microprocessor-based systems. One of eight cycle lengths may be generated under microprogram control using the cycle length inputs, L_1, L_2 and L_3.

A buffered oscillator output, F_0, is provided for external system timing in addition to the four microcode controlled clock outputs, C_1, C_2, C_3 and C_4.

System control functions include $\overline{RUN}$, $\overline{HALT}$, Single-Step, Initialize and Ready/Wait controls. In addition, the $\overline{FIRST}/\overline{LAST}$ input determines where a halt occurs and the C_x input determines the end point timing of wait cycles. $\overline{WAITACK}$ indicates that the IDT49C25/A are in a wait state.

FUNCTIONAL BLOCK DIAGRAM



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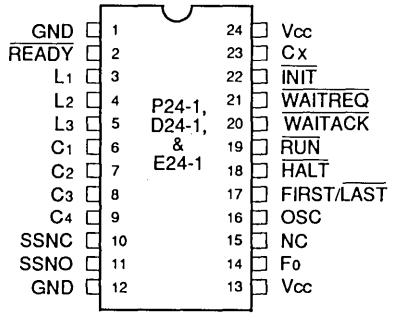
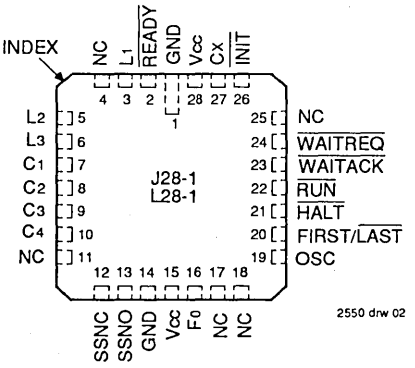
PIN CONFIGURATIONS



DIP/CERPACK
TOP VIEW



LCC/PLCC
TOP VIEW

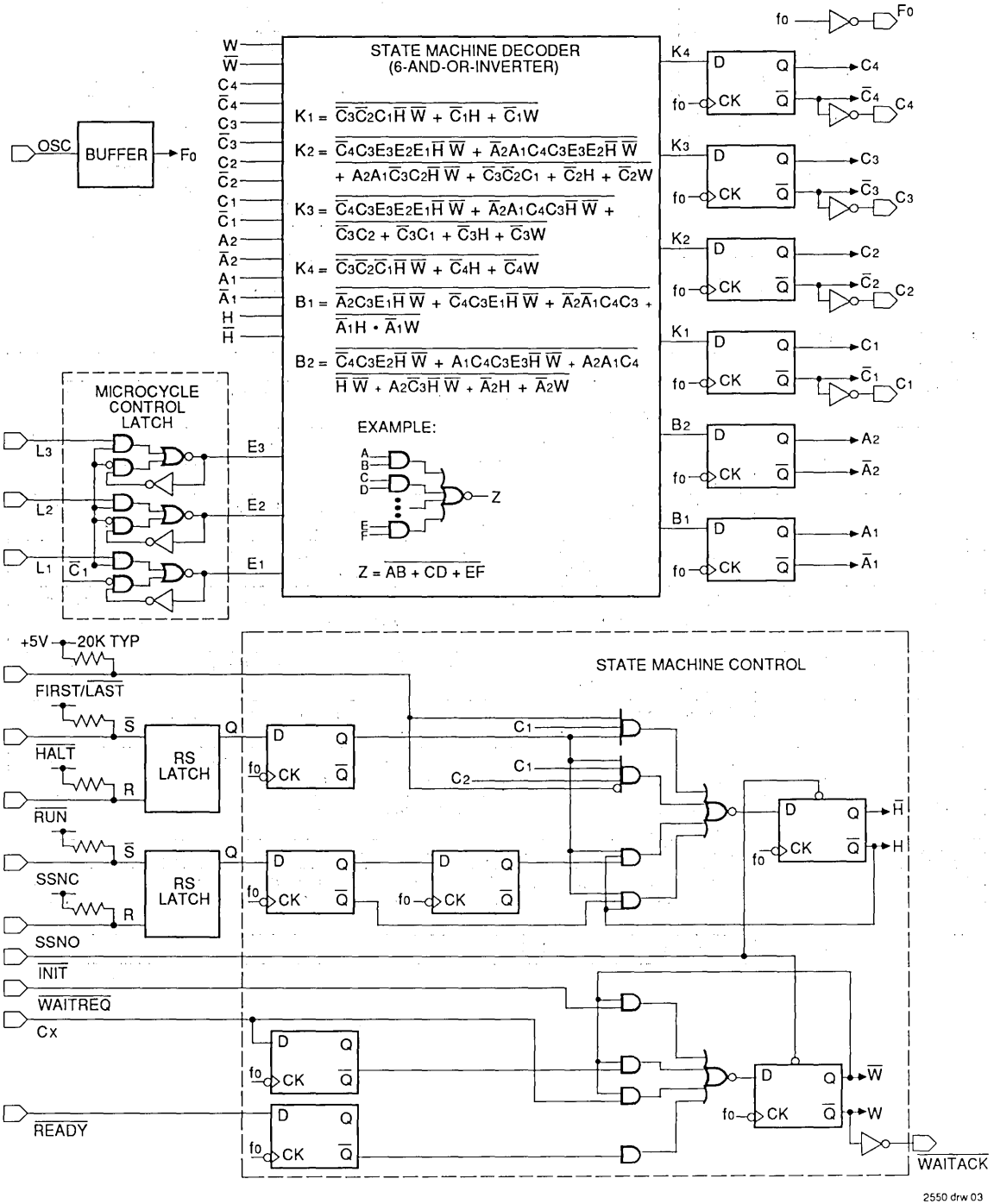
PIN DESCRIPTIONS

Pin Names	I/O	Description
C_1, C_2, C_3, C_4	O	System clock outputs. These outputs are all active during every system clock cycle. Their timing is determined by clock cycle length controls: L_1, L_2 and L_3.
L_1, L_2, L_3	I	Clock cycle length control inputs. These inputs receive the microcode bits that select the microcycle lengths. They form a control word which selects one of the eight microcycle waveform patterns F_3 through F_{10}.
F_0	O	The buffered oscillator output. F_0 internally generates all of the timing edges for outputs C_1, C_2, C_3, C_4 and $\overline{WAITACK}$. F_0 rises just prior to all of the C_1, C_2, C_3, C_4 transitions.
$\overline{HALT}$ and $\overline{RUN}$	I	Debounced inputs to provide $\overline{HALT}$ control. These inputs determine whether the output clocks run or not. A LOW input on $\overline{HALT}$ ($\overline{RUN}$ = HIGH) will stop all clock outputs.
FIRST/$\overline{LAST}$	I	$\overline{HALT}$ time control input. A HIGH input in conjunction with a $\overline{HALT}$ command will cause a halt to occur when C_4 = LOW and C_1 = C_2 = C_3 = HIGH (see clock waveforms). A LOW input causes a $\overline{HALT}$ to occur when C_1 = C_2 = C_3 = LOW and C_4 = HIGH.
SSNO and SSNC	I	Single Step control inputs. These debounced inputs allow system clock cycle single stepping while $\overline{HALT}$ is activated LOW.
$\overline{WAITREQ}$	I	The Wait Request active LOW input. When LOW, this input will cause the outputs to halt during the next oscillator cycle after the Cx input goes LOW.
Cx	I	Wait cycle control input. The clock outputs respond to a wait request one oscillator clock cycle after Cx goes LOW. Cx is normally tied to any one of C_1, C_2, C_3 or C_4.
$\overline{WAITACK}$	O	The Wait Acknowledge active LOW output. When LOW, this output indicates that all clock outputs are in the "WAIT" state.
$\overline{READY}$	I	The $\overline{READY}$ active LOW input is used to continue normal clock output patterns after a wait state.
$\overline{INIT}$	I	The Initialize active LOW input. This input is intended for use during power-up initialization of the system. When LOW, all clock outputs run free regardless of the state of the Halt, Single Step, Wait Request and Ready inputs.
OSC	I	External oscillator input (TTL level input).

2550 tbl 01

6

LOGIC DIAGRAM



2550 drw 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2550 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2550 tbl 03

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = Vcc - 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max., V_{IN} = Vcc		—	—	25	µA
I_{IL}	Input LOW Current	Vcc = Max.	SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$	—	—	-1.0	mA
		V_{IN} = GND	FIRST/$\overline{LAST}$	—	—	-1.5	
			Other Inputs	—	—	-5	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = -18mA		—	-0.7	-1.2	mA
I_{SC}	Short Circuit Current	Vcc = Max.(3), V_O = GND		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	Vcc	—	V
		Vcc = Min.	I_{OH}= -300µA	V_{HC}	Vcc	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA MIL.	2.4	4.0	—	
			I_{OH}= -5.0mA COM'L	2.4	4.0	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min.	I_{OL} = 300µA	—	GND	V_{LC}(4)	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL.	—	—	0.5	
			I_{OL} = 24mA COM'L	—	—	0.5	

NOTES: 2550 tbl 04

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circiut test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., $V_{IN} \geq V_{HC}$, $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.24	0.4	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max., Outputs Open, f_{CP} = OSC = 5MHz (50% duty cycle) $\overline{READY}$, SSNO, $\overline{WAITREQ}$, $\overline{HALT}$, $\overline{INIT}$ = V_{CC} L_1, L_2, L_3, SSNC, FIRST/$\overline{LAST}$, $\overline{RUN}$, C_X = GND		—	6.5	9.7	mA
		V_{CC} = Max. Outputs Open f_{CP} = OSC = 5MHz (50% duty cycle) SSNO, $\overline{HALT}$ = V_{CC} $\overline{READY}$, $\overline{WAITREQ}$, $\overline{INIT}$ = 3.4V (98% duty cycle) L_1, L_2, L_3, SSNC, FIRST/$\overline{LAST}$, $\overline{RUN}$, C_X = GND		—	8.5	16.6	

2550 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_O N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at DH
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

				IDT49C25				IDT49C25A				
				Com'l.		Mil.		Com'l.		Mil.		
	Symbol	Parameter	Condition	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
1	f_{MAX1}	F_O Frequency (C_x Connected)[1, 6]	C_L = 50pF R_L = 500Ω	31	—	31	—	40	—	40	—	MHz
2	f_{MAX2}	F_O Frequency (C_x = HIGH)[6]		—	—	—	—	—	—	—	—	MHz
3	t_{OFFSET}	F_O (↗) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↗)		—	8.5	—	8.5	—	6.0	—	6.0	ns
4	t_{OFFSET}	F_O (↗) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↘)		—	17	—	18	—	11.5	—	12	ns
5	t_{SKEW}	C_1 (↗) to C_2 (↗)		—	2	—	2	—	1.5	—	1.5	ns
6	t_{SKEW}	C_1 (↗) to C_3 (↗)		—	2	—	2	—	1.5	—	1.5	ns
7	t_{SKEW}	C_1 (↗) to C_4 (↘) Opposite Transition		—	11	—	11	—	8.0	—	8.0	ns
8	t_{SU}	L_1, L_2, L_3, to C_1 (↗)		6	—	6	—	5	—	5	—	ns
9	t_H	L_1, L_2, L_3, to C_1 (↗)		8	—	8	—	6	—	6	—	ns
10	t_{SU}	C_x to F_O (↗)[2]		18	—	18	—	12	—	12	—	ns
11	t_H	C_x to F_O (↗)[2]		0	—	0	—	0	—	0	—	ns
12	t_{SU}	$\overline{WAITREQ}$ to F_O (↗)[3]		18	—	18	—	12	—	12	—	ns
13	t_H	$\overline{WAITREQ}$ to F_O (↗)[3]		0	—	0	—	0	—	0	—	ns
14	t_{SU}	$\overline{READY}$ to F_O (↗)[3]		18	—	18	—	12	—	12	—	ns
15	t_H	$\overline{READY}$ to F_O (↗)[3]		0	—	0	—	0	—	0	—	ns
16	t_{SU}	$\overline{RUN}$, $\overline{HALT}$ (↗) to F_O (↗)[3,4]		18	—	18	—	12	—	12	—	ns
17	t_{SU}	SSNC, SSNO to F_O (↗)[3,4]		18	—	18	—	12	—	12	—	ns
18	t_{SU}	FIRST/$\overline{LAST}$ to F_O (↗)[5]		18	—	18	—	12	—	12	—	ns
19	t_{SU}	$\overline{INIT}$ (↗) to F_O (↗)[3]		18	—	18	—	12	—	12	—	ns
20	t_W	$\overline{INIT}$ LOW Pulse Width		20	—	25	—	18	—	23	—	ns
21	t_{PLH}	$\overline{INIT}$ to $\overline{WAITACK}$		—	25	—	27	—	16	—	18	ns
22	t_{PLH}	OSC to F_O		—	13	—	16	—	8.5	—	10.5	ns
23	t_{PHL}			—	13	—	16	—	8.5	—	10.5	ns

NOTES:

2550 tbl 06

1. The frequency guarantees apply with C_x connected to C_1, C_2, C_3, C_4 or HIGH. The C_x input load must be considered part of the 50pf/500Ω clock output loading.
2. These set-up and hold times apply to the F_O LOW-to-HIGH transition of the period in which C_x goes LOW.
3. These inputs are synchronized internally. Failure to meet ts may cause a $1/F_O$ delay but will not cause incorrect operation.
4. These inputs are "debounced" by an internal R-S flip-flop and are intended to be connected to manual break-before-make switches.
5. FIRST/$\overline{LAST}$ normally wired HIGH or LOW.
6. This parameter is guaranteed but not tested.

SWITCHING WAVEFORMS

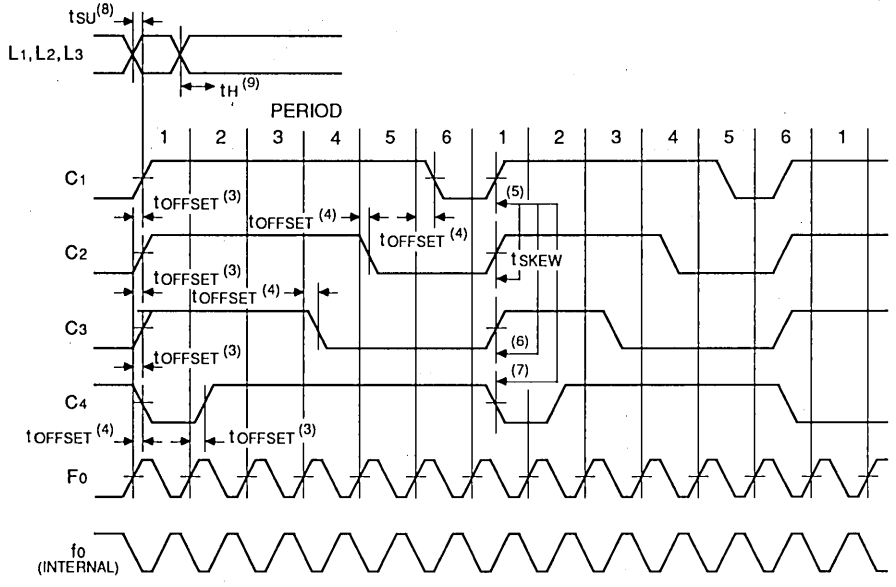
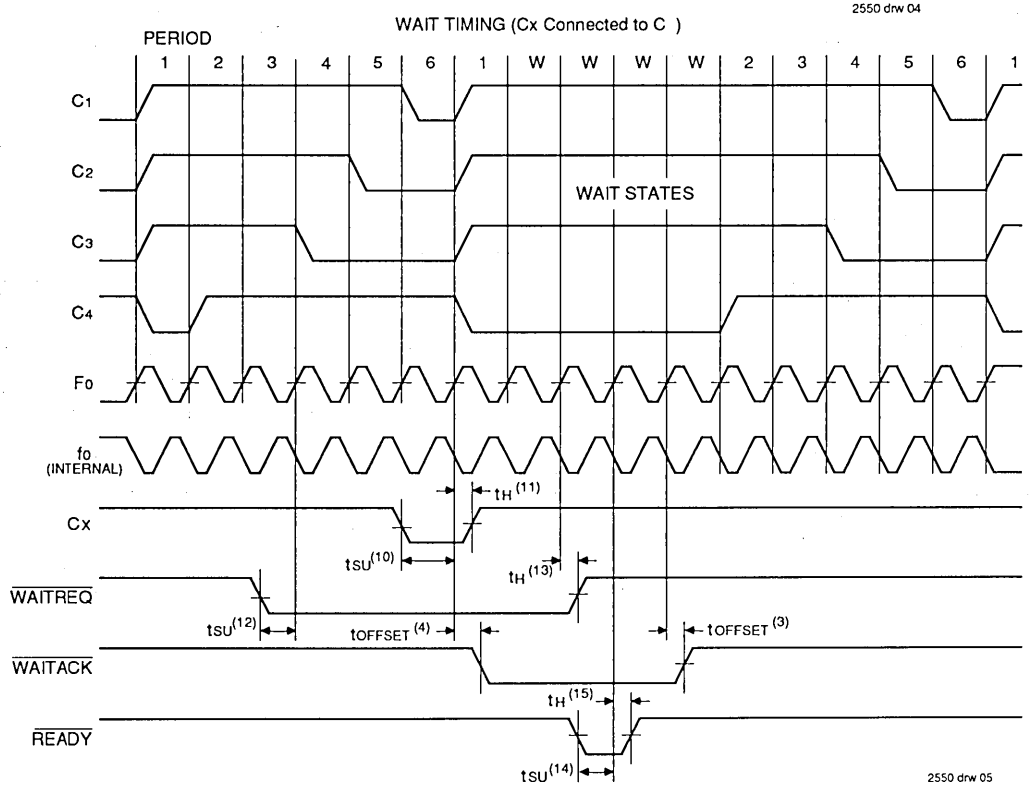


Figure 2. Normal Cycle Without Wait States (Pattern F6 Shown)

2550 drw 04



2550 drw 05

Figure 3. Wait Timing (CX Connected to C1)

DETAILED DESCRIPTION

The IDT49C25/A are dynamically programmable general-purpose clock controllers. They can be logically separated into two parts — a state machine decoder and a state machine control section.

The state machine takes microcode information from the Microcycle Length (L) inputs L_1, L_2 and L_3 and counts the fundamental frequency of the oscillator (OSC) to create the clock outputs F_0, C_1, C_2, C_3 and C_4.

The clock outputs have a characteristic wave shape

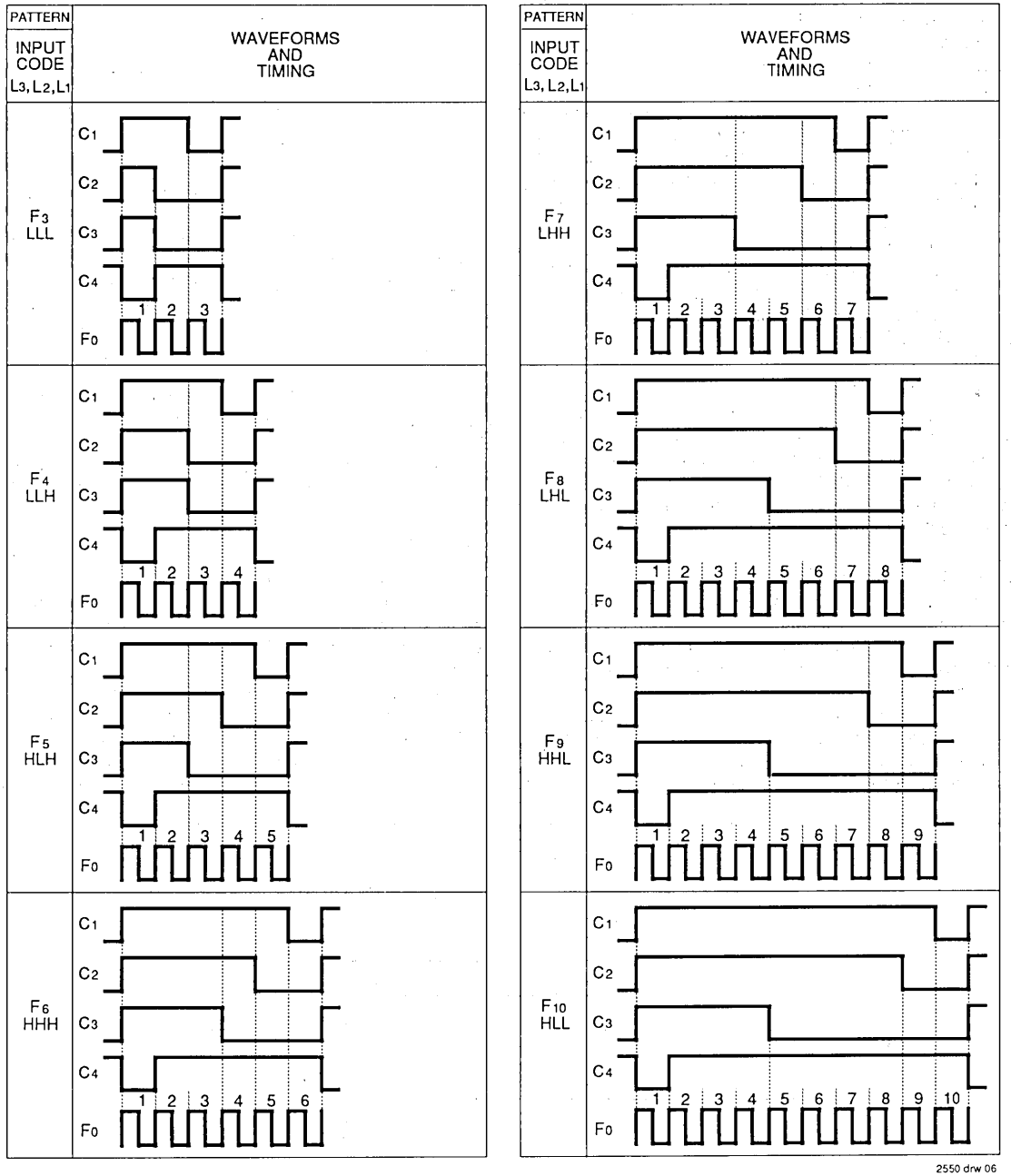


Figure 4. IDT49C25/A Clock Waveforms

relationship for each microcycle length. For example, C_1 is always LOW only on the last F_0 clock period of a microcycle and C_4 is always LOW on the first. C_3 has an approximate duty cycle of 50% and C_2 is HIGH for all but the last two periods (see Figure 4).

The current state of the machine is contained in a register, part of which is the Clock Generator Register. C_1, C_2, C_3 and C_4 are the outputs of this register. These outputs and the outputs of the Microcycle Control Latch are fed into combinatorial logic to generate the next state. On each falling edge of the internal clock, the next state is entered into the current state register. The Microcycle Control Latch is latched when C_1 is HIGH. This means that it will be loaded during the last state of each microcycle ($C_1 = C_2 = C_3$ = LOW, C_4 = HIGH). This internal latch selects one of eight possible microcycle lengths, F_3 to F_{10}.

The state machine control logic, which determines the mode of operation of the state machine, is intended to be connected to a front panel. There are four basic modes of operation of the IDT49C25/A comprised of $\overline{RUN}$, $\overline{HALT}$, $\overline{WAIT}$ and SINGLE STEP.

SYSTEM TIMING

In the typical computer, the time required to execute different instructions varies. However, the time allotted to each instruction is the time that it takes to execute the longest instruction. The IDT49C25/A allows the user to dynamically vary the time allotted for each instruction, thereby allowing the user to realize a higher throughput.

IDT49C25/A CONTROL INPUTS

The control inputs fall into two categories, microcycle length control and clock control. Microcycle length control is provided via the "L" inputs which are intended to be connected to the microprogram memory. The "L" inputs are used to select one of eight cycle lengths ranging from three oscillator cycles for pattern F_3 to ten oscillator cycles for pattern F_{10}. This information is always loaded at the end of the microcycle into the Microcycle Control Latch which performs the function of a pipeline register for the microcycle length microcode bits.

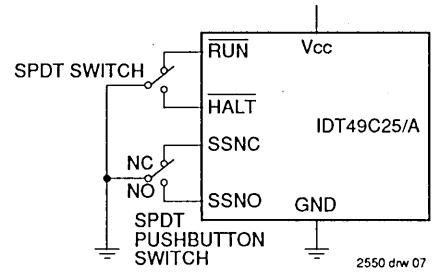


Figure 5. Switch Connection for $\overline{RUN}$/$\overline{HALT}$ and Single Step

Therefore, the cycle length goes in the same microword as the instruction that it is associated with.

The clock control inputs are used to synchronize the microprogram machine with the external world and I/O devices. Inputs like $\overline{RUN}$, $\overline{HALT}$, SSNO and SSNC, which start and stop execution, are meant to be connected to switches on the front panel of the microprogrammed machine (see Figure 5). These inputs have internal pull-up resistors and are connected to an R-S flip-flop in order to provide switch debouncing. The FIRST/$\overline{LAST}$ input is used to determine at what point of the microcycle the IDT49C25/A will halt when $\overline{HALT}$ or a SINGLE STEP is initiated. In most applications, the user wires this input HIGH or LOW, depending on the design.

When $\overline{HALT}$ is held low ($\overline{RUN}$ = HIGH), the state machine will start the halt mode on the last (C_1 = LOW) or the first (C_4 = LOW) state of the microcycle as determined by the FIRST/$\overline{LAST}$ input. When $\overline{RUN}$ goes low ($\overline{HALT}$ = HIGH), the state machine will resume the run mode.

The $\overline{WAITREQ}$, Cx, $\overline{READY}$ and $\overline{WAITACK}$ signals are used to synchronize other parts of a computer system (memory, I/O devices) to the CPU by dynamically stretching the microcycle. For example, the CPU may access a slow peripheral that requires the data remain on the date bus for several microseconds. In this case, the peripheral pulls the $\overline{WAITREQ}$ line LOW. The Cx input lets the design specify when the $\overline{WAITREQ}$ line is sampled in the microcycle. This has a direct impact on how much time the peripheral has to

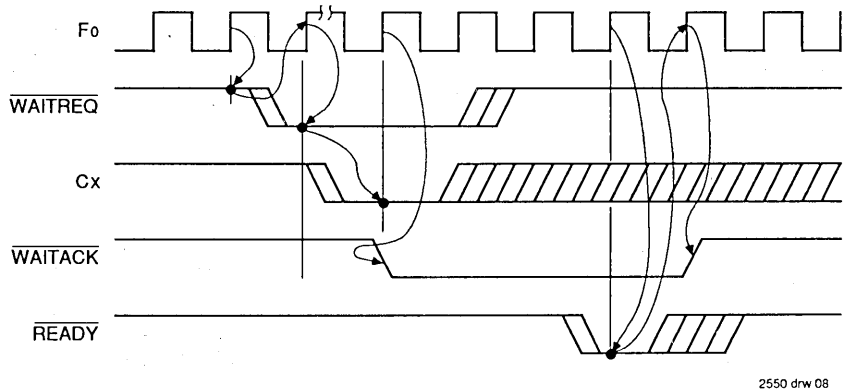


Figure 6. $\overline{WAIT}$/$\overline{READY}$ Timing

respond in order to request a wait cycle (see Figure 6). The $\overline{READY}$ line is used by the peripheral to signal when it is ready to resume execution of the rest of the microcycle. The $\overline{WAITACK}$ line goes LOW on the next oscillator cycle after the Cx input goes LOW and remains LOW until the second oscillator cycle after $\overline{READY}$ goes LOW.

The SSNO and SSNC inputs are used to initiate the SINGLE STEP mode. These debounced inputs allow a single microcycle to occur while in the halt mode. SSNO (normally open) and SSNC (normally closed) are intended to be connected to a momentary SPDT switch. After SSNO has been high for one clock edge, the state machine will change to the next run mode. The microcycle will end on the first or last state of the microcycle, depending on the state of the FIRST/$\overline{LAST}$.

AC TIMING SIGNAL REFERENCES

Set-up and hold times in registers and latches are measured relative to the clock signals that drive them. In the IDT49C25/A, the external oscillator provides a free running clock signal that drives all the registers on the devices. This clock is provided for the user through the buffered output of F_0. Therefore, F_0 is used as the reference of set-up, hold and clock-to-output times. However, for the Microcycle Control Latch, the set-up and hold times are referenced to the C_1 output which is the buffered version of the latch enable. This reference is appropriate for the Microcycle Control Latch because, in a typical application, this latch is considered part of the pipeline register which is also driven by one of the "C" outputs.

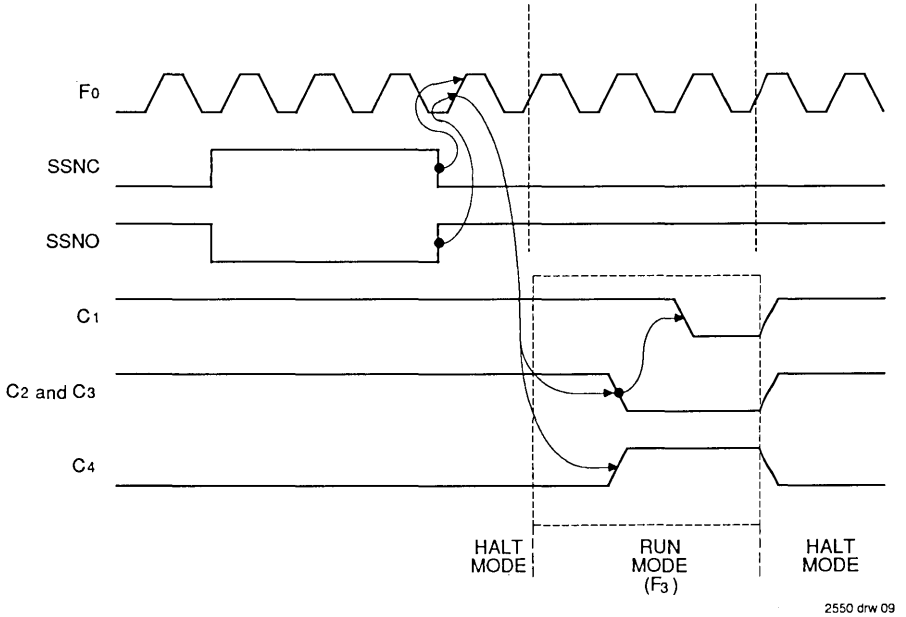
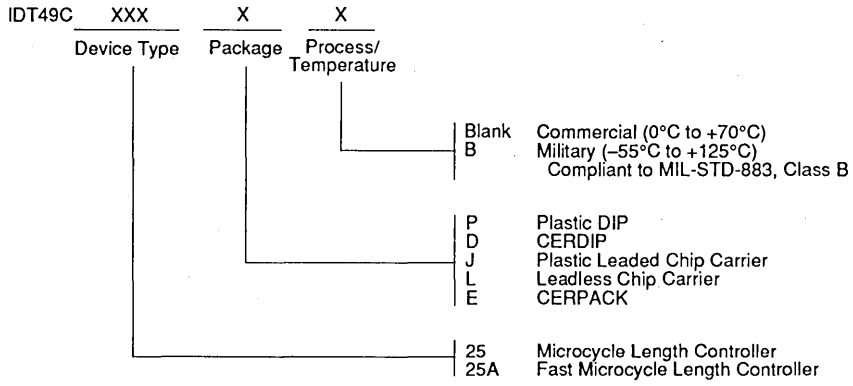


Figure 7. Single Step Timing Sequence

ORDERING INFORMATION



2550 drw 10

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE

IDT39C8XX

The part numbering scheme for the IDT39C8XX family had been changed in 1988 to conform with the new proposed JEDEC part numbering system. The new system is as follows:

Previous Part Number	New Part Number
IDT39C821	IDT54/74FCT821A
IDT39C822	IDT54/74FCT822A
IDT39C823	IDT54/74FCT823A
IDT39C824	IDT54/74FCT824A
IDT39C825	IDT54/74FCT825A
IDT39C826	IDT54/74FCT826A
IDT39C827	IDT54/74FCT827A
IDT39C828	IDT54/74FCT828A
IDT39C841	IDT54/74FCT841A
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IDT39C843	IDT54/74FCT843A
IDT39C844	IDT54/74FCT844A
IDT39C845	IDT54/74FCT845A
IDT39C846	IDT54/74FCT846A
IDT39C861	IDT54/74FCT861A
IDT39C862	IDT54/74FCT862A
IDT39C863	IDT54/74FCT863A
IDT39C864	IDT54/74FCT864A

Refer to data sheets under the new part number system for all specifications.

6

Integrated Device Technology, Inc.

FAST CMOS 1-OF-8 DECODER

IDT54/74FCT138
IDT54/74FCT138A
IDT54/74FCT138C

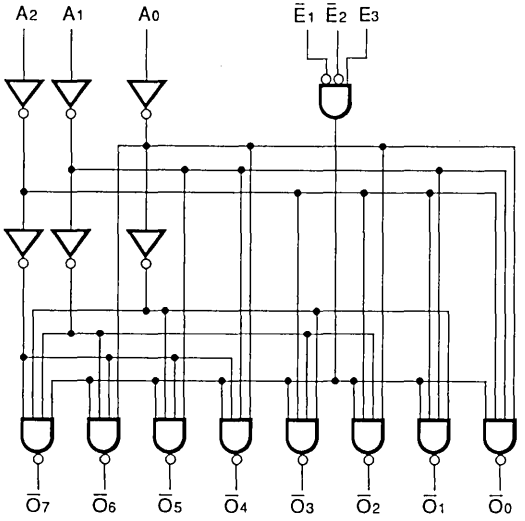
FEATURES:

- IDT54/74FCT138 equivalent to FAST™ speed
- **IDT54/74FCT138A 35% faster than FAST™**
- Equivalent to FAST™ speeds output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 1-of-8 decoder with enables
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing # 5962-87654 is listed on this function. Refer to section 2

DESCRIPTION:

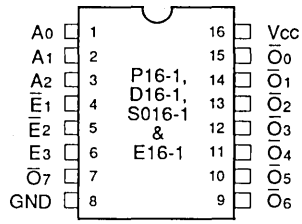
The IDT54/74FCT138/A/C are 1-of-8 decoders built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT138/A/C accept three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provide eight mutually exclusive active LOW outputs ($\overline{O}_0$ - $\overline{O}_7$). The IDT54/74FCT138/A/C feature three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74FCT138/A/C devices and one inverter.

FUNCTIONAL BLOCK DIAGRAM

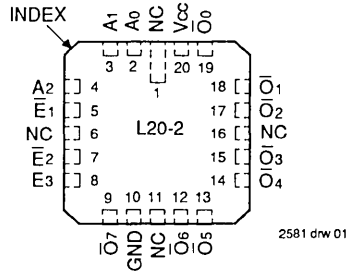


2581 drw 02

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2581 drw 01

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0$–$\overline{O}_7$	Outputs (Active LOW)

2581 tbl 05

FUNCTION TABLE

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

2581 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2581 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2581 tbl 02

1. This parameter is guaranteed characterization data and not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2581 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} ≥ V_{HC}; V_{IN} ≤ V_{LC}		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Output Toggling 50% Duty Cycle	V_{IN} ≥ V_{HC} V_{IN} ≤ V_{LC}	—	0.15	0.3	mA/MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open Toggle $\overline{E}_1$, $\overline{E}_2$ or E_3	V_{IN} ≥ V_{HC} V_{IN} ≤ V_{LC} (FCT)	—	1.7	4.5	mA
		50% Duty Cycle f_O = 10MHz One Output Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	

2581 tbl 04

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + ΔI_{CC} $D_H N_T$ + I_{CCD} (f_{CP}/2 + $f_O N_O$)
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT138				IDT54/74FCT138A				IDT54/74FCT138C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay An to $\overline{On}$	CL = 50pF RL = 500Ω	1.5	9.0	1.5	12.0	1.5	5.8	1.5	7.8	—	—	—	—	ns
tPLH tPHL	Propagation Delay $\overline{E1}$ or $\overline{E2}$ to $\overline{On}$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	—	—	—	—	ns
tPLH tPHL	Propagation Delay E3 to $\overline{On}$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	—	—	—	—	ns

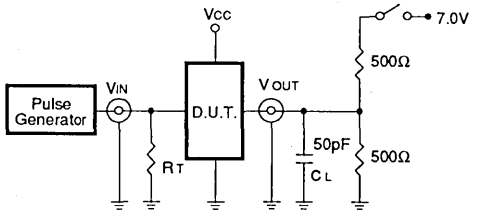
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2581 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



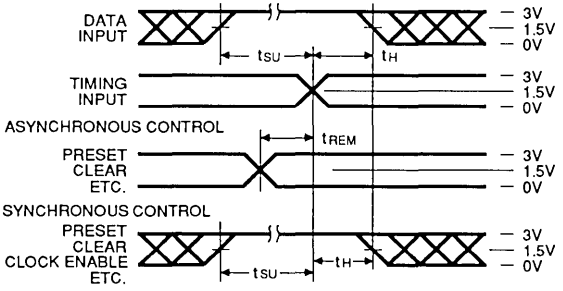
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

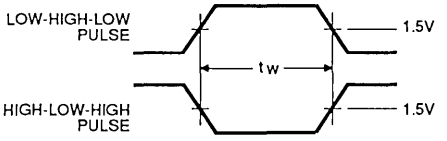
DEFINITIONS: 2581 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

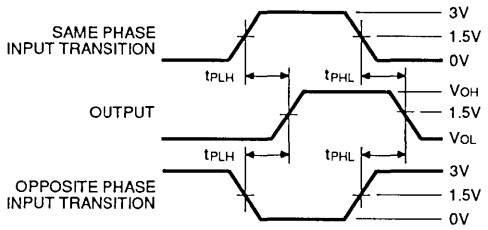
SET-UP, HOLD AND RELEASE TIMES



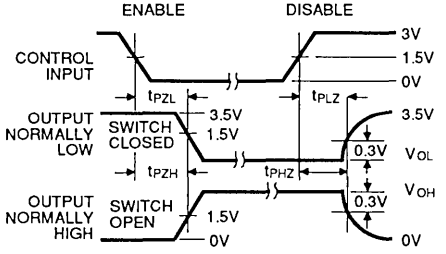
PULSE WIDTH



PROPAGATION DELAY



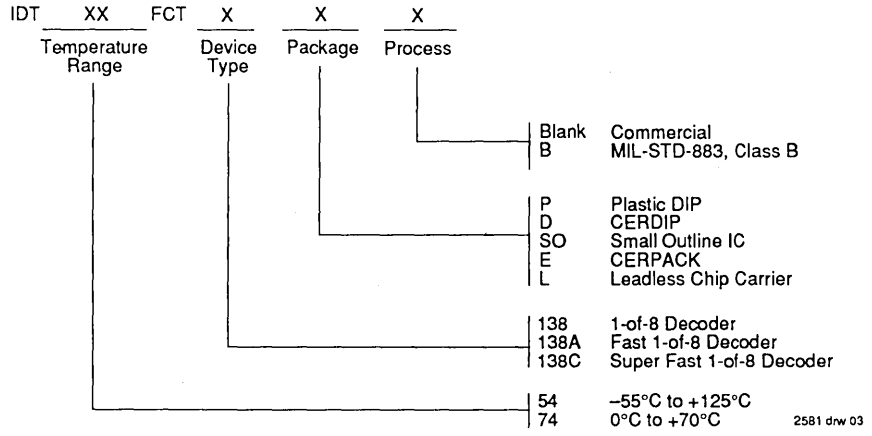
ENABLE AND DISABLE TIMES



NOTES 2581 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

DUAL 1-OF-4 DECODER

IDT54/74FCT139
IDT54/74FCT139A
IDT54/74FCT139C

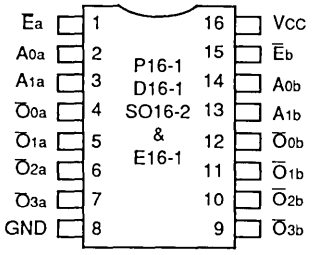
FEATURES:

- IDT54/74FCT139 equivalent to FAST™ speed
- **IDT54/74FCT139A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Dual 1-of-4 decoder with enable
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

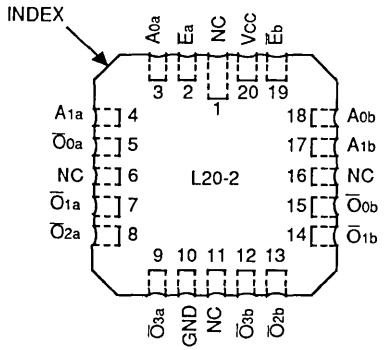
DESCRIPTION:

The IDT54/74FCT139/A/C are dual 1-of-4 decoders built using advanced CEMOS™, a dual metal CMOS technology. These devices have two independent decoders, each of which accept two binary weighted inputs (A_0-A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

PIN CONFIGURATIONS



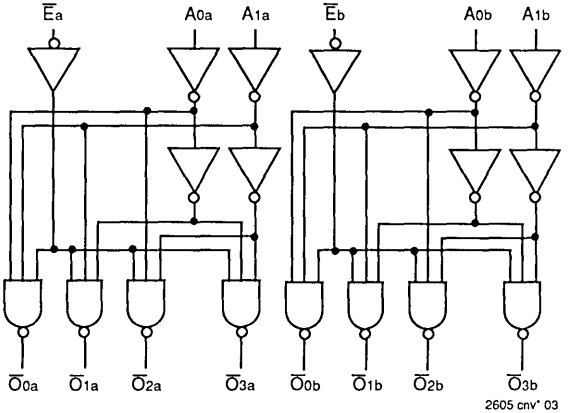
DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

2605 cnv* 02

FUNCTIONAL BLOCK DIAGRAM



2605 cnv* 01

2605 cnv* 03

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor, Inc.

FUNCTION TABLE[1]

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

2605 tbl 05

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
A_0, A_1	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
$\overline{O}_0$ - $\overline{O}_3$	Outputs (Active LOW)

2605 tbl 04

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

2605 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2605 tbl 02

NOTE:
1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2605 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS $V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT) V_{IN} = 3.4V V_{IN} = GND	— —	1.7 2.0	4.5 5.5	mA
		V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle One Bit Toggling on Each Decoder	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT) V_{IN} = 3.4V V_{IN} = GND	— —	3.2 3.7	7.5[5] 9.5[5]	

NOTES: 2605 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_O = Number of Outputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

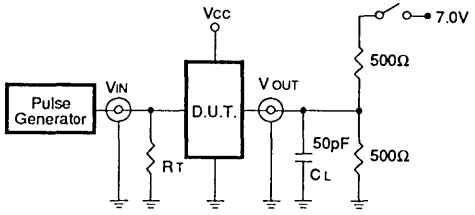
			IDT54/74FCT139				IDT54/74FCT139A				IDT54/74FCT139C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Parameter	Description	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{On}$	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	12.0	1.5	5.9	1.5	7.8	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{On}$		1.5	8.0	1.5	9.0	1.5	5.5	1.5	7.2	—	—	—	—	ns

NOTES: 2605 tbl 07

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



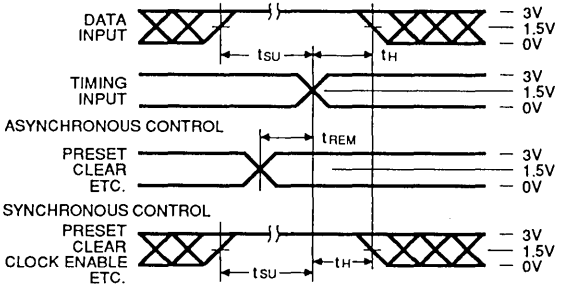
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

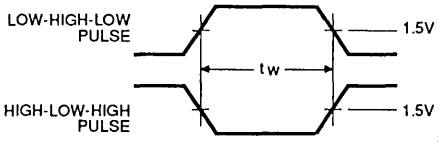
DEFINITIONS: 2605 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

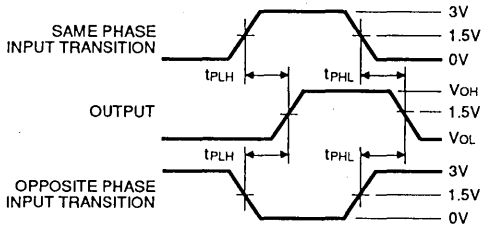
SET-UP, HOLD AND RELEASE TIMES



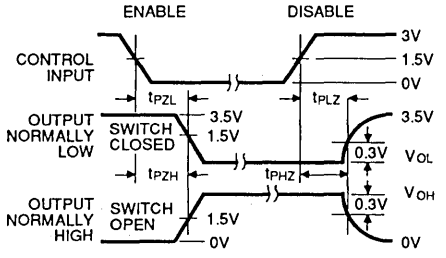
PULSE WIDTH



PROPAGATION DELAY



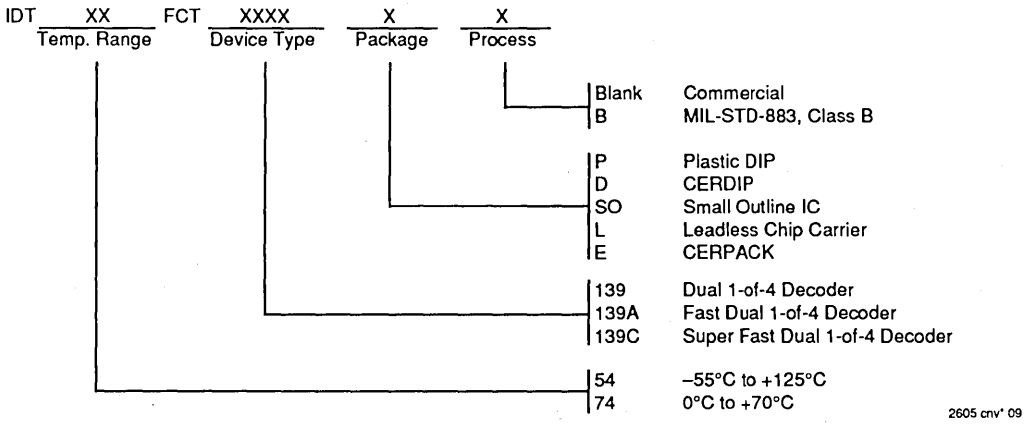
ENABLE AND DISABLE TIMES



NOTES 2605 drw 10

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_O \leq 50\Omega$; $t_F \leq 2.5$ns; $t_R \leq 2.5$ns.

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54/74FCT161
IDT54/74FCT161A
IDT54/74FCT163
IDT54/74FCT163A

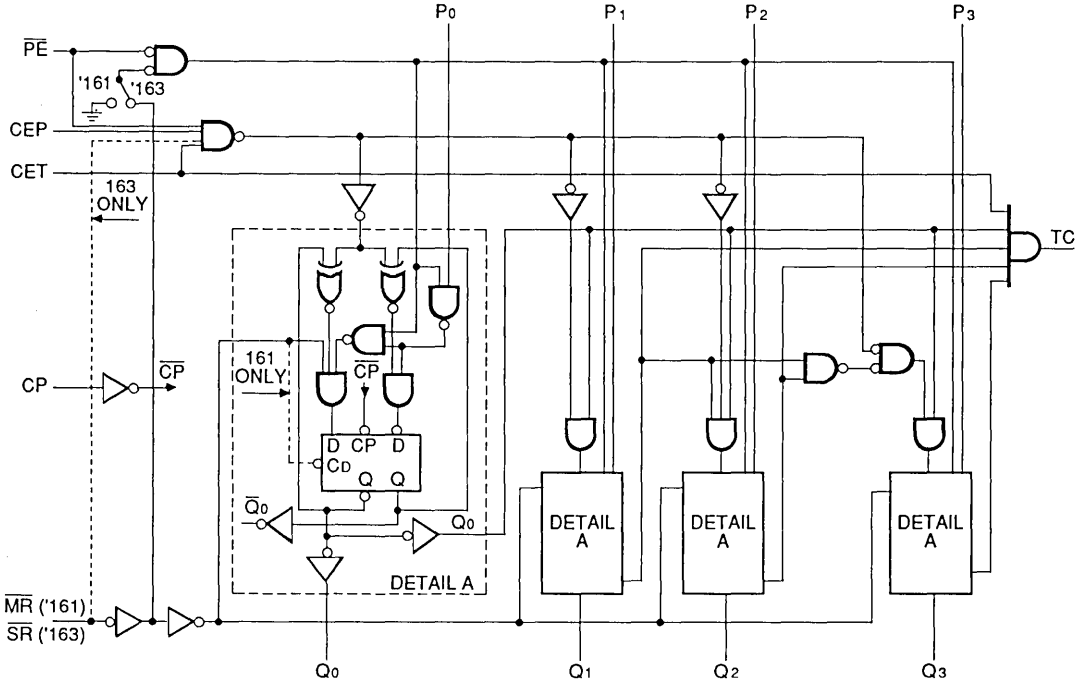
FEATURES:

- IDT54/74FCT161/163 equivalent to FAST™ speed
- **IDT54/74FCT161A/163A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT161/163 and IDT54/74FCT161A/163A are high-speed synchronous modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multistage counters. The IDT54/74FCT161 and IDT54/74FCT161A have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54/74FCT163 and IDT54/74FCT163A have Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

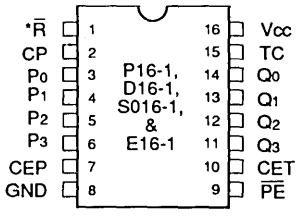
FUNCTIONAL BLOCK DIAGRAM



2612 drw 01

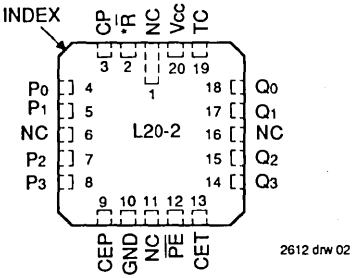
CEMOS is a trademark of Integrated Device Techology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

*$\overline{MR}$ for '161
*$\overline{SR}$ for '163



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)
P_{0-3}	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q_{0-3}	Flip-Flop Outputs
TC	Terminal Count Output

2612 tbl 05

FUNCTION TABLE[2]

$\overline{SR}$[1]	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge(s)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES: 2612 tbl 06
1. For FCT163/163A only.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care.

6

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2612 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2612 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V, V_{HC} = Vcc - 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = Vcc	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	-5[4]	
			V_I = GND	—	—	-5	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.[3], V_O = GND		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	Vcc	—	V
		Vcc = Min.	I_{OH} = -300µA	V_{HC}	Vcc	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2612 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open Load Mode $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	12.8[5]	

NOTES:

2612 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

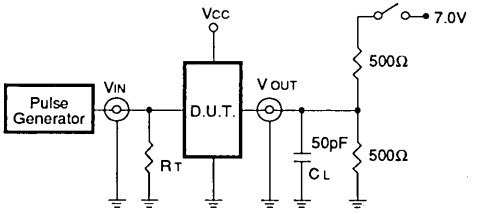
Symbol	Parameter	Condition[1]	IDT54/74FCT161/163				IDT54/74FCT161A/163A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Qn ($\overline{PE}$ Input HIGH)	C_L = 50pF R_L = 500Ω	2.0	11.0	2.0	11.5	2.0	7.2	2.0	7.5	ns
tPLH tPHL	Propagation Delay CP to Qn ($\overline{PE}$ Input LOW)		2.0	9.5	2.0	10.0	2.0	6.2	2.0	6.5	ns
tPLH tPHL	Propagation Delay CP to TC		2.0	15.0	2.0	16.5	2.0	9.8	2.0	10.8	ns
tPLH tPHL	Propagation Delay CET to TC		1.5	8.5	1.5	9.0	1.5	5.5	1.5	5.9	ns
tPHL	Propagation Delay $\overline{MR}$ to Qn ('161)		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.1	ns
tPHL	Propagation Delay $\overline{MR}$ to TC ('161)		2.0	11.5	2.0	12.5	2.0	7.5	2.0	8.2	ns
tSU	Set-up Time, HIGH or LOW Pn to CP		5.0	—	5.5	—	4.0	—	4.5	—	ns
tH	Hold Time, HIGH or LOW Pn to CP		1.5	—	2.0	—	1.5	—	2.0	—	ns
tSU	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		11.5	—	13.5	—	9.5	—	11.5	—	ns
tH	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time, HIGH or LOW CEP or CET to CP		11.5	—	13.0	—	9.5	—	11.0	—	ns
tH	Hold Time, HIGH or LOW CEP or CET to CP		0	—	0	—	0	—	0	—	ns
tW	Clock Pulse Width (Load) HIGH or LOW		5.0	—	5.0	—	4.0[3]	—	4.0[3]	—	ns
tW	Clock Pulse Width (Count) HIGH or LOW		7.0	—	8.0	—	6.0	—	7.0	—	ns
tW	$\overline{MR}$ Pulse Width, LOW ('161)		5.0	—	5.0	—	4.0[3]	—	4.0[3]	—	ns
tREM	Recovery Time $\overline{MR}$ to CP ('161)		6.0	—	6.0	—	5.0	—	5.0	—	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2612 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

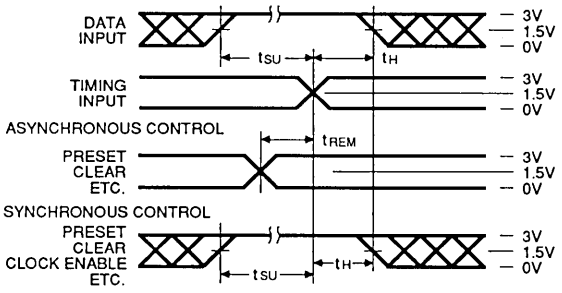
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2612 tbl 08

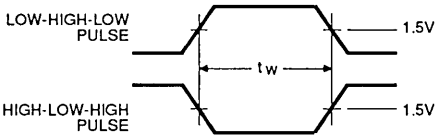
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

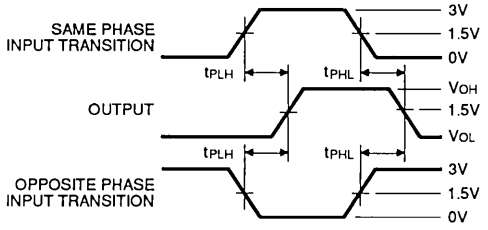
SET-UP, HOLD AND RELEASE TIMES



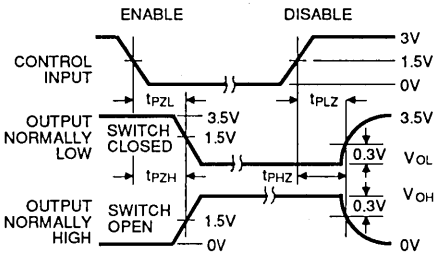
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



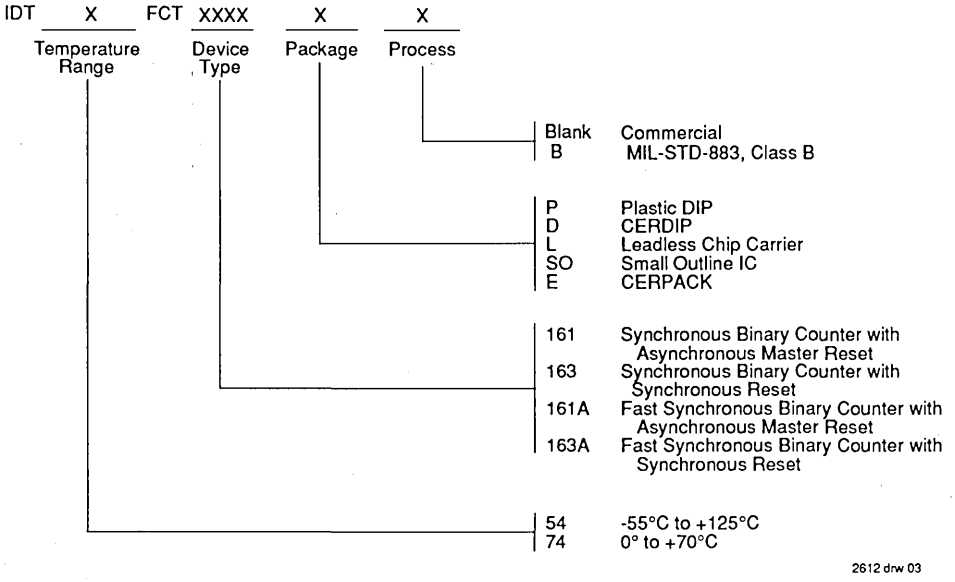
2612 drw 04

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS CARRY LOOKAHEAD GENERATOR

IDT54/74FCT182
IDT54/74FCT182A

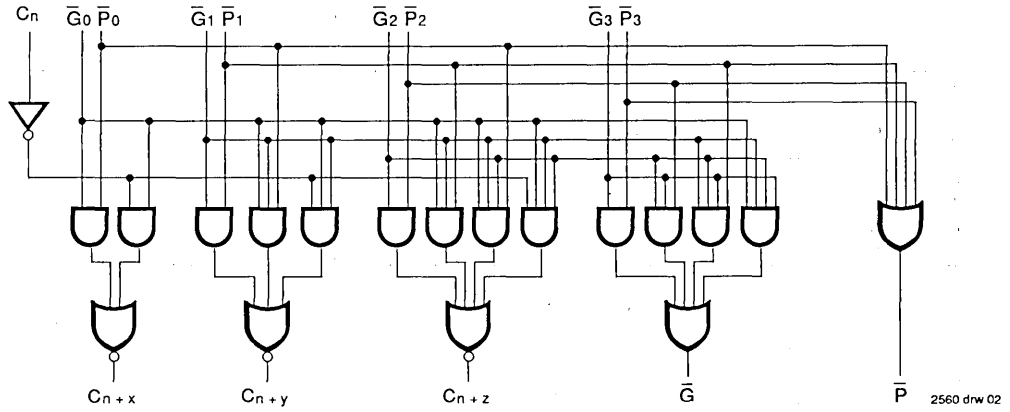
FEATURES:

- IDT54/74FCT182 equivalent to FAST™ speed;
- **IDT54/74FCT182A 30% faster than FAST ™**
- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Carry lookahead generator
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

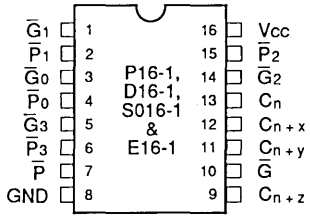
DESCRIPTION:

The IDT54/74FCT182 and IDT54/74FCT182A are high-speed carry lookahead generators built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT182 and IDT54/74FCT182A are carry lookahead generators that accept up to four pairs of active LOW Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH carry input (C_n) and provides anticipated HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. These products also have active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead.

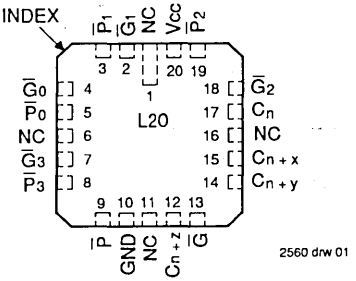
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
C_n	Carry Input
$\overline{G}_0 - \overline{G}_3$	Carry Generate Inputs (Active LOW)
$\overline{P}_0 - \overline{P}_3$	Carry Propagate Inputs (Active LOW)
$C_{n+x} - C_{n+z}$	Carry Outputs
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)

2560 tbl 05

FUNCTION TABLE[1]

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

2560 tbl 06

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2560 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2560 tbl 02

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = Vcc - 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = Vcc	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	-5[4]	
			V_I = GND	—	—	-5	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.[3], V_O = GND		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	Vcc	—	V
		Vcc = Min.	I_{OH} = -300µA	V_{HC}	Vcc	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2560 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	

2560 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	IDT54/74FCT182				IDT54/74FCT182A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay C_n to C_{n+x}, C_{n+y}, C_{n+z}	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	16.5	2.0	7.0	2.0	10.7	ns
tPLH tPHL	Propagation Delay $\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$ to C_{n+x}, C_{n+y}, C_{n+z}		1.5	9.0	1.5	11.5	1.5	8.5	1.5	9.0	ns
tPLH tPHL	Propagation Delay $\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ to C_{n+x}, C_{n+y}, C_{n+z}		1.5	9.5	1.5	11.5	1.5	8.5	1.5	9.0	ns
tPLH tPHL	Propagation Delay $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$ to $\overline{G}$		2.0	11.0	2.0	16.5	2.0	7.2	2.0	10.7	ns
tPLH tPHL	Propagation Delay $\overline{G}_n$ to $\overline{G}$		2.0	11.5	2.0	16.5	2.0	7.6	2.0	10.7	ns
tPLH tPHL	Propagation Delay $\overline{P}_n$ to $\overline{P}$		1.5	8.5	1.5	12.5	1.5	6.0	1.5	7.4	ns

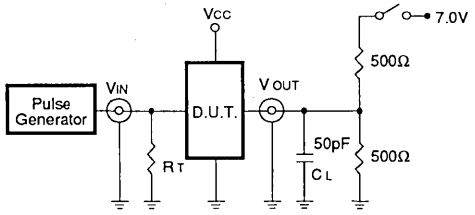
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2560 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

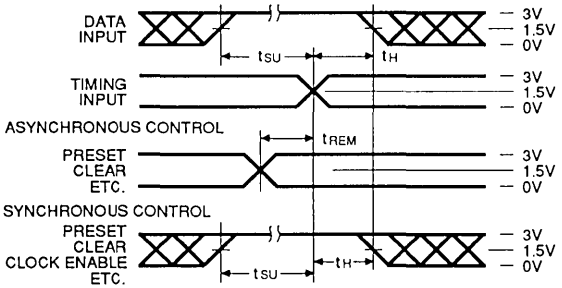
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2560 tbl 08

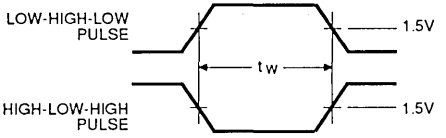
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

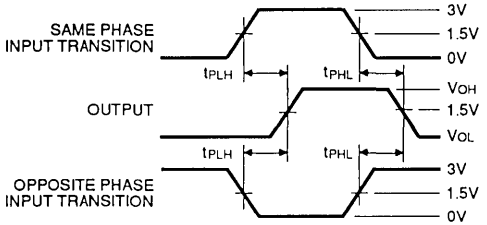
SET-UP, HOLD AND RELEASE TIMES



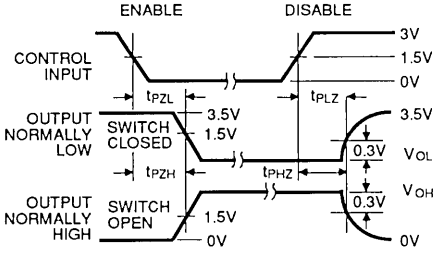
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

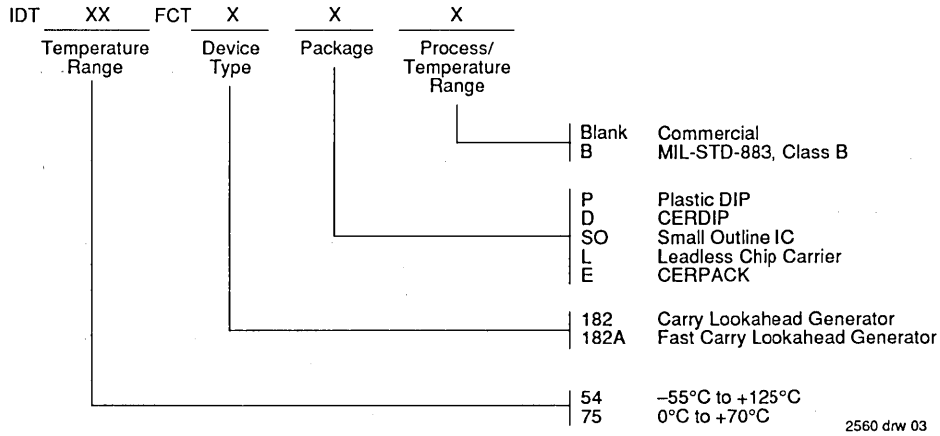


2560 drw 04

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

FAST CMOS UP/DOWN BINARY COUNTER

IDT54/74FCT191
IDT54/74FCT191A

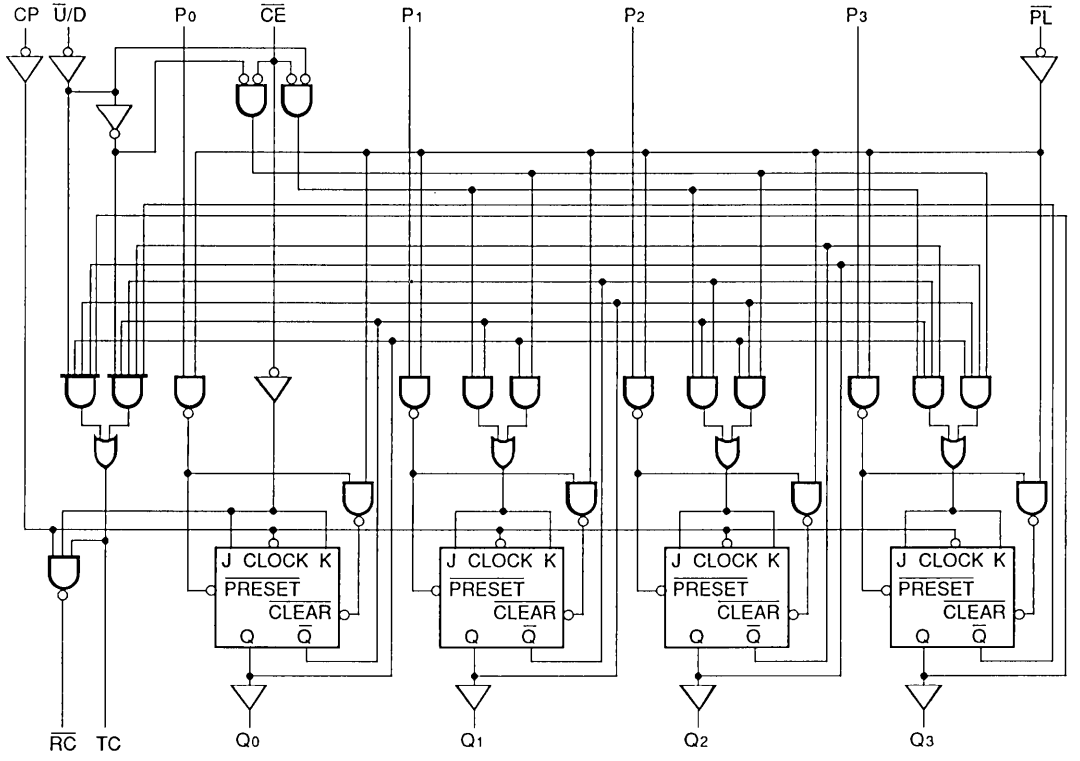
FEATURES:

- IDT54/74FCT191 equivalent to FAST™ speed
- **IDT54/74FCT191A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5μA max.)
- JEDEC standard pinout for DIP, LCC and SOIC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT191 and IDT54/74FCT191A are reversible modulo-16 binary counters, featuring synchronous counting and asynchronous presetting and are built using advanced CEMOS™, a dual metal CMOS technology. The preset feature allows the IDT54/74FCT191 and IDT54/74FCT191A to be used in programmable dividers. The count enable input, terminal count output and ripple clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM



2616 drw 01

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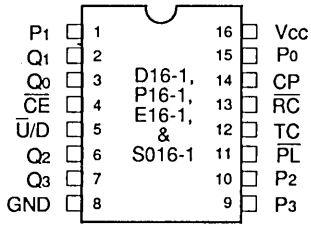
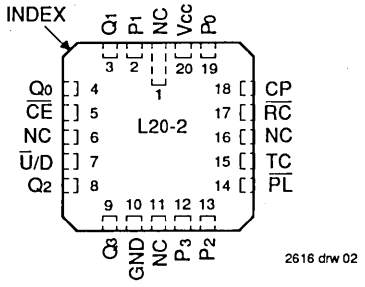
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P_{0-3}	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}/D$	Up/Down Count Control Input
Q_{0-3}	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Count Output (Active HIGH)

2616 tbl 05

$\overline{RC}$ FUNCTION TABLE[2]

Inputs		Outputs	
$\overline{CE}$	CP	TC[1]	$\overline{RC}$
L	⊓	H	⊓
H	X	X	H
X	X	L	H

2616 tbl 06

MODE SELECT FUNCTION TABLE[2]

Inputs				
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	Mode
H	L	L	∫	Count Up
H	L	H	∫	Count Down
L	X	X	X	Preset (Asynchronous)
H	H	X	X	No Change (Hold)

2616 tbl 07

NOTES:
1. TC is generated internally.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, ∫ = LOW- to-HIGH clock transition.

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2616 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2616 tbl 02

1. This parameter is guaranteed at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = Vcc - 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = Vcc	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	-5(4)	
			V_I = GND	—	—	-5	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	Vcc	—	V
		Vcc = Min.	I_{OH} = -300µA	V_{HC}	Vcc	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min.	I_{OL} = 300µA	—	GND	V_{LC}(4)	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2616 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.0	2.8	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.2	3.8	
		V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	4.2	10.5[5]	

2616 tbl 04

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at VCC or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

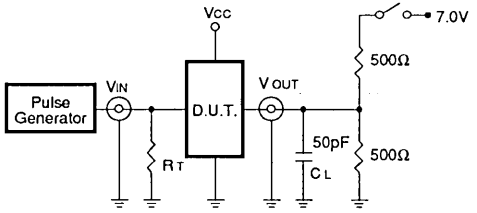
Symbol	Parameter	Condition[1]	IDT54/74FCT191				IDT54/74FCT191A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	2.5	12.0	1.5	16.0	2.5	7.8	1.5	10.5	ns
tPLH tPHL	Propagation Delay CP to TC		3.0	14.0	2.0	16.0	3.0	11.8	2.0	12.2	ns
tPLH tPHL	Propagation Delay CP to $\overline{RC}$		2.5	8.5	1.5	12.5	2.5	8.5	1.5	10.0	ns
tPLH tPHL	Propagation Delay $\overline{CE}$ to $\overline{RC}$		2.0	8.0	2.0	8.5	2.0	7.2	2.0	8.0	ns
tPLH tPHL	Propagation Delay $\overline{U}$/D to $\overline{RC}$		4.0	20.0	4.0	22.5	4.0	13.0	4.0	14.7	ns
tPLH tPHL	Propagation Delay $\overline{U}$/D to TC		3.0	11.0	3.0	13.0	3.0	7.2	3.0	8.5	ns
tPLH tPHL	Propagation Delay P_n to Q_n		2.0	14.0	1.5	16.0	2.0	9.1	1.5	10.4	ns
tPLH tPHL	Propagation Delay $\overline{PL}$ to Q_n		3.0	13.0	3.0	14.0	3.0	8.5	3.0	9.1	ns
tSU	Set-up Time, HIGH or LOW P_n to $\overline{PL}$		5.0	—	6.0	—	4.0	—	5.0	—	ns
tH	Hold Time, HIGH or LOW P_n to $\overline{PL}$		1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time LOW $\overline{CE}$ to CP		10.0	—	10.5	—	9.0	—	9.5	—	ns
tH	Hold Time LOW $\overline{CE}$ to CP		0	—	0	—	0	—	0	—	ns
tSU	Set-up Time, HIGH or LOW $\overline{U}$/D to CP		12.0	—	12.0	—	10.0	—	10.0	—	ns
tH	Hold Time, HIGH or LOW $\overline{U}$/D to CP		0	—	0	—	0	—	0	—	ns
tW	$\overline{PL}$ Pulse Width LOW		6.0	—	8.5	—	5.5	—	8.0	—	ns
tW	CP Pulse Width HIGH or LOW		5.0	—	7.0	—	4.0[3]	—	6.0	—	ns
tREM	Recovery Time $\overline{PL}$ to CP		6.0	—	7.5	—	5.0	—	6.5	—	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2616 tbl 08

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



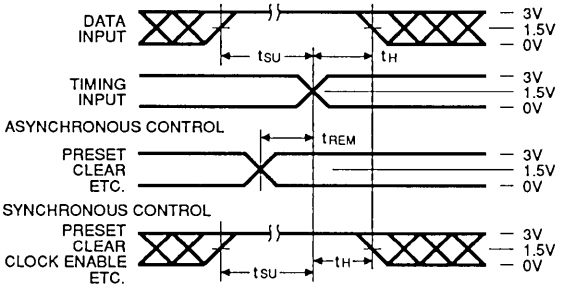
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

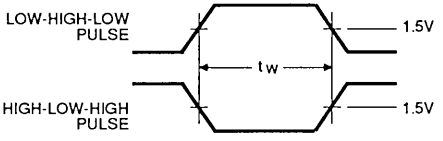
DEFINITIONS: 2616 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

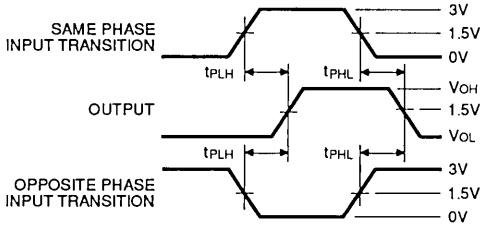
SET-UP, HOLD AND RELEASE TIMES



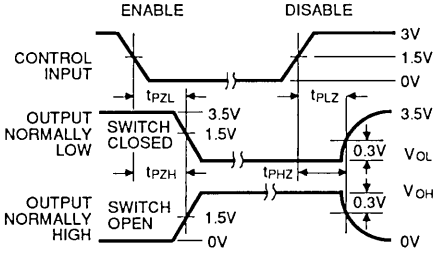
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

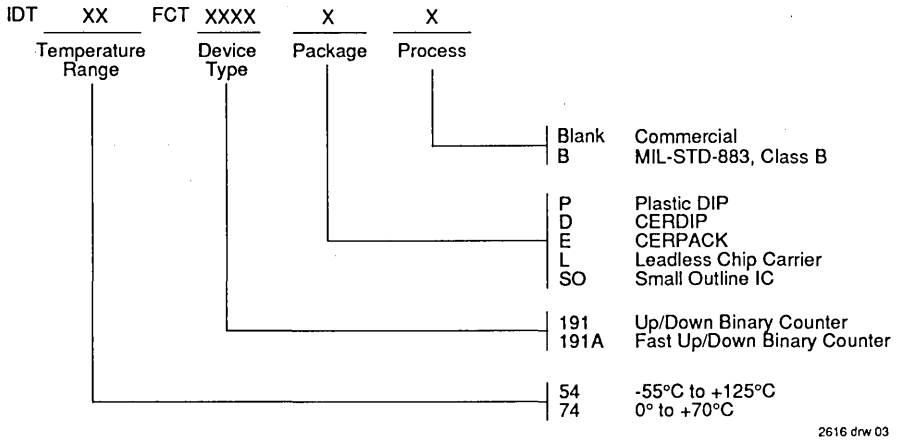


NOTES 2616 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2616 drw 03

Integrated Device Technology, Inc.

FAST CMOS UP/DOWN BINARY COUNTER

IDT54/74FCT193
IDT54/74FCT193A

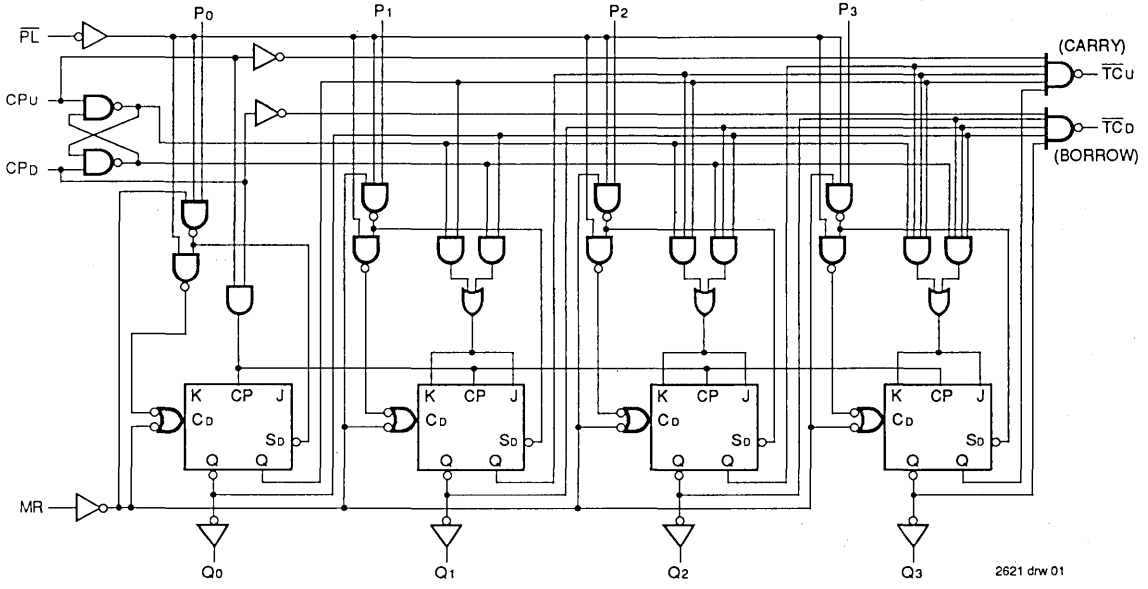
FEATURES:

- IDT54/74FCT193 equivalent to FAST™ speed
- **IDT54/74FCT193A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT193 and IDT54/74FCT193A are up/down modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. Separate count-up and count-down clocks are used and, in either counting mode, the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate terminal count-up and terminal count-down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multiusage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

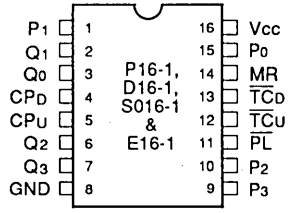
FUNCTIONAL BLOCK DIAGRAM



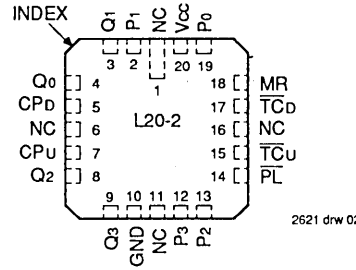
6

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
CPU	Count Up Clock Input (Active Rising Edge)
CPD	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
Pn	Parallel Data Inputs
Qn	Flip-Flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)

2621 tbl 05

FUNCTION TABLE[1]

MR	$\overline{PL}$	CPU	CPD	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↑	Count Down

NOTE: 2621 tbl 06

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM[3]	Terminal Voltage with Respect to GND	-0.5 to VCC	-0.5 to VCC	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTE: 2621 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals.
3. Output and I/O terminals.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE: 2621 tbl 02

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military; T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	-5[4]	
			V_I = GND	—	—	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2621 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND One Bit Toggling at f_i = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	4.2	10.5[5]	

2621 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT193				IDT54/74FCT193A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CPU or CPD to $\overline{TCU}$ or $\overline{TCD}$	CL = 50pF RL = 500Ω	2.0	10.0	2.0	10.5	2.0	6.5	2.0	6.9	ns
tPLH tPHL	Propagation Delay CPU or CPD to Qn		2.0	13.5	2.0	14.0	2.0	8.8	2.0	9.1	ns
tPLH tPHL	Propagation Delay Pn to Qn		2.0	15.5	2.0	16.5	2.0	10.1	2.0	10.8	ns
tPLH tPHL	Propagation Delay $\overline{PL}$ to Qn		2.0	14.0	2.0	13.5	2.0	8.8	2.0	9.1	ns
tPHL	Propagation Delay MR to Qn		3.0	15.5	3.0	16.0	3.0	10.1	3.0	10.4	ns
tPLH	Propagation Delay MR to $\overline{TCU}$		3.0	14.5	3.0	15.0	3.0	9.4	3.0	9.8	ns
tPHL	Propagation Delay MR to $\overline{TCD}$		3.0	15.5	3.0	16.0	3.0	10.1	3.0	10.4	ns
tPLH tPHL	Propagation Delay $\overline{PL}$ to $\overline{TCU}$ or $\overline{TCD}$		3.0	16.5	3.0	18.5	3.0	10.8	3.0	12.0	ns
tPLH tPHL	Propagation Delay Pn to $\overline{TCU}$ or $\overline{TCD}$		3.0	15.5	3.0	16.5	3.0	10.1	3.0	10.8	ns
tSU	Set-up Time, HIGH or LOW Pn to $\overline{PL}$		5.0	—	6.0	—	4.0	—	5.0	—	ns
tH	Hold Time, HIGH or LOW Pn to $\overline{PL}$		2.0	—	2.0	—	1.5	—	1.5	—	ns
tW	$\overline{PL}$ Pulse Width, LOW		6.0	—	7.5	—	5.0	—	6.5	—	ns
tW	CPU or CPD Pulse Width HIGH or LOW		5.0	—	7.0	—	4.0[3]	—	6.0	—	ns
tW	CPU or CPD Pulse Width LOW (Change of Direction)		10.0	—	12.0	—	8.0	—	10.0	—	ns
tW	MR Pulse Width HIGH		6.0	—	6.0	—	5.0	—	5.0	—	ns
tREM	Recovery Time $\overline{PL}$ to CPU or CPD		6.0	—	8.0	—	5.0	—	7.0	—	ns
tREM	Recovery Time MR to CPU or CPD		4.0	—	4.5	—	3.0	—	3.5	—	ns

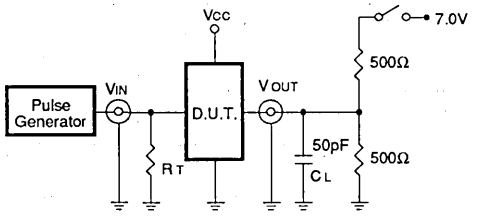
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2621 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



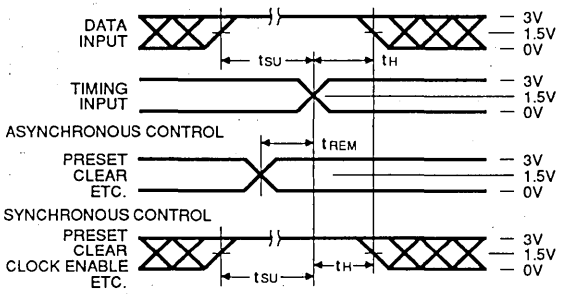
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

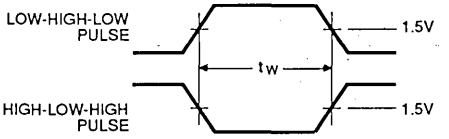
DEFINITIONS: 2621 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

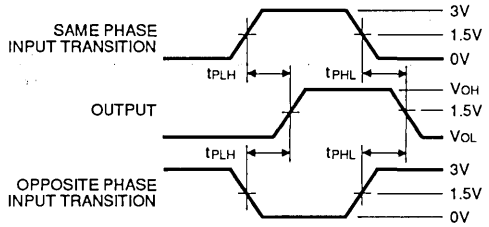
SET-UP, HOLD AND RELEASE TIMES



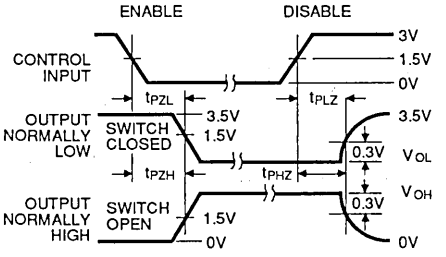
PULSE WIDTH



PROPAGATION DELAY



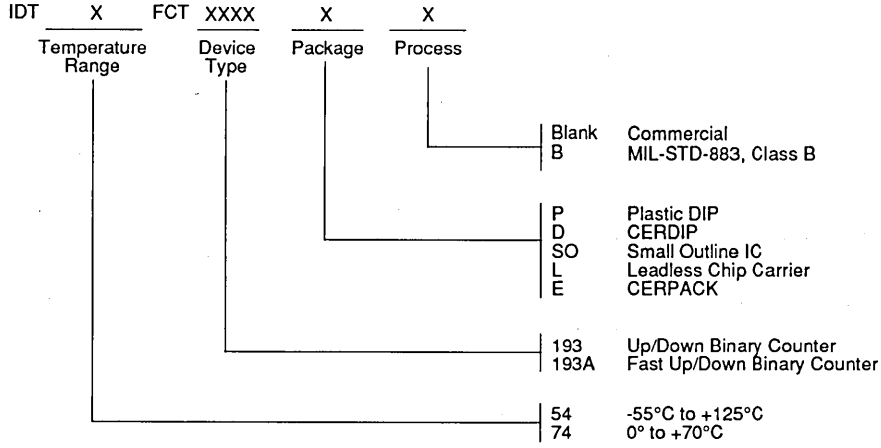
ENABLE AND DISABLE TIMES



NOTES 2621 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2621 drw 03

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT240/A/C
IDT54/74FCT241/A/C
IDT54/74FCT244/A/C
IDT54/74FCT540/A/C
IDT54/74FCT541/A/C

FEATURES:

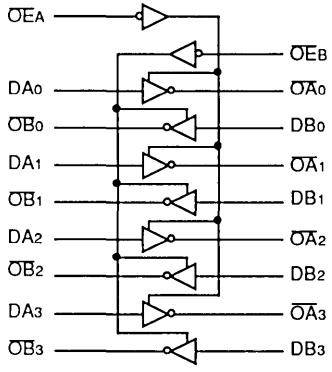
- IDT54/74FCT240/241/244/540/541 equivalent to FAST™ speed and drive
- **IDT54/74FCT240A/241A/244A/540A/541A 25% faster than FAST™**
- **IDT54/74FCT240C/241C/244C/540C/541C up to 55% faster than FAST™**
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications

DESCRIPTION:

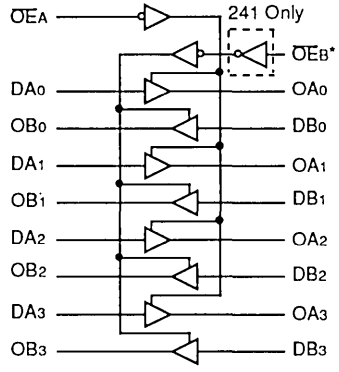
The IDT octal buffer/line drivers are built using advanced CEMOS™ a dual metal CMOS technology. The IDT54/74FCT240/A/C, IDT54/74FCT241/A/C and IDT54/74FCT244/A/C are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitter/receivers which provide improved board density.

The IDT54/74FCT540/A/C and IDT54/74FCT541/A/C are similar in function to the IDT54/74FCT240/A/C and IDT54/74FCT244/A/C, respectively, except that the inputs and outputs are on opposite sides of the package. This pinout arrangement makes these devices especially useful as output ports for microprocessors and as backplane drivers, allowing ease of layout and greater board density.

FUNCTIONAL BLOCK DIAGRAMS

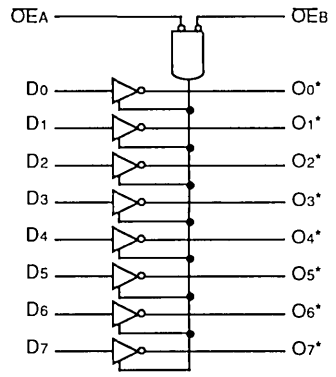


IDT54/74FCT240



IDT54/74FCT241/244

*$\overline{OE}_B$ for 241, $\overline{OE}_B$ for 244



IDT54/74FCT540/541

*Logic diagram shown for 'FCT540.
'FCT541 is the non-inverting option.

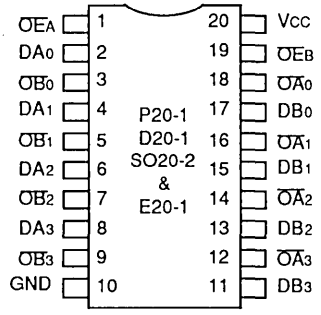
2606 dwg 01-03

CEMOS is a trademark of Integrated Device Technology, Inc.

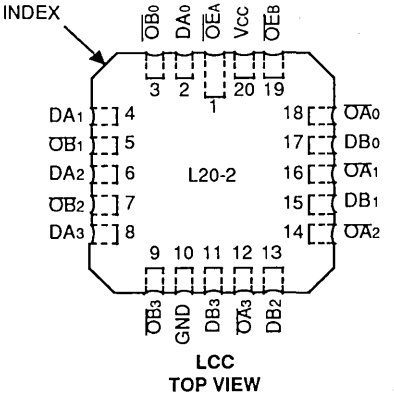
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS

IDT54/74FCT240

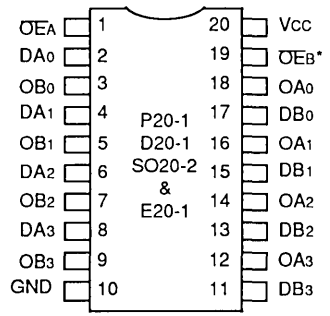


DIP/SOIC/CERPACK
TOP VIEW



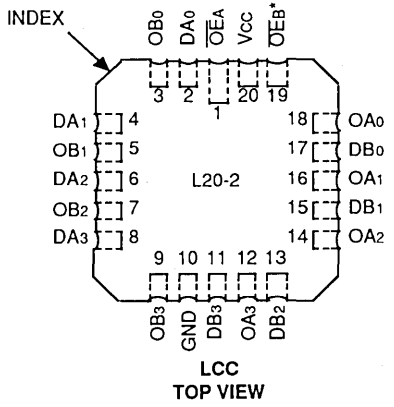
LCC
TOP VIEW

IDT54/74FCT241/244



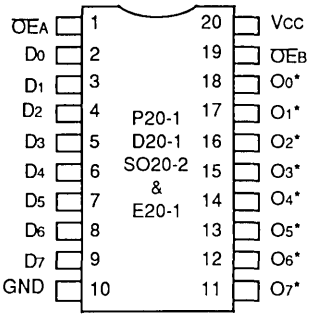
DIP/SOIC/CERPACK
TOP VIEW

*OE_B for 241, $\overline{OE}_B$ for 244



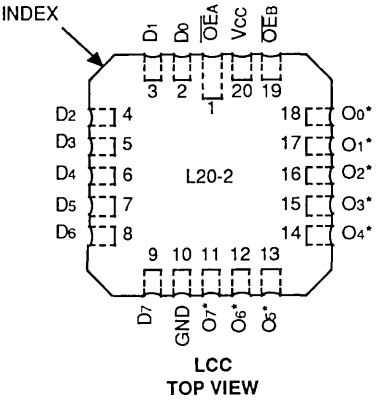
LCC
TOP VIEW

IDT54/74FCT540/541



DIP/SOIC/CERPACK
TOP VIEW

*Ox for 540, Ox for 541



LCC
TOP VIEW

2606 cnv* 04-09

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PIN DESCRIPTION

Pin Names	Description
$\overline{OE_A}$, $\overline{OE_B}$	3–State Output Enable Inputs (Active LOW)
OE_B[1]	3–State Output Enable Input (Active HIGH)
Dxx	Inputs
Oxx	Outputs

NOTE: 2606 tbl 04
1. OE_B for 241 only.

FUNCTION TABLE

Inputs[1]				Outputs[1]				
$\overline{OE_A}$	$\overline{OE_B}$	OE_B[2]	D	240	241	244	540	541
L	L	H	L	H	L	L	H	L
L	L	H	H	L	H	H	L	H
H	H	L	X	Z	Z	Z	Z	Z

NOTE: 2606 tbl 05
1. H = High Voltage Level
   X = Don't Care
   L = Low Voltage Level
   Z = High Impedance
2. OE_B for 241 only.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2606 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter [1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2606 tbl 02
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ. (2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5(4)	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10(4)	
I_{OZL}			V_O = 0.5V	—	—	–10(4)	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}(4)	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	

2606 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_A}$ = $\overline{OE_B}$ = GND or $\overline{OE_A}$ = GND, OE_B = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		$\overline{OE_A}$ = $\overline{OE_B}$ = GND or $\overline{OE_A}$ = GND, OE_B = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
		$\overline{OE_A}$ = $\overline{OE_B}$ = GND or $\overline{OE_A}$ = GND, OE_B = V_{CC} Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2606 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT240[1,2]

			54/74FCT240				54/74FCT240A				54/74FCT240C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.0	1.5	5.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	4.5	1.5	4.6	ns

2606 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT241 AND FCT244[1,2]

			54/74FCT241/244				54/74FCT241A/244A				54/74FCT241C/244C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

2606 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT540 AND FCT541[1,2]

			54/74FCT540/541				54/74FCT540A/541A				54/74FCT540C/541C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N IDT54/74FCT540	C_L = 50pF R_L = 500Ω	1.5	8.5	1.5	9.5	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N IDT54/74FCT541		1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

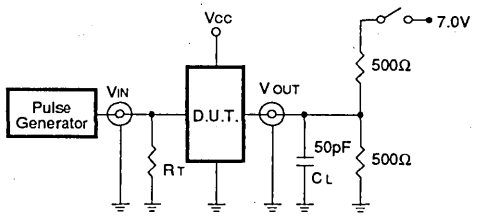
NOTES:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2606 tbl 09

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



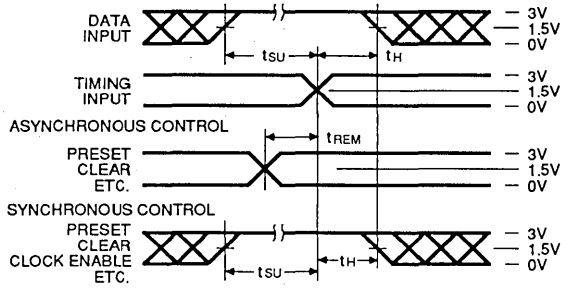
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

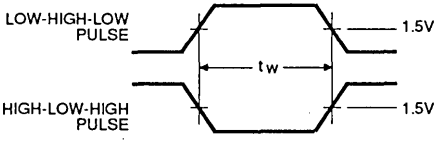
DEFINITIONS: 2606 tbl 10

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

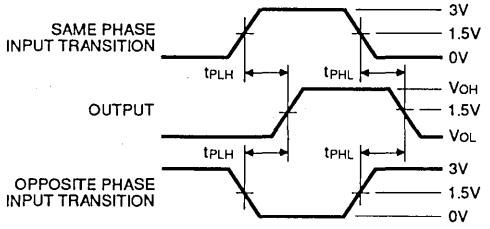
SET-UP, HOLD AND RELEASE TIMES



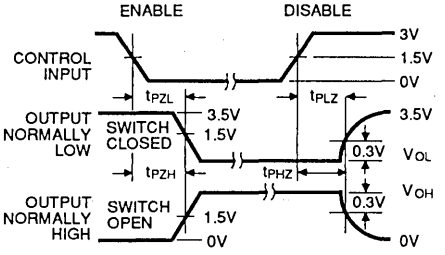
PULSE WIDTH



PROPAGATION DELAY



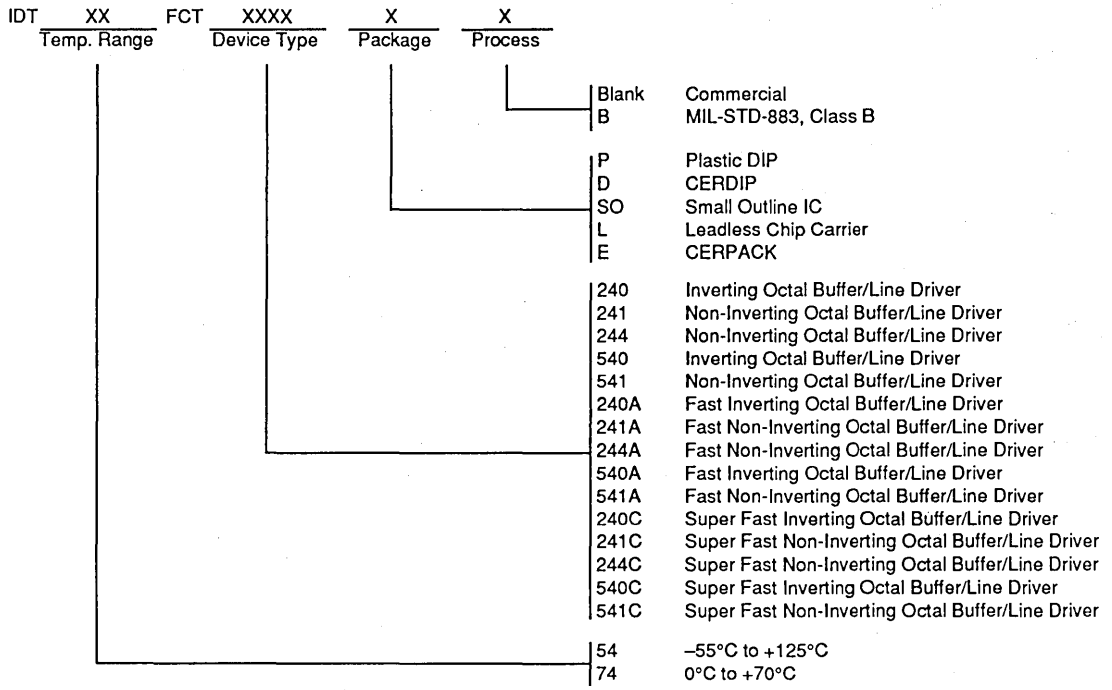
ENABLE AND DISABLE TIMES



NOTES 2606 drw 10

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2606 cnv* 15

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Integrated Device Technology, Inc.

FAST CMOS OCTAL BIDIRECTIONAL TRANSCEIVERS

IDT54/74FCT245/A/C
IDT54/74FCT640/A/C
IDT54/74FCT645/A/C

FEATURES:

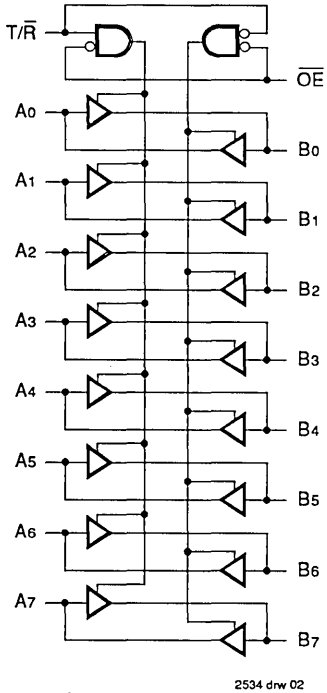
- IDT54/74FCT245/640/645 equivalent to FAST™ speed and drive
- **IDT54/74FCT245A/640A/645A 25% faster than FAST™**
- **IDT54/74FCT245C/640C/645C 40% faster than FAST™**
- TTL input and output level compatible
- CMOS output level compatible
- IOL = 64mA (commercial) and 48mA (military)
- Input current levels only 5μA max.
- CMOS power levels (2.5mW typical static)
- Direction control and over-riding 3-state control
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed
- Meets or exceeds JEDEC Standard 18 specifications

DESCRIPTION:

The IDT octal bidirectional transceivers are built using advanced CEMOS™, a dual-metal CMOS technology. The IDT54/74FCT245/A/C, IDT54/74FCT640/A/C and IDT54/74FCT645/A/C are designed for asynchronous two-way communication between data buses. The transmit/receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The IDT54/74FCT245/A/C and IDT54/74FCT645/A/C transceivers have non-inverting outputs. The IDT54/74FCT640/A/C has inverting outputs.

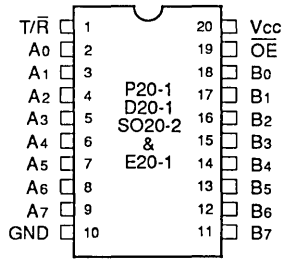
FUNCTIONAL BLOCK DIAGRAM



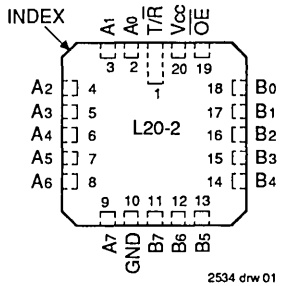
2534 drw 02

FCT245, 645 are non-inverting options.
FCT640 is the inverting option.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2534 drw 01

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-State Outputs
B_0–B_7	Side B Inputs or 3-State Outputs

2534 tbl 05

FUNCTION TABLE[2]

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A[1]
L	H	Bus A Data to Bus B[1]
H	X	High Z State

NOTE: 2534 tbl 06

1. 640 is inverting from input to output.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2534 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2534 tbl 02

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max	V_I = V_{CC}	—	—	15	µA
			V_I = 2.7V	—	—	15[4]	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	—	—	–15[4]	
			V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage (Port A and Port B)	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	

NOTES: 2534 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.5	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	2.0	4.0	mA
		50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.3	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.5	6.5[5]	
		50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.5	14.5[5]	

2534 tbl 04

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT245/A/C

			54/74FCT245				54/74FCT245A				54/74FCT245C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay A to B, B to A	C_L = 50 pF R_L = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	1.5	4.1	1.5	4.5	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tPZH tPZL	Output EnableTime T/$\overline{R}$ to A or B[3]		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

2534 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT640/A/C

			54/74FCT640				54/74FCT640A				54/74FCT640C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay A to B, B to A	C_L = 50 pF R_L = 500Ω	2.0	7.0	2.0	8.0	1.5	5.0	1.5	5.3	1.5	4.4	1.5	4.7	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		2.0	13.0	2.0	16.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		2.0	10.0	2.0	12.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to A or B[3]		2.0	13.0	2.0	16.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		2.0	10.0	2.0	12.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

2534 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT645/A/C

			54/74FCT645				54/74FCT645A				54/74FCT645C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay A to B, B to A	C_L = 50 pF R_L = 500Ω	1.5	9.5	1.5	11.0	1.5	4.6	1.5	4.9	1.5	4.1	1.5	4.5	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		1.5	11.0	1.5	12.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		1.5	12.0	1.5	13.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	11.0	1.5	12.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	12.0	1.5	13.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

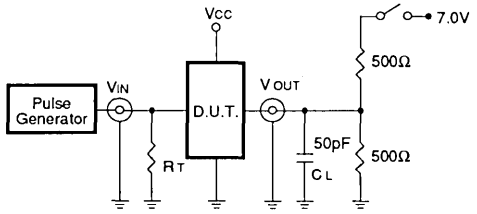
NOTES:

2534 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

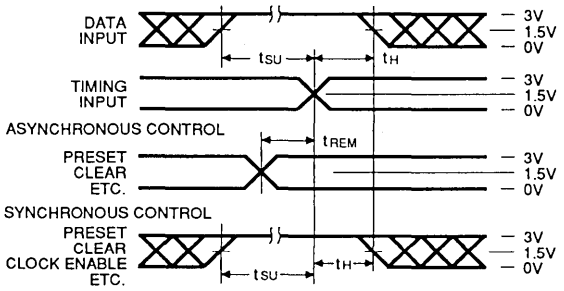
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2534 tbl 08

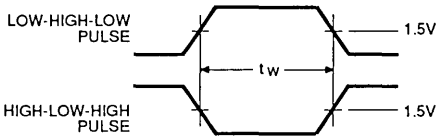
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

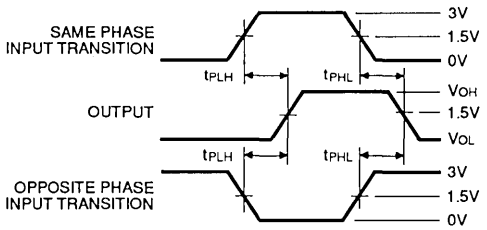
SET-UP, HOLD AND RELEASE TIMES



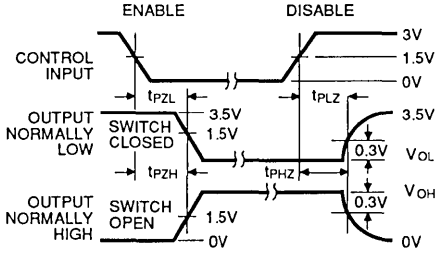
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



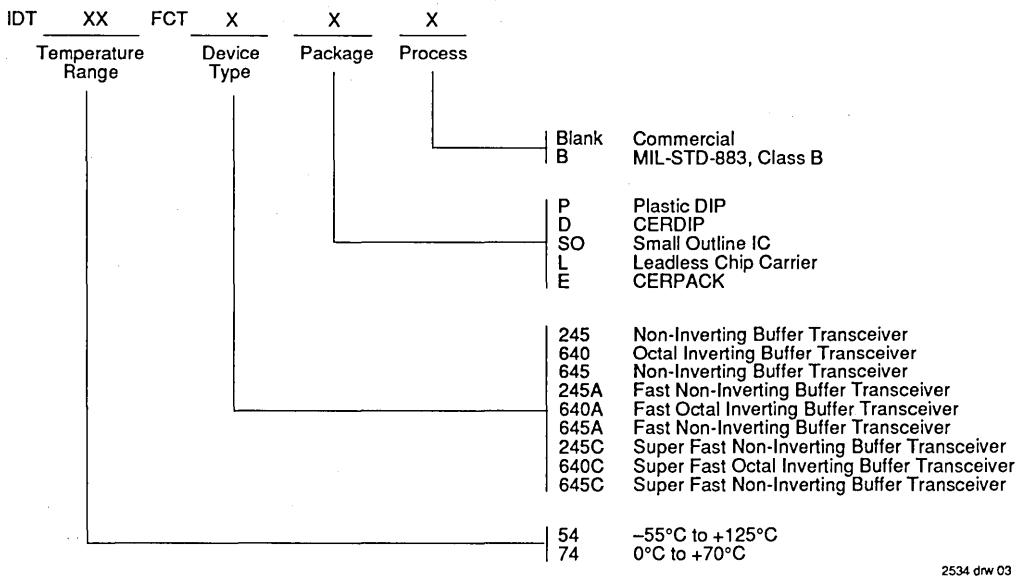
2534 drw 04

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2534 drw 03

Integrated Device Technology, Inc.

FAST CMOS OCTAL FLIP-FLOP WITH MASTER RESET

IDT54/74FCT273
IDT54/74FCT273A
IDT54/74FCT273C

FEATURES:

- IDT54/74FCT273 equivalent to FAST™ speed;
- **IDT54/74FCT273A 45%faster than FAST™**
- **IDT54/74FCT273C 55% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal D flip-flop with Master Reset
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

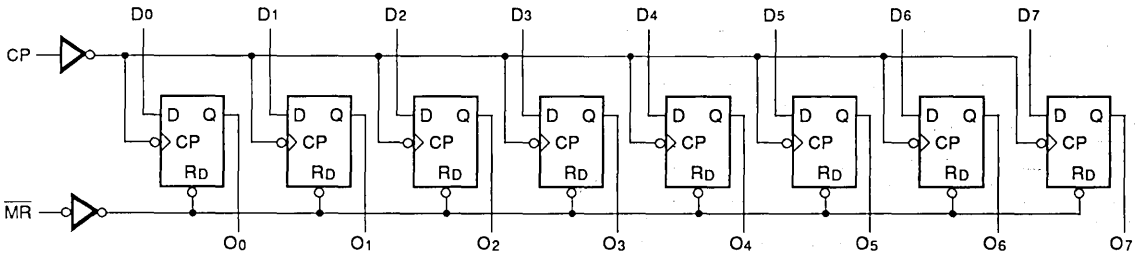
DESCRIPTION:

The IDT54/74FCT273/A/C are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT273/A/C have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

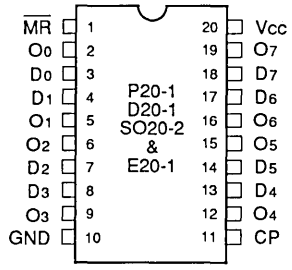
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

FUNCTIONAL BLOCK DIAGRAM

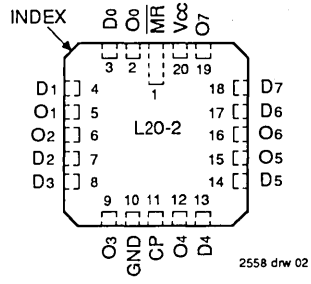


2558 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW



2558 drw 02

LCC TOP VIEW

CEMOS is a trademark of Integrated Device Techology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
D_N	Data Input
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
O_N	Data Outputs

2558 tbl 05

FUNCTION TABLE

	Inputs			Outputs
Operating Mode	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

2558 tbl 06

NOTES:
H = HIGH voltage level steady-state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

2558 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2558 tbl 02

NOTE:
1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2558 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{MR}$ = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{MR}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{MR}$ = V_{CC} Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2558 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at DH
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT273				IDT54/74FCT273A				IDT54/74FCT273C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Clock to Output	CL = 50 pF RL = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.8	2.0	6.5	ns
tPHL	Propagation Delay $\overline{MR}$ to Output		2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	6.1	2.0	6.8	ns
tSU	Set-up Time HIGH or LOW Data to CP		3.0	—	3.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Data to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tREM	Recovery Time $\overline{MR}$ to CP		4.0	—	5.0	—	2.0	—	2.5	—	2.0	—	2.5	—	ns

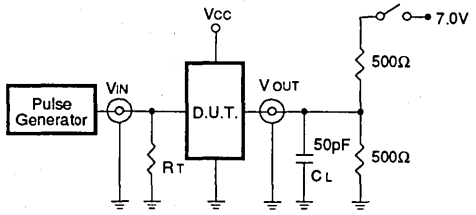
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2558 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



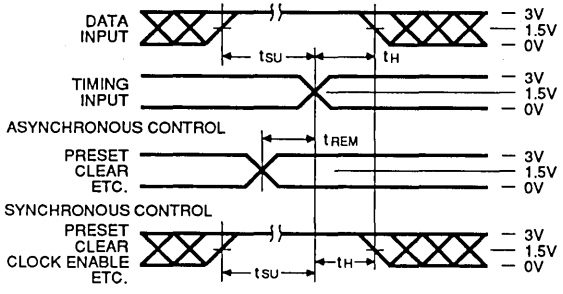
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

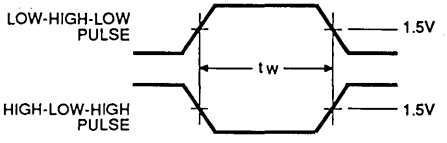
DEFINITIONS: 2558 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

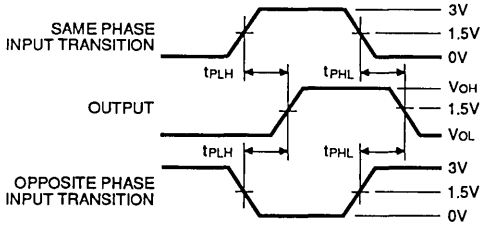
SET-UP, HOLD AND RELEASE TIMES



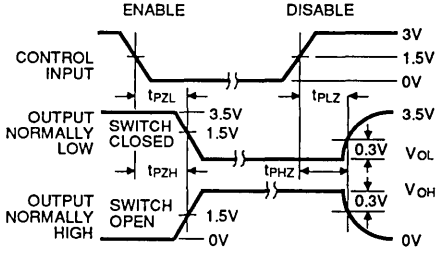
PULSE WIDTH



PROPAGATION DELAY



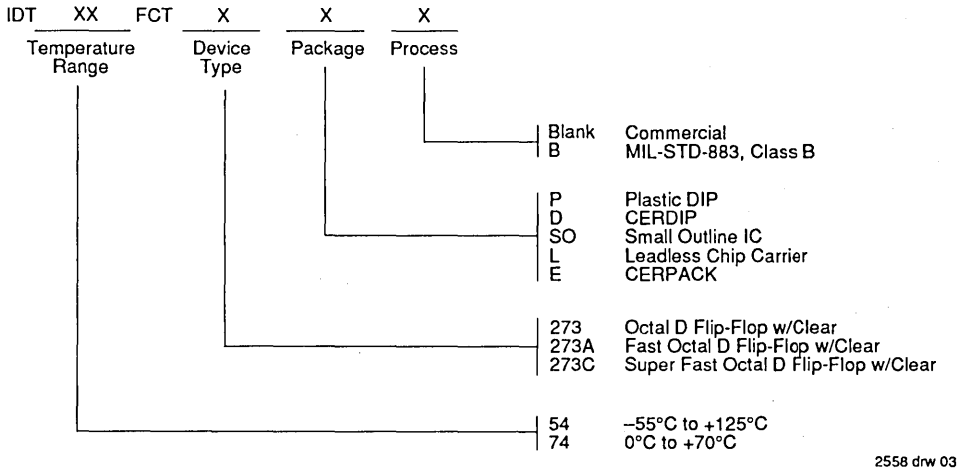
ENABLE AND DISABLE TIMES



NOTES 2558 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2558 drw 03

6

Integrated Device Technology, Inc.

FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74/FCT299
IDT54/74/FCT299A

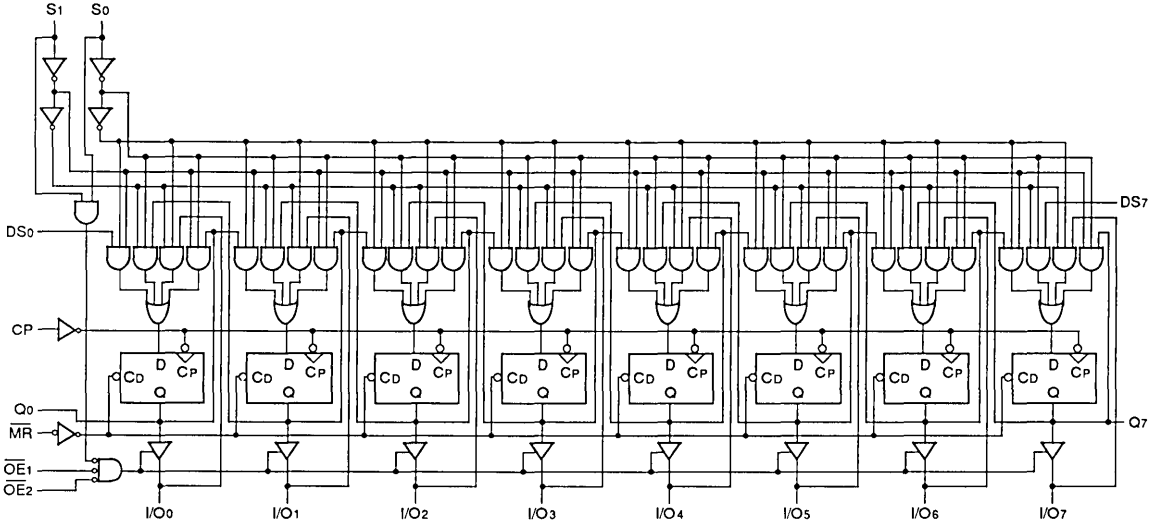
FEATURES:

- IDT54/74FCT299 equivalent to FAST™ speed
- **IDT54/74FCT299A 25% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 8-input universal shift register
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86862 is listed on this function. Refer to section 2

DESCRIPTION:

The IDT54/74FCT299 and IDT54/74FCT299A are built using advanced CEMOS™, a dual-metal CMOS technology. The IDT54/74FCT299 and IDT54/74FCT299A are 8-input universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

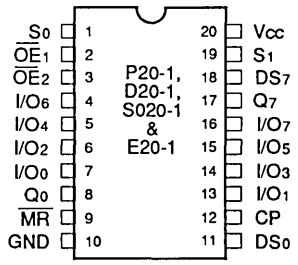
FUNCTIONAL BLOCK DIAGRAM



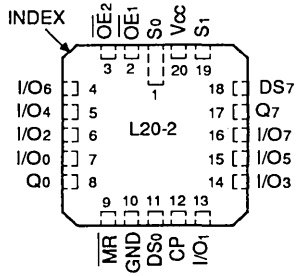
2561 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2561 drw 02

LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
CP	Clock Pulse Input (Active Edge Rising)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O_0–I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
Q_0, Q_7	Serial Outputs

2561 tbl 05

FUNCTION TABLE[1]

Inputs				
$\overline{MR}$	S_1	S_0	CP	Response
L	X	X	X	Asynchronous Reset Q_0–Q_7 = LOW
H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

NOTE: 2561 tbl 06

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2561 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5 unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2561 tbl 02

1. This parameter is guaranteed by characterization data and not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
	(Except I/O Pins)		V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
	(Except I/O Pins)		V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	15	µA
	(I/O Pins Only)		V_I = 2.7V	—	—	15[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–15[4]	
	(I/O Pins Only)		V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2561 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_1 = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_7 = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_7 = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2561 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at DH
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

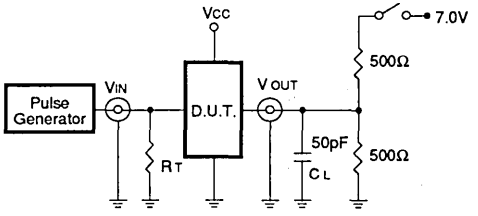
Symbol	Parameter	Condition[1]	IDT54/74FCT299				IDT54/74FCT299A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	14.0	2.0	7.2	2.0	9.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		2.0	12.0	2.0	12.0	2.0	7.2	2.0	9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		2.0	10.0	2.0	10.5	2.0	7.2	2.0	9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		2.0	15.0	2.0	15.0	2.0	8.7	2.0	11.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_n$ to I/O_n		1.5	11.0	1.5	15.0	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_n$ to I/O_n		1.5	7.0	1.5	9.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW S_0 or S_1 to CP		7.5	—	7.5	—	3.5	—	4.0	—	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		1.0	—	1.0	—	1.0	—	1.0	—	ns
t_{SU}	Set-up Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		5.5	—	5.5	—	4.0	—	4.5	—	ns
t_H	Hold Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns
t_W	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns
t_{REM}	Recovery Time $\overline{MR}$ to CP		7.0	—	7.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2561 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



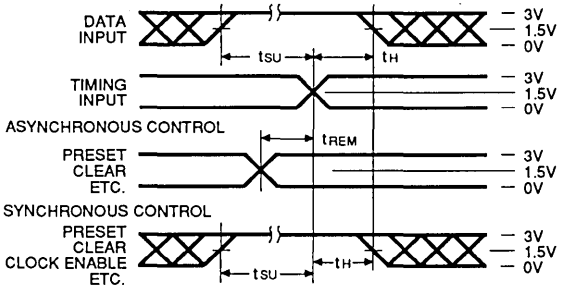
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

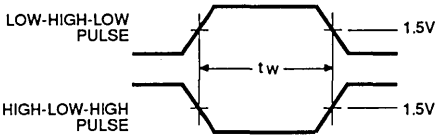
DEFINITIONS: 2561 tbl 08

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

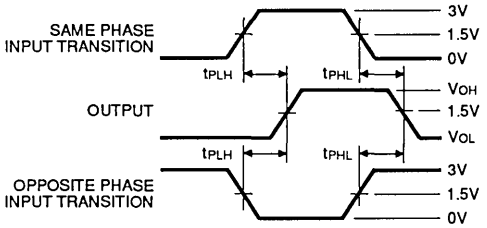
SET-UP, HOLD AND RELEASE TIMES



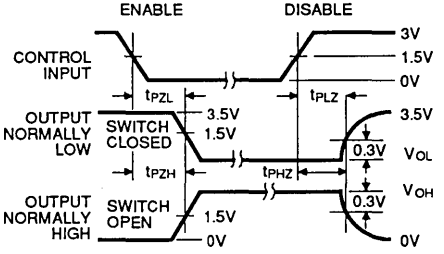
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

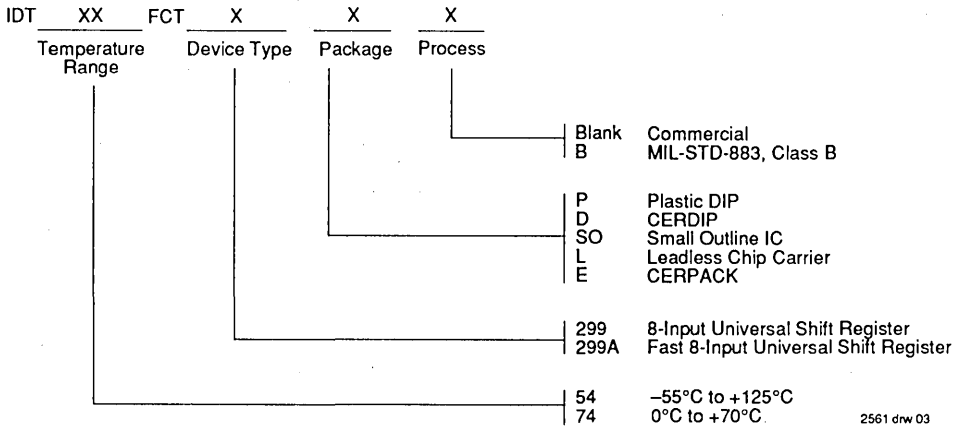


NOTES 2561 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tF ≤ 2.5ns; tR ≤ 2.5ns.

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCHES

IDT54/74FCT373/A/C
IDT54/74FCT533/A/C
IDT54/74FCT573/A/C

FEATURES

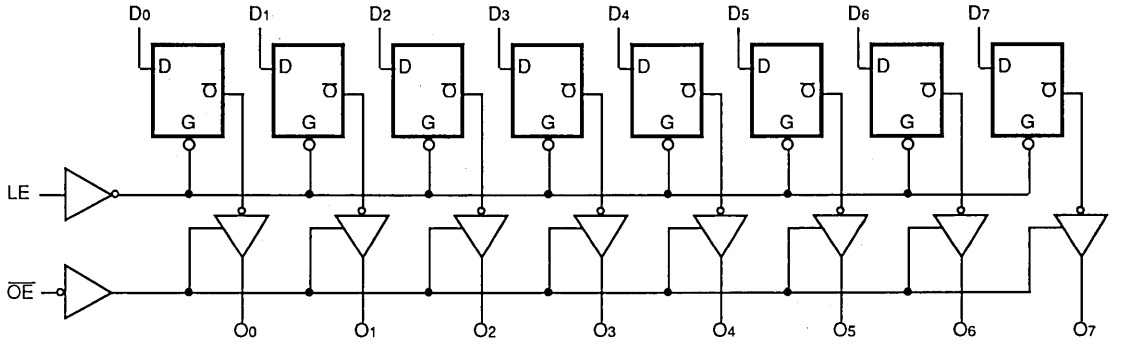
- IDT54/74FCT373/533/573 equivalent to FAST™ speed and drive
- **IDT54/74FCT373A/533A/573A up to 30% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Octal transparent latch with 3-state output control
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

The IDT54/74FCT373/A/C, IDT54/74FCT533/A/C and IDT54/74FCT573/A/C are octal transparent latches built using advanced CEMOS™, a dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

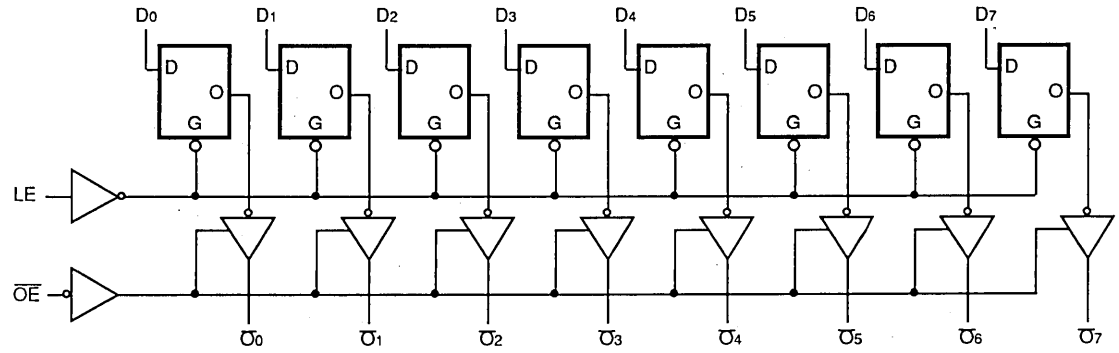
FUNCTIONAL BLOCK DIAGRAMS

IDT54/74FCT373 AND IDT54/74FCT573



2602 cnv* 01

IDT54/74FCT533

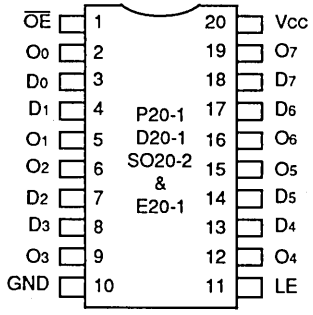


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

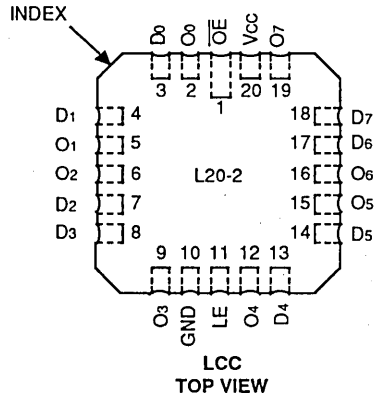
2602 cnv* 02

PIN CONFIGURATIONS

IDT54/74FCT373

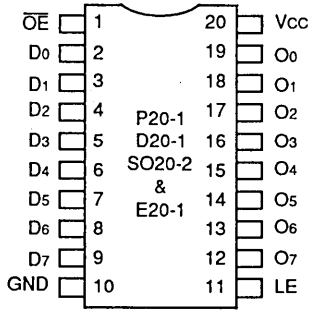


DIP/SOIC/CERPACK
TOP VIEW

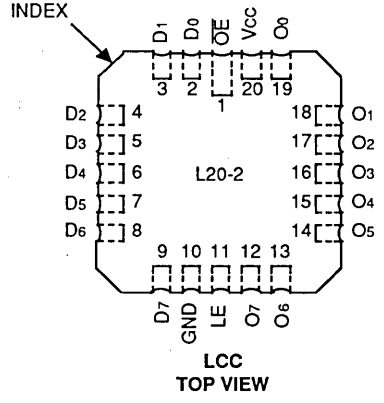


LCC
TOP VIEW

IDT54/74FCT573

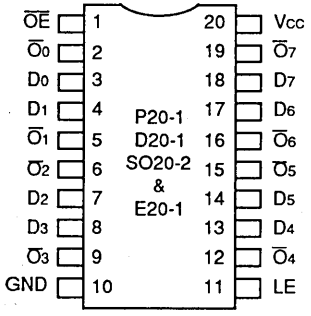


DIP/SOIC/CERPACK
TOP VIEW

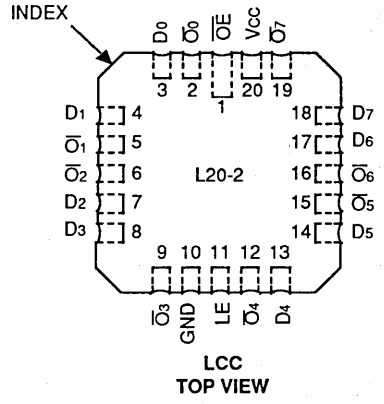


LCC
TOP VIEW

IDT54/74FCT533



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

2602 cnv* 03-08

FUNCTION TABLE (FCT533)[1]

Inputs			Outputs
Dn	LE	$\overline{OE}$	$\overline{On}$
H	H	L	L
L	H	L	H
X	X	H	Z

2602 tbl 05

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance

FUNCTION TABLE (FCT373 and FCT573)[1]

Inputs			Outputs
Dn	LE	$\overline{OE}$	On
H	H	L	H
L	H	L	L
X	X	H	Z

2602 tbl 06

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance

PIN DESCRIPTION

Pin Names	Description
Dn	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
On	3-State Outputs
$\overline{On}$	Complementary 3-State Outputs

2602 tbl 07

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

2602 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2602 tbl 02

NOTE:
1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10[4]	
I_{OZL}			V_O = 0.5V	—	—	–10[4]	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2602 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
		50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2602 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT373/A/C/FCT573/A/C

Symbol	Parameter	Conditions[1]	FCT373/573				FCT373A/573A				FCT373C/573C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Dn to On	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	1.5	4.2	1.5	5.1	ns
tPLH tPHL	Propagation Delay LE to On		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	2.0	5.5	2.0	8.0	ns
tPZH tPZL	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
tPHZ tPLZ	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
tSU	Set-up Time HIGH or LOW, Dn to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, Dn to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

2602 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT533/A/C

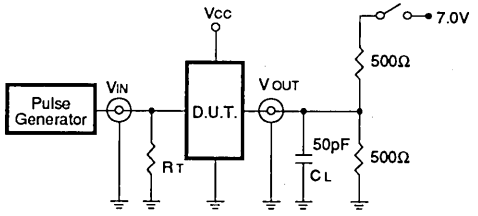
Symbol	Parameter	Conditions[1]	FCT533				FCT533A				FCT533C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Dn to $\overline{On}$	CL = 50pF RL = 500Ω	1.5	10.0	1.5	12.0	1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1	ns
tPLH tPHL	Propagation Delay LE to $\overline{On}$		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.8	2.0	6.9	2.0	8.0	ns
tPZH tPZL	Output Enable Time		1.5	11.0	1.5	12.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
tPHZ tPLZ	Output Disable Time		1.5	7.0	1.5	8.5	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
tSU	Set-up Time HIGH or LOW, Dn to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, Dn to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2602 tbl 09

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



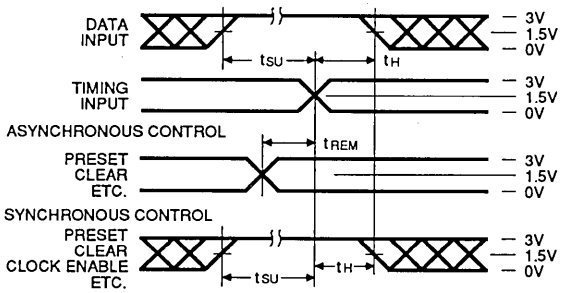
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

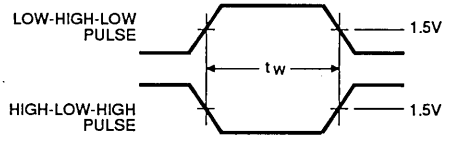
DEFINITIONS: 2537 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

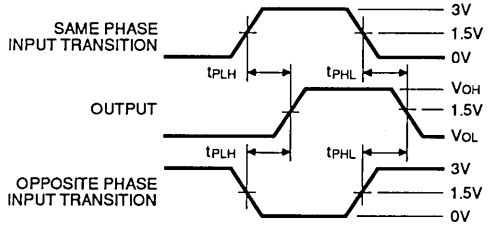
SET-UP, HOLD AND RELEASE TIMES



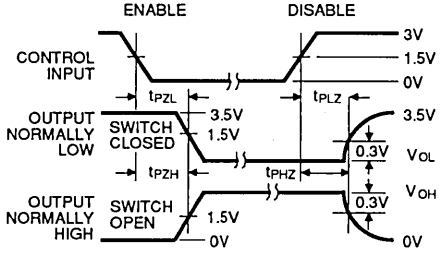
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

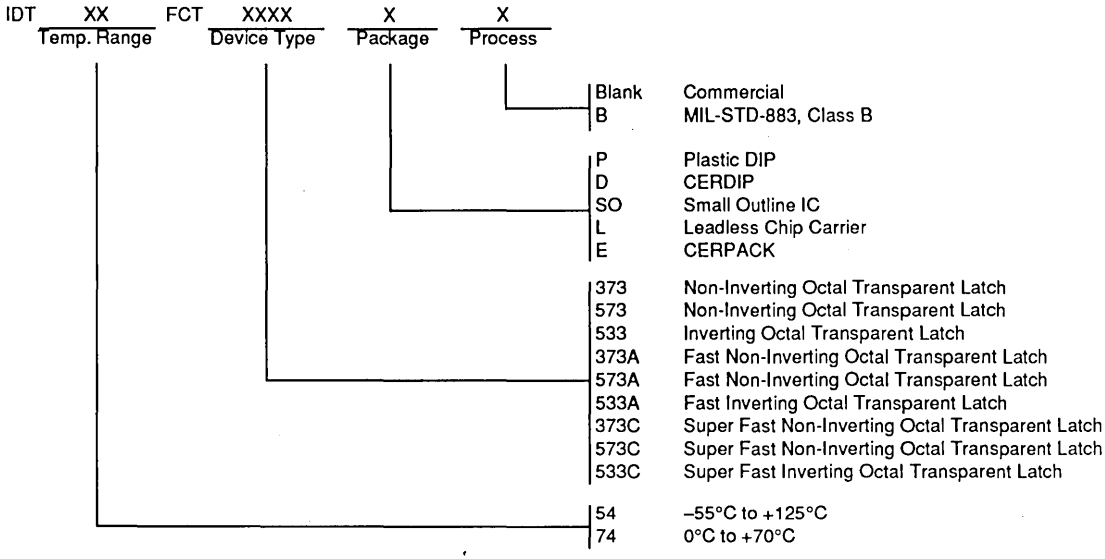


NOTES 2537 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2602 cnv' 14

Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTERS (3-STATE)

IDT54/74FCT374/A/C
IDT54/74FCT534/A/C
IDT54/74FCT574/A/C

FEATURES:

- IDT54/74FCT374/534/574 equivalent to FAST™ speed and drive
- **IDT54/74FCT374A/534A/574A up to 30% faster than FAST™**
- **IDT54/74FCT374C/534C/574C up to 50% faster than FAST™**
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Edge triggered master/slave, D-type flip-flops
- Buffered common clock and buffered common three-state control
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications

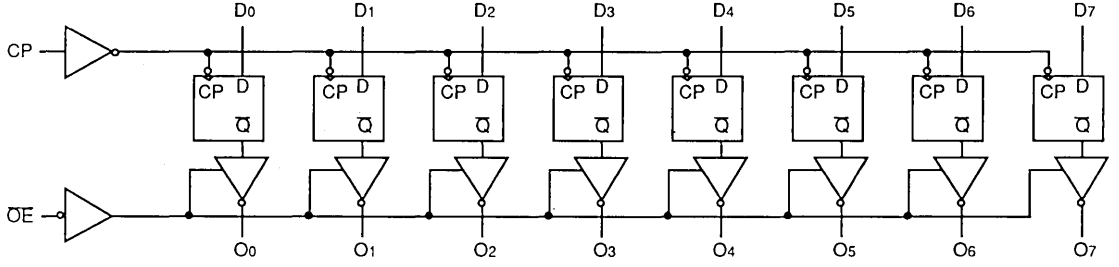
DESCRIPTION:

The IDT54/74FCT374/A/C, IDT54/74FCT534/A/C and IDT54/74FCT574/A/C are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable ($\overline{OE}$) is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high-impedance state.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

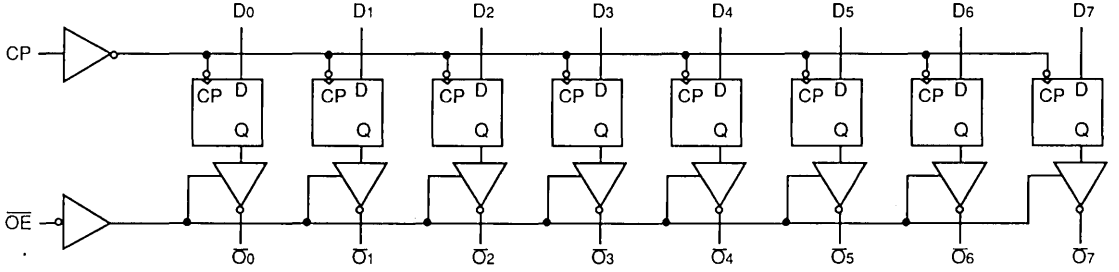
The IDT54/74FCT374/A/C and IDT54/74FCT574/A/C have non-inverting outputs with respect to the data at the D inputs. The IDT54/74FCT534/A/C have inverting outputs.

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT374 AND IDT54/74FCT574



2603 cnv* 01

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT534



2603 cnv* 02

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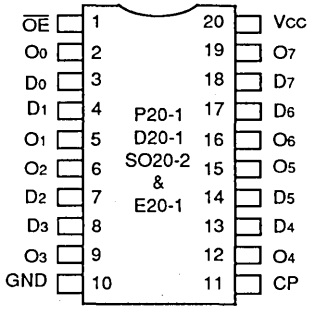
FAST is a trademark of Fairchild Semiconductor, Inc.

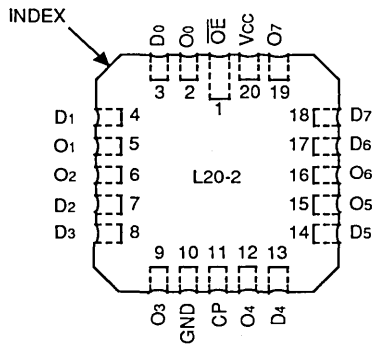
PIN CONFIGURATIONS

IDT54/74FCT374



2603 cnv* 03

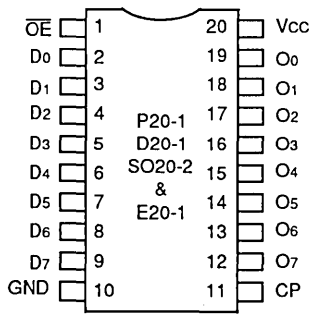
DIP/SOIC/CERPACK
TOP VIEW



2603 cnv* 04

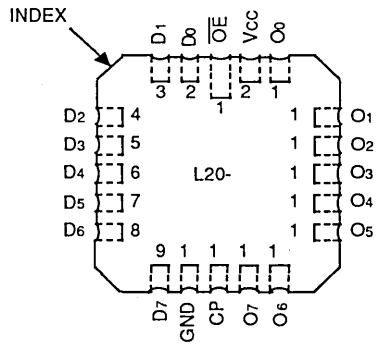
LCC
TOP VIEW

IDT54/74FCT574



2603 cnv* 05

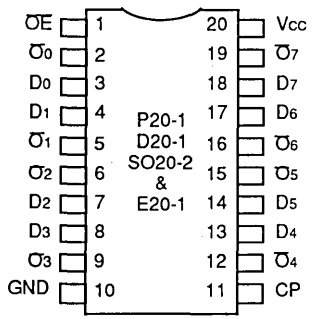
DIP/SOIC/CERPACK
TOP VIEW



2603 cnv* 06

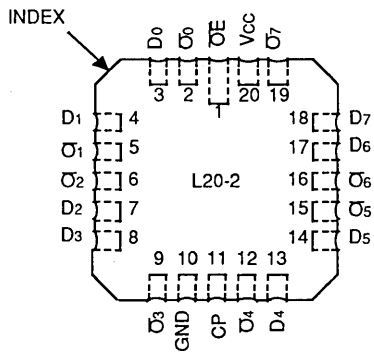
LCC
TOP VIEW

IDT54/74FCT534



2603 cnv* 07

DIP/SOIC/CERPACK
TOP VIEW



2603 cnv* 08

LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
D_N	D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition.
O_N	3-state outputs, (true).
$\overline{O_N}$	3-state outputs, (inverted).
$\overline{OE}$	Active LOW 3-state Output Enable input.

2603 tbl 06

FUNCTION TABLE[1]

Function	Inputs			FCT534 Outputs	FCT534 Internal	FCT374/574 Outputs	FCT374/574 Internal
	$\overline{OE}$	CP	D_N	$\overline{O_N}$	Q_N	O_N	$\overline{Q_N}$
Hi-Z	H	L	X	Z	NC	Z	NC
	H	H	X	Z	NC	Z	NC
Load Register	L	↑	L	H	L	L	H
	L	↑	H	L	H	H	L
	H	↑	L	Z	L	Z	H
	H	↑	H	Z	H	Z	L

2603 tbl 05

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance
   NC = No Change
   ↑ = LOW-to-HIGH transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

2603 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2603 tbl 02

NOTE:
1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10[4]	
I_{OZL}			V_O = 0.5V	—	—	–10[4]	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:

2603 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		$\overline{OE}$ = GND f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
		$\overline{OE}$ = GND Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2603 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

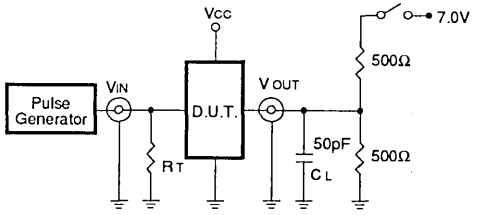
Symbol	Parameter	Conditions[1]	FCT374/534/574				FCT374A/534A/574A				FCT374C/534C/574C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N[3]	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	2.0	5.2	2.0	6.2	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.7	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to CP		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, D_N to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. O_N for FCT374 and FCT574, O_N for FCT534.

2603 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



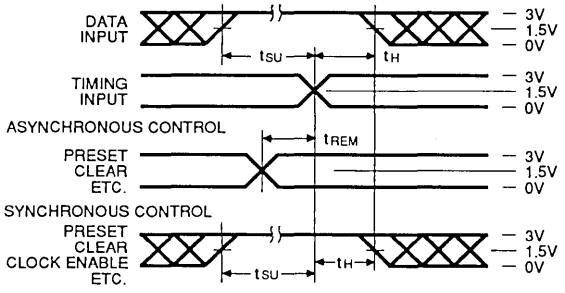
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

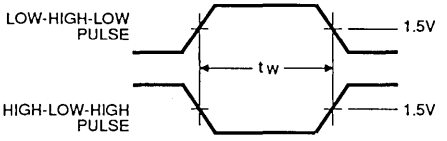
DEFINITIONS: 2603 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

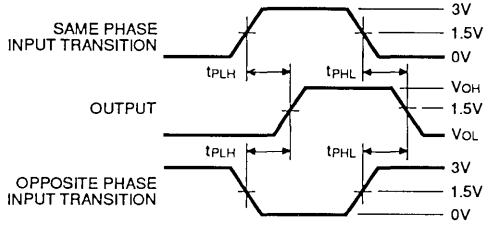
SET-UP, HOLD AND RELEASE TIMES



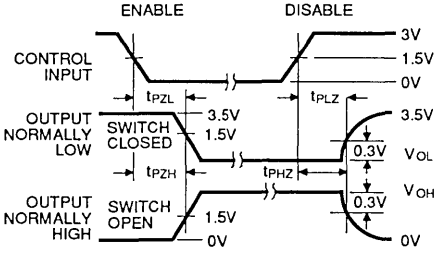
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

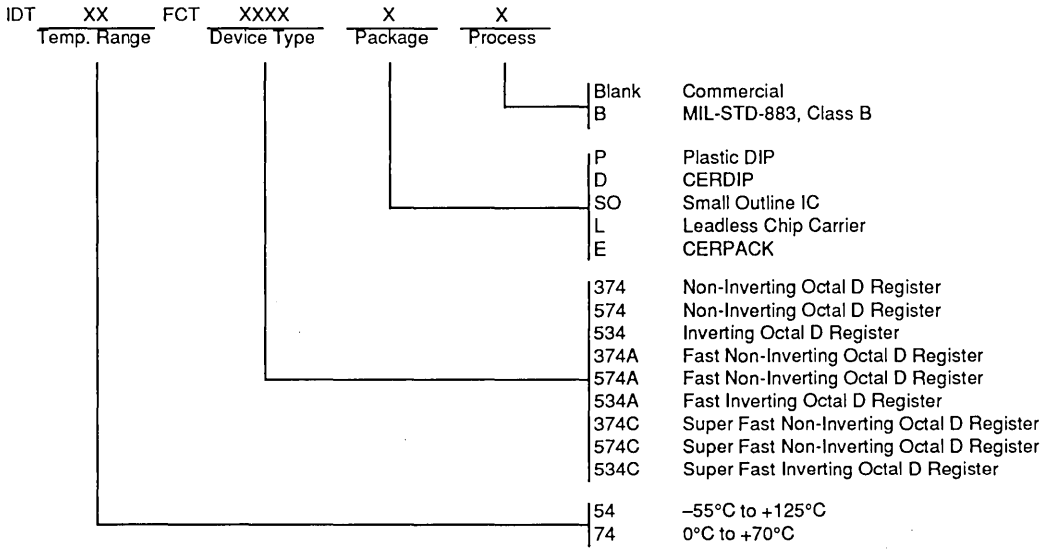


NOTES 2603 drw 15

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2603 cnv* 14

Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74FCT377
IDT54/74FCT377A
IDT54/74FCT377C

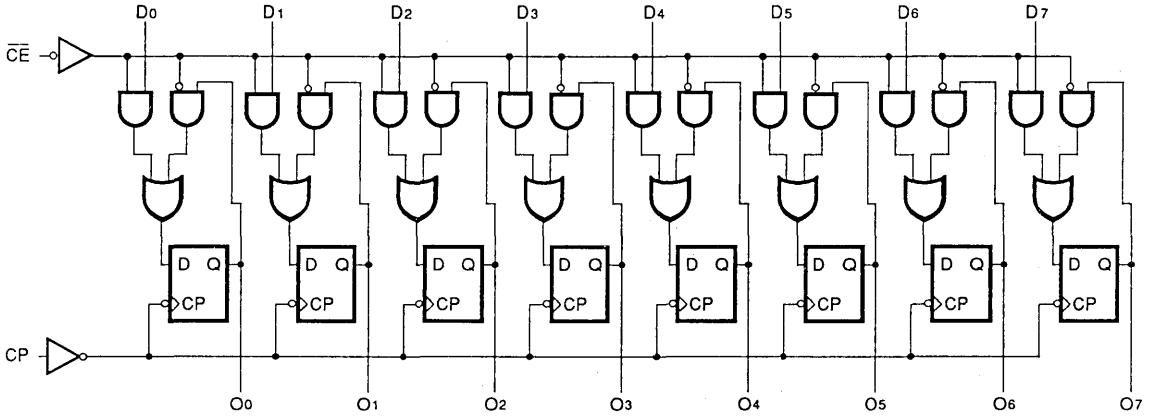
FEATURES:

- IDT54/74FCT377 equivalent to FAST™ speed
- **IDT54/74FCT377A 25% faster than FAST™**
- **IDT54/74FCT377C 40% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- I_{IH} and I_{IL} only 5µA max.
- CMOS power levels (1mW typ. static)
- CMOS output level compatible
- Meets or exceeds JEDEC Standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

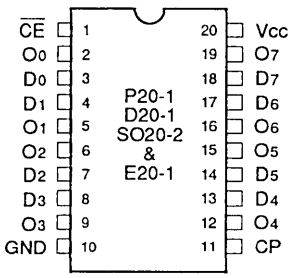
The IDT54/74FCT377/A/C is an octal D flip-flop built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT377/A/C have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

FUNCTIONAL BLOCK DIAGRAM

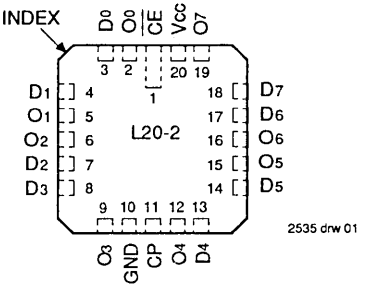


2535 drw 02

PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW



2535 drw 01

LCC TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
O_0–O_7	Data Outputs
CP	Clock Pulse Input

2535 tbl 05

FUNCTION TABLE[1]

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D	O
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	H	H	X	No Change

2535 tbl 06

NOTE:
1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock Transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition
   X = Immaterial
   ↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

2535 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2535 tbl 02

NOTE:
1. This parameter is guaranteed but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2535 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{CE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2535 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT377				IDT54/74FCT377A				IDT54/74FCT377C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to On	C_L = 50pF R_L = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.2	2.0	5.5	ns
tSU	Set-up Time HIGH or LOW Dn to CP		2.5	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Dn to CP		2.0	—	2.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW $\overline{CE}$ to CP		4.0	—	4.0	—	3.5	—	3.5	—	3.5	—	3.5	—	ns
tH	Hold Time HIGH or LOW $\overline{CE}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width, HIGH or LOW		7.0	—	7.0	—	6.0	—	7.0	—	6.0	—	7.0	—	ns

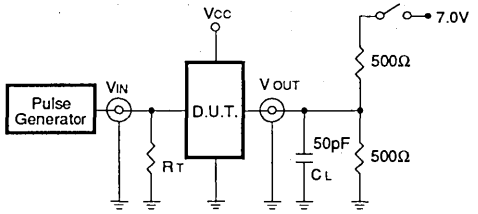
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2535 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

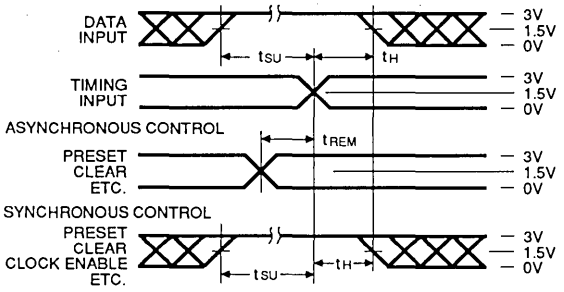
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2535 tbl 08

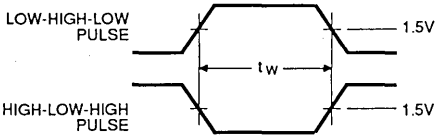
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

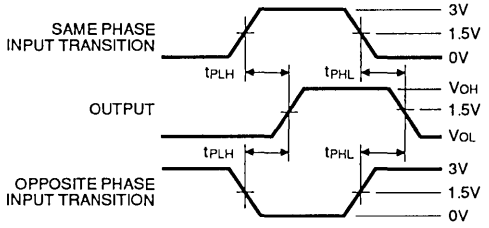
SET-UP, HOLD AND RELEASE TIMES



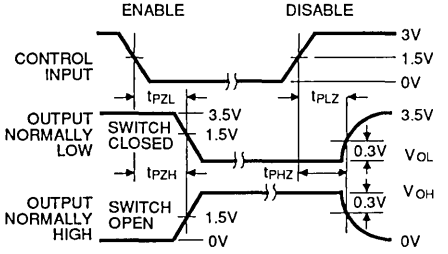
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

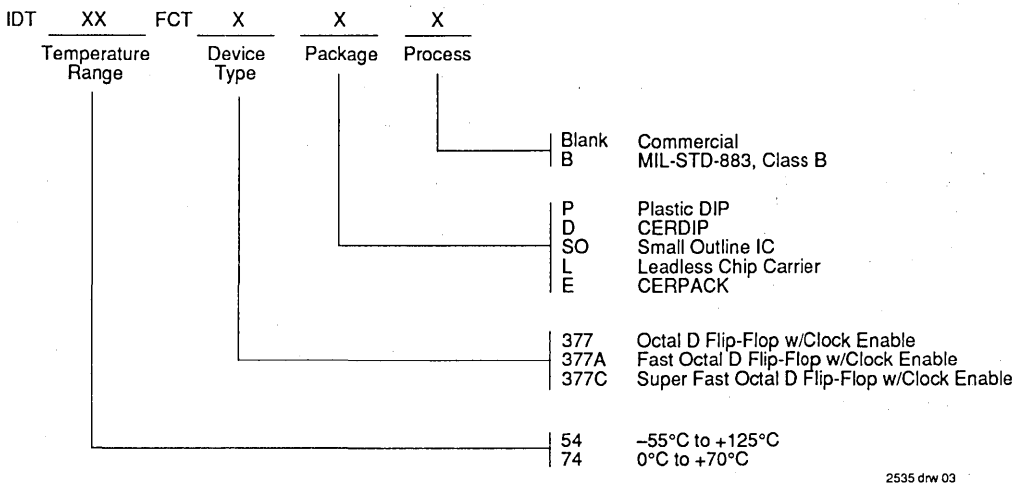


2535 drw 04

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

FAST CMOS QUAD DUAL-PORT REGISTER

IDT54/74FCT399
IDT54/74FCT399A

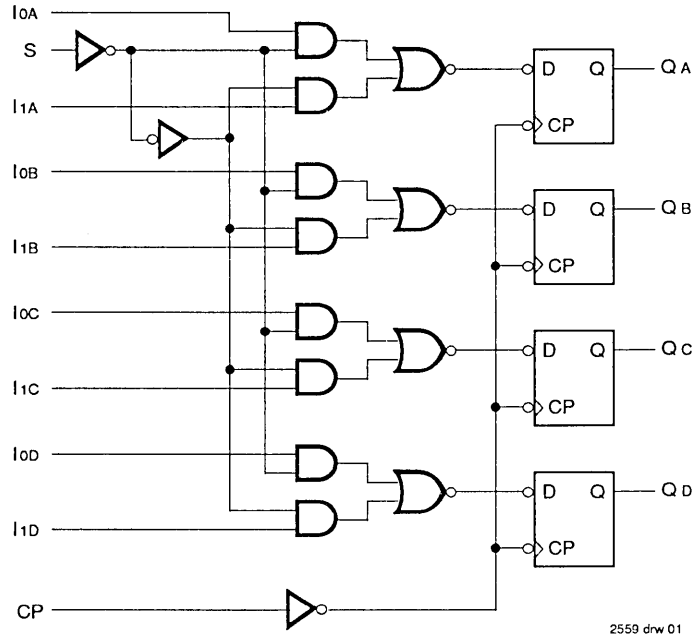
FEATURES:

- IDT54/74FCT399 equivalent to FAST™ speed
- **IDT54/74FCT399A 30% faster than FAST™**
- Equivalent to FAST™ pinout/function and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Available in 16-pin DIP and SOIC, and 20-pin LCC
- Product avilable in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

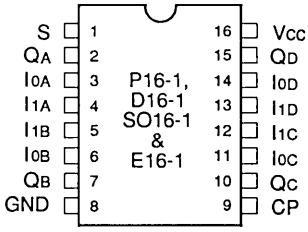
The IDT54/74FCT399/A is a high-speed quad dual-port register. The register selects four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0X}, I_{1X}) and Select input (S) must be stable only one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input for predictable operation.

FUNCTIONAL BLOCK DIAGRAM

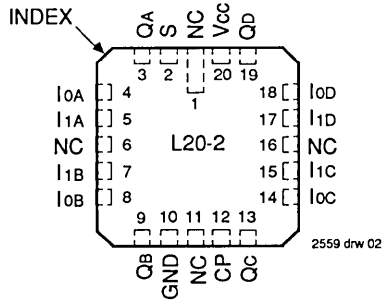


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
S	Common Select Input
CP	Clock Pulse Input (Active Rising Edge)
I_{0A} – I_{0D}	Data Inputs from Source 0
I_{1A} – I_{1D}	Data Inputs from Source 1
Q_A – Q_D	Register True Outputs

2559 tbl 03

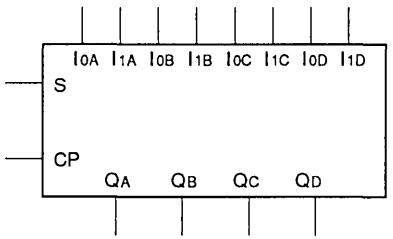
FUNCTION TABLE[1]

Inputs			Outputs
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

2559 tbl 04

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
   l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
   X = Immaterial

LOGIC SYMBOL



2559 drw 03

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2559 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2559 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = Vcc – 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = Vcc	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	-5(4)	
			V_I = GND	—	—	-5	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	Vcc	—	V
		Vcc = Min.	I_{OH} = –300µA	V_{HC}	Vcc	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min.	I_{OL} = 300µA	—	GND	V_{LC}(4)	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2559 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle One Bit Toggling at f_i = 5MHz 50% Duty Cycle S = Steady State	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle Four Bits Toggling at f_i = 5MHz 50% Duty Cycle S = Steady State	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	12.8[5]	

2559 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

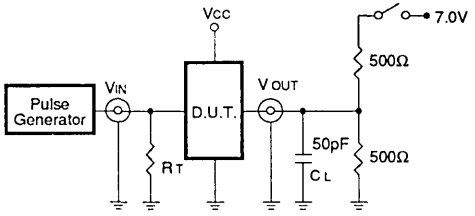
Symbol	Parameter	Condition[1]	IDT54/74FCT399				IDT54/74FCT399A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	3.0	10.0	3.0	11.5	2.5	7.0	2.5	7.5	ns
t_{SU}	Set-up Time HIGH or LOW I_n to CP		4.0	—	4.5	—	3.5	—	4.0	—	ns
t_H	Hold Time HIGH or LOW I_n to CP		1.0	—	1.5	—	1.0	—	1.0	—	ns
t_{SU}	Set-up Time HIGH or LOW S to CP		9.0	—	9.5	—	8.5	—	9.0	—	ns
t_H	Hold Time HIGH or LOW S to CP		0	—	0	—	0	—	0	—	ns
t_W	CP Pulse Width HIGH or LOW		5.0	—	7.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2559 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



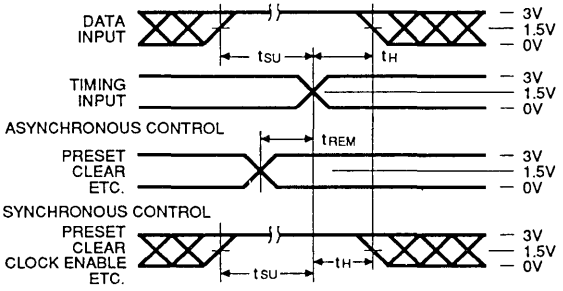
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

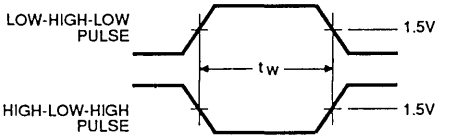
DEFINITIONS: 2559 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

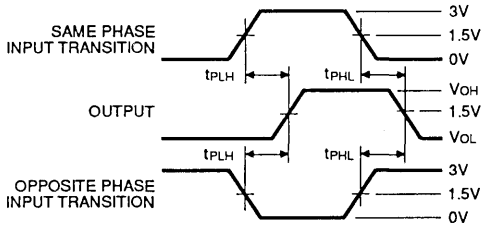
SET-UP, HOLD AND RELEASE TIMES



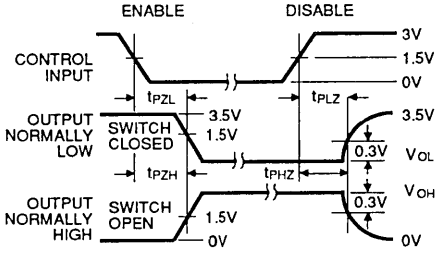
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

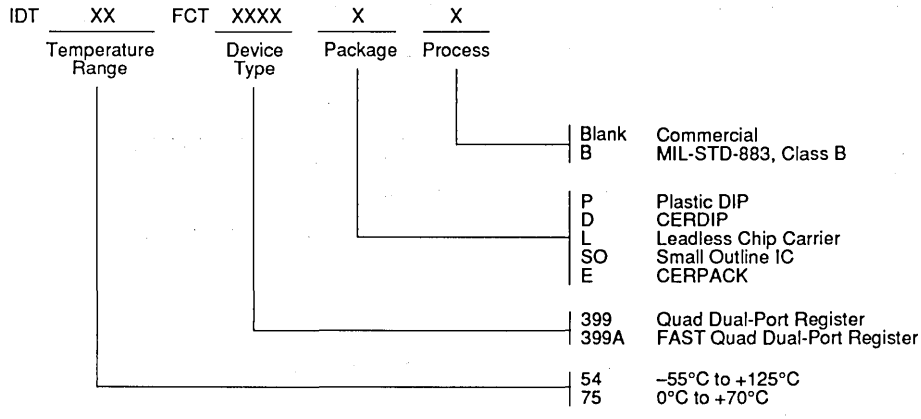


NOTES 2559 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2559 drw 04

Integrated Device Technology, Inc.

FAST CMOS 8-BIT IDENTITY COMPARATOR

IDT54/74FCT521
IDT54/74FCT521A
IDT54/74FCT521B
IDT54/74FCT521C

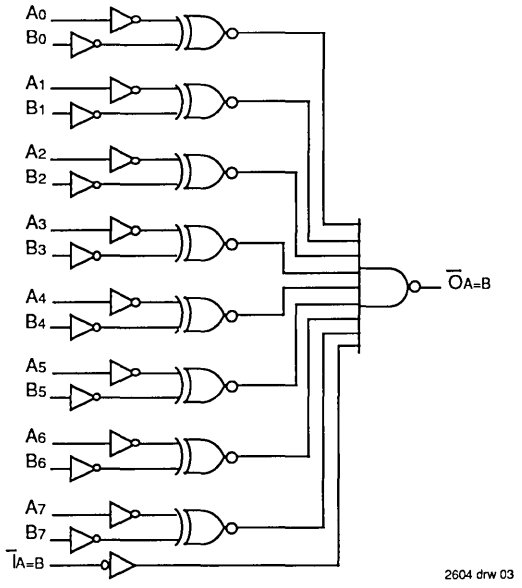
FEATURES:

- IDT54/74FCT521 equivalent to FAST™ speed
- **IDT54/74FCT521A 35% faster than FAST™**
- **IDT54/74FCT521B 50% faster than FAST™**
- **IDT54/74FCT521C 60% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial), and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

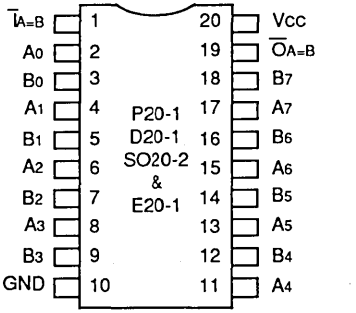
The IDT54/74FCT521/A/B/C are 8-bit identity comparators built using advanced CEMOS™, a dual metal CMOS technology. These devices compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

FUNCTIONAL BLOCK DIAGRAM



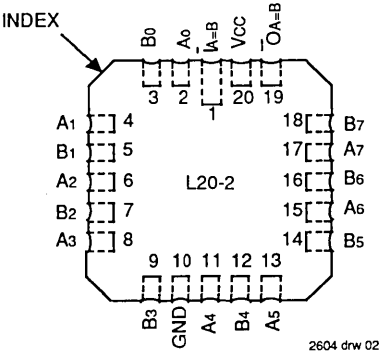
2604 drw 03

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

2604 drw 01



2604 drw 02

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor, Inc.

PIN DESCRIPTION

Pin Names	Description
A_0 - A_7	Word A Inputs
B_0 - B_7	Word B Inputs
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active LOW)

2604 tbl* 05

FUNCTION TABLE[1]

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

NOTE: 2604 tbl* 06

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   *A_0 = B_0, A_1 = B_1, A_2 = B_2, etc.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2604 tbl* 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
2. Input and VCC terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2604 tbl* 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions [1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

2604 tbl 03

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POWER SUPPLY CHARACTERISTICS $V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		f_i = 10MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	

NOTES:
2604 tbl* 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

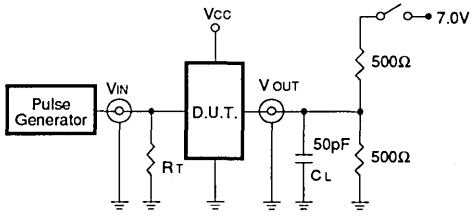
			IDT54/74FCT521				IDT54/74FCT521A				IDT54/74FCT521B				IDT54/74FCT521C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay An or Bn to $\overline{O}_A$ = B	C_L = 50pF R_L = 500Ω	1.5	11.0	1.5	15.0	1.5	7.2	1.5	9.5	1.5	5.5	1.5	7.3	1.5	4.5	1.5	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_A$ = B to $\overline{O}_A$ = B		1.5	10.0	1.5	9.0	1.5	6.0	1.5	7.8	1.5	4.6	1.5	6.0	1.5	4.1	1.5	4.5	ns

NOTES:
2604 tbl* 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



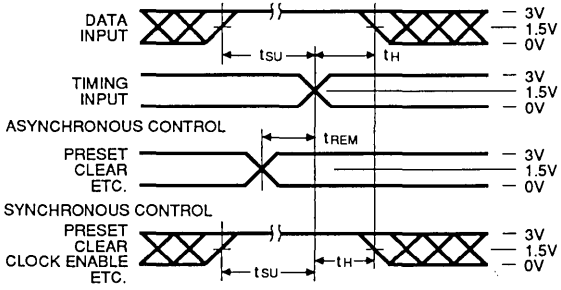
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

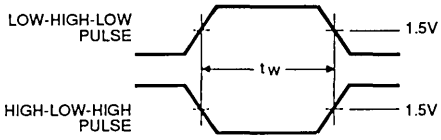
DEFINITIONS: 2604 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

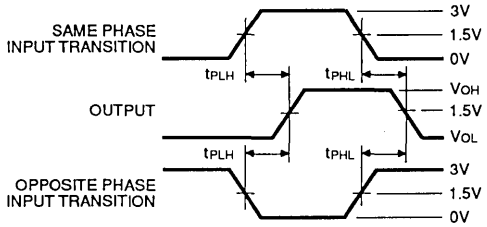
SET-UP, HOLD AND RELEASE TIMES



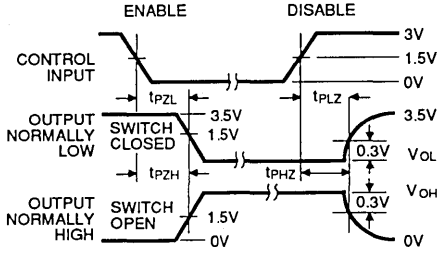
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

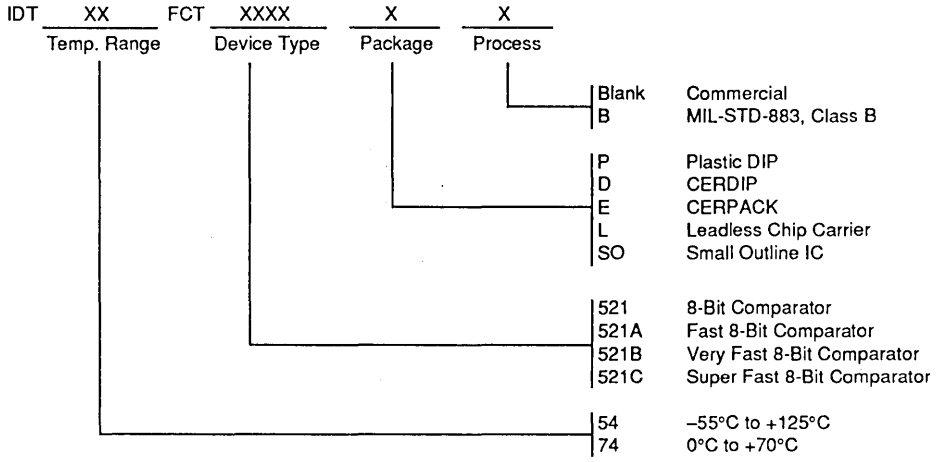


NOTES 2604 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2604 cnv* 09

Integrated Device Technology, Inc.

FAST CMOS OCTAL LATCHED TRANSCEIVER

IDT54/74FCT543
IDT54/74FCT543A

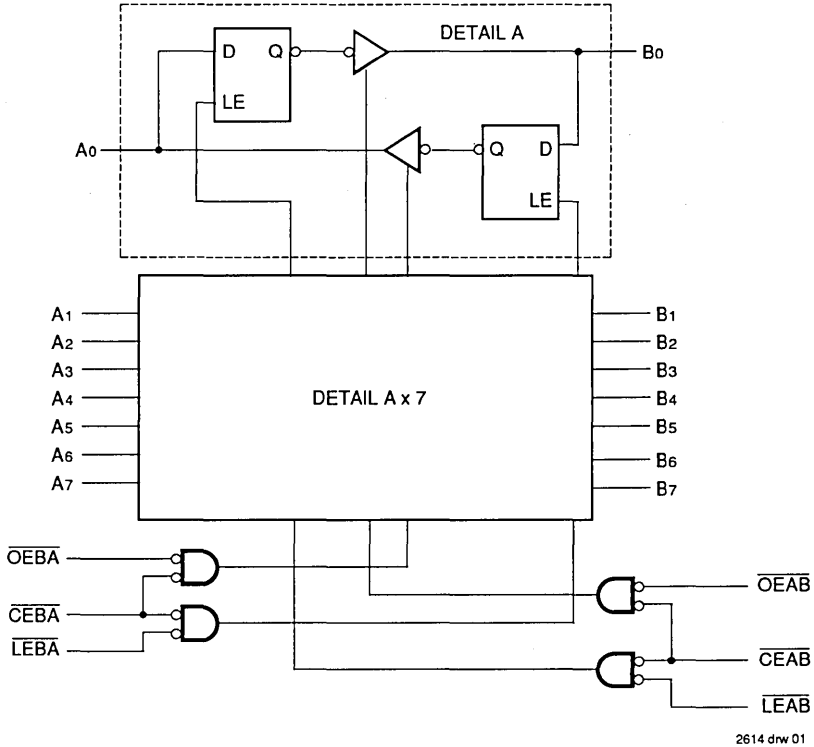
FEATURES:

- IDT54/74FCT543 equivalent to FAST™ speed
- **IDT54/74FCT543A 25% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial), 48mA (military)
- 8-bit octal latched transceiver
- Separate controls for data flow in each direction
- Back-to-back latches for storage
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than FAST™ (5μA max.)
- TTL input and output level compatible
- CMOS output level compatible
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT543/A is a non-inverting octal transceiver built using advanced CEMOS™, a dual metal CMOS technology. These devices contain two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0–A_7 or to take data from B_0–B_7, as indicated in the Function Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

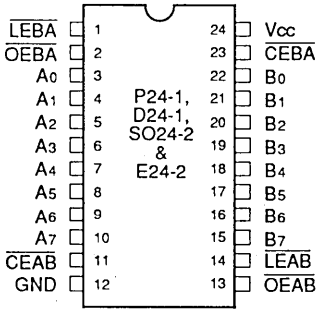
FUNCTIONAL BLOCK DIAGRAM



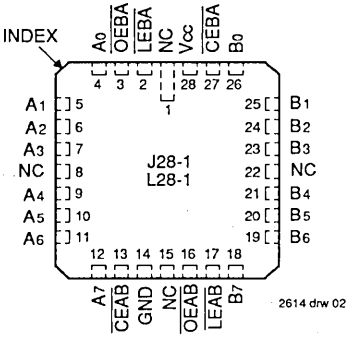
2614 drw 01

CEMOS is a trademark of Integrated Device Techology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A 3-State Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B 3-State Outputs

2614 tbl 02

FUNCTION TABLE (1,2)

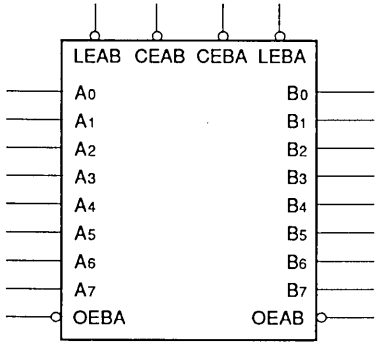
For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B_0–B_7
H	—	—	Storing	High Z
—	H	—	Storing	—
—	—	H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

2614 tbl 01

NOTES:
1. * Before $\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   — = Don't Care or Irrelevant
2. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

LOGIC SYMBOL



2614 drw 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	−0.5 to V_{CC}	−0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2614 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2614 tbl 04

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	-5(4)	µA
			V_I = GND	—	—	-5	
I_{IH}	Input HIGH Current (I/O pins Only)	V_{CC} = Max.	V_I = V_{CC}	—	—	15	µA
			V_I = 2.7V	—	—	15(4)	
I_{IL}	Input LOW Current (I/O pins Only)		V_I = 0.5V	—	—	-15(4)	µA
			V_I = GND	—	—	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}(4)	
			I_{OL} = 48mA MIL.(5)	—	0.3	0.55	
			I_{OL} = 64mA COM'L.(5)	—	0.3	0.55	

NOTES: 2614 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not excedd one second.
4. This parameter is guaranteed but not tested.
5. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

6

POWER SUPPLY CHARACTERISTICS V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	7.0	12.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

2614 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT543				IDT54/74FCT543A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparent Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	2.5	8.5	2.5	10.0	2.5	6.5	2.5	7.5	ns
tPLH tPHL	Propagation Delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn		2.5	12.5	2.5	14.0	2.5	8.0	2.5	9.0	ns
tPZH tPZL	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		2.0	12.0	2.0	14.0	2.0	9.0	2.0	10.0	ns
tPHZ tPLZ	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		2.0	9.0	2.0	13.0	2.0	7.5	2.0	8.5	ns
tSU	Set-up Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		3.0	—	3.0	—	2.0	—	2.0	—	ns
tH	Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	ns

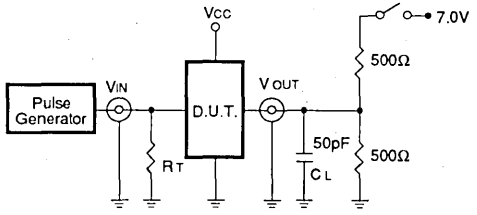
NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2514 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



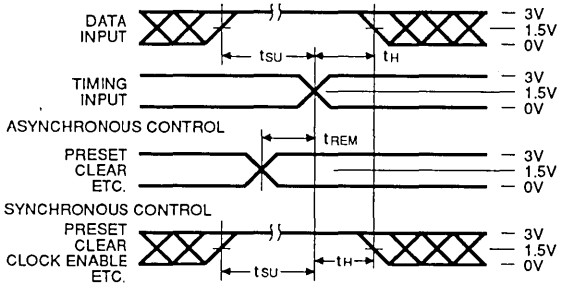
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

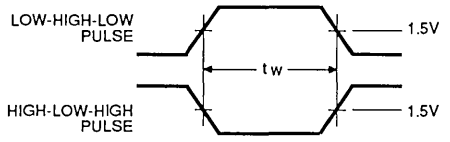
DEFINITIONS: 2614 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

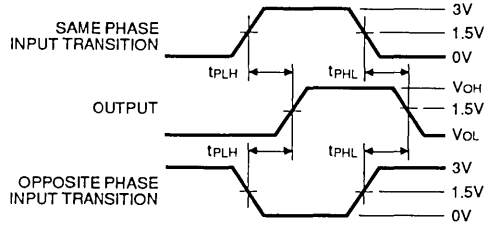
SET-UP, HOLD AND RELEASE TIMES



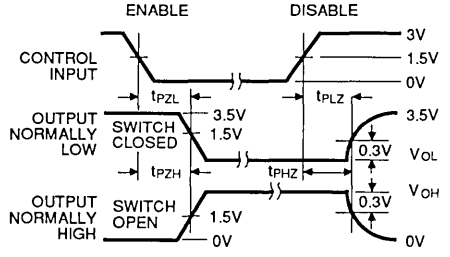
PULSE WIDTH



PROPAGATION DELAY



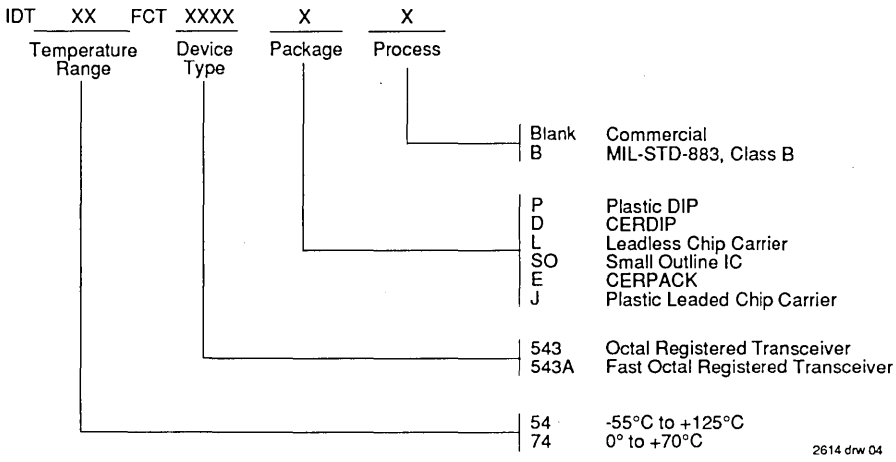
ENABLE AND DISABLE TIMES



NOTES 2614 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_O \leq 50\Omega$; $t_F \leq 2.5$ns; $t_R \leq 2.5$ns.

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSCEIVER/REGISTER

IDT54/74FCT646
IDT54/74FCT646A
IDT54/74FCT646C

FEATURES:

- IDT54/74FCT646 equivalent to FAST™ speed;
- **IDT54/74FCT646A 30% faster than FAST™**
- **IDT54/74FCT646C 40% faster than FAST™**
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typical static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin (300 mil) CERDIP, plastic DIP, SOIC, CERPACK, 28-pin LCC and PLCC
- Product available in Radiation Tolerant and Radiation Enhanced Versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

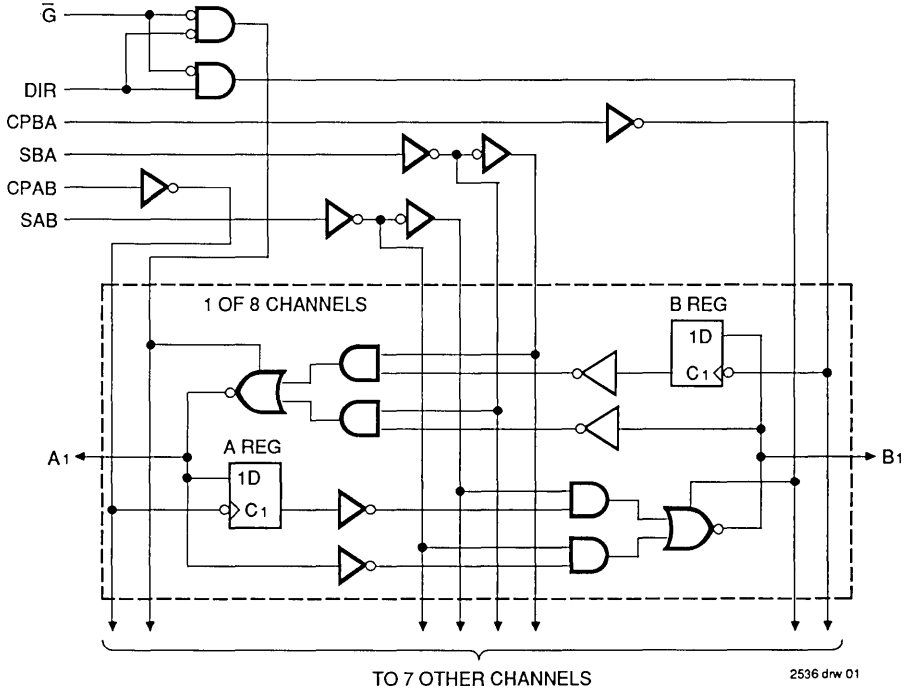
The IDT54/74FCT646/A/C consists of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

The IDT54/74FCT646/A/C utilizes the enable control ($\overline{G}$) and direction (DIR) pins to control the transceiver functions.

SAB and SBA control pins are provided to select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

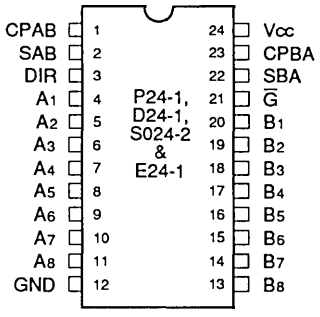
Data on the A or B data bus or both can be stored in the internal D flip flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA) regardless of the select or enable control pins.

FUNCTIONAL BLOCK DIAGRAM

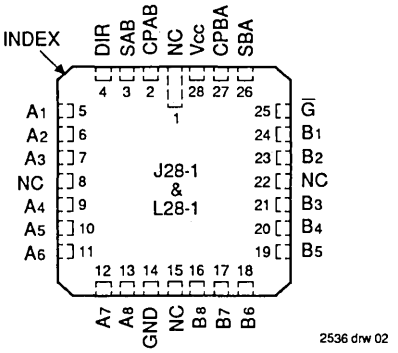


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



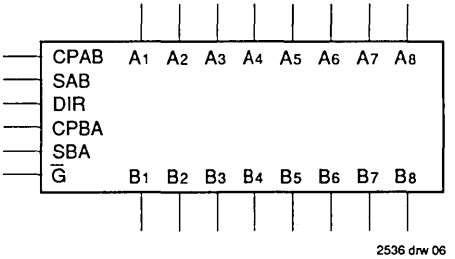
LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
A_1–A_8	Data Register A Inputs Data Register B Outputs
B_1–B_8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs

2536 tbl 01

LOGIC SYMBOL



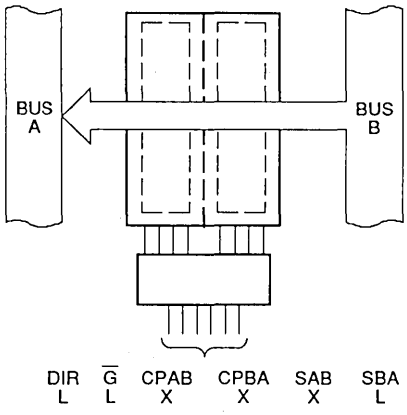
FUNCTION TABLE[2]

Inputs						Data I/O[1]		Operation or Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1–A_8	B_1–B_8	IDT54/74FCT646
H H	X X	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B Data
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus

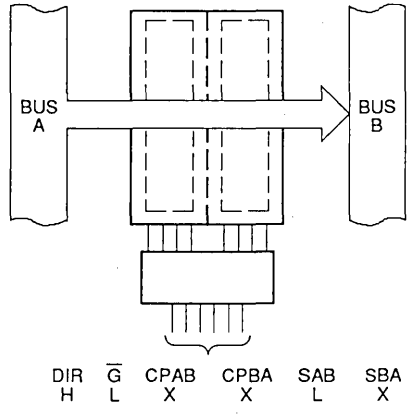
NOTES:
2536 tbl 02

1. The data output functions may be enabled or disabled by various signals at the $\overline{G}$ or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. H = HIGH, L = LOW, X = Don't Care, ↑ = LOW-to-HIGH Transition.

6

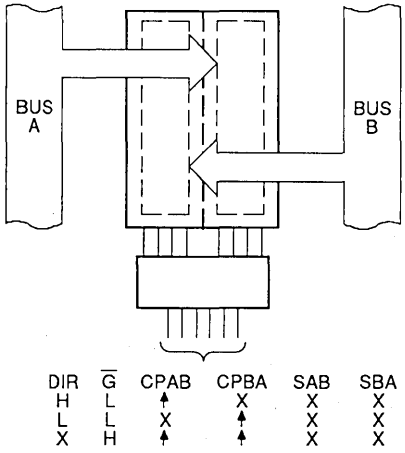


REAL–TIME TRANSFER BUS B TO BUS A

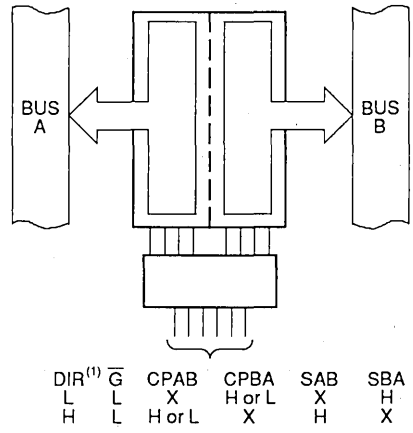


2536 drw 03

REAL–TIME TRANSFER BUS A TO BUS B



STORAGE FROM A AND/OR B



2536 drw 04

TRANSFER STORED DATA TO A AND/OR B

NOTE:
1. Cannot transfer data to A bus and B bus simultaneously.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2536 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2536 tbl 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = Vcc − 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = −55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	Vcc = Max.	V_I = Vcc	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	−5[4]	
			V_I = GND	—	—	−5	
I_{IH}	Input HIGH Current (I/O pins only)	Vcc = Max.	V_I = Vcc	—	—	15	µA
			V_I = 2.7V	—	—	15[4]	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	—	—	−15[4]	
			V_I = GND	—	—	−15	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.[3], V_O = GND		−60	−120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = −32µA		V_{HC}	Vcc	—	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300µA	V_{HC}	Vcc	—	
			I_{OH} = −12mA MIL.	2.4	4.0	—	
			I_{OH} = −15mA COM'L.	2.4	4.0	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	

NOTES: 2536 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{G}$ = DIR = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{G}$ = DIR = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{G}$ = DIR = GND Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	7.0	12.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

2536 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	54/74FCT646				54/74FCT646A				54/74FCT646C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	C_L = 50 pF R_L = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	5.4	1.5	6.0	ns
tPZH tPZL	Output Enable Time $\overline{G}$, DIR to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	1.5	7.8	1.5	8.9	ns
tPHZ tPLZ	Output Disable Time $\overline{G}$, DIR to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	6.3	1.5	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	1.5	5.7	1.5	6.3	ns
tPLH tPHL	Propagation Delay SBA or SAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	1.5	6.2	1.5	7.0	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

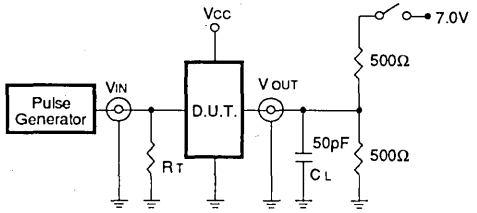
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2536 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



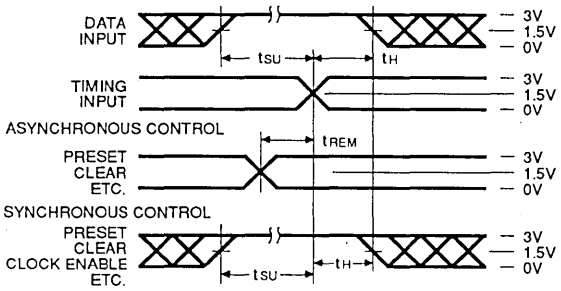
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

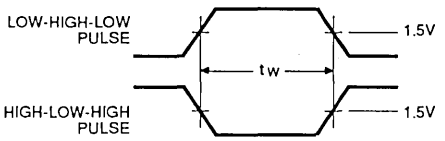
DEFINITIONS: 2536 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

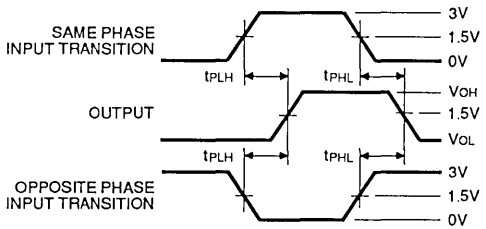
SET-UP, HOLD AND RELEASE TIMES



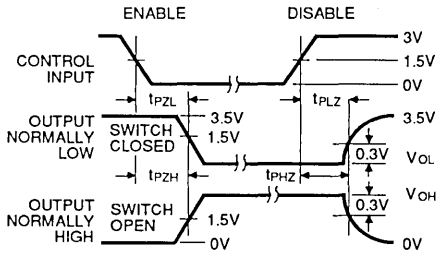
PULSE WIDTH



PROPAGATION DELAY



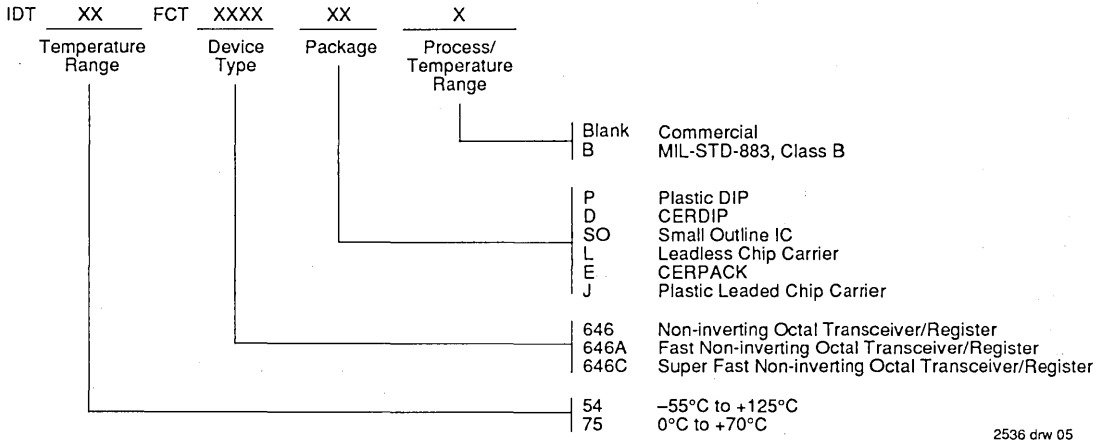
ENABLE AND DISABLE TIMES



NOTES 2536 drw 07

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT54/74FCT821A/B/C
IDT54/74FCT823A/B/C
IDT54/74FCT824A/B/C
IDT54/74FCT825A/B/C

FEATURES:

- Equivalent to AMD's Am29821-25 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT821A/823A/824A/825A equivalent to FAST™ speed
- **IDT54/74FCT821B/823B/824B/825B 25% faster than FAST™**
- **IDT54/74FCT821C/823C/824C/825C 40% faster than FAST™**
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output compatibility
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

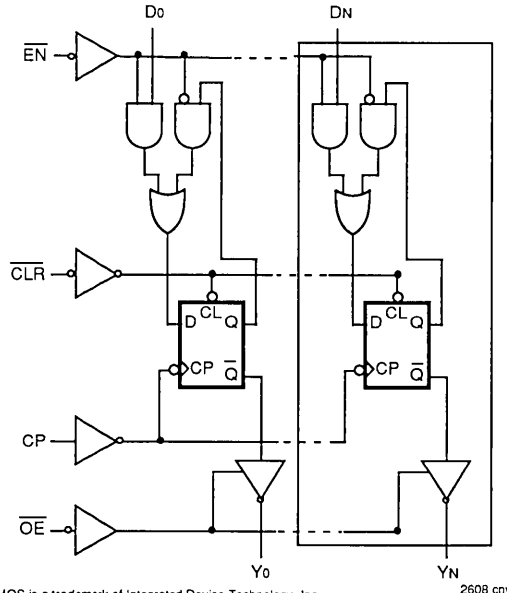
The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT821 are buffered, 10-bit wide versions of the popular '374 function. The IDT54/74FCT823 and IDT54/74FCT824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825 are 8-bit buffered registers with all the '823 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high impedance state.

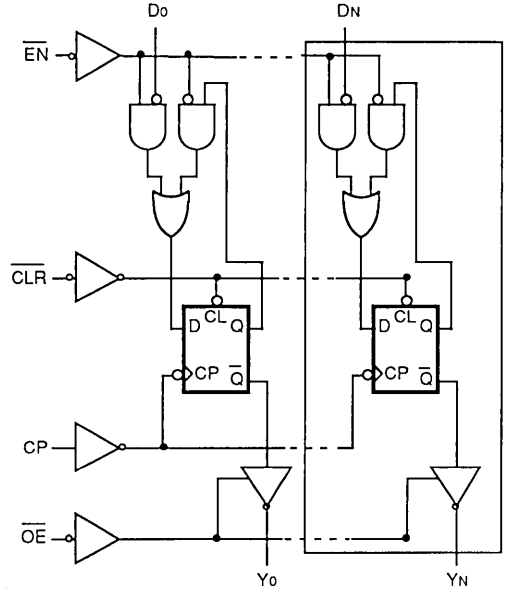
FUNCTIONAL BLOCK DIAGRAMS

IDT54/74FCT821/823/825



2608 cnv* 01

IDT54/74FCT824



2608 cnv* 02

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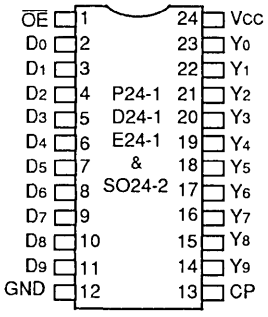
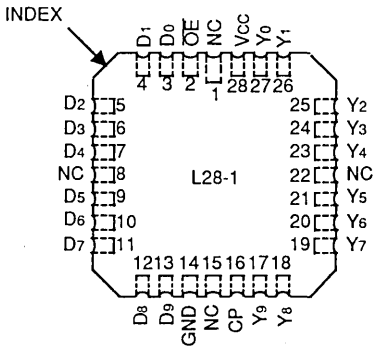
FAST is a trademark of Fairchild Semiconductor Co.

PIN CONFIGURATIONS

IDT54/74FCT821 10-BIT REGISTER

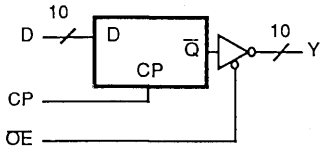


DIP/SOIC/CERPACK
TOP VIEW



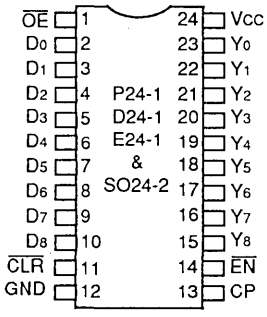
LCC
TOP VIEW

LOGIC SYMBOLS

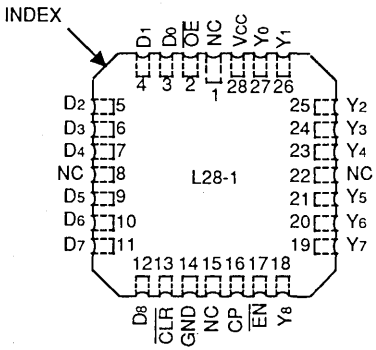


2608 cnv* 03

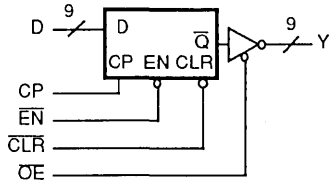
IDT54/74FCT823/824 9-BIT REGISTERS



DIP/SOIC/CERPACK
TOP VIEW

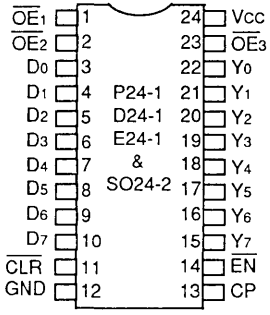


LCC
TOP VIEW

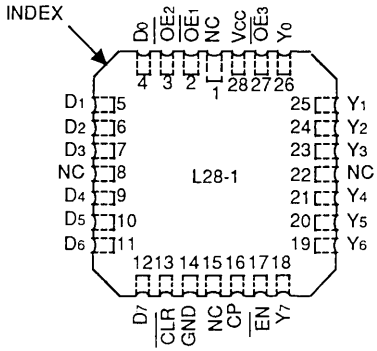


2608 cnv* 04

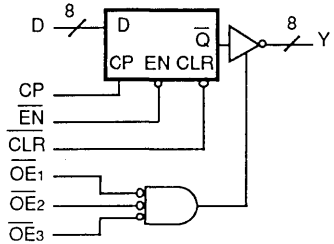
IDT54/74FCT825 8-BIT REGISTER



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW



2608 cnv* 05

PRODUCT SELECTOR GUIDE

	Device		
	10-Bit	9-Bit	8-Bit
Non-inverting	54/74FCT821A/B/C	54/74FCT823A/B/C	54/74FCT825A/B/C
Inverting		54/74FCT824A/B/C	

2608 tbl 01

PIN DESCRIPTION

Name	I/O	Description
D_I	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both inverting and non-inverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_I outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_I, $\overline{Y_I}$	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_I input is transferred to the Q_I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_I outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_I outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_I outputs.

2608 tbl 01

FUNCTION TABLE[1] IDT54/74FCT821/823/825

Inputs					Internal/ Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	Function
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE: 2608 tbl 02
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = HIGH-impedance

FUNCTION TABLE[1] IDT54/74FCT824

Inputs					Internal/ Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	Function
H	H	L	L	↑	H	Z	High Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

NOTE: 2608 tbl 03
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = HIGH-impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2608 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2608 tbl 05
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = Vcc − 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = −55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ. (2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = Vcc	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	−5(4)	
			V_I = GND	—	—	−5	
I_{OZH}	Off State (High Impedance) Output Current	Vcc = Max.	V_O = Vcc	—	—	10	µA
			V_O = 2.7V	—	—	10(4)	
I_{OZL}			V_O = 0.5V	—	—	−10(4)	
			V_O = GND	—	—	−10	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		−75	−120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = −32µA		V_{HC}	Vcc	—	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300µA	V_{HC}	Vcc	—	
			I_{OH} = −15mA MIL.	2.4	4.3	—	
			I_{OH} = −24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}(4)	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2608 tbl 06
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = $\overline{EN}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2608 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Test Conditions[1]	IDT54/74FCT821A/ 823A/824A/825A				IDT54/74FCT821B/ 823B/824B/825B				IDT54/74FCT821C/ 823C/824C/825C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Y I ($\overline{OE}$ = LOW)	C_L = 50pF R_L = 500Ω	—	10.0	—	11.5	—	7.5	—	8.5	—	6.0	—	7.0	ns
		C_L = 300pF[3] R_L = 500Ω	—	20.0	—	20.0	—	15.0	—	16.0	—	12.5	—	13.5	
tSU	Set-up Time HIGH or LOW D I to CP	C_L = 50pF R_L = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW D I to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW $\overline{EN}$ to CP		4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $\overline{EN}$ to CP		2.0	—	2.0	—	0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, $\overline{CLR}$ to YI		—	14.0	—	15.0	—	9.0	—	9.5	—	8.0	—	8.5	ns
tREM	Recovery Time $\overline{CLR}$ to CP		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	$\overline{CLR}$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI	C_L = 50pF R_L = 500Ω	—	12.0	—	13.0	—	8.0	—	9.0	—	7.0	—	8.0	ns
		C_L = 300pF[3] R_L = 500Ω	—	23.0	—	25.0	—	15.0	—	16.0	—	12.5	—	13.5	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI	C_L = 5pF[3] R_L = 500Ω	—	7.0	—	8.0	—	6.5	—	7.0	—	6.2	—	6.2	ns
		C_L = 50pF R_L = 500Ω	—	8.0	—	9.0	—	7.5	—	8.0	—	6.5	—	6.5	

NOTES:

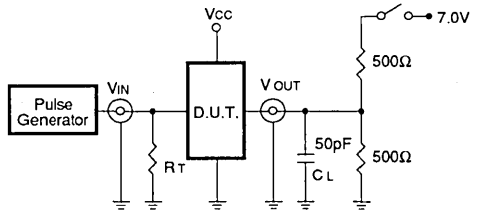
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2608 tbl" 08

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



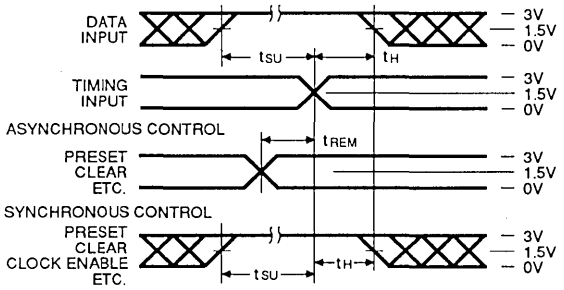
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

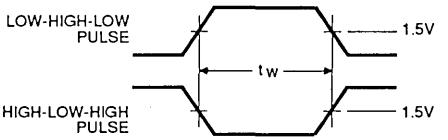
DEFINITIONS: 2608 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

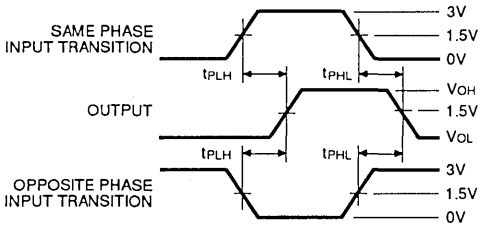
SET-UP, HOLD AND RELEASE TIMES



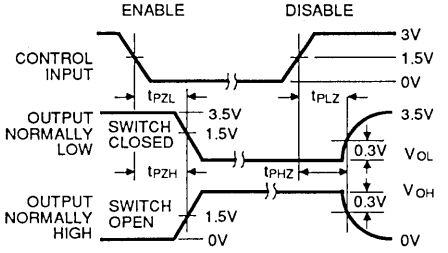
PULSE WIDTH



PROPAGATION DELAY



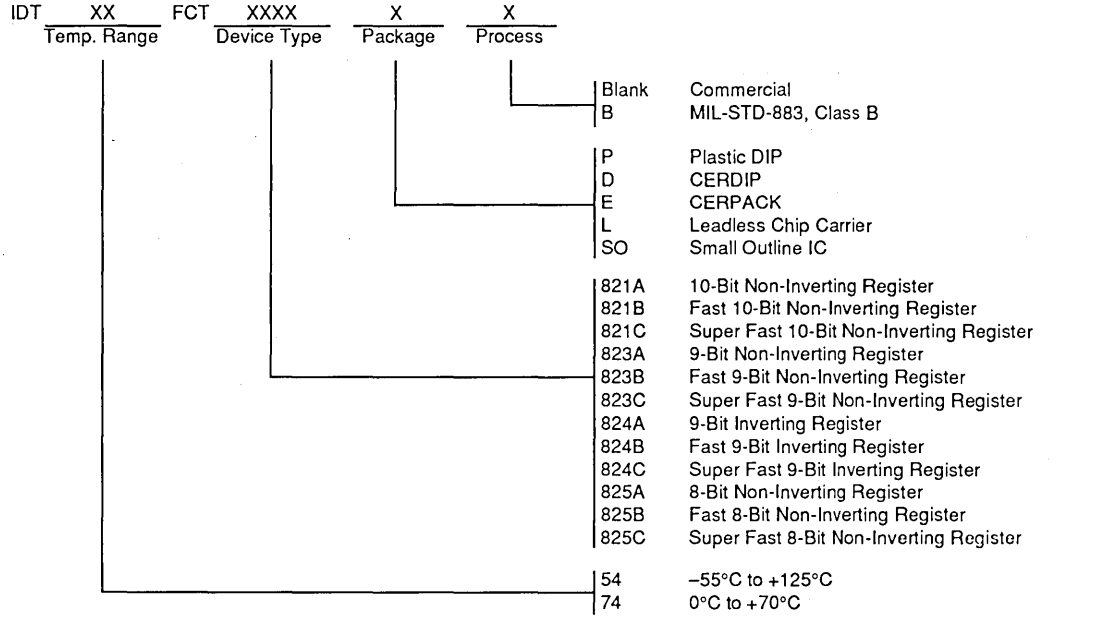
ENABLE AND DISABLE TIMES



NOTES 2608 drw 01

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2608 drw 11

6

Integrated Device Technology, Inc.

HIGH-PERFOMANCE CMOS BUFFERS

IDT54/74FCT827A
IDT54/74FCT827B
IDT54/74FCT827C

FEATURES:

- Faster than AMD's Am29827 series
- Equivalent to AMD's Am29827 bipolar buffers in pinout/ function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT827A equivalent to FAST™
- **IDT54/74FCT827B 35% faster than FAST™**
- **IDT54/74FCT827C 45% faster than FAST™**
- I_{OL} = 48mA (commercial), and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

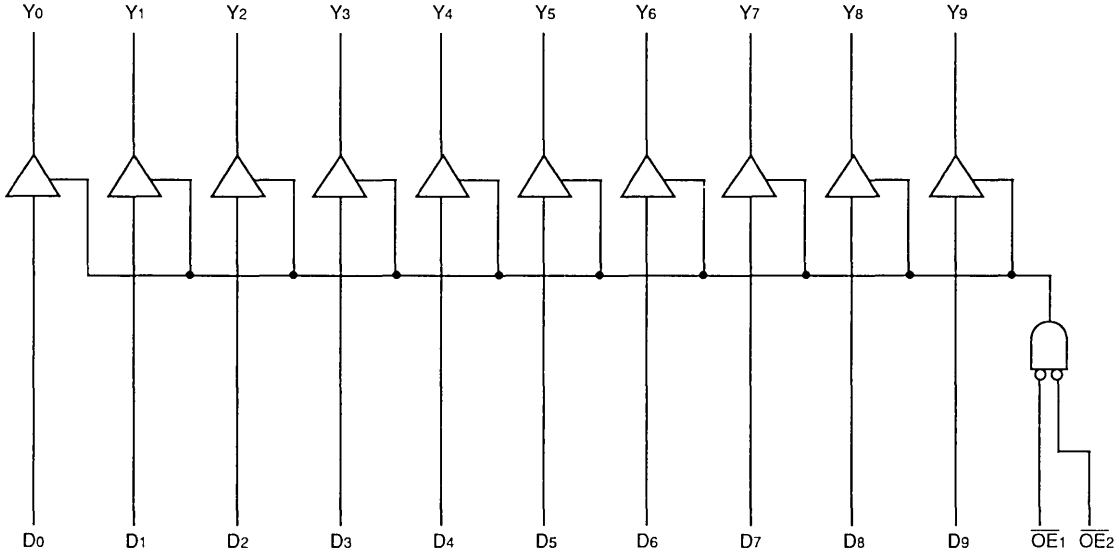
DESCRIPTION:

The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT827A/B/C 10-bit bus drivers provide high-performance bus interface buffering for wide data/ address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high impedance state.

FUNCTIONAL BLOCK DIAGRAM



2609 drw 01

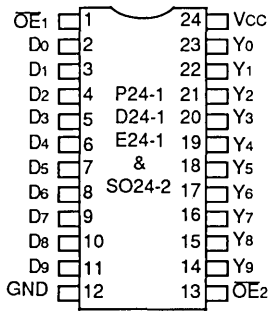
PRODUCT SELECTOR GUIDE

	10-Bit Buffer
Non-inverting	IDT54/74FCT827A/B/C

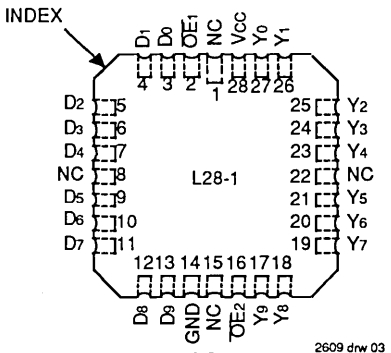
2609 tbl 01

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

PIN CONFIGURATIONS



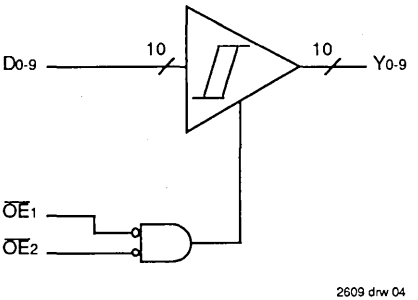
DIP/CERPACK/SOIC
TOP VIEW 2609 drw 02



2609 drw 03

LCC
TOP VIEW

LOGIC SYMBOL



2609 drw 04

PIN DESCRIPTION

Name	I/O	Description
$\overline{OE}_I$	I	When both are LOW, the outputs are enabled. When either one or both are HIGH, the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

2609 tbl 02

FUNCTION TABLE(1)

Inputs			Output	Function
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High-Impedance

2609 tbl 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to V_{CC}	V
TA	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

2609 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and VCC terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

2609 tbl 05

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC}–0.2V

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5[4]	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10[4]	
I_{OZL}			V_O = 0.5V	—	—	–10[4]	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–75	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA MIL.	2.4	4.3	—	
			I_{OH} = –24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2609 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_1}$ = $\overline{OE_2}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f i = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT) V_{IN} = 3.4V V_{IN} = GND	— —	1.7 2.0	4.0 5.0	mA
		V_{CC} = Max. Outputs Open f i = 2.5MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT) V_{IN} = 3.4V V_{IN} = GND	— —	3.2 5.2	6.5[5] 14.5[5]	

NOTES:

2609 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Conditions[1]	IDT54/74FCT827A				IDT54/74FCT827B				IDT54/74FCT827C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	—	8.0	—	9.0	—	5.0	—	6.5	—	4.4	—	5.0	ns
		CL = 300pF[3] RL = 500Ω	—	15.0	—	17.0	—	13.0	—	14.0	—	10.0	—	11.0	
tPZH tPZL	Output Enable Time $\overline{OE}$I to YI	CL = 50pF RL = 500Ω	—	12.0	—	13.0	—	8.0	—	9.0	—	7.0	—	8.0	ns
		CL = 300pF[3] RL = 500Ω	—	23.0	—	25.0	—	15.0	—	16.0	—	14.0	—	15.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$I to YI	CL = 5pF[3] RL = 500Ω	—	9.0	—	9.0	—	6.0	—	7.0	—	5.7	—	6.7	ns
		CL = 50pF RL = 500Ω	—	10.0	—	10.0	—	7.0	—	8.0	—	6.0	—	7.0	

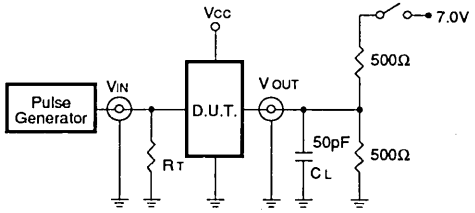
2609 tbl 08

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



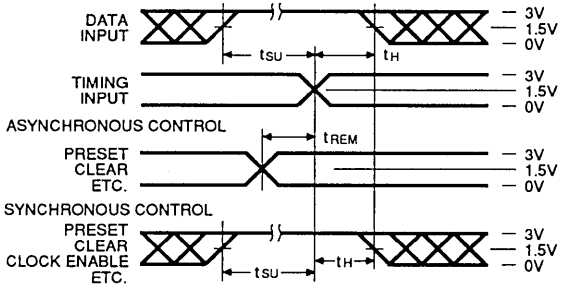
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

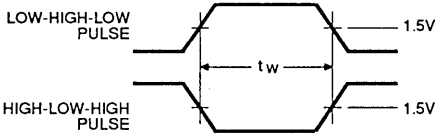
DEFINITIONS: 2609 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

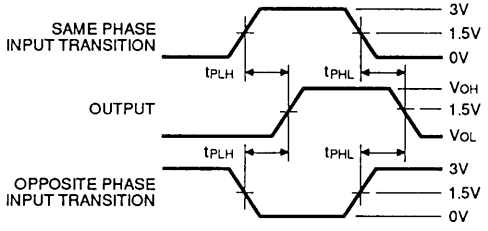
SET-UP, HOLD AND RELEASE TIMES



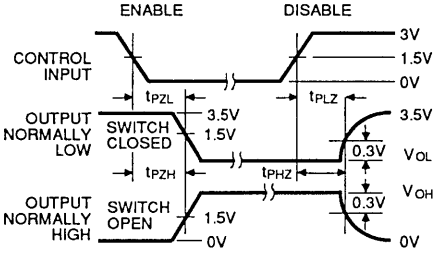
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

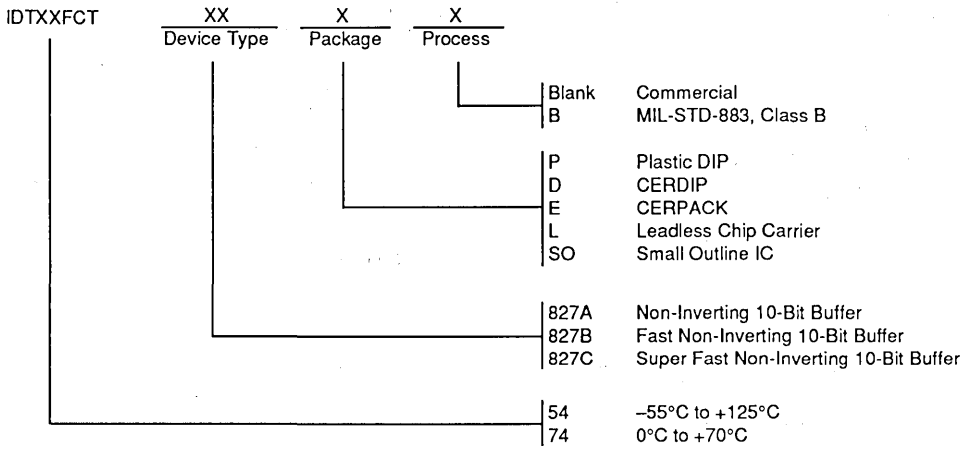


NOTES 2609 drw 11

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2609 cnv* 10

Integrated Device Technology, Inc.

FAST CMOS PARITY BUS TRANSCEIVER

IDT54/74FCT833A
IDT54/74FCT833B

FEATURES:

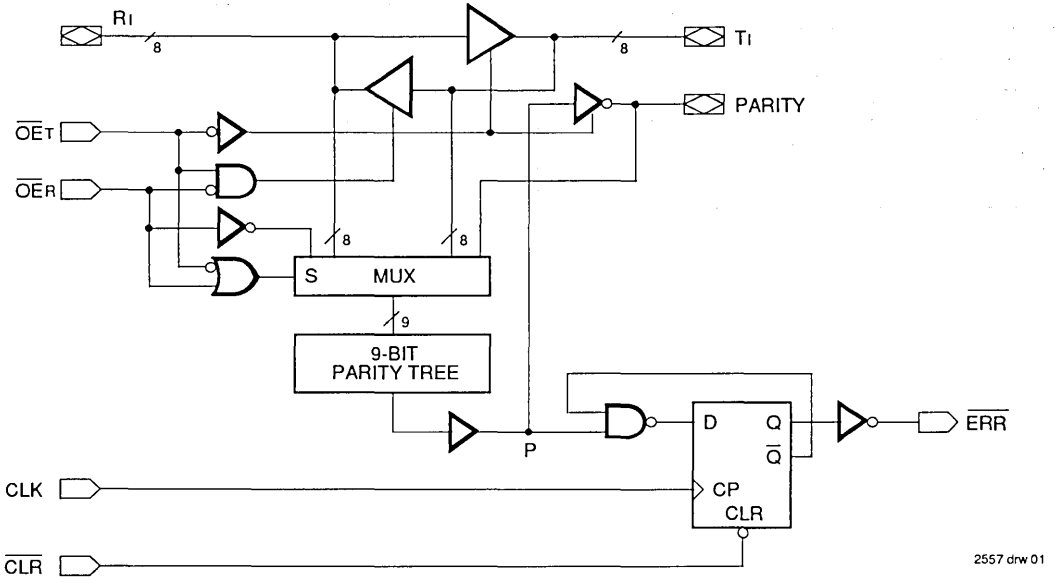
- Equivalent to AMD's Am29833 bipolar parity bus transceiver in pinout/function, speed and output drive over full temperature and voltage supply extremes
- High-speed bidirectional bus transceiver for processor-organized devices
- IDT54/74FCT833A equivalent to Am29833A speed and output drive
- **IDT54/74FCT833B 30% faster than Am29833A**
- Buffered direction and three-state controls
- Error flag with open-drain output
- I_{OL} = 48mA (commercial) and 32mA (military)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Available in plastic DIP, CERDIP, LCC, PLCC and SOIC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT833s are high-performance bus transceivers designed for two-way communications. They each contain an 8-bit data path from the R (port) to the T (port), an 8-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. The error flag can be clocked and stored in a register and read at the $\overline{ERR}$ output. The clear ($\overline{CLR}$) input is used to clear the error flag register.

The output enables $\overline{OE_T}$ and $\overline{OE_R}$ are used to force the port outputs to the high-impedance state so that the device can drive bus lines directly. In addition, $\overline{OE_R}$ and $\overline{OE_T}$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability. The devices are specified at 48mA and 32mA output sink current over the commercial and military temperature ranges, respectively.

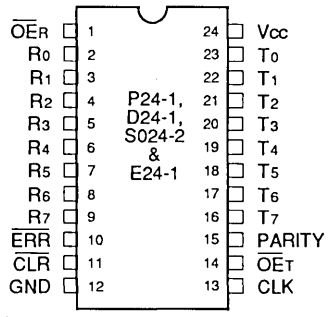
FUNCTIONAL BLOCK DIAGRAM



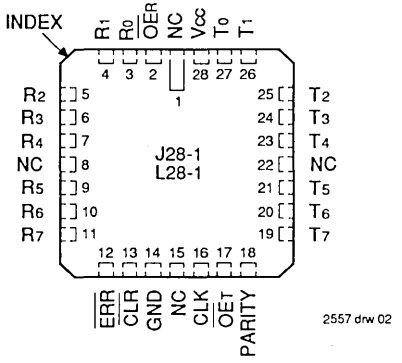
6

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTION

Pin Name	I/O	Description
$\overline{OE}_R$	I	RECEIVE enable input.
RI	I/O	8-bit RECEIVE data input/output.
$\overline{ERR}$	O	Output from fault registers. Register detection of odd parity fault on rising clock edge (CLK). A registered $\overline{ERR}$ output remains low until cleared. Open drain output, requires pull up resistor.
$\overline{CLR}$	I	Clears the fault register output.
TI	I/O	8-bit TRANSMIT data input/output.
PARITY	I/O	1-bit PARITY output.
$\overline{OE}_T$	I	TRANSMIT enable input.
CLK	I	External clock pulse input for fault register flag.

2557 tbl 01

ERROR FLAG OUTPUT FUNCTION TABLE(1,2)

Inputs		Internal To Device	Output Pre-State	Output	
$\overline{CLR}$	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	Sample
H	↑	—	L	L	(1's
H	↑	L	—	L	Capture)
L	—	—	—	H	Clear

2557 tbl 02

NOTE:
1. $\overline{OE}_T$ is HIGH and $\overline{OE}_R$ is LOW.
2. H = HIGH
   L = LOW
   ↑ = LOW to HIGH transition of clock
   – = Dont Care or Irrelevant

FUNCTION TABLE[2]

Inputs						Outputs				
$\overline{OE_T}$	$\overline{OE_R}$	$\overline{CLR}$	CLK	R_I (Σ or H's)	T_I Incl Parity (Σ of H's)	R_I	T_I	Parity	$\overline{ERR}$[1]	Function
L	H	H	↑	H (Odd)	NA	NA	H	L	H	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	H	↑	H (Even)	NA	NA	H	H	L	
L	H	H	↑	L (Odd)	NA	NA	L	L	H	
L	H	H	↑	L (Even)	NA	NA	L	H	L	
H	L	H	↑	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag: transmitting path is disabled.
H	L	H	↑	NA	H (Even)	H	NA	NA	L	
H	L	H	↑	NA	L (Odd)	L	NA	NA	H	
H	L	H	↑	NA	L (Even)	L	NA	NA	L	
—	—	L	—	—	—	NA	NA	NA	H	Clear the state of error flag register.
H	H	H	H or L	—	—	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	—	—	—	Z	Z	Z	H	
H	H	H	↑	H or L (Odd)	—	Z	Z	Z	H	
H	H	H	↑	H or L (Even)	—	Z	Z	Z	L	
L	L	H	↑	H (Odd)	NA	NA	H	H	L	Forced-error checking.
L	L	H	↑	H (Even)	NA	NA	H	L	H	
L	L	H	↑	L (Odd)	NA	NA	L	H	L	
L	L	H	↑	L (Even)	NA	NA	L	L	H	

2557 tbl 03

NOTES:

1. Output state assumes HIGH output pre-state.
2. H = HIGH
   L = LOW
   ↑ = LOW to HIGH transition of clock
   *No change to stored Error State
   Z = HIGH Impedance
   NA = Not Applicable
   – = Don't Care or Irrelevant
   Odd = Odd number of logic one's
   Even = Even number of logic one's
   I = 0, 1, 2, 3, 4, 5, 6, 7

6

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to V_{CC}	−0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2557 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2557 tbl 05

1. This parameter is guaranteed by characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} − 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current (Except I/O Pins)		V_I = 0.5V	—	—	-5[4]	
			V_I = GND	—	—	-5	
I_{IH}	Input HIGH Current (I/O Pins Only)	V_{CC} = Max.	V_I = V_{CC}	—	—	15	µA
			V_I = 2.7V	—	—	15[4]	
I_{IL}	Input LOW Current (I/O Pins Only)		V_I = 0.5V	—	—	-15[4]	
			V_I = GND	—	—	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	—	mA
V_{OH}	Output HIGH Voltage (Except $\overline{ERR}$)	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = −32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300µA	V_{HC}	V_{CC}	—	
			I_{OH} = −15mA MIL.	2.4	4.3	—	
			I_{OH} = −24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	Except $\overline{ERR}$ I_{OL} = 300µA	—	GND	V_{LC}[4]	
			Except $\overline{ERR}$ I_{OL} = 32 mA MIL.	—	0.3	0.5	
			Except $\overline{ERR}$ I_{OL} = 48mA COM'L.	—	0.3	0.5	
			$\overline{ERR}$ I_{OL} = 48mA	—	0.3	0.5	

NOTES: 2557 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS $V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.; $V_{IN} \geq V_{HC}$, $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_T = \overline{OE}_R$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_T$ = GND $\overline{OE}_R$ = V_{CC} f_i = 2.5MHz One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.4	3.4	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.9	5.4	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_T$ = GND f_i = 2.5MHz $\overline{OE}_R$ = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2557 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

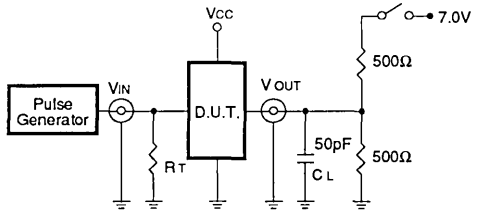
Symbol	Parameter	Conditions[1]	IDT54/74FCT833A				IDT54/74FCT833B				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH	Propagation Delay	C_L = 50pF	—	10.0	—	14.0	—	7.0	—	10.0	ns
tPHL	R_I to T_I, T_I to R_I	C_L = 300pF[3]	—	17.5	—	21.5	—	14.5	—	17.5	
tPLH	Propagation Delay	C_L = 50pF	—	15.0	—	20.0	—	10.5	—	14.0	ns
tPHL	R_I to PARITY	C_L = 300pF[3]	—	22.5	—	27.5	—	18.0	—	21.5	
tPZH	Output Enable Time	C_L = 50pF	—	12.0	—	16.0	—	8.5	—	11.0	ns
tPZL	$\overline{OE}_R$, $\overline{OE}_T$ to R_I, T_I	C_L = 300pF[3]	—	19.5	—	23.5	—	16.0	—	18.5	
tPHZ	Output Disable Time	C_L = 5pF[3]	—	10.7	—	14.7	—	7.2	—	9.8	ns
tPLZ	$\overline{OE}_R$, $\overline{OE}_T$ to R_I, T_I	C_L = 50pF	—	12.0	—	16.0	—	8.5	—	11.0	
tSU	T_I, PARITY to CLK Set-up Time	C_L = 50pF	12.0	—	16.0	—	8.5	—	11.0	—	ns
tH	T_I, PARITY to CLK Hold Time		0	—	0	—	0	—	0	—	ns
tREM	Clear Recovery Time $\overline{CLR}$ to CLK		15.0	—	20.0	—	10.5	—	14.0	—	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	9.5	—	5.5	—	7.0	—	ns
tW	Clear Pulse Width LOW		7.0	—	9.5	—	5.5	—	7.0	—	ns
tPHL	Propagation Delay CLK to $\overline{ERR}$		—	12.0	—	16.0	—	8.5	—	11.0	ns
tPLH	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$		—	16.0	—	20.0	—	15.0	—	18.0	ns
tPLH	Propagation Delay	C_L = 50pF	—	15.0	—	20.0	—	10.5	—	14.0	ns
tPHL	$\overline{OE}_R$ to PARITY	C_L = 300pF[3]	—	22.5	—	27.5	—	18.0	—	21.5	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

2557 tbl 08

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



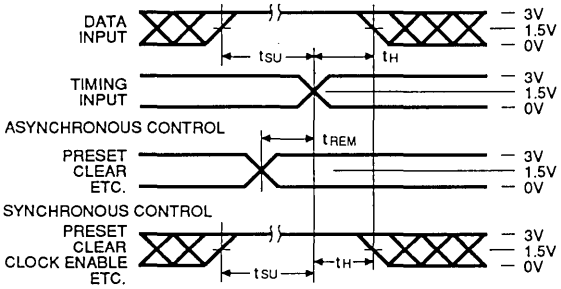
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

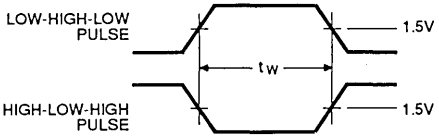
DEFINITIONS: 2557 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

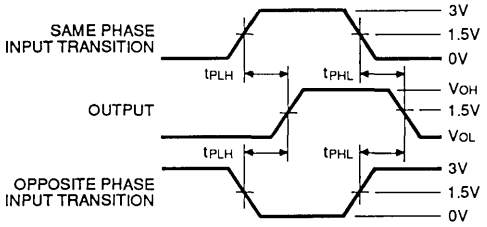
SET-UP, HOLD AND RELEASE TIMES



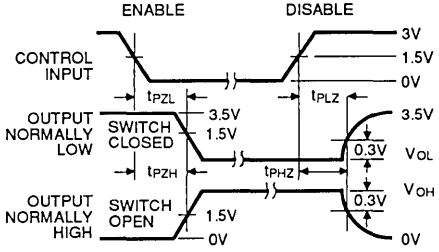
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

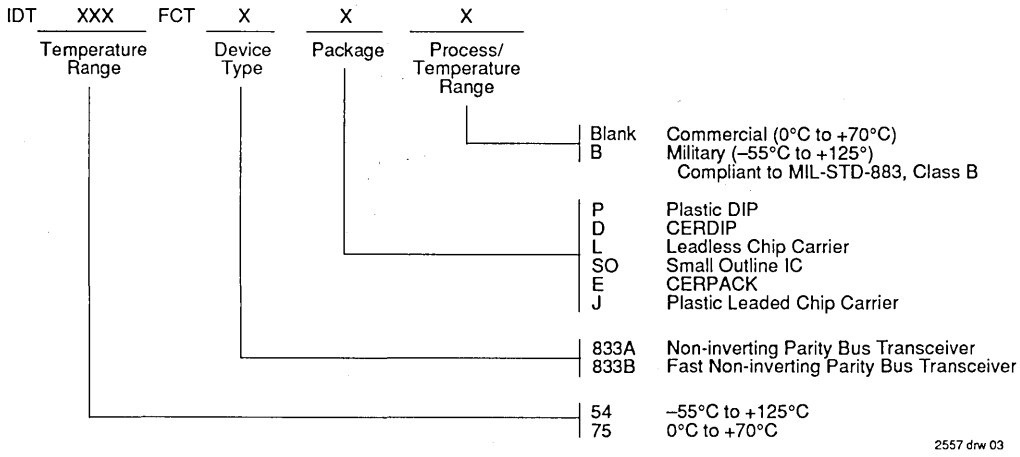


NOTES 2557 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT54/74FCT841A/B/C
IDT54/74FCT843A/B/C
IDT54/74FCT844A/B/C
IDT54/74FCT845A/B/C

FEATURES:

- Equivalent to AMD's Am29841-46 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT841A/843A/844A/845A equivalent to FAST™ speed
- **IDT54/74FCT841B/843B/844B/845B 25% faster than FAST™**
- **IDT54/74FCT841C/843C/844C/845C 40% faster than FAST™**
- Buffered common latch enable, clear and preset inputs
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

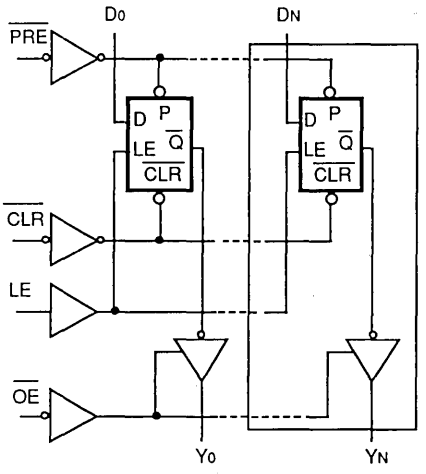
The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT840 series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841 is a buffered, 10-bit wide version of the popular '373 function. The IDT54/74FCT843 and IDT54/74FCT844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$)—ideal for parity bus interfacing in high-performance systems. The IDT54/74FCT845 is an 8-bit buffered latch with all the '843/4 controls, plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. It is ideal for use as an output port requiring high IOL/IOH.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

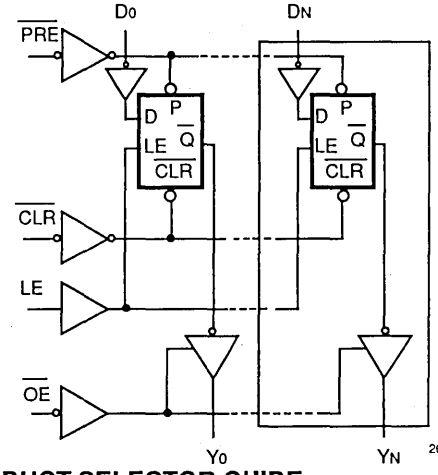
FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT841/843/845



2607 cnv* 01

IDT54/74FCT844



2607 cnv* 02

PRODUCT SELECTOR GUIDE

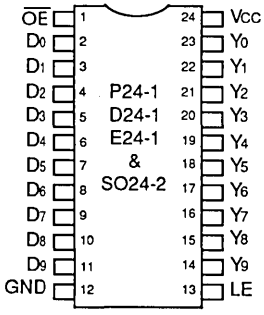
	Device		
	10-Bit	**9-Bit**	**8-Bit**
Non-inverting	IDT54/74FCT841 A/B/C	IDT54/74FCT843 A/B/C	IDT54/74FCT845 A/B/C
Inverting		IDT54/74FCT844 A/B/C	

2607 tbl 01

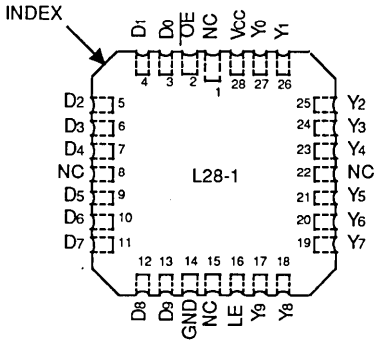
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS

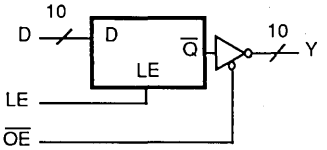
IDT54/74FCT841 10-BIT LATCH



DIP/CERPACK/SOIC
TOP VIEW

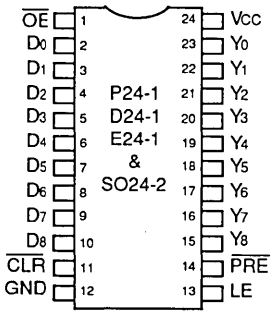


LCC
TOP VIEW

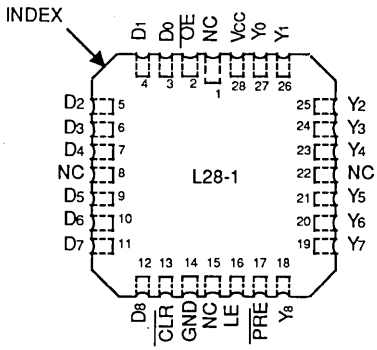


2607 cnv* 03,04,05

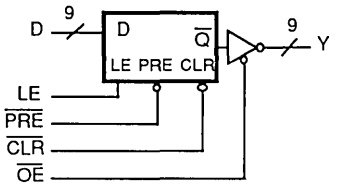
IDT54/74FCT843/844 9-BIT LATCHES



DIP/CERPACK/SOIC
TOP VIEW

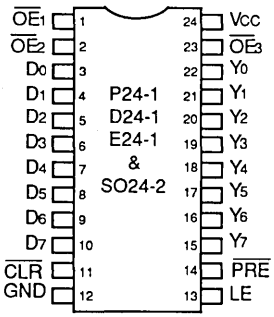


LCC
TOP VIEW

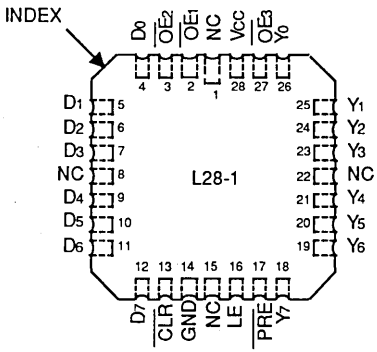


2607 cnv* 06,07,08

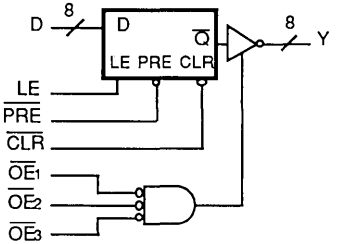
IDT54/74FCT845 8-BIT LATCH



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



2607 cnv* 09,10,11

PIN DESCRIPTION

Name	I/O	Description
IDT54/74FCT841/843/845 (Non-inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
DI	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
YI	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs (YI) are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$
IDT54/74FCT844 (Inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
DI	I	The latch inverting data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
YI	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs (YI) are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$

2607 tbl 02

FUNCTION TABLE[1]
IDT54/74FCT841/843/845

Inputs					Inter - nal	Out - puts	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	DI	QI	YI	Function
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE: 2607 tbl 03
1. H = HIGH, L = LOW, X = Don't Care, NC = No Charge, Z = High-Impedance

FUNCTION TABLE[1]
IDT54/74FCT844

Inputs					Inter - nal	Out - puts	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	DI	QI	YI	Function
H	H	H	X	X	X	Z	High Z
H	H	H	H	H	L	Z	High Z
H	H	H	H	L	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE: 2607 tbl 04
1. H = HIGH, L = LOW, X = Don't Care, NC = No Charge, Z = High-Impedance

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2607 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2607 tbl 06

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = Vcc − 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = −55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ. (2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = Vcc	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	−5(4)	
			V_I = GND	—	—	−5	
I_{OZH}	Off State (High Impedance) Output Current	Vcc = Max.	V_O = Vcc	—	—	10	µA
			V_O = 2.7V	—	—	10(4)	
I_{OZL}			V_O = 0.5V	—	—	−10(4)	
			V_O = GND	—	—	−10	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		−75	−120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = −32µA		V_{HC}	Vcc	—	V
		Vcc = Min.	I_{OH} = −300µA	V_{HC}	Vcc	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15mA MIL.	2.4	4.3	—	
			I_{OH} = −24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min.	I_{OL} = 300µA	—	GND	V_{LC}(4)	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2607 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2607 tbl 08

NOTES:

1. For conditions shown as Max. or Mn., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

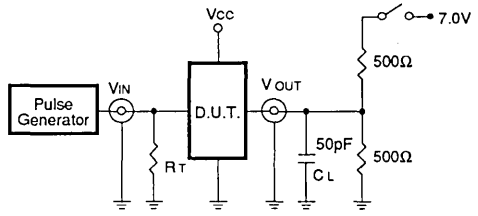
Parameter	Description		Test Conditions [1]	IDT54/74FCT841A/ 843A/844A/845A				IDT54/74FCT841B/ 843B/844B/845B				IDT54/74FCT841C/ 843C/844C/845C				Unit
				Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
(FCT841, 843, 845) tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)		CL = 50pF RL = 500Ω	—	9.0	—	10.0	—	6.5	—	7.5	—	5.5	—	6.3	ns
			CL = 300pF[3] RL = 500Ω	—	13.0	—	15.0	—	13.0	—	15.0	—	13.0	—	15.0	
(FCT844) tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)		CL = 50pF RL = 500Ω	—	10.0	—	12.0	—	8.0	—	9.0	—	7.0	—	8.0	ns
			CL = 300pF[3] RL = 500Ω	—	13.0	—	15.0	—	13.0	—	15.0	—	13.0	—	15.0	
tSU	Data to LE Set-up Time		CL = 50pF RL = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Data to LE Hold Time			2.5	—	3.0	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tPLH tPHL	Propagation Delay LE to YI		CL = 50pF RL = 500Ω	—	12.0	—	13.0	—	8.0	—	10.5	—	6.4	—	6.8	ns
			CL = 300pF[3] RL = 500Ω	—	16.0	—	20.0	—	15.5	—	18.0	—	15.0	—	16.0	
tPLH	Propagation Delay, $\overline{PRE}$ to YI		CL = 50pF RL = 500Ω	—	12.0	—	14.0	—	8.0	—	10.0	—	7.0	—	9.0	ns
tREM	Recovery Time $\overline{PRE}$ to YI			—	14.0	—	17.0	—	10.0	—	13.0	—	9.0	—	12.0	ns
tPHL	Propagation Delay, $\overline{CLR}$ to YI			—	13.0	—	14.0	—	10.0	—	11.0	—	9.0	—	10.0	ns
tREM	Recovery Time $\overline{CLR}$ to YI			—	14.0	—	17.0	—	10.0	—	10.0	—	9.0	—	9.0	ns
tW	LE Pulse Width[3]	HIGH	CL = 50pF RL = 500Ω	4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tW	$\overline{PRE}$ Pulse Width[3]	LOW		5.0	—	7.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tW	$\overline{CLR}$ Pulse Width[3]	LOW		4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI		CL = 50pF RL = 500Ω	—	11.5	—	13.0	—	8.0	—	8.5	—	6.5	—	7.3	ns
			CL = 300pF[3] RL = 500Ω	—	23.0	—	25.0	—	14.0	—	15.0	—	12.0	—	13.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI		CL = 5pF[3] RL = 500Ω	—	7.0	—	9.0	—	6.0	—	6.5	—	5.7	—	6.0	ns
			CL = 50pF RL = 500Ω	—	8.0	—	10.0	—	7.0	—	7.5	—	6.0	—	6.3	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

2607 tbl 09

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



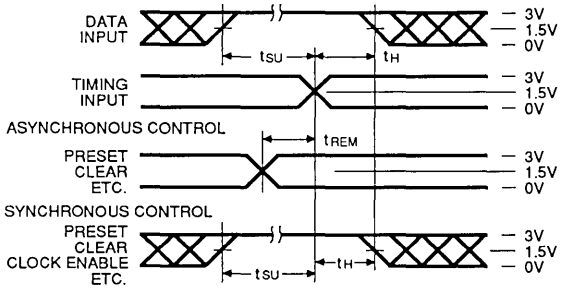
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

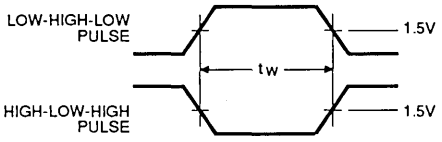
DEFINITIONS: 2607 tbl 07

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

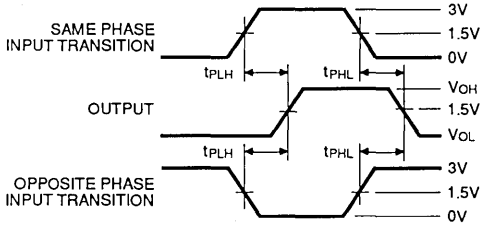
SET-UP, HOLD AND RELEASE TIMES



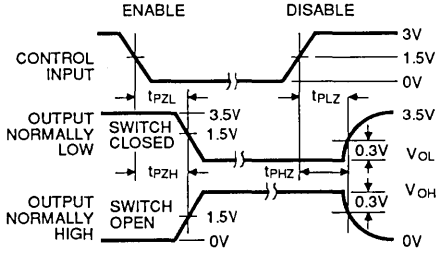
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

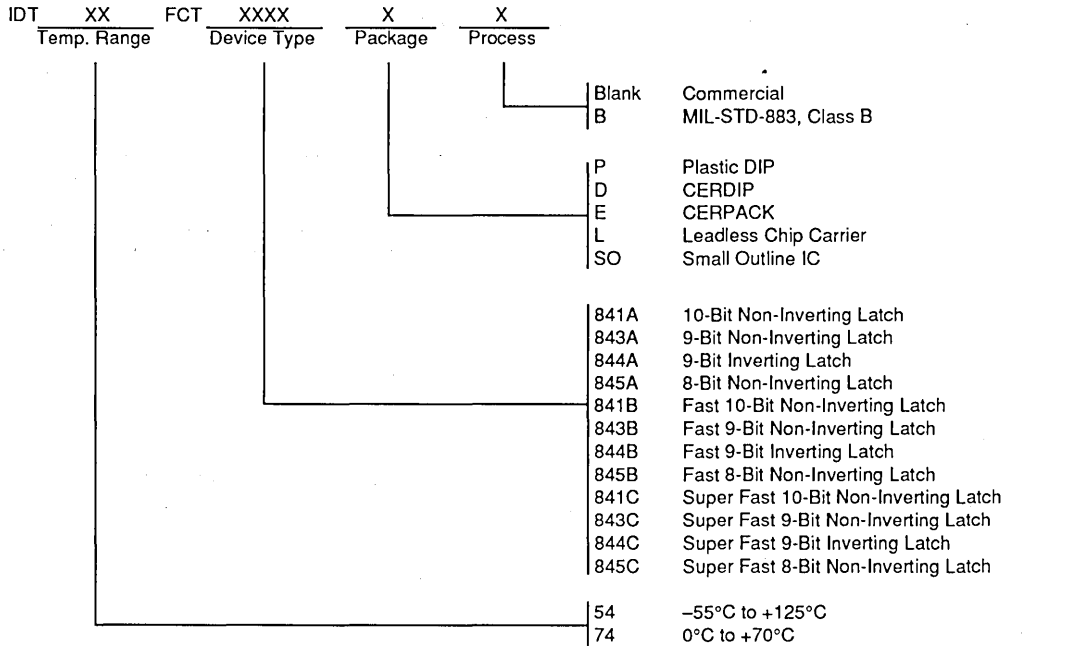


NOTES 2607 drw 12

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2607 cnv* 17

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS TRANSCEIVERS

IDT54/74FCT861A/B/C
IDT54/74FCT863A/B/C
IDT54/74FCT864A/B/C

FEATURES:

- Equivalent to AMD's Am29861-64 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT861A/863A/864A equivalent to FAST™ speed
- **IDT54/74FCT861B/863B/864B 25% faster than FAST™**
- High-speed symmetrical bidirectional transceivers
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series (5μA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

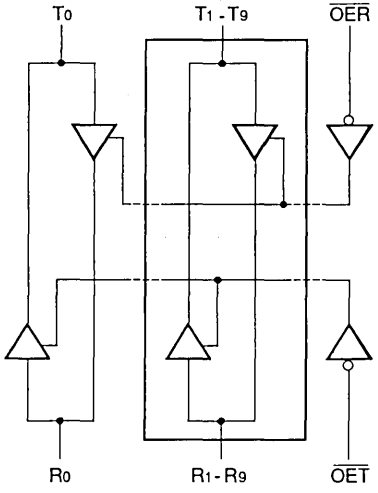
The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT860 series bus transceivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The IDT54/74FCT863/864 9-bit transceivers have NAND-ed output enables for maximum control flexibility.

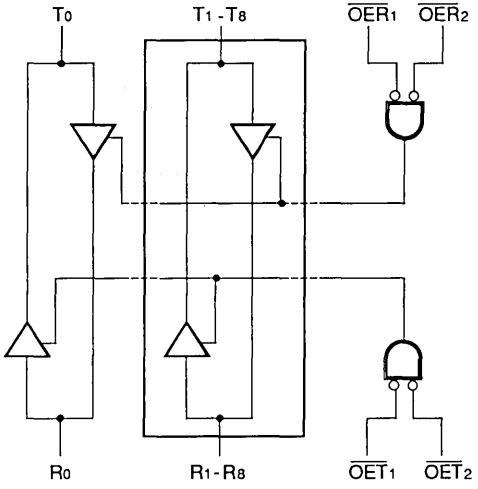
All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high-impedance state.

FUNCTIONAL BLOCK DIAGRAMS

IDT54/74FCT861



IDT54/74FCT863/864



2610 drw 01

PRODUCT SELECTOR GUIDE

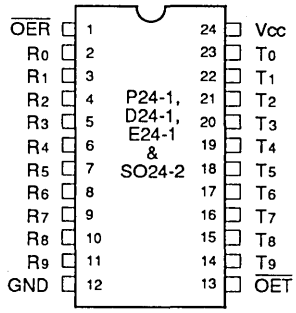
	Device	
	10-Bit	9-Bit
Non-inverting	IDT54/74FCT861	IDT54/74FCT863
Inverting		IDT54/74FCT864

2610 tbl 01

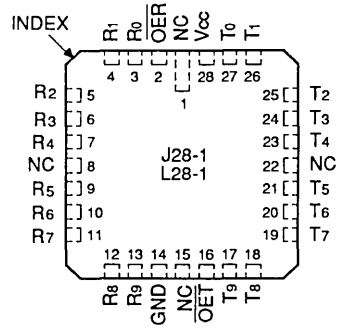
CEMOS is a trademark of Integrated Device Techology, Inc.
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS

IDT54/74FCT861 10-BIT TRANSCEIVER

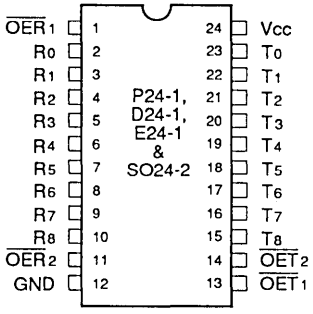


DIP/CERPACK/SOIC
TOP VIEW

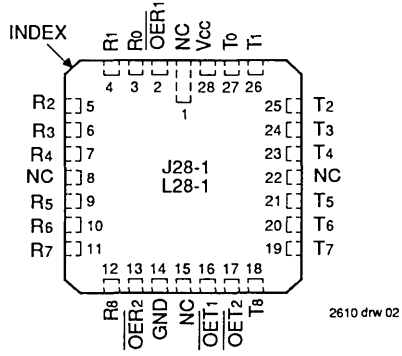


LCC/PLCC
TOP VIEW

IDT54/74FCT863/864 9-BIT TRANSCEIVERS



DIP/CERPACK/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
IDT54/74FCT861		
$\overline{OER}$	I	When LOW in conjunction with $\overline{OET}$ HIGH activates the RECEIVE mode.
$\overline{OET}$	I	When LOW in conjunction with $\overline{OER}$ HIGH activates the TRANSMIT mode.
RI	I/O	10-bit RECEIVE input/output.
TI	I/O	10-bit TRANSMIT input/output.
IDT54/74FCT863/864		
$\overline{OER}$I	I	When LOW in conjunction with $\overline{OET}$I HIGH activates the RECEIVE mode.
$\overline{OET}$I	I	When LOW in conjunction with $\overline{OER}$I HIGH activates the TRANSMIT mode.
RI	I/O	9-bit RECEIVE input/output.
TI	I/O	9-bit TRANSMIT input/output.

2610 tbl 02

FUNCTION TABLE[1]

IDT54/74FCT861/863 (Non-Inverting)

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	RI	TI	RI	TI	Function
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	High Z

NOTE: 2610 tbl 03

1. H = HIGH, L = LOW, Z = High Impedance, X = Don't Care, N/A = Not Applicable.

FUNCTION TABLE[1]

IDT54/74FCT864 (Inverting)

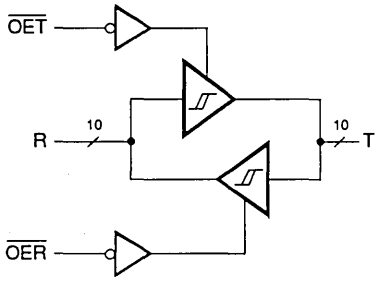
Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	RI	TI	RI	TI	Function
L	H	L	N/A	N/A	H	Transmitting
L	H	H	N/A	N/A	L	Transmitting
H	L	N/A	L	H	N/A	Receiving
H	L	N/A	H	L	N/A	Receiving
H	H	X	X	Z	Z	High Z

NOTE: 2610 tbl 04

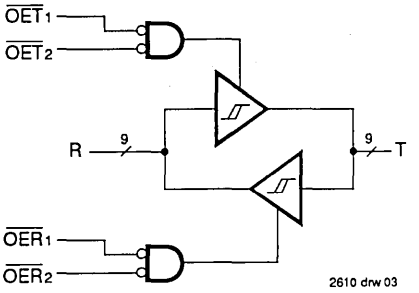
1. H = HIGH, L = LOW, Z = High Impedance, X = Don't Care, N/A = Not Applicable.

LOGIC SYMBOLS

IDT54/74FCT861



IDT54/74FCT863/864



2610 drw 03

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	−0.5 to V_{CC}	−0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2610 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2610 tbl 06

1. This parameter is guaranteed by characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	-5(4)	µA
			V_I = GND	—	—	-5	
I_{IH}	Input HIGH Current (I/O pins Only)	V_{CC} = Max.	V_I = V_{CC}	—	—	15	
			V_I = 2.7V	—	—	15(4)	
I_{IL}	Input LOW Current (I/O pins Only)		V_I = 0.5V	—	—	-15(4)	
			V_I = GND	—	—	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-75	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -15mA MIL.	2.4	4.3	—	
			I_{OH} = -24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}(4)	
			I_{OL} = 32mA MIL.(5)	—	0.3	0.5	
			I_{OL} = 48mA COM'L.(5)	—	0.3	0.5	

NOTES: 2610 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. These are maximum I_{OL} values per output, for 10 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 480mA for commercial and 320mA for military. Derate I_{OL} for number of outputs exceeding 10 turned on simultaneously.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OER}$ or $\overline{OET}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		$\overline{OER}$ or $\overline{OET}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
		$\overline{OER}$ or $\overline{OET}$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2610 tbl 08

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at VCC or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

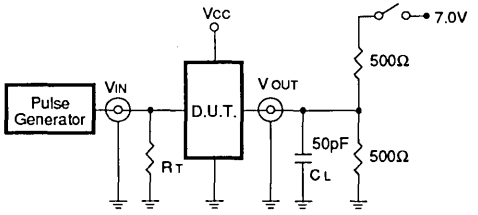
Symbol	Parameter	Condition[1]	FCT861A/863A/864A				FCT861B/863B/864B				FCT861C/863C/864C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay $\overline{RI}$ to TI or TI to $\overline{RI}$	CL = 50pF RL = 500Ω	—	8.0	—	9.0	—	6.0	—	6.5	—	—	—	—	ns
	FCT861/863	CL = 300pF[3] RL = 500Ω	—	15.0	—	17.0	—	13.0	—	14.0	—	—	—	—	ns
tPLH tPHL	Propagation Delay $\overline{RI}$ to TI or TI to $\overline{RI}$	CL = 50pF RL = 500Ω	—	7.5	—	9.0	—	5.5	—	6.5	—	—	—	—	ns
	FCT864	CL = 300pF[3] RL = 500Ω	—	14.0	—	16.0	—	13.0	—	14.0	—	—	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OET}$ to TI or	CL = 50pF RL = 500Ω	—	12.0	—	13.0	—	8.0	—	9.0	—	—	—	—	ns
	$\overline{OER}$ to $\overline{RI}$	CL = 300pF[3] RL = 500Ω	—	20.0	—	22.0	—	15.0	—	16.0	—	—	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OET}$ to TI or	CL = 5pF[3] RL = 500Ω	—	9.0	—	9.0	—	6.0	—	7.0	—	—	—	—	ns
	$\overline{OER}$ to $\overline{RI}$	CL = 50pF RL = 500Ω	—	10.0	—	10.0	—	7.0	—	8.0	—	—	—	—	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not tested.

2610 tbl 09

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

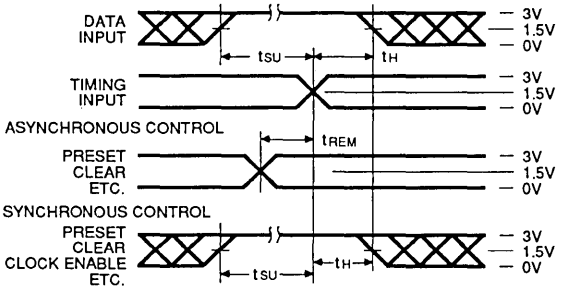
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2610 tbl 10

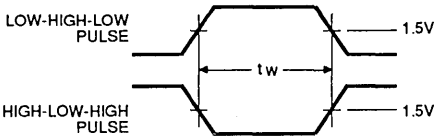
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

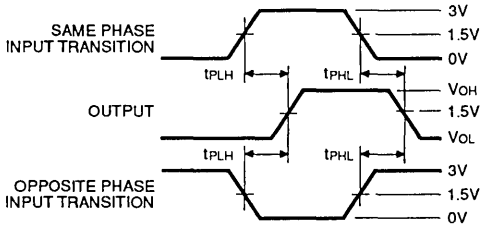
SET-UP, HOLD AND RELEASE TIMES



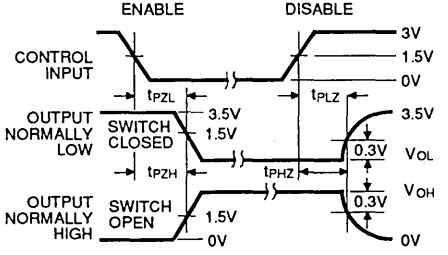
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



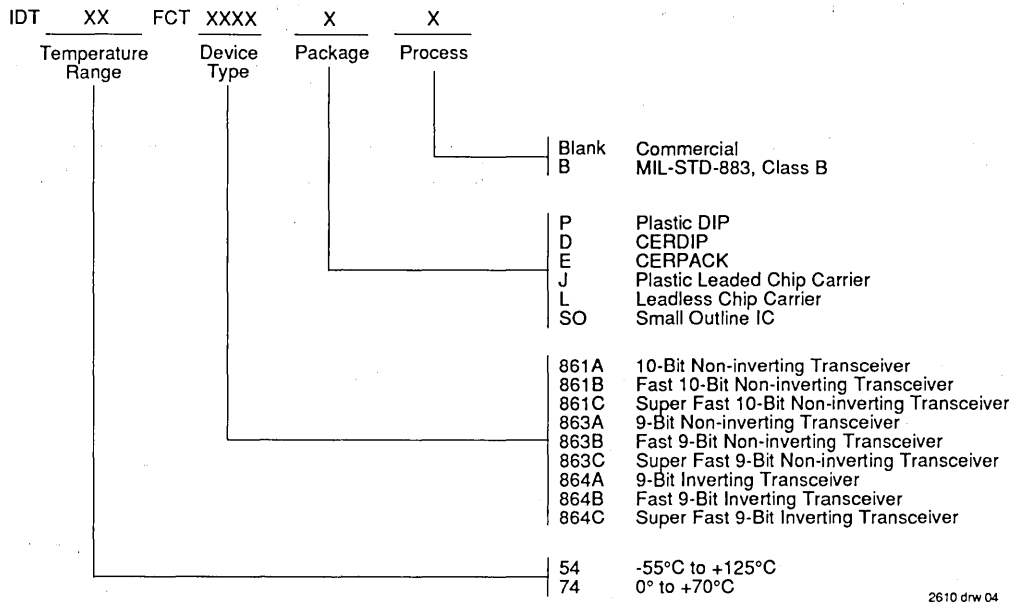
NOTES

2610 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS OCTAL BUFFER/LINE DRIVER

ADVANCE INFORMATION
IDT54/74FBT240
IDT54/74FBT240A
IDT54/74FBT240C

FEATURES:

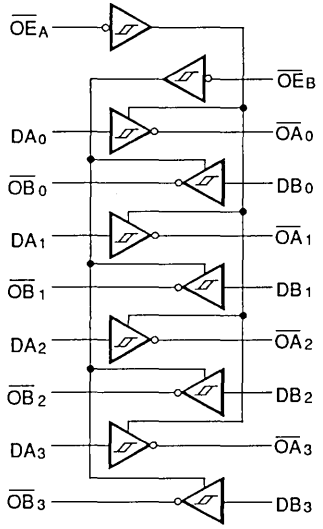
- IDT54/74FBT240 equivalent to 54/74BCT240
- **IDT54/74FBT240A 25% faster than the 240**
- **IDT54/74FBT240C 10% faster than the 240A**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The FBT series of BiCMOS Octal Buffers and Line Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

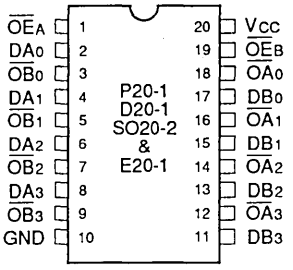
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM

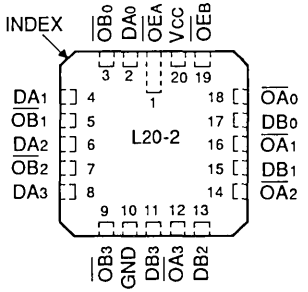


2644 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2644 drw 02

LCC
TOP VIEW

6

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
D_{XX}	Inputs
$\overline{O}_{XX}$	Outputs

2644 tbl 01

FUNCTION TABLE[1]

Inputs		Output
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	H
L	H	L
H	X	Z

NOTE: 2644 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2644 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2644 tbl 05

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.4	3.3	—	V
			I_{OH} = -18mA MIL. I_{OH}= -24mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2644 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	6.5[5]	
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	14.5[5]	

NOTES: 2644 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL HIgh Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

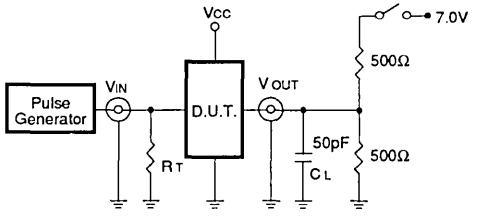
			IDT54/74FBT240				IDT54/74FBT240A				IDT54/74FBT240C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Dn to $\overline{On}$	C_L = 50pF R_L = 500Ω	1.5	5.6	—	—	1.5	4.8	—	—	1.5	4.3	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.8	—	—	1.5	6.2	—	—	1.5	5.0	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.1	—	—	1.5	5.6	—	—	1.5	4.5	—	—	ns

NOTES: 2644 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

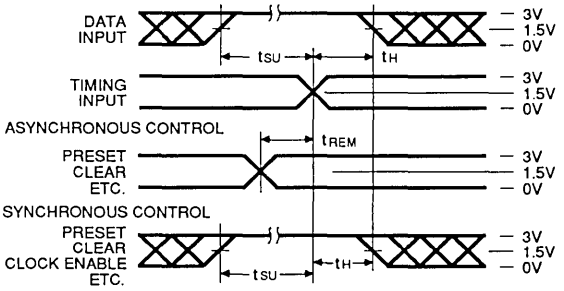
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2644 tbl 08

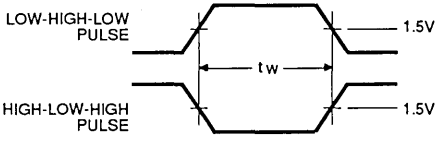
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

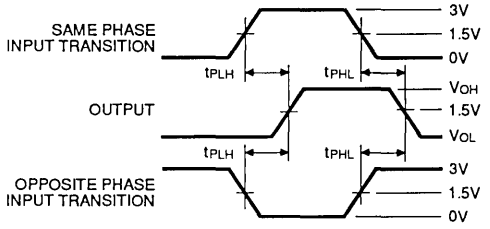
SET-UP, HOLD AND RELEASE TIMES



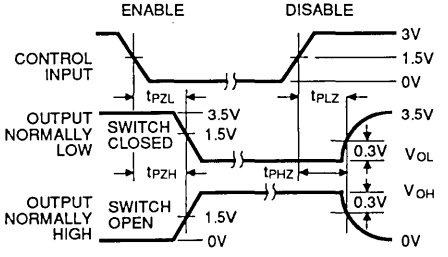
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



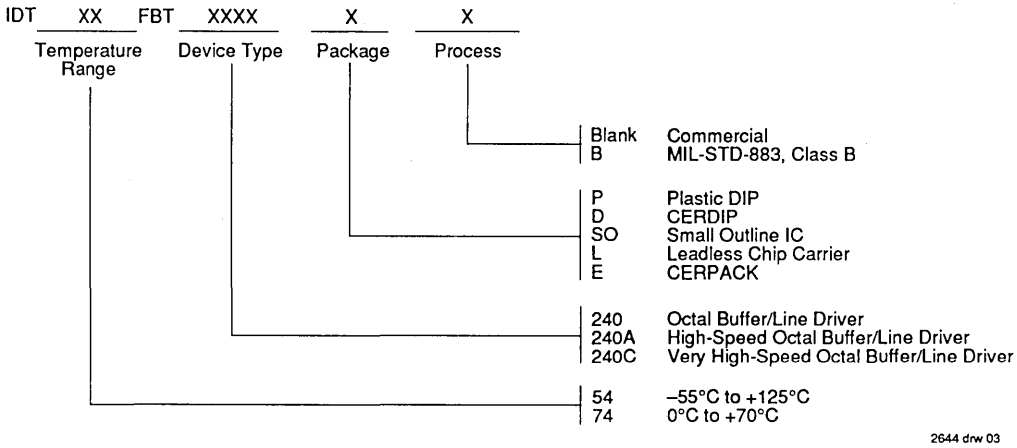
2644 drw 04

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS OCTAL BUFFER/LINE DRIVER

ADVANCE INFORMATION
IDT54/74FBT241
IDT54/74FBT241A
IDT54/74FBT241C

FEATURES:

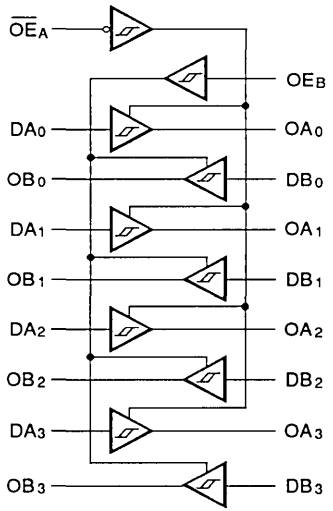
- IDT54/74FBT241 is equivalent to the 54/74BCT241
- **IDT54/74FBT241A is 25% faster than the 241**
- **IDT54/74FBT241C is 10% faster than the 241A**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The FBT series of BiCMOS Octal Buffers and Line Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

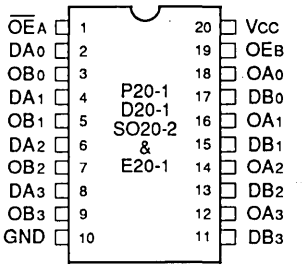
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads, with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM

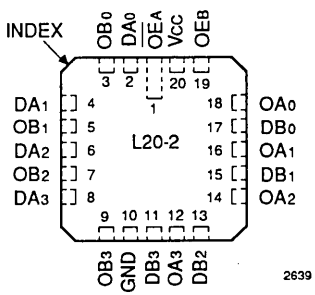


2639 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2639 drw 02

LCC
TOP VIEW

6

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, OE_B	3-State Output Enable Inputs
D_0 - D_7	Inputs
O_0 - O_7	Outputs

2639 tbl 01

FUNCTION TABLE(1)

Inputs			Output
$\overline{OE}_A$	OE_B	D	
L	H	L	L
L	H	H	H
H	L	X	Z

NOTE: 2639 tbl 02

1. H = HIGH
   L = LOW
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2639 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2639 tbl 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	-150	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -12mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15mA COM'L.				
			I_{OH} = -18mA MIL.	2.0	3.0	—	V
			I_{OH} = -24mA COM'L.				
V_{OL}	Output LOW Voltage		I_{OL} = 48mA MIL.	—	0.3	0.55	V
			I_{OL} = 64mA COM'L.				
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2639 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ = OE_B = GND, One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}$ = OE_B = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	6.5[5]	
		$\overline{OE}_A$ = GND, OE_B = V_{CC} All Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	14.5[5]	

NOTES: 2639 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

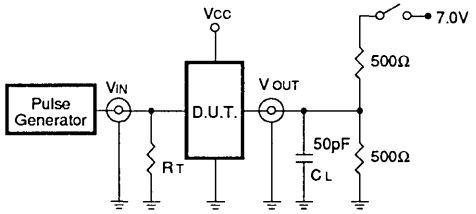
			IDT54/74FBT241				IDT54/74FBT241A				IDT54/74FBT241C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Dn to On	C_L = 50pF R_L = 500Ω	1.5	5.9	—	—	1.5	4.8	—	—	1.5	4.1	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.7	—	—	1.5	6.2	—	—	1.5	5.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.1	—	—	1.5	5.6	—	—	1.5	5.2	—	—	ns

NOTES: 2639 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



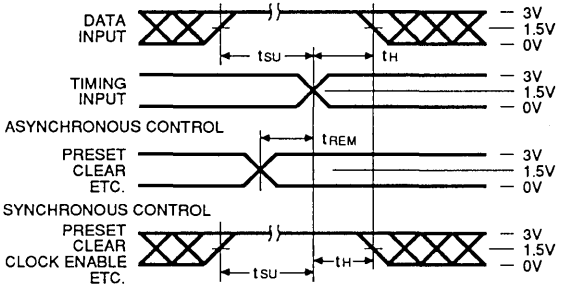
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

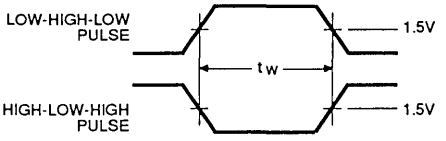
DEFINITIONS: 2639 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

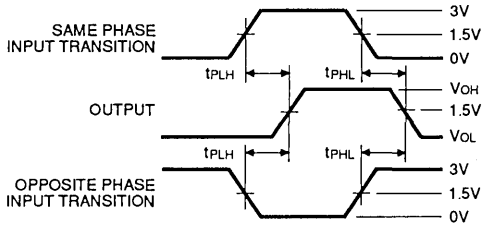
SET-UP, HOLD AND RELEASE TIMES



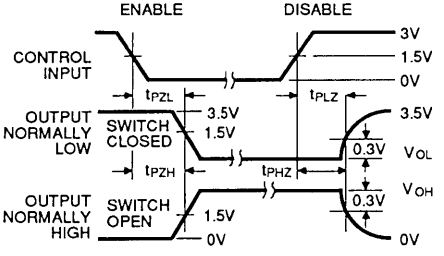
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

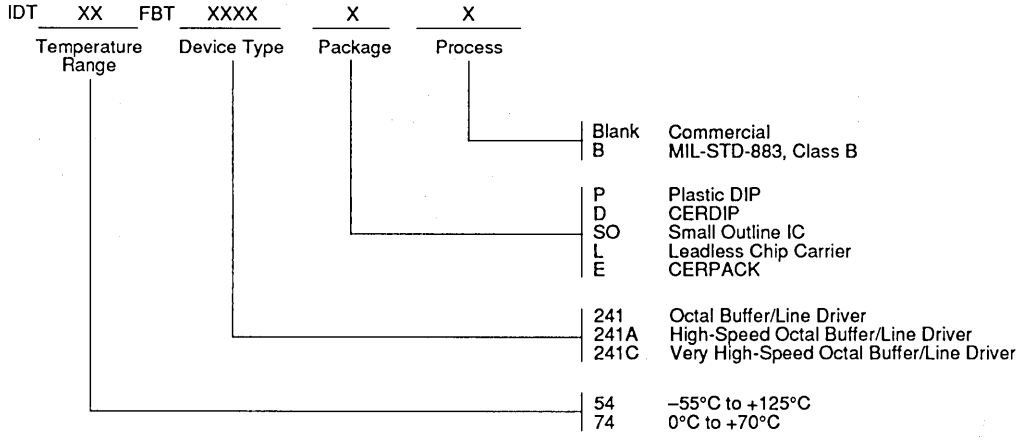


NOTES 2639 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2639 drw 03

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS OCTAL BUFFER/LINE DRIVER

ADVANCE INFORMATION
IDT54/74FBT244
IDT54/74FBT244A
IDT54/74FBT244C

FEATURES:

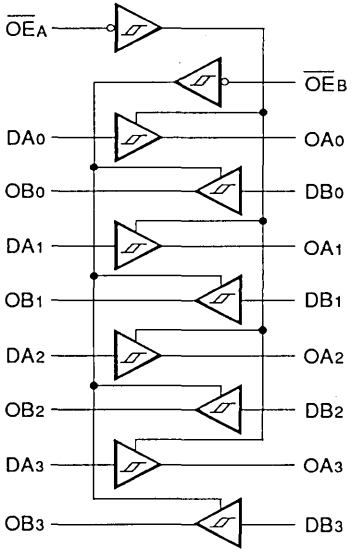
- IDT54/74FBT244 is equivalent to the 54/74BCT244
- **IDT54/74FBT244A is 25% faster than the 244**
- **IDT54/74FBT244C is 10% faster than the 244A**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The FBT series of BiCMOS Octal Buffers and Line Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

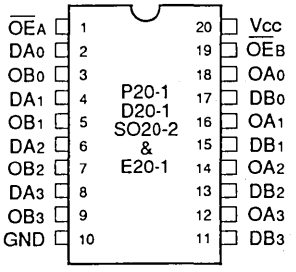
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM

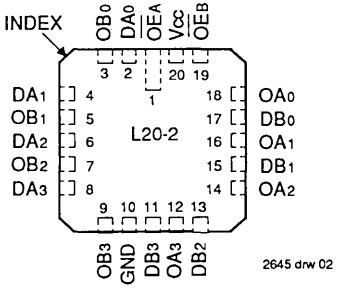


2645 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2645 drw 02

LCC
TOP VIEW

6

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs
D_{XX}	Inputs
O_{XX}	Outputs

2645 tbl 01

FUNCTION TABLE

Inputs		Output
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	L
L	H	H
H	X	Z

NOTE: 2645 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2646 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2645 tbl 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.4	3.3	—	V
			I_{OH} = -18mA MIL. I_{OH} = -24mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2645 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	6.5[5]	
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	14.5[5]	

2645 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

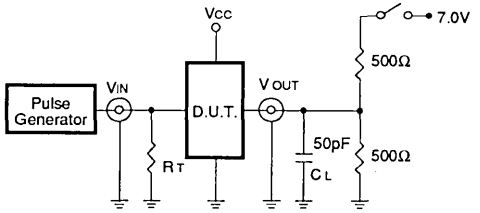
			IDT54/74FBT244				IDT54/74FBT244A				IDT54/74FBT244C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Dn to On	C_L = 50pF R_L = 500Ω	1.5	5.5	—	—	1.5	4.8	—	—	1.5	4.1	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.7	—	—	1.5	6.2	—	—	1.5	5.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.7	—	—	1.5	5.6	—	—	1.5	5.2	—	—	ns

2645 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



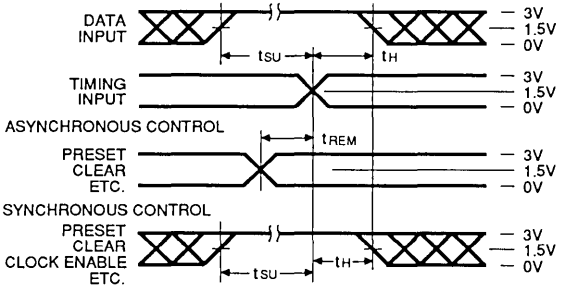
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

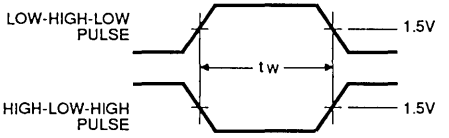
DEFINITIONS: 2645 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

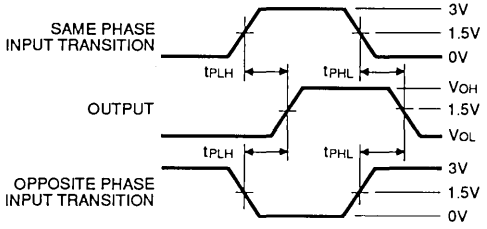
SET-UP, HOLD AND RELEASE TIMES



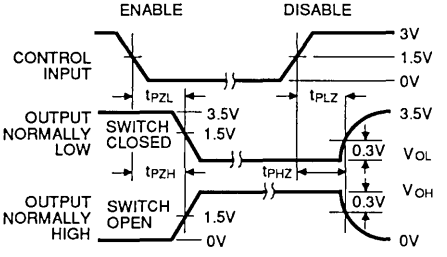
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

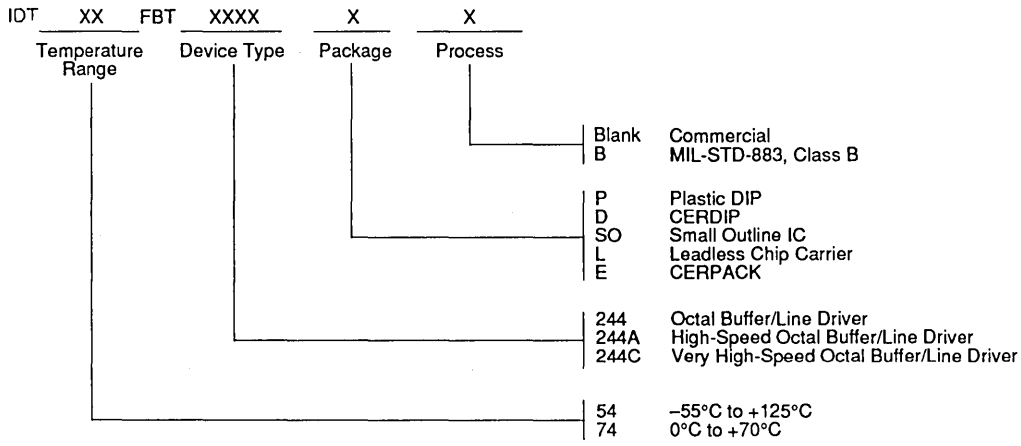


NOTES 2645 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2645 drw 03

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS NON-INVERTING BUFFER TRANSCEIVER

ADVANCE INFORMATION
IDT54/74FBT245
IDT54/74FBT245A
IDT54/74FBT245C

FEATURES:

- IDT54/74FBT245 equivalent to the 54/74BCT245
- **IDT54/74FBT245A 25% faster than the 245**
- **IDT54/74FBT245C 10% faster than the 245A**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

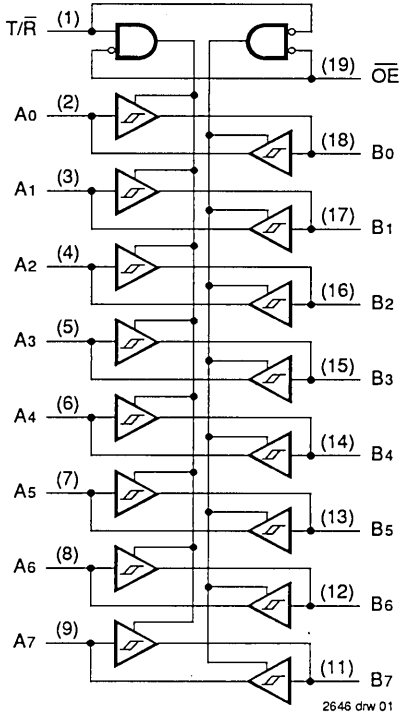
DESCRIPTION:

The FBT series of BiCMOS Buffer Transceivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

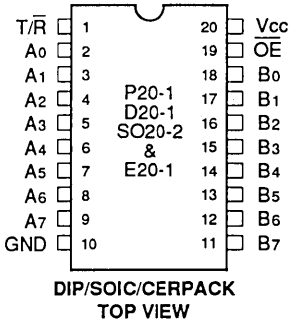
The IDT54/74FBT245 series of 8-bit non-inverting, bidirectional buffers have 3-state outputs and are intended for bus interface applications. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports. Receive (active LOW) enables data from B ports to A ports. The Output Enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in the high impedance state.

The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

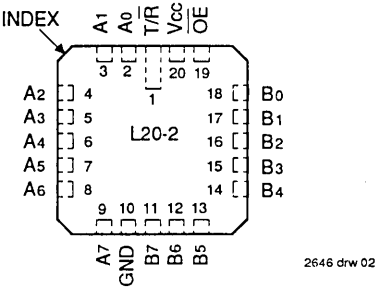
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

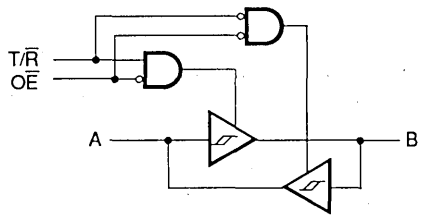
BiCEMOS is a trademark of Integrated Device Technology Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
$A_0 - A_7$	Side A Inputs or 3-State Outputs
$B_0 - B_7$	Side B Inputs or 3-State Outputs

2646 tbl 01

LOGIC SYMBOL



2646 drw 03

FUNCTION TABLE(1)

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

2646 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2646 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2646 tbl 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	Except I/O Pins	—	—	10	µA
		V_I = 2.7V	I/O Pins	—	—	60	
I_{IL}	Input LOW Current	V_{CC} = Max.	Except I/O Pins	—	—	-10	µA
		V_I = 0.5V	I/O Pins	—	—	-60	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -12mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15mA COM'L.				
			I_{OH} = -18mA MIL.	2.0	3.0	—	V
			I_{OH} = -24mA COM'L.				
V_{OL}	Output LOW Voltage		I_{OL} = 48mA MIL.	—	0.3	0.55	V
			I_{OL} = 64mA COM'L.				
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2646 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND, T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		T/$\overline{R}$ = $\overline{OE}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	6.5[5]	
		T/$\overline{R}$ = $\overline{OE}$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	14.5[5]	

NOTES:

2646 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FBT245				IDT54/74FBT245A				IDT54/74FBT245C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50pF R_L = 500Ω	1.5	7.0	—	—	1.5	4.9	—	—	1.5	4.1	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		1.5	10.9	—	—	1.5	6.2	—	—	1.5	5.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		1.5	9.1	—	—	1.5	5.0	—	—	1.5	4.8	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B		1.5	10.9	—	—	1.5	6.2	—	—	1.5	5.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time T/$\overline{R}$ to A or B		1.5	9.1	—	—	1.5	5.0	—	—	1.5	4.8	—	—	ns

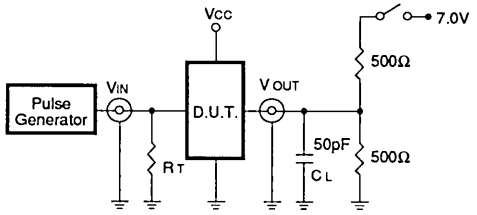
NOTES:

2646 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



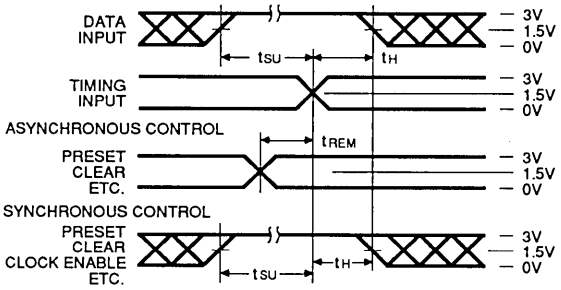
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

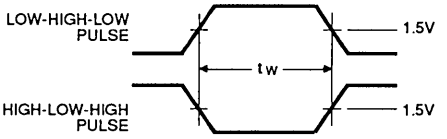
DEFINITIONS: 2646 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

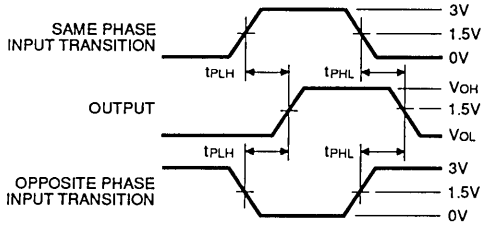
SET-UP, HOLD AND RELEASE TIMES



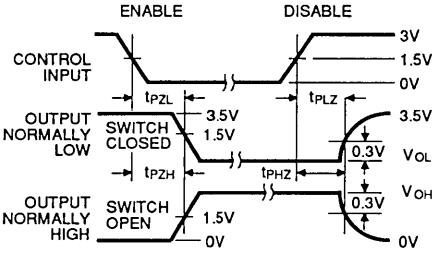
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

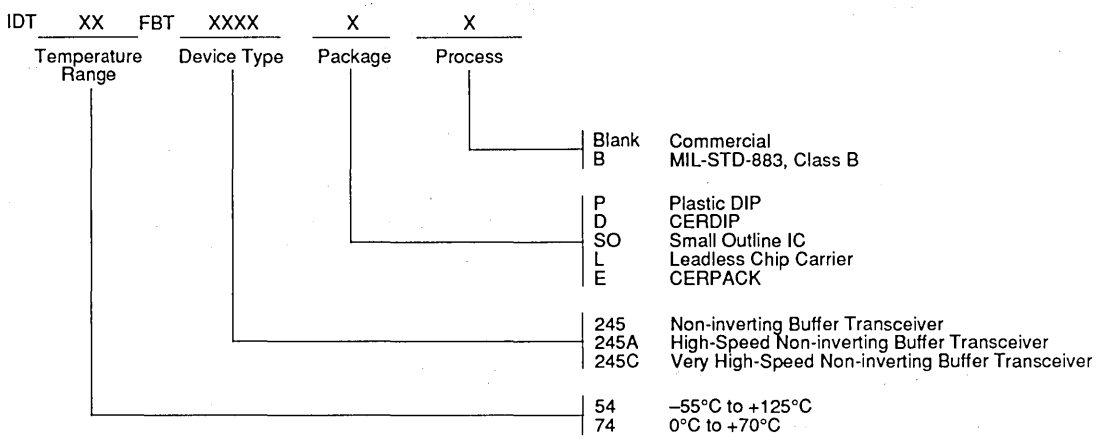


NOTES 2646 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2646 drw 04

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS OCTAL TRANSPARENT LATCH

ADVANCE INFORMATION
IDT54/74FBT373
IDT54/74FBT373A
IDT54/74FBT373C

FEATURES:

- Functionally equivalent to 54/74BCT373
- **IDT54/74FBT373A 30% faster than the 373**
- **IDT54/74FBT373C 15% faster than the 373A**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

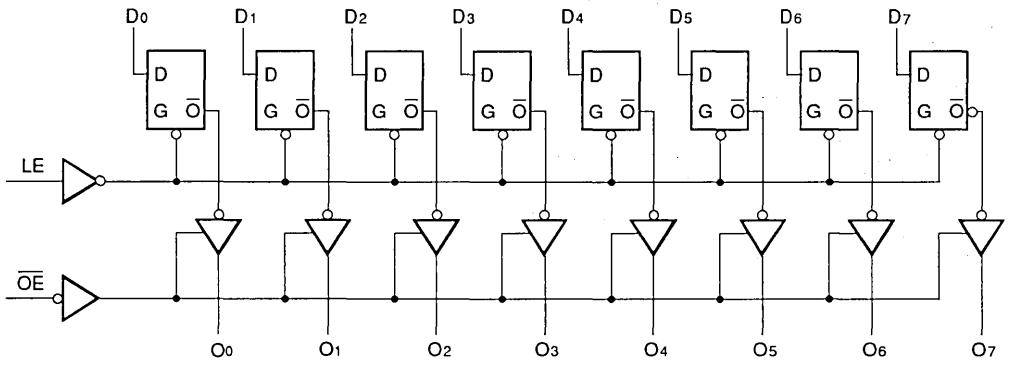
DESCRIPTION:

The FBT series of BiCMOS Octal Transparent Latches are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT373 series are 3-state, 8-bit latches for Bus Driving applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

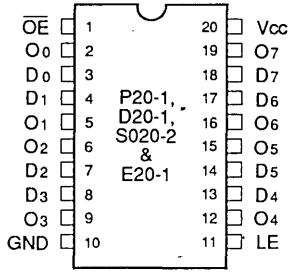
The FBT series of bus interface devices are ideal for use in designs needed to drive large capacitive loads with low static (DC) current loading. All inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM

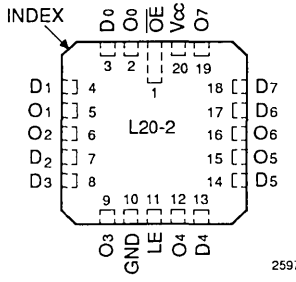


2597 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2597 drw 02

LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Techology, Inc.

PIN DESCRIPTION

Pin Names	Description
$D_0 - D_7$	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
$O_0 - O_7$	3-State Latch Outputs

2597 tbl 05

FUNCTION TABLE[1]

Inputs		Outputs	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	L	L	Q_{n-1}
X	X	H	Z

NOTE: 2597 tbl 06

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2597 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2597 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	-150	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.4	3.3	—	V
			I_{OH} = -18mA MIL. I_{OH} = -24mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:
2597 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz $\overline{OE}$ = GND 50% Duty Cycle LE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz $\overline{OE}$ = GND 50% Duty Cycle LE = V_{CC} Eight Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	—	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	—	14.5[5]	

NOTES:

2597 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FBT373				IDT54/74FBT373A				IDT54/74FBT373C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Dn to On	C_L = 50pF R_L = 500Ω	1.5	9.3	—	—	1.5	5.2	—	—	—	4.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	11.8	—	—	1.5	6.5	—	—	—	5.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	—	—	1.5	5.5	—	—	—	5.0	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay LE to On		—	8.8	—	—	2.0	8.5	—	—	—	5.5	—	—	ns
t_{SU}	Set-up time HIGH or LOW Dn to LE		2.0	—	—	—	2.0	—	—	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW Dn to LE		5.5	—	—	—	1.5	—	—	—	1.5	—	—	—	ns
t_W	LE Pulse Width HIGH or LOW		7.5	—	—	—	5.0	—	—	—	5.0	—	—	—	ns

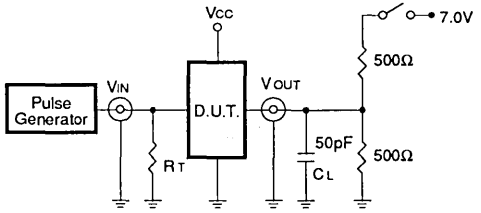
NOTES:

2597 tbl 07

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



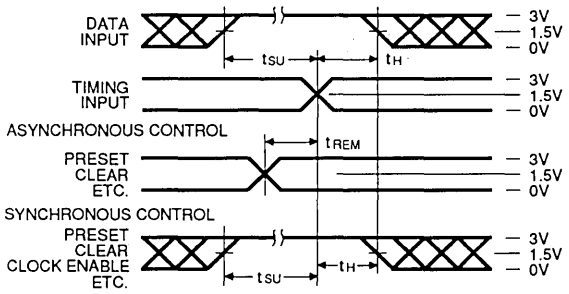
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

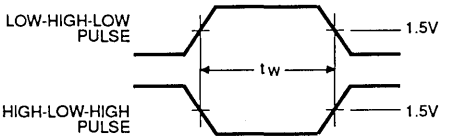
DEFINITIONS: 2597 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

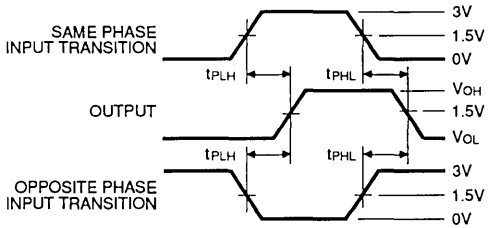
SET-UP, HOLD AND RELEASE TIMES



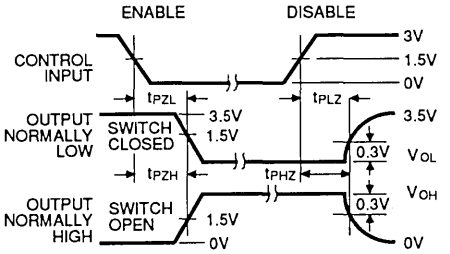
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

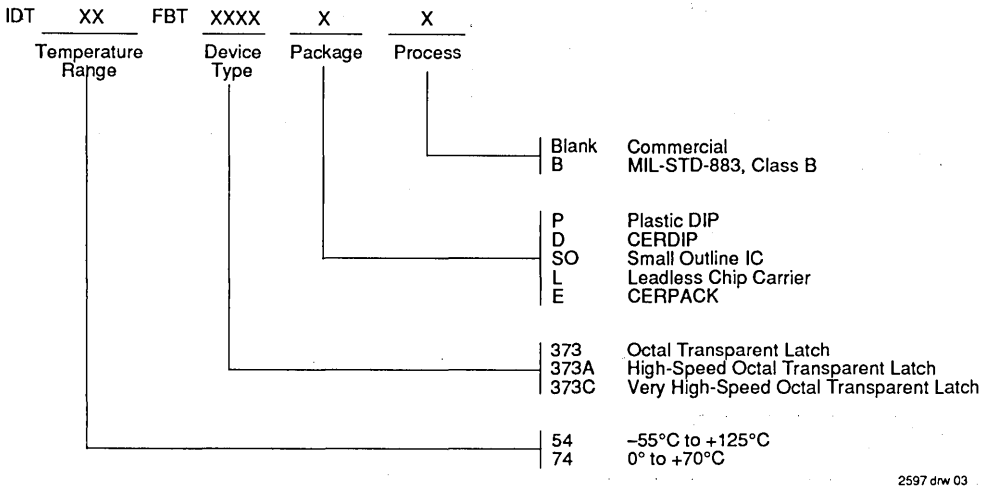


NOTES 2597 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS OCTAL D REGISTER (3-STATE)

ADVANCE INFORMATION
IDT54/74FBT374
IDT54/74FBT374A
IDT54/74FBT374C

FEATURES:

- IDT54/74FBT374 equivalent to the 54/74BCT374
- **IDT54/74FBT374A 25% faster than the 374**
- **IDT54/74FBT374C 10% faster than the 374A**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

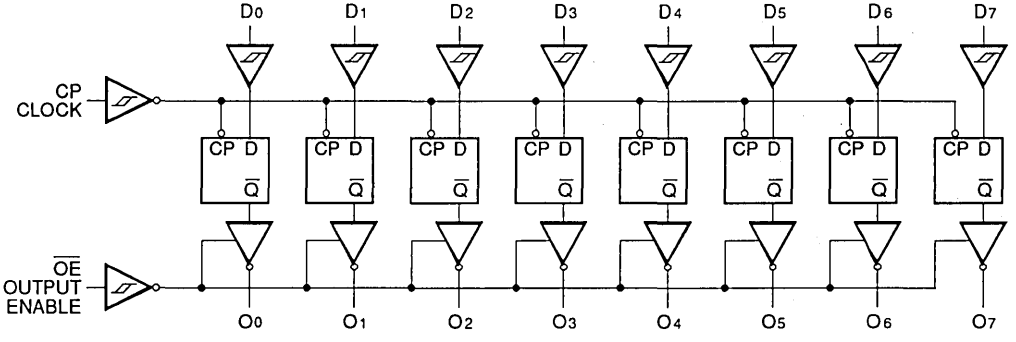
The FBT series of BiCMOS Octal D Registers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT374 series are 8-bit registers consisting of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the Output Enable ($\overline{OE}$) is LOW, the eight outputs are enabled. When $\overline{OE}$ is HIGH, the outputs are in the three-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

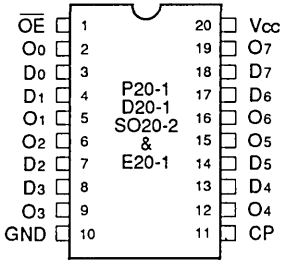
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM

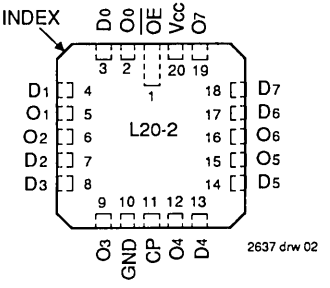


2637 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2637 drw 02

LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
D_0-D_7	The D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
O_0-O_7	The register three-state outputs.
$\overline{OE}$	Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

2637 tbl 01

FUNCTION TABLE[1]

	INPUTS			OUTPUTS	INTERNAL
Function	$\overline{OE}$	Clock	D_I	O_I	$\overline{Q}_I$
Load Register	L	∫	L	L	H
	L	∫	H	H	L
	H	∫	L	Z	H
	H	∫	H	Z	L

2637 tbl 02

NOTE:
1. H = HIGH
   L = LOW
   X = Don't Care
   Z = High Impedance
   ∫ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
2637 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
2637 tbl 05

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	-150	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -12mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15mA COM'L.				
			I_{OH} = -18mA MIL.	2.0	3.0	—	V
			I_{OH} = -24mA COM'L.				
V_{OL}	Output LOW Voltage		I_{OL} = 48mA MIL.	—	0.3	0.55	V
			I_{OL} = 64mA COM'L.				
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2637 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	7.8[5]	
		$\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	—	16.8[5]	

NOTES:

2637 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FBT374				IDT54/74FBT374A				IDT54/74FBT374C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay CP to On	C_L = 50pF R_L = 500Ω	2.0	10.0	—	—	2.0	6.5	—	—	—	5.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.3	—	—	1.5	6.5	—	—	—	5.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	6.8	—	—	1.5	5.5	—	—	—	5.0	—	—	ns
t_{SU}	Set-up Time HIGH or LOW D_n to CP		6.5	—	—	—	2.0	—	—	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW D_n to CP		0	—	—	—	1.5	—	—	—	1.5	—	—	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	—	—	—	5.0	—	—	—	5.0	—	—	—	ns

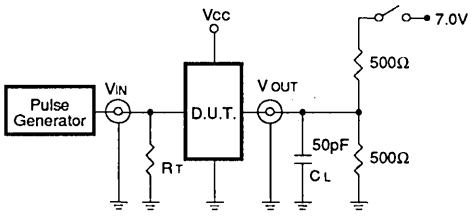
NOTES:

2637 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

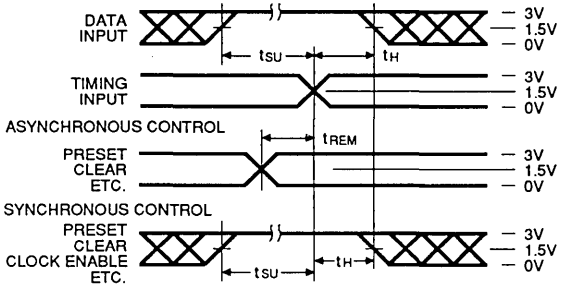
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2637 tbl 08

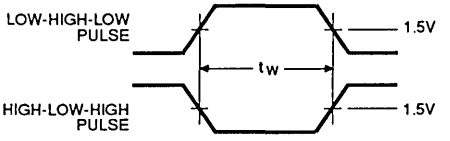
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

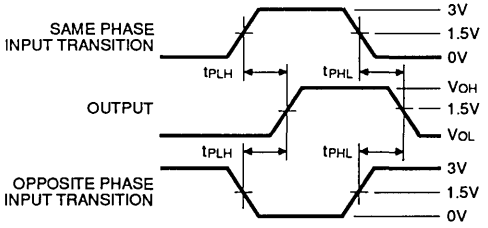
SET-UP, HOLD AND RELEASE TIMES



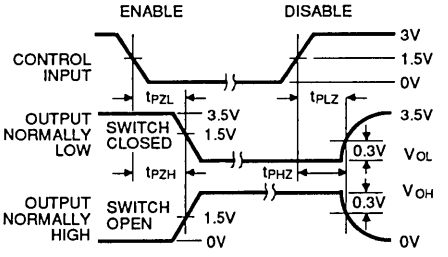
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



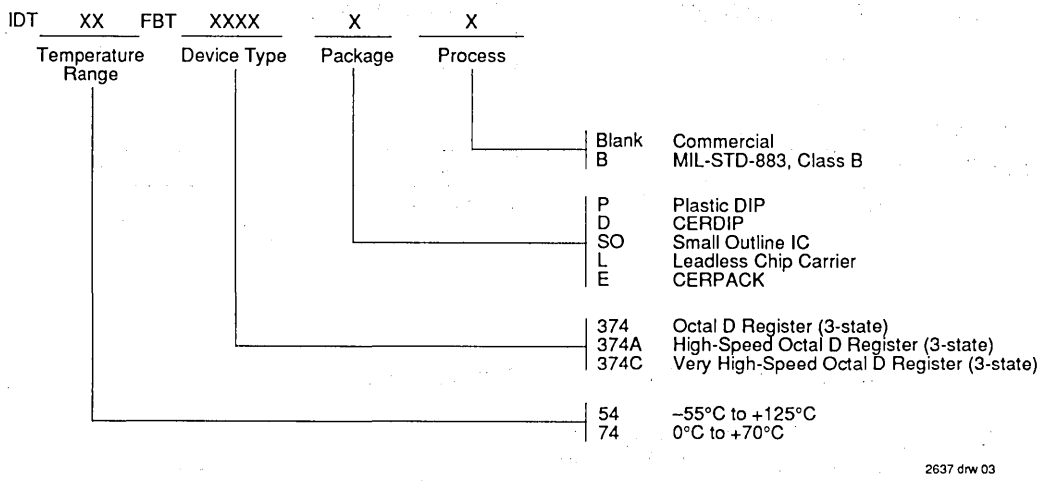
NOTES

2637 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2637 drw 03

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS OCTAL BUFFER/LINE DRIVERS

ADVANCE INFORMATION
IDT54/74FBT540/541
IDT54/74FBT540A/541A
IDT54/74FBT540C/541C

FEATURES:

- IDT54/74FBT540/541 equivalent to 54/74BCT540/541
- **IDT54/74FBT540/541A 25% faster than the 540/541**
- **IDT54/74FBT540/541C10% faster than the 540/541A**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

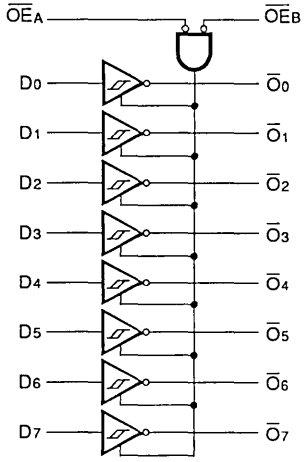
DESCRIPTION:

The FBT series of BiCMOS Octal Buffers and Line Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

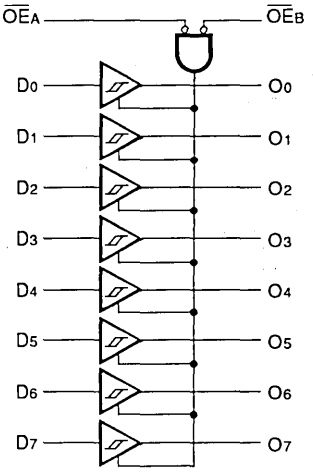
The IDT54/74FBT540 and IDT54/74FBT541 are similar in function to the 54/74FBT240 and 54/74FBT241, respectively, except that the inputs and outputs are on opposite sides of the packages. This pinout arrangement allows for easier layout and greater board density when designing output ports for microprocessors.

The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAMS



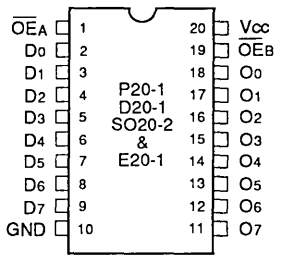
IDT54/74FCT540



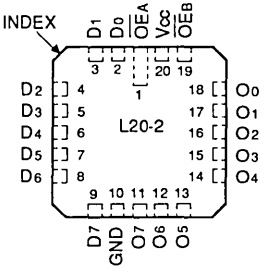
2636 drw 01

IDT54/74FCT541

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2636 drw 02

LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
D_0-D_7	Inputs
O_0-O_7	Outputs

2636 tbl 01

FUNCTION TABLE[1]

Inputs		Output	
$\overline{OE}_A$, $\overline{OE}_B$	D	540	541
L	L	H	L
L	H	L	H
H	X	Z	Z

NOTE: 2636 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2636 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2636 tbl 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.4	3.3	—	V
			I_{OH} = -18mA MIL. I_{OH}= -24mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2636 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	6.5[5]	
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	14.5[5]	

2636 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR 'FBT 540

Symbol	Parameter	Condition[1]	IDT54/74FBT540				IDT54/74FBT540A				IDT54/74FBT540C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Dn to On	CL = 50pF RL = 500Ω	1.5	6.9	—	—	1.5	4.8	—	—	1.5	4.3	—	—	ns
tPZH tPZL	Output Enable Time		1.5	10.1	—	—	1.5	6.2	—	—	1.5	5.8	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	8.5	—	—	1.5	5.6	—	—	1.5	5.2	—	—	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR 'FBT 541

Symbol	Parameter	Condition[1]	IDT54/74FBT541				IDT54/74FBT541A				IDT54/74FBT541C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Dn to On	CL = 50pF RL = 500Ω	1.5	8.2	—	—	1.5	4.8	—	—	1.5	4.1	—	—	ns
tPZH tPZL	Output Enable Time		1.5	10.7	—	—	1.5	6.2	—	—	1.5	5.8	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	8.6	—	—	1.5	5.6	—	—	1.5	5.2	—	—	ns

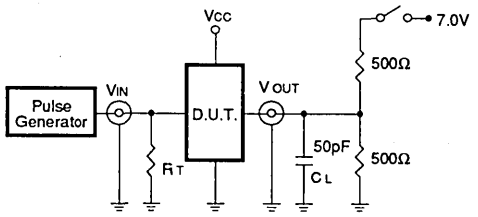
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2636 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

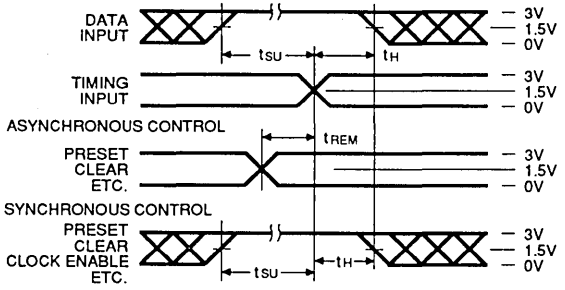
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2636 tbl 08

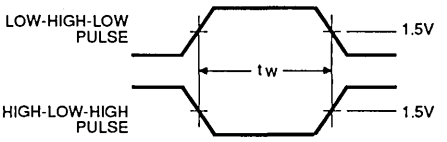
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

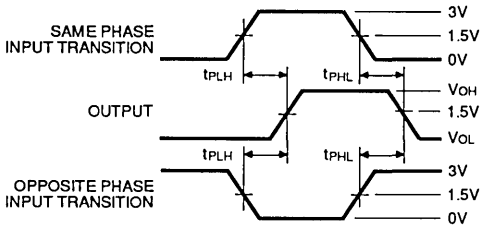
SET-UP, HOLD AND RELEASE TIMES



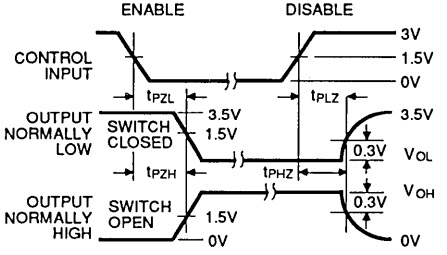
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

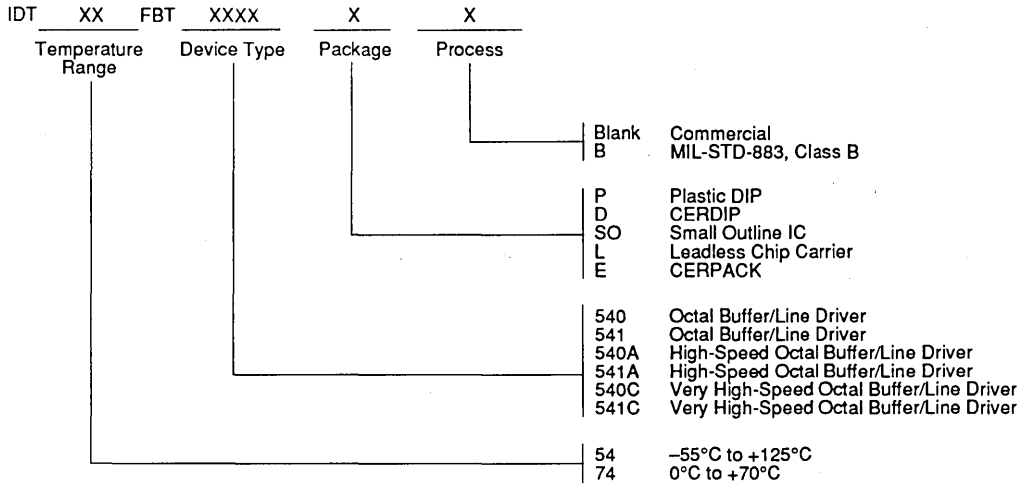


NOTES

2636 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2636 drw 03

6

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS 10-BIT REGISTER

ADVANCE INFORMATION
IDT54/74FBT821A
IDT54/74FBT821B
IDT54/74FBT821C

FEATURES:

- IDT54/74FBT821A equivalent to the 54/74BCT821
- **IDT54/74FBT821B 25% faster than the 821A**
- **IDT54/74FBT821C 10% faster than the 821B**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

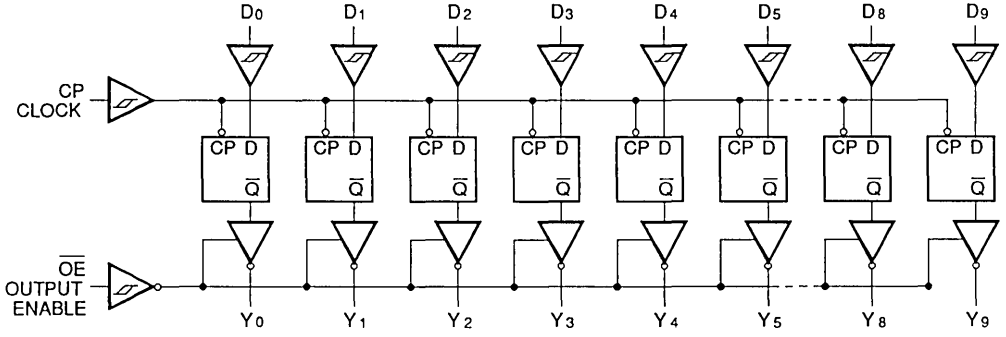
DESCRIPTION:

The FBT series of BiCMOS registers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT821A is a buffered, 10-bit wide version of the '374/'574 function.

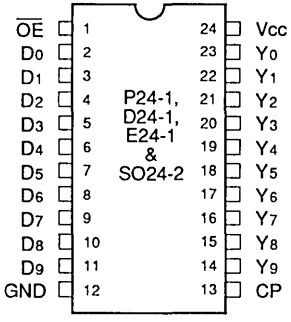
The FBT series of buffers are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM

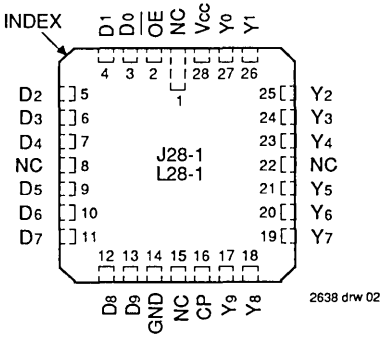


2638 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2638 drw 02

LCC/PLCC
TOP VIEW

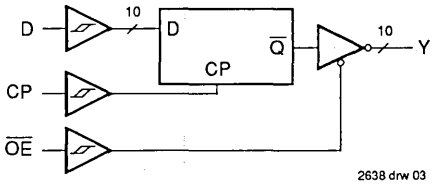
BiCEMOS is a trademark of Integrated Device Techology, Inc.

PIN DESCRIPTION

Pin Names	I/O	Description
D_0-D_9	I	The D flip-flop data inputs.
$\overline{OE}$	I	Three-state Output Enable input (Active LOW).
CP	I	Clock Pulse for the register; enters data into the register on the LOW-to-HIGH transition.
Y_0-Y_9	O	The register three-state outputs.

2638 tbl 01

LOGIC SYMBOL



2638 drw 03

FUNCTION TABLE[1]

Inputs			Output	
$\overline{OE}$	D_I	CP	Y_I	Function
H	L	↑	Z	Load Data
H	H	↑	Z	
L	L	↑	L	
L	H	↑	H	

NOTE: 2638 tbl 02

1. H = HIGH
   L = LOW
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2638 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2638 tbl 04

1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.4	3.3	—	V
			I_{OH} = -18mA MIL. I_{OH}= -24mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:

2638 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA/
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	7.8[5]	
		$\overline{OE}$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	17.8[5]	

2638 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

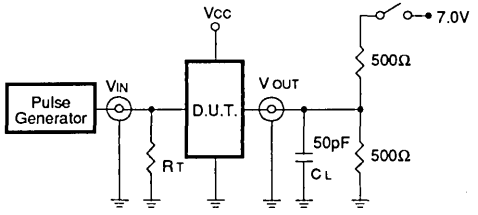
Symbol	Parameter	Condition[1]	IDT54/74FBT821A				IDT54/74FBT821B				IDT54/74FBT821C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Clock to YI ($\overline{OE}$ = LOW)	CL = 50pF RL = 500Ω	—	10.0	—	—	—	7.5	—	—	—	6.0	—	—	ns
tPZ tPZL	Output EnableTime $\overline{OE}$ to YI		—	12.0	—	—	—	8.0	—	—	—	7.0	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI		—	8.0	—	—	—	7.5	—	—	—	6.5	—	—	ns
tSU	Data to CP		—	7.0	—	—	—	3.0	—	—	—	3.0	—	—	ns
tH	Data to CP		—	1.0	—	—	—	1.0	—	—	—	1.0	—	—	ns
tW	Clock Pulse Width		—	7.0	—	—	—	5.0	—	—	—	5.0	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2638 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



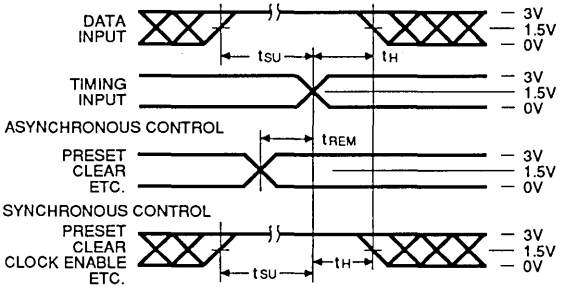
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

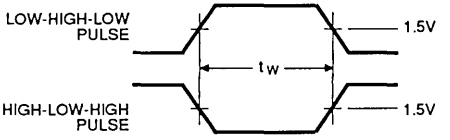
DEFINITIONS: 2638 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

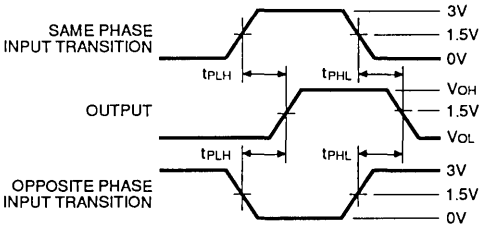
SET-UP, HOLD AND RELEASE TIMES



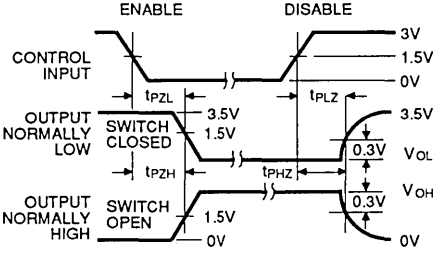
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

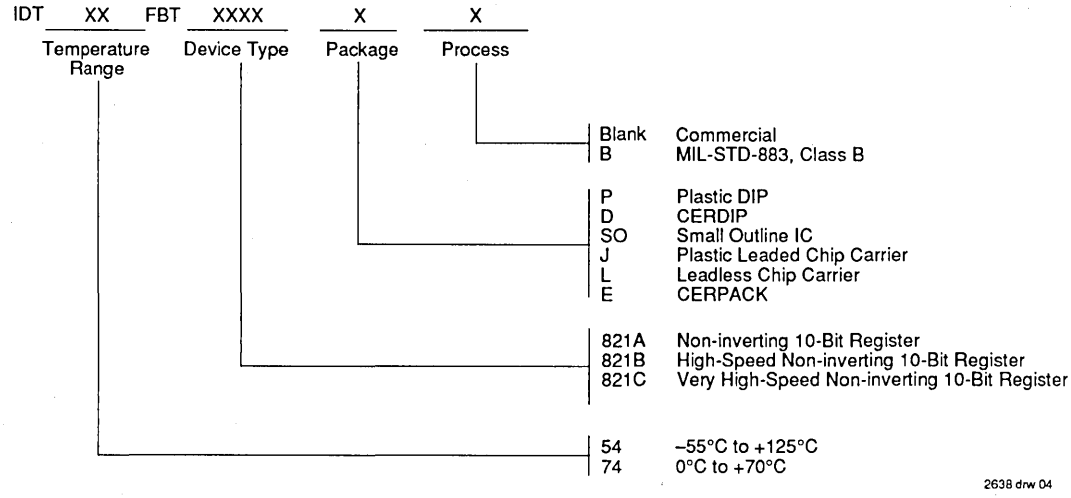


NOTES 2638 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2638 drw 04

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS 9-BIT REGISTER

ADVANCE INFORMATION
IDT54/74FBT823A
IDT54/74FBT823B
IDT54/74FBT823C

FEATURES:

- IDT54/74FBT823A equivalent to 54/74BCT823A
- **IDT54/74FBT823B 25% faster than the 823A**
- **IDT54/74FBT823C 10% faster than the 823B**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

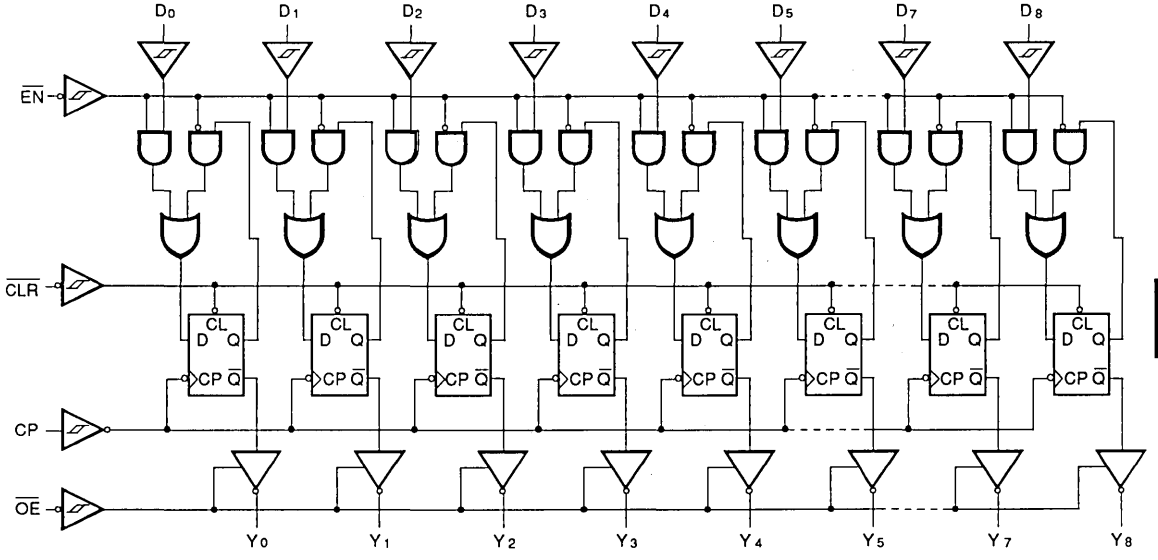
DESCRIPTION:

The FBT series of BiCMOS buffers and bus drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT823 is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$). The '823 is ideal for parity bus interfacing in high-peformance microprogrammed systems.

The FBT series of buffers are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM



2643 drw 01

6

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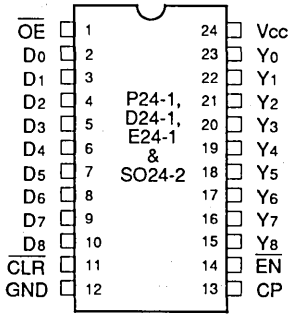
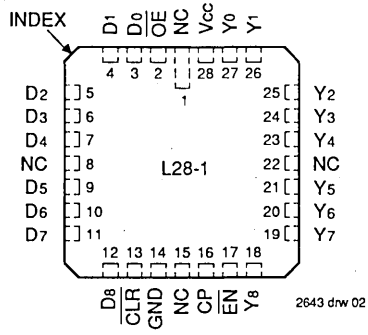
PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
D_{0-8}	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both inverting and non-inverting registers, when the clear input is LOW, the Q_I outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_0- Y_8	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the Clock Enable is LOW, data on the D_I input is transferred to the Q_I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_I outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_I outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_I outputs.

2643 tbl 05

FUNCTION TABLE[1]

Inputs					Internal Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	Function
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

2643 tbl 06

NOTE:
1. H = HIGH
   L = LOW
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2643 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2643 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = .5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = .5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.4	3.3	—	V
			I_{OH} = -18mA MIL. I_{OH} = -24mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2643 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max., Outputs Open V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = $\overline{GND}$ One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}$ = $\overline{GND}$ One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	7.2[5]	
		$\overline{OE}$ = $\overline{GND}$ Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	16.2[5]	

NOTES:

2643 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FBT823A				IDT54/74FBT823B				IDT54/74FBT823C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Clock to Yi ($\overline{OE}$ = LOW)	CL = 50pF RL = 500Ω	—	10	—	—	—	7.5	—	—	—	6.0	—	—	ns
tSU	Data to CP Set-up Time		7	—	—	—	3	—	—	—	3	—	—	—	ns
tH	Data CP Hold Time		1.5	—	—	—	1.5	—	—	—	1.5	—	—	—	ns
tSU	Enable ($\overline{EN}$) to CP Set-up Time		6	—	—	—	3	—	—	—	3	—	—	—	ns
tH	Enable ($\overline{EN}$) to CP Hold Time		0	—	—	—	0	—	—	—	0	—	—	—	ns
tPHL	Propagation Delay, Clear to Yi		—	12	—	—	—	9	—	—	—	8.0	—	—	ns
tREM	Clear Recovery ($\overline{CLR}$)Time		6	—	—	—	6	—	—	—	6	—	—	—	ns
tW	Clock Pulse Width		7	—	—	—	6	—	—	—	6	—	—	—	ns
tW	Clear ($\overline{CLR}$=LOW) Pulse Width		6	—	—	—	6	—	—	—	6	—	—	—	ns
tPZH tPZL	Output EnableTime $\overline{OE}$ to Yi		—	12	—	—	—	8	—	—	—	7.0	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Yi		—	8	—	—	—	7.5	—	—	—	6.5	—	—	ns

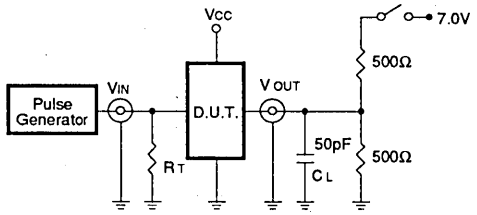
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2643 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



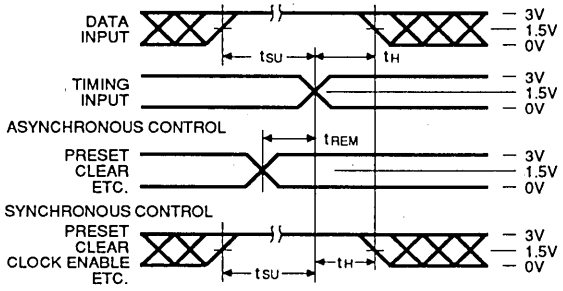
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

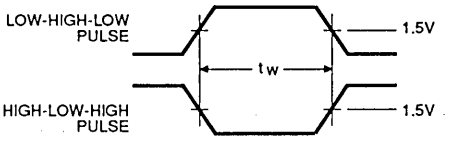
DEFINITIONS: 2643 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

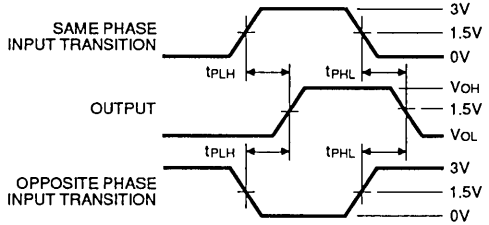
SET-UP, HOLD AND RELEASE TIMES



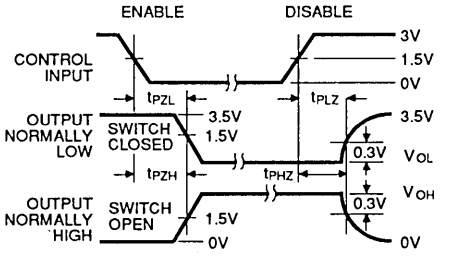
PULSE WIDTH



PROPAGATION DELAY



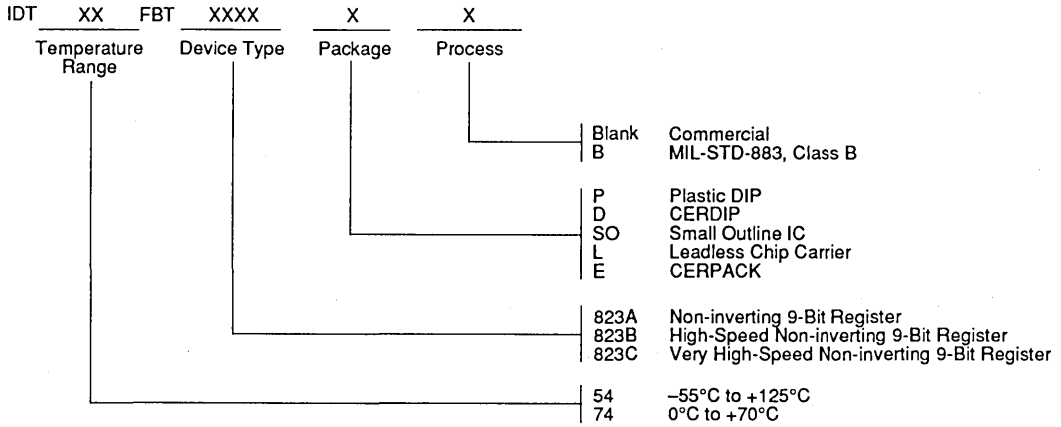
ENABLE AND DISABLE TIMES



NOTES 2643 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_O \leq 50\Omega$; $t_F \leq 2.5$ns; $t_R \leq 2.5$ns.

ORDERING INFORMATION



2643 drw 03

6

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS 10-BIT BUFFERS AND BUS DRIVERS

ADVANCE INFORMATION
IDT54/74FBT827A/B/C
IDT54/74FBT828A/B/C

FEATURES:

- Functionally equivalent to 54/74BCT827A/828A
- **IDT54/74FBT827B/828B 25% faster than the 827A/828A**
- **IDT54/74FBT827C/828C 10% faster than the 827B/828B**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ± 10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

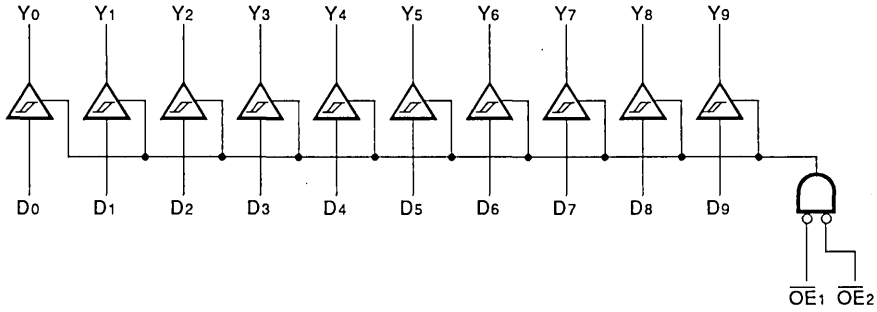
DESCRIPTION:

The FBT series of BiCMOS buffers and bus drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is desgined to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT827 and IDT54/74FBT828 are 3-state, 10-bit bus drivers. They provide bus interface to wide data/address paths or buses carrying parity. The output buffers are enabled when the two active-low output enable pins are both logic low.

The FBT series of buffers are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM[1]



2598 drw 01

NOTE:
1. Non-inverting part shown.

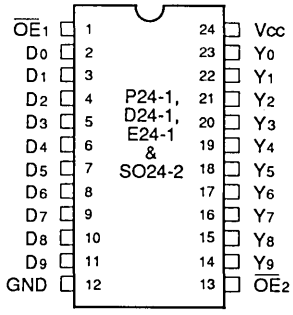
PRODUCT SELECTOR GUIDE

	10-Bit Buffers
Non-inverting	IDT54/74FBT827A/B/C
Inverting	IDT54/74FBT828A/B/C

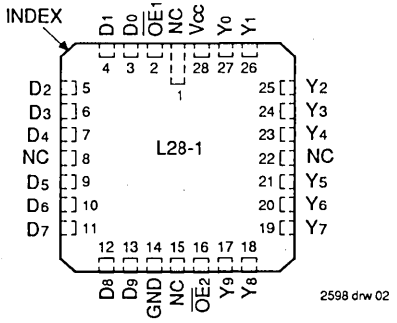
2598 tbl 01

BiCEMOS is a trademark of Integrated Device Techology, Inc.

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



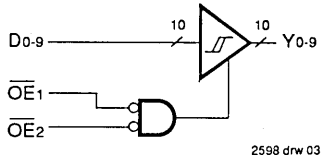
LCC
TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
$\overline{OE}_{1, 2}$	I	When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_0 - D_9	I	10-bit data input.
Y_0 - Y_9	O	10-bit data output.

2598 tbl 02

LOGIC SYMBOL



2598 drw 03

FUNCTION TABLES

IDT54/74FBT827A/B/C (NON-INVERTING)(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-state
X	H	X	Z	

NOTE:
1.H = HIGH, L = LOW, X = Don't Care, Z = High Impedance.

2598 tbl 03

IDT54/74FBT828A/B/C (INVERTING)(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	Three-state
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance.

2598 tbl 04

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES: 2598 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2598 tbl 06

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: TA = 0°C to +70°C, Vcc = 5.0V ± 10%; Military: TA = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
VIH	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
VIL	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
IIH	Input HIGH Current	Vcc = Max., VI = 2.7V		—	—	10	µA
IIL	Input LOW Current	Vcc = Max., VI = 0.5V		—	—	-10	µA
IOZH	High Impedance	Vcc = Max.	VO = 2.7V	—	—	50	µA
IOZL	Output Current		VO = 0.5V	—	—	-50	
II	Input HIGH Current	Vcc = Max., VI = 5.5V		—	—	100	µA
VIK	Clamp Diode Voltage	Vcc = Min., IN = -18mA		—	-0.7	-1.2	V
IOS	Short Circuit Current	Vcc = Max., VO = GND(3)		-75	-150	-225	mA
VOH	Output HIGH Voltage	Vcc = Min. VIN = VIH or VIL	IOH = -12mA MIL. IOH = -15mA COM'L.	2.4	3.3	—	V
			IOH = -18mA MIL. IOH = -24mA COM'L.	2.0	3.0	—	V
VOL	Output LOW Voltage		IOL = 32mA MIL. IOL = 48mA COM'L.	—	0.3	0.5	V
VH	Input Hysteresis	Vcc = 5V		—	200	—	mV
IOFF	Bus Leakage Current	Vcc = 0V, VO = 4.5V		—	—	100	µA
ICC	Quiescent Power Supply Current	Vcc = Max. VIN = GND or Vcc		—	0.2	1.5	mA

NOTES: 2598 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_1 = \overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}_1 = \overline{OE}_2$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	—	7.8[5]	
		$\overline{OE}_1 = \overline{OE}_2$ = GND Ten Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	17.8[5]	

2598 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz..

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FBT827A/B/C

			54/74FBT827A				54/74FBT827B				54/74FBT827C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPHL tPLH	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	—	7.0	—	—	—	5.0	—	—	—	4.4	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI		—	12.0	—	—	—	8.0	—	—	—	7.0	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI		—	12.0	—	—	—	7.0	—	—	—	6.0	—	—	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FBT828A/B/C

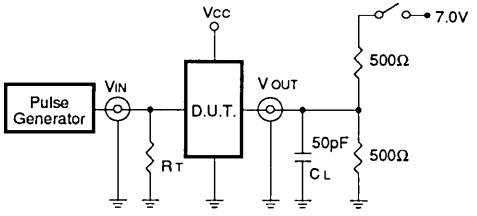
			54/74FBT828A				54/74FBT828B				54/74FBT828C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPHL tPLH	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	—	7.0	—	—	—	5.5	—	—	—	4.4	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI		—	11.0	—	—	—	8.0	—	—	—	7.0	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI		—	10.0	—	—	—	7.0	—	—	—	6.0	—	—	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed, but not tested.

2598 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



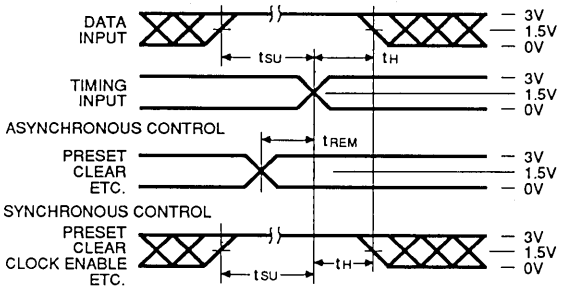
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

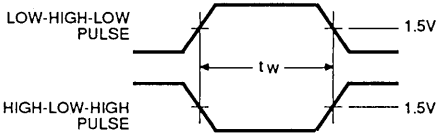
DEFINITIONS: 2598 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

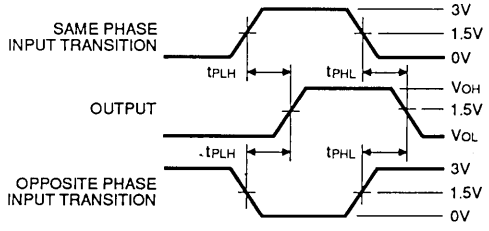
SET-UP, HOLD AND RELEASE TIMES



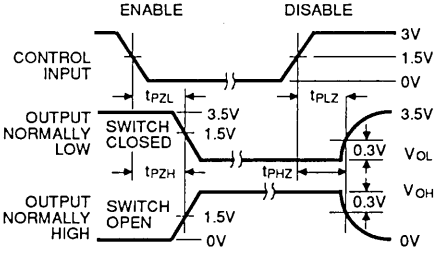
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

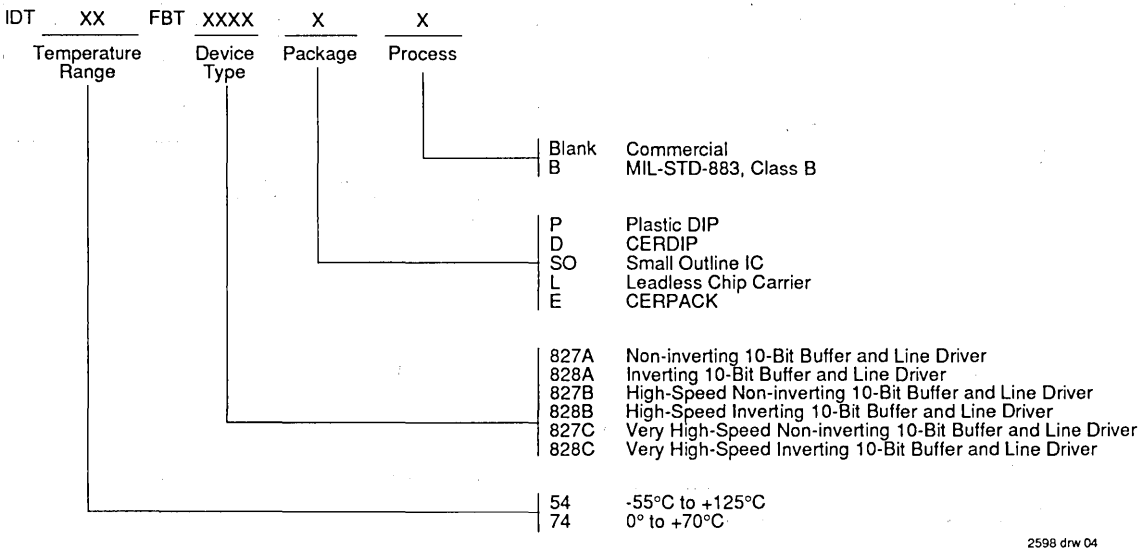


NOTES 2598 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2598 drw 04

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS 10-BIT INTERFACE LATCHES

ADVANCE INFORMATION
IDT54/74FBT841A
IDT54/74FBT841B
IDT54/74FBT841C

FEATURES:

- Functionally equivalent to the 54/74BCT841 series
- **IDT54/74FBT841B 20% faster than the 841A**
- **IDT54/74FBT841C 15% faster than the 841B**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

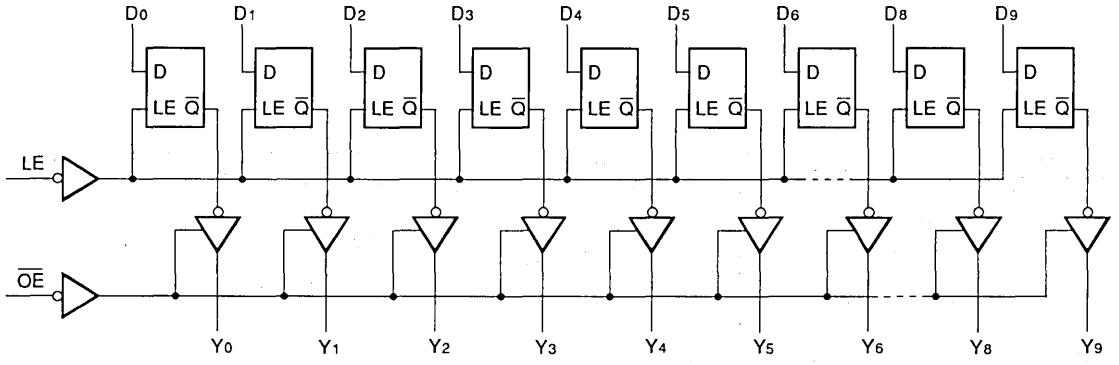
DESCRIPTION:

The FBT series of BiCMOS Bus Interface Latches are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is desgined to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT841 series are 3-state, 10-bit bus interface latches.

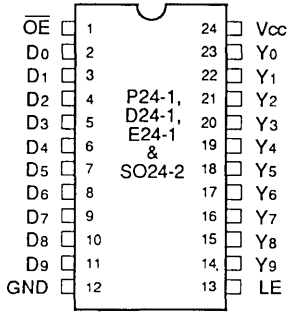
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static(DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM

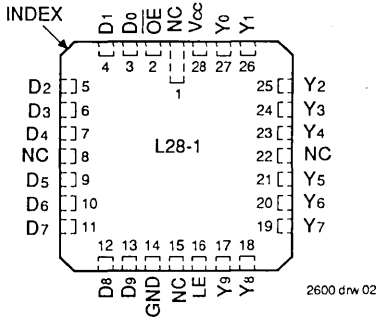


2600 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2600 drw 02

LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Techology, Inc.

PIN DESCRIPTION

Name	I/O	Description
D_{0-9}	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_{0-9}	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is high, the outputs Y_I are in the high-impedance (off) state.

2600 tbl 05

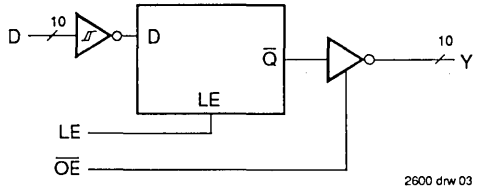
FUNCTION TABLE[1]

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

NOTE: 2600 tbl 06

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

LOGIC SYMBOL



2600 drw 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2600 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2600 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	-150	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.4	3.3	—	V
			I_{OH} = -18mA MIL. I_{OH} = -24mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:
2600 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not excedd one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling LE = V_{CC} 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}$ = GND, LE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	7.8[5]	
		$\overline{OE}$ = GND, LE = V_{CC} Ten Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	17.8[5]	

NOTES:

2600 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at VCC or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	54/74FBT841A				54/74FBT841B				54/74FBT841C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Data (DI) to Output (YI) (LE = HIGH)	CL = 50pF RL = 500Ω	—	8.0	—	—	—	6.5	—	—	—	5.5	—	—	ns
tPLH tPHL		CL = 300pF[3] RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
tSU	Data to LE Set-up Time	CL = 50pF	—	1.5	—	—	—	1.5	—	—	—	1.5	—	—	ns
tH	Data to LE Hold Time	RL = 500Ω	—	3.5	—	—	—	2.5	—	—	—	2.5	—	—	ns
tPLH tPHL	Latch Enable (LE) to YI	CL = 50pF RL = 500Ω	—	10.0	—	—	—	8.0	—	—	—	6.4	—	—	ns
tPLH tPHL		CL = 300pF[3] RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
tW	LE Pulse Width HIGH	CL = 50pF RL = 500Ω	—	4.0	—	—	—	4.0	—	—	—	4.0	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI	CL = 50pF RL = 500Ω	—	8.0	—	—	—	8.0	—	—	—	6.5	—	—	ns
tPZH tPZL		CL = 300pF[3] RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI	CL = 50pF[3] RL = 500Ω	—	15.0	—	—	—	7.0	—	—	—	6.0	—	—	ns
tPHZ tPLZ		CL = 50pF RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns

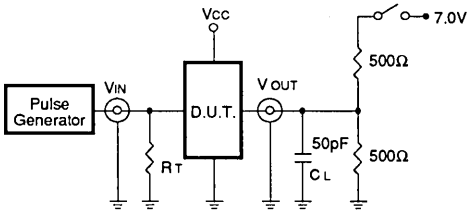
NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not tested.

2600 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

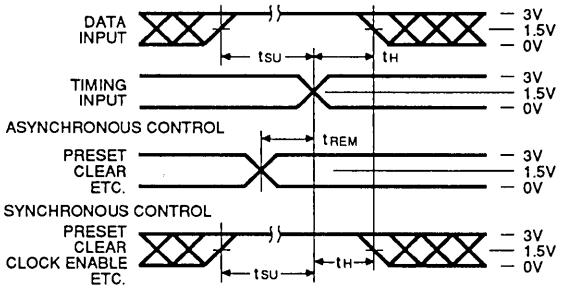
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2600 tbl 08

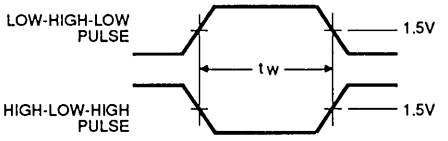
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

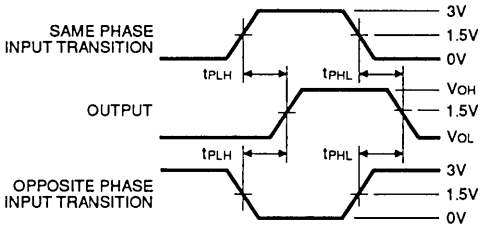
SET-UP, HOLD AND RELEASE TIMES



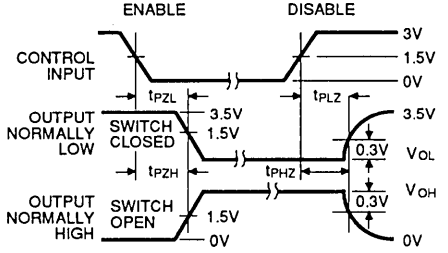
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

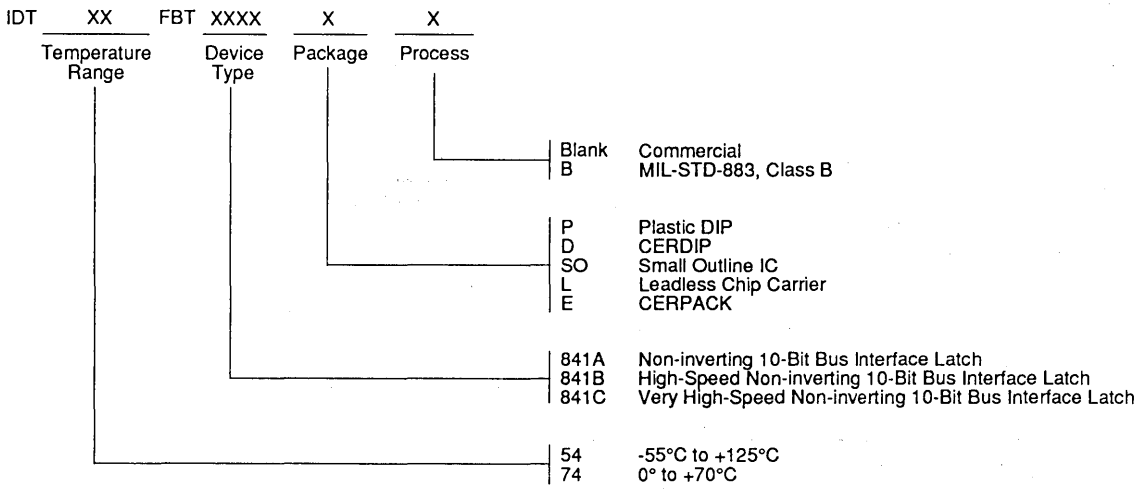


2600 drw 04

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2600 drw 04

6

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS MEMORY DRIVERS

ADVANCE INFORMATION
IDT54/74FBT2240
IDT54/74FBT2240A
IDT54/74FBT2240C

FEATURES:

- IDT54/74FBT2240 equivalent to the 54/74BCT2240
- **IDT54/74FBT2240A 25% faster than the 2240**
- **IDT54/74FBT2240C 10% faster than the 2240A**
- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

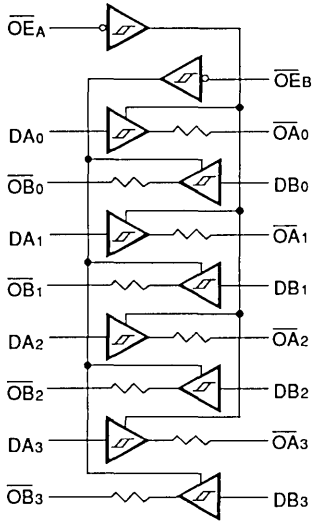
DESCRIPTION:

The FBT series of BiCMOS Memory Drivers is built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2240 series are octal buffers/line drivers where each output is terminated with a 25Ω series resistor.

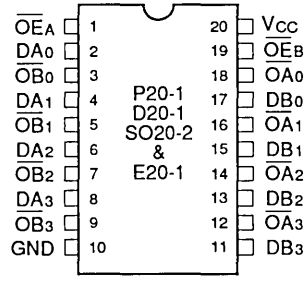
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. This higher output level in the high state will result in a significant reduction in overall system power dissipation.

FUNCTIONAL BLOCK DIAGRAM

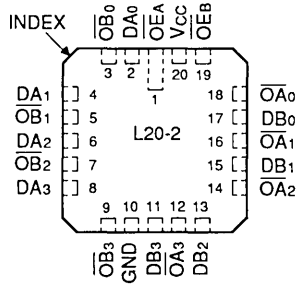


2642 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

2642 drw 02

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
D_0-D_7	Inputs
$\overline{O}_0$-$\overline{O}_7$	Outputs

2642 tbl 01

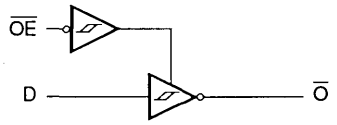
FUNCTION TABLE[1]

Inputs		Output
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	H
L	H	L
H	X	Z

NOTE: 2642 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

LOGIC SYMBOL



2642 drw 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2642 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2642 tbl 04

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = -18mA		—	-0.7	-1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2V		-35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-60	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -1mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA	2.0	3.0	—	
V_{OL}	Output LOW Voltage		I_{OL} = 1mA	—	0.15	0.5	V
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:

2642 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	6.5[5]	
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	14.5[5]	

NOTES: 2642 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL HIgh Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FBT2240				IDT54/74FBT2240A				IDT54/74FBT2240C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	1.5	5.7	—	—	—	—	—	—	—	—	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	9.3	—	—	—	—	—	—	—	—	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.7	—	—	—	—	—	—	—	—	—	—	ns

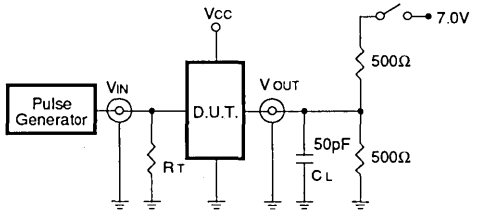
NOTES: 2642 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

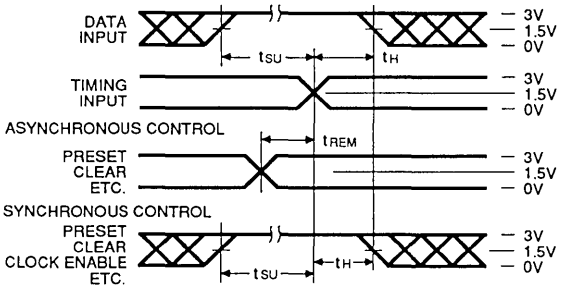
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2642 tbl 08

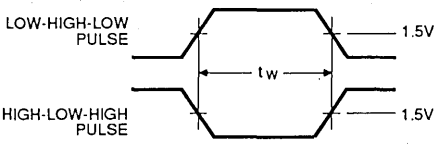
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

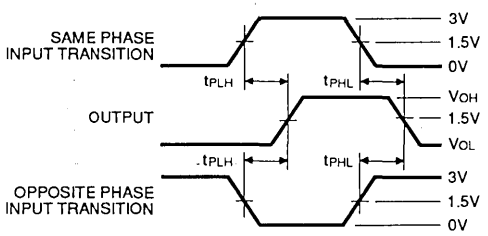
SET-UP, HOLD AND RELEASE TIMES



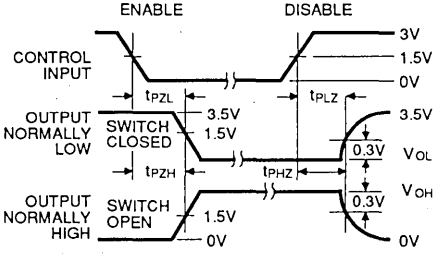
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

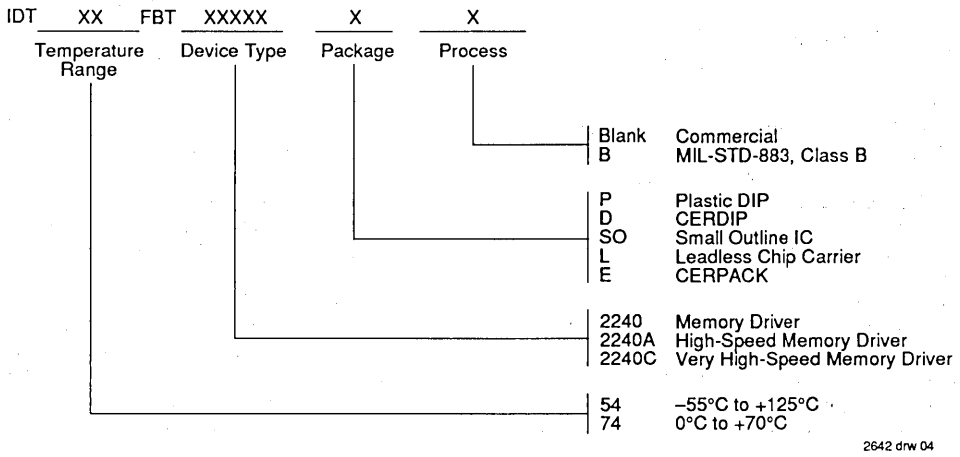


NOTES

2642 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2642 drw 04

6

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS MEMORY DRIVERS

ADVANCE INFORMATION
IDT54/74FBT2244
IDT54/74FBT2244A
IDT54/74FBT2244C

FEATURES:

- IDT54/74FBT2244 equivalent to the 54/74BCT2244
- **IDT54/74FBT2244A 25% faster than the 2244**
- **IDT54/74FBT2244C 10% faster than the 2244A**
- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

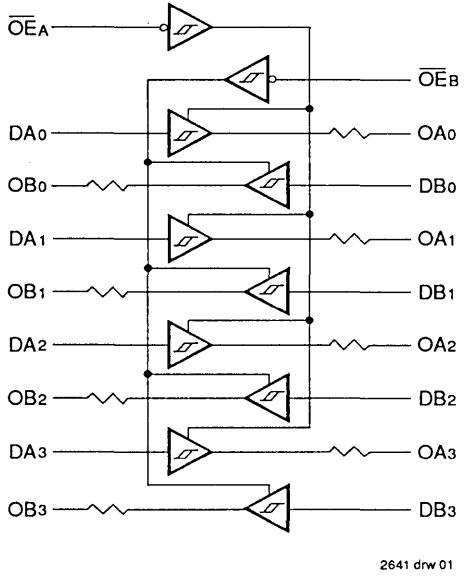
DESCRIPTION:

The FBT series of BiCMOS Memory Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2244 series are octal buffers/line drivers where each output is terminated with a 25Ω series resistor.

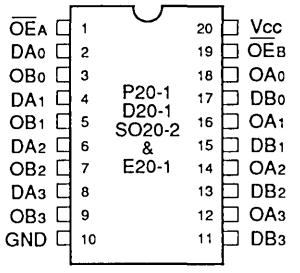
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. This higher output level in the high state will result in a significant reduction in overall system power dissipation.

FUNCTIONAL BLOCK DIAGRAM

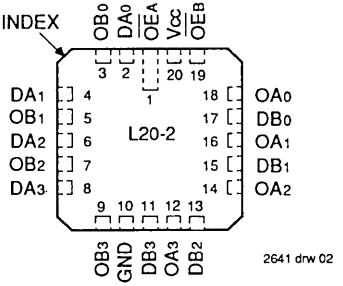


2641 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2641 drw 02

LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs
Dxx	Inputs
Oxx	Outputs

2641 tbl 01

FUNCTION TABLE[1]

Inputs		Output
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	L
L	H	H
H	X	Z

NOTE: 2641 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2641 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2641 tbl 04

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V[4]		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		-35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-60	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -1mA	2.4	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA	2.0	—	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 1mA	—	0.15	0.5	V
			I_{OL} = 12mA	—	0.35	0.8	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2641 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	6.5[5]	
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	14.5[5]	

NOTES:

2641 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FBT2244				IDT54/74FBT2244A				IDT54/74FBT2244C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	C_L = 50pF R_L = 500Ω	—	6.7	—	—	—	—	—	—	—	—	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		—	8.7	—	—	—	—	—	—	—	—	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		—	7.8	—	—	—	—	—	—	—	—	—	—	ns

NOTES:

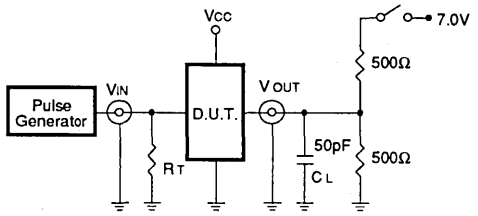
2641 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



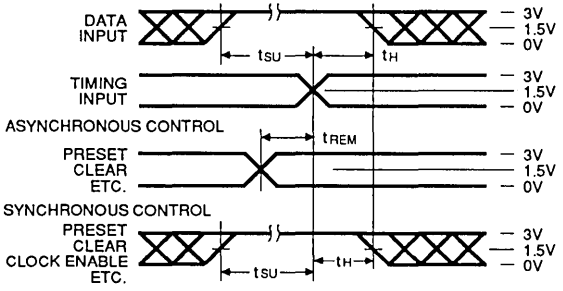
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

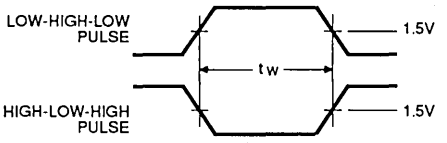
DEFINITIONS: 2641 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

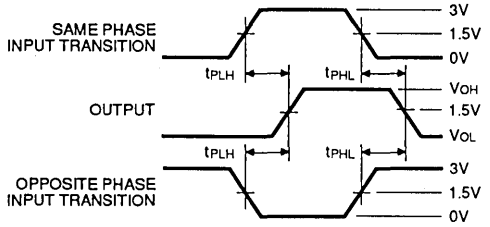
SET-UP, HOLD AND RELEASE TIMES



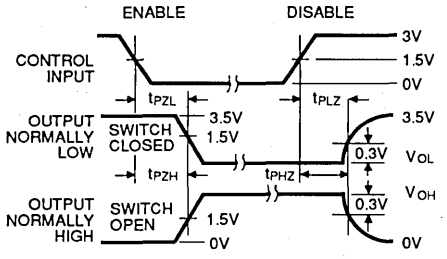
PULSE WIDTH



PROPAGATION DELAY



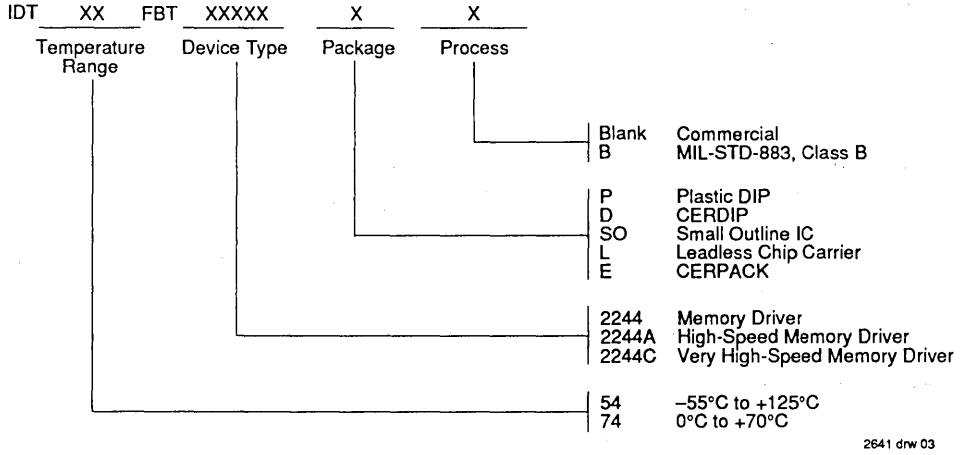
ENABLE AND DISABLE TIMES



NOTES 2641 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS OCTAL TRANSPARENT LATCH DRIVERS

ADVANCE INFORMATION
IDT54/74FBT2373
IDT54/74FBT2373A
IDT54/74FBT2373C

FEATURES:

- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

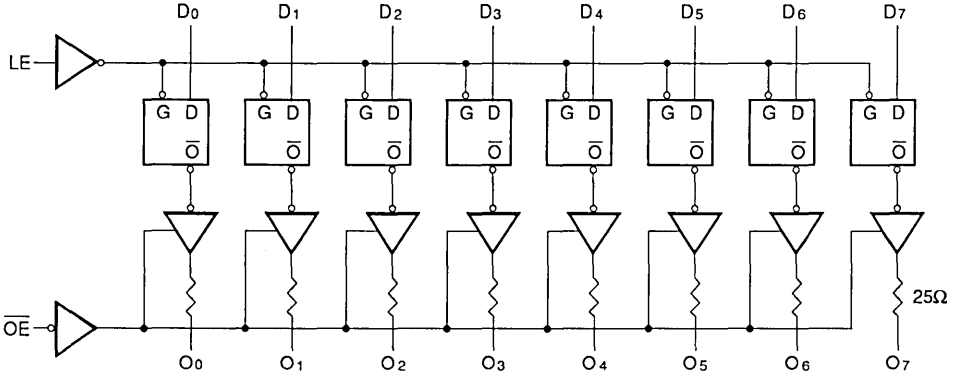
DESCRIPTION:

The FBT series of BiCMOS Latch Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2373 series are 3-state, 8-bit latches where each output is terminated with a 25Ω series resistor. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

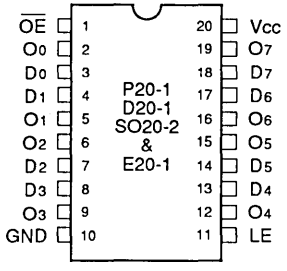
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. This higher output level in the high state will result in a significant reduction in overall system power dissipation.

FUNCTIONAL BLOCK DIAGRAM

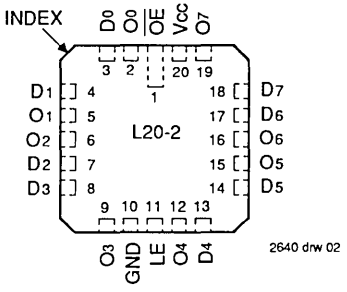


2640 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2640 drw 02

LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$D_0 - D_7$	Data Inputs
LE	Latch Enables Input (Active HIGH)
$\overline{OE}$	Output Enables Input (Active LOW)
$O_0 - O_7$	3-State Latch Outputs

2640 tbl 05

FUNCTION TABLE[1]

Inputs			Outputs
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	L	L	Q_n
X	X	H	Z

NOTE: 2640 tbl 06

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2640 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2640 tbl 02

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-60	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -1mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA COM'L.	2.0	3.2	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 1mA COM'L.	—	0.15	0.5	V
			I_{OL} = 12mA MIL.	—	0.35	0.8	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		-35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA

2640 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_1 = \overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}_1 = \overline{OE}_2$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	6.5[5]	
		$\overline{OE}_1 = \overline{OE}_2$ = GND Ten Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	14.5[5]	

2640 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTLI inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

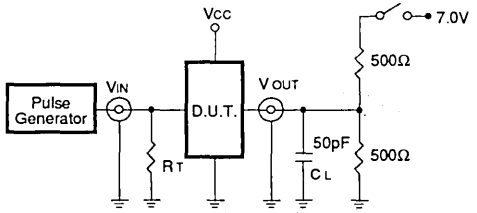
			IDT54/74FBT2373				IDT54/74FBT2373A				IDT54/74FBT2373C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	C_L = 50pF R_L = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		—	—	—	—	—	—	—	—	—	—	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		—	—	—	—	—	—	—	—	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		—	—	—	—	—	—	—	—	—	—	—	—	ns
t_{SU}	Set-up Time HIGH or LOW D_n to LE		—	—	—	—	—	—	—	—	—	—	—	—	ns
t_H	Hold Time HIGH or LOW D_n to LE		—	—	—	—	—	—	—	—	—	—	—	—	ns
t_W	LE Pulse Width HIGH or LOW		—	—	—	—	—	—	—	—	—	—	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2640 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



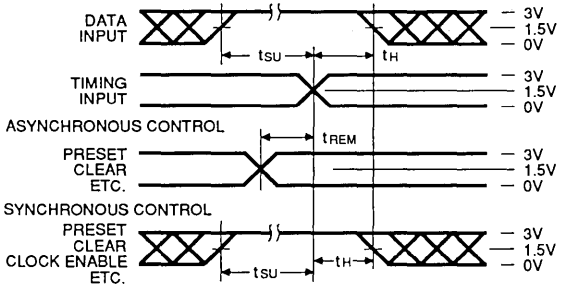
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

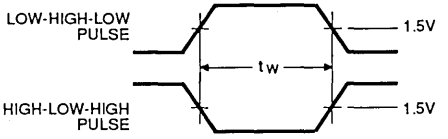
DEFINITIONS: 2640 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

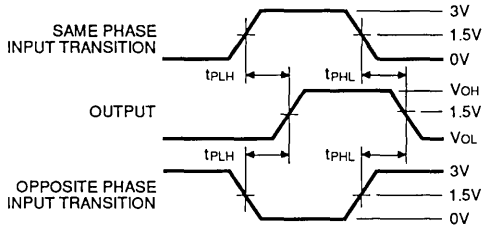
SET-UP, HOLD AND RELEASE TIMES



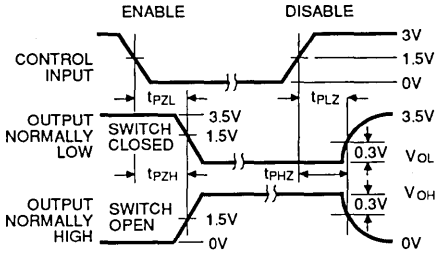
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

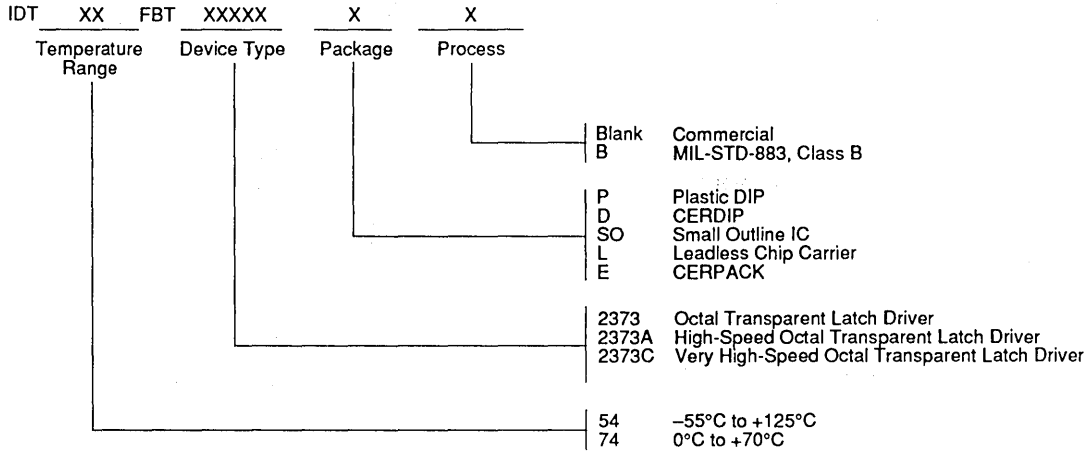


NOTES 2640 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2640 drw 03

Integrated Device Technology, Inc.

HIGH SPEED BiCMOS 10-BIT MEMORY DRIVERS

ADVANCE INFORMATION
IDT54/74FBT2827A/B
IDT54/74FBT2828A/B

FEATURES

- IDT54/74FBT2827A/2828A is equivalent to 54/74BCT2827A/2828A
- **IDT54/74FBT2827B/2828B is 30% faster than BCT**
- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

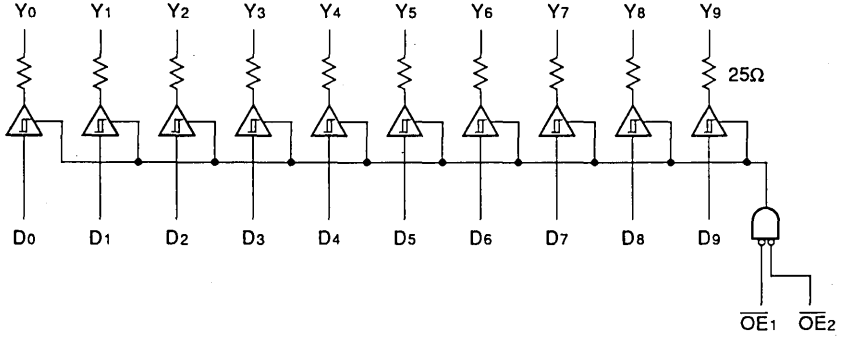
DESCRIPTION

The FBT series of BiCMOS Memory Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2827A/B and IDT54/74FBT2828A/B are 3-state 10-bit buffers where each output is terminated with a 25Ω series resistor. The output buffers are enabled when the two active-low output enable pins are logic low.

The FBT series of memory line drivers are ideal for use in designs needed to drive large capacitive loads, with low static (DC) current loading. They are also designed for rail-to-rail output switching. This higher output level in the high state will result in significant reduction in overall system power dissipation.

FUNCTIONAL BLOCK DIAGRAM



2516 drw 01

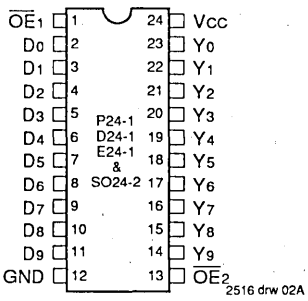
PRODUCT SELECTOR GUIDE

	10-Bit Memory Driver
Non-inverting	IDT 54/74FBT2827A/B
Inverting	IDT 54/74FBT2828A/B

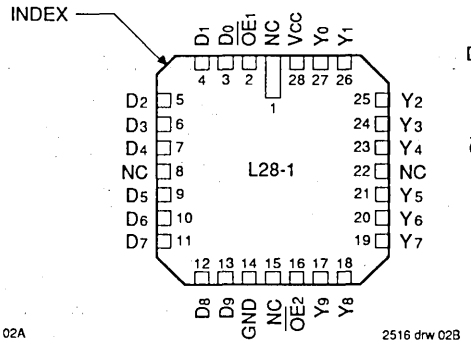
2516 tbl 01

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

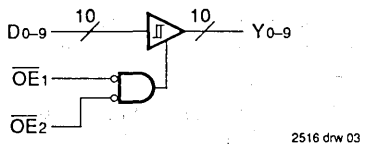


DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN DESCRIPTION

Name	I/O	Description
$\overline{OE}_1$ $\overline{OE}_2$	I	When both are LOW, the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

2516 tbl 02

FUNCTION TABLES

IDT54/74FBT2827A/B (Non-Inverting)(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

2516 tbl 03

IDT54/74FBT2828A/B (Inverting)(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

2516 tbl 04

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2516 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Condition	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2516 tbl 07

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 10%; Military: T_A = −55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Condition(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = 2.7V	—	—	10	µA
I_{IL}	Input LOW Current	Vcc = Max.	V_I = 0.5V	—	—	−10	µA
I_{OZH}	High Impedance	Vcc = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	−50	
I_I	Input HIGH Current	Vcc = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{ODH}	Output Drive Current	Vcc = Min., V_O = 2.25V		−35	—	—	mA
I_{ODL}	Output Drive Current	Vcc = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	Vcc = Max., V_O = GND(3)		−60	—	−225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min.	I_{OH} = −1mA	2.4	3.3	—	V
			I_{OH} = −12mA	2.0	3.2	—	V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA	—	0.1	0.5	V
			I_{OL} = 12mA	—	0.35	0.8	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	Vcc = Max. V_{IN} = GND or Vcc		—	0.2	1.5	mA

NOTES: 2516 tbl 05

1. For condition shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Condition[1]		Min.	Typ.	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_1$ = $\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		$\overline{OE}_1$ = $\overline{OE}_2$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
		$\overline{OE}_1$ = $\overline{OE}_2$ = GND Ten Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	6.5	17.8[5]	

NOTES: 2516 tbl 08

1. For condition shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Quiescent Current
   D_H = Duty Cycle for a TTL High Input (V_{IN} = 3.4V)
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in MHz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

		FBT2827A				FBT2827B			
		Commercial		Military		Commercial		Military	
Symbol	Parameter	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.
t_{PHL} t_{PLH}	Prop Delay, Di to Yi	—	7.0	—	7.5	—	5.0	—	6.5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yi	—	13.0	—	14	—	8.0	—	9.0
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Yi	—	13.0	—	14	—	7.0	—	8.0

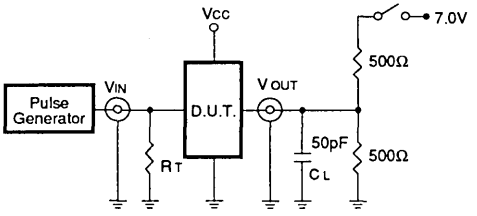
		FBT2828A				FBT2828B			
		Commercial		Military		Commercial		Military	
Symbol	Parameter	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.
t_{PHL} t_{PLH}	Prop Delay, Di to Yi	—	8.0	—	8.5	—	5.5	—	6.5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yi	—	12.0	—	13.0	—	8.0	—	9.0
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Yi	—	14.0	—	15.0	—	7.0	—	8.0

NOTES: 2516 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



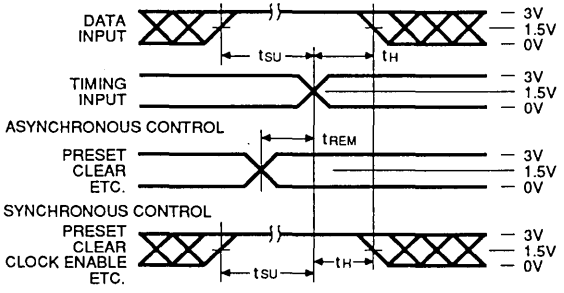
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

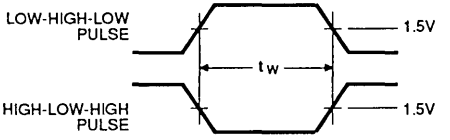
DEFINITIONS: 2516 tbl 10

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

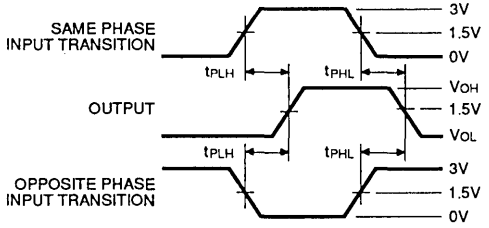
SET-UP, HOLD AND RELEASE TIMES



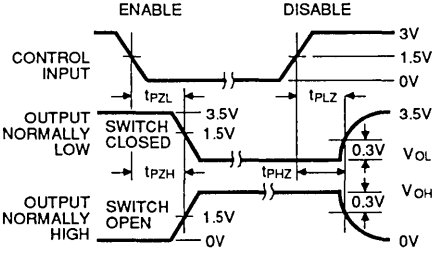
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES 2516 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; ZO ≤ 50Ω; tF ≤ 2.5ns; tR ≤ 2.5ns.

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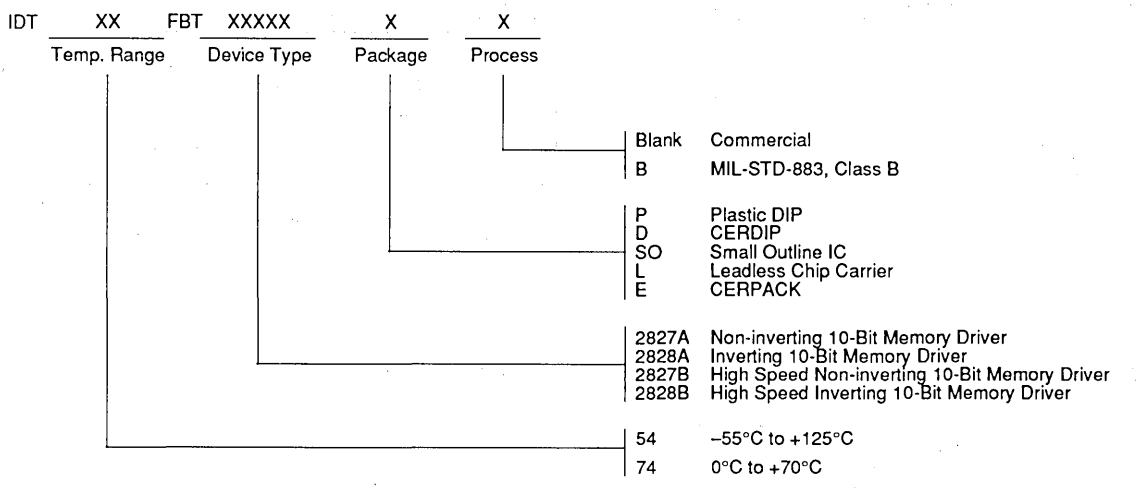
ORDERING INFORMATION



2516 drw 04

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS 10-BIT MEMORY LATCHES

ADVANCE INFORMATION
IDT54/74FBT2841A
IDT54/74FBT2841B
IDT54/74FBT2841C

FEATURES:

- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ± 10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

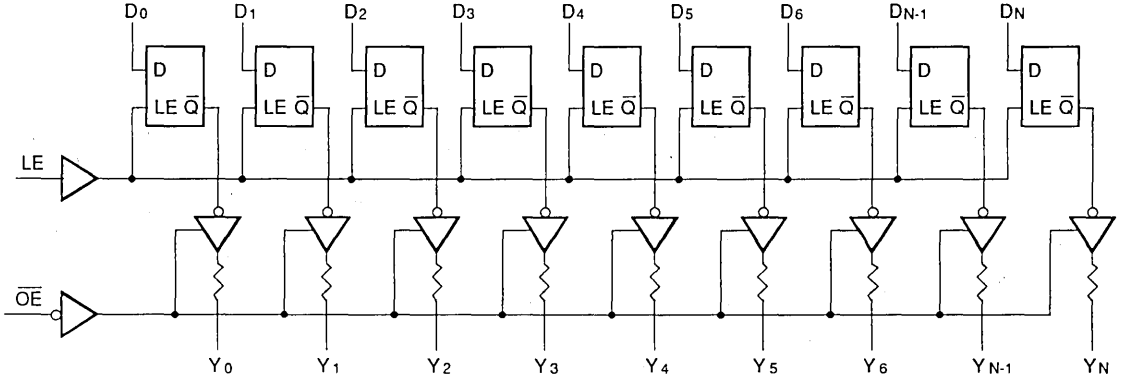
DESCRIPTION:

The FBT series of BiCMOS Memory Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2841 series are 3-state, 10-bit latches where each output is terminated with a 25Ω series resistor.

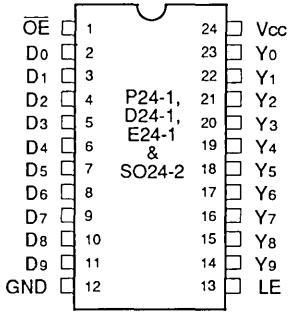
The FBT series of memory line drivers are ideal for use in designs needed to drive large capacitive loads with low static (DC) current loading. They are also designed for rail-to-rail output switching. This higher output level in the high state will result in a significant reduction in overall system power dissipation.

FUNCTIONAL BLOCK DIAGRAM

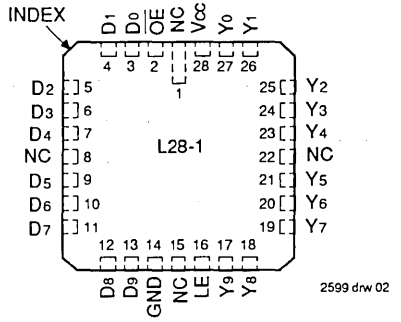


PIN CONFIGURATIONS

2599 drw 01



DIP/SOIC/CERPACK
TOP VIEW



2599 drw 02

LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Techology, Inc.

PIN DESCRIPTION

Name	I/O	Description
$D_0 - D_7$	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
$Y_0 - Y_7$	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is high, the outputs Y_I are in the high-impedance (off) state.

2599 tbl 05

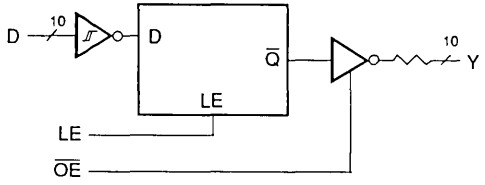
FUNCTION TABLE(1)

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

NOTE: 2599 tbl 06

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

LOGIC SYMBOL



2599 drw 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2599 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2599 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I =5.5V[4]		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.0V		-35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.0V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-60	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -1mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA	2.0	3.2	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 1mA	—	0.1	0.5	V
			I_{OL} = 12mA	—	0.35	0.8	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2599 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling LE = V_{CC} 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}$ = GND, LE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	7.8[5]	
		$\overline{OE}$ = GND, LE = V_{CC} Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	17.8[5]	

2599 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	54/74FBT2841A				54/74FBT2841B				54/74FBT2841C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Data (Di) to Output (Yi) (LE = HIGH)	CL = 50pF RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
tPLH tPHL		CL = 300pF[3] RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
tSU	Data to LE Set-up Time	CL = 50pF RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
tH	Data to LE Hold Time														
tPLH tPHL	Latch Enable (LE) to Yi	CL = 50pF RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
tPLH tPHL		CL = 300pF[3] RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
tW	LE Pulse Width HIGH/LOW	CL = 50pF RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to Yi	CL = 50pF RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
tPZH tPZL		CL = 300pF[3] RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Yi	CL = 5pF[3] RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns
tPHZ tPLZ		CL = 50pF RL = 500Ω	—	—	—	—	—	—	—	—	—	—	—	—	ns

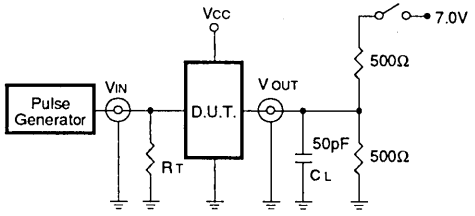
NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed, but not tested.

2599 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

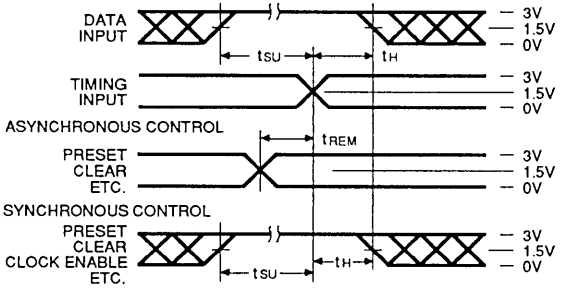
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2599 tbl 08

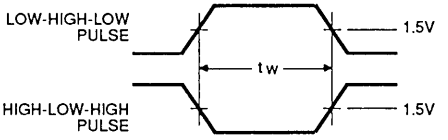
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

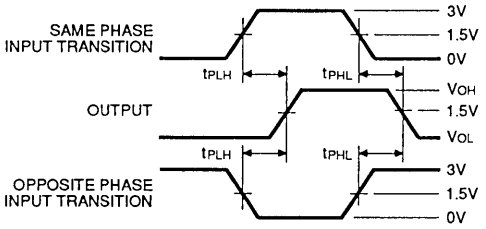
SET-UP, HOLD AND RELEASE TIMES



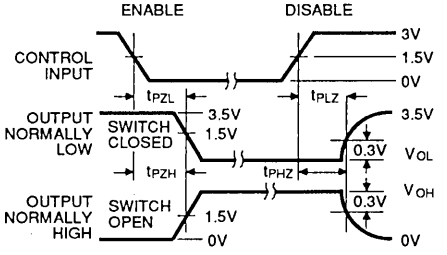
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

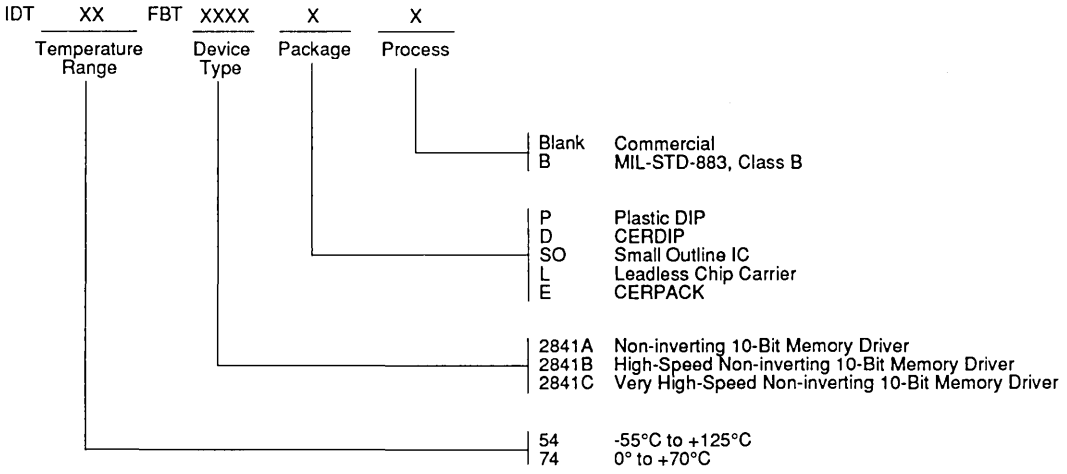


NOTES

2599 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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APPLICATION AND TECHNICAL NOTES

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Integrated Device Technology, Inc.

BUILD A 20 MIP DATA PROCESSING UNIT

TECHNICAL NOTE TN-02

by Michael J. Miller

INTRODUCTION

With the latest generation of CMOS devices from IDT, it is now possible for a user to design a data processing unit that will operate at 20 million instructions per second. The devices that make this possible are in the MICROSLICE™ family which provides such VLSI building blocks as sequencers and ALUs, a new generation of CMOS RAM devices which support 15ns access times, and a memory interface family called FCT which is 20-50% faster than the equivalent functions in Fairchild FAST™. Putting these devices together, the designer can construct a microprogrammed machine which has a system clock speed of 20 MHz. These microprogram designs can be used in a variety of application areas where high-speed processing and control sequences are required. Such application areas include dedicated graphics engines, digital signal processing, I/O controls for disk and tape, medical imaging, process control and special purpose computers.

BALANCED PATHS

For maximum performance and highest return on hardware investment, all critical paths should be as well-balanced as possible. Figure 1 shows a simplified block diagram of the basic structure of a microprogrammed machine. Microprogrammed machines are composed of static RAM, registers, latches and combinational logic. There are no dynamic elements involved. In the block diagram, there are three main elements: next state generator, current state register, and data processing element. The next state generator takes the current state information and generates the next state to be executed. The next state is stored into a current state register by the system clock on each clock cycle. Out of the current state register flow all control lines to the rest of the system. These control lines must control the next state generation as well as the data processing elements. The data processing elements might include such devices as fixed and floating point ALUs, register files and I/O devices. These data processing elements can generate status information which also may be fed back into the next state generator such that the next state is determined by a combination of current state and the current status.

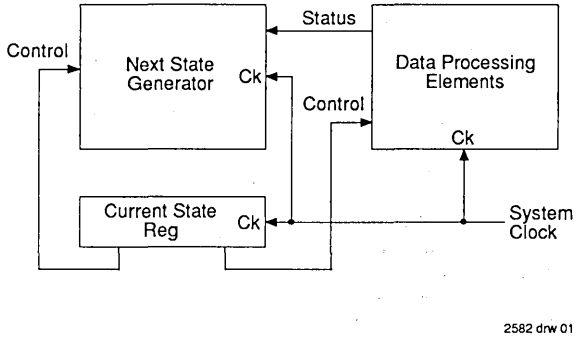

Figure 1. Simplified Block Diagram of a Microprogrammed Machine

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MICROSLICE is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

Most designs generally have two critical paths. One path incorporates the time delay from the current state register clocked by the system clock, through the next state generator, and a set up into the current state register. This is called the control path (Path B in Figure 2). The other path generally involved is from the system clock, through the current state output which controls the data processing elements which generate status which, in turn affects the next state selected. This is called the data path (Path A in Figure 2). In order to break up the data path delay, the status can be put in a register rather than directly into the next state generator. For the highest performance designs, a status register is used. Therefore, when optimizing a microprogrammed design, these two paths must be taken into consideration and balanced for maximum performance.

CONTROL PATH

The control path can be designed using the IDT49C410A as the heart of the next state generation mechanism. Figure 2 shows the block diagram of a data processing unit using IDT devices. The IDT49C410A is used to generate the next address which is put into a RAM referred to as a writable control store (WCS). Out of the WCS comes the next instruction to be executed. This is stored in a register built of IDT74FCT374A octal registers. This is the current state register and is often referred to as the pipeline register. The pipeline register can be viewed as containing several control fields — one control field for the IDT49C410A, another for the data processing elements, as well as additional fields for control of other elements in the system.

The field which controls the IDT49C410A contains instructions for the IDT49C410A, as well as bits to control a multiplexer which selects status bits from a current status register. The particular status bit which is selected out of the status register is used in combination with the instruction of the IDT49C410A to generate the next address. This latter path is the critical path. In the block diagram, the critical path in the control half is labeled as path B. All cycles start out with a system clock which generates a new instruction in 6.5ns[1] using the IDT74FCT374A. This current instruction then controls the status mux which can be constructed of a 74F151 using the Z bar output, which is the fastest output of the mux. The propagation delay is 9ns. The condition code input on the IDT49C410A will then be combined together with the instruction input and generate a new microprogram address in 16ns. This new address can then be used to access the next microprogram instruction in 15ns using the IDT6167A-15 static RAMs. At this point in the cycle, the microprogram instruction must be placed in the pipeline register with a 2.5ns set-up time. The total control loop then is 49ns, thus accommodating 20MHz operation in the control path.

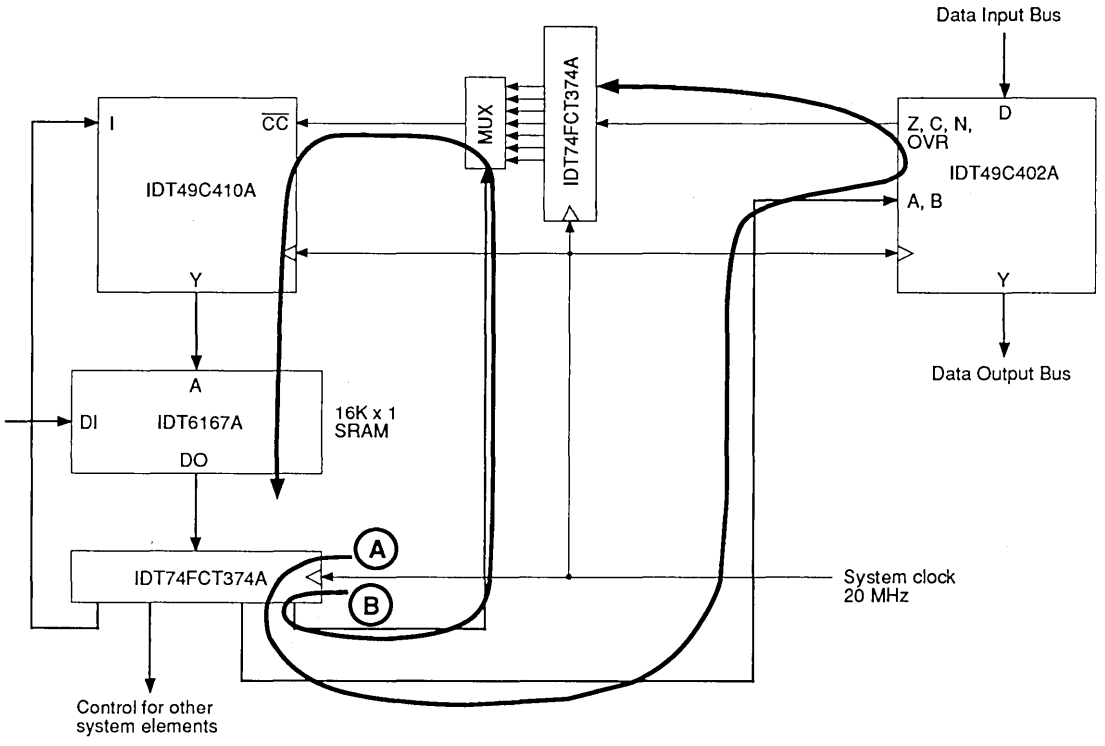
THE DATA PATH

The other critical path in the data processing unit is the data path which includes elements for processing data. The data may, for example, be data coming off a disk controller, graphics information or DSP data, just to name a few possibilities. Shown in the block diagram is an IDT49C402A which is a 16-bit cascadable binary ALU with 64 x 16 register file. The critical path starts with the system clock which generates a new instruction at the output of the pipeline register in 6.5ns. The field in the pipeline register is then fed into an IDT49C402A. This instruction controls the operation of the ALU unit, as well as providing addresses to select operands out of the internal 64 word register file. As a consequence of the data coming out of the register file into the ALU and the ALU instruction inputs, a result is generated. The ALU result can be brought out on the Y-bus or stored back into the register file. Status flags which correspond to Zero, Sign and Overflow are also output. The instruction and A/B addresses delay to status flags and Y output is 37ns. The status flags require a 2.5ns set-up time into the status register. Therefore, this path totals 45ns (labeled Path A) and matches the control path fairly well.

CONCLUSION

It can be seen that, by using the latest in CMOS devices from IDT, the designer is capable of creating a machine that can execute 20 million instructions per second. This type of performance is almost twice that achievable a year ago using the 2900 family and corresponding devices. With the previous devices, the typical control path required 100ns to execute and the data path typically took 80ns to execute. This was using the fastest available devices implemented in bipolar TTL interface-type technology. Not only are the CMOS devices from IDT extremely fast, they also consume a minimum of power — 75mA for the IDT49C410A and 125mA for the IDT49C402A. Each of the IDT74FCT374s typically consume 10mA. Therefore, it is not unreasonable to expect the designer to achieve a design which consumes about 1 watt for the ALU and sequencer shown in the simplified block diagram in Figure 2.

NOTE:
1. Times given are worst case maximum over commercial range.



Path (A)	
CP → Q	6.5 ns
ABI → Flags & Y	37.0 ns
Set-up	2.5 ns
Total	**45.0 ns**

Path (B)	
CP → Q	6.5 ns
MUX ('F151)	9.0 ns
CC → Y	16.0 ns
RAM	15.0 ns
Set-up	2.5 ns
Total	**45.0 ns**

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Figure 2. More Detailed Diagram of a DPU Capable of 20 MIPS Using IDT MICROSLICE Parts

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Integrated Device Technology, Inc.

USING THE IDT49C402A ALU

TECHNICAL NOTE TN–03

by Michael J. Miller

The MICROSLICE™ family consists of high-performance VLSI building blocks that provide such functions as ALUs, sequencers for building complex finite state machines, register files and support devices. The IDT49C402A is a member of this MICROSLICE family and is the first in a series of 16-bit ALUs from IDT. This high-speed ALU (shown in Figure 1) is capable of supporting 20MHz operations. This phenomenal speed is a result of CEMOS™, a single-poly double-metal structure using 1.2 micron gate lengths designed for high-performance and high-reliability.

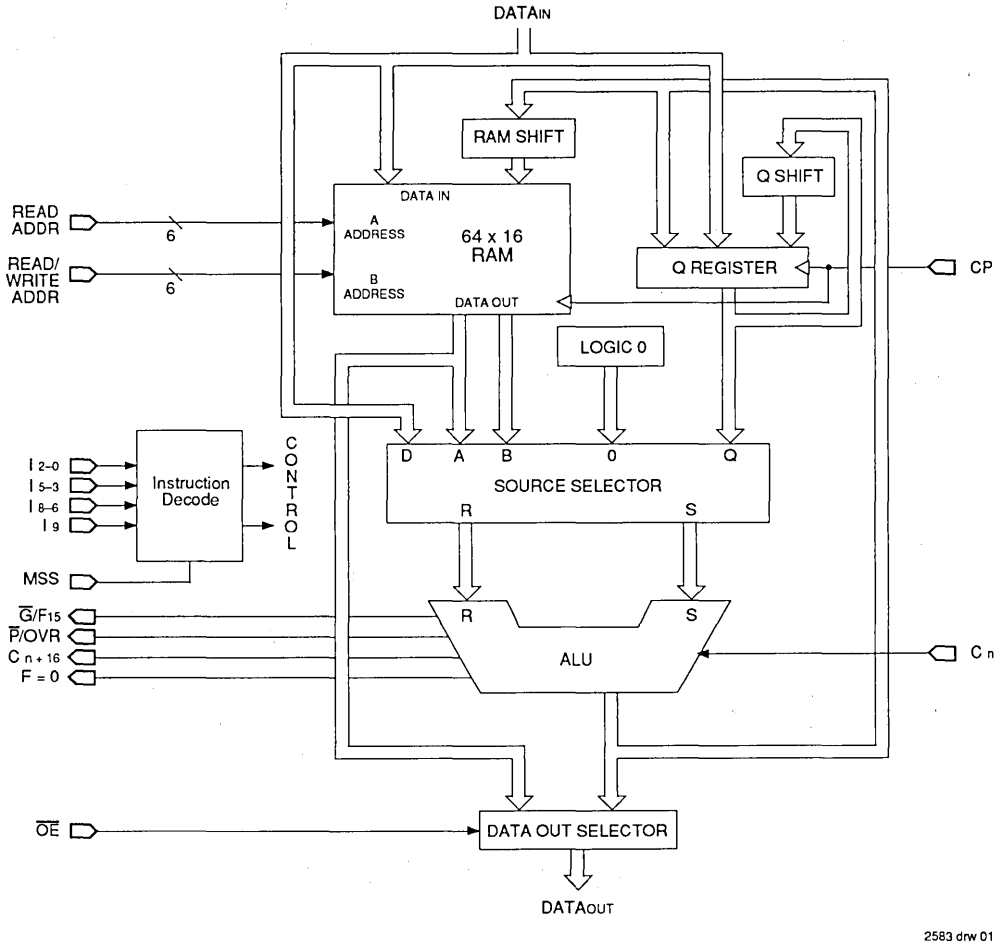

Figure 1. Block Diagram of the IDT49C402A

APPLICATIONS

The IDT49C402A can be thought of as a VLSI building block. This building block has a register file, an ALU and an accumulator. Since the IDT49C402A is designed out of static random logic, this device may be used in many different places. It can be used as a data path element in a general purpose computer or as an address generator to generate complex addresses for accessing data structures and linked lists. It might also be used as a complex accumulator with an ALU on its input to achieve sophisticated counter-type operations where constants may be in the register file in order CORDIC-type algorithms. Put simply, the IDT49C402A can be thought of and used as a very high-performance 16-bit version of the widely used 4-bit 7400 family (74181, 251, 381) ALUs.

FUNCTIONAL DESCRIPTION

The IDT49C402A is a high-speed, fully cascadable 16-bit CMOS ALU slice with 64-by-16-bit register file. It combines the standard functions of four 2901s (4-bit ALU) and a 2902 (carry lookahead) with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

Based on the normal control functions associated with a standard 2901 bit-slice operation, the IDT49C402A includes twice the destination codes. Its standard functions (Figures 2 and 3) include a 3-bit instruction field which controls the source operand select of the ALU (I_0, I_1, I_2), a 3-bit instruction field used to control the 8 possible functions of the ALU (I_3, I_4, I_5), and a 3-bit instruction field (I_6, I_7, I_8) for selecting the standard 8 destination control functions supported by the 2901. A tenth microinstruction input, I_9, offers 8 additional destination control functions. This I_9 input, in conjunction with I_6 through I_8, allows many new functions to take place – like shifting of the Q register up and down independently, as well as loading the RAM or Q registers directly from the D inputs without going through the ALU. By tying the I_9 instruction input high, the I_8 through I_6 instruction lines exhibit the destination codes found in the 2901. With the I_9 line low, the new additional functions of the IDT49C402A can be accessed.

EXTRA DATA PATHS

The IDT49C402A, while using the same basic 2901-type architecture, incorporates a new data path aimed at increasing system parallelism. This data path goes directly from the D inputs into the register file and Q register. Normally, the loading of the register file and the Q register in the 2901 requires that the ALU work as a pass function in order to route the direct data input path through the ALU and then store the results in the register file or Q register. With the new data path, the data can be put directly into the register file in parallel with other ALU operations. For example, in one cycle the DFF destination instruction allows the A output port of the register file and the Q register to be combined together in the ALU with the results being stored into the Q register, while new data is brought into the register file and stored at the address selected by the B address port. One of the more sophisticated destination functions available in the IDT49C402A is DFA. This allows the RAM to be loaded directly from the D inputs, the Q register to receive the results of the ALU and the Y output bus to output data directly from the RAM. This extra data path allows full, complete utilization of all three major buses inside the IDT49C402A.

FUNCTION CONTROL

Mnemonic	Microcode I_5	I_4	I_3	Octal Code	ALU Function
ADD	L	L	L	0	R Plus S
SUBR	L	L	H	1	S Minus R
SUBS	L	H	L	2	R Minus S
OR	L	H	H	3	R OR S
AND	H	L	L	4	R AND S
NOTRS	H	L	H	5	$\overline{R}$ AND S
EXOR	H	H	L	6	R EX-OR S
EXNOR	H	H	H	7	R EX-NOR S

2583 tbl 01

SOURCE CONTROL

Mnemonic	Microcode I_2	I_1	I_0	Octal Code	ALU Source Operands R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

2583 tbl 02

Figure 2. Function and Source Codes

ALU DESTINATION CONTROL

Mnemonic	Microcode I9	I8	I7	I6	Hex Code	Data to be Stored in RAM at B Address	Data to be Stored in Q Register	Y Output	
OREG	H	L	L	L	8	—	F	F	Original 2901
NOP	H	L	L	H	9	—	—	F	Functions
RAMA	H	L	H	L	A	F	—	A	
RAMF	H	L	H	H	B	F	—	F	
RAMQD	H	H	L	L	C	F/2	Q/2	F	
RAMD	H	H	L	H	D	F/2	—	F	
RAMQU	H	H	H	L	E	2F	2Q	F	
RAMU	H	H	H	H	F	2F	—	F	
DFF	L	L	L	L	0	D	F	F	New Added
DFA	L	L	L	H	1	D	F	A	IDT49C402
FDF	L	L	H	L	2	F	D	F	Functions
FDA	L	L	H	H	3	F	D	A	
XQDF	L	H	L	L	4	—	Q/2	F	
DXF	L	H	L	H	5	D	—	F	
XQUF	L	H	H	L	6	—	2Q	F	
XDF	L	H	H	H	7	—	D	F	

2583 tbl 03

Figure 3. Destination Codes

REGISTER FILE

The register file in the IDT49C402A is 64 addressable locations, each 16 bits wide. Being four times larger than most other 16-bit slices, this increased data space provides a larger cache of data which minimizes the traffic to bring in data from the outside world into the register file. From another perspective, the register file also can be viewed as 4 banks of 16 location register files. By using 2 of the address lines, a register file may be bank-selected, thus allowing the programmer to have 4 virtual 2901s operating inside the IDT49C402A. This enables the user to perform multi-tasking microcode. On each clock cycle a new task may be selected, thus having the minimal overhead for context switches.

INCREASED PERFORMANCE

The critical path through the IDT49C402A is the address and instruction lines to the Y output and status flags (ABI to Y/Flags). For the A version of the IDT49C402 this is 37ns, the time required for the address input lines to select operands out of the RAM register file and be output as data. This allows the user to construct a data path well under 50ns. This would include the pipeline register instruction time with a clock-to-Q of 6.5ns (utilizing the IDT74FCT374A) and a set-up time of data and status (37ns) from the IDT49C402A into a status register with a set-up time of 2.5ns.

32-BIT APPLICATIONS

High-speed operation for most 32-bit applications is easily obtainable when using the IDT49C402A. In order to build a 32-bit ALU, two IDT49C402As can be cascaded by connecting the carryout of the ALU of one device into the carry-in of the next device (see Figure 4). In this 32-bit design the critical path is through the ABI to carryout (C_{n+16}), which is 34ns, and then through the carryin (C_n) of the most significant device as a set-up to the clock, which is 32ns. Using IDT's new FCT/A logic family, a cycle time of 75ns can be constructed.

CONCLUSION

The IDT49C402A can be used in a multitude of applications which previously incorporated discrete 2901s. Upgrading to this high-performance device allows the user to operate at a 20MHz level while reducing board space and overall power. It exemplifies its overall flexibility as a VLSI building block wherever an ALU function with register files is used.

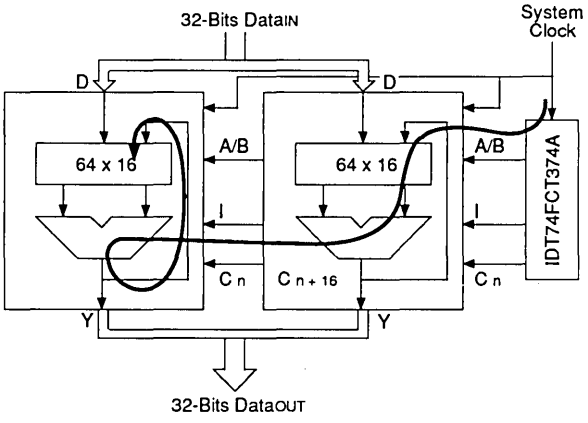

Figure 4. 32-Bit configuration showing critical delay path

Integrated Device Technology, Inc.

TRUST YOUR DATA WITH A HIGH-SPEED CMOS 16-, 32-, OR 64-BIT EDC

APPLICATION NOTE AN-03

By Suneel Rajpal and John R. Mick

INTRODUCTION

As a computer-science corollary to Parkinson's First Law, "Work expands to fill the time available," it is observably always true that "Computer software expands to fill the memory available." There is an insatiable demand for higher speed and denser memory, be it dynamic RAM or static RAM. However, there are reliability considerations that have to be made in large memory systems that must always provide correct data. This article deals with methods of enhancing data integrity and system performance by using Error Detection and Correction (EDC) logic circuits.

TYPES AND SOURCE OF ERROR

In memory systems, two types of errors can occur — hard errors or soft errors. A hard error is a permanent error and it occurs when a memory location is stuck-at-one or stuck-at-zero. A soft error is temporary, random and correctable. As these errors are non-recurring and non-destructive they can be corrected using EDC logic.

Hard errors are caused by factors such as interconnect failures, internal shorts and open leads. Soft errors can be caused by system noise, power surges, pattern sensitivity and alpha particle radiation. The charge of an alpha particle can become comparable to the charge on memory cells as geometries shrink. This implies that susceptibility to alpha particle radiation is likely to increase as memory densities increase; however, memory manufacturers try to reduce or eliminate the problem by design or packaging techniques.

In spite of that there is a probability of failure or error, especially where large systems are concerned. A graph that shows the trend of error rate versus chip density for dynamic RAMs is presented in Figure 1. One can calculate the Mean Time Between Failures (MTBF) for a DRAM system quite easily based on such data from a DRAM manufacturer.

A common method to examine data integrity is to incorporate parity. In a simple case of a three bit number and one parity bit, the following relationship exists as shown in Table 1.

TABLE 1.

DATA	ODD PARITY
000	1
001	0
010	0
011	1
100	0
101	1
110	1
111	0

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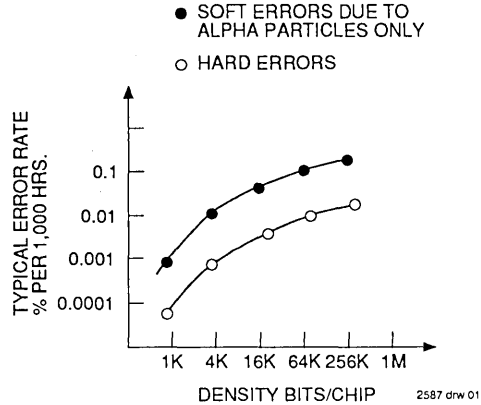

Figure 1. Typical Error Rates

The odd parity is generated by an exclusive-NOR operation of the data bits. An error can be identified by taking the entire word and the parity bit, called a code, and performing an exclusive-OR operation. If the exclusive-OR result was a one, it indicates that the data was probably correct and the combination of the data and parity bits represent a valid code; "probably" is mentioned, and will be explained in the following lines. However, if the exclusive-OR result was a zero, then it can only be identified that an error occurred and the combination of the data and parity bits represent an invalid code.

Another interesting aspect of Table 1 is the fact that to go from one valid code, say 0001 to another valid code 0100, at least two bits have to change. This is called a distance of two. If only one bit changed on the code, it could be used to identify an error, but it could not point to the correct valid code. For example, if an invalid code of 0011 is seen, it lies between 0001 and 0010 and it is not possible to tell if the last data bit is in error or the parity bit is in error. Now, back to the mention of the word "probably." If two bits in the data changed erroneously, the parity tree performing the exclusive-OR would not be able to catch that kind of an error. Detection codes using parity are therefore limited and useful only in detecting one bit in error (or any number of odd errors), and they cannot provide any correction. Unfortunately, they cannot detect two errors (or any even number of errors).

The detection capability of the codes with different distances are shown in Figure 2. An invalid code that occurs in the distance of two cannot tell which bit was erring as outlined in the previous paragraph. Codes that keep a distance of three (or at least 3 bits have to change to go from

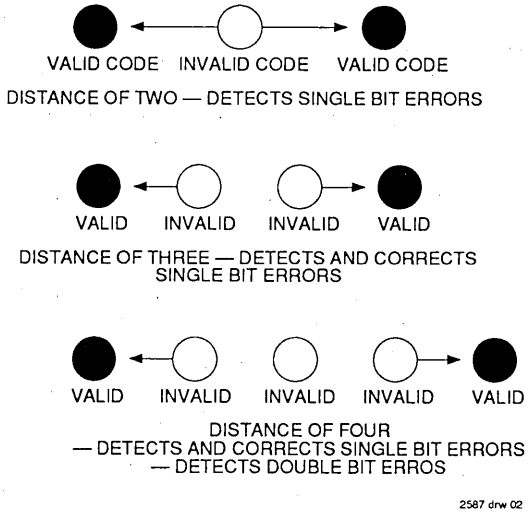

Figure 2. Codes of Various Distances and Their Effectiveness

one valid code to another) can detect single bit errors and also correct them. However, codes with a distance of three cannot detect two failing bits. As shown in the distance of three example, if a two-bit error occurs, it would be identified as if one bit failed. An invalid code associates detection/correction with the valid code adjacent to it rather than the other valid code that is a distance of two from it. Codes of a distance of four can detect all single-bit errors, detect all double-bit errors and also correct all single-bit errors. Double-bit errors are equidistant from two valid codes as shown by the central invalid code in Figure 2. The Single Error Correction and Double Error Detection (SECDED) capability is highly desirable for data integrity in high-reliability computer systems.

EDC ICs TO THE RESCUE

Codes with a distance of four are used in the IDT39C60/IDT49C460 Error Detection and Correction ICs. The overhead in the EDC implementation is additional check bits to the words in memory. For example, 6 bits are needed for 16-bit data, 7 bits for 32-bit data, and 8 bits for 64-bit data to generate a distance of four. The code formed is a catenation of the word bits and the check bits and, as in the parity case, the code can be valid or invalid. The valid codes are a distance of four apart from the next valid code. Valid codes are implemented by generating check bits based on the data word and writing the check bits with the data bits to the memory. On reading the data and check bits from memory, a possibly valid or invalid code could have been read. The determination of whether the code was valid or not is done by regenerating check bits using the data bits; these are compared (ex-ORed) to the check bits that were read and the result is syndrome bits. These syndrome bits are indicative of an error-free situation, or a single or double-bit error, and are used to determine validity of a code, and also to point to single-bit errors and identify the occurrence of two or more bits in error.

As an example, let us write (FFFF)H as the data word. The corresponding check bits that will be written in the memory are 001100 and can be computed using Table 2 which is based on a modified Hamming code. On reading back, if the data was FFFE and the data in position 15 had erroneously flipped from a "1" to a "0," the regenerated check bits would be 000111 (based on FFFE). The syndrome bits are the ex-OR of the two sets of check bits and are 001011. Referring to Table 3, a syndrome of 001011 indicates bit 15 is in error and has to be flipped.

The internal hardware of the IDT39C60 16-bit EDC, shown in Figure 3A, consists of ex-OR trees that can generate check bits and syndromes and also contains hardware to correct data. In addition, two or four IDT39C60s and some SSI, MSI can be connected to form 32-bit or 64-bit EDC systems. The IDT39C60 is a functional and pin-compatible replacement of the 16-bit 2960, and runs at a quarter of the power. Faster versions, such as IDT39C60-1 and the IDT39C60A (the IDT39C60-1 replaces the Am2960-1 and the IDT39C60A is the fastest 16-bit EDC available), demonstrates that CMOS circuits can not only run cooler than their equivalent bipolar circuits, but also run faster with higher output drive.

The architecture of a 32-bit EDC, the IDT49C460, is shown in Figure 3B. The IDT49C460 provides efficient means of generating check bits, calculating syndrome bits and

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TABLE 2: 16-BIT MODIFIED HAMMING CODE CHECK BIT GENERATION(1)

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

NOTE:
The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

2587 tbl 02

TABLE 3: SYNDROME DECODE TO ERROR LOCATION/ TYPE

SYNDROME BITS			S8	0	1	0	1	0	1	0	1
			S4	0	0	1	1	0	0	1	1
			S2	0	0	0	0	1	1	1	1
SX	S0	S1									
0	0	0		*	C8	C4	T	C2	T	T	M
0	0	1		C1	T	T	15	T	13	7	T
0	1	0		C0	T	T	M	T	12	6	T
0	1	1		T	10	4	T	0	T	T	M
1	0	0		CX	T	T	14	T	11	5	T
1	0	1		T	9	3	T	M	T	T	M
1	1	0		T	8	2	T	1	T	T	M
1	1	1		M	T	T	M	T	M	M	T

NOTES:
* = No errors detected
Number = Number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

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correcting data bits on a 32-bit data path. In addition, diagnostic capability is provided to verify data operations in the memory system and verify that the EDC IC is functional too.

Figures 4A and 4B show the dataflow for the generate and error detect/correct operations in the IDT49C460. In Figure 4A, check bits based on input data are generated by the EDC and are written to the check-bit memory along with the data. In Figure 4B, the data and check bits are read from the memory. Based on their values the syndrome bits are generated inside the IDT49C460. If the EDC is in the correct mode, any single-bit error is corrected and the corrected data is placed in the output data latch. The syndrome bits are also available if error logging is done.

Another necessary operation that is required is byte handling. When the memory is organized as a 32-bit word and an 8-bit update is being performed, it requires a 2-step operation. The first step is to read the 32-bit data and check bits, and correct any erroneous single bit failure. The second step is to write the new byte with the unmodified bytes back to the system memory. The check bits corresponding to the newly formed 32-bit word are generated and also written to the memory. This operation is supported by having four separate output byte enables in the IDT49C460. The two-step process is shown in Figures 5A and 5B.

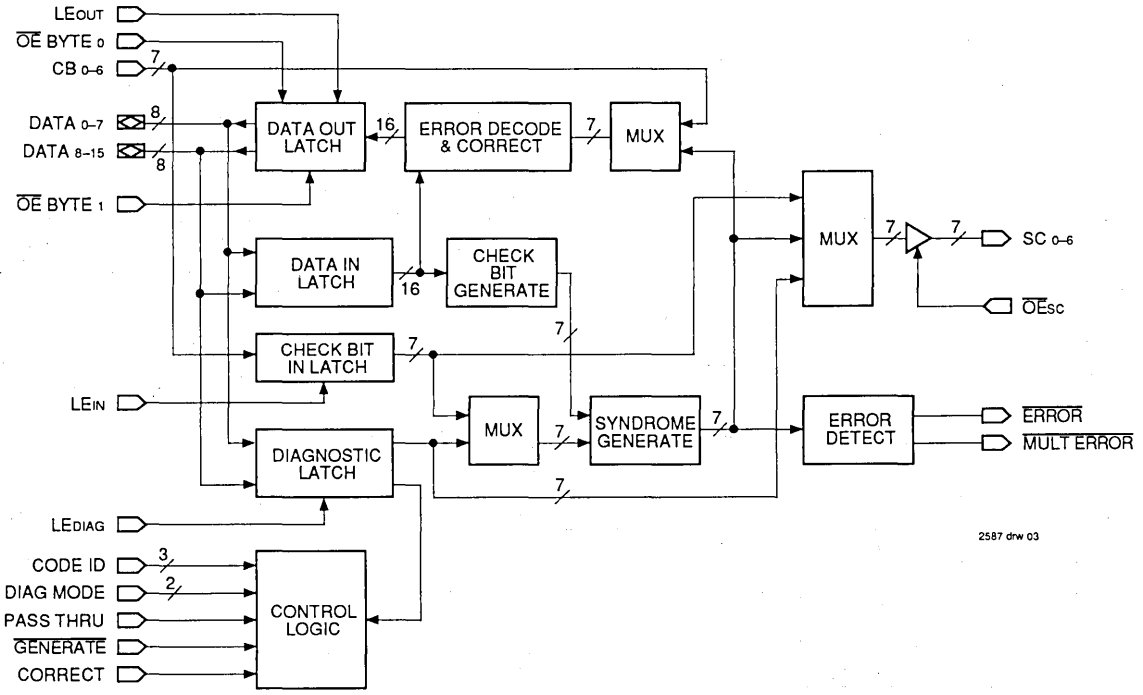

Figure 3A. The IDT39C60/-1/A 16-Bit EDC Architecture

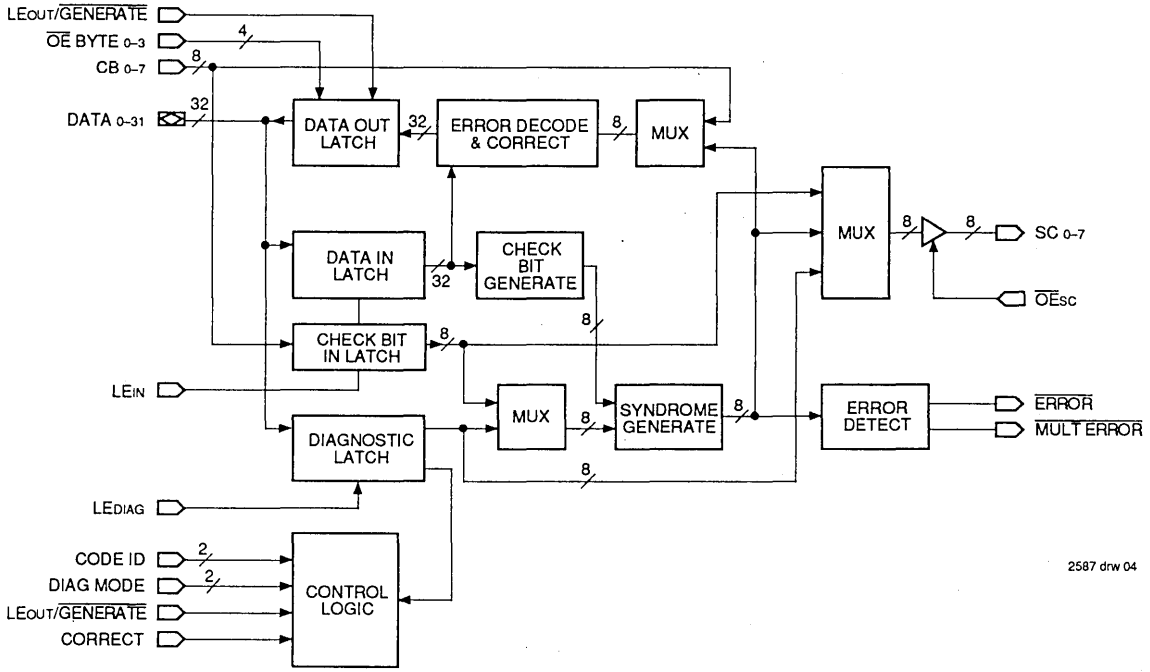

Figure 3B. The IDT49C60/A 32-Bit EDC Architecture

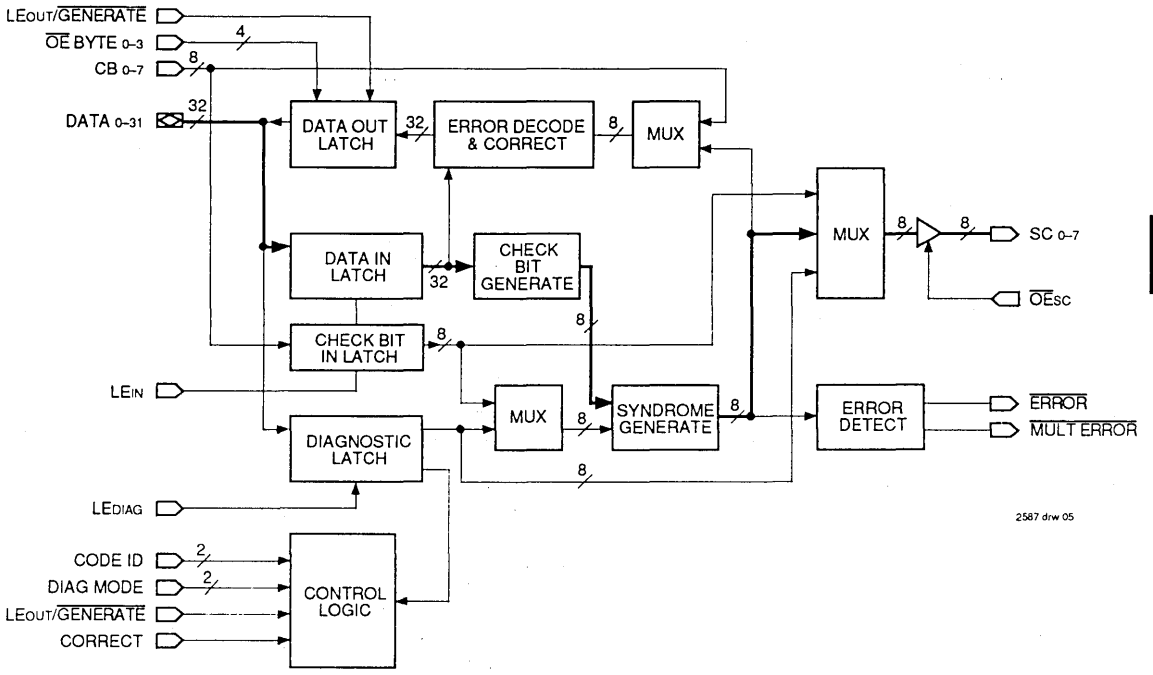

Figure 4A. Check Bit Generation in the IDT49C460

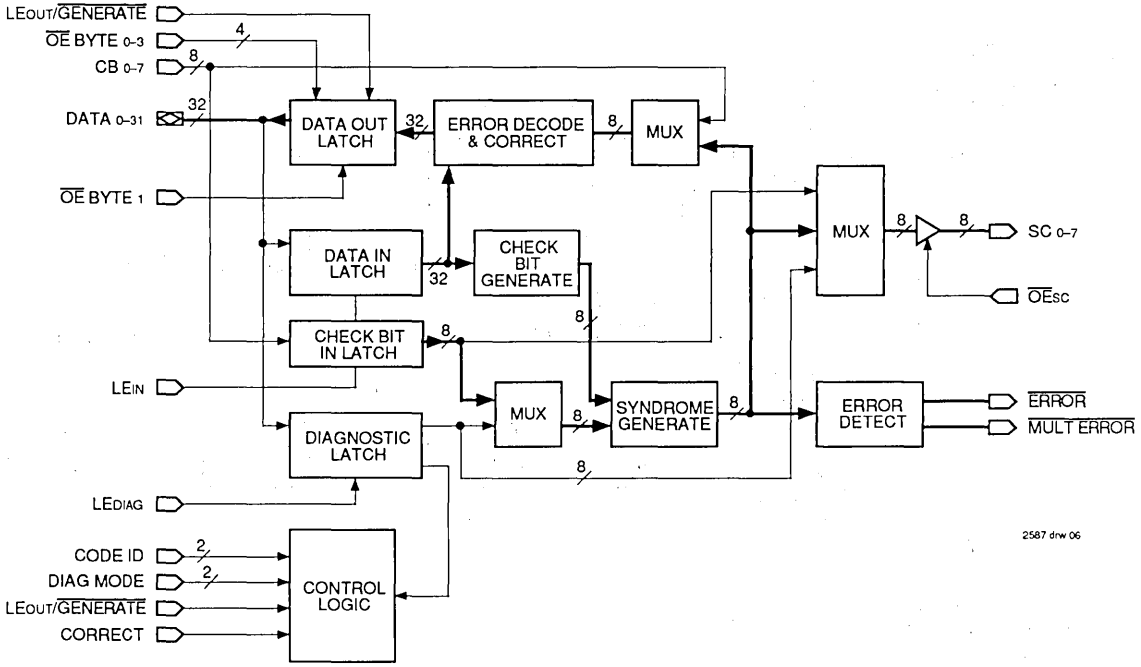

Figure 4B. Error Detection and Correction in the IDT49C460

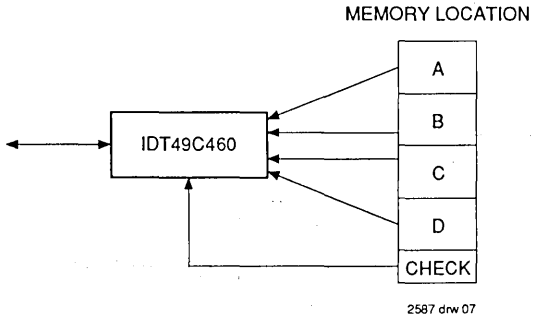

Figure 5A. Byte-Write Operation; Step 1. Read 32-Bit Word and Correct Any Single-Bit Error

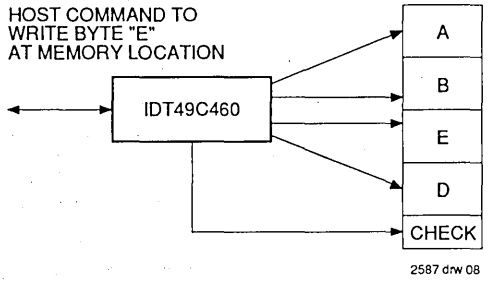

Figure 5B. Byte-Write Operation; Step 2. Newly Generated Check Bits Corresponding to Bytes A, B, E, and D Are Written to Memory Along With Bytes A, B, E, and D

The IDT49C460 is expandable to 64-bit wordlengths as shown in Figure 6A. The external buffer may not be required if the path from the memory already has a three-state buffer in its output stage or externally in the data path to the EDC. Figure 6B shows a 2-step operation when an error detection and correction occurs in bit 32-63 of the 64-bit word. The IC on the first level, with code ID=10, receives the data bits 0-31 and the entire check bits. In the example shown, bit 63 has erroneously flipped from a "1" to a "0". The partial syndrome bits are passed from the first device to the second. (The actual syndrome bits are generated from a table not shown in this article but are in the IDT49C460 data sheet.) The check input latch of the second device is open, due to its code ID=11, and the partial syndrome bits are combined with the data bits to generate the final syndrome bits. The final syndrome bits indicate that bit 63 is in error and it is inverted to produce a correct result. The final syndrome bits are also sent back to the first device, but the resulting syndrome does not alter any data bits in the first device. Therefore, the error correction is a 2-step process. In Figure 6C, an error occurs in bits 0-31. In this case, the partial syndrome is sent to the second device. The second device generates the final syndrome and sends it back to the first device. Finally the erroneous bit is flipped over. In this case, a 3-step operation takes place.

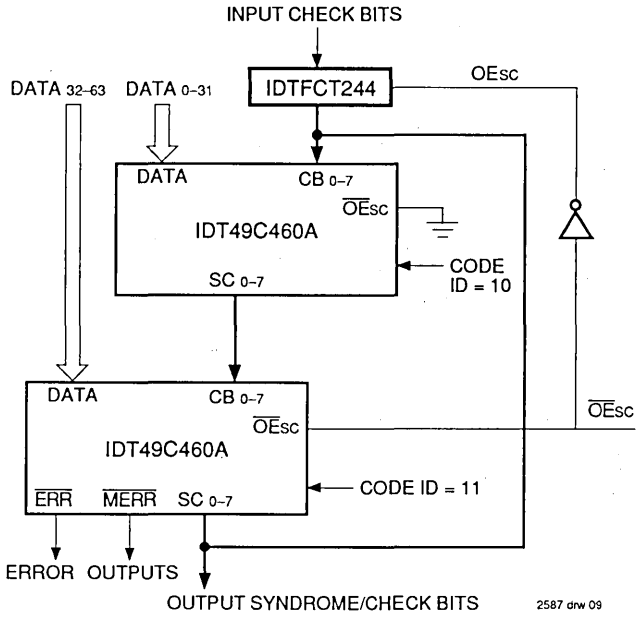

Figure 6A. The IDT49C460 in a 64-Bit Configuration

DATA	CHECK		
FFFFFFFFFFFFFFFF	30	WRITE	
FFFFFFFFFFFFFFFE	30	READ	
CODE = 10 FFFFFFFF (BITS 0–31)	30 (INPUT CHECK BITS)		STEP 1
	00 (PARTIAL SYNDROME)		
CODE = 11 FFFFFFFE (BITS 32–63)	00 (PARTIAL SYNDROME)		STEP 2
FFFFFFFF (CORRECTED 32–63)	AE (FINAL SYNDROME)		
CODE = 10 FFFFFFFF (UNCHANGED 0–31)			

2587 drw 10

Figure 6B. Error Correction on a 64-Bit Word, When Error is in Bits 32-63

DATA	CHECK/SYNDROME		
FFFFFFFFFFFFFFFF	30 (CHECK)	WRITE	
FFFFFFFEFFFFFFFF	30 (CHECK)	READ	
CODE = 10 FFFFFFFE (BITS 0–31)	30 (INPUT CHECK BITS)		STEP 1
	2F (PARTIAL SYNDROME)		
CODE = 11 FFFFFFFF (BITS 32–63)	2F (PARTIAL SYNDROME)		STEP 2
FFFFFFFF (BITS 32–63)	2F (FINAL SYNDROME)		
CODE = 10 FFFFFFFF (CORRECTED 0–31)	2F (FINAL SYNDROME)	—	STEP 2

2587 drw 11

Figure 6C. Error Correction on a 64-Bit Word, with Error in Bits 0-31

HOW THE IDT49C460 FITS IN A SYSTEM

By virtue of their function, EDC ICs tie in closely with system memory architectures. Figure 7 shows a host that generates addresses and accesses a memory system. The memory contains memory elements, error detection logic and interface circuits. These are needed to start a memory cycle, to send/receive data on the system bus, and to inform the host that it has completed the memory operation.

One may use EDC for dynamic RAM memories or static RAM memories. Figures 8A and 8B show general configurations for DRAM arrays. Normally, in DRAM systems, separate pins exist for the DATAOUT and DATAIN. Therefore, IDTFCT244s can be used to provide an isolation between the DATA port of the EDC and the DATAOUT from the RAM. This isolation may be required after a read operation, and the EDC provides corrected data to the system and the DRAM. Another buffer is needed between the DATA port of the EDC and the system data bus to allow the corrected data to be placed on the system bus. The DRAM controller can be implemented using standard off-the-shelf products. An important operation that has to be supported is byte or word handling. The IDT49C460 EDC configuration shown in Figure 8A has four individual byte enable controls going to the IDTFCT244s and their complements to the IDT49C460. The IDT39C60 shown in Figure 8B has two individual byte controls to the IDTFCT244s and their complements going to the IDT39C60.

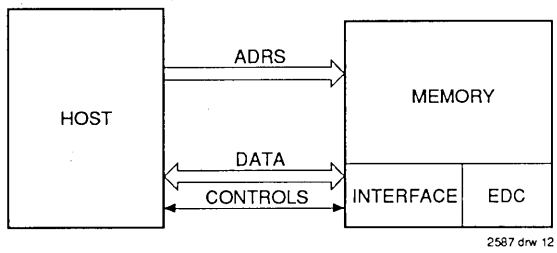

Figure 7. Typical High-Reliability Memory System

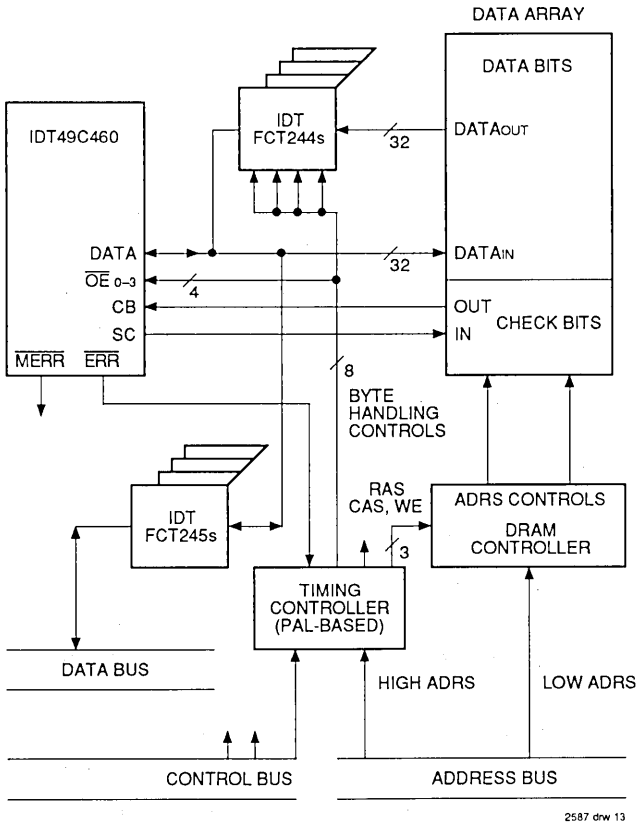

Figure 8A EDC Logic in 32-Bit DRAM-Based Memory Systems

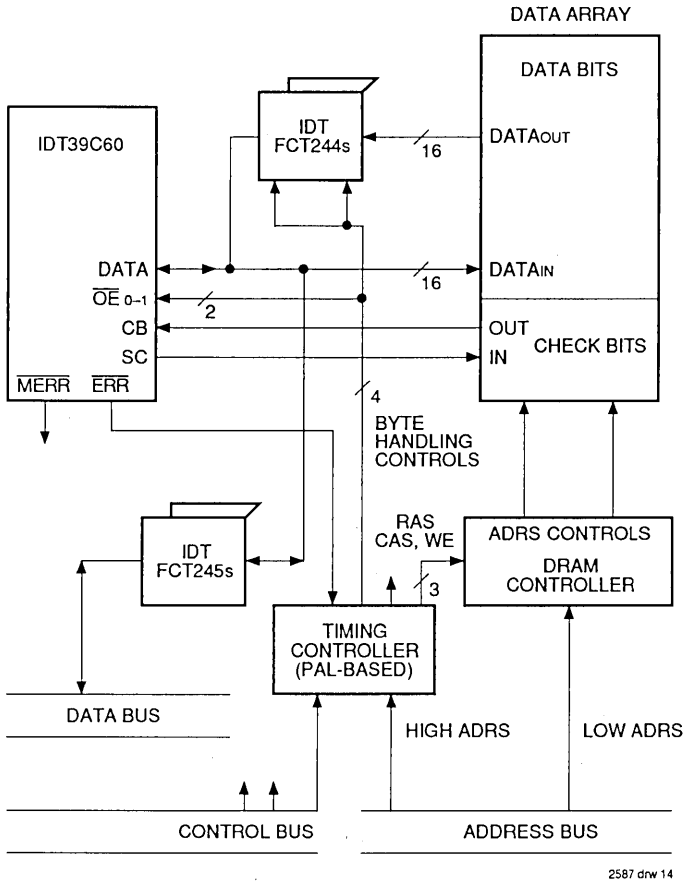

Figure 8B. EDC Logic in 16-Bit DRAM-Based Memory Systems

In static RAM systems, as shown in Figure 9, there is no need for dynamic memory array controller; however, bidirectional buffers are required on the ports of the static RAMs as RAMs have common I/O lines for data. If the SRAMs had separate I/O pins for the data, the buffer configuration of the DRAM array could be used.

The timing controller, common to both DRAM and SRAM systems, controls the buffer and the EDC ICs. This is an interesting task to the memory system designer, as a choice of EDC architectures are available.

BUS-WATCH AND FLOW-THROUGH EDC ARCHITECTURES

The architecture of the EDC ICs can be categorized as Bus-Watch and Flow-Through as shown in Figure 10. In a bus-watch architecture, there is only one bus to handle the data and one set of pins that handle incoming data from the memory, corrected data from the EDC, and incoming data from the system to be written to the memory. The IDT39C60 and IDT49C460 are based on a bus-watch architecture. In a flow-through architecture, such as Intel's 8206, there are two ports that handle data movement. The WDIN/DOUT handle incoming data from the system, so that the EDC can generate check bits. The second function of the WDIN/DOUT is to supply the corrected data to the system and the memory. The second set of pins, DIN, only handles incoming data from the RAM. These architectures lend themselves to "Check Only" and "Correct Always" configurations.

The "Check Only" method is used in high-performance systems. The memory system always sends data directly to the host when a read is requested. In the event a single bit error occurs, one approach is that the read cycle is delayed and a correction is performed. The corrected data is sent to the host and written into the memory. In this case, the timing control circuit would disable the Memory Data Out Buffer (the IDTFCT244 for the DRAM case and the IDTFCT245 for the

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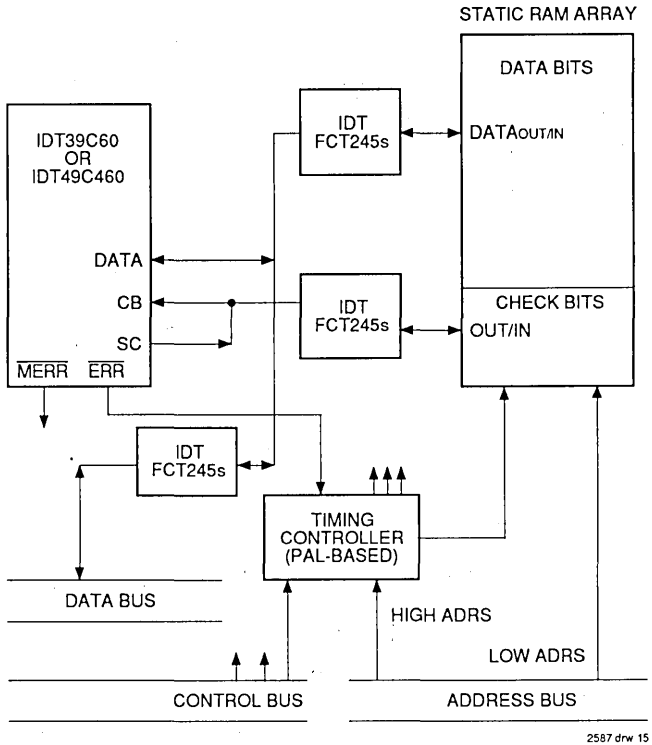

Figure 9. EDC Logic in 16-, 32-, 64bBit Static RAM-Based Systems

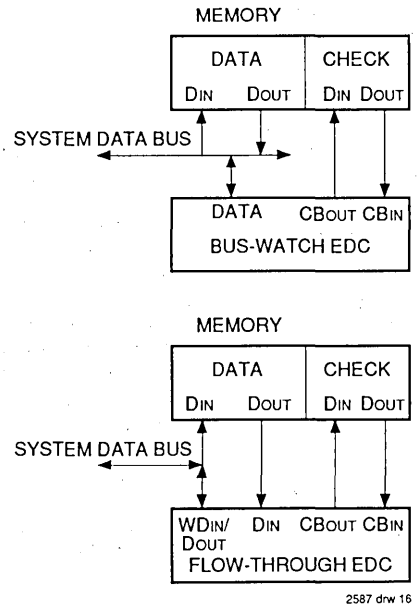

Figure 10. Architecture of Bus Watch and Flow-Through EDC Logic

static RAM case) and put corrected data from the EDC IC onto the system data bus, also writing the corrected data back into the memory array. For the "Check Only" method, the DATA TO $\overline{ERR}$ parameter is of key concern to designers as this can be used to generate the DTACK, READY or BERR signals to the host.

The other option is that a "Correct Always" method is used. In this case, the EDC always corrects data (regardless of the fact that it may be error-free), sends it on the system data bus and writes it back to the memory. In this case, the cycle time for the data read includes the "DATAIN TO CORRECTED DATAOUT" parameter for the EDC. The IDT49C460 and the IDT39C60 provide the fastest timings for the "DATAIN TO $\overline{ERR}$" and "DATAIN TO CORRECTED DATAOUT" parameters when compared to other currently available 32-bit and 16-bit EDCs. This was made possible by using IDT's CEMOS™ II 1.2μ process.

The IDT49C460A dissipates only 95mA and the IDT39C60A dissipates only 85mA over the commercial temperature range. The quiescent power consumption is only 5mA for the IDT49C460A and the IDT39C60A.

The delay for the DATAIN TO $\overline{ERR}$ is only 30ns for the stand-alone 32-bit IDT49C460A (worst case commercial) and is 46ns for the 64-bit for the cascaded case. The delay for the DATAIN TO CORRECTED DATAOUT is only 36ns for the stand-alone case and 63ns for the 64-bit cascaded case. These parameters are very important when considering EDC ICs discussed further in a later section. They are, however, shown in Tables 4 and 5 for the 16-bit IDT39C60 and 32-bit IDT49C460, respectively.

TABLE 4: KEY PARAMETERS FOR THE IDT39C60/-1/A FOR COMMERCIAL RANGE

CONDITIONS	IDT39C60	IDT39C60-1	IDT39C60A
DATAIN to $\overline{ERR}$	32ns	25ns	20ns
DATAIN to Corrected DATAOUT	65ns	52ns	30ns

2587 tbl 04

TABLE 5: KEY PARAMETERS FOR THE IDT49C460/A FOR COMMERCIAL RANGE

CONDITIONS	IDT49C460	IDT49C460A	2 IDT49C460As FOR 64-BIT EDC
DATAIN to $\overline{ERR}$	40ns	30ns	46ns
DATAIN to Corrected DATAOUT	49ns	36ns	63ns

2587 tbl 05

The acid test is how a flow-through architecture compares in performance to a bus-watch architecture in the "Check Only" mode and the "Correct Always" mode. In Figure 11, a flow-through EDC device is connected to a DRAM array system for the IDTFCT244 buffer to the system bus directly and simultaneously to the EDC device. Within the DATAIN TO $\overline{ERR}$ of the device, it is determined if a single-bit error occurred and, if so, a timing controller would disable the IDTFCT244 and allow corrected data to be sent on the system bus via the IDTFCT245.

A bus-watch EDC in a "Check Only" configuration is shown in Figure 12. The data path from the DRAM to the EDC goes through one IDTFCT244 delay and is identical to the flow-through case. After that the DATAIN TO $\overline{ERR}$ delay determines whether or not the cycle would be stretched. The data from the DRAM goes through an IDTFCT244 buffer and an IDTFCT245 buffer in the bus-watch case. One emerging fact is that the time it takes to make a decision to stretch a memory cycle is the same for the bus-watch and flow-through EDC parts and is determined by the DATAIN TO $\overline{ERR}$ of the respective devices.

In the flow-through "Correct Always" configuration, as shown in Figure 13, data has to always pass through the EDC and any IDTFCT245 and on to the system bus. In the case of bus-watch ICs, data from the DRAM goes through an IDTFCT244, in and out the EDC device and through an IDTFCT245 as shown in Figure 12. A bus switch has to take place every cycle as memory data comes into the EDC, is corrected and then transferred to the system bus. In a practical design this bus switch may be the longest delay path for "Correct Always". However, if just the specification is being reviewed, the flow-through path is shorter by an IDTFCT244 delay. A specification comparison is that the "DATAIN TO CORRECTED DATAOUT" delay of a flow-through EDC part should be compared to the "DATAIN TO CORRECTED DATAOUT" delay of the IDT49C460/A, plus an external 7ns buffer delay (for the IDTFCT244). However, in an actual system, such as the one in Figure 8A, a "bus-switch" has to take place, as explained below.

In a DRAM system that has a bus-watch EDC, a sequence of events has to be created by the timing controller that was shown in Figure 8A. The timings that the controller generates are shown in Figure 14. The example being considered is "Correct Always." The RAS, CAS, WE signals have to be generated to read data from the DRAM. The read takes place before state 7, and the read data is latched in the DATAIN latch of the EDC. It is then corrected and the corrected data can be latched in the DATAOUT latch. The data correction can take place between states 7 and 10. Any time after state 10, the EDC can place the corrected data on the bus. The bus that was loading the data in the EDC has to be turned around as the EDC is going to send corrected data

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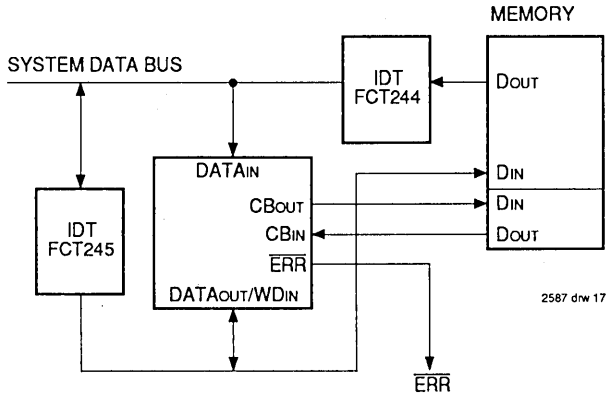


Figure 11. The "Check Only" Configuration for Flow-Through EDC ICs

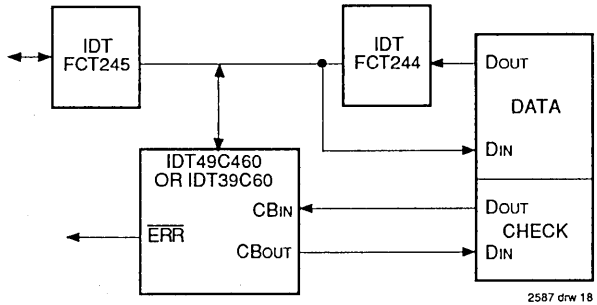


Figure 12. The Bus-Watch EDC in "Check Only" or "Correct Always" Configurations

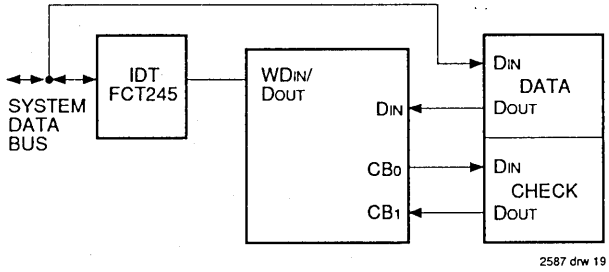
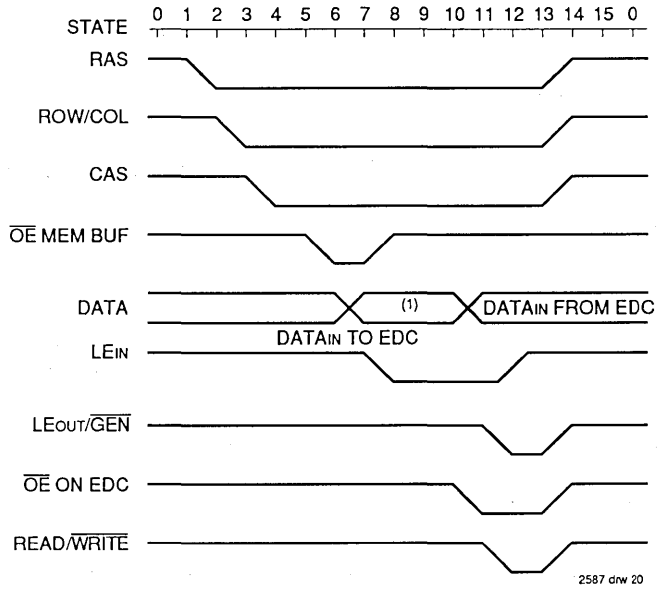


Figure 13. A Flow-Through EDC in "Correct Always" Mode



NOTE:
1. A BUS-SWITCH TAKES PLACE BETWEEN STATES 6 AND 10.

Figure 14. Timing Diagram for Correct Always in Figure 7A

to the host. The EDC also writes back the corrected data and the newly generated check bits to the memory. The memory buffers shown in Figure 8A are three-stated, as the $\overline{OE}$ MEM BUFF are high from state 7 onwards and the EDC would be enabling data on the bus. The timing diagram in Figure 14 explains a typical case and users will have to customize it based on their memory speeds and the time the system has for receiving valid data.

Other factors that may be a consideration are package count and board space. The number of packages used in flow-through and bus-watch implementations are the same for "Check Only" configurations. In "Correct Always" configurations the bus-watch implementation requires four more IDTFCT244s than the flow-through implementation. Flow-through ICs have more pins and therefore leave a larger footprint on the PC. However, in terms of board space, since the footprint of the flow-through EDC is larger than the bus-watch, the bus-watch approach takes less space for "Check Only" configurations and there is a tie for the "Correct Always" configuration.

SUMMARY

This article has covered reliability issues in memory systems and solutions using EDC devices. In considering EDC devices, two parameters are critical: the "DATAIN TO $\overline{ERR}$" and the "DATAIN TO CORRECTED DATAOUT". At Integrated Device Technology, we have optimized these two parameters and produce ultra fast, TTL-compatible CMOS Error Detection and Correction devices for high performance 16-, 32- and 64-bit systems.

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Integrated Device Technology, Inc.

16-BIT CMOS SLICES—NEW BUILDING BLOCKS MAINTAIN MICROCODE COMPATIBILTY YET INCREASE PERFORMANCE

APPLICATION NOTE AN-06

by Michael J. Miller

INTRODUCTION

The electronics industry has been an evolutionary succession of dominating technologies. This has been true for semiconductor devices in general, as well as the product family called bit-slice microprocessors. With the extinction of each technology and the emergence of the new, there is an associated transition for both the manufacturer and the consumer. Each company seeks to minimize the effort of this transition.

In the 1950s it was a generation of germanium diodes and transistors. During the 1960s, silicon transistors and bipolar ICs dominated. The last decade saw the emergence of the NMOS microprocessor and dynamic memories. This decade will be dominated by very high-speed CMOS as the primary volume process. This evolution is not only taking place with the industry but, in specific, with the microprogrammed bit-slice microprocessors. Today very high-speed, low-power CMOS is taking the place of very high-speed bipolar. CMOS is capable of operating faster and at 1/5 to 1/10 the power of bipolar technologies. Because of this, CMOS is becoming the technology of choice for bit-slice microprocessors.

In the past, technological changeovers have been expensive to the manufacturer as well as the consumer. The MICROSLICE™ family from IDT seeks to facilitate this transition by offering two families of CMOS bit-slice devices: IDT39C000, IDT49C000. The IDT39C000 family provides high-speed CMOS devices that fit into the sockets of current designs which utilize the 2900 family of bit-slice devices. The IDT39C000 family is pin-for-pin compatible to the 2900 family as well as compatible with its highest speed grade. An easy upgrade path is provided by the IDT49C000 family of bit-slice devices. This family starts off by providing higher densities, improved architecture, and progresses on into innovative architectures of the future.

RE-EMERGENCE OF MICROPROGRAMMING

As a result of CMOS, bit-slice microprogram designs are experiencing a new renaissance. In the mid-70s, the emergence of the 2900 family, as heralded by the 2901, was designed entirely using TTL bipolar technology. The 2901 has progressed from a propagation time — A/B to $\overline{G}/\overline{P}$ equal to 80ns — to the 2901C which sports 37ns. To achieve these final speeds though, the total TTL design had to be abandoned and ECL was substituted for the inner workings of the 2901, with TTL buffers interfacing to the outside world. Today at IDT, very high-speed CMOS is being used to produce an IDT39C01E with A/B to $\overline{G}/\overline{P}$ of 21ns, at 1/8 the power of the bipolar 2901C.

In parallel with the evolution of the 2901 has been the blossoming of the 2900 family to a multi-device product family. All of the latest designs use ECL internally. The trend in this family has been to add more and more gates on chip. To achieve this, though, more current has been consumed by each of the ICs starting with the 2901 at 1.25W to the 29300 family at approximately 8W. To handle the 8W, new packaging technology was developed which incorporates heat spreaders and cooling towers mounted on top.

Within the limits of maximum speed and density, tradeoffs can be made. For a given package, more speed can be achieved with less gates; or conversely, more gates can be incorporated at the expense of overall speed in critical paths. This relationship is referred to as the speed/power product of a given technology. The bipolar 2900 family has been extended to the limit of feasible packaging and cooling technology because of the density and speed requirements of today's applications. Very high-speed CMOS, in contrast, has a speed/power product an order-of-magnitude smaller than bipolar for the same speed. Therefore, CMOS requires less expensive packages and cooling systems.

COMPARISON OF FAMILY PERFORMANCE[1]

	MICROSLICE		BIPOLAR		
	SPEED (ns)	DYNAMIC POWER (mA)	SPEED (ns)	DYNAMIC POWER (mA)	SPEED PATH
IDT39C01C	37, 25	30	37, 25	265	A/B – $\overline{G}/\overline{P}$, C_n – F = 0
IDT39C01D	28, 17	35	—	—	A/B – $\overline{G}/\overline{P}$, C_n – F = 0
IDT39C01E	21, 14	40	—	—	A/B – $\overline{G}/\overline{P}$, C_n – F = 0
IDT39C10B	30	80	30	340	$\overline{CC}$ – Y
IDT39C10C	16	80	—	340	$\overline{CC}$ – Y

NOTE:

2588 tbl 01

1. Reflects performance over commercial temperature and voltage range.

A decade ago, CMOS was noted for lower power and low-performance. Today, CMOS is capable of running at speeds faster than bipolar at 1/5 to 1/10 the power. Dramatically smaller power consumption and smaller gate sizes allow for even higher levels of integrations to be achieved. In previous bipolar designs, an ALU, a barrel shifter, and a multiplier each required a package of their own for heat dissipation, whereas CMOS can incorporate them all on one piece of silicon while still having room to include a reasonable amount of RAM. This means that CMOS has room to grow, thus providing for new innovative architectures in the future.

While the lower power consumption allows for more gates in the same package, there is also freedom to shrink the size of the packages because the package is being used less as a means of dissipating the heat. This is timely because consumers are requesting more and more in smaller volume of space.

THE LATEST IN CMOS TECHNOLOGY

CEMOS™ is used to produce the MICROSLICE family with its two sub-families — named, respectively, the IDT39C000 family and the IDT49C000 family. These families address microprogrammable designs of the present and future. CEMOS is a trademark for the proprietary CMOS process technology of IDT. CEMOS is an enhanced CMOS technology which includes such features as high ESD protection, latch-up protection and high alpha particle immunity.

MICROSLICE IN EXISTING DESIGNS

The IDT39C000 family allows the designer to take advantage of very high-speed CMOS in existing designs. This family is a pin-for-pin compatible family with the 2900 counterparts. By replacing the current 2900 parts with IDT39C000 parts in existing sockets, the power consumption of that portion of the circuitry may be reduced down to 1/5 to 1/10 of the bipolar power consumption at full operating speeds. The IDT39C000 family is specified around the highest speed grade versions of the current bipolar devices. Currently in the IDT39C000 family is one of the common ALU architectures, the IDT39C01. Included in the family is the sequencer IDT39C10. The family also includes the 16 x 16 multipliers, IDT7216/17, and the 16 x 16 multiplier-accumulator, IDT7210. Not to be ignored, the IDT39C60 family is available for high-performance error correcting memory designs. This family also includes the first speed upgrade beyond the bipolar technology. The IDT39C01D is 25% faster than the 2901C, while the IDT39C01E exhibits speeds 40% faster than the 2901C.

THE IDT49C000 FAMILY, THE NEXT GENERATION

The IDT49C000 family takes advantage of all the benefits that CEMOS has to offer: high-speed, low-power, very large scale integration and smaller packages. Because of the new freedoms imparted by CEMOS, the IDT49C000 family is the next family of innovation for bit-slice microprogrammed designs.

While the IDT39C000 family minimizes upgrade costs by being pin-compatible, the IDT49C000 family addresses the aspect by providing parts in the family which are code-compatible, thus achieving conservation of previously written code. This is significant because, in the last decade, the cost of the software portion of the system has surpassed the hardware. The IDT49C000 family, however, is not limited to code-compatible devices and will, in the future, include devices with new and wider architectures.

THE IDT49C402A 16-BIT ALU PLUS

The first ALU in the IDT49C000 family is the IDT49C402A which is a 16-bit ALU and register file. This device is a superset of the 2901 architecture. It is a very high-speed, fully-cascadable 16-bit CMOS microprocessor slice, which combines the standard functions of four 2901s and one 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs. The IDT49C402A includes all of the normal functions associated with the standard 2901 bit-slice operation: (A) a 3-bit instruction field (I_0, I_1, I_2) which controls the source operands selection of the ALU; (B) a 3-bit microinstruction field (I_3, I_4, I_5) used to control the eight possible functions of the ALU; (C) eight destination control functions which are selected by the microcode inputs (I_6, I_7, I_8); and (D) a tenth instruction input (I_9) offering eight additional designation and control functions. This I_9 input, in conjunction with I_6, I_7 and I_8, allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU, and new combinations of destination functions with the RAM A-port output available at the Y output pins of the device. This eliminates bottlenecks of inputting data into the on-chip RAM.

The block diagram, Figure 1, shows the familiar architectures of the 2901 with register files which have both A and B data feeding into an ALU data source selector. This combines together the data from the register file along with direct data input (D) and the Q Register. The output of the ALU data source selector produces two operands, R and S. R and S are fed into an eight-function ALU, the output of which can go to the data output pins or be fed back into the register file and/or Q Register.

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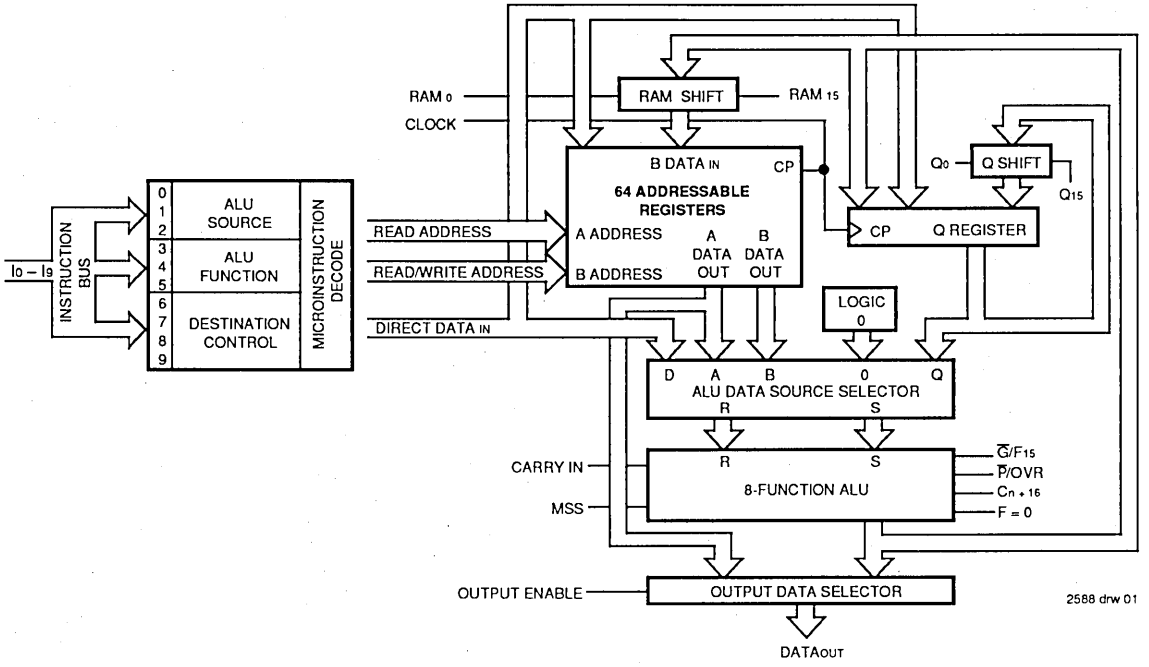

Figure 1. IDT49C402A 16-bit Microprocessor Slice

WHERE THE IDT49C402A EXCELS

The IDT49C402A, however, differs from the regular 2901 architecture by the addition of a new data bus that goes from the direct data input pins (D) into the register file and Q Register, thus providing a data path directly into the register file and Q Register rather than passing through the ALU block. With conventional 2901 architecture, in order to get data into the register file the ALU must be placed in the pass mode taking data directly from the D inputs through the ALU and around to the register file. With this new architecture, data can be operated on out of the register file and the Q Register and the result placed back in the Q Register while new direct data is being brought into the register file. Conversely, the Q Register can be loaded while operations are being performed on the register file and placed back into the register file.

Whereas the 2901 has a 16-deep register file, the IDT49C402A has 64 addressable registers. The 2901 architecture does not allow for direct cascading of the register file. Dead cycles can be eliminated because four times more data can be cached on-chip with the ALU. Other applications may use the 64 registers as four banks of 16 registers. The bank selection could be thought of as task switching for interrupt-driven multi-tasked applications.

The third difference from the 2901 is the ALU expansion mechanism. The IDT49C402A incorporates an MSS input which programs the device, being the most significant device or not. When not the most significant slice, the P and G signals are brought out. When the most significant slice, the sign and overflow are brought out on the P and G.

IDT49C402A 16-BIT ALU DESTINATION FUNCTIONS

	RAM	Q	Y-OUT
2901	F - Up	Q - Up	F
Functions	F - Up	—	F
(3-Bits I6 - I8)	F - Down	Q - Down	F
I9 HIGH	F - Down	—	F
	—	—	F
	—	Load F	F
	Load F	—	F
	Load F	—	A
Added	Load D	Load F	F
IDT	Load D	Load F	A
Functions	Load F	Load D	F
(1 Additional	Load F	Load D	A
Bit I9)	—	Q - Up	F
I9 LOW	—	Q - Down	F
	Load D	—	F
	—	Load D	F

2588 tbl 02

CODE CONSERVATION

The microinstruction word of the IDT49C402A looks the same as the 2901 with the exception of the additional destination control line called I9. Conservation of microcode can be achieved via two methods. The first and the most simple method is to tie the instruction line, I9, high on the socket and not connect it to the microcode. In this way, the remaining destination control lines, I8, I7 and I6, are compatible to the 2901.

For those systems that intend to add more code, or rewrite code for performance optimization, the second method is performed by making minor alterations on the microcode. For many designers this can be a fairly easily-achieved task by making minor alterations in the meta assembler used to compile the microcode source. The alteration in the meta assembler would add I9 such that all previously written code would have this signal default to a Don't Care state of high, thus enabling the standard destination instructions (the traditional 2901 codes). Additional code could then be written which utilizes this instruction line and the extra features provided in the IDT49C402.

An alternative to the second method for achieving microcode compatibility would take the already-compiled microcode and run it through a simple program, written in another language, which would spread the microcode apart and introduce in this additional instruction bit. This method is used for microcode which no longer has existing source.

ONE IDT49C402A WINS RACE AGAINST FOUR 2901s

While the IDT49C402A seeks to improve performance through architectural enhancements, it also achieves improved performance through raw technology. The IDT49C402A achieves an A and B address to Y output of 41ns for military and 37ns for commercial temperature ranges, as compared to four 2901Cs and a 2902A which have A and B to Y and flag of 80ns for military and 68ns for commercial. Thus, the IDT49C402A is 45% faster than five discrete parts of the older 2900 family, the IDT49C402A could achieve processing of approximately 15 MIPS.

COMPARISON OF 16-BIT MICROPROGRAMMED SOLUTIONS

	IDT49C402A CMOS	4 — 2901C & 2902A BIPOLAR	29116 BIPOLAR
Dynamic Power(1)	125mA	1049mA	735mA
ABI – V/FLAG(1)	37ns	68ns	84ns
Package Space Sq. Inches	0.32 LCC 1.5 DIP	1.8 LCC 5.04 DIP	0.56 LCC 2.08 DIP
Features	ALU 64 RAM Q REG SHIFTER	ALU 16 RAM Q REG SHIFTER	ALU 32 RAM ACCUM BAR. SHIFT

NOTE: 2588 tbl 03

1. Reflects performance over commercial temperature and voltage range.

THE IDT49C402A IS COOL

Even though the IDT49C402A has five times the circuitry on-chip as does the 2901, it is 1/2 the power of just one 2901.

The 16-bit solution of the IDT49C402A is 1/8 the power of four 2901Cs and one 2902A. While total power consumption is the concern of many designers because it has impact on power supplies and cooling systems, the lower power consumption also provides other benefits. Because less power is being consumed, less of the package is needed as a heat sink. This allows for packages with much smaller outlines. Besides being offered in a standard 68-pin PGA, the IDT49C402A comes in a standard 68-pin LCC with pad spacing of 50 mil centers. When the board space taken up by just the packages are added up, the LCC version of the IDT49C402A is 0.32 square inches, as opposed to 1.8 square inches for four 2901Cs and a 2902A. Respectively, the IDT49C402A in the PGA package is 1.0 square inches as opposed to 5 square inches for four 2901Cs and a 2902A. Not included in the calculations for the multi-chip solutions is the spacing between the ICs.

A 16-BIT SEQUENCER TO MATCH A 16-BIT ALU

While ALUs provide the data path for performing computations, the sequencer is another important building block which orchestrates the entire machine. The first sequencer in the IDT49C000 family is the IDT49C410. The IDT49C410 is architecture- and function code-compatible to the 2910A, with an expanded 16-bit address path which allows for programs up to 64K words in length.

The IDT49C410 is a microprogram address sequencer intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the sequential accesses, it provides conditional branching to any microinstruction within its 64K word range.

While the 2910A incorporates a 9-deep stack, the IDT49C410 has a 33-deep stack which provides micro subroutine return linkage and looping capability. This deep stack can be used for highly nested microcode applications.

Referring to Figure 2, it can be observed that, during each microinstruction, the microprogram controller provides a 16-bit address from one of four sources: 1) the microprogram address register (μPC) which usually contains an address of one greater than the previous address; 2) an internal direct input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; 4) a last-in first-out stack (F).

The IDT49C410 is completely code-compatible with the 2910A. This allows the IDT49C410 to execute previously written microcode, while allowing for more microcode to be added to the application and taking the program beyond the 4K word boundary. Because the IDT49C410 is microcode-compatible, older microcode routines can be incorporated in new designs utilizing the IDT49C410.

The 16-bit IDT49C410 uses approximately 1/4 the power consumption of the 2910A (which is a 12-bit sequencer), thus maintaining the 1/5 power consumption on a bit-by-bit basis. The IDT49C410 consumes, over frequency and

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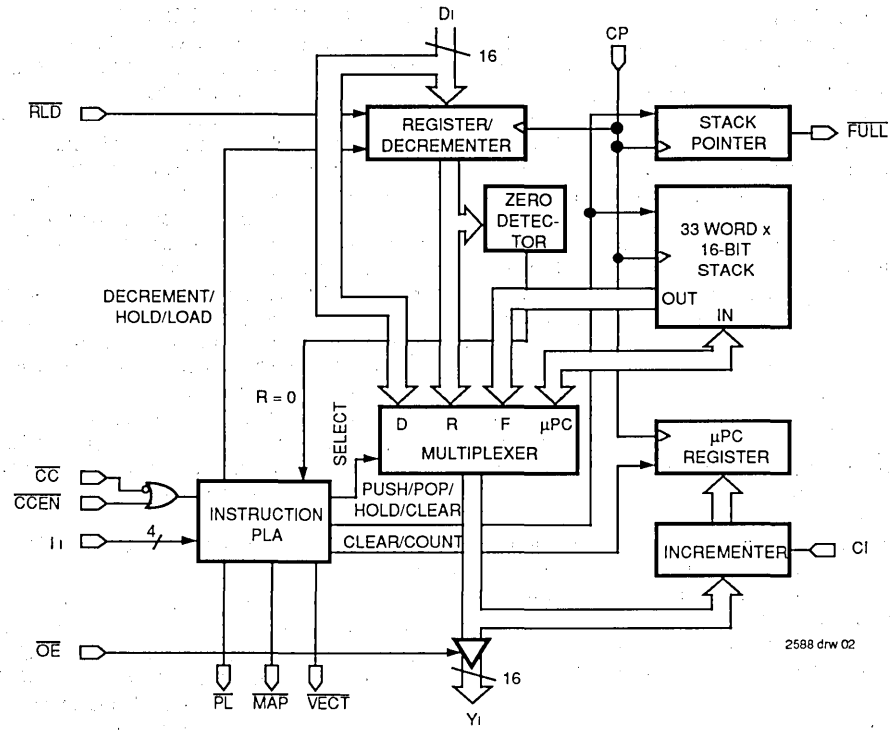

Figure 2. IDT49C410 16-bit Microprogram Sequencer

temperature ranges, 75mA for commercial and 90mA for military. The 2910A compares with 340mA for military and 344mA for commercial. Because of the lower power consumption, smaller packaging may be utilized. The IDT49C410 is offered in a standard 600 mil wide package with pins on tenth inch spaces.

WORKING TOGETHER

The simplified block diagram of an example Central Processing Unit (CPU) is shown in Figure 3 using devices manufactured by IDT. This CPU architecture can be viewed as two major sections which have a MICROSLICE family part at the heart of each. The major section of the left hand side of the diagram is the control path. The microprogram sequencer at the heart is the IDT49C410 which generates the address for the microprogram stored in the writeable control store (WCS). The output of the WCS is registered by the pipeline register. Together, the sequencer, WCS and pipeline register make up a state machine which controls the operation of the entire CPU. In this CPU, the state machine first fetches a machine instruction and captures it in the instruction register. The instruction register determines the starting address for each sequence of microinstructions associated with each machine opcode.

In this example, both the microprogram store and the instruction mapping memory are formed using RAM. The RAM has separate DATAIN and DATAOUT buses (IDT71682). This allows the input side to be connected conveniently to an 8-bit bus for initialization at power up.

The second major section is on the right hand side. This section is called the data path. The heart of this section is the IDT49C402A. In it is contained all of the working registers and the arithmetic logic unit for performing data computations. One of the internal registers always contains the value of the program counter (PC) which is the address at which the opcode for the machine instruction is fetched. When an opcode is fetched, the memory address register (MAR) is loaded with the value of the PC while, at the same time, the value of the PC plus one is loaded back into the internal register file. The DATAIN and DATAOUT registers are used to buffer data coming from and going to the memory during execution of the machine instruction.

COMPARISON OF MICROPROGRAM SEQUENCERS

	IDT49C410A	IDT49C410	2910A
$\overline{CC}$ – Y[1]	15ns	24ns	24ns
Stack Depth	33	33	9
Address Range	64K	64K	4K
Dynamic Power[1]	75mA	75mA	340mA

2588 tbl 04

NOTE:
1. Reflects performance over commercial temperature and vlotage range.

CONCLUSION

The MICROSLICE family from IDT provides high-performance CMOS solutions for microprogrammed applications. Not only does the family provide for yesterday's designs with plug-compatible devices of the IDT39C000 family, it also provides solutions for future applications. With the IDT49C000 family, the designer can take advantage not only of the lower power consumption of CMOS, but utilize higher speeds and smaller board spacing, yielding smaller packaging concepts required by today's customers. In the future, the IDT49C000 MICROSLICE family will provide alternative architectures which will provide for yet higher performance solutions.

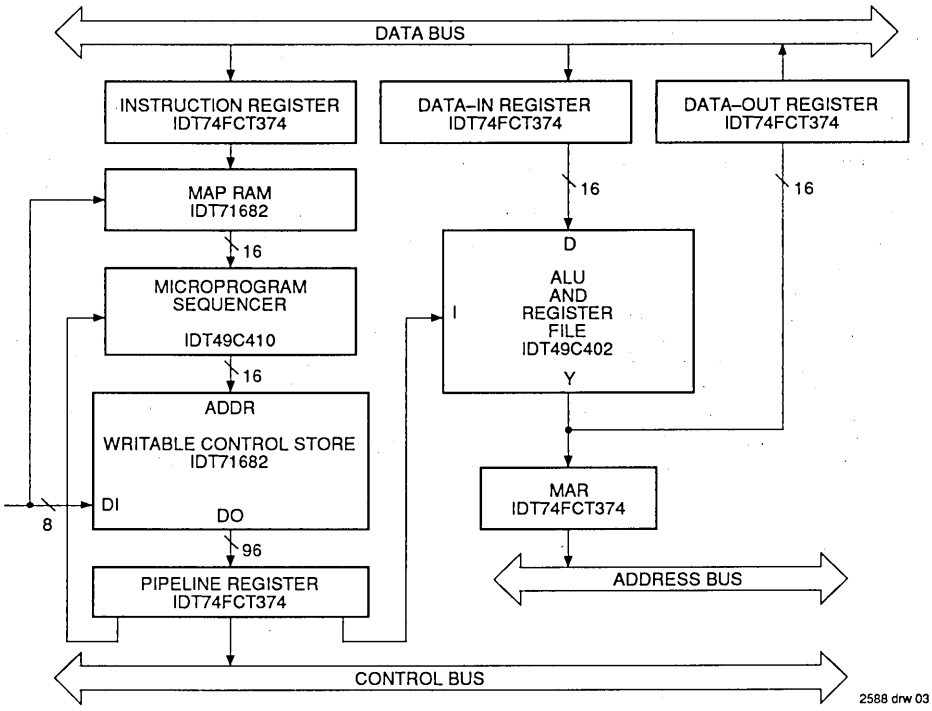

Figure 3. Central Processing Unit Block Diagram

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Integrated Device Technology, Inc.

FIR FILTER IMPLEMENTATION USING FIFO AND MACs

APPLICATION NOTE AN-17

By Suneel Rajpal and Dave Wyland

INTRODUCTION

This application note shows a relatively simple method of implementing an N-tap finite duration impulse response (FIR) filter using FIFOs for the data and coefficient storage instead of space-consuming counters, RAMs and control logic. The multiply-accumulate operations can be performed 16 x 16 multiply-accumulators (MACs) such as the IDT7210.

Finite duration impulse response filters are popular in many DSP applications. FIRs have no feedback elements and no poles and they are unconditionally stable. Also, with FIRs one can have linear phase response that may be important for certain applications.

FIR filters are one of the basic building blocks of digital signal processing (DSP). The FIR filter uses digital multipliers and accumulators to perform a series approximation of an analog filter. High-pass, low-pass and band-pass filters may be implemented. The digital FIR filter has several advantages over its analog counterpart. Its performance can be precisely specified and does not drift with time. Also, the filter type and performance can be changed with no change in hardware components and not introduce any amplifier noise. These features make the FIR filter popular in high-performance designs.

The FIR filter continuously processes (i.e. filters) the digital equivalent of the input analog signal. It does this by processing each input digital data word in a repetitive manner as a sum-of-products algorithm. In this algorithm, the current data word and some number of previous data words used and by the coefficients. The number of data words used is called the number of filter taps. An N-tap filter uses N data words and coefficients in the FIR calculation.

An FIR can be thought of as an average of incoming data values. Each of the successive data values is multiplied by its own coefficient and these values are totaled by an adder. A block diagram of this operation is shown in Figure 1. This sequence continues for each clock cycle as each data value advances one position and is multiplied by a new coefficient and a new sum is output. If one used a multiplier for every tap, a1 to a4, and an adder that added the four products (the multiplier outputs), a result can be obtained every cycle.

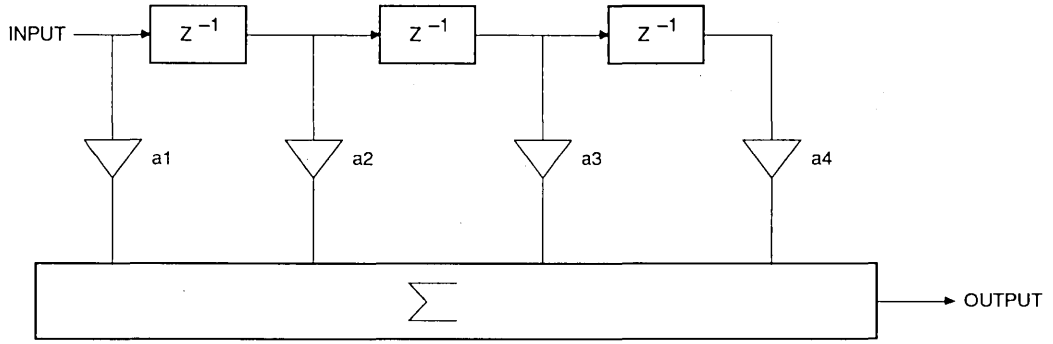


Figure 1. FIR Block Diagram

In many applications, only one MAC is used and the calculation is performed in 4 clock cycles for a four tap filter. If a single chip MAC is used, the appropriate data and coefficients are loaded to the MAC input registers. A new output results every four cycles, while a new input data value is loaded every four cycles. The hardware for loading the data and the coefficients is RAM with up/down counters and some logic. However, with the advent of FIFOs with asynchronous read and write capabilities and retransmit capability, one can have a better solution.

The IDT7201/7202 are high-speed 512 x 9 and 1K x 9 FIFOs that can be used to hold the data and coefficients for FIR filters. Higher density FIFOs such as the IDT7203/7204 (2K x 9/4K x 9) are also available. The IDT7201/7202, shown in Figure 2, are high-speed buffers that have an access time of 35ns and a cycle time of 45ns. These FIFOs support asynchronous and simultaneous read and write operations. On every falling edge of the write line, a new write cycle begins and the read pointer is incremented on every rising read edge. The data is available after a delay of t_A (or 35ns for the highest speed part) after the falling read edge.

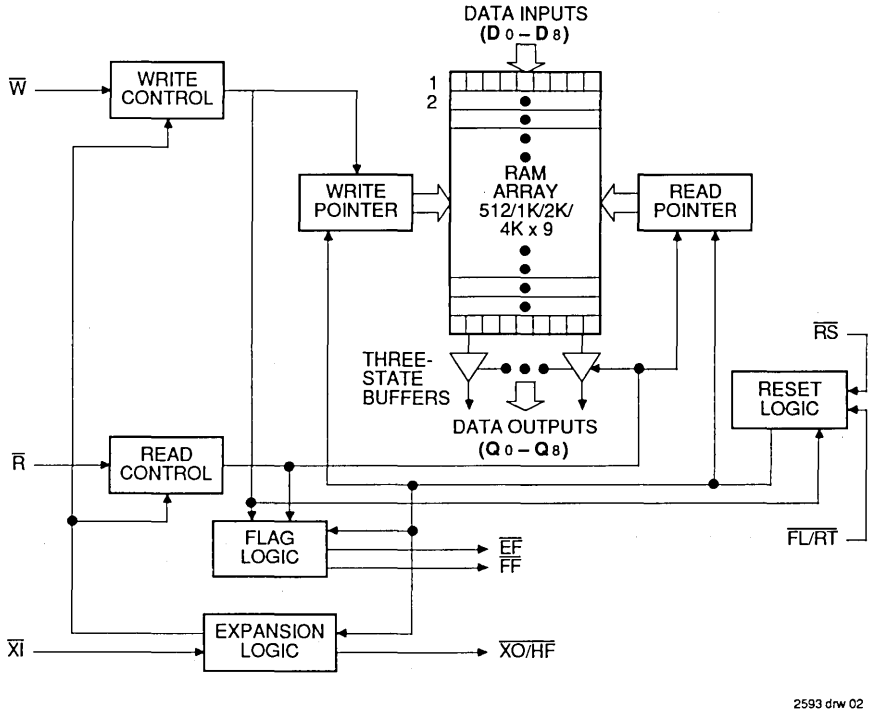


Figure 2. FIFO Block Diagram

The IDT7201/7202 FIFOs have a retransmit feature which is particularly useful in applications where the same data is repeatedly required. In a FIFO, N bytes can be written and then read. The retransmit feature allows the same N bytes to be read again without rewriting them. The retransmit feature resets the read pointer in the FIFO to zero, allowing a reread of the written information. If a FIFO is used to hold the filter coefficients, the retransmit feature can be used to reread the coefficients for each FIR calculation pass without having to reload them. Retransmit is performed by pulsing the retransmit input with the read and write clock lines high. This is shown in Figure 3 and, in greater detail, in Figure 7.

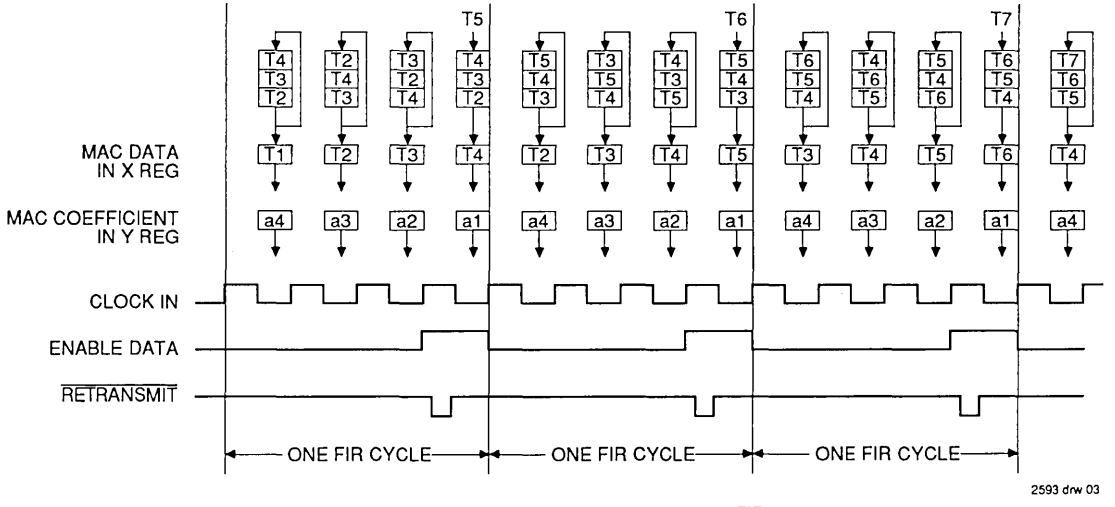


Figure 3. Sequence of Operations to Perform an FIR

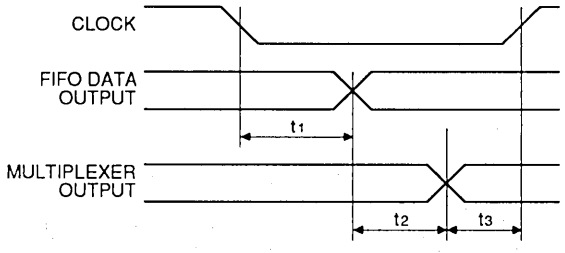
The clock cycle time can be at 120ns with a 50% duty cycle. For the data storage, the data is read from the FIFO, passes through the multiplexer and is then stored back in the FIFO. The delay path for the clock low time is as follows:

Read Going Low to Data on FIFO Output	35ns
FIFO Output to Multiplexer Output	5ns
Multiplexer Output to Write Going Low-to-High (Set-up)	18ns
Minimum Clock Low Time	58ns

The delay path for the clock high time is as follows:

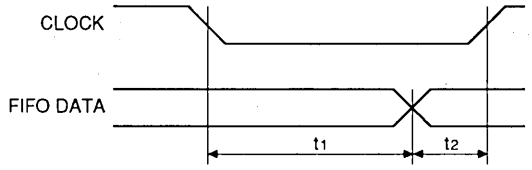
Control Circuit to Have RT Go From High-to-Low	10ns
Retransmit Minimum Low Time	35ns
Read and Write High Time After the RT Low-to-High	10ns
Minimum Clock High Time	55ns

Timing diagrams for these cases are shown in Figures 4 and 5.



t1 = FIFO Access Time, tA = 35ns
t2 = Multiplexer Delay = 5ns
t3 = FIFO Input Set-up Time = 18ns

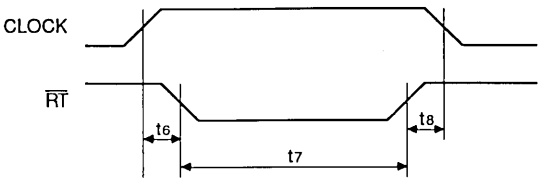
2593 drw 04



t1 = FIFO Access Time = 35ns
t2 = MAC Data Set-up Time = 25ns on 100ns (Com'l.) MAC

2593 drw 05

Figure 4. Clock Low Timings



t6 = Time for External Circuit to Create $\overline{RT}$ Going From High-to-Low = 10ns
t7 = Minimum Pulse Width for Retransmit Pulse = 35ns
t8 = Read/Write High Time Requirement After the RT Goes From Low-to-High = 10ns

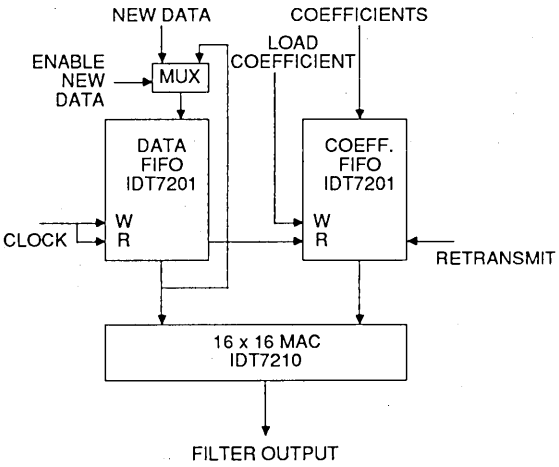
2593 drw 06

Figure 5. Clock High Timings

The MACs have input registers and an output accumulator. The MAC specification is based on the multiply-accumulate time or the time it takes for the input operates to be multiplied, the accumulator added or subtracted from this product and the result stored in the accumulator. The specification, called the multiply-accumulate time, is a register-to-register delay.

Another timing consideration for the data path is the set-up time for the MACs input registers. In the case of the FIFO loading data to the MAC, the tA of the FIFO plus the set-up of the MAC is 60ns (for the IDT7210 100ns MACs) and this delay is equal to the suggested clock low time.

With the configuration shown in Figure 6, the clocked cycle time is 120ns at a 50% duty cycle using 35ns FIFOs (IDT7201/2) and 100ns multiplier-accumulators (IDT7210). This system gives an output every 120ns where N is the number of taps.



2593 drw 07

Figure 6. Logic Implementation of N-Tap FIR

If the 120ns cycle time is considered slow for the user's application, a faster speed of 70ns cycle (60ns clock low and 10ns clock high) can be achieved. This is done by recirculating the coefficient through the FIFO using a multiplexer instead of using the retransmit feature, as shown in Figure 7. This is similar to the way the data is recirculated on the left side of Figure 6. The difference is that the coefficients are loaded into the FIFO initially from another source and, after loading, the FIFO output data becomes its input data (i.e., the input MUX selects the FIFO output to be the input after the initial loading of the coefficients). This configuration reduces the clock high minimum time requirements as the retransmit feature is not used. The clock low time does not change from the 60ns value.

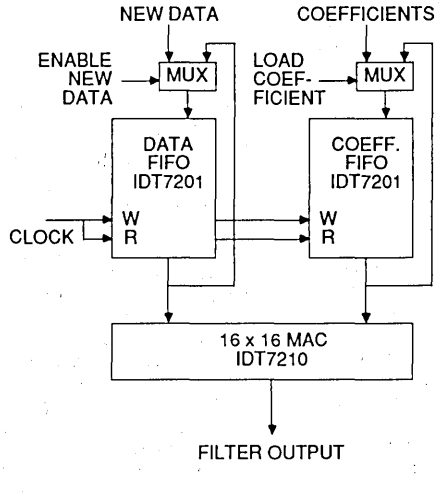


Figure 7. Logic Implementation of a Higher Speed N-Tap FIR

The FIFOs used in this application have 35ns access times, but MACs faster than the 100ns used in the previous example have to be used. IDT has MACs that are as fast as 35ns clocked multiply-accumulate times and these would have to be used if the clock high time was only 10ns. The FIFO read and write minimum high times are also 10ns. This system yields a filter that gives an output every 70ns where N is the number of taps.

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Integrated Device Technology, Inc.

DESIGNING WITH THE IDT49C460 AND IDT39C60 ERROR DETECTION AND CORRECTION UNITS

APPLICATION NOTE AN-24

By Robert Stodleck

INTRODUCTION

The Error Detection and Correction (EDC) chip itself is one element of an EDC system. How it is connected to the surrounding system and controlled is left to the system designer. Because there are so many design variations possible, it is important for the designer to develop a clear idea of the target design before beginning the design process. Basic design approaches and perturbations are enumerated in this application note.

The details of the EDC control logic depend on the configuration of the EDC system, EDC bus topology, the nature of the CPU or system bus involved and the nature of diagnostic hardware used. The data bus topology is highly dependent on the individual target system.

This applications note approaches the bus topology issue first. The advantages and disadvantages of using EDC word widths that are different from the system bus are discussed. The next topic to be covered is the use of EDC in a system with a cache. Then the operational configuration of the EDC system is discussed. This implies answering questions about how the EDC unit handles errors in a particular system is discussed. How an operating system deals with the EDC function is discussed, followed by a practical discussion of some non obvious hardware topics. The final topic is memory system diagnostics and verification. An appendix includes tables and software that are useful in debugging and in writing diagnostic software for an EDC board.

Data Bus Topology

Most contemporary CPUs execute write operations of a byte or other sub-word width types. These cause special problems for all EDC units since EDC transactions with the memory are carried out on whole width EDC words. To facilitate partial word write operations with the IDT39C60 or IDT49C460 type EDC units, a set of tri-state transceivers are normally required between the system bus and the EDC unit. These buffers are required to prevent bus contention between the CPU or system bus drivers and the EDC units data outputs during partial word write operations. Figure 3 shows a bus arrangement appropriate for large DRAM arrays. The need for isolation of the EDC data bus and the system bus is shown by examining the data paths, shown with white arrows. These are used by the final write operation of a partial-word write cycle. In this case, only data bits 0-7 are being written from the processor to memory. If the processor or system bus drivers can be tri-stated on byte boundaries then this set of buffers could be removed, but this is not a common situation.

Depending on the memory size, additional buffering may be required between the EDC and the memory bus proper. The buffer configuration must be determined before beginning the EDC and memory controller design.

An appropriate general purpose bus topology is shown in Figure 1. It is common for one or the other sets of bi-directional buffers to be a latched type such as an IDT74FCT646 instead of the IDT74FCT245 shown. A family of waveforms appropriate for the bus format shown in Figure 1 is shown in Figure 2. The waveform diagrams do not include precise timing considerations which are left to the designer.

In any given system, any of the buffers separating the EDC from the memory IC's may be eliminated if bus capacitance and speed considerations allow.

EDC Bus Width vs. System Bus Width

The width of the EDC bus and the System Bus are normally matched. However, there are valid reasons for making the EDC bus both wider or narrower than the system bus.

Wide EDC words are significantly more efficient than narrower EDC word widths in terms of the amount of check-bit memory used for a given amount of data memory. The amount of check-bit memory required for 64 data bits is 8 bits if the 64 data bits are organized as one word and 14 bits if it is handled as two 32-bit words. Twenty-four bits of check-bit memory would required for 64 data bits organized as four 16-bit EDC data words.

For the purposes of speed, it would be ideal to have 8-bit EDC words for systems that do byte write operations. This would make it unnecessary to ever have to read a memory location prior to writing a partial word on these systems. Unfortunately, eight-bit EDC words are grossly inefficient in terms of check-bit memory usage. Therefore, the EDC word widths are normally 16-bits or more.

Since the EDC word widths must generally be 16-bits or more for check-bit memory efficiency, and since general-purpose computers generally use byte or partial-word-write operations, general-purpose computers force the EDC unit to be able to process partial EDC word-width write operations. Partial word-width write operations require the EDC subsystem to execute a read-modify-write type memory cycle. Thus, the EDC controller must take over control of the memory system and execute a read before completing a partial word write. For some applications, where EDC is in use, it may be desirable to speed up processing by prohibiting partial word operations either at the hardware level or software level. Speed critical sections of code should be executed without partial-word write operations.

The read-modify-write EDC cycle executed during a partial-word write is identical to the EDC correction cycle executed during a read cycle when an error has occurred. The read-modify-write EDC cycle should not be confused with the read-modify write cycle executed by some CPU's.

Verification of a memory system using an EDC word wider than the system word is complicated by the fact that all memory write cycles become read-modify-write cycles i.e. partial-word-write EDC cycles. Careful consideration of diagnostic procedures needs to be made during the design to avoid unnecessarily complex debugging procedures.

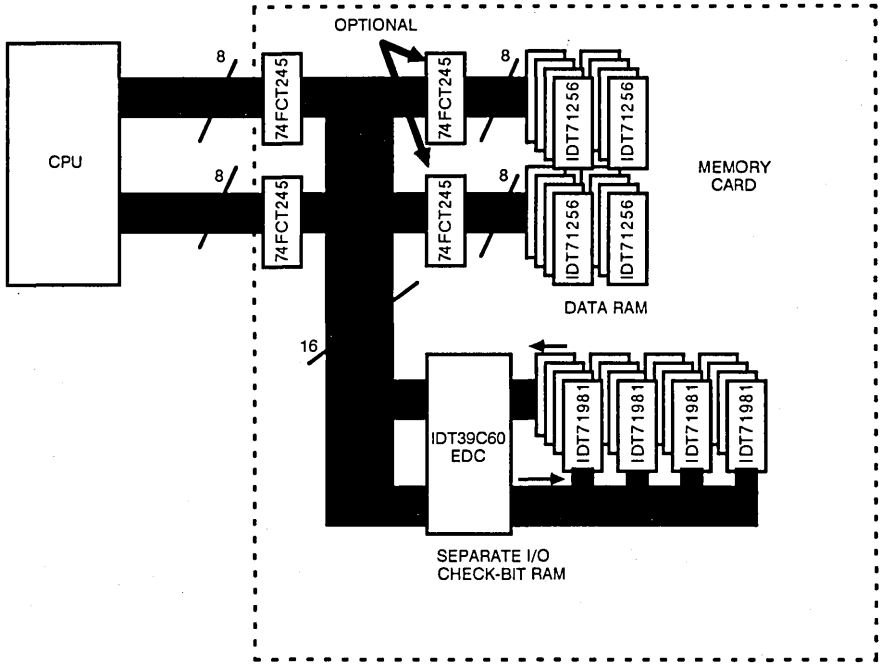

Figure 1. A general purpose 16-bit EDC data bus topology. Corresponding timing waveforms are shown in Figure 2. IDT74FCT245 buffers separate the EDC data bus from the CPU and the main memory. Separate-I/O RAMs are used in the check-bit memory.

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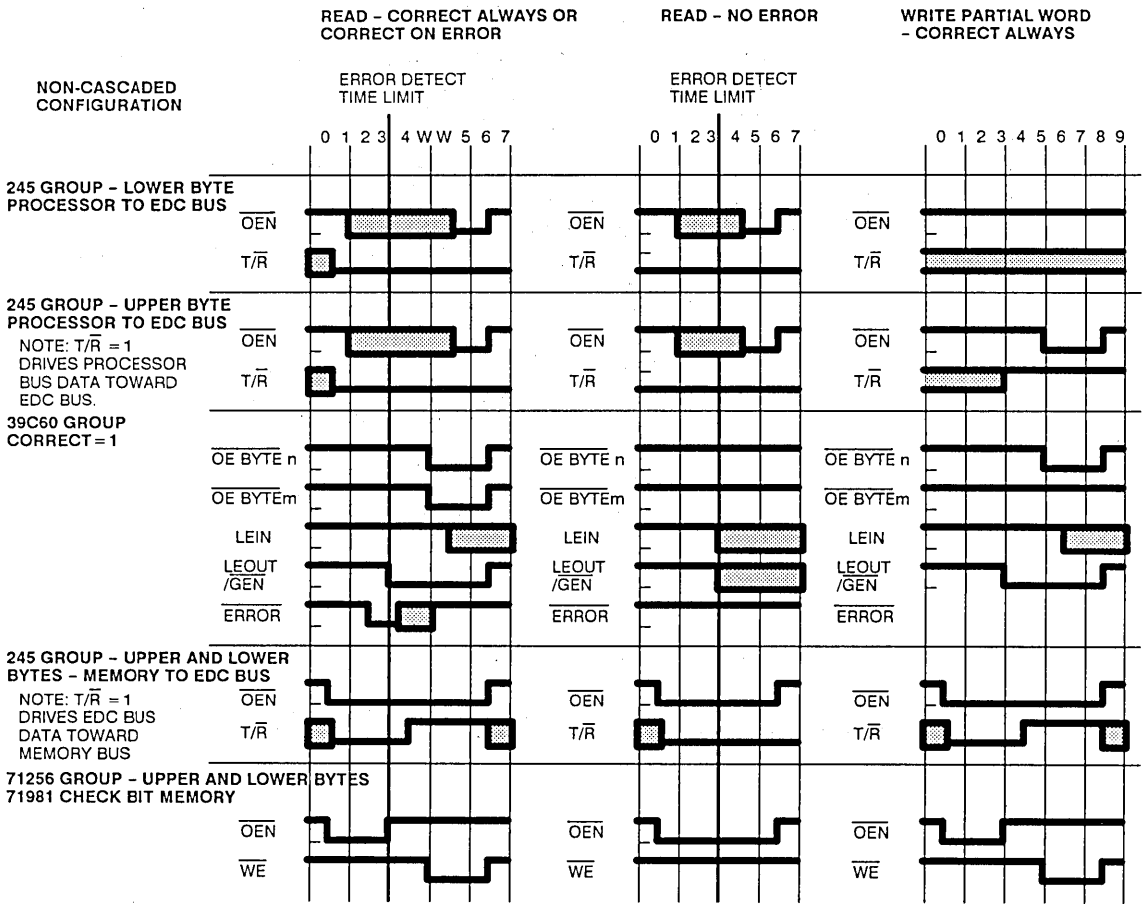

Figure 2. A sample family of timing waveforms for an EDC system. The target system is based on IDT71256 static RAMs for main memory with IDT71981 separate I/O RAMs for checkbit memory. (See Figure 1.) The partial word write case illustrates a low order byte write.

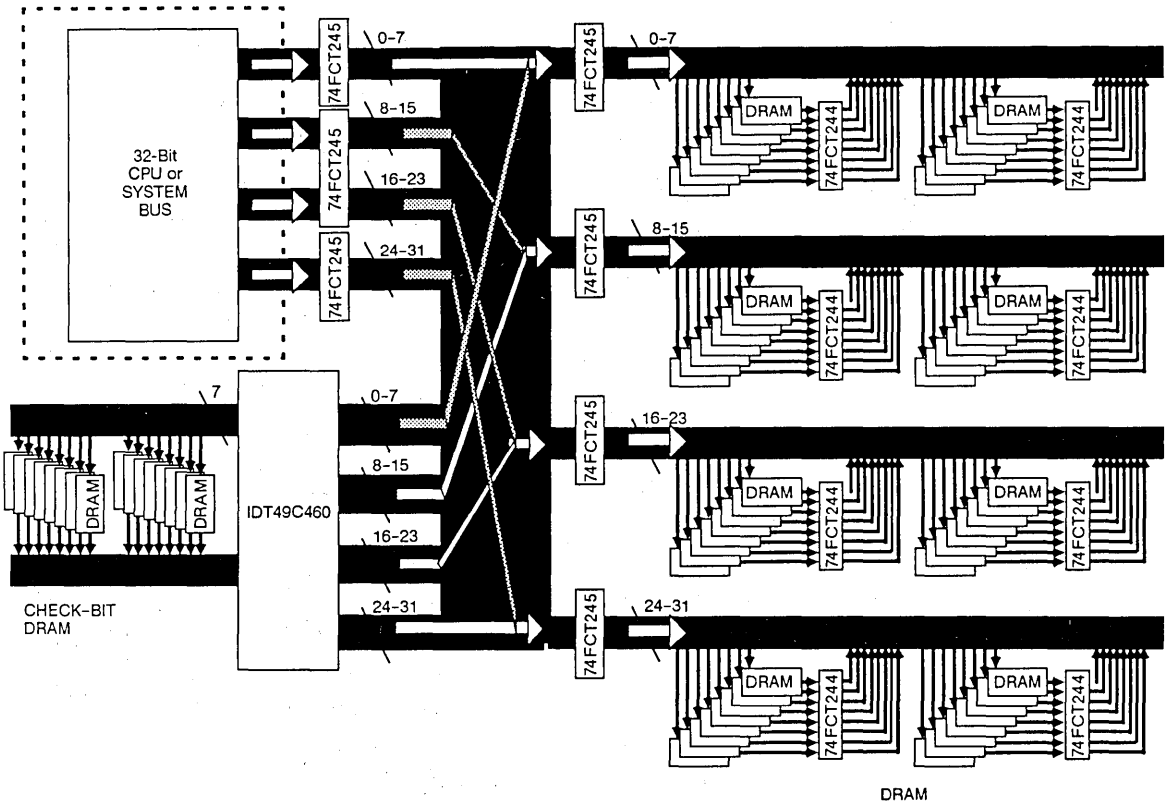

Figure 3. A general purpose 32-bit EDC bus topology for 1 bit wide DRAMS. The white arrows indicate the data flow paths used on the final write phase of a partial word write cycle. Data bits 0-7 are being written into memory from the processor.

EDC in Systems Using Cache

In systems using cache memory, it may be desirable to place the EDC function between the cache and main memory, as opposed to locating the EDC function between the processing elements and cache. Parity can be used as a single-bit error detection scheme between the CPU and cache. RISC architectures tend to require more memory accesses per unit time that complex-instruction-set processors. This makes the use of cache memory more important in the RISC system. An appropriate bus topology for a RISC type processor with cache memory is shown in Figure 4.

Use of a cache memory also affords the possibility of using a different error correcting philosophy. If the EDC function is located between the cache and main memory, then it may be allowable for data reads to be corrected and sent on to the cache, but not to be immediately written back to main memory, after an error has been discovered. In this approach, corrected memory words are updated in the normal write-back processes of the cache memory.

Instruction reads must be thought of differently than data reads since instructions are normally not written back to memory from the cache. However, it may be possible to not write a corrected instruction word back to memory after detection, since the instruction is usually backed up on a different media. In most systems there is no way for the EDC to know whether it is operating on instructions or data, so a correction philosophy must be selected that can be applied to both instruction and data words.

Diagnostic Hardware

A syndrome latch for capturing syndrome values after errors and transferring them to the system data bus is always recommended. Providing a check-bit memory read-back ability allows direct verification of the gross functionality of the check-bit memory 'on board'. This greatly facilitates check-bit memory verification. More subtle problems can be explored indirectly by interpreting correction patterns on known data or by using syndrome data to interpret failure patterns. Depending on the EDC configuration, it may be possible to use the same latch to capture check-bits from the check-bit memory, or a second latch may be provided to allow this.

Ideally, diagnostic hardware includes address latches to capture the address of an error. However, this may not be practical in any particular application. It may be sufficient to identify the individual RAM in which an error has occurred.

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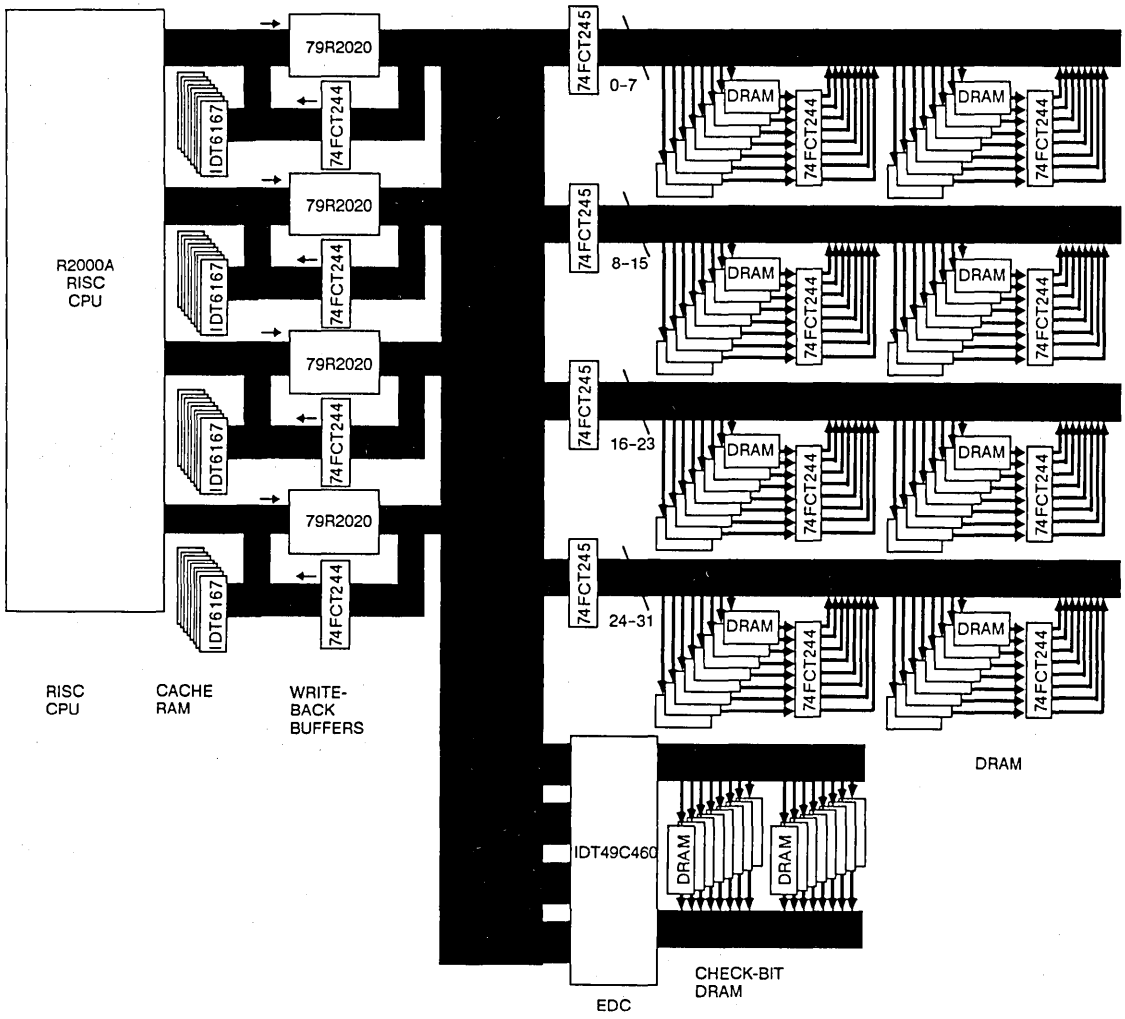


Figure 4. An EDC bus arrangement appropriate for a CPU with caches such as the IDT R3000 or IDT R2000 RISC processor.

OVERVIEW OF EDC OPERATIONAL MODES

Bus Watch vs. Correct Always for the Memory Read Cycle

In a bus-watch system, errors are only corrected after they have been detected by the EDC chip. Data is corrected and written back to memory to scrub errors, only after an error has been detected. In theory, the EDC chip only "watches" the bus normally, and does not slow memory read cycles with correction delays unless an error has been detected. Since errors during read operations are normally very rare, read cycle bus-watch systems are normally faster than correct-always systems.

In correct-always systems, data read by the system is always corrected. The EDC control logic is simpler to design and implement because there is only one type of read cycle. Memory cycle timing in correct-always systems can be completely deterministic and thus such systems may lend themselves more effectively to real-time applications.

Bus Watch vs. Correct Always for the Partial Word Write Cycle

A write operation that is of a width less than the EDC word width forces the EDC subsystem to execute a read cycle prior to actually writing to memory. This is required to provide the EDC unit with the whole data word to be written into memory for the purpose of check-bit generation. No time is saved by not correcting the data read from memory prior to the subsequent write operation. The partial-word-write operation is virtually identical to a read cycle in correct-always mode or a read cycle with an error detected. Consequently, a partial word write is usually done in a "correct always" mode.

Operating System Involvement

In systems capable of doing partial-word-write operations, it is necessary to initialize the memory on power up. This can be done in hardware but it is usually done by the operating system. Initialization implies writing every memory location with an arbitrarily chosen constant and thereby writing the check-bit memory with the correct corresponding check-bits. The need to initialize memory results from the nature of the read-modify-write EDC cycle required by the event of a partial-word-write operation. If the memory has not been initialized, the read cycle will normally result in an error indication and an attempt to 'correct' a bit in the data field before writing back to memory. This tends to introduce errors into previously written data bytes or sub-words.

It is possible to design a state machine EDC controller that corrects all single bit errors in a fashion transparent to the CPU. This is not always desirable since it masks hard single-bit errors that indicate hardware problems. In any case, the operating system must become involved in the event of multiple errors if only to issue an appropriate error message to the system operator.

It is desirable to log single bit errors and as much information about the error as is practical. Relevant data ideally includes the syndrome bits to identify the bit location in the word, and the physical address of the error. For complete EDC transparency, such as that desired for real time systems, error logging must be eliminated or accommodated entirely in hardware. For non real-time systems, interrupting the CPU after an error occurrence is the conventional way to log error data. Syndrome data is collected, and any other error information the system hardware retains is retrieved.

Non-obvious Hardware Topics

In a 32-bit system with a bi-directional check-bit bus or in 64-bit cascaded mode, the check-bit input-output and syndrome functions are time-multiplexed onto the same bus. If the EDC unit is in the correction mode, the input latches are open, and the OESC pins are low, the bus will tend to oscillate. This combination of control inputs would not be appropriate for normal operation but might occur in an idle period between memory cycles unless the designer specifically designs this condition out. The oscillation occurs in this condition because the EDC units are attempting to output syndrome bits based on the data and 'check-bit' inputs. However, the syndrome outputs in this state are being fed back to the check-bit inputs. The result is an oscillation on the check-bit/ syndrome bus.

It is an important and sometimes overlooked fact that it is not acceptable to allow inputs on most CMOS parts to 'float'. The result of doing this is increased power consumption, on chip noise and sometimes outright oscillation which can lead to latch-up. The check-bit inputs and the data bus of an EDC unit should not be allowed to float when not being used. In low power systems in particular, all inputs not in use must be brought to logic highs or lows when not in use. This may imply not tri-stating some buffers that would otherwise be tri-stated when not actively driving, or actually including pull-up or pull-down resistors on a bus to bias it when it is not actively being driven.

Basic EDC Unit Operation

Basic 32-bit 49C460 EDC operation with timing diagrams is illustrated in Figures 5, 6 and 7. These timing diagrams are also appropriate for a 16-bit IDT39C60 system. In the IDT39C60, the LEout and the Generate functions have separate pins. In the IDT49C460, they are both controlled by one pin. It is usually convenient when using the IDT39C60 to wire the two pins together.

In the non-expanded case, with either EDC unit, use of the input latch may be convenient but is not logically dictated (i.e. the LEin pin may be tied high). Also, the correct pin may be simply left asserted in normal operation. The "detect" mode is usually only used as a diagnostic aid, which allows the data correction function to be shut off while still generating an error signal based on the input data.

Diagnostic Modes

Since the EDC function introduces a complicating layer between the system bus and the memory, diagnostic modes are provided for the EDC to provide testability for the entire memory subsystem. In memory systems where the EDC word is wider that the system bus memory, verification is complicated by the fact that all writes are partial word writes. Good diagnostic design requires forethought.

The EDC unit's internal diagnostic latches have two distinct and unrelated data fields. The check-bit data field is used to provide check data to be substituted for normal check-bits in the diagnostic modes. These will be written to memory in diagnostic generate mode, or substituted for check-bits read from memory in diagnostic-detect or correct mode. The second field in the diagnostic latch is the control field. The control field is ignored except when the part is placed in the internal control mode.

The control byte is used to control the operating features of the part when the part has been placed in internal control mode. Each bit in the control field corresponds to a pin on the part and overrides the logic sense of that pin when the part is in the internal control mode. For example, we could place the part into the correct mode by setting the correct pin on the EDC unit to a logic high, or we could put the part into the internal control mode and set the correct bit in the diagnostic latch to '1'. Thus there are always two ways to achieve any mode of operation. For example, the diagnostic modes may be entered by setting the external diagnostic inputs appropriately, or entering the internal control mode and setting the diagnostic latch bits appropriately. The internal control mode is provided as a convenience and is useful for controlling operating modes during diagnostic testing and software initialization. Conceptually, it is important to realize that anything that can be done in this mode can be done with external logic as well.

Memory System Verification Strategies

When a new design is being verified, it is critical to isolate different problem factors; this is one function of the EDC diagnostics.

To prove the function of the primary memory array, the EDC unit is placed in the pass-through mode so that it does not interact with the data stream. Once the primary memory array has been verified as functional, the check-bit memory must be verified. The diagnostic generate mode is used to write known data into the check-bit memory. Reading the check-bit memory directly through the EDC is not possible, so gross functional testing must be done via an external latch or with a logic analyzer. Using an external latch greatly facilitates check-bit memory verification.

Collecting syndrome data from error events requires that an external latch be included in the design to capture the syndrome data after an error has occurred. It should be possible to clear this latch after reading its contents from the system bus. Depending on the EDC configuration, it may be possible to use the same latch to capture check-bits from the check-bit memory. More subtle problems can be explored indirectly by interpreting correction patterns on known data or by using syndrome data to interpret failure patterns.

SUMMARY

The error detection and correction unit is located in the critical path between a CPU and the memory. The operational configuration of the EDC intimately affects the speed of the final system. Due to the wide variation between computer architectures that EDC is desirable for, the EDC unit is necessarily a generalized IC. Thus, designing an EDC system is not a straightforward process. The object of this applications note has been to illuminate some of the topics that any designer will encounter in the process of designing an EDC system.

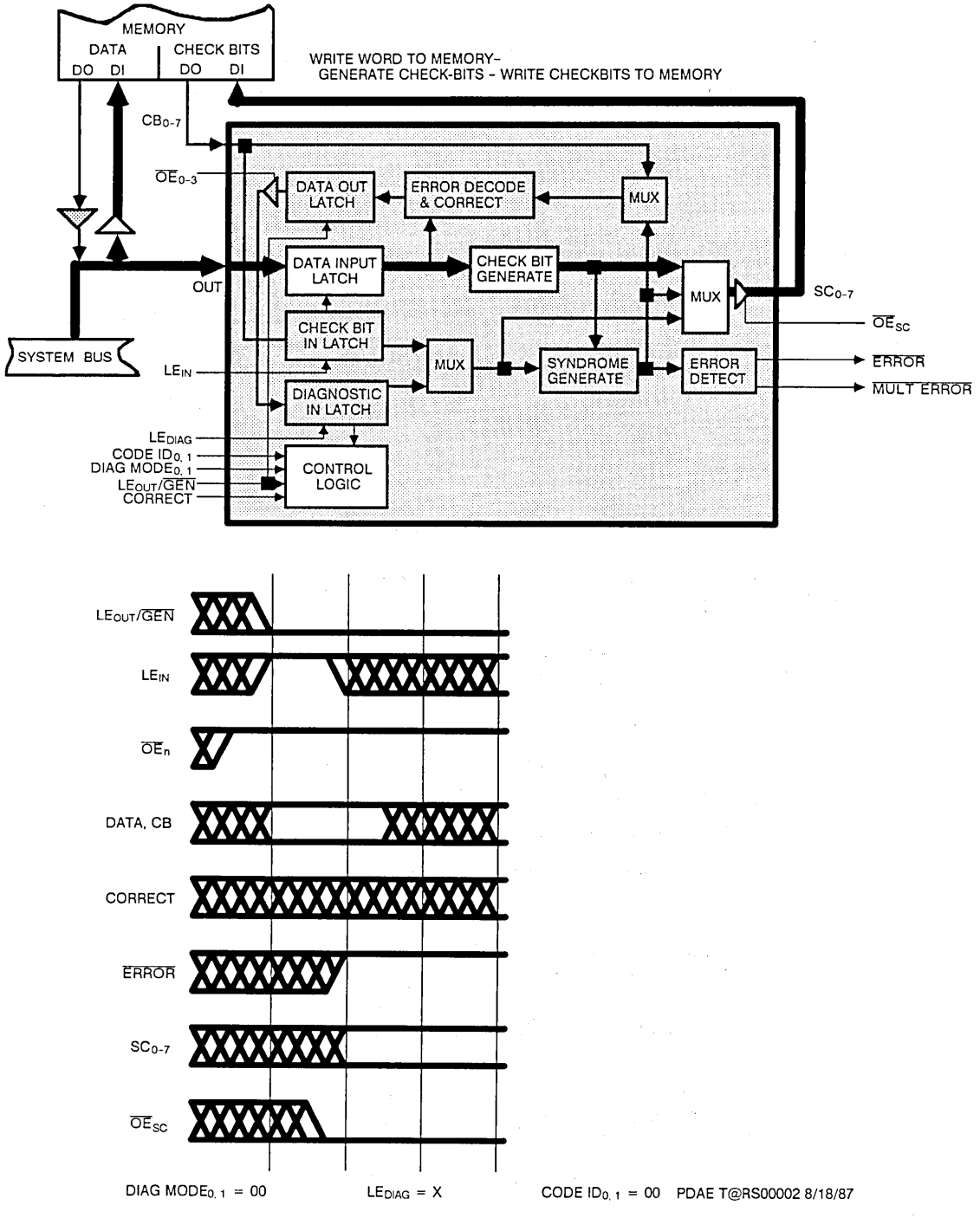


Figure 5. 32-bit full-word-width write operation (generate mode).

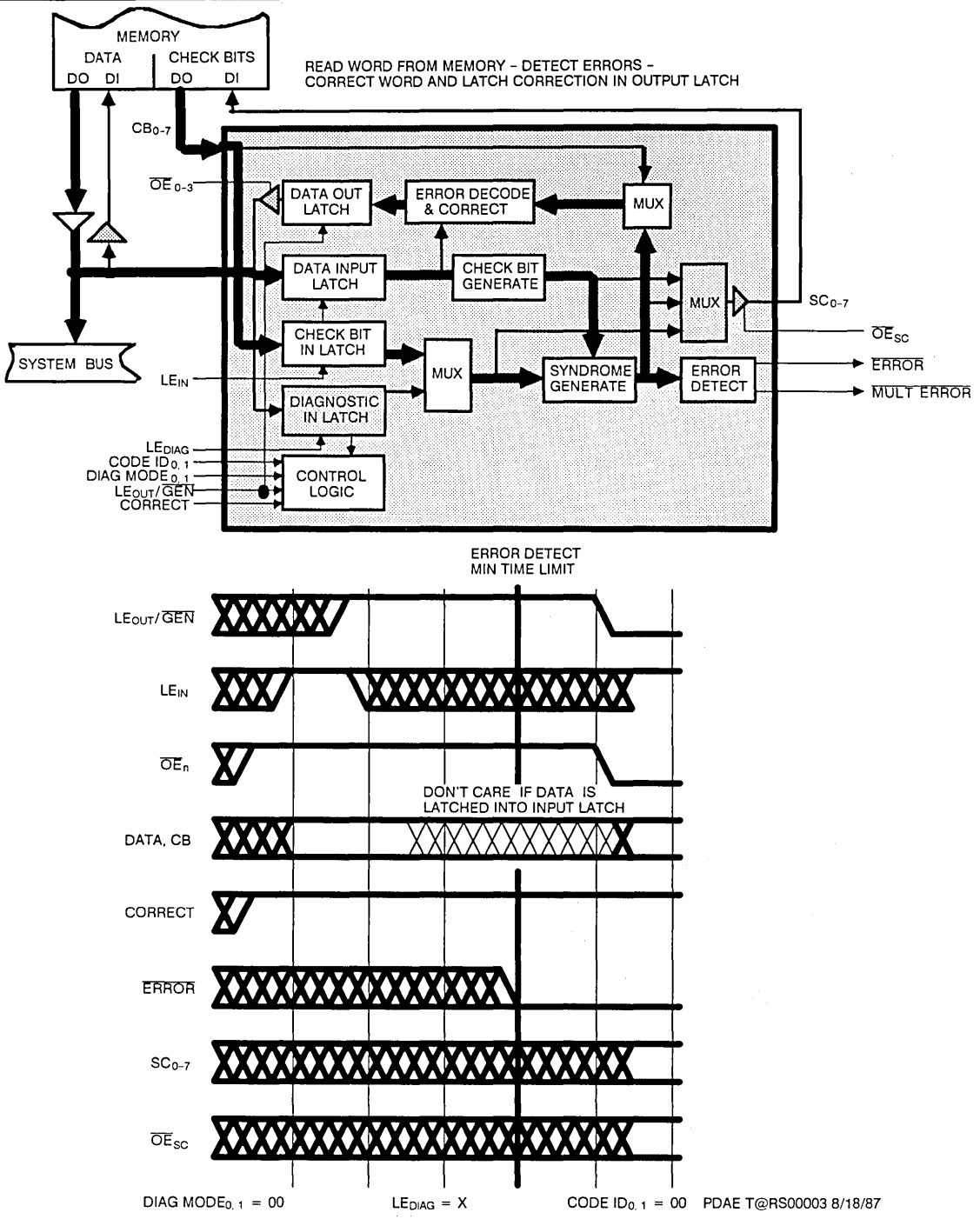
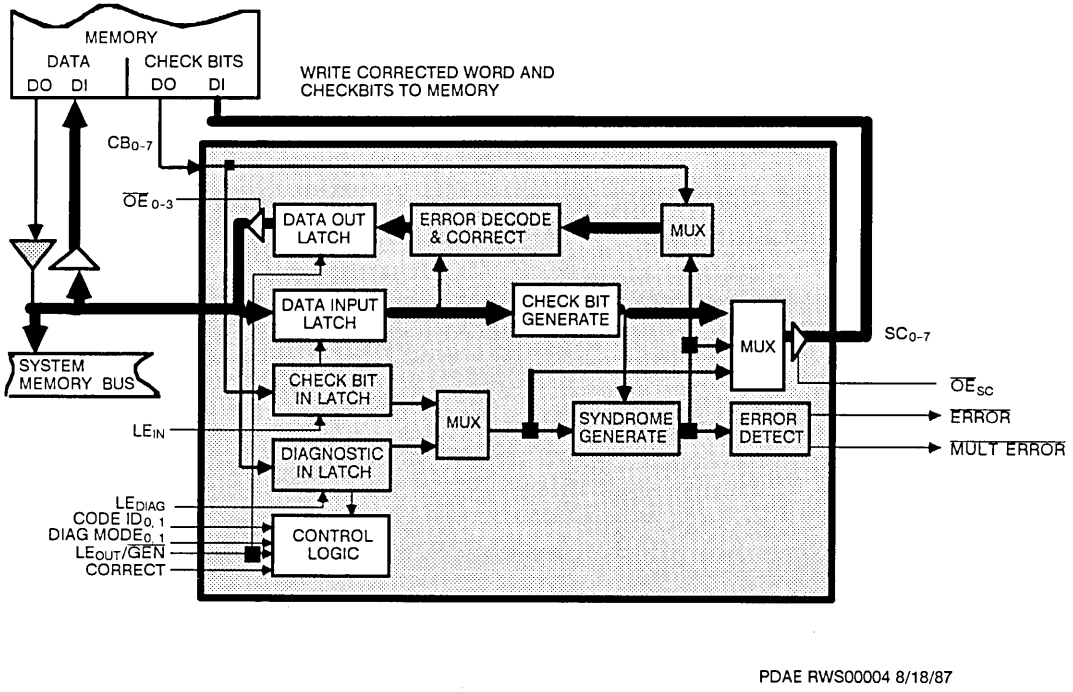


Figure 6. Memory read and error detect. Identical for read operations and the first phase of a partial-word-write operation (correct mode).



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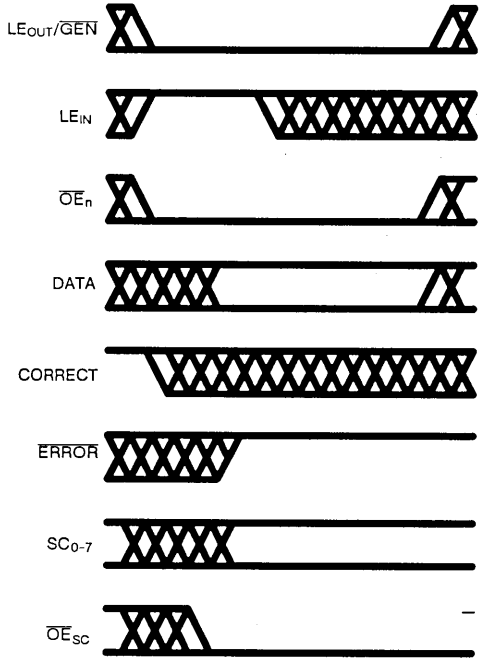

DIAG MODE0, 1 = 00 LEDIAG = X CODE ID0, 1 = 00

Figure 7. Memory correct and check-bit regenerate. Identical for the second phase of a read operation in which an error has occurred, and for a partial-word-write operation except for the state of the individual byte output enables.

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Appendix

ERROR				HEX	0	1	2	3	4	5	6	7
DECIMAL				S6	0	0	0	0	1	1	1	1
SYNDROME				S5	0	0	1	1	0	0	1	1
HEX				S4	0	1	0	1	0	1	0	1
	S3	S2	S1	S0								
0	0	0	0	0	NE	C4	C5	T	C6	T	T	30
DECIMAL EQUIVALENT> >					0	16	32	48	64	80	96	112
1	0	0	0	1	C0	T	T	14	T	M	M	T
					1	17	33	49	65	81	97	113
2	0	0	1	0	C1	T	T	M	T	2	24	T
					2	18	34	50	66	82	98	114
3	0	0	1	1	T	18	8	T	M	T	T	M
					3	19	35	51	67	83	99	115
4	0	1	0	0	C2	T	T	15	T	3	25	T
					4	20	36	52	68	84	100	116
5	0	1	0	1	T	19	9	T	M	T	T	31
					5	21	37	53	69	85	101	117
6	0	1	1	0	T	20	10	T	M	T	T	M
					6	22	38	54	70	86	102	118
7	0	1	1	1	M	T	T	M	T	4	26	T
					7	23	39	55	71	87	103	119
8	1	0	0	0	C3	T	T	M	T	5	27	T
					8	24	40	56	72	88	104	120
9	1	0	0	1	T	21	11	T	M	T	T	M
					9	25	41	57	73	89	105	121
A	1	0	1	0	T	22	12	T	1	T	T	M
					10	26	42	58	74	90	106	122
B	1	0	1	1	17	T	T	M	T	6	28	T
					11	27	43	59	75	91	107	123
C	1	1	0	0	T	23	13	T	M	T	T	M
					12	28	44	60	76	92	108	124
D	1	1	0	1	M	T	T	M	T	7	29	T
					13	29	45	61	77	93	10	125
E	1	1	1	0	16	T	T	M	T	M	M	T
					14	30	46	62	78	94	110	126
F	1	1	1	1	T	M	M	T	0	T	T	M
					15	31	47	63	79	95	111	127

NE = NO ERROR
Cn = check-bit error bit n
n = data-bit error bit n
n = decimal equivalent of the syndrome

T = Two errors
M = Multiple errors

Table 1. 32-bit Syndrome Tables with Hex, Binary and Decimal Equivalents.

ERROR				HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				S6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0	=	=	=	=	=	=	=	=	=	=	=	=	=	=	=	=
0	0	0	0	0	NE	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
					0	16	32	48	64	80	96	112	128	144	160	176	192	208	224	240
1	0	0	0	1	C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
					1	17	33	49	65	81	97	113	129	145	161	177	193	209	225	241
2	0	0	1	0	C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
					2	18	34	50	66	82	98	114	130	146	162	178	194	210	226	242
3	0	0	1	1	T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
					3	19	35	51	67	83	99	115	131	147	163	179	195	211	227	243
4	0	1	0	0	C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
					4	20	36	52	68	84	100	116	132	148	164	180	196	212	228	244
5	0	1	0	1	T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
					5	21	37	53	69	85	101	117	133	149	165	181	197	213	229	245
6	0	1	1	0	T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
					6	22	38	54	70	86	102	118	134	150	166	182	198	214	230	246
7	0	1	1	1	M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
					7	23	39	55	71	87	103	119	135	151	167	183	199	215	231	247
8	1	0	0	0	C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
					8	24	40	56	72	88	104	120	136	152	168	184	200	216	232	248
9	1	0	0	1	T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
					9	25	41	57	73	89	105	121	137	153	169	185	201	217	233	249
A	1	0	1	0	T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
					10	26	42	58	74	90	106	122	138	154	170	186	202	218	234	250
B	1	0	1	1	17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
					11	27	43	59	75	91	107	123	139	155	171	187	203	219	235	251
C	1	1	0	0	T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
					12	28	44	60	76	92	108	124	140	156	172	188	204	220	236	252
D	1	1	0	1	M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
					13	29	45	61	77	93	109	125	141	157	173	189	205	221	237	253
E	1	1	1	0	16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
					14	30	46	62	78	94	110	126	142	158	174	190	206	222	238	254
F	1	1	1	1	T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T
					15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255

NE = NO ERROR
Cn = check-bit error bit n
n = data-bit error bit n
n = decimal equivalent of the syndrome

T = Two errors
M = Multiple errors

Table 2. 64-bit Syndrome Tables with Hex, Binary and Decimal Equivalents.

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CB	DATA	CB	DATA	CB	DATA	CB	DATA
0	28	20	127	40	E	60	101
1	1000F	21	10100	41	10029	61	10126
2	10000	22	1010F	42	10026	62	10129
3	27	23	128	43	1	63	10E
4	1000C	24	10103	44	1002A	64	10125
5	2B	25	124	45	D	65	102
6	24	26	12B	46	2	66	10D
7	10003	27	1010C	47	10025	67	1012A
8	10024	28	1012B	48	10002	68	1010D
9	3	29	10C	49	25	69	12A
A	C	2A	103	4A	2A	6A	125
B	1002B	2B	10124	4B	1000D	6B	10102
C	0	2C	10F	4C	26	6C	129
D	10027	2D	10128	4D	10001	6D	1010E
E	10028	2E	10127	4E	1000E	6E	10101
F	F	2F	100	4F	29	6F	126
10	10022	30	1012D	50	10004	70	1010B
11	5	31	10A	51	23	71	12C
12	A	32	105	52	2C	72	123
13	1002D	33	10122	53	1000B	73	10104
14	6	34	109	54	20	74	12F
15	10021	35	1012E	55	10007	75	10108
16	1002E	36	10121	56	10008	76	10107
17	9	37	106	57	2F	77	120
18	2E	38	121	58	8	78	107
19	10009	39	10106	59	1002F	79	10120
1A	10006	3A	10109	5A	10020	7A	1012F
1B	21	3B	12E	5B	7	7B	108
1C	1000A	3C	10105	5C	1002C	7C	10123
1D	2D	3D	122	5D	B	7D	104
1E	22	3E	12D	5E	4	7E	10B
1F	10005	3F	1010A	5F	10023	7F	1012C

Table 3. Minimal 32-bit check-bit to data tables for diagnostic use. One data value is listed to generate every possible check-bit pattern.

DATA	CB	DATA	CB	DATA	CB	DATA	CB
0	C	100	2F	10000	2	10100	21
1	43	101	60	10001	4D	10101	6E
2	46	102	65	10002	48	10102	6B
3	9	103	2A	10003	7	10103	24
4	5E	104	7D	10004	50	10104	73
5	11	105	32	10005	1F	10105	3C
6	14	106	37	10006	1A	10106	39
7	5B	107	78	10007	55	10107	76
8	58	108	7B	10008	56	10108	75
9	17	109	34	10009	19	10109	3A
A	12	10A	31	1000A	1C	1010A	3F
B	5D	10B	7E	1000B	53	1010B	70
C	A	10C	29	1000C	4	1010C	27
D	45	10D	66	1000D	4B	1010D	68
E	40	10E	63	1000E	4E	1010E	6D
F	F	10F	2C	1000F	1	1010F	1F
20	54	120	77	10020	5A	10120	79
21	1B	121	38	10021	15	10121	36
22	1E	122	3D	10022	10	10122	33
23	51	123	72	10023	5F	10123	7C
24	6	124	25	10024	8	10124	2B
25	49	125	6A	10025	47	10125	64
26	4C	126	6F	10026	42	10126	61
27	3	127	20	10027	D	10127	2E
28	0	128	23	10028	E	10128	2D
29	4F	129	6C	10029	41	10129	62
2A	4A	12A	69	1002A	44	1012A	67
2B	5	12B	26	1002B	B	1012B	28
2C	52	12C	71	1002C	5C	1012C	7F
2D	1D	12D	3E	1002D	13	1012D	30
2E	18	12E	3B	1002E	16	1012E	35
2F	57	12F	74	1002F	59	1012F	7A

Table 4. Minimal 32-bit data to check-bit tables for diagnostic use. At least one data value is listed for every possible check-bit pattern. This table is identical to Table 3 except in sequence of presentation.

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Integrated Device Technology, Inc.

IMPLEMENTATION OF DIGITAL FILTERS USING IDT7320, IDT7210, IDT7216, AND IDT7383

APPLICATION NOTE AN-32

By Tao Lin and Dahn Le Ngoc

INTRODUCTION

Traditionally, signal processing tasks were performed with specialized analog processors. However, it is well known that digital techniques have some inherent advantages such as flexibility, accuracy, reliability over analog techniques. Moreover, because of the rapid progress in digital computer and VLSI technology, both digital processing units and storage devices are becoming less expensive year by year. Therefore, the digital approach is usually preferred over modern signal processing.

Digital filtering is one of the most important digital signal processing techniques. This technique has found many applications in a variety of areas. Perhaps the most widely known applications of digital filtering have been in the area of speech processing and communication. In many situations, speech signals are degraded in ways that limit their effectiveness for communication. In such cases digital filtering techniques are applied to improve speech quality (to remove noise or echoes from speech, etc.). Lowpass and bandpass digital filters have also been utilized in speech analysis and synthesis, speech coding, and data compression. Digital filtering techniques have also been widely used in the area of image processing: enhancement of the image to make it more acceptable to the human eye; removal of the effects of some degradation mechanism; separation of features for easier identification or measurement by human or machine. For example, we can use two-dimensional digital filters to reduce spatial low-frequency components in an X-ray image, and this process will make features with large high-frequency components such as fracture lines easier to identify.

BASIC THEORY OF DIGITAL FILTERS

General Form

A digital filter is a system or device which transforms an input sequence $\{\mu(k)\}$ into an output sequence $\{y(k)\}$. As shown in Figure 1, a digital filter is characterized by its impulse response $\{h(k)\}$ or by its transfer function H(z).

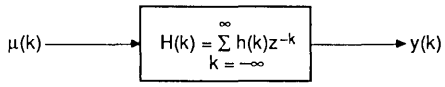

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Figure 1. Block Diagram of Digital Filter

The output sequence can be calculated from the input sequence as follows:

$$y(n) = \sum_{k=-\infty}^{\infty} h(k)\,\mu(n-k)$$

A digital filter is said to be causal or realizable if the output at $n = n_0$ is dependent only on values of the input for $n \le n_0$. This implies that the impulse response h(n) is zero for $n < 0$. The most important subset of the class of causal digital filters is that where the transfer function H(z) can be described by an Nth-order rational function

$$H(z) = \sum_{k=0}^{\infty} h(k)z^{-k} = \frac{a_0 + a_1 z^{-1} + \ldots + a_N z^{-N}}{1 - b_1 z^{-1} - \ldots - b_N z^{-N}} \qquad (2\text{–}1)$$

FIR FILTERS

A digital filter is said to be a finite impulse response (FIR) filter if the number of nonzero h(k) is finite. Otherwise, it is said to be an infinite impulse response (IIR) filter. It can be readily seen that for FIR filters, the denominator of H(z) is 1, i.e. the transfer function becomes

$$\begin{aligned} H(z) &= h(0) + h(1)z^{-1} + h(2)z^{-2} + \ldots + h(N)z^{-N} \\ &= a_0 + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_N z^{-N} \end{aligned} \qquad (2\text{–}2)$$

The output of an Nth-order FIR filter can be calculated from N+1 input data as follows:

$$y(k) = a_0\mu(k) + a_1\mu(k-1) + a_2\mu(k-2) + \ldots + a_N\mu(k-N), \quad \text{for } k = 0, 1, 2, \ldots \qquad (2\text{–}3)$$

with initial conditions: $\mu(-1) = \mu(-2) = \ldots = \mu(-N) = 0$. Therefore, FIR filters nonrecursive and can be implemented by using adders, multipliers and delay elements without a feedback path. The canonical form of an FIR filter is illustrated in Figure 2.

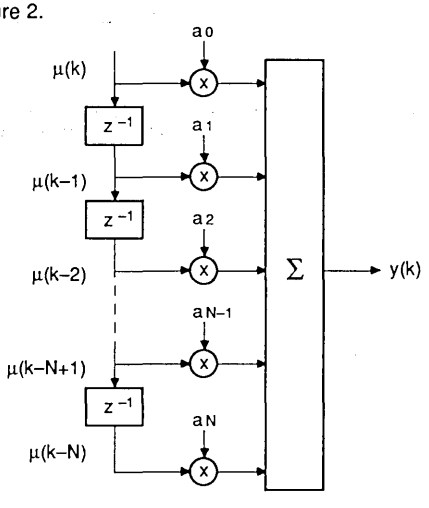

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Figure 2. Block Diagram of Canonical FIR Filter

IIR Filters

On the other hand, IIR filters are recursive, i.e., the output of an IIR filters is calculated from both input data and previous output data as follows:

$$y(k) = b_1y(k-1) + b_2y(k-2) + ... + b_Ny(k-N) + a_0\mu(k) + a_1\mu(k-1) + a_2\mu(k-2) + ... + a_N\mu(k-N), \quad \text{for } k = 0, 1, 2, ... \qquad (2-4)$$

with initial conditions: $\mu(-1) = \mu(-2) = ... = \mu(-N) = 0$. The canonical form of IIR filters is shown in Figure 3.

While FIR filters have the advantages of being unconditionally stable, less sensitive to quantization error and linear phase, IIR filters have lower order than FIR filters with equivalent performance. Therefore, IIR filters require less memory and fewer arithmetic operations than FIR filters.

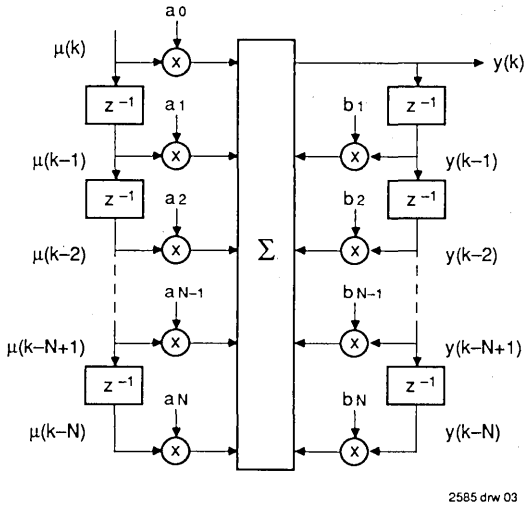

Figure 3. Block Diagram of Canonical IIR Filter

In this application note, we will discuss various implementations of both FIR and IIR filters using the IDT 16–bit DSP building block family: IDT7320, 16–bit 8–level pipeline register; IDT7210, 16x16–bit multiplier–accumulator; IDT7216 16x16–bit multiplier and IDT7383, 16–bit ALU.

IMPLEMENTATIONS OF FIR FILTERS

There are many FIR filter structures. Two particular structures are universally utilized: the transversal structure and the lattice structure.

Transversal Structure

The transversal structure is a rather direct realization of the equation (2–3) in terms of delays, multiplications, and additions. As shown in Figure 4 for a 7th–order (8-tap) filter, the output y(k) of the transversal structure is simply the weighted sum of the current input μ(k) and the delayed inputs μ(k–1), μ(k–2). The coefficient a_0, a_1, ... determine the frequency response of a particular filter such as lowpass, bandpass or highpass.

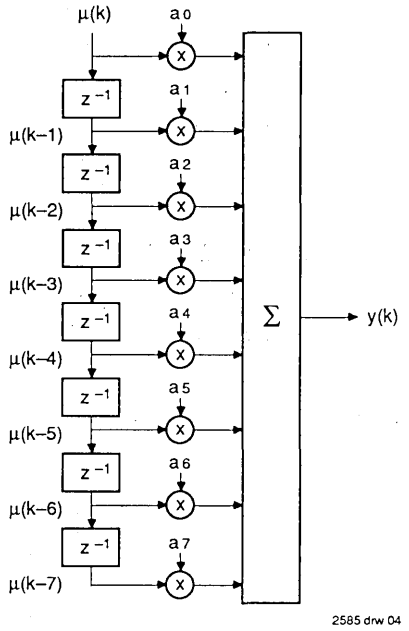

Figure 4. 8–Tap Transversal Structure

Figure 5 illustrates the implementation of the 8-tap transversal structure using two IDT7320s and an IDT7210. One IDT7320 is for the storage of input data, and the other for the storage of filter coefficients. The IDT7210 is used to perform multiplication and accumulation. Registers REG G_1 and REG H_2 of the IDT7320s are connected to X and Y input registers of the IDT7210, respectively. Both IDT7320s are shifted every clock cycle. Thus, the input data and the coefficients are loaded into the input registers of the IDT7210 in the sequence shown in Figure 6. In the first clock cycle, a new input word is loaded into REG A_1 and the pipeline registers A_1–G_1 shift down. In the next seven clock cycles, the output of REG G_1 is connected to the input of REG A_1, so that the pipeline registers A_1–G_1 shift as a ring every clock cycle. Similarly, the output of REG H_2 is connected to the input of REG A_2. A new output is unloaded every eight clock cycles. A sequence controller generates the clock and the control signals SEL and ACC. The filter coefficients are preloaded into the pipeline registers A_2–H_2. Generally, for an N-tap transversal structure, a filter cycle has N clock cycles. Therefore, a filter cycle time is NST_{MA}, where t_{MA} = 25ns is the multiply–accumulate time of IDT7210.

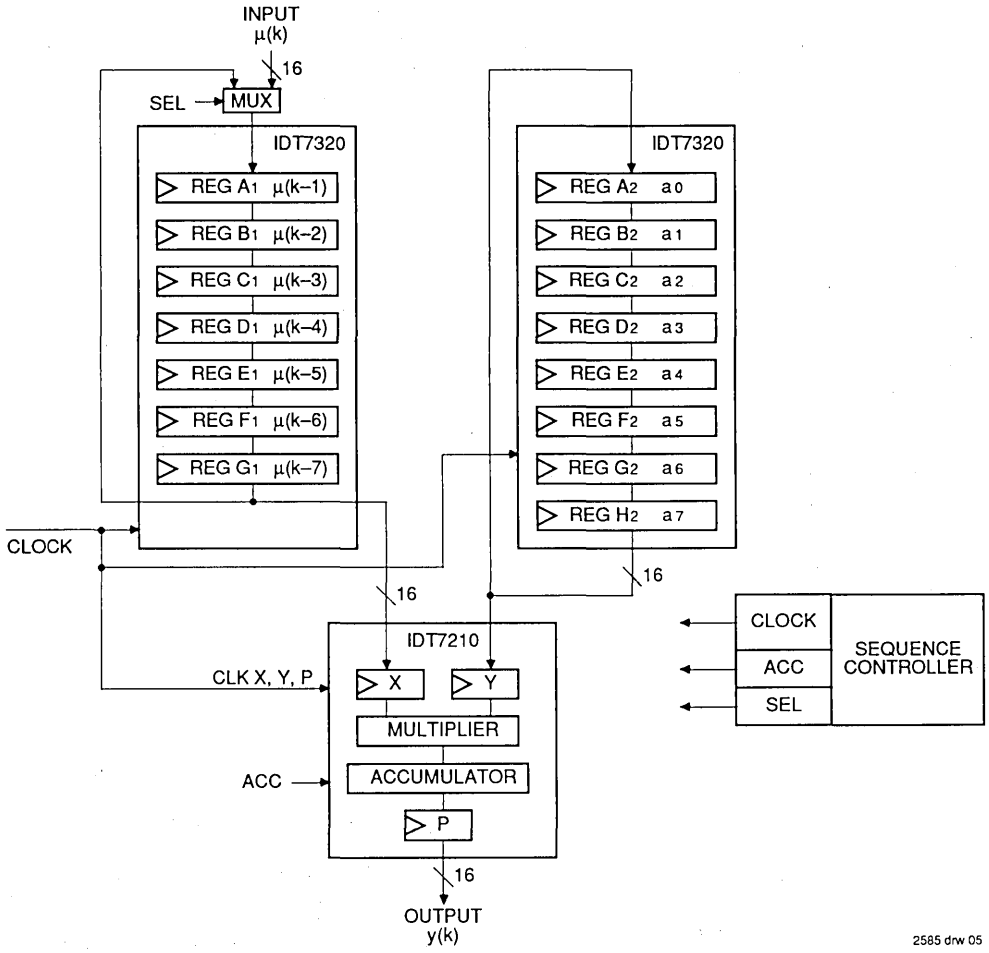

Figure 5. Implementation of the Transversal Structure Using IDT7320s and IDT7210

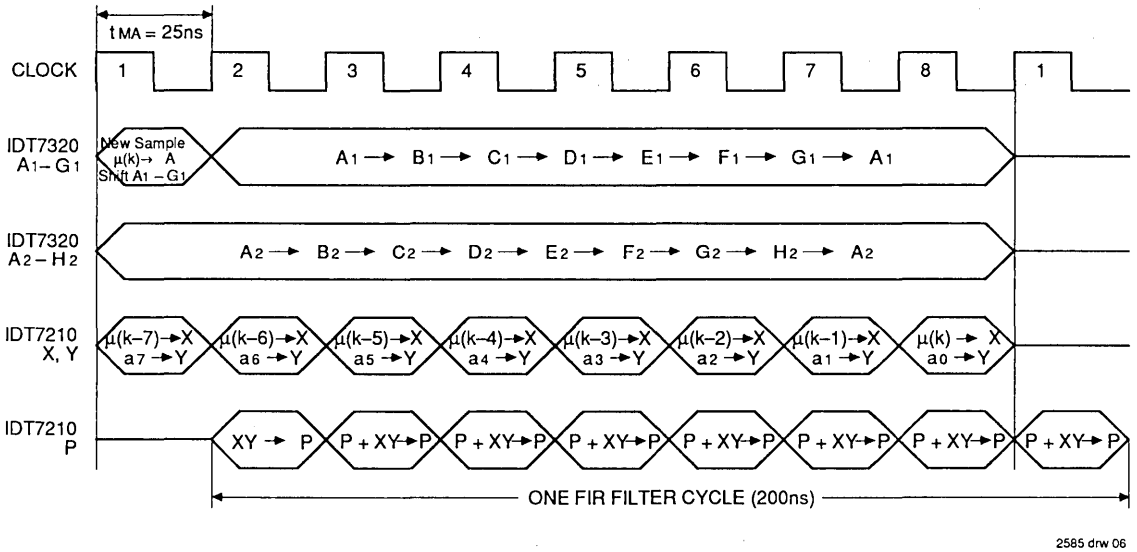

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Figure 6. Operation Sequence of IDT7320s and IDT7210 for the Transversal Structure

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Lattice Structure

The lattice structure of an Nth-order FIR filter shown in Figure 7 for n = 8. The lattice structure is equivalent to the transversal structure, in the sense that any transfer function which can be represented by the transversal structure can also be represented within a multiplicative constant by the lattice structure. The origin and utility of the structure is that it has several advantages over the transversal structure in the field of adaptive filtering.

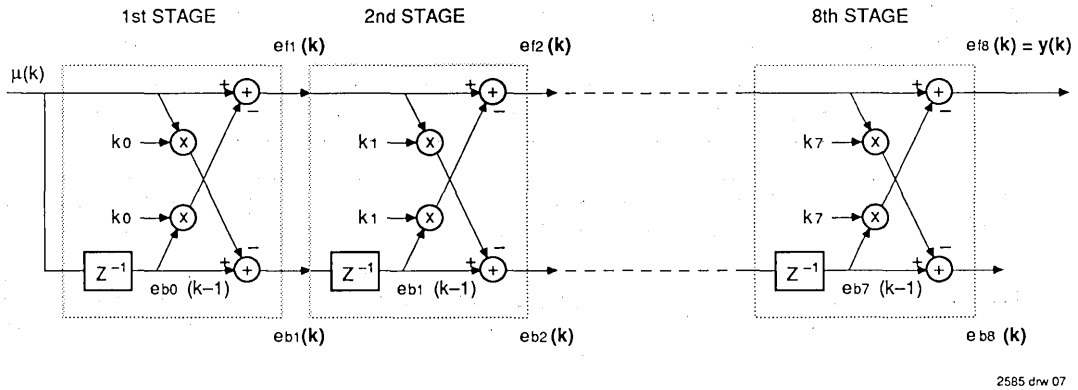

Figure 7. Block Diagram of the Lattice Structure

From Figure 7, we can see that an Nth-order lattice structure consists of N stages, each having two inputs and two outputs. The outputs {$e_{fm}(k)$, k = 0, 1, 2, ...} and {$e_{bm}(k)$, k = 0, 1, 2, ...} of the mth (1mN) stage are called mth-order forward and backward prediction errors, respectively, which are related to the inputs of the stage (the outputs of the previous stage) as follows:

$$e_{fm}(k) = e_{f(m-1)}(k) - k_{m-1}\, e_{b(m-1)}(k-1) \quad (3\text{–}1a)$$
$$e_{bm}(k) = e_{b(m-1)}(k-1) - k_{m-1}\, e_{f(m-1)}(k) \quad (3\text{–}1b)$$

where the input of the first stage is

$$e_{f0}(k) = e_{b0}(k) = \mu(k) \quad (3\text{–}1c)$$

Equation (3–1) shows that we need to store {$e_{b0}(k-1)$, $e_{b1}(k-1)$, ... , $e_{b(N-1)}(k-1)$}, the backward prediction errors at time k–1, for calculating the outputs of all stages at time k: {$e_{b1}(k)$, $e_{f1}(k)$, $e_{b2}(k)$, $e_{f2}(k)$, ... , $e_{bN}(k)$, $e_{fN}(k)$}. An implementation of the 8-stage lattice structure is given in Figure 8 using IDT7320s, 7216s, and 7383s. Two IDT7320s store the previous outputs $e_{b0}(k-1)$, $e_{b1}(k-1)$, ... , $e_{b7}(k-1)$ and the coefficients k_0, k_1, ..., k_7. The multiplications of

$$k_{m-1}\, e_{b(m-1)}(k-1) \text{ and } k_{m-1}\, e_{f(m-1)}(k)$$

are performed by two IDT7216s. Two IDT7383s execute the subtractions

$$e_{f(m-1)}(k) - k_{m-1}\, e_{b(m-1)}(k-1) \text{ and } e_{b(m-1)}(k-1) - k_{m-1} e_{f(m-1)}(k).$$

The sequence of the operations is shown in Figure 9. A filter cycle consists of 8 clock cycles. In the first clock cycle, $e_{b0}(k-1) = \mu(k-1)$ stored in REG H_1 is loaded into registers X_1 and R_1; k_0 stored in REG H_2 is loaded into registers Y_1 and Y_2; and the new input $\mu(k) = e_{f0}(k)$ is loaded into registers X_2 and R_2. The new input $\mu(k) = e_{b0}(k)$ is also loaded into REG H_1. After a time delay of t_{MUC} = 30ns, the results of multiplication appear at the output pins of the IDT7216s which are directly connected to the input of the ALU of the IDT7383s. Then, after another time delay of t_{ALU} = 25ns, we obtain the outputs of the first stage, $e_{b1}(k)$ and $e_{f1}(k)$, at the output pins of the IDT7383s. In the second clock cycle, $e_{b1}(k-1)$ stored in REG G_1, k_1 stored in REG G_2, and $e_{f1}(k)$ appeared at the output port of the IDT7383 are loaded into corresponding input registers of the IDT7216s and 7383s. At the same time, $e_{b1}(k)$ is loaded into REG G_1. After a time delay of $t_{MUC} + t_{ALU}$ = 55ns, we obtain $e_{b2}(k)$ and $e_{f2}(k)$, at the output pins of the IDT7383s, and so on. Finally, in the eighth cycle, we obtain $e_{b8}(k)$ and $y(k) = e_{f8}(k)$. It should be noted that in each clock cycle, the IDT7216s first perform the multiplication, then the IDT7383s complete the subtraction. Therefore, the time of a clock cycle is $t_C = t_{MUC} + t_{ALU}$ = 55ns. For an Nth-order lattice FIR filter, the filter cycle time is 55 x N nanoseconds (440ns for N = 8).

The signals I_{0-3} control to which register of the IDT7320 a new backward prediction error will be written. The signals SEL_{0-2} select one of the eight registers of the IDT7320s to be read from the output port. A sequence controller is needed to generate the clock and the control signals I_{0-3} and SEL_{0-3}. The filter coefficients k_0–k_7 are preloaded into the registers A_2–H_2.

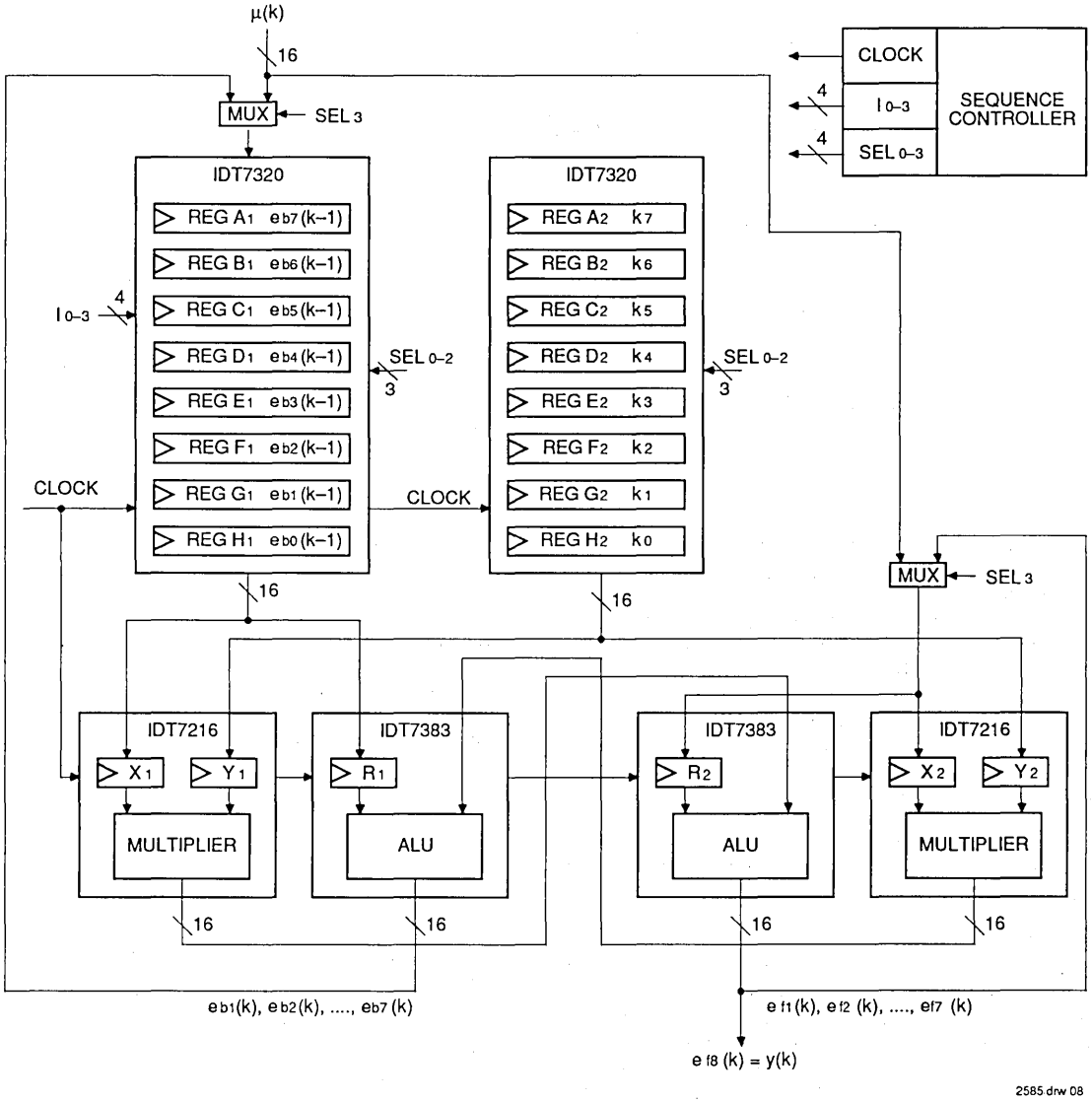

Figure 8. Implementation of the Lattice Structure Using IDT7320s, IDT7216s and IDT7383s

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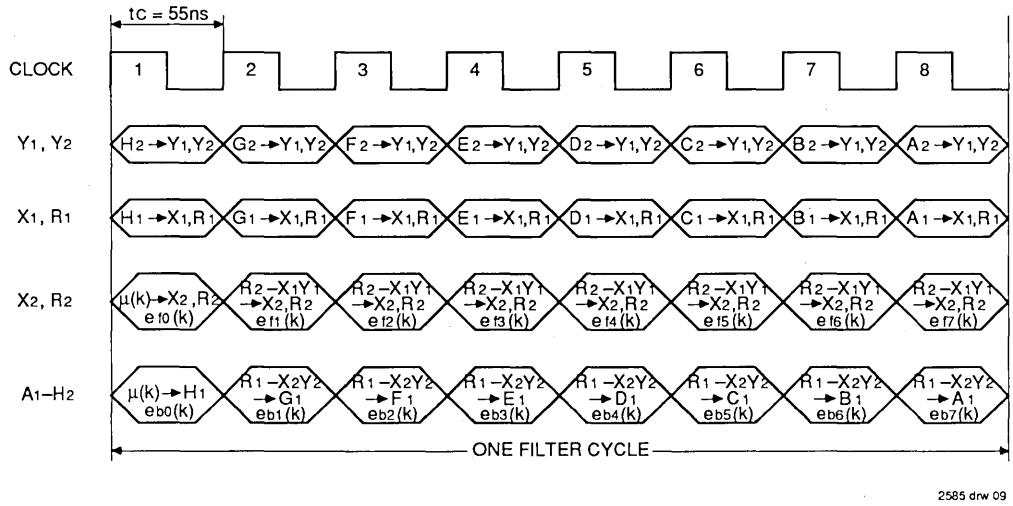

Figure 9. Operation Sequence of IDT7320s, IDT7216s and IDT7383s for the Lattice Structure

IMPLEMENTATIONS OF IIR FILTERS

Since IIR filters have feedback elements, architecture for implementing IIR filters are more complex than those for filters. Moreover, roundoff errors of multiplication may accumulate and be amplified through the feedback loop so that the roundoff noise at the filter output becomes a serious problem. However, IDT's flexible and high-precision DSP product lines provide unique solution for implementing IIR filters.

There are a variety of structures to implement IIR filters, such as direct form structure, cascade structure, parallel structure, lattice structure, ladder structure, state-space structure. Among these, direct form, parallel and cascade structures are popular in many applications. In the following, we will consider how to implement these filter structures using the IDT7320, 7210, and 7383.

Direct Form Structure

The direct form structure is the simplest implementation of IIR filters and requires the fewest multiplication, addition and delay elements. This means that it can achieve higher speed and needs less hardware than other structures. The disadvantage of the direct form structure is that it may have multiplication roundoff noise. This can be overcome by using the IDT high-precision 16-bit multiplier–accumulator (MAC), where the whole 32-bit product is preserved and used in the accumulator.

Let U(z) and Y(z) be the z-transforms of the input {μ(k)} and the output {y(k)}, respectively, then an IIR filter is described by

$$Y(z) = H(z)\,U(z) = \frac{a_0 + a_1 z^{-1} + \ldots + a_N z^{-N}}{1 - b_1 z^{-1} - \ldots - b_N z^{-N}} U(z) = \frac{A(z)}{B(z)} U(z). \quad (4\text{–}1)$$

Define $W(z) = \frac{1}{B(z)} U(z)$, we obtain

$$W(z)B(z) = U(z) \text{ and } Y(z) = A(z)W(z). \quad (4\text{–}2)$$

Equation (4–2) can be written in the time domain as

$$w(k) = \mu(k) + b_1 w(k-1) + b_2 w(k-2) + \ldots + b_N w(k-N) \quad (4\text{–}3a)$$

and

$$y(k) = a_0 w(k) + a_1 w(k-1) + a_2 w(k-2) + \ldots + a_N w(k-N) \quad (4\text{–}3b)$$

From (4–3), we get the direct form structure of the IIR filter as shown in Figure 10. The direct form structure can be implemented using a single MAC or two MACs.

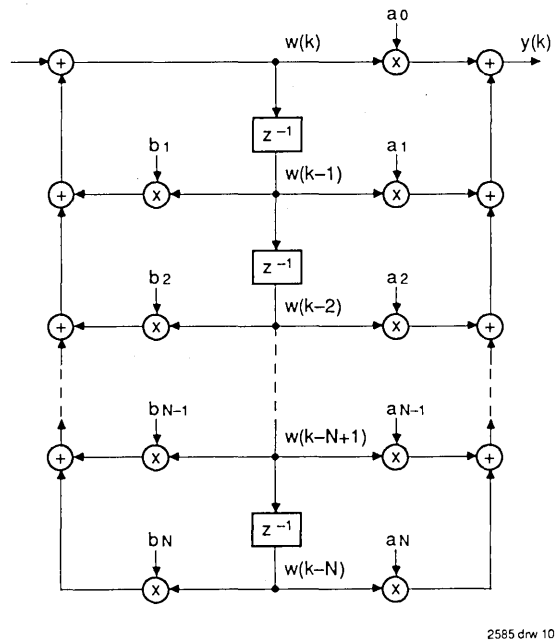

Figure 10. Block Diagram of the Direct Form Structure

Implementation Using A Single MAC

Using a single MAC, for each new input μ(k), we first calculate w(k) given by (4–3a), and then calculate y(k) by (4–3b). The implementation of a 7th-order filter is shown in Figure 11. Three IDT7320s are used to store {w(k)}, the coefficients {$b_1, b_2, ..., b_7, 1$} and the coefficients {$a_0, a_1, ..., a_6, a_7$}. The new input μ(k) and the data {w(k)} stored in the IDT7320 are sent to X input port of the IDT7210 through a multiplexer, while the coefficients {$a_0, a_1, ..., a_6, a_7$} are sent to Y input port of the IDT7210 through another multiplexer.

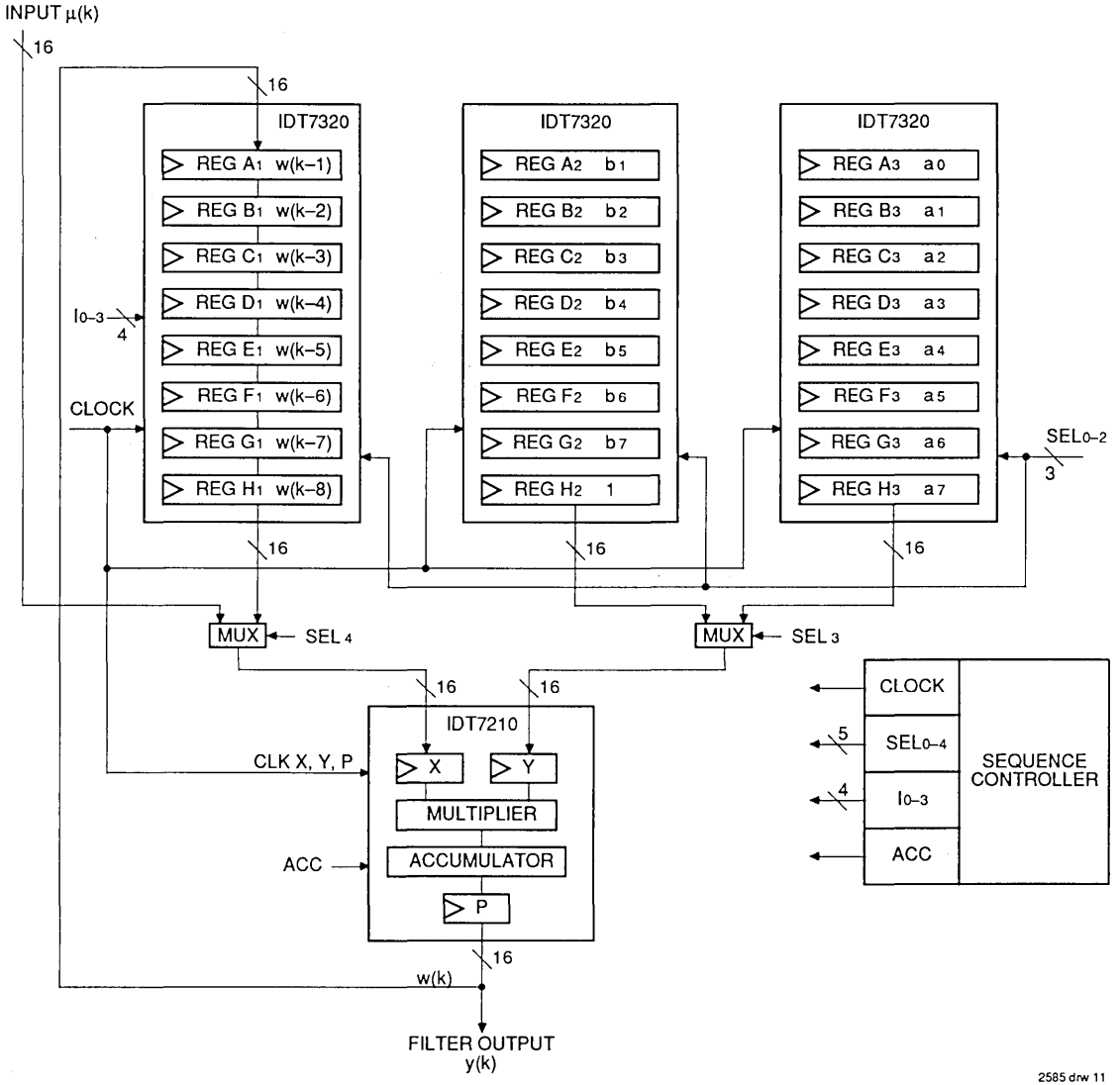

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Figure 11. Direct Implementation of IIR Filter Using a Single MAC

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As shown in Figure 12, each filter cycle consists of 16 clock cycles. The first eight clock cycles calculate w(k) while the last eight clock cycles calculate y(k). In the first clock cycle, the new input μ(k) and the content of REG H_2 are loaded into the input registers of the IDT7210. Since 1 is stored in REG H_2, the result obtained in the output register of the IDT7210 is μ(k). In the second clock cycle, the contents of REG G_1 and REG G_2 are sent to the input registers of the IDT7210, and so on. Then, in the ninth clock cycle, w(k) is obtained in the output register of the IDT7210. In the tenth cycle, we load w(k) into REG A_1 which will be used in the sixteenth cycle. Before w(k) is loaded, in the eighth cycle, we shift down the pipeline registers A_1–H_1, so that in the ninth cycle, the data stored in H_1 is not w(k–8) but w(k–7) which is multiplied by a_7 stored in REG H_3. A new output y(k) is obtained in the first clock cycle of the next filter cycle. It should be noted that in this implementation, we obtain different data at the output ports of the IDT7320s by using the output selection signal SEL_{0-2}, not by shifting the pipeline registers every clock cycle.

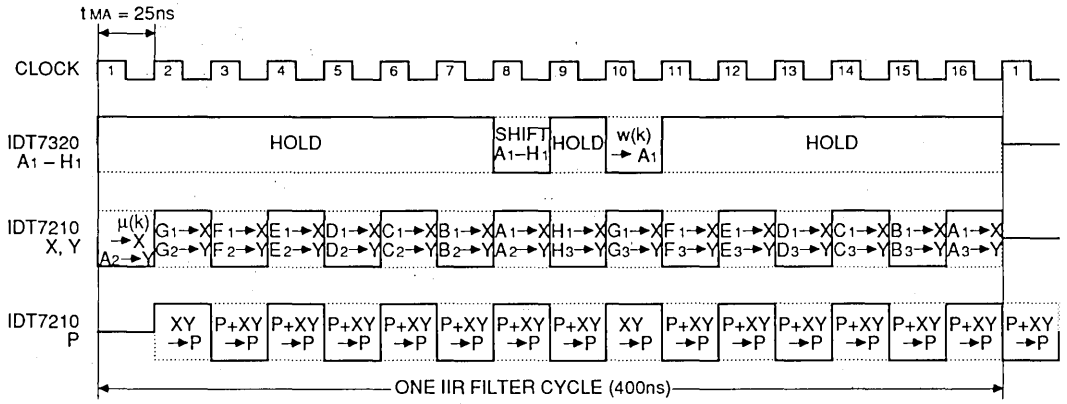

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Figure 12. Sequence of Operations of IDT7320s and IDT7210 for the Direct Form Implementation Using a Single MAC

Implementation Using Two MACs

In the implementation mentioned above, we use a single MAC to calculate w(k) and y(k) alternately. If we use two MACs, one MAC for calculating y(k) given by

$$y(k) = a_0w(k)+a_1w(k-1)+a_2w(k-2)+...+a_Nw(k-N) \quad (4-4a)$$

and another MAC for simultaneously calculating w(k+1) given by

$$w(k+1) = \mu(k+1)+b_1w(k)+b_2w(k-1)+...+b_Nw(k-N+1) \quad (4-4b)$$

then the processing speed can be doubled. The implementation of a 7th-order filter using two IDT7210s is shown in Figure 13.

A filter cycle has 8 clock cycles as shown in Figure 14. In the first cycle, $\mu(k+1)$ is loaded into register X, and multiplied by the content of REG H_2 which is one, so that the result in the output register P_1 is still $\mu(k+1)$. In the next seven cycles, w(k–6), w(k–5), ..., w(k) are loaded into register X_1 through the multiplexer and multiplied by b_7, b_6, ..., b_1, respectively. In the eighth cycle, we shift down the pipeline registers A_1–H_1 to prepare for the next filter cycle. Then, in the first clock cycle of the next filter cycle, we obtain w(k+1) in the output register P_1 which is loaded into REG A_1 in the second clock cycle. When one IDT7210 calculates w(k+1), another IDT7210 calculates y(k) and an output is unloaded from register P_2 every 8 clock cycles.

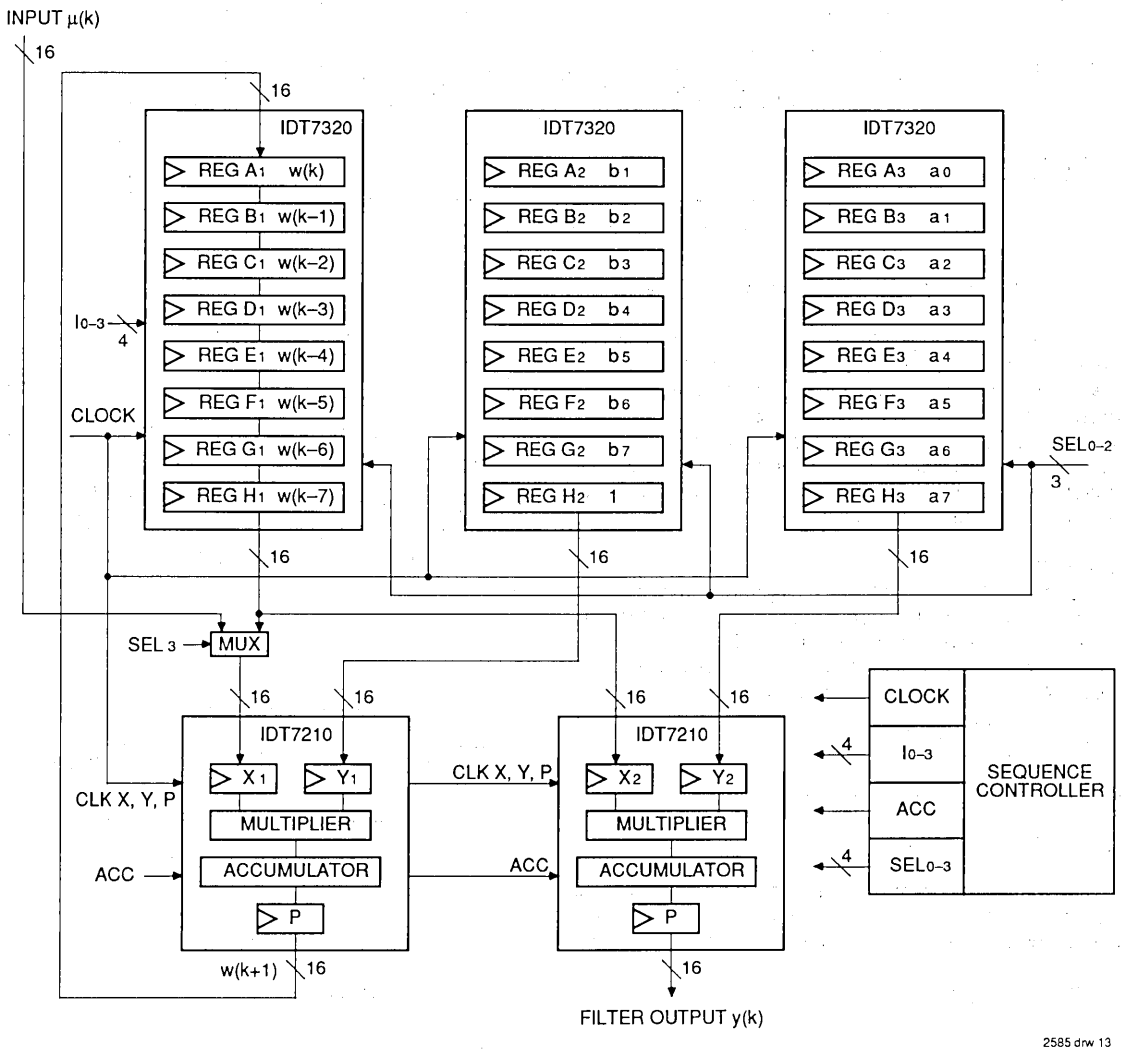

Figure 13. Direct Form Implementation of IIR Filter Using Two MACs

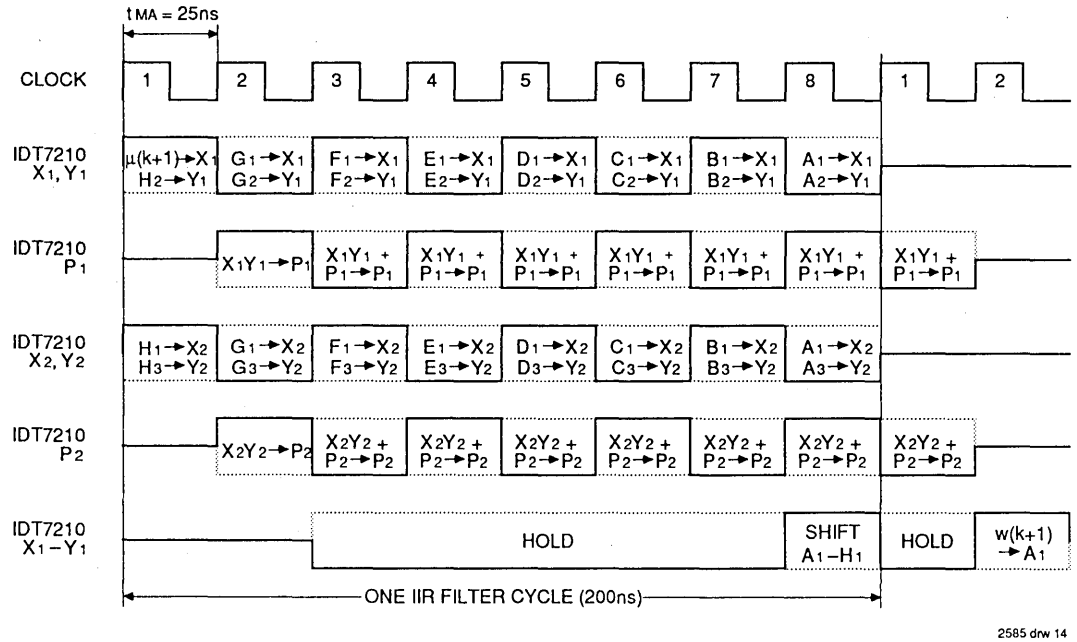

Figure 14. Sequence of Operations of IDT7320s and IDT7210 for the Direct Form Implementation Using Two MACs

Whether using a single MAC or two MACs, the signals I0–3 control whether or not the pipeline registers shift or hold and to which register of the IDT7320 a new result w(k) will be written. On the other hand, the signals SEL0–2 select one of the eight registers of the IDT7320s to be read from the output port. A sequence controller generates the clock and the control signals. The filter coefficients are preloaded into IDT7320s as in the FIR filter case.

Parallel Structure

The parallel structure has the advantage of less multiplication roundoff noise and coefficient quantization sensitivity than the direct form structure. However, the parallel structure uses more hardware. The basic principle of the parallel structure is that an Nth-order rational transfer function

$$H(z) = \frac{a_0 + a_1 z^{-1} + \ldots + a_N z^{-N}}{1 + b_1 z^{-1} + \ldots + b_N z^{-N}} \qquad (4\text{–}5)$$

can be expanded to partial fraction as follow

$$H(z) = H_1(z) + \ldots + H_M(z) \qquad (4\text{–}6)$$

The expansion suggests that the filter could be implemented in a parallel structure shown in Figure 15. To minimize the roundoff noise and coefficient sensitivity, $H_i(z)$ is usually a first-order filter or a second-order filter

$$H_i(z) = \frac{a_0 + a_1 z^{-1}}{1 + b_1 z^{-1}} \qquad (4\text{–}7)$$

$$H_i(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}} \qquad (4\text{–}8)$$

which can be implemented by the direct form structure mentioned before. For example, a fourth-order filter can be implemented with two parallel sections, each being a second-order filter, as shown in Figure 16. In this particular implementation, each section uses two MACs. The outputs of two sections are added by the IDT7383 to obtain the filter output {y(k)}.

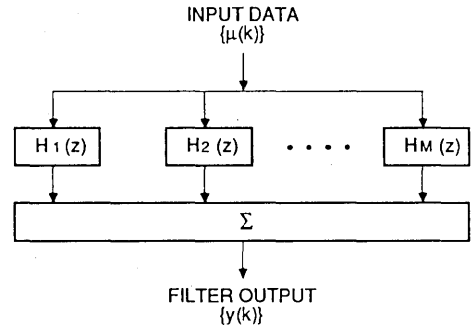

Figure 15. Parallel Structure of IIR Filters

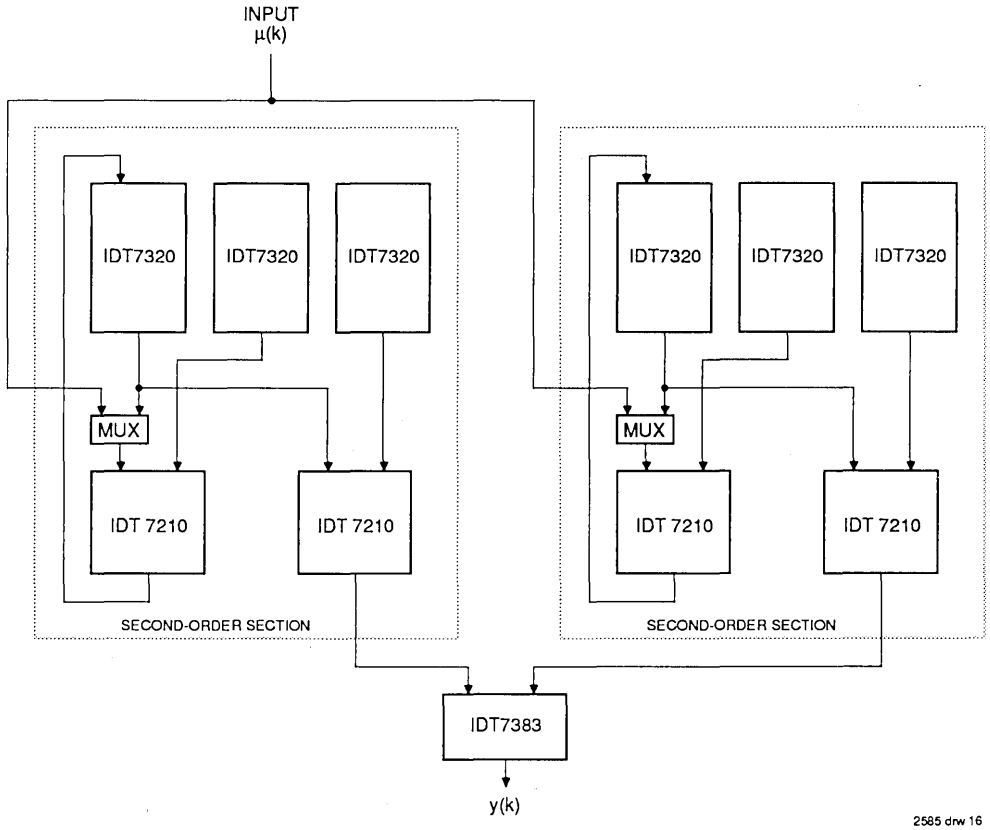

Figure 16. Parallel Implementation of a Fourth–Order Filter Using Two Second–Order Sections

Cascade Structure

Like the parallel structure, the cascade structure has the advantage of less multiplication roundoff noise and coefficient quantization sensitivity and the disadvantage of more hardware than the direct form structure. The basic principle of the cascade structure is to decompose an Nth-order rational transfer function given by (4–5) into first-order or second-order sections as follows:

$$H(z) = H_1(z)S \ldots S H_M(z) \qquad (4\text{–}9)$$

where $H_i(z)$ is given by (4–7) or (4–8). From the decomposition, the filter of (4–5) can be implemented by the direct form structure. For example, a fourth-order filter can be implemented with two cascade sections, each being a second-order filter, as shown in Figure 18. The output of the first section is the input of the second section.

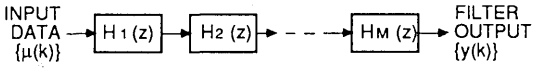

Figure 17. Cascade Structure of IIR Filters

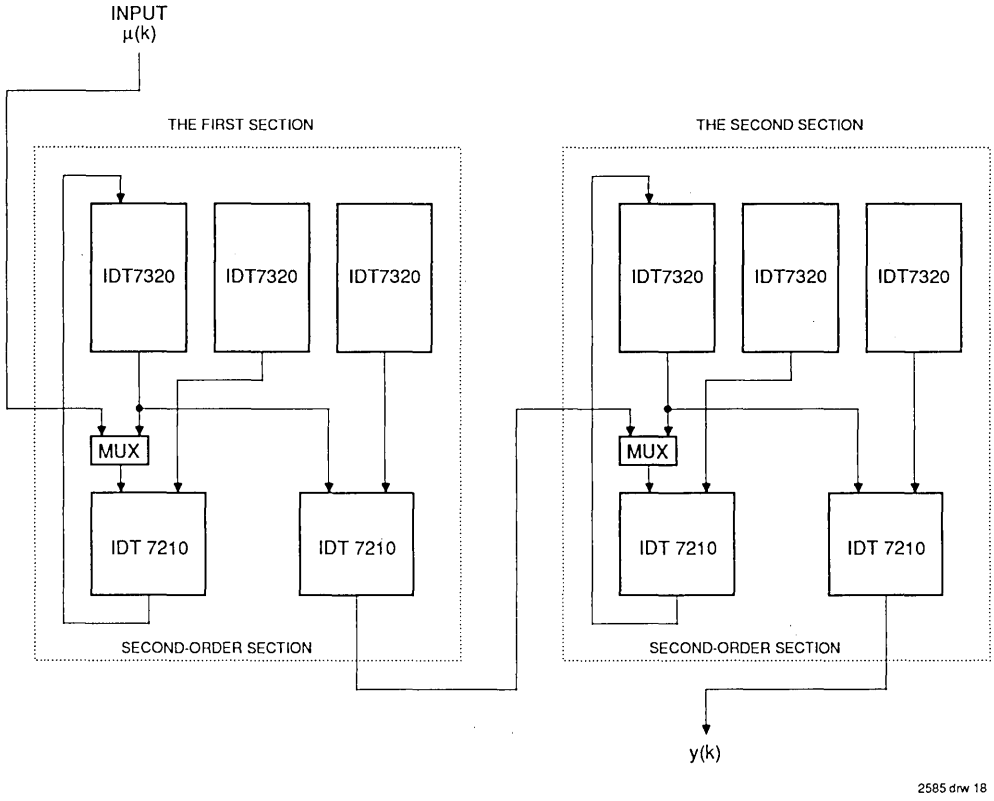

Figure 18. Cascade Implementation of a Fourth–Order Filter Using Two Second–Order Sections

CONCLUSIONS

In this application note, we have discussed the basic methods to implement a variety of structures of both FIR and IIR filters using IDT DSP building block family: pipeline registers, MACs, multipliers, and ALUs. Which structure and implementation should be selected in a particular application is decided by many factors such as the available filter design tools, cost, speed, etc.. In many applications, the FIR transversal structures is used because of the simplicity of filter design and implementation. The FIR lattice structure is employed in the application where the filter coefficients have to be adaptively changed and fast convergency of the coefficients is required. In applications requiring high speed and compact hardware, IIR filters are usually preferred. Different IIR filter structures may have completely different finite wordlength effects (roundoff error, coefficient error and limit cycles). The direct form structure is the simplest one and uses the least hardware. However, if the filter order is large and the bandwidth of the filter is very narrow, then the direct form structure may have severe roundoff noise and limit-cycles so that the actual input-output characteristic of the filter dramatically deviates from the ideal one. In this situation, parallel structure or cascade structure should be utilized.

The building block approach discussed in this application note can achieve 10 times the performance of some simple FIR and IIR filter structures. Table 1 gives a comparison between the building block approach using IDT's DSP building blocks and the single chip DSP approach using the latest Texas Instruments TMS320C25–50, a single chip digital signal processor with an instruction cycle time of 80ns.

IDT's extensive and flexible product lines provide various possibilities to implement different filter structures. In the FIR filter implementations and IIR filter direct form implementations shown in this application note, we have using at most two MACs, multipliers and ALUs. The number of the clock cycles in a filter cycle is proportional to the filter order. If more MACs, multipliers and ALUs are used, a filter cycle can contain only a single clock cycle to achieve the highest speed.

Integrated Device Technology, Inc.

ADDRESS GENERATOR FOR A MATRIX MANIPULATION ENGINE

APPLICATION NOTE AN-35

By Yuping Chung

INTRODUCTION

An address generator is essential in every system requiring access to both the programming code and data. In a microprocessor–based system, the address generator is already built–in on the microprocessor chip. Other high performance systems use dedicated address generators to achieve a high degree of parallelism. The address generator must be fast and flexible to cope with the system's different addressing requirements, such as random addressing and structured data addressing. A loadable up/down counter can be used as an address generator, but it is limited to access the adjacent locations. A better solution is an ALU based address generator which can access the address in several modes: sequential accessing, interval accessing, segmented addressing, and indexed addressing. These flexible accessing modes are especially useful in systems with structured data, such as matrices. The following sections discuss a high speed matrix manipulation engine incorporates its own ALU–based addressing generators.

Digital signal processing, array processing and scientific computing systems require matrix operations. An example shown in Figure 1 is the matrix multiplication. Most often, the data of each matrix are stored sequentially in a buffer. However, the matrix operation requires accessing the memory both sequentially and non–sequentially. We will examine the memory organization of the matrix first and subsequently examine the matrix manipulation engine.

$$\begin{pmatrix} a_{11} & a_{12} & \cdots & a_{1j} \\ a_{21} & \ddots & & \\ \vdots & & & \\ a_{i1} & & & a_{ij} \end{pmatrix} \times \begin{pmatrix} b_{11} & b_{12} & \cdots & b_{1k} \\ b_{21} & \ddots & & \\ \vdots & & & \\ b_{j1} & & & b_{jk} \end{pmatrix} = \begin{pmatrix} c_{11} & c_{12} & \cdots & c_{1k} \\ c_{21} & \ddots & & \\ \vdots & & & \\ c_{i1} & & & c_{ik} \end{pmatrix}$$

$$c_{ik} = \sum_{j=1}^{j} a_{ij}\, b_{jk} \qquad \begin{matrix} i = 1, 2, \ldots, i \\ j = 1, 2, \ldots, j \\ k = 1, 2, \ldots, k \end{matrix}$$

$$\begin{pmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \end{pmatrix} \times \begin{pmatrix} b_{11} & b_{12} & b_{13} & b_{14} \\ b_{21} & b_{22} & b_{23} & b_{24} \\ b_{31} & b_{32} & b_{33} & b_{34} \end{pmatrix} = \begin{pmatrix} c_{11} & c_{12} & c_{13} & c_{14} \\ c_{21} & c_{22} & c_{23} & c_{24} \end{pmatrix}$$

$$c_{11} = a_{11}b_{11} + a_{12}b_{12} + a_{13}b_{13}$$

2586 drw 01

Figure 1. Matrix Multiplication and its Unit Operation

7

MATRIX MEMORY ORGANIZATION AND ADDRESSING

Sequential Memory Organization

In most applications the entries each matrix are stored linearly row by row in a dedicated memory segment, as illustrated in Figure 2. In applications such as spectrum analysis, image processing, and graphics engine, the segment size may be as large as several thousand words.

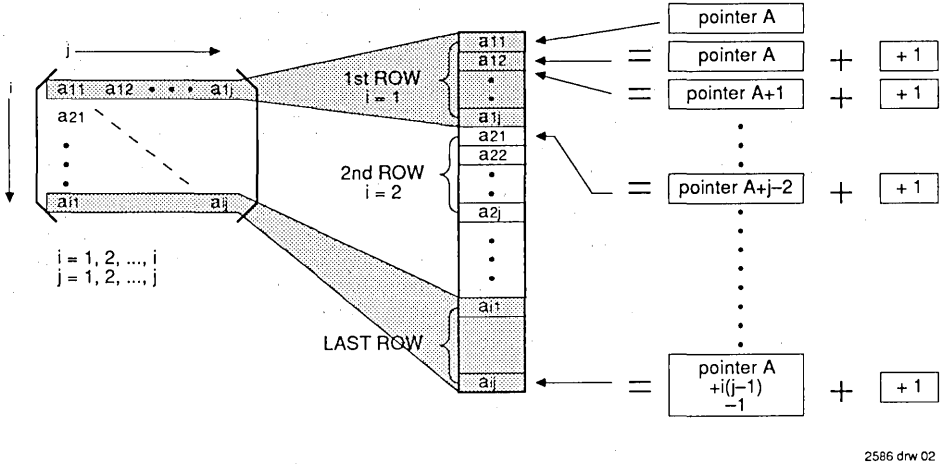

Figure 2. Sequential Memory Organization and Sequential Accessing for a Matrix

Interleaved Memory Organization

Another type of memory organization is implemented by interleaving matrices in the same memory segment (Figure 3). This can be found in the time multiplexed data acquisition and processing. The memory segment contains two sets of data [X] and [Y]. The entries of [X] and [Y] are interleaved in the same segment of the memory and therefore the entries of each matrix is accessed at an interval of two.

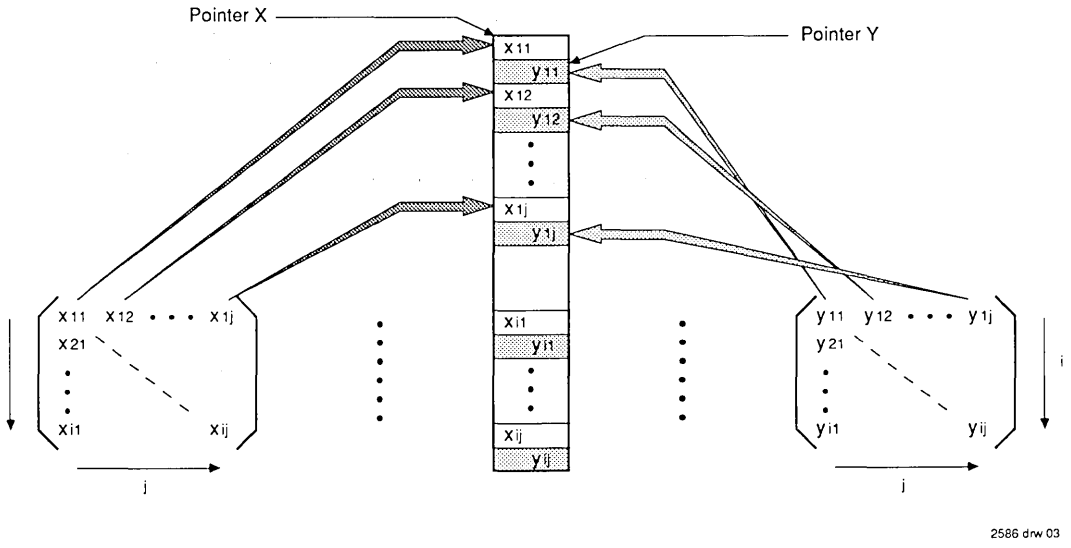

Figure 3. Interleaved Memory Organization and Interval Accessing for Two Matrices

Matrix Column Addressing

In the example of multiplication in Figure 1, the multiplier matrix [B] is accessed by the column instead of the row. Therefore, the address pointer increments at an interval of k, the column size of the matrix. Figure 4 shows the memory organization and accessing of the matrix [B].

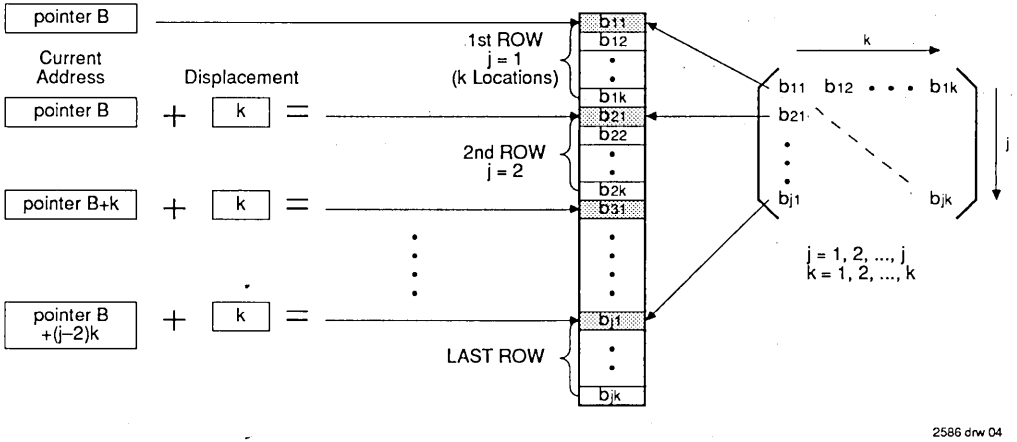

Figure 4. Sequential Memory Organization and Interval Accessing for Matrix [B]

Address Generator

Different addressing schemes are required to access different memory organizations, or different structured data organizations. An ALU–based address generator is best suited for this type of application since it can increment the address based on a pointer and a displacement (Figure 5).

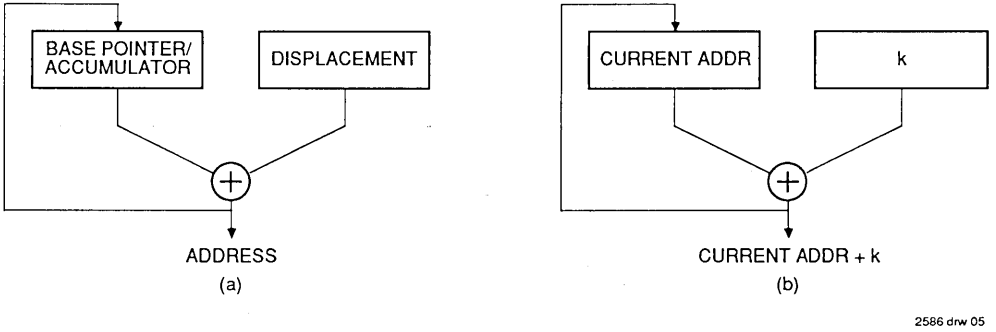

Figure 5. ALU-based Address Generator for Matrix Column Addressing

MATRIX UNIT OPERATIONS

In a matrix multiplication (Figure 1) involving two matrices [A] and [B], each entry in the product matrix [C] is obtained by summing the products which are obtained by multiplying the entries in the first matrix [A] with the corresponding entries in the second matrix [B].

The matrix multiplication process can be described as C–language program where the loop in the line 6 and 7 fetches two entries from the memory and stores the product entry back into the memory. The unit operation line 7 consists of a multiplication and an addition which can be performed in hardware with a single chip multiplier–accumulator, such as the IDT7210 16–bit MAC.

```
1   {
2       for (i = 0, i < MaxRow_A,.i++)
3       {
4           for (k = 0, k < MaxColumn_B, k++)
5           {
6               for (j = 0, j < MaxColumn_A, j++)
7                   cik = cik + aij x bjk
8           }
9       }
10  }
```

* MaxRow_A = number of row in matrix A,
MaxColumn_A = number of column in matrix A,
MaxColumn_B = number of column in matrix B.

7

PIPELINED MATRIX MANIPULATION ENGINE

To implement the matrix operation in hardware, three functional blocks are required: the address generator, the multiplier/accumulator (MAC), and the memory (Figure 6). The IDT7383 or IDT7381 is used as the address generator. An IDT7210 is used to implement the multiply–accumulate operation. This implementation uses both pipeline registers and a multi–bank memory to achieve the highest performance using a high degree of parallelism. In the pipelined architecture, four operations execute in parallel during a single cycle: generating a read address, reading out data from memory, loading two operands and multiplying and adding, and generating write address and writing data to memory. These four stages are easily identified by locating the clock input of the pipeline registers (Figure 7).

The multiplication–and–addition is performed using a multiplier–accumulator. The two input data pipeline registers and output data pipeline register reduces the part count during pipelined operation. It allows the system to do the multiplication and addition while the result of the previous operation is stored into memory.

The multi–bank memory allows the system to simultaneously access two entries of matrices [A] and [B]. It also allows the system to write the product entry into matrix [C] in the same cycle. It requires one address generator for each bank of memory to simultaneously access all three banks of memory. The 16–bit ALU–based address generator is capable of accessing up to 64K locations.

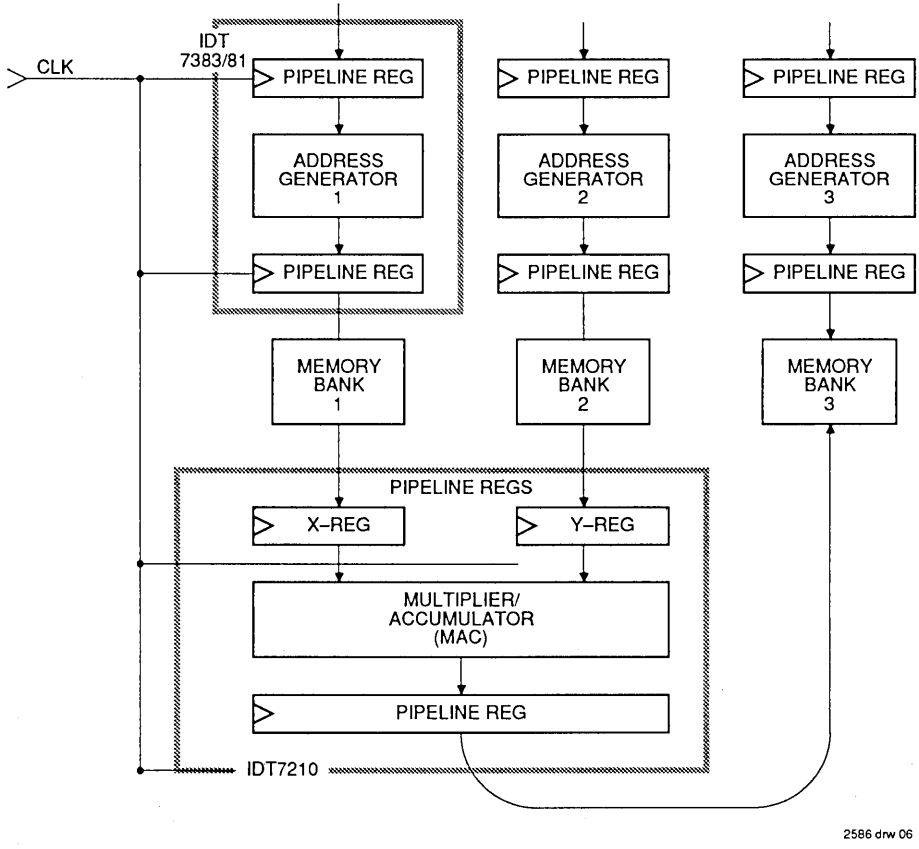

Figure 6. Block Diagram of Pipelined Matrix Manipulation Engine

PIPELINED STAGE, DATA PATH, AND CYCLE TIME

The first pipeline stage, i.e. address calculation, consists of the input pipeline registers and the ALU in the IDT7383/IDT7381. The ALU calculates the address and sends the results to the output pipeline register. The propagation delay from the input clock to the valid result from the ALU is 25ns (Figure 7).

The second pipeline stage, i.e. memory read, consists of the output pipeline register of the IDT7383/7381 and two banks of IDT6116 2K x 8 SRAMs. The address generator provides the address to the memory. The data is subsequently read from the memory. The propagation delay from the output clock to the memory output data valid is 33ns (Figure 7).

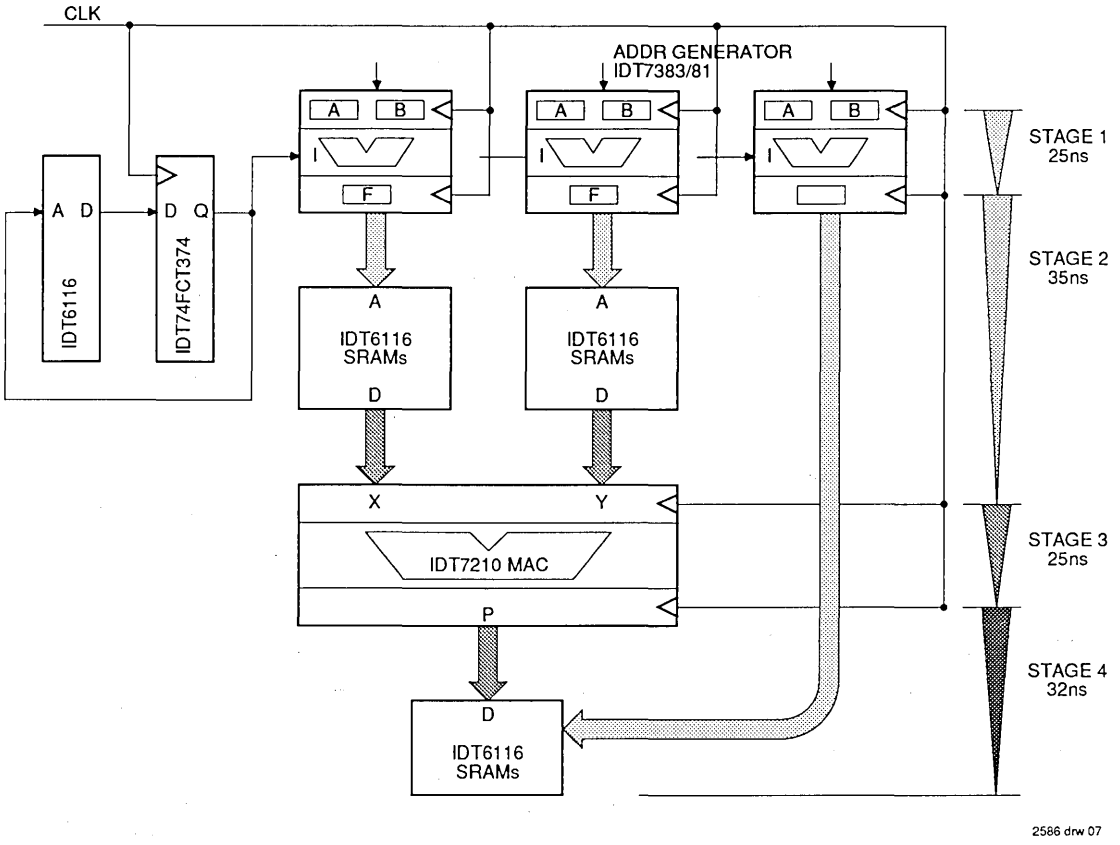

Figure 7. Propagation Delay of the 4-Stage Pipelined Matrix Manipulation

The third pipeline stage, i.e. multiply–accumulate, consists of the input registers and multiplier–and–accumulator in the IDT7210. Two operands are multiplied and added to the content retained in the accumulator. The result, stored in the accumulator, is ready to be clocked into the output register. The propagation delay from the clock of the input register to the valid output of the MAC is 25ns.

The fourth pipeline stage, i.e. memory write, consists of the output pipeline register of the IDT7210 and the third bank of IDT6116 2K x 8 SRAM. An address generator simultaneously provides the address for the memory write. The propagation delay from the clock of the output register of the IDT7210 to the end of the memory write is 32ns.

The control section consists of the IDT6116 2K x 8 SRAM and IDT74FCT374 Octal register. It is found that the propagation delay is the combination of the output valid delay, 6.5ns, and the instruction setup time, 19ns. The total propagation delay is 25.5ns.

Effectively, the cycle time of this engine is determined by the memory read cycle which requires a 35ns cycle time. The four–stage pipelined cycle time and timing diagram are shown in Figure 8 and Figure 9. For the corresponding control signals, please refer to the IDT data book.

				Total Delay
	Stage 1 ADDRESSING	Min. CLK to CLK IDT7383/81	25ns	25ns
	Stage 2 SRAM READ	CLK to F IDT7383/81 (FTAB = 0, FTF = 0) Addr to Data IDT6116–12 Input Setup IDT7210	11ns 12ns 12ns	35ns
	Stage 3 MAC CYCLE	Min. CLK to CLK IDT7210	25ns	25ns
	Stage 4 SRAM WRITE	CLK to P IDT7210 Addr to Data IDT6116–12	20ns 12ns	32ns
	CONTROL CYCLE	CLK to Q IDT74FCT374 I Setup IDT7383/81 (FTAB = 0, FTF = 0)	6.5ns 19ns	25.5ns

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Figure 8. Minimal Cycle Time of Each Stage of Matrix Manipulation Engine

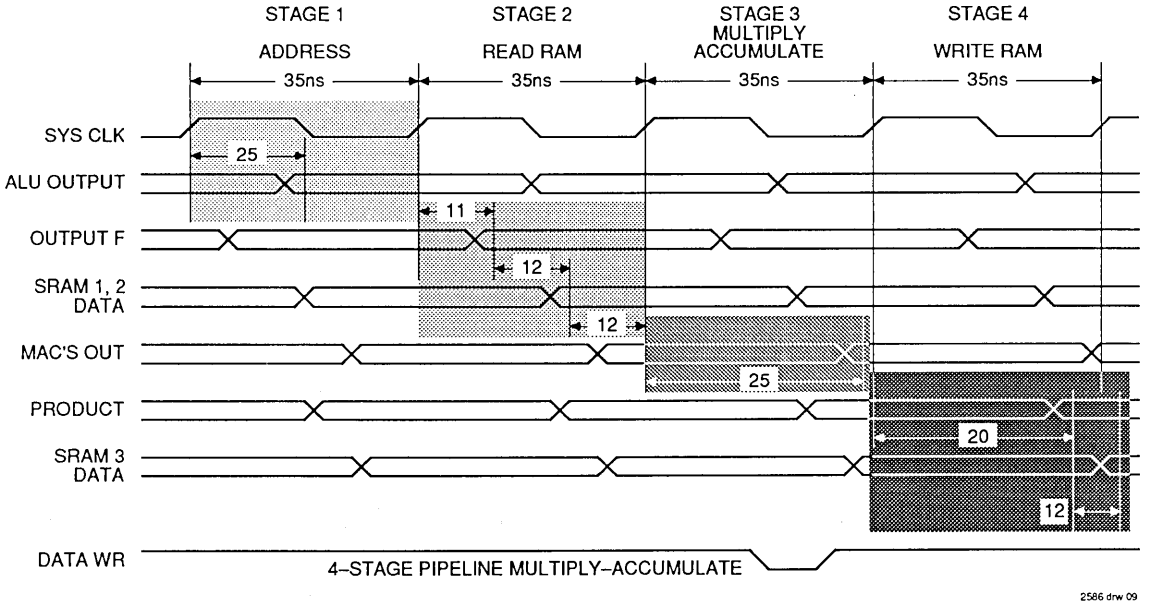

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Figure 9. Pipelined Timing Diagram of Matrix Manipulation Engine

SUMMARY

A high performance matrix manipulation engine can be implemented by using the IDT7383/IDT7381 16–bit ALU, IDT7210 MAC, and IDT6116 2K x 8 SRAM. A cycle time of 35ns is achieved in the matrix unit operation engine by using a 4–stage pipelined architecture. These four stages, addressing, SRAM read, Multiply–Accumulate, and SRAM write, are pipelined together so that effectively one matrix unit operation is processed every cycle. Both the IDT7383/IDT7381 16–bit ALU and the IDT7210 16–bit MAC have on chip input/output pipeline registers, which reduce board space and chip count.

Highly structured data is easily accessed by using the IDT7383/7381 ALU–based address generator. The structured data may be organized in several ways: segmented organization, sequential organization, and interleaved organization. The ALU–based address generator supplies the sequential or non–sequential addresses based on the base–pointer and displacement provided by the system.

Integrated Device Technology, Inc.

HIGH-PERFORMANCE GRAPHICS SYSTEM DESIGN USING THE IDT75C458 PaletteDAC™

APPLICATION NOTE AN-37

By Tao Lin, Wing Leung and Frank Schapfel

INTRODUCTION

The IDT75C458 PaletteDAC™ is a triple 8-bit video DAC with on-chip dual-ported color palette memory. The PaletteDAC is optimally designed for use in high performance bit-mapped graphics display applications. The architecture eliminates the ECL pixel interface by providing multiple TTL-compatible pixel ports and by multiplexing the pixel data on chip.

Video data rates of 165MHz enable color monitors of 1600 x 1280 pixel resolution to display up to 256 simultaneous colors from a palette of 16.8 million colors using one PaletteDAC. Using three IDT75C458s, the full spectrum of 16.8 million colors can be displayed, a required feature in true color, photo realistic graphics display.

Synchronizing Three PaletteDACs

When synchronizing three PaletteDACs for true color applications, an on-chip Phase-Locked Loop (PLL) fixes the pipeline delay from the pixel input ports to the triple DAC. The PLL sets the pipeline delay to nine clock cycles, and insures synchronization of the three PaletteDACs with only one clock signal. The performance of true color systems is enhanced because the time skew from the digital components of the pixel data path.

Other implementations of the PaletteDAC, such as the Brooktree® Bt458, have a variable pipeline delay of six to ten clock cycles, which must be set during the power up sequence. To set the pipeline delay of the Bt458, a complicated power up and timing sequence is necessary by starting, stopping and re-starting the CLOCK and $\overline{\text{CLOCK}}$ signals. When using multiple Bt458s, a hardware reset of the blink counter circuitry is not possible when setting the pipeline delay to 8 clock cycles. Therefore, the blink counters must be synchronized using software control.

The PaletteDAC's on-chip PLL automatically sets the pipeline delay to 9 clock cycles, thereby eliminating the complicated power up sequence required by the Bt458. We will discuss the mechanism to fix the pipeline delay and the role of the PLL.

On-Chip Phase-Locked Loop

The next generation, true color graphics display will use a 1600 x 1280 pixel resolution screen and requires three PaletteDACs with the pixel clock operating at 165MHz to display the full spectrum of 16.8 million colors. Typically, slow speed video RAMs (VRAM) built using dynamic RAM technology store the pixel information in the frame buffer. Five pixel ports and internal multiplexing on the PaletteDAC enable a TTL-compatible interface to the frame buffer while maintaining a 165MHz pixel clock rate.

On the rising edge of Load Clock input ($\overline{\text{LD}}$) color data for four or five consecutive pixels is latched into the PaletteDAC. Therefore, the $\overline{\text{LD}}$ signal is four to five times slower than the pixel clock (CLK), and is typically derived by externally dividing the pixel clock by 4 or 5. Inevitably, the $\overline{\text{LD}}$ signal is phase shifted with respect to CLK because of the propagation delay of generating $\overline{\text{LD}}$.

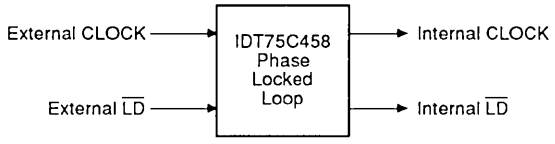

Figure 1. Phase Locked Loop on the PaletteDAC

The PLL on the IDT75C458 synchronizes the $\overline{\text{LD}}$ and CLK signals. As shown in Figure 1, the PLL receives the external $\overline{\text{LD}}$ and CLK signals and generates internal $\overline{\text{LD}}$ and CLK signals. The phases of the external $\overline{\text{LD}}$ and external CLK may differ, (Figure 2). The PLL corrects the phase shift by forcing the internal $\overline{\text{LD}}$ and internal CLK to have the same phase. The PLL approach guarantees that the internal $\overline{\text{LD}}$ follows the external $\overline{\text{LD}}$ by less than one pixel clock cycle. Alternatively, the internal counter approach implemented in the Bt458 allows the internal $\overline{\text{LD}}$ to follow the external $\overline{\text{LD}}$ by between one and four clock cycles.

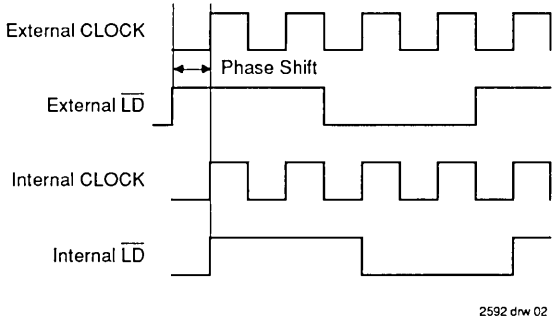

Figure 2. Phase Relationship of the Internal and External Load Clock and Clock

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Brooktree is a registered trademark of Brooktree Corporation

Fixing the Pipeline Delay

Figure 3 illustrates the data path inside the PaletteDAC for the pixel select input data, overlay select input data, $\overline{SYNC}$ and $\overline{BLANK}$ signals. All data operations are pipelined to maximize throughput performance. The rising edge of external $\overline{LD}$ latches pixel data to the Master Latch while the rising edge of the internal $\overline{LD}$ latches pixel data to the Slave Latch. All subsequent internal data operations are controlled by the internal pixel clock. Since the on-chip PLL forces the internal $\overline{LD}$ signal to follow the external $\overline{LD}$ by less than one clock cycle, the pipeline delay from the pixel input port to the triple DAC is fixed at 9 clock cycles.

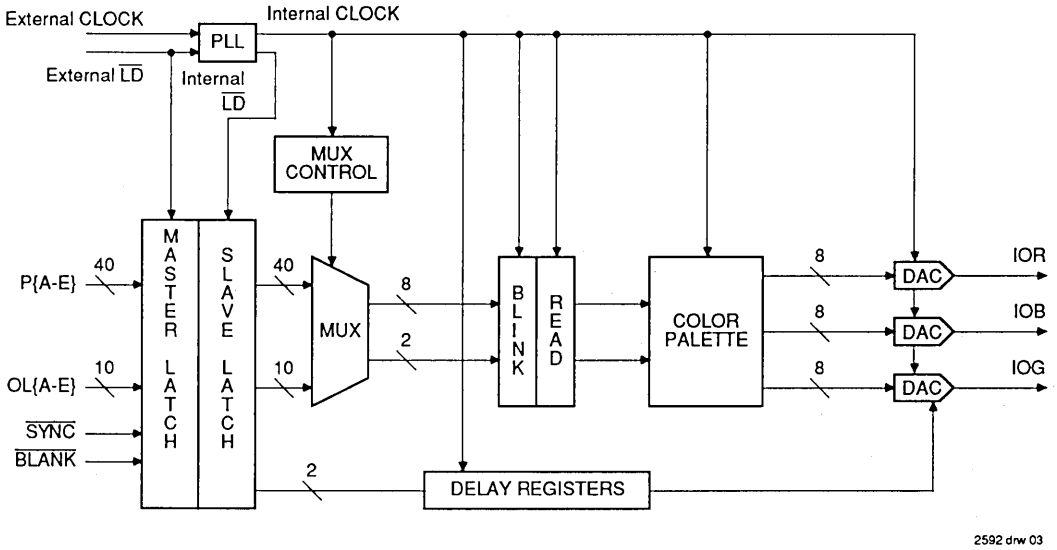


Figure 3. Pixel Data Path of the IDT75C458

25MHz Graphics Engine Interface

Today's high-speed graphics workstations employ graphics engines operating at clock frequencies in excess of 10MHz. The IDT75C458's microprocessor interface can handle a data rate of up to 25MBytes per second. The enhanced interface to the color palette allows today's 25MHz graphics engines or RISC microprocessors, such as the IDT7953000, the ability to change the colors in the PaletteDAC's RAM thereby increasing the throughput of the controlling microprocessor. Since the IDT75C458 is intended for high-speed operation, there is less control timing error tolerance compared to that of a slower part. To maintain proper operation, the control timing parameters (i.e., zero write data hold time) must not be exceeded at full operational speed and throughout the operational temperature range.

High-Speed Analog Output

To achieve a 165MHz pixel conversion rate, the analog outputs are designed to operate with a 1.5ns rise/fall time at a full-scale swing of 0 to 0.7V. The full-scale output settles within 6ns (including the rise and fall time) with proper termination and an output load to 17pF. The fast settling time is the result of the low output capacitance (7-8pF) of the digital-to-analog converters and the minimal package inductance of the 84-pin grid array and plastic leaded chip carrier (PLCC).

High Performance Design Considerations

When designing high performance digital and analog systems using the IDT75C458, special attention should be paid to the PC board layout, impedance matching and decoupling considerations, as these are crucial to minimizing noise and obtaining stable performance.

Analog Output Connection and Impedance Matching

To fully utilize the superior performance capabilities of the IDT75C458, special attention must be paid to the handling of the analog output signals. To minimize the transmission line effects, accurate termination resistance, cable assembly and well-matched characteristic impedance in the operating frequency range are necessary. The loading impedance to the analog outputs resulting from the PC board metal trace, cable assembly, and termination must not be inductive. Inductive loading impedance introduces overshoots and ringing on the analog output waveforms, which in turn increase the settling time and smear images on the CRT screen. To avoid inductive loading impedance, the PC board metal traces connecting the analog outputs of the IDT75C458 to the BNC must be as short as possible, as illustrated in Figure 4.

For most applications, the inductive effect can be cancelled out (at the expense of frequency bandwidth) by adding 10 to 20pF capacitor at the analog outputs as close to the package pins as possible. Each analog output should have a 75 ohm

load resistor connected to ground to achieve maximum performance. To minimize transmission line effect reflections, the resistors should have the shortest leads and be placed as close to the IDT75C458 as possible.

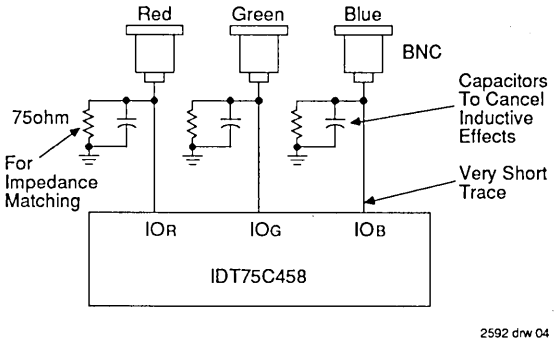


Figure 4. Output Connection and Impedance Matching

Ground Plane

Although the ground pins on the IDT75C458 are called analog ground (AGND), they should be connected to the digital groundplane of the PC board through ferrite beads and decoupled to the analog VAA. To minimize noise on the board, the analog groundplane area should surround all peripheral circuitry and connections for the IDT75C458: the decoupling capacitors, the external voltage reference circuitry, the analog output traces and output amplifiers and all digital input signals leading to the IDT75C458.

Analog Power Plane and Supply Decoupling

Most of the circuits on the chip are synchronized to the pixel clock and switch at the clock edges. Consequently, large voltage spikes are generated on the power supply lines. Without good power supply decoupling these voltage spikes can be decoupled to the analog outputs and result in a snowy screen. Therefore, a separate analog power plane should be furnished for the IDT75C458 and its associated analog circuitry. Figure 5 illustrates how the analog power plane should be connected to the digital PC board power plane (Vcc) at a single point through a ferrite bead located as close as possible to the IDT75C458. The IDT75C458 has six analog ground pins separated into three groups, with each group decoupled with a 0.1µF ceramic capacitor in parallel with a 0.1µF chip capacitor. These capacitors should be installed close to the PaletteDAC using the shortest leads possible.

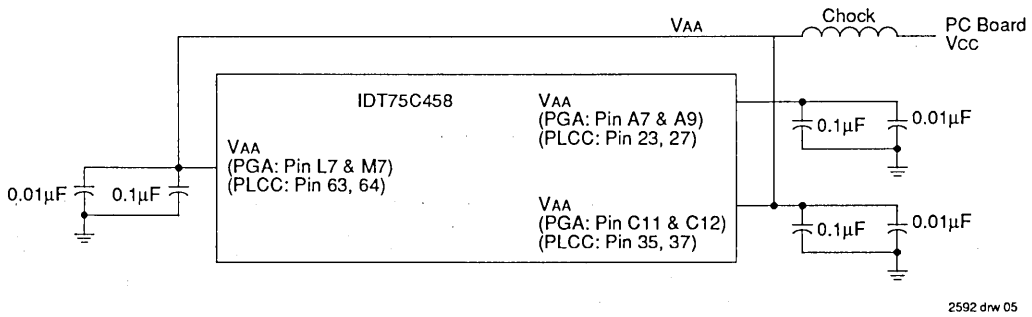


Figure 5. Analog Power Plane and Decoupling of Each Group of Analog Pins

For the lowest levels of cross talk and noise pickup between the PaletteDAC's analog circuitry and the digital traces on the printed circuit board, power for the digital logic should come from the digital power supply plane.

CONCLUSION

The PaletteDAC provides an easy upgrade of existing high performance graphics display boards. With the 165MHz version, a 1600 x 1280 pixel screen resolution can be achieved with minimal design effort. Taking advantage of the on-chip phase locked loop, three PaletteDACs display true color images using a palette of 16.8 million colors, without complicated external synchronization circuitry. The 25MHz microprocessor interface allows today's high performance graphics engines and RISC microprocessors to change palette colors without wait states. The PaletteDAC clearly supplies the best upgrade path for today's graphics display boards.

Integrated Device Technology, Inc.

USING THE IDT75C457s PaletteDAC™ IN TRUE-COLOR AND MONOCHROME GRAPHICS APPLICATIONS

APPLICATION NOTE AN-63

by Tao Lin

The IDT75C457 is the newest member in the IDT PaletteDAC™ family which targets high-performance graphics systems. The IDT75C457 is primarily used in high-resolution true-color applications, although it can also be applied to high-resolution monochrome graphics systems.

Besides having all the features of the industry standard Bt457, the IDT75C457 is unique in that the device includes an on-chip Phase-Locked Loop (PLL) and consumes less power. The block diagram of the IDT75C457 is shown in Figure 1. The PLL automatically synchronizes the load-data clock, $\overline{LD}$, and the high-frequency pixel clock, CLOCK. This feature results in the following major advantages of the IDT75C457 over the Bt457: (1) a reset operation is not required. Therefore, an external clock chip with a reset feature such as the Bt439, is not necessary, (2) the internal pipeline delay is automatically fixed to 9 clock cycles and (3) in true-color graphics systems where three IDT75C457s are used for red, green and blue channels, respectively, the internal pixel clocks of all the three chips are synchronized to the same external reference clock, $\overline{LD}$. The synchronization minimizes the internal pixel clock skew from chip to chip. Consequently, the video output skew among the three channels is usually within sub-pixel resolution even without an external PLL.

The low power consumption of the device results from the lower static and dynamic switching current of the chip. Thus, the IDT75C457 generates less digital noise than the industry standard part. As a result, less noise is coupled to the analog output and the display quality is improved. To further decouple the internal analog circuitry from outside noise and improve the stability of the analog video output, it is recommended that a separate ground be provided for the external voltage reference circuitry.

A typical configuration using the IDT75C457 in a monochrome graphics system is shown in Figure 2. In true-color applications, three IDT75C457s are needed and a typical configuration is shown in Figure 3. Note that a separate ground is provided for the external voltage reference circuitry. This ground is connected to the PC board ground plane at a single point through a ferrite bead. Moreover, for maximum and stable performance, designers using the IDT75C457 should pay close attention to high-speed design issues such as PC board layout, impedance matching and decoupling. They should follow the same guidance as given in Application Note AN-37[1] for the IDT75C458.

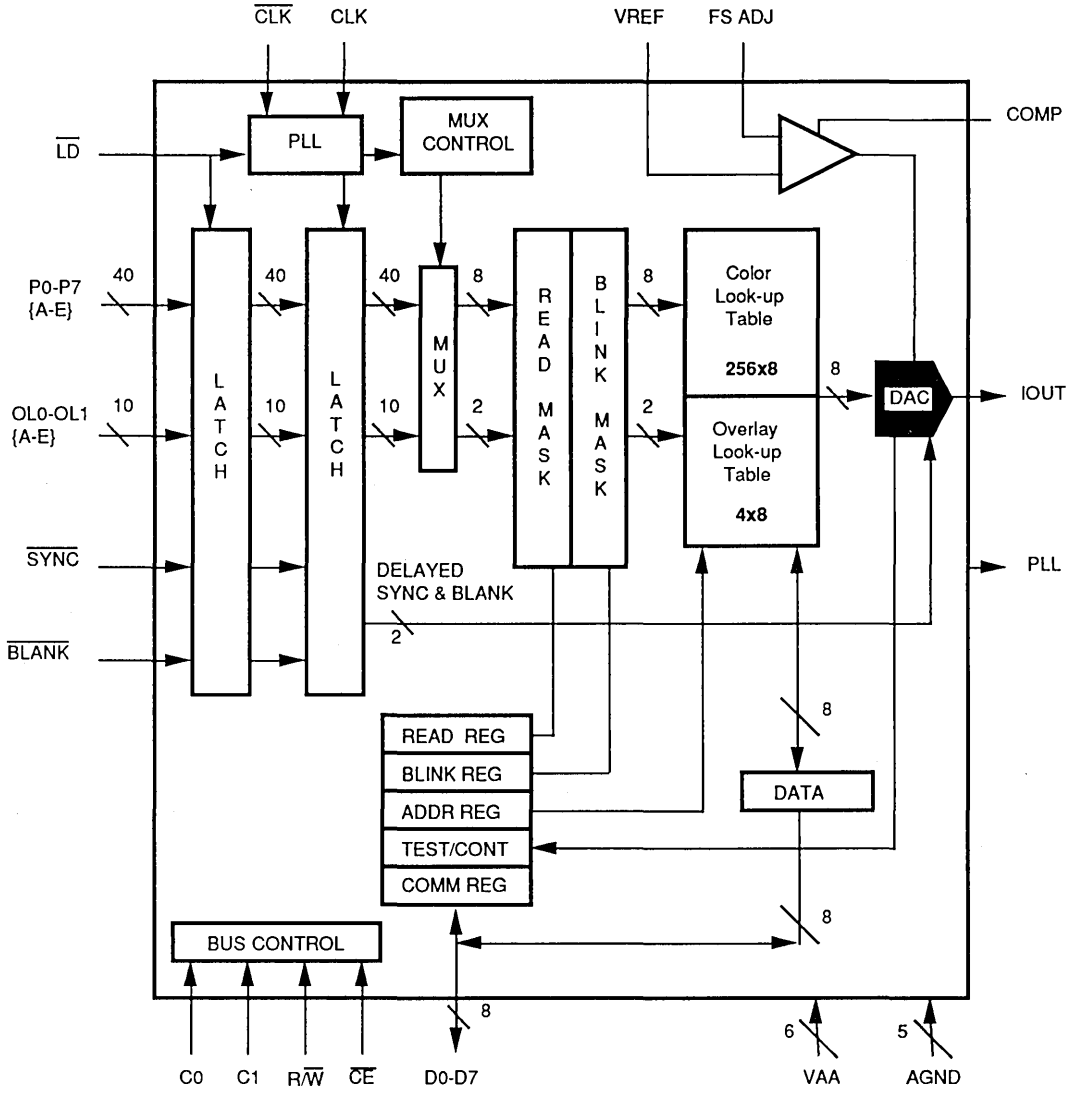
Since the IDT75C457 does not need an external clock reset operation to synchronize the internal clock signals, the clock generator can be simply built using a crystal oscillator and a few ECL chips. Figure 4 shows a typical clock circuit using three ECL chips for either 4:1 multiplexing or 5:1 multiplexing. Figure 5 shows another typical clock circuit using two ECL chips for 5:1 multiplexing.

In conclusion, the IDT75C457 simplifies the design of high-resolution graphics systems and, with the advantages of the internal PLL and low power dissipation, offers the best upgrade path towards tomorrow's photo-realistic graphics display systems.

7

NOTE:

1. Tao Lin, Wing Leung and Frank Schapfel, "High-performance Graphics System Design Using the IDT75C458 PaletteDAC™", IDT Application Note AN-37.


CLK
CLK
VREF
FS ADJ
COMP
LD
PLL
MUX CONTROL
P0-P7 {A-E}
OL0-OL1 {A-E}
40
10
LATCH
MUX
READ MASK
BLINK MASK
8
2
Color Look-up Table
256x8
Overlay Look-up Table
4x8
DAC
IOUT
PLL
SYNC
BLANK
DELAYED SYNC & BLANK
READ REG
BLINK REG
ADDR REG
TEST/CONT
COMM REG
DATA
BUS CONTROL
C0
C1
R/W
CE
D0-D7
VAA
AGND
6
5

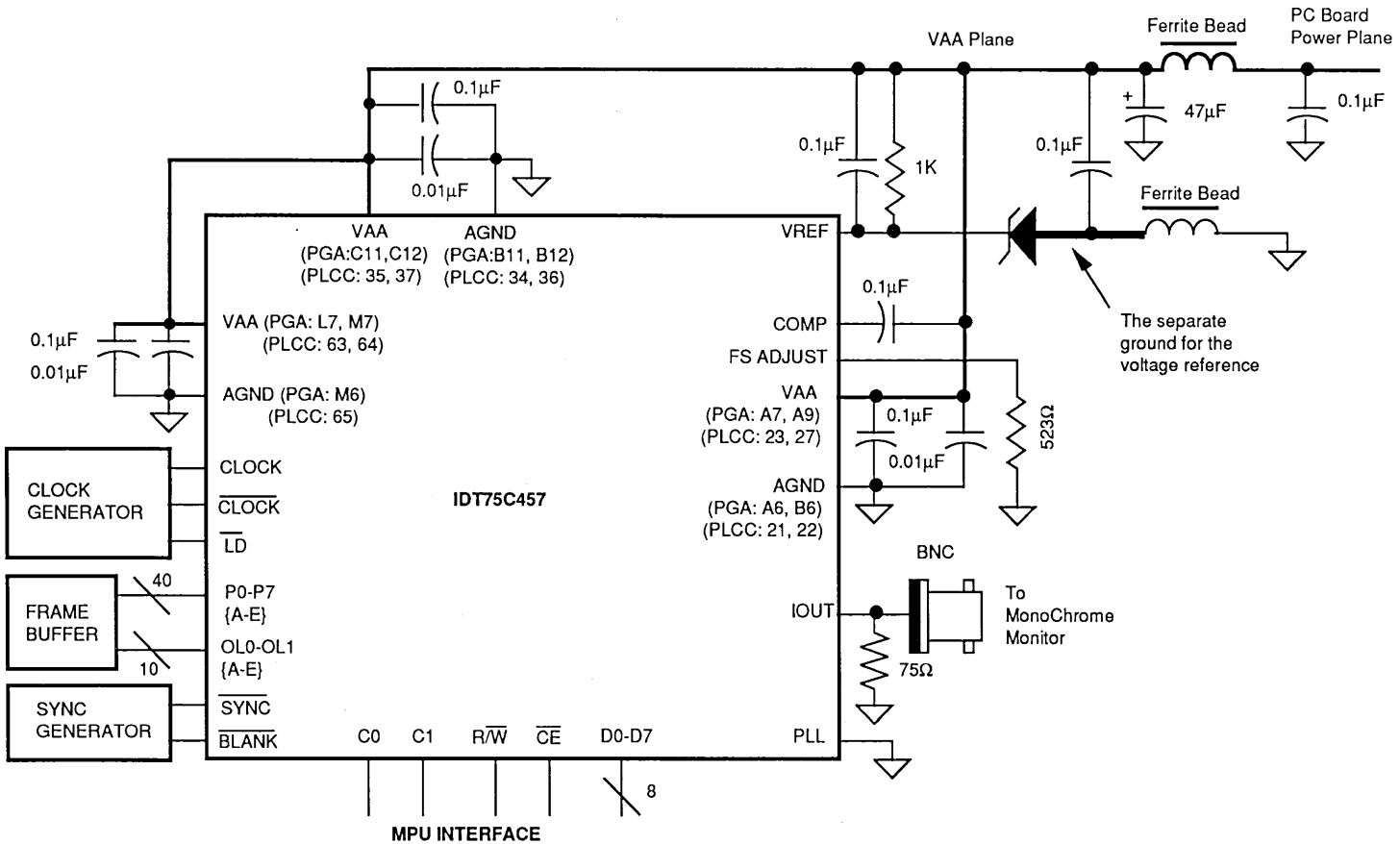


Figure 2. A Typical Configuration for Monochrome Applications

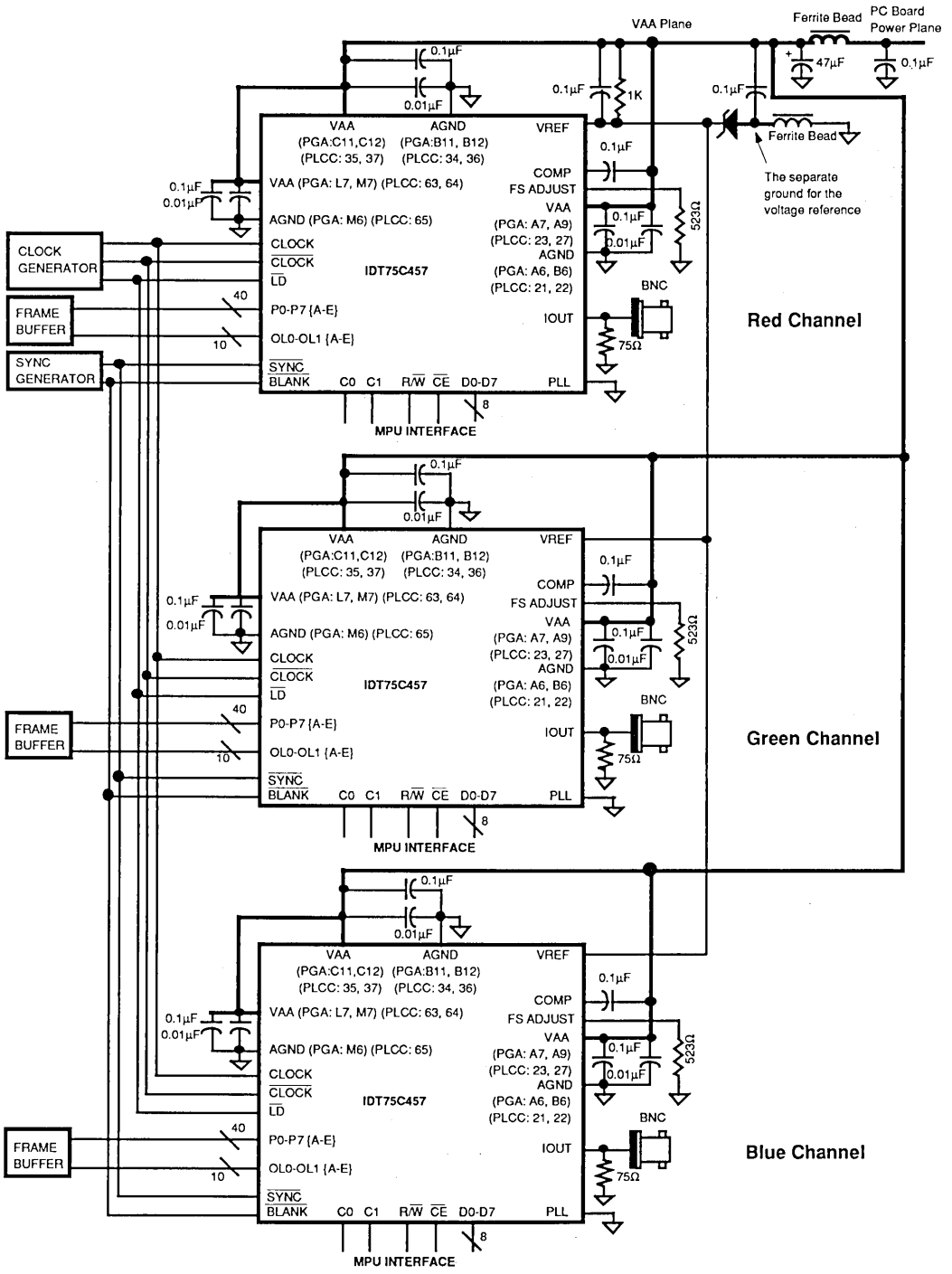


Figure 3. Typical Configuration for True-Color Applications

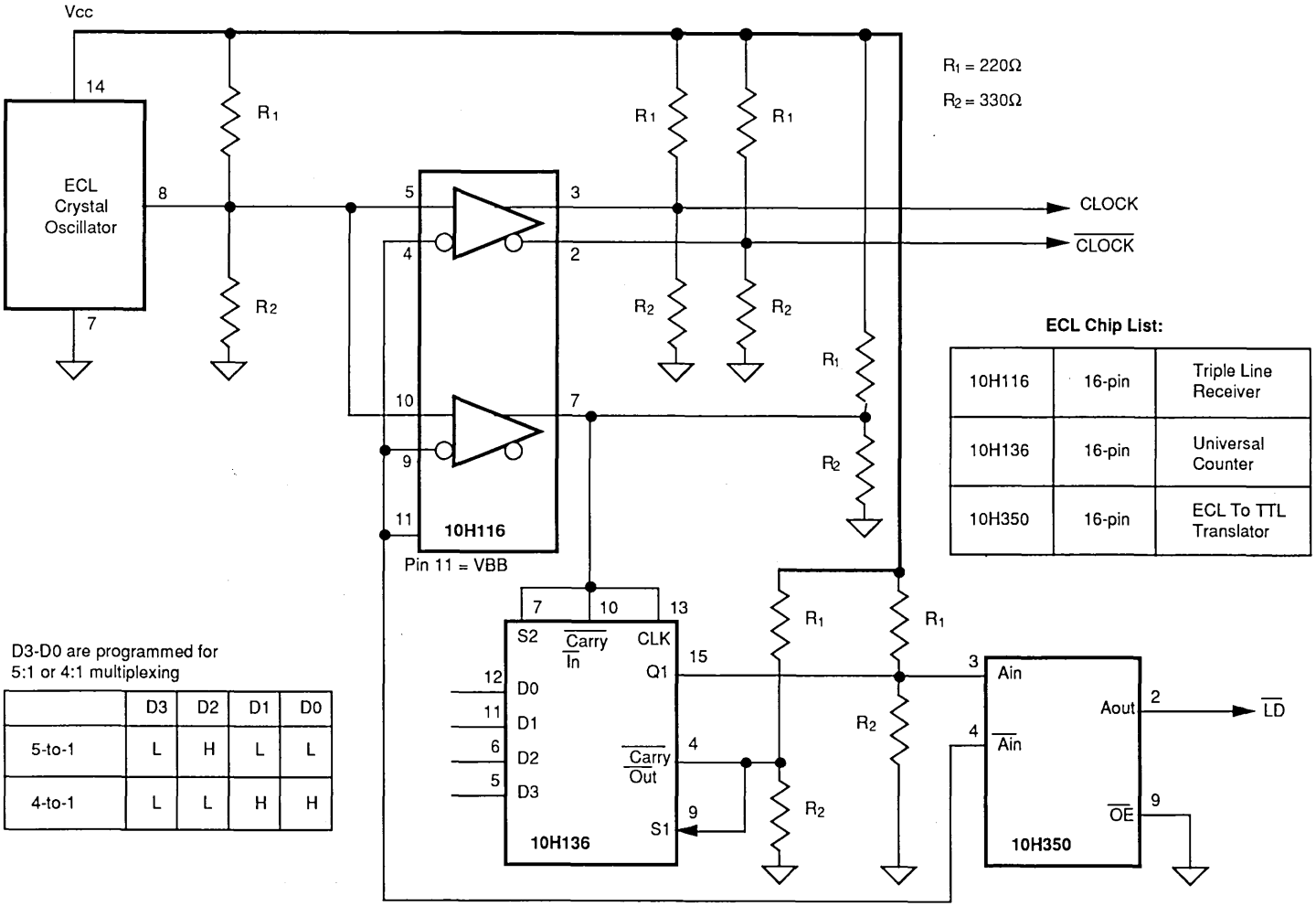
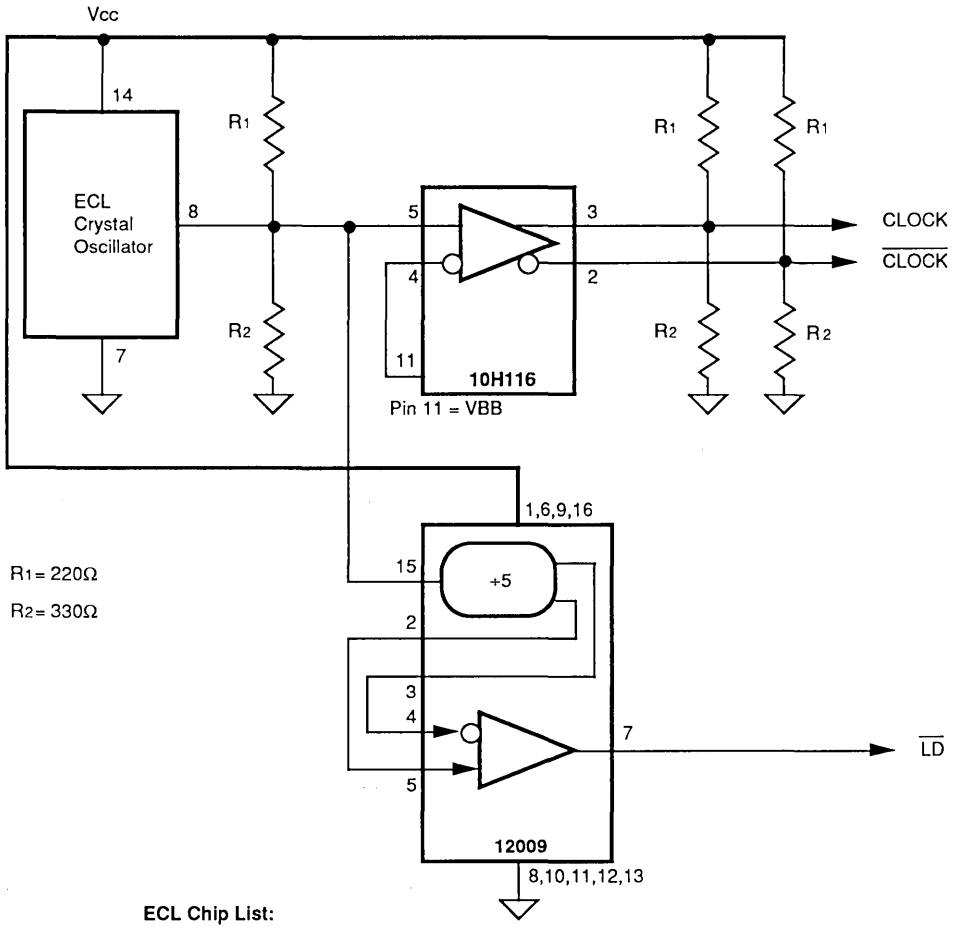


Figure 4. A Typical Clock Circuit for 5:1 or 4:1 Multiplexing



ECL Chip List:

10H116	16-pin	Triple Line Receiver
12009	16-pin	Prescaler w/ ECL To TTL Translator

Figure 5. A Typical Clock Circuit for 5:1 Multiplexing

Integrated Device Technology, Inc.

PROTECTING YOUR DATA WITH THE IDT49C465 32-BIT Flow-thruEDC™ UNIT

APPLICATION NOTE AN-64

by Tao Lin, Gerard Lyons and Frank Schapfel

INTRODUCTION

A TIME FOR ERROR-FREE MEMORIES

With the advent of high-performance 32-bit RISC and CISC microprocessors, general purpose computing across a wide spectrum of applications software is now easily accessible on a desktop. We can now draw on computer resources which are very sophisticated, multi-task systems with distributed processing power, and we no longer must rely on the centralized mini-computers and mainframes for processing horsepower. Both the technical and the commercial computing environments demand the insatiable hunger for processing power.

This increasing demand for sophisticated applications software requires more system memory on a local level. Tightly coupled microprocessors and cache memory are designed for optimized processing throughput, but the cache memory is no substitute for system memory. Cache memory is typically composed of very high-speed static RAMs, with access times of 35 nanoseconds or less. System or main memory is almost always comprised of slower but very high-density dynamic RAMs, typically with access times of 100 nanoseconds or more, but with four times the density of static RAMs. So, when the state-of-the-art static RAMs are 1 Megabit large, the newest density dynamic RAM is 4 Megabits. Therefore, dynamic RAMs will always provide the most cost-effective implementation for system memory.

Dynamic RAMs, though, are very prone to externally induced errors. These externally induced errors are called soft errors, since they do not cause permanent damage to the memory cell. Soft errors can be induced by system noise, alpha particle and power supply surges, and will cause random data bits to be flipped from "1" to "0", or vice versa. Although these soft error occurrences may be rare and inconsequential when using small amounts of DRAMs, large DRAM arrays are much more error prone. Also, as seen in Figure 1, larger DRAM components are much more susceptible to soft errors by virtue of their smaller memory cell size. Hardware errors may also occur on system memory boards. These hard errors occur if one RAM component or RAM cell fails and is stuck at "0" or stuck at "1". Although less frequent, hard errors may cause a complete system shut down.

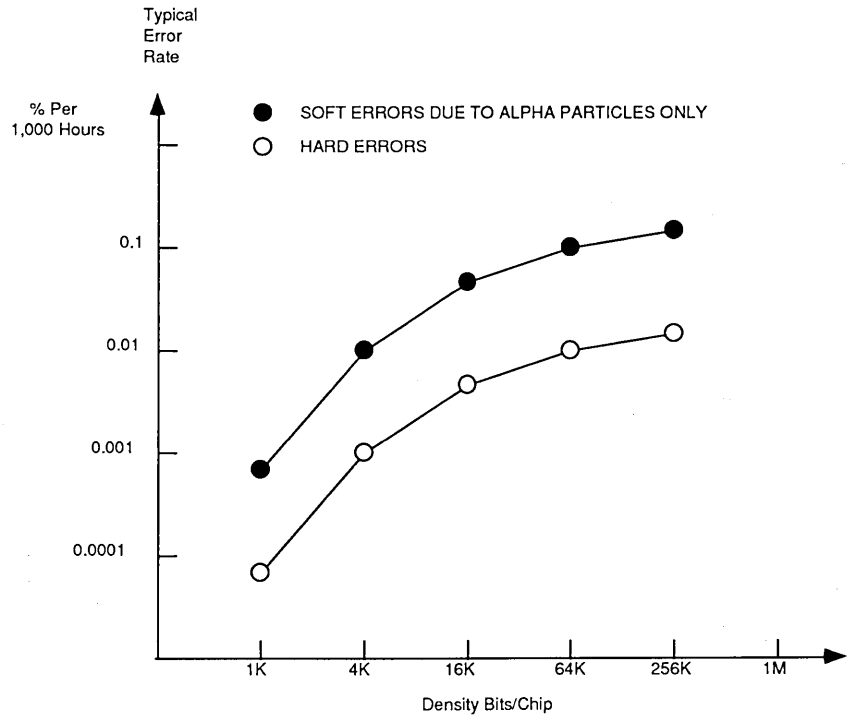


Figure 1. Typical Error Rates

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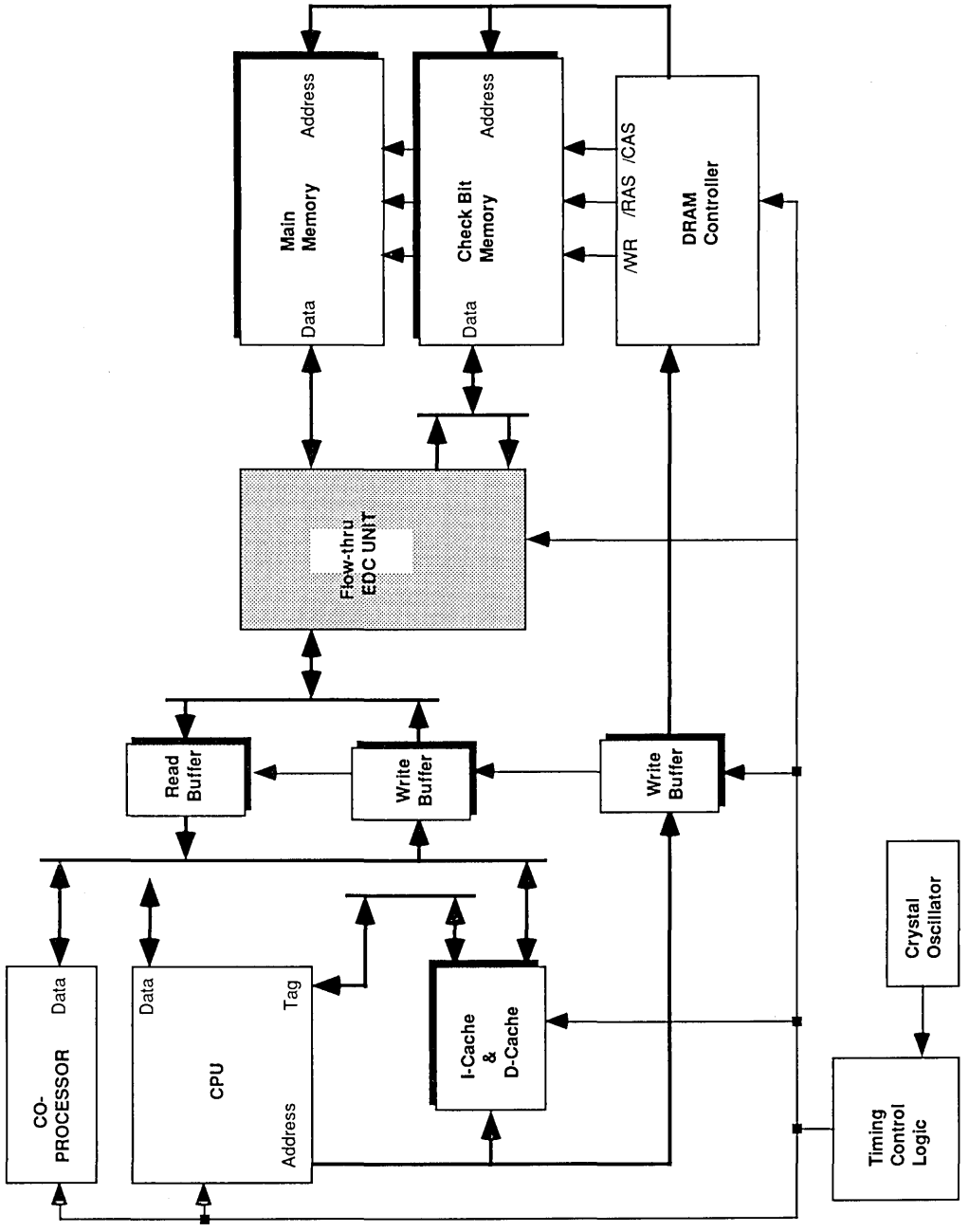

Figure 2. A Typical Architecture of High-performance RISC or CISC Systems

ERROR CORRECTION TO THE RESCUE

A scheme exists that not only is able to detect soft and hard errors, but is capable of correcting the erroneous bits. This scheme is implemented by a family of error detection and correction chips from Integrated Device Technology. Using a modified Hamming code, developed at AT&T Bell Labs, all single-bit errors may be detected and corrected, while all two-bit and most three-bit errors can be detected. IDT pioneered EDC chips, using CMOS technology in 1986, after recognizing the importance of large DRAM memory arrays in distributed computing.

TYPICAL ARCHITECTURE OF HIGH-PERFORMANCE RISC/CISC SYSTEMS

Figure 2 shows a typical architecture of high-performance RISC or CISC systems which have the following features: (1) high-speed cache memory (separate or common, Instruction-cache and Data-cache) for fast access to frequently used instructions and data, (2) write and read buffers to handle the mismatch between the high-speed CPU and the slow-speed main memory and (3) high-speed flow-thru EDC unit to insure data integrity.

While most high-performance computer systems in current market have the first and second features, the third feature is becoming more attractive and important when the main memory space grows and the memory word-length increases. Certainly, using an EDC unit is an effective way to improve the system reliability.

GENERAL EDC OPERATION

The basic function of an EDC device is to check the integrity of data being read from a memory system, flag an error if one has been detected and if possible correct that error. The IDT family of EDC devices implements this function using the same general principles, with some variations from device to device.

The operation of an EDC device can be generally split into:(1) generation of a coded word based on the data-word being written to memory. This coded word is called **The Check-Bit Word.** This operation is called **Generate;** (2) detection of errors in a data-word read from memory by comparing the corresponding check-bit word read from memory and a newly generated check-bit word (based on the data-word read from memory) and if possible correcting this error. The comparison of these two check-bit words (an exclusive-or (XOR) function) produces the so-called **Syndrome Word**. This operation is called **Detect/Correct.**

The coding scheme employed in IDT's EDC devices is a modified **Hamming Code.** For each data-word written to memory, a coded pattern, or check-bit word, is appended to the date-word. The new word (the data-word plus the check-bit word) can be termed a **valid code.** The modified Hamming Code establishes a Distance-of-4 between one valid code and another. This means that to go from one valid code to another, 4-bits have to change. It can be shown that a **Distance-of-4** code enables you to **detect all Single and Double-Bit** errors and **correct all Single-Bit** errors.

To implement a Distance-of-4 code on a 32-bit data-word, a 7-bit check-bit word must be appended. For a 64-bit word, a 8-bit check-bit word must be appended. The Hamming Code algorithm to generate a check-bit word from a 32-bit data-word or a 64-bit data-word can be found in either IDT49C460 data sheet or IDT49C465 data sheet.

EDC ARCHITECTURES AND WORD-LENGTH

There are two basic architectures for EDC operation: flow-thru and bus-watch. IDT provides a full line of EDC devices to support 16-bit and 32-bit bus-watch architectures and 32-bit and 64-bit flow-thru architectures, as shown in Table 1.

Part Number	Architecture	Word-length	Comment
IDT39C60	Bus-watch	16-bit	Cascadable up to 64-bit using 4 devices
IDT49C460	Bus-watch	32-bit	Cascadable up to 64-bit using 2 devices
IDT49C465	Flow-thru	32-bit	Cascadable up to 64-bit using 2 devices
IDT49C466	Flow-thru	64-bit	

Table 1. IDT EDC Product Line

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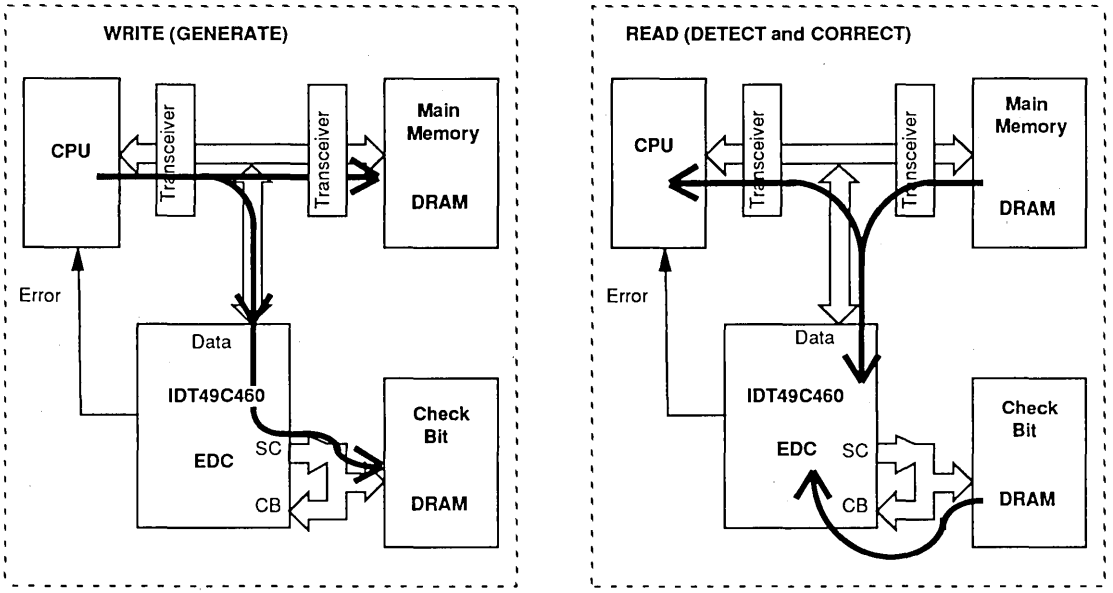
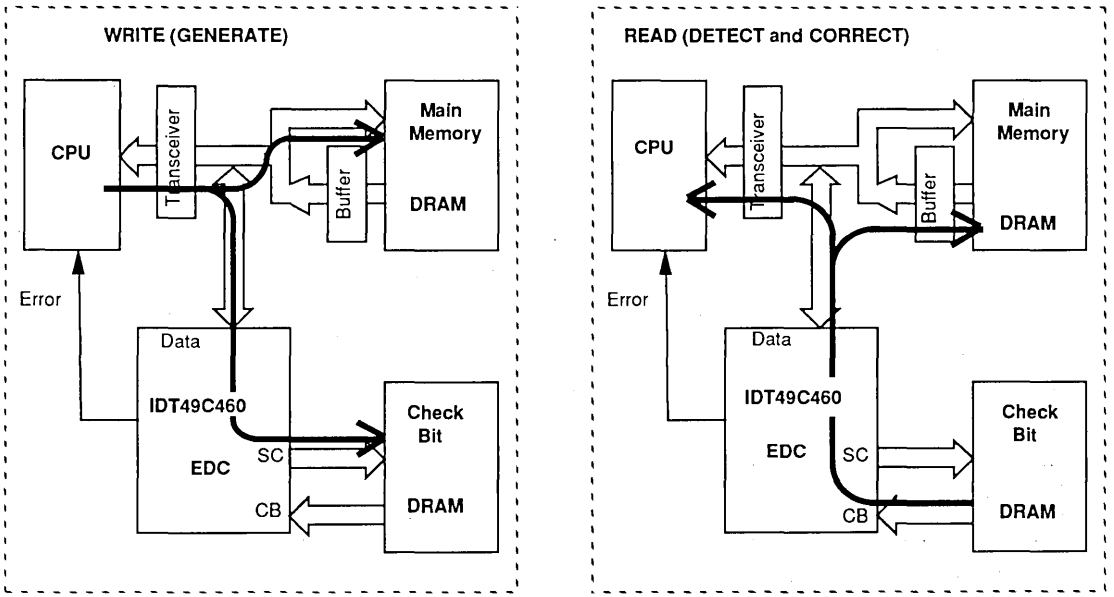
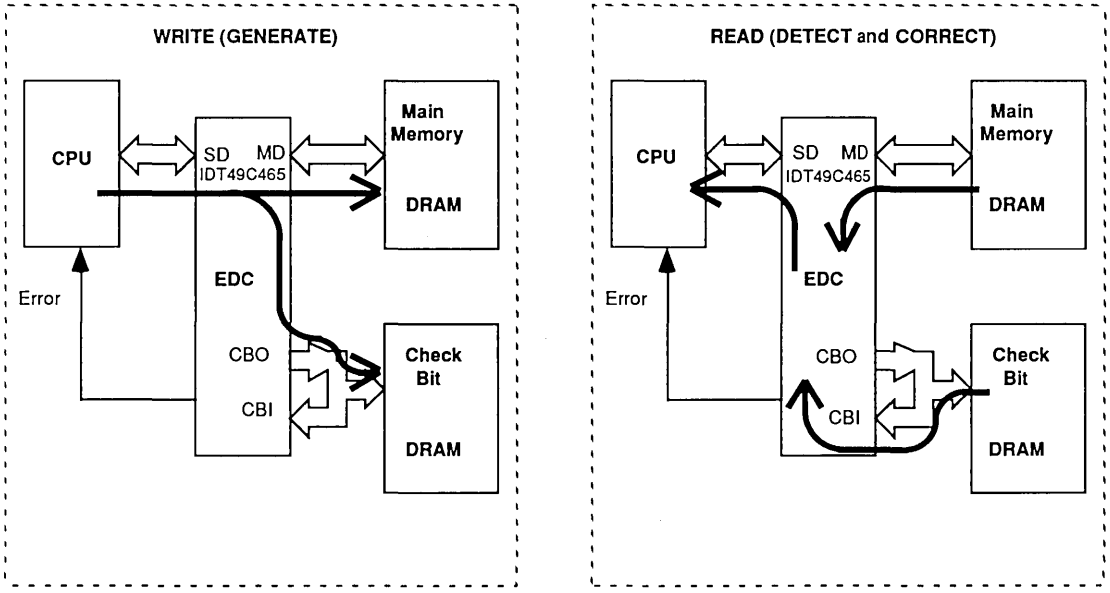


(a) Common I/O Memory System

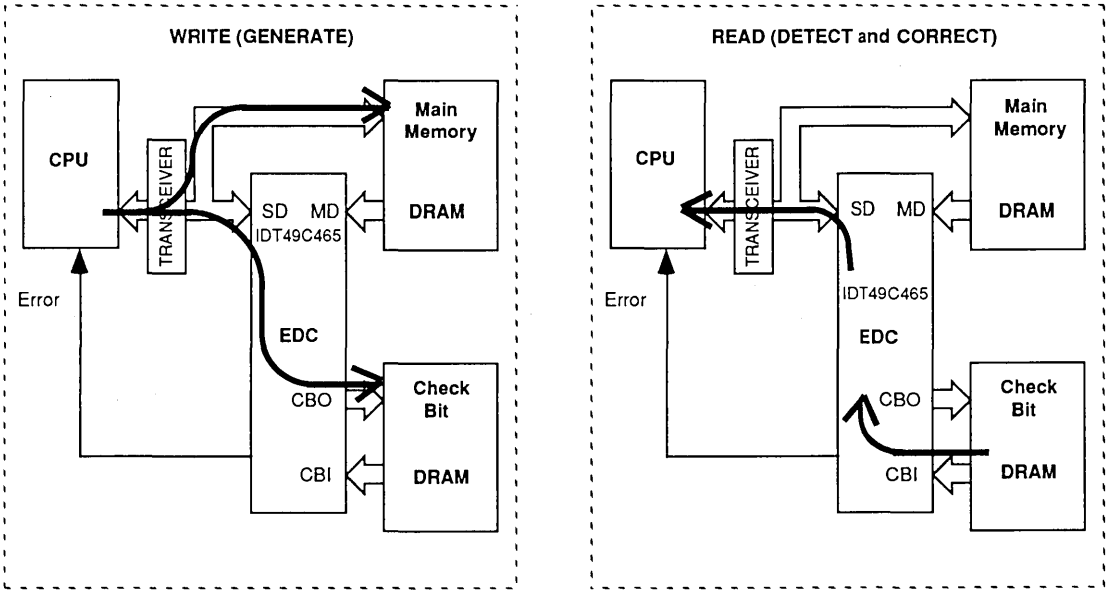


(b) Separate I/O Memory System

Figure 3. Basic Configurations Using a Bus-watch EDC Architecture



(a) Common I/O Memory System



(b) Separate I/O Memory System

Figure 4. Basic Configurations Using a Flow-thru EDC Architecture

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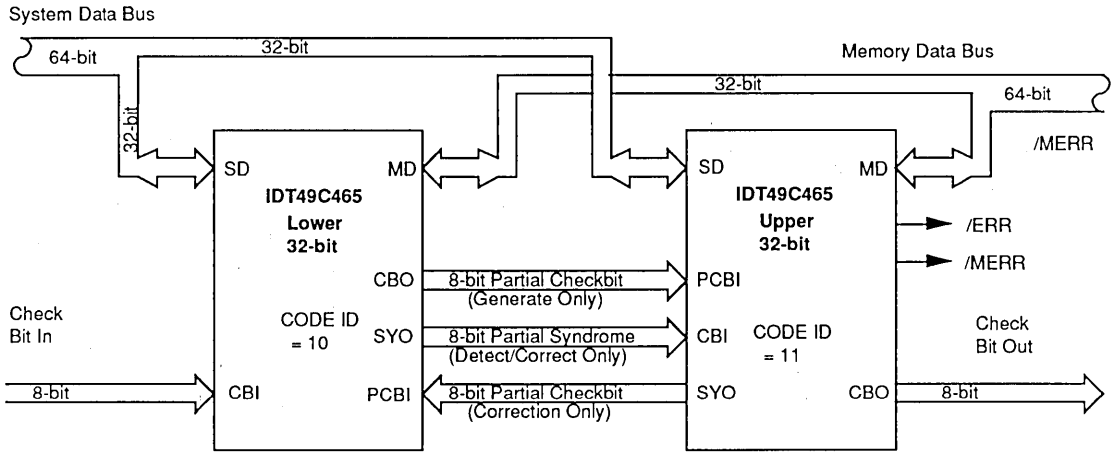
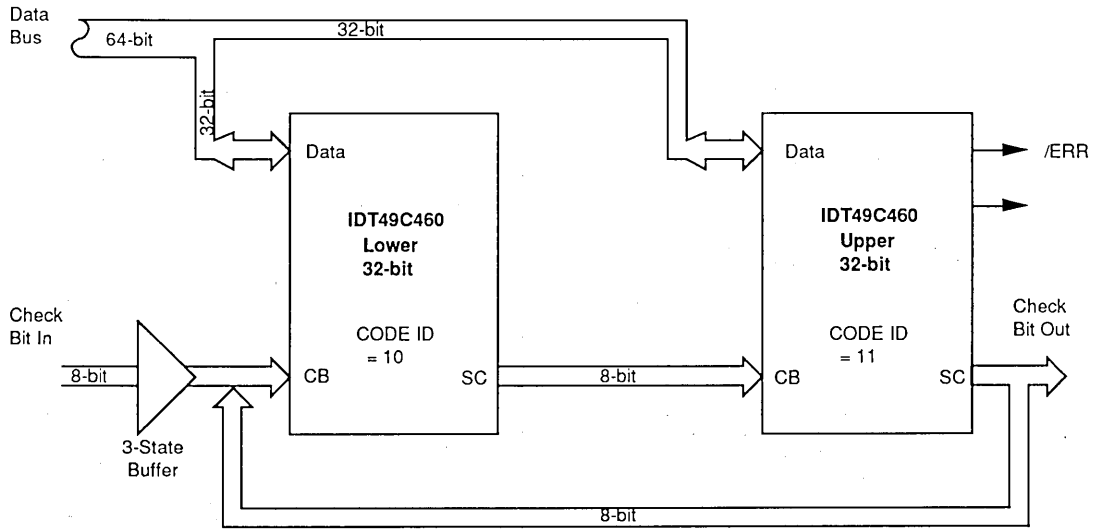


(a) Cascading Flow-thru EDC IDT49C465



(b) Cascading Bus-watch EDC IDT49C460

Figure 5. 64-bit Configurations by Cascading Two 32-bit EDC Units

BUS-WATCH ARCHITECTURE

A bus-watch EDC such as the IDT49C460 has a single data bus. The basic configurations, using the IDT49C460 for common I/O memory and separate I/O memory, are illustrated in Figure 3.

During a write (store) operation, the CPU sends data to the main memory. At the same time the data goes to the EDC unit, which then generates the check bits and stores them in the check-bit memory.

On the other hand, during a read (load) operation, the data from the main memory and the check bits from the check-bit memory first go to the EDC unit. Based on the information carried by the check bits, the EDC unit can detect all single-bit and some multiple-bit errors, and correct all single-bit errors. The corrected data is then sent to the CPU.

FLOW-THRU ARCHITECTURE

In contrast to a bus-watch EDC, a flow-thru EDC such as the IDT49C465 provides two data buses: a system data (SD) bus and a memory data (MD) bus. The dual-bus architecture improves the throughput of the EDC operation and simplifies the interface between the CPU system bus and the memory bus. The basic configurations using the IDT49C465 for common I/O memory and separate I/O memory are illustrated in Figure 4.

In the common I/O configuration, during a write (store) operation, the data from CPU flows through the EDC unit and is written to the main memory. When the data flows through the EDC, the check bits are generated and stored into the check-bit memory. During a read (load) operation, the data from the main memory enters the EDC unit through the MD bus while the check bits enter the EDC unit through the CBI bus. The EDC unit then detects any errors and loads the corrected data to the CPU through the SD bus.

In the separate I/O configuration, during a write (store) operation, the data from CPU are directly sent to the main memory. At the same time, the data is sent to the EDC unit through the SD bus. The EDC unit then generates the check bits and stores them into the check-bit memory. During a read (load) operation, the data from the main memory enters the EDC unit through the MD bus while the check bits enter the EDC unit through the CBI bus. The EDC unit then detects any errors and loads the corrected data to the CPU through the SD bus.

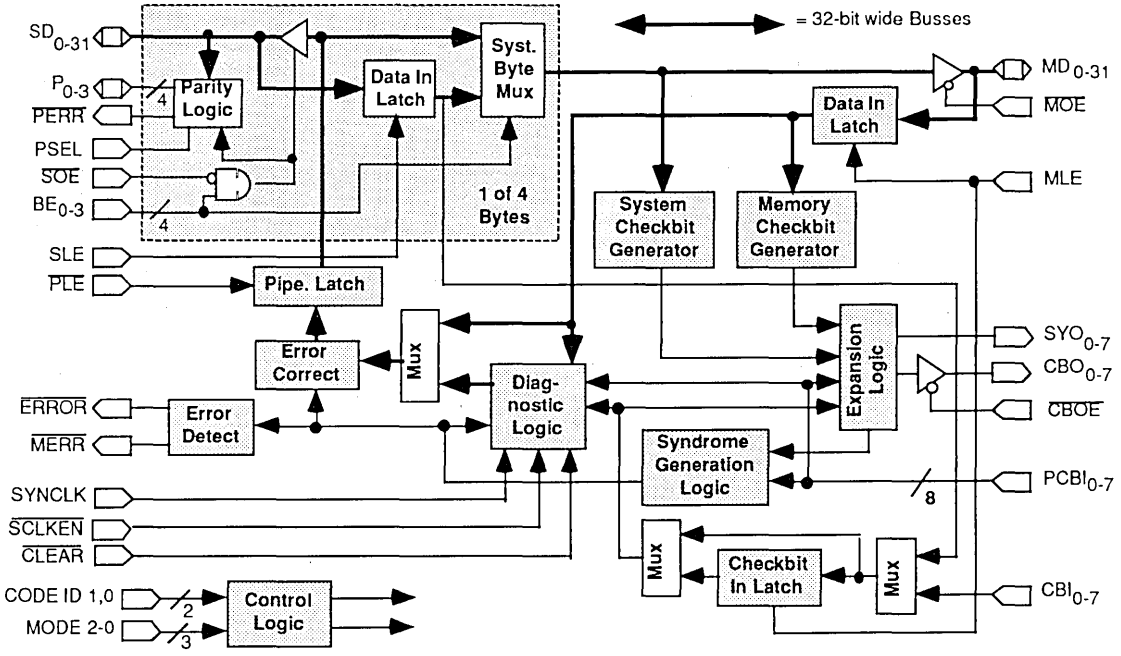


Figure 6. Block Diagram of IDT49C465

CASCADING 32-BIT EDC DEVICES FOR 64-BIT MEMORY SYSTEMS

As mentioned in the previous section, for a 32-bit data word, 7 check bits are necessary, while for a 64-bit data word, 8 check bits are needed. Although the IDT49C460 and the IDT49C465 are both 32-bit EDC units, they have an **8-bit output-bus** for output of generated check-bits to memory and an **8-bit input bus** to read back check-bit from memory. In this way, they can be cascaded to support 64-bit applications. In the 32-bit mode, only 7 bits of the check-bit input and output buses are used, while in the 64-bit mode, all 8 bits are used.

Figure 5 shows how two IDT49C465s (or two IDT49C460s) can be cascaded to build a complete 64-bit EDC unit. In the cascaded 64-bit mode, the EDC operation can be broken into two stages; a **lower 32-bit** stage and an **upper 32-bit** stage.

For the IDT49C465 (see Figure 5a), a general description of the EDC operation is discussed below.

1. Generation starts by generating a **Partially Generated Check-bit Word** in the lower slice, based on the lower 32-bit of the 64-bit data-word, and sending this to the upper slice. The upper slice combines the Partially Generated Check-bit word from the lower slice, with its generated check-bit word (based on the upper 32-bit of the 64-bit data-word), to form a final check-bit word. Thus, the source of check-bit in a cascaded system is the upper-slice device.
2. Detection/Correction starts in the **lower-slice** where the check-bits from memory are input, as well as the lower 32-bit of the 64-bit data-word. Here the inputted check-bits are compared with the newly generated check-bits (based on the lower 32-bit of DATA-word) using an XOR function to produce a **Partial Syndrome Word,** which is passed onto the upper-slice device. At the same time, in the upper slice the upper 32-bits of 64-bit data-word is used to generated a so-called **Partial Check-Bit Word** which is sent to the lower slice. So now we have in both the upper and lower slice devices almost simultaneously two pieces of data; **the Partial Syndrome Word** (generated in the lower-slice) and the **Partial Check-Bit Word** (generated in the upper-slice). In each slice these two pieces of data are XOR'd to produce a **Final Syndrome Word** which is used to detect and correct errors on the 64-bit data word.

The IDT49C460 carries out Detect/Correct slightly differently (see Figure 5b), namely, the Partial Syndrome generated in the lower-slice is sent to the upper slice, then the Final Syndrome is generated in the upper-slice and this Final-Syndrome is now fed back to the lower-slice. Thus Detect/Correct in the IDT49C460 employs a serial approach, whereas the IDT49C465 uses a faster paralleled approach. Moreover, in the IDT49C460 case, an additional tri-state buffer such as the IDT74FCT244 is needed while in the IDT49C465 case, no additional external logic is needed.

OVERVIEW OF THE IDT49C465 ARCHITECTURE

The IDT49C465 architecture is an evolutionary development on the IDT49C460 EDC device. The IDT49C460 is a single-bus 32-bit EDC cascadable to 64-bits. The IDT49C465 draws on this basic architecture to provide a dual-bus or flow-Thru 32-bit EDC cascadable to 64-bits. Figure 6 shows a block diagram of the IDT49C465; the key difference between the IDT49C460 and the IDT49C465 is the presence of a second 32-bit DATA bus to provide the flow-thru path for data through the device.

DATA BUSES

The System Data Bus, or **SD Bus,** is a 32-bit bi-directional bus. Data is written to the EDC using this bus for **Check-Bit Generation,** so that when a data-word is written to memory the corresponding check-bits are written simultaneously. Also when a data-word read from memory is corrected, the corrected data-word is read from the SD Bus by the system processor. The SD Bus has associated with parity-checking and generation and also separate byte enables on the SD Bus' output buffers so that Partial Byte operations can be supported.

The Memory Data Bus, or **MD Bus,** is a 32-bit bi-directional bus. Data written from the system processor through the SD Bus can be written to memory using this bus. When the processor is reading a word from memory, the data word is read in through the MD Bus and the corrected data word (depending on the status of the data) is sent to the processor through the SD Bus.

EXPANSION BUSES

The IDT49C465 has four 8-bit buses that are an integral part in the Detect/Correct path for both a 32-bit EDC system and a 64-bit EDC system.

CBI(7:0)

1. When the IDT49C465 is operating as a 32-bit EDC system or is the lower 32-bit slice in a 64-bit EDC system, this 8-bit bus is the input port for Check-Bits read from Memory.
2. When the IDT49C465 is operating as the upper 32-bit slice in a 64-bit EDC system, this bus is the input port for partial Syndromes from the lower slice.

PCBI(7:0)

1. When the IDT49C465 is operating as a 32-bit EDC system, this bus is unused .
2. When the IDT49C465 is operating as the lower 32-bit slice in a 64-bit EDC system, this 8-bit bus is the input port for Partial Check-Bits read from the upper slice.
3. When the IDT49C465 is operating as the upper 32-bit slice in a 64-bit EDC system, this bus is the input port for Partially Generated Check-Bits from the lower slice.

CBO(7:0)

1. When the IDT49C465 is operating as a 32-bit EDC system or is the upper 32-bit slice in a 64-bit EDC system, this 8-bit bus is the output port for Check-Bits being written to Memory
2. When the IDT49C465 is operating as the lower 32-bit slice in a 64-bit EDC system, this bus is the output port for Partially Generated Check-bits being sent to the upper slice.

SYO(7:0)

1. When the IDT49C465 is operating as a 32-bit EDC system, this 8-bit bus outputs the Final Syndrome word associated with the Detect/Correct logic.
2. When the IDT49C465 is operating as the lower 32-bit slice in a 64-bit EDC system, this bus is the output port for Partial Syndrome word being sent to the upper slice.
3. When the IDT49C465 is operating as the upper 32-bit slice in a 64-bit EDC system, this bus is the output port for Partial Check-bit word being sent to the lower slice.

Operating Modes

The IDT49C465 has 3 mode control pins, MODEID(2:0), which enable the user to select which mode the part is operating in. These modes are summarized in Table 2.

	MODE DESCRIPTION
000	ERROR DATE MODE
X01	DIAGNOSTIC OUTPUT MODE
X10	GENERATE-DETECT MODE
100	CHECK-BIT INJECTION MODE
X11	NORMAL OPERATING MODE

Table 2. IDT49C465 Operating Modes

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ERROR DATA MODE (000) :

In this mode the contents of the Error-Data Register are output uncorrected on the SD Bus. The Error-Data Register is a 32-bit register which gets latched under the following conditions: 1. an error condition has been detected by the EDC-$\overline{\text{ERROR}}$) and is asserted low, 2. the on-chip 4-bit Error-Counter reads zero 0000 (i.e. no error has occurred since the last clear operation), 3. the input signal, $\overline{\text{SCLKEN}}$), is held low so that the diagnostic clock, SYNCLK, is enabled, 4. the diagnostic clock, SYNCLK, undergoes a LOW-to-HIGH transition.

Data is latched into the Error-Data Register from the output of the Memory Data Latch when and only when these conditions are met. Thus, the Error Data Register contains the Memory Data word corresponding to the first error since a clear operation (assuming SYNCLK has been run continuously). If the Error Data Register has just been cleared, then output of the contents of this register will provide a source of zero-data if that is required.

DIAGNOSTIC OUTPUT MODE (X01) :

In this mode a 32-bit Diagnostic Word is output on the SD Bus. The structure of this word is outlined in Figure 7.

BITS 0:7 The output of the check-bit multiplexer is output directly on the SD Bus at these positions (LSB at bit 0 and MSB at bit 7).

BIT 8:15 Whatever is being forced on the PCBI(7:0) input pins is output on the SD Bus at these positions (LSB at bit 8 MSB at bit 15).

BIT16:23 The contents of the Syndrome Register, which is an 8-bit register within the Diagnostic Unit, is output on the SD Bus at these positions (LSB at bit 16, MSB at bit 23). The Syndrome Register gets latched at the same time as the Error Data Register and contains the Final Syndrome corresponding to the first error to occur since a clear operation.

BIT 24:27 The contents of the on-chip 4-bit Error-Counter are output on the SD Bus at these positions (LSB at bit 23 and MSB at bit 27). The Error-Counter which gets clocked under the following conditions: 1. An error condition has been detected by the EDC, i.e. xto(ERROR) is asserted low, 2. the on-chip 4-bit Error Counter does not read 1111 (or F HEX), therefore, not more than 16 errors have occurred since the last clear operation, 3. the input signal, xto(SCLKEN), is held low so that the diagnostic clock, SYNCLK is enabled and 4. the diagnostic clock, SYNCLK, undergoes a LOW-to-HIGH transition.

The Error Counter will tell the number of errors that have occurred since the last clear operation.

BIT28:29 Reserved

BIT30:31 The contents of the Error Signal Register, which is a 2-bit register is output on the SD Bus at these positions (SB at bit 30 and MSB at bit 31). Bit 0 and bit 1 of the register are set if a Multiple Error has been flagged and bit 1 only is set if a Single Error has been flagged at the same time and under the same conditions as the Error Data and Syndrome Registers are latched.

Error Type	Test	Error Counter	Syndrome Bits Register Contents	Partial Checkbits from Input Pins	Checkbits
Byte 3			Byte 2	Byte 1	Byte 0

M	S	—	—	2^3	2^2	2^1	2^0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
31			28	27			24	23							16	15							8	7							

Figure 7. Output Syndrome/Diagnostic Word

GENERATE-DETECT MODE (X10) :

In this mode, detection and generation take place but no correction. Data whether correct or not, passes thru the device from the MD Bus to the SD Bus.

NORMAL OPERATING MODE (X11) :

This is the mode where normal detection/correction and generation takes place for a single-slice device (32-bit EDC system) or for the upper and lower slices in a cascaded 64-bit EDC system.

CHECK-BIT INJECTION MODE (100) :

In this mode the check-bit multiplexer enables bits 0:7 from the output of the System Data Latch to be fed into the EDC as a check-bit input, normal correction is activated. This is a very useful capability for carrying out a diagnostic check on the detect/correct path of the EDC.

PARITY FOR THE SYSTEM BUS

The IDT49C465 supports byte parity on the SD Bus, with the polarity of the parity (even or odd) selectable using the input pin PSEL. If PSEL is low, then parity (both checking and generation) will be even. If SPSEL is high, then parity will be odd. The part has 4 parity I/O lines one for each byte of the SD Bus and a parity error signal, $\overline{PERR}$), which flags a parity error on in-coming data by being asserted low.

PARTIAL BYTE WRITE AND READ-MODIFY-WRITE CAPABILITY

The IDT49C465 supports, through a number of features, **Partial Byte Writes** and **Read-Modify-Writes** cycles. Firstly the SD Bus has 4 Byte Enable signals associated with it, **BE(3:0),** these input lines provide, in conjunction with $\overline{SOE}$), separate output enable control on each byte of SD bus data. The BE bus is also the control input to the Sys-Byte-Mux, this mux enables mixing on a byte-by-byte basis of data from the SD latch (A input to mux) and from the Pipe-Line latch (B input to mux). So, for example, if the processor wanted to do a Partial Write or Partial Store of a byte (byte position 3) to a memory location byte position 3 the following sequence would occur: (1) read the memory location in question through the MD Bus and correct if possible or necessary. The corrected data-word will be latched into the Pipe-Line latch, (2) the byte to be written is latched into the SD Latch at byte position 3, all other byte are undetermined, (3) Now we have both pieces of data necessary to construct the 32-bit word to be written to memory and (4) BE(3) is held low and all other BEs are held high. Thus the output of the Sys-byte-Mux is the correctly constructed 32-bit word which is then written to memory through the MD Bus with it's corresponding check-bits.

64-BIT GENERATE

A very useful and ultimately cost-saving measure associated with the IDT49C465, is its 64-bit generate mode. If the CODE ID of the IDT49C465 is set at 01, the part is configured as a single-slice 64-bit generate EDC. While operating in this mode, the lower 32-bit of the 64-bit data word is input on the MD bus pins and the upper 32-bit of the 64-bit data word is input on the SD bus. The 8-bit generated check bits are output on the CBO bus. In 64-bit generate mode, the EDC is dedicated to check-bit generation, all other features are disabled.

Because the 64-bit generate is executed in a single slice, very fast generate speed can be achieved (15ns as opposed to 30ns in a two-slice 64-bit cascaded system). This feature can also help reduce part count. In 64-bit memory systems, it is common to use 4 32-bit EDC devices; 2 for detect/correct and 2 for generate. With the 64-bit generate capability, this part count is reduced from four to three.

WHY FLOW-THRU EDC

To fully understand the advantages of the IDT49C465 flow-thru EDC over the IDT49C460 bus-watch EDC, it is necessary to first know the architectural differences between the IDT49C465 and the IDT49C460. Figure 8 compares the simplified internal architectures of the two chips. As compared with the IDT49C460, the IDT49C465 has the following unique features:

- Dual data buses
- Dual check-bit generators: one for SD Bus and the other for MD bus
- Independent check-bit generation path
- Independent error detection/correction path
- Dedicated syndrome output
- Dedicated check-bit output
- Output pipeline latch
- Parity check/generation

These features greatly simplify the interface of the EDC unit with the system data bus and the memory data bus, and thus can considerably improve the system performance. Generally speaking, in a single bus EDC architecture like the IDT49C460, the data bus connects to both the processor and the memory system. Thus, in a normal correction cycle, data is read into the EDC from memory through the data bus, and the data is corrected. Then, the data bus is enabled as an output and the corrected data is sent to the processor. Therefore, during a correction cycle, the data bus must be turned around from being an input to being an output. Consequently, a single bus architecture has inherent delays associated with the enable/disable times of the data bus output buffer. On the other hand, separate data buses, as in the IDT49C465, allow us to dedicate buses to a specific direction of data flow and, as such, is a superior architecture.

In a 32-bit system using common I/O memory, the dual bus architecture of the IDT49C465 allows direct interface of the flow-thru EDC unit with the system data bus and the memory data bus, as shown in Figure 4a. On the other hand, if the IDT49C460 is used, then two sets of transceivers are needed to buffer both system data bus and memory data bus to the single data bus of the IDT49C460, as shown in Figure 3a.

Similarly, in a 32-bit system using separate I/O memory, the dual bus architecture of the IDT49C465 allows direct interface of the flow-thru EDC unit with the memory data bus. Only a single set of transceivers is used to connect the CPU

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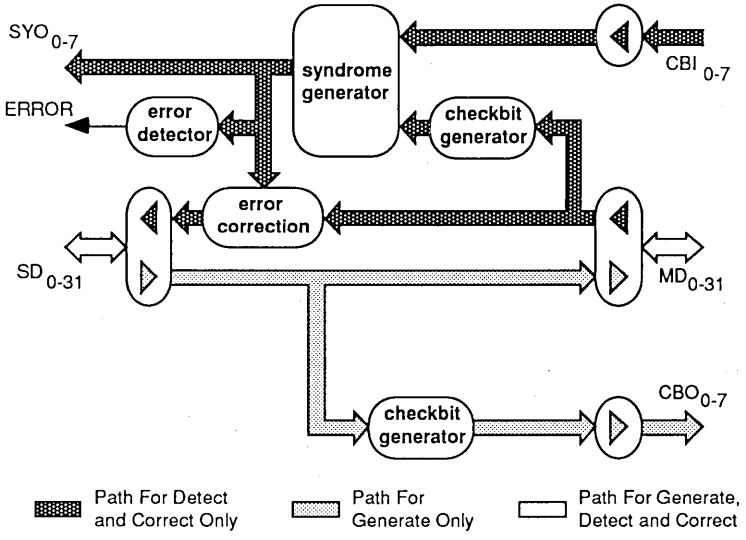
system data bus to the EDC unit, as shown in Figure 4b. On the other hand, if the IDT49C460 is used, then a set of transceivers and a set of buffers are needed to hook up both system data bus and memory data bus with the single data bus of the IDT49C460.

In particular, the multi-bus architecture and the independent error generation and detection/correction paths of the IDT49C465 provide significant performance improvement in a 64-bit system using two cascaded EDC units. Figure 9 shows the internal data paths of cascaded IDT49C465s and cascaded IDT49C460s during a read (error detect/correct) operation. In the IDT49C465 case, the entire error detect/correct path can be divided into two steps. In the first step, the lower 32-bit unit generates the partial check bits from the lower 32-bit data, and then compares the partial check bits with the original check bits to generate the partial syndrome bits. At the same time, the upper 32-bit unit generates the partial check bits from the upper 32-bit data. Then, the partial syndrome bits from the lower unit and the partial check bits from the upper unit are exchanged between the two units. In the second step, both lower and upper units generate the final syndrome bits independently and then correct errors in the lower 32-bit data and the upper 32-bit data, respectively, in parallel. Therefore, the total delay time is the sum of MD-to-SYO plus CBI-to-SD. On the other hand, in the IDT49C460 case, the entire error detect/correct path can be divided into three steps. In the first step, like in the IDT49C465 case, the lower 32-bit unit generates the partial check bits from the lower 32-bit data, and then compares the partial check bits with the original check bits to generate the partial syndrome bits. At the same time, the upper 32-bit unit generates the partial check bits from the upper 32-bit data. However, in contrast to the IDT49C465 case, only the partial syndrome bits from the lower unit are sent to the upper unit. In the second step, the upper unit compares the partial check bits from the upper 32-bit data with the partial syndrome bits from the lower unit to generate the final syndrome bits. Then, the final syndrome bits are sent back to the lower unit. Finally, in the third step, the lower unit and the upper unit correct the errors in the lower 32-bit data and the upper 32-bit data, respectively. Consequently, the total delay time is the sum of DATA-to-SC plus BC-to-SC plus CB-to-DATA, which is much longer than the delay in the IDT49C465 case. Moreover, since the IDT49C460 has only one check bit input bus, an external octal tri-state buffer is needed to multiplex the original check bits and the partial check bits.

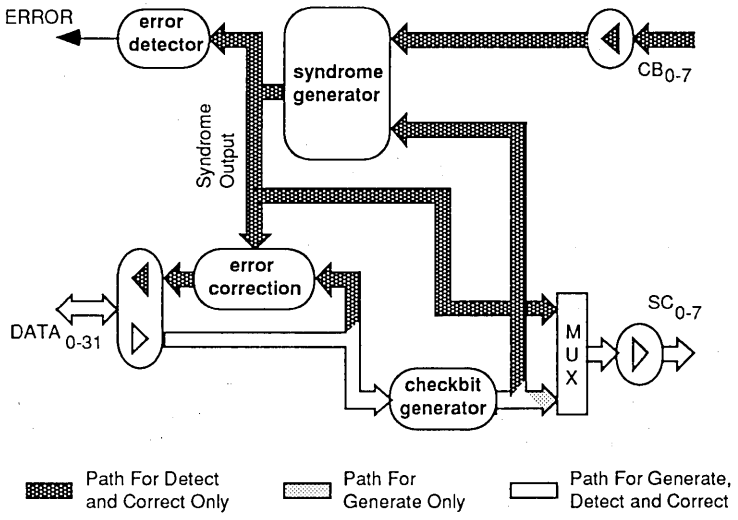
Based on the above discussion, Table 3 summarizes the performance comparison between the IDT49C465 and the IDT49C460D, the fastest version of the IDT49C460. It can be seen that in most situations, the IDT49C465 has significant speed advantage over the IDT49C460.



Features Of IDT49C465

- Dual Data Bus Architecture
- Dual CheckBit(CB) Generators
- Independent CB Generate Path
- Independent Error Detect/Correct Path
- Dedicated Syndrome Output
- Dedicated CB Output
- Output Pipeline Latch
- Parity Check/Generate
- 1 Off-chip Feedback for 64-bit Error Correct
- 144-pin PGA

(a) Simplified Block Diagram of IDT49C465 EDC Unit



Features Of IDT49C460

- Single Data Bus Architecture
- Single Checkbit Generator
- Shared Syndrome and CB Output
- 2 off-chip Feedback for 64-bit Error Correct
- 68-pin PGA

(b) Simplified Block Diagram of IDT49C460 EDC Unit

Figure 8. Internal Architecture Differences Between IDT49C465 and IDT49C460

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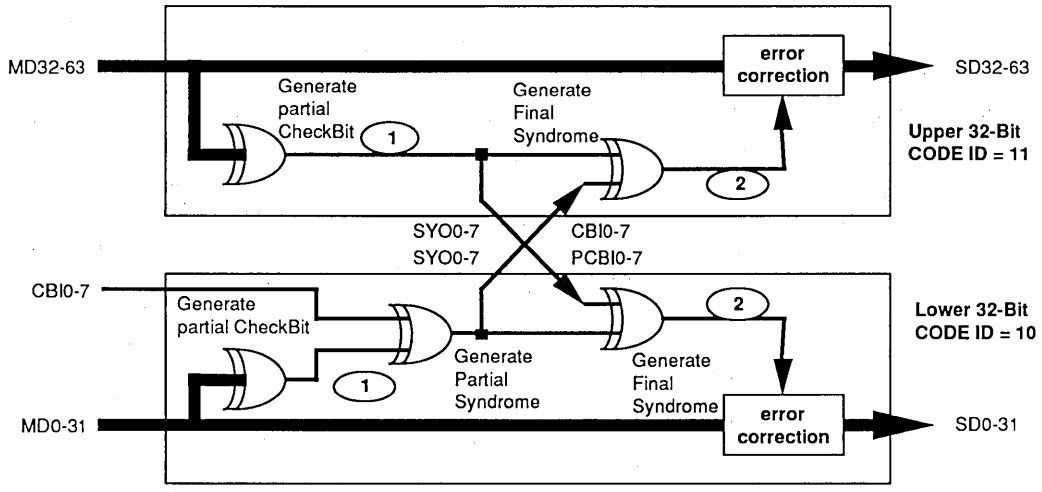
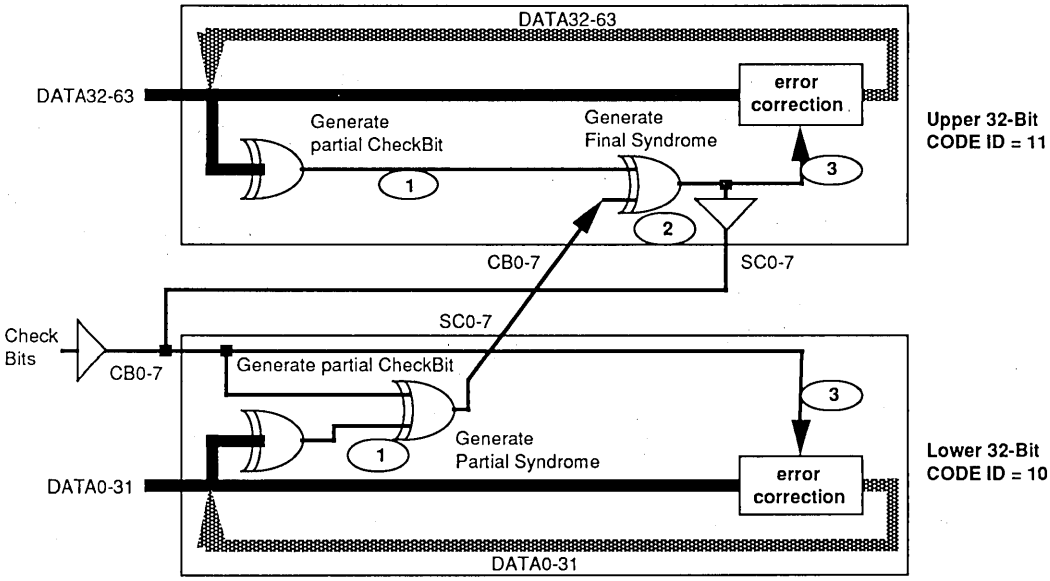


(a) 64-bit Error Detect/Correct Path of Cascading IDT49C465



(b) 64-bit Error Detect/Correct Path of Cascading IDT49C460

Figure 9. Comparison of 64-bit Error Detect/Correct Path Between IDT49C465 and IDT49C460

	Common I/O				Separate I/O			
	32-bit		64-bit Cascade		32-bit		64-bit Cascade	
	Read [1]	Write	Read [1]	Write	Read [1]	Write	Read [1]	Write
IDT49C 465	MD->SD 20ns 20ns *40% Faster*	SD->CBO 15ns 15ns *26% Faster*	MD->SYO 15ns CBI->SD 20ns 35ns *34% Faster*	SD->CBO 15ns PCBI->CBO 15ns 30ns	MD->SD 20ns FCT245[2] 5ns 25ns *12% Faster*	FCT245[2] 5ns SD->CBO 15ns 20ns	MD->SYO 15ns CBI->SD 20ns FCT245[2] 5ns 40ns *18% Faster*	FCT245[2] 5ns SD->CBO 15ns PCBI->CBO 15ns 35ns
IDT49C 460D	28ns FCT245[2] 5ns D->D 18ns FCT245[2] 5ns	19ns FCT245[2] 5ns D->SC 14ns	47ns FCT245[2] 5ns D->SC 14ns CB->SC 11ns CB->D 12ns FCT245[2] 5ns	30ns FCT245[2] 5ns D->SC 14ns CB->SC 11ns	28ns FCT245[2] 5ns D->D 18ns FCT245[2] 5ns	19ns FCT245[2] 5ns D->SC 14ns	47ns FCT245[2] 5ns D->SC 14ns CB->SC 11ns CB->D 12ns FCT245[2] 5ns	30ns FCT245[2] 5ns D->SC 14ns CB->SC 11ns

NOTES:
1. The EDC units perform correction always.
2. FCT245 is high-speed bidirectional transceiver.

Table 3. Performance Comparison

CONCLUSIONS

Whether designing a correct always (flow-thru) EDC or bus-watch EDC memory systems, IDT offers a high performance solution for keeping memories error free. The key system benefit for using EDC is the continuous system operation, even with hard or soft errors occur. The key benefit for using a flow-thru EDC is the reduced memory design time when performing the correct always function, and improved performance for 64-bit memory systems.

Integrated Device Technology, Inc.

USING IDT73200 OR IDT73210 AS READ AND WRITE BUFFERS WITH R3000

APPLICATION NOTE AN-65

CONTENTS

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Integrated Device Technology, Inc.

USING THE IDT73200 MULTILEVEL PIPELINE REGISTERS AS READ AND WRITE BUFFERS WITH R3000/1

APPLICATION NOTE AN-65A

By Danh Le Ngoc, Ignacio Osorio and Avigdor Willenz

INTRODUCTION

The objective of this application note is to describe the use of the IDT 73200 multilevel pipeline register as the write buffer and read buffer for the R3000/1 RISC processor. The following topics are discussed:

- **The IDT73200 Multilevel Pipeline Register**, presents a brief description of general characteristics and configura tions of the multilevel pipeline register.
- **Read-Write buffers**, explains what read and write buffers are, and how they function in a R3000/1 system.
- **Implementing R-W Buffers**, describes how to implement the IDT73200 as read and write buffers. Buffer depths are also discussed in this section.
- **A Typical System**, provides an example of read-write buffers using the IDT73200, within a RISC system. It also presents the control logic and PAL equations to operate the IDT73200 as read and write buffers.

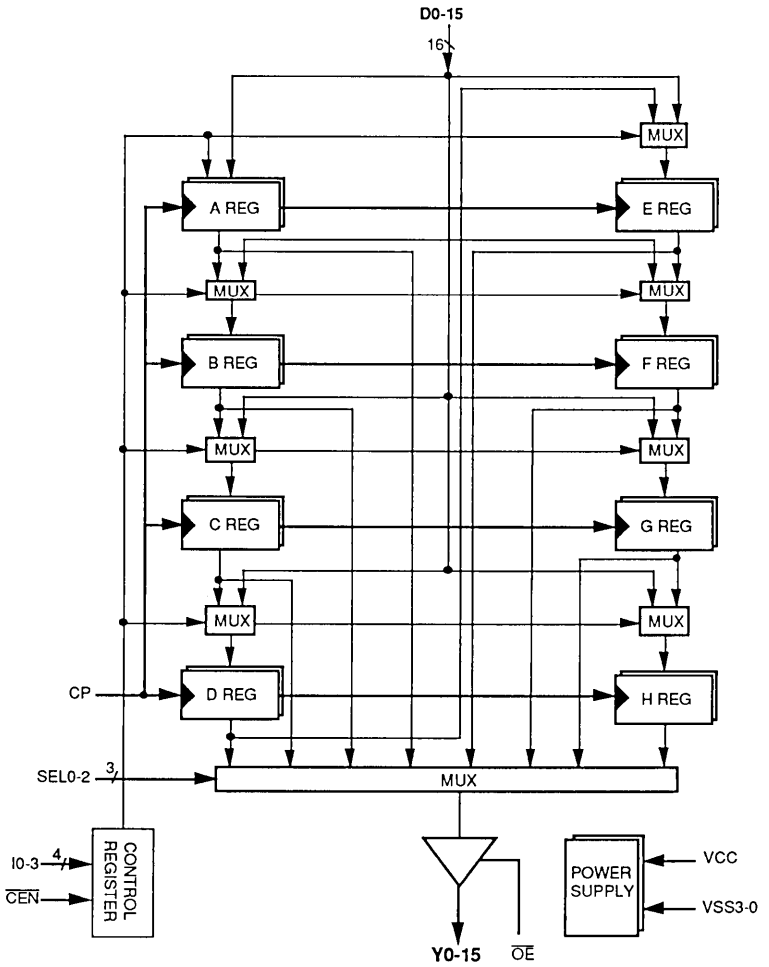

Figure 1. Block Diagram of the IDT73200

I3	I2	I1	I0	MNEMONIC	FUNCTION	PIPELINE LEVEL
0	0	0	0	LDA	D0-15->A	1
0	0	0	1	LDB	D0-15->B	1
0	0	1	0	LDC	D0-15->C	1
0	0	1	1	LDD	D0-15->D	1
0	1	0	0	LDE	D0-15->E	1
0	1	0	1	LDF	D0-15->F	1
0	1	1	0	LDG	D0-15->G	1
0	1	1	1	LDH	D0-15->H	1
1	0	0	0	LSHAH	D0-15->A->B->C->D->E->F->G->H	8
1	0	0	1	LSHAD	D0-15->A->B->C->D	4
1	0	1	0	LSHEH	D0-15->E->F->G->H	4
1	0	1	1	LSHAB	D0-15->A->B	2
1	1	0	0	LSHCD	D0-15->C->D	2
1	1	0	1	LSHEF	D0-15->E->F	2
1	1	1	0	LSHGH	D0-15->G->H	2
1	1	1	1	HOLD	HOLD ALL REGISTERS	

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Figure 2. Load Control

THE IDT 73200 MULTILEVEL PIPELINE REGISTER

The IDT 73200 is a high-speed, low-power Programmable Multilevel Pipeline Register. It has a dedicated 16-bit input port and a dedicated 16-bit output port.

As shown in figure 1, the IDT73200 contains eight 16-bit registers which can be configured as one 8-level, two 4-level, four 2-level, or eight 1-level pipeline registers. Data at the input port D0-15 can be written into any of the eight registers under control of the load control: I0-3. Figure 2 illustrates the load control for the input port .

An eight-to-one output multiplexer allows data to be read on the Y-bus from any of the eight registers using the output-selection control: S0-2. Figure 3 illustrates the output control.

READ-WRITE BUFFERS

As shown in the Figure 4 , a high-speed computer system consists of a R3000/1 chip set, high-speed cache, write buffer, read buffer , I/O devices, and main memory. Since the main processor supports a write-through cache policy, all data written into the data cache must also be written into the main memory to maintain the cache coherency. Due to the data-rate mismatch between the high-speed processor bus (33MHz -> 240Mbytes/sec) and slow speed main memory (10-15MHz ->10-40 Mbytes/sec), a write buffer and a read-buffer are required. The write buffer is an elastic buffer which is used to capture addresses and data at the cache speed. At the other side of the write buffer, data is transfered into the main memory at the system memory speed.

When a load operation causes a cache miss, a main memory read is initiated. Two types of main memory read are supported on the R3000/1: single word transfer and multiple word transfer. In either case, a read-buffer is used to capture data from the system memory at memory speed. Then data is written into the cache at the cache speed. The depth of the write buffer and the read-buffer are dependent on different factors such as processor speed, system memory speed, bus protocol and the application.

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SEL2	SEL1	SEL0	Y OUTPUT
0	0	0	A REG
0	0	1	B REG
0	1	0	C REG
0	1	1	D REG
1	0	0	E REG
1	0	1	F REG
1	1	0	G REG
1	1	1	H REG

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Figure 3. Output Selection

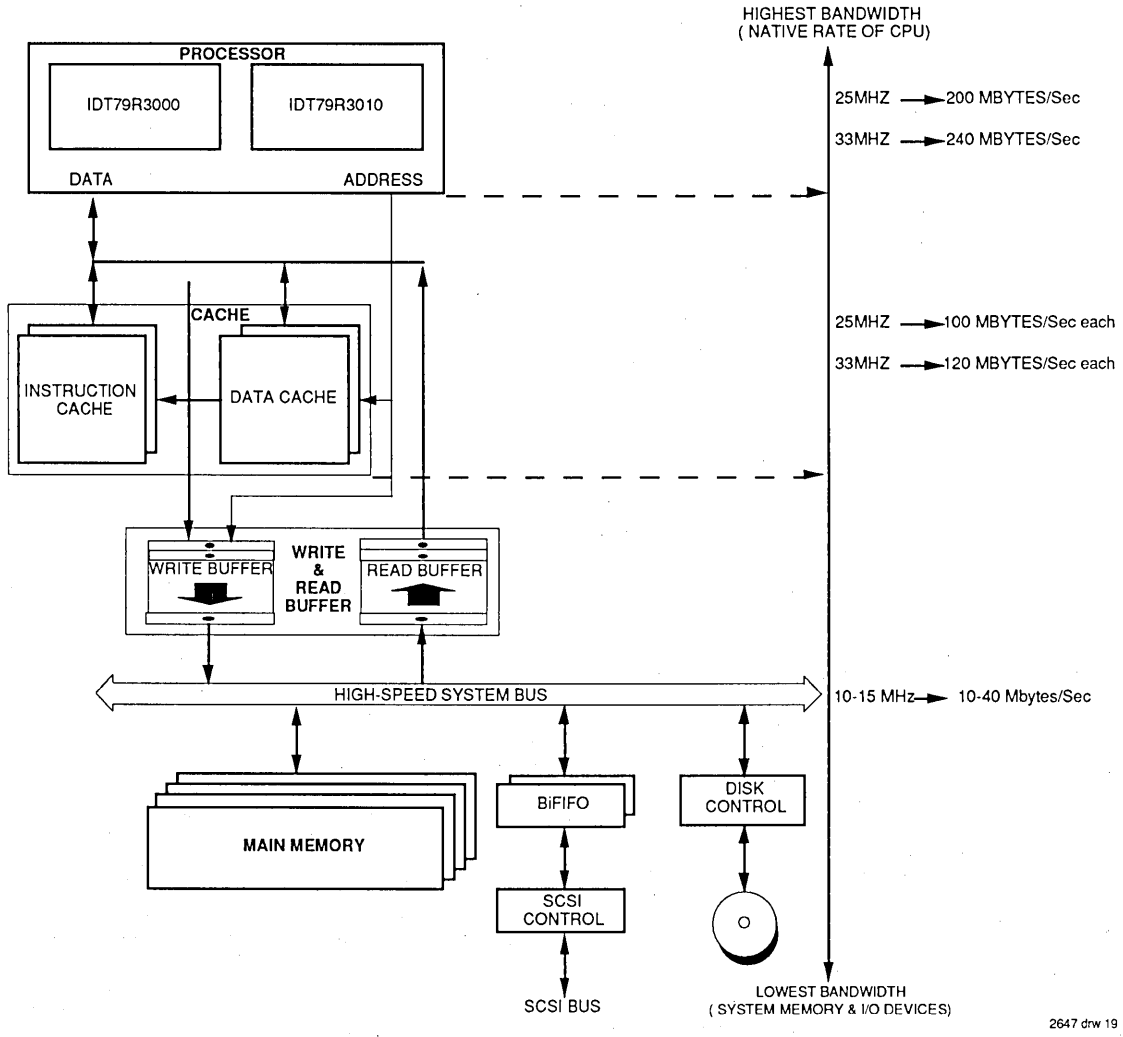

Figure 4. Simplified Block Diagram of a High-Speed RISC System

IMPLEMENTING R-W BUFFERS

As previously described in section 1, the IDT 73200 is like a high-speed synchronous memory with a depth that is programmable from 1 to 8 deep. Therefore, a write buffer and read buffer for the high performance R3000/1 system can be easily implemented with the help of the IDT 73200.

Figure 5 illustrates a detailed R3000/1 system which consists of the R3000/1 chip set, write buffer, read buffer, IDT49C465 Flow-thruEDC™, system main memory, and several state machines to control the main memory interface. In this scheme, the data bits together with the parity bits flow from the main memory through the EDC device for error detection and correction. When an error is detected, the EDC informs the read buffer control through an error feedback path.

In figure 5 the write buffer consists of two paths: address and data. The address path (34-bit) is created with three IDT 73200s to capture the address, tag, and the access type bits. The data path of the write buffer (32-bit), is formed by two IDT73200. Data coming from the CPU is buffered into the "data path" write buffer prior to being written into the main memory.

The read buffer in figure 5 consists only of a "data path" (36-bits) which includes the required data parity on the R3000/1 system. The IDT 49C465 high speed Flow-thruEDC can be used to maintain the data integrity of the system main memory. Also, parity bits are generated with the help of the IDT49C465 Flow-thruEDC.

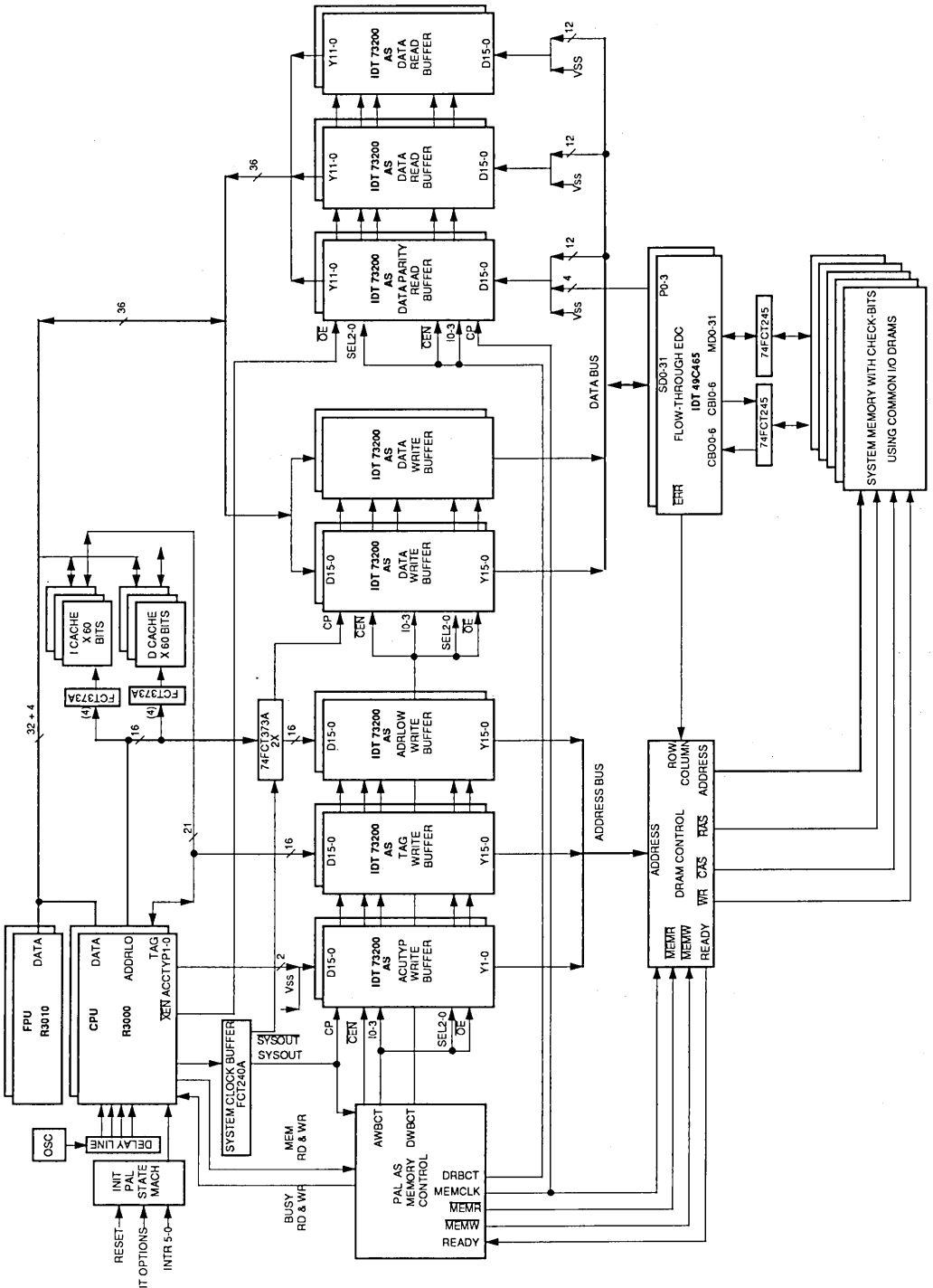

Figure 5. Detailed R3000 System with Read and Write Buffer

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BUFFER DEPTH

As discussed earlier, the IDT 73200 can be configured for different depths: eight 1-level, four 2-level, two 4-level or one 8-level deep registers. This feature makes the 73200 particularly flexible in Read/Write buffer applications.

The depth of the write buffer is programmable using the load-control and the output selection. A single IDT 73200 can be programmed to a buffer depth of 1 to 8. A deeper write buffer can be implemented by cascading several devices in depth as shown in the figure 6. The right depth depends on the application program and/or hardware requirements.

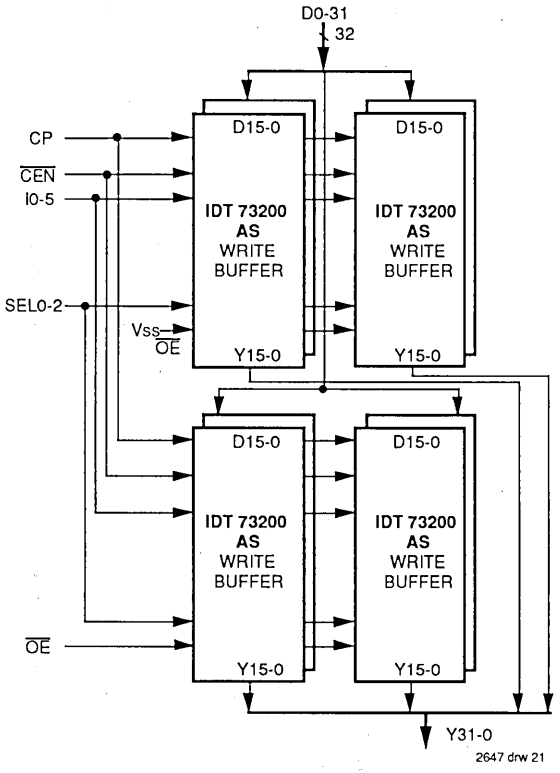

Figure 6. 16-Deep and 32-Wide Write Buffer Using IDT73200s

With the help of the write buffer, the CPU can write to the memory without regard to the memory speed. However, if consecutive (or back to back) write operations take place, the write buffer would eventually become full and cause the CPU to stall. Naturally, this could present a problem in high performance systems. A logical solution to CPU stalls is to increase the depth of the write buffer.

Typical write buffer depths are two and four levels. However, high end applications with intensive memory access may require deeper write buffers, i.e., eight or sixteen levels as shown in figure 6.

Read buffer depth design issues are somewhat different from those of the write buffers. For example, when an I-cache miss occurs we are faced with the question of "how many blocks to refill in the I-cache? " To answer this question, we should recall that the miss rate is determined by the cache size and the block size. Therefore, the block size determines the size of the read buffer. Thus to bring 16 words from memory into the I-cache would require a 16 level deep read buffer.

Fetching small blocks of instructions using a shallow read buffer implies constantly fetching instructions and therefore stalling the CPU for several cycles. Depending on the application, this could impose significant penalty on system performance. Due to program locality (sequentiality of instructions), we would benefit most by fetching a large block. Deep read buffers for I-cache are therefore an appealing solution. Typical read buffer depths are 4 levels; high end applications could consider from 8 to 16 levels read buffers.

D-cache fetching, on the other hand, is random in nature and typical schemes prefer a 1-level deep read buffer.

The flexibility of the 73200 allows instantaneous re-configuration when fetching for the I-cache and then for the D-cache. For example, we could have an R3000/1 initialized for 16 words I-cache fetching and 1 word D-cache fetching and still use the same read buffer. This can be accomplished through a read buffer controller capable of configuring the 73200 to different depths.

Lets now discuss two popular read buffer configurations.

a) 1-level deep Read Buffer &
b) 8-level deep Read Buffer

1-LEVEL DEEP READ BUFFER

One-level deep read buffers can be used in high performance systems where the data transfer between the main memory and the CPU is efficiently handled. This can be accomplished through a sophisticated memory scheme, like interleaving, and supported by a fast DRAM architecture. Such a scheme minimizes the transfer rate mismatch between the CPU and the main memory. One-level deep read buffers can also be applied in low performance systems where the penalty in fetching one word at a time is not significant.

8-LEVEL DEEP READ BUFFER

This configuration can be used in a general purpose system. An 8-level deep write buffer offers the benefit of effective data rate capture from the R3000/1 to the main memory. The 8-level Read Buffer is convenient for slow main memory systems.

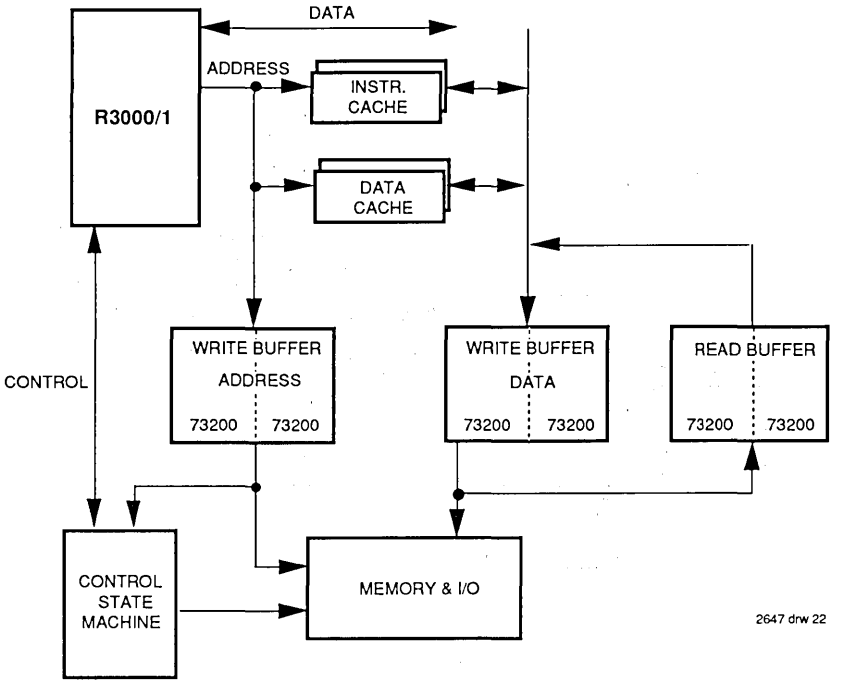

Figure 7. R3000/1 System with the Read-Write Buffers

A TYPICAL SYSTEM

Figure 7 shows the interconnections among the R3000/1, Instruction and Data Cache, Read/Write Buffers, control state machine, and the system memory. The read and write buffers are built from multilevel pipeline registers denoted by the IDT 73200. The control state machine represents the logic needed to drive the read and write buffers.

WRITE BUFFER INTERFACE

A write buffer, as discussed earlier, transfers data from cache to main memory and provides address bits to select memory locations. This is illustrated in Figure 8: one write buffer is dedicated to pass address bits and the other transfers data to the main memory. Therefore, the write buffer labeled "address" is activated in both memory reading and memory writing operations.

As seen in Figure 8, the address path carries address, tag and Acc type bits. Notice that the write buffer labeled "Address", is formed by two IDT 73200. The first 73200 captures Address low 0-13 and AccTyp 0,1. The second 73200 captures Adr High 14-29 and Tag 0,1.

The Data path, as shown in figure 8, carries data and parity bits. The data write buffer uses two IDT 73200. They latch 32 data bits from the cache and transfer them to a memory location selected by a memory controller. Notice that parity bits can be generated using the IDT49C465 when data is flowing from the write buffer to the system memory.

A situation of interest in deep write buffers is the following: The CPU requests reading data from a memory location that is about to be updated by the write buffer. The potential problem is clear: reading data that hasn't been updated yet. To avoid this problem, write buffer systems use conflict checking schemes.

A common "conflict checking scheme" is implemented by comparing addresses of memory locations to be read and written by the read/write buffers. When an address match is found, a match signal is send to the CPU. This solution may involve using more hardware to implement such scheme. Another approach is "flushing". To simplify the design, the write buffer is "flushed", i.e., all pending writings are placed in the main memory before any read buffer operation takes place. Such is the case in figure 8 where no additional hardware was needed.

Figure 8 shows the associated control circuitry to drive the write buffer. Notice that write buffer "data" and AdrHi (14-31) are clocked at the $\overline{\text{SYSOUT}}$ signal, whereas AccTyp (0:1) and adr-Lo(0:13) are clocked at $\overline{\text{SYSOUT}}$.

WRITE BUFFER CONTROLLER

The write buffer controller is internally driven by two counters: The I-counter selects the load operation for the input to the 73200 . The SEL-counter selects the register to be read in the 73200 output. The write buffer controller also takes care of the "flushing" scheme.

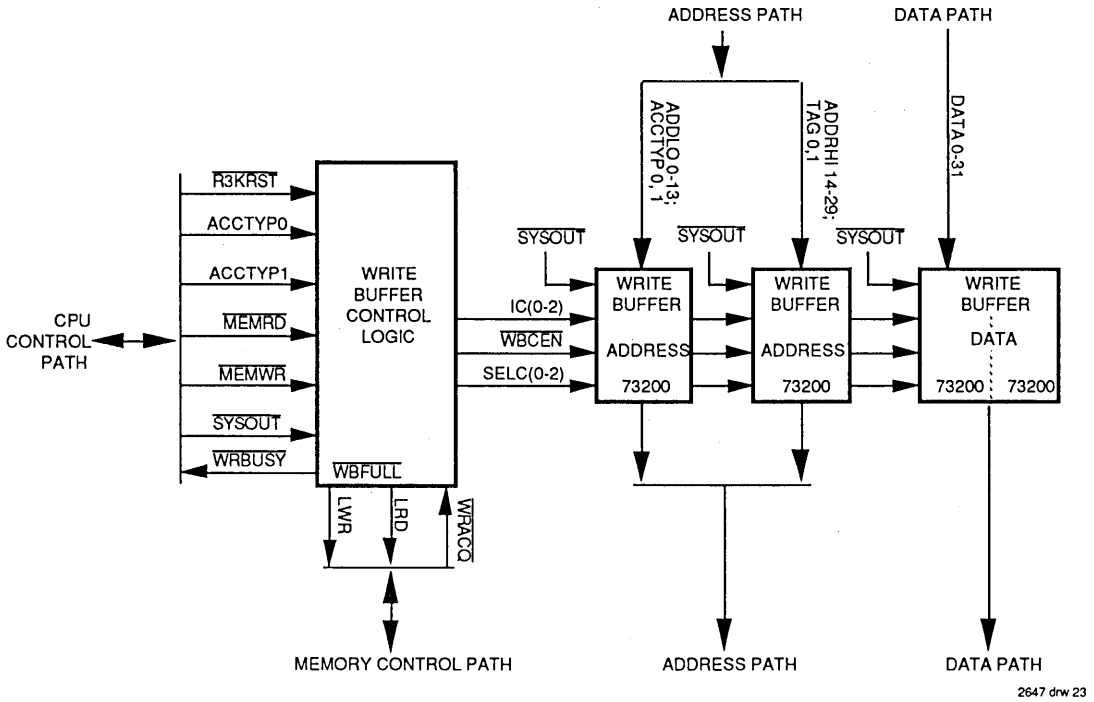

Figure 8. Write Buffer Interface

The PAL equations for the write buffer controller are:

```
MODULE WB_CONT;

TITLE WB_CONT;
TYPE MMI 16R4;
Inputs;
        IC3                     Node[pin2];
        SELC3                   Node[pin3];
        WBEMPTY                 Node[pin4];
        WRACQ                   Node[pin4];
        MEMRD                   Node[pin5];
        WBFULL                  Node[pin6];
        MEMWR                   Node[pin7];
        RESET                   Node[pin9];

        LRD                     Node[pin15];
        LWR                     Node[pin14];

Outputs;
        LRD                     Node[pin15];
        LWR                     Node[pin14];
        X                       Node[pin19];
        WBCEN           Node[pin12];
        ICE             Node[pin13];
        SELCE           Node[pin18];

Table;
        X NOT =         ICE3 XOR SELC3;
        LWR NOT:=       LRD AND WBEMPTY AND WRACQ
                        AND RESET OR LRD AND!MEMWR
                        AND WRACQ AND! WBEMPTY AND
                        RESET;

        LRD NOT :=      (!WBEMPTY AND !MEMRD AND
                        LWR AND RESET) OR (!LRD AND
                        !MEMRD AND RESET);

        WBCEN NOT =     WBFULL;

        ICE NOT =       (!MEMWR AND WBFULL)
                        OR(!MEMRD AND !WBEMPTY);

        SELCE NOT=      (!LWR AND !WRACQ) OR
                        (!LRD AND MEMRD);
END;
END WB_CONT.
```

The PAL equations for the I-counter are:

```
MODULE I-COUNTER;
TITLE I_COUNTER;
TYPE MMI 16R4;

Inputs;
        X               Node[pin2];
        IC              Node[pin3];
        /ICE            Node[pin4];
        /R3KRST         Node[pin5];
        IC3             Node[pin17];
        IC2             Node[pin16];
        IC1             Node[pin15];
        IC0             Node[pin14];
Outputs;
        IC3             Node[pin17];
        IC2             Node[pin16];
        IC1             Node[pin15];
        IC0             Node[pin14];
        /WBFULL         Node[pin19];
        /WBEMPTY        Node[pin12];
Table;
        IC0 NOT :=      ( IC0 AND !/ICE ) OR (!IC0
                        AND /ICE) OR !/R3KRST;

        IC1 NOT:=       (!IC0 AND !IC1 AND !IC1AND
                        !/ICE) OR (IC0 AND IC1 AND
                        !/ICE) OR (!IC1 AND /ICE) OR
                        !/R3KRST;

        IC2 NOT:=       (!IC0 AND !IC1 ABD !IC2
                        ABD !/ICE) OR (IC0 AND IC1
                        AND IC2 AND !/ICE) OR
                        (!IC0 AND IC1 AND !IC2 AND
                        !/ICE) OR (IC0 AND !IC1
                        AND !IC2 AND !/ICE) OR
                        (!IC2 AND /ICE) OR
                        !/R3KRST;

        IC3 NOT :=      (!IC2 AND !IC3 AND !/ICE)
                        OR (!IC1 AND IC2 AND !IC3
                        AND !/ICE) OR (!IC0 AND
                        IC1 AND IC2 AND !IC3 AND
                        !/ICE) OR (IC0 AND IC1 AND
                        IC2 AND IC3 AND !/ICE) OR
                        (!IC3 AND /ICE) OR
                        !/R3KRST;
        /WBFULL NOT =   !IC AND !X;
        /WEMPTY NOT=    !IC AND X;
End;
End I_Counter;
```

The PAL equations for the SEL-counter are:

```
MODULE SEL_COUNTER;
TITLE SEL_COUNTER;
TYPEMMI 16R4;
Inputs;
        /SELCE          Node[pin2];
        IC0             Node[pin3];
        IC1             Node[pin4];
        IC2             Node[pin5];
        /R3KRST         Node[pin6];
        SELC3           Node[pin17];
        SELC2           Node[pin16];
        SELC1           Node[pin15];
        SELC0           Node[pin14];

        S0              Node[pin18];
        S1              Node[pin13];
        S2              Node[pin19];
Outputs;
        S0              Node[pin18];
        S1              Node[pin13];
        SELC3           Node[pin17];
        SELC2           Node[pin16];
        SELC1           Node[pin15];
        C0              Node[pin14];
        S2              Node[pin19];
        C               Node[pin12];
Table;
        SELC0 NOT:=     (SELC0 AND !/SELCE) OR
                        (!SELC0 AND /SELCE) OR
                        !/R3KRST;

        SELC1 NOT:=     (!SELC0 AND !SELC1 AND
                        !/SELCE) OR (SELC0 AND
                        SELC1 AND !/SELCE) OR
                        !/R3KRST;

        SELC2 NOT:=     (!SELC0 AND !SELC1 AND
                        !SELC2 AND !/SELCE) OR
                        (SELC0 AND SELC1 AND
                        SELC2 AND !/SELCE) OR
                        (!SELC0 AND SELC1 AND
                        !SELC2 AND !/SELCE) OR
                        (SELC0 AND !SELC1 AND
                        !SELC2 AND !/SELCE) OR
                        (!SELC2 AND /SELCE) OR
                        !/R3KRST;

        SELC3 NOT:=     (!SELC2 AND !SELC3 AND
                        !/SELCE) OR (!SELC1 AND
                        SELC2 AND !SELC3 AND
                        !/SELCE) OR (!SELC0 AND
                        SELC1 AND SELC2 AND
                        !SELC3 AND !/SELCE) OR
                        (SELC0 AND SELC1 AND
                        SELC2 AND SELC3 AND
                        !/SELCE) OR (!SELC3 AND
                        /SELCE) OR !/R3KRST;

        S0 NOT =        (IC0 XOR SELCO);
        S1 NOT =        (IC1 XOR SELC1);
        S2 NOT =        (IC2 XOR SELC2);

C NOT = S0 AND S1 AND S2;
End;
End SEL_Counter;
```

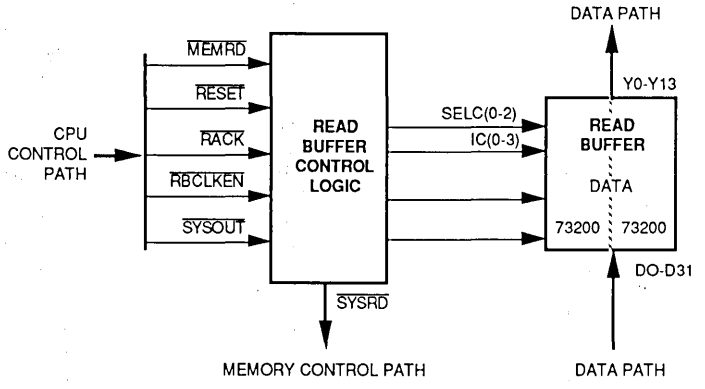

Figure 9. Read Buffer Interface

READ BUFFER INTERFACE

When reading from the main memory to the cache, the R3000/1 sends a memory read signal to the control state machine, represented in Figure 9 as the Read Buffer Control Logic. Once the signal has been acknowledged, the R3000/1 places the address, tag, and data size in the write buffers. Internally, the 73200 registers capture this information at R3000/1 clock rate with load and output configurations determined by the read buffer controller. Once the address is available in the address bus, the controller will then drive memory signals to initiate the memory transfer at memory clock rate into the read buffer.

READ BUFFER CONTROLLER

The read buffer controller monitors the flow of data within the Read Buffer by programming the 73200 internal registers to the appropriate load mode and memory clock frequency. Finally, the controller selects the output registers at such speed to match the R3000/1 frequency.

The PAL equations for the read buffer controller are:

```
MODULE W/RB_CONT;
TITLE W/RB_CONT;
TYPE MMI 16R8;
Inputs;
        WRACQ           Node[pin5];
        MEMRD           Node[pin6];
        MEMWR           Node[pin8];
        RESET           Node[pin9];
        LRD             Node[pin15];
        LWR             Node[pin14];
        WB_CLK_DIS      Node[pin19];
        CMEMRD          Node[pin13];
        CCMEMRD         Node[pin18];
        WRBUSY          Node[pin16];
Outputs;
        LRD             Node[pin15];
        LWR             Node[pin14];
        WB_CLK_DIS      Node[pin19];
        WB_DATA_OE      Node[pin12];
        CMEMRD          Node[pin13];
        CCMEMRD         Node[pin18];
        WRBUSY          Node[pin16];
Table;
        LWR NOT :=      LRD AND !MEMWR AND
                        RESET OR !LWR AND
                        WRACQ;
        LRD NOT :=      LWR AND !MEMRD;

        WRBUSY NOT :=   !MEMWR OR
                        !WRBUSY AND WRACQ
                        OR !MEMRD;

        WBCEN NOT :=    !MEMWR OR !WB_CLK_DIS
                        AND WRACQ OR !MEMRD
                        AND CCMEMRD;

        WB_DATA_OE NOT:= LRD AND !MEMWR OR
                        (need to be inverted)
                        !LWR AND WRACQ;

        CMEMRD NOT :=   !MEMRD;

        CCMEMRD NOT:=   CMEMRD;
End;
End W/RB_CONT;
```

CONCLUSION

As the speed of the processor increases, write and read buffers must also become faster and deeper. The high-speed multi-level pipeline register IDT 73200 meets that challenge by providing a fast and flexible data path to suit various high-speed RISC and CISC processors.

Integrated Device Technology, Inc.

USING IDT73210 AS READ AND WRITE BUFFERS WITH R3000

APPLICATION NOTE AN-65B

By V. S. Ramaprasad

INTRODUCTION

In this application note, the design of one deep read and one deep write buffer to be used in an R3000 system is described with boolean equations and timing diagrams. The boolean equations are for the control signals of the read and write buffers and the main memory interface. This control logic can be implemented with any PLD. The syntax chosen to describe these equations is simple and it is not associated with any PLD programming software. The timing diagrams explain the various states during the operation of one deep read and write buffers. Also described in this application note are the other possible configurations of implementing read and write buffers with IDT73210s. These components can be used as two deep read and one deep write , and one deep read and two deep write buffers. Before the application is presented, the features of 73210 are described and a summary of the memory interface signals of R3000 is given.

R3000 based systems require read/write buffers between the CPU and the main memory due to memory bandwidth mismatch. The main memory system supplies the instructions/ data through a read buffer. The CPU makes the data updates to the main memory through a write buffer. The speed differences between the CPU, the caches and the main memory that typically exist in many systems demand the use of at least one level deep read and write buffers. The use of these buffers isolates the caches from the rest of the memory system. They also limit the physical length of the address and data lines and serve as drivers to the rest of the system.

The gain in performance by increasing the depth of the read and the write buffers is completely dependent on the application program being executed. By modeling memory subsystems with different depths of read/write buffers (using the System Programmer's Package tools for the R3000) and running the application program on the model, the designer can make the trade-off between the cost and the depth of the buffers. For high performance systems with sophisticated main memory schemes like interleaving, and for systems with fast DRAM architectures like Page Mode, or Static Column Mode, a one deep read buffer might satisfy the transfer rate of the processor. For low performance systems, where the penalty of fetching one word at a time is not significant, and for applications with infrequent successive writes, a one deep write buffer might also deliver optimal performance.

In systems where one-level deep read and write buffers proved to be sufficient, a bidirectional register can be utilized to serve as both read and write buffers. The 8-bit bidirectional register, IDT73210, with parity checking and parity generation is an ideal candidate for this purpose. This bidirectional register also allows the designer to build a two-level deep read buffer and one level deep write buffer, or one- level read buffer and two-level write buffer configurations. Using IDT73210 reduces the parts that are needed for parity generation. Also, by clocking in the lower address bits and the higher address bits with separate clocks, the designer can eliminate latching the address low bits.

IDT73210 FEATURES

Figure 1 shows the features of IDT73210 with all the control signals and data paths. It is a bidirectional buffer with separate output enables and clock enables. Data is registered with the same clock in both directions. There is a single data path from port A to port B. The 8-bit data and the parity bit are clocked through register X. The POLARITY signal is used to select even or odd parity generation. Even parity checking is done on the data, and a parity error is indicated by PERRA. The 8-bit data and the parity bit are enabled through a tri-stateable buffer to port B.

There are two data paths from port B to port A. A multiplexer controlled by SEL selects a path. Even parity checking is done in both the paths and parity error is indicated by PERRB. The first path is through latch W and register Z. In this path bit W8 is complemented by POLARITY to yield either even or odd parity.The second path is through registers Y & Z and even parity is generated on the data. The two registers in the second data path provide the user with two- level deep buffering. The 9-bit output is enabled through a tri-stateable buffer to port A.

7

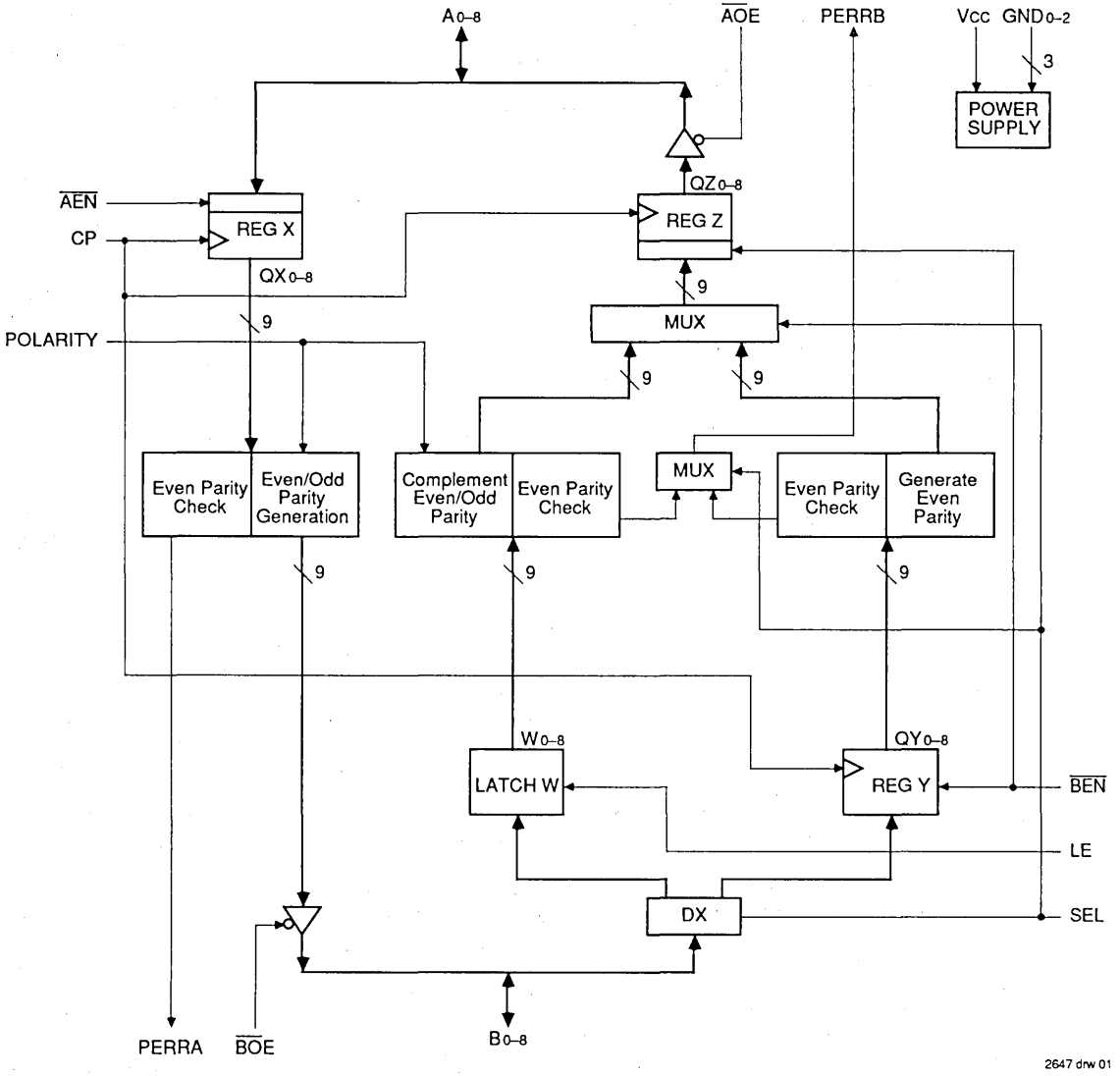

Figure 1. IDT73210

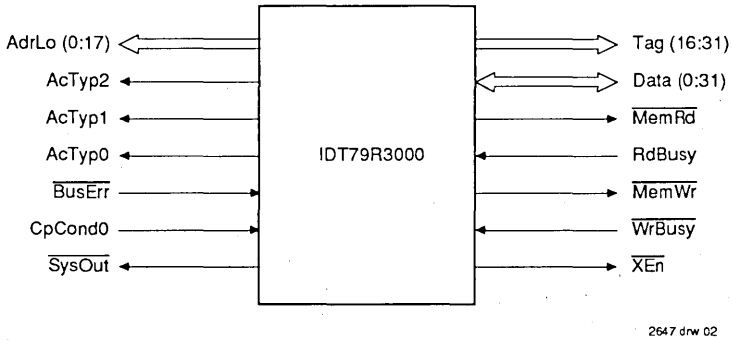

Figure 2. Memory Interface Signals

IDT79R3000 MEMORY INTERFACE

The R3000 has interfaces to the main memory through the asynchronous memory bus. The output signals indicate the nature of operation that the R3000 is performing. The input signals are used to indicate the termination of a stall, block refills, and to cause exception processing.

The figure above shows the signals used to interface to main memory. The address bus is split into AdrHi and AdrLo. The AdrHi bus is also used as the Tag bus for cache reads and therefore is shown as bidirectional.

MemRd: This signal indicates the entry into the stall on a read operation. It is an active-low output signal. This output signal of the R3000 is used by the state machines to enter a read state and signal the memory system that the R3000 accepts data from the supplied 32-bit address. For one word refill, MemRd is deasserted by the R3000 one cycle after the RdBusy signal is deasserted indicating that the required data is ready. The deassertion of MemRd signals the end of a read stall. MemRd stays asserted during the entire stall cycles.

RdBusy: This input signal to the R3000 is used to enter and terminate read stall cycles. The deassertion of RdBusy terminates stall cycles and the R3000 enters a fixup one cycle later during single word loads or it enters refill cycles in case of multiple word loads. RdBusy assertion and deassertion is sampled by the R3000 in phase 1 of the clock cycle.

XEn: This active-low, output signal is used to enable the output of the read buffer in refill and fixup cycles.

MemWr: This output signal is asserted low for store operations. Unlike MemRd, this signal is active for only one cycle as are the associated data and addresses. MemWr is used to enter a write state.

WrBusy: In order to create a write stall, this input signal to the R3000 has to be asserted low during the cycle in which MemWr is asserted. The deassertion of WrBusy terminates a write stall and the R3000 enters the fixup cycle. In the fixup cycle, the last write operation during which WrBusy was asserted is repeated. WrBusy is usually tied to the signal that indicates the write buffer is full. WrBusy assertion is sampled by the processor in phase 2 and the deassertion is sampled in phase 1 of the clock cycle.

SysOut: This is the clock output of the 79R3000 and is the clock frequency at which the R3000 is rated.

CpCond0: The condition of this input signal to the R3000 in stall cycles determines if the processor will do a single word read or a multiple word read.

BusErr: This input signal is provided as a mechanism to create an exception in the R3000 and as an aid to escape from interminable stall cycles.

AccTyp0: This output signal has three functions. During cached reads it indicates whether there was a data cache miss or an instruction cache miss. This information is useful if the block refill size is different for data and instructions. During uncached reads it is used with AccTyp1 to indicate the size of the data being read. During writes it is used along with the AccTyp1 to indicate the size of the data being written.

AccTyp1: This output signal is undefined for cached reads. For uncached read operations and for store operations, AccTyp1 along with AccTyp0, indicates the size of data transfer.

AccTyp2: AccTyp2 is undefined for store operations with stall cycles. For load operations, it is high for cached operations and low for uncached operations. During run cycles, this line indicates whether there is any data transfer during the second phase.

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USING IDT73210s

Figure 3 shows the application of the 73210s as one-deep read and one-deep write buffer. Four 73210s are used to transfer the 32-bit data and the associated four parity bits. On the address bus, four 73210s are used to pass the 32-bit physical address and the access type bits(0:1) to the main memory. Port B of the 73210s are connected to the processor side, and Port A of the 73210s are connected to the memory side.

The read and the write data paths are explained in Figures 4 and 5. In this design, one single set of four IDT73210s serve the function of read and write buffers. Also, a set of four IDT73210s are used to capture the addresses during read and write operations. The timing diagrams point out the control signals that resolve any conflicts in the use of these buffers.

The control logic, described in the following sections, can be implemented with any PLD that matches the processor speed. To interface with the main memory, signals are defined to make a request to the main memory ($\overline{MREQ}$), to specify a read or a write operation to the main memory ($\overline{MRD}$, $\overline{MWR}$), and a signal from the main memory to indicate the completion of read or write operation ($\overline{CYCEND}$).

The memory interface signals from the R3000 are used by the PAL state machine inorder to generate controls to the buffers and the main memory. The RdBusy, $\overline{WrBusy}$, $\overline{MREQ}$, $\overline{MRD}$, $\overline{MWR}$, and the clock and data output enables for the 73210s are generated by the state machine.

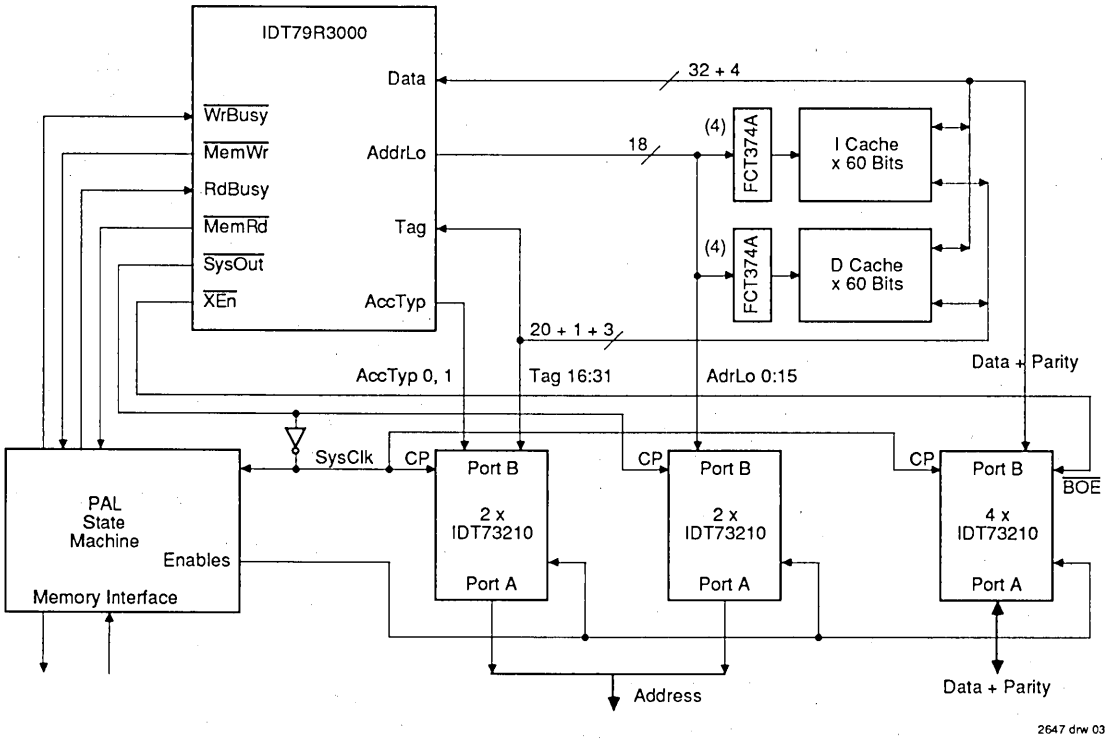

Figure 3. Using IDT73210 as Read and Write Buffer

Read Operations

The data path for the read operations is through register X. The address and the access type bits go through the latch W and the register Z. The lower address bits are clocked in with $\overline{SysOut}$. The tag bits, along with the access type bits, are registered with inverted $\overline{SysOut}$ (SysClk). The latch W is always transparent to bypass the address bits and access type bits. The POLARITY signal is held low to pass the access type bits as parity bits through the two 73210 on the tag bus. The low POLARITY signal to the four 73210s on the data bus generates even parity on the data passing through register X.

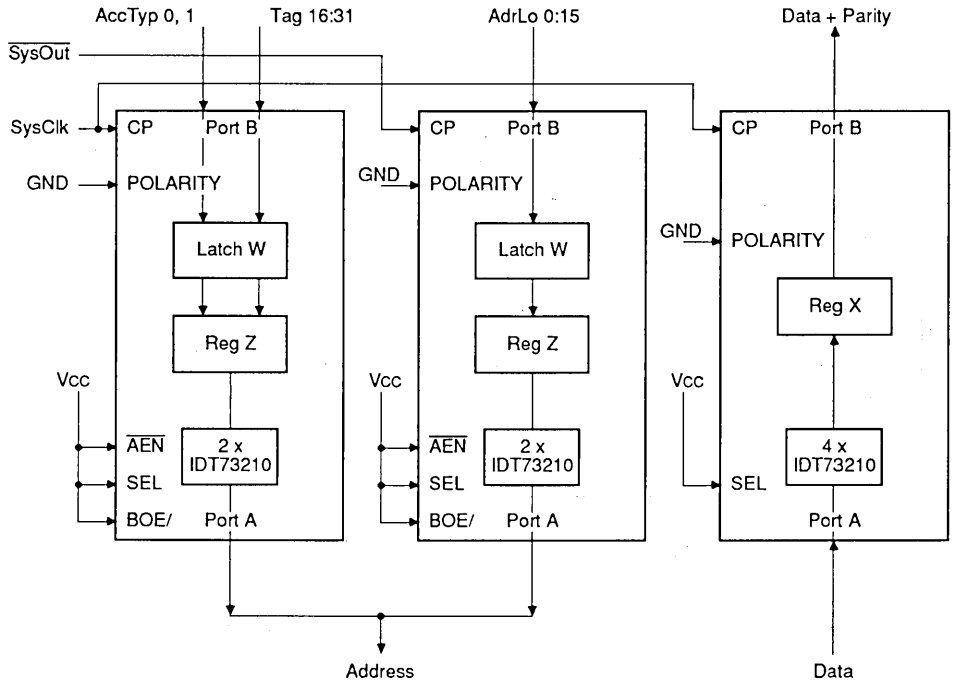

Figure 4. Read Data Path. One Deep Read, One Deep Write Buffers Using IDT73210

Write Operations

The data path for write operations is through latch W and register Z. Data is clocked in the 73210s on the data bus with SysClk along with the tag bits. The lower address bits are clocked in with $\overline{SysOut}$. Once the address and data are available in the Z registers, the PAL state machine generates the output enable signals and presents the address and the data to the memory. The even parity that is generated by the CPU passes through the parity unit without getting modified.

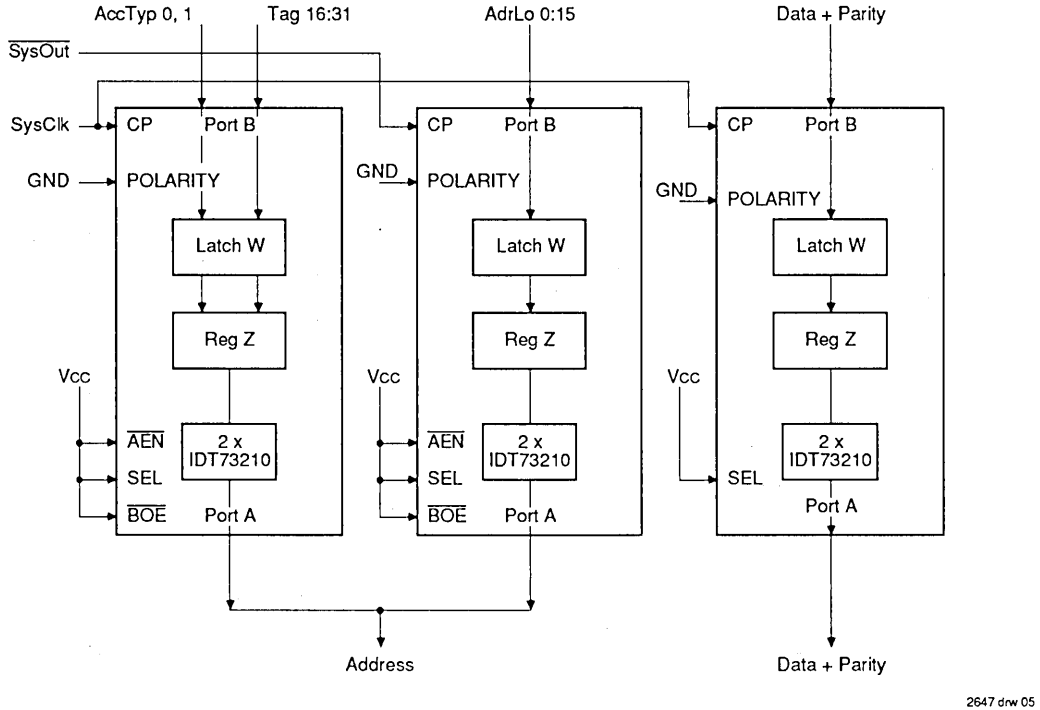

Figure 5. Write Data Path. One Deep Read, One Deep Write Buffers Using IDT73210

CONTROL LOGIC

The control logic for the signals that control the address 73210s, the data 73210s, and handshake signals to the main memory system is described with simple boolean equations. The 73210s are used to capture the data and addresses during read and write operations and to provide the system with one-level deep read and write data paths. Byte enable signals for partial word writes can be generated by extending these equations. In this design, block refills are supported and instruction streaming is assumed to be enabled.

The control signals that are utilized by the PAL state machine to control the read/write buffers, and communicate with the main memory controller are $\overline{WIP}$, $\overline{WrBusy}$, RdBusy, $\overline{MRD}$, $\overline{MWR}$, $\overline{MREQ}$ and $\overline{CYCEND}$. The clock input to the PAL is inverted $\overline{SysOut}$. In the following boolean equations the following notation is adopted:

!	Logical NOT operation.
*	Indicates the corresponding signal is active low.
OR	Logical OR operation.
AND	Logical AND operation.
;	To end a boolean equation.
:=	Registered output.
=	Combinatorial output.

Main Memory Controls

```
{ RdBusy usually stays asserted even when there is no read          }
{ operation going on. It is deasserted when the memory system       }
{ acknowledges ( asserting CycEnd) that the read is finished. It    }
{ remains deasserted till MemRd gets deasserted.                    }
{ It is assumed here that the memory system asserts CYCEND in       }
{ phase 1. RdBusy gets deasserted in phase 2, and the CPU puts      }
{ out XEn(s) from the next clock cycle.                             }
{ RdBusy is not deasserted with CYCEND associated with a prior      }
{ write operation.                                                  }
{ RdBusy is a registered output.                                    }

RdBusy :=  !( !WIP AND MemRd AND CYCEND) OR
           !( !RdBusy AND MemRd);

{A single pulse request is sent out to the main memory system to    }
{ indicate that a read or write operation is coming along. It is    }
{ asserted only when a read or write operation is feasible through  }
{the one deep read and write buffers.                               }
{ This is a registered output.                                      }

MREQ :=  ( !WIP AND !MemRd AND MemWr AND !MREQ) OR
         ( !WIP AND MemRd AND !MREQ );

{ A read strobe is given out to the main memory system to           }
{ indicate a read operation. This signal is asserted while there is }
{ no write in progress and MemRd is asserted.                       }
{ To support block refills MRD stays asserted with MemRd.           }
{ This is a registered output.                                      }

MRD :=  ( !MRD AND !WIP AND MemRd) OR
        ( MRD AND MemRd);
```

The control signal CYCEND is asserted by the main memory controller to indicate the finish of a write operation or the availability of the first word of the block refill in the read buffer.

It is assumed that CYCEND is asserted in phase 1, so that RdBusy can also be deasserted in phase 1.

```
{ WIP signal is used to indicate whether the write buffer is in     }
{ the process of retiring its contents to the main memory.          }
{ WIPis asserted when MemWr is asserted and deasserted when         }
{ an acknowledge (CYCEND) from the main memory system comes         }
{ back indicating that the write is carried out.                    }
{ WIP is a registered output                                        }

WIP :=  ( !WIP AND !MemRd AND MemWr) OR
        ( WIP AND !CYCEND);

{ Write busy (WrBusy) is asserted when there is a write in          }
{ progress or when read operation is going on. During read          }
{ operations with streaming enabled, WrBusy should be               }
```

```
{ asserted to stop any writes because there is a common data      }
{ buffer for both read and writes.                                }

WrBusy = WIP OR MemRd;

{ A write strobe is given out to the main memory system to        }
{ indicate a write operation is in progress.                      }

MWR = WIP;
```

Higher Address Buffer Controls

```
{ Controls for 73210s that pass higher address bits (Tag 16:31)   }
{ and access type bits (AccTyp 0,1).                              }
{ The path through latch W & register Z is selected by the internal }
{ Mux.                                                            }

SEL = 1;

{ Register Z is enabled for read and write operations when there  }
{ is no contention between read and writes.Latch W is transparent. }
{ A read operation in progress is indicated by MemRd signal.      }
{ For write operations ABEN is enabled for one clock cycle.       }

DMemWr := MemWr;
ABEN = ( MemRd AND !WIP AND !MemWr) OR
       ( MemWr AND !WIP AND !MemRd) OR
       ( ABEN AND MemWr AND !DMemWr);

{ Allows the Access Type bits to pass through "Compliment         }
{ Even/Odd Parity" unit as parity bits without getting modified.  }

POLARITY = 0;

{ The higher address bits along with the access type bits are     }
{ clocked into the register Z with inverted SysOut.               }

CP = ! SysOut;

{ The higher address bits along with the access type bits are put }
{ out to port A when there is a write in progress or while MemRd  }
{ is asserted.                                                    }

AAOE = WIP OR MemRd;

{ AEN always disabled for the address 73210.                      }

AEN = 1;

{ BOE always disabled for the address 73210.                      }

BOE = 1;
```

Lower Address Buffer Controls

```
{ Controls for 73210s that pass lower address bits (AddrLo 0:15)  }
```

```
{ The path through latch W & register Z is selected by the internal    }
{ Mux.                                                                 }

SEL = 1;

{ Register Z is enabled for read and write operations when there       }
{ is no contention between read and writes.Latch W is transparent.     }
{ A read operation in progress is indicated by MemRd signal.           }
{ For write operations ABEN,is enabled for one clock cycle.            }

DMemWr := MemWr;
ABEN = ( MemRd AND !WIP AND !MemWr) OR
       ( MemWr AND !WIP AND !MemRd) OR
       ( ABEN AND MemWr AND !DMemWr);

{ POLARITY is Don't Care.                                              }

POLARITY = 0;

{ The lower address bits are clocked into the register Z with          }
{ SysOut signal, because they are available in the first phase.        }

CP = SysOut;

{ The lower address bits are put out to port A when there is a         }
{ write in progress or while MemRd is asserted.                        }

AAOE = WIP OR MemRd;

{ AEN always disabled for the address 73210.                           }

AEN = 1;

{ BOE always disabled for the address 73210.                           }

BOE = 1;
```

Data Buffer Controls

```
{ Controls for 73210s that transfer data bits for reads & writes.      }
{ The path through latch W & register Z is selected by the internal    }
{ Mux to provide one-deep write buffer.                                }

SEL = 1;

{ Register Z is enabled for write operations when there is no          }
{ read operation in progress. A read operation in progress is          }
{ indicated by MemRd signal. Latch W is transparent.                   }

DMemWr := MemWr;
DBEN = ( MemWr AND !WIP AND !MemRd) OR
       ( DBEN AND MemWr AND !DMemWr);

{ Even polarity generated by the CPU is passed through by setting      }
{ POLARITY to ZERO.                                                    }
```

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```
POLARITY = 0;

{ The data bits along with the parity bits are clocked into the      }
{ register Z with inverted SysOut.                                   }

CP = ! SysOut;

{ The data bits are put out to port A when there is a write in       }
{ progress.                                                          }

DAOE = WIP;

{ DAEN is enabled during read operations.                            }

DAEN = MemRd AND !WIP;

DBOE is enabled by XEn to read the data from the read buffer.
```

TIMING DIAGRAMS

Figures 6 through 11 give the timing waveforms for the one-deep read and one-deep write buffer described in Figure 3. The signals shown in these figures are described by the boolean equations presented earlier. In these timing diagrams, the signals that are generated by the PAL state machine are shown with a displacement in relation to their input signals. Also, some of the signals generated by the PAL state machine are registered with SysClk. The main memory interface signals generated by the PAL are MREQ, MRD, CYCEND, and MWR. The enable signals to the address 73210s are ABEN, and AAOE. The enable signals to the data 73210s are DBEN, DAOE, DAEN, and DBOE. The memory acknowledge signal, CYCEND is asserted two cycles after MREQ is asserted, for both read and write operations.

Figure 6 shows read and write operations. The memory read operation starts with the MemRd signal being asserted. A MREQ pulse is sent out to the memory, and MRD signal is asserted for the duration that the MemRd signal stays asserted. The memory system responds to the request by placing the data in the read buffer and asserting CYCEND. This deasserts the RdBusy signal. RdBusy is sampled in phase 1 by the processor, and it generates XEn in the next clock cycle. Since the one-deep read and write buffers are implemented using the same buffers, during a memory read operation the WrBusy signal is asserted to halt any write operations. The address enables are asserted through out the read operation to capture the addresses. For read operations, DAEN is asserted with MemRd signal to capture the data coming from the memory. The port B output enable for the data buffers is controlled by XEn for reading in the data. The read latency is five clock cycles including the fixup cycle.

For write operations in Figure 6 , the WrBusy signal is asserted as long as the write operation is in progress. This is indicated by WIP. It should be noticed that the RdBusy signal is asserted during write operations to block any read operations. The address enables are asserted during the write run cycle, and the address output enable is asserted throughout the write operation. The data buffer enables are asserted in the same way. It should be noted that WIP is a clocked output. The write operation takes three cycles.

Figure 7 shows a four word data block refill. The RdBusy signal, once deasserted, remains deasserted until MemRd is deasserted.

Figure 8 shows four word instruction block refill with streaming enabled. The instruction cache miss occured on the instruction I1. The refill starts with the basic block boundary instruction I0. The processor enters fixup as the missed instruction is fetched. The processor streams through the rest of the block.

Figure 9 shows a memory read requested by the processor before a previous write is retired to the main memory. The state machine puts out a request for the read operation only after the completion of the write operation, indicated by the first assertion of CYCEND. The enable ABEN is not enabled for the read untill the previous write is completed.

Figure 10 shows two write operations in two consecutive clock cycles. Since the write buffer is one word deep, the second write is not absorbed by the write buffer, and the processor stalls untill the first write is retired to the main memory. In the following fixup cycle, the second write is completed to the write buffer. The memory request MREQ for the second write is only generated in the fixup cycle. The data and the address of the second write are not captured by the buffers while the first write is in progress. In should be noted that deassertion of WrBusy is sampled by the processor in phase 1.

Figure 11 shows a write operation occuring in the middle of streaming. Streaming starts with instruction I1. The next instruction I2 issues a write. Since the write busy signal is already asserted, instruction streaming is aborted. The instruction I2 is executed in the following fixup cycle. WIP is asserted only in the fixup cycle. The data and the address of the write instruction I2 are not captured during streaming.

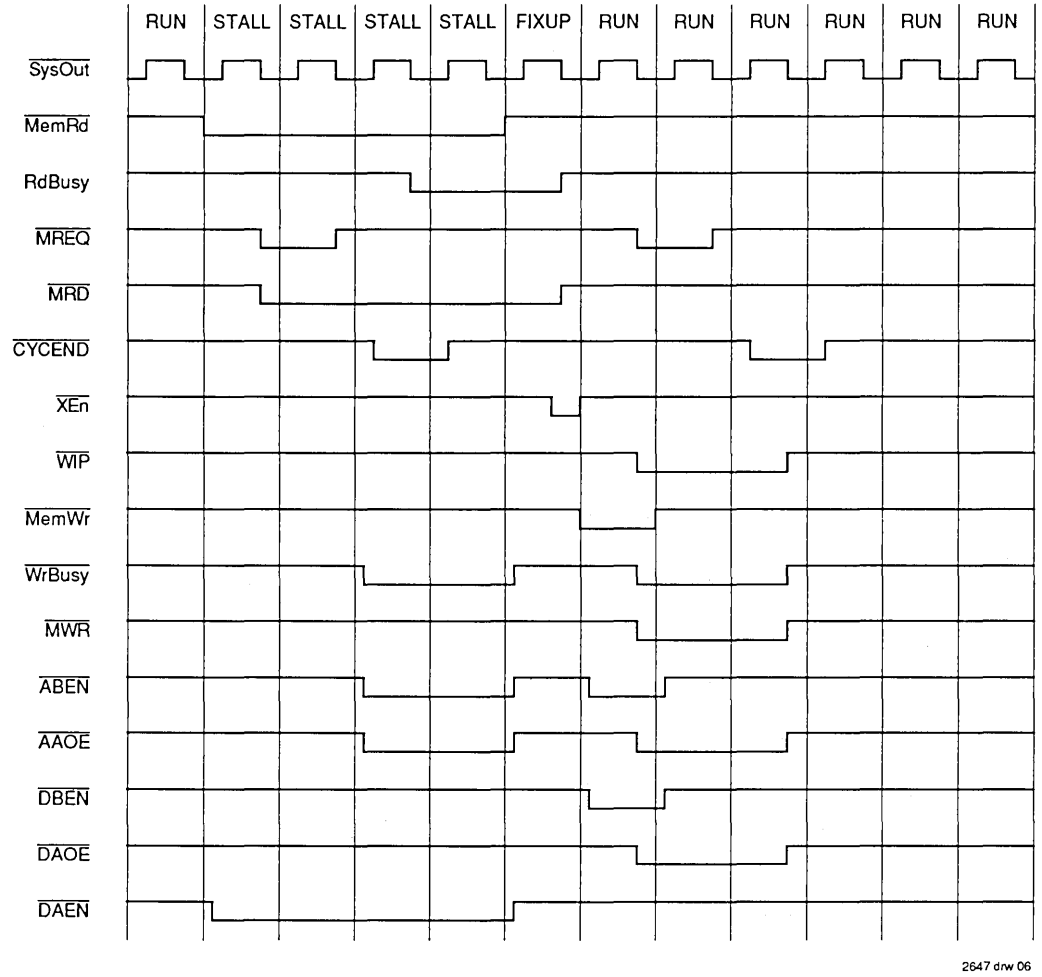
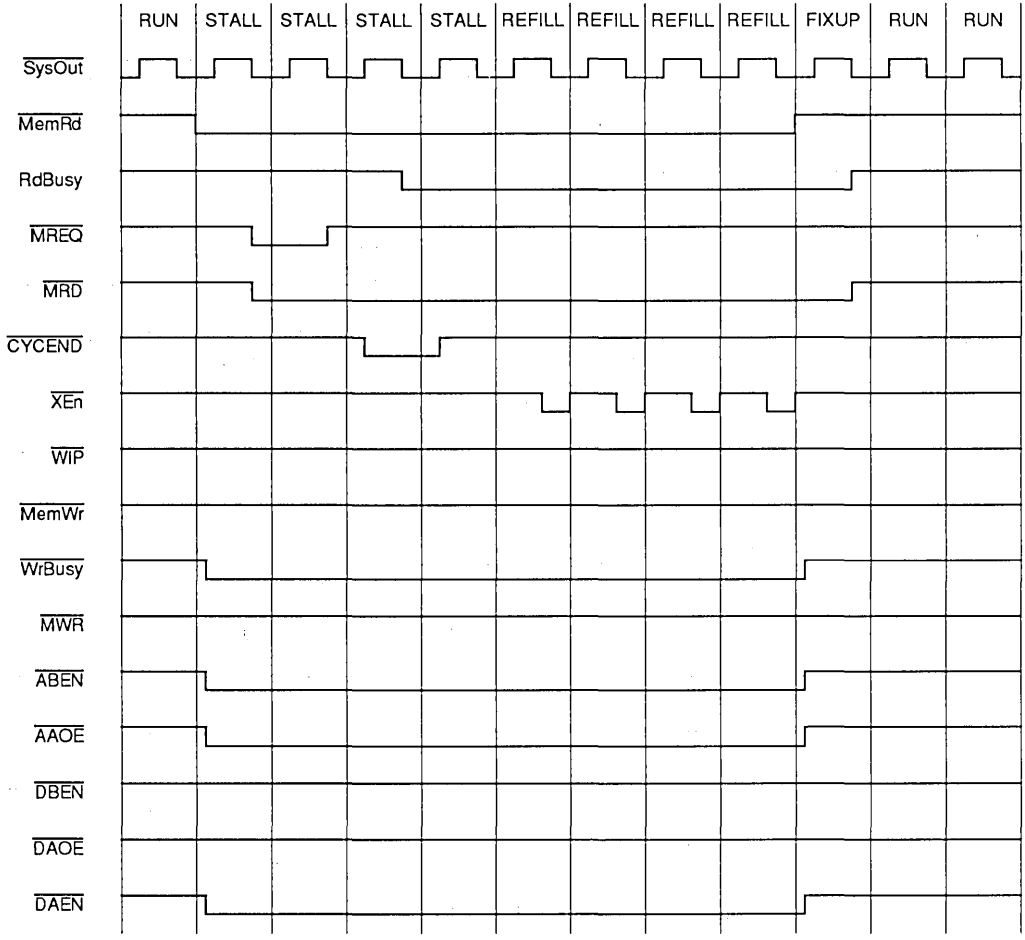


Figure 6. Read, Write Operations



2647 drw 07

Figure 7. Data Block Refill

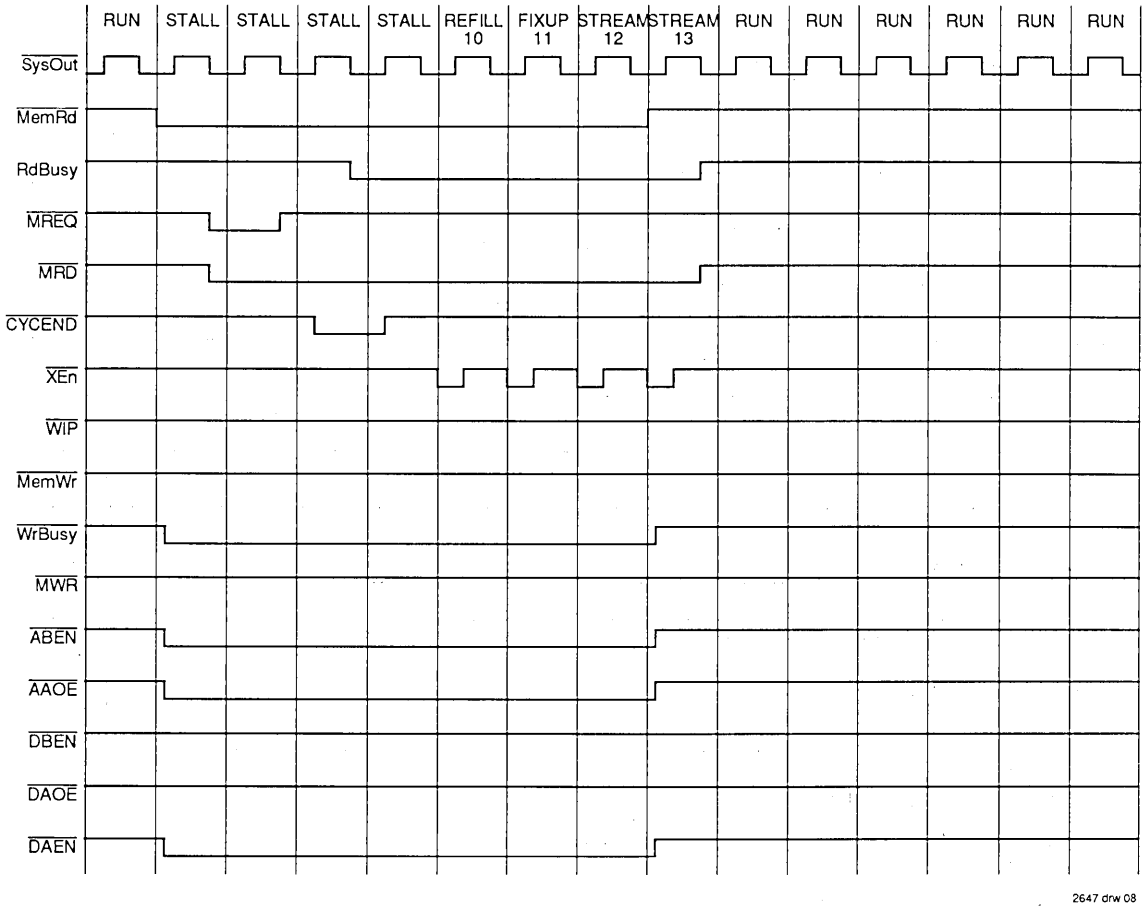


Figure 8. Instruction Streaming

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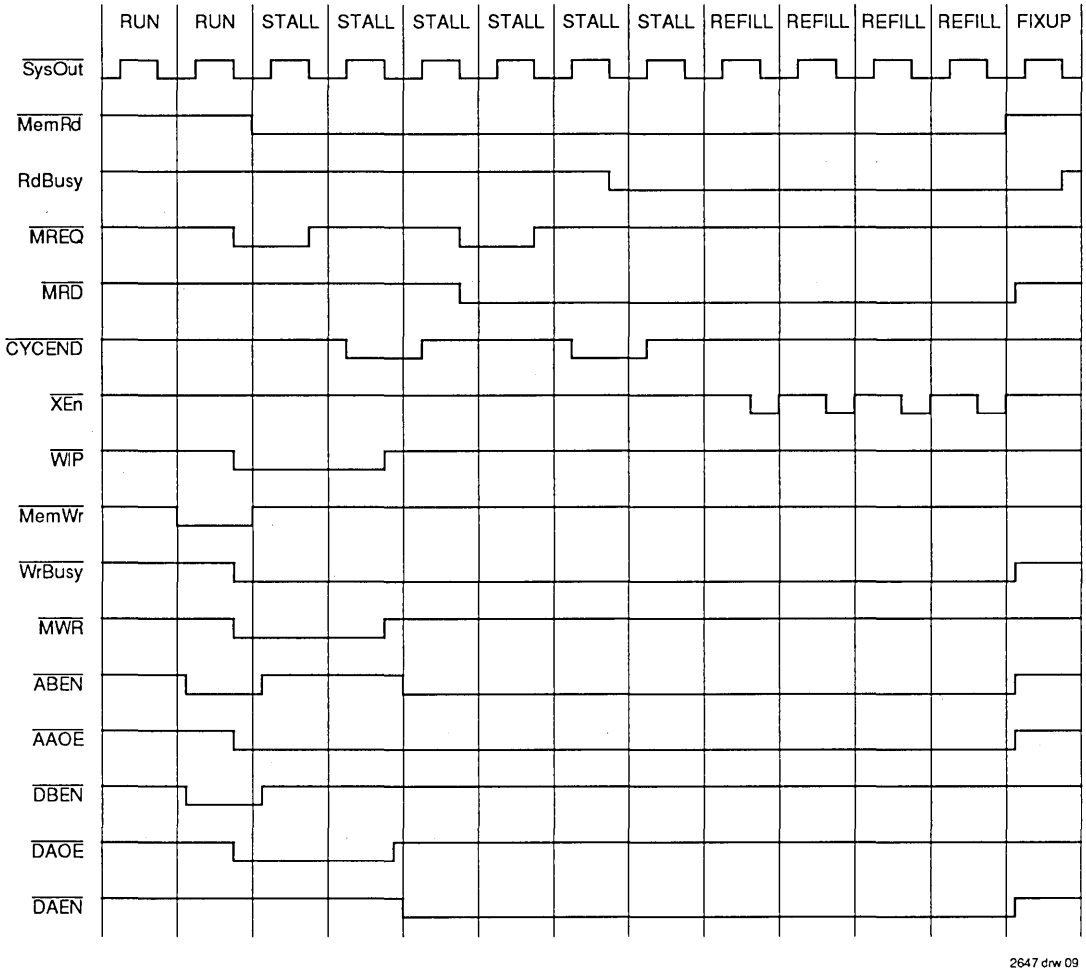

Figure 9. Read During Write in Progress

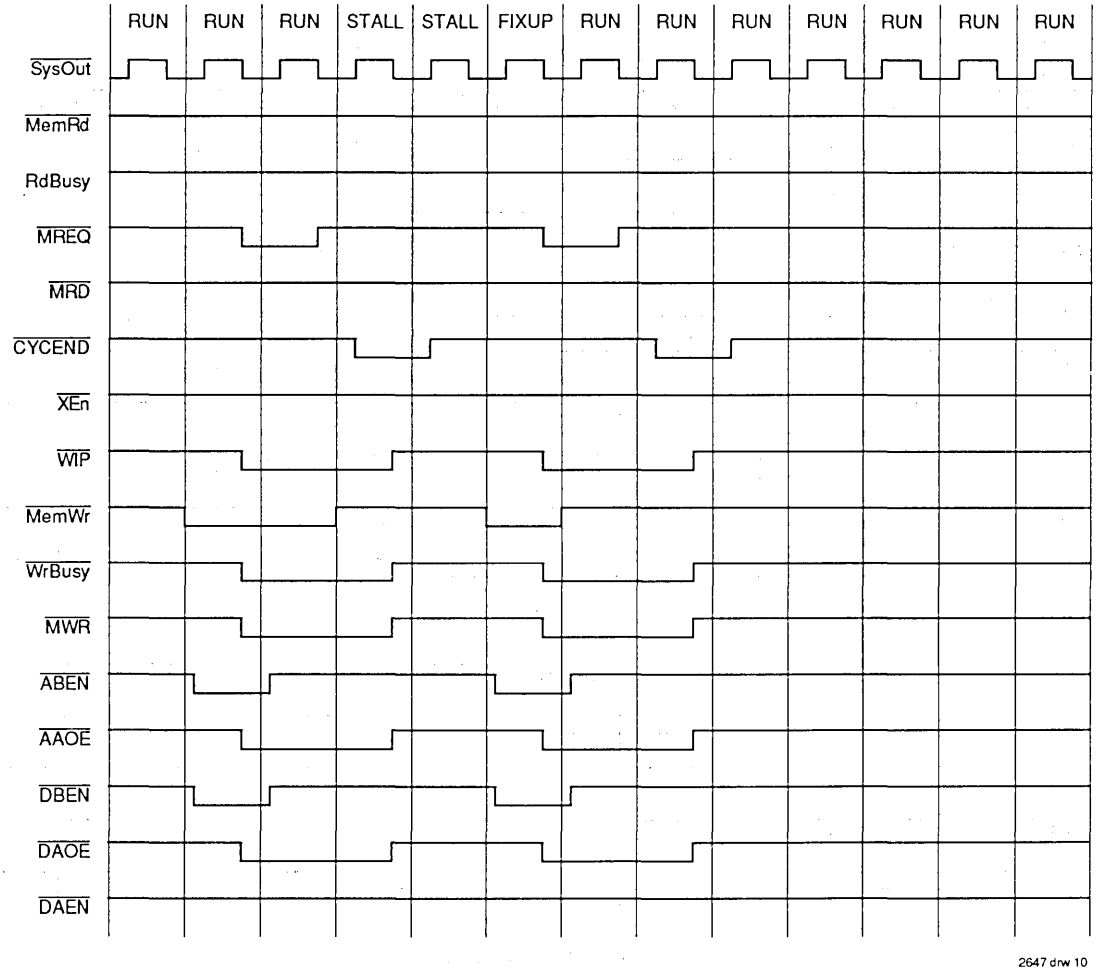

Figure 10. Write During Write in Progress

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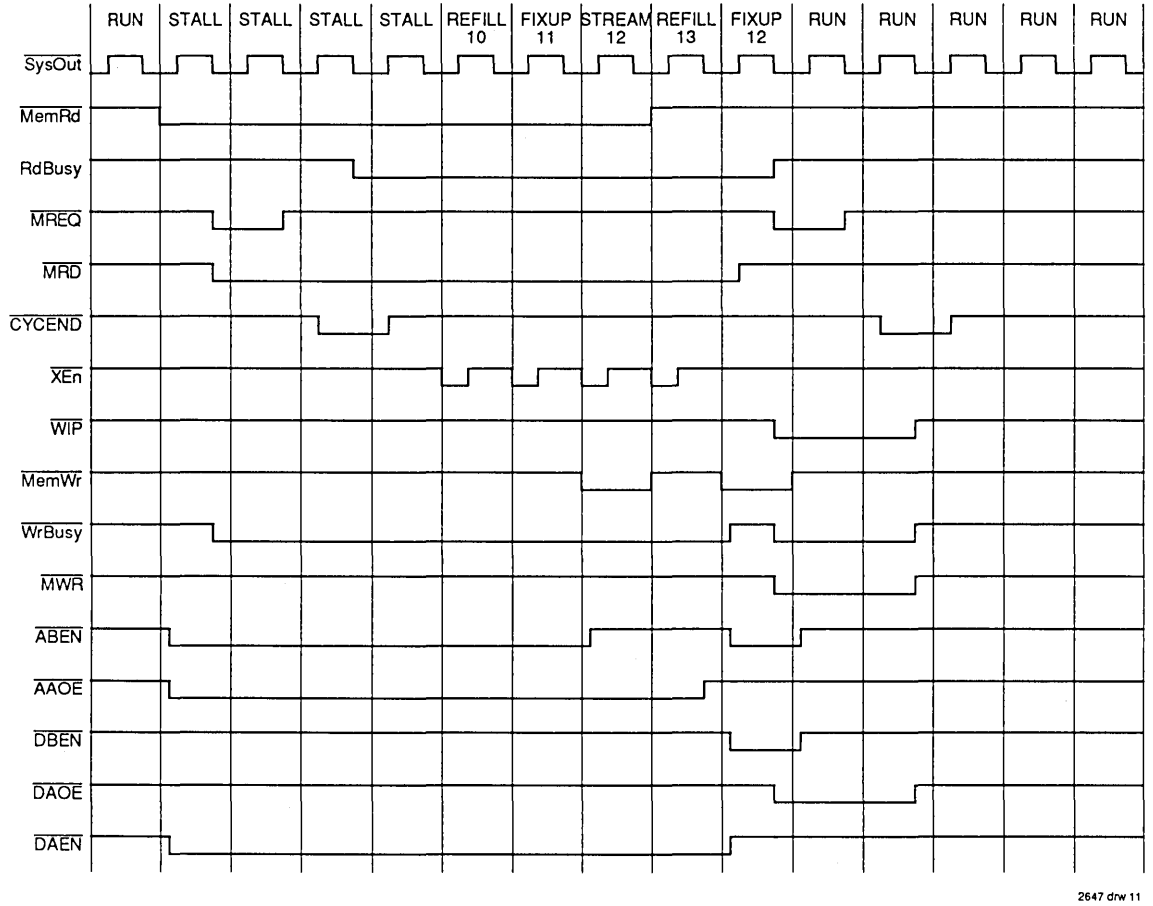

Figure 11. Write in Streaming

TWO DEEP READ AND ONE DEEP WRITE

IDT73210s can also be used in two-deep read and one deep write configuration. For capturing the addresses and the access type bits, four IDT73210s are used with B ports connected to the processor. For transfering data, four IDT73210s are used with A ports connected to the processor.

This configuration of the data path uses the registers Y and Z for read operations as two-level deep buffers. For write operations, the data is wrtten to the register X, thus providing a one-deep write buffer. The read and write data paths are shown in Figures 12 and 13. It should be noticed that even parity is generated on the data in both the directions.

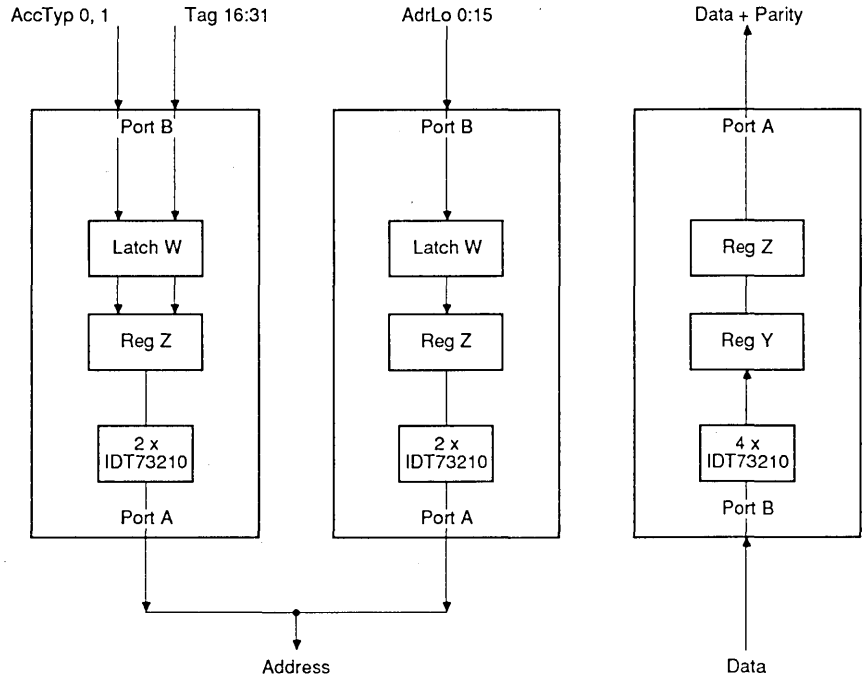

Figure 12. Read Data Path — Two Deep Read, One Deep Write Buffers Using IDT73210

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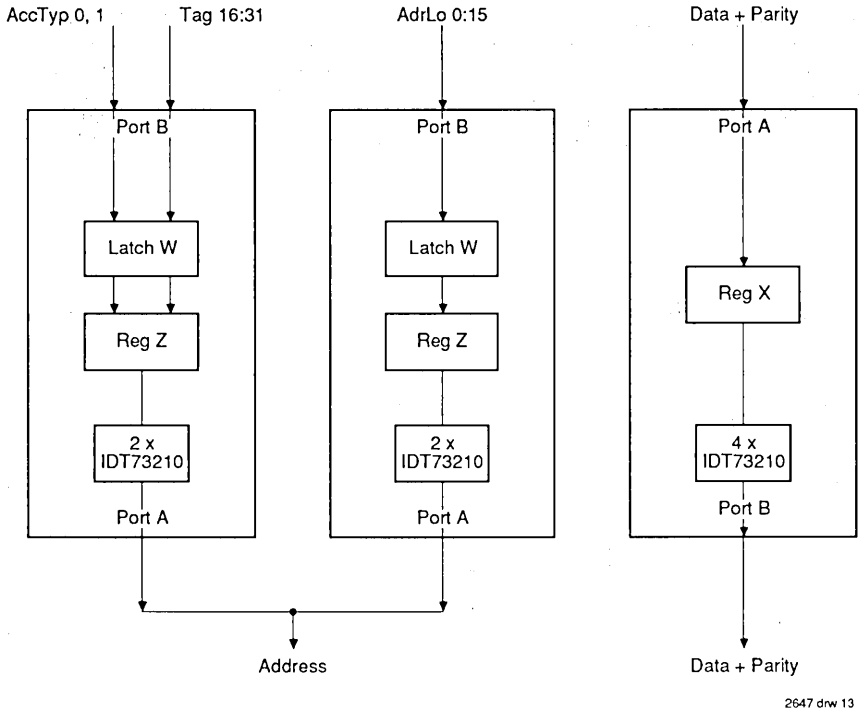

Figure 13. Write Data Path — Two Deep Read, One Deep Write Buffers Using IDT73210

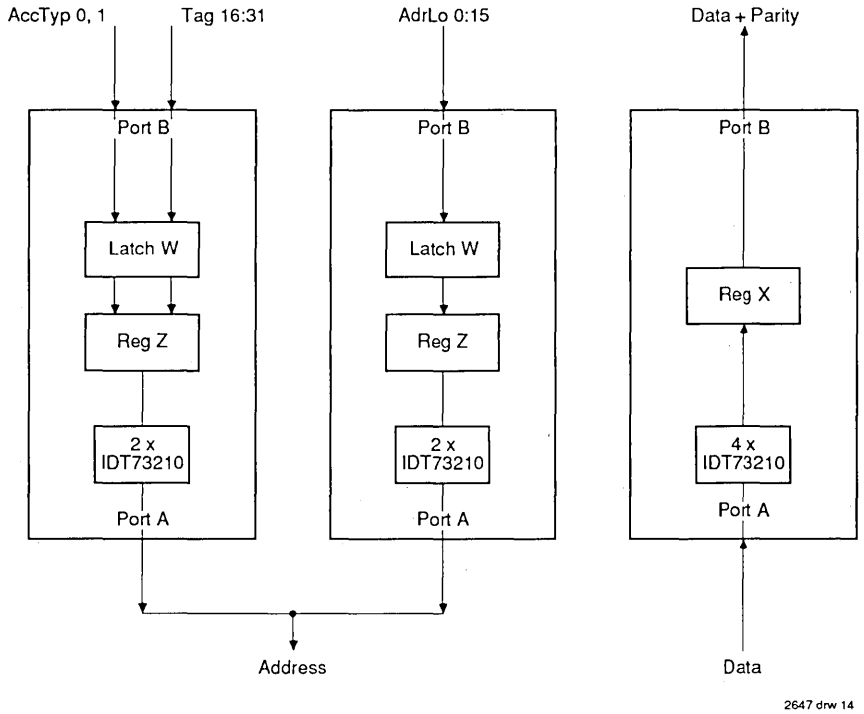

Figure 14. Read Data Path — One Deep Read, Two Deep Write Buffers Using IDT73210

ONE DEEP READ AND TWO DEEP WRITE

To use IDT73210s in a one deep read and two deep write configuration, four IDT73210s are connected to the address bus with B ports on the processor side. Four IDT73210s are connected to the data bus with B ports on the processor side to transmit data. The data path for the read operations is shown in Figure 14. The address and the access type bits can be passed through the latch W and the register Z. Data is read back from the memory through the register X after even parity is generated.

Figure 15 shows the write data path. To utilize the 73210s as two deep write buffer, the addresses and the data are passed through registers Y and Z. These two registers provide the two-level deep buffering for the addresses and the data. If any write operations, such as writing to the registers of I/O devices, require only one-deep write buffer, then the path through the latch W and the register Z is useful for both data and the addresses. It should be noticed that to transfer access type bits in two-deep write configuration, separate two-level deep buffering is required. Increasing the depth of the write buffer to two may improve the performance significantly if the application executes the second store before the first store is absorbed by the main memory.

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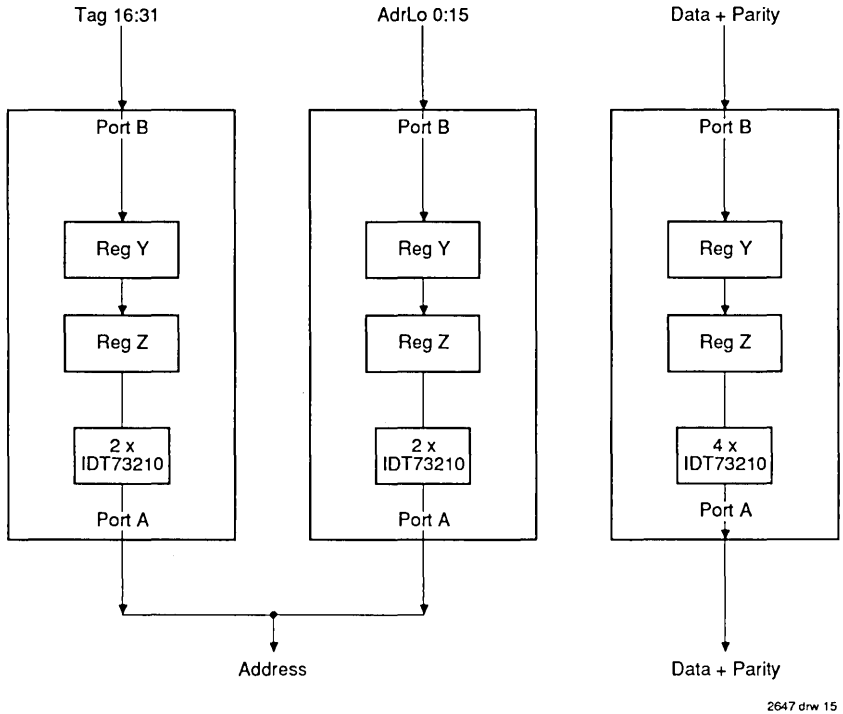

Figure 15. Write Data Path. One Deep Read, Two Deep Write Buffers Using IDT73210

CONCLUSIONS

IDT73210 is an ideal part for one/two-deep read/write buffers for R3000 applications. It is bidirectional, and speed compatible with the existing RISC processors. It generates and checks even parity and hence reduces the parts count in the memory interface for R3000 based systems. Using IDT73210s on the address bus, separate latches for capturing the address low bits can be eliminated. IDT73210 also provides the designer two different data paths from port B to port A to be selected dynamically depending on the operation.

Integrated Device Technology, Inc.

HIGH-SPEED CMOS LOGIC APPLICATION NOTES

ABSTRACT

This collection of application notes is presented to provide information which has been proven useful to the designers who use of plan to use high-speed, TTL-compatible, CMOS logic in high-performance systems. These notes cover a broad range of topics; some explore specific issues applicable to the FCT and FCT-T logic families, while others discuss general topics such as Simultaneous Switching Noise, Printed Circuit Board layouts and series termination.

INTRODUCTION

With the push for high clock rates to increase system performance in a predominantly TTL world, the hardware designer is now required to deal with problems and issues which were largely academic only a few years ago. The introduction of high-speed, high-drive CMOS logic, combined with the increase packing density of multi-layer boards, has resulted in the awareness and the need to deal with problems such as simultaneous switching noise (a.k.a. Ground Bounce), transmission line effects and dynamic power dissipation.

Integrated Device Technology, Inc. pioneered the high-speed, high-drive, TTL-compatible CMOS logic with the introduction of the FCT family. This logic family is now the established leader in the high-performance logic area. By offering a variety of speed grades, functions and packages, the system designer now has an opportunity to optimize overall system performance in terms of speed, power, cost and board space. However, experience has shown that using high-speed logic is an exercise that is more complex than package replacement or paper design. An understanding of switching noise and related issues is important for a successful outcome. Recently, the FCT-T family of TTL-compatible logic with "true TTL" output swing (approximately 3.3 volts typ.) has been added to IDT's logic product line offering functions with a reduced level of switching noise for those users who do not need the rail-to-rail output swing of the FCT family.

This collection of application notes is intended to assist the hardware designer in designing with the FCT and FCT-T logic families. Each application note is independent and deals with a separate topic. Typical device characteristics and performance data are provided where possible. The following is a brief summary of the subjects covered:

- SIMULTANEOUS SWITCHING NOISE — The cause and effects of ground bounce caused by simultaneous switching of high-drive outputs are discussed. Effects of package parasitics are explained. Different solutions for the ground bounce problem are given.
- USING HIGH-SPEED LOGIC — This application note gives general guidelines and recommendations in terms of board layout, power distribution and device selection.
- CHARACTERISTICS OF PCB TRACES — In this application note we discuss the transmissive behavior of printed circuit board traces in the presence of fast signal edges. Effect of loading on trace parameters is described and a simplified measurement method is given.
- SERIES TERMINATION — Pros and cons of series termination are discussed in detail in this note.
- POWER DISSIPATION IN CLOCK DRIVERS — The components of power dissipation in CMOS and CMOS-based BiCMOS circuits are described. The FCT244 Octal Buffer is used as an example to illustrate the effect of loading on the dynamic component of power dissipation.
- FCT OUTPUT STRUCTURES AND CHARACTERISTICS — This application note describes the implementation of the output buffer in various mask-sets used to produce FCT logic product. The output characteristics corresponding to each implementation are shown. This information is useful in calculating estimated speed derating due to capacitive loading and also to determine the impact of termination on the signal characteristics.
- POWER-DOWN OPERATION — Use of FCT family of devices in power-down mode is discussed.
- FCT-T LOGIC FAMILY — This application note describes in detail the features and benefits, electrical characteristics and performance of the FCT-T family of products. Typical V-I characteristics of all important DC parameters are shown. The power-off disable feature of backplane drivers is described.
- SPECIFIC PRODUCT APPLICATION BULLETINS — These application notes describe in detail technical information referring to the pertaining part number.

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Integrated Device Technology, Inc.

SIMULTANEOUS SWITCHING NOISE

APPLICATION NOTE AN–47

By Suren Kodical

INTRODUCTION

The need for increasing levels of throughput and improved performance in today's systems has placed certain demands on the logic and interface devices used in these systems. Two of the key requirements are high speed and high dynamic drive. Often the traditional glue logic and interface parts are in the critical timing paths and play a key role in determining system performance. Better speed (shorter propagation delays) lead to improved timing margins and offer opportunities for performance upgrading. The techniques used for improving the speed also result in faster edge rates at the outputs of these devices. As edge rates get faster, printed circuit board traces and back plane wiring appear transmissive at shorter distances. More and more interconnections between circuits now have to be treated as transmission lines. This scenario leads to a requirement for higher dynamic drive at the outputs of most high–speed circuits in order to drive low impedance transmission lines and to sustain high levels of DC current if the traces or backplane wiring are terminated at the far end.

This simultaneous requirement for high speed and high drive has certain important implications. First, the high speed in most CMOS integrated circuits is achieved by improved device processing and topology. Internal nodes slew faster and transistors reach their saturation current more rapidly, resulting in a higher rate of change of current (di/dt) in all switching transistors. Since most outputs of glue logic and interface devices are designed to handle high levels of dynamic current, the rate of build–up of current is particularly severe in the output transistors. When several outputs switch simultaneously, the total build–up of current in the common ground or Vcc lead inductance can be substantial (of the order of 200mA/ns to 300mA/ns) and can develop a large transient potential difference between the device power trace (ground or V_{cc} trace) and the external power plane. The term "lead" used here refers to the combination of bonding wire and package pin. A specific area of interest is the simultaneous switching of several "sink" transistors during the logic HIGH to LOW transition and the resultant transient potential difference between the chip ground and the external ground plane. This phenomenon is the simultaneous switching noise on the device (chip) ground plane and is commonly referred to as "GROUND BOUNCE".

Second, the high dynamic drive currents will cause very fast voltage edges at the switching outputs of the device subjected to predominantly capacitive loads. For example, a load capacitance of 50pF (equivalent of 6 to 7 typical CMOS inputs) will be discharged at a rate of 2V/ns during the high–to–low output transition if the dynamic drive current of the output sink transistor is 100mA. Such rapid edge rates will make relatively short PCB traces look like transmission lines. For example, a 2V/ns edge rate will make a typical trace of 6 inches or more look transmissive. These fast edges will contribute to system noise due to ringing, overshoots and undershoots on the signals, EMI and RFI due to sharp output voltage transitions and cross–talk between two adjacent signal lines on a PCB surface.

In this application note we will discuss the phenomenon of GROUND BOUNCE, its contributing factors and some design and application guidelines for minimizing the effects of ground bounce.

THE "GROUND BOUNCE" PHENOMENON

Figure 1 shows the equivalent circuit of a typical CMOS output buffer stage with the package parasitics and the external load.

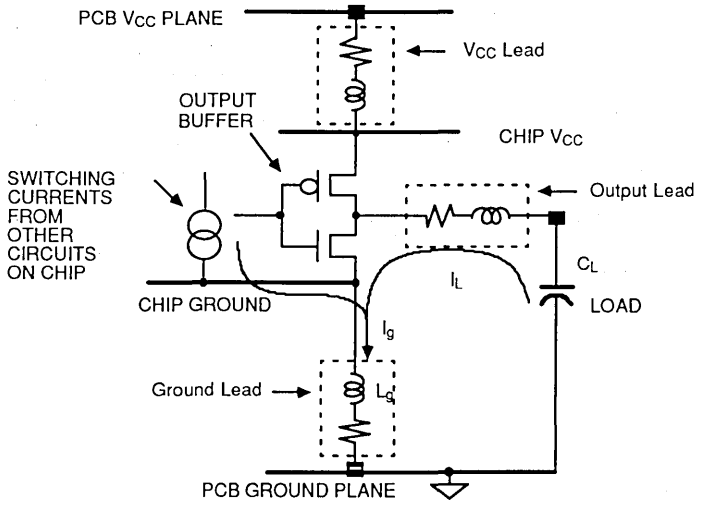

Figure 1. Output Buffer with External Parasitics

The parasitic components which influence ground bounce are; (a) inductance and resistance of the ground bond wire and pin, (b) inductance and resistance of the output bond wire and pin, and (c) load impedance. For first order analysis, the parasitics associated with the V_{CC} terminal can be ignored. Also the external ground plane is assumed to be ideal.

During the output high to low transition, the sum of output load current and all switching current through the internal gates of the device flows through the ground lead. The rate of change of this current (di/dt) develops a voltage drop across the ground lead inductance (Lg) and causes a positive ground bounce or an overshoot in an otherwise quiet ground. This positive bounce is normally followed by an undershoot coincident with the voltage waveform on the output terminal. The amplitudes of both positive and negative ground bounce are a function Lgdi/dt and of the number of outputs switching simultaneously. The ground bounce phenomenon can be clearly observed at an unswitched "LOW" output of a device by switching several other outputs simultaneously from logic HIGH to LOW. Figure 2 shows a typical output voltage transition and the corresponding ground bounce as observed at the unswitched LOW output.

The positive ground bounce is primarily the result of the rate of change of current (dig/dt) through the ground lead inductance. This rate is determined by the rate at which the gate to source voltage (Vgs) of the sink transistor changes. During the early part of the output fall time, the ground voltage rises while the output voltage (at the drain of the transistor) falls, forcing the sink transistor into the linear region. The transistor then behaves like a resistor Ron (the "on" resistance of the transistor in the linear region). For the remainder of the output voltage excursion, the equivalent circuit at the output can be treated like a resonant L–C–R circuit formed by the ground and output lead inductance, load capacitance and the total resistance in the loop which includes Ron. The oscillation frequency is determined by the net values of L and C while the damping is determined by L and the total resistance in the loop.

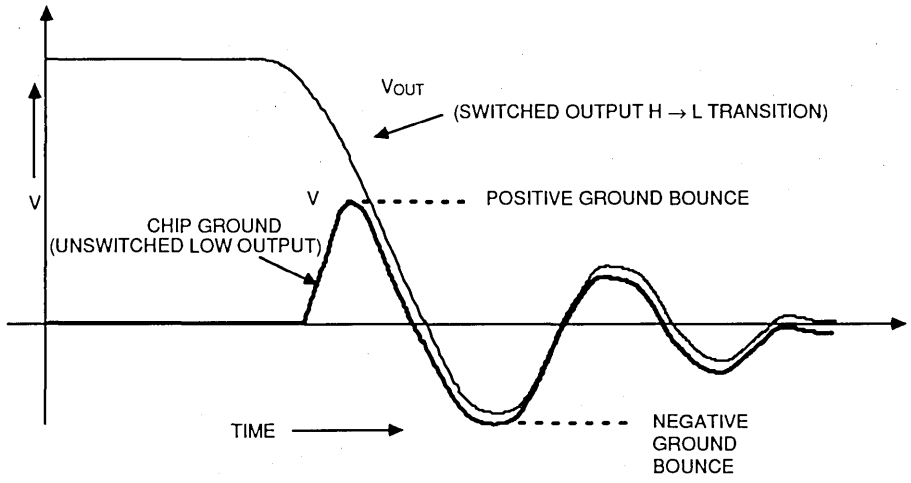

Figure 2. Ground Bounce Waveform

Ground bounce is also generated during the output LOW to HIGH transition. However, the magnitude of this ground bounce is much smaller because of the absence of load current in the ground lead.

GROUND BOUNCE MEASUREMENT

There is no industry standard *per se* for measuring ground bounce. However, the method most commonly used by IC vendors and customers alike is based on observing the disturbance of the logic LOW level of an unswitched output of a multiple output device while switching all other (or several other) outputs from HIGH to LOW state. Figure 3 shows the schematic for measuring ground bounce on a device such as the FCT244 octal buffer. One output is in the LOW state while 7 outputs are switched simultaneously. The load on each output consists of a 50pF capacitor to ground in parallel with a 500Ω resistor to ground. Two outputs are connected to the oscilloscope; one for observing the HIGH to LOW transition of a "switched" output and the other for observing the ground bounce on the "quiet" output. At these outputs, the 500Ω load is split into a 450Ω resistor in series with the 50Ω input impedance of the scope probe. Alternatively, a 500Ω load resistor can be returned to ground and a high impedance probe connected to the device output pins.

With careful layout, proper bypassing to filter out high frequency noise and with a good oscilloscope and probes (bandwidth of at least 400 MHz), it is possible to observe the ground bounce on the internal ground of the chip by observing the voltage at the unswitched "LOW" output whose sink transistor operates in the linear region and provides a "Kelvin connection" to the chip ground.

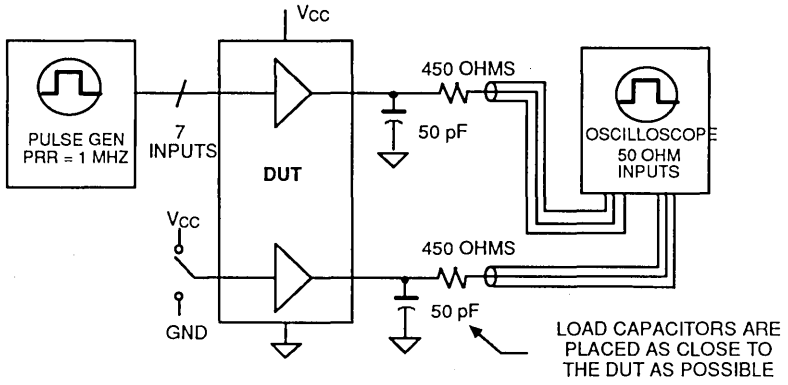

Figure 3. Ground Bounce Test Circuit

A scheme similar to the one shown in Figure 3 can be adapted for any multiple-output circuit. It can also be modified (by changing the load on the switched outputs) to observe and measure ground bounce during HIGH Z to LOW transitions in devices with 3-state control.

THE RELATIONSHIP BETWEEN GROUND BOUNCE AND SPEED

In CMOS circuits, the effective channel length (Leff) is the primary determinant of speed. However, for a given topology, this parameter also determines the saturation current (dynamic drive current) in the output sink transistor. A shorter Leff results in a faster device, but at the same time gives a larger di/dt in the sink transistor. Therefore, there is a direct correlation between ground bounce (caused by di/dt) and speed. This relationship is shown in Figure 4 where the positive ground bounce is plotted as a function of t_{PHL} for an FCT244 device in PDIP, SOIC and LCC. The ground bounce is measured at room temperature and V_{CC} = 5V using the test method shown in Figure 3.

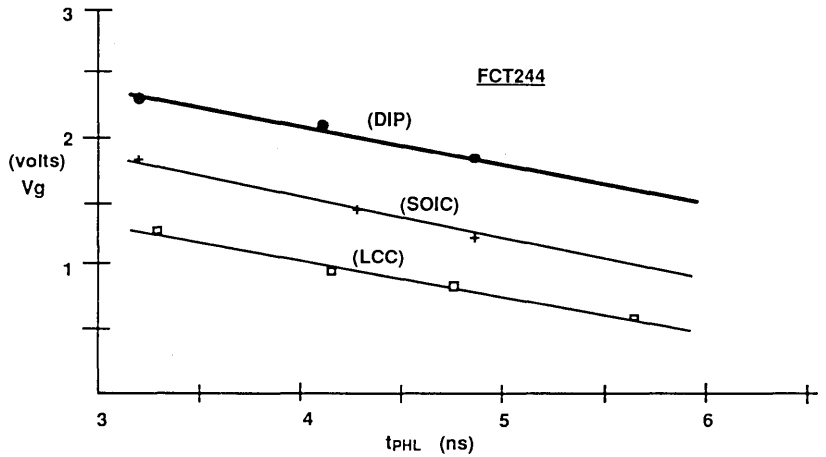

Figure 4.

Figure 4 illustrates two important points. First, because faster devices show a higher amplitude of ground bounce, one must exercise caution when comparing different logic families or different vendors for ground bounce. The samples to be compared should be in the same type of package and their propagation delays should be in close proximity. Second, package parasitics (ground lead inductance in particular) have a significant impact on the magnitude of ground bounce. In a standard DIP package, the corner pin ground lead inductance (pin #10 in a 20 pin package) is around 12 nH. In an SOIC this inductance is only about 7 nH and shrinks to around 4 nH in an LCC. The difference in ground bounce amplitude for different packages is clear from the above graph.

EFFECT OF NUMBER OF OUTPUTS SWITCHING

Ground bounce increases as more outputs switch HIGH to LOW simultaneously. Actual measurements indicate that the relationship is not linear. The reason is as follows. When the chip ground voltage rises due to the Ldi/dt effect, it modulates the gate–to–source voltage (Vgs) of the sink transistor and limits the peak current in the transistor. As more outputs switch simultaneously, the peak current in each transistor actually decreases, although the total current in the ground lead increases. This "diminishing returns" effect results in a non–linear relationship between ground bounce and the number of outputs switching simultaneously.

Figure 5 shows the ground bounce for an FCT244 octal buffer in a PDIP package measured on pin #18 under nominal operating conditions.

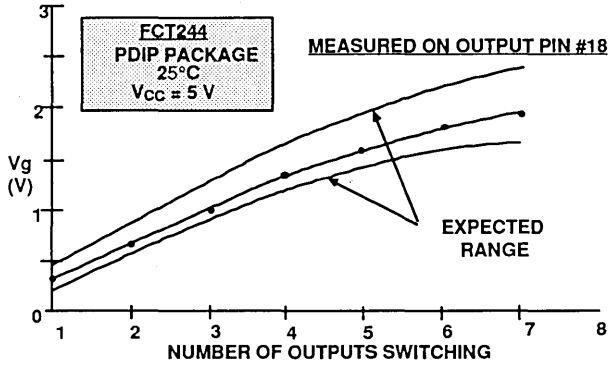

Figure 5. Simultaneous Switching Effect on Ground Bounce

EFFECT ON DEVICE PERFORMANCE

Ground bounce causes a variety of effects in the application environment as described below:

1. The most commonly observed effect is the noise on a "quiet" logic LOW output level in a device when several other outputs switch from high to low simultaneously. If the amplitude of the positive ground bounce exceeds the input threshold of the device driven by it, then all noise margin disappears and the driven device may recognize the noise as a legitimate input transition. A work–around for this problem is to allow some settling time before the signals at the output of the device are treated as valid. This solution generally applies to combinatorial paths only. A large positive transition on certain control signals such as CLOCK, LATCH ENABLE, RESET, etc. can cause loss of data. Such a problem can only be solved by taking steps to reduce the magnitude of the positive ground bounce below the recognition level (threshold) of the device.

2. Changes in the chip ground voltage disturb the thresholds, or trip points, of internal gates. This can cause non–monotonic output transitions that look similar to the effect of short unterminated transmission lines. Often this is not a serious issue.

3. The phenomenon described in (2) also causes a skew or a separation between edges of several outputs switching simultaneously. This skew is a function of the number of outputs switching. Figure 6 shows the effect of simultaneous switching on output skew for an FCT244 device used as a clock driver. The actual measurements were made under worst case commercial temperature and V_{CC} conditions for speed.

In critical clock driving applications, the absolute magnitude of output skew can be reduced by using devices in SOIC or LCC packages. Switching fewer outputs per device will further reduce the skew. However, this approach has to be weighed against the device to device skew if more packages have to be used as a result.

4. The most serious effect of ground bounce is associated with the loss of dynamic noise margin which results in the loss of stored data in latches and registers. This loss of noise margin is often caused by the negative ground bounce which follows the high to low transition of several simultaneously switching outputs (see Figure 2). Simply stated, the undershoots on the chip ground lower the input threshold, or trip point, of the device. This has the same effect as an input making a LOW to HIGH transition relative to the chip ground. If the undershoot is large enough to bring the input threshold near the logic LOW level of any of the inputs held LOW (with reference to the external ground plane), all dynamic noise immunity in the input stage of the device is destroyed. The apparent LOW to HIGH transition of clock (or latch enable) and any logic "LOW" data inputs of registers (or latches) will have the effect of losing stored "LOW" data which is now replaced by "HIGH" data.

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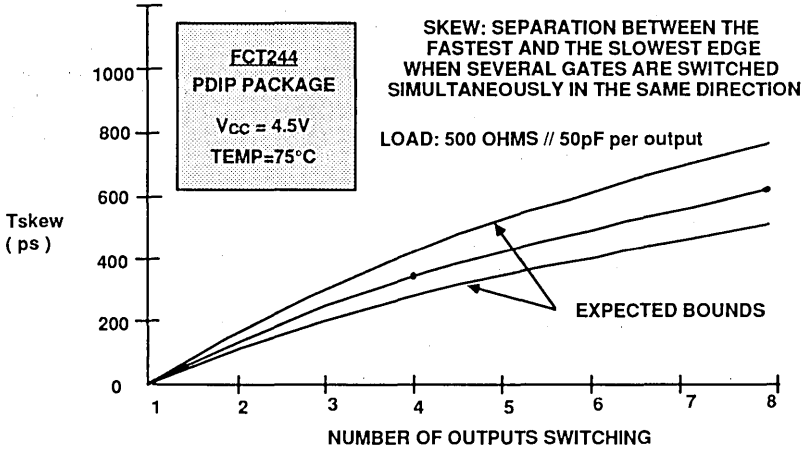

Figure 6. Effect of Simultaneous Switching on Output Skew

SOLUTIONS TO THE GROUND BOUNCE PROBLEM

Ground bounce is a pervasive phenomenon. It can be minimized or circumvented, but rarely eliminated since the parasitic inductance cannot be totally removed from the package. The solutions to the ground bounce problem take essentially two forms; (a) minimizing the effects of ground bounce and (b) minimizing the magnitude of ground bounce.

To minimize the effects of ground bounce, the design should be made "ground bounce tolerant". This can only be done at the expense of system throughput, since additional time must be allowed for the ground bounce to settle. As a result, the benefit of using high speed logic is partially negated.

The techniques for minimizing the magnitude of ground bounce take many forms. They are generally aimed at reducing either the parasitic inductance, or the amount of di/dt or both. These techniques are discussed in some detail below.

Using Smaller Packages

Since ground bounce is the voltage induced in the ground lead inductance by the rapid rate of change of current through it, there is a direct correlation between the amount of inductance and the magnitude of ground bounce. Ground lead inductance can be reduced by using packages with smaller internal cavities and lead dimensions. For example, for corner V_{CC} and GND configuration, the typical ground lead inductance for a 20 or 24 pin Plastic DIP package is of the order of 12 nH to 15 nH. This inductance drops to about 7 nH in an SOIC package and to about 4 nH in an LCC package. Figure 7 shows the effect of package lead inductance on the positive ground bounce for an FCT244 device.

Another method of reducing ground lead inductance is to arrange the pad layout such that the power pins (particularly the GND pins) are at the center of the package for the shortest lengths. Although this is an acceptable solution, it raises standardization and compatibility issues on industry–standard functions. This choice does exist for new functions and as an addition to existing standard functions.

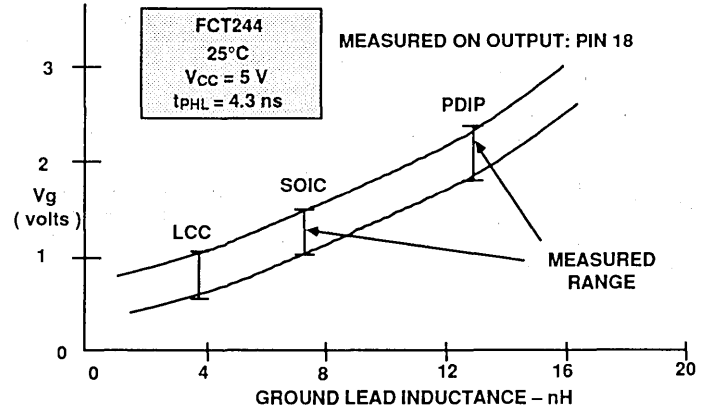

Figure 7. Effect of Package Lead Inductance

Series Damping

di/dt can be reduced either by limiting the magnitude of the peak current (Imax) *through the ground lead* or by slowing down the build-up of the total ground lead current during the output transition. The value of Imax depends on the size of the output sink transistor as well as on the load. Since this is a dynamic phenomenon, the peak current depends more on the amount of energy stored in the load capacitance.

One effective method of limiting the magnitude of Imax is to use a series damping resistor at the output. During the output transition, this resistor comes in series with the "on" resistance of the output buffer and limits the peak current, and hence the di/dt. Figure 8 shows the effect of series damping resistance on ground bounce for an FCT244 device.

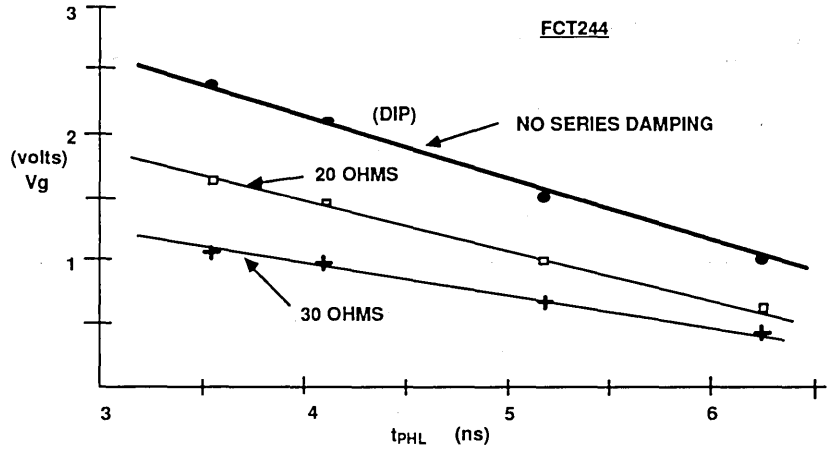

Figure 8. Effect of Series Damping on Positive Ground Bounce

As seen from the figure above, the series damping resistor causes a significant reduction in ground bounce. However, it is important to understand the implications of using series damping. Since the total output impedance is significantly higher, the transmitted signal is attenuated at the driving end; the attenuation being determined by the source impedance ($R_O + R_S$) and the loaded transmission line impedance (Z_L). R_O is the "on" impedance of the output circuit. This attenuation limits the amplitude of the first incident wave. Therefore, the series damping technique must be used with caution and is not recommended if first incident wave switching is desired. This subject is covered more thoroughly in the Application Note entitled "*SERIES TERMINATION*". The series damping resistor, if properly chosen, does have the advantage of limiting overshoots and undershoots on the transmitted signal without increasing system power dissipation.

The series damping resistor also decreases the magnitude of negative ground bounce and the undershoot on HIGH to LOW transitions. Therefore, series damping is effective in driving CMOS memories, particularly DRAMs where undershoots on input signals are undesirable.

Reduced Output Swing

Another technique for reducing ground bounce relies on limiting the energy stored in the load on the device output(s). If the voltage swing at the output is limited, less energy stored in the load. For example, if the output swing is limited to 3.3 volts nominal (similar to most bipolar or BiCMOS totem-pole outputs) instead of rail-to-rail, the energy stored in the output load can be decreased by a factor of 2.5:1 for a given load capacitance. This results in a smaller positive as well as negative ground bounce.

There is a beneficial side effect of this method. Since the high to low transition starts from a lower voltage level, the fall time component (the time taken for the output to switch from the logic HIGH level to the 1.5V measurement level) of t_{PHL} is smaller than that for a rail-to-rail transition. This translates into an improvement in t_{PHL}. However, since speed improvement is not the primary objective, some or all of this speed improvement can be sacrificed in order to further reduce the simultaneous switching noise. This can be achieved by means of a circuit configuration which provides a smaller initial di/dt during the logic HIGH to LOW transition. The resulting degradation in the output fall time cancels the speed improvement. In practice, about 40 improvement in ground bounce (relative to rail to rail swing output) can be obtained for the same speed. The FCT-T family of products introduced by IDT has been designed using this approach. Figure 9 shows the ground bounce characteristics for IDT74FCT244T/AT devices in PDIP and SOIC packages in comparison with the IDT74FCT244/A.

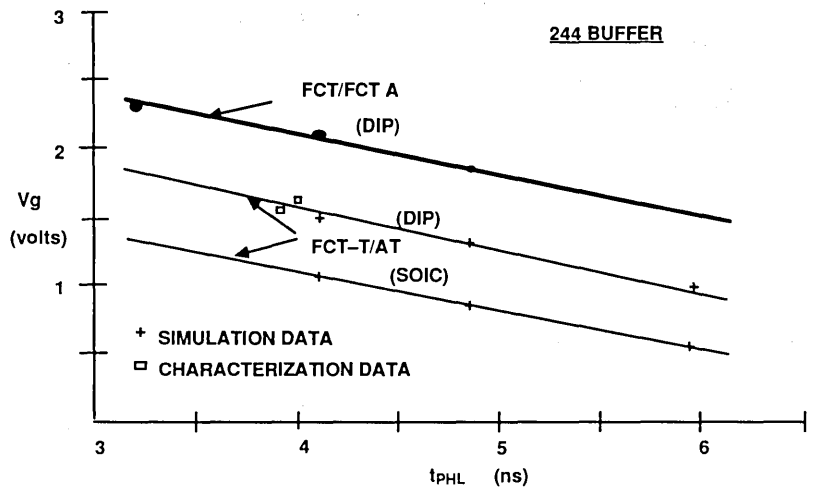

Figure 9. Improved Ground Bounce in FCT–T Family

SUMMARY

The requirement for high speed and high drive results in the phenomenon of ground bounce or simultaneous switching noise in high speed logic and interface circuits. The effects of ground bounce range from a noise spike on a quiet output to data loss in registers and latches. The magnitude of ground bounce can be reduced by using smaller packages with lower ground lead inductance, by switching fewer outputs of a device simultaneously, or by using a series damping resistor in the rail–to–rail swing FCT logic. The new FCT–T logic family is designed to offer much smaller ground bounce at the same speed by reducing the output voltage swing and by controlling the di/dt in the ground lead during the output transitions.

Integrated Device Technology, Inc.

USING HIGH–SPEED LOGIC

APPLICATION NOTE AN–48

By Suren Kodical

This application note gives some general guidelines and recommendations for using high speed logic such as FCT, FCT A and FCT B family of products.

POWER DISTRIBUTION

1. Use Ground and V_{CC} planes on multi–layer boards.
2. On two–layer boards with no V_{CC} and Ground plane, use a "grid" type ground distribution system to equalize ground potential at different points on the P C board.
3. Use Power Distribution Elements – PDEs (conductor–dielectric–conductor) to reduce characteristic impedance. Use separate PDEs for devices that switch large amounts of sink and source currents.
4. Do not use jumper wires for ground connections.
5. Provide a separate "noisy" ground distribution for high current drivers, particularly those driving backplanes.
6. Place high current driving circuits near their loads. For example, place backplane drivers at the edge of the board.
7. Make adequate provision for supplying transient energy to handle PC trace impedance and load capacitance. This is done by connecting individual bypass capacitors across the power pins of high current switching circuits.
8. Use low–inductance, ceramic disk capacitors (4700 pF to 0.1 uF) for high frequency filtering. These can be used in parallel with normal bypass capacitors.

SIGNAL TRACES

1. Treat the PC board traces as transmission lines. A conservative rule of thumb is to consider a trace as a transmission line if the unloaded signal transition time at the driving end equals the round–trip propagation delay for the trace in question. Typically, the transmission line delay is 0.15 ns per inch, or 0.3 ns for one inch round–trip. That means, for a transition time of 2 ns, a trace longer than 7 inches should be considered as a transmission line.
2. To minimize cross–talk between signal traces, avoid running sensitive signal lines close to traces connected to high current drivers.
3. Any signal lines that cross each other should be placed at right angles to further reduce cross–talk.

DEVICE SELECTION

1. Select devices which offer the largest amount of "real" noise margin. Ground noise due to simultaneous switching of multiple outputs causes a loss of dynamic noise immunity in the logic low state. Therefore, it is important to improve "low level" noise immunity. This can be achieved by:

a. Using CMOS outputs to drive inputs of "storage" devices such as latches and registers. This will offer better noise margin when compared to driving with devices with bipolar outputs which have a higher logic low level due to the offset voltage of the Schottky–clamped NPN sink transistor.

b. Reducing DC loading, i.e. reduce the fanput, on the outputs of devices that drive the data and control inputs of latches and registers.

c. Using devices with "hysterisis" on the inputs. This will further improve dynamic as well as static noise margin.

d. Use of series damping resistors (25 to 35 ohms) at the output of latches and registers will reduce the undershoot on the device intenal ground due to simultaneous switching of multiple outputs of the device. This undershoot normally follows the overshoot (also referred to as the ground bounce).

Series damping will overdamp the series L–C–R circuit formed by the parasitic ground path inductance, load capacitance and the low impedance of the sink transistor.

2. Several measures can be taken to reduce the power supply noise — both ground bounce and V_{CC} bounce:

a. Contention should be avoided on devices connected to a bus. Although bus contention is not detrimental to the device in a normal application, it causes very large positive and negative di/dt in the ground and V_{CC} paths. Such contention has the same effect as charging a very large load capacitance.

b. Series termination (i.e. series damping resistors) will also reduce the magnitude of the ground bounce by limiting the maximum transient current and thereby decreasing the total energy transferred to the parasitic inductances.

c. Use of local high frequency filtering will minimize the propagation of noise on ground and V_{CC} traces.

3. Avoid running control lines through a device that drives data/address buses.
4. Since the magnitude of ground and V_{CC} noise is a direct function of parasitic inductance, if all other conditions are unchanged, much benefit is gained by using packages with lower bond–wire and lead inductance. Thus, surface mount packages (SO, LCC, PLCC, etc.) will offer lower levels of ground and V_{CC} noise than standard DIP packages
5. Output drive "overkill" should be avoided. In non–critical paths, use of low–drive circuits will generally reduce the overall supply noise.
6. In very high speed circuits, minimize the loading per device to reduce total load capacitance.

SUMMARY

A combination of high speed (particularly fast edge rates) and high drive contribute to increased noise in power supply path as well as in signal paths. Much care is needed to minimize such noise so that maximum performance benefit is derived from the FCT family of high speed logic products.

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Printed in the U.S.A.

Integrated Device Technology, Inc.

CHARACTERISTICS OF PCB TRACES

APPLICATION NOTE AN–49

By Suren Kodical

Printed circuit board traces carrying high speed digital signals can behave like transmission lines for fast edge rates of the driving signal. The transmission line effects can cause signal distortion, overshoots, undershoots and crosstalk between adjacent lines. It is therefore important to understand this behavior for trouble–free board design. In this application note we discuss the transmissive effects of PCB traces, the relevant electrical parameters and a simple technique for measuring unloaded or loaded characteristic impedance.

PCB TRACE AS A TRANSMISSION LINE

A PCB trace is normally regarded as a very low impedance medium which carries electrical signals from one point to another. This is true for most signals with relatively slow edge rates (long rise and fall times). However, when a trace is subjected to fast edge rates, its behavior changes completely. It behaves like a transmission line with a certain characteristic impedance Z. This impedance now presents a load to the driving circuit. In addition, the transmissive trace introduces a finite signal delay from source (driving end) to destination (receiving end). The equivalent circuit for a transmission line, represented by distributed L+R and C is shown in Figure 1.

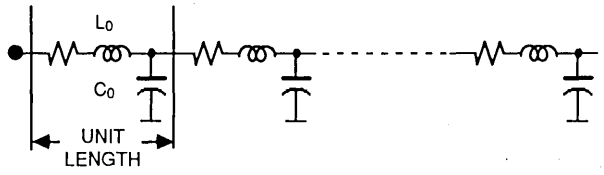


Figure 1. Transmission Line — Equivalent Circuit

In this schematic,

L_0 = Inductance of the trace per unit length, and

C_0 = Capacitance per unit length.

For the purpose of this discussion the series resistance can be ignored, thus treating the PCB trace as a "lossless" transmission line. The subscript "0" implies that the inductance and capacitance pertain to the "unloaded" condition, i.e. the inductance is the "self inductance" of the trace and the capacitance is that offered by the dielectric separating the trace in question from the adjacent conducting media.

Two important parameters can be derived from L_0 and C_0. The first one is Z_0, the characteristic impedance of the trace. The second parameter is T_0, the propagation delay per unit length of the trace. It should be noted that the parameter Z_0 is independent of the length of the trace.

$$Z_0 = (L_0/C_0)^{1/2}, \text{ normally defined in ohms} \quad (1)$$

$$T_0 = (L_0C_0)^{1/2} \text{ per unit length, normally defined in nanoseconds} \quad (2)$$

Example

A typical *MICROSTRIP* PCB trace (a dielectric separating the trace from the ground plane on one side and free air on the other 3 sides of a rectangular trace cross–section) which is 10 mils wide and 1.5 mil thick separated from the ground plane by 15 mil glass–filled epoxy has a typical $C_0 = 2$ pF/inch and $L_0 = 10$ nH/inch. Using the above equations, we get $Z_0 = 70\ \Omega$ and $T_0 = 0.15$ ns/inch. The table in Figure 2 gives various transmission line geometries and their parameters.

TYPE	GEOMETRY	Z_0 ohms	T_0 ns / inch
CO–AX		50 – 125	0.13
WIRE OVER GROUND		70 – 170	0.14
MICROSTRIP LINES		30 – 150	0.15
STRIP LINE		15 – 100	0.19
PC BOARD TRACES		50 – 200	0.16

Figure 2. Transmission Line Geometries

EFFECT OF LOADING

The concept of an unloaded transmission line applies to point–to–point connections which consist of a driver and a receiver at the two ends of a trace, with no connections to the trace in–between. Most often, a PCB trace is tapped at several points and connected to inputs of several ICs. Clock, R/W, Chip Select lines and Data and Address buses are examples of this. These IC inputs represent a quasi–distributed load to the driving circuit. Whereas bipolar TTL inputs present a DC leakage path to V_{CC} in addition to the input capacitance, most CMOS inputs offer a capacitive load (ignoring the effects of input lead inductance).

As a result, the transmission line parameters are modified under the loaded condition, because the additional distributed load capacitance must be taken into account in addition to the unloaded distributed capacitance C_0.

To simplify the discussion, let us assume that the distributed load capacitance is represented by C_L per unit length, as shown in Figure 3.

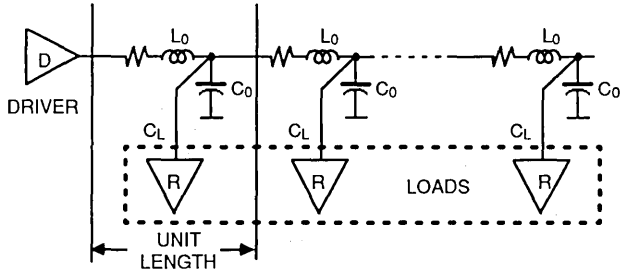


Figure 3. Loaded Transmission Line

Taking the effect of C_L into account, the loaded trace impedance Z_L and the loaded transmission delay T_L per unit length are given by:

$$Z_L = Z_0 [\, C_0 / (C_0 + C_L)\,]^{1/2} \text{ ohms} \quad \ldots\ldots (3)$$

$$\text{and } T_L = T_0 [\, (C_0 + C_L)/ C_0\,]^{1/2} \text{ per unit length} \quad \ldots\ldots (4)$$

Example

Consider a clock driver driving a bank of registers in DIP package, mounted 0.5 inches apart. Assuming a typical input capacitance of the clock pin of 5 pF, the PCB trace is loaded with 5 pF capacitance every 1/2 inch. This is equivalent to a distributed C_L of 10 pF per inch.. Using the example for the PCB trace given earlier, the loaded parameters can be calculated using equations (3) and (4):

$$Z_L = 70\ [\, 2 / (\, 2+10\,)\,]^{1/2} = 70[\, 1/6\,]^{1/2} = 70/2.45 = 29\ \Omega \text{ and}$$

$$T_L = 0.15 \times 2.45 = 0.37 \text{ ns/inch.}$$

This example illustrates the need for a significantly higher drive as the trace impedance drops from 70 Ω to 29 Ω. It also shows the impact of such loading on clock skew caused by the increase in transmission delay.

WHEN IS THE PCB TRACE TRANSMISSIVE?

As a general statement, a PCB trace looks like a transmission line for fast edge rates of the transmitted signal. To quantify this, a commonly used **rule of thumb** is:

TREAT A PC BOARD TRACE AS A TRANSMISSION LINE IF $T \leq 2L \times T_L$.

In this equation, T = output transition time (rise or fall time)
T_L = loaded transmission delay per unit length.
$T_L = T_0$ for the point–to–point case
L = Length of the PCB trace

Example

Consider the loaded transmission line in the example cited above. If the clock driver has an output transition time of 5 ns, the length at which the PCB trace should be treated as transmissive is given by:

$$L = T / 2T_L = 5 / (2 \times 0.37) = 6.8 \text{ inches.}$$

It is clear that, with slower edge rates a driver can drive longer traces without transmission line effects. The table in Figure 4 shows the limiting signal line length for different logic families based on typical edge rates for each of the families and typical unloaded signal traces.

LOGIC FAMILY	SIGNAL LINE LENGTH* (INCHES)
LS	25
S , AS	11
F, ACT	8
AS, ECL	6
FCT, FCT A	5

*Length above which the signal trace looks like a transmission line.

Figure 4. Signal Line Length vs Logic Family

This table shows that, as we go to faster logic devices, it becomes more critical to understand the transmission–line effects. Note that the signal lengths given in the table are not guarantees for any logic family. The actual limiting signal length is a function of trace and board characteristics, trace loading and the edge rates of individual devices in any logic family.

MEASUREMENT OF PCB TRACE PARAMETERS

Since both Z_L and T_L depend on board layout and loading, a simple practical method of determining these two parameters is useful. Described below is one such method which is particularly applicable to traces with well–distributed loading.

Equipment required:

1. Pulse generator with known source impedance (typ. 50 Ω) and capable of rise and fall times faster than 2.5 ns.
2. Oscilloscope: >350 MHz bandwidth.
3. High impedance scope probes.

Method

a. If the source impedance of the pulse generator is unknown, it can be easily obtained by observing the unloaded output waveform of the pulse generator, and then loading the pulse generator output with a resistance that will halve the amplitude of the original signal. The value of this load resistance is the source impedance (Rs) of the pulse generator.

b. Connect the pulse generator and the oscilloscope to one end of the PCB trace. Use a minimum of 9 inches of PCB trace. Insert the devices that will form the distributed load on the PCB trace. See Figure 5.

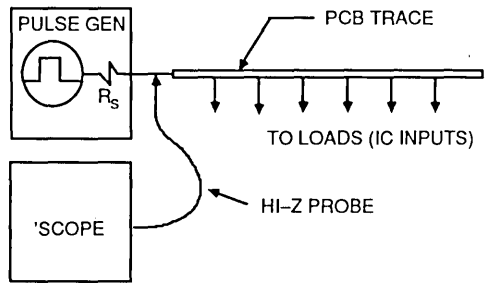


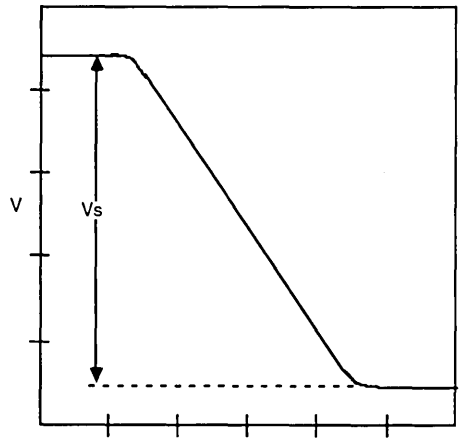
Figure 5. Test Set–Up for Measuring PCB Trace Parameters

c. Set up the pulse generator to obtain a 5V amplitude square wave of 1 MHz frequency. Adjust the rise and fall times to get 30 ns (10% to 90%). These slow edges ensure that the PCB trace behaves like a lumped load and not like a transmission line. Overshoots and undershoots on the waveform are avoided. Record the amplitude (V_s) observed on the oscilloscope *under these conditions* as shown in Figure 6A.

d. Now change the setting on the pulse generator to get the fastest rise and fall time. Observe the high to low transition on the oscilloscope. Note that there is a step in the output transition as shown in Figure 6B. Record the amplitude of the first segment of the output transition (V_t) and time interval between the start of the first transition and the start of the second transition ($2L \times T_L$).

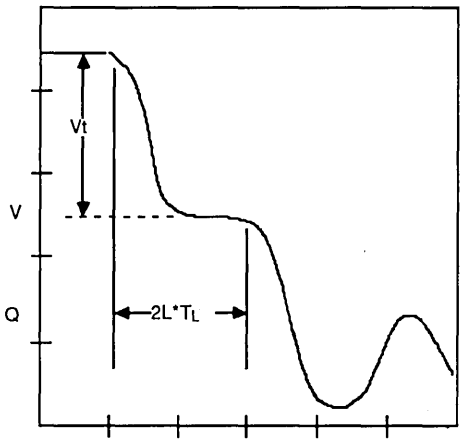
e. Determine the characteristic impedance of the loaded PCB trace (Z_L) by the formula:

$$Z_L = R_S \times [\, V_t / (V_s - V_t) \,]$$



Measuring Vs with Slow Edge Rate

Figure 6A.



Measuring Vt and T_L with Fast Edge Rate

Figure 6B.

The line propagation delay to the end of the trace is given by T_L.

Example

In a test performed on a 9 inch trace, we get $R_S = 45\ \Omega$, $V_t = 2.8$ V and $2L \times T_L = 6$ ns. Then,

$$ZL = 45 \times [\ 2.8 / (5 - 2.8)\ ]$$
$$= 57\ \Omega.$$
$$TL = 6 / (2 \times 9)$$
$$= 0.33 \text{ ns per inch}$$

THE IMPORTANCE OF PCB TRACE CHARACTERISTICS

The relative values of source impedance (R_S) of the driving circuit and the loaded characteristic impedance of the transmission line (Z_L) determine the effectiveness of driving transmission lines. As Rs increases for a given ZL, the amplitude of the transmitted component of the waveform (V_t) decreases. If the transmitted wave does not cross the threshold of a receiving device, the receiving device may not respond to the signal at the driving end (see Figure 6B) until the reflected wave reinforces the signal after a turn–around delay along the PCB trace. This implies that if a driver is driving a PCB trace from one end, the receiver nearer to the driver will respond *after* the receiver at the far end of the PCB trace. Such skew may be unacceptable in certain conditions.

The relative values of trace impedance and the load impedance at the far end also determine the amount of reflection and hence the overshoots and undershoots on the waveform. By understanding the implications of transmissive traces, a designer can choose the right termination and drive capability of the driving circuit to derive the maximum benefit.

SUMMARY

This application note describes the effect of fast edge–rates on the behavior of PCB traces. A simplified method for measuring the trace parameters in a given application environment is shown. The procedure discussed here can be extended to fully loaded backplanes.

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Integrated Device Technology, Inc.

SERIES TERMINATION

APPLICATION NOTE AN-50

By Suren Kodical

Series termination is one of several forms of terminating transmissive lines. In this bulletin we discuss the pros and cons of series termination and the effect of termination impedance on simultaneous switching noise (a.k.a. Ground Bounce).

WHY TERMINATE?

With the constant push for higher speeds, particularly in the area of standard logic and bus interface products, system designers have to deal with devices with fast edge rates. At the same time, high packing density of multi-layer boards results in PC board traces with low loaded impedance and long transmission delays. This combination of fast edge rates and low transmission line impedance requires the system designer to pay careful attention to PCB design in order to maximize the benefits of today's high-speed logic. As more and more devices on the boards go to CMOS technology, typical nets consist of outputs with fast edges looking into transmission lines with some distributed capacitance along the line or lumped capacitance of CMOS IC inputs at the end of the line or a combination of both. In the absence of some form of termination, overshoots and undershoots on the signal can impose bandwidth limitation on the system, or subsystem due to settling time requirements or, even worse, can cause false triggering and data loss.

Termination of transmission lines is the time-honored method of improving signal quality. There are several forms of termination:

a. **Parallel or shunt termination:** a single resistor terminated to either V_{CC} or GND at the end of the PCB trace. For backplanes, termination is provided at each end.

b. **Series termination:** a single resistor is connected between the output node of the driver and the PCB trace or any other transmission line being driven.

c. **Thevenin termination:** two resistors form a potential divider at the far end of the transmission line. The junction of the two resistors goes to the transmission line and the two ends typically go to GND and V_{CC}. This type of termination is commonly used on backplanes at both ends.

d. **RC termination:** an R-C series combination is connected between the transmission line and GND at the far end.

Each of the termination schemes listed above has certain advantages and disadvantages. A detailed discussion of the relative merits of these schemes will be part of a separate application note. In this issue, we will focus on **SERIES TERMINATION**.

SERIES TERMINATION

Figure 1 shows a typical case of a series terminated driver connected to a load via a PCB trace.

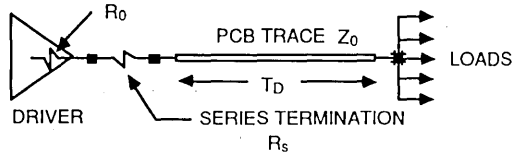

Figure 1.

The effective output impedance of the driver is now the sum of device source impedance (R_0) and the series terminating resistance (R_S). This modified output impedance of the driver comes in series with the characteristic impedance (Z_0) of the PCB trace and forms a potential divider for the incident signal. Therefore, the signal that propagates down the trace is a fraction of the "open-circuit" signal at the driving end. The magnitude of the transmitted wave is given by the following equation:

$$V_t = V_s [Z_0 / (R_0 + R_s + Z_0)] \quad \text{.....(1)}$$

This equation shows that, as the total source impedance approaches the characteristic impedance of the line, approximately half of the incident wave will be transmitted to the other end of the trace. Since the load impedance is much larger than Z_0 due to the high input impedance of the CMOS devices, most of the transmitted wave is reflected. As a result, overshoots and undershoots on the signal are minimized at the receiving end. If $R_0 + R_S$ is much smaller than Z_0, a larger portion of the incident wave is transmitted down the trace. Since most of it is reflected, such a condition will cause overshoots and undershoots at the receiving end. Figure 2 shows the effect of series termination under prefect matching (total source impedance equals trace impedance).

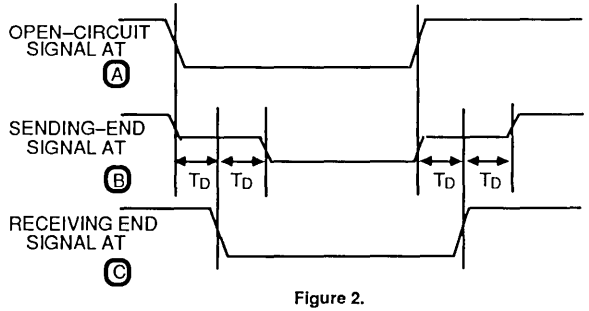

Figure 2.

The example shown highlights some important points:

1. For the best signal quality, the series terminating resistor should be chosen such that the total source impedance ($R_O + R_S$) is close to the characteristic impedance of the PCB trace. It is not essential that the two quantities match exactly. It is, however, important to ensure that the total source impedance is not greater than the trace impedance. Otherwise, multiple reflections may be needed to obtain the entire signal transition at the receiving end.
2. The waveforms in Figure 2 clearly show the effect of series termination on the waveform at both the sending end A and receiving end B. For a perfectly matched condition, the signal will attain the final value at the sending end after a round-trip delay ($2T_D$), although it will attain the final value after one transmission delay (T_D) at the receiving end. If loads (several IC inputs) are distributed along the PCB trace and are driven by the driver at one end, this condition results in signal skew which may be unacceptable. Therefore, series termination may not be the most suitable form of termination for distributed loads. Of course, the ratio of source to trace impedance can be adjusted to ensure that the threshold of the receiver is crossed on the **first incidence of the transmitted wave**, but this is normally at the expense of some undershoot and overshoot during signal transitions.
3. There is no limit to the number of lumped loads (as shown in Figure 1) that can be used, provided that the total DC loading does not reduce the static noise margin because of a voltage drop across the series terminating resistor. This implies that series termination is well-suited to drive inputs of CMOS devices because of their very low input current requirements. The primary limitation to the number of CMOS loads is the additional delay due to the total input capacitance being driven.
4. When series termination is used with lumped loads, the distance between the indvidual loads should be kept to a minimum. If the loads being driven are spread apart, a preferred method of driving them from one source is to make several groups of loads and drive each group from the driving source via individual transmission lines with their own series termination resistors. The driver should of course be capable of handling this additional transmission line loading.
5. It is clear that the series termination does not add any power dissipation to the system. It is, therefore, the preferred form of termination if power dissipation is a key consideration.
6. Series termination adds flexibility to the design in that the termination values can be tailored to suit a variety of trace characteristics and timing requirements.

SERIES TERMINATION WITH FCT DRIVERS

Like most TTL-compatible drivers designed to meet the standard DC specifications, the FCT output buffers offer different output impedance in the logic LOW and HIGH states. Typically, the output impedance is 6 ohms in the LOW state and 25 ohms in the HIGH state. Since the internal thresholds of all TTL-compatible devices (independent of technology) are with reference to GND and the noise immunity is normally worse in the logic LOW state, it is important to consider the logic LOW state and the high-to-low transitions when evaluating the effect of terminations.

First, let us consider the requirements for first incident wave switching. The aim is to cause enough voltage swing on the first part of the transmitted wave to cross the threshold of a receiving device close to the driver. For a typical V_{OH} of 4.8V with CMOS P-channel pull-up transistors and specified V_{IL} = 0.8 V for the receiver, the required amplitude of the incident signal is $V_t = V_{OH} - V_{IL} = 4.8 - 0.8 = 4$ V. The open circuit swing is $V_S = 4.8$ V.

Reworking equation #1, we get:

$$Z_O = (R_O + R_S)\ [\ (V_{OH} - V_{IL}) / V_{IL}]$$

Therefore,

$$R_S = Z_O\ [\ V_{IL} / (V_{OH} - V_{IL})\ ] - R_O \quad \text{.....(2)}$$

Using the values for V_S and V_t and for a device source impedance of 6 ohms, the maximum value of series termination resistance which will assure incident wave switching is given by

$$R_S = Z_O\ [\ 0.8 /\ (4.8 - 0.\ )\ ] - 6$$
$$= (0.2Z_O - 6) \text{ ohms}$$

For example, if the PCB trace impedance is 70 ohms, the maximum value of series termination resistance is **8 ohms** to assure incident wave switching. A similar consideration for the low to high transition yields the expression:

$$R_S = Z_O\ [\ (V_{OH} - V_{IH}) / V_{IH}\ ] - R_O \quad \text{.....(3)}$$

For a V_{OH} = 4.8 V, V_{IH} = 2.0 V and a source impedance of 25 ohms in the logic high state, the maximum value of series termination resistance to assure incident wave switching is,

$$R_S = (1.4Z_O - 25) \text{ ohms}$$

Again, if the PCB trace impedance is 70 ohms, the maximum value of Rs is **73 ohms**. This indicates that the high to low transition is the worst case.

The above example shows that a requirement for incident wave switching will impose severe restrictions on the series termination resistance due to the high to low switching case. Since the termination value is much less than the trace impedance, a certain amount of overshoots and undershoots are to be expected on the output waveform at the far end of the PCB trace. In effect, the incident wave switching requirement is in conflict with signal integrity for FCT logic devices with rail to rail output switching *when using series termination.* If signal integrity is the primary consideration, then the series termination has to be chosen to match the trace impedance. However, signal skew has to be tolerated when driving a transmission line with distributed loading. Alternatively, series termination should be limited to driving lumped loads at the far end of the transmission line (PCB trace).

In high-speed switching circuits, series termination offers another advantage. When driving predominantly capacitive loads, the series resistor serves to limit the peak current in the output pull-down transistor and therefore the resultant di/dt in the parasitic lead and bond wire inductance. This has the beneficial effect of limiting the amount of ground bounce (induced by the L.di/dt effect) as a result of simultaneous switching of high drive outputs.

SUMMARY

Series termination is an effective method for minimizing overshoots and undershoots on signals with fast edges and for reducing the amount of ground bounce caused by simultaneous switching. An understanding of the device output characteristics, particularly the output impedance values, is required to properly determine the value of series termination in order to assure incident wave switching.

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Integrated Device Technology, Inc.

POWER DISSIPATION IN CLOCK DRIVERS

APPLICATION NOTE AN-51

By Suren Kodical

Power dissipation in switching circuits is discussed in this bulletin, particularly with reference to CMOS clock driver circuits. The IDT54/74FCT244 octal buffer is used as an example to compare the power supply current in CMOS, bipolar and bipolar–based BiCMOS technologies over a wide range of operating frequencies.

POWER DISSIPATION COMPONENTS

There are two components of power dissipation in integrated circuits. One is the steady–state component. This is the dissipation when all inputs are held at some fixed voltage level. The other component is frequency dependent and is generally referred to as the dynamic component.

In CMOS and CMOS–based BiCMOS circuits, the steady–state component is further divided into two sub–components; the quiescent power supply current (I_{CC}) primarily due to device leakage and the quescent power supply current when inputs are at TTL high level (ΔI_{CC}). This latter component applies to circuits with TTL compatible inputs. In bipolar and bipolar–based BiCMOS circuits, no such distinction is made and it is customary to specify power supply current for a given logic state on the output(s).

The dynamic component of power dissipation (I_{CCD}) is dominant in CMOS circuits because most of the power is dissipated in moving charge in the parasitic capacitors of CMOS gates. Therefore, the simplified model of a CMOS circuit consisting of several gates looks like one large capacitor which is charged and discharged between power supply rails. For this reason, a parameter called C_{PD} (power dissipation capacitance) is often specified as a measure of this equivalent capacitance and is used by the designers to estimate the dynamic power supply component. In the bipolar technology, the dynamic component is generally very small in comparison with the steady–state component because internal voltage swings are small.

Since power supply parameters are traditionally specified under "unloaded" condition, a comparison of power dissipation for a given device type (FCT244 with F244, for example) based on data sheet numbers alone can be misleading. For a true "apples–to–apples" comparison, the effect of capacitive load on the device should be taken into consideration. This is particularly true in the case of clock drivers which drive heavy capacitive loads and operate at high frequency. Under these conditions, the dynamic power dissipation component due to output loading could be significant in both bipolar and CMOS circuits. This is illustrated in the following section by using the '244 Octal Buffer as an example.

'244 Example

Consider the '244 as a clock driver with 30 pF load on each of the 8 outputs, operating at room temperature and V_{CC} = max. Power dissipation of IDT's FCT244 is compared with F244 (FAST™) and TI's BCT244. Data sheet numbers are used where applicable.

FCT244

First, we need to determine the C_{PD} for the device. Since $C_{PD} = I_{CCD}/V$ in pF if I_{CCD} is expressed in μA/MHz, we can determine C_{PD} using the max. limit specified for I_{CCD} in the data sheet. Therefore,

$$C_{PD} = 250 / 5.5 = 45 \text{ pF}$$

When the device is loaded with 30 pF capacitance per output, the dynamic dissipation component increases due to load. The loaded value is given by,

$$I_{CCD} \text{ (loaded)} = \{ (C_{PD} + C_L) / C_{PD} \} I_{CCD}$$
$$= \{ (45 + 30) / 45 \} 250 \text{ μA / MHz / bit}$$
$$= 0.42 \text{ mA / MHz / bit.}$$

When all eight outputs are switching simultaneously, the total I_{CCD} (loaded) is 3.3 mA/MHz.

If quiescent power dissipation is ignored, the above equation can be used to determine the total power dissipation at any frequency when the input levels are CMOS compatible. For the case where the inputs are driven from a bipolar TTL device, the ΔI_{CC} component needs to be added in order to obtain the total power dissipation. Assuming a 50 duty cycle, for ΔI_{CC} (max.) of 2 mA, this static I_{CC} component is 8 mA. Figure 1 shows the power dissipation versus frequency for both conditions.

F244

The specified power dissipation is I_{CCL} = 90 mA and I_{CCH} = 60 mA. For a 50 duty cycle, the steady–state dissipation is 75 mA. In addition, the dynamic dissipation component appears due to the external load capacitance and the output pin capacitance of the device. For C_L = 30 pF and C_{OUT} = 10 pF (assumed), the dynamic component can be derived:

$$I_{CCD} \text{ (loaded)} = 40 \text{ pF x } (4.3 \text{ V} - 0.3 \text{ V}) \text{ in μA/MHz.}$$
$$= 160 \text{ μA / MHz / bit}$$

where the 4.3 V – 0.3 V represents the voltage swing (for V_{CC} = 5.5V) on the total load capacitance. For 8 outputs switching simultaneously, I_{CCD} is 1.28 mA/ MHz. The total dissipation as a function of frequency is also shown in Figure 1.

BCT244

The BCT family from TI is developed with a bipolar–based BiCMOS process. Therefore, the power dissipation characteristics are similar to F244. The steady–state dissipation is 57.5 mA for a 50 duty cycle. The dynamic component of the dissipation is 1.28 mA/MHz. The total power dissipation versus frequency is again shown in Figure 1.

The graph in Figure 1 shows that over a wide range of frequencies the power dissipation of FCT family of circuits is much less than that of BCT and F families, even under heavy capacitive loading.

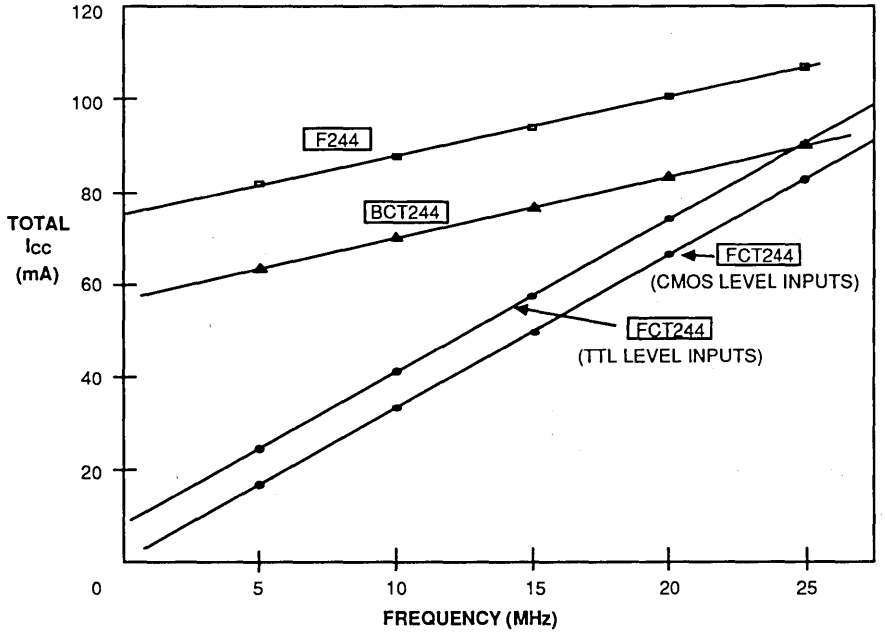

Figure 1. Total Icc vs Frequency

SUMMARY

A simple method for calculating "real" power dissipation in an operating environment is shown by using '244 as an example. This method can be extended to any other product and can be used to determine realistic power consumption if the loading and effective operating frequency can be estimated for each device.

Integrated Device Technology, Inc.

FCT OUTPUT STRUCTURES AND CHARACTERISTICS

APPLICATION NOTE AN-52

By Suren Kodical

INTRODUCTION

The FCT family of products has gone through an evolution in terms of die size, process technology (critical dimensions) and circuit implementation. Originally, the family of products was derived from the Z–step gate arrays ("4004" gate array for small gate count and "8000" array for large gate count). Later, a "shrunk" version of the smaller array was developed to obtain performance improvement. This array is called the Y–step. Recently, some of the high volume runners have been "customized", i.e. redesigned to minimize the die size and get some performance improvement with a more efficient topology. These customized versions are called the W–step devices. The current FCT portfolio consists of a mix of Z, Y and W step devices. This bulletin describes the output structures used in different steppings and the corresponding output characteristics for the logic HIGH and LOW states.

"4004" Z– STEP OUTPUT BUFFER

The schematic for the buffer used in the "4004" Z step devices is shown in Figure 1. This output consists of an N–channel "sink" transistor which turns on in the logic low state at the output and maintains a logic low voltage close to GROUND for normal loading.

The pull–up or "source" circuit consists of a combination of a P–channel transistor, an N–channel transistor and an NPN bipolar transistor with a series current limiting resistor. This circuit configuration is designed to give a resistive characteristic during the LOW to HIGH transition at the output.

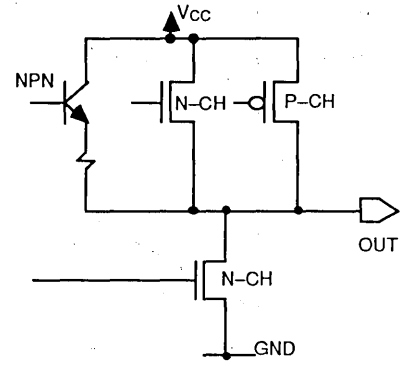

Figure 1. Step Output Structure

The output V–I characteristics for the Z step output structure in the logic HIGH and LOW states are shown in Figures 2A and 2B, respectively.

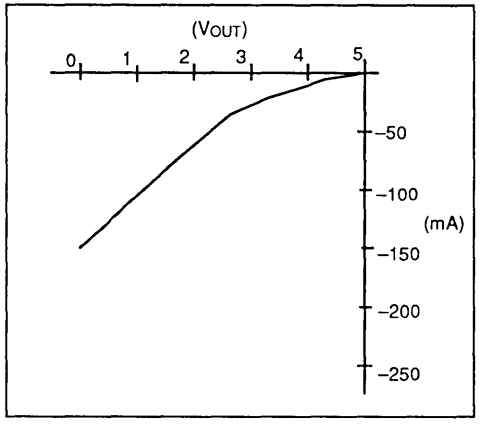

Figure 2A. "4004" Z Step Logic "High" Characteristics

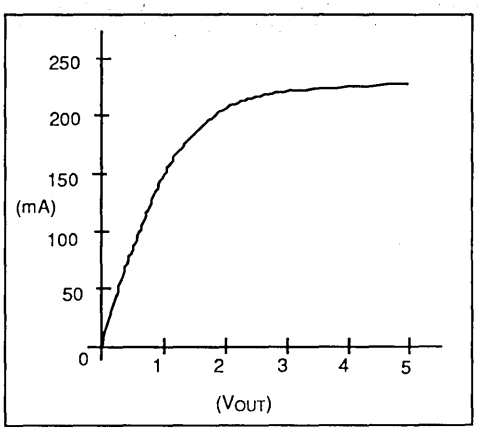

Figure 2B. "4004" Z Step Logic "Low" Characteristics

The output characteristic in the logic HIGH state is dominated by the current limiting resistor in series with the NPN pull–up transistor. As the output reaches the V_{CC} rail, the output characteristic is primarily influenced by the P–channel transistor. In the logic LOW state, the output characteristic is that of a large N–channel pull–down transistor. Note that the characteristics shown in Figure 2 represent typical process parameters at 25°C.

Y–STEP OUTPUT BUFFER

The circuit schematic for the Y step output buffer is shown in Figure 3.

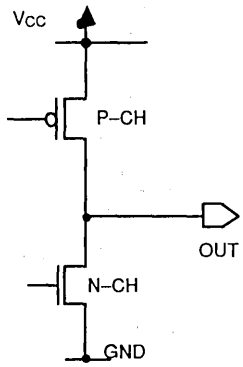

Figure 3. Y–Step Output Structure

This output structure is designed to get shorter propagation delays. The output characteristic in both HIGH and LOW states is non–linear as shown in Figures 4A and 4B, below.

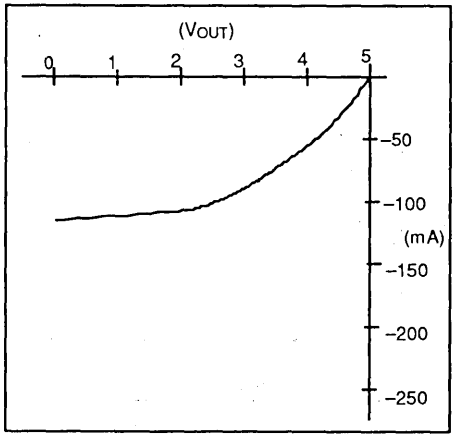

Figure 4A. Y Step Logic "High" Characteristics

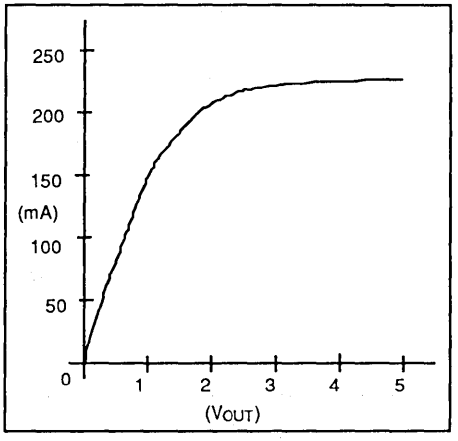

Figure 4B. Y Step Logic "Low" Characteristics

W STEP & "8000" Z STEP OUTPUT BUFFER

The schematic of the output buffer used in the "8000" Z step gate array as well as the W step devices is shown in Figure 5. The structure consists of a parallel combination of P–channel and N–channel transistors in the pull–up circuit and a large N–channel transistor in the pull–down circuit.

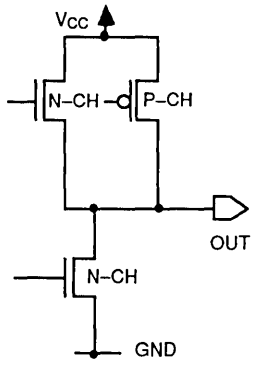

Figure 5. W Step and "8000" Z Step Output Structure

The pull–up structure yields an almost resistive characteristic in the logic HIGH state. The characteristic in the logic LOW state is again non–linear due to the N–channel transistor.

These output characteristics are shown in Figures 6A and 6B.

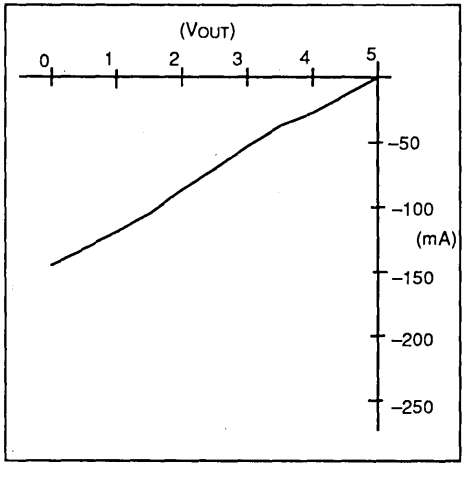

Figure 6A. W & "8000" Z Step Logic "High" Characteristics

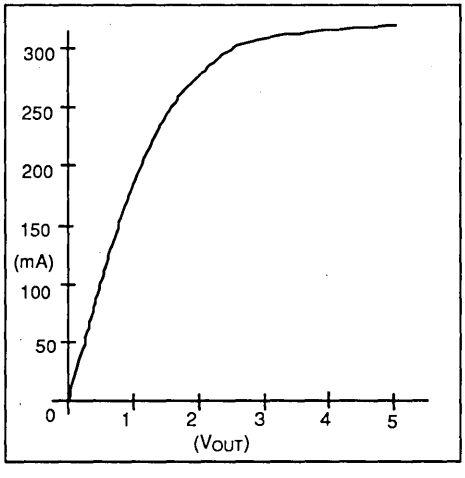

Figure 6B. W & "8000" Z Step Logic "Low" Characteristics

SUMMARY

The output V–I characteristics are determined by the circuit implementation and transistor geometries. Output buffer schemes and the corresponding typical characteristics for FCT devices manufactured in the Z, Y and W stepping are shown in this bulletin.

The characteristics are intended to aid the designer in developing nominal circuit simulation models so that the effect of driving different types of lumped and transmissive loads can be evaluated. In order to develop suitable models, the customer should first determine the stepping for the subject device. This information can be obtained by contacting IDT's LOGIC Marketing group.

Integrated Device Technology, Inc.

POWER–DOWN OPERATION

APPLICATION NOTE AN–53

By Suren Kodical

INTRODUCTION

In a **POWER–DOWN** mode, a device operates with a supply voltage that is lower than the normal operating range of 5V ± 5 for commercial grade and 5V ± 10 for military grade. *This should not be confused with the "low–power dissipation standby mode" of CMOS static RAMs where part of internal circuitry is shut off to reduce standby power.* The power–down mode is used to either conserve power in a part of a system or to provide a battery back–up in fault–tolerant systems. The devices operating in the power down mode are expected to co–exist with other devices which are connected to normal power supply rails in the same system. This bulletin discusses the use of our FCT devices in the power–down mode.

DESIGN FEATURES

All FCT and AHCT devices currently manufactured by IDT support rail–to–rail output voltage swing. This is a benefit in the power–down operation because the logic high noise immunity is not compromised. In addition, these circuits have the following design features:

- The inputs (except for I/O ports) do not have a clamp diode to V_{CC} but do have a clamp diode to ground to prevent excessive undershoot on the inputs.
- The outputs have P–channel pull–up transistors to raise output high level close to V_{CC}.

The P–channel devices have a junction diode as an integral part of the geometry. To prevent this junction from floating, the cathode of this diode is tied to V_{CC}, the most positive potential. Similarly, the N–channel transistors used in the output circuit have an integral junction diode whose anode is tied to GND, the most negative potential. Figure 1 shows the diodes associated with inputs and outputs.

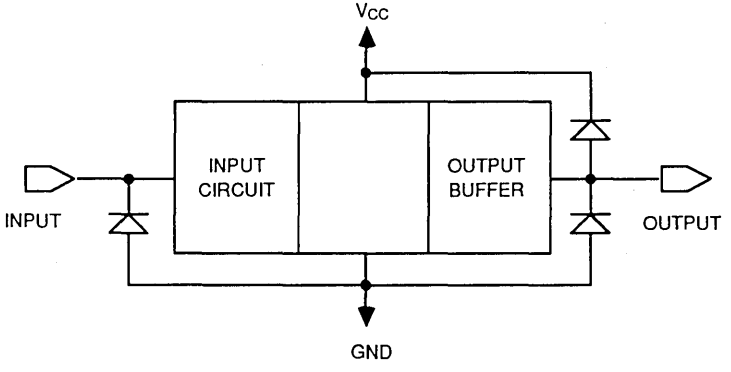

Figure 1. FCT Logic with Parasitic Diodes

POWER–DOWN OPERATION

Consider the case where an FCT or AHCT device operating in the power–down mode (say at a V_{CC} of 3 volts) is driven from another device operating from a higher V_{CC}. Because of the absence of a diode clamp to V_{CC}, there is no current flow from the driving device into the low voltage power supply through the input pin. The FCT and AHCT inputs thus permit power down operation on the input side.

An FCT or AHCT device in the power–down mode can easily drive TTL–compatible inputs or I/O ports, because the TTL–compatible inputs normally demand negligible input current in the logic high state.

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LIMITATIONS

The presence of a diode from the output pin to V_{CC} as shown in Figure 1, however, imposes certain limitations in the power–down operation when the output of a device which is powered down is in the high–impedance state and the bus to which this device is tied is driven by another device operating from a higher V_{CC} (see Figure 2).

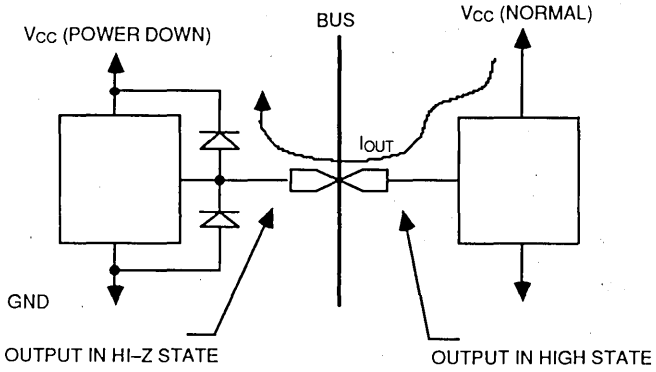

Figure 2.

In this case, the output diode to V_{CC} provides a low impedance path to the lower V_{CC} if the interfacing device output is in the HIGH state and the logic HIGH voltage is in excess of the power–down supply rail by more than a forward diode drop. In such an event, the logic high voltage will be clamped. This is normally not a serious issue if the driving devices have bipolar outputs or N–channel CMOS outputs with reduced voltage swings. However, if the driving device pulls up to V_{CC} and offers a low source impedance, the current into the output of the FCT or AHCT device in the power–down mode can exceed the absolute maximum rating. This situation can be avoided if a current limiting resistor (25 ohms or more) is used in series with the outputs of the device in power–down mode.

A similar restriction applies to I/O ports of devices such as the FCT245 and FCT646 when operating from a lower V_{CC}. The I/O port consists of an input node physically connected to an output which can be put in high–Z state when the port is to be used as an input. The presence of P–channel pull–up transistor in the output circuit adds a parasitic diode to V_{CC} at the I/O port. Therefore, this diode will offer a low impedance path to the lower V_{CC} if the driving device pulls up to the higher (nominal 5V) V_{CC}.

SUMMARY

The design of the FCT and AHCT input structures facilitates use of these devices in a dual–rail system or in a power–down mode to conserve system power or to provide a battery back–up. Although the design of the output structures imposes a limitation in certain power–down situations, it can be overcome easily.

Integrated Device Technology, Inc.

FCT–T LOGIC FAMILY

APPLICATION NOTE AN–54

By Suren Kodical

INTRODUCTION

Present day systems and board level products have two important characteristics; higher clock rates to obtain improved throughput and higher packing density to reduce space and cost. System designers are demanding higher speed and user friendliness from IC vendors to cope with the tight timing requirements and with the switching noise induced by high–speed TTL circuits. As discussed in the Application Note entitled "***SIMULTANEOUS SWITCHING NOISE***", high speed and simultaneous switching noise (particularly Ground Bounce) go hand in hand. For a given speed, less board–level noise translates into reduced design time, lower rework cost and better quality of outgoing product. Since most standard "glue" logic elements such as buffers, transceivers, latches and registers are used for their high drive capability and speed, they can also become the primary source of noise. Therefore, vendors of such high–speed circuits are faced with the challenge of providing "*friendly but fast*" glue logic to the performance–driven user.

IDT has met this challenge with the FCT–T family of standard logic which is designed to give the best speed/noise trade–off to the system designer. This new logic family features reduced output voltage swing and a high current output stage designed to minimize simultaneous switching noise. In this application note, we discuss this TTL–compatible family in terms of its features and benefits, product characteristics, performance curves and certain special features.

WHAT IS FCT–T LOGIC?

The FCT–T family is form, fit and function compatible with the industry standard FCT family of high–speed, high–drive logic from IDT. The FCT–T family offers the same speed grades (standard, A, B and C) as the FCT family while generating much lower level of noise (particularly ground bounce). It is, therefore, backward–compatible with the FCT family of products in all applications where rail–to–rail switching at the output is not essential. Typical FCT–T output logic levels are 0.1V in the logic LOW state and 3.3V in the logic HIGH state.

The FCT–T family also includes several products with *power off/up/down disable* feature. These are intended for backplane driving, especially in applications which require "hot insertion" capability for the boards without interrupting system operation.

FCT–T FEATURES AND BENEFITS

The key features of FCT–T family are described below:

TTL Level Outputs — The output pull–up circuit has been modified to offer a quiescent output HIGH level of about 3.3V, similar to most bipolar and BiCMOS output stages. This feature makes FCT–T truly compatible with existing bipolar and BiCMOS functions and thus offers an attractive low–power alternative without any performance penalty.

Ground Bounce Control — The output pull–down circuit has been modified to control the rate of build–up of current in the "sink" transistors so that the Lgdi/dt effect is minimized (Lg is the total inductance in the ground return path) and ground bounce is reduced for a given speed. This feature also slows the output edge rates and minimizes transmission–line effects on PC boards.

Input Hysteresis — Input buffers (TTL–to–CMOS translators) have been designed to offer 200mV (typical) hysteresis in order to improve both high and low level noise immunity. This feature decreases propensity for data loss or oscillations in high noise environment and offers immunity to noise superimposed on slow input signal transitions.

Variety Of Speed Grades — The FCT–T family offers the following speed grades:

FCTxxxT — corresponds to FCTxxx
FCTxxxAT — corresponds to FCTxxxA
FCTxxxBT — corresponds to FCTxxxB
FCTxxxCT — corresponds to FCTxxxC

The system designer can choose the speed grade necessary for optimum performance. It is important to note, however, that there is a strong correlation between the amount of simultateous switching noise and speed. Therefore, designers using higher speed devices should pay careful attention to board layout, termination, decoupling and package selection in order to get the maximum benefit.

Compatibility — The FCT–T logic family is compatible with all other TTL compatible logic families (AS, ALS, FAST, BCT, etc.). The reduced output swing makes the FCT–T outputs look very much like standard bipolar outputs. The static noise margin when driving from an FCT–T device is the same as that with any bipolar output device in the logic HIGH state. In the logic LOW state, the typical static noise margin is greater with the FCT–T family than with any bipolar logic family because of the absence of a voltage offset usually seen in bipolar Schottky outputs in the logic LOW state. Input thresholds are set to be within the 0.8V and 2.0V range.

Power–Off Disable — Certain members of the FCT–T family are designed to offer the power off/up/down disable feature. These devices with 3–state control maintain high–impedance state at their outputs during power supply ramping and power down (i.e., V_{CC} = 0V) if the Output Enable pin is conditioned to *disable* the outputs. This feature is attractive, and often essential, for backplane drivers in applications which require *hot insertion.* These applications include on–line transaction systems, factory floor automation, critical medical life support systems, etc. This feature is currently offered in double density devices with high drive capability, since these devices offer board space savings in backplane environment.

JEDEC Standard 18 Compliance — FCT–T specifications meet or exceed the requirements of JEDEC Standard No. 18 entitled **"Standard for Description of 54/74FCTXXXX, Fast CMOS TTL Compatible Logic"**.

FCT–T CHARACTERISTICS

In this section, we discuss various characteristics of the FCT–T family. This information is offered to the system designer to understand the operation of a device, boundary conditions and interface requirements in terms of transmission line driving.

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DC CHARACTERISTICS TABLE

Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ± 5%
Military: T_A = –55°C to +125°C; V_{CC} = 5.0V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IL}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IH}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max. V_I = 2.7V	Except I/O Pins	—	—	5	µA
			I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max. V_I = 0.5V	Except I/O Pins	—	—	–5	µA
			I/O Pins	—	—	–15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max.; V_I = V_{CC} (Max.)		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min.; I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.; V_O = GND[3]		–60	—	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL.	2.4	3.3	—	V
			I_{OH} = –8mA COM'L.				
			I_{OH} = –12mA MIL.	2.0	3.0	—	V
			I_{OH} = –15mA COM'L.				
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} Line Drivers	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} Standard, 3–State and 800 Series	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.; V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

Figure 1.

The table in Figure 1 is similar to that for the FCT family of products. Significant differences are summarized below. Then individual parameters are discussed in detail with the aid of circuit schematics and V–I characteristics.

Differences between FCT–T and FCT

1. V_{OH} limit of 2.4 volts is guaranteed at –6mA military and –8mA commercial for the FCT–T family. The corresponding currents are –12mA and –15mA, respectively, for FCT.

2. Maximum limit of –225mA has been added to the Ios (Short Circuit Current) specification to maintain compatibility with other TTL–output families.

3. Since the output voltage swing is reduced, low drive (300µA) specifications for logic HIGH and LOW levels have been omitted. Similarly, all specifications at V_{CC} = 3.3V have been omitted, as these CMOS level output specifications are not applicable.

4. Hysteresis specification has been added to indicate the amount of nominal hysteresis built into the design.

5. Static I_{CC} specification has been added to maintain compatibility with other TTL data sheets.

INPUT CIRCUIT AND CHARACTERISTICS

The input circuit for the FCT–T family is shown in Figure 2.

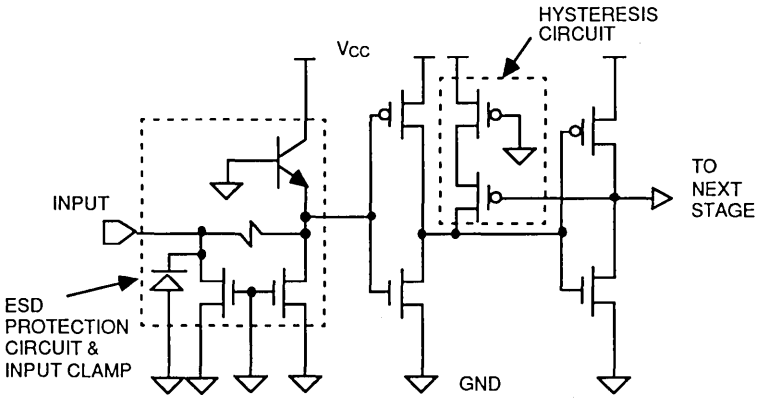

Figure 2. FCT–T Input Stage

The input stage is, in effect, a TTL to CMOS translator. It consists of (a) Input clamp diode to limit input voltage undershoots to approximately one diode below ground, (b) ESD protection circuit, (c) Input buffer designed for TTL threshold with a typical 200mV hysteresis and (d) Inverter which interfaces with the following stage.

Hysteresis is achieved by means of a change in the ratio of P–channel to N–channel transistor areas in the input translator. Typical V–I characteristics of the input stage is shown in Figure 3A and the typical transfer characteristic is shown in Figure 3B.

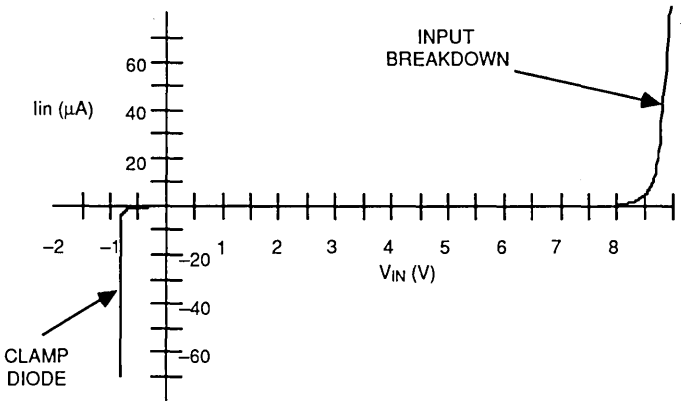

Figure 3A. FCT–T Input V–I Characteristics

The input current in the operating input voltage range is extremely low, in the order of nanoamps because of the very high input impedance of the CMOS gate. At voltages greater than one diode drop below device ground, the input offers low impedance because of the forward–biased input clamp diode. Input breakdown voltage is well outside the normal operating limit of V_{CC} (max).

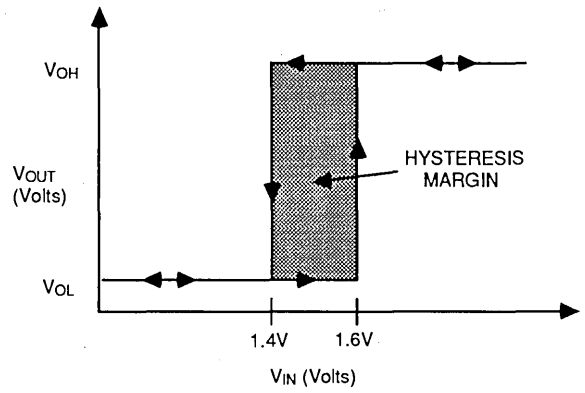

Figure 3B. Input Stage Transfer Characteristics

An important feature of the FCT–T logic family is that all inputs have hysteresis in the input stage transfer characteristic. Hysteresis increases static noise immunity in both logic states and also offers immunity to noise superimposed on slow edge–rate input signals, if the amplitude of the superimposed noise is less than the hysteresis margin.

OUTPUT CIRCUIT AND CHARACTERISTICS

The FCT–T output circuit is designed for a nominal voltage swing of about 3.3V. (In comparison, the FCT family output swing is from rail to rail.) The reduced output swing has certain benefits:

Benefits of reduced output swing

1. The output characteristics of FCT–T logic more closely match those of the industry–accepted Bipolar and BiCMOS logic families (AS, ALS, FAST, BCT, etc.).
2. Nominal threshold of any TTL inputs tied to an FCT–T output is almost in the middle of the output swing. Therefore duty–cycle distortion of signal propagating through a chain of devices is minimized.
3. For the same High–to–Low edge rate, reduced output swing would result in improved t_{PHL} because of smaller output voltage excursion relative to a device with full rail–to–rail output swing. Alternatively, a given t_{PHL} spec can be met with a slower High–to–Low edge rate. In the FCT–T family, we have taken advantage of this latter feature and improved the output circuit to reduce ground bounce as well as the level of radiated noise (EMI and RFI) caused by sharp output transitions and fast edges.
4. Less energy is stored in the output load capacitance when compared with a rail–to–rail swing device. This results in less ground bounce for the same speed when compared with a rail–to–rail switching device.

Output Circuit Schematic

The equivalent circuit of a typical FCT–T output stage is shown in Figure 4.

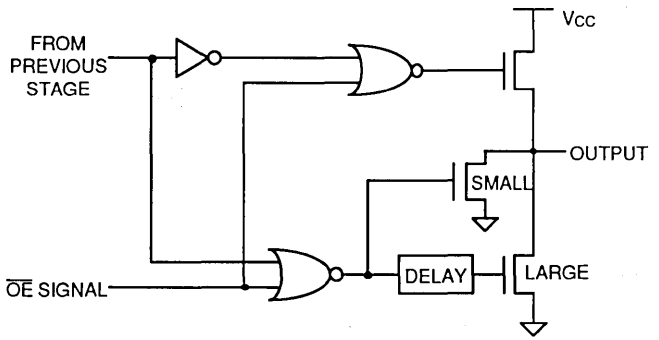

Figure 4. FCT–T Output Stage Schematic

The schematic shown here differs from a traditional CMOS output stage (P–channel pull up and N–channel pull–down) in the following ways:

- An N–channel pull–up transistor is used to obtain a voltage offset in the logic High state, so that the quiescent V_{OH} level is approximately 3.3 volts.
- The pull–down circuit consists of two stages. During the High–to–Low transition, a small N–channel transistor turns on first, followed by a large N–channel transistor after some delay. This arrangement results in a smaller di/dt in the ground return path during the output transition and adequate DC drive in the logic Low state. There are minor variations in the actual implementation of the output stage from mask–set to mask–set. The schematic shown is intended to give the general concept.

DC Output Characteristics (Logic LOW and HIGH States)

Typical DC output characteristics for the logic LOW and HIGH states are shown in Figures 5A and 5B, respectively. These curves are obtained at 25°C and V_{CC} = 5 volts.

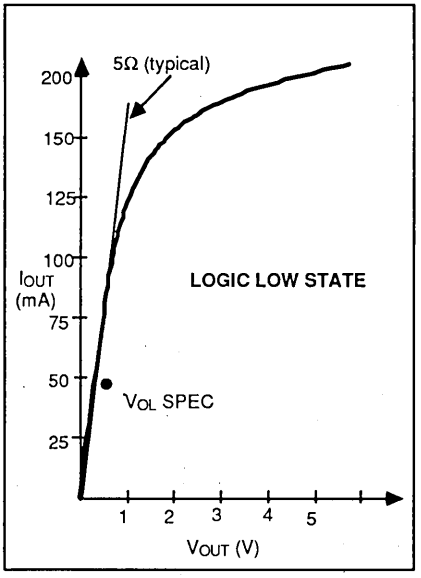

Figure 5A. Output Low Characteristics

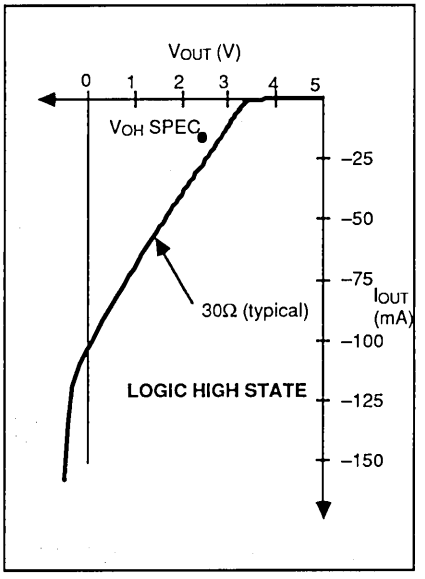

Figure 5B. Output High Characteristics

The output characteristic in the logic LOW state shows high static drive capability and low output impedance in the linear region. Typical output impedance in the LOW state is 5Ω.

The output characteristic in the logic HIGH state has a slope of 30Ω typical. This relatively high output impedance and the reduced voltage swing make the LOW–to–HIGH transition the worst case for incident wave switching. The characteristics are presented here to assist the system designer in determining proper termination based on the application at hand.

DC Output Characteristics (High Z State)

The output characteristics in the High Impedance state are shown in Figure 6 on the following page. The breakdown region for output voltage above V_{CC} depends on the actual circuit implementation.

In the High Impedance state, both pull–up and pull–down sections of the output stage are disabled. Therefore, the output ports exhibit very high impedance in the normal operating range. For output voltages below GND, parasitic junction diodes associated with the N–channel output transistors come into effect and offer very low output impedance to GND as shown by the diode characteristic in Figure 6. For output voltages above V_{CC}, one of two different characteristics can be observed:

7

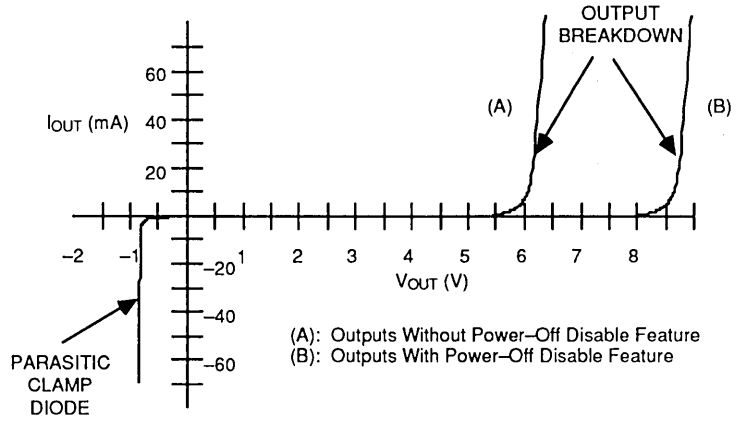

Figure 6. Output High–Z Characteristics

Curve (A): The devices with P–channel transistors in the output stage exhibit low impedance at output voltage greater than a diode above V_{CC}. These devices do not have the *"power–off disable"* feature.

Curve (B): The devices with the "power–off disable" feature show high output impedance at output voltages higher than V_{CC}. The output stage in these devices has been designed to avoid any parasitic junction diode to V_{CC}.

The "power–off disable" feature is discussed in detail later in this bulletin.

POWER SUPPLY CHARACTERISTICS

Components of Power Supply Current

There are three power supply current components in TTL compatible CMOS circuits:

(1) I_{CC} — The quiescent power supply current through the supply pin when all inputs are either at GND or at applied V_{CC}. This current normally represents internal leakages as well as pacakage–related leakages.

(2) ΔI_{CC} — The quiescent power supply current when inputs are held at "TTL levels", and

(3) I_{CCD} — Dynamic current caused by an Input Transition Pair (HLH or LHL). This current is a function of frequency associated with the signal transitions.

The total current $I_C = I_{CC} + \Delta I_{CC} + I_{CCD}$.

The last two components of power supply current are discussed in detail below.

ΔI_{CC} Characteristics

The input stage of a CMOS device draws current from the power supply pin for an input voltage range bounded by V_{tn} and (V_{CC}–V_{tp}) where V_{tn} and V_{tp} are the thresholds of N–channel and P–channel devices, respectively. Within this voltage range, both P and N channel transistors in the input translator stage are on (see Figure 2 for reference). Figure 7 shows the relationship between ΔI_{CC} and input voltage (V_{IN}) for a typical FCT–T input stage.

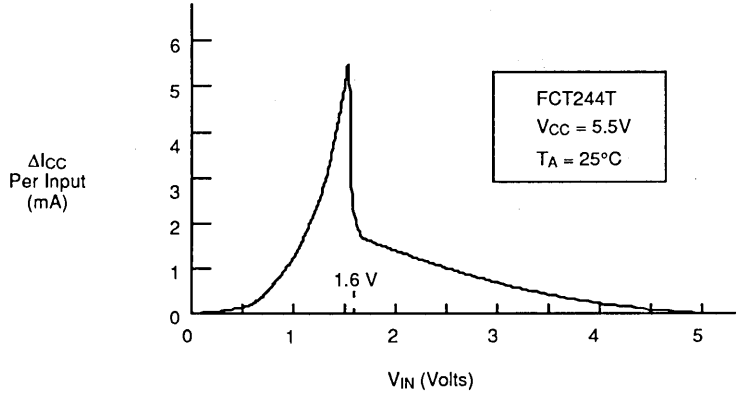

Figure 7. ΔI_{CC} Characteristics

As the input voltage is raised above V_{tn}, the ΔI_{CC} component increases, reaching a peak at the input threshold for the low–to–high transition. The sharp drop in current at threshold indicates the presence of hysteresis which effectively modifies the P–channel to N–channel ratio. As the input voltage is raised further, the ΔI_{CC} component falls because the P–channel transistor is being progressively turned off. Note that the characteristic is plotted "per input". The total current drawn from an IC depends on the number of inputs and the voltage applied to each input. The ΔI_{CC} parameter is specified for an input voltage of 3.4 volts at V_{CC} = max. in the data sheet.

Dynamic Power Supply Current – I_{CCD}

CMOS gates use power from the power supply source to charge and discharge parasitic capacitances when changing logic levels. This power is related to the frequency at which the logic level transitions occur. It is given by the formula:

$$\text{Power} = V \times i = fC_pV^2$$

where f = frequency of logic level transitions,
C_p = parasitic capacitance associated with the gate,
V = voltage change on the capacitor, and
i = average switching current through the power supply path.

The average power supply current is given by $i = fC_pV$. Since this current is a function of frequency, it can be represented in the form of current per MHz and its value is given by C_pV with appropriate units. This is the *dynamic power supply current* for the gate. In a CMOS integrated circuit the total dynamic current is the sum of all such currents and is represented by I_{CCD}.

I_{CCD} is measured with the switching output(s) open, so that there is no influence of capacitance external to the package. Capacitive loading on the switching outputs will increase the measured value of I_{CCD} by an amount equal to the load–dependent fC_LV. Also, input transitions should be from GND to V_{CC} to eliminate any ΔI_{CC} component in the measurement. For devices with multiple identical paths (FCT244T Octal Buffer, for example), I_{CCD} is specified for one bit switching. Figure 8 shows a graph for dynamic power supply current for FCT244T buffer. This graph shows the linear relationship between I_{CCD} and frequency. I_{CCD} characteristic for an FCT244 with rail–to–rail output swing is also shown for comparison. The difference in the current at any frequency is due to the reduced output voltage swing.

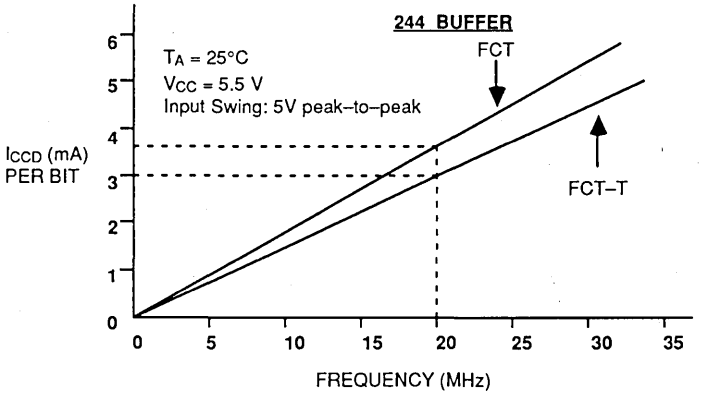

Figure 8. Dynamic Power Supply Current

NOTE: The units for I_{CCD} have the dimensions of current x time. Therefore, this parameter should be treated as "charge". In fact, the JEDEC Standard 18 for FCT logic uses the symbol Q_{CCD} for this parameter. In this application note, the author has chosen the symbol I_{CCD} since the measurement is in terms of current and is also consistent with the data sheets.

Figure 9, below, shows the Power Supply Characteristics table for FCT244T as an example.

SYMBOL	PARAMETER	TEST CONDITIONS		TYP.	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = V_{CC} or GND f = 0		0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V		0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	0.15	0.25	mA/ MHz

Figure 9. FCT244T Power Supply Characteristics

Total Power Supply Current – Example

From the information provided in the table above, the total power supply current can be calculated for a given operating condition. For example, let us assume that the FCT244T is used as a clock buffer, distributing the clock with a fan–out of 8 (one input, 8 outputs) at 25 MHz with 50 duty cycle. This clock distribution is accomplished by tying all inputs together. Output Enable pins are at GND. Inputs are driven from a TTL compatible device.

Typical power supply current I_C (*outputs unloaded*) is calculated as follows:

I_{CC} = 0.2mA

ΔI_{CC} = 0.5(duty ratio) x 8(switching inputs) x 0.5mA = 2mA

I_{CCD} = 25(frequency) x 8(switching outputs) x 0.15mA = 30mA

Therefore,

I_C = 0.2 + 2 + 30 = 32.2mA (typical).

Note that the above example shows the dissipation due to the device alone. In reality, the capacitive loading on the outputs will contribute additional power dissipation and must be taken into consideration for determining power supply requirements. This topic is discussed in depth in the Application Note entitled "*POWER DISSIPATION IN CLOCK DRIVERS*".

Similar calculations can be performed for any device once the operating conditions are known. In more complex devices, as well as in interface devices used in data and address paths, it is necessary to estimate the "average" frequency of operation to determine the total device dissipation under realistic operating conditions.

AC PERFORMANCE

Except for the reduced output voltage swing, the AC characteristics of the FCT–T family are the same as those of the FCT family in terms of operating conditions and limits. Given below in Figure 10 are the performance figures for four FCT–T logic parts for different speed grades. The performance is compared with the popular FAST family of bipolar parts.

FCT–T Speed Grades

DEVICE	74FCT–CT CMOS	74FCT–AT CMOS	74FCT–T CMOS	74F BIPOLAR	PARAMETER
244 Buffer	4.1ns	4.8ns	6.5ns	6.5ns	D to Y
245 XCVR	4.1ns	4.6ns	7.0ns	7.0ns	A to B, B to A
373 Latch	4.7ns	5.2ns	8.0ns	8.0ns	Dn to Qn
374 Register	5.2ns	6.5ns	10.0ns	10.0ns	CLK to Qn

Figure 10. FCT–T AC Performance Comparison

The variety of speed grades offer the system designer a choice in optimizing overall system performance. In many cases, the use of higher speed logic allows the designer a choice of using lower speed memory devices to reduce the overall cost of the system.

AC Performance Over Temperature Range

The AC performance of FCT–T family of products over the operating temperature range is similar to that of the FCT family. A normalized graph of t_{PLH} and t_{PHL} for the FCT244T device is presented in Figure 11 as an example.

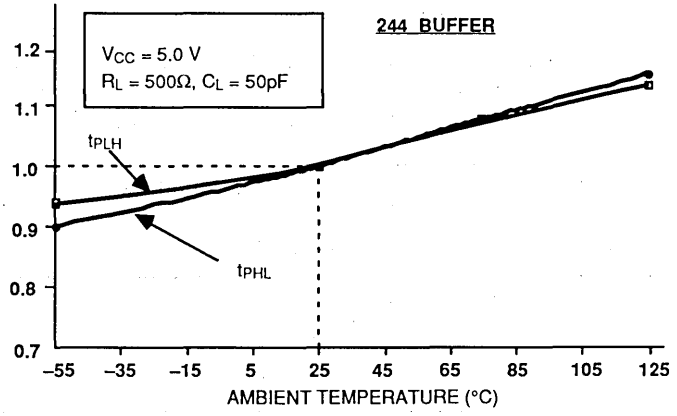

Figure 11. Normalized Switching Characteristics

Simultaneous Switching Noise

One of the primary benefits of FCT–T family of products is the improvement in performance with respect to simultaneous switching noise, or ground bounce, when compared with any CMOS family with rail–to–rail output swing. The combination of a modified TTL output stage and reduced output voltage swing results in a significant reduction in the magnitude of both the positive and the negative components of ground bounce. The relationship between ground bounce and t_{PHL} for the FCT244T is shown in Figure 12. The graph shows the improvement achieved when compared with the FCT family over the same speed range. All measurements are at V_{CC} = 5 volts and 25°C ambient temperature.

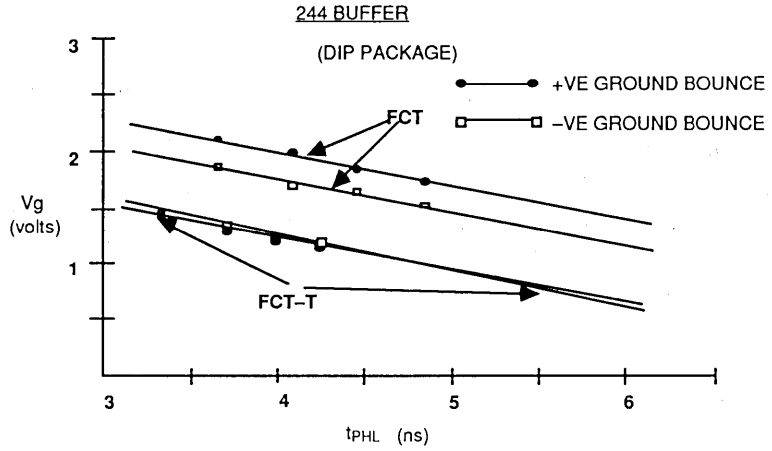

Figure 12. Ground Bounce vs. Speed

The reader is referred to the Application Note entitled "*SIMULTANEOUS SWITCHING NOISE*" for an in–depth discussion on the cause and effects of ground bounce and applications guidelines.

POWER–OFF DISABLE FEATURE

Power–off Disable is a condition where the output of a device maintains high impedance state **during power supply ramping** if the output enable control pins are conditioned to place the appropriate outputs in the high–Z state. This is a desirable feature in backplane applications where it is often necessary to perform "hot" insertion and disinsertion of printed circuit cards for on–line maintenance. It is essential that this activity does not violate data integrity on the backplane. Another application where this feature is useful is in systems with multiple redundancy where one or more redundant cards may be powered off while still plugged into the system. Under these conditions the backplane drivers on these cards should offer very low loading on the backplane.

Most drivers designed for backplane application do not offer this feature. For example, CMOS drivers which use a P–channel output transistor in the pull–up circuit have a parasitic diode to the V_{CC} rail at each such output. Therefore the output node offers a low impedance to the V_{CC} pin when the output voltage exceeds applied V_{CC} by a junction diode drop. This feature precludes use of such devices in applications which require power–off or power up/down disable capability.

Certain members of the FCT–T family (such as the 646/648T, 651/652T Bidirectional Register/Transceivers, FCT52/53T bidirectional registers, 620/621/622/623T backplane transceivers) offer the power off/up/down disable capability. When the outputs of these devices are conditioned to be in the High Impedance state, all 3–state outputs will offer high impedance independent of power supply voltage (excluding negative V_{CC} with respect to GND). The Power Off Disable capability is shown in the DC Characteristics table in the form of a leakage current of 100µA max. at V_{CC} = 0 volts and V_{OUT} = 4.5 volts.

SUMMARY

The FCT–T family of logic products is introduced in an effort to alleviate some of the simultaneous switching noise problems while maintaining compatibility with the industry–standard FCT family as well as with other TTL–compatible logic families. A variety of speed grades and packaging alternatives are offered to help design an optimum system in terms of speed, cost, performance and board space.

Integrated Device Technology, Inc.

SHARED RAM AND DRAM ADDRESS MULTIPLEXER APPLICATION

LOGIC TECHNICAL BULLETIN IDT49FCT804

SHARED RAM APPLICATION

128K x 8 Shared RAM

This application illustrates the use of IDT49FCT804 Bus Multiplexer in a shared memory application. In this example, two processors share a 128Kbyte memory bank. A pair of IDT49FCT804 multiplexers are used for address selection. The address buses from the two processors are connected to A and C ports,respectively. The B port serves as the memory address bus. With all Latch Enable and Output Enable signals asserted, address from A or C ports is routed to B port under the control of S0 which receives its input from an external arbiter/decoder (S1 = 0 and D_{AB} = D_{CB} = 1).

Two more IDT49FCT804 multiplexers route data between the processor data buses connected to A and C ports and the memory data bus connected to the B port. Again, address bus selection is under the control of input S0. Inputs D_{AB} and D_{CB} provide direction control for READ and WRITE operations. The RAM $\overline{OE}$ signal is asserted during the READ operation.

An external arbiter/decoder performs arbitration between two processor requests and provides chip select and write enable signals for the memory array.

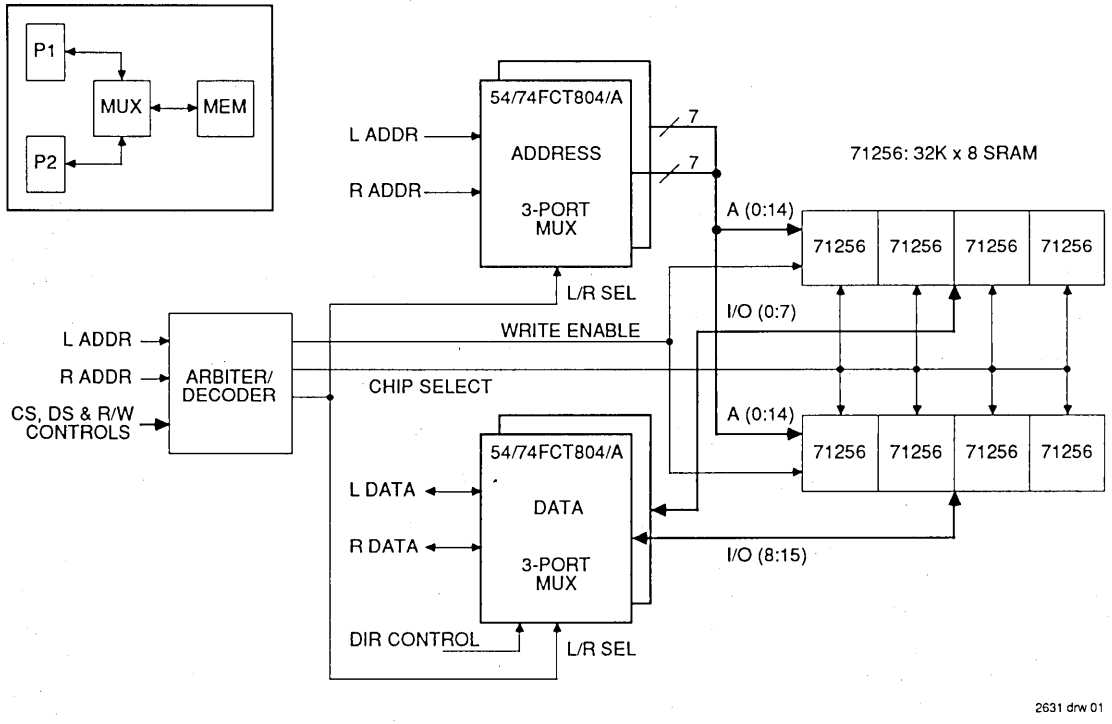

Figure 1. 128K x 8 Shared RAM

DRAM ADDRESS MULTIPLEXER APPLICATION

This application illustrates the use of IDT49FCT804 Bus Multiplexer for row and column addressing in a large DRAM array. In this example, the full 10-bit capability of the Bus Multiplexer is used to address a 1 MBit DRAM array. The row address lines are connected to the A port and the column address lines are connected to the C port. All address signals are latched simultaneously in the A and C port input latches. Under the control of path selection input S0 (S1 = LOW), the row and column addresses are sent sequentially to the DRAM array.

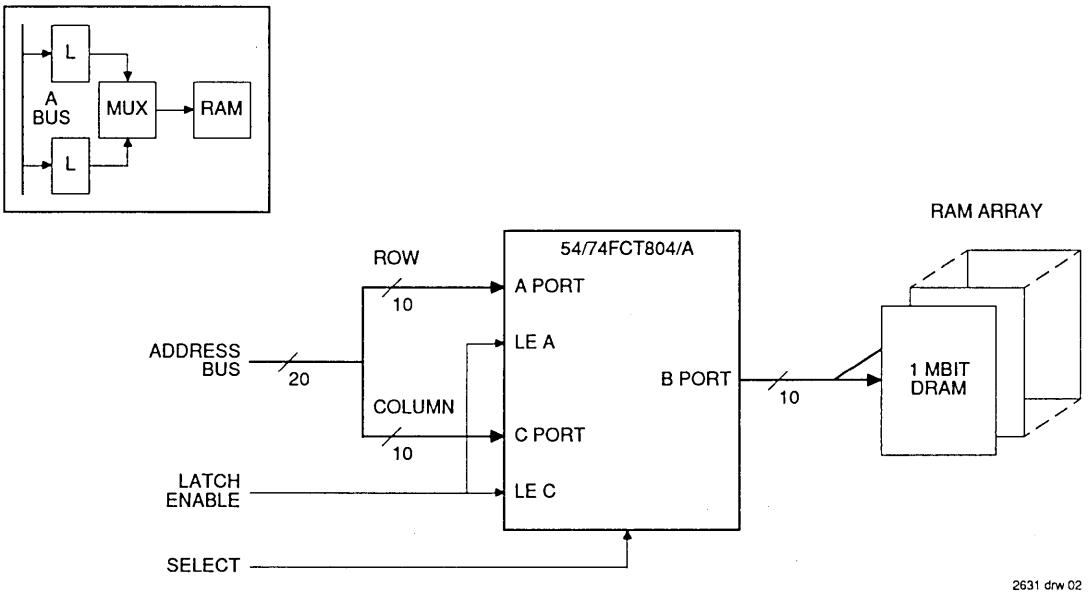

Figure 2. DRAM Address Multiplexer Application

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Integrated Device Technology, Inc.

PREVENTING DECODE GLITCHES

TB-LOGIC
001-A
IDT74FCT138/139

By Suren Kodical

This bulletin describes the timing considerations for avoiding spurious output glitches in FCT138 and 139 decoders.

When these decoders are used in microprocessor-based systems to generate clock or latch enable signals, spurious decoding glitches are likely to cause system errors. Even though the input signals to the decoders may be clean, differences in the propagation delays in the combinatorial paths can cause unwanted output transitions under certain conditions. This is illustrated below by using an FCT138 decoder as an example:

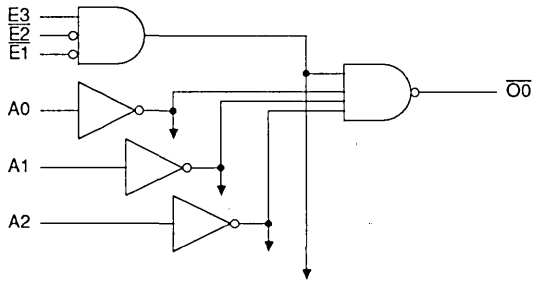

Figure 3. Section of Decoder

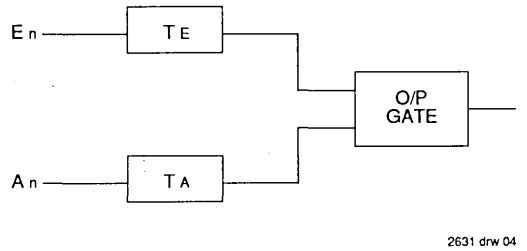

Figure 4. Signal Delays

When the enable lines are asserted, the decoded output corresponding to the appropriate weighted binary inputs will be LOW. When the enable lines are deasserted, the outputs may respond to logic level changes at An inputs if the propagation delay TA is shorter than delay TE through the enable path. This is illustrated in the timing diagram.

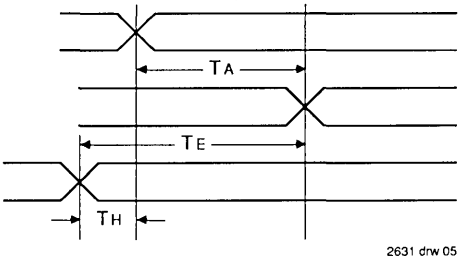

Figure 5. Timing Diagram

To prevent spurious transitions at the decoder outputs, it is necessary to keep the address lines stable for at least TE - TA. This is designated in the timing diagram by Th.

Characterization data on the IDT54/74FCT138 shows that Th = 1ns can be used as a guideline for design. The same number also applies to FCT139. Note, however, that this is not a testable parameter on automated test equipment.

By Suren Kodical

When devices such as the FCT374 (Octal Register) are used as Pipeline Registers (as shown in Figure 1), two sets of AC parameters govern performance boundaries:

1. t_{PD} (max.) from clock to output + t_{SU} determines the maximum frequency of operation.
2. The timing difference between t_{PD} (min.) from clock to output and t_H from data to clock determines the amount of margin for successful pipelining.

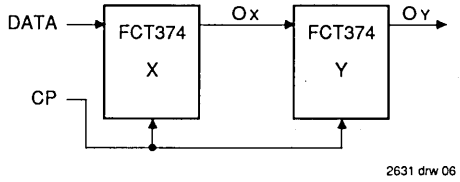

Figure 1.

In the case of high-speed registers, the maximum frequency limit far exceeds most design requirements. Therefore, condition #1 described above is generally not an issue. However, the high-speed switching and data transfer can cause problems if the minimum delay from clock to output approaches the positive t_H in magnitude. This situation is described by means of Figures 2 and 3, below.

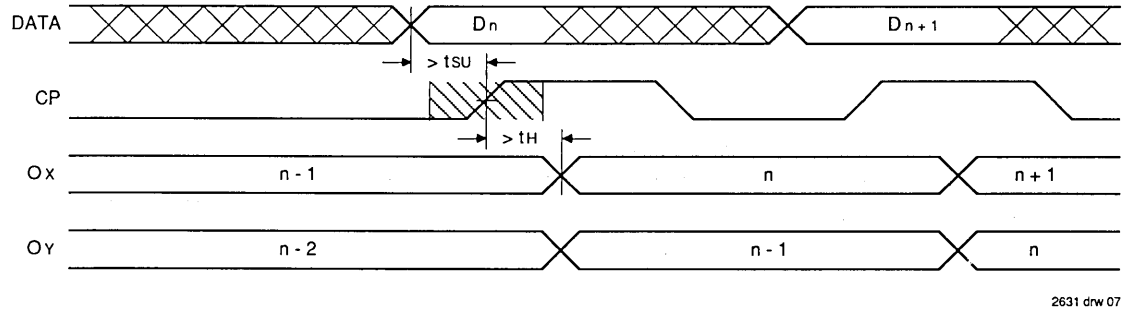

Figure 2.

In Figure 2, the propagation delay from CP to Ox exceeds the hold time t_H for register X. Therefore, for each positive transition of the clock, data at the input of register X is transferred to output Ox and previous data at Ox is transferred to output OY of register Y. The difference between t_{PD} from CP to Ox and the hold time t_H is the safety margin for successful pipelining.

Figure 3 shows the result of loss of timing margin. In this illustration, the clock to output delay of the high-speed register X is less than the required hold time for register Y under given conditions. As a result, on the positive transition of the clock, register Y will transfer new data at the input of the pipeline instead of the previous data at Ox.

7

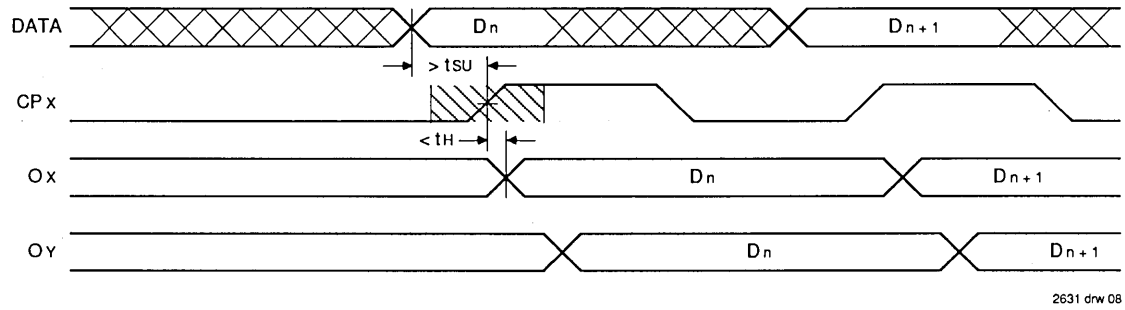

Figure 3.

System designers rely on the published switching characteristics for a product to determine the worst-case timing margin. Often this can lead to erroneous conclusions. This is because both the propagation delay (from clock to output) and the hold time (data to clock) generally have a positive temperature coefficient. As a result, the *real* timing margin may be better than that implied by the data sheet parameters. This is illustrated by the specifications for the FCT374 shown in Figure 4 and the actual timing margin based on characterization data shown in Figure 5.

	FCT374		FCT374A		
Para.	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{PLH} t_{PHL} CP to O_n	2.0	10.0	2.0	6.5	ns
t_H D_n to CP	2.0	—	1.5	—	ns

2631 tbl 01

Figure 4.

This table shows that the worst-case margin, t_{PD} (min.) - t_H, is 0.5ns for the FCT374A and 0ns for the FCT374. In reality, the margin under worst-case conditions is about 2.5ns based on characterization data. The effect of temperature on the two parameters is shown in Figure 5. It is clear that the worst-case condition for t_{PD} (min.) is cold temperature, but the worst-case condition for t_H is hot temperature. Therefore, the actual worst-case timing margin is greater than that implied by the data sheet limits.

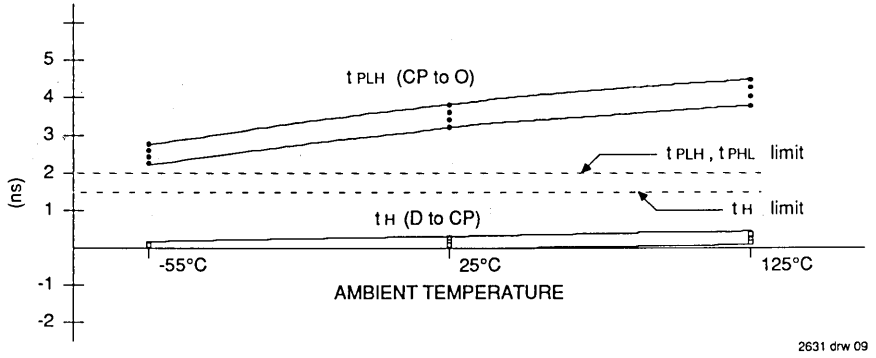

Figure 5. FCT374A/574A Data

SUMMARY

When using high-speed registers such as IDT's 54/74FCT374/A for pipelining applications, the margin between t_{PD} (min.) and t_H becomes the limiting factor. Calculations based on data sheet limits give worse numbers than actual margins. To utilize the performance of such high-speed registers, the system designer must take the effect of temperature on the critical parameters into account.

Integrated Device Technology, Inc.

FUNCTIONALITY

TB-LOGIC
013-A
IDT74FCT833

By Kelly Maas

This Technical Bulletin addresses possible confusion regarding the functioning of the $\overline{ERR}$ output pin on the FCT833.

The FCT833 is a bidirectional transceiver with parity generate and check. When in the transmit mode (Port R to Port T), a parity tree is used to generate a parity (9th) bit. When in the receive mode (Port T to Port R), the same parity tree is used to check the parity of the input. The result of this parity check can be clocked into the error register using the CLK pin. This is shown in the Block Diagram in the IDT54/74FCT833 data sheet.

The Error Flag Output Truth Table and the Function Table (found in the IDT54/74FCT833 data sheet) show the value of $\overline{ERR}$ only for certain combinations of $\overline{OER}$ and $\overline{OET}$. But the output of the parity tree is always registered when the CLK pin is strobed.

This means that if the FCT833 is used both for transmitting and receiving data, with a free running clock, the $\overline{ERR}$ pin reflects parity error status only when in the receive mode. To ensure that $\overline{ERR}$ goes low only on a parity error, the clock input should be disabled whenever the FCT833 is not in the receive mode.

Shown below is a clarification to the FCT833 Function Table. The changes indicate how the $\overline{ERR}$ output pin functions in the transmit, error check and Hi-Z modes when the $\overline{CLR}$ pin is held high and CLK is strobed.

When $\overline{CLR}$ is held high and CLK is held steady (logic high or low), $\overline{ERR}$ will not change. This is true, regardless of the mode. Note also that the footnote below the Error Flag Output Truth Table should be ignored.

IDT54/74FCT833 NON-INVERTING REGISTER OPTION

Inputs						Outputs				
$\overline{OE_T}$	$\overline{OE_R}$	$\overline{CLR}$	CLK	R_I (Σ of H's)	T_I incl Parity (Σ of H's)	R_I	T_I	Parity	$\overline{ERR}$	Function
L	H	H	↑	(Odd)					H	Transmit from R
L	H	H	↑	(Even)					L	Port to T Port.
L	H	H	↑	(Odd)					H	Parity generate.
L	H	H	↑	(Even)					L	
H	L	H	↑		(Odd)				H	Receive from T
H	L	H	↑		(Even)				L	Port to R Port.
H	L	H	↑		(Odd)				H	Parity generate.
H	L	H	↑		(Even)				L	
—	—	L	—						H	Clear error register.
H	H	H	↑	(Odd)					H	Hi-Z.
H	H	H	↑	(Even)					L	
L	L	H	↑	(Odd)					L	Forced error
L	L	H	↑	(Even)					H	checking while
L	L	H	↑	(Odd)					L	transmitting.
L	L	H	↑	(Even)					H	Parity generate.

2631 tbl 02

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