INDEX OF LOGICAL DRAWINGS FOR PAC CONTROL (WGC.07)

SUB	Iss	1	2	3	

Logic Description of PAC Character Data Buffer

The Character Data Buffer (WGC07/3) has very similar "hardware" to the standard Word Data Buffer (WGC07/1). The only changes to the logic drawings are that sheet 2 of WGC07/1 has been replaced by new sheets 2 and 3, the rest being identical except for one wire on sheet 1.

Inwards Transfers

Now consider the case of an R request from a character peripheral after being initiated by a 174 read order. Control Words will be loaded in the usual way by means of steps 1 and 2 and then step 5 which sets the OUT stat A27/2 (Sh.1) to IN, thus producing PANTC+ which sets the BTD (Buffer Transferring Data) stat. PANTC+ also sets the A stat A36/1 (Sh.2) because PANR+ will be +ve.

Since A36/1 (Sh.2) is set then PANGC+ will be -ve and allowing the A line to the peripheral to be activated (see standard interface logic sheets). The second PANTC+ will set the GT stat A29/2 (Sh.2) producing PANGTP+ which will allow a T pulse to be emitted from A33/2 (Sh.1). The second PANTC+ will also allow a PANTINO+ which gates the first character into the buffer. The third PANTC+ will reset the A stat A36/1 (Sh.2) and PANTC+ pulses will be continued to be produced at 1 µS intervals also the buffer will remain selected but no further action occurs until the next R request arrives i.e. PANR+ (Sheet 2).

The second R will set the A stat again thus producing PANGTP+ which allows another T pulse at the next PANTC+ and gates in the second character into the buffer, the A stat A36/1 (Sh.2) being reset again by the third PANTC+.

This procedure is repeated until the fourth character is strobed, in which case the BTD stat (Sh.1) is reset by PANGTP- and PANCH3- and causing PAEOTI- which will eventually lead to step 6. Step 6 writes the word now in the data buffer into the store.

If however the peripheral which was engaged in the inwards transfer terminates part way through a word, then the following sequence would be initiated. Obviously if say the second character had been strobed into the data buffer and then the peripheral had terminated, then nothing further could happen until the B interrupt arising from the terminated condition is interrogated and identified.

Continued..../

Considering when the peripheral on this particular interface is interrogated via the 174 SSQ command then PANESM+ (Sh.2) will be +ve thus setting the C stat A29/3 (Sh.2) (because PANRETD+ (Sh.1) will be -ve

Hence, PANC- (Sh.2) will be -ve and PANGC- will be -ve also, PASIT+ (Sh.3) will be +ve because of the terminated state of the peripheral, therefore the PWT (partial word terminated) stat will be set. PWT stat being set will make the outputs of power inverters A35/1, A35/2, A35/3, A35/4 all positive, thus forcing *74 on the DI lines. PANPWT- is also now -ve thus enabling PANGTP+ to be +ve with alternate PANTC+ pulses via A34/4 (Sh.2).

The remaining character positions in the buffer will be filled with *74s and when CH3- (Sh.1) is -ve on the last character, the BTD stat (Sh.1) will be reset allowing the PWT stat (Sh.3) to be reset and leaving the DI lines free again.

Also at this time PAEOTI- becomes -ve and eventually leads to a step 6 which writes the final word away, including the *74 dummy characters.

Outwards Transfers

On Outward transfers the action of the A stat A36/1 is the same. It allows one T pulse at a time to be sent with each character, PANGDO- now being -ve lets the data in the data buffer to be gated on the DO lines, one character for every R request from the peripheral.

If the peripheral terminates part way through an outward transfer and is then interrogated by a 174 SSQ command, the PWT stat will be set (as mentioned previously for an inwards transfer) and *74s will appear on the DI lines which do not matter, also the unwanted characters will be placed in the DO lines and T pulses occur until the last character is strobed. Note that the peripheral will not respond to these dummy characters because the A stat A36/1 is not set again after the peripheral terminates.

When the BTD stat is reset on the fourth character, the buffer is freed for further use.

Special case when Count Control Word = 1

It is necessary in order to write file marks on 20 Kc/s to send 1 character which must be accompanied by Limit. Normally one would expect 4 characters to be transferred with a CCW = 1.

When a CCW=1 has been loaded in step 2, it is detected by logic on sheet 3. The EL (early limit) stat which is used upside down is set by loading control word 0 (PALCWO-) i.e. step 2 at the end of step 2, clocked by PATDB. There are two ways of resetting the EL stat, one way is by means of A30/4 (Sn.2) which is +ve if the mill test $\neq 0$. If the loaded CCW=1 then PAMT = $\emptyset$- would be -ve and thus A30/4 would be -ve and would not reset the EL stat.

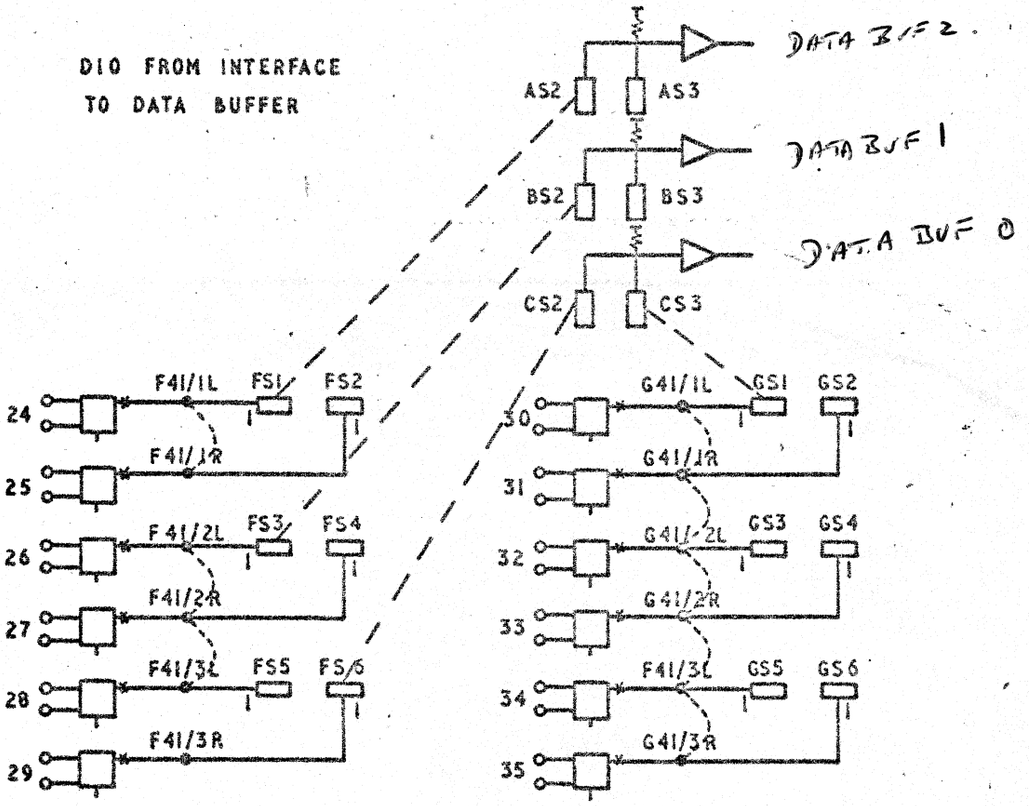
The other way of resetting the EL stat is by A24/6 (Sh.1) which is +ve if an inwards transfer is to be started, i.e. step 5. In summary, the EL stat is set by step 2 and only remains set if an outward transfer is to take place and the loaded CCW=1.

A33/4 (Sh.3) which is collector-orred with PANL+ (Sh.2) will therefore be positive when the A stat (Sh.2) is set, thus sending L with the first character to the peripheral.

Now element A28/2 which produces PAINHT+ (Sh.3), is also +ve when the EL stat is set, and returns -ve when PA DBS- (Sh.1) goes +ve which occurs at the end of step 4. PAINHT+ is connected to A30/2 mix which inhibits T pulses until the end of step 4, by which time the test on CCW=1 will have been effected.

The buffer will be freed as explained previously by the action of sending a SSQ command after the peripheral terminates.

J.N. Trainor
19th June 1968



	S.I. Nº	26 WAY SKt Nº	LINK BOARD CONNECTIONS						
A	24	FS1	1L	4L	7L	10L	13L	16L	BOX F
	25	FS2	1R	4R	7R	10R	13R	16R	
B	26	FS3	2L	5L	8L	11L	14L	17L	
	27	FS4	2R	5R	8R	11R	14R	17R	
	28	FS5	3L	6L	9L	12L	15L	18L	
	29	FS6	3R	6R	9R	12R	15R	18R	
C	30	GS1	1L	4L	7L	10L	13L	16L	BOX G
	31	GS2	1R	4R	7R	10R	13R	16R	
	32	GS3	2L	5L	8L	11L	14L	17L	
	33	GS4	2R	5R	8R	11R	14R	17R	
	34	GS5	3L	6L	9L	12L	15L	18L	
	35	GS6	3R	6R	9R	12R	15R	18R	

CONNECTING FROM A STANDARD INTERFACE TO A DATA BUFFER

PLUG A LINKING CABLE BETWEEN THE SOCKET ON THE DATA BUFFER AND THE 26 WAY SOCKET ASSOCIATED WITH THE STANDARD INTERFACE. ADD LINKS ON THE LINK BOARDS TO CONNECT THIS DATA BUFFER TO FURTHER STANDARD INTERFACES. THE DOTTED LINES ABOVE SHOW THE CONNECTIONS NECESSARY TO CONNECT DATA BUFFER A TO 24 AND 25, B TO 26, 27 AND 28 AND C TO 29, 30, 31, 32, 33, 34 AND 35.

SOCKET AND LINK BOARD CONNECTIONS

DATA BUFFER ALLOCATION

NAME OF SIGNAL	26 WAY SOCKET PINS	LINK BOARD LOCATION	LINK BOARD PINS FOR DEVICES ON BOX F						LINK BOARD PINS FOR DEVICES ON BOX G					
			24	25	26	27	28	29	30	31	32	33	34	35
DIØ +	1	41	1L	1R	2L	2R	3L	3R	1L	1R	2L	2R	3L	3R
DI1 +	2		4L	4R	5L	5R	6L	6R	4L	4R	5L	5R	6L	6R
DI2 +	3		7L	7R	8L	8R	9L	9R	7L	7R	8L	8R	9L	9R
DI3 +	4		10L	10R	11L	11R	12L	12R	10L	10R	11L	11R	12L	12R
DI4 +	5		13L	13R	14L	14R	15L	15R	13L	13R	14L	14R	15L	15R
DI5 +	6		16L	16R	17L	17R	18L	18R	16L	16R	17L	17R	18L	18R
DOØ +	7	42	1L	1R	2L	2R	3L	3R	1L	1R	2L	2R	3L	3R
DO1 +	8		4L	4R	5L	5R	6L	6R	4L	4R	5L	5R	6L	6R
DO2 +	9		7L	7R	8L	8R	9L	9R	7L	7R	8L	8R	9L	9R
DO3 +	10		10L	10R	11L	11R	12L	12R	10L	10R	11L	11R	12L	12R
DO4 +	11		13L	13R	14L	14R	15L	15R	13L	13R	14L	14R	15L	15R
DO5 +	12		16L	16R	17L	17R	18L	18R	16L	16R	17L	17R	18L	18R
T +	13	43	1L	1R	2L	2R	3L	3R	1L	1R	2L	2R	3L	3R
No +	14		4L	4R	5L	5R	6L	6R	4L	4R	5L	5R	6L	6R
L +	15		7L	7R	8L	8R	9L	9R	7L	7R	8L	8R	9L	9R
EOTI −	16		10L	10R	11L	11R	12L	12R	10L	10R	11L	11R	12L	12R
EOTO −	17		13L	13R	14L	14R	15L	15R	13L	13R	14L	14R	15L	15R
GC −	18		16L	16R	17L	17R	18L	18R	16L	16R	17L	17R	18L	18R
GC +	19	44	1L	1R	2L	2R	3L	3R	1L	1R	2L	2R	3L	3R
ESM +	20		4L	4R	5L	5R	6L	6R	4L	4R	5L	5R	6L	6R
RSM +	21		7L	7R	8L	8R	9L	9R	7L	7R	8L	8R	9L	9R
−	−		10L	10R	11L	11R	12L	12R	10L	10R	11L	11R	12L	12R
−	−		13L	13R	14L	14R	15L	15R	13L	13R	14L	14R	15L	15R
AM +	24		16L	16R	17L	17R	18L	18R	16L	16R	17L	17R	18L	18R

TO CONNECT A PERIPHERAL OR A GROUP OF PERIPHERALS TO A DATA BUFFER, LINK THE CORRESPONDING PINS ON THE LINK BOARDS FOR EACH SIGNAL, AND CONNECT ANY SOCKET INCLUDED IN THE GROUP TO ANY SOCKET ON THE DATA BUFFER WITH A LINKING CABLE (26 WAY).

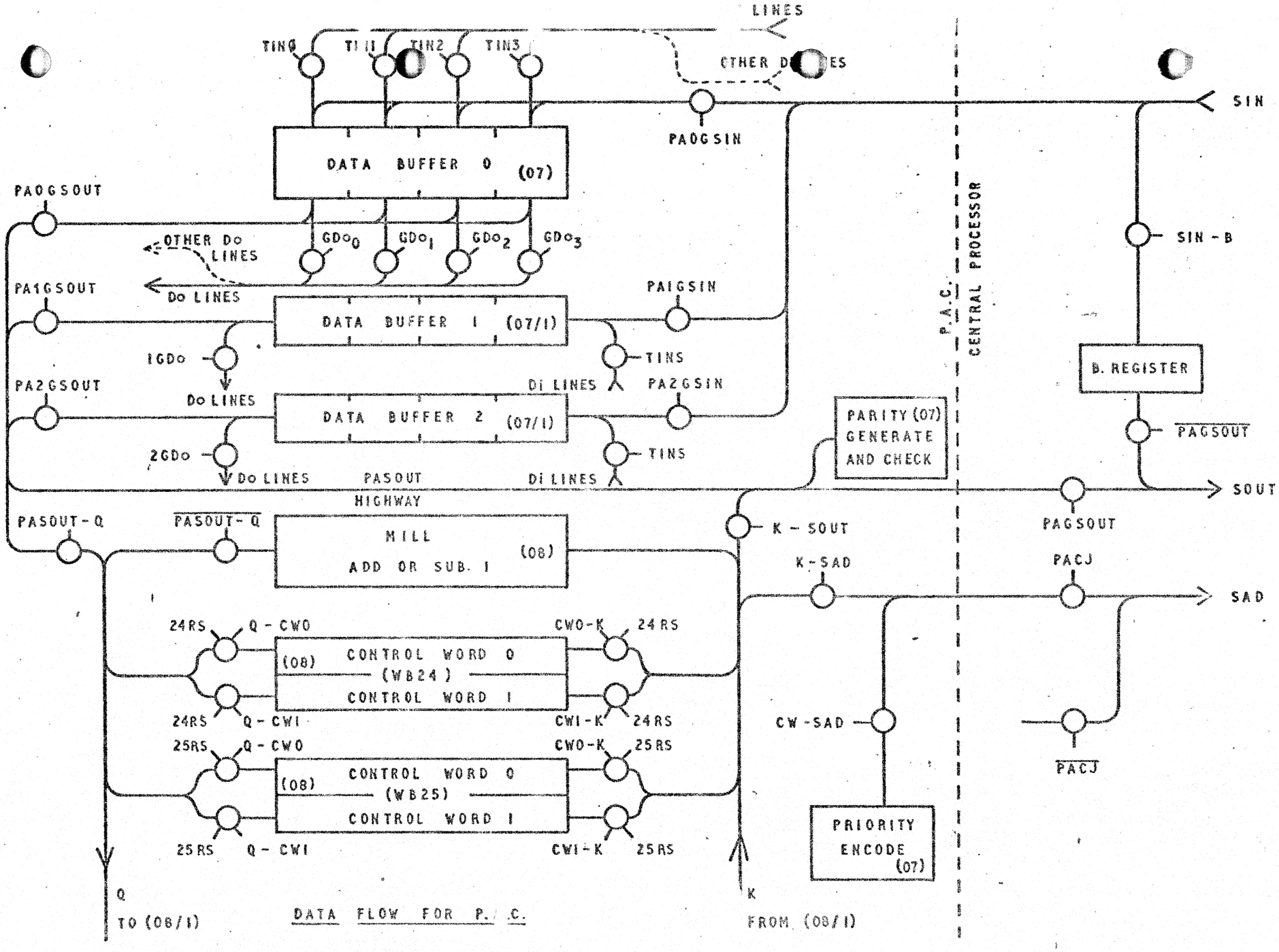
PERIPHERAL DEVICE No.	S. I. 26 WAY SOCKETS.
24	FS1
25	FS2
26	FS3
27	FS4
28	FS5
29	FS6
30	GS1
31	GS2
32	GS3
33	GS4
34	GS5
35	GS6

DATA BUFFER	BOX WGCØ7	26WAY SOCKETS DATA BUFFER
2	A	AS2 - AS3
1	B	BS2 BS3
Ø	C	CS2 CS3

NOTE:- SOCKETS ON DATA BUFFERS ARE COMMON.

W.G.C.Ø7/GEN 2.

ISS 1



DATA FLOW FOR P.A.C.

Fault Finding on P.A.C.

The majority of the logic on P.A.C.can be tested with the use of a few "status symbols" i.e. jumper leads,and a little know how,without utilising complicated devices called peripherals.

A P.A.C. channel will operate when its R line receiver is connected with a "status symbol" to 0V.

To continually cycle steps 1 & 2 earth the reset side of a CWL stat in WGC 08.

To continually cycle steps 3 & 4 or steps 5 & 6 allow P.A.C. to load then earth E26/1 & E25/3 in WGC 07. This stops the address & count being updated but allows the transfer to take place.If the BTD stat in a data buffer has its reset side earthed the transfer will not take place.

To continually cycle steps 1,2,7 & 8 link D7/7 to D10/3 in WGC 08.

To continually cycle step 8 earth the set side of a CT stat in WGC 08.

To cause a Data Buffer to continuously send or receive data operate INH PAC switch and PAC RUN switch and earth the set side of its BTD stat.

To continually cycle steps 9 & 10 set CWL & CWO bit 19 and earth the set side of the CT stat on the required channel.

If the PAC timing logic locks up because it does not receive end of read or end of cycle or both,the contents of the control word buffers can be shown on the K highway lights by operating the CFRZ switch,earthing the set side of the CWL stat of the relevant channel & then pushing the 'GO' button until the steps for that channel show the contents of the control word buffers which have both been incremented by one from the point of failure. P.A.C. can be made to operate with the mains ticker (timer) when PACRUN and TICKER switches are operated.

A fault finding program has been written called PACB to locate and display faults in the PAC data flow and to test the PAC timing logic. When this program runs successfully on each channel,it should then be used to test time sharing if more than one data buffer is fitted.One channel per data buffer can be operated simultaneously.
To make one data buffer timeshare between N channels,earth R of lowest priority peripheral on that buffer and connect its A line to the N - 1's R line. Then connect the N-1's A line to the N-2's R line .

A useful test of the control logic and the core store is to transfer the entire contents of the core store outwards through PAC using a status symbol in an R line receiver and the outward and control word recharge style bits in control word 0,while FLIT is running.

Useful scope trigger points for all the above tests are STEP2+ (E31/1), STEP4+ (E31/6), STEP10+ (E29/3) when examining the microprogram & timing logic, SBUSY(D28/1) when checking core store timing,PAC (D31/1) when PAC & CPU are time sharing the core store,BTD (A or C 29) in a data buffer to see data being transferred to or from the data buffer,A (24 to 35) when watching data go through a channel.When a real peripheral is transferring data CWL stat in WGC 08 provides a trigger at the beggining of each transfer.

The standard interface for each peripheral can be tested by sending a selection of commands using the handkeys i.e. 100 order followed by 174 order.With the peripheral on line send *20 (Q status)the response will be bits 5,4 & 3 at least and can be seen on the CPU Q highway (fanned to 4 characters)on the beat before the T stat sets on the 174 order or in the A register after the 174 order. Similarly bits 2 & 0 can be tested by sending the peripheral its normal read or write command. Bit 1 can be tested if the peripheral HOLD button is pushed and *24 is sent.

The P.A.C. ONLY switch can be usefully employed if one needs to check what happens after a peripheral has transferred some data e.g. to see if the peripheral terminates properly or to examine the control words. Operating the PACONLY switch can be done in complete safety with normal mode or executive mode programs. P.A.C. will take and keep control of the store when a data transfer is started causing the CPU to stop. Switch the CPU off 'RUN' and go off PACONLY. The CPU can then proceed.

SUB	ISS		
ACW	1566		
ACD			

SETTING UP TIMING OF PAC

WGC 07

a) Set 4.5 volt bias on D22 (Monitor point 2) using an AVO.

b) Set D21/2 to produce a pulse 450 n/sec wide to mask the selection of a STEP(Pot 9)

c) Set D21/1 to produce a pulse (i) 150 n/sec wide for no 'Step' (Pot 2)
(ii) 450 n/sec wide for 'Sout-Q' (Pot 3)
(iii) 700 n/sec wide for 'Sub' (Pot 4)
(iv) 700 n/sec wide for 'Add) (Pot 5)
(v) 630 n/sec wide for 'Sub'& 'Variable' (Pot 8)
(Can be set with 1 word recharge outward transfer, on PAC ONLY Trigger Step 10+)

d) Set D37/2 to produce a cycle initiate 150 n/sec wide.
Monitor D26/6- (Approx Tap 40)

e) Set D25/1 so that PASDD+ is true until 50 n/sec after PABUSYB+ sets when loading control word 1 (i.e. Step 9). Should be set with a 1 word outwards transfer (Approx. Tap 6)

f) Set D34/2 so that SNR+ (D29/2) goes negative 650 nsec or 1.8 usec after SCI (D26/8).

g) Set D25/2 to Tap 25 except if one or more 650 n/sec stores are connected when this delay allows the parity to be calculated for some time before a write cycle is initiated, such that SCI+ (D26/8) occurs no earlier than 250 n/sec after PATSELD+ (D27/1) during Step 6 (Approx Tap 33)

h) Set D34/1 to allow the 'Enable' logic in WGC 02 to become steady before a cycle initiate is given by WGC 01 after PAC relinquishes the store (Approx Tap 6)
(Set with a 1 word outwards recharge transfer, transferring data to the upper store and with the C.P.U. doing an 04.5 function on "ORDER")

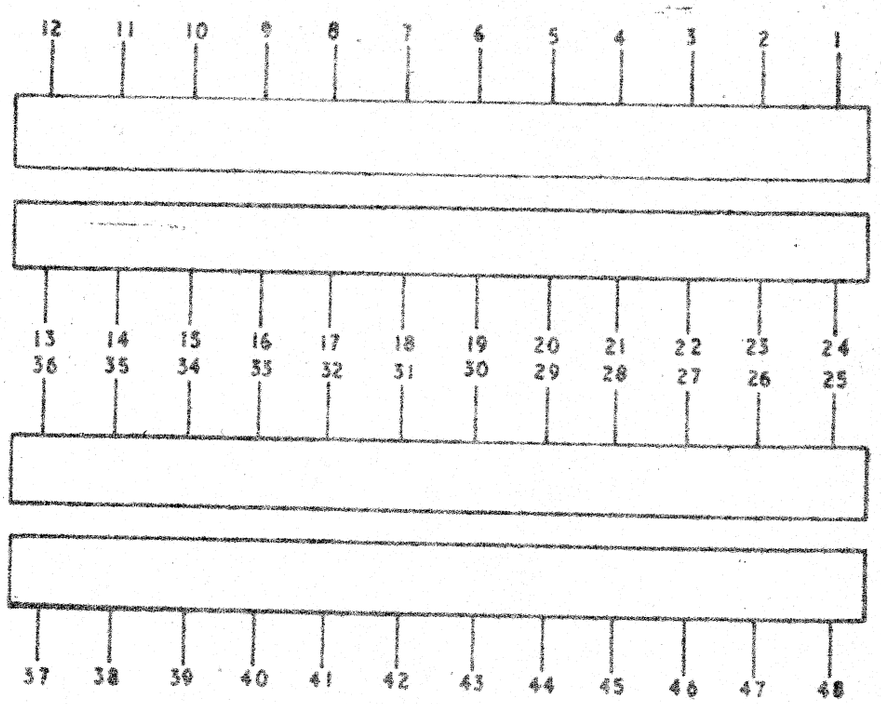
j) Set D37/1 to allow the parity fail stat to be strobed at least 150 n/sec after its input (D20/6) is steady when reading from store (Approx Tap 24)

WGC 07/1 & WGC 07 Box 'C'

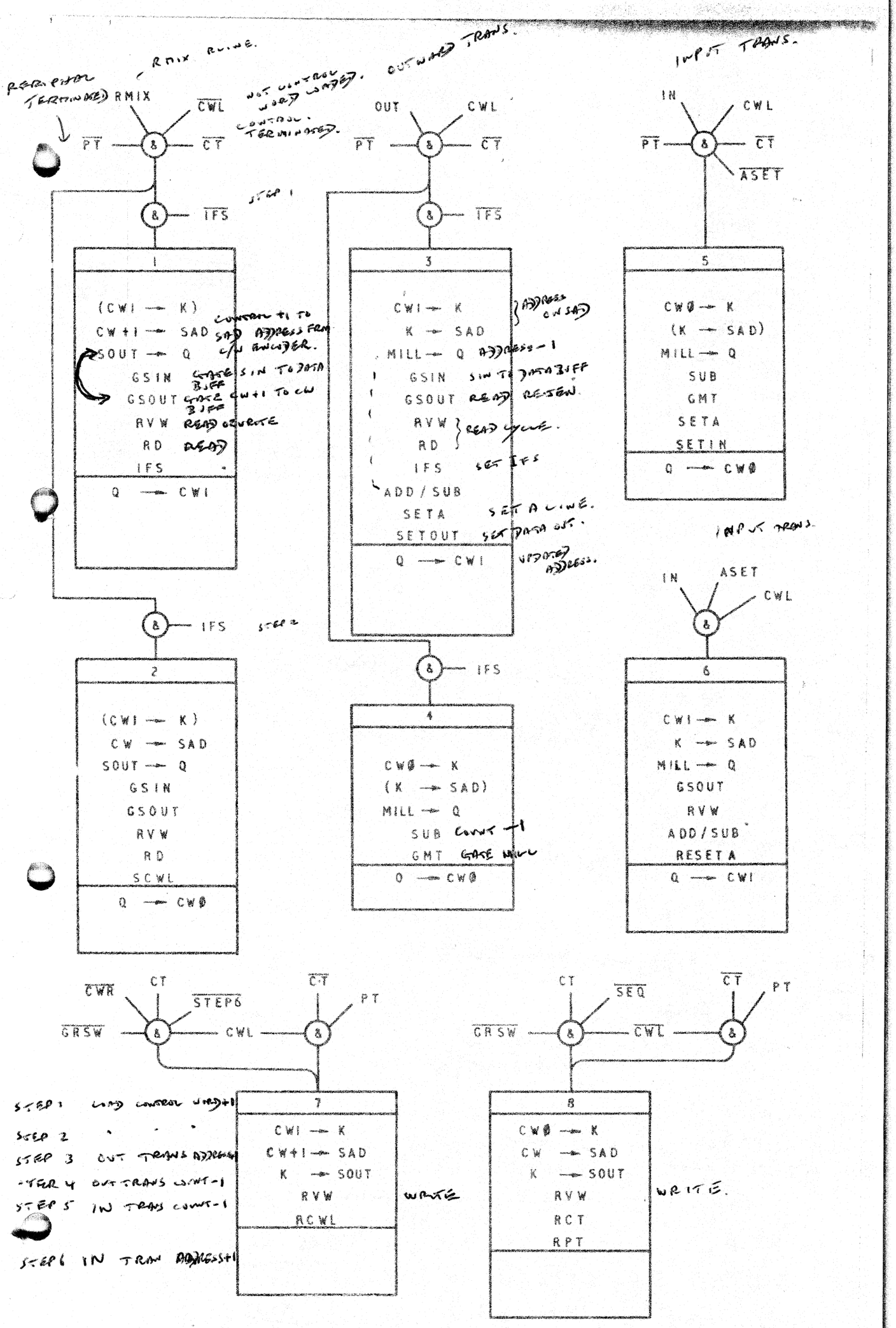
a) Set D32/1 to produce clock pulses from 23/1 1 u/sec apart minimum(Approx Tap 24)

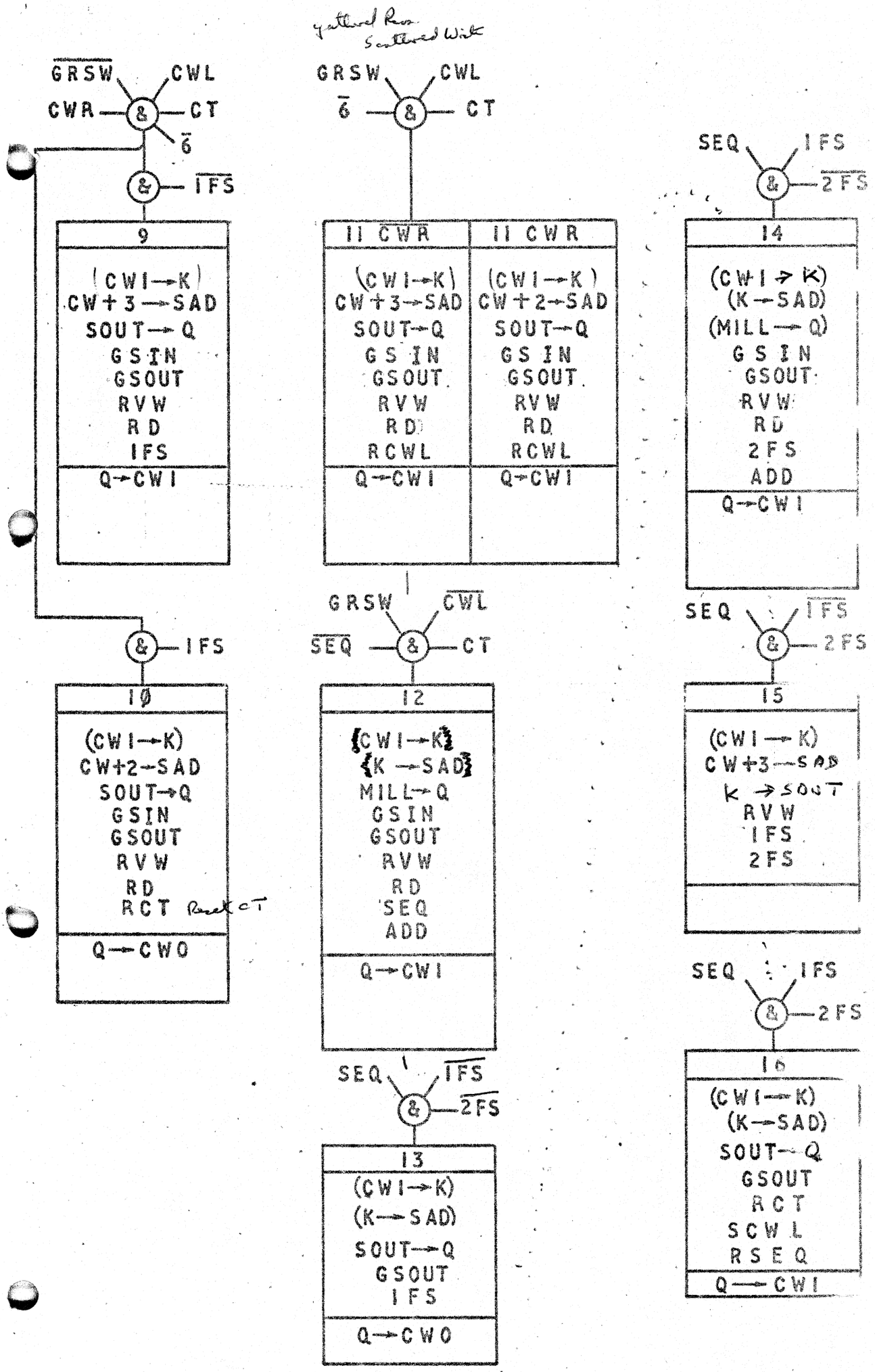
b) Set D32/2 so that its output goes negative 0-50 ns after 31/6 goes negative (Approx TAP 42)

Numbering of Delay Line Taps



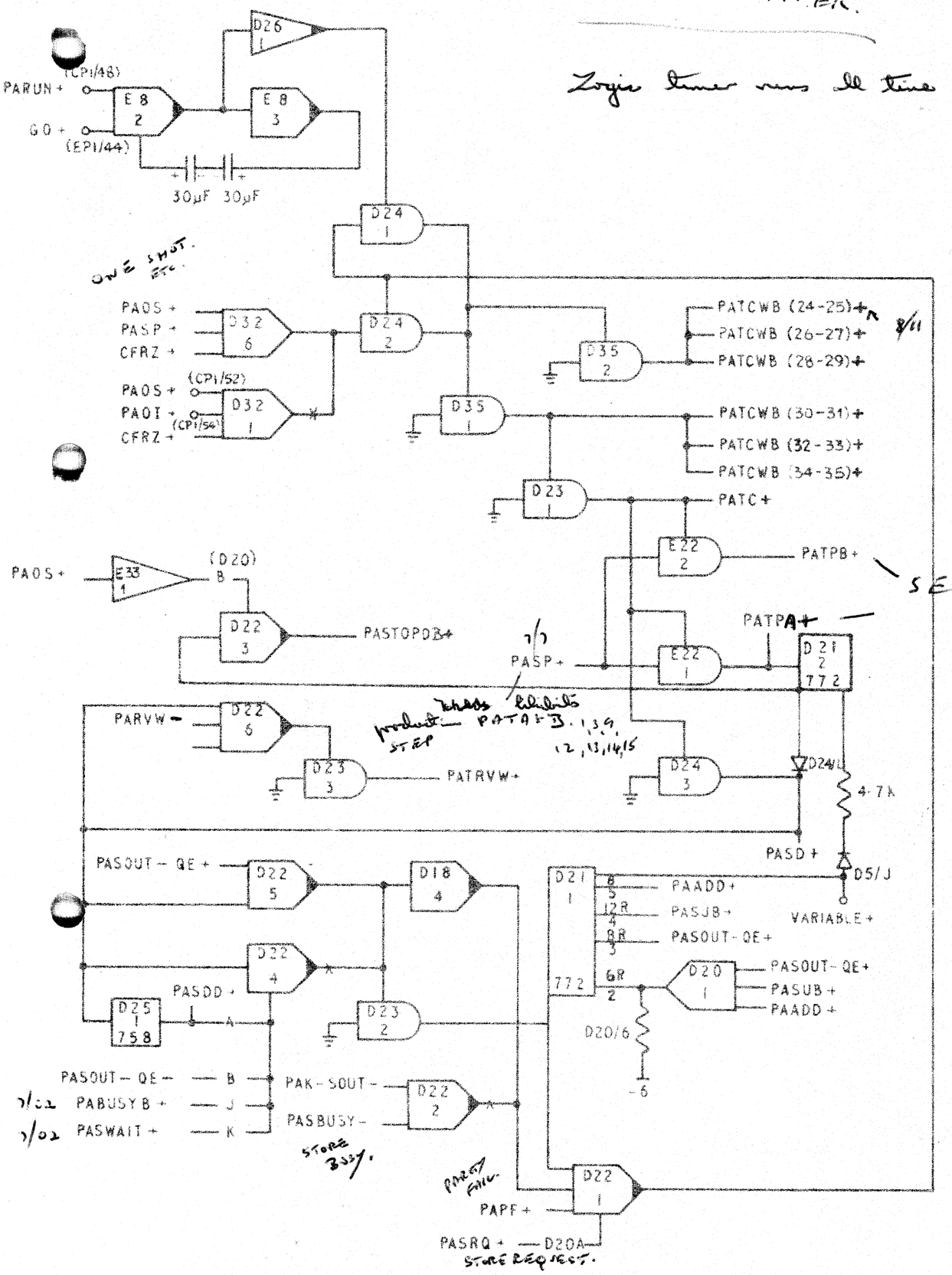
SUB	ISS	1	2	3	
ACW	0912	0970	1517	1546	
ACD	-	-	-	-	
DATE	29/12/67	4/3/68	30/6/68	29/10/68	


RMIX RUNS.
INPUT TRANS.
REMOTE TERMINATED
RMIX
CWL
PT
CT
NOT CONTROL WORD WANTED.
CONTROL TERMINATED.
OUT
CWL
PT
CT
IN
CWL
PT
CT
ASET
STEP 1
IFS
1
(CWI → K)
CW+1 → SAD
SOUT → Q
GSIN GATE SIN TO DATA BUFF
GSOUT GATE BUFF CW+1 TO CW
RVW READ OR WRITE
RD READ
IFS
Q → CWI
CONTENTS +1 TO SAD ADDRESS FROM C/W ANSWER.
3
CWI → K
K → SAD
MILL → Q ADDRESS + 1
GSIN SIN TO DATA BUFF
GSOUT READ REGEN.
RVW
RD
READ CYCLE.
IFS SET IFS
ADD / SUB
SETA SET A LINE.
SETOUT SET DATA OUT.
Q → CWI
ADDRESS ON SAD
UPDATED ADDRESS.
5
CW0 → K
(K → SAD)
MILL → Q
SUB
GMT
SETA
SETIN
Q → CW0
INPUT TRANS.
IN
ASET
CWL
6
CWI → K
K → SAD
MILL → Q
GSOUT
RVW
ADD/SUB
RESETA
Q → CWI
IFS
STEP 2
2
(CWI → K)
CW → SAD
SOUT → Q
GSIN
GSOUT
RVW
RD
SCWL
Q → CW0
4
CW0 → K
(K → SAD)
MILL → Q
SUB COUNT +1
GMT GATE MILL
Q → CW0
CWR
CT
STEP6
GRSW
CWL
CT
PT
CT
SEQ
GRSW
CWL
CT
PT
STEP 1 LOAD CONTROL WORD+1
STEP 2 " " "
STEP 3 OUT TRANS ADDRESS
STEP 4 OUT TRANS COUNT-1
STEP 5 IN TRANS COUNT-1
STEP 6 IN TRAN ADDRESS+1
7
CWI → K
CW+1 → SAD
K → SOUT
RVW
RCWL
WRITE
8
CW0 → K
CW → SAD
K → SOUT
RVW
RCT
RPT
WRITE.


Scattered Row
Scattered Write
GRSW
CWL
CWR
CT
6
IFS
9
(CWI→K)
CW+3→SAD
SOUT→Q
GSIN
GSOUT
RVW
RD
IFS
Q→CWI
10
(CWI→K)
CW+2→SAD
SOUT→Q
GSIN
GSOUT
RVW
RD
RCT
Read CT
Q→CWO
11 CWR
11 CWR
(CWI→K)
CW+3→SAD
CW+2→SAD
SOUT→Q
GSIN
GSOUT
RVW
RD
RCWL
Q→CWI
SEQ
12
(CWI→K)
(K→SAD)
MILL→Q
GSIN
GSOUT
RVW
RD
SEQ
ADD
Q→CWI
13
(CWI→K)
(K→SAD)
SOUT→Q
GSOUT
IFS
Q→CWO
2FS
14
(CWI→K)
(K→SAD)
(MILL→Q)
GSIN
GSOUT
RVW
RD
2FS
ADD
Q→CWI
15
(CWI→K)
CW+3→SAD
K→SOUT
RVW
IFS
2FS
16
(CWI→K)
(K→SAD)
SOUT→Q
GSOUT
RCT
SCWL
RSEQ
Q→CWI

LOGIC TIMER.

Logic timer runs all time after PARUN.



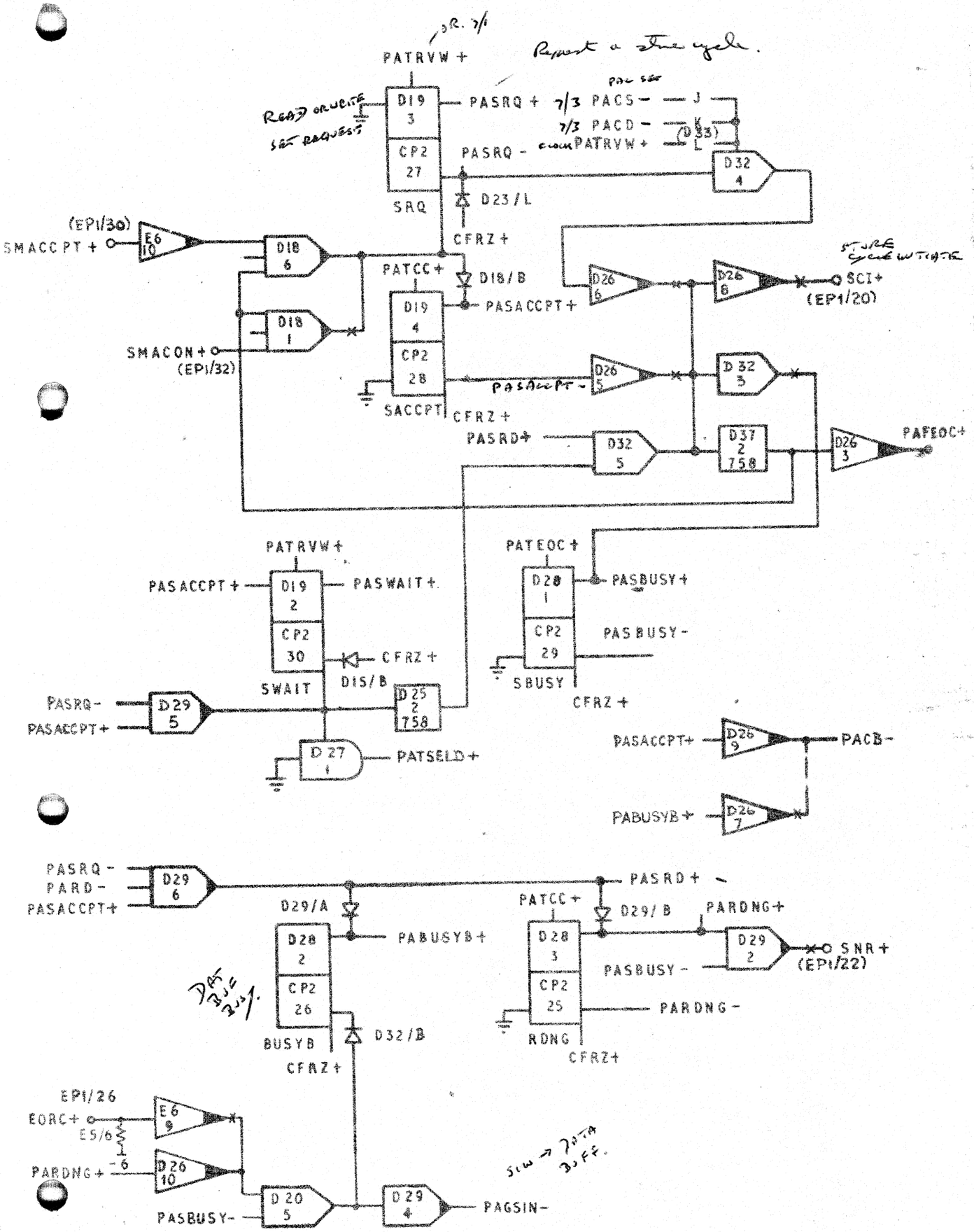
D 22/5 Must wait if SOUT → Q

D 22/4 Must wait if BUSY B to SOUT → Q. or SWAIT.

D 22/2 wait if K → SOUT & SBUSY.

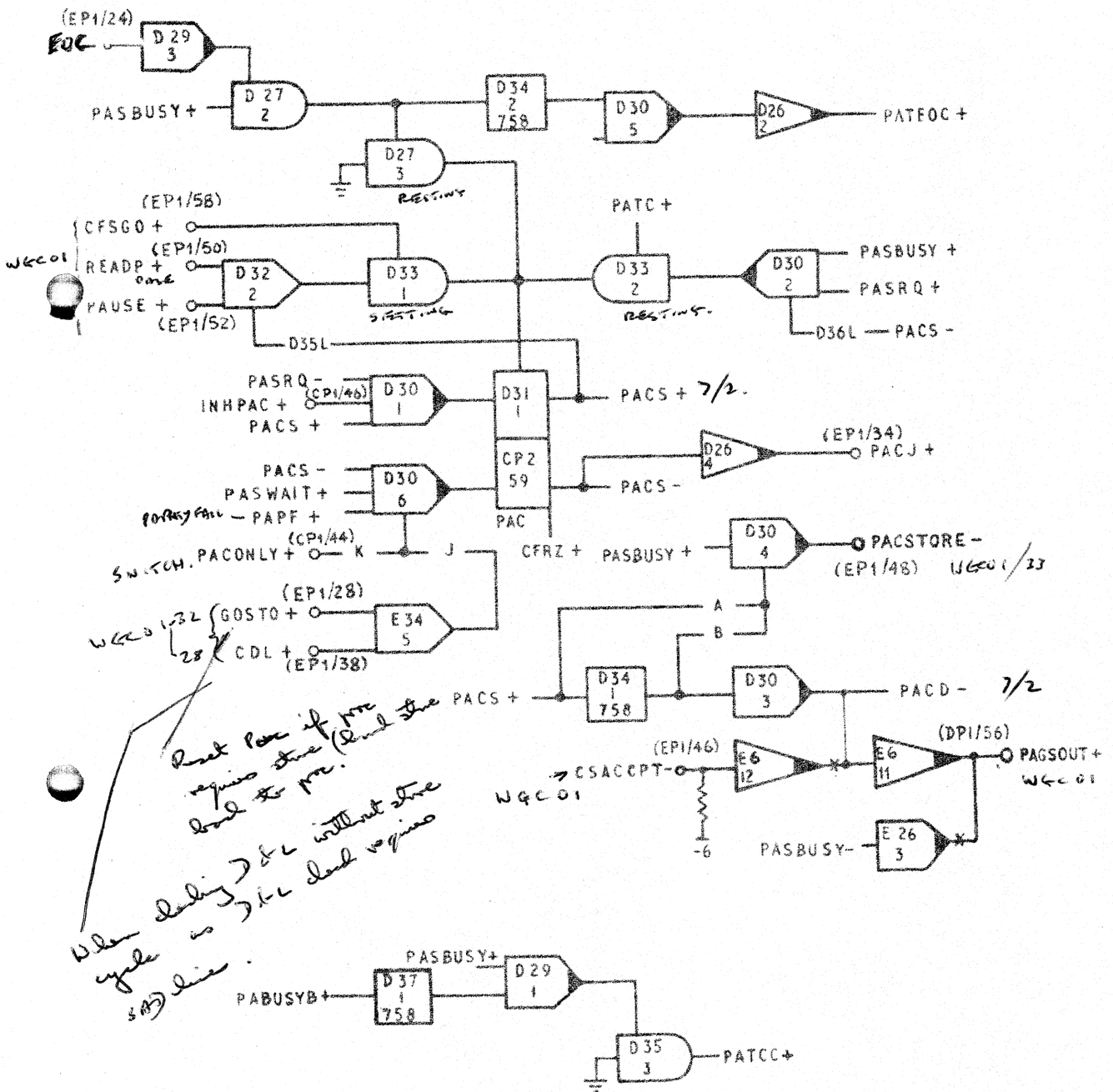
D 22/1 wait if PASRQ. ERQ set. somebody else using store.

STORE TIMER CONTROL.

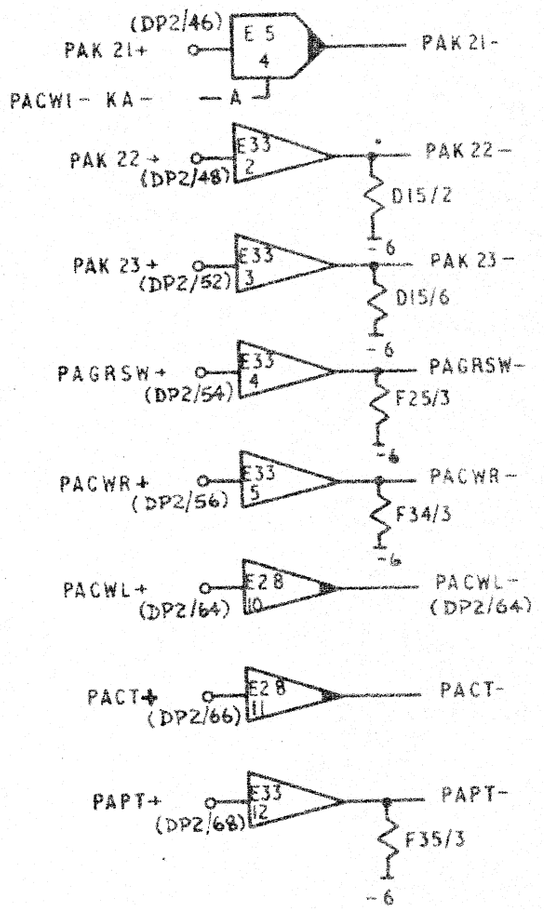


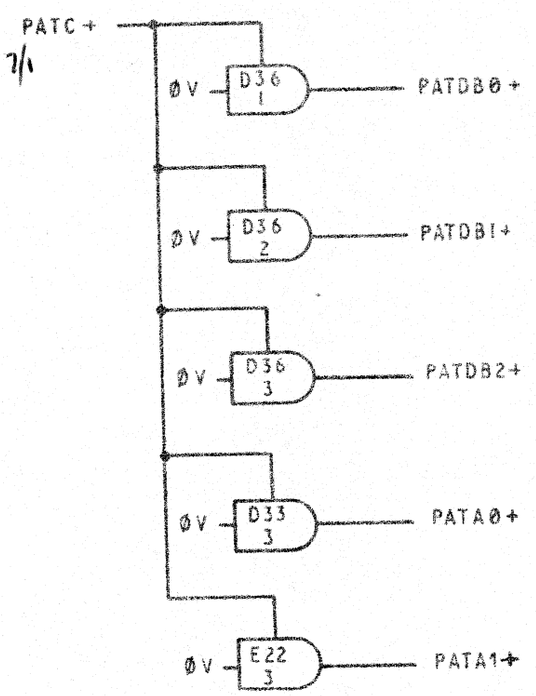
WGC 07/02

PIPE CONTROL.



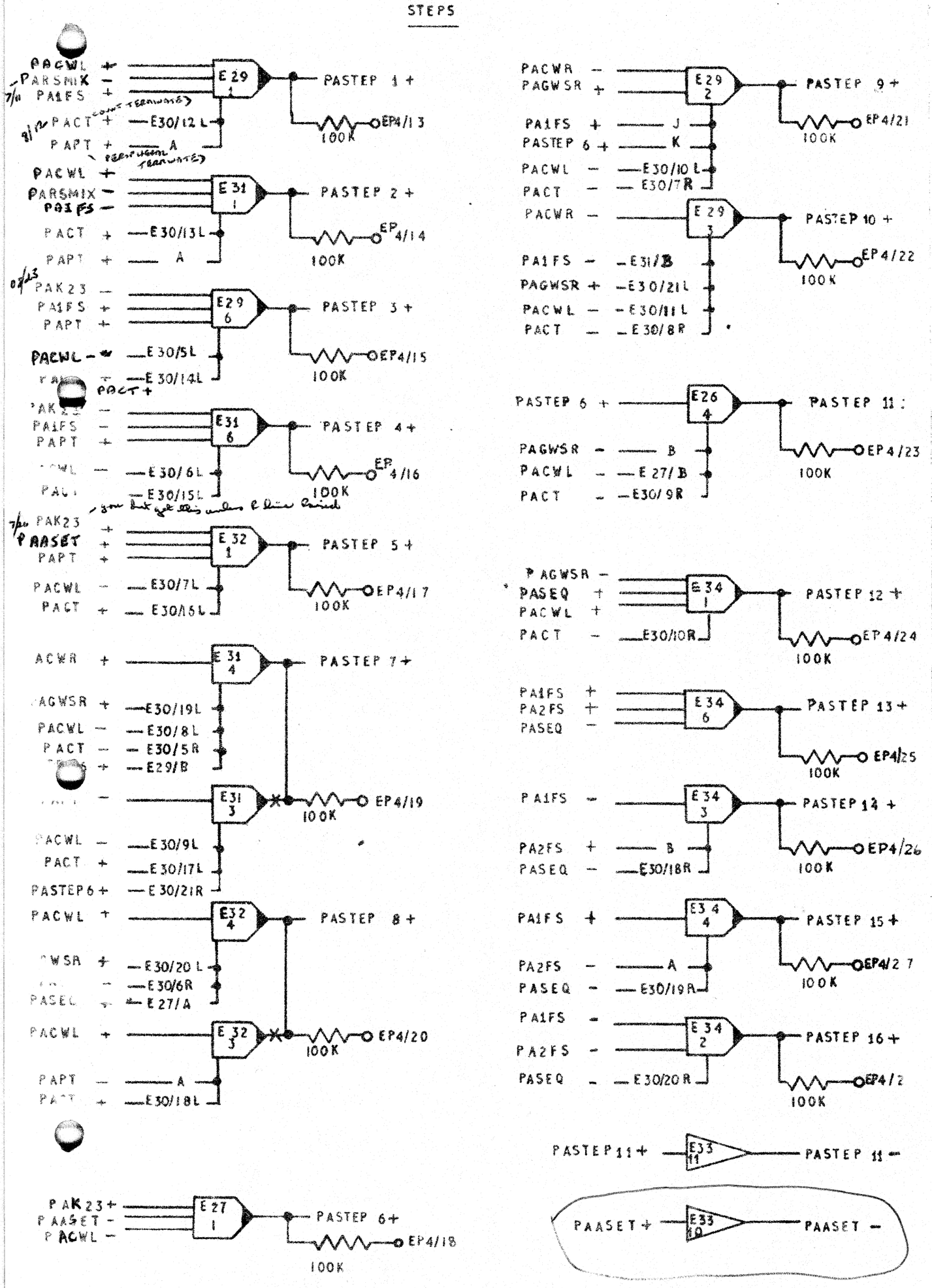
SUB	ISS	1	2	3	4


(DP2/46)
PAK 21+
E 5
4
PAK 21-
PACWI- KA-
A
PAK 22+
(DP2/48)
E33
2
PAK 22-
D15/2
-6
PAK 23+
(DP2/52)
E33
3
PAK 23-
D15/6
-6
PAGRSW+
(DP2/54)
E33
4
PAGRSW-
F25/3
-6
PACWR+
(DP2/56)
E33
5
PACWR-
F34/3
-6
PACWL+
(DP2/64)
E28
10
PACWL-
(DP2/64)
PACT+
(DP2/66)
E28
11
PACT-
PAPT+
(DP2/68)
E33
12
PAPT-
F35/3
-6


PATC+
7/1
ØV
D36
1
PATDB0+
ØV
D36
2
PATDB1+
ØV
D36
3
PATDB2+
ØV
D33
3
PATA0+
7/20.
ØV
E22
3
PATA1+

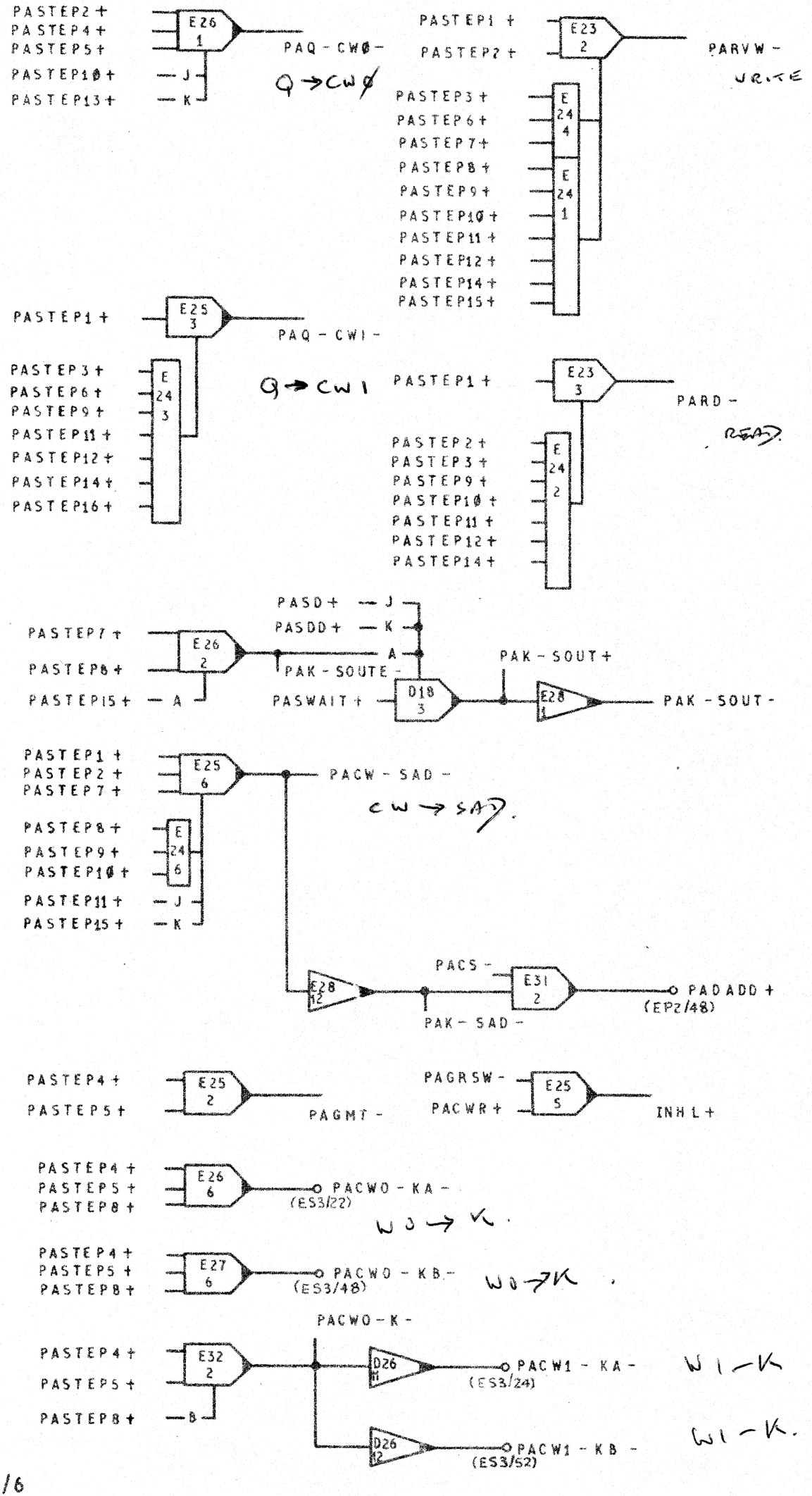
MICRO PROC STEPS.

STEPS

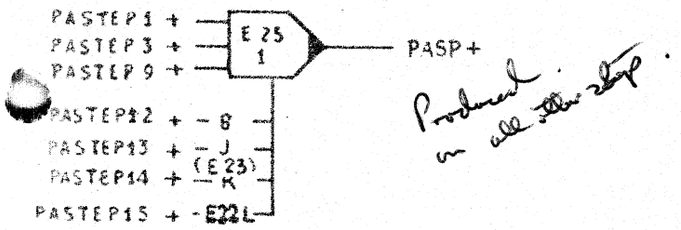


WGC07/5

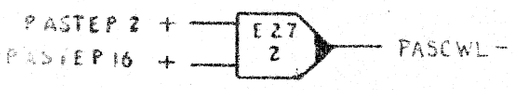
PART DECODED OF STEPS.

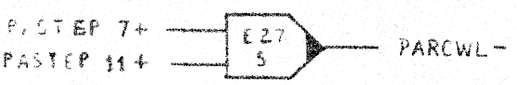


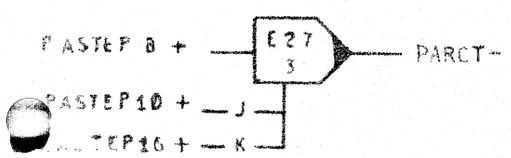
DECODE OF STEPS

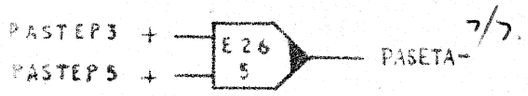


Produced in all other steps.









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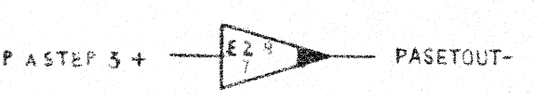
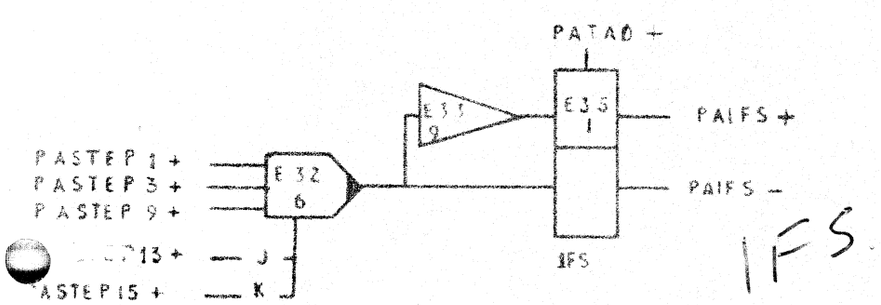


?/26



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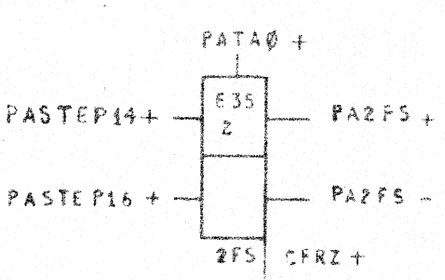

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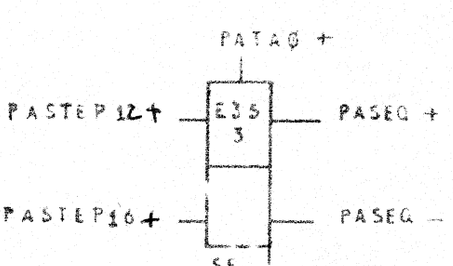
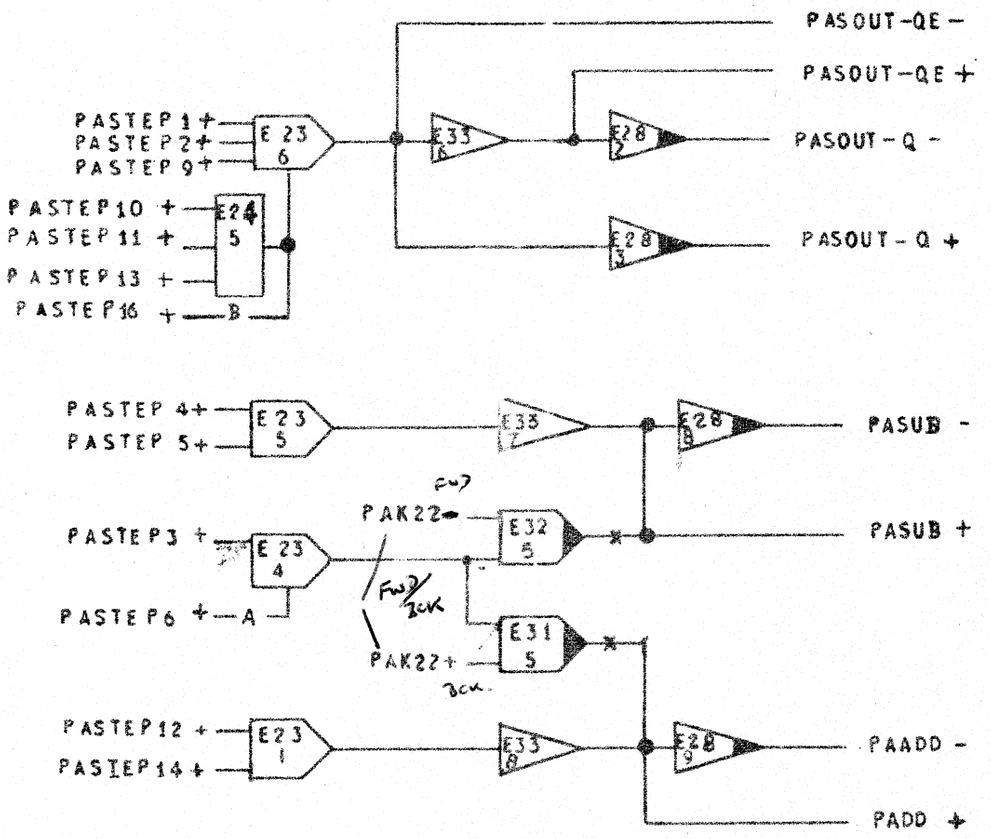


SEQ.

DECODE OF STEPS



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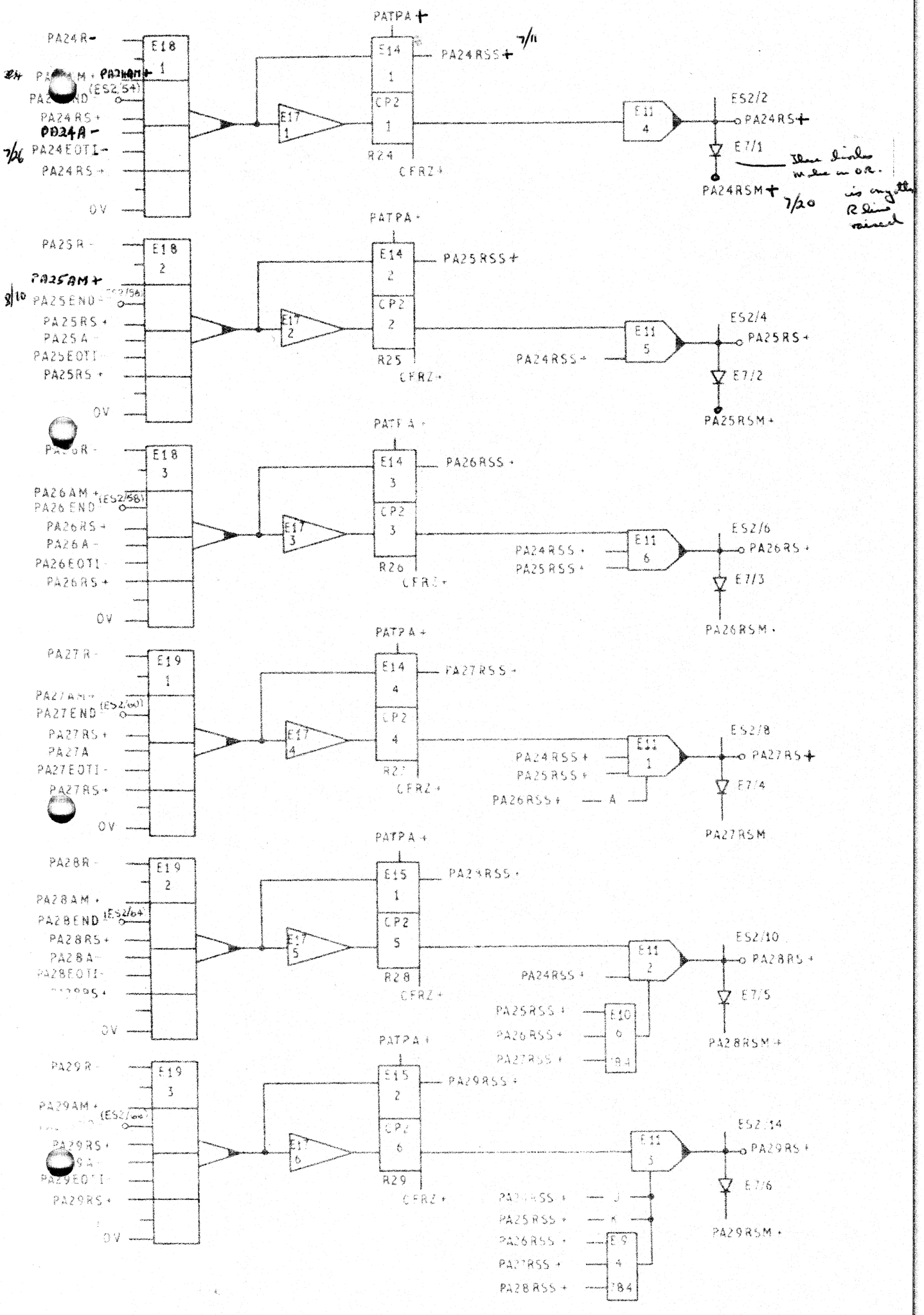
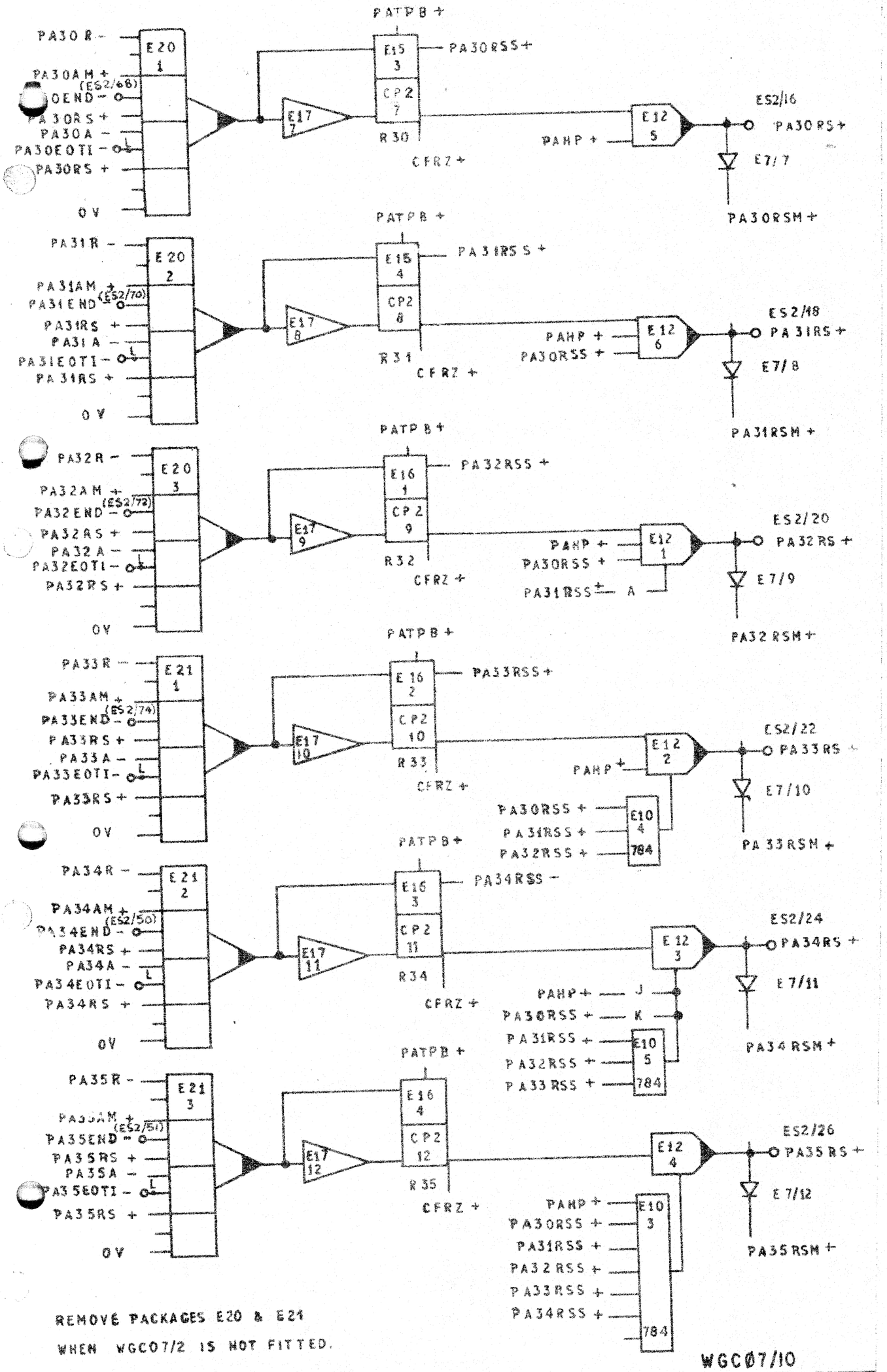
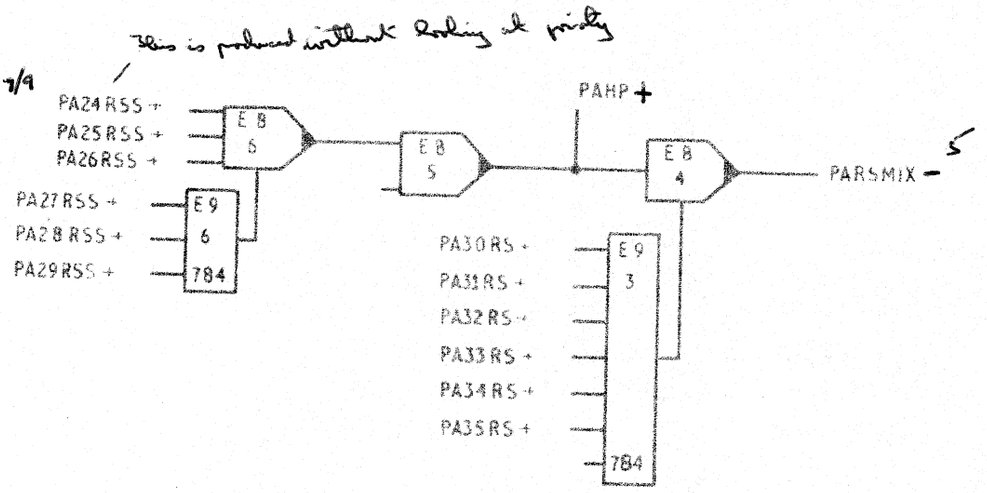
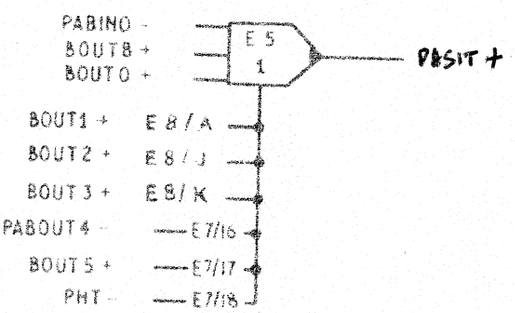
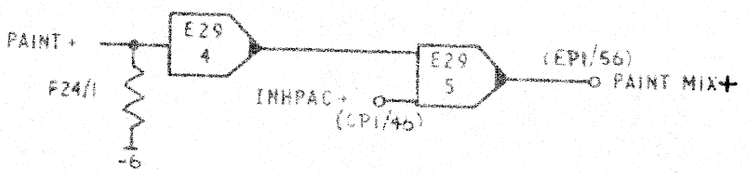


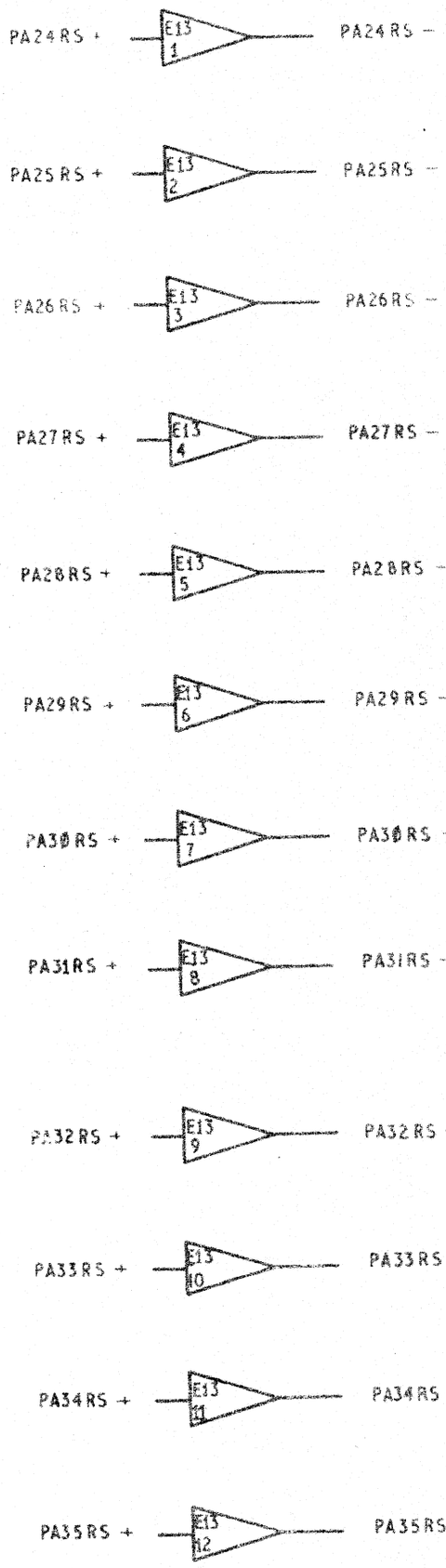
WGC07/9


PATPB +
PA30R –
E20 1
PA30AM + (ES2/68)
OEND –
PA30RS +
PA30A –
PA30EOTI –
PA30RS +
0V
E17 7
E15 3
CP2 7
R30
PA30RSS +
CFRZ +
PAHP +
E12 5
ES2/16
PA30RS +
E7/7
PA30RSM +
PATPB +
PA31R –
E20 2
PA31AM + (ES2/70)
PA31END –
PA31RS +
PA31A –
PA31EOTI –
PA31RS +
0V
E17 8
E15 4
CP2 8
R31
PA31RSS +
CFRZ +
PAHP +
PA30RSS +
E12 6
ES2/18
PA31RS +
E7/8
PA31RSM +
PATPB +
PA32R –
E20 3
PA32AM + (ES2/72)
PA32END –
PA32RS +
PA32A –
PA32EOTI –
PA32RS +
0V
E17 9
E16 1
CP2 9
R32
PA32RSS +
CFRZ +
PAHP +
PA30RSS +
PA31RSS + A
E12 1
ES2/20
PA32RS +
E7/9
PA32RSM +
PATPB +
PA33R –
E21 1
PA33AM + (ES2/74)
PA33END –
PA33RS +
PA33A –
PA33EOTI –
PA33RS +
0V
E17 10
E16 2
CP2 10
R33
PA33RSS +
CFRZ +
PAHP +
PA30RSS +
PA31RSS +
PA32RSS +
E10 4
784
E12 2
ES2/22
PA33RS +
E7/10
PA33RSM +
PATPB +
PA34R –
E21 2
PA34AM + (ES2/50)
PA34END –
PA34RS +
PA34A –
PA34EOTI –
PA34RS +
0V
E17 11
E16 3
CP2 11
R34
PA34RSS –
CFRZ +
PAHP +
PA30RSS +
PA31RSS +
PA32RSS +
PA33RSS +
J
K
E10 5
784
E12 3
ES2/24
PA34RS +
E7/11
PA34RSM +
PATPB +
PA35R –
E21 3
PA35AM + (ES2/51)
PA35END –
PA35RS +
PA35A –
PA35EOTI –
PA35RS +
0V
E17 12
E16 4
CP2 12
R35
CFRZ +
PAHP +
PA30RSS +
PA31RSS +
PA32RSS +
PA33RSS +
PA34RSS +
E10 3
784
E12 4
ES2/26
PA35RS +
E7/12
PA35RSM +
REMOVE PACKAGES E20 & E21
WHEN WGC07/2 IS NOT FITTED.
WGC07/10
SUB ISS 1

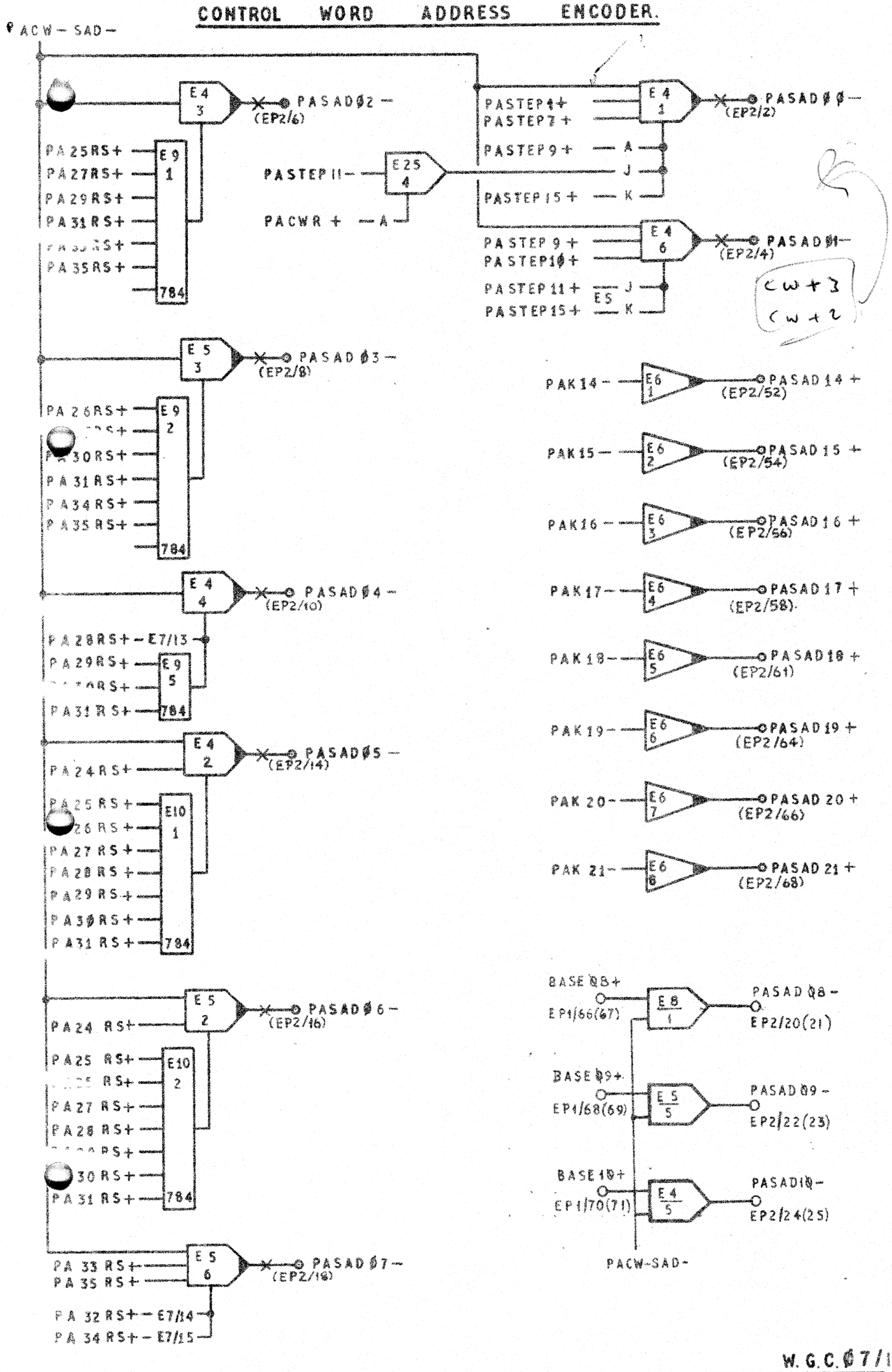

This is produced without looking at polarity
7/9
PA24RSS+
PA25RSS+
PA26RSS+
E8 6
PA27RSS+
PA28RSS+
PA29RSS+
E9 6 784
E8 5
PAHP+
E8 4
PARSMIX−
5
PA30RS+
PA31RS+
PA32RS+
PA33RS+
PA34RS+
PA35RS+
E9 3 784


PABINO−
BOUTB+
BOUTO+
E5 1
PBSIT+
BOUT1+
BOUT2+
BOUT3+
PABOUT4−
BOUT5+
PHT−
E8/A
E8/J
E8/K
E7/16
E7/17
E7/18


PAINT+
F24/1
-6
E29 4
INHPAC+
(CP1/45)
E29 5
(EP1/56)
PAINT MIX+

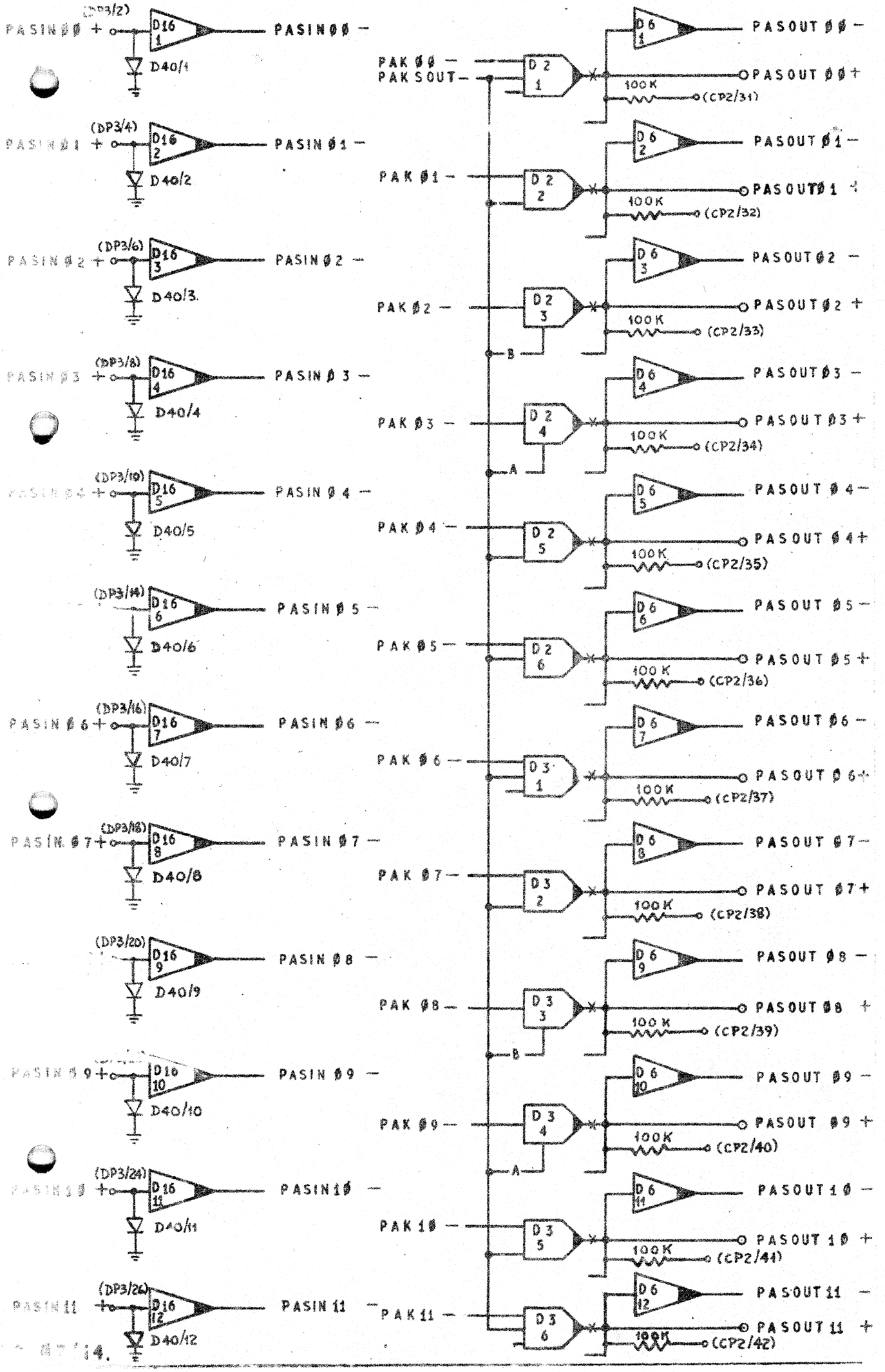

PA24RS +
E13
1
PA24RS –
PA25RS +
E13
2
PA25RS –
PA26RS +
E13
3
PA26RS –
PA27RS +
E13
4
PA27RS –
PA28RS +
E13
5
PA28RS –
PA29RS +
E13
6
PA29RS –
PA30RS +
E13
7
PA30RS –
PA31RS +
E13
8
PA31RS –
PA32RS +
E13
9
PA32RS –
PA33RS +
E13
10
PA33RS –
PA34RS +
E13
11
PA34RS –
PA35RS +
E13
12
PA35RS –

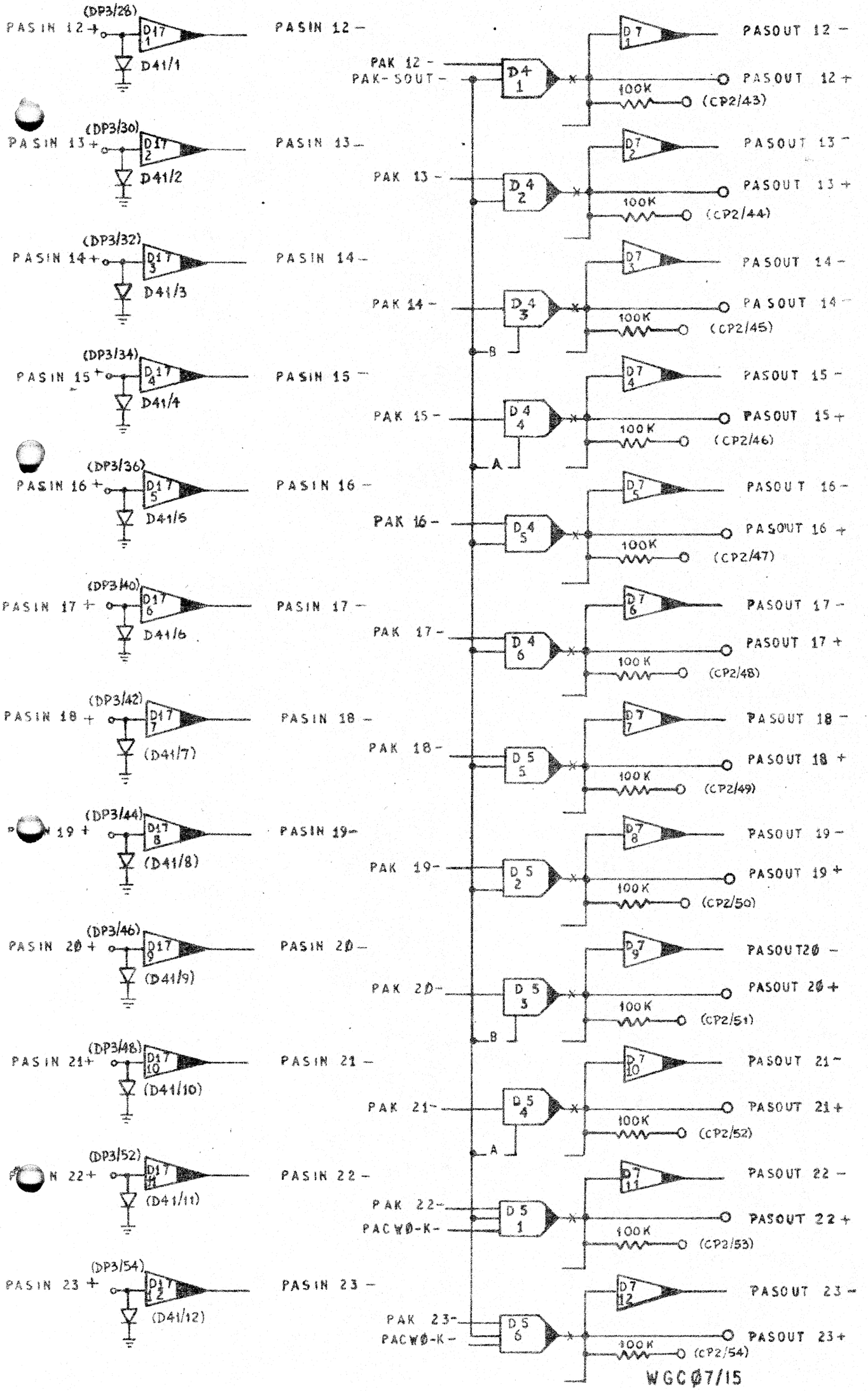
CONTROL WORD ADDRESS ENCODER.



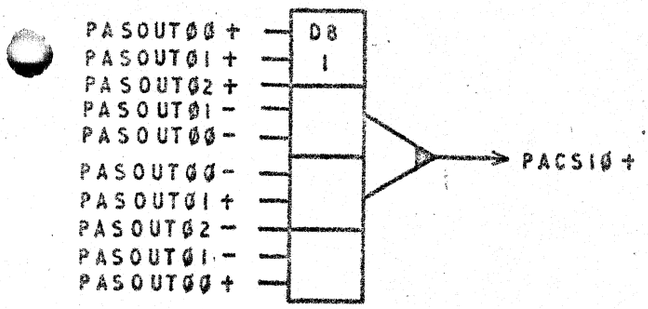
W.G.C.Ø7/13

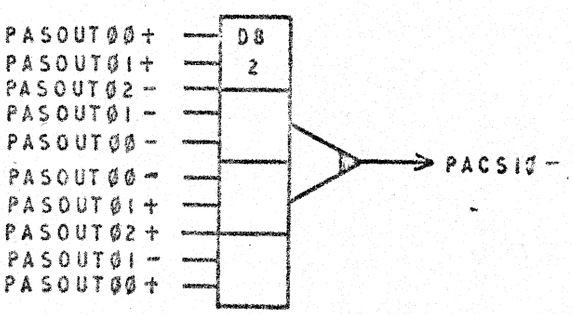
CENTRAL CONTROL SIN & SOUT

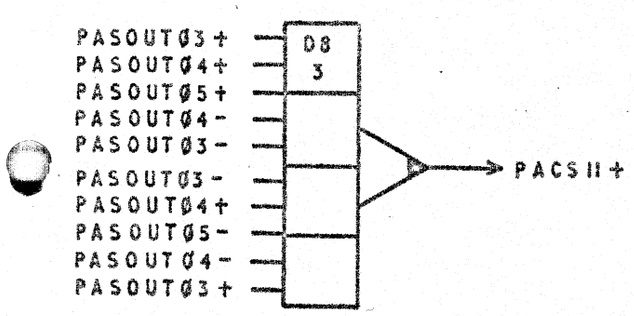


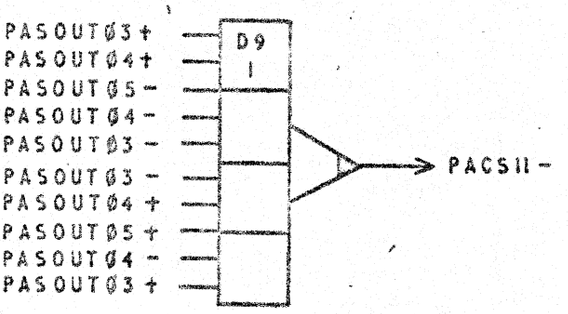

(DP3/28)
PASIN 12+
D17 1
D41/1
(DP3/30)
PASIN 13+
D17 2
D41/2
(DP3/32)
PASIN 14+
D17 3
D41/3
(DP3/34)
PASIN 15+
D17 4
D41/4
(DP3/36)
PASIN 16+
D17 5
D41/5
(DP3/40)
PASIN 17+
D17 6
D41/6
(DP3/42)
PASIN 18+
D17 7
(D41/7)
(DP3/44)
19+
D17 8
(D41/8)
(DP3/46)
PASIN 20+
D17 9
(D41/9)
(DP3/48)
PASIN 21+
D17 10
(D41/10)
(DP3/52)
N 22+
D17 11
(D41/11)
(DP3/54)
PASIN 23+
D17 12
(D41/12)
PASIN 12-
PAK 12-
PAK-SOUT-
D4 1
100K
(CP2/43)
D7 1
PASOUT 12-
PASOUT 12+
PASIN 13-
PAK 13-
D4 2
100K
(CP2/44)
D7 2
PASOUT 13-
PASOUT 13+
PASIN 14-
PAK 14-
D4 3
100K
(CP2/45)
D7 3
PASOUT 14-
PASOUT 14+
B
PASIN 15-
PAK 15-
D4 4
100K
(CP2/46)
D7 4
PASOUT 15-
PASOUT 15+
A
PASIN 16-
PAK 16-
D4 5
100K
(CP2/47)
D7 5
PASOUT 16-
PASOUT 16+
PASIN 17-
PAK 17-
D4 6
100K
(CP2/48)
D7 6
PASOUT 17-
PASOUT 17+
PASIN 18-
PAK 18-
D5 5
100K
(CP2/49)
D7 7
PASOUT 18-
PASOUT 18+
PASIN 19-
PAK 19-
D5 2
100K
(CP2/50)
D7 8
PASOUT 19-
PASOUT 19+
PASIN 20-
PAK 20-
D5 3
100K
(CP2/51)
D7 9
PASOUT20-
PASOUT 20+
B
PASIN 21-
PAK 21-
D5 4
100K
(CP2/52)
D7 10
PASOUT 21-
PASOUT 21+
A
PASIN 22-
PAK 22-
PACW0-K-
D5 1
100K
(CP2/53)
D7 11
PASOUT 22-
PASOUT 22+
PASIN 23-
PAK 23-
PACW0-K-
D5 6
100K
(CP2/54)
D7 12
PASOUT 23-
PASOUT 23+
WGC07/15

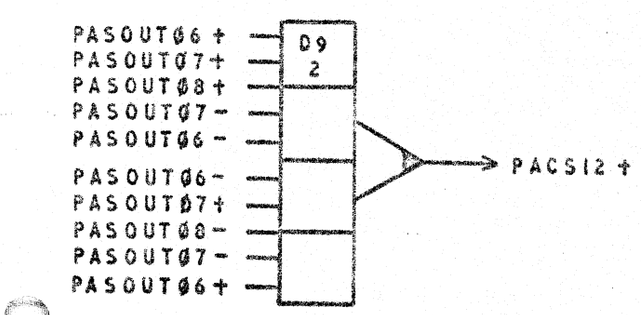
PARITY

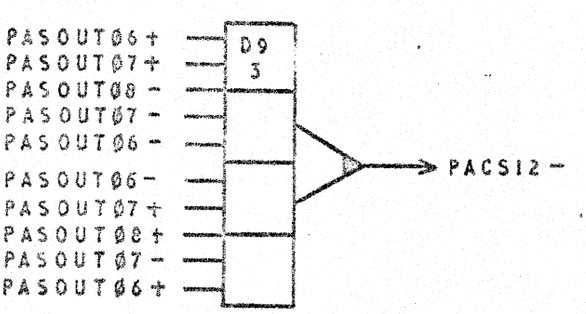


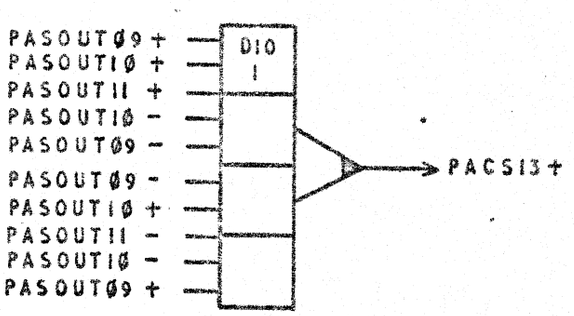


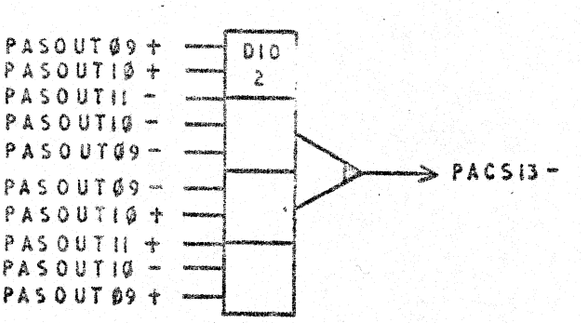












WGCØ7/16

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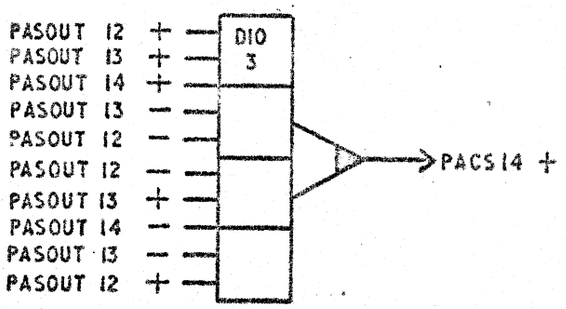
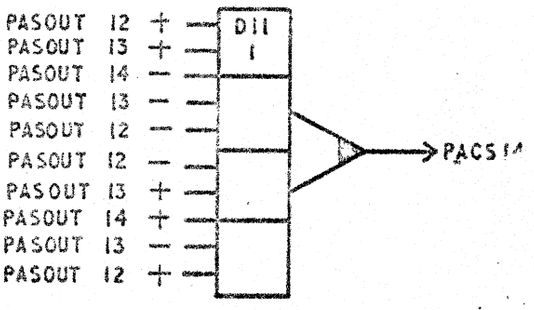
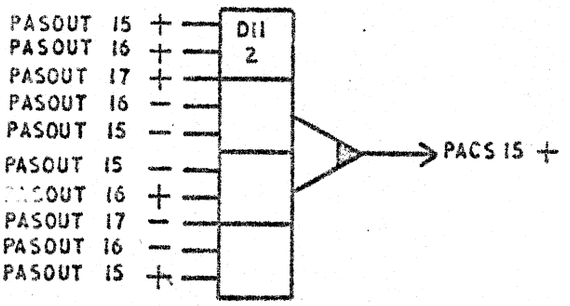
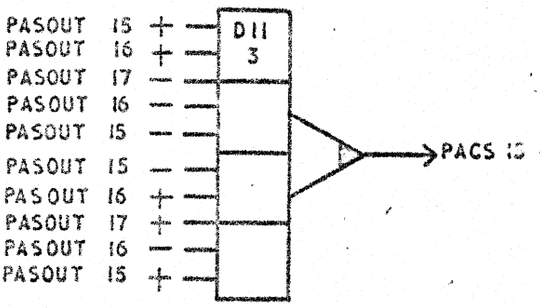
ACW	0874														
DATE															

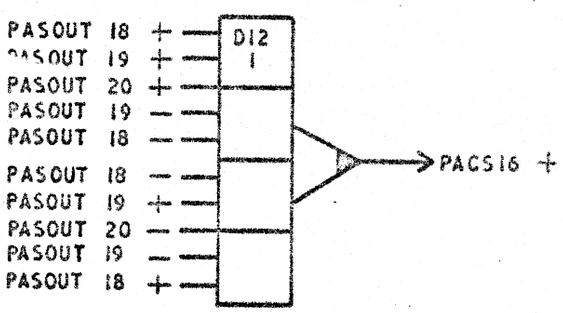
PARITY.

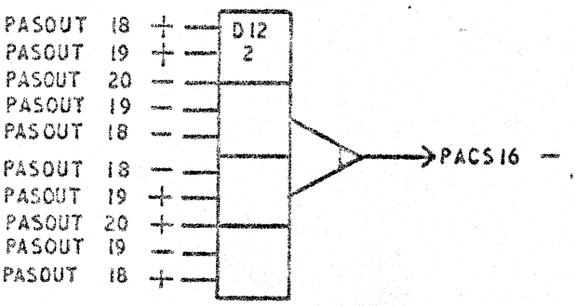


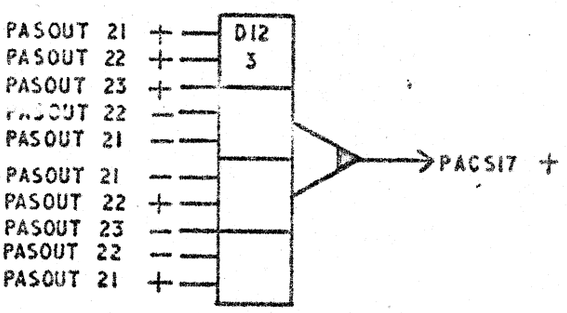


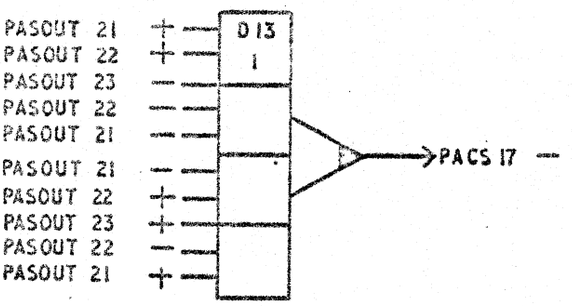












WGC07/17

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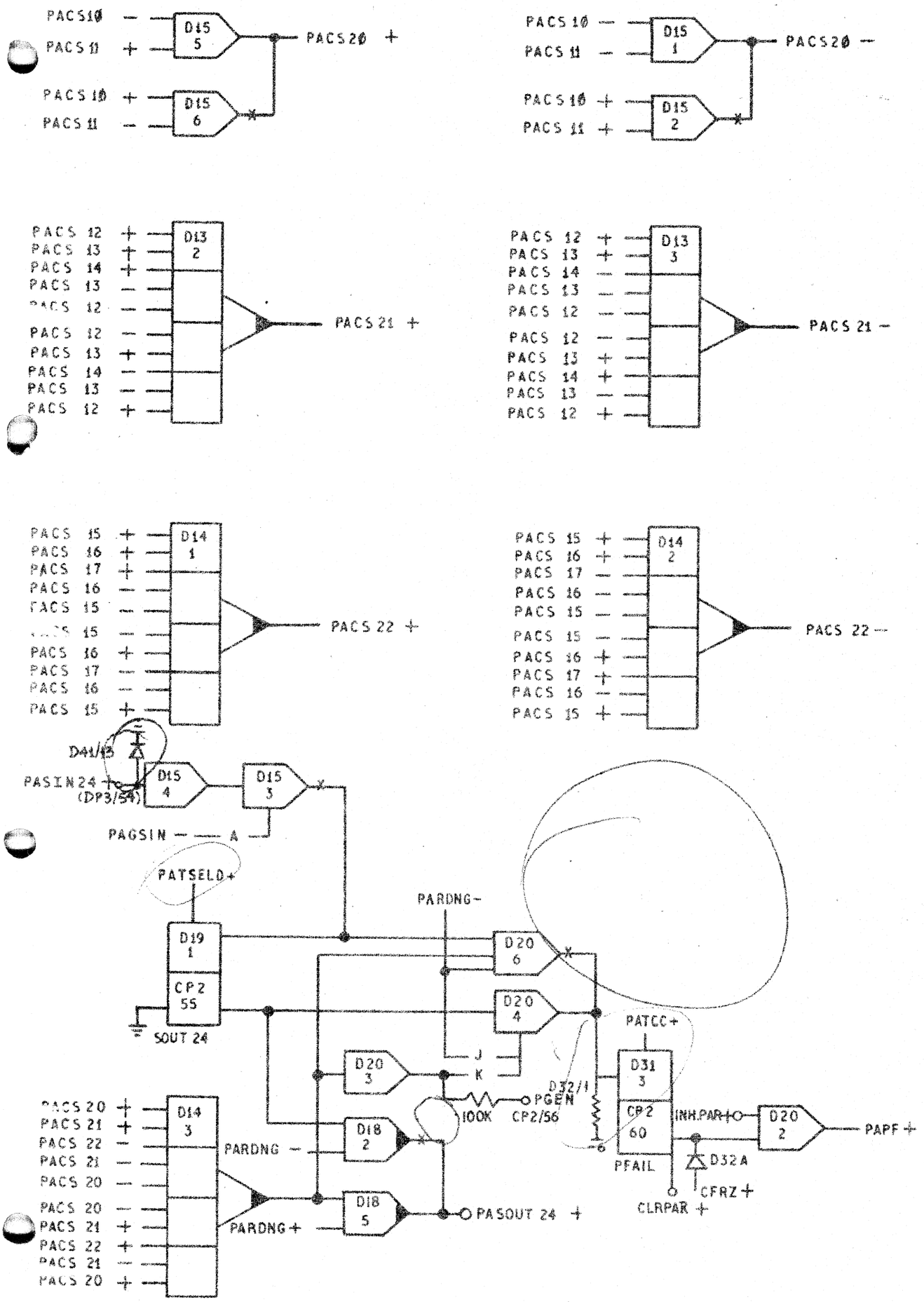
DATE	31/10/67														


PACS10 −
PACS 11 +
D15 5
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PACS 10 +
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PACS 10 +
PACS 11 +
D15 2
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100K
CP2/56
D32/1
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PACS 22 +
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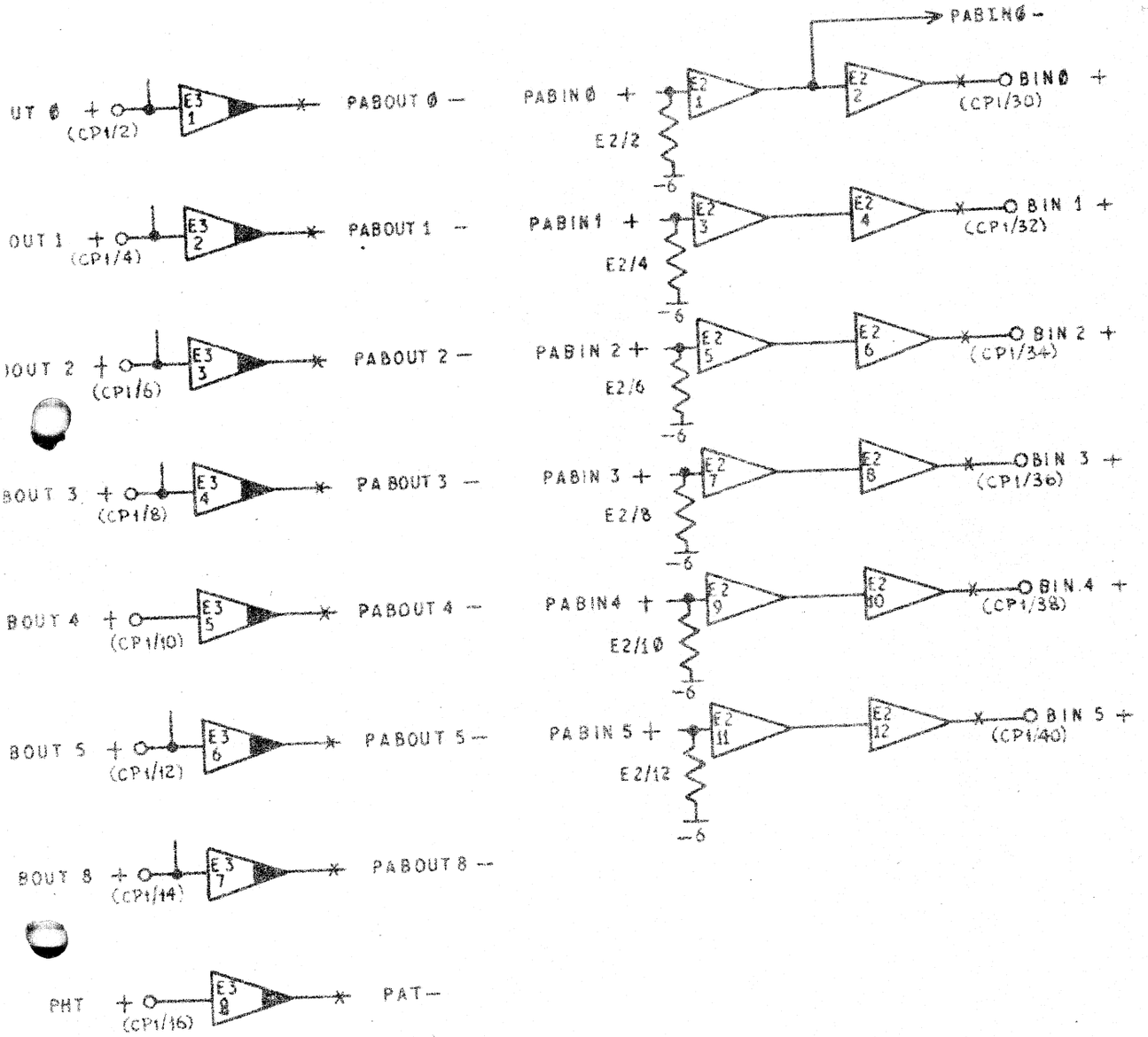
PACS 20 +
D14 3
PARDNG −
PARDNG+
D18 2
D18 5
PASOUT 24 +

GC.07/18

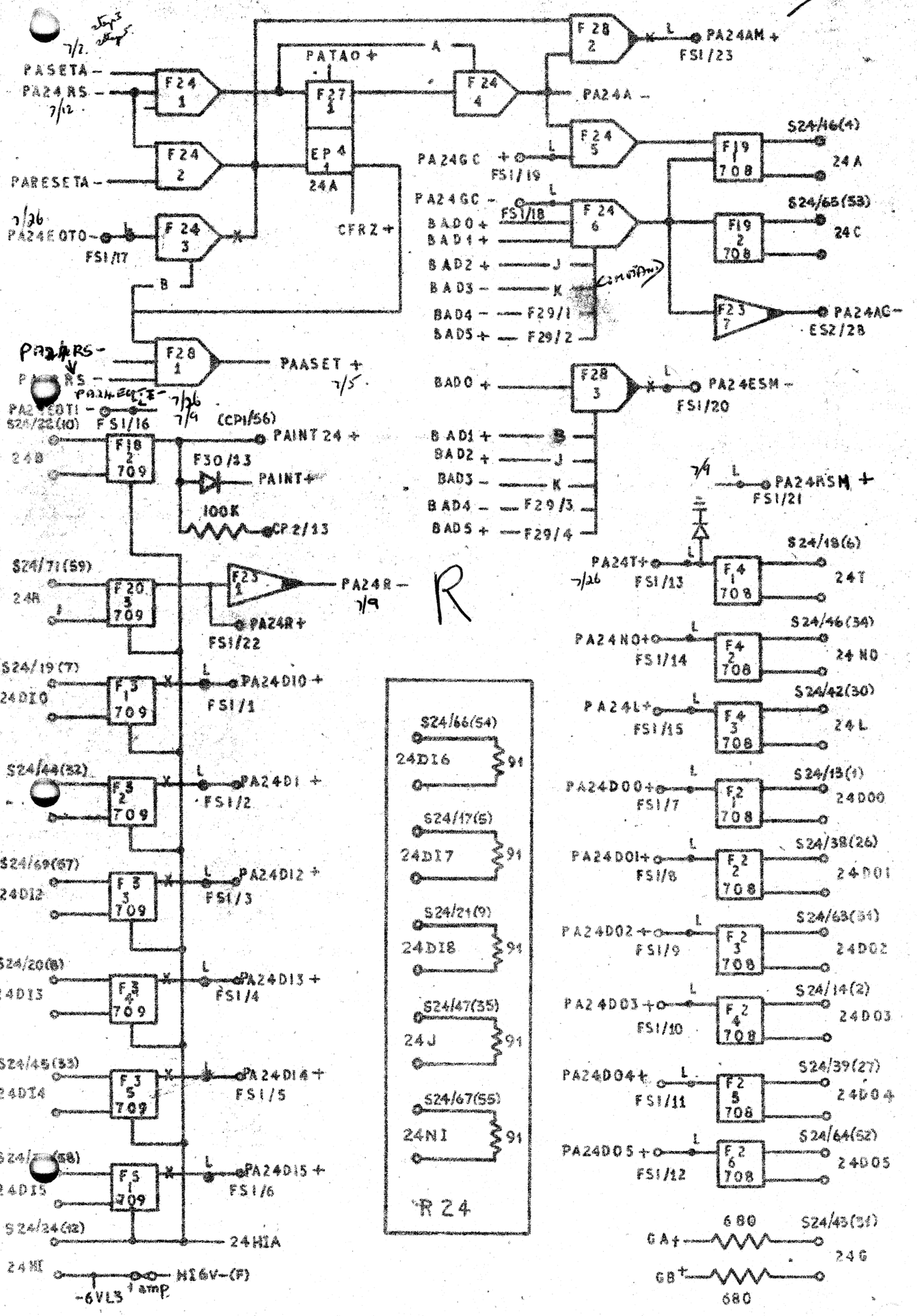
BIN & BOUT


PABIN0 –
UT 0 +
(CP1/2)
E3 1
PABOUT 0 –
PABIN 0 +
E2 1
E2 2
BIN0 +
(CP1/30)
E2/2
–6
OUT 1 +
(CP1/4)
E3 2
PABOUT 1 –
PABIN1 +
E2 3
E2 4
BIN 1 +
(CP1/32)
E2/4
–6
)OUT 2 +
(CP1/6)
E3 3
PABOUT 2 –
PABIN 2 +
E2 5
E2 6
BIN 2 +
(CP1/34)
E2/6
–6
BOUT 3 +
(CP1/8)
E3 4
PA BOUT 3 –
PABIN 3 +
E2 7
E2 8
BIN 3 +
(CP1/36)
E2/8
–6
BOUT 4 +
(CP1/10)
E3 5
PABOUT 4 –
PABIN4 +
E2 9
E2 10
BIN 4 +
(CP1/38)
E2/10
–6
BOUT 5 +
(CP1/12)
E3 6
PABOUT 5 –
PABIN 5 +
E2 11
E2 12
BIN 5 +
(CP1/40)
E2/12
–6
BOUT 8 +
(CP1/14)
E3 7
PABOUT 8 –
PHT +
(CP1/16)
E3 8
PAT –

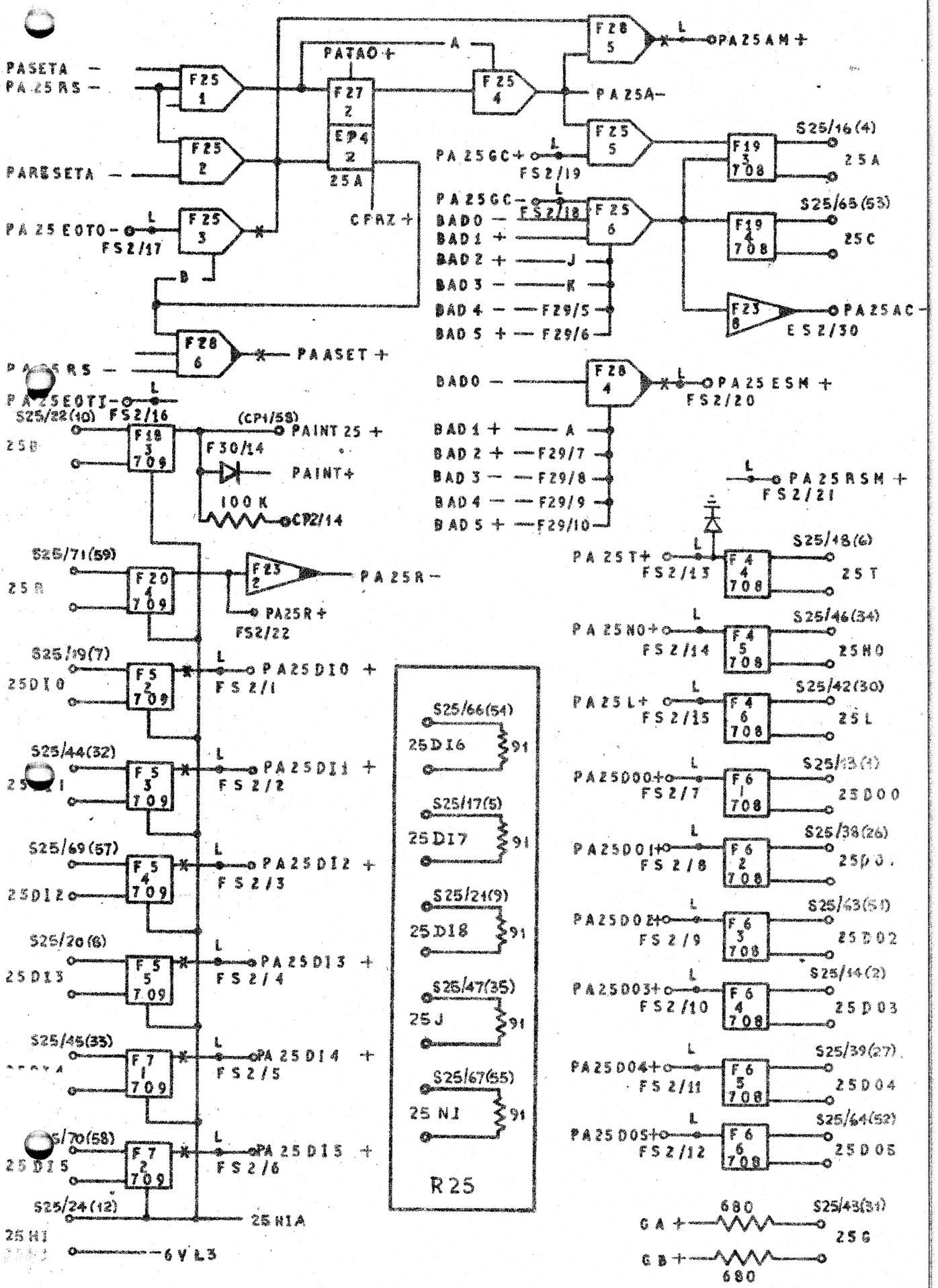
S.I. 24

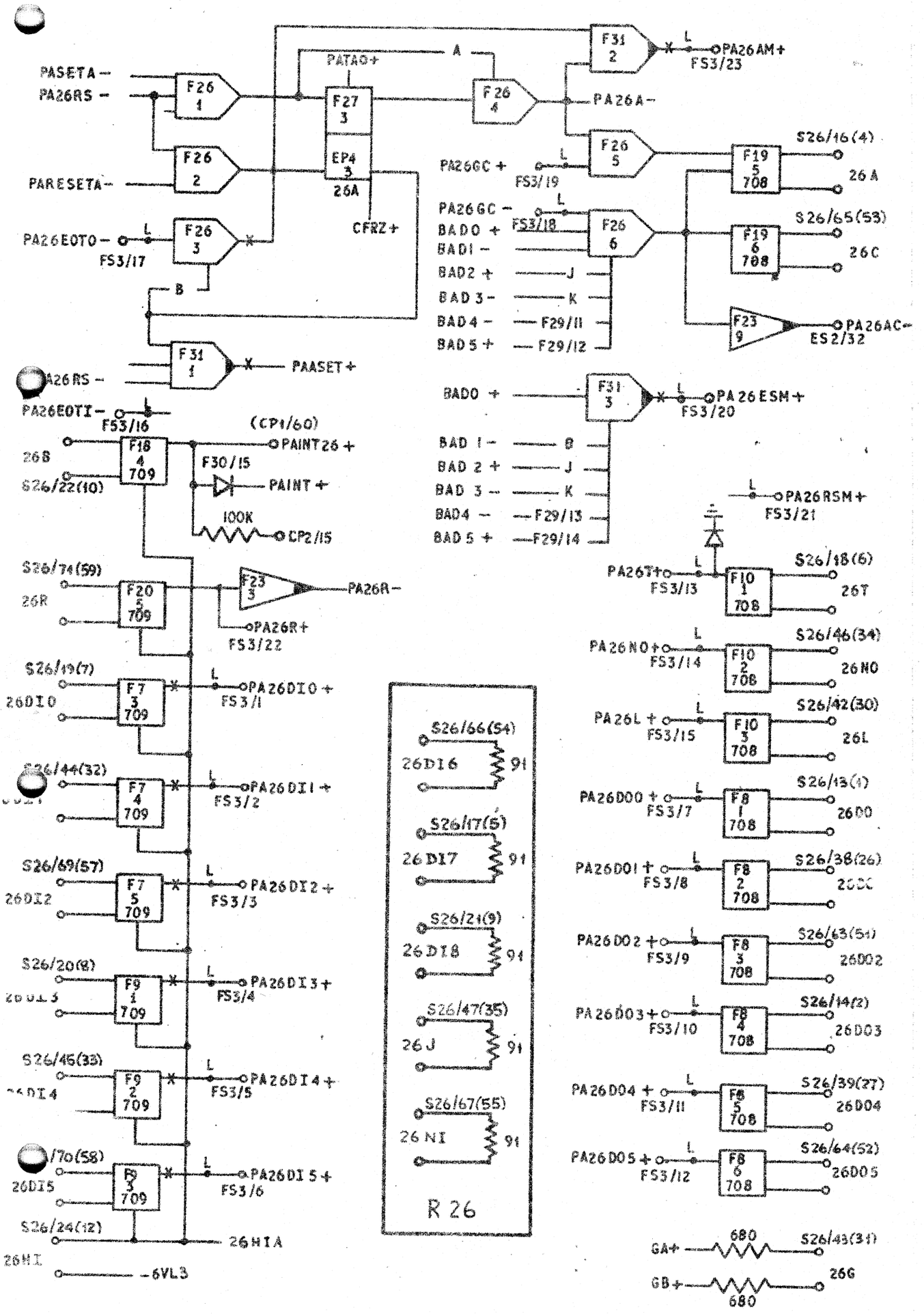
Using A line of group if pins limited

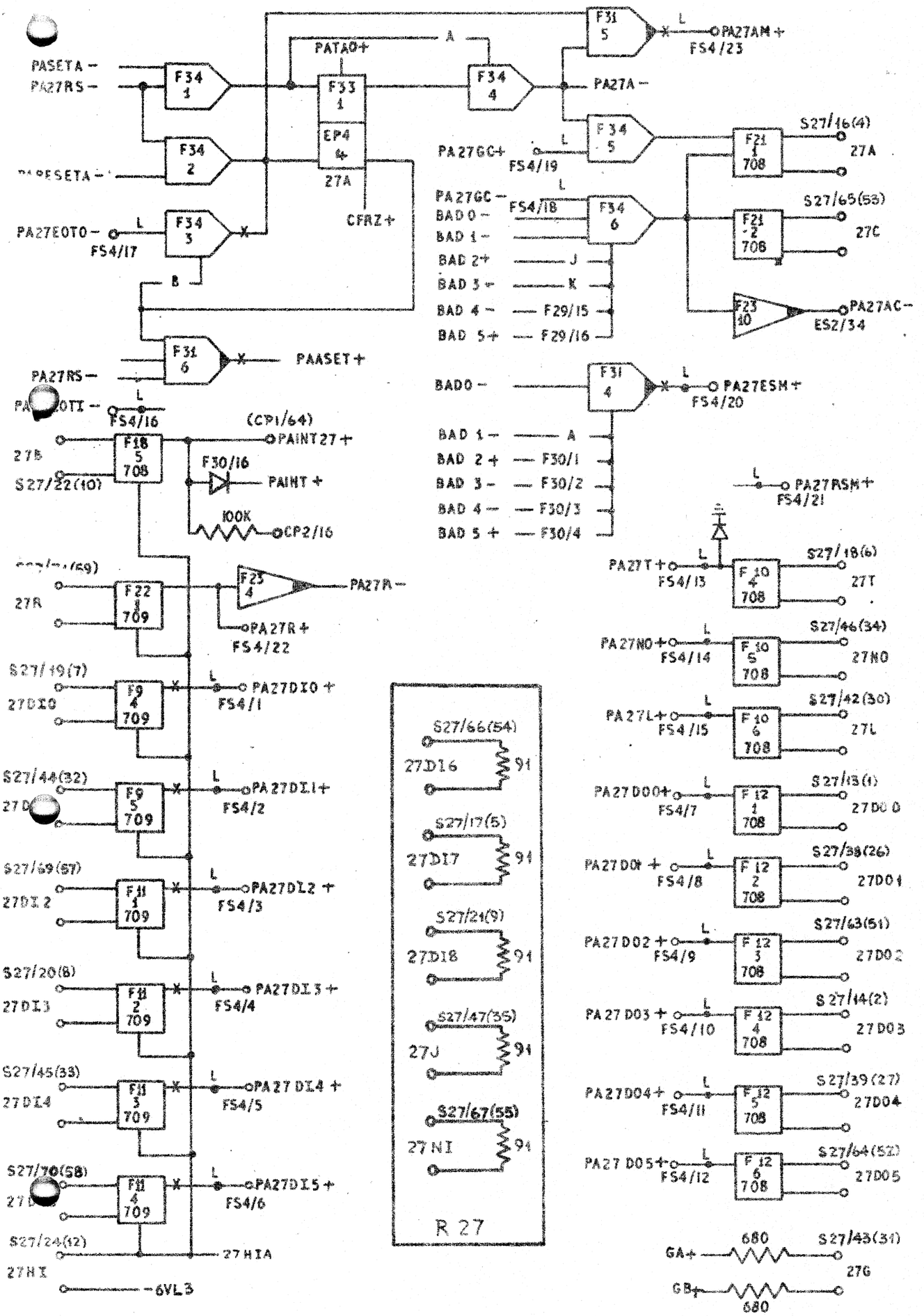
A MIX

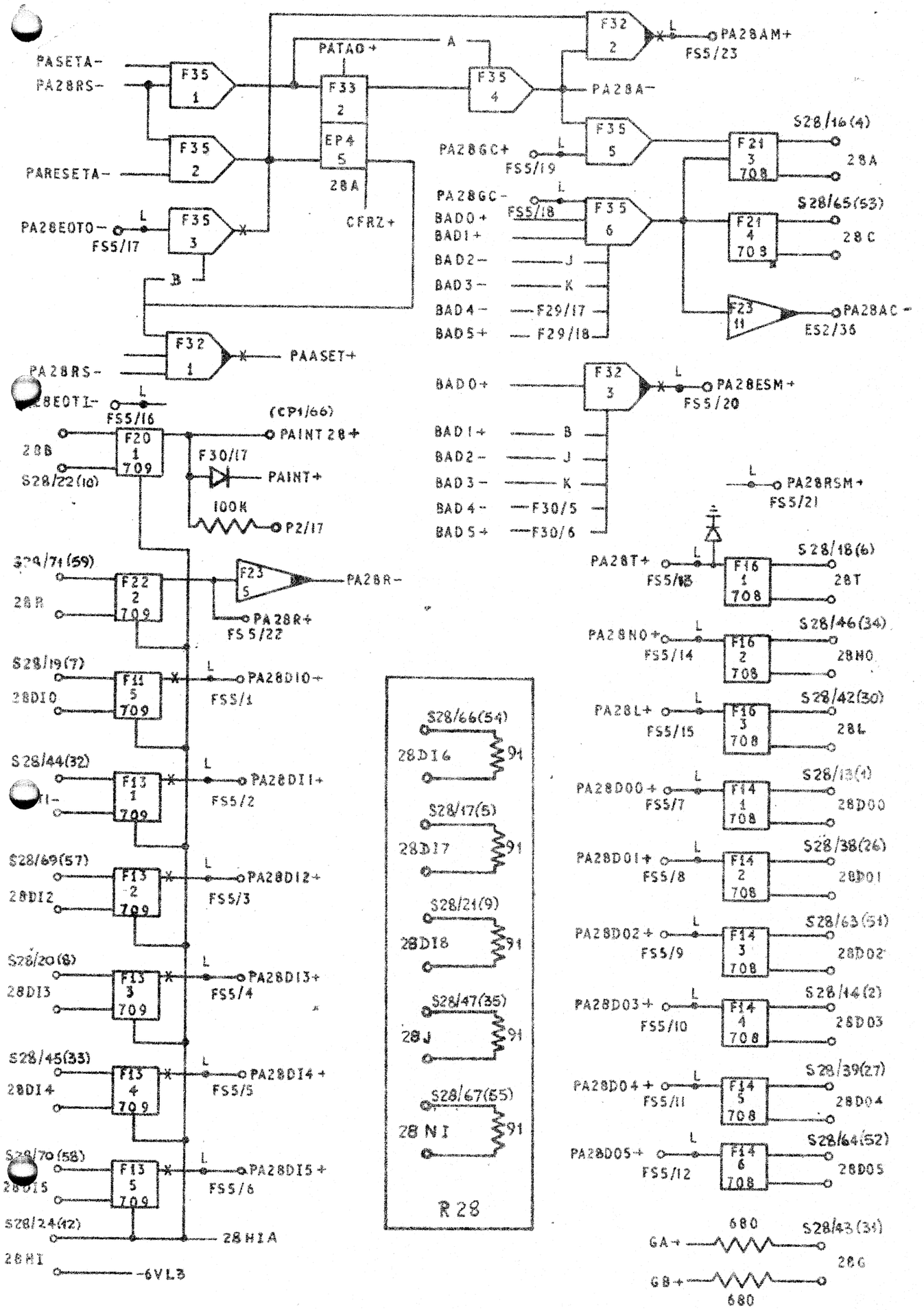


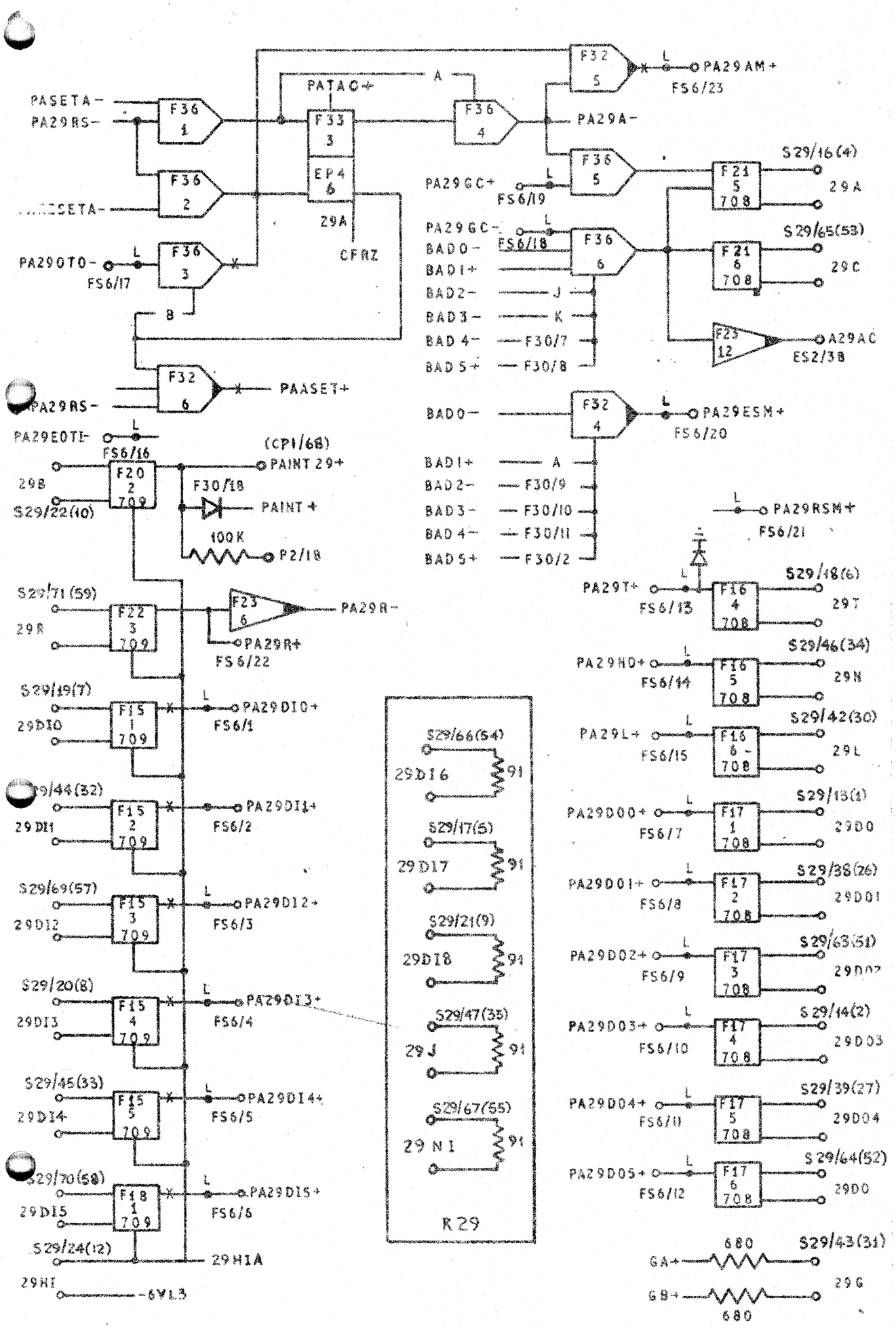
WGC07/20

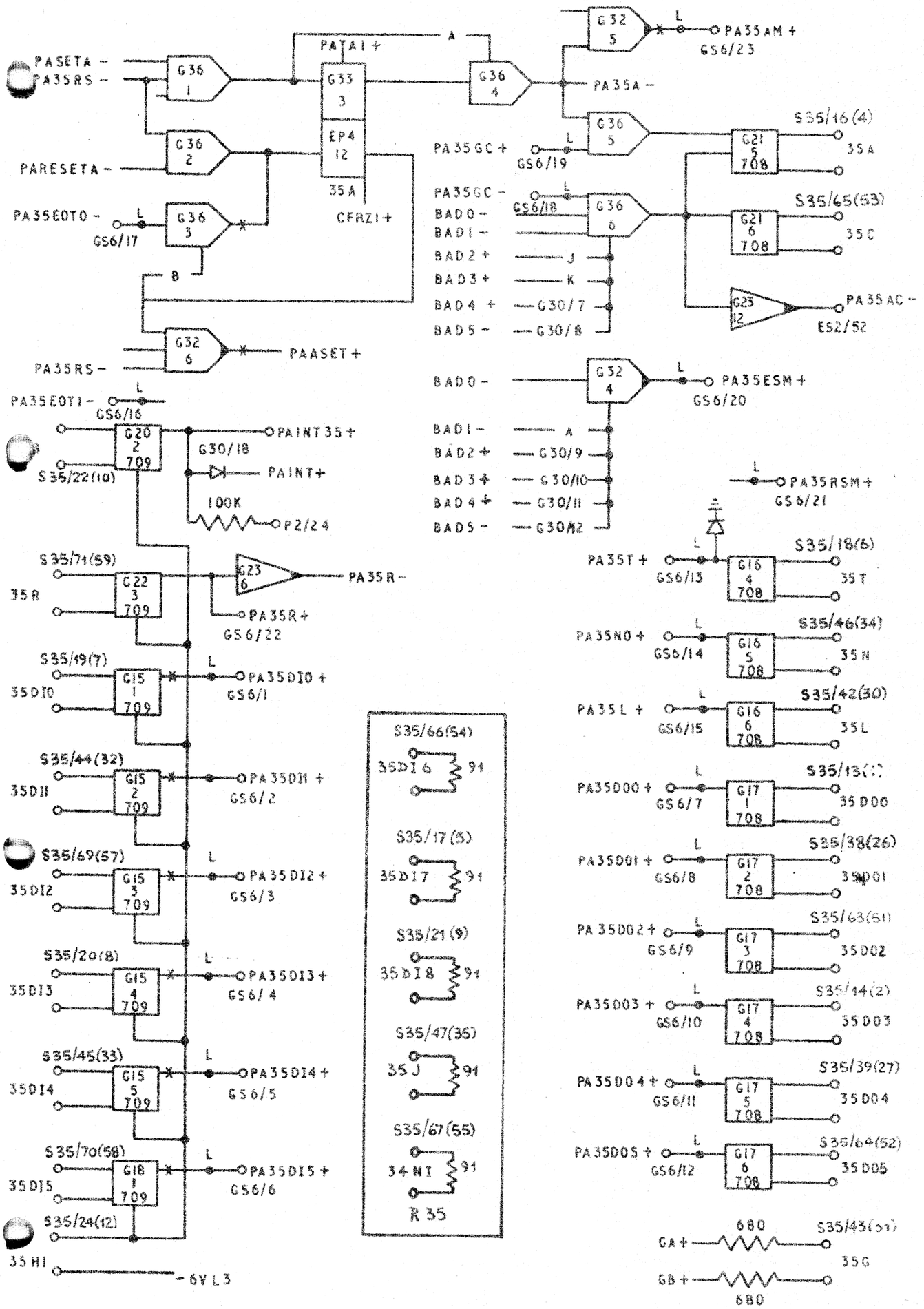

PASETA –
PA 25 RS –
PARESETA –
PA 25 EOTO –
FS2/17
PATAO +
A
B
CPAZ +
25A
PA25GC +
FS2/19
PA25GC –
FS2/18
BAD0 –
BAD1 +
BAD2 +
BAD3 –
BAD4 –
BAD5 +
F29/5
F29/6
PA25AM +
PA25A –
PA25AC –
ES2/30
PA25ESM +
FS2/20
PA25RSM +
FS2/21
PAASET +
PA25EOTI –
FS2/16
S25/22(10)
25B
(CP1/58)
PAINT 25 +
F30/14
PAINT +
100K
CP2/14
S25/71(59)
25R
PA25R –
PA25R +
FS2/22
S25/19(7)
25DI0
PA25DI0 +
FS2/1
S25/44(32)
PA25DI1 +
FS2/2
S25/69(57)
25DI2
PA25DI2 +
FS2/3
S25/20(6)
25DI3
PA25DI3 +
FS2/4
S25/45(33)
PA25DI4 +
FS2/5
S25/70(58)
25DI5
PA25DI5 +
FS2/6
S25/24(12)
25NIA
25NI
6VL3
S25/66(54)
25DI6
91
S25/17(5)
25DI7
S25/21(9)
25DI8
S25/47(35)
25J
S25/67(55)
25NI
R25
PA25T +
FS2/13
S25/48(6)
25T
PA25NO +
FS2/14
S25/46(34)
25NO
PA25L +
FS2/15
S25/42(30)
25L
PA25D00 +
FS2/7
S25/43(31)
25D00
PA25D01 +
FS2/8
S25/38(26)
25D01
PA25D02 +
FS2/9
S25/63(51)
25D02
PA25D03 +
FS2/10
S25/44(32)
25D03
PA25D04 +
FS2/11
S25/39(27)
25D04
PA25D05 +
FS2/12
S25/64(52)
25D05
GA +
680
S25/43(31)
25G
GB +
680


PASETA –
PA26RS –
PARESETA –
PA26E0TO –
FS3/17
PA26E0TI –
FS3/16
PAATA0 +
A
B
CFRZ +
26A
EP4 3
F26 1
F26 2
F26 3
F26 4
F26 5
F26 6
F27 3
F31 1
F31 2
F31 3
PAASET +
PA26AM +
FS3/23
PA26A –
PA26GC +
FS3/19
PA26GC –
FS3/18
BAD0 +
BAD1 –
BAD2 +
BAD3 –
BAD4 –
BAD5 +
J
K
F29/11
F29/12
F19 5 708
F19 6 708
F23 9
S26/16(4)
26A
S26/65(53)
26C
PA26AC –
ES2/32
BAD0 +
BAD1 –
BAD2 +
BAD3 –
BAD4 –
BAD5 +
B
J
K
F29/13
F29/14
PA26ESM +
FS3/20
PA26RSM +
FS3/21
PA26T +
FS3/13
F10 1 708
S26/18(6)
26T
PA26N0 +
FS3/14
F10 2 708
S26/46(34)
26N0
PA26L +
FS3/15
F10 3 708
S26/42(30)
26L
PA26D00 +
FS3/7
F8 1 708
S26/13(1)
26D0
PA26D01 +
FS3/8
F8 2 708
S26/38(26)
26D1
PA26D02 +
FS3/9
F8 3 708
S26/63(51)
26D02
PA26D03 +
FS3/10
F8 4 708
S26/14(2)
26D03
PA26D04 +
FS3/11
F8 5 708
S26/39(27)
26D04
PA26D05 +
FS3/12
F8 6 708
S26/64(52)
26D05
(CP1/60)
PAINT26 +
26B
S26/22(10)
F18 4 709
F30/15
PAINT +
100K
CP2/15
S26/74(59)
26R
F20 5 709
F23 3
PA26R –
PA26R +
FS3/22
S26/19(7)
26DI0
F7 3 709
PA26DI0 +
FS3/1
S26/44(32)
F7 4 709
PA26DI1 +
FS3/2
S26/69(57)
26DI2
F7 5 709
PA26DI2 +
FS3/3
S26/20(8)
F9 1 709
PA26DI3 +
FS3/4
S26/46(33)
F9 2 709
PA26DI4 +
FS3/5
S26/70(58)
26DI5
F9 3 709
PA26DI5 +
FS3/6
S26/24(12)
26HIA
26HI
–6VL3
S26/66(54)
26DI6
91
S26/17(5)
26DI7
91
S26/21(9)
26DI8
91
S26/47(35)
26J
91
S26/67(55)
26NI
91
R26
GA +
680
S26/43(31)
GB +
680
26G


PASETA −
PA27RS −
F34 1
F34 2
PA27EOTO −
FS4/17
F34 3
PATAO+
A
F33 1
EP4 4
27A
CFAZ+
B
F34 4
F31 5
PA27AM+
FS4/23
PA27A−
F34 5
PA27GC+
FS4/19
F34 6
PA27GC−
FS4/18
BAD 0 −
BAD 1 −
BAD 2+
BAD 3+
BAD 4 −
BAD 5+
J
K
F29/15
F29/16
F21 1 708
S27/46(4)
27A
F21 2 708
S27/65(53)
27C
F23 10
PA27AC−
ES2/34
F31 6
PAASET+
PA27RS −
F31 4
BAD 0 −
BAD 1 −
BAD 2 +
BAD 3 −
BAD 4 −
BAD 5 +
A
F30/1
F30/2
F30/3
F30/4
PA27ESM+
FS4/20
PA27RSM+
FS4/21
FS4/16
(CP1/64)
PAINT27+
F18 5 708
27B
S27/22(10)
F30/16
PAINT+
100K
CP2/16
F22 1 709
27R
F23 4
PA27R−
PA27R+
FS4/22
S27/19(7)
27DI0
F9 4 709
PA27DI0+
FS4/1
S27/44(32)
F9 5 709
PA27DI1+
FS4/2
S27/69(57)
27DI2
F11 1 709
PA27DI2+
FS4/3
S27/20(8)
27DI3
F11 2 709
PA27DI3+
FS4/4
S27/45(33)
27DI4
F11 3 709
PA27DI4+
FS4/5
S27/70(58)
F11 4 709
PA27DI5+
FS4/6
S27/24(12)
27HI
27HIA
−6VL3
S27/66(54)
27D16
91
S27/17(5)
27DI7
91
S27/21(9)
27DI8
91
S27/47(35)
27J
91
S27/67(55)
27NI
91
R 27
PA27T+
FS4/13
F10 4 708
S27/18(6)
27T
PA27NO+
FS4/14
F10 5 708
S27/46(34)
27NO
PA27L+
FS4/15
F10 6 708
S27/42(30)
27L
PA27D00+
FS4/7
F12 1 708
S27/13(1)
27D00
PA27D01+
FS4/8
F12 2 708
S27/38(26)
27D01
PA27D02+
FS4/9
F12 3 708
S27/63(51)
27D02
PA27D03+
FS4/10
F12 4 708
S27/14(2)
27D03
PA27D04+
FS4/11
F12 5 708
S27/39(27)
27D04
PA27D05+
FS4/12
F12 6 708
S27/64(52)
27D05
GA+
680
S27/43(31)
27G
GB+
680

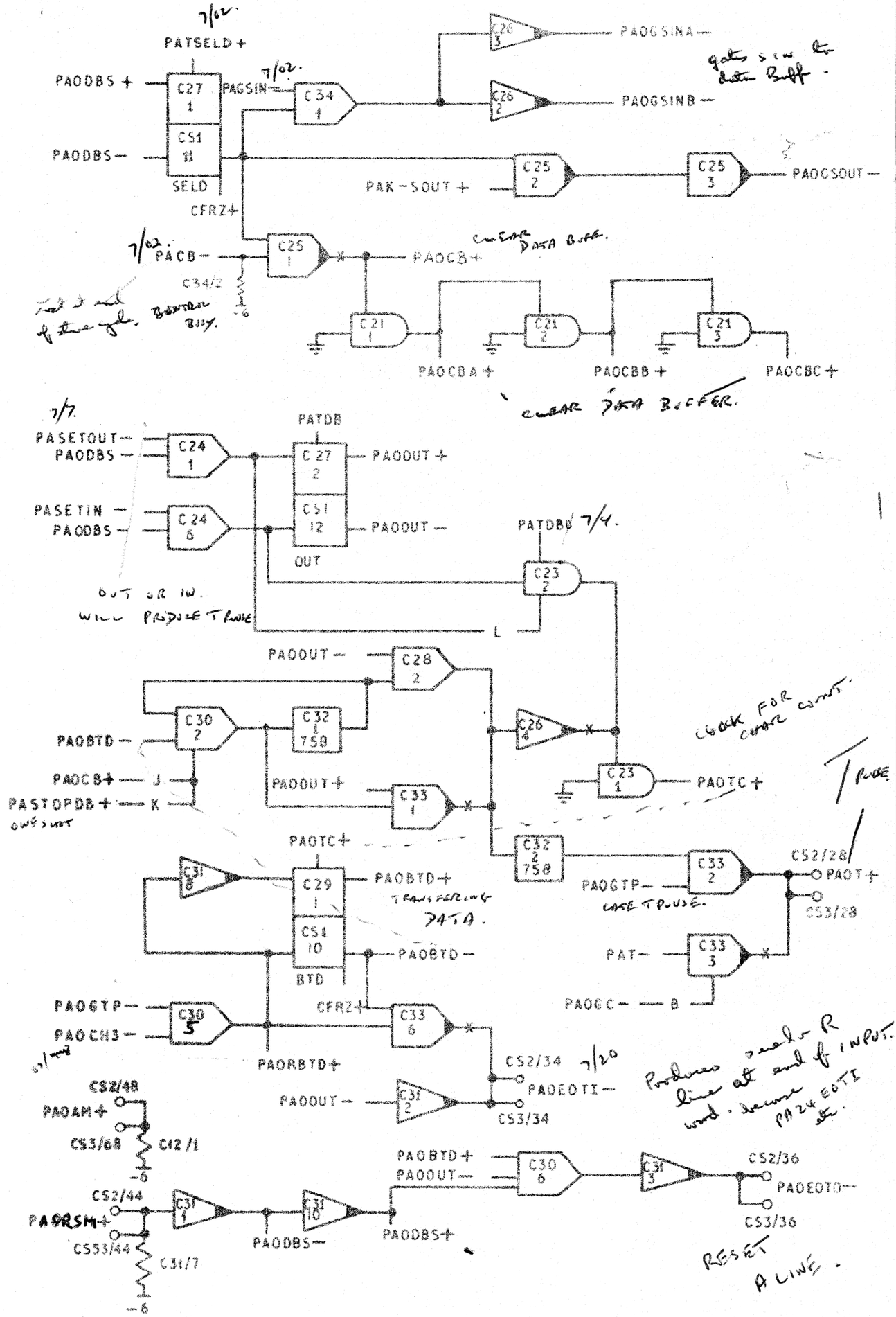

PASETA-
PA28RS-
PARESETA-
PA28EOTO-
FS5/17
PA28EOTI-
FS5/16
PATAG+
A
B
CFRZ+
PAASET+
PA28A-
PA28AM+
FS5/23
PA28GC+
FS5/19
PA28GC-
FS5/18
BAD0+
BAD1+
BAD2-
BAD3-
BAD4-
BAD5+
F29/17
F29/18
PA28AC-
ES2/36
S28/16(4)
28A
S28/65(53)
28C
PA28ESM+
FS5/20
PA28RSM+
FS5/21
PA28T+
FS5/13
S28/18(6)
28T
(CP1/66)
PAINT 28+
28B
S28/22(10)
F30/17
PAINT+
100K
P2/17
28R
PA28R-
PA28R+
FS5/22
S28/19(7)
28DI0
PA28DI0+
FS5/1
S28/44(32)
PA28DI1+
FS5/2
S28/69(57)
28DI2
PA28DI2+
FS5/3
S28/20(8)
28DI3
PA28DI3+
FS5/4
S28/45(33)
28DI4
PA28DI4+
FS5/5
28DI5
PA28DI5+
FS5/6
S28/24(12)
28HIA
28HI
-6VL3
S28/66(54)
28DI6
91
S28/17(5)
28DI7
S28/21(9)
28DI8
S28/47(35)
28J
S28/67(55)
28NI
R28
PA28NO+
FS5/14
S28/46(34)
28NO
PA28L+
FS5/15
S28/42(30)
28L
PA28D00+
FS5/7
S28/13(4)
28D00
PA28D01+
FS5/8
S28/38(26)
28D01
PA28D02+
FS5/9
S28/63(51)
28D02
PA28D03+
FS5/10
S28/14(2)
28D03
PA28D04+
FS5/11
S28/39(27)
28D04
PA28D05+
FS5/12
S28/64(52)
28D05
680
GA+
S28/43(31)
28G
GB+
680


PASETA-
PA29RS-
F36 1
PATAC+
A
F33 3
EP4 6
29A
CFRZ
F36 2
PA29OTO-
FS6/17
F36 3
B
F32 6
PAASET+
PA29RS-
PA29EOTI-
FS6/16
F20 2 709
(CP1/68)
PAINT 29+
29B
S29/22(10)
F30/18
PAINT +
100K
P2/18
S29/71(59)
29R
F22 3 709
F23 6
PA29R-
PA29R+
FS6/22
S29/19(7)
29DI0
F15 1 709
PA29DI0+
FS6/1
S29/44(32)
29DI1
F15 2 709
PA29DI1+
FS6/2
S29/69(57)
29DI2
F15 3 709
PA29DI2+
FS6/3
S29/20(8)
29DI3
F15 4 709
PA29DI3+
FS6/4
S29/45(33)
29DI4
F15 5 709
PA29DI4+
FS6/5
S29/70(58)
29DI5
F18 1 709
PA29DI5+
FS6/6
S29/24(12)
29HI
29HIA
-6VL3
F32 5
PA29AM+
FS6/23
F36 4
PA29A-
F36 5
PA29GC+
FS6/19
S29/16(4)
F21 5 708
29A
PA29GC-
FS6/18
F36 6
BAD0-
BAD1+
BAD2-
J
BAD3-
K
BAD 4-
F30/7
BAD 5+
F30/8
S29/65(53)
F21 6 708
29C
F23 12
A29AC
ES2/38
BAD0-
F32 4
PA29ESM+
FS6/20
BAD1+
A
BAD2-
F30/9
BAD3-
F30/10
BAD 4-
F30/11
BAD 5+
F30/2
PA29RSM+
FS6/21
PA29T+
FS6/13
F16 4 708
S29/18(6)
29T
PA29ND+
FS6/14
F16 5 708
S29/46(34)
29N
PA29L+
FS6/15
F16 6 708
S29/42(30)
29L
PA29D00+
FS6/7
F17 1 708
S29/13(1)
29D0
PA29D01+
FS6/8
F17 2 708
S29/38(26)
29D01
PA29D02+
FS6/9
F17 3 708
S29/63(51)
29D02
PA29D03+
FS6/10
F17 4 708
S29/14(2)
29D03
PA29D04+
FS6/11
F17 5 708
S29/39(27)
29D04
PA29D05+
FS6/12
F17 6 708
S29/64(52)
29D0
S29/66(54)
29DI6
91
S29/17(5)
29DI7
91
S29/21(9)
29DI8
91
S29/47(35)
29J
91
S29/67(55)
29NI
91
R29
680
S29/43(31)
GA+
GB+
29G
680



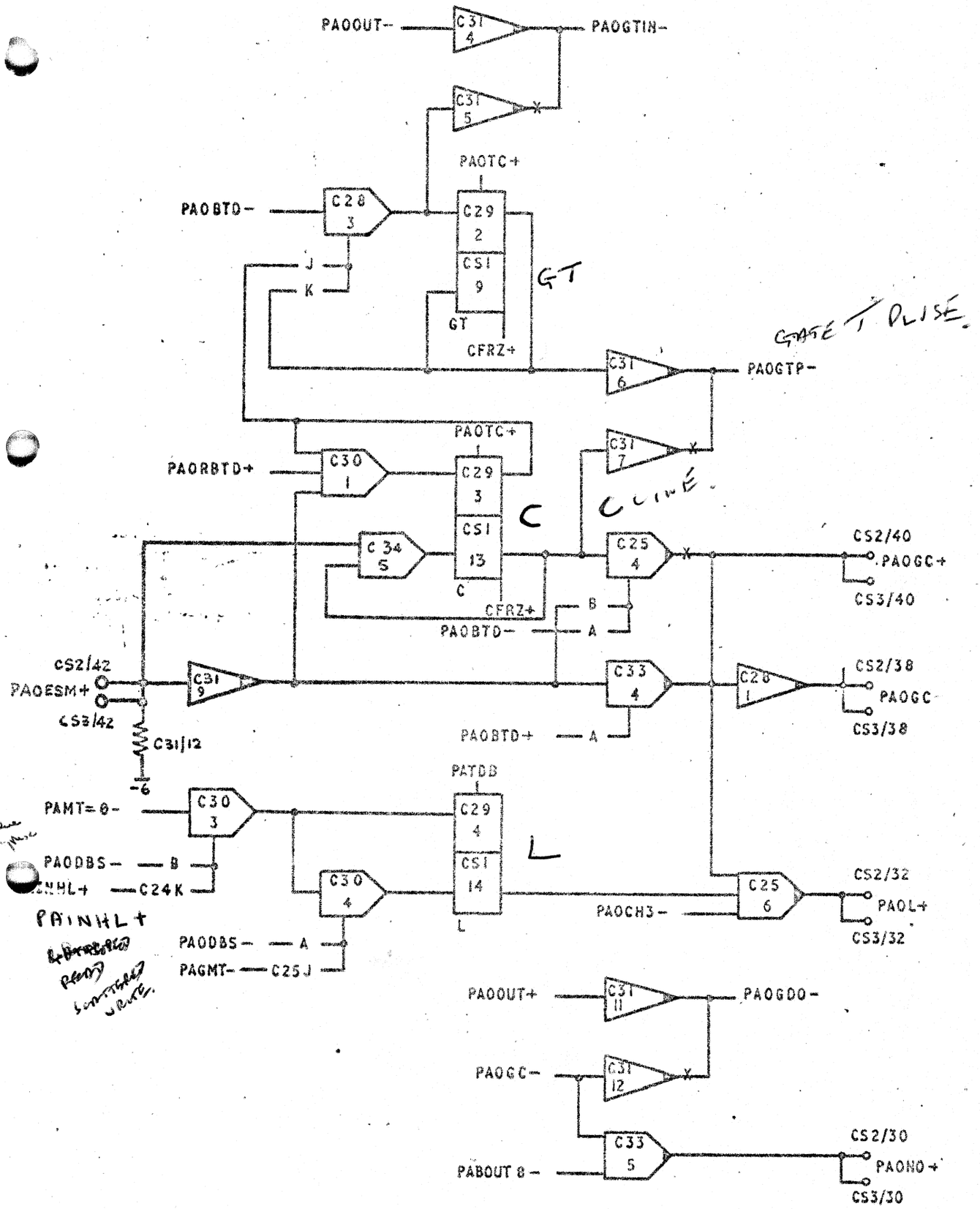
WGC07/2/6 — 6 X STANDARD INTERFACE

SUB	ISS	1	2	3											
ACW	0972	0992	1539	1559											
DATE	14/3/68	24/4/68	11/8/68	18/9/68											



WGC.Ø7/26

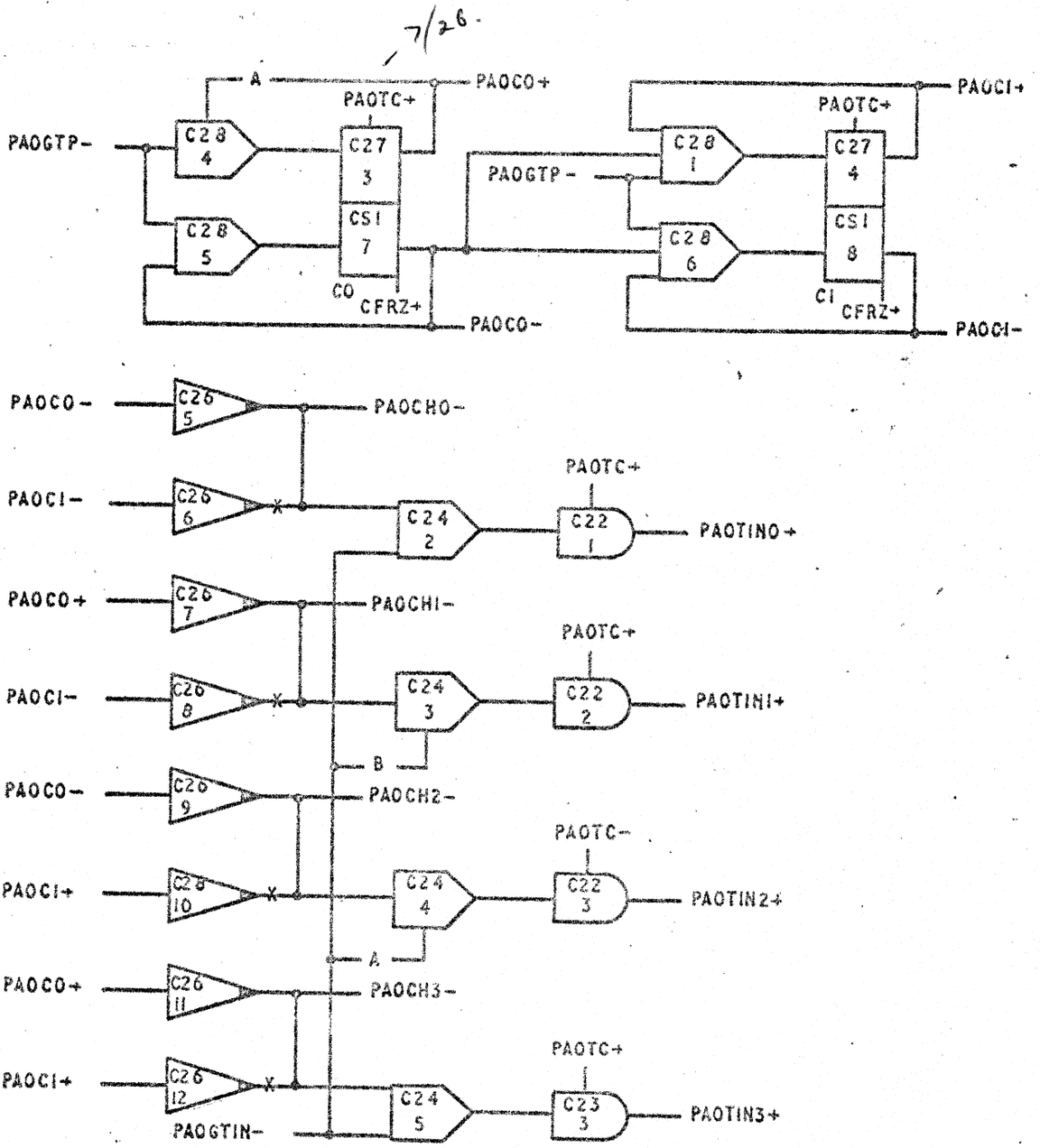
ISS	1	2	3	4										
0874	0931	0970	1516	1560										
31/10/67	2/1/68	4/3/68	30/4/68	19/9/68										



DATA BUFFER CONTROL Ø WGC07/27

SUB	ISS	1														
ACW	0874	0944														

CHAR COUNT.

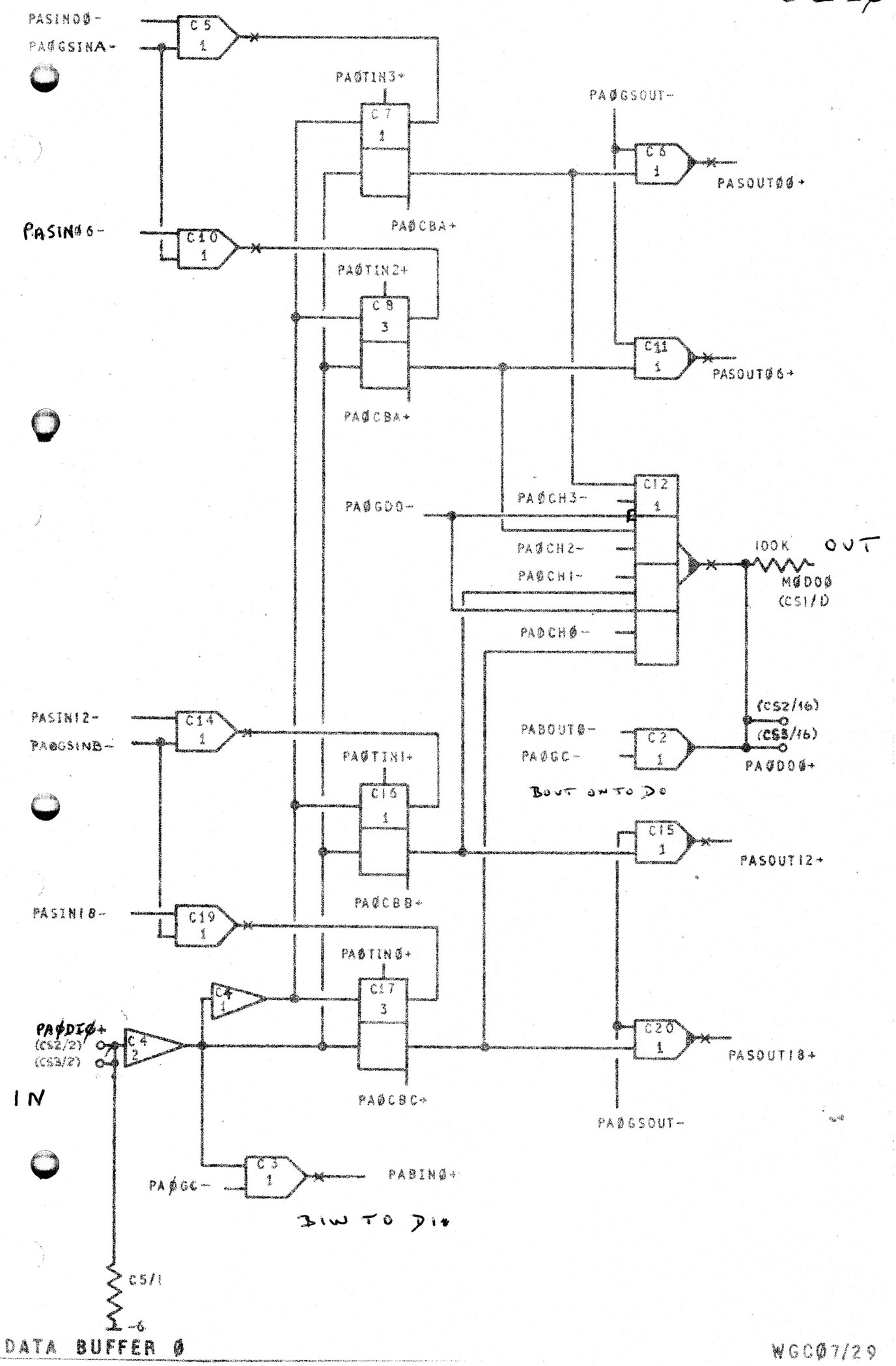


DATA BUFFER CONTROL Ø

WGC07/28

SUB	1SS
ACW	0874

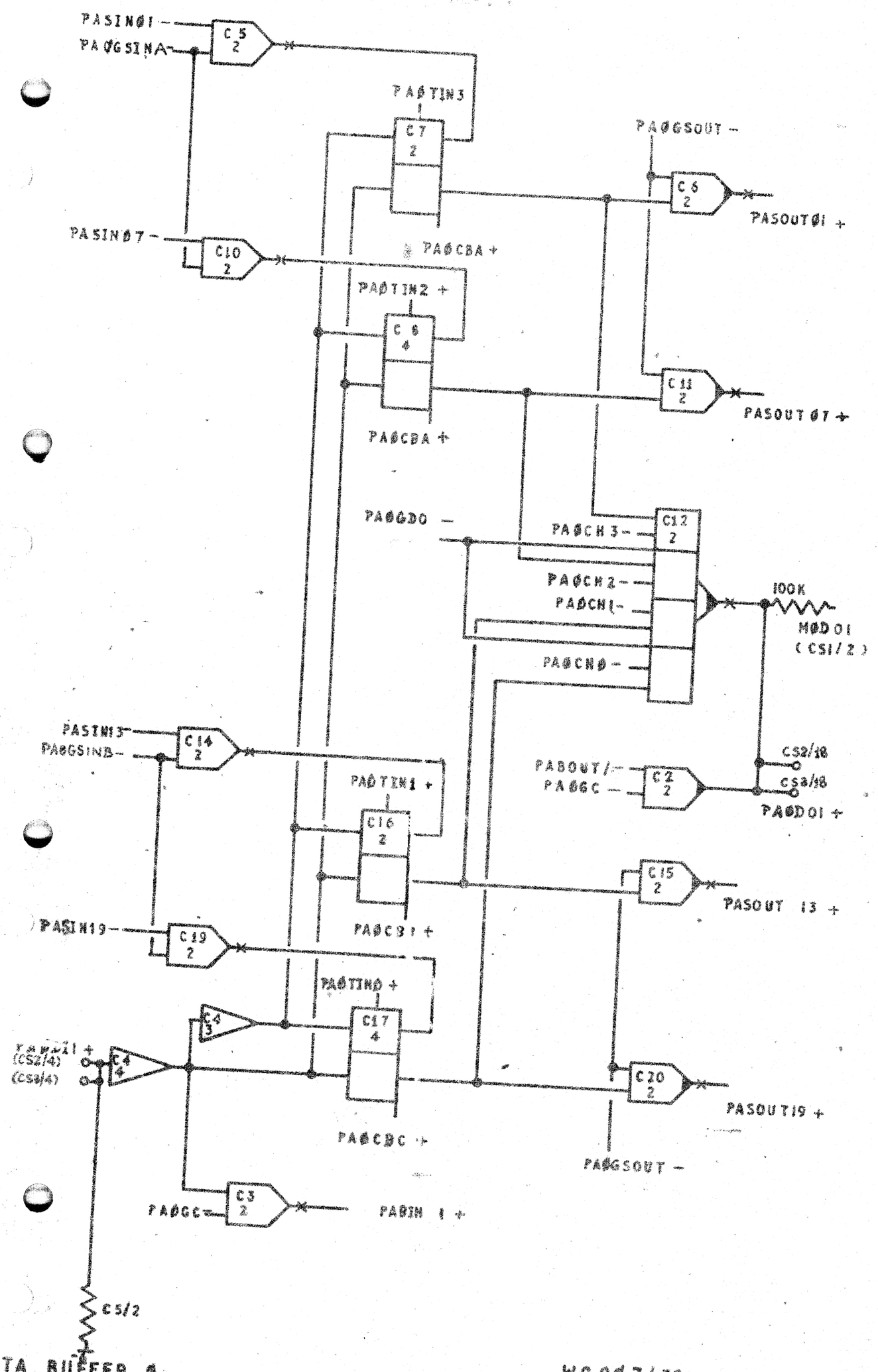
DATA BUFF Ø
BIT Ø OF CHARS 3, 2, 1, Ø
3210



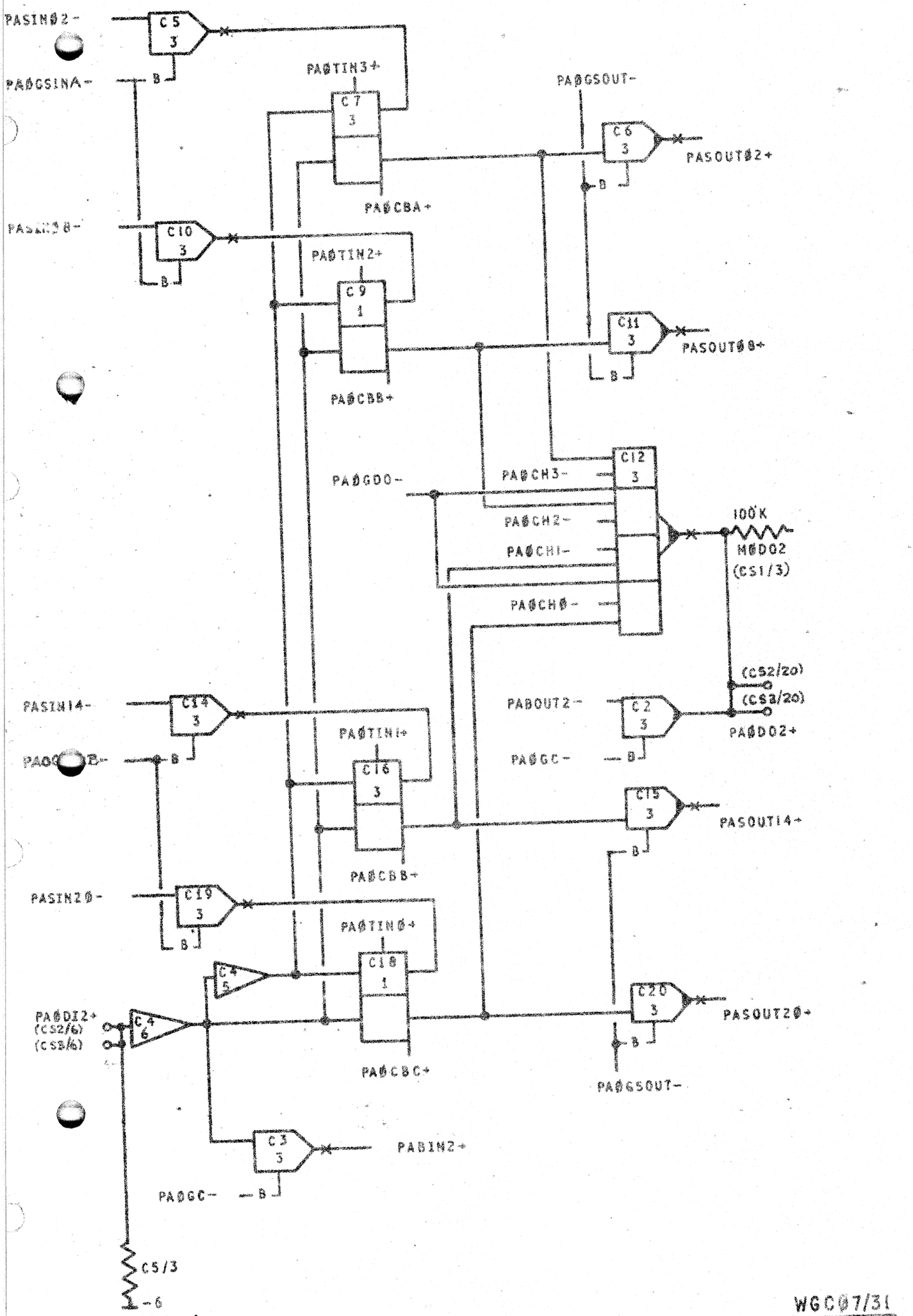
DATA BUFFER Ø

WGCØ7/29

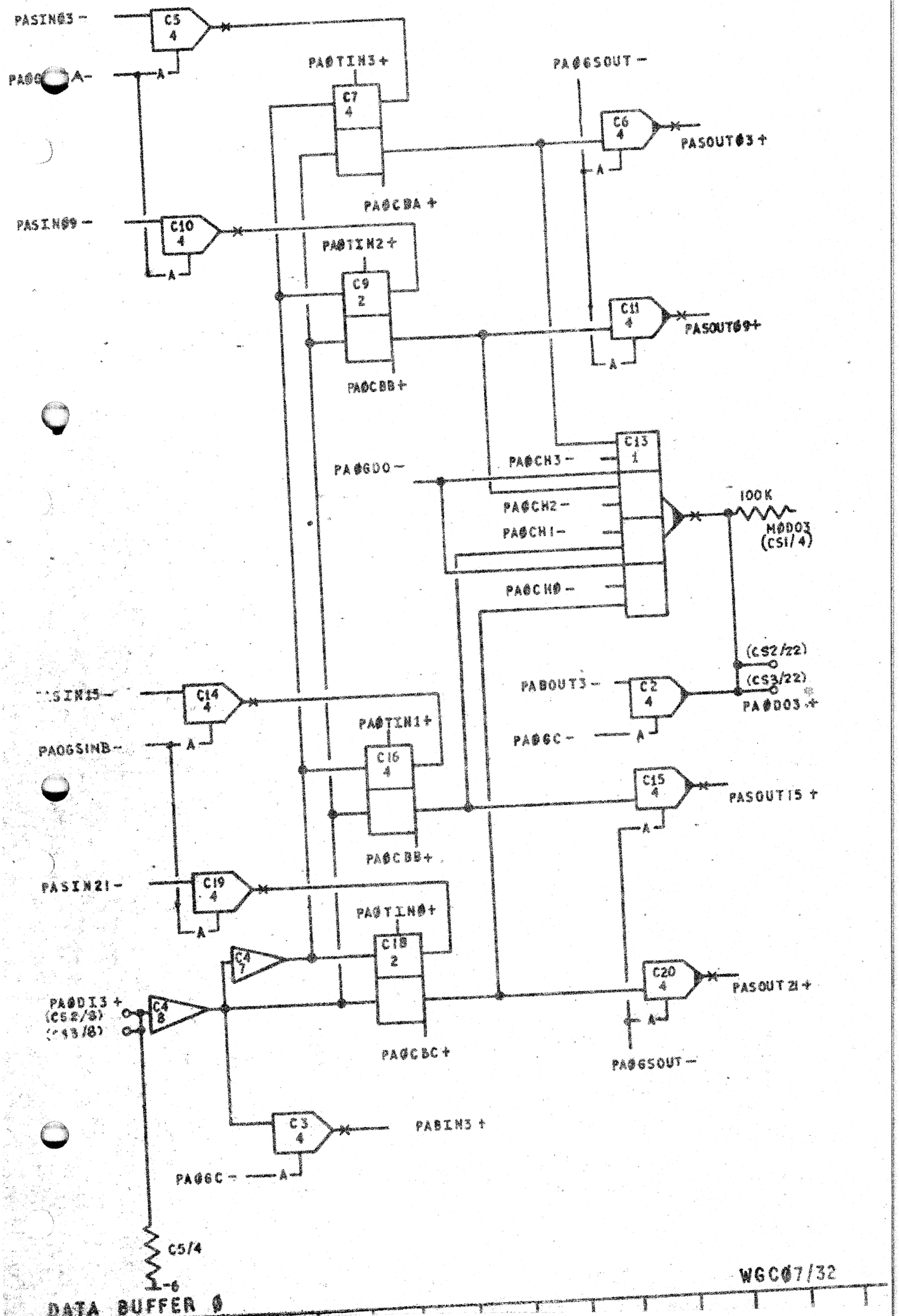
BIT 1


PASIN0I –
PA0GSINA –
C5 2
PA0TIN3
C7 2
PA0GSOUT –
C6 2
PASOUT0I +
PASIN07 –
C10 2
PA0CBA +
PA0TIN2 +
C8 4
C11 2
PASOUT07 +
PA0CBA +
PA0GDO –
C12 2
PA0CH3 –
PA0CH2 –
PA0CH1 –
PA0CH0 –
100K
M0D0I
(CSI/2)
PASIN13 –
PA0GSINB –
C14 2
PA0TIN1 +
C16 2
PABOUT/ –
PA0GC –
C2 2
CS2/18
CS3/18
PA0D0I +
C15 2
PASOUT 13 +
PASIN19 –
C19 2
PA0C81 +
PA0TIN0 +
C17 4
C4 3
C4 4
(CS2/4)
(CS3/4)
C20 2
PASOUT19 +
PA0CBC +
PA0GSOUT –
C3 2
PA0GC –
PA0IN 1 +
C5/2
DATA BUFFER 0
WG C0 7/30

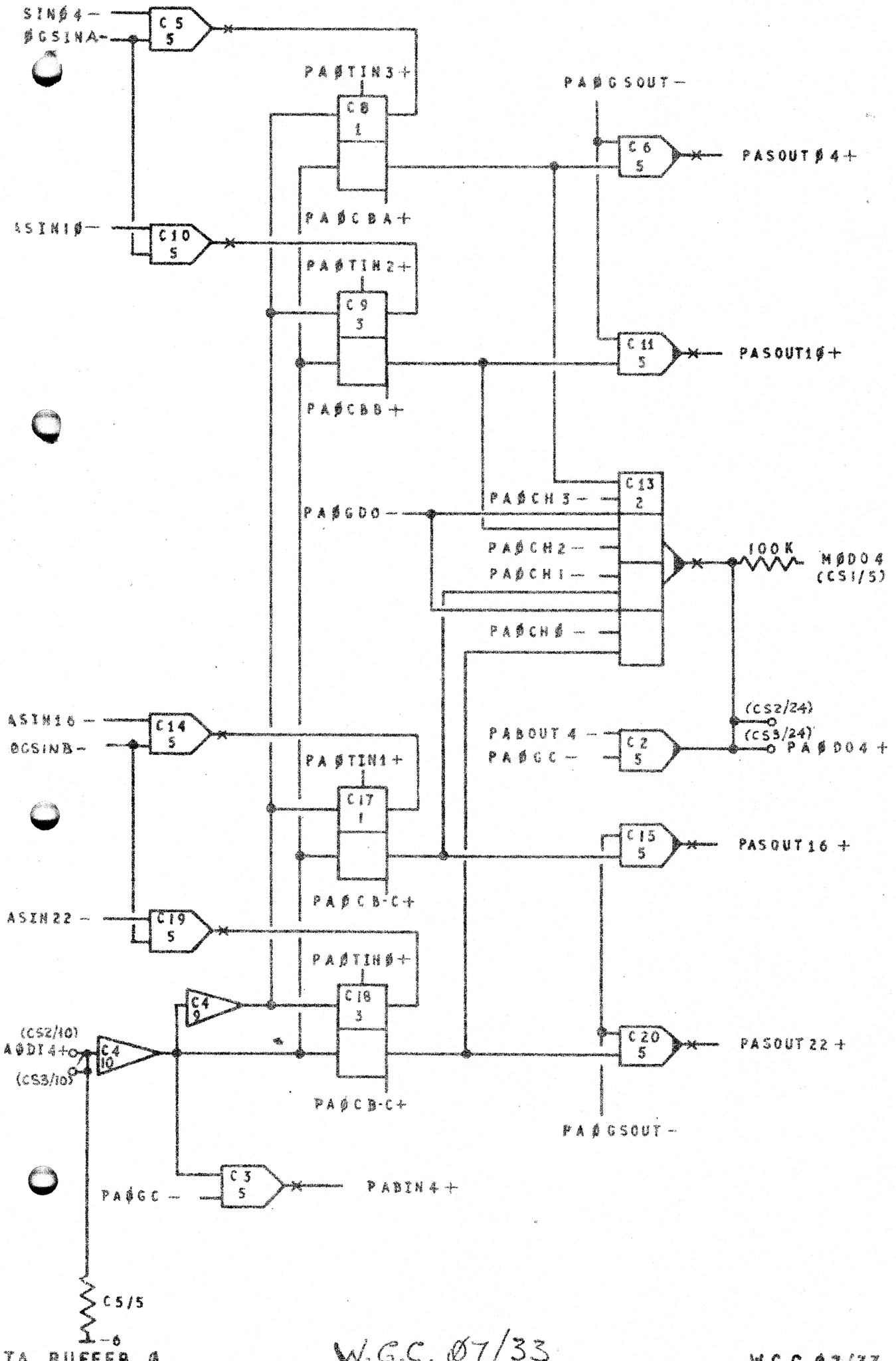
BIT 2


PASIN02-
C5 3
B
PA0GSINA-
PA0TIN3+
C7 3
PA0GSOUT-
C6 3
PASOUT02+
B
PA0CBA+
PASIN10-
C10 3
B
PA0TIN2+
C9 1
C11 3
PASOUT00+
B
PA0CBB+
PA0GD0-
C12 3
PA0CH3-
PA0CH2-
PA0CH1-
PA0CH0-
100K
M0D02
(CS1/3)
(CS2/20)
(CS3/20)
PA0D02+
PASIN14-
C14 3
B
PA0TIN1+
PA0BOUT2-
C2 3
PA0GC-
B
C16 3
C15 3
PASOUT14+
B
PA0CBB+
PASIN20-
C19 3
B
PA0TIN0+
C4 5
C18 1
C20 3
PASOUT20+
PA0DI2+
(CS2/6)
(CS3/6)
C4 6
B
PA0CBC+
PA0GSOUT-
C3 3
PABIN2+
PA0GC-
B
CS/3
-6
DATA BUFFER 0
WGC07/31

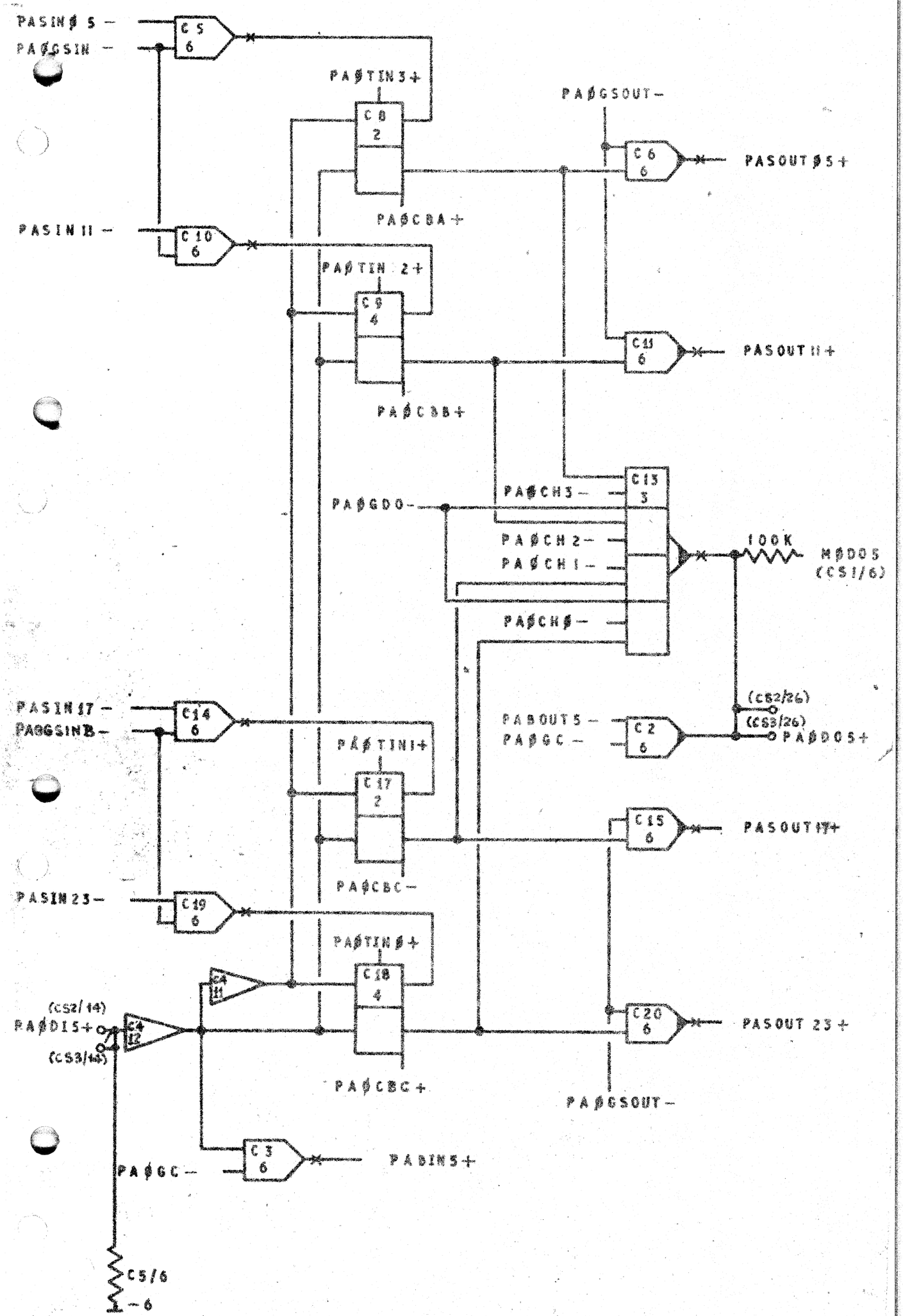
BIT 3


PASIN03 -
C5 4
PA00 A-
A
PA0TIN3+
C7 4
PA0CBA +
PA06SOUT -
C6 4
PASOUT03 +
A
PASIN09 -
C10 4
A
PA0TIN2+
C9 2
PA0CBB+
C11 4
PASOUT09+
A
PA0GDO -
C13 1
PA0CH3 -
PA0CH2 -
PA0CH1 -
PA0CH0 -
100K
M0D03 (CS1/4)
(CS2/22)
(CS3/22)
PA0D03 +
PABOUT3 -
C2 4
PA0GC -
A
"SIN15 -
C14 4
PA0GSINB -
A
PA0TIN1+
C16 4
PA0CBB+
C15 4
PASOUT15 +
A
PASIN21 -
C19 4
A
PA0TIN0+
C18 2
C4 7
C4 8
PA0DI3 +
(CS2/8)
(CS3/8)
C20 4
PASOUT21 +
A
PA0CBC+
PA06SOUT -
C3 4
PABIN3 +
PA0GC - A
C5/4
-6
DATA BUFFER 0
WGC07/32

BIT 4


SINØ4 –
ØGSINA–
C5 5
PAØTIN3+
C0 1
PAØGSOUT –
C6 5
PASOUTØ4+
PAØCBA+
ASINIØ–
C10 5
PAØTIN2+
C9 5
C11 5
PASOUT1Ø+
PAØCBB+
C13 2
PAØCH3 –
PAØGDO –
PAØCH2 –
PAØCH1 –
100K
MØDO4
(CS1/5)
PAØCHØ –
(CS2/24)
(CS3/24)
PAØDO4+
ASIN16 –
C14 5
ØGSINB–
PABOUT4 –
PAØGC –
C2 5
PAØTIN1+
C17 1
C15 5
PASOUT16+
PAØCB-C+
ASIN22 –
C19 5
PAØTINØ+
C4 9
C18 3
(CS2/10)
AØDI4+
(CS3/10)
C4 10
C20 5
PASOUT22+
PAØCB-C+
PAØGSOUT –
C3 5
PAØGC –
PABIN4+
C5/5
–6
TA BUFFER Ø
W.G.C. Ø7/33
W.G.C. Ø7/33.

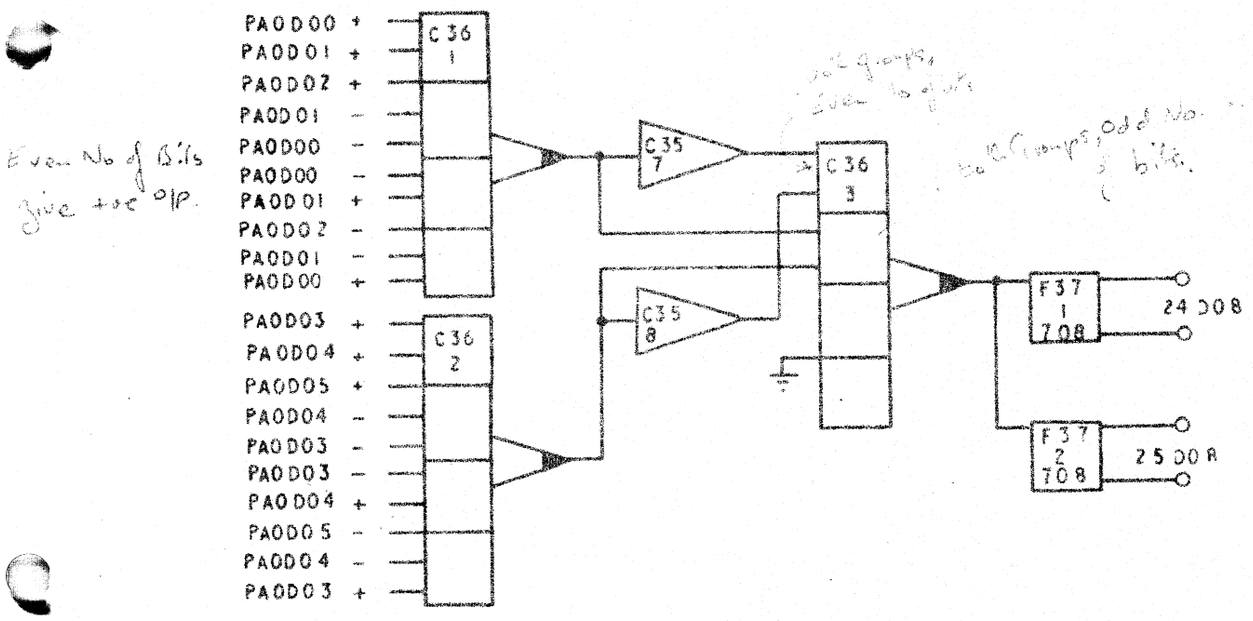
BIT 5

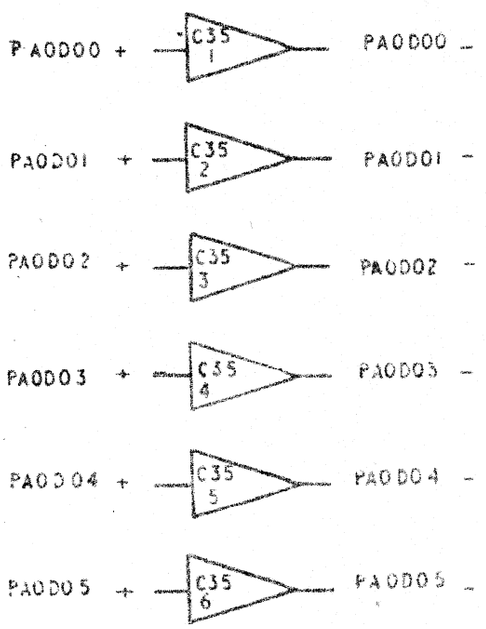


DATA BUFFER ∅

M.G.C.07/34

PARITY FOR ORION II LINK





Re WGC 07/27 PA0GD0 – made as shown below:-