Contents

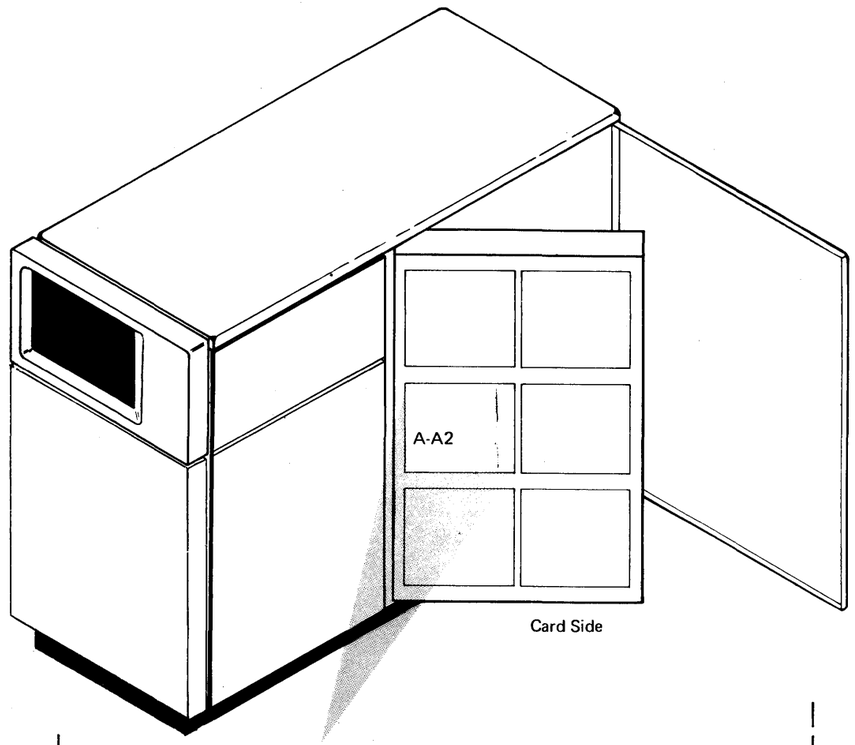
33FD/53FD/72MD Diskette Drive and Attachment (Level 2)

INTRODUCTION

The diskette drive and diskette drive attachment are located inside the 5340 System Unit. System/34 uses a 33FD diskette drive, a 53FD diskette drive, or a 72MD diskette magazine drive. The diskette drive attachment card and the data separator card are located on the A-A2 board. Each diskette drive also contains a file control card. The control storage program and the diskette drive attachment with the file control card control the diskette drive. The diskette drive can read a data track, write on a data track, or seek to a data track of a diskette. The data separator separates serialized data pulses from clock pulses as they are read from the diskette. The data is moved between the attachment and main or control storage in 2-byte bursts by cycle steal.

The 33FD and 53FD diskette drives have a continuously turning shaft that turns the diskette. A solenoid-loaded data head (33FD/53FD) or cam-loaded data heads (72MD) are moved to the correct data track by a stepper motor. A data head can then read or write the data track.

The 33FD diskette drive records data using frequency modulation. The 53FD and 72MD diskette drives record data using either frequency modulation or modified frequency modulation.

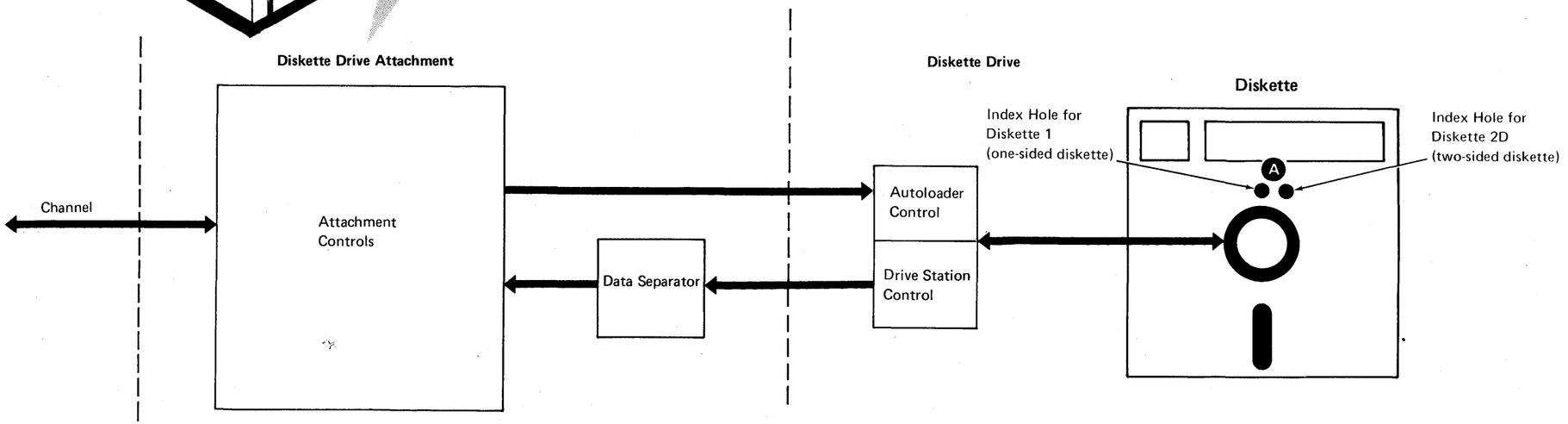


The System/34 uses two types of diskettes: Diskette 1 and Diskette 2D. One side of Diskette 1 (33FD, 53FD, or 72MD) and both sides of Diskette 2D (53FD or 72MD) are used for recording. The two types of diskettes are identified by the physical location of the index hole (A). When a Diskette 1 is inserted in a 53FD or 72MD diskette drive, the circuits that sense the index hole prevent the use of the second side. A Diskette 2D cannot be used in a 33FD diskette drive. There is 1 label cylinder, 74 primary data cylinders, and 2 alternative cylinders per diskette. Commands from the control storage program start the diskette selection and the read, write, and seek operations in addition to performing various control functions. An index hole in the diskette references the start of the first sector on the cylinder that the data head is on.

The 72MD is a 53FD type diskette drive with the diskette turning at double speed. The 72MD also has a diskette autoloader. The diskettes can be contained in either of two 10-pack magazines or in three manual insertion slots. All diskettes used for a specific operation must be the same type and have the same format and may be placed in either magazines or I/O slots, but not both. The 72MD operates in two distinct modes: autoloader mode and diskette drive mode.

Autoloader mode permits the selection of a diskette, the loading of this diskette into the drive, plus the unloading of that diskette and returning it to its correct slot. The autoloader includes a carriage bed and a picker mechanism; both are driven by stepper motors. The carriage bed contains two magazines (each magazine can contain 10 diskettes) and three I/O slots for insertion and removal of single diskettes by the operator. The carriage bed is moved at right angles to the diskette drive by the carriage bed stepper motor until the selected diskette is aligned with the picker mechanism. The selected diskette is moved from the carriage bed to the drive and returned to the carriage bed by means of the picker and the picker stepper motor.

Diskette drive mode allows the seek, read, and write functions, which are similar to functions of other diskette drives. The 72MD diskette drive can read and write both one-sided and two-sided diskettes.



33FD Diskette Drive

33FD Diskette Drive Assembly

When the cover (A) of the 33FD diskette drive is open, the diskette can be inserted or removed. When the cover is closed, the spring-loaded collet (B) centers and holds the diskette to the drive hub.

The data head load actuator assembly (C) is a magnet and an armature. During a read or write operation, the magnet is active and makes the pressure pad arm push the diskette against the data head. At the same time, the armature puts a slight pressure on the diskette jacket, which cleans the diskette. When not reading or writing, the data head load actuator is not active and holds the pressure pad assembly away from the diskette to decrease wear on the diskette surface and the data head.

When the cover is closed, the continuous light from the light-emitting diode (D) points toward the phototransistor. Every time the diskette turns, the index hole in the diskette lets the light from the light-emitting diode reach the phototransistor. The phototransistor sends index pulses to the diskette drive attachment.

The preload spring (E) pushes the leadscrew to ensure that the data head is aligned with the diskette.

The upper-limit stop (F) stops the data head from going past track 76. The lower-limit stop (G) stops the data head from going past track 00.

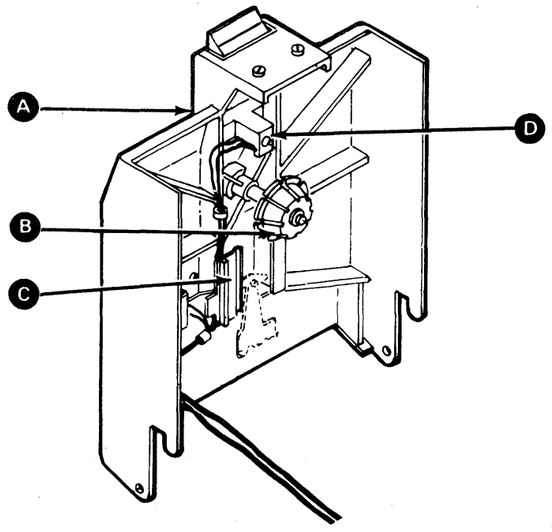
The leadscrew nut and spring (H) push against the data head and carriage assembly to ensure that the data head is aligned with the diskette.

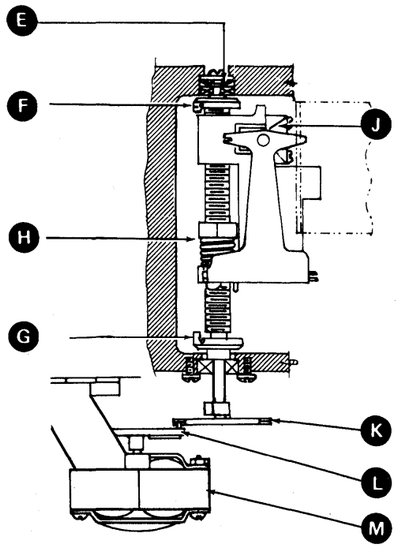
The data head (J) can either read data from the diskette or erase and write data on the diskette.

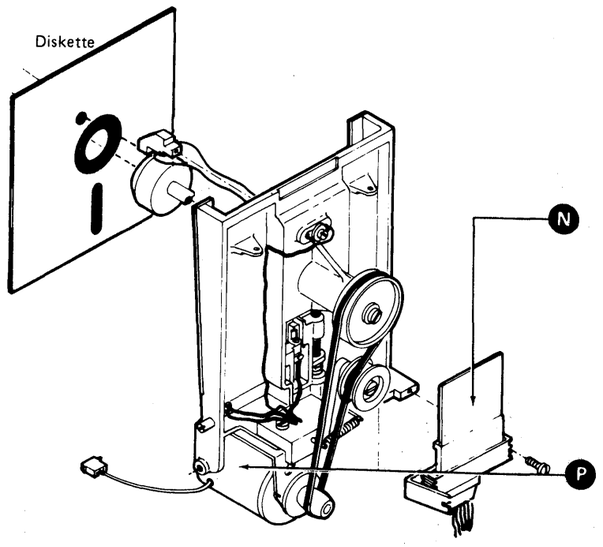
The stepper motor wheel (L) is on the end of the stepper motor shaft. The stepper motor (M) turns in steps of 90 degrees in either direction under the control of access pulses. The stepper motor wheel engages the leadscrew wheel (K). When the stepper motor wheel turns 90 degrees, it turns the leadscrew wheel 90 degrees. The data head carriage assembly then moves up or down one track on the diskette.

The circuits for the stepper motor, the data head load actuator, and the data head are on the file control card (N). The amplifier circuits for the phototransistor and data head are also on the file control card. The file control card circuits and test pins face out.

The drive motor (P) turns the diskette at a speed of 360 ± 2.5% revolutions per minute with the head loaded.







33FD Operating Sequences

Diskette Operation

The following events make the diskette operational:

1. When system power is on, the diskette drive motor turns continuously.

2. When the diskette is inserted in the diskette drive and the cover assembly is closed, the collet assembly (B) clamps the diskette to the drive hub (A). The diskette then starts turning.

3. When the diskette is up to speed and the heads are loaded, index pulses (G) are sensed once every 166.7 (+4.27, -4.06) milliseconds. The attachment uses these pulses to ensure that the diskette is turning at the correct speed, thereby sensing the diskette-ready condition.

Seek Operation

To move the data head to the desired track:

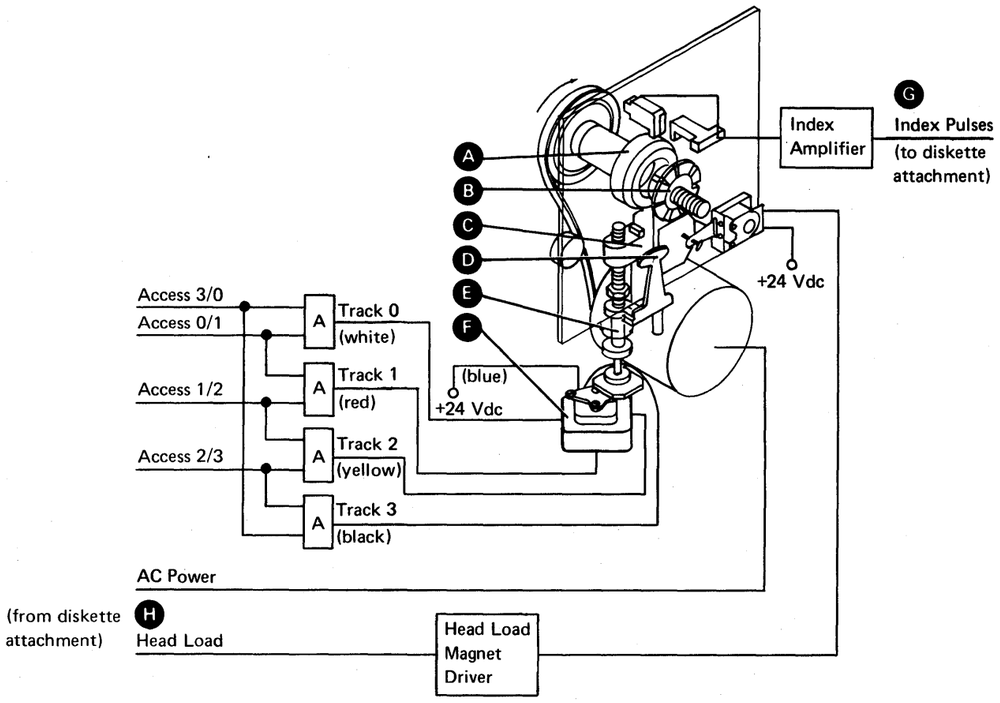
1. The control processor issues a control command to start the seek. The 'diskette ready' line is activated if the diskette speed is OK. (See Note 1.)

2. Two access lines are activated at the same time for a minimum of 57.4 milliseconds to seek one track (L). (A seek does not change the data head condition.) A 98.4-millisecond delay is added after the last seek to allow for head settling.

   Example: The chart shows the data head moving from track 2 to track 6. The access lines are activated for a minimum of 57.4 milliseconds to move the data head across each track, and 98.4 milliseconds (M) to allow the data head to settle on the last track.

3. For each access operation, the stepper motor (F) turns the leadscrew (E) 90 degrees clockwise or counterclockwise. This moves the data head one track position. When the leadscrew is turned clockwise (looking into the unit from the front of the machine), the carriage moves out (toward the front). (See Note 2.)

Notes:
1. Before the first seek is performed, the control processor issues a recalibrate operation (a minimum of 76 seeks to cylinder 0).
2. At the end of the seek operation, no stepper motor lines remain active. This is different from the 53FD and 72MD drives.



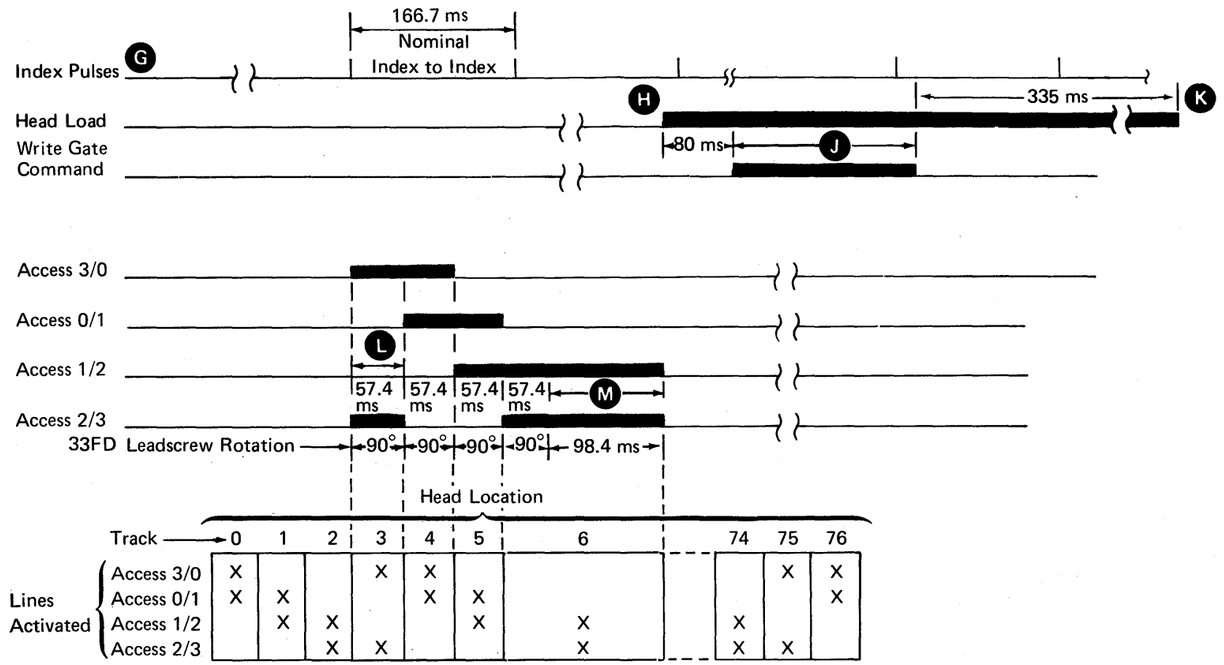
Read or Write Operation

To load the data head and write on or read from the diskette:

1. The control storage program issues a data head load command (H) before a read or write operation. This causes the pressure pad (D) to push the diskette against the data head (C). Data is valid after 80 milliseconds (time for the data head to load).

2. The control storage program issues a read or write command (J).

3. The control storage program issues a command to unload the head (K) 335 milliseconds after a seek, read, or write operation is complete (if no other operation is issued during the 335 milliseconds). This decreases wear on the diskette and the data head. The 335-millisecond delay occurs because during normal diskette use, the next diskette operation usually starts during the 335-millisecond delay. Therefore, the data head does not have to be loaded before each operation.



53FD Diskette Drive

53FD Diskette Drive Assembly

When the cover (A) of the diskette drive is open, the diskette can be inserted or removed. When the cover is closed, the collet (B) centers and clamps the diskette to the drive hub.

The belt (G), the drive motor (E), the drive pulley (J), and the idler assembly (H) turn the diskette at 360 ± 2.5% revolutions per minute with the heads loaded.

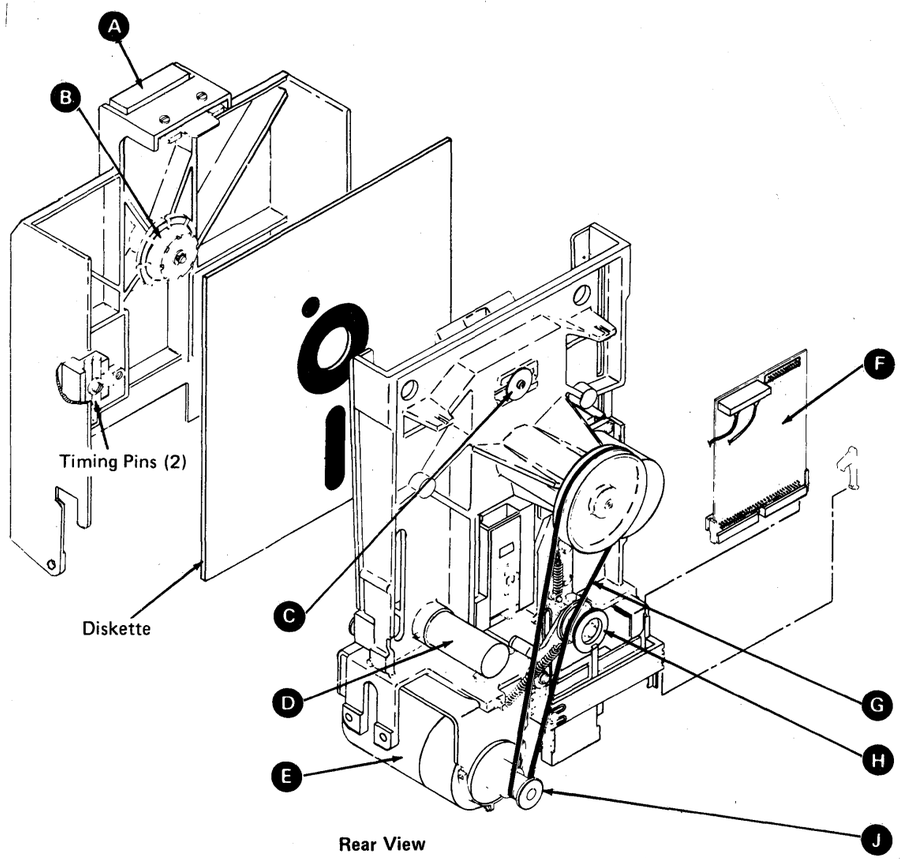
The stepper motor (K) turns in either direction under control of access pulses. The stepper motor pulley (R), the stepper motor pulley clamp (S), the stepper drive band (Q), and the stepper idler assembly (L) move the data heads across the diskette surface.

Two data heads are on a common carriage assembly (N) and move under control of the stepper motor. The data heads read data from and write new data on a diskette.

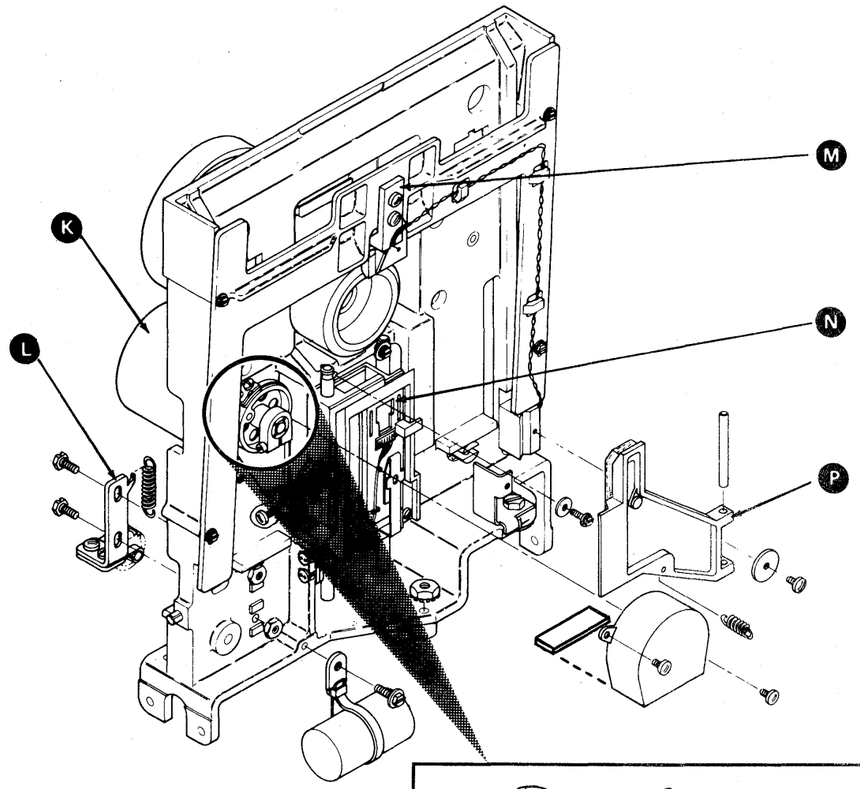
The data head load solenoid (D) causes the bail (P) to load the data heads.

The two light-emitting diodes (M) and the two phototransistors (C) work together to sense the diskette index hole and identify the type of diskette inserted (Diskette 1 or Diskette 2D).

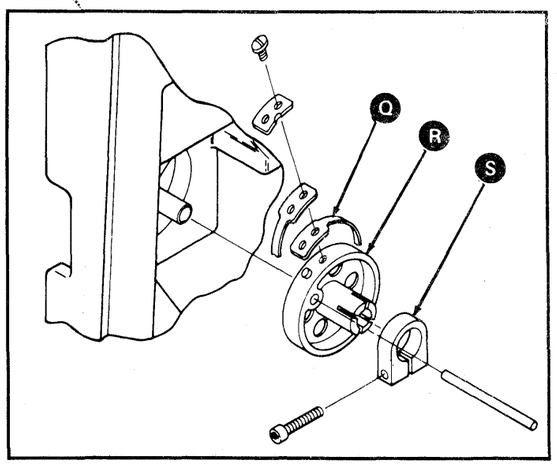
The diskette drive control card (F) has the drive circuits for the stepper motor, the data head load solenoid, and the write and erase functions. The card also has the amplifiers for the data heads and the light-emitting diode and phototransistor circuits.



Rear View



Front View



53FD Operating Sequences

Diskette Operation

The following events make the diskette operational:

1. When system power is turned on, the diskette drive motor starts turning (A).

2. When the diskette is inserted in the diskette drive and the cover assembly is closed, the collet (B) clamps the diskette to the drive hub. The diskette then starts turning.

3. When the diskette is up to speed and the heads are loaded, index pulses (G) are sensed once every 166.7 (+4.27, -4.06) milliseconds. The attachment uses the index pulses to ensure that the diskette is turning at the correct speed, thereby sensing the diskette-ready condition.

Seek Operation

To move the data heads to the desired cylinder:

1. The control processor issues a control command to start the seek. The 'diskette ready' line is activated if the diskette speed is OK. Seeking is done by activating the two access lines to the stepper motor (F). This moves the head/carriage assembly (E) in (toward the hub) or out (away from the hub). Activating two sequential access lines turns the stepper motor a distance equal to 1 cylinder (L). (See note.)

2. Two access lines are activated for a minimum of 8.2 milliseconds to seek one track (L). A 32.8-millisecond delay is added after the last seek to allow for head settling.

   Example: The chart shows the data heads moving from track 2 to track 6. The access lines are activated for a minimum of 8.2 milliseconds to move the data heads across each track, and 32.8 milliseconds (M) to allow the data heads to settle on the last track.

3. At the end of a seek operation, two access lines remain active. The two access lines keep the stepper motor stopped to keep the data heads on track.

Note: Before the first seek is performed, the control processor issues a recalibrate operation (76 seeks to cylinder 0).

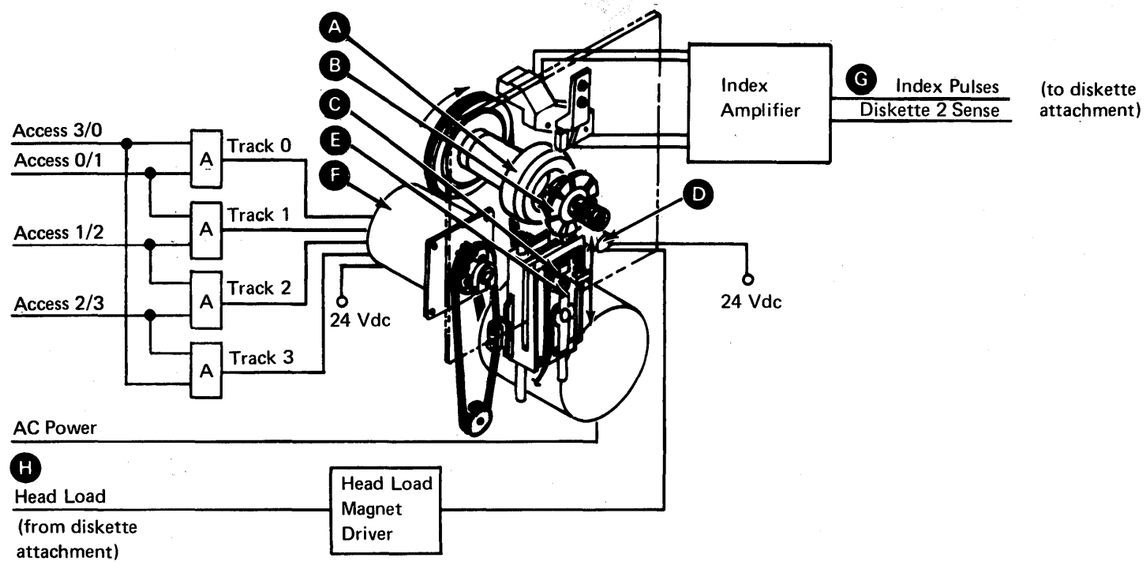
Read or Write Operation

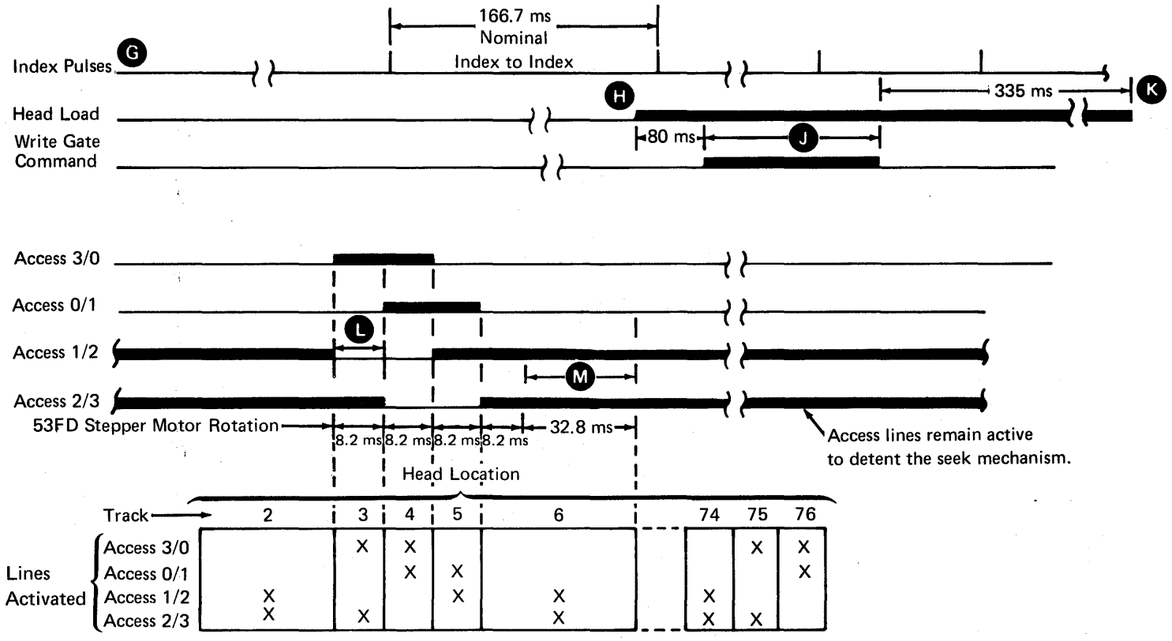
To load the data heads and write on or read from the diskette:

1. The control storage program issues a data head load command (H) before a read or write operation. This activates the data head load solenoid (D), which pushes the data heads (C) against the diskette. Data is valid after 80 milliseconds (time for the data heads to load).

2. The control storage program issues a read or write command (J).

3. The control storage program issues a command to unload the heads (K) 335 milliseconds after a seek, read, or write operation is complete (if no other operation is issued during the 335 milliseconds). This decreases wear on the diskette and the data heads. The 335-millisecond delay occurs because during normal diskette use, the next diskette operation usually starts during the 335-millisecond delay. Therefore, the data heads do not have to be loaded before each operation.





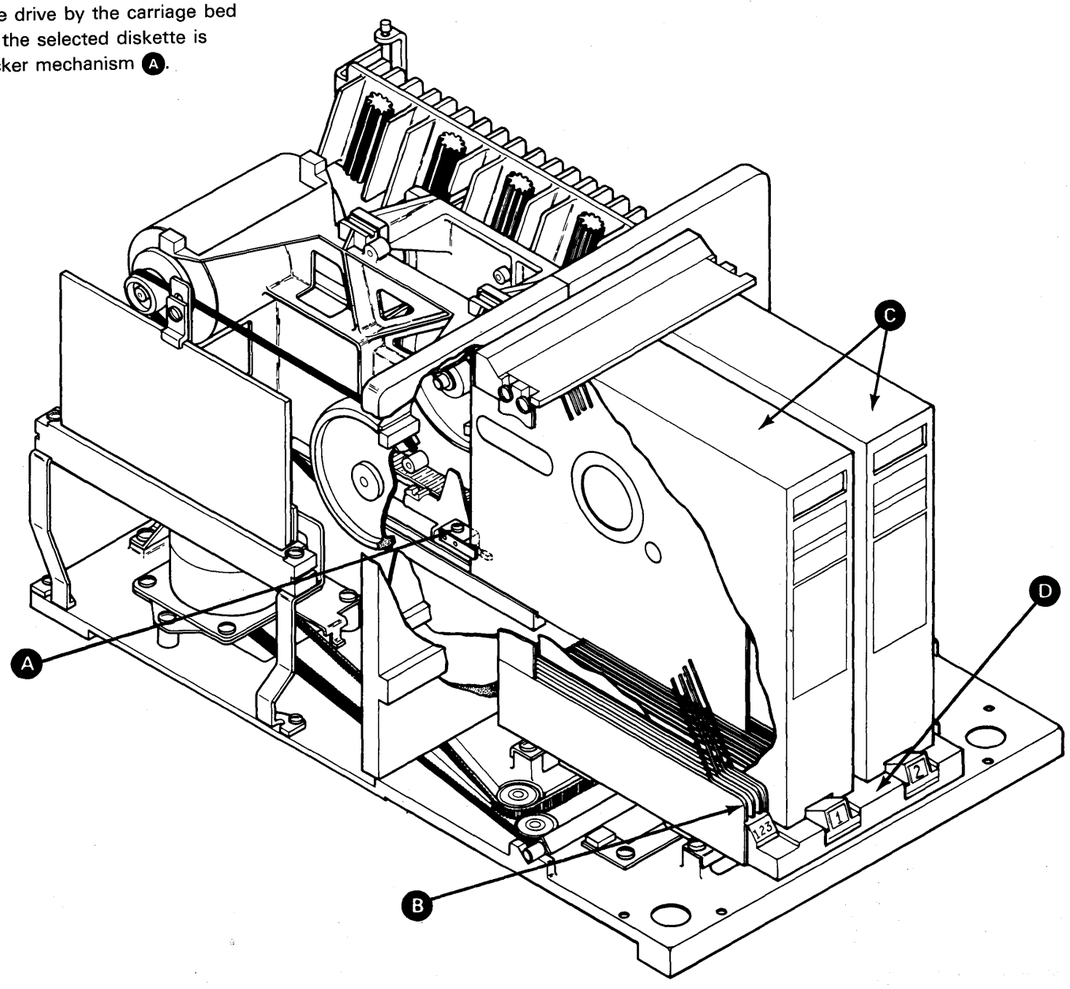
72MD Diskette Magazine Drive

Autoloader Units

The autoloader units include a carriage bed and a picker mechanism; both are driven by stepper motors.

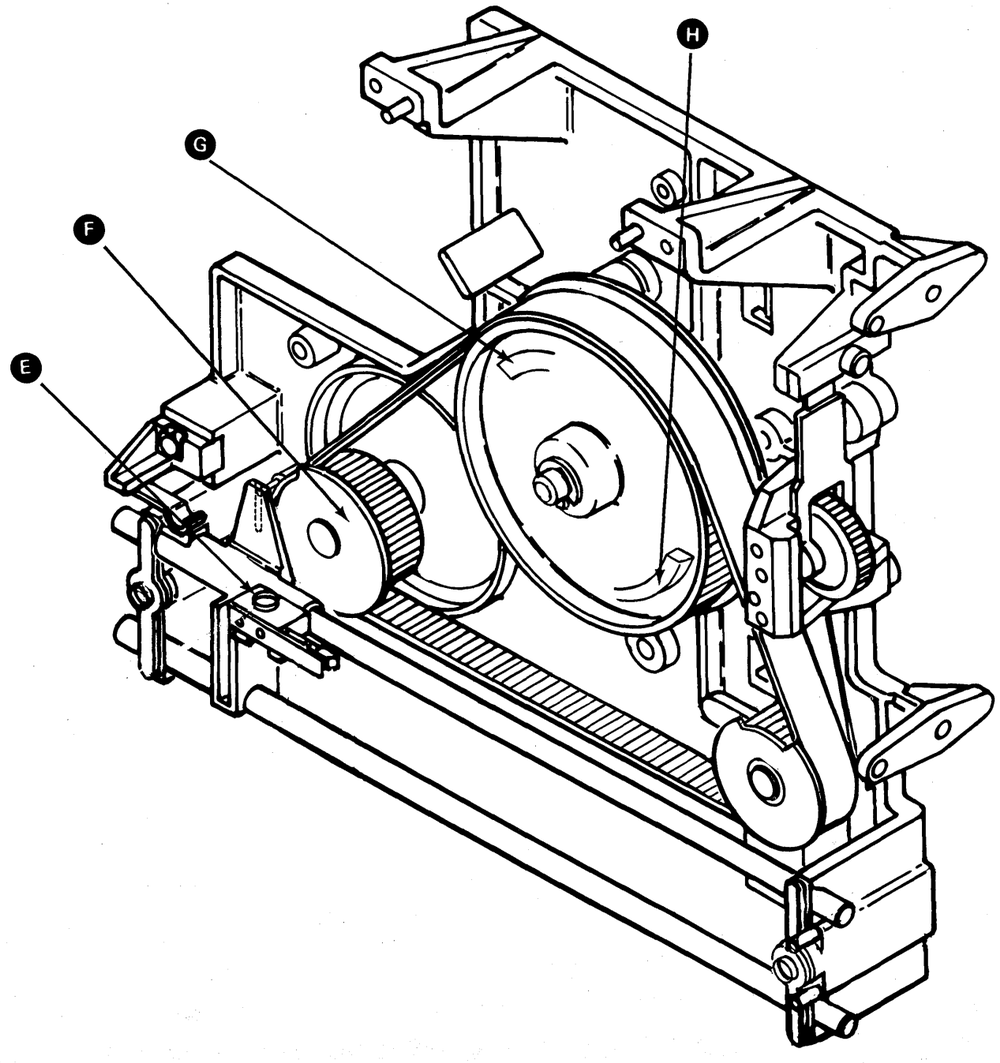
Carriage Bed

The carriage bed holds two magazines Ⓒ and has three I/O slots Ⓑ. The I/O slots are available for the operator to insert or remove single diskettes. The carriage bed Ⓓ is moved at 90 degrees to the drive by the carriage bed stepper motor until the selected diskette is aligned with the picker mechanism Ⓐ.



Picker Mechanism

The picker mechanism moves the selected diskette from the carriage bed to the drive and back to the bed again with the picker arm Ⓔ driven by the picker/cam stepper motor Ⓕ The picker/cam stepper motor also controls a cam Ⓗ to load a collet, which centers and clamps the diskette to the drive hub. Additional rotation of the picker/cam stepper motor causes a cam Ⓖ to load the data heads.

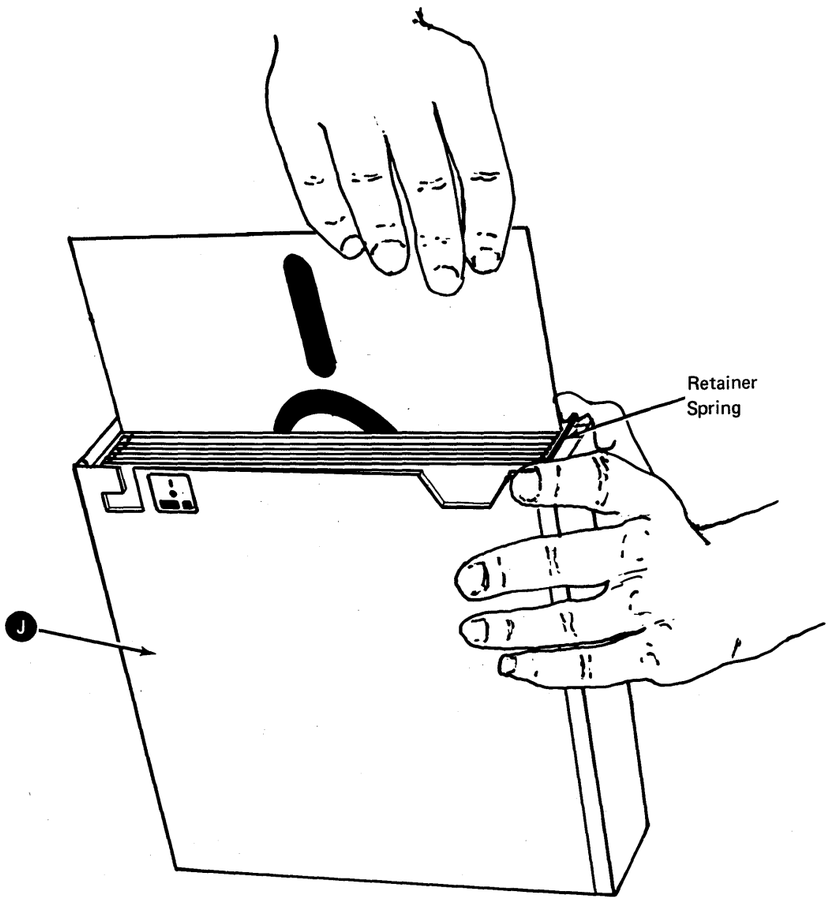


Heat Sink and Driver Assembly

This assembly contains the power drivers and associated predriver logic for the picker and carriage bed stepper motors.

Magazine

The magazine (J) is an autoloader accessory. It has 10 slots and can hold up to 10 diskettes.



Diskette Drive Components

Diskette Drive Mechanism

The drive hub (A) is belt driven by an AC motor (B)

Data Head and Carriage Assembly

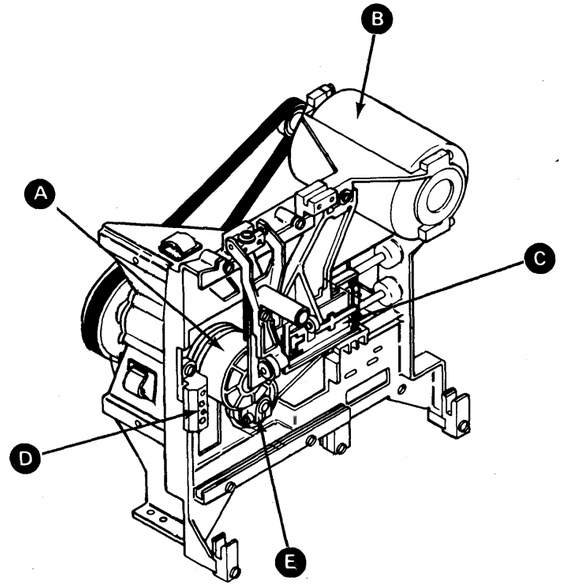
Two data heads are attached to a common carriage assembly (C). The data heads read data from a diskette or write data on a diskette.

Data Head and Carriage Access Mechanism

A DC stepper motor (E) moves the data heads from cylinder to cylinder in either direction, 1 cylinder per step.

Diskette Detection Mechanism

The two light-emitting diodes and two phototransistors (D) work together to sense the diskette index hole and to identify the type of diskette inserted (Diskette 1 or Diskette 2D).



Logic Cards

File Control Card

This card is located in the diskette drive and is under control of the diskette attachment card located on the A-A2 board. The file control card controls the seek, read, write, index detection, and autoloader functions.

Variable Frequency Oscillator (VFO) Card

The function of this card (located on the A-A2 board) is to separate data. File data from the diskette drive must be separated into clock and data pulses before being passed on to the attachment card.

Diskette Attachment Card

This card (located on the A-A2 board), together with the control storage program, controls all diskette magazine drive functions.

72MD Diskette Magazine Drive (continued)

Stepper Motors

The stepper motors turn in steps of 90 degrees in either direction under the control of access pulses. The three stepper motors used in the 72MD diskette magazine drive are the picker/cam drive motor, the carriage bed drive motor, and the head/carriage drive motor.

Picker/Cam Drive Motor

The picker/cam drive motor moves the picker to its maximum extension. This maximum extension position is known as picker home or picker orient. All other picker positions reference from picker orient.

Position	Number of 90° Stepper Motor Steps from Picker Orient
Picker Rest	36[1]
Diskette In	276[2]
Collet Loaded	392
Heads Unloaded	412
Heads Loaded	452

The Picker Rest position of the picker mechanism is used during carriage bed motion. The Diskette In position[2] is used when the diskette is in the drive. The Collet Loaded position is used when the collet clamps the diskette to the turning hub. The Heads Unloaded position is used when the diskette is turning but the heads are not on the surface of the diskette. The Heads Loaded position is used when the heads are on the diskette surface.

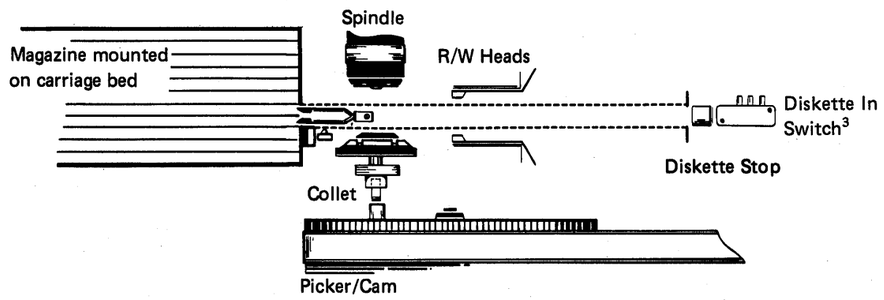
The access times for the picker/cam drive motor are as follows:

Acceleration Time	2.5 ms to 3.3 ms
Constant Velocity	2 ms
Deceleration Time	4 ms
Settling Time	35 ms

[1] Picker rest is 20 steps from picker orient on machines with the new style picker.
[2] This position is not used on machines with the new style picker.
[3] The Diskette In switch is not present on machines with the new style picker.

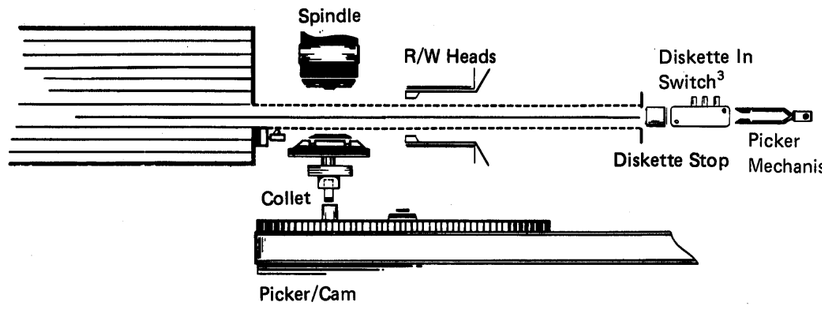
(36 steps from orient)[1]

Picker Rest



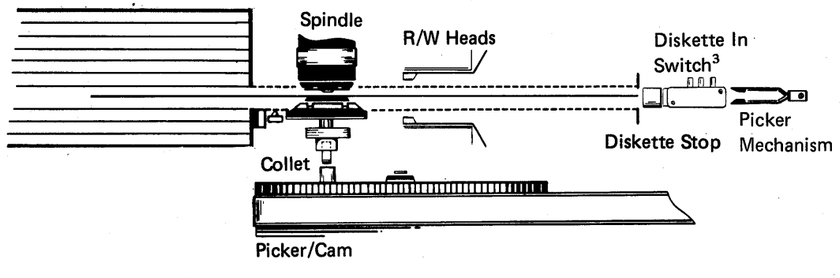
(276 steps from orient)[2]

Diskette In[2]



(392 steps from orient)

Collet Loaded



Carriage Bed Drive Motor

The carriage bed drive motor moves the carriage bed from magazine 2 slot 10 to I/O slot 1, the home position. Each position on the carriage bed is separated by eight 90-degree steps of the stepper motor. There are three extra positions between I/O slot 3 and magazine 1 slot 1, and four extra positions between magazine 1 slot 10 and magazine 2 slot 1.

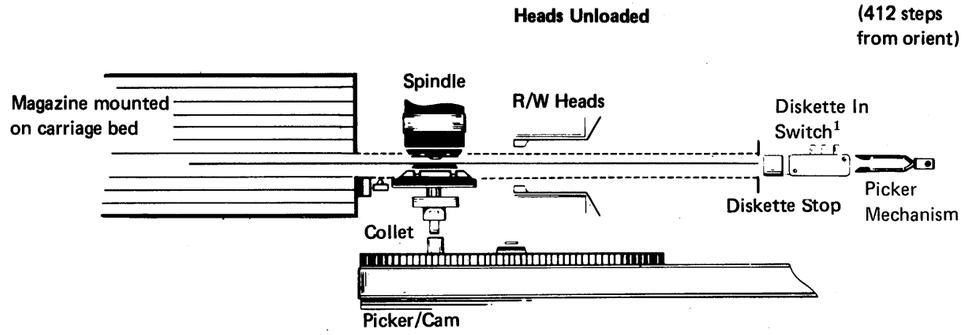
The access times for the carriage bed drive motor are as follows:

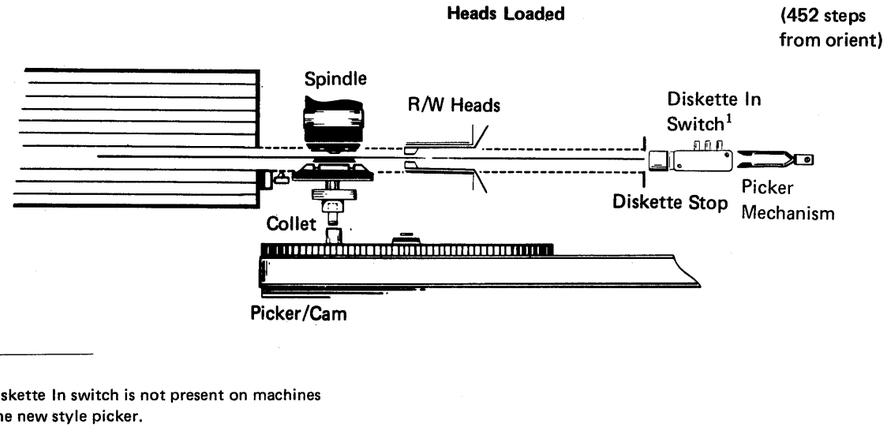
Acceleration Time	13 ms to 14 ms
Constant Velocity	12 ms
Deceleration Time	13 ms
Settling Time	60 ms

Head/Carriage Drive Motor

The head/carriage drive motor, under control of the control storage program, moves the head/carriage to cylinder 00 and from there moves the head/carriage 1 cylinder per 90-degree step.

The access time for a recalibrate operation is 0.84 seconds. The access time for a seek operation can be determined by using the formula of 41 + 8.2(n) = maximum time in milliseconds, where n is the number of cylinders to seek.





[1] The Diskette In switch is not present on machines with the new style picker.

72MD Operating Sequences

The 72MD has two modes of operation: autoloader mode and diskette drive mode. Carriage bed control, diskette insertion and removal from the drive, clamping and unclamping of the diskette to the drive hub, and loading and unloading of the data heads are functions of autoloader mode. The read, write, seek, and index hole detection are functions of diskette drive mode.

The following events make the 72MD operational:

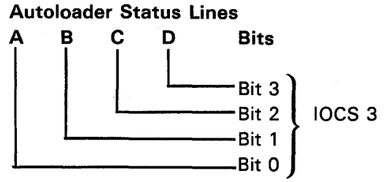
1. When system power is turned on, the power is also supplied to the 72MD.
2. When a diskette is inserted in an I/O slot or when a magazine is inserted and the 72MD cover is closed, the 72MD is operational.

Some of the lines between the channel and the 72MD attachment are used for both autoloader mode and diskette drive mode. These lines are controlled by the '+enable autoloader' line.

See *Input/Output Lines* later in this section.

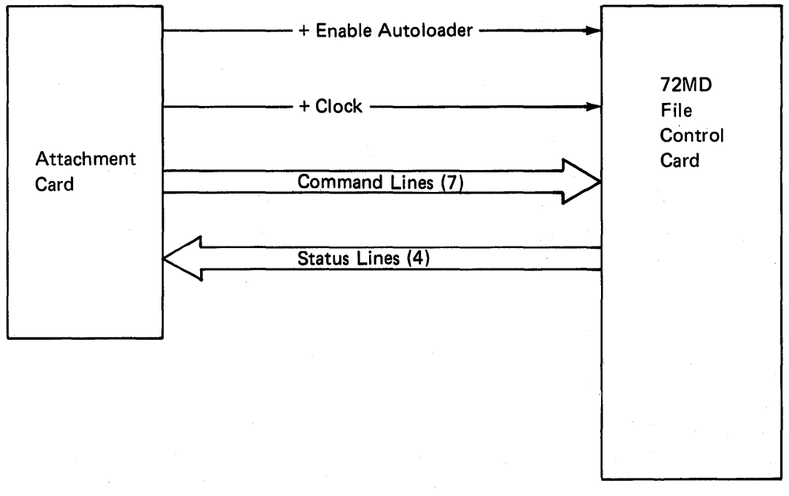
Autoloader Operation

When the '+enable autoloader' line is at the up level, the lines between the channel and the 72MD attachment control the autoloader. An operation that is started by the attachment, in response to a control storage program command, places an autoloader command on the 72MD command bus. At the end of an autoloader command, the autoloader status lines (bits 0 through 3 of IOCS 3) are sensed:



If an error is indicated (autoloader status line B), the autoloader status lines are sensed three more times and the assembled 16 bits become status bytes 4 and 5. See *Error Conditions* later in this section.

The picker and carriage bed motion necessary to complete the autoloader commands is performed by the picker/cam stepper motor or carriage bed stepper motor.



A description of the autoloader commands follows:

- Orient Command: This command causes the picker mechanism to move to the Picker Rest position (if a diskette is in the drive, it is ejected), to permit carriage bed motion. The carriage bed is stopped with I/O slot 1 aligned with the drive.

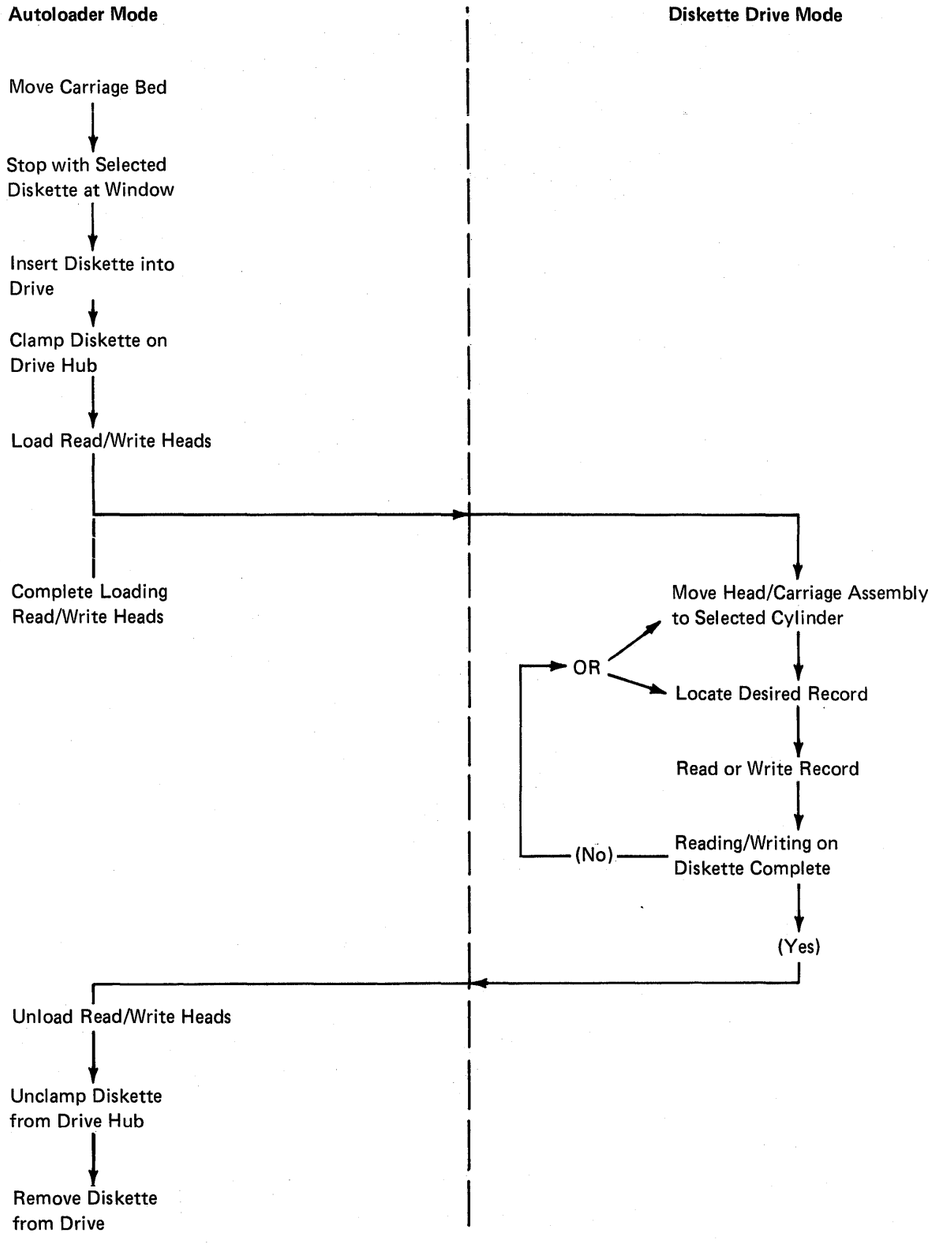
  On machines with the new style picker, this command causes the picker mechanism to move to the Picker Rest position, then to a position 280 steps from the Picker Orient position (to reset a mechanical latch), and then back to the Picker Rest position (if a diskette is in the drive, it is ejected) to permit carriage bed motion. The carriage bed is stopped with I/O slot 1 aligned with the drive.

- Select Diskette: This command causes the carriage bed to align the selected diskette position to the drive, the picker to insert that diskette into the drive, and the collet to clamp the diskette to the drive hub. If a diskette is already in the drive, that diskette is ejected to its magazine or I/O slot before the carriage bed is moved to the selected diskette position. The heads are not loaded by this command.

- Load Heads: This command causes the heads to be loaded if the collet has clamped a diskette to the drive hub.

- Unload Heads: This command causes the heads to be unloaded, but the collet continues to clamp the diskette to the drive hub.

- Eject Diskette: This command causes the diskette in the drive to be returned to its magazine or I/O slot.



Diskette Drive Operation

When the '+enable autoloader' line is at the down level, the lines between the channel and the 72MD attachment control the drive functions.

A description of the diskette drive functions follows:

- Seek Operation: To move the data heads to the desired track:
  - The control processor issues a control command to start the seek. The seek operation is done by activating the access lines in sequence. This action moves the head assembly in (toward the hub) or out (away from the hub). Activating two sequential access lines moves the head assembly 1 cylinder.
  - Before a read or write operation can occur, a 35-millisecond delay is needed for head carriage settle time.
  - At the end of a seek operation, two access lines remain active. The two access lines keep the stepper motor stopped, to keep the data heads on the track.

- Index Detection: This function senses a physical marker (the hole in the diskette). The 'index' line pulses when the index hole passes between the index phototransducer and the index light-emitting diode.

- Diskette Sense Line: This line uses the index pulse to determine the type of diskette turning in the drive. An up level indicates a Diskette 2D and a down level indicates a Diskette 1.

- Head Selection: This 'select head 1' line controls head selection. A down level selects head 0 for read or write operations. Head 0 is used for both Diskette 1 and Diskette 2D diskettes.

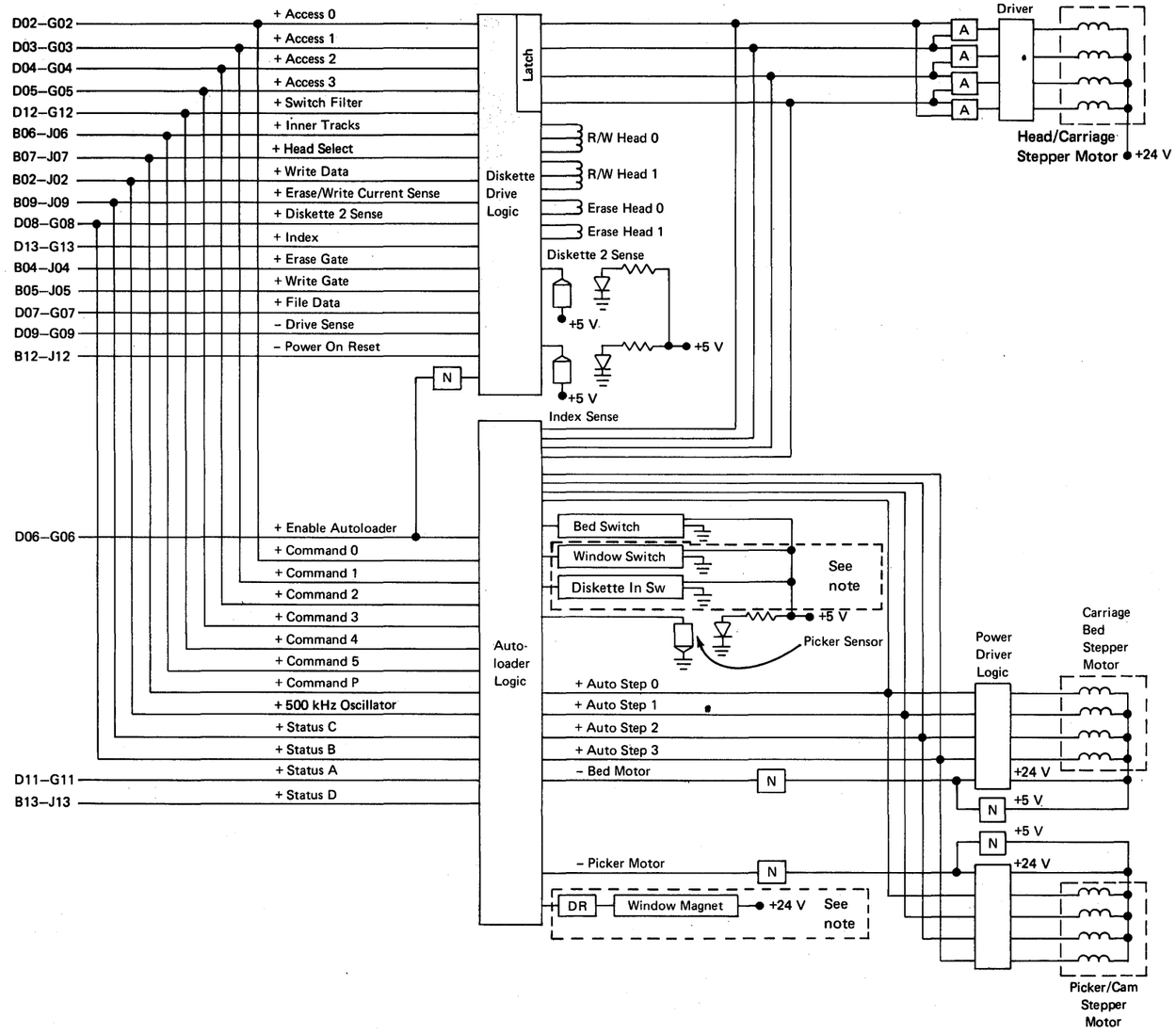
Read or Write Operation

To load the data heads and write on or read from the diskette:

1. With the 72MD in autoloader mode, the control processor issues a load heads command. The load heads command activates the access lines to the picker/cam stepper motor, which forces the data heads against the diskette. This action needs 121 milliseconds, after which the 'op end' signal is sent to the control processor. The 'op end' signal disables autoloader mode and enables diskette drive mode.

2. With the 72MD in diskette drive mode, the control processor issues a read or write command.

3. The control processor issues a command to unload the heads 335 milliseconds after a seek, read, or write operation is completed (if no other operation is issued in the 335 milliseconds). This action decreases wear on the diskette and the data heads. The 335-millisecond delay occurs because during normal diskette use, the next diskette operation usually starts within the 335-millisecond delay. Therefore, the data heads do not have to be loaded before each operation.



Note: The Diskette In switch, window switch, and window magnet are not present on machines with the new style picker.

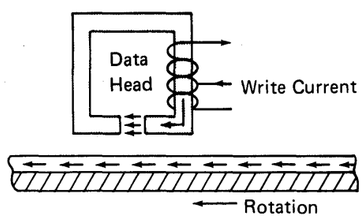
Frequency Modulation Read and Write Circuits

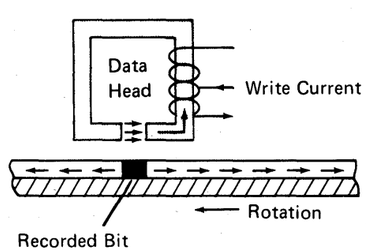
Writing

During a write operation, reversing the direction of the current in the data head coil (which reverses the direction of the magnetic flux in the gap) records a clock bit (identifies the start of a bit cell) or a 1-bit (data). When the direction of the flux reverses on the diskette surface, either a clock bit or a 1-bit is recorded.

Writing Data Bits

For each change on the 'diskette write data' line (A), a clock bit or a 1-bit is written on the diskette. No change between clock bits represents a 0-bit (not a 1-bit). Level changes on the 'diskette write data' line cause the current to be switched in the data head, which results in a polarity change on the diskette track. Therefore, a polarity change on the diskette represents a clock bit or a 1-bit. The time from 1 clock bit to the next clock bit is a bit cell and is approximately 4 microseconds for a 33FD or 53FD and 2 microseconds for a 72MD. Data bits are written in the center of the bit cell.



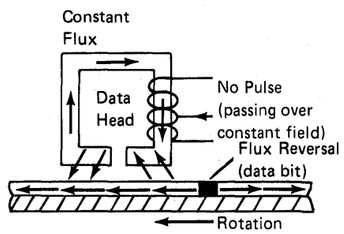


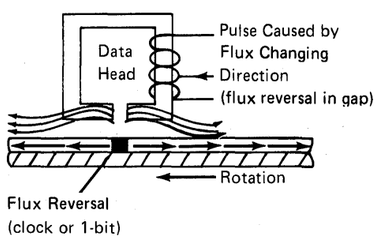
Reading

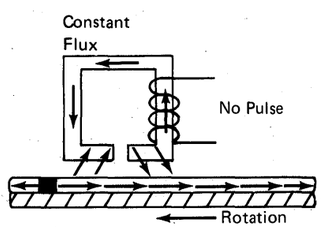
During a read operation, with the recording surface magnetized in one horizontal direction, constant flux flows and the coil senses no output voltage. However, when a recorded clock bit or 1-bit (180 degrees horizontal flux reverse) passes the gap, the flux moving through the ring and coil also reverses and causes a voltage output pulse.

Reading Data Bits

The horizontal flux changes on the diskette surface are represented on the '33FD raw read data' line (B), when read, as positive pulses with an approximate width of 150 nanoseconds. During a read operation, clock bits and data are separated in the variable frequency oscillator card.







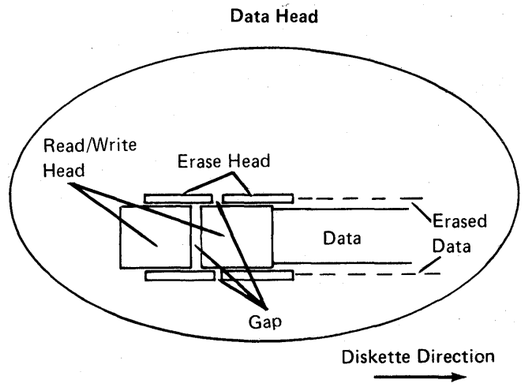
Controls

The 'write gate command' line (C) is active during a write operation. This line lets current flow through the data head (D) and de-activates the read circuits.

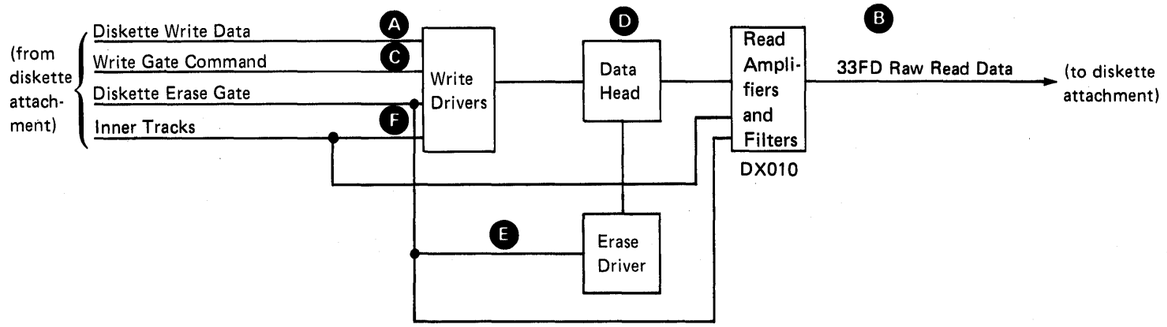
The 'diskette erase gate' line (E) also is active during a write operation. This line causes the edges of the data track to be erased, which leaves a gap between tracks (removes old data that could exist between tracks).

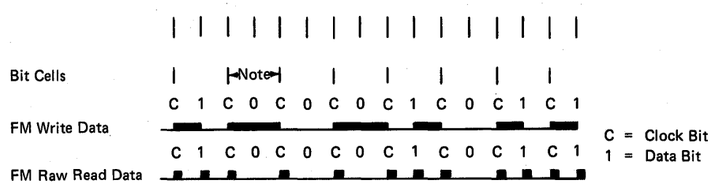
When the 'write gate command' line is not active, the write circuits are not gated and the read circuits are ready to read.

The 'inner tracks' line (F) is active from track 43 through track 76. When this line is active during a write operation, the write current through the data head is decreased. Less write current is needed on the inner tracks because the bit density increases toward the center tracks. When this line is active during a read operation, read filters compatible with tracks 43 through 76 are enabled.



33FD File Control Card





The above 1000 1011 represents hex 8B.

Note: The duration of a bit cell is 4 μs for a 33FD or 53FD and 2 μs for a 72MD.

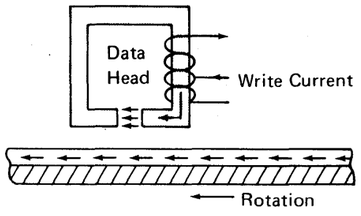
Modified Frequency Modulation Read and Write Circuits

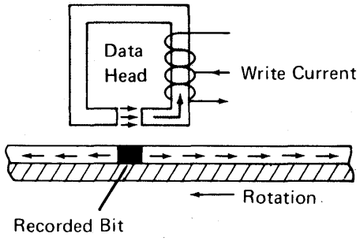
Writing

During a write operation, reversing the direction of the current in the data head coil (which reverses the direction of the magnetic flux in the gap) records a clock bit or a 1-bit (data). When the direction of the flux reverses on the diskette surface, either a clock bit or a 1-bit is recorded.

Writing Data Bits

For each change on the 'diskette write data' line (A), a clock bit or a 1-bit is written on the diskette. Data bits (1-bits) are always written in the center of the bit cell. If two bit cells in a row do not contain data bits, a clock (sync) bit is written at the start of the second bit cell. Data bits and clock bits are both shown if hexadecimal 8B is written. These changes cause the current in the data head to be switched, which results in a polarity change on the diskette track.



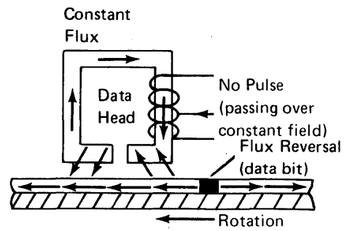


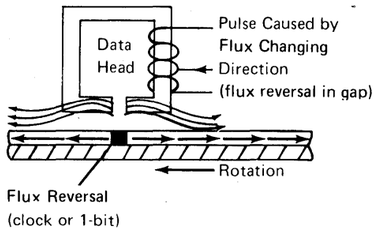
Reading

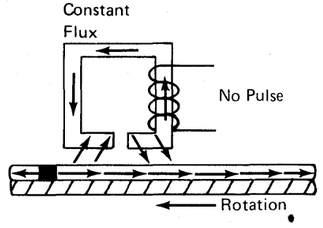
During a read operation, with the recording surface magnetized in one horizontal direction, constant flux flows and the coil senses no output voltage. However, when a recorded clock bit or data bit (180 degrees horizontal flux reverse) passes the gap, the flux moving through the ring and coil also reverses and causes a voltage output pulse.

Reading Data Bits

When data is read from the diskette (B), the read clock is synchronized to the incoming data by the variable frequency oscillator sync field. This field is 12 bytes of clock bits.







Controls

The 'select head 1' line (C) selects either head 1 or head 0.

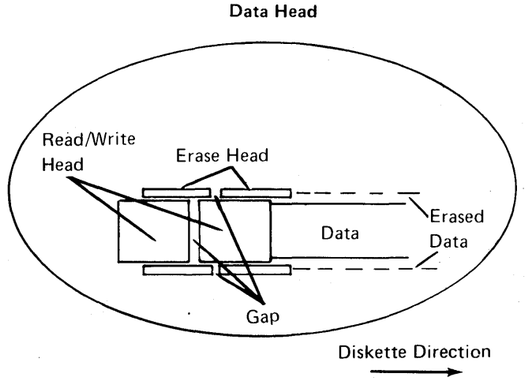
The 'write gate command' line (D) is active during a write operation. This line lets current flow through the selected data head (E) and de-activates the read circuits.

The 'diskette erase gate' line (F) also is active during a write operation. This line causes the edges of the data track to be erased, which leaves a gap between tracks (removes old data that could exist between tracks).

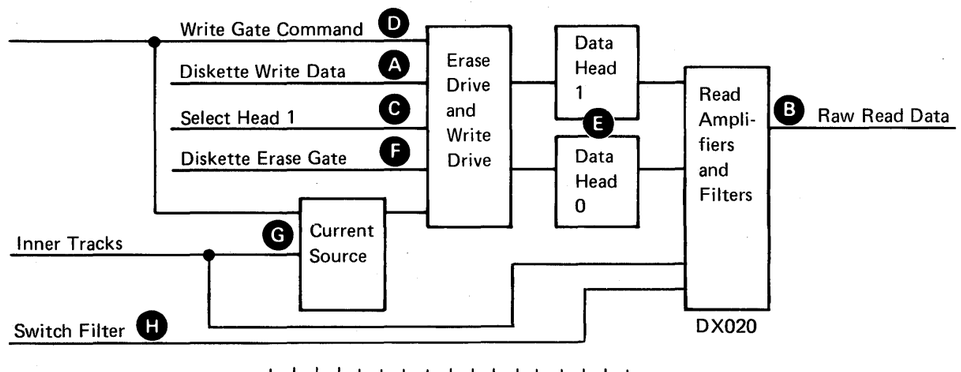
When the 'write gate command' line is not active, the write circuits are not gated and the read circuits are ready to read.

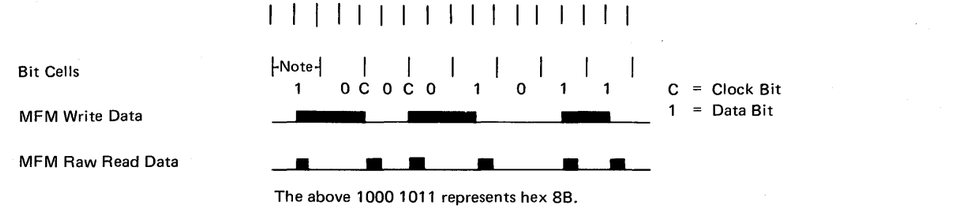
The 'inner tracks' line (G) is active from track 43 through track 76. When this line is active during a write operation, the write current through the data head is decreased. Less write current is needed on the inner tracks because the bit density increases toward the center tracks. When this line is active during a read operation, read filters compatible with tracks 43 through 76 are enabled.

The 'switch filter' line (H) is active from track 60 through track 76. When this line is active during a read operation, read filters compatible with tracks 60 through 76 are enabled. This line is not used during a write operation.



53FD/72MD File Control Card





The above 1000 1011 represents hex 8B.

Note: The duration of a bit cell is 2 μs for a 33FD or 53FD and 1 μs for a 72MD.

Diskette 1 Format

There are 77 tracks written in frequency modulation mode on the Diskette 1 surface. A track is a circular path on the surface of the diskette. The tracks are numbered 00 through 76. Track 00 is the outside track and track 76 is the inside track. Of the 77 tracks, only 74 tracks are data tracks. Track 00 is a label track; tracks 75 and 76 are reserved and are used in place of tracks that become damaged.

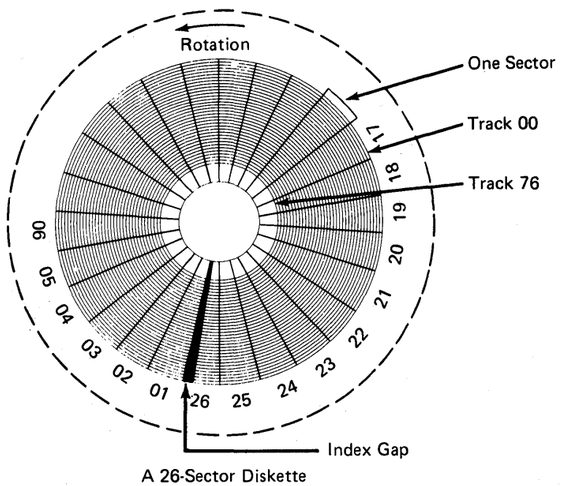
A damaged track is flagged by writing binary 1's in all ID fields of that track. The ID that would have been used on the damaged track is written in the ID field of the next physical track. When the ID field of a damaged track is read, the data head under control of the control storage program moves to the next higher or lower numbered physical track.

Each track is divided into either 8 or 26 sectors. The data stored in one sector is a record. When the tracks are divided into 8 sectors, each record is 512 bytes long; when tracks are divided into 26 sectors, each record is 128 bytes long. Diskettes with 74 data tracks that are divided into 8 sectors per track have 303,104 bytes of data; those diskettes whose data tracks are divided into 26 sectors per track have 246,272 bytes of data.

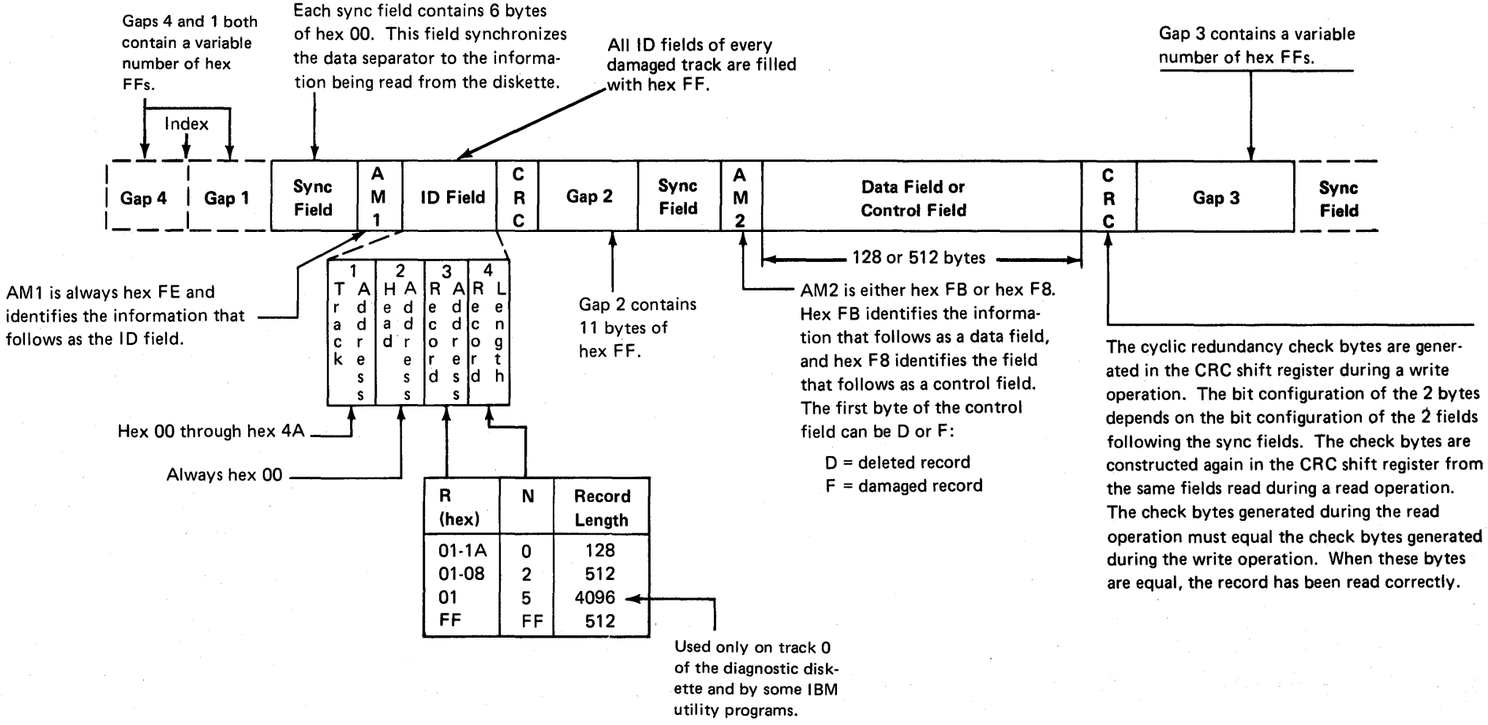
Some diagnostic programs and IBM utility programs write one 4,096-byte sector in frequency modulation mode on a track. Therefore, record length can be 128, 512, or 4,096 bytes. The value recorded in the record length byte indicates the record length.

Each sector on the diskette has its track and sector identification (address) recorded at the physical location of the sector on the diskette.

Diskettes that contain recorded sector identification fields (addresses) for each sector are known as initialized diskettes. Each sector has two parts; the first part contains the sector identification field, and the second part contains the data record field or the control record field.



A 26-Sector Diskette



R (hex)	N	Record Length
01-1A	0	128
01-08	2	512
01	5	4096
FF	FF	512

Diskette 2D Format

There are 77 tracks written in modified frequency modulation mode on each side of the Diskette 2D surface. A track is a circular path on the surface of the diskette. Two tracks (one on each side of the diskette) that can be read or written without moving the data head make up a cylinder. The cylinders are numbered 00 through 76. Cylinder 00 is the outside cylinder and cylinder 76 is the inside cylinder.

Of the 77 cylinders, only 74 cylinders are data cylinders. Track 0 of cylinder 00 is a label track written in frequency modulation mode. Track 1 of cylinder 00 is an extension of the label track written in modified frequency modulation mode. Cylinders 75 and 76 are reserved and are used in place of cylinders that become damaged.

A damaged cylinder is flagged by writing binary 1's in all ID fields of that cylinder. The ID that would have been used on the damaged cylinder is written in the ID field of the next cylinder.

When the ID field of a damaged cylinder is read, the data head under control of the control storage program moves to the next higher or lower numbered physical cylinder.

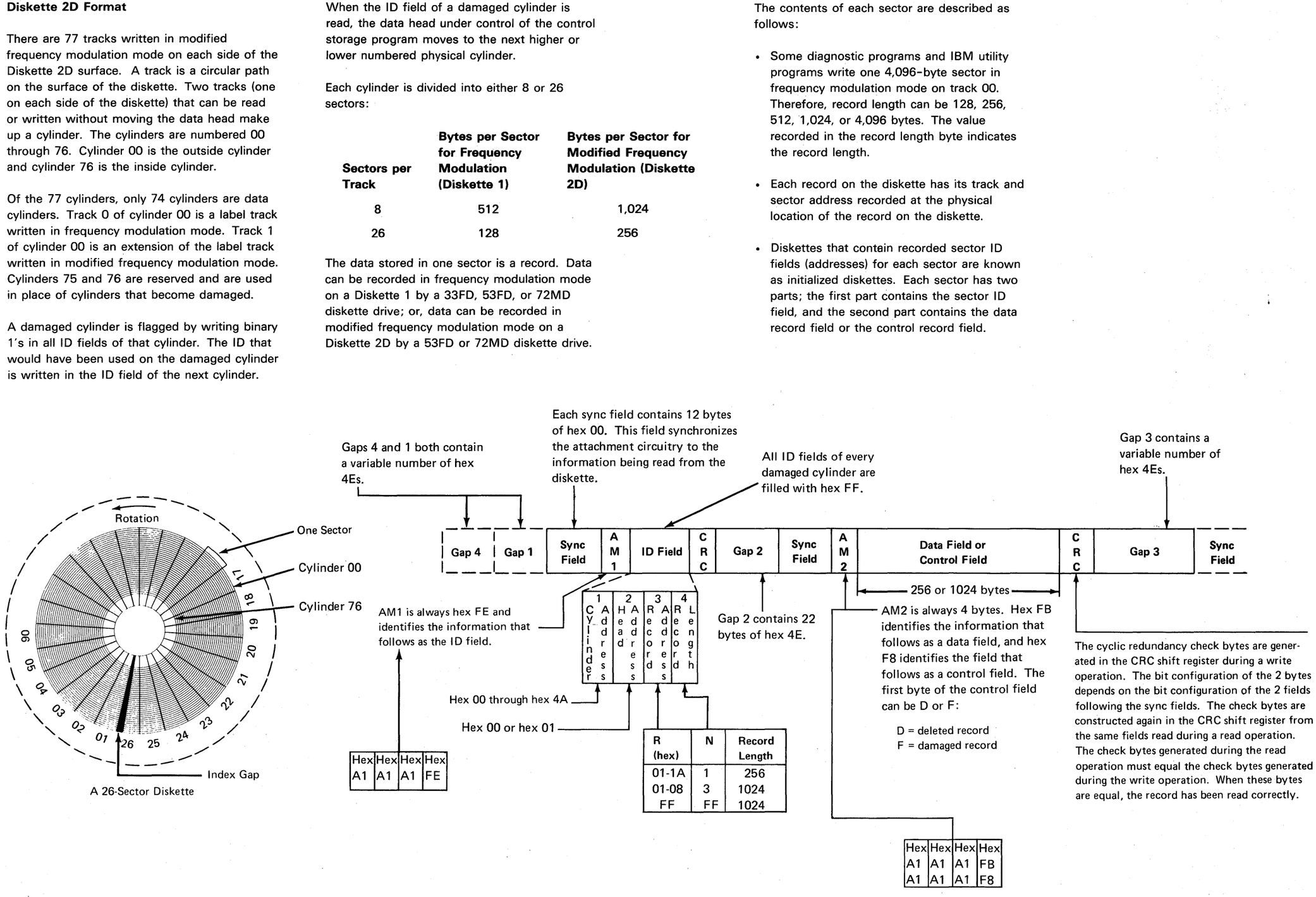
Each cylinder is divided into either 8 or 26 sectors:

Sectors per Track	Bytes per Sector for Frequency Modulation (Diskette 1)	Bytes per Sector for Modified Frequency Modulation (Diskette 2D)
8	512	1,024
26	128	256

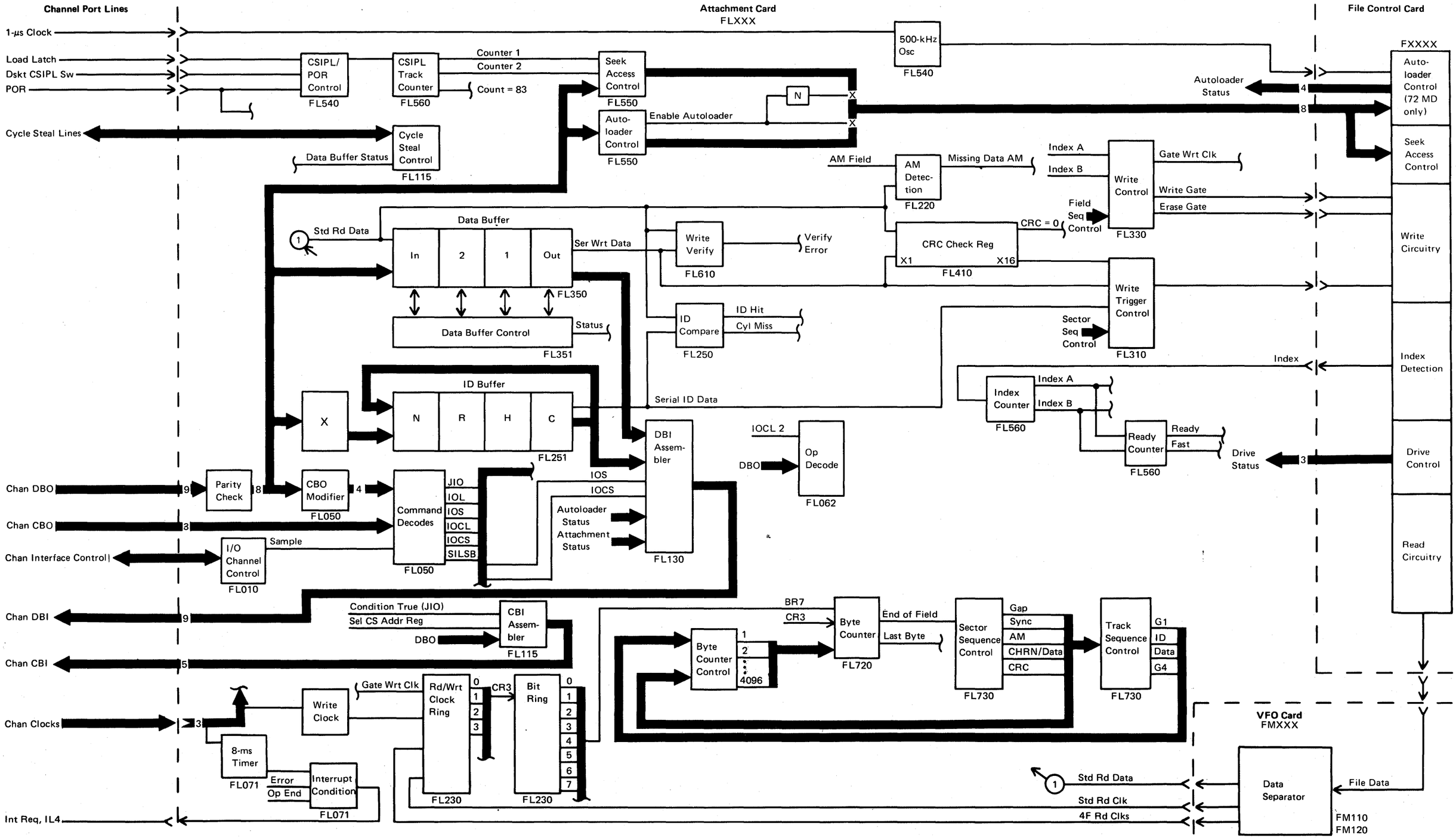
The data stored in one sector is a record. Data can be recorded in frequency modulation mode on a Diskette 1 by a 33FD, 53FD, or 72MD diskette drive; or, data can be recorded in modified frequency modulation mode on a Diskette 2D by a 53FD or 72MD diskette drive.

The contents of each sector are described as follows:

- Some diagnostic programs and IBM utility programs write one 4,096-byte sector in frequency modulation mode on track 00. Therefore, record length can be 128, 256, 512, 1,024, or 4,096 bytes. The value recorded in the record length byte indicates the record length.
- Each record on the diskette has its track and sector address recorded at the physical location of the record on the diskette.
- Diskettes that contain recorded sector ID fields (addresses) for each sector are known as initialized diskettes. Each sector has two parts; the first part contains the sector ID field, and the second part contains the data record field or the control record field.



DATA FLOW


Channel Port Lines
Attachment Card
FLXXX
File Control Card
FXXXX
1-µs Clock
Load Latch
Dskt CSIPL Sw
POR
CSIPL/ POR Control
FL540
CSIPL Track Counter
FL560
Counter 1
Counter 2
Count = 83
Seek Access Control
FL550
500-kHz Osc
FL540
Auto-loader Control
FL550
Enable Autoloader
N
Autoloader Status
Auto-loader Control (72 MD only)
Seek Access Control
Cycle Steal Lines
Cycle Steal Control
FL115
Data Buffer Status
AM Field
AM Detec-tion
FL220
Missing Data AM
Index A
Index B
Write Control
FL330
Gate Wrt Clk
Write Gate
Erase Gate
Field Seq Control
Std Rd Data
Data Buffer
In
2
1
Out
FL350
Ser Wrt Data
Write Verify
FL610
Verify Error
CRC Check Reg
X1
X16
FL410
CRC = 0
Write Circuitry
Data Buffer Control
FL351
Status
ID Compare
FL250
ID Hit
Cyl Miss
Write Trigger Control
Sector Seq Control
FL310
Index
Index Detection
ID Buffer
N
R
H
C
FL251
Serial ID Data
Index Counter
FL560
Index A
Index B
Ready Counter
FL560
Ready
Fast
Drive Status
Drive Control
X
IOCL 2
DBO
Op Decode
FL062
DBI Assem-bler
FL130
IOS
IOCS
Autoloader Status
Attachment Status
Chan DBO
Parity Check
CBO Modifier
FL050
Command Decodes
JIO
IOL
IOS
IOCL
IOCS
SILSB
FL050
Chan CBO
Chan Interface Control
I/O Channel Control
FL010
Sample
Read Circuitry
Chan DBI
Condition True (JIO)
Sel CS Addr Reg
DBO
CBI Assem-bler
FL115
Chan CBI
BR7
CR3
Byte Counter Control
1
2
4096
Byte Counter
FL720
End of Field
Last Byte
Sector Sequence Control
FL730
Gap
Sync
AM
CHRN/Data
CRC
Track Sequence Control
FL730
G1
ID
Data
G4
Chan Clocks
Write Clock
Gate Wrt Clk
Rd/Wrt Clock Ring
FL230
CR3
Bit Ring
FL230
8-ms Timer
FL071
Error
Op End
Interrupt Condition
FL071
Int Req, IL4
VFO Card
FMXXX
Std Rd Data
Std Rd Clk
4F Rd Clks
Data Separator
File Data
FM110
FM120

OPERATIONS

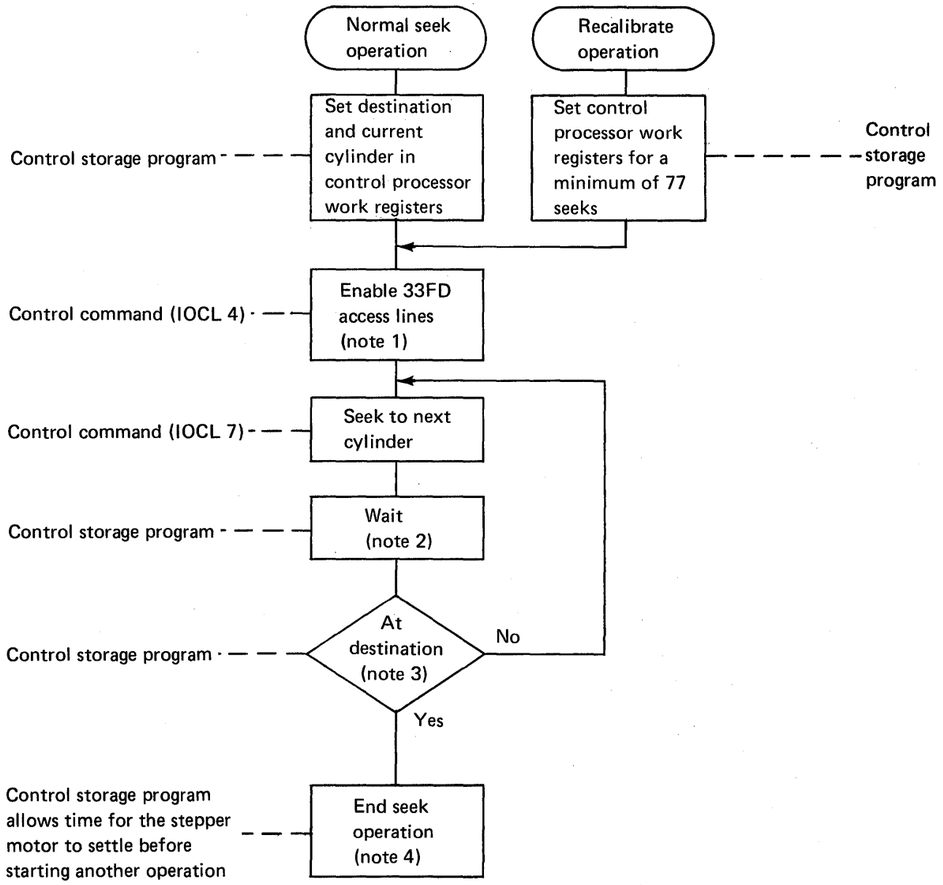
Diskette Drive Operations

Seek Operation

The attachment controls the seek operation by controlling the four access lines to the head/carriage stepper motor. The two types of seek operations are:

- Normal Seek: Seek from the present known cylinder to a specified cylinder.
- Recalibrate: Seek from present location (location not known) to cylinder 00.

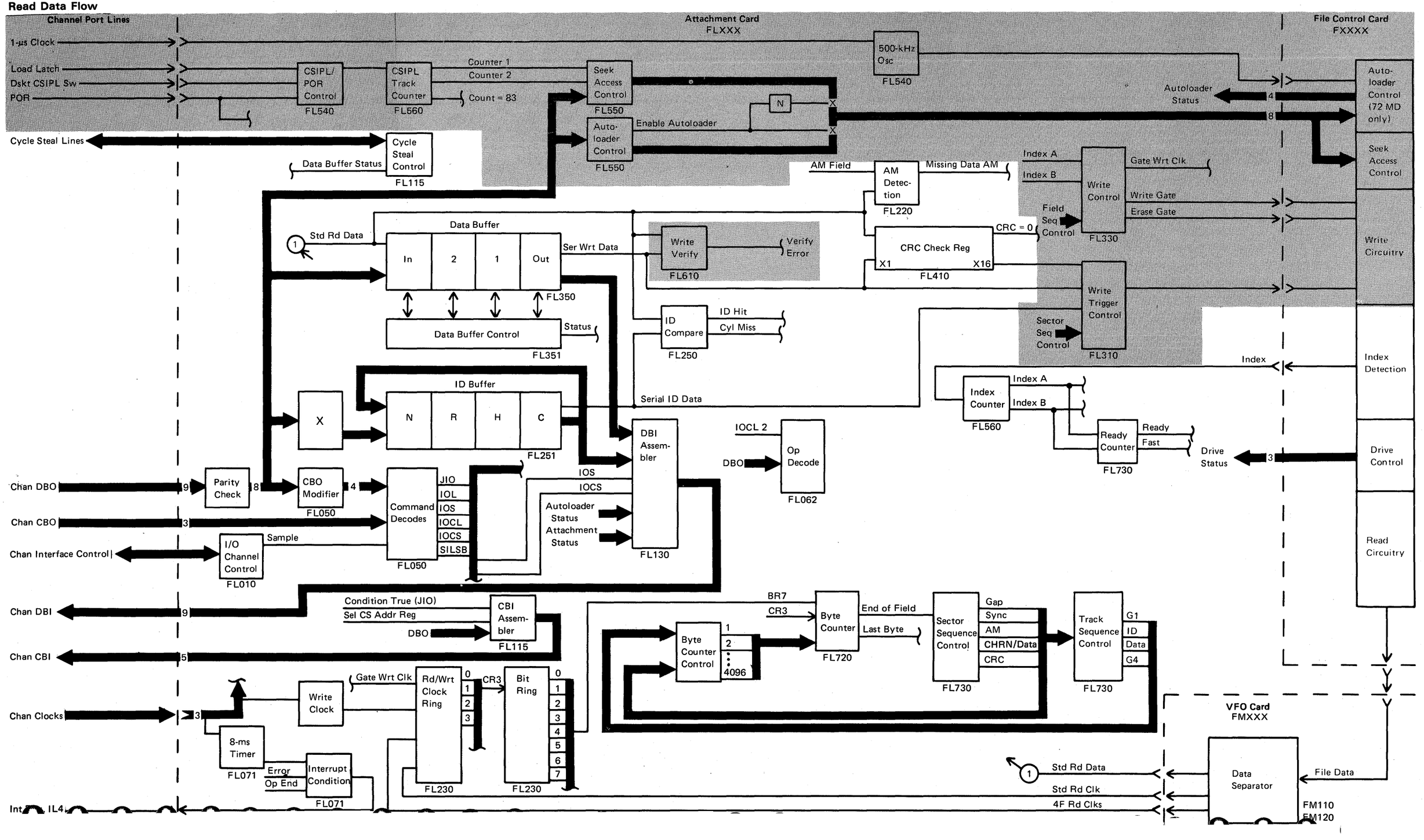
The control processor controls the seek operation (except for the recalibrate done during a diskette CSIPL; this recalibrate is done completely by attachment hardware). The control processor must know the cylinder location of the data heads before starting the operation (except for the recalibrate operation) and also must know the specified target cylinder. The control processor issues a seek command, which starts a seek operation. The seek operation moves the data heads 1 cylinder per command until the specified cylinder is reached or the operation is ended. The recalibrate operation is necessary when the cylinder location of the data head is not known. The control processor sets up a reverse seek of 77 cylinders.



Notes:

1. If the diskette drive is a 33FD, the stepper motor lines must be enabled. This is not necessary for 53FD or 72MD drives because two of the four lines are always active (for detent).
2. A wait time of 56 milliseconds for a 33FD or 8.2 milliseconds for a 53FD or 72MD is allowed for the seek.
3. The control storage program updates the current cylinder and compares to the destination. If the two are not the same, another seek is issued.
4. The settle time is 96 milliseconds for a 33FD or 33 milliseconds for a 53FD or 72MD.

Read Data Flow



Read Operation

There are three types of read operations:

- Read Data: This operation reads specified data records into main storage. Control records flagged as deleted or defective are not read.
- Read Data and Control Records: This operation is the same as the read data operation, except that records flagged as deleted or defective are read as well as a data field.
- Read Identifier: This operation reads one 4-byte identifier field (CHRN) from the track under the data head and sends it to main storage. The field that is sent to main storage is the first identifier read without an error.

The control processor starts the read operation. I/O load commands (IOL A) specify the cylinder, head, record number, record format, and number of records to be processed (CHRNX field) to the attachment hardware. An I/O control load command (IOCL 2) then starts the read operation. The first job of the attachment hardware is to locate the specified record to be processed. See *Find Sector Identification Operation* later in this section.

After the specified identifier field is located, the data field is processed. The read clock and read bit ring synchronize the attachment to the serial input data from the diskette. The sector sequence control and the track sequence control logic use the byte counter, the address mark detection logic, and the CRC register logic to specify the start and end of the data record. The data record is moved to main storage by cycle steal (2-byte bursts). Byte parity is generated and the CRC for the serialized data read is assembled and compared to the data field CRC read from the diskette.

The number of records processed by a single control processor command depends on the number in the X byte of the CHRNX data loaded into the attachment ID buffer at the start of the operation. When the last record has been processed, the attachment hardware indicates the operation is complete by issuing an interrupt level 4 request; control is returned to the control processor.

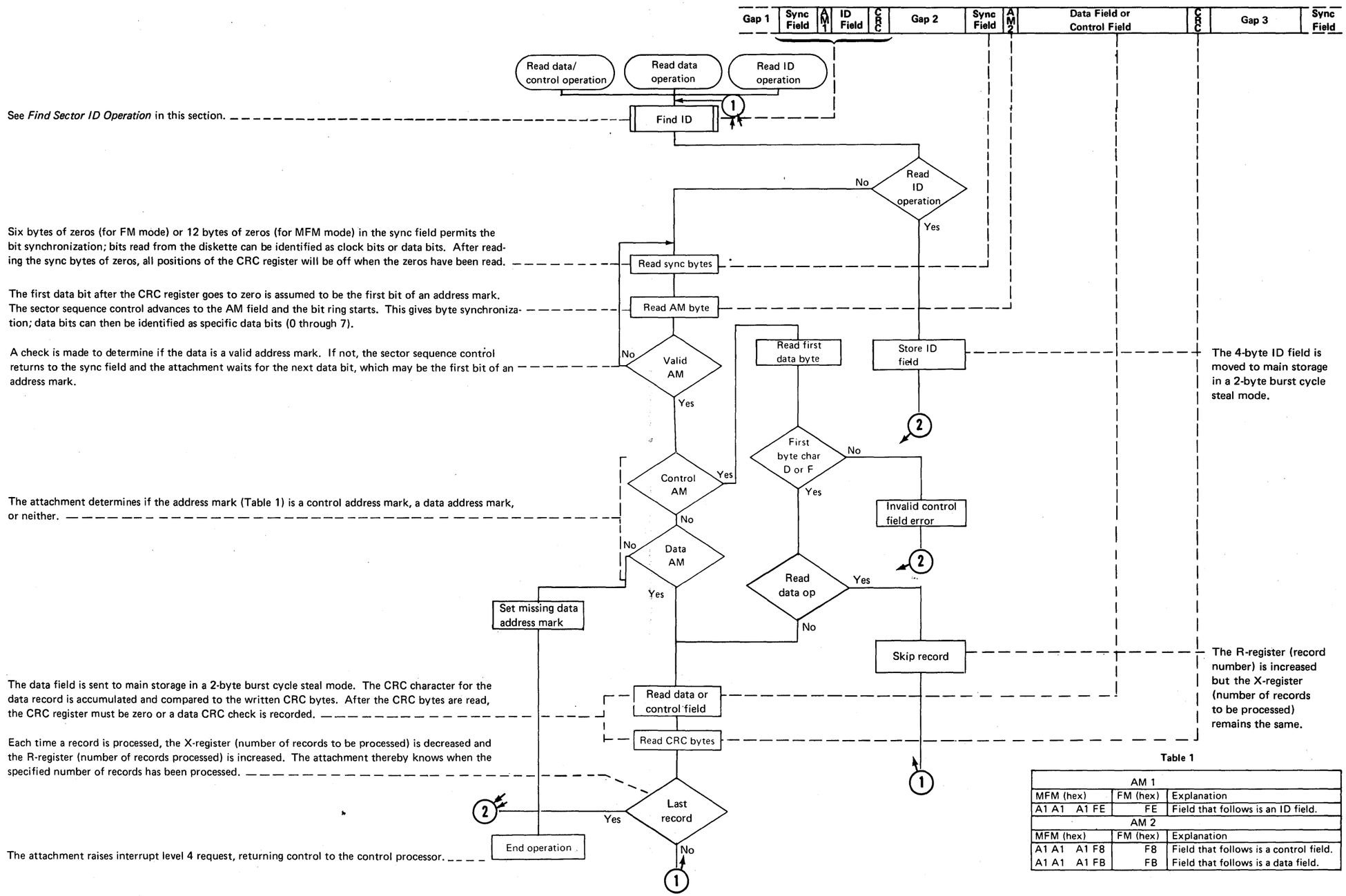
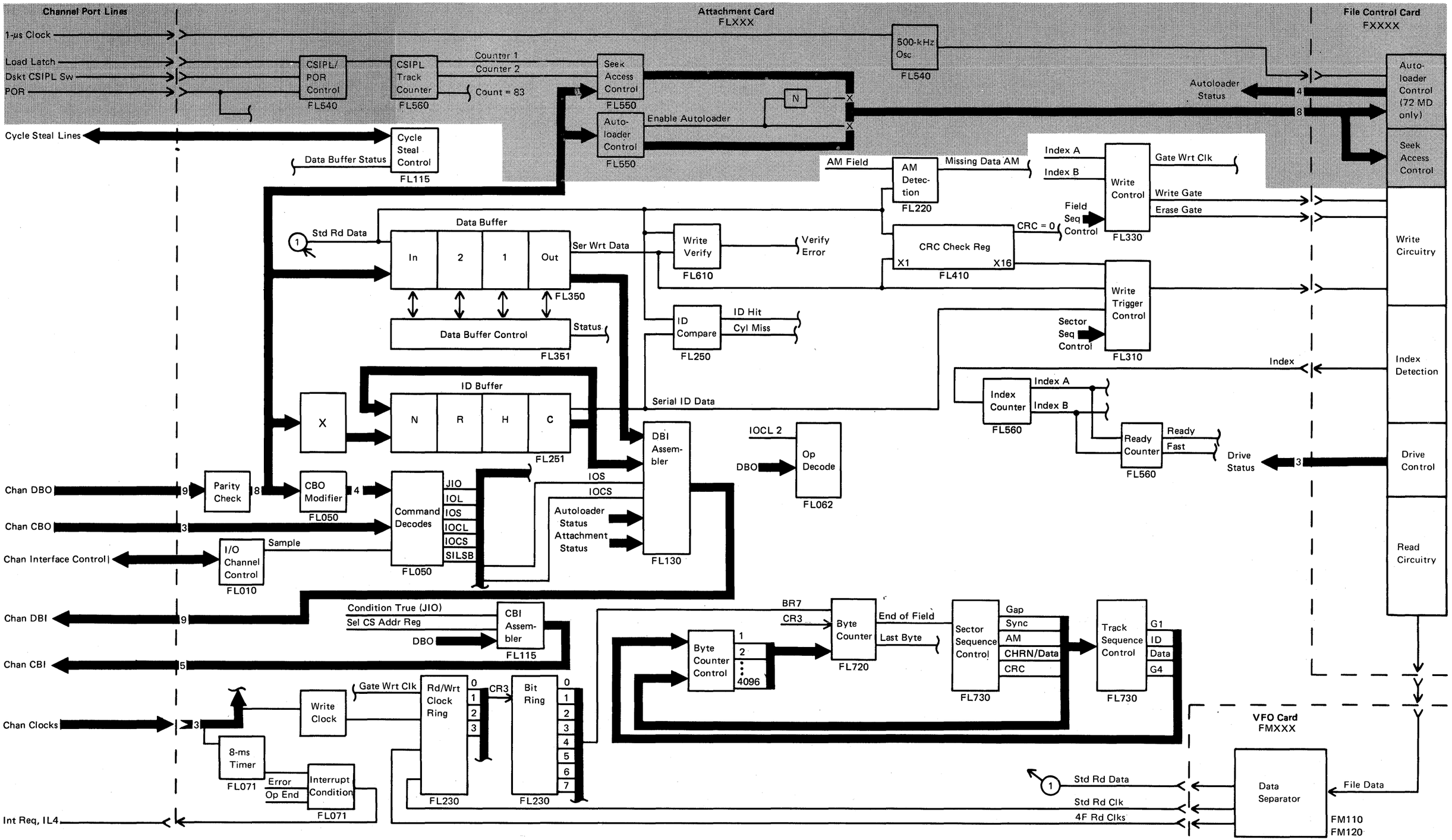


Table 1

AM 1		
MFM (hex)	FM (hex)	Explanation
A1 A1 A1 FE	FE	Field that follows is an ID field.
AM 2		
MFM (hex)	FM (hex)	Explanation
A1 A1 A1 F8	F8	Field that follows is a control field.
A1 A1 A1 FB	FB	Field that follows is a data field.

Write Data Flow



Write Operation

Write operations are performed on data fields and their sync fields. Identifier fields and gaps are not written again.

There are two types of write operations:

- Write Data: This operation moves data from the data field in main storage to the specified diskette sector.
- Write Control Record: This operation writes control records on the specified diskette sectors. The first byte in the data field in main storage is repeated for all bytes in all records that are written. A byte of hexadecimal C4 (EBCDIC character D) is used to indicate deleted records.

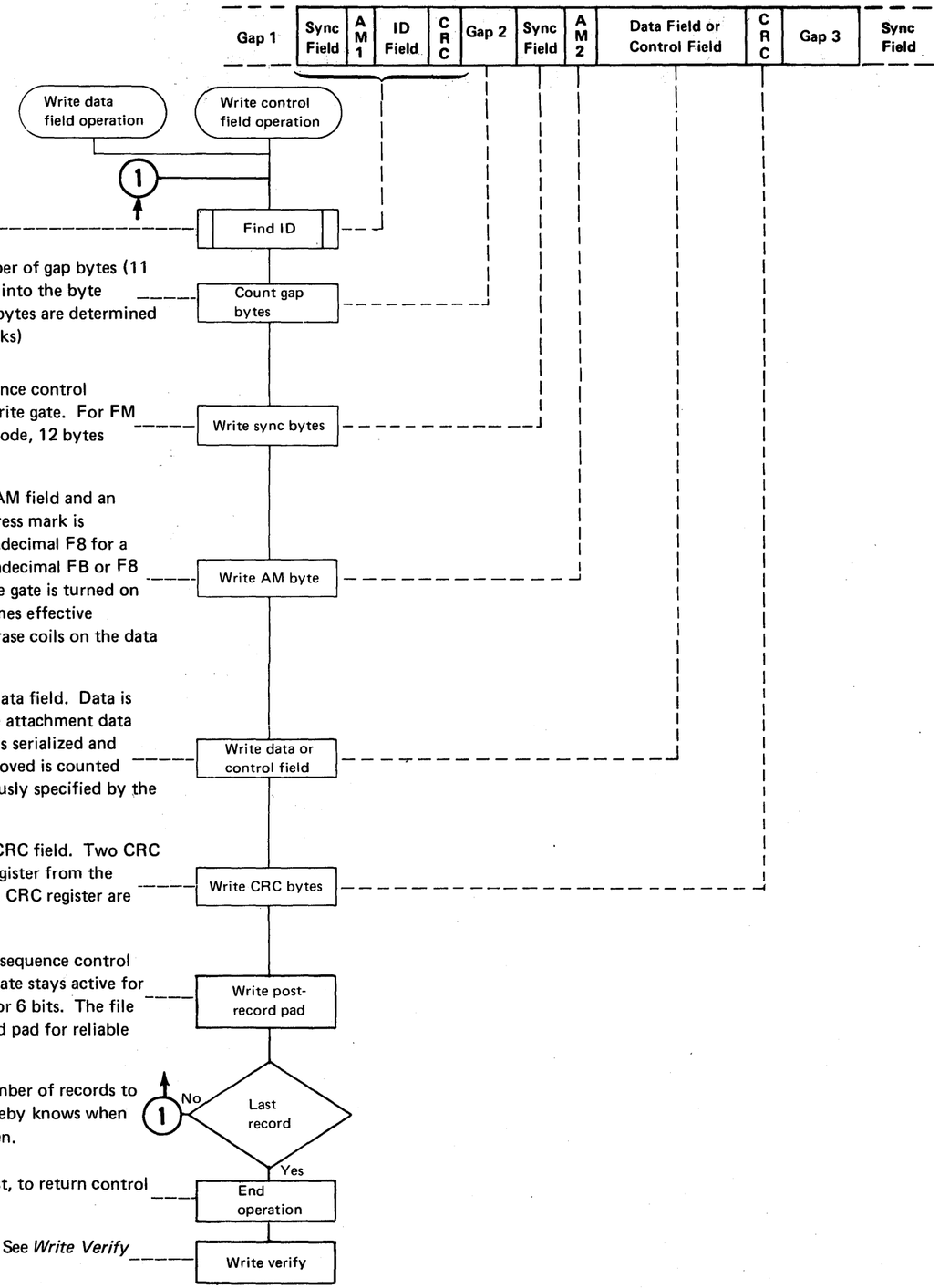
The write operations are started by the control processor. The cylinder, head, record number, record format, and number of records to be written (CHRNX field) are specified to the attachment hardware by I/O load commands (IOL A). The first job of the attachment hardware is to find the specified location on the diskette where the record is to be written. See *Find Sector Identification Operation* later in this section.

After the specified identifier field is found, the data field is written. The write clock is gated during gaps and while the write gate is on, and drives the bit ring to supply bit and byte synchronization for the write data output of the attachment card. The write circuits of the file control card are controlled by the write gate, which is on from the start of the data record sync field until after the data field CRC field is written. The erase circuits of the file control card are controlled by the erase gate, which is on from the start of the data record AM field until the start of the next ID field sync field. The write gate and erase gate are turned on at different times because of the physical location of the write and erase coils on the data head.

The sector sequence control and the track sequence control logic determine the field locations on the diskette and the physical location of the sync field and data record to be written. The data is moved from main storage to the attachment data buffer by cycle steal (2-byte bursts). The data is serialized and sent to the file control card as write data with the clock bits inserted.

The number of records to be written by a single control processor command depends on the X byte of the CHRNX data that was loaded into the attachment ID buffer at the start of the operation. When the last record has been written, the attachment hardware indicates the operation is complete by issuing an interrupt level 4 request; control is returned to the control processor.

Immediately following each write data or write control record operation, the control processor issues an I/O control load command (IOCL 2) to do a write verify operation. The verify is done by reading the data just written and comparing it to the original data in main storage. See *Write Verify Operation* in this section.



See *Find Sector ID Operation* in this section.

Position tracking is realized by loading the number of gap bytes (11 bytes for FM mode or 22 bytes for MFM mode) into the byte counter and decreasing the counter every byte (bytes are determined by the bit ring, which is controlled by write clocks)

When all gap bytes are counted, the sector sequence control advances to the sync field, which turns on the write gate. For FM mode, 6 bytes of zeros are written. For MFM mode, 12 bytes of zeros are written.

The sector sequence control is advanced to the AM field and an address mark is written. For FM mode, the address mark is hexadecimal FB for a date address mark or hexadecimal F8 for a control address mark. For MFM mode, the hexadecimal FB or F8 is preceded by 3 bytes of hexadecimal A1. Erase gate is turned on at the beginning of the AM field and erase becomes effective somewhere in gap 2 due to the position of the erase coils on the data head.

The sector sequence control is advanced to the data field. Data is moved from the data field in main storage to the attachment data buffer by cycle steal in 2-byte bursts. The data is serialized and written on the diskette. The number of bytes moved is counted by the byte counter. The record size was previously specified by the CHRNX field.

The sector sequence control is advanced to the CRC field. Two CRC characters have been accumulated in the CRC register from the written AM and data fields. The contents of the CRC register are written on the diskette.

After the 2-byte CRC field is written, the sector sequence control advances to the gap field. For FM mode, write gate stays active for 4 bits. For MFM mode, write gate stays active for 6 bits. The file control card write circuits require the post-record pad for reliable operation.

Each time a record is written, the X-register (number of records to be processed) is decreased. The attachment thereby knows when the specified number of records have been written.

The attachment raises an interrupt level 4 request, to return control to the control processor.

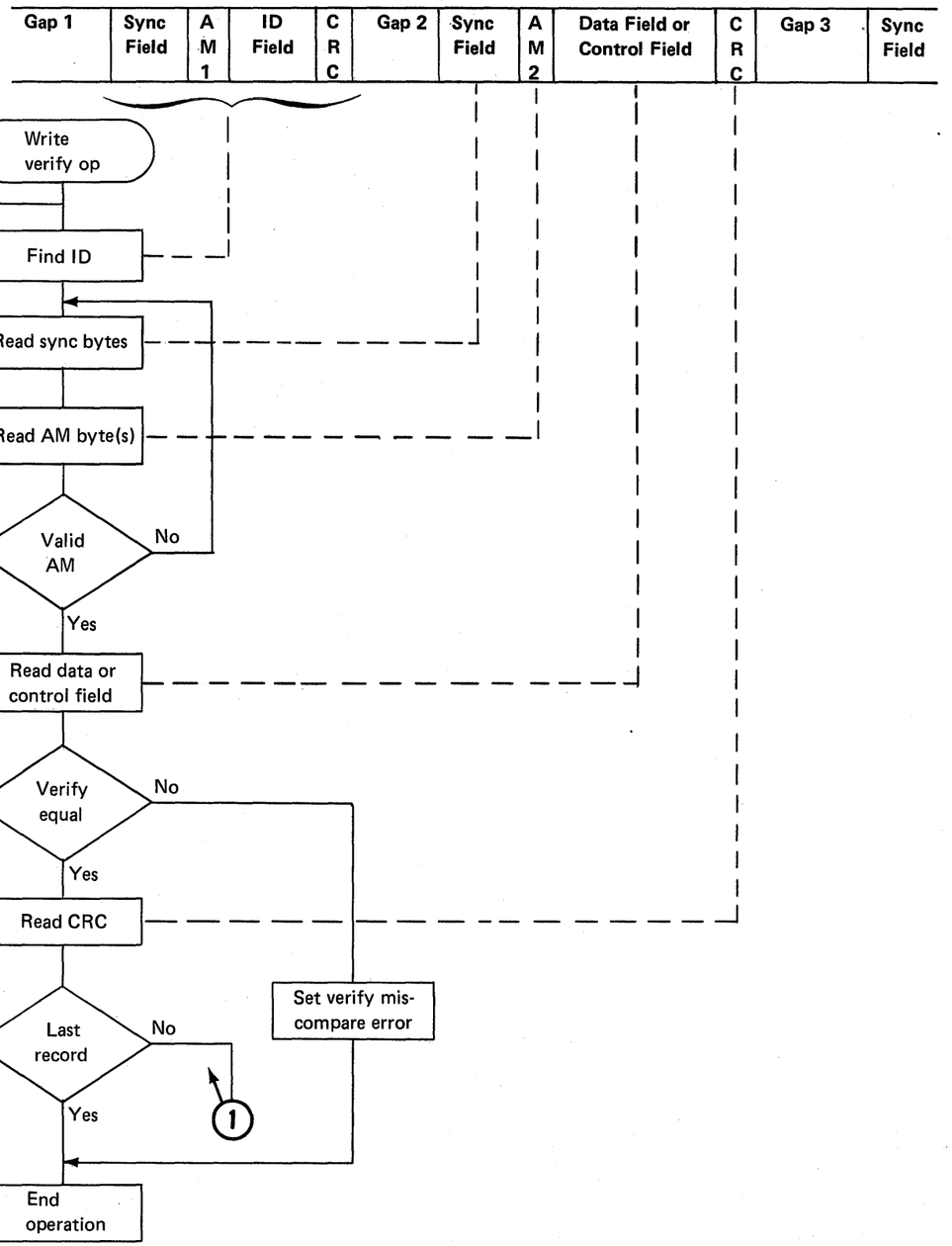
A write verify operation always follows a write. See *Write Verify Operation* later in this section.

Write Verify Operation

The write verify operation is performed after every write operation. The verify is done by reading the data just written and comparing it to the original data in main storage.

The write verify operation is started by the control processor. The cylinder, head, record number, record format, and number of records to be verified (CHRNX field) are specified to the attachment hardware by I/O load commands (IOL A). The first job of the attachment is to find the specified location of the record on the diskette. See *Find Sector Identification Operation* in this section.

After the specified identifier field is found, the sector sequence control and the track sequence control logic determine the field locations on the diskette to find the data fields just written. The original data is moved from main storage to the attachment data buffer by cycle steal (2-byte bursts). The contents of the data buffer are compared bit by bit to the serial read data from the diskette. The CRC for the serial read data is assembled and compared to the CRC of the original data. When the last record has been compared, the attachment hardware indicates the operation is complete by issuing an interrupt level 4 request; control is returned to the control processor.



See *Find Sector ID Operation* in this section.

Six bytes of zeros (for FM mode) and 12 bytes of zeros (for MFM mode) in the sync field permits bit synchronization; bits read from the diskette can be identified as clock bits or data bits. All positions of the CRC register will be off when the zero bytes have been read.

The first data bit after the CRC register goes to zero is assumed to be the first bit of an address mark. The sector sequence control advances to the AM field and the bit ring starts. The bit ring gives byte synchronization; data bits can be identified as specific data bits (0 through 7).

A check is made to determine if the data is a valid address mark. If not, the sector sequence control returns to the sync field, and the attachment reads the sync bytes to zero the CRC register and waits for the next data bit, which may be the first bit of an address mark.

Data is moved from main storage to the attachment data buffer by cycle steal in 2-byte bursts. This data is compared bit by bit to the serial read data from the diskette.

If the data does not compare, the write verify mismatch error is set and the operation is terminated, which returns control to the control processor.

The CRC for the data record on diskette was accumulated and compared to the written CRC characters. After the CRC bytes are read, the CRC register must be zero or a CRC check is set.

Each time a record is processed, the X-register (number of records to be processed) is decreased. This allows the attachment to know when the specified number of records have been processed.

The attachment raises an interrupt level 4 request, which returns control to the control processor.

Find Sector Identification Operation

This operation is an attachment hardware function and is part of all data mode operations except the write sector ID operation.

Before a command is issued for a read, write, or write verify operation, the control processor issues I/O load commands (IOL A) to specify the cylinder, head, starting record number, record format, and number of records to be processed (CHRNX field). This information is stored in the attachment ID buffer and specifies the logical location on the diskette where processing is to start.

The operation is started by the control processor when the data mode operation command is issued. The sector sequence control and track sequence control logic determine the field locations on the diskette. The sector sequence control starts in the sync field. When a diskette sync field is read, bit synchronization is completed, and enough 0-bits are read to fill all positions of the CRC register with zeros. The next data bit causes the sector sequence control to advance to the AM field. The data read is checked to see if it is a valid address mark and if it is an ID address mark.

If the data is a valid ID address mark, the sector sequence control is advanced to the CHRN field; if not, the sector sequence control returns to the sync field.

If the address mark was a valid ID address mark, the next data read (CHRN) is compared to the CHRN data in the ID buffer. If the read CHRN is the specified address, an ID hit is made and the data record processing starts. If the CHRN does not compare, the sector sequence control returns to the sync field and the search for the specified address ID continues.

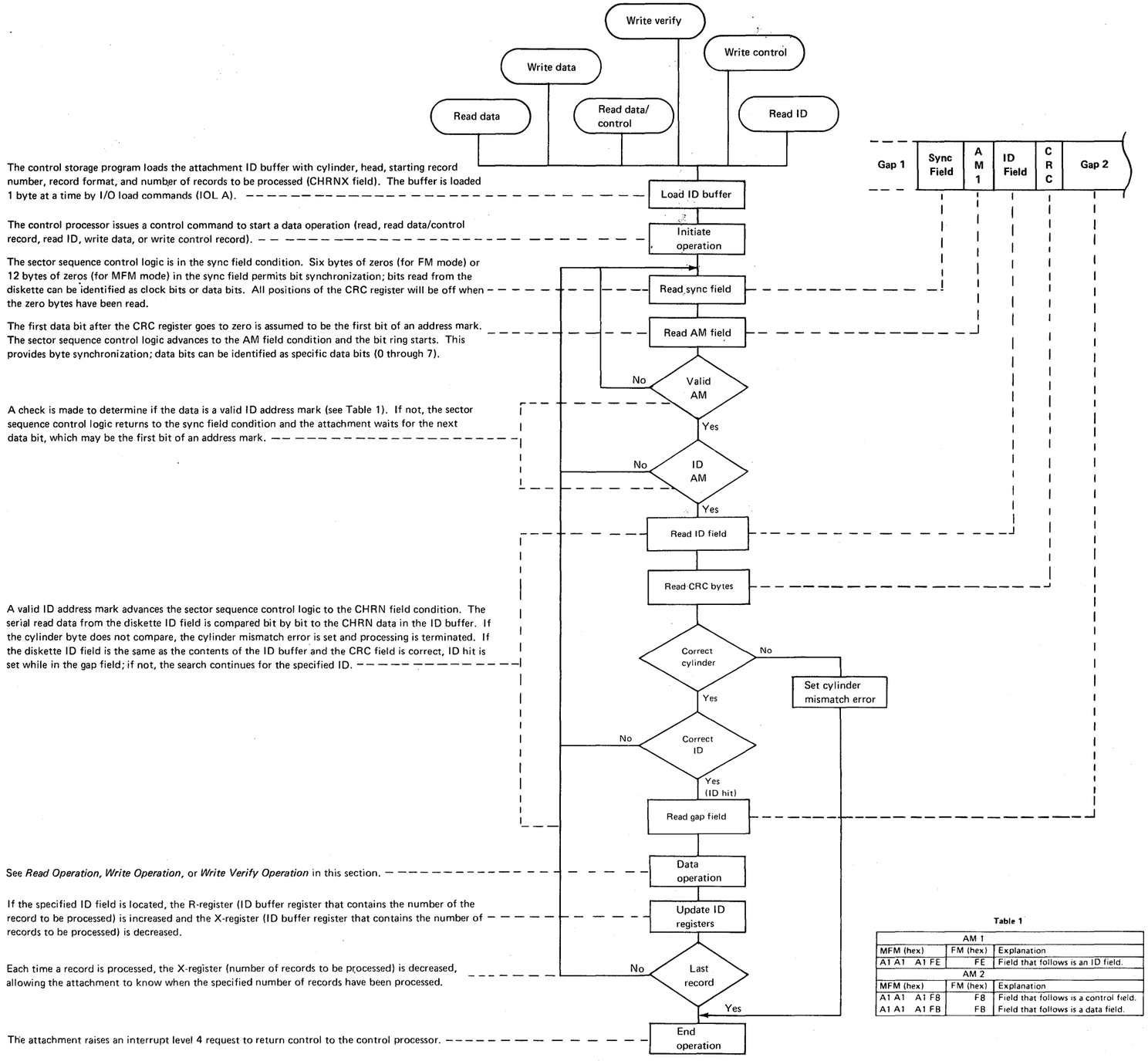


Table 1

AM 1		
MFM (hex)	FM (hex)	Explanation
A1 A1 A1 FE	FE	Field that follows is an ID field.
AM 2		
MFM (hex)	FM (hex)	Explanation
A1 A1 A1 F8	F8	Field that follows is a control field.
A1 A1 A1 FB	FB	Field that follows is a data field.

Write Sector Identification Operation

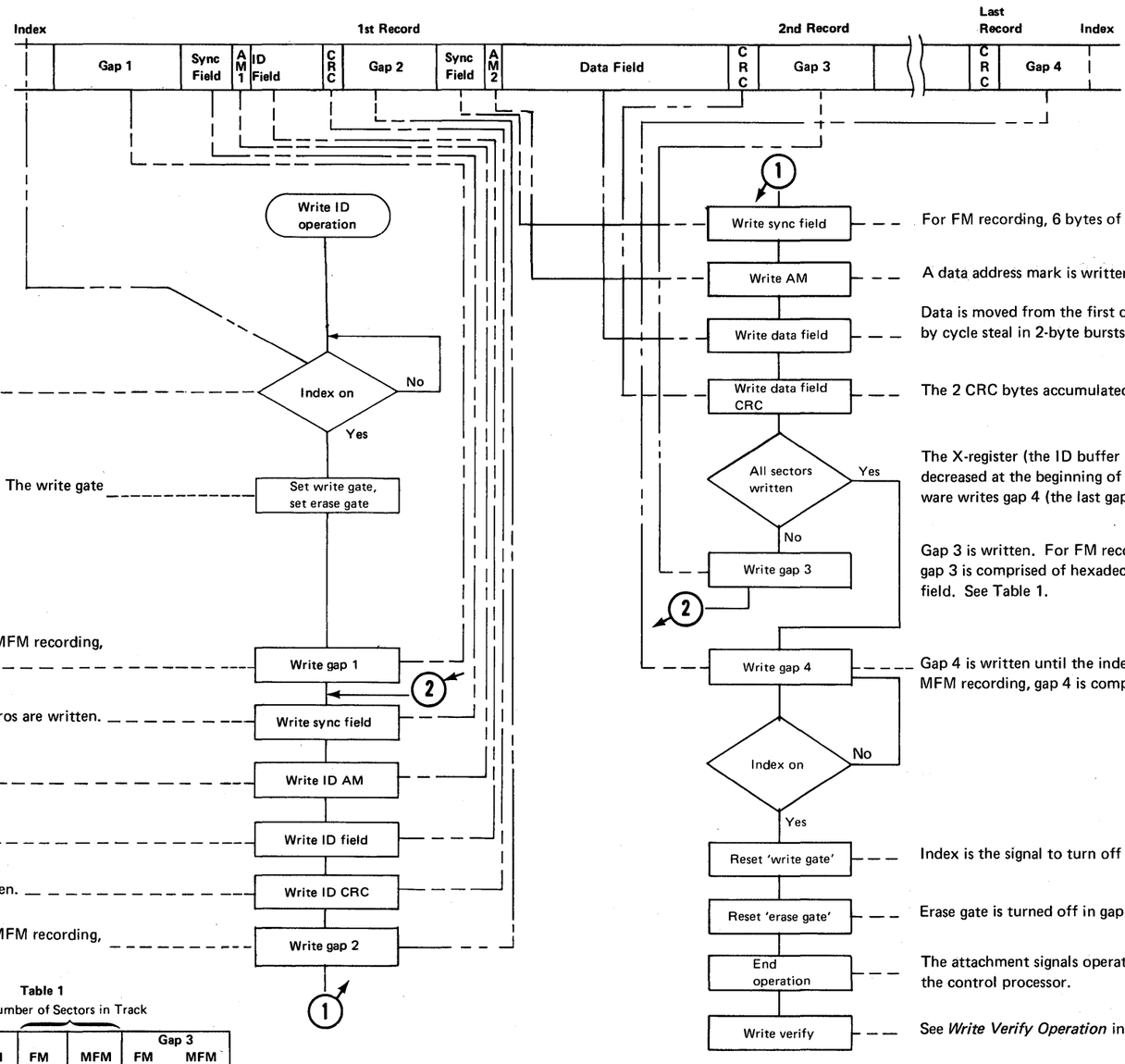
This operation is used to initialize a diskette. The sector identification fields and data fields, and their gaps, are written. During initialization, the first data byte in the main storage data area is written to all data fields on the diskette.

If a defective track is found, defective track identifiers (CHRN field hexadecimal FFFFFFF) are written in all ID fields of that track. The track is written in an 8-record format.

The write sector ID operation is started by the control processor. The cylinder, head, starting record number, record format, and number of records to be written (CHRNX field) are specified to the attachment hardware by I/O load commands (IOL A), which load the hardware ID buffer.

The write clock drives the bit ring to supply bit and byte synchronization for the attachment write data output. The write circuits of the file control card are controlled by the write gate.

The sector sequence control and the track sequence control logic determine the physical location of the fields on the diskette.



The attachment waits for an index pulse to begin the operation.

The index pulse signals the attachment to turn on the write gate and the erase gate. The write gate and the erase gate condition the file control card write and erase circuits.

Gap 1 is written. For FM recording, 73 bytes of hexadecimal FF are written. For MFM recording, 146 bytes of hexadecimal 4E are written.

For FM recording, 6 bytes of zeros are written. For MFM recording, 12 bytes of zeros are written.

An ID address mark field is written. See Table 2.

The CHRN data from the ID buffer is written.

The 2 CRC bytes accumulated from the two fields following the sync field are written.

Gap 2 is written. For FM recording, 11 bytes of hexadecimal FF are written. For MFM recording, 22 bytes of hexadecimal 4E are written.

For FM recording, 6 bytes of zeros are written. For MFM recording, 12 bytes of zeros are written.

A data address mark is written. See Table 2.

Data is moved from the first data byte in the data area of main storage to the attachment data buffer by cycle steal in 2-byte bursts, until the specified record length is written.

The 2 CRC bytes accumulated from the two fields following the sync field are written.

The X-register (the ID buffer register that contains the number of records to be processed) is decreased at the beginning of the gap following the data field CRC. If all sectors are written, hardware writes gap 4 (the last gap before the index); if not, hardware writes gap 3.

Gap 3 is written. For FM recording, gap 3 is comprised of hexadecimal FFs. For MFM recording, gap 3 is comprised of hexadecimal 4Es. Gap length is dependent on the recording mode and the N field. See Table 1.

Gap 4 is written until the index. For FM recording, gap 4 is comprised of hexadecimal FFs. For MFM recording, gap 4 is comprised of hexadecimal 4Es.

Index is the signal to turn off the write gate.

Erase gate is turned off in gap 1 (after 18 bytes for FM, 36 bytes for MFM).

The attachment signals operation end by raising an interrupt level 4 request and returning control to the control processor.

See *Write Verify Operation* in this section.

Table 1
Number of Sectors in Track

Bytes in Data Field	N Field	FM	MFM	Gap 3 FM	Gap 3 MFM
128	0	26		27	
256	1		26		54
512	2	8		58	
1024	3		8		116
512	FF	8		58	
1024	FF		8		116

Table 2

AM 1		
MFM (hex)	FM (hex)	Explanation
A1 A1 A1 FE	FE	Field that follows is an ID field.
AM 2		
MFM (hex)	FM (hex)	Explanation
A1 A1 A1 F8	F8	Field that follows is a control field.
A1 A1 A1 FB	FB	Field that follows is a data field.

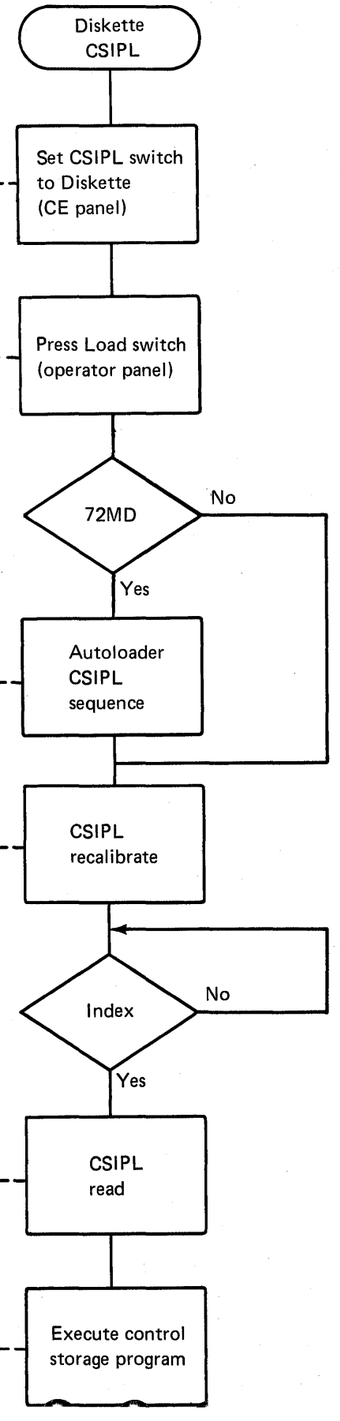
CSIPL Read Operation

This is an attachment hardware function, which is started by setting the CSIPL switch on the CE panel to the Diskette position and then pressing the Load switch on the operator panel.

If the diskette drive is a 72MD, the carriage bed is aligned with I/O slot 1, the diskette in that position is inserted into the drive, and the data heads are loaded. If the diskette drive is a 33FD or a 53FD, the data heads are loaded after recalibration.

A hardware-controlled recalibrate is executed to position the data head over track 00 with data head 0 selected. When the recalibrate is complete, the next index pulse starts the CSIPL read operation. A 4,096-byte (FM) record (record number 1) is read from track 00 and moved to control storage address hexadecimal 0000 through hexadecimal 07FF.

When this read operation is complete, the record just read is executed.



Selects the diskette, as opposed to the disk, as the source of the initial control storage program.

Pressing the Load switch causes a system reset, and an autoloader reset. Releasing the Load switch sets the 'CSIPL cycle' latch, an input to the attachment.

System reset, caused by pressing the Load switch, starts an orient command to the autoloader logic. An orient command causes any diskette in the drive to be ejected and the carriage bed to align I/O slot 1 with the drive. The 'CSIPL cycle' latch starts a select slot 1 command to the autoloader. This command causes the diskette in I/O slot 1 to be inserted into the drive and clamped to the drive hub. Completion of the select slot 1 command causes a load heads command, which loads the data heads and selects head 0.

Upon completion of the autoloader sequence, or following system reset if a 33FD or 53FD, the CSIPL recalibrate operation begins. The four stepper motor access lines from the attachment are controlled by a CSIPL counter. When the count = 83, the data head is positioned at cylinder 00 with the stepper motor access lines in the detent condition. (If the drive is a 33FD or a 53FD, the data head(s) are loaded at this time.)

When the recalibrate operation is completed, an index pulse begins the CSIPL read operation. 4,096 bytes of FM recorded data are moved from the diskette to control storage address hexadecimal 0000 through hexadecimal 07FF. The data is moved by cycle steal in 2-byte bursts. If no index pulse occurs, the Load light and all indicators in byte 0 on the CE panel remain on.

When 4,096 bytes are moved to the channel, the 'CSIPL cycle' latch becomes inactive, terminating the CSIPL operation. The control storage program begins execution.

Autoloader Operations

The autoloader operations are started in the attachment by:

- Activating the 500-kHz oscillator to the autoloader control logic
- Setting the '+enable autoloader' line to an up level
- Placing the needed command on the command bus

The autoloader actions are controlled in two ways. During a diskette CSIPL, the attachment hardware controls the aligning of the carriage bed to I/O slot 1, the inserting of the diskette in that position into the drive, and the loading of the data heads. For all other autoloader operations, the control processor and the attachment hardware are used.

Select Slot

During a select slot operation, if a diskette is in the drive, the heads are unloaded (if they were loaded) and the diskette is ejected. Then, the carriage bed is moved to the specified slot. At the specified slot, the diskette is moved into the drive by the picker arm and clamped to the hub. The heads are not loaded. The end of the operation is indicated by an 'op end' signal. If any condition prevents a select slot operation from completing, then an 'op end' signal and an 'error' signal are given.

Orient

During an orient operation, the picker is moved to the Picker Rest position and an eject operation is performed if a diskette is in the drive. The carriage bed is then aligned to I/O slot 1. The end of the operation is indicated by an 'op end' signal. If any condition prevents an orient operation from completing, then an 'op end' signal and an 'error' signal are given.

An orient operation must follow an abort operation or the next motion command will result in an error. It is recommended that an orient operation be done before a normal power off.

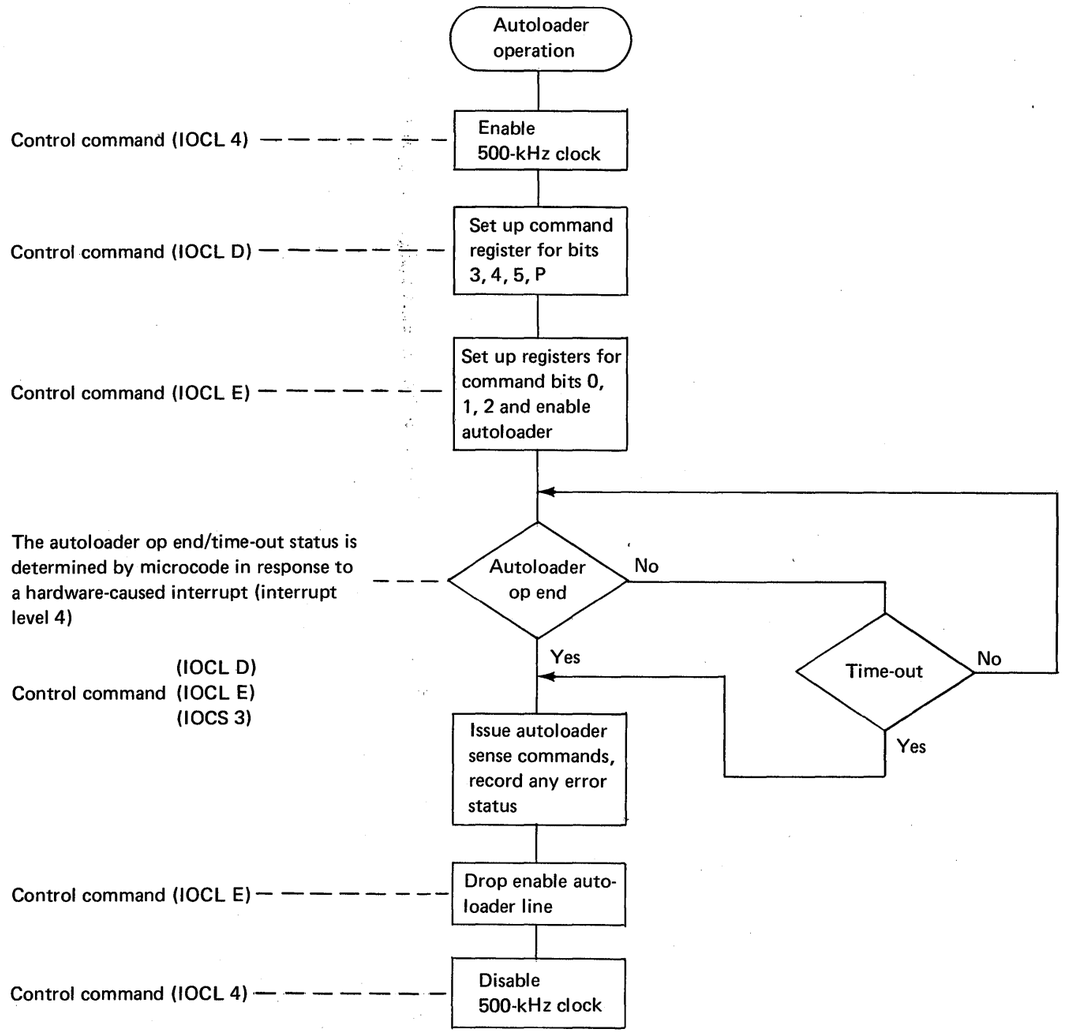
Eject

During an eject operation, the picker returns the diskette to the correct slot and then is moved to the Picker Rest position. The end of the operation is indicated by an 'op end' signal. If any condition prevents an eject operation from completing, then an 'op end' signal and an 'error' signal are given.

On machines with the new style picker, an eject operation moves the picker to the Picker Rest position (returning the diskette to its slot). The end of the operation is indicated by an 'op end' signal. No error indications are given during an eject operation.

Abort

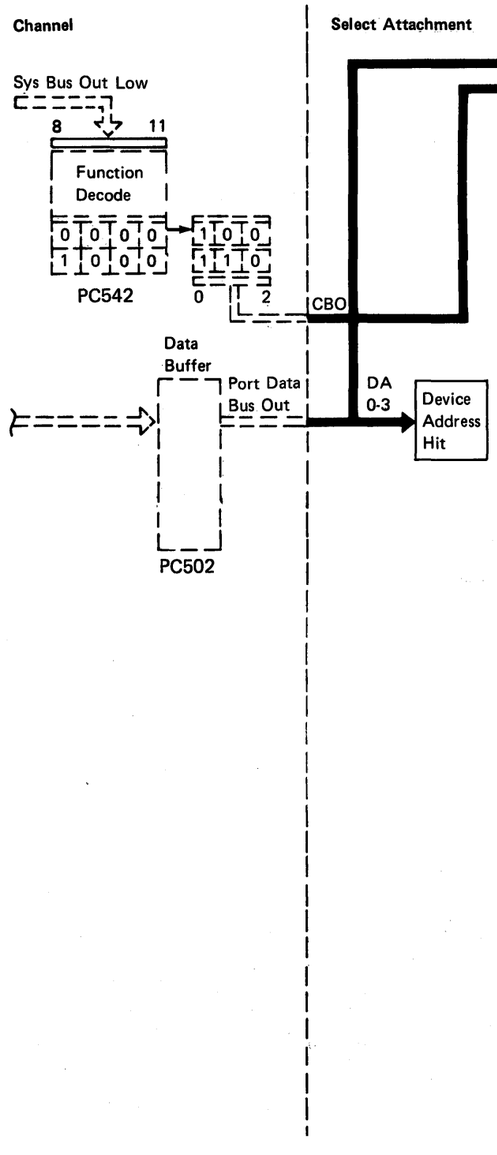
An abort operation resets the autoloader logic, similar to a power-on-reset operation to the autoloader logic.



COMMANDS

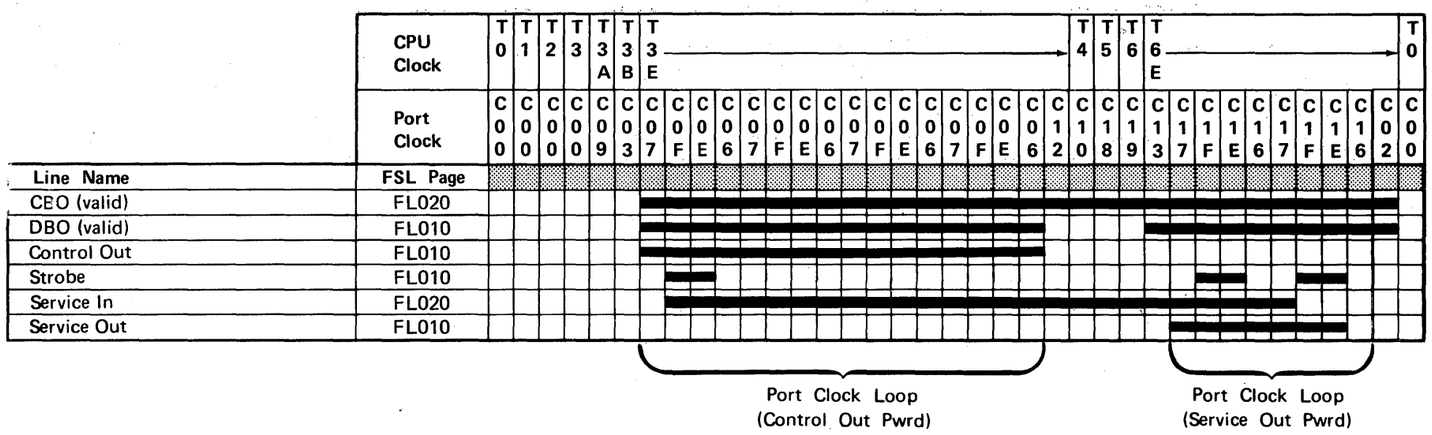
I/O Load Command—I/O Control Load Command

These commands send 1 byte of information from the control processor to the attachment. See *Commands* in the *Channel* section of this manual for a description of how this command is executed.



CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
100 I/O Load	0 0 0 0 Op End Control							Enable/disable op end interrupt, reset op end latch	
	0 0 1 1 Reset Interruot Request	Immediate command (resets IL 4 latch and 7680 ms time-out latch)							
	0 1 0 1 Reset Checks/Data Mode Control 1		Inhibit address increment	Inhibit standard read clocks/data	0 = Main storage 1 = Control storage		0 = Sense 1 = Load		
	0 1 1 0 Enable Interrupt Request						Enable/disable IL 4 requests to channel		Enable/disable time-out interrupt, reset counter
	1 0 0 1 Load Data Buffer	Input buffer							
	1 0 1 0 Load ID buffer	X-reg buffer							
	1 1 0 0 Diagnostic Mode Control 0	CE wrap fast sync on zeros		CE wrap 1's	CE ID hit	CE sector ID	CE AM/data field	CE data/CRC field	CE CRC/gap field
	1 1 1 1 Diagnostic Mode Control 1	CE cycle steal trigger	CE FD strobe	CE 100-ns oscillator	CE 1-µs oscillator	CE clock	CE data	CE 8F	CE 512-µs oscillator
110 I/O Control Load	0 0 0 1 Enable Diagnostic Mode	CE CSIPL latch	CE wrap mode latch	CE step mode latch		Program attachment reset	Program autoloader reset		
	0 0 1 0 Data Mode Control 2	0 = FM 1 = MFM	Write flagged track	Inhibit 8F read oscillator		1 = rd/wr MSIPL (DCP only)	Op decode* bit 5	Op decode* bit 6	Op decode* bit 7
	0 1 0 0 Physical Mode Control					Enable/disable 33FD stepper motor lines	Enable/disable 2-µs clock for autoloader op	Diskette working	33FD/53FD load heads
	0 1 1 1 Stepper Motor							Stepper motor phase (binary 2)	Stepper motor phase (binary 1)
	1 0 1 1 Diagnostic Mode Control 2					Increment byte counter by 256	Increment byte counter by 16	Increment byte counter with 1-µs clock	CE index
	1 1 0 1 Autoloader Mode Command 0					Autoloader command bit 3	Autoloader command bit 4, switch filter	Autoloader command bit 5, inner tracks	Autoloader command bit P, select head 1
	1 1 1 0 Autoloader Mode Command 1					Enable autoloader	Autoloader command bit 0	Autoloader command bit 1	Autoloader command bit 2

*See *Op Decode* under *Functional Units* later in this section.



I/O Load Command

Modifier (DBO 4-7)	DBO Bits	Command	Action Taken	FSL Page
0 0 0 0	6	Op end control	Enables and disables the 'op end interrupt' latch and resets the 'op end' latch.	FL071
0 0 1 1	–	Reset interrupt request	Resets the 'interrupt level 4 request' latch and the '8-ms time-out' latch.	FL071
0 1 0 1	1-3, 5	Reset checks/data mode control 1	Resets all attachment error latches and sets the 'diskette ready' latch if the diskette is turning at the correct speed. Sets attachment logic conditions, which are operation dependent, for data operations.	FL061
0 1 1 0	5, 7	Enable interrupt request	Enables and disables the 'interrupt level 4 request' latch to the channel. Enables and disables and resets the '8-ms time-out' latch used for interrupt logic.	FL071
1 0 0 1	0-7	Load data buffer	Diagnostic use only. Loads 1 byte of data into the attachment data buffer.	FL351
1 0 1 0	0-7	Load ID buffer	Loads the attachment ID buffer with CHRNX data, 1 byte at a time.	FL250
1 1 0 0	0, 2-7	Diagnostic mode control 0	Conditions various logic functions for diagnostic purposes.	FL063
1 1 1 1	0-7	Diagnostic mode control 1	Conditions various logic functions for diagnostic purposes.	FL063

I/O Control Load Command

Modifier (DBO 4-7)	DBO Bits	Command	Action Taken	FSL Page
0 0 0 1	0-2, 4, 5	Enable diagnostic mode	Conditions various logic functions for diagnostic purposes.	FL061
0 0 1 0	0-2, 4-7	Data mode control 2	Sets control latches that define the data operation.	FL062
0 1 0 0	4-7	Physical mode control	Sets control latches that enable or cause motion in the diskette drive.	FL061 FL540
0 1 1 1	6, 7	Stepper motor	Controls the head access stepper motor drive lines to move the data head(s) one track in either direction.	FL550
1 0 1 1	4-7	Diagnostic mode control 2	Conditions various logic functions for diagnostic purposes.	FL063
1 1 0 1	4-7	Autoloader mode command 0	Sets latches that define the autoloader command if in autoloader mode, or drive functions if not in autoloader mode.	FL550
1 1 1 0	4-7	Autoloader mode command 1	Sets latches to enable the autoloader and define the autoloader commands.	FL550

Autoloader Mode Commands

The autoloader command lines (bits 4 through 7 of an IOCL D and bits 5 through 7 of an IOCL E) are used to describe autoloader operations. These six command lines and one parity line make the command codes shown in the chart.

Autoloader Mode Command Codes IOCL E		IOCL D		Meaning	
Bits	5 6	7 4 5 6	7		
	0 0	0 0 0 0	1	I/O Slot 1	
	0 0	0 0 0 1	0	I/O Slot 2	
	0 0	0 0 1 0	0	I/O Slot 3	
	0 0	0 0 1 1	1	Reserved	
	0 0	0 1 0 0	0	Reserved	
	0 0	0 1 0 1	1	Magazine 1	Slot 1
	0 0	0 1 1 0	1		Slot 2
	0 0	0 1 1 1	0		Slot 3
	0 0	1 0 0 0	0		Slot 4
	0 0	1 0 0 1	1		Slot 5
	0 0	1 0 1 0	1		Slot 6
	0 0	1 0 1 1	0		Slot 7
	0 0	1 1 0 0	1		Slot 8
	0 0	1 1 0 1	0		Slot 9
	0 0	1 1 1 0	0		Slot 10
	0 0	1 1 1 1	1	Reserved	
	0 1	0 0 0 0	0	Reserved	
	0 1	0 0 0 1	1	Reserved	
	0 1	0 0 1 0	1	Magazine 2	Slot 1
	0 1	0 0 1 1	0		Slot 2
	0 1	0 1 0 0	1		Slot 3
	0 1	0 1 0 1	0		Slot 4
	0 1	0 1 1 0	0		Slot 5
	0 1	0 1 1 1	1		Slot 6
	0 1	1 0 0 0	1		Slot 7
	0 1	1 0 0 1	0		Slot 8
	0 1	1 0 1 0	0		Slot 9
	0 1	1 0 1 1	1		Slot 10
	0 1	1 1 0 0	0	Reserved	
	0 1	1 1 0 1	1	Reserved	
	0 1	1 1 0 1	1	Reserved	
	0 1	1 1 1 0	1	Reserved	

Autoloader Mode Command Codes IOCL E		IOCL D		Meaning
Bits	5 6	7 4 5 6	7	
	1 0	0 0 0 0	0	Not Valid
	1 0	0 0 0 1	1	Not Valid
	1 0	0 0 1 0	1	Not Valid
	1 0	0 0 1 1	0	Not Valid
	1 0	0 1 0 0	1	Not Valid
	1 0	0 1 0 1	0	Not Valid
	1 0	0 1 1 0	0	Not Valid
	1 0	0 1 1 1	1	Not Valid
	1 0	1 0 0 0	1	Not Valid
	1 0	1 0 0 1	0	Not Valid
	1 0	1 0 1 0	0	Orient
	1 0	1 0 1 1	1	Eject
	1 0	1 1 0 0	0	Load Heads
	1 0	1 1 0 1	1	Unload Heads
	1 0	1 1 1 0	1	Reset Sense
	1 0	1 1 1 1	0	Abort
	1 1	0 0 0 0	1	Not Specified
	1 1	0 0 0 1	0	Not Specified
	1 1	0 0 1 0	0	Not Specified
	1 1	0 0 1 1	1	Not Specified
	1 1	0 1 0 0	0	Not Specified
	1 1	0 1 0 1	1	Not Specified
	1 1	0 1 1 0	1	Not Specified
	1 1	0 1 1 1	0	Not Specified
	1 1	1 0 0 0	0	Sense 0
	1 1	1 0 0 1	1	Sense 1
	1 1	1 0 1 0	1	Sense 2
	1 1	1 0 1 1	0	Sense 3
	1 1	1 1 0 0	1	Sense 4
	1 1	1 1 0 1	0	Sense 5
	1 1	1 1 1 0	0	Not Specified
	1 1	1 1 1 1	1	Not Specified

Notes:

1. A reserved command causes the carriage bed to be stopped at the reserved slot and the picker to attempt to pick a diskette. This causes a fail-to-pick error.
2. A not-specified command gives not-known results.

Select Diskette

The select diskette command causes the autoloader to select a diskette from one of the 23 slots. If a diskette is in the drive, the autoloader first ejects that diskette to its slot. The autoloader then selects the correct diskette.

The diskette to be selected is specified in a 1-byte data control field located in control storage. This byte must be loaded before a select diskette command is issued. The autoloader logic receives the information from this byte on seven control bus lines from the attachment. The 23 slots and the value that must be placed in the data control field are shown in the chart.

Orient

The orient autoloader command ejects the diskette, if one is present, from the drive and moves the carriage to the home position, I/O slot 1.

Eject

The eject command causes the autoloader to eject the diskette from the drive into the proper slot.

Load Heads

The load heads command causes the data heads to be loaded.

Unload Heads

The unload heads command causes the data heads to be unloaded.

Reset Sense

The reset sense command causes the following latches to be reset:

- Command reject
- Motion check
- Not valid command
- Check modifier code
- Oriented

Abort

The abort command resets the autoloader logic. This command must be used for some error recovery action.

Sense 0 through Sense 5

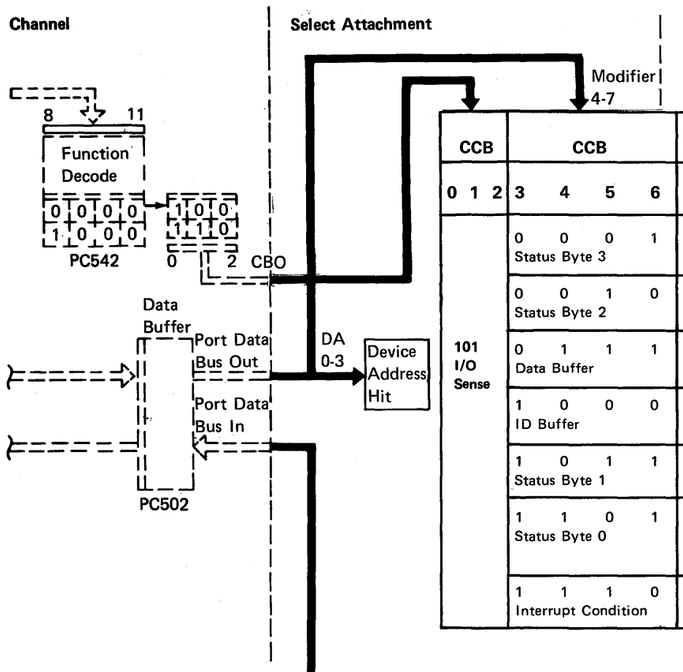
These sense commands cause the following sense information to be displayed on the autoloader status lines.

Command Code (hex)	Autoloader Status A	Autoloader Status B	Autoloader Status C	Autoloader Status D
38	Command Reject	Motion Check	Not Valid Command	
39	Check Modifier Codes			
3A	Diskette Window Open[1]	Picker	Diskette In	Carriage Bed Orient
3B		Oriented Latch	Cover Open	
3C	Head Access Latch 0	Head Access Latch 1	Head Access Latch 2	Head Access Latch 3
3D	Autoloader Access 0	Autoloader Access 1	Autoloader Access 2	Autoloader Access 3

[1] Applies only for machines with the old style picker.

I/O Sense Command—I/O Control Sense Command

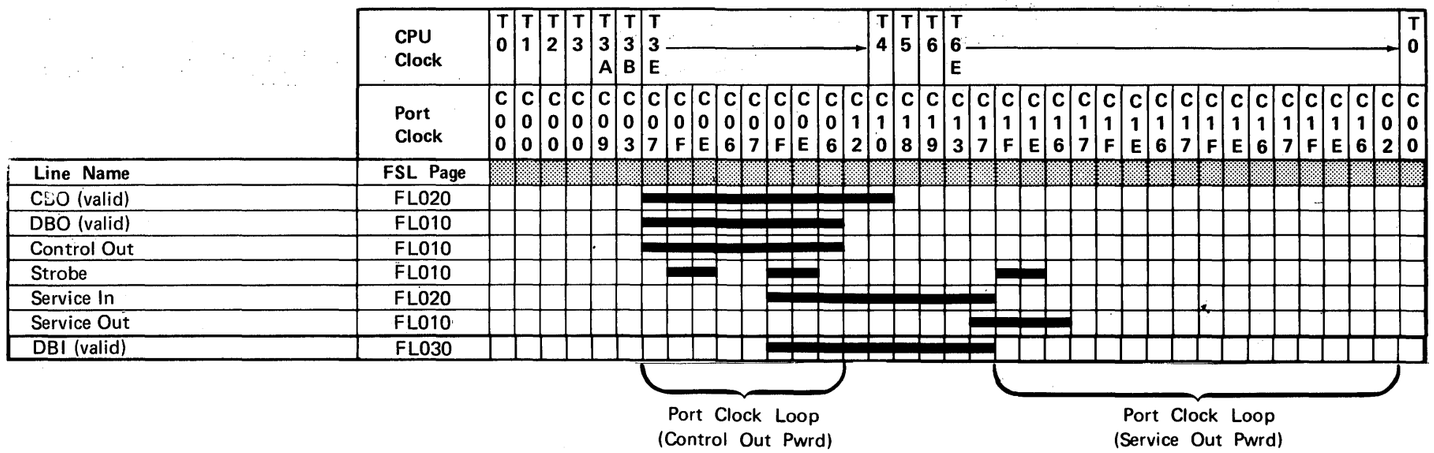
These commands send 1 byte of information from the attachment to the control processor. See *Commands* in the *Channel* section of this manual for a description of how this command is executed.



CCB 0 1 2	CCB 3 4 5 6	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
101 I/O Sense	0 0 0 1 Status Byte 3	Data unsafe		Drive type	Erase current off	Head 0 selected	Diskette type		Diskette not busy
	0 0 1 0 Status Byte 2	Fast check	Diskette not ready	Missing erase current	ID not found	Buffer underrun	Data mode	Buffer overrun	
	0 1 1 1 Data Buffer	Output buffer							
	1 0 0 0 ID Buffer	C-reg buffer							
	1 0 1 1 Status Byte 1	No op condition	Not valid control record found	Write verify mismatch	Control address mark found		Write error	End of track	Channel busy
	1 1 0 1 Status Byte 0	Missing data address mark (see Note 1)		Data cyclic redundancy check (see Note 1)	Cylinder mismatch (see Note 1)				Seek reverse
	1 1 1 0 Interrupt Condition			Op end	Time-out				
111 I/O Control Sense	0 0 0 0 Control Sense	360 RPM	Speed check counter	CSIPL count = 83	Read clock latch				
	0 0 1 1 Drive Sense 1	Autoloader op end, autoloader status A (see Note 2)	2-sided dskt, autoloader status B (see Note 2)	Erase sense, auto-loader status C (see Note 2)	Autoloader wrap-back, autoloader status D (see Note 2)	Not CSIPL latch	Not autoloader reset	Select low byte	FM mode
	0 1 0 1 Data Separator and Write Control	Not find bit sync on 0's	Not index	Not CE wrap mode to drive sense	Not CE wrap data to drive sense	Write data/auto-loader 2-µs clock	Not erase gate	Not write gate	Not load read/ write head (33FD/53FD)
	0 1 1 0 Device Interface	Enable autoloader	Not autoloader command 0, not step 3/0	Not autoloader command 1, not step 0/1	Not autoloader command 2, not step 1/2	Not autoloader command 3, not step 2/3	Not autoloader command 4, not switch filter	Not autoloader command 5, not inner tracks	Not autoloader command P, not select head 1
	1 0 0 1 Diagnostic Sense	Bit rings 1-4	Bit rings 2-5	Bit rings 3-6	Bit rings 4-7	CRC = 0	Not CRC register 16	Read/write clock 0/1	Not read/write clock 1/2
	1 1 0 0 Track Sequence Control	Not gap 1 sector	Sector ID	Not end of field	Not gap 4 sector				
	1 1 1 1 Sector Sequence Control	Not gap field	Sync field	Not AM field	Not data, not CHRN field	Not CRC field	Not ID hit	Byte counter = 0	

Notes:

1. If byte 1 bit 0 is on, byte 0 bits 0-3 are coded by microcode to describe the error.
2. Bits 0-3 of drive sense 1 are sensed four times to become status bytes 4 and 5.



I/O Sense Command

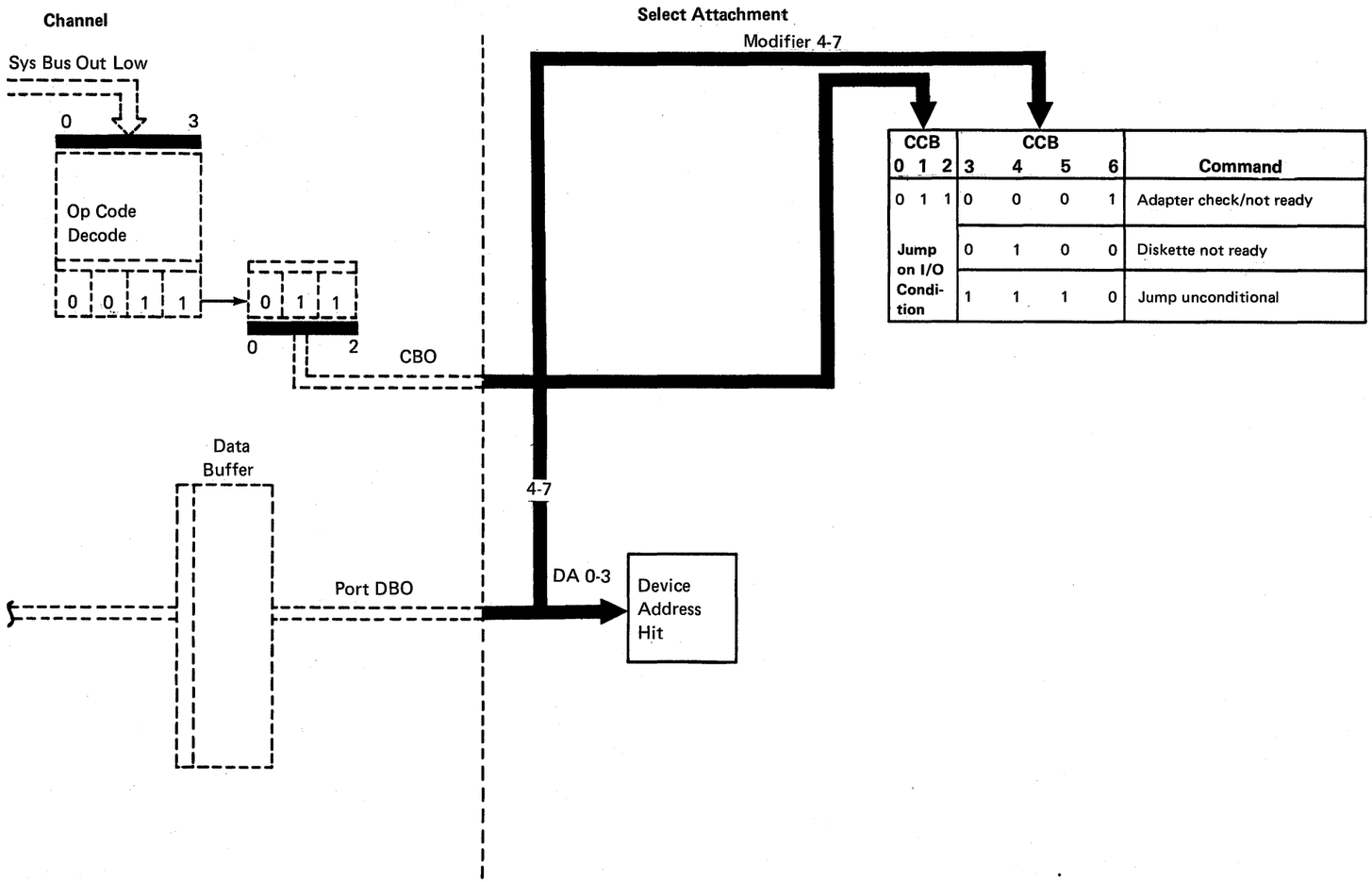
Modifier (DBO 4-7)	DBI Bits	Command	Action Taken	FSL Page
0 0 0 1	0, 2-5, 7	Status byte 3	Sends 1 byte of status information from the attachment to the control processor.	FL131
0 0 1 0	0-7	Status byte 2	Sends 1 byte of status information from the attachment to the control processor.	FL131
0 1 1 1	0-7	Data buffer	Sends 1 byte of data from the attachment data buffer to the control processor.	FL131
1 0 0 0	0-7	ID buffer	Sends 1 byte of data from the ID buffer to the control processor.	FL131
1 0 1 1	0-3, 5-7	Status byte 1	Sends 1 byte of status information from the attachment to the control processor.	FL131
1 1 0 1	0-7	Status byte 0	Sends 1 byte of status information from the attachment to the control processor.	FL131
1 1 1 0	2, 3	Interrupt condition	Sends 1 byte of status information, relating to the condition of the interrupt logic, from the attachment to the control processor.	FL131

I/O Control Sense Command

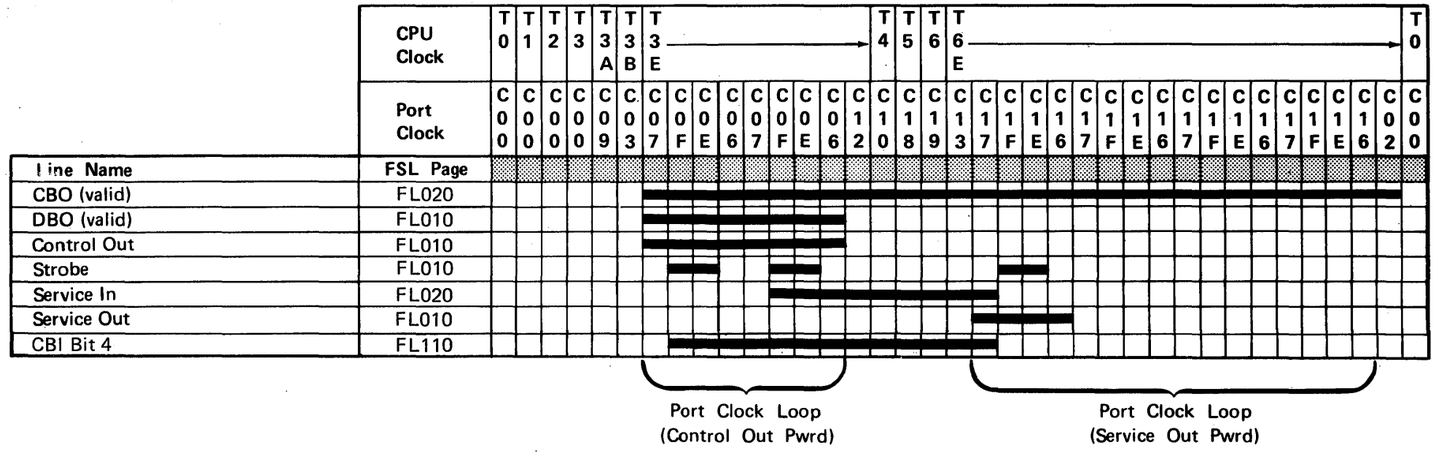
Modifier (DBO 4-7)	DBO Bits	Command	Action Taken	FSL Page
0 0 0 0	0-3	Control sense	Sends 1 byte of status information from the attachment to the control processor.	FL130
0 0 1 1	0-7	Drive sense 1	Sends 1 byte of diskette drive or autoloader status information from the attachment to the control processor.	FL130
0 1 0 1	0-7	Data separator and write control	Sends 1 byte of information, relating to the data separator and the write logic functions, to the control processor.	FL130
0 1 1 0	0-7	Device interface	Sends 1 byte of attachment/diskette drive interface information to the control processor.	FL130
1 0 0 1	0-7	Diagnostic sense	Sends 1 byte of clock ring, bit ring, and CRC register status information to the control processor.	FL130
1 1 0 0	0-3	Track sequence control	Sends 1 byte of track sequence control status information to the control processor.	FL130
1 1 1 1	0-6	Sector sequence control	Sends 1 byte of sector sequence control status information to the control processor.	FL130

Jump on I/O Condition Command

The jump on I/O condition command tests the attachment for a specific condition. If the condition is active, the attachment activates the 'CBI bit 4' line to the control processor to indicate a positive result. See *Commands* in the *Channel* section of this manual for a description of how this command is executed.



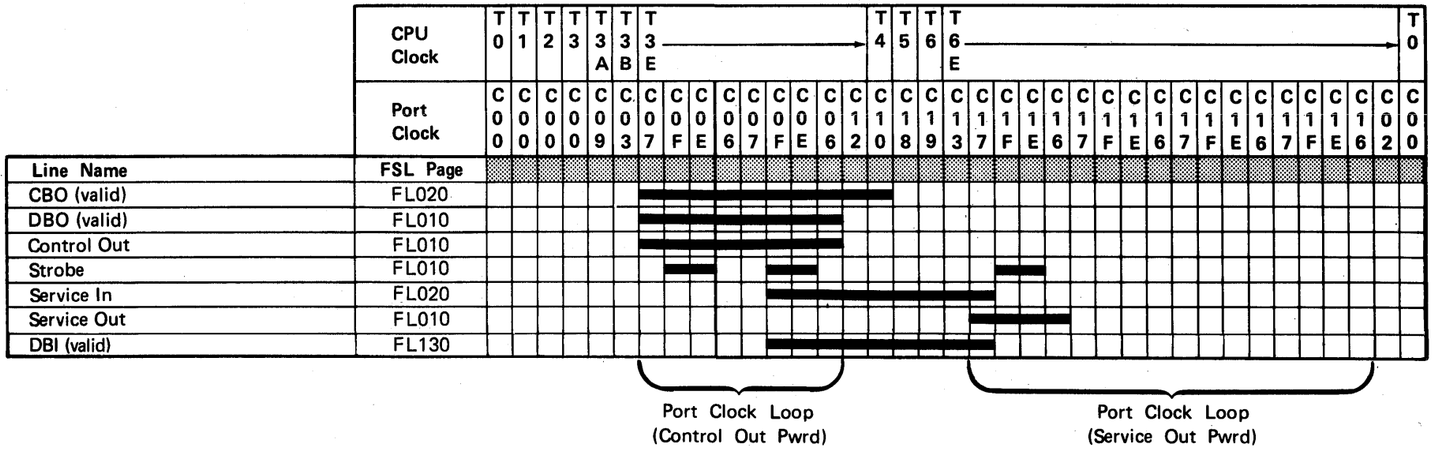
CCB 0 1 2	CCB 3	4	5	6	Command
0 1 1	0	0	0	1	Adapter check/not ready
Jump on I/O Condition	0	1	0	0	Diskette not ready
	1	1	1	0	Jump unconditional

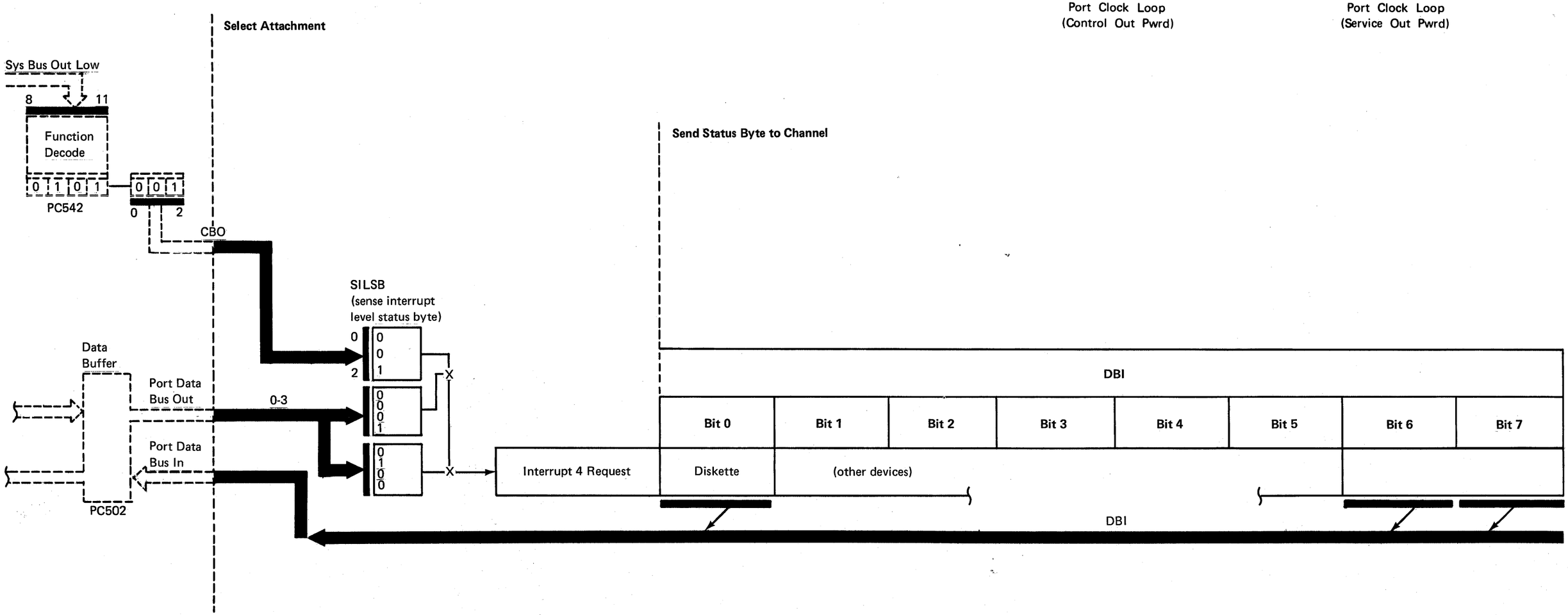


Modifier (DBO 4-7)	CBI Bit	Condition Tested	Action Taken	FSL Page
0 0 0 1	4	Adapter check/ not ready	Tests for the following conditions: Unexpected erase current present Fast check Not ready Diskette not ready Missing erase current ID not found Buffer underrun Buffer overrun Not valid control record check Write verify mismatch Missing data address mark Data cyclic redundancy check Cylinder mismatch If any of these conditions is found, CBI bit 4 is sent to the control processor.	FL120
0 1 0 0	4	Diskette not ready	Tests the 'diskette ready' latch. If the latch is off, CBI bit 4 is sent to the control processor.	FL560
1 1 1 0	4	Jump unconditional	CBI bit 4 is sent to the control processor.	FL120

Sense Interrupt Level Status Byte Command

The sense interrupt level status byte command senses all interrupt requests on either interrupt level 1 or interrupt level 4. All attachments that use interrupt level 1 or interrupt level 4 will respond. The control storage program uses this information to decide which attachment to service. A diskette interrupt level 4 request indicates that the attachment has completed an operation started by the control storage program or that an error or time-out has occurred during an operation.



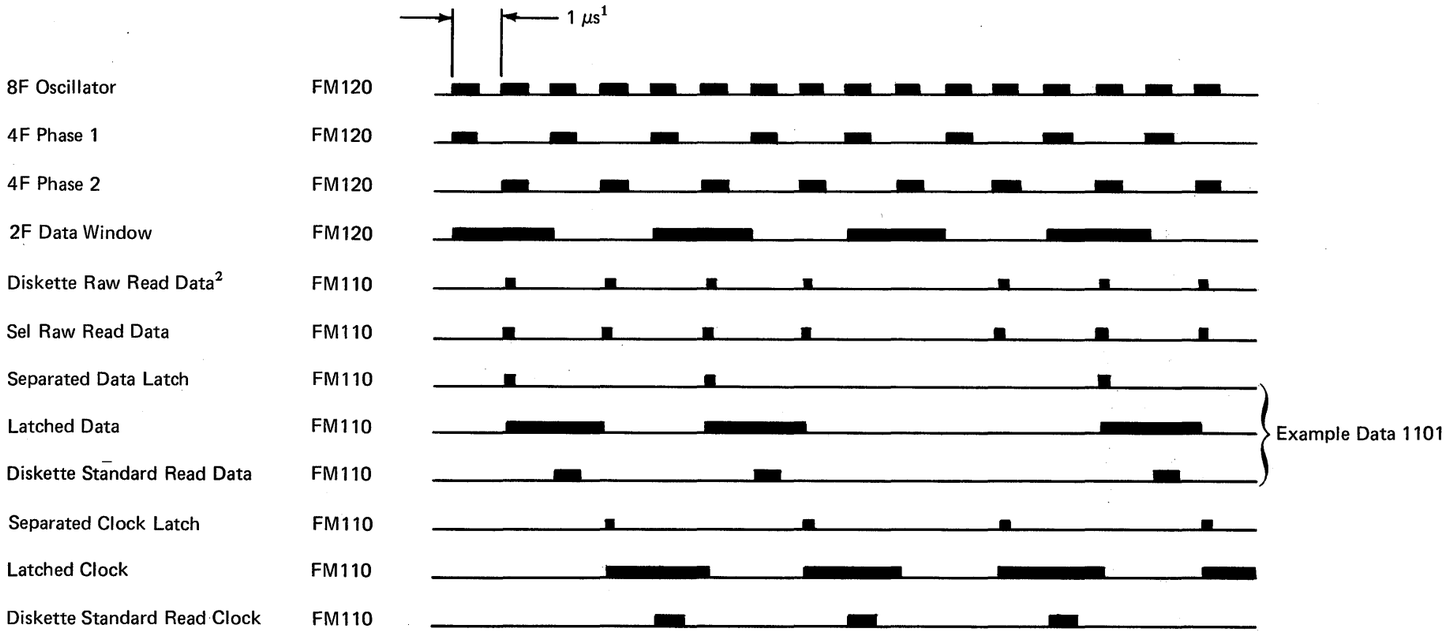


Functional Units

Data Separator

The data separator separates data pulses from clock pulses.

The data separator oscillators are synchronized with the 'diskette raw read data' line from the diskette. This bit synchronization is completed when a diskette sync field (6 bytes of zeros for FM mode or 12 bytes of zeros for MFM mode) is read. As a result, data pulses occur when the 'data window' line is active and clock pulses occur when the 'data window' line is not active.



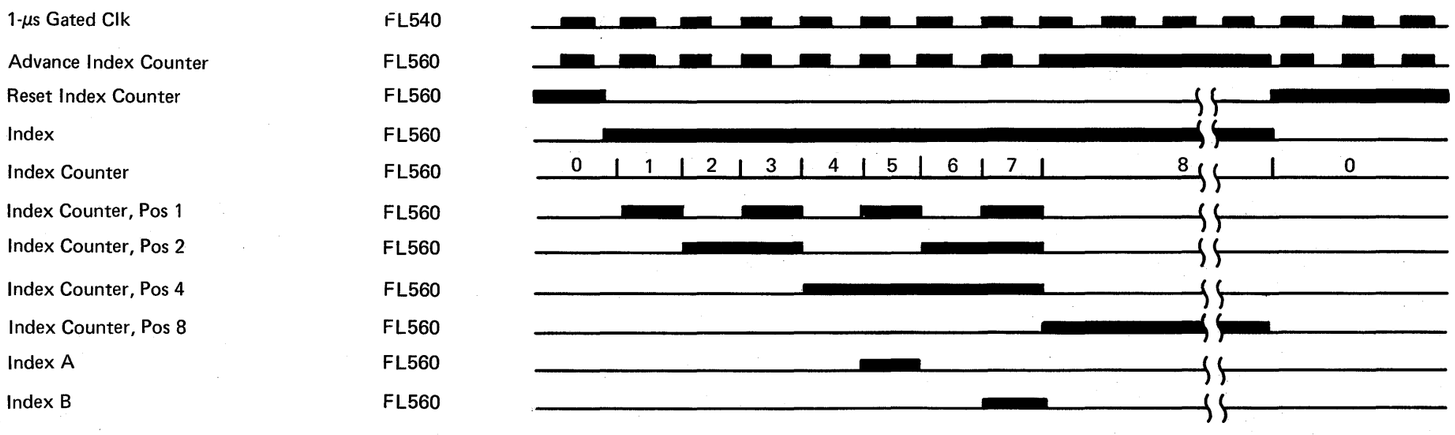
[1] The 8F oscillator frequency shown is for FM recording on a 360 revolutions per minute drive. This frequency is dependent on the drive used:

1 microsecond for FM recording on a 360 revolutions per minute drive
0.5 microsecond for MFM recording on a 360 revolutions per minute drive
0.5 microsecond for FM recording on a 720 revolutions per minute drive
0.25 microsecond for MFM recording on a 720 revolutions per minute drive

[2] FM data is shown. The data separator operates the same for MFM data.

Index Counter

The index counter is an attachment card function. The index counter is used to generate the 'index A' and 'index B' timing pulses from the diskette 'index' signal. The attachment rejects any index pulse shorter than 4 microseconds. The counter is held reset until an index occurs. Then, the counter advances with a 1-microsecond clock to a count of 8 and remains at this count until the 'index' line falls. If the 'index' line is not active at a count of 4, the counter is reset and no index is recognized.



Ready Counter

The ready counter is a binary counter that is used to check the speed of the diskette. It is reset each time an index pulse is sensed. Between index pulses, the ready counter is permitted to advance with each pulse from the 512-microsecond oscillator.

The output of the counter is sent to the speed check control circuits, which determine whether the diskette is running too quickly or too slowly. See FSL page FL560.

Control Storage Initial Program Load Track Counter

This counter controls the recalibrate operation during control storage initial program load. This counter also counts the number of one-track seeks (83) and controls the bits being set in the seek track register (each counter advance is a one-track seek).

The counter is held reset during a CSIPL operation until the autoloader sequence is completed. At this time, the counter is enabled and advances at each index phase B time. The counter also advances when specific ready counter values are decoded:

33FD Two advances per revolution (index plus 1 at 64 milliseconds)

53FD Nine advances per revolution (index plus 1 every 16 milliseconds for 128 milliseconds)

72MD Nine advances per revolution (index plus 1 every 8 milliseconds for 64 milliseconds)

See FSL page FL560.

CSIPL Autoloader Sequence

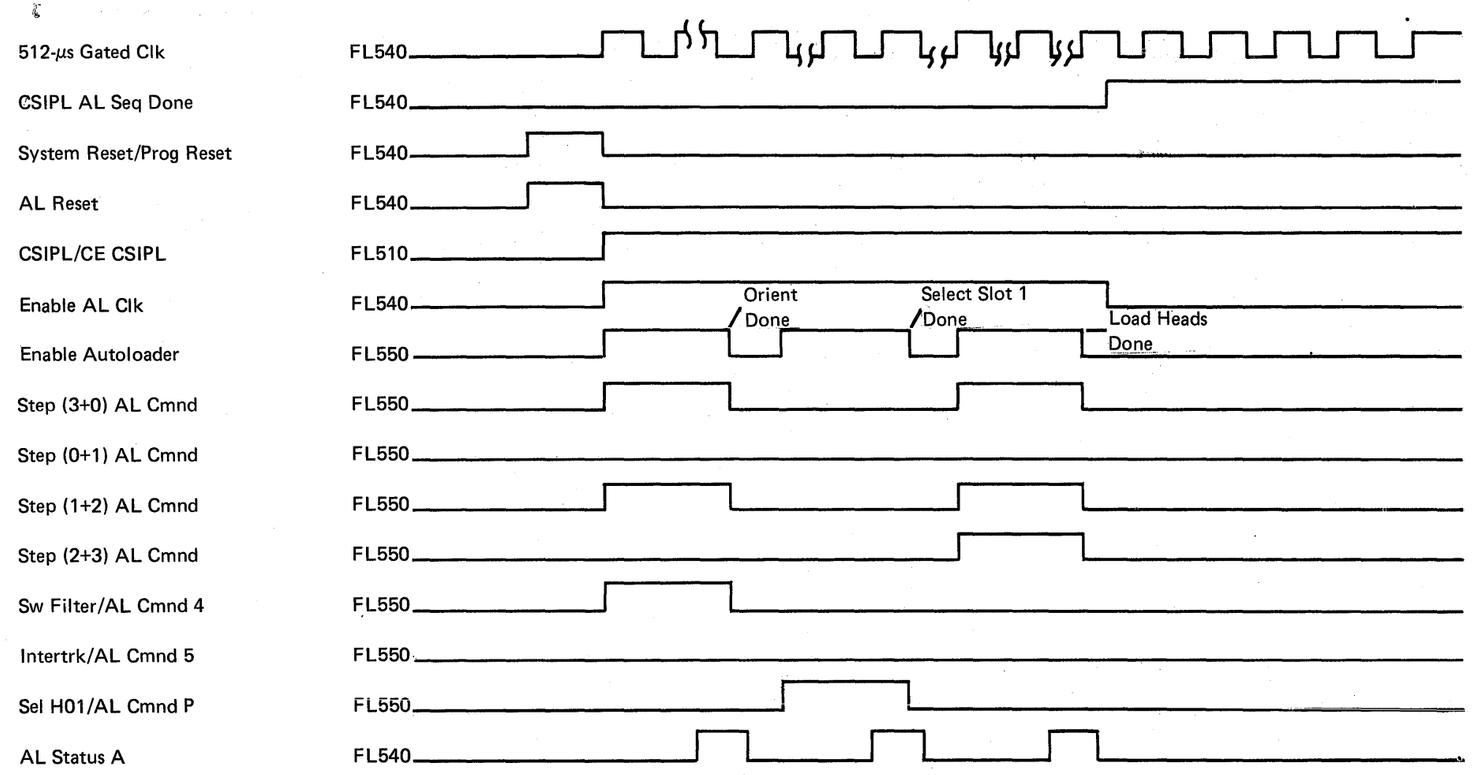
If the diskette drive is a 72MD, the CSIPL operation first selects and inserts a diskette into the drive. These functions, as well as the load heads function, are autoloader operations and are controlled by the attachment CSIPL autoloader sequence logic.

Pressing the Load switch causes a system reset. Releasing the Load switch sets the 'CSIPL/CE CSIPL' line. If the CSIPL switch on the CE panel is set to the Diskette position, pressing the Load switch starts the autoloader sequence.

The sequence is:

1. Align the diskette in I/O slot 1 with the diskette drive (first eject any diskette in the drive).
2. Insert the diskette in I/O slot 1 into the diskette drive.
3. Load the data heads.
4. Signal CSIPL sequence complete so a recalibrate function will be executed.

Autoloader command logic switches with a 512-microsecond clock pulse when the logic conditions are suitable.

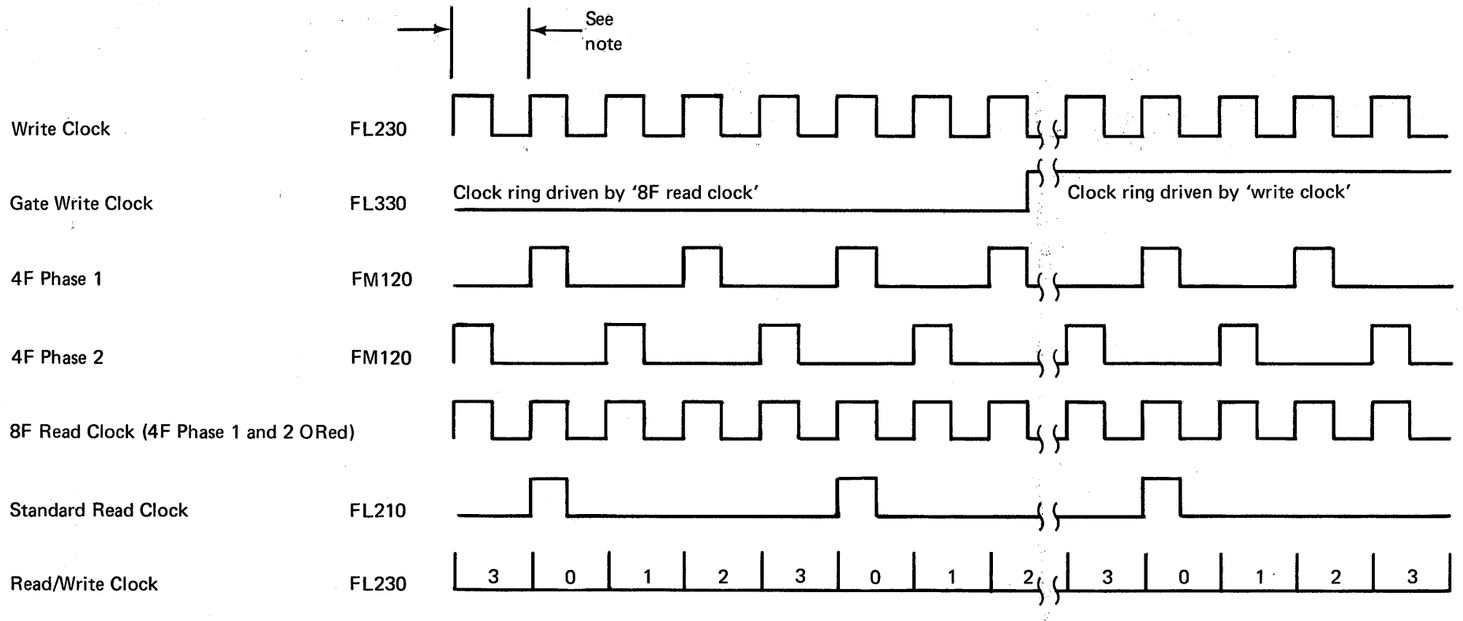


Read/Write Clock

This attachment logic generates clock timings for read and write operations.

The clock ring is driven by the '4F phase 1' and the '4F phase 2' read clocks from the data separator, except when the 'gate write clock' line is active. The 'gate write clock' line is active during gap fields and while the 'write gate' latch is on during write or initialize operations. During these times, the write clock drives the clock ring.

The clock ring is reset by system reset, or by the 'standard read clock' signal from the data separator if the 'gate write clock' line is not active.



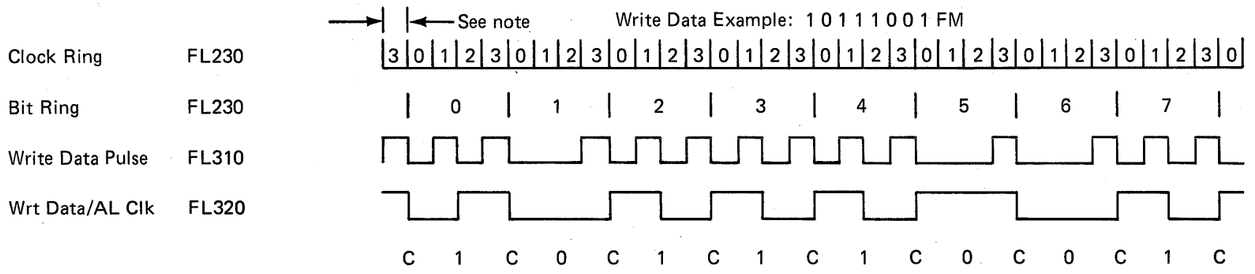
Note: The frequencies of the write clock and the 8F read clock are dependent on drive speed and recording mode:

33FD/53FD (FM)	= 1 μs	72MD (FM)	= 0.5 μs
33FD/53FD (MFM)	= 0.5 μs	72MD (MFM)	= 0.25 μs

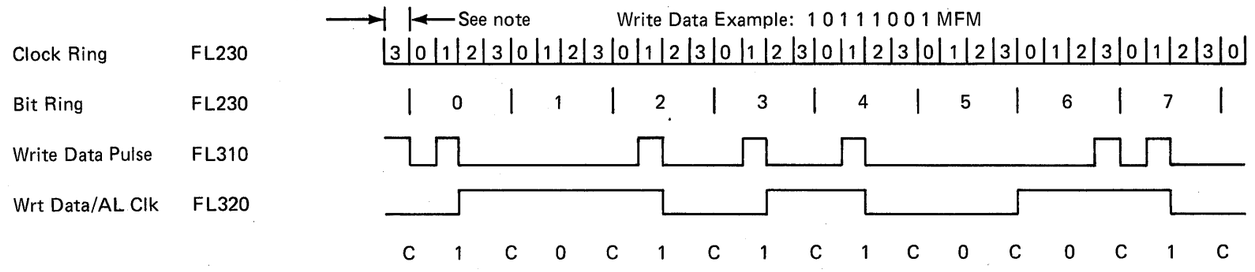
Write Trigger

The write trigger logic codes bits of information into serial bit cells. Each bit cell has one possible clock transition and one possible data transition. For FM encoding, each bit cell contains a clock transition. An FM bit cell contains a data transition for a 1-bit and no data transition for a 0-bit. For MFM encoding, the bit cell data transitions are the same as for FM encoding. Each MFM bit cell that has no data transition (0-bit), and is preceded by a bit cell that has no data transition, contains a clock transition.

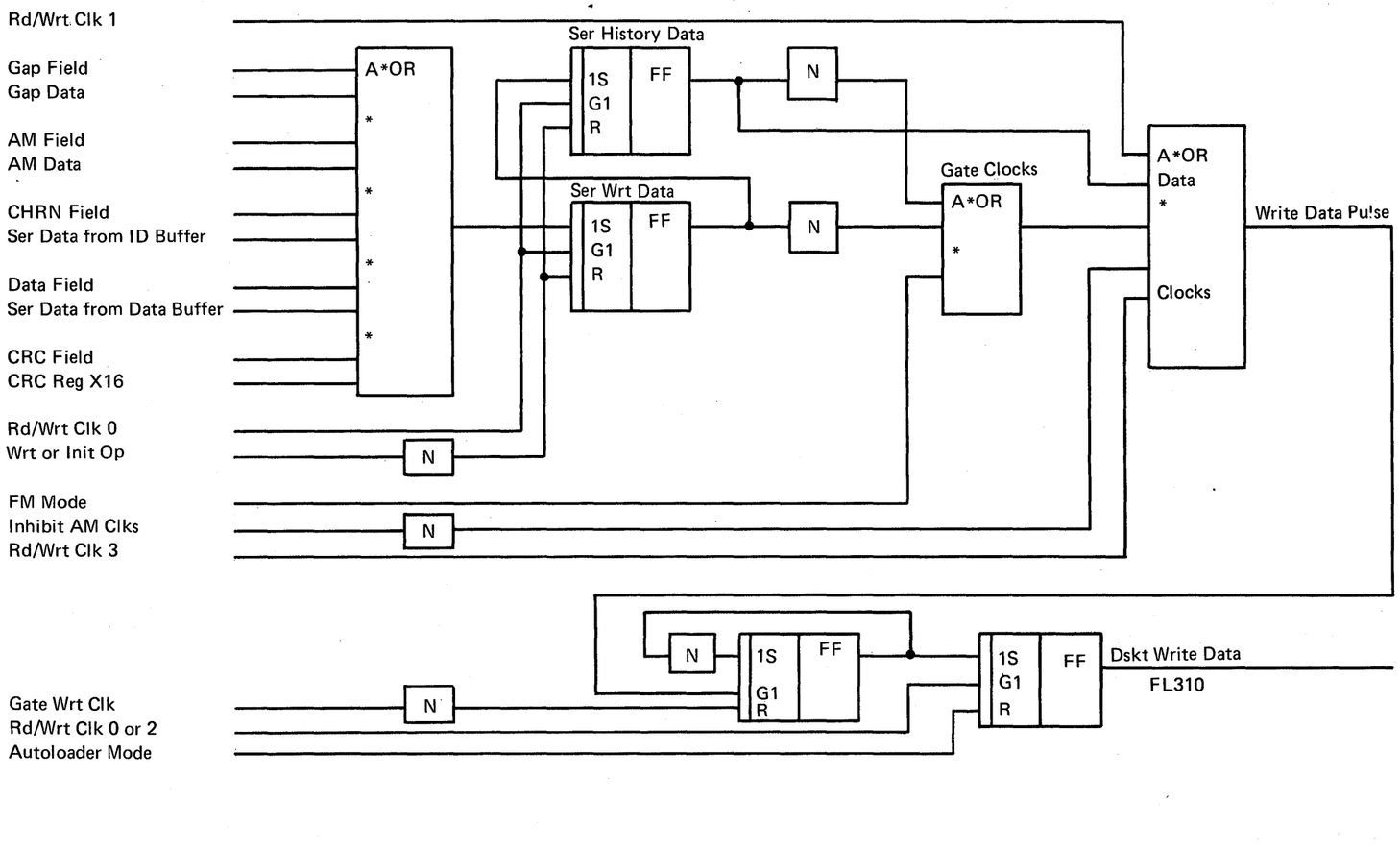
The write trigger logic uses sector sequence control conditions (diskette field information) to gate the suitable serial data to the write trigger. Clock gating is dependent on the recording mode, preceding and present data, and the clock needs of the address mark.



Note: 1 μs for 33FD or 53FD, 0.5 μs for 72MD.



Note: 0.5 μs for 33FD or 53FD, 0.25 μs for 72MD.


Rd/Wrt Clk 1
Gap Field
Gap Data
AM Field
AM Data
CHRN Field
Ser Data from ID Buffer
Data Field
Ser Data from Data Buffer
CRC Field
CRC Reg X16
Rd/Wrt Clk 0
Wrt or Init Op
FM Mode
Inhibit AM Clks
Rd/Wrt Clk 3
Gate Wrt Clk
Rd/Wrt Clk 0 or 2
Autoloader Mode
A*OR
*
*
*
*
N
N
N
N
Ser History Data
1S
G1
R
FF
Ser Wrt Data
1S
G1
R
FF
Gate Clocks
A*OR
*
A*OR
Data
*
Clocks
Write Data Pulse
N
1S
G1
R
FF
1S
G1
R
FF
Dskt Write Data
FL310

Address Mark Detection

When the sector sequence control logic is in the AM field condition:

- The read data is tested to ensure that it is an address mark.
- The type of address mark is determined.

For FM recording, a valid address mark is a 1-byte field with 1's in bit positions 0 through 4 and missing clock pulses in bit positions 2 through 4.

For MFM recording, a valid address mark is a 4-byte field. The first 3 bytes are hexadecimal A1's with a missing clock bit in bit position 5. The fourth byte has 1's in bit positions 0 through 4, as in an FM address mark.

The types of address marks are:

MFM (Hex)	FM (Hex)	Definition
A1 A1 A1 FE	FE	Field that follows is an ID field
A1 A1 A1 F8	F8	Field that follows is a control field
A1 A1 A1 FB	FB	Field that follows is a data field

If the address mark is found to be not valid (different from the above definition or a data address mark is decoded when an ID address mark is expected), the sector sequence control logic returns to the sync field condition. See FSL page FL220.

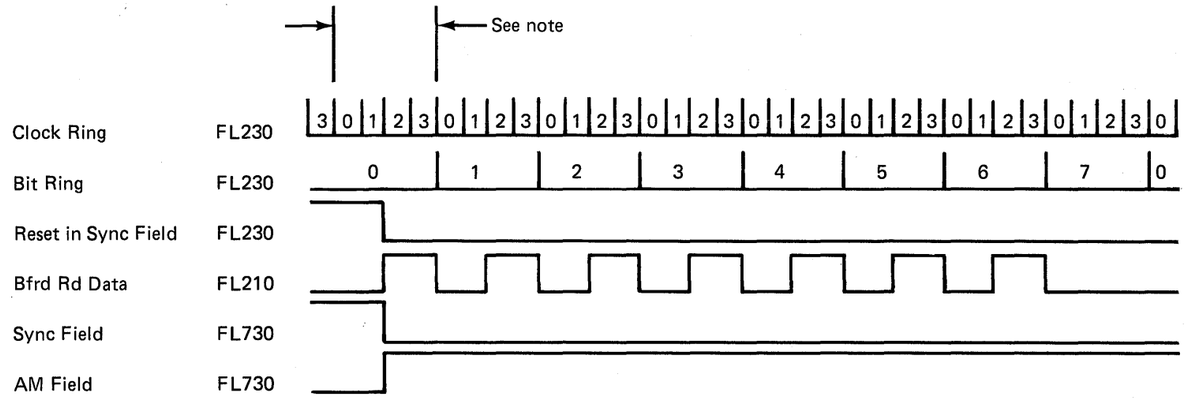
Bit Ring

The bit ring is used to get byte synchronization (to identify data bits as bits 0 through 7).

The bit ring is an 8-bit ring and is driven by the read/write clock. The bit ring is advanced, when gated, at the start of read/write clock 0.

During a read operation, a diskette sync field is needed to supply byte synchronization. While the sync field is being read, the bit ring advances to position 7, is reset, and is held reset until a data bit is read. The sector sequence control logic advances from the sync field condition to the AM field condition. The bit ring is then permitted to advance, in sync, with the diskette data byte.

During a write operation, byte synchronization is obtained while reading an ID field. The bit ring starts and continues running until the next ID sync field.



Note: The frequency of the clock ring is dependent on drive speed and recording mode:

33FD/53FD (FM) = 4 μs 72MD (FM) = 2 μs
33FD/53FD (MFM) = 2 μs 72MD (MFM) = 1 μs

Cyclic Redundancy Character Shift Register

The CRC shift register:

- Identifies sync fields
- Verifies diskette data integrity
- Generates 2 CRC bytes when writing

When the CRC shift register is used to identify sync fields, the 'CRC divide' signal never becomes active and the CRC register becomes a 16-position shift register. When the sector sequence control logic is in the sync field condition, a read data bit causes all 16 positions of the shift register to turn on if:

- The operation is a read operation
- The operation is a write operation and the sync field is part of an ID that is being read

If the sector sequence control logic is in the sync field or gap field condition and the CRC register is not zero, the 'fast sync on zeros' signal to the data separator is on. This signal causes clock bit synchronization in the data separator.

Sixteen consecutive 0-bits (FM) or 32 consecutive 0-bits (MFM) cause the CRC register to go to zero (all bits off), turning off the 'fast sync on zeros' line when bit synchronization is completed.

During read or write operations, the CRC register functions as three separate shift registers connected by exclusive OR (OE) circuits. A unique CRC character is assembled in the register while fields are written or read.

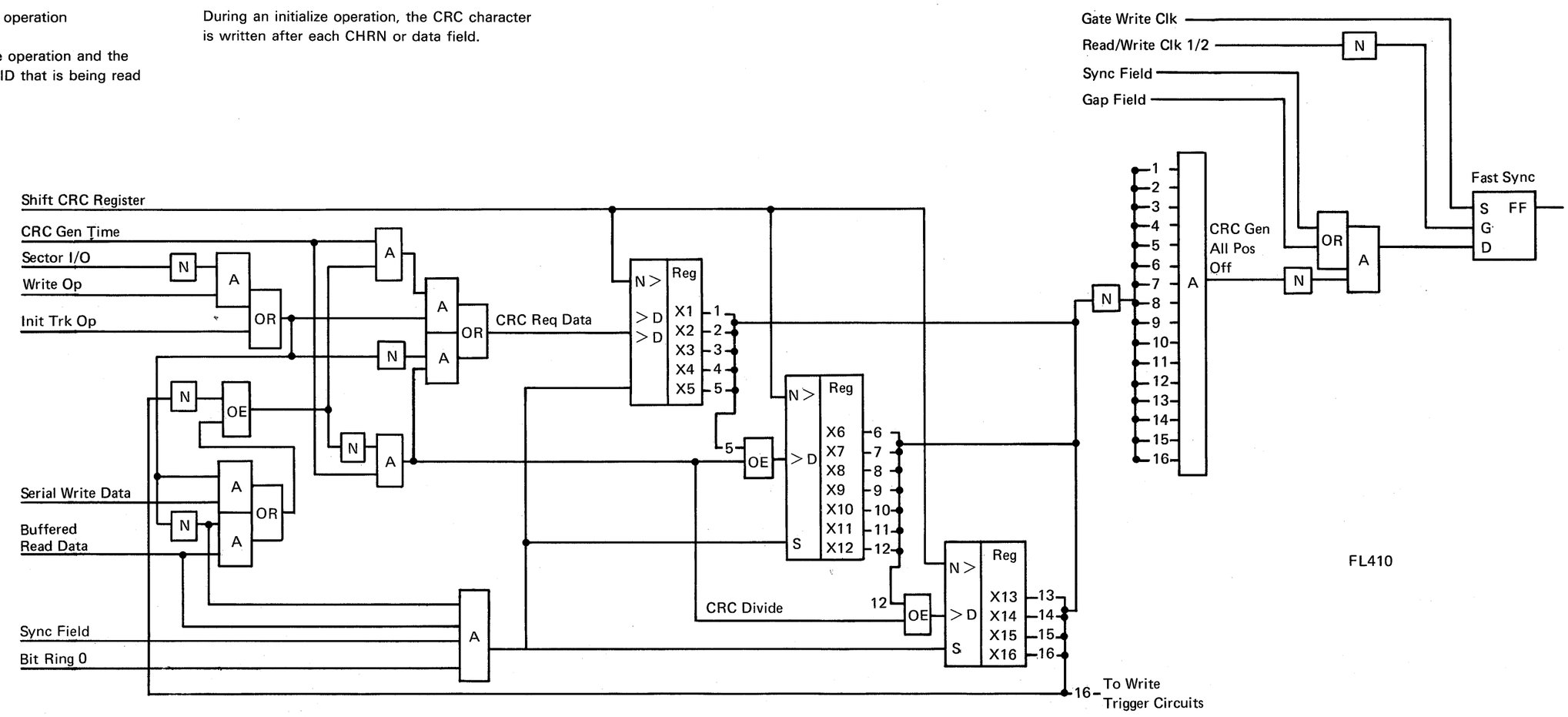
During an initialize operation, the CRC character is written after each CHRN or data field.

When searching for a record during a read or write operation, the CRC register must go to zero after the ID CRC field is read in order for an ID hit to occur.

During a write operation, the CRC characters are written after a data field.

During a read operation, the CRC register must go to zero after the data CRC field is read. If not, a data CRC error is detected.

CRC check time, used to determine an ID hit or to detect data CRC errors, occurs at the first bit ring 1 time of the gap field following the CRC field.



FL410

ID Buffer

The ID buffer contains five 8-bit registers. The registers and associated control circuits perform diskette ID field processing functions.

All data records are preceded by an ID field that describes the location of the data record on the diskette. The ID field includes cylinder, head, record, and number of bytes (CHRN) to give a unique address on the diskette for each record.

Before a data operation is started, the ID buffer is loaded by the control storage program with the C, H, R, N, and X bytes.

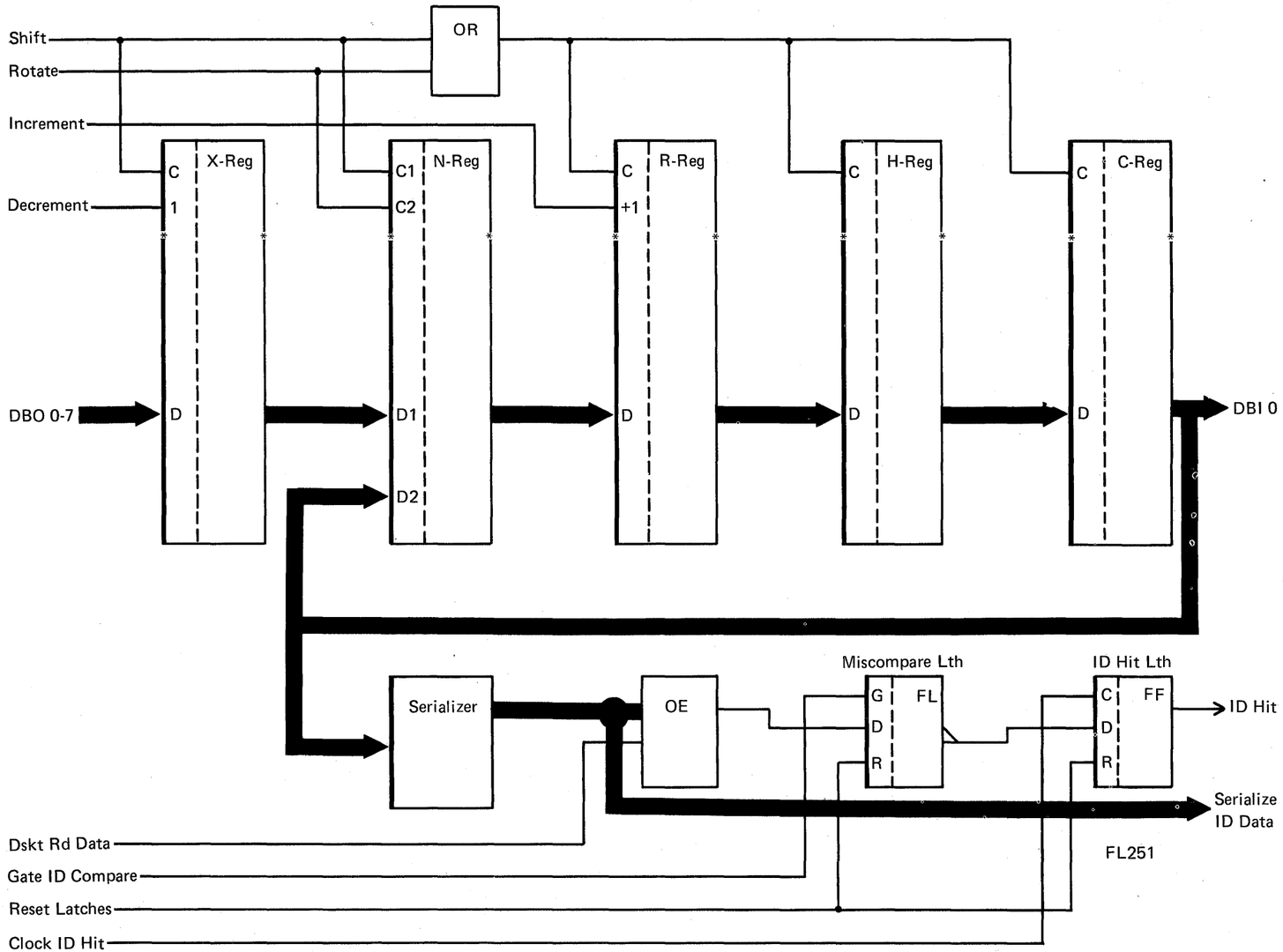
The C, H, R, and N bytes define the starting address for processing. The X byte specifies the number of records to be processed.

When a data operation is started, the attachment locates a diskette ID field by means of an address mark. The cylinder (C-reg) register byte is serialized and compared bit by bit to the diskette read data. At the end of the cylinder byte, the CHRN registers are switched so that the head byte is the next to be serialized and compared. In this way, the contents of the ID buffer are compared to the ID field, and all of the ID buffer bytes end up in the register in which they started.

A CRC field follows the CHRN field on the diskette to ensure the integrity of ID information. At the end of the CRC field, the miscompare latch is tested to see if a miscompare occurred while comparing the diskette CHRN field to the contents of the ID buffer. If no miscompare occurred, an ID hit latch is set. If a miscompare occurred, the operation will be repeated when the next ID field is located.

If an ID hit occurs, the data record is processed and when completed, the X-register is decreased and the R-register increased. The new value in the R-register causes a search for the next sequential record. When the X-register is cleared, the operation is ended.

The control storage program can sense the ID buffer using I/O sense commands (IOS 8).



Data Buffer

The attachment data buffer is a 4-register buffer (8 data bits and a parity bit). The buffer is used when moving data between main storage and a diskette.

In the case of a read operation, serial read data from the diskette is deserialized and gated into the data buffer input register. When the input register is full, the data is gated into register 2 and the input register can receive the next byte of read data. In this way, read data is advanced from the data buffer input register, to register 2, to register 1, and to the output register. From the output register of the data buffer, the read data goes to the DBI assembler and is moved to main storage by cycle steal.

During a write operation, data from main storage is moved to the attachment by cycle steal on the channel DBO. The data on the DBO is gated into the data buffer input register. Data is advanced from the input register to the output register the same way as during a read operation. The contents of the output buffer are serialized and passed to the attachment write trigger, and written on the diskette.

The status of the data buffer registers is checked by the cycle steal control logic to determine when a cycle steal request is needed.

If the data is not moved at the correct rate, the following errors are detected and recorded in hardware:

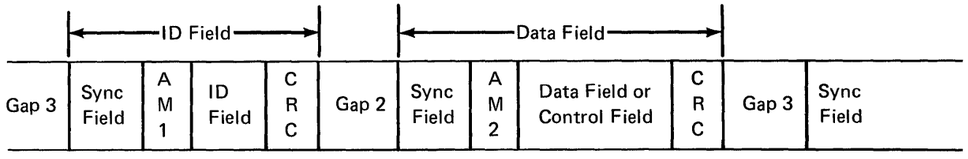
- Buffer overrun: The input buffer is full and diskette read data is ready to be gated or main storage write data is ready to be moved.
- Buffer underrun: The output buffer is empty and the channel is expecting read data or it is time to gate the output register contents to the write trigger.

See FSL page FL350.

Sector Sequence Control

During a data operation, with the data head loaded, this logic determines and identifies the type of field under the data head.

Each diskette sector has two parts: the sector identification field and the sector data record field.



The sector sequence control logic checks logic conditions (such as type of data operation, byte counter decodes, and diskette read data) to sequence through the following logic conditions:

- Sync field
- AM field
- CHRN/data field
- CRC field
- Gap field

See FSL page FL730.

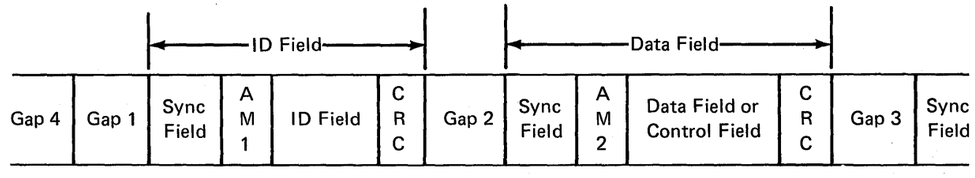
Note: The sector ID output of the track sequence control logic determines if the field described by the sector sequence control logic is an ID field or a data field.

Track Sequence Control

One of the functions of this logic is to modify the output of the sector sequence control logic. The ID fields and data fields of the diskette sectors have the same basic format. The sector sequence control logic specifies fields within a sector but does not determine between ID and data fields. The sector ID output of the track sequence control logic determines if the field under the data head is an ID field or a data field.

Another function of this logic is to determine when the data head is over the special gap fields before and after index.

See FSL page FL730.



Byte Counter

The byte counter is a binary counter that specifies the end of fields for the sector sequence control logic. The byte counter also counts the number of bytes moved from main storage to the data buffer during a write, initialize, or verify operation, and terminates the cycle steal when the data record has been completely moved.

The diskette format, the type of data operation, the data recording mode, and the present field being processed determine field length and are, therefore, input to the byte counter control logic. From this input, values are selected to set the byte counter. The byte counter is then decreased:

- Once for every byte of data moved from main storage to the data buffer during a write, initialize, or verify operation.
- Once every bit ring 6 time for all other data operations.

When the byte counter is zero, the cycle steal control logic or the sector sequence control logic is signaled. Which logic is signaled depends on the type of operation.

Another output of the byte counter is the 'last byte of field' signal, used by the address mark detection logic to identify the last byte of an MFM address mark (MFM ID address mark is a 4-byte field of hexadecimal A1A1A1FE).

See FSL page FL720.

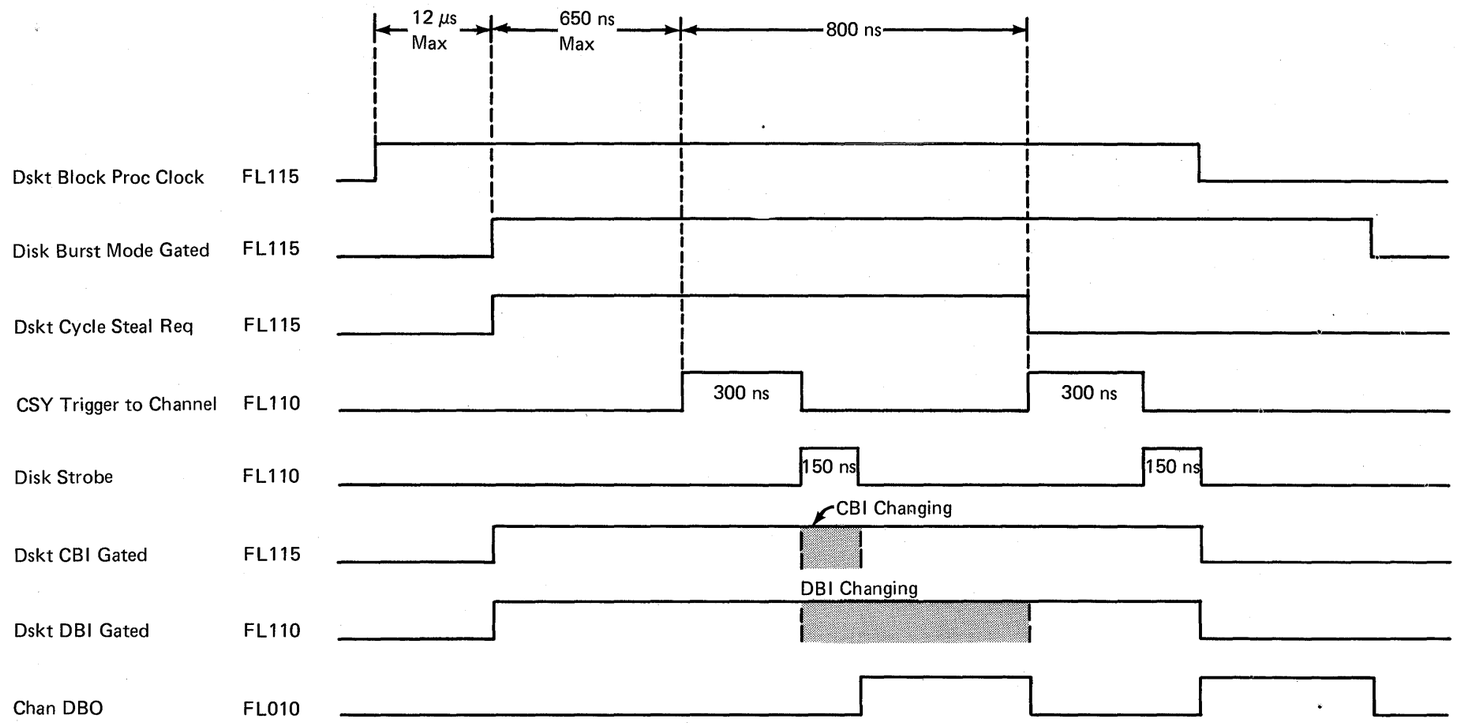
Cycle Steal Control

Data is moved from main storage to the attachment data buffer during a write operation and from the data buffer to main storage during a read operation. This data is moved by burst mode cycle steal.

The cycle steal operation is started by the attachment activating the 'dskt/disk block proc clock' signal. The control logic determines when to activate this signal by checking the four register data buffers. If the buffer output register and register 1 are full during a read operation, or if the input register and register 2 are empty during a write operation, the signal is activated. Before starting the data movement, the attachment logic must have the CBI bits set up. The CBI bits control selection of LSRs that contain the address of the storage location, the direction of data movement, the storage type (main or control) used, and the increasing of the storage addresses. This information is operation dependent, with the exception of the storage location address, and is set up by the control storage program.

The control processor responds to the 'dskt/disk block proc clock' signal by activating the 'chan burst mode' line, after the present instruction is executed. This permits the attachment to activate the 'dskt/disk cycle steal req' line. The control processor responds with two 'chan CSY trigger' pulses and two 'chan FD strobe' pulses, which are used for gating in the attachment. A byte of data is moved for each 'chan CSY trigger' pulse.

The 'dskt/disk block proc clock' line drops after the second 'chan FD strobe' pulse. The control processor drops the 'chan burst mode' line and continues processing.



Interrupt Level 4 Request

The function of the interrupt level 4 request logic is to signal the control processor when an operation is complete, an error has occurred, or after a time-out.

The 'op end irpt' latch, if enabled by an I/O load command (IOL 0), will be set if an operation is complete or if an error has been detected. An I/O load command (IOL 0) also resets the 'op end irpt' latch.

The '8-ms counter irpt' latch is set if 8 milliseconds is decoded in the time-out counter. The counter must first be enabled by an I/O load command (IOL 6). This command also resets the timer.

If conditions cause either of the interrupt latches to set, the 'interrupt level 4 request' latch becomes active only if it is enabled by an I/O load command (IOL 6).

An I/O load command (IOL 3) resets the 'interrupt level 4 request' latch and the '8-ms counter irpt' latch.

See FSL page FL071.

DBI Assembler

The DBI (data bus in) assembler passes data or sense information from the attachment to the channel. The information moved and the timing of this data movement are controlled as follows:

- Data operation: The gating of the read data is controlled by the cycle steal control logic. For more information, see *Cycle Steal Control* earlier in this section and FSL page FL130.
- Sense operation: The contents of the sense byte are determined by the command decode logic. Each IOS or IOCS command gates unique data to the channel. For more information, see *Commands* earlier in this section and FSL page FL130.

CBI Assembler

The CBI (command bus in) assembler passes control information from the attachment to the channel. The CBI bits used (0, 1, 3, 4, and 5) are described as follows:

CBI 0 If CBI bit 0 is on, the storage address is increased.

CBI 1 If CBI bit 1 is on, the operation is a write. If CBI bit 1 is off, the operation is a read.

CBI 3 CBI bit 3 is always on during cycle steal operations. This bit selects interrupt level 1 work register 5 for the storage location address.

CBI 4 If CBI bit 4 is on, (1) the data to be moved goes to control storage or (2) the condition is true for a jump on I/O condition command.

CBI 5 If CBI bit 5 is on, bad parity was detected on the port data bus out.

CBI bits 0, 1, 3, and 4 are set before starting the cycle steal operation.

See FSL page FL110.

Op Decode

The op (operation) decode is used to determine the type of data operation to be done. When an IOCL 2 command is issued to the diskette attachment, DBO bits 5 through 7 indicate the type of operation as follows:

Bit 5	Bit 6	Bit 7	Operation
0	0	0	Null data
0	0	1	Read data
0	1	0	Read data and control records
0	1	1	Read ID
1	0	0	Write verify
1	0	1	Write data with data address mark
1	1	0	Write data with control address mark
1	1	1	Initialize track

See FSL page FL062.

Autoloader Control

The autoloader control determines which autoloader command is sent to the file control card. These autoloader commands, except during CSIPL, are determined by latches set by I/O control load commands (IOCL D and IOCL E). When the '+enable autoloader' line is activated, the command is sent to the file control card on the command bus (lines 0 through 5 and a parity line) to be decoded by the file control card autoloader logic.

See *Commands* earlier in this section and FSL page FL550.

Seek Control

When the '+enable autoloader' line is not active, the four seek control lines from the attachment card to the file control card control the seek operation.

The seek control logic includes latches. The output of these latches determines the conditions on the four seek control lines. Except during CSIPL, these latches are set and reset by I/O control load commands (IOCL 7).

See FSL page FL550.

500-Kilohertz Oscillator

The 500-kilohertz oscillator supplies the clock pulses for autoloader operations. The 500-kilohertz oscillator is started by an I/O control load command (IOCL 4) and is generated from the 1-microsecond clock.

See *Commands* earlier in this section and FSL page FL540.

Error Conditions

Byte	Bit	Error Condition	Logged in ERAP	Detected by: Micro-code	Detected by: Hard-ware	Corrective Action
0	0	Missing Data Address Mark	Yes		X	1
	2	Data Cyclic Redundancy Check	Yes		X	1
	3	Cylinder Mismatch	No		X	2
1	0	No Op Condition	Yes	X		1
	1	Not Valid Control Record Check	Yes		X	3
	2	Write Verify Mismatch	Yes		X	1
	5	Write Error	Yes	X		
2	0	Fast Check	Yes		X	1
	1	Diskette Not Ready	No		X	4
	2	Missing Erase Current	No		X	1
	3	ID Not Found	Yes		X	1
	4	Buffer Underrun	No		X	1
	6	Buffer Overrun	Yes		X	1
3	0	Unexpected Erase Current Present	Yes		X	1
4	1	Autoloader Error	No		X	5
	2	Parity Check	Yes		X	1
	4	Autoloader Command Reject	No		X	5
	5	Autoloader Motion Check	No		X	5
	6	Not Valid Command Check	Yes		X	1
	7	Time-out Check	Yes		X	6
5		Carriage Bed Failure	Yes			
		Carriage bed stuck at home			X	7
		Carriage bed stuck off home			X	7
		Picker Failure	Yes			
		Picker stuck in magazine			X	7
		Picker stuck in drive			X	7
		Failure to Eject[1]	Yes			
		Diskette stuck in drive[1]			X	7
		Failure to Pick	Yes			
		Diskette failed to pick			X	8
		Window Magnet Failure[1]	Yes			
		Diskette window stuck open[1]			X	8
		Diskette window stuck closed[1]			X	6
		Cover Open	No			
		Operation Out of Sequence	Yes			
		Operation out of sequence			X	9
		Not oriented	No		X	7
		Write or Erase Current Present	Yes			
		Write or erase current active			X	1
		Parity Check	Yes		X	1

Byte 5

Bit	Description
0	Motion check bit 8
1	Motion check bit 4
2	Motion check bit 2
3	Motion check bit 1
4	Not used
5	Not used
6	Not used
7	Not used

Motion Check Codes (hex)

- 00 = Not used
- 10 = Carriage bed stuck at home
- 20 = Carriage bed stuck off home
- 30 = Picker stuck in magazine
- 40 = Picker stuck in drive
- 50 = Diskette stuck in drive[1]
- 60 = Diskette failed to pick
- 70 = Diskette window stuck open[1]
- 80 = Diskette window stuck closed[1]
- 90 = Cover open
- A0 = Not used
- B0 = Operation out of sequence
- C0 = Not oriented
- D0 = Write or erase current active
- E0 = Not used
- F0 = Parity check

[1] Conditions apply only for machines with the old style picker.
[2] 33FD or 53FD
[3] 72MB only

Description of Corrective Actions	
1.	a. Retry the operation up to two times if a write operation; 9 times if a read operation. b. If the retry is successful, log a temporary error indicating the number of retries required and return to processing. c. If the retry is not successful and the operation is not a read operation, log a permanent error.[2] d. If the retry is not successful and the operation is a read operation, issue eject, select slot, and recalibrate commands and then return to step *a*.[3] e. If the failure continues after returning to step *a* three times, log a permanent error.
2.	a. Issue a seek to the logical cylinder desired, then issue the data operation again. b. Retry the operation three times. c. If the retry is successful, log a temporary error for each time the operation failed and return to processing. d. If the retry is not successful, log a permanent error.
3.	Call a not valid control record and return to processing.
4.	a. Do a recalibrate operation and verify that the correct diskette is in the drive. b. If the failure continues, log a permanent error.
5.	See byte 5 for more information.
6.	a. Issue an abort command followed by an orient command and then the proper command sequence. b. Retry the operation two times. c. If the retry is successful, log a temporary error indicating the number of retries required and return to processing. d. If the retry is not successful, log a permanent error.
7.	a. Issue an orient command followed by the proper command sequence. b. Retry the operation two times. c. If the retry is successful, log a temporary error indicating the number of retries required and return to processing. d. If the retry is not successful, log a permanent error.
8.	a. Issue an eject command followed by the failing command. b. Retry the operation two times. c. If the retry is successful, log a temporary error indicating the number of retries required and return to processing. d. If the retry is not successful, log a permanent error.
9.	a. Issue the proper command sequence. b. Retry the operation two times. c. If the retry is successful, log a temporary error indicating the number of retries required and return to processing. d. If the retry is not successful, log a permanent error.

Diskette Drive Errors

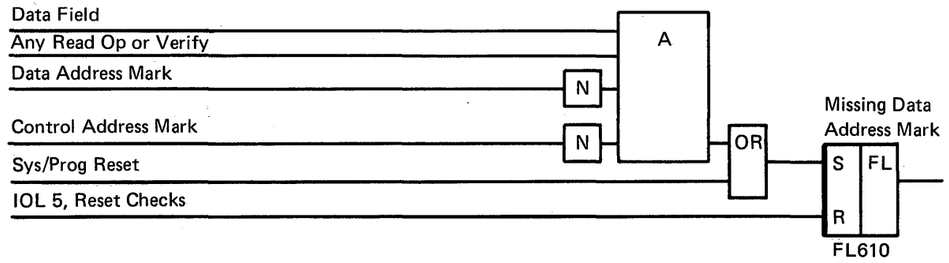
The control storage program issues a jump on I/O condition command with a modifier of hexadecimal 1 to determine if there is a drive error condition or a not ready condition. An I/O sense command is then used to determine the specific error. The following are drive errors:

- Missing data address mark
- Data cyclic redundancy check
- Cylinder mismatch
- No op condition
- Not valid control record check
- Write verify mismatch
- Write error
- Fast check
- Diskette not ready
- Missing erase current
- ID not found (record not found)
- Buffer underrun
- Buffer overrun
- Unexpected erase current present (data unsafe)

Missing Data Address Mark (Byte 0, Bit 0): During a read or verify operation, the physical location of the desired data record is located by its ID field. An ID hit occurs when the contents of the ID buffer compare equally to the diskette ID field (CHRN).

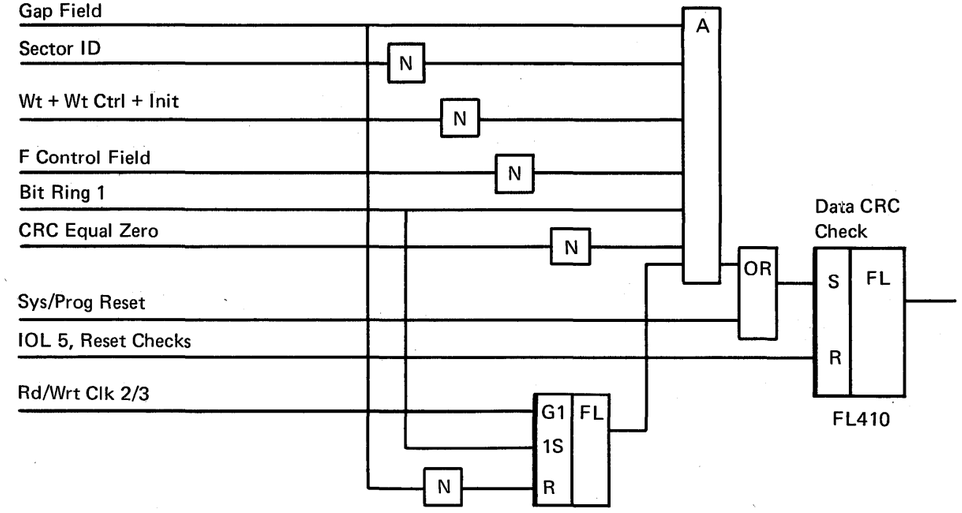
The ID hit conditions the logic to expect the next address mark to be a data address mark.

If a valid address mark is decoded and it is not a data or control address, the 'missing data address mark' error latch is set.



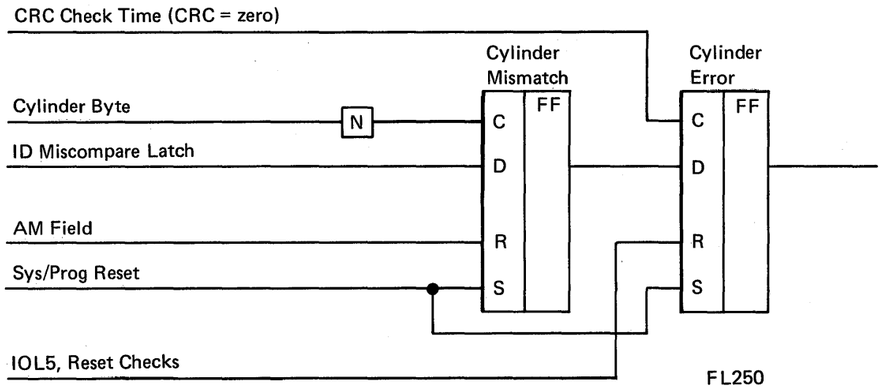
Data Cyclic Redundancy Check (Byte 0, Bit 2): As the data record is read during a read or verify operation, a CRC character (unique to the data record) is assembled in the CRC register. When the data CRC field is read, all positions of the CRC register will go to zero if the CRC character assembled during the read or verify operation is the same as the written CRC field.

CRC check time occurs at the first bit ring 1 time of the gap field following the data CRC field. If the operation is a read or verify operation and the CRC register is not equal to zero at CRC check time, the 'data CRC check' error latch is set.



Cylinder Mismatch (Byte 0, Bit 3): During the ID search of a data operation, the serialized CHRN data from the attachment ID buffer is compared bit by bit to the read data from the diskette CHRN field. If a miscompare occurs, the 'ID miscompare' latch is set.

If the 'ID miscompare' latch is set when the cylinder byte was read and the head byte is about to be read, the 'cylinder mismatch' latch is set. The 'cylinder error' latch is set if the ID CRC equals zero.



FL250

No Op Condition (Byte 1, Bit 0): The desired diskette operation cannot be executed because a field of the input/output block (IOB) is not valid or not compatible with the status of the hardware.

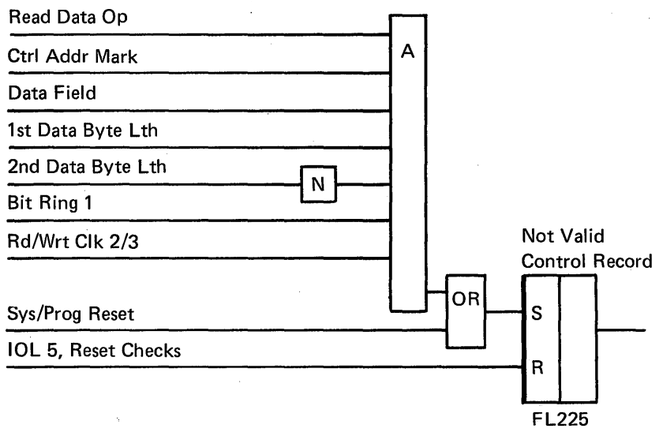
The control storage program sets this bit on (if a diskette operation cannot be executed) and uses byte 0, bits 0-3 to describe the error.

This bit is reset by the next diskette operation or by a system reset.

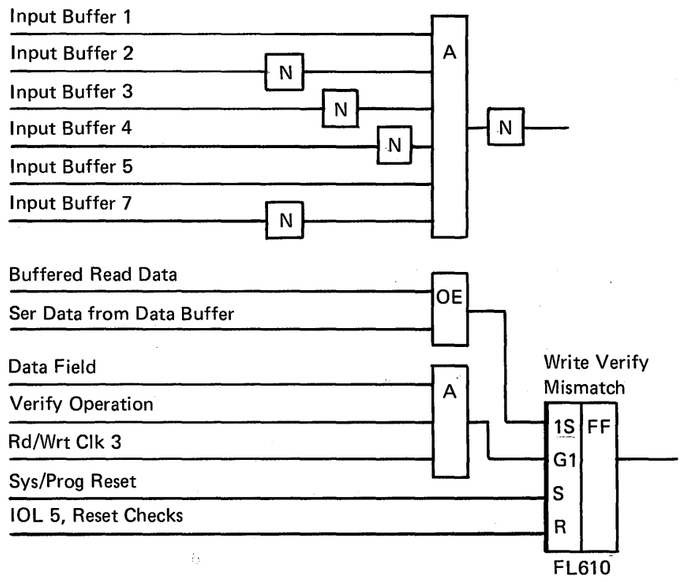
Byte 0 Bit 0 1 2 3	Description
0 0 0 0	Device address or port address not valid: The control storage program has detected that the diskette device address or port address received from the IOB is not valid.
0 0 0 1	Command not valid: The control storage program has detected that a diskette command received from the IOB is not valid.
0 0 1 0	Not ready — not seek operation: The command issued to the diskette is rejected because the diskette is not ready and the command is not a seek.
0 0 1 1	Not ready — seek is not a recalibrate: The command issued to the diskette is rejected because the diskette was not ready and the command was not a recalibrate.
0 1 0 0	Errors not reset: One or more errors have not been reset.
0 1 0 1	Reject head 1 operation: The command issued to the diskette is rejected because head 1 is selected, but a Diskette 1 is in the machine.
0 1 1 0	Reject MFM operation: The command issued to the diskette is rejected because MFM mode is requested, but a Diskette 1 is in the machine.
0 1 1 1	Write gate or erase gate on: A command should not be issued to the diskette because the write gate or erase gate is not off.
1 0 0 0	Reject autoloader command: The command issued is rejected because the slot number specified is not valid.
1 0 0 1	IOB error detected: The control storage program has detected an error in the IOB.
1 0 1 0	Time-out in data mode operation: The control storage program has detected that the data operation was not completed in a predetermined time.

Not Valid Control Record Check (Byte 1, Bit 1): If during a read data operation, the address mark following an ID field is decoded as a control address mark, the first byte of the control field must be a graphic D or F. The first byte immediately following the address mark is the control flag identifying the type of record. The character code for the graphic D (hexadecimal C4 for EBCDIC) indicates that this physical record has been logically deleted. The character code for the graphic F (hexadecimal C6 for EBCDIC) indicates that the physical record space contains a defect. Diskettes recorded in ASCII will have the ASCII bit patterns for the graphics D and F.

If the operation is a read data operation and the first byte of a control field is not a graphic D or F, the 'not valid control record' latch is set.



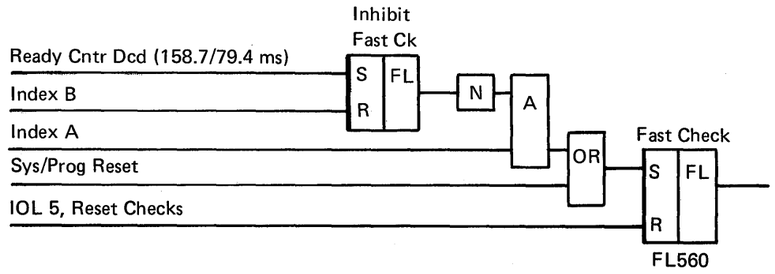
Write Verify Mismatch (Byte 1, Bit 2): A write verify operation is performed after every write operation. The data to be verified is moved from the main storage data area to the attachment data buffer. The contents of the data buffer are compared bit by bit to the serial data read from the diskette data field. If a miscompare is detected, the 'write verify mismatch' latch is set.



Write Error (Byte 1, Bit 5): This error condition is set by the control storage program if an adapter check occurs during a write operation. More error information may be obtained from other bits.

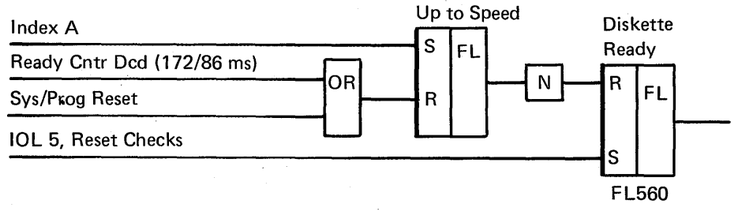
Fast Check (Byte 2, Bit 0): A fast check is indicated if the diskette index pulses occur more often than once every 158.7 milliseconds for a 33FD or 53FD drive or once every 79.4 milliseconds for a 72MD drive.

The ready counter is used to measure the time between index pulses. The ready counter is increased by a 512-microsecond clock. The ready counter is reset by each index and if a count of 158.7 milliseconds (33FD or 53FD) or 79.4 milliseconds (72MD) is not decoded before the next index pulse occurs, the 'fast check' latch is set.



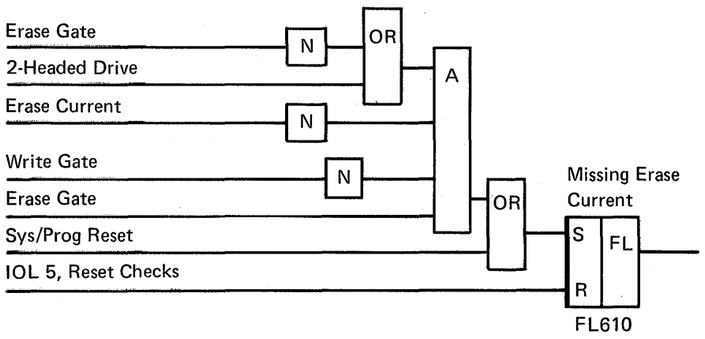
Diskette Not Ready (Byte 2, Bit 1): A diskette not ready condition occurs when diskette index pulses occur less frequently than once every 172 milliseconds for a 33FD or 53FD drive or once every 86 milliseconds for a 72MD drive.

The ready counter is used to measure the time between index pulses. The ready counter is increased by a 512-microsecond clock. The ready counter is reset by each index and if a count of 172 milliseconds (33FD or 53FD) or 86 milliseconds (72MD) is decoded before the next index pulse occurs, the 'diskette ready' latch is reset.



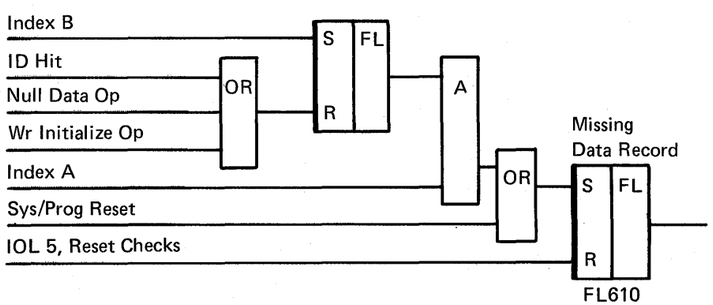
Missing Erase Current (Byte 2, Bit 2): The 'missing erase current' latch is set if erase current fails to turn on during a write operation. The 'erase gate' line conditions the file control card erase circuits.

At the fall of the 'write gate' line, if the 'erase gate' line is active and erase current is not sensed, the 'missing erase current' error latch is set.

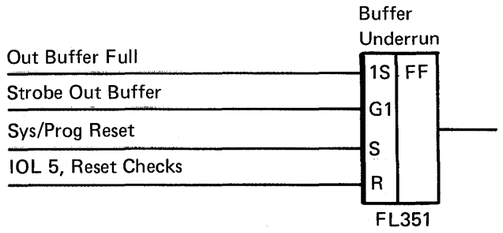


ID Not Found (Byte 2, Bit 3): The 'missing data record' latch is set if two consecutive index pulses occur without an ID hit, unless the data mode is a null data operation or an initialize track operation.

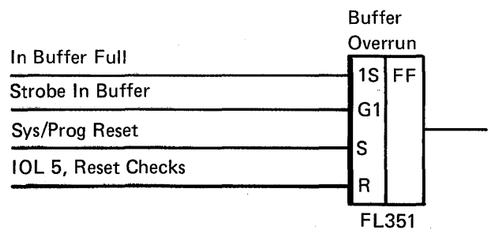
An ID hit occurs when the CHRN identification field in the attachment ID buffer, specifying the sector to be processed, matches a CHRN field on the track under the data head.



Buffer Underrun (Byte 2, Bit 4): The 'buffer underrun' latch is set if the output register of the data buffer is empty when it is strobed, which indicates that the minimum data rate into the buffer was not maintained during a data operation.



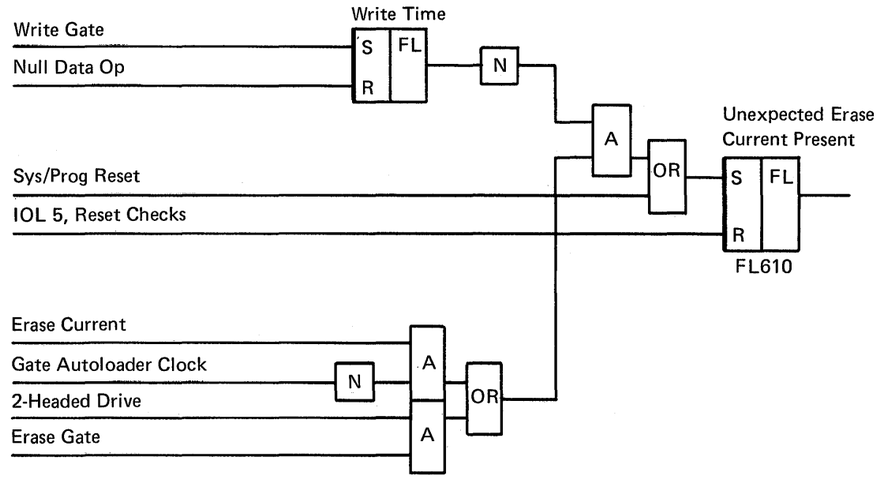
Buffer Overrun (Byte 2, Bit 6): The 'buffer overrun' latch is set if the input register of the data buffer is already full when it is strobed, which indicates that the minimum data rate out of the buffer was not maintained during a data operation.



Unexpected Erase Current Present (Byte 3, Bit 0): The 'unexpected erase current present' latch is set if the attachment 'write time' latch is reset and:

- The drive is a 33FD and the attachment 'dskt erase gate' line is active.
- The drive is a 53FD or a 72MD and the drive 'erase current' line is active.

The 'write time' latch is set by the 'write gate' line (an attachment output signal that conditions the drive write and erase circuits) and reset when the data operation is ended.



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Autoloader Errors

The control storage program determines the autoloader status by using an I/O control sense command (IOLS 3) when an autoloader motion command or an autoloader sense command has been issued. Autoloader status and error information is encoded on the autoloader status line (bits 0 through 3 of IOCS 3). The following are autoloader errors:

- Autoloader error
- Parity check
- Autoloader command reject
- Autoloader motion check
- Not valid command check
- Time-out check
- Carriage bed failure
- Picker failure
- Failure to eject[1]
- Failure to pick
- Window magnet failure[1]
- Cover open
- Operation out of sequence
- Write/erase current present

Autoloader Error (Byte 4, Bit 1): This condition is sensed by the autoloader control logic (on the file control card) and indicates that an error has occurred during an autoloader operation. See byte 5 and other byte 4 bits for more information.

Parity Check (Byte 4, Bit 2): This condition is sensed by the autoloader control logic (on the file control card) and indicates a parity error on the command lines (0 through 5, P) for any command. See FSL page FX210.

Autoloader Command Reject (Byte 4, Bit 4): This condition is sensed by the autoloader control logic (on the file control card) and indicates that a motion command cannot be executed. The condition of the control logic is not acceptable to execute the issued command. See byte 5 for more information. Also see FSL page FX255.

Autoloader Motion Check (Byte 4, Bit 5): This condition is sensed by the autoloader control logic (on the file control card) and indicates that an autoloader error was detected during an autoloader motion. See byte 5 for more information. Also see FSL page FX255.

Not Valid Command Check (Byte 4, Bit 6): This condition is sensed by the autoloader control logic (on the file control card). This condition indicates, between 3 milliseconds and 17 milliseconds after the enable autoloader signal becomes active, that the command on the command lines to the file control card is not valid. See FSL page FX255.

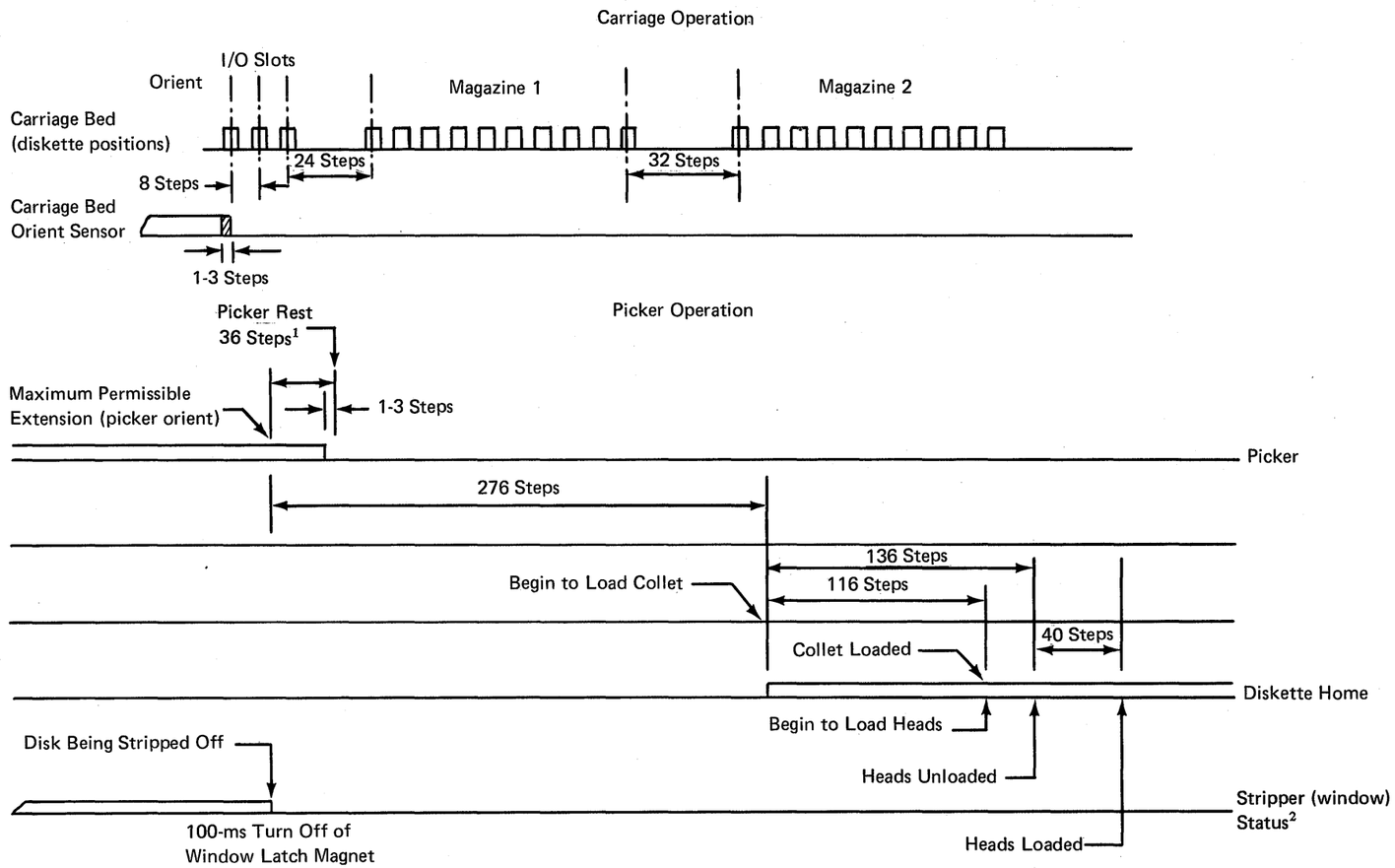
Time-out Check (Byte 4, Bit 7): This condition indicates the autoloader control logic did not return an op end status in time after an autoloader command was issued.

Window Magnet Failure[1] (Byte 5; see motion check codes): These conditions are sensed by the autoloader control logic (on the file control card):

- Diskette window stuck open (motion check code hex 70).
  - During an eject operation, indicates the Window Magnet switch is on when the picker has stopped at the Picker Rest position (96 milliseconds after the diskette window magnet is de-activated).
- Diskette window stuck closed (motion check code hex 80).
  - During a select slot operation, indicates the Window Magnet switch is off when the picker has stopped at the Picker Rest position (96 milliseconds after the diskette window magnet is activated).

See FSL page FX255.

Carriage and Picker Timings



[1] Picker rest is 20 steps from picker orient on machines with the new style picker.
[2] Applies only for machines with the old style picker.

Cover Open: (Byte 5; see motion check codes): This condition indicates the diskette magazine unit cover is open. See FSL page FX255.

Operation Out of Sequence (Byte 5; see motion check codes): These conditions are sensed by the autoloader control logic (on the file control card):

- Operation out of sequence (motion check code hex B0).
  - Indicates the command cannot be executed because the autoloader control logic is not in a condition that is acceptable for the issued command.

- Not oriented (motion check code hex C0).
  - Indicates the command cannot be executed because the autoloader control logic is not in an oriented condition (physical location of autoloader mechanisms is not known).

See FSL page FX255.

Write/Erase Current Present (Byte 5; see motion check codes): This condition is sensed by the autoloader control logic (on the file control card):

- Write or erase current active (motion check code hex D0).
  - Indicates a load heads command could not be executed because the autoloader control logic sensed write or erase current present.

See FSL page FX255.

Parity Check (Byte 5; see motion check codes): This condition is sensed by the autoloader control logic (on the file control card):

- Parity check (motion check code hex F0).
  - Indicates even parity on the command lines when the '+enable autoloader' line is active.

See FSL page FX255.

Carriage Bed Failure (Byte 5; see motion check codes): These conditions are sensed by the autoloader control logic (on the file control card):

- Carriage bed stuck at home (motion check code hex 10).
  - During an orient operation, indicates the Carriage Bed switch is on and fails to go off after 16 ninety-degree steps[1] of the carriage bed stepper motor toward I/O slot 1.
  - During a select slot operation, indicates the Carriage Bed switch is on.

- Carriage bed stuck off home (motion check code hex 20).
  - During an orient command, indicates the Carriage Bed switch failed to turn on after 256 ninety-degree steps of the carriage bed stepper motor toward I/O slot 1.

See FSL page FX255.

Picker Failure (Byte 5; see motion check codes): These conditions are sensed by the autoloader control logic (on the file control card):

- Picker stuck in magazine (motion check code hex 30).
  - During an orient operation, indicates the Picker Rest sensor is on and fails to go off after 64 ninety-degree steps of the picker stepper motor toward the drive.
  - During an orient, select slot, or eject operation, indicates the Picker Rest sensor is on when the picker is at the Picker Rest position.[2]

- Picker stuck in drive (motion check code hex 40).
  - During an orient operation, indicates the Picker Rest sensor fails to turn on after 448 ninety-degree steps of the picker stepper motor toward the Picker Orient position.
  - During an orient, select slot, or eject operation, indicates the Picker Rest sensor is off after 32 ninety-degree steps[3] of the picker stepper motor from the Picker Orient position.

See FSL page FX255.

Failure to Eject (Byte 5; see motion check codes): This condition is sensed by the autoloader control logic (on the file control card):

- Diskette stuck in drive (motion check code hex 50).[4]
  - Indicates the Diskette In switch is on when the picker mechanism is located at the Picker Rest position. This indicates that the diskette is still in the drive.

See FSL page FX255.

Failure to Pick (Byte 5; see motion check codes): This condition is sensed by the autoloader control logic (on the file control card):

- Diskette failed to pick (motion check code hex 60).
  - Indicates the Diskette In switch is off at a point where the diskette should activate the switch. This indicates that the diskette was not picked.
  - On machines with the new style picker, during a select slot operation, indicates the 33FD index sensor has not sensed that a diskette was inserted into the drive. The sensor tests for the diskette hub hole during the operation of the picker mechanism.

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[1] Sixty-four 90-degree steps on machines with the new style picker.
[2] The Picker Rest sensor is on when carriage bed motion is required on machines with the new style picker.
[3] Four 90-degree steps on machines with the new style picker.
[4] Applies only to machines with the old style picker.

INPUT/OUTPUT LINES

Pin Number	33FD	53FD	72MD	
			Diskette Drive Mode	Autoloader Mode
A2B02	+write data	+write data	+write data	500-kHz clock
A2B03	+5 V	+5 V		
A2B04	+erase gate	+erase gate	+erase gate	
A2B05	+write gate	+write gate	+write gate	
A2B06	+inner tracks	+inner tracks	+inner tracks	+command 5
A2B07		+select head	+select head	+command P
A2B08	ground	ground		
A2B09	+erase current sense	+erase current sense	+erase current sense	+status C
A2B10	+24 V	+24 V		
A2B11	-5 V	-5 V		
A2B12			-power on reset	-power on reset
A2B13			+status D	+status D
A2D02	+access 0	+access 0	+access 0	+command 0
A2D03	+access 1	+access 1	+access 1	+command 1
A2D04	+access 2	+access 2	+access 2	+command 2
A2D05	+access 3	+access 3	+access 3	+command 3
A2D06			+enable autoloader	+enable autoloader
A2D07	+file data	+file data	+file data	
A2D08		+diskette 2 sense	+diskette 2 sense	+status B
A2D09		-drive sense	-drive sense	-drive sense
A2D10	+head engage	+head engage		
A2D11			+status A	+status A
A2D12		+switch filter	+switch filter	+command 4
A2D13	+index	+index	+index	+index