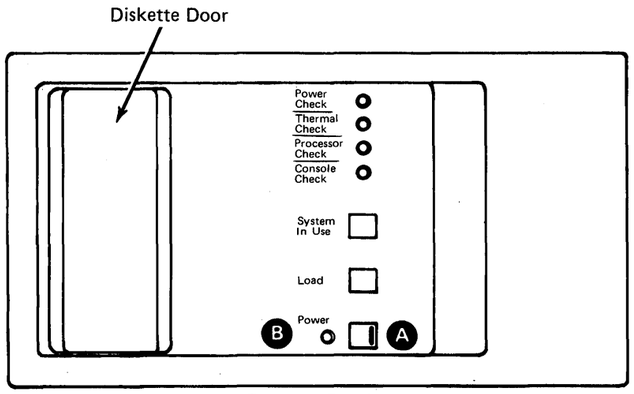
Contents

Control Panels

OPERATOR PANEL



Operator Panel

Power Switch (A)

Set the Power switch to I to power on the system. If the keylock feature is installed, turn the key to the horizontal (on) position. When you switch the power on:

- A system reset occurs.
- The Power light comes on.

Set the Power switch to O to power off the system. When you set the Power switch to O:

- The Power light goes off.
- The contents of registers and storage are lost.
- The information stored in the power failure latches about the most recent power failure is kept.

Power Light (B)

The Power light is on when system power is on. The Power light is off when system power is off.

Load Switch/Light

Press the Load switch to start the control storage initial program load (CSIPL) and main storage initial program load (MSIPL) sequences.

When you press the Load switch, the Load light comes on. The Load light remains on until the first 4,096 bytes of the control storage program are loaded correctly.

System In Use Light

The System In Use light comes on when one or more programs or commands are active in main storage. The System In Use light goes off when no programs or commands are using main storage. When on, the System In Use light indicates that programs have not completed running, so the system should *not* be powered off and the Load switch should *not* be pressed.

Power Check Light

The Power Check light comes on if the voltage or current in one of the power supplies does not meet specifications. When the Power Check light comes on, the system is powered off and the information stored in the power failure latches is kept until primary power is removed or the circuit breaker (CB1) is switched off (down).

You can use the CE panel lights to find out why the power check occurred. For an explanation of how to use these lights to determine the cause of a power check, see paragraphs 05-420 and 05-430 of the *5340 System Unit Maintenance Manual*.

Thermal Check Light

The Thermal Check light comes on if the A-gate or the power supply housing is too hot. A thermal check condition powers off the system. After the failing part becomes cool, set the Power switch to O, then to I, to power on the system.

Processor Check Light

The Processor Check light comes on if the processing unit senses an error for which there is no correction procedure. If the Processor Check light comes on, press the Load switch to start a new initial program load sequence.

Console Check Light

The Console Check light comes on if the system console or the work station controller fails. If the system console fails, another work station can be assigned as the system console before processing continues (if an alternate is specified in the system configuration). If the work station controller fails, the cause of the failure must be found and corrected before processing continues. The Console Check light goes off after the cause of the failure is corrected.

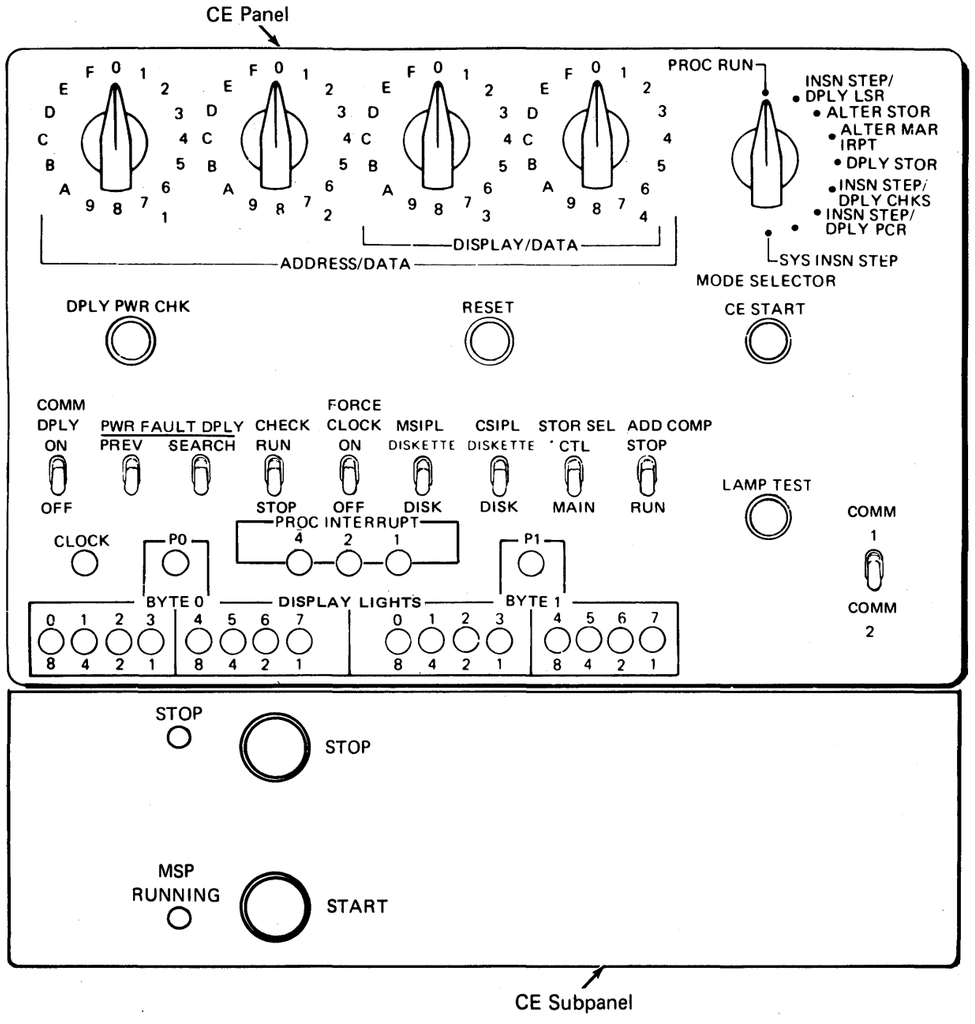
Immediate Power Off Switch

The Immediate Power Off switch, on the left side of the 5340 System Unit:

- Must remain set to I (on) during normal system operation
- When set to O (off), removes all power from the system *except AC to the control power supply*

CAUTION
The Immediate Power Off switch is for emergency use only. Do not use the Immediate Power Off switch to power on and power off the system. When powering on, you must use the Power switch on the operator panel to initialize the system correctly.

CE PANEL



Start Switch

The Start switch is on the CE subpanel, below the CE panel. When the Stop light is on, and the system is under control of the SSP, the alter/display routine is usually in control and the Start switch has no function. The Start switch only causes the Stop light to go off.

MSP Running Light

The MSP Running light is on the CE subpanel, below the CE panel. The MSP Running light remains on as long as the main storage processor clocks are running. The MSP Running light goes off when the main storage processor clocks are stopped.

Stop Switch

The Stop switch is on the CE subpanel, below the CE panel. After each system instruction is executed, the control storage program tests to see if the Stop switch was pressed. If the Stop switch *was* pressed:

- The main storage processor stops.
- The control processor continues to run.
- The alter/display routine becomes active on the system console and the option menu is displayed.

Stop Light

The Stop light is on the CE subpanel, below the CE panel. The Stop light comes on:

- When you press the Stop switch
- When the system has been powered on
- If an address-compare stop occurs for a main storage address
- If you are using the Sys Insn Step position of the Mode Selector switch (see *Sys Insn Step Position* later in this section)

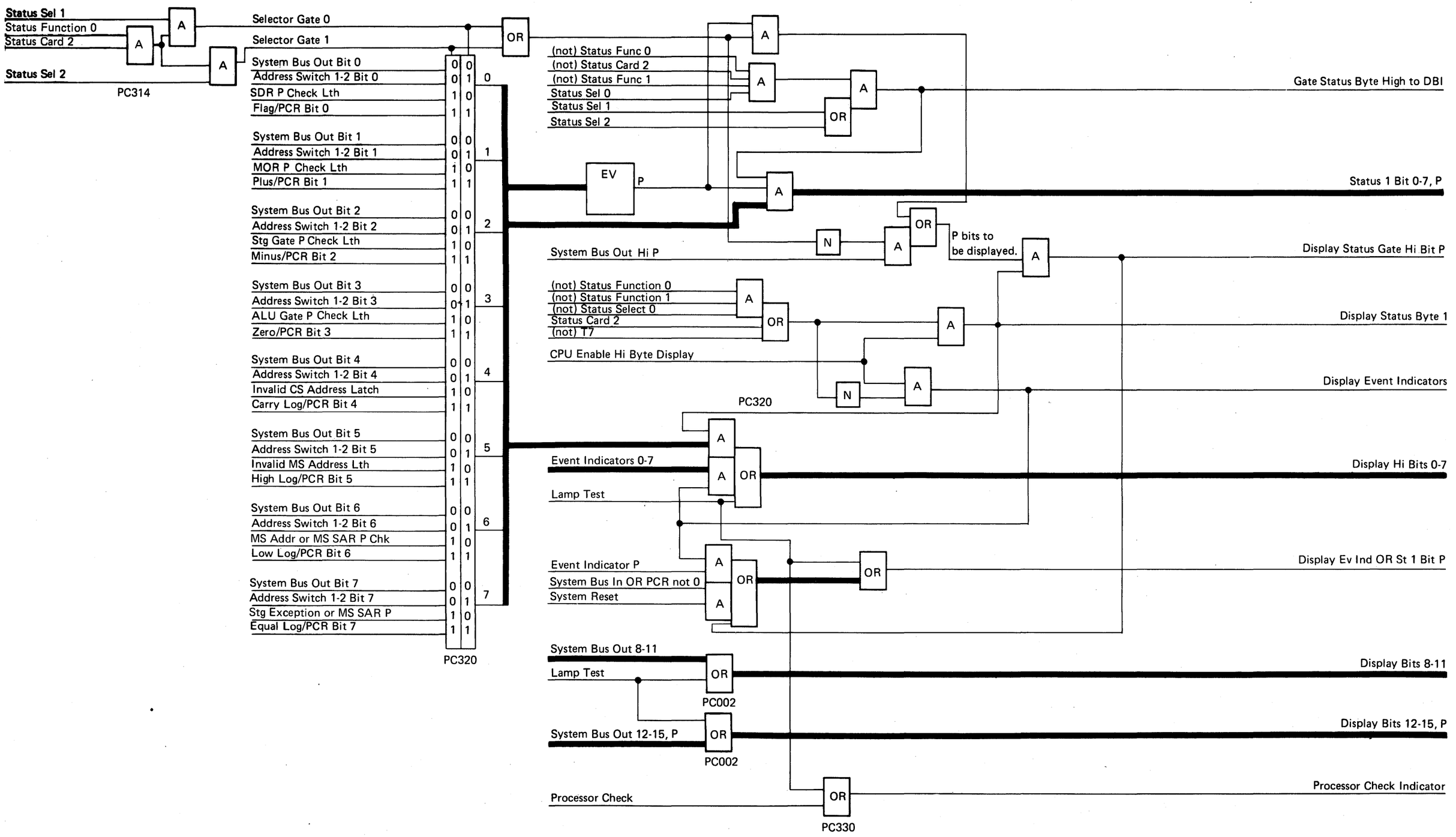
The Stop light goes off when you press the Load switch (on the operator panel), and when the main storage processor is running.

Mode Selector Switch

The following paragraphs describe the positions to which you can set the Mode Selector switch.

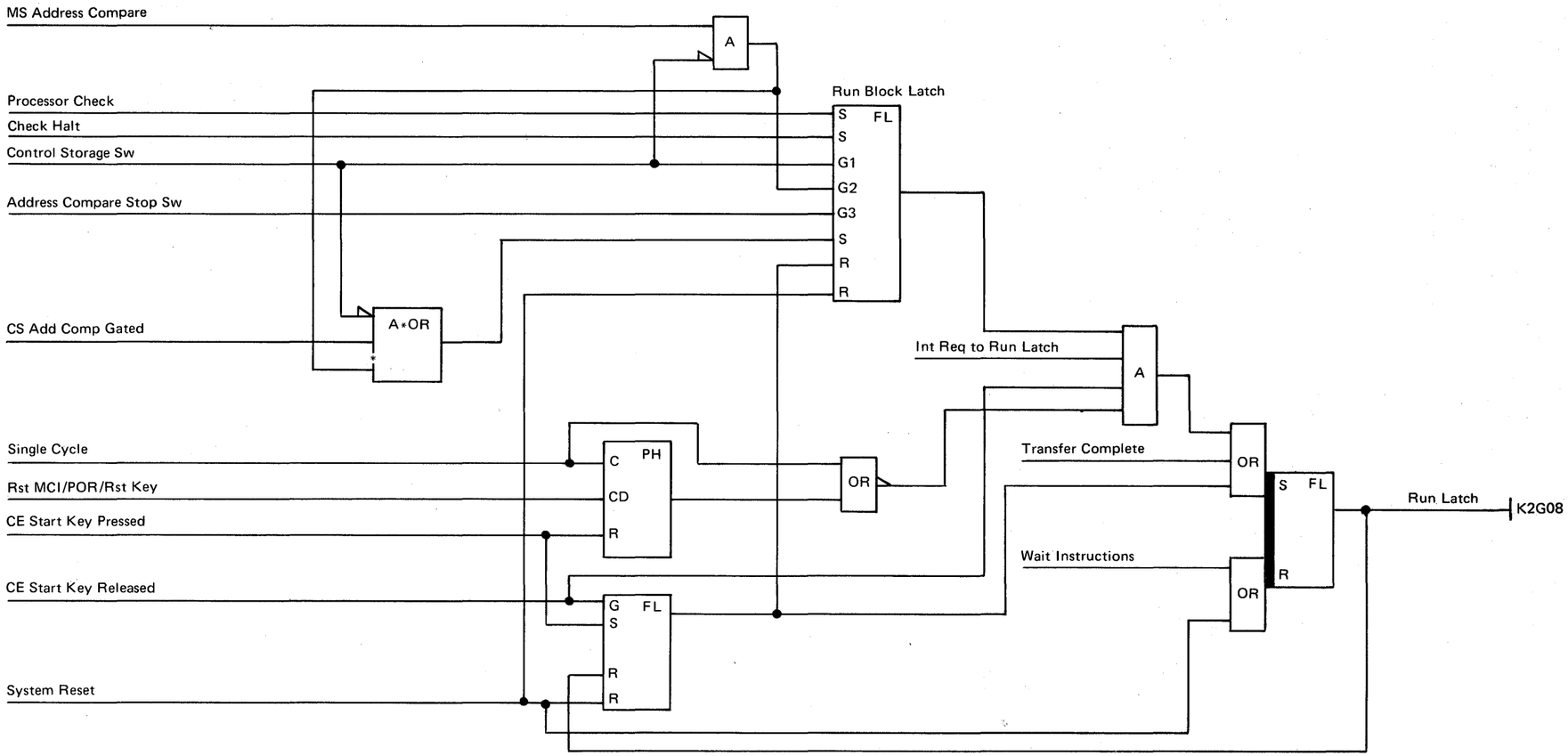
Proc Run (Processor Run) Position

You must leave the Mode Selector switch set to the Proc Run position when the system is running. If you move the Mode Selector switch to another position, the control processor and the main storage processor stop after executing their present instructions. To start the control processor again, set the Mode Selector switch to the Proc Run position and press the CE Start switch. The control processor starts at the instruction addressed by the microaddress register (MAR).


Status Sel 1
Status Function 0
Status Card 2
Status Sel 2
PC314
Selector Gate 0
Selector Gate 1
System Bus Out Bit 0
Address Switch 1-2 Bit 0
SDR P Check Lth
Flag/PCR Bit 0
System Bus Out Bit 1
Address Switch 1-2 Bit 1
MOR P Check Lth
Plus/PCR Bit 1
System Bus Out Bit 2
Address Switch 1-2 Bit 2
Stg Gate P Check Lth
Minus/PCR Bit 2
System Bus Out Bit 3
Address Switch 1-2 Bit 3
ALU Gate P Check Lth
Zero/PCR Bit 3
System Bus Out Bit 4
Address Switch 1-2 Bit 4
Invalid CS Address Latch
Carry Log/PCR Bit 4
System Bus Out Bit 5
Address Switch 1-2 Bit 5
Invalid MS Address Lth
High Log/PCR Bit 5
System Bus Out Bit 6
Address Switch 1-2 Bit 6
MS Addr or MS SAR P Chk
Low Log/PCR Bit 6
System Bus Out Bit 7
Address Switch 1-2 Bit 7
Stg Exception or MS SAR P
Equal Log/PCR Bit 7
PC320
OR
(not) Status Func 0
(not) Status Card 2
(not) Status Func 1
Status Sel 0
Status Sel 1
Status Sel 2
EV
P
Gate Status Byte High to DBI
Status 1 Bit 0-7, P
System Bus Out Hi P
N
P bits to
be displayed.
Display Status Gate Hi Bit P
(not) Status Function 0
(not) Status Function 1
(not) Status Select 0
Status Card 2
(not) T7
Display Status Byte 1
CPU Enable Hi Byte Display
Display Event Indicators
PC320
Event Indicators 0-7
Display Hi Bits 0-7
Lamp Test
Event Indicator P
System Bus In OR PCR not 0
System Reset
Display Ev Ind OR St 1 Bit P
System Bus Out 8-11
Display Bits 8-11
PC002
System Bus Out 12-15, P
Display Bits 12-15, P
PC002
Processor Check
Processor Check Indicator
PC330

Run Signal

The circuits that set and reset the 'run' latch are shown here.



PC400

Insn Step/Dply LSR (Instruction Step/Display Local Storage Register) Position

Set the Mode Selector switch to the Insn Step/Dply LSR position and press the CE Start switch to execute the next sequential control storage instruction. You can also use the Insn Step/Dply LSR position to display the contents of a selected local storage register in display bytes 0 and 1. To do this, select the local storage register (0-63) that you want to display by setting Display/Data switches 3 and 4 to hexadecimal values 00 through 3F as shown in the following figure:

Program Level	Display Bytes 0 and 1	Switch Setting (Hex)	Decimal Value
Main Level or Machine Check (interrupt level 0)	WR0	00	0
	WR1	01	1
	WR2	02	2
	WR3	03	3
	WR4	04	4
	WR5	05	5
	WR6	06	6
	WR7	07	7
MAR/MAB Stack 1	MAR	08	8
	MAB	09	9
	MAR (MC)	0A	10
	MAB (MC)	0B	11
	MAR (IL=1)	0C	12
	MAB (IL=1)	0D	13
	MAR (IL=2)	0E	14
	MAB (IL=2)	0F	15
Interrupt Level 1	WR0	10	16
	WR1	11	17
	WR2	12	18
	WR3	13	19
	WR4	14	20
	WR5	15	21
	WR6	16	22
	WR7	17	23
Interrupt Level 2	WR0	18	24
	WR1	19	25
	WR2	1A	26
	WR3	1B	27
	WR4	1C	28
	WR5	1D	29
	WR6	1E	30
	WR7	1F	31

Program Level	Display Bytes 0 and 1	Switch Setting (Hex)	Decimal Value
Interrupt Level 3	WR0	20	32
	WR1	21	33
	WR2	22	34
	WR3	23	35
	WR4	24	36
	WR5	25	37
	WR6	26	38
	WR7	27	39
MAR/MAB Stack 2	MAR (IL=3)	28	40
	MAB (IL=3)	29	41
	Spare	2A	42
	Spare	2B	43
	MAR (IL=4)	2C	44
	MAB (IL=4)	2D	45
	MAR (IL=5)	2E	46
	MAB (IL=5)	2F	47
Interrupt Level 4	WR0	30	48
	WR1	31	49
	WR2	32	50
	WR3	33	51
	WR4	34	52
	WR5	35	53
	WR6	36	54
	WR7	37	55
Interrupt Level 5	WR0	38	56
	WR1	39	57
	WR2	3A	58
	WR3	3B	59
	WR4	3C	60
	WR5	3D	61
	WR6	3E	62
	WR7	3F	63

Alter Stor (Alter Storage) Position

Use the Alter Stor position of the Mode Selector switch with the Stor Sel switch, the contents of the microaddress register (MAR), and the Address/Data switches to alter the contents of a control storage location from the CE panel.

To change the contents of a location in control storage, set the Stor Sel switch to the Ctl position. The microaddress register (MAR) contains the address of the control storage position to be changed. To change the contents of the MAR, see *Alter MAR Irpt Position* later in this section.

When you are changing the contents of a control storage location, information that you set in Address/Data switches 1 through 4 is stored in the addressed control storage location. Information that you set in these four switches also appears in display bytes 0 and 1.

After you set the Mode Selector and Stor Sel switches, press the CE Start switch to change the contents of a control storage location.

Note: Each time you press the CE Start switch to change the contents of a control storage location, the contents of the microaddress register are increased by 1. Therefore, you can change the contents of several sequential control storage locations without using the Alter MAR Irpt position of the Mode Selector switch to set each new address in the MAR.

CAUTION
Do not attempt to do an alter storage operation with the Stor Sel switch set to the Main position. You should not alter a specified main storage location from the CE panel using the alter storage procedure written here because you have no way of knowing if the address of the location is translated or real. You should use the SSP alter/display routine to alter main storage (see the *Data Areas Handbook*). (If you cannot use the SSP alter/display routine, you should use the procedure following this caution notice to alter main storage from the CE panel.)

If you must alter main storage without using the SSP alter/display routine, the following procedure allows you to use the CE panel:

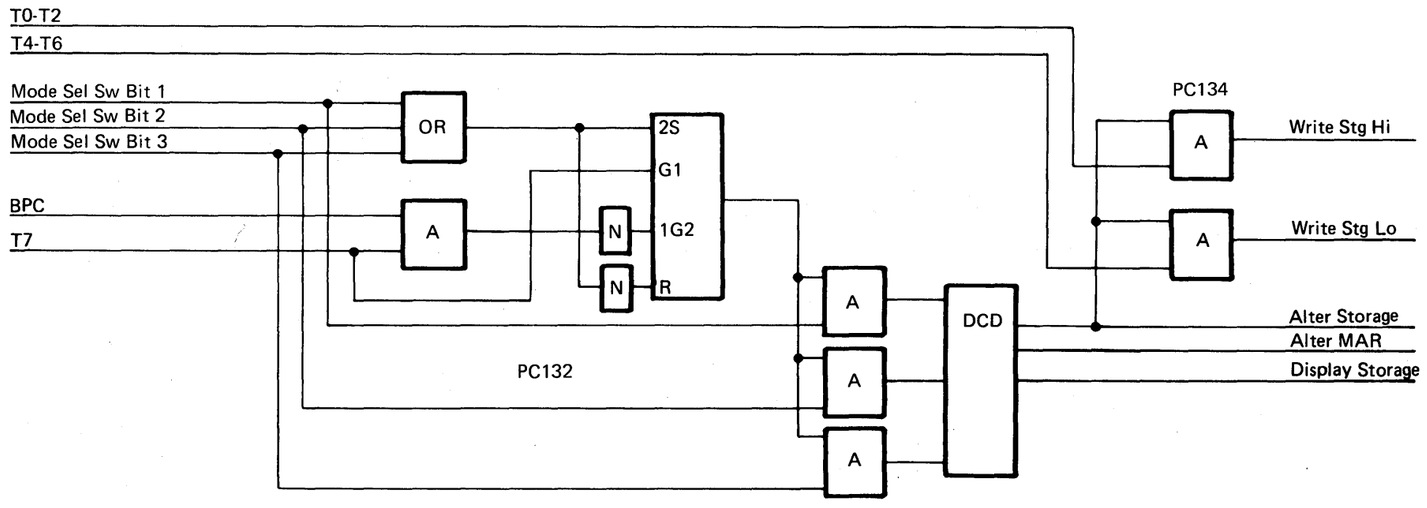
1. Reset the CMR (control mode register), the PMR (program mode register), and the BMR (backup mode register) to 00 by loading the following instructions into *control* storage addresses 0000 through 0009:

Data	Address
A13E	0000
A900	0001
49D1	0002
A13F	0003
A900	0004
49D1	0005
A13C	0006
A900	0007
49D1	0008
0000	0009

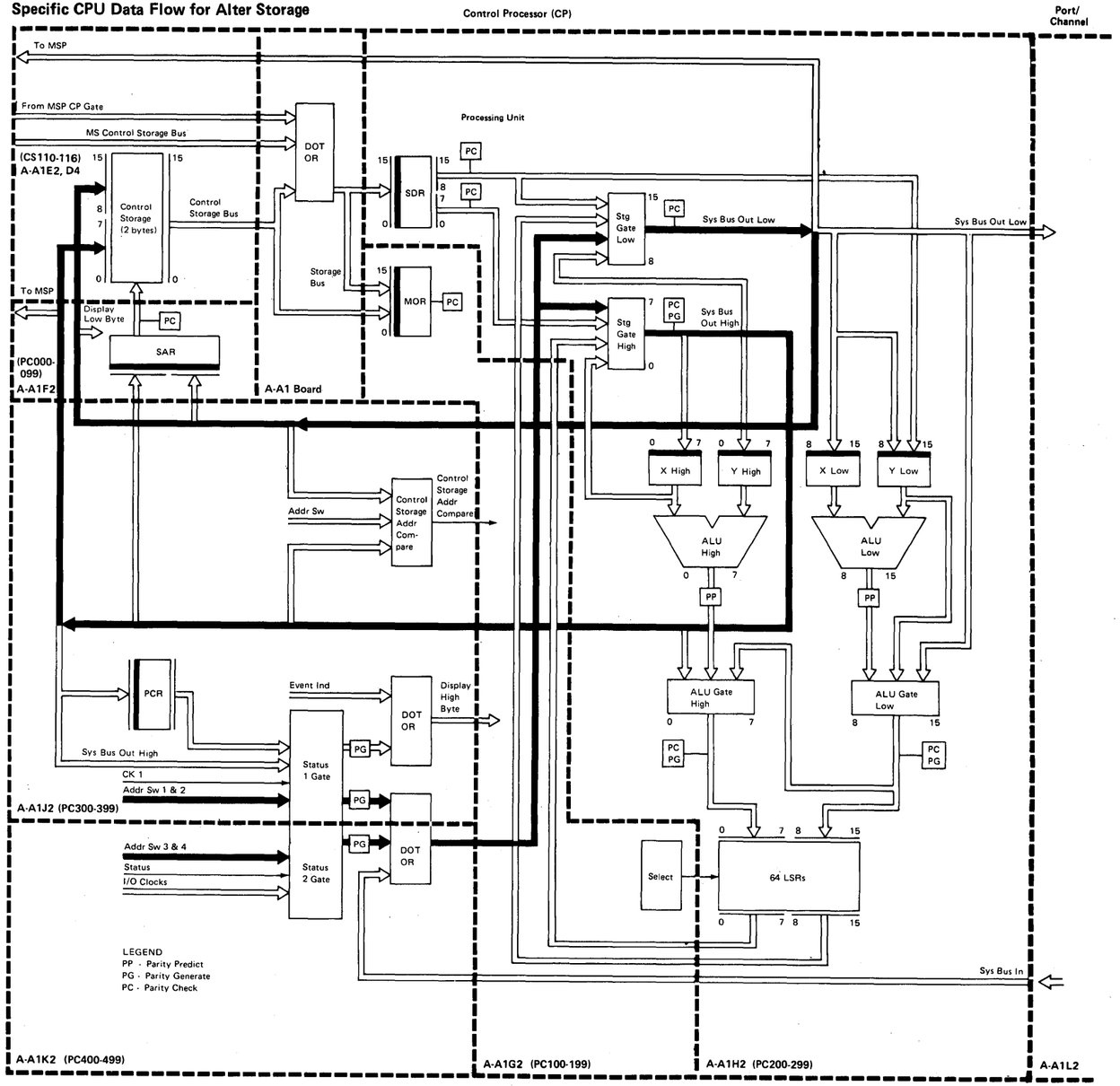
2. Press the Reset switch to alter the MAR to 0000.
3. Set the Mode Selector switch to the Proc Run position.
4. Press the CE Start switch.
5. Press the Reset switch. (The program will loop until the Reset switch is pressed.)

This procedure ensures that the main storage address (0000-FFFF) you specify is the real address and not a translated address. You can now alter the contents of main storage locations (0 to 64K) using the same procedure as for altering control storage. When altering main storage from the CE panel, use only Address/Data switches 3 and 4.

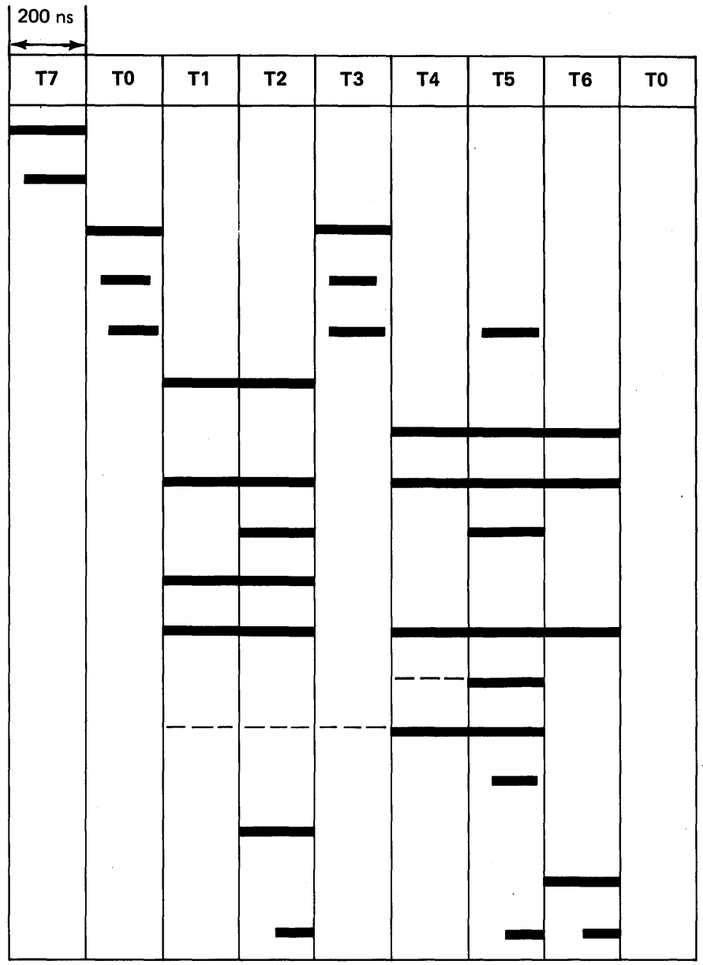
Alter Storage Function



Specific CPU Data Flow for Alter Storage



Alter Storage

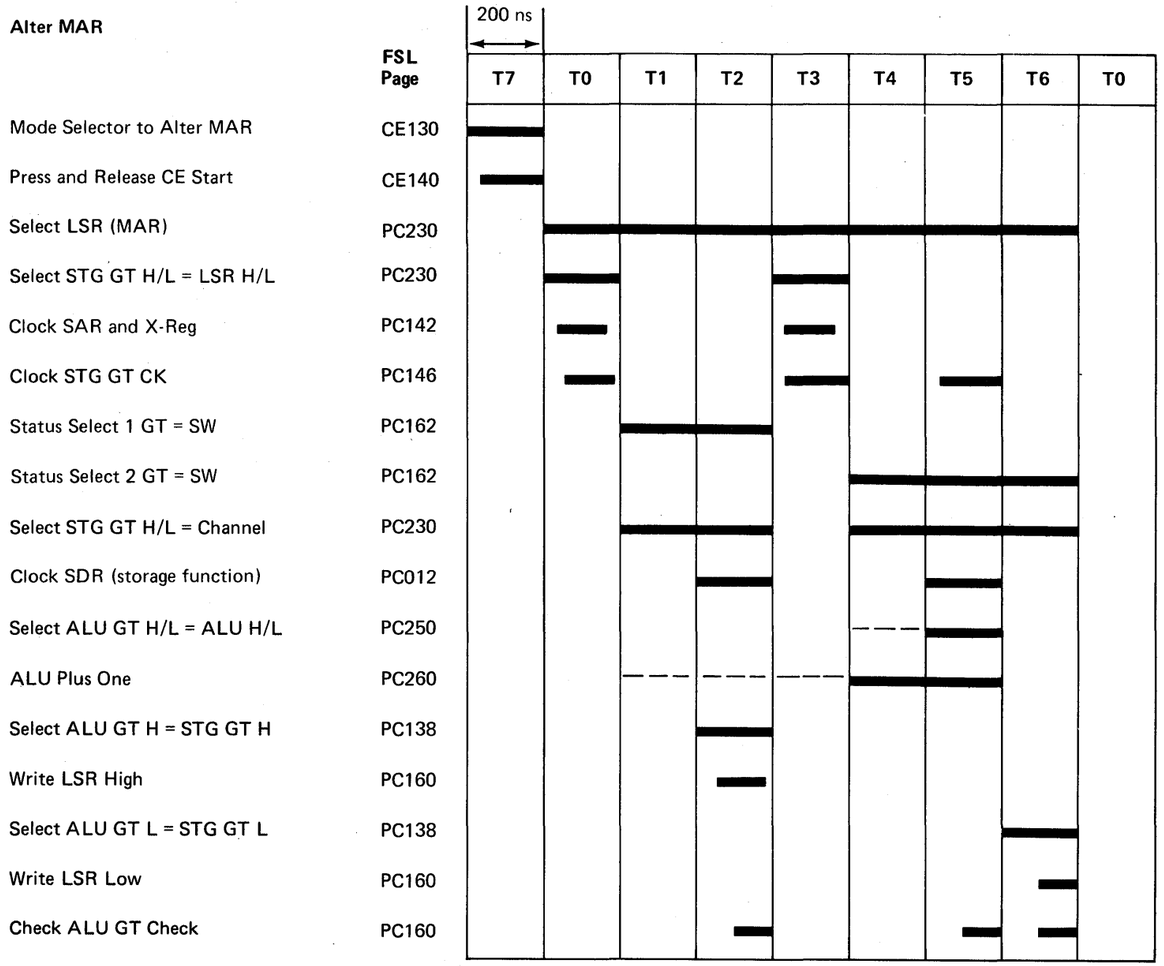


Alter MAR Irpt (Alter Microaddress Register Interrupt) Position

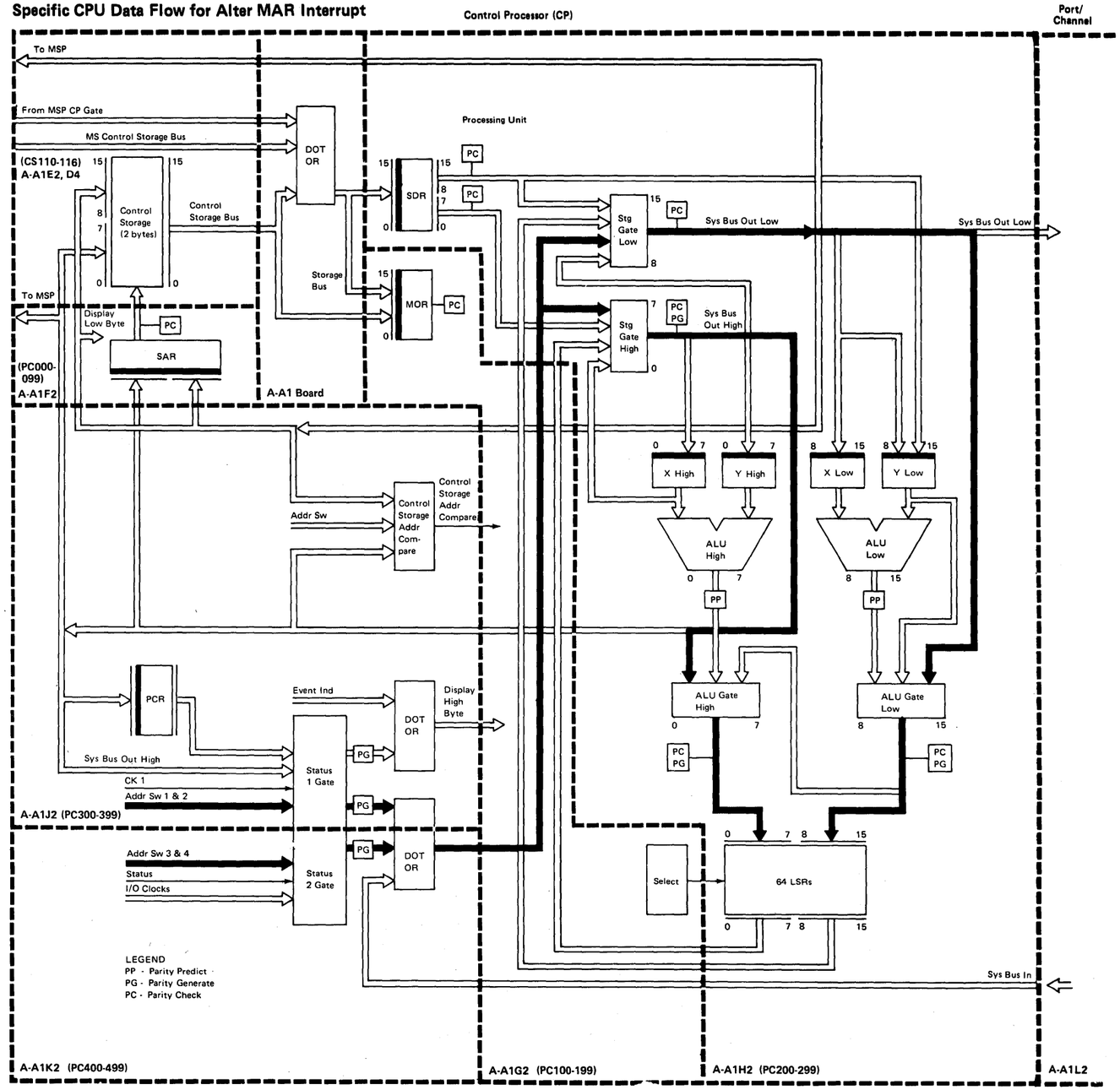
CAUTION
Before doing an alter MAR interrupt operation, display and write down the address in the microaddress register (see *Insn Step/Dply LSR Position* earlier in this section). You must reset the MAR to this address before continuing processing.

Set the Mode Selector switch to the Alter MAR Irpt position to change the contents of the MAR. When you set the Mode Selector switch to the Alter MAR Irpt position and press the CE Start switch, the address that you set in the four Address/Data switches is entered into the MAR of the interrupt level the control processor is in. Information that you set in these four switches also appears in display bytes 0 and 1.

Alter MAR



Specific CPU Data Flow for Alter MAR Interrupt



Dply Stor (Display Storage) Position

Set the Mode Selector switch to the Dply Stor position to display the contents of:

- The storage data register
- A control storage location

When you set the Mode Selector switch to the Dply Stor position, the contents of the storage data register appear in display bytes 0 and 1.

To display the contents of a control storage location:

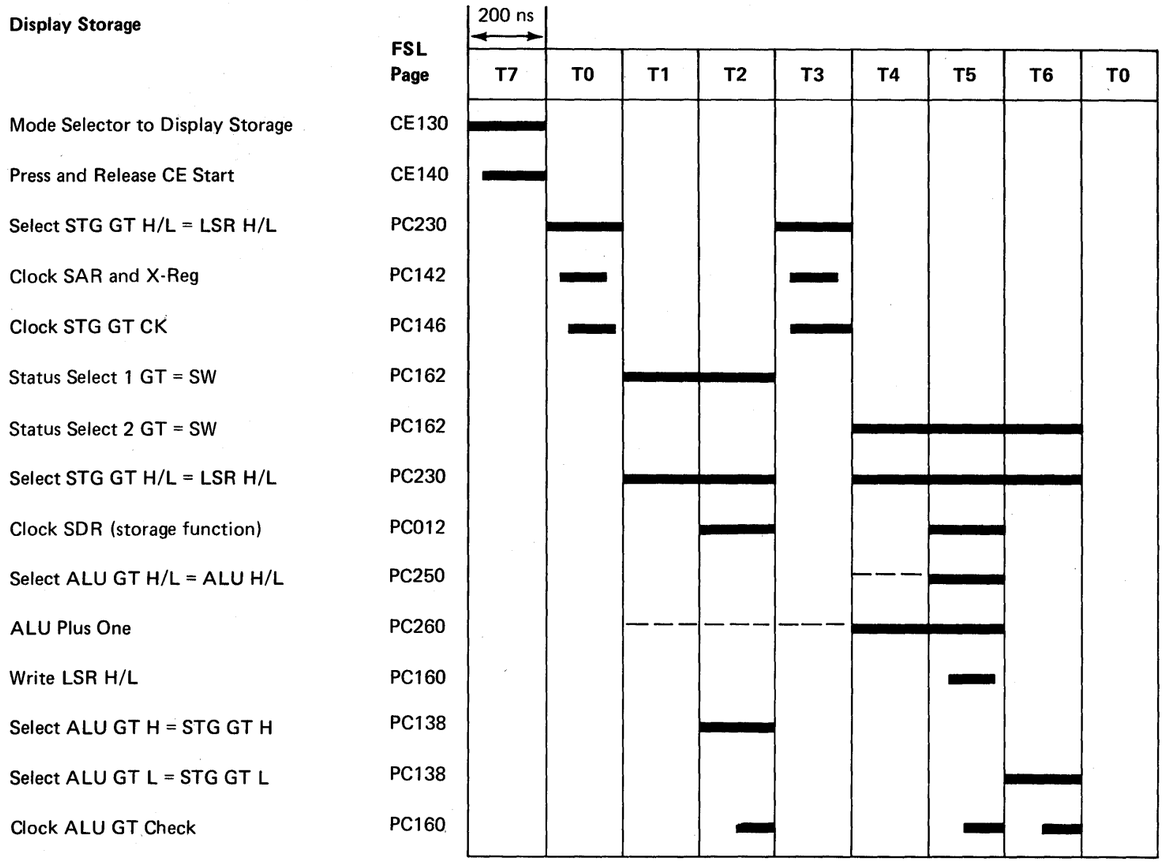
1. Set the Mode Selector switch to the Alter MAR Irpt position.
2. Use the Address/Data switches to enter the address of the control storage location you want to display into the microaddress register (see *Alter MAR Irpt Position* earlier in this section).
3. Set the Stor Sel switch to the Ctl position to select control storage.
4. Set the Mode Selector switch to the Dply Stor position and press the Reset switch and the CE Start switch.

When you complete these actions, the contents of the control storage location to be displayed are set into the storage data register and appear in display bytes 0 and 1.

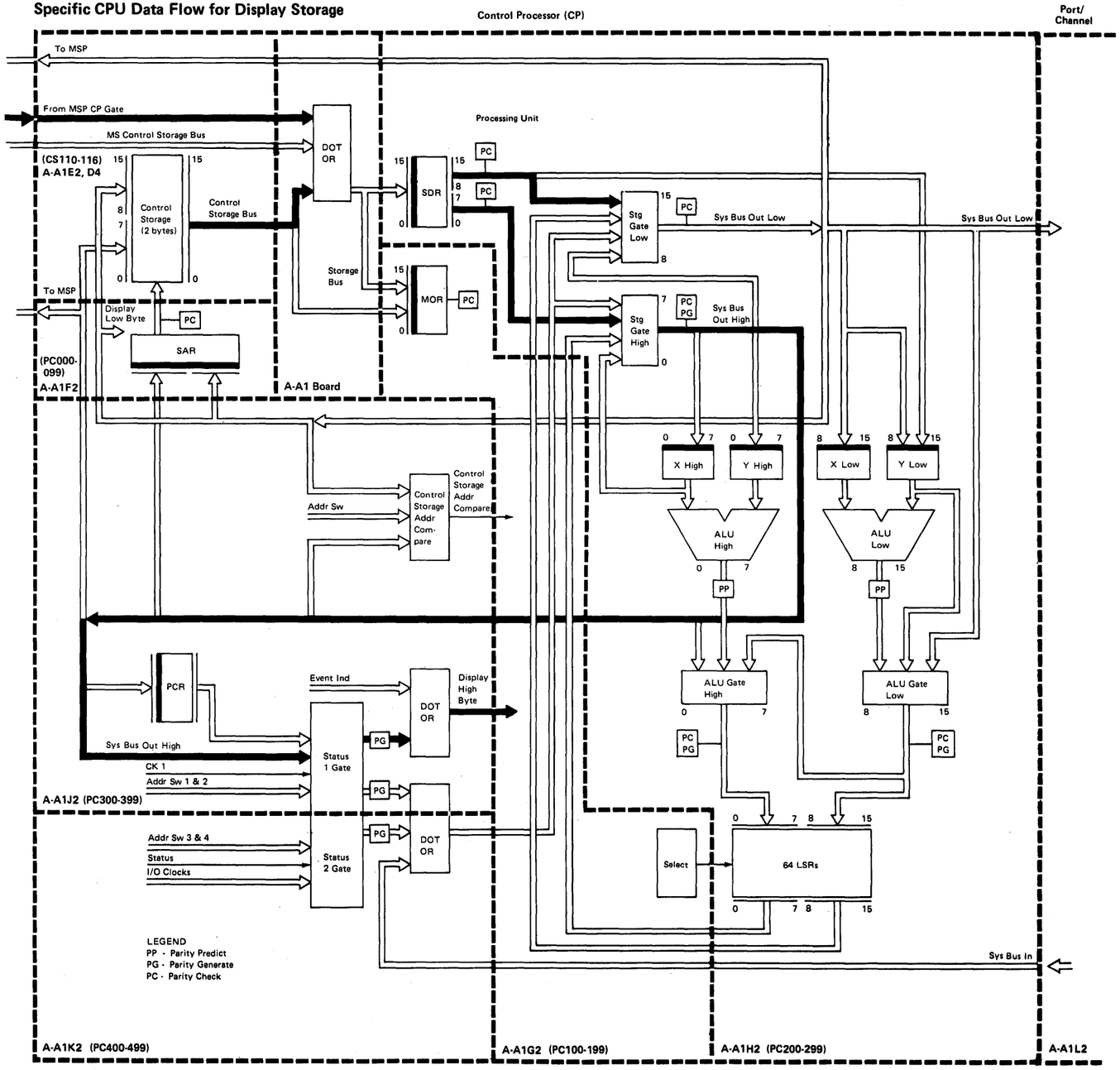
Note: Each time you press the CE Start switch during a display storage operation, the contents of the MAR are increased by 1. Therefore, you can display the contents of several sequential control storage locations without using the Alter MAR Irpt setting of the Mode Selector switch to set each new address in the MAR.

CAUTION
You should not attempt to display a specified main storage location from the CE panel by using the display storage procedure written here. Instead, you should use the SSP alter/display routine (see the *Data Areas Handbook*). If you must display a main storage location without using the SSP alter/display routine, you must first reset the CMR, the PMR, and the BMR to 00 (see *Alter Stor Position*, items 1 through 5, earlier in this section). The contents of main storage appear in display byte 1 only.

Display Storage



Specific CPU Data Flow for Display Storage



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Insn Step/Dply Chks (Instruction Step/Display Checks) Position

When you set the Mode Selector switch to the Insn Step/Dply Chks position and press the CE Start switch, the control processor executes the next control storage instruction. After each step, the processor error byte and the port error byte appear in display bytes 0 and 1 as shown in the following figures:

Processor Error Byte (Display Byte 0)

Bit	Error	Cause
0	Storage data register parity check	Parity in the storage data register is not correct.
1	Micro-operation register parity check	Parity in the micro-operation register is not correct.
2	Storage gate parity check	Parity at the output of the storage gate is not correct.
3	ALU gate parity check	The parity expected does not match the parity generated at the ALU gate.
4	Illegal control storage address/ storage address register	Control storage was addressed outside its limits. Bits 4 and 5 both on indicates that parity in the storage address register is not correct.
5	Control storage program check/storage address register	The control storage program remained in a loop for more than 7 seconds. Bits 4 and 5 both on indicates that parity in the storage address register is not correct.
6	Illegal main storage address/main storage address register	The real or translated main storage address used by the control storage program is greater than the main storage size of the system. Bits 6 and 7 both on indicates that parity in the main storage address register is not correct.
7	Storage exception/ main storage address register	The control storage program addressed a not valid address translation register; that is, an address translation register containing hexadecimal FF. Bits 6 and 7 both on indicates that parity in the main storage address register is not correct.

Decode of Bits 6 and 7

Bits 6 7	CMR Bit 7	PMR Bit 7	Cause
1 0	0	*	Invalid main storage address (real)
1 0	1	*	Invalid main storage address (translate)
0 1	1	*	Storage protect
0 1	*	1	MSP tried to alter PMR while PMR bit 7 = 1
1 1	*	*	MSAR parity check
1 1	1	*	ATR parity check

Legend: * = don't care

Port Error Byte (Display Byte 1)

Bit	Error	Cause
0	Data bus out parity check	Wrong parity was sensed by an attachment on the DBO bus (MPXPO bus out).
1	Incorrect device assigned	The port put an address on the DBO bus (MPXPO bus out), but no response was received from an attachment in the specified time. (The port activated the 'control out' line to address an attachment and the attachment did not respond by activating the 'service in' line in 5.4 μs.) This check also occurs if the DBO bus (MPXPO bus out) has wrong parity during the transmission of an address.
2	Data bus in parity check	Wrong parity was sensed by the port during the transmission of data from an attachment (MPXPO data in).
3	I/O time-out check	The channel sensed an error in the normal channel sequence. This check occurs if an attachment does not de-activate the 'service in' line in 5.4 μs after the rise of the 'service out' line.
4	Channel bus in/data bus in not zero	The I/O lines were not cleared in time. This check is made after the 'service out' line falls during T6 time and after a byte of data is transmitted to or from an attachment.
5	System bus out parity check	Wrong parity was sensed on the data sent from the processing unit to the port. (The check is made when the 'service out' line is active or when data is being sent to disk during a burst mode operation.)
6	Cycle steal operation check	Any processor or port parity check was sensed during a cycle steal operation.
7	Incorrect port	Bits 4–7 of work register 0 (high byte) were not 0000.

After a processor check occurs, set the Mode Selector switch to the Insn Step/Dply Checks position to display the error conditions that caused the processor check. If display bytes 0 and 1 contain all zeros, the processor check occurred while a check halt instruction was executing.

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Insn Step/Dply PCR (Instruction Step/Display Processor Condition Register) Position

When you set the Mode Selector switch to the Insn Step/Dply PCR position and press the CE Start switch, the control processor executes the next control storage instruction. After each step, the contents of the processor condition register appear in display byte 0.

Each time you press the CE Start switch, the next control storage instruction is executed. The contents of the processor condition register, which were changed by the instruction, are displayed in display byte 0.

Processor Condition Register

		Flag (bit 0)	Positive (bit 1)	Negative (bit 2)	Zero (bit 3)	Carry (bit 4)	High (bit 5)	Low (bit 6)	Equal (bit 7)
L/A1 or L/A2 Logical	Set		R1 or R2 = all ones and results ≠ zero	Results ≠ zeros and R1 or R2 ≠ all ones	Result = all zeros				
	Reset		Result = all zeros or R1 or R2 ≠ all ones	Result = all zeros or R1 or R2 = all ones	Result ≠ all zeros				
L/A1 or L/A2 Arithmetic	Set		Result has a carry and result ≠ zero	Result has no carry and result ≠ zero	Result = zero	Result had a carry (add) no borrow (sub)	Result has a carry and result ≠ zero	Result has no carry and result ≠ zero	
	Reset		Result = no carry or result = zero	Result has a carry or result = zero	Result ≠ zero	Result had no carry (add) a borrow (sub)	Result — no carry or result = zero	Result has a carry or result = zero	Result ≠ zero
Test Mask	Set		Tested bits = all ones	Tested bits ≠ all ones and tested bits ≠ all zeros	All tested bits = zero (or no bits tested)				
	Reset		Tested bits ≠ all ones	Tested bits = all ones or tested = all zeros	Tested bits ≠ zero				
Compare or Subtract Immediate	Set		Register data > immediate data	Register data < immediate data	Register data = immediate data				
	Reset		Register data is not > immediate data	Register data is not < immediate data	Register data is not = immediate data				
I/O Immediate Reset Carry— Set Equal	Set								Equal set on
	Reset					Carry set off	Decoded from carry and equal and set off	Decoded from carry and equal and set off	
I/O Immediate Load PCR	Set	Loaded bit 0 is on	Loaded bit 1 is on	Loaded bit 2 is on	Loaded bit 3 is on	Loaded bit 4 is on	Loaded bit 4 is on and bit 7 is off	Loaded bit 4 is off and bit 7 is off	Loaded bit 7 is on
	Reset	Loaded bit 0 if off	Loaded bit 1 if off	Loaded bit 2 is off	Loaded bit 3 if off	Loaded bit 4 is off	Loaded bit 4 is off or loaded bit 7 is on	Loaded bit 4 is on or loaded bit 7 is on	Loaded bit 7 is off
Reset *Note:* Power on Reset or CE Reset	Set								Equal set on
	Reset	Set off	Set off	Set off	Set off	Carry set off	Decoded from 4 and 7 and set off	Decoded from 4 and 7 and set off	
I/O Immediate Flag Length	Set	Set on							
	Reset	Set off							

Sys Insn Step (System Instruction Step) Position

Use this position only in conjunction with the SSP alter/display routine, option 5 or 6 (see the *Data Areas Handbook*).

When you set the Mode Selector switch to the Sys Insn Step position, both processors stop. To start the control processor clock again, you must press and release the CE Start switch.

CSIPL and MSIPL Switches

The positions of the CSIPL (control storage initial program load) and MSIPL (main storage initial program load) switches determine if the initial program load sequence will be from disk or diskette. During normal system operation, both the CSIPL and the MSIPL switches are set to the Disk position.

The combinations of MSIPL and CSIPL switch settings and their uses are:

Switch	Setting	Function
MSIPL CSIPL	Disk Disk	Load the SSP (see the *Control Storage Logic Manual*).
MSIPL CSIPL	Diskette Disk	Reload the SSP from diskette.
MSIPL CSIPL	Diskette or Disk Diskette	Load the diagnostic supervisor from diskette for dedicated maintenance.

Proc Interrupt (Processor Interrupt) Lights

The Proc Interrupt lights indicate the interrupt level being used, as shown in the following figure:

Lights 4	2	1	Interrupt Level
1	1	1	0 (machine check)
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
0	0	0	Main level

1 = light on
0 = light off

Reset Switch

When you press the Reset switch, a system reset takes place as follows:

- The microaddress register (MAR) for interrupt level 0 is set to hexadecimal 0000.
- The control processor timing circuits are initialized.
- The error lights and status lights are reset. (Information stored in the power failure latches is not lost.)
- The processor condition register (PCR) is set to the equal condition.
- The disk access mechanism is returned to home (track 0).

After a system reset:

- Press the CE Start switch to write the contents of main storage, control storage, and controllers to the CE cylinder(s) on disk.
- Press the Load switch (on the operator panel) to start the system again.

Address/Data and Display/Data Switches

You can use the four Address/Data switches to enter addresses and data into storage. You can also use the two Display/Data switches to display the contents of the local storage registers. Details about how to use the Address/Data and Display/Data switches are included in the description of the Mode Selector switch earlier in this section.

Clock Light

The Clock light is on:

- When the control processor is executing an instruction.
- When an I/O attachment is operating in cycle-steal mode.

Force Clock Switch

Set the Force Clock switch to the On position to cause continuous control processor processing cycles. If the Mode Selector switch is set to the Alter Stor position, information set in the Address/Data or Display/Data switches is loaded into sequential locations of control storage, starting at the address in the microaddress register. Set the Force Clock switch to the Off position to stop the operation. If the Processor Check light (on the operator panel) comes on, press the Reset switch.

When set to the On position, the Force Clock switch overrides the setting of the Check switch. Therefore, the control processor may be running even if the Check switch is set to the Stop position.

CAUTION
You should not attempt to load sequential locations of main storage from the CE panel by using the procedure written here. Instead, you should use the SSP alter/display routine (see the *Data Areas Handbook*). If you must load sequential locations of main storage without using the SSP alter/display routine, you must first reset the CMR, the PMR, and the BMR to 00 (see *Alter Stor Position*, items 1 through 5, earlier in this section).

Check Switch

The position of the Check switch determines if the system continues to run or stops when a machine check or parity error occurs, as follows:

- When the Check switch is set to the Stop position, the system stops when the error occurs.
- When the Check switch is set to the Run position, the error is stored in the processor error byte or the port error byte, but the system continues to run.

The On position of the Force Clock switch overrides the Stop position of the Check switch.

CE Start Switch

Press the CE Start switch to start the processing of instructions. The first instruction executed is at the address in the microaddress register (MAR).

Lamp Test Switch

When you press the Lamp Test switch:

- If system power is on, all system lights come on.
- If system power is off, but the circuit breaker (CB1) is on:
  - The Power Check and Thermal Check lights on the operator panel come on.
  - The display byte 0 lights on the CE panel come on.

Note: The circuit breaker is in the AC box, behind the left front cover.

Stor Sel (Storage Select) Switch

The Stor Sel switch determines if main storage or control storage will be addressed. The Stor Sel switch must be set to the Ctl position when performing operations from the CE panel that address control storage. These operations include display storage (Dply Stor), alter storage (Alter Stor), and address compare (Add Comp).

Add Comp (Address Compare) Switch

If an address compare occurs while the Add Comp switch is set to the Run position:

- An address-compare synchronization signal is generated for CE diagnostic use. This signal is available at pin A1K2D12.
- System operation continues without interruption.

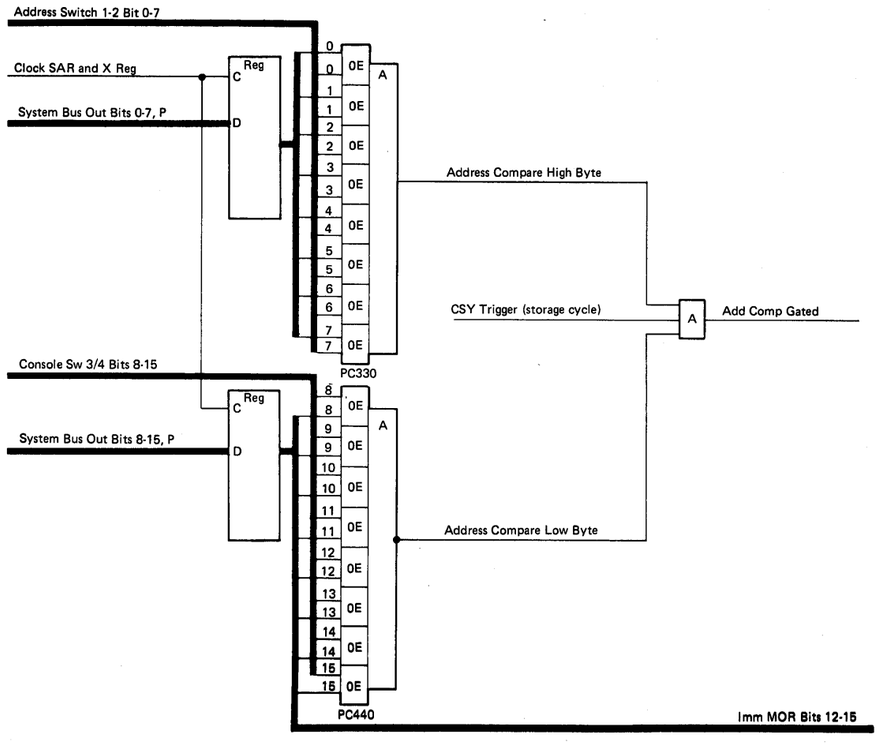
If an address compare occurs while the Add Comp switch is set to the Stop position:

- An address-compare synchronization signal is generated. This signal is available at pin A1K2D12.
- If the address compare occurs for a main storage address (Stor Sel switch set to the Main position):
  - The main storage processor stops.
  - The Stop light comes on.
  - The alter/display option menu appears on the system console (unless certain terminal operations are being performed).

  Note: The alter/display routine must be terminated before processing continues. (See the *Alter/Display* section of the *Data Areas Handbook* for more information on main storage address compares.)
- If the address compare occurs for a control storage address (Stor Sel switch set to the Ctl position):
  - The main storage processor and the control processor stop.
  - You must press the CE Start switch before processing continues.

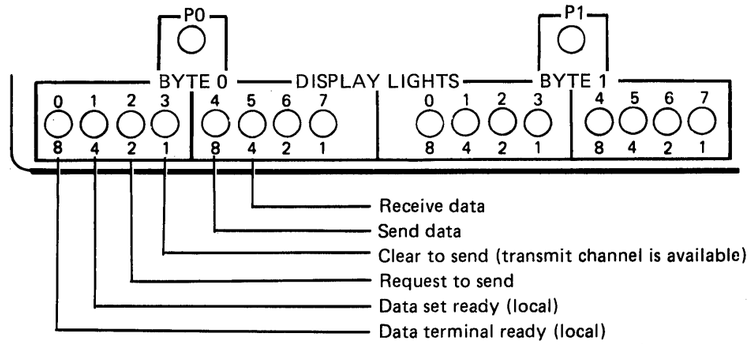
The time at which the system stops is determined as follows:

1. If an address compare occurs for a main storage address (Stor Sel switch set to the Main position):
   a. The main storage processor completes the main storage instruction being executed, and then stops.
   b. The control processor continues to run.
2. If an address compare occurs for a control storage address (Stor Sel switch set to the Ctl position):
   a. If an I/O cycle-steal operation is being executed, the system stops after all I/O cycle-steal operations are complete.
   b. If an I/O cycle-steal operation is *not* being executed, the control processor clock stops after executing the instruction at the address set in the Address/Data switches. The main storage processor clock stops after all I/O cycle-steal operations are complete.



Comm Dply (Communications Display) Switch

The Comm Dply switch is present on the CE panel only if a communications adapter is installed on the system. When set to the On position, the Comm Dply switch enables the CE display lights for byte 0 (bits 0-7). The lights indicate the status of the communication interface lines as shown in the following figure:



Dply Pwr Chk (Display Power Check) Switch

This switch is for CE diagnostic use only. Its use is described in paragraphs 05-420 and 05-430 of the *5340 System Unit Maintenance Manual*.

Pwr Fault Dply (Power Fault Display) Switches

These two switches are for CE diagnostic use only. Their use is described in paragraphs 05-420 and 05-430 of the *5340 System Unit Maintenance Manual*.

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