IBM

PUBLICATION DRAWING

Part number	4237866
Date	Change number
01 APRIL 79	834807
25 JULY 79	834824

Base form number: SY31-0458

Title: System/34 5340 System Unit Theory Diagrams Manual

NOTE: All items following the last row of asterisks are to be shipped.

Change number	Form/TNL	Description/Comments
832742	SY31-0458	First release
832742M	SY31-0458	Second release
832850	SY31-0458	Version 1, first customer ship
832964	SN31-6216	TNL to correct the first 6 sections of the manual
833024	SN31-6217	TNL to correct the last 6 sections of the manual
832999	SY31-0458-1	Major revision of manual; Ship new version of manual.
834777	SY31-0458-2	Major revision of manual; Version 3
834807	SN31-6268	TNL to Section 14 to support the new style picker.
834824	SY31-0458-3	Major revision of manual; Version 4

A

VOL C MLM OVERVIEW

5340
VOLUME
A
MAINTENANCE
ANALYSIS
PROCEDURES
S/N_____
MAP'S 0000-1149
BOOK 1 OF 2

0000-0011 MAP TABLE OF CONTENTS AND DESCRIPTION
0101-0199 SYSTEM ENTRY
0303-0351 INITIAL PROGRAM LOAD
0500-0584 POWER
0700-0782 5211 PRINTER CONTROLLER
0800-0842 3262 PRINTER CONTROLLER
0900-0999 62EH DISK ATTACHMENT
1000-1099 62PC DISK ATTACHMENT
1101-1149 WORK STATION CONTROLLER (PART 1)

5340
VOLUME
A
MAINTENANCE
ANALYSIS
PROCEDURES
S/N_____
MAP'S 1160-89XX
BOOK 2 OF 2

1160-1199 WORK STATION CONTROLLER (PART 2)
1301-1309 CE PANEL
1501-1589 CONTROL PROCESSOR
2101-2105 OPERATOR PANEL
2718-2719 72MD DISKETTE DRIVE
31XX-39XX DATA COMMUNICATIONS ATTACHMENT
41XX-4171 1255 ATTACHMENT
5001-5010 INTERMITTENT FAILURE REPLACEMENT LIST
81XX-89XX ERROR LOG

5340
VOLUME
B
MAINTENANCE
S/N_____
BOOK 1 OF 1

01-000 INTRODUCTION TO MAINTENANCE
02-000 REFERENCE INFORMATION
05-000 POWER
07-000 5211 PRINTER ATTACHMENT
09-000 62EH DISK DRIVE
10-000 62PC DISK DRIVE
11-000 WORK STATION ATTACHMENT
13-000 CE PANEL
15-000 PROCESSING UNIT
21-000 OPERATOR PANEL
23-000 33FD DISKETTE DRIVE
25-000 53FD DISKETTE DRIVE
27-000 72MD DISKETTE DRIVE
31-000 DATA COMMUNICATIONS
40-000 1255 MICR ATTACHMENT
45-000 INSTALLATION INSTRUCTIONS
80-000 ERROR INFORMATION INTRODUCTION
81-000 MAIN STORAGE PROCESSOR
82-000 CONTROL PROCESSOR
83-000 DISK
84-000 DISKETTE
85-000 LINE PRINTER
86-000 WORK STATION CONTROLLER
87-000 5251 DISPLAY STATION
88-000 5256 PRINTER
89-000 DATA COMMUNICATIONS
99-000 DIAGNOSTIC SERVICE GUIDE
PARTS CATALOG

5340
VOLUME
C
THEORY
DIAGRAMS
S/N_____
BOOK 1 OF 1

INTRODUCTION
CONTROL PROCESSOR
MAIN STORAGE PROCESSOR
INTERRUPTS AND CYCLE STEAL REQUESTS
CHANNEL
CONTROL PANELS
62EH DISK DRIVE AND ATTACHMENT
62PC DISK DRIVE AND ATTACHMENT
DISKETTE DRIVE AND ATTACHMENT(LEVEL 1)
DISKETTE DRIVE AND ATTACHMENT(LEVEL 2)
5211 PRINTER ATTACHMENT
ATTACHMENT CONTROLLERS
WORK STATION ATTACHMENT
DATA COMMUNICATIONS
3262 PRINTER ATTACHMENT

5340
VOLUME
D
FIELD
SERVICE
LOGICS
S/N_____
BOOK 1 OF 1

AA000 TABLE OF CONTENTS
AA100 INTRODUCTION
ABXXX CABLE AND PIN INFORMATION
ACXXX PLUGCHARTS
ADXXX NET LISTS AND PIN LISTS
AEXXX SECOND LEVEL LOGIC DIAGRAMS
AFXXX VOLTAGE DISTRIBUTION
AYXXX LOGIC BLOCK SYMBOLOGY
CEXXX CE PANEL
CHXXX CHANNEL
CSXXX CONTROL STORAGE
DXXXX DISKETTE ATTACHMENT LEVEL 1 (DL, DM, AND DX PAGES)
FAXXX DATA COMMUNICATIONS ATTACHMENT
FLXXX 72MD DSKT
FMXXX 72MD D.S.
FXXXX 72MD DRIVE
GXXXX DISK ATTACHMENT (GE, GF, AND GV PAGES)
HXXXX 62PC DISK ATTACHMENT (HA, HB, HC, HD, HE, AND HH PAGES)
MRXXX 1255 ATTACHMENT
MSXXX MSP STORAGE
OPXXX OPERATOR PANEL
PAXXX DEVICE ATTACHMENTS FOR CHANNEL
PCXXX CONTROL PROCESSOR
PMXXX MAIN STORAGE PROCESSOR
PRXXX 5211 PRINTER ATTACHMENT
PSXXX PRINTER CONTROLLER
PTXXX 3262 PRINTER ATTACHMENT
PUXXX 3262 PRINTER ATTACHMENT
WSXXX WORK STATION CONTROLLER
YAXXX POWER

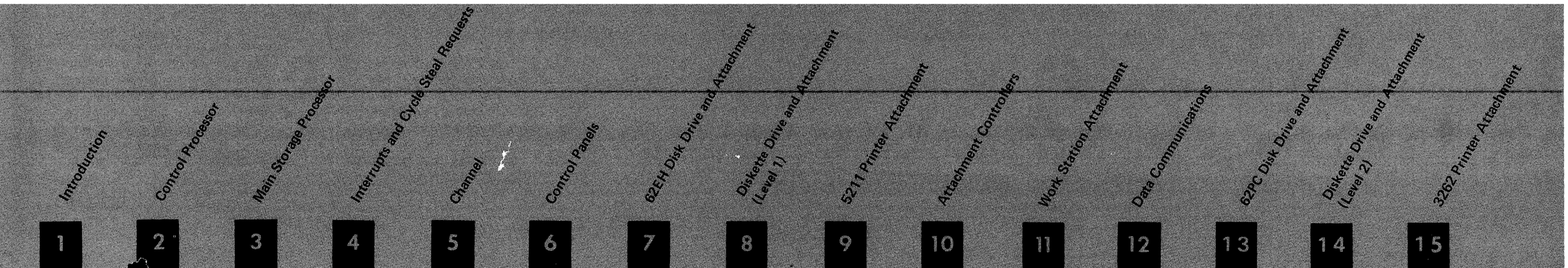
EC HISTORY		DRAWING TITLE
27 DEC 77	832902	VOL C MLM OVERVIEW
29 JUN 78	832999	MACH 5340
13 DEC 78	834777	PART NO. 4237998
25 JUL 79	834824	CLASSIFICATION
		JLC 01 DEC 77

C

IBM CORP

SY31-0458-3

IBM System/34
5340 System Unit
Theory Diagrams Manual



Preface

This manual contains information about the operation of the IBM System/34. The manual is for the customer engineer who is troubleshooting a failure that the System/34 MAPs (maintenance analysis procedures) failed to isolate, or for one who wishes to improve his knowledge of System/34 operation. Each major system function is described in a separate section, as listed in the *Contents*.

Customer engineers using this manual are assumed to have been trained on System/34 as described in the *IBM System/34 Technical Service Letter*.

There are several CAUTION messages in this manual. You can use the blank lines below each message to translate the message into your own words.

Note: This manual follows the convention that *he* means *he or she*.

Related Publications

- *IBM System/34 5340 System Unit Maintenance Manual*, SY31-0457
- *IBM System/34 Control Storage Logic Manual*, SY31-0562
- *IBM System/34 Functions Reference Manual*, SA21-9243
- *IBM System/34 System Data Areas and Diagnostic Aids Handbook*, LY21-0049
- *IBM System/34 Program Products and Physical Setup, Installation and Modification Reference Manual*, SC21-7689
- *IBM System/34 System Support Program Logic Manual: System*, LY21-0050
- *IBM 5211 Printer Maintenance Information*
- *IBM 3262 Printer Maintenance Information*

Fourth Edition (August 1979)

This is a major revision of, and obsoletes, SY31-0458-2 and Technical Newsletter SN31-6268. Because the changes and additions are extensive, this publication should be reviewed in its entirety.

Changes are periodically made to the information herein; before using this publication in connection with the operation of IBM systems, be sure you have the latest edition and any technical newsletters.

Use this publication only for the purposes stated in the *Preface*.

This publication could contain technical inaccuracies or typographical errors. Use the Reader's Comment Form at the back of this publication to make comments about this publication. If the form has been removed, address your comments to IBM Corporation, Publications, Department 245, Rochester, Minnesota, 55901. IBM may use and distribute any of the information you supply in any way it believes appropriate without incurring any obligation whatever. You may, of course, continue to use the information you supply.

Contents

LIST OF ABBREVIATIONS AND ACRONYMS . ix

LEGEND xiii

INTRODUCTION TO IBM SYSTEM/34 1-1

CONTROL PROCESSOR 2-1
DATA FLOW AND CLOCKS 2-1
Data Flow 2-1
Clocks 2-3
System 2-3
I/O Attachment and Controller 2-4
Storage 2-4
OPERATIONS 2-5
IPL-Customer User Programs 2-5
Control Storage Initial Program Load (CSIPL) . . 2-5
Main Storage Initial Program Load (MSIPL) . . 2-6
IPL Timing Sequence 2-7
Display Light Sequence (Byte 0) 2-7
Disk Operation 2-8
Disk Sequence 2-9
62EH Disk Timing 2-11
62PC Disk Timing 2-12
IPL-Customer SSP from Diskettes 2-13
IPL-CE Diagnostics 2-15
Diskette CSIPL Diagnostic Sequence 2-17
Diskette Timing (Level 1 Attachment) 2-18
33FD/53FD CSIPL Flowchart (Level 1 Attachment) 2-19
Diskette Timing (Level 2 Attachment) 2-21
33FD/53FD/72MD CSIPL Flowchart (Level 2 Attachment) 2-22
Error Indications 2-24
CSIPL Switch Options 2-27
Instructions 2-28
Instruction Times 2-28
Sequence and Timing 2-28
Routine Printout 2-29
Mnemonic Listing 2-30
INSTRUCTION EXECUTION 2-32
Signals, Gating Lines, and Logical Functions for Timing Charts 2-32
Branch (B) 2-34
Branch (Stop Condition) (B) 2-35
Branch and Link (BAL) 2-36
Jump on Condition (JC) 2-38
Jump on Condition (Stop Condition) (JC) 2-40
Logical/Arithmetic 1 (XR, ZAR, OR, NCR, NR, OCR, DEC, ACYR, SR, AR, SCYR, INC) 2-42
Condition Code for Logical Operations 2-42
Condition Code for Arithmetic Operations . . 2-42
Logical/Arithmetic Functions 2-43
Logical/Arithmetic 2 (XR, ZAR, OR, NCR, NR, OCR, DEC, ACYR, SR, AR, SCYR, INC) 2-46
Condition Code for Logical Operations 2-46
Condition Code for Arithmetic Operations . . 2-46
Logical/Arithmetic Functions 2-47
Load Immediate (LI) 2-50
Compare Immediate (CI) 2-52
Subtract Immediate/Add Immediate (SI, AI) . . 2-54
Test Mask (TM) 2-56
Set Bits On (SBN) 2-58
Set Bits Off (SBF) 2-60
Storage (LC, LM, STC, STM) 2-63
Instruction List 2-63
Main Storage Access by Control Processor 2-66
Control Processor Control of MSAR 2-67
MSP Bus Line Control 2-68
Main Storage Address Decoding 2-69
Register Control (WMPR, RMPR) 2-73
Instruction List 2-73
Storage Direct (L, ST) 2-76
Move Local Storage Register (MVR) 2-78
Hexadecimal Branch (HBN, HBZ) 2-80
Hexadecimal Move (SRL, SRLD, MZZ, MZN) . . 2-82
I/O Immediate 2-88
I/O Load or I/O Control Load (IOL, IOCL) . . 2-94
I/O Sense or I/O Control Sense (IOS, IOCS) . 2-96
Sense Interrupt Level Status Byte (SILSB) . . 2-98
Control Processor Load Function (MPLF) . . . 2-99
Control Processor Sense (MPS) 2-99
I/O Storage (WTCL, WTCH, RDCL, RDCH, WTM, RDM) 2-100
Instruction List 2-100
Jump on I/O Condition (JIO) 2-104
FUNCTIONAL UNITS 2-108
Control Storage 2-109
Storage Address Register 2-109
Micro-Operation Register 2-109
X-Registers and Y-Registers 2-109
Arithmetic and Logic Units 2-110
Arithmetic and Logic Unit Gates 2-111
Arithmetic and Logic Unit Parity Predict . . . 2-111
Storage Data Register 2-112
Local Storage Registers 2-113
Processor Condition Register 2-114
Storage Gate High/Low 2-116
Status 1 Gate 2-117
Status 2 Gate 2-118
ERROR CONDITIONS 2-119
Control Processor Checks 2-119
Processor Errors 2-119
Error Conditions (Second Level) 2-119
Machine Check Interrupt and Processor Check Generation 2-120
MSP Hardware Checks 2-121
Control Processor Checks 2-122
SDR Parity Check Generation 2-123
MOR Parity Check 2-124
Storage Gate High/Low Parity Check and Generation 2-125
ALU Gate High Parity Check and Generation 2-126
ALU Gate Low Parity Check and Generation 2-127
Control Storage SAR Parity Check 2-128
MSP Check Bits 1 and 2 2-129

MAIN STORAGE PROCESSOR 3-1
DATA FLOW AND CLOCK 3-2
Data Flow 3-2
Parity Checking and Generation 3-2
Clock 3-4
OPERATIONS 3-6
Instruction and Execution Cycles 3-6
Sequential Instruction Execution 3-6
I/O Data Movement 3-6
Instruction Formats 3-6
Instruction Fetch Operation 3-8
Addressing 3-10
Direct Addressing 3-10
Indexing 3-10
Address Translation 3-10
INSTRUCTION EXECUTION 3-12
Arithmetic Instructions 3-13
Zero and Add Zoned (ZAZ) 3-13
Add Zoned Decimal (AZ) 3-15
Subtract Zoned Decimal (SZ) 3-16
Recomplement Cycle 3-18
Add Logical Characters (ALC) 3-21
Subtract Logical Characters (SLC) 3-22
Add to Register (A) 3-24
Data Control Instructions 3-26
Move Hexadecimal Character (MVX) 3-26
Move Characters (MVC) 3-28
Edit (ED) 3-30
Insert and Test Characters (ITC) 3-32
Move Logical Immediate (MVI) 3-34
Set Bits On Masked (SBN) 3-35
Set Bits Off Masked (SBF) 3-35
Store Register (ST) 3-36
Load Register (L) 3-37
Load Address (LA) 3-38
Logical Instructions 3-39
Compare Logical Immediate (CLI) 3-39
Compare Logical Characters (CLC) 3-40
Test Bits On Masked (TBN) 3-42
Test Bits Off Masked (TBF) 3-42
Branch on Condition (BC) 3-44
Command Instructions 3-46
Jump on Condition (JC) 3-46
Load Program Mode Register (LPMR) 3-47
Supervisor Call (SVC) 3-48
FUNCTIONAL UNITS 3-50
Main Storage 3-51
Main Storage Address Register 3-51
Operation Register 3-51
Q-Backup Register 3-51

Q-Register 3-51
X-Registers 3-51
Y-Register 3-51
Arithmetic and Logic Unit 3-51
Arithmetic and Logic Unit Parity Predict 3-51
Incrementer or Decrementer 3-51
Decimal Correct 3-52
Local Storage Register 3-52
Program Status Register 3-53
Status Byte Registers 3-54
Status Byte 0 (Sense Only) 3-54
Status Byte 1 (Load Only) 3-54
Status Byte 2 3-54
Status Byte 3 3-54
Backup Mode Register 3-54
Configuration Control Register 3-54
Address Compare Register 3-54
Address Translation 3-55
Address Translation Registers 3-55
Program Mode Register 3-55
Control Mode Register 3-55
ERROR CONDITIONS 3-56
Main Storage Processor Checks 3-56

INTERRUPTS AND CYCLE STEAL REQUESTS . 4-1
INTERRUPTS 4-1
Local Storage Register Stack 4-2
Interrupt Levels 4-3
Interrupt Level 0 4-3
Interrupt Level 1–Disk and Diskette 4-3
Interrupt Level 2–Communications and Fixed Interval Timer 4-3
Interrupt Level 3 4-3
Interrupt Level 4 4-3
Interrupt Level 5 4-3
Main Program Level Interrupt 4-3
Interrupt/Cycle Steal Priority Encode and LSR Selection 4-4
MSP Set Interrupt Level 5 4-5
CONTROL PROCESSOR AND MAIN STORAGE PROCESSOR COMMUNICATION 4-6
CONTROL PROCESSOR AND CHANNEL COMMUNICATION 4-7

CHANNEL 5-1
INTRODUCTION 5-1
DATA FLOW 5-1
I/O Instructions 5-2
Processing Unit Storage Link to I/O Attachments 5-2
Control Processor Local Storage Register Link to I/O Attachments 5-2
Control Processor Jump on I/O Condition Link to I/O Attachments 5-5
PORT CARD 5-6
Port Parity 5-6
Port Clock 5-8
Generation of Port Clock Times 5-8
Generation of Port Triggers 5-8
Data Buffer 5-12
Port Register 5-13
Port Checks Register 5-14
Port Decodes 5-14
Interrupt/Cycle Steal Priority Control for LSRs 5-14
Command Bus Out Decode 5-15
CONTROL PROCESSOR/PORT CONTROLS . . 5-16
Port to Control Processor Lines 5-16
System Bus In–Nine Lines 5-16
Storage Cycle Request–One Line 5-16
Advance Time–One Line 5-16
Block Processor Clock (BPC Tgr)–One Line . . 5-16
Interrupt/Cycle Steal LSR Decode–Three Lines 5-16
CBI Bit 4 Gated–One Line 5-16
New Channel Check–One Line 5-16
Proc Interrupt 1, 2, 4–Three Lines 5-16
I/O Service Request–One Line 5-16
Interrupt Request to Run Latch–One Line . . 5-16
Control Processor to Port Lines 5-16
T4 Through T6–One Line 5-16
System Bus Out–Nine Lines 5-16
I/O Instruction–One Line 5-16
Phase A–One Line 5-16
Machine Check Interrupt–One Line 5-16
CSY Trigger–One Line 5-16
System Reset–One Line 5-16
T7–One Line 5-16
Lamp Test–One Line 5-16
PORT/ATTACHMENT CONTROLS 5-17
Port to Attachment Lines 5-17
MPXPO Bus Out–Nine Lines 5-17
Control Out Pwrd–One Line 5-17
Service Out Pwrd–One Line 5-17
Command Bus Out 0, 1, 2–Three Lines . . . 5-17
Strobe Pwrd–One Line 5-17
Transfer Error–One Line 5-17
Disk Burst Mode Gated–One Line 5-17
Disk Strobe–One Line 5-17
CSY Trigger–One Line 5-17
Attachment to Port Lines 5-18
MPXPO Data In–Nine Lines 5-18
Service In–One Line 5-18
Microinterrupt Request–Five Lines 5-18
Multidevice Response–One Line 5-18
Base Cycle Steal Request–One Line (Per Device) 5-18
Disk/Dskt Block Processor Clock–One Line . 5-18
Disk/Dskt (Load) BC Req–One Line 5-18
Command Bus In (Bits 0, 1, 2, 3, 4, 5)–Six Lines 5-18
Direct Lines–Control Processor/Attachments . . 5-18
Power On Reset–One Line 5-18
System Reset–One Line 5-18
Control Storage Initial Program Load (CSIPL) Latch–One Line 5-18
CSIPL Cycle–One Line 5-18
Interface Clock Times–Eight Lines 5-18
OPERATIONS 5-19
Burst Cycle Steal Mode 5-19
Disk Support Timing 5-19
Disk Support Lines 5-19
Burst Cycle Steal Mode (Operational Sequence) 5-20
Base Cycle Steal Mode 5-22
Base Cycle Steal Mode (Operational Sequence) 5-22
Microinterrupt Level Mode 5-24
Channel Exerciser Loop Program 5-24
COMMANDS 5-25
I/O Immediate 5-26
I/O Load or I/O Control Load (IOL, IOCL) . . 5-26
I/O Load Instruction 5-27
I/O Load (Big Picture) 5-28
I/O Load (Detail) 5-30
I/O Sense or I/O Control Sense (IOS, IOCS) . 5-32
I/O Sense Instruction 5-33
I/O Sense (Big Picture) 5-34
I/O Sense (Detail) 5-36
Sense Interrupt Level Status Byte (SILSB) . . 5-38
Sense Interrupt Level Status Byte (Big Picture) 5-38
Sense Interrupt Level Status Byte (Detail) . . 5-40
Control Processor Load Function (MPLF) . . . 5-42
Control Processor Sense (MPS) 5-42
I/O Storage (WTCL, WTCH, RDCL, RDCH, WTM, RDM) 5-43
I/O Storage (Load–Big Picture) 5-44
I/O Storage (Load–Detail) 5-46
I/O Storage (Sense–Big Picture) 5-48
I/O Storage (Sense–Detail) 5-50
Jump on I/O Condition (JIO) 5-52
Jump on I/O Condition (Big Picture) 5-52
Jump on I/O Condition (Detail) 5-54
ERROR CONDITIONS 5-56
Blast Conditions 5-56
Blast Condition Because of Time-out Check . 5-56
Blast Condition Because Data Bus In Is Not Zero 5-57
Blast Condition Because of Assigning the Wrong Device 5-58
Port Checks 5-59
Check Generation 5-59
Transfer Error 5-60
Time-out Conditions 5-61
Processor Check Halt 5-62

CONTROL PANELS 6-1
OPERATOR PANEL 6-1
Power Switch 6-1
Power Light 6-1
Load Switch/Light 6-1
System In Use Light 6-1
Power Check Light 6-1
Thermal Check Light 6-1
Processor Check Light 6-1
Console Check Light 6-1
Immediate Power Off Switch 6-1
CE PANEL 6-2
Start Switch 6-2
MSP Running Light 6-2
Stop Switch 6-2
Stop Light 6-2
Mode Selector Switch 6-2
CSIPL and MSIPL Switches 6-16
Proc Interrupt (Processor Interrupt) Lights . . 6-16
Reset Switch 6-16
Address/Data and Display/Data Switches . . 6-16
Clock Light 6-16
Force Clock Switch 6-16
Check Switch 6-16
CE Start Switch 6-16
Lamp Test Switch 6-16
Stor Sel (Storage Select) Switch 6-16
Add Comp (Address Compare) Switch 6-17
Comm Dply (Communications Display) Switch 6-17
Dply Pwr Chk (Display Power Check) Switch 6-17
Pwr Fault Dply (Power Fault Display) Switches 6-17

62EH DISK DRIVE AND ATTACHMENT 7-1
INTRODUCTION 7-1
62EH Disk Drive 7-1
Subframe 7-2
Grounding 7-2
Disk Enclosure 7-2
Disk Spindle 7-3
Transducer 7-3
Actuator Lock 7-3
Actuator 7-4
Actuator Position Indicator 7-4
Circuit Locations 7-4
Motor and Brake 7-4
Write Safety 7-5
Data Unsafe Conditions 7-5
File Ready 7-5
Disk Speed 7-5
Power On 7-5
Disk Format 7-5
Data Tracks 7-5
Sector Format 7-6
Disk Addressing 7-7
Servo Tracks 7-8
Landing Zone 7-8
Guard Band 7-8
Data Recording 7-8
Actuator Movement 7-9
Seek 7-9
Recalibrate 7-9
Servo Track Follow 7-10
Head Alignment and Disk Description 7-11
Missing Clock Pulse and Position Pulses . . . 7-11
Guard Band 7-11
Behind Home 7-11
DATA FLOW 7-12
OPERATIONS 7-13
Write Identification 7-14
Read Identification 7-15
Write Data 7-16
Read Data 7-18
Read Diagnostic 7-18
Read Verify 7-18
Scan Read Data Equal 7-20
Scan Read Data Low or Equal 7-20
Scan Read Data High or Equal 7-20
Write Circuits 7-22
Write 7-22
Write Waveshapes 7-23
Read Circuits 7-26
Read 7-26
Read Waveshapes 7-27
Track Follow Principles 7-30
Track Follow 7-30
Track Follow Waveshapes 7-31
Servo Clock 7-32
Servo Clock Waveshapes 7-33
Phase Lock Oscillator 7-34
Phase Lock Oscillator Synchronization 7-34
Recalibrate Operation 7-35
Disk Ready 7-37
Seek Operation 7-38
Seek 7-38
Actuator Feedback During Seek 7-39
Seek Waveshapes 7-41
Power On and Off 7-42
Power On and Seek Home 7-43
Cycle Steal 7-44
Cycle Steal from the Control Processor . . . 7-44
Cycle Steal to the Control Processor 7-45
Control Storage Initial Program Load 7-46
Command Bus In 7-47
COMMANDS 7-48
I/O Load Command–I/O Control Load Command 7-48
I/O Sense Command–I/O Control Sense Command 7-50
Sense Interrupt Level Status Byte Command . . 7-52
Jump on I/O Command 7-54
ERROR CONDITIONS 7-56
Write Data Echo Check 7-56
DBO Parity Check 7-57
Cycle Steal Overrun Check 7-58
Overrun Circuit Description 7-58
SERDES Check 7-60
Cyclic Redundancy Check 7-61
Sector Check 7-62
Sector Check Circuit Description 7-62
Not Valid Seek Address 7-63
Write Check 7-64
Channel Transfer Check 7-65
Sector Sync Check 7-66
Off Track Check 7-67
PLO Out of Sync 7-68
Interrupt Time-out Check 7-69
Data Unsafe 7-70
JUMP ON I/O CONDITIONS 7-71
Sector Hit 7-72
Scan Hit 7-73
INPUT/OUTPUT AND SENSE LINES 7-75
Output Bus Lines 7-75
Input Bus Lines 7-75
Sense Lines Used with MAPs 7-76
33FD/53FD DISKETTE DRIVE AND ATTACHMENT (Level 1) 8-1
INTRODUCTION 8-1
Diskette Addressing 8-1
33FD Diskette Drive 8-2
33FD Diskette Drive Assembly 8-2
33FD Operating Sequences 8-3
Frequency Modulation Read and Write Circuits . 8-4
Diskette 1 Format 8-5
53FD Diskette Drive 8-6
53FD Diskette Drive Assembly 8-6
53FD Operating Sequences 8-7
Modified Frequency Modulation Read and Write Circuits 8-8
Diskette 2D Format 8-9
DATA FLOW 8-11
OPERATIONS 8-12
Seek Operations 8-12
Seek Data Flow 8-13
Read Operation 8-14
Read Data Flow 8-17
Write Operation 8-18
Write Data Flow 8-19
Find Sector Identification Operation 8-20
Find Sector Identification Data Flow 8-23
Write Sector Identification Operation 8-24
Write Sector Identification Data Flow 8-25
COMMANDS 8-26
I/O Load Command 8-26
I/O Sense Command 8-28
I/O Control Load Command 8-30
Write Byte or Write Address Mark Byte Command 8-32
Write Data Trigger 8-34
Write Cyclic Redundancy Character Byte Command 8-35
Seek to Next Track Command 8-37
Search for Address Mark Byte Command 8-38
I/O Control Sense Command 8-40
Sense Interrupt Level Status Byte Command . . 8-43
Jump on I/O Command 8-44
FUNCTIONAL UNITS 8-46
Data Separator 8-46
Index Counter 8-46
Ready Counter 8-47
Control Storage Initial Program Load Track Counter 8-47
Write Clock and Write Bit Ring 8-47
Read Clock and Read Bit Ring 8-47
Cyclic Redundancy Character Shift Register . . . 8-48
Interrupt 1 and Interrupt 4 Requests 8-49
ERROR CONDITIONS 8-50
Fast Check 8-52
Not Ready 8-52
Missing Erase Current and Unexpected or Erase Current Present 8-53
ID Not Found (Missing Record) 8-53
Read Overrun Check 8-54
Write Overrun Check 5-54
Write Parity Check 8-54

5211 PRINTER ATTACHMENT 9-1
INTRODUCTION 9-1
Circuit Locations 9-1
Printer Interface 9-1
DATA FLOW 9-2
FUNCTIONAL UNITS 9-3
OPERATIONS 9-13
Printer Commands 9-13
Example of Print Operations 9-14
Printing Operations 9-15
Spacing Operations 9-15
COMMANDS 9-16
I/O Load Command 9-16
I/O Control Load Command 9-18
I/O Sense Command–I/O Control Sense Command 9-20
Sense Interrupt Level Status Byte Command . . 9-22
Jump on I/O Command 9-24
ERROR CONDITIONS 9-26
INPUT/OUTPUT LINES 9-28
Hammer Interface Lines 9-28
Control Interface Lines 9-30
Operator Panel Interface Lines 9-31

ATTACHMENT CONTROLLERS 10-1
INTRODUCTION 10-1
DATA FLOW AND FUNCTIONAL UNITS 10-2
Data Flow 10-2
Functional Units 10-3
CONTROLLER LINES 10-4
Lines to the Controller 10-4
Lines from the Controller 10-4
Data Bus Lines 10-4
Storage Select Lines 10-4
Storage Data Lines 10-5

WORK STATION ATTACHMENT 11-1
INTRODUCTION 11-1
DATA FLOW 11-2
FUNCTIONAL UNITS 11-3
Channel Interface 11-3
Controller Interface 11-4
Serial Interface 11-5
SERIAL INTERFACE TO WORK STATIONS . . . 11-6
Data Transmissions 11-6
Phase Encoded Data 11-6
Predistorted and Distorted Data 11-7
Differential Data 11-7
Bit Synchronization 11-8
Frame Synchronization 11-8
Line Turnaround 11-8
Typical Transmission Sequences 11-8
Examples of Transmission Sequences 11-9
Commands 11-11
Frame Formats 11-11
OPERATIONS 11-12
Displaying a Message 11-13
Transmit and Receive Operations 11-14
Transmit Operation 11-14
Receive Operation 11-15
COMMANDS 11-16
I/O Load Command 11-16
I/O Control Load Command 11-18
I/O Sense Command 11-20
Jump on I/O Command 11-22
Sense Interrupt Level Status Byte Command . . 11-23
ERROR CONDITIONS 11-24
Controller Storage Parity Check 11-25
Controller DBO/DBI Parity Check 11-27
Long Time-out Check 11-27
Serial Parity Check 11-28
Work Station Controller Check (Any Check) . 11-28
Channel DBO Parity Check 11-28
BASE CYCLE STEAL 11-29
INPUT/OUTPUT LINES 11-30

DATA COMMUNICATIONS 12-1
INTRODUCTION 12-1
Data Communications Systems 12-1
Data Communications Networks 12-1
Point-to-Point Network 12-1
Multipoint Network 12-1
Binary Synchronous Communications 12-2
BSC Message Format 12-2
Transmit and Receive Storage Contents of Message 12-4
EBCDIC, ASCII, and Line Control Characters . 12-5
Synchronous Data Link Control 12-6
Frame Format 12-6
Control Field Formats 12-7
Primary Station Commands and Secondary Station Responses 12-8
Examples of SDLC Commands and Responses . 12-9
Systems Network Architecture 12-10
SNA/SDLC Data Relationship 12-10
Types of Network Addressable Units 12-10
Physical Configuration 12-10
SNA/SDLC Buffer 12-12
Modems and Interfaces 12-19
COMMUNICATIONS ADAPTER 12-20
Data Flow 12-20
Functional Units 12-21
Adapter Controls 12-24
System Level Interface 12-28
Queue 12-28
Input/Output Blocks 12-28
Operations 12-28
BSC Receive Only 12-28
BSC Receive Initial Delayed (Multipoint) . . . 12-31
BSC Receive Initial (Point-to-Point) 12-31
BSC Receive Initial (Multipoint) 12-31
BSC Transmit/Receive Overlay 12-31
BSC Transmit/Receive Initial (Multipoint) . . 12-32
BSC Transmit/Receive 12-33
BSC Transparent Operations 12-36
BSC Multipoint Operations 12-37
SDLC Transmit Operations 12-38
SDLC Receive Operations 12-39
Commands 12-42
I/O Load Command–I/O Control Load Command 12-42
Load/Sense Buffer 12-44
Load Time-out Clock and Registers 12-45
Load Timing Chart 12-47
I/O Sense Command 12-48
Sense Data, Registers, and Interrupt Conditions 12-50
Sense Data Timing Chart 12-51
Sense Microinterrupt Level Timing Chart . . . 12-53
Error Conditions 12-54
Adapter Check 12-54
Data Set (Not) Ready 12-55
Abortive Disconnect 12-55
Receive Time-out 12-55
Invalid ASCII Character 12-55
Invalid Frame 12-55
Secondary SDLC Time-out (Inactivity Timer) 12-55
Primary SDLC Time-out (Idle Detect) and Nonproductive Timer) 12-55
Block/Frame Check Error 12-55
DBO Parity 12-55
Diagnostics 12-56
Diagnostic Mode and Wrap Test 12-56
Internal Clock Feature 12-60
EIA/CCITT Line Adapter 12-61
MODEMS 12-62
IBM 1200 BPS Integrated Modem 12-62
Nonswitched Network Interface 12-62
Switched Network Interface 12-64
1200 BPS Transmit Operations 12-66
Receive Operations 12-66
Automatic Answering 12-66
1200 BPS Integrated Modem Tests 12-67
Line Plate for Public Switched Network . . . 12-68
IBM 2400 BPS Integrated Modem 12-68
Operation 12-68
2400 BPS Transmit Data Flow 12-72
2400 BPS Receive Data Flow 12-74
Unclamp Demodulation Circuits 12-74
Switched Network and Automatic Answering Operation 12-76
2400 BPS Integrated Modem with Switched Network and Automatic Answering 12-77
Switched Network Backup (SNBU), Wrap, and Line Connections 12-78
Switching and Jumpers for 2W/4W, SNBU, Wrap, and Line Connections 12-79
DIGITAL DATA SERVICE ADAPTER 12-80
Transmission Rates 12-80
Transmission Signal 12-80
Line Control Characters 12-80
Idle 12-80
Zero Suppression 12-81
Out of Service 12-81
Line Control Character Flow 12-82
Interface Lines 12-83

62PC DISK DRIVE AND ATTACHMENT 13-1
INTRODUCTION 13-1
62PC Disk Drive 13-1
Grounding 13-1
Subframe 13-1
Disk Enclosure and Spindle Brake 13-1
Actuator Lock 13-1
Drive Motor Assembly 13-1
Attachment 13-1
Circuit Locations 13-2
DISK FORMAT 13-3
Cylinders 13-3
Tracks 13-3
Servo Track 13-3
Data Track 13-3
Guard Band 13-3
Landing Zone 13-3
Sectors 13-4
Data Recording 13-6
Reading and Writing Data 13-6
DATA PROTECTION 13-7
Data Unsafe Conditions 13-7
Not Ready 13-7
Power On and Power Off 13-7
DATA FLOW 13-8
System I/O Channel Interface 13-10
Common Adapter Interface 13-10
State Counter 13-10
Controller 13-10
Buffer Storage 13-10
Oscillator and Clocks 13-10
Disk Drive Interface 13-11
Write Data Flow 13-11
Read Data Flow 13-11
OPERATIONS 13-12
Operation Sequence 13-12
Read ID 13-14
Read Data 13-15
Read Diagnostic 13-15
Read Verify 13-15
Write ID 13-16
Write Data 13-17
Scan Equal, Scan High or Equal, Scan Low or Equal 13-18
Diagnostic Operations 13-19
Load Seek Required Address Direct 13-19
Load Seek Control Direct 13-19
Sense File Direct 13-19
Sense File Diagnostic Sense Bytes 1, 2, and 3 13-19
Sense File Diagnostic Sense Bytes 1, 2, and 3 256 Sample Test 13-19
Sense File Diagnostic Wrap 13-19
Disk Speed Timing Diagnostic 13-19
Timed Seek Diagnostic 13-19
Read Data with Data Repeat 13-19
Read Common Adapter Buffer Storage . . . 13-19
Common Adapter File Control Block 13-20
Loading and Sensing the Common Adapter File Control Block 13-24
Loading the Common Adapter File Control Block 13-24
Sensing the Common Adapter File Control Block 13-24
Interrupts 13-28
Burst Mode Cycle Steal 13-30
Servo Tracks and Servo Track Follow 13-34
Access Locating 13-34
Dedicated Servo 13-34
Track Follow Waveshapes 13-38
Sample Servo 13-39
Sample Servo Waveshapes 13-40
Access Operations 13-42
Starting the Operation 13-42
Performing the Operation 13-44
Seek Calibration Sequence 13-44
Seek Waveshapes 13-46

Reading and Writing Data 13-47
Head Selection 13-47
Writing Data 13-48
Reading Data 13-49
Write Waveshapes 13-50
Read Waveshapes 13-52
Power On and Power Off Operations 13-54
Power Sequence 13-54
Emergency Power Off 13-55
Control Storage Initial Program Load 13-56
Common Adapter Initial Program Load Operation 13-56
Command Bus In 13-58
COMMANDS 13-60
I/O Load Command–I/O Control Load Command 13-60
I/O Sense Command–I/O Control Sense Command 13-62
Sense Interrupt Level Status Byte Command 13-63
Jump on I/O Condition Command 13-64
Common Adapter Commands 13-65
Common Adapter Command Descriptions . . 13-69
ERROR CONDITIONS 13-70
Channel Adapter Sensed Errors 13-71
Disk Drive Sensed Errors 13-72
Common Adapter Sensed Errors 13-73
INPUT/OUTPUT LINES 13-78
Lines Between the Channel and the Channel Adapter 13-79
Lines Between the Channel Adapter and the Common Adapter 13-80
CA Data Bus (18 Lines, Bidirectional) 13-80
Tag Bus (9 Lines) 13-80
Lines Between the Common Adapter and the 62PC Disk Drive 13-80
Dedicated Cable 13-80
Bus Cable 13-81

33FD/53FD/72MD DISKETTE DRIVE AND ATTACHMENT (LEVEL 2) 14-1
INTRODUCTION 14-1
33FD Diskette Drive 14-2
33FD Diskette Drive Assembly 14-2
33FD Operating Sequence 14-3
53FD Diskette Drive 14-4
53FD Diskette Drive Assembly 14-4
53FD Operating Sequence 14-5
72MD Diskette Magazine Drive 14-6
Autoloader Units 14-6
Diskette Drive Components 14-7
Logic Cards 14-7
Stepper Motors 14-8
72MD Operating Sequences 14-10
Frequency Modulation Read and Write Circuits 14-12
Modified Frequency Modulation Read and Write Circuits 14-13
Diskette 1 Format 14-14
Diskette 2D Format 14-15
DATA FLOW 14-16
OPERATIONS 14-17
Diskette Drive Operations 14-17
Seek Operation 14-17
Read Operation 14-19
Write Operation 14-21
Write Verify Operation 14-22
Find Sector Identification Operation 14-23
Write Sector Identification Operation 14-24
CSIPL Read Operation 14-26
Autoloader Operations 14-27
Select Slot 14-27
Orient 14-27
Eject 14-27
Abort 14-27
COMMANDS 14-28
I/O Load Command–I/O Control Load Command 14-28
Autoloader Mode Commands 14-30
Select Diskette 14-31
Orient 14-31
Eject 14-31
Load Heads 14-31
Unload Heads 14-31
Reset Sense 14-31
Abort 14-31
Sense 0 through Sense 5 14-31
I/O Sense Command–I/O Control Sense Command 14-32
Jump on I/O Condition Command 14-34
Sense Interrupt Level Status Byte Command 14-36
FUNCTIONAL UNITS 14-37
Data Separator 14-37
Index Counter 14-37
Ready Counter 14-38
Control Storage Initial Program Load Track Counter 14-38
CSIPL Autoloader Sequence 14-38
Read/Write Clock 14-39
Write Trigger 14-40
Address Mark Detection 14-42
Bit Ring 14-42
Cyclic Redundancy Character Shift Register . . . 14-43
ID Buffer 14-44
Data Buffer 14-45
Sector Sequence Control 14-45
Track Sequence Control 14-45
Byte Counter 14-46
Cycle Steal Control 14-46
Interrupt Level 4 Request 14-47
DBI Assembler 14-47
CBI Assembler 14-47
Op Decode 14-47
Autoloader Control 14-47
Seek Control 14-47
500-Kilohertz Oscillator 14-47
Error Conditions 14-48
Diskette Drive Errors 14-49
Autoloader Errors 14-54
INPUT/OUTPUT LINES 14-56

3262 PRINTER ATTACHMENT 15-1
INTRODUCTION 15-1
Circuit Locations 15-1
Printer Interface 15-1
Circuit Description 15-2
Attachment States 15-4
DATA FLOW-T2 CARD 15-10
DATA FLOW-U2 CARD 15-11
FUNCTIONAL UNITS 15-12
OPERATIONS 15-37
Printer Commands 15-37
Example of Print Operations 15-38
Printing Operations 15-39
Spacing Operations 15-39
COMMANDS 15-40
I/O Load Command 15-40
I/O Control Load Command 15-42
I/O Sense Command-I/O Control Sense Command 15-44
Sense Interrupt Level Status Byte Command . . 15-46
Jump on I/O Command 15-48
ERROR CONDITIONS 15-50
INPUT/OUTPUT LINES 15-52
Hammer Interface Lines 15-52
Control Interface Lines 15-54
Operator Panel Interface Lines 15-55

APPENDIX A. DISKETTE FORMATS A-1

GLOSSARY 1

INDEX X-1

This page intentionally left blank.

List of Abbreviations and Acronyms

μA	microampere
μs	microsecond
A	add to register; AND gate
AA	automatic answering
AC	alternating current
ACE	action control element
ACK	acknowledge character
ACK0	even acknowledgment
ACK1	odd acknowledgment
ACR	adapter control register; address compare register
ACTB	alternating current terminal block
ACTLU	activate logical unit
ACTPU	activate physical unit
ACW	action control word
ACYR	add registers with carry
add/addr/adr	address
AEQ/AEL	automatic equalizer
AGC	automatic gain control
AI	add immediate
ALC	add logical characters
ALU	arithmetic and logic unit
AM	address mark
amp	ampere
ANS	auto network shutdown
ANSC	auto network shutdown complete
AOI	and or invert
AR	add registers; amplifier symbol
AR-DIFF	differentiator to amplifier
ARR	address recall register
ASCII	American National Standard Code for Information Interchange
asm	assembly
ASR	adapter status register
assn	assigned
ATR	address translation register
aux	auxiliary
AZ	add zoned decimal
B	branch
BAL	branch and link
BC	branch on condition; byte counter
BCC	block check character
BCD	binary-coded decimal
bfr/buf	buffer
BH	behind home
BIND	bind session
BIU	basic information unit
blk	block
BLU	basic link unit
BMR	backup mode register
BPC	block processor clock
bps	bits per second
BR	bit ring
BSC	binary synchronous communications
BTU	basic transmission unit
C	Celsius; clock pulse
CA	common adapter
CADUCEE	data communications network in France
CANCEL	cancel
CB	circuit breaker
CBI	command bus in
CBO	command bus out
CBS	data coupler for modem with automatic answering
CCB	channel command bus
CCBO	controller command bus out
CCITT	International Consultative Committee on Telegraph and Telephone
CCR	configuration control register
CCT	coupler cut through
CD	carrier detect
CDBI	controller data bus in
CDBO	controller data bus out
CDSTL	connect data set to line
CDT	data access arrangement for manual calling
CE	customer engineer
chan	channel
CHK	check
CI	compare immediate
CKB	check byte
CLC	compare logical characters
CLEAR	clear
CLI	compare logical immediate
clk	clock
cm	centimeter
cmd	command
CMDR	command reject
CMR	control mode register
cnt	count
cntr	counter
COD	change of direction
COMM	communications
COMP	compare
COMTB	communications terminal block
CONS	console
COR	control output register
CP	control processor
CPMGR	connection point manager
CPU	processing unit
CR	crystal rectifier
CRC	cyclic redundancy check
CRT	cathode-ray tube
CS	control storage; cycle steal
CSCD	clear to send/carrier detect
CSILSW	control storage interrupt level status word
CSIPL	control storage initial program load
CSP2	clock sync phase 2
CSP3	clock sync phase 3
CSX	clock trigger for MSP
CSY	clock trigger for MSP
CS1 P2	clock sync 1, phase 2
CS1 P3	clock sync 1, phase 3
CS2 P2	clock sync 2, phase 2
CS2 P3	clock sync 2, phase 3
CTL/cntl/ctrl	control
CTS	clear to send
cyc	cycle
DA	data modem ready; device address
DAA	data access arrangement
DAC	digital-to-analog converter
DACTLU	de-activate logical unit
DACTPU	de-activate physical unit
DAF	destination address field
DAR	data address register
dB	decibel
DBI	data bus in
DBO	data bus out
DC	direct current
dcd	decode; decoder
DCF	data count field
DCP	diagnostic control program
DCR	diagnostic control register
DDSA	Digital Data Service Adapter
DE	device end
DEC	decrement register by 1
demod	demodulator
det	detector
diag	diagnostic
DISC	mandatory disconnect
disp	displacement
div	division
dk	disk
DLC	data link control
DLE	data link escape
dly	delay
DM	disconnected mode
DPLY	display
DPSK	differential phase shift keying
DR	data ring; driver
DRAR	driver/receiver activity register
DSF	data storage facility
dskt	diskette
DSR	data set ready
DT	data tip
DTE	data terminal equipment
DTR	data terminal ready
EBCDIC	extended binary-coded decimal interchange code
EC	engineering change
ECC	emitter column counter
ED	edit
EFI	expedited flow indicator
EIA	Electronic Industries Association
EIR	enable interrupt register
ENQ	enquiry
EOF	end of file
EOT	end of transmission
ERAP	error recording analysis procedure
ERP	error recovery procedure
ESC	extended storage control
ETB	end of text block
ETX	end of text
EWG	end write gap
ext	extended
FET	field effect transistor
FF	flip-flop
FID	format identification field
FL	flip latch
FM	frequency modulation
FRU	field replaceable unit
FSK	frequency shift keying
FSL	field service logic
func/funct	function
GB	guard band
gen	generator
GND	ground
GT/gt	gate
H/L	high/low
HBN	hexadecimal branch numeric
HBZ	hexadecimal branch zone
HCP	head connector point
hd	head
hex	hexadecimal
hh:mm:ss	hour:minute:second
Hz	hertz
I-fetch	instruction fetch
I/O	input/output
IAR	instruction address register
ID	identification; identifier
IDB	identification buffer
IFP	internal fire pulse
IL	interrupt level
IMPSS	impression control singleshot
INC	increment register by 1
incr	increment
INITC	initialization complete
INSN/inst	instruction
int	internal
intrpt/irpt	interrupt
IOB	input/output block
IOCH	input/output control handler
IOCL	I/O control load
IOCS	I/O control sense
IOL	I/O load
IOS	input/output supervisor; I/O sense

IPL initial program load
IPO immediate power off
ITB intermediate text block
ITC insert and test characters

JC jump on condition
JCB job control block
JCY jump on carry
JE jump on equal
JFLG jump on flag
JH jump on high
JIO jump on I/O condition
JL jump on low
JM jump on mixed
JN jump on negative
JNE jump on not equal
JNH jump on not high
JNL jump on not low
JNN jump on not negative
JNP jump on not positive
JNZ jump on not zero
JO jump on all ones
JP jump on positive
JSR jump on service request
JZ jump on zero

K 1,024
Kana Katakana
kbd keyboard
kHz kilohertz

L load direct to control storage; load register
LA load address
LA1 logical/arithmetic 1
LA2 logical/arithmetic 2
LC load from control storage; link control
LCRR length count recall register
LED light-emitting diode
LI load immediate
LIO load input/output
LL leased line
LM load from main storage
LPDL least positive down level
lpi lines per inch
LPMR load program mode register
LPUL least positive up level
LRC longitudinal redundancy check
LSAR load/sense address register
LSID local session identifier
LSR local storage register
lth latch
LU logical unit
LUSTAT logical unit status
LZ landing zone

M (mega) million
mA milliampere
MAB microaddress backup register
MAP maintenance analysis procedure
MAR microaddress register
MB megabyte
MC machine check; missing clock pulse; motor connector
MCI machine check interruption
MCR magnetic character reader
MDI MAP diagnostic integration
MFM modified frequency modulation
MHz megahertz
MIC message identification code
MICR magnetic ink character recognition
mm millimeter
mod modifier
modem modulator/demodulator
MOR micro-operation register
MPDL most positive down level
MPF mapping field
MPL control processor load; main program level
MPLF control processor load function
MPLS control processor load special
MPS control processor sense
MPUL most positive up level
MPXPO multiplexer port out
MS main storage
ms millisecond
MSAR main storage address register
MSIPL main storage initial program load
MSP main storage processor
MSR modem status register
MST monolithic storage technology
mV millivolt
MVC move characters
MVI move logical immediate
MVR move local storage register
MVX move hexadecimal character
MZN move zone to numeric
MZZ move zone to zone

N inverter symbol
N/C normally closed
N/O normally open
NAK negative acknowledge character
NAU network addressable unit
NCR AND complement
NDM normal disconnect mode
NR AND register
NRM normal response mode
NRZI zeros complemented transition coding
ns nanosecond
NSA nonsequenced acknowledgment
NTF no trouble found

O/C over current
OAF origin address field
OCD off-chip driver
OCR OR complement
OE exclusive or
OH off hook
op operand; operation
osc oscillator

P parity; position pulse
P/F poll/final
PAD fill character
PC parity check; path control
PCB printed circuit board
PCR processor condition register
PDTB power distribution terminal board
PFN print fire number
PG parity generate; parity generator
PH polarity hold
PIU path information unit
PLA programmable logic array
PLB power logic board
PLO phase lock oscillator
PMR program mode register
POR power on reset
pos position
PP parity predict; print position; program product
prc processor
preamp preamplifier
PREPS prepare to switch
PREV previous
PROC processor
prtr printer
PSN public switched network
PSR program status register
PSS print subscans
PTT Post, Telephone, and Telegraph
PTX phototransistor
PU physical unit
PWR power
pwrd powered

R/C resistor/capacitor
R/W read/write
RB request block
rcv receive
rd read
RDCH read from control storage high
RDCL read from control storage low
RDM read from main storage
recal recalibrate
reg register
req request
REQMS request maintenance statistics error log
REQTEST request test
resp response
RETRN return
RH request/response header
RI ring indicate
RIB request indicator byte
RMPR sense main storage processor register
RNR receive not ready
ROS read-only storage
rpm revolutions per minute
RQR request recovery
RR receive ready
RSHUTD request shutdown
RST reset
RTS request to send
RU request/response unit
RVI reverse interrupt

s second
S/D serializer/deserializer
SAR storage address register
SBAR storage buffer address register
SBF set bits off; set bits off masked
SBI system bus in
SBN set bits on; set bits on masked
SBO system bus out
SC sequence counter
SCS standard character string
SCYR subtract with borrow
SDLC synchronous data link control
SDR storage data register
SDT start data traffic
sel select; selector
SERDES serializer/deserializer
SG signal ground
SH switch hook
SI subtract immediate
SIGNAL signal
SILSB sense interrupt level status byte
SILSW system interrupt level status word
SIO start input/output
SLC subtract logical characters
SLL shift left logical
SLLD shift left logical double
SLT solid logic technology
SNA systems network architecture
SNBU switched network backup (standby)
SNF sequence number field
SNRM set normal response mode

SNS	sense input/output
SOH	start of header
SR	subtract register
SRL	shift right logical
SRLD	shift right logical double
SS	sequential sector; singleshot
SSCP	system services control point
SSP	System Support Program Product
ST	store register
STC	store to control storage
STG/STOR	storage
STM	store to main storage
STSN	set and test sequence numbers
STX	start of text
SVC	supervisor call
SW	switch
SWG	switch write gap
SWICOM	switch complete
SYN	synchronous idle
sync	synchronize; synchronization
SYS	system
SZ	subtract zoned decimal
TB	terminal block
TBF	test bits off masked
TBN	test bits on masked
TCB	task control block
TD	time delay
TH	thermal; transmission header
THP	test header point
TM	test mask
TP	test point
TPA	test point A
TPB	test point B
TP1	test point 1
TP2	test point 2
TQE	timer queue element
TR/tgr	trigger
trans	transfer
TTD	temporary text delay
TU	test unit
TUB	terminal unit block
T1,T2,T3,T4	test 1, 2, 3, 4
UDT	unit definition table
UNBIND	unbind session
V	volts
Vac	volts, AC
Vdc	volts, DC
vert	vertical
VFL	velocity follow latch
VFO	variable frequency oscillator
VRC	vertical redundancy check
VTL	vendor transistor logic
WACK	wait before transmit (positive acknowledgment)
WC	write clock
WMPR	load main storage processor register
WR	work register
wr/wrt	write
WSDM	work station data management
WSIOCH	work station input/output control handler
WT	World Trade
WTCH	write to control storage high
WTCL	write to control storage low
WTM	write to main storage
XDLE	transparent data link escape
XENQ	transparent block cancel
XETB	transparent end-of-text block
XETX	transparent end of text
xfer	transfer
XID	exchange station ID
XITB	transparent intermediate text block
xmt	transmit
XR	exclusive OR
XSTX	transparent start of text
XSYN	transparent synchronous idle
XTTD	transparent temporary text delay
yymmdd	year-month-day
ZAR	zero and add to register
ZAZ	zero and add zoned
2w	two-wire connection
4w	four-wire connection

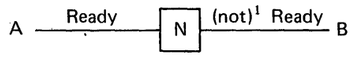
This page intentionally left blank.

Legend

This section describes the symbols and conventions used in System/34 maintenance documentation.

Symbols and Conventions Used in Positive-Logic Diagrams and in Field Service Logics (FSLs)

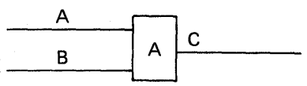
Inverter (N)



A must be active for B to be not active.

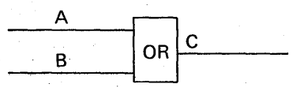
[1] Parentheses are used to enclose words that are not part of an actual line name; they are put there to help you better understand the purpose of a signal.

AND (A)



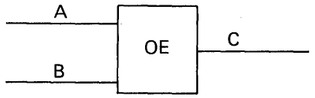
Both A and B must be active for C to be active.

OR



Either A or B must be active for C to be active.

Exclusive OR (OE)

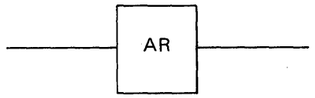


Either A or B, but not both, must be active for C to be active.

If A and B are both active, C is not active.

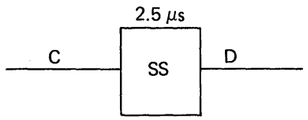
If A and B are both not active, C is not active.

Amplifier (AR)



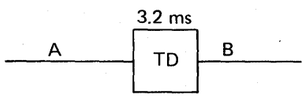
Increases the amplitude of a signal.

Singleshot (SS)



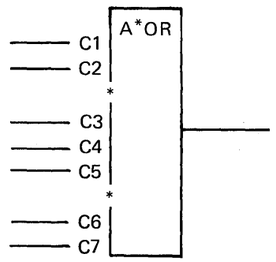
A pulse on C causes a 2.5-microsecond waveshape on D. The time that D is active (2.5 μs) is written above the symbol.

Time Delay (TD or DLY)



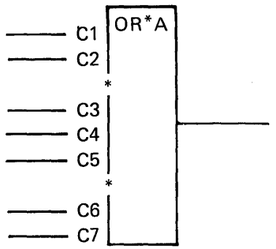
When A changes state, B changes state 3.2 milliseconds later. The length of the delay (3.2 ms) is written above the symbol.

AND-OR



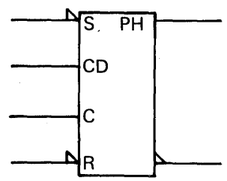
This symbol shows an OR circuit with three AND circuits as inputs. The AND circuits are separated by asterisks (*). An asterisk is a special character that separates groups of inputs in field service logics (FSLs).

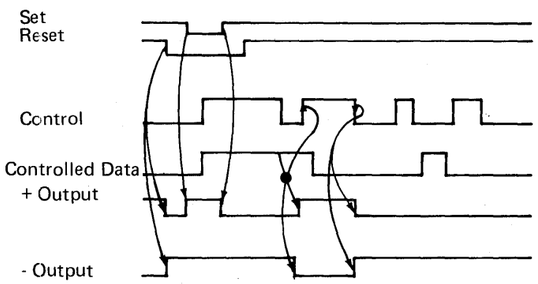
OR-AND



This symbol shows an AND circuit with three OR circuits as inputs. The OR circuits are separated by asterisks (*).

Polarity Hold (PH)

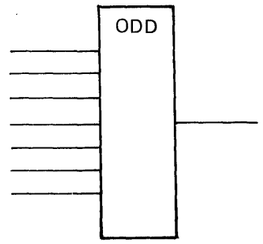




This is a polarity hold circuit with four possible inputs. When the 'control' line (C) becomes active at the same time the 'controlled data' line (CD) is active, both output lines of the PH become active and stay active for the length of the 'control' line (C).

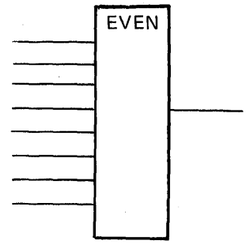
The 'set' line (S), when active, sets the '+ output' line of the PH. The 'reset' line (R), when active, resets both output lines of the PH.

Odd Count (ODD)



The output of the odd-count circuit is active only when an odd number of inputs is active.

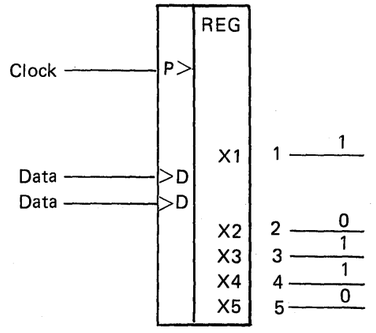
Even Count (EVEN)



The output of the even-count circuit is active only when an even number of inputs is active.

Symbols and Conventions Used in Field Service Logics (FSLs)

Shift Register (REG)



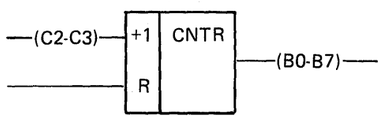
Register Trigger	X1	X2	X3	X4	X5
Initial State	1	0	1	1	0
1st Shift (D = 0)	0	1	0	1	1
2nd Shift (D = 1)	1	0	1	0	1
3rd Shift (D = 1)	1	1	0	1	0

This is an example of a shift down register. In a shift down register, the contents of the high-order position (X1) are shifted into the next lower position (X2), and so on, each time there is a clock pulse.

The greater-than symbol (>) identifies a shift down register; a less-than symbol (<) identifies a shift up register. The letter P on the 'clock' line indicates that shifting occurs on the rise of a positive clock pulse.

If either 'data' line (D) is active at shift time, the high-order position of the shift register is set to 1. If both 'data' lines (D) are not active at shift time, the high-order position of the shift register is set to 0.

Counter (CNTR)

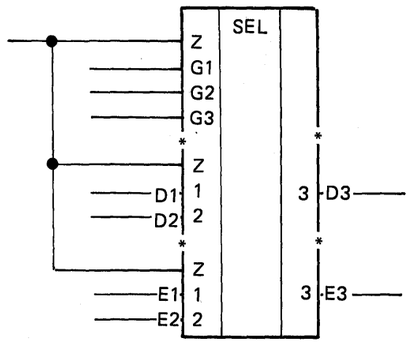


This example of a counter shows two input lines (C2 and C3) and eight output lines (B0 through B7).

The plus symbol (+) indicates that the contents of the counter are increased by 1 each time C2 or C3 becomes active. A minus symbol (-) indicates that the contents of the counter are decreased each time C2 or C3 becomes active.

When R is active, the counter is reset.

Selector (SEL)



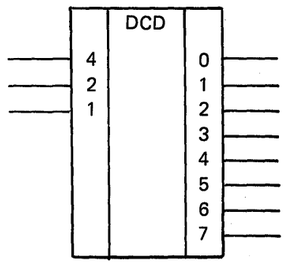
A selector is a gating circuit. The upper part of the selector symbol contains the gates (G1, G2, G3), and the lower part contains the gated data lines (D1, D2, E1, E2).

In this example, gate 1 (G1) controls input data lines D1 and E1; gate 2 (G2) controls lines D2 and E2. Gate 3 (G3) controls output data lines D3 and E3.

Thus, for data to pass through the selector, one of the input gates (G1 or G2) must be active at the same time output gate G3 is active.

This example of a selector also has a Z input. If the Z input is active at the same time gate G3 is active, output lines D3 and E3 are both active.

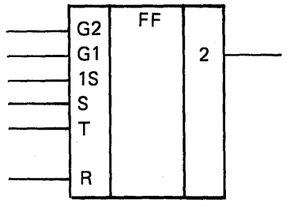
Decoder (DCD)



This example of a decoder converts the output from a 3-position binary counter into 1 of 8 decimal digits. The value of the active output line equals the sum of the active input lines. For example, when input lines 4 and 1 are active, output line 5 is active.

Flip-Flop (FF)

FSL Diagram

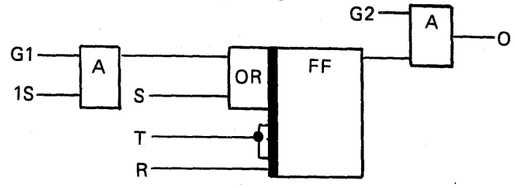


This example shows a flip-flop as it would appear in an FSL diagram, and the way the same trigger would appear in a positive-logic diagram. In this example, there are two sets (S and 1S) and one reset (R).

The trigger is turned on when S is active, or when 1S and gate 1 (G1) are active at the same time. Gate 2 (G2) must also be active for the output (O) to be active.

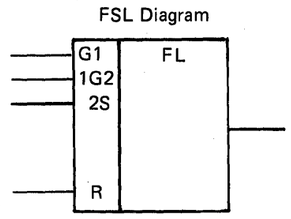
The toggle input (T) reverses the state of the trigger, turning the trigger off if it is on, or turning the trigger on if it is off. When active, the reset input (R) resets the trigger.

Positive-logic Diagram



Flip Latch (FL)

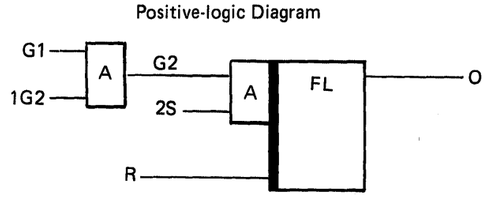
FSL Diagram



This example shows a flip latch as it would appear in an FSL diagram, and the way the same latch would appear in a positive-logic diagram. In this example, gate 1 (G1) must be active when 1G2 is active in order for gate 2 (G2) to be active.

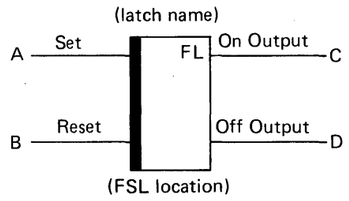
This latch is turned on if G2 is active and the set line (2S) becomes active. When active, the reset input (R) resets the latch. G2 is not shown in the FSL diagram.

Positive-logic Diagram



Symbols and Conventions Used in Positive-Logic Diagrams

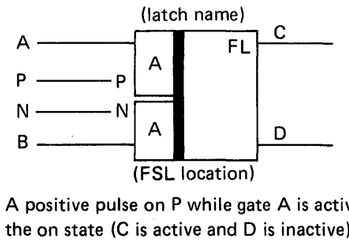
Flip Latch (FL)



If A becomes active, the latch is set to the on state (C is active and D is inactive).

If B becomes active, the latch is set to the off state (D is active and C is inactive).

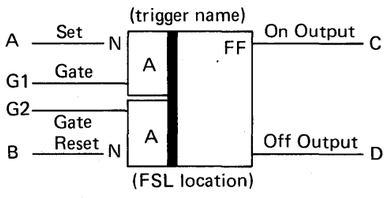
Flip Latch (FL)



A positive pulse on P while gate A is active sets the latch to the on state (C is active and D is inactive).

A negative pulse on N while gate B is active sets the latch to the off state (D is active and C is inactive).

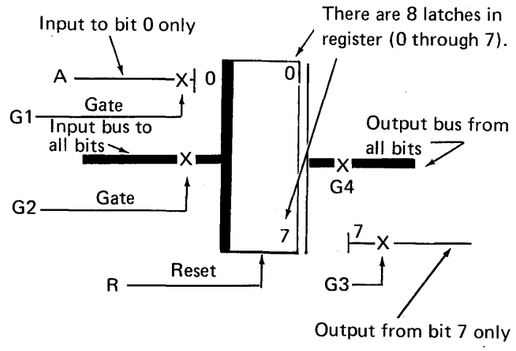
Flip-Flop (FF)



If A is active while gate G1 is active, the latch is set to the on state (C is active and D is inactive).

If B is active while gate G2 is active, the latch is set to the off state (D is active and C is inactive).

Register (Reg)



If gate G1 becomes active while input A is active, latch 0 is set to the on state (latches 1 through 7 do not change state).

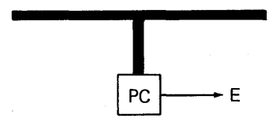
If gate G2 becomes active, latches 0 through 7 are set to the on state for each input bus line that is active.

If gate G3 is active, only the output from latch 7 is gated out.

If gate G4 is active, the output from latches 0 through 7 is gated out.

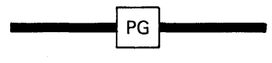
A pulse on the 'reset' line (R) resets all latches to the 0 (off) state.

Parity Check (PC)



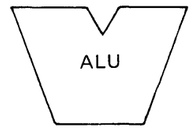
Checks the parity of a signal bus. If parity is not correct, line E becomes active to indicate an error.

Parity Generator (PG)



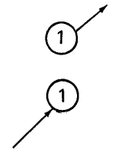
Generates the correct parity for a signal bus.

Arithmetic and Logic Unit (ALU)

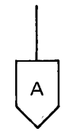


Performs arithmetic and logic operations in a processor.

On-Page Connectors



Off-Page Connector

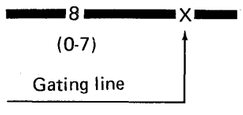


Electrical Connection

No Electrical Connection

Bus Containing 8 Lines

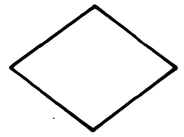
(bits 0 through 7)



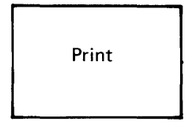
Boolean Algebra Symbols

- In a line name means AND
- \+ In a line name means OR

Symbols Used in Flowcharts

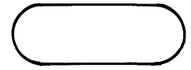


Decision block on a flowchart (asks a question)

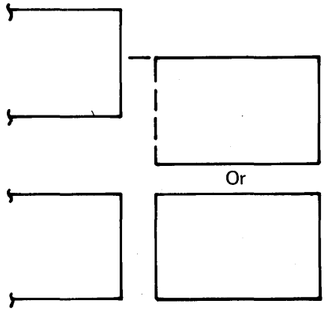


Processing block on a flowchart

Keying operation on a flowchart



Terminal on a flowchart



Note on a flowchart

This page intentionally left blank.