RC 9225 (#40521) 1/22/82
Computer Science 40 pages

THE IBM SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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Abstract: The IBM Selective Sequence Electronic Calculator (SSEC) was placed in operation in January, 1948. It was partly electronic and partly electromechanical. It is of historical interest, in part because of its capability of operating dynamically on its own stored instructions as data. This report includes a summary of its major functional units, its program and value formats, and the manner in which it operated. This description is based primarily upon information contained in U.S. Patent No. 2,636,672, "Selective Sequence Electronic Calculator," issued on April 28, 1953, to F.E. Hamilton, R.R. Seeber, Jr., R.A. Rowley, and E.S. Hughes, Jr.

Introduction

The IBM Selective Sequence Electronic Calculator (SSEC) was a large-scale electronic and electromechanical machine with all the system components of a modern general-purpose computer. It was developed and built in the IBM laboratory in Endicott, N.Y., in the period from 1945 to 1947, moved to IBM corporate headquarters in mid-1947, and placed in service with a formal dedication on January 27, 1948.

The SSEC performed its computations electronically, according to "lines of sequence" (instructions) stored in the same memory and in the same word form as ordinary data. Its memory consisted of three levels in three technologies, in order of increasing capacity and decreasing speed: electronic storage units (registers), relays, and punched paper tape. It was capable of modifying any part of an instruction in memory, including the part that specified the next instruction to be executed.

The SSEC contained 12,500 vacuum tubes, 21,400 electromechanical relays, and 66 paper tape readers, and occupied the periphery of a room about 60 feet long and 30 feet wide. It is of historical interest, in part because of its ability to modify its own program. It was not described in great detail in its own day (it was dismantled in mid-1952), and in order to produce the equivalent of a programmers's description of the machine, a study was made of U.S. Patent No. 2,636,672, "Selective Sequence Electronic Calculator," issued on April 28, 1953, naming as inventors F.E. Hamilton, R.R. Seeber, Jr., R.A. Rowley, and E.S. Hughes, Jr., of IBM. That patent is the primary source of information that has been used in this description.

I

CONTROL DESK

The Control desk is a manual switching center at which a duplicate of practically every control circuit in the machine may be set up by manipulating switches and keys. The control desk holds control keys such as start and stop keys; also sets of dial storage and the switches and keys for use in setting up an artificial line of sequence. A keyboard and connection are also provided at the control desk for applying desired numbers to relay storage. Cancel circuits (clearing circuits) for the MD calculating unit, the accumulator unit, the denominational shift unit, the electronic storage, the main commutator, the pilot units and every other unit desired may be operated individually or together from the control desk as well as automatically.

II

ARTIFICIAL LINE OF SEQUENCE

The machine is started by an artificial line of sequence, which is manually set. This consists of S1 or S2 data or both and is inserted in sequence storage under manual control, as the starting instruction for sequencing of operations of a problem. In other words, the artificial line of sequence data provides direction as to where the first real set or line of sequence data is to be obtained. By a real set of sequence data is meant such data as is called out automatically from tape storage or relay storage or other source for sequencing operations leading to the solution of some problem.

III

RECORD TAPES

The record tapes may be used to store values either for computational purposes or for program or sequence control purposes. Sequence data is made up of numbers which can be handled the same as the numbers involved in calculation. Tapes which store numbers for computation are called "value tapes." Tapes which bear programming or sequence data are called "program tapes." For both program and value tapes, the numbers are punched according to the same code, binary coded decimal, in which a complete binary zone which is called a column, is made up of four successive binary positions 8, 4, 2 and 1.

The record tape has the width of a standard 80 index position card, but owing to the space occupied by the marginal feed holes, 78 positions are allowed. In other words, tape has a capacity of 19 and half digit columns, or sufficient capacity to be punched, if desired, with representation of nineteen decimal digits and a sign. Hence, this row of 19 and one-half index positions illustrated in Fig. 1 is called a "word."

VALUE TAPE

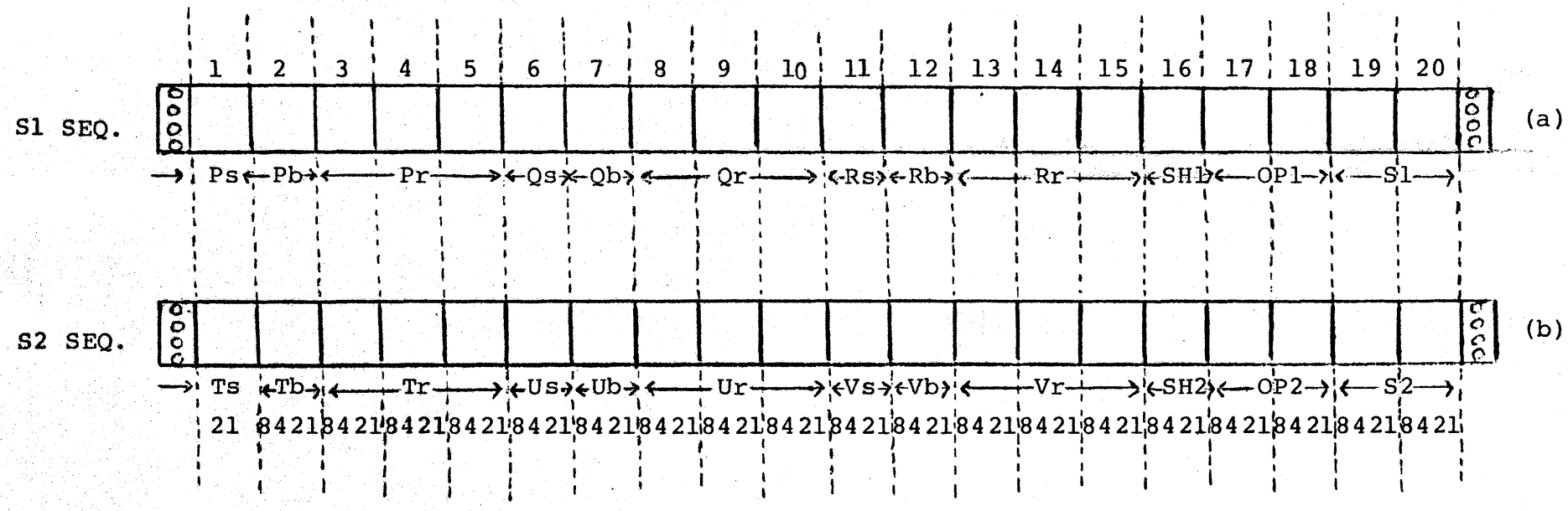

Figure 1

PROGRAM TAPES

Programming or sequencing of machine operation is controlled by the program tapes illustrative portions of which appear in Fig. 1 (a) and (b). Successive designation lines of the program tapes bear sequence data which may be referred to as an "instruction word," or as "sequence data." A complete line of sequence data is made up of two designation lines on a pair of program tapes. One half of the line of sequence data or one "word" is a designation line on one tape and the other half is a designation line on another of the tapes. The values of words are differentiated as S1 Seq. and S2 Seq. portions. So a program tape will be punched with either S1 Seq. data or S2 Seq. data. Both S1 Seq. and S2 Seq. data are similar with respect to the arrangements of fields and subfields, but have certain differences with regard to programming functions. S1 Seq. portion is made up of fields P, Q, R, SH1, OP1 and S1 (Fig. 1(a)), whereas, S2 Seq. of portion is made of fields T, U, V, SH2, OP2 and S2 (Fig. 1(b)). The fields Q, R, U and T may be used as either IN or OUT fields. Field P is always an OUT field and field V is always an IN field. An OUT field is one which calls for the reading out of data from a selected tape or relay storage source to a selected electronic storage unit by way of the out bus set fixed by association with the electronic storage. An IN field is one which calls for transmission of data from a selected electronic storage unit along the corresponding IN bus set to a tape or relay storage distinction. Each of the fields P, Q, R, T, U and V are divided into three subfields, s, b and r. Ps subfield comprises column 1, which is actually half a column (2 bits) with decimal values 0, 1, 2 and 3 only, and is used to designate the operational sign which is to be applied for a number read from a source. A perforation in binary position 2 designates operational "+" sign, i.e., the number taken from the source named in Pr (see later) is to be handled in calculation without any change of its sign. A perforation in binary position 1 represents operational "-" sign, i.e., the number read to be operated upon with an inversion in its sign. The absence of perforation in Ps represents "0," which is for operational fixed "+" sign, i.e., regardless of the original sign of the number it is to be treated as a positive number. Perforations in both binary 2 and 1 position represents decimal 3 which

means operational fixed "-" sign, or treating the number as "-" regardless of the original sign. Pb subfield is the column 2, which may contain the decimal values 1, 2, 3 ... 8, designating the electronic storage unit and corresponding out bus set involved.

Pr subfield is made up of columns 3, 4 and 5 bearing the hundreds, tens and units digits of the Code number for the source from which a value is to be transmitted to the electronic storage unit named in Pb.

When a subfield "b" in any program field P, Q, R, U, V and T is blank, it represents "0" and calls for the field to be, in effect, skipped over, during a scanning sequence of the program line. When a subfield r in an OUT field is blank, then it calls for transmission from the electronic storage unit named in its b field to the electronic storage unit named in the b subfield of an IN field, which may also be blank in its r subfield. Field Q may be used either as IN field or an OUT field. Subfield Qs is a complete decimal column, unlike Ps, and occupies column 6, in which 0, 1, 2, and 3 have same designation as Ps. Additionally, any of these numbers in Qs characterize Q field as an OUT field. Any digit in Qs higher than 3 makes Q an IN field. Besides the values 4 to 9 designate the tens denomination of a column shift and whether the shift to be executed to the left or right. The value 4 in Qs thus designates Q as an IN field and also calls for a shift to the right with a zero tens order. A 5 has same interpretation only with a shift to the left. The value 6 calls for right shift with a tens order shift of 1. 7 calls for the same amount of left shift. The value 8 calls for a right shift with a tens order shift of 2. 9 does the same for a left shift.

Subfield b, in column 7, is used to designate the electronic storage unit number to send or to receive data, depending on whether Q is an IN field or an OUT field. Qr is located in columns 8, 9 and 10 to represent the source from which a number is to be sent to the electronic storage unit if the field Q is an OUT field or to represent the receiving unit to which the number is to be transmitted from the electronic storage unit if the field Q is an IN field.

Field R is contained in columns 11 to 15 and its subfields are similar to the field Q and its subfield.

Field SH1 in column 16 designates the units order amount of column shift to be executed.

Field OP1, in column 17 and 18 calls for the fundamental calculating operations to be performed, such as accumulation, multiplication, division, etc.

The field S1 is a two column field in 19 and 20 which designates the source for next left half line of sequence data.

The right half line of programming, S2 Seq., has fields and subfields similar to those of the left half line, S1 Seq. Generally, all fields and subfields of S2 Seq. correspond to those of S1 Seq. with the following exceptions:

1. As mentioned before, field V is always an IN field while P is always an OUT field.

2. The field T can be either IN or OUT field depending on the code in the field OP2. When the latter field has the designation O1, it characterizes T as an IN field. In all other cases, the field T is an OUT field.

It is important to understand the sequential nature of the scanning and execution of the elementary operations called for in a line of sequence: The left half line, or word, is executed first; then the right half line; then the next half line, etc. Furthermore, within a half line, the fields are interpreted and the specified elementary operations executed also from left to right.

IV

ELECTRONIC STORAGE

The electronic storage units are used for the temporary storage of numbers, and may be compared to the general arithmetic registers of a modern computer.

There are eight similar electronic storage units designated as ES1, ES2 ..., ES8. Each has twenty columns (eighty bits) of decimal digit storage capacity. Entry into the ES may be made from the internal IN bus set or alternatively from the corresponding numbered OUT bus set. Read out or exit from an ES unit may be into the internal OUT bus set or alternatively into the corresponding numbered IN bus set.

All control and timing signals of ES are provided by the eight correspondingly numbered pilot units. Whenever any transfer occurs, the data are passed through the electronic storage unit. All numbers on the OUT bus sets enter electronic storage on their way to selected destinations.

All numbers on the IN-bus sets, with the exception of the artificial line of sequence from the dial switches, are taken from the associated electronic storage units and directed to the specified receiving units. The electronic storage units are numbered 1, 2, 3, ..., 8 and can be accessed by the use of corresponding digits in the single-column "b" subfield in the program sequence.

V

RELAY STORAGE

Relay storage consists of sets of relay storage registers, also called relay storage units, which receive numbers from the IN bus sets and store them until called out for transmission along the OUT bus sets. Certain of these relay storage units also serve to control the printing unit, as will be explained later (in printing section). There are ten sets of storage relays designated as the 0, 1, ..., 9 sets. Each set has fifteen storage units and each unit has twenty columns of storage relays, each column capable of storing a decimal digit. As the decimal digit is represented in BCD code, there are four relays in each column, which may be called "8," "4," "2" and "1" relays of a column. Each relay storage unit is identified by a three-decimal-digit number, which may appear in the "r" subfield of any IN/OUT field. The digit in units place is the number of the relay storage set containing that unit of storage. The two left hand digits form the unit identification number. Thus in relay storage set "0," the fifteen units are designated as 010, 020, 030, ..., 150; and for example, unit 159 is the 15th unit in the set 9. The code numbers for selecting relay storage units are the same as the identification numbers of these units except for certain special numbers relating to selection of relay storage units for controlling record operations. As mentioned earlier, all the numbers on an IN/OUT bus set from any source or to any receiving means are passed through ES (with the minor exception of the artificial line of sequence). Hence, when the program calls for a number to be entered into or taken out from a relay storage unit, it is necessary to refer one of the ES also, which is done by using the corresponding "b" subfield.

If only 10 column numbers are to be handled, then each storage unit can be used as a split storage device to store two numbers each with 9 digits and a sign. Right and left half of the storage unit can be reset and written independently. All these are done by plugging as has been explained in the Patent.

VI

TAPE STORAGE

Tape storage comprises three banks Nos. 1, 2 and 3, each with ten tape stations. Each bank has eight group sets associated with eight OUT bus sets 1 to 8. Selection of a unique tape storage location, therefore, requires selection of a tape storage bank and selection of one of its group outs. The selection of a bank is determined by the tape storage code number in the r subfield and selection of one of the group outs from this bank is determined by the digit in the adjacent b subfield. The code number for the tape storage stations run from 403 to 422 and 503 to 522 for bank 1; from 433 to 452 and 533 to 552 for bank 2; and from 463 to 482 and 563 to 582 for bank 3. It is clearly seen that the hundred order digit 4 or 5 identifies tape storage, and of tens order digits 0, 1, and 2 identifies bank 1, any of tens order digits 3, 4 and 5 identifies bank 2 and any of tens order digit 6, 7 and 8 identifies bank 3. The following section is not needed for programming purposes, but is included for better understanding.

TAPE STORAGE BANK

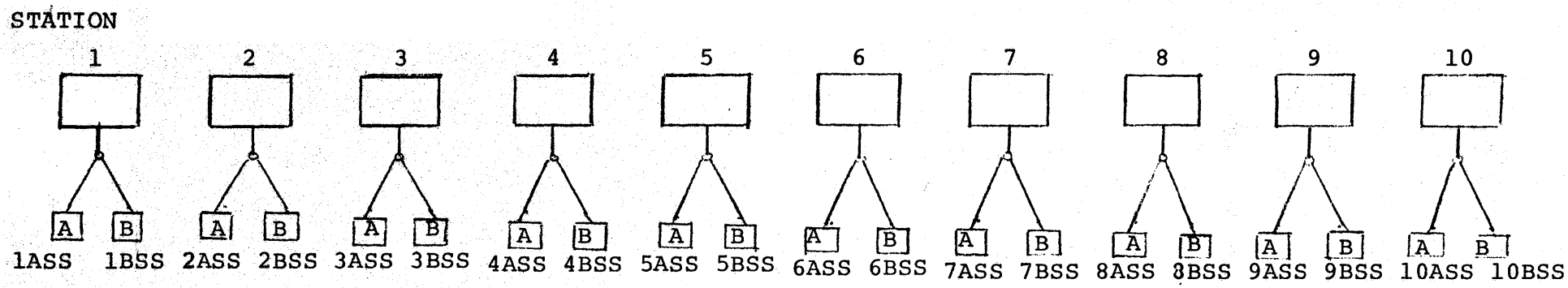

Figure 2

Figure 2 shows the ten tape stations in one bank. Associated with each station there are two outlets called station selector A and B. Each of the station selectors A comprise a gang relay ASS and each of the station selectors B includes a gang relay BSS. The station relays may be differentiated by a prefixed number corresponding to the associated station, e.g., relays 1ASS are associated with station 1. As there are thirty stations in all there are sixty station relays ASS and BSS. The tape storage code number calls for a particular one of these station relays. As explained before, all tape storage code numbers have 4 or 5 in their hundreds order digits. The distinction is that the hundred order digit 5 calls for the station tape to move after being read out while hundred order digit 4 calls for the station tape to remain at rest after being read out. Regardless of whether the hundreds order digit is 4 or 5, tens order digit 0, 1, 2 characterize code numbers for station relays in tape storage bank 1, tens order digit 3, 4 and 5 are in the code number for the relays in bank 2 and tens order digit 6, 7 and 8 select the relays of bank 3. Units order digits which are odd relate to relays ASS and those which are even related to relays BSS. The ten station relays in bank one identified as follows (ignoring the digit 4 and 5 in hundred order places): 1ASS by 03, 2ASS by 05, 3ASS by 07, 4ASS by 09, 5ASS by 11, 6ASS by 13, 7ASS by 15, 8ASS by 17, 9ASS by 19 and 10ASS by 21. The ten BSS relays in bank 1 are identified as follows: 1BSS by 04, 2BSS by 06, 3BSS by 08, 4BSS by 10, 5BSS by 12, 6BSS by 14, 7BSS by 16, 8BSS by 18, 9BSS by 20, and 10BSS by 22. Similarly the relays 1ASS to 10ASS of bank 2 are identified by code numbers 4 or 5 in hundreds order followed by 33 to 51 (all odds) and relays 1BSS to 10BSS in bank 2 by numbers 34 to 52 (all evens). The relays 1ASS to 10ASS in bank 3 are identified by 63 to 81 (all odds) and the relays 1BSS to 10BSS by 64 to 82 (all evens).

There are two more relays MA and MB for each bank of ten stations which, when energized, cause the tapes to move. Relay MA when energized allows any of the selected ASS relays of the bank to transmit the effect of a move signal to the related move network. Relay MB serves the same purpose in relation with the BSS relays. If the code number in the r field for a tape storage station had the hundreds order digit 4 then neither the MA nor MB

actuates. But if there is 5 instead of 4, then relay MA will be energized if any station relay ASS is selected or relay MB will be energized if any station relay BSS is selected. Thus, there are three factors to be considered in this selection or nonselection of the move relay. One, whether the hundreds order digit is 4 or 5; another, whether the units order digit is odd or even (i.e., whether ASS or BSS relay, whether MA or MB) and finally with respect to the selection of a move relay from a particular storage bank, whether the tens order digit is in one of the three mentioned group of digits.

VII

TABLE-LOOKUP UNIT

This unit is used to look up table values by comparing arguments punched in the tape with the computed arguments received from electronic storage units. The table lookup unit is used also to read sequence and value tapes.

This unit includes 36 tape stations which may carry tapes bearing tables of arguments and related function values. The tape argument may consist of from 1 to 5 columns of numerical digits punched in the left portion of the tape, starting with binary position 3 but not exceeding position 24. (3 and 4 contain the sign). The unit will handle up to 6 tables of one or two tape width, which can be arranged by plugs and connections. A table may consist of maximum 36 tapes in length if the table is only one tape wide, with a limitation of maximum width of 12 tapes wide.

The lookup operation is conducted by comparing the arguments portion of each successive word from tape with the computed argument. The argument selected is the last one that does not go beyond the computed argument. This determination is facilitated by the inclusion of a pair of reading stations. At that time the function value corresponding to the selected argument is available for reading out from the electronic storage unit via its associated bus.

The code for a table lookup is one of the numbers 281 to 286 in an "r" subfield. A program for this operation is:

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
2	1	127	4	1	281					02	01

which calls for a transfer of a computed argument from relay storage 127 to the table lookup apparatus (since 281 in "r" subfield represents Table 1) via ES1.

The selected functional value is positioned at the reading station of the selected tape unit. During the lookup operation other computations may be performed following the above line of instruction. After such calculation, the following line may be used for reading out the selected functional values.

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
			2	1	281	4	1	126	0	02	01

The selected functional value will be read out to ES1 after the execution of this line, and stored in the relay storage unit 127.

VIII

DIAL STORAGE

Here, unlike all other storage, data can be set manually by the operator. A dial storage bank consists of a set of twenty dial switches named as DS1, DS2, ..., DS20. Each dial switch is manually settable to a desired decimal digit. Thus, twenty digits, i.e., a whole word, may be registered by the set of dial switches. The switches are further identifiable as column 1 to column 20 switches to conform with the numbering of the bus columns. If the code number in an r subfield is "603," it calls for a value to be read out from the dial storage unit no. 3. The corresponding subfield "b" selects the dial storage group out and electronic storage, depending on which OUT bus set is to receive the value from the dial storage.

IX

PLUGGABLE STORAGE

Besides the various memory storage units, the machine provides pluggable storage as a convenient means for applying constants to the OUT-bus sets to be entered in electronic storage. Several pluggable storage units are provided. Ten of these are designated by code numbers 610 to 619, which may occur in subfield r of an OUT field of a line of sequence.

X

THE ELECTRONIC ACCUMULATOR UNIT

This is an arithmetical unit in the electronic computing section. When accumulation is called for, the accumulator unit receives numbers successively in binary coded decimal form (19 decimal digits) from the columns 11 to 29 of the internal IN bus. Along with each number, the internal IN bus set will supply the sign of the number to this unit. This unit can perform simple accumulation of positive and negative numbers. Means are also provided for rounding off up to a desired order of the result in the accumulator. The accumulator may also perform a special accumulation operation called tolerance check which will be discussed later.

Associated with the accumulator unit is a so-called internal commutator which subsequences all the operations of the accumulator upon reception of certain signals from main sequence.

A block diagram representation of the electronic calculating circuit has been attached (Fig. 3). The accumulator has 29 orders, of which the 29th is a result sign evaluating order. The internal IN bus columns 2 to 29 are connected respectively to entry means for accumulator orders 28 to 1. However, in the present case only the bus columns 11 to 29 may carry significant digits since it is only these columns which receive digits from electronic storage. These bus columns 29 to 11 are associated with accumulator orders 1 to 19 respectively. With regard to orders 20 to 28, they will receive "0" entries from the bus columns 2 to 10. The internal IN bus column 1 which carries the algebraic sign of the number to be entered in the accumulator is connected into a "sign mixing" circuit. The outputs of orders 1 to 28 are connected to the internal OUT bus columns 29 to 2 respectively and that of the 29th order is connected to the internal OUT bus column 1 to apply the sign of the result.

The operation will consist, in general, in entering the number from the internal IN bus set into the entry registers and thereafter from there transmitting the number to the corresponding

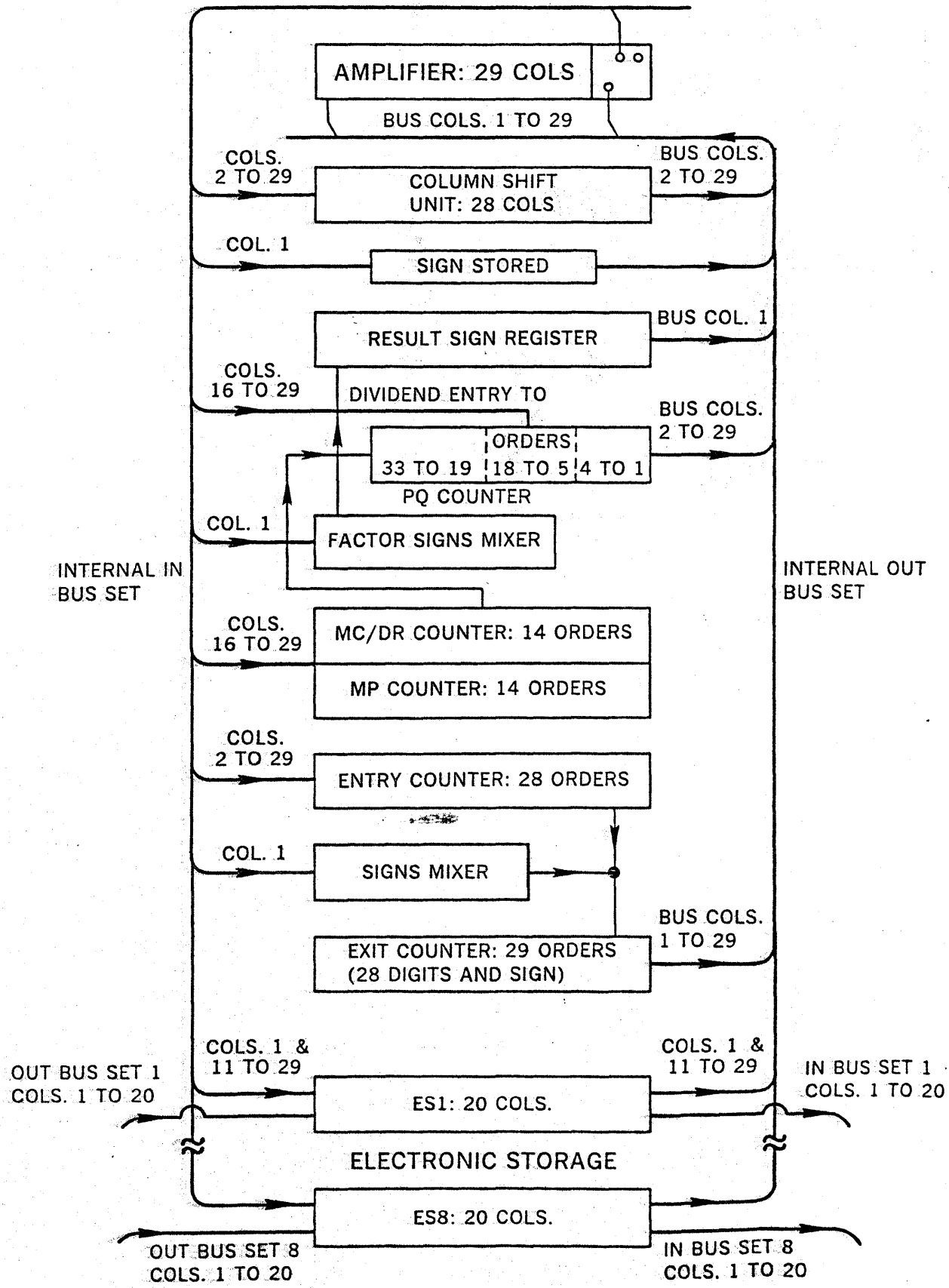
AMPLIFIER: 29 COLS
BUS COLS. 1 TO 29
COLS. 2 TO 29
COLUMN SHIFT UNIT: 28 COLS
BUS COLS. 2 TO 29
COL. 1
SIGN STORED
RESULT SIGN REGISTER
BUS COL. 1
COLS. 16 TO 29
DIVIDEND ENTRY TO
BUS COLS. 2 TO 29
ORDERS
33 TO 19
18 TO 5
4 TO 1
PQ COUNTER
COL. 1
FACTOR SIGNS MIXER
INTERNAL IN BUS SET
INTERNAL OUT BUS SET
COLS. 16 TO 29
MC/DR COUNTER: 14 ORDERS
MP COUNTER: 14 ORDERS
COLS. 2 TO 29
ENTRY COUNTER: 28 ORDERS
COL. 1
SIGNS MIXER
BUS COLS. 1 TO 29
EXIT COUNTER: 29 ORDERS (28 DIGITS AND SIGN)
COLS. 1 & 11 TO 29
COLS. 1 & 11 TO 29
OUT BUS SET 1 COLS. 1 TO 20
IN BUS SET 1 COLS. 1 TO 20
ES1: 20 COLS.
ELECTRONIC STORAGE
ES8: 20 COLS.
OUT BUS SET 8 COLS. 1 TO 20
IN BUS SET 8 COLS. 1 TO 20

Figure 3

orders of the accumulating registers. The first set of registers is called the entry counter. The second set of registers, the exit counter, comprises the accumulating device per se and its register orders are denominationally associated by carry means. Both "+" and "-" numbers may be accumulated and an albegraic sum obtained. All numbers are represented on the busses in true, binary form if the operation sign is "+." But if it is "-," then tens complement of the number in entry registers will be read out therefrom to the accumulating registers. The sign of a number and the operational sign may be 0, 1, 2 or 3, as previously explained.

XI

ACCUMULATION

Assume a line of sequence data selected by S1 and S2 numbers is as follows:

S1 Seq→	Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
	2	1	010	2	2	011	4	1	030	0	02	16
S2 Seq→	Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
	1	3	433	2	6	552	4	5	151	6	04	02

P is always an OUT field. The code number in this field calls for an amount to be read out of relay storage unit 010 (Pr) to OUT bus set 1 (Pb) and without a change in sign. The Q field is characterized as an OUT field by number 2 in QS and this number also specifies that the number to be read out of relay storage unit 011 (Qr) to OUT bus set 2 (Qb) is to be handled without any change of sign. The R field is characterized as an IN field by the 4 in RS which also calls for a shift to the right with a zero tens order. In its entirety, therefore, the R field calls for the result to be entered into relay storage unit 030 from accumulator via IN bus set 1 with a denominational shift to the right of zero tens order. The code number "0" in SH1 signifies the shift in units place digit will be zero. So it is clear that the denominational shift will be zero. Code number 02 in OP field calls for accumulation without half correction.

In brief, the instruction given by P, Q, R, SH1 and OP1 fields are to send numbers from relay storage 010 and 011 via electronic storage units 1 and 2, respectively, to the accumulator to be accumulated without change in sign of the numbers and without half correction and for the algebraic sum to be routed through the denominational shift unit without column shifting and then via electronic storage 1 to relay storage unit 030.

The T field is classed by 04 in OP2 as an out field. 433 in Tr calls for the number to be read from the tape at station 1 in the tape storage bank via the A outlet of this station via electron-

ic storage ES3 (Tb) and for the tape to remain at rest after the number has been read out. Ts signifies that the sign of the number is to be changed. Field U is classed as an out field by 2 in Us which signifies further that no change of sign should take place. Number 552 in Ur calls for the number to be read out of the tape at station 10 in bank 2 via the B outlet of this station through the ES6 (Ub) and for the tape to be moved after the number has been read out. Field V is always an IN field, and 4 at Vs calls for a zero tens place right shift. Digit 5 in Vb indicates that the transferred should be through IN bus set 5 via ES5. Vr represents relay storage 151 which is the 15th unit of set 1 and which is the destination of the result from accumulator. Code 04 in OP2 instructs the machine to perform accumulator, with half correction of the result.

In short, the instructions given by T, U, V, SH2 and OP2 are that the numbers from stations 1 and 10 of bank 2 be applied via their A and B outlets to out bus sets 3 and 6, respectively, to be routed through electronic storage units 3 and 6; that the tape at station 10, bank 2 be advanced after the number has been read; that the sign of the number taken from station 1, bank 2 be changed; that the result be shifted by the denominational shift unit 6 places to the right; that the half correction entry of 5 be made in the 5th order of the sum before denominational shift is completed and that the rounded off result be routed via electronic storage unit 5 to relay storage unit 151.

In the preceeding example, we have seen instructions for combining pairs of numbers in one instance by addition and without half correction or shift, and in the other instance by subtraction with half correction and denominational shift of the result.

Suppose another line of sequence of data is:

S1 Seq→	Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
	2	1	012	2	2	013	1	3	030	0	01	01

S2 Seq→	Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
	0	5	121	1	4	151	4	1	122	0	01	02

The code 01 in OP1 calls for accumulation without half correction of the accumulated result. The interpretation of this program sequence is as follows. A number is to be taken from relay storage unit 012 (Pr) and applied to OUT bus set 1 (Pb) without any change of sign (PS=2). A second number is to be taken from relay storage unit 013 (Qr) and applied to OUT bus set 2(Qb) without any change of sign (QS=2). A third number to be read out of relay storage unit 030 (Rr) to OUT bus set 3 (Rb) to be handled with a change in sign (RS=1). These numbers are to be entered successively to the accumulator (OP1=01). The accumulated result and sign are to be transmitted to relay storage unit 121 (Tr) via IN bus set 5 (Tb) as T field is characterized as an IN field (OP2=01).

After executing one in field (i.e., storing one result) the machine clears the accumulator and proceeds to scan the rest of the sequence. The number in relay storage unit 151 (Ur) is routed to accumulator via ES4 (Ub) with a change in sign (Us is 1). The number changed in sign is to be transmitted via the denominational shift unit without column shifting (VS=4, SH2=0) via ES1 (Vb) to relay storge unit 122 (Vr). This program shows the accumulation of three numbers and utilization of T field as an IN field. Also it shows that other operations are possible with multi word accumulation. If in this example we should use 02 for OP2 then T field would be an OUT field. In that case the terms selected by P, Q, R T (OUT field) and U fields would be accumulated and their result stored in the unit selected by V field. A single line of sequence thus may call for successive accumulation of a maximum of five numbers. If it is desired to accumulate more than five numbers, two or more lines of sequence may be used. In that case, V field of each line except the last line will be left blank and will act as a skip field. The V field of last line will be the IN field to store the result of accumulation and its sign. Obviously, any number of terms may be accumulated successively and directly in this manner.

XII

MULTIPLICATION

If the code number in OP field is 10, multiplication without half correction is called for and if it is 15, then multiplication with half correction is ordered. A maximum of two multiplications can be ordered by a complete line of sequence with each multiplication in one half lines. An example of S1 Seq. of data calling for multiplication without half correction is given below:

S1 Seq.	Ps	Pr	Pb	Qs	Qr	Qb	Rs	Rb	Rr	SH1	OP1	S1
	1	1	017	2	2	158	4	3	139	0	10	01

The above program calls for a number from relay storage unit 01 (Pr) to be sent to ES1 (Pb) and thence to the MD unit (multiplying and dividing unit) to serve as the multiplicand and for the "-" operational sign to be applied to the sign mixing circuit; for the number from storage unit 158 (Qr) to be sent to ES2 (Qb) and from there to the MD unit to serve as multiplier and for the "+" operational sign to be applied; the product to be noted through the denomination shift unit without column shifting and to ES3 (Rb) and transmitted from there to relay storage unit 139 (Rr) with the sign of the product being determined by the sign mixing network.

XIII

DIVISION

The code number 20 in the OP field calls for division without half correction which may be ordered by a half line of sequence. The code number 25 in the OP field calls for division with half correction of quotient. A sample half line of S2 Seq. for a division without half correction is,

S2 Seq.	Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Br	SH2	OP2	S2
	2	1	151	1	2	142	4	130	136	9	20	02

This program instructs the machine to take the divisor from relay storage unit 151 (Tr) and direct it via ES1 (Tb) to the MD unit without sign change; to take the dividend from relay storage unit 142 (Ur) and bring it through ES2 (Rb) to the MD unit; to pass the quotient to the denominational shift unit where it shall be shifted nine places to the right (VS = 4, SH2 = 9), and to transmit the shifted quotient to ES3 (Vb) and thence to relay storage unit 136 (Vr).

XIV

COMPUTED OR MODIFIED SEQUENCE

For some problems the course and characteristics of the calculation have no deviations, and pre-chosen program paths and instructions may be used. For other problems, the course or extent of calculations varies according to computed results and completely preselected sequence lines are not suitable. Because simple, computable numbers have been used as instructions, the lines of sequence may be computed to steer (a) the course, (b) the nature, and (c) the extent of subsequent calculation. In this section we will show an example of the first of the capabilities, computed selection of the sequence path. Let's consider a program for finding the square root of a number N using Newton's formula

$$X(NEW)=(X(OLD)+\frac{N}{X(OLD)})/2.$$

As by this time we are already familiar with the way in which accumulation, multiplication, division, etc. are accomplished in the SSEC program, we won't discuss those elaborately. Instead, the terms shown in parenthesis in the program will carry the information about calculations in progress.

P	Q	R	SH1	OP1	S1	T	U	V	SH2	OP2	S2
s b r	s b r	s b r				s b r	s b r	s b r			
2 5 031	2 6 128	4 2 032	8	25	22	2 2	2 5	4 3 033		02	21
(X(0))	N	(N/X(0))					(X(0)+N/X(0))				
2 3	2 4 614	4 5 129	1	15	22	0 0	2 5	4 1 100	5	04	21
	(X(0)+N/X(0))/2=X(N)							$X(N)/10^5$=t (tolerance)			
2 5	1 4 031	4 2 034		02	22	2 1	3 2	6 3 157	9	02	21
(X(N)-X(0))=d (difference)							(t-d)='+' or '-'				
2 5 157	2 3 613	4 1 152		02	22	2 2 612	2 5	4 4 153		02	21
(27±5) =32 or 22							(26±5)=31 or 21				
					32 or 22		2 5 129	4 5 031		02	53
							(X(N) goes to unit 031)				31 or 21

X(0)=X(OLD) is the first guessed square root which is preliminarily put into storage unit 031. The first calculated approximation of square root X(N) is to be used to obtain tolerance. Tolerance is computed in the second half of the second line by dividing X(N) by 10^5, which is equivalent to shifting it five places to the right. The second half of 3rd line computes (t-d) and shifts the result to the right, 19 places to discard the numerical value of the result and to leave the sign only, which is enough information to know whether the computed value is less or greater than the tolerance. The "+" or "-" sign is transmitted from ES3 to column 1 of relay storage unit 157, which has been preliminarily plugged so that its two halves will be reset and receive data independently. The constant 5 is preliminarily entered in the right hand column of the right half of storage unit 157 through pluggable storage. Hence standing in 157 is ± 5. Pluggable storage has been preliminarily set to apply the number 27 to out bus set 3. The Q field of the 4th line of sequence does that. The same half of the 4th line does the accumulation of ± 5 and 27 and transmits the result 32 or 22 in relay storage unit 152 during the execution of the R field. During the execution of the second half of the 4th line number, 26 is directed from pluggable storage to the ES2 and hence to the accumulator after which ± 5, which was buffered in ES5 by unit 157, is applied to the accumulator and the result 31 or 21 is transmitted in relay storage unit 153.

Now present in relay storage units 152 and 153 are computed S1 and S2 numbers. The output hubs 52 and 53 of S1 and S2 pyramid are preliminarily plugged to relay storage hubs 152 and 153, respectively. During the execution of the 5th line of sequence, therefore, the next computed line of sequence is called out from relay storage 152 and 153 and transmitted to sequence storage. The computed line of sequence just transmitted comprises S1 and S2 numbers 32 and 31 respectively, if the first calculated approximation X(N) and the first guess X(0) do not differ from each other by more than "t." This means the square root of N has been calculated to the required degree of accuracy so the main sequencing path may be resumed for the continuation of the main calculation. On the other hand, if the computed S1 and S2 numbers are 22 and 21, i.e., the difference d is greater than the tolerance t then the

iteration sequence is repeated. During the execution of the 2nd half of the 5th line the first calculated square root X(N) is transmitted from unit 129 to unit 031 and so has replaced the first guess for the next iteration sequence.

In this manner the above loop can be run as many times as necessary to obtain a square root with required accuracy and when it has been obtained, the computed S1 and S2 numbers will be 32 and 31 and will direct the calculation into the main path. Besides the modification of sequence codes, other modifications of the program through computation are possible. These include, for example, computed operation code, shift code, address code (any of the six "r" subfields), bus code, operational sign code. An example of each of these has been given in the SSEC patent.

XV

TOLERANCE CHECK

This check ordinarily serves for checking the accuracy of computations. Through programming, the same computation is done by two different methods and the results are stored and later brought to the accumulator -- one as a negative and one as a positive number -- so that accumulator can obtain the difference, if any, between the two computation results. This difference is then read out of the accumulator and re-entered therein as a negative absolute number. The main sequence then selects the source for a tolerance number which is usually set up in dial storage no. 3. This tolerance number is the allowable difference between the results of two computations of a particular problem. This number is entered into the accumulator unit as a positive number. If the tolerance number is less than the difference between the two computations, then the result of the comparison is negative and out of tolerance, and machine operation is interrupted. If the tolerance number is equal to or greater than the difference between the two computations then the result is positive and the scanning of sequences is continued. In other words, if the 29th order of the accumulator is at "0," then the algebraic sum of two numbers sent to the accumulator is positive, hence, in present case the program continues, but if the 29th order is at "9," then it is negative and program is interrupted. An illustrative line of sequence ordering an answer tolerance check is given below:

S1 Seq.	Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
	2	3	016	1	2	137	4	1		0	02	01
S2 Seq.	Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
	2	6	603	3	1		4			0	03	02

S1 Seq. calls for the answer relay storage unit 016 (Pr) to be sent via electronic storage unit ES3 (Pb) to the accumulator unit to be acted on without a change in sign (Ps is 2); the

answer in relay storage unit 137 (Qr) to be brought via electronic storage ES2 (Qb) to the accumulator unit to be subtracted (Qs is 1; which implies "-" sign of the number) from the number previously accumulated, and the difference will be stored in electronic storage unit 1 (Rb), because R field is an IN field (Rs is 4). The S2 Seq. of the above line calls for the tolerance number, which is set from the outside to be read out (OP2 is not 01, hence T is OUT field) of dial storge unit no. 3 (Tr is 603) and via ES6 to the accumulator unit to be handled without a change of sign; the answer difference in electronic storage unit 1, (Ub is 1) which was stored there by R field to be sent to the accumulator unit to have its absolute value subtracted (Us is 3) from the tolerance number and the proceed signal will be produced (Vs is 4), if the tolerance check (required code is 03 at OP2) finds the answer difference to be equal to or less than the tolerance number.

The tolerance check can be used for some other purposes. For instance, it can be used to stop computations, when a table of f(x) has been computed between the limits of +0.001 and 0.0075. To check the upper limit, the tolerance number +0.0075 may be used and f(x) value is subtracted therefrom, and to check the lower limit the number -0.001 is added to each f(x) value. This check may be made after each computation of f(x). The line of sequence is:

S1 Seq.	Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
	16	1	012	1	2	013	4			0	03	01
S2 Seq.	Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
	2	3	014	2	2		4			0	03	02

The upper tolerance value +0.0075 is in relay storage unit 012 (Pr) and the lower tolerance value -0.001 is in relay storage unit 014 (Tr). The value of f(x) obtained from the last computation is in relay storage unit 013 (Qr). As the code for both OP1 and OP2 is 03, the tolerance check means will be used in both half of scanning sequence. At the first of calculating steps the entry of upper tolerance limit into ES1 (Pb), the value of f(x) into ES2

(Qb) and the lower tolerance limit into ES3 (Tb) will be made from corresponding relay storage. In the second step, the upper limit is transferred from ES1 to the accumulator without any change in the sign (Ps is 2) and the value of f(x) will be transferred from ES2 to accumulator with a change in sign (Qs is 1). This change in sign of one of the two numbers being sent to the accumulator, causes the subtraction. If the value of f(x) is equal to or less than the upper tolerance limit in the result of the accumulation or the number in accumulator is positive then proceed signal will be generated. If check result is negative then the scanning sequence will stop. Assuming as above, the value of f(x) is less than the upper tolerance, then the program will start the second half of the scanning sequence. First step of this half that the accumulator will be cancelled and the previous values will be cleared, then the lower tolerance limit will be transferred from ES3 to the accumulator without any sign change. If the value of f(x) is not smaller than +0.001, then the addition of this value to the lower tolerance number -0.001 will produce a positive number, otherwise negative. During the scanning of V field, the result of the second check will be tested and proceed signal will be generated if the test result is positive.

XVI

HALF CORRECTION

The number of digits in the product is either equal to or one less than the sum of the digits in the multipliers and multiplicand factors. The rounding off of a result is called for only in connection with a column shift to the right. The number of digits to be discarded is equal to the column shift to the right. The product may be a maximum of 28 digits (as allowed maximum number of decimal digits in both multiplier and multiplicand is 14), but the receiving unit is designed to receive a maximum of 19 digits plus the sign. Therefore, when the product is the full 28 digits, then at least 9 rightmost digits must be discarded through the operation of denominational shift. In such a case, the column shift amount will be nine and a shift to the right will be signalled for. The half correction or rounding off operation consists of adding 5 to the order of the number at the right of the rightmost digit to be transmitted through the receiving unit.

XVII

PRINTERS

Each of the two printers is capable of printing, on one line, the numbers stored in four relay storage units. For printer No. 1, the storage units are 120, 121, 122, and 123. It prints, on one line, either four 19-digit numbers with their four signs, or eight 9-digit numbers with their eight signs, depending on how these relay storage units are being used. The units may be filled in any order and printing may be called for upon filling the fourth storage unit by substituting a "6" for the "2" in the middle digit of the code number for that unit. (See Table 3.) A line of sequence calling for printing may also include one or two calculations. The printer code number will always appear in the last program field that specifies entry into relay storage units 120-123. Consider a programming example:

S1 SEQ	Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
	2	1	010	2	2	011	4	3	123	0	01	01
S2 SEQ	Ts	Tb	Tr	Os	Ob	Or	Vs	Vb	Vr	SH2	OP2	S2
	0	4	121	4	5	122	4	6	160	0	01	02

This program calls for the accumulation of the number in storage 010 and 011, the transmission of the result to storage 123, to 121 (T is an infield), to 122 and to 120 (160=120). At this point (Vr=160) when 160 is recognized, a printing cycle is called in to print numbers placed in 120, 121, 122, and 123. (This program may be used to check the relay storage unit.) Another printing program is:

S1 SEQ.	Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
	0	0	0	2	1	151	6	2	161	0	02	01
S2 SEQ.	Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
	2	3	010	2	4	011	4	5	012	5	15	02

In this case, the number in relay storage unit 151 is transmitted to storage unit 121 (Rr being 161) with a shift of ten places to the right, and the printing is called into operation to print the numbers in 120, 121, 122, and 123. Here, if any of the relay storages 120-123 is blank, then the machine will print nothing for those storage. Actually this program assumes that the numbers are already present in storage 120, 122, and 123. The second half of the sequence schedules a multiplication, showing that other calculation can be performed concurrently with printing. Third example is:

S1 SEQ.	Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
	2	1	101	2	2	011	4	3	120	0	02	01
S2 SEQ.	Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
	2	4	121	2	5	122	4	6	163	0	10	02

The first half of the program calls for addition of the numbers in storage unit 010 and 011 and entry of the sum in 120. The second half calls for the multiplication of the numbers in 121 and 122 and entry the product into 123 (vr=163). Since, Vr is 163, the sum is 120, the factors in 121 and 122 and the product in 123 will all be printed on the same line.

Comment - One discrepancy is that whenever the program calls for printing the contents of 120-123, all are printed. No one of them can be printed individually.

XVIII

OTHER INPUT/OUTPUT DEVICES

The input data for the SSEC is entered in two ways, by punched cards or by punched tapes. There are two card readers each of which reads 200 eighty column cards in a minute. There are two types of coding provided for read out of data from cards, one that causes a read out followed by a card feed operation and one that causes only read out. The card readers deliver the numbers from the cards they read to memory units 150-154 for Reader No. 1 and 155-159 for Reader No. 2. If only one number is to be read from a card then the other four memory units for that card reader are available for normal relay memory use. When certain numbers are required repeatedly in the course of a problem or at very close intervals or in great numbers, a tape is automatically prepared in advance by means of an auxiliary reproducing punch which is arranged to read 300 cards and punch 300 lines of tape a minute. The punching done by this unit is checked in the same operation to give complete assurance of true copy of the card data on the tape. The tapes may be placed on any of the 66 tape reading stations (as described in Section VI). The data from the tape are read into the calculator directly over the main buses without the aid of special relay memory units. The operation and codes for addressing for tape reading have been described in the tape storage section (Section VI).

When intermediate or final results or data are to be delivered as an output, they are supplied to the user in three ways, by printing, by punched cards and by punched tapes. The relay storage units and corresponding address codes for printing have been discussed in the printing unit section (Section XVII) for Printer No. 1. Similar coding applies for printer no. 2, but the corresponding relay storage units are 126-129. Even if only one number is to be printed, the other three storage units corresponding to that printer cannot be used as normal relay storage units while printing continues. The numbers stored in punched cards are usually final results. Eighty column cards may be punched at the rate of 100 a minute on any of the

two card punches. Four pairs of relay memory units are associated with each punch. Each pair of relays is used in an alternating mode to be described shortly. When more than one pair of memory unitd are used, the entry of the last number before punching is done by a sequence code that directs the unit to store and also initiates the operation of the punch. Results to be punched on cards are placed in memory units 130-133, 136-139, 140-143 and 146-149. The numbers which are punched in paper tapes on one of the three tape memory units are sent to designated relay memory units associated with each of the tape units, namely units 134 and 144; 135 and 145; 115 and 125 for tape units no. 1, no. 2 and no. 3, respectively. The instruction to store in a tape memory unit causes the tape punch on the tape unit to operate after the number has been stored in one of the two alternate relay memory units. While a number is being punched, the correct punching of the previous number is being checked against the number standing in the alternate memory unit.

Thus, as we see from the above discussion, 40 units (16 units for card punch, 6 units for tape punch, 8 units for printers and 10 units for card readers) out of 150 relay storage units are used as auxiliary storage in connection with the input and output devices of the SSEC. The rest of 110 relay storage units are solely memory units. Of course, those forty units can also be used as memory, if programmed accordingly. Whether they will be used as normal memory, or for input/output transfer is established by programming, using the sequence codes given in table No. III.

SEQUENCE	FIELD	SUB FIELD (DIGITS)	VALUES	INTERPRETATION
LEFT HALF	P (only out field)	s (1/2)	0	Operational Fixed Positive sign.
			1	Inversion in the original sign.
			2	No change of sign.
			3	Operational fixed negative sign.
		b (1)	0	Corresponding field to be skipped
			1-8	Electronic storage unit and corresponding in/out bus set (for in/out field)
		r (3)	-	Destination/source (for in/out field, as applicable) of data or program word in storage including relay storage, dial storage, tape storage, pluggable storage and table look-up unit. (See Table No. 2)
	Q (both out and in field)	s (1)	0-3	Same as Ps, in addition, any of them characterize the field as an out field
			4	The field is an in field and a shift to the right with a tens order shift of '0'
			5	The field is an in field and a shift to the left with a tens order shift of '0'
			6	The field is an in field and a shift to the right with a tens order shift of '1'
			7	The field is an in field and a shift to the left with a tens order shift of '1'
			8	The field is an in field and a shift to the right with a tens order shift of '2'
			9	The field is an in field and a shift to the left with a tens order shift of '2'
		b(1)	0-8	Same as Pb
		r(3)	-	Same as Pr
	R (both out and in field)	s(1)	0-9	Same as Qs (see note below)
		b(1)	0-8	Same as Pb
		r(3)	-	Same as Pr
	SH1(1)		0-9	Units order of column shift
	OP1(2)		00	No operation of the accumulator
			01	Accumulation without half correction
			02	Accumulation without half correction
			03	Tolerance check
			04	Accumulation with half correction of the sum
			10	Multiplication without half correction
			15	Multiplication with half correction of the product
			20	Division without half correction
			25	Division with half correction of the quotient
	S1(2)		-	Source for the next left half line of sequence data
RIGHT HALF	T* (both in and out field)	s(1/2)	0-3	Same as Qs (see note below)
		b(1)	0-8	Same as Pb
		r(3)	-	Same as Pr
	U (both in and out field)	s(1)	0-9	Same as Qs (see note below)
		b(1)	0-8	Same as Pb
		r(3)	-	Same as Pr
	V	S(1)	0-3	Not used, as they are not necessary, (see note below)
			4-9	Same as Qs with an exception that this field is always an in field
	(only in field)	b(1)	0-8	Same as Pb
		r(3)	-	Same as Pr
	SH2(1)		0-9	Same as SH1
	OP2(2)		-	Same as OP1 with an exception only when the code is 01, which characterizes T field as an in field. In all other cases T field is an out field.
	S2(2)		-	Source for the next right half line of sequence data.

* See interpretation of field OP2.

Note: As the sign of result is already determined, digits 0-3 are invalid in 's' subfield of any in field.

TABLE I

Type of Storage	Code Number	INTERPRETATION OF CODE NO.	
Relay Storage (1)	010-159	Units digit identifies one of the ten sets of relay storage units. The two left digits distinguish one of 15 units in the set.	
Table Look-up Unit	281 to 286	Address of Table 1-6 respectively.	
TAPE STORAGE (2)	4**	Station tape remains at rest after being read out.	
	5**	Station tape is to be moved after read out.	
	0 *1* *2*	IDENTIFIES BANK 1	ODD UNITS ORDER DIGITS RELATE TO ASS RELAYS, EVEN UNITS ORDER DIGIT RELATES TO BSS RELAYS.
	3 *4* *5*	IDENTIFIES BANK 2	
	6 *7* *8*	IDENTIFIES BANK 3	
Dial Storage	603	Address of dial storage no. 3 (3)	
Pluggable Storage	610 to 609	Address of ten units of pluggable storage.	

(1) For special use of relay storage, see Table 3.

(2) See Section VI also.

(3) Dial storage no. 1 and no. 2 are used for artificial line of sequence.

TABLE 2

INTERPRETATION OF STORAGE CODES

I/O DEVICE	NORMAL RELAY STORAGE OPERATION	CODES USED		
		I/O TRANSFER	ALTERNATING STORAGE	
			NO I/O TRANSFER	I/O TRANSFER
1. CARD READER #1	150 - 154	170 - 174		
2. CARD READER #2	155 - 159	175 - 179		
3. CARD PUNCH #1	130 - 133 140 - 143		180 - 183	190 - 193
4. CARD PUNCH #2	136 - 139 146 - 149		186 - 189	196 - 199
5. TAPE READERS: AS GIVEN IN SECTION VI AND TABLE 2.				
6. TAPE PUNCH #1	134 144			194
7. TAPE PUNCH #2	135 145			195
8. TAPE PUNCH #3	115 125			185
9. PRINTER #1	120 - 123	160 - 161		
10. PRINTER #2	126 - 129	166 - 169		

TABLE 3

CODES FOR SPECIAL USES OF RELAY STORAGE AS I/O BUFFER

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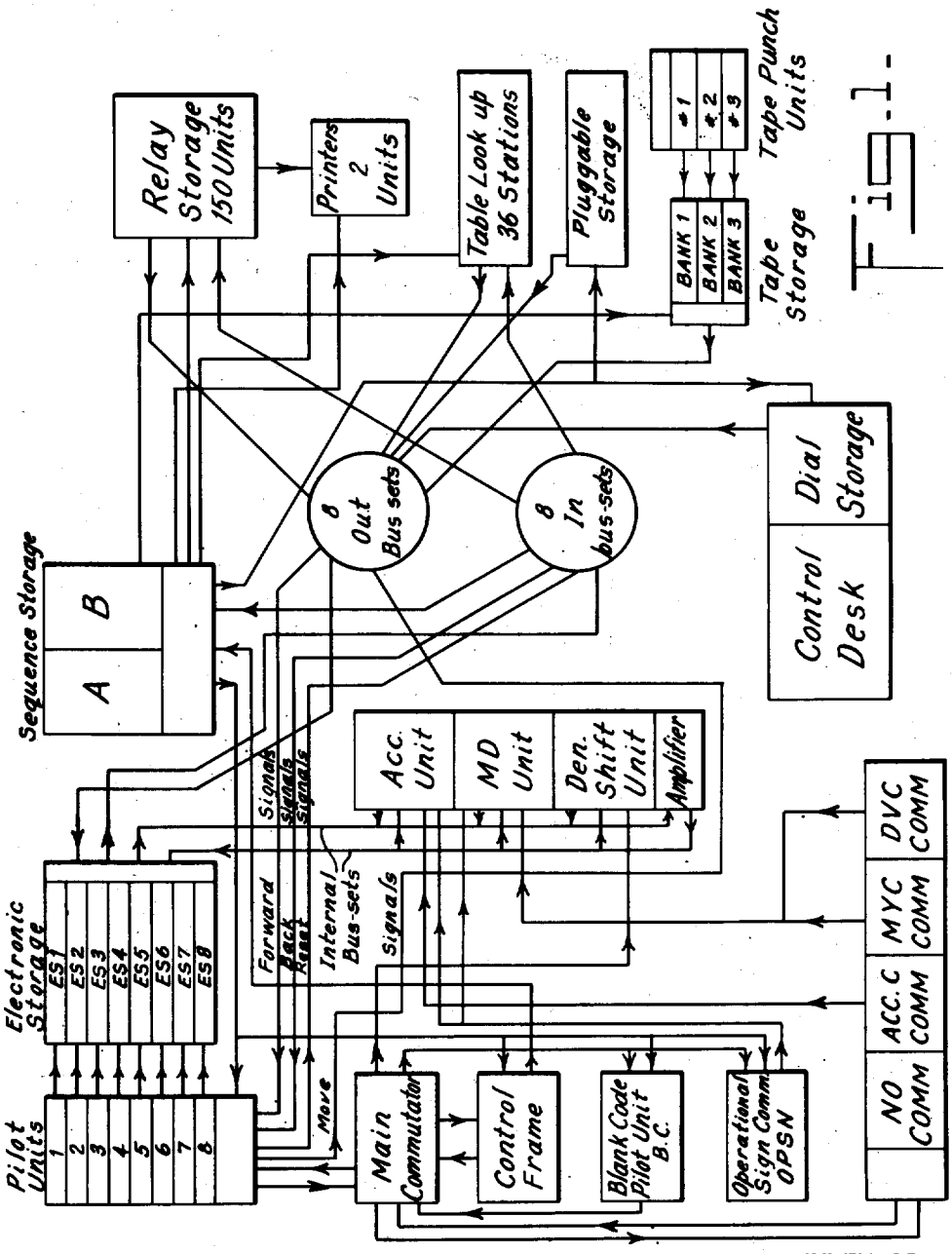

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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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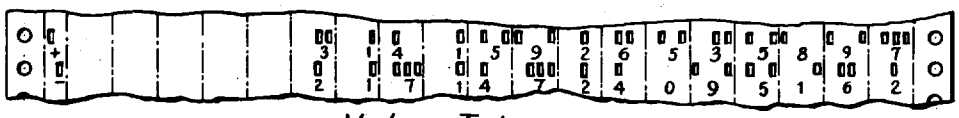
Fig. 2.



Value Tape

Fig. 3.

Program Tape - S1Seq Data

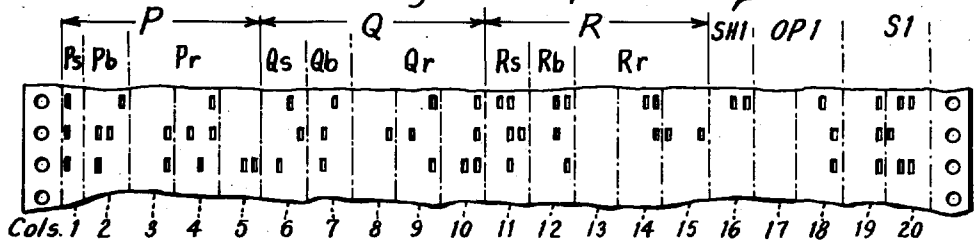
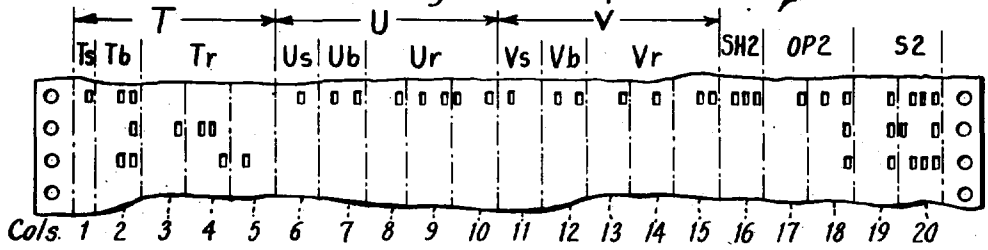


Fig. 4.

Program Tape - S2Seq Data



Code

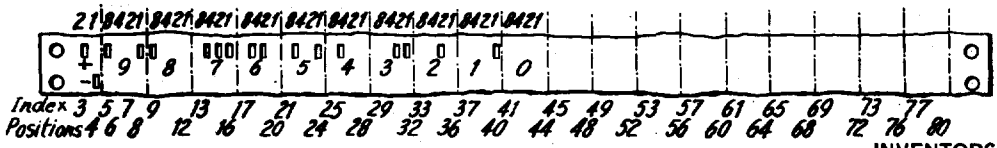


Fig. 4a

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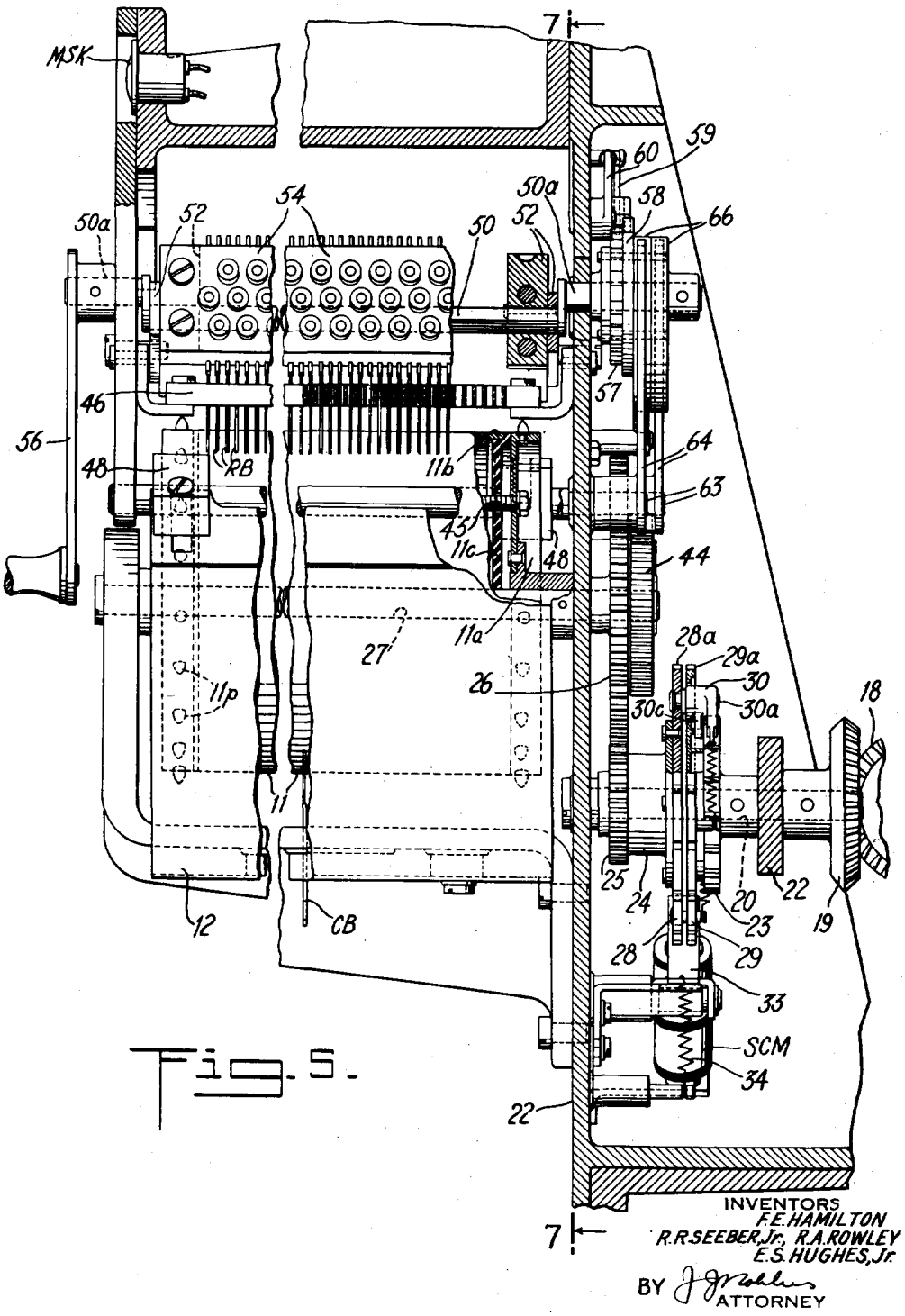

Fig. 5.

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Fig. 6.

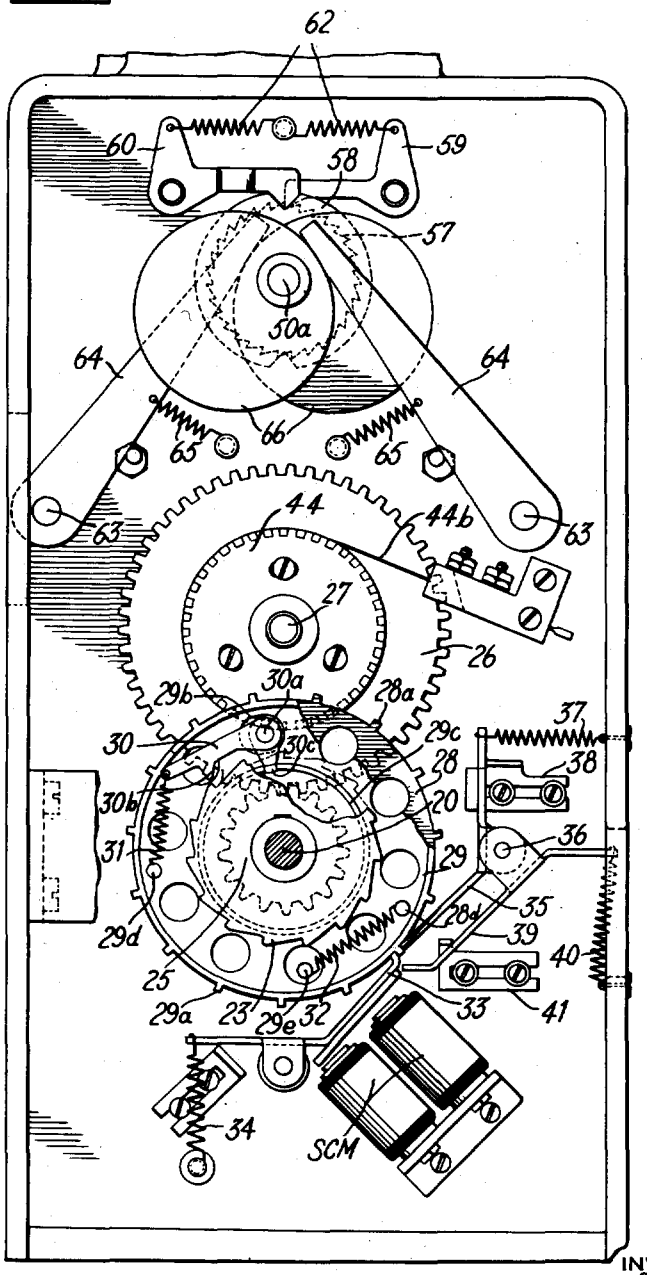

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Fig. 7.

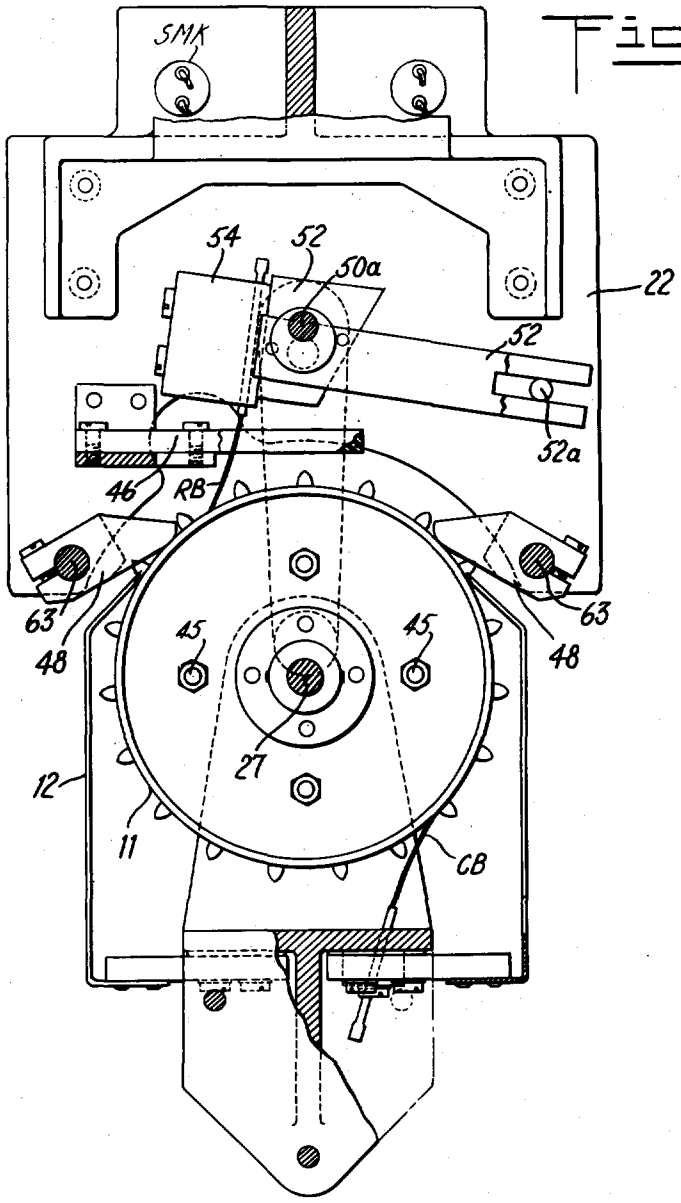

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Fig. 8.

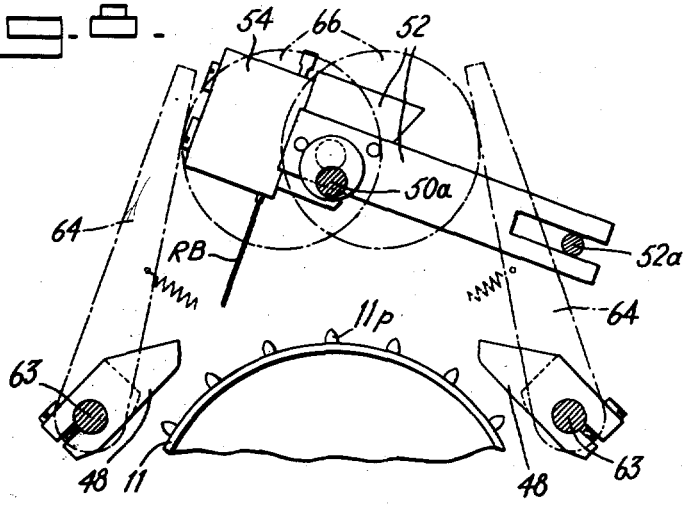
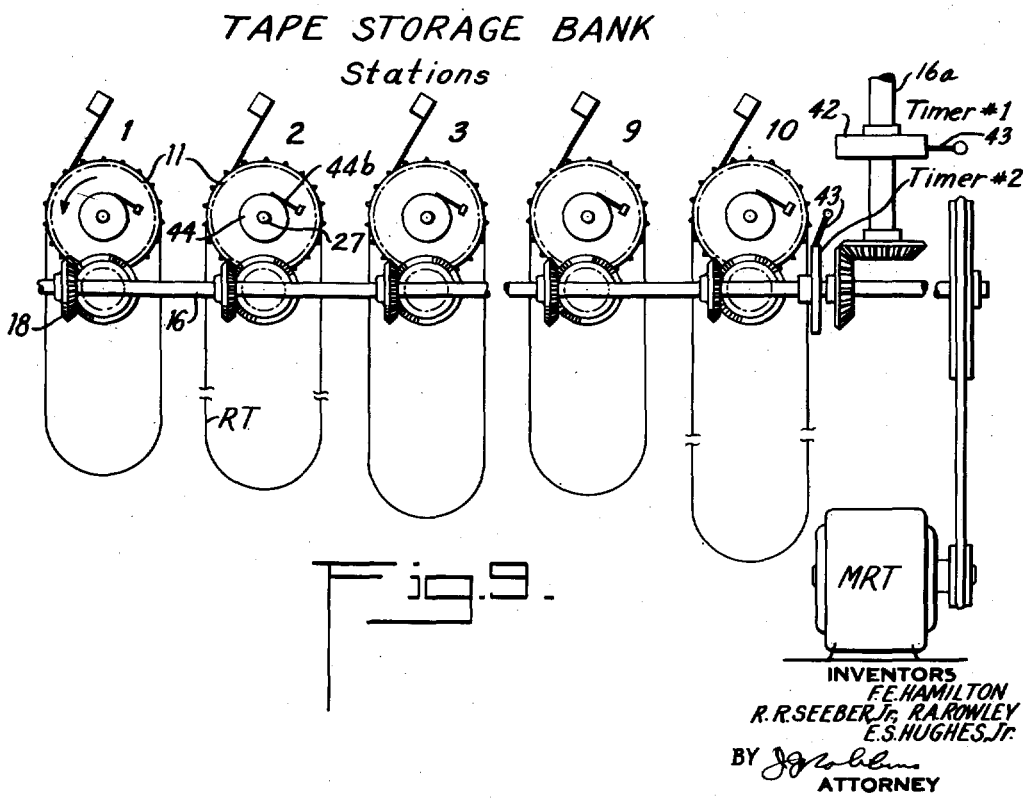


Fig. 9.



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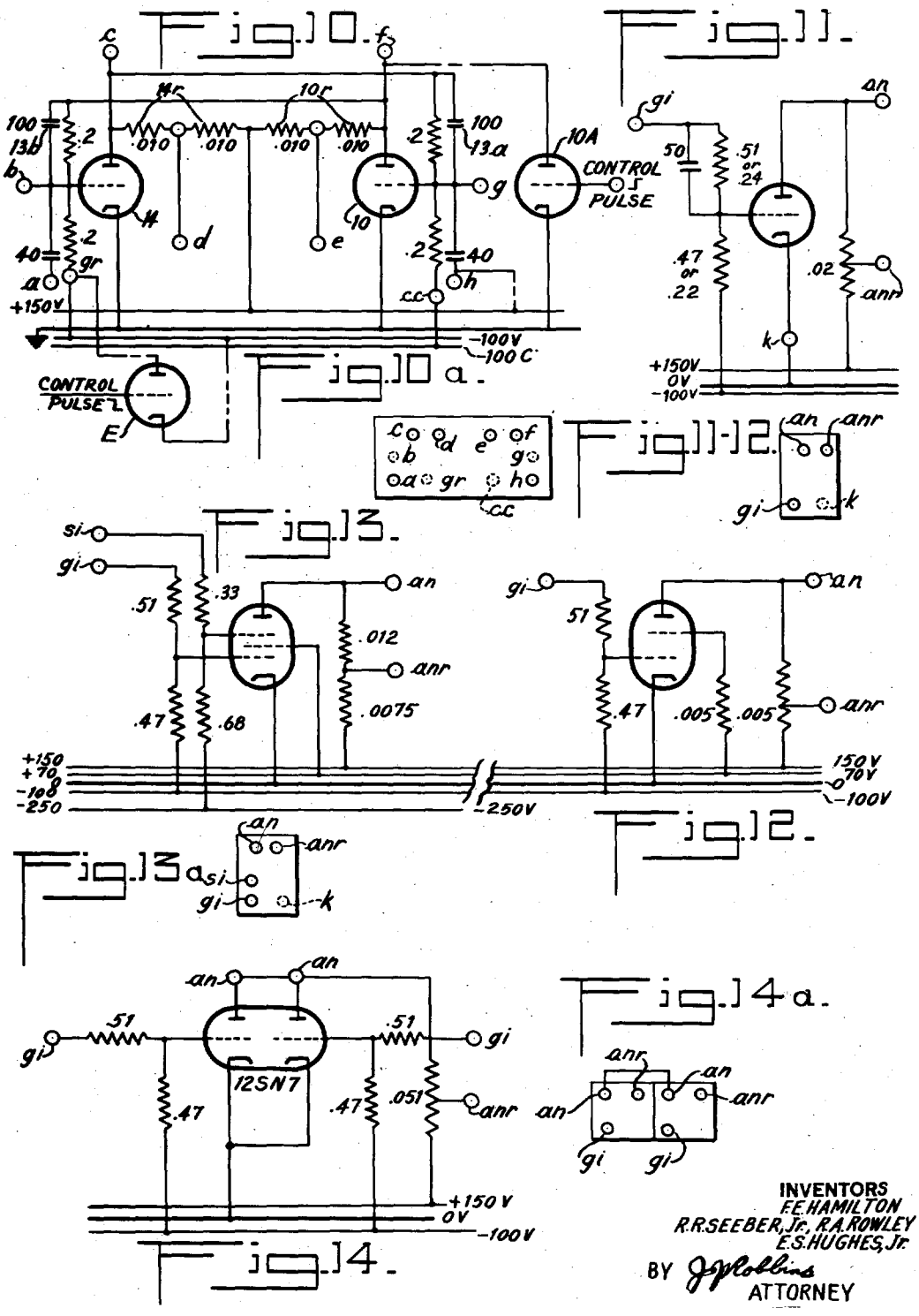

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Fig. 15.

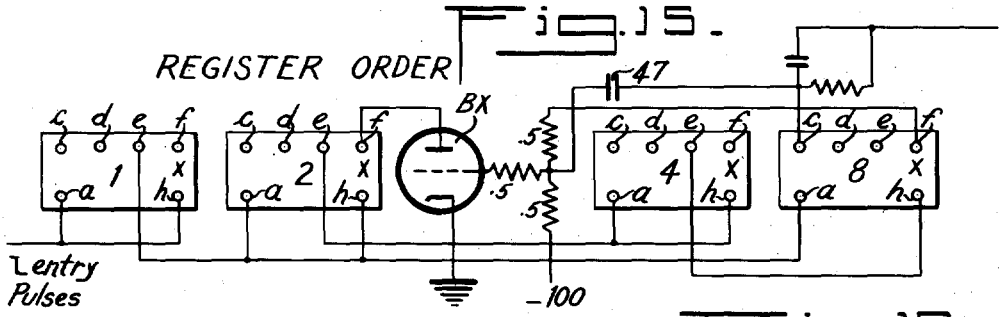
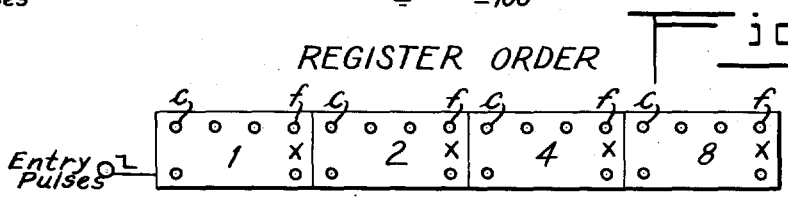


Fig. 15a.



TYPICAL CANCEL CIRCUIT

Fig. 16.

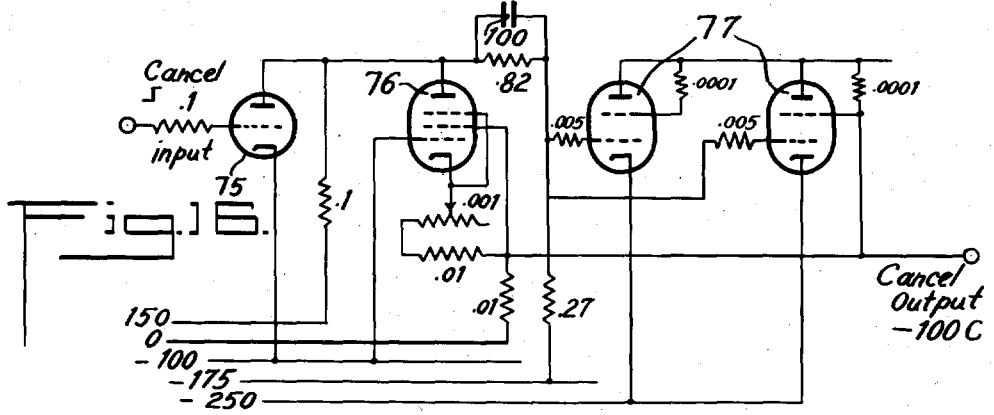
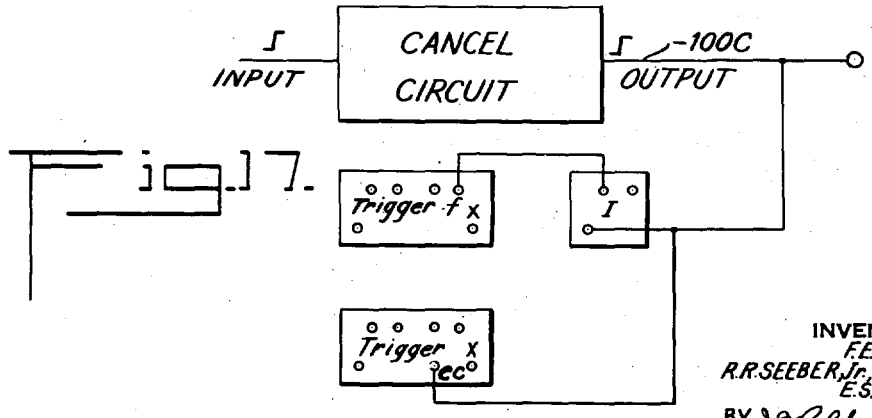


Fig. 17.



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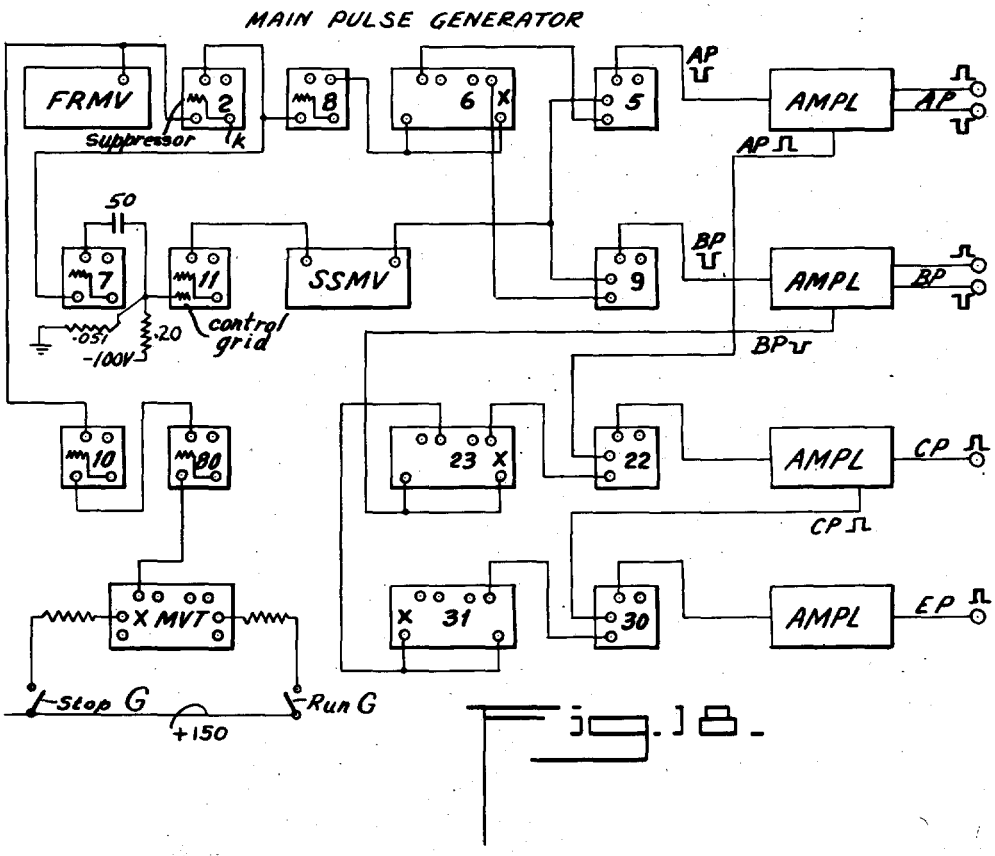

Fig. 18.

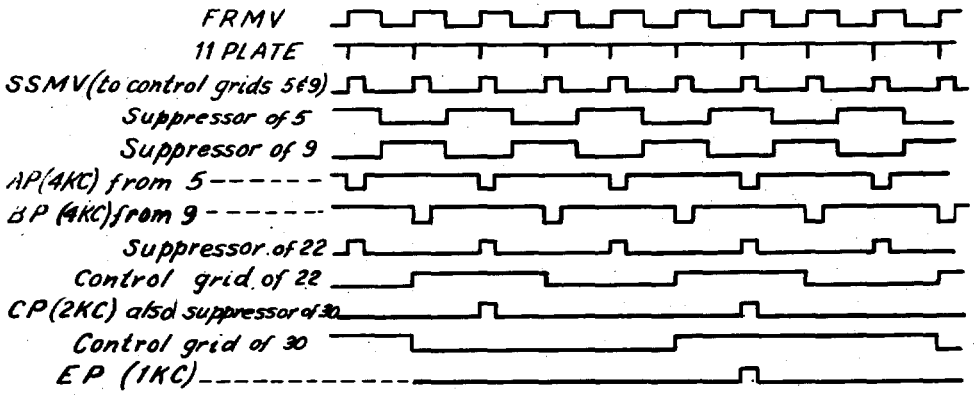

Fig. 19.

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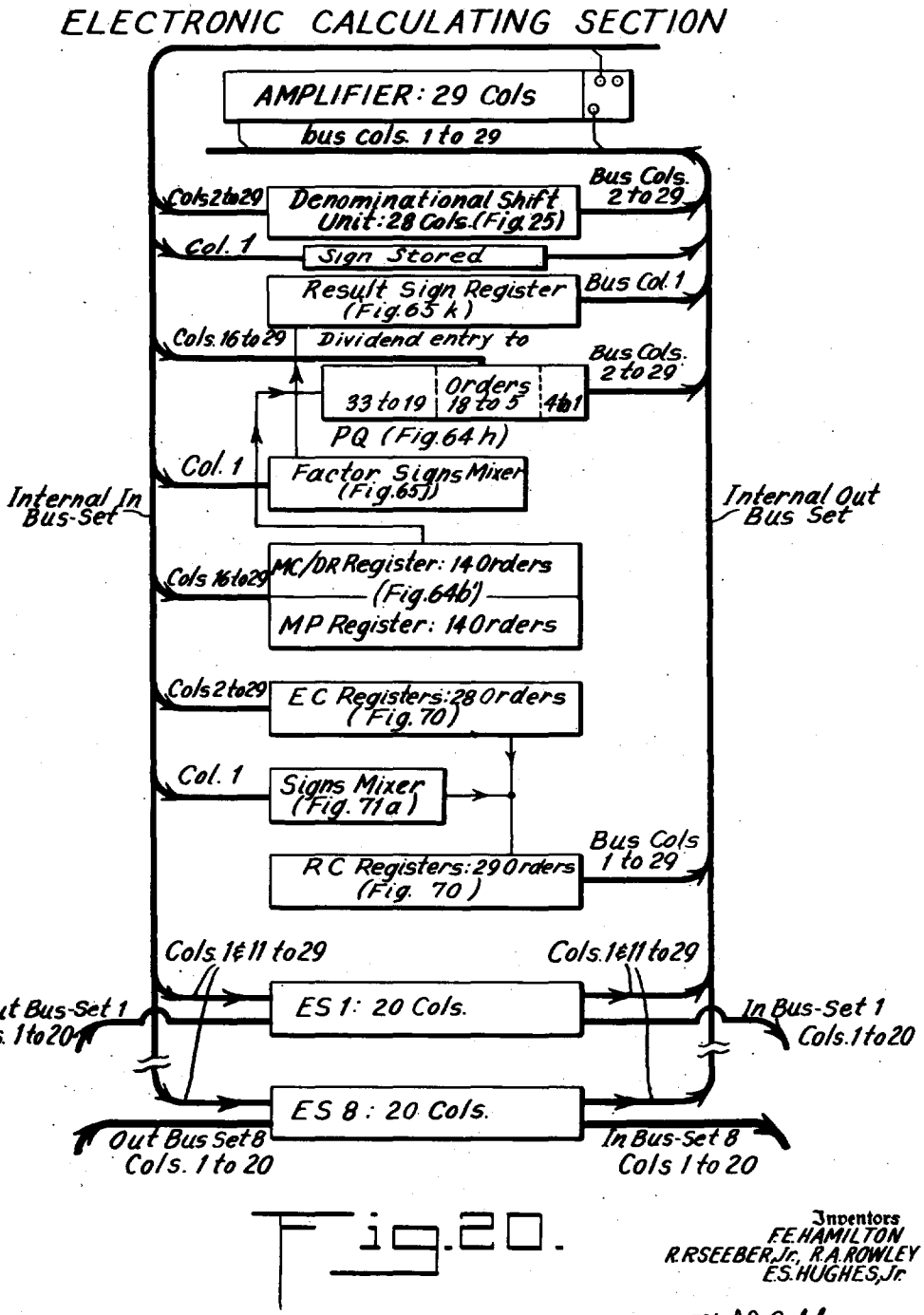

Fig. 20.

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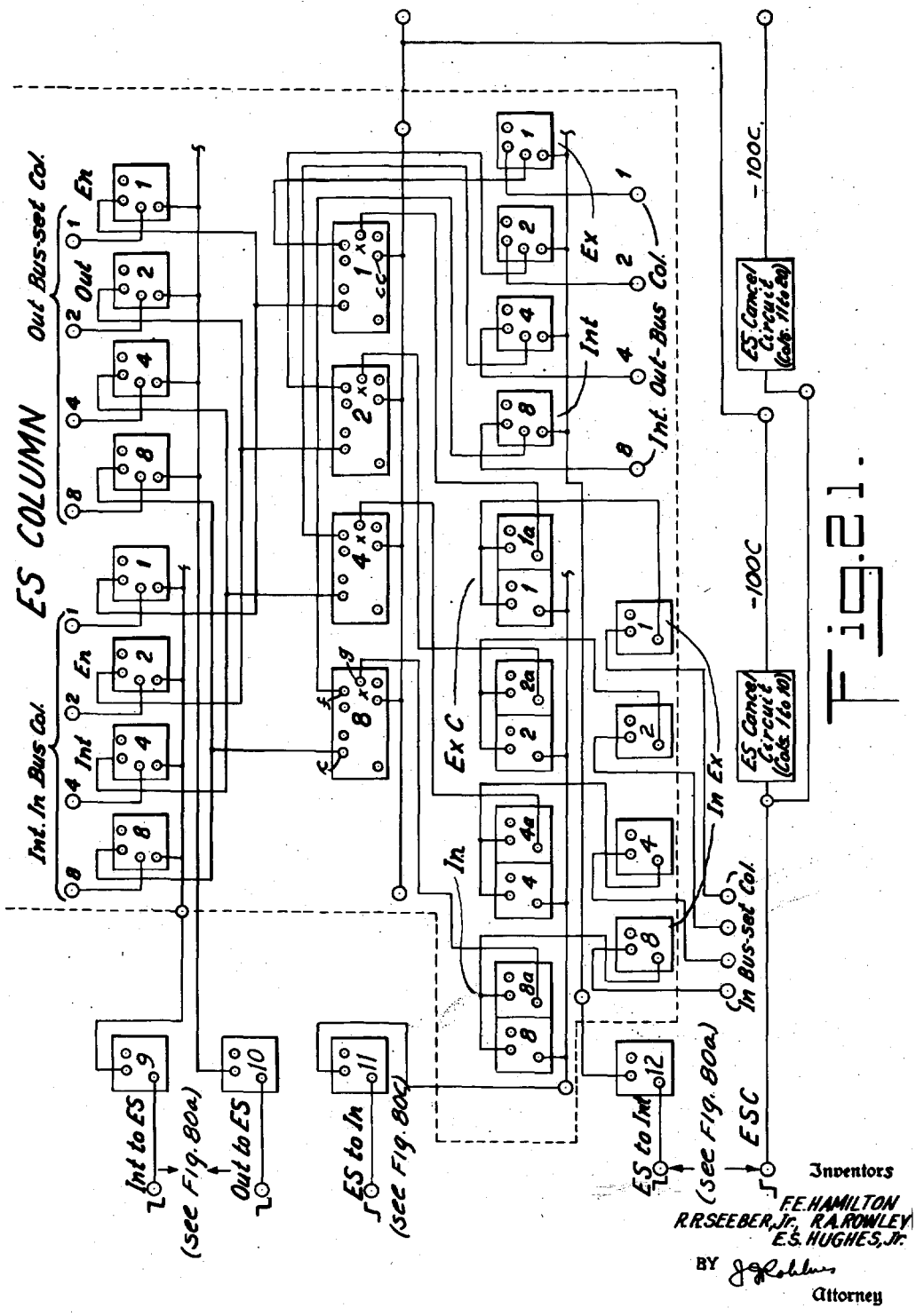

Fig. 21.

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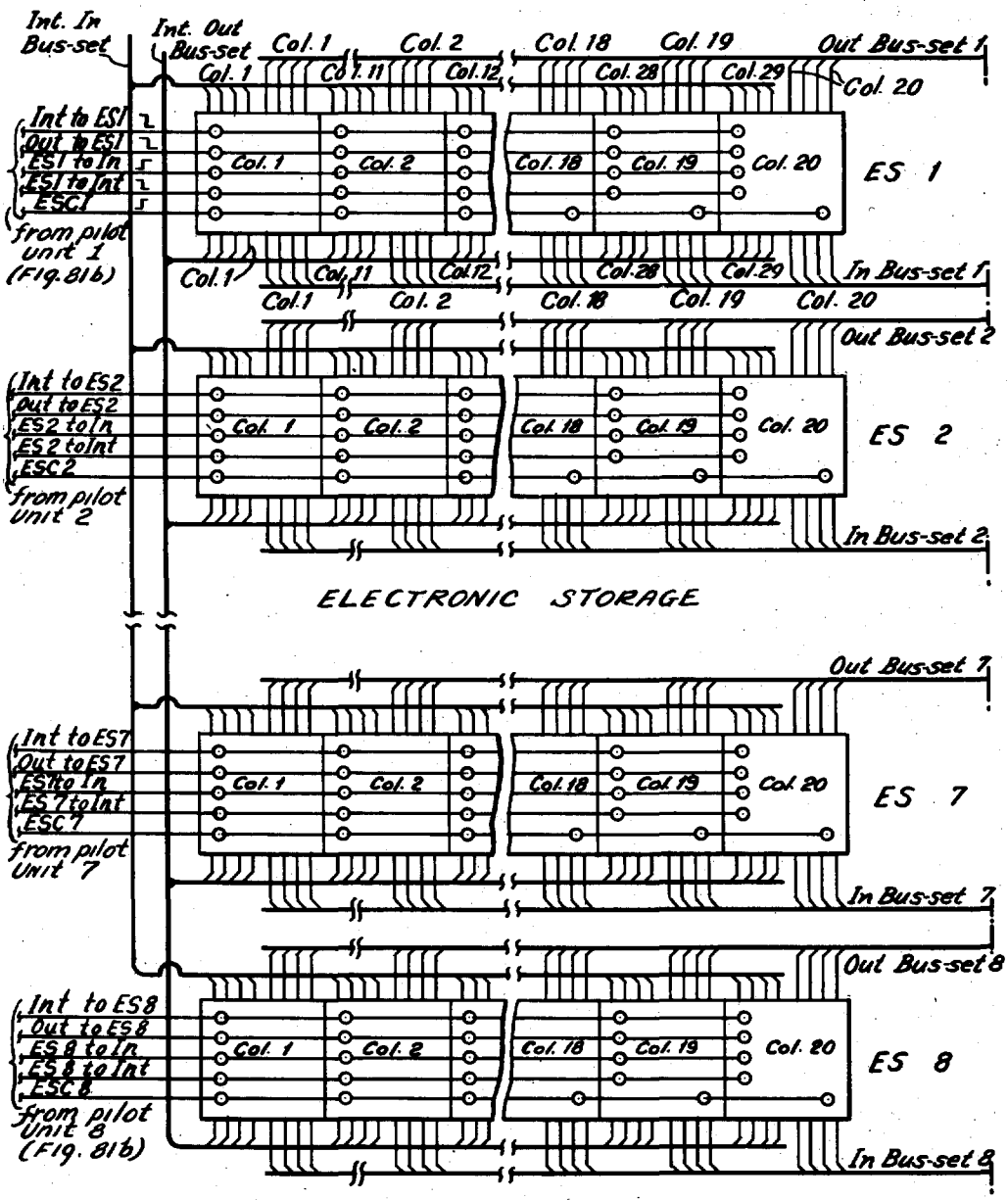

Fig. 22.

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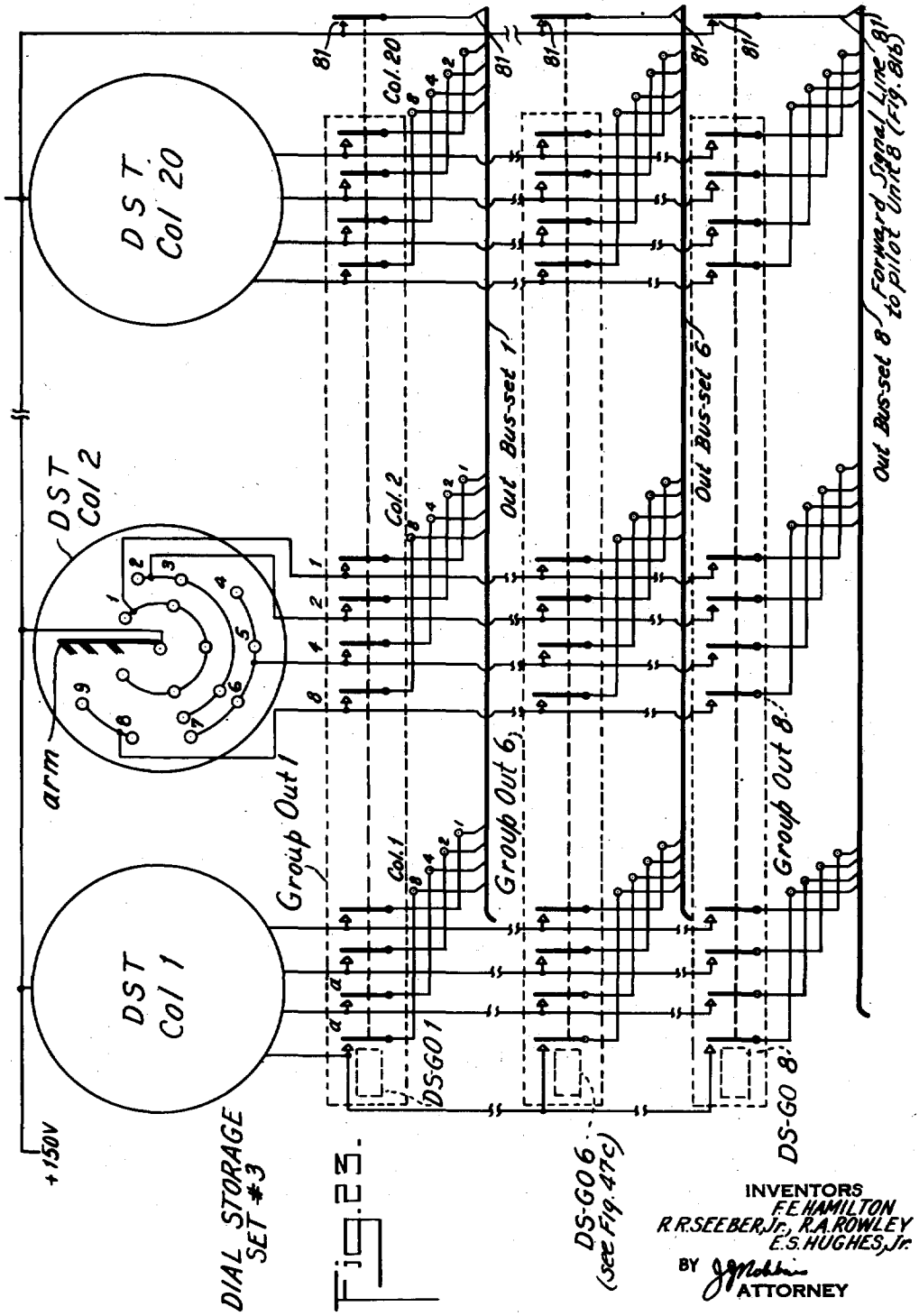

Fig. 23.

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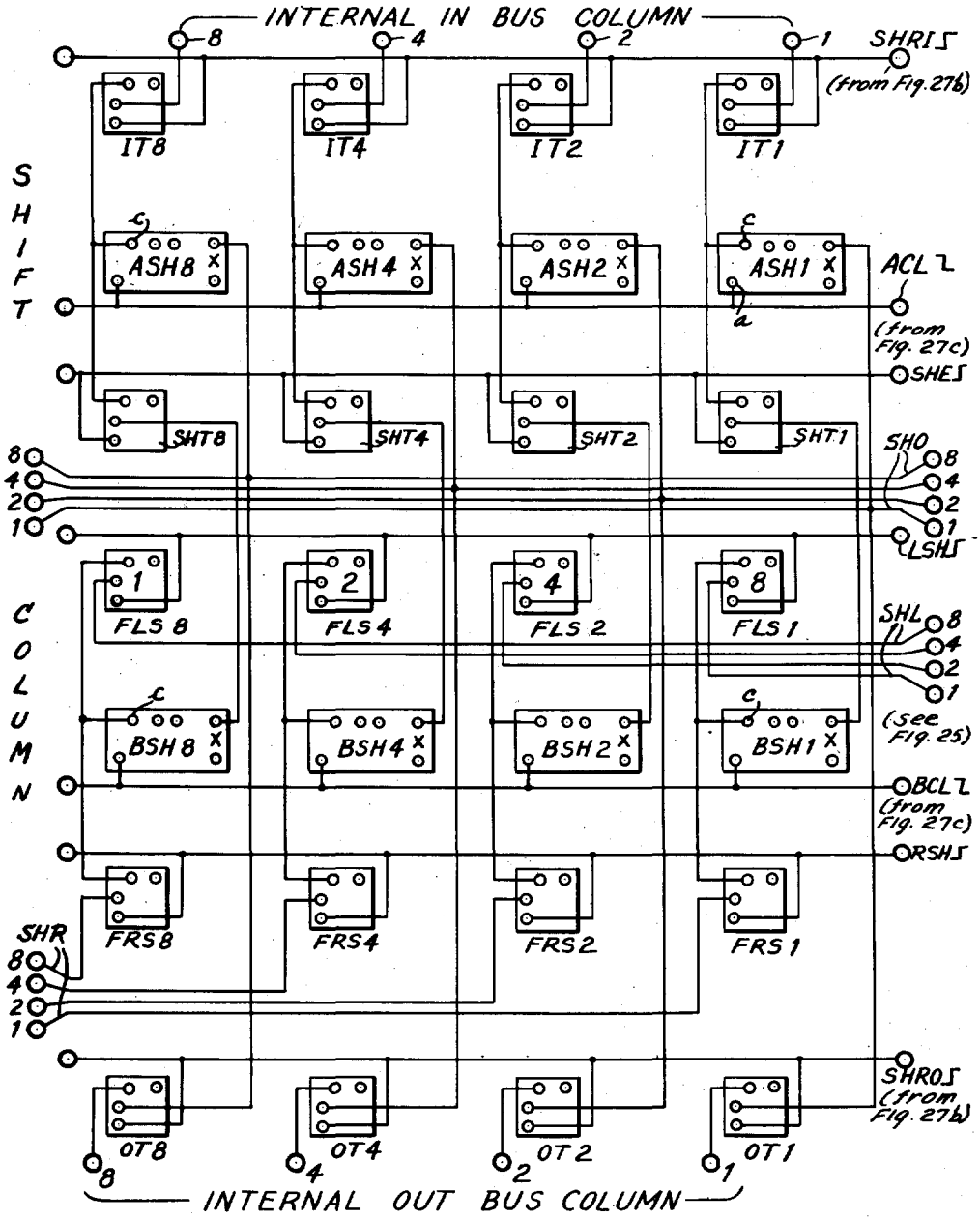

Fig. 24.

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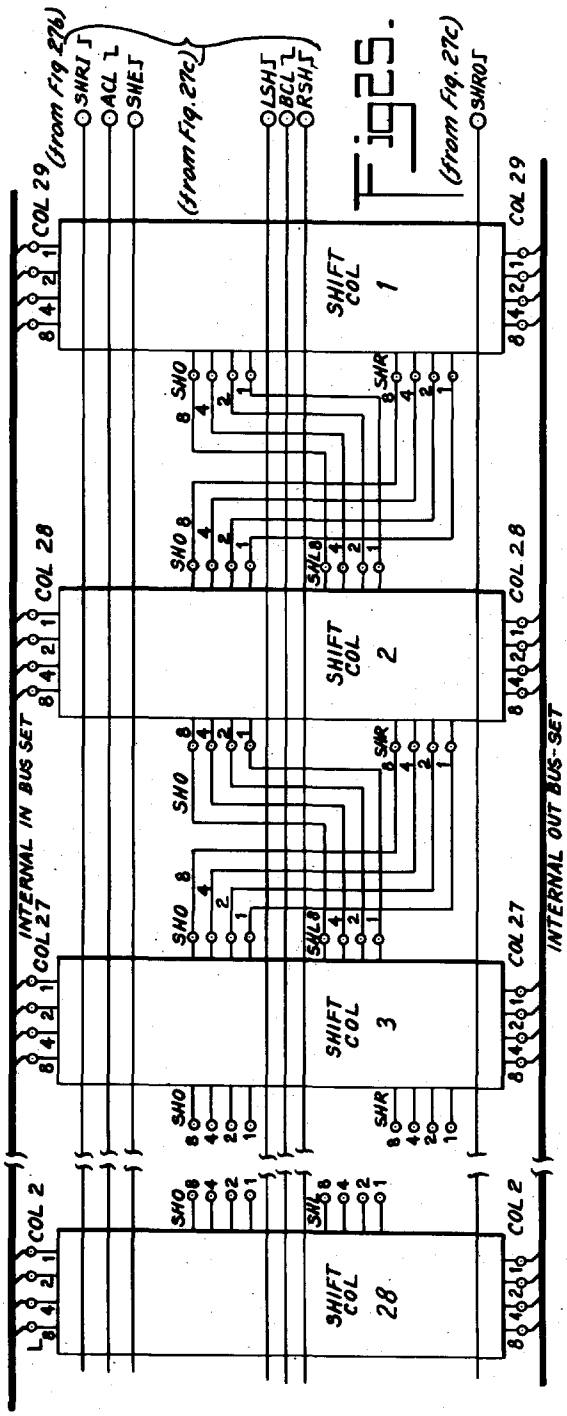

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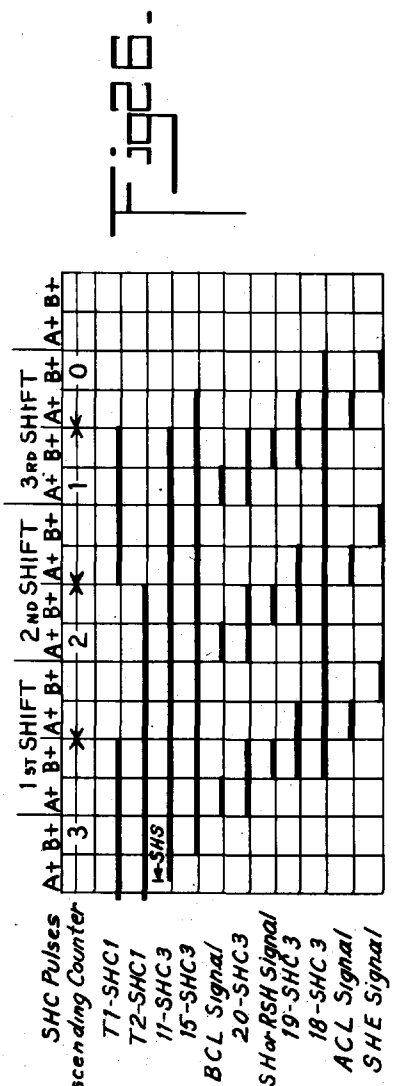

Fig 26.

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SHC 1

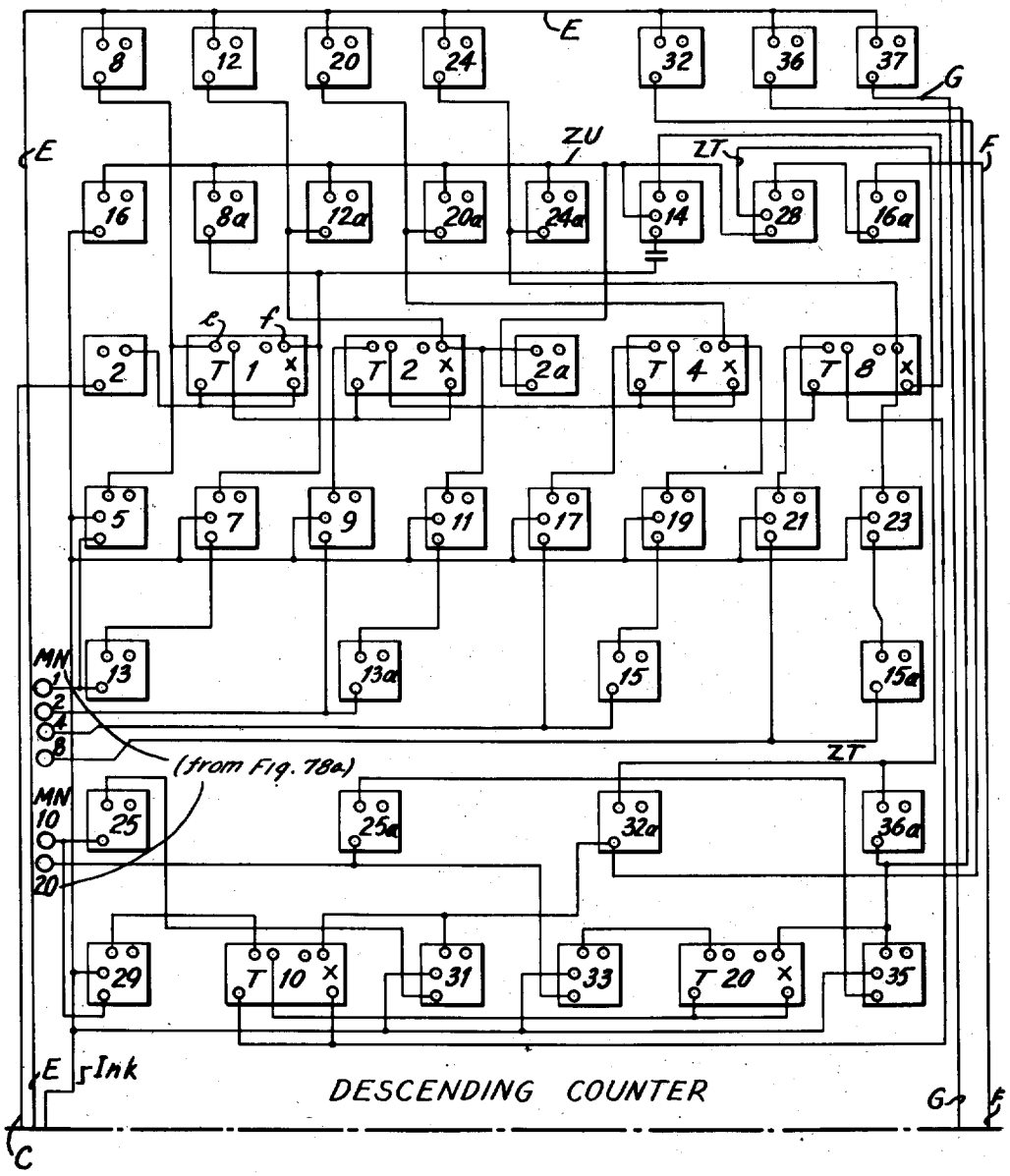

Fig. 27a.

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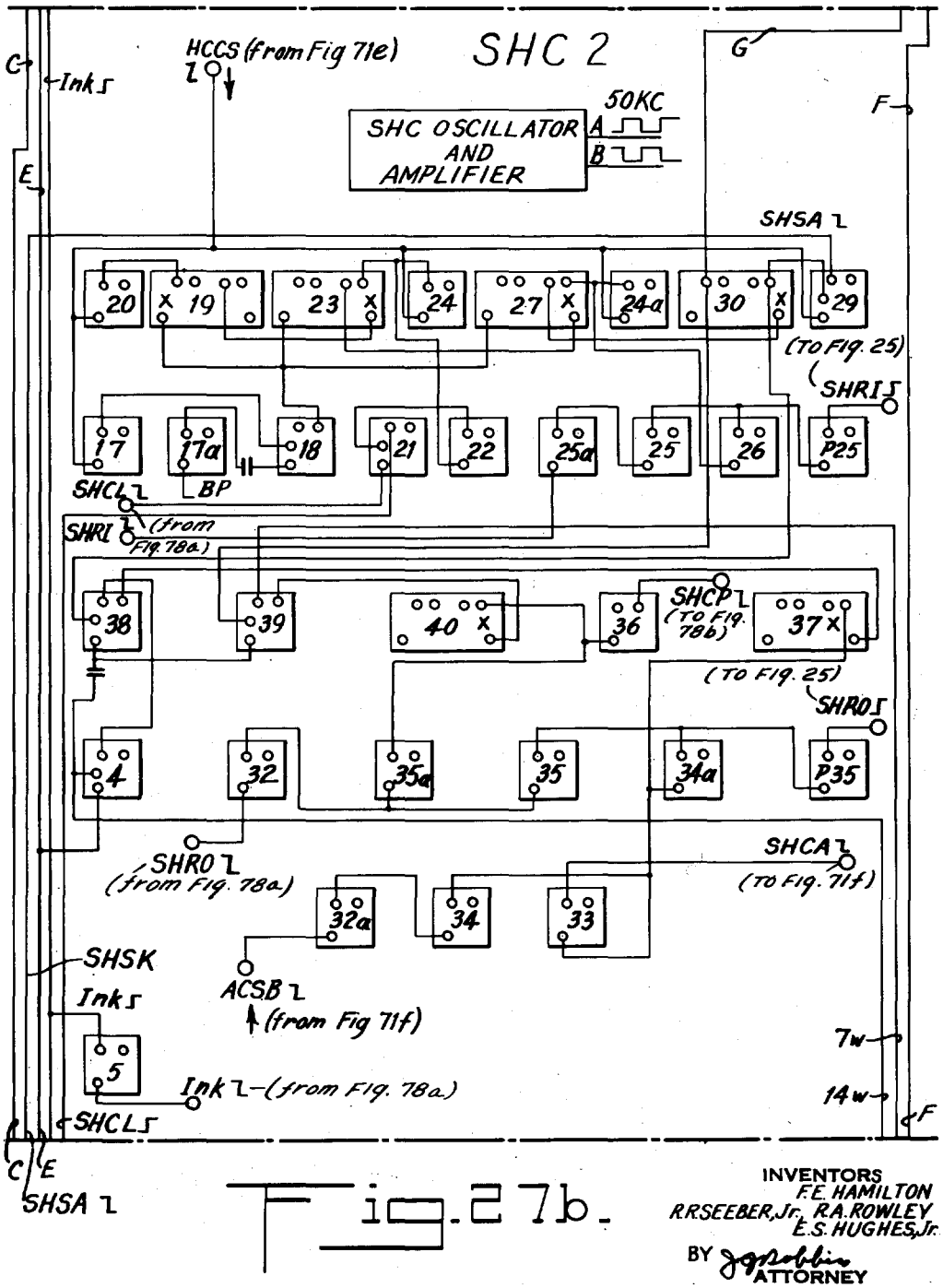

Fig. 27b.

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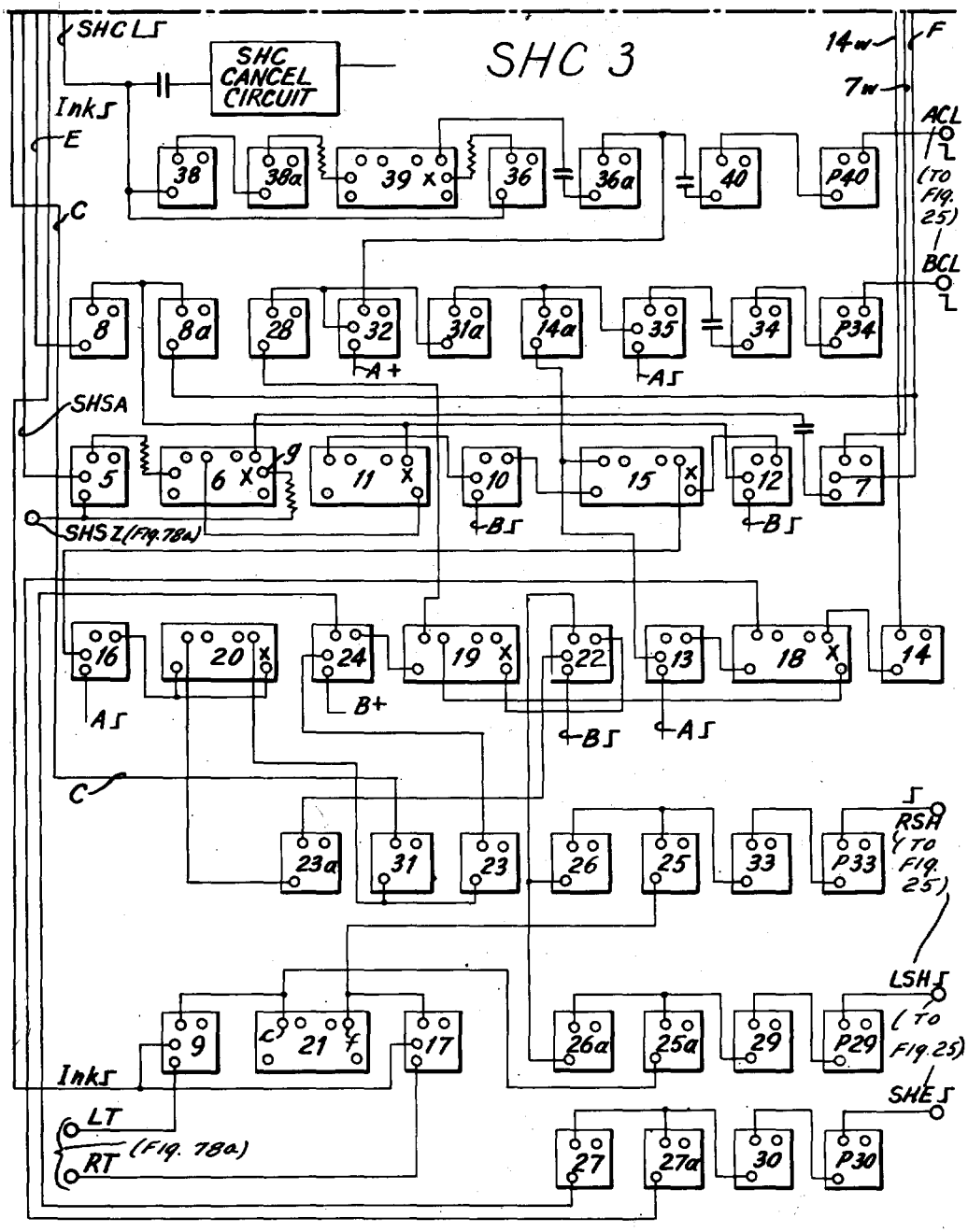

Fig. 27c.

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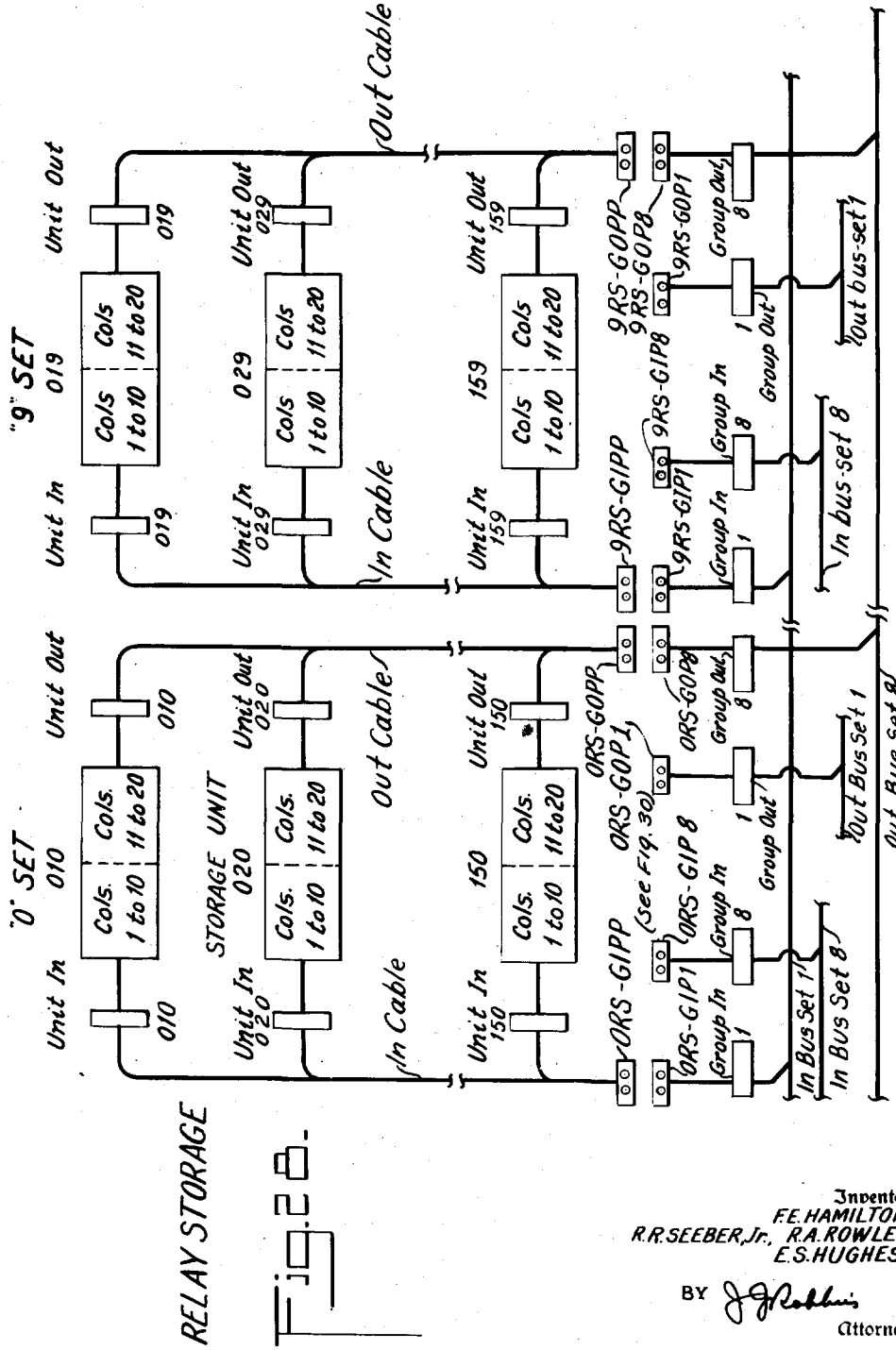

RELAY STORAGE

Fig. 28.

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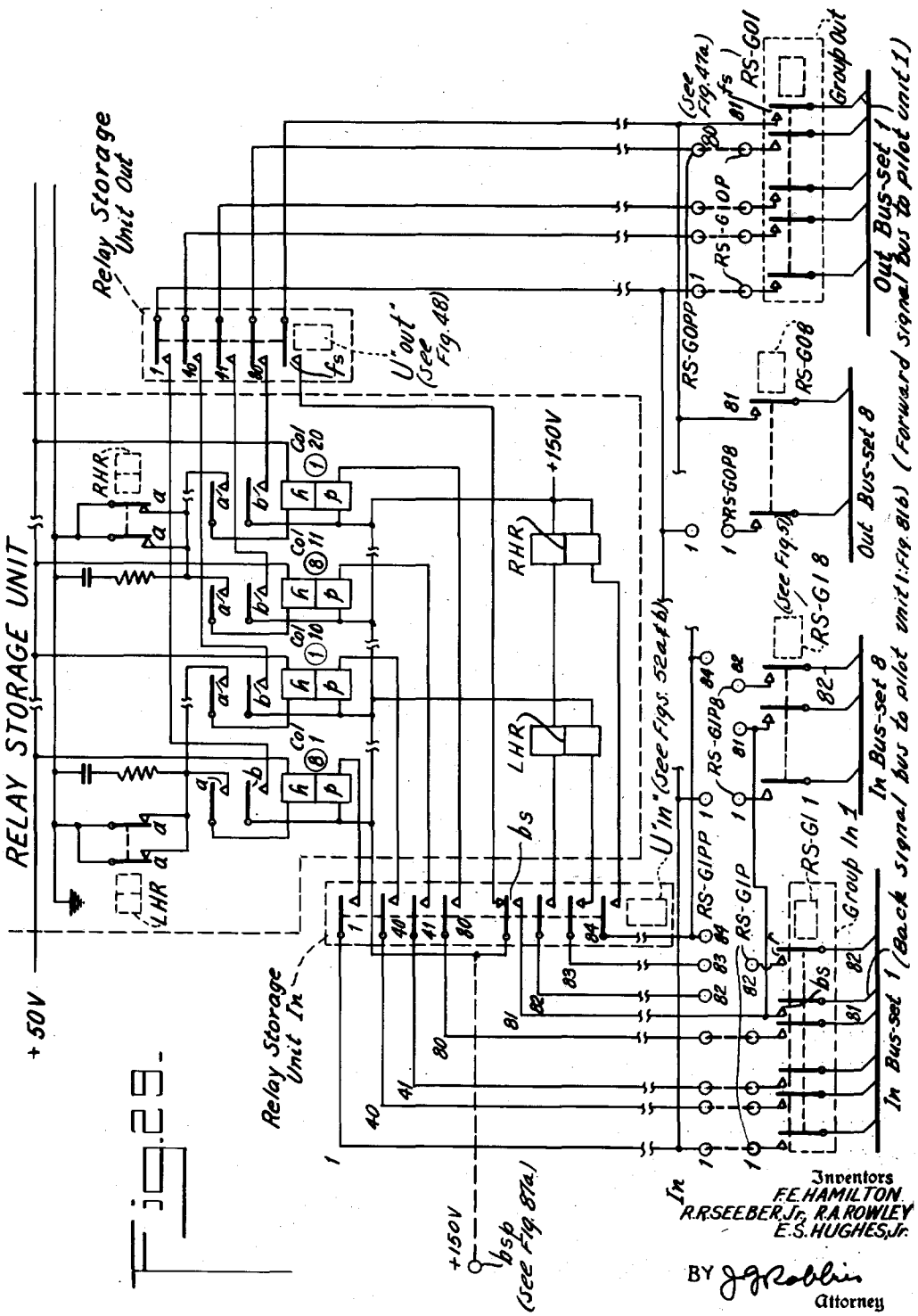

Fig. 29.

Inventors
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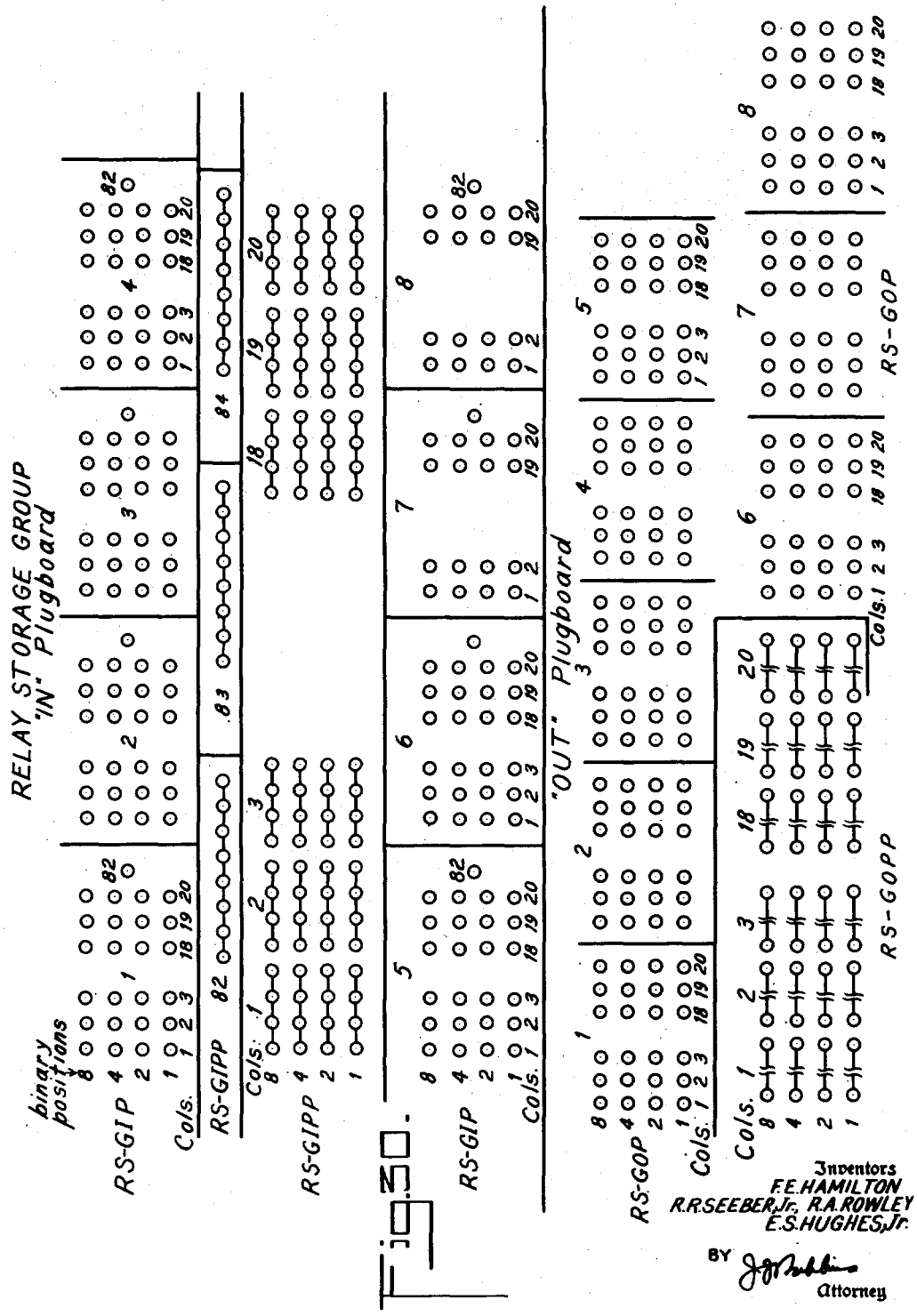

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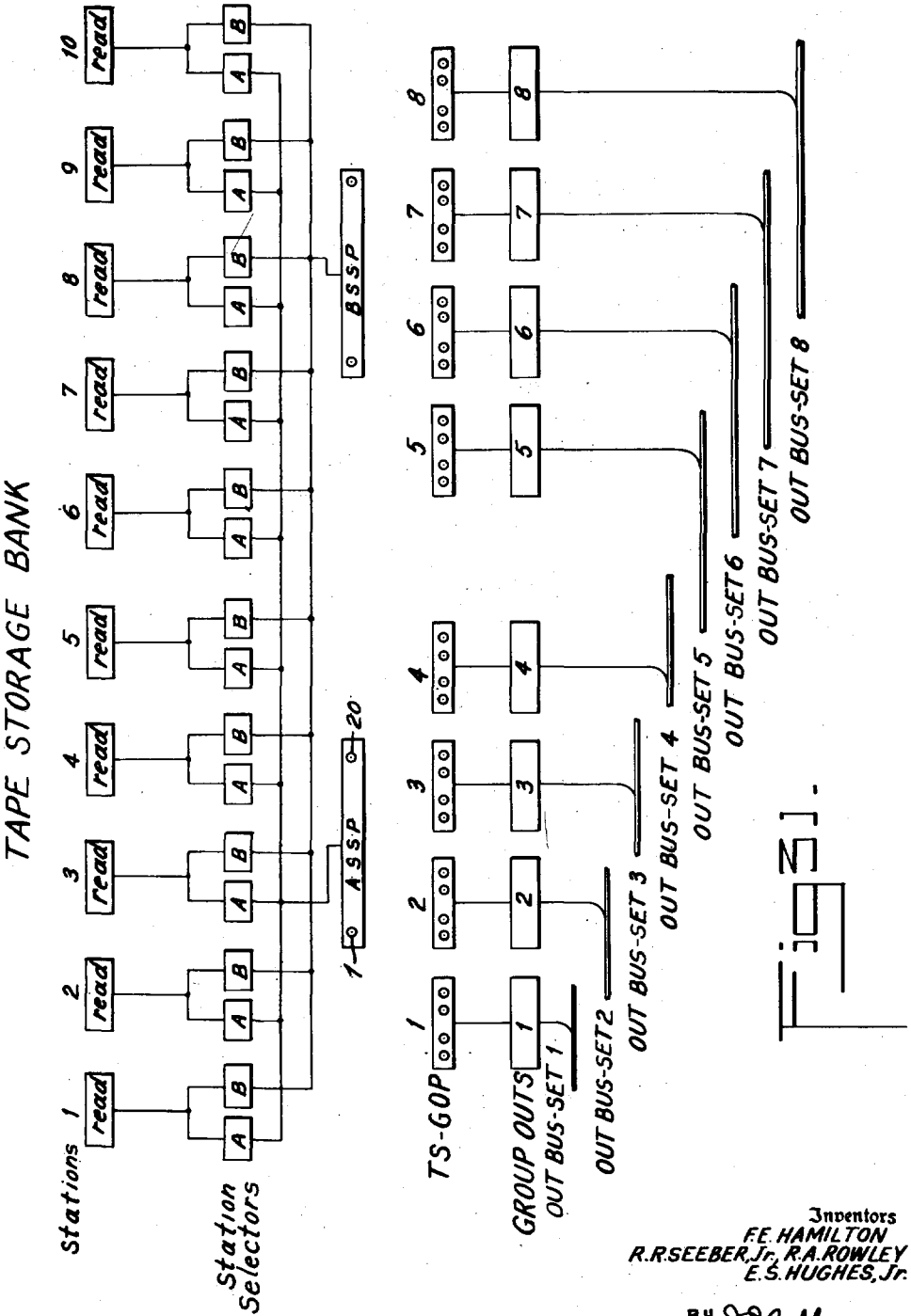

FIG. 1.

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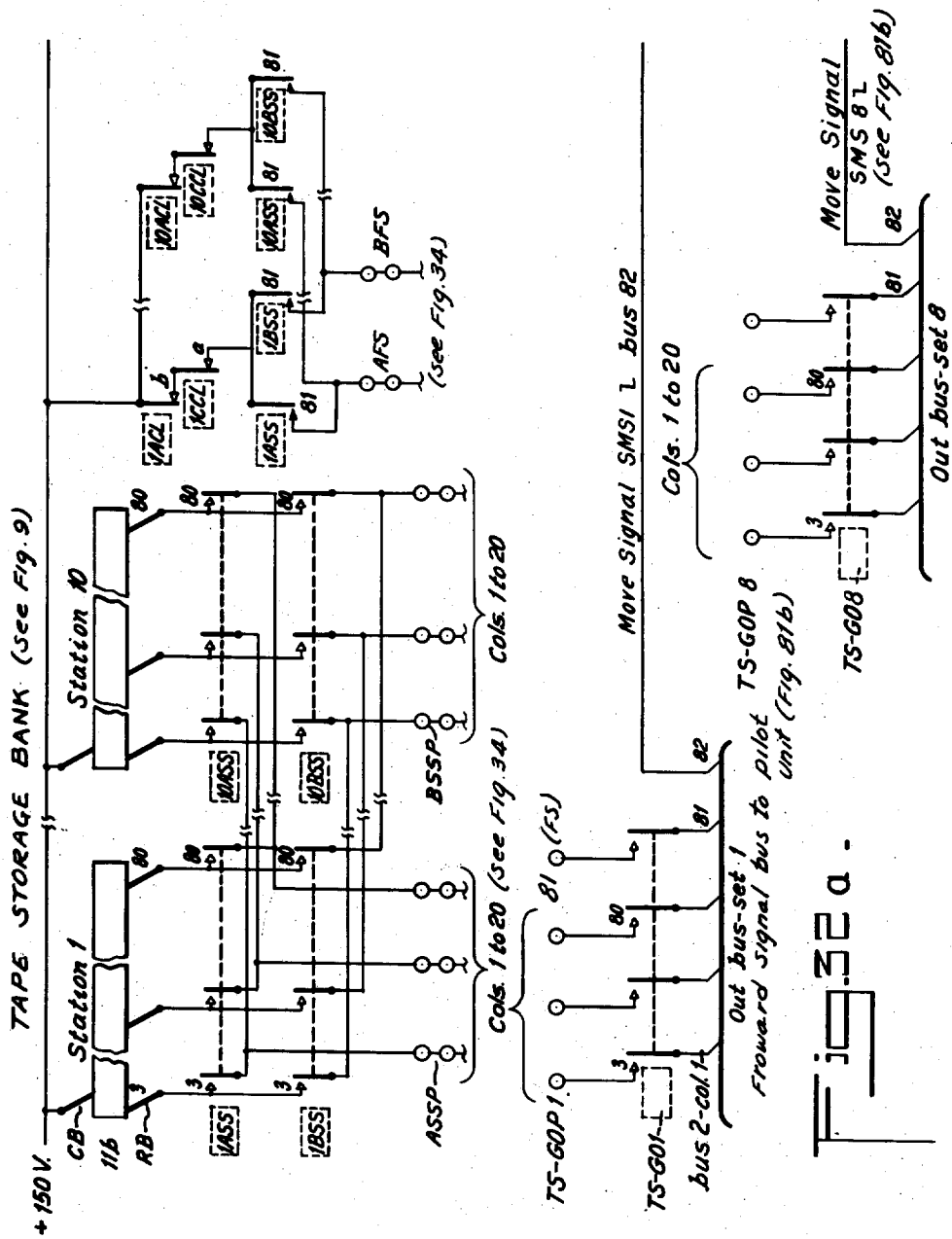

Fig. 32a.

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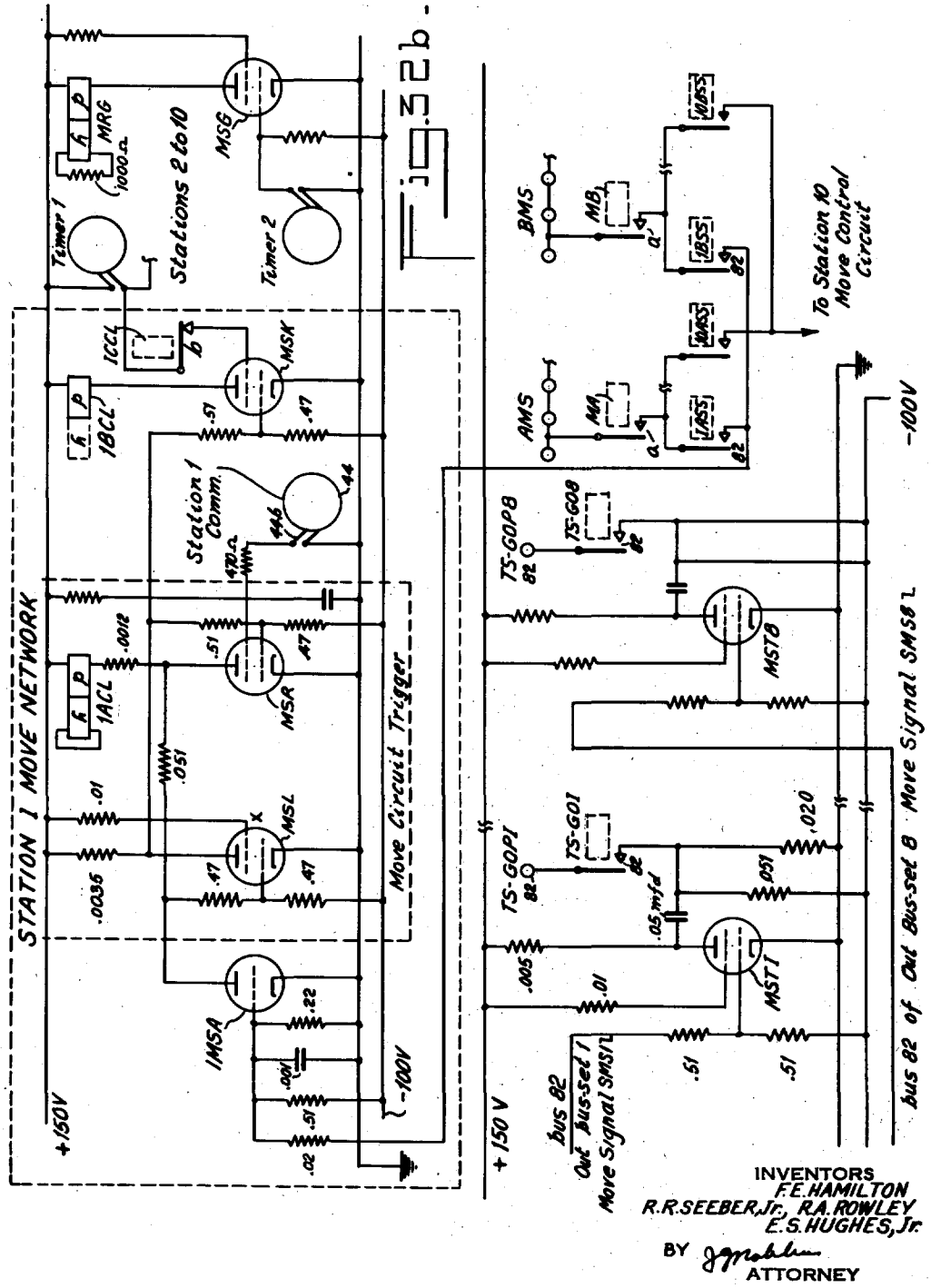

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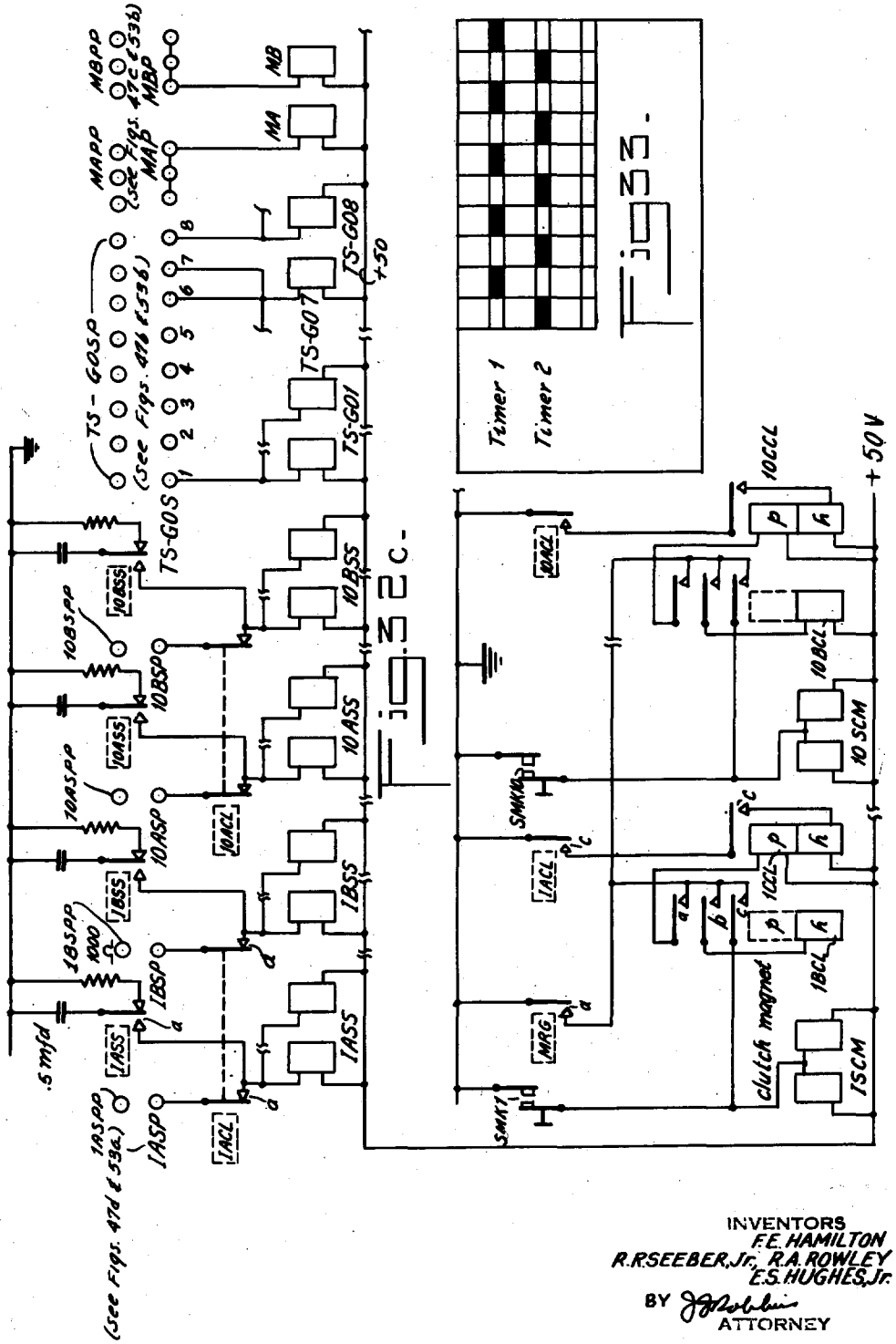

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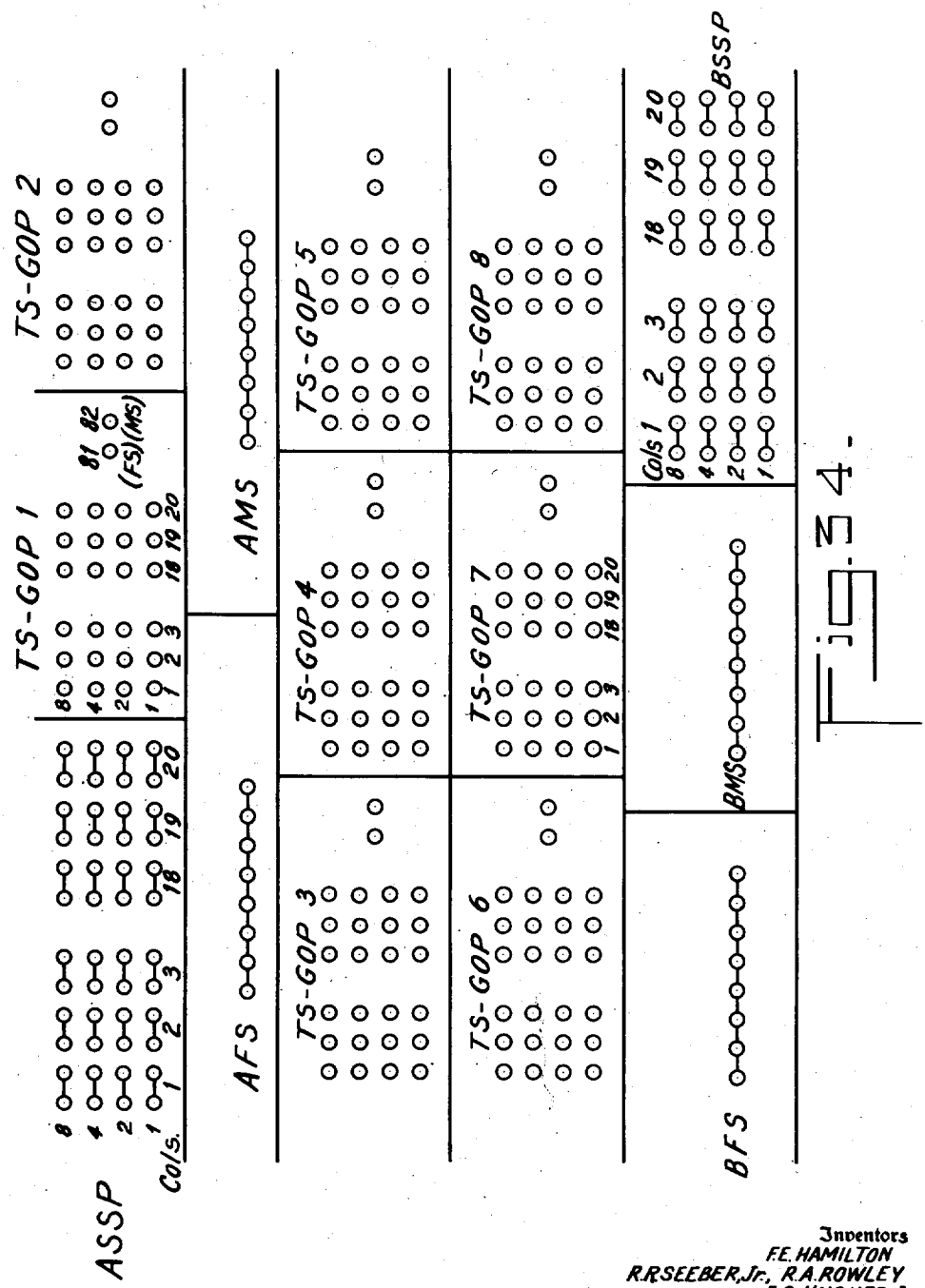

Fig. 4.

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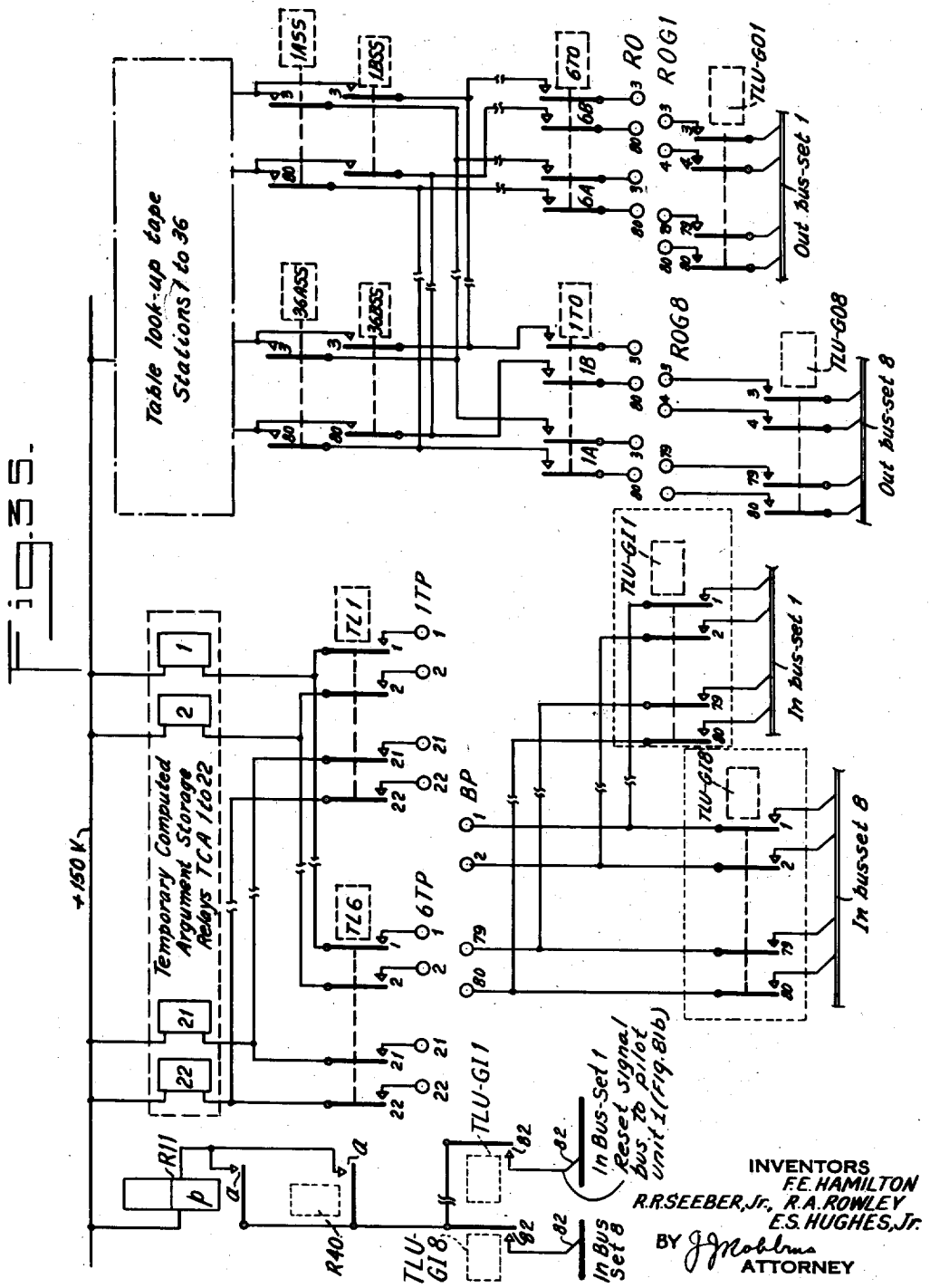

Fig. 135.

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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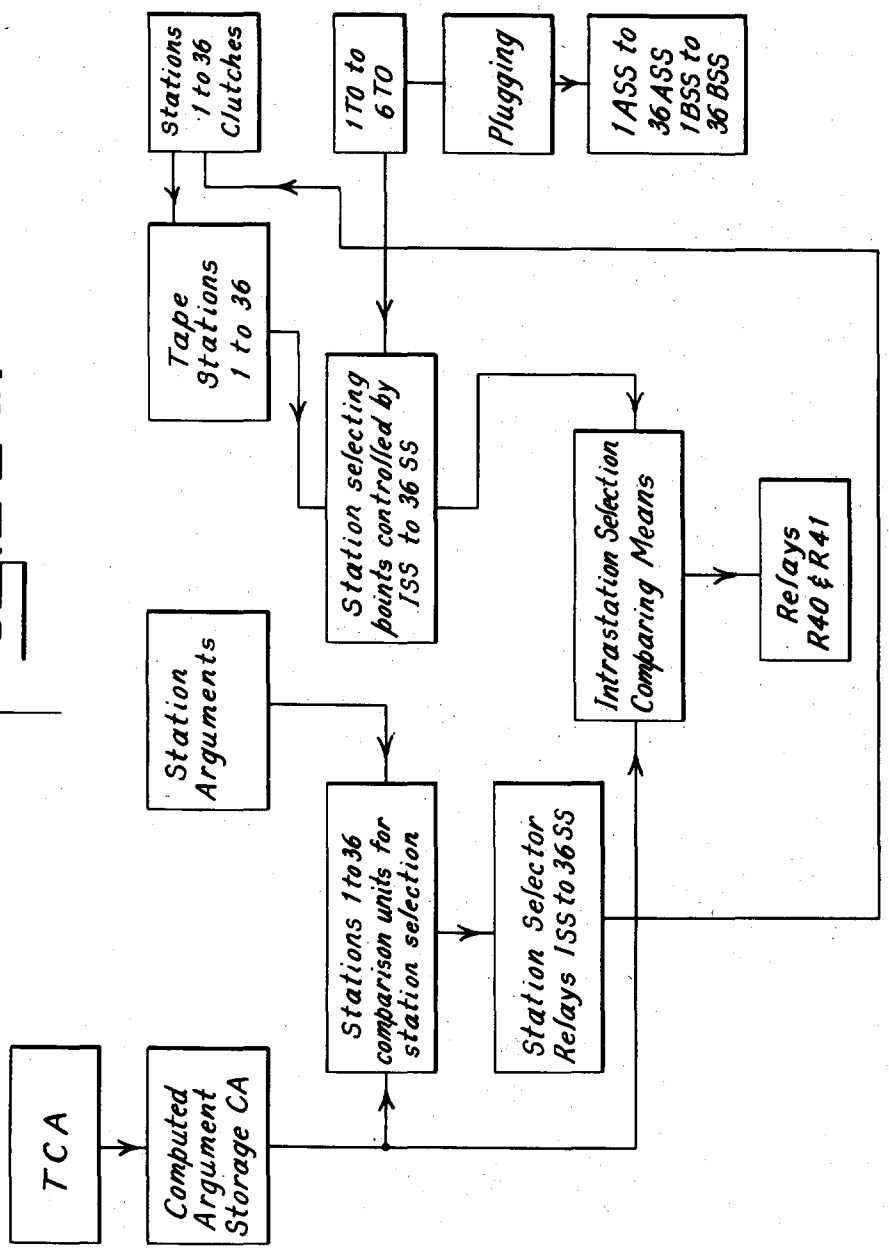
Fig. 35a.



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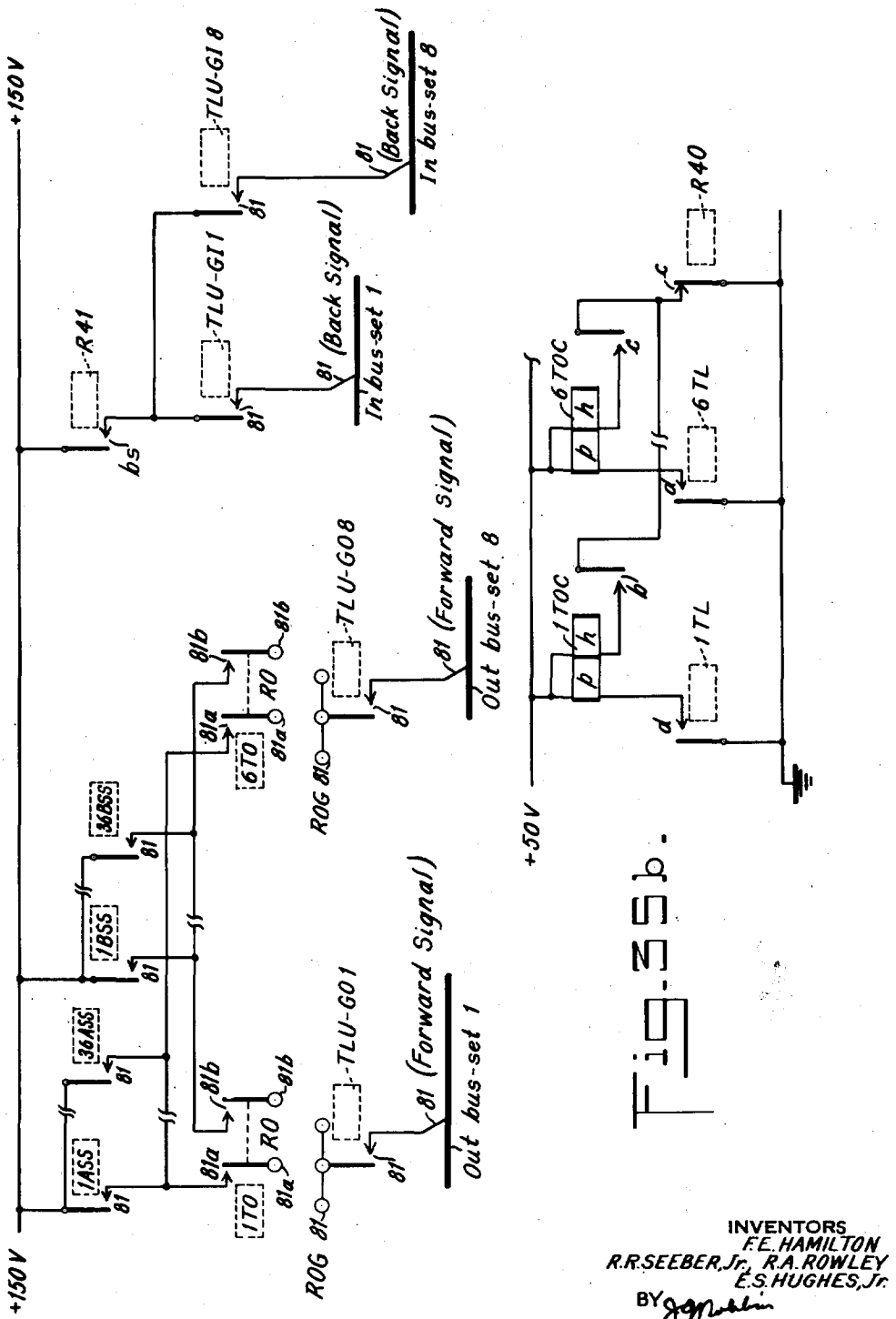

Fig. 15b.

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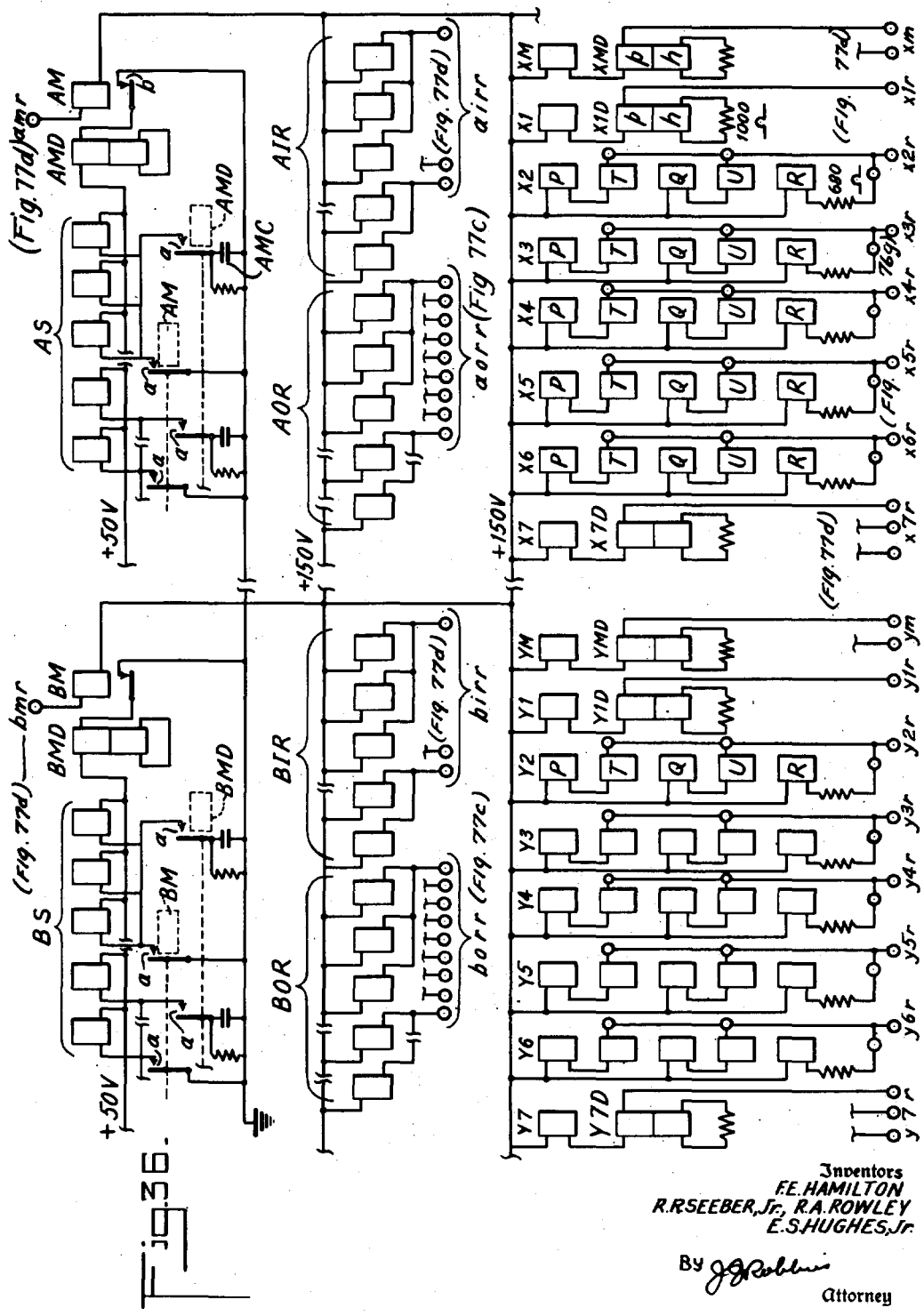

Fig. 36.

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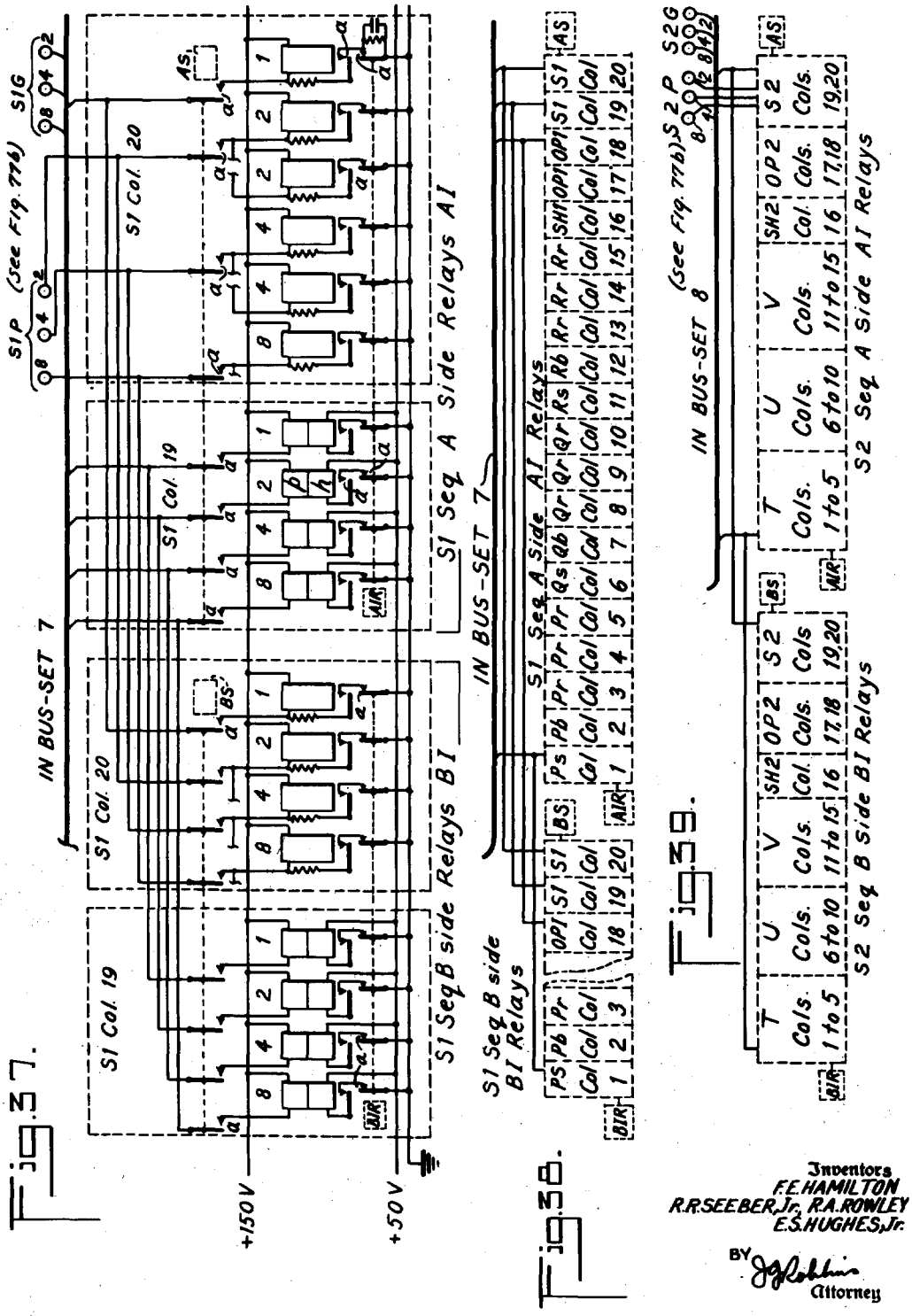

Fig. 37.

Fig. 38.

Fig. 39.

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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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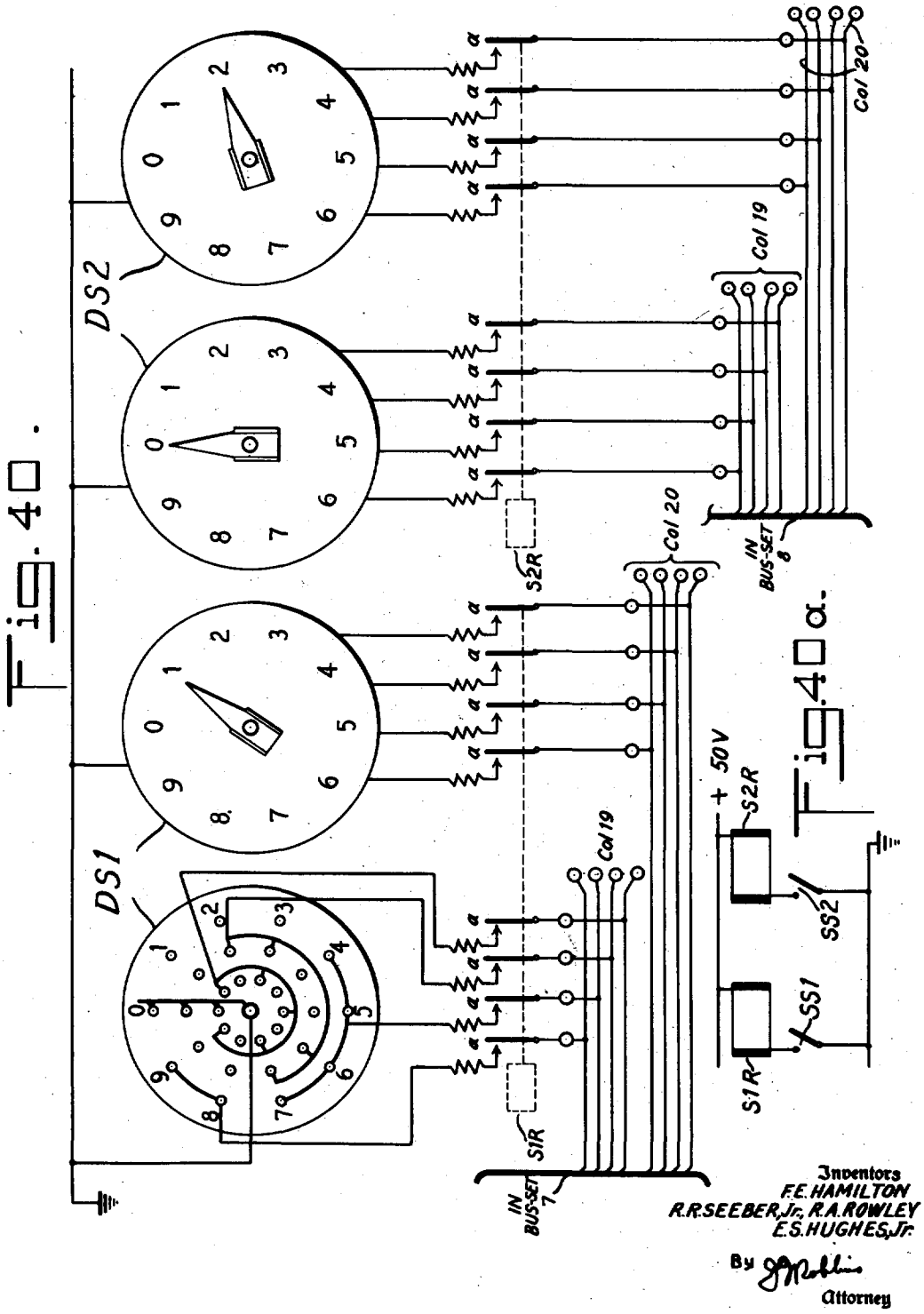

Fig. 40.

Fig. 40a.

Inventors
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By J. Mahlin
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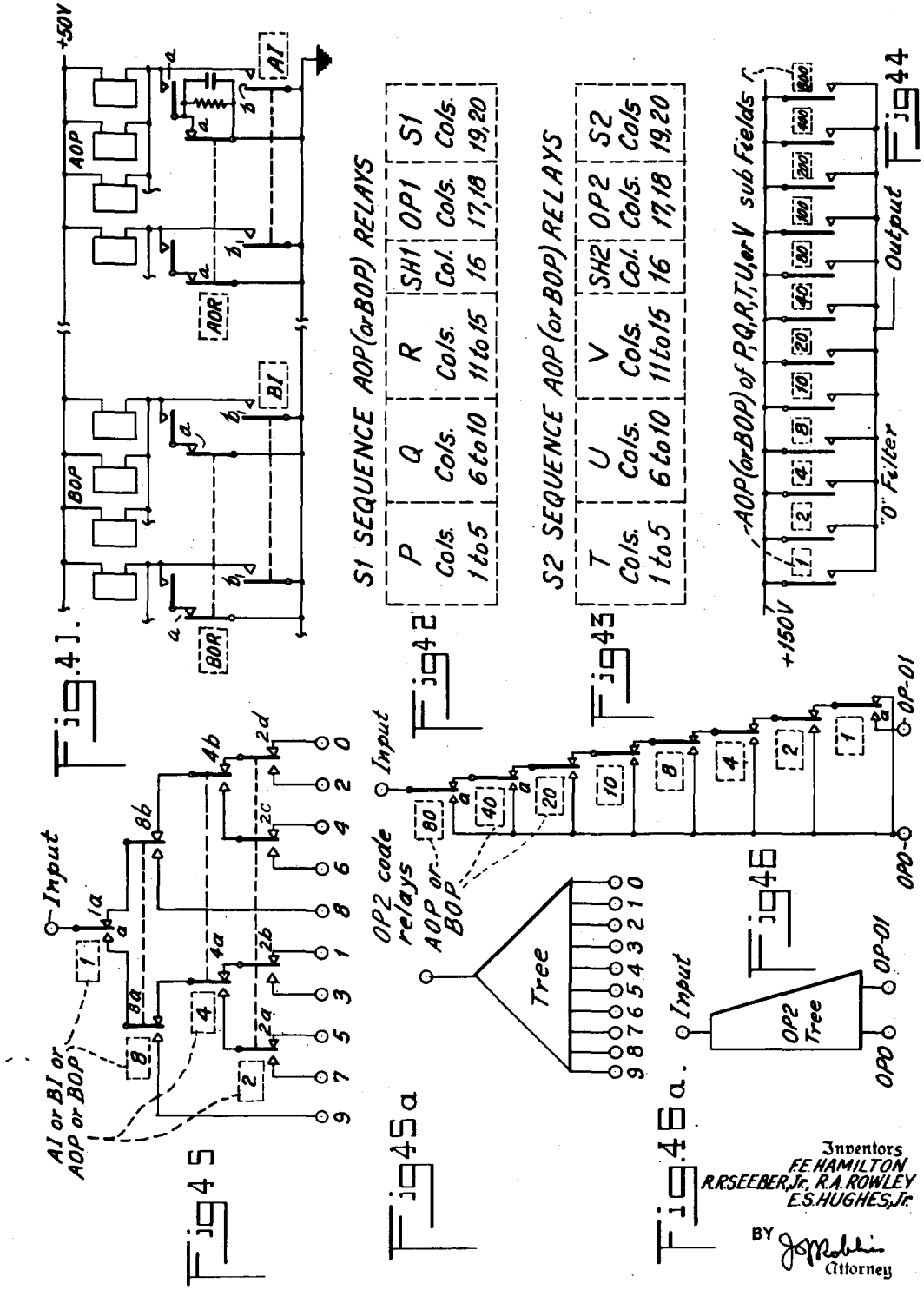

Inventors
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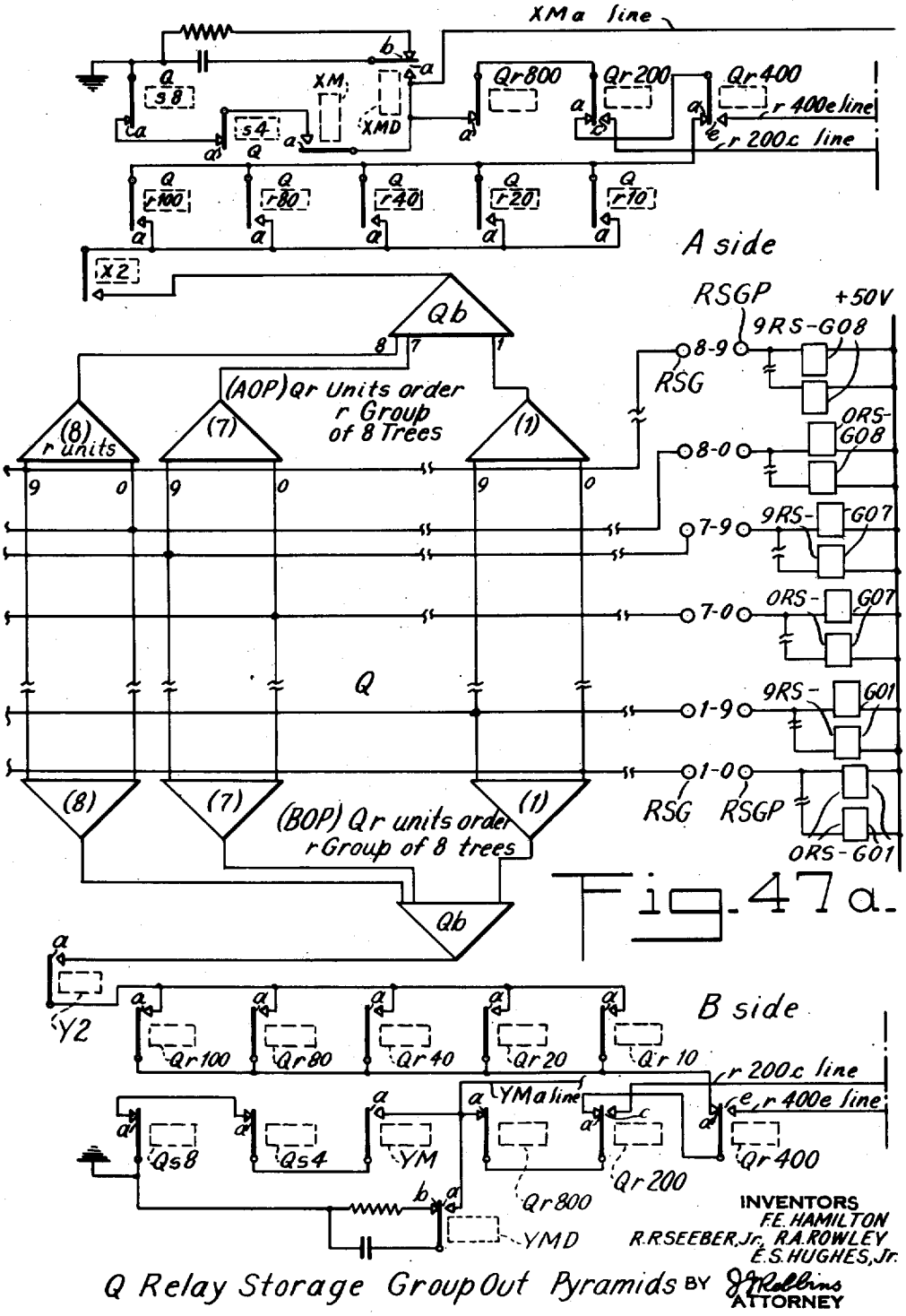

Fig. 47a.

Q Relay Storage Group Out Pyramids

INVENTORS
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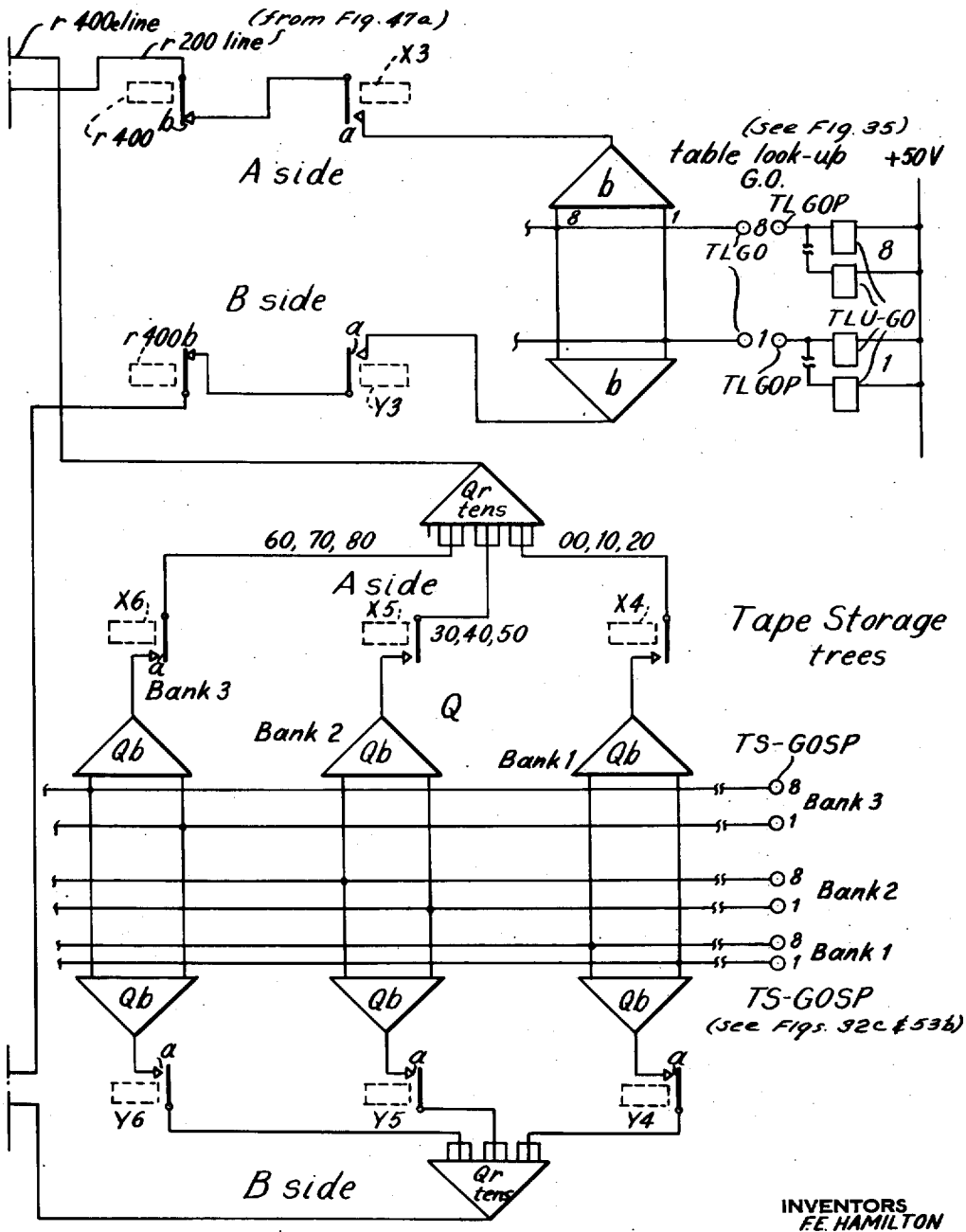

Fig. 47b.

INVENTORS
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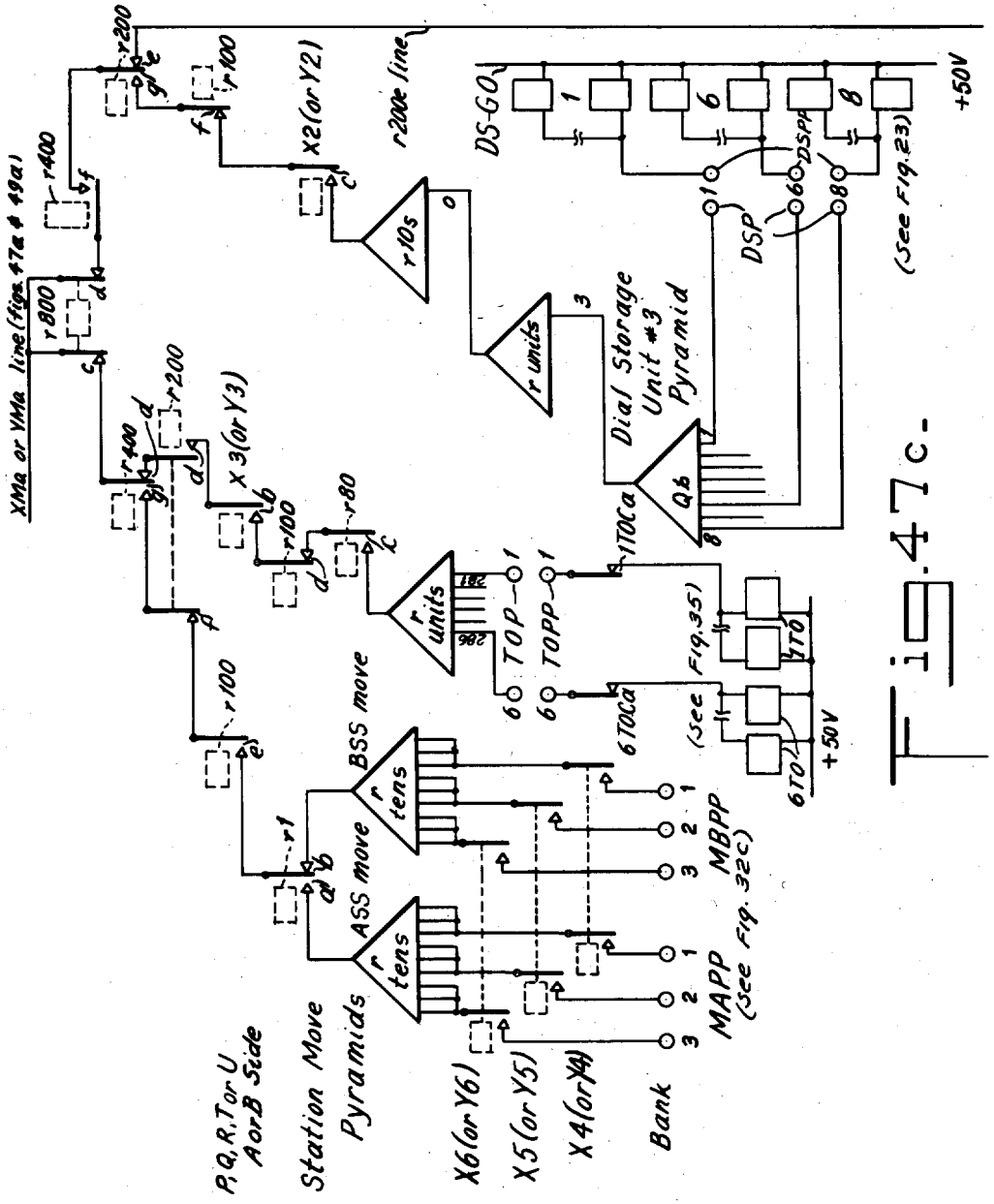

Fig. 47c.

INVENTORS
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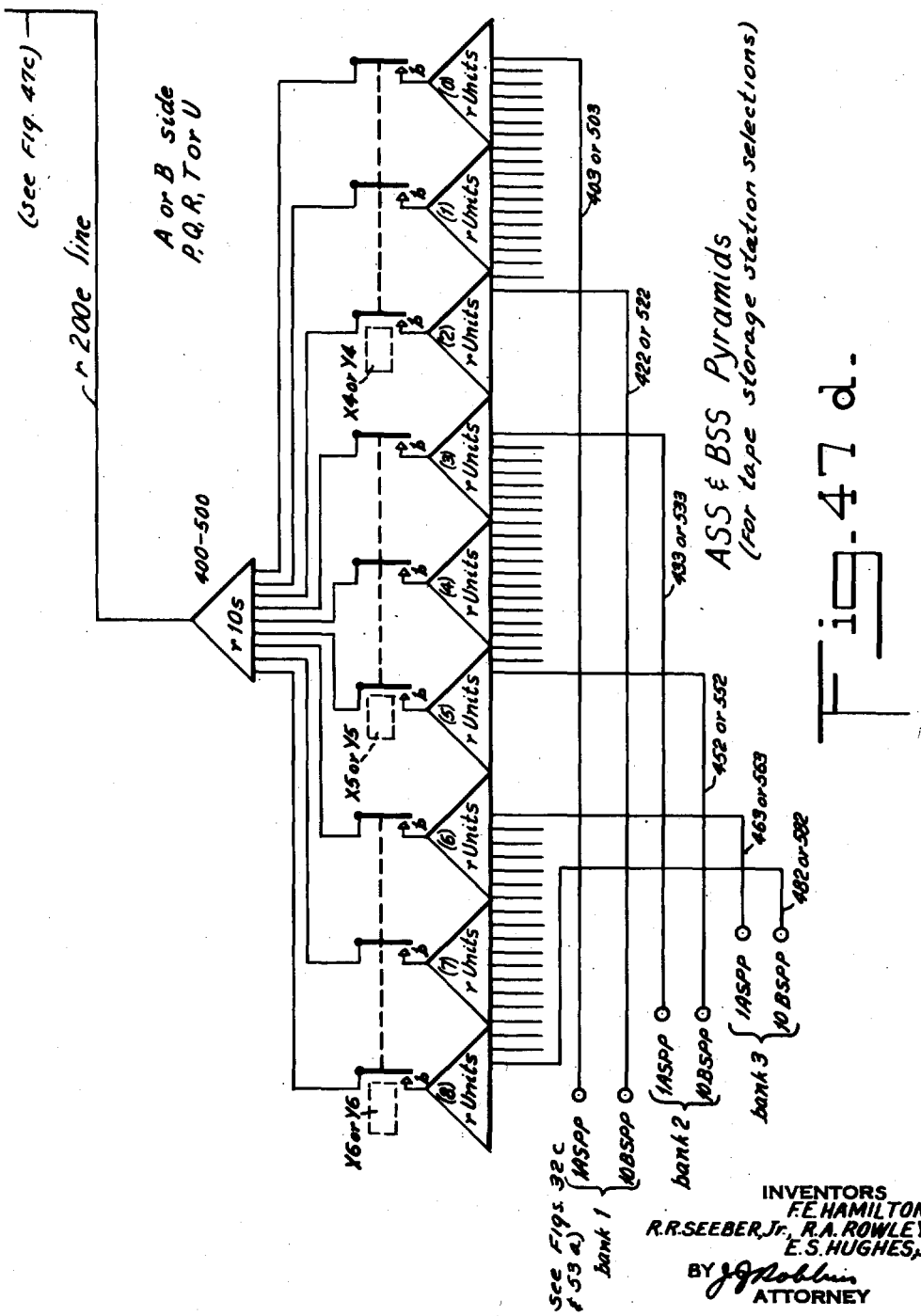

Fig. 47d.

INVENTORS
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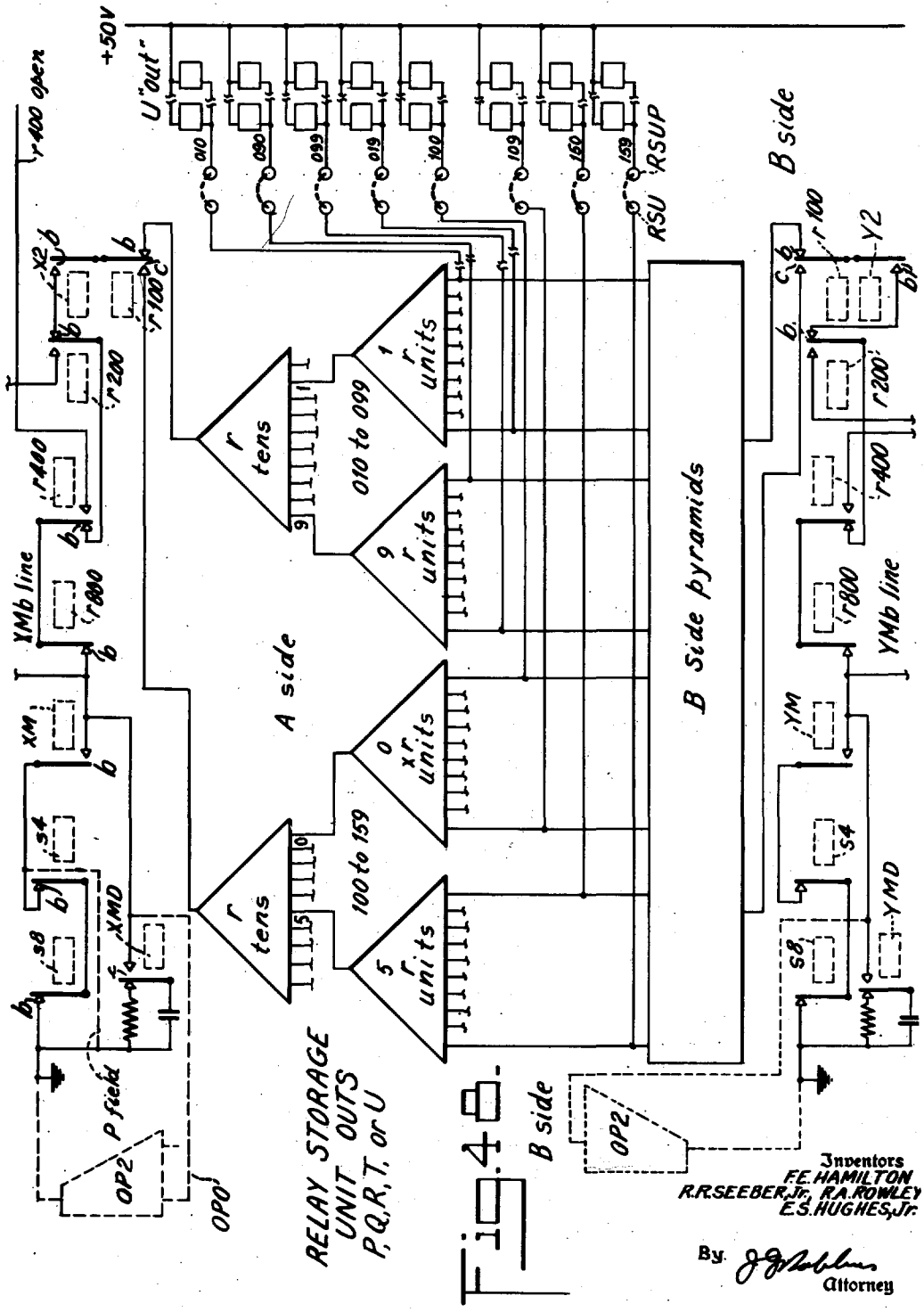

Fig. 40.

Inventors
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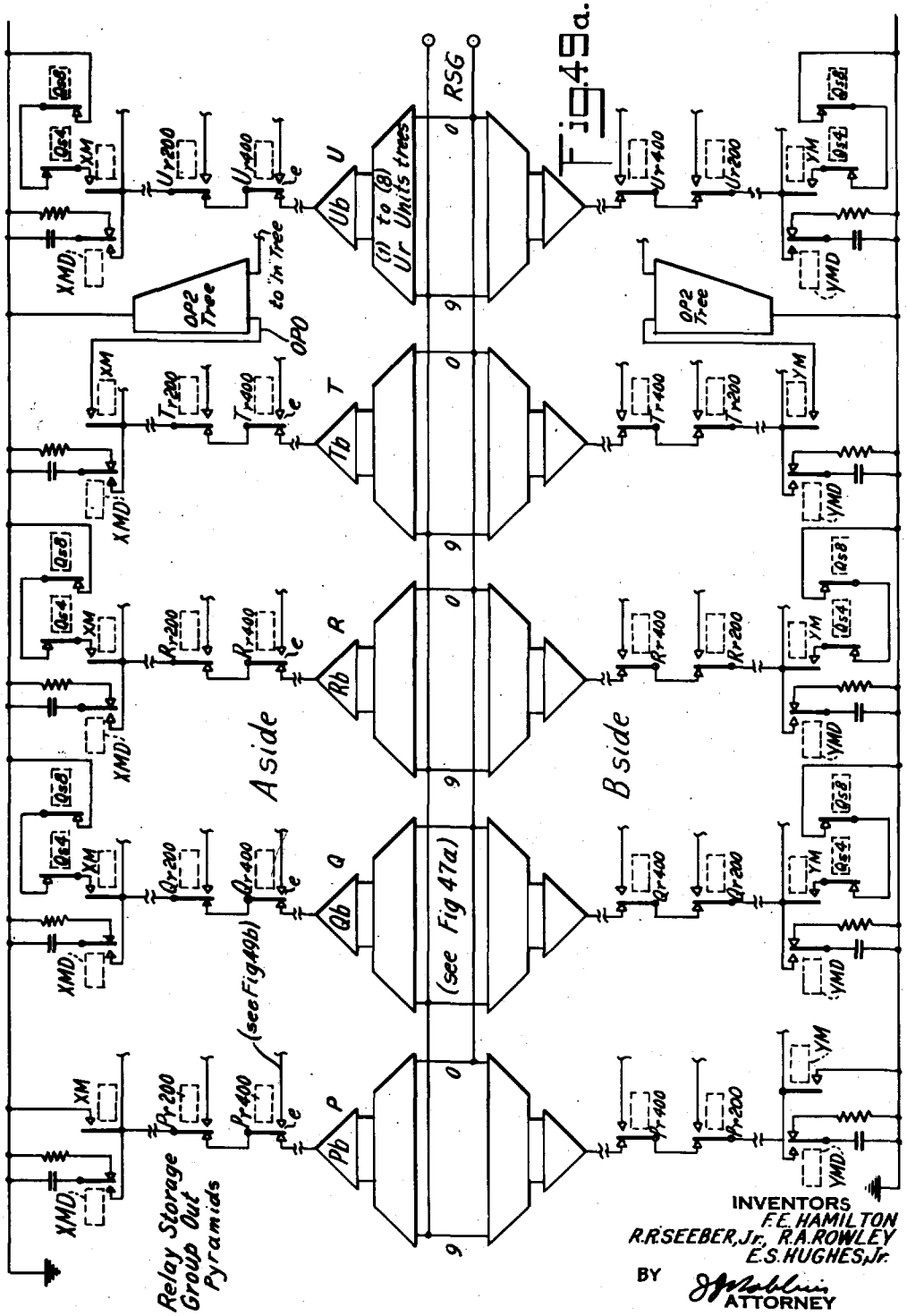

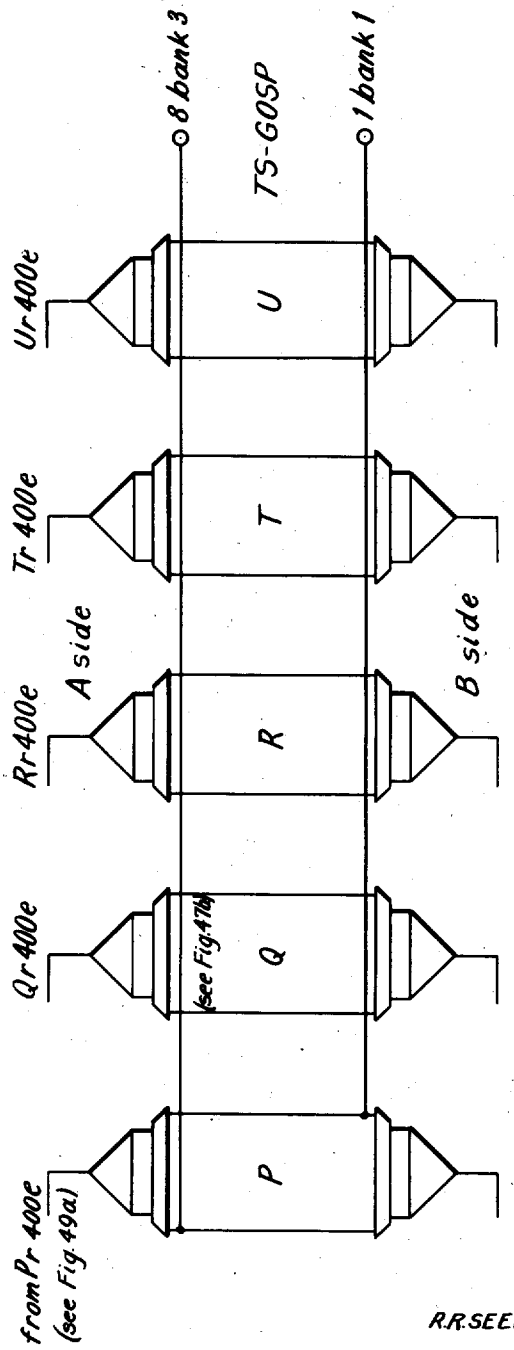

Fig. 49b.

INVENTORS
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BY J. J. Lobbins
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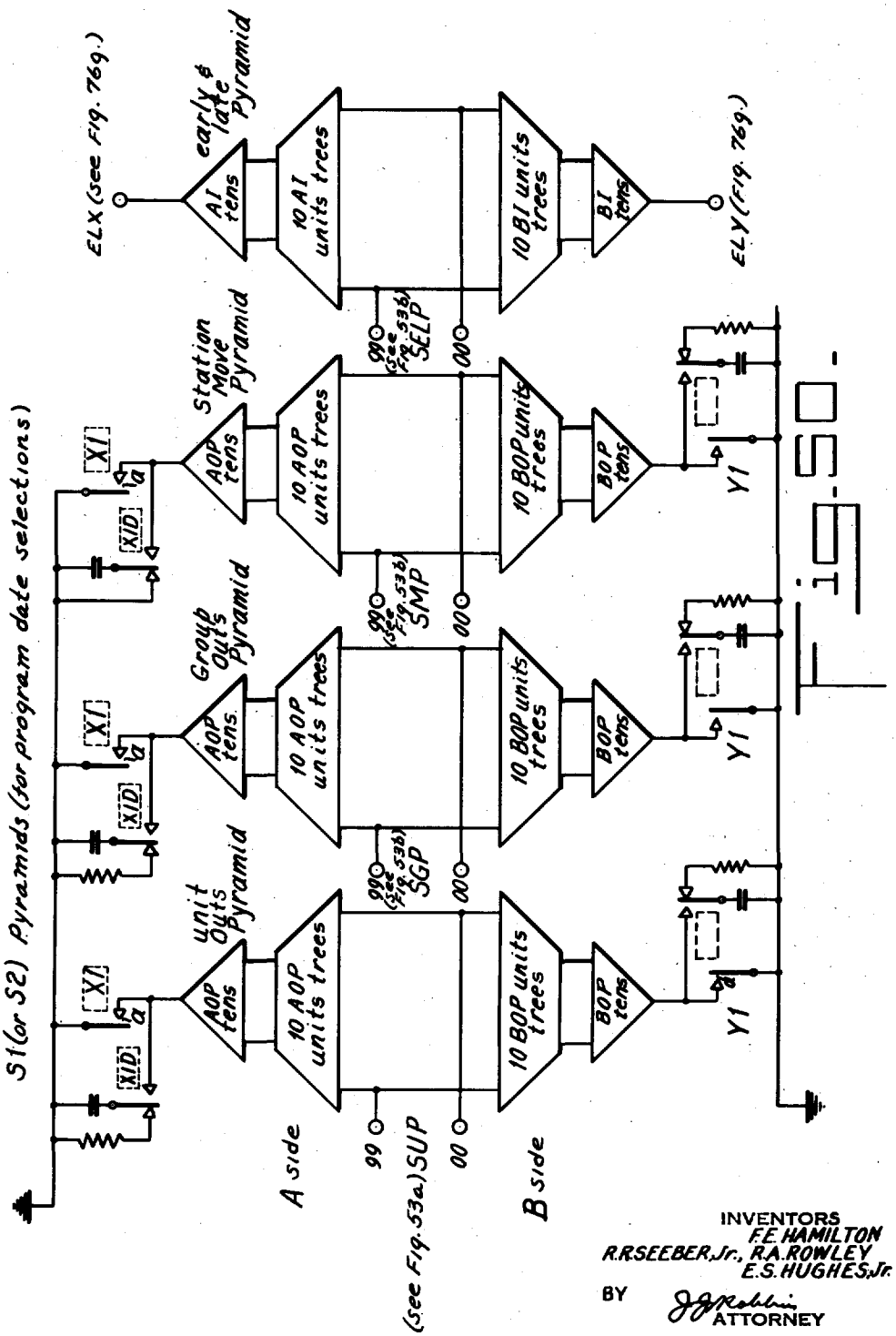

INVENTORS
F.E. HAMILTON
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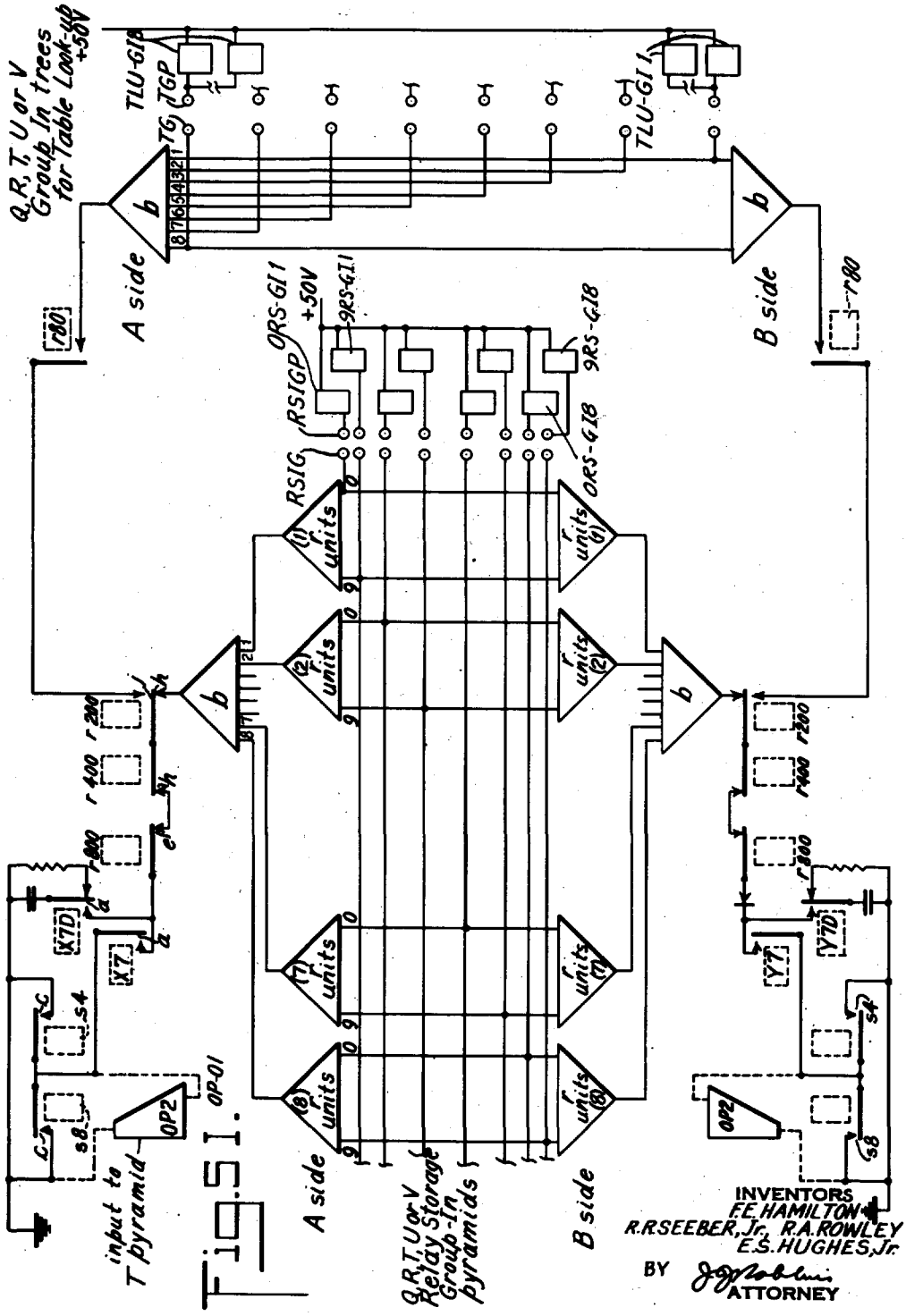

Fig. 51.

INVENTORS
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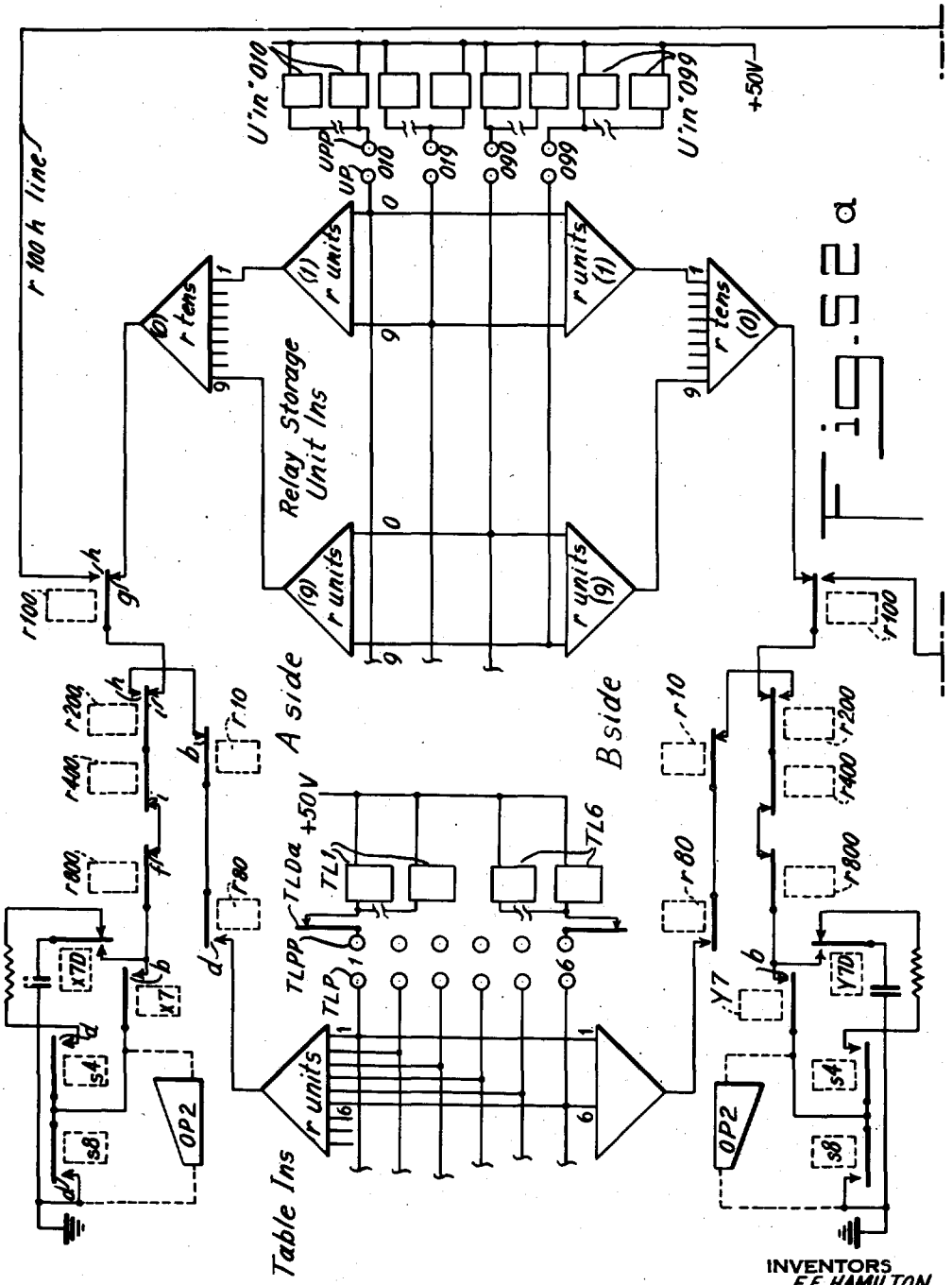

Fig. 52a

INVENTORS
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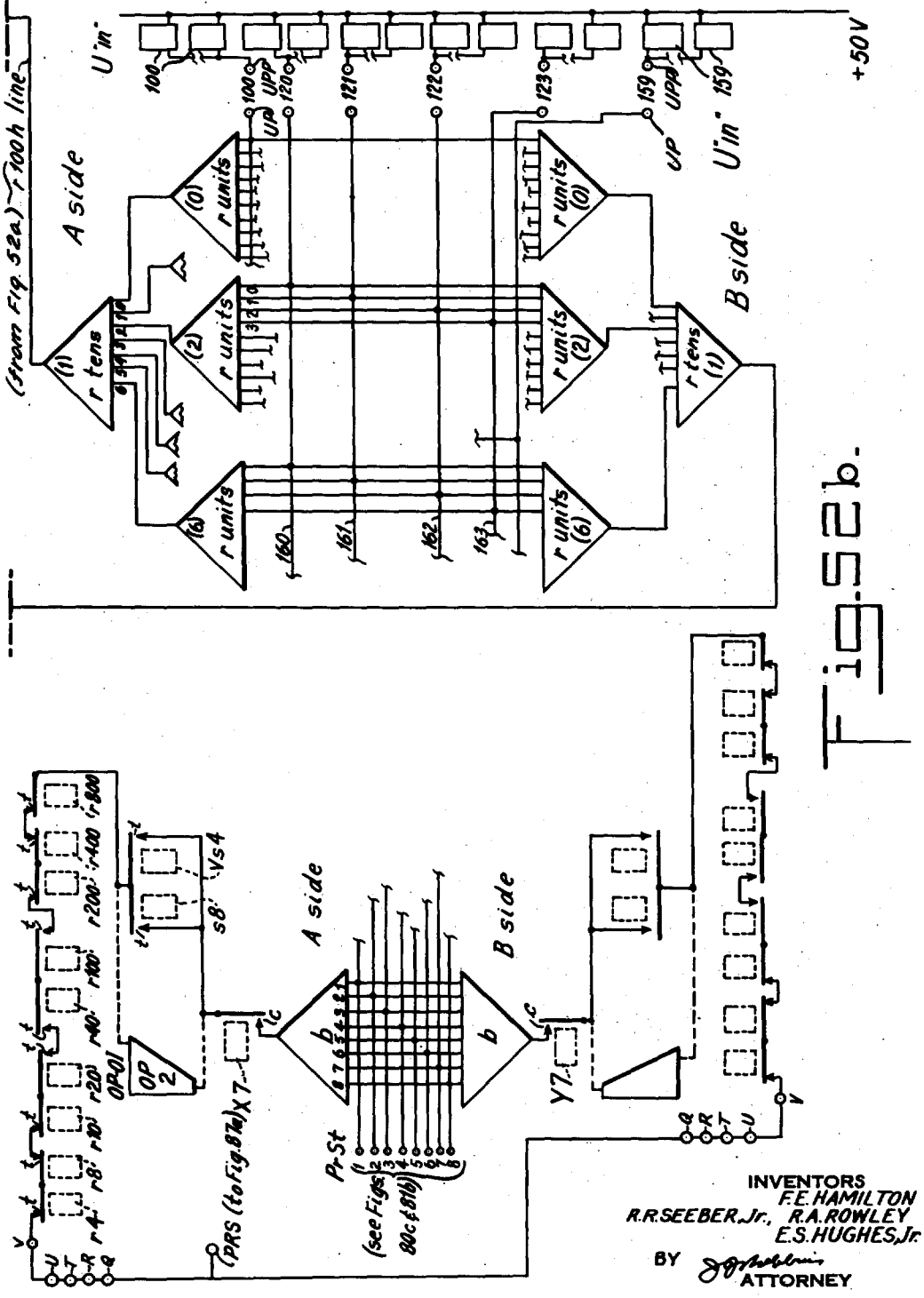

Fig. 52b.

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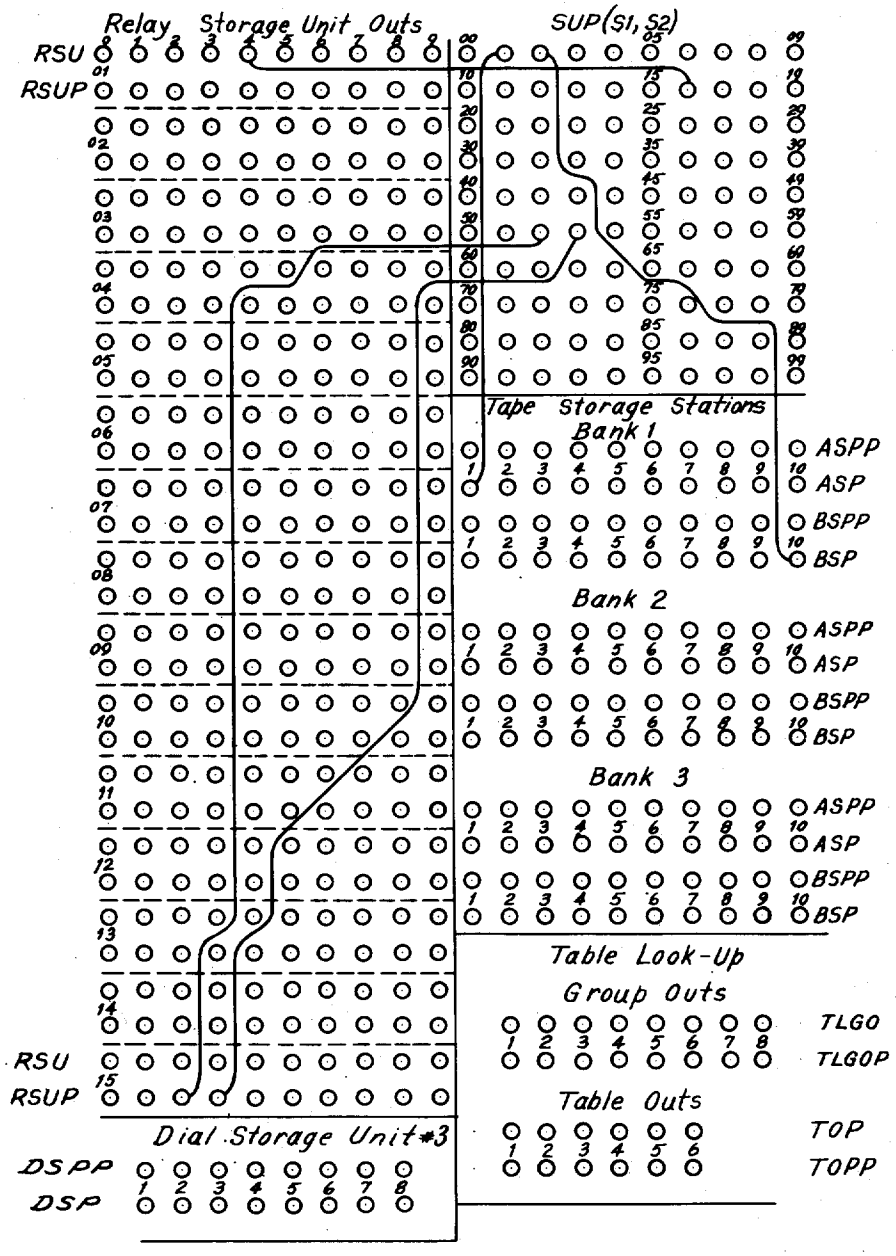

Fig. 53a.

INVENTORS
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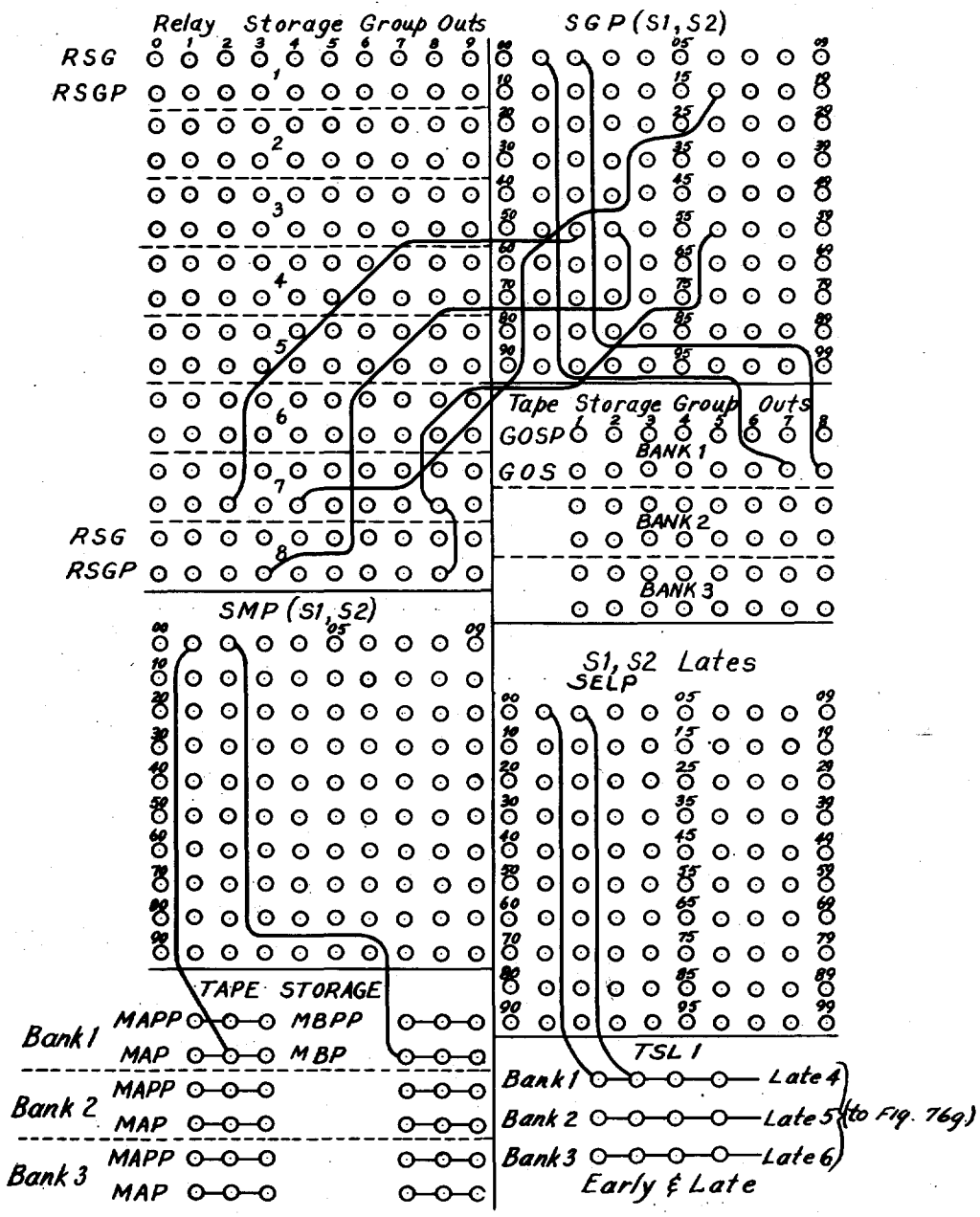

Fig. 53b.

INVENTORS
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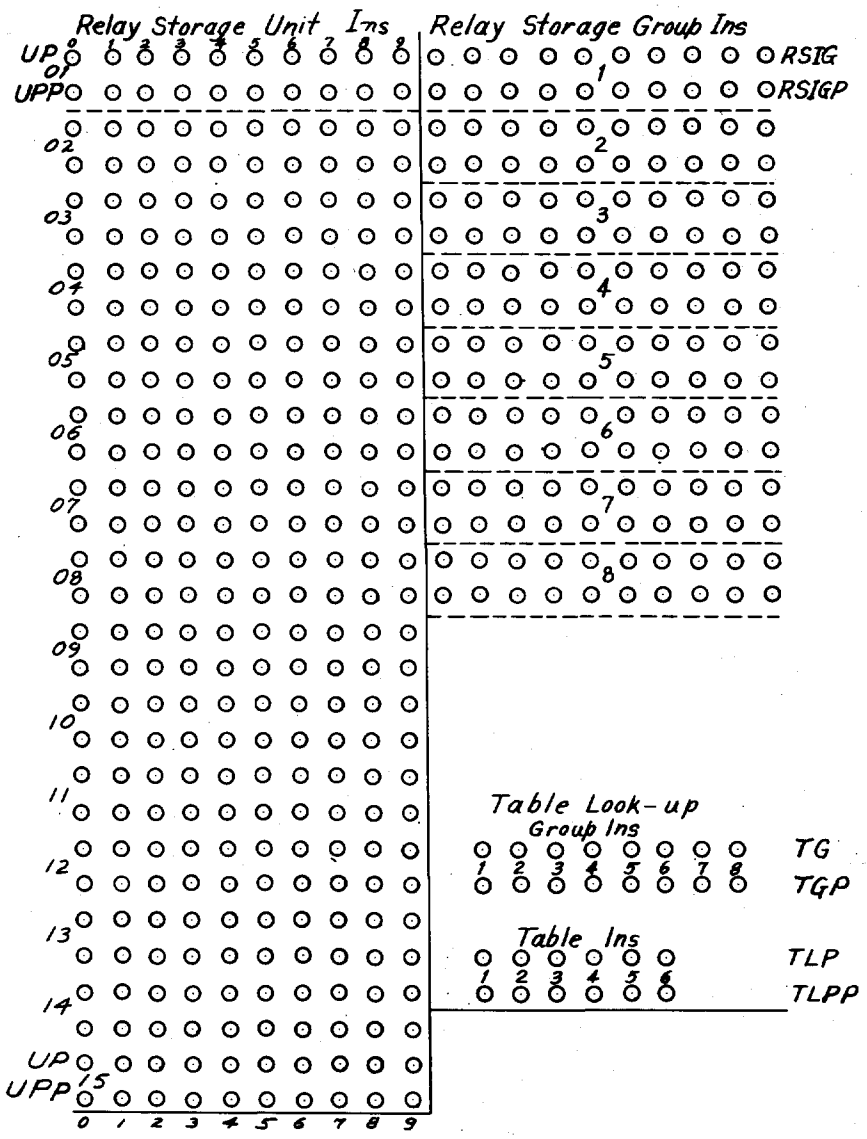

Fig. 53c.

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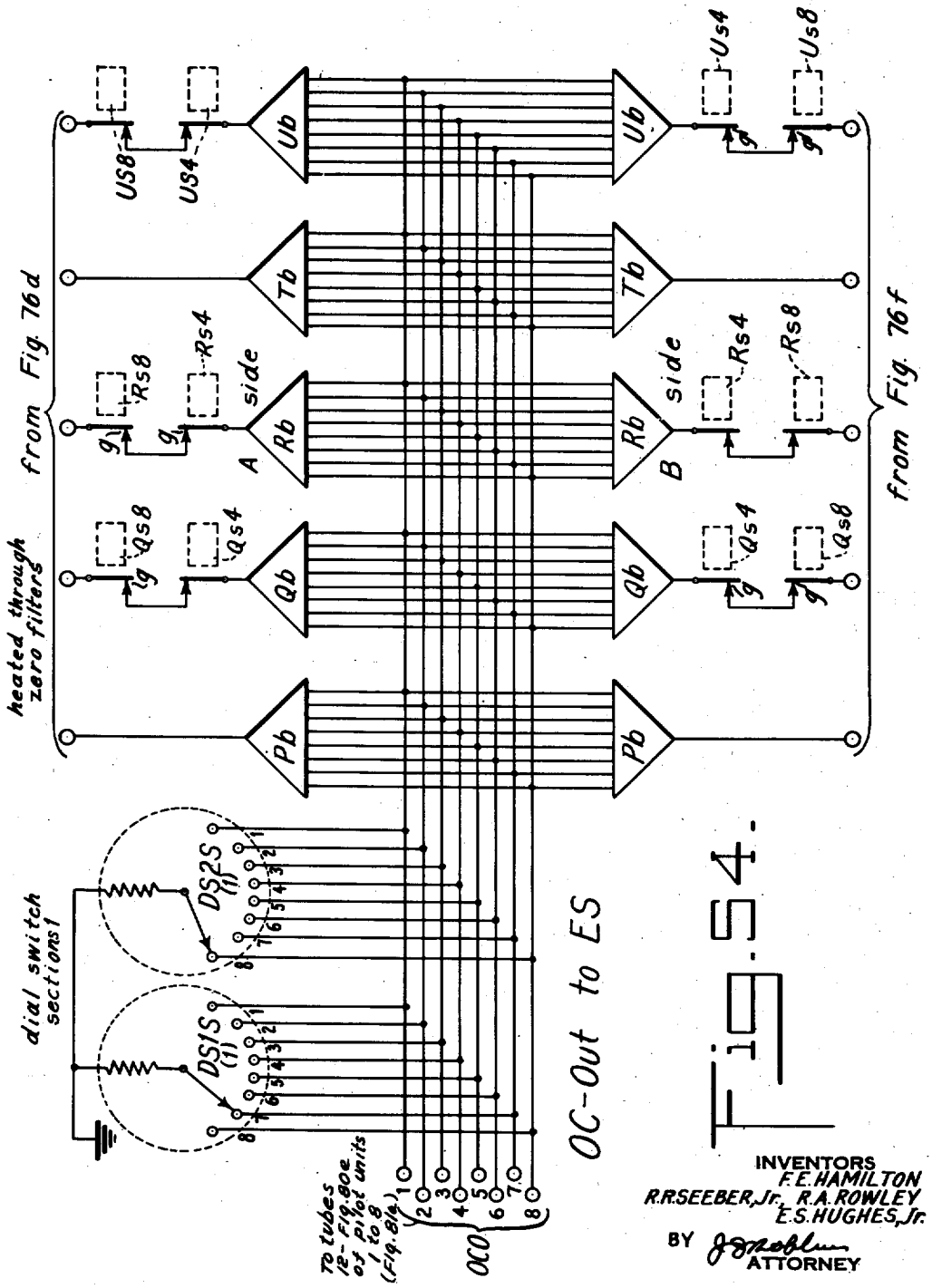

Fig. 54.

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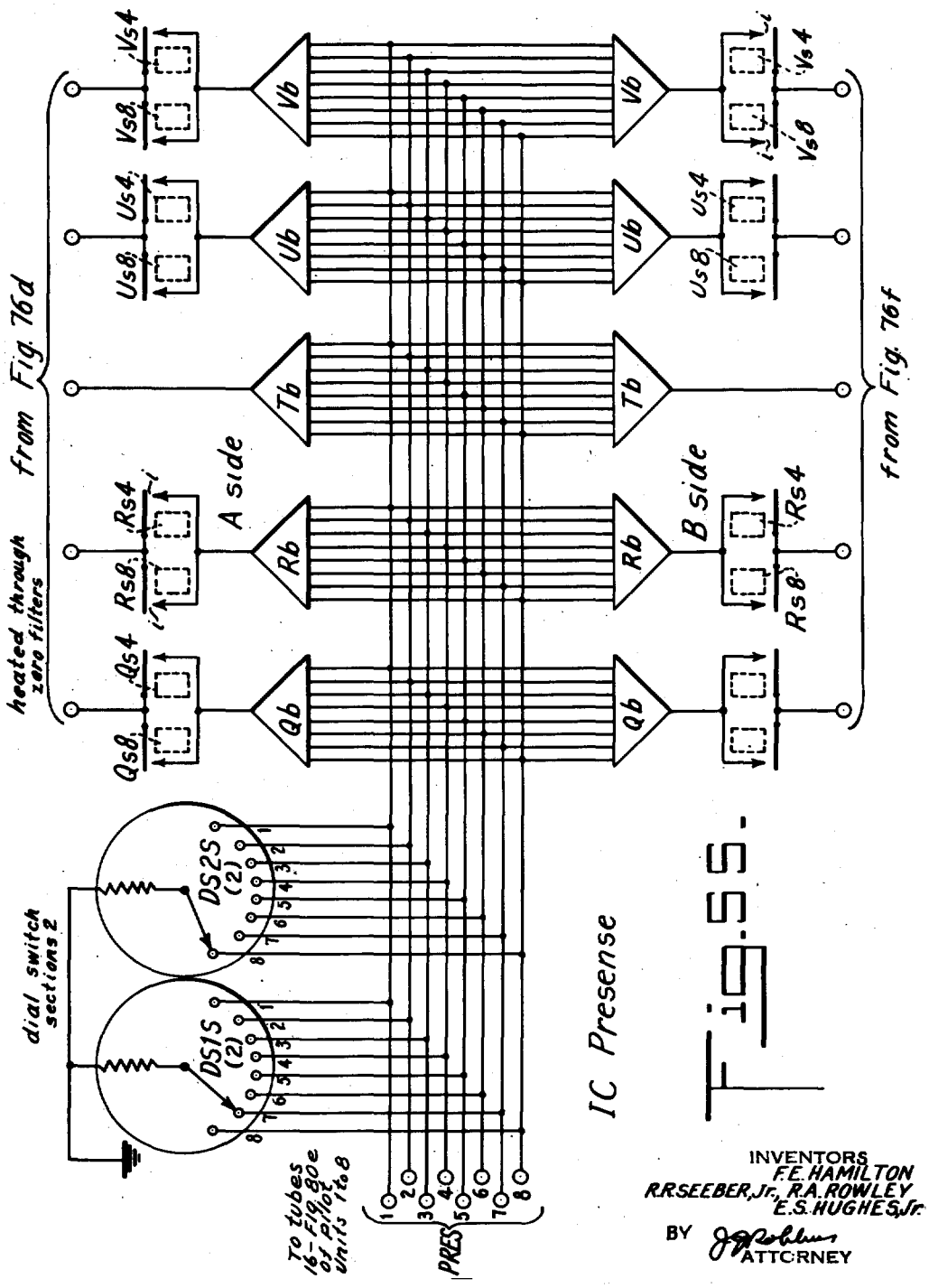

IC Presense

Fig. 55.

INVENTORS
F.E. HAMILTON
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E.S. HUGHES, Jr.

BY J. J. Robbins
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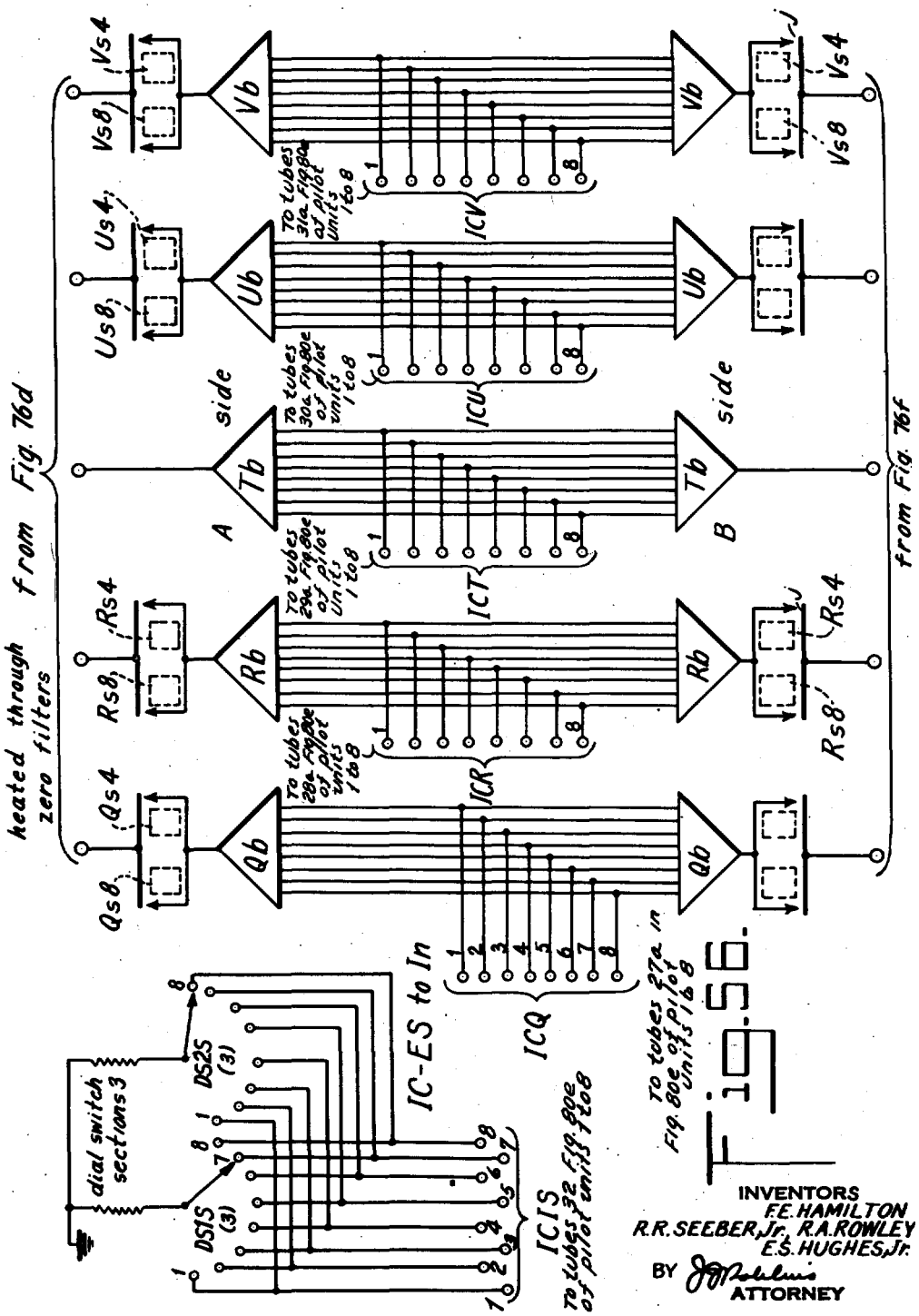

FIG. 56.

INVENTORS
F.E. HAMILTON
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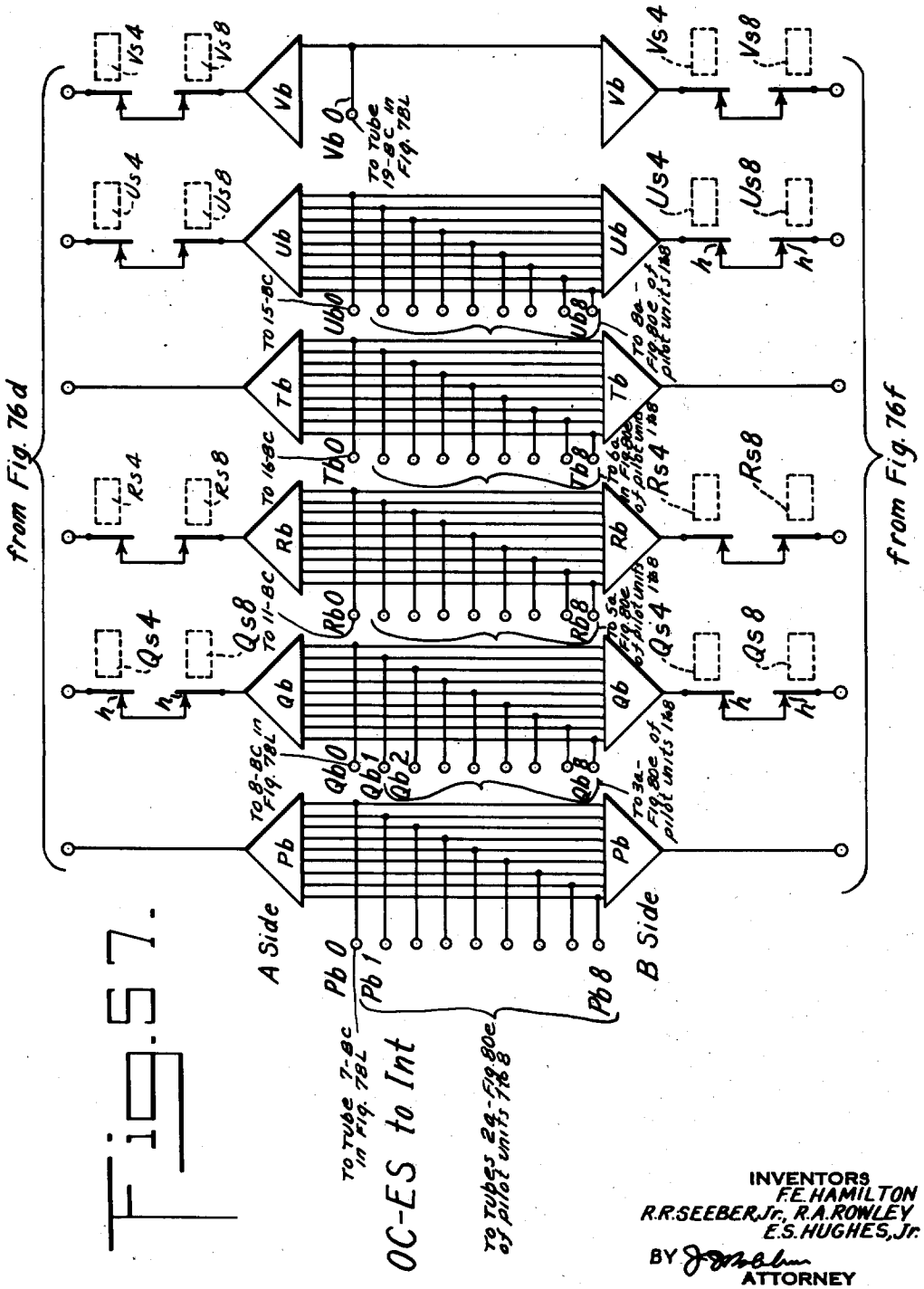

Fig. 57.

OC-ES to Int

INVENTORS
F.E. HAMILTON
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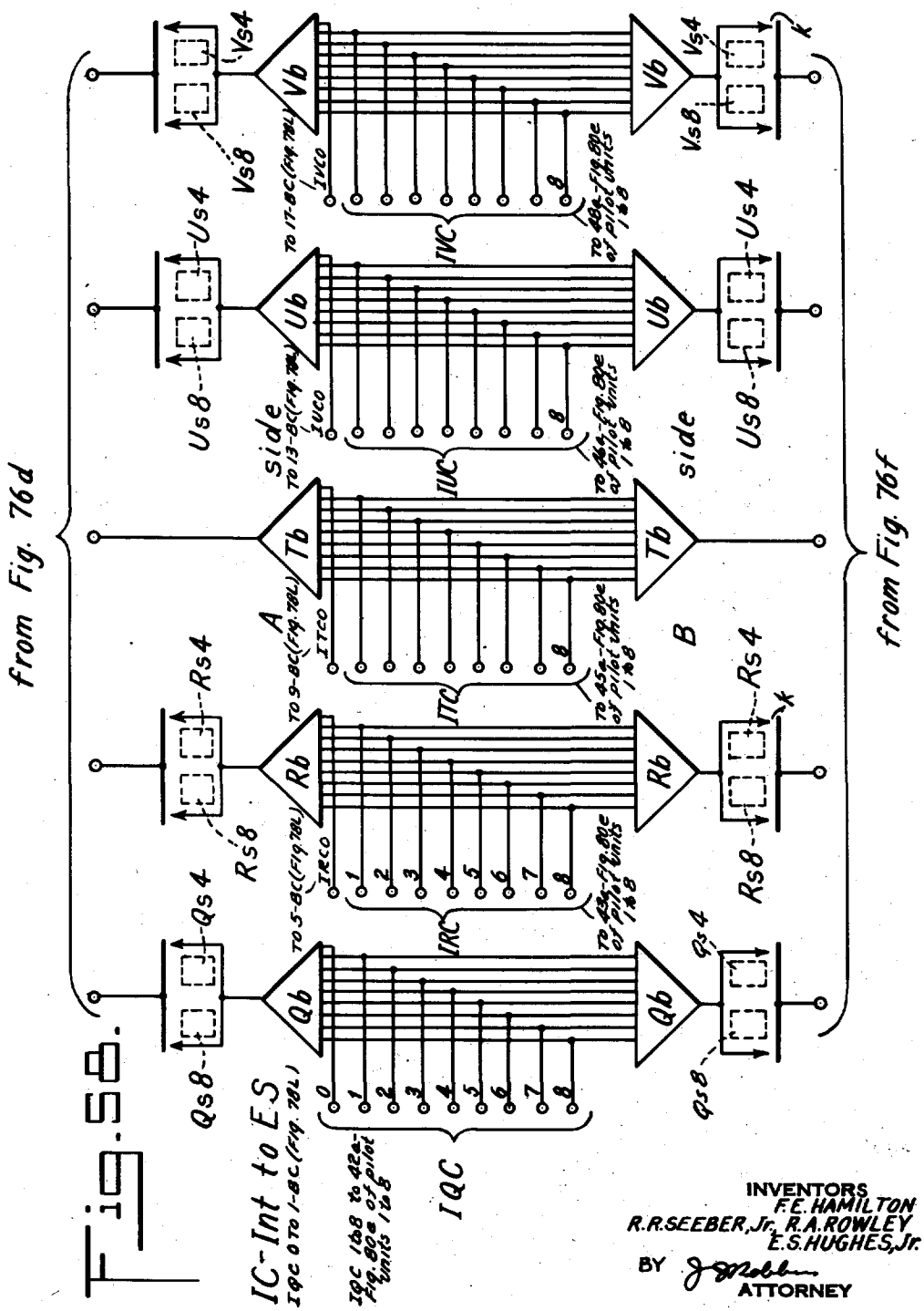

Fig. 58.

INVENTORS
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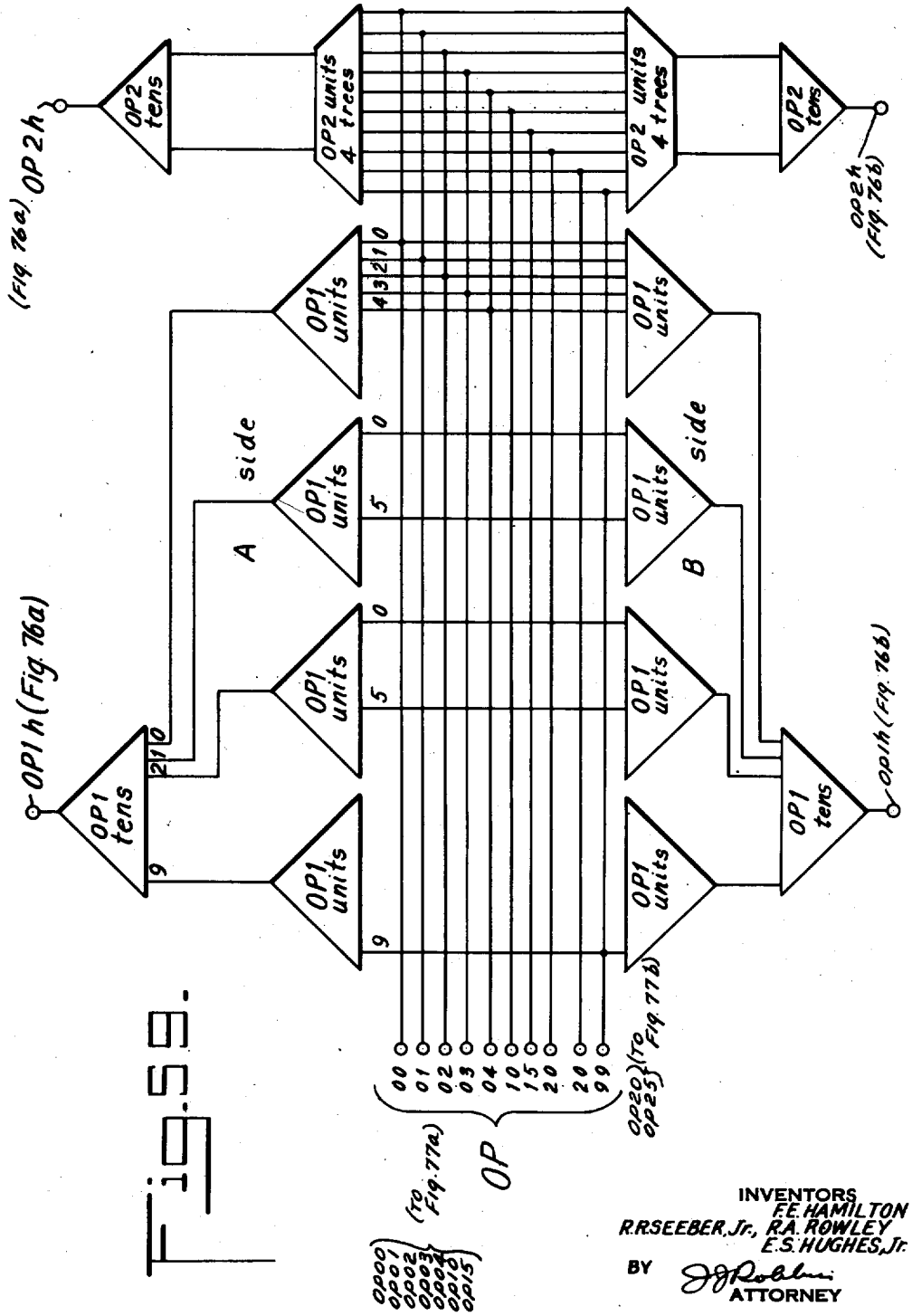

Fig. 59.

INVENTORS
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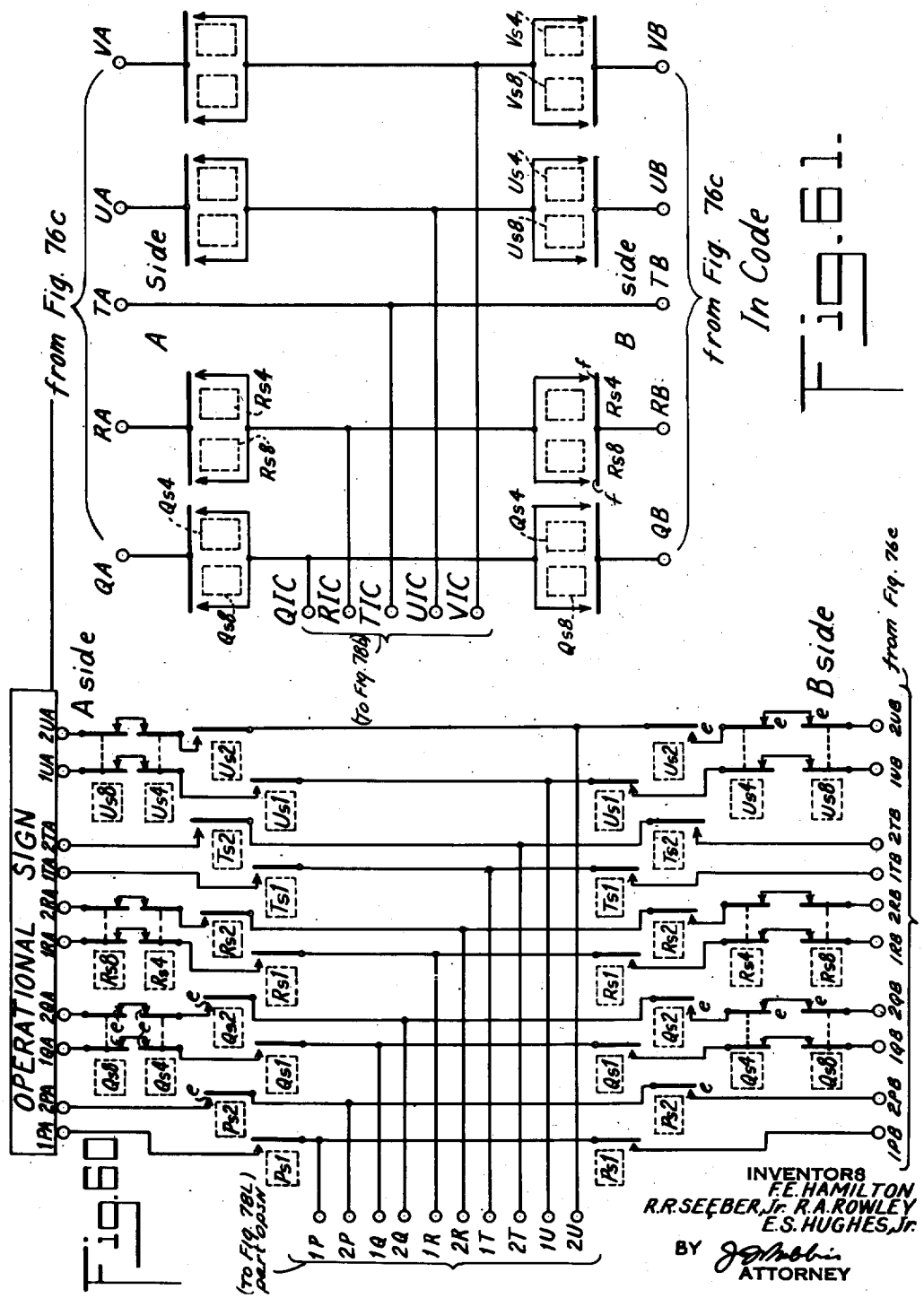

Fig. 61.

Fig. 60

INVENTORS
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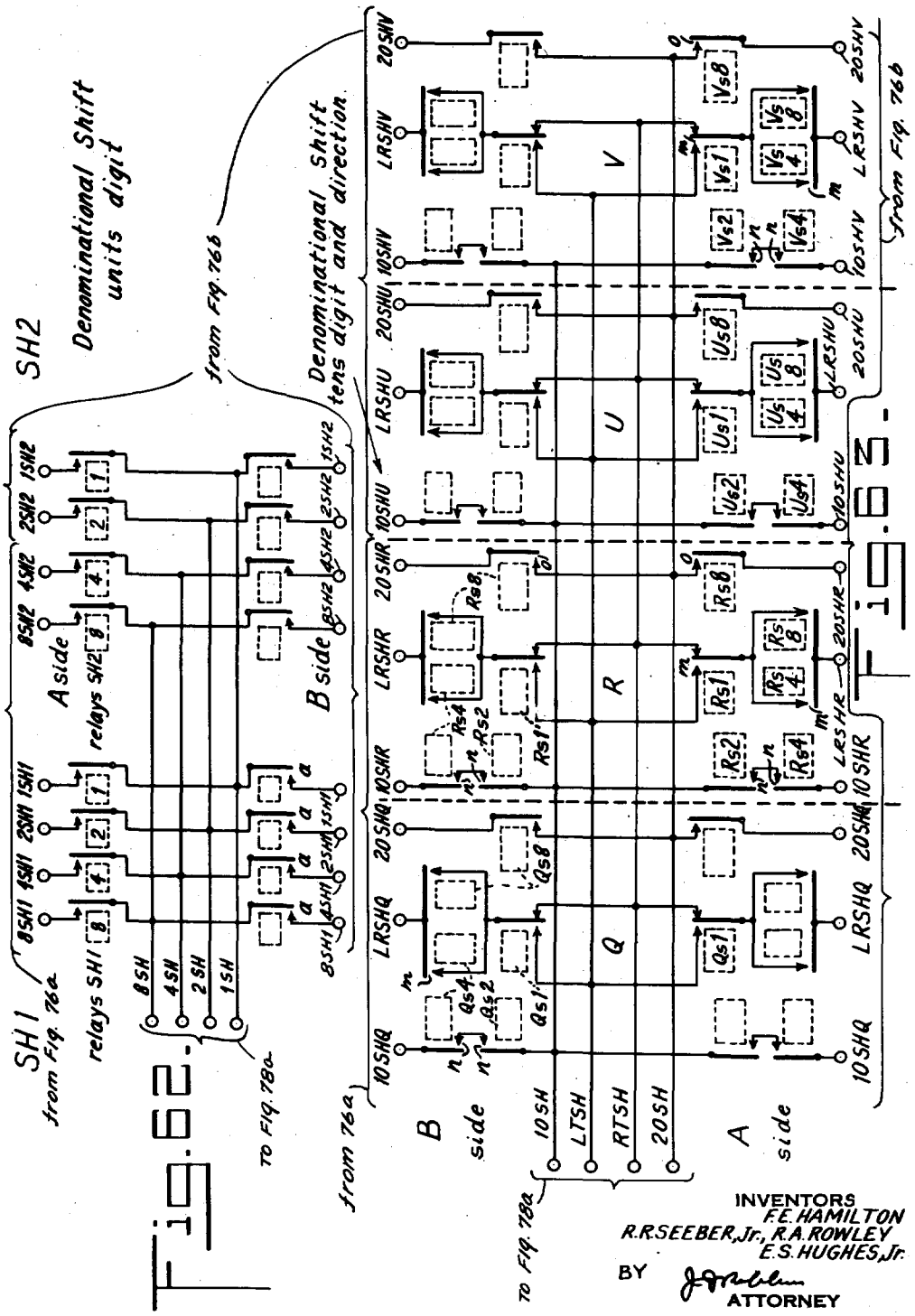

Fig. 62.

Fig. 15.

INVENTORS
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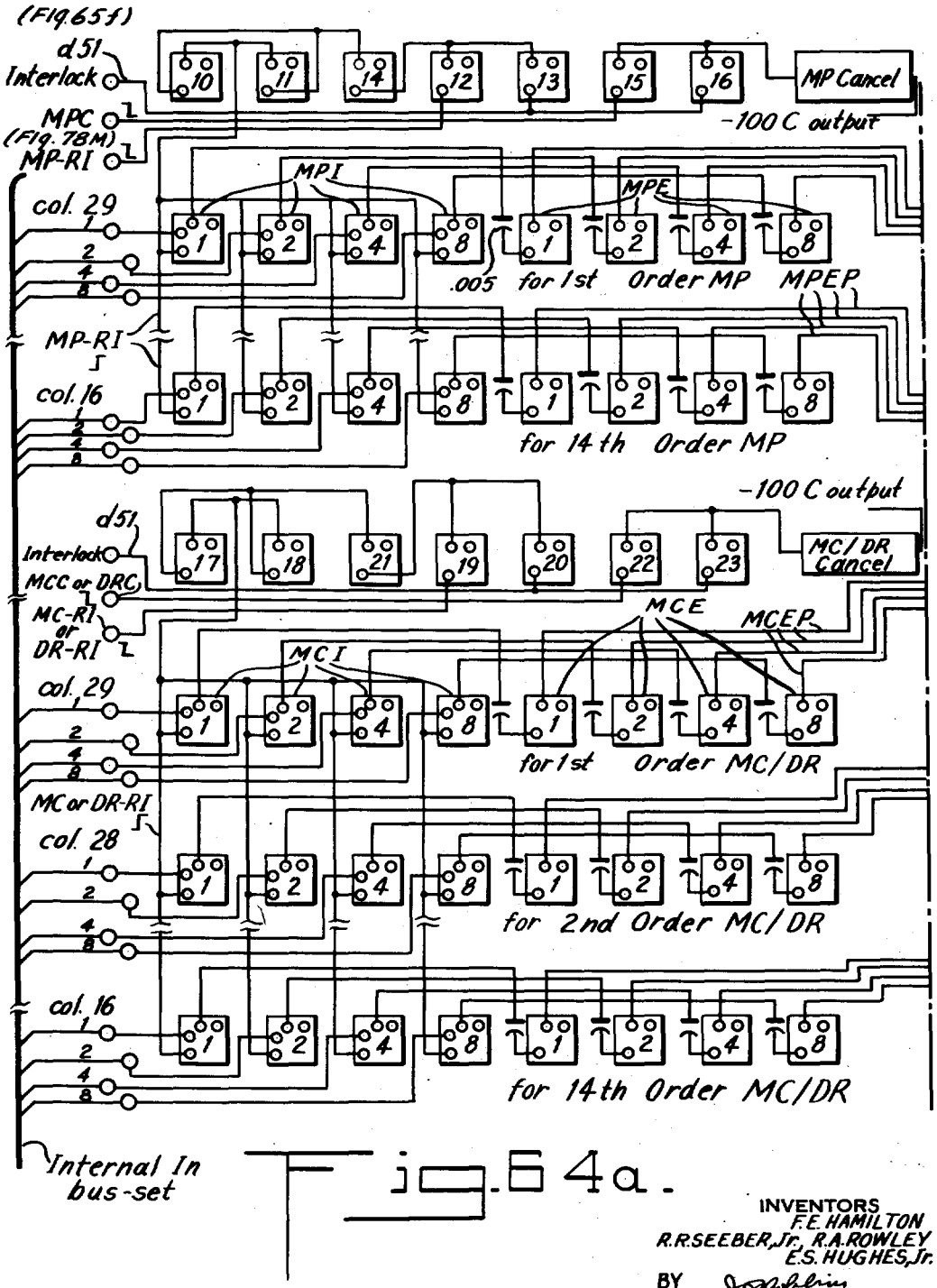

Fig. 64a.

INVENTORS
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E.S. HUGHES, Jr.

BY J. O'Neill
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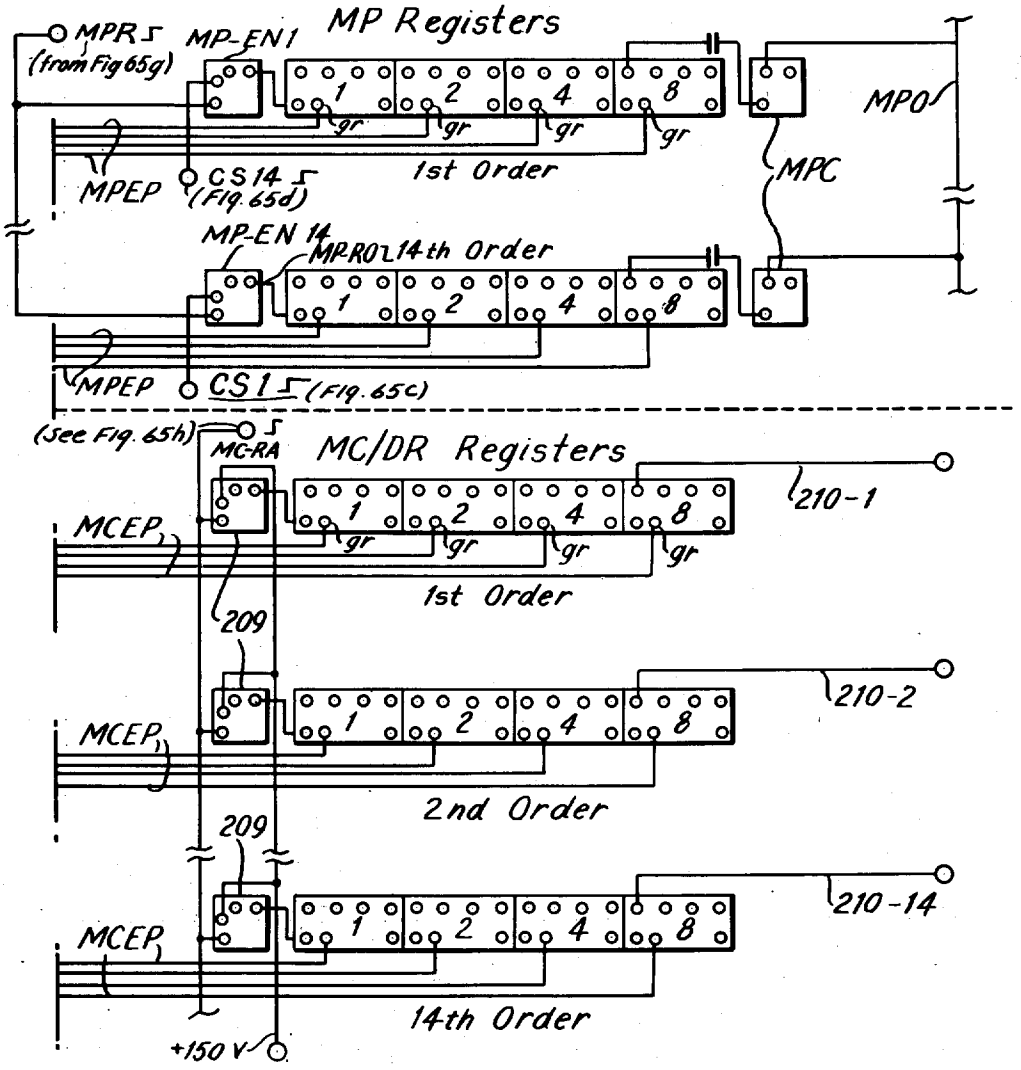

Fig. 64b.

INVENTORS
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BY
ATTORNEY

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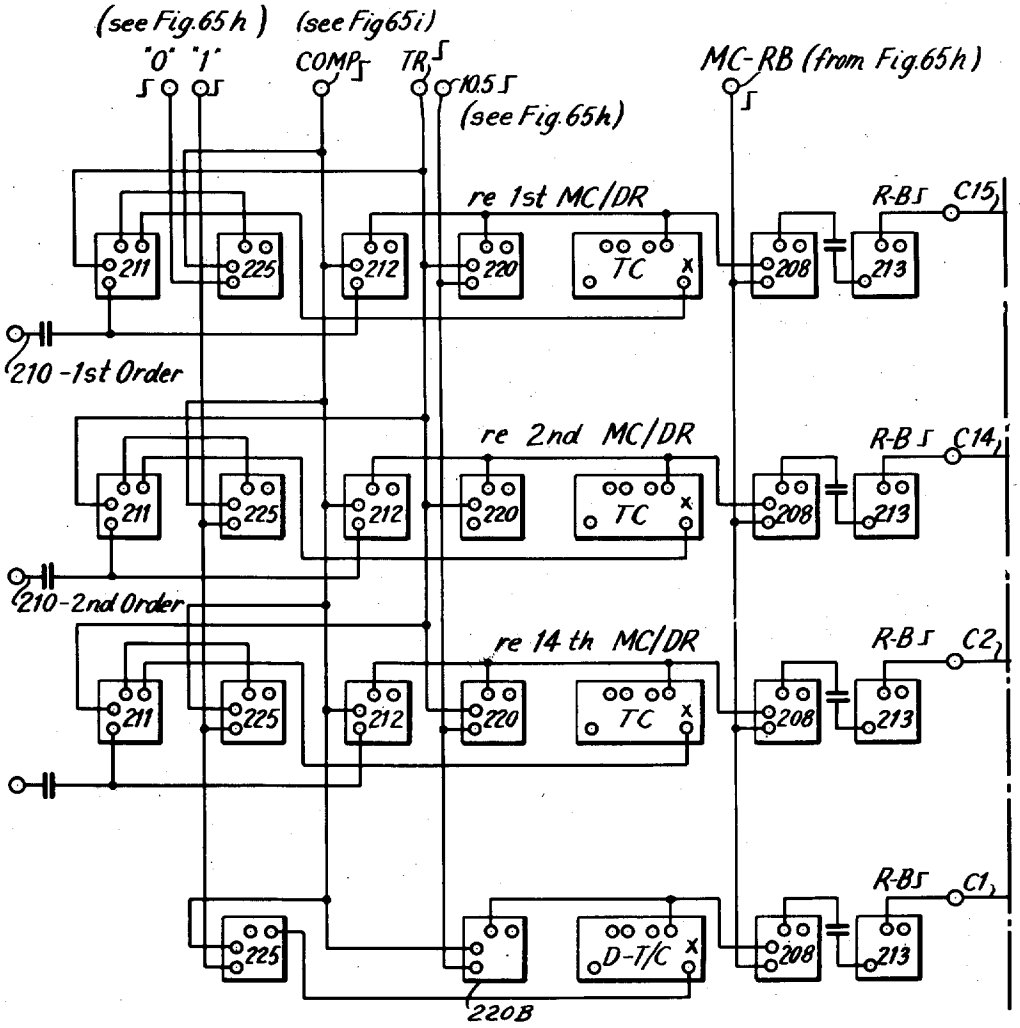

Fig. 64c.

INVENTORS
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BY
ATTORNEY

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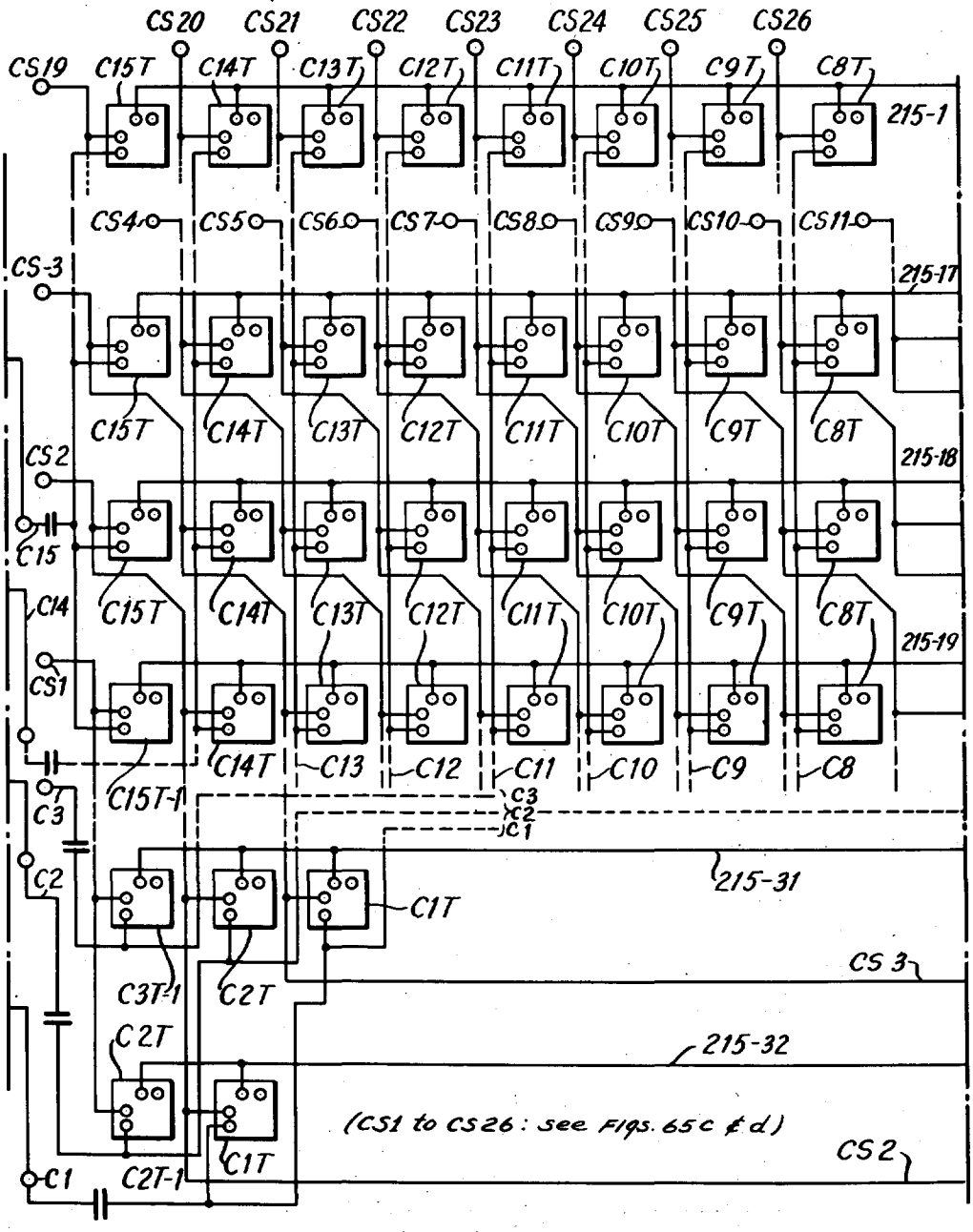

Fig. 64d.

INVENTORS
F.E. HAMILTON
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E.S. HUGHES, Jr.
BY J. J. Pebbles
ATTORNEY

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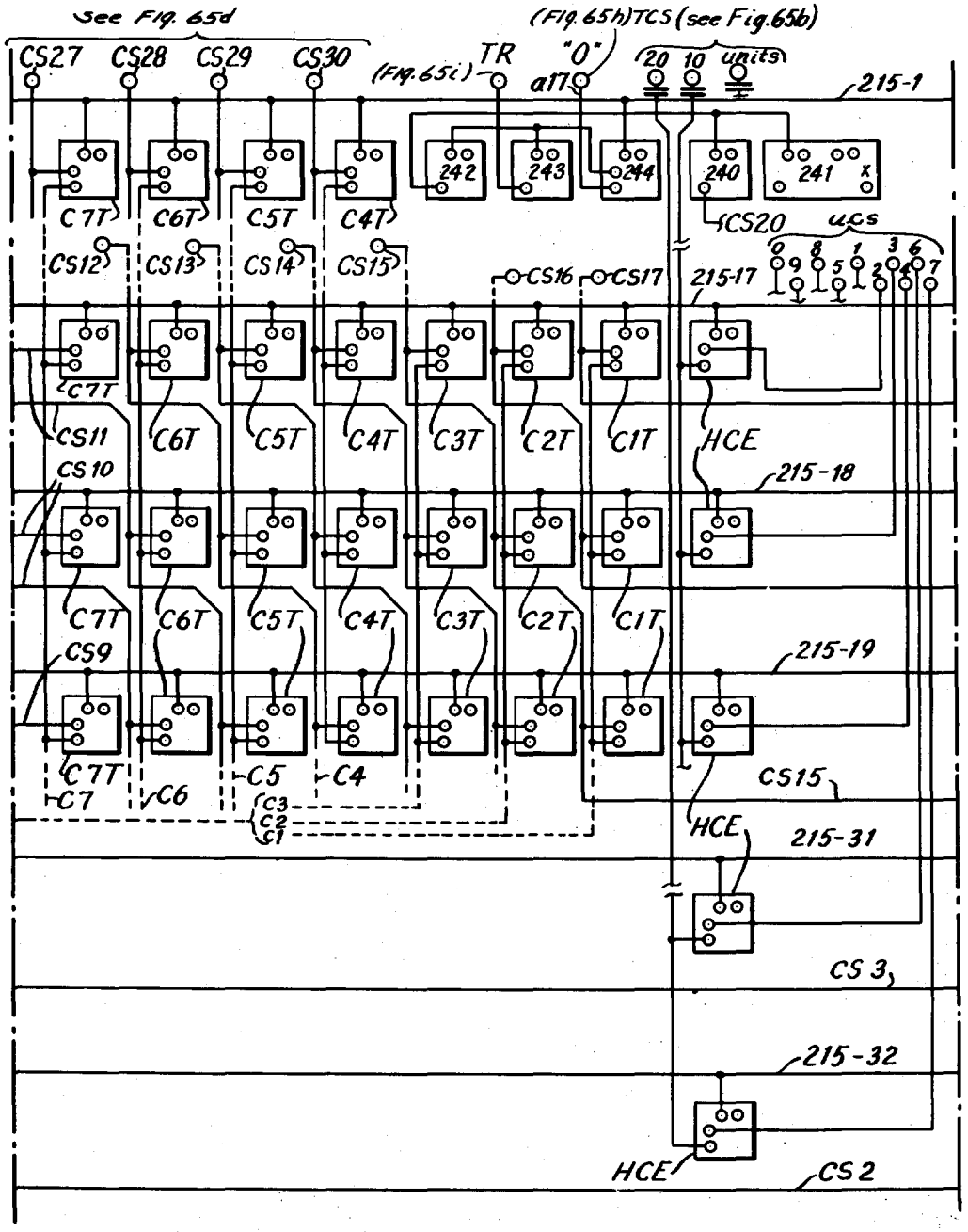

Fig. 64e.

INVENTORS
F.E. HAMILTON
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BY J. J. Mahon
ATTORNEY

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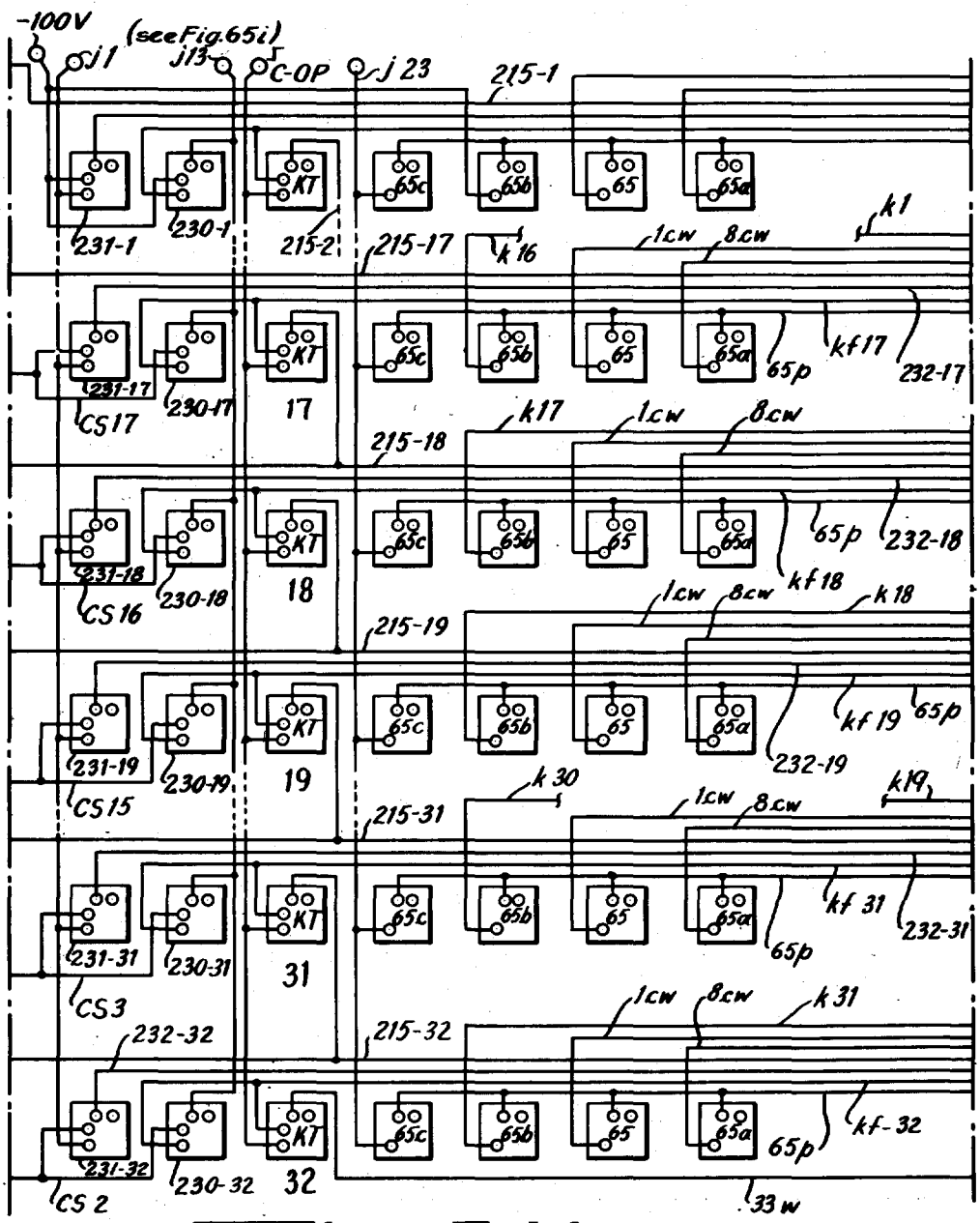

Fig. 64f.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.
BY J. P. Robbins
ATTORNEY

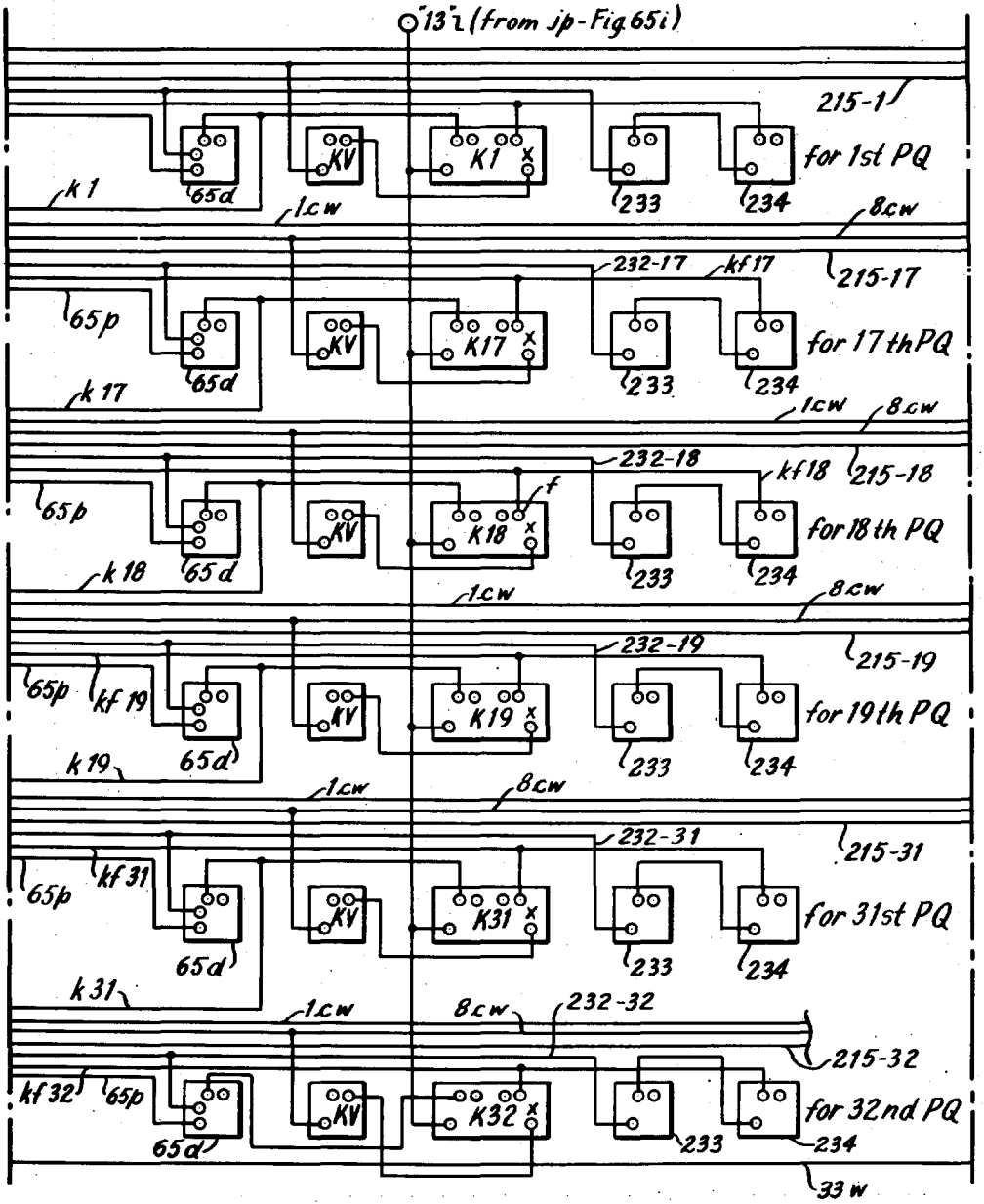

Fig. 64.

INVENTORS
F.E.HAMILTON
R.R.SEEBER,Jr. R.A.ROWLEY
E.S.HUGHES,Jr.
BY
ATTORNEY

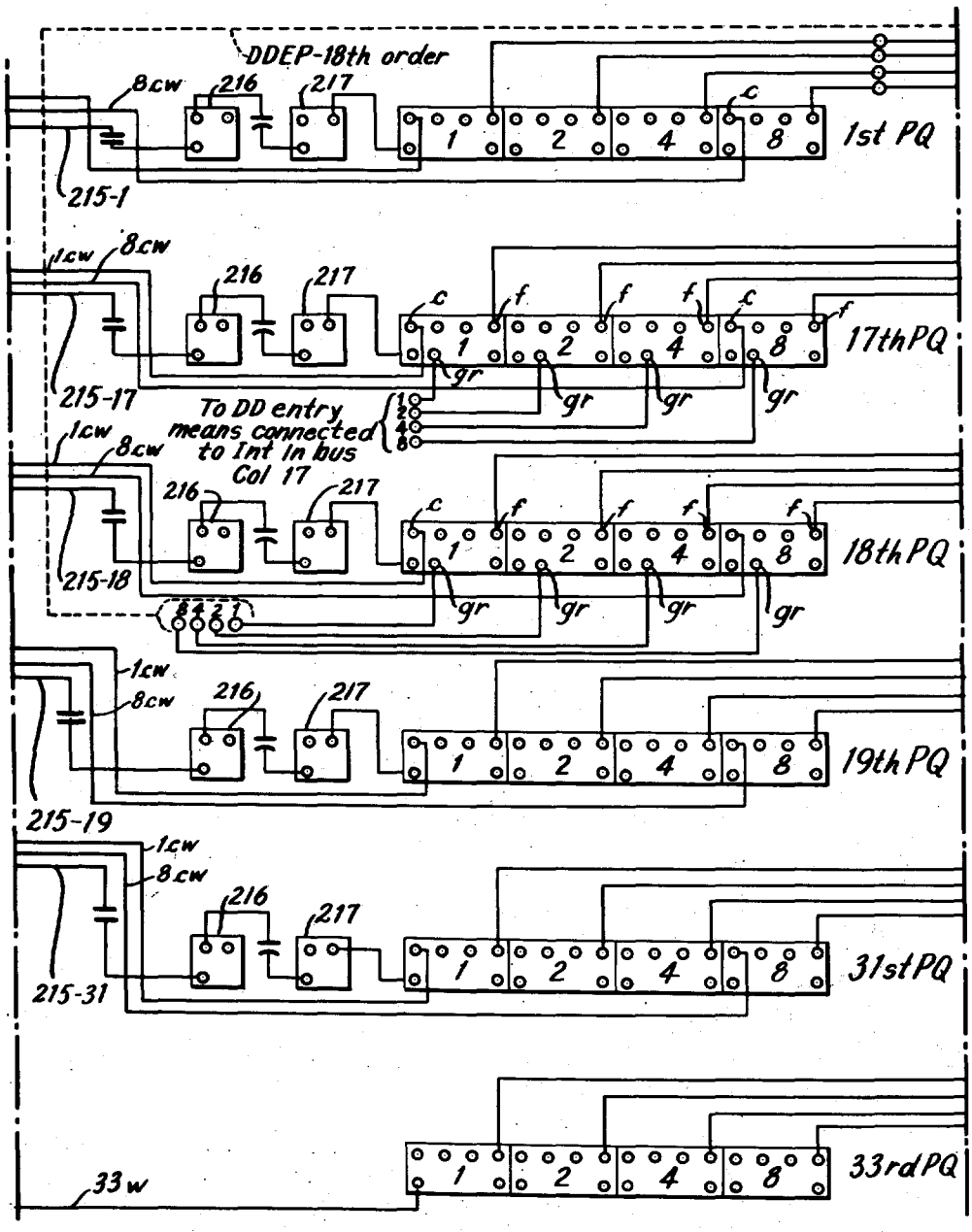

Fig. 64h.

INVENTORS
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ATTORNEY

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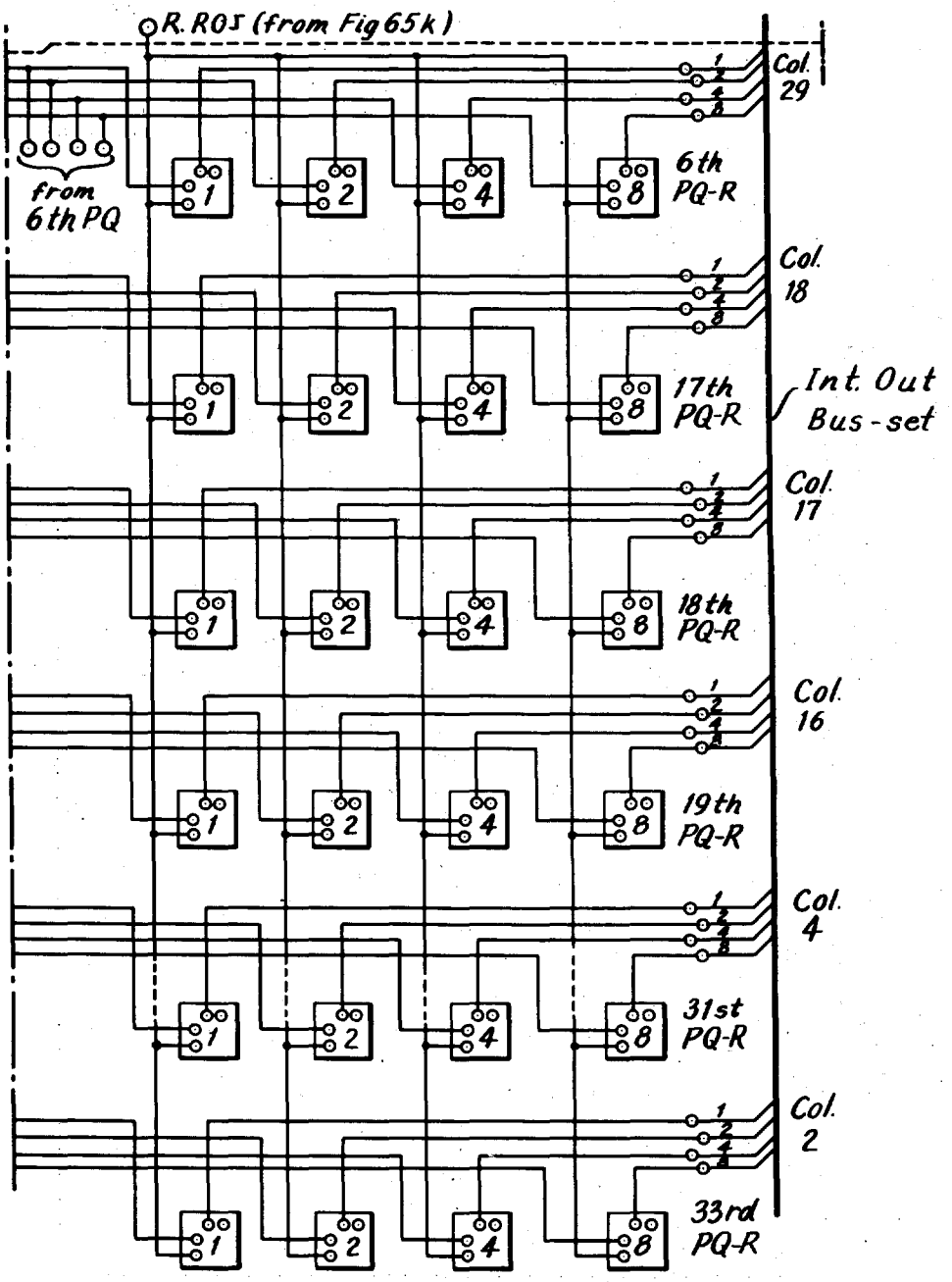

Fig. 64i.

INVENTOR
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April 28, 1953 F. E. HAMILTON ET AL 2,636,672

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 65

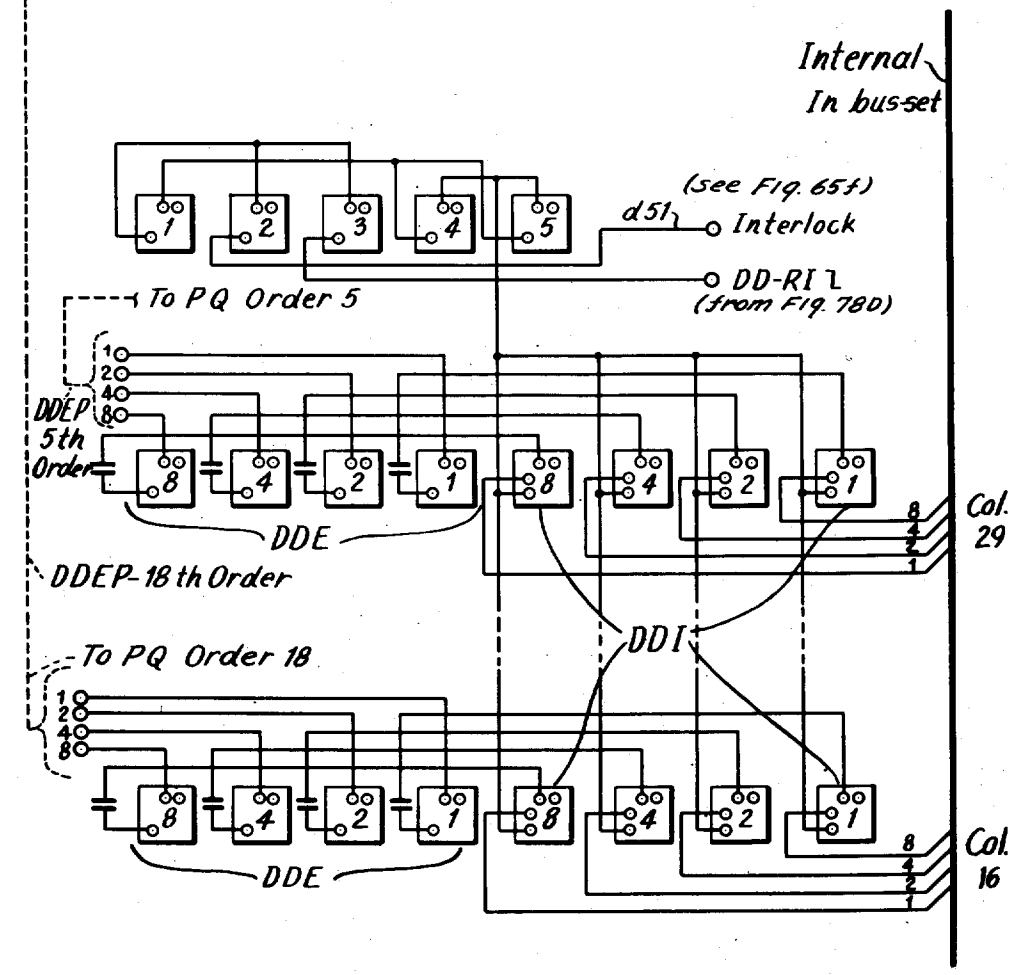

Fig. 64j.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.
BY J.O. Robbins
ATTORNEY

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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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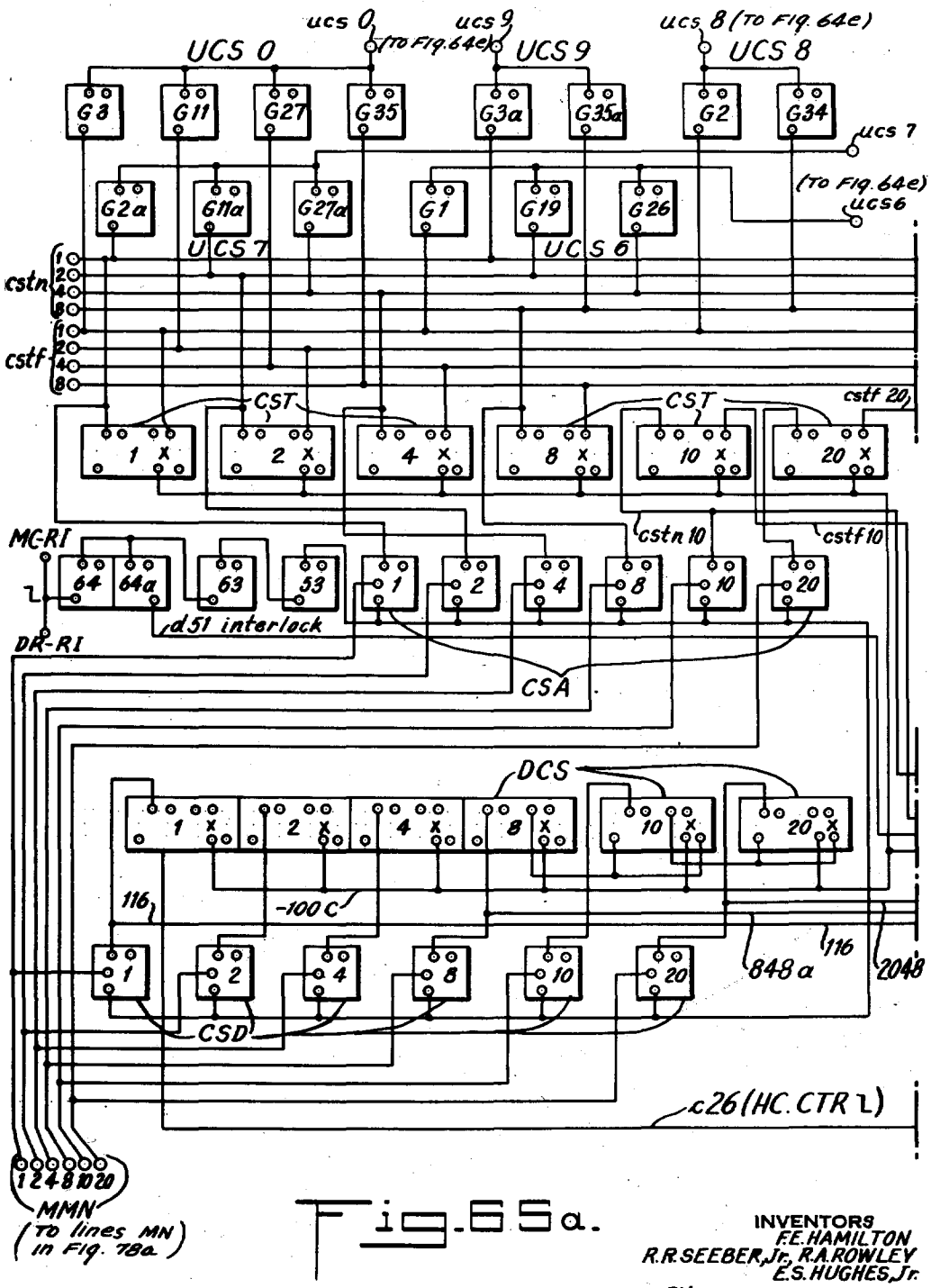

Fig. 65a.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.

BY J. P. Eckert
ATTORNEY

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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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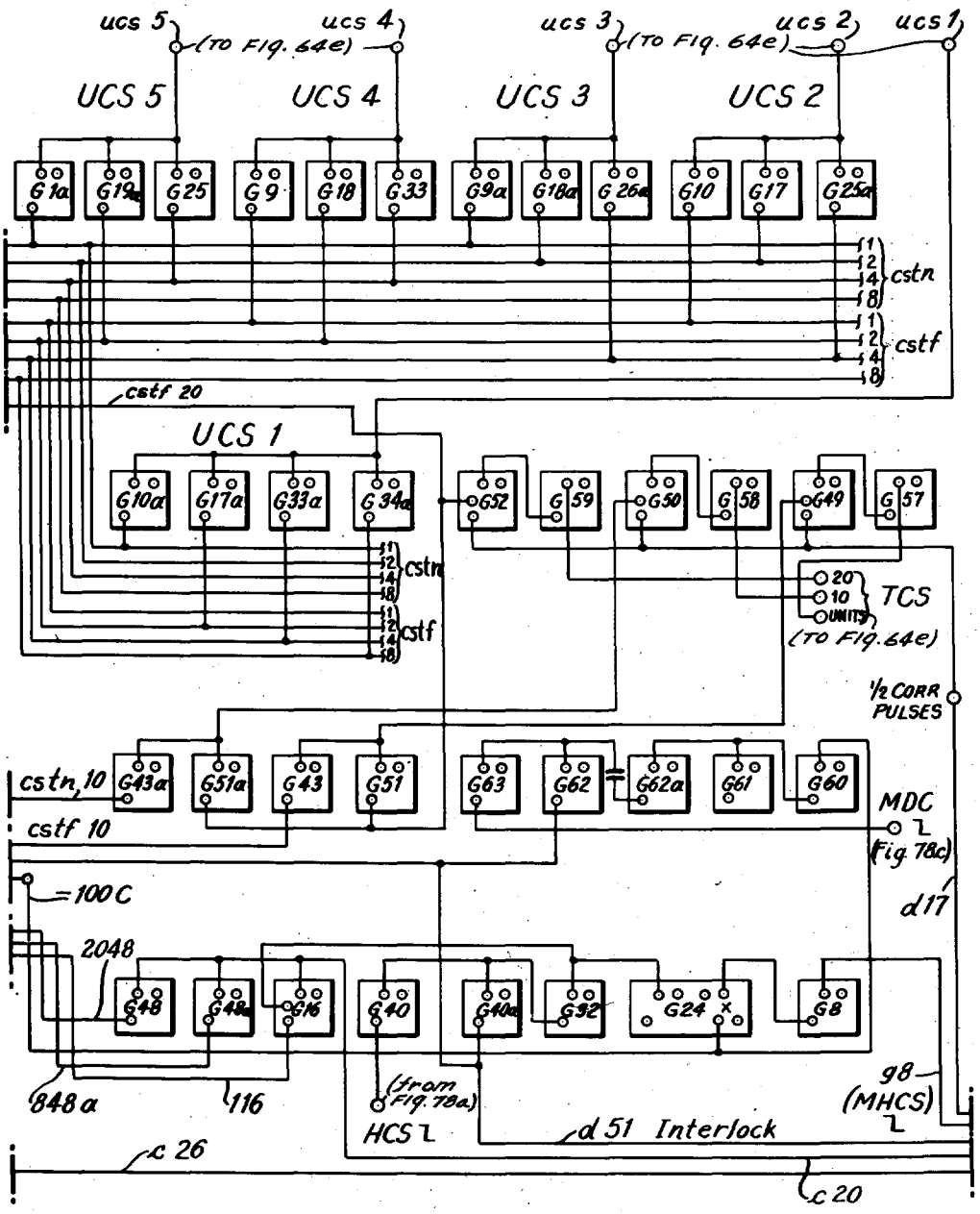

Fig. 65b.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr. R.A. ROWLEY
E.S. HUGHES, Jr.

BY J. Mabin
ATTORNEY

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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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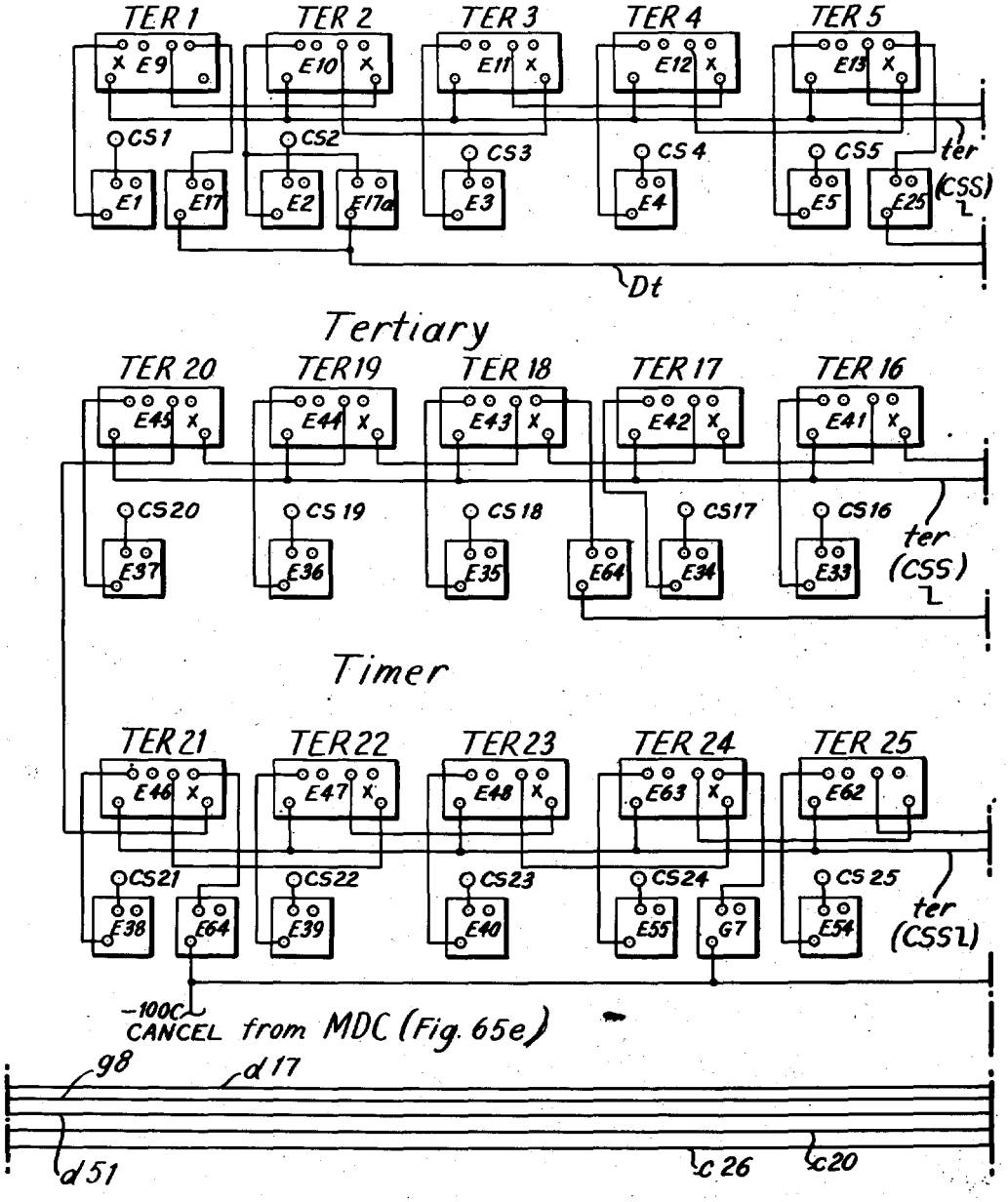

Fig. 65c.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr
BY J. Mobbins
ATTORNEY

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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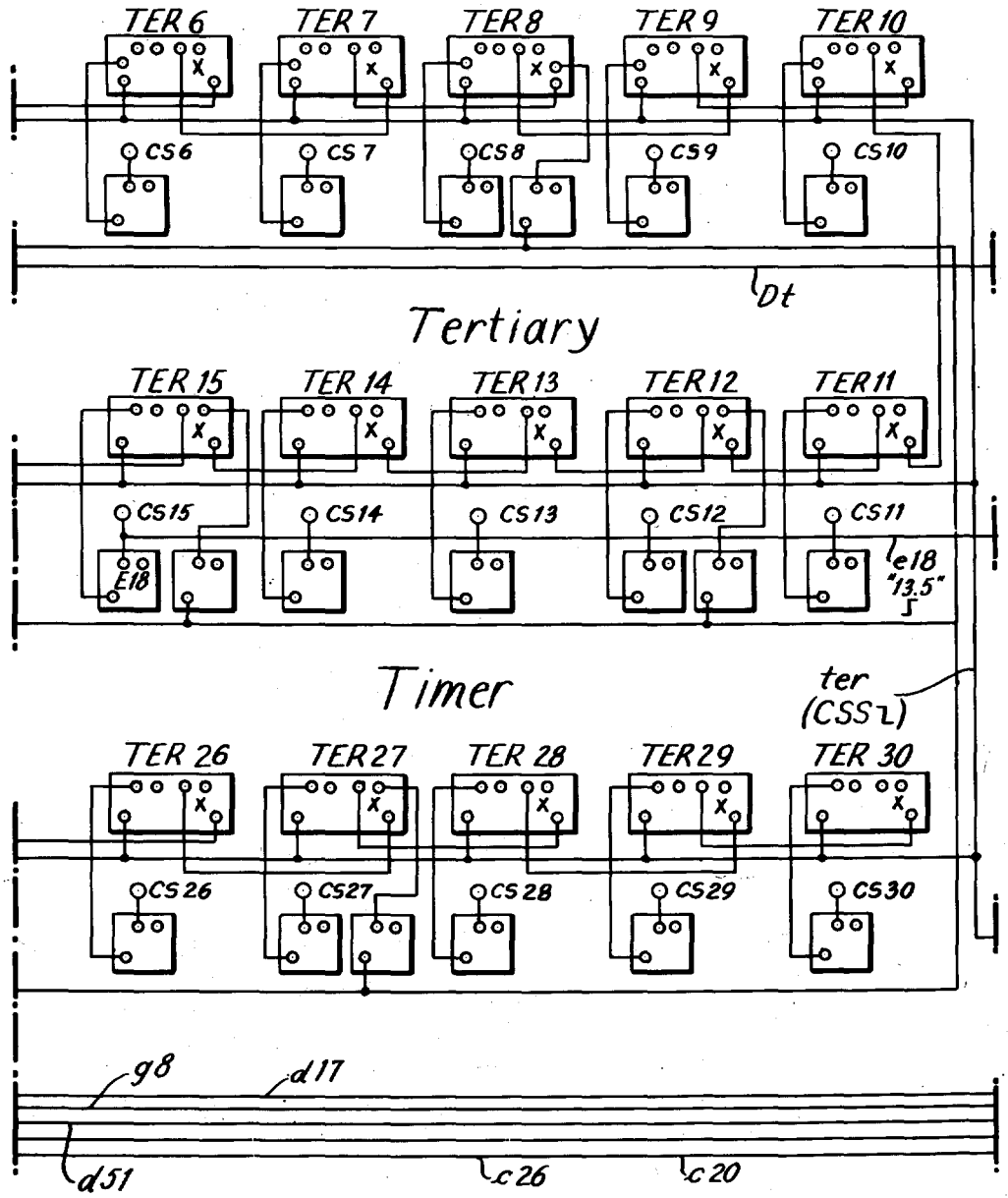

Fig. 65d.

INVENTORS
F.E. HAMILTON
R.R.SEEBER, Jr., R.A.ROWLEY
E.S.HUGHES, Jr.
BY J. Noblemn
ATTORNEY

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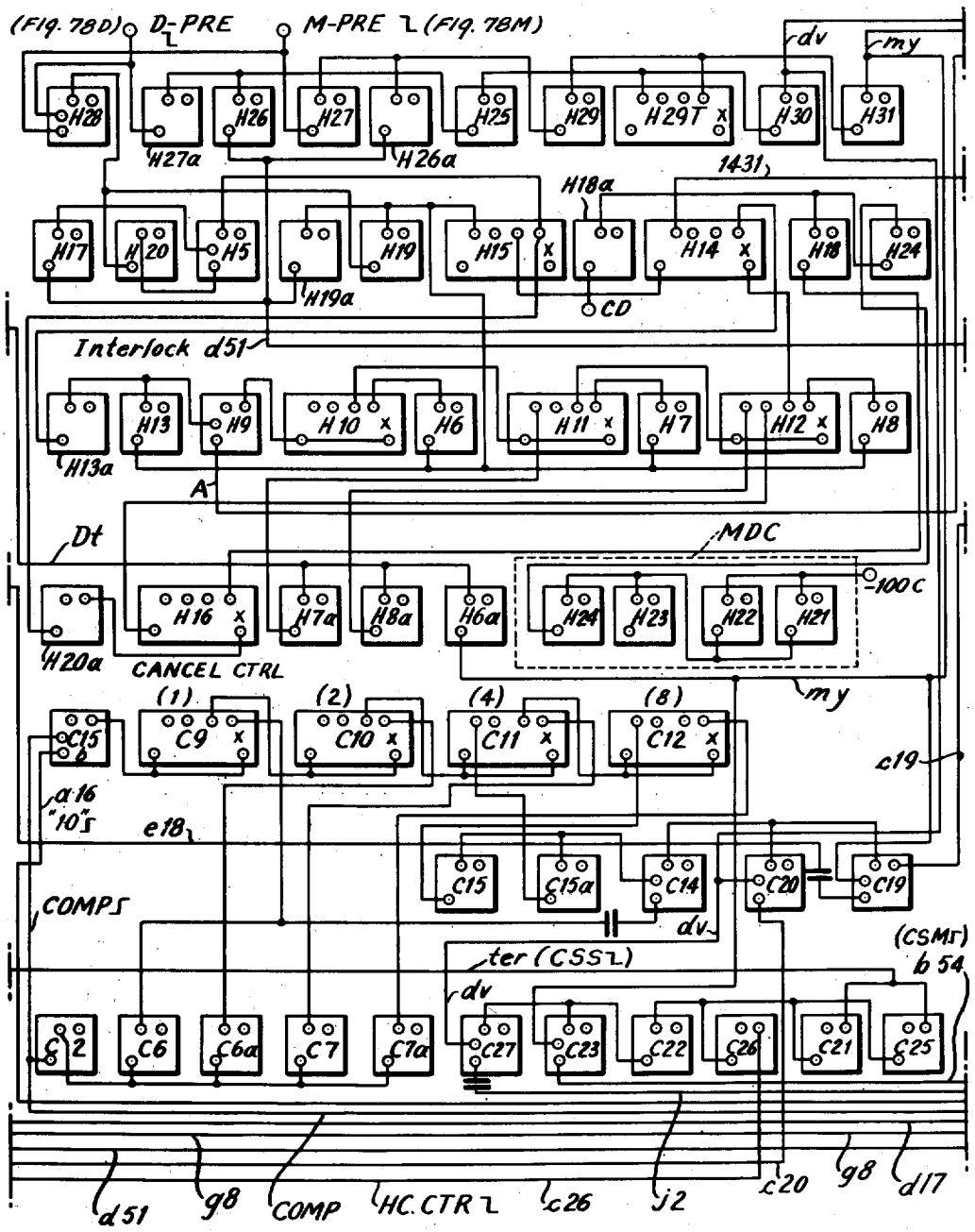

Fig. 65e.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.

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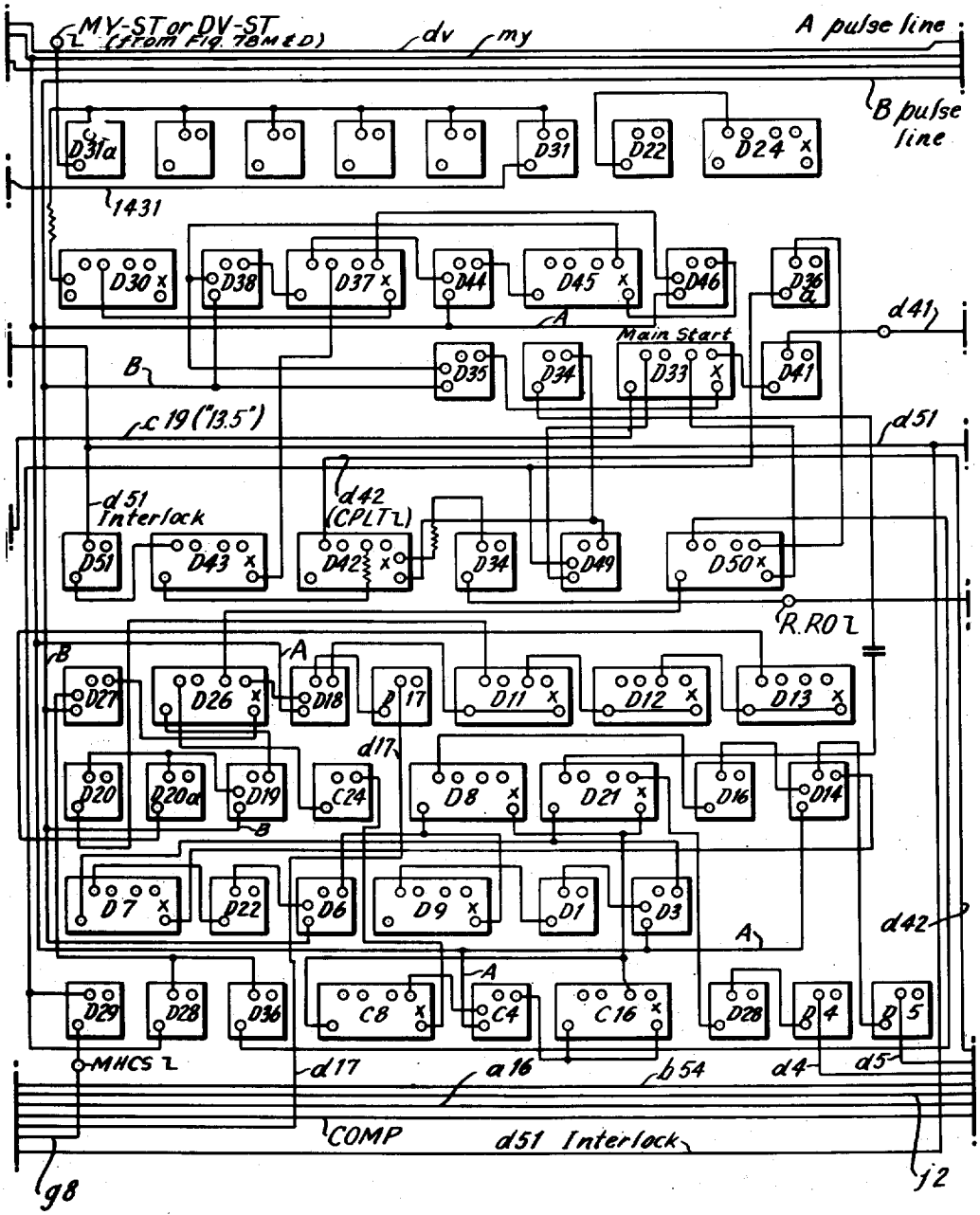

Fig. 65f.

INVENTORS
F. E. HAMILTON
R. R. SEEBER, Jr. R. A. ROWLEY
E. S. HUGHES, Jr.

BY
ATTORNEY

April 28, 1953 F. E. HAMILTON ET AL 2,636,672

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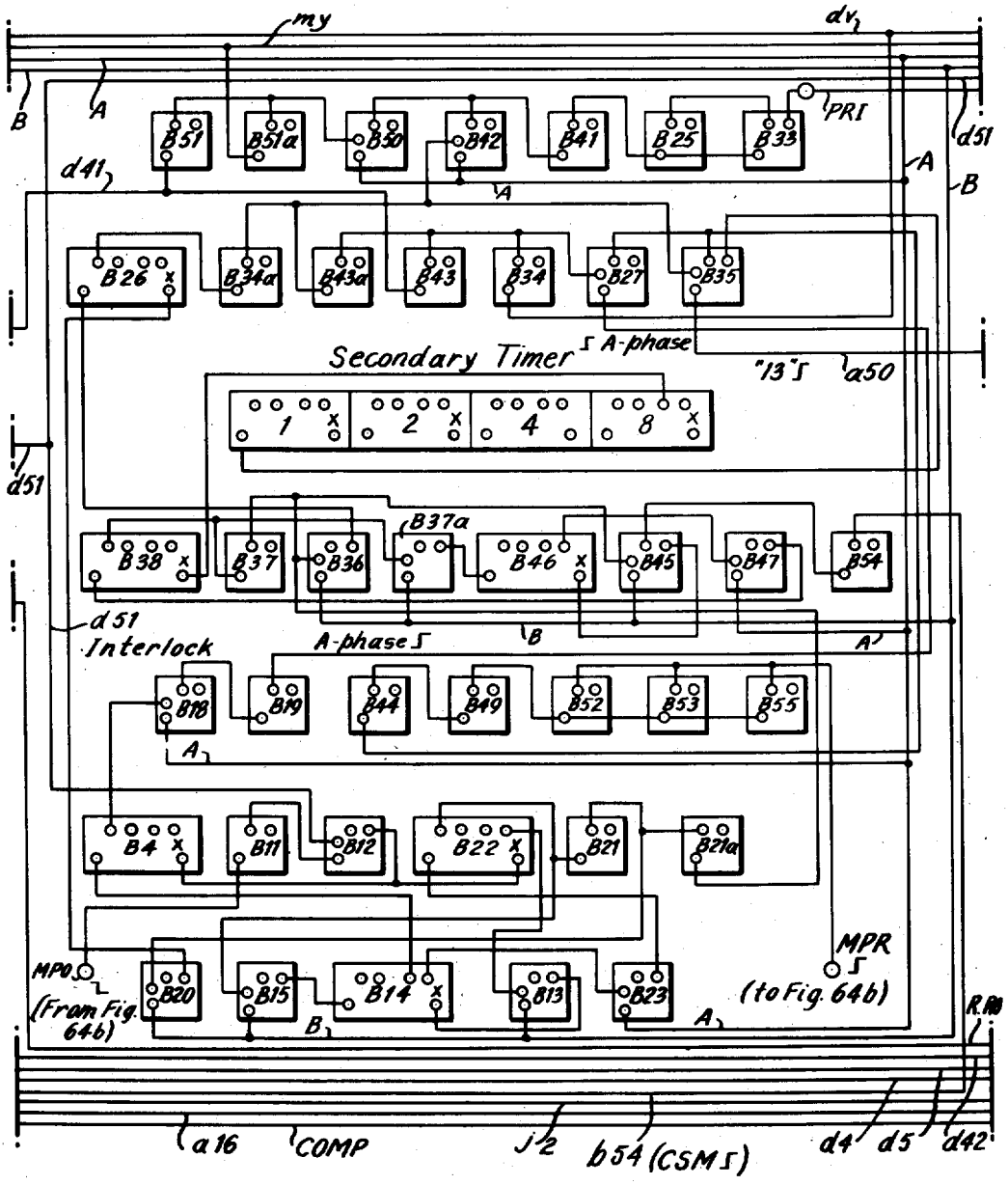

Fig. 65g.

INVENTORS
F.E. HAMILTON
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E.S. HUGHES, Jr.

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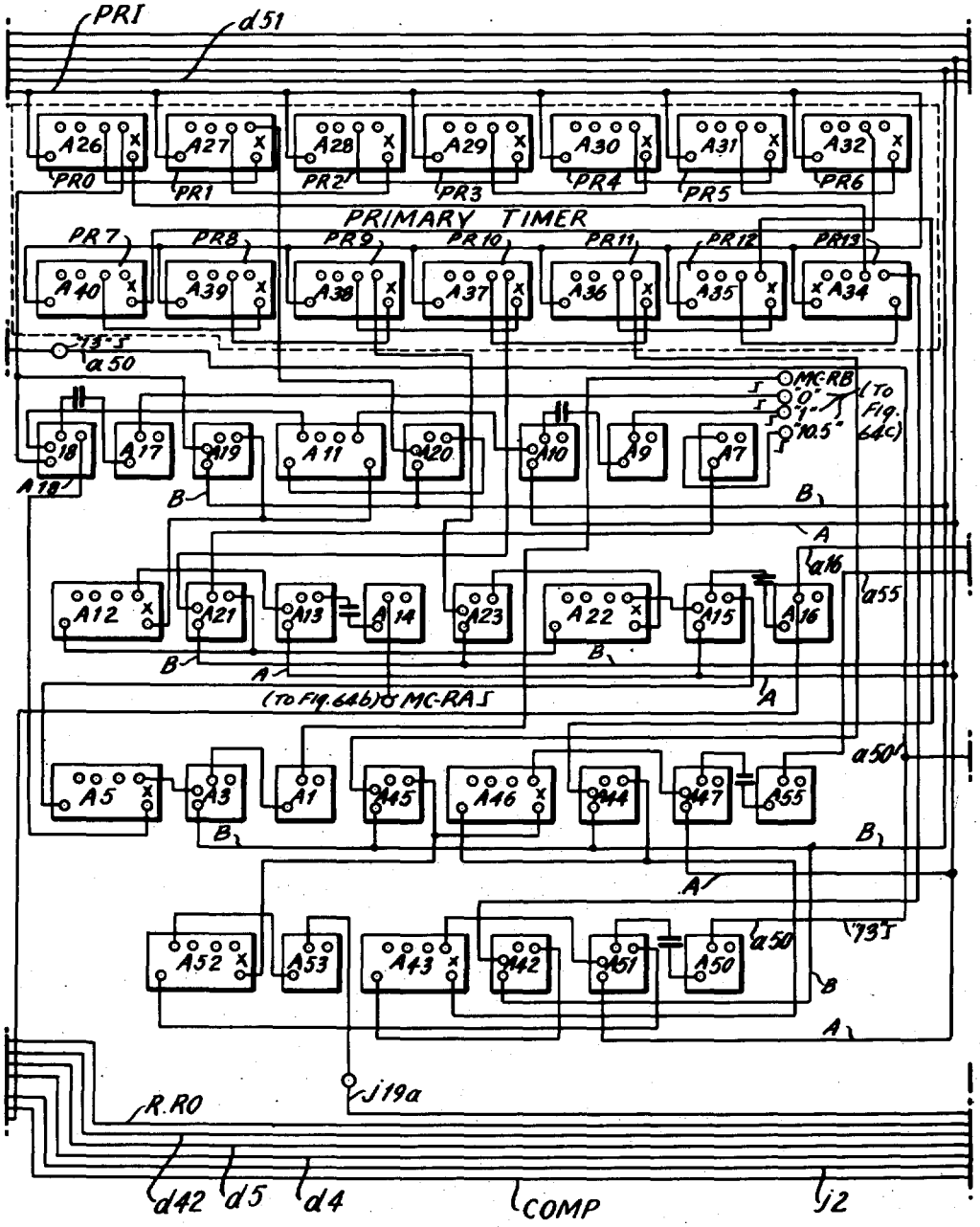

Fig. 65h.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.

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ATTORNEY

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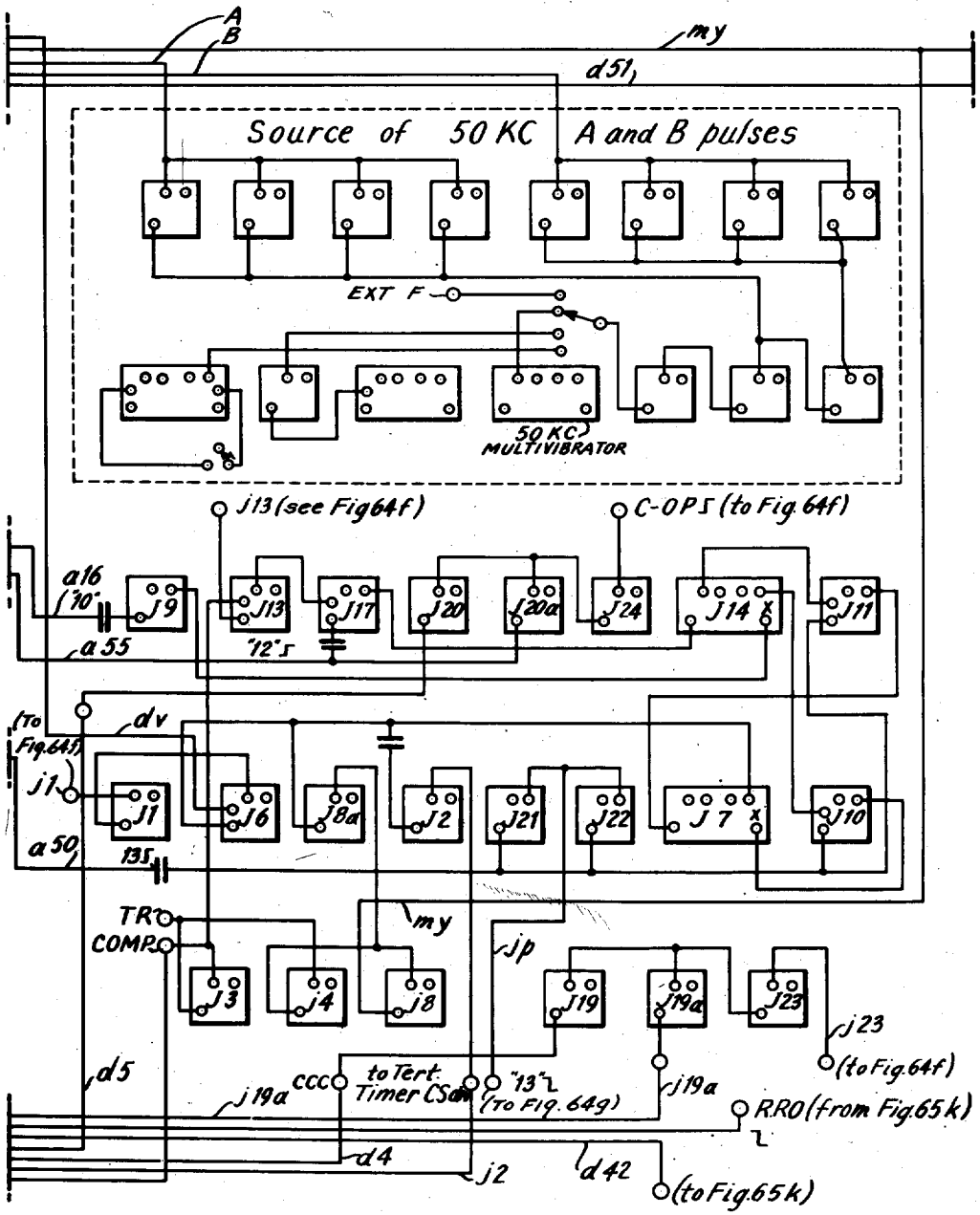

Fig. 65i.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.

BY J.J. Noble
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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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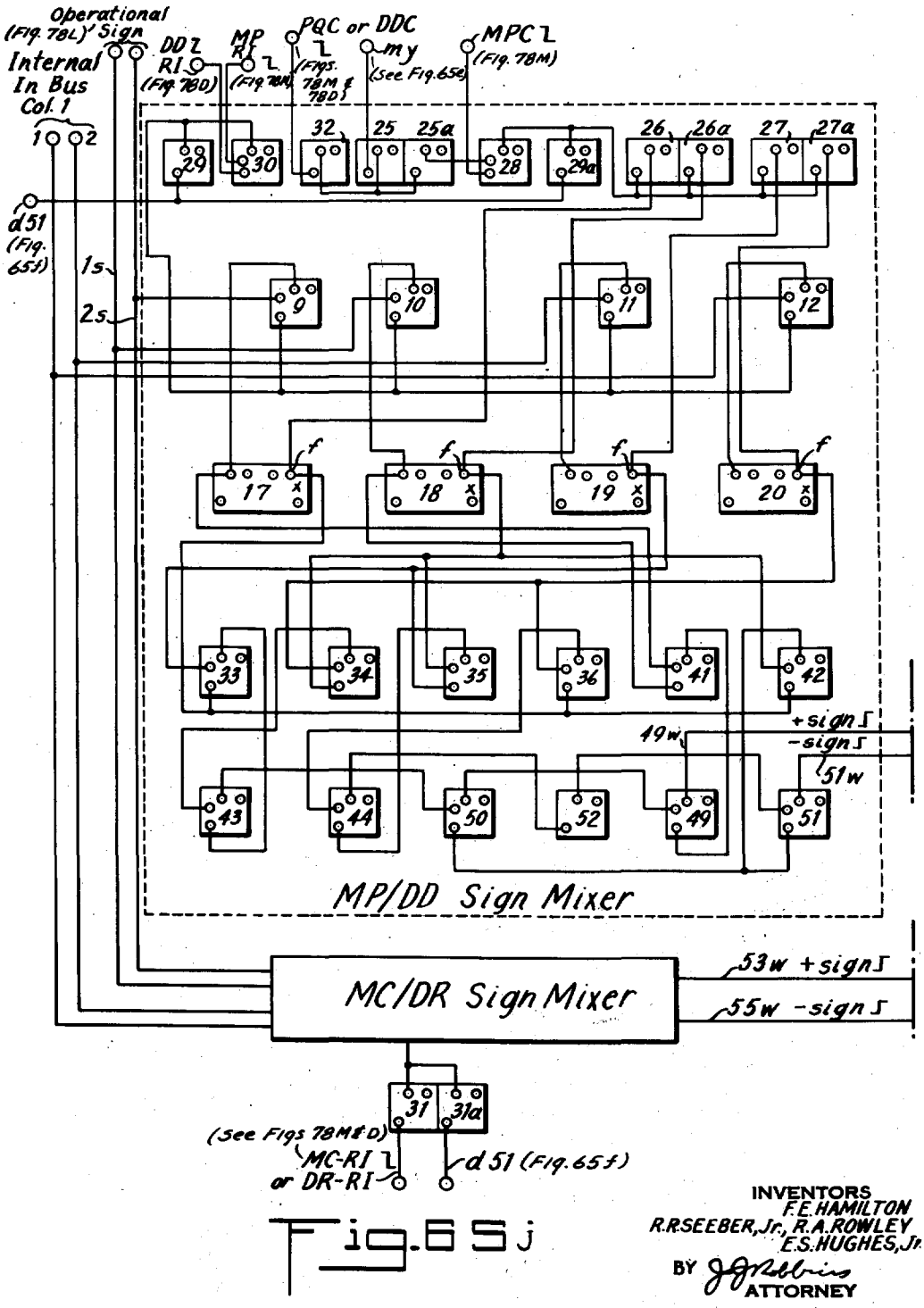

Fig. 65j

INVENTORS
F.E.HAMILTON
R.R.SEEBER, Jr., R.A.ROWLEY
E.S.HUGHES, Jr.
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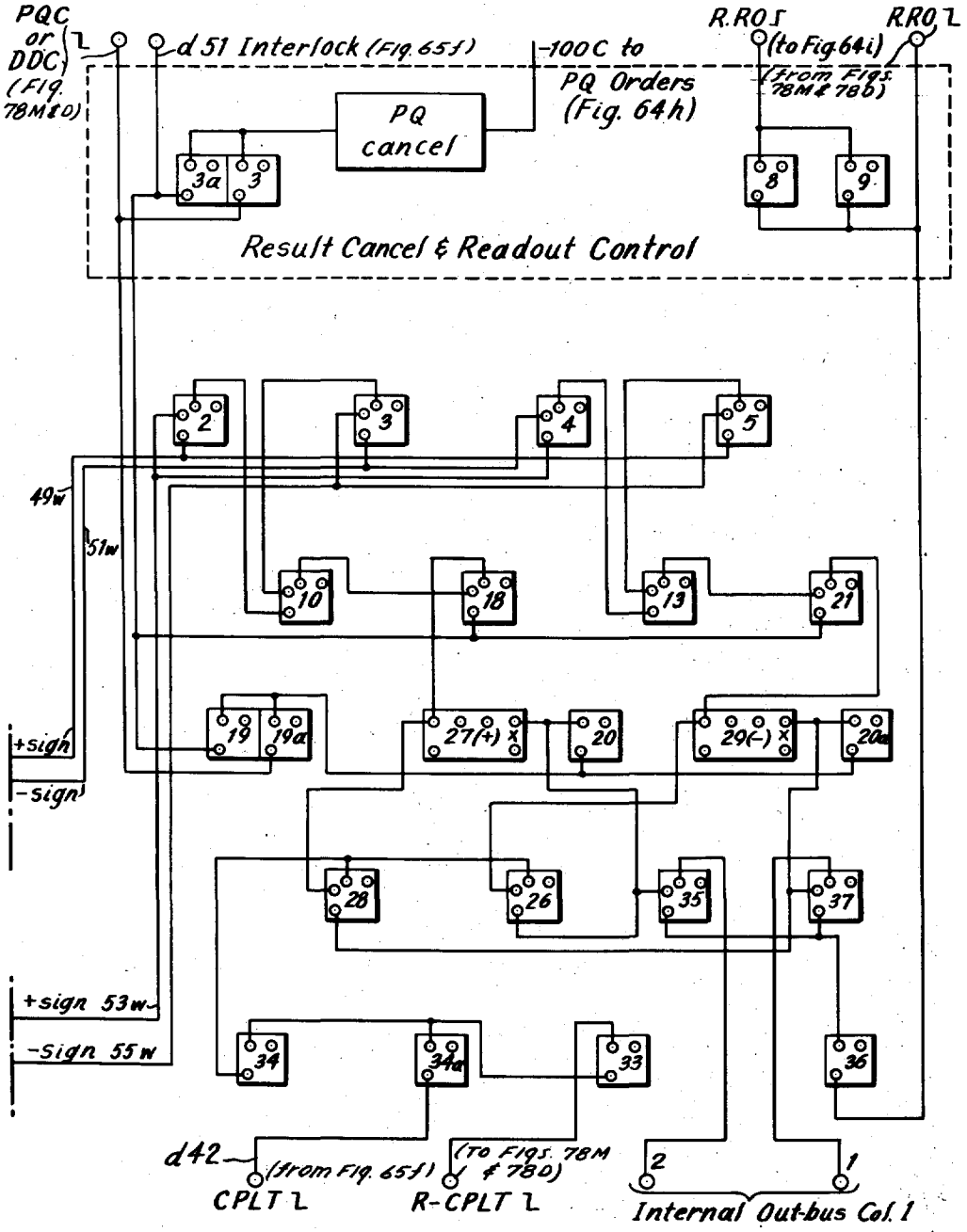

Fig 65k

INVENTORS
F.E.HAMILTON
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E.S.HUGHES,Jr.
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ATTORNEY

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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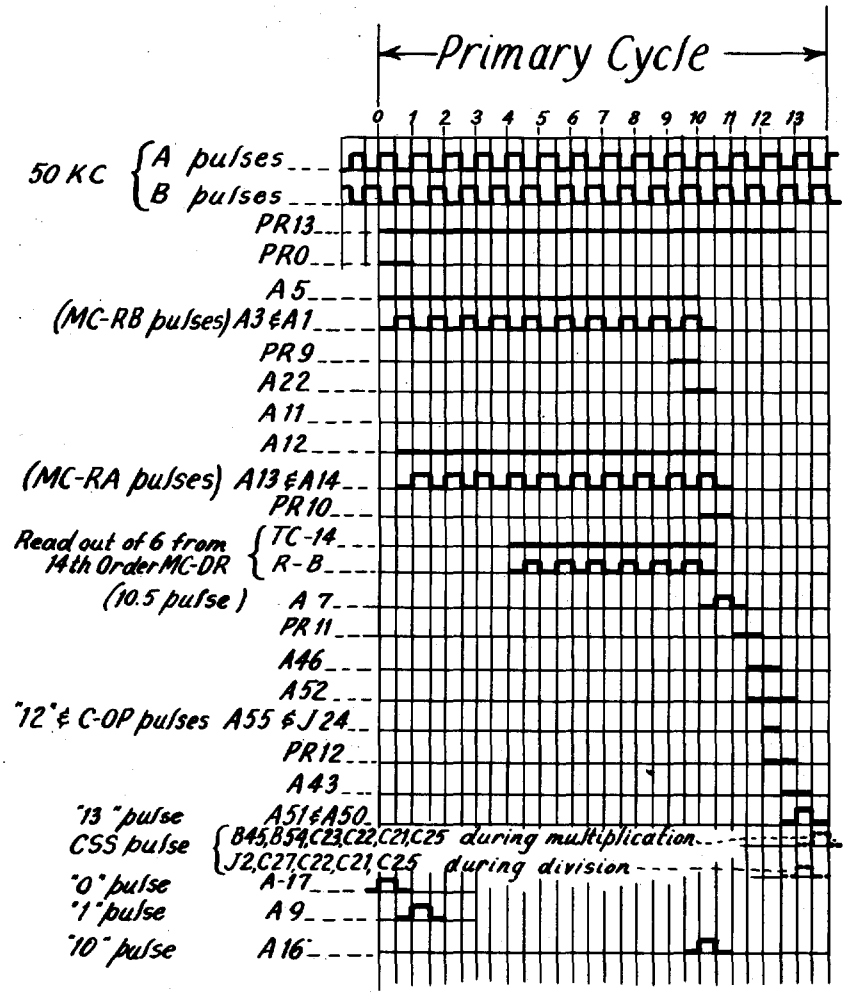

Fig. 66.

INVENTORS
F.E.HAMILTON
R.R.SEEBER,Jr., R.A.ROWLEY
E.S.HUGHES,Jr.
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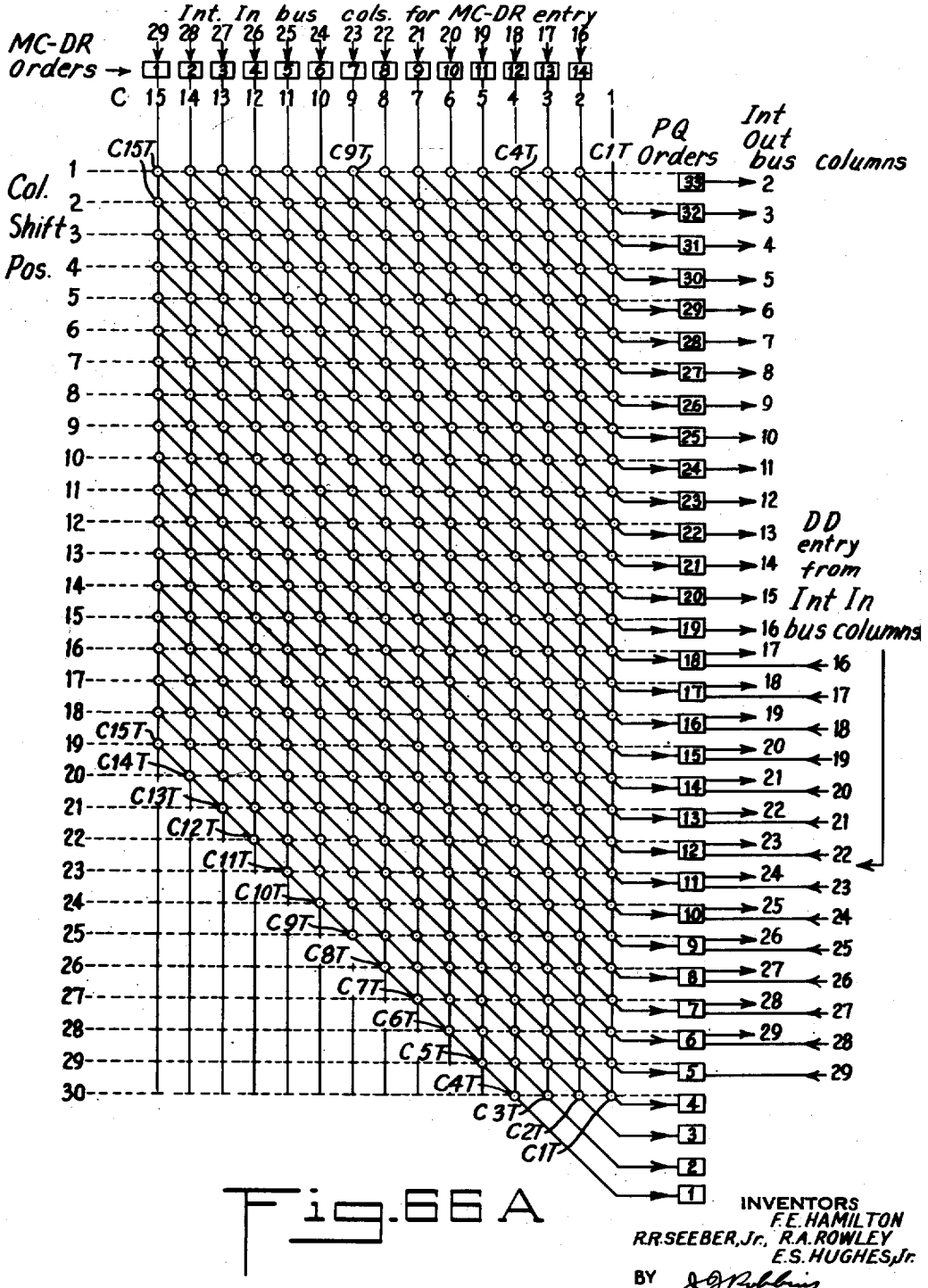

Fig. 66A

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.

BY J. J. Robbins
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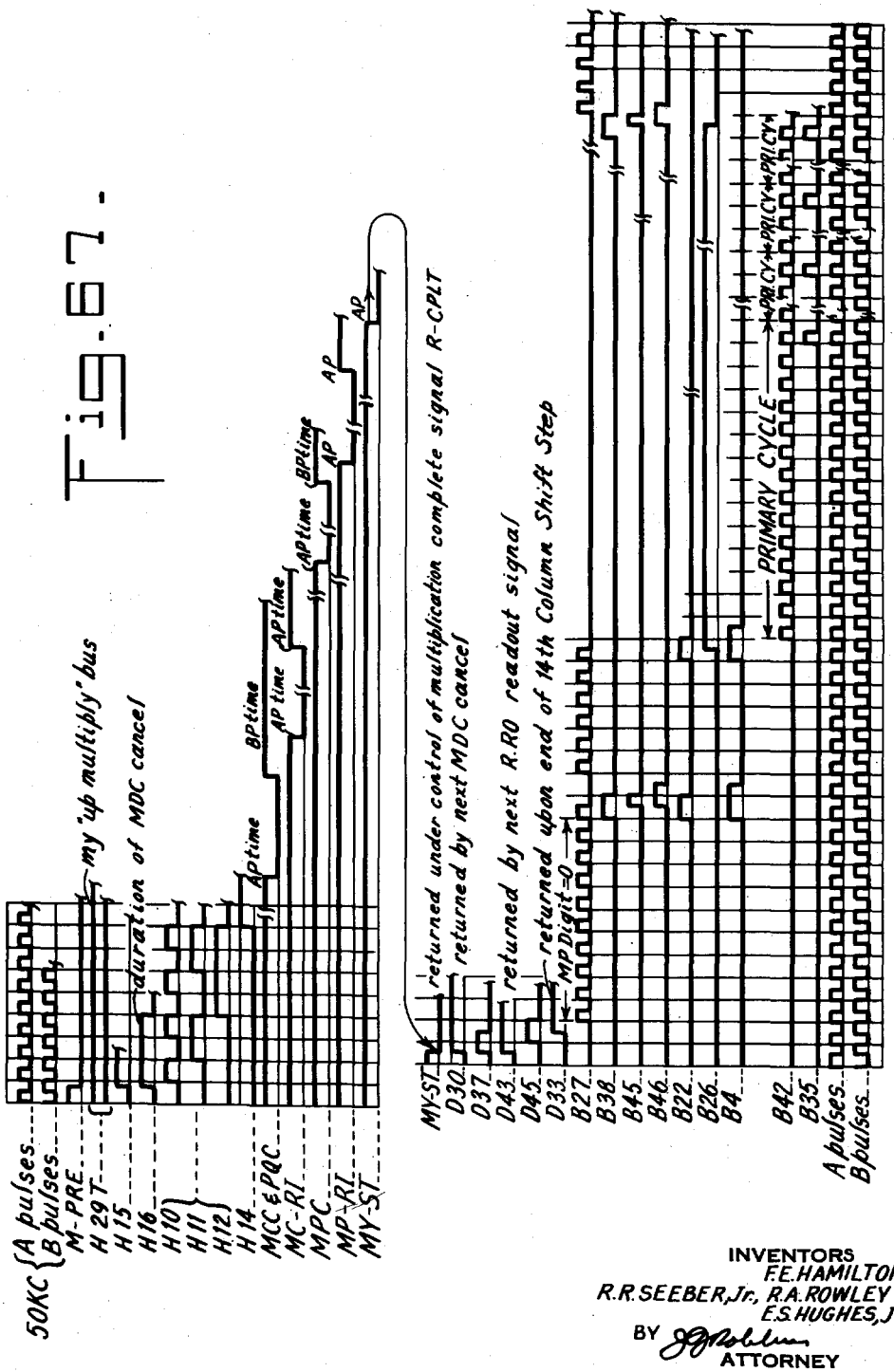
Fig. 67.



INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.
BY
ATTORNEY

Fig. 68.

Ex: 72 000 000 000 000 ÷ 00 000 000 000 200
Rightward Denominational Shift 24 with ½ correction

Col. shift pos.	14/0	13/0	12/0	11/0	10/0	9/0	8/0	7/0	6/0	5/0	4/0	3/2	2/0	1/0	MC/DR								PQ cycle
	33/0	32/0	31/0	30/0	29/0	28/0	27/0	26/0	25/0	24/0	23/0	22/0	21/0	20/0	19/0	18/7	17/2	16/0	15/0	14/0	13/0	-----	1/0
2	0	9	9	9	9	9	9	9	9	9	9	9	9	8	0	7	2	0	0	0	0	-----	0 comp
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	7	2	0	0	0	0	-----	0 true
3	0	0	9	9	9	9	9	9	9	9	9	9	9	9	8	7	2	0	0	0	0	-----	0 comp
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	7	2	0	0	0	0	-----	0 true
4	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	5	2	0	0	0	0	-----	0 comp
4	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	3	2	0	0	0	0	-----	0 comp
4	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	1	2	0	0	0	0	-----	0 comp
4	0	0	3	9	9	9	9	9	9	9	9	9	9	9	9	9	2	0	0	0	0	-----	0 comp
4	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	1	2	0	0	0	0	-----	0 true
5	0	0	3	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	-----	0 comp
5	0	0	3	2	0	0	0	0	0	0	0	0	0	0	0	0	8	0	0	0	0	-----	0 comp
5	0	0	3	3	0	0	0	0	0	0	0	0	0	0	0	0	6	0	0	0	0	-----	0 comp
5	0	0	3	4	0	0	0	0	0	0	0	0	0	0	0	0	4	0	0	0	0	-----	0 comp
5	0	0	3	5	0	0	0	0	0	0	0	0	0	0	0	0	2	0	0	0	0	-----	0 comp
5	0	0	3	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-----	0 comp
5	0	0	3	6	9	9	9	9	9	9	9	9	9	9	9	9	8	0	0	0	0	-----	0 comp
5	0	0	3	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-----	0 true
6	0	0	3	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-----	0
½ correction					5																		
Quotient	0	0	3	6	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-----	0

Quotient after denominational shift of 24 to right — Den. shift Cols. 28/0 27/0 ---- 6/0 5/0 4/0 3/0 2/3 1/6

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr.
R.A. ROWLEY
E.S. HUGHES, Jr.
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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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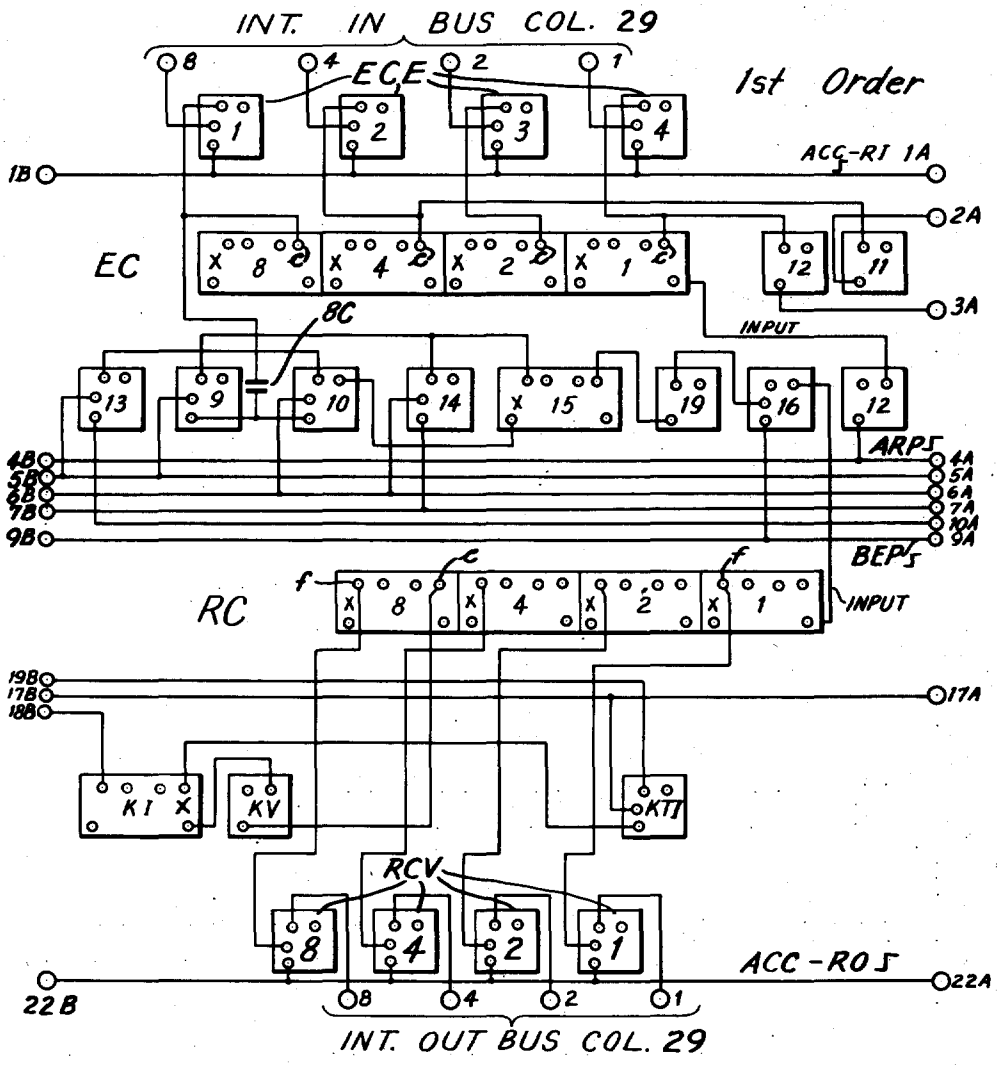

Fig. 69a.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.
BY J. O. Hobbins
ATTORNEY

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 82

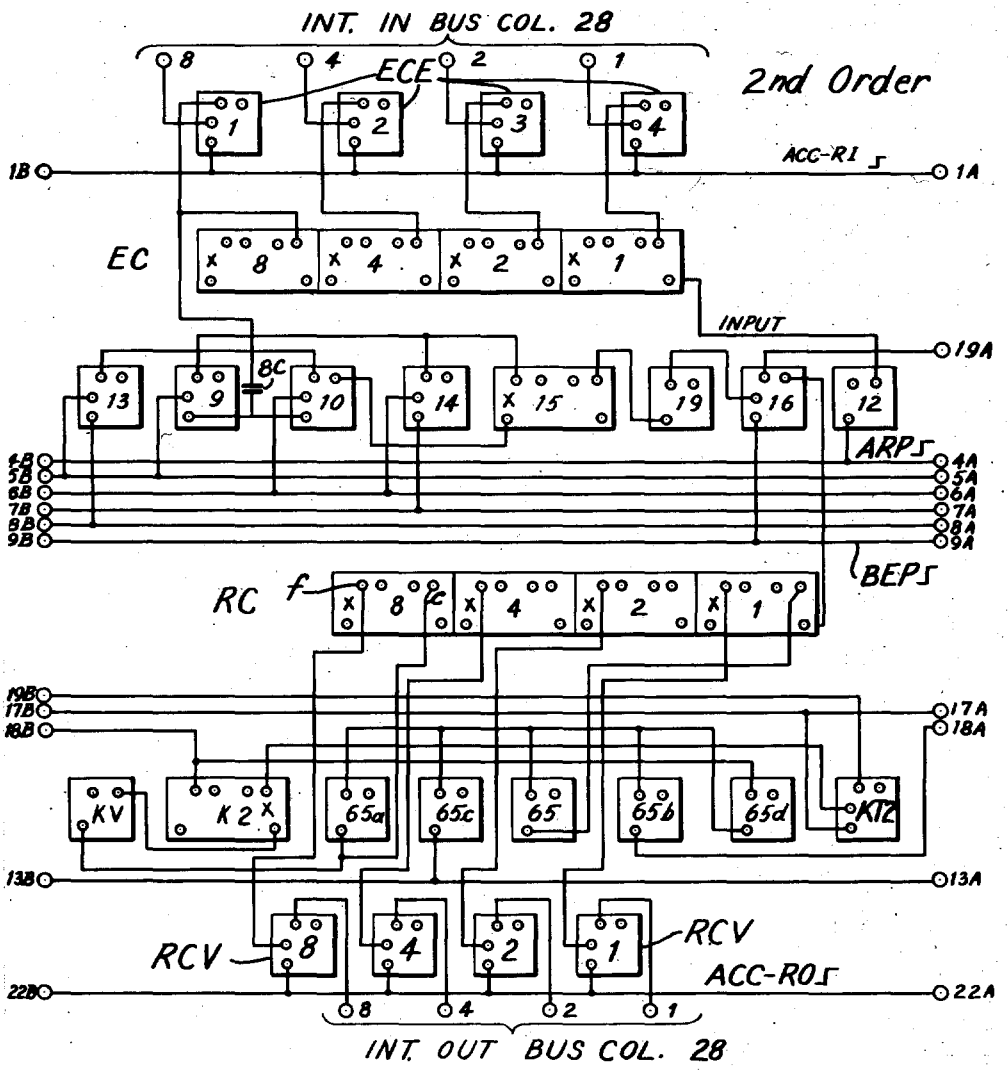

Fig. 69b.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.
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April 28, 1953 F. E. HAMILTON ET AL 2,636,672

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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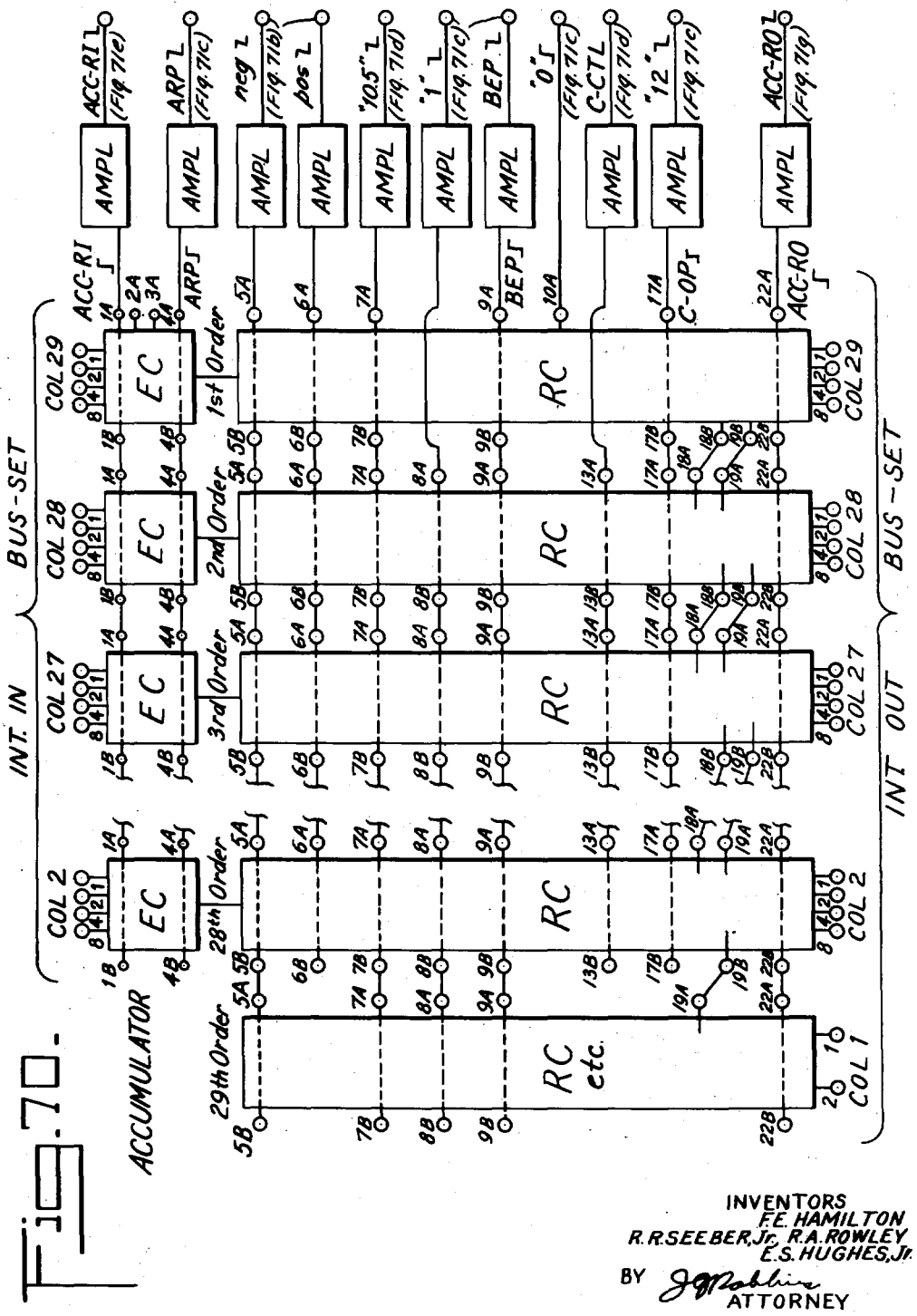

Fig. 70.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr. R.A. ROWLEY
E.S. HUGHES, Jr.
BY J.G. Mabbins
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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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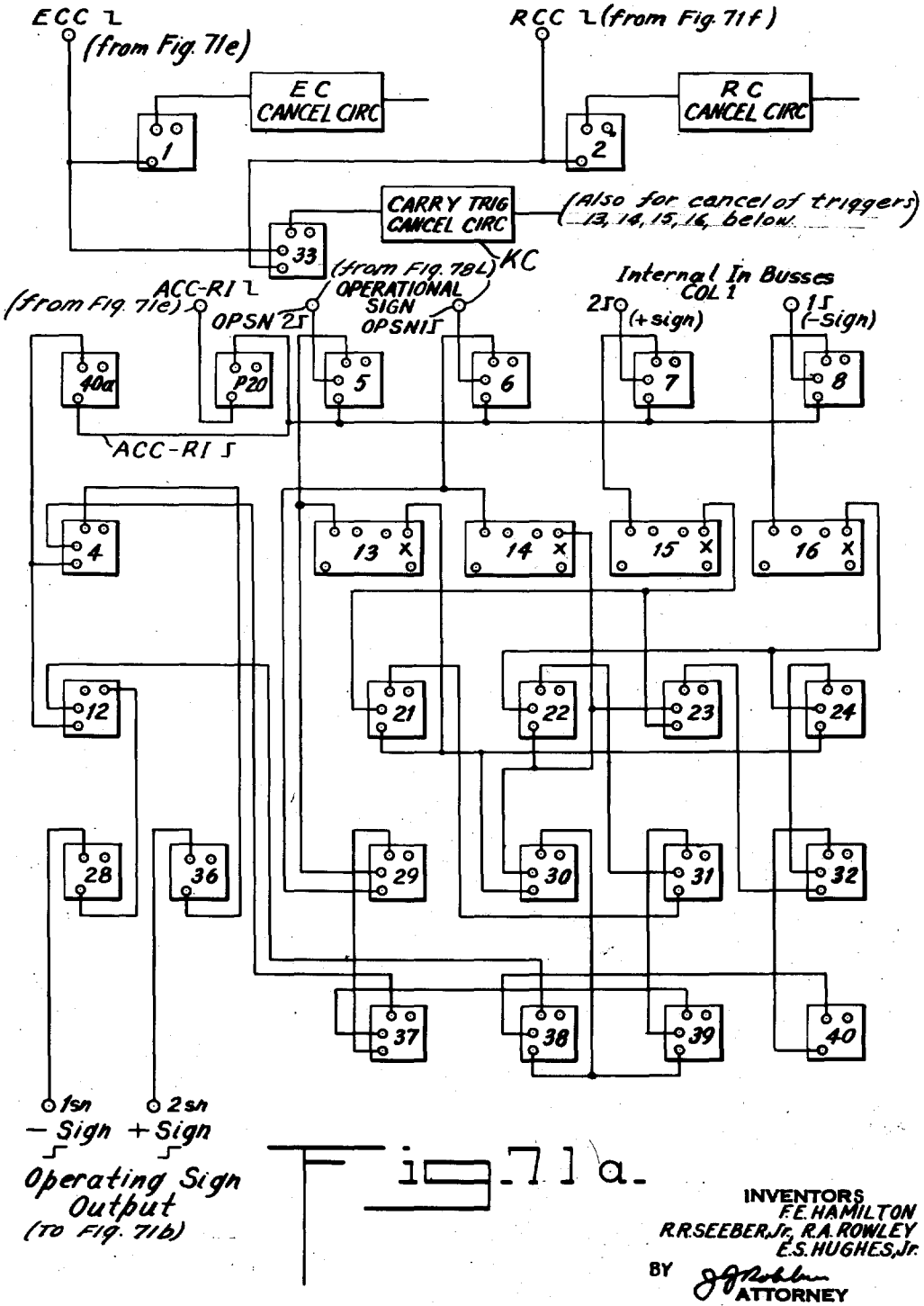

Fig. 71a.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr.
R.A. ROWLEY
E.S. HUGHES, Jr.
BY
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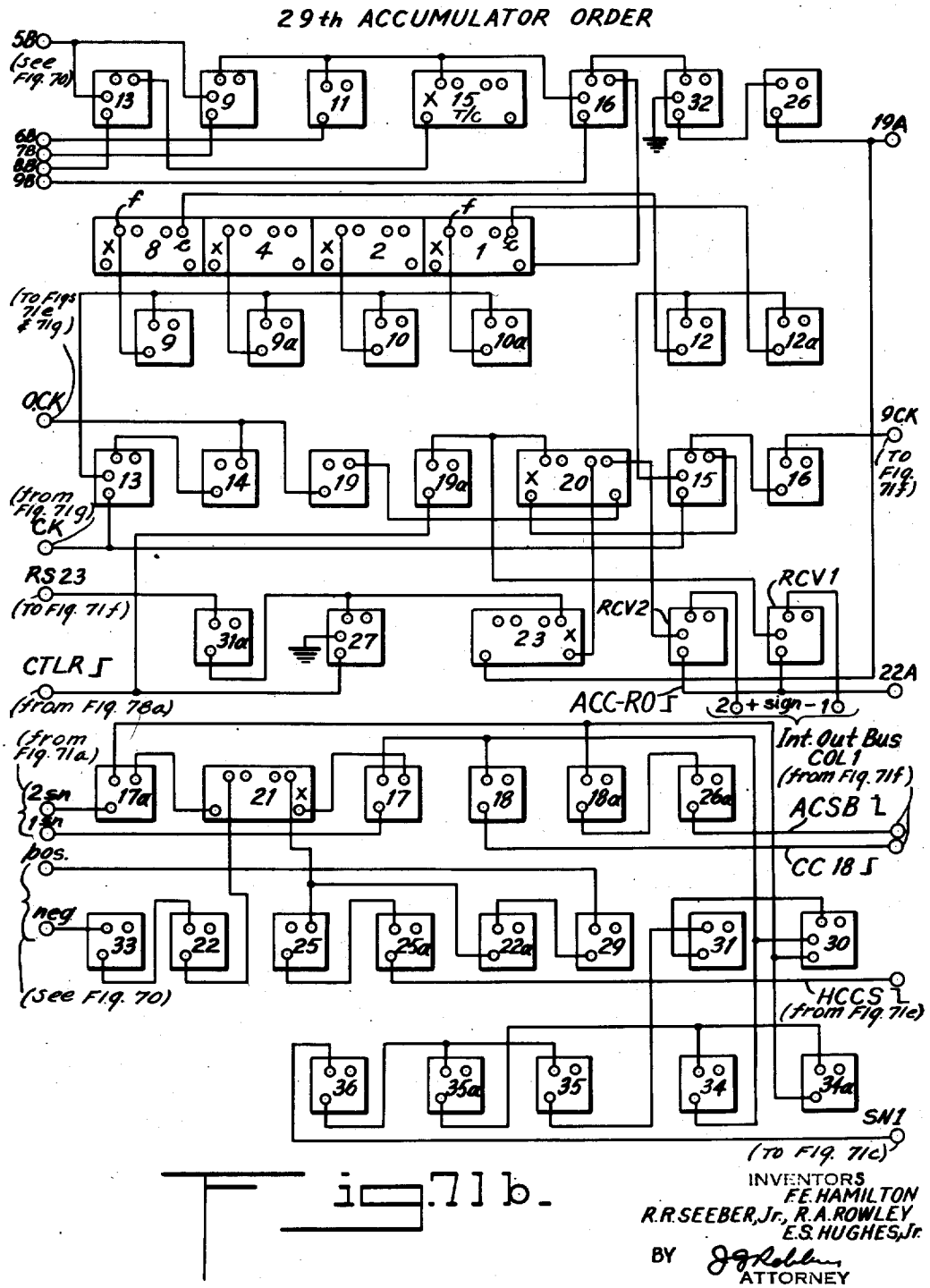

Fig. 71b.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.
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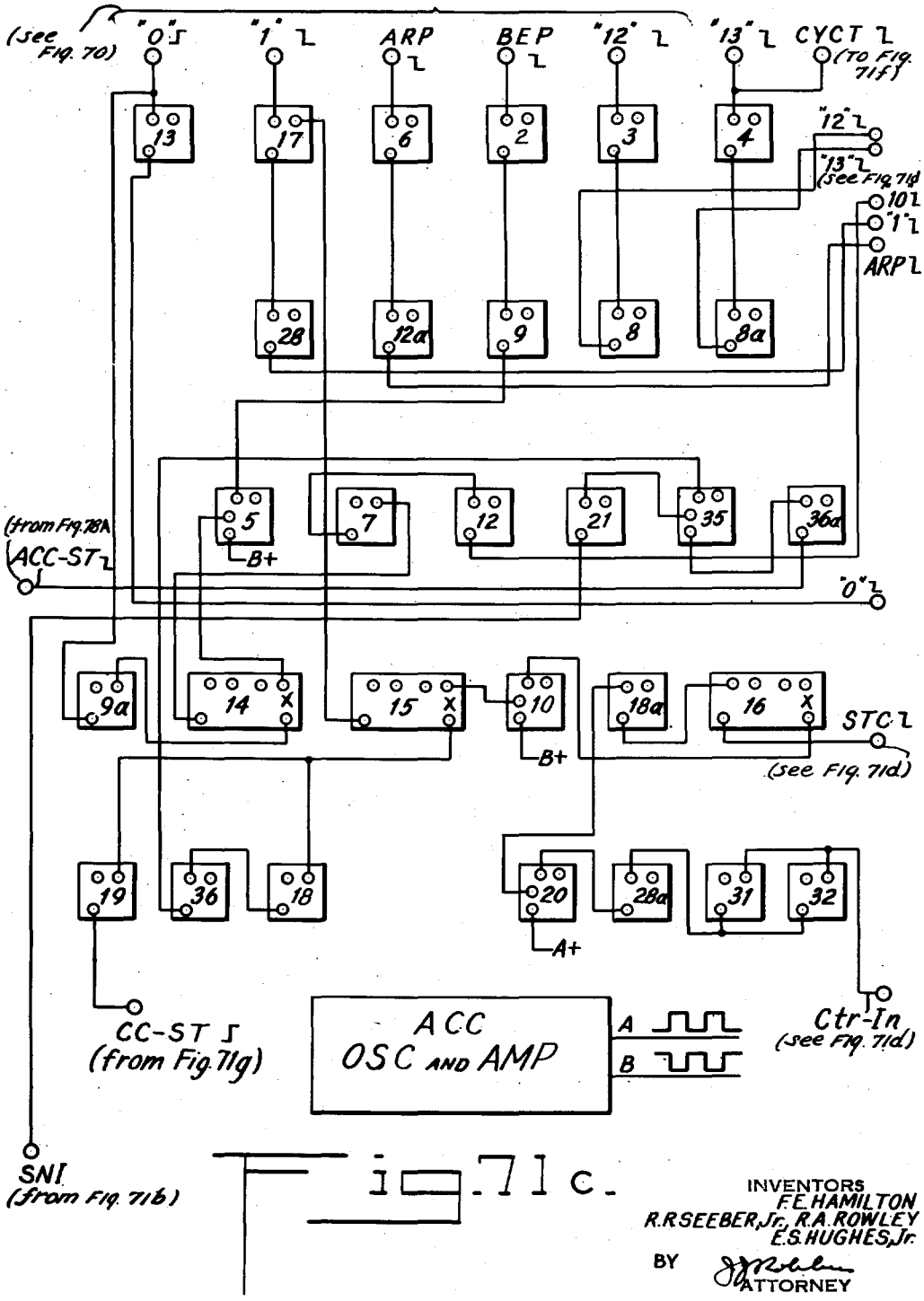

Fig. 71c.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr.
R.A. ROWLEY
E.S. HUGHES, Jr.

BY
ATTORNEY

April 28, 1953 F. E. HAMILTON ET AL 2,636,672

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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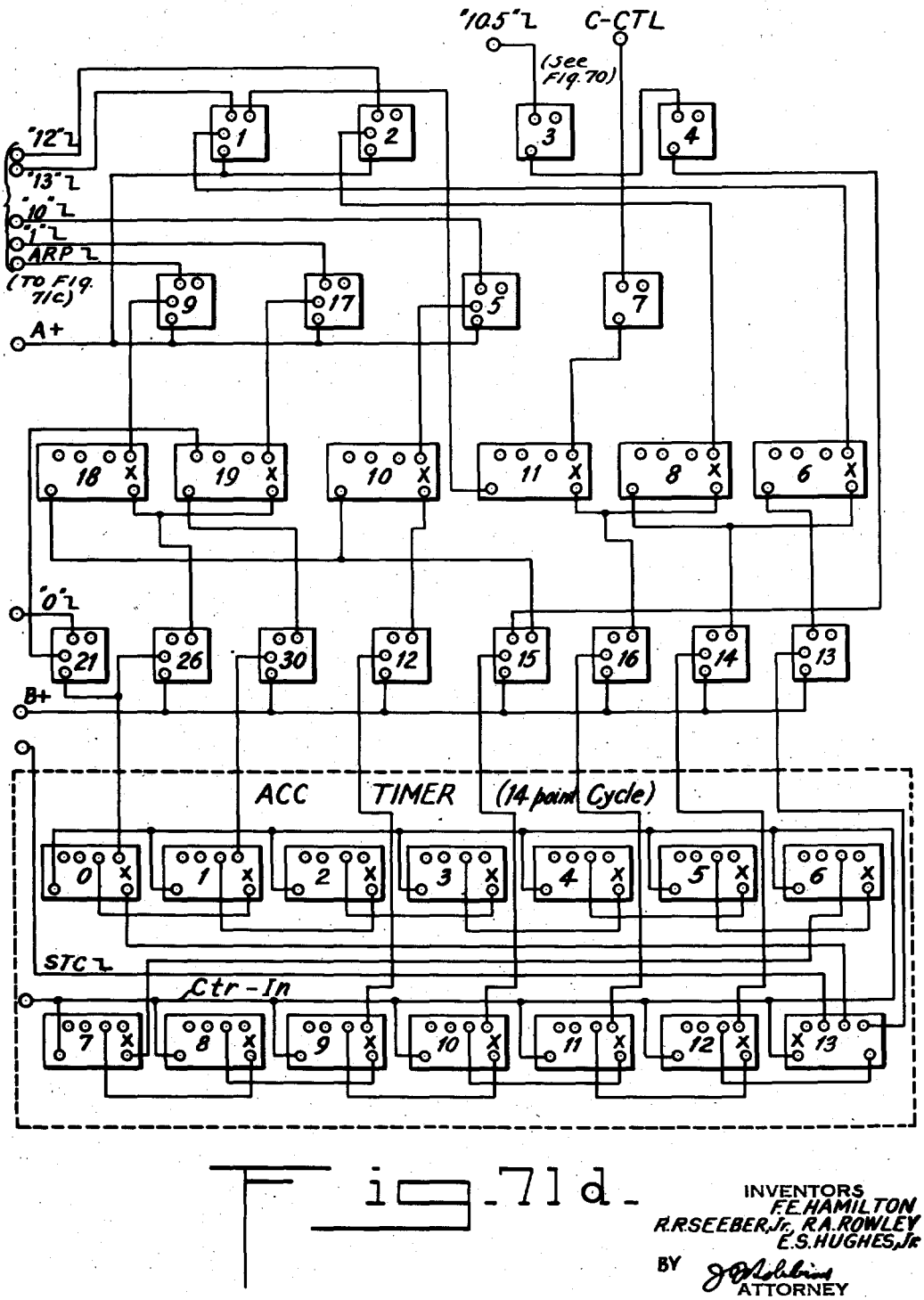

Fig. 71d.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr. R.A. ROWLEY
E.S. HUGHES, Jr.
BY J. P. Laboon
ATTORNEY

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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

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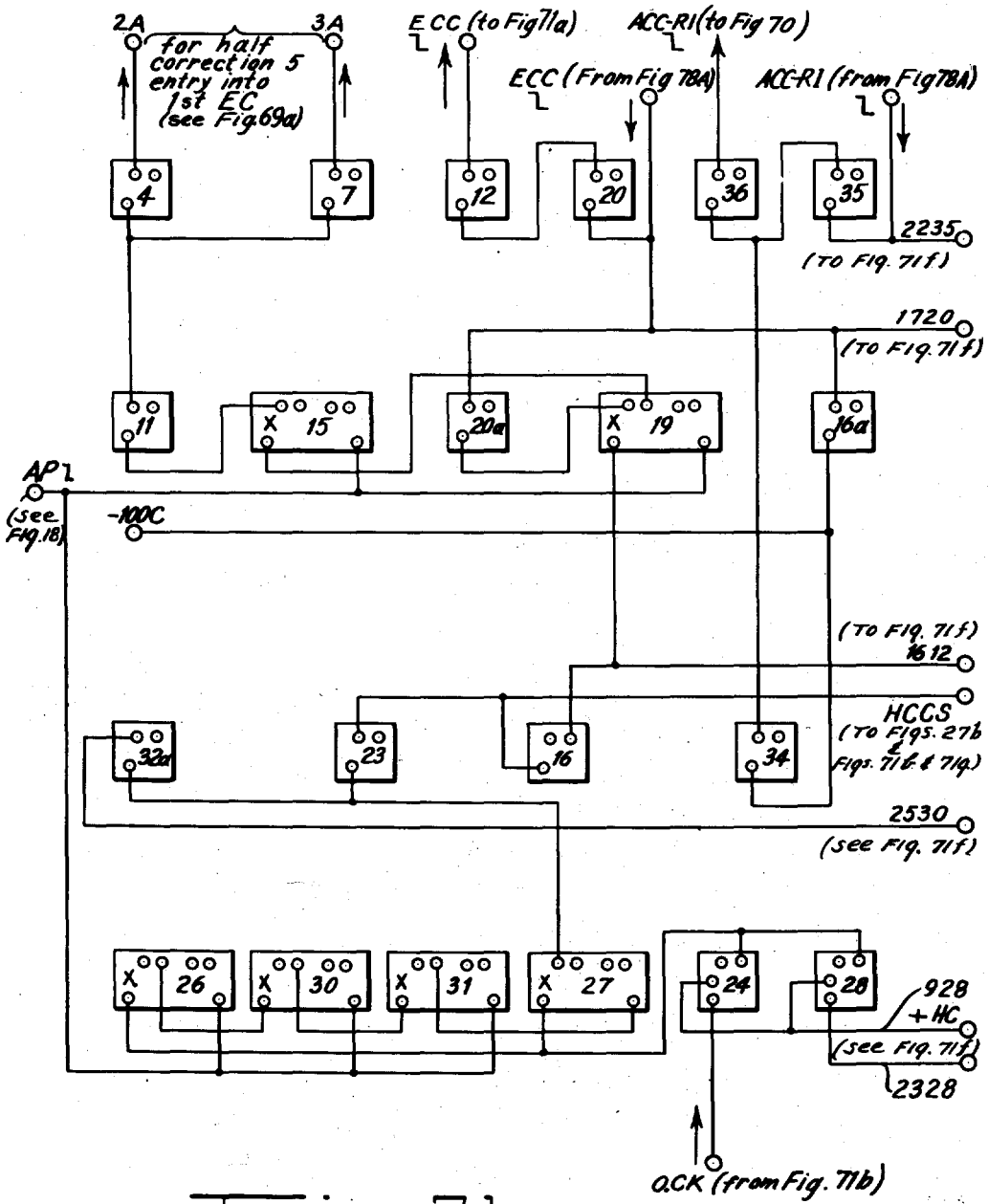

Fig. 71e.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.
BY J. G. Nobles
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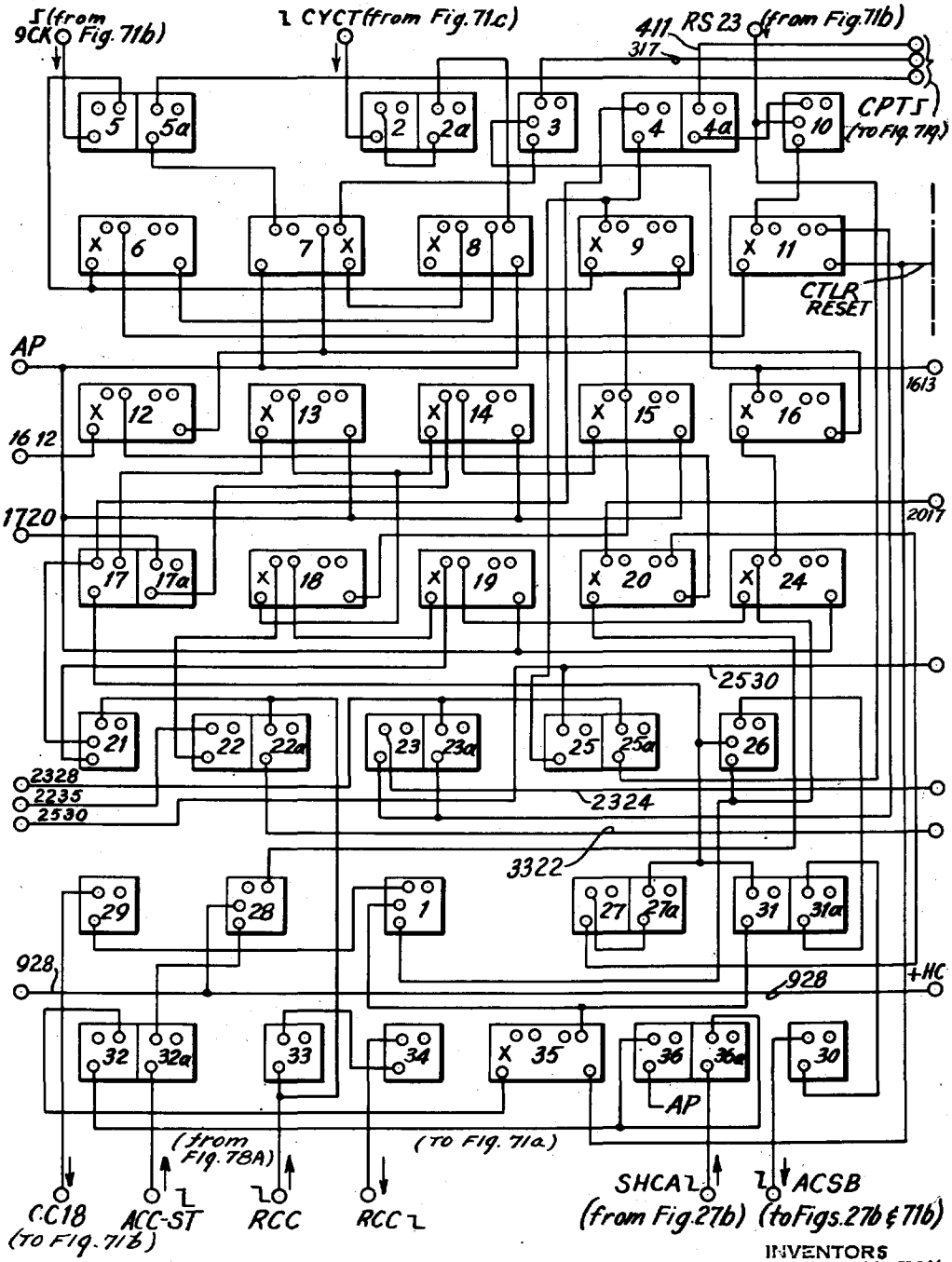

Fig. 71f.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr. R.A. ROWLEY
E.S. HUGHES, Jr.

BY J. G. Mallin
ATTORNEY

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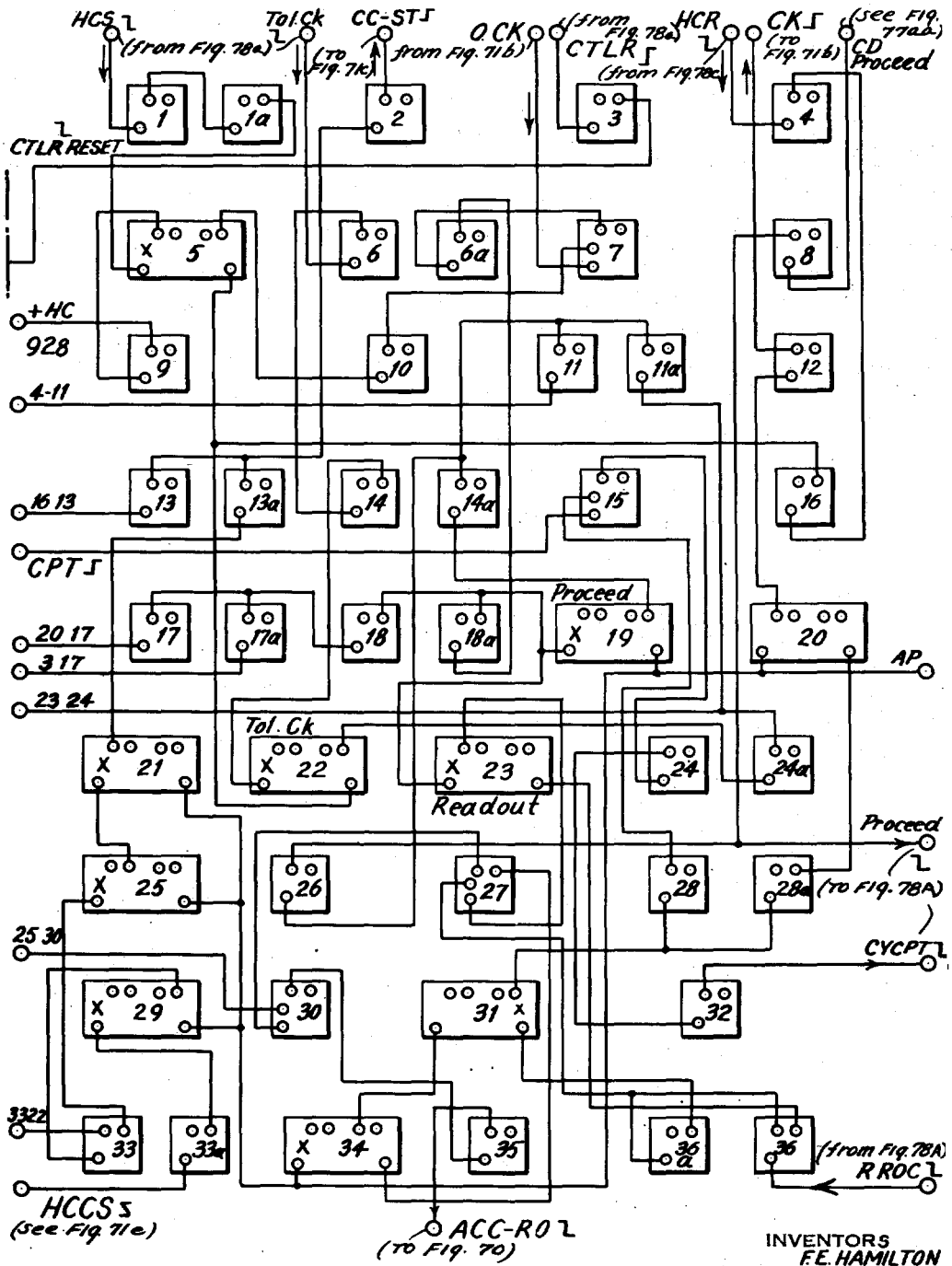

Fig. 71g.

INVENTORS
F. E. HAMILTON
R. R. SEEBER, Jr., R. A. ROWLEY
E. S. HUGHES, Jr.
BY J. J. Nebling
ATTORNEY

ACCUMULATOR CYCLE

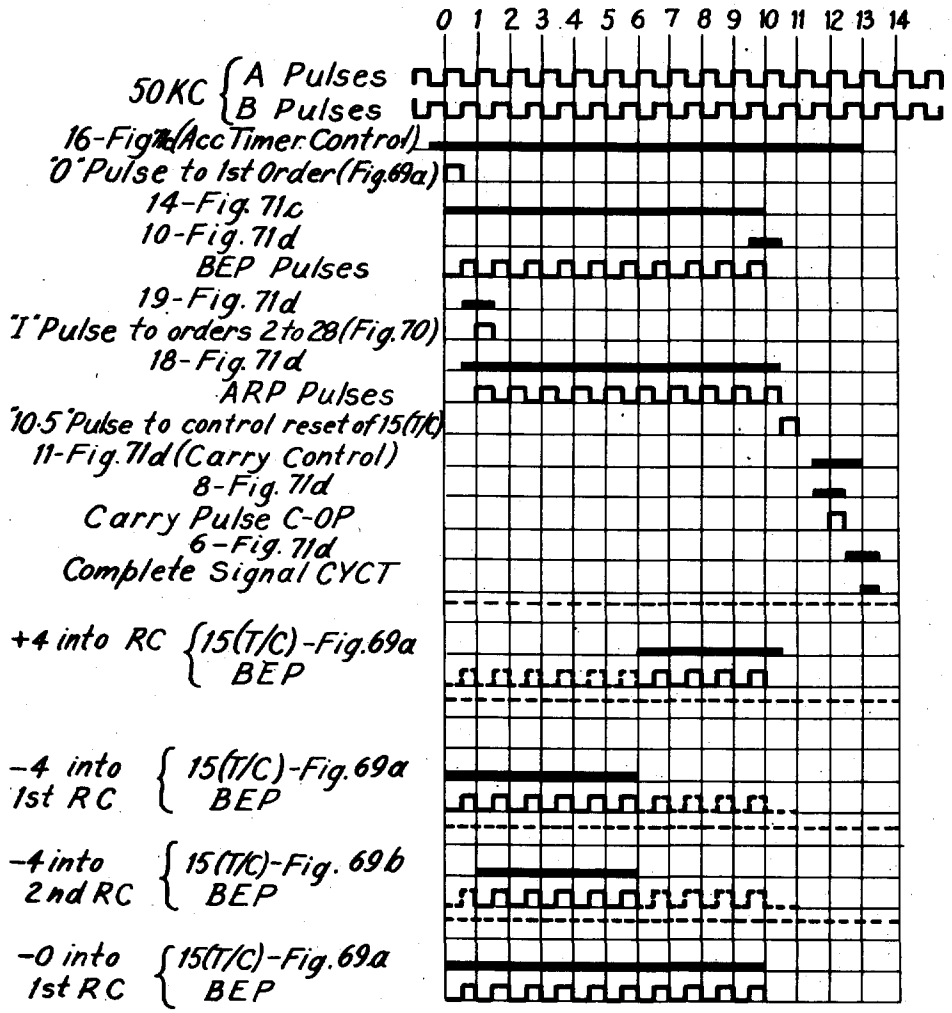

Fig. 72.

INVENTORS
F.E. HAMILTON
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E.S. HUGHES, Jr.
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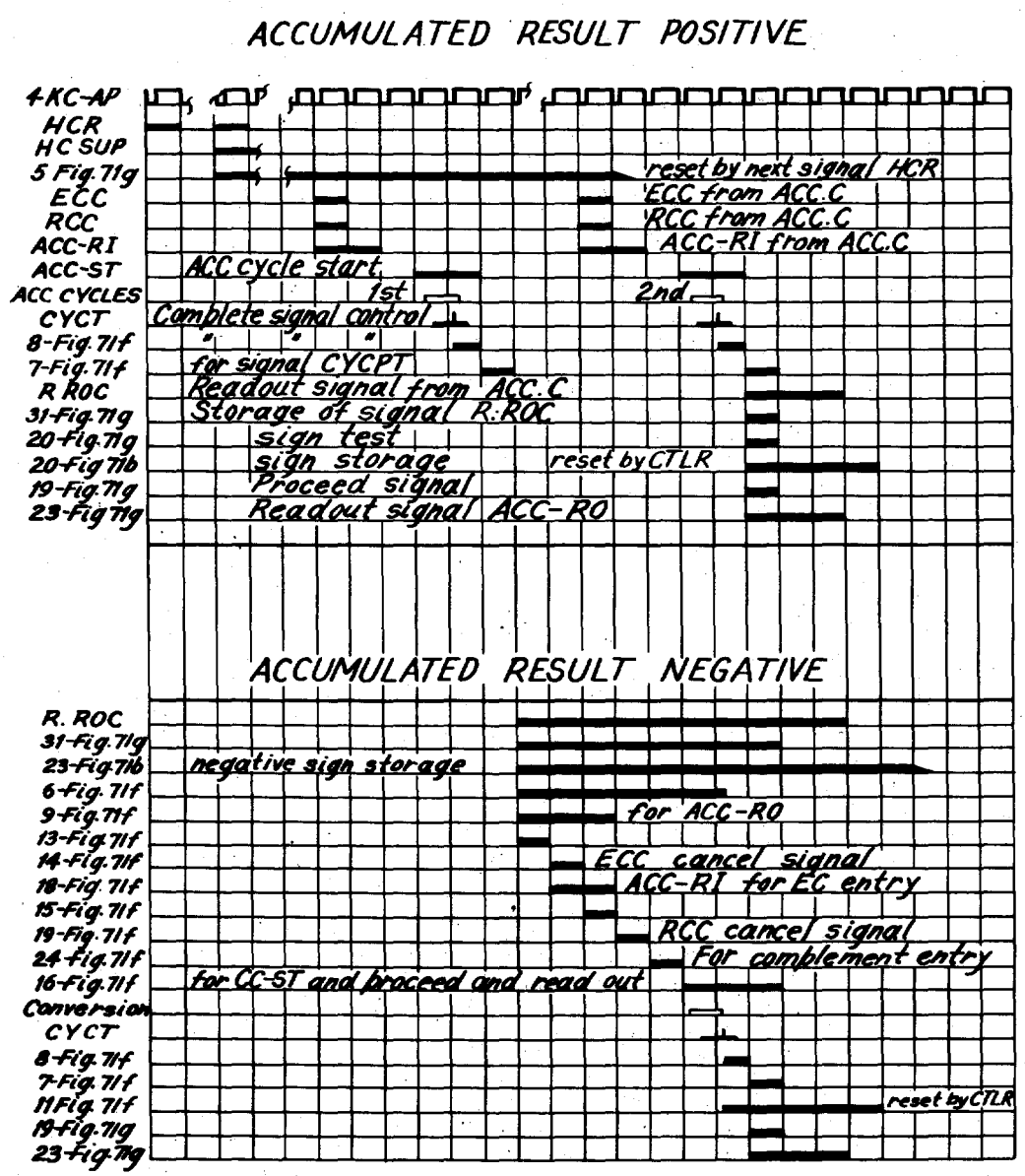

Fig. 73.

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R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.
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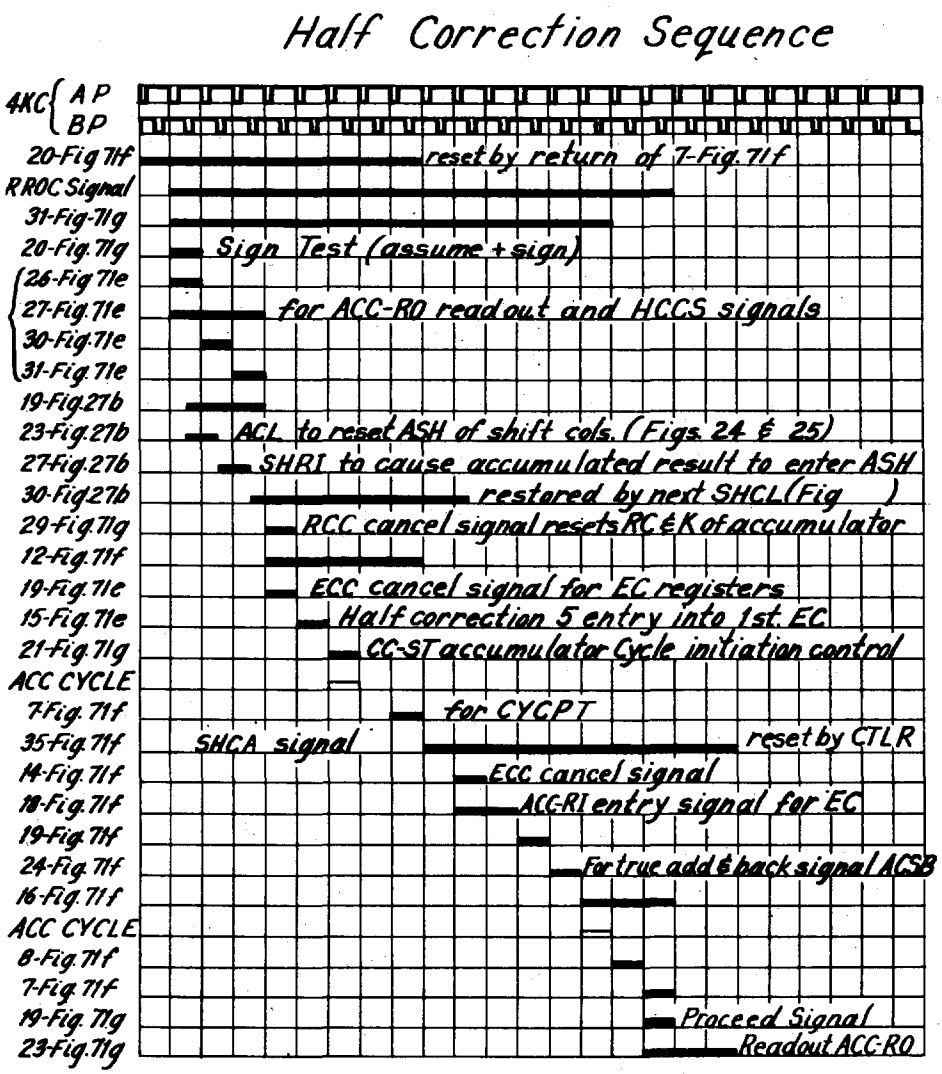

Fig. 74.

INVENTORS
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R.R. SEEBER, Jr., R.A. ROWLEY
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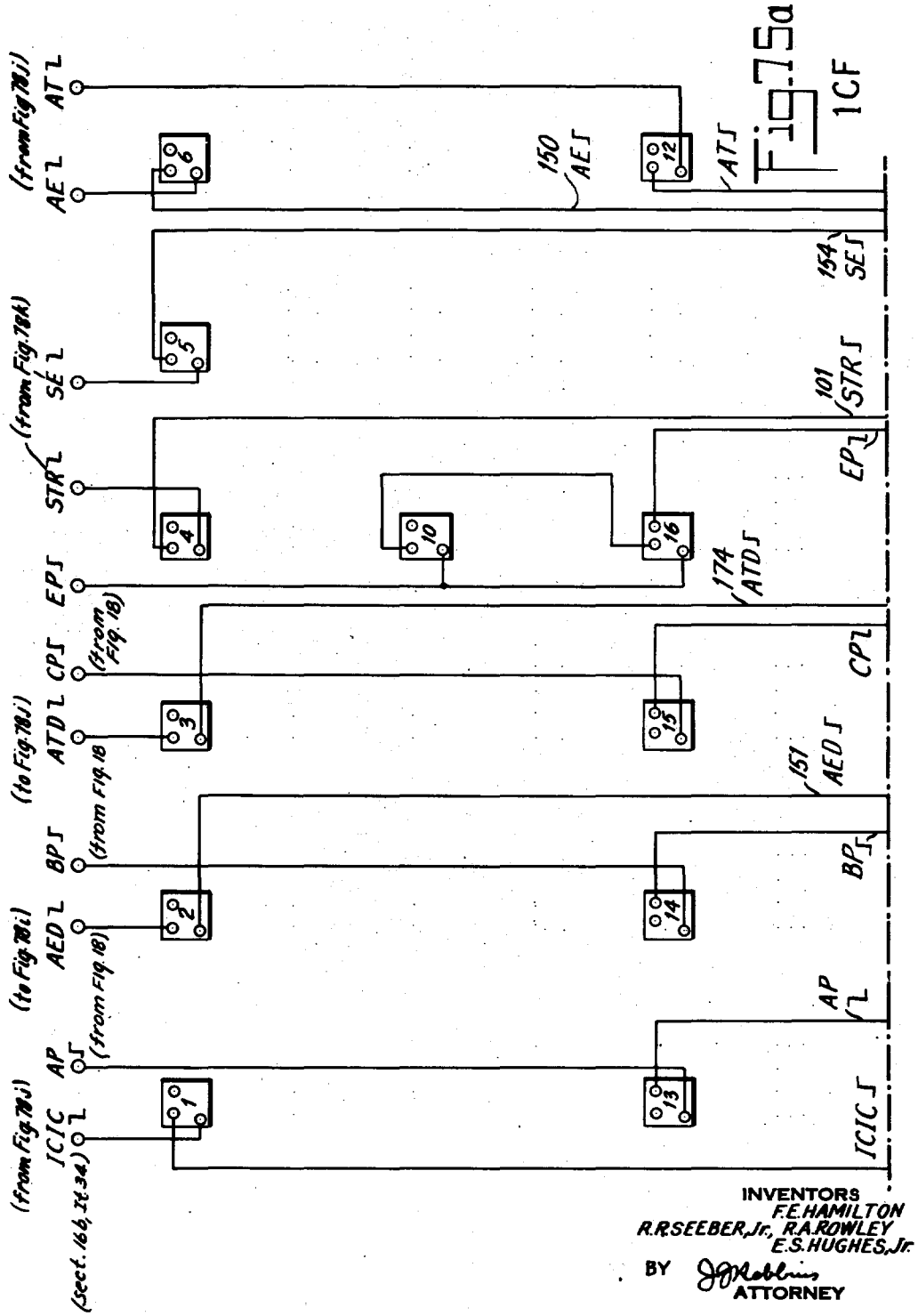

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E.S.HUGHES,Jr.

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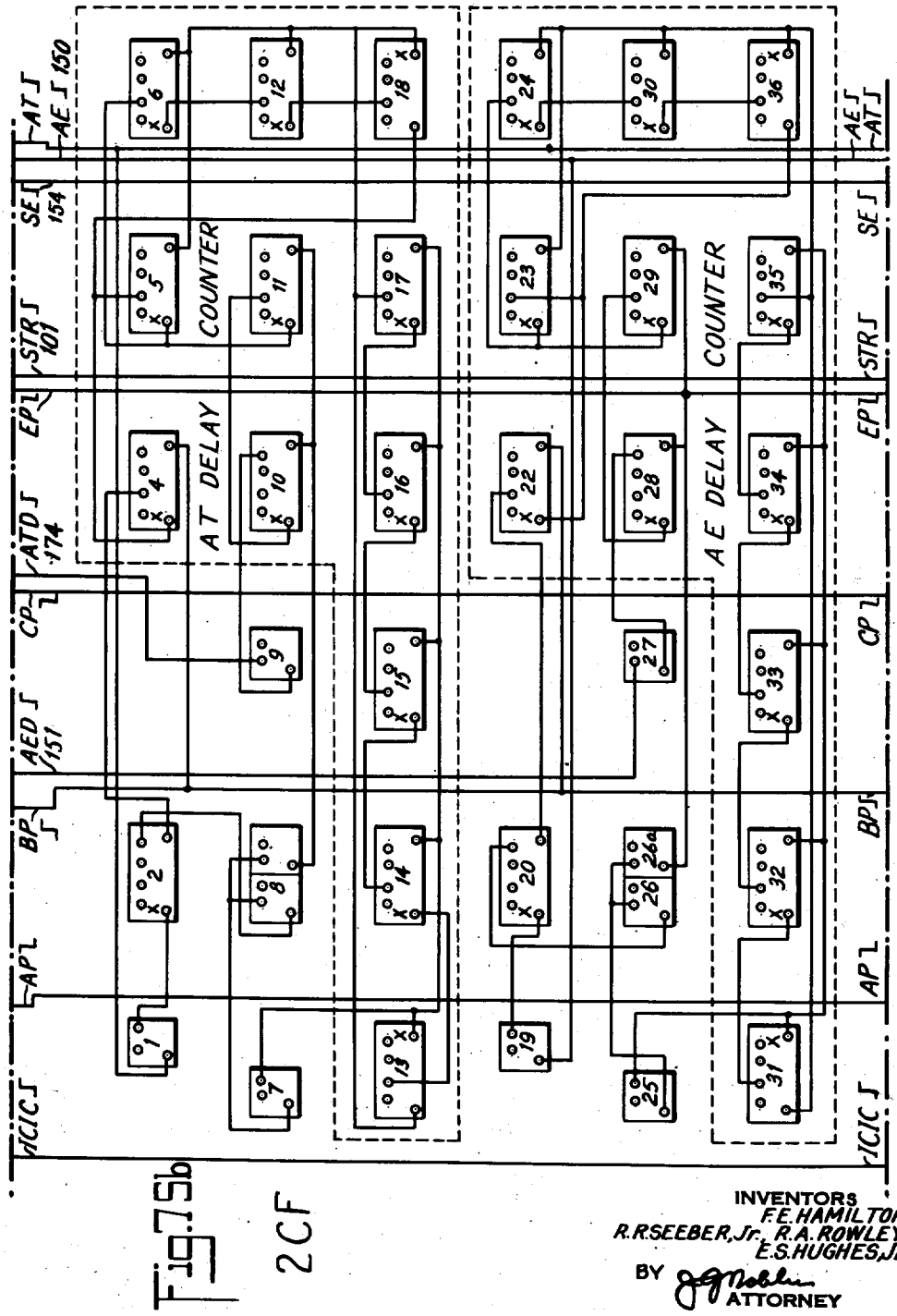

Fig. 75b

2CF

INVENTORS
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R.R. SEEBER, Jr., R.A. ROWLEY
E.S. HUGHES, Jr.

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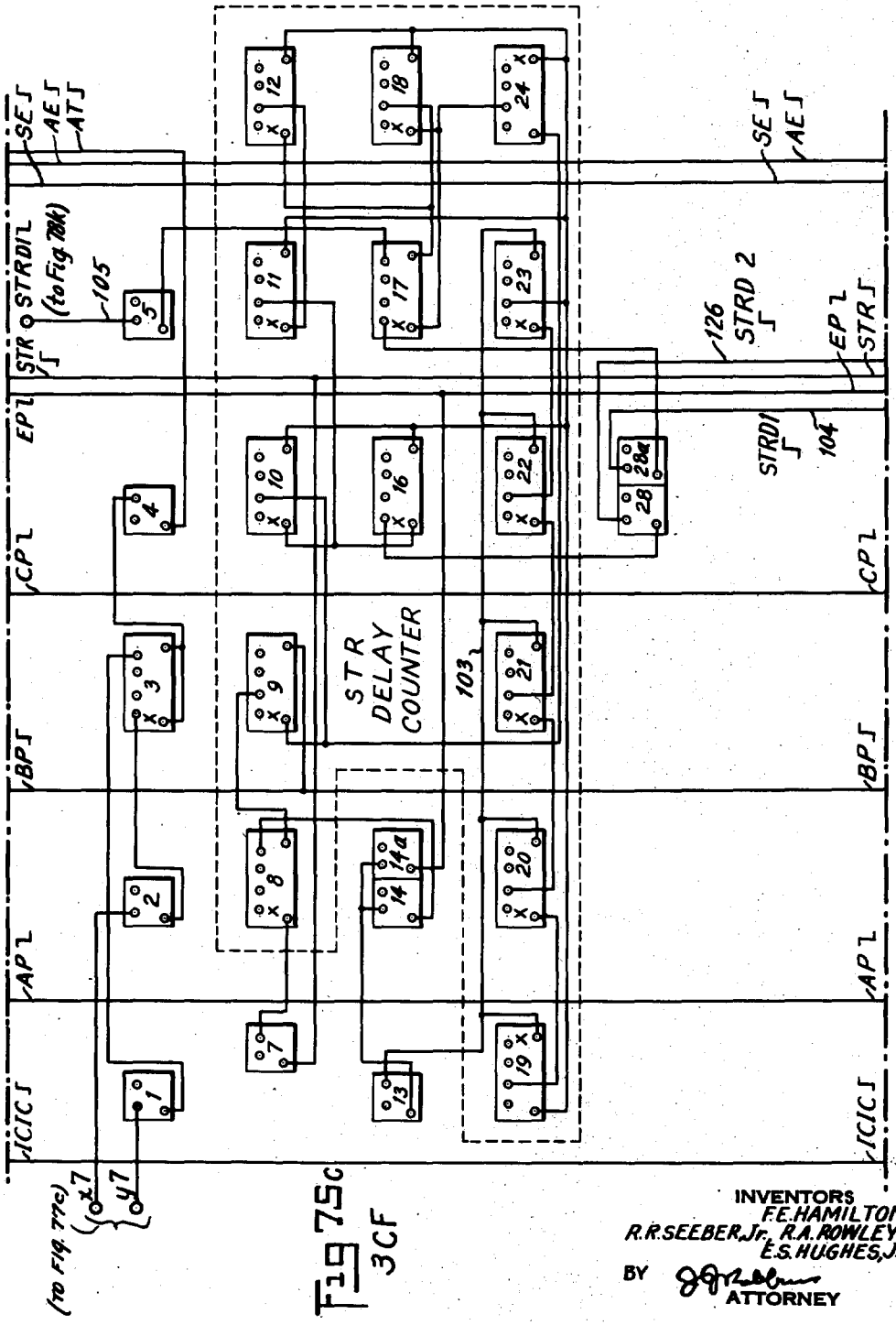

Fig 75c

3CF

INVENTORS
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R.R.SEEBER,Jr. R.A.ROWLEY
E.S.HUGHES,Jr.

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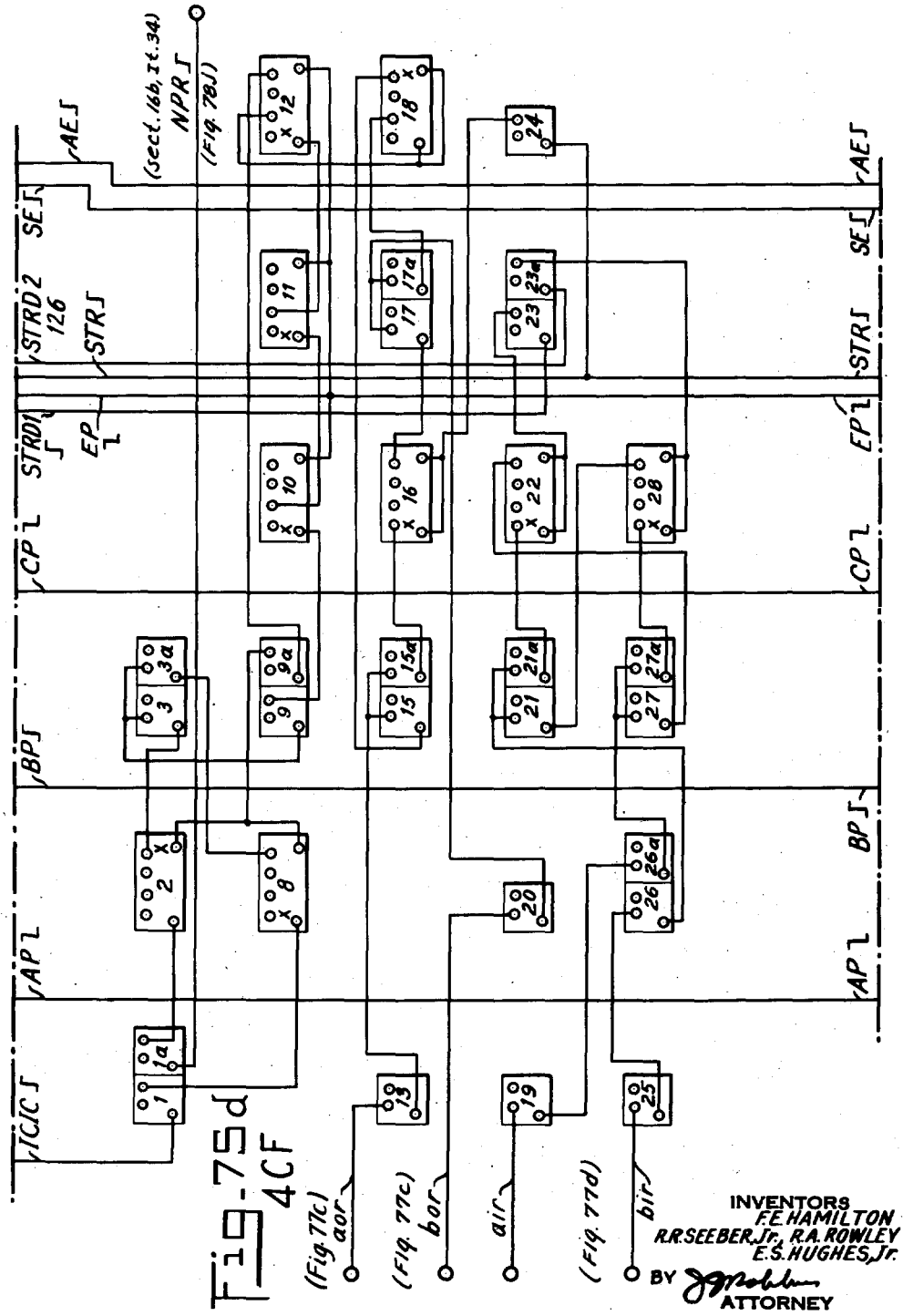

Fig. 75d
4CF

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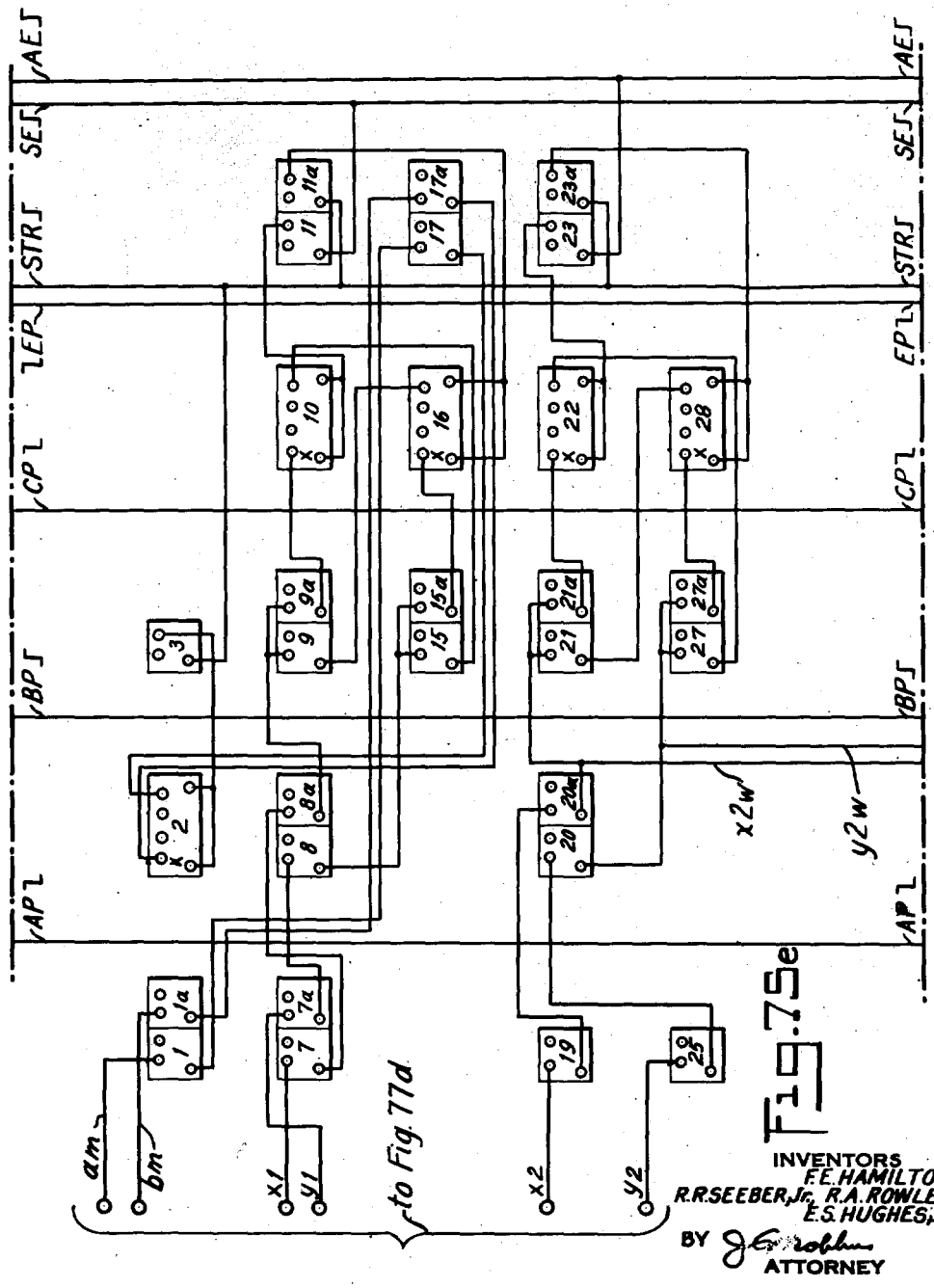

Fig. 75e

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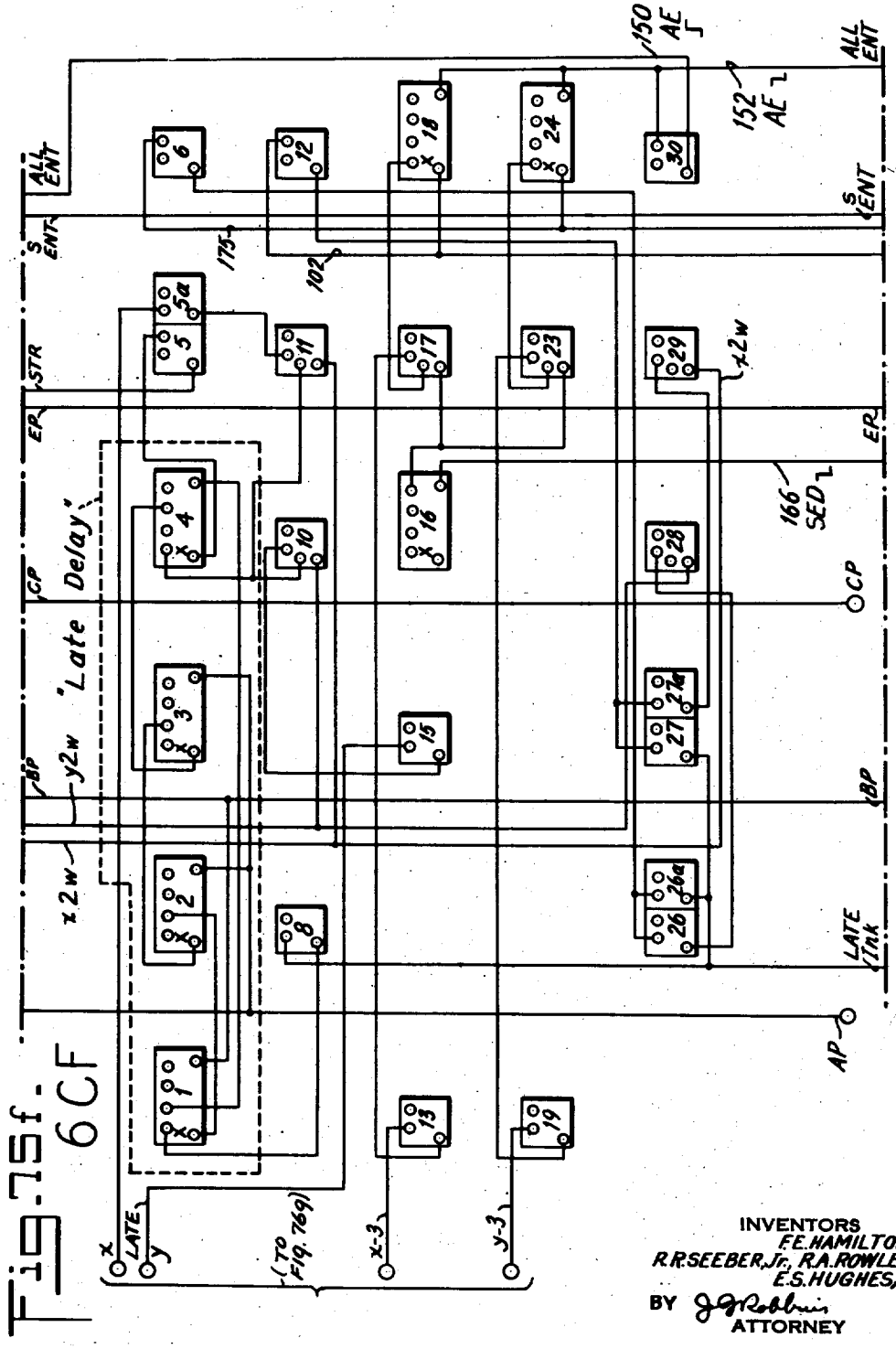

Fig. 75f. 6CF

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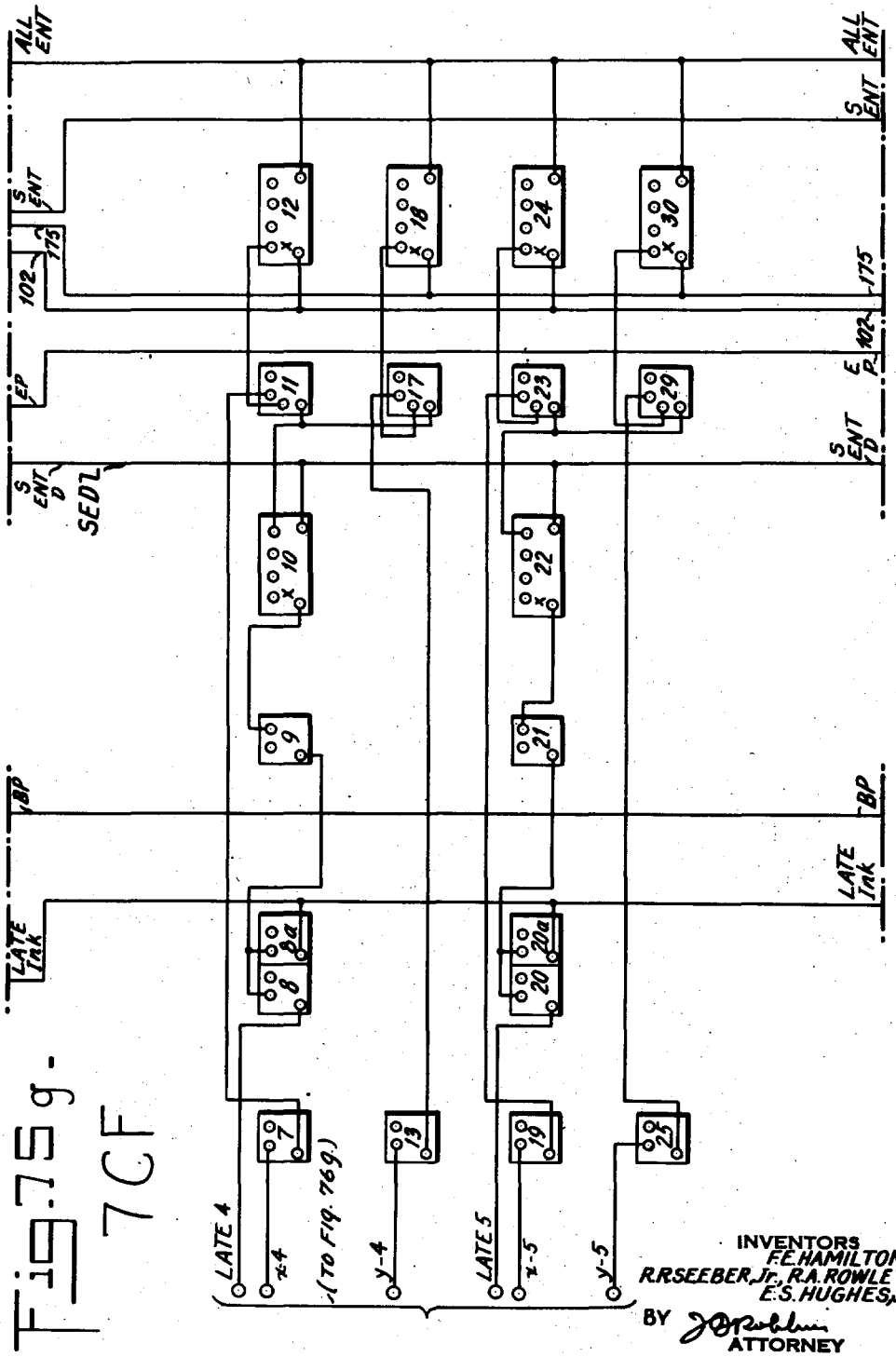

Fig. 75g-7CF

INVENTORS
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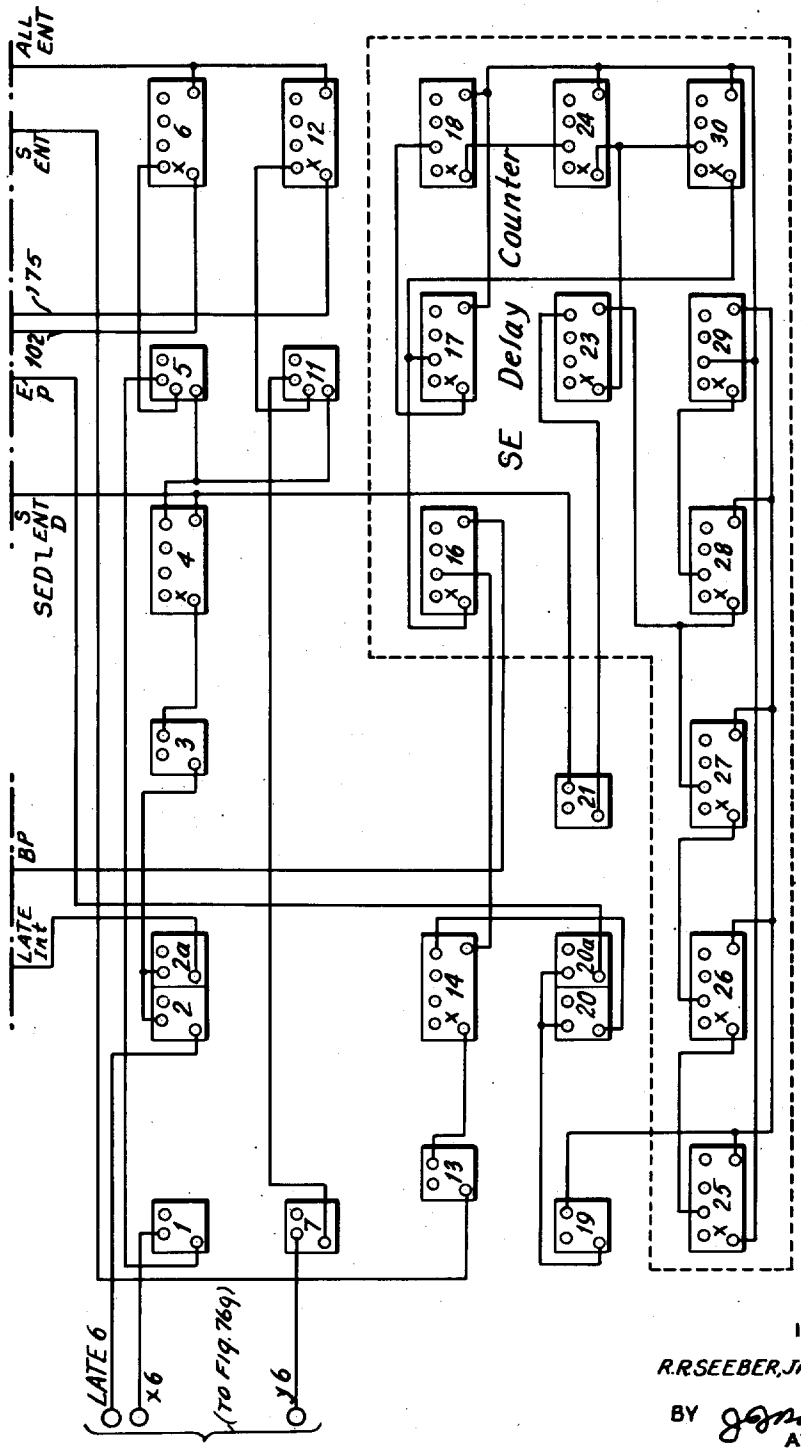

Fig. 75h. 8CF

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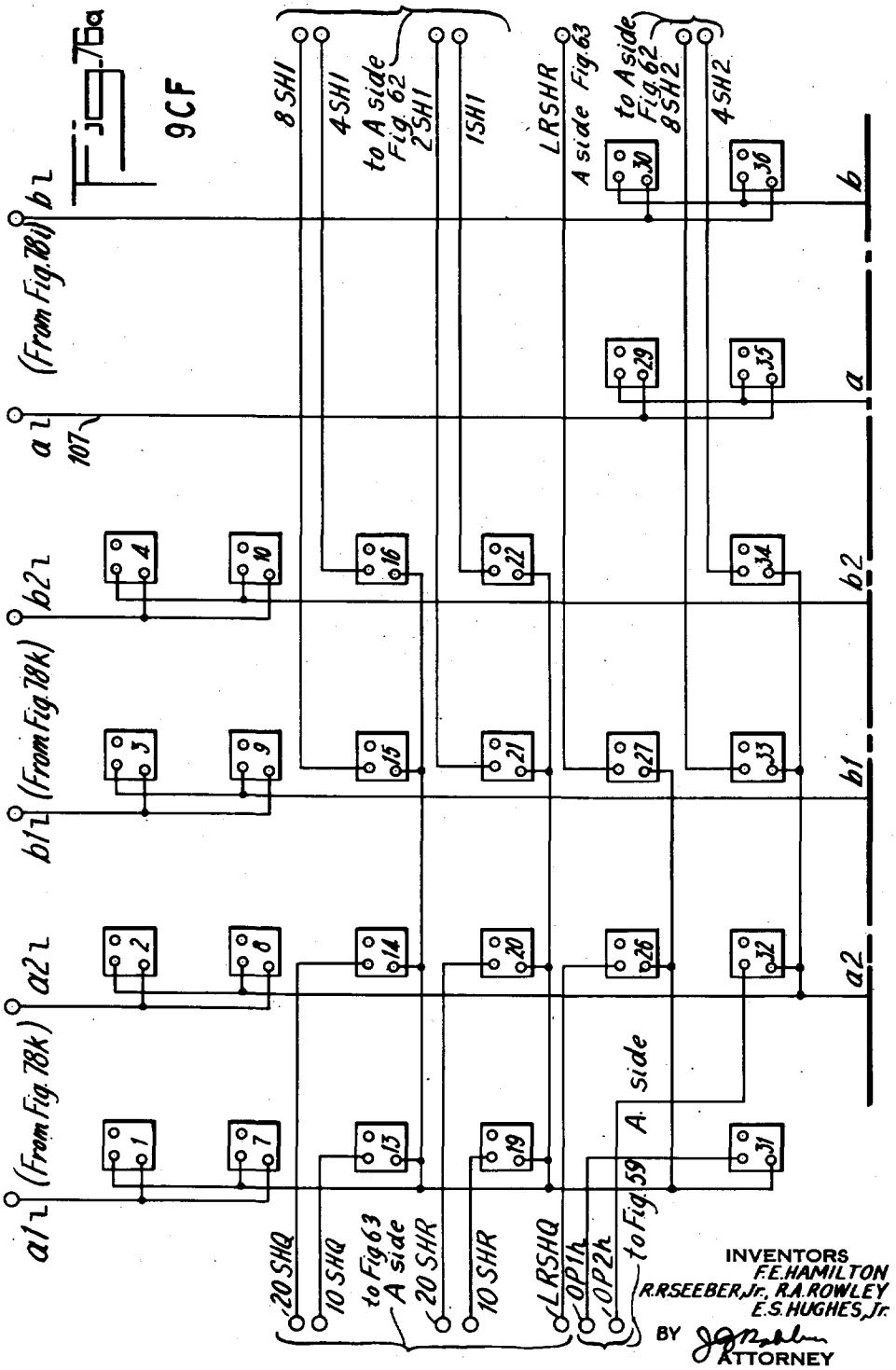

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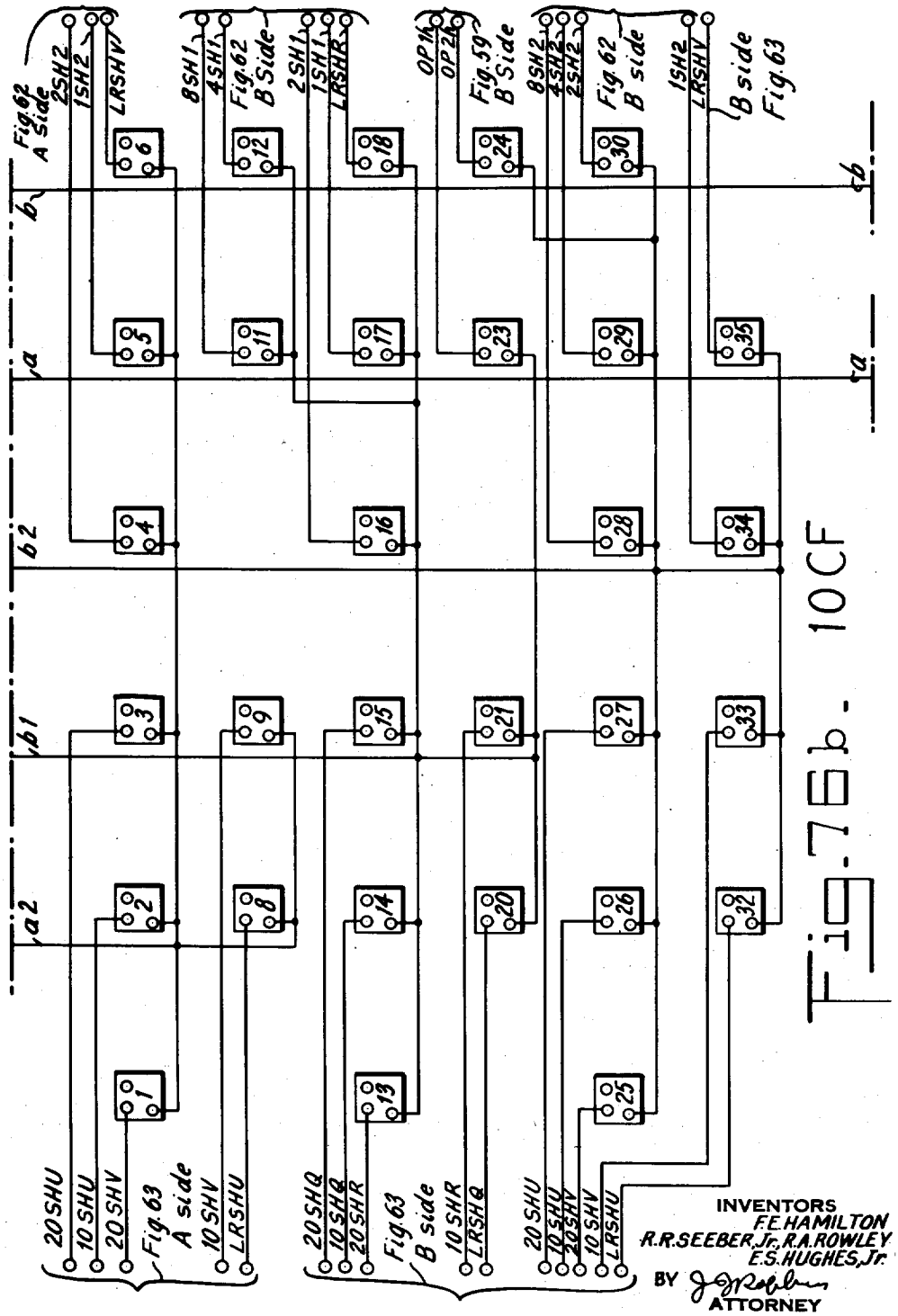

Fig. 76b. 10 CF

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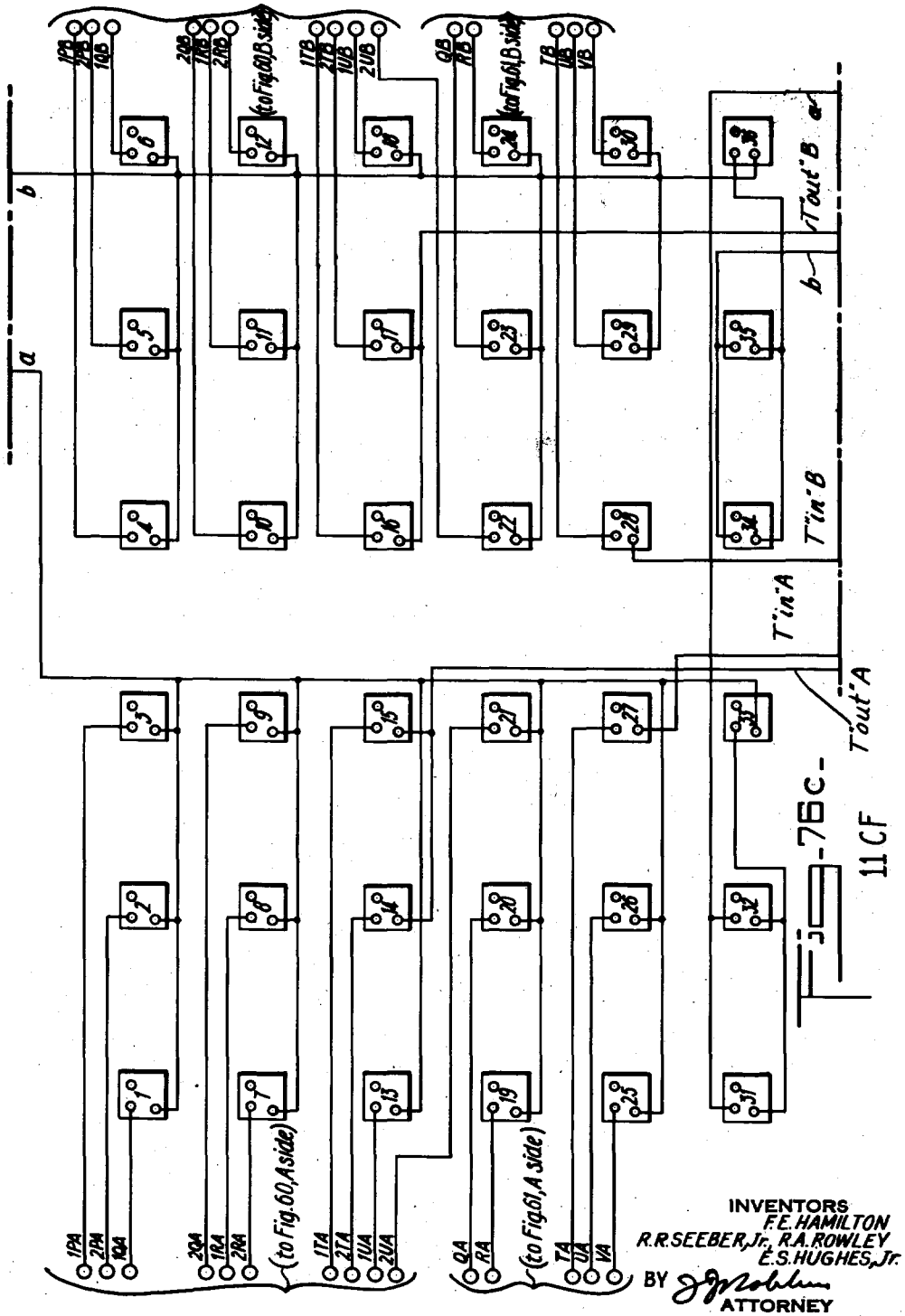

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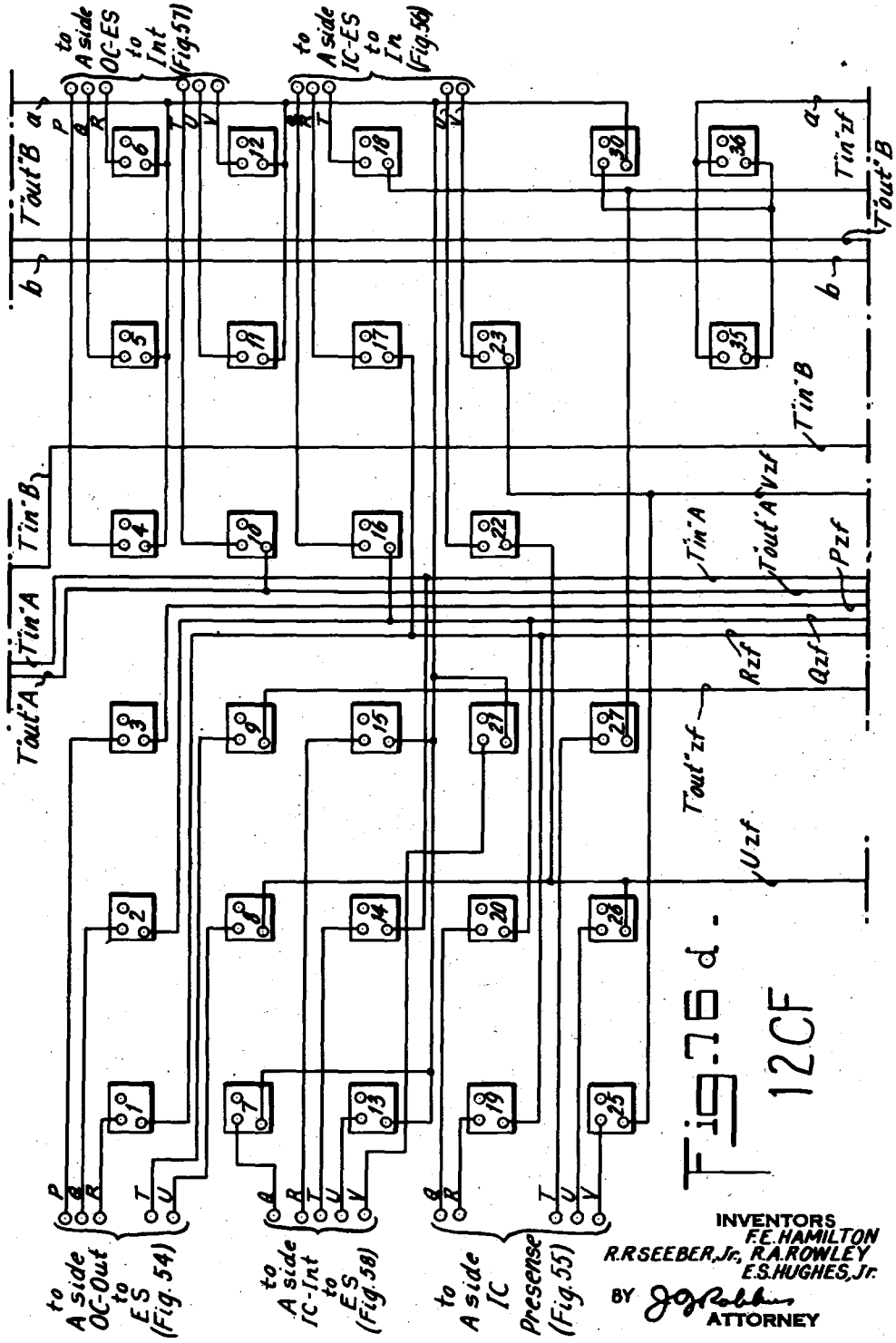

Fig. 76 d.

12CF

INVENTORS
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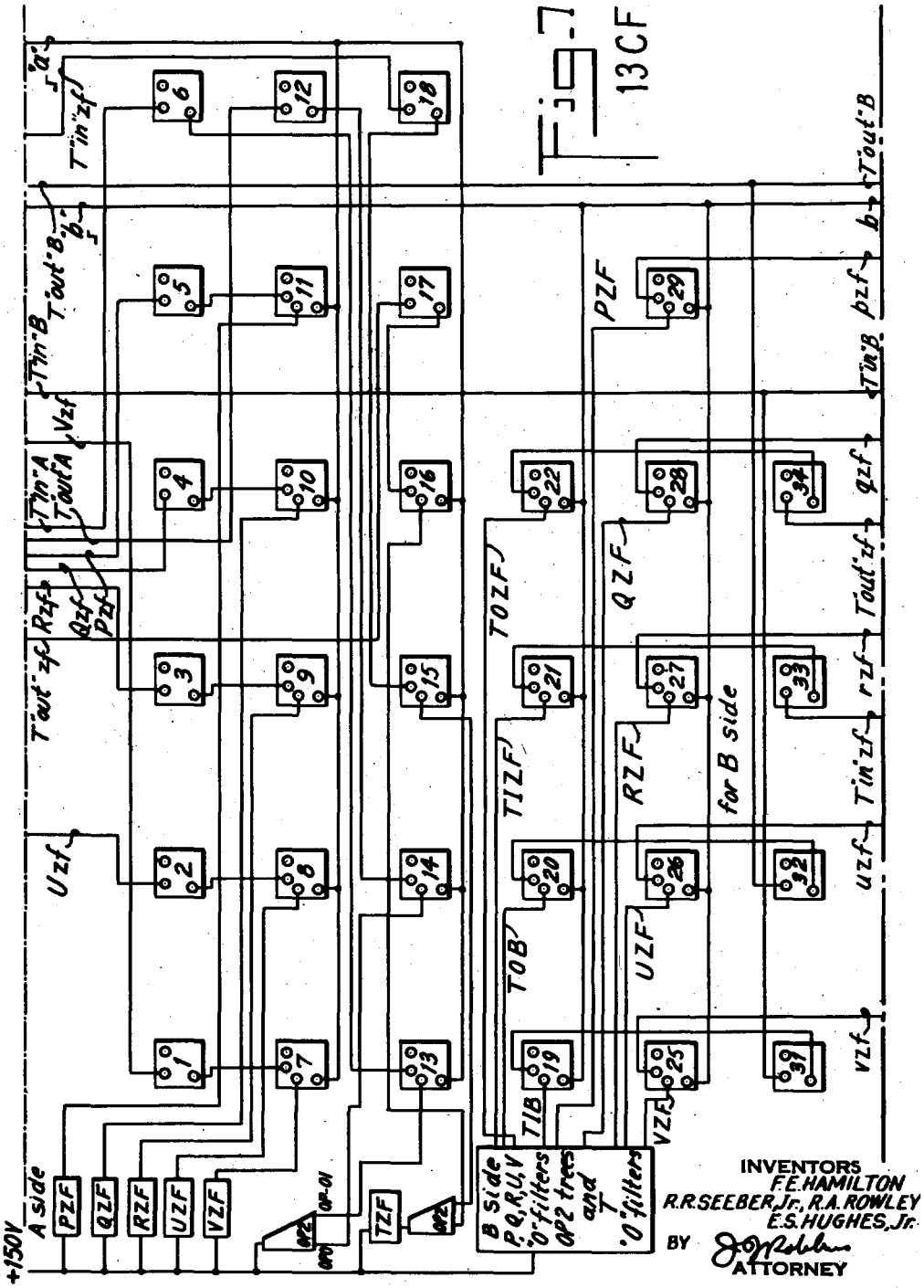
Fig. 76e
13CF



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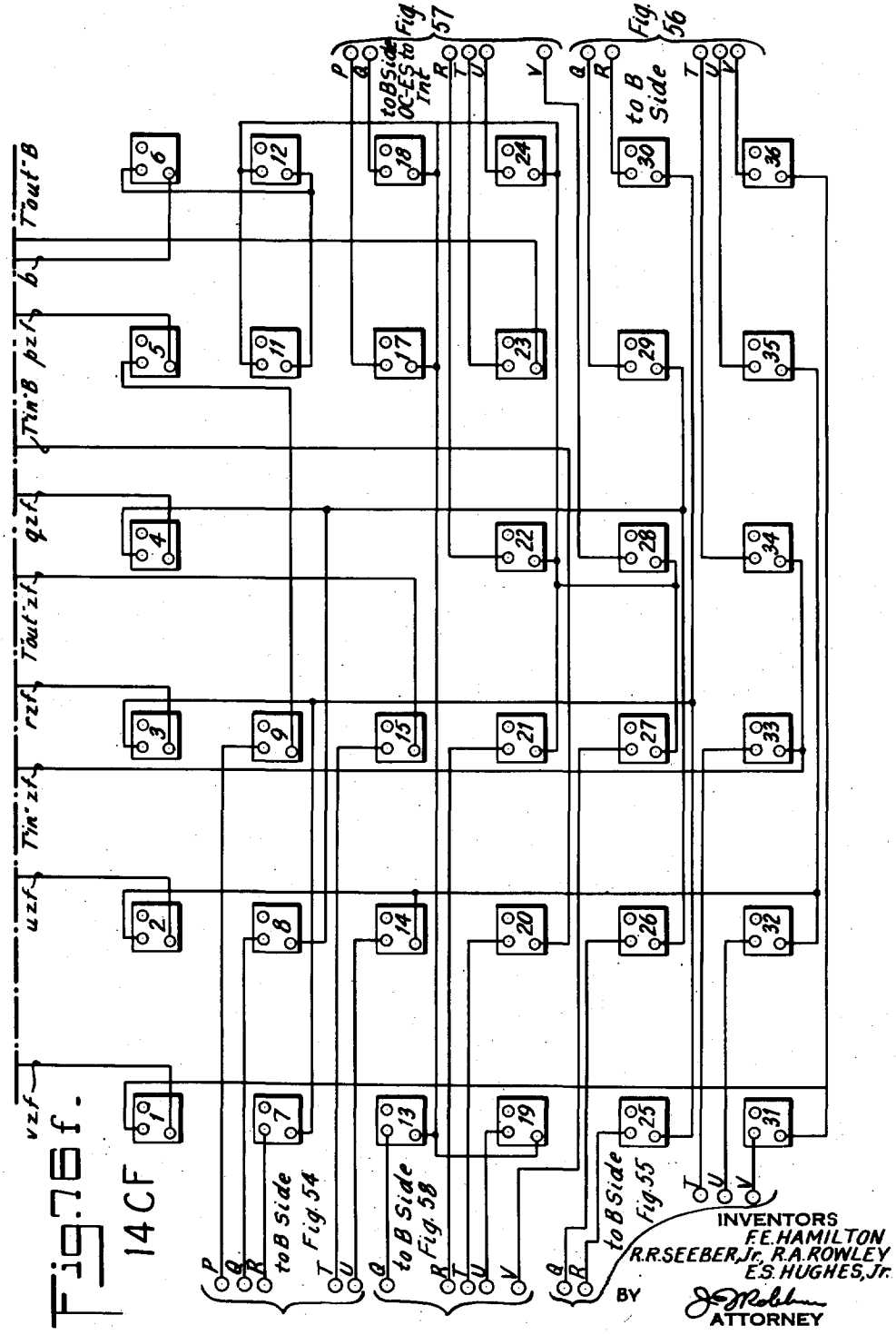

Fig. 86 f.

14 CF

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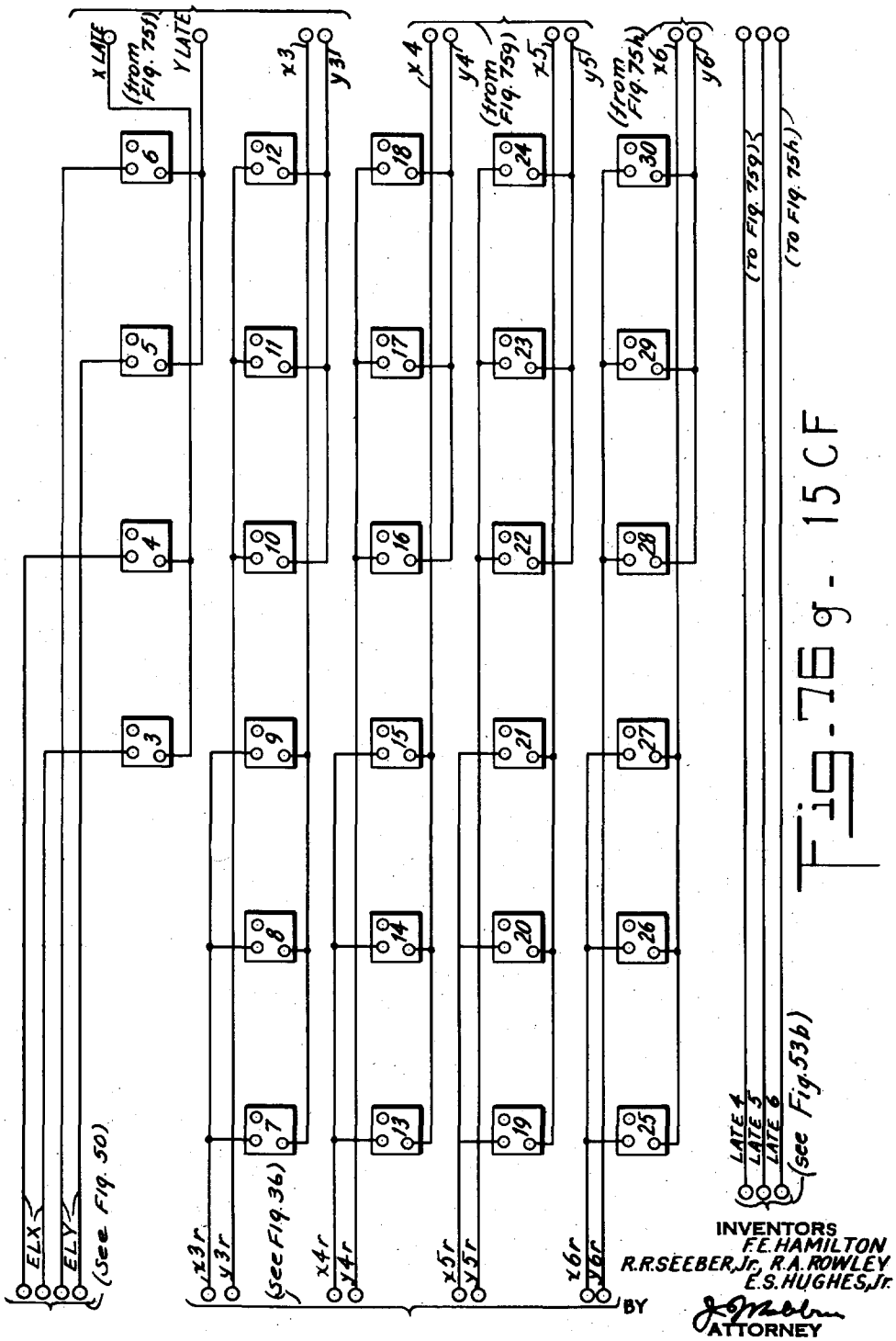

Fig. 76 g - 15 CF

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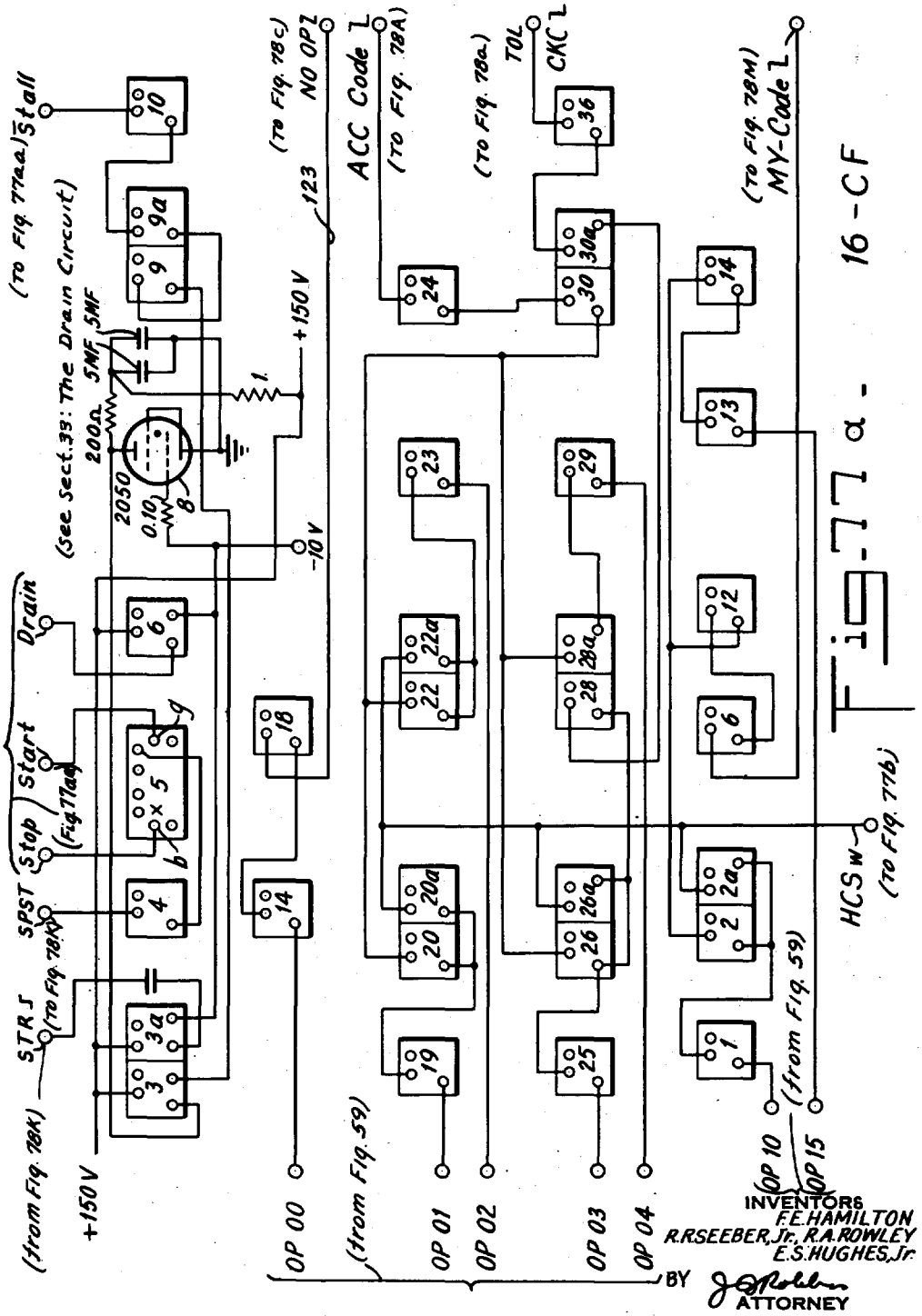

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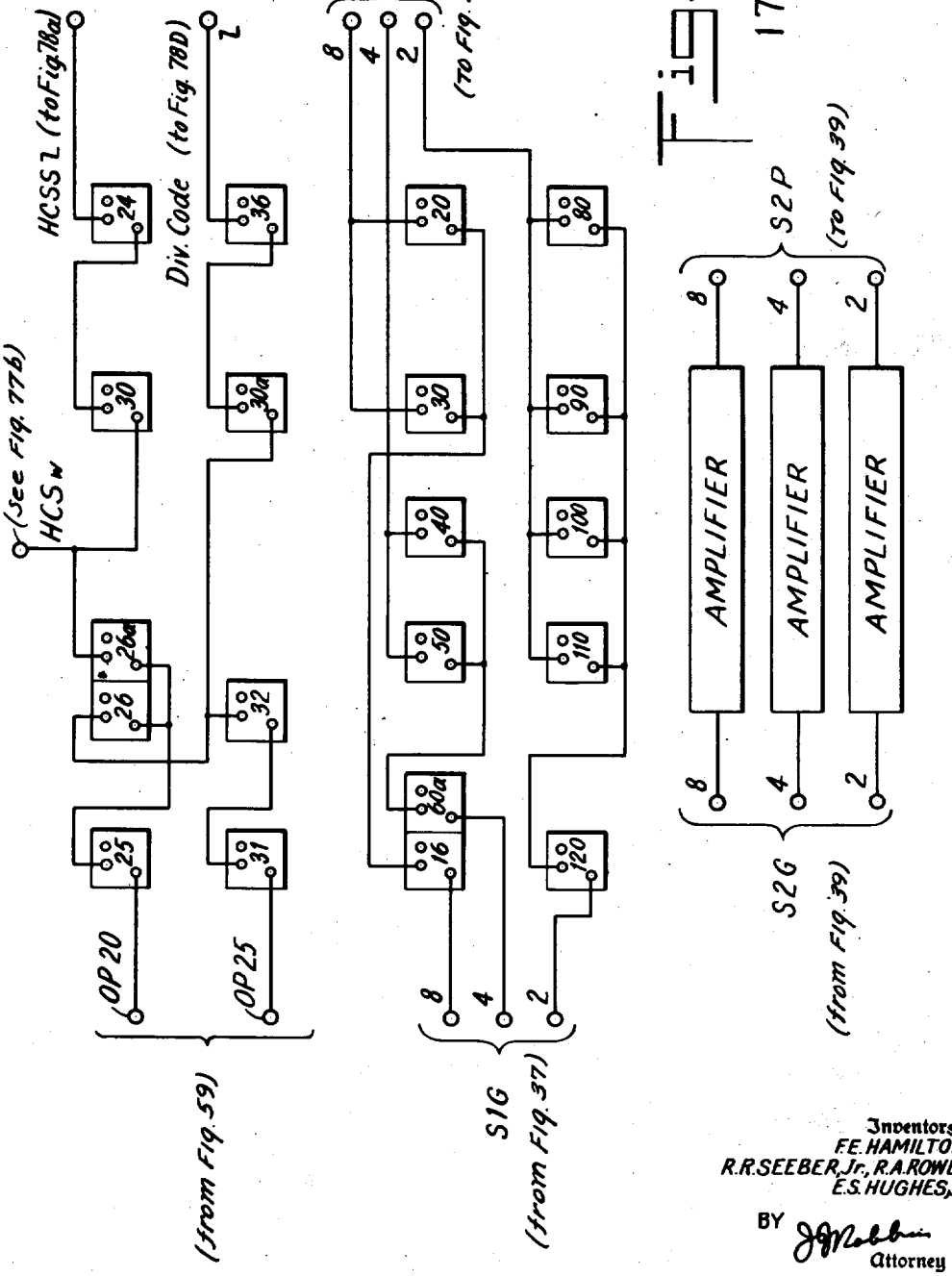

Fig. 77b.

17CF

Inventors
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BY J. J. Mabbin
Attorney

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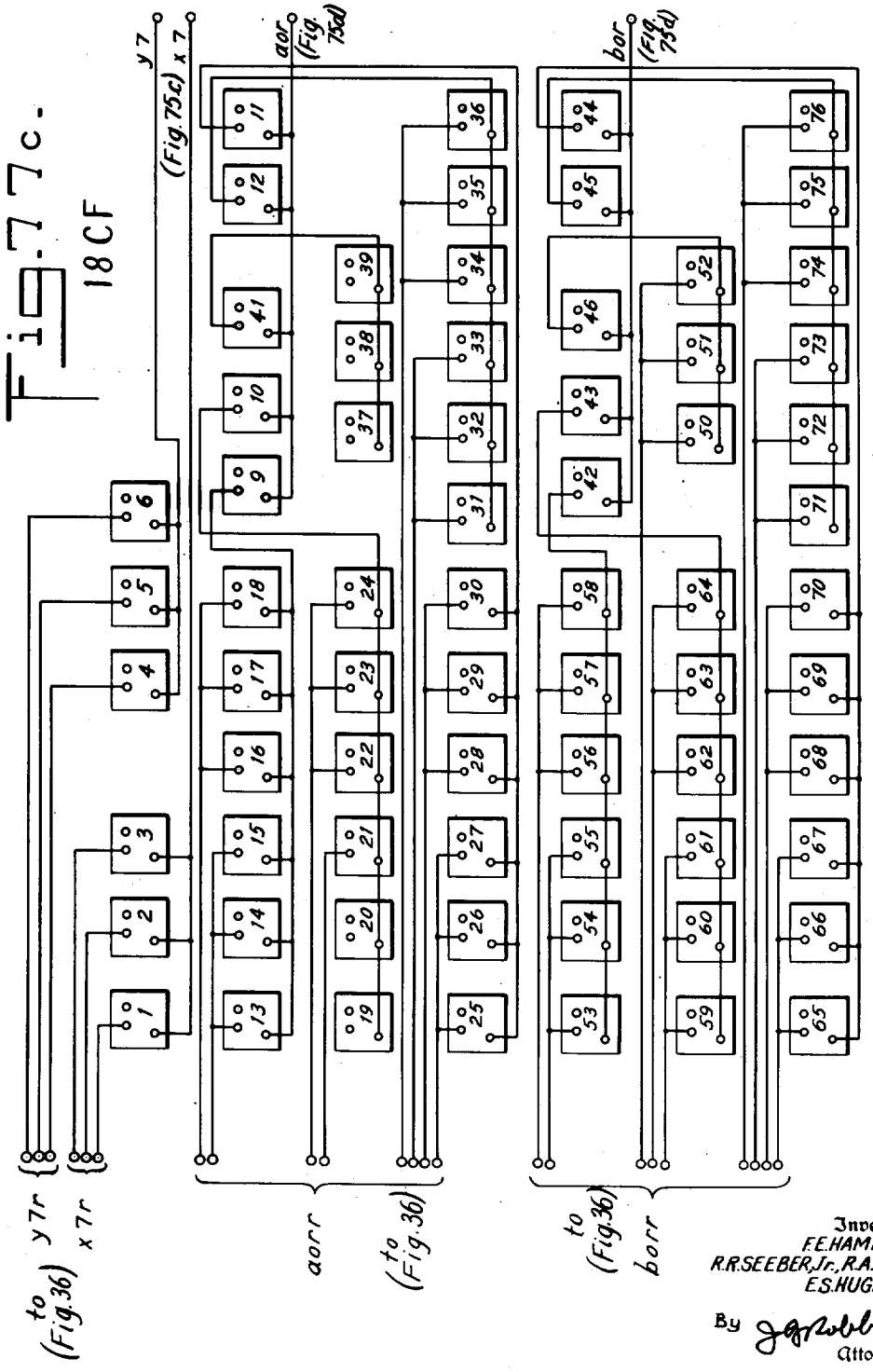
Fig. 77c.



Inventors
F.E. HAMILTON
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By J. J. Robbins
Attorney

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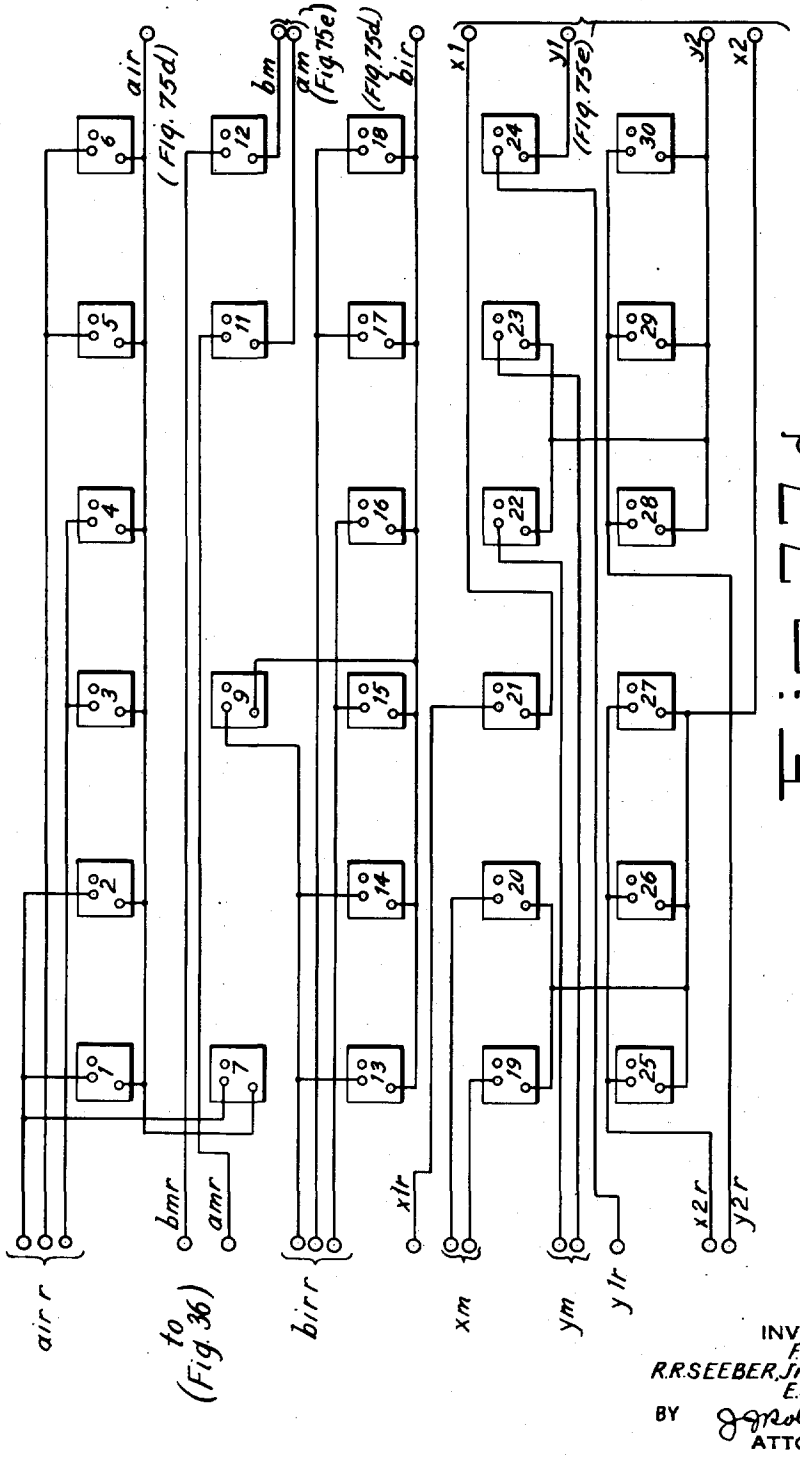

Fig. 77 d.

19 CF

INVENTORS
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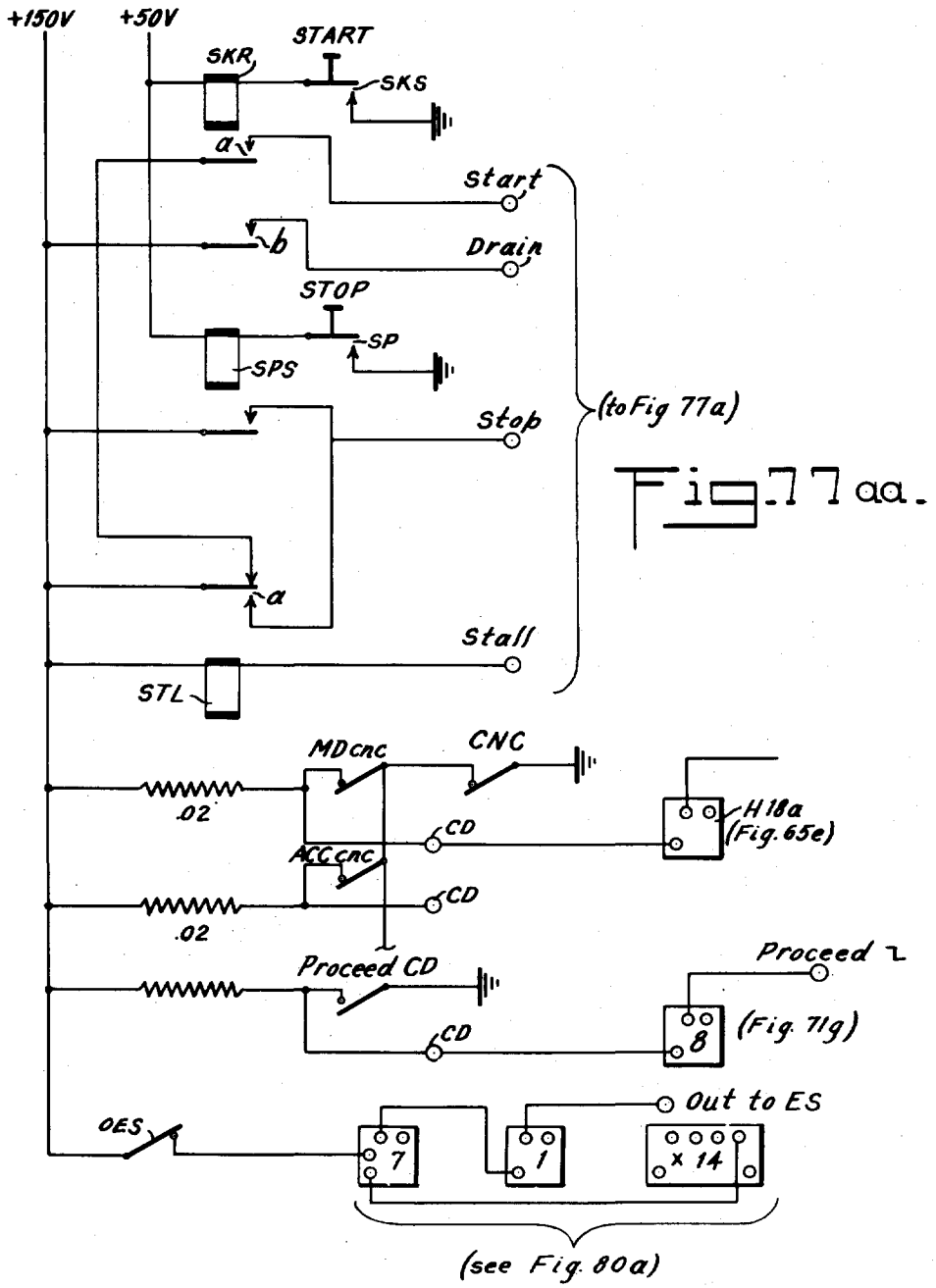

Fig. 77aa.

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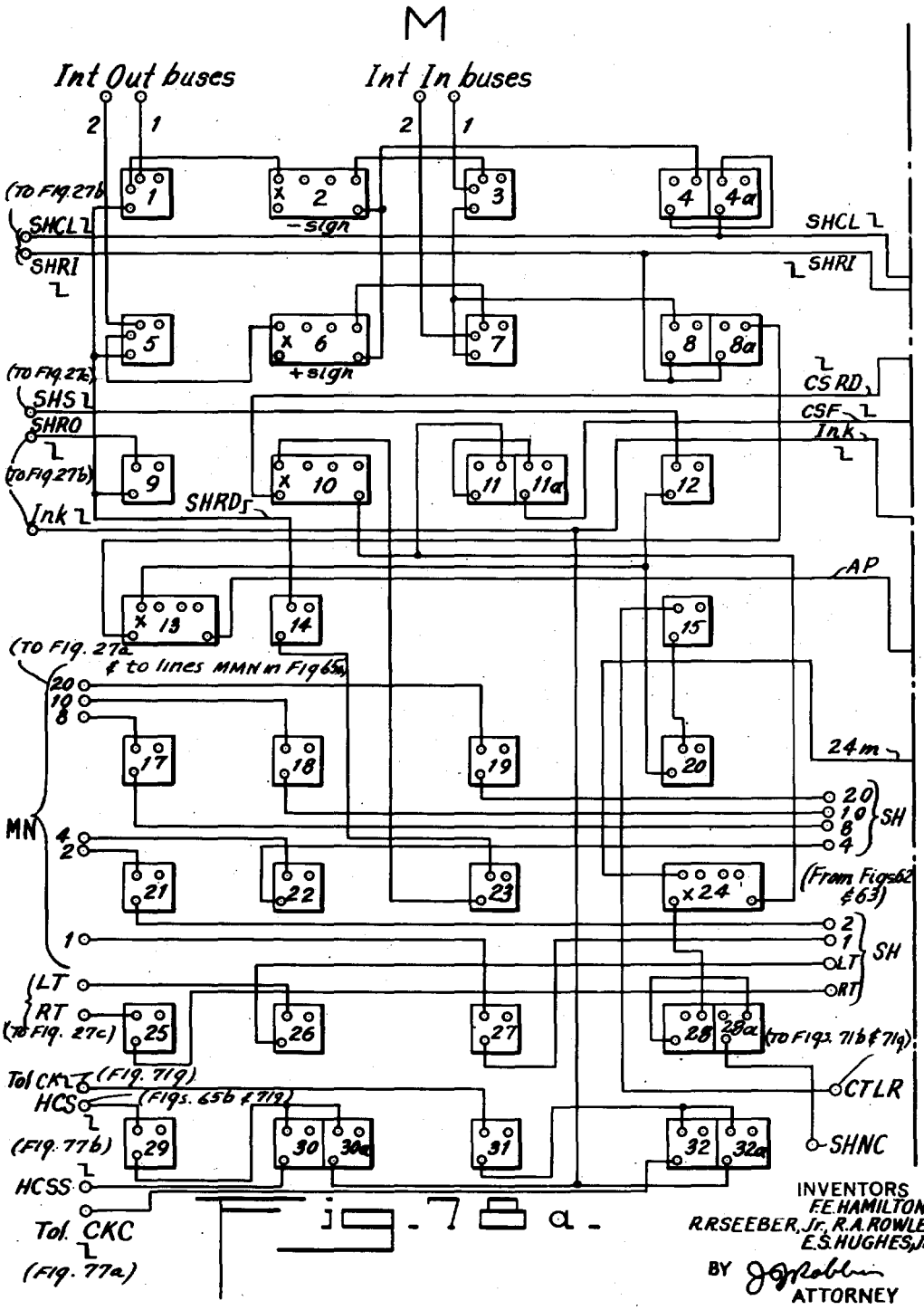

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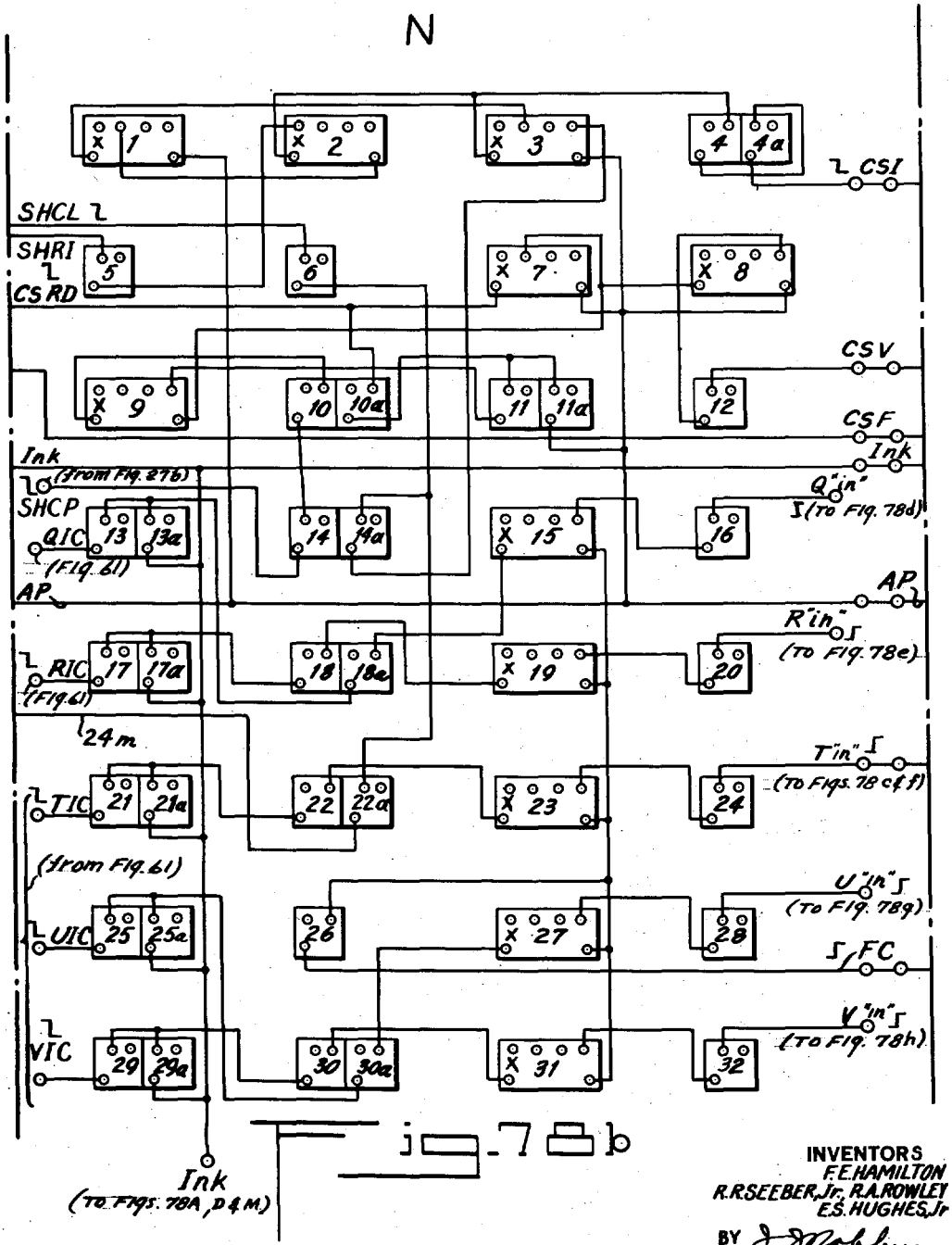

Fig. 78b

INVENTORS
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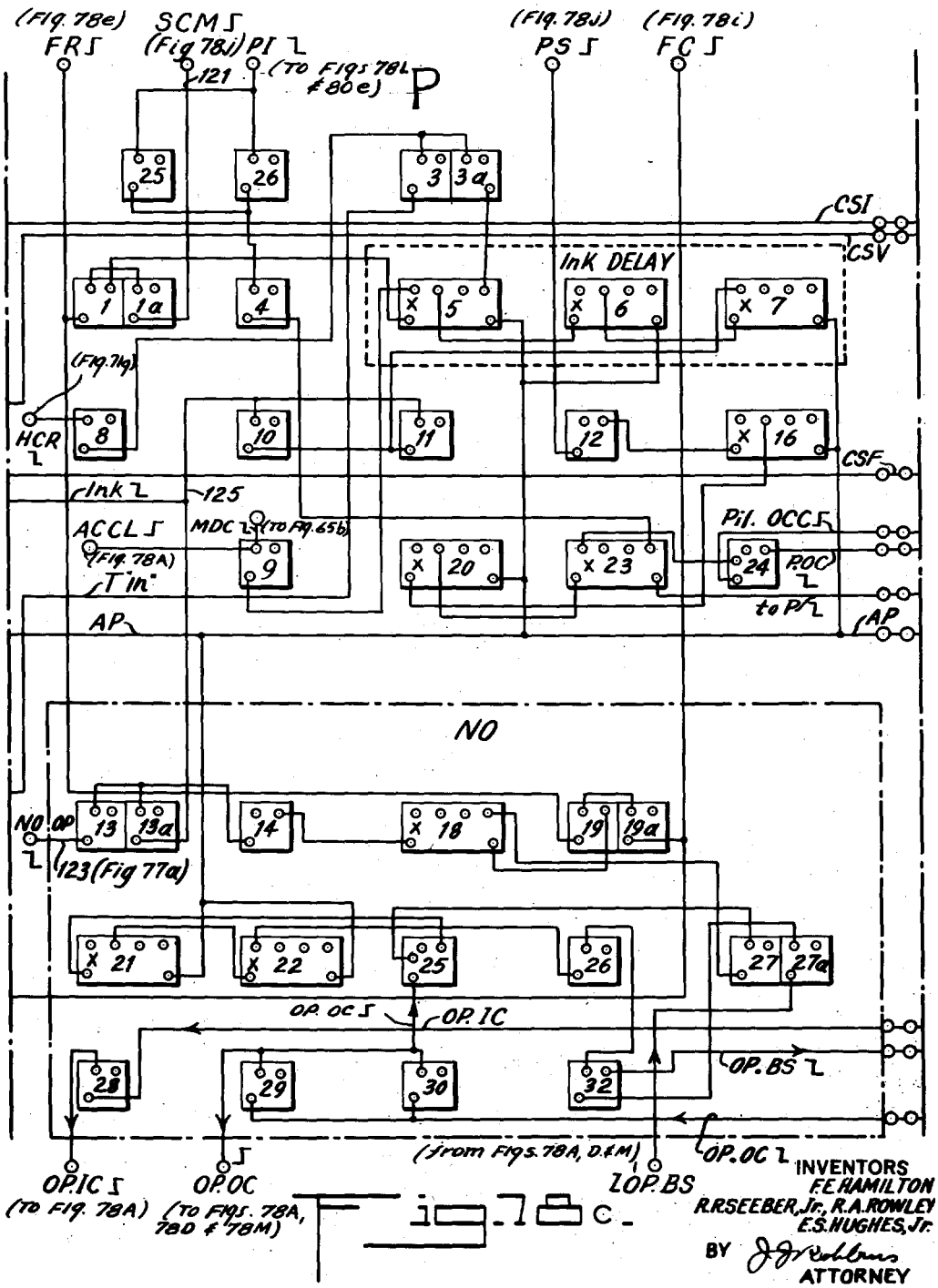

Fig. 78c

INVENTORS
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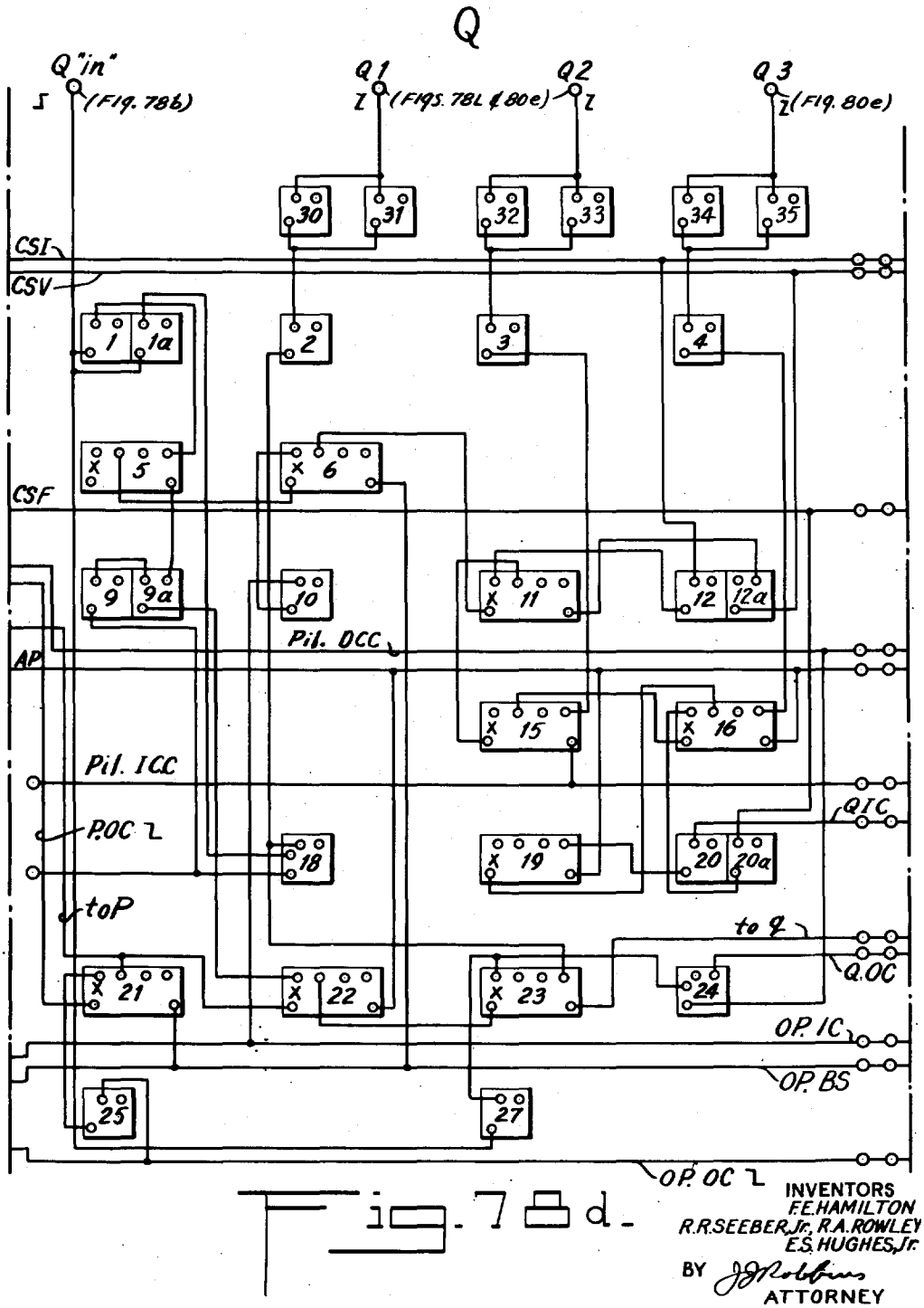

Fig. 78d.

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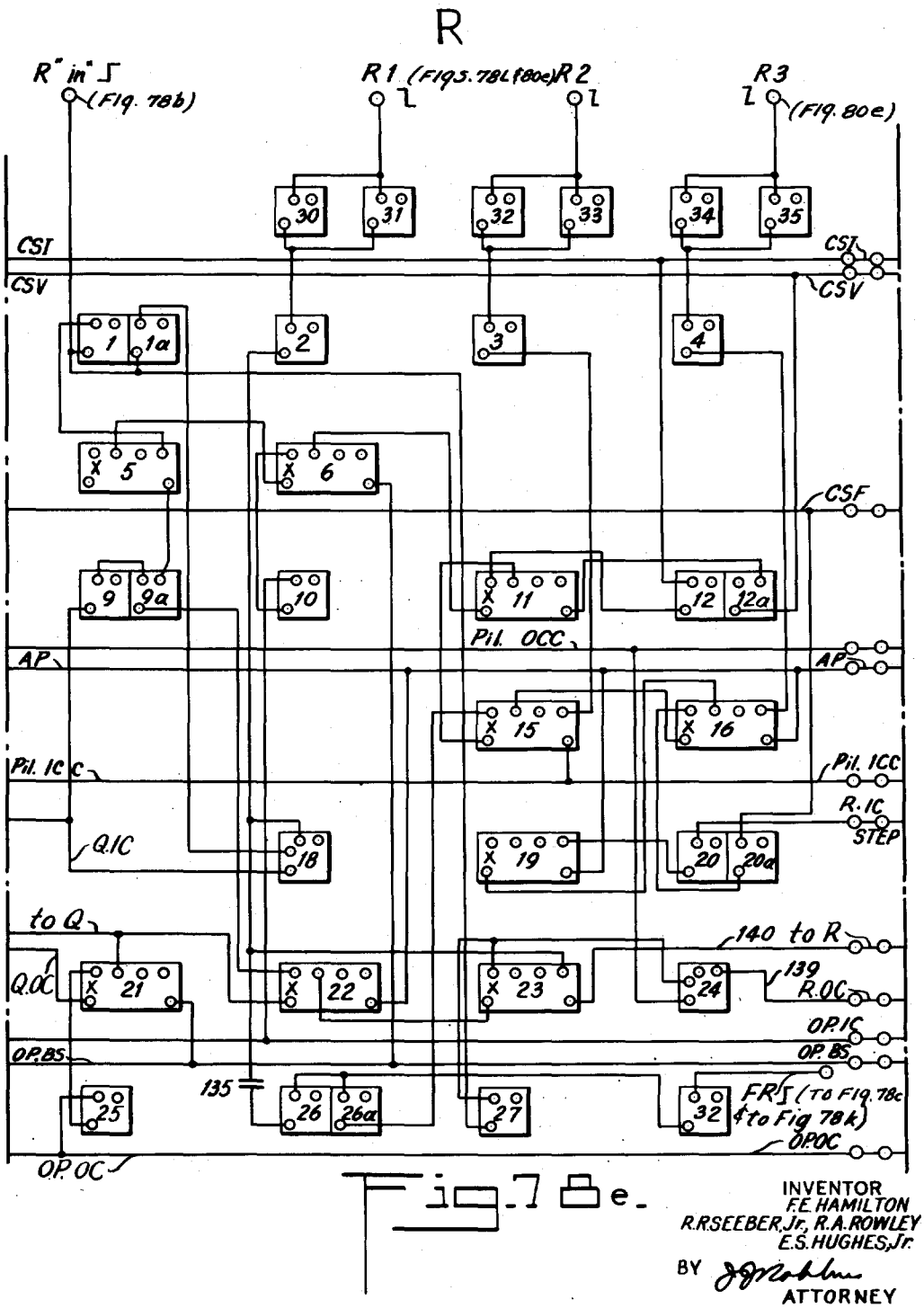

Fig. 7 8e.

INVENTOR
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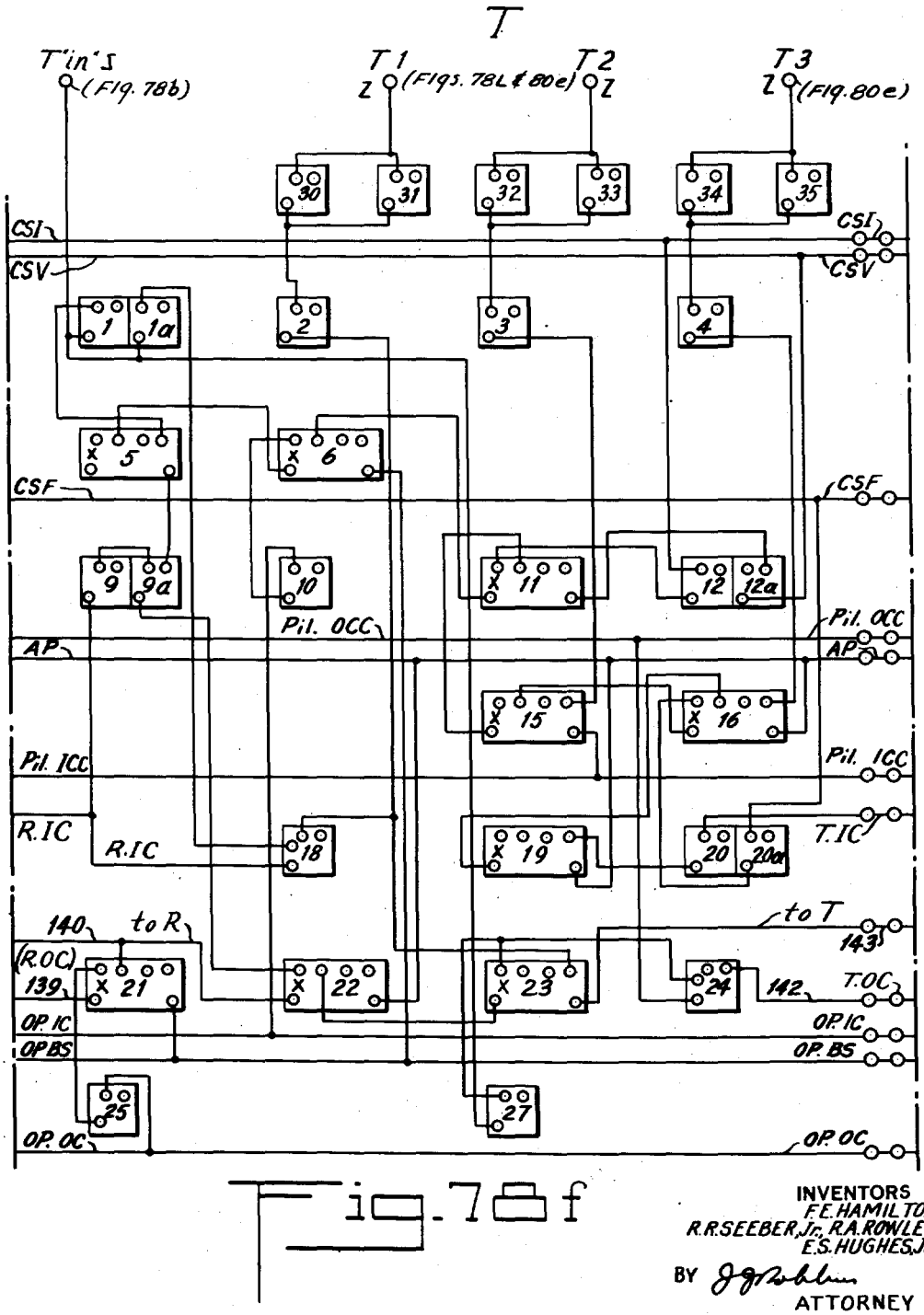

Fig. 78f

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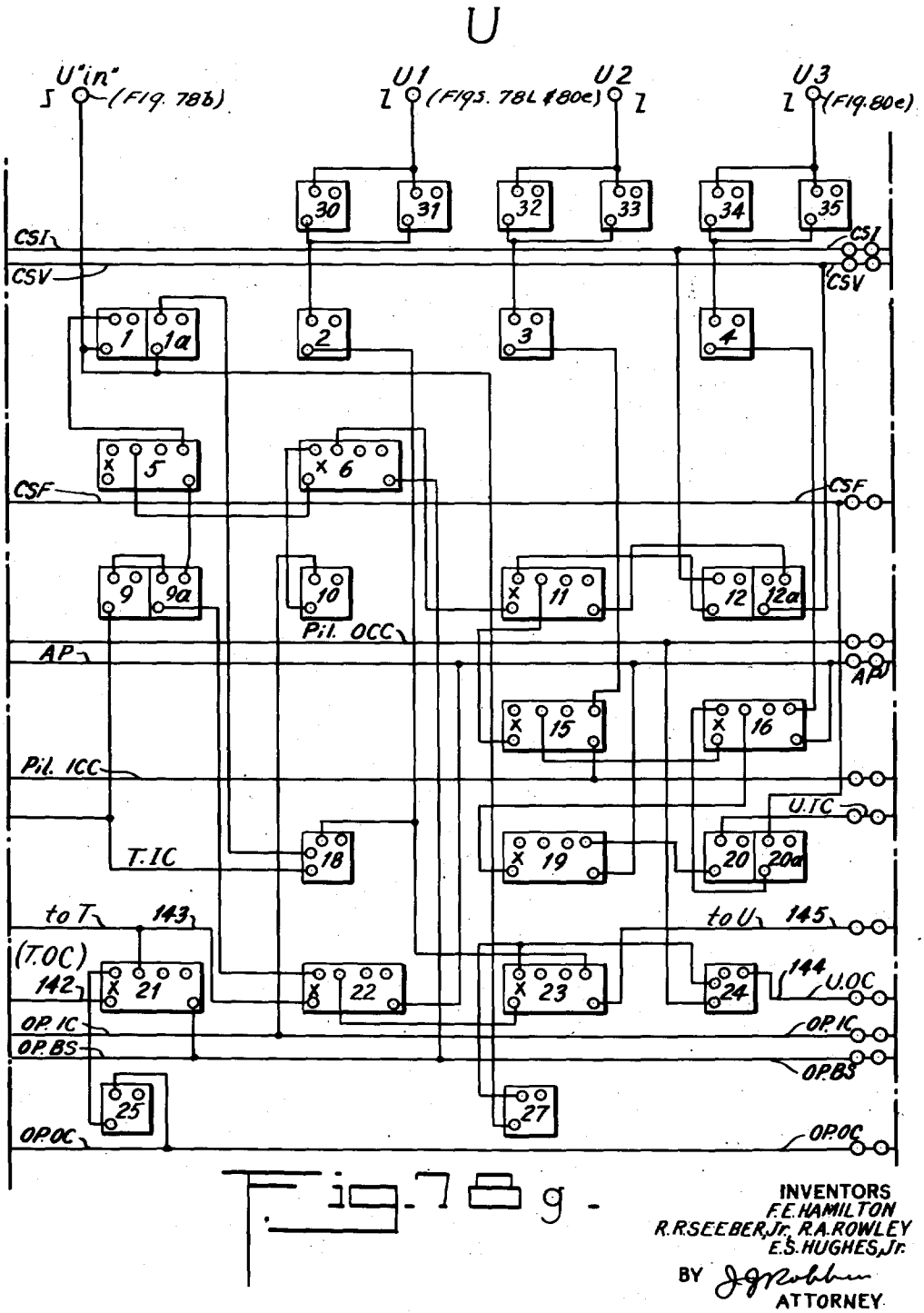

Fig. 78g.

INVENTORS
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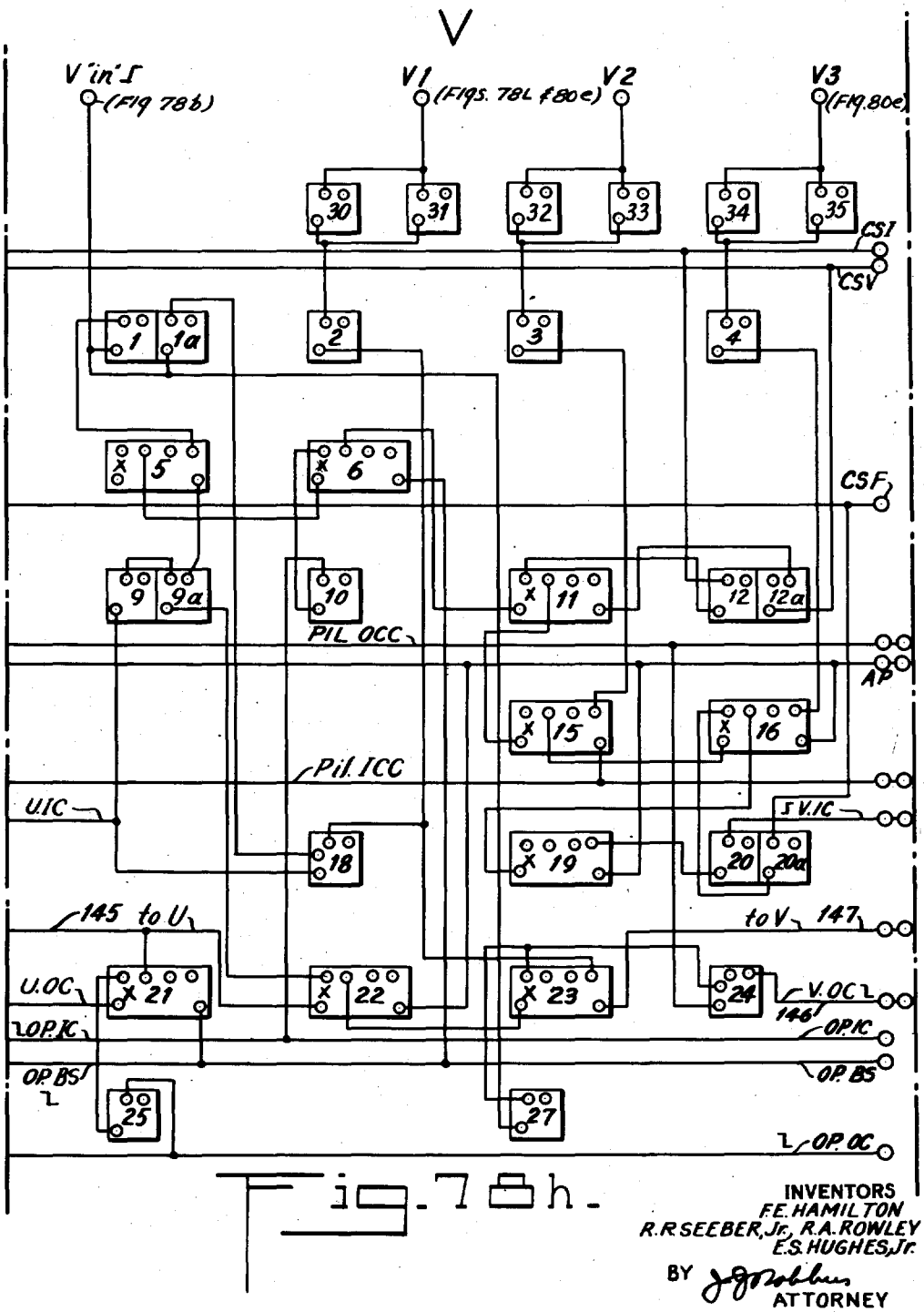

Fig. 78h.

INVENTORS
F.E. HAMILTON
R.R. SEEBER, Jr., R.A. ROWLEY
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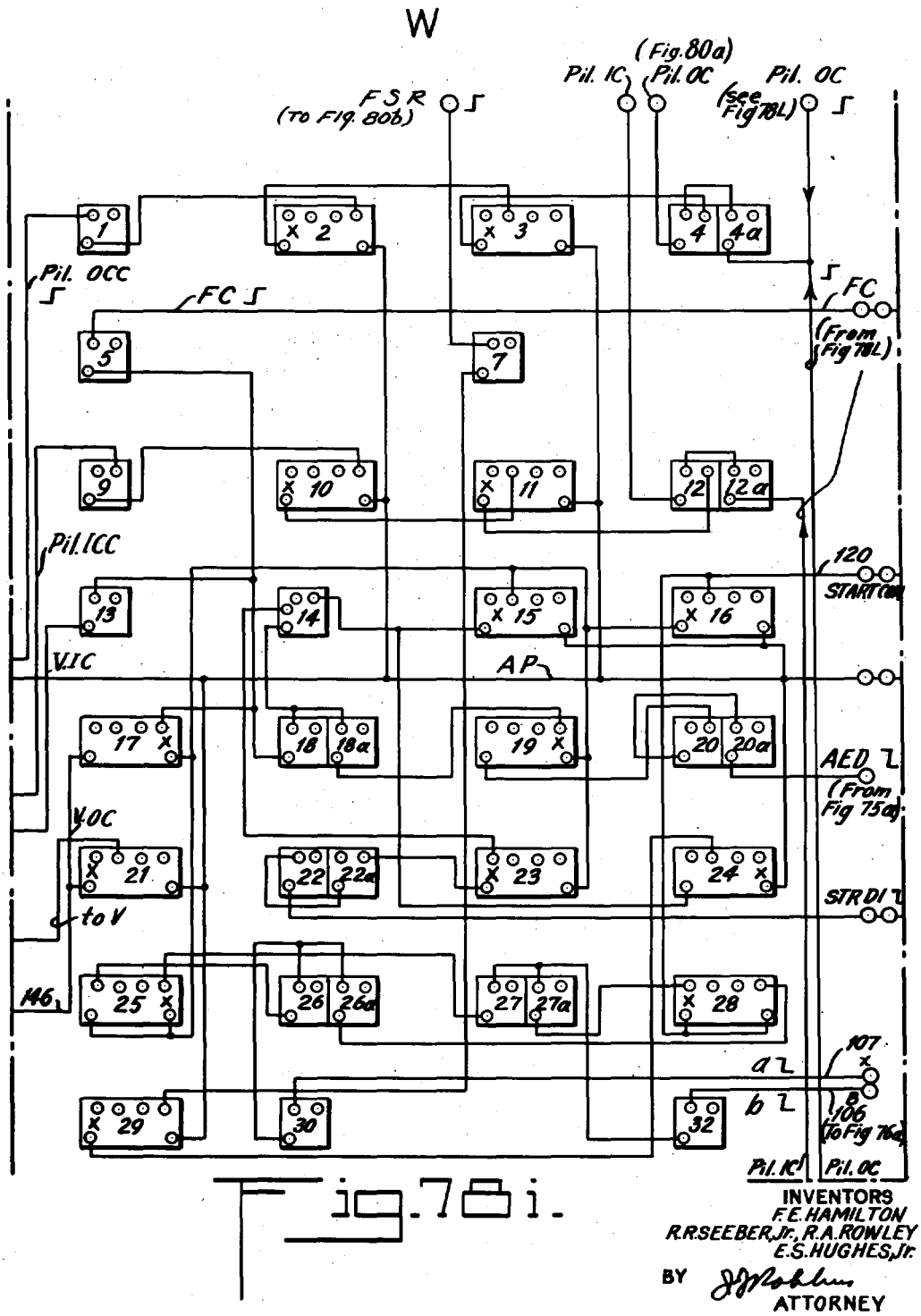

Fig. 78i.

INVENTORS
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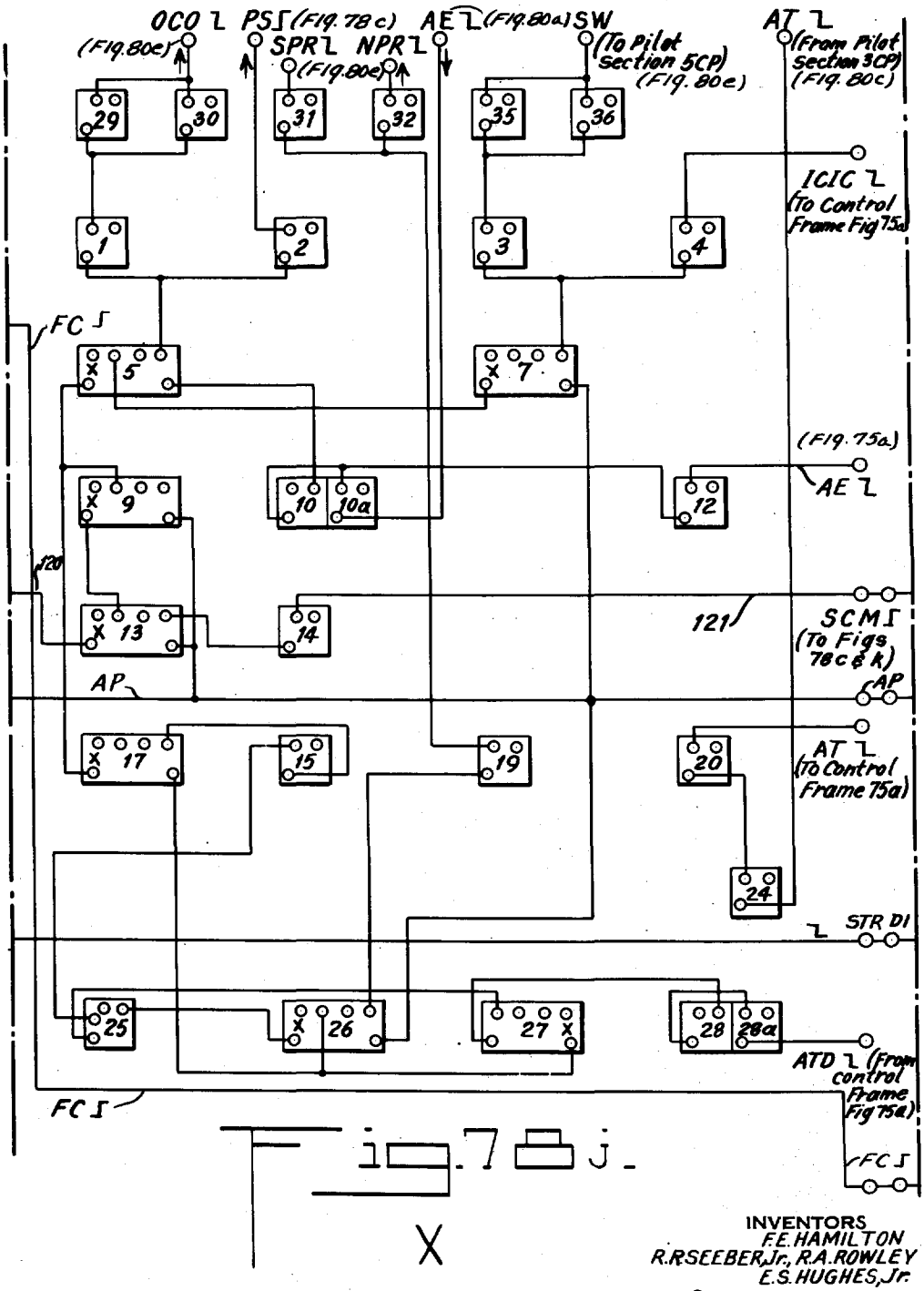

Fig. 7 B

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F.E. HAMILTON
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BY J. G. Robbins
ATTORNEY

April 28, 1953 F. E. HAMILTON ET AL 2,636,672

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 124

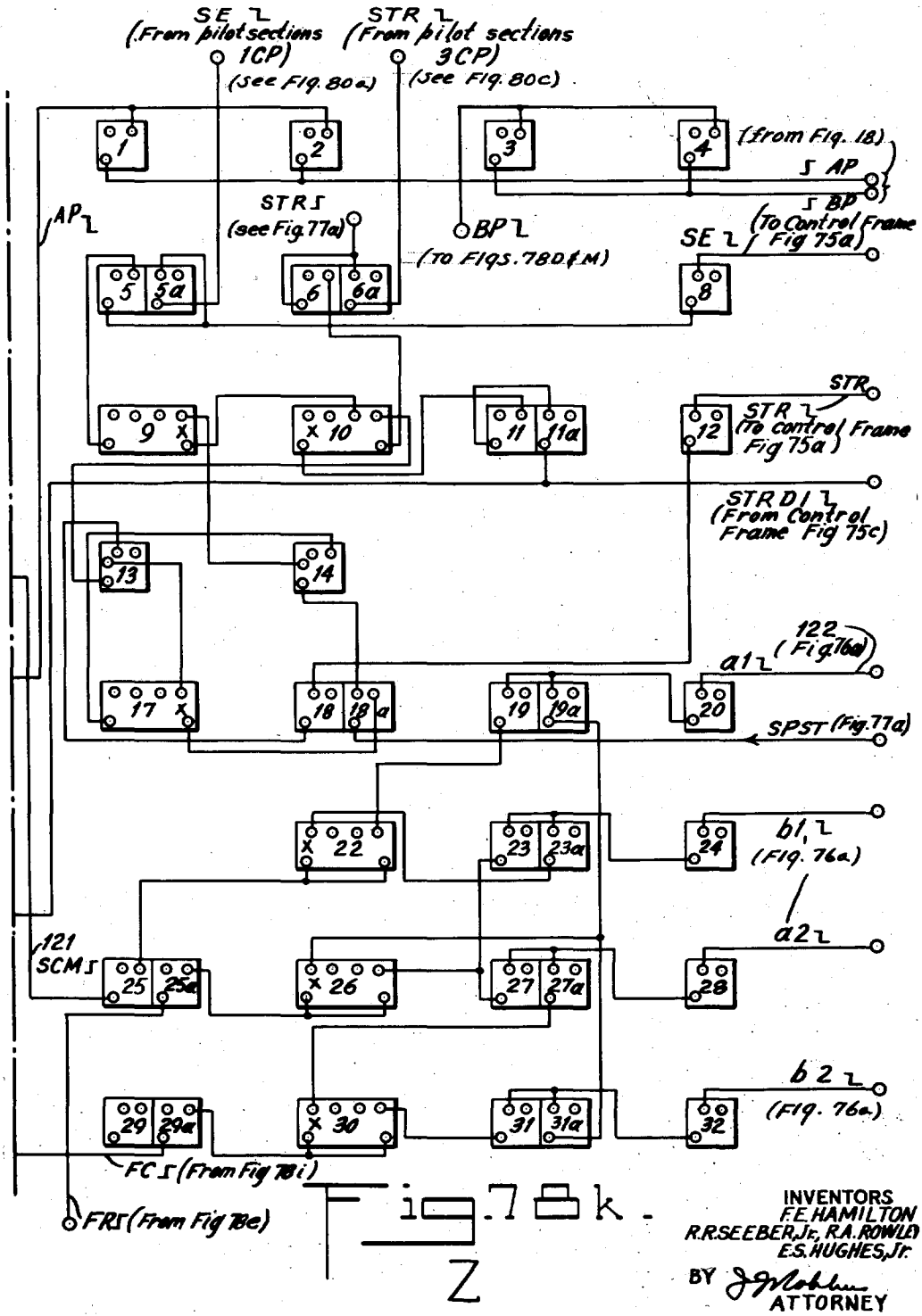

Fig. 78k.

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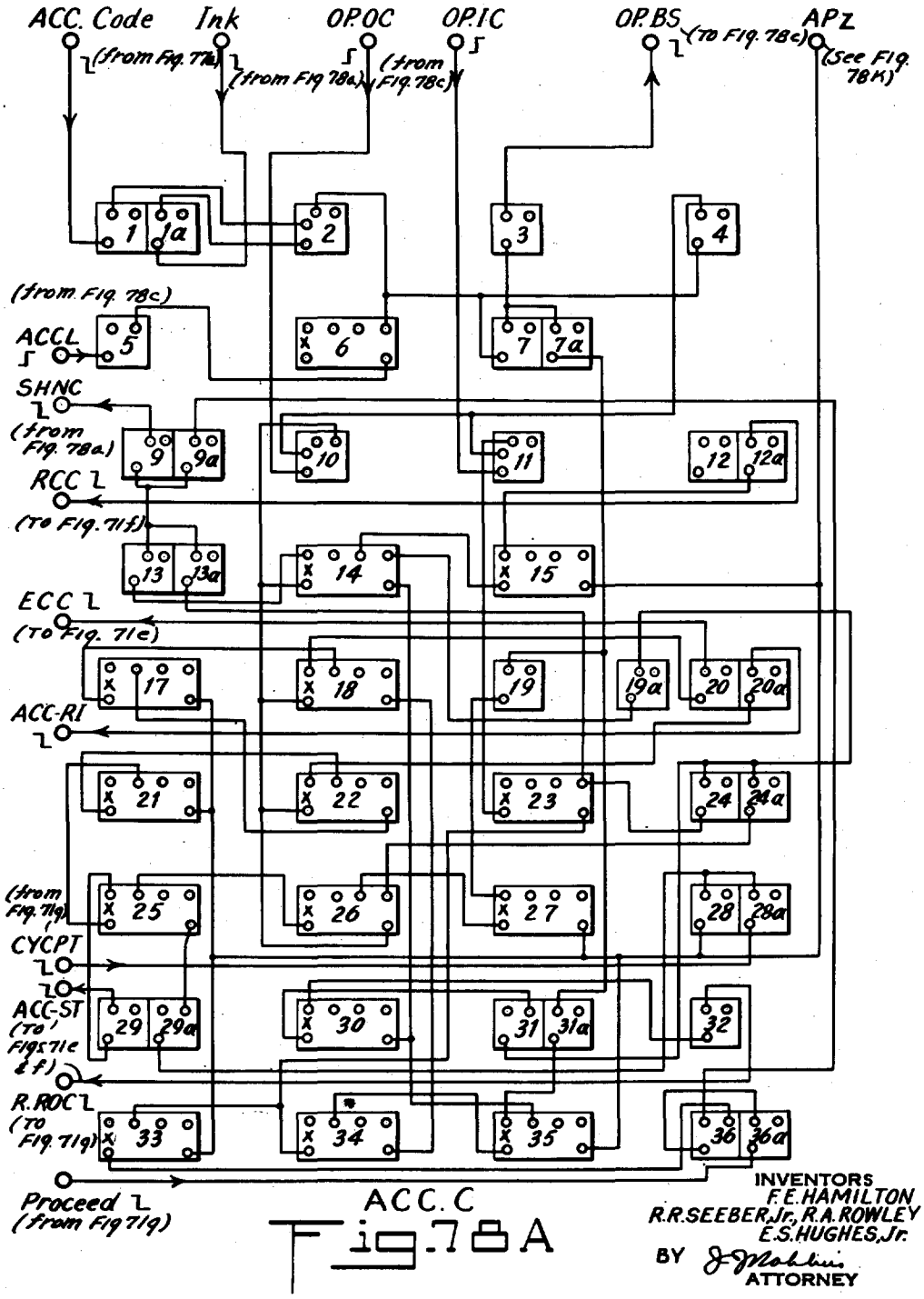
SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 125



ACC. C

Fig. 78A

INVENTORS
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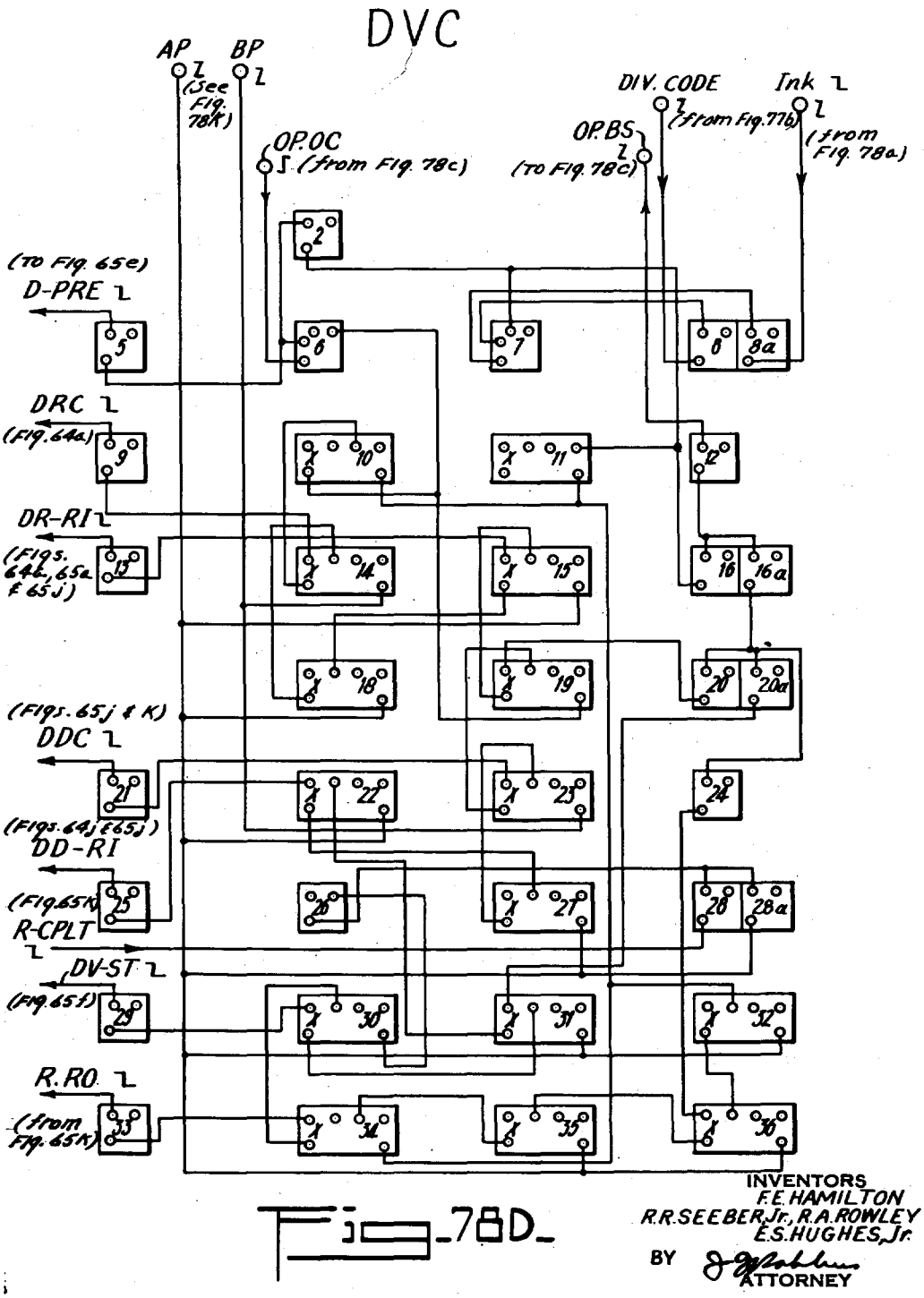

Fig. 78D

INVENTORS
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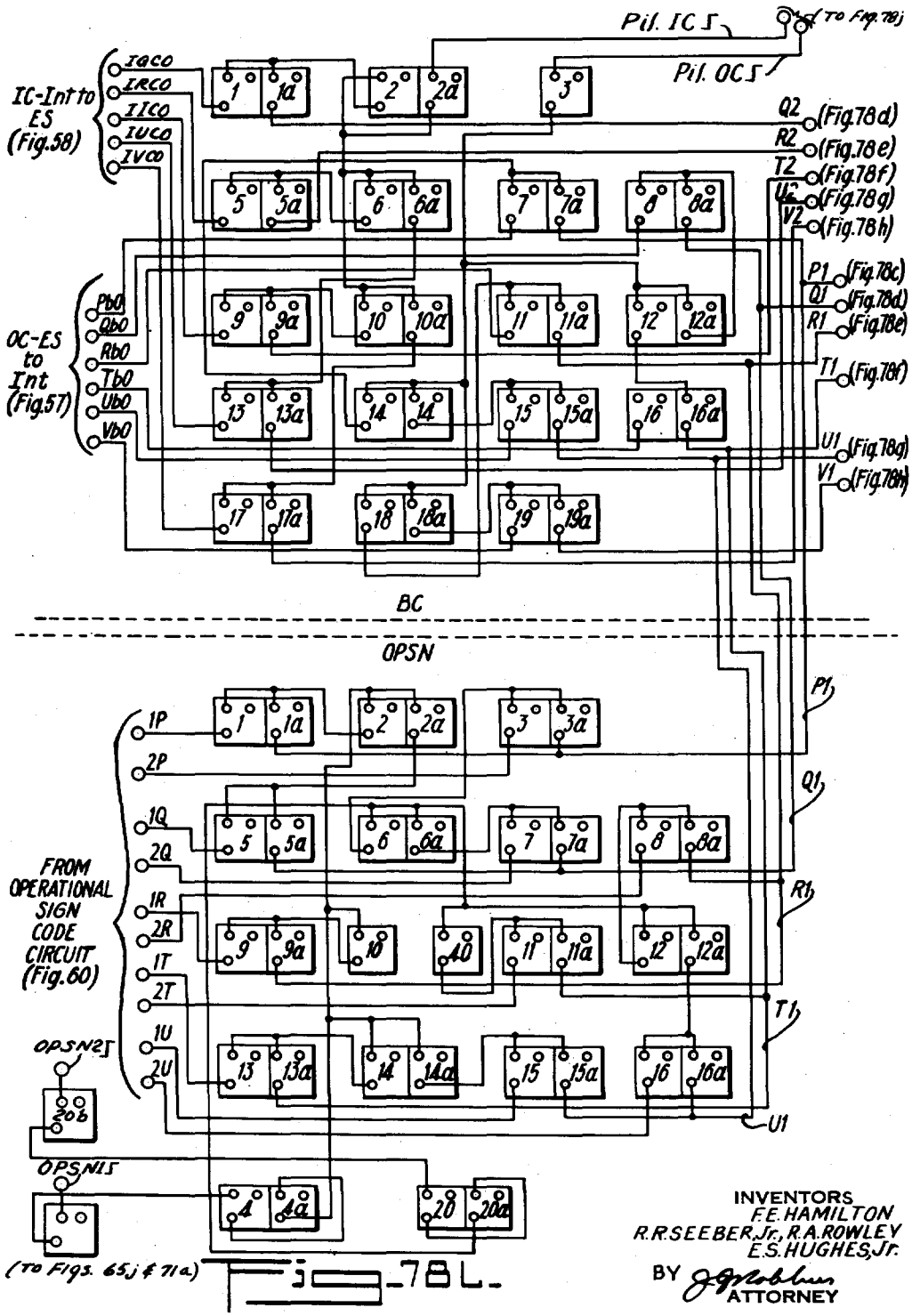
SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 127



INVENTORS
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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 128

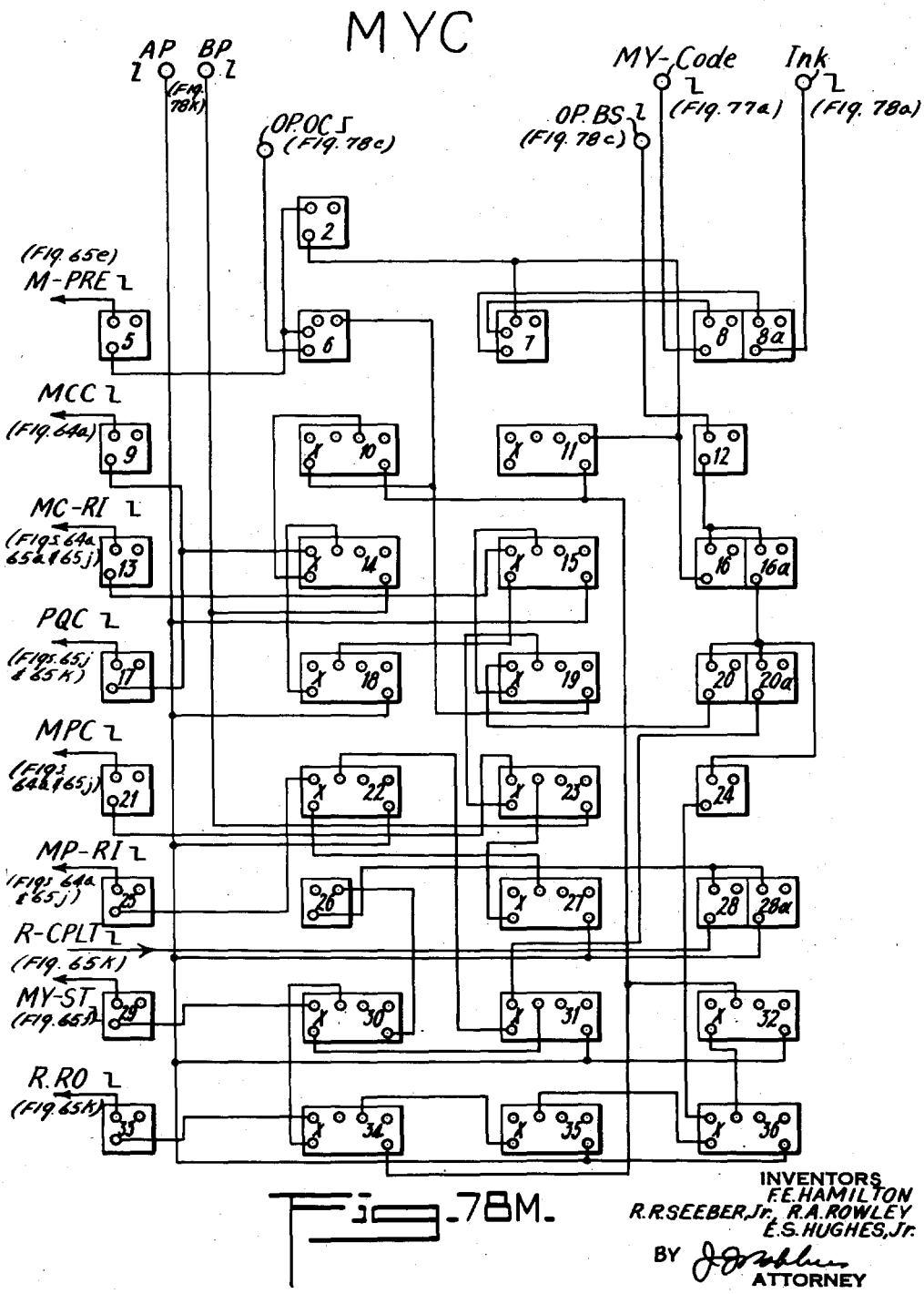

Fig. 78M.

INVENTORS
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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 129

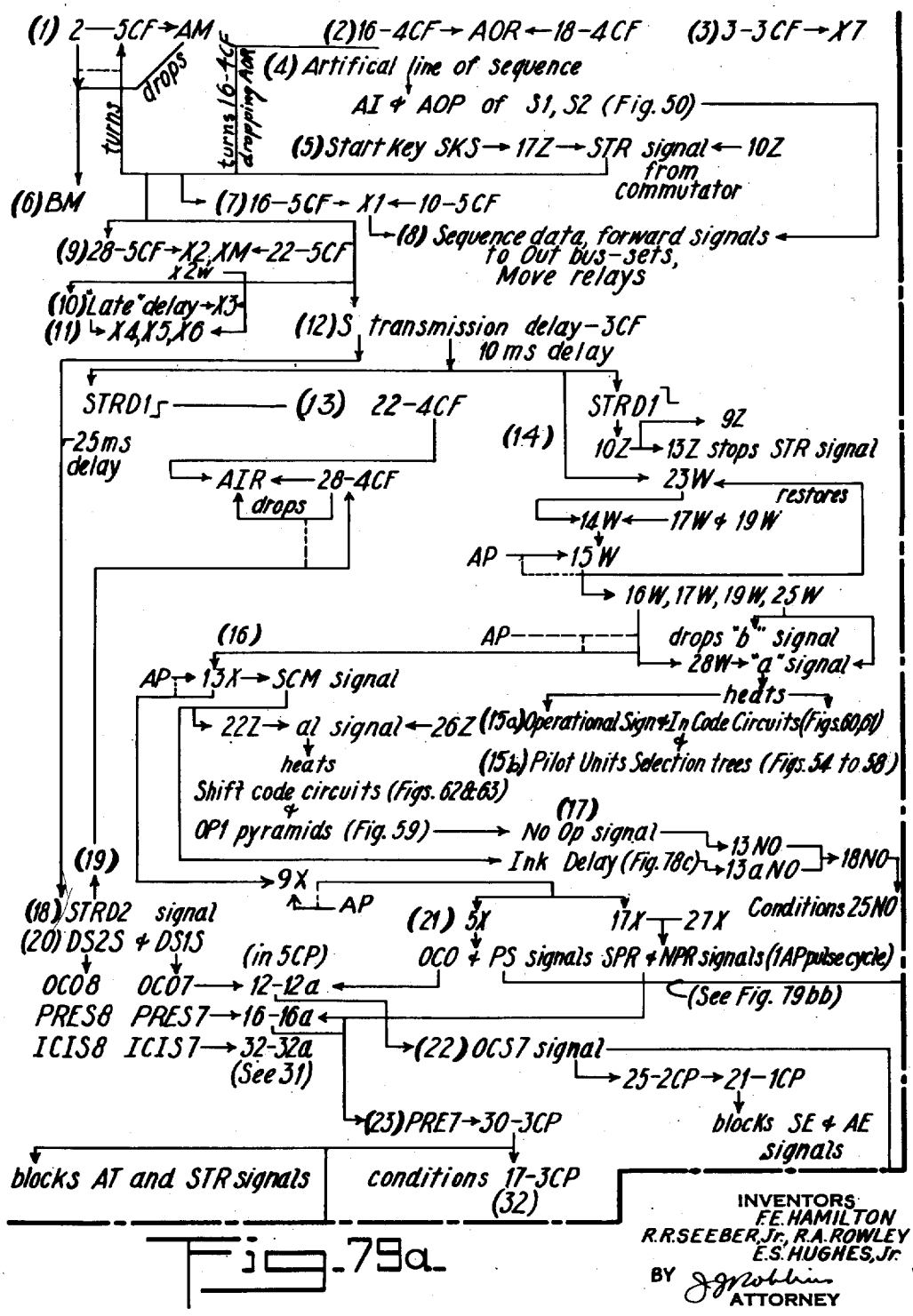

Fig. 79a

INVENTORS
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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 130

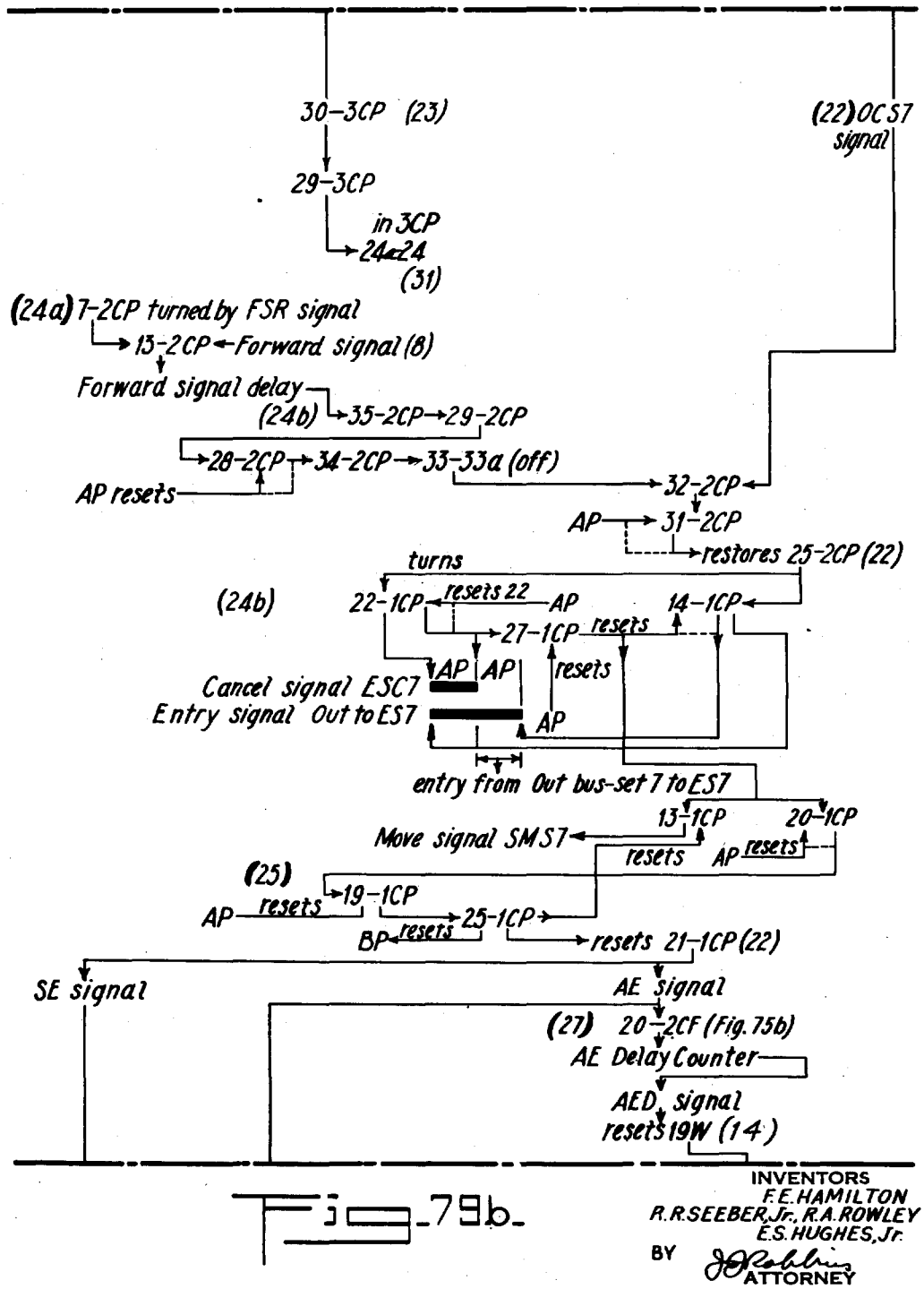

Fig. 79b.

INVENTORS
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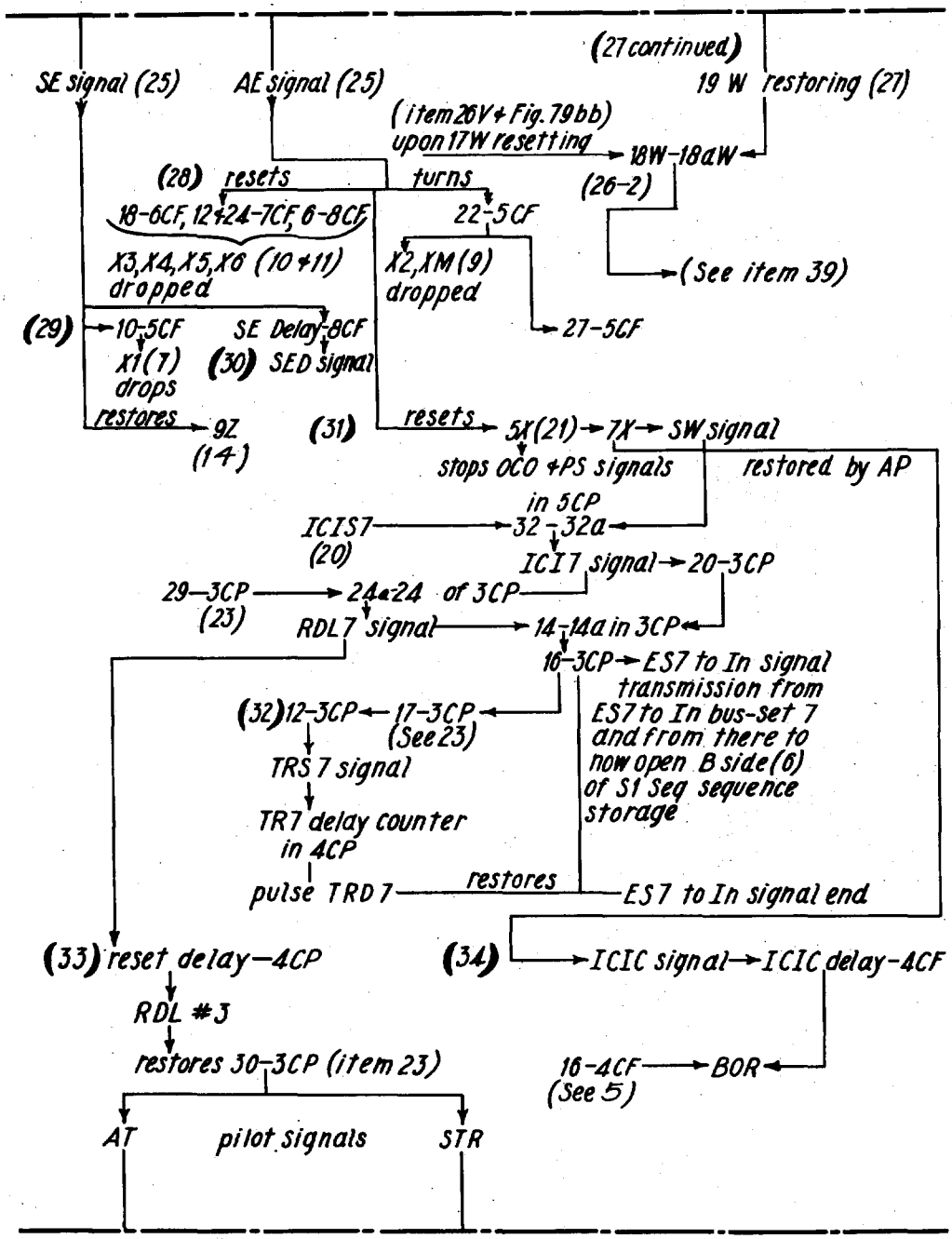

Fig. 79c.

INVENTORS
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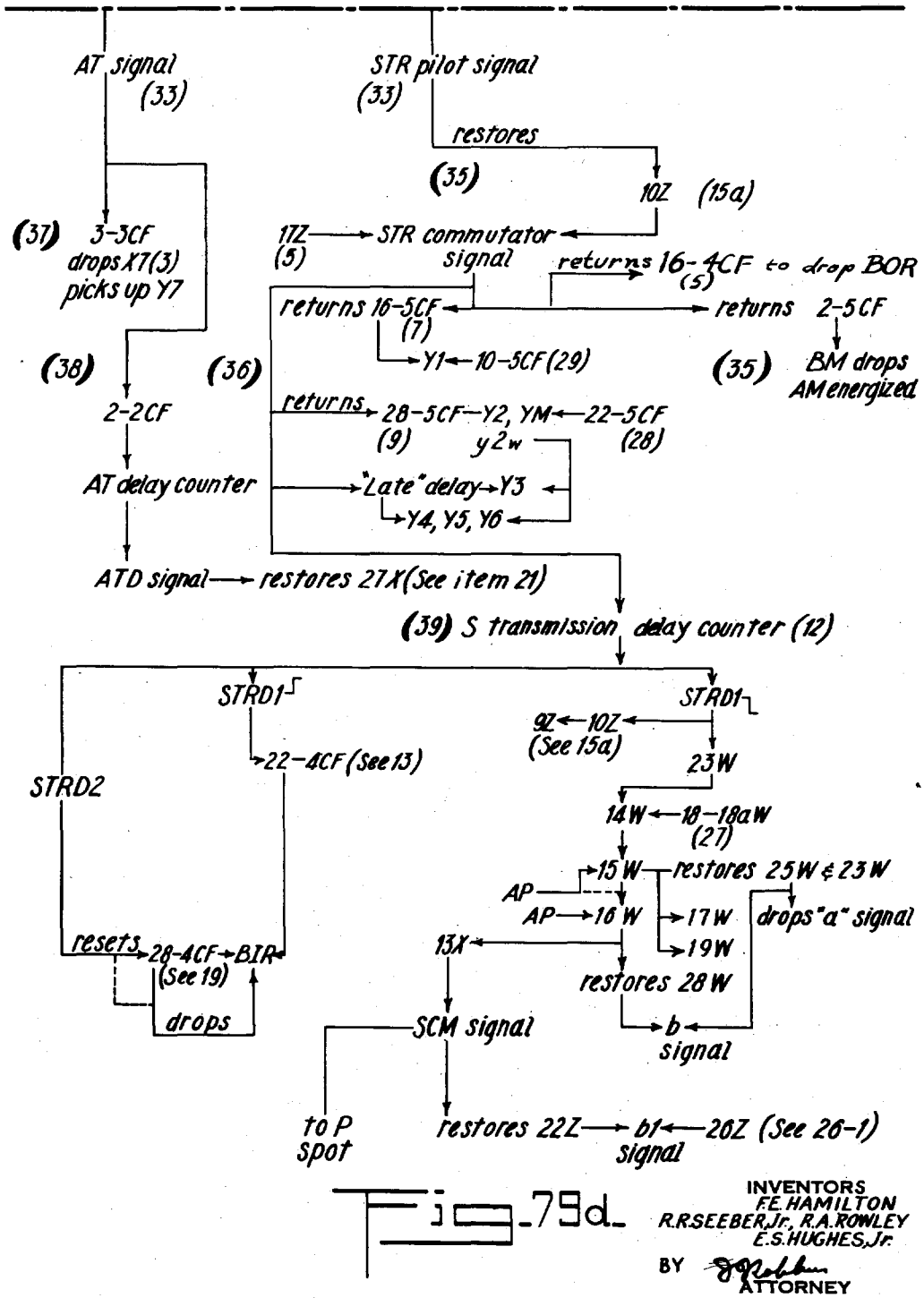

Fig. 79d.

INVENTORS
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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 133

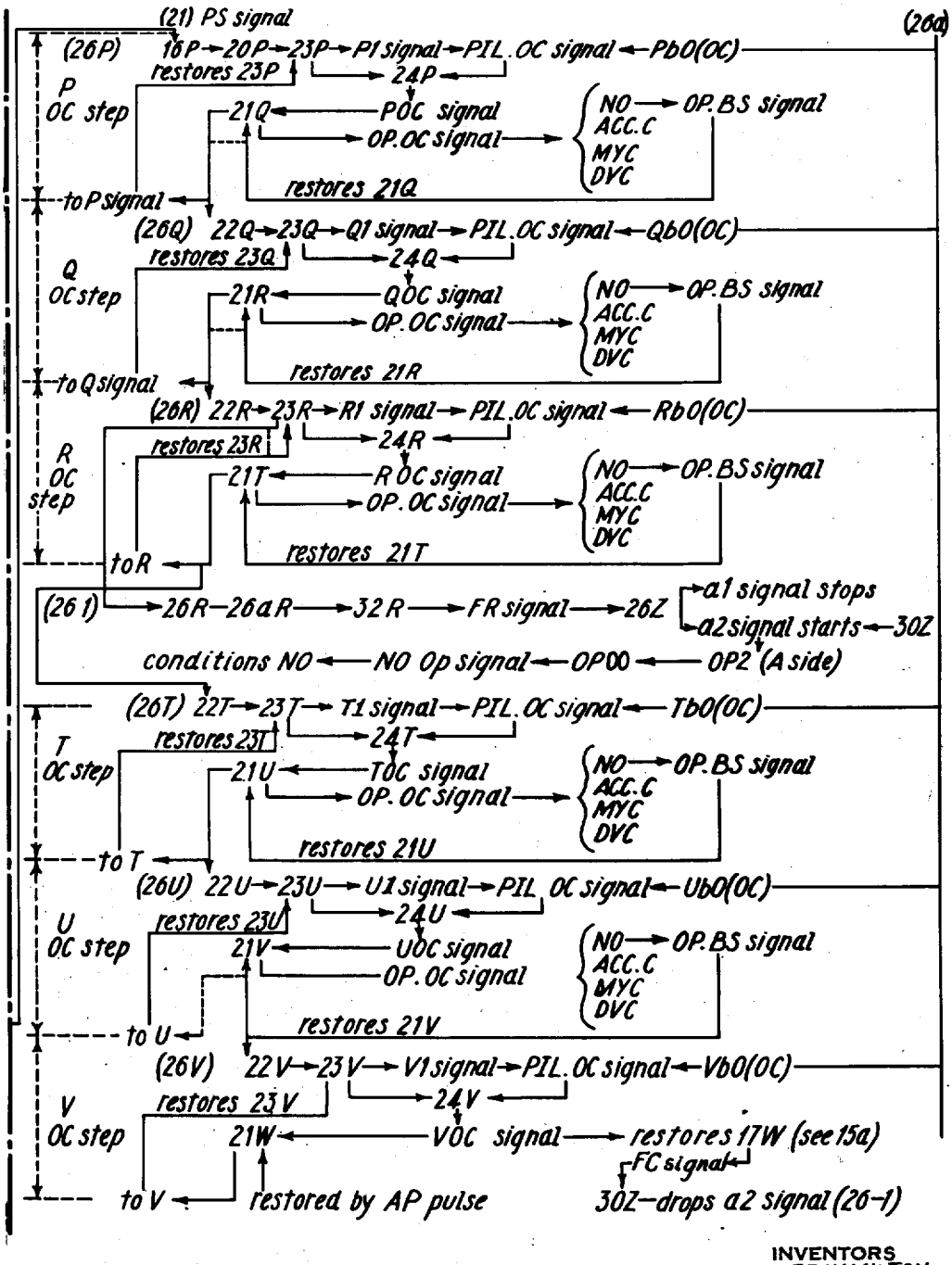

Fig. 79bb.

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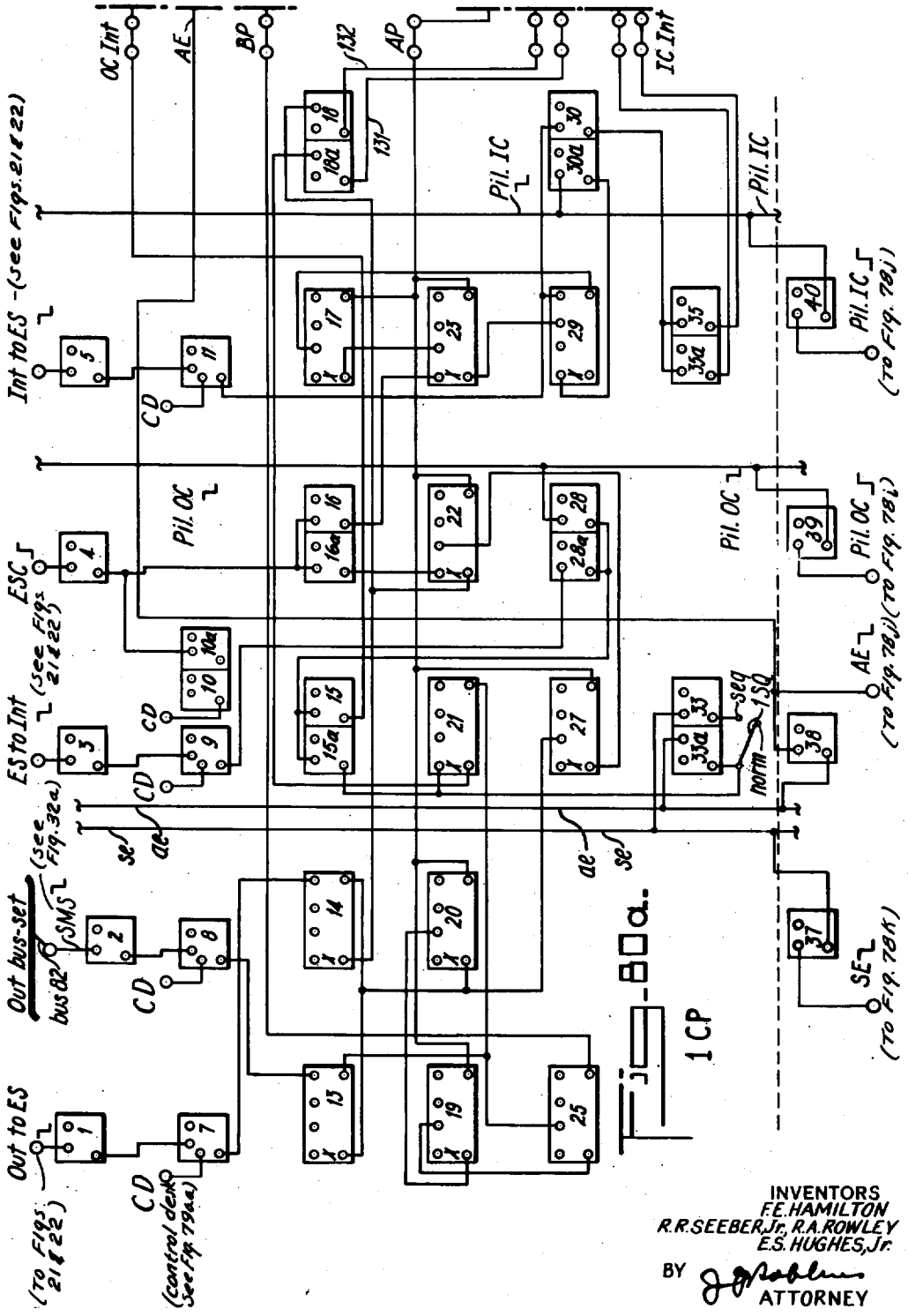
April 28, 1953 F. E. HAMILTON ET AL 2,636,672

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 134



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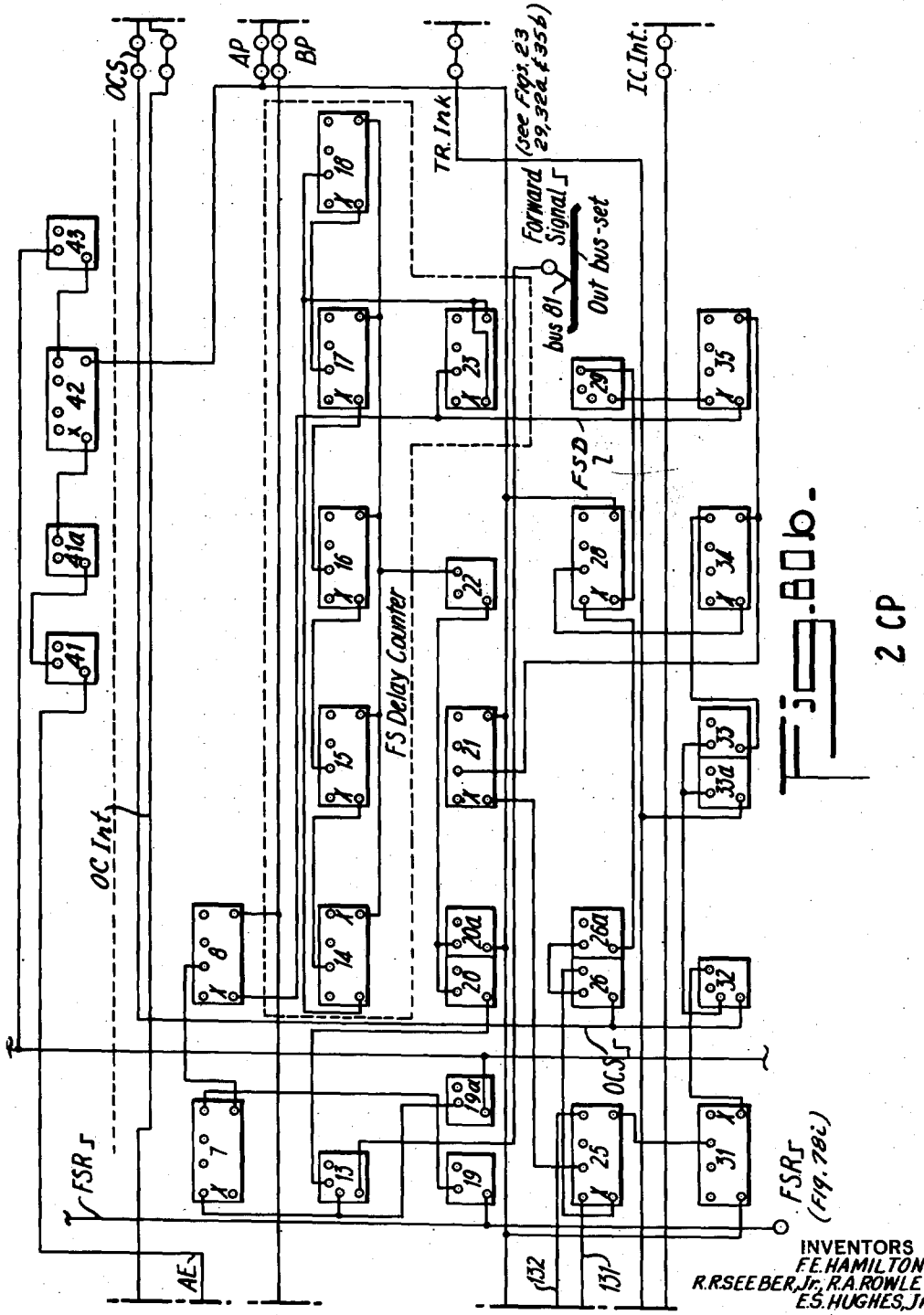
SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 135



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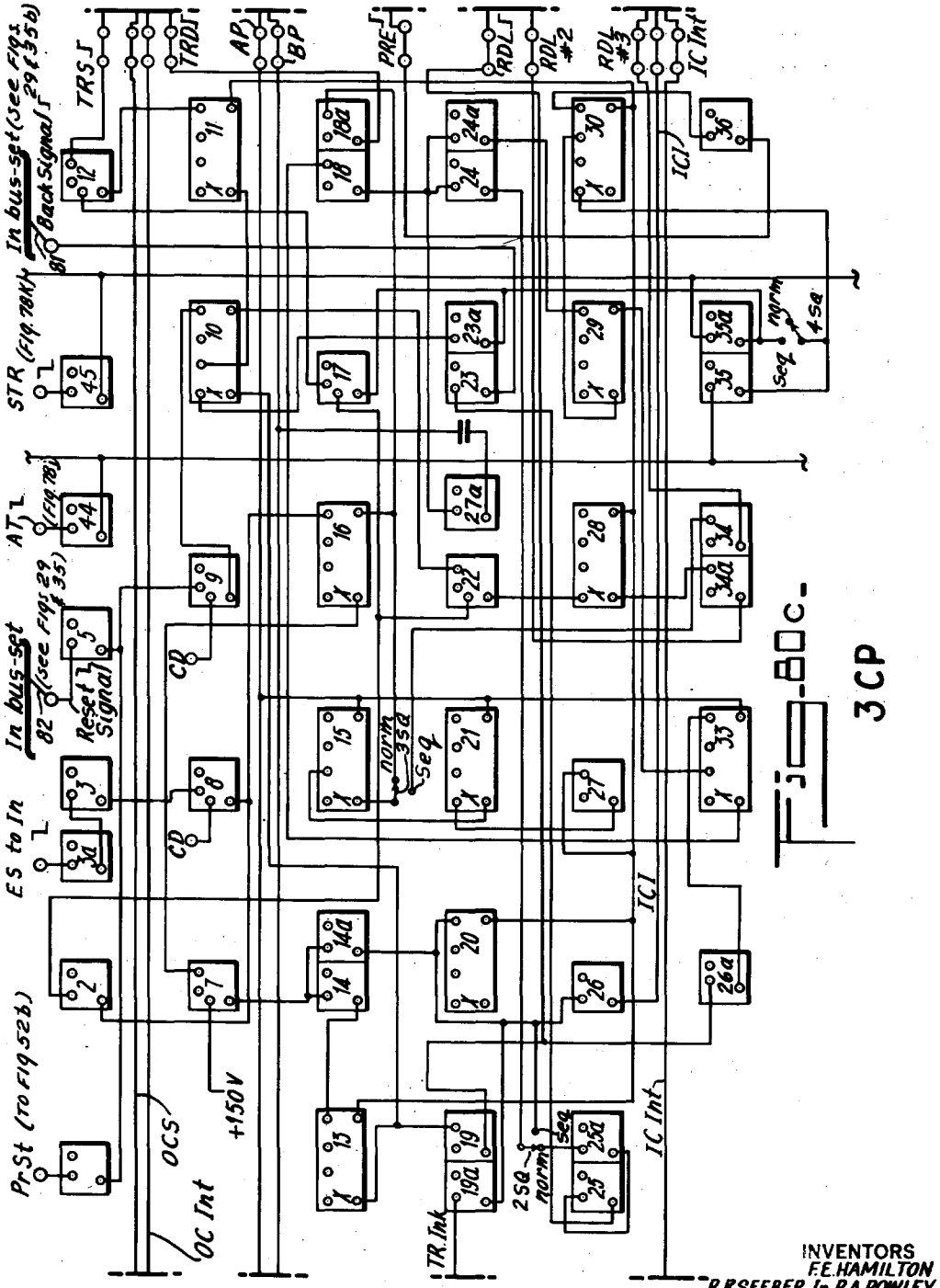
April 28, 1953 F. E. HAMILTON ET AL 2,636,672

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 136



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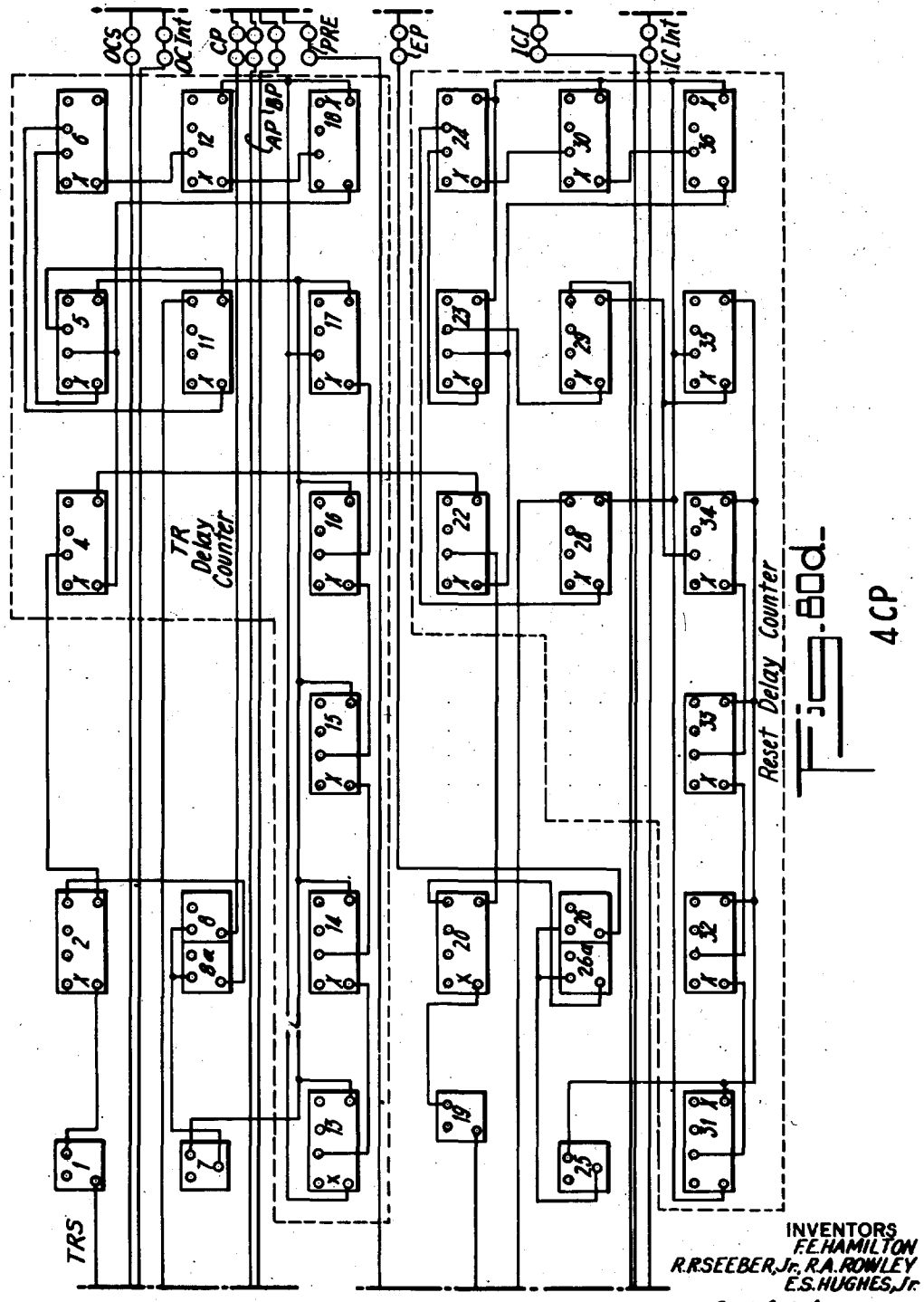
SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 137



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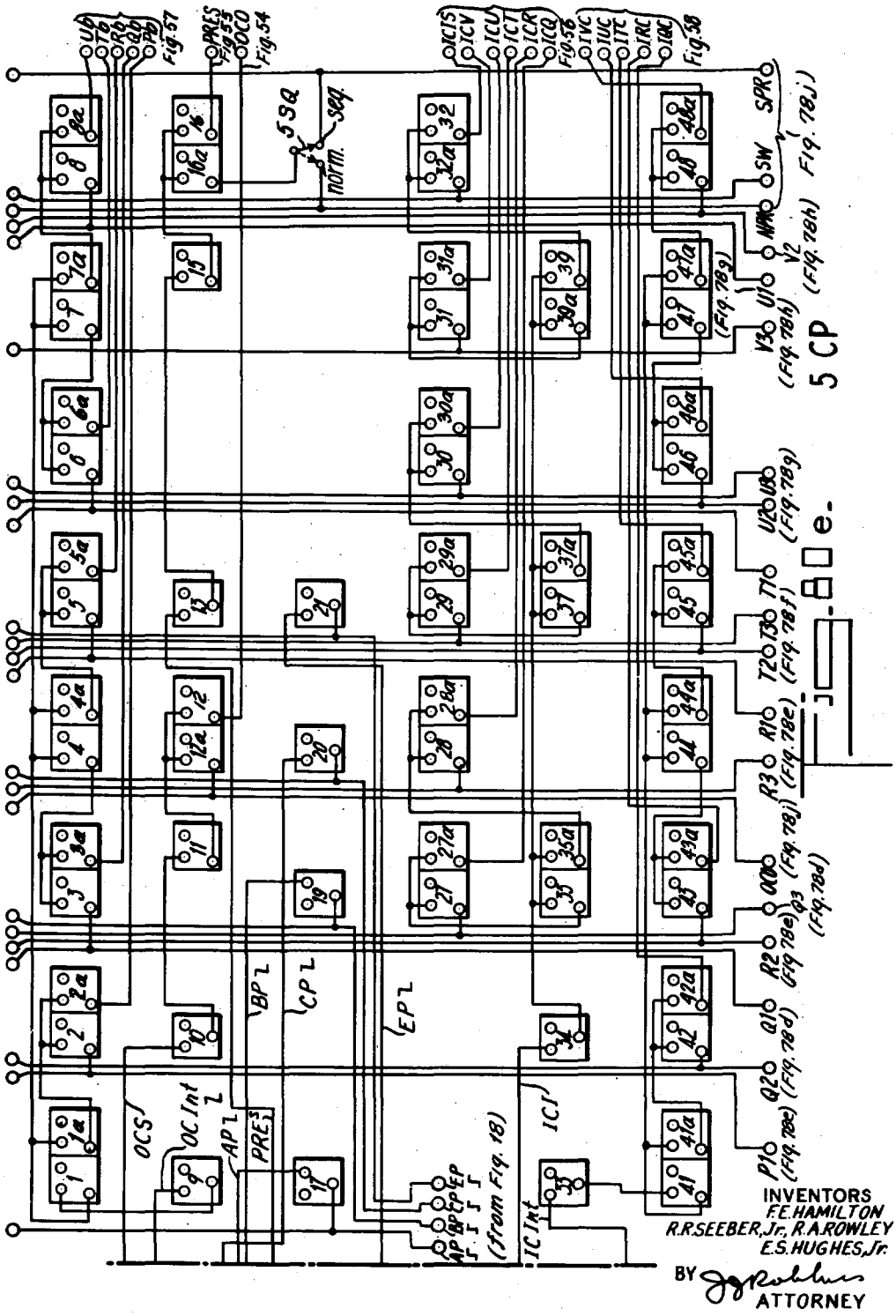
SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 138



INVENTORS
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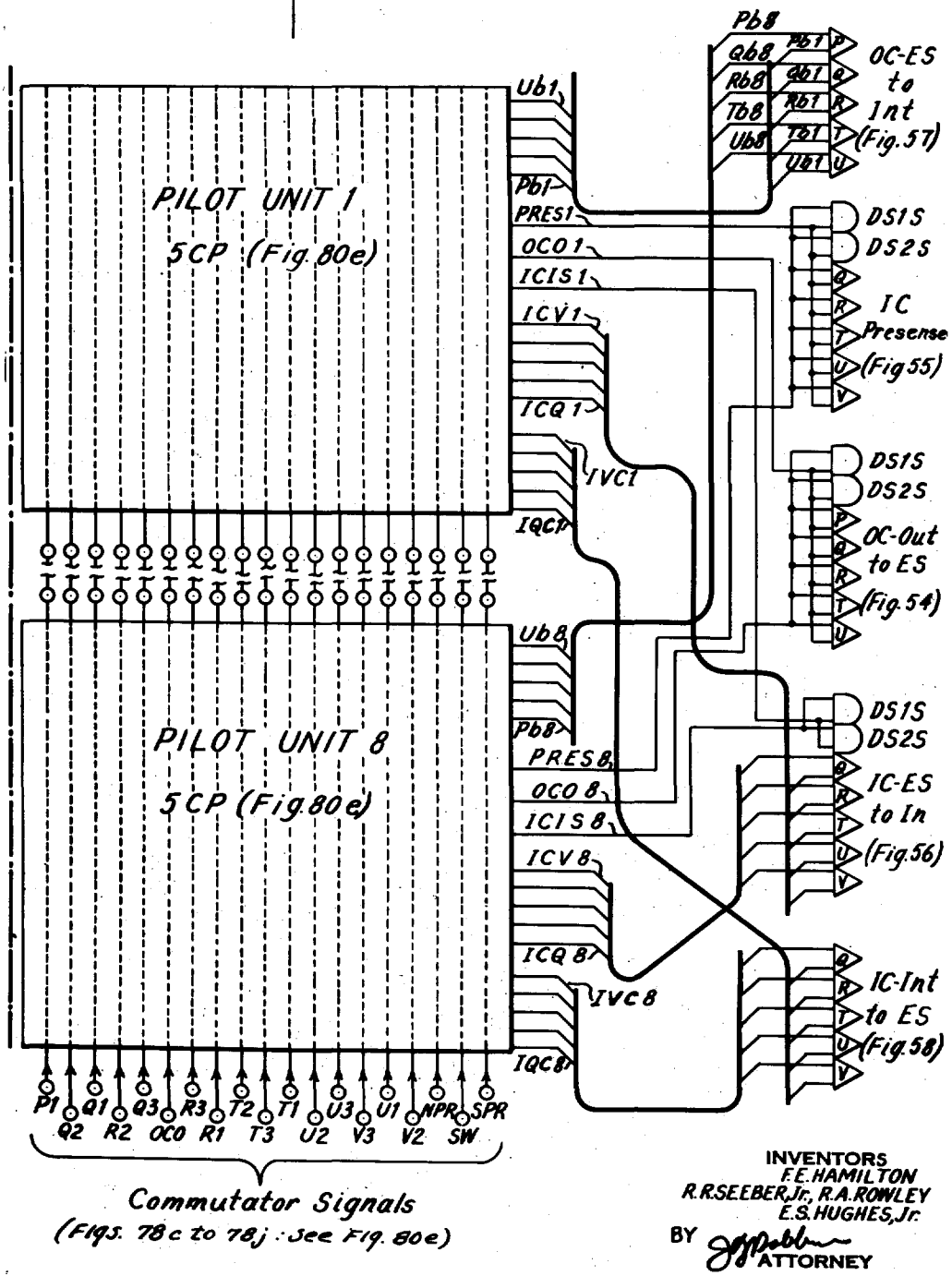
SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 139

Fig. 81a.



INVENTORS
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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 140

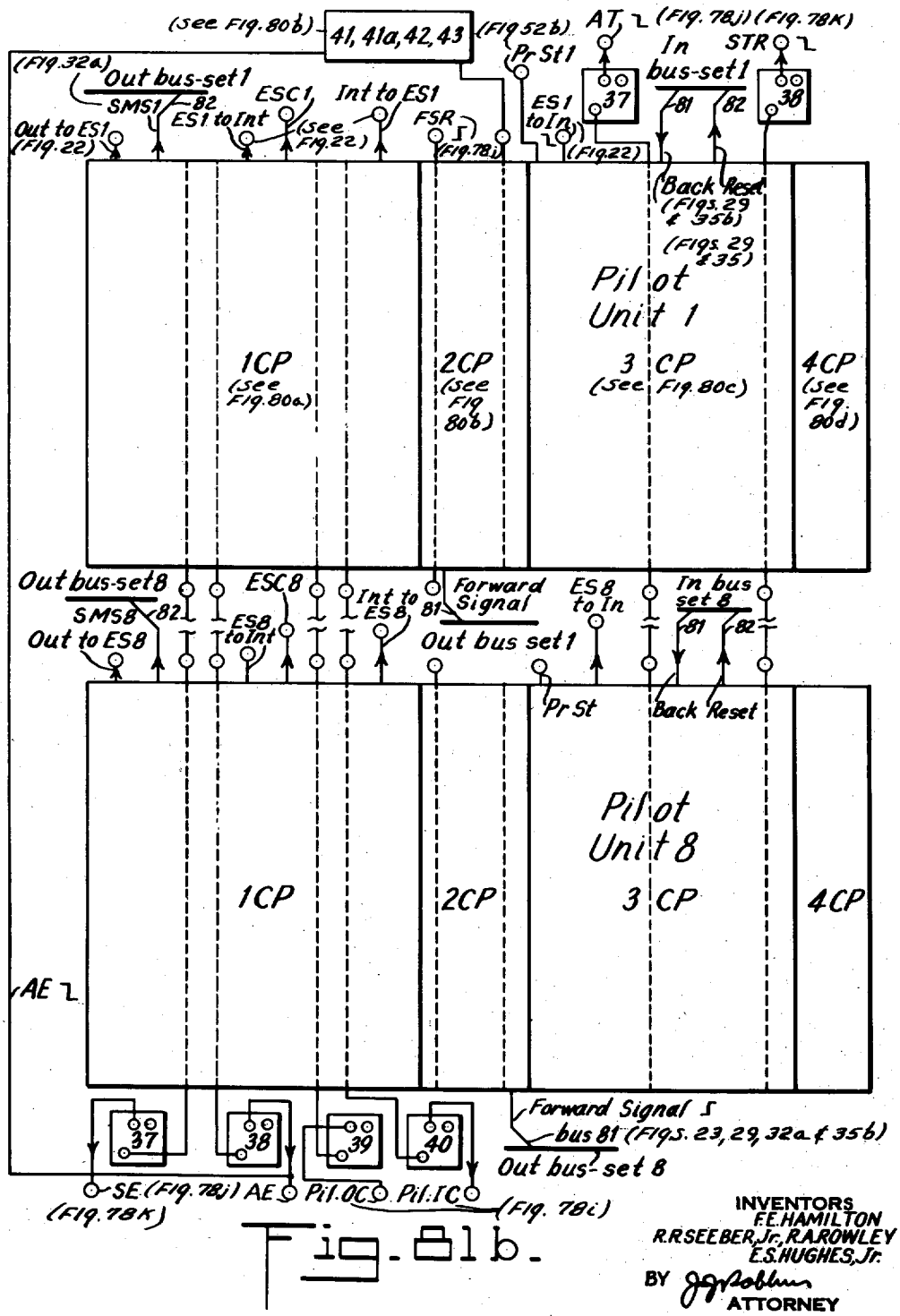

Fig. 81b.

INVENTORS
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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 141

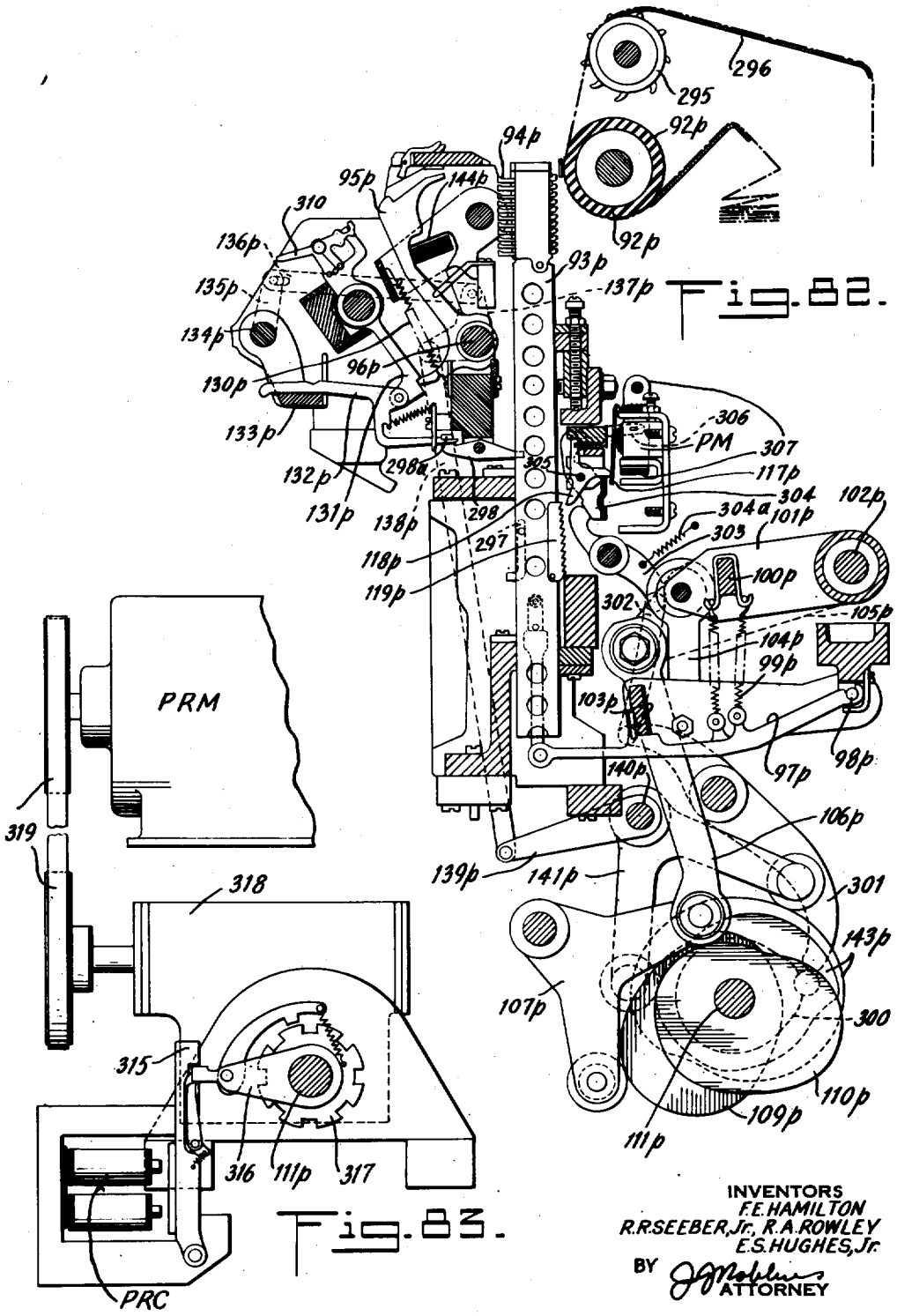

Fig. 82.

Fig. 83.

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April 28, 1953 F. E. HAMILTON ET AL 2,636,672

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 142

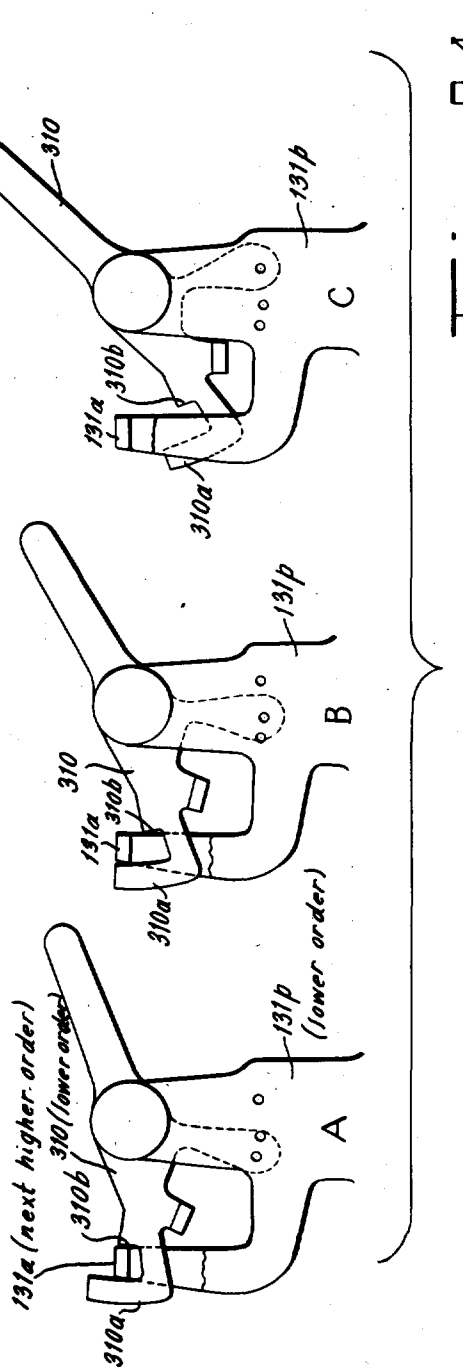

Fig. 4.

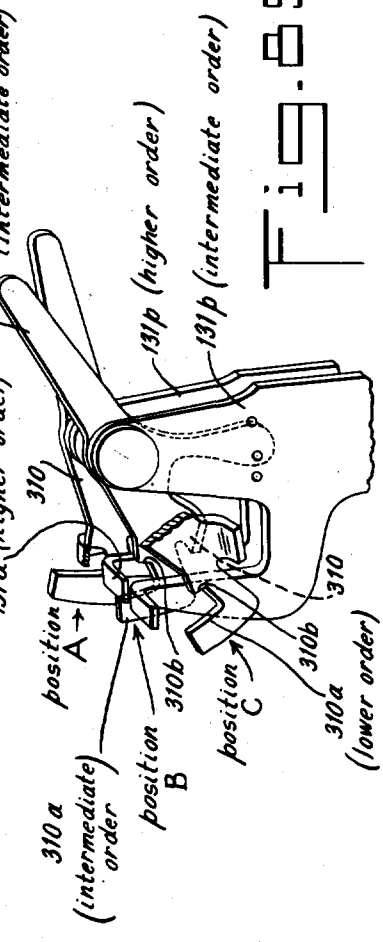

Fig. 5.

INVENTORS
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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 143

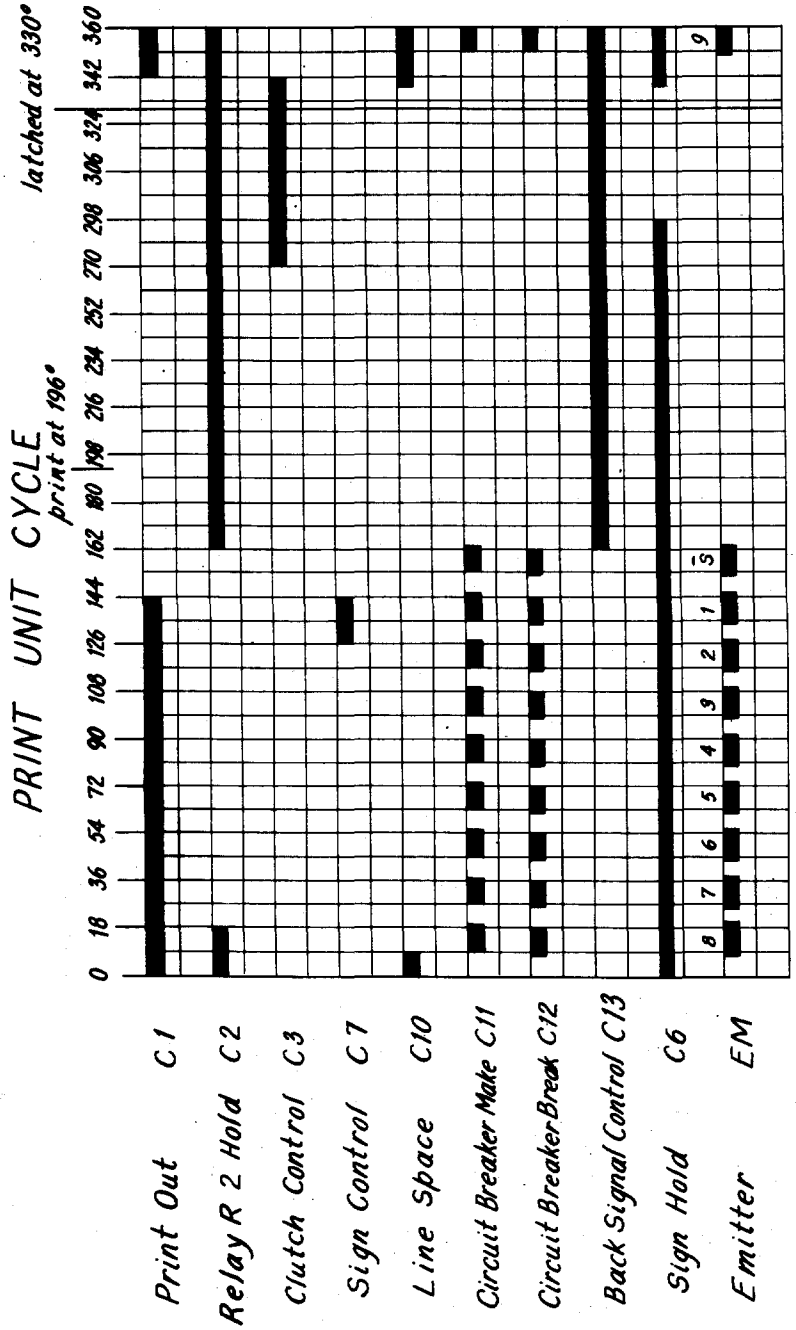

Fig-86-

INVENTORS
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SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 144

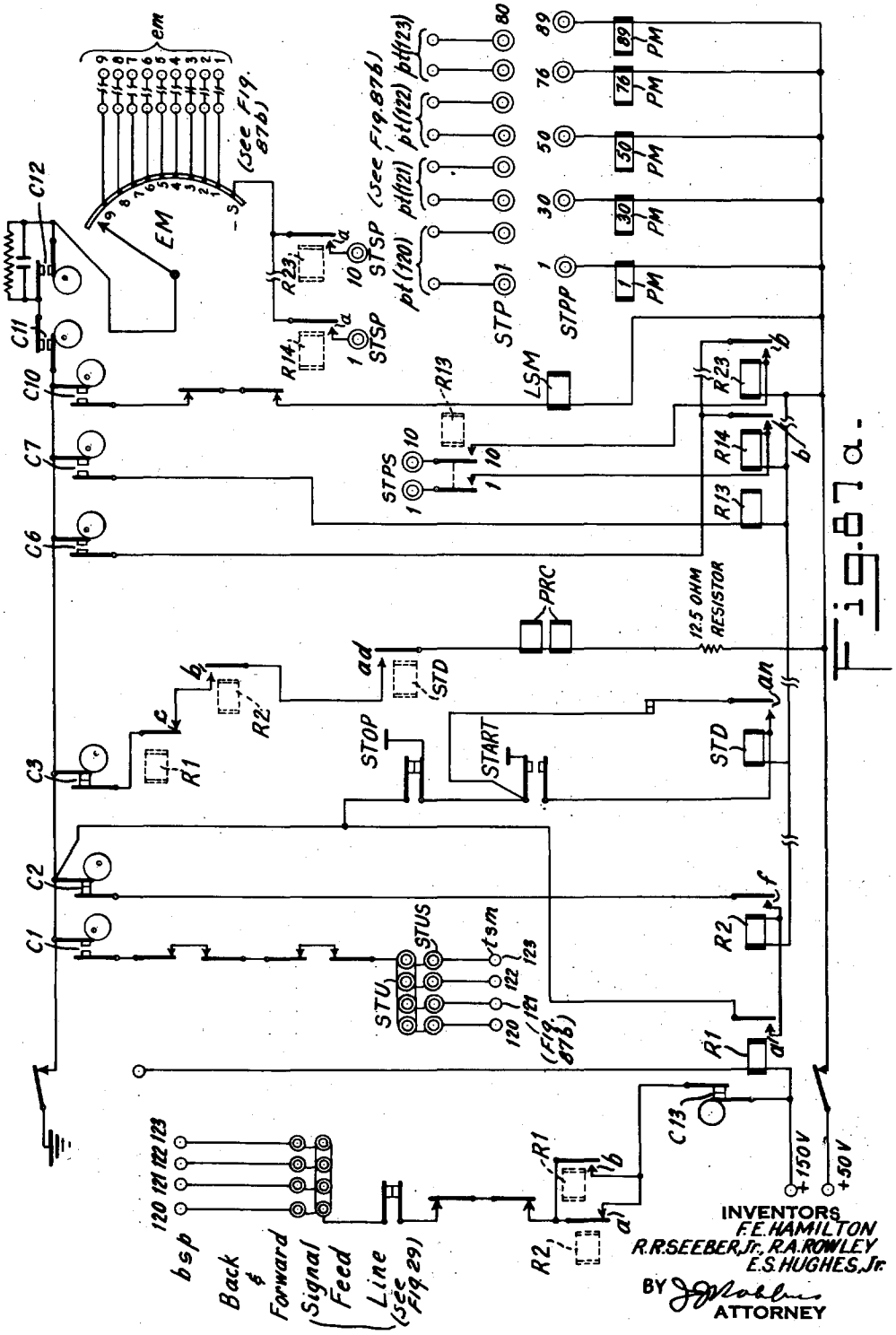


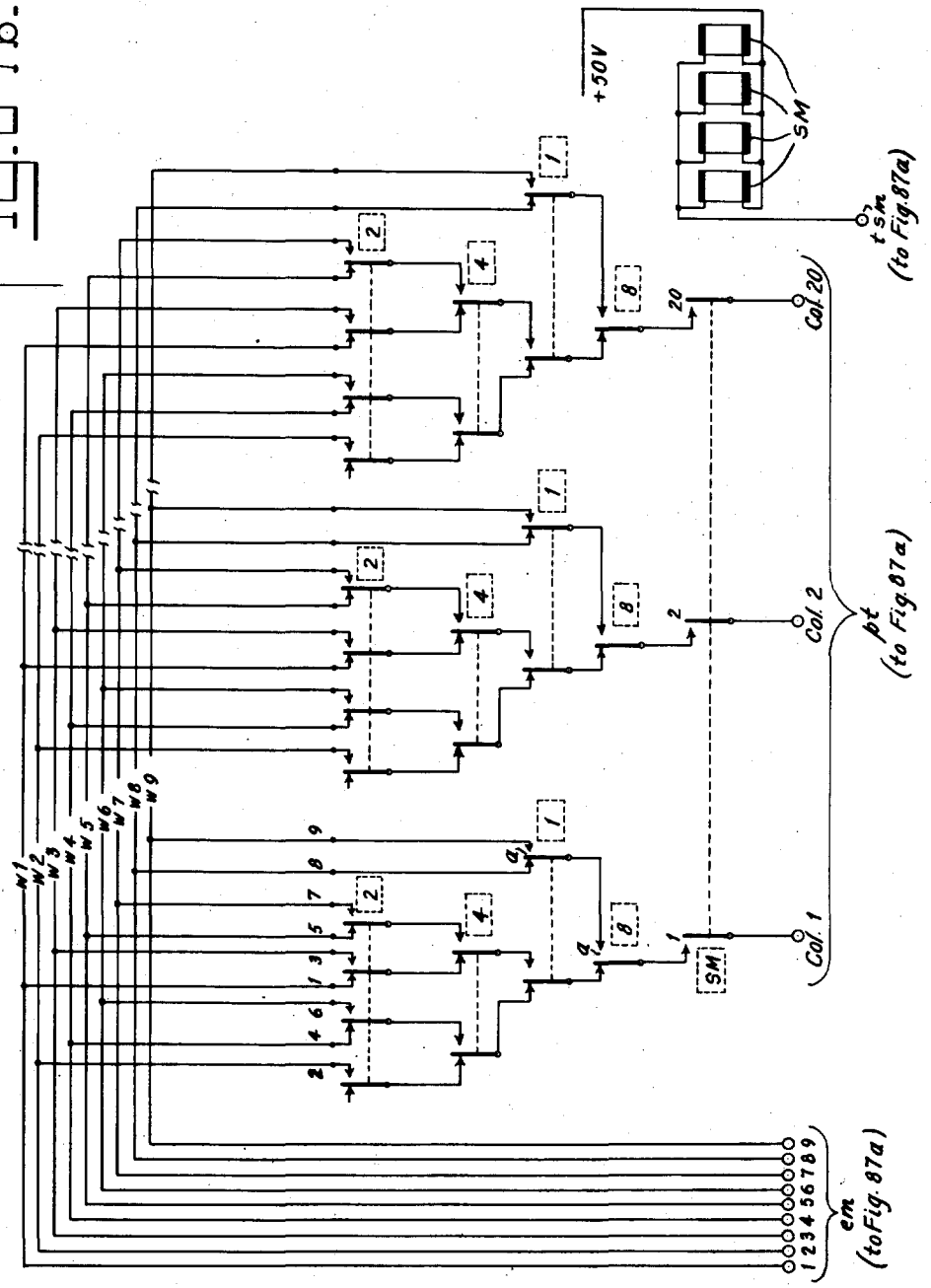
Fig. 87a.

April 28, 1953 F. E. HAMILTON ET AL 2,636,672

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 145

Fig. 87b.



INVENTORS
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April 28, 1953 F. E. HAMILTON ET AL 2,636,672

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 146

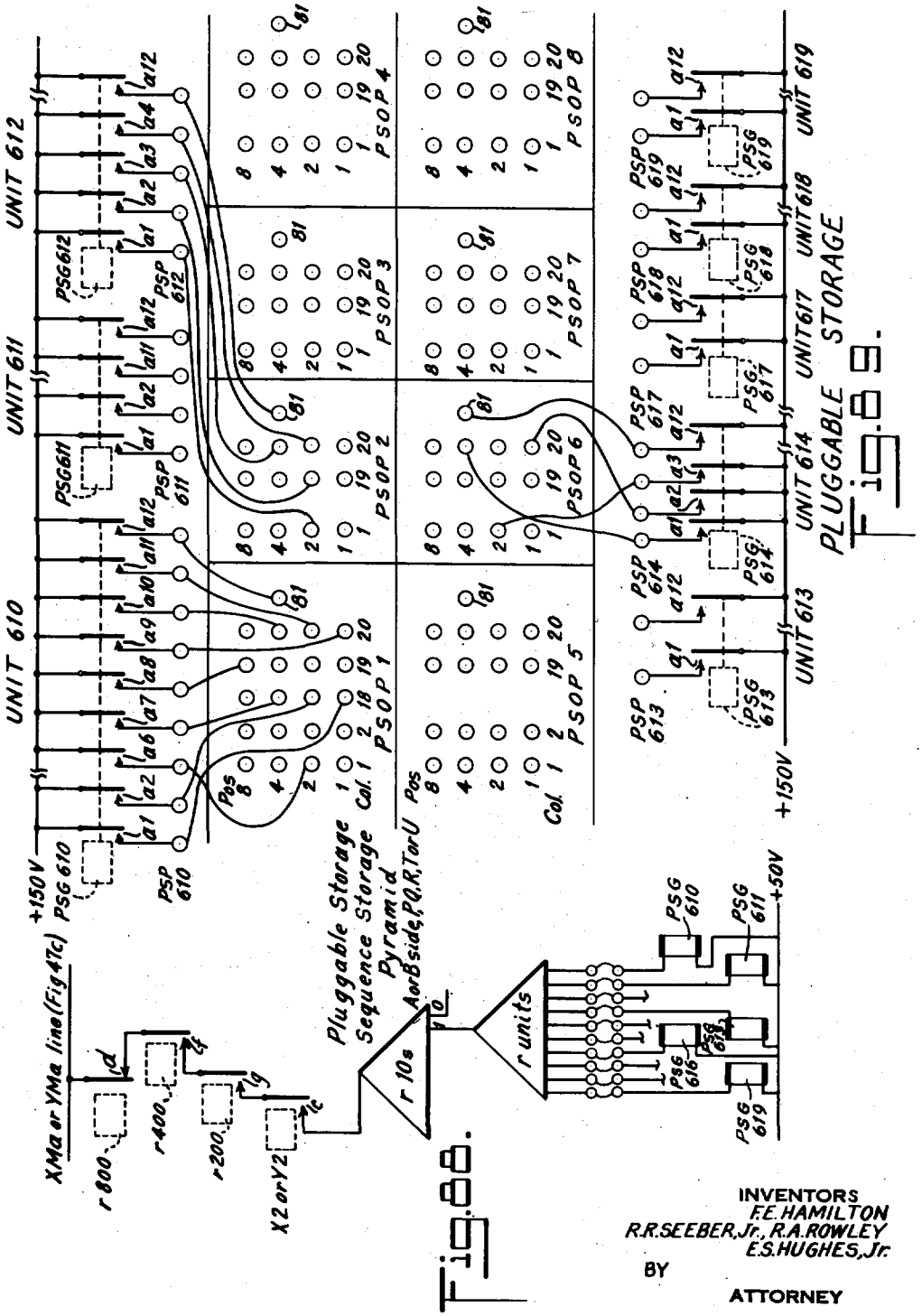

Fig. 9.

Fig. 8a.

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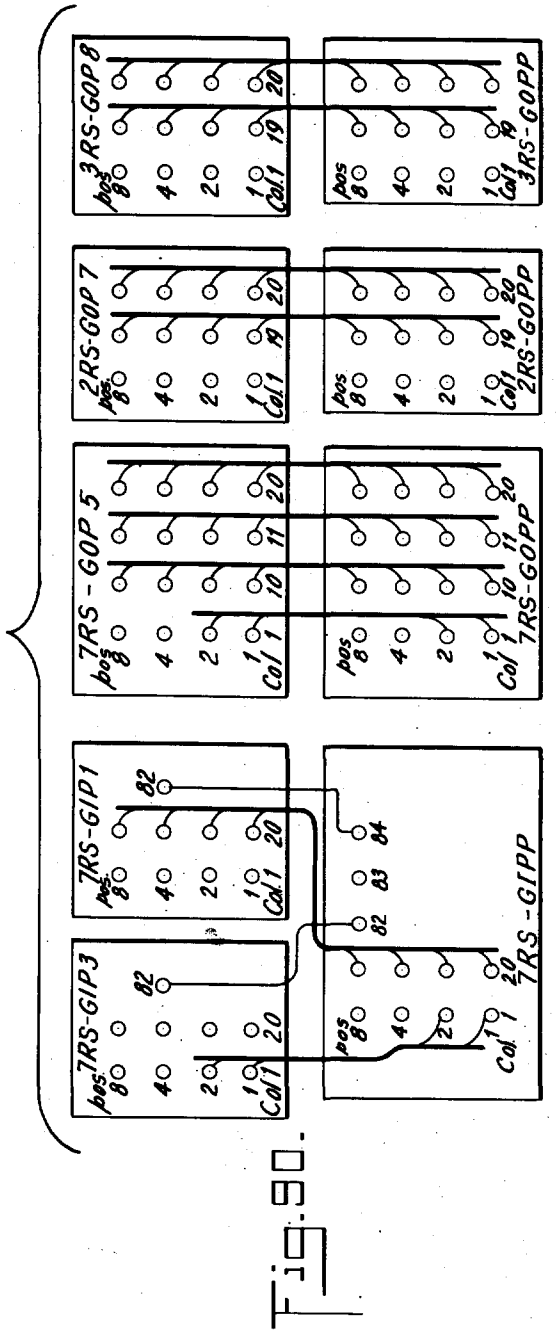

Fig. 90.

(Re: Section 24, Case 1)

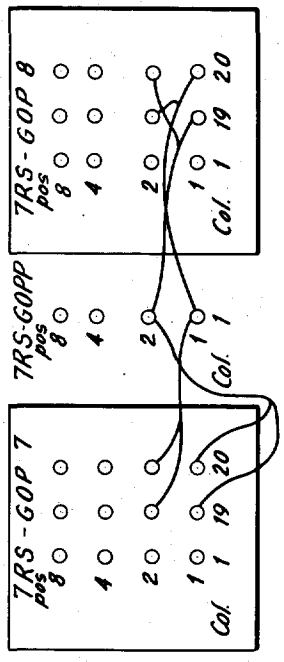

Fig. 90a

INVENTORS
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April 28, 1953 F. E. HAMILTON ET AL 2,636,672

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Filed Jan. 19, 1949 148 Sheets-Sheet 148

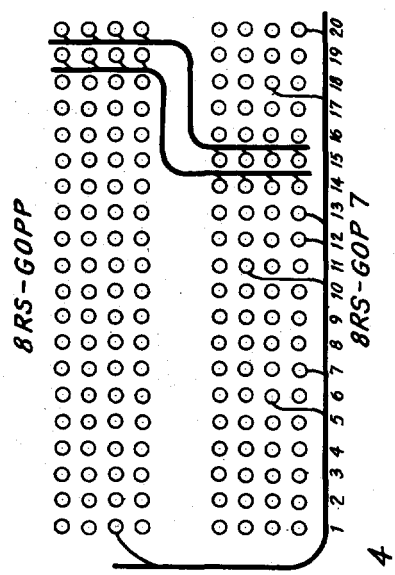

Fig. 92.

Case 4

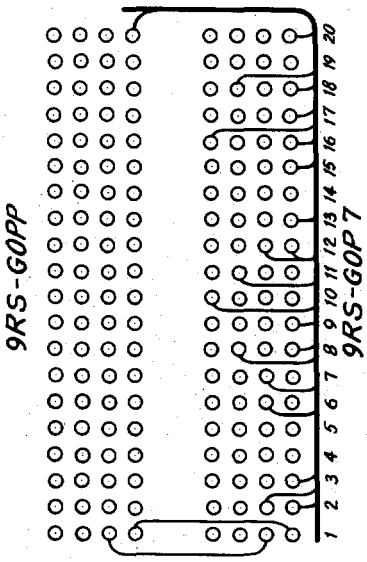

Fig. 94.

Case 6

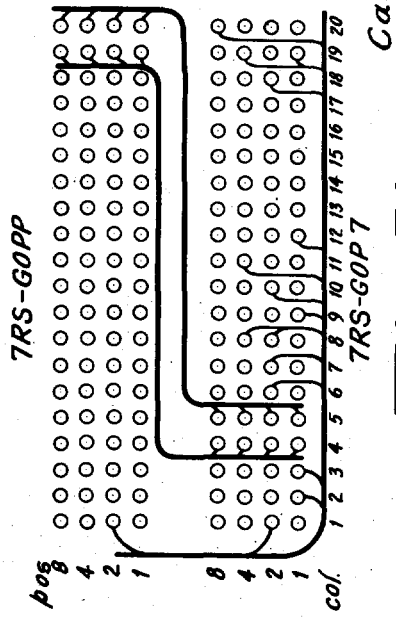

Fig. 91.

Case 5

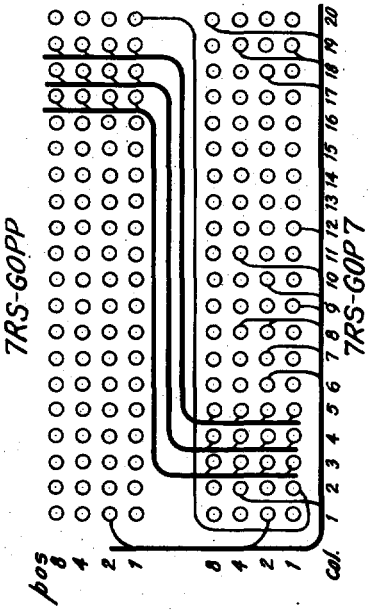

Fig. 93.

INVENTORS
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Patented Apr. 28, 1953 2,636,672

UNITED STATES PATENT OFFICE

2,636,672

SELECTIVE SEQUENCE ELECTRONIC CALCULATOR

Francis E. Hamilton, Endicott, Robert R. Seeber, Jr., Scarsdale, Russell A. Rowley, Binghamton, and Ernest S. Hughes, Jr., Vestal, N. Y., assignors to International Business Machines Corporation, New York, N. Y., a corporation of New York

Application January 19, 1949, Serial No. 71,642

110 Claims. (Cl. 235—61)

1

This invention relates to a computing apparatus, particularly one of the super-calculator class, and more particularly one which is directed by program means.

A programmed super-calculator has been disclosed in application Serial No. 576,892 of C. D. Lake et al., filed February 8, 1945, now Patent No. 2,616,626.

The general objective of the invention is the provision of a calculator which is superior to the calculator disclosed in the above identified application as well as to other calculators in many respects, including speed, flexibility, memory and productive capacity, and programming ability.

An outstanding object of the invention is to provide a calculator including units which perform their internal operations independently but are tied together externally by interchange of electric signals. According to the invention calculator elements are brought into operation concurrently or successively and by signal cross-talk among the elements arrived without collisions at desired calculation destinations.

The invention provides for interchange of signals among memory units, sequence means, and calculation units to control the transfer of data from memory to calculator units, performance of calculations and transmission of calculated results to memory in a directed interlocked manner. According to the invention, operations of calculator units may overlap and yet be directed to desired intersecting ends by signal cross-talk among the units.

According to the invention, cycles of operations involving transfer of data from memory to calculation units, performance of calculations on received data and transmission of results to memory are not carried out in fixed cyclic times but are effected in sequence runs of variable durations, determined by signal cross-talk among the calculator units.

The invention provides machine sequencing means having successive runs, producing in each run signals to initiate machine operations and which may begin a new run before all the operations initiated in the previous run are completed. In particular, the invention provides for selection of memory units to read out data before calculations on data previously received from memory have been completed or before the results of these calculations have been transmitted to memory. The invention also provides for entries of data from selected memory units into a calculator section to be made before the calculator transmits the results of calculations on previously entered data to memory units or while

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such transmission is taking place. With respect to any memory unit selected to send data to the calculator section and to receive the result of the calculation, the invention provides for a signal interlock to indicate when the unit has completed reading out its data and to then allow the unit to be conditioned to receive data.

According to the invention, data may be entered into a calculator section and a calculation performed thereon while the result of a previous calculation is still in the calculator section or before or during the transmission to a receiving unit of the result of the previous calculation.

The invention provides for automatic signal control of single-timed electrical transfer of data between calculator units.

The invention also provides for an automatic resetting of a data receiving unit as an accompaniment to application of new data to said unit. Stated otherwise, each time entry into a unit is called for, the unit will be cleared for reception of the new data as a result of receiving a reset signal either simultaneously or just before the entry signal is applied to the unit, and automatic sequencing of the reset and entry signals will occur.

Another outstanding object of the invention is the provision of a program means for a calculator apparatus which is more flexible and selective and of greater capacity than previous program means.

The invention provides for the programming of the program means itself. More specifically, the derivation of program data from a source may be programmed by means controlled by other program data. According to the invention, the program data may be obtained from different sources and the application of program data from one source to a programming device may be programmed by and according to program data in another source. Further, the invention provides for program means to receive program data and to control according to an item or items of the program data the selection of future program data from the same or another source. Stated differently, certain program devices have program data applied thereto to determine calculation programs and other program devices have program data applied thereto to select subsequent program data to be applied to the program devices.

Still another outstanding feature of the invention is the computation of sequence data. According to the invention, the program data are numbers which can be modified, enter into cal-

culations and be derived from calculating means. The program data are arranged in sets of instructions for selection of memory units to send out data, to receive data, of calculator units to perform calculations, selection of channels of communication between memory units and the calculator section, selection of operational signs for numerical data to be used in calculations, selection of amounts and directions of column-shifting of results to be effected by a column-shifting unit, and of the source for the next set of program data. The invention provides for computations of any one or more of these program instructions.

An object of the invention is the provision of means for shifting the columnar relation of a number being sent from one unit to another through a number of columns selected by program data. Further, the invention provides a column shift means which may shift a number to the right or to the left as directed by program instructions.

Among many other objects of the invention are: the provision of means to direct entries of data from memory units to a calculator section and to produce an entry completion signal which notifies sequencing means that it may proceed to initiate subsequent entries; the provision of means for directing transmission of data to memory units and production of a signal notifying the sequencing means that transmissions have been completed and that it may proceed to initiate subsequent transmissions; the provision of multiple program units for alternately receiving program data and alternately coacting with the sequencing means in operating the calculator apparatus through the programs defined by the program data; the provision of means for directing data to be read out of record material and moving or not moving the record material after data have been read out in accordance with the conditioning of move circuits for response or rejection of move signals; the provision of signals from memory units notifying the sequencing means that they are ready to send forth or to receive data; and the provision of recording means controlled by program data to record data after transmission of data to memory units which read out their data to the recording means.

Other objects of the invention will be made clear in the general and detailed descriptions of the machine and be understood from the claims.

1. *A brief outline of the machine*

Fig. 1 is a schematic diagram of most of the units of the machine and of their relationship.

A calculator section composed entirely of electronic circuits and devoid of moving parts has three calculator units, an accumulator, a multiplying and dividing unit (MD), a denominational or column shift unit. These coact with eight electronic storage units which have independent inputs and outputs in addition to the In and Out connections to the calculator section (see Fig. 20). The units of the calculator section are in communication through a single data channel, called the Internal bus sets and which may be considered as having an Out side from which data flows through an amplifier to an In side. All numbers to be used in calculations are transferred from selected memory units through eight selective channels called Out bus-sets to the eight electronic storage units, respectively and then called out one at a time from the latter units to the selected accumulator unit or the MD unit. All results obtained by the MD unit and the accumulator unit are sent to the denominational shift unit and after being shifted a desired number of places to the right or to the left are sent to selected electronic storage units. The results may then be transmitted from the electronic storage units to selected memory units by way of eight selective channels called In bus-sets. The electronic storage units may be called rapid transit data memory units since numbers may be entered therein at the speed of operation of electronic elements and read out therefrom in a similar way. Signals for controlling entries and transmissions from the eight electronic storage units are provided by eight associated pilot units which are composed of electronic circuits. The pilot units and other parts of the machine are sequenced by a main commutator. Associated with the main commutator is a control frame for producing delayed control signals and performing other operations in a sequence determined by signals from the main commutator. Also associated with the main commutator are calculation control commutators. These are the ACC.C commutator controlling the accumulator, the MYC commutator controlling the MD unit to carry out a multiplication, the DVC commutator controlling the MD unit to perform a dividing operation, and the NO commutator which is used in skipping operations when no calculation is called for in a sequence run.

Each number entering into a calculation is accompanied by a sign and when the number is applied to a calculator unit an operational sign is also applied to the unit. The operational sign determines whether the number sign is to remain the same for the calculation or is to be inverted to the opposite sign or is to be ignored and the number treated as an absolute positive or negative quantity. The operational sign is sent to the calculator section from an operational sign commutator sequenced by the main commutator.

Memory units include 150 relay storage units which have relay input and output gates through which data may be sent into or out of the relay storage units. There are dial storage units which may be manually set and which may send out data when relay output gates are closed. Pluggable storage units also may read out numbers to the selected Out bus-sets when related relay output gates are closed. Memory also includes three banks of record stations each bank having ten stations which may individually carry record tapes on which data are represented to be read out through selected relay gates. The record or tape storage banks also may receive punched tapes from punch units which will not be discussed further in this application. Memory also includes record or tape sections in a table look-up unit which is per se the subject of application Serial No. 768,600, of F. E. Hamilton et al., filed August 14, 1947. Computed arguments may be entered through selected relay gates into the table look-up unit and selected functional values read out of this unit, also through relay gates.

Numbers may be recorded by punching or printing. In the present application only one of the printer units will be described. Numbers which are to be printed are first sent to assigned relay storage units from which they are applied to the printing unit during a print cycle.

The interplay of the various units of the machine is controlled by program means. The pro-

gram means includes two identical units, called the A and B sides, of sequence storage. Program data are alternately entered into the A and B sides of sequence storage and these sides alternately coact with the sequencing network, which includes the main commutator, control frame, calculation control commutators NO, ACC, MYC, and DVC, the pilot units and the operational sign commutator. The sides of sequence storage also control the operation of the desired gates between memory units and the Out bus-sets and In bus-sets according to program data applied to the sequence storage sides. Program data may be derived from any of the memory units as selected by program instructions and may also be calculated. All program data except the First artificial line are routed through selected electronic storage units to sequence storage.

When a memory unit is ready to send forth data it applies a Forward signal to a pilot unit selected by a program instruction. When a memory unit or the printing unit is ready to receive data it sends a Back signal to a selected pilot unit. The blank code pilot unit comes into play when the program data does not select a pilot unit which is associated with an electronic storage unit.

The sequencing network performs successive runs of coaction with the sequence storage sides. In each run it sends signals to the pilot units to control its application of signals to the electronic storage units. Whenever the pilot unit enters data into an electronic storage unit it sends out a Move signal which may act on a selected tape storage station if the station is selected by the program to respond. The responsive station is one which has acted to read out data and it is conditioned to advance or not advance the record tape at the station upon receiving the Move signal. Whenever a memory unit is selected to receive data it receives a Reset signal from a selected pilot unit when the pilot unit is signalled by the sequencing network to send forth the signal. The main commutator and the related pilot units interchange signals which determine the progress of a sequence run. There is also an interchange of signals among the calculator units and the calculation control commutators and the main commutator.

By sequencing the multiplying and dividing unit MD and the accumulator through the four basic calculations of addition, subtraction, multiplication and division, the most complicated of mathematical problems may be solved. A sequence of the machine through one or more of these calculations performed in any order may be called a calculation path.

A main pulse generator is provided for applying pulses to the main commutator, the pilot units and other electronic circuits. This main pulse generator is shown in Fig. 18 and discussed in Section 4 and is per se the subject of application Serial No. 71,502 of P. E. Fox, filed January 18, 1949.

A control desk is provided with switches and dials which may be manipulated to simulate the automatic controls of the machine. Before starting operations, cancel circuits for desired units of the machine, including the main commutator, pilot units and other units, may be established under control of switches at the control desk.

The speed of the machine may be gauged from the fact that in the moon problem to compute the position of the moon at any given time—11,000 accumulations, 9000 multiplications, and 2000 references to the tables in the table look-up means were done in about 7 minutes.

Memory units, except pluggable storage, but including electronic storage units, have a capacity of 19 digits and a sign in each unit. The accumulating unit may add or subtract 19-digit numbers and produce a 28-digit result and its sign in less than $\frac{1}{1000}$ of a second. The MD unit may multiply two 14-digit numbers and produce a 28-digit product and sign in about $\frac{1}{50}$ of a second. Division of one 14-digit number by another may produce a 14-digit quotient in about $\frac{1}{30}$ of a second. Division may be carried out to as many as 28 quotient digits. Results to 28 digits may be read from the accumulating unit or the MD unit into the column shift unit and a maximum of 19 digits may be read out of the shift unit into electronic storage.

The multiplying and dividing unit is the subject of application Serial No. 71,641 of B. E. Phelps and G. E. Mitchell, filed January 19, 1949, now Patent No. 2,604,262.

Certain elements of the print unit are claimed in application Serial No. 70,575 of F. E. Hamilton, filed January 12, 1949.

Other objects of the invention will be pointed out in the following description and claims and illustrated in the accompanying drawings, which disclose, by way of example, the principle of the invention and the best mode, which has been contemplated, of applying that principle.

In the drawings:

Fig. 1 is a diagrammatic chart of the parts of the machine disclosed herein and shows in a general way the associations among these parts.

Fig. 2 is a fragment of a value tape used in tape storage and in the table look-up unit.

Fig. 3 is a fragment of a program tape bearing successive left-half lines of sequence data.

Fig. 4 is a fragment of a program tape bearing successive right-half lines of sequence data.

Fig. 4*a* shows the code used for designating numbers on the record tapes.

Fig. 5 is a partially sectioned side view of a tape station in a tape storage bank.

Fig. 6 is a rear elevational view of the tape station.

Fig. 7 is a section on line 7—7 of Fig. 5.

Fig. 8 shows the upper portion of Fig. 7 with parts in a different position.

Fig. 9 is a semi-diagrammatic chart of tape stations in a tape storage bank, showing the drive for these stations.

Fig. 10 shows a typical trigger circuit used herein.

Fig. 10*a* is a block symbol of the trigger circuit.

Fig. 11 shows a typical triode circuit switch used herein.

Fig. 11–12 is a block symbol of the triode circuit switch and also of the tetrode circuit switch.

Fig. 12 shows a typical tetrode circuit switch used herein.

Fig. 13 shows a typical pentode circuit switch employed herein.

Fig. 13*a* is a block symbol of the pentode circuit switch.

Fig. 14 shows a typical circuit of the so-called lock couple, constituting another form of electronic switch.

Fig. 14*a* is a block symbol of the lock couple.

Fig. 15 is a partially diagrammatic view of a register order.

Fig. 15*a* is a block diagram used herein to represent the register order.

Fig. 16 shows a typical cancel circuit used for resetting trigger circuits.

Fig. 17 shows the block diagram of the cancel circuit and also shows connections of the cancel circuit output to triggers.

Fig. 18 is a diagrammatic circuit view of the main pulse generator system.

Fig. 19 is a timing chart relating to the main pulse generator.

Fig. 20 is a diagrammatic showing of the electronic calculating section.

Fig. 21 shows in block circuit form a column of electronic storage the two sets of entry and exit means associated therewith and also the pilot signals for controlling a column.

Fig. 22 shows several of the electronic storage units and their associations with the In and Outs bus-sets with the Internal bus-sets and also the pilot signals for controlling the units.

Fig. 23 is a diagrammatic circuit representation of a dial storage set.

Fig. 24 is a block circuit view of a column of the denominational shift unit.

Fig. 25 is a diagrammatic representation of the denominational shift unit.

Fig. 26 is a timing chart of operations concerned with a denominational shift.

Figs. 27*a*, 27*b*, and 27*c* represent the circuit of the internal commutator or sub-sequencing means of the denominational shift unit.

Fig. 28 is a diagrammatic view of relay storage sets or groups, each with fifteen relay storage units.

Fig. 29 is a circuit showing of parts of a relay storage unit and their connections to the In and Out bus-sets.

Fig. 30 represents a plugboard for a relay storage group.

Fig. 31 is a diagrammatic representation of a tape storage bank and its associated station selectors, plugging, and Group Outs.

Figs. 32*a*, 32*b*, and 32*c* represent the circuits relating to a tape storage bank.

Fig. 33 is a timing diagram of timers 1 and 2 of Fig. 32*b*.

Fig. 34 represents the plugboard associated with a tape storage bank.

Fig. 35 is a diagrammatic circuit showing of elements of the table look-up unit.

Fig. 35*a* is a flow chart of the table look-up unit.

Fig. 35*b* shows the circuits for controlling the production of Forward and Back signals of the table look-up unit.

Fig. 36 is a circuit showing of elements of sequence storage and their heating relays.

Fig. 37 shows the circuits of intermediate relays of sequence storage.

Fig. 38 is a block view of the intermediate relays for storing sequence instructions given by the left half of a line of sequence.

Fig. 39 is a similar view of the intermediate relays controlled by the sensing of instructions given in the right half of a line of sequence.

Fig. 40 diagrammatically shows dial switches for setting up an artificial line of sequence (see Section 16*b*).

Fig. 40*a* shows the circuit control relays for bringing the circuit of Fig. 40 into operation.

Fig. 41 shows the circuit of a few of the operational relays in sequence storage.

Fig. 42 is a block diagram of the operational relays for storing the left half of a line of sequence.

Fig. 43 is a similar view relating to the right half of a line of sequence.

Fig. 44 shows the internal circuit of a "zero-filter."

Fig. 45 is a circuit showing of a code translating circuit called a tree.

Fig. 45*a* is a block symbol of a tree.

Fig. 46 is a circuit showing of a so-called OP2 tree.

Fig. 46*a* is a block diagram of the OP2 tree.

Fig. 47*a* is a diagrammatic representation of a pyramid of trees in sequence storage for picking up relay storage Group Outs.

Fig. 47*b* shows sequence storage pyramids for table look-up Group Outs and for tape storage Group Outs.

Fig. 47*c* shows sequence storage pyramids for station move relays and for dial storage Group Outs, and Table Outs.

Fig. 47*d* shows sequence storage pyramids for station selector relays ASS and BSS of tape storage.

Fig. 48 is a diagrammatic representation, partially in circuit form, of sequence storage pyramids for picking up relay storage Unit Outs.

Fig. 49*a* shows elements of the relay storage Group Out pyramids relating to the five possible Out fields of a line of sequence.

Fig. 49*b* shows the pyramids for controlling tape storage Group Outs from all possible Out fields.

Fig. 50 represents the pyramids operated in sequence storage in accordance with the code number in the S1 or S2 field of a line of sequence.

Fig. 51 represents sequence storage pyramids for operating relay storage Group Ins and table look-up Group Ins.

Fig. 52*a* represents sequence storage pyramids for operating relay storage unit Ins 010 to 099, and also for operating table look-up relays TL1 to 6.

Fig. 52*b* shows sequence storage pyramids for operating relay storage unit Ins 100 to 159, and also shows a circuit controlled by sequence storage and pilot units for applying a start signal to the printer unit (Sections 22 and 22*a*).

Figs. 53*a*, 53*b*, and 53*c* represent the plugboards associated with sequence storage.

Figs. 54 to 58 show the sequence storage pyramids for the pilot units selection.

Fig. 59 shows the sequence storage pyramids relating to the OP1 and OP2 fields.

Fig. 60 shows the sequence storage circuit for the operational sign.

Fig. 61 shows the sequence storage circuit for the In Code control.

Fig. 62 shows the sequence storage circuits for the SH1 and SH2 denominational shift selection.

Fig. 63 shows the sequence storage circuits for the Q, R, U, and V shift selection.

Figs. 64*a* to 64*j* represent the circuits of the multiplying and dividing unit MD.

Figs. 65*a* to 65*k* represent control circuits of the multiplying and dividing unit.

Fig. 66 is a timing chart, showing the primary cycle of the multiplying and dividing unit.

Fig. 66A is a chart of the relationship of the Internal buses to the multiplicand and divisor register orders and to the dividend receiving orders of the result register orders; the chart also indicates the relationship, in different column shift positions, between the two registers.

Fig. 67 is a timing chart relating to controlling

and controlled operations of the multiplying and dividing unit.

Fig. 68 illustrates by an example the principle of dividing used herein.

Figs. 69*a* and 69*b* represent the circuits of the first and second orders of the accumulator unit.

Fig. 70 is a block diagram of the registers in the accumulator unit.

Figs. 71*a* to 71*g* represent the circuits of the internal commutator or the sub-sequencing means of the accumulator unit.

Fig. 72 is a timing chart, showing the accumulator cycle.

Fig. 73 is a timing chart, showing the various signal times relating to the accumulating operation when the result is positive (upper part of the figure) and also when the result is negative (lower part of the figure).

Fig. 74 is a timing chart indicating the half correction sequence in the accumulator operation.

Figs. 75*a* to 75*h* represent the circuits of one portion of the Control Frame, this portion mainly involving various delay circuits and also heating control circuits for sequence storage.

Figs. 76*a* to 76*g* represent the circuits of another portion of the Control Frame, this portion mainly involving heating control circuits for the pilot units selection pyramids shown in Figs. 54 to 58.

Figs. 77*a* and 77*d* represent circuits of a third portion of the Control Frame, this portion mainly involving Start, Stop, Drain circuits, also various circuits for controlling calculation control commutators, and also amplifier and inverter circuits for sequence storage control relays.

Figs. 77*aa* shows parts of some circuits operated at the control desk.

Figs. 78*a* to 78*k* represent the circuits of the main commutator.

Fig. 78L, in the BC portion, represents the circuits of the blank code pilot unit, and, in the OPSN section, represents the circuits of the operational sign routing elements.

Fig. 78*A* represents the circuit of the accumulating calculation control commutator.

Fig. 78D represents the circuits of the dividing calculation control commutator.

Fig. 78M represents the circuits of the multiplying calculation control commutator.

Figs. 79*a* to 79*d* and 79*bb* constitute a flow diagram of operations described in Section 16*b*.

Figs. 80*a* to 80*e* represent the circuits of a pilot unit.

Figs. 81*a* and 81*b* show, in block form, pilot units 1 and 8 of the group of eight pilot units.

Fig. 82 is a vertical, sectional view through the printing unit.

Fig. 83 shows the drive and clutch means for the main shaft of the printing unit.

Fig. 84 shows three different positions of the carry-zero levers of the hammer latches in the printer unit.

Fig. 85 is a perspective view of a pair of hammer latches and of associated carry-zero levers.

Fig. 86 is a timing chart for the printer unit.

Fig. 87*a* represents the circuit of the printer unit.

Fig. 87*b* represents readout circuits for reading out a number from a relay storage unit into the printing unit.

Fig. 88 shows the sequence storage pyramid for pluggable storage selection relays.

Fig. 89 represents typical circuits and the plugboard which constitute pluggable storage.

Fig. 90 is a plugging diagram relating to Case 1 discussed in Section 24.

Fig. 90*a* is an additional plugging diagram relating to an alternate step in Case 1.

Figs. 91 and 92 show plugging used for Case 4 discussed in Section 24.

Fig. 93 shows plugging for Case 5 discussed in Section 24.

Fig. 94 shows plugging for Case 6 discussed in Section 24.

2. *The record tapes*

The machine uses a large number of record tapes which may be used to store values either for computational purposes (see Fig. 2) or for program or sequence control purposes (see Figs. 3 and 4). Sequence data is made up of numbers which can be handled the same as numbers involved in a calculation. Those tapes which store values for computation may be called value tapes to differentiate them from program tapes which bear programming or sequencing data. The program tapes are the main sources of sequence or program information according to which the machine is controlled to perform the desired operations in the desired sequences.

As many as thirty-six tapes may be installed at tape stations in the table look-up section (see Fig. 35) which is the subject matter of application Ser. No. 768,600, of F. E. Hamilton et al., filed August 13, 1947. Thirty tapes may be installed in the tape storage section which comprises three similar banks 1, 2, and 3 of ten tape stations each (see Figs. 1, 9, and 31). Whether a tape is used for storing numbers to enter into a computation or to represent sequence data, the numbers are punched according to the same code, preferably the binary term code (see Fig. 4*a*) in which a complete binary zone is made up of four successive binary positions 8, 4, 2, and 1. Since the coded representation of a decimal notation digit is contained in such zone, it is convenient to refer to the zones as columns. One or more number signs may also be represented along a designation line. A half-zone or half-column containing binary positions 2 and 1 is sufficient for a sign representation. The designation 1 in a half-column represents — and the designation 2 represents +. Also, with respect to a sign field in a program tape, 0 (no perforations) in the sign field and 8 (the 2 and 1 perforations) represent other sign functions which will be explained in the next section.

The record tape has the width of a standard 80 index position card but owing to the space occupied by the marginal feed holes, only 78 index positions are allowed for. In other words, the tape has a capacity of nineteen-and-a-half digit columns or sufficient capacity to be punched, if desired, with representations of nineteen decimal notation digits and a sign. This, if desired, may be designated as a "word." Obviously, the arrangement of numbers and signs within a designation line may vary according to requirements.

Each record tape is preferably joined at the ends to form a continuous loop. The tape is interchangeably positionable at any of the tape stations which will be described in Section 2*b*.

2*a*. *The program tapes*

Programming or sequencing of machine operations is controlled generally by the program tapes, illustrative portions of which appear in Figs. 3 and 4. Successive designation lines of the pro-

gram tapes bear sequence data which may be referred to as an Instruction "word" or as Seq data. A complete line of Seq data is made up of two designation lines respectively of a pair of program tapes. One half of the line of Seq data or one "word" is a designation line of one tape and the other half is a designation line on another of the tapes. The halves of Seq data may be differentiated as the S1Seq and S2Seq portions. A program tape will be punched either with S1Seq data or S2Seq data. Both portions S1Seq and S2Seq are similar with respect to the arrangement of fields and subfields but have certain differences with regard to programming functions. The S1Seq portion is made up of fields P, Q, R, SH1, OP1 and S1. The S2Seq portion is made up of fields T, U, V, SH2, OP2, and S2. The fields Q, R, T and U may be used either as In or Out fields. Field P is always an Out field and field V always an In field. An Out field is one which calls for the reading out of data from a selected source into a selected electronic storage unit (see Section 6) by way of the Out bus-set fixedly associated with the electronic storage unit. An In field is one which calls for transmission of data from a selected electronic storage unit and along the corresponding In bus-set to a selected receiving means. Each of the fields P, Q, R, T, U and V is divided into three subfields generally designated *s*, *b*, and *r*. The P*s* subfield comprises column 1 which is actually a half-column with binary positions 1 and 2, and is used to designate the operational sign which is to be applied to a number read out from a selected source. The P*b* subfield is the single column 2 which may be punched with the binary terms representing 1, 2, 3, 4 . . . 7 or 8, designating the electronic storage unit and corresponding Out bus-set involved. The P*r* subfield is made up of the three columns 3, 4 and 5, bearing the hundreds, tens and units digits of the code number for the source from which a value is to be transmitted to the electronic storage unit named in subfield P*b*.

Further considering field P*s*, a perforation in binary position 2 represents the operational + sign. This means that the number taken from the source named in P*r* is to be handled in a calculation without any change in its sign. A perforation in binary position 1 of P*s* represents the operational — sign and this calls for the number to be operated upon with an inversion in its sign. The absence of a perforation in P*s* represents 0 which is the designation in this field for the operational fixed + sign. This means that regardless of the original sign of the number, it is to be treated as a positive number. Digit 3 in P*s*, represented by perforations in binary positions 2 and 1 of P*s*, is the operational fixed — sign which calls for treating the number as —, regardless of its original sign.

When a subfield *b* in a program field P, Q, R, T, U or V is blank, it represents 0 and calls for the field to be, in effect, skipped over during a scanning sequence of the program line. When the subfield *r* in an Out field is blank, it calls for transmission from the electronic storage unit named in its *b* subfield to an electronic storage unit named in the *b* subfield of an In field which, in such event, will also be blank in its *r* subfield.

The Q field is subdivided into subfields Q*s*, Q*b* and Q*r*. Field Q may be either an In or an Out field. Subfield Q*s* is a complete binary zone, in column 6, in which the 0, 1, 2 and 3 designations have the same operational sign significance as the subfield P*s*. Additionally, any of these designations in Q*s* characterize field Q as an Out field. Any digit in Q*s* higher than 3 characterizes the Q field as an In field. Besides characterizing the Q field as an In field, digits 4 to 9 variously designate the tens denomination digit representing of a column shift amount and whether a shift is to be executed to the left or to the right by the Denominational Shift Unit (Section 12). Digit 4 in Q*s* thus designates the Q field as an In field and also calls for a shift to the right with a zero tens order shift. Digit 5 in Q*s* calls for a shift to the left with a zero tens order shift. Digit 6 calls for a shift to the right with a tens order shift of 1. Digit 7 calls for a shift to the left with a tens order shift of 1. Digit 8 calls for a shift to the right with a tens order shift of 2. Digit 9 calls for a shift to the left with a tens order shift of 2. The units order shift amount is given by program field SH1.

Subfield Q*b* is a single binary zone, in column 7, and is used to designate the electronic storage unit to send out or receive a number, depending on whether field Q is an In or an Out field, respectively.

Subfield Q*r* is located in columns 8, 9, and 10 to represent the source from which a number is to be sent to the electronic storage unit if the field Q is an Out field or to represent the receiving unit to which a number is to be transmitted from the electronic storage unit if the field Q is an In field.

Field R is contained in columns 11 to 15, and its subfields are similar to field Q and its subfields.

Field SH1 is in column 16, and, as already stated, designates the units order amount of column shift to be executed by the Denominational Shift Unit (Figs. 24 to 27*c*).

Field OP1 is a two-column field, columns 17 and 18 which designate the fundamental calculating operations to be performed. The fundamental operations to be considered in this case are accumulation, division, and multiplication.

The field S1 is a 2-column field, columns 19 and 20, which designates the source for the next left half line of sequence data.

The right half line of programming S2Seq is similar to the left half line S1Seq and the fields and subfields of the two half lines generally correspond to each other.

As mentioned before, V is always an In field while P is always an Out field.

The field T may be either an In or an Out field depending on the code in the field OP2. When the latter field has the designation 01 it characterizes field T as an In field. In all other cases, the field T is an Out field.

2*b*. *The tape stations*

Fig. 9 indicates the arrangement of tape stations of a tape storage bank. Either a value tape or program tape may be installed at a station. Figs. 5, 6, 7 and 8 provide a detailed illustration of a tape station all of which are of like construction. Drum 11 at each station has marginal feed pins 11*p* to mesh with the feed apertures of a tape for feeding it upon rotation of the drum. The drums 11 at the plurality of stations are individually clutchable to continuously rotating drive means which may be driven by an electric motor MRT. Shaft 16 represents a continuously turning shaft of the drive mechanism. Fixed on shaft 16 are bevel gears 18, one

for each station. Referring now to Fig. 5, each bevel gear 18 meshes with a bevel gear 19 to turn a shaft 20 which is journalled in a sub-frame. Fixed on shaft 20 is a ratchet wheel 23 (also see Fig. 6) which is the drive element of a station clutch. The driven portion of this clutch includes a sleeve 24 rotatably mounted upon the shaft 20. Sleeve 24 is formed with a gear 25 meshed with a gear 26 on the shaft 27 of the station drum 11. Fixed on sleeve 24 is a toothed disk 28. Positioned between disk 28 and ratchet wheel 23 and freely mounted on sleeve 24 is a toothed disk 29. Disks 28 and 29 are of the same diameter and respectively provided with the same number of teeth 28*a* and 29*a*. Projecting from disk 28 and passing with appreciable play through an elongated slot 29*b* in disk 29 is the pivot stud 30*a* of a clutch dog 30. The clutch dog 30 lies in front of the disk 29 and has a tooth 30*b* to engage the driving ratchet 23. The tail 30*c* of the clutch dog is rounded at the free end which is seated in a round notch cut in a front rib 29*c* of the disk 29. A spring 31 connects the clutch dog with a stud 29*d* projecting from disk 29. Another spring 32 is anchored at opposite ends to studs 29*e* and 28*d* of disks 29 and 28 respectively. Springs 31 and 32 urge the disk 29 to turn clockwise relative to disk 28, such relative movement, when permitted, being limited by the play of the hub of the clutch dog in notch 29*b* of the disk 29. The clockwise movement of disk 29 relative to disk 28 is prevented in the declutched positions of the parts (Fig. 6) by a latch 33 engaged with alined teeth of the disks. Latch 33 carries the armature of the station clutch magnet SCM and is urged to latching position by a spring 34. A rebound pawl 35 pivoted on a stud 36 is urged clockwise by a spring 37 against a stop 38 and is constantly maintained effective to prevent reverse movement of the disks 28 and 29.

To effect clutch engagement, magnet SCM is energized, withdrawing latch 33 from disks 28 and 29. Springs 31 and 32 now act to turn disk 29 clockwise relative to disk 28 and by reason of the pivotal engagement between the disk 29 and the tail 30*a* of the clutch dog and under the further direct pull of the spring 31, the dog is rocked into engagement with ratchet 23. Clockwise rotation of the ratchet now is transmitted to disk 28 and through springs 31 and 32 to the disk 29. Sleeve 24 rotates clockwise with disk 28 and through gears 25 and 26 rotates the tape-feeding drum 11 counterclockwise. It should be noted that in the final increment of movement of latch 33 away from disks 28 and 29, it encounters a lever 39 pivoted on stud 36 and urged by a spring 40 against a stop 41. Spring-urged lever 39 assists spring 34 in overcoming the residual attraction of magnet SCM when its circuit subsequently is broken, thus speeding return of latch 33 to clutch disengaging position. During rotation of the disks 28 and 29, their teeth 28*a* and 29*a* are out of alinement, disk 29 having moved clockwise to a limited extent relative to disk 28 upon release of the disks by the latch 33. Deenergization of magnet SCM to effect clutch disengagement is timed to occur just before a tooth of disk 29 reaches the latch position. Thus, latch 33 will first encounter a tooth of disk 29 and arrest it while disk 28 continues to turn until a tooth thereof meets latch 33. While the disk 28 is moving clockwise relative to the arrested disk 29, the clutch dog 30 gradually withdraws from ratchet 23 and is free of the ratchet by the time the disk 28 is latched.

The drum 11 is built up of several parts, including end rings 11*a* which carry the feed pins 11*p*. Between the end rings is a contact cylinder 11*b*. Insulating disks 11*c* space the cylinder from the end rings. The parts 11*a*, 11*b* and 11*c* are clamped tightly together by bolts 45.

A transverse row of 18 sensing brushes RB, one for each index position of a designation line (see Fig. 4*a*) coact with the contact cylinder in the sensing of one designation line of the tape at a time (columns 1 to 20). A common brush CB (Fig. 7) constantly wipes the contact cylinder. The contact cylinder and common brush together may be referred to as the brush common. It may be mentioned that when a station clutch is disengaged, the drum 11 is arrested with a designation line of the tape centered under the brushes RB. The portion of the record tape adjacent to and under the sensing brushes is held taut by pressure fingers 48. The pressure fingers and the sensing brushes RB are commonly adjustable at will from their active positions (Fig. 7) to their inactive positions (Fig. 8) remote from the drum when it is desired to remove or apply a record tape at the tape station. The adjusting means comprises an eccentric shaft 50 with end pintles 50*a* rotatably bearing in the sub-frame 22. Two parallel links 52 are each pivotally supported at one end by the eccentric portion of shaft 50 and have pin and slot connection 52*a* at the opposite ends with the subframe. The arms 52 rigidly carry between them a block 54 of insulating material which mounts the row of brushes RB. One of the pintles 50*a* carries a crank handle 56. Fixed to the other pintle are a ratchet wheel 57 and a disk 58 with diametrically opposite V notches. Detents 59 and 60 are pivoted to the subframe and urged by springs 62 into engagement, respectively, with the ratchet wheel 57 and the notched disk 58. Coaction of detent 59 with the ratchet wheel restricts the shaft 50 to rotative adjustment in one direction. The detent 60 is seated in one of the V notches of disk 58 when the parts are in the positions shown in Figs. 5, 6 and 7. When shaft 50 is given half a turn by handle 56, it lifts the links 52, adjusting the brushes RB to elevated positions remote from the drum, as shown in Fig. 8. The detent 60 springs into the other of the V notches in disk 58 when the half turn of the crank shaft is completed. Detent 60 thus coacts with disk 58 to releasably latch the crank shaft and the parts operated thereby either in the positions shown in Fig. 7 or the positions shown in Fig. 8. To return the parts from inactive positions to active positions, the shaft 50 is turned through the second half of its revolution, at the completion of which the detent 59 springs into a V notch of disk 58 to position the brushes accurately on the drum.

The pressure fingers 48 are clamped on a pair of shafts 63 turnable in the subframe. Each of shafts 63 fixedly carries at its right hand end (Fig. 5) an arm 64 to which springs 65 (Fig. 6) are connected. The free ends of the arms 64 rest against the peripheries of a pair of cams 66 fixed, in front of notched disk 58, to the right-hand one of the pintles 50*a* of the shaft 50. With the shaft 50 in the position shown in Figs. 6 and 7, the cams 66 allow the arms 64 to be close to each other and the pressure fingers 48 to press against the record tape on the drum 11. When the crank shaft is given half a turn to the posi-

tion shown in Fig. 8, the cams 66 rock the arms 64 apart, displacing the pressure fingers to positions away from the drum. Thus, the pressure fingers and the sensing brushes are commonly adjustable from the positions shown in Fig. 7 to the positions shown in Fig. 8, and vice versa. It may be noted that the pressure exerted by arms 64, under the influence of springs 65, against the cams 66 helps to prevent unintentional movement of the adjusting means for the sensing brushes and the pressure fingers. Also, the pressure fingers not only serve to keep the record tape taut under the sensing brushes but they exert a braking effect on rotation of the drum 11 and its drive gearing. This braking effect is desirable to prevent overrunning of the drum with respect to the drive means, particularly at the time the station clutch is being engaged.

A station is provided with at least a move key switch SMK which is closed whenever the tape at the station is to be moved under manual control to a desired line position. The clutch circuits will be explained later in Section 9. At present it is sufficient to state that a tape bearing sequence or value data will be advanced only a single step at a time. The means for controlling the single step advance of a tape station includes an individual commutator for each tape station. Such commutator comprises a disk 44 fixed to the drum shaft 27 (Figs. 5 and 9) and wiped by brushes 44*b*. For each line space movement of a drum, this station commutator makes and breaks once. The timing means for a single step advance also includes in each tape storage group a pair of commutators common to all the stations in the group and called timers No. 1 and No. 2. These timers include commutator disks 42 wiped by brushes 43. One of the disks 42 is fixed to shaft 16 and the other fixed to a shaft 16*a* geared 1:1 to shaft 16. Commutator timers Nos. 1 and 2 will time station clutch magnet energization to insure only a single line spacing step of the tape and also provide a favorable time for clutch engagement so as to avoid injury to the ratchet and clutch teeth. The deenergization of the clutch magnet will be timed to occur just after a tooth of the disk 28 has passed and just before a tooth of the disk 29 is about to pass the latching position.

3. *General circuit data*

A source of supply (not shown) is provided for the voltage lines running through the various circuits. This source supplies voltages shown in the various figures. The line —100C is a cancel bias line, the purpose of which will be explained in the subsequent descriptions of the trigger and the cancel circuit. The triodes used in the circuits are of the 6SN7 type and may be the halves of twin tubes 12SN7. The tetrodes which are used mainly as power amplifiers are of the 25L6 type. The pentodes are generally of the 6SK7 type. In some instances 6SJ7 tubes are also used. Resistance values shown are in megohms and capacitance values in micro-microfarads, unless otherwise indicated.

Referring to Fig. 11, the cathode terminal *k* of the triode is connected to ground or 0 v. line. The anode terminal *an* is connected through a resistor to the +150 v. line. The value of the resistor for an individually operated triode is generally .02 meg. Operation of the triode is generally effected by applying a pulse from the output of another tube to an input terminal *gi*. This input terminal leads to a voltage divider which is tapped by a connection to the grid of the triode. The voltage divider terminates at the —100 v. line. The part of the voltage divider between the grid and the —100 v. line generally has a resistance value of .47 meg. and the other part of the voltage divider, in that event, has a resistance value of .51 meg. In some instances where it is desired to reduce the time constant or to provide for a smaller grid leak impedance, the resistance values of the upper and lower portions (as shown) of the voltage divider are .24 and .22. The input potential to the voltage divider generally has a swing from about 50 v. to 150 v. although in extreme instances the input voltage may descend to about 15 v. It may be seen from Fig. 11 that the triode is normally biased to cut-off when the input potential to the voltage divider is at its lower value. When the input voltage rises to its upper value, then the grid potential is driven above cut-off and the tube conducts. Where it is required to increase the rapidity of response of the triode to an input pulse, the upper portion of the voltage divider is shunted by a capacitor which is generally 50 mmf. The anode resistor may be tapped at a suitable point *anr* for connection to an element to be operated by the output of the triode. It is understood that constants given are illustrative and other appropriate constants may be used.

Fig. 12 indicates appropriate values for the tetrodes. The screen grid of the tetrode is generally connected by a .005 meg. resistor to the +70 v. line. Operation of the tetrode is effected in the same general manner as the triode.

Fig. 11–12 shows the block diagram representing either the triode or the tetrode. The cathode terminal *k* in the block diagram will be omitted except where it is necessary to an understanding of the operation of the tube. It is to be understood that the tetrodes will be used wherever power amplification is a prime requisite.

Fig. 13 shows the connections for a pentode. The screen grid is generally connected directly to the +70 v. line. Suitable values for the anode resistor and the voltage dividers connected to the control grid and the suppressor are indicated. The operation of the control grid is effected similarly to the operation of the control grid of the triode and the input terminal for the voltage divider tapped by the control grid is also marked *gi*. The input terminal *si* is connected through a resistor generally having a value of .33 meg. to the suppressor grid and the suppressor grid is connected through a resistor of .68 meg. to the —250 v. line. The input potential to the terminal *si* also varies from about 50 v. to 150 v., in general, although as previously indicated in connection with the input potential to the terminal *gi*, the input potential may drop to as low as 15 v. It is clearly seen from Fig. 13 that when the input potential on either terminal *si* or *gi* is at its low value, the pentode is cut off. The input potentials to both terminals *si* and *gi* must be at their upper levels in order to render the pentode conductive. Fig. 13*a* shows the block diagram representing the pentode.

The output potentials at the terminals *an* of the triode and the pentode may be taken as having a lower value of approximately 40 to 50 v. when the tube is conductive. However, it is quite possible for the potential at the anode of a pentode to drop to as low as 15 v. The anode resistor will be tapped at a point such as to provide the necessary working potential for an element to be controlled by the tube. It

may be stated that where the output of the tube is to be applied to both input terminals *a* and *h* of a trigger (see Fig. 10), then the tap point *anr* is generally the midpoint of the anode resistor. Where the output potential of a tube is to be applied to only one of the terminals *a* and *h*, the point *anr* is generally connected through a .0075 meg. resistor to the +150 v. line and connected through a .002 resistor to the anode of the tube. Fig. 14 shows the 12SN7 tube with both triode sections of the tube having their anodes connected to each other. The common anode resistor in such case generally has the value .051 meg. The inputs to the sections are separate so that each of the sections may be individually operated. This circuit may be referred to as a lock couple. Both of the tube sections must be cut off in order to allow the common anode line to attain its upper voltage level. If both tube sections are at cut-off and one of the sections is then made conductive, the common anode potential generally will drop to about 50 v. Fig. 14*a* shows the block symbol for the lock couple.

The block symbols will be employed in the circuit diagrams of the machine. It may be mentioned that the impulses to the input terminals of the tubes may be applied through coupling capacitors which are of varying capacities depending on the desired pulse shape to be transmitted by the capacitor to the input terminal.

Where it is necessary to clarification, arrows will be used to indicate whether signals are coming in or going out of a circuit.

Where a coupling capacitor is used to transmit a pulse to a grid of a tube, the coupling capacitor is not shunted by a resistor. For instance, if a pulse is to be applied to the grid of the triode shown in Fig. 11 through a coupling capacitor, the resistor shown in this figure as shunting the capacitor is omitted. In some instances a tube may be used as a cathode follower in which case suitable resistance will be provided between the cathode of the tube and a voltage supply line. A tube may be biased normally to cut-off or to conductive condition. Where it is necessary to clarification, the normally conductive tube will be identified by the small letter *x* placed below the symbol for the tube.

Elements in a block diagram circuit may be identified by a particular reference character along with a general reference legend for the circuit, which legend may be the figure number or a capital letter or letters. Where an element is thus identified in an item of the description, subsequent mention of elements of the same circuit will be made without reference to the general identifying legend unless mention of another circuit figure intervenes or unless it is necessary to clarification.

3*a*. *The trigger*

One of the fundamental elements of the circuits is a double-stability electronic trigger circuit which will be called simply a trigger. The general form of this trigger is shown in Fig. 10. Typical constants are indicated for the trigger but it is understood that other suitable constants may be used. This trigger is fully discussed in application Serial No. 569,902 of Palmer and Phelps, filed December 27, 1944. Briefly, it includes two retroactively coupled tubes 10 and 14. In one state of a trigger, tube 10 is conductive and its anode terminal *f* is at about 50 v., while tube 14 is non-conductive and its anode terminal *c* at about 150 v. In the opposite state of the trigger, tube 10 is non-conductive and point *f* is about 150 v. while tube 14 is conductive and point *c* at about 50 v. Upon reversal of the trigger from one state to the other state, there is a steep drop in potential or negative going impulse of about 100 v. at the anode terminal of the previously non-conductive tube and a simultaneous rise in potential or positive going impulse of about +100 v. at the anode terminal of the other tube. Also, a negative impulse of about 50 v. appears at the midpoint *d* of the anode resistor 14*r* when the trigger is reversed from the status in which tube 14 is non-conductive to the status in which this tube is conductive. Also, upon return to its previous status in which tube 10 again is conductive, a negative impulse of about 50 v. appears at the midpoint *e* of the anode resistor 10*r*. It is characteristic of this trigger that it reacts sensitively to a negative impulse of suitable amplitude but is insensitive to a similarly applied positive impulse of similar amplitude. In the present case, a negative impulse of about 40 v. applied to the trigger input terminal *a* or *h* is effective to reverse the trigger, but a similarly applied positive pulse of such amplitude is not effective to reverse the trigger. A negative impulse of about 50 v. applied concurrently to both *a* and *h* will be effective to reverse the trigger but a positive impulse of the same amplitude and similarly applied will be ineffective. Reversal of the trigger also may be effected by directly impressing adequate positive potential (about 150 v.) on the grid terminal of the non-conducting tube of the trigger. Where an impulse source is connected to only one of points *a* or *h*, the other point terminates at the +150 v. line, this adding stability to the trigger.

Reversal of the trigger also may be effected by an auxiliary circuit operable to draw current through anode resistor 10*r* or 14*r* so as to depress the potential at the terminal *c* or *f* to about 50 v. Such auxiliary circuit may take the form of an auxiliary tube. For instance, in Fig. 10, a triode 10A is indicated as having its anode connectible to terminal *f* of tube 10. If tube 10A is rendered conductive, then it will force the potential at terminal *f* down to about 50 v., reversing the trigger to the status in which tube 10 is conducting or blocking reversal of the trigger from this status.

In some instances the trigger may omit the coupling capacitors 13*a* and 13*b*, these capacitors being essential as a rule only if it is desired to trip the trigger by applying impulses simultaneously to the points *a* and *h*. The digit representing triggers in the electronic storage units (see Fig. 22) are instances of triggers which omit the coupling capacitors.

It will be noted that in Fig. 10, the grid resistor of tube 10 terminates at the cancel line —100C, normally at —100 v. potential, but in other instances, the cancel line will be connected to the grid resistor of tube 14. A positive cancel impulse will be applied at a desired time to the line —100C to increase its potential to approximately ground potential. This will reset the trigger to the state in which the tube connected to the cancel line, through the grid resistor, is conductive. The reset status of a trigger is denoted by the small letter *x* adjacent the side at which the tube is conducting in the reset status.

In some instances, the grid resistor terminal *gr* is connected to the —100 v. line through an auxiliary tube E. When this auxiliary tube is con-

ductive it simply acts as a low impedance connection between the grid resistor and the —100 v. line and allows the trigger to function in a normal manner. When the auxiliary tube E is rendered non-conductive, its anode potential and therefore the potential at the grid of the connected tube 14 rises above cut-off potential and causes the trigger to assume the status in which tube 14 is conductive. The auxiliary tube E may thus be used to reverse a trigger. The block symbol for the trigger is shown in Fig. 10*a*. The terminals shown in dotted lines will be omitted in most instances in order to simplify the drawings and will be shown only where they are utilized in controlling the trigger. The cancelled status of the trigger will be considered as its normal reset status and the trigger will be spoken of as being turned and returned or reversed and reset, it being understood that the reset or return is to its shown cancelled status.

3*b*. *The basic cancel circuit*

Fig. 16 shows the basic cancel circuit operable to cancel a group of triggers. A plurality of such circuits are provided for various groups of triggers in the machine. The basic cancel circuit includes a normally cut off tube 75, a voltage regulator tube 76, and one or a group of power tubes 77, depending on the power requirement. The output of 77 is connected to the cancel line —100C of a group of triggers. The constants of the cancel circuit are such that 77 is normally conductive to sustain line —100C at —100 v. The voltage of line —100C may fluctuate slightly according to changes in the states of the connected triggers. These fluctuations are counteracted through the action of the voltage regulator tube 76 and its circuit. For instance, if line —100C goes slightly more negative than —100 v., it causes the voltage regulator tube to become proportionately more conductive so as to increase the negative bias on 77. As the negative bias on 77 increases, its output voltage rises, increasing the voltage on line —100C to —100 v. When it is desired to cancel or reset the group of triggers, a positive cancel signal is applied to tube 75 to make it conduct and negatively bias 77 to non-conductive condition. The line —100C thereupon rises to substantially cathode potential, so that the connected triggers are reset to the states indicated by the *x* marks.

Fig. 17 shows the block diagram representing the basic cancel circuit and two methods employed by the cancel circuit to reset a trigger. According to one method, the cancel circuit output —100C is connected to the terminal *cc* of a trigger (also see Fig. 10). According to the other method, the line —100C is connected to the grid of an inverter tube I which serves, in the manner of tube 10A in Fig. 10, to force a trigger to its reset status when the tube becomes conductive. Thus, when a positive cancel signal is applied to the input of the cancel circuit, its output line rises in potential and renders tube I conductive to reset the trigger.

3*c*. *The relays*

The machine uses relays of the type disclosed in Patent No. 2,282,066 to Lake et al. These relays may either have 4, 6, or 12 armature contacts and may be referred to as 4, 6, or 12 position relays. Two coils wound in the same direction may be placed on the same core and operate the same armature contacts. Such relay may be termed a double coil relay or a duo-wound relay. One coil of such relay may be used as a pickup coil *p* to be initially energized. This coil *p*, when energized, may then close contacts for establishing the circuit of the companion coil which may be called the hold coil *h* (see, for instance, Fig. 29). In some cases, the two coils of the duo-wound relay may be independently energized (see relays RHR and LHR in Fig. 29). The duo-wound relay also may be used as a delay relay. In that case, the hold coil *h* will have its ends connected to each other through a resistor so as to form in effect a transformer coil. Upon energization of the pickup coil *p*, the induced flux in the hold coil will be of opposite direction to the flux in the pickup coil and will tend to delay the operation of the common armature contacts. Also, upon the deenergization of the pickup coil *p*, the flux induced in the coil *h* will tend to maintain the armature contacts operated. The relay produced by the hold coil in the operation of the armature contacts will depend upon the inductance of the coil and the resistance across its ends; the higher the resistance, the greater the delay. These delay relays may be used in connection with arc suppression, as will be described for circuits shown in Figs. 36 and 47*a* (Section 11). It is to be understood that a relay will handle a maximum of twelve single or double pole contacts. Accordingly, if a group of 84 contacts is provided, then at least seven relays are used for operating these contacts. For instance, associated with each relay storage unit (Fig. 29), is a Unit In containing 84 relay contacts. For simplicity of illustration, only a single dotted relay coil U "in" is shown as operating these 84 contacts, but it is to be understood that actually this relay showing represents seven relays in the same group. Usually, the relays of the group will be connected in parallel to be energized concurrently through a common circuit (see, for instance, Fig. 48). Such group of relays may be referred to, for convenience, as a plural relay or a gang relay.

4. *The main pulse generator*

Fig. 18 diagrammatically illustrates the main pulse generating system which generates pulses called the AP, BP, CP and EP pulses, the timing of which is shown in Fig. 19. The pulse generating system is fully disclosed and claimed in application Serial No. 71,502 of P. E. Fox, filed January 18, 1949.

A brief description of the essentials of the system follows: FRMV represents a free running multivibrator, preferably one with provisions for varying the frequency. The output of one side of the multivibrator is applied to the control grid of tube 2, Fig. 18. The output of the tube is connected to the control grids of tubes 7 and 8. The tapped output of 8 is connected to both sides of a trigger 6. For each negative pulse produced by the multivibrator, tube 2 produces a positive pulse which is inverted by 8 to a negative pulse for reversing the status of trigger 6. Point *c* of trigger 6 is connected to the control grid of the tube 5. Point *f* of trigger 6 is connected to the control grid of a tube 9. It is seen therefore that in one status of the trigger, it conditions tube 5 and in the other status of the trigger it conditions tube 9. Since trigger 6 is reversed in status for each negative pulse produced by the multivibrator, it may be stated that tube 5 is conditioned for one multivibrator cycle while tube 9 is conditioned for the next such cycle.

The output of tube 2 connects to the control

grid of a tube 7. Hence, for every positive pulse produced by the multivibrator FRMV, tube 2 produces a negative pulse which is inverted by 7 to a positive pulse. Each positive pulse produced by 7 acts through a differentiator circuit to cause a tube 11 to produce a sharply peaked negative pulse. The negative pulses produced by 11 are applied to a one-shot multivibrator SSMV to reverse its status. Upon such reversal, this one-shot multivibrator applies a positive pulse to the suppressors of tubes 5 and 9. Depending on whether 5 or 9 is conditioned, the output pulse from SSMV is effective to render one of these tubes conductive, to produce the pulse AP or BP. Since trigger 6 is alternated with each negative pulse produced by FRMV, it is understood that tubes 5 and 9 are conditioned alternatively, each of these tubes being conditioned for one pulse cycle of the multivibrator FRMV. It is clear then that tubes 5 and 9 will alternatively produce pulses. The width of each pulse is determined by the self-restoring time of the one-shot multivibrator SSMV.

It is to be noted that trigger 6 acts at each of points *c* and *f* to halve the frequency of the control pulses derived from the free running multivibrator FRMV. Further, the pulses at *c* are 180° out of phase with those at *f*. The single stability multivibrator SSMV is controlled by the pulses derived from FRMV to produce pulses in phase with the FRMV pulses but of a controlled width. The tube 5 serves as a coincidence mixer for the pulses from SSMV and *c* of trigger 6. The SSMV pulses applied to 5 determine the width of the output pulses of 5 and restrict the output pulses to coincide in phase with the FRMV pulses. The pulses from *c* of trigger 6 further restrict 5 to producing its output pulses at a frequency half that of the SSMV and FRMV pulses. Similarly, tube 9 mixes the pulses SSMV and the pulses from point *f* of trigger 6 to produce pulses BP of the same shape as the AP pulses produced by 5 but 180° out of phase with the AP pulses.

The AP and BP pulses from 5 and 9 are applied to amplifier circuits, shown diagrammatically, which produce + and — AP and BP pulses. These pulses will be directed to desired destinations where they may be amplified before utilization. The ultimately utilized pulses AP and BP are the negative pulses and hence the +AP and +BP pulses from the amplifier circuits will be inverted as well as amplified at their destinations before utilization.

Intermediate points of the amplifier circuits for the AP and BP pulses coming from 5 and 9 are tapped for +AP and —BP pulses. +AP pulses are mixed in tube 22 with pulses from points *f* of a trigger 23. The trigger 23 is alternated in status by the negative BP pulses derived from the BP pulse amplifier. Hence, point *f* of 23 produces pulses at half the frequency of the BP pulses. It is clear that each AP pulse applied to 22 restricts it to produce a pulse of the same width as the AP pulse and at the same time as an AP pulse, while the pulses from 23 restrict 22 to producing output pulses at half the frequency of the AP and BP pulses. The output pulses from 22 are applied to an amplifier circuit which is arranged to produce +CP pulses. This amplifier circuit is tapped at an intermediate point for +CP pulses which are mixed in tube 30 with pulses from trigger 31. Trigger 31 is reversed each time trigger 23 is turned from its cancelled status. Thus, point *f* of 31 produces pulses at half the frequency of the CP pulses. It is seen that the CP pulses control 30 to produce pulses of the same width as the CP pulses, while the pulses from *f* of 31 limit 30 to produce an output pulse once for every two CP pulses. The output pulses from 30 are applied to an amplifier circuit which produces +EP pulses.

It is clear from the foregoing description and Fig. 19 that all the pulses are of equal width, that each pulse CP is coincident with every second AP pulse and each pulse EP is coincident with every fourth AP pulse. The frequency of the AP and BP pulses will be generally adjusted to about 4 kc., which means that the CP pulses are at 2 kc. and the EP pulses are at 1 kc.

The proper starting sequence of pulses from the main pulse generator is an AP pulse, BP pulse, CP pulse, and EP pulse in the order named. To insure the proper starting sequence, triggers 6, 23, and 31 are first cancelled to shown state. In addition, it is necessary that the free running multivibrator FRMV start with a positive pulse. The reason for this is that with 6 in cancelled status it is conditioning 5. Trigger 6 therefore must remain in this status in order that the first pulse produced by SSMV under control of FRMV be effective upon 5 to produce the AP pulse. Means for attaining the proper starting and stopping condition of FRMV are diagrammatically shown in Fig. 18. To stop FRMV from producing effective pulses, a switch, stop G is closed so as to apply potential from the +150 v. line to the control grid terminal *b* of a trigger MVT, thereby establishing the trigger in shown state. In this state the trigger acts through a tube 80 to make a tube 10 conductive, thereby depressing the pulse output terminal of FRMV to a low and ineffective potential. To start the pulse generating system the operator may close a switch, run G to apply the potential from the +150 v. line to the grid terminal *g* of the trigger MVT, thus reversing the trigger. In the reversed state of the trigger it causes tube 80 to cut off tube 10, thus allowing the pulse output terminal of FRMV to rise in potential to an effective level. Hence the first pulse produced by FRMV will be a positive pulse. By starting with production of a positive pulse and by starting with triggers 6, 23 and 31 in shown state, the pulse generating system is restricted to producing a starting sequence of pulses AP, BP, CP and EP in the order named.

5. *The register order*

Fig. 15 shows the register order used here in the computing units. This register order is similar to the one disclosed in Fig. 3 of application Serial No. 654,175 of B. E. Phelps, filed March 13, 1946. Fig. 15*a* shows the block diagram for the register order. Each order has four trigger stages designated 1, 2, 4 and 8 and a triode designated BX. The digit standing in an order is given by the sum of the reference numbers of the reversed stages.

Briefly, the order is in 0 status when all the triggers are in cancelled status. Operation of the register order may be effected by applying negative entry pulses to terminals *a* and *h* of the first stage 1. Assuming the order is initially at 0, a first entry pulse reverses stage 1. The second entry pulse returns stage 1 and upon its return, stage 1 applies a negative pulse from terminal *e* to the terminals *a* and *h* of stage 2 to reverse the latter stage. A third entry pulse again reverses stage 1. A fourth entry pulse returns stage 1, causing it to return stage 2. Thereupon, stage 2 reverses stage 4. The fifth and sixth entry pulses effect a third cycle of stage 1 and a second re-

versal of stage 2. The seventh and eighth pulses effect a fourth cycle of stage 1 and a return of stage 2. Stage 2 thereupon returns stage 4 and the latter stage upon returning reverses stage 8. The order then stands at 8. With stage 8 reversed, its anode terminal *f* is at high potential which is applied through resistance means to the grid of triode BX causing the triode to become conductive. With the triode conductive, it is effective to block stage 2 against reversal. A ninth entry pulse turns stage 1 and the order stands at 9 (stages 1 and 8 reversed). A tenth entry pulse returns stage 1 which thereupon returns stage 8 so that the order has been returned to its initial 0 status. The return of stage 1 by the tenth pulse is ineffective to reverse stage 2 because the latter is now blocked against reversal by the conductive tube BX. The return of stage 8 is effective to restore the tube BX to its non-conductive status after a momentary delay determined by the capacitor 47.

The value cycle of the register order through ten steps from 0 back to 0 has been described. Manifestly, the value cycle may start with the register order in any other value position and at the end of the value cycle the register order will be back in the same position. The number of pulses required to effect the 9 to 0 step of the order is the tens complement of the starting digit. For instance, if digit 6 is the starting digit, then four entry pulses will step it from 9 to 0. This step is manifested by the return of the last stage 8 of the order to its reset status. As the stage 8 returns, a positive carry out pulse appears at its terminal *c*.

6. *Electronic storage*

Electronic storage is part of the electronic calculating section (see Fig. 20) and may be considered as temporary number storage. There are eight similar electronic storage units designated ES1, ES2, ES3 . . . ES7 and ES8 (also see Figs. 1 and 22). Each unit has twenty columns of digit storage capacity, each column consisting of the four binary positions, as now understood. Fig. 21 shows a typical electronic storage column. Triggers 8, 4, 2 and 1 are the digit storage elements per se of the column. Entry into electronic storage may be made from the Internal In bus-set or alternatively from the correspondingly numbered Out bus-sets. Readout or exit from the electronic storage units may be into the Internal Out bus-set or alternatively into the correspondingly numbered In bus-sets.

There are eight pilot units (see Fig. 1) hereinafter designated PIL1, 2, 3 . . . 7 and 8. In a manner described later, each pilot unit provides five control and timing signals for the correspondingly numbered electronic storage unit. These signals are (Fig. 21): Cancel signal ESC, two alternative entry signals Int to ES and Out to ES and two alternative exit signals ES to Int and ES to In. The cancel signal and the ES to In signals are positive while the other three signals are negative, as they come from the pilot unit.

For entry into electronic storage from an Internal In bus column, there are four tubes Int En 8, 4, 2 and 1, (Fig. 21) conditioned respectively according to the permutation of different potentials representation of a digit on the In bus column. For entry into electronic storage from an Out bus-set column, there are four tubes designated Out En 8, 4, 2 and 1 conditioned or not conditioned selectively according to the permutation of different digit potentials representative of a digit on the Out bus-set column.

When an entry into an electronic storage unit from the Internal In bus-set is called for, the correspondingly numbered pilot unit emits the signals ESC and Int to ES concurrently but the latter signal has twice the duration of the former signal. The ESC signal operates two standard cancel circuits (Figs. 17 and 21) such as previously described and which respectively effect the resetting of the digit storage triggers in columns 1 to 10 and 11 to 20. The entry signal Int to ES is inverted by tube 9, Fig. 21, to a positive signal which operates the conditioned ones of the tubes Int En, causing them to reverse the related triggers as soon as the cancel signal ends.

When entry into an electronic storage unit from the correspondingly numbered Out bus-set is called for, the correspondingly numbered pilot unit concurrently produces the signals ESC and Out to ES. The signal ESC resets the digit storage triggers while the signal Out to ES is inverted by tube 10 to a positive signal which operates the conditioned ones of the tubes Out EN, causing them to reverse related triggers.

For exit from an electronic storage unit to the Internal Out bus-set, four tubes Int Ex 8, 4, 2, and 1 are provided for each column. The suppressors of these tubes are respectively coupled to the anode terminals *f* of the correspondingly numbered triggers in the same column. When a trigger is reversed, manifesting storage of a binary digit, it applies increased potential to the suppressor of the correspondingly numbered tube Int Ex, thereby conditioning the tube. If exit from an electronic storage unit to the Internal Out bus-set is called for, the correspondingly numbered pilot unit produces the negative signal ES to Int which is inverted by tube 12 to a positive signal for operating the conditioned ones of the tubes Int Ex causing them to apply reduced, digit representing potentials on the related buses of the Internal Out bus-set.

For exit from an electronic storage unit to the correspondingly numbered In bus-set, there are for each column, four electron tube lack couples In Ex C and four respectively related tubes In Ex. Each couple has its right hand tube (as shown) connected to the grid terminal *g* of the correspondingly numbered trigger. Accordingly, the tubes 1*a*, 2*a*, 4*a* and 8*a* of the In Ex C couples assume the same conditions as the right hand tubes of the correspondingly numbered digit storage triggers. When a trigger is in reversed condition, storing a binary digit, the related tube 1*a*, 2*a*, 4*a* or 8*a* is cut off. When exit from an electronic storage unit to the correspondingly numbered In bus-set is called for, the pilot unit sends a positive going signal ES to In to the tube 11 which applies the negative going counterpart In to In to the tubes 8, 4, 2 to 1 of the In Ex C couples. Those couples which have been partially cut off by the reversed triggers are now completely cut off, so as to apply increased potential to the correspondingly numbered tubes In Ex. These tubes become conductive and apply reduced potentials to the associated lines only of the four comprising one column of the In bus-set. Thus the permutation of reduced and non-reduced potentials on the four lines represent the digit stored in the Electronic Storage column.

As may be understood from the foregoing description and now with reference to Fig. 22, all the eight electronic storage units are connected via their respective tubes Int En (Fig. 21) to the common Internal In bus-set. However, entry

may be made from this common bus-set into one selected unit only upon receipt of an Int to Es entry signal from the corresponding pilot unit. In short, only a selected one at a time of the entry signals (Fig. 22) Int to ES1, Int to ES2 . . . Int to ES7 and Int to ES8 will be applied to ES1, 2 . . . 7 and 8 respectively.

Likewise, all the eight electronic storage units have exit connections via their respective Int Ex tubes (Fig. 21) to the common Internal Out bus (Fig. 22) but only a selected one at a time of the exit signals ES1 to Int, ES2 to Int . . . ES7 to Int and ES8 to Int will be produced, so that only a selected one of the electronic storage units at a time will read out upon the common Internal Out bus-set.

Each of the eight electronic storage units has an entry receiving connection via its Out En tubes to a correspondingly numbered one of the eight Out bus-sets. In this case any number of the entry signals Out to ES1, 2 . . . 7 and 8 (Fig. 22) may be produced concurrently so that numbers from the Out bus-sets may be applied concurrently to a plurality of the electronic storage units. Likewise the eight electronic storage units have individual exit connections via the couples in Ex C and tubes In Ex to the corresponding In bus-sets 1 to 8. Any number of the exit timing signals ES1 to In, ES2 to In . . . ES8 to In (Fig. 22) may be applied concurrently so that a plurality of electronic storage units may be read out concurrently upon their respective In bus-sets.

As stated previously in the General Description, all numbers on the Out bus-sets enter electronic storage units to be routed therethrough to selected destinations. Also, except for S1 and S2 codes from dial switches DS1 and DS2 (Fig. 40), all numbers on the In bus-sets are taken from the electronic storage units which receive them from selected sources, and the numbers are directed from the electronic storage units via the In bus-sets to selected receiving means.

Referring to Figs. 20 and 22, it is to be noted that columns 1 to 20 of an electronic storage unit are associated with columns 1 to 20, respectively, of the corresponding In and Out bus-sets. Thus, columns 1 to 20 of ES1 receive digits from columns 1 to 20, respectively, of Out bus-set 1 and apply digits to columns 1 to 20, respectively, of In bus-set 1. With respect to the relation between the electronic storage columns and the Internal In and Internal Out bus columns, columns 1 of the electronic storage units are all associated with columns 1 of the Internal In and Internal Out bus-sets. It is to be particularly noted, however, that columns 2 to 20 of all the electronic storage units are associated with columns 11 to 29, respectively, of the Internal In and Internal Out bus-sets. Thus, the sign digit column 1 of each electronic storage unit may read out a sign digit upon column 1 of the internal Out bus-set and receive a sign digit from column 1 of the Internal In bus-set, but on the other hand columns 2 to 20 of the electronic storage unit read out digits upon columns 11 to 29 of the Internal Out bus-set and receive digits from columns 11 to 29 of the Internal In bus-set. Columns 2 to 10, inclusive, of the Internal Out and of the Internal In bus sets are employed as described later.

7. Relay storage

Relay storage consists of sets of relay storage registers, also called relay storage units, which receive numbers from the In bus-sets and store them until called out for transmission along the Out bus-sets. Certain of the relay storage units also serve to control the printing unit, as will be explained in Section 21. There are ten sets of storage relays, designated the 0, 1, 2 . . . 9 sets, of which the 0 and 9 sets are diagrammatically and partially shown in Fig. 28. Each set has fifteen storage units and each unit has twenty columns of storage relays for storing a number in binary decimal form.

The fifteen units in a set which do the actual storing are respectively connectable to a common Input cable via the points of fifteen separate Unit In relays generally designated U "in" (see Fig. 29), which Unit In relays are controlled by the program, as described later. The fifteen units of a relay storage set are also connectable respectively to a common Output cable via the points of fifteen associated Unit Out relays generally designated U "out" which are also program controlled. The Unit In relays and their contact points associated with a relay storage unit may simply be referred to as a Unit In and designated by the number designation of the particular storage unit. For instance, the storage unit whose number designation is 010 is associated with Unit In 010. Similarly the Unit Out relays and their contact points may simply be referred to as Unit Outs and designated by the same reference number as the associated storage units.

The Input cable has 84 individual wires which are numbered 1 to 84 over which the permutations of voltage conditions representative of the digits to be stored are transmitted. Wires 1 to 80 pertain to the binary positions of digit columns 1 to 20 (Fig. 4, for example), the wire 81 is a back signal wire, and wires 82, 83 and 84 are relay storage reset signal wires. The wires 1 to 80 of the In cable terminate at plug sockets generally designated RS–GIPP (also see columns 1–20, RS–GIPP, Fig. 30). The wires 82, 83 and 84 terminate at plug sockets RS–GIPP 82, 83 and 84 (Fig. 29). Sockets RS–GIPP are pluggable to any of eight different gangs of plug sockets RS–GIP1 to P8 designated generally RS–GIP. Each of these gangs includes columns 1 to 20 plug sockets adapted to be connected through points of a set of relay storage Group In relays (controlled by the program), generally designated RS–GI, to the buses in columns 1 to 20 of one of the In bus-sets. Each gang of sockets RS–GIP also includes a socket RS–GIP82 (see 82 of RS–GIP1, Fig. 29, for example) which is connected through a Group In relay contact, when closed, to bus 82 of the related In bus-set. Socket RS–GIP82 may be plugged to any one of the sockets RS–GIPP–82, 83 and 84 for selective reset purposes as will be explained further. The back signal wires 81 is connected directly via Group In relay points, when closed, to bus 81 of the In bus-set. As may be understood, for each relay storage set, there are eight Group In relay sets which are designated RS–GI1 to RS–GI8 and connect to In bus-sets 1 to 8 respectively. For convenience, each of the sets of Group In relays RS–GI1 to RS–GI8 and their contacts may be referred to simply as "Group Ins" 1 to 8. The elements of a relay storage set may further be identified by a prefixed digit corresponding to the relay storage set number. For instance, the Group Ins for relay storage set 9 may be identified as 9RS–GI1 to 9RS–GI8. Thus, there are ten Group Ins RS–GI1, one for each of the ten relay storage sets, which connect

to the In bus set 1. Likewise, there are ten Group Ins RS–GI2, one for each relay storage set which connect to the In bus-set 2, and so on, making a total of 80 Group Ins, eight for each relay storage set.

The output cable of each relay storage set has 81 individual wires which, except for the wire 81 (see Fig. 29), terminate at plug sockets RS–GOPP (also see columns 1–20 of RS–GOPP, Fig. 30). These plug sockets may be plugged to any of eight gangs of columns 1 to 20 Group Out plug sockets RS–GOP. Each of the eight gangs of sockets RS–GOP1 to RS–GOP8 (Fig. 29) connects, through relay contacts, when closed, of Group Out relays RS–GO1 to RS–GO8, respectively, to one of the eight Out bus-sets. The Group Out relays are program controlled. Wire 81 in the output cable of a relay storage set connects directly via contacts in an active Group Out relay to bus 81 in the associated Out bus-set. Each of the Group Out relay sets and its contacts may simply be referred to as a Group Out. It is clear now that there are eight Group Outs for each relay storage set and which connect respectively to the eight Out bus-sets, making a total of 80 Group Outs for the ten storage sets.

As previously stated, each relay storage unit has twenty columns of storage relays for storing a number in binary decimal form. It is clear therefore that there are four relays in a column which may be called the "8," "4," "2" and "1" relays of a column. Fig. 29 shows the circuits of the "8" relay in column 1, the "1" relay in column 10 connected to line 40, the "8" relay in column 11 connected to wire 41 and the "1" relay in column 20 connected to line 80. These circuits are typical of the circuits of all the storage relays although it is understood that some of the relays have additional contacts such as the relays for controlling the printing unit. Each of the storage relays is a duo-wound relay. Upon energization of the pick-up winding of the relay, in a manner to be explained soon, it closes the relay points *a* to establish the circuit of the hold winding *h* of the relay. The circuit of the hold winding is from the +50 v. line through the hold winding, the relay points *a*, and via normally closed relay reset points LHR*a* or RHR*a* to ground. The reset points LHR*a* are provided for the left half of a storage unit; namely, for columns 1 to 10, and reset points RHR*a* for the right half of the storage unit; namely for columns 11 to 20. This enables the right and left hand halves of the storage unit to be reset independently and therefore to store numbers independently. In other words, if only 10-column numbers are to be handled, then one such number may be entered in one-half of a storage unit and another such number entered in the other half of a storage unit. The plugging from the plug socket RS–GIP82 of a Group In gang of sockets to the sockets RS–GIPP82, 83 and 84 is made selectively in accordance with whether the entire storage unit is to be reset or whether the left or right half is to be reset. If the entire storage unit is to be reset, then the socket RS–GIP82 is plugged to the socket RS–GIPP82. If the left half is to be reset, then the plugging is from the socket RS–GIP82 to the socket RS–GIPP83. Finally if, the right half is to be reset, the plugging is from the socket RS–GIP82 to the socket RS–GIPP84. As will be explained in Section 11, when a number is to be entered into a storage unit, the corresponding Unit In will be operated under control of the program, closing 84 contacts 1 to 84 (Fig. 29) between the wires of the input cable and the pick up coils of the relays in the storage unit. Also a Group In will be operated under control of the program to close contacts between a connected In bus-set and the related gang of plug sockets RS–GIP. Just prior to entry of the number, a preliminary reset signal is applied to the sockets RS–GIP82. Depending on the plugging, this reset signal will be transmitted to one of the wires 82, 83 or 84 of the input cable and thence through either the contacts 82, 83 or 84 of the Unit in Relays for the selected storage unit to both the reset relays LHR and RHR or one of them. There is a pair of these relays associated with each storage unit. Each of these relays is a duo-wound relay in which each of the windings operates the same set of armature contacts (see Section 3*c*). If the reset signal is applied to wire 82 of the Input cable, it is routed by contacts 82 of the operated Unit In through a coil of LHR and thence through a coil of RHR to the +150 v. line, thus causing energization of both coils. Accordingly, the contacts LHR*a* and RHR*a* will be opened and reset the entire storage relay unit. If the reset signal is applied to wire 83 of the Input cable, it is routed by contact 83 of the Unit In through a coil of LHR and to the +150 v. line, causing energization only of this one coil. Accordingly, only the left half of the relay unit will be reset. Finally, if a reset signal is applied to wire 84 of the Input cable, it is routed by contact 84 of the Unit In through a coil of RHR and to the +150 v. line, so that only the right half of the relay unit will be reset.

Each relay storage unit is identified by a three-place number. The units place digit in the identification number of a unit is the number of the relay storage set containing the unit. The two left-hand digits of a unit identification number distinguish a unit from the other units in the same group. Thus, in 0 relay storage set the units are designated 010, 020, 030 . . . 090, 100, 110 . . . 150. In the 9 set, the units are designated 019, 029 . . . 159. In other words, the unit 159 is the 15th unit in the 9 set.

As has been stated previously (see Section 6, for instance), all the numbers on the In bus-sets, with the minor exception of the artificial line of sequence described in Section 11, come from the electronic storage units and all the numbers on the Out bus-sets are directed to the electronic storage units. When the program or sequence means calls for a number to be entered (via the In bus-sets) into a relay storage unit, it brings about the energization of the Group In relay of one group only and the Unit In relays for the desired unit only through which the number is to be transmitted to the desired relay storage unit. Since each Group In is fixedly associated with a particular In bus-set which in turn is in fixed association with an electronic storage unit, it is clear that by selecting a certain Group In, a selection is made of one electronic storage unit from which the number is to be taken. Upon the energization of the selected Unit In, a back signal is sent to that pilot unit which is associated with the selected electronic storage unit. This back signal originates from the +150 v. supply line (labeled +150 v. b. s., Fig. 29) and is directed over the line shown dotted to the now shifted contacts *bs* of the active Unit In and via the corresponding, now closed, contacts *bs* of the active Group In to the bus 81 in the selected In bus-set. This back signal proceeds to the pilot unit where, in a manner explained later, it notifies

the pilot unit, so to speak, that the selected storage unit is ready to receive the number. The pilot unit then sends out a reset signal which is in the form of reduced potential on the bus 82 of the associated In bus-set. This reset signal is directed via contacts *r* of the active Group In to the plug socket RS–GIP82 and by plug wire to the desired one of the plug sockets RS–GIPP82, 83 or 84, depending on whether the entire storage unit or its left or right half is to be reset. Following the emission of the reset signal and consequent deenergization of the required relays in the selected relay storage unit, the pilot unit acts to send the exit timing signal ES to In (see Fig. 22) to the associated electronic storage unit, causing this unit to apply a permutation of reduced and non-reduced potentials to the connected In bus-set. The reduced potentials representative of the digit stored in the Electronic Storage Unit on the particular buses of the selected In bus-set are applied via the columns of contacts in the active Group In and via the plug connections between the associated sockets RS–GIP and the sockets RS–GIPP to the wires of the Input cable of the relay storage set containing the selected unit. The reduced potentials on the wires of the Input cable are further applied via the active Unit In to one side of the pick-up coils *p* of the selected relay unit and the circuits of these relay coils are completed to the +150 v. line. Since the voltage is reduced on one side of the selected coils, these particular pick-up coils are energized followed by the energization of the hold coils *h*, so that the particular number entered in the selected storage unit is stored therein.

In a manner explained later in Section 11, the program or sequencing means may call for a number to be read out of a relay storage unit by bringing about the energization of the related Unit Out. Also, the sequence means will bring about the energization of a Group Out in accordance with which electronic storage unit is to receive the number from the selected relay storage unit. Upon the energization of the selected Unit Out and Group Out, a forward signal is transmitted from the +150 v. source, over the dotted line (Fig. 29) and through the points *bs* of the Unit In (which cannot be energized on read-out) associated with the selected storage unit and thence via the contacts *fs* of the Unit Out made active by the program, to the wire 81 of the Out cable of the relay storage group, and via the corresponding contacts *fs* of the active Group Out to the bus 81 of the associated Out bus-set. The forward signal goes to the pilot unit associated with the electronic storage unit corresponding to the active Group Out and the connected Out bus-set. In a manner which will be explained subsequently, the forward signal notifies the pilot unit, so to speak, that the selected relay storage unit is ready to transmit the number. It may be noted that the forward signal is routed through the points *bs* of the Unit In for the selected relay storage unit. Hence, the forward signal is sent out only if these contacts *bs* are in normal status (as shown in Fig. 29), indicating the storage unit is not conditioned to receive data.

As understood, the relays of a relay storage unit are selectively energized to store a number and sign. The energized relays close their points *a* and *b* and additional points if the storage unit is one for controlling a recording unit (Section 21). As described, points *a* are in the circuits of the hold coils *h*. When a selected relay storage unit is to be read out, its Unit Out and a desired Group Out are energized. Readout circuits are thereupon selectively closed from the +150 v. source via the closed points *b* of the storage unit, which closed points are storing the number to be read out, the connected points of its Unit Out, to sockets RS–GOPP, plugwires to sockets RS–GOP of the bank related to that selected Group Out, and via contacts of the latter to bus columns 1 to 20 of the related Out bus-set. In this way, the data in the form of a number stored in a relay storage unit is read out as increased potentials placed on the selected permutation of buses of the selected Out bus-set (Fig. 21) and this number is entered in the associated electronic storage unit when the latter receives its entry signal Out to ES (as described above in Section 6).

The plugboard for a relay storage set is shown in simplified, diagrammatic form in Fig. 30. There is one such plugboard for each of the ten relay storage sets.

8. *Dial storage*

Besides relay storage (Section 7) and tape storage (Section 9), the machine provides other sources for values. One such source is dial storage. Representative of dial storage is dial storage set #3 which is diagrammatically and partially illustrated in Fig. 23. A dial storage bank consists of twenty dial switches, generally designated DST, and each dial switch is manually settable to a desired digit. Thus, twenty digits may be registered by the set of dial switches. The switches are further identifiable as column 1 to column 20 switches to conform with the numbering of the bus columns. It is understood that column 1 is the sign column and that columns 2 to 20 correspond to denominations 19 to 1, respectively. Each dial switch has three rings of contact segments having contacts 1 to 9 selectively wired to four output lines 8, 4, 2, and 1. The wiring is such that a decimal notation digit to which the dial is set will be read out in binary decimal form. For instance, if the switch in column 2 is adjusted to position 7, a circuit path is closed from the +150 v. line through the common switch arm to the 7 spot of the inner circle of contacts and to the 1 output wire; also from the switch arm via the 7 spot of the second circle of contacts to the 2 output line; and lastly from the switch arm via the 7 spot of the outer ring of contacts to the 4 output line. In this way the single adjustment of the switch arm to position 7 enables potential to be applied to the 1, 2 and 4 output lines so as to read out the decimal notation digit 7 as its binary terms equivalent 1, 2 and 4. The output wires of each column of dial switches are connectable through contacts *a* of dial storage Group Outs 1 to 8 to the Out but-sets 1 to 8 respectively. Fig. 23 indicates the Group Outs 1, 6 and 8. Each Group Out includes a group relay designated DS–GO and contacts *a* operated by the relay. In a manner which will be explained in Section 11, the program of sequence means may select any of the eight Groups Outs of dial storage set #3 for operation. Assume, for instance, that Group Out 1 is selected; i. e. relay DS–GO1 is energized by the program. Digit representing potentials thereupon will be applied through each dial switch column to the corresponding column of Out bus-set 1. For instance, if the column 2 dial switch is adjusted to 7, then potential will be applied to the 1, 2 and 4 output lines of this dial switch and thence by way of the associated contacts *a* of Group Out 1 to the buses

4, 3 and 2 in column 2 of Out bus-set 1 which respectively represent binary #1, binary #2 and binary #4 (Fig. 4a).

Along with the application of the digits, stored in the dial storage bank, to an Out bus-set, a forward signal is applied to bus 81 of this Out bus-set. The forward signal starts from the +150 v. line and is routed through the contacts 81 of the active dial storage Group Out to bus 81 of the related Out bus-set. The purpose of the forward signal will be explained in Section 16b, Item 24b.

9. Tape storage

Tape storage comprises three banks 1, 2 and 3, each with ten tape stations. Selection of a tape station is controlled by the sequence means in a manner described in Section 11. Fig. 31 diagrammatically shows the essential elements for transmitting information from a tape storage bank to any of the Out bus-sets 1 to 8. Associated with each station are two outlets called station selectors A and B. All the station selectors A are associated with a common set of plug sockets ASSP. All the station selectors B are associated with a common set of sockets BSSP. The information at a station may be read out alternatively through its A or its B station selector, as determined by the sequence means. For each bank of tape storage stations, there are eight Group Outs, each Group Out associated with a different one of the Out bus-sets. Each of the Group Outs is connected to a separate set of plug sockets TS–GOP. The sets of plug sockets ASSP and BSSP may be plugged in any desired combination to the sets of plug sockets TS–GOP, depending on which of the Out bus-sets are to receive information from stations through their A selectors and which of the Out bus-sets are to receive information from the stations through their B selectors. At this point, it may be brought out that if each station had only one outlet, then in order that a station in the bank be capable of reading out a number into any of the eight Out bus-sets, it would be necessary to connect the sensing brushes of the ten stations in the bank through the one station outlet to all of the eight sets of sockets TS–GOP. Under this condition, it would be impossible to read out more than one station of a bank at a time in view of the fact that selection of an outlet from one station and the concurrent selection of the outlet from another station along with selection of two Group Outs concurrently, would result in the reading out of the numbers from both selected stations upon both selected Out bus-sets. But it is desired to be able to read out at least two of the stations of a bank simultaneously upon two different selected Out bus-sets. To attain this object, each station is provided with the two outlets, station selectors A and B. Only one A outlet in a bank and only one B outlet in the same bank may be selected simultaneously. The sockets ASSP or BSSP may be plugged to all of the eight Group Out plug sockets TS–GOP, if it is desired to read out only one station at a time upon any selected Out bus-set. If it is desired to read out at least two stations of a bank simultaneously, then sockets ASSP are plugged, for instance, to a group of four of the sockets sets TS–GOP and the sockets BSSP are plugged to the remaining four sets of plug sockets TS–GOP. Then, the outlet A of one station and the outlet B of another station may be operated simultaneously and two selected Group Outs, one plugged to sockets ASSP and the other plugged to sockets BSSP may be operated to select the Out bus-sets upon which the numbers from the two selected stations may be respectively but simultaneously applied.

As understood now, the selection of a station in a bank to read out upon a selected Out bus-set requires the operation of one of its station selectors A or B and the Group Out associated with the desired Out bus-set. Each of the station selectors A comprises a gang relay ASS (see Fig. 32a) and each of the station selectors B includes a gang relay BSS. The station relays may be differentiated by a prefixed number corresponding to the associated station; e. g., relays 1ASS are associated with station 1. Each of the two relays ASS andBSS at a station operates contacts 3 to 80 (Figs. 4a and 32a) wired to the station brushes RB which sense index positions 3 to 80 (Fig. 4a) in record columns 1 to 20. Each brush at the station is wired to one side of a contact of the station relay ASS and a parallel contact of the station relay BSS. The other side of the contact of ASS is wired to a plug socket of the ASSP bank. The other side of the BSS contact is wired to a socket of the BSSP bank. The correspondingly numbered ASS contacts of all the stations are wired in common to the same plug socket ASSP and similarly the corresponding contacts of the BSS relays of the stations are wired in common to a corresponding plug socket BSSP. It is seen that if the ASS relay of a station is active, then its contacts connect the read brushes RB to columns 1 to 20 of sockets ASSP (also see Fig. 34), while if the BSS relay of this station is active, its contacts connect the read brushes to the columns 1 to 20 of sockets BSSP (also see Fig. 34).

Each of the tape storage Group Outs includes a gang relay TS–GO (see Fig. 32c) and contacts operated thereby. Contacts 3 to 80 of the Group Out (see Fig. 32a) are wired each at one side to columns 1 to 20 of the associated sockets TS–GOP and at the opposite side to columns 1 to 20 buses of the associated Out bus-set. The relays TS–GO and the sets of sockets TS–GOP may be further identified by a suffixed digit corresponding to the associated Out bus-set; e. g., TS–GO8 and TS–GOP8 are associated with Out bus-set 8. The relays TS–GO are selected by the sequence or program means in the manner described later in Section 11. Such selection circuit will connect ground to that one of sockets TS–GOS1 to 8 (Fig. 32c) wired to the desired relay, and the circuit will be completed through the desired relay to the +50 v. line. The grounding of socket TS–GOS1, for instance, will establish the circuits of gang relays TS–GO1, the circuits being completed to the +50 v. line. Only a few of the elements of TS–GO1 (several relays), TS–GO7, and TS–GO8 are shown, as illustrative, the others TS–GO2 to 6 being in a similar arrangement and connected to sockets TS–GOS2 to 6 (Fig. 53b). Likewise, the sequence means selects either the ASS or BSS relay of a desired station. Considering, for instance, relay 1ASS (Fig. 32c), the sequence means will ground the socket 1ASPP connected by plugging to 1ASP and a circuit will thereupon be completed via a normally closed relay point 1ACLa through the relay 1ASS to the +50 v. line. Energized relay 1ASS will shift the contacts 1ASSa so that when the pick

up circuit of the relay drops, the relays will momentarily remain energized through the shifted points and a series capacitor. It will be recognized that the points *a* of lASS along with the associated capacitor and resistor constitute an arc suppressor arrangement.

The data designated on a line of the tape under the read brushes of the selected station are read out while the record tape is at rest. A typical readout circuit is: From the +150 v. line (Fig. 32*a*) through the common brush CB, the contact cylinder 11*b*, the brush RB3 sensing a perforation in binary position 2, column 1 (see Fig. 4*a*), then via contact lASS3 or lBSS3 (depending on whether the lASS or lBSS relay has been energized), to the plug socket 2, in column 1 of ASSP (see Fig. 34) or to the corresponding socket BSSP, a plug connection from, say the ASSP socket, to the corresponding socket of TS–GOP1, for instance, and via the contacts 3 of TS–GO1 to bus 2, column 1 of the Out bus-set 1.

The above circuit applies increased potential to a bus of the Out bus-set. This increased potential is applied to the suppressor of a tube Out En (see Fig. 21) of the electronic storage unit associated with the selected Out bus-set. In the foregoing manner, the information read out of a designation line of the tape at the selected station is represented by increased potentials selectively applied to the tubes Out En associated with the electronic storage unit fixedly related to the selected Out bus-set (see Section 6).

At the same time that the information from the record tape is applied to the selected Out bus-set, a forward signal is applied to the bus 81 of this same bus-set. Assuming that station 1 is being read out to Out bus-set 1, the forward signal circuit extends from the +150 v. line, through normally closed contacts lACL*b* and lCCL*a*, thence via contacts 81 of the active lASS or lBSS relay, and either to a hub of the plug sockets AFS or BFS. If station selector relay lASS has been energized, then the forward signal circuit will be directed to a plug socket AFS while if the relay lBSS has been energized, the forward signal circuit will be directed to a socket BFS. If the sockets ASSP have been plugged, for instance, to the sockets TS–GOP1, the socket AFS will be plugged to the socket 81 of the same group TS–GOP1 (see also Fig. 34). On the other hand, if the sockets BSSP have been plugged to the sockets TS–GOP1, then a plug connection will be made between BFS and the socket 81 of TS–GOP1. The forward signal circuit will continue via the contacts 81 of TS–GO1 to bus 81 of the selected Out bus-set 1. The forward signal is transmitted by this bus to pilot unit 1, associated with Out bus-set 1, informing this pilot unit that the information from the selected station has been applied to the selected Out bus-set and is ready to be entered into electronic storage unit ES1 (Fig. 22). In other words, the forward signal is an indication that the proper Group Out has been operated, that the proper station selector has been operated, and that the station drum is not in motion. As will be brought out later in this section, the relays lACL and lCCL are deenergized while the tape at station 1 is at rest. There are similar circuit paths for the forward signal from each of the ten stations of a tape storage group. Each station has associated therewith correspondingly numbered relays ACL and CCL for controlling points in the path for the forward signal from the station. Each of these paths also extends through the contact 81 of either the ASS or BSS relay associated with the station. All the points 81 of the relays ASS are connected in common to sockets AFS and all the points 81 of the relays BSS are commonly wired to the sockets BFS.

In response to receipt of a forward signal, a pilot unit will operate to produce the entry timing signal Out to ES (see Figs. 21 and 22), causing the information applied from the record tape to the Out bus-set to be entered into the corresponding electronic storage unit.

After the pilot unit has sent forth the entry signal it sends out a Move signal, generally designated SMS. This signal is a negative going pulse on the bus 82 of the Out bus-set associated with the pilot unit. Depending on the program or coding, the Move signal will or will not be effective to produce a step of advance of the selected station from which the information has been read out. For each tape storage group there are two move relays MA and MB (Fig. 32*c*). If the program calls for the movement of the tape of any selected A station selector in the group, then the relay MA will be energized. If the program calls for movement of the tape to any station selector B in the group then the relay MB will be energized. It is clear that since two stations in a group may be read out concurrently, one through its A station selector and the other through its B station selector, that both the relays MA and MB may be simultaneously energized. When the program calls for movement of a tape at a station which has been read out through its selector A, then the sequence means operates in a manner described in Section 11 to apply ground to a socket MAPP plugged to MAP, thereby establishing the circuit of relay MA. Similarly, the sequence means may apply current to socket MBP to energize relay MB. If either of these relays MA and MB are energized, then the Move signal will be effective to cause a step of advance of a selected station in the group.

There is a Move signal receiving circuit associated with each Out bus-set. Fig. 32*a* shows the receiving circuits associated with the Out bus-sets 1 and 8. Bus 82 of Out bus-set 1 (Fig. 32*b*) is coupled to the control grid of an amplifier tube MST1. Normally, the bus 82 is at its upper level of potential, maintaining the tube conductive. The negative going Move signal on bus 82 cuts off the tube allowing its plate potential to rise. Similarly, the bus 82 of Out bus-set 8 is coupled to a tube MST8 and a Move signal on this bus will cut off this tube. Likewise, all the other Out bus-sets have their buses 82 coupled to tubes generally designated MST, each in a Move signal receiving circuit. For simplicity of explanation, assume that station 1 has been read out to Out bus-set 1 and is now to be advanced a single step. The Move signal on bus 82 of Out bus-set 1 cuts off tube MST1 which thereupon applies a positive going pulse via a capacitor to the contacts 82 of TS–GO1. It is clear that TS–GO1 is in energized condition under the assumption that Out bus-set 1 has been selected to receive information. Accordingly, contacts 82 of TS–GO1 are closed and the positive going pulse is applied therethrough to the plug socket 82 of TS–GOP1. This socket may be plugged either to a hub of Move signal sockets AMS or to a hub of Move signal sockets BMS (also see

Fig. 34) depending on whether it is intended to read out selected station 1 through its A station selector or its B station selector. Assume that station 1 selector A is being used. Accordingly, the plugging will be from the socket 82 of TS–GOP1 to a socket of the bank AMS. The positive impulse applied from the plate of tube MST1 will therefore proceed to the points *a* of the relay MA. Under the assumed conditions the relay MA will have been energized and its contacts *a* will be closed. The positive pulse will then proceed further through the contacts 82 (closed under the assumed conditions) of 1ASS to the station 1 Move network. If the program had called for station 1 to be read out through its B station selector and for movement of the station to be effected, the relay MB would have been energized and closed its contacts *a* and also the relay contacts 1BSS82 would be closed. Further, the plugging would have been from socket 82 of TS–GOP1 to the socket BMS and the positive impulse from the plate of tube MST1 would have been directed to the station 1 Move network via the contacts *a* of MB and the contacts 82 of 1BSS. There is a similar Move network for each of the ten stations. Each of the Move networks may selectively receive a positive pulse resulting from the Move signal coming from any of the Out bus-sets. Further, the positive pulse may be applied either through contacts 82 of the A or B station selector to the corresponding station Move network. While only the station 1 network is shown, it is to be understood that all the other station Move networks are similar.

To follow up the assumed example, a Move signal has been applied from bus 82 of Out bus-set 1 to the receiving network for the Move signal of this bus-set and the amplified inverted signal directed to the station 1 Move network. This amplified positive signal renders the tube 1MSA in the station 1 Move network conductive. The output of this tube is coupled to a Move circuit trigger in the station 1 Move network. This trigger includes the tubes MSR and MSL retroactively coupled, plate to control grid. The constants shown for the trigger are such as to make it a double stability trigger of not too acute sensitivity. When tube 1MSA is made conductive, it forces down the plate potential of tube MSR of the trigger, thereby turning the trigger to the condition in which tube MSR is conductive and tube MSL is non-conductive. When tube MSR becomes conductive, it establishes the circuit of the pick-up coil *p* of a delay relay 1ACL of the type previously discussed in Section 3*c*. After a momentary delay, the energization of relay 1ACL opens its contacts *b* in the forward signal circuit (see Fig. 32*a*). Further, the relay 1ACL opens the contacts *a* in the pick-up circuit for the station selector relays 1ASS or 1BSS (see Fig. 32*c*). It is clear thus far that as a result of the Move signal the previously selected station from which information has been read out is isolated from the selected Out bus-set and also the forward signal is terminated. Accordingly, after the Move signal has been applied, information cannot be read out from a station and a forward signal cannot be transmitted to a pilot unit.

When the Move circuit trigger (Fig. 32*b*) is in reversed status in which the tube MSL is non-conductive and the tube MSR is conductive, the tube MSL is applying increased potential to the control grid of a tube MSK. The screen grid of the tube MSK is coupled through contacts *b* of a relay 1CCL and the timer 1 for the entire bank of ten stations to the +150 v. line. The timer 1 makes in synchronism with the passage of ratchet teeth 23 (Fig. 6) across the clutch dog 30*d*. When timer 1 makes, it allows the tube MSK to conduct under the influence of the reversed Move circuit trigger. As soon as MSK becomes conductive, it establishes the circuit of coil *p* of the duo-wound relay 1BCL. As this relay is energized, its points *a*, *b* and *c* (Fig. 32*c*) close.

Referring to Fig. 33, it is seen that the make times of timers 1 and 2 alternate with respect to each other. After the timer 1 has operated to cause the pick-up coil of relay 1BCL to be energized, the timer 2 makes and renders a tube MSG conductive so as to establish the circuit of a delay relay MRG. After a slight delay, the relay MRG is effective to close its contacts *a* (see Fig. 32*c*). Since the contacts *a*, *b* and *c* of relay 1BCL have previously been closed, the following circuits are now completed upon the closure of contacts *a* of MRG. One of these circuits extends from ground via *a* of MRG and *c* of BCL through the clutch magnet 1SCM for station 1, to the +50 v. line. Another of the circuits is completed via *a* of MRG and *b* of BCL through the coil *h* of BCL. A third circuit is completed via *a* of MRG and *a* of BCL through the pick-up coil *p* of a duo-wound relay 1CCL. Contacts *c* of this relay close and the circuit of its coil *h* is established via these contacts and the now closed contacts *c* of 1ACL. Relay 1CCL opens contacts *b* (Fig. 32*b*) to prevent the picking up of relay 1BCL for a second time within one move period. Relay 1CCL also opens contacts *a* (Fig. 32*a*) to form another open point in the forward signal circuit. It may be seen from Fig. 33 that timer 1 causes the relay 1BCL to be energized prior to the operation of timer 2 in bringing about the energization of relay MRG. Accordingly, the circuit through the clutch magnet 1SCM will be made for a complete make period of the timer 2. In other words, the timing is such that even though the Move signal is received at a time which is random with respect to the timers 1 and 2, these timers serve to insure a full duration (make period of timer 2) of energizing pulse for the selected clutch magnet. Further, the timer 2 is so timed with respect to the travel of the clutch teeth past the clutch dog as to cause the circuit of the clutch magnet to be completed for tripping the clutch dog at a favorable time with respect to the clutch teeth.

After the clutch of the selected station starts to turn, the station commutator 44—44*b* (see Figs. 9 and 32*b*) makes and grounds the screen grid of the tube MSR, cutting off this tube so as to return the Move circuit trigger to its initial condition. Upon the return of the trigger, the circuit of relay 1ACL is disestablished and the points *c* of the relay open after an appropriate delay so as to drop out the relay 1CCL. The relays 1ACL and 1CCL, being deenergized, permit their respective contacts *b* and *a* (see Fig. 32*a*) in the forward signal circuit paths to reclose. Also, the contacts *a* of relay 1ACL reclose (see Fig. 32*c*) to allow the station selector relays 1ASS or 1BSS to be picked up again, if called for.

As described in Section 2*b*, each of the stations has a Move key SMK. Closure of this key switch establishes the circuit of the clutch magnet SCM for the station (see Fig. 32*c*). By this means, the tape at a station may be advanced under

manual control so as to position any desired designation line of the tape under the read brushes RB.

10. *The table look-up (Fig. 35)*

The table look-up apparatus is disclosed in detail in previously mentioned application Serial No. 768,000 of F. E. Hamilton et al., filed August 14, 1947. Briefly, the table look-up apparatus includes 36 tape stations which may be used to carry record tapes bearing, in coded form, mathematical tables of arguments and related function values. A table may be distributed over one or more tapes and a maximum of six tables may be handled by the table look-up means without changing the tapes at the stations. The sequence or program means (Section 11) selects a table from which a tape argument and function values are to be taken. The tape argument (and its function values) is selected by comparison with a computed argument which is obtained from a selected value source in the machine. The computed argument will be routed by way of a selected electronic storage unit to the associated In bus-set and then by way of a corresponding table look-up Group In and Table In and plugging (see Fig. 35) to a temporary computed argument storage device.

If a sequence field calls for a table look-up operation, it calls for selection of one of the six Table Ins and also for selection of one of the table look-up Group Ins. There are six Table Ins, one for each table which may be looked up. Each Table In includes a gang relay TL and its contacts 1 to 22. There are eight Group Ins, each associated with one of the eight In bus-sets. Fig. 35 shows, as illustrative, Table Ins 1 and 6, and Group Ins 1 and 8 associated with In bus-sets 1 and 8. Each Group In includes a gang relay TLU–GI and contacts 1 to 80 connected to columns 1 to 20 buses of the related In bus-set. The corresponding contacts 1 to 80 of all eight Group Ins are commonly connected to sockets 1 to 80 of a group of plug sockets BP. These sockets are variously plugged to plug sockets 1 to 22 of the different groups of sockets 1TP to 6TP. Each group of sockets TP is connected through contacts 1 to 22 of a Table In relay TL to elements of the temporary computed argument storage device, which include relays TCA1 to 22. The corresponding contacts 1 to 22 of the different relays TL1 to TL6 are commonly connected to the relay elements TCA1 to 22, respectively.

Assume, for instance, that a computed argument is to be used to select a tape argument from table 1 and that the computed argument is to be derived from electronic storage unit 1. The sequence means (Section 11) will cause the table look-up Group In relay TLU–GI1 to be energized and also will cause the Table In relay TL1 to be energized. The computed argument is limited in the present case to a five decimal place number and a sign. Such decimal place number and sign occupy 22 binary term positions. Therefore, any of the sockets BP1 to 80 may be plugged to the sockets 1 to 22 of the sets 1TP to 6TP. After the energization of relays TLU–GI1 and TL1, the computed argument present on the buses of In bus-set 1 will be transmitted, as will be explained further in Section 20, by way of the contacts of the Group In 1 to the plug sockets BP and via plugging to sockets 1 to 22 of 1TP, thence by way of the contacts 1 to 22 of TL1 to the temporary computed argument storage relays 1 to 22 and to the +150 v. line. It is understood now that digits are represented on the In bus columns by permutations of non-reduced and reduced potentials which reduced potentials may be taken as about 50 v. Accordingly, the circuit just traced will cause energization of the relays of TCA1 to 22 selectively in accordance with the permutations of voltages representative of the digits present on the In bus-set 1. In the foregoing manner a computed argument may be applied to a temporary computed argument storage.

In the manner described in the aforementioned application, the internal operation of the table look-up apparatus will be initiated by energization of relay R11. The circuit for energizing this relay will be explained subsequently.

After comparison with the computed argument has located the desired tape argument and its function values on the particular tape at the particular one of the 36 tape stations in the selected table, the function values as well as the tape argument may be read out to a selected Out bus-set. Fig. 35 shows at the right hand side the essential elements for reading out selected values. When the program means calls for table values to be read out, it calls for energization of one of the six Table Out relays 1TO to 6TO and of the table look-up Group Out relay TLU–GO which is associated with the Out bus-set intended to receive the table values. The table look-up apparatus includes station outlet relays ASS and BSS which function similarly to the relays ASS and BSS described in connection with tape storage (Section 9). The selection of the station relays ASS and BSS of the table look-up apparatus will not be described herein as it is fully explained in the aforementioned co-pending application. It is sufficient to state that when a Table Out relay is energized it completes a circuit through the relay ASS or BSS of the station (selected by the internal operation of the table look-up) containing the selected tape argument and function values. The selected station relay closes its contacts 3 to 80 connected to the read brushes of the tape at the station selected. It is to be noted that each Table Out includes a set of A contacts 3 to 80 and a set of B contacts 3 to 80. The contacts 3 to 80 of all the station relays ASS are connected in common to points 3 to 80, respectively, of the different sets 1A to 6A operated by the six Table Out relays 1TO to 6TO. Likewise, the contacts 3 to 80 of all the station relays BSS are connected in common to all the B sets of contacts 3 to 80. The contacts 3 to 80 of each A and B set terminate at A and B sets, respectively, of plug sockets RO3 to 80. These are variously pluggable, according to requirements to the sockets ROG1 to ROG8. Sockets 3 to 80 in each set of sockets ROG are connectable via contacts 3 to 80 of a Group Out to columns 1 to 20 buses of the related Out bus-set.

Assume, for instance, that station 1 is in table 6 and that a selected value is to be read out of station 1 through outlet 1ASS and upon Out bus-set 1. Further, assume that the table out relay 6TO and table look-up relay TLU–GO1 have been energized. Accordingly, readout circuits will be established from the +150 v. line through the sensing means for station 1, contacts 3 to 80 of 1ASS, contacts 3 to 80 of the 6A set operated by relay 6TO, thence to sockets RO of the 6A set and by plugging to sockets 3 to 80 of the group ROG1 and the contacts 3 to 80 operated by relay

TLU–GO1, to columns 1 to 20 buses of Out bus-set 1.

11. *Sequence storage and related circuits*

Sequence storage comprises means to receive and store sequence data and to control the program of machine operations in accordance with such data. The sequence data generally originate in the program tapes (see Section 2*a*) but may be derived from other sources such as relay storage (Section 7) or dial storage (Section 8).

Sequence storage is made up of two identical units, one called the A side, the other the B side. Each side is adapted to receive a complete set of sequence data. As explained in Section 2*a*, each set of sequence data consists of the 20 columns of S1Seq data (see Fig. 3) and the 20 columns of S2Seq data (see Fig. 4). The two identical sides A and B of sequence storage are provided in order to speed up operations of the machine since one side will receive a set of sequence data while the other side is still controlling per a preceding set of sequence data. Furthermore, there is some overlap in time between the functioning of the two sequence storage sides or units, to the end of speeding up the program of operations.

Except for an initial so-called artificial line of sequence data, the sequence data is routed to sequence storage through a pair of chosen electronic storage units. It may be assumed here that the electronic storage units ES7 and ES8 are the chosen units. ES7 will contain an S1Seq line of data and ES8 will contain an S2Seq line of data. The pilot units 7 and 8 (see Figs. 80*a* to 80*e* and 81) will operate, in a manner described later in Section 16*b*, Item 31, to apply the exit signals ES7 to In and ES8 to In (see Fig. 22) to electronic storage units ES7 and ES8 respectively. As a result the sequence data in ES7 and ES8 will be applied to the In bus-sets 7 and 8.

The A and B sides of sequence storage are to receive the sequence data alternately from the In bus-sets 7 and 8. For this purpose two relays AM and BM (Fig. 36) are alternately energized. Energization of AM will, in a manner of speaking, open the A side of sequence storage to the reception of sequence data while energization of BM will similarlly open the B side of sequence storage.

Referring to Fig. 36, when AM is energized, it closes its several points *a* to establish the circuits of a number of relays AS. The circuit for a relay AS extends from the +50 v. line through the relay and points *a* of AM to ground. Relay AM when energized also closes its points *b* to establish the circuit of a delay relay AMD of the type described in Section 3*c*. Relay AMD closes its several points *a* which are in arc suppressing circuits for the points AM*a* and AMD*a*. Each such arc suppressing circuit comprises a condenser AMC and a parallel, high ohmic resistor. Upon deenergization of AM, the deenergization of AMD is delayed slightly and its points *a* remain momentarily closed, allowing the condensers AMC to charge so that the circuits of relays AS decay relatively gradually with the result that the arcing of points AM*a* and AMD*a* is virtually suppressed.

The points of relays AS close so as to prepare circuits to be made through the so-called intermediate relays AI in the A side of sequence storage. There is one group of relays AI for each column of S1Seq data and S2Seq data (see Figs. 37, 38 and 39). Most of the relays AI are duo-wound, 4 or 6-position relays of the type described in Section 3*c*. Others of the relays AI, as in columns 20 of S1 and S2 sequence storage, are 12-position relays with only a single effective winding. The circuits of relays AI for storing the S1Seq data are similar to those for the S2Seq data and hence, only illustrative circuits for the S1Seq data are shown and will be described in sufficient detail. Considering, now, the S1Seq A side relays, the pick-up circuits of relays AI are connected by respective points AS*a* to the proper buses of In bus-set 7. Through these buses the pick-up circuits are connected to the plate circuits of the tubes In-Ex (Fig. 21) of the columns of electronic storage unit ES7. As may be understood from the previous description of electronic storage (Section 6), the tubes In-Ex of ES7 are selectively rendered conductive upon the receipt of the exit signal ES7 to In (see also Fig. 22) so as to manifest the binary digits stored in ES7. Each such tube when rendered conductive is limited to drawing current for only one relay circuit. Accordingly, with the exception of the units order S1 relays AI for positions 8, 4 and 2 there is only one single coil relay AI or duo-wound relay AI for each binary position in the sequence data. Since the number of circuits to be handled by sequence storage far exceeds the capacity of one relay per binary position, so-called sequence storage A side operational relays AOP are provided to be picked up in multiple by points of the relays AI. As many as thirty 12-point relays AOP may be provided for a single binary position of sequence data. Each column group of relays AI will thus pick up a corresponding column group of relays AOP (see Figs. 38, 41 and 42) but the number of relays AOP in each group is a multiple of the number of relays AI in the corresponding group. The prime purpose of relays AOP is to operate the necessary points in permutation circuits for converting the combinational binary coded sequence data numbers into related control functions. There is one function called "early and late" function which may be called for by the S1 data. If called for, it is to be brought into action before the other functions which are ordered by sequence data. The AOP relays are picked up under control of relays AI and hence subsequently to energization of relays AI. In order to provide for operation of the "early and late" permutation circuits prior to operation of the other permutation circuits, it is desired to use the earlier energized relays AI of the S1 group for operating the points of the "early and late" permutation circuits. The number of points in the units order of the latter circuits exceeds the capacity of four six-point relays AI, one for each binary position of column 20 (units order) of S1 data. Hence, the S1 column 20 group of relays AI is made up of 12-point relays of which there is one for binary position 1 and several for each of the other binary positions 8, 4 and 2 (see Fig. 37). To provide the power necessary to pick up the relays AI for each of the binary positions 2, 4, and 8 in column 20, amplification between the corresponding buses of In bus-set 7 and the relays is resorted to. When the AS*a* points have been closed and the exit timing signal ES7 to In has been applied to ES7, the tubes In-Ex of ES7 are selectively rendered conductive to produce reduced digit representing potentials upon the buses of In bus-set 7. With respect to buses 8, 4 and 2 of column 20, they are brought to terminals S1G8, 4 and 2 which are wired to correspondingly named terminals in Fig.

77b. Reduced potential on S1G2 is amplified by 120, Fig. 77b, and 110, 100, 90 and 80. The output of the latter four tubes goes to terminal S1P2 which is connected to the correspondingly named terminal in Fig. 37. When reduced potential is produced on terminal S1P2, current flows through a point AS*a* and a group of relays AI2 in column 20 to the +150 v. line. Similarly, reduced potential on S1G4 (Fig. 37) is amplified by 60*a*, 50 and 40 in Fig. 77b and the amplified current fed via S1P4 and a point AS*a* (Fig. 37) to a group of relays AI4 in column 20. Finally, reduced potential on S1G8 is amplified by 16, 30 and 20 (Fig. 77b) and the amplified power fed via S1P8 to a group of relays AI8 in Fig. 37. Thus, groups of 12-position, single coil relays AI for binary positions 2, 4, and 8 in column 20 are selectively energized. Only one 12-position, single coil relay AI is required for position 1 in column 20. For this relay, the bus 1 in column 20 of In bus 7 connects via a point AS*a* to relay AI for position 1 of column 20 and the circuit may be completed therethrough to the +150 v. line. The circuit of AI in position 1 of column 20 is typical of the circuit of other 12-position, single coil relays AI associated directly with buses of an In bus-set. When a single coil relay AI is energized, it establishes its hold circuit from the +150 v. line through the relay, a series resistor, the relay stick points *a*, and via normally closed points of a relay AIR, to ground.

With respect to the duo-wound, 4 or 6-position AI relays, their pick-up coils *p* are connected directly via points *a* of AS to the proper buses of In bus-set 7. An energizing circuit may be completed from such bus, when at reduced potential, via a point AS*a* through the pick up coil *p* and to the +150 v. line. The companion hold coil *h* of the relay is then energized by a circuit from the +50 v. line through the hold coil, the relay stick point *a* and normally closed AIR*a* points to ground.

When a relay AI is energized, it closes its points *b*, an illustrative pair of which are shown in Fig. 41, to pick up a multiple number of relays AOP. A typical pick-up circuit extends from the +50 v. line through a plurality of relays AOP (in parallel) and via a now closed pair of points AI*b* to ground. A hold circuit for the plurality of relays AOP is made from the +50 v. line, through the plurality of relays and via one or more of the relay stick points *a* (only one is shown for a group) and via normally closed points *a* of an A side operational reset relay AOR to ground. It may be mentioned that each of the normally closed contacts *a* of AIR (see Fig. 37) and of the relays AOR (see Fig. 41) is protected by an arc reducing parallel condenser and resistor arrangement, as indicated for one of the contacts in each of Figs. 37 and 41.

For simplicity, only a few of the circuits for the AI and AOP relays in the S1Seq A side of sequence storage have been shown, the other circuits being similar. There are duplicate sets of relays AI and AOP for the S2Seq A side of sequence storage (see Figs. 39 and 43). However, it is understood that the relays AI in the S2Seq A side are energized selectively under control of electronic storage unit ES8 acting via In bus-set 8. Also, the terminals S2G8, 4 and 2 and S2P8, 4 and 2 (Fig. 39) correspond to the similar terminals S1G and S1P (Fig. 37). The terminals S2G are connected to the amplifiers shown in Fig. 77b and the outputs of these amplifiers are directed to the terminals S2P.

The B side of sequence storage is a duplicate of the A side and each of the input connections to the relays AI of the S1Seq A side and S2Seq A side is wired to a corresponding relay BI in the S1Seq B side and S2Seq B side. The circuits of relays BI are established via points *a* of BS and are held via points *a* of BIR (Fig. 37). The circuits of relays BOP are similar to the circuits of AOP but are established via points *b* of relays BI and are held through points *a* of relays BOR (see Fig. 41).

The artificial line of sequence.—Mention has been made of an initial artificial line of sequence data. This consists only of S1 or S2 data or both and is inserted in sequence storage under manual control, as the starting instruction for the sequencing of operations of a problem. In other words, the artificial line of sequence data provides directions as to where the first real set or line of sequence data is to be obtained. By a real set of sequence data is meant such data as is called out automatically from tape storage or relay storage or other source for sequencing operations leading to the solution of a problem. The S1 and S2 data for the artificial line of sequence are set on dial switches DS1 and DS2 (Fig. 40) respectively. Each dial switch DS is of the same type as a switch DST (Fig. 23) described in Section 8 on Dial Storage. Briefly, the internal wiring of a dial switch is such that a decimal notation digit set up on the dial will be read out in binary decimal form. The wires 8, 4, 2 and 1 coming from a dial DS1 are associated with relay contacts S1R*a*. There are four contacts for each dial and they connect to the buses 8, 4, 2 and 1 in column 19 or 20 of In bus-set 7 or 8. As shown in Fig. 40, the dial DS1 (tens) is set at 0, the dial DS1 (units) is set at 1, and the dials DS2 are set at 02. The tens and units dials DS1 are respectively connected through the contacts S1R*a* to the buses in columns 19 and 20 of In bus-set 7. Similarly, the tens and units dials DS2 are connected by points S2R*a* to columns 19 and 20 of In bus-set 8. In order to enter the artificial line of sequence data into sequence storage, the operator closes switches SS1 and SS2 (Fig. 40a) or either one. The closure of the switch SS1 establishes the circuit of relay S1R from the +50 v. line through the relay and the switch to ground. Likewise, the closure of switch SS2 establishes the circuit of S2R. The energization of S1R closes its points *a* so as to cause the S1 data set up on the dials DS1 to be applied to columns 19 and 20 of In bus-set 7. Assume, for instance, that the tens dials DS1 were set to digit position 7. A circuit would then be established from ground through the switch arm of this dial, to the "7" segment in the inner circle and thence to the "1" output wire and the connected points S1R*a* to bus 1, column 19, of In bus-set 7; another circuit would be established from ground through the switch arm, the "7" segment in the second circle and via the output wire 2 and the connected points S1R*a* to bus 2, column 19, In bus-set 7; and a third circuit would be established from ground via the switch arm, the "7" segment in the outer circle to the "4" output line and via connected points S1R*a* to bus 4, column 19, In bus-set 7.

It is clear now that upon the closure of switches SS1 and SS2, reduced (ground) potential will be selectively applied to the buses of columns 19 and 20 of In bus-sets 7 and 8 according to the S1 and S2 data set on the dial switches

DS1 and DS2. These reduced potentials may serve in the same way as the reduced potentials produced on the buses under control of electronic storage units ES7 and ES8 to enter the S1 and S2 data into the A or B side of sequence storage, depending on which side is open. Actually the artificial line of sequence will be applied to the A side and enter the intermediate storage relays AI of columns 19 and 20 in the S1Seq A side and the S2Seq A side of sequence storage. The switches SS1 and SS2 are closed only momentarily by the operator since entry of the S1 and S2 data is effected very rapidly and after such entry it is desired that the switches be reopened.

As stated before, the relays AOP provide the necessary contacts in permutation circuits for translating the coded sequence data into the designated control functions. Also, the relays AI of columns 19 and 20 operate contacts in "early and late" permutation circuits. The BOP relays and the BI relays of columns 19 and 20 operate similar permutation circuits. In general the permutation circuits function to effect a conversion from the binary decimal code system to the single-point decimal notation system. The chief device for making the conversion is a so-called tree. Although several arrangements of the tree points are possible, they produce the same result and the choice depends largely on ease of wiring. A preferred tree arrangement is shown in Fig. 45. This is a full tree and is made up of points operated by four AOP (or BOP or AI or BI) relays storing the binary decimal terms of a digit of sequence data. The input to the tree is adapted to be placed in circuit either with the plate of a tube or with ground. When the tube is made conductive or the connection to ground is completed, the tree is said to be heated. There are ten possible outputs of the tree and these outputs are designated **0, 1, 2 . . . 9**. The points are so arranged that if the sequence digit is 0, a circuit path is established from the input via the normally closed points *1a*, *8b*, *4b* and *2d* to the output terminal "0." If the sequence digit is 1, then points *1a* are shifted, and a circuit path is closed from the input via the shifted points *1a* and the normally closed sides of *8a*, *4a* and *2b* to the output terminal "1." As another example, if the sequence digit is 7, then the points *1a*, *4a* and *4b* and the points *2a*, *2b*, *2c* and *2d* are shifted. A circuit path is then established from the input via the shifted points *1a*, the normally closed side of *8a*, the shifted points *4a* and the shifted points *2a* to the output terminal "7." Similarly, for any other binary decimal coded sequence digit, a circuit path is established from the input terminal of the tree to the output terminal corresponding to the decimal notation digit represented by the binary decimal terms.

Fig. 45*a* shows the block diagram representing a full tree. One or more of the output terminals of a tree related to a column of sequence data may be connected to the inputs of a plurality of other trees. Such an arrangement may be referred to as a tree pyramid, which may be represented diagrammatically as indicated in Fig. 50, for example. Hereafter, the AOP or BOP relays may simply be identified by the symbol designating the related sequence data field, subfield, and order or column of the subfield. For example, the relay Q*r*200 represents a relay for storing the binary digit 2 in the hundreds order of subfield Q*r* (decimal notation digit column 8; see Figs. 3 and 4*a*), of the Q field. Further, if reference is being made to a subfield of any one of a plurality of fields, the sequence storage relay may be designated simply by the subfield letter followed by the order designation; e. g., *r*200 designates a relay for storing 2 in the hundreds order of subfield *r* of any of different sequence fields.

As previously described in Section 2*a*, the T field is an Out field unless the OP2 code number is 01. To translate this code number into a control for the T Out trees, the form of tree shown in Fig. 46 is used. This tree includes points *a* of the relays OP2–80, 40, 20, 10, 8, 4, 2 and 1. It is seen that unless the OP2 code is 01 that the input of the tree is connected in circuit with the tree output OP0. If the OP2 code is 01, then the shifting of the points *a* of the relay OP2–1 directs the circuit from the input to the output line OP–01. Fig. 46*a* shows the block diagram representing this OP2 tree.

Fig. 44 shows a so-called "0" filter circuit. There is one such circuit for the *r* subfield of each of the sequence fields P, Q, R, T, U and V. The purpose of such filter is to prevent certain operations when the code in a mentioned one of the *r* subfields is 0. It is evident that unless there is a significant digit in the stated subfield, that a circuit path will not be established from the +150 v. line through the filter circuit to the output side of the circuit.

As is now understood, sequence storage receives and stores numbers codally representing a line of sequence data. This sequence data may instruct the machine to take values out of sources, enter values into receiving means, perform calculations such as accumulation, multiplication and division, effect selected denominational shifts of results, and select the sources for the next line of sequence data.

The sources from which values may be taken, as disclosed here, include electronic storage (Section 6), relay storage (Section 7), dial storage (Section 8), tape storage (Section 9), pluggable storage (Section 23), and the table look-up unit (Section 10). The receiving means for values include relay storage and the table look-up unit and, also a recording unit Section 21) which receives the values from an assigned relay storage unit. Selection of sources for values is controlled by the Out fields of sequence data and also by the S1 and S2 fields. Selection of receiving means for values is controlled by In fields of sequence data. Selection of mathematical calculations is controlled by the OP1 and OP2 fields of sequence data. Selection of denominational shift amounts is controlled as to the units order by the SH1 and SH2 fields and as to the tens order by the digits 4, 5, 6, 7, 8 or 9 in the *s* subfields of fields Q, R, U, and V, the even *s* numbers also determining right shift and the odd numbers left shift (see Section 2*a*). The S1 and S2 fields control selection of the sources for the next line of sequence data. The P field always is an Out field, the V field always an In field, the T field is an Out field when the OP2 code is any number other than 01 and an In field when the OP2 code number is 01. The Q, R, and U fields are Out fields if their respective subfields *s* contain 3 or less and In fields if their respective subfields *s* contain 4 or greater. The operational signs apply only to Out fields and are determined by the numbers 0, 1, 2 and 3 in their subfields *s*.

With respect to an Out field, the *r* subfield selects the value source and the *b* subfield selects the electronic storage unit to which the value is

to be sent. Selection of the electronic storage unit involves selection of a Group Out and the related Out bus-set and pilot unit (see Figs. 80*a* to *e* and 81). When the coding in the *r* subfield indicates that a value is to be taken from the table look-up unit, the coding also selects the Table Out relay (see Section 10).

With respect to an In field, the *r* subfield selects the value receiving means and the *b* subfield selects the electronic storage unit from which the value is to be transmitted. Selection of the electronic storage unit involves selection of a Group In and the related In bus-set and pilot unit. When the coding in the *r* subfield relates to the table look-up unit, it also selects a Table In relay (see Section 10).

Various premutation circuits controlled by sequence storage for translating the numbers codally representing sequence data into directed selections and operations will be described below. The first circuits to be described are for the selection of relay storage Group Outs generally designated RS–GO.

Relay storage Group Outs selection.—The code numbers for selecting relay storage units (Figs. 28 and 29) are the same as the identification numbers for these units, except for certain special numbers relating to selection of relay storage units for controlling recording operations. The identification numbers for the relay storage units are 010 to 150, 011 to 151, 012 to 152, 013 to 153, 014 to 154, 015 to 155, 016 to 156, 017 to 157, 018 to 158, and 019 to 159. When any of these code numbers 010 to 159 occurs in the *r* subfield of an Out field, it brings about the selection of a relay storage Group Out and the selection of the relay storage unit.

Fig. 47*a* represents the pyramids controlled by the Q field in the A and B sides of sequence storage for selecting the relay storage Group Out multiple relays RS–GO. There are eighty of these multiple relays, eight for each of the ten sets of relay storage (see Section 7), but only a representative number of the relays are shown. Fig. 49*a* diagrammatically represents the assembly of all the pyramids controlled by the several Out fields for selecting the relays RS–GO.

Referring to Figs. 47*a* and 49*a* and considering the A side, at a time determined by the closure of the several contacts XM*a* (see Section 16*b*, Item 9), the circuits are tested for completion through relays RS–GO. For each of the Q, R and U fields, the circuit extends to contacts XM*a* by way of normally closed *s*8 and *s*4 contacts. If both these contacts are closed, the number in the *s* subfield is 3 or smaller, indicating that the field is an Out field. Since the P field always is an Out field, the *s*4 and *s*8 contacts are not needed to test whether the field is an Out field and the circuit goes from ground directly to XM*a* contacts. The T field is Out if the OP2 coding is other than 01. Hence, for the T field circuit, connection is made from ground to the input of an OP2 tree (also see Figs. 46 and 46*a*) and from the OP0 output of the three to XM*a* contacts.

Considering now the Q field and referring to Fig. 47*a*, from the XM*a* contacts the circuit proceeds serially through normally closed contacts *a* of Q*r*800, Q*r*200 and Q*r*400. If all of these contacts remain closed, the hundreds order digit in the Q*r* subfield is not higher than 1, which is a condition for selection of relay storage. From contacts *a* of Q*r*400, the circuit extends to the common side of parallel contacts *a* of Q*r*100, Q*r*80, Q*r*40, Q*r*20, and Q*r*10. At least one of these contacts will be closed if the Q*r* subfield contains any of the code numbers 010 to 159. At this point, the circuit has ascertained that relay storage has been called. It remains for the circuit to select one of the eighty relay storage Group Outs. This selection is determined by the digit in the *b* subfield and by the units place digit in the *r* subfield. The *b* subfield determines which Out bus-set is to be used and must therefore make a selection among the eight relay storage Group Outs 1 to 8 (see Section 7). Thus, if the *b* code number is 1, it makes a selection of Group Outs 1, each of which connects to Out bus-set 1. There are ten Group Outs #1, one for each of the 10 relay storage sets 0 to 9. Selection must be made not only of one of the eight sets of Group Outs but also of a particular one of ten Group Outs from the selected set in order that a particular relay storage set be connected to the selected Out bus-set. As explained in Section 7, the units place digit in the identification number of a relay storage unit represents the relay storage set containing the storage unit. Hence, the selection of a particular one of the ten relay storage Group Outs from a selected set of these Group Outs is determined by the code digit in the units order of the *r* subfield. Therefore, by combining the control by the *b* subfield with the control by the *r* units order code number, a particular relay storage Group Out will be selected. Considering for instance the Q field, the control by its *b* subfield is effected through a Q*b* tree (also see Figs. 45 and 45*a*). The eight output lines 1 to 8 of this Q*b* tree connect respectively to eight similar Q*r* units trees (8) to (1). These units trees (1) to (8) relate to the eight sets of Group Outs 1 to 8, respectively. Thus, according to the number in the Q*b* tree, one of these eight units trees (1) to (8) is selected, thereby effecting a selection of one of the eight sets of Group Outs. Each of the Q*r* units trees has its ten outputs connecting through plugging between sockets RSG and RSGP (also see Fig. 53*b*) to ten Group Out gang relays. Thus, according to the Q*r* units digit, one of the ten Group Outs from the selected set will be operated. Considering, for instance, the (1) units tree, its ten outputs are connected to the multiple relays 0RS–GO1 to 9RS–GO1. If this (1) tree is selected by the Q*b* tree and the Q*r* units digit is 9, then the relay 9RS–GO1 will be selected.

The above explanation clarifies the remainder of the circuit. The circuit was traced before to the output side of the parallel contacts Q*r*100, Q*r*80, Q*r*40, Q*r*20 and Q*r*10. From there, the circuit continues, via X2*a* contacts, to the input of the Q*b* tree and through this tree to the input of one of the eight Q*r* units trees (1) to (8). The circuit is completed via the selected units tree and plugging through one of the relays RS–GO associated with the selected tree.

As a specific example, assume the code number in the Q*r* subfield is 159 and the code number in the Q*b* field is 1. The circuit will be made, in the manner described, to the input of the Q*b* tree. As this tree is set to 1, the circuit will continue to the input of the Q*r* units tree (1). The Q*r* units digit is 9, so the Q*r* units tree (1) directs the circuit to its 9 output line which is wired to plug socket RSG1–9 (also see Fig. 53*b*). This will be plugged, normally, to the socket RSGP1–9 and the circuit will be completed through multiple relay 9RS–GO1 (Fig. 47*a*) to the +50 v. line. The energization of relay 9RS–GO1 operates the relay storage Group Out 1 for the relay storage set 9

(see Fig. 28), connecting its Out cable to Output bus-set 1.

Each of the contacts XM*a* is shunted by contacts XMD*a* (see Figs. 47*a* and 49*a*). Relay XMD is of the delay type discussed in Section 3c and is in series with relay XM (see Fig. 36), so as to be controlled by the same circuit. Accordingly, after deenergization of XM, relay XMD is still energized and its contacts XMD*a* (Fig. 47*a*) remain closed to hold the circuit, if previously made, through a relay RS–GO. The contacts XMD*a* are in series with a capacitor XMDC and as this capacitor charges, the current decays to zero. Hence, when relay XMD deenergizes, there is no arc across its points *a*. In this manner, the arcing of any of the contacts in the circuits for selecting relays RS–GO is suppressed. The capacitor XMDC is discharged through the normally closed points *b* of relay XMD and a series resistor.

The A sequence side circuit shown in Fig. 47*a* has been described. The B sequence side is similar; its trees and *r* contacts are operated by BOP relays in the B side instead of by AOP relays in the A side. For the B side, the timing contacts YM*a*, YMD*a*, and Y2*a* take the place of the contacts XM*a*, XMD*a* and X2*a*, respectively. Energization of relays YM, YMD and Y2 will be described in Section 16*b*, Item 36.

It is to be noted that the Q*b* tree is a feeder tree for the Q*r* units trees. In other cases, a tens order tree may be used as the feeder for units order trees relating to the same sequence field. Also, a hundreds order tree or its equivalent may be used as a feeder for the tens order tree. Such an arrangement of trees constitutes a tree pyramid for translating a plural digit code number into a single directional control operation. A tree pyramid consisting of a feeder tree superimposed on other trees may be shown diagrammatically in the manner illustrated in Fig. 49*a*, for instance. A tree pyramid may be identified by its function; i. e., the pyramids shown in Figs. 47*a* and 49*a* are RS–GO pyramids.

All the corresponding units order trees of the RS–GO pyramids in the A and B sides of the P, Q, R, T and U fields of sequence storage connect to common lines leading to the plug socket RSG, as may be seen in Fig. 49*a*.

Relay storage Unit Outs selection.—Fig. 48 illustrates the permutation circuit for selecting relay storage Unit Outs (see Section 7). For economy of illustration, the showing in Fig. 48 is not repeated for each Out field but represents the circuit which may be set up under control of any of the Out fields P, Q, R, T and U. For the P field, the contacts *b* of *s*8 and *s*4 are omitted for reasons previously stated. Also, for the T field, the contacts *b* of *s*8 and *s*4 are shunted by an OP2 tree, for reasons now understood. The circuit, on the A side, is timed by contacts XM*b*, XMD*c* and X2*b* and on the B side by the corresponding contacts YM*b*, YMD*c* and Y2*b*.

Considering the A side, upon closure of contacts *b* of XM and X2, the circuit extends from ground through contacts *b* of *s*8 and *s*4 (for the Q, R, or U fields) to contacts XM*b* or directly to XM*b* (for the P field) or through an OP2 tree (for the T field). The circuit continues via the normally closed contacts *b* of *r*800, *r*400 and *r*200 and thence via X2*b* to the common blade of contacts *b* and *c* of *r*100.

As previously stated, the relay storage code numbers are 010 to 159. If the code number is 0 in the hundreds order of subfield *r*, the circuit continues through the normally closed contacts *b* of *r*100 to the input of the *r* tens tree in the 010 to 099 pyramid. But if the code number is 1 in the hundreds order, contacts *c* of *r*100 are closed and the circuit is routed to the *r* tens tree of the 100 to 159 pyramid.

Assume that the *r* tens tree in the 010 to 099 pyramid has been heated; i. e., the circuit to its input has been established. This tens tree feeds nine *r* units trees (1) to (9) and according to the tens order digit in the *r* subfield, one of these *r* units trees is heated. Each of these units trees has ten outputs wired to plug sockets RSU (also see Fig. 53*a*). These are plugged to corresponding sockets RSUP which connect to the relay storage Unit Out relays U "out" (also see Fig. 29). Depending on the *r* units order digit, the heated *r* units tree will direct the circuit through the connected plug sockets and a multiple relay U "out" to the +50 v. line.

Assume, now, that the *r* tens tree in the "100 to 159" pyramid has been heated. The outputs 0, 1, 2, 3, 4 and 5 of the tree feed five *r* units trees (0) to (5), respectively. Each of these units trees has ten outputs connected through the mentioned plugging to relays U "out."

It will be observed that the circuit shown in Fig. 48 includes, in effect, a pyramid made up of a hundreds order *r* tree (contacts of *r*800, *r*400, 4200 and *r*100), a pair of *r* tens trees fed by the hundreds order tree, and fifteen *r* units trees fed by the *r* tens trees. Such pyramid is effective to reduce a three-place number to a selection of the element identified by the three-place number. Thus, the fifteen *r* units trees provide 150 outlets, each connected to a different one of the 150 Units Out gang relays U "out," each such gang relay being associated with one of the 150 relay storage units (see Section 7).

In the foregoing manner, if the code number in the *r* subfield of an Out field is 010 to 159, one of the relay storage units is selected to transmit a number to the Out bus-set selected by the RS–GO pyramid for this field (see Figs. 47*a* and 49*a*).

The table look-up Group Outs selection.—Fig. 47*b* shows the A and B side circuits, of an Out field of sequence storage, for selecting a table look-up Group Out (see Section 10). There is a network such as shown in Fig. 47*b* for each of the Out fields but for economy of illustration only a single one of the networks is shown. Each such network relating to a sequence storage field is connected to the normally open *r*200*c* points of the field (see Figs. 47*a* and 49*a*).

The code for table look-up is one of the numbers 281 to 286 in the *r* subfield. If the field is an Out field, a circuit through the A side will be established when contacts of relays XM and X3 (see Section 16, item 10) close through one of the table look-up Group Outs. A similar circuit may be established through the B side when circuits of YM and Y3 close. There are eight of these table look-up Group Outs and their selection is determined by the digit in the *b* subfield.

For simplicity of explanation, assume that the network shown in the upper portion of Fig. 47*b* is the Q field network. Assume, further, that the Q*r* number is 285 and the Q*b* number is 1. A circuit may then be established from ground (Fig. 47*a*) via contacts Q*s*8*a*, Q*s*4*a*, XM*a*, Q*r*800*a*, Q*r*200*c*, the (Q)*r*200*c* line (also see Fig. 47*b*), and thence via contacts *r*400*b* (of the Q field),

and X3*a* to the input of the *b* tree (Q field). The circuit will be routed by this tree and by a plug wire between sockets TLGO and TLGOP (Fig. 53*a*) through one of the eight gang relays TLU–GO1 to TLU–GO8 (also see Fig. 35).

The table outs selection.—As explained in Section 10, concerning the table look-up unit, a tape argument will be selected from one of six tables. When this argument is to be read out, the table out relay TO (Fig. 35) must be energized, along with a table look-up Group Out. Code numbers 281 to 286 respectively identify tables 1 to 6.

Fig. 47*c* shows the form of circuit for selecting one of the relays 1TO to 6TO. For the A side, the input of the circuit comes from the XM*a* contacts of the related field and for the B side, the input comes from the YM*a* contacts (see Figs. 47*a* and 49*a*). The circuit continues through contacts *r*800*c*, *r*400*d*, *r*200*d*, contacts *b* of X3 or Y3 (depending upon whether the circuit is in the A or in the B side of sequence storage); thence via *r*100*d*, *r*80*c*, and the *r* units tree to one of the output lines 281 to 286. The circuit is completed via plugging between sockets TOP and TOPP (also see Fig. 53*a*) and normally closed interlock contacts TOC*a* through a table relay TO to the +50 v. line.

Tape storage Group Outs selection.—As described in Section 9, there are three banks 1, 2 and 3 of tape storage. Each bank has eight Group Outs associated with Out bus-sets 1 to 8 (see Figs. 31 and 32*a*). Selection of a tape storage Group Out therefore requires selection of a tape storage bank and selection of one of its Group Outs. The selection of a bank is determined by the tape storage code number in an *r* subfield and selection of one of the Group Outs from this bank is determined by the digit in the adjacent *b* subfield.

The code numbers for tape storage stations run from 403 to 422 and 503 to 522 for bank 1; from 433 to 452 and 533 to 552 for bank 2; and from 463 to 482 and 563 to 582 for bank 3. It is seen that the hundreds order digit 4 or 5 identifies tape storage; that any of tens order digits 0, 1, and 2 identifies bank 1; any of tens order digits 3, 4, and 5 identifies bank 2; and any of tens order digits 6, 7 and 8 identifies bank 3.

Fig. 47*b* shows the A and B side pyramids of the Q field of storage for selecting the tape storage Group Outs. The input of the pyramid, in the A side, is connected to the Q*r*400*e* line on the A side (see also Fig. 47*a*) and the pyramid in the B side is connected to the Q*r*400*e* line on the B side. The timing of a circuit through the A side pyramid is controlled by relays XM, X4, X5 and X6 (see Section 16*b*, items 9 and 11). The timing of a circuit through the B side is controlled by relays YM, Y4, Y5 and Y6 (Section 16*b*, Item 36).

Considering the A side, the circuit path to and through XM*a* contacts (Fig. 47*a*) is as previously traced for the RS–GO pyramids. From XM*a*, the circuit extends via Q*r*800*a* and Q*r*200*a* to the common blade of Q*r*400*a* and Q*r*400*e*. If a tape storage code is present in the Q*r* subfield, Q*r*400 is energized and closing Q*r*400*e*. The circuit then proceeds to the input of the Q*r* tens tree (Fig. 47*b*). The outputs 0, 1 and 2 of the tree are commoned and lead via X4*a* to the input of the Q*b* tree #1 pertaining to bank 1. Outputs 3, 4 and 5 all lead via X5*a* to the input of the Q*b* tree #2, pertaining to bank 2, and outputs 6, 7 and 8 of the Q*r* tens tree all lead to the input of the Q*b* tree #3 relating to bank 3. Thus, depending on the tens order digit of the code number in the Q*r* subfield, the circuit will be directed to the input of one of the three Q*b* trees. The eight outputs of the Q*b* tree #1 are connected to the eight sockets GOSP for bank 1 (see also Fig. 53*b*). The outputs of the Q*b* tree #2 connect to eight sockets GOSP for bank 2, and the outputs of Q*b* tree #3 connect to eight sockets GOSP for bank 3. Thus, depending on the Q*b* code digit, the selected Q*b* tree will direct the circuit to one of the sockets in the related group of eight sockets GOSP. The eight sockets GOSP1 to 8 for a storage bank are plugged to the eight sockets GOS1 to 8 (Fig. 32*c* and Fig. 53*b*). The circuit therefore will be completed through a gang relay TS–GO (see Fig. 32*c*) to the 50 v. line.

In the foregoing manner, one of the Group Outs in a tape storage bank is selected.

It is understood by now that there are similar A and B side pyramids for each of the Out fields P, Q, R, T and U and that corresponding output lines of their respective Q*b* trees are connected to the same plug sockets TS–GOSP. Fig. 49*b* is included to make this clear. The inputs of the P, Q, R, T and U pyramids in Fig. 49*b* connect respectively to the P*r*400*e*, Q*r*400*e*, R*r*400*e*, T*r*400*e* and U*r*400*e* contacts in Fig. 49*a*.

Tape storage station relays selection.—In Section 9, it was brought out that there are two alternatively operated relays ASS and BSS for each of the tape stations. As there are thirty stations in all, there are sixty station relays ASS and BSS. The tape storage code number calls for a particular one of these station relays. All tape storage code numbers have hundreds order digit 4 or 5. The tens and units order digits identify a particular station relay regardless of whether the hundreds order digit be 4 or 5, the distinction being that hundreds order digit 5 calls for the station tape to move after being read out while hundreds order digit 4 calls for the station tape to remain at rest after being read out. Tens order digits 0, 1, and 2 characterize code numbers for station relays in tape storage bank 1; tens order digits 3, 4, and 5 are in the code numbers for relays of bank 2; and tens order digits 6, 7 and 8 are in code numbers for relays of bank 3. Units order digits which are odd relate to relays ASS and units order digits which are even relate to relays BSS. The ten station relays ASS in bank 1 are identified as follows, ignoring the hundreds order digit 4 or 5: 1ASS (station 1) by 03; 2ASS by 05, 3ASS by 07, 4ASS by 09, 5ASS by 11, 6ASS by 13, 7ASS by 15, 8ASS by 17, 9ASS by 19, and 10ASS by 21. The ten BSS relays in bank 1 are identified as follows: 1BSS by 04, 2BSS by 06, 3BSS by 08, 4BSS by 10, 5BSS by 12, 6BSS by 14, 7BSS by 16, 8BSS by 18, 9BSS by 20, and 10BSS by 22. Similarly, the relays 1ASS to 10ASS in bank 2 are identified by code numbers having 4 or 5 in the hundreds order followed by the numbers 33 to 51 and the relays 1BSS to 10BSS by numbers 34 to 52. The relays 1ASS to 10ASS in bank 3 are identified by numbers 63 to 81 and the relays 1BSS to 10BSS by numbers 64 to 82.

Fig. 47*d* shows the form of tens and units order pyramid for selecting relays ASS and BSS. It is understood that there is one such pyramid in the A and B sides of each Out field of sequence storage; i. e., for fields P, Q, R, T, and U. It is further understood that the corresponding outlets of all these pyramids are commoned in the

manner shown for the RS–GO and TS–GO pyramids (Figs. 49*a* and *b*).

Assume for simplicity of description that the pyramid shown in Fig. 47*d* is the Q pyramid in the A side. A circuit may then make as follows: From ground (Fig. 47*a*) via Q*s*8*a*, Q*s*4*a*, XM*a*(Q), the connected XM*a* line (also see Fig. 47*c*), (Q)*r*800*d*, (Q)*r*400*f*, (Q)*r*200*e*, the (Q)*r*200*e* line (also see Fig. 47*d*) to the input of the (Q)*r* tens tree. Since relay *r*400 is operated when the hundreds order digit is 4 or 5, it is seen that the *r* tens tree in Fig. 47*d* will be heated in either case. The tens order digit in the tape storage code number may be 0, 1, 2 . . . . 8. Accordingly, the nine output lines 0 to 8 of this tens tree are connected through heating contacts *b* of relays X4, X5, and X6 (the A side is being discussed) to the inputs of nine *r* units trees (0) to (8). Depending on the units order digit in the code number, the heated one of the *r* units tree will direct the circuit to one of the sixty sockets ASPP and BSPP (also see Fig. 53*a*).

As a specific example, if the code number is 403 or 503, the *r* units tree (0) in Fig. 47*d* will be heated and will direct the circuit to plug socket 1ASSP (bank 1). This socket will be normally plugged to socket 1ASP (bank 1) so that the circuit will be completed via an interlock point *a* of 1ACL (Fig. 32*c*) through gang relay 1ASS (bank 1) to the +50 v. line.

The station move relays selection.—As described in Section 9, there are two move relays MA and MB (Fig. 32*c*) for each bank of ten stations. Relay MA when energized closes its contacts *a* (Fig. 32*b*) to allow any of the selected ASS relays of the bank to transmit the effect of a move signal to the related station move network. Relay MB when energized serves a similar purpose in relation to the BSS relays of the storage bank. If the code number for a tape storage station has the hundreds order digit 4, then neither the MA nor MB relays, in the bank containing the selected station, will be energized. But if the code number for the station has the hundreds order digit 5, then the relay MA will be energized if any station relay ASS is selected and relay MB will be energized if any station relay BSS has been energized. It has been explained that the ASS relays are selected by code numbers with units order digits which are odd while the BSS relays are selected by code numbers with units order digits which are even. Also, any of the tens order digits 0, 1 and 2 selects tape storage bank 1; any of tens order digits 3, 4 and 5 selects storage bank 2; and any of tens order digits 6, 7 and 8 selects bank 3. Thus, there are three factors to be considered in the selection or non-selection of the move relays; one, whether the hundreds order digit is 4 or 5; another whether the units order digit is odd or even; and, finally, with respect to the selection of a move relay from a particular storage bank, whether the tens order digit is in one of the three mentioned groups of digits.

Fig. 47*c* shows the form of selecting circuit for the move relays. The input for this circuit connects to the XM*a* or YM*a* line, depending on whether the A or B side of sequence storage is being considered. The XM*a* or YM*a* line is the same as previously discussed in connection with the Table Outs Selection. From the XM*a* or YM*a* line the circuit continues through *r*800*c* to the common of contacts *r*400*d* and *r*400*g*. If the code number has 4 or 5 in the hundreds order, then it relates to tape storage and relay *r*400 is energized, closing *r*400*g*. The circuit proceeds via *r*200*f* to contacts *r*100. If the hundreds order digit in the code number is 5, then the code number calls for tape movement; relay *r*100 is energized along with relay *r*400, and contacts *r*100*e* are closed, directing the circuit to the common of contacts *r*1*a* and *r*1*b*. If the units order digit in the tape storage code number is even, then sequence storage relay *r*1 will not be energized since the binary terms of all even digits are lacking the binary term 1. But if the units order digit is odd, then the binary terms representing this digit include binary term 1 and relay *r*1 is energized. If *r*1 remains deenergized, its points *b* are closed, leading the circuit to the input of the *r* tens tree in the BSS move tree. If *r*1 is energized, its points *a* are closed and the circuit is directed to the input of the ASS move tree. Depending on the tens order digit in the code number, the selected *r* tens tree will lead the circuit through a control relay point of X4 (or Y4), or X5 (or Y5) or X6 (or Y6) to one of the plug socket MAPP1, 2 or 3 or MBPP1, 2 or 3. The sockets MAPP1, 2 and 3 are normally plugged to sockets MAP1, 2 and 3 (see Fig. 53*b*) and sockets MBP1, 2 and 3 are normally plugged to sockets MBP1, 2 and 3. Fig. 32*c* shows the sockets MAP and MBP of a relay storage bank. Assume, for instance, that sockets MAP and MBP in Fig. 32*c* relate to bank 1 and that the ASS move, *r* tens tree (Fig. 47*c*) has been heated. Assume, further, that the tens order digit is 2, so that the output of the tree is directed to bank 1 socket MAPP, plugged to socket MAP in Fig. 32*c*. Accordingly, the circuit will be completed through relay MA of bank 1 to the +50 v. line.

Both relays MA and MB of the same bank may be concurrently energized, but under control of code numbers in different sequence fields. For instance, field P may call for selection of the station relay 2ASS in bank 1 and field Q may call for selection of the station relay 6BSS in bank 1, with the code numbers in each field also calling for station movement. The move selection circuit of sequence storage field P will then cause energization of the relay MA of bank 1 and the move selection circuit of sequence storage field Q will cause energization of the relay MB in bank 1.

Energization of the relays MA and MB or either of them, allows the move signals or signal to be effective, in the manner described in Section 9.

Selection of dial storage unit #3.—If the code number in an *r* subfield is 603, it calls for a value to be read out of dial storage unit #3 (see Fig. 23). The *b* subfield selects the Dial Storage Group Out, depending on which Out bus-set is to receive the value from dial storage (see Section 8).

Fig. 47*c* shows the form of selection circuit for the Group Outs of dial storage unit #3. The circuit connects to the XM*a* (or YM*a*) line, previously discussed, and continues through the points *r*800*d*, *r*400*f*, *r*200*g*, *r*100*f*, and control contacts X2*c* (or Y2*c*) to the input of the *r* tens tree. Thus, the latter tree will be heated if the hundreds order digit in the *r* subfield is 6. If the tens order digit is 0, then the *r* tens tree continues the circuit to the *r* units tree. If the units order digit is 3, then the *r* units tree heats a *Qb* tree. This particular *Qb* tree will thus be heated only if the code number in the *r* subfield is 603. Depending on the digit in the adjacent *b* subfield, the *Qb* tree directs the circuit to one of the plug sockets DSP1 to 8 (also see Fig. 53*a*). The sockets DSP1 to 8

are normally plugged to sockets DSPP1 to 8 to complete the circuit through the selected dial storage Group Out gang relay DS–GO to the +50 v. line. As shown in Fig. 23 and explained in Section 8, each dial storage Group Out connects the value register dials of dial storage unit #3 to a different one of the Out bus-sets.

S1 and S2 pyramids for sequence data selection.—The S1 and S2 fields of a line of sequence data select the sources for the next line of sequence data to be entered in the A or B side of sequence storage. The sequence data may be selected from relay storage in which case the S1 and S2 fields of sequence storage must select relay storage Group and Unit Outs. Sequence data may be selected also from tape storage. In that case, the S1 and S2 fields of sequence storage must select tape storage Group Outs and station relays ASS and BSS. The station relays may be considered as tape storage Unit Outs. In addition, if movement of the selected stations is to be effected after data have been read out therefrom, the S1 and S2 sequence storage fields must bring about operation of the required move relays MA and MB (Fig. 32*c*). Sequence data also may be selected from dial storage and this requires the selection of a dial storage Group Out.

Fig. 50 shows the form of S1 and S2 pyramids for selecting Group Outs, Unit Outs, and Move relays. Fig. 50 also shows a similar pyramid relating to the "early and late" control subsequently described.

Each of the pyramids in Fig. 50 is diagrammatically shown and consists of an S1 (or S2) tens tree feeding ten S1 (or S2) units trees, respectively. In other words, the ten outlets 0 to 9 (also see Figs. 45 and 45*a*) of each tens tree are connected respectively to the inputs of ten similar units trees. The ten units trees in a pyramid have 100 outlets which are individually wired to 100 plug sockets. The plug sockets connected to the Unit Outs pyramid are designated SUP00 to 99 (also see Fig. 53*a*). The plug sockets associated with the Group Outs pyramid are designated SGP00 to 99 (also see Fig. 53*b*), and the plug sockets connected to the Station Move pyramid are designated SMP00 to 99 (also shown in Fig. 53*b*). Finally, the sockets associated with the "early and late" pyramid are designated SELP (also see Fig. 53*b*). It is clear that each of the hundred sockets 00 to 99 of a pyramid relate to the corresponding code numbers 00 to 99 any of which may be in S1 or S2 fields.

The plug sockets SGP may be variously plugged to the relay storage Group Outs sockets RSGP (see Figs. 47*a* and 53*b*), or tape storage Group Outs sockets GOS (Figs. 32*c* and 53*b*) or to dial storage Group Outs sockets DSPP (Figs. 47*c* and 53*a*). The plugging will be made in accordance with which Group Out is to be operated for a particular S1 or S2 code number. The Group Outs, as now understood, are associated with the Out bus-sets and, therethrough, to the electronic storage units. As previously stated, it may be assumed that the electronic storage units ES7 and ES8 are to be used for receiving S1Seq and S2Seq portions of a line of sequence data. Accordingly, the plugging from sockets SGP will be to sockets for Group Outs 7 and 8. For instance, if S1 code number 01 is to select S1Seq data from a station in tape storage bank 1, then socket 01 of SGP is plugged to socket 7 of the bank 1 set of sockets GOS. If, further, the S2 code number 02 is to select S2Seq data from a station in tape storage bank 1, then socket 02 of SGP is plugged to socket 8 in the bank 1 set of sockets GOS. As another example, if S1 code number 39 is to select S1Seq data from dial storage, then socket SGP39 is plugged to socket DSPP7. As a third example, if S2 code number 75 is to select S2Seq data from relay storage set 9, then socket SGP75 is plugged to socket 9RSGP8; i. e., to socket 9 in the bus 8 group of sockets RSGP.

The sockets SUP of the Unit Outs pyramid (Fig. 50) are selectively plugged to sockets RSUP (Figs. 48 and 53*a*) and sockets ASP and BSP (Figs. 32*c* and 53*a*) according to which Unit Outs are to be selected by the S1 and S2 code numbers. For example, if S1 code number 01 is to select S1Seq data to be read out of station 8 of tape storage bank 1 through the A outlet of this station, the socket SUP01 (Fig. 53*a*) is plugged to socket 8 of the bank 1 set of sockets ASP. If S2 code number 02 is to select S2Seq data to be read out of station 9 of bank 1 through its B outlet, socket SUP02 is plugged to socket 9 of the bank 1 set of sockets BSP. If, as another example, the code number 35 in S1 is to select S1Seq data from relay storage unit 019, which is the first unit in storage set 9 (Fig. 28) then socket SUP35 is plugged to socket RSUP019.

At this point, it may be mentioned that a twin plug jack is used wherever it is required to plug a single socket, such as one of the sockets ASP, to a pair of other sockets, such as a socket SUP and a socket ASPP. It may also be mentioned here that plugging connections are provided between the relay storage pyramids, tape storage pyramids, dial storage pyramid, etc., and the relays respectively controlled thereby to insure a high degree of flexibility in the selection of the relays. For instance, the plugging between sockets TS–GOSP and TS–GOS (Fig. 53*b*) and between ASP and ASPP (Fig. 53*a*) enables the code numbers in the *b* and *r* subfields of an Out field of sequence data to select any of the tape stations in any of the banks 1, 2 and 3. Thus, while code number 6 in subfield *b* and code number 403 in subfields *r* are normally assigned to selection of station 1 relay ASS from bank 1 to be read out to Out bus-set 6, the plugging enables these code numbers to select, for instance, station 2 relay BSS in bank 3, to be read out to Out bus-set 1. Hence, if bank 1 is not in running condition for some reason; then the sequence coding need not be changed but the plugging may be arranged to select a station from another bank.

When the S1 or S2 coding selects a tape station and it is desired to step the station after reading out its data, the sockets SMP of the Station Move Pyramid (Fig. 50) are selectively plugged to sockets MAP and MBP (Figs. 32*c* and 53*b*). Thus, if S1 code number 01 is to select S1Seq data to be read out through an ASS relay of a station in bank 1 and the station tape is to be advanced following the reading out of data, then socket 01 of the group of sockets SMP is plugged to the gang socket MAP of bank 1 (Fig. 53*b*). Consequently, the relay MA of this bank will be energized at the proper time and the move signal receiving means of bank 1 will be effective to cause advance of the selected station in the bank, as described in Section 9.

The Unit Outs, Group Outs, and Station Move Pyramids are heated upon closure of timing contacts X1*a* on the A side and of timing contacts Y1*a* on the B side. X1D and Y1D serve as arc suppression relays.

The "early and late" plugging will be de-

scribed later. It is to be understood that while Fig. 50 shows only four pyramids in the A side and four in the B side, there are actually eight such pyramids in each side, four for the S1 fields of sequence storage and four for the S2 fields of sequence storage in each side. It is to be understood further that the corresponding S1 and S2 pyramids on the A and B sides have common outlet connections to the set of 100 plug sockets associated with these pyramids. For instance, the four S1 and S2 Unit Outs pyramids on the A and B sides have their corresponding outlets connected to the same sockets SUP. As an example, the outlets 99 of these four S1 and S2 Unit Outs pyramids are all wired to socket SUP99 (Figs. 50 and 53*a*).

Relay storage Group-Ins selection.—Fig. 51 shows the A and B sides of the form of selection network for the relay storage Group Ins (also see Figs. 28 and 29). There is one such network for each of the fields Q, R, T, U and V. Each of the circuits except the circuit for the T field connects from ground through parallel contacts *s*8*c* or *s*4*c* to contacts X1*a*. If in the Q, R or U subfield *s*, the code number is higher than 3, then the field is an In field. The V field always is an In field and unless the field is skipped, its subfield *s* will contain a number higher than 3. All numbers higher than 3 include the binary term 4 or 8. Hence a corresponding sequence storage relay *s*4 or *s*8 will be energized if the number in this *s* subfield is higher than 3. The field containing this subfield therefore will be an In field and a circuit connection will be closed from ground through either contacts *s*8*c* or *s*4*c* to the contacts X1*a*. As far as the T field is concerned, its subfield *s* has only the two binary positions 2 and 1 and therefore this subfield *s* cannot designate a digit higher than 3. Previously it was explained that the T field is an In field if the code in the OP2 field is 01. Accordingly, for the T pyramid of the form shown in Fig. 51, the circuit extends from ground to the input of an OP2 tree and from the outlet OP–01 of this tree to the X1*a* contacts.

As stated before, the code numbers for selecting relay storage units are 010 to 159. If any of these code numbers occurs in subfield *r* of an In field, then one of the relay storage Group Ins will be selected depending on the *r* code number and the digit in the adjacent *b* field. The circuit, on the A side, is timed by the closure of contacts X1*a* (see Section 16*b*, item 3). Upon the closure of these contacts a circuit may be established as follows (Fig. 51): From ground, through one of the paths previously mentioned, to the contacts X1*a*, thence via contacts R800*e*, R400*h* and R200*h* to the input of the *b* tree. This tree serves as a feeder for eight *r* units trees. The arrangement is the same as described for relay storage Group Out selection (see Fig. 47*a*) and the units trees shown in Fig. 51 direct the circuit selectively to one of the plug sockets RSIG (also see Fig. 53*c*). There are eighty of these sockets and each is associated with a correspondingly numbered socket RSIGP. Normally the correspondingly numbered sockets RSIG and RSIGP will be plugged to each other and if the circuit is made to one of these sockets RSIG then it is completed through the plugging to the correspondingly numbered socket RSIGP and a gang relay RS–GI (also see Fig. 29) to the +50 v. line. Assume for example that the circuit shown in Fig. 51 relates to the Q field and that the coding in this field is 5 in the subfield *s*, 1 in the subfield *b*, and 010 in the subfield *r*. Upon the closure of contacts X1*a*, a circuit will be established from ground through contacts (Q)*s*4*c* X1*a*, (Q)*r*800*e*, (Q)*r*400*h*, (Q)*r*200*h* to the input of the (Q)*b* tree, thence from the output 1 of this tree to the *r* units tree (1) and to the output 0 of this tree, and by way of the plugging between the sockets 010 of groups RSIG and RSIGP through the gang relay ORS–GI1 to the +50 v. line.

In this manner, when Q is an In field, the code number 1 in the subfield Q*b* and any code number in Q*r* which is under 200 and terminates in the units order digit 0 causes the selection of the Group In 1 associating relay storage set 0 (see Fig. 28) to In bus-set 1.

The A side of the circuit shown in Fig. 51 has been explained. The B side is similar except that the *s* and *r* contacts and *b* and *r* trees are operated by BOP relays instead of by AOP relays and contacts Y1*a* are used in place of the contacts X1*a*. It is to be noted also that contacts X1*a* and Y1*a* are shunted respectively by arc suppressor contacts X1D*a* and Y1D*a*. It is to be understood also that there are five such circuits as shown in Fig. 51, one for each of the fields Q, R, T, U and V and their corresponding outputs are commonly connected to the same sockets RSIG.

Relay storage Units In selection.—Figs. 52*a* and 52*b* show the A and B sides of a Unit In network for selecting the relay storage Unit Ins (also see Figs. 28 and 29). There is one such Unit In network for each of the possible In fields Q, R, T, U and V, and their corresponding outputs are commoned in the manner now understood. Each network provides a path such as described for the relay storage Group In network (Fig. 51) to and through contacts X1*b*, on the A side, and contacts Y1*b* on the B side. As in the Units Out relay selection network (Fig. 48) the Units In network (Figs. 52*a* and *b*) includes two *r* tens trees (0) and (1). The paths from X1*b* to the inputs of these tens trees are such as described for the relay storage Group G In network. The same as in the Unit Out network, the Unit In tens tree (0) feeds nine *r* units trees (1) to (9) and the tens trees (1) in Fig. 52*b* feeds 7 *r* units trees (0) to (6). The outputs of the *r* units trees in the Unit In network are connected to sockets UP010 to 159 (also see Fig. 53*c*). These are pluggable to sockets UPP010 to 159. Sockets UPP are wired to the corresponding Unit In relays. As now understood, code numbers 010 to 159 identify the relay storage units and if any of these code numbers is in the subfield *r* of an In field, the corresponding relays in sequence storage will establish a selection circuit for the identified relay U "in," the circuit being timed by contacts X1*b*, considering the A side or by contacts Y1*b* considering the B side.

For simplicity of explanation, assume the Units In network shown in Figs. 52*a* and 52*b* is the one pertaining to the Q field and that Q*r* contains code number 010 while Q*s* contains code number 9. Considering the A side, a circuit will be made from ground via (Q)*s*8*d*, X1*b*, (Q)*r*800*f*, (Q)*r*400*i*, (Q)*r*200*i*, (Q)*r*100*g*, the (Q)*r* tens tree (0), the (Q)*r* units tree (1), and plugging between sockets UP010, UPP010 and through the Unit In relay U "in" 010 to the +50 v. line. As another example, assume the code number in Q*r* is 123; relay (Q)*r*100 will be energized and open contacts *g* while closing contacts *h*. Ac-

cordingly, the circuit will be detoured to the (Q)r100h line (also see Fig. 52b) so as to heat the (Q)r tens tree (1). The circuit will be completed through this tens tree, the (Q)r units tree (2), plugging between UP123 and UPP123 and through relay U "in" to the +50 v. line.

Code numbers 160, 161, 162 and 163 all call for selection of one of the recording units; specifically Printer 1 (see Section 21). This printer unit may record values selectively taken from relay storage unit 120, 121, 122 or 123 depending on whether the code number is 160, 161, 162 or 163 respectively. In order to provide for selection of the relay storage units 120, 121, 122 and 123 under control of the code numbers 160, 161, 162 and 163, the r tens tree (Fig. 52b) also feeds an r units tree (6). The outputs 0, 1, 2 and 3 of this (6) tree are commoned with outputs 0, 1, 2 and 3 respectively of the r units tree (2). Therefore, the code numbers 160, 161, 162 and 163 will serve the same as code numbers 120, 121, 122 and 123 to bring about the selection of relay storage Unit Ins 120, 121, 122 and 123, respectively. The code numbers 160, 161, 162 and 163 also bring about the selection of the start circuit for Printer 1. This start circuit will be explained later in Section 21.

The table look-up In selection networks.—When any of the code numbers 281 to 286 is in the subfield r of an In field, it calls for a computed argument to be read into the table look-up apparatus (see Fig. 35 and Section 10). This involves the selection of a table look-up Group In and of a Table In. Fig. 51 shows the form of selection circuit for a table look-up Group In while Fig. 52a shows the form of selection circuit for a Table In. The circuit for selecting a table look-up Group In (Fig. 51) starts the same as the circuit for selecting a relay storage Group In but is diverted by contacts r200j to the input of a b tree. The circuit is completed through this tree, plugging between sockets TG and TGP (also see Fig. 53c) and through a Group In relay TLU-GI to the +50 v. line.

The selection circuit for a Table In starts the same as the circuit for a relay storage unit In but detours through contacts r200h, r10b, and r80d, to the input of the r units tree in the Table In selection network. The contacts r200h, r10b and r80d are all closed if the code number in the r subfield lies between 280 and 289 inclusive. The r units tree in the Table In selection circuit has its outputs 1 to 6 connected to plug sockets TLP1 to 6 (also see Fig. 53c). These are plugged to sockets TLPP1 to 6. If the code number is one of the numbers 281 to 286, the circuit will be directed to one of the sockets TLPP and completed via interlock contacts TLDa through a Table In relay TL to the +50 v. line.

The remaining selection circuits controlled by sequence storage will be described in the subsequent sections which deal with operations involving these selection circuits.

12. *The denominational shift unit*

One of the units of the electronic calculating section (Fig. 20) is a denominational shift unit. Its purpose is to shift an amount a chosen number of columns to the right or to the left. The amount to be shifted is sent into the denominational shift unit from the Internal In bus-set and delivered to the Internal Out bus-set. The shift unit has 28 shift columns (Figs. 20 and 25). Each column is alike and one is fully illustrated in Fig. 24. Shift columns 1 to 28 are associated respectively with Internal bus columns 29 to 2. Each column of the denominational shift unit has a set of elements allotted to each binary position. The tubes IT1, IT2, IT4, and IT8 are the input tubes of a shift column and their suppressors are coupled to buses 1, 2, 4, and 8 of a column of the Internal In bus-set. The binary decimal terms of a digit are represented by increased potential selectively present in the buses of an Internal In bus column. Accordingly, tubes IT are selectively conditioned according to these binary decimal terms. Subsequent to conditioning of the tubes IT, a positive entry timing signal SHRI is applied to the control grids of the tubes, rendering the selectively conditioned tubes conductive. The anodes of IT1, 2, 4, and 8 are coupled to terminals c of triggers ASH1, ASH2, ASH4, and ASH8, respectively. When a tube IT becomes conductive, it reverses the corresponding trigger ASH. A cancel signal ACL is applied to points a of all the triggers ASH to reset those which are not being held in turned state by conductive tubes IT. The signal ACL is produced concurrently with signal SHRI but is shorter and has a briefer effect, so that the triggers ASH turned under control of signal SHRI remain turned to store an entry. The turned triggers ASH apply increased potential to correspondingly numbered output lines SHO. As an example, assume the binary decimal terms 4 and 1, representing digit 5, have been applied to a shift column, conditioning tubes IT1 and 4. The entry signal SHRI will render the conditioned tubes IT1 and IT4 conductive, causing them to reverse the triggers ASH1 and ASH4 which thereupon apply increased potential to the output lines SHO1 and SHO4. As indicated diagrammatically, in Fig. 25, the output lines SHO1, SHO2, SHO4, and SHO8 of each shift column, except the end columns 1 and 28, connect to the shift columns at the right and at the left. The connection to the column at the right is to a set of input lines SHR and the connection to the column at the left is to a set of input lines SHL. The lines SHL1, SHL2, SHL4, and SHL8 are coupled to the suppressors of tubes FLS1, FLS2, FLS4, and FLS8, respectively (see Fig. 24). The lines SHR are coupled to the suppressors of a set of tubes FRS. It is seen therefore that increased potentials on output lines SHO of a column are applied to the input lines SHL of the column at the left to condition its tubes FLS selectively. At the same time the increased potentials on the lines SHO are applied to the input lines SHR of the column at the right to condition its tubes FRS. The outputs of tubes FLS1 and FRS1 of a shift column connect to point c of a trigger BSH1. Similarly, FLS2 and FRS2 are connected to BSH2; FLS4 and FRS4 are connected to BSH4; and FLS8 and FRS8 are connected to BSH8.

After the application of the entry signal SHRI to the denominational shift unit, a negative cancel signal BCL is applied to the unit. This signal resets all the triggers BSH, of which there are four for each column. Following the resetting of triggers BSH, either selected one of two positive signals RSH and LSH is applied to the denominational shift unit, depending on whether the shift is to be effected towards the right or towards the left. Assuming that the shift is to be effected towards the right, the signal RSH is applied and renders the conditioned ones of

the tubes FRS conductive. The conductive ones of the tubes reverse the associated triggers BSH. If, instead, the shift is to be effected towards the left, then the signal LSH is applied and causes the conditioned ones of the tubes FLS to conduct so as to reverse the associated triggers BSH. As may be understood now, a digit applied to a shift column is ready to shift to the right and to the left but is permitted to shift only in one direction depending on whether the left or right shift signal is applied to the denominational shift unit. Also, each intermediate shift column has applied to it, in the form of conditioning potential, a digit from the column at its right and another digit from the column at its left. But only one of these digits will be allowed to enter the column. If the shift is to be to the right, then the digit entered into a column comes from the column at the left. If the shift is to be to the left, then the digit entered in a column comes from the column at the right. The shifted digit, from the left or from the right, is manifested by the selective reversals of triggers BSH1, BSH2, BSH4, and BSH8. These triggers temporarily store the shifted digit. After the digit has been shifted into triggers BSH, the triggers ASH of each column are again reset by the signal ACL in preparation for receiving the shifted digit from the triggers BSH of the same column. Reversed triggers BSH condition related tubes SHT. The next signal, after reset of triggers ASH, is a positive signal SHE which renders the conditioned ones of the tubes SHT conductive to reverse the related triggers ASH. In this manner, a digit which has been shifted into a column is entered in its triggers ASH.

Briefly, after the application of the digits of a number from the Internal In bus-set to tubes IT of the shift columns, the triggers ASH are reset by a cancel signal ACL, the first of which is produced under control of the main sequence commutator (Section 16*a*), as will be described fully later. A signal SHRI is then produced under control of the main sequence commutator to cause the conditioned tubes IT to conduct and reverse the related triggers ASH. Triggers ASH in each shift column thereupon apply the digit to the flanking shift columns. The denominational shift unit is now ready to perform one or more successive column shift steps.

The sequence of signals in each shift step is:

1. The cancel signal BCL to cause triggers BSH to be reset, preparing then to receive a shifted digit.

2. The shift signal RSH or alternative shift signal LSH to cause either the right or left shifted digits to be entered in triggers BSH. For a shift to the right, the signal RSH is applied and the digits shift into the columns at the right. For a shift to the left, the signal LSH is applied and the digits shift into the columns at the left.

3. The cancel signal ACL to clear the triggers ASH, of each column, of the digits previously entered therein and now shifted to an adjacent column.

4. The signal SHE to transfer the digit shifted into a column from its triggers BSH to its triggers ASH.

Each above sequence effects a single step of column shift. This same sequence is repeated as many times as the number of steps of column shift to be effected. For instance, if eleven steps of column shift are to take place, then the sequence is repeated eleven times. It will be understood that if the original amount has, say, 28 digits, eleven steps of column shift to the right will drop out the eleven right-hand digits, leaving seventeen of the original digits in positions displaced eleven places to the right of their original places.

After completion of the desired number of steps of column shift, the amount remaining in the denominational shift unit and manifested by the selectively reversed triggers ASH is read out to the Internal Out bus-set. For this, triggers ASH which are in reversed status, condition related output tubes OT8, 4, 2 and 1. A positive read out signal SHRO is applied, after completion of the desired number of shift steps, to the tubes OT to render the conditioned ones of the tubes OT conductive. In this manner, the amount left in the column shift unit is read out in its binary decimal form as decreased potentials selectively applied to the buses 8, 4, 2 and 1 in columns of the Internal Out bus-set.

The number of steps of column shift is determined by the sequence means in a manner which will be explained hereinafter. It is sufficient for the present to state that the column shift amount is represented by increased potentials selectively applied to lines MN1, 2, 4, 8, 10 and 20 (see Fig. 27*a*) of the internal commutator or subsequencing means (Figs. 27*a*, *b* and *c*) of the denominational shift unit. The column shift amount may be referred to as the minuend, for a reason which will become clear. The tens order of the minuend will not exceed 2. The minuend is entered into a descending counter which is, per se, the subject matter of application Serial Number 768,393 of B. E. Phelps, filed August 13, 1947, now Patent 2,500,294 issued March 14, 1950. Briefly, this counter has a complete units order of triggers T1, 2, 4 and 8 (Fig. 27*a*) and a partial tens order comprised of triggers T10 and T20. For each trigger in the counter, there are three tubes which control the application of a binary decimal term of a minuend to the trigger. For instance, trigger T1 has its terminal *c* coupled to the plate of a pentode 5–SCH1 (Fig. 27*a*) and its terminal *f* coupled to the plate of a pentode 7. The control grid of 7 is connected to the plate of a triode 13. The control grids of 5 and 13 are connected to the line MN1. Subsequent to the selective application of increased potentials on the input lines MN, a positive going timing signal Ink is applied to the suppressors of the tubes 5, 7 and the similar tubes relating to the other triggers of the descending counter. Assume, for instance, that line MN1 is at increased potential. Accordingly, the application of a timing signal renders 5 and 13 conductive. Since 13 is conductive, it keeps 7 in a non-conductive condition. Since 5 becomes conductive and 7 remains non-conductive, the trigger T1 is reversed. In this manner a binary digit 1 is applied to the descending counter. Similarly, tubes 9, 11 and 13*a* serve to apply a binary digit 2 to the trigger T2. Tubes 15, 17 and 19 serve to apply a binary digit 4 to the trigger T4. Tubes 15*a*, 21 and 23 serve to apply the binary digit 8 to the trigger T8. Tubes 25, 29 and 31 function to apply binary digit 1 in the tens order to the trigger T10. Finally, the tubes 25*a*, 33 and 35 serve to apply a tens order binary digit 2 to the trigger T20. The tubes 7, 11, 19, 23, 31 and 35 function as blocking tubes to prevent reversal of the associated triggers if a binary digit is not to be applied to these triggers. For instance, if the amount to be entered does not con-

tain the binary digit 4 in the units order, the tubes 15 and 17 remain non-conductive. With 15 non-conductive, it conditions 19. Accordingly, the timing signal Ink will render 19 conductive to block reversal of trigger T4. Such blocking action is necessitated by the interconnections between the triggers. At this point it may also be stated that when the units order of the counter is at 0, the line ZU is at increased potential and renders a tube 2a conductive to block the reversal of trigger T2. Such blocking action must be inhibited during the application of a minuend to the counter, inasmuch as such minuend may include the binary digit 2 in the units order. For this reason, a triode 16 has its plate coupled to the line ZU and its control grid connected to the line upon which the signal Ink is applied. This signal will render 16 conductive so as to insure the presence, at the time, of a decreased potential upon the line ZU. The tube 2a will thus become non-conductive and will be ineffective to block reversal of trigger 2 during the application of the minuend to the descending counter.

For each step of column shift, the descending counter will be driven one step in a descending count sense. The stepping of the counter is effected by negative entry pulses coming from a tube 2 which is operated in a manner described hereinafter. Each entry pulse is applied to the both sides of the trigger T1 in the units order. Hence, the trigger will be shifted in response to each entry pulse. In further explanation, assume that the minuend 17 has been applied to the descending counter. Hence, triggers T1, 2, 4 and 10 are in reversed states prior to the application of entry pulses to the counter. The first entry pulse returns trigger T1, leaving 6 standing in the units order. The second entry pulse reverses trigger T1 which thereupon applies a negative pulse to both sides of trigger T2 causing it to return to the shown status. Since triggers T1 and T4 are now in reversed status, the units order stands at 5. The third pulse returns trigger T1, leaving 4 in the units order. The fourth pulse again reverses trigger T1 causing it to effect reversal of trigger T2. As T2 reverses, it applies a negative pulse to opposite sides of trigger T4, returning it to shown status. Since triggers T1 and T2 are now in reversed status the units order stands at 3. The fifth pulse returns trigger T1 leaving the units order at 2. The sixth pulse again reverses trigger T1 which causes trigger T2 to return. Since trigger T1 now is the only reversed trigger in the units order, the units order stands at 1. The seventh pulse restores trigger T1 and the units order then stands at 0. It is seen that the application of seven entry pulses has stepped the units order descendingly from its initial "7" status to its "0" status. With the units order in 0 status, the tubes 8a, 12a, 20a and 24a are all held non-conductive by the related triggers 1, 2, 4 and 8. Accordingly, the common output line ZU of these tubes is at increased potential. The increased potential on line ZU is applied to the suppressor of a tube 14, to the control grid of a tube 28, and to the grid of the tube 2a. In response to the increased potential, tube 2a becomes conductive to block trigger T2. The eighth entry pulse applied to the descending counter reverses trigger T1. Inasmuch as trigger T2 is now blocked, the reversal of trigger T1 is ineffective to reverse trigger T2. As the trigger T1 reverses, it acts through a suitable coupling capacitor to apply a positive going impulse to the control grid of the now conditioned tube 14. This tube accordingly becomes conductive and reverses trigger T8. The triggers T1 and T8 are now in reversed status, so that the units order stands at 9. In other words, the units order, when at 0, is stepped by the next entry pulse to 9, as is required of a descending counter. It is further required that upon the units order being stepped from 0 to 9, a subtractive carry of 1 be effected into the tens order. Trigger T8 reverses only when the units order steps from 0 to 9. Upon its reversal, trigger T8 applies a negative pulse to both sides of trigger T10, causing it to shift in status. Since the trigger T10, in the assumed example, was previously in reversed status, this carry pulse from trigger T8 causes the trigger T10 to return to the shown status. Since both triggers T10 and T20 of the tens order are now in reset status, the tens order stands at 0. The related tubes 32a and 36a are then non-conductive and their common anode line ZT is at increased potential which is impressed on the suppressor of 28. The descending counter now stands at 9, having been stepped descendingly from its initial "17" status to its "9" status in response to 8 successive entry pulses. The ninth entry pulse returns trigger T1 and the counter then stands at 8. The tenth entry pulse turns trigger T1 causing it to turn trigger T2. As trigger T2 turns, it reverses trigger T4. Upon reversal of trigger T4, it resets trigger T8. Thus, the triggers T1, 2 and 4 are now in reversed status, so that the counter stands at 7. It is seen that ten entry pulses have effected a descending value cycle of the units order from its initial "7" status back to a "7" status. Also, during this value cycle, as the units order stepped from 0 to 9, it effected a subtractive carry of 1 from the tens order. In a manner now clear, seven more entry pulses will bring the units order to "0" status. Thereupon, line ZU goes to high potential, which is impressed on the control grid of the tube 28, previously conditioned by the line ZT under control of the tens order in "0" status. The tube 28 thus becomes conductive when the descending counter is at zero and applies decreased potential to tube 16a, causing output line F to rise in potential. This brings about termination of column shifting, in a manner described hereinafter.

The operation of the descending counter has been explained above. The minuend, which is the column shift amount, is applied to tubes in the descending counter prior to the application of the positive entry signal Ink. This entry signal comes from the plate of a tube 5–SHC2 (Fig. 27b). The main sequence means operates at the proper time to apply a negative signal Ink to the grid of tube 5 which thereupon produces the positive Ink signal, as a result of which the column shift amount is entered into the triggers of the descending counter.

The direction of shift is determined by the program means, in a manner explained later (Section 17, Item 11). If the shift is to be to the left, increased potential is present on line LT (Fig. 27c), but if the shift is to be to the right, then increased potential is present on line RT. Increased potential on line LT conditions 9–SHC3 (Fig. 27c), while increased potential on line RT conditions 17. Subsequently, the positive signal Ink renders the conditioned one of the tubes 9 and 17 conductive. If 9 is conductive, it turns 21 to the left (its terminal c goes to low potential) and if 17 is conductive, it turns 21 to the

right (its terminal *f* goes to low potential). If **21** is in its left status, it cuts off **25***a*, which is a condition to production of the left shift signal LSH at the proper times. If **21** is in right status, it cuts off **25** which is a condition to production of the right shift signal RSH.

The column shift means has its own oscillator and amplifier source (Fig. 27*b*) of 50 kc. pulses A and B which are 180 degrees out of phase with each other.

After entry of the column shift amount into the descending counter, main sequence produces a negative signal SHCL (see Section 17, Item 22) which cuts off **21**–SHC**2**. Tube **21** thereupon applies a positive signal SHCL to the standard, SHC cancel circuit (Fig. 27*c* and Section 3*b*). The output of the cancel circuit resets those triggers (except the triggers in the descending counter) in the internal commutator of the denominational shift means which are marked with the reset status symbol *x*. The triggers in the descending counter (Fig. 27*a*) are in shown states when the counter is at zero. This counter is reset to zero by the column shifting operation, to be described. The counter also may be reset to zero from the Control Desk.

The positive signal SHCL is also applied to the grids of **38** and **36** in Fig. 27*c*. In response, **38** cuts off **38***a*, to turn **39**, which then applies, through a capacitor, a positive impulse to **36***a* which, in turn, through a capacitor, cuts off **40**. Tube **40** then causes P**40** to produce the negative cancel signal ACL which, as explained before, is impressed on all the triggers ASH of the shift columns (Figs. 24 and 25). The positive signal SHCL is of short (one AP pulse cycle) duration. When this signal terminates, **36** and **38** become non-conductive. As **36** becomes non-conductive, it resets trigger **39**. It is clear that the first cancel signal ACL for the shift columns is produced under control of signal SHCL.

Concurrently with signal SHCL, main sequence produces the negative signal SHRI, which cuts off **25***a*, Fig. 27*b*. Tube **25***a* then renders a tube **25** conductive to cause a power amplifier P**25** to produce the positive going entry SHRI signal which, as previously described, is applied to the shift columns to effect the entry of the number from the Internal In bus-set into the shift columns (see Figs. 24 and 25).

The apparatus is now ready for column shifting the number which has been read into the shift columns. The column shift is initiated by a negative start signal SHS produced by the sequence means at the termination of the SHRI read-in or entry signal. This SHS signal has a chance time relation to the 50 kc. A and B pulses continually produced by the SHC oscillator and amplifier (Fig. 27b). Fig. 26 is a timing chart of pertinent operations which follow upon the occurrence of the SHS signal and based on the example of a column shift amount of 3 entered into the descending counter (Fig. 27*a*).

The negative start signal SHS goes to the control grid of the normally conductive tube **5**–SHC**3** (Fig. 27*c*) and also to the terminal *g* of a trigger **6**. This signal cuts off **5**, forcing **6** to reverse. The signal is of short duration and at its termination, the line carrying the signal returns to high potential and thereby restores **6**. Meanwhile, upon reversal of **6**, it reversed **11** (also see Fig. 26). The time of reversal of **11** is an indication of the time of occurrence of the start signal SHS. Upon reversal of **11**, it conditions **12**, Fig. 27*c*, to become conductive in response to the next B+ pulse, thereby to reverse **15**. Reversed **15** cuts off **14***a*. At present, **31***a* also is cut off, so **31***a*—**14***a* is effective to condition **35** to respond to the next A+ pulse. This next pulse causes **35** to apply, through a capacitor, a negative pulse to **34** cutting it off, which makes P**34** conductive to produce the negative BCL signal. As previously described, this is the first signal in the sequence of four signals occurring in each shift step. BCL resets triggers BSH of each shift column (see Fig. 24), as previously described, preparing them to receive a right or left shifted digit. When **15** was reversed at the B+ time to cause the BCL signal to appear at the next A+ time, it also conditioned **16**, Fig. 27*c*, to respond to A+ pulses. The negative pulses produced by **16** are applied to both sides of **20** to alternate its status. The first A+ pulse turns **20** which thereupon cuts off **23***a* to condition **22** to become conductive with the next B+ pulse. When **22** becomes conductive, it cuts off **26** and **26***a*. As explained before, if a right shift has been called for by the main sequence means, trigger **21** is in right-shifted position and cuts off **25**. But, if a left shift has been called for, then **21** is in left-shifted condition and cuts off **25***a*. Accordingly, when **26** and **26***a* are now cut off under control of **22**, either **26**—**25** or **26***a*—**25***a* becomes fully cut off, depending on whether a right or left shift is to be performed. If **26**—**25** is cut off, it works through **33** and P**33** to produce the positive RSH signal while if **26***a*—**25***a* is effective, it operates through **29** and P**29** to produce the positive LSH signal. As previously described, the signal RSH or LSH respectively cause the right or left shifted digits to be entered in triggers BSH of the shift columns.

When **22**, Fig. 27*c*, became conductive at the first B+ time in the 1st shift step, it caused the shift signal LSH or RSH to be produced, as just explained. It also reversed **19** which, in turn, reversed **18**. With **19** reversed it cuts off **28** to make **31***a* conductive so that **31***a*—**14***a* will be ineffective and the next A+ pulse will not cause a BCL cancel signal to appear. Instead, the ACL cancel signal will be produced. This results from **28** conditioning **32** to respond to the next A+ pulse. Thereupon, **32** applies, through a capacitor, a negative pulse to **40** as a result of which P**40** produces the negative ACL signal. This signal, the third in the sequence of four signals appearing in each shift step, resets triggers ASH of each shift column (see Fig. 24), preparing these triggers to receive the shifted digits now stored in triggers BSH. It may be noted that the first ACL signal was produced in consequence of the application of the signal SHCL from the main sequence means, as previously described. The next and successive ACL signals are produced by the internal timer of the column shift means in the manner just described.

At the A+ time at which the ACL signal is produced, **16**, Fig. 27*c*, responds to an A+ pulse and restores **20**. Thereupon **20** cuts off **31** and **23**. As **31** is cut off, it produces a positive pulse which is transmitted via line C to tube **2**–SHC**1**. In response to this pulse, tube **2**–SHC**1** produces a negative entry pulse which steps the descending counter to diminish the count by 1. As the descending counter in the assumed example started at 3, it is now stepped to a count of 2 (see Fig. 26). In this manner the descending counter is operated in each shift step to reduce the count by 1.

The first three signals in the 1st shift step have

been produced in the manner just explained. These first three signals are BCL at the A+ time in the shift step, LSH or RSH at the succeeding B+ time, and ACL at the following A+ time. The fourth and final signal in the sequence for each shift step is the SHE signal which is produced at the B+ time following the ACL signal. The SHE signal will cause the shifted digits to be transferred from triggers BSH to ASH. It was explained above that 20–SHC3 was restored by the second A+ pulse in the shift step and thereupon cut off the tubes 31 and 23. The tube 31 thereupon caused the descending counter to diminish the count by 1. The tube 23 when cut off conditions 24 to become conductive with the next B+ pulse. When 24 becomes conductive it cuts off 27. Tube 27*a* has already been cut off by the previously mentioned reversal of trigger 18 (also see Fig. 26) which will not be restored until the end of the last shift step. Accordingly, when 24 cuts off 27, the couple 27—27*a* is effective to make 30 conductive and thereupon cause P30 to produce the SHE signal. This signal as previously stated causes the shifted digit to be transferred from triggers BSH of each shift column to triggers ASH of the same shift column. This completes one shift step.

The same sequence of signals BCL, LSH or RSH, ACL and SHE, along with a step of descent of the descending counter to 1, is repeated in the 2nd shift step. The 3rd shift step takes place in which this same sequence of signals is again produced and half way in this 3rd shift step the descending counter is stepped to 0. As previously described, when the descending counter is at 0, the tube 16*a*–SHC1 applies increased potential to the line F. The increased potential on this line renders 8*a*–SHC3 conductive to restore 11. With 11 restored, it conditions 10 to operate in response to the next B+ pulse to restore 15. With 15 restored, it conditions 13 to become conductive with the next A+ pulse and thereupon to restore 18. It will be noted that 18 is restored at the termination of the SHE signal in the last shift step. All the triggers 11, 15, 20, 19 and 18 are now in reset status and shift steps are terminated.

In the foregoing manner, when the column shift amount is 3, three shift steps are produced. Similarly, any other number of required column shift steps are performed, the number of such steps being given by the column shift number applied to the descending counter.

At the termination of the steps of column shift, the shifted number in the denominational shift unit (Fig. 25) is to be read out upon the Internal Out bus-set. As already explained, 18–SHC3 (Fig. 27*c*) was restored at the end of the last shift step. As 18 restores, it applies a negative going pulse to 14, causing 14 to apply a positive going pulse by way of a line 14*w* (also see Fig. 27*b*) and a capacitor to the control grid of the normally conditioned tube 39–SHC2. Accordingly, 39 becomes conductive and turns the trigger 40. As 40 turns, it makes 36 conduct to produce a negative going shift complete signal SHCP. This signal is utilized by the main sequence, in a manner explained later, to apply a negative read out signal SHRO to 32–SHC2, cutting it off. Thereupon, 35*a* becomes conductive and restores 40. Also 35 becomes conductive and acts through P35 to produce a positive going SHRO signal. As described before, this SHRO positive signal causes the number stored in the triggers ASH of the shift columns to be applied to the buses of the Internal Out bus-set (see Figs. 24 and 25).

When the colmun shift amount is 0, and a number is entered from the Internal In bus-set to the denominational shift unit, it will be read out of this unit to the Internal Out bus-set with no column shift. In the event that the denominational shift amount is 0, the descending counter (Fig. 27*a*) maintains line F at increased potential to condition a tube 7–SHC3. Then, when the start signal SHS turns trigger 6, the trigger applies a positive pulse through a capacitor to the conditioned tube 7 to render it conductive. The output of this tube is applied via a wire 7*w* and the anode resistor of 39–SHC2 to the trigger 40, turning the trigger. The effect of this is to cause the shift complete signal SHCP to be produced in the manner explained before. Consequently, the read out signal SHRO will be produced, causing the number read into the denominational shift unit to be read out without a column shift.

Shift columns are numbered here to correspond to orders of an amount whereas storage and bus columns are numbered inversely to orders.

Amounts will be entered in the shift unit only from calculator units, as will be clear from Sections 17, 18, and 19. The shift columns 28 to 1 will apply an amount to Internal bus columns 2 to 29 but as only bus columns 11 to 29 are connected to electronic storage (columns 2 to 20 thereof), it is evident that only the amount in shift columns 19 to 1 will be sent to electronic storage from where it goes to relay storage. A shift to the right or to the left therefore discards from the amount in shift columns 19 to 1 the given number of right or left-hand places, so that the shifted number in these columns is the one which ultimately is received by electronic and relay storage. It is understood, therefore, that in speaking of the reading out of a shifted amount from electronic storage, reference is made to the shifted amount in shift columns 19 to 1.

As an example, assume a 28-place number in shift columns 28 to 1. A shift to the right of 10 places brings the 28th place of the original number into shift column 18 and the 11th place of the original number into shift column 1. The shifted amount to be read out is therefore the result of discarding the 10 right-hand places of the original number. If the 28-place number in shift columns 28 to 1 is shifted 10 places to the left, the 1st place of the original number moves to shift column 11 and the 18th place of the original number moves to shift column 28. The shift columns 11 to 19 then contain nine orders of the original amount and it is these nine orders which constitute the shifted number to be read into storage. This shifted number is the result of discarding the 10 left-hand places of the amount originally in shift columns 19 to 1.

13. *The electronic accumulator unit*

This is an arithmetical unit of the electronic computing section (see Fig. 20). When accumulation is called for, the accumulator unit will receive numbers successively in binary decimal form from the buses of the Internal In bus columns 11 to 29. Along with each number, the Internal In bus-set will apply to the accumulator unit the sign of the number. As now understood, a + sign is represented by increased potential on bus 2 and a — sign is represented by increased potential on bus 1 of column 1.

The accumulator unit may perform simple accumulation of positive and negative numbers.

means are also provided for rounding off a desired order of the result in the accumulator. Main sequence will contain a column shift number, obtained from the program means, which will determine the extent of denominational shift of the accumulated result when this result is read out of the accumulator unit to a receiving unit. The selected number of steps of column shift of the result; i. e. the extent of denominational shift of the result will be effected through the column shift means described in section 12. As there explained, column shifting may be to the right or to the left. When column shifting is to the left, then rounding off will not be desired. When column shifting is to the right, then rounding off is useful and will occur unless suppressed by main sequence. The column shift number set in main sequence will select the ultimate units order of the column-shifted result and thereby will select the order to be rounded off.

The accumulator may also perform a special accumulation operation called the tolerance check which will be explained later.

Associated with the accumulator unit is a so-called internal commutator (Figs. 71*b* to 71*g*) which subsequences all the operations of the accumulator upon reception of certain signals from main sequence. All of these signals come from the accumulator control commutator ACC.C (Fig. 78A) except for a tolerance check signal, a rounding off or half correction suppression signal and two reset signals, HCR and CTLR (Fig. 71*g*) which come from other parts of main sequence. With the exception of a few triggers in the internal commutator, the triggers in this commutator are reset as an initial operation by the manually controlled cancel signals mentioned in Section 3*b* after which each sequence of normal accumulation returns these triggers to canceled status. Certain triggers in the commutator cannot be reset readily in the normal accumulation sequence, due to timing conditions and special requirements, so that for these triggers the two reset signals HCS and CTLR are provided.

The internal commutator has its own oscillator and amplifier source (Fig. 71*c*) of 50 kc. A and B pulses, 180 degrees out of phase with each other.

The accumulator unit has 29 orders, of which the 29th is a result sign evaluating order. The Internal In bus columns 2 to 29 are connected respectively to entry means for accumulator orders 28 to 1 (see Figs. 20 and 70). However, in the present case, only the bus columns 11 to 29 may carry significant digits and since it is only these columns which receive digits from electronic storage (Section 6). These bus columns 29 to 11, respectively, are associated with accumulator orders 1 to 19, respectively. With regard to orders 20 to 28, they will in effect receive 0 entries from the bus columns 2 to 10. The Internal In bus column 1 which carries the algebraic sign of the number to be entered in the accumulator is connected into a sign mixing circuit included in Fig. 71*a*. The outputs of orders 1 to 28 are connected respectively to the Internal Out bus columns 29 to 2, and the output of the 29th order is connected to the Internal Out bus column 1 to apply the result sign to this column. Orders 1 to 28 each include a digit indexing or entry receiving device or register EC (Figs. 20, 69*a*, 69*b* and 70) and an accumulating device or register RC. The sign registering order, the 29th, does not include an entry register EC but includes a register RC. The devices EC and RC are each constructed as a register order such as shown in Figs. 15 and 15*a*.

In general, the operation will consist in entering the number from the Internal In bus-set into the entry registers EC and thereafter transmitting the numbers from EC to the corresponding orders of the accumulating registers RC. The registers RC comprise the accumulating means per se and are denominationally associated by carry means. Both positive and negative numbers may be accumulated and an algebraic sum obtained. All numbers are represented on the buses in true, binary decimal form and their negative or positive sense designated by the accompanying sign, 1 for the — sign and 2 for the + sign. For each number entry, the program means provides an operational sign. Whether the accumulating unit is to act upon a number as a negative or a positive number is dependent not only upon the sign of the number but also upon the operational sign. The sign of a number and the operational sign are applied to the sign mixing circuit network (Fig. 71*a*) of the accumulator unit. The operational sign may be 0 or 1 or 2 or 3, as previously explained in Section 2*a*. If the operational sign is 0, this means that the number is to be treated by the accumulator unit as having a + sign, regardless of its original sign. If the operational sign is 1, then the original sign of the number will be inverted and the accumulator unit will treat the number according to the inverted sign. If the operational sign is 2, then the accumulator unit will act on the number according to its original sign. Finally, if the operational sign is 3, then the accumulator unit will treat the number as having a — sign regardless of its original sign. The mixed sign produced by the mixing network also may be referred to as the operating sign. If the operating sign is +, then the number in registers EC will be transferred in true form to the registers RC.

But if the operating sign is —, then the tens complement of the number in EC will be read out therefrom to the registers RC.

The accumulator unit will be called in for operation by main sequence acting through an accumulation calculation commutator ACC.C (Fig. 78A). This commutator will produce cancel signals ECC and RCC (Figs. 71*e* and *f*) for cancelling the registers EC and RC, respectively, prior to entry of the first number into the accumulator unit. An entry signal ACC–RI will be produced by the commutator ACC.C concurrently with the cancel signals but will be prolonged past the cancel signals. This entry signal will cause the number on the Internal In bus-set to be entered into registers EC. The entry signal also will cause the number sign in column 1 of the Internal In bus-set and the operational sign to be entered into the sign mixing circuit (Fig. 71*a*). After the entry of the number and signs, the commutator ACC.C produces a start signal ACC–ST (see Fig. 71*c*) which calls into operation the internal commutator (Figs. 71*a* to 71*g*) of the accumulator unit. The internal commutator will then function to initiate an accumulator cycle (Fig. 72) during which, under control of the operating sign, the number or its complement will be transferred from EC to RC. At the end of the accumulator cycle, the internal commutator will send a complete signal CYCPT (Fig. 71*g*) back to the com-

mutator ACC.C. The latter will then signal main sequence to apply a new number and its sign to the Internal In bus-set. Also main sequence will apply a new operational sign to the sign mixing circuit. The commutator ACC.C again will send out an ECC cancel signal but this time the RCC cancel signal will be suppressed in the manner explained later in Section 17. The entry signal will be applied again, causing entry of the new number into EC. A second start signal is applied to the internal commutator of the accumulator unit to bring about the accumulation of the second and first numbers. When the accumulation of the desired number of successive amounts has been completed, the commutator ACC.C sends out a result read-out signal R.ROC (Fig. 71*g*) to the internal commutator. In response to this signal the internal commutator tests the 29th order RC of the accumulator for 0 or 9. If the highest order is at 0, it is an indication that the algebraic sum in the accumulator is a true, positive number. If the highest order RC is at 9, it is an indication that the algebraic sum is a complement; i. e., a negative number. If the test finds that the highest order RC contains 9, a complement conversion cycle is effected under control of the internal commutator. During this conversion cycle the complement in registers RC is read out upon the Internal Out bus-set and through the power amplifier P. A. (Fig. 20), explained before in Section 1, to the Internal In bus-set. The internal commutator also proceeds during the conversion cycle to cause the registers EC to be cancelled and then to cause the complement on the Internal In bus-set to be entered into EC. Upon the completion of this entry, the registers RC are cancelled. The fact that a complement conversion cycle has been initiated forces the sign control portion of the circuit to be set up for a complement transfer operation from EC to RC. The internal commutator will then produce a start signal which will cause the complement of the complement in EC to be transferred to RC. The registers RC will therefore contain the true figures of the negative number accumulated by the accumulator unit. Upon completion of the transfer from EC to RC, a Proceed signal is sent to the commutator ACC.C by the internal commutator. The internal commutator also produces a read-out signal as a result of which the number standing in RC and the sign of the number will be read out upon the Internal Out bus-set.

If a 0 is sensed in the highest order RC register after accumulation, a complement conversion cycle will not be effected and the read out signal will be produced by the internal commutator to cause a positive number and its sign to be read out from RC, and a Proceed signal will be sent out at the same time to ACC.C.

Fig. 69*a* shows the 1st or units order of the accumulator; Fig. 69*b* shows the 2nd order; and Fig. 71*b* shows the 29th, sign evaluating, order. The 2nd to the 28th orders are alike and differ from the 1st order in that the 1st order omits the tubes required for carry-through-9 purposes which are not necessary in the 1st order. Also, the 1st order includes elusive one entry means. The 29th order, as stated before, does not contain an entry receiving register EC but only a register RC.

The carry means.—The carry means includes a trigger K for each order of RC except the 29th or sign registering order. The carry means will be described in detail with regard to the 1st and 2nd orders shown in Figs. 69*a* and *b*. When an order of RC steps from 9 to 0 during the entry period, which may be taken as 0.5 to 9.5 of an accumulator cycle (Fig. 72), it produces a positive carry out pulse at the terminal *c* of stage **8**. This pulse is effective to render a triode KV conductive. The triode thereupon reverses the trigger K associated with the order of RC which has advanced from 9 to or through 0. For instance, assuming that the 1st order of RC has stepped from 9 to 0, the trigger **K1** will be in reversed state. Carry-through-9 means are provided for the intermediate orders. By this means, when such order is at 9 and the preceding order effects a carry, the carry will be instantaneously applied not only to the first higher order but also to the second higher order, and so on. Considering, for instance, the 2nd order (Fig. 69*b*), when it stands at 9, its stages **1** and **8** are in reversed status. With stage **1** in reversed status, its terminal *c* is at reduced potential. Likewise the terminal *c* of stage **8** is at reduced potential. The reduced potential at *c* of stage **1** is applied to a tube **65**, cutting it off. Likewise, the decreased potential at *c* of stage **8** is applied to a tube **65***a* having its anode commoned with the anode of the previously mentioned tube **65**. Assume for instance that order 1 (Fig. 69*a*) has stepped from 9 to 0 so that trigger **K1** is reversed and that order 2 stand at 9 at the end of the entry period, so that the tubes **65** and **65***a* related to order 2 are cut off. Further, with **K1** reversed, it is effective via wire **18B–A** to cut off tube **65***b* (Fig. 69*b*) which has its anode commoned with the anodes of **65** and **65***a* associated with the 19th order. A fourth tube **65***c* has its anode commoned with the anodes of the tubes **65**, **65***a* and **65***b* associated with the 2nd order RC. The tubes **65***c* associated with all the orders of RC are cut off except for a short period 11.5 to 13 of an accumulator cycle (Fig. 72) for a reason stated later in the present section. Accordingly, in the example where the 1st order RC has stepped from 9 to 0 during an entry period, **K1** is reversed and has cut off **65***b* associated with the 2nd order. Further, as the 2nd order has been assumed to stand at 9, the tubes **65** and **65***a* associated with the 2nd order are also cut off. As the tube **65***c* also is cut off until 11.5 of the accumulator cycle, the lock group of four tubes, **65**, **65***a*, **65***b* and **65***c* for the 2nd order are all cut off. It is clear that **65***c* is initially cut off during the entry period and remains so until after the entry period. Further, the tube **65***b* may be brought to non-conductive condition at any point of the entry period at which the preceding order, the 1st order, goes from 9 through 0. When the 2nd order stands at 8, the tube **65***a* goes to cut off and when this order steps to 9 the tube **65** also goes to cut off. It is evident then that either **65** or **65***b* will be the last one of the group of four tubes in the 2nd order, to be rendered nonconductive. Upon this tube being rendered nonconductive, the common anode potential of the group of four tubes rises and renders a tube **65***d* conductive, thereby reversing the connected trigger **K2**. This reversal will occur at any mid index point time of the entry period 0.5 to 9.5 of a cycle (Fig. 72). If, in this same entry period, the 3rd order is at 9 or advances to 9, then the reversal of **K2** (2nd order) will cut off **65***b* in the 3rd order group of lock tubes **65**, **65***a*, **65***b* and **65***c*, and thereupon the trigger K in

the 3rd order will reverse. This chain of events may continue through any number of higher orders at 9.

It is seen then, that by the end of the entry period, reversal will have been effected of all those triggers K associated either with RC orders which have stepped from 9 through 0, or associated with a succession of orders of which the lowest has stepped from 9 through 0 and the higher ones are at 9.

When a trigger K is reversed, it conditions a related tube KT. In the example the tubes KT1 and KT2 are conditioned. At the 12 point of the cycle, a positive carry operating pulse C–OP is applied commonly, along wire 17A–B (see also Fig. 70) to all the tubes KT. Any conditioned one of these tubes will become conductive and apply a negative going impulse along a wire 19B–A and through the anode resistor circuit of a tube 16 associated with the next higher order RC to the input of this next higher order RC. Thus, a carry entry will be made into this next higher order.

In this manner, an instantaneous carry is effected into all orders of RC following orders which have stepped from 9 to 0 or following one or more orders which are at 9 at the end of the entry period and are in turn preceded by an order which has stepped from 9 to 0.

As stated before, the tube 65c in each order of the carry means above the 1st order cuts off except between 11.5 and 13 of the cycle. This prevents a carry-through-9 of an order if the order has been advanced to 9 during the carry entry period. For instance, if the 2nd order had not been at 9 before the carry period, but instead had been at 8 and were advanced to 9 by a carry entry from the 1st order, it would cut off the tubes 65 and 65*a* during the carry period. The tube 65*b* will also be at cut-off under control of the trigger K1 in the 1st order. If the tube 65c were not present or if this tube were not conductive during the carry period, then the common anode line of the lock group of tubes in the 2nd order would be at increased potential and would operate through 65*d* to reverse K2. Consequently, the carry operating pulse would be effective to produce an undesired carry entry into the 3rd order. By providing the tube 65*c* and rendering it conductive for a period starting before and ending after the carry period, such misoperation is prevented.

Assuming that accumulation has been called for, the commutator ACC.C (Fig. 78*A*) is conditioned for operation. Assume further that the first of a plurality of numbers is to be entered in the accumulator, and that half correction is to be suppressed. Fig. 73 is a timing chart relating to the accumulator procedures when half correction is suppressed. A negative half correction suppression signal HCS is produced by main sequence, as will be explained in item 11, Section 17. This signal is applied to 1, Fig. 71*g*, which acts via 1*a* to turn 5. Thereafter, the commutator ACC.C concurrently sends out the negative signals ECC, RCC, and ACC–RI. The ECC signal functions through 20 and 12 in Fig. 71*e* to produce an amplified signal ECC. The latter signal is inverted by 1, Fig. 71*a* to a positive signal which is applied to the EC cancel circuit. The RCC signal functions via 33 and 34 in Fig. 71*f* to produce the amplified signal RCC. This is inverted by 2, Fig. 71*a* for operating the RC cancel circuit. Either cancel signal ECC or RCC also cuts off a tube 33 to make it apply a positive signal to the carry triggers cancel circuit KC. Each of these cancel circuits is of the type shown in Figs. 16 and 17. The output of the EC cancel circuit goes to the EC registers (Figs. 69*a* and *b* and 70), and resets them. The output of the RC cancel circuit resets the RC registers (also see Fig. 71*b*). The output of the KC circuit resets the carry triggers K.

As mentioned before, for the second and successive number entries, the RCC cancel signal will not be produced. The ECC signal will be produced, however, each time an entry is to be made and will always bring the KC cancel circuit into operation along with the EC cancel circuit.

Prior to the production of the cancel signals and the entry signal, ACC–RI, the number to be entered in the accumulator will be present on the buses of the Internal In bus columns 2 to 29, of which columns 2 to 10 will always contain zeros, and the sign of the number will be present in Internal In bus column 1. The digit in each Internal bus column is represented, as now understood, by increased potential selectively present on buses 1, 2, 4 and 8 of the column. The buses 1, 2, 4 and 8 of each column are coupled to the suppressors of entry tubes ECE1, 2, 4 and 8 respectively of the related accumulator order. It is to be noted that the bus columns 2 to 29 are thus respectively associated with accumulator orders 28 to 1. The tubes ECE of the accumulator orders will therefore be selectively conditioned according to the binary terms in the decimal notation digits of the number on the Internal In bus columns 2 to 29. The negative ACC–RI signal produced by the commutator ACC.C, along with the cancel signals ECC and RCC or along with the cancel signal ECC only, functions via 35 and 36 in Fig. 71*e* to produce an amplified signal ACC–RI. This is inverted by an amplifier (Fig. 70) to a positive signal which is applied via line 1A–1B to the control grids of all the ECE tubes. Thereby, the conditioned ones of the ECE tubes are rendered conductive. The outputs of the tubes ECE1, 2, 4 and 8 of an accumulator order are coupled to points *c* of the trigger stages 1, 2, 4 and 8 of the register EC in the order. Hence, as soon as the cancel signal ECC terminates, the conductive ones of the tubes EC reverse the related trigger stages of the EC register. In this manner the number on the Internal In busset is applied to the entry registers EC.

The entry signal ACC–RI also causes the number sign and an operational sign to be entered in the sign mixing circuit which is shown in Fig. 71*a*. Buses 1 and 2 of Internal In bus column 1, which carries the number sign, are respectively connected to the suppressors of tubes 8 and 7 in Fig. 71*a*. The operational sign 1 is represented by an increased potential signal OPSN1, the operating sign 2 is represented by the increased potential signal OPSN2. These signals respectively condition tubes 6 and 5. It can be seen that the tubes 5, 6, 7 and 8 will be selectively conditioned according to the number sign and the operational sign. The amplified negative read-in signal from Fig. 71*e* also is applied to the sign mixing network where it is inverted by a tube P20 to a positive signal which is applied to the control grids of the tubes 5, 6, 7 and 8. Accordingly, any of these tubes which has been conditioned by increased suppressor potential will be rendered conductive by the positive read-in signal. Tubes 5, 6, 7 and 8 are coupled to the triggers 13, 14, 15 and 16, respectively in such man-

ner that when any of these tubes is rendered conductive, it reverses the associated trigger. If the operational sign is 2, trigger 13 will be reversed. If the operational sign is 1, trigger 14 will be reversed; if the operational sign is 3, triggers 13 and 14 will be reversed; if the operational sign is 0, triggers 13 and 14 will remain in cancelled status. If the number sign is +, then the trigger 15 will be reversed and if the number sign is —, then the trigger 16 will be reversed.

The various examples of number and operational signs are given below:

Example 1.—Assume the number sign is + and the operational sign is 2. Accordingly, the triggers 13 and 15 will be reversed. With 13 and 15 reversed, 21 is rendered conductive. As 21 is conductive, it cuts off 31 and 31 thereupon conditions the suppressor of 39. With 14 in normal state, it cuts off 30 which accordingly conditions the control grid of 39. As both the suppressor and control grids of 39 are conditioned by increased potentials, 39 becomes conductive and cuts off 37. With 37 cut off, it conditions the suppressor grid of 4. The positive read-in signal ACC–RI which is applied to the control grids of 5, 6, 7, and 8 to render any of these conditioned tubes conductive, also is applied to the control grid of tube 40*a* making this tube conductive so as to render 4 and 12 non-conductive until the termination of the read-in signal. When this read-in signal terminates, 40*a* again becomes non-conductive and applies increased potential to the control grids of 4 and 12. In the present example, the suppressor grid of 4 has been conditioned. Accordingly, when 40*a* becomes non-conductive, 4 becomes conductive and cuts off the power tube 36 which thereupon applies increased potential to the output line 2*sn* to serve as a representation of the + operating sign. The line 1*sn* remains at decreased potential so as not to manifest the — operating sign. In the present example this result is obtained as follows: With 14 in normal status it is cutting off 22, 23 and 30. With 16 in normal status it is cutting off 24. As 23 is cut off it conditions the control grid of 32. Also, 24 being cut off conditions the suppressor of 32. Hence 32 conducts and cuts off 40 to apply conditioning potential to the suppressor of 38. Since 30 has been cut off it is applying conditioning potential to the control grid of 38. Therefore, 38 is conductive and deconditioning 12. The latter thereby remains non-conductive and sustains the power tube 28 in conductive condition so that its output, the line 1*sn*, remains at low potential.

Example 2.—Assume the number sign is + and the operational sign is 1. This operational sign is to cause the inversion of the number sign. Accordingly, the mixing network for this example should produce the — operating sign. It is understood now, with the signs assumed for this example, the triggers 14 and 15 are reversed. With 14 reversed, it cuts off 29 which thereupon conditions the control grid of 37. With 13 in normal status it cuts off 21 which thereupon conditions the control grid of 31. Trigger 16 remaining in normal status cuts off 22 so as to condition the suppressor of 31. Hence 31 is conductive and cuts off 39 to apply conditioning potential to the suppressor of 37. Since 29 is applying conditioning potential to the control grid of 37, the latter becomes conductive and deconditions 4 with the result that the output line 2*sn* will remain at ineffective, low potential. 14 and 15 being in reversed status, render 23 conductive so that 23 cuts off 32. Since 32 is cut off, it makes 40 conduct whereby 38 is cut off. As 38 is cut off it conditions the suppressor of 12. At the termination of the read-in signal the control grid of 12 is conditioned and 12 becomes conductive so as to operate through 28 to produce the increased potential on line 1*sn*, representing the — operating sign.

Example 3.—Assume the number sign is — and the operational sign is 2. Accordingly, triggers 13 and 16 will be reversed. Reversed trigger 13 cuts off 29 to condition the control grid of 37. 14 in normal status cuts off 22, 23, and 30. 15 in normal status cuts off 21. With both 21 and 22 cut off, 31 is receiving increased suppressor and control grid potentials and is conductive, thereby cutting off 39. Accordingly, 39 conditions the suppressor of 37. Also, 29 being cut off, conditions the control grid of 37. Hence, 37 is conductive and 4 is deconditioned so that the tube 36 will remain conductive and the + operating sign, line 2*sn*, will remain at ineffective low potential. With 13 and 16 reversed, 24 is conductive cutting off 32 which through 40 cuts off 38. Accordingly, 12 is conditioned to operate upon the termination of the ACC–RI pulse so as to cause 28 to produce the effective increased potential of the — operating sign, line 1*sn*.

Example 4.—Assume the number sign is — and the operational sign is 1. Accordingly, triggers 14 and 16 will be reversed. 13, in normal status cuts off 30 so as to condition the control grids of 38 and 39. Trigger 15 in normal status cuts off 23 so as to condition the control grid of 32. 13, in normal status cuts off 24 so as to condition the suppressor of 32. Accordingly, 32 is conductive and cuts off 40 to condition the suppressor of 38. Since the control grid of 38 is also conditioned, it becomes conductive so that the — operating sign will not be read out. Since 14 and 16 are both reversed, in this example, 22 is conductive thereby cutting off 31. As 31 is cut off it applies conditioning potential to the suppressor of 39 which is also at increased control grid potential. Hence, 39 becomes conductive and cuts off 37, with the result that the line 2*sn* will be at high potential at the termination of the read-in signal as now understood.

It is seen from the above examples that when the operational sign is 2, then the operating sign is the same as the normal sign, but, when the operational sign is 1, then the operating sign is the reverse of the number sign.

Example 5.—Assume the operational sign is 0. Accordingly, 13 and 14 will remain in cancelled status. With 13 and 14 in this status, 29 is conductive and cutting off 37. Hence, at the termination of the read-in signal ACC–RI 4 will be rendered conductive and 36 non-conductive to produce the effective increased potential on the line 2*sn*, such potential manifesting a + operating sign. It will be noted that with 13 in cancelled status, it cuts off 30 to condition the control grid of 38. Also 14 in cancelled status cuts off 23 conditioning the control grid of 32. 24 is also cut off by 13 and conditions the suppressor of 32. Accordingly, 32 will conduct and through 40 will condition the suppressor of 38. Since the control grid of 38 also has been conditioned, 38 conducts so that 12 will not be conditioned and the — operating sign 1*sn* will remain at ineffective low potential.

It is seen from this example that when the operational sign is 0, a + operating sign will be read out, regardless of the number signs.

Example 6.—Assume the operational sign is 3. Accordingly, **13** and **14** are both reversed, causing **30** to become conductive. With **30** in conductive status it cuts off **38** and **39**. **39** thereupon conditions the suppressor of **37**. With **13** and **14** in reversed status, **29** is cut off conditioning the control grid of **37**. Hence **37** is conductive while **38** has been cut off. Under this condition, as now understood, the line **2***sn* will be at ineffective potential while the line **1***sn* will be at effective potential for representing the — operating sign.

It is seen from this example that when the operational sign is 3, the operating sign will be — regardless of the number sign.

As explained above, the + and — operating signs for a number entry into the accumulator are represented by increased potential selectively present on lines **1***sn* and **2***sn* (Fig. 71*a*), respectively. The conditions of these lines will be unchanged until a new number entry is made. Lines **1***sn* and **2***sn* connect to the internal commutator of the accumulator and according to which of the lines is at high potential the internal commutator will control means for transferring either the true number or its complement from registers EC to RC. Specifically, high potential on line **1***sn* or **2***sn* renders **17** or **17***a* in Fig. 71*b* conductive to set a sign storing trigger **21** in — or + sign storing state, respectively. The + state is the shown state while the — state is the reverse state of **21**. Depending on whether **21** is in — or + state, it cuts off **22** or **22***a*, respectively. If **22** is cut off it acts via **33**, Fig. 71*b*, to hold a line *neg* at low potential which is inverted by an amplifier (Fig. 70) to increased potential on the line **5A–5B**. If **22***a* (Fig. 71*b*) is cut off, it acts via **29** to hold a line *pos* at low potential which via an amplifier (Fig. 70) provides increased potential on the line **6A–6B**. Line **5A–5B** connects to the suppressors of pairs of tubes **9** and **13** (see Figs. 69*a* and *b*) of which there is a pair in each of the accumulator orders 1 to 29 (also see Fig. 71*b*). Line **6A–6B** connects to the suppressors of pairs of tubes **10** and **14**, each of accumulator orders 1 to 28 including one pair of these tubes. Thus, depending on whether the operating sign is — or +, the tubes **9** and **13** or **10** and **14** in the accumulator orders will be conditioned. With **9** and **13** conditioned, the complement of the number in EC will be transferred during an ensuing accumulator cycle (Fig. 72) to RC, but with **10** and **14** conditioned, the true number will be transferred during the accumulator cycle from EC to RC.

The accumulator cycle is initiated under control of a negative start signal ACC–ST produced by the commutator ACC.C (Fig. 78A) one AP pulse cycle after the entry signal ACC–RI (see Section 17, item 15*b*). This start signal will take effect, however, only if a proper determination of an operating sign has been made. Assuming that the + operating sign is being manifested, then **17***a*, Fig. 71*b*, is conductive and in addition to insuring that sign storing trigger **21** is in + state (the shown state), cuts off **30** and **34***a*. If, instead, the — operating sign is manifested, tube **17** is conductive and besides establishing trigger **21** in — state, also cuts off **30** and **34**. With **30** cut off, it acts via **31** to cut off **35**. Thus, if either or both operating signs are manifested, then **35** will be cut off, but if neither operating sign is manifested, **30** will be conductive and through **31** will maintain **35** conductive. If either operating sign alone is manifested, then either **34** or **34***a*, but not both, will be cut off, and the output of **34**—**34***a* will remain at low potential so as to cut off **35***a*. If, by misoperation, both operating signs are manifested, then both **34** and **34***a* will be cut off and **35***a* will be conductive. From the foregoing, it is evident that the couple **35**—**35***a* will be cut off only if a proper operating sign determination has been made.

Assuming couple **35**—**35***a* has been cut off, it acts through **36**, Fig. 71*b*, to place terminal SNI at reduced potential. Low potential on terminal SNI cuts off **21**, Fig. 71*c*, to condition the suppressor of start control tube **35**. Upon termination of the entry signal ACC–RI, the negative start signal ACC–ST is produced, as previously stated. This signal cuts off **36***a* to condition the control grid of tube **35**. Hence, if a proper operating sign determination has been made, the start signal causes **35** to become conductive. **35** thereupon acts via **36** and **18** to reverse start trigger **15**. Reversed trigger **15** conditions **10** to be made conductive by the next B+ pulse and thereupon to reverse **16**. With **16** reversed, it serves via **18***a* to condition **20** to respond to A+ pulses. The output of **20** is effective via **28***a*, **31** and **32** to cause negative pulses, in phase with the A+ pulses, to appear on line *Ctr–In*. This is the common input line for the accumulator timer (Fig. 71*d*). The fourteen stages of the accumulator timer are designated **T0** to **T13** and perform a complete ring of operation in response to fourteen input pulses at A+ timing. The accumulator timer, acting through associated tubes, sequences operations of the accumulator unit during the 14-point accumulator cycle (Fig. 72). It is evident that the first input pulse turns **T13** which reverses stage **T0**. The succeeding input pulse resets **T0** to cause **T1** to be reversed, and so on. The stages **T0** to **T12** are thus reversed, each for a cycle point, at the "0," "1" . . . "11" and "12" times of the cycle, while **T13** is turned at "0" and reset at "13," completing the ring operation of the timer.

During the accumulator cycle, a series of ten positive pulses BEP (see Fig. 72) is applied at the mid-index times "0.5," "1.5" . . . "8.5" and "9.5" to the line **9A–9B** connected to the control grid of the tube **16** in each accumulator order (see Figs. 69*a*, *b* and 70). These pulses BEP are inverted by **16**, if the latter has been conditioned by increased suppressor potential, to negative entry pulses applied to the input of the stages **1**, **2**, **4** and **8** of the register order RC. Also, during the accumulator cycle, ten positive pulses ARP are applied to line **4A–4B** connected to a tube **12** in each of orders 1 to 28. These pulses ARP occur at the cycle points "1," "2" . . . "9" and "10." Tube **12** inverts the applied positive pulses to negative entry pulses on the input of the stages of the register order EC. As previously explained in Section 5, ten pulses applied to a register order effect a value cycle thereof. A number of pulses equal to the tens complement of the digit standing in EC advances it from 9 to 0, causing stage **8** to produce a positive carry-out pulse at its terminal *c*. Assuming that the true number is being transferred from EC to RC, then the pair of tubes **10** and **14** in each of orders 1 to 28 have previously been conditioned, as explained. The carry-out pulse from an EC order is applied through a suitable coupling capacitor **8C** to the control grid of **10**. With **10** conditioned, the carry-out pulse renders it conductive to reverse the trigger **15** (T/C). Hence, when a true number is being read out, this trigger will have been

reversed at a cycle point designated by the number which is the tens complement of the digit initially in EC. For instance, if the EC order initially stood at 4 (see Fig. 72), trigger 15 will be reversed at the "6" point of the accumulator cycle. Also, when the true number is being transferred, 14 in each of orders 1 to 28 has also been previously conditioned. At the "10.5" time of the cycle, a pulse is applied via line 7A–7B to the control grid of 14, causing it to become conductive so as to return trigger 15 to its initial state. During the interval in which trigger 15 was reversed, it acted through 19 to condition 16 to respond to the pulses BEP. The number of these pulses passed through 16 to the input of RC will be equal, when the true number is being transferred, to the digit initially in EC. Thus, in the assumed example, where EC is initially at 4, trigger 15 is in reversed state from "6" to "10.5" of the accumulator cycle and during this interval, tube 16 will produce four negative entry pulses in phase with the BEP pulses. These four pulses will enter digit 4 into the register order RC.

Assuming instead that the complement of a number in EC is to be transferred to RC, the tubes 13 and 9 in each order have previously been conditioned. With regard to the 1st or units order (Fig. 69*a*) a positive "0" pulse is applied, via line 10A, to the control grid of 13 causing it, if conditioned, to become conductive. 13 thereupon acts through the anode resistor of 10 to reverse 15. The carry pulse from the EC order is effective through the capacitor 8C to render 9 conductive, if conditioned. Upon 9 becoming conductive, it restores 15. It is clear that as far as the units order is concerned, the trigger 15 will be in reversed state from "0" of the accumulator cycle to a point of the cycle corresponding to the tens complement of the digit in the register order EC. During this interval, 15, acting through 19 will have conditioned 16 to pass the BEP pulses to register RC, thus entering the tens complement of the digit initially in EC into RC. As an example, assume the units order EC initially stands at 4 (see Fig. 72). Trigger 15 in the units order therefore will be in reversed state from "0" to "6" of the cycle. During this interval, 16 in the units order will pass six BEP pulses to register RC, entering 6 therein. With regard to the orders above the first order, a "1" pulse will be applied via line 8A–8B to 13 so that if 13 is conditioned, it will become conductive and reverse 15 at the "1" time of the accumulator cycle. The carry-out pulses from the EC orders act through 9 to restore 15 at the point of the cycle corresponding to the tens complement of the digit initially in EC. Thus, the trigger 15, of each order above the first, will be in reversed state for a number of cycle points equal to the nines complement of the digit initially in EC. As an example, if EC in the second order initially stands at 4 (see Fig. 72) then the related trigger 15 will be in reversed state from "1" to "6" of the cycle. During this interval, 16 will be conditioned and will pass through five pulses BEP to the input of the related register order RC. In this manner the nines complement of the digit in EC of the second order will be transferred to the corresponding order of register RC. The entry of the tens complement of the units order digit into RC and the entries of the nine complements of the digits in the other orders has the effect of transferring the tens complement of the number in EC to RC.

Each time a complement is entered into the accumulator, 9 must be entered in the 29th order (Fig. 71*b*) as a negative sign manifestation. As previously explained, during complement entry the line 5A–5B is at increased potential conditioning the tubes 13 and 9 in all the orders, including the 29th order. The "1" pulse applied to line 8A–8B also is transmitted to 13 in the 29th order rendering it conductive to reverse the trigger 15 (T/C) in the 29th order. Upon reversal of this trigger, it applies conditioning potential to the suppressor of the gate tube 16 in the 29th order. The control grid of this tube is connected to the line 9A–9B upon which the pulses BEP are applied in each accumulator cycle. The control grid of 9 in the 29th order is connected to the line 7A–7B upon which a positive pulse is applied at the "10.5" time of the cycle. This pulse will render conditioned 9 in the 29th order conductive to restore the trigger 15 in the 29th order, deconditioning tube 16. Since tube 16 in the 29th order was conditioned from "1" to "10.5" of the cycle, it will pass nine BEP pulses to the input of the register RC of this order, thus entering 9 therein, as a manifestation of a negative sign for the number entered into the registers RC.

To make certain that trigger 15 of the 29th order is in reset status when a true number entry into registers RC is called for, the line 6A–6B (see Figs. 70 and 71*b*) connects to the grid of 11, Fig. 71*b*. This line carries increased potential when a true entry is called for as explained before. This makes 11, Fig. 71*b*, conductive to insure reset of 15 in the 29th order.

It is evident that successive entries of complements will cause the 29th order to produce a 9 representation. This will result from the entry of 9 in the 29th order and the carry from the preceding order manifestly consequent upon the entry of successive complements in the accumulator. If a complement is standing in registers RC and a positive entry is made therein which is algebraically greater than the complement, then the registers RC will produce a representation of a true balance. As is well known, when the accumulator goes from a complement balance to a true balance, carry is always effected into the highest, sign representing order, which is the 29th order in this case. This carry will add 1 to the 9 previously in the 29th order RC, so that this order will then stand at 0, signifying a true balance. A negative going carry pulse, produced in the manner described before by the 28th order is transmitted from its output terminal 19B to the input terminal 19A of the 29th order. The pulse is inverted by 26*a* and 32 in Fig. 71*b* to a negative pulse which is applied via the anode resistor of the gate tube 16 in this order to the 29th order register RC, thereby entering 1 therein.

The production of the various pulses required in the accumulator cycle is controlled by the accumulator timer, as previously stated. When stage T0 (Fig. 71*d*) is reversed at the "0" time of the accumulator cycle, it applies a positive pulse to the control grid of 21 in Fig. 71*d*. At this time of the cycle, trigger 19, Fig. 71*d*, still is in cancelled state and applying conditioning potential to the suppressor of 21. Hence, when T0 applies a positive pulse to the control grid of 21, the latter becomes conductive and produces a negative "0" pulse. This pulse is inverted by 13, Fig. 71*c*, to the positive "0" pulse which as previously described is applied via line 10A to the control grid of 13 in the units order (Figs. 69*a* and 70) of the accumulator unit.

This pulse, as already described, is effective, if 13 is conditioned, to cause the trigger 15 (T/C) to be reversed, so that the tens complement of the digit in the first order of EC may be transferred to the corresponding order of RC. As explained above, 13, Fig. 71c, produced a positive pulse at the "0" point of the accumulator cycle. This pulse, in addition to being applied to the tube 13 in the units order of the accumulator is also applied to tube 9a in Fig. 71c, causing the latter to become conductive and thereupon to reverse 14, Fig. 71c. Reversed 14 conditions the tube 5 to respond to B+ pulses. As 5 was conditioned at "0" the first effective B+ pulse occurs at "0.5." In response to the B+ pulse, 5, when conditioned, acts through 9 and 2 to produce a negative-going BEP pulse. Each such pulse is inverted by an amplifier (Fig. 70) to a positive BEP pulse. At the "9" time of the accumulator cycle, stage T9 (Fig. 71d) is reversed and conditions 12, Fig. 71d, to respond to the next B+ pulse occurring at 9.5. In response to this pulse 12 becomes conductive and reverses trigger 10. Reversed trigger 10 thereupon conditions 5 to become conductive in response to the next A+ pulse at "10." Tube 5 thereupon produces a negative going "10" pulse. This pulse acts through 12 and 7 in Fig. 71c to restore 14. It is clear then that 14, Fig. 71c, is in reversed condition from "0" to "10" of the accumulator cycle. During this interval, 14 conditions 5 to respond to ten B+ pulses and thus to bring about the production of the ten BEP pulses indicated in Fig. 72. When stage T0 (Fig. 71d) is reversed at "0" of the cycle, it also conditions 26 to respond to the next B+ pulse at 0.5. Thereupon 26 becomes conductive and reverses triggers 18 and 19.

Upon reversal of 19, it conditions 17 to respond to the next A+ pulse at "1" of the cycle. Tube 17 therefore produces a negative "1" pulse. This pulse is inverted by 28, Fig. 71c, and again inverted by 17, Fig. 71c, to a negative "1" pulse. The pulse produced by 17, Fig. 71c, is inverted by an amplifier (Fig. 70) to the positive "1" pulse which is applied via line 8A–8B to the tubes 13 in the orders of the accumulator unit above the 1st order. As previously described, this pulse will act through tubes 13, if conditioned, to cause triggers 15 to be reversed at the "1" time in order to initiate transfer of the nines complement of the digits standing in the EC orders 2 to 28 to the related registers RC, and to initiate entry of 9 in the 29th order, as already explained.

As explained in the preceding paragraph, 17, Fig. 71c, produced the negative "1" pulse. The tube 17 also produces at this time a pulse for restoring start trigger 15, Fig. 71c.

The trigger 18, Fig. 71d, is reversed at "0.5" of the cycle, as previously described. The reversed trigger 18 conditions 9 to respond to A pulses, the first effective one occurring at "1" of the cycle. At the "10" point of the cycle, the stage T10 is reversed and conditions 15 to be made conductive by the next B+ pulse at 10.5 so as to restore 18. It is seen that 18 is in reversed state from 0.5 to 10.5 of the cycle. During this interval, 9 produces ten negative ARP pulses. These pulses are applied by way of 12a and 6 in Fig. 71c to an amplifier (Fig. 70) which produces the ten positive ARP pulses indicated in Fig. 72.

Stage T10 (Fig. 71d) is reversed at the "10" time of the cycle and causes 15 to respond to the B+ pulse occurring at 10.5 so as to restore 10 and 18. Further, 15 also produces a negative "10.5" pulse which is applied via 4 and 3 to an amplifier shown in Fig. 70 to produce the positive 10.5 pulse (Fig. 70). This pulse, as previously described, is applied along line 7A–7B to the tubes 14 to cause the tubes, if conditioned for true number transfer, to restore the triggers 15.

As explained before, tubes 65c (see Fig. 69b for example) are rendered conductive between "11.5" and "13" of the cycle to prevent carry through the 9 position of an order if this order was stepped to 9 by a carry. Tubes 65c are controlled by the potential on line 13A–13B. The potential on line 13A–13B is under control of a trigger 11 (Fig. 71d). Prior to "11.5" of the cycle, this trigger is in cancelled state in which it maintains 7 non-conductive. With 7 non-conductive, it produces increased potential on the output terminal C–CTL. This terminal connects to the correspondingly designated terminal in Fig. 70 and the increased potential on the terminal is effective via an amplifier to produce cutoff potential on the line 13A–13B for the tubes 65c. At the "11" time of the cycle, stage T11 (Fig. 71d) is reversed, conditioning 16 for operation at 11.5 by a B+ pulse. Tube 16 thereupon reverses triggers 11 and 8. Reversed trigger 11 now renders 7 conductive causing the amplifier (Fig. 70) to produce increased potential on line 13A–13B thereby rendering the tubes 65c conductive, for the purpose explained above. Trigger 8 was reversed as explained above at "11.5." The reversed trigger 8 thereupon conditions 2, Fig. 71d, and the next A+ pulse at "12" of the cycle renders 2 conductive to produce a negative "12" pulse. This pulse is inverted by 8, Fig. 71c, and 3 to a negative "12" pulse which is inverted by an amplifier, (Fig. 70) to the positive carry operating pulse C–OP on the line 17A–17B.

At the "12" time of the cycle, stage T12 (Fig. 71d) is reversed, conditioning 14 to respond to the B+ pulse at 12.5 and thereupon to restore 8 and to turn 6. Reversed trigger 6 conditions 1, Fig. 71d, to respond to the A+ pulse at 13 of the cycle. Tube 1 thereupon produces a negative "13" pulse. This pulse acts through 8a, Fig 71c, and 4 to produce the negative signal CYCT. This signal will control the production of a cycle complete signal CYCPT in a manner explained subsequently. When 1, Fig. 71d, became conductive at "13" of the cycle, it also restored 11, Fig. 71d, terminating the period of increased potential on the line 13A–13B (see Figs. 69b and 70).

Also, at the "13" time of the cycle, stage T12 (Fig. 71d) is restored, and effects reset of stage T13. Stage T13 thereupon conditions tube 13 to be made conductive by the B+ pulse at 13.5 and thereby to restore trigger 6, under control of which the signal CYCT was produced. Further, when stage T13 is restored, it produces a negative going pulse STC. This pulse is applied to 16, Fig. 71c, restoring it to terminate the production of input pulses for the accumulator timer.

Mention has been made of the production of the negative signal CYCT (see Fig. 71c) at the "13" time of the cycle. This negative signal acts through tubes 2 and 2a in Fig. 71f to reverse trigger 8. Pulses AP are produced by the main pulse generator, as explained in Section 4, at a frequency of 4 kc. The effective AP pulses referred to hereinafter are the negative going AP pulses. After reversal of 8, Fig. 71f, an AP pulse restores this trigger. Upon restoration of the trigger, it turns 7, Fig. 71f. The next AP pulse restores this trigger 7. While in its reversed

state, trigger 7 cuts off 5a to produce a positive signal CPT. This signal renders the normally conditioned tube 15, Fig. 71g, conductive. Tube 15 thereupon produces a negative pulse which acts via 24 and 32 to produce the negative going cycle complete signal CYCPT. This signal goes to the accumulator control commutator ACC.C (Fig. 78A) which reacts in a manner described in Section 17, item 15b, to initiate operation of the main commutator to remove the already entered number and its sign from the Internal bus-sets and to terminate the previous operational sign signal. The main commutator proceeds to apply the next number and sign to the Internal bus-sets and to cause a new operational sign to be applied to the sign-mixing circuit (Fig. 71a), all as described in Section 17, item 17. The commutator ACC.C then proceeds as before to produce the cancel signal ECC for cancelling the registers EC. As previously mentioned the RCC cancel signal will not be produced by commutator ACC.C except as a prelude to the entry of the first number of a succession of numbers. The commutator ACC.C also produces, as before, the signal ACC–RI for causing the entry of the new number now on the Internal bus-sets into registers EC at the termination of the ECC cancel signal. The commutator ACC.C then produces the start signal ACC–ST as a result of which a new accumulator cycle is initiated. During this accumulator cycle, the accumulation of the new number in EC with the number previously entered in RC is effected.

In the foregoing manner, successive numbers may be entered into the accumulator unit. After the last number of the succession of numbers has been entered, main sequence acts through commutator ACC.C to produce a negative control signal R.ROC (see Section 17, item 18). The upper portion of Fig. 73 is a timing chart indicating the important operations when the accumulated result is positive. This signal operates via 36, Fig. 71g, and 36a to reverse 31 which thereby serves as a storage element for storing the fact that a readout control signal has been sent out by main sequence. Reversed trigger 31 acts through 28a to reverse 20.

The next AP pulse restores 20, Fig. 71g. Meanwhile, 20, while in reversed state, initiates a sign test of the result in the accumulator. As explained before, the 29th order will register 0 at the end of a series of number accumulations in the accumulator if the algebraic sum of the numbers is positive. On the other hand, the 29th order will register 9 if the algebraic sum of the series of numbers is a complement, indicating a negative result. The trigger 20, Fig. 71g, when reversed, initiates a test of the 29th order to determine whether it stands at 0 or 9. Reversed 20 serves via 12 to apply increased potential to terminal CK, Fig. 71g, which connects to terminal CK in Fig. 71b. The increased potential on these terminals is applied to the control grids of 13 and 15, Fig. 71b. If the 29th or sign register order of the accumulator is at 0, indicating a positive result, then 13, Fig. 71b, will have been conditioned and will be rendered conductive by the application of increased potential to its control grid. But if the 29th order is at 9, indicating a complement result, then 15, Fig. 71b, will have been conditioned and will be rendered conductive by the increased potential applied to its control grid.

Assume first that 29th order of the accumulator stands at 0. Accordingly, its stages 1, 2, 4 and 8 are in reset status and are cutting off 10a, 10, 9a and 9 respectively. The common output of these tubes therefore is at increased potential which is applied to the suppressor of 13, conditioning it to become conductive when the terminal CK increases in potential. Upon 13 becoming conductive, it acts through 14 and 19 to establish a trigger 20, Fig. 71b, in shown status. In its shown status, 20 conditions the suppressor of RCV2 in Fig. 71b. Subsequently, a result readout signal ACC–RO will be applied to the control grid of RCV2 to make it conduct and apply reduced potential to the + sign bus 2 in column 1 of the Internal Out bus-set. When 13, Fig. 71b, becomes conductive, as described above, as a manifestation during the sign check that the result sign is +, it also serves via 14 to apply increased potential to the terminal O.CK. This increased potential is transmitted to the terminal O.CK, Fig. 71g, connected to the control grid of 7, Fig. 71g. It may be stated now that rounding off or half correction is normally effected. Trigger 5, Fig. 71g, is in shown status if half correction is not suppressed. To insure that this trigger is in shown status before accumulation starts, the main commutator produces a negative signal HCR prior to the start of accumulation, as will be described in Section 17, item 11. The signal acts via 4, Fig. 71g, and 16 to establish 5, Fig. 71g, in shown status unless half correction is called for. The signal HCR also serves via 4 and 16 in Fig. 71g to establish tolerance check storage trigger 22, Fig. 71g, in shown status. If half correction is not to be effected, a negative signal H. C. S. is applied before the run of accumulation starts to the tube 1, Fig. 71g, cutting off this tube. This causes the tube 1a to reverse trigger 5, Fig. 71g. Reversed trigger 5 is effective via 10 to maintain increased conditioning potential on the suppressor of 7, Fig. 71g. Accordingly, when the terminal O.CK is increased in potential as explained before, it renders 7, Fig. 71g, conductive. Upon 7 becoming conductive, it acts through 6a to render 18a conductive. The tube 18 is cut off at this time because 17a is now conductive. This is so because tube 3, Fig. 71f, is cut off except when a complete signal is being transmitted by reversal of trigger 7, Fig. 71f, as previously described. Furthermore, 16, Fig. 71f, is in shown status at this time and also cuts off 3, Fig. 71f. The output line 317 of 3, Fig. 71f, connects to the grid of 17a, Fig. 71g. Accordingly, with 3, Fig. 71f, cut off, 17a, Fig. 71g, is conductive and cutting off 18. 18a normally is cut off and conducts when 6a is cut off as a result of 7 being made to conduct by the increased potential on the terminal O.CK. The output of couple 18—18a thereupon goes down in potential and causes Proceed trigger 19 and Readout trigger 23 to reverse.

Upon reversal of 23, it applies increased potential to the control grid of 27. During this time the negative result readout control signal R.ROC is still holding 36 non-conductive, so that the suppressor of 27 also is at increased potential. Accordingly, 27 becomes conductive upon reversal of 23 and cuts off 30. Previously, 30 was in conductive condition. Its suppressor is connected via wire 2530 to the common output of 25, Fig. 71f, and 32a, Fig. 71e. Tube 32a, Fig. 71e, is normally cut off under control of trigger 27 in its shown state. 25, Fig. 71f, is normally cut off under control of 9, Fig. 71f, in shown state. Therefore, line 2530 and the suppressor of 30, Fig. 71g, are normally at increased potential, as

is the control grid. When 23 is reversed, as explained above, it acts through 27 to cut off 30, causing 35, Fig. 71g, to produce a negative signal ACC–RO. This is inverted by an amplifier in Fig. 70 to produce the ACC–RO positive signal upon line 22A—22B.

It should also be noted that when 27, Fig. 71g, becomes conductive, it reverses the trigger 34, Fig. 71g. The next AP pulse restores 34, causing it to restore the trigger 31 which has been storing the result readout control signal R.ROC.

The signal ACC–RO is applied along line 22A—22B (Figs. 69a, b and 70) to the control grids of the tubes RCV8, 4, 2 and 1. There is a set of these tubes in each order except the 29th (Fig. 71b) which contains only the tubes RCV2 and 1. The suppressors of tubes RCV in each of orders 1 to 28 will be selectively at increased potential under control of reversed, correspondingly numbered stages of the register RC in the order. Accordingly, the application of the positive signal ACC–RO is effective to render the conditioned ones of the tubes RCV conductive, causing them to apply decreased potentials to the connected buses of the Internal Out bus columns. Assume, for instance, that in the first order (Fig. 69a) the digit standing in the register RC is 7, so that stages 1, 2 and 4 are reversed. Hence, the tubes RCV 1, 2 and 4 in the first order are conditioned and become conductive in response to the signal ACC–RO. These conductive tubes apply decreased potentials to the buses 1, 2 and 4 of the Internal Out bus column 29, thereby applying binary digits 1, 2 and 4, equivalent to decimal notation digit 7, to this bus column. The tubes RCV1 and 2 in the 29th order (see Fig. 71b) are selectively conditioned according to the status of trigger 20 which is controlled by the 29th order RC according to whether this order stands at 0 or 9. As described, 20, Fig. 71b, is reversed, if the 29th order is at 0, and conditions RCV2. Accordingly, the ACC–RO signal will cause this tube to conduct, reducing the potential on bus 2, column 1 of the Internal Out bus-set, this serving as an electrical manifestation of a + sign for the result.

In the foregoing manner, a positive algebraic sum and its sign are read out from the accumulator unit.

It was stated before that the Proceed trigger 19, Fig. 71g, was turned upon the occurrence of increased potential on the sign check terminal O.CK. The next AP pulse resets 19. Meanwhile, 19 cuts off 14a, Fig. 71g. The output of this tube is coupled with the outputs of two tubes 11 and 11a. Unless a tolerance check operation is being effected, the trigger 22 remains in shown state and is effective via 24a to maintain 11a at cutoff. The trigger 11, Fig. 71f, is in shown state and blocking tube 10, Fig. 71f. This tube therefore renders 4a, Fig. 71f, conductive to apply cutoff potential via wire 411 to tube 11, Fig. 71g. Accordingly, under the stated conditions when the Proceed trigger 19, Fig. 71g, is reversed, cutting off 4a, the common output of 14a, 11 and 11a rises in potential and is effective via 26 to send out a negative Proceed signal to the accumulator control commutator ACC.C (Fig. 78A). In a manner explained subsequently in Section 17, Item 18, this Proceed signal, after a delay equal to the duration of three AP pulses, causes termination of the result readout control signal R.ROC.

The mentioned delay insures ample time for completion of the readout operation before the main sequence means is allowed to call in the next operation.

At the termination of the signal R.ROC, 36, Fig. 71g, is effective to restore 23, Fig. 71g. After the result has been read out, the main commutator produces a positive signal CTLR, in a manner explained later in Section 17, Item 19. This signal acts through 19a, Fig. 71b, to insure that 20 is in shown state and acts through 27 to insure 23 being in shown state, before the start of the next accumulation run.

The reading out of a positive result from the accumulator has been described. Assume instead that the result number is a complement as manifested by the presence of 9 in the 29th order RC (Fig. 71b). The lower portion of Fig. 73 is a timing chart indicating the timing of the important operations which follow the sensing of a complement in the accumulator. As will be made clear, as a result of sensing a complement, a series of events are initiated which are entirely under the control of the internal commutator of the accumulator unit and include the reading out of the complement from registers RC, the entry of this complement into registers EC and a complement transfer of the complement in EC to RC. Such transfer results in RC containing the true digits of the negative result of the accumulation. The internal commutator then proceeds to cause the true digits of the negative result to be read out of RC along with a negative sign.

After the final accumulating cycle of a run of accumulation, the commutator ACC.C (Fig. 78A) produces the R.ROC signal, as in the case of a positive result. This signal reverses 31, Fig. 71g, to cause the reversal of 20, Fig. 71g. Reversed trigger 20 acts through 12, Fig. 71g, to apply increased potential to the terminal CK, Fig. 71g, connected to CK, Fig. 71b, such increased potential producing the sign test of the 29th order for 0 or 9, as previously described.

Assuming that 9 is in the 29th order, its stages 8 and 1 are in reversed state and cutting off tubes 12 and 12a, thereby conditioning tube 15. The increased potential applied to terminal CK, Fig. 71b, therefore makes 15 conduct. Upon 15 conducting it reverses 20, Fig. 71b. The reversal of 20 effects the reversal of 23 which thereby stores the fact that a negative result sign has been sensed. With 20, Fig. 71b, reversed, it conditions the tube RCV1 so that subsequently a readout signal ACC–RO will be effective to make this tube conduct and apply reduced potential to bus 1 of Internal Out bus column 1, thereby representing a — sign. When 15 became conductive it also operated through 16 to apply increased potential to the line 9CK. This causes 5, Fig. 71f, to conduct and thereby reverse 6, Fig. 71f, and 9, Fig. 71f. When 9 turns, it causes 4 to conduct and apply a negative pulse via the anode resistor of 17 to the trigger 13, reversing this trigger. The next AP pulse restores 13, causing 14 and 18 to be reversed. The following AP pulse restores 14 which thereupon causes 15 to be reversed. The next AP pulse restores 15 so as to cause 9 and 18 to be reset. Upon restoration of 18, it turns trigger 19 for one AP pulse time.

While 9, Fig. 71f, is in its reversed state, it makes 25, Fig. 71f, conduct. The anode line 2530 of 25 is connected to the anode of 32a, Fig. 71e, which is normally at cutoff. Accordingly, when trigger 9, Fig. 71f, is turned and renders 25, Fig.

71f, conductive, it applies a negative signal to the normally conductive tube 30, Fig. 71g, cutting off this tube. Hence, 35 conducts and sends out the negative readout signal ACC–RO, which is inverted by an amplifier (Fig. 70) to the positive ACC–RO signal on the line 22A—22B. Consequently, the tens complement result in orders 1 to 28 of the registers RC is read out upon the Internal Out buses 29 to 2. Also, the ACC–RO signal renders the conditioned tube RCV1, Fig. 71b, conductive so as to apply the negative sign signal to bus 4 in column 1 of the Internal Out bus-set. The number and sign on the Internal Out bus-set are transmitted through the amplifier (Fig. 20) to the Internal In bus-set and thereby applied to the entry tubes ECE (Figs. 69a and b). When the trigger 14, Fig. 71f, is turned (also see Fig. 73) it makes 17a conduct, causing its output lines 1720 to drop in potential so as to cut off 20, Fig. 71e, whereupon 20 acts through 12 to apply the negative ECC cancel signal to the tube 1, Fig. 71a. As a result, the EC registers and the carry triggers K (see Figs. 69a and b) are reset.

When trigger 18, Fig. 71f, is turned (also see Fig. 73), it makes 22 conduct, whereupon its output line 2235 drops in potential so that 35, Fig. 71e, is cut off. As a result, 36 becomes conductive and produces the negative signal ACC–RI which is inverted by an amplifier (Fig. 70) to the positive signal ACC–RI on the line 1A—1B. The trigger 14, Fig. 71f, is restored one AP pulse before the restoration of 18, Fig. 71f, so that the EC cancel signal terminates while the read-in signal is still effective. As a result, the complement now on the Internal In bus-set is entered into registers EC.

During the turned interval of 19, Fig. 71f (also see Fig. 73) it conditions the control grid of 21. As 9, Fig. 71f, has now been restored, it cuts off 4 so as to apply increased potential to the suppressor of 21. Accordingly, 21 is now conductive under control of the restored trigger 9 and the turned trigger 19 and produces a negative RCC cancel signal which is transmitted by 33 and 34 to 2, Fig. 71a, and causes registers RC to be reset.

Upon the restoration of trigger 19, Fig. 71f, it turns 24, Fig. 71f. As a result, increased potential is applied to the control grid of 1, Fig. 71f, causing this normally conditioned tube to produce a negative output pulse which cuts off 29, Fig. 71f. Tube 29 thereupon applies a positive pulse to the line CC18. This pulse renders 18, Fig. 71b, conductive thereby establishing the trigger 21 in reversed, minus sign state. In this reversed state, trigger 21 is effective through 22 and 33 to apply decreased potential to the line *neg.* This decreased potential is inverted by an amplifier (Fig. 70) to increased potential on line 5A—5B, as a result of which the tubes 9 and 13 in registers EC (Figs. 69a and b) are conditioned for controlling complement entry into registers RC.

The trigger 24, Fig. 71f, is restored by the next AP pulse following its reversal. Upon its restoration, 24 turns 16, Fig. 71f. Trigger 16 thereupon applies increased potential via line 1613 to the tube 13, Fig. 71g, rendering it conductive. The companion tube 13a is normally off under control of 21, Fig. 71g, so that when 13 becomes conductive a negative going signal is produced on the output of 13—13a. This negative signal is inverted by 2, Fig. 71g, to a positive signal CC–ST which goes to 19, Fig. 71c, and renders the latter conductive. Consequently, the start trigger 15, Fig. 71c, is reversed. Reversal of this trigger causes an accumulator cycle to occur, in the manner already explained. During this accumulator cycle, which is, in effect, a conversion cycle, a tens complement transfer is effected from EC to RC. Since the tens complement of the negative result has been entered in EC, a tens complement transfer of this result to RC brings the true digits of the negative result into RC.

As before, the accumulator cycle complete signal CYCT is produced and turns 8, Fig. 71f. This results in restoring 6, Fig. 71f. Upon restoration of 6, it turns 11 which thereupon applies increased potential to the control grid of 10. However, the tube 10 remains non-conductive because trigger 23, Fig. 71b, has been reversed previously and is acting through 31a, Fig. 71b, to maintain decreased potential on the terminal RS23. This terminal connects to the correspondingly numbered terminal in Fig. 71f and therefore the suppressor of 10 is maintained at decreased potential so that 10 remains non-conductive. With 10 non-conductive, it maintains 4a, Fig. 71f, conductive, so that its output 411 is at low potential and the tube 11, Fig. 71g, is cut off. The tube 11a is now also maintained non-conductive because of the trigger 22 holding the tube 24a conductive. Both 11 and 11a must be maintained at cutoff in order to allow a Proceed signal to be emitted when the Proceed trigger 19, Fig. 71g, is subsequently turned. It will be recalled that the Proceed trigger as well as the readout control trigger 23, Fig. 71g, are turned under control of an O.CK signal when a positive balance is sensed in the accumulator, as previously described. When a negative balance is sensed, then the conversion cycle takes place as explained in detail above and the Proceed signal will be produced after the conversion cycle. It has been explained that trigger 8, Fig. 71f, was turned under control of the accumulator cycle complete signal CYCT. Trigger 8, Fig. 71f, is restored by the next AP pulse following its reversal and upon its restoration it turns 7, Fig. 71f. The trigger 16, Fig. 71f, is still in reversed status and is applying conditioning potential to the suppressor of 3, Fig. 71f. Upon trigger 7 turning, it applies increased potential to the control grid of this now conditioned tube 3. Accordingly, tube 3 becomes conductive and is effective via wire 317 to cut off 17a, Fig. 71g. Tube 17, Fig. 71g, is normally at cut-off, as previously explained. Accordingly, when 17a is cut off, a positive pulse is applied by the output of 17—17a to 18, causing the latter to conduct and to reverse the Proceed trigger 19 and the readout control trigger 23. When trigger 19 reverses, it cuts off 14a. Since 11 and 11a also have been cut off, as already described, the common output of 14, 11 and 11a applies increased potential to 26, causing the latter to emit the negative going Proceed signal which is directed to the commutator ACC.C (Fig. 78A) and causes the next sequence step to occur, as will be described in Section 17, item 18. The reversal of the readout control triggr 23, Fig. 71g, results in the reading out of the true negative result and the — sign now in registers RC, in a manner explained before in connection with the reading out of a positive result.

The next AP pulse following the reversal of 7, Fig. 71f, restores it and upon its restoration it restores 16, Fig. 71f. The trigger 11, Fig. 71f, is restored under control of the next, positive CTLR signal produced by the main commutator, as described in Section 17, item 19, in preparation for the next run of accumulation. The positive sig-

nal CTLR, from the main commutator, is inverted by 3, Fig. 71g, to a negative signal CTLR which restores 11, Fig. 71f.

It is to be noted that if, in the complement conversion cycle, a carry is effected to the 29th order (Fig. 71b), this order will advance from 9 to 0. Such occurrence is an indication of a misoperation or that the capacity of the accumulator has been exceeded. The carry pulse to the 29th order is applied to its terminal 19A and not only operates through 26a, 32, and the anode resistor of 16 to produce the carry entry into the 29th order RC but also is effective to restore the trigger 23, Fig. 71b, to its cancelled position. The trigger 23 in this position is operative through 31a to apply increased potential to the line RS23. This increased potential acts on the suppressor of 10, Fig. 71f. Subsequently, when trigger 11, Fig. 71f, reverses under control of the cycle complete signal CYCT, it applies increased potential to the control grid of 10, Fig. 71f. Accordingly. this tube becomes conductive and acts through 4a and its output line 411 to render 11, Fig. 71g, conductive. Hence when the proceed trigger 19, Fig. 71g, is subsequently reversed to cut off 14a, the conductive tube 11 prevents the common anode line of 14, 11, and 11a from rising in potential so that the Proceed signal is not produced. The result in the accumulator is read out, however, in the manner described before but the main sequence means receives no Proceed signal and the machine operation is interrupted as an indication of misoperation.

The main sequence means may call for a tolerance check operation, in a manner described in Section 17c. This is an operation for checking the accuracy of a computation. For instance, a computation may be effected in one way and the result stored. The same computation may then be effected in a different way and its result stored. The two computation results may then be sent to the accumulator one as a negative and the other as a positive number so that the accumulator will obtain the difference if any between the two computation results. This difference is then read out of the accumulator and reentered therein as a negative absolute number. The main sequence means then selects the source for a tolerance number which has been set up in storage. This tolerance number is the allowable difference between the results of two computations of a particular type. This tolerance number is entered into the accumulator as a positive number. It is apparent that if the tolerance number is equal to or greater than the actual difference obtained between the two computations performed in different manners, that the computation results are within the tolerance. On the other hand, if the tolerance number is less than the difference between the two computations, then the computation results are not within the tolerance. In other words, if the 29th order of the accumulator is at 0 at the end of the accumulation of the tolerance number and the difference between the two computation results, then the computations are within the tolerance, but if the 29th order of the accumulator stands at 9 at the end of the accumulation, then the computation results are not within the tolerance. Prior to the tolerance check accumulation, main sequence applies a negative tolerance check signal ToL.Ck to the tube 6a, Fig. 71g. This signal cuts off the tube. As a result tube 14 is made conductive so as to reverse the tolerance check trigger 22, Fig. 71g. With this trigger reversed, it is cutting off 24a so as to tend to render the interlock tube 11a conductive. If tolerance check accumulation ends with a 0 in the 29th order of the accumulator, then the O.CK signal produced by the sign test of the 29th order is effective through 7, Fig. 71g, and 6a to render 18a conductive so as to reverse the Proceed trigger 19, Fig. 71g, and the readout control trigger 23. Since a complement conversion cycle has not been effected, the trigger 11, Fig. 71f, remains in shown status and renders 23 conductive. The output 2324 of 23, Fig. 71f, is commoned with the output of 24a, Fig. 71g. Hence, even though the tolerance check trigger 22 has reversed and cut off 24a, the common output 2324 of 23, Fig. 71f, and 24a, Fig. 71g, does not rise in potential because 23, Fig. 71f, remains conductive. Accordingly, 11a, Fig. 71g, stays in cut-off condition and does not interfere with the production of a Proceed signal to main sequence.

If the tolerance check accumulation cycle ends with a 9 in the 29th order of the accumulator, a complement conversion cycle takes place in the same manner as explained before in connection with Fig. 73. After the completion of the conversion cycle, trigger 11, Fig. 71f, is reversed. Consequently the tube 23, Fig. 71f, is cut off and since 24a, Fig. 71g, also is cut off, the output 2324 of these tubes is at high potential so tube 11a, Fig. 71g, becomes conductive and blocks the production of a Proceed signal. This is an indication that the computations are not within the desired tolerance.

The description of accumulation thus far has considered half correction of the result as suppressed. When the program calls for a desired receiving unit to receive the result, it also calls for a desired column shift of the result into the receiving unit. The column shift number in sequence is applied to the descending counter (Fig. 27a) of the denominational shift unit described in Section 12. Unless suppressed, half correction of the result will be made. It is understood that half correction is suppressed unless the column shift called for is a shift of at least one column to the right. The column shift number determines the order of the result to be rounded off or half corrected and, thereby, determines the sub-units order into which the half correction entry of 5 is to be made. If the sub-units order of the result is 5 or higher, the half correction entry of 5 acts through the carry means of the result accumulator to add 1 to the final column-shifted result.

All numbers transmitted to a receiving unit from the computing section are to be in true form. Accordingly, if the accumulated result is negative, a complement conversion cycle will precede the half correction sequence. But if the result is positive, the half correction sequence will start directly after the detection of the positive result indicant 0 in the 29th accumulator order.

The half correction sequence is under control of the internal commutator of the accumulator unit. This commutator calls for the accumulated result to be read out of the registers RC (Figs. 69a, b and 70) and brings the denominational shift unit into operation to receive the result and to effect column shifting thereof for a number of steps less by 1 than the column shift number entered by sequence into the descending counter. This shift brings the sub-units order of the result into shift column 1 (Fig. 25); hence, for convenience, this shift may be identified as the sub-column shift and the thus-far shifted result may

be called the sub-shifted result. Meanwhile, the internal commutator of the accumulator unit causes the EC and RC registers to be cleared and thereafter produces an entry of 5 in the 1st order EC followed by a true transfer of the 5 into the 1st order RC. When this 5 entry and the sub-units column shift have both been completed, the internal commutator of the accumulator causes the sub-shifted result to be true added into registers RC. The accumulation of the sub-shifted result with the half correction entry of 5 in the 1st order RC effects the rounding off of the ultimate result. This is the final stage in the half correction procedure performed under control of the internal commutator of the accumulator unit. At this stage, the units order, rounded off digit of the ultimate result stands in the 2nd order RC. Upon completion of this final stage the internal commutator sends a Proceed signal to main sequence. Main sequence then functions, in the manner described later in Section 17, item 20, to direct the result from registers RC to the shift columns and to cause the denominational shift unit to resume operation. Since the descending counter (Fig. 27*a*) now stands at 1, the denominational shift unit will perform the final shift step which brings the units order of the ultimate result into shift column 1. Thus, the total number of shift steps called for by main sequence has been effected and the shifted result is a rounded off result.

Fig. 74 is a timing chart indicative of the half correction procedure. Since it is assumed that a half correction suppression signal HCS has not been received by 1, Fig. 71*g*, the trigger 5, Fig. 71*g*, remains in shown state. With the trigger in this state, it allows the potential on certain control lines to remain at high or low potential, as the case may be, and these lines are marked HC+ or HC—, indicating respectively high or low potential on these lines during the half correction procedure.

As mentioned before, the commutator ACC.C (Fig. 78A) applies a negative going start signal ACC–ST to the internal commutator of the accumulator unit. This start signal initiates an accumulating cycle. The first signal ACC–ST is effective when half correction is not suppressed to reverse a trigger 20, Fig. 71*f*, as follows. This signal ACC–ST, besides being applied to 36*a*, Fig. 71*c*, is also applied to 32*a*, Fig. 71*f*, cutting it off to apply increased potential to the control grid of 28. With trigger 5, Fig. 71*g*, in normal status, it serves via 9, Fig. 71*g*, and line 928 to apply conditioning potential to the suppressor of 28, Fig. 71*f*. Accordingly, when the control grid of 28 is raised in potential under control of the signal ACC–ST, 28 conducts and turns 20, Fig. 71*f*. Turned trigger 20, Fig. 71*f*, acts via line 2017 to render 17, Fig. 71*g*, conductive. This serves as a Proceed signal block until trigger 20, Fig. 71*f*, is reset, which will not occur until the half correction sequence has been completed, as will be described.

Accumulation of a plurality of numbers is effected in the manner already described. After the last accumulator cycle in the accumulation run has been completed, commutator ACC.C (Fig. 78A) produces the readout control signal R.ROC which causes trigger 31, Fig. 71*g*, to reverse, as previously explained. Upon reversal of 31, it acts via 28*a* to reverse the sign test initiating trigger 20, Fig. 71*g*. Assume the sign test finds a positive result in the accumulator, so that positive signal O.CK is produced. When half correction was suppressed, tube 7, Fig. 71*g*, remained conditioned under control of reversed trigger 5, Fig. 71*g*, acting via 10, Fig. 71*g*. The O.CK signal was then effective to make 7, Fig. 71*g*, conduct as a result of which the Proceed trigger 19 and the read out control trigger 23 were reversed. However, it has now been assumed that half correction is not suppressed, so that 5, Fig. 71*g*, is not turned and 7 is not conditioned. Accordingly, the O.CK signal will not cause a Proceed signal to be produced and will not cause the result to be read out of the accumulator.

The O.CK signal, instead, initiates the half correction procedure. The tube 24, Fig. 71*e*, is being conditioned by the increased potential on line 928, so that the O.CK signal renders this tube conductive to reverse stages 26 and 27 of a 2-AP pulse counter 26, 27, 30 and 31. The first AP pulse following reversal of 26, restores it, causing 30 to turn. The next AP pulse returns 30, whereupon 31 turns. The third AP pulse returns 31, which restores 27. Thus, 27 is in reversed state for three AP pulse cycles.

Upon reversal of 27, Fig. 71*e*, it renders 32*a* conductive, reducing the potential on line 2530 so as to cut off the otherwise conductive tube 30, Fig. 71*g*. Upon 30 becoming non-conductive, it serves via 35 to produce the negative ACC–RO signal which is inverted by the related amplifier (Fig. 70) to the positive ACC–RO signal on line 22A—22B. Consequently, the digits and sign in the RC orders 1 to 29 are applied as reduced potentials on the buses of the Internal Out bus columns 29 to 1, respectively. The amplifier (Fig. 20) inverts these potentials to increased potentials on the corresponding buses of the Internal In bus columns.

During the three AP pulse period of reversal of 27, Fig. 71*e*, it makes 23 conductive to produce a negative signal HCCS. This signal acts via 25*a* and 25 in Fig. 71*b* to assure the setting of 21, Fig. 71*b*, in true add condition, which is its cancelled condition. The signal HCCS also initiates operation of the denominational shift unit. Referring to Fig. 27*b*, signal HCCS cuts off tubes 17, 20, 24, 24*a* and 29 in the subsequencing means of the denominational shift unit. Tubes 20, 24 and 24*a* are cut off to release triggers 19, 23 and 27 for subsequent reversal. Tube 17 is cut off to apply conditioning potential to the suppressor of 18, Fig. 27*b*. It may be noted from Fig. 74 that reversal of 27, Fig. 71*e*, and consequent occurrence of signal HCCS occurred at AP pulse time. The next effective BP pulse (see Fig. 19) cuts off 17*a*, Fig. 27*b*, which applies a positive pulse via a suitable coupling capacitor to 18, conditioned under control of signal HCCS, causing 18 to conduct and reverse 19. As 19 reverses, it turns 23. Turned 23 makes 22 conduct to cut off the otherwise conducting tube 21. This tube then produces the positive cancel signal SHCL. As described in Section 12, this signal acts on the SHC cancel circuit (Fig. 27*c*) and the line of elements shown below this cancel circuit to cause the triggers of the sub-sequencing means of the denominational shift unit to be reset and to cause the signal ACL to be produced. The signal ACL resets triggers ASH in each shift column (see Figs. 24 and 25).

The next BP pulse acts via still-conditioned 18, Fig. 27*b*, to restore 23, causing it to turn 27. Turned 27 makes 26 conduct to cause P26 to produce the positive SHRI signal. This signal renders the conditioned tubes IT, in each shift column (see Fig. 24), conductive to reverse the related triggers ASH. The tubes IT are now se-

lectively conditioned according to the digits of the accumulated result applied to the internal In bus-set, as previously described. Accordingly, the digits read out of accumulator orders 1 to 28 are entered, upon application of the SHRI signal to tubes IT, into shift columns 1 to 28, respectively.

The next BP pulse, acting through the still-conditioned tube **18**, Fig. 27*b*, resets **27**. As **27** is reset, it turns **30**. Turned **30** applies conditioning potential to **29** and **38** but these tubes do not conduct at this time as their control grids are still biased to cut-off.

The 3-AP pulse counter **26**, **27**, **30** and **31** in Fig. 71*e* completes its cycle and **27** returns at the next AP pulse time following the turning of **30**, Fig 27*b*. Accordingly, the negative signal HCCS terminates and the control grid of **29**, Fig. 27*b*, rises above cut-off potential. Also, tubes **17**, **20**, **24** and **24***a* in Fig. 27*b* become conductive. Tube **20** restores **19** while **24** and **24***a* block reversal of **23** and **27**. Tube **17** deconditions **18** to prevent repeat operation of **19**. Since **30**, Fig. 27*b*, is now in reversed state, conditioning tube **29**, the tube becomes conductive at the termination of the negative signal HCCS and produces a negative signal SHSA. This signal is applied to tube **5**, Fig. 27*c*, and serves, in the same way as the start signal SHS from the main commutator, to initiate steps of column shift. The column shift steps are performed in the manner already described in Section 12.

Upon restoration of **27**, Fig. 71*e*, the tube **23** produces a positive HCCS signal which is inverted by **33***a*, Fig. 71*g*, to a negative pulse, causing reversal of **29**, Fig. 71*g*, for one AP pulse cycle. When **29** is reversed, it cuts off **33**, causing it to apply a positive pulse via line **3322** to **22***a*, Fig. 71*f*. The latter thereupon produces a negative RCC signal which causes the RC cancel circuit and the KC cancel circuit (Fig. 71*a*) to function for resetting registers RC and carry triggers K of the accumulator.

The positive pulse produced by **23**, Fig. 71*e*, upon return of **27** also is inverted by **16** to a negative pulse which turns **19**. The negative pulse also is applied via line **1612** to trigger **12**, Fig. 71*f*, reversing it. The trigger **19**, Fig. 71*e*, is restored by the next AP pulse, but the trigger **12**, Fig. 71*f*, stays reversed until a complete signal CYCT is produced in an ensuing accumulator cycle.

The reversal of **19**, Fig. 71*e*, renders **20***a* conductive to produce an ECC cancel signal which causes the EC cancel circuit (Fig. 71*a*) to function for resetting entry registers EC.

Upon return of **19**, Fig. 71*e*, it reserves **15** for one AP pulse cycle. During the reversed time of **15**, it causes **11** to conduct and cut off tubes **4** and **7** to apply increased potential to terminals **2A** and **3A** (see Figs. 69*a* and 70). Accordingly, tubes **11** and **12** in Fig. 69*a* become conductive and force stages **4** and **1** of the 1st order EC register to reverse. In this manner, an instantaneous half correction entry of 5 is made into the 1st order EC, one AP pulse cycle following the resetting of EC and RC and carry triggers K of the accumulator.

The next step is to transfer the 5 from the 1st order EC to the 1st order RC. The trigger **29**, Fig. 71*g*, which was turned to cause an RC cancel to take place, as described above, is returned by the next AP pulse. Upon its return, it renders **33** conductive, causing it to reverse **25**, Fig. 71*g*. The following AP pulse returns **25**, causing it to reverse **21** for one AP pulse cycle. Upon reversal of **21**, it renders **13***a* conductive to cause **2** to produce the positive CC–ST start pulse. It may be noted that this signal is produced under control of **16**, Fig. 71*f*, and **13**, Fig. 71*g*, when a complement conversion cycle is called for (see Fig. 73). The signal CC–ST acts through **19**, Fig. 71*c*, to turn the start trigger **15**, as a result of which an accumulator cycle takes place. Since the trigger **21**, Fig. 71*b*, has been set in true add status, as previously explained, a true transfer of 5 from the 1st order EC to the 1st order RC takes place during the accumulator cycle. It should be noted that the start pulse CC–ST was produced one AP pulse cycle after the entry of 5 into EC. At completion of the accumulator cycle, the signal CYCT turns **8**, Fig. 71*f*, for one AP pulse cycle. Upon its return, **8** turns the "complete signal" trigger **7** for an AP pulse cycle. Upon reversal of **7**, it cuts off **5***a* to produce the positive signal CPT which goes to tube **15**, Fig. 71*g*, but since trigger **31**, Fig. 71*g*, is still in turned state, it functions via **28***a* to maintain **15** at cut-off, whereby a complete signal CYCPT to main sequence is blocked. Upon restoration of **7**, Fig. 71*f*, it returns **12**, Fig. 71*f*. As **12** returns, it restores **20**. Restored **20** acts via line **2017** to cut off **17**, Fig. 71*g*. This releases **17***a* for subsequent operation, under control of the next complete signal CYCT, to cause a Proceed signal and a result readout signal to be produced.

Meanwhile, the denominational shift unit has been column-shifting the accumulated result previously directed into the shift columns (Fig. 25). For each column shift step, the descending counter (Fig. 27*a*) is stepped to diminish the column shift number by 1 (see Fig. 26). When all but the last step of the column shift steps called for by main sequence have been performed, the descending counter stands at 1, i. e., only stage T1 is in reversed state. Under this condition, the tubes **8**, **12**, **20**, **24**, **32** and **36** are all cut off. The trigger **30**, Fig. 27*b*, was turned after the accumulated result was entered into the shift columns, as previously brought out. Trigger **30**, Fig. 27*b*, remains in turned state until reset under control of the next cancel signal SHCL from the main commutator. With **30** turned, it is effective via line G to cut off **37**, Fig. 27*a*. It is seen that when half correction for an accumulated result is taking place that the common anode line E of tubes **8**, **12**, **20**, **24**, **32**, **36** and **37** will rise in potential as soon as the descending counter stands at 1. The increased potential on line E makes **8**, Fig. 27*c*, conductive to reset trigger **11**–SHC3. It is to be noted that except in the half correction procedure for an accumulated result, the trigger **11** is restored when the descending counter goes to 0 as explained in Section 12. Restoration of **11** is followed by restoration of **15** and then by **18** in Fig. 27*c*. When **18** is restored, it cuts off **14** to cause a positive going pulse to be applied via wire **14***w* to tubes **4**, **38** and **39** in Fig. 27*b*. In the normal column shift procedure, this pulse makes **39** conductive to reverse **40** with the effect of sending the shift complete signal SHCP to the main commutator. When column shift under control of the accumulator unit is taking place, **30**, Fig. 27*b*, is in reversed state and deconditioning **39**. Accordingly, the positive pulse on wire **14***w* is not effective to make **39** conductive and the complete signal SHCP is blocked. Instead, a complete signal SHCA is sent to the internal commutator of the accumulator, to direct it to continue the half correction procedure, and at the same time, the sub-shifted result is read out to the Internal buses. To provide these

effects, turned 38, Fig. 27b, conditions 38 which becomes conductive upon receiving the positive pulse, via a capacitor, from wire 14w.

When 38 becomes conductive, it reverses 37. Reversed 37 serves via 33 to produce the negative, complete signal SHCA. Reversed 37 also acts via 34a and P35 to produce the positive signal SHRO which causes the number in the shift columns to be applied to the Internal Out buses and thence via the amplifier (Fig. 20) to the Internal In buses.

If the number of column shift steps called for by main sequence and entered in the descending counter is simply one step, then the signals SHCA and SHRO are produced as soon as 30, Fig. 27b, is turned. At that point, tube 37 in Fig. 27a will be cut off and line E will rise in potential. The tube 8, Fig. 27c, will become conductive and block 11 from reversal by the trigger 6 when the latter turns under control of the shift start pulse SHS. Failure of 11 to reverse prevents initiation of column shift steps, and trigger 18 remains normal. Hence, tube 14 is effective via line 14w to maintain tube 4, Fig. 27b, conditioned. Accordingly, upon the rise in potential of line E, 4, Fig. 27b, becomes conductive and applies a turning pulse by way of the anode resistor of 38 to trigger 37. Hence, the signals SHRO and SHCA are produced.

The negative complete signal SHCA goes to the grid of 36a, Fig. 71f, and cuts off this tube. The next AP pulse cuts off 36, and 36—36a thereupon make 32 conductive, so as to turn 35, Fig. 71f. It has been explained that 20, Fig. 71f, is turned off when the accumulator cycle for entry of 5 in the 1st order RC has been completed. Trigger 35, Fig. 71f, may be reversed by the signal SHCA either before or after 20 is returned, depending on the number of column shift steps which precede the production of signal SHCA. Only when 20 has been returned and 35 also been reversed, is the half correction procedure continued by the internal commutator of the accumulator unit. Returned 20 is effective via 27 to cut off 27a, and reversed 35 cuts off 31. The common anode line of 27a and 31 thereupon rises in potential and renders 17 conductive, turning 13 for one AP pulse cycle. Attention is directed to the fact that this same trigger 13 also is turned, but under control of 9 and 4, during the complement conversion sequence (see Fig. 73). Just as in the latter sequence, the triggers 14 and 18 in Fig. 71f are turned when 13 is restored; 14 is returned by the next AP pulse and turns 15 which, upon its return by a following AP pulse, resets 18. Just as in the complement conversion sequence, 14 and 18, while in reversed state, respectively cause the signals ECC and ACC–RI to be produced. Signal ECC cancels the registers EC and signal ACC–RI causes the number on the Internal In buses to be entered in registers EC. In the half correction sequence, the 5 standing in the 1st order EC is canceled and the sub-shifted accumulated result issued from the shift columns is entered in the registers EC.

Upon the return of 18, it turns 19, as in the complement conversion procedure. In the complement conversion procedure, the reversed trigger 19 was effective to cause 21 to conduct and produce the negative going RC cancel signal RCC. In the half correction procedure, it is not desired to cancel registers RC, but, instead, to retain the half correction 5 in the 1st order RC. As previously explained, the common anode line of 27a and 31 is now at increased potential owing to 20 being reset and 35 being turned. The increased potential on the anode line of 27a and 31 maintains 17 conductive, whereby the suppressor of 21 is held to cut-off. Accordingly, when trigger 19 is turned, it does not make 21 conduct to produce the RCC cancel signal.

Trigger 19 is reset by the next AP pulse after its reversal. Upon return of 19, it turns 24. In the complement conversion sequence, turned 24 was effective to make conditioned 1, Fig. 71f, conductive, as a result of which trigger 21, Fig. 71b, was set in complement entry control position. In the half carry procedure, the suppressor of 1, Fig. 71f, is held to cut-off by turned 35, Fig. 71f, and, therefore, the complement conditioning of trigger 21, Fig. 71b, does not occur. Instead, a tube 26, Fig. 71f, is made conductive by the turning of 24, the tube 26 being conditioned by the increased potential existing now on the common output of 27 and 31. When 26 becomes conductive, it acts via 31a and 30 to produce the negative going signal ACSB. This is a back signal to the internal commutator of the denominational shift unit and also serves via 26a, Fig. 71b, and 18a to insure the setting of 21, Fig. 71b, in true add status. Referring to Fig. 27b, signal ACSB acts via 32a to make 34 conductive, forcing trigger 37 to return. This terminates the complete signal SHCA sent by 33 to 36a, Fig. 71f, of the internal commutator of the accumulator unit.

Restoration of 24, Fig. 71f by the next AP pulse results in the reversal of 16. Just as in the complement conversion procedure, reversed 16 acts via 13, Fig. 71g, and 2 to produce the positive signal CC–ST which causes an accumulator cycle to take place. During this cycle, the sub-shifted accumulated result in EC is transferred to RC, being added therein to the half correction 5 in the 1st order RC. This means that the registers RC now contain the rounded off result in orders 2 to 29.

As now understood, 8, Fig. 71f, is turned at completion of the accumulator cycle and returned by the next AP pulse, causing 7 to turn, for one AP pulse cycle. When turned, 7 is still ineffective to produce the complete signal CYCPT because 31, Fig. 71g, is still in turned status. However, just as in the complement conversion procedure, turned 7, Fig. 71f, along with turned 16 is effective to make 3, Fig. 71f, conductive. When 3 becomes conductive, it acts via wire 317 to cut off 17a, Fig. 71g. This results in the turning of Proceed trigger 19 and readout control trigger 23.

When 7, Fig. 71f, is returned by the AP pulse following its turning, it restores 16.

As already explained, the reversal of 23, Fig. 71g, causes tube 27, still conditioned under control of the R.ROC signal, to become conductive, cutting off 30. This acts via 35 to produce the ACC–RO signal. The signal ACC–RO causes the rounded off result along with the sub-units order digit to be read out of the accumulator and onto the Internal buses. The Proceed signal, in a manner explained in Section 17, Item 20, causes main sequence to complete the half correction procedure. This involves the entry of the result, read out of the accumulator, into the shift columns (Fig. 25) and the initiation of column shifting according to the procedure outlined in Section 12. A new column shift number is not entered in the descending counter (Fig. 27a) which remains set at 1 to which it was brought by the half correction procedure. Accordingly, the denominational shift unit will effect the final additional column shift step, discarding the sub-units order digit of the result and bringing the rounded

off result read out of orders 2 to 28 of the accumulator, into shift orders 1 to 27. The trigger **35**, Fig. 71*f*, is restored under control of the positive signal CTLR from the main commutator. This signal is produced at the time the accumulated rounded off result is entered into the denominational shift unit (see Section 17, Item 19). Signal CTLR is inverted by **3**, Fig. 71*g*, to a negative reset signal for **11** and **35** in Fig. 71*f*.

The above description of the half correction sequence has considered the accumulated result as positive. If the accumulated result is negative, the **0.CK** signal is not produced when the sign test is made, so that **26**, Fig. 71*e*, is not turned and the half correction sequence is delayed. The negative sign of the result is stored by triggers **20** and **23** in Fig. 71*b*, and a complement conversion sequence (see Fig. 73) is effected in the manner previously described. When the conversion cycle is completed, **8**, Fig. 71*f*, turns and restores **6** which causes **11** to turn, all as described before. When **11** turns, it cuts off **23***a*, causing a positive pulse to be transmitted via line **2328** to the control grid of **28**, Fig. 71*e*. Since the half carry suppression trigger **5**, Fig. 71*g*, has not been reversed, the line **928** is at high potential and conditioning **28**, so that upon the turning of **11**, Fig. 71*f*, **28**, Fig. 71*e*, becomes conductive and reverses **26** and **27**. This starts the half correction sequence which is effected in the manner already described.

To complete the description of the accumulator unit, attention is directed to the fact that if the sign test at the completion of the accumulation of a plurality of numbers finds neither 0 nor 9 in the 29th accumulator order, neither the **0.CK** nor **9CK** signal is produced and the Proceed signal is not sent to main sequence, nor is the result read out. The failure to sense either 0 or 9 in the 29th accumulator order is an indication of misoperation in which is included the possibility, remote as it may be, that the sum of the numbers entered in the accumulator exceeds its capacity. It is to be noted, also, that even though the RC registers are cancelled under control of the internal commutator of the accumulator during the complement conversion and half correction procedures, the sign of the result is not cancelled because it is stored by the trigger **20**, Fig. 71*e*, which is reset under control of signal CTLR, as previously described.

14. *The multiplying and dividing unit*

This is a unit of the electronic computing section diagrammatically shown in Fig. 20. The multiplying and dividing means per se of this unit are of the same general type as the multiplying and dividing means disclosed in application Serial No. 704,914, of Dickinson et al., filed October 22, 1946, with certain novel changes and additions which will be described hereinafter.

The multiplying and dividing unit includes a 14-order register MP (note Fig. 64*b*) for receiving a multiplier factor when multiplication is called for. The multiplying and dividing unit, hereinafter abbreviated as the MD unit, also includes a 14-order register MC–DR (note Fig. 64*b*) for receiving a multiplicand factor when multiplication is called for and for receiving a divisor factor when division is called for. The MD unit further includes a register PQ having 33 orders a few of which are shown in Fig. 64*h*. The register PQ functions during a multiplying computation to form the product of the multiplier and multiplicand factors. The register PQ serves during a dividing computation to receive a dividend factor in orders 5 to 18 and thereafter serves to compare the divisor with the original dividend and successive dividend remainders so as to form the quotient. The multiplier register MP, the register MC–DR and the dividend receiving orders 5 to 18 of PQ all have their entry means associated with the buses in Internal In bus columns 16 to 29.

Entries of the numbers on these buses will be selectively made into the different registers and register orders according to whether multiplying or dividing computation is called for. The MD unit also has a sign mixing circuit (Fig. 65*j*) which mixes the operational signs with the factor signs and produces a result sign through the circuit shown in Fig. 65*k*. The result sign will be applied to Internal Out bus column 1. The result number, quotient or product, will be read out to 28 places from orders 33 to 6 of PQ and applied to columns 2 to 29, respectively, of the Internal Out bus-set, as indicated in Fig. 20.

Multiplication will be effected during a run of sequence for multiplication (see Section 18), while division will be effected during a run of dividing sequence (see Section 19). During the multiplying sequence, the multiplying computation control commutator MYC (Fig. 78M) is conditioned for operation to apply signals to the MD unit. During the dividing run, the dividing computation control commutator DVC (Fig. 78D) is conditioned for operation and applies control signals to the MD unit. The MD unit includes its own subsequencing means which may be called the internal commutator of this unit and is illustrated in Figs. 65*a* to *i*. The internal commutator includes its own source (see Fig. 65*i*) of 50 kc. A and B pulses for controlling operations of the multiplying and dividing means. Only the positive A and B pulses are effective pulses as used herein and it is to be understood that reference to these pulses is to the positive pulses. The MD unit includes, in its internal commutator, three electronic commutators or timers, called the primary, secondary and tertiary timers. The primary timer (Fig. 65*h*) is used in multiplication or in division to define what may be called the primary cycle (see Fig. 66). During this cycle a number in the register MC–DR may be transferred to the result register PQ. This transferred number is a multiplicand number if multiplication is being performed and is a divisor number, if division is being performed. The secondary timer (Fig. 65*g*) is used only in a multiplying calculation and controls stepping of orders of the register MP for the initiation of primary cycles. The tertiary timer (Figs. 65*c* and *d*) is used both in division and in multiplication to determine the column shift positions. The tertiary timer has thirty positions. During multiplication only the first fourteen positions are used and multiplication is terminated upon the end of the 14th column shift step of multiplication. In division, the first column shift position which is used is position 2 and the last which may be used is position 30. Half correction or rounding off may be effected in an order of PQ selected by the denominational shift number in the program means.

The multiplying means will now be described:

14*a*. *The multiplying means*

Multiplication is effected here by repeat addition of the multiplicand. The multiplicand dur-

ing a series of multiplication steps is routed from MC–DR into orders of DD–PQ selected by column shift means which has successive positions during the successive multiplication steps. The number of times the multiplicand is entered into the selected orders of PQ in each column shift position is determined by the digit standing in the multiplier order which is brought into control in the particular column shift position. When the multiplicand has been entered in the selected orders of PQ a number of times equal to the value of the decimal notation digit standing in the controlling order of MP, a multiplication step is over and the column shift means is stepped to its next position. In this next position, the next lower order of register MP will be the controlling order and the multiplicand will be directed from register MC–DR into orders of PQ which are, each to the right of the orders receiving the multiplicand in the previous column shift position.

As typical, the 1st and 14th orders of MP and the 1st, 2nd, and 14th orders of MC–DR are shown in Fig. 64*b*, and the 1st, 17th, 18th, 19th, 31st and 33rd orders of PQ are shown in Fig. 64*h*. It is understood that each register order is of the type discussed in Section 5 and shown in Figs. 15 and 15*a*.

The multiplicand and multiplier factors are applied one at a time to the Internal In bus-columns 16 to 29, being represented in binary decimal form, as now understood, by selective high and low potentials on the buses 1, 2, 4 and 8 of each of columns 16 to 29 of the Internal In bus-set. The buses of columns 16 to 29 of the Internal In bus-set are connected to corresponding orders 14 to 1 of respective multiplicand and multiplier entry means, as indicated in Fig. 64*a* (also see Fig. 20). The entry means for each order of MC–DR includes four gate tubes MCI8, 4, 2 and 1 and four associated entry effecting tubes MCE8, 4, 2 and 1. The entry means for each order of MP similarly includes four gate tubes MPI8, 4, 2 and 1 and four associated tubes MPE8, 4, 2 and 1. Increased potential on an Internal In bus of one of columns 16 to 29 is applied to the suppressors of the corresponding gate tubes MCI and MPI, conditioning both tubes. However, only one set of gate tubes will be rendered effective to pass through the digit representing potentials, depending on whether an entry signal MC–RI or MP–RI is applied. The signal MC–RI is the multiplicand entry signal and acts only upon the control grids of the set of gate tubes MCI. The signal MP–RI is the multiplier entry signal and is applied only to the control grids of the set of gate tubes MPI. Hence, only the conditioned tubes of one set of gate tubes will be rendered effective, according to which entry signal is being applied.

A gate tube MCI when rendered conductive, applies a negative pulse, by way of a suitable coupling capacitor to the associated tube MCE, cutting off this tube. The outputs MCEP of the tubes MCE are connected to the terminals *gr* of the corresponding orders of triggers in the register MC–DR (see Figs. 64*a* and *b*). Likewise the tubes MPE are connected by their outputs MPEP to the terminals *gr* of the related triggers in the register MP. The tubes MPE and MCE function, in the manner explained for the tube E in Fig. 10 (see Section 3*a*), to reverse the related triggers when the tubes are cut off. It is clear now that for making the entry of a multiplicand factor, the multiplicand representing potentials will be applied to the buses of Internal In bus columns 16 to 29, selectively conditioning the tubes MCI and MPI of orders 14 to 1, respectively. The multiplicand entry signal MC–RI will then be applied causing the conditioned tubes MCI to become conductive and cut off the corresponding tubes MCE. Thereupon, the tubes MCE cause the related triggers of register MC–DR to be reversed, so as to represent or register the multiplicand factor. Similarly, for making the entry of the multiplier factor, the multiplier factor will be applied to the Internal In bus-columns 16 to 29 after which the entry signal MP–RI will be applied to tubes MPI causing the conditioned ones of these tubes to become conductive. As a result, the related tubes MPE will be cut off to reverse the corresponding triggers of register MPE which thereupon will store the multiplier factor. As a specific example, assume that the MC factor includes the digit 6 in the 1st place. This digit is represented by increased potentials on the buses 4 and 2 of column 29 of the Internal In buses. Accordingly, the tubes MCI2 and 4 of order 1 and the tubes MPI2 and 4 of order 1 are conditioned. The MC–RI signal will then render the tubes MCI2 and 4 in order 1 conductive, so as to cut off the tubes MCE2 and 4 of this order. As a result, the triggers 2 and 4 of the first order of register MC–DR are reversed. The first order of this register is then storing the digit 6.

When multiplication is called for by the program, a multiplication calculation control commutator MYC (Fig. 78M) is conditioned for operation, in the manner later described in Section 18. This commutator produces signals for controlling the multiplying procedure. The first signal produced by the commutator is the negative signal M–Presense. This signal cuts off the normally conductive tubes H28 and H27 (Fig. 65*e*). The tube H26*a* is at cut-off unless a previous multiplying or dividing calculation is still in process. It may be assumed that this is not the case at present and that tube H26*a* is at cut-off at the time that the tube H27 is cut off. When both tubes H27 and H26*a* are at cut-off, they render the tube H29 conductive, so that trigger H29T remains cancelled, maintaining tube H31 effective to apply increased potential to the line *my* which is called the "up multiply" bus of the internal commutator of the multiplying-dividing section.

The M–PRE negative signal also is effective to render the normally conductive tube H28 non-conductive. The tube thereupon applies high potential to H19 which becomes conductive and forces H15 to reverse. It may be noted that H15 is normally blocked against reversal by H5 but when H28 becomes non-conductive it acts through H20 to cut off H5, releasing H15 for reversal by H19. With H15 reversed, it cuts off the blocking triodes H6, H7, and H8, releasing the triggers H10, H11, and H12, respectively, for reversals. These triggers are elements of a cancel timing counter. Also, H15 upon reversal renders H20*a* conductive to apply a turning pulse to cancel trigger H16. With H16 reversed it acts through H18 and H24 to apply a positive pulse to the input of the cancel circuit MDC. This cancel circuit is a basic cancel circuit such as explained in Section 3*b* and serves to reset the control triggers of the MD internal commutator, except for those in Figs. 65*a* and *b*. The duration of the cancel signal is limited to four 50 kc. pulse cycles by the cancel timing circuit

which comprises triggers H10, H11, and H12 (Fig. 65e). When H15 was turned to release the cancel timing counter for operation, it also brought the cancel control trigger H16 into operation. H15 also cut off H13. H13a is already cut off under control of H14. With both H13 and H13a cut off, H9 is conditioned to respond to A pulses and produces negative, A-phase pulses which are applied to the cancel timing counter. The first pulse reverses H10. The second pulse returns H10 and H10 thereupon reverses H11. The third and fourth pulses effect a second cycle of H10 to return H11. H11 upon returning, reverses H12. H12, when it turns, restores the cancel control trigger H16, thus terminating the cancel signal. The next four pulses applied to the cancel timing counter result in H12 being restored. As H12 restores, it turns H14. H14 thereupon makes H13a conduct, thus deconditioning H9 to render it unresponsive to the A pulses so that the operation of the cancel timing counter ceases.

When H14 is turned, it acts via connection 1431 to cut off D31 which is the cancel interlock tube. With this tube cut off, it does not prevent the multiply start signal which is subsequently applied, from functioning effectively.

The next signals produced by the MYC commutator (Fig. 78M) are the negative cancel control signal MCC and a concurrent negative cancel control signal PQC. Signal MCC cuts off 22, Fig. 64a. It may be assumed that interlock tube 23 is also cut off. Hence, couple 22—23 now applies a positive pulse to the input of the MC–DR cancel circuit. Register MC–DR (Fig. 64b) is thereby reset to zero status. The PQC signal is effective to cut off 3, Fig. 65k. Interlock tube 3a, Fig. 65k, may be assumed to be off, so the couple 3—3a now applies a positive pulse to the input of the PQ cancel circuit which operates to reset all the orders of PQ (Fig. 64h).

Just prior to cancellation of the registers MC–DR and PQ, the multiplicand factor is applied to Internal In bus columns 16 to 29. After the MCC and PQC cancel signals have been produced, commutator MYC produces a negative signal MC–RI which cuts off 19 (Fig. 64a). The interlock tube 20 is also at cut-off. Accordingly, the couple 19—20 becomes effective upon the receipt of the negative signal MC–RI to produce the positive signal MC–RI which is applied to the control grids of all the tubes MCI, causing the multiplicand factor to enter the register MC–DR, in a manner explained before. Following this, the commutator MYC produces the multiplier cancel signal MPC which is effective to cut off 15, Fig. 64a. The interlock tube 16, Fig. 64a, is off at this time, so the couple 15—16 is now effective to apply a positive cancel control signal to the input of the MP cancel circuit. As a result, the register MP is reset. Prior to the resetting of MP and after entry of the multiplicand into MC–DR, the multiplicand is removed by operation of the main sequence means from the Internal In bus-set, after which the multiplier factor is applied to columns 16 to 29 of this bus-set. Following this, the register MP is reset, after which the commutator MYC produces a negative signal MP–RI which cuts off 12 (Fig. 64a). The interlock tube 13 is also at cut-off at this time and hence the couple 12—13 produces the positive signal MP–RI which causes the multiplier factor to enter register MP, in the manner already explained.

The primary timer (Fig. 65h) has fourteen stages PR0 to PR13 and is driven by negative A phase pulses on the input PRI. Each series of 14 such pulses produces a cycle of the primary timer. The first pulse reverses PR13 to cause reversal of PR0. Upon reversal of PR0 it applies a positive pulse to A18 (Fig. 65h), initially conditioned by A11, causing A18 to become conductive and turn A5. A5, now turned, conditions A3 to respond to B+ pulses. A3 acts through A1 to produce positive MC–RB pulses in phase with the B+ pulses. The first of these pulses MC–RB is produced at 0.5 of a primary cycle (see Fig. 66). At the "9" point of the cycle, stage PR9 of the primary timer is reversed, thereupon conditioning A23 to respond to the next B pulse at "9.5" of the cycle. A23 thereupon becomes conductive and reverses A22. With A22 reversed, it conditions A15 to respond to the next A pulse at "10" of the cycle. A15 thereupon restores A5. It is clear that A5 is in reversed status from the "0" to the "10" time of the multiplying cycle and in this interval ten B-phase MC–RB pulses are produced (see Fig. 66). These MC–RB pulses are applied commonly to all the tubes 208 (see Fig. 64c) of which there is one for each order of register MC–DR.

When PR0 was reversed at the "0" time of the cycle, it conditioned A19 (Fig. 65h) to become conductive in response to the next B pulse at the "0.5" time and thereupon to reverse A11 and A12. With A12 reversed, it conditions A13 to respond to A pulses. A13 is capacitatively coupled to A14 and the output of A13 is inverted by A14 to positive A-phase pulses MC–RA. At the "10" point of the cycle primary timer stage PR10 is reversed and conditions A21 to respond to the next B pulse at 10.5 of the cycle. A21 thereupon restores A12 and A22. The restoration of A12 terminates the production of the MC–RA pulses. In the interval from "0.5" to "10.5" of the cycle, 10 positive A phase pulses MC–RA are produced (see Fig. 66), starting with the "1" point of the cycle. The MC–RA pulses are applied to the tubes 209 (Fig. 64b), of which there is one for each order of the MC–DR register. These tubes are normally conditioned and in response to the applied pulses produce negative A phase entry pulses to the orders of MC–DR and effect value cycles thereof such as explained in Section 5. A number of these pulses equal to the complement of the starting digit will cause stage 8 of a register order to produce a positive carry out pulse. This carry out pulse is applied through a line 210 (also see Fig. 64c) and a suitable coupling capacitor to the control grids of tubes 211 and tubes 212 associated with the same MC–DR register order. During multiplication, only the tubes 211 are conditioned. The conditioning potential is applied by a line TR which connects to the output of a tube J4 (Fig. 65i). Since line *my* is at increased potential during multiplication, as previously described, it makes J8 conduct, causing J4 to be non-conductive, so that line TR is at increased potential. Hence, a tube 211 (Fig. 64c) upon receiving a carry out pulse becomes conductive and turns the related trigger TC. As soon as the trigger turns, it conditions the connected tube 208, to which the B-phase MC–RB pulses (also see Fig. 66) are being applied, as previously explained.

It is clear that each tube 208 is conditioned by the related MC–DR register order at a cycle point which is the tens complement of the multiplicand digit in the order. For instance, if the multiplicand digit is 6, in the 14th order of MC, then

4 pulses MC–RA will cause the related trigger TC to be reversed and thereupon to condition the associated tube 208 at the "4" point (Fig. 66) to respond to the six pulses MC–RB at "4.5," "5.5," "6.5," "7.5," "8.5," and "9.5." The tube 208 is capacitatively coupled to a tube 213. Accordingly, tube 213 (14th order), in the example, will produce six positive B phase pulses R–B upon the wire C2 (also see Fig. 64*d*). These pulses are applied through a coupling capacitor to the control grids of a set of tubes C2T, which are further controlled by the column shift means so as to be successively conditioned in the sequential column shift positions. Similar means associated with the 13th order of MC–DR produces pulses R–B representing the multiplicand digit in this order. These pulses are applied to the control grids of a set of tubes C3T. Similarly, the control grids of tubes C4T, C5T . . . C15T receive the R–B pulses from the 12th, 11th . . . 1st orders of MC–DR. The tubes C2T to C15T are conditioned selectively according to column shift positions to respond to the pulses R–B and produce negative B-phase entry pulses for orders of PQ. Fig. 66A is a chart giving the columnar relation of the Internal In bus-sets to the MC–DR and PQ orders and also indicating the relation between the orders of MC–DR and PQ in the sequential column shift positions. In effect, the tubes C2T to C15T are the interrelating means between the MC–DR and the PQ orders in the different column shift positions, and these tubes are presented by small circles in Fig. 66A. The dotted lines indicate which of these tubes is conditioned in each column shift position. The full, light lines indicate the tubes receiving pulses R–B from the different orders of MC–DR, and the full heavy lines indicate the output connections of these tubes to the PG orders. It can be seen from Fig. 66A that there are thirty tubes C2T1 to 30 receiving pulses R–B from the 14th order of MC–DR and that in column shift position 1, the tube C2T–1 is conditioned to respond to these pulses and produce negative, B-phase entry control pulses for order 32 of PQ. It can be seen, further, that all the tubes C2T–1, C3T–1 . . . C15T–1 are conditioned in the 1st column shift position and, in response to pulses R–B from orders 14 to 1 of MC–DR produce entry control pulses for orders 32 to 19 of PQ. In other words, in column shift position 1, the factor in MC–DR is transferred to orders 19 to 32 of PQ. In column shift position 2, all the tubes C2T–2, C3T–2 . . . C15T–2 are conditioned and, in response to the R–B pulses, produce entry control pulses for PQ orders 31 to 18. During multiplication, the last column shift position is 14. In this 14th position, the tubes C2T–14 to C15T–14 are conditioned and, in repsonse to R–B pulses, produce entry control pulses for PQ orders 19 to 6. The negative, B-phase entry control pulses produced by the tubes C2T to C15T are transmitted via lines 215 and suitable coupling capacitors to capacitatively coupled pulse shaping tubes 216 and 217 (Fig. 64*h*) which apply the shaped negative entry pulses to the PQ registers.

The triggers TC (Fig. 64*c*) are reset at "10.5" of the cycle. As previously explained, stage PR10 of the primary timer (Fig. 65*h*) is turned at "10" of the cycle so as to condition A21 for operation by the next B pulse. Thereupon, A21 becomes conductive and restores A12 and A22, as mentioned before. In addition, when A21 becomes conductive it applies a negative impulse to A7 causing the latter to produce a positive "10.5" pulse. This pulse is applied to the control grids of the tubes 220 (Fig. 64*c*) which are being conditioned by the increased potential present on the line TR during the multiplying calculation, as previously explained. Accordingly, the "10.5" positive pulse applied to the tubes 220 renders them conductive to return the triggers TC.

As described above, pulses MC–RA will be applied in each primary cycle (Fig. 66) to the inputs of the MC–DR orders. A number of these pulses equal to the tens complement of the digit standing in an MC–DR order will cause this order to reverse the related trigger TC. The trigger TC will thereupon render the associated tube 208 effective to produce pulses R–B in response to the MC–RB pulses. These pulses will act on a set of tubes C2T to C15T, according to which order of MC–DR is being considered. In successive column positions 1 to 14, the tubes 1 to 14 of each set of tubes C2T to C15T will be conditioned to respond to the pulses R–B and produce a corresponding number of entry control pulses for the PQ orders related to these tubes. The multiplicand will thus be transferred in each primary cycle from MC–DR to orders of PQ selected by the column shift means. The entry into PQ will be completed by "10" of the cycle. The number of such cycles performed in each column shift position is determined by the digit in the MP order selected by the column shift position, in a manner described later.

Carry means are needed between the orders of the PQ register. The carry means used her is of the same nature as that described in Section 13 as used in the accumulator. Briefly, the carry means includes a trigger K (Fig. 64*g*) for each order of PQ. When an order of PQ (Fig. 64*h*) steps from 9 to 0 during the entry period it produces a positive carry out pulse at the terminal *c* of stage 8. This pulse is applied to a wire 8*cw* and is effective to render a triode KV (Fig. 64*g*) conductive. The triode thereupon reverses the trigger K associated with the order of PQ which has advanced from 9 to or through 0. For instance, assuming that the 17th order of PQ has stepped from 9 to 0, the trigger K17 will be in reversed state.

When an order of PQ (Fig. 64*h*), say the 18th order, is at 9, its stages 1 and 8 are in reversed status. With stage 1 in reversed status, its terminal *c* is at reduced potential. Likewise the terminal *c* of stage 8 is at reduced potential. The reduced potential at *c* of stage 1 is applied via wire 1*cw* to the tube 65 (Fig. 64*f*), cutting it off. Likewise, the decreased potential at *c* of stage 8 is applied via wire 8*cw* to 65*a* (Fig. 64*f*) having its anode commoned with the anode of 65. Assume, further, that PQ order 17 has stepped from 9 to 0 so that trigger K17 (Fig. 64*g*) is reversed. With K17 reversed, it is effective, via connection *k*17, to cut off the tube 65*b* (Fig. 64*f*) which has its anode commoned with anodes of 65 and 65*a* associated with the 18th order. A fourth tube 65*c* has its anode commoned with the anodes of tubes 65, 65*a*, and 65*b* associated with the same order of PQ. The tubes 65*c* associated with all the orders of PQ have their grids commonly connected to a wire *j*23. This wire is connected to the anode of tube J23 (Fig. 65*i*) controlled by a tube couple J19—J19*a*. J19 is normally cut off. The grid of J19*a* is connected by wire *j*19*a* to the plate of tube A53 (Fig. 65*h*) which is under control of trigger A52. The trigger A52 is in shown status except for the inter-

val between "11.5" and "13" of a cycle. Thus, A53 remains conductive except for this interval which overlaps the carry time between "12" and "12.5." Accordingly, the tube J19*a* (Fig. 65*i*) is non-conductive during the entry period "0" to "10" and couple J19—J19*a* renders J23 conductive to maintain wire *j*23 (also see Fig. 64*f*) at reduced potential during the entry period, so that the tubes 65*c* are at cut off during this period.

In the example where the 17th order has stepped from 9 to 0 during an entry period, K17 is reversed and has cut off 65*b* associated with the 18th order. Further, as the 18th order has been assumed to stand at 9, the tubes 65 and 65*a* associated with the 18th order are also cut off. As the tube 65*c* also is cut off during the entry period, the group of four tubes 65, 65*a*, 65*b*, and 65*c* for the 18th order are all cut off. It is clear that 65*c* is initially at cut off during the entry period and remains so until after the entry period. Further, the tube 65*b* may be brought to non-conductive condition at any point of the entry period at which the preceding order goes from 9 through 0. When the order stands at 8, the tube 65*a* goes to cut-off and when this order steps to 9 the tube 65 also goes to cut-off. It is evident then that either 65 or 65*b* will be the last one of the group of four tubes to be rendered non-conductive. Thereupon, the common anode line 65*p* of the group of tubes 65, 65*a*, 65*b*, and 65*c* rises in potential and renders a normally conditioned tube 65*d* conductive, thereby reversing the connected trigger K. In the example, the group of four tubes 65, 65*a*, 65*b* and 65*c* associated with the 18th order becomes effective through the related tube 65*d* to reverse the trigger K18. This reversal will occur at any mid-index time of the entry period 0.5 to 9.5 of a cycle (Fig. 66). If, in this same entry period, the 19th order also advances to 9, then the reversal of K18 will cut off 65*b* in the 19th order group of lock tubes and thereupon the trigger K19 will reverse. This chain of events may continue through any number of higher orders at 9.

It is seen then, that by the end of the entry period, reversal will have been effected of all those triggers K (Fig. 64*g*) associated either with PQ orders which have stepped from 9 through 0, or with a succession of orders of which the lowest has stepped from 9 through 0 and the higher ones are at 9. With a trigger K reversed, it acts via connection *kf* to condition a related tube KT (Fig. 64*f*). In the example, the tubes KT17 and KT18 are conditioned. At the "12" point of the cycle, a positive carry operating pulse C–OP is applied commonly to all the tubes KT. Any conditioned one of these tubes will become conductive and via connected line 215 and a capacitor apply a negative going impulse to entry tubes 216 and 217 (Fig. 64*h*) for the next order of PQ, whereby a carry entry is made into this next order. In the example, where KT17 and KT18 (Fig. 64*f*) are conditioned, the pulse C–OP renders these tubes conductive, with the result that carry entries are made into PQ orders 18 and 19.

In this manner, an instantaneous, simultaneous carry is effected into all orders of PQ following orders which have stepped from 9 to 0 or following one or more, successive orders which are at 9 at the end of the entry period and are preceded by an order which has stepped from 9 to 0. It may be noted that the carry entry is made into orders 1 to 27 through the same entry tubes 216 and 217 which are used during the entry of the multiplicand into orders of PQ. The highest order, the 33rd, of PQ never receives a direct entry of the multiplicand for obvious reasons and does not have associated therewith entry tubes 216 and 217. Only carry entries may be made into this highest order and these carry entries are made directly from the associated tube KT32 (Fig. 64*f*) via the connection 33*w* (also see Figs. 64*g* and *h*).

The carry operating pulse C–OP is taken from the output of tube J24 (Fig. 65*i*). This tube is controlled by the couple J20—J20*a*. Tube J20 is normally cut off. At the "11" point of the cycle, stage PR11 (Fig. 65*h*) is reversed and conditions a tube A45. At "11.5" of the cycle, a B pulse renders the conditioned tube A45 conductive to reverse A46 and A52. The reversal of A52 cuts off A53, causing line *j*19*a* to rise in potential and thereby to render tube J19*a* (Fig. 65*i*) conductive. Accordingly, the line *j*23 rises in potential and the tubes 65*c* (Fig. 64*f*) become conductive. This prevents the lock groups of tubes 65, 65*a*, 65*b* and 65*c* from being effective during the carry period to reverse the carry triggers K (64*g*), so that the carry-through-9 means is not operative during this period. The trigger A46 is reversed at "11.5" of the cycle, as explained above. Upon its reversal A46 conditions A47 and the next A pulse, occurring at "12" of the cycle renders A47 conductive to apply through a capacitor a negative pulse to A55. The latter thereupon produces a positive going pulse on the wire *a*55 which renders J20*a* (Fig. 65*i*) conductive. Thereupon J24 becomes non-conductive and produces the carry operating pulse C–OP which is applied to tubes KT (Fig. 64*f*). At "12" of the cycle the primary timer stage PR12 (Fig. 65*h*) is reversed and conditions A44. The next B pulse at "12.5," renders A44 conductive to restore A46, deconditioning A47. Also, when A44 becomes conductive, it turns A43 which thereupon conditions A51 to be made conductive by the next A pulse at "13." Upon A51 becoming conductive, it restores A52. Thus A52 is in turned condition between "11.5" and "13" of the cycle so as to cause the tubes 65*c* (Fig. 64*f*) to remain conductive during this period, for reasons explained before. Also, when A51 becomes conductive it applies a negative impulse by way of a suitable coupling capacitor, to tube A50 (65*h*), causing this tube to be cut off. Accordingly, tube A50 produces a positive "13" pulse on its anode line *a*50. This pulse renders the tubes J21 and J22 (Fig. 65*i*) conductive causing them to apply a negative "13" impulse to their output line *jp*. This negative "13" impulse is applied to the carry triggers K (Fig. 64*g*) causing any of these triggers which has been reversed during the previous pulse of the cycle, to be restored. At "13" of the cycle, the stage PR13 (Fig. 65*h*) is restored and conditions A42 to be made conductive by the next B pulse at "13.5." Upon A42 becoming conductive, it restores A43.

It has been stated that the number of times the multiplicand is routed into orders of PQ, selected by the column shift position, is determined by the digit in the multiplier register order also selected in the same column shift position. The control by an order of the multiplier register MP (Fig. 64*b*) is effected by applying entry control pulses to the order to roll it through a value cycle. The number of such entry control pulses equal to the tens complement of the multiplier digit will effect the advance of the MP order from 9 to 0. Upon an MP order effecting this 9 to 0 step, it applies a positive pulse, through

a capacitor, to a related tube MPC. The tube becomes conductive and applies a negative going pulse to a common output line MPO of all the orders of MP. In a manner which is explained later, the negative pulse on line MPO initiates the operation of the primary timer and the attendant primary cycles to cause the multiplicand to be transferred to the selected orders of PQ. The number of such cycles and therefore the number of times the multiplicand transfer repeats during a multiplication step is equal to the multiplier digit. The progress of the multiplication steps is determined by the secondary timer (Fig. 65*g*). This secondary timer is a decade counter exactly similar to a register order (Fig. 15). The secondary timer counts out ten entry control pulses applied in each column shift position to the MP order selected in this column shift position. When ten such pulses have been applied to the MP order it is back in its starting position. The secondary timer then controls the operation of the tertiary timer, which is the column shift control commutator, to advance to the next column shift position thus starting a next multiplication step. It is to be noted that, in each column shift position, a series of ten entry pulses will be applied to a selected order of MP; that a number of these pulses equal to the tens complement of the multiplier digit in the order will produce a carry out pulse from the order, initiating the cycle or cycles of transfer of the multiplicand to the selected orders of PQ. The remaining number of entry pulses of the series of 10 is equal to the value of the multiplier digit. At the end of the series of ten pulses, the column shift means is advanced to the next position and the operation of the primary timer and the multiplicand entry cycles is interrupted. It is clear that the number of primary, multiplicand transfer cycles in each column shift position will be equal to the value of the multiplier digit in the order selected by the column shift position. It may be noted that since no primary, multiplicand transfer cycles are to occur until the selected MP order has been advanced from its 9 to 0 position, that the entry pulses applied to the MP order may be high speed pulses. Likewise the secondary timer may be operated at correspondingly high speed to count these pulses. Thereafter the primary timer begins to operate to produce the multiplying cycles. Since there is to be one such multiply cycle for each remaining step of the MP order from its 0 position back to its starting value position and since these multiply cycles occur at reduced speed, the entry pulses applied to the selected MP order after it is stepped to 0 are supplied under control of the primary timer once for each multiply cycle. The secondary timer is operated correspondingly at the relatively lower speed by pulses produced under control of the primary timer.

The entry control pulses, designated MPR, are positive and applied to the control grids of all the input tubes MP–EN (Fig. 64*b*) of which there is one for each MP order. Only one of these tubes, however, is conditioned in each column shift position. Thus, in the 1st column shift position, there is increased potential upon terminal CS1 conditioning tube MP–EN14 to invert the pulses MPR to negative entry pulses MPRO for the 14th MP register order. In the 2nd column shift position, the input tube for MP order 13 will be conditioned by increased potential on terminal CS2 (see Fig. 65*c*), and so on, to the 1st order tube MP–EN (Fig. 64*b*) which is conditioned in the 14th column shift position in which terminal CS14 is at increased potential.

The feature of operating the selected order of MP and the secondary timer by high frequency pulses until the MP order is stepped to 0 saves considerable time in the multiplying computation. It avoids the use of comparatively slow speed primary cycles which are idle as far as the transfer of the multiplicand into the selected orders of PQ is concerned. The primary cycles, in each column shift position, are limited to just the number of cycles equal to the value of the multiplier in the MP order digit selected in the column shift position, and during which multiplicand transfers to PQ are effected.

To recapitulate, in each multiplication step the multiplicand is transferred into PQ at the primary timer controlled speed a number of times equal to the value of a multiplier digit. The column shift means selects the orders of PQ to receive the multiplicand and also selects the MP order to control the number of repeat cycles of multiplicand entry. The column shift means then is advanced to select an adjacent order of MP as a controlling order and to select adjacent orders of PQ to receive the multiplicand entries. The number of repeat cycles of the multiplicand entry is equal to the value of the multiplier digit and the selected MP order is advanced by a series of ten pulses in each column shift position. The number of advancing pulses equal to the tens complement of the multiplier digit effects the carry out step of the MP order and the remaining number of pulses of the series of ten is equal to the number of times the multiplicand entry is effected into the selected PQ orders. To clarify this, if an MP order is at 0, the entire series of ten pulses are required to step it back to 0. These pulses will be high frequency pulses so as to produce this idle value cycle of the MP order, registering 0, at very high speed. If the MP order contains, for instance, the digit 4 then the first six pulses applied thereto are high frequency pulses rapidly stepping it from its 9 to its 0 position, as indicated in Fig. 67. The next four pulses for returning the MP order to its starting digit 4 will be slower frequency pulses timed under control of the primary timer. Thus, a relatively considerable, over-all saving in multiplying time during a multiplying calculation is effected by operating the multiplying means at very high speed.

The entries of the multiplier and multiplicand factors into registers MC and MP have been described previously in this section. After these entries have been made, the commutator MYC (Fig. 78M), in a manner described in Section 18, produces a negative start signal MY–ST which cuts off D31*a* (Fig. 65*f*). D31 has already been cut off as a result of reversal of H14 (Fig. 65*e*) at the end of the operation of the cancel timing counter (Fig. 65*e*) initiated under control of the first signal M–PRE. Accordingly, when the start signal cuts off D31*a*, the common anode of D31*a* and D31 rises in potential and reverses trigger D30. Thereupon D30 reverses D37 and D37 reverses D43. With D43 reversed it cuts off D51 so that its output line, which is called the interlock line, goes to increased potential. It is to be noted that the interlock tubes 13, 16, 20, and 23 (Fig. 64*a*) now become conductive, positively preventing any alteration of the multiplicand and multiplier registrations in MC and MP.

When D37 (Fig. 65*f*) is reversed, as described above, it conditions D46 to be rendered conduc-

tive by the next A pulse and thereupon to reverse D45. D45, upon reversing, applies conditioning potential to D38 and the next B pulse renders D38 conductive to restore D37. As D37 is restored it conditions D44 to respond to the following A pulse and thereupon to restore D45. During the interval between two successive A pulses in which D45 was reversed, it conditioned D35 and the next B pulse caused D35 to become conductive and reverse the main start trigger D33. This trigger remains in reversed status until returned at the completion of the multiplying computation. With D33 reversed, it acts through D41 to apply decreased potential to a wire *d41* (also see Fig. 65*g*), cutting off B43. B43*a* is normally cut off under control of B26 acting via B34*a*. The tube B34 is cut off during the multiplying calculation because the line *dv* is at low potential except when dividing calculation is being effected. Accordingly, when B43 is cut off, the common anode line of B43, B43*a* and B34 rises in potential and conditions B27 to respond to the high frequency (50 kc.) A-phase pulses. These A-phase pulses are supplied from B19 which is coupled to the output of B18, normally conditioned by B4 to respond to the A+ pulses. In response to each applied positive A-phase pulse, B27 produces a negative pulse which operates through B44, B49, B52, B53 and B55 to apply a positive A-phase pulse MPR to the tubes MP–EN (also see Fig. 64*b*). As previously explained, the pulses applied to these tubes are inverted by the one tube which is conditioned in the existing column shift position to an entry pulse which effects a step of advance of the associated MP order (also see Fig. 64*b*). The negative pulse output of B27 (Fig. 65*g*) also is applied, via the anode resistor of B35, to the secondary timer to effect a step of advance thereof, so that each high speed pulse applied to the MP register is counted by the secondary timer.

A number of entry pulses equal to the tens complement of the multiplier digit in the selected MP order (Fig. 64*b*) advances this order to its carry out condition and as previously explained, the order then acts through the associated tube MPC to apply a negative pulse to the common line MPO. The negative pulse on MPO is applied to a tube B11 (Fig. 65*g*), cutting off this tube to impress a positive going pulse on the control grid of B12. As previously stated, start signal MY–ST has caused the interlock line to go to high potential. This line connects to the suppressor of B12. Accordingly, when under control of the MPO pulse, tube B11 applies a positive pulse to B12, the latter becomes conductive and reverses B22 and B4. With B4 reversed, it deconditions B18 so that the high speed A+ pulses no longer are effective to operate through B18, B19 and B27 to produce the high frequency operating pulses for the active MP order and for the secondary timer. With B22 reversed, it conditions B13 to respond to the next B pulse and turn B14 (see Fig. 67). Also with B22 reversed, it cuts off B21. At this time B21*a* is also cut off under control of a trigger B38, in its cancelled state, and a tube B37. Hence, when B21 is cut off by the reversal of B22, B21—B21*a* is effective to condition B20 to respond to the next B pulse. In response to this pulse, B20 turns B26. With B26 turned, it cuts off B34*a* to render B43*a* conductive, thus deconditioning B27. B34*a* also at this time conditions B35 to take over the control of the generation of pulses for operating the secondary timer and the selected MP register order. In addition, B34*a*, when cut off, conditions B42 to respond to A+ pulses and produce negative A-phase pulses. These negative A-phase pulses are transmitted via B41, B25 and B33 to the input line PRI of the primary timer. B14 was turned at the same B time as B23. Turned B14 causes B23 to respond to the next A pulse and return B22. B22 then conditions B15 to act, in response to the following B pulse, to reset B14. B14 thereupon resets B4. This allows A-phase pulses to be re-applied to B27 but these pulses are not effective because B27 has been deconditioned by turned B26. Hence, high speed operation of secondary timer and selected MP order will not occur. Instead, their operation will be controlled by the primary timer to which advancing pulses will be applied in consequence of the turning of B26, as described above.

In a manner explained before, the primary timer now operates through one or more primary cycles (Fig. 66) to cause the multiplicand to be transferred in each cycle to the selected orders of PQ (Fig. 64*h*). At "12" of the cycle, PR12 (Fig. 65*h*) is reversed and conditions A44 to respond to the next B+ pulse and reverse A43 at the "12.5" time. With A43 reversed, it conditions A51 to respond to the next A pulse at "13" which is inverted by A50 to a positive A-phase "13" pulse on the wire *a50*. This pulse, besides causing reset of the carry triggers K (Fig. 64*g*), as described before, is impressed on the now conditioned tube B35 (Fig. 65*g*), causing this tube to apply an advancing pulse to the secondary timer and also to apply a pulse to the tubes B44, B49, B52, B51 and B55 as a result of which the positive pulse MPR is applied to the tube MP–EN B49, B52, B53 and B55 as a result of which the primary cycle in which a multiplicand amount is transferred to orders of PQ, a single pulse is applied under control of the primary timer to the secondary timer and also to the active order of MP. The pulse applied to the MP order steps it to its next value position while the pulse applied to the secondary timer advances it so as to continue the count of the total number of pulses applied to the active MP order.

At the "13" time of the cycle, the primary timer stage PR13 (Fig. 65*h*) is restored and thereupon conditions A42 to respond to the next B+ pulse at "13.5." A42 thereupon becomes effective to restore A43, as described previously.

When the number of primary cycles equal to the value of the multiplier digit has been performed, then ten pulses have been applied to the secondary timer and to the active MP order in a particular column shift position. The 10th pulse of the series completes the cycle of the secondary timer and completion of the cycle is manifested by the return of its stage 8 to cancelled status. Upon the return of stage 8 to this status, which occurs at the "13" time of a cycle, it reverses B38. Upon the reversal of B38, it acts through B37 to condition B36 and B45 to respond to the next B pulse. B36 in response to this pulse becomes conductive and restores B26. B45 in response to the B pulse becomes conductive and reverses B46. B45, upon becoming conductive, also acts through B54 to apply a positive going pulse CSM to the wire *b54*. It is to be noted that this pulse is produced at "13.5" of the primary cycle. The positive pulse CSM is applied through a capacitor to the tube C23 (Fig. 65*e*) which is conditioned during multiplication by the high potential on the wire *my*. Ac-

cordingly, the pulse CSM renders C22 conductive to cut off C22. The latter thereupon acts through parallel tubes C21 and C25 to apply a negative going impulse CSS to the wire *ter* which is the input wire for the tertiary timer (Figs. 65*c* and *d*). The tertiary time has 30 stages TER1 to 30 and is part of the column shift means. In the cancelled condition of the tertiary timer, the 1st stage TER1 (Fig. 65*c*) is in a status which is opposite the status of each of the other stages. In this canceled status of the 1st stage TER1, it is effective to maintain a tube E1 non-conductive, so that its output terminal CS1 is at high potential. The remaining stages of the tertiary timer, in their canceled states, maintain the remaining terminals CS2 to CS30 at low potential. The terminal CS1 is connected to the correspondingly designated terminals in Figs. 64*b* and 64*d*. With the terminal CS1 in Fig. 64*d* at high potential, all the tubes C2T–1 to C15–1 are being conditioned. Accordingly, the multiplicand will be routed by the means described before and including these tubes into orders 32 to 19 of PQ, in the 1st column shift position (see Fig. 66A). Also, with the terminal CS1 in Fig. 64*b* at high potential, it is conditioning the tube MP–EN14 to pass the pulses MPR to the 14th order of register MP to effect the value cycle of this order in the manner explained before.

When, in the 1st column shift position, the multiplicand has been transferred to orders 32 to 19 of PQ a number of times equal to the value of the multiplier digit in order 14 of MP, the secondary timer (Fig. 65*g*) brings about the production of the negative pulse on wire *ter*, in the manner already explained. This pulse is effective to reverse TER1 of the tertiary timer. Upon its reversal TER1 reverses the 2nd stage TER2. Now, there is no longer increased potential at the terminal CS1 but instead there is high potential at the terminal CS2. With high potential on this terminal, all the tubes C2T–2 to C15T–2 (Fig. 64*d*) are conditioned and prepared to route the multiplicand into orders 31 to 18 of PQ (see Fig. 66A). Further, with CS2 at high potential, the tube MP–EN13 (Fig. 64*b*) is conditioned to direct the pulses MPR into the 13th order of MP to effect a value cycle.

The tertiary timer was stepped at "13.5" of a primary cycle. B26 (Fig. 65*g*) also was reset at this point and rendered B34*a* conductive. Consequently, B42 was deconditioned before the next A pulse time and operation of the primary timer is interrupted. Further, B27 was reconditioned to pass through the A-phase pulses, so that high speed operation of the secondary timer and of the MP order selected by the new column shift position will restart at the A pulse time following the advance of the tertiary timer to this new position.

B46 was turned also at the "13.5" time of the primary cycle in which B26 was reset and the tertiary timer stepped to its next position. Turned B46 conditions B47 to conduct in response to the next A pulse and thereupon to return B38. B38 then conditions B37*a* to act in response to the next B pulse to reset B46. All the initial conditions for high speed operation of the multiplier have been reestablished.

If the selected MP order stands at 0, the 10th high speed A-phase pulse will cause the order to produce the pulse MPO, causing B12 to turn B4 and B22. With B4 turned, it stops application of high speed A-phase pulses to B27. With B22 turned, it cuts off B21. But at the same A pulse time, the secondary counter has been advanced from 9 to 0 and has turned B38. This cuts off B37, so B21*a* conducts and prevents B20 from being conditioned to turn B26 at the next B pulse time. Hence B27 remains conditioned and primary cycles will not be initiated. The turning of B22 is effective, as before, to cause B13 to turn B14 at said next B pulse time, so B23 will restore B22 at the following A pulse time, causing B15 to restore B14 at the succeeding B pulse time (see Fig. 67). Upon restoration of B14, it resets B4 so that high speed A-phase pulses may be reapplied to B27 which has remained conditioned. This occurs at the second B pulse time following the stepping of the secondary timer from 9 to 0, and as a result of which B38 was turned. At the first following B pulse time, the turned trigger B38 allows B54 to produce the pulse CSM under control of which the tertiary timer is advanced to its next position. At the second, following B pulse time, B4 is reset so that A-phase pulses may be reapplied to conditioned B27. It is seen, therefore, that when an MP order stands at 0 it is advanced through a cycle at high speed, that at the next B pulse time the tertiary timer is advanced to select the next MP order, and that after a skip of one A pulse cycle, the high speed advance of this next MP order begins (see Fig. 67).

In the foregoing manner, the multiplicand will be transferred to successively lower orders of PQ in successive column shift positions. When the multiplication operations in the 14th column shift position have been completed, a pulse on wire *ter* will be effective to restore the stage TER14 (Fig. 65*d*).

Upon its restoration, TER14 reverses stage TER15. This stage thereupon cuts off a tube E18 to produce a positive going pulse on wire *e18*. This pulse is applied through a capacitor to the control grid of a tube C19 (Fig. 65*e*) which is normally conditioned when multiplication has been called for, as a result of the increased potential on the wire *my*. Accordingly, the pulse applied to the control grid of C19 is inverted to a negative impulse by this tube and is applied along a wire *c19* to the trigger D33 (Fig. 65*f*), restoring it. As previously explained, this trigger was reversed under control of a multiply start signal MY–ST. It may be recalled that this trigger D33 when reversed, initiated operation of the secondary timer and, thereby initiated, the performance of the multiplication operation after the factors have been read into their respective receiving registers. Now, at the completion of multiplication, the trigger D33 is restored in the manner just described. Upon restoration of D33, it applies a positive pulse to the control grid of D49. If half correction suppression has been signalled for, then the suppressor of D49 also will be at high potential and the application of increased potential to its control grid will render it conductive. The half correction suppression signal is produced, if the program calls for it, prior to the signal M–PRE, in a manner described in Section 18. The suppression signal, designated HCS comes from the main commutator and is negative. This signal is applied to G40 (Fig. 65*b*). As this signal is applied before the multiply start signal MY–ST has been produced, the interlock line will still be at decreased potential and cutting off a tube G40*a*. Hence, when G40 also is cut off, the couple G40—G40*a* becomes effective to make G32 conduct and thereby reverse trigger G24. With G24 reversed,

it maintains G8 conductive to produce a maintained, negative half correction suppress signal MHCS at decreased potential on its output line *g8*. The signal MHCS on line *g8* cuts off a tube D29 (Fig. 65*f*), so that the output of this tube goes to increased potential and conditions the tube D49. As previously described, with this tube conditioned, the return of trigger D33 at completion of multiplication is effective to render D49 conductive. When D49 becomes conductive, it reverses the "complete" trigger D42. The reversal of D42 sends out an internal, complete, negative signal CPLT along wire *d42* to the result sign circuit (Fig. 65*k*), where the signal cuts off 34*a*. As will be brought out in the description, to follow shortly, of the sign mixing and result sign means (Figs. 65*j* and *k*), if this means produces a proper result sign, tube 34, Fig. 65*k*, is at cut off by the time 34*a* is cut off by the internal, complete signal CPLT. With 34 and 34*a* both cut off, the couple 34—34*a* acts to render 33 conductive. Tube 33 thereupon emits a negative back signal R–CPLT which goes to the commutator MYC (Fig. 78M) and causes it, in a manner described in Section 18, to emit a negative result readout signal R.RO. This signal causes the product and its sign to be read out to the Internal Out bus-set. Before explaining the reading out means and operation, the sign mixing and result sign circuit and the rounding off or half correction means will be explained.

The sign mixing means.—The multiplicand and multiplier factors are accompanied by negative or positive signs. When the factors are applied successively to the Internal In bus columns 16 to 29, their accompanying signs are applied to Internal In bus column 1. If the sign of a factor is positive, it is represented by increased potential on bus 2 of Internal In column 1 (Fig. 65*j*) and if the sign is negative it is represented by increased potential on bus 1 of this column. The ultimate sign of the product is determined not only by these signs of the factors but also by the operational signs which are derived from the program means, in a manner explained later in Section 18. At the time the multiplicand factor and its sign are applied to the Internal buses, an operational sign representation for the multiplicand is applied to lines 1*s* and 2*s*. The sign mixing circuit includes an MC–DR factor sign and operational sign mixing network. The network mixes the operational sign representation for the multiplicand and the sign representation for the multiplicand (or divisor) factor and produces an output sign representation for this factor. When the multiplicand and its sign are removed from the Internal buses, the operational sign representation for the multiplicand also is removed from the input lines 1*s* and 2*s*. Subsequently, when the multiplier factor is applied to the Internal In bus columns, its input sign is applied to column 1 and an accompanying operational sign is applied to lines 1*s* and 2*s* in Fig. 65*j*. The input and operational sign representations for the multiplier are mixed by a multiplier (or dividend) sign mixing network MP/DD which produces a resulting multiplier (or dividend) output sign representation.

There are four possible operational signs explained in Section 2*a*. These are the operational signs 0, 1, 2, and 3. Operational sign 0 signifies that the output sign for a factor is to be + regardless of the input sign. Operational sign 1 signifies that the mixing network for a factor is to produce an output sign which is opposite to the input sign of the factor. Operational sign 2 means that the output sign of the factor is to be the same as the input sign. Finally, operational sign 3 means that the output sign for a factor is to be — regardless of the input sign.

Fig. 65*j* shows the complete mixing circuit network for the multiplier factor input and operational signs. If the multiplier sign is —, it is represented by increased potential on bus 1, column 1 of the Internal In bus-set. This increased potential is applied to 12, Fig. 65*j*, to condition the latter. If the multiplier sign is + then the bus 2 of column 1 of the Internal In bus-set is at increased potential and results in the conditioning of 11. If the operational sign 1 is accompanying the multiplier factor, then it takes the form of increased potential on line 1*s*, causing 10 to be conditioned. Operational sign 2 is represented by increased potential on line 2*s* and conditions 9. As previously explained, an MP–RI negative signal is produced by commutator MYC (Fig. 78M) to time the entry of the multiplier into register MP (see Figs. 64*a* and *b*). This same signal is applied to 30, Fig. 65*j*. The interlock tube 29 is off at this time, since its grid is connected to the interlock line *d51* which, as previously described, remains at low potential until the start signal MY–ST is applied, and this occurs only after the factor and sign entry times. Accordingly, 30—29 becomes effective upon the application of the MP–RI signal to apply increased potential to the control grids of the tubes 9, 10, 11 and 12. Any of these tubes which has been conditioned becomes conductive and effects the reversal of a related one of the four triggers 17, 18, 19 and 20 in Fig. 65*j*.

Asssume that operational sign 0 is applied to the MP/DD sign mixing circuit. As previously indicated, this operational sign requires that the mixing network produces a + output sign, regardless of the input sign for the factor. It will be noted that when the operational sign is 0, the lines 1*s* and 2*s* remain at decreased potential so that neither tube 9 nor 10 is conditioned. Accordingly, triggers 17 and 18 remain in cancelled status. With 17 and 18 in cancelled status, they render 41 conductive. Hence 41 fails to condition 49, the output 49*w* of which is the multiplier (or dividend) + sign output. Accordingly, this output remains at effective, high potential. With 17 in cancelled status, it is deconditioning 33, 36, and 42. With 18 in cancelled status, it is deconditioning 34, 35 and 42. It is clear now that when both the triggers 17 and 18 are in cancelled status, only the tube 41, of the set of tubes 33, 34, 35, 36, 41 and 42 is conductive. As 42 remains nonconductive, it applies conditioning potential to the control grid of 51. With 35 and 36 nonconductive, they apply increased potentials to the control and suppressor grids of 44. Accordingly, 44 is conductive and cuts off 52 which applies increased potential to the suppressor of 51. Inasmuch as 51 is conditioned by increased potential on its control grid, 51 becomes conductive and applies reduced potential to the multiplier (or dividend) — sign output line 51*w*. The reduced potential on this line indicates absence of a — sign output for the multiplier (or dividend) factor.

Assume the operational sign applied to the multiplier factor is the operational sign 1 which requires that the mixing network produces an output sign which is opposite the input sign of

the multiplier. The application of operational sign 1 causes reversal of trigger 18. With this trigger reversed, it conditions 34, 35 and 42. Assume the input sign for the multiplier factor is —, so that the trigger 20 is reversed. With this trigger reversed, it applies increased potential to grids of 36 and 34. Under the stated conditions, the tube 34 becomes conductive and deconditions 43. Accordingly, 43 applies increased potential to the suppressor of 50. Inasmuch as 42 remains non-conductive, it applies increased potential to the control grid of 50 and also to the control grid of 51. Since the suppressor of 50 also is at increased potential, it becomes conductive and deconditions 49 so that the + sign output line 49*w* goes to increased potential which is the effective potential for reading out a + output sign for the multiplier (or dividend) factor. Under the stated conditions tube 35 remains non-conductive inasmuch as its control grid is being held at low potential by unreversed trigger 19. Also the tube 36 remains non-conductive because its control grid is kept at low potential by trigger 17 in its cancelled state. Since 35 and 36 are both non-conductive, they act on 44 to render it conductive. In turn, 44 cuts off 52 to apply increased potential to the suppressor of 51. Since increased potential has been applied by the non-conductive tube 42 to the control grid of 51, the latter is conductive and the output line 51*w* goes to low potential, indicating that the output sign for the multiplier (or dividend) is not the — sign. In short, under the conditions where the input sign for the multiplier (or dividend) factor is — and the operational sign is 1, the output sign is +.

Assume the operational sign is still 1 but that the multiplier sign is +. Accordingly, triggers 18 and 19 are reversed. In this case tube 35 becomes conductive and tubes 33, 34, 36, 41 and 42 remain non-conductive. With 35 conductive, it deconditions 44 which makes 52 conduct. Accordingly, 51 is deconditioned and its output 51*w* goes up in potential, manifesting a — sign output for the multiplier factor. As 33 and 34 are off, 43 is conductive and deconditioning 50; hence increased potential is being applied to the suppressor of 49. Also, since 41 remains non-conductive it is applying increased potential to the control grid of 49. Thus 49 is conductive and its output 49*w* goes down in potential indicating that the output sign is not a + sign.

In the case where the operational sign is 2, the output sign will be the same as the input sign of the factor. In this case, trigger 17 is reversed. Assume the input sign for the factor is +, so that trigger 19 also is reversed. Under these conditions tube 33 is conductive while tubes 34, 35, 36, 41 and 42 remain non-conductive. As 33 is conductive it causes 43 to be non-conductive so as to condition 50. Inasmuch as 42 is non-conductive it is also applying increased potential to 50. Therefore, 50 is conductive and rendering 49 non-conductive to apply increased potential to line 49*w* manifesting a + output sign for the multiplier factor. With 35 and 36 non-conductive, 44 is conductive and cutting off 52 to apply increased potential to the suppressor of 51. Also, 42, being non-conductive, applies increased potential to the control grid of 51 so that the — sign output line 51*w* is at decreased potential. Assume instead that the input sign for the factor is — and that the operational sign is 2. Under these conditions 17 and 20 are reversed. In this case tube 36 will be conductive and tubes 33, 34, 35, 41 and 42 will be non-conductive. Accordingly, 44 will be rendered non-conductive so as to make 52 conduct. With 52 conducting, it renders 51 non-conductive to produce an increased potential on its output line 51*w*, representing a — output sign for the multiplier factor.

It is seen that when the operational sign is 2, the output sign for the factor is unchanged with respect to the input sign.

Assume the operational sign to be 3, which means that the output sign is to be — regardless of the input sign of the factor. With both the lines 1*s* and 2*s* at increased potential, representing operational sign 3, the triggers 17 and 18 will be reversed. Accordingly, 42 will be conductive and will render 51 non-conductive to produce increased potential on line 51*w* to represent a — output sign. Since 42 is conductive, it also cuts off 50 to apply increased potential to the suppressor of 49. With either trigger 17 or 18 reversed, 41 remains non-conductive and applies increased potential to the control grid of 49. Hence, under the stated conditions 49 is conductive and its output line 49*w* goes down in potential, indicating that the output sign is not the + sign. It is evident therefore that when the operational sign is 3, the output sign will be — regardless of the input sign of the factor. The negative multiplier cancel signal MPC coming from commutator MYC (Fig. 78M) and which as previously explained causes the multiplier cancel circuit (Fig. 64*a*) to operate for resetting the register MP is also applied to 28, Fig. 65*j*. During the multiplying calculation, line *my* is at high potential and renders 25 conductive. This causes 25*a* to maintain 28 conductive except when signal MPC is applied. This signal cuts off 28. The interlock tube 29 is still cut off. Accordingly, upon 28 receiving the cancel signal MPC, 28—29 renders elements 26, 26*a*, 27 and 27*a* conductive. These elements are respectively coupled to the terminals *f* of triggers 17, 18, 19, and 20. Hence, when the tubes 26, 26*a*, 27 and 27*a* become conductive, they cancel the respective triggers. Thus before the multiplier factor is entered and its output sign determined, the triggers in the multiplier sign mixing network are reset.

The multiplicand (or divisor) sign mixing circuit MC/DR (Fig. 65*j*) and its controls are similar to the multiplier (or dividend) sign mixing circuit and its controls, with the exception that the sign entering circuits are rendered effective by the multiplicand read in signal MC–RI (or dividend entry signal DR–RI) applied to 31, the anode of which is coupled to the anode of interlock tube 31*a*. The + output sign of the MC/DR mixing circuit is represented by high potential on line 53*w*, while the — output sign is represented by increased potential on line 55*w*. Also the sign triggers in the MC/DR mixing circuit network are cancelled under control of the MC/DR cancel circuit (Fig. 64*a*).

The sign of the product (or quotient) is determined by the output signs of the factors. If the output signs of both factors are +, then tube 2, Fig. 65*k*, is conductive and cuts off 10. This conditions the suppressor of 18. The control grid of 18 is connected to interlock line *d*51 which goes to increased potential as a result of the application of start signal MY–ST (Fig. 65*f*). Accordingly, 18, Fig. 65*k*, becomes conductive at that time, if both factor output signs are +, and

reverses a trigger 27. This stores the fact that the sign of the calculated result is +. If both output signs are —, then 3 is conductive and deconditions 10. Again 18 is caused to conduct at start signal time and trigger 27 is reversed to store a + sign for the result. If the multiplier (or dividend) output sign is positive and the multiplicand (or divisor) output sign is negative, then 5 is conductive and deconditions 13, as a result of which 21 conducts at start signal time and reverses a trigger 29 to store a — sign for the result. If the multiplier (or dividend) output sign is — and the multiplicand (or divisor) output sign is +, then 4 is conductive and also deconditions 13 with the result that 21 conducts and 29 is reversed to store a — sign for the product.

The triggers 27 and 29 are cancelled at the same time that the accumulator PQ is cancelled, prior to factor and sign entries, under control of the PQC signal. This signal is also applied to 19*a* in Fig. 65*k* to render it non-conductive. The interlock tube 19 is still off at that time and 19—19*a* becomes effective to render 20 and 20*a* conductive, thereby resetting triggers 27 and 29.

As previously explained, if half correction is not called for, then the signal CPLT, signaling the completion of multiplication, will be produced by reversal of trigger D42 (Fig. 65*f*) upon the restoration of D33 after the 14th column shift step. The signal CPLT will cause a complete signal R–CPLT to be sent to commutator MYC (Fig. 78M) if the sign mixing and result sign circuit (Figs. 65*j* and *k*) has operated properly. Commutator MYC will then return a result readout signal R.RO (Fig. 65*k*) to the MD unit. The readout signal will cause the product and product sign to be read out from register PQ to the Internal Out bus-set. On the other hand, if half correction is not suppressed, then the complete signal CPLT and reading out will be delayed until half correction has been effected.

In the description of the sign mixing and result sign producing means, it was explained that either a trigger 27 or a trigger 29 in Fig. 65*k* is reversed to store either a + or a — result sign, respectively. If neither or both of these triggers are reversed, then it is a manifestation of some misoperation. In that event, tube 34, Fig. 65*k*, will remain conductive and the cutting off of 34*a* by the signal CPLT will be ineffective. The control of tube 34 is effected as follows. If 27 is reversed, it applies increased potential to the control grid of 26. When 27 is reversed, then 29 should remain in its cancelled state and apply increased potential to the suppressor of 26. Therefore, the conditions for making 26 conduct have been satisfied and the tube applies decreased potential to 34 cutting it off. On the other hand, if 29 also is reversed along with 27, indicating a misoperation, then 26 will remain nonconductive and 34 will remain conductive nullifying the effect of the signal CPLT on tube 34*a*. Assume that neither of the triggers 27 and 29 has been reversed, also indicating misoperation. In that case the control grid of 26 will remain at low potential. Also the control grid of a tube 28 will remain at low potential. As a result, 34 will remain conductive. Assume that 29 has been reversed and 27 remained in cancelled state. 29 then will apply increased potential to the control grid of 28 and at the same time 27 will apply increased potential to the suppressor of 28. Tube 28 will conduct and 34 will be cut off to enable the signal CPLT to be effective to render 33 conductive so as to emit the negative complete signal R–CPLT. In response to this signal, commutator MYC (Fig. 78M) produces a negative result readout signal R.RO. This signal is applied to 36, Fig. 65*k*. The same signal also is applied to 8 and 9 in Fig. 65*k* which apply a positive signal R.RO to the control grids of all the sets of readout tubes PQ–R (Fig. 64*i*). There is a set of four tubes PQ–R1, 2, 4 and 8 for each of orders 6 to 33 of register PQ, which are associated with columns 29 to 2, respectively, of the Internal Out bus-set, as may be understood from Fig. 66A. It should be noted that orders 1 to 5 are inactive during the multiplication operation and, in any event, are not read out to the buses. The suppressors of tubes PQ–R are respectively coupled to the terminals *f* of the stages 1, 2, 4 and 8 (Fig. 64*h*) of the associated order of PQ. The number standing in an order of PQ is represented by the stages or combination of stages which have been reversed. When a stage is reversed, its terminal *f* is at high potential and conditioning the related one of the tubes PQ–R (Fig. 64*i*). It is clear now that there are 28 sets of readout tubes PQ–R which are selectively conditioned in accordance with the amount standing in register PQ. The positive readout signal R.RO renders the conditioned ones of the tubes PQ–R conductive to send out negative going binary digit representing impulses on the buses of the Internal Out bus-set columns 2 to 29. These digit signals are transmitted to the denominational shift means explained in Section 12. The product sign is read out as decreased potential upon bus 1 or 2 of column 1 of the Internal Out bus-set. Assuming that the product sign is +, trigger 27, Fig. 65*k*, is reversed and conditioning 35. The signal R.RO applied to 36 cuts it off and causes it to apply increased potential to the control grid of 35. Consequently 35 becomes conductive and applies a reduced potential to bus 2, column 1, Internal Out bus-set. This reduced potential on this bus represents a + sign. If, on the other hand, 29, Fig. 65*k*, has been reversed, then it is conditioning 37 and the readout signal R.RO, acting through 36, makes 37 conduct to apply reduced potential to bus 1 of column 1, representing the — sign.

The negative readout signal R.RO, from commutator MYC (Fig. 78M) is also applied to a tube D34 (Fig. 65*f*), cutting it off so as to restore the trigger D42. Upon restoration of D42, it restores the control interlock trigger D43, so the interlock line *d*51 returns to low potential.

The half correction—The number of digits in the product is either equal to or one less than the sum of the digits in the multiplier and multiplicand factors. The column shift amount is chosen according to the number of digits of the product to be ultimately transmitted through the column shift means to a receiving unit. For instance, the product may be a maximum of 28 digits but the receiving unit in the present case is designed to receive a maximum of 19 digits plus, of course, the sign. Therefore, when the product is 28 digits in size, at least the nine right-hand digits must be discarded through the operation of the denominational shift means (Section 12). In such case, the column shift amount will be at least nine and the shift to the right will be signalled for. The maximum column shift amount when column shift is to take place to the right is a shift of 27. It is seen therefore that the column shift amount may

vary from 0 to 27. The last right-hand order to be transmitted to the receiving means is rounded off, unless a half correction suppression signal is received by the MD unit. As understood, the half correction, or rounding off operation, consists in adding five to the order of the product at the right of the last right-hand order to be transmitted to the receiving unit. For convenience, this right-hand order will be called the transmitted units order and the order to the right thereof and to which five is to be applied for rounding off purposes will be called for convenience the sub-units order. The column shift amount determines or selects the transmitted units order and therefore selects the sub-units order. This follows from the fact that the last right-hand order to be discharged is the sub-units order and the discarding of this order is effected through the column shift means described in Section 12. Actually, rounding off of a product result will be called for only in connection with a column shift to the right. The number of digits to be discarded is equal to the column shift amount to the right. This means, for example, that if the nine right-hand digits are to be discarded, the column shift amount will be 9. The sub-units order of PQ is the last one which is to have its result digit discarded by the column shift means. As indicated in Fig. 66A, PQ orders 1 to 5 are not connected to the Internal Out bus columns and are not read out. In effect, therefore, PQ order 6 is the lowest units order which is read out. Thus, in relation to the Internal bus columns 2 to 29 and the 28-place result which may be applied thereto by PQ, orders 6 to 33 of PQ correspond to result places 1 to 28. Therefore, if one right hand place of the result is to be discarded by the denominational shift unit (Section 12) then order 7 of PQ will be the one which carries the ultimate units order result digit and order 6 will be the sub-units order. In other words, to arrive at the PQ order number which carries the sub-units place digit of the result to be read out of the denominational shift amount, 5 must be added to the column shift amount. For instance, if the column shift amount is 13, then the sub-units order of PQ is order 18, and the transmitted units order is order 19. Clearly then, the column shift amount selects the sub-units order. The column shift amount is originally represented in its binary decimal form. It was also explained in the description of the column shift means that the column shift amount was applied to lines MN1, 2, 4, 8, 10 and 20 (Fig. 27*a*). These lines connect to corresponding lines MMN (Fig. 65*a*) in the control section for the multiplication means. Referring to Fig. 65*a*, the increased potentials selectively present on these lines, are applied to the suppressors of tubes CSA1, 2, 4, 8, 10 and 20. When the negative signal MC–RI is produced to cause the multiplicand factor to be read in, the signal also is applied to a tube 64, Fig. 65*a*. At this time, the control interlock line *d*51 is still at low potential and is cutting off 64*a*. When 64 is cut off by the signal MC–RI the couple 64—64*a* is effective to make 63 conduct which in turn cuts off 53 to apply increased potential to the control grids of all the tubes CSA1, 2, 4, 8, 10 and 20. Those tubes which are conditioned according to the column shift amount by increased suppressor potential become conductive and reverse the related triggers CST1, 2, 4, 8, 10 and 20. These triggers function through interpreting circuits to translate the binary decimal terms of the column shift amount into electrical representations of the equivalent amount in a decimal notation. Assume for simplicity of explanation that the column shift amount is 21. Accordingly, the triggers CST1 and CST20 are reversed. With CST1 reversed, it applies increased potential to line *cstf*1 connected to tubes G3, G2, G1 (Fig. 65*a*), G9 and G10 (Fig. 65*b*). This eliminates the 0, 8, 6, 4 and 2 groups of units order column shift amount interpreting tubes from consideration in the application of the rounding off pulses. At this point it may be stated that there are ten interpreting groups of tubes, the groups being designated UCS0, 1, 2 . . . 9. These groups select, for receiving the five rounding off pulses, the PQ orders whose order numbers have, in the right-hand place, the interpreting group digit plus 5. For reasons now understood, the interpreting group number is less by 5 than the actual sub-units order of PQ. Thus, the group UCS0 will select those PQ orders whose order numbers have 5 as their right-hand digit; i, e., orders 5, 15 and 25. The group UCS1 selects PQ orders 6, 16, and 26. The group UCS3 selects PQ orders 8, 18 and 28. The group UCS4 selects PQ orders 9, 19 and 29, and so on. The selection by an interpreting group is effected by its conditioning the suppressors of tubes HCE (Fig. 64*e*) individually associated with the possible sub-units orders selected by the group. One of the conditioned tubes will receive the five rounding off pulses and pass them to the entry means of the desired sub-units order. For example, if the column shift amount is 13, the selected sub-units order is 18. The interpreting group UCS3 will be rendered effective, in a manner described soon, to condition the three tubes HCE associated, respectively, with PQ orders 8, 18 and 28. Subsequently, five rounding off pulses will be applied via line TCS 10 to tubes HCE associated with PQ orders 15 to 24. Of these tubes, only the tube HCE associated with order 18 has been conditioned and will pass the rounding off pulses to the entry means for the 18th order of PQ. In this manner, when the column shift amount is 13, five rounding off pulses will be applied to PQ order 18.

The effective output potential of the USC groups (Figs. 65*a* and *b*) is an increased potential. If any tube in a group is rendered conductive it prevents the group from producing effective increased output potential. As already explained, the triggers CST are reversed according to the binary decimal terms of the column shift amount. The triggers CST1, 2, 4 and 8 will determine in accordance with their status which of the UCS groups is to be effective. For instance, if only the trigger CST1 (Fig. 65*a*) has been reversed, then only the group UCS1 (Fig. 65*b*) will produce effective output potential. The other groups will have one or more tubes which will be maintained conductive under control of one of the four triggers CST1, 2, 4 and 8. Groups 0, 2, 4, 6 and 8 will be made ineffective because reversed trigger CST1 places increased potential on line *cstf*1 which renders conductive G3 in UCS0, G2 in UCS8, G1 in UCS6, G9 in UCS4 and G10 in UCS2. The group UCS7 will be made ineffective because G11 will be maintained conductive by trigger CST2 in reset status and also because tube G27*a* will be maintained conductive by the unreversed trigger CST4. Group UCS9 will remain ineffective because G35*a* is being held conductive by unreversed trigger

CST8. Group UCS3 will be ineffective because unreversed trigger CST2 is holding G18a conductive. On the other hand, the group UCS1 will be made effective because tube G10a will be cut off by the decreased potential, on line *cstn1*, produced by reversed trigger CST1. Tubes G17a, G33a and G34a will be cut off by the unreversed triggers CST2, 4 and 8 respectively. The increased potential produced by group UCS1 on its output line *ucs1* will be applied to the suppressors of tubes HCE associated with orders 6, 16 and 26 of PQ. As another example, if the units order of the column shift amount is 3, then triggers CST1 and CST2 will be reversed and group UCS3 will be effective to condition tubes HCE of orders 8, 18 and 28 of PQ.

The binary terms representing the tens place of the column shift amount will be translated into the selective conditioning of either of three tubes G52, G50 and G49 in Fig. 65b. If the tens place of the column shift amount is 0, it does not result in reversal of either CST10 or CST20 (Fig. 65a). If the tens digit of the column shift amount is 1, CST10 will be reversed and if the tens order digit is 2, then CST20 will be reversed. Assuming both of these triggers are in canceled state, they are applying cut-off potential, via lines *cstf10* and 20 to G43 and G51 (Fig. 65b). Consequently, this couple is applying conditioning potential to G49. If CST10 is reversed, its output line *cstn10* is cutting off G43a. At the same time the trigger CST20 will not be reversed and will be cutting off G51a. Accordingly, couples G43a and G51a will be applying conditioning potential to G50. Similarly, if CST20 has been reversed, it will be applying conditioning potential directly to G52. It is clear that G49, G50 and G52 are conditioned selectively according to whether the tens order digit of the column shift amount is 0, 1 or 2 respectively.

It has been explained that at completion of multiplication, the trigger D33 (Fig. 65f) is restored. Upon its restoration, it reverses a trigger D50 unless G24 (Fig. 65b) has been turned by a half correction suppression signal. If G24 is turned, line *g8* is at low potential and cutting off D29 (Fig. 65f). The output of D29 not only conditions D49 but also makes D36a conduct and block reversal of D50. If the HCS signal has not been given, D36a remains at cut-off and allows D33, upon restoration, to turn D50. D50 thereupon cuts off a tube D36. In the absence of a half correction suppression signal, and its resulting signal MHCS, tube D29 remains conductive and cutting off D28. Hence, when D36 is cut off, the couple D28—D36 is effective to condition D27. The next B pulse makes D27 conduct and reverse a trigger D26. D26 then conditions D18 to respond to A pulses. The negative A phase pulses produced by D18 are applied to a tube D17 and also to a trigger D11 which is the first stage of a five-pulse counter. D17 which receives the negative A phase pulses produces positive A phase pulses on its output line *d17*. These pulses are applied via this line to tubes G49, G50 and G52 (Fig. 65b). The conditioned one of these tubes responds and acts through a related tube to produce positive pulses on output line TCS units 10 or 20. The output line TCS units connect to control grids of the tubes HCE (Fig. 64e) associated with orders 5 to 14 of PQ. The output TCS10 goes to the tubes HCE associated with orders 15 to 24 of PQ and the output line TSC20 goes to the tubes HCE for orders 25 to 32 of PQ. In this manner one of three groups of tubes HCE receives half correction pulses, such group being selected in accordance with the tens order digit of the column shift amount. Further, only one tube in the selected group will be conditioned depending on the units order digit of the column shift amount. It follows then that only that tube HCE which is associated with the selected sub-units PQ order will be conditioned and also receive the half-correction pulses. This tube will produce negative pulses on its output line 215. This line, as already explained, leads the pulses via a capacitor to the entry tubes 216 and 217 (see Fig. 64h) for the selected sub-units PQ order. In this way the rounding off pulses are transmitted to the selected sub-units PQ order.

As described, the rounding off A-phase pulses are indirectly derived from D18 (Fig. 65f) which applies a pulse to D11 for each rounding off pulse. The first two pulses effect the turn and return of D11 and a consequent reversal of D12. The third and fourth pulses effect a repeat action of D11 and a return of D12. Upon D12 returning, it reverses D13. The fifth pulse turns D11. At this point, D11 is cutting off D20 and D13 is cutting off D20a. D20—D20a then conditions D19 to become conductive in response to the next B pulse and thereupon to return D26. With D26 returned, it renders D18 ineffective thus terminating the production of rounding off pulses. It is to be noted that upon D26 returning, it restored D50. It is clear now that the number of rounding off pulses is limited to five.

As understood, five rounding off pulses applied to a sub-units order, if this order registers 5 or higher, must produce a carry to the next higher order, which is to be the transmitted units order of PQ. This carry to the units order is the rounding off entry.

During the entries of partial products into PQ, the carry control and carry operating pulses were produced under control of the primary timer (Fig. 65h) which is now out of operation. Accordingly, during half correction operation, other means are provided to control the production of these pulses. When D26 (Fig. 65f) is in its reset status, it is maintaining C24 conductive. D26 was reversed to initiate the production of rounding off pulses and was restored to limit the rounding off pulses to five. Upon restoration of D26, it renders C24 again conductive. Upon C24 becoming conductive, it reverses C8 which then conditions C4 to produce negative A-phase pulses in response to applied A pulses. The first A-phase pulse from C4 turns C16. The second A-phase pulse from C4 returns C16 which causes C8 to return and D8 and D21 to turn. D21 in reversed condition renders D28 conductive, causing D4 to be cut off and apply a positive pulse, via connection *d4* to J19 (Fig. 65i) causing J23 to be cut off. Thereupon the output *j23* goes to increased potential with the same effect on elements 65c (Fig. 64f) as previously described in connection with the carry means. When D8 (Fig. 65f) is reversed, it acts through D16 to condition D14. The next A pulse renders D14 conductive to cut off D5. The increased potential on the output *d5* is applied to J20 (Fig. 65i) with the result that J20 becomes conductive and cuts off J24 to produce the carry operating pulse C–OP (see Fig. 64f). In the manner described before, this pulse causes the carry means to operate if carry is called for. As just described, D14 (Fig. 65f) was conditioned by reversal of D8 to become conductive in response

to an A pulse and cause the production of the carry operating pulse. Further, D14 upon becoming conductive, reverses D7. D7 then acts through D22 to condition D6. The next B pulse makes D6 conduct and turn D9 and return D8. With D9 reversed, it works through D1 to condition D3. The next A pulse renders D3 conductive to restore D7 and D21.

Upon the restoration of D21, it applies a positive going pulse by way of a capacitor to D34*a*. D34*a* becomes momentarily conductive and reverses "complete" trigger D42. As described before, the effect of reversing D42 is to cause a complete signal R–CPLT (see Fig. 65*k*) to be sent back to the sequence means. The sequence means in response, returns a result readout signal R.RO. The product is then read out in the manner described before.

14*b*. *Dividing means*

The dividing means uses much of the same structure as the multiplying means, as will become clear in the following description. The dividend, to a maximum of 14 places, will be entered from the Internal In bus columns 16 to 29 into the PQ orders 5 to 18 (see Figs. 64*h* and *j* and 66A). The divisor will be entered in MC–DR, also from Internal In bus columns 16 to 29. In dividing, the starting column shift position will be column shift position 2, so that in this position the divisor will be routed to PQ orders 18 to 31 (see Fig. 66A).

The plan of dividing is similar to that employed in application Serial No. 704,914 of Dickinson et al., filed October 22, 1946. Briefly, in each column shift position the divisor will be subtracted one or more times from the dividend or divdend remainder. Subtraction is effected by addition of the tens complement of the divisor. In order to establish the proper number of places in the complement, 9 is entered in the PQ order to the left of the order associated, in the particular column shift position, with the 14th order of MC–DR, such entry being controlled by a special circuit D–T/C (Fig. 64*c*). It is clear then that in each column shift position, a group of fifteen PQ orders will be selected to receive the complement of the divisor from the 14 orders of MC–DR and from a special true-complement control D–TC. If the divisor is smaller than the amount in PQ from which it is being subtracted, then the addition of the complement of the divisor to such an amount will result in a carry to the PQ order which is at the left of the group of 15 orders receiving the divisor and the supplemental 9. In other words, a "go" condition is manifested by a carry entry to the order at the left of the group of orders of PQ receiving the complement in a column shift position. This carry entry is, in reality, a unit quotient entry into the PQ order which is serving as the quotient receiving order in the particular column shift position. On the other hand, a "no go" condition is manifested by failure of such carry entry. It is seen then that in each column shift position, a number of carries, equal to the number of units in the quotient digit, will be applied to a quotient receiving order to the left of the group of 15 PQ orders selected in the column shift position.

Whenever a "no go" condition is found, as determined by failure of carry into the quotient receiving order, in a column shift position, then the true value of the divisor is entered into the selected group of PQ orders, thereby canceling the last complement entry and restoring the dividend or dividend remainder to its value prior to the detection of a "no go" condition. The column shift means is then advanced to its next position. There are special terminating controls for terminating the dividing operations and these controls will be explained at the proper times in the present section.

During a run of sequence for the dividing calculation, the commutator DVC (Fig. 78D) is in operation to produce control signals for the dividing calculation procedure (see Section 19). The first control signal produced by commutator DVC is the negative presense signal D–PRE. This signal cuts off H28 and H27*a* (Fig. 65*e*). At this time the interlock tube H26 is still at cutoff, so that H27*a*—H26 becomes effective to make H25 conduct and turn H29T. With H29T turned, it renders H30 non-conductive and H31 conductive. This is the reverse of the conditions of the tubes H30 and H31 during the multiplying calculation. With H31 conductive, the "up multiply" bus *my* is down in potential. With H30 nonconductive, the "up divide" bus *dv* is up in potential. The cutting off of H28 by the presense signal D–PRE has the same effect as when H28 is cut off by the presense signal M–PRE during the multiplying calculation, so far as the operation of the cancel timing circuit and the MDC cancel circuit are concerned. Briefly, when H28 is cut off it makes H19 and H20 conduct. H20 cuts off H5 so as to release H15 for reversal by now conductive H19. Upon reversal of H15 it works through H20*a* to reverse the cancel trigger H16 which causes the cancel circuit MDC to function for resetting the triggers (except those in Figs. 65*a* and *b*) in the internal commutator of the MD unit. Reversed H15 unblocks the cancel timing counter for operation and acts through H13 to condition H9 for response to the A pulses. H9 produces negative A-phase pulses for operating the cancel timing counter. The first two pulses turn and return H10, causing H11 to turn. The third and fourth pulses again turn and return H10 causing H11 to return and thereupon to turn H12. Upon H12 turning it restores the cancel trigger H16 terminating the operation of the MDC cancel circuit. The 5th and 6th pulses applied to the cancel timing counter turn and return H10 causing H11 to turn. At this point H11 and H12 are both in turned status and respectively cutting off H7*a* and H8*a*. Since the bus *my* is now down in potential it is cutting off H6*a*. The common anode line D*t* of H7*a*, H8*a* and H6*a* thus rises in potential after the cancel circuit MDC has terminated its operation. The rise in potential on D*t* is applied to E17 and E17*a* (Fig. 65*c*), causing these tubes to become conductive and to turn triggers TER1 and TER2 of the tertiary timer. With TER1 turned, the first column shift position is ineffective because the terminal CS1 is down in potential. With TER2 turned the 2nd column shift position is effective because terminal CS2 is at increased potential. It is therefore seen that during the dividing calculation the starting position for the column shift means is position 2.

To return to the operation of the cancel timing counter, the 7th and 8th pulses turn and return H10 causing H11 to restore and thereupon to reset H12. Upon H12 being reset it turns H14 and H14 thereupon renders H13*a* conductive to render H9 unresponsive to the applied A pulses so that the operation of the cancel timing counter is terminated.

In the manner to be described in Section 19, the divisor is applied to the Internal In bus columns 16 to 29 and its sign is applied to column 1. The operational sign for the divisor is applied to lines *1s* and *2s* in Fig. 65*j*. Shortly thereafter, the commutator DVC (Fig. 78D) emits the second signal DRC. This signal goes to the same line in Fig. 64*a* as the signal MCC did during multiplication. The application of the signal DRC to this line results in the MC/DR cancel circuit resetting register MC–DR and the MC/DR sign mixing circuit (Fig. 65*j*) as explained in Section 14*a*.

The third signal from commutator DVC is the signal DR–RI, which occurs after termination of the cancel signal DRC. The signal DR–RI is applied to the same line in Fig. 64*a* as the signal MC–RI was applied during multiplication and causes entry of the divisor into register MC–DR (Fig. 64*b*) in the manner described in Section 14*a*. The signal DR–RI is also applied in Fig. 65*j* to the same line as the signal MC–RI was applied during multiplication and results in the entry of the input sign and operational sign for the divisor into the MC/DR sign mixing circuit. Following the entry operations controlled by the signal DR–RI, the divisor, the divisor sign and operational sign are removed from the Internal bus-sets and from lines *1s* and *2s* (Fig. 65*j*). Thereafter the dividend is applied to Internal bus columns 16 to 29, its sign is applied to Internal bus column 1, and its operational sign is applied to lines *1s* and *2s*.

Shortly thereafter the 4th signal DDC is produced by commutator DVC (Fig. 78D) and is applied to the same line as the signal PQC (Fig. 65*k*) was applied during multiplication and causes resetting of the register PQ (Fig. 64*h*). With respect to the dividing calculation, the signal DDC, also cuts off **32**, Fig. 65*j*. During dividing, the line *my* is at reduced potential and cutting off **25**—65*j*. Hence, the couple **32**—**25** renders **25***a* conductive so as to cut off the tube **28**, to the same effect as when this tube was cut off by the signal MPC during multiplication; i. e. to the effect of resetting the MP/DD sign mixing circuit.

The fifth signal from commutator DVC (Fig. 78D) is the signal DD–RI, which occurs after the termination of the cancel signal DDC. The signal DD–RI cuts off **30**—65*j*, with the same effect as when this tube was cut off by the entry signal MP–RI during the multiplying calculation; i. e., with the effect of entering the number sign and the operational sign of the dividend into the MP/DD sign mixing circuit.

As already explained, the dividend amount is present now on the Internal bus columns 16 to 29 and is represented by increased potentials selectively applied to the buses of the Internal In bus columns. Reference to Fig. 66*a* indicates that the dividend will be applied by these bus columns to orders 5 to 18 of register PQ. Fig. 64*j* shows, as typical, the dividend entry means for PQ orders 5 and 18 which are respectively associated with the Internal In bus columns 29 and 16. The dividend entry means for each of orders 5 to 18 of PQ is similar to the entry means for the registers MC–DR and MP. Briefly, the dividend entry means for a PQ order includes four tubes DDI**8**, **4**, **2** and **1** which have their suppressors connected to buses **8**, **4**, **2** and **1** respectively of the related Internal In bus column. The plates of the tubes DDI**8**, **4**, **2** and **1** are capacitatively coupled to the grids of tubes DDE**8**, **4**, **2** and **1**, respectively. The outputs DDEP of the tubes DDE, associated with a PQ order are connected to the terminals *gr* of the triggers **8**, **4**, **2** and **1** in the PQ order, as shown for PQ order 18 in Fig. 64*h*. Accordingly, the triggers will be reversed upon the connected tubes DDE being cut off, in the manner explained for the tube E in Fig. 10.

It is evident that at the time the signal DD–RI is produced by the commutator DVC, the tubes DDI are already selectively conditioned in accordance with the dividend factor. The signal DD–RI cuts off **3**, Fig. 64*j*. At this time the interlock line *d***51** still is at reduced potential and cutting off **2**, Fig. 64*j*. Accordingly, the couple **2**—**3** is effective to render **1** conductive, causing **4** and **5**, in parallel, to be cut off and to apply increased potential to the control grids of all the tubes DDI. Those tubes DDI which have been conditioned in accordance with the dividend factor become conductive and cut off the associated tubes DDE. As a result the dividend factor is entered into PQ orders 5 to 18.

The sixth signal from commutator DVC (Fig. 78D) is the start signal DV–ST which occurs after termination of the dividend entry signal DD–RI. The signal DV–ST is applied to the tube D**31***a* in Fig. 65*f* to which tube the start signal MY–ST was applied during the multiplying calculation. As explained in Section 14*a* the start signal results in the reversal of D**30** which causes reversal of D**37** which in turn reverses D**43**. D**43** cuts off D**51** so that the interlock line *d***51** rises in potential. Reversed D**37** conditions D**46**. The next A pulse causes D**46** to turn D**45** which thereupon conditions D**38** and D**35**. The next B pulse makes D**38** conduct to reverse D**37** which thereupon conditions D**44** to respond to the next A pulse, so as to restore D**45**. The same B pulse which operated D**38** also operated D**35** during the interval in which D**45** was reversed and conditioned both these tubes D**38** and D**35**. The operation of D**35** reverses the main start trigger D**33**. D**33** now turned, renders D**41** conductive to apply reduced potential to line *d***41**. As in multiplication, the reduced potential on *d***41** cuts off B**43** (Fig. 65*g*). During multiplication the line *dv* was at low potential and cutting off B**34**, so that when B**43** was cut off, the tube B**27** was conditioned to produce A-phase pulses. B**27** was therefore effective to cause the production of the pulses MPR which were applied to the input tubes MP–EN (Fig. 64*b*) successively operable, in the sequential column shift positions, to invert the pulses MPR to rolling pulses for the related MP orders. Further, the pulses produced by B**27** were effective to drive the secondary timer (Fig. 65*g*). During the dividing calculation, the line *dv* is at high potential so that B**34** is conductive and prevents the conditioning of B**27**. Hence rolling pulses will not be applied to the MP orders and the secondary timer also will remain idle during the dividing calculation.

The reduced potential on the line *d***41**, resulting from the turning of start trigger D**33** (Fig. 65*f*) is effective also to cut off B**51** (Fig. 65*g*). During multiplication the line *my* was at high potential and rendering B**51***a* conductive so that the couple B**51**—B**51***a* was ineffective. During the dividing calculation the line *my* is at low potential and cutting off B**51***a*. Accordingly, when B**51** is cut off, upon the turning of the start trigger D**33**, the couple B**51**—B**51***a* is effective to condition B**50** to

respond to A pulses. B50 produces negative A-phase pulses which cause B41 to apply positive A-phase pulses to parallel tubes B25 and B33. These tubes, in turn apply negative A-phase pulses to the input line PRI for the primary timer (Fig. 65*h*). It is seen therefore that during the dividing calculation, the primary timer is placed in operation upon the turning of the main start trigger resulting from the receipt of the start signal DV–ST by the internal commutator of the MD section.

In multiplication the line *my* is at high potential. Accordingly, J8, Fig. 65*i*, is conductive so that J4 is cut off and the line TR is at increased potential. With line TR at increased potential it should be noted that J3 is conductive and its output line COMP is at reduced potential. The line TR, when at increased potential, controls the true-complement means shown in Fig. 64*c* for causing transfer of the true number in MC–DR to PQ. As explained in Section 14*a* on multiplication, the line TR when at high potential conditions the tubes 211 and 220 in Fig. 64*c*. With the tube 211 conditioned the carry-out pulse from the related order of MC–DR is effective to render 211 conductive and thereby to turn the associated true-complement trigger TC. This permits the tube 208 to pass through a number of pulses MC–RB equal to the true value of the digit standing in the MC–DR order. Further, with line TR at high potential and conditioning tubes 220, a pulse at "10.5" of the primary cycle is effective to render the tubes 220 conductive so as to restore all the triggers TC. In the dividing calculation, the line *my* is at reduced potential. Accordingly, J8, Fig. 65*i*, is at cut-off. Initially, and whenever trigger J7 is in the shown status, it is cutting off J8*a*. Accordingly, with J8 also at cut-off, the couple J8—J8*a* is effective to render J4 conductive. Consequently, the line TR is at reduced potential while the line COMP is at increased potential. With the line TR at reduced potential, the true number transfer from MC–DR to PQ cannot take place. With the line COMP at increased potential, it is conditioning the true-complement means in Fig. 64*c* to allow a complement transfer from MC–DR to PQ to be effected. As indicated in Fig. 64*c*, when line COMP is at increased potential it is conditioning the tubes 212 and 225 which control triggers TC relating to orders 1 to 14 of MC–DR. Also, line COMP is conditioning tubes 225 and 220B which control the additional trigger D–T/C. This is the situation prior to the beginning of the first primary cycle which is initiated, in the manner explained before, as a result of the start signal DV–ST. At "0" of the primary cycle, in response to the first input pulse on the line PRI (Fig. 65*h*), the primary stage PR13 is reversed and upon its reversal, turns stage PR0. Upon PR0 turning, it applies a positive pulse to the control grid of A18 which at this time is conditioned under control of trigger A11. Accordingly, A18 becomes conductive at "0" and through a coupling capacitor applies a negative pulse to A17 which in response produces a positive "0" pulse on line *a*17. This pulse is applied to the conditioned tube 225 associated with the first order of MC–DR (see Figs. 64*b* and *c*). This first order tube 225 becomes conductive and acts through the anode resistor of 211 to turn the first order true-complement trigger TC. As a result the related tube 208 is conditioned at "0" to pass the pulses MC–RB which are produced in the manner described in Section 14*a* during the primary cycle and briefly reviewed below.

When A18 become conductive at "0" it turned A–5 which conditioned A3 to pass B pulses. These pulses are inverted by A1 to the positive MC–RB pulses (see Fig. 66). At the "10" time of the cycle A5 will be restored. Accordingly, ten pulses MC–RB will be produced beginning with "0.5." These pulses, as now understood, are applied to the tubes 208 (Fig. 64*c*).

During the turned interval of PR0 (Fig. 65*h*) it conditions A19 to become conductive in response to the next B pulse at 0.5 and thereupon to turn A11 and A12. With the turning of A11, A18 is deconditioned. All, when turned, condition A10 to be made conductive by the next A pulse at "1." A10 thereupon applies a pulse by way of a capacitor to A9 which produces a positive "1" pulse. This pulse is applied to the tubes 225 associated with orders 2 to 14 of MC–DR and also to the tube 225 associated with the special true-complement trigger D–T/C. Since these tubes 225 are now conditioned by the increased potential on line COMP, they become conductive and act through the anode resistors of the related tubes 211 to turn the triggers TC (of orders 2 to 14) and the trigger D–T/C. As is now understood the first order trigger TC is turned at "0" while the other order triggers and the special trigger are turned at "1." Accordingly, the first order tube 208 will start passing the MC–RB pulses at "0.5" while the other tubes 208 will start passing these pulses at "1.5." A maximum of ten pulses may thus be passed through by the first order trigger 208 while a maximum of nine pulses may be passed through by each of the other tubes 208.

It has been explained that trigger A12 (Fig. 65*h*) was turned at "0.5." With A12 turned, it conditions A13 to pass A pulses to A14 which produces the positive pulses MC–RA. The trigger A12 will be returned at "10.5." Hence, ten pulses MC–RA will be produced starting with "1." As previously explained in Section 14*a* these pulses are applied to tubes 209 for causing these tubes to apply rolling pulses to the orders of MC–DR. In response to these pulses, each order of MC–DR will produce a carry out pulse at a time of the cycle which corresponds to the tens complement of the digit initially standing in the order. The carry-out pulse is transmitted by the output line 210 of the order to the control grids of the tubes 211 and 212 for the same order. Since, at this time, the tubes 212 of all the orders are conditioned, such tube, upon receiving the positive pulse on line 210 will become conductive and restore the trigger TC. This terminates the conditioning of the related tube 208 so as to cease passing the pulses MC–RB. In this manner, a number of pulses will be passed by the first order 208 equal to the tens complement of the digit standing in the first order MC–DR, while the other order tubes 208 will pass through numbers of pulses MC–RB equivalent to the nines complements of the digits standing in these other orders. It should be noted that with respect to the special trigger D–T/C it remains reversed until "10.5" of the cycle at which time a pulse is applied to the tube 220B which is conditioned by the increased potential on line COMP and causes the tube to become conductive and reset the trigger D–T/C. In the interval in which this trigger is reversed, its related tube 208 passes nine pulses. The pulses passed through by the tubes 208 are

inverted by 213 to positive pulses on the lines C1 to C15 to be applied to the rows of tubes C1T to C15T. As explained in Section 14*a* successive tubes of each of these sets of tubes are conditioned in the sequential column shift positions. In the starting column shift position 2 for the dividing calculation, the tubes C1T–2 to C15T–2 are conditioned (see Fig. 66A). These tubes will cause the entry of the complement of the divisor, as represented by the pulses applied to these tubes, to be entered in PQ orders 18 to 32.

As was previously explained, when the divisor is smaller than the dividend now present in PQ orders 5 to 18, the addition of the tens complement of the divisor to the dividend results in a carry, corresponding to a unit of the quotient, from the highest order of the group of 15 in PQ receiving the divisor complement in the column shift position, to the quotient receiving order at the left. Thus, in column shift position 2, the selected group of PQ orders is the group of orders 18 to 32 and the quotient order is the 33rd order of PQ.

The carry operations will take place in the manner explained before in Section 14*a*.

In each column shift position as many cycles of complement entries of the divisor into the group of 15 selected PQ orders will take place as the number of times the divisor goes into the dividend or dividend remainder. For each "go" condition, a carry entry will be made to the PQ order to the left of the group of 15 receiving the divisor complement, and the total of these carry entries will make up the quotient digit obtained in the column shift position. As long as "go" conditions are present in a column shift position, the highest order of the group of 15 orders of PQ receiving the divisor complement will produce a carry pulse as now understood. This pulse occurs at the "12" time in response to the carry operating pulse C–OP which is produced in the manner explained in Section 14*a*. Briefly, the pulse C–OP is produced in response to a "12" pulse appearing on the line *a*55 (see Figs. 65*h* and 65*i*). The pulse on line *a*55 renders J20*a* conductive causing J24 to be cut off and produce the pulse C–OP.

It is clear that the digit entries are completed before "10" of the cycle. At the "10" time of the cycle a "10" pulse is derived from A16 (Fig 65*h*) and transmitted via line *a*16 to J9 (Fig. 65*i*) rendering the latter conductive so as to reverse a trigger J14. If a carry out from the highest order of the group of 15 in PQ receiving the divisor in a column shift position occurs, then J14 will be returned and will not cause a shift from complement to true transfer operations in the next primary cycle, but if a carry out is not produced from said highest order of the group of 15, J14 will remain in reversed status and will condition J10 to respond to a "13" pulse on the line *a*50. This pulse is produced on line *a*50 in the manner described in Section 14*a* and upon its application to conditioned J10 causes J10 to conduct and reverse J7. The effect of the reversal of J7 will be explained soon. To provide for the control of J14 in accordance with the carry out condition from the highest order of the group of 15 receiving a divisor complement in a column shift position, the following means are used. Referring to Fig. 64*f* there are a plurality of tubes 230, one for each order of PQ. These tubes are successively conditioned in the sequential column shift positions; that is, the tubes 230 associated with orders 32 to 4 of PQ are successively conditioned in column shift positions 2 to 30. In starting column shift position 2 for division, the tube 230 associated with PQ order 32 is thus conditioned by connection of its suppressor to the terminal CS2. Assuming that there is a "go" condition in column shift position 2, the carry trigger K32 will be reversed sometime before "10" of the cycle and thereby will apply increased potential, via line *kf*, to the control grid of the tube 230—32, now conditioned. As previously described in Section 14*a* the triggers K are not restored until "13" of the cycle. Hence, the tube 230—32 will remain conductive until "13" and the common output line, *j*13 of the tubes 230 will be at decreased potential. Referring to Fig. 65*i* with line *j*13 at decreased potential, it is cutting off J13. Therefore, J13 is applying conditioning potential to J17. At the "12" time of the cycle a pulse appears on *a*55 in order to cause the carry pulse C–OP to be produced as previously described. This "12" pulse is also applied via a capacitor to J17 and if the latter has been conditioned in the manner just described, it becomes conductive and restores J14. Accordingly, J7 will not be reversed at the "13" time.

Assuming that there is a "no go" condition, say in column shift position 2, then trigger K32 (Fig. 64*g*) will not be reversed and will not render now-conditioned tube 230—32 (Fig. 64*f*) conductive. Accordingly, J13 (Fig. 65*i*) will be maintained at effective control grid potential. The suppressor of J13 is at increased potential under control of the line COMP, during a cycle in which a complement entry is being effected into PQ. Thus, in the absence of a carry from the highest order of the group of fifteen selected in a column shift position, J13 will be conductive and will decondition J17 so that it will not respond to the "12" pulse on line *a*55. Accordingly, J14 will remain in the reversed condition in which it has been put by the "10" pulse on line *a*16. With J14 in reversed status it enables J10 to be rendered conductive by the "13" pulse on line *a*50 and thereupon to reverse J7. Upon reversal of J7 it applies a positive pulse by way of a capacitor to the tube J2 causing the latter to produce a negative pulse on line *j*2. This negative pulse is applied via a capacitor to the control grid of C27 (Fig. 65*e*). C27 is conditioned during dividing by increased potential on its suppressor which is connected to the "up divide" line. However, C27 is cut off by the negative bias on its control grid, and the negative pulse from line *j*2, therefore, has no effect.

When J7 (Fig. 65*i*) is turned, as previously described, it also makes J8*a* conductive, causing J4 to be cut off which in turn renders J3 conductive. Accordingly, the line TR is increased in potential while the line COMP is dropped in potential. This is the condition for a true number transfer from MC–DR to PQ and such true number transfer will occur in the next primary cycle and will cancel the last complement entry of the divisor into the selected group of 15 PQ orders in the column shift position.

Further, when J7 is reversed, it applies increased potential to the control grid of J6. During the dividing calculation the suppressor of J6 is held at increased potential by the "up divide" line. Accordingly, when J6 has increased control grid potential applied thereto, it becomes conductive and cuts off J1 so that the output *j*1 is

brought to increased potential. Referring to Fig. 64*f*, the output *j1* connects to the control grids of tubes **231** of which there is one for each PQ order except the 33rd order. The tubes **231** related to the PQ orders, in descending succession, are conditioned sequentially in the successive column shift positions in the same manner as explained for the tubes **230**. Thus, in column shift position 2, the tube **231—32** is conditioned as well as the tube **230—232**. Hence, if in column position 2, a "no go" condition is found, so that in the manner described, the output *j1* is at increased potential, the conditioned tube **231—32** will be rendered conductive and its output **232** will be at decreased potential. As a result the tube **65d** (Fig. 64*g*) of the associated order 32 will be cut off for a reason which will be explained below. Also the decreased potential on line **232** cuts off a tube **233**, rendering the tube **234** conductive to block the reversal of the related trigger **K32**.

The conditions have now been set up for a true number transfer of the divisor from MC—DR into PQ during the next primary cycle. The addition of the true divisor to the amount now in PQ necessarily will result in a carry from the highest order of the group of 15 selected in the column shift position, unless provision were made to suppress such carry. It is evident that if a carry were permitted to occur, it would add a unit to the quotient digit and this is only desired as a result of a "go" condition which is not the case when the true divisor is entered into PQ. The carry from the highest order of the selected group of 15 is suppressed because tube **234** (Fig. 64*g*) related to this order is being kept conductive under control of a tube **231** (Fig. 64*f*), as explained before. Since **234** remains conductive, it blocks reversal of K (Fig. 64*g*) controlled by this highest order. In the explanation of the carry means, it was pointed out that if an order stood at 9 and a preceding order went from 9 to 0 during the entry period of a cycle, then the group of tubes **65**, **65***a*, **65***b* and **65***c* (Fig. 64*f*) associated with the order at 9 would be effective to apply increased potential to the control grid of a related tube **65***d* (Fig. 64*g*), so that the latter would produce a negative pulse reversing trigger K of the higher order. This same negative pulse also is applied to the tube **65***b* of the still higher order and cuts off this tube. Should this latter order also be at 9, its trigger K would be reversed. During a cycle in which transfer is being effected of a true divisor to PQ, the line **232** associated with the highest order of the group of 15 receiving the divisor is at low potential, as previously described and effective via **233** and **234** to prevent reversal of the related carry trigger K. This, of itself, would not be enough to prevent a carry entry into the quotient order, if the latter stood at 9. The highest order of the selected group of 15 would inevitably pass through 9 during the true add cycle. If a preceding order goes from 9 to 0 at that time or prior thereto in the cycle, then the tubes **65**, **65***a*, **65***b* and **65***c* of said highest order would, unless prevented, render tube **65***d* of this order conductive. Although this would not reverse the trigger K of this highest order, which trigger now is blocked by the conductive tube **234**, the tube **65***b* of the quotient order (the order above the selected group of 15) would be cut off. If the quotient order stood at 9, then its trigger K would be reversed and the net effect would be to effect a carry entry into the quotient order. This same effect would be produced in as many successive higher quotient orders as stood at 9. It is for this reason that, during the true add cycle, the carry suppression line **232** not only is connected to tube **233** to cause tube **234** to block reversal of the trigger K of the highest order group of 15, but is also connected to the suppressor of **65***d* associated with this highest order. This tube **65***d* therefore is held at cut-off to prevent its pulsing tube **65***b* of the quotient order. In other words, if it should happen that the quotient receiving order above said highest order in the selected group of 15 is at 9, during the true add cycle, then the carry-through-9 to this quotient order will not be effected. This prevents an incorrect quotient from being registered.

At "12" of the true add cycle, a positive pulse again appears on line *a*55 and is applied via a capacitor to the control grid of **J17** (Fig. 65*i*). Although the line *j13* (Fig. 64*f*) remains at high potential and does not manifest a carry from the highest order of the selected group of 15, during the true add cycle, the tube **J13** (Fig. 65*i*) is at cut-off because the connected line **COMP** is now at low potential. Accordingly, **J13** is nonconductive and conditioning **J17** at the time that the "12" pulse is applied thereto. Hence, **J17** becomes conductive and returns **J14** which was reversed as a result of a "no go" condition detected during the complement add cycle preceding a true add cycle. Since **J14** is now returned, it is deconditioning **J10** and instead is conditioning **J11**. Therefore, the "13" pulse on line *a*50 is effective to render **J11** conductive so as to restore **J1**. Upon restoration of **J1** it cuts off **J8***a*, so that **J8—J8***a* is then effective via **J4** to return the line **TR** to reduced potential and the line **COMP** to increased potential. This is the condition for a complement entry which will be effected in the next cycle. Further with **J1** returned, it is deconditioning **J6** so that the line *j1* will not be at high potential and carry suppression will not occur during the ensuing complement add cycle. Still further, upon the return of **J1**, it applies a negative pulse to **J2** which in turn sends out a positive pulse along line *y2* to the tube **C21** (Fig. 65*e*). This tube, being only conditioned during dividing, becomes conductive and cuts off **C22** so as to cause **C21** and **C25** to produce a negative pulse CSS on the input line ter of the tertiary (column shift) timer, thereby advancing the column shift means to its next position. Accordingly, during the next and following cycle or cycles the divisor will be transferred to a group of 15 PQ orders to the right of the group of 15 orders selected in the preceding column shift position.

It should be noted that each time a pulse CSS is produced as a result of **C21** and **C25** being made conductive by **C22** being cut off, a tube **C26** also is made conductive to produce a negative pulse HCCTR for a reason which will be made clear later.

When column shift position 19 is reached, the divisor entry will be made into PQ orders 1 to 15 (see Fig. 66A). In the next column shift position 20, the divisor will be entered in PQ orders 1 to 14 so that the units order digit of the divisor will be lost. This makes no appreciable difference in the ultimate quotient result because at best only a 19-place quotient will eventually be sent to a receiving unit, namely an electronic storage unit. Since the maximum size of the dividend is 14 places, it is evident that the maximum number of places in the in-

tegral portion of a quotient is 14. The integral 14-place portion of the quotient will stand in PQ orders 20 to 33. During the entry of a quotient digit into PQ order 20, the column shift means will be in position 15. It follows that the quotient digits obtained in the lower PQ orders will be the digits of a decimal fraction. In column shift position 20, the quotient receiving order is order 15, which means that the quotient digit in order 15 is of magnitude $k10^{-5}$. Thus, any possible error resulting from the dropping of the units order of the divisor from consideration in the dividing operation in column shift position 20 will make no appreciable difference in the ultimate quotient result. It is clear further that in column shift position 21, the units and tens places of the divisor will be dropped from consideration in the dividing operation and so on for the successive column shift positions, as far as column shift position 30 where only the four highest orders of the divisor will be used in the dividing calculation. However, to minimize the error, no matter how inappreciable, in dropping the lower places of the divisor during the successive column shift positions starting from column shift position 20, the tens complement of the remaining portions of the divisor are entered during the complement add cycles. As long as the units digit of the divisor is being transferred to a PQ order, the tens complement of the divisor is taken care of by reversing the trigger TC (Fig. 64*c*) associated with the first order of MC–DR, at the "0" time of the complement add cycle. After the units place of the divisor is dropped from consideration in the dividing operations, the tens complement of the remaining portion of the divisor is taken care of by an elusive one circuit. Referring to Fig. 64*e*, when column shift position 20 is reached, the increased potential on column shift line CS20 is effective to render a tube 240 conductive thereby reversing a trigger 241. This trigger will remain in reversed status until reset under control of the cancel circuit MDC (Fig. 65*e*) at the beginning of the next multiplying or dividing calculation. With trigger 241 (Fig. 64*e*) reversed, it is cutting off 242. During the complement add cycles, the line TR is at reduced potential, as now understood. This line has a connection to the tube 243 and cuts it off. The couple 242—243 is therefore effective to condition 244 during complement cycles occurring in the 20th and further column shift positions. With 244 conditioned it is responsive to a "0" pulse on line *a*17 and becomes conductive so as to apply a negative pulse to the first order line 215—1. This line carries the negative pulse to the tube 216 (Fig. 64*h*) associated with the first PQ order, causing the latter to be cut off. As a result the related tube 217 becomes conductive and applies the elusive one entry pulse to the first order of the PQ register.

The sign mixing operations for the dividing calculation are the same as for the multiplying calculation and need not be described. The termination of the dividing calculation is under control of a column shift number registering counter DCS (Fig. 65*a*). The control varies according to whether or not half correction is called for. Termination of the dividing calculation also may be effected under control of a so-called disappearing divisor detecting means. When the divisor has been shifted so far to the right that the portion thereof which is entering into PQ orders is zero, successive carries will be effected to the quotient receiving order in the particular column shift position and a "no carry" condition will not be reached. In other words, if the divisor is 0 its tens complement will be entered and will produce a carry into the quotient receiving order. Actually, this will be produced in the following manner. Ten pulses will be applied to the first order of PQ and nine pulses will be applied to the orders to the left of the first order. Since the first order goes through a value cycle, in response to the ten applied pulses, carries will be effected to the succeeding higher orders and each of these will be advanced to 0, with the result that the highest order of the group of selected orders in the column shift position will go from 9 to 0 and produce a carry into the quotient receiving order. If this occurs 13 times in succession, i. e. during 13 successive complement add cycles in a column shift position, then it is a manifestation of a disappearing divisor. In order to count the number of complement add cycles occurring in a column shift position, a counter shown in Fig. 65*e* is used. During the complement add cycle the line COMP is at high potential and renders C2 Fig. 65*e*, conductive thereby cutting off C6, C6*a*, C7 and C7*a* so as to release triggers C9, C10, C11 and C12 of the counter for operation. The increased potential on line COMP is also effective to condition the entry tube C15*b*. At the "10" point of each cycle a pulse is applied to conditioned C15*b* to cause it to apply an entry pulse to C9. In the now familiar manner every two entry pulses will turn and return C9 causing it to reverse C10. Every two reversals of C10 will reverse C11 while every two reversals of C11 will reverse C12. When 12 entry pulses have been applied to C9, then C11 and C12 will be in reversed condition while C9 and C10 will be in cancelled condition. With C12 and C11 reversed, they are cutting off C15 and C15*a* respectively so as to cause C15—C15*a* to condition C14. Upon the reversal of C9 in response to the 13th entry pulse, it applies a positive pulse via a capacitor to C14 causing it to become conductive and thereby to apply a negative pulse by way of the anode resistor of C19 to line *c*19. This pulse is effective to restore the main start trigger D33 with the effect of terminating the calculation if half correction is not called for. If half correction is called for, the return of D33 conditions the MD section for terminating the calculation after the half correction has been made, all as explained in Section 14*a*.

In Section 14*a*, the entry of the denominational shift number from lines MMN (Fig. 65*a*) into the triggers CST was explained. The same entry occurs during the dividing calculation but, in addition, the denominational shift number is also entered into a counter DCS. If half correction is not called for then the number of steps of dividing column shift will be equal to 28 minus the denominational shift number in the counter DCS. If half correction is called for then the number of steps of dividing column shift will be one greater than when half correction is suppressed.

The denominational shift number is represented by increased potentials selectively present on the lines MMN (Fig. 65*a*). In addition to the increased potentials on the lines MMN1, 2, 4, 8, 10 and 20 selectively conditioning the tubes CSA, they also condition tubes CSD1, 2, 4, 8, 10

and G16, respectively. When the divisor entry signal DR–RI is produced by the control commutator DVC (Fig. 78D), it is applied in Fig. 65*a* to the same line as the signal MC–RI was applied during multiplication. The signal DR–RI causes the tubes 64, 64*a*, 63 and 53 in Fig. 65*a* to produce a positive pulse for operating the conditioned ones of the tubes CSA and CSD. The tubes CSA control the entry of the denominational shift number into the triggers CST to select the PQ order to receive the half correction pulses, as described in Section 14*a*. The tubes CSD1, 2, 4, 8, 10 and 20 respectively control stages 1, 2, 4, 8, 10 and 20 of the counter DCS. This counter includes, as its first order, a decade counter which is constructed as a register device (see Section 5 and Figs. 15 and 15*a*) and also includes as its higher order, two additional stages 10 and 20. Upon a tube CSD becoming conductive it reverses the correspondingly numbered stage of the counter DCS, so that this counter stores the denominational shift number taken from main sequence.

It was mentioned before that each time a pulse CSS is applied to the input line ter of the tertiary timer to advance the dividing column shift position by 1, the tube C26 (Fig. 65*e*) produces a negative pulse HC.CTR. This pulse is applied via line c26 to the input of the counter DCS (Fig. 65*a*) advancing it by one count step. Since the counter has been set with a count equal to the number of denominational shift steps to be effected by the denominational shift unit (Section 12), each of the input pulses increases this count by one. When the total count is 28, the stages 8 and 20 are reversed status. Stage 8 then acts to apply cut-off potential by way of a connection 848*a* to a tube G48*a* in Fig. 65*b*. When stage 20 of the counter is reversed, it applies cut-off potential via a connection 2048 to the tube G48 in Fig. 65*b*. Thus, when the count in DCS is 28, both tubes G48 and G48*a* are at cut-off. If half correction is being suppressed, then a signal HCS has been received prior to the start of the dividing calculation by the tube G40. At this time the interlock line *d*5*f* is still at cut-off potential. Accordingly, G40—G40*a* become effective upon receipt of the suppression signal HCS to render G32 conductive for reversing trigger G24. With G24 reversed, it cuts off G16. Hence, when G48 and G48*a* are also cut off the common anode line of the latter two tubes and G16 rises in potential and the rise in potential is supplied by way of a connection *c*20 to the control grid of the tube C20 (Fig. 65*e*). This tube is continuously conditioned during the dividing calculation because its suppressor is connected to the "up divide" line and when the tube C20 receives increased potential on its control grid, it becomes conductive and applies a negative impulse by way of the anode resistor of tube C19 to the line *c*19. Accordingly, the main start trigger D33 (Fig. 65*f*) is restored. The restoration of this trigger brings about the termination of the dividing calculation in the same way as explained in Section 14*a* for the multiplying calculation, when half correction is suppressed. It is evident from the foregoing explanation that when the number of steps of dividing column shift plus the denominational shift number in the counter DCS (Fig. 65*a*) equal 28, the dividing calculation will be terminated provided half correction is being suppressed. If half correction is not suppressed, then the trigger G24 (Fig. 65*b*) remains in its cancelled status and does not cut off G16. Each time stage 1 of the counter DCS (Fig. 65*a*) is reversed, it applies cut-off potential by way of a connection 116 to the tube G16. When the count is 28 the tubes G48 and G48*a* are cut off in the manner explained before. Upon the application of the next pulse HC.CTR to the counter, stage 1 is reversed and thereupon cuts off G16. It is evident, therefore, that if half correction is not being suppressed, then the common anode line *c*20 of G48, G48*a* and G10 rises in potential when the sum of the denominational shift number and the number of dividing column shift steps equal 29. The increased potential on the line *c*20 (Fig. 65*b*) results in tube C20 (Fig. 65*e*) becoming conductive and causing restoration of main start trigger D33 (Fig. 65*f*). As a result the dividing calculation will terminate after half correction has been effected, in the same manner as has been described for the multiplying calculation in Section 14*a*.

Fig. 68 illustrates the mathematics of an extremely simple example of division, in which the quotient is to be half-corrected and shifted by the denominational shift unit 24 places to the right.

15. *The pilot units*

There are eight pilot units numbered 1 to 8 as indicated in Figs. 1, 81*a* and 81*b*. Pilot units 1 to 8 respectively control electronic storage units ES1 to 8 (see Section 6 and Figs. 20, 21 and 22). Each of these pilot units is alike and it is sufficient to show the circuit of one of the pilot units in Figs. 80*a* to *e*. All timing signals required by an electronic storage unit are generated in its controlling pilot unit. These signals are Out to ES (also see Fig. 80*a*), ES to Int, ESC, Int to ES, and ES to In (see Fig. 80*c*). Functions of these signals have been explained before in Section 6 and will be further mentioned in subsequent sections. A pilot unit also sends out a move signal SMS (see Fig. 80*a*) to bus 82 of the correspondingly numbered Out bus-set. This move signal controls the stepping of a selected tape storage station, after it has transmitted its data to the Out bus-set, as explained in Section 9. A pilot unit also produces a Reset signal (see Fig. 80*c*) upon the bus 82 of the correspondingly numbered In bus-set. This Reset signal controls the resetting of the selected receiving unit which in this case is a relay storage unit, as described in Section 7. A pilot unit receives a Forward signal (Fig. 80*b*) from bus 81 of the Out bus-set. This signal notifies the pilot unit that the data source which has been selected to read out to an Out bus-set is ready to send its data along this Out bus-set to the correspondingly numbered electronic storage unit. A pilot unit also receives a Back signal (Fig. 80*c*) via bus 81 of the corresponding In bus-set from a selected data receiving unit, such as a relay storage unit. This Back signal notifies the pilot unit that the selected receiving unit is prepared to receive data.

The pilot units may be set to pilot sequence data or arithmetical data. As now understood, two of the electronic storage units are assigned to sequence data and their corresponding pilot units are set to pilot sequence data. To selectively condition a pilot unit for sequence data or arithmetical data, five manual switches 1SQ to 5SQ are provided in each pilot unit. If the pilot unit is used for sequence data, its switches are set to the seq positions but if used for arithmetical data, the switches are set to norm positions.

The pilot units for piloting arithmetical data are selected by the program means according to the code numbers in sub-fields *b* of fields P, Q, R, T, U and V. The selection of the pilot units is effective through pilot units selection trees shown in Figs. 54 to 58.

There are five pilot units selection sequence circuits shown in Figs. 54 to 58. The functions of these circuits are roughly indicated by their titles. The OC–Out to ES trees (Fig. 54) and the OC–ES to Int are controlled by the Out fields, while the IC-Presense trees (Fig. 55), IC–ES to In trees (Fig. 56), and the IC-Int to ES trees (Fig. 58) all are controlled by the In fields.

The pilot units selection trees are heated in a manner described in Section 16*b* (items 15*b* and 39) at which times the outputs of tubes connected to selected branches of these trees are brought to low anode potentials.

The trees OC-Out to ES (Fig. 54) have eight outputs which are designated OCO with an appended digit 1 to 8 to denote the pilot units to which these outputs are connected and which are seletced thereby. These outputs may be called tree signals and go to tubes 12–5CP (Fig. 80*e*) of the correspondingly numbered pilot units, cutting off these tubes. Subsequently, the main commutator (Sections 16*a*, *b* and 17) produces a sensing signal OCO for cutting off the tubes 12*a* in 5CP of all the pilot units. The pilot units which have been selected by their tubes 12 in 5CP being cut off by tree signals OCO will thereby be rendered effective to initiate operations leading to the production of the Out to ES signals, several of which may occur simultaneously.

The OC–ES to Int trees (Fig. 57) produce nine separate tree signals designated Pb0 to 8, Qb0 to 8, Rb0 to 8, Tb0 to 8, Ub0 to 8 and Vb0. These signals go to the correspondingly numbered pilot units except for the signals having the appended digit 0 which go to a blank code chassis (Fig. 78L). The signals Pb1 to 8 cut off the tubes 2*a*–5CP (Fig. 80*e*) of pilot units 1 to 8 respectively. Similarly, the Qb1 to 8 signals cut off tubes 3*a*; the signals R*b* cut off tubes 5*a*; the signals T*b* cut off tubes 6*a* and the signals U*b* cut off tubes 8*a*. Subsequently, the main commutator may produce in succession any of the scanning signals P1, Q1, R1, T1 and U1 which cut off the tubes 2, 3, 5, 6 and 8, respectively, of all the pilot units. For example, under control of the scanning signal P1 (note Fig. 80*e*) and under further control of the signal Pb1, the tubes 2 and 2*a* of pilot unit 1 are cut off and through 1*a* and 1 produce a signal OC Int which enters into the production of a signal ES1 to Int by this pilot unit. Signals Q1 and Qb1 are mixed by couple 3—3*a* which acts via 4 and 1 to produce the signal OC Int in pilot unit 1. Signals R1 and Rb1 are mixed by couple 5—5*a* to act via 4*a* to produce this signal OC Int. Signals T1 and Tb1 act on couple 6—6*a* to cause 7 and 1 to produce this signal OC Int. Signals U1 and Ub1 are mixed by 8—8*a* which via 7*a* and 1 produces this signal OC Int.

The IC presense trees (Fig. 55) control the production of signals PRES1 to 8 for cutting off the tubes 16–5CP (Fig. 80*e*) of each of the correspondingly numbered pilot units. These signals are mixed with the sensing signal NPR, from the main commutator to cause a selected couple 16—16*a* in 5CP to become effective causing the production of a signal PRE. This signal in the manner described in Section 17, Item 22, enters into the production of the Reset signal and the transmission signal ES to In (Section 17, Item 24).

The IC-Int to ES trees (Fig. 58) produce the individual nine tree signals IQC0 to 8, IRC0 to 8, ITC0 to 8, IUC0 to 8, and IVC0 to 8. The signals with the appended digit 0 go to the blank code chassis BC (Fig. 78L). The signals with appended digits 1 to 8 go to tubes in the correspondingly numbered pilot units. These signals cut off the indicated tubes in Fig. 80*e* of the correspondingly numbered pilot units. Subsequently, the main commutator may produce successive signals Q2, R2, T2, U2 and V2. These signals scan the pilot units for their selection by the signals from the IC-Int to ES trees. For instance, if the signal IRC1 has been produced, it has cut off 43*a* in 5CP of pilot unit 1. Subsequently, the signal R2 cuts off 43 of this pilot unit, so that the couple 43—43*a* becomes effective and via 44, 41 and 33 produce a signal IC Int which is a condition to the production of the signal Int to ES1 by pilot unit 1, in a manner which will be described in Section 17, Item 21. Signals Q2 and IQC1 similarly act via 42—42*a*, 41*a* and 33 to produce the pilot unit 1 signal IC Int. Signals T2 and ITC1 act via 45—45*a*, 44*a*, 41 and 33 to produce this signal IC Int. Signals U2 and IUC1 are mixed by 46—46*a* which via 47, 41 and 33 produces this signal IC Int. Signal V2 and IVC1 acting via 48—48*a*, 47*a*, 41 and 33 produce this signal IC Int.

The pilot units selection trees IC–ES to In (Fig. 56) produce individual signals ICQ1 to 8, ICR1 to 8, ICT1 to 8, ICU1 to 8 and ICV1 to 8. These signals cut off tubes in the correspondingly numbered pilot units. Subsequently, the main commutator may produce successive scanning signals Q3, R3, T3, U3 and V3. Signals Q3 and ICQ are mixed by couple 27—27*a* in 5CP (Fig. 80*e*) of the pilot unit selected by the particular signal ICQ. The couple 27—27*a* then acts via 35 and 34 to produce the signal ICI in the selected pilot unit. This signal enters into the production of the signal ES to In by the selected pilot unit, as described in Section 17, Item 24. Signals R3 and ICR are mixed by 28—28*a* which via 35*a* and 34 causes the selected pilot unit to produce the signal ICI. Signals T3 and ICT are mixed by 29—29*a* which through 37 and 34 produces a signal ICI in the selected pilot unit. Signals U3 and ICU are mixed by 30—30*a* which acting via 37*a* and 34 produces the signal ICI in the selected pilot unit. Signals V3 and ICV are mixed by 31—31*a*, causing 39*a* and 34 to produce the signal ICI in the selected pilot unit.

As stated before, the pilot units used for piloting sequence data are conditioned by their switches 1SQ to 5SQ being set in seq positions. As will be explained in Section 16*b*, Item 24*b*, these pilot units must produce signals ESC and Out to ES for causing the selected sequence data to be sent to the electronic storage units selected for routing sequence data. Also these pilot units must produce the signals ES to In for causing the selected electronic storage units to transmit the sequence data to sequence storage, as will be described in Section 16*b*, Item 31. The signals ESC and Out to ES must be produced under control of the main commutator sensing signal OCO and a tree signal OCO (Fig. 54). The signal ES to In requires the production of tree signals PRES and either a sensing signal SPR or NPR. Signal NPR is effective only if the switch 5SQ is set to norm position. The simultaneous signal SPR is effective if the switch 5SQ is set to seq position. The signal ES to In also

requires the production of a tree signal and a scanning signal which when mixed will result in the production of the signal ICI.

To produce the requisite tree signals for the pilot units which are set to pilot sequence data, a pair of dial switches DS1S and DS2S (Fig. 55) are provided. Each of these switches has three sections (Figs. 54, 55 and 56) or stacks of contacts and commonly operated switch blades. The switch DS1S is set according to which pilot units and related electronic storage unit are to be used for S1Seq data while switch DS2S is adjusted according to which pilot unit and related electronic storage unit are used for S2Seq data. It may be assumed that switch DS1S is set to 7 and switch DS2S is set to 8. Referring to Fig. 54, it is seen that sections 1 of switches DS1S and DS2S are connected to the outputs of the OC-Out to ES trees. With DS1S set at 7, it transmits ground potential to the line OCO7 and with switch DS2S set to 8, it applies ground potential to OCO8. In other words, sections 1 of these switches, as adjusted in the example, produce tree signals OCO7 and 8. Signals OCO7 and 8 cut off tubes 12–5CP (Fig. 80e) in pilot units 7 and 8.

Referring to Fig. 55, with dial switches DS1S and DS2S set at 7 and 8, respectively, they apply ground potential to the lines PRES7 and 8. In other words the tree signals PRES7 and 8 are produced and cut off the tubes 16–5CP (Fig. 80e) in pilot units 7 and 8. The scanning signal SPR will be effective during each run of sequence to cut off 16a in the pilot units which have their switches 5SQ set at positions seq and so these pilot units will produce the signals PRE.

Referring to Fig. 56, with the dial switches DS1S and DS2S set at 7 and 8, respectively, their sections 3 produce the tree signals ICIS7 and 8 which cut off the tubes 32–5CP in pilot units 7 and 8 (Fig. 80e). During each run of sequence, the main commutator will produce the signal SW (see Section 16b, Item 31). This signal cuts off 32a of all the pilot units. Accordingly, the couples 32—32a of pilot units 7 and 8 will be effective via 39 and 34 to produce the signals ICI which enter into the production of the signals ES to In (also see Item 31 of Section 16b).

The pilot units also control the production of back signals SE, AE, Pil.OC, Pil.IC (Fig. 80a), STR and AT (Fig. 80c). These back signals are directed to the main commutator. Signal AE (see Section 16b, item 25) notifies the main commutator that the pilot units have completed the piloting of all data from Out bus-sets to electronic storage units. The signal SE notifies the main commutator that the pilot units used for piloting sequence data have completed the piloting of the sequence data into the selected electronic storage units. The signal Pil.OC is produced by a pilot unit at the time that it produces the signal ES to Int and notifies the main commutator that it may proceed with the next Out code step (see Section 17, Item 15a, as an example.) The signal Pil.IC is produced at the time the pilot units produces a signal Int to ES. This signal notifies the main commutator that it may proceed with the next In code scanning step (see Section 17, Item 23). The signal AT produced by a pilot unit notifies the main commutator that the pilot units have completed the piloting of all data from electronic storage to In bus-sets (see Section 16b, Item 33). Signal STR is produced by those pilot units which are piloting sequence data to notify the main commutator that the transmission of sequence data from the selected electronic storage units has been completed. The detailed construction and features of the pilot units will be brought out in subsequent sections.

16a. *The main commutator*

The main commutator (Figs. 78a to k) is a network of electronic elements which performs a round of operations for causing the instructions given by a line of sequence data to be carried out as an ordered process. The main commutator and the sequence means, including the sources of sequence data and sequence storage, may be referred to as main sequence means, as distinguished from the sub-sequence means of the multiplying-dividing unit, the accumulator unit, and the denominational shift unit. An extension of the main commutator is a so-called Control Frame (Figs. 75a to h, 76a to g, and 77a to d) which is a network of electronic circuits having functions which will be described subsequently. The main commutator may also be considered as including calculation control commutators ACC.C (Fig. 78A), MYC, (Fig. 78M) and DVC (Fig. 78D), and the no-calculation commutator NO (Fig. 78c).

As stated above the main commutator functions to perform a round of operations for carrying into effect instructions given by a line of seqeunce or program data. Such instructions normally include directions given by the program fields P, Q, R, T, U and V (see Figs. 3 and 4 and Section 2a) for transferring data from selected sources to the electronic storage units and for transmitting results from electronic storage units to selected receiving units. A set of instructions also normally includes directions given by the program fields OP1 and OP2 for the performance of mathematical operations among which are multiplications, division and accumulation. A set of instructions further includes directions for denominational shifts to be performed by the denominational shift unit (see Section 12), such directions being given by In codings in subfields s and by the program fields SH1 and SH2 (Section 2a). Finally, a set of instructions includes directions given by program fields S1 and S2 for selecting the next line of sequence data. A common set of instructions therefore will order numbers from selected sources to be transmitted via selected electronic storage units to selected calculation units and for the results of the calculations to be transmitted, after a selected denominational shift, through selected electronic storage units to selected receiving means. As now understood, when a calculation is ordered by a group of instructions, a plurality of numbers have to be sent from selected sources along selected out bus-sets to the corresponding electronic storage units and thence via the Internal Out and Internal-In bus-sets (Fig. 20) to the selected calculation unit. This is performed under directions given by Out program fields. In other words, an Out program field must be so interpreted by the machine as to cause a number to be sent from a source selected by its subfield r through an Out bus-set and corresponding electronic storage unit selected by its subfield b to the Internal Out bus-set and thence via the Internal-In bus-set to the calculation unit selected by the OP1 or OP2 field, whichever is in command. The interpretation of an Out field, therefore, must lead to the production of signals ESC, Out to ES, and ES to Int by the pilot unit which relates to the electronic storage unit selected by the sub-field b of the Out field.

The result of a calculation must be directed to a selected receiving unit, such as a relay storage unit. The transmission of a result from the calculating unit to the selected receiving unit is effected through the denominational shift unit and a selected electronic storage unit and its corresponding In bus-set. Such transmission is carried out to satisfy instructions in an In field. In other words, an In field must be so interpreted by the machine as to bring about the production of the signals ESC, Int, to ES, and ES to In by the pilot unit corresponding to the selected electronic storage unit.

With regard to the S1 and S2 program fields, they must be interpreted by the machine to cause entry from selected sources of sequence data into electronic storage and to cause transmission from electronic storage of the sequence data to sequence storage. In a sense, therefore, the S1 and S2 fields are both In and Out fields and operations by the pilot units and main commutator in connection with these fields must include the production of the signals ESC, Out to ES, and ES to In.

The control of the pilot units for producing the signals for causing entries into and transmission from electronic storage is chiefly exercised by the main commutator during a round of its operations. It has been explained above that entries via Out bus-sets into electronic storage are directed under control of Out fields and the S1 and S2 fields of a line of sequence data. Since the Out bus-sets provide a plurality of separate channels to electronic storage, it is possible to make the entries via the Out bus-sets into a plurality of the electronic storage units simultaneously or in overlapping time relationship. In other words, entries into electronic storage units as directed by the Out fields and the S1 and S2 fields may be effected concurrently. The main commutator produces a signal OCO (see Section 16*b*, Item 21) which is applied to all the pilot units and enables the pilot units selected by sequence storage to produce their signals ESC and Out to ES. All of these signals, which lead to the entry of data via the Out bus-sets to the electronic storage units may thus be produced simultaneously by the selected pilot units. As will be brought out in subsequent sections, the OCO main commutator signal is not sufficient of itself to cause the selected pilot units to produce the signals ESC and Out to ES. A Forward signal must also have been received by a selected pilot unit from the source which is to read out its data through the Out bus-set to the electronic storage unit. As previously explained, this Forward signal must be received by the pilot unit as an indication that the source of data is in condition for transmitting data to the Out bus-set and is not in a condition for receiving data from an In bus-set. Further, the OCO signal and the Forward signal will be effective only if the selected pilot unit is not then storing a condition for piloting transmission of data from the corresponding electronic storage unit.

Although the entries via Out bus-sets to electronic storage units may occur simultaneously, the transmission of the entered data from electronic storage units to the Internal Out bus-sets and into a selected calculating unit must occur singly, i. e. from only one electronic storage unit at a time. This is evident from the fact that the Internal In and Internal Out bus-sets (Figs. 20 and 22) provide only a single channel in association with electronic storage and this single channel can handle the data from only one electronic storage unit at a time. It follows that the signals ES to Int for directing the transmission of data from the electronic storage units to the calculating units by way of the Internal Out bus-sets must be produced successively. In other words, while the Out fields may be so interpreted by the machine as to cause the numbers from sources selected by these fields to be entered concurrently into electronic storage units, on the other hand the transmission of these numbers from electronic storage to a selected calculating unit can be effected only successively, from one electronic storage unit after another.

The In fields must be so interpreted by the machine as to cause the transmission of calculated results from the selected calculating units via the Internal In bus-sets to electronic storage units and thence to the selected receiving units. Since the Internal In bus-sets provide only a single communicating channel, the signals for causing the transmission of data along the Internal In bus-sets to electronic storage units must be produced successively. With regard to the transmission of data from electronic storage to the In bus-sets, such transmission may occur simultaneously or in overlapping time relationship from a plurality of electronic storage units in view of the fact that the In bus-sets provide a plurality of separate channels.

In order to control the pilot units for producing the signals ES to Int and Int to ES successively, the main commutator includes a series of scanning spots P, Q, R, T, U and V (Figs. 78*c* to *h*). These spots, it will be noticed are designated the same as the fields, P, Q, R, T, U and V of a line of sequence data. This is because the scanning spots function to control the pilot units for producing the signals which are required to carry out the instructions given by the corresponding program fields and which involve passage through electronic storage.

The spots P, Q, R, T, U and V come into operation successively, in the stated order, each, except the P spot, under control of the preceding spot. The P spot is put in operation under control of a signal PS produced by the main commutator at the same time as the signal OCO. When a program field is an Out field its corresponding scanning spot is conditioned to perform an Out code step, abbreviated as the OC step, but when a program field is an In field, its corresponding spot is conditioned to perform an In code step, abbreviated as the IC step. Since the P field always is an Out field, the P spot is always conditioned for an OC step. The other spots must be conditioned to perform IC steps when their corresponding program fields are In fields and this is effected under control of the In code sequence circuits (Fig. 61) as described in Section 16*b*, Items 15*b* and 39 and Section 17, Item 6. It may be mentioned now that when a program field is blank in its subfield *b*, the corresponding scanning spot will produce a signal which is effective in the blank code chassis BC (Fig. 78L). On the other hand, when a program field has a significant digit in its subfield *b* the corresponding scanning spot produces a signal or signals which are effective in the pilot units. When a scanning spot is conditioned for an OC step, it operates during a run of the commutator to produce a signal identified by the reference letter of the spot and the numeral 1. Thus the signals P1, Q1, R1, T1, U1 and V1 are OC step signals. These signals as now under-

plod occur successively during a scanning sequence of the spots P, Q, R, T, U and V. The scanning sequence is initiated by the signal PS which is produced concurrently with the signal OCO. The signal PS brings into operation the R spot for producing the P1 signal (see Section 16b, Item 26P). Assuming that the subfield Pb is not blank, the signal P1 acts upon the pilot units to sense which of them has been selected by the Pb subfield. Under control of the P1 signal the selected pilot unit is conditioned to produce its ES to Int signal when this pilot unit has completed its piloting of an entry via the related Out bus-set to the related electronic storage unit selected by the Pb subfield and which entry is under control of the OCO signal. After all the operations attendant upon the transmission under control of the ES to Int signal resulting from the P1 signal have been completed, the next scanning spot Q, comes into operation. If program field Q is an Out field, then this spot also will produce an Out code signal, Q1, which has the same function as the P1 signal but with relation to the Qb field. The signals R1, T1, and U1 have similar functions and are produced successively and applied to the pilot units successively. The signal V1 is not applied to the pilot units but only to the blank code chassis since program field V is always an In field and therefore is not used for directing the transmission of data from electronic storage to the Internal bus-sets. The V1 signal, however, has a purpose in conjunction with the blank code chassis in completing the scanning sequence (see Section 16b, Item 26V).

When a scanning spot is conditioned to perform an IC step, it functions during a scanning sequence to produce in succession signals designated by the reference letter of the spot and the numerals 2 and 3. Thus, the signals Q2 and Q3 are IC signals which are produced in sequence by the spot Q if it is conditioned for an IC step. Similarly, the signals R2 and R3, T2 and T3, U2 and U3 and V2 and V3 are IC signals. The signals Q2, R2, T2 etc. are applied during successive IC steps to the pilot units to sense which of them has been selected by the subfields b of the corresponding In field. Under control of the scanning signal, the selected pilot unit is controlled to produce the signal Int to ES. As an example see Section 17, Item 21. The signal Q2 or R2 etc. will not of itself cause the selected pilot unit to produce the signal Int to ES. It is also a condition to production of this signal that the selected pilot unit shall not be storing a condition for piloting transmission from its related electronic storage unit to an In bus-set.

After the operations attendant upon the production of the 2 signal by a scanning spot have been completed, the scanning spot produces its 0 signal. This signal is applied to the pilot units to sense which of them has been selected by the b subfield of the corresponding In field and to produce in this selected pilot unit one of the conditions for the pilot unit to emit its signal ES to In (see Section 17, Item 24). The other conditions are the application of a presense signal by the main commutator to the pilot units and the application of a back signal by the selected receiving unit to the pilot unit (see Section 17, Items 22 and 23).

With regard to the sequence data, the main commutator will produce the signal OCO for initiating the operations of the selected pilot units for piloting the sequence data from selected sources to the selected electronic storage units.

The main commutator will also produce the signals SPR and SW for controlling the selected pilot units in piloting transmission of the sequence data from the selected electronic storage units to the then open side of sequence storage.

The main commutator produces presense signals SPR and NPR simultaneously (see Section 16b, Item 21). The presense signal SPR is utilized by the pilot units which have been set for piloting sequence data; the NPR signal is utilized by those pilot units which are set to pilot arithmetical data, as mentioned in Section 15. The presense signal NPR is applied to the pilot units to sense which of them has been selected by an In field which calls for transmission to a receiving unit. The presense signal establishes in the pilot unit one of the conditions for causing the pilot unit to produce the transmission signal ES to In. Also, in conjunction with the Back signal from the selected receiving unit, the presense signal will cause the selected pilot unit to produce a Reset signal (see Section 17, Item 22). The presense signal SPR is utilized by the pilot units which are set to pilot sequence data to establish one condition for the transmission of the sequence data to the related In bus-sets and thence to sequence storage. The other condition for transmission of sequence data under control of the pilot units is the application of a signal SW by the commutator to the pilot units (see Section 16b, Item 31).

During a run of the commutator with respect to a line of sequence data, the signal OCO under control of which the entries are made from the Out bus-sets into electronic storage, and the signal PS which initiates the scanning sequence of spots P, Q . . . V, will be produced following three conditions. One condition is that the entries into electronic storage as ordered by a preceding line of sequence must have been completed as manifested by the pilot units having produced a signal AE under control of which a delay signal AED is produced some 16 ms. later. It is the signal AED which establishes one condition for the production of the signals OCO and PS. A second condition for the production of these signals is that the previous scanning sequence of spots P, Q . . . V has been completed (see Section 16b, Item 39). A third condition for the production of signals OCO and PS is that the transmission of sequence data as directed by S1 and S2 in the preceding line of sequence data has been completed and the pilot units consequently have produced the signal STR which is followed about 10 ms. later by the negative signal STRD1. It is the latter signal which satisfies the third condition for the production of the OCO and PS signals.

The production of the presense signals SPR and NPR requires the above three conditions for the OCO and PS signals and, in addition, requires that all transmissions relating to the preceding line of sequence data have been completed. Such completion is manifested by the application to the commutator of the signal AT which comes from the pilot units. The AT signal will be followed by an ATD signal about 16 ms. later to satisfy the fourth condition for the production by the commutator of the presense signals. Thus prior to the production of the presense signals, it is possible that the previous scanning sequence has been completed and the signals 3 from the scanning spots conditioned for IC steps have been applied to the pilot units and their effects stored therein to produce signals

ICI (see Figs. 80c, d and e). The Back signals from the units which are to receive the data resulting from the scanning of the new line of sequence data may also be effective upon the pilot units prior to the production of the presense signals. The ICI signals and the Back signals are two of the conditions required for causing selected pilot units to produce the transmission signals ES to In. The third condition involves the presense signals. Thus, it is possible that the presense signals may be the final timing control for transmission from electronic storage to the In bus-sets. Hence, under certain conditions such transmission from a plurality of electronic storage units to the In bus-sets may occur simultaneously. This is permissible since the In bus-sets provide a plurality of separate data transmitting channels.

The SW signal is produced by the commutator at the time the OCO signal is dropped (see Section 16b, Item 31). The OCO signal times the entry of data from Out bus-sets to electronic storage and when all such entries have been completed during a round of the commutator, the all-entry signal AE from the pilot units is applied to the commutator and initiates operations which lead to the termination of the OCO signal and the production of the SW signal. The latter signal in conjunction with the presense signal SPR will cause the sequence data in electronic storage to be transmitted to sequence storage (Section 16b, Item 31).

The main commutator also functions during a round of operations to cause the Control Frame to control the alternate closing and opening of the A and B sides of sequence storage, the alternate heating of the A and B sides of sequence storage circuits and trees, and the production of a plurality of time delay signals all of which will be explained further in subsequent sections. The calculation control commutators and the NO commutator are selectively conditioned according to the setting of the sequence storage pyramids OP1 and OP2 (Fig. 59). The OP1 pyramid is heated for the first half of a scanning sequence which involves the successive operation of spots P, Q and R while the OP2 pyramid is heated for the second half of the scanning sequence which involves successive operation of spots T, U and V.

Positive AP and BP pulses from the main pulse generator (see Section 4) are applied to the main commutator where they are inverted and amplified by tubes 1, 2, 3 and 4 in the Z spot (Fig. 78k). The resulting negative AP pulses are utilized by the main commutator, including all the calculation commutators, while the resulting negative BP pulses are utilized only by the calculation commutators MYC and DVC (Figs. 78M and D).

Details of construction and various operations of the main commutator will be brought out fully in the subsequent sections. The first run of sequence will be described in the next Section 16b. This is a run of sequence which is required to call the first real line of sequence data into sequence storage. When power is reapplied to the machine after it has been shut down, the operator at the control desk first operates the manual cancel keys which cause the resetting of the various triggers in the main commutator and elsewhere as previously mentioned in Section 1. An artificial line of sequence, consisting only of S1 and S2 data, is set into the dial switches DS1 and DS2 (see Fig. 40 and Section 11). This artificial line of sequence will select the first real line of sequence data in the carrying out of a succession of programmed operations.

16b. *The first run of sequence*

The sequence of events in this run is given in Figs. 79a, b, bb, c and d. The numbers in parentheses denote items of the present section, unless otherwise indicated.

1. *Relay AM.*—With the machine cancelled, trigger 2–5CF (Fig. 75e) is effective via tube elements 17 and 1 to place increased potential on line *am*. Consequently, 11–19CF (Fig. 77d) conducts and its output line *amr* (also see Fig. 36) drops in potential, causing current to flow through relay AM to the +150 v. line. Thereupon, relay AM is energized and its points AM*a* close and make the circuits of the plurality of relays AS (see Section 11), thereby opening the A side of sequence storage.

2. *Relays AOR.*—In cancelled condition of the machine, triggers 16 and 18 in 4CF (Fig. 75d) cut off the lock couple 15—15*a* to apply high potential to 13–4CF, which brings line *aor* to low potential. The low potential on line *aor* is inverted by 9 to 12 and 41 in 19CF (Fig. 77c) to increased potential on tubes 13 to 39. These tubes conduct, and their output lines *aorr* drop in potential. Each of these output lines connects to a group of relays AOR (see Fig. 36, where an illustrative number of these relays is shown). Upon lines *aorr* dropping in potential, current flow through relays AOR to the +150 v. line occurs. Energized relays AOR open their points *a* (Fig. 41), so as to break any existing stick circuits of relays AOP (see Section 11). The relays AOR are called the A operational reset relays since they serve to clear the A side sequence storage operational relays AOP of any data which may previously have been stored therein.

3. *Relays X7.*—With the machine cancelled, trigger 3 in 3CF (Fig. 75c) holds tube 2 in 3CF off and line *x7* at increased potential so amplifiers 1, 2 and 3 in 18CF (Fig. 77c) produce low potential on lines *x7r* (also see Fig. 36). A relay X7 and delay relay X7D are in series between the +150 v. line and each of the lines *x7r* (an illustrative pair of relays X7 and X7D appears in Fig. 36). When lines *x7r* drop in potential, relays X7 and X7D are energized. Relays X7 are the timing relays and relays X7D are the arc suppression relays for the A sides of the In sequence storage pyramids shown in Figs. 51, 52*a* and 52*b*. Since all these pyramids are at zero in the first run of sequence, the energization of relays X7 and X7D has no effect during the first run.

4. *Entering the artificial line of sequence.*—The artificial line of sequence was explained in Section 11. Such line of sequence consists of S1 or S2 codes, or both, set on dials DS (Fig. 40). The setting of these dials is made according to where the first real line of sequence for a program of operations is to be obtained. Having cancelled the machine, the operator now closes switches SS1 and SS2 (Fig. 40*a*) to cause the predetermined artificial line of sequence to be applied to sequence storage, as described in Section 11. Since the A side of sequence storage now is open (see item 1), the S1 and S2 code numbers set on the dials DS1 and DS2 are applied to relays AI (Figs. 37, 38 and 39) in the S1 and S2 columns 19 and 20 of the A side of sequence storage. The energized relays AI close their points *b* (Fig. 41), establishing the pickup circuits of the corre-

sponding groups of relays AOP. In this manner, the S1 and S2 data are stored in the S1Seq and S2Seq relays AI and AOP of sequence storage columns 19 and 20 (see also Figs. 42 and 43). Thus, the very first artificial line of sequence is entered in the A side of sequence storage so that the S1, S2 pyramids (Fig. 50) are set, on their A sides, in accordance with the S1 and S2 data contained in the artificial line of sequence.

5. *Start key switch, commutator signal STR, dropping AM and AOR.*—The operator next closes a start key switch SKS (Fig. 77*aa*) at the control desk picking up a relay SKR, the point *a* of which connects the +150 v. line to point *g* of trigger 5, Fig. 77*a*, so that the trigger turns and cuts off 4 to bring line SPST to increased potential. The increased potential is applied to tube 18*a*Z (Fig. 78*k*), making the tube conduct and turn trigger 17Z. With 17Z turned, it applies increased suppressor potential to 13 which is already conditioned plus by trigger 10 as is (reset). The series of tubes 13Z, 18Z, 12Z thereupon produce a negative going STR commutator signal which goes to the control frame (Fig. 75*a*) where it is inverted by 4–1CF (Fig. 75*a*) to a positive going STR signal, on wire 101, which is transmitted to tube 3–5CF (Fig. 75*e*). This tube produces a negative going pulse applied to both sides of trigger 2–5CF, turning it (see item 1). Accordingly, wire *am* drops in potential, and relays AM and AS (Fig. 36) are deenergized. Meanwhile, the artificial line of sequence has been applied to relays AI and AOP (Item 4). The positive STR signal on wire 101 also makes 24, Fig. 75*d*, conductive so as to turn 16. Consequently, relays AOR are deenergized (note Item 2), and their points *a* reclose to establish the hold circuits through the energized relays AOP. In every case, after the relays AM and AS have served their purpose of opening the A side of sequence storage to an entry, the relays AM and AS and AOR are dropped under control of an STR signal.

6. *Relay BM.*—With trigger 2–5CF (Fig. 75*e*) turned, it acts through 17*a* and 1*a* to increase the potential on the line *bm*, whereupon tube 12–19CF (Fig. 77*d*) conducts, its output line *bmr* (also see Fig. 36) drops in potential, so relay BM is energized. Relays BS pick up via points *a* of BM, opening the B side of sequence storage to subsequent entry of the next line of sequence. Each STR signal switches the status of 2–5CF, so that relays AM and BM alternately are energized by successive STR signals and the A and B sides of sequence storage alternately opened to sequence data.

7. *Relays X1.*—The positive STR signal also acts through 11*a*–5CF (Fig. 75*e*) to turn trigger 16–5CF. The trigger now cuts off 9 of the couple 9—9*a*. Tube 9*a* is being held off by trigger 10. Accordingly, the couple now serves through 8*a* and 7 in 5CF to cause the potential on line *x1* to rise. This makes 21–19CF (Fig. 77*d*) conduct, so its output line *x1r* (Fig. 36) drops in potential and relays X1D and X1 are energized. Points X1*a* (Fig. 50) now heat the A sides of the S1 and S2 Unit Outs, Group Outs, and Station Move pyramids. It is clear that after entering sequence data into the A side of sequence storage, the A sides of the S1, S2 pyramids are heated.

8. *Selection of the next line of sequence.*—The A sides of the S1, S2 pyramids (Fig. 50) have been set (Item 4) according to where the next (First Real) line of sequence data is to be obtained. The Unit Outs, Group Outs and Station Move S1, S2 pyramids have been heated on the A sides by the closure of points X1*a* (Item 7). Depending on the setting of these pyramids and the plugging, described in Section 11, the sources for the next line of sequence are selected and the next line of sequence is applied to Out bus-sets. In the present example, it is assumed that the S1 and S2 code numbers (Fig. 40) in the S1, S2 pyramids (Fig. 50) are 01 and 02, respectively. Assume, further, that code numbers 01 and 02 are to select the S1Seq and S2Seq portions of the next line of sequence from tape storage stations 1 and 10 of bank 1 (Section 9), with station 1 to be read out through its ASS selector and station 10 to be read out through its BSS selector. Assume, further, that S1Seq data are to be applied to Out bus-set 7 and S2Seq data to Out bus-set 8. Finally, assume both stations are to be moved after reading out a line of data. The plugging in tape storage bank 1 will be between sockets ASSP (Figs. 31, 32*a* and 34) and sockets TS–GOP7 and between BSSP and TS–GOP8. The plugging for selection of tape storage Group Out 7 by the 01 setting of the S1 Group Outs pyramid (Fig. 50) is between SGP01 (Figs. 50 and 53*b*) and TSGOS7 of bank 1. The plugging for selection of the tape storage Group Out 8 by the 02 setting of the S2 Group Outs pyramid is between SGP02 and TSGOS8 of bank 1. For selection of 1ASS and 10BSS (Fig. 32*c*) of bank 1 by the 01 and 02 settings of the S1 and S2 Unit Outs pyramids, sockets SUP01 and 02 are plugged to 1ASP and 10BSP of bank 1, as shown in Fig. 53*a*. For selection of Move relays MA and MB (see Fig. 32*c*) of bank 1 by the 01 and 02 settings of the S1 and S2 Station Move pyramids (Fig. 50), sockets SMP01 and 02 (Fig. 53*b*) are plugged to MAP and MBP of bank 1, as shown.

With the illustrated plugging, the heating of the Unit Outs, Group Outs and Station Move pyramids (Fig. 50) by the closure of contacts X1*a* establishes the following circuits:

Tape storage Group Out 7 (bank 1).—From ground (Fig. 50) through an X1*a* contact, the S1 Group Outs pyramid to the socket SGP01, plug connection to TSGOS7 (Fig. 32*c*) (bank 1), and through the Group Out gang relay TS–GO7 (Fig. 32*c*) of bank 1 to the +50 v. line.

Tape storage Group Out 8 (bank 1).—From ground via X1*a* contact (Fig. 50) the S2 Group Outs pyramid to socket SGP02 (Fig. 53*b*), the socket GOS8 (bank 1), and through gang relay TS–GO8 (Fig. 32*c*) of bank 1 to the +50 v. line.

Station selector 1ASS (bank 1).—From ground via an X1*a* point, the S1 Unit Outs pyramid (Fig. 50) to the socket SUP01 (Fig. 53*a*) socket 1ASP (Fig. 32*c*) (bank 1) and through an interlock relay point 1ACL*a* and the gang relay 1ASS (see Fig. 32*c*) of bank 1 to the +50 v. line.

Station selector 10BSS (bank 1).—From ground via an X1*a* point, the S2 Unit Outs pyramid to socket SUP02 to socket 10BSP (bank 1) and via an interlock point 10ACL*a* through gang relay 10BSS of bank 1 to the +50 v. line.

Move relay MA (bank 1).—From ground to an X1*a* point, the S1 station move pyramid to socket SMP01 (Fig. 53*b*) to socket MAP (bank 1) and through relay MA (see Fig. 32*c*) of bank 1 to the +50 v. line.

Move relay MB (bank 1).—From ground via an X1*a* point, the S2 station move pyramid to socket SMP02, socket MBP (bank 1) and through relay MB (Fig. 32*c*) of bank 1 to the +50 v. line.

Energization of the relays TS–GO7 and 8 of bank 1, relays 1ASS and 10BSS of bank 1, and the relays MA and MB of bank 1 will cause sta-

tions 1 and 10 of bank 1 to read out S1Seq and S2Seq data, respectively, to the Out bus-sets 7 and 8, and line spacing of these two stations later to occur, all in the manner previously described in Section 9. Also, forward signals are applied to buses 81 of Out bus-sets 7 and 8. In a manner to be described at the end of Item 24b, the pilot units 7 and 8 will produce the Move signals for bringing about the stepping of selected stations 1 and 10 in bank 1 (see Section 9).

In the foregoing manner the S1 and S2 code numbers have selected the next line of sequence and this line has been applied to the selected Out bus-sets 7 and 8 to be entered at the proper time in electronic storage units 7 and 8 (see Item 24b).

9. *Relays X2 and XM.*—The positive STR signal on wire 101 (see Item 5) also serves via 23a–5CF (Fig. 75e) to turn 28 which thereupon cuts off 21 of couple 21—21a of which 21a already is off under control of 22. The couple 21—21a now provides increased potential on wire x2w and also is effective through 20a and 19 to increase the potential on line x2 (also see Fig. 77d). This renders tubes 19, 20, 25, 26 and 27 in Fig. 77d conductive, whereupon lines x2r and xm drop in potential. The decreased potential on a line xm (also see Fig. 36) results in an energizing circuit being completed through relays XM and XMD to the +150 v. line. There are two pairs of serially connected relays XM and XMD, each pair connected to a line xm, but only one pair is shown in Fig. 36. In general, it is to be understood that where similar circuits are provided, only one or a few illustrative circuits will be shown. The decreased potential on line x2r results in energizing circuits being completed through relays X2 (P, Q, R, T, U) to the +150 v. line. There is one relay X2 for each of the possible Out sequence storage fields P, Q, R, T and U, as indicated by the identifying letters applied to the relays X2. Relays XM, XMD, and X2 serve as timing relays for the A sides of the Out sequence permutation circuits shown in Figs. 47a, b, c, d, 48 and 49a and b and described before in Section 11. These circuits are adapted to select relay and tape storage and table look-up Group Outs, relay and tape storage Unit Outs, Station Move relays, Table Outs, and dial storage Group Outs. In the first run of sequence, none of these circuits is effective since Sequence storage is at zero except in the S1 and S2 fields.

10. *Relays X3.*—As explained in Item 9, the STR signal brought about a rise in potential on wire x2w (Fig. 75e), whereupon X2, XM, and XMD were energized. The increased potential on wire x2w is inverted by 29–6CF (Fig. 75f) to reduced potential which cuts off 27a of the lock couple 27—27a. Element 27 is being held conductive at present by trigger 1 acting through 8, so that 27—27a continues at low output potential even though 27a has been cut off under control of the STR signal. This same signal STR initiates operation of a "Late" delay circuit shown in 6CF (Fig. 75f). The signal STR is inverted by 5 of 6CF to a negative pulse which reverses trigger 4. As 4 reverses, it turns trigger 3. The next AP pulse restores 3, which turns 2. The following AP pulse restores 2, causing it to turn 1. The next BP pulse restores 1 which thereupon restores 4. Meanwhile, trigger 1 has applied increased potential to 8—6CF which in turn applied reduced potential to 27—6CF, cutting it off momentarily. In this way, 27 is cut off after 27a is cut off, the delay being determined here by the successively operated triggers 3 and 2 of the delay circuit in 6CF and being roughly equal to the duration of two AP pulse cycles (Fig. 19). That is, about two AP pulse cycles after the STR signal, the trigger 1 operates to cut off 27. Taking the AP pulses as at 4KC (Fig. 19 and Section 4) the delay is about half a millisecond. It may be noted that when 8–6CF cuts off 27, it also cuts off 26a. But 26 is now being maintained conductive since 28 is now at cut-off under control of low potential on a wire y2w.

When tube 27 is cut off momentarily during the brief reversed period of 1–6CF, the couple 27—27a applies increased potential to 12 which in turn applies reduced potential via wire 102 to trigger 18, turning it. The trigger 18 thereupon renders conductive the tube 17, which is being conditioned by trigger 16. Tube 17 now acts through 13 to place wire x3 at increased potential whereupon the amplifier, comprising tubes 7, 8 and 9 in 15CF (Fig. 76g), applies reduced potential to output wire x3r (also see Fig. 36), causing relays X3 to be energized.

These relays close their points to ground the A sides of the Table Out and table look-up Group Out pyramids (Figs. 47b and c). These pyramids are at zero during this run, and operation of relays X3 has no effect.

11. *X4, X5 and X6 relays.*—In similar fashion, the relays X4, X5 and X6 (Fig. 36) are picked up. Briefly, the negative going pulse produced on wire 102 by 12–3CF (Fig. 75f) goes to the triggers 12 and 24 in 7CF (Fig. 75g) and to trigger 6 in 8CF (Fig. 75h), turning these three triggers. Trigger 12–7CF renders conductive the tube 11 conditioned by 10. The tube conducts and via 7 causes an increase of potential on the line x4. Consequently, tubes 13, 14 and 15 of 15CF (Fig. 76g) become conductive, and line x4r (also see Fig. 36) drops in potential, so relays X4 are energized. Similarly, turned trigger 24–7CF (Fig. 75g) causes 23 conditioned by 22, to conduct and through 19 to bring wire x5 to increased potential. Tubes 19, 20 and 21 (Fig. 76g) become conductive, their output line x5r (also see Fig. 36) drops in potential and relays X5 are energized. Turned trigger 6–8CF (Fig. 75h) renders 5, conditioned by 4, conductive, whereupon 1–8CF becomes non-conductive and increased potential is placed on wire x6. Tubes 25, 26 and 27 (Fig. 76g) now conduct, and output line x6r (also see Fig. 36) drops in potential, so relays X6 are energized.

Relays X4, X5 and X6 close points in the circuits of the A sides of the tape storage Unit Outs, Group Outs, and Station Move trees (Figs. 47b, c and d). All of these trees being at zero during the first run, the operation of relays X4, X5 and X6 has no effect.

12. *The S transmission delay counter and the STRD1 pulses.*—The positive STR signal (Item 5) also acts via 7–3CF (Fig. 75c) to turn 8. This trigger now cuts off 14, making couple 14—14a responsive to pulses EP (also see Fig. 19) continually applied to 14a. The couple 14—14a then acts through 13 to apply input pulses to the input line 103 of the S transmission delay counter. This delay counter is of a known type and will provide required delay times between the STR signal and an output signal or signals. It will be understood that other suitable delay counters may be used. Triggers 19, 20, 21, 22 and 23 may be considered as the first order of the delay counter. The input pulses are applied through line 103 to all the triggers of the first order.

However, the first trigger 19 is in a status which is responsive to the input pulses but the other triggers of the first order are in states which are immune to the input pulses. Accordingly, the first input pulse turns 19 alone and 19, upon turning, produces a transfer pulse which reverses 20. 20 is now in a state responsive to an input pulse. Hence the second input pulse returns 20. As 20 returns, it causes 21 to turn. The third input pulse returns 21, causing it to turn 22. The fourth input pulse returns 22, whereupon 23 is turned. The fifth input pulse returns 23. As 23 returns, it restores the first trigger 19. The first order of the delay counter is then in its initial condition. In the foregoing manner five successive input pulses effect a cycle of operation of what may be considered the first order of the delay counter. In general, the input pulses will be derived from a tap point of a voltage divider between the anode of a tube and the +150 v. line, with the portion of the voltage divider between the tap point and the anode having a value of approximately .0035 megohm and the portion of the voltage divider between the tap point and the +150 v. line having a value of approximately .0015 megohm. At completion of the cycle, 23 restores and turns 24, which reverses triggers 17 and 18. At the completion of a second cycle of the first order, trigger 23 returns 18, which thereupon restores 17. As 17 restores, it applies a negative impulse to 28*a* which produces a positive STRD1 signal on wire 104. At the same time, 17 applies a positive impulse to 5 which produces a negative STRD1 signal on wire 105. The STRD1 pulses appear about 10 ms. after the STR pulse.

13. *The AIR Relays.*—The positive STRD1 signal on wire 104 is inverted by 23–4CF (Fig. 75*d*), and the resulting pulse turns trigger 22–4CF. Trigger 22–4CF (Fig. 75*d*), turned, now is applying reduced potential to 27 of couple 27—27*a*. 27*a* is held off by 28–4CF. The couple 27—27*a* now is effective through 26*a* and 19 to place high potential on line *air*. Tubes 1 to 7 (Fig. 77*d*) now conduct, whereupon lines *airr* (also see Fig. 36) drop in potential, causing the reset relays AIR to be energized. Their points *a* (Fig. 37) open and deenergize the relays AI (Fig. 37). Contacts *b* (Fig. 41) of AI open and drop the pick-up circuits through relays AOP (see Item 4). Relays AOP remain energized by the circuits made through their stick contacts *a* and the points *a* of AOR (Item 5).

14. *Terminating the STR signal and producing the "a" signal.*—The negative signal STRD1 (Item 12) on the output wire 105 (Fig. 75*c*) is effective via 11*a* and 11, in the Z section (Fig. 78*k*) of the main commutator, to turn 10, which turns 9. Trigger 10, now turned, renders 13Z nonconductive to terminate the STR signal (Item 5). When trigger 9 turned, it applied a positive pulse to 14 but 14 is being held at cut-off by 18*a* now conductive under control of trigger 5, Fig. 77*a*, which was reversed under control of the start key SKS. Accordingly, 14 (Fig. 78*k*) does not become conductive and does not reset 17. Hence, 17 maintains 13 conditioned so that when 10 is reset later, an STR commutator signal will again be produced. To stop the sequencing operations which start with the STR signal, the operator may close the stop key switch SP (Fig. 77*aa*), picking up relay SPS which connects the +150 v. line to point *b* of 5, Fig. 77*a*, resetting it. This results in line SPST going down in potential, whereupon 18*a*, Fig. 78*k*, is cut off and conditions 14. When the next STRD1 signal causes trigger 9 to turn, 14 will become conductive and restore 17. As a result, a next STR signal will not be produced and sequencing operations will terminate at the end of the sequencing run.

The STRD1 negative pulse also is transmitted to the W spot (Fig. 78*i*) of the main commutator, where it is amplified by 22 and 22*a*. The resulting negative pulse switches 23W to apply increased potential to a grid of 14W. The other grid is conditioned by triggers 17W and 19W through a lock couple 18—18*a*, so when 23 applies increased potential to 14, it becomes conductive and turns 15W. The next AP pulse restores 15W which thereupon applies a negative impulse to triggers 16, 17, 19, 23 and 25 of the W spot, turning 16, 17, 19 and 25 and restoring 23. It should be noted that with 25W turned, it is applying increased potential to 27 of the lock couple 27—27*a* and is applying reduced potential to 26 of lock couple 26—26*a*. Coincidentally, 28W is applying reduced potential to 27*a* and increased potential 26*a*. At this point, then, both these lock couples are at reduced output potential, whereas before 25W was turned, the couple 27—27*a* was effective to produce increased potential which, applied to inverter 32W, produced a negative signal "*b*" on wire 106. When the trigger 25W is turned, it interrupts the "*b*" signal. The trigger 16W, which was turned by trigger 15 when the latter was restored by an AP pulse, is itself restored by the next following AP pulse. As it restores, it turns trigger 28W which then cuts off 26*a*. At this time, turned trigger 25 is cutting off 26. Therefore, when 28W cuts off 26*a*, the couple 26—26*a* acts through 30W to produce the negative "*a*" signal on wire 107.

15*a*. *Heating the A sides of Operational Sign and In code permutation circuits.*—The negative "*a*" signal on wire 107 is transmitted to amplifiers 29 and 35 in Fig. 76*a* which apply a positive "*a*" signal to the tubes 1, 2, 3, 7, 8, 9, 13, 19, 20, 21, 25 and 26 in Fig. 76*c*. These tubes become conductive and their outputs go down in potential. The outputs 1PA, 2PA, 1QA, 2QA, 1RA, 2RA, 1UA and 2UA heat the A sides of the Operational Sign permutation network (Fig. 60) set by sequence storage according to the code numbers in subfields *s*. The tube outputs QA, RA, UA and VA heat the A sides of the In code permutation network (Fig. 61) controlled by the *s* subfields of sequence storage.

The T portions of the Operational Sign and In code networks (Figs. 60 and 61) are heated when the outputs 1TA, 2TA and TA of tubes 14, 15 and 27 in Fig. 76*c* go down in potential. These tubes are not rendered conductive directly by the "*a*" signal since it is desired to heat the T portions of the Operational Sign network only when T is an Out field and to heat the T portion of the In code circuit only when T is an In field. As stated before in Sections 2*a* and 11, the field T is an In field if the OP2 code number is 01 and is an Out field for any other OP2 number. Therefore, the control of the tubes 14, 15 and 27 in Fig. 76*c* includes an A side OP2 tree (Fig. 76*e*). The input of this tree is at +150 v. The output OP–01 (also see Figs. 46 and 46*a*) of the OP2 tree in Fig. 76*e* goes to the suppressor of a tube 13 in Fig. 76*e*, while the output OP0 of the tree goes to the suppressor of a tube 14. Thus, if the OP2 code indicates that T is an In field, then tube 13 is conditioned while if the OP2 code indicates that T is an Out field, then tube 14 is conditioned. The positive "*a*" signal (Figs. 76*b* and *c*) is amplified by 33, 31 and 32 in Fig. 76*c* and by 30, 35 and 36 in Fig. 76*d*. The resulting positive "*a*"

pulse is applied to the control grids of tubes 13 and 14 in Fig. 76e, causing the conditioned one of these tubes to become conductive. If 13 conducts, its output is inverted by 6 to a positive T "in" A pulse which renders 27 in Fig. 76c conductive. The output line TA of the tube 27 goes down in potential, heating the A side of the T portion of the In field designating circuit in Fig. 61. If tube 14 in Fig. 76e is conditioned, then the applied "a" positive pulse renders 14 conductive, and its output in inverted by 12 to a positive T "out" A pulse. This pulse makes 14 and 15 in Fig. 76c conduct, so that their outputs 1TA and 2TA go down in potential, heating the A side of the T portion of the Operational Sign circuit (Fig. 60).

The heating of the Operational Sign and In code permutation circuits has no effect during the first run because the sequence subfields *s* are now at zero.

15b. *Heating the A sides of the pilot units selection trees.*—The heating of the A sides of the trees, shown in Figs. 54 to 58 and explained in Section 15, is under control of the "a" signal, as described below.

The positive "a" pulse from amplifier 33, 31 and 32 in Fig. 76c also is applied to tubes 4, 5, 6, 7, 11, 12, 13, 15 and 21 in Fig. 76d. If T is an In field, the positive T "in" A pulse is produced as explained before and is also applied to 14 in Fig. 76d, but if T is an Out field, the positive T "out" A pulse is produced and is applied to 10. The mentioned tubes become conductive and their outputs heat the A sides of the indicated P, Q, R, T, U and V branches of the OC–ES to Int trees (Fig. 57), and the IC–Int to ES trees (Fig. 58).

As previously described, a positive "a" pulse was produced by amplifier tubes 35 and 36 in Fig. 76d and the pulse was applied to tubes 13 and 14 in Fig. 76e in order to render one of these tubes conductive, depending on whether the OP2 tree was in 01 status or in any other code number status. This same "a" pulse is also applied to tubes 7, 8, 9, 10, 11, 15 and 16 in Fig. 76e so as to render any of these tubes which have been conditioned, in a manner soon to be explained, to become conductive. The tubes 7, 8, 9, 10, 11 are conditioned under control of zero filters of the V, U, R, Q, P sequence fields, respectively. The tubes 15 and 16 are conditioned under control of the OP2 tree, on the A side, and T zero filters. The zero filter has been described before in Section 11 and is shown in Fig. 44. In Fig. 76e the zero filters are shown diagrammatically as boxes and the field controlling the zero filter is marked inside the box along with the letters ZF. The zero filter permits a circuit to be made therethrough if the subfield *r* of the field relating to the zero filter has any significant digit. In other words, if this subfield *r* is at zero, then the zero filter will not allow a circuit to be made through the filter. If the P, Q, R, U and V subfields *r* are not at zero, the tubes 11, 10, 9, 8 and 7 are conditioned to be rendered conductive by the applied "a" pulse. Likewise, if the T subfield *r* is not at zero, the tube 15 is conditioned if the OP2 tree (A side) is set at 01. On the other hand, if this tree is set at any other number, then the tube 16 is conditioned. The applied "a" pulse therefore will render either the tube 15 or 16 conductive. The outputs of tubes 7, 8, 9, 10, 11, 15 and 16 are coupled by inverters 1, 2, 3, 4, 5, 18 and 17, respectively, to the lines designated by the identifying letters of the fields followed by the small letters *zf*, with the further identification of the lines relating to the T field as "out" and "in" lines. Positive pulses therefore will appear on these lines if the tubes conditioned through the zero filters become conductive. The positive pulses are applied to tubes 1, 2, 3, 8, 9, 16, 17, 18, 19, 20, 22, 23, 25, 26 and 27 in Fig. 76d causing these tubes to conduct and heat the A sides of the P, Q, R, T, U and V branches of the indicated sequence storage trees IC–ES to In (Fig. 56), IC Presense (Fig. 55) and OC–Out to ES (Fig. 54).

Inasmuch as only S1 and S2 sequence data have been set up for the first run of sequence, the sequence storage subfields *r* now stand at zero and the zero filters will not allow circuits to be made therethrough. Consequently for the first run, the IC–ES to In, IC Presense and OC–Out to ES trees are not heated.

The OC–ES to Int (Fig. 57) and the IC–Int to ES trees are heated because their heating circuits are not made through zero filters. However the T tree of the IC–Int to ES group is not heated because the OP2 trees are in zero status during the first sequence run.

16. *The SCM and a1 signals.*—When trigger 16W (Fig. 78*i*) is restored (Item 14) it applies a negative going pulse to a wire 120 which leads to trigger 13X (Fig. 78*j*), turning this trigger. Trigger 13X thereupon, through 14X, produces a positive SCM signal on wire 121. The SCM signal is inverted by 25Z (Fig. 78*k*) to a negative impulse effective to turn 22Z. 22Z then cuts off 19 of couple 19—19*a*. At this time, 19*a* also is held at cut-off by 26Z, so the lock couple now is effective to apply increased potential to 20Z which in turn produces the negative *a1* signal on wire 122. This signal *a1* which is produced substantially simultaneously with the "a" signal, is transmitted to 1 and 7–9CF (Fig. 76*a*) which apply increased potential to tubes 13, 14, 15, 16, 19, 20, 21, 22, 26, 27 and 31 rendering all of these tubes conductive to heat the A sides of the Q, R and SH1 shift code circuits (Figs. 62 and 63) and the A side of the OP1 pyramid (Fig. 59). The shift code circuits are all at zero during the first run and their heating has no consequence. For the present, we need consider only the OP1 pyramid which now is in zero status. Hence, the OP00 terminal now is at reduced potential.

17. *The "No Op" control and the Ink signal.*—The 00 terminal of the OP1 pyramid (Fig. 59) connects to 14–16CF (Fig. 77*a*). Since this terminal now is at reduced potential, 14–16CF is cut off and through 18, produces a negative No Op signal on wire 123. This signal goes to the NO (no calculator operation code) commutator spot (Fig. 78*c*) where it cuts off 13 of couple 13—13*a*. The positive SCM signal (Item 16) on wire 121 (Fig. 78*j*) also is applied to and turns on tube 1*a* of couple 1—1*a* in the P spot (Fig. 78*c*), releasing the couple to produce a negative impulse which reverses trigger 5P in the Ink delay circuit. The next AP pulse restores 5P which thereupon turns 6P. The next following AP pulse restores 6P to cause it to turn 7P. The succeeding AP pulse restores 7P. During the AP pulse interval in which 7P is in turned status, it acts through parallel 10 and 11P to produce a negative Ink signal on wire 125. This signal cuts off 13*a* of the couple 13—13*a*. Previously, 13 of this couple was cut off by the No Op signal. Accordingly, when 13*a* also goes

off, the couple is effective through 14 to turn 18NO, which may be called the gate of the NO commutator. It is to be noted that 5P, 6P and 7P constitute a delay counter which provides a short delay between the heating of the OP1 pyramid under control of the *a1* signal (Item 16) and the production of the Ink signal. This delay insures time for the operation code to be read out before the Ink signal tests for the operation which has been read out. Where no operation has been called for by the OP1 or OP2 tree, the No Op signal first cuts off 13 and the Ink signal then tests this condition by cutting off 13*a*. As 13 has been cut off, the result here is that 18NO is turned. With 18NO turned, it is effective via 27NO to condition 25NO.

18. *The STRD2 pulse.*—When the S transmission delay counter in 3CF (Fig. 75*c*) completed a second cycle of the first order, it restored 18–3CF (see Item 12), whereupon 18 turned 12. At completion of a third cycle, 23 restores 12. The latter thereupon reverses 11. Upon completion of a fourth cycle, 23 restores 11, which turns triggers 10 and 16. These are restored by 23 at the end of a fifth cycle. 16 thereupon acts through 28 to produce a positive STRD2 pulse on line 126. This pulse appears some 25 ms. after the STR pulse (see Item 5) and about 15 ms. after the STRD1 pulses (Item 12).

When trigger 10–3CF restored, it switched trigger 9 which is returned by the next BP pulse. In returning, 9 restores 8 previously switched (Item 12) under control of the signal STR. With 8 restored, it turns on 14 of couple 14—14*a*, interrupting response of the couple to the applied EP pulses. Accordingly, actuation of the delay counter in 3CF ceases. Also, when 10–3CF returned, it restored 24. Thus, the delay counter and allied elements are now back in their original conditions.

19. *Dropping AIR.*—The positive STRD2 pulse on wire 126 (see Item 18) acts through 23*a* (Fig. 75*d*) to turn 28–4CF which then applies high potential to 27*a*, releasing the couple 27—27*a* in 4CF. Consequently, 26*a* is cut off and line *air* falls in potential, so that lines *airr* (Figs. 77*d* and 36) rise and relays AIR (Fig. 36 and Item 14) are dropped.

RECAPITULATION

To summarize, the relay AM and relays AS were energized (Item 1), opening the A side of sequence storage. The artificial line of sequence, comprising manually chosen S1, S2 codes was entered in the A side of sequence storage (Item 4), selected relays AI and AOP being energized through points of AS. The start key SKS was then operated to produce the Sequence Transmission Signal STR (Item 5). The relays BM and BS were then operated (Item 6) to open the B side of sequence storage. Relay X1 was energized (Item 7) to ground the A side of the S1 and S2 trees, to effect selection of the next line of sequence data. In the assumed example (Item 8), stations 1 and 10 of tape storage bank 1 were selected and applied the next line of sequence data, along with forward signals, to Out bus-sets 7 and 8. Data applied to the Out bus-sets is manifested by selectively increased potentials which are applied to related sets of tubes Out En (Fig. 21) of the electronic storage units ES7 and ES8 (Fig. 22) to condition these tubes (Section 6). Thereafter (see Item 24*b*), pilot units 7 and 8 will apply the entry signals Out to ES7 and Out to ES8 to the conditioned tubes, causing entry of the selected, next line of sequence into the electronic storage units 7 and 8. The relays AOR were deenergized (Item 5) to maintain the circuits of the previously energized AOP relays. The AI relays were then dropped (Item 13). An "*a*" signal was emitted (Item 14) to heat the A sides of certain sequence storage permutation circuits (Figs. 54 to 63). An SCM signal was produced (Item 16) causing the *a1* signal to be emitted. This signal heated the OP1 tree, now set to zero. Consequently, a No Op signal was produced (Item 17) which along with a slightly delayed Ink signal caused the gate trigger 18 of the NO commutator (Fig. 78*c*) to be opened, whereby 25NO is conditioned.

The sequence data, selected by the A side of sequence storage and now applied to the entry gates of tubes Out En (Fig. 21) of electronic storage units ES7 and ES8 will be entered into these storage units and transmitted therefrom into the now opened B side of sequence storage. The manner in which the sequence data entry is completed and then transmitted to the B side of sequence storage will be explained below. Operations will be explained, in the main, with reference to electronic storage unit ES7, since the operations with respect to ES8 are similar.

20. *Dial switches DS1S and DS2S.*—The functions of these dial switches DS1S and DS2S have been explained in Section 15. Briefly reviewed, these switches are set to select the pilots whose associated electronic storage units receive the real lines of sequence and to transmit these lines to sequence storage. It has been assumed that electronic storage units ES7 and 8 will be used for this purpose, with ES7 to handle S1Seq data and ES8 to handle S2Seq data. On this assumption, the sequence data were applied to Out bus-sets 7 and 8 (Item 8). On the same assumption, DS1S and DS2S are adjusted to 7 and 8, respectively.

Considering dial switch section 1 (Fig. 54) of dial switch DS1S, it produces signal OCO7 to cut off tube 12 of the couple 12—12*a* in Section 5CP (Fig. 80*e*) of pilot unit 7.

With regard to section 2 of DS1S (Fig. 55) it produces the cut off signal PRES7, cutting off 16 of 16—16*a* in 5CP of pilot unit 7. With regard to section 3 of DS1S (Fig. 56), it produces cut off signal ICIS7, cutting off 32 of 32—32*a* in 5CP of pilot unit 7. The cutting off of tubes 12, 16 and 32 in 5CP of pilot unit 7, conditions this pilot unit for control by the main commutator to cause the S1-selected sequence data S1Seq to be entered in electronic storage unit ES7, as will be described in Item 24*b*.

In a similar manner the sections 1, 2 and 3 of dial switch DS2S, set at 8, produce signals OCO8 (Fig. 54), PRES8 (Fig. 55), and ICIS8 (Fig. 56) cutting off the tubes 12, 16 and 32 in 5CP of pilot unit 8. Consequently, pilot unit 8 is conditioned for control by the main commutator to cause the S2-selected sequence data S2Seq to be entered in electronic storage unit 8.

21. *The OCO, PS, NPR and SPR commutator signals.*—Trigger 13X (Fig. 78*j*) was turned (Item 16) under control of trigger 16W (Fig. 78*i*) to produce the SCM and *a1* signals. This caused the OP1 tree to be heated, and also, after a slight delay, caused 18NO (Fig. 78*c*) to be turned, in view of the initial setting of this tree to 00 (see Item 17). The next AP pulse occurring after 13X is turned, restores 13X. In restoring, 13X is

effective to turn 9X. The next AP pulse restores 9X. As 9X restores, it turns 5X and 17X. Trigger 5X, turned, applies reduced potential to 1X and 2X, cutting them off. The increased anode potential of 1X is inverted and amplified by 29X and 30X, producing a negative OCO signal.

At the same time, 2X, being cut off, produces a positive PS signal.

The trigger 17X, turned, serves through inverter 15X to apply increased potential to a grid of 25X. The other controlling grid of 25X is already conditioned by 27X in its initial status. Accordingly, 25X now conducts and turns 26X which thereupon is effective via 19X and amplifiers 31 and 32 to produce negative SPR and NPR signals.

The next AP pulse restores 26X which thereupon restores 17X and turns 27X. With 17X restored and 27X turned, tube 25X is again nonconductive. 27X remains turned so as to keep 25X de-conditioned until an ATD signal (Item 38) is produced. The signals NPR and SPR are of one AP pulse cycle duration as trigger 26X is reversed only for that length of time. The NPR signal is applied to all the pilot units to be utilized by those pilot units which are conditioned for piloting transmission of data other than sequence data out of electronic storage units. The SPR signal also is common to all the pilot units but is used only by the pilot units conditioned to pilot entry and transmission of sequence data; specifically by pilot units 7 and 8 in the assumed example. Either signal will be used by a pilot unit to produce its individual pilot signal PRE (explained in later Item 23).

22. *The OCO signal control of SE and AE return signals and of 32–2CP.*—The negative OCO commutator signal (see Item 21) cuts off 12*a* of the couple 12—12*a* in 5CP (Fig. 80*e*) of each pilot unit. Those couples 12—12*a* which also have had their elements 12 previously cut off by OCO tree signals thereupon produce increased anode potential. In the case under present discussion, only the pilot units 7 and 8 have had their elements 12–5CP cut off (Item 20) and when the companion elements 12*a* are cut off under control of the OCO commutator signal, the couples 12—12*a* of these pilot units 7 and 8 rise in anode potential. For simplicity, the following detailed discussion deals with pilot unit 7. When 12—12*a* in 5CP (Fig. 80*e*) rises in anode potential, it renders 11 conductive causing it to cut off 10 so as to produce a positive OCS7 signal on the wire 130. This signal is transmitted to the control grid of coincidence tube 32–2CP (Fig. 80*b*) of pilot unit 7.

Also, the OCS7 signal, through 26–2CP turns trigger 25–2CP. As trigger 25 turns, it applies increased potential via wire 131 to 18*a*–1CP (Fig. 80*a*), causing this element to reverse trigger 21–1CP. Trigger 21 now applies increased potential to 33*a* and also by way of hand switch 1SQ in Seq position to a tube 33. Accordingly, these tubes are rendered conductive to apply decreased potentials to output wires *se* and *ae*. These wires connect, respectively, to amplifiers 37 and 38 which must be conductive to produce effective negative SE and AE signals to the main commutator. As wires *se* and *ae* are now down in potential, 37 and 38 are cut off and the SE and AE signals are blocked. Attention is called to the fact that the wires *se* and *ae* are respectively common to the tubes 33*a* and 33 of all eight pilot units. Accordingly, wire *ae* will remain at low, ineffective potential as long as any of the tubes 33*a* remains conductive. With regard to the tubes 33, their grids may be connected to the grids of the adjacent tubes 33*a* through the related pilot unit switches 1SQ. However, only the switches 1SQ in those pilot units which are being used for piloting sequence data are placed in seq position, the others being left in norm position. In the example under discussion, therefore, the switches 1SQ of pilot units 7 and 8 alone will be in seq position so that only in these two pilot units will the tubes 33*a* and 33 be simultaneously rendered conductive upon the reversals of related triggers 21–1CP and simultaneously rendered non-conductive upon the resetting of the triggers 21. It is seen therefore that the potential on the line *se* is under control of the tubes 33 in pilot units 7 and 8 which are being used for sequence data entry and transmission. In short, all the pilot units control the production of the signal AE (all entry) while only those pilot units used for sequence data entry and transmission control the production of the SE (sequence entry) signal.

23. *The control of the pilot units by the SPR and NPR signals.*—The negative signals SPR and NPR were produced by the main commutator along with the signals OCO and PS (see Item 21). The control by signal OCO of the pilot units was explained in Item 22. Control of the pilot units by signals SPR and NPR will now be explained. Either the signal SPR or NPR will be applied to the tube 16*a*, Fig. 80*e*, of a pilot unit, depending on the position of the pilot unit hand switch 5SQ. If the pilot unit, such as Unit 7, is being used to pilot sequence data, then its switch 5SQ is set to the seq position, but if the pilot unit is being used to pilot other data, then its switch is set to the norm position. In the full line position of the switch, it conducts the signal SPR to tube 16*a* of the pilot unit, while in the dotted position of the switch it conducts the signal NPR to the tube 16*a*. In the example under discussion, pilot unit 7 is being used to pilot sequence data. Therefore, its switch 5SQ is in full line position and the negative signal SPR cuts off 16*a*, Fig. 80*e*. As previously described, the companion tube 16 is also cut off since wire PRES7 is now adjusted to ground potential (see Item 20). Accordingly, upon 16*a* being cut off, the couple 16—16*a* is effective via 15 and 13 to produce a positive PRE7 signal on the wire 133. This signal renders 35, Fig. 80*c*, conductive, causing it to turn 30.

The turning of trigger 30, Fig. 80*c*, under control of the PRE signal causes 29–3CP (Fig. 80*c*) to be turned. With 29 turned, it cuts off 24*a* of couple 24—24*a*, for a reason which will be explained in Item 31, dealing with the transmission of sequence data from an electronic storage unit to sequence storage.

Further, reversed 30–3CP (Fig. 80*c*) applies increased potential to 35 and also, via switch 4SQ, in seq position, to tubes 35*a*, 23*a* and 17. Tube 17 is thereby conditioned for a purpose brought out in Item 32. Tubes 35 and 35*a* are rendered conductive to cut off tubes 44 and 45, respectively. This prepares tubes 44 and 45 to produce the negative pilot signals AT and STR when 30–3CP later is restored (Item 33). Tube 23*a*, by being rendered conductive, blocks turning of 10–3CP which otherwise would occur when an RDL signal is produced in a manner described in Item 31. The turning of 10 would produce a reset signal on bus 82 of In bus-set 7 which signal has no purpose in connection with transmission of data to sequence storage.

24*a*. *The forward signal delay counter.*—It was

explained in Item 8 that StSeq data has been applied along with the forward signal to Out bus-set 7. The forward signal is applied to bus 81 of the Out bus-set 7. This signal which originates at the +150 v. line (see Figs. 23, 29, 32*a* and 35*b* and Section 9) goes to a grid of switch tube 13–2CP (Fig. 80*b*). In order for the forward signal to render tube 13 conductive, the tube must have been previously conditioned under control of a signal FSR. Referring to Fig. 78*i*, the signal FSR is produced each time a trigger 29W is turned. This will normally occur following the fulfillment of three conditions: (1) The completion of the scanning sequence of commutator spots P, Q, R, T, U and V (Figs. 78*c* to 78*h*); (2) The production of the AED signal which occurs under control of and about 16 ms. after the AE signal (see Item 27); and (3) The production of the signal STRD1 which follows the STR signal by about 10 ms. (see Items 12 and 39).

In the initial situation which characterizes the first run of sequence, the trigger 29W is turned at the very start under control of the first AP pulse within the main commutator. This pulse turns 24W which causes 29W to turn and thereupon the latter acts through 7W to produce a positive FSR signal. 24W remains turned, but 29W is restored by the next AP pulse. The signal FSR, one AP pulse cycle in duration, is transmitted to 19–2CP (Fig. 80*b*) of each pilot unit causing 19 to become conductive so as to reverse the trigger 7–2CP. As a result, the turned trigger 7 conditions tube 13. Hence, when the forward signal is applied to this tube it becomes conductive and cuts off 20 of couple 20—20*a* rendering the couple responsive to AP pulses continually applied to 20*a*. The couple now acts through 22–2CP to transmit negative AP phase pulses to the input 132 of the FS (forward signal) delay counter. As now understood, the first five pulses effect a cycle of elements 14, 15, 16, 17 and 18. As 18 restores at the end of this cycle, it turns 23–2CP. A second cycle of the counter is effected and at the completion of this cycle the negative pulse from 18 restores 23. As 23 restores it produces a negative signal FSD which may be called the Forward delay signal. This signal turns 8. The following BP pulse restores 8 which thereupon restores 7–2CP which has been turned under control of the signal FSR acting through 19–2CP. Now with 7 restored, it deconditions 13 so that 20 becomes conductive and interrupts transmission of AP pulses by the couple 20—20*a* to the forward signal delay counter which will remain in its restored status at the end of the second cycle. The FS delay counter provides a delay in the order of 2 ms. from the Forward signal to the delay signal FSD.

The signal FSD also turns 35–2CP, which thereupon renders 29 conductive, causing 28 to turn. The next AP pulse resets 28, causing it to turn 34. Turned 34 cuts off 33. Tube 33*a* is cut off unless the pilot unit has been operated to store a transmission control signal ICI (see Item 32). In the instant situation, it may be safely assumed that 33*a* is at cut-off when 33 is cut off. The couple 33—33*a* becomes effective to apply increased potential to the suppressor of 32. It has been assumed that the OCS signal as timed by the OCO signal preceded the delay signal FSD and has already turned 25 and is conditioning 32 (Item 22). Hence when the suppressor of 32 receives increased potential under control of the signal FSD, 32 conducts and turns 31. The next AP pulse restores 31 which thereupon resets 25.

As will be brought out in the next Item (24*b*), when 25 is reset it brings about the production of a cancel signal and entry signal for the electronic storage unit. The delay signal FSD may occur before, after, or simultaneously with the OCO signal and its resulting mixed signal OCS. This depends on varying factors which enter into the production of a forward signal. The production of a forward signal, as now understood, accompanies the application of digit signals from a selected data source to an Out bus-set. The selection of a data source is made by Out sequence storage circuits, when these circuits are heated by the closure of contacts of heating relays X1, X2 . . . X6 or Y1, Y2 . . . Y6. Upon the sequence storage circuits being heated, they pick up group and unit out relays or in the case of dial storage, pick up group out relays alone (see Section 8). The group and unit out relays may be called the read-out relays and these close their points to establish paths for the digit signals and the Forward signals to the selected Out bus-sets from the selected data sources. In the case of relay storage and dial storage or the like the data sources are in condition to transmit the digit signals and the Forward signals as soon as the group and unit out relays close their points. In the case of tape storage, a tape may be still in motion at the time that a group-out and station selector close their relay points and the readout circuits will not be established until a designation line of the tape arrives at the sensing position. The Forward signal in that case may occur a varying time after the operation of the group out and station selector relays. In the case of the table look-up operation, special means are provided as will be explained in Section 22 to produce a Forward signal when a desired tape argument has been looked up and checked. The Forward signal in that case may occur a chance time later than the operation of the heating relays for the table look-up group outs and table outs. It is clear then that the Forward signal may occur at varying chance times after the operation of the heating relays for the Out sequence storage circuits. The operation of the heating relays X1, X2 and XM occurs upon the production of the STR signal. The operation of the heating relays X3, X4, X5 and X6 occurs some two AP pulse cycles after the STR signal. It is seen, therefore, that a Forward signal from a selected source may occur at a variable time after the STR signal.

The OCO signal and the signal OCS timed thereby occur about a millisecond after the STRD1 signal which follows the STR signal by about ten ms. (see Item 21). The Forward signal delayed pulse FSD, which follows the Forward signal by about 2 ms., may occur prior to, simultaneously with, or subsequently to the OCS signal. If, as assumed before, the OCS signal comes first, it causes 25–2CP (Fig. 80*b*) to turn and it also causes 32 to be conditioned. The signal FSD then coming along will cause 32 to conduct and through 31 return 25, as previously described. On the other hand, if the signal FSD comes before the OCS signal, it acts through 35 and 29 to turn 28 which thereupon functions to make 26*a* conduct and apply a negative impulse via the anode resistor of 26 to trigger 25, turning this trigger to cause the SE and AE return signals to be blocked. Also, as before, 28 is restored by the next AP pulse and turns 34 to cut off 33 and with 33*a* also cut off, 32 is conditioned. The OCS signal coming along later, will render

32 conductive causing 31 to turn and the next pulse, returning 31, causes the latter to restore 25. If, as may possibly happen, the OCS signal and the FSD signal occur simultaneously, then 25 is turned under control of either signal. Two AP pulses later, 31 functions to reset 25. The effect of resetting 25 is described in the next item.

24b. *The sequence data entry into electronic storage.*—In the preceding item it was explained that 25–2CP (Fig. 80b) was turned and returned under joint control of the signals FSD and OCS. Upon 25 restoring, it applies a positive going pulse via wire 132 to inverter 18–1CP (Fig. 80a) which thereupon turns 22 and 14 in 1CP.

The electronic storage unit cancel signal.— When 22–1CP turns, it renders conductive 16a of normally non-conductive couple 16—16a, causing it to act through an amplifier 4 to produce the cancel signal ESC7 (see also Figs. 21 and 22) as a result of which electronic storage unit 7 is canceled.

The electronic storage unit entry signal Out to ES.—When 14–1CP is turned, it cuts off normally conductive tube 7–1CP, which, through amplifier 1–1CP, produces the negative signal Out to ES7 (Fig. 22). This signal is inverted by an amplifier tube 10 (see Fig. 21) to a positive Out to ES7 signal which is applied to the control grids of all the entry tubes Out En (Fig. 21) of electronic storage ES7. Those entry tubes which have been conditioned by digit representative potentials on Out bus-set 7, thereby become conductive and reverse the associated digit storing triggers of ES7 as soon as the cancel signal ESC7 terminates (see Section 6). In the example under discussion, Out bus-set 7 is carrying the S1Seq data applied to it by station 1, tape storage bank 1, as described in Item 8. Accordingly, the entry tubes Out En of ES7 are being conditioned by Out bus-set 7 according to the digits in the selected S1Seq data. These conditioned tubes will be made conductive by the positive entry timing signal Out to ES7 and the S1Seq data will enter ES7, when the cancel signal ESC7 ends.

The cancel signal (ESC7) started with reversal of 22–1CP (Fig. 80a) upon restoration of 25–2CP at AP pulse time. The next AP pulse restores 22, terminating the cancel signal. As 22 restores, it turns 27. The next AP pulse returns 27 which thereupon restores 14, terminating the entry timing signal (Out to ES7). It is seen that the cancel and entry timing signals start simultaneously but the entry timing signal outlasts the cancel signal by one AP pulse cycle. Accordingly, the conditioned entry tubes Out En (Fig. 21) remain effective, after the unit has been reset, and cause entry of the related data (S1Seq data) into the electronic storage unit.

It is clear from the foregoing that 25–2CP (Fig. 80b) of a pilot unit has to be reset to initiate the cancel and entry signals for the corresponding electronic storage unit. One factor in resetting 25–2CP is the OCS signal timed by the OCO signal (Item 22). The other necessary factor is the delay signal FSD produced by the FS delay counter in 2CP about 2 ms. after the Forward signal. As explained in Item 24a, if the OCS signal should come first, electronic storage reset and entry still will await the forward delay signal FSD. If the forward delay signal FSD should come first, electronic storage cancel and entry signals will await the OCS signal. In any event, resetting of 25–2CP occurs no sooner than 2AP pulse cycles after the FSD signal, and the entry signal does not become exclusively effective until 1AP pulse cycle later or 3AP pulse cycles after the FSD signal. The forward signal accompanies the application of digit signals from a selected value source to an Out bus-set which transmits the digit signals to the entry tubes Out En of the corresponding electronic storage unit. The forward signal circuit and the digit signal circuits are made through relay points. The exact concurrence of the closures of different relay points is difficult to obtain and, hence, the forward signal may occur as much as nearly 2 ms. before the occurrence of the digit signals. Nevertheless, the entry signal Out to ES does not become effective, as explained before, until about one ms. after the FSD signal which follows the Forward signal by some 2 ms. This allows a minimum of about 1 ms. between the closure of the digit signal circuits and the occurrence of the entry signal. In other words, the entry signal (Out to ES) will not be applied to the entry tubes (Out En) until at least about 1 ms. after the digit signals have been applied to these tubes. This is more than sufficient to allow electrical transients and talk across the buses by the digit signals, to die out before the entry timing signal is effective. Such transients may momentarily fail to condition the proper tubes, while the cross talk may momentarily condition the wrong entry tubes (Out En). By delaying the entry timing signal until the transients and cross talk have disappeared, incorrect entries into the electronic storage units are prevented.

The move signal.—Going back to Fig. 80a, the restoration of 27–1CP which was explained before, in addition to restoring 14 to terminate the entry timing signal (Out to ES7) turns triggers 13 and 20. With 13 turned, it serves through normally conductive tube 8 and amplifier 2, to produce a negative going station move signal (SMS7). This signal is applied to bus 82 of the Out bus-set related to the pilot unit. In a manner which has been described in Section 9, the Move signal is effective to cause the selected tape storage station, which has read out its data upon the Out bus-set, to be advanced one line space. In the example under discussion the Move signal SMS7 is applied by pilot unit 7 to bus 82 of Out bus-set 7; and station 1, tape storage bank 1, which has read out a line of data to Out bus-set 7, is line-spaced under control of this Move signal. It is clear from the foregoing that the Move signal and the resulting line spacing of a tape storage station occur after the data from the tape station have been entered into the selected electronic storage unit.

25. *Production of SE and AE return signals.*— Under control of the OCO signal, 21–1CP (Fig. 80a) was turned (Item 22) and rendered tubes 33 and 33a conductive to reduce potentials on lines *se* and *ae*, so as to block the SE and AE return signals to the main commutator. After entry of sequence data into electronic storage, it is to be transmitted therefrom to the then open side A or B of Sequence storage. At this time, the B side is open (Item 6), so the sequence data will be transmitted to this side. Transmission will be initiated by an AE return signal, produced upon the return of high potential to line *ae*.

The line *se* is under control of the two pilot units (7 and 8) which are being used in connection with sequence data and both of these pilot units must have detected the termination

of the entry of sequence data into the respective electronic storage units (7 and 8) before the line *se* can be returned to high potential. The line *ae* is under control of all the pilot units and will remain at reduced potential until all the pilot units have detected completion of entries into their respective electronic storage units. In the initial situation, only the pilot units 7 and 8 are active, since only the entry and transmission of sequence data are under consideration. Accordingly, when pilot units 7 and 8 have detected completion of sequence data entries into ES7 and 8, they will bring about the concurrent return of high potential to lines *se* and *ae*, and amplifiers 37 and 38 thereupon will become conductive to produce the SE and AE return signals.

The restoration of 14–1CP, in pilot unit 7, which terminates the Out to ES7 entry timing signal (Item 24*b*) signifies completion of entry of data into ES7. After a fractional millisecond delay, the tubes 33 and 33*a* of pilot unit 7 will be returned to off status. It was previously explained, under the subheading The Move Signal in Item 24*b*, that triggers 13–1CP and 20–1CP turned at the same time that 14–1CP was restored. The next AP pulse restores 20 which thereupon turns 19. The following AP pulse restores 19 which turns 25. The next BP pulse restores 25, which restores 13–1CP to terminate the Move signal SMS7. Further, as 25 returns, it restores 21–1CP (see Item 22) to reduce the potentials on 33 and 33*a* of pilot unit 7. Assuming similar action in pilot unit 8, lines *se* and *ae* now return to high potentials, and amplifiers 37 and 38 produce the negative SE and AE signals which respectively notify the main commutator that sequence data entry and all entries have been completed. Signals such as AE and SE from the pilot units may be referred to as pilot signals.

26*a*. *Scanning the pilot units.*—While a new line of sequence data is being entered into electronic storage, the main commutator spots, P, Q, R, T, U and V (Figs. 78*c* to 78*h*) act successively to scan the pilot units for their selection by the pilot units selection trees (Figs. 54 to 58) which are set in accordance with the digits in the *b* subfields of the preceding line of sequence data. The preceding line of sequence data is the one which is stored, in the present situation, in the A side of sequence storage and the new line of sequence data is the one which is selected by the A side according to the S1 and S2 code numbers in the preceding line of sequence data. The new line of sequence data was entered in the manner explained in Item 24*b* in electronic storage units ES7 and ES8. This new line of sequence data is to be transmitted from electronic storage to the other side B of sequence storage. Scanning is initiated by the PS signal, produced concurrently with the OCO signal (Item 21) which initiated the operations of the pilot units leading to data entry into electronic storage units. In Item 15*a*, it was explained that the "*a*" signal brought about the heating of the A sides of the OC–ES to Int trees (Fig. 57) and the IC-Int to ES trees (Fig. 58). Since the first, artificial line of sequence data now in the A side of sequence storage, contains only the data S1 and S2 (Item 4), all the sequence storage trees, pyramids and permutation circuits, except the S1, S2 pyramids (Fig. 50), are in zero status. Since the OP2 trees are in zero status, the T tree of the OC–ES to Int group is heated while the T tree of the IC–Int to ES tree is not heated (see Item 15*b*). The heating of the IC-Int to ES trees is not pertinent to the first run of sequence. The heating of the OC–ES to Int trees results in the production of tree signals P*b*O, Q*b*O, R*b*O, T*b*O, U*b*O and V*b*O. These signals cut off tubes 7, 8, 11, 16, 15 and 18 in the blank code chassis BC (Fig. 78L) for a reason which will be made clear in the following items.

Also, the *a*1 signal heated the A side of the OP1 pyramid (Fig. 59) as explained in Item 16. Since this pyramid is at zero status, trigger 18NO (Fig. 78C) was turned under control of the No Op and the SCM signals and is conditioning 25NO (see Item 17). In other words with the OP tree set at zero, the "no operation" commutator NO is conditioned for action.

26P. *The P spot operation.*—The PS signal (Item 21) is directed from the X spot (Fig. 78*j*) to the P spot (Fig. 78*c*) where it is inverted by 12P to turn trigger 16. The next AP pulse restores 16 causing 20 to turn. The second next AP pulse returns 20, causing 23 to reverse. Thus, ½ ms. after the PS signal, 23 acts through 4, and 25 and 26, in parallel, to produce a negative going P1 signal. Also with 23 turned, it applies conditioning potential to a grid of 24.

The negative P1 signal goes to all the pilot units, including units 1 to 8 (Figs. 1 and 80*a*) and blank code pilot unit BC (Fig. 78L), to test for the one selected by a P*b* signal from the P*b* branch of the OC–ES to Int trees (Fig. 57). In pilot units 1 to 8, signal P1 cuts off tubes 2, Fig. 80*e*, but as none of the signals P*b*1 to 8 has been produced, the tubes 2*a*, Fig. 80*e*, are not cut off, so that none of the pilot units reacts to signal P1-In the BC pilot unit (Fig. 78L) signal P1 cuts off 7*a*. Element 7 already is cut off, as explained in Item 26*a*, under control of the P*b*O (OC) ground signal from the OC–ES to Int tree (Fig. 57). Accordingly, 7—7*a* upon receiving the P1 signal acts through 14 and 3 to produce a positive PIL.OC signal. This signal goes to the W spot (Fig. 78*i*) and is inverted by 4*a*W to a negative pulse which turns 3. The next AP pulse restores 3 which then turns 2. The following AP pulse restores 2W but meanwhile when this trigger was turned it applied a negative going impulse to 1 which produced a positive going signal PIL.OCC. This signal, which occurs about ¼ ms. after the PIL.OC signal, goes to grids of all the coincidence tubes 24 in the P, Q, R, T, U and V spots of the main commutator (see Figs. 78*c* to 78*h*). As 24P is the only one which is conditioned at this time, the PIL.OCC signal is effective only on this tube, causing it to produce a negative P.OC signal. This signal turns 21Q (Fig. 78*d*), which may be called the gate of the Q spot.

When 21Q turns, it acts through 25Q to produce a negative signal OP.OC. This signal is applied to the NO (no operation) commutator (Fig. 78*c*), the accumulator operation commutator ACC.C (Fig. 78A), the multiplication operation commutator MYC (Fig. 78M) and the division operation commutator DVC (Fig. 78D). Since no calculating operation has been called for by the OP1 field of the S1Seq portion of the first artificial line of sequence, only the NO commutator will respond to the OP.OC signal. The response results from the fact that as previously explained (Item 17), with no operation called for, 25NO is conditioned. The negative OP.OC signal is amplified and is inverted by 29 and 30, in parallel, to a positive pulse which

renders the conditioned tube 25NO conductive, causing it to turn 21NO. The next AP pulse restores 21NO causing it to turn 22. The following AP pulse restores 22 but, meanwhile, the latter when turned applied a positive pulse to 26, rendering it conductive to produce a negative back signal OP.BS. This signal is applied to the triggers 21 of spots Q, R, T, U, and V. As only 21Q has been turned, the back signal OP.BS restores only this trigger. Upon 21Q restoring, it applies a negative signal "to P" (turn off P) to 23P, restoring it to terminate the P1 signal and the conditioning of 24P, thereby terminating the scanning step of the P spot. The restoration of 21Q also initiates the scanning operation of the Q spot.

It is seen from the foregoing explanation that with subfield P*b* at zero, the P1 signal from the commutator spot acted together with the P*b*O (OC) signal from the OC–ES to Int group of trees (Fig. 57) to cause the blank code pilot unit BC to produce the PIL.OC signal immediately. Under control of this signal, the gate trigger 21Q of the Q spot was turned. When 21Q was turned, it caused an OP.OC signal to be emitted, to test the calculation operation control commutators for conditioning. Since the "no calculation" commutator NO only, was conditioned, it responded to this OP.OC signal to send out, after one AP pulse cycle, an OP.BS back signal which restored 21Q to terminate the OC scanning step of the P spot and initiate the scanning step of the Q spot. In effect, therefore, when no calculating operation is called for, the OP.OC signal is followed with a minimum delay by an OP.BS signal which calls the next commutator spot into operation. In brief, under the stated conditions where the subfield P*b* is at zero and no calculating operation is called for, the P spot operation is momentary and is followed almost immediately by a Q spot operation. This amounts to skipping the P sequence step.

Similarly, under the present conditions, the operations of the Q, R, T, U and V spots will be momentary and equivalent to skipping steps which follow one another in quick succession and skip the Q, R, T, U and V sequence steps. These operations will be explained briefly below.

26Q. *The Q spot operation.*—When 21Q (Fig. 78*d*) is restored, it also turns 22Q. One AP pulse later, 22Q is restored and turns 23Q. 23Q then is effective to condition 24Q and also through 2Q, 30Q and 31Q to emit a negative Q1 signal. This signal cuts off 8*a*–BC (Fig. 78L). Element 8 has already been cut off by the Q*b*O(OC) signal (see Item 26*a*). Accordingly 8—8*a* produces a positive impulse which through 12*a* and 3 emits the PIL.OC signal. As before, this signal is utilized by the W section (Fig. 78*i*) of the commutator to produce the PIL.OCC signal. This signal is effective to operate the conditioned tube 24Q (Fig. 78*d*) which produces the Q.OC signal. The signal is negative and acts to turn 21R, the gate of the R spot. As 21 turns it applies a positive going pulse to the tube 25R which produces the second OP.OC signal. Again the tube 25NO is rendered conductive and initiates the operation of the one AP pulse cycle delay circuits 21 and 22. As before, the delay circuit through 26 produces the OP.BS signal which restores 21R. As 21R restores it emits a negative signal to Q which restores 23Q, terminating the Q spot operation.

26R *The R spot operation.*—Upon 21R (Fig. 78*e*) restoring, it also turns 22. The next AP pulse restores 22, causing 23 to turn. 23, turned, conditions 24 and through 2, 30 and 31, produces the R1 signal which cuts off 11*a*–BC (Fig. 78L). 11 already is cut off by the R*b* (OC) signal. Accordingly, 11—11*a* is now effective through 18 and 3 to produce the PIL.OC signal. As before, this results in a PIL.OCC signal which acts on the conditioned tube 24R (Fig. 78*e*) to render it conductive producing a negative signal R.OC which turns 21T (Fig. 78*f*), the gate of the T spot of the main commutator.

As 21T turns, it applies a positive going pulse to the tube 25T which produces the third OP.OC signal. Again this signal causes the NO commutator (Fig. 78*c*) to produce the OP.BS signal. This signal restores trigger 21T. As 21T restores, it emits a negative signal to R, which restores 23R (Fig. 78*e*), terminating the R spot operation.

26–1. *The a2 signal.*—The successive operations of the P, Q, and R spots of the commutator in performing the OC steps have been described. In effect, these operations successively scanned the P, Q and R fields in the S1Seq portion of a sequence data line. The progress of the P, Q, and R steps was determined by which of the calculation control commutators ACC.C, MY.C, DV.C and NO was conditioned under control of the OP1 pyramid (Fig. 59). The OP1 pyramid was heated by the *a*1 signal (Item 16). Now that the P, Q, and R commutator steps have been completed, the *a*1 signal is to be terminated. The next series of steps will be steps performed by the T, U and V spots of the commutator with respect to the S2Seq portion of the line of sequence data. The progress of the T, U and V steps will be determined in accordance with the setting of the OP2 pyramid (Fig. 59). In order to bring this OP2 pyramid into control, it will be heated under control of an *a*2 signal which will be produced upon termination of the *a*1 signal. The OP2 code number will then be read out to determine which of the calculation control commutators is to be conditioned. The production of the *a*2 signal and the termination of the *a*1 signal is under control of the trigger 23R of the R spot (Fig. 78*e*). It will be recalled that this trigger is restored at the end of the R spot operation (Item 26R).

As 23R returns, it applies a positive going impulse by way of a capacitor 135 to the normally cut off tube 26 of the couple 26—26*a* in the R spot, rendering 26 conductive. The element 26*a* is normally cut off by 15R. Accordingly, upon 26 becoming conductive, the lock couple applies a negative pulse to 32R which produces a positive going FR (finish of R spot operation) signal. The signal renders 19NO (Fig. 78*c*) conductive causing it to produce a negative pulse for restoring 18 from its previously turned condition (see Item 17). Accordingly, tube 25NO is deconditioned. In short, upon the finish of the scanning of the S1Seq half of the sequence data line, the commutator NO is deconditioned.

The positive signal FR also acts through 1P (Fig. 78*c*) to turn 5 which is the first trigger of the Ink delay counter. In other words, the FR signal starts the Ink delay in operation again to produce the Ink signal (see Item 17). One purpose of the Ink signal is to test the different commutators NO, ACC.C, DVC and MYC for conditioning by the OP1 and 2 pyramids.

The positive signal FR also goes to the Z spot (Fig. 78*k*) and is inverted by 25*a* of this spot to a negative going impulse which turns trigger 26Z. 26Z now renders 19*a* conductive, terminat-

ing the *a1* signal (see Item 16). Further, **26Z** is now applying cut off potential to **27** of the couple **27—27***a*. The element **27***a* is already cut off under control of **39Z**. Accordingly, when **26** turns to cut off **27**, the couple **27—27***a* becomes effective to apply increased potential to **28** rendering it conductive to produce the negative *a2* signal. This signal is inverted by **2** and **8** in **9CF** (Fig. 76*a*) and applied to **32, 33, 34** in **9CF** and to **1** to **6, 8** and **9** in **10CF** (Fig. 76*b*). These tubes become conductive, heating the A sides of the U, V, and SH2 shift code combinational circuits (Figs. 63 and 62) and also of the **OP2** pyramid (Fig. 59). As this pyramid is set at 00, again a **No Op** signal is produced (see Item 17), as a result of which **25NO** (Fig. 78*c*) is again conditioned.

26T. *The T spot operation.*—At the end of Item 26R, it was explained that **21T** (Fig. 78*f*) was restored, terminating the R spot operation. Upon restoration of **21T** it turns **22T**. The next AP pulse restores **22T** which turns **23T**. With **23T** turned, it conditions **24T**, and serves through **2, 30** and **31** to produce a negative **T1** signal. This signal cuts off **16***a* in the BC pilot unit (Fig. 78L). Element **16** already is cut off by the TbO(OC) signal (Item 26*a*). Accordingly, **16—16***a* in BC now becomes effective through **12** to cut off **3** which again produces a PIL.OC signal. As before, this signal is acted on in the W section (Fig. 78*i*) to produce the PIL.OCC signal which renders the conditioned tube **24T** (Fig. 78*f*) conductive to apply a turning pulse T.OC to **21U**, the gate of the U spot (Fig. 78*g*). As **21U** turns, it acts through **25** to produce the OP.OC signal. As before, the conditioned NO commutator (Fig. 78*c*) responds and sends back an OP.BS signal. This restores **21U**, causing it to produce a negative signal "to T," which restores **23T**, terminating the T spot operation.

26U. *The U spot operation.*—Upon restoration of **21U** (Fig. 78*g*), it turns **22U**. The next AP pulse restores **22** which turns **23**, conditioning **24U** and acting through **2, 30** and **31** to produce the negative **U1** signal. This signal cuts off **15***a* of the BC pilot unit (Fig. 78L). **15** is already cut off under control of the UbO (OC) signal (Item 26*a*) tree now at **0**. Accordingly, **15—15***a* now becomes effective to render **14***a* conductive, causing **3** to be cut off so as to produce the positive PIL.OC signal. Again the W spot (Fig. 78*i*) converts this to a PIL.OCC signal. This goes back to the conditioned tube **24U** (Fig. 78*g*), rendering it conductive to apply a turning signal U.OC to **21V** (Fig. 78*h*). As **21V** turns, it acts through **25** to apply an OP.OC signal to the NO commutator (Fig. 78*c*) which sends back an OP.BS signal, restoring **21V**. Upon **21V** restoring, it emits a signal to U which restores **23U**, terminating the U spot operation.

26V. *Operation of the V spot.*—When **21V** (Fig. 78*h*) restored, it turned **22V** which then was restored by an AP pulse and thereupon turned **23** to condition **24V**. Also **23** through **2, 30**, and **31** produces the negative **V1** signal. This cuts off **19***a* (Fig. 78L). **19** already is cut off under control of the VbO (OC) signal (Item 26*a*). Accordingly, **19—19***a* becomes effective through **18***a* and **3** to produce the PIL.OC signal. This is inverted by the W spot (Fig. 78*i*) to a PIL.OCC signal which renders the conditioned tube **24V** (Fig. 78*h*) conductive to apply a negative signal V.OC to **17W** and **21W** (Fig. 78*i*). Trigger **17W**, which was turned before (see Item 14), is now restored by the signal V.OC. Trigger **21** is turned by the impulse received from **24V**. The next AP pulse restores **21W** causing it to produce a negative signal "to V" for restoring **23V** to terminate the V spot operation.

26–2. *Commutator finish operations.*—Trigger **17W** (Fig. 78*i*), upon restoration (Item 26V) applies a negative going impulse to **5W** which produces a positive signal FC. This is inverted by **29***a* in the Z spot (Fig. 78*k*) to a negative going impulse which turns trigger **30**, dropping out the *a2* signal (see Item 26–1).

Further, with **17W** (Fig. 78*i*) restored, it cuts off **18W**, establishing one condition for start of a next commutator run. Another condition is established under control of an all-entry delay signal AED which follows the all-entry signal AE (Item 25) by about 16 ms. As now understood, signal AE is emitted by the pilot units when all entries into electronic storage called for by a line of sequence data have been completed. One of the functions of the AE signal is to initiate operation of delay means to produce the AED signal, as described below.

The positive FC signal also is applied to tube **19***a* in Fig. 78*c*. The tube **19***a* becomes conductive and through the plate circuit of **19** applies a negative pulse to the gate trigger **18** of the commutator NO, restoring this trigger (Item 17) from its previously turned condition. With **18** restored, it renders **27** conductive thereby deconditioning **25**. In short, at the finish of the present commutator scanning operation, the commutator NO is deconditioned.

27. *The all-entry delay signal AED.*—The negative all entry-pilot signal AE (Item 25) goes to the X spot (Fig. 78*j*) of the main commutator, where the signal is amplified by **10***a* and **12** to be sent out to Fig. 75*a* as a negative commutator signal AE. This commutator signal AE is inverted by **6–1CF** (Fig. 75*a*) to a positive going signal AE on wire **150**. The positive signal is inverted by **19** in **2CF** (Fig. 75*b*) to a negative impulse which turns **20**. **20** thereupon cuts off **26** of the lock couple **26—26***a*, making the couple responsive to EP pulses continually acting on **26***a*. Accordingly, the lock couple now is effective, through **25** to apply negative EP phased pulses to the common input line of the primary order of the All-Entry Delay Counter. This counter includes, as its primary order, the triggers **31, 32, 33, 34** and **35**. In the now familiar manner, at the end of the first cycle of this order, it turns **36** to turn **30**. The next cycle restores **30** which turns **24**. The third cycle restores **24**, causing **23** and **29** to turn. The next EP pulse restores **29**, which turns **28**. At this point, **28** serves through **27** to produce a positive AED signal on wire **151**. Trigger **28** is returned by the next EP pulse. A fourth cycle of the primary order resets **23**, which restores **36** and turns **22**. The next BP pulse resets **22**, which restores **20**, ending operation of the delay counter.

The positive AED signal on wire **151** is inverted by **2–1CF** (Fig. 75*a*) to a negative signal AED called the all-entry delay signal. This signal goes to the W spot (Fig. 78*i*) of the main commutator and acts through cascaded tubes **20***a* and **20** to restore **19** (note Item 14). Trigger **19** now cuts off **18***a*, which is another condition for restarting the operation of the commutator. A previously discussed condition is the cutting off of **18** as a commutator finsh operation (Item 26–2). When both **18** and **18***a* are at cut-off, the couple **18—18***a* conditions **14W**. As a final condition to restarting the commutator, **14W** will

have to be rendered conductive by the turning of trigger **23** under control of an STRD**1** negative signal. The first such STRD**1** signal was produced (see Item 12) under control of the first STR pulse which resulted from operation of the start key (Item 5). Trigger **23**W was turned by the first STRD**1** signal and restored shortly after (Item 14). The next STRD**1** signal will be produced after transmission of sequence data out of electronic storage has taken place. Such transmission is initiated under control of the all-entry signal AE (Item 25) and will be explained in Section 31.

28. *Dropping XM and X2 and X3, X4, X5 and X6.*—The positive going signal AE (see preceding Item 27), in addition to bringing the AE delay circuit (Fig. 75*b*) into operation, also acts via inverter **23–5**CF (Fig. 75*e*) to turn **22**. With **22** turned, it renders **21***a* conductive, releasing the couple **21—21***a*, to cause deenergization of the relays XM and X**2** (note Item 9). At the same time, the turned trigger **22** cuts off **27** of couple **27—27***a*. Since trigger **28–5**CF is now also in turned condition (Item 9), it is still keeping **27***a* conductive, so that the lock couple does not serve, as yet to bring about the energization of the relays YM and Y**2**.

The positive AE signal on wire **150** also goes to **30–6**CF (Fig. 75*f*) to be inverted to a negative going AE pulse on wire **152**. This negative pulse resets **18–6**CF, **12** and **24** in 7CF (Fig. 75*i*) and **6–8**CF (Fig. 75*h*). Accordingly, the relays X**3**, X**4**, X**5** and X**6** are deenergized (note Items 10 and 11).

29. *Dropping X*1:—The negative SE pilot signal (Item 25) which in the present situation was produced by the pilot section at the same time as the all-entry signal AE, goes to the Z spot (Fig. 78*k*) of the main commutator where it is amplified by **5***a* and **8** to be sent out as a negative-going commutator signal SE. This signal is inverted by **5–1**CF (Fig. 75*a*) to a positive SE signal on the wire **154**. The positive SE signal operates **11–5**CF (Fig. 75*e*) to turn **10**. With **10** turned, it renders **9***a* conductive, releasing the lock couple **9—9***a*, as a result of which the relay X**1** is dropped (note Item 7). The points *a* of X**1** re-open and cease to ground the A sides of the S**1**, and S**2** pyramids (Fig. 50), these having completed their function of controlling the section of the next line of sequence data to go into the B side of sequence storage (see Item 8).

The SE pilot signal also operates through **5***a* and **5** (Fig. 78*k*) to return **9**Z which previously was turned (see Item 14). With **9**Z returned, it deconditions **14**. This prevents a stop signal, which is a down signal on wire SPST, from having any effect at this time in stopping the commutator at the end of its present run, but it will have the effect of stopping the commutator at the end of its next run. In other words, after the SE signal is given, the stop signal is ineffective for the present run. Trigger **17**W remains turned and conditioning **13**. The next STR pilot signal will return **10**Z which will operate conditioned **13** to produce a new STR commutator signal. The subsequent STRD**1** signal will turn **10**Z and **9**Z. Assuming that the stop signal on wire SPST is present, then **14**Z will be conditioned and so upon **9**Z being turned it will apply increased potential to conditioned **14**Z to render **14**Z conductive so as to return **17**Z. Accordingly, the means for producing another STR commutator signal will be rendered ineffective and so a subsequent STR commutator signal will not be produced until another start key operation is effected.

30. *S entry delay signal SED.*—The positive SE signal also is inverted by **13–8**CF (Fig. 75*h*) to a negative going impulse which reverses **14**. Trigger **14** now cuts off **20** of couple **20—20***a*, making the couple responsive to the applied EP pulses. The couple now acts through **19** to apply negative pulses to the common input of the ring of triggers **25**, **26**, **27**, **28**, and **29** of the SE delay counter. As now understood, a first series of five pulses operates the ring to reverse **30**, which reverses **23** and **24**. The third pulse of the second series restores **27** to turn **28** and, also, to reset **23**. As **23** resets, it applies a positive pulse to **21** to produce the negative SED signal on a wire **166**. There is a delay of approximately 8 ms. between the SE signal (Item 25), and the SED pulse. The SED signal will restore **10** and **22** in 7CF (Fig. 75*g*) and **16** in **16** and **6**CF (Fig. 75*f*) if these triggers are turned, which is not the case at present. The triggers **10** and **22** in 7CF may be selectively turned when "late" operations are performed (see later Section 21).

In the now familiar manner, **24–8**CF (Fig. 75*h*) is restored and turns **18** at the end of the second cycle of the ring circuit in the SE delay counter. A third cycle restores **18** to turn **17**. A fourth cycle restores **17** to turn **16** which is returned by the next BP pulse and thereupon resets **14** to terminate operation of the delay counter.

31. *Transmission of sequence data from electronic storage to sequence storage.*—The negative all-entry pilot signal AE (Item 25), in addition to its functions explained in Items 27 and 28, also initiates operation to bring about the transmission of the sequence data now in ES**7** and ES**8** to the open side of sequence storage, this open side being, at present, the B side. Referring to Fig. 78*j*, the AE pilot signal acts through tubes **10** and **10***a* to restore **5**X, terminating the commutator timing signal OCO (Item 21) which initiated the events leading to the application by the selected pilot unit **7** of the entry timing pulse Out to ES**7** to the entry tubes Out En of electronic storage unit **7** (see Item 24*b*). Restoration of **5**X also terminates the PS signal (Item 21) which initiated scanning operations (see Item 26*a*). Further, as **5**X restores, it turns **7**X, which through **3**X and an amplifier **35—36** produces a negative signal SW. The next AP pulse restores **7**X, terminating the SW signal. Meanwhile, the signal SW goes to **5**CP (Fig. 80*e*) where it cuts off tube **32***a* of couple **32—32***a*. Element **32** of this couple has already been cut off (Item 20) by ground signal ICIS**7** through section **3** of dial switch DS**1**S (Fig. 56), set to position 7. Accordingly, upon **32***a* now being cut off by the SW signal, the couple applies increased potential to **39–5**CP which becomes conductive and cuts off **34–5**CP to produce a positive ICI**7** signal (Fig. 79*c*). This signal renders **26–3**CP (Fig. 80*c*) conductive to turn **20–3**CP and also, through switch **2**SQ, in seq position, to cut off **24** of couple **24—24***a* in 3CP. The turned trigger **20–3**CP cuts off **14***a* of couple **14—14***a* in 3CP. The ICI**7** signal initiated by the SW signal and the ICIS signal (Item 20) has thus caused **24** and **14***a* in 3CP to be cut off. Element **24***a* has been cut off previously under control of trigger **29** (Fig. 79*c*) and the presense signal

SPR (Item 23). The SPR signal as described in Item 23, mixed with the signal PRES to produce the signal PRE. Under control of signal PRE, trigger 30–3CP turned and caused 29 to turn, as a result of which 24*a*–3CP is cut off. Under control of the later ICI signal, 24 is also cut off. When at the next BP pulse time, 27*a* is cut off, the common anode line of 24—24*a*—27*a* rises in potential and makes 18 conduct, which turns 33. Turned 33 cuts off 26*a* to produce a positive RDL signal. This signal, through 19, turns trigger 13 to cut off 14 of couple 14—14*a*. Since element 14*a* has also been cut off by turned 20, as explained above, 14—14*a* now is effective via 7–3CP to turn trigger 16. Trigger 16, turned, cuts off normally conductive switch tube 8–3CP to emit a positive pulse which causes amplifier tubes 3 and 3A to produce the positive transmission timing pulse ES to In (also see Figs. 21 and 22). In the manner described in Section 6, this positive pulse ES to In emitted by pilot unit 7 causes the value in electronic storage unit ES7 to be applied through the In Ex C couples and the In Ex tubes, as reduced digit representative potentials upon In bus-set 7.

In the assumed example, ES7 has received the S1Seq sequence data (see Item 24*b*) which are now transmitted to In bus-set 7. In the manner described in Section 11, the S1Seq data on In bus-set 7 are entered in the then-open A or B side of sequence storage. At present, the B side is open (see Item 6) since relay BM (Fig. 36) is energized. Therefore, the S1Seq data now enter the B side of sequence storage, and the BI relays (Fig. 37) are selectively energized in accordance with the S1Seq data. Relays BI close their contacts *b* (Fig. 41), establishing the pick up circuits of relays BOP for storing the sequence data S1Seq.

While operations have been described in detail with respect to pilot unit 7 and the S1Seq data, it is to be understood that pilot unit 8 acts similarly, under control of commutator signal OCO, to pilot the S2Seq data into electronic storage unit ES8 and, under control of commutator signal SW, to pilot the transmission of data from this storage unit to the S2Seq relays BI and BOP.

The relays BI and BOP set the B sides of the various trees, pyramids and permutation circuits (Figs. 47*a* to 63) according to the new, first real line of sequence data which was obtained from tape storage stations 1 and 10 of bank 1 (see Item 8) in the assumed example.

The positive RDL pulse, which initiated the transmission signals ES to In, occurred upon the turning of 33. The next AP pulse returns 33, causing it to restore 29, which has served its purpose in impressing the stored presense signal upon 24*a* which was a factor in producing the RDL signal.

It should be noted that control of a pilot unit for piloting transmission of sequence data is by commutator signals SW and SPR (presense). As will be brought out in Section 17, Items 22 to 24, the control of a pilot unit for piloting transmission of data other than sequence data is by the "3" signal of a scanning spot (see Section 16*a*), the presense signal NPR, and a Back signal from the data receiving unit.

32. *The transmission delay.*—As explained in the preceding item, the trigger 16–3CP (Fig. 80*c*) was reversed to cause the signal ES to In to be produced for timing the transmission of the S1Seq data to the open side B of sequence storage. The reversal of the trigger 16 also, through 2, applies increased potential to 22 and 17 in 3CP. 17 has been conditioned already by the now-reversed trigger 30–3CP (see Item 23). Accordingly, when trigger 16 reversed to start the transmission from electronic storage and, through 2, applied increased potential to tube 17, this tube became conductive. Tube 17 then cuts off switch tube 12–3CP, which has been held conductive by unturned 11. 11 can be turned only upon return of 10. But 10 is blocked from turning (see the end of Item 23) and hence will not have a return action. Accordingly, 11 will not turn and will hold 12 conductive until cut off upon 17 becoming conductive. At that point 12 produces a positive pulse TRS to start the 7½ ms. transmission delay. The pulse TRS is inverted by 1–4CP (Fig. 80*d*) to reverse 2–4CP which thereupon cuts off 8*a* to render couple 8—8*a* responsive to the CP pulses continually applied to 8. The couple 8—8*a* now acts through 7 to impress negative pulses on the common input of triggers 13, 14, 15, 16 and 17 of the Transmission Delay Counter in 4CP. In a now familiar manner, each series of five pulses effects a cycle of these five triggers, the trigger 17 being restored at the end of each cycle. The first time 17 restores, it reverses 18. In turn, 18 reverses 12. The second time 17 restores, it resets 12, which turns 6 to also turn 11. The counter goes through a third cycle and this time 17, upon restoring, resets 6, which turns 5 and the latter thereupon returns 11. The fourth cycle of the counter causes 17, upon its restoration, to restore 5, which turns 4 and restores 18. The next BP pulse restores 4. As 4 restores, it resets 2 to stop operation of the counter.

At the end of the third cycle of the counter, 11 was restored. Thereupon 11 produced a positive TRD pulse. This pulse is inverted by 18*a*3CP (Fig. 80*c*) to a negative pulse which restores 16, terminating the ES to In signal. The delay counter in 4CP has permitted 16 in 3CP to remain conditioned for approximately 7½ ms. which is, therefore, the duration of the ES to In signal. This exceeds the time required for relay points, such as those of sequence storage relays BI, to shift from one position to the reversed position. To provide sufficient tolerance, 7½ ms. is allowed for transmission of data from electronic storage unit to a receiving unit such as sequence storage or relay storage.

33. *The reset delay and pilot signals STR and AT.*—The positive RDL signal in conjunction with signal ICI turned 16–3CP to produce the ES to In signal (see Item 31). The RDL signal also initiates the operation of a Reset Delay Counter in 4CP (Fig. 80*d*). The pulse RDL is reversed by 19–4CP to turn 20–4CP, which then cuts off 26*a* to make the couple 26—26*a* respond to the EP pulses applied to 26. Through 25, the couple then impresses negative EP-phase pulses on the common input wire of the triggers 31, 32, 33, 34 and 35 of the reset delay counter. The first cycle (5EP pulses) of these triggers produces a pulse which turns 36, which reverses 30. The second cycle restores 30. Upon restoration of 30, it turns 24 which thereupon turns 28. The third cycle restores 24 and 28. As 28 restores, it produces a positive RDL #2 pulse, which has no real function when a pilot unit is used to pilot sequence data. When a pilot unit is used for piloting other than sequence data, trigger 10–3CP may be turned to produce a

Reset signal for resetting a relay storage unit. The RDL #2 pulse will then cause **10** to return (see Item 24, Section 17). When **24–4CP** restores, it turns **23**, which reverses **29**. A fourth cycle restores **23** and also **29**. As **29** restores, it produces a positive RDL #3 pulse. When **23** restores, it resets **36** and turns **22**. The next BP pulse restores **22** causing it to reset **20**, terminating operation of the reset delay counter.

The positive RDL #3 pulse, produced at the end of the fourth cycle, is inverted by **34–3CP** (Fig. 80*c*) to a negative impulse which is applied via a switch **3SQ**, in seq position, to **15–3CP**, turning it. The next AP pulse returns **15**. As **15** returns, it turns **21**. A following AP pulse returns **21**, which causes the inverter **27** to apply a negative impulse to **13**, **20**, and **30**, restoring them.

It may be noted that the RDL #3 pulse occurs some 20 ms. after the RDL signal, while the transmission signal ES to In lasted some 7½ ms. (see Item 32) after the RDL signal. Accordingly, it is understood that triggers **13**, **20** and **30** are restored after the transmission from electronic storage has taken place. With **20** returned, it is ready for control by the next ICI signal (Item 31). The return of **13** conditions it for response to the next RDL signal (Item 31). With **30** returned, it is prepared for operation upon the production of the next PRE signal (Item 23). Further, when **30** in each of pilot units **7** and **8** restores, it returns **35** and **35***a* in 3CP to cut-off condition. None of the tubes **35** and **35***a* in the other pilot units have been switched from their normal cut-off condition. Accordingly, when **35** in pilot units **7** and **8** is returned to cut-off condition, the single tube **44** common to all the pilot units becomes conductive to produce a negative AT (all-transmission) signal. Similarly, return of **35***a* in pilot units **7** and **8** causes common tube **45** to produce a negative STR (S transmission) signal (see Item 12). The plate circuits of tubes **35** of all the pilot units are commoned and if any of the tubes **35** remain conductive, then tube **44** will remain cut off and the AT signal will not be produced. The plate circuits of tubes **35***a* of all the pilot units also are commoned, but only the tubes **35***a* of the two pilot units used in connection with sequence entry and transmission are placed by their switches **4SQ** in control of the STR signal. At present, only pilot units **7** and **8** are active and set for control of sequence data entry and transmission. Accordingly, that pair of tubes **35** and **35***a* of pilot units **7** and **8** which is last cut off causes the AT and STR pilot signals to be produced, simultaneously in the present situation, to signal that all data and sequence data transmissions are completed.

34. *BOR.*—Trigger **7X** (Fig. 78*j*) was turned (Item 31) to produce the SW signal which, mixed with the ICIS signal (Item 20), initiated sequence data transmission to the B side of sequence storage. One AP pulse cycle later, **7X** is restored and through **4X** produces a negative going signal ICIC. This signal is inverted by **1–1CF** (Fig. 75*a*) to a positive signal which acts through **1–4CF** (Fig. 75*d*) to turn **8–4CF**, which cuts off **3A**. As **3** is already cut off at this time by **2–4CF**, the couple **3—3***a* now is effective through **9** to turn **10** of an ICIC 3 ms. delay circuit. The next EP pulse restores **10** to cause **11** to turn. The second next EP pulse restores **11** which thereupon turns **12**. The third next EP pulse restores **12**. As **12** is restored it turns **18** which then cuts off **17***a*. Element **17** already has been cut off by the trigger **16** which was reversed previously (see Item 5) to drop relays AOR. The couple **17—17***a* is now effective through **20** to apply decreased potential to wire *bor*. Tubes **42** to **46–18CF** (Fig. 77*c*) consequently are cut off, causing tubes **50** to **76** to conduct and drop the potential on their output lines *borr*. Consequently, relays BOR (Fig. 36) are energized and their contacts *a* (Fig. 41) open so as to drop those BOP sequence storage relays which may previously have been held by their stick circuits and are not being energized by the pick up circuits through contacts *b* of relays BI (see Item 31).

When **12–4CF** (Fig. 75*d*) was restored at the end of the 3 ms. delay, it made **9***a* conduct so as to reset **8** and to turn **2**. When in a next sequence run, a presence signal NPR is produced, it will act via **1***a* to reset **2**. This is one condition to restart of operation of the ICIC delay circuit, the purpose of which is to pick up the B or A operational reset relays 3 ms. after transmission to the B or A side of sequence storage starts. The other condition to restart of this delay circuit is the signal ICIC which occurs whenever a transmission signal SW is given.

35. *Dropping BM and re-energizing AM.*—As explained in Item **33**, the STR and the AT pilot signals were produced at the end of a reset delay which occurred after the transmission of sequence data into the B side of sequence storage. The negative STR pilot signal is applied via **6***a* and **6** in the Z section (Fig. 78*k*) to **10Z**, restoring it from its previously turned status (see Item 14). Trigger **10** now re-applies increased potential to the control grid of **13Z** which remains conditioned by **17Z** turned under control of the start key **SKS** (see Items 5 and 14). Accordingly, **13Z** through **18** and **12** causes a negative going STR commutator signal to re-appear. It is to be noted that this commutator signal was produced the first time under control of the start key switch. Thereafter, it re-appears each time an STR pilot signal is produced. As in Item 5, the STR commutator signal is inverted by **4–1CF** (Fig. 75*a*) to a positive going STR signal on wire **101** which is inverted by **3–5CF** (Fig. 75*e*) to a negative going pulse applied to both sides of trigger **2–5CF**. The first STR pulse turned this trigger (see Item 5). The second STR pulse now returns trigger **2**. This trigger is thus alternated in status by successive STR signals. Trigger **2–5CF** now restored, serves through **17***a* to make **1***a* conduct so that wire *bm* drops in potential whereupon the relay BM is deenergized, in turn dropping relays BS (see Item 6.)

With trigger **2–5CF** turned, it also applies increased potential to **17**, which through **1** causes wire *am* to rise in potential so that relay AM is again energized (note Items 1 and 5).

The STR signal on wire **101** also, makes **24** conduct to reset **16** (note Item 5). Consequently, **17** is made conductive, with the result that relays BOR are deenergized (see Item 34), causing the stick circuits of the energized relays BOP to close.

It is clear now that the A side of sequence storage is initially open (Item 1) to receive sequence data (Item 4) while the B side is initially closed. After sequence data was read into the A side of sequence storage (Item 4), the start key was depressed to produce a first STR commutator signal (Item 5) and relays AM, AS and AOR were deenergized, while relay BM and its subsidiary relays BS were energized (Item 6) to open the B side of sequence storage. The first real line of sequence data, selected by codes **S1** and **S2** in

the A side of sequence storage, was then applied to electronic storage (Item 24*b*) and sent therefrom to the B side of sequence storage (Item 31). The STR pilot signal was then given (Item 33) after a short delay. Now the B side of sequence storage has been shut by the dropping of relays BM and BS and the A side of sequence storage has been reopened by the picking up of AM and AS relays. In this manner the A and B sides of sequence storage receive alternate lines of sequence data, the line going into each side being selected by the S1 and S2 codes in the other side of sequence storage.

It is also clear that alternate STR signals drop the relays AOR and BOR; that is, after the sequence data has been safely transmitted to the open side of sequence storage, the STR signal drops the operational reset relays for this open side, so as to allow the stick circuits of the operational relays for the open side to be established.

36. *Relays Y1, Y2 and YM, and Y3 to Y6.*—The positive going STR control frame signal on wire **101** (see the preceding item) acts via **11***a*—**5CF** (Fig. 75*e*) to apply a negative going impulse to both sides of **16** restoring it from its previously turned condition (see Item 7). The restored trigger **16** now cuts off **15***a*. Previously, trigger **10**–**5CF** was turned under control of signal SE (see Item 29) and dropped X1. With **10** turned, it is cutting off **15**. Accordingly, when **16** also is turned to cut off **15***a*, the couple **15**—**15***a* becomes effective through **8** and **7***a* to apply increased potential to wire *y1*. Thereupon tube **24**–**19CF** (Fig. 77*d*) becomes conductive and its output line *y1r* drops in potential, so that relays Y1 and Y1D (Fig. 36) are energized. Contacts Y1*a* close and ground the B side of the S1, S2 trees (Fig. 50).

The STR positive pulse also acts through **23***a*–**5CF** (Fig. 75*e*) to apply a negative going pulse to both sides of trigger **28**, restoring it from the turned condition (see Item 9). As **28** is restored it cuts off **27***a*. Trigger **22**–**5CF** was previously turned under control of the all-entry signal AE and dropped X2 and XM (see Item 28) so that **27** also is cut off. Accordingly, the couple **27**—**27***a* is now effective to apply increased potential to wire *y2w* and also through **20** and **25** to apply increased potential to the wire *y2*. The tubes **22**, **23** and **28** to **30** (Fig. 77*d*) become conductive and output lines *ym* and *y2r* drop in potential, causing relays Y2, YM, and YMD (Fig. 36) to be energized. The increased potential on wire *y2w* is inverted by **28**–**6CF** (Fig. 75*f*) to cut off **26**. As explained in Item 10, the STR pulse operates through the "Late" delay circuit in **6CF** to cause **8** to conduct momentarily so as to cut off **26***a*. Accordingly, the couple **26**—**26***a* becomes effective through **6** to produce a negative pulse, on wire **175**, to turn **24**–**6CF**, **18** and **30**–**7CF** (Fig. 75*g*) and **12**–**8CF** (Fig. 75*h*). **24**–**6CF** in turned state applies increased potential to a grid of **23**. The other grid already is at increased potential under control of the trigger **16** in its standby state, so **23** now becomes conductive and through **19** causes an increased potential to appear on line *y3*. Tubes **10**, **11**, **12** in **15CF** (Fig. 76*g*) become conductive so that output line *y3r* drops in potential. Similarly, the turned trigger **18**–**7CF** (Fig. 75*g*) and trigger **10** combine to render **17** conductive so that **13** is cut off and applies increased potential to wire *y4*. Tubes **16**, **17** and **18** of **15CF** (Fig. 76*g*) become conductive and output line *y4r* drops in potential. The turned trigger **30**–**7CF** (Fig. 75*g*) and trigger **22** now render **29** conductive cutting off **25** for applying higher potential to wire *y5*. The tubes **22**, **23** and **24**–**15CF** become conductive and output line *y5r* drops in potential. Finally the turned trigger **12**–**8CF** (Fig. 75*h*) and trigger **4** combine to render **11** conductive, cutting off **7** to bring about an increase of potential on wire *y6*. Tubes **28**, **29** and **30**–**15CF** conduct and their output line *y6r* drops in potential.

As a result of output lines *y3r*, *y4r*, *y5r* and *y6r* dropping in potential, the relays Y3, Y4, Y5, and Y6 (Fig. 36) are energized.

The relays Y2, YM, Y3, Y4, Y5, and Y6 close their respective points in the B sides of the Out sequence permutation circuits shown in Figs. 47*a* to *d*, 48, and 49 and *b* (see Section 11).

37. *The Y7 relays.*—The pilot signal AT, which in the present situation was produced concurrently with the pilot signal STR (see Item 33) goes to the X section (Fig. 78*j*) of the main commutator and through **24** and **20** produces the commutator signal AT. This signal is inverted by **12**–**1CF** (Fig. 75*a*) to a positive AT signal. This positive signal is again inverted by **4**–**3CF** (Fig. 75*c*) to turn **3**. As **3** is turned, it makes **2** conduct and drop the potential on wire *x7* (see Item 3). As a result, relays X7 and X7D (see Item 3) are deenergized. The turned trigger **3** also works through **1**–**3CF** to produce a higher potential on wire *y7* so as to make tubes **4**, **5**, and **6** in Fig. 77*c* conductive so that output lines *y7r* (also see Fig. 36) drop in potential and relays Y7 and Y7D are energized. Relays Y7 close points in the B side heating circuits of the In permutation circuits shown in Figs. 51, 52*a* and 52*b*.

38. *Reconditioning 25X in preparation for the next SPR and NPR signals.*—The positive AT signal (see the preceding item) is also applied to **1**–**2CF** (Fig. 75*b*) to be inverted to a negative pulse which turns **2** cutting off **8** to render the couple **8**—**8***a* responsive to the EP pulses. The pulse output of this couple is applied by **7** to the common input of the All-Transmission Delay Counter in **2CF** which is a duplicate of the All-Entry Delay Counter described in Item 27. The All-Transmission Delay Counter at the end of about 15 or 16 ms. produces through **9**–**2CF** a positive ATD pulse. This pulse is inverted by **3**–**1CF** to a negative ATD pulse which goes to the X spot (Fig. 78*j*). The negative ATD pulse is applied via **28***a* and **28** to 27X and restores it to recondition **25X** (see Item 21) in preparation for production of the next SPR and NPR presense signals.

39. *The b and b1 signals, relays BIR and the restart of commutator scanning.*—In Item 26–2 it was explained that **17W** (Fig. 78*i*) is restored by the V.OC signal at the end of a scanning sequence (also see Item 26V) to cut off **18** as one prerequisite to the start of a next commutator run. Item 27 explained the control by the all-entry delay signal AED of the restoration of **19W** to cut off **18***a* as a second prerequisite to the start of the next commutator run. The third prerequisite is met by the STRD1 signal produced under control of the STR pilot signal, acting through the commutator to produce the commutator signal STR which in turn acts through the S transmission delay circuit (Fig. 75*c* and Item 12). Prior to start of the next commutator run, *b* and *b1* signals will be produced under control of signal STRD1, in preparation for the scanning of the B side of sequence storage. These signals perform the same function for the B

sides of the pilot units selection trees and the Operational sign In Code and OP1 sequence circuits (Figs. 54 to 63) as the *"a"* and the *a1* signals performed for the A sides (see Items 15*a*, 15*b* and 16). The STRD1 signal, through **22** and **22***a* in Fig. 78*i*, reverses **23W**, which applies a positive pulse to **14W**. If **14W** is conditioned by **18—18***a* the pulse applied to it by **23W** will make it conduct to turn **15W**. As stated before, **18—18***a* is cut off when the first two mentioned conditions for a new commutator run have been met. The third condition is the reversal of **23W** by the STRD1 signal. When all three conditions have been met, **14W** conducts to turn **15W**. The next AP pulse restores **15W** which turns **17W** and **19W** to prepare them, respectively, to sense completion of the next scanning sequence and next AED signal. The return of **15W** also resets **23W** to prepare it to sense the next STRD1 signal. Also, the return of **15W** this time restores **25W** (compare with Item 14). As **25** is now restored, it makes **26** conductive so that **26—26***a* is released and the *"a"* signal is discontinued (note Item 14). In the manner explained in the latter item, **16W** is turned upon the rstoration of **15W**, and is itself restored by the next AP pulse. Upon its restoration, **16W** returns **28W** which was turned by the previous pulse from **16W** (see Item 14). Now, with **25W** and **28W** both restored, the couple **27—27***a* is cut off and through **32** produces the negative *b* signal.

When **16W** restored, it again turned **13X** (Fig. 78*j*) which thereupon produces the second SCM signal (also see Item 16). This may be taken as the second start commutator run signal. This signal, for one thing, is inverted by **25Z** (Fig. 78*k*) to a negative impulse which this time restores **22Z** (compare Item 16). Restored **22Z** cuts off **23***a*. The trigger **26Z** was turned before by the FR signal produced at the end of the scanning step of the R spot (see Item 26–1). With **26Z** turned, it cuts off **23**. As couple **23—23***a* is now being cut off, the couple acts via **24Z** to produce the *b1* signal.

It should be noted that the triggers **25W** and **28W** are alternated in status each time **14W** is rendered conductive by the fulfillment of all three conditions for a new commutator run, so that the *"a"* and *b* signals are produced alternately for successive runs. Likewise, the triggers **22Z** and **26Z** are alternated in status by the signals SCM and FR, so that signals *a1* and *b1* are produced alternately for successive scannings by the spots P, Q and R.

The SCM signal also goes to the P spot (Fig. 78*c*) and starts the operation of the Ink delay circuit (see also Item 16).

The STRD1 negative signal also acts through **11***a* and **11** in the Z spot (Fig. 78*k*) to reverse **10Z** (see Item 35). With **10Z** reversed, it deconditions **13** to stop the STR commutator signal, as in Item 15*a*. Further, upon reversal of **10Z**, it again turns **9Z** which was restored by the SE pilot signal (Item 29).

The STRD1 positive pulse also acts through **23–4CF** (Fig. 75*d*) to reset **22** in **4CF**, which was turned before (Item 13) in order to pick up relays AIR. These relays were dropped later when **28–4CF** was turned under control of the first STRD2 pulse (see Item 19). With **22–4CF** now turned and **28–4CF** in turned state, couple **21—21***a* is cut off and through **26** and **3** produces increased potential on the wire *bir*. This causes tubes **9** and **13** to **18** in Fig. 77*d* to conduct and apply reduced potential to line *birr*. Consequently, relays BIR (Fig. 36) are energized and the energized relays BI (Item 31) are dropped. Some 15 ms. later the new STRD2 pulse, acting through **23***a*–**4CF** (Fig. 75*d*) restores **28**, causing relays BIR to be dropped.

Reference has been made to the fact that the *b* and *b1* signals serve the same functions with respect to the B sides of the operational sign and the In code permutation circuits and to the B sides of the pilot units selection trees as the *"a"* and *a1* signals perform with respect to the A sides of these various circuits. Briefly, the negative *b* signal is amplified by **30** and **36** in Fig. 76*a* and the resulting positive *b* signal renders tubes **4, 5, 6, 10, 11, 12, 18, 22, 23, 24, 29** and **30** in Fig. 76*c* conductive. Accordingly, the B sides of the P, Q, R, and U branches of the Operational Sign permutation circuits and of the Q, R, U, V branches of the In code permutation circuits (see Figs. 60 and 61) are heated. The positive *b* signal in Fig. 76*c* is also applied to **36** and the resulting negative *b* signal inverted and amplified by **34** and **35**, which produce a positive *b* signal. With respect to the T branches of these permutation circuits they are not heated directly under control of the *b* signal but are heated under control of this signal in accordance with whether the OP2 field characterizes the T field as an In or an Out field. As already understood, the T field is an "Out" field except when the OP2 number is 01. Fig. 76*e* diagrammatically indicates the P, Q, R, U and V zero filters, the OP2 trees and the T zero filter relating to the B sides of the Operational Sign, In Code, and pilot units selection trees. The arrangement of these filters and trees for the B side is similar to that explained in Items 15*b* and *c* with respect to the A side. Briefly, if the OP2 field bears any number other than 01, then line TOB is at high potential and conditions a tube **20** in Fig. 76*e*. This tube will be rendered conductive by the *b* signal coming from **34** and **35** in Fig. 76*c* and thereupon will cut off a tube **32**. The output of this tube is designated T "out" B and goes to the grids of tubes **16** and **17** in Fig. 76*c*. These two tubes thereupon become conductive and heat the **1T** and **2T** branches of the Operational Sign permutation circuits on the B side. If the OP2 number is 01, then line TIB is at high potential and conditions a tube **19–76***e*. The *b* signal renders this tube conductive, cutting off **31** to apply increased potential to output line T "in" B, as a result of which **29** in Fig. 76*c* becomes conductive and heats the T branch of the In Code permutation circuit on the B side.

With regard to the heating of the B sides of the pilot units selection trees, the positive *b* signal coming from **34** and **35** in Fig. 76*c* is applied via an inverter **5–76***f* and amplifier and inverter **11** and **12** to tubes **13, 17, 18, 19, 21, 22, 24, 27** and **28** in Fig. 76*f*. These tubes are rendered conductive and heat the B sides of the P, Q, R, and U branches of the OC–ES to Int trees (Fig. 57) and of the Q, R, U, and V branches of the IC-Int to ES trees (Fig. 58). With regard to the T branches of these trees, their B sides are heated in accordance with whether the T field is an In or an Out field. As previously stated, if the T field is an Out field, then the line T "out" B is at high potential but if the T field is an In field then the line T "in" B is at high potential. If the former line is at high potential, then it renders **23**, Fig. 76*f*, conductive thereby heating the T branch of the OC–ES to Int trees. If

the line T "in" B is at high potential, it renders 28 in Fig. 76f conductive, thus heating the T branch of the IC-Int to ES trees. With regard to the B sides of the IC–ES to In, the IC Presense and the OC-Out to ES trees, they are heated under control of the b signal in accordance with the conditions of the various zero filters and the OP2 trees in the same manner as described for the A sides. Briefly, if the P field is not blank, then the line PZF (Fig. 76e) is at high potential and conditioning 29. Similarly, if the fields Q, R, U and V are not blank, then the lines QZF, RZF, UZF and VZF are at high potential, conditioning 28, 27, 26 and 25. If the T field is not blank, and the OP2 field bears any other code number except 01, then the line TOZF is at high potential and conditioning 27. On the other hand, if the OP2 field bears the code number 01 and the T field is not blank, then the line TIZF is at high potential, conditioning 24. The positive b signal coming into Fig. 76e renders the conditioned tubes conductive. Assuming that the tubes 24, 22, 25, 26, 27, 28 and 29 have been conditioned and rendered conductive, their reduced outputs are inverted by 33 and 34 in Fig. 76e and by tubes 1, 2, 3, 4 and 5 in Fig. 76f. The resulting increased potential outputs of these tubes are applied to 33, 34, 15, 31, 36, 14, 32, 35, 7, 25, 30, 8, 26, 29, and 9 in Fig. 76f. These mentioned tubes become conductive and heat the B sides of the OC-Out to ES circuits, the IC Presense circuits and the IC–ES to In circuits.

The negative bf signal coming from the main commutator is applied to 3 and 9 in Fig. 76a and the resulting positive bf signal renders conductive the tubes 11 to 18 and 20, 21, and 23 in Fig. 76b thereby heating the B sides of the Q, R and SH1 shift code combinational circuits shown in Figs. 62 and 63 and also heating the B side of the OP1 pyramid shown in Fig. 59.

SUMMARY

To start with, the A side of sequence storage was open (Item 1), and the relays AOR and X7 were energized (Items 2 and 3). The artificial line of sequence was then entered under manual control (Item 4) into the open A side of sequence storage. After this was done, the start key switch SKS (Fig. 77aa) was closed to cause the first commutator signal STR to be produced and as a result the relays AOR (Item 2) and gate relay AM of the A side of sequence storage were deenergized (Item 5). With relays AOR deenergized, the stick circuits of the selected AOP relays were closed. At the same time the STR signal caused the gate relay BM of the B side of sequence storage to be energized, thereby opening the B side of sequence storage (Item 6). The STR signal also caused the relays X1 to be energized (Item 7) as a result of which the S1, S2 pyramids (Fig. 50) were heated so as to apply the next line of sequence data from S1, S2 selected sources to selected Out bus-sets 7 and 8 (Item 8). Along with the application of the sequence data to the Out buses, forward signals were applied to their buses 81. Also, the S1, S2 pyramids, in the assumed example, selected and caused energization of the Move relays associated with the tape storage banks containing the selected tape storage stations from which the sequence data were taken in the assumed example. The STR signal also caused relays X2 and XM to be energized (Item 9) so as to close timing contacts in the A sides of the Out sequence permutation circuits shown in Figs. 47a to 47d, 48 and 49a and 49b. The signal STR also was effective to initiate operation of a "Late" delay circuit (Fig. 75f) which in conjunction with an increased potential applied to wire x2w, resulting also from the STR signal, caused the relays X3, X4, X5 and X6 to be energized (Items 10 and 11). With the relays X2, XM and X3 to X6 energized, all the Out sequence permutation circuits are heated on the A side. According to program data present in the P, Q, R, T (if Out), and U fields, the Unit Outs, Group Outs, Move relays and Table Outs are selectively operated, in the manner described in Section 11. However, the artificial line of sequence bears zero data except in the S1, S2 fields so that the only result of the heating of the various trees and pyramids shown in Figs. 47a to 50 is the application of the new line of sequence data from the S1, S2 selected sources to the Out bus-sets 7 and 8.

The STR signal acted upon the S transmission delay counter in Figs. 75c to cause the 10 ms. delayed signals STRD1 to be produced (Item 12). Under control of these signals, the A intermediate reset relays AIR were energized (Item 13), breaking the pick-up circuits of relays AOP which are now held by their stick circuits. The STR signal was then terminated under control of the signal STRD1 and also the "a" signal was produced (Item 14). Under control of the "a" signal, the A sides of the Operational Sign and the In Code permutation circuits (Figs. 60 and 61) were heated (Item 15b), and also the A sides of the OC–ES to Int and IC-Int to ES pilot units selection trees (Figs. 57 and 58) were heated (Item 15a), the heating of the T branches being further dependent on the OP2 trees. The "a" signal also may function to heat the other three groups of pilot units selection trees (Figs. 54 to 56) selectively according to the zero filter conditions and the OP2 conditions (Item 15b). In the present situation only the heating of the A sides of the OC–ES to Int trees has any effect on the scanning operation of the commutator.

The STRD1 signal also was effective through the same means which produced the "a" signal and through a trigger 13X (Fig. 78j) to cause the signal SCM to be produced (Item 16). This signal controlled the production of the a1 signal which caused the heating of the A sides of the Q, R, and SH1 shift code circuits (Figs. 62 and 63) and of the A side of the OP1 pyramid (Fig. 59).

The OP1 pyramid, being set at 00, caused the No OP signal to be produced (Item 17). After a short delay sufficient to allow the OP1 pyramid to perform its function, the SCM signal caused the Ink signal to be produced. The Ink signal combined with the No OP signal to condition the commutator NO.

Two AP pulse cycles after the SCM signal was produced, the signals OCO, PS, SPR and NPR were produced (Item 21).

15 ms. after the production of the STRD1 signals, the STRD2 signal was produced (Item 18) causing the relays AIR to be deneergized (Item 19).

As described in Item 20, the dial switches DS1S and DS2S were preliminarily adjusted to cause certain ground signals to be applied to pilot units 7 and 8. These are the OCO7 and 8, the PRES7 and 8, and the ICIS7 and 8 ground signals. Upon the production of the commutator signal OCO (Item 21), it acted in conjunction with the OCO7 and 8 signals to cause the pilot units 7 and 8 to produce their re-

spective signals OCS (Item 22). One effect of the OCS signals is to block the production of SE and AE return signals and prepare for their subsequent emission. The OCS signals, in pilot units 7 and 8, also provide one condition for the production of the cancel signals and entry signals for electronic storage units ES7 and ES8. Another condition of the production of these signals was the receipt of Forward signals by pilot units 7 and 8 (see Item 24*a*). Under control of the Forward signals (acting through Forward Signal Delay Counters) and the signals OCS, the pilot units 7 and 8 produced the cancel signals ESC and the entry signals Out to ES (Item 24*b*). As a result, the first real line of sequence data was brought from the selected tape stations into the electronic storage units 7 and 8. Move signals SMS were produced, after termination of the entry signals, for causing the selected tape stations to step to their next designation lines.

The signals PRE produced in pilot units 7 and 8 by the mixing of the signals PRES7 and 8 with the signal SPR (Item 23) were stored by triggers 30 and 29 in 3CP (Fig. 80*c*), as a condition to the production subsequently of the transmission signals ES to In. With 30 turned, the AT and STR pilot signals were blocked. Also, turned 30 conditioned 17 to prepare for subsequent initiation of the operation of the TR transmission delay counter (Fig. 80*d*).

Substantially at the same time as the Move signals were terminated, the pilot units 7 and 8 became effective to produce the SE and AE return signals (Item 25). The signal SE manifests completion of the entry of sequence data into electronic storage while the signal AE manifests the completion of entry of all data into electronic storage.

At the time that the signal OCO initated events leading to entry of data into electronic storage, the signal PS (Item 21) initiated the scanning sequence of the commutator spots P, Q, R . . . V (Items 26*a* to 26V). The PS signal acted upon the P spot of the commutator to cause a signal P1 to be produced and to prepare for the production of a P.OC signal (Item 26P). The P1 signal combined with a P*b*O (OC) signal in the blank code chassis BC in Fig. 78L to produce the PIL.OC signal as a result of which the P.OC signal was emitted and caused an OP.OC signal to be applied to the calculation control commutators and the NO commutator. Since the NO commutator was the only one which was conditioned for response to the OP.OC signal (Item 17), this commutator returned an OP.BS signal which terminated the P spot operation and initiated the Q spot operation. In a similar manner the Q and the R spots successively operated (Items 26Q and R). At the end of the R spot operation, a finish R signal FR was produced and this signal caused the *a*1 signal to terminate and the *a*2 signal to be produced (Item 26–1). The FR signal also restarted the Ink delay, at the end of which the timing signal Ink again was produced. The *a*2 signal controlled the heating of the A sides of the U and V shift code circuits and of the OP2 pyramid. As this pyramid was also set at 00, the commutator NO again was conditioned under control of a NO OP and Ink signals for the scanning of the second half of the line of sequence by the T, U and V commutator spots. Scanning by these spots is similar to that explained for the P spot. At the termination of the scanning step of the V spot, the *a*2 signal was dropped and the trigger 17*w* is reset so that one condition for start of the next commutator run was established (Item 26–2).

Under control of the AE signal (Item 25) which followed the entry into electronic storage, the signal AED was produced about 16 ms. later and reset 19*w*, so that another condition for the next run of the commutator was established (Item 27). The final third condition for a new commutator run was established (Item 39) under control of an STRD1 signal given about 10 ms. after the STR pilot signal was produced after the transmission of data from electronic storage (Item 33).

The AE signal also acted to cause the relays X2, XM and X3 to X6 to be deenergized (Item 28).

The SE signal (Item 25) served to cause the relays X1 to be deenergized (Item 29).

Another function of the AE signal (Item 25) was to terminate the OCO and PS signals and then cause an SW signal to be produced (Item 31) which signal combined with the ICIS signals (Item 20) to produce the ICI signals. The effect of these ICI signals, in combination with the stored effect of signals PRE (Item 23), was to produce the RDL signals in pilot units 7 and 8 (Item 31). Under control of these signals RDL and ICI, these pilot units produced the transmission signals ES to In for causing the new line of sequence data in electronic storage units 7 and 8 to be transmitted to the then open B side of sequence storage (Item 31). After a transmission delay (Item 32), the transmission signals terminated. The RDL signals also functioned through reset delay counters in pilot units 7 and 8 to allow the AT and STR pilot signals to be produced, this occurring after the transmission from electronic storage had been completed (Item 33). One AP pulse cycle after the SW signal was produced, the ICIC signal was produced and initiated operation of the ICIC delay counter. Some 3 ms. after the transmission from electronic storage started, the ICIC counter caused the relays BOR to be energized (Item 34).

Under control of the STR pilot signal, the STR commutator signal was again produced (Item 35). One effect of the STR signal from the commutator was to cause the relay BM to be deenergized and the relay AM to be energized again. In other words the gate to the B side of sequence storage was closed and the gate to the A side reopened. Further, the STR signal dropped the relays BOR (Item 35).

The STR signal also caused the relays Y1, Y2, YM and Y3 to Y6 to be energized (Item 36). With these relays energized, the B sides of the S1, S2 pyramids and of the Out sequence storage permutation circuits are heated and the program data now in the B side of sequence storage is translated into selective energizations of the relay storage Group and Unit Outs, the tape storage group and unit (station selector relays) Outs, the Move relays, the dial storage Group Outs, and the Table Look-up Group Outs and Table Outs.

The AT pilot signal (Item 33) caused the commutator to produce the AT commutator signal as a result of which relays X7 were deenergized and the relays Y7 energized (Item 37) so that the B sides of the In sequence storage circuits are heated, with the effect of causing selective operation of the relay storage Group

Ins and Unit Ins and table look-up Group Ins and Table Ins, in accordance with the program data presented by the In fields of the line of sequence now stored in the B side.

Another effect of the AT commutator signal is to cause a delayed ATD signal to be produced (Item 38) for restoring 27X in preparation for the production of the next SPR and NPR signals (Item 38).

The STR commutator signal again functioned through the S transmission delay counter (Item 39) to cause the STRD1 pulse and the STRD2 pulse to be produced. Under control of the STRD1 pulses, the relays BIR were energized (Item 39); the "a" signal terminated, the b signal produced, and the final, third condition for the start of a new commutator run, as manifested by production of a signal SCM was satisfied. This signal SCM, in conjunction with the previous FR signal (Item 26–1) caused the b1 signal to be produced. The signal SCM also started the operation of the Ink delay circuit in the P spot (Fig. 78c).

The b and b1 signals control the heating of the B sides of the Operational Sign and the In code permutation circuits (Figs. 60 and 61), of the pilot units selection trees (Figs. 54 to 58), of the Q, R and SH1 shift code combinational circuits (Figs. 62 and 63), and of the OP1 pyramid (Fig. 59).

17. *A sequence run for accumulation*

Assume that the first real line of sequence data selected by the S1 and S2 numbers in the A side of sequence storage and entered into the B side of sequence storage, during the first sequence run (Section 16b), consists of the following:

S1Seq

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	Op1	S1
2	1	010	2	2	011	4	1	030	0	02	16

S2Seq

Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	Op2	S2
1	3	433	2	6	552	4	5	151	6	04	02

The significance of the code numbers is clear from Sections 2a, 7 and 11 and also will be brought out in the following portions of the present section.

P always is an Out field, and the code numbers in this field call for an amount to be read out of relay storage unit 010 (Pr) to Out bus-set 1 (Pb) and for the amount to be handled without a change in sign, since code number 2 (Ps) designates the + operational sign (see Section 2a).

The Q field is characterized as an Out field by number 2 in Qs and this number also indicates that the amount to be read out of relay storage unit 011 (Qr) to Out bus-set 2 (Qb) is to be handled without a change in sign.

The R field is characterized, by 4 in its s subfield, as an In field. Further, this number in Rs calls for a shift, if any, to the right of less than 10 columns. Code number 030 in Rr represents relay storage unit 030. In entirety, therefore, the R field calls for a result to be entered in relay storage unit 030 from In bus-set 1 (Rb) with a denominational shift of less than 10 columns to the right to be effected by the denominational shift unit (Section 12).

The code number 0 in SH1 signifies that the units place digit of the denominational shift amount is zero. Since the code number 4 in Rs indicates zero in the tens place of the denominational shift amount, it is clear that the denominational shift is to be zero.

Code number 02 in field OP1 calls for accumulation without half correction.

In brief, the instructions given by the above fields P, Q, R, SH1, and OP1 are to send terms from relay storage units 010 and 011 via electronic storage units 1 and 2, respectively, to the accumulator to be accumulated without change in sign of the terms and without half correction, and for the algebraic sum to be routed through the denominational shift unit without column shifting and thence via electronic storage unit 1 to relay storage unit 030.

The code number 16 in S1, along with plugging such as explained in Section 11, selects the source of the next S1Seq data.

Field T is classed by 04 in OP2 as an Out field, as it would be by any other number but 01 in OP2. The fact that T is an Out field means that digit 3 in Tb will select the Out bus-set 3 to receive an amount from the source selected by Tr. Number 433 in Tr calls for the amount to be read out from the tape at station 1 in tape storage bank 2 via the A outlet of this station, and for the tape to remain at rest after the number has been read out. Designation 1 in Ts represents the — operational sign which signifies that the number is to be handled with a change in sign.

Feld U is classed by 2 in Us as an Out field which means that 6 in Ub will select Out bus-set 6 to receive a number. Number 2 in Us further signifies that the number is to be handled without a change in sign. Number 552 in Ur calls for the number to be read out of the tape at station 10 in bank 2 via the B outlet of this station, and for the tape to be moved after the number has been read out.

Field V is classified by 4 in Vs as an In field and this number in Vs also indicates that column shift, if any, of the result is to be to the right and of less than 10 columns in extent. Digit 5 in Vb calls for a number to be applied to In bus-set 5 via electronic storage unit 5. Code number 151 in Vr represents relay storage unit 151, which is the 15th such unit in set 1.

Code number 6 in SH2 designates the units digit of the denominational shift amount. This, together with the fact that Vs bears digit 4, means that the denominational shift is to be 6 columns to the right.

Code number 04 in OP2 instructs the machine to perform accumulation with half correction of the result.

In short, the instructions given by fields T, U, V, SH2 and OP2 are that numbers from stations 1 and 10 of bank 2 be applied via their A and B outlets to Out bus-sets 3 and 6, respectively, to be routed through electronic storage units 3 and 6 to the accumulator, that the tape at station 10, bank 2 be advanced after the number has been read out of the tape, that the sign of the term taken from station 1, bank 2 be changed, that the sum be shifted by the denominational shift unit 6 places to the right, that the half correction entry of 5 be made in the 5th order of the sum before the denominational shift is completed and that the rounded off result be routed via electronic storage unit 5 to relay storage unit 151.

Code number 02 in S2 together with the plugging given in Section 16b, Item 8, selects the tape at station 10, bank 1 as the source for the next S2Seq data and calls for this tape to be line-spaced after the data has been read out of the tape.

Reference to the summary given at the end of Section 16*b* shows that after the transmission of sequence data from electronic storage to the B side of sequence storage, the STR pilot signal was produced and caused the A side of sequence storage to be reopened (Item 35, Section 16*b*), and the relays YM and Y1 to Y6 to be energized (Item 36, Section 16*b*). The STR signal was followed by the 10 ms. delayed signal STRD1 which was effective, when the scanning sequence had been completed and the all entry delay signal AED had been given, to initiate operations leading to the production of the *b* signal, a new SCM signal, the *b1* signal, and new OCO and PS signals.

At the end of all data transmission from electronic storage, the AT signal (Item 33, Section 16*b*) was produced and caused the relay Y7 to be energized (Item 37, Section 16*b*). The signal AT also was followed about 16 ms. later by the ATD signal which caused the restoration of 27X (Fig. 78*j*) so as to allow the new SPR and NPR signals (Item 38, Section 16*b*) to be produced provided three other precedent conditions have been met, these three conditions being the same as required for the new OCO and PS signals.

As the relays YM and Y1 to Y7 are energized, the S1, S2 pyramids, the Out and the In sequence storage circuits (see Figs. 47*a* to 52*b*) are all heated on the B sides. The *b* signal causes the heating of the B sides of the Operational Sign and the In Code sequence storage circuits (Figs. 60 and 61), and of the pilot units selection trees (Figs. 54 to 58); the *b1* signal causes the heating of the B sides of the Q, R and SH1 shift code sequence storage circuits (Figs. 62 and 63) and the heating of the B side of the OP1 pyramid (Fig. 59), all as described in detail in Item 39, Section 16*b*.

1. The heating of the B side of the relay storage Group Out pyramids (Figs. 47*a* and 49*a*) causes the P pyramid set at 010 in the subfield *r* and at 1 in the subfield *b*, to pick up the relays ORS–GO1 of relay storage Group Out 1 associated with the "0" set of relay storage units (see Section 7 and Fig. 28). The heating of the B side of the relay storage Unit Out pyramids (Fig. 48) causes the P pyramid to pick up the relays U "out" 010; i. e., the relays in relay storage Unit Out 010 which is the outlet for station 010 in the "0" set of relay storage. With the Unit Out 010 and Group Out 1 of relay storage set "0" operated, the data in relay storage unit 010 is applied along with a Forward signal to Out bus-set 1, in the manner described in Section 7.

2. The heating of the B sides of the Q branches of the relay storage Group Out pyramids and Unit Out pyramids causes these branches set at 2 in Q*s*, at 2 in Q*b* and at 011 in Q*r* to pick up relay storage Group Out 2 of relay storage set 1 and Unit Out 011 which is in this relay storage set. The amount in this relay storage unit is therefore impressed, along with a Forward signal, on Out bus-set 2.

3. The heating of the B side of the tape storage Group Out pyramids (Figs. 47*b* and 49*b*) causes the T branch set at 3 in T*b* and at 433 in T*r* to pick up tape storage Group Out 3 of tape storage bank 2 (see Section 11). The heating of the B side of the station selector pyramids (Fig. 47*d*) causes the T branch set at 433 in T*r* to pick up station selector relays 1ASS of bank 2. Accordingly, the data designated on the line, at sensing position, of the tape at station 1 of bank 2 is applied along with a Forward signal to Out bus-set 3. The heating of the B side of the station move pyramids (Fig. 47*c*) does not establish a circuit through the T branch because the T*r* sequence storage relay *r*100 is not energized inasmuch as the code number in T*r* is 433, and hence the T*r*100*e* contacts are open. This prevents a circuit from being established through the T branch of the station move pyramids. Accordingly, the relay MA of bank 2 of tape storage is not energized.

4. The heating of the B side of the tape storage Group Out pyramids (Figs. 47*b* and 49*b*) causes the U branch set at 2 in U*s*, at 6 in U*b* and at 552 in U*r*, to pick up the tape storage Group Out 6 associated with bank 2. The heating of the B side of the station selector pyramids (Fig. 47*d*) causes the U branch to pick up the station selector relays 10BSS of bank 2. Accordingly, the data designated on the line, at sensing position, of the tape at station 10 in bank 2 is impressed along with a Forward signal upon Out bus-set 6. The heating of the B side of the station move pyramids (Fig. 47*c*) causes the U pyramid to establish a circuit path through the station move relay MB of bank 2.

5. The heating of the B sides of the relay storage Group and Unit In sequence storage circuits (Figs. 51 and 52*a*) causes the R pyramids set at 4 in R*s*, at 1 in R*b* and at 030 in R*r* to pick up relay storage Group In 1 and relay storage Unit in 030 of relay storage set 0. Accordingly, relay storage Unit 030 is conditioned to receive a result from In bus-set 1 and a reset signal from bus 82 of In bus-set 1. Also, a back signal is sent from the +150 v. line (Fig. 29) via the shifted points *bs* of the operated Unit In 030 and the points *bs* of the operated Group In 1 of storage set 0 to bus 81 of In bus-set 1.

6. The heating of the B sides of the relay storage Group In and Unit In pyramids causes the V pyramids set at 4 in V*s*, at 5 in V*b* and at 151 in V*r* to pick up Group In 5 and Unit In 151 of relay storage set 1. Accordingly, relay storage Unit 151 is conditioned to receive a result from In bus-set 5 along with a reset signal from bus 82 of this In bus-set. Further, a back signal is applied via contacts *bs* of Unit In 151 and via contacts *bs* of Group In 5 of relay storage set 1 to bus 81 of In bus-set 5.

7. The heating of the B sides of the S1, S2 pyramids (Fig. 50) causes the S1 pyramid set at 16 to apply ground to socket SUP16, SGP16 and SMP16; and causes the S2 pyramid set at 02 to apply ground to sockets SUP02, SGP02 and SMP02. The plugging of the latter three sockets has been explained in Item 8, Section 16*b*. Accordingly, the code number 02 in S2 and the illustrative plugging causes selection of the next S2Seq data from station 10 of bank 1, to be applied through its B station selector to Out bus-set 8, along with a Forward signal. Further, the move relay MB of bank 1 is energized.

Assume the S1 code number 16 is to select relay storage unit 014 as the source for the next S1Seq data to be piloted through electronic storage unit 7. For this, the plugging is from socket SUP16 (Fig. 53*a*) to socket RSUP014 and from socket SGP16 (Fig. 53*b*) to socket RSGP7–4. Consequently, Group Out 7 and Unit Out 014 of relay storage set 4 are actuated, and the data in relay storage unit 014 are impressed along with a Forward signal on Out bus-set 7. The socket SMP16 is not plugged inasmuch as a Move signal is not required for relay storage.

8. The heating at *b* signal time of the B side of the operational sign sequence storage circuits (Fig. 60) causes reduced potential to be applied via contacts Ps2*e* to output wire 2P. Similarly, reduced potential is applied to output line 2Q via contacts Qs3*e*, Qs4*e* and Qs2*e*. Also, reduced potential is applied to line 1T via contacts Ts1*e* and reduced potential is applied to line 2U via contacts Us3*e*, Us4*e* and Us2*e*. The output lines 2P, 2Q, 1T and 2U are connected to the grids of tubes 3, 7, 13 and 16 in the OPSN section of Fig. 78L. Accordingly, these tubes are now cut off.

9. The heating at *b* signal time of the B side of the In code sequence storage circuits (Fig. 61) causes reduced potential to be applied via the B side contacts Rs4*f* to output wire RIC. Also, reduced potential is applied via the B side contacts Vs4*f* to output wire VIC. The low potentials on the output lines RIC and VIC are applied to tubes 17 and 29, respectively, in Fig. 78*b*, cutting off these tubes.

10. The heating at *b* signal time of the B sides of the pilot units selection trees in Figs. 54 to 58 results in signals being produced as follows:

(*a*) OCO1: Via the B side tree P*b* (Fig. 54) set at 1.

(*b*) OCO2: Via the normally closed B side contacts Qs8*g* (Fig. 54) and Qs4*g*, and the tree Q*b* set at 2.

(*c*) OCO3: Via the B side tree T*b* (Fig. 54) set at 3.

(*d*) OCO6: Via the normally closed B side contacts Us8*g* (Fig. 54) and Us4*g*, and the U*b* tree set at 6.

(*e*) PRES1: Via the now closed B side contacts Rs4*i* (Fig. 55), of the tree R*b* set at 1.

(*f*) PRES5: Via the now closed contacts Vs4*i* (Fig. 55), and the tree V*b* set at 5.

(*g*) ICR1: Via the now closed B side contacts Rs4*j* (Fig. 56) and the R*b* tree set at 1.

(*h*) ICV5: Via the now closed B side contacts Vs4*j* (Fig. 56) and the tree V*b* set at 5.

(*i*) P*b*1: Via the P*b* tree, on the B side, (Fig. 57), set at 1.

(*j*) Q*b*2: Via the normally closed B side contacts Qs8*h* (Fig. 57) and Qs4*h*, and Q*b* tree set at 2.

(*k*) T*b*3: Via the B side tree T*b* (Fig. 57) set at 3.

(*l*) U*b*6: Via the normally closed B side contacts Us8*h* (Fig. 57) and Us4*h* and the tree U*b* set at 6.

(*m*) IRC1: Via the now-closed B side contacts Rs4*k* (Fig. 58), and the R*b* tree set at 1.

(*n*) IVC5: Via the now-closed B side contacts Vs4*k* (Fig. 58) and the V*b* tree set at 5.

11. The *b*1 signal has caused the heating of the B sides of the SH1, Q, and R shift code sequence storage circuits (Figs. 62 and 63) as previously explained. The code number 1, 2, 4, or 8 in SH1 would result in the energization of the B side relay 1SH1, 2SH1, 4SH1 or 8SH1 and the closure of their respective contacts *a*, so as to apply reduced potential to the lines 1SH, 2SH, 4SH and 8SH, respectively, in Fig. 62. Reduced potential on the lines 1SH, 2SH, 4SH or 8SH would cut off the tube 27M (Fig. 78*a*), 21, 22, or 17, respectively, causing increased potential to appear on the output line MN1, 2, 4, or 8 (also see Section 12 and Fig. 27*a*). In the present example, the field SH1 is blank; therefore none of the lines 1SH, 2SH, 4SH and 8SH in Fig. 62 is reduced in potential, and none of the lines MN1, 2, 4, and 8 is increased in potential.

Since the code number in the B side of the Rs subfield is 4, the B side relays Rs4 are energized. Hence, upon the heating of the B side of the R shift code sequence storage circuits (Fig. 63) cut-off potential is applied from the B side heating terminal LRSHR via the contacts Rs4*m* and Rs1*m*, as is, the output line RTSH. In the present example, the contacts Rs2*n* are not closed and therefore the heating potential on terminal 10SHR on the B side, will not be transmitted to the output line 10SH. Also, since the contacts Rs8*o* are also open, the heating potential from the terminal 20SHR, on the B side, will not be applied to the output line 20SH. It should be noted further that if the contacts RS1*m* were shifted, which is the case when there is an odd digit in subfield Rs, then the circuit to the output line RTSH would be open and instead the circuit to the output line LTSH would be closed. Referring to Fig. 78*a*, if reduced potential were present on line 10SH, then tube 18 would be cut off and increased potential would appear on the minuend line MN10. Likewise, if reduced potential were present on the line 20SH, the tube 19 would be cut off and the line MN20 would be at increased potential. In the present example neither of the lines 10SH and 20SH is at reduced potential and accordingly the lines MN10 and 20 remain at reduced potential. In short, the denominational shift called for by the S1*seq* line being 0, none of the minuend lines MN is at increased potential. The line RTSH is at reduced potential and cutting off 25 so that the output line RT in Fig. 78*a* is at increased potential. The increased potential on line RT conditions the tube 17 in Fig. 27*c* so that upon the subsequent application of the Ink signal to the tube the trigger 21 will be placed in its right-shift condition. This would cause the denominational shift, if any had been called for, to take place to the right, as explained in Section 12.

12. The signal SCM was produced upon the turning of 13X (Fig. 78*j*) following the meeting of three conditions arising from the previous commutator run. These three conditions are the completion of the scanning sequence, the production of the signal STRD1 and the production of the signal AED. The signal SCM restored 22Z (Fig. 78*k*) so as to cause the *b*1 signal to be produced for heating the B sides of the SH1, Q and R shift code circuits (Figs. 62 and 63) and the B side of the OP1 pyramid (Fig. 59). As only the turning time of trigger 22Z elapses between the signal SCM and the signal *b*1, these two signals may be considered as substantially simultaneous.

The SCM signal, which is positive in character, is effective to render 1*a* in the P spot (Fig. 78*c*) conductive, causing it to produce a negative pulse which is applied by way of the anode resistor of 1 to the first trigger 5 in the Ink delay circuit. Upon 5P turning, it is reset by next AP pulse and acts through 8 to cause the positive signal ACCL to be produced. This signal is applied to 5-ACC.C (Fig. 78A) so as to cause 6, if it had been turned to be reset. As will be brought out in Item 14*c*, 6 will have been turned if the commutator ACC.C had been conditioned in the preceding sequence run. As understood, the calculation control commutators are selectively conditioned in the first half of a sequence run according to the code number in field OP1 and are conditioned in the second half of a sequence run according to the code number in field OP2. At the beginning of the first half of a run, the signal SCM causes the trigger 5P to turn.

At the end of this first half of a sequence run, the signal FR acts similarly to the signal SCM to turn 5P. Hence, if the accumulator commutator ACC.C has been conditioned during the second half of a previous sequence run, it will be de-conditioned by the signal SCM at the beginning of the next run. If the commutator ACC.C has been conditioned for the first half of a sequence run, it will be de-conditioned under control of the signal FR at the end of the first half of the run. When 5P is turned as described above, it cuts off 3*a*. Unless field T is an In field, the tube 3P also will be cut-off and when 3*a* is cut off, upon the turning of 5, the couple 3—3*a* is effective to make 8 conductive, causing it to produce the negative signal HCR. This signal as previously described in Section 13 resets the half correction suppression storage trigger 5 and the tolerance check storage trigger 22, both in Fig. 71*g*. It is seen that these two triggers are reset at the beginning of a sequence run, under control of the signal SCM. At the end of the first half of a sequence run, the signal FR causes 5P (Fig. 78*c*) to turn and as a result the signal HCR again is produced for resetting triggers 5, Fig. 71*g*, and 22, Fig. 71*g*. Thus, the trigger 5, Fig. 71*g*, is reset at the beginning of each half of a commutator run, in order to prepare this trigger to be selectively turned or left unturned for each half of a sequence run according to whether the codes in fields OP1 and OP2 do or do not call for suppression of half correction to attend an accumulation calculation.

13. The *b*1 signal also heated the B side of the OP1 pyramid (Fig. 59). Since this pyramid is now set at 02, cut off potential is applied to 77*a*, non-conductive causing the tubes 22 and 22*a* to become conductive. The tube 22 then cuts off 30, which causes tube 24 to produce a negative ACC Code signal. This signal is sent to tube 1 in the accumulator control commutator ACC.C (Fig. 78A) and cuts off the tube, which then applies conditioning potential to the suppressor of 2.

The OPO2 signal also causes the tube 22*a*, Fig. 77*a*, to be made conductive, as described above. Tube 22*a* then applies reduced potential to line HCS*w*. Consequently, 30, Fig. 77*b*, is cut off, causing 24 to produce a negative signal HCSS. This signal cuts off 30, Fig. 78*a*. Subsequently (about ½ ms. later) the signal Ink will be produced (see Item 14) and will cut off 30*a*. If 30 has been cut off by the signal HCSS, then the couple 30—30*a* will make 29 conduct so as to produce the negative signal HCS. As described in Section 13 this signal acts through 1 and 1*a* in Fig. 71*g* to turn 5 so as to store a half correction suppression command with respect to the accumulating operation.

14. The signal ECM has initiated the operation of the Ink delay in Fig. 78*c* as pointed out in Item 12. The signal Ink is produced by the Ink delay circuit ½ ms. after the signal SCM. The Ink signal times the following operations:

a. The tubes 17 and 29 in Fig. 78*b* have been cut off as a result of the R and V branches of the In code sequence storage circuits (Fig. 61) being set to represent the In codes in the subfields R*s* and V*s*. This has resulted in the lines RIC and VIC being reduced in potential, at *b* signal time, so as to cut off the tubes 17 and 29 in Fig. 78*b* (see Item 9). The Ink signal which occurs about ½ ms. later cuts off 17*a* and 29*a*. Hence, the couple 17—17*a* acts through 18 to turn 19 causing 20 to produce a positive R "in" signal. Similarly, the couple 29—29*a* acts through 30 to turn 31 which causes 32 to produce the positive V "in" signal. It is seen that the triggers 19 and 31 have been turned to store the fact that the R and V program fields are In fields. These triggers will not be restored until the scanning sequence has been completed as manifested by the signal FC (see Section 16*b*, Item 26—2). The signal FC will then render 26, Fig. 78*b*, conductive causing it to return any of the triggers 15, 19, 23, 27 and 31 which may have been turned to store In conditions of the fields Q, R, T, U and V respectively.

As described above the positive signals R "in" and V "in" were produced upon the occurrence of the signal Ink. The signal R "in" goes to the R spot (Fig. 78*e*) and renders 1 and 1*a* conductive. Upon 1 becoming conductive it turns 5. This conditions the R spot to perform an IC step during which the signals R2 and R3 will be produced at sequential times as will be described. When 1*a* is made conductive it cuts off 18. This prevents 18 from being rendered conductive at the end of an IC step of the preceding spot Q (Fig. 78*d*). If the tube 18 were not de-conditioned under control of the signal R "in," then if the tube 18 should receive a signal QIC from spot Q as would be the case at the termination of an IC step of the Q spot, the tube 18 would be made to conduct and cause trigger 23R to turn. Turned 23 would act through 2 and 30 and 31 to produce the signal R1. This signal is to be produced only if the R spot is conditioned to perform an OC step. When a spot such as the R spot is not conditioned for an IC step and the preceding spot performs an IC step, then the turning of 23R is effected by rendering 18 conductive in the manner described above. If the preceding spot is performing an OC step, then its signal, as Q.OC, turns trigger 21R. This trigger is reset by the next OP.BS signal, causing 22R to turn, which turns 23R.

The signal R "in" also renders 27R (Fig. 78*e*) conductive so as to block the reversal of 23 which otherwise might take place under control of triggers 21 and 22. The reversal of 23 would cause the signal R1 to be produced during the scanning sequence at the end of the step of the Q spot, and this signal is to be suppressed when spot R is conditioned to perform an IC step.

The signal V "in" similarly acts in the V spot (Fig. 78*h*) to condition this spot for an IC step and to block its production of a V1 signal. Briefly, the signal V "in" makes 1 and 1*a* in the V spot conduct. When 1 is made conductive it turns 5 which prepares the V spot to perform an IC step. When 1*a* conducts, it de-conditions 18 so as to block the production of a signal V1 at the termination of an IC step of the U spot if the latter step has been called for. The signal V "in" also renders 27V conductive to block the turning of 23 so as to prevent the production of the signal V1 at the termination of an OC step of the U spot should the latter be called for.

b. The signal Ink renders the tube 5, Fig. 27*b*, non-conductive to produce a positive Ink signal as a result of which the denominational shift amount, if any, manifested by increased potentials on the lines MN in Fig. 27*a*, is entered into the descending counter of the denominational shift unit, in the manner described in Section 12. The positive Ink signal from tube 5, Fig. 27*b*, also renders the conditioned tube 17, Fig. 27*c*

(see Item 11) conductive so as to cause the trigger 21 to be placed in its right-shift status. In the preparation for the first half of the present run, none of the lines MN has been placed at increased potential (see Item 11) and the descending counter in Fig. 27*a*, remains at zero.

c. The negative signal Ink also is applied to tube 1*a* in the commutator ACC.C (Fig. 78A) cutting it off so as to apply increased potential to the control grid of the previously conditioned tube 2 (see Item 13). Accordingly, tube 2 becomes conductive and reverses trigger 6 which may be called the gate of the commutator ACC.C. The trigger 6 in turned state cuts off tubes 4 and 7. Tube 4 conditions tubes 10 and 11. The commutator ACC.C is now conditioned for operation.

d. The Ink signal cuts off 30*a*, Fig. 78*a*. As 30 also has been cut off (Item 13), the signal HCS is produced, causing trigger 5, 71*g*, to turn and store the half correction suppression signal.

15*a*. Trigger 13X (Fig. 78*j*) turned at AP pulse time to cause signal SCM to be produced (Item 12). The next AP pulse resets 13X which causes 9X to turn (see Section 16*b*, Item 21). 9*x* is restored by the following AP pulse and thereupon turns 5X and 17X, which produce the commutator signals OCO and PS.

15*b*. The commutator signal OCO senses the pilot units for their selection by the tree signals OCO. These tree signals cut off selected tubes 12–5CP (Fig. 80*e*) in the pilot units. In the present example, the tree signals OCO1, 2, 3 and 6 have been produced, at *b* signal time (see Item 10), because fields P, Q, T and U are Out fields and their subfields *b* contain digits 1, 2, 3 and 6, respectively. The dial switches DS1S and DS2S are not readjusted and their sections 1 cause signals OCO7 and 8 to be produced (see Section 16*b*, Item 20). The signals OCO1, 2, 3, 6, 7 and 8 cut off the tubes 12–5CP (Fig. 80*e*, for example) in pilot units 1, 2, 3, 6, 7 and 8, respectively. The commutator signal OCO now cuts off all the tubes 12–5CP. Accordingly, couples 12–12*a* in 5CP of pilot units 1, 2, 3, 6, 7, and 8 are effective to cause the signals OCS to be produced by these pilot units. These pilot units also have received Forward signals (see Items 1, 2, 3, 4, and 7). If the delay signal FSD of such pilot unit has been produced prior to the signal OCS, it will have caused 25–2CP (Fig. 80*b*) to turn, and one AP pulse cycle later, the suppressor of 32–2CP will have been conditioned. The signal OCS will then cause 32 to conduct and turn 31 which will be returned by the next AP pulse and thereby will reset 25. If a pilot unit has produced the signal OCS prior to the signal FSD, then the signal OCS will have caused 25–2CP to turn and 32–2CP to be conditioned. The signal FSD will then act to cause 32–2CP to conduct, whereupon 31 will turn. The return of 31 by the next AP pulse will cause 25 to be reset.

When 25–2CP of a pilot unit is in turned status, it acts through 18*a*–1CP (Fig. 80*a*) to turn 21–1CP. With 21–1CP turned, it renders 33*a* conductive to block the all-entry signal AE (Section 16*b*, Item 22). In pilot units 7 and 8, switches 1SQ are in seq positions and, therefore, tubes 33–1CP also are conductive upon the turning of 21–1CP, thus also blocking the sequence-entry signal SE.

Further, turned 21–1CP renders 15*a*–1CP conductive. Normally, 15–1CP also is conductive. With either 15*a* or 15 conductive, tubes 28 and 28*a* are cut off. As long as 28 is cut off, it blocks the positive pilot signal Pil.OC. As long as 28*a* is cut off, it blocks the pilot signal ES to Int which is the signal for timing transmission from the related electronic storage to the Internal Out bus-set (see Section 6). The tube 15–1CP in a pilot unit will be cut off by a signal OC Int produced when this pilot unit receives a "1" signal from the scanning spot corresponding to the Out sequence field which has slected the pilot unit, as will be described in Item 16. When the trigger 21–1CP of this pilot unit is returned, which occurs after entry into electronic storage has been effected (see Section 16*b*, Item 25), the tube 15*a* is cut off. Only then can the cutting off of the companion tube 15 by the signal OC Int be effective to cause the Pil.OC signal and the ES to Int signal to be produced. It is seen, then, that a pilot unit selected by an Out sequence field will be conditioned, under control of a Forward signal received thereby or under control of a signal OCS produced in the pilot unit at the time determined by the commutator signal OCO, to block transmission from the related electronic storage unit to the Internal bus-sets until the entry of data from a source selected by the Out field has been completed into the electronic storage unit.

The above considerations apply, in the present example, to pilot units 1, 2, 3, and 6 selected by Out fields P, Q, T, and U. With respect to pilot units 7 and 8, which are set to pilot sequence data, the signals ES to Int are not needed and are not produced, since the sequence data is transmitted from the electronic storage units 7 and 8 to sequence storage and not to the Internal bus-sets. Hence, in pilot units 7 and 8, the blocking of signals ES to Int and Pil.OC is merely incidental since these signals will not be produced in any event.

When trigger 25–2CP (Fig. 80*b*) in a pilot unit is reset, which occurs after this unit has produced both signals OCS and FSD, it renders 18–1CP (Fig. 80*a*) conductive, causing 14–1CP and 22–1CP to turn. Upon 22 turning, it serves through 16*a* and 4 to produce the cancel signal ESC. When 14 is turned, it cuts off 7, causing 1 to produce the negative entry signal Out to ES. One AP pulse cycle after 22 is turned, it is reset and ends the cancel signal. Upon the return of 22, it turns 27 which is reset by the next AP pulse and thereupon returns 14 to end the entry signal. The return of 27 also causes 13 and 20 to turn. Turned 13 acts through 8 and 2 to produce the negative Move signal SMS. One AP pulse cycle after 20 is turned, it is reset and turns 19. The next AP pulse resets 19, which causes 25 to turn. The next BP pulse resets 25, causing it to return 18 and 21. The return of 13 terminates the Move signal. The return of 21 releases 15*a*—15 for operation by an OC Int signal and also removes the pilot unit from blocking control over the AE return signal. In the case of pilot units 7 and 8, the return of their triggers 21–1CP also removes these pilot units from blocking control over the SE return signal, as well as the AE return signal.

In the above manner, the pilot units 1, 2, 3, 6, 7 and 8 have produced the cancel signals ESC 1, 2, 3, 6, 7 and 8; the entry signals Out to ES 1, 2, 3, 6, 7 and 8; and the Move signals SMS 1, 2, 3, 6, 7 and 8, respectively. Accordingly, the number and sign in relay storage unit 010 are entered in ES1 (Figs. 20 and 22), the number and sign in relay storage unit 011 are entered in ES2, the number and sign read out of a line of the tape

at station 1, bank 2 are entered in ES3, the number and sign read out of a line of the tape at station 10, bank 2 are entered in ES6, the sequence data S1Seq in relay storage unit 014 are entered in ES7, and the sequence data S2Seq are read out of a line of the tape at station 10, bank 1 and entered in ES8. The Move signals SMS1, SMS2 and SMS7 are ineffective in this example because the pilot units 1, 2 and 7 are now piloting data from relay storage units. The Move signal SMS3 is not effective because the move relay MA of bank 2 has not been energized (see Item 3). In order to allow for reading out of station 1 in bank 2 through its A station selector to Out bus-set 3, under instructions of the sequence data, the sockets TS–GOP3 of bank 2 will have been preliminarily plugged to sockets ASSP (see Figs. 32*a*, 34 and Section 9). Further, the Move signal receiving circuit in bank 2 and associated with Out bus-set 3 will have had its socket 82 of the bank 2 set TS–GOP3 plugged to a socket AMS (see Fig. 32*b*). Inasmuch as the relay MA of bank 2 has not been energized (Item 3), the Move signal SMS3 will not be transmitted to any station in bank 2 which has been selected to read out through its A station selector.

Thus, the Move signals SMS1, 2, 3 and 7 will have no effect in the present example. The Move signal SMS6 will be effective because Out bus-set 6 has been selected to receive data via the B station selector of station 10 in bank 2, and relay MB of this bank has been energized (see Item 4). In this case, the sockets TS–GOP6 for bank 2 will have been preliminarily plugged to bank 2 sockets BSSP and socket 82 of TS–GOP6 in bank 2 will have been plugged to a socket BMS. Accordingly, the Move signal receiving circuit, in bank 2, which is associated with Out bus-set 3 will transmit the effect of the Move signal via the now-closed contacts MB*a* (see Fig. 32*b*) and the now-closed contacts 82 of 10BSS, in bank 2, to the station 10 move control circuit in bank 2. Accordingly, station 10 in bank 2 will be stepped to its next line position after the data has been read out of the preceding line and entered into ES6.

Similarly, the Move signal SMS8 will be effective to cause the tape at station 10, bank 1 to be advanced one line space after the S2Seq data designated in its preceding line has been entered in ES8.

15*c*. When the S1Seq and S2Seq data have been entered in ES7 and 8, the negative return signal SE will be produced, in the manner described before. This signal is applied to the Z spot (Fig. 78*k*) which, in response, produces the negative commutator signal SE (also see Section 16*b*, Item 29). The SE signal from the commutator is applied to the control frame, where it is inverted by 5, Fig. 75*a*, and again by 11, Fig. 75*e*, to return trigger 10 (see Section 16*b*, Item 29). As a result, 9*a* is cut off to prepare for subsequent energization of heating relays X1 (Section 16*b*, Item 7) under control of the next STR signal. Returned trigger 10 also renders 15 conductive, causing relays Y1 to be dropped (see Section 16*b*, Item 36).

15*d*. When all the entries into electronic storage have been completed, the negative signal AE is sent by the pilot units to the X spot (Fig. 78*j*) of the main commutator. In the manner described in Section 16*b*, Item 27, the commutator signal AE is produced and sent to the control frame where it initiates operation of the All-Entry delay counter in Fig. 75*b*. The delay signal AED is produced after about 16 ms. The signal AED goes to the W spot (Fig. 78*i*) and acts through 20*a* and 20 to reset 19W. This trigger is turned every time 15W is returned. As explained in Section 16*b*, Item 39, 15W is turned when all three prerequisites to a new commutator run have been satisfied. The next AP pulse resets 15W which causes 19W to turn (also see Section 16*b*, Item 14). The trigger 19W stays turned to render 18*a* conductive until one condition for a new commutator run has been satisfied, this condition being the signalling of completion of all entries into electronic storage, followed by about 16 ms. delay, as manifested by the signal AED. Thus, 19W, which was turned at the beginning of the present run, is now reset since the mentioned one of the three conditions for a new run has now been satisfied.

The AE signal also acts through 23, Fig. 75*e*, to return 22 which was turned by the previous AE signal (see Section 16*b*, Item 28). With 22 in its reset status, it renders 27 conductive, as a result of which heating relays Y2 and YM are dropped (see Section 16*b*, Item 36). The return of 22 also cuts off 21*a* to prepare for subsequent energization of relays X2 and XM under control of the next STR signal.

The positive AE signal on wire 150 in the control frame also is inverted by 30, Fig. 75*f*, to a negative signal which this time resets 24, Fig. 75*f*, 18 and 30 in Fig. 75*g*, and 12 in Fig. 75*h* (see Item 38, Section 16*b*). As a result, the heating relays Y3, Y4, Y5 and Y6 are dropped (compare Item 28, Section 16*b*).

The negative AE pilot signal also acts through tubes 41 and 41*a* in Fig. 80*b* to turn trigger 42, which is returned by the next AP pulse. When 42 is turned, it cuts off 43 to render tubes 19*a*-2CP, of all the pilot units, conductive. As a result, all the triggers 7–2CP are forced back to canceled status. This insures the reconditioning of all the Forward signal receiving circuits (Section 16*b*, Item 24*a*) of the pilot units to non-receptive status prior to the next commutator run.

Finally, the AE signal initiates operation to end the OCO and PS signals and to bring about the transmission of sequence data (see Section 16*b*, Item 31). In brief, the pilot signal AE acts through 10 and 10*a* in Fig. 78*j* to restore 5X, which ends the OCO and PS signals. As 5X restores, it turns 7X, as a result of which the sequence data transmission control signal SW is produced for one AP pulse cycle. The signal SW is mixed in pilot units 7 and 8 with the cut off signals ICIS7 and 8, still acting on tubes 32–5CP (Fig. 80*e*) since dial switches DS1S and DS2S have been left in positions 7 and 8, respectively (see Fig. 56). In the manner described in Section 16*b*, Item 31, the sequence data now in ES7 and ES8 will be transmitted to the now reopened A side of sequence storage (Section 16*b*, Item 35).

16. At the same time that the OCO commutator signal initiated the operations leading to the entries being made into electronic storage of numbers taken from sources selected by the Out code fields and S1 and S2 fields, the PS signal initiated the OC step of the P spot (Fig. 78*c*). In the manner explained in Section 16*b*, Item 26P, the PS signal causes the P spot to produce the P1 signal and also to condition 24P (also see Fig. 79*bb*).

16*a*. The P1 signal is effective to cut off 3*a*-

OPSN (Fig. 78L). Previously the tube 3 has been cut off by tree signal 2P (see Item 8). The P1 signal therefore renders 3—3a effective through 6, 20a, 20 and a power amplifier and inverter 20b to produce the positive operational sign signal OPSN2. Thus, with the subfield Ps bearing code number 2, the operational sign signal OPSN2 is produced during the OC step of the P spot. The OPSN2 signal conditions tube 5, Fig. 71a, which is in the sign mixing circuit of the accumulator as described in Section 13.

16b. The P1 signal is also applied to the tubes 2–5CP of all the pilot units to test the pilot units for selection by branch P of the pilot units selection trees OC–ES to Int (Fig. 57). With subfield Pb containing digit 1, the Pb trees are set at 1, and signal Pb1 has been produced (Item 10). This signal has cut off 2a–5CP of pilot unit 1. Accordingly, the P1 signal upon cutting off 2–5CP of pilot unit 1 renders the couple 2—2a through 1a, 1 and 9 in 5CP, of this pilot unit, effective to produce the negative signal OC Int. This signal cuts off 15–1CP of pilot unit 1. As previously described in Item 15b, the tubes 15a–1CP remain conductive under control of trigger 21 turned during the entry of data into electronic storage and thereby blocks the ES1 to Int signal and the P1l.OC signal. After the entry and upon termination of the Move signal at a B pulse time, trigger 21 is reset in the manner which has been described in Item 25 of Section 16b. When 21 is reset, it returns 15a to cut-off status. Thus, provided that entry into electronic storage unit 1 has been completed, the cutting off of tube 15–1CP under control of the signal OC Int in pilot unit 1 renders the couple 15—15a effective to render 28 and 28a conductive. Tube 28a thereupon serves through 9 and 3 to produce the timing signal ES1 to Int (see Figs. 20, 21 and Section 6). This signal causes electronic storage unit ES1 to apply decreased potentials selectively to the buses of the Internal Out bus-set. In this manner the number in ES1 is applied to the Internal Out bus-set. It should be noted that the algebraic sign of the number is present in column 1 of ES1 and is applied to bus column 1 of the Internal Out bus-set. The digits present in columns 2 to 20 of ES1 are applied to bus columns 11 to 29 of the Internal Out bus-set. The number and its sign in relay storage unit 010 have now been transmitted via ES1 to the Internal Out bus-set.

The decreased potentials on the Internal Out bus-set are inverted by the amplifier of the electronic calculating section (Fig. 20) to increased potentials on the corresponding bus columns of the Internal In bus-set. At this time then the tubes 1, 2, 3 and 4 in each order of register EC of the accumulator section (see Figs. 69a, 69b and 70) and the tubes 5, 6, 7 and 8 in the sign mixing circuit of the accumulator (see Fig. 71a) are all selectively conditioned according to the digits and the algebraic sign taken from electronic storage unit 1 and according to the operational sign derived from Section OPSN (Fig. 78L).

17a. As described in the preceding item, tube 28a–1CP (Fig. 80a) of selected pilot unit 1 was rendered conductive at a B pulse time to cause the signal ES1 to Int to be produced, as a result of which the number and its sign present in ES1 were applied to the Internal bus-sets. At the same time as 28a–1CP was rendered conductive, tube 28 also became conductive, producing a negative signal P1l.OC. This signal is inverted by 39, Fig. 80a, to a positive signal which renders 4W (Fig. 78i) conductive. Accordingly, 3W is turned, just as it was turned under control of the signal P1l.OC from blank pilot unit BC (Fig. 78L) during the first sequenced run. The next BP pulse resets 3W, and as a result a signal P1l.OCC is sent, half an AP pulse cycle after the ES to Int signal, to the tubes 24 of all the scanning spots of the commutator (see Item 16P, Section 16b and Fig. 79bb). Only tube 24P (Fig. 78c) is now conditioned and responds to the P1l.OCC signal so as to produce the signal P.OC which turns 21Q (Fig. 78d). Upon 21Q turning, it causes the signal OP.OC to be produced. This signal goes to all the calculator control commutators ACC.C, MYC, DVC and NO to test them for conditioning according to the OP code number. In the present example, the OP1 code number 02 has selected ACC.C (Fig. 78A) and its trigger 6 has been turned, causing 4 and 7 to be cut off (see Items 13 and 14c). With 4 cut off, it is conditioning tube 10. The OP.OC signal makes this tube conductive, which causes 14, 18 and 22 to turn and 26, if turned during a previous accumulator run of sequence, to be restored. As 14 turns, it turns 15 which acts via 12a to produce the negative cancel signal RCC. Turned 18 acts via 20 to produce the negative cancel signal ECC. Turned 22 serves via 20a to produce the negative accumulator entry signal ACC–RI. In the manner described in section 13, dealing with the accumulator, the cancel signals ECC and RCC reset the registers EC and RC and the carry control triggers K (Figs. 69a, 69b, 70 and 73) and also the sign entry receiving triggers 5, 6, 7, and 8 in Fig. 71a. One AP pulse cycle after triggers 15 and 18 were turned under control of the OP.OC signal, an AP pulse resets these triggers, ending the ECC and RCC cancel signals. As 18 returns, it turns 17. One AP pulse cycle later, an AP pulse resets 17 which restores 22, ending the ACC–RI signal. The latter signal is thus prolonged one AP pulse cycle past the cancel signals and causes the number on the Internal In bus-set to be entered in registers EC and the operational sign and algebraic sign to be entered in the mixing circuit (Fig. 71a) which produces the mixed, operating sign, all as described in Section 13.

It may be noted that the P1l.OCC signal is produced half an AP pulse cycle after the occurrence of the exit signal ES1 to Int. The signals ECC and ACC–RI are produced one AP pulse cycle after the P1l.OCC signal. The ACC–RI signal becomes effective upon the termination of the cancel signal ECC to produce the entry of the number on the Internal bus-sets into the registers EC. It is evident then that the effective entry into registers EC occurs one-and-a-half AP pulse cycles later than the application of the number from electronic storage to the Internal bus-sets. This gives sufficient time for cross-talk to be dissipated, i. e. for transient signals on the entry tubes for the registers EC to die down. In this manner, incorrect entries are avoided.

17b. When 22–ACC.C (Fig. 78A) is restored to terminate the entry signal ACC–RI, it turns 21. The next AP pulse resets 21, causing it to turn 25. Turned 25 renders 29 conductive to produce the negative start signal ACC–ST which goes to 36a (Fig. 71c) of the internal commutator of the accumulator and initiates an accumulator cycle, as explained in Section 13 (also

see Figs. 72 and 73). During the accumulator cycle, the number in registers EC is transferred to registers RC. At the end of the accumulator cycle, the internal commutator of the accumulator produces the "cycle complete signal" CYCPT at AP pulse time (also see Fig. 71*g*). This signal cuts off **28***a*–ACC.C (Fig. 78A). The first effective AP pulse cuts off **28**, causing **28**—**28***a* to act via **29***a* to restore **25**, terminating the ACC–ST start signal. As **25** restores, it turns **26** which causes **27** also to turn. Turned **26** cuts off **24***a* to condition **24**—**24***a* for operation under control of an In code signal OP.IC should this occur next. Trigger **27** is restored by the next AP pulse but, meanwhile, it renders **19** conductive, causing it to cut off **7***a*. Tube **7** is in cut-off condition as long as the commutator ACC.C is conditioned (see Item 14*c*). Accordingly, as **7***a* is now cut off under control of the accumulator cycle complete signal CYCPT, the couple **7**—**7***a* becomes effective through **3** to produce the negative OP.BS signal. This signal, after amplification, goes to the triggers **21** of all the commutator scanning spots to restore the turned one of these triggers. In the instant situation, **21Q** is the one which has been turned (Item 17*a*) and is now restored by the OP.BS signal. In the manner described in Section 16*b*, Item 26P, the return of **21Q** causes the P**1** signal to terminate which is the end of the P.OC step. The return of **21Q** also initiates the Q.OC step (see Fig. 79*bb*).

With the end of the P**1** signal, the OC Int signal (Item 14*b*) and, hence, the ES**1** to Int signal terminate. Accordingly, the tubes Int Ex (Fig. 21) associated with ES**1** return to their cut-off status, so that the number and sign on the Internal bus-sets are removed. Also, with the end of the P**1** signal, the OPSN**2** signal produced under its control (Item 1*a*) terminates.

18. In recapitulation, a number and sign from relay storage unit **010**, selected by subfield P*r* was entered in ES**1**, selected by subfield P*b*. Meanwhile, the P.OC step was initiated and the signal P**1** produced. This signal caused the operational sign **2**, selected by subfield P*s* to be applied to the mixing circuit (Fig. 71*a*) of the accumulator. The signal P**1** also was effective after entry into ES**1** was completed to cause pilot unit **1** to produce the exit signal ES**1** to Int which caused the number and its sign to be read out of ES**1** and applied to the entry tubes of the registers EC of the accumulator. At the next AP pulse time after ES**1** was read out, the signal Pi**1**.OCC was emitted and caused the P spot to produce the P.OC signal which acted through **21Q** to produce the OP.OC signal. This signal operated on conditioned commutator ACC.C to cause it to produce the ECC and RCC cancel signals and the entry signal ACC–RI. Consequently, registers EC and RC were reset, after which the number received by ES**1** from relay storage unit **010** was entered in EC and the sign of the number received by ES**1** from this relay storage unit was mixed with the operational sign to produce the operating sign (see Section 13). Upon termination of the entry signal ACC–RI, the commutator ACC.C sent out an accumulator cycle start signal ACC–ST. An accumulator cycle occurred during which the number was transferred from registers EC to registers RC. At the end of the cycle the accumulator unit returned a complete signal CYCPT to the commutator ACC.C which, in response, produced the OP.BS signal. Under control of this signal, the P.OC step was ended and the Q.OC step was initiated.

In general, after a number from a source selected by an Out field is entered into the electronic storage unit selected by the Out field, the number is read out of the electronic storage unit upon the Internal Out bus-sets and a return signal Pi**1**.OC signal is sent to the main commutator. Under control of this signal, an OP.OC signal is produced to cause the conditioned one of the computation control commutators MYC, DVC, ACC.C and NO to operate. In the case of the commutator NO it sends out an OP.BS Back signal immediately so as to cause the next scanning spot to be placed in action. In the case of the other calculation control commutators, they operate in response to the OP.OC signal to send out cancel and entry signals to the related calculating unit. At the end of the entry signal, the operative control commutator produces a calculation start signal which initiates a calculation cycle. Upon completion of this cycle, a return signal goes to the operative calculation control commutator, causing it to produce an OP.BS Back signal for the main commutator. This signal causes the OC step of one scanning spot to end and the next scanning step to be initiated. The essential distinction between the sequence produced under control of the NO commutator and the other control commutators ACC.C, MYC and DVC is that where the NO commutator is in operation, the scanning steps are successively effected with no pause for calculations whereas when one of the other commutators is in operation, the scanning steps are successively effected with delay in each step dependent upon the calculation being performed.

19. As described in Item 17*b*, the trigger **21Q** (Fig. 78*d*) was restored, at the end of the P.OC step, to initiate the Q.OC step. The return of **21Q** turns **22Q** which is restored by the next AP pulse and thereupon turn **23Q**. As a result, **24Q** is conditioned and the Q**1** signal produced. This signal cuts off **7***a*–OPSN (Fig. 78L). Tube **7** previously was cut off (Item 8) under control of the Q branch of the Operational Sign sequence storage circuit (Fig. 60), the Q branch being set at **2**. With **7**—**7***a* in OPSN (Fig. 78L) cut off, it is effective via **6***a*, **20***a*, **20** and **20***b* to produce the operational sign signal OPSN**2** which is applied to the sign mixing circuit (Fig. 71*a*) of the accumulator, as in Item 16*a*.

The Q**1** signal also tests the pilot units, by cutting off their tubes **3**, for selection by the subfield *b* of the Out field Q. In the present example, pilot unit **2** has been selected by code number 2 in Q*b*, as manifested by the signal Q*b***2** (Item 10). The signal Q*b***2** cuts off **3***a*–**5**CP (Fig. 80*e*) of pilot unit **2**. The Q**1** signal now cuts off **3**–**5**CP of all the pilot units. As **3***a*–**5**CP of pilot unit **2** has been cut off, the couple **3**—**3***a* in **5**CP of this unit acts via **4**, **1** and **9** in **5**CP of this pilot unit to produce the signal OC Int. This signal in pilot unit **2** is effective after entry into ES**2** has been completed, as manifested by the return of **21**–**1**CP (Fig. 80*a*) of this pilot unit, to cause the pilot unit to produce the signal ES**2** to Int (note Item 16*b*). The signal ES**2** to Int causes ES**2** to apply the number therein to the Internal bus-sets. In this way, the number received by ES**2** from relay storage unit **011** (see Item 15*b*) is applied to the Internal bus-sets.

The signal Pi**1**.OC again is produced (see Item

17a), this time under control of pilot unit 2. Under control of this signal, conditioned 24Q (Fig. 78d) becomes conductive and produces the signal Q–OC (see Fig. 79bb), turning 21R (Fig. 78e). Upon 21R turning, it produces the OP.OC signal which causes conditioned tube 10–ACC.C (Fig. 78A) to become conductive. As in Item 17a, when tube 10 becomes conductive, it turns 18 and 22, under respective control of which the cancel signal ECC and the accumulator entry signal ACC–RI are produced. Unlike the situation discussed in Item 17a, tube 10, when it becomes conductive does not turn 14, since 14 is already in its turned state and has not been reset. Accordingly, trigger 15 will not be operated and therefore the cancel signal RCC will not be produced. It is evident then that after entry of the first number of a plurality of numbers to be accumulated, the signal RCC is not produced as a preliminary operation to the entry of a number into the accumulator. Thus, the number previously entered (Item 17b) in the registers RC of the acculator remains in these registers. It should also be noted that when tube 10–ACC.C becomes conductive the second time, it is effective to restore 26 which was turned under control of the previcus accumulator cycle complete signal CYCPT (see Item 17b). In the same manner as explained in Item 17b, 25 again is turned, at the end of the entry signal ACC–RI, whereby the start signal ACC–ST is produced by commutator ACC.C and initiates the second accumulator cycle (see Figs. 72 and 73). During this accumulator cycle, the second number which in the present example is the number from a source (relay storage unit 011) selected by the Q field, is transferred from EC to RC of the accumulator in the manner described in Section 13. At the end of the accumulator cycle the signal CYCPT (see Fig. 71g) again is effective to cut off 28a–ACC.C (Fig. 78A). An AP pulse cuts off 28, and 28—28a then causes 25 to be reset which results in the turning of 26 and 27. With 26 turned, it cuts off 24a. 27 stays turned for one AP pulse cycle and causes the commutator ACC.C to produce the back signal OP.BS, in the manner explained in Item 17b. The signal OP.BS is effective this time to restore 21R (Fig. 78e). Upon restoration of 21R it terminates the Q.OC step in the manner explained in Section 16b, Item 26Q. The signal QI ends and terminates the exit signal ES2 to Int and the operational sign signal OPSN2. This removes the operational sign, designated in subfield Qs, from the mixing circuit in Fig. 71a and the number, along with its sign, derived from the source selected by subfield Qr, from the Internal bus-sets.

At this stage of the commutator run, the numbers from the sources selected by the P and the Q fields have been accumulated in the registers RC of the accumulator unit.

20. The return of 21R also initiates the scanning step of the R spot (Fig. 78e). This will be an In code step, because of the fact that field R is an In field and has conditioned the R spot in the manner explained in Item 14a. When 21R is restored, it turns 22 which is restored by the next AP pulse, as in the OC step. But this time upon restoration of 22 it is ineffective to turn 23. This is because 23 is now being locked in cancelled position under control of the signal R in acting through tube 27, as described in Item 14a. Inasmuch as 23 is not turned, it does not produce the RI signal which is characteristic of the R.OC step, and 24R is not conditioned to respond to a PI.OOC signal. When trigger 22R was turned, it acted through 9a to restore trigger 5 which has been turned under control of the signal R "in." Upon the restoration of 5, it turns 6. With 6 turned, it serves through 10 to produce a negative OP.IC signal. This signal is inverted by 28NO (Fig. 78c) to a positive OP.IC signal which renders conditioned 11–ACC.C (Fig. 78A) conductive. Note may be taken of the fact that the OP.IC signal is applied only to the accumulation calculation control commutator ACC.C. 11–ACC.C was conditioned previously under control of the OPI code number 02 (see Item 14c). 11 now becomes conductive and turns 23 which thereupon cuts off 24. 24a has already been cut off under control of trigger 26, turned under control of the last CYCPT signal (Item 19); hence 24—24a becomes completely cut off at this time and acts through 31 to turn 30. Upon 30 turning, it is effective via 32 to produce the negative signal R.ROC. Under control of this signal the internal commutator of the accumulator unit functions to initiate a test of the sign of the accumulated result. If the sign is positive, then the result read signal ACC–RO and the Proceed signal are sent out at once (see Section 13 and the upper portion of Fig. 73). If the sign is negative, then a complement conversion cycle takes place, which is followed by the signals ACC–RO and Proceed (see the lower portion of Fig. 73). The Proceed signal is coincident with the start of the readout signal ACC–RO. As understood from Section 13, the signal ACC–RO causes the accumulated number and its sign to be applied to the Internal bus-sets. The Proceed signal goes to the commutator ACC.C (Fig. 78A) and operates through 36a and 36 to turn 33. The next AP pulse restores 33 causing it to turn 34 and also to reset 23. 34 is restored by the following AP pulse and turns 35 which is itself restored by the next AP pulse. Upon restoration of 35, it restores 30, thus terminating the R.ROC signal. The termination of the signal R.ROC causes the accumulator readout signal ACC–RO to end, as described in Section 13. Upon the termination of the signal ACC–RO, the accumulated result and its sign go off the Internal bus-sets. The return of 35 also resets 14, in order that the cancel signal RCC may again be produced (see Items 17a and 19) in a new accumulation sequence run.

21. The accumulated result, and its sign, of the numbers from sources selected by the Out fields P and Q were applied to the Internal bus-sets by the signal ACC–RO produced under control of the signal R–ROC, as described. This signal was produced by commutator ACC.C as a result of its receiving the signal OP.IC from the scanning spot R during its IC step. The Proceed signal was sent, at the same time as the signal ACC–RO started, to the commutator ACC.C and under control of the Proceed signal, the scanning spot R will continue its IC step. During the continuation of this step, the R spot will initiate the operation of the denominational shift unit (see Section 12) to receive the accumulated result and shift it the programmed number of steps. The sign of the accumulated result is not received by the denominational shift unit per se but is stored in special triggers 2M and 6M (Fig. 78a). Thus, when a num-

ber and its sign have been applied to the Internal Out bus-set and the number is to be routed through the denominational shift unit, the sign is stored in the special triggers and will not be read out until the denominational shift steps have been completed and the shifted number has been read out. It is necessary to preserve the sign during the operation of the denominational shift unit, as otherwise it would be lost since the signal, as ACC–RO, for reading out the sign from a calculation unit is only a brief signal which terminates before column shifting starts.

22. Two AP pulse cycles after commutator ACC.C (Fig. 78A) received the Proceed signal, **35**, Fig. 78A, was turned (see Item 20). When **35** is turned, it acts through **31***a* to cut off **7***a*. The companion element **7** has been cut off before (see Item 14*c*) as a result of the commutator ACC.C having been selected and conditioned for operation. Now, when **7***a* is cut off, the couple **7**—**7***a* acts through **3** to produce the negative OP.BS signal. This signal is effective to restore trigger **6**R (Fig. 78*e*), terminating the OP.IC signal.

In brief review: the first OP.BS signal was produced by the turning of **27**, Fig. 78A, under control of the first cycle complete signal CYCPT (Item 17*b*). The signal OP.BS then functioned to return **21**Q which terminated the P.OC step and initiated the Q.OC step. The next signal OP.BS was produced again by the turning of **27**, Fig. 78A, under control of the second complete signal CYCPT (see Item 19) and caused return of **21**R to terminate the Q.OC step and initiate the R step. The return of **21**R caused **22**R to turn for one AP pulse cycle but since the R spot has been conditioned for an IC step, **23**R does not turn upon the return of **22**R and the signal R**1** is not produced, nor is **24**R conditioned and operated later to produce a signal R.OC for turning **21**T.

When **22**R was operated, in consequence of the return of **21**R by the second OP.BS signal, it reset **5**R, causing **6**R to turn and produce the OP.IC signal which caused the commutator ACC.C to apply the readout control signal R.ROC to the accumulator unit. This initiated operations of the accumulator unit which led to its production of the signal ACC–RO to cause the accumulated result and sign to be read out to the Internal bus-sets. Concurrently with the accumulator unit producing the readout signal ACC–RO, it sent the Proceed signal to commutator ACC.C. The effect of the latter signal on the commutator was to cause the trigger **35**–ACC.C to turn, as a result of which the signal OP.BS again was produced. This signal did not act, as it did before, to terminate an OC step and initiate a next scanning step. Instead, the third signal OP.BS returned **6**R to end the OP.IC signal (which initiated the reading out of the accumulated result from the accumulator unit) and to cause the R.IC step to continue, as follows:

Upon the return of **6**R, it turns **11**R. When **11**R turns, it operates through **12** to produce the negative signal CSI. This signal is effective through **4***a* and **4** of the commutator spot N (Fig. 78*b*) to turn triggers **2**N and **3**N concurrently. The next AP pulse returns **3**N causing it to reverse **1**N. The following AP pulse restores **1**N which thereupon restores **2**N. Upon the reversal of **3**N, it cuts off **14***a*. Tube **22***a* is also off because line **24***m* is at low potential under control of trigger **24**M (Fig. 78*a*). Hence, the cutting off of **14***a*, **78***b*, causes the couple **14***a*—**22***a* to act via **6**N to produce the negative cancel control signal SHCL. The trigger **2**N, reversed at the same time as **3**N, causes **5**N to produce the negative entry control signal SHRI. The signal SHCL is applied to **21**, Fig. 27*b*, of the internal commutator of the denominational shift unit. In the manner described in Section 12, this signal SHCL operates to produce the signal ACL, which applies a capacitatively fed resetting impulse, to each of the triggers ASH (Fig. 24) in the shift columns. The negative entry control signal SHRI acts via **25***a*, **25** and P**25** in Fig. 27*b* to produce the positive entry signal SHRI, which is applied to tubes IT in the shift columns. These tubes are already selectively conditioned according to the accumulated result applied to the Internal bus-sets under control of still effective signal ACC–RO. These conditioned tubes IT are made conductive by the positive signal SHRI and turn and hold turned the related triggers ASH, blocking these triggers from being canceled by the signal ACL. In this way, the accumulated result is entered in the shift columns.

The signal SHCL also initiates the operation of the SHC cancel circuit in Fig. 27*c*. The signal SHCL also is operative through tubes **4***a* and **4** in Fig. 78*a* to apply a negative capacitatively fed cancel impulse to the triggers **2**M and **6**M.

The negative signal SHRI, concurrent with signal SHCL, also operates via **8**M (Fig. 78*a*) to apply increased potential to the control grids of **3**M and **7**M. One of these is conditioned according to the result sign represented in Internal bus column **1**. If the sign is +, then bus **2** of column 1 of the Internal in bus-set is at high potential and conditioning **7**, but if the sign is —, then bus **1** of this column is at increased potential and is conditioning **3**. Whichever one of the tubes **3** and **7** is conditioned, becomes conductive under control of signal SHRI and reverses its connected one of triggers **2** and **6** and blocks cancellation of the reverse trigger by the momentary impulse derived from the signal SHCL. Trigger **2** may thus store the — sign, or trigger **6** the + sign, of the accumulated result.

It is to be noted that the entry control signal SHRI and the cancel control signal SHCL start concurrently at a time determined by the turning of trigger **35**, Fig. 78A. One AP pulse cycle later **35** is reset, causing the signal R.ROC to end and thereby end the signal ACC–RO as described before. Thus, one AP pulse cycle after start of signals SHCL and SHRI the accumulated result and sign are removed from the Internal buses. The signal SHRI thus has one AP pulse cycle entry time for causing the accumulated result and the sign to be entered into the shift column and sign storage triggers. This is sufficient because the effect of signal SHCL is momentary inasmuch as it is appled through capacty couplings to the entry receiving and storage triggers, while the effect of the signal SHRI is more lasting because it is applied through direct coupling to the entry receiving triggers. Also, it should be noted that the entry signal SHRI is produced two AP pulse cycles after the number and its sign are applied to the Internal bus-sets under control of the signal ACC–RO. This allows sufficient time for cross-talk and transients to disappear before the actual entry of the sign and number is effected under control of the signal SHRI.

The signal SHRI renders **8***a*, Fig. 78*a*, non-

conductive. Upon termination of this signal 8a returns to conductive condition and applies a negative, turning impulse to trigger 13M, which is restored by the next AP pulse. During its turned status 13M acts through 12 to produce the negative signal SHS which, as described in Section 12, acts upon 5, Fig. 27c, to cause the denominational shift unit to perform the number of shift steps determined by the shift program and entered into the descending counter (Fig. 27a) as described in Item 12a. At present, the shift program is the one determined by the subfield Rs and the field SH1 and, in the example, calls for zero shift.

When trigger 13M (Fig. 78a) is turned, in addition to causing the start signal SHS to be produced, it acts through 20 and 15 to produce the positive signal CTLR. This signal acts as described in Section 13 to cause the sign storage trigger 20, Fig. 71b, the trigger 23, Fig. 71b, the trigger 11, Fig. 71f, and the trigger 35, Fig. 71f, to be restored (also see Figs. 73 and 74).

When the denominational shift unit has completed its allotted number of shift steps, it produces the negative complete signal SHCP (see Fig. 27b and Section 12). This signal cuts off 14N (Fig. 78b), causing it to make 10N conductive. As a result 10N turns 9N. With 9N turned, it cuts off 11N which becomes effective at AP pulse time when 11a is cut off to render 10a conductive so as to produce the negative signal CSRD. This signal reverses 7N (Fig. 78b) and also 10M (Fig. 78a). The reversal of 10M is effective via 23 and 14 to produce the positive signal SHRD. This is inverted by 9 to the negative signal SHRO which goes to 32, Fig. 27b, and causes the shifted number in the denominational shift unit to be applied to the Internal bus-sets as described in Section 12. The positive signal SHRD also is applied to the control grids of 1M and 5M (Fig. 78a). One of these is conditioned depending on whether the — sign storage trigger 2M or the + sign storage trigger 6M has been reversed. If 1M has been conditioned, then the signal SHRD causes it to apply reduced potential to bus 1, column 1 of the Internal Out bus-set, so as to manifest the — sign. If 5 has been conditioned, then the signal SHRD causes it to apply reduced potential to bus 2 of column 1 of the Internal Out bus-set so as to manifest the + sign. The shifted number and its sign are now on the Internal bus-sets.

Trigger 7N (Fig. 78b) was reversed by the signal CSRD as described above. It is reset by the next AP pulse and causes 9N to restore and 8N to turn. Turned 8N acts via 12N to produce a positive signal CSV. This signal is inverted by 12aR (Fig. 78e) to a negative impulse which restores 11R which was turned when 6R was restored under control of the last issued OP.BS signal. The turning of 11R initiated the entry of the accumulated result into the shift columns and the sign of the result into the sign storage triggers 2M and 6M in Fig. 78a. Now, one AP pulse cycle after the shifted result is applied to the Internal bus-sets, the trigger 11R is reset.

At this stage, the calculation instruction stored in the B side of the OP1 pyramid (Fig. 59) and the shift instructions stored in the B side of the SH1 sequence storage circuit (Fig. 62) and the B side of the R shift code sequence storage circuit (Fig. 63) have been carried out. Accordingly, the selected calculation control commutator ACC.C (Fig. 78A) may be de-conditioned and the instructions read out from the SH1 and R shift code sequence storage circuits and from the OP1 pyramid may be discarded. In other words, the heating, under control of the signal b1, of the OP1 pyramid and the SH1 and Q and R shift code circuits may be terminated. Also, preparation may now be made for the heating of the B side of the OP2 pyramid and the B sides of the SH2 and U and V shift code sequence storage circuits.

The above results are accomplished under control of the signal FR which is this time produced in consequence of the restoration of 11R (Fig. 78e). This trigger 11R was restored about one AP pulse cycle after the accumulated result and its sign were read out from the denominational shift unit and the sign storage triggers to the Internal bus-sets. Upon 11R restoring, it turns 15R which thereupon makes 26a conductive so as to cut off 32 which produces the positive signal FR.

Signal FR acts through 1P (Fig. 78c) to turn 5P which is the first trigger in the Ink delay counter. Upon 5P turning it serves, as previously described, to cause the signal HCR to be produced for resetting the half correction suppression storage trigger 5, Fig. 71g, and also the tolerance check storage trigger 22, Fig. 21g.

When 5P is turned it makes 9P conduct so as to decrease the potential on the output line of the latter. One AP pulse cycle later 5 is returned and again cuts off 9, causing its output line to rise in potential and produce the positive signal ACCL. This signal makes 5, Fig. 78A, conduct and thereupon restore 6–ACC.C. This terminates the conditioning of the commutator ACC.C.

The positive signal FR also is inverted by 25a of the Z spot (Fig. 78k) to a negative impulse which this time returns 26Z. Note that 26Z was turned under control of the previous FR signal (see Section 16b, Item 26–1). Upon the return of 26Z, it returns 23 to a conductive status and as a result the heating control signal b1 is terminated. At the same time restored trigger 26 cuts off 31a. The tube 31 already is cut off under control of trigger 30 which was turned by the previous finish of scanning sequence signal FC (see Section 16b, Item 2). Since both 31 and 31a are now cut off, the tube 32 is made to conduct and produce the negative heating control signal b2. The signal b2 is inverted by 4 and 10 in Fig. 76a to a positive pulse which makes tubes 24 to 30, and 32, 33, 34 and 35 in Fig. 76b conductive. Accordingly, the B sides of the OP2 pyramid and of the SH2 and U and V shift code sequence storage circuits are heated.

Since in the assumed example the field OP2 bears the code number 04 which is now stored in the B side of the OP2 pyramid, the heating of the B side of this pyramid causes it to produce decreased potential on the output line OP04 (see Fig. 59). Reduced potential on line OP04 cuts off 29, Fig. 77a, causing 28a to conduct and cut off 30. This results in 24 producing the negative signal ACC Code. This signal, as described before in Item 13, prepares the commutator ACC.C (Fig. 78A) to be conditioned about two AP pulse cycles later by the Ink signal (also see Item 14c).

The signal HCSS (note Fig. 77d) is not produced this time as it was under control of the calculation code number 02, in field OP1. Ac-

cordingly, the trigger 5, Fig. 71g, will remain in its canceled status so that half correction of the accumulated result will be effected in the manner described in Section 13.

The heating of the B side of the SH2 circuit in Fig. 62 causes the output lines 4SH and 2SH to be reduced in potential since in the assumed example the SH2 code number is 6. The heating of the B side of the V branch of the shift selection circuit shown in Fig. 63 results in reduced potential being present on the output line RTSH, since the code number in sub-field Vs is 4.

The lines 2SH and 4SH, being at reduced potential, increased potential is produced on lines MN2 and 4 (see Figs. 78a and 27a and Item 11). Also, reduced potential on the line RTSH causes the line RT (see Figs. 78a and 27c) to be at increased potential. Subsequently, the Ink signal will cause the selected denominational shift amount 6, as represented now by increased potential on the lines MN2 and 4, to be entered in the descending counter (Fig. 27a). The Ink signal also will cause the shift direction control trigger 21 to be placed in its right-shift status as selected by the increased potential on the line RT (note Item 14b).

In the foregong manner the commutator ACC.C (Fig. 78A) is conditioned for the second half of the scanning sequence and the denominational shift unit is conditioned for carrying out the denominational shift of 6 columns to the right, as ordered by the S2Seq portion of the sequence line under discussion.

23a. The result of the accumulation ordered by the S1Seq portion has been applied by the denominational shift unit to the Internal bus-sets. The result is ready to be entered in electronic storage and then transmitted to the selected receiving unit.

Trigger 11R (Fig. 78e) was reset one AP pulse cycle after the result was applied to the Internal bus-sets by the denominational shift units. As 11R reset, it turned 15R. One effect of the turning of 15R was to produce the FR signal, as described before. Further, 15R when it turns acts through 3R and 32 and 33 to produce the signal R2. This signal senses all the pilot units for selection by the R branch of the IC–Int to ES trees (Fig. 58). Since the heated B side of the R branch is storing the code number 1, the signal IRC1 is being produced (Item 10m). This signal is cutting off 43a–5CP (Fig. 80e) of pilot unit 1, thus selecting this pilot unit for producing the signal, Int to ES1, which is to bring the result of the calculation into electronic storage unit 1. The time for producing this signal has now arrived, as manifested by the production of sensing signal R2. Signal R2 cuts off tubes 43 of all the pilot units. Since the tube 43a of pilot unit 1 also is at cut-off, couple 43—43a of this pilot unit becomes effective through 44, 41, and 33 to produce the pilot unit negative signal IC Int. This signal cuts off 35–1CP (Fig. 80a) of pilot unit 1. Tube 35a–1CP is cut off except when transmission is taking place from electronic storage unit 1 to the In bus-set 1. As such transmission is not taking place, the tube 35a–1CP of pilot unit 1 is at cut-off and when 35 is cut off by the signal IC Int, the couple 35—35a becomes effective to render 30 conductive. As a result, 29 is turned and causes 23 to turn. When 29 is turned it cuts off 11 which causes 5 to produce the negative signal Int to ES1 (see Figs. 21 and 22 and Section 6). When 23–1CP (Fig. 80a) of pilot unit 1 is turned, it acts through 16 and 4 to produce the positive cancel signal ESC1. As a result of the production of these signals ESC1 and Int to ES1, electronic storage unit 1 is canceled and the number and sign present on the Internal bus-sets are entered into this storage unit in the manner described in Section 6. Trigger 23–1CP is returned by the next AP pulse, so that cancel signal ESC1 has a duration of one AP pulse cycle. When 23 returns, it turns 17. The next AP pulse returns 17, which causes 29 to return. Thus, the entry signal Int to ES1 lasts for two AP pulse cycles.

In the present example, the number and sign on the Internal buses are those of the accumulated result which is being applied to the Internal buses under control of signals SHRO and SHRD, as described in the preceding item. The tubes Int En (Fig. 21) of the electronic storage units are now being conditioned according to this accumulated result. Two AP pulse cycles after the signals SHRO and SHRD were issued, the trigger 15R (Fig. 78e) was turned to cause signal R2 to be produced. This signal, in turn, caused the selected pilot unit 1 to produce the ESC1 and Int to ES1 signals. The Int to ES1 signal renders the conditioned tubes Int En of electronic storage unit ES1 conductive, causing these tubes to turn the related storage triggers and to block them from being reset under control of the cancel signal ESC1. As the signals ESC1 and Int to ES1 were not issued until two AP pulse cycles after the result signals were applied to the Internal buses, cross-talk arising from the result signals will have died out before the signal Int to ES1 is applied to the set of tubes Out En of electronic storage unit ES1.

When trigger 29–1CP (Fig. 80a) turned to cause the entry signal Int to ES1 to apear, it also made 30a conductive to cause the negative signal Pil.IC to appear. This signal made tube 40 (Fig. 80a), common to all the pilot units, nonconductive, so as to produce the positive signal Pil.IC. The signal Pil.IC makes 12W (Fig. 78i) conduct, causing it to turn 11W for one AP pulse cycle. Upon the return of 11W, it turns 10W for one AP pulse cycle. Upon the return of 10W, it makes 9W conduct causing it to produce the negative signal Pil.ICC. This signal is applied to the trigger 15 in each of the scanning spots Q to V (Figs. 78d to h). As only the trigger 15 of spot R (Fig. 78e) is in turned condition, the signal Pil.ICC is effective only on this trigger and restores it.

23b. The signal Pil.ICC was produced in the manner described above two AP pulse cycles after 29–1CP (Fig. 80a) was turned. Trigger 29 was turned under control of signal R2 to initiate the entry from the Internal buses into electronic storage. Two AP pulse cycles later, the signal Pil.ICC restores 15R (Fig. 78e), ending the R2 signal and also the FR signal. The return of 15R also turns 16R. The next AP pulse resets 16R but meanwhile, 16R cuts off 20a to produce a negative signal CSF on a line common to spots Q to V. The signal CSF is effective through 11a and 11 in Fig. 78a to restore 10M, thereby ending the SHRO and SHRD signals. The accumulated result thus applied to the Internal buses by the denominational shift unit is removed from these buses two AP pulse cycles after the entry signal Int to ES1 was produced. In other words, the accumulated result is removed at the same time as the entry signal ends.

When 16R (Fig. 78e) was turned, it also acted

through 4 and 34 and 35 to produce the negative signal R3.

The shifted accumulated result, including its sign, has now been entered into electronic storage unit 1 and is to be transmitted therefrom to In bus-set 1 and thence to selected relay storage unit 030 (see Item 5). There are three conditions for transmission of data from electronic storage to an In bus-set.

23c. One of these conditions is the production by a commutator spot which has been conditioned for an IC step, of its "3" signal after this spot has produced its "2" signal. In the present example, spot R is conditioned for an IC step and has produced its signal R2 to cause pilot unit 1, selected by subfield Rb, to pilot the result on the Internal bus-sets into electronic storage unit 1. After the entry of the result into electronic storage unit 1 was completed, the spot R produced the signal R3. Production of this signal satisfies one of the conditions for transmission from the storage unit to the related In bus-set.

It should be noted that for the transmission of sequence data, the main commutator, under control of signal AE, produces the signal SW (see Figs. 78*j* and 80*e* and Item 15*d*) which takes the place of the "3" signal from a commutator spot.

23*d*. Another condition for the transmission of data from electronic storage to an In bus-set is the production of the signal PRE. This signal is produced by a selected pilot unit as a result of the mixing of a tree signal PRES with the commutator signal NPR (in the case of transmission of data other than sequence data), or the signal SPR (for the transmission of sequence data).

23*e*. A third condition for the transmission of data from electronic storage to an In bus-set is the receipt, by the selected pilot unit, of a Back signal when the unit which has been selected to receive the transmitted result has been conditioned to receive data from a selected In bus-set. In the example, relay storage unit 030 has been selected by subfield R*r* (Item 5) to receive data from In bus-set 1 and the Back signal is being applied to bus 81 of this In bus-set. This signal makes 23–3CP (Fig. 80*c*) of pilot unit 1 conductive. When 23 conducts it cuts off 25 causing 25*a* to be conductive and via switch 2SQ in norm position to maintain 24 (Fig. 80*c*) at cut-off. This satisfies a third condition for transmission under control of pilot unit 1. Similarly, relay storage unit 151 has been selected by field V to receive data from In bus-set 5 and a Back signal is being applied to bus 81 of this bus-set. This signal makes 23–3CP of pilot unit 5 conductive with the result that 24 of this pilot unit is cut off.

It should be noted that in the case of transmission of sequence storage a Back signal is not received by the pilot unit selected for piloting such transmission. Such pilot unit, however, has its switch 2SQ (Fig. 80*c*) set in seq position so as to allow the signal ICI, produced under control of the signal SW, to be effective via 26 and switch 2SQ to substitute for the Back signal in cutting off 24. This is in addition to the functioning of the SW signal as a substitute for the "3" signal from the commutator spot conditioned for an IC step. The transmission of sequence data, therefore, in reality requires but two conditions. One of these is the SW signal and the other is the PRE signal (see Section 16*b*, Items 20 and 31).

23*f*. The signals NPR and SPR are produced by the commutator in a manner which is clear from Section 16*b*, Items 21 and 38, and the last part of the summary in Section 16*b*. Briefly, in addition to the three conditions for causing new OCO and PS signals to be produced and transmitted (see Item 15*a*), a fourth condition is necessary to the production of the signals SPR and NPR (subsequent to the first "Artificial" line run). This fourth condition is the return of the trigger 27X (Fig. 78*j*) by an ATD signal which follows by some 16 ms. the AT signal. This latter signal manifests the completion of all data transmission called for by a program line and carried into effect during a commutator run. In the "Artificial" line commutator run (Section 16*b*), the signals STR and AT were produced concurrently (see Section 16*b*, Item 33). Also, in this "Artificial" line run SPR and NPR were produced prior to AT. In subsequent runs of the commutator SPR and NPR are produced only after ATD resets trigger 27X, to thus evidence that all data has been transmitted. Accordingly, such SPR and NPR signals will follow the OCO and PS signals. The signals SPR and NPR are of one AP pulse cycle duration.

With regard to the transmission of the sequence data, per se, selected by the fields S1 and S2 in the first "Real" line of sequence taken as an example, the signal SPR is mixed with the signals PRES1 and 8 to cause the pilot units 7 and 8 to produce their signals PRE (see Section 16*b*, Item 23). Under control of these signals the tubes 24*a*–3CP (Fig. 80*c*) of the pilot units 7 and 8 are cut off, conditioning the couples 24—24*a* of these pilot units to be made effective under control of the signal SW, in the manner described in Section 16*b*, Item 31. The transmission of sequence data will take place this time to the A side of sequence storage which has been opened to receive sequence data (see Section 16*b*, Item 35), while the B side has been barred against receipt of data. The third sequence data line, therefore, will be transmitted to the A side of sequence storage. When this transmission has been completed, the pilot units produce the pilot signal STR.

The signal NPR, produced at the same time as the signal SPR, is effective upon those pilot units which are set with their respective switches 5–SQ (Fig. 80*e*) in norm position, to cut off their respective tubes 16*a*–5CP. In the example, the tree signals PRES1 and 5 have been produced (Items 10*e* and 10*f*). These signals respectively maintain tubes 16–5CP (Fig. 80*e*) of pilot units 1 and 5 at cut-off, and thus select these pilot units to respond to the signal NPR. Upon this signal cutting off tubes 16*a*–5CP, couples 16—16*a* of pilot units 1 and 5 become effective to produce, through tubes 15 and 13, the respective presense signals PRE of these pilot units. These presense signals, which are positive, act through 36–3CP (Fig. 80*c*) of pilot units 1 and 5 to turn their respective triggers 30–3CP. As a trigger 30–3CP turns, it turns 29–3CP. The triggers 30 and 29 in 3CP of pilot units 1 and 5 are thus turned to store the fact that these units have been presensed for producing transmission. With 29–3CP turned, it cuts off 24*a*. This satisfies the condition for transmission discussed in Item 23*d*. This condition is satisfied under control of a presense signal which presenses the fact that a pilot unit has been selected for piloting transmission from electronic storage to an In bus-set.

As explained in Section 16*b*, Items 23 and 32, the turned triggers 30 in pilot units 7 and 8,

which are piloting sequence data, make tubes **35**, **35***a* and **23***a* conductive and condition the tube **17** in each of these pilot units. The tubes **35** and **35***a* while conductive block the AT and STR signals, respectively. The tube **23***a* while conductive blocks trigger **10** from turning, under control of a signal RDL, so as to prevent a Reset signal from being produced by the pilot unit. The tube **17** is conditioned in order that the transmission delay (7.5 ms.) should start at the same time as the transmission signal ES to In. The transmission of sequence data will not be described in further detail since it has been described already in Section 16*b*.

With regard to a pilot unit for piloting data other than sequence data, the turned trigger **30**–3CP renders tubes **35**–3CP alone conductive. Since switch **4SQ** is in norm position, the tubes **35***a* and **23***a* are not rendered conductive and the tube **17** is not conditioned. Thus, in the present example, tubes **35***a* of pilot units **1** and **5** are made conductive by turned triggers **30**–3CP. These tubes **35** also block the AT signal.

It is seen now that the Back signal to pilot unit **1** and the presense signal applied to this pilot unit combine to cut off the couple **24**—**24***a* in 3CP of pilot unit **1**. Similarly, the Back signal and presense signal in pilot unit **5** combine to cut off the couple **24**—**24***a* in 3CP of this pilot unit.

When **24**—**24***a* in the pilot unit **1** or **5** has been competely cut off, then at the next BP pulse time when **27***a* is cut off, the common anode line of **24**—**24***a*—**27***a* rises in potential and makes **18** conduct. This causes **33** to turn and cut off **26***a* to produce the positive signal RDL. Moreover, when **26***a* is cut off, it makes **19** conduct and turn **13**, whereupon **13** cuts off **14**. Also, when **19** conducts it turns **10**. Turned trigger **10** cuts off **9**, causing **5** to become conductive and produce the negative Reset signal upon bus **82** of In bus-set **1**. This signal, in a manner explained in Section 7, causes the selected relay storage unit to be reset. Trigger **33** is reset by the next occurring AP pulse and thereupon resets trigger **29**.

It is clear now that when two of the conditions, the receipt of a Back signal and the receipt of a presense signal by a selected pilot unit have been satisfied, that the tube **14**–3CP of this pilot unit is cut off and, at the same time, a positive signal RDL is produced.

The RDL signal initiates the operation of the Reset Delay counters in 4CP (Fig. 80*d*) of the pilot unit, in the manner explained in Section 16*b*, Item 33. It is seen further that when the two mentioned conditions for transmission have been satisfied, the selected pilot unit produces the Reset signal for resetting the relay storage unit which has been selected to receive the transmitted data.

The Reset Delay counter produces, some 15 ms. after it has started operation, the delay pulse RDL #2. This pulse renders **34***a*–3CP conductive so as to turn **28** which thereupon conditions **22**.

In brief, when the two mentioned conditions for transmission, i. e., the Back signal and the presense signal have been produced, the couple **14**—**14***a* in 3CP is conditioned by **14** being cut off, and the tube **22**–3CP is conditioned by turned trigger **28**, and also a Reset signal is produced.

24. Signal R3 (see Fig. 78*e*) was produced after the accumulated result was entered from the Internal buses into electronic storage unit **1**, selected by In field R (see Item 23*b*). Signal R3 satisfies one of the three conditions for transmission under control of selected pilot unit **1** (see Item 23*c*). The signal R3 senses the pilot units for conditioning by the pilot unit selection trees IC–ES to In (Fig. 56). As explained in Item 10*g*, the R*b* branch of these trees has produced the tree signal ICR**1**. As a result, **28***a*–5CP (Fig. 80*e*) of pilot unit **1** is cut off. The signal R3 cuts off the tube **28**–5CP in each of the pilot units. Since **28***a* of pilot unit **1** has been cut off, couple **28**—**28***a* of this pilot unit becomes effective through **35***a* to cut off **34** so as to produce the positive signal ICI. This signal makes **26**–3CP (Fig. 80*c*) of pilot unit **1** conductive so as to reverse trigger **20**. Reversed **20** cuts off **19***a* and **14***a*. When **19***a* is cut off, it produces the positive transmission interlock signal TR. Ink. This signal makes **33***a*–2CP (Fig. 80*b*) and **35***a*–1CP (Fig. 80*a*) conductive. With **33***a*–2CP conductive, it prevents the pilot unit from producing an entry signal Out to ES. With **35***a*–1CP conductive, it blocks the pilot unit from producing an entry signal Int to ES. It is seen that upon receipt by a pilot unit, selected by an In field, of the "3" signal from the scanning spot associated with the In field, the pilot unit is blocked from producing entries into its related electronic storage unit from the Out buses or from the Internal buses. In the example, signal R3 has been received by pilot unit **1** and this pilot unit is now blocked against piloting entries into electronic storage unit **1** from the Out bus-set **1** or from the Internal buses. This block on pilot unit **1** will be maintained until transmission has taken place from electronic storage unit **1** to In bus-set **1**.

As described in Items 23*d*, *e* and *f*, the two other conditions for transmission under control of pilot unit **1** are the receipt of a Back signal from selected relay storage unit **030** and the receipt of the presense signal NPR. Assuming the Back signal has been received, **24**–3CP is at cut-off. Assuming the presense signal has been received, the tube **24***a*–3CP has been cut off. Accordingly, **18**–3CP has been made conductive at BP pulse time and turned **33**–3CP which results in the turning of **13** and **10** in 3CP, and the production of signal RDL to start the Reset Delay counter (4CP) in operation. The turning of **10**–3CP caused the Reset signal to be applied to bus **82** of In bus-set **1**, in order to reset selected relay storage unit **030**. The turning of **13**–3CP cuts off **14**–3CP.

As described in the present item, the R3 signal has caused **20**–3CP of selected pilot unit **1** to be turned, whereupon the interlock signal TR.Ink was produced and **14***a*–3CP was cut off.

Now, when all three conditions for transmission have ben met, couple **14**—**14***a* in 3CP is completely cut off and renders the normally non-conducting tube **7**–3CP conductive, whereupon **16**–3CP is turned.

Turned **16**–3CP of pilot unit **1** acts via **8**, **3** and **3***a* to produce the positive transmission signal ES**1** to In. As explained in Section 6, this causes electronic storage unit **1** to be read out to In bus-set **1**. Thus, the accumulated result now in ES**1** is transmitted via In bus-set **1** to selected relay storage unit **030**.

Also, trigger **16**–3CP, upon being turned, acts via **2** to apply increased potential to **22**. This has been conditioned as described in Item 22 under control of the 15 ms. delay pulse RDL #2. Hence, **22** now becomes conductive and resets **10**

thus terminating the Reset signal. It is seen that the Reset signal will be terminated under joint control of the delay signal RDL #2 and the turning of trigger 16 at the time it produces the transmission signal. The transmission signal cannot occur before the Reset signal because the Back signal and the NPR presense signal are required as well as the scanning signal R3. At best then, the Reset and transmission signals may occur simultaneously. When a pilot unit is used to pilot sequence data, the turning of 16 to produce the transmission signal acts via 2 to render 17 conductive which is conditioned by turned 30 when switch 4SQ is in Seq position. When tube 17 becomes conductive it cuts off 12 to produce the TRS signal for initiating the operation of the 7½ ms. transmission delay counter TR in 4CP (Fig. 80*d*). At the end of this transmission delay, the trigger 16–3CP is restored (see Item 32, Section 16*b*). In the present case where pilot unit 1 is being used for piloting other data than sequence data, tube 17–3CP (Fig. 80*c*) is not conditioned because switch 4SQ of this pilot unit is in norm position. Accordingly, the transmission delay does not start solely under control of the turning of 16 when it initiates the transmission signal. Instead, it starts with the return of 10–3CP and the termination of the reset signal. The return of 10, as described above, is effected when the coincidence tube 22 is made to conduct under the joint control of the RDL #2 signal and the turning of 16 when it starts the transmission signal. Upon the restoration of 10 in the above manner, it turns 11. This cuts off 12 to produce the signal TRS for initiating operation of the transmission delay counter TR in 4CP. At the end of this delay, the pulse TRD is produced. This pulse is inverted by 18–3CP to a negative pulse which turns 15 and restores 16. The restoration of 16 terminates the transmission signal. Thus, when a pilot unit is used to pilot data other than sequence data, the transmission signal lasts at least 7½ ms. longer than the Reset signal. When a pilot unit is used for piloting sequence data, the reset delay signal RDL #3 occurring 5 ms. after the Reset delay signal RDL #2, causes 15–3CP to turn (see Item 33, Section 16*b*). But when a pilot unit is used for piloting other data than sequence data, the switch 3SQ is in norm position and therefore the RDL #3 pulse has no effect. Instead 15 is turned concurrently with the return of 16 at the end of the 7½ ms. transmission delay. Trigger 15 is reset by the next AP pulse and turns 21 which is restored by the following AP pulse. When 21 is in turn restored, it acts via 27 to restore 13, 20, 28, 30, and 11, thus ending the transmission control operations. The return of 20–3CP in pilot unit 1, removes the interlock signal TR.Ink from blocking control over pilot unit 1. The return of 30–3CP in pilot unit 1 removes this pilot unit from blocking control over the AT signal.

25. Trigger 16R (Fig. 78*e*) was turned (Item 23*b*) to produce the scanning signal R3 as a condition to the transmission signal. Trigger 16R is restored by the next AP pulse, ending the R3 signal. Upon 16R being restored, it turns 19R which is reset by the following AP pulse. Meanwhile, 19 in its turned status cuts off 20R to produce the positive signal R.IC which goes to the T scanning spot. This marks the termination of the IC scanning step of commutator spot R.

The S1Seq portion of the first real line of sequence data entered in the B side of sequence storage has now been interpreted and its instructions have been carried into effect.

26. The positive signal R.IC is applied to the control grid of 18T (Fig. 78*f*). Since the spot T has not ben conditioned for an In step, the suppressor of 18T has remained at conditioning potential. Accordingly, at completion of the IC step of the R spot, signal R.IC renders 18T conductive, causing it to turn 23T. This conditions 24T and also causes signal T1 to be produced. This signal senses the pilot units for a selection by the T field. In the example, the T field has selected pilot unit 3. This selection results from tree signal T*b*3 (Item 10*h*) which cuts off 6*a*–5CP (Fig. 80*e*) of pilot unit 3. The signal T1 now cuts off the tubes 6–5CP of all the pilot units. As 6*a*–5CP of pilot unit 3 also is cut off, couple 6—6*a* of pilot unit 3 becomes effective via 7, 1 and 9 in 5CP to produce the negative signal OC Int of this pilot unit. In a manner clear from Item 16*b*, this signal causes the pilot unit 3 to produce the signal ES3 to Int. Under control of signal ES3 to Int, the data received from tape storage station 1, bank 2 by electronic storage unit 3 (see Item 15*b*) is now applied to the Internal bus-sets. A Pil.OC signal is sent at the same time to the commutator spot W (Fig. 78*i*). This is followed by the Pil.OCC signal (see Item 17*a*) which causes conditioned 24T (Fig. 78*f*) to produce the signal T.OC. The latter signal turns 21U (Fig. 78*g*), causing it to produce an Op.OC signal. As commutator ACC.C (Fig. 78A) has again been conditioned (Item 22), this commutator responds to the signal OP.OC and produces the signals ECC, RCC, and ACC–RI. Consequently, the number and sign now present on the Internal buses are entered in the accumulator unit. The T1 signal also has caused the operational OPS1 to be applied to the mixing circuit (Fig. 71*a*). A detailed description of these operations is unnecessary since they are similar to those controlled by the P1 signal in this example (note Items 16*a*, 17*a*, and 17*b*). When the accumulator cycle has been completed, the commutator ACC.C produces the signal OP.BS which causes 21U to return, thus ending the T OC step and initiating the U OC step. During the latter step, the signal U1 is produced and causes the operational sign 2 to be applied to the mixing circuit (Fig. 71*a*) and the selected pilot unit 6 to produce the signal ES6 to Int. This causes the data received by electronic storage unit 6 from tape storage station 10, bank 2 (Item 15*b*) to be applied to the Internal buses. Another Pil.OC signal is produced and results in the now-conditioned tube 24U (Fig. 78*g*) producing the signal U.OC which turns 21V (Fig. 78*h*). As 21V turns, it causes an OP.OC signal to be produced. This signal renders conditioned commutator ACC.C (Fig. 78A) effective to produce the signals ECC, ACC–RI and then the signal ACC–ST, so that the number on the Internal buses is entered into the accumulator unit and another accumulator cycle takes place.

At the end of the last mentioned accumulator cycle, a complete signal CYCPT again causes the commutator ACC.C to produce a signal OP.BS (see Item 17*b*). This signal resets 21V which thereupon terminates the U OC step and initiates the scanning step of the V spot (Fig. 78*h*). As this spot has been conditioned for an IC step (Item 14*a*) its trigger 5V is in turned status. In a manner such as described in Item 20, when 21V is restored it turns 22 which causes trigger 5 to be reset. As 5V resets, it turns 6V which thereupon

acts to produce an OP.IC signal. This signal causes the commutator ACC.C to issue the signal R.ROC. The latter signal is applied to the accumulator unit and initiates a sign test of the accumulated result. Since trigger 5–71*g* has not been reversed, it is not storing a half correction suppression condition (see Item 22). Accordingly, the sign test is the first step in the half correction procedure which has been outlined in Section 13 and indicated in Fig. 74. In the course of this procedure the accumulated result is entered into the denominational shift unit (Fig. 25) after which shift steps are initiated. The accumulator unit is then canceled except for the stored sign, and a half correction entry of 5 is made into the first accumulator order. When the shift unit has completed all but one of the selected number and shift steps, it sends a complete signal SHCA to the accumulator unit and at the same time reads out the sub-shifted result to the Internal buses. In response to the complete signal SHCA, the accumulator unit receives the sub-shifted result to be accumulated with the half correction entry of 5 in the first order. At this point the accumulator unit contains the half corrected result in the orders above the first order. The accumulator unit then produces its readout signal ACC–RO and at the same time the Proceed signal is sent to commutator ACC.C (Fig. 78A).

The Proceed signal acts in the manner described in Items 20, 21 and 22 and causes the commutator ACC.C to produce another back signal OP.BS. This signal now restores 6V which causes 11V to turn and produce the signal CSI, under control of the latter signal, signals SHCL and SHRI are produced and the sub-shifted result now being applied to the Internal buses by the accumulator unit is entered into the denominational shift unit, and the sign of the result is entered into the sign storage trigger 2M or 6M (Fig. 78*a*). Upon termination of the SHRI signal the signal SHS is produced by the turning of 13M. This causes the denominational shift unit to perform the number of steps called for by the number now present in the descending counter (Fig. 27*a*). Originally, the number entered into the descending counter for the second half of the present commutator run was 6 (see Item 22). During the half correction procedure for the accumulated result, the denominational shift unit performed five shift steps, and the descending counter now therefore stands at 1. Accordingly, under control of the signal SHS produced under control of the main commutator, the denominational shift unit performs the final shift step, completing the total of six shift steps to the right called for by the S2Seq portion of the line of sequence data.

When the shift has been completed the denominational shift unit sends out the complete signal SHCP. Under control of this signal, the trigger 9N (Fig. 78*b*) is turned to cause the signal CSRD to be produced at the next effective AP pulse time. This signal reverses 7N and also 10M. Reversed 10M causes the signals SHRD and SHRO to be produced for timing the reading out of the shifted number and sign to the Internal buses. One AP pulse cycle after 7N is turned the trigger 8N acts to produce the positive signal CSV, as a result of which the trigger 11V is reset.

Upon the restoration of 11V (Fig. 78*h*), it turns 15 so that the signal V2 is produced. This signal senses the pilot units for a selection by the V branch of the IC-Int to ES trees (Fig. 58). This branch is storing the code number 5 and therefore is producing the tree signal IVC5 (Item 10*h*). This tree signal cuts off 48*a*–5CP (Fig. 80*e*) of pilot unit 5. The V2 signal now cuts off tubes 48 of all the pilot units. Since 48*a* of pilot unit 5 has been cut off, the couple 48–48*a* of this pilot unit now acts through 47*a*, 41 and 33 to produce the negative signal IC Int. In the manner which is clear from Item 23*a*, this signal is effective to cause the pilot unit 5 to produce its signals ESC5 and Int to ES5. Consequently, the shifted result and its sign are now entered in electronic storage unit 5.

Upon the production of the signal Int to ES5, the pilot unit 5 produces the signal Pil.IC which brings about the return of 15V (Fig. 78*h*). This terminates the V2 signal. Upon the return of 15, it turns 16 which causes signal CSF to be produced for terminating the SHRO and SHRD signals (see Item 23*b*).

The turning of 16 also causes the signal V3 to be produced by the V spot. The signal V3 cuts off the tubes 31–5CP (Fig. 80*e*) of all the pilot units. The tree signal ICV5 has been produced in the manner described in Item 10*f* and is cutting off 31*a* of pilot unit 5. Accordingly, the signal V3 renders 31—31*a* of this pilot unit effective to produce the pilot unit 5 signal ICI.

In the manner described in Item 24 this signal produces the transmission interlock signal TR Ink and causes 14*a*–3CP of pilot unit 5 to be cut off. It has been assumed that the presense signal NPR has been applied to the pilot units and has caused 24*a*–3CP of pilot unit 5 to be cut off (see Item 23*f*). Assuming that the Back signal from the Vr-selected relay storage unit 151 has been received by pilot unit 5, all three conditions for transmission under control of pilot unit 5 have been satisfied and the signal ES5 to In is produced for causing the shifted accumulator result to be read out from electronic storage unit 5 into selected relay storage unit 151.

Trigger 16V (Fig. 78*h*) is returned after being turned for one AP pulse cycle. The return of 16V terminates the V3 signal and also causes 19V to turn. As a result, 20V produces the positive signal V.IC which renders 13W conductive, causing 17W (Fig. 78*i*) to return. It should be noted that in the first scanning sequence and also whenever the V field is blank, the negative V.OC signal will be produced by the V spot (see Section 16*b*, Item 26*v*) to cause 17W to return. It is also to be remembered that 17W was turned after all three conditions for a new commutator start had been established (see Section 16*b*, Item 39).

Upon restoration of 17W the tube 18W is cut off. This satisfies one condition for a new commutator run, this one condition being the termination of the scanning sequence in the present run.

Also upon 17W restoring, it causes 5W to produce the signal FC. This signal is inverted by 26N, Fig. 78*b*, to a negative signal for restoring the triggers 19 and 31 which have been storing the In conditioning of the scanning spots R and V. The FC signal also acts through 29*a* (Fig. 79*k*) to return 30Z. It should be noted that 30Z was turned in the preceding scanning sequence (see Section 16*b*, Item 22*a*) in order to drop out the *a*2 signal. With trigger 30 then turned, it conditioned 31—31*a* to produce the *b*2 signal when 26Z was subsequently restored under control of the FR signal, as described in Item 22. Now, at the end of the present scanning se-

quence, the signal FC returns 30Z as a result of which the signal *b2* is dropped.

The return or back signals SE, AE, STR and AT produced during the present run are discussed below.

The SE signal occurs when the selected sequence data have been safely entered into the then open side of electronic storage. Such selection has been made in accordance with the setting of the S1, S2 pyramids (Fig. 50) in the B side of sequence storage. When the selected sequence data have been safely entered into electronic storage the heating of the B side of the S1, S2 pyramids may be terminated and preparation may be made for the heating of the B side of sequence storage. The SE signal this time causes the trigger 10, Fig. 75*e*, to return and thereby drop the heating relay Y1 for the B side of the S1, S2 pyramids. Note that 10 was turned by the preceding SE signal (Section 16*b*, Item 29) in order to drop the heating relay X1 for the A side of the S1, S2 pyramids. The next STR signal then returned 16, Fig. 75*e* (this was turned by the first STR signal; Section 16, Item 7), in order to energize the heating relay Y1. Now the SE signal when produced in the present run, returns 10, Fig. 75*e*, whereupon Y1 is deenergized. When the next STR signal is given, it again turns 16 and X1 is again energized as in Section 16*b*, Item 7.

The AE signal is produced when all the entries called for by the active line of sequence data have been safely made into electronic storage. When the signal AE is produced it causes 7X (Fig. 78*j*) to be turned and to produce the sequence data transmission control signal SW, in the manner described in Section 16*b*, Item 31. The signal SW and the presense signal SPR combine to control the two selected pilot units 7 and 8 to transmit the selected sequence data to the open side of sequence storage. In the present run the open side is the A side and the relays AI will be energized selectively in accordance with the second real line of sequence data. As a corollary to the transmission of the new sequence data into the A side of sequence storage, the previously operated relays AOR and AOP are to be reset.

The trigger 7X, Fig. 78*j*, was turned to produce the SW transmission signal for the sequence data to be transmitted to the then open A side of sequence storage (see Item 23*f*). One AP pulse cycle later the restoration of 7X causes the signal ICIC to be produced. This signal, in a manner described in Section 16*b*, Item 34, initiates operation of the ICIC delay counter in Fig. 75*d*. The trigger 18, Fig. 75*d*, was turned under control of the preceding ICIC signal. As a result relays BOR were energized. The next STR signal returned 16, Fig. 75*d*, causing relays BOR to be deenergized (Item 35, Section 16b). Now the new ICIC signal produced in this commutator run acts through the ICIC delay counter to return 18, so the relays AOR are energized as in Section 16*b*, Item 2. When the sequence data have been safely transmitted into the A side of sequence storage, the STR signal is produced and causes the relays AOR to be deenergized, so that the stick circuits for the AOP relays are made, just as in Section 16*b*, Item 5.

The signal AE is followed, after some 15 ms. by the signal AED (see Section 16*b*, Item 27). The latter signal resets 19W, Fig. 78*i* (note that 19W was turned after a condition for a new commutator run had been satisfied; see Section 16*b*, Item 39). Now the new AED signal restores 19W cutting off 18*a*. This satisfies a condition for a new commutator run. Another condition referred to previously is the return of 17W at the end of the scanning sequence so as to cause 18W to be cut off.

The AE signal also returns 22, Fig. 75*a* (see Section 16, Item 2). As a result, the relays YM and Y2 are deenergized. Further, the signal restores 24, Fig. 75*f*, 18 and 30 in Fig. 75*g*, and 12 in Fig. 75*h*. Consequently, the relays Y3, 4, 5 and 6 are deenergized (see Section 16*b*, Item 36). As the relays YM, and Y2 to Y6 are deenergized, the heating of the B sides of the Out sequence storage circuits terminates. This may be safely done now as all the numbers from the sources selected by the B sides of these circuits have now been entered, from the Out bus-sets, into electronic storage.

When the sequence data has been safely transmitted into sequence storage, the pilot units produce the signal STR. Briefly, this signal produces the STR commutator signal (Fig. 78*k*) which accomplishes the following.

It returns 16, Fig. 75*d*, in order to drop out the relays AOR, as in Section 16*b*, Item 5.

The signal STR also turns 16, Fig. 75*e*, in order to pick up the relays X1 to heat the A sides of the S1, S2 pyramids (Fig. 50).

The signal also turns 28, Fig. 75*e*, and since 22 has been seset under control of the all-entry signal AE, the relays X2, XM, and then X3, X4, X5, and X6 are again energized, as in the first run of sequence (see Section 16*b*, Items 9, 10, and 11) to heat the A sides of the Out sequence storage circuits.

Signal STR also turns 2, Fig. 75*e*, so that the relay AM is dropped and the relay BM is reenergized. Consequently, the B side of sequence storage is ready for the third real line of sequence data, while the A side now storing the second read line is shut.

The signal STR also starts the S transmission delay which, after some 10 ms., produces signal STRD1 which turns 22, Fig. 75*d* (this was restored by the previous STRD1 signal; see Section 16*b*, Item 39). Since 22, Fig. 75*b*, is now again turned by the new STRD1 signal, the relays AIR are again energized as in Section 16*b*, Item 13. The later STRD2 pulse turns 28 and causes relays AIR to be dropped (see Section 16*b*, Items 18 and 19).

The STRD1 signal also turns 23W (Fig. 78*i*) causing it to apply a potential rise to 14W. This satisfies a third condition for a new commutator run. If the other two conditions; namely, the completion of the scanning sequence and the production of the AED signal also have been met, then 14W becomes conductive and turns 15. Since 25W and 28W have both been reset (see Section 16*b*, Item 39), when 15W is returned by the next AP pulse it turns 25W so that the b signal is dropped. One AP pulse cycle later, 28W is turned and the a signal is produced, as in Section 16*b*, Item 14. The return of 15W also brings about the production of the new signal SCM. Just as in the first sequence run (Section 16*b*), the al signal is produced under control of the SCM signal. Also, new OCO and PS signals are produced to time the piloting of new entries into electronic storage and to time the beginning of the new scanning sequence (Section 16*b*, Item 21).

The signal AT is given when all the transmissions from electronic storage into the selected

receiving means have been safely completed. The signal AT accomplishes the following:

It starts the AT delay counter (Fig. 75*b*) which, after some 16 ms. produces the signal ATD. This signal returns 21X (Fig. 78*j*) to allow the new presense signals SPR and NPR to be produced if the other three conditions, those for producing signals OCO and PS, also have been met (see Section 16*b*, Items 21, 38, and 39).

The signal AT this time causes trigger 3, Fig. 75*c*, to be reset from the status to which it was turned by the signal AT in the preceding run (see Section 16*b*, Item 37). With 3, Fig. 75*c*, reset, it causes relay Y1 to be dropped and relay X1 to be energized, as in Section 16*b*, Item 3. Relays Y1 and X1 are the heating relays for the B and A sides, respectively, of the In sequence storage circuits. Since the transmissions into the receiving means selected by the B side has been completed and since the A side is now set according to the In data in the next line of sequence data, the relay Y1 is dropped as stated above and the relay X1 energized.

To recapitulate, a new commutator run is started when: (1) the all-entry delay signal AED has been given, manifesting that all the entries into electronic storage as called for by the active line of sequence data have already been safely made; (2) when the scanning sequence has been completed, and (3) when the sequence data called for by the active line of sequence data in one side of sequence storage have been safely entered into the alternate side of sequence storage, as manifested by the delay signal STRD1. Preparation is thus made for operation to be performed during a new commutator run, as directed by the Out fields and the S1 and S2 fields in the new line of sequence data. The signals SCM, OCO and PS are produced. The signal SCM starts the Ink delay in Fig. 78*c* and causes the pilot units selection trees to be heated on the proper side. The signal PS starts the new scanning sequence. The signal OCO allows the entry signals Out to ES to be produced by selected pilot units. However, such selected pilot unit must also receive a Forward signal and must not be storing a transmission condition arising from the preceding line of sequence data. If a pilot unit is still in a transmission storage condition, its signal TR.Ink is still effective to prevent the pilot unit from producing the signal Out to ES.

During the new scanning sequence, the "1" signals from the accummulator spots conditioned for OC steps will be successively applied to the selected pilot units to cause them to produce their signals ES to Int. However, such signal will be blocked until the entry from the Out bus-set into the electronic storage unit, both associated with the pilot unit have been completed. Also, the signal Int to ES will be blocked if the pilot unit is still in a transmission storage condition.

It is seen, then, that all transmissions called for by a line of sequence data do not have to be completed before a new commutator run is started. During the new run, entries may be made into electronic storage from Out bus-sets and from electronic storage to the Internal buses. But until some 16 ms. after the AT signal has been produced to signal that all transmissions have been made as called for by the preceding line of sequence data, the transmissions called for by the next line of sequence data will not be made because this requires new NPR and SPR signals. These signals cannot be produced until the ATD signal has been given. Meanwhile, a new commutator run may start and operations, including a calculation, called for by Out fields and an OP field of new line of a sequence data, may take place.

17a. Re the second real line of sequence

Suppose the second real line of sequence data entered in the A side in the preceding run (Section 17) is:

S1Seq

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
2	1	012	2	2	013	1	3	030	0	01	01

S2Seq

Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
0	5	121	1	4	151	4	1	122	0	01	02

The code number 01 in field OP2 characterizes field T as an In field (see Sections 2*a* and 11). This code number in fields OP1 and OP2 also called for accumulation to be effected with the field T serving as an In field.

The interpretation of the fields P, Q, R, SH1, OP1, T, SH2 and OP2, in the above line is as follows. A number is to be taken from relay storage unit 012 (Pr) and applied to Out bus-set 1 (Pb) and to be handled without a change in sign (Ps=2). A second number is to be taken from relay storage unit 013 (Qr) and applied to Out bus-set 2 (Qb) to be handled without a change in sign (Qs=2). A third number is to be read out of relay storage unit 030 (Rr) to Out bus-set 3 (Rb) to be handled with a change in sign (Rs=1). These numbers are to be successively entered in the accumulator unit, as instructed by the code number 01 in field OP1. The accumulated result and sign are to be transmitted to relay storage unit 121 (Tr) by way of In bus-set 5 (Tb). The code number 01 in OP2 is to maintain the accumulator control commutator ACC.C (Fig. 78A) conditioned and also characterizes field T as an In field. No column shift is to take place of the accumulated result, since the fields SH1 and SH2 are blank and since the subfield Ts has no control over the shift amount and, hence, is left blank when T is an In field. Half correction of the accumulated result is to be suppressed.

The interpretation of fields U and V, in conjunction with OP2 and SH2, in the second real line of sequence is:

The number in relay storage unit 151 (Ur) is to be routed via electronic storage unit ES4 (Ub) to the accumulator (01 in OP2) and the minus operational sign (1 in Us) is to be applied to the sign mixing circuit of the accumulator. The number, changed in sign, is to be transmitted via the denominational shift unit, without column shifting (Vs=4 and SH2=0), and via ES1 (Vb) to relay storage unit 122 (Vr).

The code numbers 01 and 02 in S1 and S2 of the second real line of sequence are the same as considered in the first run of sequence (Section 16) and will not be discussed in the present section.

As described at the end of the preceding section the signal "*a*" has been produced. In the manner described in Section 16*b*, Item 15*a*, the "*a*" signal acts through the control frame to cause the A sides of the operational sign and In code circuits (Figs. 60 and 61) to be heated. Since T is an In field, heating of the T branches of the operational sign circuits is not effected, while the A side of the T branch of the In code circuit is heated. The heating of the T branch causes the tree signal TIC to be produced. This signal cuts off 21, Fig. 78*b*. Subsequently the

Ink signal is produced and cuts off 21*a*, whereupon the tube 22 conducts and reverses 23, causing 24 to produce the positive signal T "in." Also, as V is an In field, the signal V "in" is given at Ink signal time (see Section 17, Items 9 and 14*a*). These signals remain in effect until the FC signal occurs at the end of the scanning sequence. The signals T "in" the V "in" condition spots T and V (Figs. 78*f* and *h*) for IC steps, by turning their triggers 5 and by blocking the turning of their triggers 23.

Also, the signal T "in," which is positive, has the special function of maintaining tube 3P (Fig. 78*c*) conductive, so that the signal HCR will not be given when the signal FR is produced at the end of the ROC step. The signal HCR if produced, would reset the trigger 5, Fig. 71*g*, from its half correction suppression condition (see Sections 17, Item 14), and this is not to be done for the second half of the scanning sequence in the present commutator run, for reasons explained later.

As described in Section 16*b*, Item 15*b*, the signal "*a*" also causes the A sides of the pilot units of the selection trees (Figs. 54 to 58) to be heated.

Also as described in Section 16*b*, Item 16, the *a1* signal is produced for causing heating of the A sides of the shift code circuits (Figs. 62 and 63) and of the A side of the OP1 pyramid (Fig. 59).

Heating of the OP1 pyramid results in the presence of decreased potential on line OPO1. Consequently, 19, Fig. 77*a*, is cut off causing 20 and 20*a* to conduct. With 20 conductive it acts through 30 and 24 to produce the signal ACC Code. This signal, as explained in Section 17, Item 13, conditions tube 2 of the commutator ACC.C (Fig. 78A). Also, with 20*a*, Fig. 77*a*, conducting, it applies decreased potential to the wire HCS*w*. Consequently, the signal HCSS is produced (see Figs. 77*b* and 78*a*).

The Ink signal occurs about ½ ms. later and completes the conditioning of the commutator ACC.C (Fig. 78A), in the manner described in Section 17, Item 14*c*. The Ink signal also mixes with the signal HCSS to cause the couple 30—39*a* in Fig. 78*a* to produce the half correction suppression signal HCS (see Section 17, Item 14*d*). Also, the Ink signal completes the condition for production of the signals T "in" and V "in" as previously described.

Entries from the selected Out bus-sets into the related electronic storage units from the sources selected by the Out fields occurs in the same manner as described in Section 17, Item 15*a* and *b*.

Briefly, the OCO commutator signal is mixed with Forward signals to cause the pilot units 1, 2, 3 and 4 to produce their respective signals Out to ES to pilot the numbers from relay storage units 012, 013, 030, and 151 to electronic storage units 1, 2, 3, and 4, respectively.

The pilot unit 1 will be effective for producing the entry signal Out to ES1 provided that the transmission called for by the R field of the preceding line of sequence has been completed (see Section 17, Item 24). The R field in the preceding line of sequence called for transmission to be piloted by pilot unit 1 into relay storage unit 030. If this transmission has not yet been completed, the signal TR Ink will still be effective to pilot unit 1 to hold 33*a*, Fig. 80*a*, conductive, so that 32 will be deconditioned and the trigger 25 will not be able to return and cause the signal Out to ES1 to be produced. When the transmission called for by the R field in the preceding line of sequence has been completed the interlock signal TR Ink in pilot unit 1 no longer blocks the production by this pilot unit of the entry signal Out to ES1.

The pilot unit 3 will not function to produce the entry signal Out to ES3 in this particular example unless the signal AT has been given to indicate that all the transmissions called for by the preceding line of sequence have been completed. In this instance the blocking of pilot unit 3 results from its failure to receive a Forward signal from the relay storage unit 030 selected by subfield R*s* of the present line of sequence. The R field of the preceding line of sequence called for transmission into the relay storage unit 030. Accordingly, the unit in 030 has been operated and has shifted its contacts *bs* (note Fig. 29). If the signal AT has not been produced, then the heating relay Y7 for the IN sequence storage circuits is still in energized status and therefore the Unit In 030 is still in operating condition and maintaining its points *bs* shifted. Even though transmissions called for by the preceding line of sequence have not been completed, the Out sequence storage circuits may be heated, as described in the last part of Section 17, and so unit Out 030 may be in operating condition and closing its contacts *fs*. Even though these contacts are closed, and the contacts *fs* of the selected group Out also are closed, the Forward signal circuit may not be established if the contacts *bs* of Unit In 030 are still in shifted condition. When the transmission complete signal AT has been given, the heating relay Y7 is dropped and the relay X7 is energized, as described in the last part of Section 17. When the relay Y7 is dropped, unit In 030 is deenergized and its contacts *bs* return to normal condition, allowing a Forward signal to be applied from relay storage unit 030 to the pilot unit 3 selected by subfield R*b* of the present line of sequence. Pilot unit 3 may then function under further control of the OCO signal to produce the entry signal Out to ES3.

Similarly, a Forward signal will not be applied to pilot unit 4, selected by subfield U*b* in the present line of sequence, if the signal AT relating to the preceding line of sequence has not been given and has not yet caused relay Y7 to be dropped so as to allow Unit In 151 selected by V*r* of the preceding line of sequence to be deenergized.

The signal PS given at the same time as the signal OCO initiates the new scanning sequence. This may be done even though the signal AT relating to the preceding line of sequence has not yet been given, for reasons explained in the last part of Section 17. During the new scanning sequence the P1 signal is produced and causes the selected operational sign to be applied to the sign mixing circuit of the accumulator (see Section 17, Item 16*a*). The P1 signal also causes selected pilot unit 1 to produce signal ES1 to Int provided entry into ES1 from selected relay storage unit 012 has been completed (see Section 17, Item 16*b*). If the transmission called for by field R in the preceding line of sequence has not yet been completed, pilot unit 1 will still be producing its signal TR Ink. The trigger 25, Fig. 80*b*, in pilot unit 1 will have been turned under control of the signal OCO or the Forward signal. With the turning of 25, Fig. 80*b*, the trigger 21, Fig. 80*a*, will be turned (see Section 16*b*, Item 25)

and will make 15a conductive so as to block the ES1 to Int signal and the Pil.OC signal (see Section 17, Item 16b). As long as the interlock signal TR Int is effective, it prevents return of 25, Fig. 80b, so that the signal Out to ES1 will not be produced, and the trigger 21, Fig. 80a, will not be returned and will not release the pilot unit for producing the signal ES1 to Int or the signal Pil.OC. Only after both the transmission selected by a field in the preceding line of sequence to be piloted by a pilot unit, and the entry into electronic storage selected by a field in the next line of sequence to be piloted by the same pilot unit have been completed, is the signal OC Int in the pilot unit effective to allow the pilot unit to produce its signal ES to Int.

Concurrent with the production of the signal ES1 to Int by pilot unit 1, the pilot unit produces the signal Pil.OC. This signal, in a manner described in Section 17, Item 17a causes 21Q (Fig. 78d) to turn and to produce the signal OP.OC. Signal OP.OC causes the conditioned commutator ACC.C (Fig. 78A) to function for producing the signals ECC, RCC, and ACC–RI, so that the number from the source selected by the P field is transferred from electronic storage unit 1 to the entry tubes of the accumulator unit. One AP pulse after the termination of the entry, signal ACC–ST occurs causing the accumulator cycle to ensue so that the number is entered into the accumulator registers RC (Fig. 70). The cycle complete signal CYCPT acts upon commutator ACC.C to cause it to produce the signal OP.BC. This signal returns 21Q, ending the P OC step and initiating the Q OC step (see Section 17, Item 17b).

During the Q OC step, the signal Q1 is produced and causes the second number to be read out from electronic storage unit 2 to the Internal buses under control of the signal ES2 to Int. Concurrent with the latter signal pilot unit 2 produces the signal Pil.OC which causes the trigger 21R (Fig. 78e) to turn. The turning of trigger 21R produces another OP.OC signal. As a result, the conditioned commutator ACC.C again operates to cause the second number to be received by the accumulator unit and a second accumulator cycle to take place for transferring this second number to the registers RC to be accumulated with the first number. At the end of the cycle the commutator ACC.C is again operated to produce the signal OP.BS. This signal now returns 21R thus terminating the Q OC step and initiating the R OC step. During the OC step of the R spot the signal R1 is produced and causes the selected pilot unit 3 to produce the signal ES3 to Int. This pilot unit thereupon produces the signal Pil.OC which causes the trigger 21T (Fig. 78f) to turn. As 21T turns it produces the third signal OP.OC which caused the commutator ACC.C to produce the signals for effecting the entry of the third number into the accumulator to be accumulated with the other two numbers in registers RC. At the end of the third accumulator cycle the commutator ACC.C is again operated to produce the signal OP.BS which this time returns 21T, causing the R OC step to terminate and the IC step of the T spot to begin.

The return of 21T ends the R OC step by causing 23 R to return (see Section 16b, Item 26R). Signals FR is produced by the return of 23R (see Section 16b, Item 26–1). This signal causes the a1 signal to cease and the a2 signal to appear. Signal a2 heats the OP2 pyramid (Fig. 59). As this pyramid is set at 01, the signal ACC code again is produced and applied to the commutator ACC.C (Fig. 78A). The signal HCSS also is produced, as before. Signal FR also turns 5P (Fig. 78c) to initiate the Ink signal delay.

When 5P turns, it cuts off 3a but since signal T "in" is maintaining 3 conductive, the signal HCR is not produced and does not reset the trigger 5, Fig. 71g (Section 17, Item 12) which remains in turned, half correction suppression status in which it was placed for the first half of the present scanning sequence. The reason for blocking the signal HCR at the beginning of the second half of the scanning sequence, when T is an In field is explained below.

Upon the return of 21T, it not only reset 23R to cause signal FR to appear, but it also turned 22T to cause the turned trigger 5T to be restored. The restoration of 5T reversed 6T, causing signal OP.IC to appear (see Section 17, Item 20). Since commutator ACC.C (Fig. 78A) still is conditioned at this time, it responds to the signal OP.IC and produces the signal R.ROC. This signal initiates the sign test of the accumulated result. If trigger 5, Fig. 71g, had been allowed to return, the sign test would have initiated the half correction procedure described in Section 13, but this procedure is not called for when the accumulator unit is used and T is an In field. Signal HCR therefore is not produced in this run when 5P (Fig. 78c) is turned by signal FR because the positive signal T "in" is effective to block the signal HCR. Trigger 5, Fig. 71g, therefore remains in turned state and suppresses the half correction procedure.

The sign test initiated by signal R.ROC causes signals ACC–RO and Proceed to appear at once if the sign is positive; but if the sign is negative, then the complement conversion procedure intervenes (Fig. 73).

The Proceed signal initiates operation of counter 33, 34 and 35 in ACC.C (Fig. 78A) by turning 33 (see Section 17, Item 20). The turning of 35 occurs two AP pulse cycles after the Proceed signal. If the Proceed signal follows the detection of a positive sign in the accumulator, the turning of 35 occurs two AP pulse cycles after signal R.ROC which is concurrent with signal FR, in this sequence run. If the Proceed signal follows the complement conversion procedure, the turning of 35 occurs more than two AP pulse cycles after signal FR. The signal FR has initiated the operation of the Ink delay counter (Fig. 78c) by turning 5P. One AP pulse cycle later, 5 P is returned and signal ACCL appears (see Section 17, Item 22) and deconditions ACC.C. One AP pulse cycle later, the signal Ink is produced. Since signal ACC Code has since been reapplied to ACC.C, signal Ink reconditions ACC.C. The turning of 35–ACC.C occurs at the same time or later for reasons explained above. By then ACC.C has been reconditioned, so upon the turning of 35, it produces signal OP.BS. One AP pulse cycle later 35 is returned and resets 14, so as to prepare ACC.C to produce signal RCC.

The signal OP.BS this time causes 6T (Fig. 78f) to be reset and thereupon to turn 11T. Signals CSI, SHCL, SHRI and SHS are then produced in the manner described in Section 17, Item 22. These signals cause the accumulated result, now applied to the Internal buses by signal ACC–RO to be entered in the denominational shift unit, and in the sign storage triggers 2M and 6M in Fig. 78a, and the denominational

shift unit to perform the selected number of shift steps. The denominational shift unit then produces the complete signal SHCP which goes to the N spot (Fig. 78b) and initiates operations leading to production of readout signals SHRO and SHRD. These signals cause the denominational shift unit and the sign storing triggers to apply the accumulated result and sign to the Internal buses.

One AP pulse cycle after production of the readout signals SHRD and SHRO, signal CSV appears and returns 11T (Fig. 78f) causing 15T to turn. This results in production of signal T2. Signal T2 renders selected couple 45—45a in 5CP (Fig. 80e) of pilot unit 5 effective through 44a, 41 and 33 to produce signal IC Int in this pilot unit. As in Section 17, Item 23a, pilot unit 5 then produces signals ESC5 and Int to ES5, so that the number and sign on the Internal buses is entered in ES5. At this time, pilot unit 5 also causes signal Pil.IC to appear, and this signal is followed by signal Pil.ICC which resets 15T.

Upon return of 15T, it turns 16T for one AP pulse cycle. The turning of 16T causes signal CSF to appear and terminate the readout signals SHRO and SHRD, as in Section 17, Item 23b. The turning of 16T also brings about the production of signal T3. Assuming that selected relay storage unit 121 has applied a Back signal to selected pilot unit 5 and that a presense signal has been produced, the signal T3 completes the conditions for transmission of the accumulated result, with sign from ES5 to relay storage unit 121.

The accumulation of the numbers from sources selected by Out fields P, Q, and R has been completed and the accumulated result has been entered in the unit selected by In field T.

The trigger 16T (Fig. 78f) which was turned to produce signal T3 is reset by the next AP pulse and turns 19T for one AP pulse cycle. The turning of 19T causes signal T.IC to appear. Since the U spot (Fig. 78g) is not conditioned for an IC step, 18U is conditioned to respond to signal T.IC and to turn 23U. Signal U1 is produced and causes selected pilot unit 4 to produce the signal ES4 to Int, so that the number and sign which has been sent from selected relay storage unit 151 into ES4 is now applied to the Internal buses. Also, the operational sign 1 is applied to the sign mixing circuit of the accumulator. A Pil.OC signal is produced by pilot unit 4 and is followed by the signal Pil.OCC which causes conditioned 24U to produce signal U.OC which turns 21V. As 21V turns, it produces the signal OP.OC which causes conditioned commutator ACC.C to issue the signals ECC, RCC, and ACC–RI, as in Section 17, Item 17a. The number derived from selected storage unit 151, and now on the Internal buses is entered in registers EC (Fig. 70) and the sign of the number is entered in the sign mixing circuit to be mixed with the operational sign. Commutator ACC.C then produces signal ACC–ST and an accumulator cycle ensues in which the true number or its complement is transferred from EC to RC depending on whether the mixed sign is + or — (see Section 13). The cycle complete signal is given and causes ACC.C to produce signal OP.BS which, this time, resets 21V. Since the V spot is conditioned for an IC step, the return of 21V causes 5V to reset. Just as in Section 17, Item 26, the V IC step controls the transfer of the accumulated result to the denominational shift unit, the initiation of operations of the shift unit, the transfer of the shifted result to the selected electronic storage unit and the transmission of the result to the selected relay storage unit 122.

The accumulation of three numbers has been described in this section. It is evident that five numbers may be accumulated in a commutator run by using fields P, Q, R, T and U as Out fields and V as the only In field.

It should be noted that in the preceding run (Section 17), an accumulation called for by the S2Seq portion of the first real line of sequence was carried out. The accumulated result was transmitted to relay storage unit 151. Now, in the present run, the accumulator unit was used to receive the number from relay storage unit 151 and to apply it with inverted sign to relay storage unit 122. The result now is in both relay storage units 151 and 122, with the result sign in one being opposite the sign in the other unit. Thus a single quantity in a unit may be put, by several commutator runs, into a plurality of units and the sign of the quantity may be different in each receiving unit.

When a quantity in one unit is to be transmitted, with or without column shifting, to a plurality of units and to stand with the same sign in each unit, a single commutator run may be used. The next section explains such run.

17b. *Inserting result into plurality of units in one run*

Suppose the following line of sequence to be in sequence storage to be acted on in the present run.

S1Seq

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
2	1	010	7	2	011	5	3	012	0	01	01

S2Seq

Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
0	4	013	6	5	014	6	6	015	5	01	02

Code number 01 in OP1 and in OP2 calls for accumulation without half correction and the number in OP2 also characterizes T as an In field, as in the preceding section.

In the above line of sequence, P is the only Out field. The fields Q, R, T, U and V are In fields. The digit 7 in Qs not only characterizes Q as an In field but also calls for a denominational shift to the left of ten places, to be effected during the first half of the commutator run. The digit 5 in Rs characterizes field R as an In field and also confirms the instruction given by Qs for performing a shift to the left. The digit 6 in Us characterizes U as an In field and calls for a shift of ten places to the right to be effected during the second half of the commutator run. The digit 6 in Vs designates V as in an In field and also calls for a shift to the right of ten places. The digit 5 in SH2 calls for a shift of five places. The total shift to be effected during the second half of the commutator run is therefore fifteen places to the right.

Briefly interpreted, the above line calls for a number from relay storage unit 010 to be transferred, by way of the accumulator, to the denominational shift unit to be shifted, during the first half of the run, ten places to the left and then same number transmitted to both the relay storage units 011 and 012. During the second half of the run, the number in the denominational shift unit is to be shifted fifteen places to the right and then transmitted to each respectively of the relay storage units 013, 014 and 015.

Only operations which are of particular con-

cern to an understanding of the present run will be described here in detail.

The manner in which the pilot units are selected, and relay storage units are conditioned to send and receive quantities is described in preceding sections and need not be re-explained. The manner in which the commutator spots Q, R, T, U and V are conditioned for IC steps is also clear from Section 17, Items 9 and 14a and from Section 17a.

The manner in which the denominational shift unit is conditioned for performing a shift to the left and the manner in which the shift amount of 10 is designated on the lines MN (Fig. 78a and Fig. 77a) are clear from Section 17, Item 11. The commutator ACC.C (Fig. 78A) is conditioned in the same way as described in the preceding section.

Just as in Section 17, Item 1 and 15b, the signal OCO and the Forward signal combine to cause the selected pilot unit 1 to pilot the quantity from selected relay storage unit 010 into ES1.

The OC step of the P spot (Fig. 78c) occurs and the signal P1 acts as in Section 17, Item 16b, to cause the quantity in ES1 to be applied to the Internal buses. The Pil.OC signal is given and turns 21Q (Fig. 78d), as in Section 17, Item 17a. This produces signal OP.OC to initiate operation of commutator ACC.C (Fig. 78A) for bringing the quantity on the Internal buses into the accumulator unit and causing the accumulator cycle to ensue.

Briefly, the signal OP.OC causes conditioned 10–ACC.C to conduct and turn 14, 18 and 22 and to return 26 which has been left turned by a previous run of accumulator sequence (see, for instance, Section 17, Items 17a, 19 and 20). The return of 14 effects reversal of 15 so that the signal RCC is produced. The turning of 18 serves to produce the signal ECC. The turning of 22 causes the signal ACC–RI to be produced. The next AP pulse resets 18, turning 17. The following AP pulse returns 17 in order to reset 22. Upon 22 being reset it turns 21. The next AP pulse resets 21 causing it to turn 25. Upon 25 being returned it produces the start signal ACC–ST. The signals RCC and ECC via 71f and 71e and 71a cancel the registers RC and EC (Fig. 70). The signal ACC–RI causes the quantity now on the Internal buses to be entered into registers EC. The signal ACC–ST initiates an accumulator cycle during which the number is transferred from EC to RC. At the end of the accumulator cycle the signal CYCPT goes to ACC.C (Fig. 78A) and renders 28—28a effective to operate at AP pulse time to restore 25, ending the signal ACC–ST. The return of 25 turns 26 which causes 27 to turn and produce the signal OP.BS.

This signal via Figs. 78c and 78d returns 21Q (Fig. 78d) so as to end the P OC step and initiate the Q IC step. Briefly, the return of 21Q causes 22 to turn for one AP pulse cycle. Upon return of 22 it restores 5 which causes 6 to turn. The turning of 6 produces the signal OP.IC which renders conditioned 11–ACC.C (Fig. 78A) conductive to reverse 23. Reversed 23 cuts off 24. As tube 24a is still cut off under control of 26 turned by the signal CYCPT given during the P OC step, the couple 24—24a becomes effective, to turn 30 so as to produce the signal R.ROC. Under control of this signal the accumulator unit functions to produce the signals ACC–RO and the Proceed signal. The quantity in the accumulator unit is now applied to the Internal buses. The proceed signal initiates the operation of the counter 33, 34 and 35 in commutator ACC.C. When trigger 35–ACC.C turns it causes the signal OP.BS to be produced (see Section 17, Item 22). One AP pulse cycle later 35 returns and resets 14 and 30. The resetting of 30 ends the R.ROC signal. The resetting of 14 allows signal RCC to be produced when a next accumulating sequence is called for. The return of 14 also has a special function in the present run, as will be made clear.

The signal OP.BS which was produced when 35–ACC.C turned is effective to restore 6Q, causing it to turn 11Q (Fig. 78d).

Briefly, the turning of 11Q causes signal CSI to appear. This turns 2N and 3N in Fig. 78b. 3N is returned by the next AP pulse and turns 1N which is reset by the next AP pulse and restores 2N. When 2N is turned, it causes signal SHRI to appear and enter the number, now being applied to the Internal buses under control of signal ACC–RO, into the denominational shift unit. The signal SHRI also causes the sign of the number to be stored in 2M or 6M in Fig. 78a. 3N (Fig. 78b) was turned at the same time as 2N and cut off 14a. Tube 22N also is at cut-off and 14a–22N now functions to cause signal SHCL to appear. This signal resets that sign storage trigger 2M or 6M which is not being held turned under control of the conducting one of the tubes 3M and 7M. The signal SHCL also causes the instantaneous signal ACL to appear and reset those triggers ASH (Fig. 24) which are not being held turned under control of the conductive input tubes IT. Thus, the number and its sign have been read out of the accumulator, the number has been entered in the denominational shift unit, and the sign has been stored in 6M or 2M (Fig. 78a).

When 2N (Fig. 78b) returns, it ends signal SHRI. This allows 8a, Fig. 78a, to turn 13M for one AP pulse cycle, giving the signal SHS. The denominational shift unit now shifts the number ten places to the left, as instructed by the shift amount 10 in the descending counter (Fig. 27a) and by the left-shift status of 21, Fig. 27c. For each step of shift, the number in the descending counter is reduced by 1, as described in Section 12. In the present case, the descending counter is brought to zero status at the tenth and last step. Upon completion of the shift, signal SHCP is produced by the denominational shift unit. Under control of this signal, 9N (Fig. 78b) is turned to cause the signal CSRD to appear at AP pulse time. This signal turns 7N and 10M. Turned 10M produces signals SHRD and SHRO, as described in Section 17, Item 22. Signals SHRO and SHRD cause the shifted amount and its sign to be applied to the Internal buses. 7N is restored after one AP pulse cycle and causes 8N to turn for one AP pulse cycle. Turning of 8N produces the signal CSV which restores 11Q, causing 15Q to turn, whereupon signal Q2 appears. The selected pilot unit 2 is controlled by this signal to produce signals Int to ES2 and ESC2, so that the shifted number and its sign now on the Internal buses are applied to ES2, in a manner clear from Section 17, Item 23a. The signal Pil.IC appears and is followed by signal Pil.ICC which resets 15Q, causing 15Q to turn for one AP pulse cycle. As 16Q turns, it produces signals Q3 and CSF. Signal CSF resets 10M to end the signals SHRD and SHRO. Signal Q3 causes selected pilot unit 2 to pilot the

quantity (including sign) from ES2 to selected relay storage unit 011, in a manner explained in Section 17, Item 24.

In brief, the quantity from relay storage unit 010 has been passed through the accumulator unit and then into the denominational shift unit where it has been shifted ten places to the left, after which the shifted number and its sign were transmitted to relay storage unit 011.

Upon the return of 16Q, it turns 19Q for one AP pulse cycle. When 19Q turns, it causes positive signal Q.IC to appear. This signal acts through 9R (Fig. 78e) to reset 5R. Note that in the scanning sequence covered in Section 17, 5R was reset under control of the signal Q.OC (see Section 17, Item 20). The return of 5R initiates the IC step of the R spot.

It is seen that the R IC step is to occur in this run, directly after the Q IC step. During the Q IC step a signal R.ROC was produced by ACC.C (Fig. 78A). This signal initiated operation of the accumulator unit to produce the signals ACC–RO and Proceed. Under control of signal ACC–RO the number in the accumulator unit was read out to the Internal buses. The Proceed signal initiated operation of ACC.C to produce the signal OP.BS and to reset 14–ACC.C. The signal OP.BS initiated operations for producing the signals SHRI and SHCL followed by the signal SHS. Accordingly, the number from the accumulator unit which was being applied to the Internal buses under control of signal ACC–RO was entered into the denominational shift unit and the number was then shifted ten places to the left. At the end of the shift the descending counter (Fig. 27a) was stepped back to 0. At completion of the shift the signal SHCP initiated operations for causing the shifted number to be read out of the shift unit, after which, it was transmitted to the selected relay storage unit 011. The Q IC step ended and the R IC step was initiated. It is desired in this run to transmit the same number from the accumulator unit, after it has been shifted ten places to the left, into relay storage unit 012 during the R IC step as well as into relay storage unit 011 during the Q IC step. It is not possible, however, to follow the same procedure for shifting the number from the accumulator during the R IC step as was followed during the Q IC step, and which procedure involves the clearing of the denominational shift unit, the entry of the number from the accumulator into the shift unit, and the performance by the shift unit of a shift of ten places as directed by the shift value 10 in the descending counter (Fig. 27a). This procedure cannot be followed during the R IC step because the descending counter has descended to 0 status as a result of the shift effected during the Q IC step. Therefore, in the R IC step, when it follows the Q IC step, it is necessary to retain the previously shifted number in the denominational shift unit and to transmit this shifted number from the shift unit into the receiving unit (012) selected by the subfield Rr. In order to retain the same shifted number in the denominational shift unit, two things are necessary. One is the suppression of the shift unit cancel control signal SHCL, and the other is the suppression of the accumulator readout signal ACC–RO. If these two signals are not suppressed, then the previously shifted number would be cancelled from the shift unit and the number from the accumulator unit would be entered in unshifted relation into the shift unit. Since the descending counter is now at 0, shift steps would not occur and the unshifted number would be transmitted to the unit (012) selected by subfield Rr. If the signal SHCL were not suppressed and the signal ACC–RO were suppressed, then the shift unit would be cleared and a number would not enter the shift unit. If the signal SHCL were suppressed and the signal ACC–RO were not suppressed, then the number from the accumulator unit would enter the shift unit and mix with the shifted number to produce a haphazard number. It is seen, therefore, that both the cancel signal SHCL and the readout signal ACC–RO must be suppressed when the R IC step follows a Q IC step.

The R IC step was initiated by the return of 5R (Fig. 78e). Upon the return of 5R, it turned 6R, as a result of which the signal OP.IC is produced. This signal causes 11–ACC.C (Fig. 78A) to turn 23 which cuts off 24. The trigger 26 still is in turned status, having been set in this status under control of the signal CYCPT, last given during the P OC step. Since a signal OP.OC has not followed, 26 has remained in turned state and has continued to cut off 24a. Previously, in the Q IC step, when 24—24a was cut off it produced the signal R.ROC. This signal caused the accumulator unit to produce the signal ACC–RO. Under control of this signal the number in the accumulator unit was applied to the Internal buses. Also, concurrently with the signal ACC–RO, the signal Proceed was applied to ACC.C to initiate the operations for continuing the scanning sequence. For the reasons explained above, it is desired during the R IC step to suppress the signal ACC–RO. Accordingly, it is necessary to suppress the signal R.ROC.

During the Q IC step the Proceed signal initiated the operation of counter 33, 34 and 35, in ACC.C. This resulted in the return of 14–ACC.C, as well as in the application of the signal OP.BS to the scanning spots of the commutator. With 14 in its reset state it is maintaining 19a conductive. Now, in the R IC step, 24—24a has been completely cut off but as 19a is conductive, the common anode line of 19a, 24 and 24a does not rise in potential. Consequently, 30 does not turn, so that signals R.ROC, ACC–RO and Proceed are suppressed.

It is seen then during the first IC step a signal OP.IC is effective to cause ACC.C to produce R.ROC. A Proceed signal then returns to ACC.C and causes 14 to return and a signal OP.BS to be issued for initiating the next scanning step. If this next step is also an IC step, then the signal OP.IC is next produced and has the effect of turning 23 but inasmuch as 14 has been reset, the signal R.ROC is not issued.

With 14 now reset, it also cuts off 13. With 23 now turned under control of the OP.IC signal, it also cuts off 13a. The couple 13—13a is then effective to cause 9 to produce a negative signal SHNC. Also, couple 13—13a causes 9a to act through the anode resistor of 36 to turn 33. The turning of 33 initiates the operation of the counter of 33, 34 and 35 in ACC.C. Thus, the action of couple 13—13a in this instance substitutes for the Proceed signal in initiating the operations for continuing the scanning sequence. Upon the return of 33 it resets 23 but meanwhile the signal SHNC has been produced and cuts off 28a (Fig. 78a). As 28a is cut off, it renders 28 effective to turn trigger 24M. With 24 turned, the line 24m rises in potential and renders 22a, Fig. 78b, conductive. As a result, the couple 14a and 22a will be ineffective to cause 6 to conduct and produce the signal SHCL.

In the manner explained before, the trigger 35–ACC.C is turned two AP pulse cycles after the turning of 33, and acts through 31*a*, and 7*a* and 3 to produce the signal OP.BS. This signal now resets 6R (Fig. 78*e*) which thereupon reverses 11R. The reversal of 11R causes the reappearance of signal SHI which turns 2N and 3N in Fig. 78*b*. The turning of 2N causes signal SHRI to appear but inasmuch as a number and sign have not been applied to the Internal buses, the denominational shift unit will not receive a new number in response to the signal SHRI nor will a new sign be applied to the storage triggers 2M and 6M in Fig. 78*a*. During the first IC step which followed an OC step the turning of 3N was effective, by cutting off 14*a*, to cause the cancel signal SHCL to appear. This signal, if allowed to appear during the second of two successive IC steps, would cancel the shifted number in the denominational shift unit. For this reason the trigger 24M (Fig. 78*a*) has been turned, under control of the OP.IC signal produced at the start of the second IC step and thereby has rendered 22*a* conductive to prevent the signal SHCL from being produced. Accordingly, the number which has been shifted ten places to the left during the Q IC step is left undisturbed in the denominational shift unit during the R IC step.

When 2N returns, signal SHRI ends and 8*a*, Fig. 78*a*, conducts and turns 13M, giving out the signal SHS. The latter signal initiates operation of the denominational shift unit. Since the number in the descending counter has been reduced to 0 in the Q IC step, the shift unit immediately produces the signal SHCP. This signal causes 9N to turn and produce signal CSRD at AP pulse time. Signal CSRD causes 7N and 10M to turn. Upon 10M turning, it produces the readout signals SHRD and SHRO. The denominational shift unit now applies the shifted number to the Internal buses and the sign storage triggers 2M and 6M apply the sign of the number to the Internal bus columns 1. Trigger 7N is reset by the next AP pulse and turns 8N for one AP pulse cycle. Upon the turning of 8N, it produces signal CSV which resets 11R, causing 15R to turn and produce signal R2. The shifted number and its sign now on the Internal buses is entered under control of signal R2 into ES3.

The turning of 15R also produces signal FR (see Section 17, Item 22). Signal FR ends the heating of the SH1, Q, and R shift code sequence storage circuits (Figs. 62 and 63) and of the OP1 pyramid (Fig. 59) and initiates heating of the SH2, U and V shift code circuits and of the OP2 pyramid. Accordingly, the shift value 10 on lines MN (Figs. 78*a* and 27*a*) and the shift direction on line LT are removed and a new shift number and direction applied to these lines; also the code number 01 in OP2 is translated into a repeat issue of signal ACC Code. The new shift number is 15, since the code number in SH2 is 5 and the number 6 is in Us and in Vs. The new shift direction is a direction to shift to the right since the number in Us and Vs is 6. Therefore, at this time, the lines MN1, 4 and 10 and the line RT are placed at increased potential for the second half of the sequence run. The signal FR also initiates operation of the Ink delay in Fig. 78*c*. As 5P, in the Ink delay, turns, it cuts off 3*a*. But 3 is now conductive, since signal T "in" is in effect, whereby signal HCR is suppressed. This is of no moment in this case, when the R and T spots perform IC steps in succession, but is necessary when R performs an OC step and T and IC step, as in Section 17*a*. The return of 5P causes signal ACCL to appear and decondition ACC.C.

The Ink signal is given, two AP pulse cycles after initiation of the Ink delay by FR, and causes entry of the new shift number 15 into the descending ciunter (Fig. 27*a*) and the placing of 21, Fig. 27*c*, in right-shift state (see Section 17, Item 14b). The Ink signal also reconditions ACC.C (see Section 17, Item 14*c*).

When pilot unit 3 produced signal Int to ES3 for causing the left-shifted number and its sign to enter ES3, the pilot unit also produced signal Pil.IC. This is followed by signal Pil.ICC which resets 15R, causing 16R to turn and produce signals R3 and CSF. Signal CSF, via 11*a* and 11 in Fig. 78*a*, resets 10M, ending the SHRD and SHRO signals. The negative pulse from 11 also resets 24M which was turned before to suppress cancel signal SHCL.

The turning of 16R also produces signal R3 which controls pilot unit 3 to send out signal ES3 to In (see Section 17, Item 24), whereby the quantity in ES3 is transmitted to relay storage unit 012.

In the first half of the run, a quantity from 010 was entered in the accumulator and transferred therefrom to the denominational shift unit, where it was shifted ten places to the left. The purpose of such shift, as is clear from Section 12 is to produce for transmission to storage a shifted number which results from dropping the ten left-hand digits of the original number. Assume the original number has nineteen digits, so its 19th place enters shift column 19 and its 1st place enters shift column 1. A shift of ten places to the left brings the 1st place digit into shift column 11 and the 18th place digit into shift column 28, so that the 19th place digit is lost. The 9 right hand numbers of the original 19 digit number now in shift columns 19 to 11 are then transmitted to columns 2 to 10 of relay storage units 011 and 012 during the Q IC and R IC steps.

When the 18-place number in shift columns 28 to 11 is later shifted 15 places to the right, the five right-hand digits are dropped, leaving 13 digits standing in shift columns 1 to 13. This shortened number will be transmitted to relay storage units 013, 014 and 015 during the second half of the present program.

Trigger 16R, which turned to produce transmission control signal R3, is reset by the next AP pulse and causes 19R to turn and produce signal R.IC, as in Section 17, Item 25. Since spot T is conditioned for an IC step, signal R.IC causes 5T to return. This starts the T IC step which is similar to the R IC step, except for the production of signal FR which is a part of the R step only. Briefly, upon return of 5T, trigger 6T turns and applies signal OP.IC to ACC.C. As in the R IC step, signals R.ROC and ACC–RO and Proceed are suppressed; 24M is turned to suppress signal SHCL; but signal OP.BS is produced. The signal OP.BS resets 6T, causing 11T to turn. Signals CSI, SHRI and SHS are produced. Signal SHCL is suppressed, because 24M is turned, and the shift unit is not cleared. Signal SHRI has no effect because there is no number or sign now on the Internal buses. Signal SHS starts operation of the denominational shift unit to effect the fifteen steps of shift to the right for which the shift unit now has been conditioned. The completion of this shift is manifested by

signal SHCP which causes signals CSRD, SHRD, SHRO and CSV to follow. Signals SHRD and SHRO apply the newly shifted number and its sign to the Internal buses.

Signal CSV resets 18T, causing 15T to turn and produce signal T2. The number and sign on the Internal buses now is entered in ES4. The attendant signal PIIC causes 18T to return and reverse 16T. Signal T3 occurs and the quantity in ES4 is transmitted to relay storage unit 017.

The IC steps of the U and V spots occur successively in the same fashion as the R IC step described in this section except that the FR signal is not produced. Signal FR is a part of the R step only. The signal FC is produced at the end of the V spot and accomplishes the purposes outlined in the previous Sections 16b, 17, and 17a.

17c. *The tolerance check*

The general nature of the tolerance check was explained in Section 13. The tolerance check ordinarily serves for checking the accuracy of answers. It does this by determining whether two answers to a problem differ by more than a chosen tolerance. If the difference between the answers is within the tolerance, it indicates the answers are accurate to a desired limit and operation of the machine is continued. If the answer difference is greater than the tolerance, it indicates that at least one of the answers is wrong, and machine operation is interrupted. This answer tolerance check involves two successive comparisons, each made by the accumulator unit. The first comparison is between two answers to a problem and is made by obtaining the difference between the two answers. The answer difference is then cleared out of the accumulator and stored elsewhere. The second comparison is between the answer difference taken from storage, and a chosen positive tolerance number. For the second comparison, the absolute value of the answer difference is subtracted from the tolerance number. If the result sign of the second comparison is positive, a Proceed signal is sent to ACC.C (Fig. 73a) to continue the scanning sequence. If the second comparison result sign is negative, the Proceed signal is blocked and the scanning sequence halted. Since the scanning sequence is halted, one of the conditions for a new commutator run is not established, so machine operation is interrupted.

Basically, when the accumulator unit is conditioned for a tolerance check it allows machine operation to continue if at the end of the check the accumulator unit contains a positive sign, but if the accumulator unit contains a negative sign, then machine operation is interrupted. On this basis, the accumulator unit, when set for a tolerance check, may be used for other purposes than verifying the accuracy of answers to calculations. In fact, the column check means may be used for any purpose where a negative result in the accumulator unit is to cause machine operation to be interrupted while a positive result is to allow operation to continue.

An illustrative line of sequence ordering an answer tolerance check is given below:

S1Seq

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
2	3	016	1	2	137	4	1		6	02	02

S2Seq

Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
2	6	003	3	1		4			0	03	02

In the above line, it is assumed that relay storage units 016 and 137 contain two answers to the same problem. The tolerance number is positive and in dial storage unit #3, the code number for which is 603. The code number 02 in OP1 calls for accumulation without half correction (see Section 17). The code number 03 in OP2 calls for a tolerance check.

Briefly interpreted, the S1Seq portion of the above line calls for the answer in relay storage unit 016 (*Pr*) to be sent via ES3 (*Pb*) to the accumulator unit to be acted on without a change in sign (*Ps* is 2); for the answer in relay storage unit 137 (*Qr*) to be brought via electronic storage unit ES2 (*Qb*) to the accumulator unit to be subtracted (*Qs* is 1) from the answer previously entered in the accumulator unit; and for the difference between the two answers to be stored in electronic storage unit 1 (*Rb*). The S2Seq portion of the above line calls for the tolerance number to be read out of dial storage unit #3 (*Tr*) and via ES6 (*Tb*) to the accumulator unit to be handled without a change of sign; for the answer difference in electronic storage unit 1 (*Ub*) to be sent to the accumulator unit to have its absolute value subtracted from the tolerance number (*Us* is 3); and for the Proceed signal to be produced (*Vs* is 4) if the tolerance check (OP2 is 03) finds the answer difference to be equal to or less than the tolerance number.

Assume that the above line of sequence is in the side of sequence storage which is heated in preparation for a run about to take place. In a manner clear from Section 17, relay storage unit 016 (*Pr*) applies its number and sign to Out bus-set 3 (*Pb*) and a Forward signal to pilot unit 3. Also, the number and sign in relay storage unit 137 (*Qr*) are applied to Out bus-set 2 (*Qb*) and a Forward signal is applied to pilot unit 2. The T branch of the dial storage sequence storage pyramids selects relays DS–GO6 of dial storage unit #3, so that the tolerance number in this unit is applied to Out bus-set 6 (*Tb*) and a Forward signal is applied by way of bus 81 of this set to pilot unit 6, as explained in Sections 8 and 11. The heating of the In code sequence storage circuits (Fig. 61) causes the R and V branches to prepare for conditioning of the R and V commutator spots for IC steps.

The OC-Out to ES trees (Fig. 54) are heated through zero filtering (see Section 16b, Items 15b and 39). Since the subfields *r* of the P, Q, and T trees are not blank, the corresponding OC-Out to ES trees produce signals OCO3, 2, and 6 to be mixed with commutator signal OCO. The signal OCS in each of these pilot units will be produced and will combine with Forward signals to produce entries from Out bus-sets into ES3, 2, and 6, as called for by fields P, Q, and T. When an Out field is blank in its subfield *r* but has a significant digit in its subfield *b*, the field calls for a number to be applied by the designated electronic storage unit to the Internal buses. Such field does not call for entry via an Out bus-set into the designated electronic storage unit, and a Forward signal will not be applied to the corresponding pilot unit. If the OC-Out to ES trees were not heated through zero filtering, the tree corresponding to the Out field which is blank in subfield *r* but has a digit in subfield *b* would produce a numbered tree signal OCO to select a pilot unit. The selected pilot unit would respond to commutator signal OCO and its triggers 25, Fig. 80b, and 21, Fig. 80a, would be turned. Since this pilot unit will not receive a Forward signal, it would remain in entry interlock condition, in which 25, Fig. 80b, and 21, Fig. 80a, are turned. Accordingly, signal AE would remain blocked by

the pilot unit. Also, with 21, Fig. 80a, turned, it would block production of the signals ES to Int and Pil.OC by the pilot unit. The instructions given by the program field would not be carried out and the scanning sequence would be interrupted. For these reasons, the OC-Out to ES trees are heated through zero filtering. An example of an Out field which is blank in subfield r but has a digit in subfield b in the field U of the present program. The U tree of the OC-Out to ES group will not be heated because the U zero filter circuit remains open when Ur is blank. Accordingly, signal OCO1 will not be produced and signal OCO will not operate pilot unit 1 to place it in entry interlock condition.

The IC Presense trees (Fig. 55) also are heated through zero filtering. This is to prevent an In field which is blank in subfield r but not in subfield b from selecting a pilot unit to respond to presense signal NPR. If the designated pilot unit were allowed to respond to the presense signal, its trigger 30, Fig. 80c, would turn and block the signal AT. This trigger may be reset only at the end of the transmission delay. But since subfield r of the In field is blank, a Back signal will not be applied to the pilot unit named in the related subfield b. Accordingly, even if trigger 30, Fig. 80c, were turned, the lack of a Back signal will prevent the pilot unit from producing the transmission signal, and trigger 30 would remain in turned state, blocking signal AT. For this reason, the IC Presense trees are heated through zero filtering. In the present program, field R is an In field with a blank subfield r and with subfield b containing 1. The R tree of the IC Presense group is not heated because the Rr zero filter is in open condition. Accordingly, signal PRES1 will not be produced and pilot unit 1 will not respond to signal NPR. Trigger 39, Fig. 80c, of pilot unit 1 will not turn and block signal AT.

The IC–ES to In trees (Fig. 56) also are heated through zero filters. If this were not done, the tree set according to the digit in subfield b of an In field would select a pilot unit for response to the "3" signal from the related scanning spot even if the In field were blank in its subfield r. As a result, the trigger 20, Fig. 80c, of the pilot unit would turn and produce the signal TR Ink. This would disable the pilot unit from piloting entry into the electronic storage unit either from the Out bus-set or from the Internal buses (see Sections 17 and 17a) in a next commutator run. Since this pilot unit will not produce its transmission signal ES to In, its trigger 20, Fig. 80c, would not be reset and signal TR Ink would remain effective. The pilot unit will not produce a transmission signal if for no other reason than that it will not receive a Back signal.

In the present program, field R is an In field and its subfield r is blank but its subfield b contains digit 1. Since the zero filter for the subfield Rr is open, the R tree of the IC–ES to In group will not be heated and signal ICRI will not be produced. Accordingly, pilot unit 1 will not respond to signal R3 and the trigger 20, Fig. 80c, of this pilot unit will not turn to produce the signal TR Ink.

The heating of the operational sign storage circuits (Fig. 60) prepares for the operational signs in the P, Q, T and U fields to be applied, at the P, Q, T and U steps of the scanning sequence, to the accumulator unit. The heating of the OP1 pyramid causes the signal ACC Code to be applied to ACC.C and prepares for the production of the signal HCS.

The SCM signal initiates operation of the Ink delay counter. One of the initial functions of the Ink delay counter is the production of the signal HCR for resetting the half correction suppression storage trigger 5, Fig. 71g, and the tolerance check trigger 22, Fig. 71g. The next function of the Ink delay counter is to cause the signal ACCL to be applied to ACC.C for deconditioning it. The Ink signal subsequently occurs and completes the conditioning of the R and V spots for IC steps; also completes the conditioning of ACC.C; and times the production of the signal HCS for turning trigger 5, Fig. 71g, to its half correction suppression status.

The OCO and PS signals are produced. The OCO signal causes the numbers and signs from relay storage units 016 and 137 and from dial storage unit #3 to be entered in ES3, 2 and 6, respectively. The PS signal initiates the scanning sequence. The PI signal is given and causes ES3 to apply the number and sign from relay storage unit 016 to the Internal buses and also causes the + operational sign to be applied to the sign mixing circuit of the accumulator unit. The Pil.OC signal is produced and turns 21Q causing signal OP.OC to initiate operation of ACC.C to produce the signals RCC, ECC and ACC–RI. Accordingly, the number from relay storage unit 016 and its sign are entered in the accumulator. An accumulator cycle ensues and causes the entry of the number and sign into registers RC (Fig. 70). The complete signal CYCPT is applied to ACC.C which produces the signal OP.BS for resetting 21Q. The QI signal is given and causes the number and sign derived by ES2 from relay storage unit 137 to be applied to the Internal buses and also causes the — operational sign to be applied to the accumulator sign mixing circuit. The Pil.OC signal again is given and causes 21R to turn. This produces the signal OP.OC which initiates operation of ACC.C for causing the number derived from relay storage unit 137 to be subtracted in the accumulator unit from number derived from relay storage unit 016. The signal OP.BS then is produced and returns 21R. Since the R spot has been conditioned for an IC step, it now produces the signal OP.IC. This signal causes ACC.C to produce the signal R.ROC whereby the result and sign are read out of the accumulator unit and a Proceed signal is returned to ACC.C. The Proceed signal initiates operation of ACC.C to reset trigger 14 and to produce a signal OP.BS. The signal OP.BS resets 6R, causing 11R to turn. In a manner explained in Section 17 this initiates operations for sending the number from the accumulator unit through the denominational shift unit and storing the sign of the number. At the completion of the shift, which in this case is 0, 11R is reset and turns 15R. This produces the signal R2 in consequence of which, the result and its sign are entered in ES1. The signal Pil.IC is given and returns 15R whereupon 16R turns and produces the signal R3. Inasmuch as the subfield Rr is blank, the signal R3 has no effect, for reasons explained before in this section. The difference between the two answers in relay storage units 016 and 137 is now in ES1.

The FR signal was given upon the turning of 15R. Under control of this signal the OP2 pyramid is heated, and the operation of the Ink delay initiated.

The heating of the OP2 pyramid causes reduced potential to be applied to output line OPO3. Referring to Fig. 77a, reduced potential on line OPO3 cuts off 25 to render 26, 26a and 28 con-

ductive. When 28 is conductive it acts through 30 and 24 to produce the signal ACC Code. When 26a is conductive, it produces reduced potential on wire HCSw, causing 30 and 24 in Fig. 77b to produce the signal HCSS. When 28 in Fig. 77a is conductive it acts through 30a and 36 to produce the negative signal Tol.CKC. This signal cuts off 32, Fig. 78a. When the Ink signal is given (about 2 AP pulse cycles after the heating of the OP2 pyramid), it cuts off 32a, Fig. 78a, causing 32—32a to act through 34 for producing the signal Tol.CK. This signal goes to Fig. 71g and acts through 6 and 14 to turn the tolerance check signal storing trigger 22, Fig. 71g. With this trigger reversed the accumulator is conditioned to perform a tolerance check, in the manner described in Section 13.

The Ink signal also completes the reconditioning of ACC.C, and times the signal HCS.

Following the termination of the signal R3, the T spot performs its OC step. The signal T1 is given and causes the tolerance number derived from dial storage unit 3, to be applied by ES6 to the Internal buses. The T1 signal also causes the + operational sign to be applied to the sign mixing circuit of the accumulator unit. The Pil.OC signal is given and turns 21U causing it to send out the signal OP.OC. This signal initiates operation of ACC.C to produce the signals required for effecting the entry of the tolerance number, in a positive sense, into the result registers RC of the accumulator unit. Upon completion of the accumulator cycle in which this entry is made, ACC.C produces the signal OP.BS which returns 21U. The U OC step starts and the signal U1 is given. Under control of this signal, electronic storage unit 1, which during the R step received the answer difference, applies the answer difference to the Internal buses. Also, the absolute — operational sign is applied to the sign mixing circuit of the accumulator unit since the code number in Us is 3. The Pil.OC signal is again produced and causes 21V to turn. This produces another signal OP.OC under control of which the commutator ACC.C produces the signals ECC, ACC–RI and ACC–ST. These signals control the accumulator unit to receive the answer difference from ES1 and subtract it from the tolerance number previously entered in the accumulator during the T OC step. It should be noted that regardless of the sign of the answer difference as it stands in electronic storage unit 1, its complement is transferred from EC to RC of the accumulator unit. This is because the absolute — operational sign 3 has been applied to the sign mixing circuit and therefore causes the accumulator unit to treat the number as a negative number regardless of its original sign. In other words, the absolute value of the answer difference is subtracted from the positive tolerance number.

If the absolute value of the answer difference is less than or equal to the tolerance number, then the result is positive, but if the answer difference is greater than the tolerance number then the result will be negative. In a manner explained in Section 13, if the result of the tolerance check is positive then the Proceed signal will be produced. On the other hand, if the result is negative the Proceed signal will be suppressed.

The spot V is conditioned for an IC step in order to test whether or not the Proceed signal is being blocked. At the end of the accumulator cycle in which the answer difference is subtracted from the tolerance check number, the cycle complete CYCPT again operates on ACC.C to cause it to produce the signal OP.BS. This signal now returns 21V. As a result 5V is reset and 6V is turned. The turning of 6V produces the signal OP.IC. Under control of this signal, ACC.C applies the signal R.ROC to the accumulator unit. In a manner explained before in Section 13, the signal R.ROC initiates the sign test. Briefly, if the result sign is positive then the tube 11a, Fig. 71g, remains at cut-off, and when the Proceed trigger 19, Fig. 71g, turns, it is effective to produce the Proceed signal. On the other hand, if the sign test shows that the result sign is negative, a complement conversion cycle ensues and tube 11a, Fig. 71g, becomes conductive under the combined control of the reversed check trigger 22, Fig. 71g, and the complement conversion cycle trigger 11, Fig. 71f. With 11a, Fig. 71g, conductive the turning of the Proceed trigger is not effective to produce the signal Proceed. The readout signal ACC–RO is not interfered with, however, and the result and sign are applied to the Internal buses so that it may be transmitted to a receiving unit if so desired. If the Proceed signal is given then it acts on ACC.C to cause it to produce the signal OP.BS and to restore 14–ACC.C. The signal OP.BS this time restores 6V causing 11V to turn. Upon the turning of 11V operations are initiated for routing the number now applied to the Internal buses by signal ACC–RO through the denominational shift unit. The ACC–RO signal lasts for three AP pulses and therefore the number is removed from the Internal buses after it has been entered into the denominational shift unit. Upon completion of the shift, which in this case is 0, 11V is reset and causes 15V to turn. Inasmuch as the subfield Vb is blank, the signal V2 has no effect on any of the pilot units. The signal V2, however, goes to the blank code pilot unit (Fig. 78L) and cuts off 17a–BC. At the time the signal SCM was given for starting the commutator run the pilot units selection trees were heated. The heating of the V branch of the IC–Int to ES trees (Fig. 58) has produced cut-off potential on the output line IVCO. Accordingly, the tube 17–BC (Fig. 78L) has been cut off. Now, when the signal V2 cuts off 17a–BC, the couple 17—17a becomes effective through 10a and 2a to produce the signal Pil.IC which renders 12a, Fig. 78i, conductive, causing 11W to turn. This results in the production of the signal Pil.ICC just as when 11W is turned under control of the signal Pil.IC from the pilot units.

The signal Pil.ICC returns 15V causing 16V to turn and produce the signal V3 which has no effect because the subfields Vb and Vr are blank. The signal V.IC will be given, followed by the signal FC which is a manifestation of completion of the scanning sequence.

If the result of the tolerance check is negative then the turning of the Proceed trigger will not cause the signal Proceed to be produced. Hence, a signal OP.BS will not be sent out by ACC.C to cause the return of 6V. Since 6V is not returned 11V is not turned and signal V2 is not produced. Consequently, the signal Pil.ICC will not be produced and the operation of the spot V therefore stops. Accordingly, the FC signal will not be produced and one of the conditions for starting the next commutator run has not been satisfied. It is seen then that the machine stops if the result of the tolerance check is negative.

As stated before, the tolerance check may be

used for other purposes than to check accuracy of answers. For instance, it can be used to stop computations when a table of $f(x)$ has been computed between the limits of +.001 and +.0075. To check the lower limit, a tolerance number —.001 may be used and each $f(x)$ value added thereto. To check the upper limit, the tolerance number +.0075 may be used and each $f(x)$ value subtracted therefrom. This check may be made after each computation of $f(x)$. A typical line of sequence for ordering the check is:

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
2	1	012	1	2	013	4			0	03	01

Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
2	3	014	2	2		4			0	03	02

The upper tolerance value of +.0075 is in relay storage unit **012** (Pr) and the lower tolerance value is in relay storage unit **014** (Tr). The value of $f(x)$ obtained by the last computation is in relay storage unit **013** (Qr). Since number 03 is in fields OP1 and OP2, the tolerance check means will be used in each half of the scanning sequence. The signal OCO will time the entry of the upper tolerance limit into ES1 (Pb), the value of $f(x)$ into ES2 (Qb), and the lower tolerance limit into ES3 (Tb). The P OC step will cause the upper limit to be transferred from ES1 to the accumulator and there will be no change in sign (Ps is 2). During the Q OC step, the value of $f(x)$ will be taken from ES2 and entered into the accumulator, with a change in sign (Qs is 1). If the value of $f(x)$ is equal to or less than the upper tolerance limit, the result of the accumulation will be positive and a Proceed signal will be given during the R IC step. In this case, the R IC step functions the same way as the V IC step to test the result of the tolerance check. If the Proceed signal is given, the result in the accumulator will be read out to the Internal buses and into the denominational shift unit in the manner described for the first case in this section. The commutator ACC.C also will be conditioned to produce the RCC cancel signal in the second half of the sequence run. It may be mentioned that the R2 signal will mix with tree signal IRCO from trees IC–Int to ES (Fig. 58) in chassis BC (Fig. 78L) to produce the Pil.IC signal for allowing the first half of the scanning sequence to continue to completion if the Proceed signal has been given.

Assuming as above, that the value of $f(x)$ is not greater than upper tolerance limit +.0075, the second half of the scanning sequence will be started. In the T OC step, the accumulator will be canceled and the lower tolerance limit will be transferred from ES3 to the accumulator, without being changed in sign. During the V OC step, the value of $f(x)$ will be transferred from ES2 to the accumulator and no change in sign will be made. It should be noted that the conditions for this U step are similar to the conditions for the U step in the line of sequence explained before in this section, except that the absolute — operational sign is not used this time.

If the value of $f(x)$ is not smaller than +.001, then the addition of this value to the lower tolerance number —.001 will produce a positive result. But if the $f(x)$ value is less than +.001, its addition to the lower tolerance number —.001 will give a negative result. For example, if $f(x)$ is +.0009, its addition to —.001 gives a negative result. During the V IC step, the result of the second check will be tested and a Proceed signal will be given if the value of $f(x)$ is not less than the lower limit +.001 of the table to be computed. The machine operations then will continue.

If in the first half of the scanning sequence, the check result is negative, then the scanning sequence will stop after the signal R.ROC is given by ACC.C under control of the OP.IC signal from the R spot. In the absence of a Proceed signal, ACC.C will not produce the OP.BS signal for continuing the R IC step. If the Proceed signal is not given in the second half of the scanning sequence, the V IC step will be interrupted in the manner described before.

In Section 17, a program for accumulation of a pair of numbers, in one instance without half correction and in the other instance with half correction was explained.

In Section 17*a*, a program for accumulating three numbers and utilizing the T field as an In field was explained.

It is to be understood that the machine may be operated to accumulate directly any desired number of terms. Four terms selected by the P, Q, R, and T fields may be accumulated and their sum entered in a receiving unit selected by the U field. Five terms selected by the P, Q, R, T, and U fields of a line of sequence may be accumulated and their sum entered in a unit selected by the V field. A single line of sequence thus may call for successive accumulation of a maximum of five terms. If it is desired to accumulate directly more than five terms, two or more lines of sequence must be used. In that case, the V field of the first line will be left blank, and the V spot will act as a skip field, as in Section 16*b*, to signal the end of the scanning sequence. With other conditions for a new commutator run having been met as well, the second line of sequence may then be run off and five more terms may be accumulated. If a total of ten terms is to be accumulated successively, then the V field in the second line of sequence will be an In field. Obviously, any number of terms may be accumulated successively and directly in this manner.

18. *The multiplication sequence*

One or two multiplications may be ordered by a line of sequence, each multiplication in one half the line. If the code number in the OP field is 10, multiplication without half correction is ordered. If the code number is 15, multiplication with half correction of the product is ordered. An example of S1Seq data calling for multiplication without half correction of the product is given below:

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
1	1	017	2	2	158	4	3	139	0	10	01

Simply interpreted, the above program calls for a number from relay storage unit **017** (Pr) to be sent to ES1 (Pb) and thence to the M–D unit (see Section 14) to serve as the multiplicand, and for the — operational sign (Ps) to be applied to the MC–DR sign mixing circuit (Fig. 65*j*); for the number from storage unit **158** (Qr) to be sent to ES2 (Qb) and from there to the M–D unit to serve as the multiplier, and for the + operational sign to be applied to the MP–DD sign mixing circuit (Fig. 65*j*); for the product to be routed through the denominational shift unit without column shifting and to ES3 (Rb) and transmitted from there to relay storage unit **139**, with the sign of the product being determined by the sign mixing circuits in Figs. 65*j* and *k*. The S1 code number as now understood selects the next S1Seq data source.

Assume the above program has been entered in the side of sequence storage which is to be heated in preparation for the commutator run about to take place. The heating of the Out sequence storage circuits occurs under control of the last given signal STR (see Section 16*b*, Item 36). The heating of the In sequence storage circuits occurs under control of the last given signal AT (see Section 16*b*, Item 37). Between 10 and 11 ms. after the STR signal, the heating signal for the pilot units selection trees (Figs. 54 to 58) is produced. This heating signal also controls the heating of the operational sign sequence storage circuits (Fig. 60) and of the In code sequence storage circuits (Fig. 61). The signal SCM is given at this point and causes the heating signal to be produced for the OP1 pyramid (Fig. 59) and for the SH1, Q and R shift code sequence storage circuits (Figs. 62 and 63).

In a manner clear from Sections 11 and 17, the heating of the Out sequence storage circuits causes the multiplicand in relay storage unit 017 (*Pr*) to be applied, along with a Forward signal, to Out bus-set 1 (*Pb*). Also, the multiplier factor is applied from relay storage unit 158 (*Qr*) along with a Forward signal, to Out bus-set 2 (*Qb*). The heating of the In sequence storage circuits conditions the relay storage unit 139 (*Rr*) for receiving the product from Out bus-set 3 (*Rb*), and a Reset signal from pilot unit 3. Also, when the relay storage unit has been conditioned to receive a value, it applies a Back signal to pilot unit 3.

The heating of the operational sign sequence storage circuits (Fig. 60) results in reduced potential being present on the output wires 1P and 2Q. Accordingly, tubes 1 and 7 in the OPSN section of Fig. 78L are cut off.

The heating of the In code sequence storage circuits (Fig. 61) places reduced potential on the wire RIC, so the tube 17 in Fig. 78*b* is cut off. The heating of the pilot units selection trees (Figs. 54 to 58) causes the P branches to produce the signals OCO1 and *Pb*1 for selecting pilot unit 1 to pilot the entry of the multiplicand into ES1 from relay storage unit 017, and then the application of the multiplicand by ES1 to the Internal buses. The Q branches produce the similar signals OCO2 and *Qb*2 for selecting pilot unit 2 to pilot the reception by ES2 of the multiplier factor from relay storage unit 158 and then the application of the multiplier factor by ES2 to the Internal buses. The R branches of the pilot units selection trees produce the signals PRES3, IRC3, and ICR3 for selecting pilot unit 3 to presense a transmission, and to pilot the product from the calculating unit (M–D in this case) into the denominational shift unit and from there to ES3 and thence to selected relay storage unit 139.

The heating of the R branch of the shift code sequence storage circuit (Fig. 63) and the heating of the SH1 shift code sequence storage circuit (Fig. 62) has no real effect in the present program because a shift is not called for by code number 4 in *Rs* and because SH1 is blank.

The heating of the OP1 pyramid (Fig. 59) causes reduced potential to be present on the output line OP10. Referring to Fig. 77*a*, the reduced potential on line OP10 cuts off 1 so as to render 2 and 2*a* conductive. The output of 2*a* is connected to the wire HCS*w* so that the signal HCSS will be produced and will cut off 30, Fig. 78*a*. With 2, Fig. 77*a*, conductive, it cuts off 12, causing 6 to produce the negative signal

MY–Code. The signal MY–Code cuts off (Fig. 78M) in the multiplying calculation commutator MYC.

The SCM signal occurs at the beginning of the commutator run and initiates the operation of the Ink delay counter in Fig. 78*c*. Upon the turning of the first trigger 5P of this counter it renders 9P conductive to produce the negative signal MDC. This signal cuts off G63 (Fig. 65*b*). The tube G62 is still at cut-off because the interlock line *d*51 is still at low potential. Accordingly, when the tube G63 is cut off, the couple G62—G63 applies a positive pulse by way of a capacitor to a standard cancel circuit which is represented in Fig. 65*b* by the tubes G62*a*, G61 and G60. When G62*a* receives the positive impulse from G63 and G62, it becomes conductive and cuts off G60 so as to produce a rise in the cancel bias line —100C which is the output line of the cancel circuit. The —100C line from this cancel circuit resets the half correction suppression storage trigger G24 and also resets the triggers shown in Fig. 65*a*.

Two AP pulse cycles after the SCM signal, the Ink delay counter produces the Ink signal. The Ink signal cuts off 30*a*, Fig. 78*a*; tube 30 already has been cut off by the signal HCSS. Accordingly, the signal HCS is produced at this point and is effective to cut off G40 (Fig. 65*b*) whereupon G32 conducts and reverses G24 to store the half correction suppression signal (see Section 14*a*).

The Ink signal also cuts off 17*a*, Fig. 78*b*. Tube 17 already has been cut off by the tree signal RIC. Accordingly, trigger 19 is turned and the signal R "in" appears and conditions the R spot of the commutator for an IC step, as in Section 17, Item 14*a*.

The Ink signal also cuts off 8*a*, Fig. 78M. The tube 8 has already been cut off by the signal MY–Code. When 8 was cut off it applied conditioning potential to 7. Now, when 8*a* is cut off by the Ink signal it renders the conditioned tube 7 conductive, causing it to reverse 11. The trigger 11–MYC may be called the gate of the multiplicand control commutator MYC. When 11 is in reversed status, it is conditioning this commutator for operation. Reverse 11 maintains 2 and 16 at cut-off. With 2 cut off, it maintains 6 conditioned, and 5 conductive. Conductive 5 produces the negative signal M–PRE (see Fig. 65*e*). This signal cuts off H28—H27 in Fig. 65*e* so as to cause the "up multiplier" plus *my* to be set at increased potential, as explained in Section 14*a*. The M–PRE signal also brings into operation the cancel means shown in Fig. 65*e* for resetting the control triggers of the Internal commutator of the M–D unit, except for the triggers shown in Figs. 65*a* and *b* (see Section 14*a*).

The OCO commutator signal appears two AP pulse cycles after the signal SCM (see Section 17, Item 15*a*). This signal operates the selected pilot units 1 and 2 to produce their signals OCS. The latter signals are effective in conjunction with Forward signals received by these pilot units to cause the pilot units to produce the signals for entering the multiplicand and multiplier factors from relay storage units 017 and 158 into electronic storage units ES1 and ES2, respectively.

Commutator signal PS, which in simultaneous with signal OCO, initiates the scanning sequence. The signal P1 cuts off 1*a*–OPSN (Fig. 78L). The tube 1–OPSN has been cut off by the tree signal

1P. Accordingly, the signal P1 now is effective to render 1—1a effective through 2, 4a and 4b to produce the — operational sign signal OPSN1. This signal is applied via the line 1s in Fig. 65j to the MC/DR sign mixing circuits.

The signal P1 also mixes with the tree signal Pb1 to cause the selected pilot unit 1 to produce its signal OC Int (see Section 17, Item 16b). The pilot unit 1 produces the signal ES1 to Int and the signal Pil.OC. The former signal causes the multiplicand to be applied by ES1 to the Internal buses. The Pil.OC signal is followed by the signal Pil.OCC which occurs at AP pulse time and causes 21Q to turn, whereupon the first, negative signal OP.OC appears and is inverted by 29, Fig. 78c, to a positive signal OP.OC. This positive signal is effective now to render conditioned tube 6–MYC (Fig. 78M) conductive. As a result, trigger 10 is turned and causes 14 to turn. Upon the turning of 14 it renders 9 and 17 conductive. Conductive 9 produces the signal MCC, while conductive 17 produces the signal PQC. In a manner described in Section 14a, signal MCC resets the register MC–DR (Fig. 64b) and the MC/DR sign mixer (Fig. 65j). Signal PQC resets the register PQ (Fig. 64h).

The next BP pulse following the turning of 14, Fig. 78M, is effective to return this trigger, thus ending the cancel signals MCC and PQC. Upon termination of signal MCC, the multiplicand operational sign enters the MC/DR sign mixer (Fig. 65j). Upon the return of the trigger 14, Fig. 78M, it turns 18. The following AP pulse returns 18, causing it to turn 15. Upon the turning of 15 it renders 13 conductive to produce the signal MC–RI. This signal causes the multiplicand, now on the Internal buses, to be entered in register MC–DR (see Section 14a). Also, the signal MC–RI causes the sign of the multiplicand to be entered into the sign mixing circuit MC/DR (Fig. 65j).

The trigger 15, Fig. 78M, was turned at AP pulse time to produce the signal MC–RI. The next AP pulse resets 15, terminating the reading signal MC–RI. Upon the return of 15 it turns 19. This renders 20 conductive so that 16a is cut off. Tube 16 also is at cut-off since commutator MYC has been conditioned. Accordingly, when 16a is cut off, the couple 16—16a makes 12 conduct and produce the first negative signal OP.BS. This signal acts through 27a and 32 in Fig. 78c to produce the negative signal OP.BS which goes to all of the triggers 21 of the scanning spots. The signal is effective this time to restore 21Q. This terminates the P OC step and initiates the Q OC step. Since the P OC step has terminated, the signal ES1 to Int also ends and the multiplicand and its sign are removed from the Internal buses; also the operational sign for the multiplicand is removed.

When 21Q returned, it caused 22Q to turn for one AP pulse cycle. Upon the return of 22Q, it turns 23Q to cause signal Q1 to appear. Signal Q1 cuts off 7a–OPSN (Fig. 78L) and since 7 also is cut off by the free signal 2Q, the + operational sign signal OPSN2 is produced, as in Section 17, Item 19. This signal is applied to line 2s in Fig. 65j.

Signal Q1 also mixes with signal Qb2 to cause selected pilot unit 2 to produce its signal ES2 to Int, as in Section 17, Item 19. Under control of this signal, the multiplier factor is applied by ES2 to the Internal buses. The Pil.OC signal again occurs and this time causes 21R to turn and produce the second signal OP.OC. The signal OP.OC makes 6–MYC (Fig. 78M) conduct. The resulting negative pulse resets 19, ending the first OP.BS signal. Upon the return of 19, it turns 23, causing 21 to conduct and produce the negative signal MPC. The signal MPC resets the multiplier factor register MP (Fig. 64b) and the MP/DD sign mixer triggers (Fig. 65j), as described in Section 14a. The BP pulse following the turning of 23, Fig. 78M, resets this trigger, ending the MPC signal. The operational sign signal is still effective after the termination of the signal MPC and now enters the operational sign into the MP/DD sign mixer. Upon the return of 23, Fig. 78M, it turns 27, which is reset by the next AP pulse. When 27 is reset, it turns 22, causing 25 to produce the signal MP–RI. Under control of this signal, the multiplier factor, now being applied by ES2 to the Internal buses, is entered in the register MP. Also, the signal MP–RI enters the sign of the multiplier into the MP/DD sign mixer. The signal MP–RI lasts for one AP pulse cycle since trigger 22–MYC was turned at AP pulse time and is reset by the next AP pulse.

When 22–MYC is reset, it turns 31–MYC, making 20a conduct so as to cut off 16a. Consequently, a second signal OP.BS is produced which this time resets 21R (Fig. 78e). This ends the Q OC step and initiates the R IC step. Upon termination of the Q OC step, the signal Q1 ends, whereby signal ES2 to Int also ends and the multiplier factor and its sign are removed from the Internal buses. The ending of signal Q1 also ends the operational sign signal OPSN2 which was applied to the MP/DD sign mixing circuit.

When 21R was reset by the second OP.BS signal to end the Q OC step, it turned 22R for one AP pulse cycle. Since the R spot is conditioned for an IC step, 23R is blocked from turning and the signal R1 is suppressed, as explained in Section 17. The turning of 22R resets 5R which makes 6R turn.

The R IC step was initiated upon the return of 21R by the second OP.BS signal. This signal resulted from the turning of 31–MYC (Fig. 78M). The trigger 31–MYC was turned when 22–MYC was reset at AP pulse time and ended the MP–RI signal. The next AP pulse resets 31–MYC, which reverses 30–MYC. Reversed 30 makes 29 conduct and produce the start signal MY–ST. This signal cuts off D31a (Fig. 65f), and thereby initiates the multiplying computation, in the manner explained in Section 14a.

Upon completion of multiplication, the internal commutator of the MD unit produces the signal R–CPLT (see Section 14a and Fig. 65k). This signal cuts off 28, Fig. 78M. When 28a is cut off by the next occurring AP pulse, the couple 28—28a makes 26 conduct and return 30, thus ending the MY–ST signal. The return of 30 also turns 34 which causes 35 to turn. Turned 34 makes 33 conduct and produce the negative readout signal R.RO. Under control of this signal, tubes 8 and 9 in Fig. 65k produce the positive signal R.RO which causes the product to be read out of the result register PQ onto the Internal buses. The negative signal R.RO from the commutator MYC also operates via 36, Fig. 65k, to cause the product sign to be read out. The negative signal R.RO also causes D42 (Fig. 65f) to be reset, all as explained in Section 14a.

Trigger 35, Fig. 78M was turned at the AP pulse time at which the signal R.RO was initiated. The next AP pulse resets 35, causing it to turn 36 for one AP pulse cycle. Upon 36 turning, it makes

24 conduct and cut off 16a. Since 13 also is at cut-off, couple 16—16a now operates via 12 to produce the third OP.BS signal.

The third OP.BS signal resets 6R (Fig. 78e) causing 11R to turn. Just as in Section 17, the turning of 11R causes the number on the Internal buses to be entered in the denominational shift unit. In the present case, this number is a product being read out of PQ by signal R.RO. The sign of the product is stored at this time by the trigger 2M or 6M in Fig. 78a (see Section 17, Item 21). After the product has been entered in the denominational shift unit, and its sign stored, the shift start signal SHS is given and causes the shift unit to shift the product the desired number of steps. In the present program, the shift amount is 0, so the shift-complete signal SHCP is given at once to indicate that shifting is complete. This causes the signals SHRD and SHRO to be produced, as in Section 17, Item 22. Under control of these signals, the product number is applied by the shift unit to the Internal buses and its stored sign is applied to column 1 of the Internal buses.

When 36–MYC (Fig. 78M) was turned (at AP pulse time), it produces the third OP.BS signal which caused 11R to turn and initiate the SHRI and SHCL signals for entering the product into the shift unit. The entry signal SHRI lasted for two AP pulse cycles. Trigger 36–MYC was turned for one AP pulse cycle and upon its return, it turned 32 for one AP pulse cycle. When 32 returned, it restored 34, thereby ending the readout signal R.RO, at the same time as the entry signal SHRI ended. Also, it should be noted that the signal R.RO occured upon the turning of 34 one AP pulse cycle before 36 turned to initiate the operations leading to the entry signal SHRI and the concurrent cancel signal SHCL. This is sufficient time for cross-talk to be dissipated before entry can be effected.

When 32, Fig. 78M, returned to end the signal R.RO, it also returned triggers 10 and 11. The return of 11 deconditions commutator MYC. The return of 10 enables the commutator, when next reconditioned, again to produce the signals MCC and PQC when called for by the OP.OC signal.

One AP pulse cycle after the shift unit and sign storing triggers have been controlled by the readout signals SHRD and SHRO to apply the product and its sign to the Internal buses, the signal CSV is produced, as in Section 17, Item 22, and returns 11R which causes 15R to turn. Operations such as described in Section 17 occur for causing the product and sign to be entered in ES3 and transmitted to selected relay storage unit 139.

If the code number in the OP field is 15, then multiplication and half correction of product is called for. The tree signal OP15 will cut off 13, Fig. 77a, causing 12 and 6 to produce the signal MY–Code. The signal HCSS will not be produced. Accordingly, half correction of the product will follow the completion of the multiplying computation, after which the complete signal R–CPLT will be given (see Section 14).

19. *The Dividing Sequence*

A dividing sequence may be ordered by a half line of sequence. The code number 20 in the OP field calls for dividing without half correction. The code number 25 in the OP field calls for division with half correction of the quotient. A sample half line of sequence for a dividing calculation without half correction is:

Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
2	1	151	1	2	142	4	3	136	9	20	02

Briefly, this program instructs the machine to take the divisor from relay storage unit 151(Tr) and direct it via ES1(Tb) to the M–D unit (Section 14); to take the dividend from relay storage unit 142(Ur) and bring it through ES2 to the M–D unit; to pass the quotient to the denominational shift unit, where it shall be shifted nine places to the right (Vs is 4 and SH2 is 9); and to transmit the shifted quotient to ES3(Vb) and thence to relay storage unit 136(Vr).

Assume the program is in the heated side of sequence storage and the SCM signal has been given. This signal initiates the operation of the Ink delay counter (Fig. 78c) to produce the Ink signal. The Ink signal conditions the V spot for an IC step, as in Section 17, Item 14a. The OCO and PS signals occur, as in Section 17, Item 15a. The OCO signal operates selected pilot units 1 and 2, assuming they have received Forward signals, to pilot the divisor and dividend into ES1 and ES2. The PS signal initiates the scanning sequence. Towards the end of the first half of the scanning sequence, the signal FR is produced and initiates operation of the Ink delay to produce the second Ink signal. The FR signal also causes the heating signal for the OP2 pyramid and of the shift sequence storage circuits SH2, U and V to appear. The shift amount of 9 is applied to lines MN (Figs. 78a and 27a) and the right-shift direction is applied to line RT (Fig. 78a). The shift amount also is applied to lines MMN (Fig. 65a) for the purposes explained in Section 14b. Two AP pulse cycles later, the Ink signal causes the shift amount to enter the descending counter (Fig. 27a) and sets trigger 21, Fig. 27c, in right-shift status. Upon the heating of the OP2 pyramid, the line OP20 is reduced in potential and cuts off 25, Fig. 77b, causing 26 and 26a to conduct. As 26a conducts, the signal HCSS is produced to combine with later signal Ink in producing the half correction suppression signal. When 26 conducts, it acts via 30a and 36 to produce signal Div. Code. This signal acts through 8–DVC (Fig. 78D) to condition 7. The later Ink signal cuts off 8a to render 7 conductive. This causes gate trigger 11 of the commutator DVC to turn. With 11 turned, it maintains 2 and 16 non-conductive. Non-conductive 2 conditions 6 and also serves via 5 to produce the sustained presense signal D–PRE which is applied to H23 and H27a in Fig. 65e for causing the "up divide bus" to be placed at increased potential (see Section 14b) and for initiating operation of the MDC cancel circuit.

During the T OC step, the signal T1 is given and operates selected pilot unit 1 to produce the signal ES1 to Int, so that the divisor is applied to the Internal buses. The Pil.OC signal occurs and is followed by the signal Pil.OCC which causes conditioned 24T to turn 21U. This produces the first OP.OC signal in the second half of the scanning sequence.

This first signal OP.OC causes conditioned 6, Fig. 78D, to turn 10 which turns 14. Turned 14 makes 9 conduct to produce signal DRC. This signal causes the register MC–DR (Fig. 64b) to be reset (see Section 14b). The next BP

pulse resets 14, Fig. 78D, ending the signal DRC and turning 18. The next AP pulse resets 18, which turns 15. Turned 15 acts through 13 to produce signal DR–RI. This causes the divisor now on the Internal buses to enter register MC–DR. Trigger 15 is reset by the next AP pulse, ending the signal DR–RI and turning 19. Thereupon 20 is made to conduct and cut off 16*a*. As 16 is cut off when commutator DVC is conditioned, the couple 16—16*a* now acts through 12 to produce the signal OP.BS. This resets 21U, ending the T OC step, whereupon the divisor is removed from the Internal buses. The return of 21U also initiates the U OC step during which signal U1 is produced. Signal U1 operates selected pilot unit 2 to cause ES2 to apply the dividend to the Internal buses. Also, a signal Pil.OC is produced and causes 21V to turn, whereupon a signal OP.OC appears and acts via 6, Fig. 78D, to return 19–DVC. Upon the return of 19, it turns 23 which makes 21 conduct and produce the signal DDC. This signal cancels the register PQ (Fig. 64*h*), as explained in Section 14*b*. Trigger 23 is reset by the next BP pulse, ending signal DDC and reversing 27. The next AP pulse resets 27, causing it to turn 22, whereupon 25 produces the signal DD—RI, so that the dividend now on the Internal buses is entered in the dividend orders 5 to 18 of the register PQ (see Fig. 66A). The next AP pulse returns 22, Fig. 78D, ending the signal DD–RI and also turning 31. Turned 31 renders 20*a* conductive to cut off 16*a*, whereupon the signal OP.BS is given and returns 21V. Since the V spot is conditioned for an IC step, the signal OP.BS resets 5V, which turns 6V.

One AP pulse cycle later, 31, Fig. 78D, is reset and turns 30, causing 29 to produce signal DV—ST which initiates the dividing computation (see Section 14*b*). At the end of the dividing computation, the MD unit applies the signal R–CPLT to the commutator DVC (Fig. 78D). The signal cuts off 28. At the first effective AP pulse, 28*a* is cut off and 28—28*a* is then effective via 26 to return 30.

Upon the return of 30, signal DV–ST terminates and, also, 34 turns. Upon 34 turning, it makes 33 conduct and produce the signal R.RO which causes the quotient to be read out from PQ to the Internal buses.

When 34 turned, it reversed 35. The next AP pulse resets 35, causing it to turn 36. The following AP pulse resets 36, causing 32 to turn for one AP pulse cycle. Upon the return of 32, it resets 34, ending the R.RO signal, and also resets 10 and 11, restoring commutator DVC to initial, deconditioned status.

When 36–DVC was turned, it made 24 conduct, cutting off 16*a*, so that the signal OP.BS was produced. In the manner explained in Section 17, this signal now resets 6V and the V IC step continues. During the continuation of this step, the quotient is shifted by the donominational shift unit 9 places to the right and transmitted via ES3 to relay storage unit 136.

20. *Operations relating to the table look-up*

The table look-up apparatus was described briefly in Section 10. Portions of the circuits for reading a computed argument into the apparatus and for reading out selected functional values from the apparatus were also described in Section 10 with reference to Fig. 35. In Section 11, the selection of table look-up Group Ins and Outs and of Table Ins and Outs were described with reference to Figs. 47*b*, 47*c*, 51, and 52*a*.

Fig. 35*a* is a block diagram indicating relationship between elements of the table look-up apparatus. As mentioned in Section 10, the table look-up operation is initiated by the energization of relay R11 (Fig. 35). Under control of this relay and in a manner described in application Serial No. 768,600 of Hamilton et al, filed August 14, 1947, the computed argument storage means CA (Fig. 35*a*) is reset. Also, under control of and after the energization of relay R11, the relays R40, and R41 (Fig. 35*a*) are deenergized. When the table look-up operation is completed, these relays again are energized and remain energized until another table look-up operation is initiated. After computed argument storage CA has been reset under control of R11, the computed argument enters therein under control of temporary computed argument storage TCA (also see Fig. 35). The computed argument is compared with station arguments by station comparison units which are arranged in accordance with the arrangement of stations in the various tables 1 to 6. This comparison selects one of the stations, in the selected table, from which the computed argument is to select a tape argument. This selection is effected by the energization of one of the station selector relays 1SS to 36SS. The selected station relay controls circuits to bring into operation the clutch drives for the selected argument station and companion functional value tape stations. Further, the selected station relay operates means for closing contact points between sensing elements of the selected argument station and an intrastation selection comparing means. The intrastation selection comparing means compares the computed argument with tape arguments on the selected argument tape. This comparison selects a tape argument and its companion functional values. After this selection is checked, the relays R40 and R41 are energized.

The selected functional values are now in sensing positions and may be read out as called for by the program. The selected station relay in conjunction with a selected Table Out relay and in accordance with plugging, causes energization of one or two of the relays 1SS to 36SS and 1BSS to 36BSS, one of the selected relays being a BSS and the other an ASS relay. The selected station relays close points in the readout circuits for the selected functional values, as described in Section 10 (also see Fig. 35).

The functional values selected to be read out are routed into Out bus-sets and thence, in the same way as other values, into electronic storage. The entries into electronic storage are piloted by the pilot units, in the manner described in previous sections. Before a pilot unit can produce a signal for timing entry into electronic storage from an Out bus-set, the pilot unit must receive a Forward signal from the source of the value to be entered. In the case of the table look-up apparatus the Forward signal is not to be given until and unless a tape argument and its companion functional values have been selected and are ready to be read out. This selection is manifested by the energization of relays R40 and R41. When relay R40 is energized, it opens its points *c* (Fig. 35*b*) to break the circuits of any of the relays TOC which may have been previously established during a table look-up operation. As a result of the deenergization of the relay TOC, its points *a* (Fig. 47*c*) close so as to permit the

sequence storage circuits to be selectively established, in accordance with the program, through the corresponding one of the table Out relays 1TO to 6TO. The energized relay TO closes its contacts 81*a* and *b* (Fig. 35*b*) which are points of the Forward signal circuit for the table look-up apparatus. Other points in this circuit are contacts of the selected station relays 1ASS to 36ASS and 1BSS to 36BSS. Still other points of the Forward signal circuits are contacts 81 of the table look-up group Out relays TLU–GO1 to 8. The plugging will be made between sockets ROG81 and sockets RO81*a* and 81*b* in accordance with which of the station readout relays are to be used for reading out functional values. Assume, for instance, that readout relay 1ASS is to be energized when a certain functional value in table 1 has been found. Upon energization of table out relay 1TO and a selected table look-up group Out, for instance, table look-up group Out 1, a Forward signal path will be closed from the +150 v. line via a point 81 of 1ASS and point 81*a* of 1TO; plugging between RO81*a* and ROG81 associated with contact 31 of TLU–GO1, and via the latter contact to bus 31 of Out bus-set 1.

The computed argument will be transmitted to the table look-up apparatus from electronic storage under control of a transmission signal ES to In produced by a pilot unit. One of the conditions for a pilot unit to produce a transmission signal is that the pilot unit first receive a Back signal from the unit which is to receive the transmitted value. If the table look-up apparatus is selected to receive a value, then it will function to produce a Back signal if the apparatus is not in the process of looking up a value. If the apparatus has completed the process of looking up desired values in accordance with a selection by computed argument, then relays R40 and R41 are energized. The relay R41 then closes its contacts *bs* (Fig. 35*b*). The selected table look-up relay also closes its points 81, and a Back signal path is then established from the +150 v. line through the contacts *bs* of R41 and the contacts 81 of the selected relay TLU–GI1 to 8, to the bus 81 of the corresponding In bus-set.

A program for a table look-up operation is given below:

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
2	1	127	4	1	281					02	01

The P field calls for a computed argument to be read out of relay storage unit 127, via Out bus-set 1, to electronic storage unit ES1. The Q field is an In field since 4 stands in Qs. The In field Q calls for the computed argument which has been entered in ES1 to be transmitted therefrom to the table look-up apparatus, since the code number 281 in Qr represents table 1 of the table look-up apparatus. This means that the table look-up gang relay 1TL will be energized. Since Qb contains 1, table look-up Group In gang relay TLU–GI1 will be energized, in the manner explained in Section 11.

The energized relay TL closes its contacts *d* (Fig. 35*b*) so as to establish the circuit of the pickup coil *p* of the corresponding relay TOC. The circuit of the hold coil *h* of the relay is established via the stick contacts *b* and the normally closed contacts *c* of R40.

The code number 02 in OP1 calls for the conditioning of the accumulator control commutator ACC.C (Fig. 78A), in the manner explained in Section 17. During the commutator run for interpreting the above program, the signal OCO acts in conjunction with a Forward signal from electronic storage unit 127 to cause pilot unit 1 to produce the signal Out to ES1 for entering the computed argument into ES1. The signal PS starts the scanning sequence. The P1 signal is given and controls pilot unit 1 to produce the signal ES1 to Int, whereby ES1 applies the computed arugment to the Internal buses. As this occurs, pilot unit 1 produces the Pi1.OC signal which causes 21Q (Fig. 78*d*) to turn. Consequently, the signal OP.OC is produced and operates on conditioned ACC.C to cause it to produce the signals RCC, ECC and ACC–RI. The computed argument now on the Internal buses is entered in registers EC of the accumulator. An accumulator cycle ensues and the computed argument is transferred to registers RC of the accumulator unit. At completion of the accumulator cycle, the signal CYCPT operates on ACC.C to cause it to produce the signal OP.BS. This signal resets 21Q (Fig. 78*d*), causing 22Q to turn for one AP pulse cycle. Since Q is an In field, the Q spot has been conditioned for an IC step in a manner explained in Section 17*b*. Accordingly, 23Q is prevented from turning when 22Q returns. Instead, the return of 22Q restores 5Q which thereupon turns 6Q. When 6Q turns it produces the signal OP.IC which operates on ACC.C to cause it to produce the signal R.ROC. Accordingly, the signals ACC–RO and Proceed are produced. Signal ACC–RO causes the accumulator unit to apply the computed argument, entered during the P OC step to the Internal buses. Proceed signal acts on ACC.C to cause it to produce another signal OP.BS. This signal now restores 6Q which results in the turning of 11Q. In the manner described in the preceding Sections 17, 17*a* and 17*b*, the turning of trigger 11 of a scanning spot of the commutator initiates the operation of the denominational shift unit to receive the number on the Internal buses, while the sign of the number is stored in 2M or 6M (Fig. 78*a*). The denominational shift unit proceeds to shift the number the selected amount, and at the end of this shift the complete signal SHCP is returned to the main commutator and causes it to produce the signals SHRD and SHRO for reading out the shifted number and its sign to the Internal buses. One AP pulse cycle later the signal CSV is produced which returns 11Q, causing 15Q to turn. This results in the production of signal Q2 which controls selected pilot unit 1 to pilot the computed argument and its sign, now applied to the Internal buses by the denominational shift unit and sign storage triggers, into ES1. As this is done, the pilot unit produces the signal Pi1.IC which causes 15Q to return. Upon the return of 15Q it turns 16Q for one AP pulse cycle. When 16Q is in turned position, it produces the signal Q3. This signal is one of the conditions for the initiation of transmission from selected electronic storage unit ES1, as may be understood from Section 17. Another condition is the Presense signal NPR. A third condition is the Back signal from the selected receiving unit, which in this case is the table look-up apparatus. This Back signal is produced in the manner explained before in this section (see Fig. 35*b*). Since pilot unit 1 has been selected, the Back signal will be applied to this pilot unit. The Back signal, acting in conjunction with the Presense signal NPR, causes the pilot unit to produce the Reset signal in the manner described in Section 17. The Reset sig-

nal in this case is applied by bus 82 of In bus-set 1 to the now closed points 82 (Fig. 35) of TLU–GI1 and thence via the points *a* of R40 (energized since a table look-up operation has not yet been initiated), and from there through the pickup coil *p* of relay R11 to the +150 v. line. Upon energization of coil *p* of R11, it closes its contacts *a* so as to shunt out the contacts R40*a*. Under control of relay R11, when energized, relays R40 and R41 (Fig. 35*a*) are deenergized, as previously stated.

Assuming that the Back signal, the Presense signal and the Q3 signal all have been produced, the selected pilot unit 1 produces the signal ES1 to In which causes electronic storage unit 1 to apply the computed argument and sign to In bus-set 1. The computed argument is transmitted via this In bus-set to the contacts of TLU–GI1 (Fig. 35) plug sockets BP and 1TP, and contacts of 1TL to temporary computed argument storage, as explained in Section 10. The table look-up operation then occurs in the manner previously explained. At the end of this table look-up operation the relays R40 and R41 are deenergized and functional values, selected in accordance with the computed argument, are positioned at reading positions of the selected tape stations.

During the process of looking up the desired values under control of a computed argument, other computations may be and are as a rule performed in accordance with instructions given by lines of sequence following the line which includes the program such as given above for directing a table look-up operation to be performed. After a variable, desired number of lines of sequence have been interpreted, following the line which called for a table look-up operation, another line of sequence is used to direct the functional values selected in the previous table look-up operation to be read out. Such line of sequence may be, for example, as follows:

S1Seq

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
			2	1	281	2	2	281	0	02	01

S2Seq

Ts	Tb	Tr	Qs	Qb	Qr	Vs	Vb	Vr	SH2	OP2	S2
2	3	281	2	4	281	4				02	02

It is assumed, for this example, that two station readout relays have been selected by the table look-up operation, one being a relay ASS and the other a relay BSS (see Fig. 35). It is assumed further than two functional values are recorded on the selected line of the tape to be read out via points of the selected relay ASS and two other functional values are recorded on the line selected to be read out via points of the relay BSS.

For this example, the plugging in the Forward signal circuits (Fig. 35*b*) of the Table look-up is from the pair of sockets RO81*a* and RO81*b* associated with points 81*a* and 81*b* of 1TO to the sockets ROG81 associated with points 81 of TLU–GO1, 2, 3, and 4.

When the table look-up operation has been completed, the relay R40 is energized, so that its point *c* (Fig. 35*b*) is now open and the relay 1TOC is deenergized.

Assume the last-given line of sequence is now in one side of sequence storage and this side is now heated. Since the code number 281 is in the subfield *r* of fields Q, R, T, and U, and since point 1TOC*a* (Fig. 47*c*) is now closed, the Table Out pyramids for these fields all pick up gang relay 1TO (also see Section 11). Also, since the code number in the subfields *r* of these fields is between 200 and 399, the Q*b*, R*b*, T*b*, and U*b* trees in the table look-up Group Out pyramids (Fig. 47*b* and Section 11) are heated. As the Q*b*, R*b*, T*b*, and U*b* trees are respectively set at 1, 2, 3, and 4, the table look-up gang relays TLU–GO1, 2, 3, and 4 are energized.

Forward signals are then applied from the +150 v. line in Fig. 35*b*, via contacts 81 of the selected ASS relay and the selected BSS relay to the contacts 81*a* and *b* of relay 1TO, thence via the plugging from sockets RO81*a* and *b* associated with the latter contacts to sockets ROG81 associated with contacts 81 of TLU–GO1, 2, 3, and 4. The circuits continue in parallel via the latter contacts to buses 81 of Out bus-sets 1, 2, 3, and 4, whereby Forward signals are applied to pilot units 1, 2, 3, and 4.

The energization of the selected table look-up relays 1TO and TLU–GO1, 2, 3, and 4, as well as of the ASS and BSS pair of relays causes the four functional values from two selected tapes in the table look-up means to be applied to Out bus-sets 1, 2, 3, and 4. The readout plugging, for this example, may be from, say, sockets 3 to 40 of group 1A (Fig. 35) to sockets 3 to 40 of ROG1, from sockets 43 to 80 of group 1A to sockets 3 to 40 or ROG2, from sockets 3 to 40 of group 1B to hubs 3 to 40 of ROG3, and from hubs 43 to 80 of 1B to hubs 3 to 40 of ROG4. In this way, four nine-place numbers and their signs may be read out from two selected functional value stations in the table look-up to columns 1 to 10 buses of four Out bus-sets.

After the heating of the Out sequence storage circuits, the signal SCM is given. At the same time, the heating signals appear for the pilot units selection trees (Figs. 54 to 58), the In code and Operational Sign sequence storage circuits (Figs. 61 and 60), the SH1, Q, and R shift code sequence storage circuits (Figs. 62 and 63) and the OP1 pyramid (Fig. 59). Two AP pulse cycles later, the Ink signal occurs and completes the conditioning of ACC.C (Fig. 78A) since OP1 contains code number 02 (see Section 17), and also completes the conditioning of the V spot (Fig. 78*h*) for an IC step.

The signals OCO and PS are given at this time. Signal OCO and the Forward signals control the selected pilot units 1, 2, 3, and 4 to produce the signals for entering the functional values selected by the table look-up unit into ES1, 2, 3, and 4.

The PS signal initiates the scanning sequence, and signal P1 is given. Since field P is blank, the signal P1 acts through the blank code pilot unit BC (Fig. 78L) to produce the signal Pil.OC. This causes 21Q to turn and produce signal OP.OC. As commutator ACC.C is conditioned, signal OP.OC controls this commutator to produce the signals RCC, ECC and ACC–RI. Since there is no value now on the Internal buses, no entry occurs into the accumulator. The cycle complete signal CYCPT is returned to ACC.C which produces the signal OP.BS, causing return of 21Q. This initiates the Q OC step, and signal Q1 is given.

Signal Q1 causes selected pilot unit 1 to produce signal ES1 to Int, so that the value received before by ES1 is applied to the Internal buses and a Pil.OC signal is returned to the main commutator. This signal now turns 21R giving an OP.OC signal. Signal OP.OC acts on ACC.C to cause it to produce the signals for bringing about entry of the value on the Internal buses into the

accumulator. After this entry has been made, ACC.C produces signal OP.BS which returns 2IR, terminating the Q OC step and initiating the R OC step.

The R OC, T OC, U OC and V IC steps are performed sequentially in the manner covered in previous sections. It is to be noted that in the V IC step, the accumulator will be read out and a Proceed signal given. Accordingly, ACC.C will be reconditioned to produce the signal RCC in a next accumulator sequence. The sum of the functional values may or may not be transmitted to storage, depending on the instructions recorded in the V field. In this example, the V field is blank in subfields *b* and *r*, so the sum of the values will not be stored. The purpose of this run has been merely to enter values from the table look-up apparatus into electronic storage and the commutator ACC.C has been selected to produce the back signals OP.BS for enabling the scanning sequence to proceed to completion.

If desired, values may be entered via Out bus-sets into electronic storage during a commutator run in which none of the commutators ACC.C, MYC, and DVC is conditioned. The program data controlling such run will not include an effective In field. When the V field is blank, the V spot is conditioned to perform an OC step, as in Section 16*b*, Item 26V. Accordingly, the scanning sequence may be completed in the manner described in Section 16*b*. An illustrative line of sequence ordering entry from Out bus-sets into electronic storage, without the use of the commutator ACC.C or an In field is:

Ps	*Pb*	*Pr*	*Qs*	*Qb*	*Qr*	*Rs*	*Rb*	*Rr*	SH1	OP1	S1
			2	1	281	2	2	281			01
Ts	*Tb*	*Tr*	*Us*	*Ub*	*Ur*	*Vs*	*Vb*	*Vr*	SH2	OP2	S2
2	3	281	2	4	281						02

Since the OP fields are blank, the commutator NO (Fig. 78*c*) will be conditioned, as in Section 16*b*. During the scanning sequence, signals P1, Q1, R1, T1, U1 and V1 will be given. Signal P1 will act through chassis BC (see Fig. 78L and Section 16*b*, Item 26P) to produce signal Pil.OC for causing 2IQ to turn. The resulting signal OP.CC will act on commutator NO to cause it to produce signal OP.BS for returning 2IQ to initiate the Q OC step. The signal Q1 will be given but since pilot unit 1 has been selected by *Qb*, the signal Pil.OC will be given by this pilot unit and cause 2IR to turn. Signal OP.CC will again be produced and go to commutator NO for causing it to produce signal OP.BS for resetting 2IR. The R1 signal will be given and cause selected pilot unit 2 to produce signal Pil.OC, and so on. In this way, the signals for continuing the scanning sequence will be given by the selected pilot units, the blank code pilot unit, and the commutator NO.

21. *The "early and late" operation*

As explained in Section 9, only two stations in the same tape storage bank can be read out simultaneously, one via its A station selector (Fig. 31) and the other via its B station selector. Normally, therefore, a line of sequence may direct a tape storage bank to read out only two of its stations to two Out bus-sets. To make greater use of a tape storage bank, "early and late" means are provided to enable four stations in the same bank to be read out during a single commutator run. Two of these stations may be read out concurrently to two Out bus-sets after which two of the other stations in the same bank may be read out to two other Out bus-sets. The "early and late" means provides, specifically, for two stations in a bank to read out a next line of sequence data after which two other stations in the bank may be read out, all in a single commutator run. To plug a bank for reading out to four Out bus-sets, sockets ASSP (Fig. 32*a*) must be plugged to sockets TS–GOP related to two of the Group Outs and sockets BSSP must be plugged to sockets TS–GOP related to two other Group Outs for the same bank. Further, the relays ASS and BSS for one pair of stations and the Group Outs selected for these stations must be operated first and after entries from these stations into electronic storage have been completed, then only may the relays ASS and BSS and selected pair of Group Outs for the other pair of stations be energized.

Assume, for example, as in Section 16*b*, Item 8, that stations 1 and 10 of bank 1 are to be read out via their A and B selectors, respectively, to Out bus-sets 7 and 8. Assume, further, that stations 3 and 4 are to be read out via their A and B selectors, respectively, to Out bus-sets 1 and 2. If all four stations are to be read out in the same commutator run, then gang relays 1ASS and 10BSS and Group Outs 7 and 8 must be operated first and their data entered into ES7 and 8. After completion of this entry, the relays 1ASS and 10BSS and Group Outs 7 and 8 must be dropped, and then relays 3ASS and 4BSS and Group Outs 1 and 2 may be operated. In other words, the heating of the Out sequence storage circuits for the selected "early and late" tape storage bank must be deferred until after the sequence data entry completion signal SE (Section 16*b*, Item 25) has been given. This is done by delaying the pick up of heating relays X4, X5, or X6, depending on which tape storage bank has been selected for "early and late" operation.

If "early and late" operation of a tape storage bank is to be effected, the "early and late" S1, S2 pyramids (Fig. 50) are plugged according to the S1 and S2 code numbers to the gang socket TSL1, 2, or 3 (Fig. 53*b*) according to whether the bank to be so operated is bank 1, 2, or 3. To continue with the previous example, sockets SELP01 and 02 are plugged to socket TSL1. Socket TSL1 is wired to line Late 4. This line (also see Figs. 76*g* and 75*g*) is coupled to the grid of 8, Fig. 75*g*.

The "early and late" S1, S2, pyramids (Fig. 50) are made up of points of intermediate sequence storage relays AI, on the A side, and of points of relays BI, on the B side (see Section 11). The intermediate relays are energized earlier than the operational relays (AOP or BOP) of sequence storage. Energization of relays AI (or BI) is effected when the sequence data is transmitted from ES7 and 8. The relays AI then close points to pick up the operational relays AOP (or BOP). The STR signal, given at completion of sequence data transmission (see Section 16*b*, Item 33) drops the AOR (or BOR) relays so as to provide stick circuits for the energized AOP (or BOP) relays. The STRD1 pulse, some 10 ms. later, energizes the AIR (or BIR) relays (see Section 16*b*, Item 39) to drop the AI (or BI) relays. When the STRD1 pulse has been given, when the scanning sequence also has been completed, and when the all-entry delay pulse AED also has been given, a new commutator run for interpreting the sequence data just transmitted to sequence storage may begin. Between the time of energization of the AI (or BI) relays by the STR signal time, and the deenergi-

zation of these relays some 10 ms. later by the STRD1 pulse, the "early and late" S1, S2 pyramids (Fig. 50) function to set up a delay in the heating time for the Out sequence storage circuits of the selected "early and late" bank. The delay is terminated when, in the new commutator run, the sequence data has been safely entered in electronic storage. The terminating signal in this case is the SED signal (see Section 16*b*, Item 30).

In the assumed example, when relays AI (or BI) have been energized according to a new line of sequence data, the S1, S2 pyramids are set according to the code numbers 01 and 02. The S1, S2 Station Move, Group Outs, and Unit Outs pyramids are heated by points of relays X1 (or Y1) energized at STR signal time (see Section 16*b*, Items 7 and 36). The "early and late" S1, S2 pyramids are heated at STR signal time, as follows. The STR signal acts via **23***a*, Fig. 75*e*, to turn **28**, cutting off **21**. With **21***a* already at cut-off under control of **22** in reset state, **21**—**21***a* produces increased potential on wire *x2w*. The increased potential on this wire conditions a grid of **11**, Fig. 75*f*. The trigger **22**, Fig. 75*e*, will be turned by a next AE signal (see Section 16*b*, Item 28). The next STR signal will return **28**, Fig. 75*e*. Accordingly, increased potential will then be applied by couple **27**—**27***a* to the wire of *y2w*, causing **10**, Fig. 75*f*, to be conditioned. Thus, either the tube **11** or **10** in Fig. 75*f* is conditioned at the STR signal time depending on whether the A or B side, respectively, of sequence storage is to be heated. The STR signal also acts, as described in Section 16*b*, Item 10, via **5**, Fig. 75*f*, to turn the first trigger **4** of the "Late Delay." Upon this trigger turning, it applies increased potential to grids of **10** and **11**. One of these also is receiving increased potential on its other grid, at the STR signal time, as just described. Accordingly, when **4** turns, it renders one of the tubes **10** and **11** conductive. If **11** conducts, it acts via **5***a* to place increased potential on line *x* LATE, but if **10** conducts, it acts via **15** to cause increased potential to be present on the line *y* LATE. Increased potential on line *x* LATE makes **3** and **4** in Fig. 76*g* conduct to apply decreased potential to the line ELX. Increased potential on line *y* LATE makes **5** and **6** in Fig. 76*g* conduct to place decreased potential on line ELY. The line ELX is the heating line for the A side of the S1, S2 "early and late" pyramids (Fig. 50) while the line ELY is the heating line for the B side of these pyramids.

In the above manner the proper side of the "early and late" pyramids is heated at STR signal time. Upon the heating of these pyramids, they apply cut-off potential, in the assumed example via SELP01 and 02 and TSL1 (Fig. 53*b*), and via line Late **4** to **8**, Fig. 75*g*.

Two AP pulse cycles are allowed for sensing the existence of an "early and late" plugging. This delay is provided by the "Late Delay" in Fig. 75*f*. At the end of the delay, trigger **1**, Fig. 75*f*, turns and is effective through **8** to produce cut-off potential on line Late Ink. The cut-off potential is applied by this line to **8***a*, Fig. 75*g*. Since **8** also has been cut off, couple **8**—**8***a* acts now via **9** to turn **10** so as to block **11** and **17** from becoming conductive. The trigger **12** or **18** is also turned at this time, as described in Section 16*b*, Items 11 and 28. Briefly, if line *x2w* has been previously raised in potential, at STR signal time as explained before, it renders **29** conductive to cut off **27***a*, Fig. 75*f*. Two AP pulse cycles later, the decreased potential on line Late Ink cuts off **27**, whereupon **27**—**27***a* causes **12** to apply a negative impulse via line **102** to **12**, Fig. 75*g*, turning it. In a similar way, **18**, Fig. 75*g*, is turned if line *y2w* has been increased in potential. If the "early and late" pyramids were not plugged to Late **4**, then **10**, Fig. 75*g*, would not be turned at Late Ink time. The turning of **12** or **18** at this time would then render **11** or **17** conductive, so that heating relay X4 or Y4 would be energized. When, as in the assumed example, the "early and late" pyramids are plugged to line Late **4**, then **10** and **12** or **18** are turned at the same Late Ink time. The turning of **10** prevents the turning of **12** or **18** at this time from rendering **11** or **17** conductive, so that relay X4 or Y4 is not energized.

The relays X4 and Y4 are heating relays for the A and B sides, respectively, of the bank 1 tape storage Group Out trees (Fig. 47*b*), bank 1 move relay trees (Fig. 47*c*) and of the bank 1 station selector ASS and BSS trees (Fig. 47*d*). Thus, when X4 (or Y4) is not energized, the bank 1 pyramids and trees cannot function to pick up Group Outs, Move relays, and ASS and BSS relays.

The trigger **12** or **18** in Fig. 75*g* is not reset until an all-entry complete signal AE is given (see Section 16*b*, Item 28). In the "early and late" operation, the sequence data entry complete signal SE and its delay signal SED are given before the AE signal because Forward signals from the required units of the bank selected for "early and late" operation are delayed. The signal SED (Section 16*b*, Item 30) resets trigger **10**, Fig. 75*g*. This allows the trigger **12** or **18**, still reversed, to render **11** or **17** conductive, so that the heating relay X4 or Y4, as the case may be, is then energized. The bank 1 pyramids may then function to pick up the desired Group Outs, station selector relays ASS and BSS, and Move relays, after which Forward signals are applied to the selected Out bus-sets.

Similarly, the "early and late" S1, S2 pyramids (Fig. 50) may be plugged to line Late **5** or Late **6**, if four stations are to be read out during a run from bank 2 or bank 3 of tape storage. The Late **5** line if selected will cut off **20**, Fig. 75*g*, and the line Late **6**, if selected, will cut off **2**, Fig. 75*h*. If **20**, Fig. 75*g*, is cut off, the Late Ink signal when it cuts off **20***a*, causes **20**—**20***a* to act through **21** to turn **22**, whereby **23** and **29** are cut off. This prevents **24** or **30**, whichever is turned at Late Ink time, from rendering **23** or **29** conductive so that relay X5 or Y5 is not energized and the heating of the bank 2 sequence storage circuits is delayed. If **2**, Fig. 75*h*, has been cut off, the Late Ink signal when it cuts off 2*a*, causes **2**—**2***a* to operate through **3** to turn **4**; whereby **5** and **11** are blocked from being made conductive by turning of **6** or **12** at Late Ink time. Thus the relay X6 or Y6, as the case may be, is not energized and the bank 3 sequence storage circuits are not heated until the signal SED is given. This signal restores **4**, Fig. 75*h*, and **22** and **10** in Fig. 75*g*.

The next BP pulse after turning of **1**, Fig. 75*f*, resets it, whereupon **4** is reset, terminating the heating of the "early and late" S1, S2 pyramids (Fig. 50). This may be safely done since the test for an "early and late" plugging has already been made and the Late Ink Signal has already been given to cause trigger **10** or **22** in Fig. 75*g* or **4** in Fig. 75*h* to turn so as to delay

the heating of tape storage bank 1, 2, or 3 sequence storage relays.

An illustrative program for which the "early and late" operation may be used is:

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
2	1	505	2	2	010	2	3	011	7	15	01
Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
2	4	508	2	5	012	4	6	013	7	15	02

Assume the code numbers 01 and 02 in S1 and S2 are to select stations 1 and 10 of bank 1 to read out sequence data to ES7 and 8. The code number 505 in Pr calls for data to be read out of station 2, bank 1 via its A station selector, and digit 1 in Pb calls for the data to go to ES1. The code number 508 in Tr directs data to be read out of station 3, bank 1, via its B station selector, and digit 4 in Tb calls for the data to go to ES4.

Assume the above program has been set in the A side of sequence storage. The last given STR signal has caused relay X1 to be energized, so the S1, S2 pyramids on the A side are heated and cause relays 1ASS, 10BSS, TS–GO7 and 8, and Move relays MA and MB, all in bank 1 to be energized, as in Section 16*b*, Item 8. The "early and late" pyramids (Fig. 50) have been heated, on the A side, at STR time because tube 11, Fig. 75*f*, has been rendered conductive. Accordingly, line Late 4 has been reduced in potential and has cut off 8, Fig. 75*g*. Two AP pulse cycles later, the signal Late Ink appears and cuts off 8*a*, Fig. 75*g*, so that trigger 10 is turned and blocks 11. Trigger 12, Fig. 75*g*, also is turned at Late Ink time but with 11 cut off, the relays X4 are not energized.

In the ensuing commutator run, the OCO signal operates on selected pilot units ES7 and 8 to cause it to pilot the sequence data from stations 1 and 10 of bank 1 into ES7 and 8, as in Section 16*b*, Item 24*b*. The SE signal is given after the sequence data have been entered and stations 1 and 10, bank 1, have been advanced under control of Move signals from pilot units 7 and 8. The SE signal causes X1 to be deenergized (Section 16*b*, Item 29). Accordingly, relays 1ASS, 10BSS, TS–GO7, TS–GO8, MA and MB, all in bank 1 are dropped. Some 8 ms. later, signal SED appears (Section 16*b*, Item 30) and resets 10, Fig. 75*g*, whereupon, relay X4 is energized, heating the bank 1 sequence storage pyramids. Thereupon, relays 2AAS, 3BSS, TS–GO1, TS–GO4, and MA and MB, all in bank 1 are energized. Forward signals now appear on Out bus-sets 1 and 4 and combine with the still active OCO signal to cause selected pilot units 1 and 4 to pilot data from stations 2 and 3 of bank 1 into ES1 and 4.

When all the entries called for by a line of sequence have been safely made, signal AE is given and terminates signal OCO (see Section 16*b*, Item 31).

22. *The printing means*

Results or other information stored in the machine may be recorded by any of several units as and when called for by the program. One such unit is called printer #1 which is of the kind for printing one line at a time. The printing unit has a capacity for printing numbers stored in four relay storage units. Each relay storage unit may store a number having 19 digits and a sign, or, as explained in Section 7 may be used as a split storage device to store two numbers, each with 9 digits and a sign. The printing unit has enough capacity to print, in one line, four 19-digit numbers and their four signs, as read out from four relay storage units, or to print eight 9-digit numbers and their eight signs, as read out from the halves of the four storage units. The printing unit also has sufficient capacity to provide appropriate separation between the numbers printed along a line.

The print structure is, except for certain differences which will be indicated, of the kind disclosed in prior Patents 2,079,418, 2,199,547 and 2,042,324. Referring to Fig. 82, the printing unit includes a platen roller 92*p*. The work sheet is brought around the platen and over a pin-feed wheel 295, then over a cover plate 296. Behind the platen roller are eighty-nine parallel, vertically disposed type carriers 93*p*. Each type carrier mounts, one above the other, eleven type slides 94*p* bearing types which are, from top to bottom, 9, 8, 7, 6, 5, 4, 3, 2, 1, –, 0. The types are inverted in order that the recorded characters be in upright position for viewing by an observer when the printed portion of the sheet is on or in front of cover plate 296. Each type carrier is connected at the bottom to a link 97*p* pivoted at 98*p*, and connected by a spring 99*p* to a common bar 100*p*. Bar 100*p* is fixed between arms 101*p* and fast to a shaft 102*p*. Connected by links 104*p* to arms 101*p* is a restoring bail 103*p* overlying all the arms 97*p*.

Fixed to the shaft 102*p* is an arm 105*p* which is connected by link 106*p* to a cam follower 107*p*. The cam follower follows a pair of complementary cams 109*p* and 110*p* which are fixed to a cam shaft 111*p*. During each revolution of the cam shaft the cams 109*p* and 110*p* oscillate the cam follower 107*p*. Upon the counterclockwise movement of follower 107*p*, shaft 102*p* and arms 101*p* move clockwise. Restoring bar 103*p* also moves clockwise while the springs 99*p* force the arms 97*p* to follow, elevating the type carriers 93*p*.

The type carriers may be individually arrested in different positions to present selected types at print position. The arresting means includes ratchet teeth 119*p* provided on each type carrier and spaced similarly to the type slides 94*p*, except for the last, 0 type slide, which has no corresponding tooth 119*p* but is presented to printing position when the type carrier rises to its limit. Arranged to coact with the ratchet teeth of each type carrier is a pawl 118*p* held by armature latch 117*p* of a magnet PM from engaging the ratchet teeth. When the magnet is energized the latch 117*p* is released from pawl 118*p* which springs into arresting engagement with a tooth 119*p* of a type carrier. There is one such arresting means including a magnet PM for each type carrier.

When a type carrier is arrested, the associate arm 97*p* stops and the connected spring 99*p* stretches while the actuating arms 101*p* and restoring bail 103*p* continue to rock clockwise. After the period during which the type carriers may differentially be set in printing positions, the print hammers 95*p* are tripped at 196 degrees index time (Fig. 86), and strike the type elements at printing position in order to print the selected data through an ink ribbon upon the work sheet on the platen.

The type hammers 95*p* are free on a shaft 96*p* and urged into printing action by springs 130*p*. This action is normally restrained by latches 131*p*. Interponents 132*p* are pivotally carried by the lower ends of the latches. At their rear the interponents hook over a bail 133*p* fixed to a shaft 134*p*. A hammer restoring bail 144*p* is

fixed on the shaft 96p. Shaft 134p has fixed to it an arm 135p which has a pin and slot connection to a link 136p pivoted to a bell crank 137p fixed to the shaft 96p. The bell crank 137p is connected by a link 138p to an arm 139p fixed to a pivot shaft 140p which also has fixed to it a cam follower 141p. Cam follower 141p cooperates with complementary cams 143p carried by the cam shaft 111p. During a revolution of the cam shaft the cams 143p act through the described linkage to rock the shafts 96p and 134p first clockwise and then counterclockwise. The pin and slot connection between link 136p and arm 135p permits shaft 96p and restoring bail 144p to move clockwise before the arm 135 moves clockwise, so that the bail 144p may be moved out of the way of the hammers 95p before the bail 133p moves to the rear for releasing the hammer latches 131p. Upon the release of the hammer latches from the printing hammers, the springs 130p drive the printing hammers into printing action. Upon counterclockwise movement of the shaft 96p, the bail 144p restores the hammers to latched position.

After the printing operation, the restoring bail 103p moves down and returns the type carriers 93p to their lower limit. When the type carriers have been restored, the pawls 118p are returned into latching engagement with the latches 117p. The means for effecting the return of the pawls into latching engagement includes a cam 300 on the cam shaft 111p. The cam 300 is engaged by a follower 301 which is connected by a link 302 to a lever 303. The lever 303 is urged by a spring 304a in a counterclockwise direction so as to maintain the follower 301 engaged with the cam 300. The upper end of lever 303 abuts a bail 304 pivoted on a shaft 305 on which the pawls 118p are loosely mounted. The bail 304 is connected by a link 306 to an armature knock-off bail 307. After the type carriers have been restored, the cam 300 rocks follower 301 counterclockwise, causing the lever 303 to move clockwise for rocking the bail 304 upwardly and causing the bail 307 to move clockwise. The bail 304 thereby restores the pawls 118p and the bail 307 positively returns the armatures 117p into latching engagement with the returned pawls.

When a type carrier 93p rises to its upper limit it presents its zero type to printing position. As the type carrier rises to its upper limit, a lug 297 on the type carrier moves a pivoted bell crank 298 counterclockwise. A lateral projection 298a on the bell crank thereupon tilts the associated interponent 132p out of the path of the bail 133p, so that printing of zero may be suppressed.

It is desired, however, to be able to print zeros to the right of a significant digit; i. e., in orders below the significant digit order. In prior art machines, this has been accomplished by carry-zero levers, each pivotally mounted on a hammer latch, and having two positions of adjustment. In one position of a zero-carry lever, it has no effect on the hammer latch at the right. In an alternative position of the zero-carry lever, it communicates the motion of its own hammer latch to the hammer latch at the right. An example of such mechanical connection between adjacent hammer latches is the lever 282 in Fig. 3 of Patent 2,199,547. In this way, printing of zeros to the right of a significant digit have been effected. The present printing unit provides also for printing of zeros to the left of a significant digit; that is, in orders above the significant digit order. This is desirable when dealing with decimals.

For this purpose, a novel carry-zero lever 310 (Figs. 84 and 85) is provided. This lever is pivotally carried at the upper end of a hammer latch 131p and has three positions in place of the conventional two. The lever is frictionally retained in any of the three positions to which it may be manually adjusted.

Fig. 85 is a perspective view of a pair of adjacent hammer latches 131p, with their carry-zero levers 310 and also shows the front end of the lever 310 at the left of the two latches shown. Since the types are inverted and the printed numbers are read upright from the point of the platen 92p (Fig. 82), the denominational order relationship from left to right of the elements shown in Fig. 85 is lower order lever 310, intermediate order latch 131p and its lever 310, and higher order latch 131p and its lever 310. With lower order lever 310 in position C (also see Fig. 84), it is out of the path of movement of the intermediate order latch 310. Hence, if the intermediate order hammer latch is rocked to trip its type hammer, it will not affect the lower order hammer latch and printing of zeros in the orders below the intermediate order will not take place. This is desired if a split between numbers is to be made. With the intermediate order lever 310 in position B, its front lug 310a is in the path of the transversely bent lug 131a of the higher order. Thus, if the latch 131p in the higher order moves forward to trip its hammer, it will effect similar movement of the intermediate order hammer latch, even if the intermediate order type carrier 93p (Fig. 82) has moved to its upper limit to present 0 at printing position. In this way, if the higher order prints a significant digit, zero will be printed in the intermediate order. Should the lower order lever 310 also be in position B, the movement of the intermediate latch 131p will effect movement of the lower order latch. Thus, printing of zeros in one or more orders below a significant digit order may take place. If the lever 310 in the intermediate order were in position A, as is the lever 310 of the higher order, then its edge 310b would be behind the lug 131a of the higher order. Accordingly, forward hammer typing movement of the intermediate latch 131p would be communicated by its lever 310 to the higher order latch 131p. In this way, even if the higher order type carrier moved to zero position, a zero would be printed if the intermediate order had a significant digit. By setting successive adjacent levers 310 in position A, printing of as many zeros as desired in orders above a significant digit order may be effected.

It should be noted that if intermediate lever 310 were in position A, its lug 310a would be in the path of lug 131a of the higher order and the edge 310b of this lever also would be in position to enage the lug 131a of the higher order. Thus, if the intermediate order latch is rocked forward, it will move the higher order latch, or if the higher order latch is rocked forward it will move the intermediate order latch.

In short, with a lever 310 in position C, its carrying latch 131p is unaffected by the latch in the order above it or by the latch in the order below it. If the lever 310 is in position B, its carrying latch 131p is moved if the latch in the order above is moved, so that zero printing in the lower order will be effected. If the lever 310 is in position A, its carrying latch 131p will be moved

if either the latch in the order above or the order below is moved, so that zero will be printed if printing occurs in the order below or the order above.

The platen roller 92p (Fig. 82) and the pin-feed wheel 295 are suitably geared together and operated to line-space the work sheet upon energization of a magnet LSM (Fig. 87a) prior to a printing operation. Any suitable line spacing means may be used; such as, for example, disclosed in U. S. Patent 2,189,025.

Cam shaft 111p operates cams of a conventional type for controlling timing contacts shown only in the circuit diagram, Fig. 87a, and also operates an emitter EM, also shown in Fig. 87a. Fig. 86 is a timing chart indexed in degrees according to the marking of an index wheel (not shown) which moves 1 to 1 with the cam shaft.

The printer unit is clutched in for a cycle when called for by the program. The clutch means includes a clutch magnet PRC (Fig. 83) energization of which releases detent 315 from a clutch pawl 316. The clutch pawl springs into engagement with a tooth of a driving element 317 and couples the cam shaft 111p to the driving element. The driving element is driven by gearing in a gear box 318, which gearing is actuated by belt-and-pulley connection 319 from a motor PRM. The clutch magnet will be deenergized shortly after the cam shaft starts a revolution, and detent 315 thereby will be positioned to retract the clutch pawl 316 and stop the cam shaft at the end of its revolution. The cam shaft is stopped at 330 degrees index time (see Fig. 86), and when clutched in also starts its revolution at that point. The clutch magnet may be reenergized before the cam shaft completes its revolution, so that the cam shaft may continue uninterruptedly for a second revolution, and so on.

Printer #1 when clutched in for a cycle is capable of printing data stored in relay storage units 120, 121, 122, and 123. Each storage relay of these units not only operates stick contacts a and readout contacts b, as described in Section 7 (also see Fig. 29), but also operates one or more points in a tree, of which there is one for each storage column. Fig. 87b shows, as representative, the trees operated by columns 1, 2, and 20 of a relay storage unit 120, 121, 122, or 123. The form of tree in Fig. 87b varies slightly from that in Fig. 45 but the same form could be used if desired. Both forms provide decimal notation representations of binary-decimal settings. The tree may be used as in sequence storage (Section 11) to establish any of several circuits upon the heating of the tree, in this way translating the binary-decimal setting of the tree into a singly-timed selection of one of several elements, each corresponding to a different decimal notation digit. The tree also may be used in combination with differential timing means, such as emitter EM (Fig. 87a) to establish a circuit, at a differential point of a base cycle, through a single element. This is the manner in which the trees shown in Fig. 87b are used. The brush of emitter EM (Fig. 87a) wipes emitter spots 9 to 1 and — sequentially during a print cycle (see Fig. 86) in synchronism with the arrival of types 9 to 1 and — at the printing line. The spots 9 to 1 of the emitter are wired to four sets of terminals em9 to 1, each set being connected, as indicated in Fig. 87b, to a set of wires w9 to 1 in one of the four relay storage units. The set of wires w9 to 1 connects to the decimal notation points 9 to 1 at the bases of the twenty column trees in the storage unit. Since the emitter is connected to the sets of wires w9 to 1 of the four relay storage units, the emitter senses the decimal notation representations 9 to 1 produced by all eighty column trees, twenty in each storage unit, at the differential times at which types 9 to 1 are presented to the printing line.

During the period in which the emitter senses the trees for representations of digits, relays SM (Fig. 87b) in each storage unit are energized by a circuit traced later and close their points 1 to 20. This connects the apexes of the trees to terminals pt. The terminals pt of relay storage units 120, 121, 122, and 123 are wired, as indicated in Fig. 87a, to plug sockets STP1 to 80. Those plug sockets STP which are wired to the column trees selected to represent digits, as distinguished from signs, are selective plugged to sockets STPP1 to 89. The sockets STPP are wired to the print magnets PM (see Fig. 82) associated with the eighty-nine type carriers 93p.

Assume, for instance, that relay storage unit 120 is set to store a single number which may have as many as nineteen digits and a sign, with column 1 being used to store the sign. The sockets STP2 to 20 may be plugged to sockets STPP2 to 20 or sockets STPP3 to 21 or any other set of nineteen successive sockets, leaving a socket at the left to receive the sign representation, which is recorded only if a — sign, as will be brought out. If relay storage unit 120 is set to store a number in each half, two sign columns are present, one being column 1 and the other being column 11. Sockets STP2 to 10 may then be plugged, for instance, to sockets STPP68 to 76 and sockets STP12 to 20 to sockets STPP81 to 89. The sockets STP wired to the other storage units 121, 122, and 123 may similarly be plugged selectively to sockets STPP. It is clear that plugging may be such as to cause the numbers from relay storage units 120, 121, 122, and 123 to be printed in selected fields of a line. If four fields be designated, for convenience of the description, A, B, C, and D, from left to right, four numbers from storage units 120, 121, 122, and 123 may be printed respectively in fields A, B, C, D, or B, A, C, D, or C, A, B, D, or D, C, B, A, or D, B, C, A, and so on. Eight numbers may be printed if the relay storage units are each used to store two numbers and the plugging allows for these numbers to be printed in different positions along a line. It is clear that the number from relay storage unit 120, 121, 122, or 123 may be printed selectively in the right-hand field of the line.

During a cycle of the print unit, when the emitter wipes its 9 spot, it establishes a circuit via any storage column tree set at 9 for energizing the print magnet associated with the tree, thus causing the 9 type in the corresponding type carrier 93p to be arrested at printing position. The circuit extends from ground (Fig. 87a) via circuit breakers C11 and C12, the emitter brush, the 9 spot, the terminal em9, wire w9 (Fig. 87b), the point 9 at the base of a column tree, the shifted contacts a of the 1 storage relay, the shifted contacts a of the 8 storage relay, the connected, now-closed points of relays SM, the connected terminal pt, the plug socket STP (Fig. 87a) wired thereto, the plugwire to the selected

socket STPP, and through the magnet PM to the +50 v. line.

Similarly, the digits 8, 7, 6, 5, 4, 3, 2, and 1 may be read out of the number storing columns at the differential times at which the types **8**, **7**, **6**, **5**, **4**, **3**, **2**, and **1** are presented to printing position, so as to cause these types to be arrested at printing position. The 0 setting of a column tree need not be read out since the 0 type is presented at the upper limit position of a type bar and is printed or not printed according to the setting of the carry-zero lever **310** (Figs. 84 and 85).

Only a — sign will be printed preceding a number. The — sign type is presented to the printing position at the time the emitter brush traverses the — sign spot (Fig. 87*a*); i. e., one differential interval after the brush wipes the 1 spot. The — sign is represented, however, in the sign storage column by digit 1. But the emitter EM cannot serve when wiping the 1 spot to time the printing of the — sign because the — sign type is not presented at printing position until one differential interval later. To overcome this difficulty, the emitter is used when it wipes the 1 spot to set up a circuit for enabling the emitter as it wipes the — spot, one differential interval later, to time the printing of the — sign. For this purpose, the sockets STP which are wired to sign storage columns are plugged to selected sockets STPS. The sockets STPS are connected by contacts **1** to **10** of relay **R13**, when these contacts are closed, to relays **R14** to **R23**. The relay **R13** is energized by the closure of cam contacts **C7** (see Figs. 86 and 87*a*) after the "2" readout time. It should be noted that each readout time is determined by the circuit breaks **C11** and **12** in conjunction with the emitter EM. Thus, the "2" readout time is the interval of the cycle between 117 degrees and 126 degrees. Cam contacts **C7** close shortly after the "2" readout time and do not open until the end of the "1" readout time. Thus, relay **R13** is energized only for a period which includes the "1" relay time. During the "1" readout time, the brush of emitter EM wipes the 1 spot and in conjunction with circuit breakers **C11** and **C12** completes circuit paths through the storage column trees set at 1 to the related plug sockets STP. The plug sockets STP associated with the sign columns are plugged to sockets STPS and since contacts **1** to **10** of **R13** are closed at this time, circuits are completed through those of relays **R14** to **R23** which are wired to the plugged-in sockets STPS, according to which of the sign storage columns is storing the — sign indicant 1. Energization of a relay **R14** to **R23** closes its contacts *a*, which are wired between emitter spot — and a plug socket STSP. The plug sockets STSP are plugged to sockets STPP according to the positions selected for receiving the — sign imprint.

Assume, for example, that the left-hand column of a sheet is to receive the — sign. The plug socket **STPP1** in that case is plugged to a socket STSP. The particular socket STP wired to the sign storage column is plugged to that socket STPS which is in the circuit of the relay **R14** to **R23** having contacts *a* associated with the socket STSP which has been plugged to socket **STPP1**. If the sign storage column is storing the — sign indicant 1, then in the "1" readout time, the selected relay **R14** to **R23** will be energized and close its contacts *a*. The energized relay **R14** to **R23** is held by a stick circuit made through its contacts *b* and cam contacts **C6**, which do not open until after the emitter brush wipes its — spot. When the emitter brush wipes its — spot, a circuit is completed from ground, via **C11**, **C12**, the emitter brush, the — spot, the closed contacts *a* of the selected relay **R14** to **R23**, the connected plug socket **STSP1** to **10**, plugwire to the socket **STPP1**, and through the print magnet **PM1**, to the +50 v. line. The magnet **PM1** is thereby energized at a time to stop the related type carrier **93***p* with its — type in printing position.

Shortly after the cam shaft **111***p* has been clutched in for a revolution, cam contacts **C1** close and establish a circuit path via safety contacts which need not be discussed here to plug sockets STU and via plugwires to sockets STUS, and to terminals *tsm*. Each of these terminals is wired, as indicated in Fig. 87*b* to the group of relays SM of one of the four relay storage units which are to be read out to the print unit. Thus, the relays SM are energized to close their points **1** to **20** in order to connect the storage column trees to the plug sockets STP (Fig. 87*a*). This occurs before the emitter brush wipes the 9 spot and remains in effect until the end of the "1" readout time.

Cam contacts **C10** close before printing time, at 196 degrees, to establish a circuit via safety or interlock contacts, which need not be discussed here, through the paper line space magnet LSM. Energization of this magnet causes line spacing of the sheet, as previously mentioned.

If the printer unit is to be used, the operator closes the Start key contacts (Fig. 87*a*) to establish the circuit of a relay STD. Contacts *an* of this relay close and in conjunction with Stop key contacts (normally closed) establish a stick circuit for the relay. The circuit may be opened by depressing the Stop key.

22a. A program including printing

Printer #**1** is scheduled for operation by any of the four code numbers 160, 161, 162 and 163 in subfield *r* of an In field. The code numbers 160, 161, 162, and 163 also schedule relay storage units **120**, **121**, **122**, and **123**, respectively, for receiving an entry. Entries may have been made into three of these storage units as called for by their identifying code numbers during a preceding run or runs of sequence. When the entry is made into the fourth one of the storage units and it is desired also to print the data entered in all four of these storage units, the code number 160, 161, 162, or 163 is used depending on which of the storage units **120**, **121**, **122**, or **123** is the fourth one scheduled to receive an entry. A line of sequence calling for the printer to operate also may include one or two calculation programs. The printer code number will always be placed in the last program field which is to be scanned for an entry into the relay storage units **120**, **121**, **122**, and **123**. Several illustrative printer program lines are given below:

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
2	1	010	2	2	011	4	3	123	0	01	01
Ts	Tb	Tr	Us	Ub	Qr	Vs	Vb	Vr	SH2	OP2	S2
0	4	121	4	5	122	4	6	160	0	01	02

This program calls for accumulation with T as an In field (see Section 17*a*) and for printer operation. The terms in storage units **010** and **011** will be added and transmitted during the R IC step to storage unit **123**, during the T IC step to storage unit **121**, during the U IC step to storage unit **122**, and during the V IC step to storage unit **120** and at that point the printer unit will be called in to print the sum placed in storage units **120**, **121**, **122**, and **123**. This pro-

gram may be used if it is desired to check the relay storage units.

Another printing program is:

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
0	0	0	2	1	151	6	2	161	0	02	01
Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
2	3	010	2	4	011	4	5	012	5	15	02

This program assumes that numbers to be printed are already in relay storage units **120**, **122**, and **123**. In carrying out the program, the number in relay storage unit **151** (Q*r*) is transferred after a shift of ten places to the right to relay storage unit **121** (R*r* being 161) and the printer is called into operation to print the numbers in units **120**, **121**, **122**, and **123**. The second half of the program schedules a multiplication, with half correction (see Section 18). The multiplication can take place while the printing cycle is being performed.

A third example is:

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
2	1	120	2	2	121	2	3	123	0	01	01
Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
0	4	162	0	0	0	0	0	0	0	01	02

This program calls for accumulation of the terms in storage units **120**, **121**, and **123** and transmission of their sum to relay storage unit **122** (T*r* is 162), in the manner described in Section 17*b*. Printing will take place under control of code number 162 in T*r* after the sum has been transferred to storage unit **122**. The terms in relay storage units **120**, **121**, and **123** will be printed alongside the sum in unit **122**.

A fourth example is:

Ps	Pb	Pr	Qs	Qb	Qr	Rs	Rb	Rr	SH1	OP1	S1
2	1	010	2	2	011	4	3	120	0	02	01
Ts	Tb	Tr	Us	Ub	Ur	Vs	Vb	Vr	SH2	OP2	S2
2	4	121	2	5	122	4	6	163	0	10	02

The first half of this program calls for addition of numbers in units **010** and **011** and entry of their sum in **120** (see Section 17). The second half of the program calls for multiplication (see Section 18) of factors from **121** and **122** and entry of the product into **123** (V*r* is 163). Since V*r* is 163, the sum in **120**, the factors in **121** and **122** and the product in **123** will all be printed on the same line. This fourth example will be explained below in greater detail.

When signal AT is given to signal the fact that all transmissions called for by preceding program have been completed, heating relay **X1** or **Y1**, as the case may be, is energized (Section 16*b*, Item 37) and closes contacts to heat the In code sequence storage circuits (Figs. 51, 52*a* and 52*b*). Referring to Fig. 52*b*, the heating of the relay storage Unit Ins pyramids causes the R pyramid set at **120** to pick up Unit In **120**, in the manner described in Section 11. The heating of the V pyramid, set at 163, also causes relay storage Unit In **123** to be energized, since the output line **163** is connected to the output line **123**.

For each of the five possible In fields Q, R, T, U, and V, a printer start sequence storage circuit is provided to select the printer for operation under further control of a pilot unit signal P*rSt* (also see Fig. 80*c*). The left-hand side of Fig. 52*b* shows one such sequence storage circuit, as typical. Assume this is the circuit related to field V. In the present example, the code number **163** is in subfield V*r*. Accordingly, with contacts X1*c* or Y1*c* made, a circuit path is closed between the apex of the V*b* tree and a line PRS, as follows: From the apex of the V*b* tree, via say X7*c*, now-closed contacts *s*4*t* (V*s* is 4), contacts *r*800*t*, *r*400*t*, and *r*200*t* all closed because the code number in V*r* is not as high as 200; thence via contacts *r*100*t*, *r*40*t*, and *r*20*t* now all closed because the code number in V*r* is 163 which is between 160 and 169. The circuit path continues to line PRS via *r*10*t*, *r*8*t*, and *r*4*t*, all remaining closed because the code number in V*r* is not above 163. It is seen that the above circuit path is closed when the code number in subfield *r* of an In field is 160, 161, 162, or 163.

The line PRS is common to the printer start sequence storage circuits of all five possible In fields.

The relay storage units **120**, **121**, **122**, and **123**, when selected for sending or receiving data do not produce Forward or Back signals directly in the way described in Section 7. These four relay storage units may each send out a Forward or Back signal only if printer #1 has not started a cycle. The central blade of contacts *bs* of each of these four storage units is not connected directly to the +150 v. line, but is connected to a line *bsp* indicated as a dotted line in Fig. 29. This line connects to one of the lines *bsp* in Fig. 37*a*. If the printer has not been started, then a path is closed from the +150 v. line (Fig. 37*a*) via cam contacts C13, normally closed relay contacts R2*a*, certain safety contacts which need not be explained here, and via plugging to the four lines *bsp* and through contacts *bs* (Fig. 29), if shifted, of Unit Ins **120**, **121**, **122**, and **123**, and through contacts *bs* of the selected Group Ins to buses **81** of the related In bus-sets. Relay storage units **120**, **121**, **122**, and **123** also cannot produce a Forward signal unless the printer has not started operation, because the Forward signal path has to be made via the central blades of the *bs* contacts for these storage units.

Assume the printer unit is in condition to allow Back signals to be produced and that Unit Ins **120** and **123** and Group Ins **3** and **6**, in the selected example have already been energized because of the heating of the In sequence storage pyramids. Back signals will be applied then to pilot units **3** and **6**. Assume the Presense signal also has been applied to the pilot units. Accordingly, in the manner described in Section 17, Item 23*f*, the trigger **33**–3CP (Fig. 80*c*) in each of pilot units **3** and **6** is turned, cutting off **26***a*–3CP to produce the signal RDL. At the same time, **26***a*–3CP acts through **10**–3CP to turn **9**–3CP and **13**–3CP. The turning of **13**–3CP cuts off **14**–3CP to prepare the pilot unit for transmission response to the "3" signal from a scanning spot. The turning of **10**–3CP cuts off **9**–3CP, so that **5** produces the negative Reset signal. The Reset signal cancels the selected relay storage unit. The RDL signal initiates the operation of the Reset Delay counter in Fig. 80*d*. This counter produces, after some 15 ms., the pulse RDL #2 in order to turn **28**–3CP for conditioning **22**–3CP.

When **10**–3CP turned, it cut off **9**–3CP. This caused **5**–3CP to produce the Reset signal. At the same time, **9**–3CP made **1**–3CP conduct and produce the negative signals P*rSt*. In this way, selected pilot units **3** and **6** produce signals P*rSt***3** through contacts *bs* (Fig. 29), if shifted, of Unit Ins **120**, **121**, **122**, and **123**, and through contacts *bs* of the selected Group Ins to buses **81** of the related In bus-sets. Relay storage units **120**, **12** , **122**, and **123** also cannot produce a Forward signal unless the printer has not started operation, because the Forward signal path has to be

made via the central blades of the *bs* contacts for these storage units.

Assume the printer unit is in condition to allow Back signals to be produced and that Unit Ins **120** and **123** and Group Ins **3** and **6**, in the selected example have already been energized because of the heating of the In sequence storage pyramids. Back signals will be applied then to pilot units **3** and **6**. Assume the Presense signal also has been applied to the pilot units. Accordingly, in the manner described in Section 17, Item 23*f*, the trigger **33**–3CP (Fig. 80*c*) in each of pilot units **3** and **6** is turned, cutting off **26***a*–3CP to produce the signal RDL. At the same time, **26***a*–3CP acts through **19**–3CP to turn **10**–3CP and **13**–3CP. The turning of **13**–3CP cuts off **14**–3CP to prepare the pilot unit for transmission response to the "3" signal from a scanning spot. The turning of **10**–3CP cuts off **9**–3CP, so that **5** produces the negative Reset signal. The Reset signal cancels the selected relay storage unit. The RDL signal initiates the operation of the Reset Delay counter in Fig. 80*d*. This counter produces, after some 15 ms., the pulse RDL #2 in order to turn **28**–3CP for conditioning **22**–3CP.

When **10**–3CP turned, it cut off **9**–3CP. This caused **5**–3CP to produce the Reset signal. At the same time, **9**–3CP made **1**–3CP conduct and produce the negative signals Pr*St*. In this way, selected pilot units **3** and **6** produce signals Pr*St***3** and **6**. These signals are applied to the correspondingly numbered inputs at the bases of the *b* trees in the printer start sequence storage circuits, one of which is shown in Fig. 52*b*. These trees are set according to digits in the subfields *b* of the fields Q, R, T, U, and V. Depending on the setting of these trees, they route the signals Pr*St* to the apexes of the trees. In the example, the trees *b* for storing the digit in subfields R*b* and V*b* are set at **3** and **6**, respectively. Accordingly, the signals Pr*St***3** and **6** are routed through the R*b* and V*b* trees, respectively. The contacts **X7** or **Y7**, as the case may be, are closed so that they allow the signals to go further. The contacts *s***4***t* of the R and V printer start sequence storage circuits are closed. Accordingly, the signals Pr*St***3** and **6** are routed to the *r* contacts in the R and V circuits. Only number 163 in the subfield V*r* is one of the printer code numbers 160, 161, 162, and 163. Hence, only the V printer start sequence storage circuit passes the signal Pr*ST* to line PRS. This line connects to the same designated line in Fig. 87*a*. The signal Pr*St* is a reduced potential on the line PRS and hence, a circuit is completed through start control relay R**1**, to the +150 v. line which energizes this relay. The relay R**1** closes its points *a* to establish a pick-up circuit through a relay R**2**. Relay R**2** closes its contacts *f*, which together with cam contacts C**2**, establish a stick circuit for relay R**2**.

Relay R**2** opens its contacts *a* in the Back (and Forward) signal feed line but before this, the relay R**1** closes its contacts *b* to maintain the signal line closed. This is done to enable Forward or Back signals to be produced by any three of the relay storage units **120**, **121**, **122**, and **123** which have not been selected by printer codes **160**, **161**, **162**, and **163**. The relay storage unit selected by the printer code may produce its Back signal before the other relay storage units produce their Back or Forward signals. The relays R**1** and R**2** therefore may be energized before all the required Forward and Back signals have occurred, and it is desired to maintain the Back (and Forward) signal feed line, associated with the printer unit, closed until sufficient time has been given for all the Forward and Back signals from relay storage units **120**, **121**, **122**, and **123** to be sent to the selected pilot units. For this reason, R**1** when energized closes contacts R**1***b* to shunt the contacts R**2***a* opened when R**2** is energized.

The relay R**1** will be dropped upon the ending of the signal Pr*St* from the pilot unit selected by the field which also selected the printer for operation. As explained in Section 17, Item 24, when all the conditions for transmission have been produced in a pilot unit, the Reset signal lasts at least 15 ms. It is terminated under conjoint control of turned triggers **28**, Fig. 80*c*, and **16**, Fig. 80*c*. The trigger **28** is turned by the 15 ms. delay RDL #2 pulse and **16** is turned to produce the transmission signal ES to In. When both **28** and **16** are turned, **22** conducts and resets **10**, Fig. 80), thus ending the Reset signal. At the same time, the return of **10**, Fig. 80*c*, ends the signal Pr*St*, so that relay R**1** (Fig. 87*a*) is deenergized.

In the example, signal Pr*St***6** has caused relay R**1** to be energized. When the V**3** signal is given by the scanning spot V (Fig. 78*h*), the remaining condition for causing selected pilot unit **6** to produce transmission signal ES**6** to In has been met. Assuming pilot unit **6** also has produced its RDL #2 pulse, the signal Pr*St***6** ends, so that relay R**1** is deenergized. At this stage, the scanning sequence has been completed, the accumulation scheduled by the first half of the program line has been completed and the sum transferred during the R IC step into relay storage unit **120**. The multiplication called for by the second half of the program line has been completed and the transmission signal has been given to transmit the product into the relay storage unit **123**, selected by code number **163** in subfield V*r*. The return of **10**, Fig. 80*c*, to end the Reset and Pr*St* signals also has turned **11** to initiate operation of the TR delay counter in Fig. 80*d*. After a 7½ ms. delay, this counter ends the transmission signal, by which time the result has been safely entered in the selected relay storage unit.

Relay R**1** (Fig. 87*a*) was dropped 7½ ms. before transmission ended, as described above. The printer unit operates at the rate of 150 cycles a minute, so that more than 50 ms. elapses between start of a printer cycle and the "9" readout interval, which is the first in the cycle. Accordingly, it is safe to clutch in the printer for a cycle when relay R**1** is dropped.

The clutch magnet circuit is established from ground via cam contacts C**3**, now-reclosed contacts R**1***c*, now-closed contacts R**2***b*, now-closed contacts STD*ad*, and through clutch magnet PRM, to the +50 v. line.

A print cycle now occurs to cause the results in relay storage units **120**, **121**, **122**, and **123** to be printed, in the manner described before.

Several lines of sequence may be run off during the time taken by the print cycle. However, if the next line of sequence following the one which called the printer into operation also schedules the printer for operation, such next line of sequence will not be completely run off until the printer has finished setting the types to print the results last put into storage units **120**, **121**, **122**, and **123**. This is because the Back signal feed line from the printer will be open after relay R**2** has been energized and relay R**1** dropped. At that point, the print cycle also be-

gan. Neither Back nor Forward signals now can be produced by storage units 120, 121, 122, and 123. Cam contacts C2 open at 18 degrees index time, so that the stick circuit of R2 breaks. But cam contacts C13 in the signal line open before relay R2 is dropped, so that closure of contacts R2a does not reestablish the Back and Forward signal feed path. At 162 degrees of the cycle, after the types for printing the results have all been set, contacts C13 reclose and allow the signal feed path to reclose. It is possible now to send Back signals from storage units 120, 121, 122, and 123 to the pilot units. The pilot units may, in response, send new Reset signals to these units and a selected one of the pilot units may send out a signal PrSt. The storage units may be safely reset at this time because their data have been read out and the types have been set accordingly. New data may be read into these units now. The new signal PrSt may operate now to pick up R1. The clutch magnet circuit will be opened when cam contacts C3 remake at 210 degrees index time, and so the printer unit may continue to perform a second cycle for printing the new data entered into any one or all of the storage units 120, 121, 122, and 123.

23. *Signal data, the drain circuit, control desk, and the pluggable number storage*

Three signals are necessary to restart of a commutator run. These are the all-entry delay signal AED, sequence transmission delay signal STRD1, and the scanning finish signal FC.

The signal AED (Section 16b, Item 27).—Signal AED indicates that some 15 ms. have elapsed since signal AE was given to manifest the fact that all entries into electronic storage were completed during a commutator run. The STRD1 signal is given approximately 30 ms. after the start of sequence transmission. Sequence transmission, as described in Section 16b, Item 31, is timed by signal SW which is initiated under control of the signal AE. Therefore, signal AED precedes signal STRD1 by approximately 15 ms. and in no way affects the time of commutator restart. The purpose of using signal AED as a condition to commutator restart is to provide an early check against operations involving the phasing circuits for the heating relays X2 to X6 and Y2 to Y6 of the Out sequence storage circuits. By the phasing circuits is meant the circuits for controlling the alternation in operation of the A side relays X2 to X3 and the B side relays Y2 to Y6. The phasing circuits for these relays involve the triggers 22 and 28 in Fig. 75e. These triggers must be in relatively opposite states in order to cause the A or B side heating relays for the Out sequence storage circuits to be energized. To begin with, both triggers are in the reset status. The first STR signal turns 28 (Section 16b, Item 9), and the triggers 22 and 28 are then in such relatively opposite states as to conjointly control the phasing circuits to pick up the A side relays X2 to X6. The next AE signal reverses 22 (Section 16b, Item 28) and the triggers 22 and 28 are then in the same, turned state, with the result that the X2 relay is deenergized. Also, the AE signal causes the heating relays X3 to X6 to be deenergized. The following STR signal returns 28, Fig. 75e (Section 16b, Item 36). Now, both 22 and 28 are in relatively opposite states which are also reverse to the previous opposite states. Consequently, the phasing circuit is in condition to cause the B side relays Y2 to Y6 to be picked up. It is evident that both the AE and STR signals are necessary to the proper control of the alternation or phasing of the heating relays for the Out sequence storage circuits. It is necessary to have some assurance that these signals have reached the control frame. If the signal AE is lost at the control frame, it is clear that the phasing circuits will not operate correctly even if the STR signal later reaches the control frame. If the delay signal AED were not used as a condition to commutator restart, then the STRD1 signal and the FC signal would conjointly restart the commutator although an error had occurred. By utilizing the signal AED as a condition to commutator restart, the fact that the signal AE is lost at the control frame would produce a block on commutator restart.

Signal STRD1 (Section 16b, Item 12).—This signal is a timing signal for commutator restart as well as a check signal. It occurs about 10 ms. after signal STR. At the time the STRD1 signal is produced, the AE signal is expected to have dropped out the heating relays for the active side of the Out sequence storage circuits and, consequently, all the old Forward signals have been removed. Also, the STR signal has occurred and has caused the heating relays for the other side of the Out sequence storage circuits, including the heating relay for the S1, S2 pyramids, to be energized so that new Forward signals will be issued. Therefore, it is safe now to produce a new signal OCO (which follows commutator restart) for acting in conjunction with the new Forward signals to time the piloting of entries into electronic storage from Out bus-sets.

Signal FC (Section 16b, Item 26–2).—This signal is an indication that the scanning sequence performed by the commutator spots P, Q, R, T, U, and V (Figs. 78c to *h*) during a commutator run has been completed. Therefore, as far the scanning sequence is concerned, a new commutator run may start.

Presense signal NPR (Section 16b, Items 21 and 23).—As the name indicates, this signal affords advance conditioning of a pilot unit selected to pilot transmission from electronic storage to a selected receiving unit. Signal NPR lasts for only a single AP pulse cycle. But the effect of the signal is stored in the selected pilot unit by reversing triggers 29 and 30 in 3CP (Fig. 80c) of the pilot unit. The stored presense signal in conjunction with the Back signal from the selected receiving unit initiates operation of the pilot unit to produce the Reset signal for resetting the receiving unit before the pilot unit normally is ready to pilot the data transmission to the receiving unit (see Section 17, Item 24).

The presense signal is given under control of the all-transmission delay signal ATD (see Section 16b, Item 38) no sooner than two AP pulse cycles after the start commutator signal SCM (see Section 16b, Item 21). Prior to this, the signal AT will have dropped out the heating relay X7 or Y7 of the In sequence storage circuits (see Section 16b, Item 37). Hence, a new Presense signal will not coact with an old Back signal to control the selected pilot unit for producing the Reset signal and to condition the pilot unit for transmission in response to the "3" signal from an IC scanning spot of the commutator. The start commutator signal SCM originates the *a* or *b* heating signals for the pilot units selection trees. The Presense signal does not occur sooner than two AP pulse cycles later, which provides adequate time for dissipation of

cross-talk produced upon the heating of the Presense trees (Fig. 55).

Signal FSR.—As indicated in Section 16*b*, Item 24*a*, this signal turns all the triggers **7**, Fig. 80*b*, to condition the Forward signal delay counters to respond to Forward signals. Normally, the signal FSR does not occur until all three conditions for commutator restart have been met (see Section 16*b*, Item 39). When these three conditions are met, **14**W (Fig. 78*i*) conducts, and not only turns **15**W, but also returns **24**W from its previously turned state (see Section 16*b*, Item 24*a*). The next AP pulse again turns **24**W, causing it to reverse **29**W, for one AP pulse cycle, so as to produce signal FSR. Obviously, a Forward signal is not usable until the signal STRD**1** (one of the timing signals for commutator restart) has been given, as the Group and Unit Out relays selected upon the heating (timed by the signal STR; see Section 16*b*, Item 36) of the Out sequence storage circuits may still be in the process of picking up. Therefore, until the Forward signal line (bus **81** of an Out bus-set) is expected to receive a true Forward signal, the Forward signal delay counter is held ineffective to accept a voltage on the Forward signal line as a Forward signal. By rendering the Forward signal line ineffective to actuate the Forward signal delay counter until at least the signal STRD**1** has been given, the possibility is reduced of an advance of the Forward signal delay counter by a stray pulse that might appear on the Forward signal line concurrently with an AP pulse. If the delay counter were allowed to advance under control of an extraneous pulse on the Forward signal line, the desired delay between the appearance of a true Forward signal and the production of the signal FSD would be shortened. By holding back the signal FSR until after the signal STRD**1** has been given, sufficient time is provided for transients on the Forward signal line to disappear before the Forward signal delay counter is ready to accept a Forward signal.

Should the scanning completion signal FC appear after the STRD**1** signal, as may be the case if a large capacity calculation such as multiplication or division is performed, the Forward signals associated with the next line of sequence may arrive at the pilot units before signal FC is given. If the Forward signal delay counters were in condition to accept the Forward signals, then the Forward signal delay pulses FSD would be produced and would turn **25**, Fig. 80*b*, so as to set up the entry interlock (see Section 16*b*, Item 24*b*, and Section 17, Item 15*b*). However, the signal FSR will not be given until all conditions for commutator restart have been met, including the condition that the signal FC shall have been produced, so that the Forward signal delay counter will not be in condition to accept Forward signals even though such signals may have been applied to the pilot units as a result of the STR signal having been given before the signal FC. In the absence of this precaution, the entry interlock would operate to prevent the signal T**1** or U**1**, for example, from functioning to produce the signal ES to Int required for a yet uncompleted scanning sequence (see Section 17, Item 26).

It may be noted that the signal FSR operates on all eight pilot units to turn their triggers **7**, Fig. 80*b*, while the return of these triggers by the Forward signal delay counters is on an individual pilot unit basis. Hence, if a pilot unit is not used in one run for piloting Out code data but is to be so used in a subsequent run, its trigger **7**, if left unrestored, would allow the Forward signal delay counter to accept stray pulses as Forward signals. To avoid leaving any triggers **7** in turned status, the signal AE acts to reset all the triggers **7** (see Section 17, Item 15*d*). Therefore, the Forward signal receiving circuits are open to acceptance of signals only for the period starting with signal FSR given shortly before signal OCO and ending with signal AE which indicates that all entries required for a commutator run have been made from the Out buses to electronic storage.

Signal AT.—This signal has been discussed in previous Sections 16*a*, 16*b*, and 17. The signal AT may be delayed if transmission called for by an In field during a run has not been completed because of a lagging Back signal, for example. Thus, if a printer cycle (Fig. 86) is taking place, a new commutator run may have set up two of the conditions for a new transmission to a storage unit which is associated with the printer unit. However, until the cam contacts C**13** reclose at 162 degrees cycle time, a Back signal will not be given (see Section 22*a*) and so the third condition for transmission (Section 17, Items 23 and 24) will be lacking. Therefore, the signal AT will be delayed. Meanwhile, a new commutator run may start (see the last portion of Section 17). However, the pilot unit which has been locked up for transmission will be unable to produce signals Out to ES, ES to Int, or Int to ES because the signal TR Ink will still be effective (see also Section 17*a*).

Although absence of the signal AT required by a commutator run does not prevent a next commutator run from starting, it does prevent a second next run from starting. This is because the signal ATD is required in order for the presense signals SPR and NPR to be produced (see Section 16*b*, Items 21 and 38) for the new run. Since the signal SPR is not given, sequence transmission during the new run is delayed (see Section 16*b*, Item 23 and Section 17, Item 23*f*). Hence, a new signal STR will not be given and the delay signal STRD**1** will not occur, and so this condition for a following run will not be present. In this way, the commutator is prevented from getting too far ahead of transmission.

The drain circuit.—This circuit may be used, when desired, to stop the machine if signals STR do not follow one another within a chosen limit of time. The signal STR indicates that a new line of sequence has entered sequence storage. The time between successive signals STR varies according to the source of the sequence data and according to the nature of the calculations being performed and whether or not printing is being effected. Elapsed time between signals STR usually is from about 20 to 40 ms. but if printing is taking place, the elapsed time may be about 400 ms. It may be desired to stall the machine if the elapsed time between STR signals exceeds, say, 15 seconds. For this purpose, the drain circuit may be put into use.

The drain circuit includes a gas tube **8**, Fig. 77*a*, which is shunted by a pair of parallel 5 mf. condensers, suitable resistance being provided between the anode of tube **8** and the condensers, and between the tube anode and the +150 v. line. The constants of this circuit are so chosen that the condensers will be charged sufficiently in

15 seconds to apply effective voltage to a cathode follower tube 3 to make this tube conduct. If the STR pilot signal (negative) is given less than 15 seconds after the preceding STR signal, it will cause the tube 8 to conduct and drain the condensers before they can render the tube 3 conductive. The STR pilot signal is inverted by 6*a*, Fig. 78k, to a positive pulse which is applied via a capacitor to the grid of cathode follower tube 3*a*, Fig. 77*a* . The tube 3*a* thereupon renders tube 8, Fig. 77*a*, effective to drain the 5 mf. condensers. If this action does not occur in time, the tube 3 will be made conductive and cause tubes 9, 9*a* and 13 to produce reduced potential on the line Stall. Reduced potential on this line establishes an energizing circuit through a relay STL (Fig. 77*aa*). The relay thereupon shifts its contacts *a*, connecting the +150 v. line to the line Stop. This line connects to point *b* of start and stop trigger 5, Fig. 77*a*, and when increased potential is applied to point *b* of the trigger it is actuated to the "stop" status, shown in Fig. 77*a*. Hence, just as when this trigger is brought to this status by the operation of the stop key switch SP (Fig. 77*aa*), the tube 18*a*, Fig. 78*k*, is cut off to apply increased potential to a grid of 14, Fig. 78*k* (see Section 16*b*, Item 14). If this occurs before the SE signal, then 9, Fig. 78*k*, still is in turned state and conditioning 14 to conduct when 18*a* is cut off. If the SE signal has already been given, then 9 is in reset state (Section 16*b*, Item 29). The next STR signal will turn 10 and the later STRD1 signal will return 10, causing it to turn 9, at which point the tube 14 will conduct and restore 17. As a result, the commutator will be unable to respond to the next STR pilot signal and the machine will stop because a new STRD1 signal will not appear.

To reset the drain circuit, the start key switch SKS must be closed. The points *b* of the relay SKR close and apply voltage from the +150 v. line to the line Drain, causing a cathode follower 6, Fig. 77*a*, to render 8 conductive so as to drain the 5 mf. condensers.

The control desk (Fig. 1).—The control desk is a manual switching center at which a duplicate of practically every control circuit in the machine may be set up by manipulating switches and keys. The control desk mounts control keys such as the start and stop keys (Fig. 77*aa*); also mounts sets of dial storage such as the set described in Section 8 and shown in Fig. 23, and carries the switches and keys for use in setting up the artificial line of sequence (see Section 11 and Figs. 39 and 40). A keyboard and connections (not shown) are also carried by the control desk and operable to apply desired numbers to relay storage.

Examples of circuits operable from the control desk are shown in Figs. 65*e*, 71*g*, 80*a*, and 80*c* and the tube inputs of such circuit are marked by letters CD. Cancel circuits for the MD calculating unit, the accumulator unit, the denominational shift unit, electronic storage, the main commutator, the pilot units and every other unit desired, may be operated from the control desk as well as automatically. A group of cancel circuits, such as for the MD unit, accumulator unit, denominational shift unit, and main commutator may be operated individually or together at the control desk. Fig. 77*aa* shows the common cancel switch CNC for the group and the individual MD and accumulator cancel switches MD*cnc* and ACC*cnc*. If the switch CNC is opened, all the cancel circuits of the group are operated but if this switch is left closed, the opening of the individual cancel switches places only the related cancel circuits in operation. As respresentative, the control desk cancel control circuit for the MD internal commutator (Section 14) is shown in Fig. 77*aa*. Upon the opening of switch CNC or MD*cnc*, ground is disconnected from the grid input of the tube H18*a* (also see Fig. 65*e*), and the potential from the +150 v. line is effectively applied to the grid input, causing the tube to conduct. Thereupon, just as when H18 is rendered conductive under control of the M–PRE or D–PRE signals (see Sections 14*a* and 14*b*), tube H24 is cut off and applies increased potential to the cancel circuit MDC. As a result, the control triggers, except for those in Figs. 65*a* and *b*, of the internal commutator of the MD unit are reset.

Similarly, the automatic control of any other cancel circuit may be duplicated manually at the control desk.

Fig. 77*aa* also shows the manual control for the Proceed signal which is ordinarly given by the accumulator unit. If, in a tolerance check (Section 17*c*), the sign of the result in the accumulator is negative, the Proceed signal will not be given automatically, and sequencing will be halted. When it is desired to resume operations, this may be done by sending out a Proceed signal under manual control. For this purpose, the switch Proceed CD at the control desk is opened, disconnecting ground from the input of tube 8, Fig. 71*g*, and allowing the potential from the +150 v. line to be effective to render this tube conductive, whereupon the negative Proceed signal is sent to ACC.C (Fig. 78A).

Fig. 77*aa* also shows an example of how a control signal is applied to electronic storage by manipulating a switch at the control desk. Normally, tube 7, Fig. 80*a*, is conductive, so that tube 1, Fig. 80*a*, is cut off and the negative entry signal Out to ES is not present. In the manner described in Section 16*b*, Item 24*b*, the trigger 14, Fig. 80*a*, is automatically reversed, during automatic sequencing, to cut off 7, Fig. 80*a*, whereupon 1, Fig. 80*a*, is made conductive to produce the entry signal Out to ES. This signal may be produced under manual control by opening the switch OES at the control desk, thereby removing the +150 v. potential from the input to a grid of pentode 7, Fig. 80*a*. This tube is thereby cut off and causes 1, Fig. 80*a*, to produce signal Out to ES.

Pluggable storage.—Besides the memory or storage units described before, the machine provides pluggable storage as a convenient means for applying constants to the Out bus-sets, to be entered into electronic storage. Several pluggable storage units are provided. Ten of these are designated by code numbers 610 to 619, which may occur in subfields *r* of any Out fields of a line of sequence. Fig. 89 shows a typical sequence storage pyramid for bringing pluggable storage into operation. This pyramid is the same as the Dial Storage pyramid shown in Fig. 47*c* as far as the *r* 10's tree, but extends through this tree to its "1" output. The "1" output is directed to the top of an *r* units tree (see Fig. 88), the ten outputs of which are plugged to ten relays PSG610 to 619. As is understood, there is a similar pyramid for each of the possible Out fields P, Q, R, T, and U and the corresponding outputs of the *r* units trees of these pyramids are commoned. Hence, if any

of these Out fields contains one of the numbers 610 to 619 in its subfield r, the correspondingly numbered relay PSG is energized.

Upon energization of a relay PSG610 to 619, it connects twelve relay contacts a1 to a12 (Fig. 89) of the correspondingly numbered pluggable storage unit to the +150 v. line. The contacts of the respective relays PSG610 to PSG619 are wired to plug sockets PSP610 to PSP619. These sockets are plugged, according to numbers to be applied to Out bus-sets, to plug sockets PSOP. There are eight groups of sockets PSOP, one for each Out bus-set. Each group includes columns 1 to 20 sockets which are wired directly to columns 1 to 20 buses of the related Out bus-set; each group also includes a socket 81 wired to bus 81 of the Out bus-set and plugged for the Forward signal.

Assume, for instance, that pluggable storage unit 610 is to apply the value +787 to Out bus-set 1. Accordingly, as shown in Fig. 89, one of the sockets PSP 610 is plugged to socket 2 of column 1 of group 1 of sockets PSOP in order to provide for the + sign, three of the sockets PSP610 are plugged, respectively, to sockets 4, 2, and 1 in column 18 of group 1 of sockets PSOP, another of the sockets PSP610 is plugged to socket 8 of column 19, three of the other sockets PSP610 are plugged to sockets 4, 2, and 1 in column 20, and in order to send the necessary Forward signal to Out bus 1 along with the number, one of the sockets PSP610 is plugged to socket 81 of the PSOP group 1. Thus, when the code number 610 is in a subfield r of an Out field the related Out sequence storage pyramid (Fig. 88) which receives this number is effective, when heated just prior to a commutator run, to pick up relay PSG610. Consequently, the selected number 787 and a Forward signal are applied to Out bus-set 1.

As further examples, Fig. 89 shows unit 612 plugged to apply number 26 to Out bus-set 2 and unit 614 plugged to apply 5 to Out bus-set 6.

24. *Computed or modified sequence*

For some problems the course and characteristics of the calculations have no deviations and lines of sequence with prechosen sequence and calculation instructions may be used. For other problems the course or character or extent of calculations varies according to computed results and completely preselected sequence lines are not suitable. Through the use of simple computable numbers as sequence instructions and by reason of other features of this machine, lines of sequence and sequence instructions may be computed to steer the course, nature or extent of subsequent calculation. A line of sequence in which one or more instructions are obtained by computation is called here a modified line of sequence. Some cases in which modified sequence is employed are given below.

Case 1. A computed selection of the sequence path.—Since a line of sequence determines the calculation path this case also may be referred to as involving a computed choice between two or more paths down which subsequent calculations will follow. The selection of the sequence path or calculation path is controlled by the S1 and S2 code numbers. This case therefore deals with the computation of the S1 and S2 code numbers. One application of this case is in problems including iteration, and as will be seen, the result of the iteration operations not only determines which path of calculation is to follow but also the length of the calculation program. As an example, the sequence path for the iteration may be considered as made up of successive lines of sequence on tapes. In this iteration program to be taken as an illustration, only five lines of sequence are required and this series of five lines may be repeated twelve or more times on the tapes. This is done for mechanical expediency and to save the time which would be used up in backing the tapes to return to the first line if only a single series were to be used.

The iteration program is to be repeated until a stable condition is reached, as is done for instance to obtain a square root by the Newton formula:

$$X=\tfrac{1}{2}\left(X+\frac{N}{X}\right)$$

As an example, suppose it is desired to solve

$$r,=\frac{-b+(b^2-4ac)^{\frac{1}{2}}}{2a}$$

where (b^2-4ac) is N.

Typical sequencing is explained below and constants and plugging will be explained in connection with the sequence lines.

P			Q			R			SH1	OP1	S1	T			U			V			SH2	OP2	S2
s	b	r	s	b	r	s	b	r				s	b	r	s	b	r	s	b	r			
2	1	010	2	2	010	4	3		4	15	32	2	4	012	2	5	013	4	6		0	10	31
		(b^2)												(4a)									

The left half of this line calls for $-b$ in storage unit 010 to be multiplied by itself, for b^2 to be rounded off and shifted four places to the right and for the shifted result to be sent to ES3. The second half of the line calls for multiplication of constant 4 in unit 012 by the term a in unit 013 and for $4a$ to be sent to ES6. The respective S1 and S2 numbers 32 and 31 select the next line of main sequencing for the problem.

P			Q			R			SH1	OP1	S1	T			U			V			SH2	OP2	S2
s	b	r	s	b	r	s	b	r				s	b	r	s	b	r	s	b	r			
2	6		2	1	011	4	2			10	22	2	3		1	2		4	5	128	4	04	21
			(4ac)												($b^2-4ac=N$								

The left half of the second line instructs the machine to multiply $4a$ in ES6 by the term c in storage unit 011, and to take the product and store it in ES2. The right half of the line calls for subtraction from b^2 now in ES3 of $4ac$, and for half correction and shift of the result followed by its entry into ES5 and transmission to storage unit 128. The result b^2-4ac is the number N in

the Newton formula. The S1 and S2 numbers call in the iteration sequence:

ITERATION SEQUENCE FOR SQUARE ROOT

P	Q	R	SH1	OP1	S1	T	U	V	SH2	OP2	S2
s b r	s b r	s b r				s b r	s b r	s b r			
2 5 031 (X_i)	2 6 128 (N)	4 2 032 (N/X_i)	8	25	22	2 2	2 5 (X_i+N/X_i)	4 3 033		02	21
2 3 $\{(X_i+N/X_i)/2\}=X_{i+1}$	2 4 614	4 5 129	1	15	22		2 5 $\{X_{i+1}/10^5\}$=tolerance (t)	4 1 100	5	04	21
2 5 ($X_{i+1}-X_i$)=difference (d)	1 4 031	4 2 034		02	22	2 1 ($t-d$)=+ or −	3 2	6 3 157	9	02	21
2 5 157 (±5+27)=32 or 22	2 3 613	4 1 152		02	22	2 2 612	2 5 (26±5)=31 or 21	4 4 153		02	21
					52		2 5 129 (X_{i+1} to unit 031)	4 5 031		02	53
					32 or 22						31 or 21

X_1, a first guess, has been preliminarily put into storage unit **031**. The number N has been calculated by the first two run-off lines of main sequence and transmitted to storage unit **128**. The first line of the iteration sequence directs the machine to obtain N/X_i and enter the shifted result into ES2, then to take X_i from ES5 to which it has been sent from unit **031** and add it to the result in ES2, thereby obtaining X_i+N/X_i which is put into ES3.

The second line, first half, of the iteration sequence multiplies the result X_i+N/X_i of the previous run by 5 taken from pluggable storage (see Section 23) and shifts the product one place to the right, which is equivalent to dividing by 10, so that the result sent to ES5$=(X_i+N/X_i)/2$. This is the first calculated approximation of the square root and is denoted by X_{i+1}, which is to be used to obtain a tolerance. The tolerance is computed in the second half of the sequence run by shifting X_{i+1} five places to the right, which is equivalent to dividing it by 10^5, and sending the answer, which is the tolerance t, to ES1.

The third line of the iteration sequence controls the machine to subtract X_i, in storage unit **031**, from X_{i+1}, which was put into ES5 during the run-off of the first half of the second line of the iteration sequence; and to subtract from the tolerance t in ES1 the absolute value of the difference d between X_{i+1} and X_i, then to shift the result of $t-d$ nineteen places to the right. This discards the numerical value of the result and leaves only the sign of the result to be sent to ES3 from the sign storage triggers **2M** and **6M** (Fig. 78*a*). If the difference d is within the tolerance t, then $t-d$ is plus but if d is greater than t, the result is minus. The + or − sign is transmitted from ES3 to column 1 of relay storage unit **157**. This storage unit has been preliminarily plugged for its two halves to be reset and receive data independently (see Section 7). The reset plugging is from socket **82** of 7RS–GIP3 (see Figs. 29, 30, and 90) to socket **82** of 7RS–GIPP and from socket **82** of 7RS–GIP1, for example, to socket **84** of 7RS–GIPP. The entry plugging is such as described in Section 7, in this case, column 1 sockets **2** and **1** only, of 7RS–GIP3 need be plugged to column 1 sockets of 7RS–GIPP while column 20 sockets of 7RS—GIP1 are plugged to column 20 sockets of 7RS–GIPP. Only the left half of the relay storage unit **157** will be reset by the Reset signal applied to bus **82** of In bus-set **3** during the IC step of the V spot (Fig. 78*h*) in the running off of the third line of the iteration sequence. Thereafter in the same V IC step the sign of the result of $t-d$ is entered in the left-hand column of the left half of relay storage unit **157**, in the manner understood from Section 17, Item 24. Preliminarily, the constant 5 has been entered in the right-hand column of the right half of this storage unit through the plugging shown in Fig. 90. Since only the left half of the storage unit now has been reset, the right half remains set with 5 in the right-hand column.

Now standing in relay storage unit **157** is ±5. Pluggable storage (see Section 23) has preliminarily been set to apply number **27** to Out bus-set **3** when called on to do so. The Q field of the fourth line of the iteration sequence directs the machine to enter **27** from pluggable storage to ES3. The P field of this line directs the number in relay storage unit **157** to be entered in ES5. The plugging between 7RS–GOP5 and 7RS–GOPP to allow the entire relay storage unit **157** to be read out to Out bus-set **5** is shown in Fig. 90. It is seen that although the two halves of a storage unit may separately receive data, they may be plugged to apply their data to the same Out bus-set or to separate Out bus-sets. The addition of ±5 and **27** occurs in the P OC and Q OC steps of the fourth run in the iteration sequence. In the following R IC step, the result **32** or **22** is transmitted to relay storage unit **152** (see Section 17, Item 24). In the T OC step the constant **26** is directed from pluggable storage to ES2 and thence to the accumulator, after which the number ±5, which was sent to ES5 by unit **157** during the P OC step, is applied to the accumulator during the U OC step. The accumulation of **26** and ±5 occurs and the result **31** or **21** is transmitted during the V IC step to relay storage unit **153**.

Now present in relay storage units **152** and **153** are computed S1 and S2 numbers.

The fifth line of the iteration sequence bears the S1 number 52 and the S2 number 53. The S1, S2 pyramids are set with these numbers during the fifth commutator run of the iteration sequence. The sockets SGP52 and **53** are preliminarily plugged to RSGP1–2 and 8–3, respectively, as shown in Fig. 53*b*. The sockets SUP52 and **53** are plugged to sockets RSUP**152** and **153**, as shown in Fig. 53*a*. Accordingly, the relay storage units **152** and **153** are called to read out a line of sequence to Out bus-sets **7** and **8**. This line of sequence consists of the computed S1 and S2 numbers obtained during the iteration sequence. In order to apply these numbers to the S1 columns 19 and 20 of Out bus-set **7** and to the S2 columns 19 and 20 of Out bus-set **8**, plug-

ging, as shown in Fig. 90, is between columns 19 and 20 of sockets 2RS–GOPP and 2RS–GOP7 and between columns 19 and 20 of 3RS–GOPP and 3RS–GOP8 (see Fig. 90). Hence, in the fifth commutator run of the iteration sequence, the next, computed line of sequence is called out from relay storage units 152 and 153 and transmitted to sequence storage (see Sections 16*b* and 17).

The computed line of sequence just transmitted to sequence storage comprises S1 number 32 and S2 number 31 if the first calculated approximation X_{i+1} and the first guess X_i do not differ from each other by more than the tolerance *t*. This means that the square root of N has been calculated to the required degree of accuracy and so the main sequencing path may be resumed for the continuation of the main calculation of *r*,

$$=\frac{-b+(N)^{\frac{1}{2}}}{2a}$$

On the other hand, if the computed S1 and S2 numbers are 22 and 21, then the difference *d* between the first calculated square root and the first guess is greater than the tolerance *t*. In that event, the iteration sequence is repeated. During the running off of the fifth line of the iteration sequence, the first calculated square root X_{i+1}, obtained in the running off of the second line of the iteration sequence, was transmitted from relay storage unit 129 to unit 031 (see Section 17*a*), and so has replaced the first guess for the next iteration sequence.

In the foregoing manner, the iteration sequence will be run as many times as necessary to obtain a square root to the required accuracy, and when this has been done, the computed S1 and S2 numbers will be 32 and 31 and will direct the stream of calculation into the main path. Assuming this has been done, the line of sequence selected by the computed S1 and S2 numbers 32 and 31 is, for example:

P	Q	R	SH 1	OP 1	S1	T	U	V	SH 2	OP 2	S2
s b r	*r b r*	*s b r*				*s b r*	*s b r*	*s b r*			
2 1 010	2 2 031	4 3		02	32	2 4 013	2 5 603	4 6		10	31
$(-b)+(b^2-4ac)^{\frac{1}{2}}$						(*a*) times (2)					
2 6	2 3	4 1 160		20	01					02	

The first of the above two lines directs the addition to $-b$ of the square root obtained by the iteration sequence, and also the multiplication of the term *a* by the constant 2 taken from dial storage. The second of these lines directs the division of $-b+(b^2-4ac)^{1/2}$ by $2a$ and the printing of the answer *r* (see Section 22*a*).

An alternate method of computing the sequence path may be used. The alternate method requires one less line in the iteration sequence. The first three lines of the iteration sequence will be the same but 5 will not be present in relay storage unit 157. Accordingly, at the end of the third commutator run in the iteration sequence, the unit 157 will contain only the + or − sign in column 1. Preliminary plugging will be, for example, as shown in Fig. 90*a*. Column 1 plug socket 2 of 7RS–GOPP will be plugged to sockets 1 of columns 19 and 20 of 7RS–GOP7 and also to socket 1, column 19 and socket 2, column 20 of 7RS–GOP8. Socket 1, column 1 of 7RS–GOPP will be plugged to sockets 2 in columns 19 and 20 of 7RS–GOP7 and to sockets 2 and 1 in columns 19 and 20, respectively, of 7RS–GOP8. Accordingly, if Unit Out 157 and relay storage Group Outs 7 and 8 are operated, storage unit 157 will apply numbers 11 and 12 to the S1 and S2 columns of Out bus-sets 7 and 8, respectively, if the storage unit contains the computed + sign indicant 2; if the computed sign is −, as represented by energization of relay 1, column 1, then the storage unit will apply the S1 and S2 numbers 22 and 21 to Out bus-sets 7 and 8.

The fourth line of the alternate iteration sequence will be the same as the fifth line of the first iteration sequence but instead of 52 and 53 in S1 and S2 will contain 57 in both S1 and S2. The socket SGP57 will be plugged as shown in Fig. 53*b* to sockets RSGP7–7 and 8–7 and socket SUP57 will be plugged, as shown in Fig. 53*a* to socket RSUP157. Accordingly, in the fourth commutator run in the alternate iteration sequence, the S1 and S2 numbers will be obtained from storage unit 157 and transmitted to sequence storage. If the S1 and S2 numbers thus obtained are 22 and 21, the iteration sequence (alternate one) will be repeated, but if the S1 and S2 numbers are 11 and 12, the main calculation path will be selected in order to proceed with the problem. Continuation of the main path of the calculation need not be sequenced from the same sources which sequenced the calculations preceding the iteration. Therefore, the S1 and S2 numbers in the first part of the problem may be 32 and 31 while the computed S1 and S2 numbers for continuation of the problem after the iteration may be 11 and 12.

Case 2.—Computing the calculation instruction.—This case determines, as a result of a computation, which subsequent arithmetical operation shall be called for by an OP field of a sequence line.

As an example, the expansion of the series for the arc tangent function is accurate only to "Pi/4" (arc tan 1). For values lying in the second octant (X between Pi/4 and Pi/2), the reciprocal of the argument is used, which is equivalent to computing the arc cotangent. A computation is made to determine whether the argument is greater or less than 1. If the argument is less than 1, the sequence instruction for a multiplication is delivered to sequence storage, and the argument is multiplied by 1, after which it is used in the series expansion. If the argument is found to be greater than 1, the sequence instruction for division of 1 by the argument is delivered to sequence storage, and the reciprocal of the argument which is thereby obtained is used in the series expansion. The final answer, in the latter event, is adjusted by Pi/2.

An illustrative program is explained below.

P			Q			R			SH 1	OP 1	S1	T			U			V			SH 2	OP 2	S2
s	b	r	s	b	r	s	b	r				s	b	r	s	b	r	s	b	r			
			2	1	610	4	4	017		02	01	1	2	011	2	3	013	6	1	017	9	02	02
2	5	017	2	2	103	4	6	152		02	01	2	1	610	1	5		4	1	031	3	02	02
2	1		2	5	603	4	5	032		10	52												02
2	1	013	2	3	612	4	3	018	7	15 or 25	01	2	3		2	4	613	4	4	019	7	15	02
2	4		2	5	614	4	5	020		02	01	2	5		2	3		4	4	021	7	15	02
2	4		2	6	615	4	5	022		02	01	2	5		2	3		4	4	023	7	15	02
2	4		2	1	616	4	5	024		02	01	2	5		2	3		4	4	025	7	15	02
2	4		2	2	617	4	5	026		02	01	2	5		2	3		4	4	027	7	15	02
2	4		2	3	618	4	5	028		02	01	1	5		2	6	032	4	1	029		02	02

All plugging for this problem is standard except that relay storage unit **017** is plugged to receive entries separately in its two halves and to read out data as a unit, in the manner described for unit **157** in Case 1.

The first sequence line, S1Seq part, directs +500 to be transferred from pluggable storage unit **610** to the right half of unit **017**. The S2Seq part of the first sequence line directs a comparison to be made between X, the argument, and 1. The argument X is in relay storage unit **013** to a known number of decimal places. The constant 1 is in relay storage unit **011** to the same number of decimal places. The comparison of X to 1 is made by entering 1 from unit **011**, with a — operational sign, into the accumulator and then algebraically adding X. The algebraic sum is a positive or negative number, depending on whether X is greater or less than (also equal to) 1. The algebraic sum is shifted nineteen places to the right to discard the numerical portion and the sign + or — is transmitted to column 1 of the left half of storage unit 017. Now standing in unit 017 is ±500 with + or — in column 1 and 500 in columns 18, 19, and 20.

The second sequence line, S1Seq part, directs the algebraic addition of ±500 in unit **017** to the number taken from relay storage unit **103**. The number in unit **103** is the same as the S1Seq part of the fourth sequence line except for OP1 columns 17 and 18 which are to be computed. This computation will be pe performed by algebraically adding ±500 to the number in unit **103**. If X is less than 1, then —500 stands in unit **017** and when added to the number taken from unit **103**, the result is the data of the S1Seq part of the fourth sequence line with 15 in the OP1 field. If X is equal to or greater than 1, + 500 is in unit **017** and when added to the number in unit **103**, the result is the S1Seq part of the fourth sequence line with 25 in the OP1 field. Thus, either of the following computations is effected in the run-off of the second sequence line:

Columns	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
(103)	2	1	0	1	3	2	3	6	1	2	4	3	0	1	8	7	2	0	0	1	
(017)																		+5	0	0	
	2	1	0	1	3	2	3	6	1	2	4	3	0	1	8	7	2	5	0	1	or
Columns	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
(103)	2	1	0	1	3	2	3	6	1	2	4	3	0	1	8	7	2	0	0	1	
(017)																		−5	0	0	
	2	1	0	1	3	2	3	6	1	2	4	3	0	1	8	7	1	5	0	1	

The computed line of sequence thus has 15 or 25 in columns 17 and 18 which are in the OP1 field. This line of sequence which is produced in the accumulator during the run on the S1Seq part of the second sequence line is transferred to relay storage unit **152**.

The S2Seq part of the second sequence line directs the algebraic addition of 500, taken from pluggable storage unit **610** (also see the Qr subfield of line 1) to ±500 taken from ES5 which received the latter number from unit **017** during the run on the S1Seq part of the second sequence line. The result is either 0000 or 1000 in the accumulator and is shifted three places to the right to leave either 0 or 1 in the 20th column of ES1 and relay storage unit **031**. The purpose of this operation is to determine whether or not the ultimate answer of the series expansion is to be corrected by Pi/2. If —500 is in ES5, as received from unit **017** when X is found to be less than 1, the result of the run on the S2Seq part of the second sequence line is 0 and the correction will not be made. But if X is equal to or greater than 1, ES5 will receive +500 from unit **017**, and the calculation instructed by the S2Seq part of the second line produces the answer 1 in ES1, as a consequence of which the correction will be made.

The third sequence line, S1Seq part commands the multiplication of the number entered in ES1 during the preceding calculation by Pi/2 which is set in dial storage unit **603**. If 0 is in ES1, then the product is 0 but if 1 is in ES1, the product is Pi/2. The product is transmitted to relay storage unit **032**.

The third sequence line bears the S1 code number 52. The sockets SUP52 and SGP52 (Figs. 53*a* and *b*) will have been plugged, as now understood, to select relay storage unit **152** as the source for S1Seq data. Unit **152** is now storing the computed S1Seq data arrived at during the running off of the first two lines of the program. Accordingly, under control of the S1 code number 52 in the third line of sequence, the S1Seq data from unit **152** is called out to serve as the left half of the fourth sequence line.

The left half (S1Seq part) of the fourth sequence line bears the computed OP1 code number 15 if X has been found less than 1, but

bears the computed OPI code number 25 if X has been found greater than 1. In the former situation, X is to be used to form the argument in the subsequent calculation, while in the latter situation 1/X is to form the argument. The SISeq part of the fourth sequence line directs X to be read out of its storing unit 013 (also see Ur in line 1) to the MD unit (Section 14) to serve as the multiplicand or divisor. The number 1 is set in pluggable storage unit 612. If multiplication is called for (OPI number 15), then 1 is entered in the MD unit to serve as the multiplier factor. If the OPI number is 25, then 1 is entered in the MD unit to serve as the dividend. The answer is transmitted to storage unit 018, after a shift of seven places to the right, to be used as the argument, now denoted by y.

P			Q			R			SH	OP		T			U			V			SH	OP	
s	b	r	s	b	r	s	b	r	1	1	S1	s	b	r	s	b	r	s	b	r	2	2	S2
0	3	010	2	2	281	6	6		4	15	01				2	3		6	3		6	02	02
2	6		2	1	281	4	1			02	01				2	3		5	5	011	4	02	02
2	1		5	6	012	1	3		6	02	01		3	019	2	4	614	4	4	019	1	01	02
2	1	013	2	5	019	0	2	011		01	01		4	157								01	02
											57												
2			2	6		4 or 5	1	014	5	02	01												02

The right half of the fourth sequence calls for multiplying argument y, now in ES3, by a constant, denoted by A, taken from pluggable storage unit 613. The product Ay is entered in ES4 and stored in unit 019 for checking purposes.

The fifth line, SISeq part, directs the calculation $Ay+B$, where B is a constant taken from pluggable storage unit 614. The sum is entered in ES5, and also in unit 020 for checking purposes. The fifth line S2Seq part, directs $Ay+B$, in ES5, to be multiplied by y, in ES3 (see the fourth line) and the product Ay^2+By is entered in ES4.

The sixth, seventh, and eighth lines, and the left half of the ninth line continue the calculation of the series. At the end of this calculation, the result standing in ES5 is:

$$Ay^5+By^4+Cy^3+Dy^2+Ey+F=\text{arc tan } y$$

The ninth sequence line, right half, directs the correction of arc tan y if, as a result of X having been found greater than or equal to 1, the value Pi/2 has been stored in unit 032 during the run on the left half of the third sequence line. The computed result arc tan y is entered in ES5 during the run on the left half of the ninth sequence line. The right half of this line directs the subtraction of this computed result from the value in unit 032. If X was found less than 1, then 032 stands at zero and the final result is arc tan $X=$arc tan y. On the other hand, if X was greater than or equal to 1, then 032 stands at Pi/2 and the final answer is arc tan $X=Pi/2-$arc tan y. The final answer is transmitted via ES1 to relay storage unit 029.

Case 3.—Computation of the shift sequence instruction.—This case deals with computation of the sequence instructions for the direction or the amount of shift, or both, to be given by a line of sequence. Such sequence computation may be desired, for example, in the calculation of the anti-log of X. In this calculation, the anti-log of the mantissa is obtained and then shifted to the left, if the characteristic is positive, or to the right, if the characteristic is negative, the extent of shift being determined by the value of the characteristic.

Assume, for instance, that the anti-log $X=5.1231247008109001$ is to be calculated, that X is stored in relay storage unit 010, and that portion .12 of the number already has been used as the computed argument in a table look-up operation (see Section 20) and the functional anti-log differences, here denoted by D_1 and D_2 have been selected from table I. The calculation program continues with:

The first sequence line, SISeq part calls for multiplication of a number derived from storage unit 010 by a number read out of table I of the table look-up unit. During the commutator run on the first sequence line, the 17-place number X in 010 is delivered to columns 4 to 20 of ES3 and its sign is delivered, as usual, to column 1. Also, the first difference D, is delivered from table I to ES2. The MD unit (Section 14) handles factors to a maximum of fourteen places. These factors are applied by Internal bus columns 16 to 29 (Figs. 64*a* and *j*) which receive them from electronic storage columns 7 to 20 (see Section 6). Accordingly, during the P OC step, the fourteen places, of X, to the right of the computed argument are entered in the MD unit to serve as the multiplicand. During the Q OC step, the difference D_1, is entered in the MD unit to serve as the multiplier. The product, which may be designated XD_1, is shifted fourteen places to the right and then delivered to ES 6.

The first sequence line, S2Seq part, directs the machine to isolate the characteristic of X and store it in column 20 of ES3. At the beginning of the first commutator run, X was delivered by unit 010 to columns 4 to 20 of ES3. During the U OC step, X is sent from ES3 to the accumulator unit. In the next, V IC step, X is sent by the accumulator to the denominational shift unit and shifted sixteen places to the right (see Section 17) after which the shifted result is brought into ES3. The shift of sixteen places to the right discards the mantissa of X and locates the characteristic in column 20 of ES3.

The second sequence line, left half, directs XD_1 in ES6 to be added to D_2 which is read out of table I of the table look-up unit to ES1. The result is the anti-log of the mantissa and may be designated as anti-log X_m. This is delivered by the accumulator to ES1.

The second sequence line, right half, has as its purpose the placing of the characteristic of X in the column position 16 occupied by the SH sequence field (see Fig. 38). This will complete the computation of the shift amount which is determined in this example by the value of the characteristic. In the first commutator run, the characteristic was brought into column 20 of ES3. In the second commutator run, right half, it is shifted four places to the left during the V IC step and then delivered by the shift unit to column 16 of ES5 from which it is transmitted to relay storage unit 011.

In the third commutator run, P OC step, anti-log X_m is sent from ES1 to the accumulator. In

the next, Q IC step, the anti-log is read out from the accumulator to the shift unit and shifted six places to the left. The shifted result is delivered to ES6. The purpose of this is to center the anti-log X_m so that it may be shifted to the right or to the left according to the sign of X and the value of the characteristic. It may be assumed that the anti-log X_m has been calculated to seven places and therefore stands in columns 14 to 20 of ES1. It has been shifted now six places to the left into ES6 and therefore stands in columns 8 to 14 of ES6. This allows for a possible shift of six places to the left, if the sign of X is + and the characteristic is 6, or a possible shift of six places to the right, if the sign of X is negative and the characteristic is 6.

Relay storage unit 019 has been preliminarily plugged, in a manner now clear, to receive entries in its left half from In bus-sets 1 and 3, to receive entries in its right half from In bus-sets 2 and 4, and to read out as a single unit to Out bus-sets 5 and 6.

The third sequence line has R as an Out field and T as an In field (see Section 17*a*). ES3 still contains the characteristic in column 20 (see the right half of the first sequence line) and the sign, as is now evident, is in column 1. During the R OC step for carrying out the sequence directions given by the R and OP1 fields of the third sequence line, the characteristic and its sign in ES3 are entered into the accumulator unit. In the next, T IC step, the characteristic and sign are read out of the accumulator, the characteristic is discarded by the shift of one place to the right, and the sign is re-entered in column 1 of ES3 from where it is transmitted to column 1 of split unit 019.

Pluggable storage unit 614 (Section 23) has been plugged to apply digit 5 to column 12 of Out bus-set 4 which is the equivalent of applying number 500,000,000 to this Out bus-set.

The third sequence line, in fields U and V directs the number 500,000,000 to be read out of pluggable storage unit 614 to ES4, and fields SH2 and OP2 direct this number to be routed via the accumulator and denominational shift unit back to ES4. Note that since U is an Out field, the column shift cancel SHCL will not be suppressed, during the next V IC step. Hence, ES4 then contains number 500,000,000 which is transmitted to the right half of split unit 019 where it enters columns 12 to 20. Note that since U is an Out field, the OP.OC signal will be given in the U OC step to reset 26–ACC.C (Fig. 78*a*). Also during the U OC step, 14–ACC.C will be turned to cause the signal RCC to appear (see Section 17). Hence, during the V IC step, the signals SHCL and ACC–RO will not be suppressed, as would be the case if U were an In field following T as an In field (see Section 17*b*). The descending counter in Fig. 27*a* has been stepped back to 0 during the T IC step. Accordingly, there will be no shift in column relation between the number in ES4 and the number transmitted to the right half of unit 019.

Split unit 019 now contains the sign of X in column 1 and the number 500,000,000 in columns 12 to 20.

The computation of the shift instruction is completed in the run on the fourth line of sequence.

Before starting the program, relay storage unit 013 has been set with incomplete S1Seq data. This data will be totaled during the run on the fourth sequence line together with ±500,000,000 produced in relay storage unit 019 during the run on the third sequence line and together with the characteristic which has been put into column 16 of unit 011 during the run on the second sequence line. The accumulated amount will be the computed S1Seq half of the sixth sequence line. Assume, first, the sign of X to be positive. Hence, storage unit 019 will contain +500,000,000 and the accumulation carried out in the P OC, Q OC, and R OC steps of the fourth sequence run will be:

Columns	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
(013)	2	0	0	0	0	2	6	0	0	0	4	6	0	1	4	0	0	2	0	1
(019)												+5	0	0	0	0	0	0	0	0
(011)																+5	0	0	0	0
	2	0	0	0	0	2	6	0	0	0	5	1	0	1	4	5	0	2	0	1

If, instead of a positive sign, X has a negative sign, then −500,000,000 stands in unit 019 and the result of the accumulation differs from the above in that the 11th column of the total contains digit 4 instead of 5.

In the T IC step of the fourth sequence run, the computed total is transferred to relay storage unit 157.

The fifth sequence line has the code number 57 in S1. In a manner now understood, this code number in S1 will call out the computed data from relay storage unit 157 to serve as the S1Seq part of the sixth sequence line.

The computed, sixth sequence line, S1Seq part, directs the number in ES6 to be routed through the accumulator to the shift unit to be shifted to the right or to the left according to whether the computation of sequence has arrived at 4 or 5 in subfield *Rs*, to be shifted 5 places to the right as determined by the computed shift number in SH1 which has been derived from the characteristic of X, and for the shifted result to be delivered to relay storage unit 014 (*Rr*). The anti-log X_m was brought into columns 8 to 14 of ES6 during the Q IC step of the third commutator run. During the sixth commutator run, it is routed through the accumulator and the shift unit and the shifted anti-log is delivered to unit 014. If X is negative, then the computed digit in *Rs* is 4 and the shift unit has shifted the anti-log X_m to the right for five places. This brings the anti-log into columns 13 to 19 of unit 014. Assuming the decimal point to be between columns 7 and 8, the computed anti-log X is a decimal position to thirteen places. If X is positive, then the computed digit in *Rs* is 5 and the anti-log X_m is shifted five places to the left and brought into columns 3 to 9 of unit 014. The computed, anti-log X is then a number having six places to the left of the decimal point and fourteen places to the right of the decimal point.

Case 4.—Computation of sequence instructions for selection of number sources and receiving units.—This case deals with the computation of the instruction numbers for subfields *r* of Out or In fields. The computation of the instruction number for subfield *b* of In or Out fields also will be explained.

One simple application of this case is in a

problem of frequency distribution for statistics. Assume a census is being taken of eight different categories, arrived at by combinations of three out of six sub-categories. The six sub-categories and their code numbers may be, for instance; male (1), female (2), citizen (4), employed (5), unemployed (7), non-citizen (8). The code numbers for eight categories may be obtained by addition of the code numbers of the three-sub-categories applying to individuals, thus:

male citizen employed	(1+4+5)=10
male citizen unemployed	(1+4+7)=12
male non-citizen employed	(1+8+5)=14
male non-citizen unemployed	(1+8+7)=16
female citizen employed	(2+4+5)=11
female citizen unemployed	(2+4+7)=13
female non-citizen employed	(2+8+5)=15
female non-citizen unemployed	(2+8+7)=17

The three sub-categories pertaining to each person may be punched in code into record tapes and accumulated during a commutator run, such as described in Section 17*a*. The result of the accumulation may be entered in two receiving units. An illustrative line of sequence for controlling such a run is:

P			Q			R			SH	OP		T			U			V			SH	OP	
s	*b*	*r*	*s*	*b*	*r*	*s*	*b*	*r*	1	1	S1	*s*	*b*	*r*	*s*	*b*	*r*	*s*	*b*	*r*	2	2	S2
2	1	533	2	2	552	2	3	563		01	01		4	157				4	5	158	0	01	02

The code number 533 in P*r* calls for station 1 in bank 2 to be read out via its A selector and to be moved. Code number 522 in Q*r* calls for station 10, bank 2, to be read out via its B selector and to be moved. Code number 563 in R*r* calls for station 1 in bank 3 to be read out via its A selector and to be moved. The code 01 in OP1 and OP2 directs accumulation to be performed and 01 and OP2 also makes T an In field. The three sub-categories punched in code in tapes 1 and 10 in bank 2 and station 1 in bank 3 will be accumulated and the sum entered in both relay storage units 157 and 158 (see Sections 17*a* and *b*). The sum constitutes the code number of a category.

It is desired to maintain a progressive count of each category. The computed category code numbers may be used as computed sequence instruction data for selecting relay storage units to maintain the progressive counts. The computed category code numbers are 10, 11, 12, 13, 14, 15, 16, and 17 which are the two right-hand digits of code numbers for relay storage units 010 to 017 and 110 to 117. Either of these two groups of relay storage units may be used. The common left-hand code digit for the storage units of each group may be supplied by plugging. Relay storage unit 157 is chosen to supply sequence data supplemented by a computed code number for subfield *r* of an Out field. Relay storage unit 158 is to supply sequence data supplemented by the computed code number for subfield *r* of an In field. The computed code number comprises the category number obtained in the commutator run on the line of sequence discussed before. During this run, the category number, which in each case is positive, was transmitted to columns 19 and 20 of storage units 157 and 158 and the + sign was stored in relay 2 of column 1 of each of these storage units.

Fig. 91 shows the plugging for reading out of unit 157 to Out bus-set 7, the SISeq data supplemented by the computed code number for subfield P*r*. Since the + sign is stored in unit 157, the socket 2 in column 1 of the sockets 7RS–GOPP will be "hot" when Unit In 157 is operated

(see Section 6). The "hot" socket is used to apply the non-computed, pre-chosen portion of the SISeq part of a subsequent line of sequence. This is accomplished by plugging socket 2 in column 1 of sockets 7RS–GOPP to the proper sockets in columns 1 to 3 and 6 to 20 of the 7RS–GO7 group. The remaining two columns, namely columns 4 and 5 or 7RS–GOP7 are plugged to sockets 19 and 20 of 7RS–GOPP, so that the computed category number will supply the distinctive two right-hand digits of the code number in subfield P*r*. The plugging, as shown, supplies the following SISeq data, the computed portion being denoted by CD.

P			Q			R			SH1	OP1	S1
s	*b*	*r*	*s*	*b*	*r*	*s*	*b*	*r*			
2	1	1CD	2	2	612	4	1			02	58

The commutator run on the first line of sequence computed the category number and supplied it to columns 1, 19 and 20 of units 157 and 158. The next line of sequence will include the SI code number 57 which in a manner now understood will select relay storage unit 157 as the source of the next SISeq data, which is given above. The P*r* number will be determined by the category number and be one of the numbers 110 to 117. The code number 612 in Q*r* calls out the digit 1 set in pluggable storage unit 612 (see Section 23). The code number 02 in OP1 calls for accumulation. Accordingly, when the above SISeq data is carried into effect, the previous category count in the storage unit selected by the computed category code number will be increased by 1. The R field of the above SISeq data instructs the accumulator to read the latest count into ES1. The SI code number is 58 and is used to select relay storage unit 158 as the next source of SISeq data.

Fig. 92 shows the plugging for supplying the next SISeq data. The + sign plug socket 2, in column 1 of 8RS–GOPP is plugged to supply the non-computed portion of the SISeq data to columns 1 to 13 and 16 to 20 of the sockets 8RS–GOP7. The other two columns, 14 and 15, of sockets 8RS–GOP7 and which correspond to columns 14 and 15 of subfield R*r* are plugged to receive the computed category number from columns 19 and 20 of sockets 8RS–GOP7. The SISeq data read out of unit 158 is shown below, the computed portion being denoted by CD.

P			Q			R			SH1	OP1	S1
s	*b*	*r*	*s*	*b*	*r*	*s*	*b*	*r*			
			2	1		4	1	1CD		02	01

The above data calls for the latest progressive count, of the computed category, which was obtained in the preceding commutator run and inserted into ES1 to be transferred, by way of the accumulator and shift unit, to the relay storage unit selected by the computed category number. In this example, the computed category number is the same for the P*r* subfield of the preceding SISeq data and for the R*r* subfield of the next SISeq data. Therefore, the latest progressive count of the computed category will be returned to the same memory unit from which the previous count was taken.

In the foregoing manner, a category number may be computed and a memory unit selected

thereby to maintain a progressive count of the frequency occurrence of the category.

Case 5.—Modification of sequence instruction for bus-sets.—When the frequence counts of categories are not to exceed 9-place numbers, half as many relay storage units as the number of categories may serve to keep the frequency counts. Each such unit will then be used as a split unit. The computation of the sequence instructions for selecting the units will involve not only a determination of the storage unit code number but also of the bus-sets to which the split units are plugged. In other words, if both halves of a storage unit are to read out stored numbers separately, they must be plugged to different Out bus-sets and if they are to receive numbers separately they must be plugged to different In bus-sets. The selection of the relay storage Group Outs and Group Ins is determined not only by the number in subfield *r* but also by the digit in subfield *b* of the same field (see Section 11). On the other hand, the selection of a relay storage Unit Out or In is determined only by the number in the subfield *r*. Hence, the desired half of a split unit is selected by the number in subfield *r* and the digit in subfield *b*.

Assume, for instance, that the units of relay storage Group 0 are to be used as split units both for receiving and reading out numbers, that the left halves of the units are to receive numbers from In bus-set 4 and to read out to Out bus-set 4, while the right halves are to receive from In bus-set 5 and to read out to Out bus-set 5. The plugging for this will be as follows:

For receiving numbers in the left halves; columns 1 to 10 of sockets ORS–GIPP (Figs. 29 and 30 and Section 6) to columns 1 and 12 to 20 of ORS–GIP4, and from socket 82 of ORS–GIPP to socket 82 of ORS–GIP4.

For reading out numbers in the left halves; columns 1 to 10 of sockets ORS–GOPP to columns 1 and 12 to 20 of ORS–GOP4.

For receiving numbers in the right halves; columns 11 and 12 to 20 of sockets ORS–GIPP to columns 1 and 12 to 20, respectively, of ORS–GIP5, and from socket 84 of ORS–GIPP to socket 82 of ORS–GIP5.

For reading out numbers in the right halves; columns 11 and 12 to 20 or ORS–GOPP to columns 1 and 12 to 20 of ORS–GOP5, respectively.

By this plugging, all fifteen units of the 0 relay storage group may be used as split units. Similarly, others of the ten relay storage groups may be plugged to receive numbers in their left halves from In bus-set 4 and in their right halves from In bus-set 5 and to read out numbers from the left and right halves, separately, to Out bus-sets 4 and 5.

An example will be given of the computation of sequence instructions for Out and In bus-sets and also of the relay storage units. For this example, assume there are 200 consecutive category numbers 000 to 199 for which frequency counts are to be kept in left and right halves of the 100 relay storage units 010 to 019, 020 to 029, 030 to 039, 040 to 049, 050 to 059, 060 to 069, 070 to 079, 080 to 089, 090 to 099, and 100 to 109.

The computation of sequence will include the first step of multiplying the category number by 5. The product is one of the numbers 000, 005, 010, 015, 020 . . . 980, 985, 990, and 995. The next step in the computation is the addition of 100 to the product, giving one of the numbers 0100, 0105, 0110, 0115, 0120 . . . 1080, 1085, 1090, and 1095. The number in the thousands, hundreds, and tens orders of the sum is the identifying code number of a relay storage unit. The units order digit of the sum is either 0 or 5. The sum will be entered in storage units 157 and 158. Unit 157 will be called to read out the first computed line of sequence and unit 158 will be called to read out the second computed line of sequence.

Assume each category number when obtained is sent to storage unit 150 after which the following program may be carried out. For convenience, the program is shown as made up of the S1Seq parts of sequence lines but it is understood that each line also includes an S2Seq part.

Ps	*Pb*	*Pr*	*Qs*	*Qb*	*Qr*	*Rs*	*Rb*	*Rr*	SH1	OP1	S1
2	1	150	2	2	612	4	3			10	01
2	3		2	2	614	4	5	157		02	01
2	5		4	5	158					02	57
2	4 or 5	CDE	2	6	616	4	6 or 4			02	58
			2	6		4	4 or 5	CDE		02	01

The first line directs the category number in 150 to be multiplied by 5 taken from pluggable storage unit 612 and for the product to go into ES3. By multiplying a category number by 5, one of the numbers 000 to 995 is obtained. The next line directs the addition of the product in ES3 to 100 obtained from pluggable unit 614. The sum is transmitted to ES5 and unit 157. The third line directs the same sum, in ES5 to be transferred to unit 158. Also, the third line has the S1 code number 57 to select unit 157 for applying the sequence data in the fourth line to Out bus-set 7.

Referring to Fig. 93, the socket 2(+) of 7RS–GOPP is plugged to socket 2, column 1 and socket 4, column 2 of 7RS–GOP7. The remaining plugging is the same as in the preceding case (see Fig. 91) except that socket 2 of 7RS–GOPP is not plugged to column 3 of 7RS–GOP7. Columns 17, 18, and 19 of 7RS–GOPP are plugged to columns 3, 4, and 5 of 7RS–GOP7. The computed relay storage code number (designated by CDE) in columns 17, 18, and 19 will thus supply this code number to the subfield Pr of the fourth sequence line. The 20th column of unit 157 contains either 0 or 5. If 5 is in this column, then the 1 socket in 7RS–GOPP will be "hot" when Unit Out 157 is operated. This socket is plugged to socket 1 in column 2 of 7RS–GOP7. The 4 socket in column 2 of 7RS–GOP7 is plugged to socket 2 in column 1 of 7RS–GOPP. Hence, if 0 stands in column 20 of unit 157, the bus number 4 will be supplied to subfield Pb of the fourth sequence line, but if 5 stands in column 2 of unit 157, then the bus number 5 will be supplied to subfield Ps of the fourth sequence line. According to whether the bus number is 4 or 5, either the left or right half of the selected unit CDE will be selected to read out the category count. The S1 code number 58 in the fourth line calls for relay storage unit 158 to supply the next S1Seq data. The plugging of 8RS–GOPP to 8RS–GOP7 differs from that shown in Fig. 92 in the same respect as Fig. 93 differs from Fig. 91 and is such as to read out the fifth line shown in the above program.

Case 6.—Selection of operational sign code number.—A computation may be performed to find the sign and value of an argument. A function of the argument may be computed, treating the argument as a positive number. The result may then be modified according to the sign of the argument. For instance, sine $(-X) = -\sin X$. A table of sine functional values for positive ar-

guments X may be used to compute sine X. The value of sine X may then be modified by treating it as a positive value if the original sign of the argument is positive and treating it as a negative value if the original sign of the argument is negative. An illustrative program is:

	P			Q			R			SH	OP			T			U			V			SH	OP	
s	b	r	s	b	r	s	b	r	1	1	SI	s	b	r	s	b	r	s	b	r	2	2	S2
0	6	019	2	4	281	6	5		5	15	01	2	5		2	3	281	4	5	000		02	02
0	6		2	5		6	5		3	15	01	2	5		2	2	281	4	5	000		02	02
0	6		2	5		6	5		4	15	19	2	5		2	1	281	4	5	100	1	04	02
2 or 1	3	100	2	2	518	4	3	101	9	15	01												02

It is assumed for the above program that X is a number with less than ten places and is stored in the left half of unit **019**. It is assumed further that constant **1** has been entered in column 20 of unit **019**. The manner in which a unit such as **019** may be plugged to receive and read out entries separately in the left and right halves has been explained before (see Case 1). It is also asumed that prior to this program, the desired functional values have been selected in table 1 of the table look-up unit.

The first line of the above program directs X to be read out of unit **019** and into the MD unit and for the + absolute operational sign (Ps is 0) to be applied to the factor X. Thus, the positive absolute value of X will be used in the computation of $f(X)$. The other factor D_3 in the first multiplication is taken from table 1 and the product XD_3 is transferred to ES**5**. The right half of the first line directs another functional value D_2 from table **1** to be added to XD_3. The algebraic sum XD_3+D_2 is stored in ES**5**.

The second sequence line orders X, now in ES**6** to be treated as a + absolute number and to be multiplied by XD_3+D_2. The product $X(XD_3+D_2)$ is added to a third functional value D_1, from table **1**. The third sequence line calls for multiplication of the + absolute value of X by the previous sum, and for the product $X(X^2D_3+XD_2+D_1)$ to be added to a fourth functional value D_0 from table **1**. The sum $X(X^2D_3+XD_2+D_1)+D_0$ is transmitted to relay storage unit **100**. The left half of the third sequence line has S**1** number 19 which, in a manner now understood, selects unit **019** as the next source of S**1**Seq data. The plugging between **9**RS–GOPP and **9**RS–GOP**7** is shown in Fig. 94. It is seen that the pre-chosen sequence data is applied via the plugging between socket **1** in column 20 of **9**RS–GOPP and columns 2 to 20 of **9**RS–GOP**7**. Sockets **1** and **2** of column 1 in **9**RS–GOPP are plugged respectively to sockets **1** and **2** of column **1** in **9**RS–GOP**7**. Hence, the operational sign code number in Ps of the fourth sequence line will be either 1 or 2, depending on the sign of X.

It is to be understood that in those cases involving the selection of units for reading out values, as in Cases 4 and 5, it is possible not only to select relay storage units for this purpose but also to select others of the units such as tape storage, banks, the dial storage unit, and the pluggable storage unit.

While there have been shown and described and pointed out the fundamental novel features of the invention as applied to a preferred embodiment, it will be understod that various omissions and substitutions and changes in the form and details of the device illustrated and in its operation may be made by those skilled in the art without departing from the spirit of the invention. It is the intention, therefore, to be limited only as indicated by the scope of the following claims.

What is claimed is:

1. In a computing apparatus; an assemblage, including means for storing numerical data manifestations and a calculator, program means, means controlled by said program means for controlling variable data manifestation entry from said storage means into the calculator, means controlled by said program means for controlling arithmetical operations on the data manifestations and means controlled by said program means for controlling transmission of calculated result manifestations to said storage means, said program means including a plurality of manifestation storage means each storing manifestations of a set of sequence instructions, a circuit organization including one of said last named storage means for transmuting a set of manifestations into related program control potentials for said assemblage, a plurality of concurrently available sources of sets of sequence instruction manifestations, circuits comprising said one of said above mentioned last named storage means controlled according to its stored manifestations of sequence instructions for selecting one of said concurrently available sources of sets of sequence instruction manifestations from one of said concurrently available sources and means including said one of said above mentioned last named storage means for applying the selected set to another of said plurality of storage means.

2. In a computing apparatus; an assemblage, including means for storing numerical data manifestations and a calculator, program means, means controlled by said program means for controlling variable data manifestation entry from manifestation storage into the calculator, means controlled by said program means for controlling arithmetical operations on the data manifestations, in combination with means for storing program data manifestations, a pair of sequence data manifestation storage units, circuits including said program means for transferring manifestations of program data from the program data storing means into one of said pair of sequence data manifestation storage units, and a circuit organization coacting with the respective one of the pair of sequence storage units to transmute the manifestations of program data in said one unit into successive calculation program control potentials for said assemblage.

3. In a computing apparatus including numerical data storing means for storage of all digit values, a calculator, entry circuits for entering data from the storing means into the calculator, and readout circuits for delivering data from the calculator to the storing means, the combination of, a control circuit network including a signal circuit for applying a common entry timing and producing signal to the entry circuits to effect concurrent entry of all digit value data into the calculator, another signal circuit for applying a calculation start signal to the calculator, and a third signal circuit for applying a common deliv-

ony timing and producing signal to the readout circuits to effect concurrent readout of all digit value data from the calculator to the storing means, and a signal circuit in the calculator for applying a calculation end signal to said control circuit network to effectuate operation of said third signal circuit.

4. In a computing apparatus including numerical data storing means for storage of all digit values, a calculator, entry circuits selected according to different value digits in orders of numerical data in said storage means to be entered in the calculator, readout circuits selected according to different value digits in the orders of a result in the calculator to be transmitted to said storage means, the combination of, a signal circuit for applying a common timing signal to the selected entry circuits to produce simultaneous entry into the calculator of the different value digits in orders of numerical data in memory, a signal circuit for applying a calculation start signal to the calculator, a circuit operated by the calculator for producing a calculation end signal, and a signal circuit brought into operation under control of the calculation end signal for applying a common timing signal to the readout circuits to produce simultaneous transmission to said storage means of the different value digits in the orders of the calculated result.

5. In a computer or the like; a number representation source including number output circuit gates, a number receiver including number input circuit gates, transfer circuits effective upon closure of the output and input gates for transferring a number representation from the source to the receiver, closure devices for the output and input gates respectively, means producing conditioning potentials, and means for producing a forward signal by the number representation source comprising means operated by the operation of its output gates for producing said forward signal and means controlled jointly by said forward signal and by said conditioning potentials for controlling the operation of the closure device for the input gates.

6. In a computer or the like; a storage unit for numerical data representations, a receiving unit for numerical data representations, circuits to transfer numerical data from the storage unit to the receiving unit and including an Out bus-set, means for applying the numerical data representations in the storage unit to the Out bus-sets and transfer circuits, a pilot device for applying a timing signal to the transfer circuits to time the entry by said transfer circuits of the applied numerical data representations into the receiving unit, a source of signals for conditioning said pilot device, means operable upon operation of said applying means for producing a forward signal and routing said signal via the Out bus-set to the pilot device to cooperate with said source of signals to control it in its production of the entry timing signal.

7. In a computer or the like, numerical data representation storage means, numerical data representation receiving means, circuits to transfer data representations from storage to the receiving means and including a plurality of selectable circuit channels to which said storage means may apply numerical data representations, gate means, a plurality of pilot devices respectively controlling said gate means for respectively piloting data representations applied to the circuit channels into the receiving means, sequencing control means comprising potential producing means for selectively applying potentials to said pilot devices for effecting coordinated selection of the pilot units and the related channels, and forward signals applied by said storage means via the selected channels to the related pilot units and acting conjointly with said potential producing means to enable a selected pilot unit to pilot data representations into the receiving means.

8. In a computer or the like; a storage unit for numerical data representations of all digit values, a receiving unit for numerical data representations, circuits to transfer the numerical data representations from the storage unit to the receiving unit, and switching connections upon operation of which and via which the storage unit applies representations of numerical data therein to said transfer circuits, an entry timing device for applying a timing signal to said transfer circuits to produce a simultaneous entry thereby into the receiving unit of the numerical data representations of all digit values, means producing conditioning potentials, and means producing a forward signal comprising means operable by the operation of said switching connections, said forward signal and said potentials jointly controlling said entry timing device.

9. In a computer or the like; numerical data representation storage means, numerical data representation receiving means, circuits to transfer data representations from storage to the receiving means and including an output circuit gate effective upon operation thereof to apply the numerical data representations from storage to the transfer circuits, gate means, a pilot device controlling said gate means to pilot the entry of the data representations applied to said transfer circuits to the receiving means, a sequencing device including means producing conditioning potentials and a circuit to operate said output gate, a control circuit for the pilot device, and a signal applied by said storage means to the pilot device upon the operation of said output gate acting jointly with said conditioning potentials transmitted via said control circuit to enable the pilot device.

10. In a computer, or the like; a plurality of number representation sources, and respective output switch means therefor, number representation receiving means including input switch means, connecting circuits between the output switch means and the input switch means, selection devices for selectively operating one of said output switch means to apply the number representation from the related source and via the connecting circuits, to said input switch means to condition the latter for entering the number representation into the receiving means, a source of conditioning potentials, a circuit to detect the operation of an output switch means, and a device responsive to said detecting circuit and said conditioning potentials for operating said conditioned input switch means to effect the entry of the number into the receiving means.

11. In a computer or the like; a bank of numerical data representation storage units, receiving means for the numerical data representations, a plurality of circuit channels for transferring data representations from the bank to the receiving means, a plurality of sets of unit output circuit gates, each set including an output gate of each unit, and the number of sets being fewer than the number of channels, connections between each set of output gates and a desired number of the channels, and sequenc-

ing circuits controlling said gates for controlling the application of data from as many units of the bank, as the number of sets of gates, to a corresponding number of the channels and including circuits to selectively close only one gate of each of the data representation applying units and from a different one of the sets of gates for each such unit.

12. In a computer or the like, a unit to receive data representations, circuits to transmit data representations to the unit and including switching connections to the unit, gate means, a pilot device to apply a timing signal to said gate means and thereby time the transmission of the data to the unit, a sequencing device including means producing conditioning potentials, means to operate said device to render said switching connections effective, and a back signal applied to the pilot device by said unit via the switching connections upon their being rendered effective and acting jointly with said conditioning potentials to control operation of the pilot device in producing the timing signal.

13. In a computer or the like, a data representation receiving unit, circuits to transmit data representations to the unit and including switching connections to the unit, gate means, a pilot device to apply an effectuating signal to said gate means and thereby permit the data transmission to the unit, a sequencing device including means for producing conditioning signals including a presense signal and a circuit to render the switching connections effective, means for operating said device, a back signal applied by the unit to the pilot device upon said switching connections being rendered effective, and said conditioning signals including said presense signal applied to the pilot device to act conjointly with the back signal in controlling its production of the effectuating signal.

14. In a computer or the like; a data representation receiver, normally idle input means for the receiver, a data representation source, normally idle output means for the source, circuits for transmitting data representations from the source to the receiver upon operation of both the input and output means, enabling means for the input means, an enabling device for the output means, means producing conditioning potentials and a circuit rendered effective by operation of the input means for acting jointly with said conditioning potentials for enabling the enabling device to operate the output means.

15. In a computer or the like; data representation receiving units, a normally inactive input means for each unit, a transmission channel including data representation receiving lines and a back signal line, a device to render any of the input means active thereby to select the related unit to receive data representations, a source of data representations having a normally inactive output, means for transmitting data representations to said data representation receiving lines, a pilot device, and means producing a back signal upon operation of an active input means and applied via the active input means and the back signal line in said channel to the pilot device to condition the pilot device, means for rendering said conditioned pilot device operative to render the output means active to apply data representations from the source via the data receiving lines and the active input to the selected receiving unit.

16. In a computer or the like; a data representation register unit selectively conditionable to receive or send data representations, gate means controlling the flow of data into or out of said unit, a pilot device controlling said gate means to pilot data representations into or out of the unit, a signal circuit for applying a back signal from the unit to the pilot device when the unit is conditioned to receive data representations, means cooperating with said back signal for enabling the pilot device to pilot data into the unit, a signal circuit to apply a forward signal from the unit to the pilot device when the unit is conditioned to send data representations, means cooperating with said forward signal for enabling the pilot device to control said gate means to pilot data representations out of the unit, and connections between the signal circuits for preventing concurrent production of the signals.

17. In a machine of the class described, an electric register for numeric data registration, circuits having potentials applied thereto representative of numeric data and connected to the register to apply, in response to an entry timing signal, numeric data entering potentials to the register, a cancel circuit device connected to the register and responsive to a cancel signal to reset the register, and an automatic pilot device for producing the cancel and entry signals together and terminating the cancel signal prior to the termination of the entry signal.

18. In a machine of the class described, an electric register for numeric data, circuits responsive to an entry signal for entering into the register numeric data representations carried by the circuits, electrical reset means for the register and effective in response to a reset signal, a circuit operated for a determined time duration to produce the reset signal, and a circuit connected to the reset signal circuit for producing the entry signal, said last circuit being effective after termination of the reset signal.

19. In a machine of the class described, an electric register for numeric data, means operated by an entry signal for applying numeric data representing signals to the register to enter therein the represented data, a resetting circuit for the register and rendered operative by a reset signal, circuits for producing the entry and reset signals, and capacitive means in the resetting circuit controlled by electric pulses for relatively timing the reset and entry signals to produce a reset of the register prior to each entry therein and permitting the entry signal to have an effective portion.

20. In a machine of the class described, relays forming a numeric data register, entry circuits for energizing the relays according to numeric data, hold circuits for the energized relays, a resetting device for the register comprising means for breaking the hold circuits, and automatic sequencing means for operating the resetting device and the entry circuits in overlapping times and terminating operation of the resetting device first to allow the hold circuits of the relays energized by the entry circuits to make with minimum delay after termination of the operation of the reset device.

21. In a machine of the class described, an electrical data representation storage unit having a normally idle input circuit gate, circuits to apply data representations via said gate, when operated, to said storage unit, a reset circuit for said unit, a reset control device for operating the reset circuit to clear the unit for reception of new data, a device for operating said gate to admit data into the unit, means pro-

ducing conditioning signals, and a back signal circuit stablished via said operated gate for acting jointly with said conditioning signals for enabling said reset control device to function for operating the reset circuit to clear the unit for reception of new data.

22. In a machine of the class described, an electrical data representation storage unit having a normally idle input circuit gate, entry circuits to enter data representations into the unit by way of said gate when active, a circuit for rendering said gate active, a reset circuit for said unit, a pilot device including means for applying a reset signal to the reset circuit for clearing the unit for reception of new data, a sequencing device including means for producing conditioning signals including a presense signal, means for rendering said sequencing device operative, and a circuit effective upon said gate being rendered active for applying a back signal to the pilot device to combine with said conditioning signals for enabling the pilot device to apply the reset signal to the reset circuit.

23. In a machine such as defined in claim 22, said pilot device also including means for applying an entry timing signal to the entry circuits outlasting the reset signal.

24. In a machine such as defined in claim 23, said sequencing device when rendering operative also applying said conditioning signals to the pilot device to combine with the back signal in enabling the pilot device to produce said entry timing signal.

25. In a machine of the class described, a data representation receiver, a reset device therefor, a circuit channel having data representation transmission lines and reset and back signal lines, circuit connections operated to connect the data representation transmission lines to the receiver, the reset signal line to said reset device and the back signal line to a source of signal potential, means producing conditioning potentials and a circuit device connected to the back and reset signal lines to receive a back signal produced upon operation of said circuit connections and enabled by said back signal acting with said conditioning potentials to apply a reset signal to the reset device to clear the receiver for the reception of new data representations from the data transmission lines.

26. In a machine such as defined in claim 25, a source of data representations connected to the transmission lines in said circuit channel, said circuit device also including a circuit under control of the back signal for effecting the application of data representations from the source upon the transmission line.

27. In a machine operating with record material having successive indicia representing records; a sensing and feeding station for sensing one indicia record after another, readout circuits for an indicia record sensed at the station, a program device conditioned by one program instruction for conditioning the readout circuits to operate and conditioning a network at the station to cause the record material to feed after the readout circuits have read out an indicia representing record, said program device being controlled by another program instruction for conditioning the readout circuits to operate and conditioning said network at the station to cause the indicia record to remain in the same sensing position, and a sequencing device for rendering the program device effective for operating the conditioned circuits to read out an indicia representing record at the sensing position and to operate said network at the station to cause the record material to feed or not to feed according to the conditioning of the station.

28. In a machine operating with record material having successive numerical indicia representation records; a register, a sensing and feeding station for sensing one indicia record after another, entry circuits operable to enter the numerical indicia representation of a sensed record into the register, a program device conditioned by one sequence instruction for preparing additional entry circuits to operate and a network at the station to cause the record material to feed thereafter, said program device being controlled by another sequence instruction for preparing said additional entry circuits to operate and allowing the station to retain the same indicia record in sensing position, and a sequencing device for rendering said program device effective for connecting said additional entry circuits to the sensing station and applying an entry timing signal to said first entry circuit and operating the network at the station to cause the record material to feed if prepared for such action.

29. In a machine operating with record material having successive numerical indicia representation records; a sensing unit for sensing one record at a time, feed mechanism to feed one record after another to the sensing unit, a numerical data representation register, entry circuits connectable to the sensing unit to enter the numerical indicia of a sensed record into the register, a feed control circuit for the feed mechanism selectively conditionable according to whether or not the feed mechanism is to operate, a program record bearing either one sequence instruction which controls means for connecting additional entry circuits to the sensing unit and the feed mechanism to operate or bearing another sequence instruction which controls means for connecting said additional entry circuits to the sensing unit and the feed mechanism to remain idle, a device receiving either of said sequence instructions and effective, under control of either instruction for so connecting said additional entry circuits to the sensing unit and effective under control of only the first mentioned instruction to so condition the feed control circuit for operation of the feed mechanism, and sequencing means for rendering said device effective for connecting said additional entry circuits to the sensing station and applying an entry timing signal to said first entry circuits and rendering the feed control circuit effective to operate or not operate the feed mechanism according to the condition of the control circuit.

30. In a machine operating with record material having successive indicia representing records; a sensing unit for sensing one indicia record at a time, feed mechanism for feeding one record after another to the sensing unit, indicia representation readout circuits for coacting with the sensing unit to read out representations from a sensed indicia record, program storage means for storing either a sequence instruction for the readout circuits to operate and the feed mechanism to feed the record material or another sequence instruction for the readout circuits to operate but the feed mechanism to remain idle, means rendering said storage means operative and circuits including said means for rendering said storage means operative and rendered operative by either sequence instruction

from said storage means and controlled by the former sequence instruction for rendering operative the readout circuits and the feed mechanism, and controlled by the other sequence instruction for rendering only the readout circuits operative.

31. In a machine operating with record material having successive indicia representing records; a sensing unit for sensing one indicia record at a time, a storage device to receive indicia representations, circuits to coact with the sensing unit to enter into the storage device the indicia representations of a record being sensed, feed means for the record material, a move circuit selectively conditionable to accept or reject a move signal and upon accepting the move signal controlling the feed means to feed a next indicia record to the sensing unit, a program storage device selectively energized to store manifestations for conditioning the move circuit either to receive or reject the move signal depending on the pattern of energization, and a squencing device for rendering the program storage device effective to condition said move circuit and including a circuit for applying the move signal to the move circuit.

32. In a machine operating with record material comprised of successive indicia representation records; a sensing unit for sensing one record at a time, feed means operative to move one record after another to the sensing unit, switch means comprising a part of said feed means, means to call the feed means into operation, an indicia representation receiver, entry circuits controlled by an entry signal to enter into the receiver indicia representations applied to the circuits, output circuit connections for the sensing unit operative to apply sensed indicia representations of a record to the entry circuits, means rendering the output circuit connections operative, a forward signal circuit effective upon the output circuit connections being rendered operative and under further control of said switch means, in the absence of operation of the feed means, to produce a forward signal, a pilot device, a source of signals for conditioning said pilot, said pilot being conditioned by said signals and rendered operative by the forward signal to apply the entry signal to the entry circuits, said switch means upon detecting occurrence of operation of the feed means preventing the forward signal circuit from being made and thereby blocking the pilot device from producing an entry signal.

33. In a machine such as defined in claim 32 the means to render the feed means operative being rendered effective by a move signal, and said pilot device including a circuit rendered operative by the forward signal to produce the move signal in timed relation to the entry signal.

34. In a computer, a plural order value register having in each order an array of value representing circuits, fewer than the number of different values to be selectively registered in the order, said value representing circuits being rendered operative, singly and in various combinations, to register selectively the different digits according to a suitable combinational code, an input circuit for each value representing circuit, circuits selectively energized to represent values and concurrently conditioning the input circuits of each order, selectively, according to a plural order value to be entered in the register, a circuit for applying an entry signal, to all the input circuits, to render the conditioned input circuits concurrently effective to operate the related value representing circuits to thereby effect a single-timed entry of the plural order value, a cancel device responsive to a cancel signal for restoring the operated value representing circuits so as to clear the register for a new value entry, a circuit for producing and applying the cancel signal to the cancel device, an automatic sequencing circuit network for operating the cancel signal circuit and the entry signal circuit in determined time relationship, said automatic sequencing circuit network including a timing circuit having pulses continually applied thereto but normally unresponsive to said pulses, and also including a circuit for concurrently initiating the effective operations of the cancel signal circuit and the entry signal circuit and controlling the responsiveness of the timing circuit device to the pulses, said timing circuit device thereupon being operated by the pulses for first terminating the cancel signal and then terminating the entry signal.

35. In a computing apparatus; a calculator having calculation sequencing means, number representation source means, a read in signal circuit, switching means responsive to a read-in signal for reading a number representation from the source means into the calculator, and a calculator sequencing device including said read-in signal circuit and a delay circuit connected to the read-in signal circuit for retarding application of a start signal to the calculation sequencing means until after the number has been read into the calculator.

36. In a computing apparatus such as defined in claim 35, said read-in signal circuit including an electron tube for applying an initiating pulse to the delay circuit, only upon the termination of the effective operation of the read-in signal circuit.

37. In a computing apparatus such as defined in claim 35, and pulses continually applied to the read-in and start signal circuits, said pulsed circuits being operable, only after the sequencing device has brought the read-in signal circuit into operation, for timing the time duration of operation of the signal circuits.

38. In a computer apparatus, a calculator unit and associated sub-sequencing means for sequencing the unit through steps of a calculation to obtain a multiple digit calculated result manifestation and produce a calculation complete signal at the end of the calculation, a multiple digit calculated result manifestation receiver, and automatic, main sequencing means including a circuit conditioned to respond to said complete signal, and transfer circuits rendered operative by said circuit upon its response to the complete signal for effecting a single-timed transfer of the multiple digit calculated result manifestation from the calculator unit to the receiver.

39. In a computer apparatus such as defined in claim 38, said receiver comprising a shift unit with its own sub-sequencing means, and said main sequencing means also including a circuit operative in timed relation to said transfer circuits for applying a start signal to said shift unit to render its sub-sequencing means effective to sequence the latter unit through an operation on the result manifestation received from the first mentioned calculator unit.

40. In a computer apparatus such as defined in claim 39, said shift unit being a result manifestation shifting unit for shifting the multiple digit calculated result manifestation a selected

number of places, and program means including circuits producing controlling potentials operative on said sub-sequencing means whereby said last means produce potentials for controlling the shift of the calculated result manifestation a controlled number of places.

41. In a computer apparatus such as defined in claim 40, a register to receive the shifted multiple digit calculated result manifestation from the shifting unit, a counter for counting the number of shift steps of operation of the shifting unit, and circuits brought into operation under control of said counter for transferring the shifted result from the shifting unit to the register upon termination of counting steps of said counter.

42. In a computer device, a calculator unit to perform a calculation on arithmetical data representations and produce a calculated result manifestation, calculation sequencing means for the unit and producing a calculation complete signal after the unit produces the calculated result manifestation, a result receiver, a read-out circuit responsive to a read-out signal for reading the calculated result manifestation out of the unit, entry circuit means responsive to an entry signal for entering the result manifestation, read out of the unit, into the receiver, further circuits for controlling readout and entry, and an automatic signal sequence circuit network including a circuit conditioned to respond to the complete signal to thus render operative said further circuits for respectively producing the readout and entry signals in timed relation.

43. In a computer device as defined in claim 42, and a circuit connected to said read-out circuit for deconditioning said read-out circuit, after the read-out and entry signals have been produced.

44. In a computer device such as defined in claim 42, a plurality of calculator units and related calculation sequencing means and read-out circuit means being provided, said signal sequencing network having a separate selectively conditioned, complete-signal-receiving circuit for each unit and a separate read-out signal circuit for each unit brought into operation by the related complete-signal-receiving circuit, and said entry signal circuit being commonly connected for operation under control of any of the complete-signal-receiving circuits.

45. In a computing apparatus; a calculator to effect a calculation on arithmetical data representations and produce a calculation complete signal and including circuits responsive to a read-out signal for reading out a result manifestation obtained by the calculation, a result shift unit responsive to a read-in signal for receiving the calculated result manifestation and including means controlled by a counter for shifting the result manifestation a desired number of places and means also controlled by said counter for producing a shift complete signal at the end of the desired shift, said shift unit being responsive to an exit signal for reading out the shifted result, a register responsive to an entry signal for receiving the shifted result manifestation, a counter, means for setting said counter in accordance with said desired number of steps of shift and automatic sequencing circuit means including a circuit operated by the calculation complete signal, circuits operated by the preceding circuit upon its receiving the calculation complete signal for producing the read-out and read-in signals in timed relation to produce a transfer of the calculated result manifestation from the calculator into the shift unit, a control circuit to receive the shift complete signal and circuits brought into operation by said control circuit upon its receiving the shift complete signal for producing the exit and entry signals in timed relation to produce a transfer of the shifted result manifestation from the shift unit to said register.

46. In a computing apparatus such as defined in claim 45, said shifting means in the shift unit being initiated in operation by a shift start signal, and said sequencing circuit means having a delay circuit connected to the read-in signal circuit for producing the shift start signal after the read-in signal.

47. In combination, a calculator responsive to a data read-in signal for receiving arithmetical data manifestation and responsive to a read-out signal for reading out a computed result manifestation, said calculator including cycling means for sequencing the calculator through one step of a calculation at a time and producing a cycle complete signal at the end of the step, numerical data manifestation storage means responsive to an exit signal for reading out data manifestations and responsive to an input signal for receiving data manifestations, and automatic sequencing means including a circuit awaiting said complete signal and conditioned to operate in response thereto, and a selectively conditioned sequencing means and cooperating with said sequencing means organization controlled by said circuit either to produce said exit and read-in signals in timed relation or to produce said read-out and input signals in timed relation, depending on the conditioning of the circuit organization, whereby data manifestations from said storage means may be transferred to the calculator and means connecting said calculator and said storage means whereby the computed result may be transferred from the calculator to said storage means, as determined by the conditioning of said circuit organization.

48. In the combination as defined in claim 47, a circuit in said sequencing means, said cycling means being initiated in operation by a start signal and said circuit organization including a circuit for initiating operation of said sequencing means circuit for producing said start signal in automatically timed relationship to the exit and read-in signals so as to initiate the operation of said cycling means each time data is transferred from said storage means to the calculator.

49. In the combination as defined in claim 47, and including program means, means conditioning said program means, and means for causing said program means to operate according to selective sequence conditioning for selectively conditioning said circuit organization to produce the transfer of data manifestations from said storage means to the calculator or the transfer of the result manifestation from the calculator to said storage means.

50. In a computing apparatus; a calculator responsive to entry signals for receiving applied numerical data manifestations, numerical data manifestations storage means responsive to exit signals for applying numerical data manifestations to the calculator, a pilot device for producing the exit signals and a return signal for each exit signal, means for conditioning said pilot device, a main commutator including a calculator control device for producing the entry signals and a back signal for each entry signal, means

for conditioning said control device, said main commutator also having a series of commutator portions operable successively to produce pilot controlling signals, a first such portion applying its controlling signal to the pilot device to act jointly with said conditioning means to render said pilot device effective to produce an exit signal for applying a number manifestation from said storage means to the calculator, and said portion being controlled by the attendant return signal for producing an operation control signal applied to the calculator control device to act jointly with said control conditioning means to render said device effective to produce an entry signal to cause the number manifestation applied to the calculator to be entered therein, and a circuit for applying the accompanying back signal to the commutator portions to bring the next portion into operation.

51. In a computing apparatus as defined in claim 50, said calculator control device including a circuit for applying a calculation start signal to the calculator in timed relation to the production of an entry signal.

52. In a computing apparatus such as defined in claim 51, said calculator applying a calculation complete signal to the calculator control device at the end of a calculation, and said control device including a circuit controlled jointly by said complete signal and said control conditioning means to supply another back signal to the commutator portions to sequence their operation.

53. In a computing apparatus as defined in claim 50, said data storage comprising a plurality of storage units, the pilot device comprising a plurality of pilot units each for producing the exit signal for one of the storage units, and a program device for selecting the pilot units to be rendered effective by the pilot controlling signals from the commutator portions, whereby numerical data will be applied according to the program from selected storage units to the calculator.

54. In a computing apparatus; a calculator section, a plurality of storage devices for number manifestations, a plurality of number manifestation sources, pilot units each for producing an input signal for one of the storage devices to effect the transfer of a number manifestation from one of the sources into the storage unit, each pilot unit also having a circuit for producing an exit signal for the related storage unit to control the transfer of the number manifestation from this storage unit to the calculator, means to condition said pilot units, and a main commutator including a circuit for applying a common control signal to all the pilot units acting jointly with said conditioning means to render them effective for producing the input signals, said commutator also including circuits producing successive signals for rendering the pilot units effective successively to produce the exit signals.

55. In a signal-controlled and signal issuing apparatus; a circuit to produce a control signal and including an electron tube trigger circuit comprising an electronic circuit having two stages of stability to be turned to one stage and returned to the other for causing the circuit to produce the control signal, and means to turn and return the trigger under control of two controlling signals issued by said apparatus, either one after the other or both simultaneously, said means including a circuit operated by either controlling signal for applying a turning pulse to the trigger, said means further including a returning circuit conditioned by either controlling signal and operated by the other controlling signal for applying a returning pulse to the trigger, said returning circuit including a delay circuit to delay the application of the returning pulse to the trigger until after the turning pulse has been applied, to produce the proper turning and returning sequence for the trigger even when the controlling signals occur simultaneously.

56. In a computing apparatus; a pair of data manifestation storing units, a circuit channel, means comprising a portion of one of said units, responsive to a timing signal to render said channel effective to transfer the data from one unit to the other, means comprising a portion of the other unit for applying data manifestations to the channel, a circuit rendered operative upon the application of said data manifestations to the channel for producing a first control signal, a circuit producing a conditioning signal, a commutator having a round of operations in each of which it produces a control signal, a circuit to produce said timing signal and including an electron tube trigger circuit to be turned and returned in sequence for causing the circuit to produce the timing signal, either of the control signals occurring first or both occurring simultaneously, a turning circuit, means controlled jointly by said commutator control signal and said conditioning signal for applying a pulse to the turning circuit, and a returning circuit operated by said first control signal and said last mentioned pulse conjointly for applying a returning pulse to the trigger circuit, said returning circuit including a delay circuit to delay the application of the returning pulse to the trigger until after the trigger has been turned, regardless of whether the control signals occur simultaneously or in succession.

57. In a computing apparatus; a calculator section to perform calculations on numerical data manifestations and to produce calculated result manifestations, numerical data manifestation storage means, means connecting said calculator section and said storage means, means controlled by an out signal for transferring data manifestations from said storage means to the calculator section, means controlled by an in signal for transmitting data manifestations from the calculator section via said connecting means to said storage means, and a pilot device including a circuit for producing the out signal, a circuit for producing the in signal and means for selectively conditioning said pilot unit to produce either signal or to produce both signals in timed relation.

58. In a computing apparatus as defined in claim 57; in combination with a sequencing circuit network for applying a first transmission signal and an out timing signal successively to the pilot device to act jointly with said conditioning means to enable it to produce the in and out signals successively.

59. In a computing apparatus; a calculator section to perform calculations on numerical data manifestations and to produce calculated result manifestations, numerical data manifestation storage means, means connecting said calculator section and said storage means, controlled by an out signal for transferring data manifestations from said storage means to the calculator section, means controlled by an in signal for transmitting data manifestations from the calculator section via said connecting means to said storage means, and a pilot device including a circuit for producing the out signal, a circuit for producing the in

signal, a program device settable to patterns of control, and circuits controlled by the program device according to said patterns for conditioning the pilot device to produce either signal.

60. In a computing apparatus as defined in claim 59; in combination with a sequencing circuit network for applying out and in timing signals successively to the pilot device, respectively to enable it to produce the out or in signal, according to the conditioning of the pilot device.

61. In a computing apparatus; a calculator, a first numerical data manifestation storing means, a second numerical data manifestation storage means, circuits controlled by an entry signal for transferring data manifestations from said first to said second storage means, circuits controlled by an exit signal for sending the data from said second storage means to the calculator, a pilot device having circuits to produce the entry and exit signals, means for conditioning said pilot device, a commutator to apply a pair of signals to the pilot device, one commutator signal acting with said conditioning means to enable the entry signal acting with said conditioning means circuit to operate and the other commutator signal to enable the exit signal circuit to operate, and a delay circuit in the pilot device connected to the entry and exit signal circuits for delaying the operation of the exit signal circuit until after the entry signal circuit has operated.

62. In a computing apparatus; a calculator including a shifting circuit operated to produce a calculated result manifestation and an attendant calculation complete signal, result manifestation storage means, said shifting circuit connecting said calculator and said storage means, result manifestation receiving means, circuits controlled by an input signal for transferring the result manifestation from the calculator via said shifting circuit to said storage means, circuits controlled by an exit signal for transmitting the result manifestation from said storage means to the receiving means, a pilot device having circuits to produce said input and exit signals, conditioning means for said input signal circuits and said exit signal circuits, and a commutator operated in response to the calculation complete signal for applying input and exit timing signals successively to act jointly with said conditioning means to the pilot device respectively to enable the input and exit signal circuits to operate.

63. In a computing machine, a calculator to receive numerical data manifestations and perform a computation thereon to produce a calculated result manifestation, a plurality of data manifestation storage units, means connecting said calculator and said storage units, each of said units having an out circuit gate responsive to an out signal for sending data to the calculator and an in circuit gate responsive to an in signal for receiving via said connecting means a calculated result manifestation from the calculator, a plurality of pilot units, one for each data manifestation storage unit and selectively conditioned to produce either the out signal or the in signal for the storage unit, means for selectively conditioning the pilot units, each to produce either signal, and a sequencing network for producing out and in control signals and applying each of these control signals commonly to all the pilot units, with the out control signal enabling any pilot unit conditioned therefor to produce its out signal and the in control signal enabling any pilot unit conditioned therefor to produce its in signal.

64. In a computing machine as defined in claim 63, said conditioning means including a program device bearing in and out coding representations, means connecting said program device and said storage units, circuits connected to said storage units and controlled by said coding representations via said storage units to store an indication thereof, and circuits controlled by said connected circuits and thus settable in accordance with the respective coding representations and timed under control of said sequencing network for selectively conditioning the pilot units.

65. In a computing machine, a calculator selectively to perform out or in steps of calculation, the out step involving receipt of numerical data manifestations and performance of a calculation thereon and the in step involving delivery of a calculated result manifestation, circuits for controlling transfer of manifestations into or out of said calculator, signal responsive circuits selectively operating said controlling circuits, means for conditioning said responsive circuits, a main commutator comprising a series of electronic elements operable in steps to perform a round of operations for applying signals to the signal responsive circuits and acting with said conditioning means to render them effective in desired sequence, said sequentially acting commutator elements, each selectively conditioned to produce either out or in step control signals for the circuits, and a program device settable to in and out patterns of conditioning for conditioning the commutator elements and circuits controlled by said program device according to said patterns for selectively conditioning said elements.

66. In a computing apparatus; a data manifestation source, a data manifestation receiver, a data manifestation communicating link between the source and receiver and including input and output gates respectively controlled by input and output signals for admitting data manifestations from the source into the link and emitting the data manifestations from the link into the receiver, circuits respectively to produce and apply the input and output signals, means to condition said last named circuits, a sequencing circuit network producing and applying a control signal to the input signal circuit to act with said conditioning means to enable said circuit to produce the input signal, a circuit connected to the input signal circuit, means for operating said circuit and effective after the input signal circuit, to cause said circuit to produce and apply a return signal to the network, a circuit in the network, brought into operation under control of the return signal for applying a control signal to the output signal circuit to act with said conditioning means to enable it to produce the output signal.

67. In a computing apparatus; a data manifestation register, a data manifestation source, circuits between said source and register and responsive to a transmission signal for transmitting data manifestations from the source to the register, a reset device responsive to a reset signal for clearing the data register for reception of the transmitted data, a circuit operated to produce the reset signal, a reset delay circuit concurrently initiated in operation, a circuit operated to produce the transmission signal, and a circuit conjointly controlled by the delay cir-

cuit and the transmission signal circuit for terminating the effective operation of the reset signal circuit.

68. In a computing apparatus as defined in claim 67, and a transmission delay circuit initiated in operation under control of the reset signal terminating circuit for terminating the operation of the transmission signal producing circuit after a given interval.

69. In a computing apparatus, a calculator to perform a selected calculation, a plurality of data manifestation storage units selectable to deliver and receive data manifestations from the calculator, means connecting said calculator and said storage units, an output circuit gate for each unit to deliver data manifestations, an input circuit gate for each unit to receive the data manifestations, program circuits conditioned in patterns, according to program instructions, selecting the units to deliver and to receive data and selecting the calculation, a sequencing circuit network having a round of operations and heating circuits, operated at the beginning of the round, for applying potentials to the program circuits to operate the output and input gates of the selected units and to condition the circuit network for sequencing the calculator through the selected calculation, sequentially effective circuits in the network, acting during the round, for effecting the delivery via the operated output gate of data manifestations from the selected unit to the calculator, sequencing the calculator through the selected calculation, and thereafter effecting transmission of calculated data manifestations, from the calculator to said correcting means and via the operated input gate to the selected receiving unit, said calculator being operated during the round through successive steps of the selected calculation and receiving data manifestations from a different unit for each step, said program circuits being conditioned, in patterns according to program instructions for selecting the different units to deliver data to the calculator, said heating circuits operating said program circuits, to simultaneously operate the output gates of the different selected units, and the sequentially effective network circuits effecting the delivery of data manifestations, from the selected units to the calculator, in the same sequence as the calculation steps.

70. In a computing apparatus including an assemblage, comprising numerical data manifestation storage units and a calculator, in combination with a sequencing network set in accordance with a control pattern, means to transfer data manifestations from said storage units to the calculator, means for rendering said sequencing network effective, means conditioned by said sequencing network and rendered operable by said rendering means to selectively control said transfer means to produce selected routing of data manifestations from said storage units to the calculator, means including said rendering means to control said calculator to perform calculations on the data manifestations, and means including said transfer means selectively controlled for transmitting the computed result manifestations to said sequencing network to serve as instruction data manifestation for the subsequent sequence of operation.

71. In a computing apparatus as defined in claim 70, said computed result manifestation including representation of one or another number to designate different storage units as sources for instruction data.

72. In a computing apparatus as defined in claim 70, said computed result manifestation including one or another instruction number to designate different arithmetical operations of the calculator.

73. In a computing apparatus as defined in claim 70, said computed result manifestation including one or another instruction number designating the storage unit to deliver data to the calculator.

74. In a computing apparatus as defined in claim 70, said computed result manifestation including one or another instruction number designating the storage unit to receive data from the calculator.

75. In a computing apparatus as defined in claim 70, said last means including means for column-shifting a result a selected number of places, and said computed result manifestation including a computed shift amount designating instruction.

76. In a computing apparatus as defined in claim 75, said column-shifting means being capable of right or left shift, and said computed result manifestation also including one or another computed number manifestation designating a right or left direction of column shift.

77. In a computing apparatus as defined in claim 70, said first transfer means including a plurality of communicating circuit channels between storage and the calculator, and said result manifestation including a manifestation designating the channel to be used in transference of data between storage and the calculator.

78. In a computer or the like, a circuit system to produce alternately phased output signals and including a pair of dual-stability electron tube trigger circuits and a pair of mixer circuits, connections between one of the mixer circuits and a pair of output points of the trigger circuits to apply effective potentials from the trigger circuits, when in one relative state, to the mixer circuit to operate it for producing one of the output signals, connections between the other mixer circuit and another pair of output points of the trigger circuits to apply effective potentials from the trigger circuits, when in an opposite relative state, to this mixer circuit for operating it to produce the other output signal, and a sequencing network for producing a pair of input signals in each sequence run of the network, one input signal being applied to one of the trigger circuits to alternate its state in successive sequence runs, and the other input signal being applied to the other trigger circuit to alternate its state in successive sequence runs, whereby during one run the trigger circuits will be set by the input signals in the first mentioned relative state to cause one of the output signals to be produced, while in a next run the trigger circuits will be set by the input signals in the opposite relative state to cause the other output signal to be produced.

79. In a computer or the like, a pair of data representing circuits, a circuit system to produce alternately phased readout signals for the respective data representing circuits, said system including a pair of electron tube trigger circuits of the dual-stability type and a pair of mixer circuits, one operated jointly by the trigger circuits when in one relative state for producing one readout signal and the other operated jointly by the trigger circuits when in the opposite relative state for producing the other readout signal, a circuit for applying successive input signals to

one of the trigger circuits to alternate its state, another circuit for applying other successive input signals, out of phase with the previously mentioned input signals, to the other trigger circuit to alternate its state, whereby one input signal will change the state of one trigger circuit to disestablish one relative state of the trigger circuits and thereby to drop one of the readout signals and at the same time prepare for the opposite relative state to be established, while a following out-of-phase input signal will change the state of the other trigger circuit to establish the opposite relative state and thereby cause the other readout signal to be produced.

80. In a computing apparatus; a calculator unit operating on numerical data manifestations to produce a result manifestation, numerical data storage means network including a series of commutator electron valve circuits of which a first one is conditioned for an out step and the following ones are conditioned selectively for out or in steps, said network including a circuit for bringing said first electron valve circuit into operation to produce out signals, means producing conditioning potentials, circuits controlled jointly by said conditioning potentials and by the out signals, means controlled by said controlled circuits for transferring data manifestations from said storage means to the calculator unit to be used in a calculation, means for thereafter bringing the next commutator electron valve circuit into operation to produce either out or in signals according to the selective conditioning of said circuit, said circuit when conditioned for an out step operating similarly to the first circuit and when conditioned for an in step producing in signals, and circuits brought into operation by the in signals acting jointly with said controlled circuits for selectively transferring a calculated result manifestation from the calculator unit to said storage means.

81. In a computing apparatus as defined in claim 80, and including a circuit conditioned by said sequencing network and controlled by one of the out signals to apply a data read-in signal to the calculator unit, and said means for bringing the next electron valve circuit into operation including, a delay circuit connected to the read-in signal circuit for applying a delayed back signal to the commutator electron valve circuits to turn off the last-operated circuit and turn on the next circuit.

82. In a computing apparatus as defined in claim 80, said calculator unit also producing a calculation complete signal at the termination of a calculation and the means for bringing an in-conditioned electron valve circuit into operation including a circuit responsive to the calculation complete signal.

83. In a computing apparatus as defined in claim 80, a program device having patterns of sequence controls applied thereto, and circuits controlled by the program device according to said sequence patterns for selectively conditioning the commutator electron valve circuits for in or out steps.

84. In a computing apparatus as defined in claim 80, said sequencing network being operable automatically through successive sequence runs, and a circuit controlled by the last commutator electron valve circuit of the series upon termination of its operation for conditioning the sequencing network for a next sequence run.

85. In a computing apparatus; a calculator unit operating in successive calculation steps to produce a calculated result manifestation and a complete signal at the end of each step, numerical data manifestation storage means and a sequencing circuit network including a series of commutator electron valve circuits of which a first one is conditioned for an out step and the following ones are conditioned selectively for out or in steps, said network including a circuit for bringing said first electron valve circuit into operation to produce out signals, means producing conditioning potentials, circuits controlled jointly by said conditioning potentials and by the out signals, means controlled by said controlled circuit for transferring data manifestations from said storage means to the calculator unit to be used in a first calculation step by the calculator unit, means responsive to said complete signal for thereafter bringing the next electron valve circuit into operation to produce either out or in signals according to the selective conditioning of the circuit, said circuit when conditioned for an out step operating to similar effect as the first circuit and when conditioned for an in step producing in signals, and circuits brought into operation by the in signals acting jointly with said controlled circuits for selectively transferring a calculated result manifestation from the calculator unit to said storage means.

86. In a signal-controlled computing apparatus; a data manifestation register, a data manifestation circuit operated by an entry signal to enter data manifestations into the register, means producing conditioning potentials, a signal circuit system conditioned by said conditioning means and including an electron tube device having a limited, switched period initiated by an entry control signal applied to the signal system and operating during this period to produce the entry signal, means terminating the operation of said electron tube device, said circuit system also including another electron tube device controlled by said terminating means to operate subsequently to the first named electron tube device to produce a return signal, and a sequencing commutator for sequentially producing control signals for said apparatus and including a circuit to produce and apply the entry control signal to the signal circuit system and another circuit responsive to the return signal from said system for producing a following control signal for the apparatus.

87. In a signal-controlled computing apparatus; a data source, data transmission circuits, a data exit circuit gate between the data source and the transmission circuits and responsive to an exit signal for applying data from said source to the transmission circuits, means for producing conditioning potentials, a signal circuit system including an electron tube device having a limited, switched period initiated by a transmission control signal and said conditioning potentials, applied to the signal system and operating during this switched period to produce the exit signal, means for terminating the operation of said electron tube device, said circuit system also including another electron tube device controlled by said terminating means to operate subsequently to the first named electron tube device to produce a return signal, and a sequencing commutator for sequentially producing control signals for said apparatus and including a circuit to produce and apply the transmission control signal to said system, and also including another circuit responsive to the return signal for producing a following control signal for the apparatus.

88. In a signal-controlled computing apparatus; a circuit responsive to an operating signal, means for producting conditioning potentials, a signal circuit system including an electron tube device having a limited, switched period initiated by a control signal and said conditioning potentials applied to the signal system and operating during this period to produce said operating signal for the circuit, means terminating the operation of said electron tube device, said circuit system also including another electron tube device controlled by said terminating means to operate subsequently to the first named electron tube device to produce a return signal, and a sequencing commutator for sequentially producing control signals for said apparatus and including a tube circuit for producing the control signal applied to the signal circuit system and also including another tube circuit responsive to the return signal from said system for producing a following control signal for the apparatus.

89. In a signal-controlled calculating machine, means producing conditioning potentials, a tube circuit system responsive to an operating signal and said conditioning potentials for producing a machine control signal and a back signal in timed relation, and a sequencing commutator including a chain of signal producing circuits, each signal producing circuit being operable by an input signal for producing an operating signal for said circuit system and being responsive to the accompanying back signal for conditioning the next signal producing circuit in the chain to respond to the next input signal.

90. In a signal-controlled calculating machine, means producing conditioning potentials, a signal system including a chain of electron tubes responsive to a sequencing signal and said conditioning potentials for producing in succession a machine control signal and a back signal, and a sequencing commutator including a chain of commutator electron valve circuits each including a network of electron valves operated by an input signal for producing the sequencing signal for said signal system, one of said network of valves rendered operative by said ensuing back signal for producing a signal to condition the network in the next commutator electron valve circuit and means producing an input signal to render the latter effective to produce another sequencing signal for said signal system.

91. In a signal-controlled calculating machine as defined in claim 90, each said network including an electron valve trigger circuit turned by the input signal for producing the sequencing signal.

92. In combination, a storage circuit operated under control of pilot signals and a calculator section operated under control of calculation control commutator signals, a pilot device for producing the pilot signals and accompanying back signals, a calculation control commutator for producing the calculation control commutator signals and accompanying back signals, means producing conditioning potentials, and a main commutator having progressively operable circuits for sequentially applying operating signals in timed relation to the pilot device, said pilot device rendered operative by said conditioning potentials and said operating signals to apply said first named back signal to the main commutator and said main commutator operating in response to said last named signals to apply an operating signal to said calculation control commutator, said calculation control commutator rendered effective by said last mentioned operating signal and said conditioning signals, and said main commutator progressing under control of the back signals from the pilot device and the calculation control commutator.

93. In a combination as defined in claim 92, a plurality of calculation control commutators being provided, and a program device having calculation instructions applied thereto for selectively conditioning one of said control commutators for responding to the operating signals from the main commutator.

94. In a combination as defined in claim 93, a no-calculation commutator also being provided and conditioned, by the program device having a no-calculation representation applied thereto, for operating in response to the signals from the main commutator to produce back signals alone, for controlling the progressive operation of the main commutator circuits.

95. In a combination as defined in claim 92, said pilot device including a blank code pilot unit to be conditioned under control of the program device in accordance with the representation in an instruction field thereof for producing the back signals alone, to control the progress of the main commutator circuits.

96. In a program-controlled computing machine, a data manifestation register, a recording unit operable to record the data manifestations in the register, circuits to transmit data manifestations to the register, a program device bearing either a code number representation indicative only of a data manifestation transmission requirement to the register or another code number representation indicative of a requirement of data manifestation transmission and also of operation of the recording unit to record the data manifestation in the register, and a sequencing circuit network coacting with the program device according to the first mentioned code number representation for operating said circuits to transmit data manifestations to the register, said sequencing circuit network alternatively coacting with the program device according to the second mentioned code number representation for operating said circuits to transmit data manifestations to the register and for applying a start control signal to the recording unit.

97. In the machine as defined in claim 96, a plurality of registers being provided selectively to receive data manifestations and means responsive to said sequencing network to commonly control the recording unit to record the data manifestations in the plurality of registers, and said program device having selectively applied thereto code number representations indicative of either a requirement of transmission of data manifestations to any one of the registers or requiring transmission of data manifestations to any one of the registers and for operation of the recording unit to record the data manifestations in all the registers, and said sequencing network coacting with the program device according to code number representations representing the second requirement for operating said circuits to transmit data manifestations to one of said plurality of registers and for applying a start control signal to said recording unit.

98. In the machine as defined in claim 96, said sequencing network having a circuit for applying a transmission signal to said data manifestation transmitting circuits to render them effective and a circuit for turning off said

start control signal prior to the termination of the transmission signal, said recording unit being operable through a recording cycle and having a cycle initiating circuit conditioned under control of the start control signal and rendered effective upon termination of the start control signal.

99. In a computing apparatus; an assemblage, including numerical data manifestation storage means and a calculator, program means, means controlled by said program means for controlling variable data manifestation entry from said storage means into the calculator, means controlled by said program means for controlling arithmetical operations on the data manifestations, and means controlled by said program means for controlling transmission of a calculated result manifestation to said storage means, said program means transmuting groups of sequence instruction representations applied successively to said program means into successive program control potentials for said assemblage, means storing available groups of sequence instruction representations, and circuits for applying the groups of sequence instruction representations in a variable order to said program means to be transmuted into a variable sequence of program control potentials for said assemblage.

100. In a computing apparatus as defined in claim 99, said assemblage including circuits controlled by applied sequence instruction representations for selecting the variable order of application of the groups of sequence instruction representations to said program means.

101. In a computing apparatus; an accumulator to obtain a result manifestation indicative of the difference between two successively entered number manifestations and also to obtain a manifestation indicative of the sign of the difference, numerical data manifestation storage means, circuits to enter the number manifestations from said storage means into the accumulator, circuits to transmit the difference between number manifestations from the accumulator to said storage means, a sequencing network having sequentially active devices to render the entry circuits effective to enter the number manifestations successively into the accumulator and to render the transmitting circuits operative after the accumulation, a proceed circuit to produce a proceed signal for the sequencing network to render operative the device for rendering the transmitting circuits effective, a tolerance check circuit conditioning the proceed circuit to block production of a proceed signal, and means controlled by the accumulator and the sequencing network for canceling the blocking action of the tolerance check circuit upon the accumulator obtaining a manifestation indicative of a difference of a particular sign.

102. In a computer, a plural order value register having in each order an array of value representing circuits, fewer than the number of different values to be selectively registered in the order, said value representing circuits being rendered operative, singly and in various combinations, to register selectively the different digits according to a suitable combinational code, an input circuit for each value representing circuit, circuits selectively energized to represent values and concurrently conditioning the input circuits of each order, selectively, according to a plural order value to be entered in the register, a circuit for applying an entry signal to all the input circuits to render the conditioned input circuits concurrently effective to operate the related value represented circuits, thereby to effect a single-timed entry of the plural order value, a plural order value source operated to apply its value to the selectively energized circuits, an automatic sequencing circuit network including a control circuit for establishing the entry signal circuit, and a forward signal circuit acting upon application of the value from the source to the selectively energized circuits for enabling said control circuit, said automatic sequencing circuit network also including a circuit effective at a variable time for producing a signal acting jointly with the forward signal to bring said control circuit into operation.

103. In a computing device as defined in claim 70, said computed result manifestation including one or another number manifestation to designate the operational sign.

104. A device for storing, automatically extracting and effecting performance of an instruction, comprising storage means containing a plurality of selectable storage locations, each identified by a number address and each comprising means for storing a separate instruction word manifestation, potential controlled address selecting means for selecting and rendering available manifestations representative of the word stored at a selectable address, means controllable to produce permutations of potentials to selectively and exclusively operate said potential controlled address selecting means, means for selectively applying control potentials, representative of an address number, to said permutation of potential producing means to condition said means to produce such potentials to select one chosen address location from said plurality of address locations, means rendering said controllable means operative, translating means including said controllable means, means clearing said translating means, means interconnecting said storage means and said translating means, selective conditioning means, said rendering means and said conditioning means rendering said interconnecting means operative whereby said instruction word manifestation, at the address selected, is transferred to said translating means, and said rendering means rendering said translating means effective to produce permutations of effecting potentials representative of said selected instruction word manifestation, whereby the instruction in said word may be effected.

105. A device for storing, automatically extracting and effecting performance of an instruction, comprising storage means containing a plurality of selectable storage locations, each identified by a number address and each comprising means for storing a separate instruction word manifestation, potential controlled address selecting means for selecting and rendering available manifestations representative of the word stored at a selectable location, means controllable to produce permutations of potentials to selectively operate said potential controlled address selecting means, means for selectively applying control potentials, representative of an address number, to said permutation of potential producing means to condition said means to produce potentials to select one chosen address location from said plurality of address locations, means rendering said controllable means operative to operate said address selecting means, means for rendering said permutations of potentials producing means

controllable by said first selected word manifestation, and means for activating said potential producing means to produce selection of another word at another address in said storage means.

106. A device for storing, automatically extracting and effecting performance of an instruction, comprising storage means containing a plurality of selectable storage locations, each identified by a number address and each comprising means for storing a separate instruction word manifestation, potential controlled selecting means for selecting and rendering available manifestations representative of the word stored at a selectable location, means controllable to produce permutations of potentials to selectively operate said potential controlled address selecting means, means for selectively applying control potentials, representative of an address number, to said permutation of potential producing means to condition said means to produce potentials to select one chosen address location from said plurality of address locations, means rendering said controllable means operative to operate said address selecting means to read out the selected word manifestation, a computer section, means for entering data manifestations into said computer section, means for rendering said permutation of potential producing means controllable by said read-out selected word manifestation, and means for activating said potential producing means to produce effecting potentials in accordance with said word manifestation, means including said rendering means, acting jointly with said effecting potentials for controlling the steps of computation in said computing section, and means to transfer the calculated result manifestation to said controllable means under control of said rendering means, said activating means rendering said controllable means effective to produce another permutation of potentials for again selecting a stored instruction manifestation at a selected address.

107. A data handling device including storage means containing a plurality of number identified storage addresses, each comprising a storage location for a separate instruction word, potential controlled address selecting means for selecting and rendering available manifestations representative of the word stored at the location selected, means controllable to produce permutations of potentials to selectively operate said potential controlled address selecting means, means for selectively applying control potentials representative of a certain address number to said permutation potential producing means to condition said means to produce selected potentials, to operate said address selecting means to select one chosen address of said plurality of addresses, means rendering said controllable means operative, read-out means including said potential controlled means to read out the instruction word manifestation at the address selected, means including said controllable means, conditioned by said read out instruction word manifestation, means for activating said last mentioned means and means including said last conditioned means for producing a different instruction word manifestation.

108. A device as in claim 107, said producing means including a computer device, said activated conditioned means acting jointly with said rendering means to control said computer device to produce an intermediate result manifestation, testing means producing a test of said intermediate result manifestation and means controlled by said testing means in accordance with the result of said test and including said computer device to selectively produce either the next normal different instruction word manifestation or still another instruction word manifestation, in accordance with the results of said test.

109. A data handling device comprising a storage device having a plurality of separate address locations for holding separate instruction word manifestations, a source of control potentials, potential controlled address selecting means by which the contents of any one of said separate storage locations is made available by the supply of an appropriate group of control potentials, means for receiving a word manifestation from a selected address, means interconnecting said storage and said receiving means, means activating said source to produce a selected potential group for selecting a desired location and transferring the word manifestation selected to said receiving means, means conditioned by the word manifestation at said receiving means, means including the activating means and the source to jointly activate said conditioned means for producing a plurality of potentials representative of said word, and routing means to which said plurality of potentials is applied.

110. A device, as in claim 109, and including means including said source for receiving said plurality of potentials from said routing means, said activating means rendering said last mentioned receiving means operative to apply said potentials to select a potential controlled address selecting means whereby another instruction word is selected.

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References Cited in the file of this patent

UNITED STATES PATENTS

Number	Name	Date
2,079,429	Tauschek	May 4, 1937
2,131,226	Kölm	Sept. 27, 1938
2,176,933	Smith	Oct. 24, 1939
2,236,793	Furber	Apr. 1, 1941
2,283,999	Kozma et al.	May 26, 1942
2,308,778	Prince	Jan. 19, 1943
2,340,809	Hatton et al.	Feb. 1, 1944
2,344,885	Kozma et al.	Mar. 21, 1944
2,379,828	Rubidge et al.	July 3, 1945
2,402,988	Dickinson	July 2, 1946
2,404,047	Flory et al.	July 16, 1946
2,435,841	Morton et al.	Feb. 10, 1948

FOREIGN PATENTS

Number	Country	Date
600,896	Great Britain	Apr. 21, 1948

OTHER REFERENCES

A manual of Operation for the Automatic Sequence Controlled Calculator, by the Staff of the Computation Laboratory, Harvard University Press, 1946.

Predetermined Counter, Electronics, John J. Wild; pages 120–123, March 1947.

Disclaimer

2,636,672.—*Francis E. Hamilton*, Endicott, *Robert R. Seeber, Jr.*, Scarsdale, *Russell A. Rowley*, Binghamton, and *Ernest S. Hughes, Jr.*, Vestal, N. Y. SELECTIVE SEQUENCE ELECTRONIC CALCULATOR. Patent dated Apr. 28, 1953. Disclaimer filed Mar. 1, 1957, by the assignee, *International Business Machines Corporation.*

Hereby enters this disclaimer to claim 20 of said patent.

[*Official Gazette April 2, 1957.*]

Disclaimer

2,636,672.—*Francis E. Hamilton*, Endicott, *Robert R. Seeber, Jr.*, Scarsdale, *Russell A. Rowley*, Binghamton, and *Ernest S. Hughes, Jr.*, Vestal, N.Y. SELECTIVE SEQUENCE ELECTRONIC CALCULATOR. Patent dated Apr. 28, 1953. Disclaimer filed Dec. 18, 1959, by the assignee, *International Business Machines Corporation.*

Hereby enters this disclaimer to claim 59 of said patent.

[*Official Gazette January 26, 1960.*]

Certificate of Correction

Patent No. 2,636,672 April 28, 1953

FRANCIS E. HAMILTON ET AL.

It is hereby certified that error appears in the printed specification of the above numbered patent requiring correction as follows:

Columns 275 and 276, left-hand portion of the example, for

$$\frac{Q}{\text{rbr}} \quad \text{read} \quad \frac{Q}{sbr}$$

column 283, line 14, for "male non-ciitzen unemployed" read *male non-citizen unemployed*; column 286, line 17, in the example, fifth column thereof, under the heading "Qb", second item from the top, for "2" read *4*; column 288, line 69, after "of" strike out the comma; column 293, line 2, for "stablished" read *established*; column 295, line 23, for "squencing" read *sequencing*; column 297, line 30, for "sequence" read *sequencing*; line 70, after "shift" insert a comma; column 298, line 31, after "conditioned" insert *circuit organization controlled by said*; lines 33 and 34, strike out "organization controlled by said circuit"; column 307, line 3, for "producting" read *producing*; column 310, line 62, after "available" insert a comma;

and that the said Letters Patent should be read as corrected above, so that the same may conform to the record of the case in the Patent Office.

Signed and sealed this 16th day of June, A. D. 1953.

[SEAL]

THOMAS F. MURPHY,
Assistant Commissioner of Patents.