IBM

Series/1

SY34-0091-1

IBM Series/1
Common Features
Theory Diagrams

Preface

This manual describes the IBM Series/1 common features, a group of attachment features that communicate directly with the Series/1 processor via the I/O channel. Also described are three unit devices that extend the capabilities of the Series/1 family of processors.

This manual is designed to be used in classrooms for instructing maintenance personnel in the theory of operation of the Series/1 common features. It may also be used as a self-study or reference document in the field.

The presentation level of this manual is oriented to the field replaceable unit (FRU). Diagrams are high-level block-flow that show only the major units within a FRU. Signal lines and power lines between FRUs are described. Voltage levels and pin numbers are given for descriptive purposes only, and must not be used for machine problem analysis. Cable connector information, voltage levels, and pin numbers are listed in the engineering-generated and engineering-change-controlled documentation shipped with each machine.

Related Publications

IBM Series/1 processors and associated devices are described in separate maintenance publications. These publications are shipped from the plant of origin and accompany the device.

Refer to the *IBM Series/1 Graphic Bibliography*, GA34-0055, for a complete listing and description of all IBM Series/1 publications.

Second Edition (November 1979)

This is a major revision of and obsoletes SY34-0091-0. The primary change is the addition of Chapter 11, "Series/1-5250 Information Display System Attachment Feature."

This publication contains information relating the certain feature attachments that are common to the Series/1 family of processors. With the exceptions of Chapters 1, 10, and 11, which were written for this document, this information was previously contained in the *IBM 4953 Processor and Processor Features Theory Diagrams* manual and the *IBM 4955 Processor and Processor Features Theory Diagrams* manual, SY34-0042 and SY34-0041, respectively.

Use this publication only for the purpose stated in the Preface.

Changes are periodically made to the information herein; any such changes will be reported in subsequent revisions or Technical Newsletters.

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Contents

Chapter 1. Introduction

The IBM Series/1 common features are attachment features that communicate directly with the Series/1 processor via the I/O channel. These features are:

- Timer
- Teletypewriter Adapter
- Integrated Digital Input/Output Non-Isolated
- Customer Direct Program Control Adapter
- Series/1–System/370 Channel Attachment
- Two-Channel Switch for IBM 4959 I/O Expansion Unit
- Series/1-5250 Information Display System Attachment

In addition to the features that communicate via the I/O channel, the common features also include:

- 4959 I/O Expansion Unit
- 4993 Series/1–System/370 Model 1 Termination Enclosure (installed concurrently with Series/1–System/370 Channel Attachment)
- 4999 Battery Backup Unit

The descriptions of the common features and the processor I/O channel given in this chapter are provided as a brief overview for the reader. For a functional description of the processor I/O channel, refer to the appropriate Series/1 processor theory diagrams manual.

Common Features

Timer Feature

The Timer feature printed-circuit card has two separately addressable 16-bit timers, each of which can generate periodic or aperiodic interrupts to the processor. Each timer may be used as an interval timer, pulse counter, or pulse duration counter with end interrupt. Each timer is started, stopped, read, or set to a value by program control.

Teletypewriter Adapter Feature

The Teletypewriter Adapter feature printed-circuit card provides the circuitry to attach a Teletype* model ASR33/ASR35, or equivalent, to the channel of the processor. However, any serial-by-bit I/O device that meets the interface requirements of the adapter can be attached. All communications between the adapter and the processor are initiated by Operate I/O instructions executed in the processor.

Integrated Digital Input/Output Non-Isolated Feature

The Integrated Digital I/O feature printed-circuit card contains two 16-bit groups of non-isolated digital input/process interrupt (DI/PI), and two 16-bit groups of non-isolated digital output (DO).

Each group of DI/PI and DO has ready and sync lines for synchronizing operations with the attached devices.

All DI/PI and DO functions are initiated by Operate I/O instructions executed in the processor.

Customer Direct Program Control Adapter

The Customer Direct Program Control Adapter feature printed-circuit card allows I/O devices to be attached directly to the processor channel. The adapter performs direct program control (DPC) operations only; cycle-steal operations cannot be performed.

This feature card can be configured to accommodate 4, 8, or 16 I/O device addresses.

Series/1–System/370 Channel Attachment Feature

The Series/1–System/370 Channel Attachment feature printed-circuit card allows channel-to-channel communications between a Series/1 processor and members of the System/370 family of computers.

The feature appears as a control unit, with 32 device addresses, to the System/370 and connects to the System/370 selector or block multiplexer channel. The 4993 Model 1 Termination Enclosure is installed concurrently with this feature.

Two-Channel Switch Feature

The Two-Channel Switch (TCS) feature printed-circuit card is installed in a 4959 I/O Expansion Unit and allows program-initiated or manual switching of the 4959 I/O Expansion Unit between two Series/1 processors. This feature is designed to support a primary/backup type of operation. A processor-controlled timer, which is located on the TCS feature card, monitors the operation of the primary processor. If a time-out occurs, the TCS feature notifies the backup processor of the time-out condition, and the backup processor can assume control of the I/O features in the 4959 I/O Expansion Unit.

An operator console containing switches and indicators is located on the 4959 that contains the Two-Channel Switch feature card.

4959 Input/Output Expansion Unit

The 4959 I/O Expansion Unit expands the I/O feature and device capacity of the processor. The capacity of the 4959 is 14 I/O features or 13 I/O features plus a channel repower card. Power is provided by a multilevel power supply.

4993 Model 1 Series/1–System/370 Termination Enclosure

The 4993 Model 1 Series/1–System/370 Termination Enclosure is installed concurrently with the Series/1–System/370 Channel Attachment feature. The 4993-1 provides a power supply and channel driver/receiver circuitry for connecting the System/370 bus and tag channel cables to the attachment logic.

4999 Battery Backup Unit

The 4999 Battery Backup Unit provides ac power to the processor when the ac line voltage is temporarily lost or inadequate. The 4999 converts the battery-supplied 12 Vdc to the ac voltage required by the processor when an ac line-voltage failure occurs; otherwise, it supplies the ac line voltage directly to the processor.

Series/1-5250 Information Display System Attachment Feature

The Series/1-5250 Information Display System Attachment feature printed-circuit cards allows direct local attachment of display stations and printers from the 5250 Information Display System family. Utilizing a single Series/1 device address, the attachment handles all communications between the processor and up to eight addressable work stations.

Processor I/O Channel

The processor I/O channel provides a link between the processor and the I/O features and devices.

The processor I/O channel supports the following basic operations:

- *Direct program control (DPC) operations.* During a DPC operation, an immediate data transfer is made between main storage and the device for each Operate I/O instruction. The data may consist of one byte or one word. The operation may or may not terminate with an interrupt.
- *Cycle-steal operations.* During cycle-steal operations, an Operate I/O instruction can initiate cycle-steal data transfers up to 65,535 bytes (per device control block) between main storage and the device. Cycle-steal operations are overlapped with processing operations.
- *Interrupt servicing.* Four priority interrupt levels are available to facilitate device service. The interrupt level is assigned to a device by execution of an Operate I/O instruction (with the Prepare command and the interrupt level specified in the immediate device control block).
- *Initial program load (IPL) operations.* During an IPL operation, a record consisting of initial instructions for the processor is read into main storage from either the primary or alternate IPL device, or from a host system.

The channel provides comprehensive error checking, including timeouts, sequence checking, and parity checking. Reporting of errors, exceptions, and status is accomplished by (1) recording condition codes in the processor during execution of Operate I/O instructions and (2) recording condition codes and an interrupt information byte (IIB) in the processor during interrupt acceptance. Additional status words are used by the device, as necessary, to describe its status.

The I/O channel is asynchronous and multidropped. Except when timeout conditions are used for error detection, each sequential action is triggered by an I/O device response rather than by a specified timing condition.

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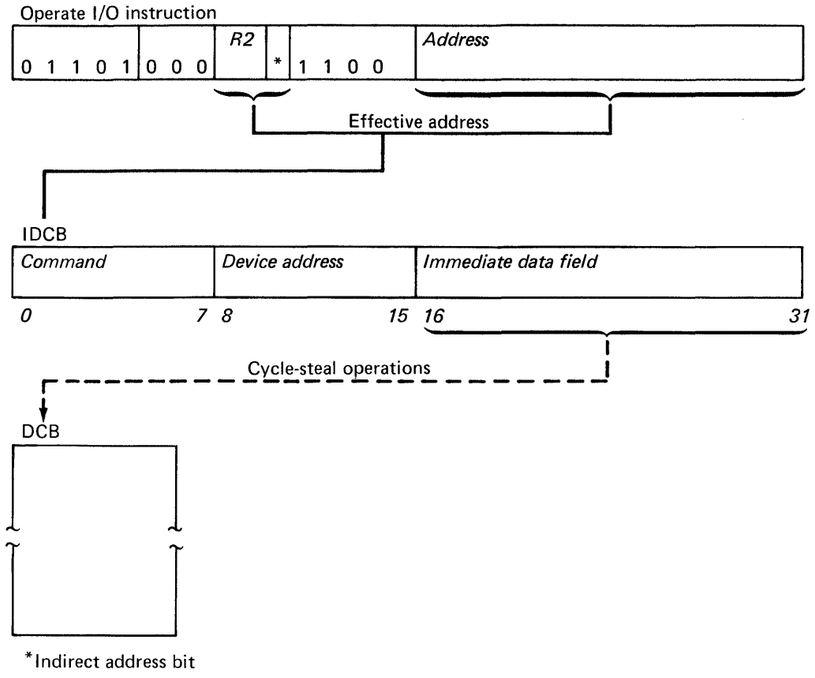
* Trademark of the Teletype Corporation

Operate I/O Instruction



*Indirect address bit

The Operate I/O instruction initiates I/O operations from the processor. The effective address generated by this instruction points to an immediate device control block (IDCB). The IDCB contains the *command field*, *device address field*, and the *immediate data field*.

I/O Commands

The first byte of the IDCB contains the command field and is used to initiate a specific operation on the processor I/O channel.

The first hex digit of the command field identifies the type of command; the second hex digit is the modifier.

Hex*	Specific command	Type of operation
0X	Read	DPC
1X	Read	DPC
20	Read ID	DPC
2X	Read status	DPC
4X	Write	DPC
5X	Write	DPC
60	Prepare	DPC
6X	Control	DPC
6F	Device reset	DPC
7X	Start	Cycle steal
7F	Start cycle steal status	Cycle steal
F0	Halt I/O	Channel

* The X indicates that the modifier is device-dependent.

Device Address

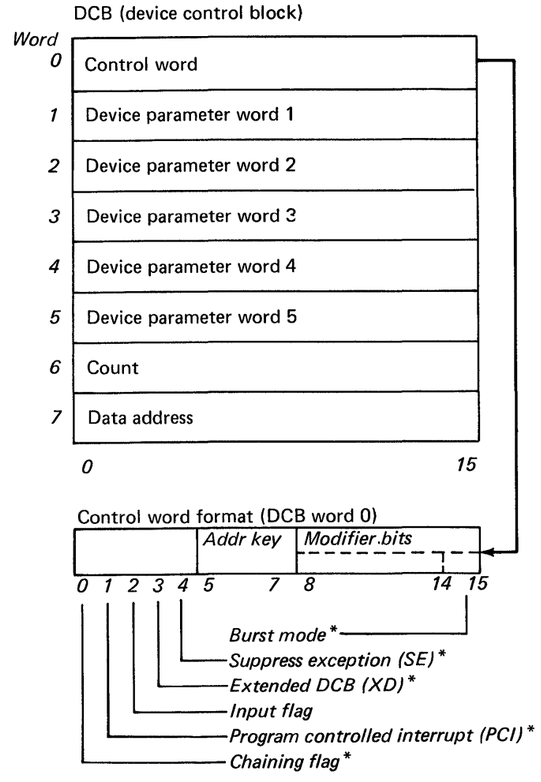
The second byte of the IDCB contains the device address field. The device addresses are defined by jumpers on the I/O attachment printed-circuit cards. The I/O channel is capable of addressing 256 (0–255) individual devices.

Immediate Data Field

During DPC operations, this two-byte field contains the word to be written to the I/O device or the word read from the I/O device. For cycle-steal operations, this field contains the address of the device control block (DCB).

Device Control Block (DCB)

The DCB is an eight-word control block, residing in main storage, that describes the specific parameters of the cycle-steal operation. The addressed device fetches the DCB after accepting a cycle-steal command.



*Device option bits

I/O Instruction Condition Codes

Each time an Operate I/O instruction is issued, the device or channel reports to the processor a condition code that reflects the execution status of the I/O command. Three bits of the level status register (LSR) are used to encode a condition code value of 0–7. The bits of the LSR used are the even, carry, and overflow bits.

These codes are reported during execution of an Operate I/O instruction:

Condition code (CC) value	LSR position Even	Carry	Over-flow	Reported by	Meaning
0	0	0	0	Channel	Device not attached
1	0	0	1	Device	Busy
2	0	1	0	Device	Busy after reset
3	0	1	1	Chan/dev	Command reject
4	1	0	0	Device	Intervention required
5	1	0	1	Chan/dev	Interface data check
6	1	1	0	Controller	Controller busy
7	1	1	1	Chan/dev	Satisfactory

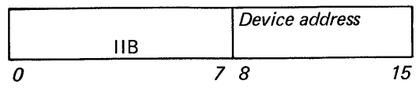
Interrupts

The processor uses an interrupt scheme of four priority levels of interrupt to service device requests on the I/O channel. These levels, listed in priority sequence, are numbered 0, 1, 2, and 3, with level 0 having the highest priority. Interrupt levels are assigned to I/O devices via program control (Operate I/O instruction with the Prepare command and the level specified in the IDCB).

Interrupt masking facilities provide additional program control over the four priority levels. Manipulation of the interrupt mask bits can enable or disable interrupts on all levels, a specific level, or for a specific device.

When an interrupt request from an I/O device is accepted, the device presents an interrupt ID word and a condition code to the processor. The automatic interrupt branching facility of the processor then branches to a program service routine to service the device request.

Interrupt ID Word



The two-byte interrupt ID word consists of the interrupt information byte (IIB) and the device address, and has the following format:

Bits 0–7 *Interrupt information byte (IIB).* For interrupt condition codes 2 and 6, the IIB has a special format, and is called an *interrupt status byte (ISB).* For other interrupt condition codes, the bit definition of the IIB is device-dependent. Exceptions are:

1. CC=0. The IIB is set to 0.
2. CC=1 or 5. The IIB contains a DCB identifier.
3. CC=3 or 7. Bit 0 may be set to 1 if suppress exception is in effect.

Bits 8–15 *Device address.* This byte contains the address of the interrupting device.

Interrupt Status Byte (ISB)

This special format of the IIB has the following meanings:

For DPC devices:

Bit	Contents
0	Device status available
1	Delayed command reject
2–7	Device-dependent

For cycle-steal devices:

Bit	Contents
0	Device status available
1	Delayed command reject
2	Incorrect length record
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

* This bit is 0 for a device attached to a processor without the storage protect feature.

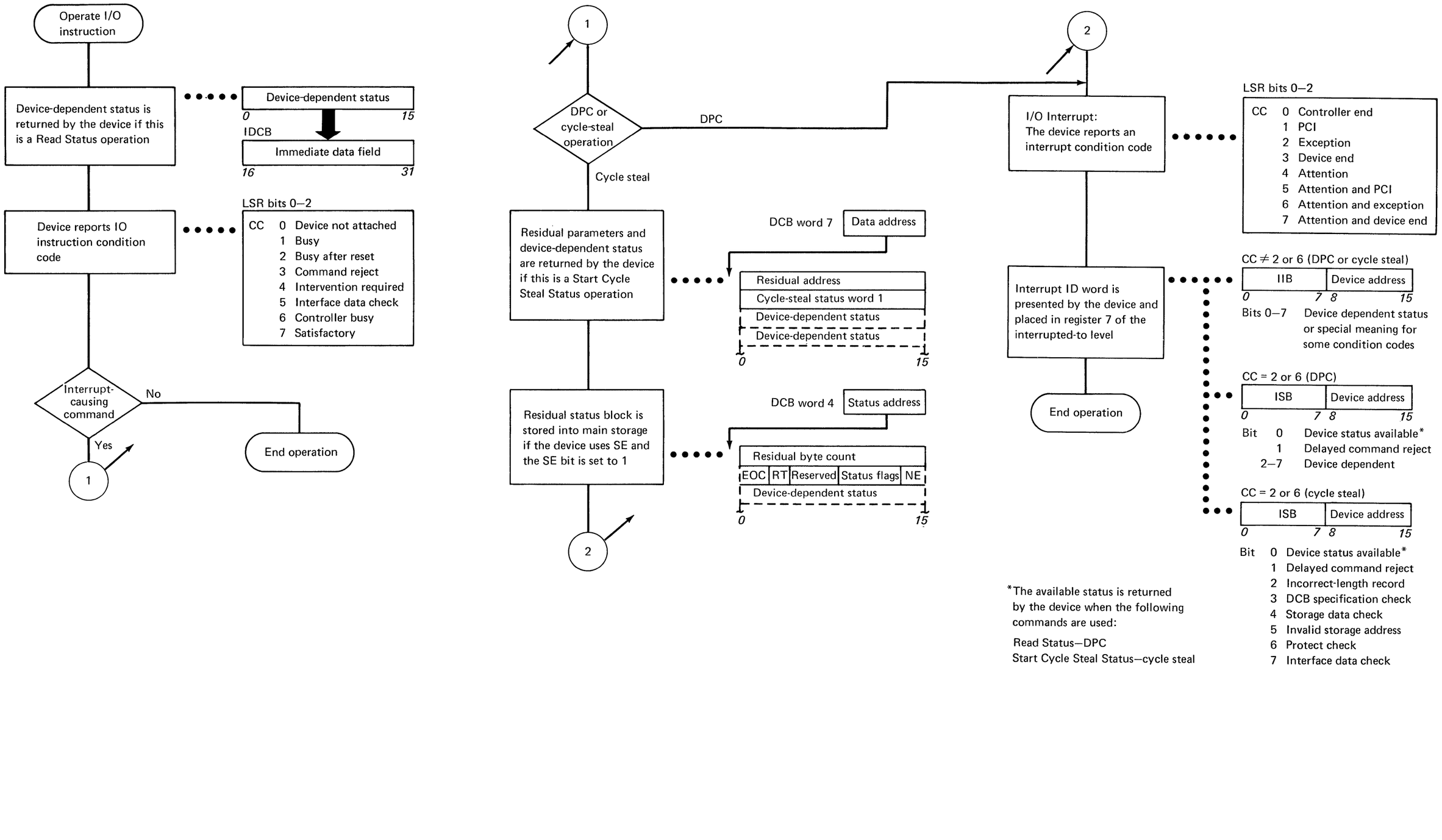
I/O Interrupt Condition Codes

When the device interrupt request is accepted, the device sends an interrupt condition code to the processor, identifying the purpose of the interrupt. Three bits of the level status register (LSR) of the interrupted-to level are used to encode a condition-code value of 0–7. The bits of the LSR used are the even, carry, and overflow bits.

The condition codes reported during interrupt acceptance are:

Condition code (CC) value	LSR position Even	Carry	Overflow	Reported by	Meaning
0	0	0	0	Channel	Device not attached
1	0	0	1	Device	Program-controlled interrupt (PCI)
2	0	1	0	Device	Exception
3	0	1	1	Device	Device end
4	1	0	0	Device	Attention
5	1	0	1	Device	Attention and PCI
6	1	1	0	Device	Attention and exception
7	1	1	1	Device	Attention and device end

I/O Device Condition Codes and Status Information Flowchart



Chapter 2. Special Maintenance Equipment

There are three special maintenance tools that may be required during certain maintenance procedures when servicing the Series/1 processor or the 4959 I/O Expansion Unit. These tools are:

1. The maintenance program load device
2. The maintenance communications panel
3. The maintenance console

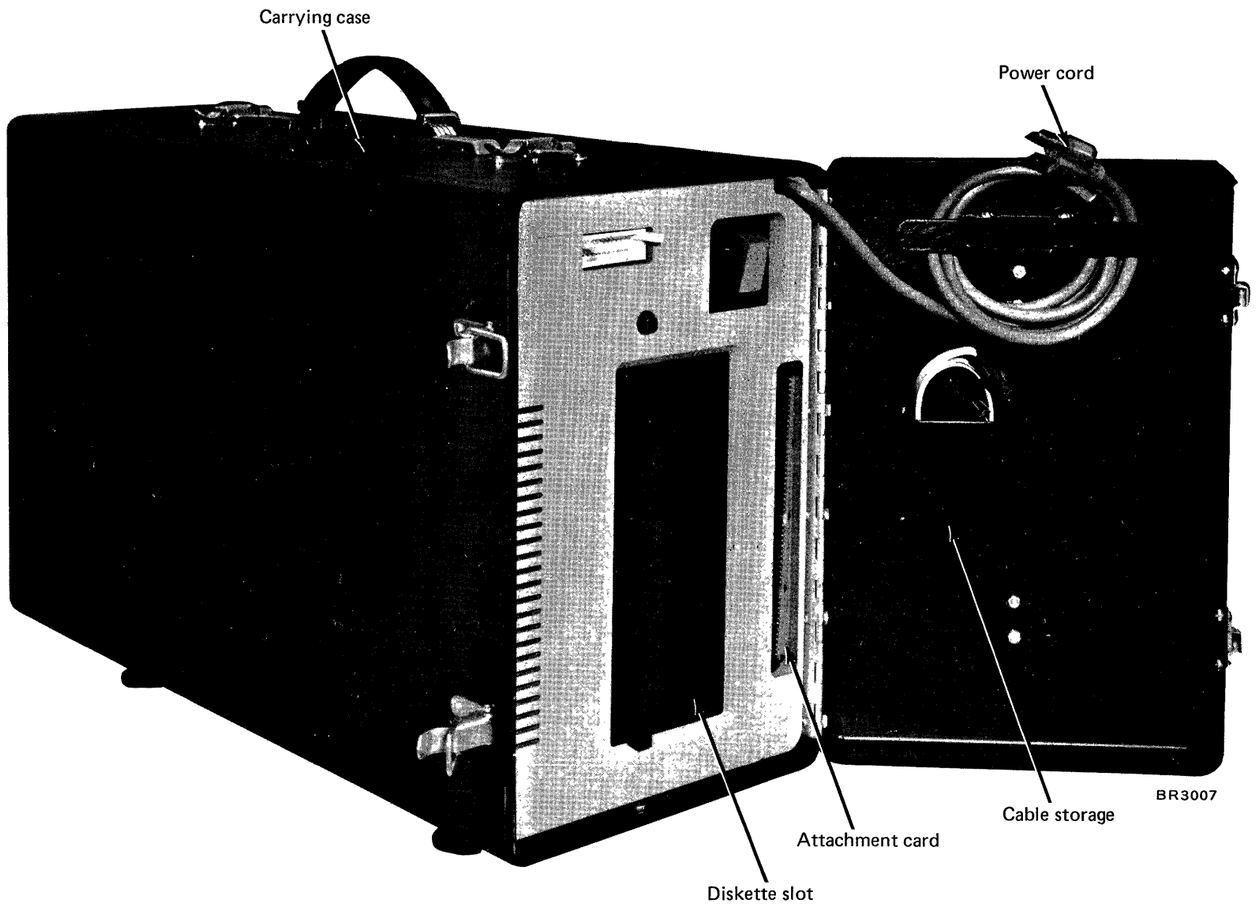
Note: Other special maintenance tools are required for maintenance of specific I/O devices. The descriptions and uses of these tools are covered in the maintenance manuals relating to the I/O device.

Maintenance Program Load Device

The maintenance program load device is used if the configuration of the Series/1 being serviced either does not include an IBM diskette unit or if the diskette unit is incapable of loading programs into processor storage.

The maintenance program load device contains an attachment card and cable, and a power cord. The attachment card is plugged into an available I/O slot in either the processor or the 4959 I/O Expansion Unit. If no I/O slot is available, one of the attachment cards must be removed. The power cord can be plugged into any available, properly grounded ac outlet.

Details for attaching and operating the maintenance program load device are described in the appropriate processor's maintenance information manual.



Maintenance program load device

Maintenance Communications Panel

The maintenance communications panel is used for maintenance of the communication features when the optional communications indicator panel is not included in the system configuration. The maintenance communications panel consists of the panel, a carrying case, and an attachment cable.

Details for attaching the maintenance communications panel are found in the appropriate processor's maintenance information manual.

A description of the keys and indicators on the panel can be found in *IBM Series/1 Communications Theory Diagrams*, SY34-0059.

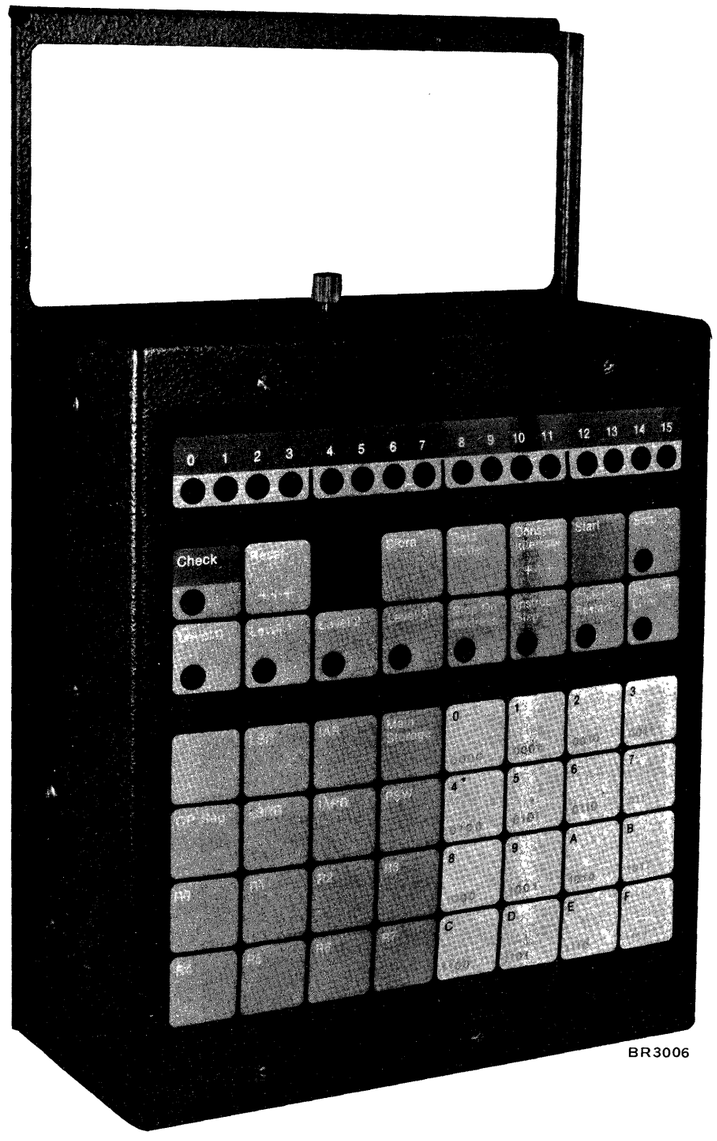
Communications panel in carrying case

Maintenance Console

The maintenance console is necessary when the processor being serviced does not contain the optional programmer console feature. The maintenance console has operating functions identical to the programmer console.

The maintenance console consists of the console, a protective case, and attaching cables.
Details for attaching the maintenance console are found in the appropriate processor's maintenance information manual.

A description of the keys and indicators is located in the appropriate processor's theory-diagrams manual.

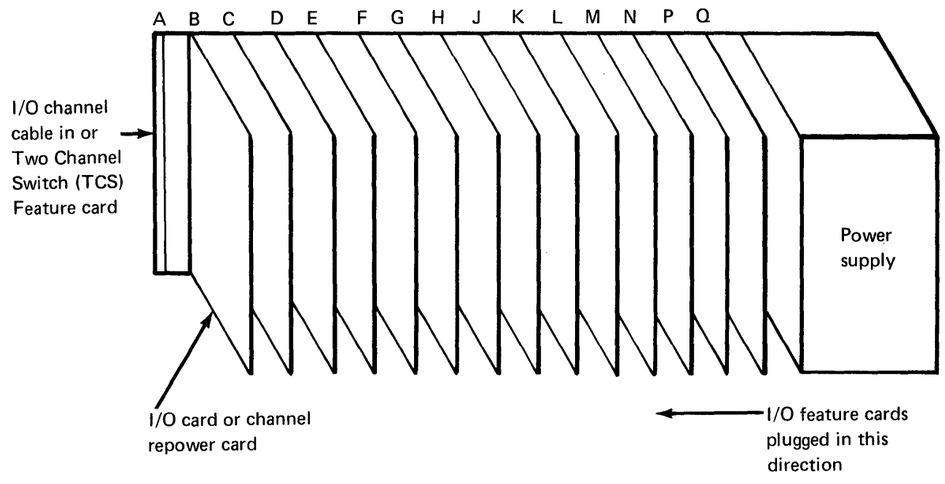


Maintenance console in case

Chapter 3. IBM Series/1 4959 Input/Output Expansion Unit

Description

The IBM Series/1 4959 Input/Output Expansion Unit is available for adding I/O feature cards beyond the capacity of the Series/1 processor unit. The expansion unit is a standard 48.3 centimeter (19 inch) rack-mountable assembly, and contains a power supply, cooling fans, and 15 card slots. The general layout of the unit is shown here:

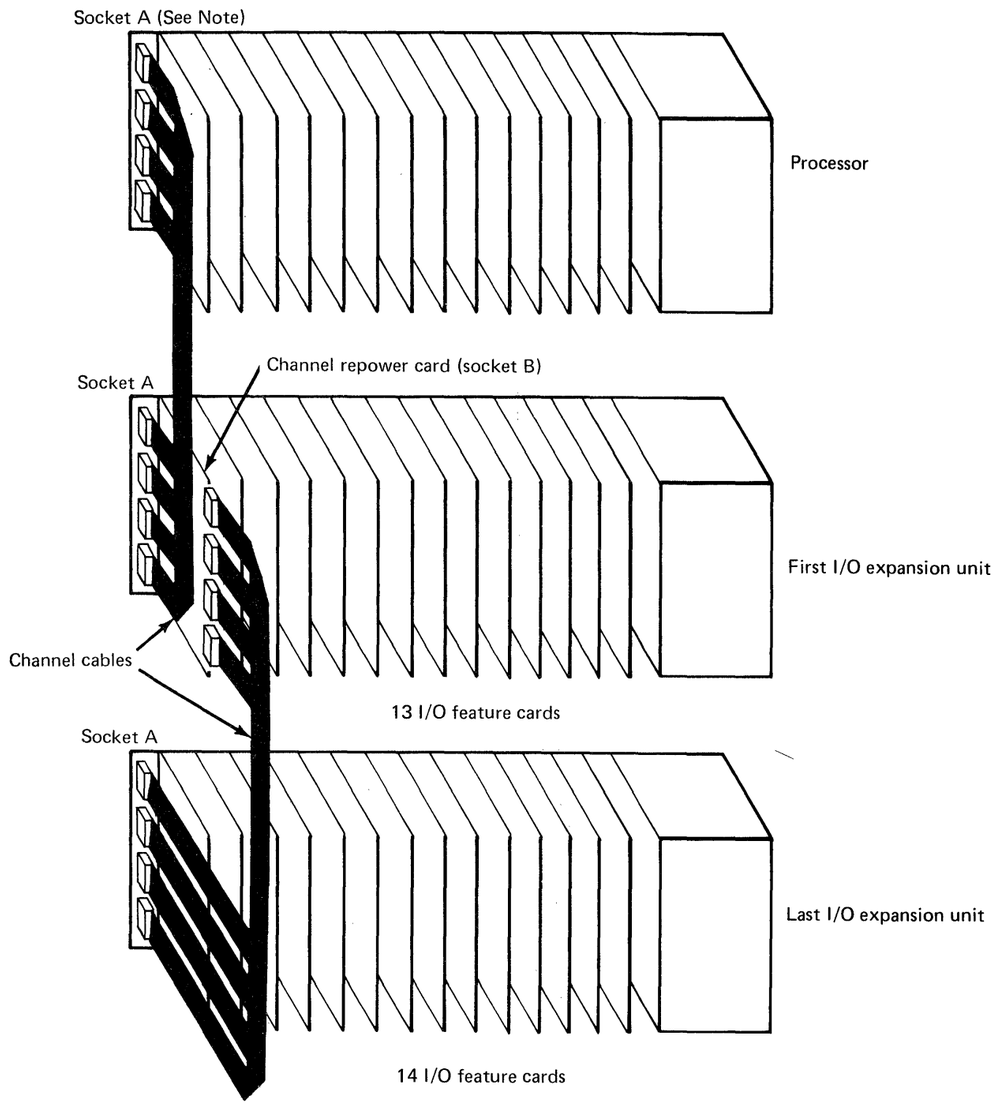


IBM 4959 Input/Output Expansion Unit

Cabling

The I/O channel cables plug into socket A. If the optional Two-Channel Switch (TCS) Feature is installed in socket A, the channel cables plug into cable connectors on the TCS feature card. Socket B is reserved for the channel repower feature if cabling is required to another I/O expansion unit; however, the channel repower feature is not required in an I/O expansion unit that contains a TCS feature card. If this is the last expansion unit on the channel, socket B can be used for an I/O feature.

The I/O channel cables consist of four unshielded flat cables. Each cable contains 20 signal and 3 ground lines.



Note: Series/1 processors, other than the 4955 processor, require the channel repower feature in socket A if an I/O expansion unit is installed.

Power Supply Voltage/Signal Distribution

Socket	Voltage/signal	Pins
S2 and S5	+5 Vdc	B04-B11
	Ground	D04-D11
S3	+12 Vdc	B04-B07
	−5 Vdc	B08-B11
	−12 Vdc	D04-D07
	+8.5 Vdc	D08-D11
S4	Power-on reset (not)	B04
	Power/thermal warning (not)	B05
	AC failure	B10
	AC failure return	B11
	Ground	D08

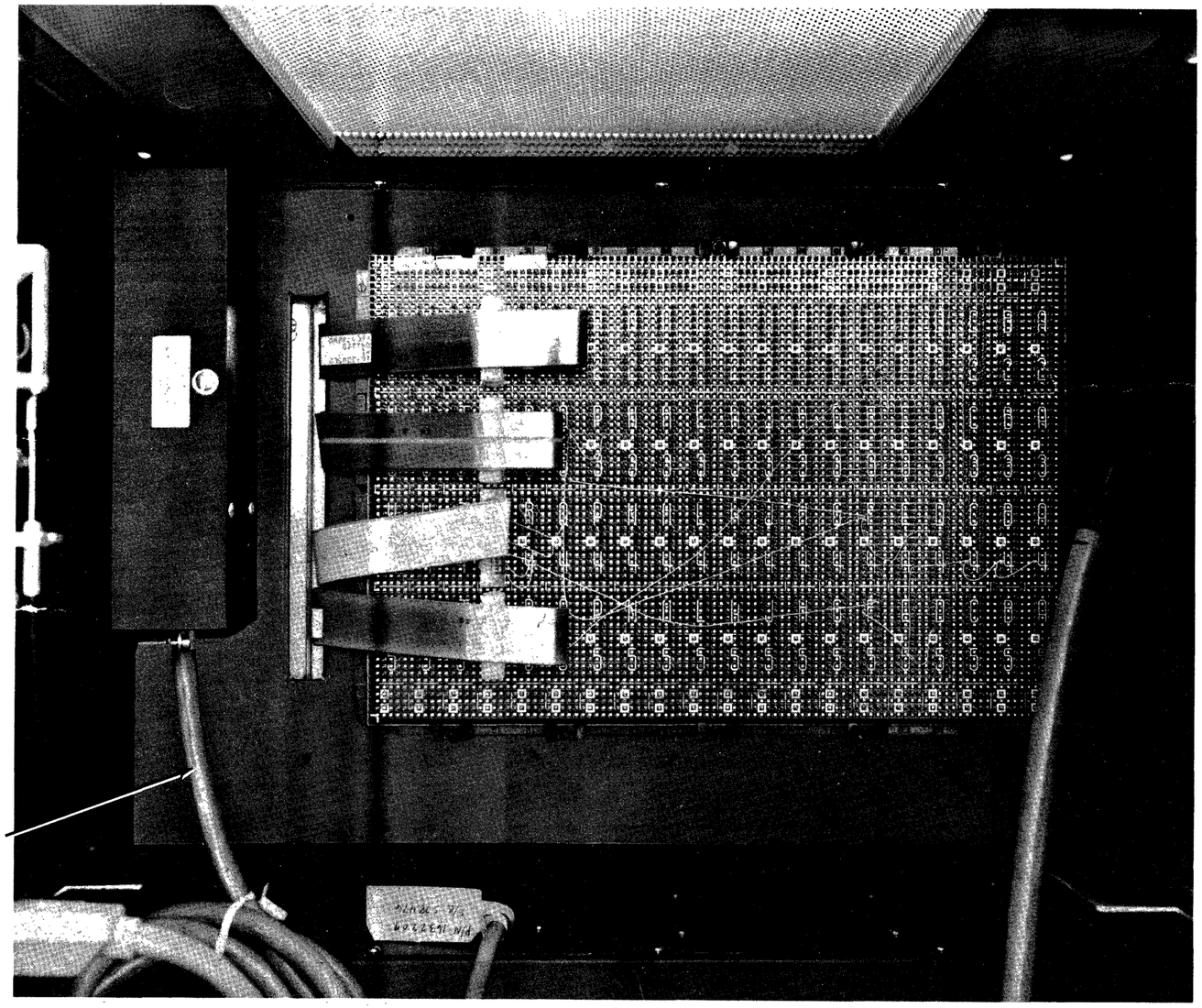
Distribution across the board (columns B–Q) is through internal planes. Rows 2, 3, and 4 contain ±5 Vdc, +8.5 Vdc, and ground. Row 2 also contains ±12 Vdc (optional).

Column A is used for the incoming channel cables or the Two-Channel Switch Feature card. Column A ground pins are B06, B11, and D08. The only voltage to column A is +5 Vdc on the D03 pins.

Power Supply Signals

The power supply provides input signals to the I/O expansion unit, as follows:

- Power-on reset
  - Provided to ensure the state of the circuit logic during power-on and power-off sequences.
  - Provides a reset when the ±5 Vdc, the +8.5 Vdc, and the ±12 Vdc (if installed) are within operational limits.
  - Causes a power down if any of the three (or five) voltages fall below approximately 3% of their minimum tolerance.
- Power/thermal warning
  - Indicates an overtemperature condition or a low ac power condition, and causes a power down. This signal is not distributed across the board.



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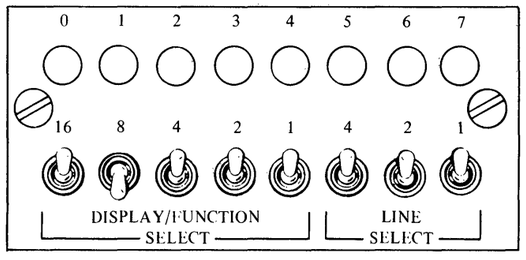
Optional Features

Communications Indicator Panel

The Communications Indicator Panel is available as an option when a communications feature is installed in the expansion unit. This panel provides a means of displaying various states, conditions, and lines of the communications feature. It also provides for manual control of certain lines to the modems.



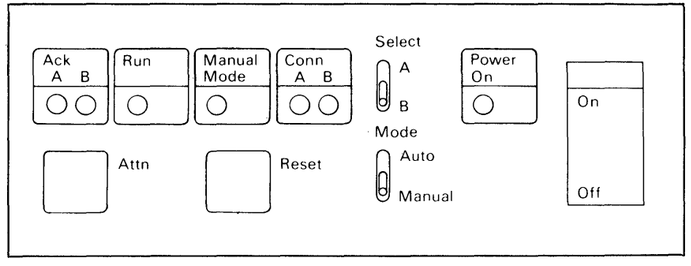
The indicator panel may be used with any of the communications features, one at a time. The panel connects to a connector on the feature control card, and can be moved between I/O expansion units or processor units. Therefore, it is not necessary to have more than one indicator panel.

The indicator panel mounts under the front cover of the I/O expansion unit via two thumb screws. The panel provides different information for each type of communications feature. Refer to *IBM Series/1 Communications Theory Diagrams*, SY34-0059, for operating instructions.

Two-Channel Switch Feature

The Two-Channel Switch (TCS) Feature can be installed to allow a primary/backup type of operation of the I/O expansion unit between two Series/1 processors. The TCS feature card is installed in socket A of the I/O expansion unit. An operator's console, containing switches and indicators, is located on the I/O expansion unit when the TCS feature is installed.

Refer to Chapter 9, "Two-Channel Switch Feature," in this publication for additional information.



Chapter 4. IBM Series/1 4999 Battery Backup Unit Models 1 and 2

Description

The primary purpose of the IBM 4999 Battery Backup Unit is to monitor the ac line voltage, and to provide square wave ac power to the Series/1 processor when the ac line voltage is either temporarily lost or inadequate. The 4999 is a dc-to-ac inverter when activated; otherwise, it supplies the line voltage directly to the processor unit.

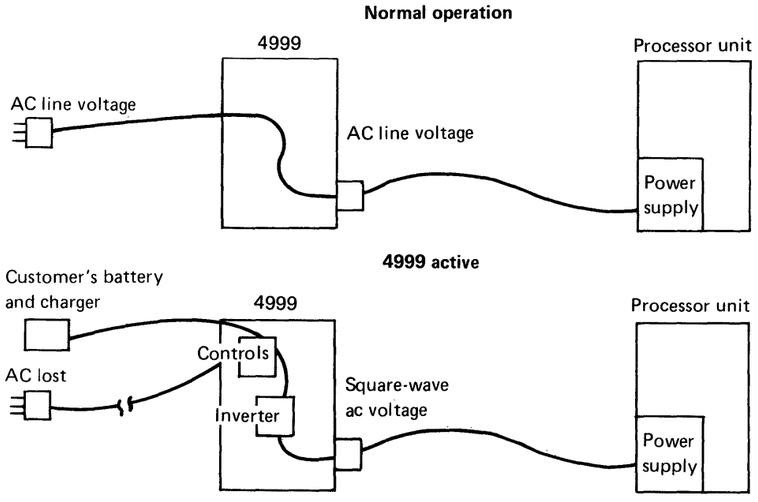
Note: Model 1 is for 100–127 Vac applications; Model 2 is for 200–240 Vac applications. For those parameters where the Model 2 differs from the Model 1, the corresponding value for the Model 2 follows immediately in parentheses.

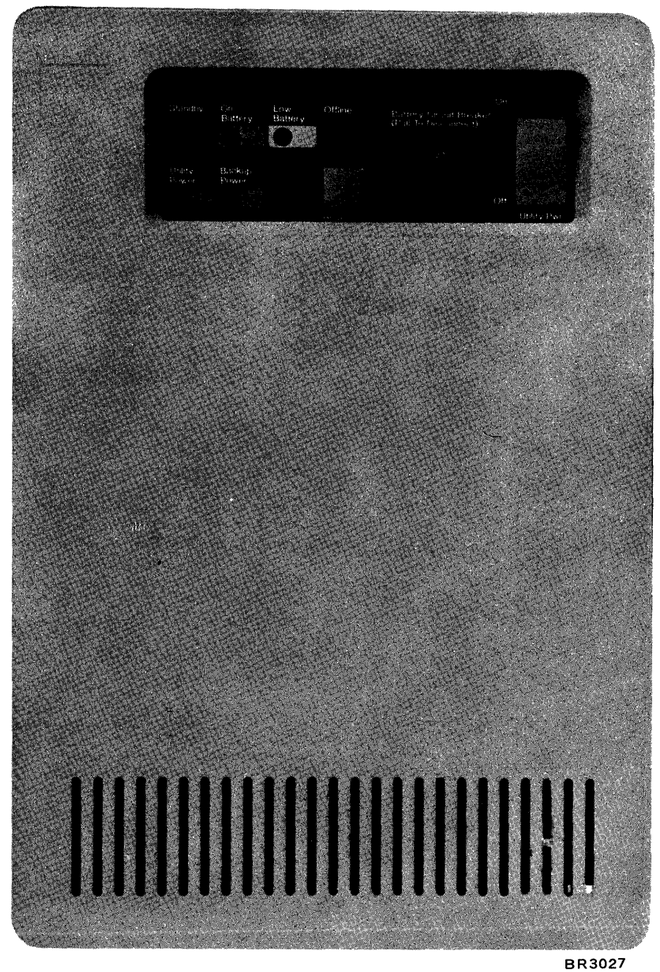
The 4999 supports Series/1 processors that have an input power requirement of 530 watts (unity power factor) or less, measured at the processor primary power input. The 4999 does not support a Series/1 processor that uses a ferroresonant power supply (for example, a 4952 Model A).

When installed with the appropriate processor, the 4999 supports only the processor unit, processor features, and processor cooling fans; it does not support a 4959 I/O expansion unit or any I/O devices.

A processor supported by a 4999 must be power isolated via the channel repower feature if a 4959 I/O expansion unit is attached.

The 4999 is used to prevent data loss in main storage during a temporary ac line voltage dip or loss. The 4999 is connected to the ac line voltage and to a user-supplied 12-volt battery and charger unit. The processor unit line cord plugs into an outlet socket on the back of the 4999. During normal operation, the 4999 transfers the ac utility power directly to the processor power supply. When a dip in the ac utility power occurs, or if the ac utility power is lost, the 4999 dc-to-ac inverter is switched on, and begins to supply a square-wave ac voltage to the processor power supply and cooling fans. When ac power returns, the 4999 switches back to the ac utility power. If battery capacity is exceeded before the ac returns, the 4999 switches back to the utility line to allow repowering when the line voltage eventually returns.





4999 Console

Standby Indicator Ⓐ

The Standby indicator is on when the following conditions are satisfied:

1. The Utility/Pwr switch is set to the On position and the reset pushbutton was pressed when the line voltage was at least 87.5 (175) volts.
2. The processor unit power supply is on.
3. The ac line voltage is above 80 (160) volts
4. An offline condition is not present; that is, from the time the Reset pushbutton was pressed, the battery voltage has not fallen below approximately 10.8 volts.

On Battery Indicator Ⓑ

The On Battery indicator is on when backup power is being supplied from the battery-powered inverter. The on-battery mode occurs within 15 milliseconds after sensing a line voltage below 80 (160) volts.

While in the on-battery mode, both the ac line voltage and the battery voltage are monitored. If the battery voltage drops below approximately 11.2 volts, the Low Battery indicator is turned on, but no further action is taken. If the battery voltage falls below approximately 10.8 volts, an *offline* shutdown occurs.

Assuming that no offline shutdown has occurred, when the ac line voltage returns to approximately 87.5 (175) volts, the Battery Backup Unit (BBU) switches back to the standby mode within 15 milliseconds. Once the processor unit is on battery power, it remains so for at least 0.5 second.

Note: The processor unit must be initially powered from the ac line before the IBM 4999 Battery Backup Unit allows the backup mode to occur. If the ac line is too low to permit the processor to be powered-on from the line, then it cannot be powered-on from the 4999. If the line voltage is below the 4999 specified limit, but is still capable of powering-on the processor, then the 4999 takes over powering of the processor after the processor's power supply becomes operational.

Low Battery Indicator Ⓒ

The Low Battery indicator turns on whenever the battery voltage falls below approximately 11.2 volts. Once the Low Battery indicator is activated, it is not turned off until the battery voltage recovers to approximately 12.5 volts.

Offline Indicator Ⓓ

The Offline indicator turns on when the battery voltage drops below approximately 10.8 volts, or when the 4999 is initially powered-on.

If the Battery Backup Unit was operating in the *on-battery* mode, the processor unit is switched back to the ac line. If the line voltage has not returned, the processor unit is powered down.

If the Battery Backup Unit was previously in standby mode, the processor unit continues operating from the ac line as long as the line is normal. If the ac line drops, the Battery Backup Unit does not transfer to the battery and the processor unit is powered down.

The Offline indicator remains on until:

1. The battery voltage has recovered to approximately 12 volts, and
2. The Reset pushbutton has been pressed.

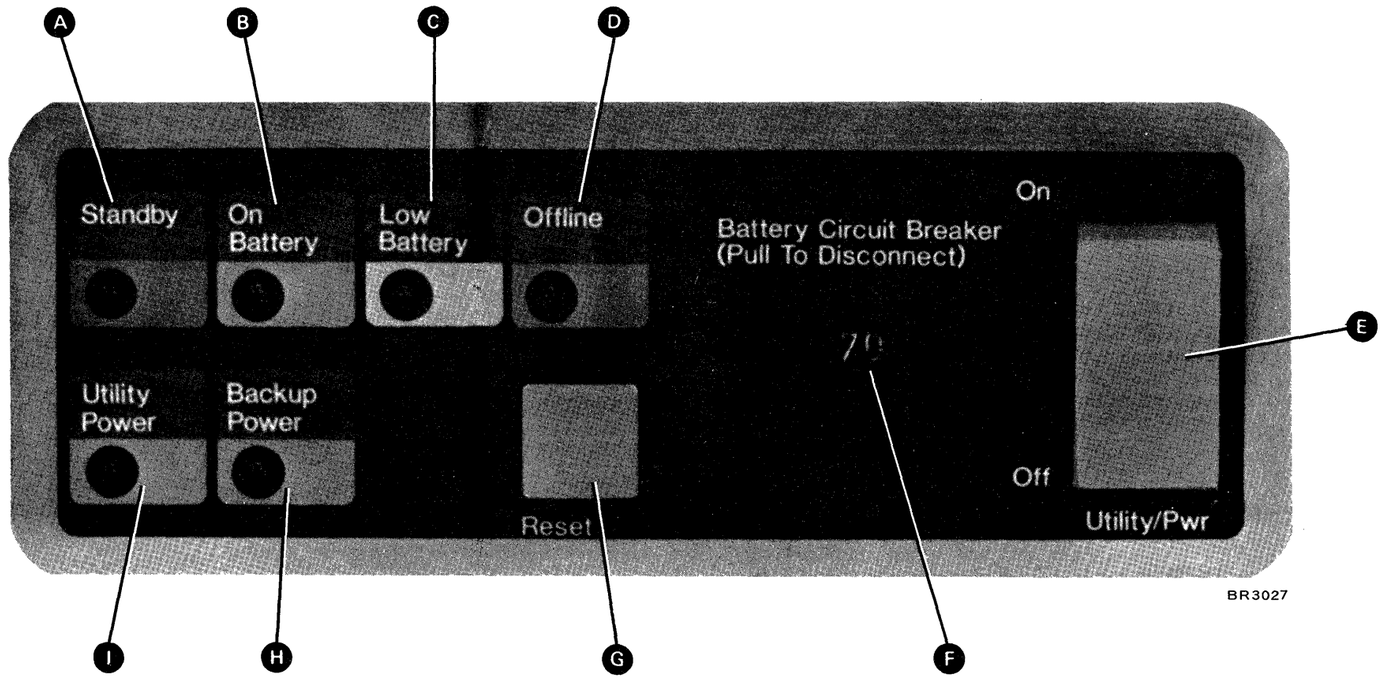
Utility/Pwr Switch Ⓔ

When the Utility/Pwr switch is set to On, ac power is applied to the Battery Backup Unit, and the Utility Power indicator turns on. Power is also supplied to the receptacle for the processor unit.

When the switch is set to Off, ac power is removed from the Battery Backup Unit and from the receptacle for the processor unit. The Utility Power indicator is turned off.

Battery Circuit Breaker Ⓕ

The 70-ampere Battery Circuit Breaker on the front panel operates automatically if excessive battery current is being used. The circuit breaker can also be operated manually. When the circuit breaker is pushed in, the battery is connected and the Backup Power indicator is turned on. When the circuit breaker is pulled out, the battery is disconnected and the Backup Power indicator is turned off.



Reset Pushbutton Ⓖ

Reset is a momentary-contact pushbutton. Pressing the pushbutton resets the Battery Backup Unit after power is initially turned on, or after an *offline shutdown* if the battery voltage has recovered to at least 12 volts.

Backup Power Indicator Ⓗ

The Backup Power indicator is always on when the battery power is available and the Battery Circuit Breaker is closed.

Utility Power Indicator Ⓘ

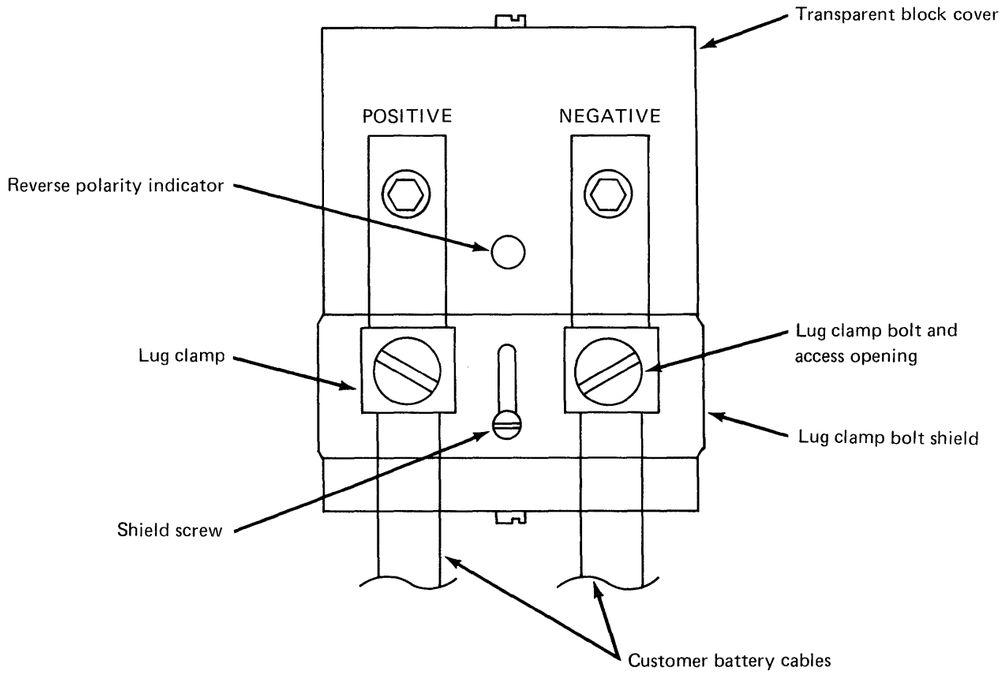
The Utility Power indicator is on when the Utility/Pwr switch is set to the On position and ac line voltage is available to the IBM 4999 Battery Backup Unit.

Battery and Battery Charger

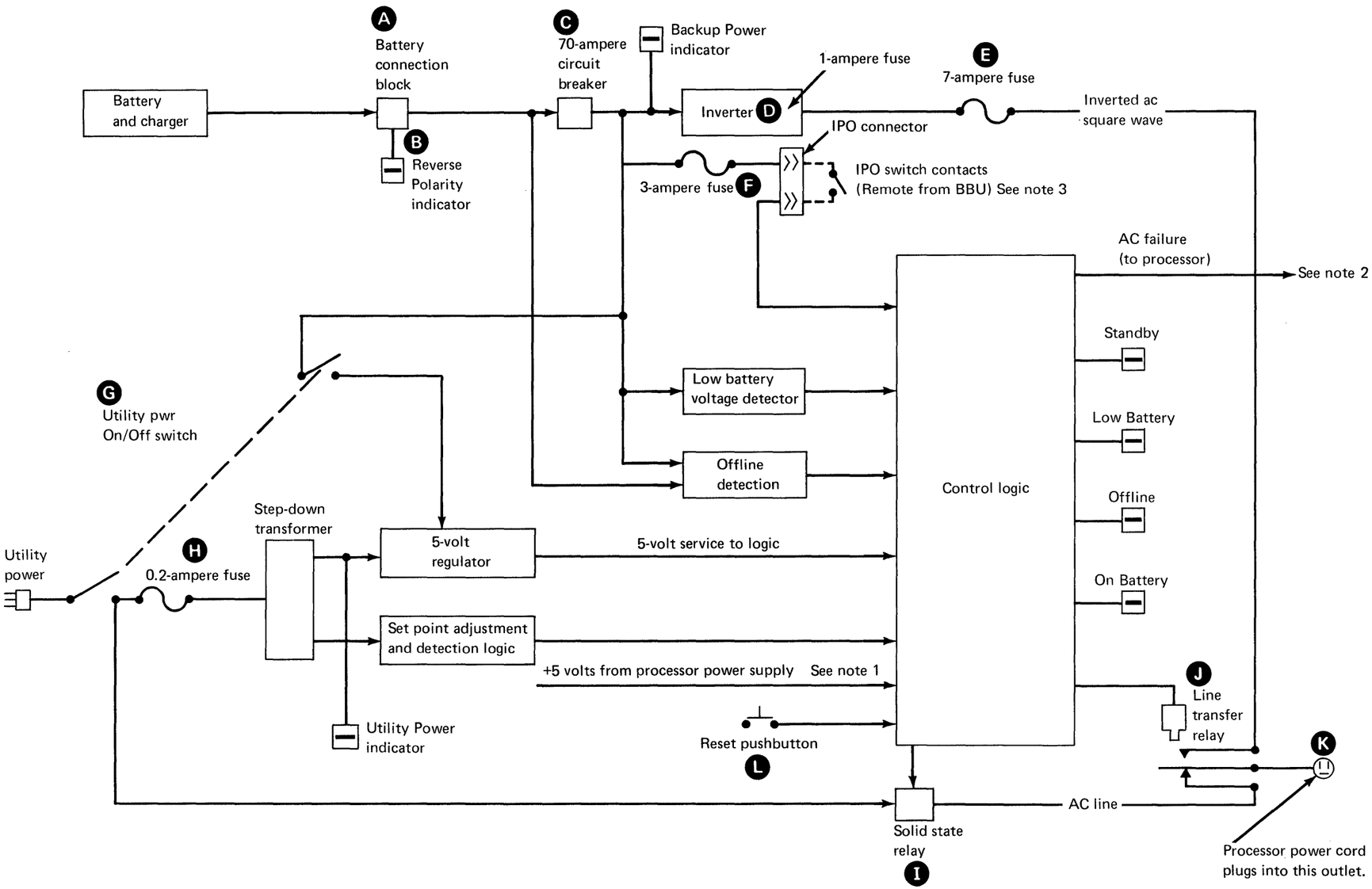
The battery and battery charger are both supplied by the customer. The battery rating must be at least 40-ampere hours at the 1-hour discharge rate. The *recommended* battery is the sealed-cell, automotive, lead-acid type, rated at 100-ampere hours or more. A 100-ampere-hour battery can power the inverter from 20 to 60 minutes between charges, depending on the load, temperature, and the state of charge and condition of the battery.

The battery must be connected to the battery connection block as indicated. Accidental reverse connection does not damage the 4999, but the unit is not activated and the Reverse Polarity indicator is flashed on and off to indicate the connection error.

Battery Connection Block



4999 Logic Block Diagram

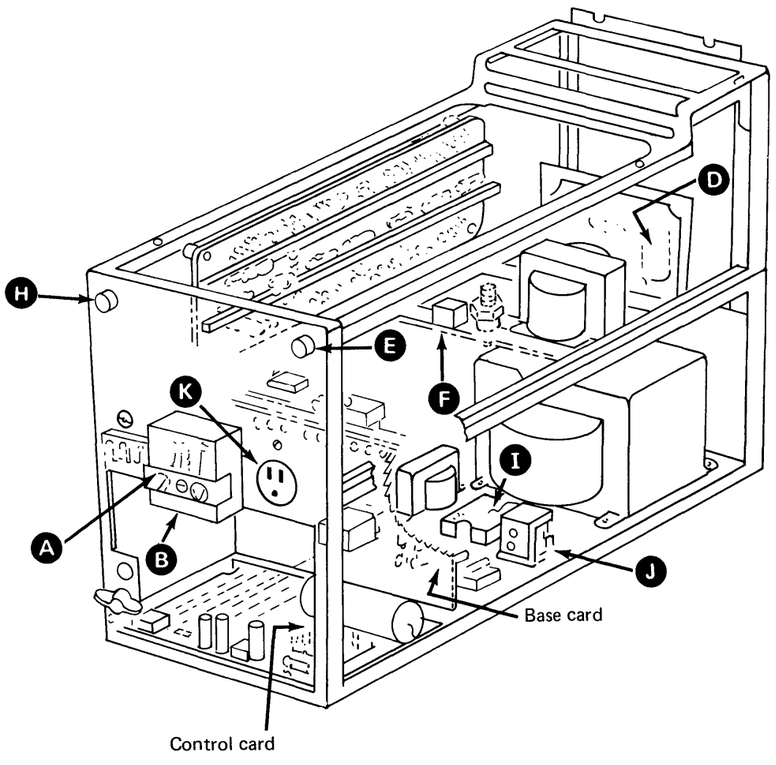


Notes:

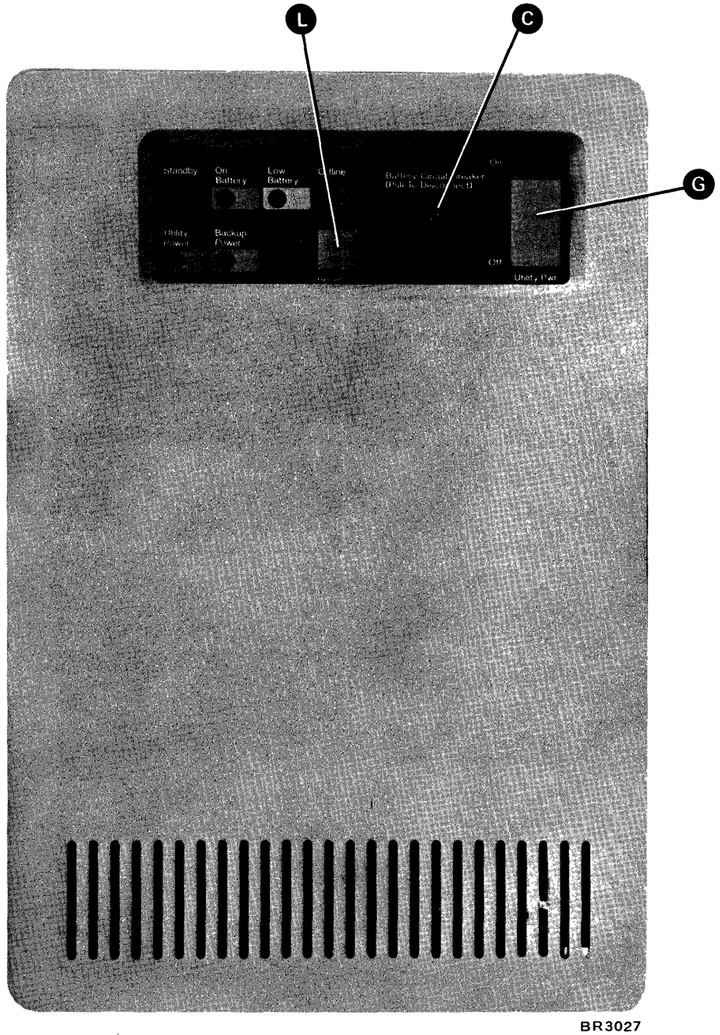
1. The 5 volts arms the control circuitry. Without the 5 volts from the processor power supply, the 4999 cannot switch to backup power. This is done to prevent initial start surges to the 4999.
2. The ac failure signal is sent to the processor when the line sensing circuit senses a line failure condition. The purpose of this signal is to maintain an ac warning condition because the processor power supply no longer recognizes that condition once the 4999 is supplying power.
3. The 4999 contains an Instant Power Off (IPO) interlock via a connector at the rear of the unit. Unless IPO is implemented, the BBU's inverter cannot operate. This is a safety feature to ensure that the 4999 does not attempt to continue powering the processor when a system IPO has been initiated (for the purpose of dropping system power). If the 4999 is housed in an IBM type 4997 rack enclosure, the cable supplied as a BBU ship-group item mates the 4999 directly to the 4997's IPO feature. In a non-IBM rack, the customer must provide a switch-contact set (single-pole, single-throw, rated at 1 ampere, 16 Vdc) that opens simultaneously with an IPO action.

Logic Block Diagram Locations

- Ⓐ Battery connection block
- Ⓑ Reverse polarity indicator
- Ⓒ Circuit breaker, 70-ampere
- Ⓓ Inverter
- Ⓔ Fuse, 7-ampere
- Ⓕ Fuse, 3-ampere
- Ⓖ Utility Pwr On/Off switch
- Ⓗ Fuse, 0.2-ampere
- Ⓘ Solid state relay
- Ⓙ Line transfer relay
- Ⓚ Processor power cord outlet
- Ⓛ Reset pushbutton



4999 rear view



BR3027

Line Voltage Sensing

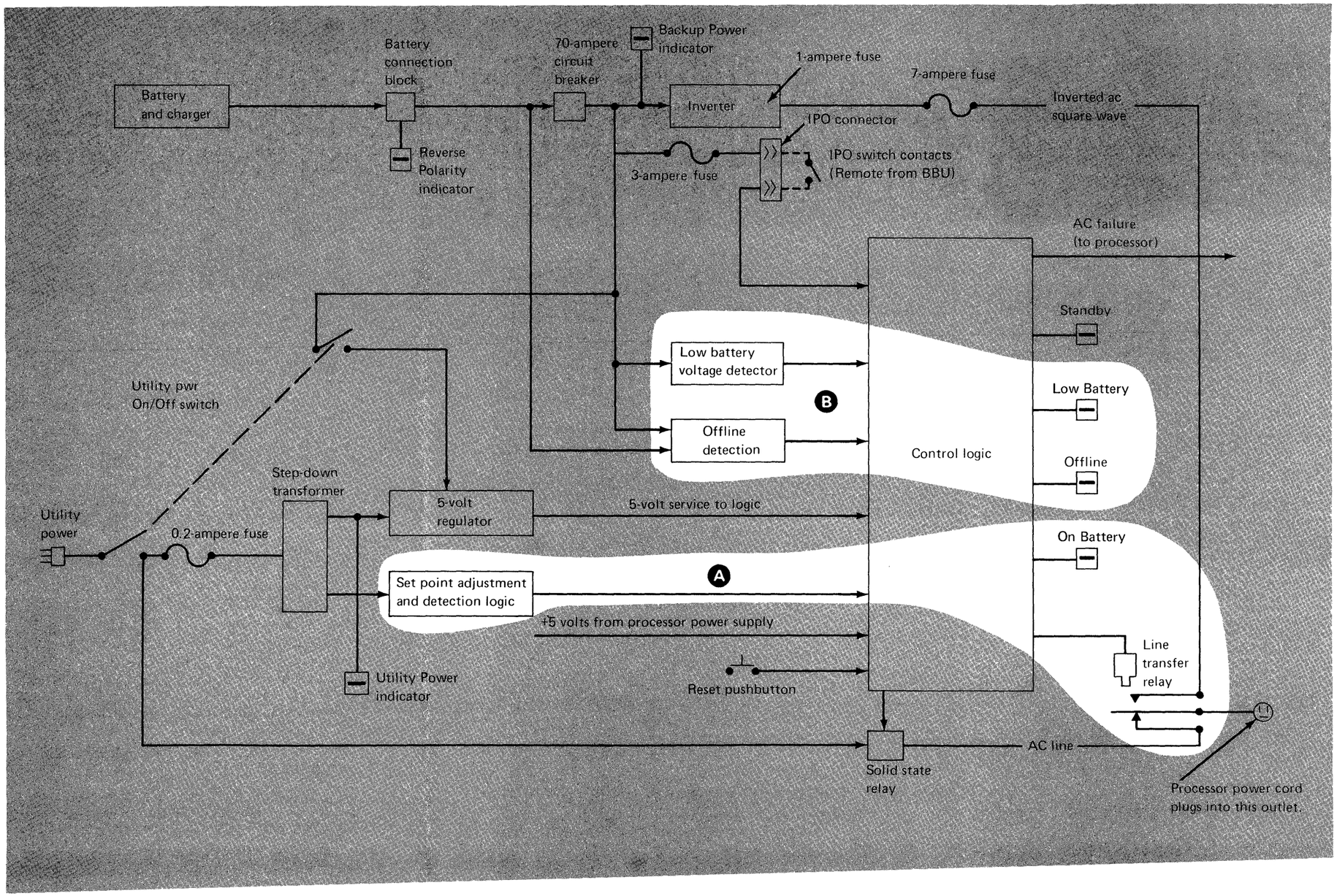
Ⓐ When the sensing circuit detects that the line voltage has fallen below the set point, normally 80 (160) volts, it picks the Line Transfer relay and starts the inverter. This transfers the input to the processor from the ac line to the ac square-wave output of the 4999 inverter. The On Battery indicator is turned on at this time, and remains on until the input is switched back to ac line input. The line transfer takes about 15 milliseconds to complete; however, the processor power supply has enough energy storage capacity to keep the dc voltages regulated until the line transfer is completed. The processor remains on inverted battery power for at least 0.5 second.

When the sensing circuit detects that the ac input power is back up to 87.5 (175) volts, it switches from inverted battery power to the ac line. This transfer takes about 15 milliseconds.

Battery Voltage Sensing

Ⓑ The battery voltage is monitored continuously. If the battery voltage falls below approximately 11.2 volts, the Low Battery indicator is turned on, but no other action is taken.

During the time the 4999 is supplying inverted ac voltage, and the battery voltage falls below approximately 10.8 volts, the inverter is turned off and the processor is switched back to the ac input line. This switching occurs whether the line voltage has returned or not. With the line voltage not present, the processor powers down immediately. This condition is called an *offline* shutdown, and is indicated by the Offline indicator on the 4999 console. After an offline shutdown, the 4999 is inoperative until the battery voltage recovers to approximately 12 volts, and the Reset button has been pressed. At this time the 4999 goes to standby mode, indicated by the Standby light on the 4999 console.



Chapter 5. Timer Feature

Description

The timer feature provides two 16-bit timers, each of which can be used as an interval timer, a pulse counter, or a pulse duration counter with end interrupt.

The two timers are contained on one four-wide, six-high printed-circuit card, and can be plugged into any I/O slot of a Series/1 processor or a 4959 I/O expansion unit. Each timer, which can be used with external signals, has two output lines ('run state' and 'external gate enabled') and two input lines ('customer clock' and 'external gate'). These external lines are transistor-transistor-logic (TTL) compatible, and connect to the timer feature card through a single top-card connector.

The two timers are separately addressable and are started, stopped, read, or set to any value, independently, under program control. A timer can be read without disturbing its operation; however, to set a timer's value or mode, it must be stopped.

Each timer has a mode register that is used to select one of four internal time bases (1, 5, 25, or 50 microseconds), or an external time base (which is provided by the user, and must be equal to or greater than 20 microseconds when the input is filtered, or 1 microsecond when the input is not filtered). This filtering capability can be selected by jumper options on the timer card. An *external gate enable bit* is also contained in the mode register. The time base and external gate enable modes are program selected, and the timer value is decremented with the selected time base.

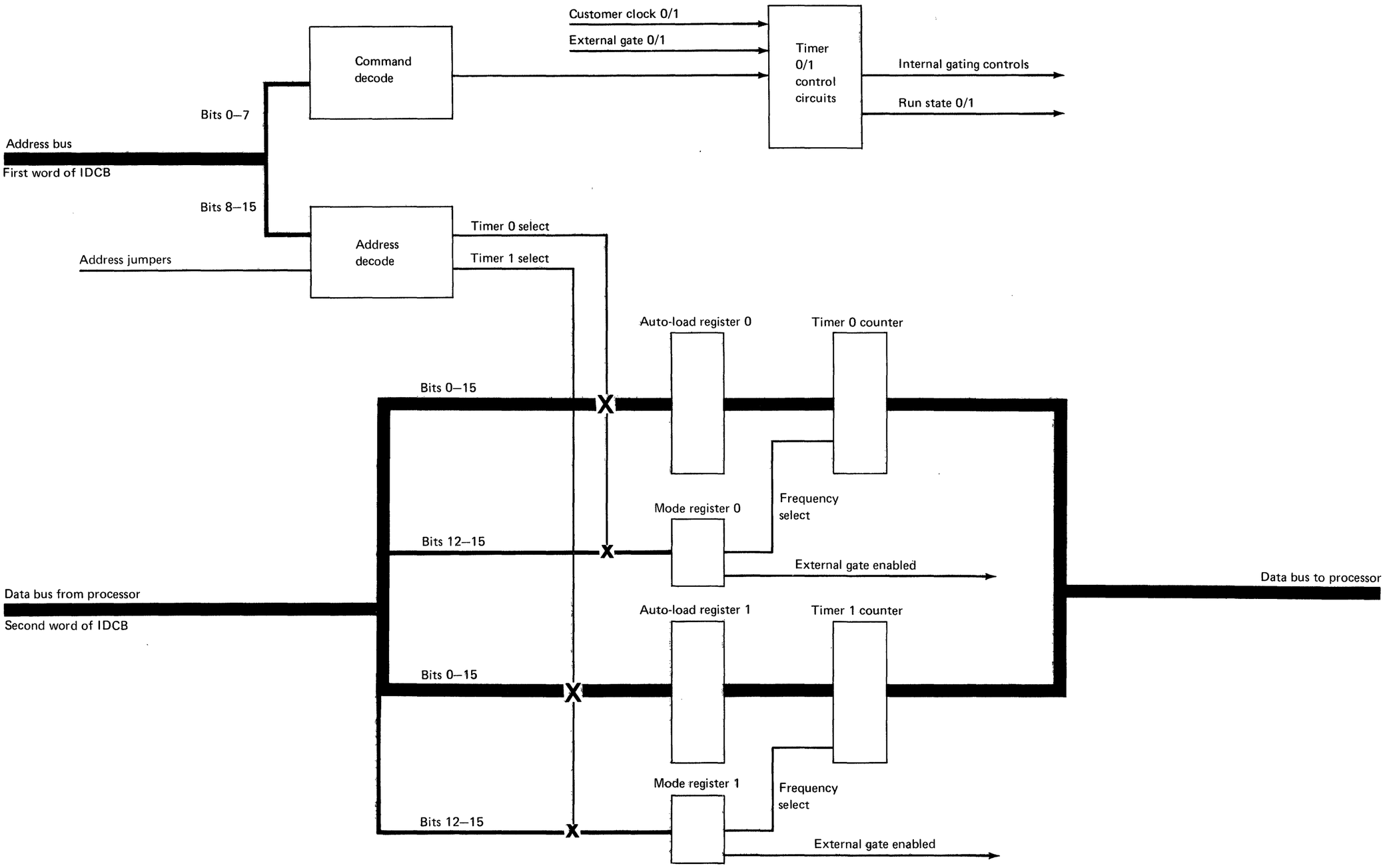
The following program-selected running modes are available for each timer:

Periodic Interrupts (Internal). A 16-bit auto-load register is set to any value by program control. This register automatically reloads the timer when the timer underflows (decrements from 0 to −1) and an interrupt is generated. The auto-load register provides the capability of generating periodic interrupts, without program intervention, on the 65,536 possible base values of the timer.

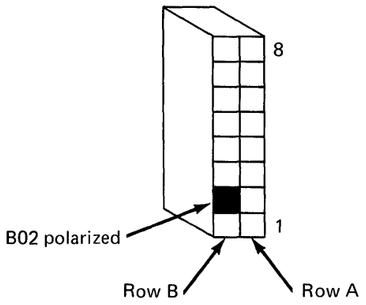
Aperiodic Interrupts (Internal). The timer is loaded with a value, under program control, and an interrupt occurs when the timer underflows. After the first interrupt, the timer is not reloaded from the auto-load register. The timer then counts the full 65,536 counts before the next interrupt occurs, unless a new value is loaded under program control.

Periodic or Aperiodic Interrupts (External). The timer generates periodic or aperiodic interrupts, but the starting and stopping of the timer is controlled by an external gate when the timer is in the run state.

Timer Card Data Flow

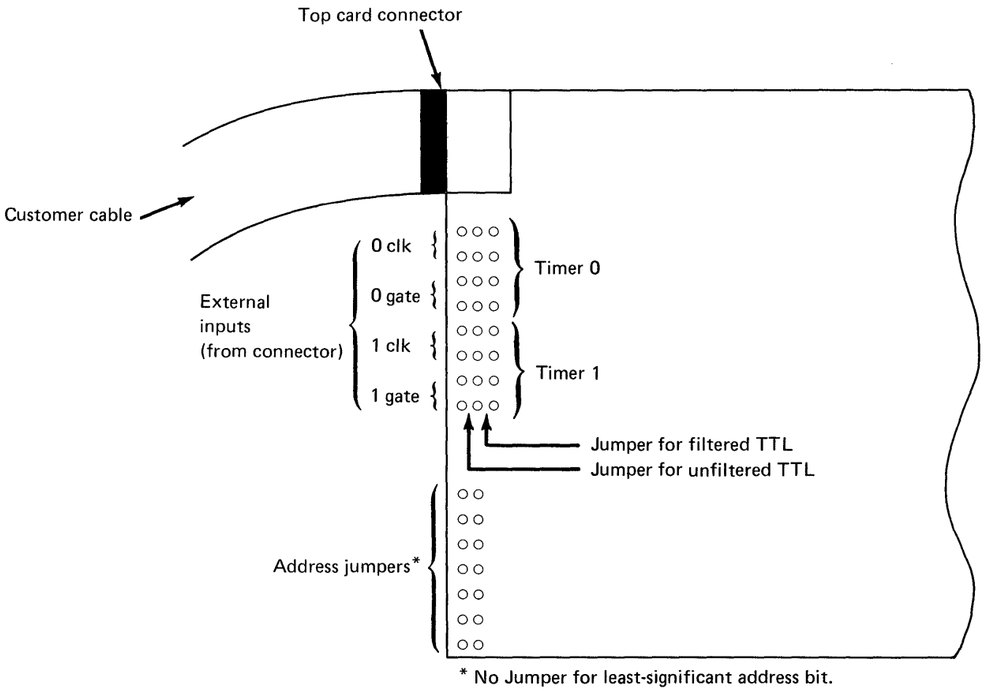


Timer Card Locations



Interface lines on customer cable

Cable pin	Timer 0	
A01	Customer clock	To timers
A02	External gate	To timers
A03	Run state	From timers
A04	External gate enabled	From timers
A05	Signal ground	
A08	Frame ground strap	To frame
	Timer 1	
B08	Customer clock	To timers
B07	External gate	To timers
B06	Run state	From timers
B05	External gate enabled	From timers
B04	Signal ground	



One device address for both timers (device address must be even).
Bit 15 of address bus selects one of the two timers.

Addressing

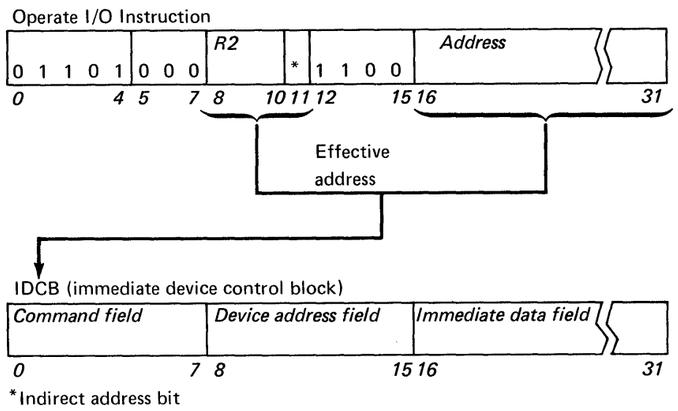
The timers appear as two separate addressable devices on the Series/1 I/O channel, but the addresses must be consecutive. One set of seven address jumper pins (corresponding to the IDCB address field bits 8–14) allow the user to specify any two consecutive addresses in the range of 0–254 (hexadecimal 00-FE). The jumpered address must be an even address, because there is no jumper pin for IDCB address bit 15. An IDCB address field with bit 15 set to 0 addresses one timer; with bit 15 set to 1, the other timer is addressed.

Refer to the appropriate MLD logic page for jumper pin locations and instructions.

Program Control

Operate I/O Instruction

Communication between the processor and the timers is established by the processor through program control. All timer functions are initiated through the execution of an Operate I/O instruction. The Operate I/O instruction addresses an IDCB in storage, which contains the command field, timer address, and the immediate data field.*



*Indirect address bit

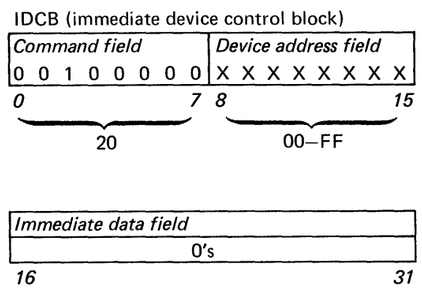
Commands

The timers respond to the following I/O commands from the Series/1 processor:

Command code (hex)	*Name*
20	Read ID
24	Read Timer Value
25	Read Timer Mode
60	Prepare
64	Set Timer Period and Initial Value
65	Set Timer Mode
66	Start Timer Periodic
67	Start Timer Aperiodic
6E	Stop Timer
6F	Device Reset
F0	Halt I/O

Note: I/O instruction condition codes are reported to the processor by the timer feature or processor channel relating to conditions that can be detected during execution of the I/O commands. In the following descriptions of the timer commands, the condition codes that can be reported during command execution are listed. If the condition that causes a condition code to be reported is unique to the command, it is explained in detail; otherwise, the condition code definitions in "I/O Instruction Condition Codes" in this chapter apply.

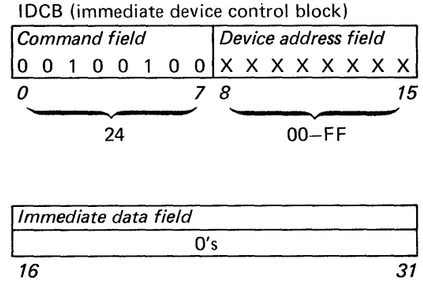
Read ID



The Read ID command causes the ID word from the addressed timer to be transferred to the data field of the IDCB. The timer ID word is 0028 (hex). No interrupt is reported by the timer to this command.

Condition code 0, 5, or 7 can be reported for this command. Condition code 1 (busy) is not reported. The command is not executed if condition code 0 or 5 is reported.

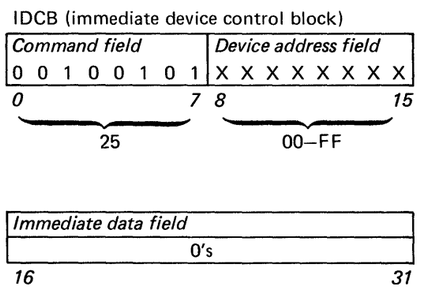
Read Timer Value



The Read Timer Value command causes the value of the addressed timer to be transferred to the data field of the IDCB. No interrupt is reported by the timer to this command.

Condition code 0, 5, or 7 can be reported for this command. Condition code 1 (busy) is not reported. The command is not executed if condition code 0 or 5 is reported.

Read Timer Mode



The Read Timer Mode command causes the value of the addressed timer's mode register to be transferred to the data field of the IDCB in the same format specified under the Set Timer Mode command. No interrupt is reported by the timer to this command.

Condition code 0, 5, or 7 can be reported for this command. Condition code 1 (busy) is not reported. The command is not executed if condition code 0 or 5 is reported.

Prepare

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 0 0 0 0	X X X X X X X X
0 *7*	*8* *15*
60	00–FF

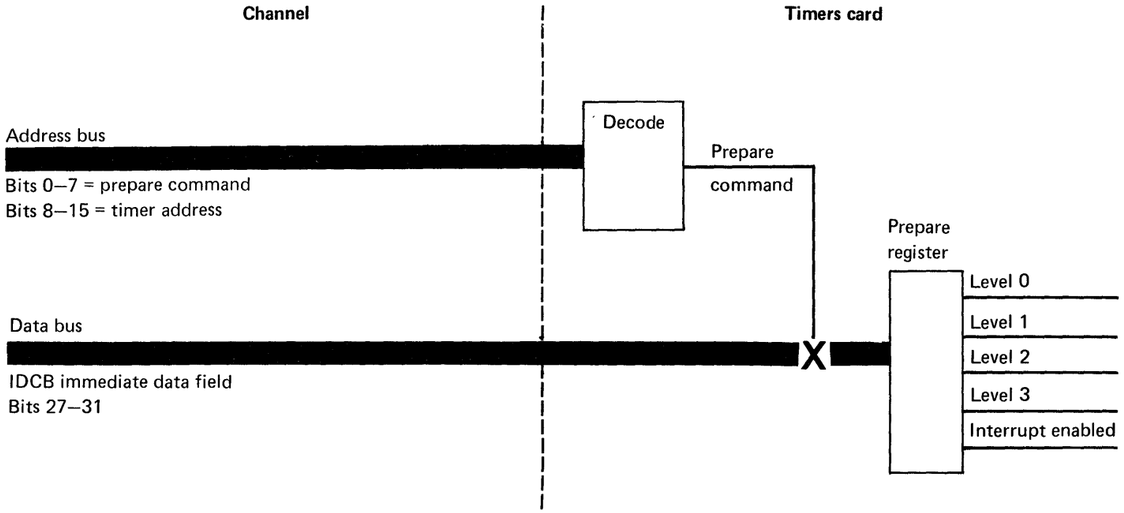
Immediate data field		
0's	Level	I
16 *26 27*	*30 31*	

Bits 27–30	Level	Bit 31
0000	0	0 = interrupts not allowed
0001	1	
0010	2	1 = interrupts allowed
0011	3	

The Prepare command loads the interrupt level and I-bit into the prepare register. Because both timers share one prepare register, they are prepared simultaneously (same level and I-bit by one Prepare command). The device address field in the IDCB can indicate either timer.

The I-bit (bit 31) determines if the timer can report an I/O interrupt. If the I-bit equals 0, I/O interrupts are not reported; if the I-bit equals 1, I/O interrupts are reported. The interrupt level (bits 27–30) is the priority level on which the timer reports I/O interrupts.

Condition code 0, 5, or 7 can be reported for this command. Condition code 1 (busy) is not reported. The command is not executed if condition code 0 or 5 is reported.



Set Timer Period and Initial Value

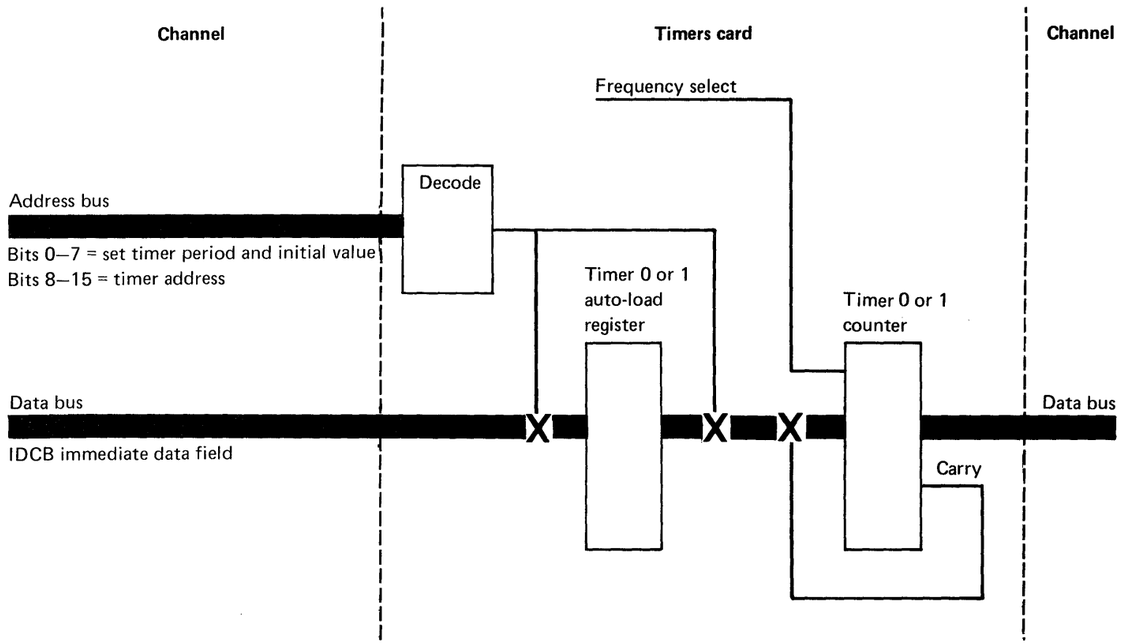
IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 0 1 0 0	X X X X X X X X
0 *7*	*8* *15*
64	00–FF

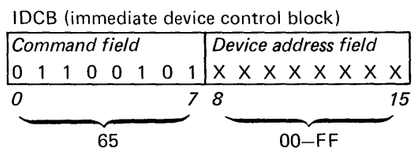
Immediate data field
X X X X X X X X X X X X X X X X
16 *31*
0000–FFFF

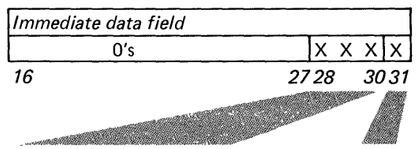
The Set Timer Period and Initial Value command loads the data field of the IDCB into the auto-load register of the addressed timer. This 16-bit value is selected by the user and can be any value from 0–65,535 (0000-FFFF hex). This value, in conjunction with the time base selected by the Set Timer Mode command, establishes the time interval for device-end interrupts. The data in the auto-load register is then loaded into the timer. No interrupt is reported by the timer to this command.

Condition code 0, 1, 5, or 7 can be reported for this command. The command is not executed if condition code 0, 1, or 5 is reported.



Set Timer Mode





Bits 28–30	Time base (microseconds)	Frequency (kHz)	Bit 31
000	50	20	0 = external gate not enabled
010	25	40	
100	5	200	1 = external gate enabled
110	1	1000	
001	user selected time base		

The Set Timer Mode command loads the data field of the IDCB into the mode register for the addressed timer. The desired time base can be selected by bits 28–30. For example, if bits 28–30 are set to 010, the timer counts once every 25 microseconds or a frequency of 40,000 Hertz. If bits 28–30 are set to 001, the user-selected time base is specified, and the timer counts once for every user-provided clock pulse; however, user-provided clocking is subject to the following restrictions:

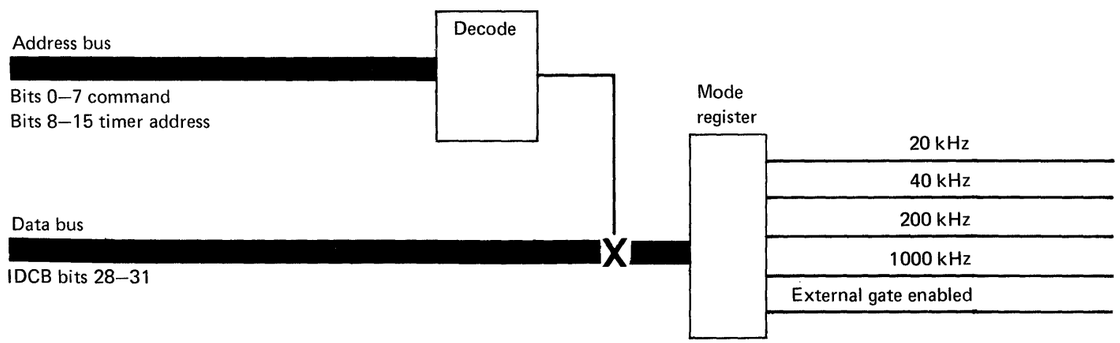
1. If the customer clock is jumpered for unfiltered TTL input, any external time base greater than 1 microsecond can be supplied to the timer.
2. If the customer clock is jumpered for filtered TTL input, the maximum input rate is 50 kHz.

Refer to "Description" in this chapter for additional information concerning external clocking.

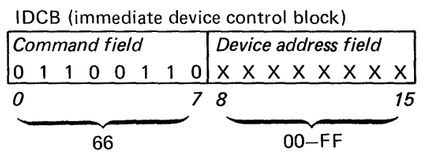
The time base selected, in conjunction with the value used in the Set Timer Period and Initial Value command, establishes the time interval for device-end interrupts.

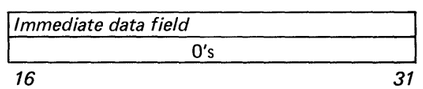
Bit 31 allows the user to provide an external gate to the timer. When this gate is enabled and activated by the user, the timer counts with the selected time base when the timer is in the run state. When the external gate is deactivated, the timer stops. No interrupt is reported by the timer to this command.

Condition code 0, 1, 5, or 7 can be reported for this command. The command is not executed if condition code 0, 1, or 5 is reported.



Start Timer Periodic





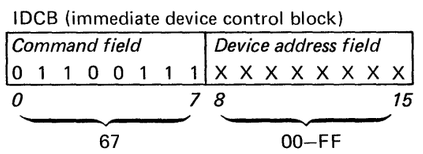
The timer's response to the Start Timer Periodic command depends upon the state of the external-gate-control lines, as described here:

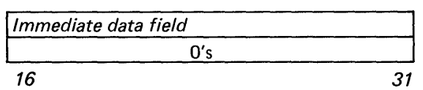
External Gate Not Enabled. The addressed timer is set to run state and is started. When the timer decrements from 0 to −1 (timer receives a decrement pulse after it has reached 0), a device-end interrupt is reported and the value of the auto-load register is set into the timer.

External Gate Enabled. The addressed timer is set to run state, but is not started. The timer starts when the external gate becomes active. When the timer decrements from 0 to −1, a device-end interrupt is reported and the value of the auto-load register is set into the timer. When the external gate becomes inactive, the timer stops, the run state is reset, and one of the following interrupts is reported: attention, attention and exception, or attention and device-end. Refer to "I/O Interrupt Condition Codes" in this chapter.

Condition code 0, 1, 5, or 7 can be reported for this command. The command is not executed if condition code 0, 1, or 5 is reported.

Start Timer Aperiodic





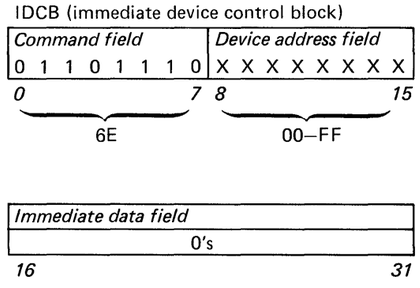
The timer's response to the Start Timer Aperiodic command depends upon the state of the external-gate-control lines, as described here:

External Gate Not Enabled. The addressed timer is set to run state and is started. When the timer decrements from 0 to −1, a device-end interrupt is reported. The value in the auto-load register is not set into the timer when the device-end interrupt is reported. The time period for the first device-end interrupt depends on the initial value set in the timer and the time base selected. The time period for subsequent device-end interrupts depends on the timer maximum value and the time base previously selected.

External Gate Enabled. The addressed timer is set to run state, but is not started. The timer starts when the external gate becomes active. When the timer decrements from 0 to −1, a device-end interrupt is reported. (Subsequent device-end interrupts are reported as described under "External Gate Not Enabled.") When the external gate becomes inactive, the timer stops, the run state is reset, and one of the following interrupts is reported: attention, attention and exception, or attention and device-end. Refer to "I/O Interrupt Condition Codes" in this chapter.

Condition code 0, 1, 5, or 7 can be reported for this command. The command is not executed if condition code 0, 1, or 5 is reported.

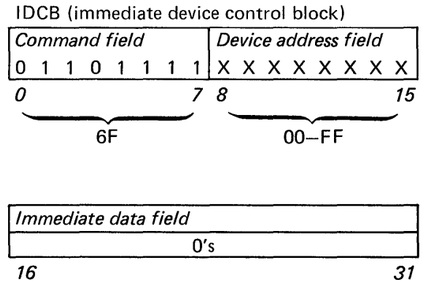
Stop Timer



The Stop Timer command stops the addressed timer and resets the timer run state. Residual interrupts are reset. A residual interrupt is an interrupt detected during execution of the command, and caused by (1) a clocking of the timer or (2) the external gate becoming inactive just after the timer has made a decision to accept and execute the command.

Condition code 0, 1, 5, or 7 can be reported for this command. Condition code 1 is reported if the timer has an interrupt pending. The command is not executed if condition code 0, 1, or 5 is reported.

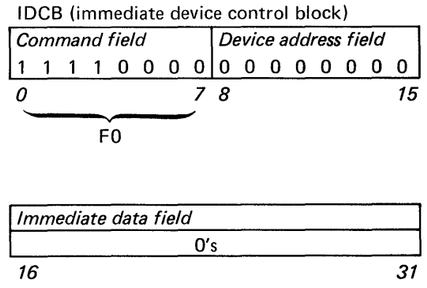
Device Reset



The Device Reset command stops the addressed timer and resets the timer run state. The mode register and any pending or residual interrupts for the addressed timer are reset. The timer and auto-load register are not reset.

Condition code 0 or 7 can be reported to this command. The command is not executed if condition code 0 is reported.

Halt I/O



Halt I/O is a channel-directed command that causes a halt of all I/O activity on the I/O channel of the processor. The timer feature responds to this command by resetting the mode register, all pending interrupts, and the timer run state. The device address field is not used for this command, and must be set to 0.

I/O Instruction Condition Codes

I/O instruction condition codes are reported to the Series/1 processor in response to an Operate I/O instruction directed to the timer feature. These codes are related to conditions that can be detected during execution of the instruction command. The following chart shows the I/O commands and the condition codes that can be reported:

	Condition code values							
Command	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*
20 Read ID	X					X		X
24 Read Timer Value	X					X		X
25 Read Timer Mode	X					X		X
60 Prepare	X					X		X
64 Set Timer Period and Initial Value	X	X				X		X
65 Set Timer Mode	X	X				X		X
66 Start Timer Periodic	X	X				X		X
67 Start Timer Aperiodic	X	X				X		X
6E Stop Timer	X	X				X		X
6F Device Reset	X							X
F0 Halt I/O								X

Note: Condition code 3 is reported if a command other than those listed is directed to the attachment.

The condition codes have the following meanings:

Condition code	*Meaning*
0	*Device not attached.* Reported if the timer feature is addressed, but is not installed on the system.
1	*Busy.* Reported when the timer is unable to execute a command because it is in the busy state. A timer is busy when the timer is in the run state or in an interrupt pending state.
2	*Not reported.*
3	*Command reject.* Reported if the command issued is outside the defined command set for the timer feature.
4	*Not reported.*
5	*Interface data check.* Reported if a parity error occurs on the data bus during data transfer.
6	*Not reported.*
7	*Satisfactory.* Reported when a command is accepted.

I/O Interrupt

If the I-bit in the prepare register has been set to 1 by a Prepare command, a timer can report five different interrupt states to the Series/1 processor:

1. Exception interrupt
2. Device-end interrupt
3. Attention interrupt
4. Attention and exception interrupt
5. Attention and device-end interrupt

Exception Interrupt

An exception interrupt is reported when an overrun has occurred in the timer. Overrun means that a device-end interrupt occurs while a previous device-end interrupt is still pending from the timer.

Device-End Interrupt

A device-end interrupt is reported when the timer is in run state and decrements from 0 to −1.

Attention Interrupt

An attention interrupt is reported when an external gate cycle ends prior to a device-end interrupt.

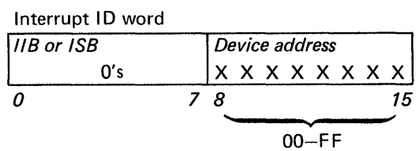
Attention and Exception Interrupt

An attention and exception interrupt is reported if an external gate cycle ends and an overrun condition is present in the timer.

Attention and Device-End Interrupt

An attention and device-end interrupt is reported if an external gate cycle end and a device-end interrupt are detected at the same time.

Interrupt ID Word



The interrupt ID word identifies the interrupting device (in this case, timer 0 or 1). The interrupt information byte (IIB) is not used for the timers and is always presented as 0. The condition code presented with the interrupt defines the interrupt. Refer to "I/O Interrupt Condition Codes" in this chapter.

Timer Interrupt Example. The timer feature initiates an I/O interrupt if the I-bit (bit 31 of the IDCB) in the prepare register was set to 1 by the Prepare command.

When the timer is decremented from 0 to −1, a device-end interrupt is reported. The time base selected and the initial value set in the timer establish the time intervals for device-end interrupts. The relationship of these values is:

B(V+1) = T

where

B = time base selected by the Set Timer Mode command.

V = value set into the timer by the Set Timer Period and Initial Value command.

T = time interval of device-end interrupts.

The constant 1 is added to the value V because device-end interrupts are not reported until the timer has been pulsed once more after the count has reached 0. For example:

The user wants device-end interrupts reported every 100 microseconds and elects a time base of 5 microseconds. Using the formula B(V+1) = T, the value to be set into the timer by a Set Timer Period and Initial Value command is 13 (hex).

$$V = \frac{T}{B} - 1$$

$$V = \frac{100}{5} - 1$$

$$V = 20 - 1$$

V = 19 (decimal) : 13 (hex)

The time interval of the first device-end interrupt reported after the timer accepts a start command, or after the external gate becomes active, may vary by as much as the value of the time base selected. This variance is due to the asynchronous condition between the internal free-running oscillator or external-user clock, and the program setting of the timer run state or the activation of the external gate. This time variance occurs only when the timer is started.

I/O Interrupt Condition Codes

The condition code reported when the timer interrupt is accepted by the processor identifies the interrupt as follows:

Condition code	*Meaning*
0	*Not reported.*
1	*Not reported.*
2	*Exception.* Reported when an overrun has occurred in the timer. Overrun means that a device-end interrupt occurs while a previous device-end interrupt is pending in the timer.
3	*Device-end.* Reported when the timer is pulsed once more after the count has reached 0.
4	*Attention.* Reported when an external gate cycle ends prior to a device-end interrupt. Timer run state is reset.
5	*Not reported.*
6	*Attention and Exception.* Reported if an external gate cycle ends and an overrun condition is present in the timer. Timer run state is reset.
7	*Attention and device-end.* Reported if an external gate cycle ends and a device-end interrupt is detected at the same time. Timer run state is reset.

Status After Resets

The following table lists the resets caused by the various resetting conditions:

Condition	Reset					
	Timer	Auto-load reg	Pre-pare reg	Mode reg	Pending inter-rupts	Timer run state
Power on reset	X (to all 1's)	X (to all 1's)	X	X	X	X
System reset			X	X	X	X
Halt I/O				X	X	X
Device reset				Y	Y	Y

X = reset in both timers
Y = reset in addressed timer only

Chapter 6. Teletypewriter Adapter Feature

Description

The Teletypewriter Adapter feature provides the circuitry necessary to attach a Teletype* Model ASR33/ASR35, or equivalent to the channel of a Series/1 processor. Any serial-by-bit device that meets the requirements of the adapter/device interface, and has one of the following bit-transfer rates, can also be attached:

Bits per second	
50	
75	
100	
110	
150	
200	The interrupt mask time of the program support system used may preclude operation at these bit rates
300	
600	
1200	
2400	
4800	
9600	

Any one of these bit rates can be selected by jumper options on the adapter feature card.

Some of the commercially available devices that can be attached to the adapter include:

- Printer-keyboards
- Keyboard-display units
- Keyboard-display-printer units
- Printers
- Tape cassettes
- Tape units
- Card readers
- Badge readers
- Plotters

The teletypewriter adapter has a four-wire interface for data exchange between the adapter and the device (two for receive and two for transmit), and uses full-duplex operation (that is, data may be concurrently transmitted and received).

The data exchange across the adapter/device interface is not checked for parity or for any device-dependent control characters. The teletypewriter adapter is code transparent, and all 256 binary combinations of a data byte can be transmitted and received; the adapter can also be configured for initial program load (IPL) operation.

Data transfer between the adapter and the Series/1 processor is by byte, using direct program control (DPC) commands, except during IPL (when the transfer is by byte, using cycle-steal).

The teletypewriter adapter is packaged on a 4-wide, 6-high, printed-circuit card that may be plugged into any I/O slot in a Series/1 processor or a 4959 I/O expansion unit. Certain adapter options require that ±12 Vdc be available at the adapter card slot. These options are described in "Adapter Options" in this chapter. The ±12 Vdc is not a standard feature on all Series/1 processor types or models, or on the 4959 I/O expansion unit; however, the ±12 Volt Communications Power feature is available, if required.

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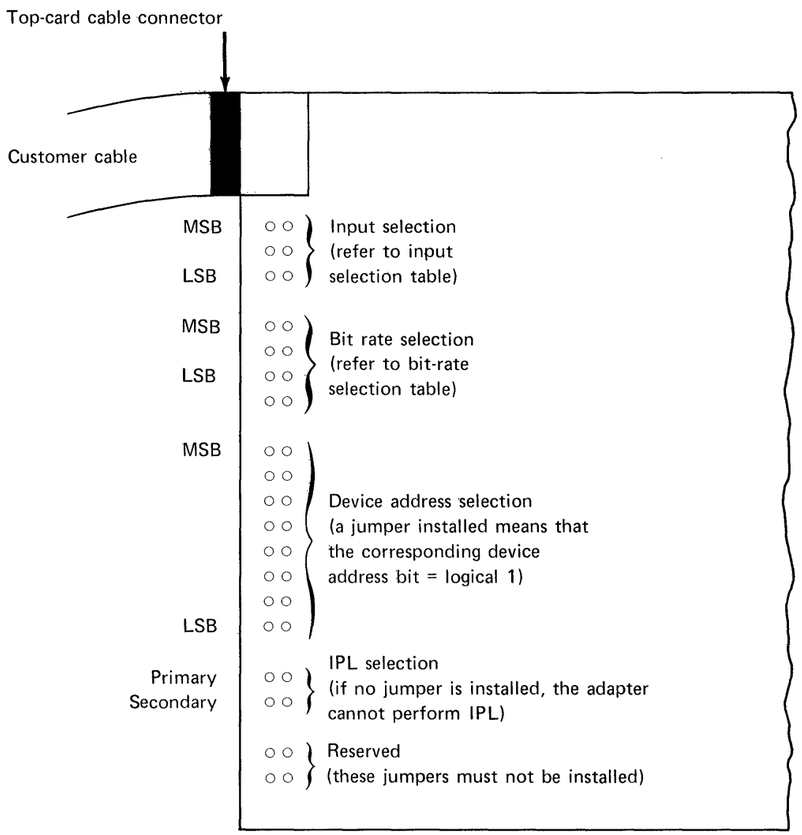
* Trademark of the Teletype Corporation

Teletypewriter Adapter Feature Card



A jumper installed equals a bit value of 1;
a jumper removed equals a bit value of 0.

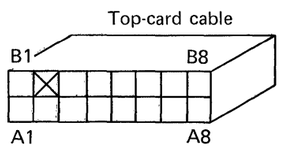
MSB = Most-significant bit
LSB = Least-significant bit

Input selection table

MSB	LSB	Input selected	Input interpreted as
0 0	0	Contact sense	Closed = data mark
0 0	1	TTL	Minus = data mark
0 1	0	EIA	Minus = data mark
0 1	1	Internal wrap	True data out
1 0	0	Contact sense	Open = data mark
1 0	1	TTL	Plus = data mark
1 1	0	EIA	Plus = data mark
1 1	1	Internal wrap	True data out

Bit rate selection table

MSB	LSB	Rate (bits per second)
0 1 0 0		50
1 0 0 0		75
0 1 0 1		100
0 0 0 0		110
1 0 0 1		150
0 1 1 0		200
1 0 1 0		300
1 0 1 1		600
1 1 0 0		1200
1 1 0 1		2400
1 1 1 0		4800
1 1 1 1		9600



Top-card connector pin assignment

A1 Isolated receive input +
A2 Current driver, current = mark
A3 Isolated receive input –, or isolated receive input +
A4 EIA received data in
A5 Frame ground
A6 EIA data terminal ready
A& Solid state switch closed = data mark or minus (–) TTL data out
A8 Solid state switch/TTL write control

B1 Non-isolated receive input –
B2 Polarization
B3 Current driver, current = space
B4 TTL received data in
B5 Signal ground
B6 EIA transmitted data
B7 Solid state switch = data mark, or plus (+) TTL data out
B8 Solid state switch, TTL load control

Adapter Options

The adapter/device interface offers signal and bit-rate selection options to accommodate a wide range of attached devices. The options are selected by using the appropriate pins in the 16-pin top-card connector on the feature card, and/or jumpering of the selection pins on the feature card.

Adapter/Device Interface Input and Output Options

Interface Input Options. The input options are:

- Isolated contact sense*
  Open circuit=mark (logical 1)
  Closed circuit=mark
- Non-isolated contact sense**
  Open circuit=mark
  Closed circuit=mark
- TTL (transistor-transistor logic)
  Plus level=mark
  Minus level=mark
- EIA (Electronics Industry Association)**
  Minus level=mark (standard convention)
  Plus level=mark

* This option requires that the customer supply external power sources to drive the transmit and receive current loops.

** These options require the ±12 Volt Communications Power feature.

These input options are selected by utilizing the appropriate connector pins of the top-card connector on the feature card, and by jumper options on the feature card.

Interface Output Options.

- Current driver*
  Current=mark (logical 1)
  No current=mark
- Solid state switch/TTL
  Closed/minus=mark
  Open/plus=mark
- EIA transmitted data*
  Minus=mark (standard convention)
- EIA data terminal ready*
  Active (on) when ±12-volt feature is installed.
- Solid state switch/TTL write control
- Solid state switch/TTL read control

*These options require the ±12 Volt Communications Power feature.

The write- and read-control outputs are available for control of the user's attached device, and are switched by modifier bit 7 of the Write and Read commands. These outputs are not used for the attachment of any standard teletypewriter I/O device.

The output options are selected by utilizing the appropriate pins of the top-card connector on the feature card.

Bit-Rate Option

Any one of the 12 bit-transfer rates can be selected by installing the appropriate jumpers on the feature card.

Device-Address Option

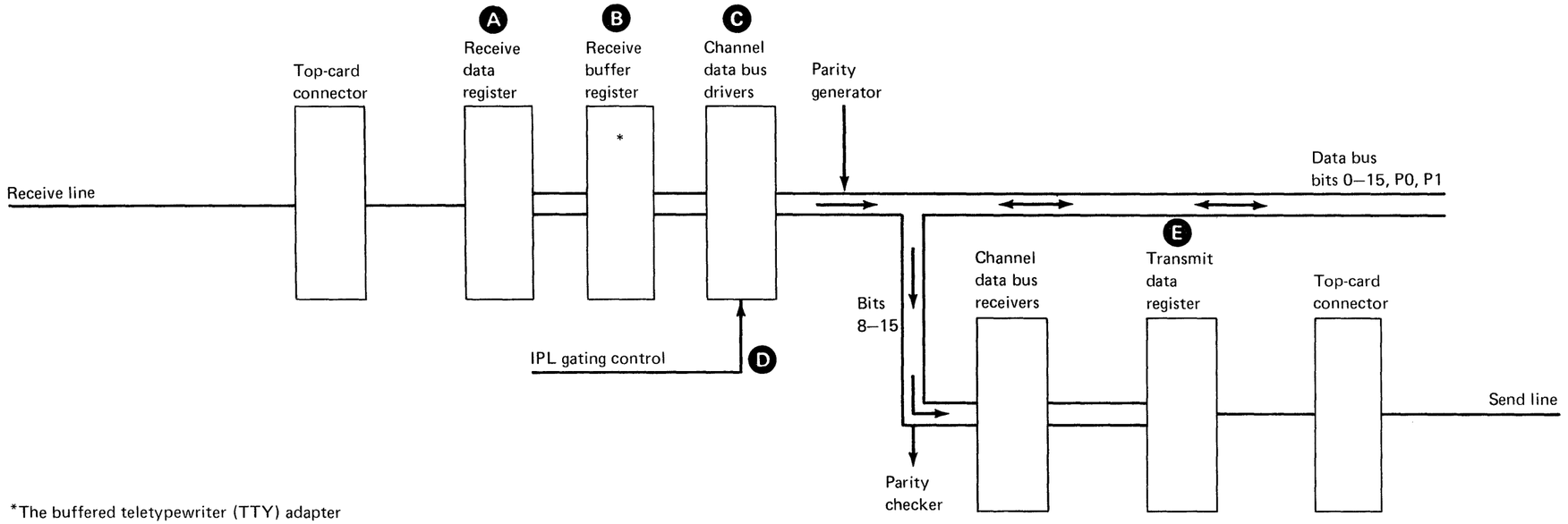
The device address used by the Series/1 processor to communicate with the teletypewriter adapter is selected by jumpers that are located on the adapter feature card. Any one of 256 device addresses (00-FF hex) can be selected by installing the appropriate jumpers.

IPL Option

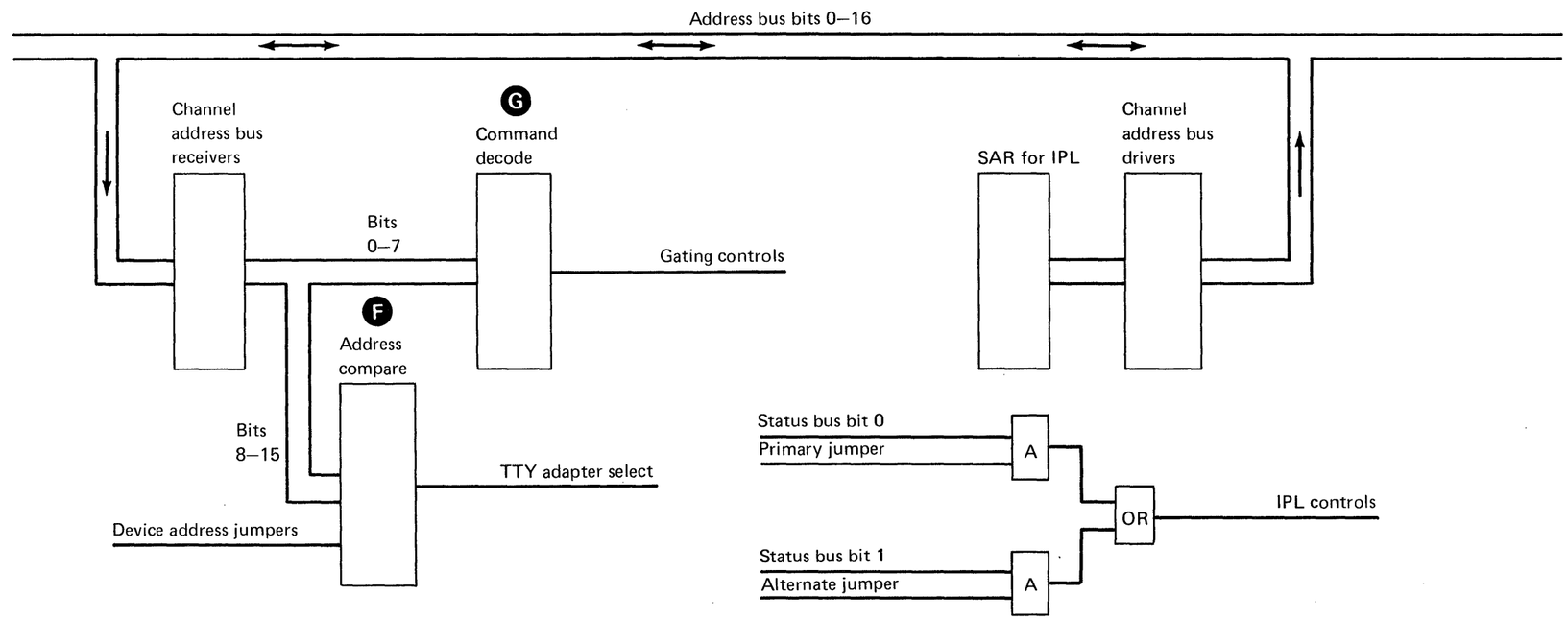
The teletypewriter adapter can be selected to perform initial program load (IPL), as either the primary or alternate IPL source, when the appropriate jumper is installed on the feature card. If a jumper is not installed on either of the IPL source jumper pins, the adapter cannot be selected for IPL.

Teletypewriter Adapter Data Flow

- (A) During a normal receive operation, data is received serially from the 'receive' line and is deserialized in the receive data register.
- (B) When a byte of data is accumulated in the receive data register, the byte is transferred to the receive buffer register, and an attention interrupt is generated in the adapter and presented to the processor.
- (C) When the processor accepts the interrupt and issues a Read command to the adapter, the contents of the receive buffer register are gated to bits 8–15 of the processor 'data bus-in' lines. Parity is generated as the data is sent to the processor.
- (D) During IPL operations, the data is gated to the processor in cycle-steal mode. After a byte of receive data is accumulated in the receive data register and moved to the receive buffer register, it is sent to the processor 'data bus-in' lines. The IPL storage address register (SAR) selects the data-bus byte (0–7 or 8–15) to which the receive data byte is gated. When SAR is even, the contents of the receive buffer register are gated to bits 0–7 of the 'data bus-in' lines. When SAR is odd, the data is gated to bits 8–15 of the 'data bus-in' lines. Parity is generated for each byte sent to the processor data bus.
- (E) For a transmit operation, the processor issues a Write command, which causes bits 8–15 of the processor 'data bus-out' lines to be loaded into the transmit data register. There, the data is serialized by shifting one bit at a time to the 'send' line (bit 15 is the first bit sent to the 'send' line).
- (F) The adapter's address compare logic samples each device address on the processor 'address bus-out' lines. The device address is compared with the device address jumpers on the adapter card, and, when an equal address compare occurs, the adapter is selected.
- (G) An equal address compare causes the adapter's command decode logic to decode bits 0–7 of the processor 'address bus-out' lines to determine the type of command. The command decode logic controls various gating lines that cause the adapter to execute the functions of the command.

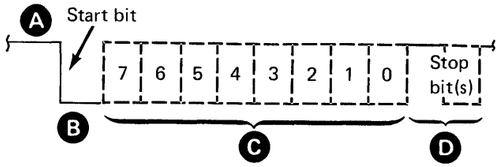


*The buffered teletypewriter (TTY) adapter applies to processors with EC 755088 installed.



Data Transmit and Receive Operations

Data bytes are transmitted and received across the adapter/device interface serially-by-bit with the least-significant bit being transmitted or received first. A start/stop frame of 10 or 11 bits is used for the data transfer. Each frame contains a start-bit, eight data-bits, and one or two stop-bits. Characters being transmitted by the teletypewriter adapter (to a device) are always followed by two stop-bits; however, characters being received by the adapter (from a device) can have either one or two stop-bits.



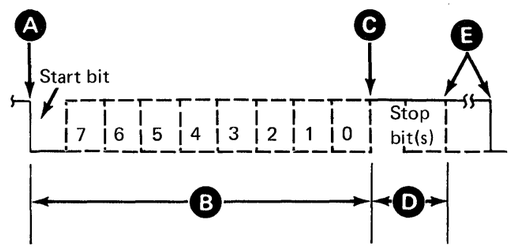
A The line is always held in a 'mark' condition when no data is being transmitted.

B The start bit is always a 'space' (logical 0).

C Eight data bits are transmitted for each character. Each bit is either a mark or a space, depending on the character code. Note that the least-significant bit is transmitted first.

D The stop bit is always a mark (logical 1). On transmit, two stop bits are always used. On receive, one or two stop bits can be used.

Transmit Operation



A The successful execution of a Write command by the adapter causes the transfer of a byte of data from the Series/1 main storage to the transmit data register in the adapter. The internal clocking necessary to serially transmit the data byte is initiated by the adapter. A start-bit is transmitted before the data-bits.

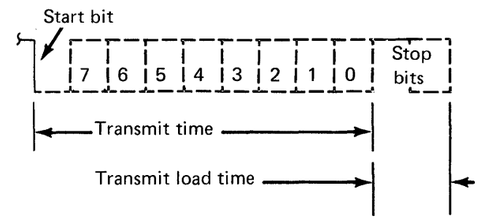
B *Transmit time*, which is measured from the beginning of the transmit operation to the posting of the device-end interrupt, is nine bit-times at the selected bit rate. Refer to the "Transmit Operation Timing Diagram," which follows, for character transmit timings at the various selectable bit rates.

C The adapter transmits two stop-bits. At the beginning of the first stop-bit, the adapter sends a device-end interrupt request to the processor to signal the completion of one character transmission. This interrupt must be serviced by the Series/1 program and another transmit operation must be initiated before the end of the second stop-bit if the maximum data transmission rate is to be sustained.

D *Transmit load time* is measured from the posting of the device-end interrupt, and is two bit-times (stop-bits) at the selected bit rate. If a new Write command is executed within this time, the character transmission rate is determined by the adapter clocking (that is, the next transmit operation cannot begin until the end of the two stop-bit times). The adapter, however, becomes "write-busy" upon successful acceptance of the Write command. If a new Write command is delayed beyond the two stop-bit times, the transmit operation is initiated immediately upon successful acceptance of the command; however, maximum data rate performance is not sustained. Refer to the "Transmit Operation Timing Diagram," which follows, for transmit load timings at the various selectable bit rates.

E The next transmit operation can begin (1) immediately after the end of transmit load time if another Write command has been accepted or (2) upon receipt of a Write command subsequent to transmit load time.

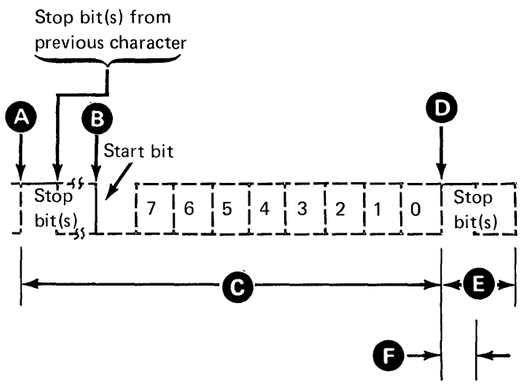
Transmit Operation Timing Diagram



Bit rate	Transmit time* (milliseconds)	Transmit load time* (milliseconds)
9600	0.936	0.208
4800	1.87	0.416
2400	3.74	0.832
1200	7.49	1.66
600	14.98	3.33
300	29.96	6.66
200	44.94	10.0
150	59.9	13.3
110	81.9	18.2
100	89.88	20.0
75	119.08	26.6
50	179.76	40.0

*Times are ±0.1%

Receive Operation



A The leading edge of the stop-bit from the received character causes the adapter to transfer the character from the receive data register to the receive buffer register, and to post an attention interrupt to the Series/1 processor.

B A subsequent start-bit signals the adapter that another character is being received from the attached device. This character is serially clocked, by the adapter, into the receive data register.

C This is the maximum interval allowed the Series/1 program to read the previously received character that is now in the receive buffer register. If the leading edge of the stop-bit from this character is sensed by the adapter, and the character in the receive buffer register has not been read at least once by the Series/1 program, a receive overrun operation occurs. In this case, the adapter posts an exception interrupt to the processor. The character in the receive buffer register is not lost; the character in the receive data register that caused the overrun is lost.

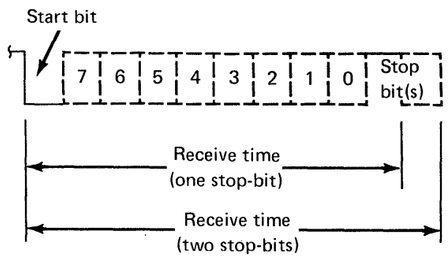
The duration of this interval can be calculated from the values in the "Receive Operation Timing Diagram." The Series/1 programmer must assume that the received data is being transmitted by the attached device at the maximum rate for the selected bit rate.

D The leading edge of the stop-bit causes the adapter to check that any previously received character in the receive buffer register has been read at least once by the Series/1 program. If the character in the receive buffer register has been read by the program, the adapter transfers the contents of the receive data register to the receive buffer register and posts an attention interrupt to the processor to indicate completion of a normal receive operation. If the character in the receive buffer register has not yet been read by the program, the adapter posts an exception interrupt to the processor to indicate that an overrun receive operation has occurred.

E If the attached device transmits two stop-bits at the end of the character, the time is two bit-times at the selected bit rate (assuming that the data is transmitted at the maximum rate for the selected bit rate).

F If the attached device transmits a single stop-bit at the end of the character, the time is one bit-time at the selected bit rate (assuming that the data is transmitted at the maximum rate for the selected bit rate).

Receive Operation Timing Diagram



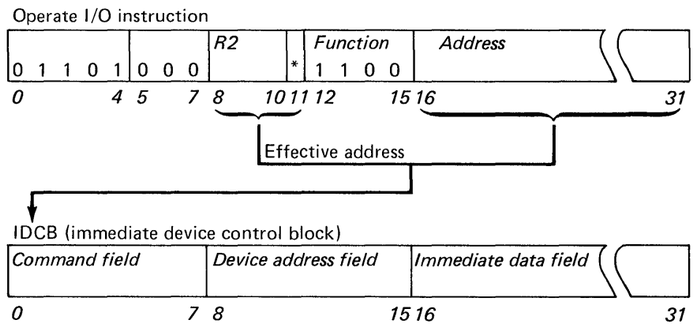
Bit rate	Receive time* with one stop-bit (milliseconds)	Receive time* with two stop-bits (milliseconds)
9600	1.01	1.12
4800	2.05	2.26
2400	4.14	4.55
1200	8.30	9.14
600	16.6	18.3
300	33.3	36.6
200	49.9	54.9
150	66.6	73.3
110	90.8	99.9
100	99.9	109.9
75	133.3	146.6
50	199.9	219.9

* Times are ±0.1%

Program Control

Operate I/O Instruction

All teletypewriter adapter functions are initiated by execution of Operate I/O instructions by the Series/1 processor.



*Indirect address bit

The Operate I/O Instruction generates an effective address that points to an immediate device control block (IDCB) in the processor main storage. The IDCB contains the command field, the adapter address, and an immediate data field.

Addressing

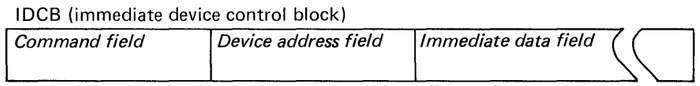
The teletypewriter adapter is addressed by the eight-bit address field of the IDCB. Field installable jumpers on the adapter card allow for selecting any one of 256 device addresses in the range of 00-FF (hex). Refer to "Device-Address Option" under "Adapter Options" in this chapter for address jumper information.

Commands

Before describing the command set for the teletypewriter adapter, it is necessary to define the two types of receive operations that can occur in the adapter. These receive operations are:

- Normal receive operation. A byte of data is transmitted from the attached device into the adapter's receive data register. The byte of data is then transferred to the receive buffer register and an attention interrupt is reported to the Series/1. The data byte remains in the receive buffer register until (1) it is read at least once by the program and (2) a subsequent normal receive operation is initiated.
- Overrun receive operation. An overrun receive operation occurs when the next data byte has been completely received by the adapter's receive data register and the data byte in the receive buffer register has not been read at least once by the program. The data in the receive buffer register is not lost; the data in the receive data register that caused the overrun is lost. Upon completion of an overrun receive operation, an exception interrupt is reported to the Series/1.

The command field (bits 0–7) of the IDCB define the various control, write, and read functions used by the adapter, as follows:



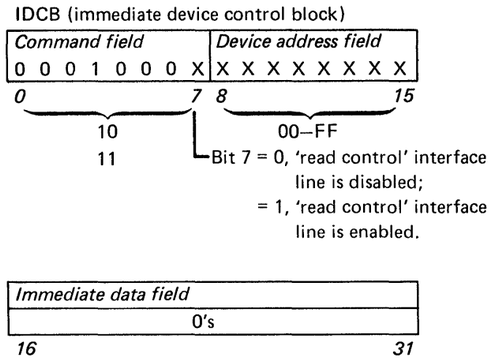
Chan	R/W	Function	Modifier	Hex	Specific command
0	1	10 Control	0000	60	Prepare
0	1	10 Control	1111	6F	Reset Device
0	1	10 Control	1110	6E	Reset to Diagnostic Wrap
0	1	01 Write	000X	50,51	Write
0	0	01 Read	000X	10,11	Read
0	0	10 Read status	0000	20	Read ID

Write bit 7 = 0, 'write control' interface line is disabled;
= 1, 'write control' interface line is enabled.

Read bit 7 = 0, 'read control' interface line is disabled;
= 1, 'read control' interface line is enabled.

Operate I/O condition codes are reported to the Series/1 by the adapter or processor channel relating to conditions that can be detected during execution of the I/O commands. In the following descriptions of the adapter commands, the condition codes that may be reported during command execution are listed. If the condition that caused a condition code to be reported is unique to the command, it is explained in detail; otherwise, the condition codes defined in "I/O Instruction Condition Codes" in this chapter apply.

Read

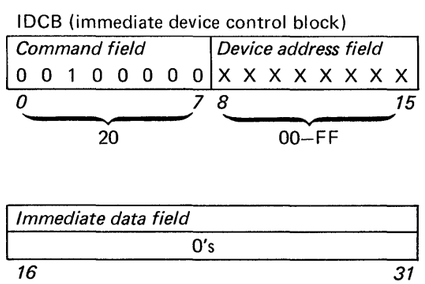


The Read command loads the byte contained in the adapter's receive buffer register into bits 24–31 of the IDCB. If command field bit 7=0, the 'read control' interface line is disabled; if command field bit 7=1, the 'read control' interface line is enabled. No interrupts result from the execution of this command.

The data in the receive buffer register is not changed or reset as a direct result of this Read command. The data in the receive buffer register is changed only by a subsequent *normal* receive operation.

Condition code 0, 1, 5, or 7 can be reported for this command. If the adapter is in either a read-busy state (Read command already accepted) or an interrupt-pending state, condition code 1 is reported. The command is not executed if condition code 0, 1, or 5 is reported.

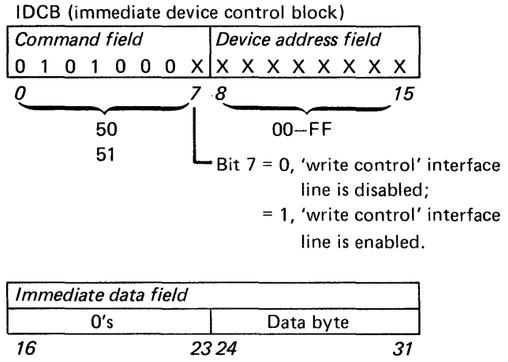
Read ID



The Read ID command loads the adapter ID byte into bits 24–31 of the IDCB. The identification byte for the teletypewriter adapter is 10 (hex).

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition 0 or 5 is reported.

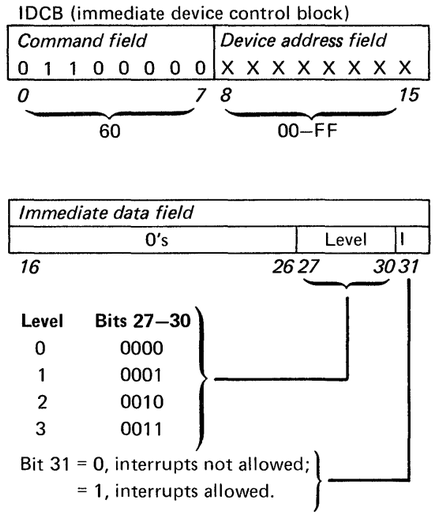
Write



The Write command loads bits 24–31 of the IDCB into the adapter's transmit data register. The adapter then transmits the byte, serially-by-bit, to the attached device. If command field bit 7=0, the 'write control' interface line is disabled; if command field bit 7=1, the 'write control' interface line is enabled. A device-end interrupt is reported to the Series/1 at the completion of the data transfer.

Condition code 0, 1, 5, or 7 can be reported for this command. If the adapter is in either a write-busy state (Write command already accepted) or an interrupt-pending state, condition code 1 is reported. The command is not executed if condition code 0, 1, or 5 is reported.

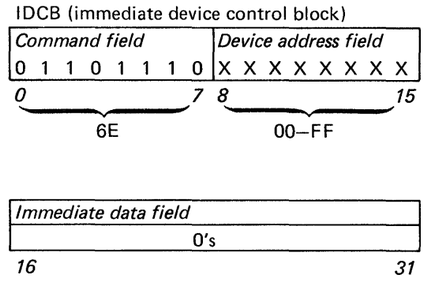
Prepare



The Prepare command loads the interrupt level and I-bit into the adapter's prepare register. The I-bit determines if the adapter is allowed to report I/O interrupts to the Series/1. If the I-bit=0, interrupts are not reported; if the I-bit=1, interrupts are reported. The interrupt level specified in bits 27–30 of the IDCB is the level on which the adapter reports interrupts. Level 0 is the highest priority level; level 3 is the lowest priority level.

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition code 0 or 5 is reported.

Reset to Diagnostic Wrap



The Reset to Diagnostic Wrap command (1) resets pending interrupts, condition codes, and all registers in the adapter, except the prepare register, and (2) disables the 'read control' and 'write control' interface lines. The adapter is placed in the diagnostic wrap state so that commands can be issued to the adapter for testing purposes. It is not necessary for an I/O device to be attached to the adapter. If a Write command is issued subsequent to this command, the data byte in the Write command IDCB is sent to the adapter's transmit data register and then serially transferred to the adapter's receive data register. At the completion of the transmit operation, the data that was diagnostically wrapped to the receive data register is transferred to the receive buffer register, and an attention interrupt is reported to the Series/1. A Read command can now be issued to check the validity of the data. A receive overrun condition can also be checked by not reading the data after the attention interrupt, but by issuing another Write command, thus causing a receive overrun condition to occur.

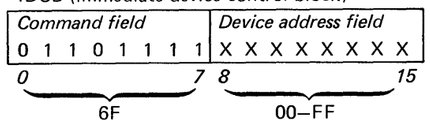
When the adapter is in the diagnostic wrap state, no data is transmitted to the attached device. The 'transmit data' line (to the device) is held in the mark state.

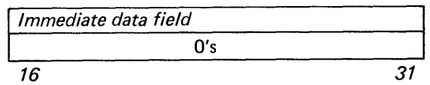
Exit from the diagnostic wrap state is by a Reset Device or Halt I/O command, a system reset, or a power-on reset.

Condition code 0 or 7 can be reported for this command. (Interface data check, condition code 5, can not be reported for this command.) The command is not executed if condition code 0 is reported.

Reset Device

IDCB (immediate device control block)





The Reset Device command resets all adapter registers, except the prepare register and the transmit data register. The 'read control' and 'write control' interface lines are disabled, and pending interrupts and condition codes are reset.

Condition code 0 or 7 can be reported for this command. The command is not executed if condition code 0 is reported.

I/O Instruction Condition Codes

Condition codes are reported to the Series/1 processor in response to I/O commands issued to the adapter. The codes are related to conditions that can be detected by the processor channel or the adapter during execution of the command. The following chart shows the I/O commands and the I/O instruction condition codes that can be reported for each command:

		I/O instruction condition code (CC=)							
Hex	**Command**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
10, 11	Read	X	X				X		X
20	Read ID	X					X		X
50, 51	Write	X	X				X		X
60	Prepare	X					X		X
6E	Reset to Diagnostic Wrap	X							X
6F	Reset Device	X							X
F0	Halt I/O								X

The condition codes have the following meanings:

CC value	Meaning
0	Device not attached. The channel reports this code if the device addressed by the I/O instruction is not attached to the system.
1	Busy. This code is reported by the teletypewriter under the following conditions: 1. To a Write command—the adapter is executing a transmit operation to the attached device or has a device-end interrupt pending. 2. To a Read command—the adapter is executing a normal receive operation or has an attention or exception interrupt pending. Busy is reported (instead of command reject) to any command not within the defined command set for the adapter if the adapter is in the write-busy, read-busy, or interrupt-pending state. Because the adapter supports full-duplex operation (simultaneous read and write), the adapter can be either (1) write-busy and read-busy, (2) write-busy and interrupt-pending, or (3) read-busy and interrupt-pending.
2	Not reported.
3	Command reject. The adapter reports this code if (1) the command received is outside the defined command set for the adapter, and (2) the adapter is not busy when the invalid command is received (refer to condition code 2 for further explanation).
4	Not reported.
5	Interface data check. This code is reported if a parity error is detected on the processor data bus during data transfer.
6	Not reported.
7	Satisfactory. This code is reported when the adapter is able to accept and execute the command.

I/O Interrupt

The teletypewriter adapter can report interrupts (if interrupts have been enabled by execution of a Prepare command) for the following conditions:

- Attention interrupt. A normal receive operation has been completed.
- Exception interrupt. An overrun receive operation has been detected.
- Device-end interrupt. A transmit or IPL operation has been completed.

Attention, exception, and device-end interrupts can be pending at the same time. I/O interrupt condition codes are presented to the Series/1 processor at interrupt acceptance time to define the type(s) of interrupt. These interrupt condition codes are subject to the following rules and considerations:

1. The attention and exception codes are associated only with receive operations; the device-end code with a transmit operation (except during an IPL operation).
2. The attention and exception codes are associated with operations initiated by the device; the device-end code is associated with operations initiated by the program.
3. Attention and exception interrupts can be posted simultaneously with the device-end interrupt. Since interrupt condition code presentation does not accommodate both the exception and device-end codes during interrupt presentation, the exception code takes precedence over the device-end code. However, the presentation and acceptance of the exception code does not reset a pending device-end interrupt.

I/O Interrupt Condition Codes

An I/O interrupt condition code defines the meaning of the adapter-presented interrupt, as follows:

Condition code (CC=)	Meaning
0	Not reported.
1	Not reported.
2	Exception. This code is reported when the adapter has completed at least one overrun receive operation. A device-end interrupt can also be pending, but the exception interrupt takes precedence in reporting.
3	Device-end. This code is reported at the completion of the transmit operation resulting from execution of a Write command or upon completion of an IPL operation. No exception interrupt is pending.
4	Attention. This code is reported when the adapter has completed a normal receive operation.
5	Not reported.
6	Attention and exception. This code is reported when the adapter has completed a normal receive operation and at least one overrun receive operation. A device-end interrupt can also be pending, but the exception code takes precedence in presentation.
7	Attention and device-end. This code is reported when the adapter has completed (1) a normal receive operation and (2) a transmit or IPL operation.

Initial Program Load (IPL)

The teletypewriter adapter can perform initial program load (IPL) as either the primary or alternate IPL source. The IPL option is selected by jumpering the appropriate pins on the adapter feature card. If the primary pins are jumpered on the adapter card and the IPL Source switch on the Series/1 console is in the Primary position, the teletypewriter adapter is selected to perform the IPL when the Load pushbutton is pressed. If the secondary pins on the adapter card are jumpered, the IPL Source switch must be in the Alternate position for the adapter to perform the IPL. If neither IPL jumper is installed, the adapter cannot be selected for IPL. Refer to "IPL Option" under "Adapter Options" in this chapter for IPL jumper pin information.

Status After Resets

The status of the registers and functions of the adapter caused by various resetting conditions are as follows:

Reset condition	Reset				
	Pending interrupts	Condition codes	Prepare level and I-bit	Transmit data register	All other registers except prepare and transmit data
Power-on reset	X	X	X	X	X
System reset	X	X	X	X	X
Halt I/O command	X	X		X	X
Reset to Diagnostic Wrap command	X	X		X	X
Reset device command	X	X			X

Chapter 7. Integrated Digital Input/Output Non-Isolated Feature

Description

The Integrated Digital Input/Output Non-Isolated feature provides sensor-based input and output in a single card attachment. The feature allows the Series/1 user to add digital sensor I/O or non-IBM devices to the processor channel, and provides the following features and operating characteristics:

- Two 16-point groups of non-isolated digital input/process interrupt (DI/PI).
- Two 16-point groups of non-isolated digital output (DO).
- Four device addresses: one for each DI/PI and DO group. All four devices are prepared for interrupt with one Prepare command.
- External synchronization for each group of DI and DO. This feature permits asynchronous data transfers.
- Interrupts can be initiated by an external-sync input (one input for each DI or DO group) or by a 0-to-1 transition on a PI point.
- Contained on one four-wide, six-high printed-circuit card which can be plugged into a Series/1 processor or a 4959 I/O expansion unit.

Digital Input

The integrated digital I/O feature has two groups of digital input/process interrupt. Each group has:

- Sixteen non-isolated input points that sense voltage input
- One 16-position DI data register for reading non-latched data
- One 16-position PI data register for reading latched data
- An 'external sync' input line and a 'ready' output line
- Interrupt capability from either external sync or process interrupt

The two groups of DI/PI points accept signals in the range of +24 Vdc to −24 Vdc. A logical 0 is any voltage of +2.5 Vdc or greater; a logical 1 is any voltage of +1.0 Vdc or less.

Latched data causes the PI data register to latch when its corresponding input goes active. The register holds this value until the program reads and resets it. This PI mode informs the user that an input signal changed at some time prior to the read instruction.

Non-latched data causes the DI data register contents to follow the changes on the corresponding input points. A read instruction in this DI mode checks the present condition of the customer input signals.

Each DI/PI group has a unique device address, and responds to specific commands. Addressing and commands are discussed in this chapter.

Each position of the DI data register follows the state of the corresponding user-input point until the register is read. The data in the register is held (1) during a Read command or (2) when the 'external sync' input line becomes active while in external-sync mode. In the second case, the data remains held until the resulting interrupt is serviced and the 'ready' line is activated. Refer to "DI External Sync" in this chapter for additional information.

Each position of the PI data register records the first 0-bit to 1-bit transition on the corresponding user-input point. The data remains in the register until one of the following is executed:

- Read PI with Reset command
- Arm PI command
- Device Reset command
- System reset
- Power-on reset

When a bit in the PI data register becomes active, a process interrupt is generated if PI mode was previously set with an Arm PI command.

A DI/PI group can be tested using two special commands: (1) Set Test Ones and (2) Set Test Zeros. When the appropriate command is executed, the user inputs are disabled, either 1's or 0's are placed on the input receivers, and the external-sync receiver is pulsed. Then, when subsequent read commands are issued, the group responds exactly as if the actual user inputs, including the PI and external-sync functions, had been set.

DI External Sync

The DI external-sync capability consists of two signal lines: an 'external sync' input line, and a 'ready' output line. A DI group is set to external-sync mode by execution of the Arm DI External Sync command. When external-sync mode is armed and the system is ready for more DI data, the 'ready' line from the DI group is set active. The user device places data on the input points, and then activates the 'external sync' line. When the 'external sync' line becomes active, the data in the DI data register is assumed to be good, and the contents of the register are held. When an interrupt is presented, the 'ready' line becomes inactive and stays inactive until the appropriate command, normally a Read DI, is executed. The 'external sync' line must then perform another transition from the 0 state to the 1 state to cause another interrupt.

External-sync mode is reset by an Arm PI command, a Device Reset command, a Halt I/O command, or any processor reset condition.

Process Interrupt (PI)

A digital input group is set to PI mode using the Arm PI command. When any bit in the register becomes active, it generates an interrupt.

PI mode is reset by an Arm DI External Sync command, a Device Reset command, a Halt I/O command, or any processor reset condition.

Digital Output

The integrated digital I/O feature has two groups of digital output. Each DO group has:

- Sixteen output points. Each point provides a non-isolated, unipolar current switch or transistor-transistor-logic (TTL) compatible output voltage.
- One 16-position DO data register.
- An 'external sync' input line and a 'ready' output line.
- Interrupt capability from the 'external sync' input line.

Each digital output group has a unique device address, and responds to the commands described in this chapter. Data is stored in the DO data register by the Write DO command. The DO data register is reset only by a power-on reset.

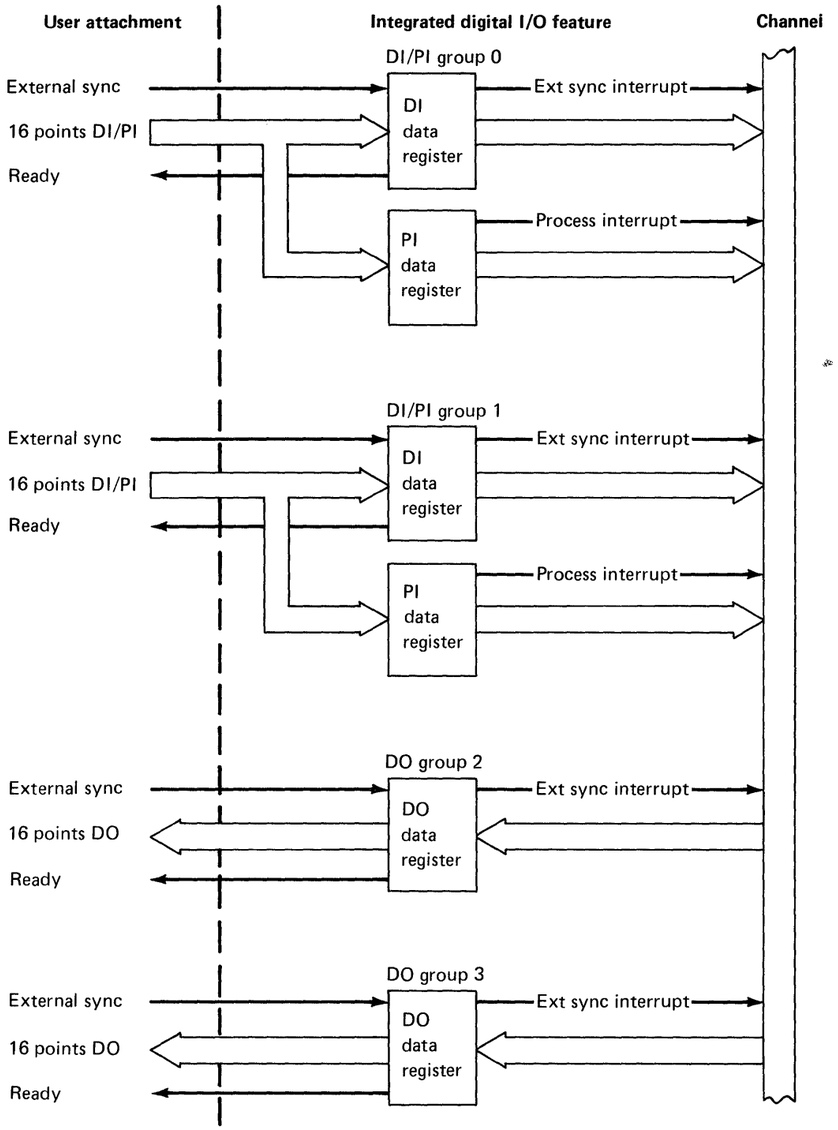
A DO group can be tested using three special commands: (1) Disable DO, (2) Read DO, and (3) Set Diagnostic External Sync. The Disable DO command disables the user outputs, the Read DO command reads the contents of the DO data register, and the Set Diagnostic External Sync command disables the user outputs and simulates the user's 'external sync' line.

DO External Sync

The DO external-sync interface consists of two signal lines: an 'external sync' input line and a 'ready' output line. A DO group is set to external-sync mode by execution of the Arm DO External Sync command. When a Write DO command is executed in external-sync mode and the data on the DO output is good, an active level on the 'external sync' input line causes the 'ready' line to become active. The user signifies receipt of the data by deactivating the 'external sync' line. When an interrupt is posted, the 'ready' line becomes inactive. The 'ready' line stays inactive until another Write DO command is executed and the 'external sync' line becomes active again. The 'external sync' line must make another transition from the 1 state to the 0 state to cause another interrupt.

External-sync mode is reset by a Device Reset command, a Halt I/O command, or any processor reset condition.

Data Flow



Addressing

The integrated digital I/O feature has four device addresses, one address for each 16-point group.

IDCB (immediate device control block)

Command field	*Device address field*
	X X X X X X X X

0 7 8 13 14 15

DI group 0 = 0 0
DI group 1 = 0 1
DO group 2 = 1 0
DO group 3 = 1 1

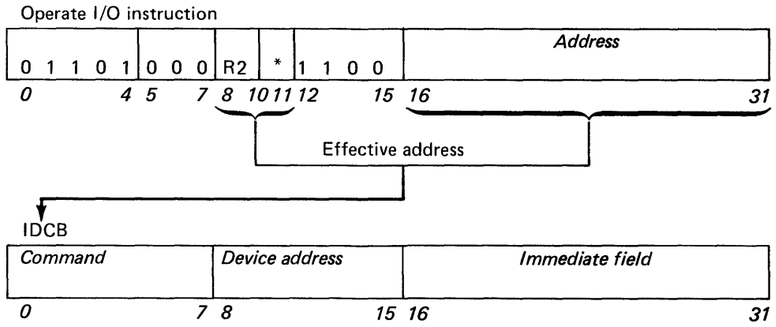
The first six (high-order) bits in the device address field of the immediate device control block (IDCB) are defined by field-installable jumpers on the feature card. The last two bits of the address field define the groups. Bit values of 00 and 01 define the DI groups; bit values of 10 and 11 define the DO groups.

Program Control

The integrated DI/DO feature uses direct program control (DPC) commands for all I/O operations; cycle-steal commands are not accepted by the feature.

Operate I/O Instruction

Communication between the Series/1 processor and the integrated digital I/O feature is initiated by the processor through execution of the Operate I/O instruction. The Operate I/O instruction generates an effective address that points to an immediate device control block (IDCB) in main storage. The IDCB contains the command field, the digital I/O device address, and the immediate data field.



*Indirect address bit

Commands

The feature responds to the following DI and DO commands from the Series/1 processor:

Digital input command code (hex)	*Name*
00	Read DI
01	Read PI
02	Read PI with Reset
20	Read ID
28	Read Status
60	Prepare
68	Arm PI
69	Arm DI External Sync
6A	Set Test 0
6B	Set Test 1
6F	Device Reset
F0	Halt I/O

Digital output command code (hex)	*Name*
20	Read ID
21	Read DO
28	Read Status
48	Write DO
60	Prepare
69	Arm DO External Sync
6B	Set Diagnostic External Sync
6C	Disable DO
6F	Device Reset
F0	Halt I/O

Note: Operate I/O condition codes, which relate to conditions that can be detected during execution of the I/O commands, are reported to the processor by the attachment or processor channel. In the following descriptions of the attachment commands, the condition codes that can be reported during command execution are listed. If the condition that causes the condition code to be reported is unique to the command, it is explained in detail; otherwise, the condition code definitions in "I/O Instruction Condition Codes" in this chapter apply.

Read DI

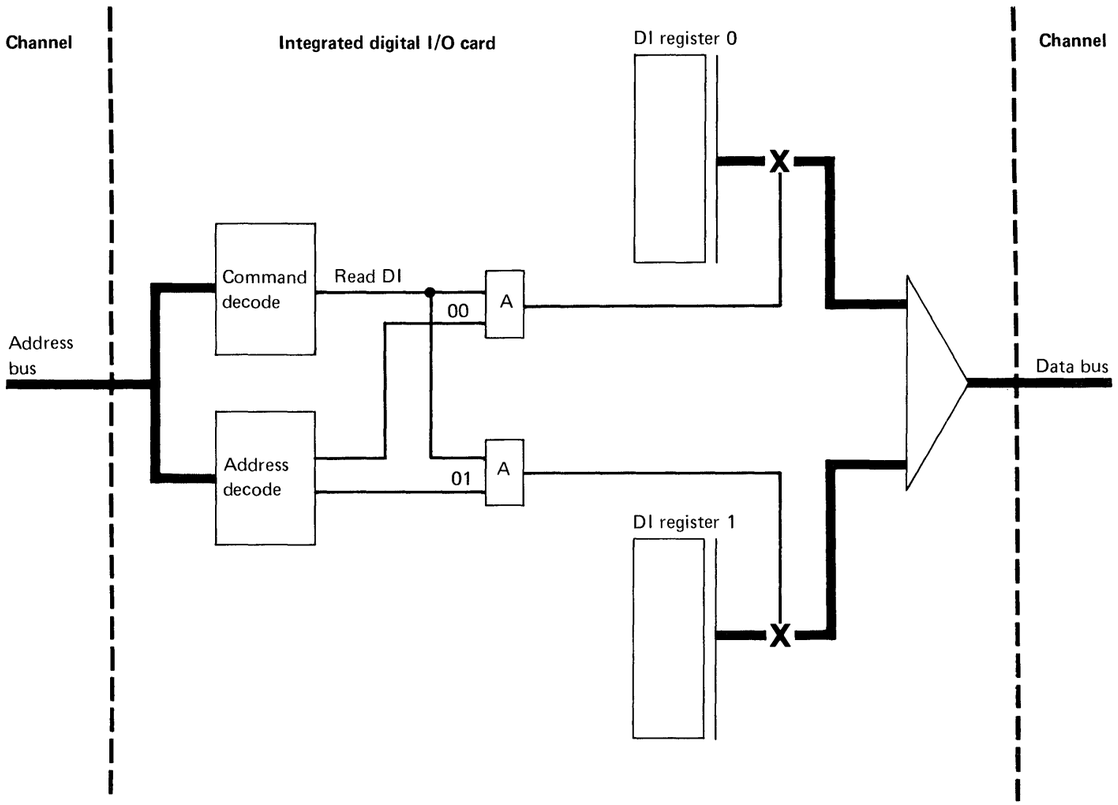
IDCB (immediate device control block)

Command field	Device address field
0 0 0 0 0 0 0 0	X X X X X X X X
0 7	8 15
00	00–3F 00–01

Immediate data field
Data from DI group
16 31

The Read DI command transfers the 16 bits of the DI data register into the immediate data field of the IDCB. If external-sync mode is armed and the 'ready' line of the addressed DI group is inactive, the 'ready' line is activated to indicate that the system is ready for more data.

Condition code 0, 1, 5, or 7 can be reported for this command. Condition code 1 is reported if external-sync mode is armed and an interrupt is pending. The command is not executed if condition code 0, 1, or 5 is reported.



Read PI

IDCB (immediate device control block)

Command field	Device address field
0 0 0 0 0 0 0 1	X X X X X X X X
0 7	8 15
01	00–3F 0–1

Immediate data field
Data from PI
16 31

The Read PI command transfers the 16 bits of the PI data register into the immediate data field of the IDCB. The PI data register is not reset.

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition code 0 or 5 is reported.

Read PI With Reset

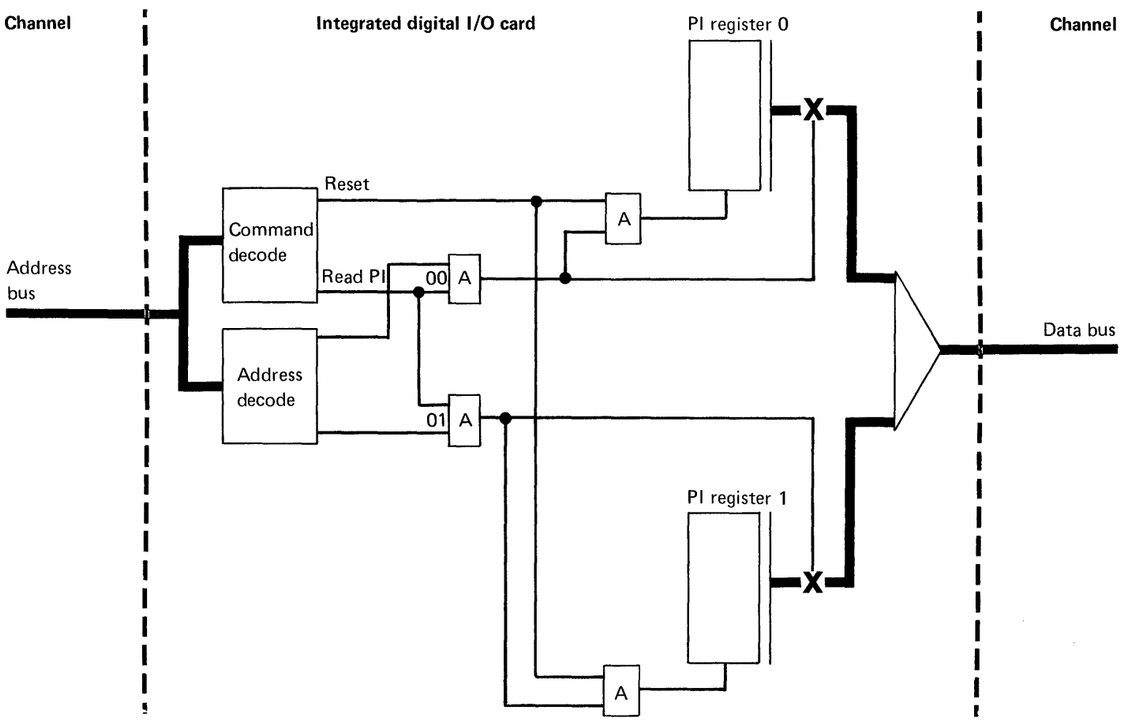
IDCB (immediate device control block)

Command field	Device address field
0 0 0 0 0 0 1 0	X X X X X X X X
0 7	8 15
02	00–3F 0–1

Immediate data field
Data from PI
16 31

The Read PI With Reset command transfers the 16 bits of the PI data register into the immediate data field of the IDCB. At the end of the command cycle, the latched data in the PI data register is reset.

Condition code 0, 1, 5, or 7 can be reported for this command. Condition code 1 is reported if PI is armed and an interrupt is pending. The command is not executed if condition code 0, 1, or 5 is reported.



Read ID

IDCB (immediate device control block)

Command field								*Device address field*							
0	0	1	0	0	0	0	0	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*
20								00–FF							

ID word from a DI group

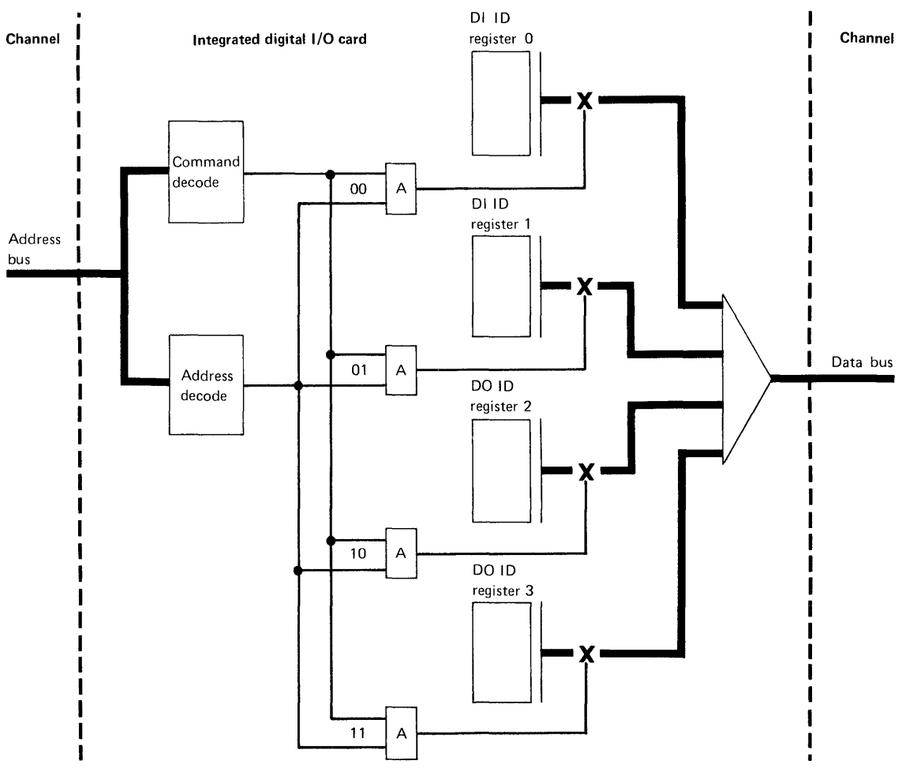
Immediate data field															
1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
16															*31*
C				0				1				0			

ID word from a DO group

Immediate data field															
1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0
16															*31*
C				0				1				8			

The Read ID command transfers a one-word identification field, called the ID word, into the immediate data field of the IDCB. The hexadecimal value of the DI ID word is C010; the hexadecimal value of the DO ID word is C018.

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition code 0 or 5 is reported.



Read DO

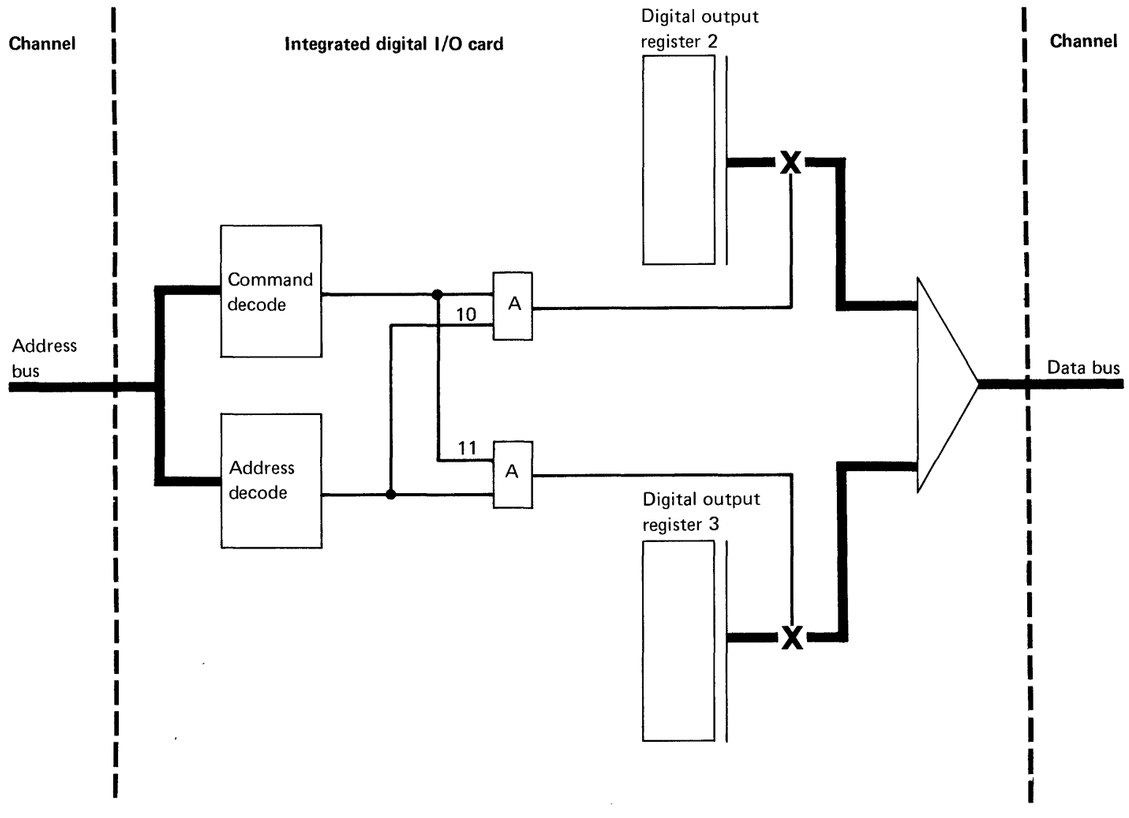
IDCB (immediate device control block)

Command field								*Device address field*							
0	0	1	0	0	0	0	1	X	X	X	X	X	X	X	X
0							*7*	*8*						*14*	*15*
21								00–3F						2–3	

Immediate data field
Data from DO group
16 *31*

The Read DO command transfers the contents of the addressed DO data register into the immediate data field of the IDCB. The command is used primarily for diagnostic purposes.

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition code 0 or 5 is reported.



Read Status

IDCB (immediate device control block)

Command field	*Device address field*
0 0 1 0 1 0 0 0	X X X X X X X X
0 — *7*	*8* — *15*
28	00–FF

Immediate data field
Status word from DI group
16 — *31*

The Read Status command transfers either the DI or DO status word into the immediate data field of the IDCB. The device address field of the IDCB determines which of the two status words is to be transferred.

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition code 0 or 5 is reported.

DI Status Word. The DI status word bits transferred to the IDCB have the following meanings:

Immediate data field

0 0 X X X X X X 0 0 0 0 0 0 0 0

16 17 18 19 20 21 22 23 24 — *31*

- *00 =* *No interrupt is pending.*
- *01 =* *The interrupt has been serviced, but either the PI register has not been reset (PI mode) or ready has not been set (external sync mode).*
- *10 =* *(Invalid bit combination.)*
- *11 =* *The device is in an interrupt state. If the device is prepared, an interrupt is being presented to the channel.*
- *1 =* *Set test 0 mode is set.*
- *1 =* *Set test 1 mode is set.*
- *1 =* *External sync mode is armed.*
- *1 =* *PI mode is armed.*

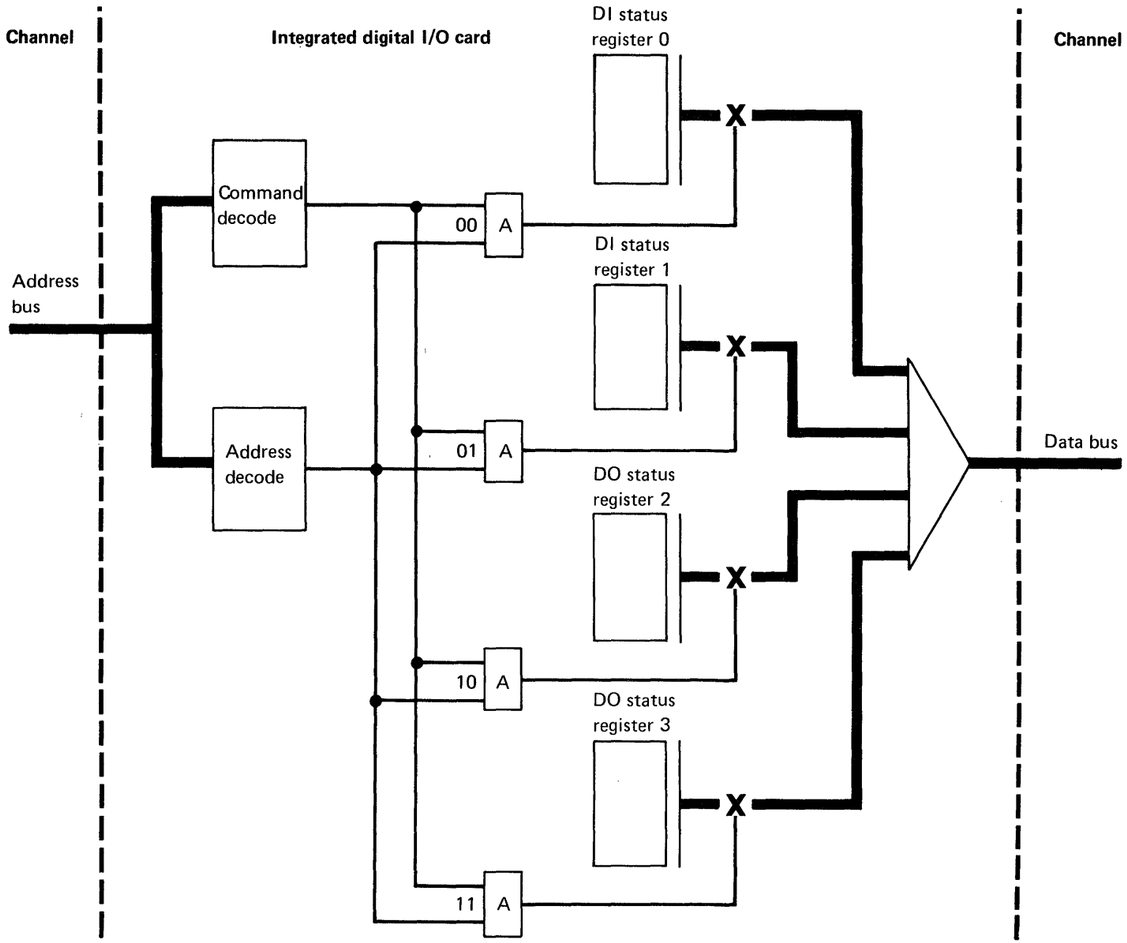
DO Status Word. The DO status word bits transferred to the IDCB have the following meanings:

Immediate data field

0 0 X X X 0 X X 0 0 0 0 0 0 0 0

16 17 18 19 20 21 22 23 24 — *31*

- *00 =* *No interrupt is pending.*
- *01 =* *The interrupt has been serviced, but ready has not been enabled.*
- *10 =* *(Invalid bit combination.)*
- *11 =* *The device is in an interrupt state. If the device is prepared, an interrupt is being presented to the channel.*
- *1 =* *Diagnostic external sync was set.*
- *1 =* *External sync mode is armed.*
- *1 =* *Disable mode is set.*



Write DO

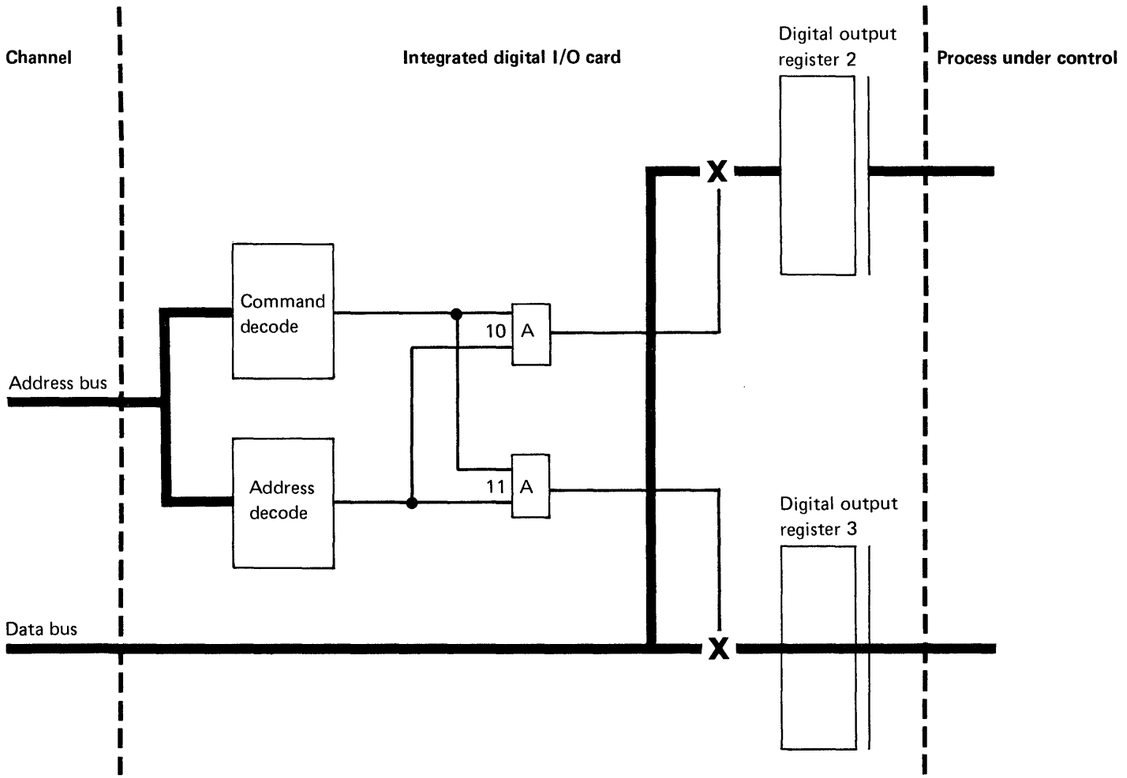
IDCB (immediate device control block)

Command field	*Device address field*
0 1 0 0 1 0 0 0	X X X X X X X X
0 — *7*	*8* — *15*
48	00–3F 2–3

Immediate data field
Data to DO
16 — *31*

The Write DO command transfers the contents of the immediate data field of the IDCB into the DO data register. If external-sync mode is armed and no interrupt is pending, the 'ready' line for the DO group is enabled.

Condition code 0, 1, 5, or 7 can be reported for this command. Condition code 1 is reported if an interrupt is pending or 'ready' is active in the external-sync mode. The command is not executed if condition code 0, 1, or 5 is reported.



Prepare

IDCB (immediate device control block)

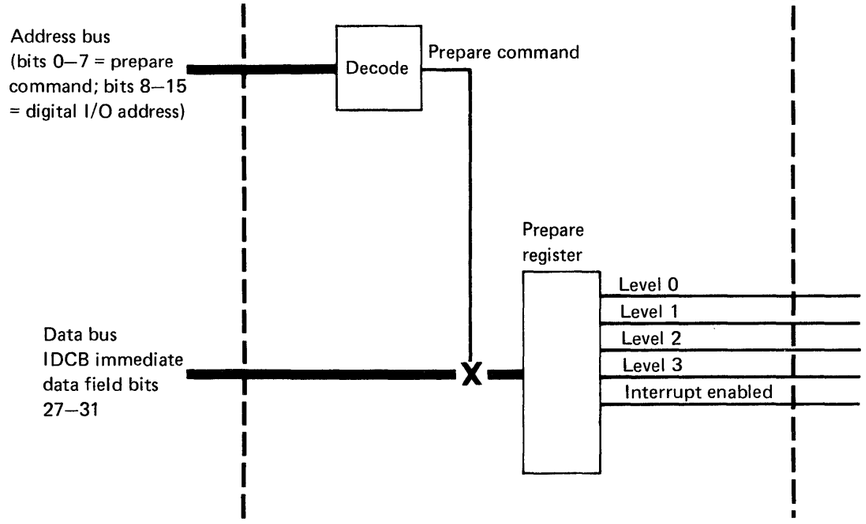
Command field	*Device address field*
0 1 1 0 0 0 0 0	X X X X X X X X
0 — *7*	*8* — *15*
60	00–FF

Immediate data field		
0's	Level	
16 — *26* *27*	— *30*	*31*

Bits 27–30	Level	Bit 31
0000	0	0 = interrupts
0001	1	not allowed
0010	2	1 = interrupts
0011	3	allowed

The Prepare command assigns the integrated DI/DO feature to a priority-interrupt level and enables or disables the ability to interrupt. The level field (bits 27–30) of the IDCB defines the interrupt level, and the I-bit (bit 31) controls the interrupt capability. All groups (four device addresses) are prepared to the same interrupt level and are enabled by the same I-bit.

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition code 0 or 5 is reported.



Arm PI

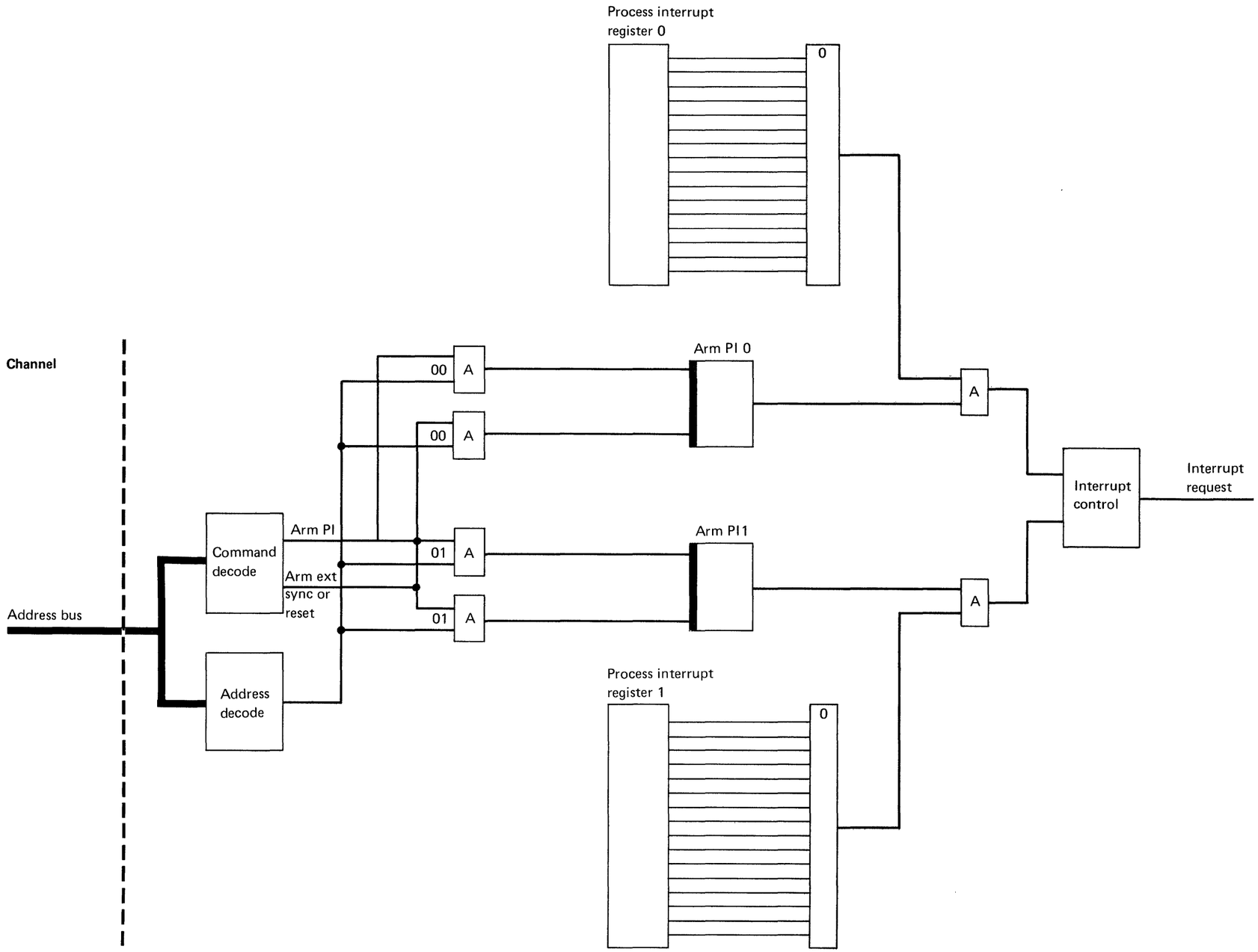
IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	0	0	0	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*
68								00–3F							0–1

Immediate data field	
0's	
16	*31*

The Arm PI command sets the addressed DI group to the PI mode. If external sync was armed, it is reset.

Condition code 0, 1, 5, or 7 can be reported for this command. Condition code 1 is reported if an interrupt is pending. The command is not executed if condition code 0, 1, or 5 is reported.



Arm DI External Sync

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	0	0	1	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*
69								00–3F							0–1

Immediate data field
0's
16 *31*

The Arm DI External Sync command sets the addressed DI group into external-sync mode. If PI was armed, it is reset. The 'ready' line is activated.

Condition code 0, 1, 5, or 7 can be reported for this command. Condition code 1 is reported if an interrupt is pending. The command is not executed if condition code 0, 1, or 5 is reported.

DI External Sync. The DI external-sync capability consists of two signal lines: an 'external sync' input line and a 'ready' output line. A DI group is set to external-sync mode by execution of the Arm DI External Sync command. When external-sync mode is armed and the system is ready to accept DI data, the 'ready' line for the DI group is set active. The user device senses the active state of the 'ready' line, presents data to the DI input points, and then activates the 'external sync' line. The 'external sync' line becoming active indicates that the data to the DI input points is assumed to be valid and that the contents of the DI register are stable. An interrupt is presented to the processor. The 'ready' line becomes inactive and remains inactive until the appropriate command, normally Read DI, is executed by the processor.

External-sync mode is reset by an Arm PI command, a Device Reset command, a Halt I/O command, or any processor reset condition.

Arm DO External Sync

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	0	0	1	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*
69								00–3F							2–3

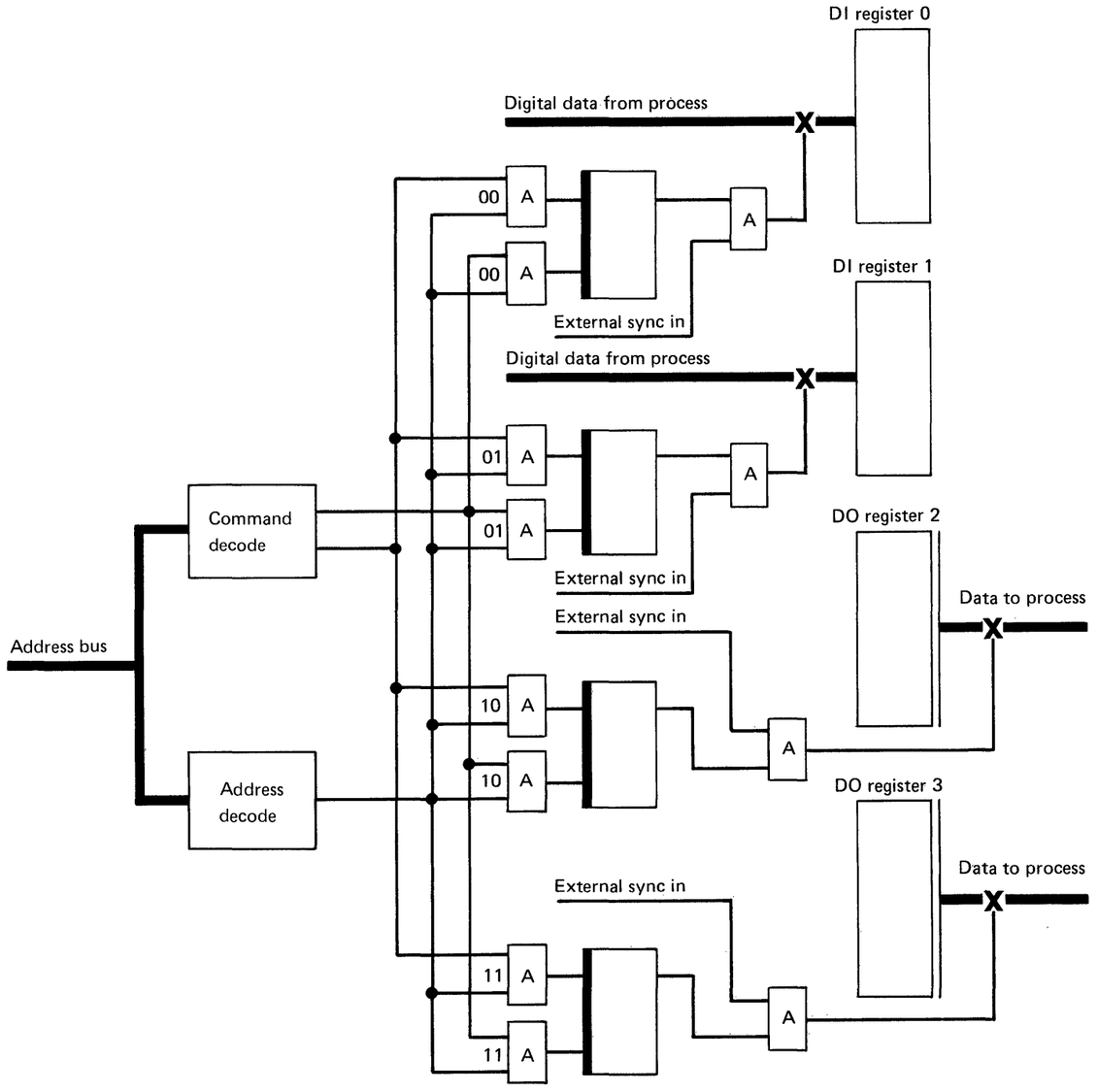
Immediate data field
0's
16 *31*

The Arm DO External Sync command sets the addressed DO group to the external-sync mode.

Condition code 0, 1, 5, or 7 can be reported for this command. Condition code 1 is reported if an interrupt is pending. The command is not executed if condition code 0, 1, or 5 is reported.

DO External Sync. The DO external-sync capability consists of two signal lines: an 'external sync' input line and a 'ready' output line. A DO group is set to external-sync mode by execution of the Arm DO External Sync command. When a user device is ready to receive the data from a DO group, it activates the 'external sync' line. If the data in the DO register is valid, the integrated DI/DO feature activates the 'ready' line to signal the user device that DO data is available. The user device signals receipt of the DO data by deactivating the 'external sync' line. When an interrupt is presented to the processor, the 'ready' line becomes inactive. The 'ready' line remains inactive until a Write DO command is executed by the processor and 'external sync' becomes active again.

External-sync mode is reset by a Device Reset command, a Halt I/O command, or any processor reset condition.



Set Test 0

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	0	1	0	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*
6A								00–3F							0–1

Immediate data field	
0's	
16	*31*

The Set Test 0 command sets a diagnostic mode that disables the user inputs, including 'external sync.' The 'ready' line is also disabled. The command places 0-bits into the digital input registers and pulses the 'external sync' input line. If external-sync mode is armed, an interrupt is presented to the processor. Subsequent Read commands result in all 0-bits from the DI and PI registers.

Condition code 0, 1, 5, or 7 can be reported for this command. Condition code 1 is reported if an interrupt is pending. The command is not executed if condition code 0, 1, or 5 is reported.

Set Test 1

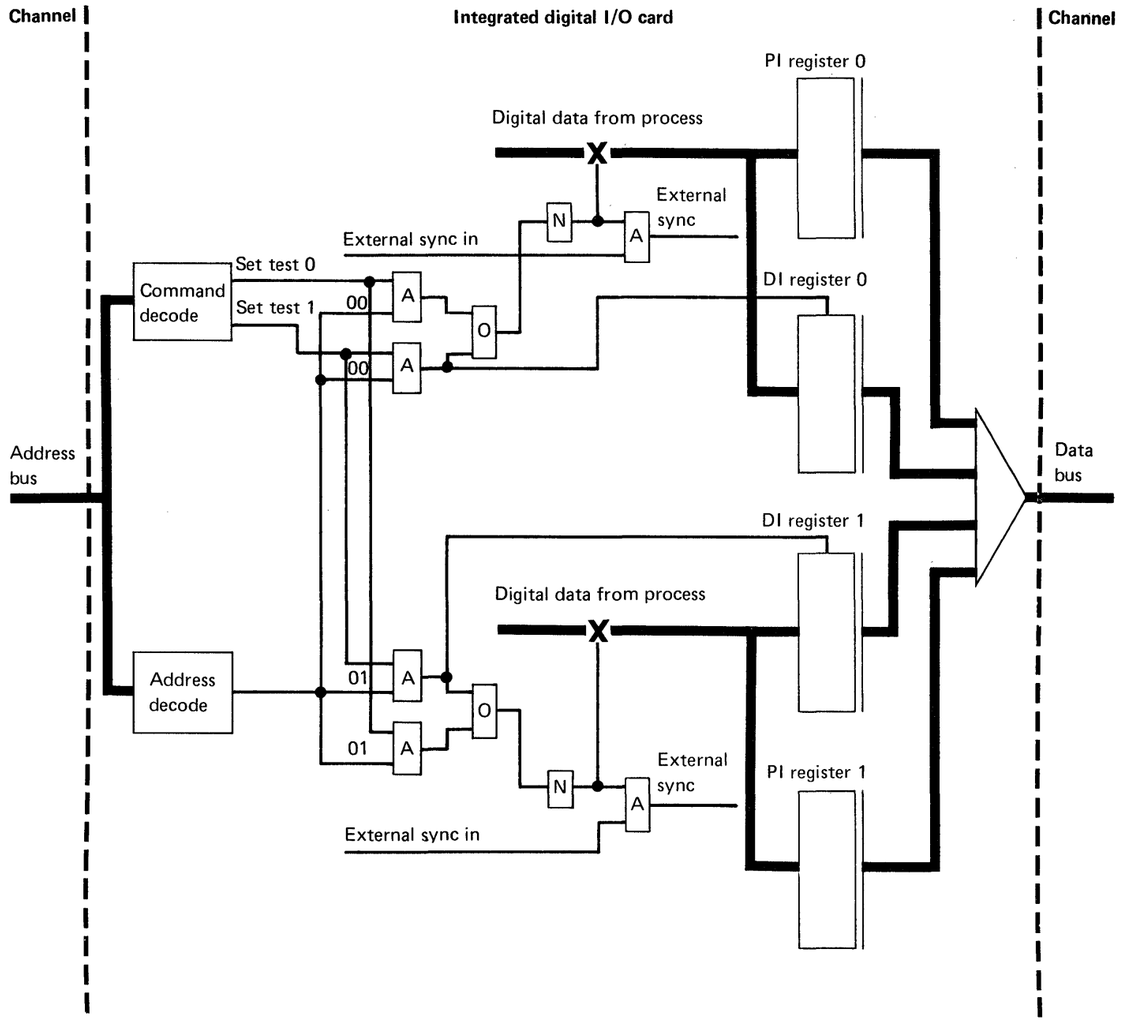
IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	0	1	1	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*
6B								00–3F							0–1

Immediate data field	
0's	
16	*31*

The Set Test 1 command sets a diagnostic mode that disables the user inputs, including 'external sync.' The 'ready' line is also disabled. The command places 1-bits in the digital input registers and pulses the 'external sync' input line. If external-sync mode is armed, an interrupt is presented to the processor. Subsequent Read commands result in all 1-bits from the DI registers. If either of the DI groups has been set previously to PI mode, the data remains all 1-bits until reset.

Condition code 0, 1, 5, or 7 can be reported for this command. Condition code 1 is reported if an interrupt is pending. The command is not executed if condition code 0, 1, or 5 is reported.



Set Diagnostic External Sync

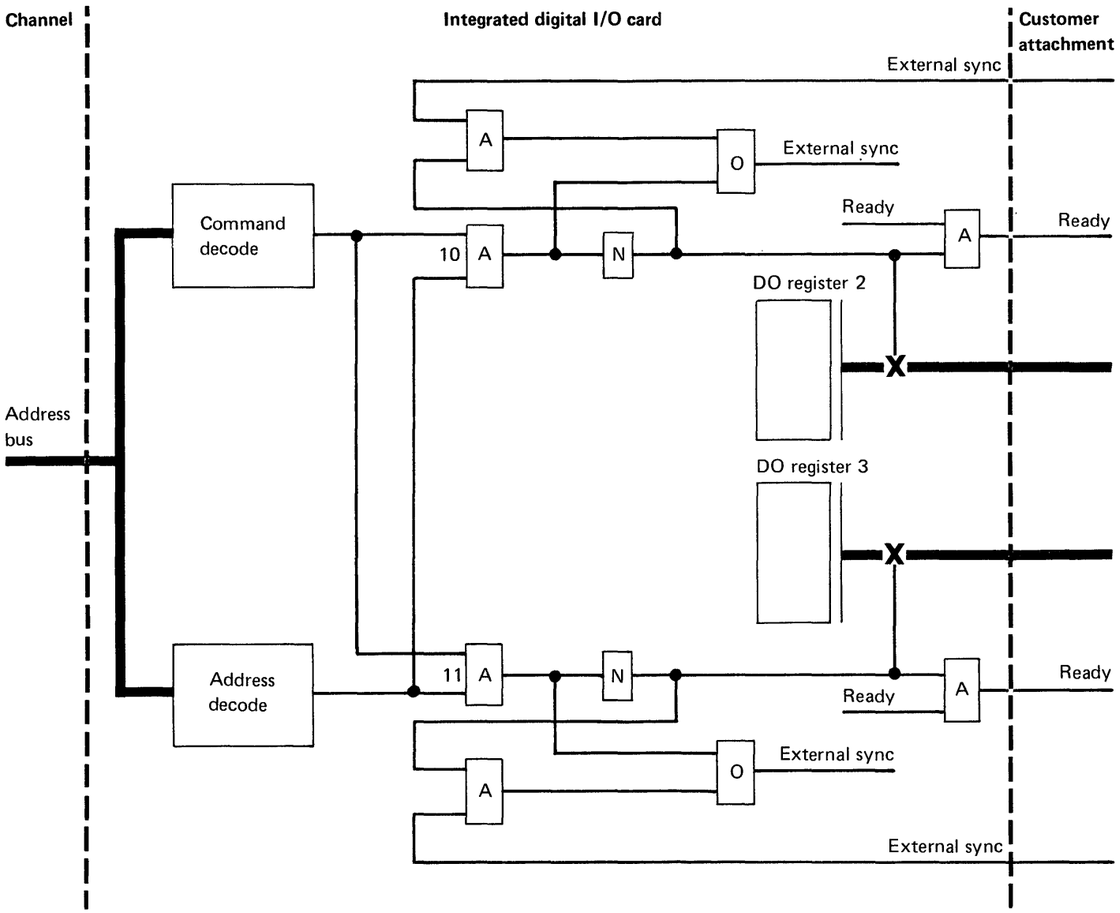
IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	0	1	1	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*
6B								00–3F							2–3

Immediate data field
0's
16 *31*

The Set Diagnostic External Sync command sets a diagnostic mode that disables the user's 'external sync' input line. The 'ready' line and DO outputs are also disabled. The command activates 'external sync' with a pulse on the input receiver. If (1) external-sync mode is armed, (2) a Disable DO command was previously executed, and (3) no current interrupt is pending, an interrupt is presented to the processor. This command must not be executed until after the Disable DO command is executed, or the external-sync interrupt cannot be set.

Condition code 0, 1, 5, or 7 can be reported for this command. Condition code 1 is reported if an interrupt is pending. The command is not executed if condition code 0, 1, or 5 is reported.



Disable DO

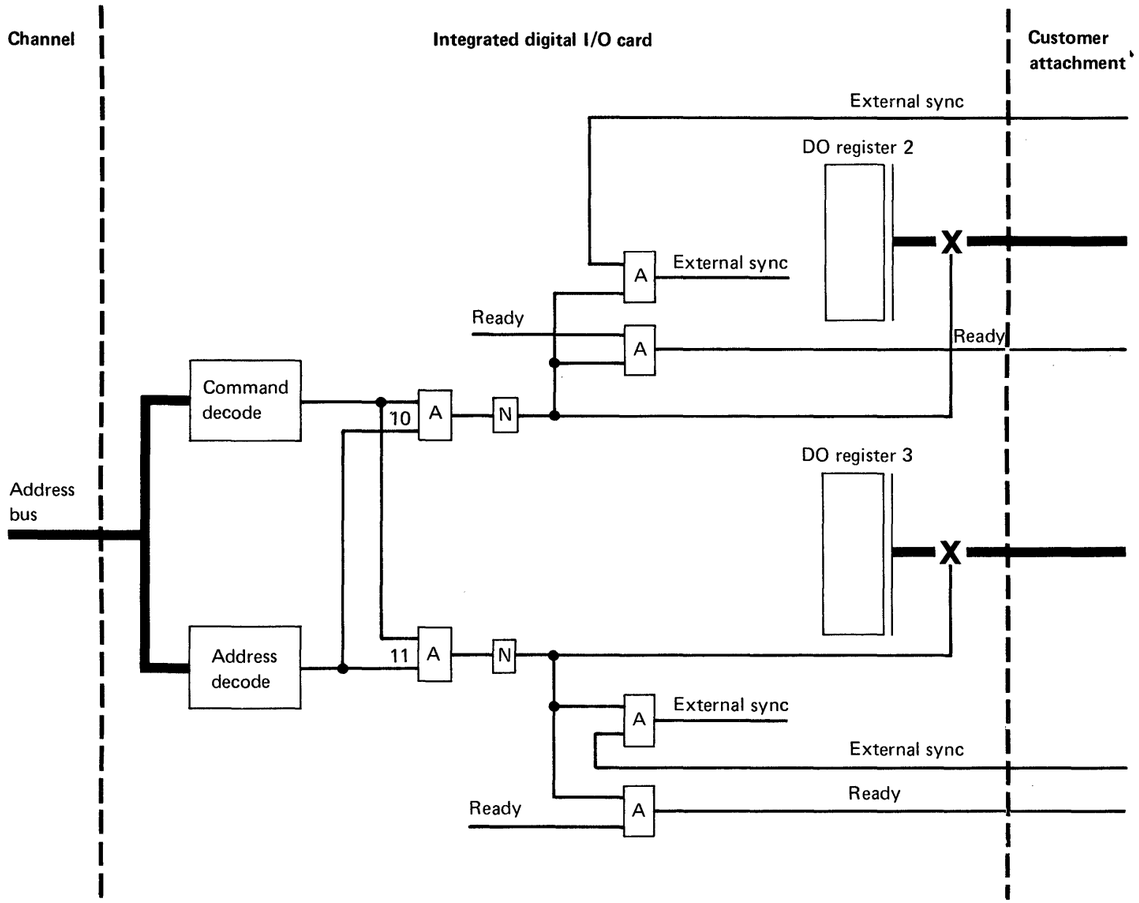
IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	0	1	1	0	0	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*
6C								00–3F							2–3

Immediate data field
0's
16 *31*

The Disable DO command sets a diagnostic mode that disables the 16 digital output lines for the addressed DO group, the 'ready' line, and the user's 'external sync' input line. All outputs for the DO group are set to 0's.

Condition code 0, 1, 5, or 7 can be reported for this command. Condition code 1 is reported if an interrupt is pending. The command is not executed if condition code 0, 1, or 5 is reported.



Device Reset

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 1 1 1 1	X X X X X X X X
0 *7*	*8* *15*
6F	00–FF

Immediate data field
0's
16 *31*

The Device Reset command resets the following items for the addressed digital input or output group:

- Any pending interrupt
- Arm PI mode
- Arm external-sync mode (DI and DO)
- Status word
- DI data register
- PI data register
- Diagnostic mode
- The 'ready' line

The DO registers are not reset.

Halt I/O

IDCB (immediate device control block)

Command field	*Device address field*
1 1 1 1 0 0 0 0	0's
0 *7*	*8* *15*
F0	

Immediate data field
0's
16 *31*

The Halt I/O command is a channel-directed command that causes a halt of all I/O activity on the channel and resets any pending interrupts. The following functions of the integrated DI/DO feature are reset:

- Arm PI mode
- Arm external-sync mode (DI and DO)
- Diagnostic mode
- The 'ready' line (DI and DO)

The following functions are not reset:

- Prepare register and I-bit
- PI and DI data registers
- DO data registers

I/O Instruction Condition Codes

Condition codes are reported to the Series/1 processor in response to an Operate I/O instruction directed to the integrated DI/DO feature. The condition codes are related to conditions that can be detected during execution of the instruction command. The following chart shows the I/O commands and the condition codes that can be reported:

I/O command	Hex	I/O instruction condition codes 0	1	2	3	4	5	6	7
Read DI	00	X	X				X		X
Read PI	01	X					X		X
Read PI with Reset	02	X	X				X		X
Read ID	20	X					X		X
Read DO	21	X					X		X
Read Status	28	X					X		X
Write DO	48	X	X				X		X
Prepare	60	X					X		X
Arm PI	68	X	X				X		X
Arm DI External Sync	69	X	X				X		X
Arm DO External Sync	69	X	X				X		X
Set Test 0	6A	X	X				X		X
Set Test 1	6B	X	X				X		X
Set Diagnostic External Sync	6B	X	X				X		X
Disable DO	6C	X	X				X		X
Device Reset	6F	X							X
Halt I/O*	F0								X

*Channel-directed command

Note: Condition code 3 is reported if a command other than the preceding commands is directed to the attachment.

The condition codes have the following meanings:

Condition code	*Meaning*
0	Device not attached
1	Busy
2	Not reported
3	Command reject
4	Not reported
5	Interface data check
6	Not reported
7	Satisfactory

I/O Interrupt

The integrated DI/DO feature presents only *attention* interrupts.

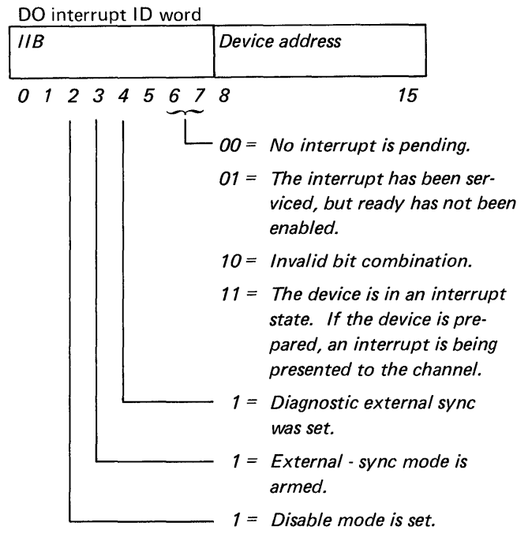
Interrupts for a DI group are initiated by (1) the 'external sync' input line becoming active while in external-sync mode or (2) any bit in the PI register becoming active while in PI mode. Interrupts for a DO group are initiated by the 'external sync' input line becoming inactive while in external-sync mode.

Because all devices are prepared to interrupt on the same level, interrupts from more than one device are stacked. The device with the lowest device address presents its interrupt first. All other interrupts waiting in the stack at that time are cleared before the same device can present a second interrupt. For example, if devices 0, 1, and 2 have interrupts stacked, device 0 presents its interrupt first. Device 0 cannot present another interrupt until the interrupts for devices 1 and 2 have been presented.

When an interrupt is accepted by the channel, the digital group presents an interrupt ID word. This word contains an IIB (interrupt information byte) in bits 0–7 and the device address in bits 8–15. The format of the IIB for the DI groups and for the DO groups has the same format as the first byte of the status word transferred into the immediate data field of the IDCB when a Read Status command is executed.

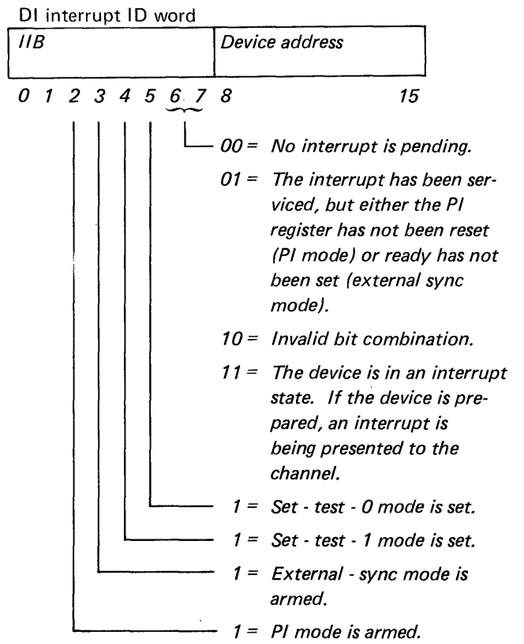
DO Interrupt ID Word

The bits in the interrupt information byte (IIB) of the DO interrupt ID word have the same meanings as the bits in the device DO status word. The meaning of each bit is defined as follows:



DI Interrupt ID Word

The bits in the interrupt information byte (IIB) of the DI interrupt ID word have the same meanings as the bits in the device DI status word. The meaning of each bit is defined as follows:



I/O Interrupt Condition Codes

The only interrupt reported by the DI/DO feature is the attention interrupt. The interrupt condition code for an attention interrupt is condition code 4.

Status After Resets

The following table lists the resets to the integrated DI/DO feature for the indicated reset conditions:

Reset	Condition		
	Power-on reset	System reset	Halt I/O command or machine check reset
Arm conditions for PI or external sync modes	X	X	X
Diagnostic modes	X	X	X
Ready lines	X	X	X
Any pending interrupts	X	X	X
Prepared level and I bit	X	X	
PI and DI data registers (DI resets only)	X	X	
DO Data registers (DO resets only)	X		

Chapter 8. Customer Direct Program Control Adapter Feature

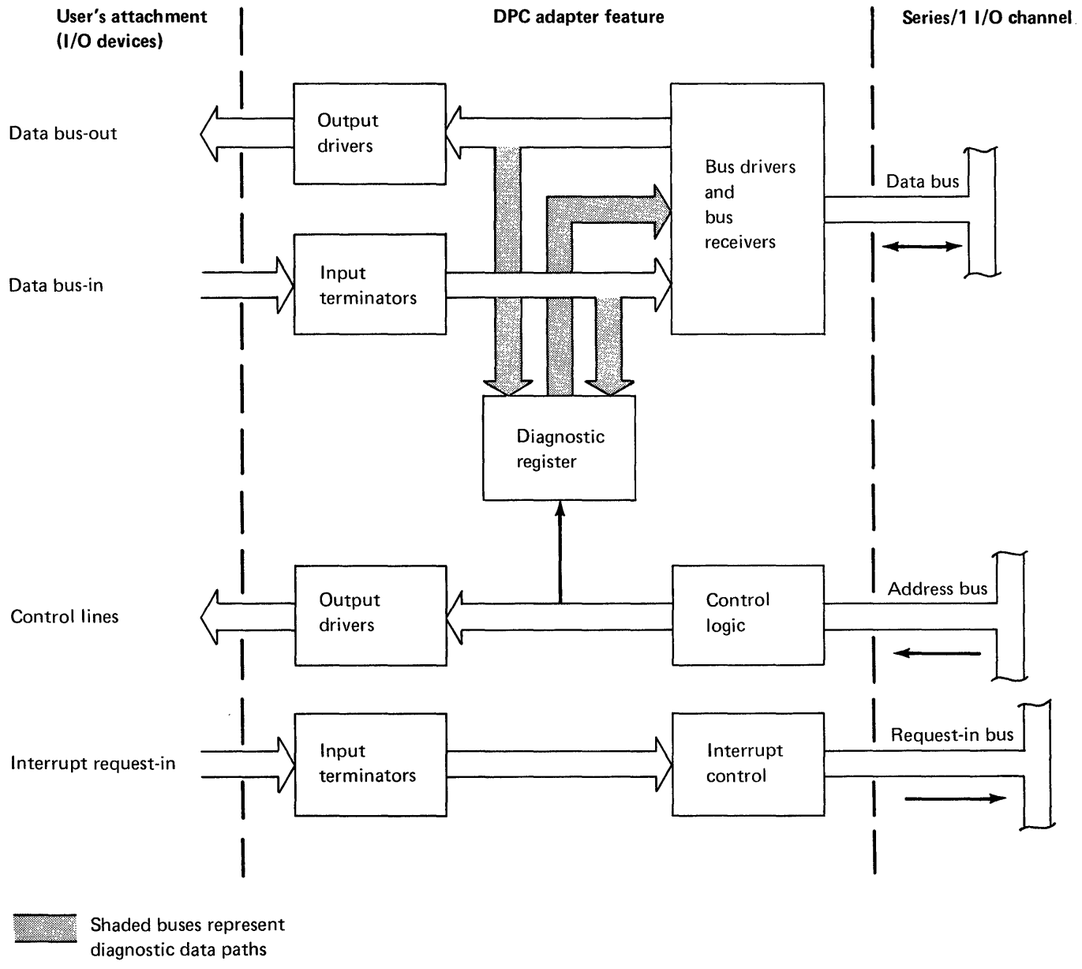
Description

The Customer Direct Program Control Adapter feature allows I/O devices and subsystems to be attached to the Series/1 processor channel. All communications between the Series/1 processor, the adapter, and the attached devices are initiated by the processor through execution of Operate I/O instructions. The adapter feature performs direct program control (DPC) functions only; it does not perform cycle-steal operations. The adapter feature is contained on one four-wide, six-high printed-circuit card, which can be plugged into any I/O slot of a Series/1 processor or a 4959 I/O expansion unit.

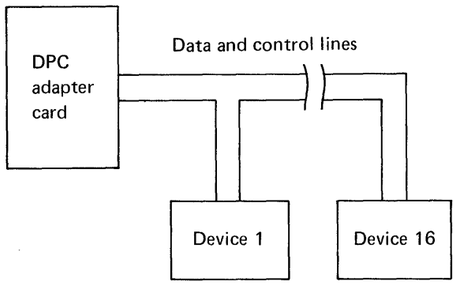
The feature card provides the following:

- Can be configured, through jumper options on the card, to accommodate 4, 8, or 16 I/O devices.
- Interrupt vectoring of 16 interrupt sources. All attached devices share the same interrupt level and interrupt enable bit. Interrupt priority is established by the device address.
- 75 data and control lines to the attached devices:
  - 18 data bus-in lines (16 data lines plus 2 parity lines)
  - 18 data bus-out lines (16 data lines plus 2 parity lines)
  - 16 interrupt request lines
  - 4 device address lines
  - 3 function lines
  - 4 modifier lines
  - 12 control and response lines
- Optional parity checking of the data bus lines to the attached devices. This parity option is selected by a jumper on the card.

Data Flow



Data and Control Lines to the Attached Devices



Line name	Number of lines	Direction	
		Adapter	Device
I/O active	1	→	
Function bits	3	→	
Modifier bits	4	→	
Device address	4	→	
Data bus-out	16 + 2 optional parity	→	
Interrupt service active	1	→	
Strobe	1	→	
Data bus-in	16 + 2 optional parity	←	
Interrupt request	16	←	
Condition code in	3	←	
Select response	1	←	
Halt or machine check	1	→	
System reset	1	→	
Power on reset	1	→	
Diagnostic mode	1	→	
Diagnostic mode modifier	1	→	

The 75 data and control lines that connect the I/O devices to the DPC adapter are described in the following paragraphs:

I/O Active. This outbound tag line signals the device that it may begin executing the command specified by the 'function' and 'modifier' lines.

Function and Modifier. These seven lines correspond to the command field of the immediate device control block (IDCB). Command field bits 1–3 are the function bits; command field bits 4–7 are the modifier bits.

Device Address. These four outbound lines represent the encoded device address bits that the adapter uses to select the device that is to respond to the specified operation. If the adapter is configured for 16 devices, all four lines are used for the device address.

Data Bus-Out. This outbound data bus consists of 16 data lines and two parity lines. If the parity option is not selected (jumper not installed on the feature card), the parity lines are not activated for data transfers to the device. The data bus is active from 200 nanoseconds prior to the rise of the 'I/O active' line until the fall of the 'select response' line.

Interrupt Service Active. This adapter-generated tag line signals an I/O device that the interrupt service sequence may begin. The line is active from 200 nanoseconds after 'device address' is activated until the fall of 'select response.'

Strobe. The 'strobe' line is generated by the adapter and sent to the device that is currently selected. 'Strobe' is active during I/O-active and interrupt-service-active sequences. During I/O-active sequences, the device uses 'strobe' to register data that is received from the adapter and to reset data on certain inbound data transfers. During an interrupt-service-active sequence, 'strobe' may be used to reset a device's interrupt request, IIB, or ISB. If the parity option is jumpered and a parity error is detected on the adapter channel during a read operation, 'strobe' is inactive for the entire sequence. When a parity error is detected during a write operation, regardless of the parity jumper option, 'strobe' is inactive for the entire sequence, except to a Device Reset command.

Data Bus-In. This inbound data bus consists of 16 data lines and two parity lines. Parity bits are accepted by the adapter only if the parity option is jumpered.

Interrupt Request. These 16 lines are inbound lines from the attached devices to the adapter. When a device detects an interrupt condition, it raises its 'interrupt request' line and holds the line active until it (1) is serviced, (2) receives a Device Reset or Halt I/O command, or (3) is reset by a system reset, a machine-check reset, or a power-on reset. The 16 'interrupt request' lines correspond to the 16 devices that can be attached to the adapter; however, only the interrupt lines corresponding to the adapter-configuration jumper option (4, 8, or 16) are used.

Condition Code In. This three-line bus carries the binary-encoded condition code status from the devices to the adapter during I/O-active or interrupt-service-active sequences.

Select Response. This tag line is sent to the adapter, from a device, to signal recognition of an I/O-active or interrupt-service-active sequence. The tag also indicates to the adapter that the data and/or control information has been placed on the 'data bus-in' lines. The data and/or control information is activated no later than the rise of this tag line, as seen at the output of the device. This tag line may fall no sooner than the fall of the 'I/O active' or 'interrupt service active' lines.

Halt or Machine Check. This tag line is generated on the adapter channel to indicate that the adapter has detected a Halt I/O command or a machine-check class interrupt. When this tag is detected by the devices, all status, states, interrupt requests, control logic, and registers are reset.

System Reset. This tag line is generated on the adapter channel to all devices. All device status, states, interrupt requests, control logic, and registers are reset.

Power On Reset. The adapter generates this tag line to indicate that it has detected a power-on sequence or a power-off sequence from the processor channel. When this tag line is active, all components are held in the system reset state.

Diagnostic Mode. This tag line becomes active when a Set Diagnostic Mode command is executed by the adapter and bit 16 of the IDCB is equal to 1. The use of 'diagnostic mode' is device-dependent, and it can be used as a programmable control line to the attached devices. Refer to "Set Diagnostic Mode" under "Adapter-Directed Commands" in this chapter for additional information.

Diagnostic Mode Modifier. This tag line becomes active when a Set Diagnostic Mode command is executed by the adapter and bits 16 and 31 of the IDCB are equal to 1's. The use of 'diagnostic mode modifier' is device-dependent, and it can be used as a programmable control line to the attached devices. Refer to "Set Diagnostic Mode" under "Adapter-Directed Commands" in this chapter for additional information.

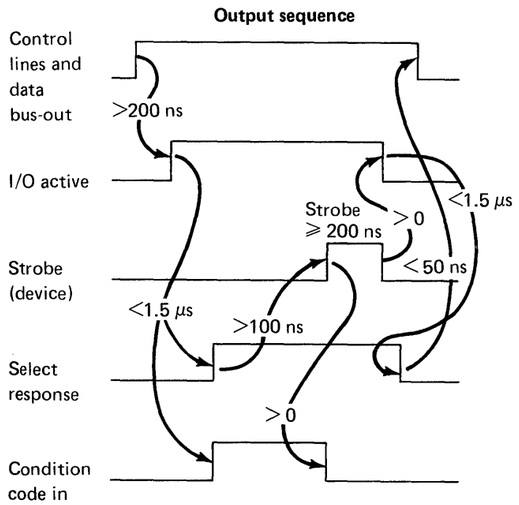
DPC Adapter Operating Sequences

Three types of operating sequences can be performed by the adapter. They are output, input, and interrupt-service sequences.

Output Sequence

An output sequence (adapter-to-device) is executed as follows:

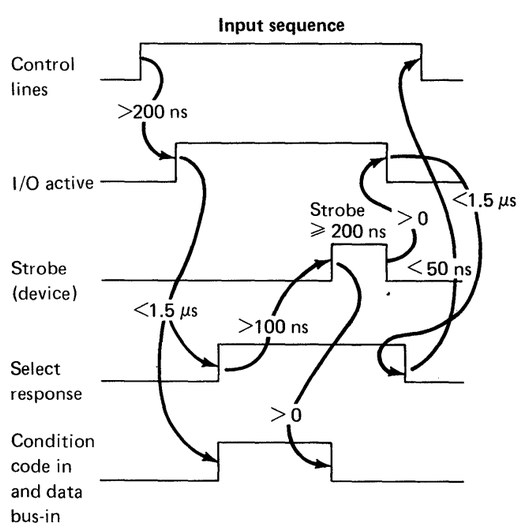
1. Function, modifier, device address, and data bits are placed on their appropriate lines.
2. The 'I/O active' tag is skewed (at least 200 nanoseconds) and activated on the interface.
3. When the device recognizes its address and 'I/O active,' it raises the 'select response' tag. Once 'select response' is raised, it must be held active at least until the fall of 'I/O active.' The 'condition code in' lines must be active until 'strobe' becomes active or until 'I/O active' becomes inactive for the duration of 'select response.'
4. 'Strobe' is activated and then dropped. If the DPC adapter is configured without the parity option and a parity error is detected between the processor I/O channel and the adapter, 'strobe' is not activated except during a subsequent Device Reset command.
5. 'I/O active' is deactivated.
6. When the device recognizes the absence of 'I/O active,' it drops the 'select response' and 'condition code in' lines.
7. The function, modifier, device address, and data bits are deactivated.



Input Sequence

An input sequence (device-to-adapter) is executed as follows:

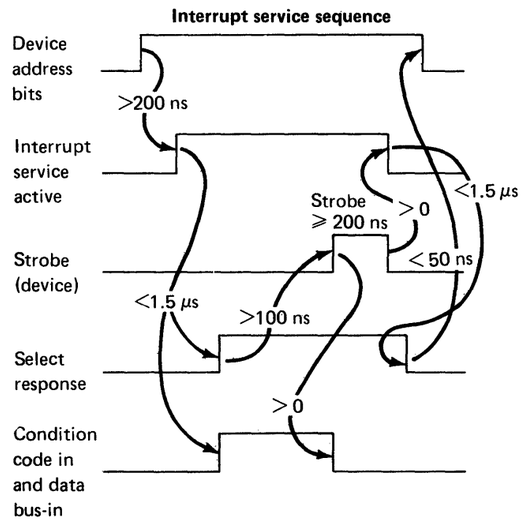
1. Function, modifier, and device address bits are placed on their appropriate lines.
2. The 'I/O active' tag is skewed (at least 200 nanoseconds) and activated on the interface.
3. When the device recognizes its address and 'I/O active,' it raises the 'select response' tag. Once 'select response' is raised, it must be held active at least until the fall of 'I/O active.' The 'data bus in' and 'condition code in' lines must be active until 'strobe' becomes active or until 'I/O active' becomes inactive for the duration of 'select response.'
4. 'Strobe' is activated and then dropped; however, if a parity error is detected by the processor, this tag is not activated.
5. 'I/O active' is deactivated.
6. When the device recognizes the absence of 'I/O active,' it drops 'select response' and deactivates the 'condition code in' and 'data bus in' lines.



Interrupt Service Sequence

A typical interrupt service sequence is executed as follows:

1. The device address bits are placed on their appropriate lines.
2. The 'interrupt service active' tag is skewed (at least 200 nanoseconds) and activated on the interface.
3. When the device recognizes its address and 'interrupt service active,' it raises the 'select response' tag. Once 'select response' is raised, it must be held active at least until the fall of 'interrupt service active.' The 'condition code in' and 'data bus in' lines must be active for the duration of 'select response' or at least remain active until 'strobe' becomes active.
4. 'Strobe' is activated and then dropped. The I/O device must reset its interrupt request at the leading edge of 'strobe.'
5. 'Interrupt service active' is deactivated.
6. When the device recognizes the absence of 'interrupt service active,' it drops 'select response' and deactivates the 'condition code in' and 'data bus in' lines.
7. The 'device address' lines are deactivated.



DPC Adapter Feature Card

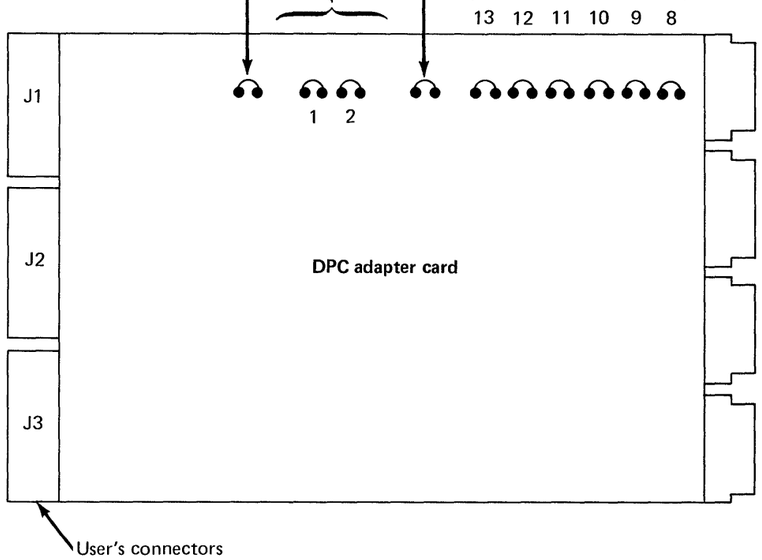
Device configuration jumpers— These two jumpers are used to specify the device configuration attached to the adapter card.

Jumper 1	Jumper 2	Configuration
On	Off	4 devices
Off	On	8 devices
Off	Off	16 devices

Diagnostic interrupt mask— When installed, this jumper masks off any interrupts from devices during external diagnostic mode.

Parity option jumper— With this jumper installed, parity is checked and generated on the data bus-in and bus-out lines.

Device address jumpers— These jumpers represent the high-order address range assigned to the adapter devices. When the adapter is configured for four devices, the device address from the IDCB is compared with address jumpers 8–13. When the adapter is configured for eight devices, the device address from the IDCB is compared with address jumpers 8–12. When the adapter is configured for 16 devices, the device address from the IDCB is compared with address jumpers 8–11.



Addressing

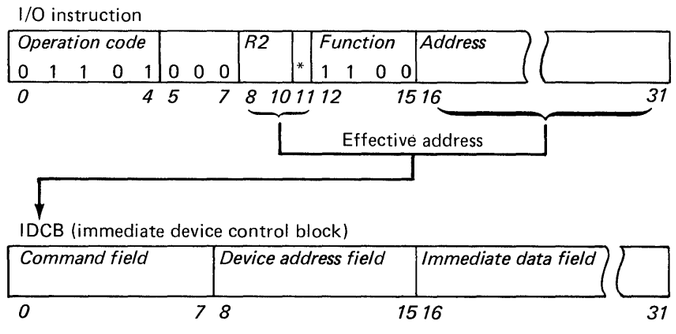
The customer DPC adapter can be configured for 4, 8, or 16 device addresses by selecting the appropriate jumper option on the feature card. The addresses can be in the range of 0–255 (hexadecimal 00–FF), but must be consecutive for the number of configured devices. Also, the first device address assigned to the adapter devices must begin on an address boundary that has bits 28–31 of the IDCB equal to 0's (for example, the device address field equal to hexadecimal 00, 10, 20, etc.).

Program Control

Communication between the Series/1 processor, the customer DPC adapter, and the attached devices is initiated by the processor. All adapter and device functions (control, write, and read) are initiated by execution of Operate I/O instructions stored in the processor.

Operate I/O Instruction

The Operate I/O instruction generates an effective address that points to an immediate device control block (IDCB) in main storage. The IDCB contains the command field, the device address field, and the immediate data field.



*Indirect address bit

Commands

There are two types of commands associated with the customer DPC adapter: adapter-directed commands and device-directed commands.

Adapter-directed commands are IBM-defined, and they perform specific actions using only the adapter. These commands must use the specified command codes.

Device-directed commands (except Read ID and Device Reset) are defined by the user. The modifier portion (bits 4–7) of the IDCB command field is available to the user to define operations in the attached devices.

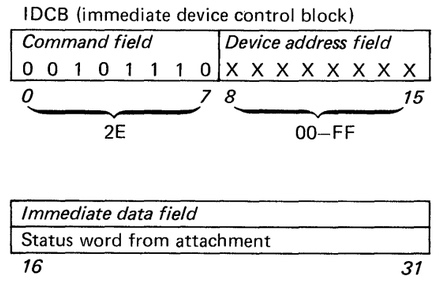
Adapter-Directed Commands

The customer DPC adapter executes the following adapter-directed commands:

Command code (hex)	Name
2E	Read Adapter Status
2F	Read Diagnostic Data
60	Prepare
61	Set Diagnostic Mode
62	Reset Diagnostic Mode

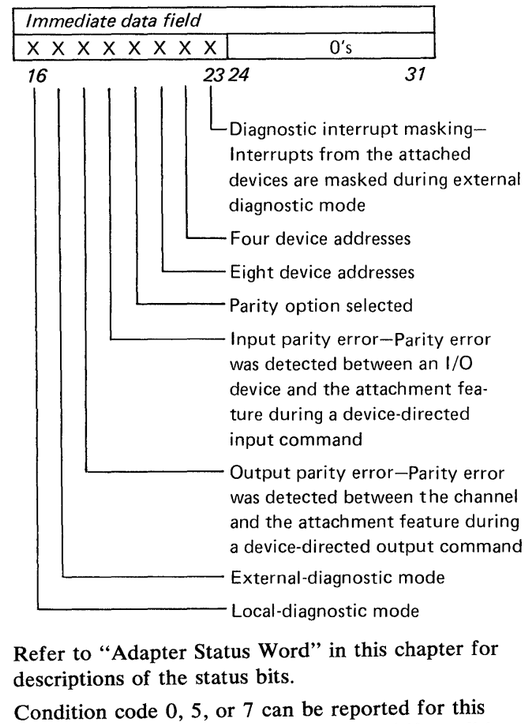
Note: Operate I/O instruction condition codes, relating to conditions that can be detected during execution of the I/O commands, are reported to the processor by the adapter or processor channel. In the following descriptions of the adapter-directed commands, the condition codes that can be reported for the commands are listed. Refer to "I/O Instruction Condition Codes" in this chapter for condition code definitions.

Read Adapter Status



The Read Adapter Status command transfers the 16 bits of the adapter status word to the immediate data field of the IDCB. Input- or output-parity error status in the adapter is reset (if active) after the status word is transferred.

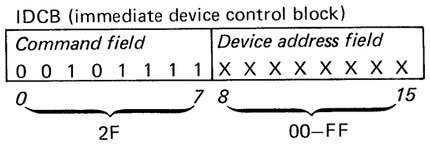
The bits in the adapter status word have the following meanings:



Refer to "Adapter Status Word" in this chapter for descriptions of the status bits.

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition code 0 or 5 is reported. If condition code 5 is reported, the status word in the IDCB immediate data field is not valid.

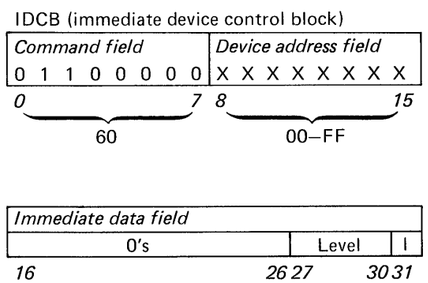
Read Diagnostic Data



The Read Diagnostic Data command transfers the 16 bits from the adapter diagnostic register to the immediate data field of the IDCB. The diagnostic register is not reset. If the adapter is not in diagnostic mode and this command is executed, the immediate data field of the IDCB is set to 0.

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition code 0 or 5 is reported.

Prepare

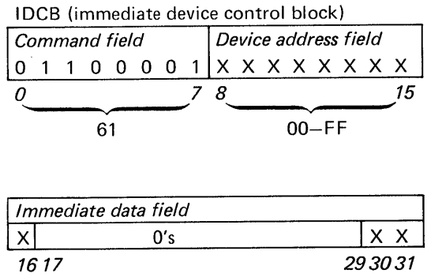


The Prepare command assigns the customer DPC adapter to a priority interrupt level and enables oı disables the adapter's ability to interrupt. All devices attached to the adapter are prepared to the same interrupt level and are enabled by the same I-bit. The interrupting priority of the attached devices is determined by the device addresses; the lowest device address has the highest interrupt priority.

The level field (bits 27–30) of the IDCB defines the interrupt level, and the I-bit (bit 31) controls the interrupt capability.

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition code 0 or 5 is reported.

Set Diagnostic Mode



The Set Diagnostic Mode command sets the adapter into diagnostic mode, resets the diagnostic register, and provides a "wrap-back" test of the adapter 'control' and 'data bus-out' lines. The data that is "wrapped back" is loaded into the diagnostic register, and can be read by executing a Read Diagnostic Data command.

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition code 0 or 5 is reported.

The particular diagnostic functions performed by the Set Diagnostic Mode command and subsequent commands are controlled by the bits in the IDCB, as follows:

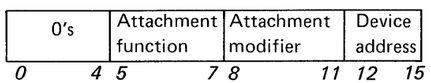
IDCB Bit 16=0. When bit 16 of the IDCB is 0, the Set Diagnostic Mode command is directed to the adapter card. The command places the adapter in local-diagnostic mode. With the adapter in local-diagnostic mode, output- and input-parity error bits in the status word are always 0's, all interrupts from the attached I/O devices are masked, data from the I/O devices is ignored, and all data and control lines from the adapter to the I/O devices are inactive. Any subsequent device-directed commands are responded to by the adapter. Under this condition, bits 30 and 31 of the IDCB have the following meanings:

Bits 30 and 31=00—This causes the adapter to initiate an attention interrupt. The interrupt information byte (IIB) is presented as 0, and the device address is either DDDD0000 for a 16-device configuration, DDDDD000 for an 8-device configuration, or DDDDDD00 for a 4-device configuration (the D's are the high-order bits of the jumpered device address on the adapter card). After the interrupt is serviced by the processor channel, the interrupt request is reset. If an additional interrupt request is desired, another Set Diagnostic Mode command, with the same IDCB format, must be issued.

Bits 30 and 31=01—This causes the adapter to load data into the diagnostic register during any subsequent device-directed command, as follows:

1. A Write or Write Control command loads the data field of the IDCB into the adapter diagnostic register. The contents of the diagnostic register can then be read by issuing a Read Diagnostic Data command. If condition code 5 is reported to the Write or Write Control command, the data in the diagnostic register is not changed.
2. A Read or Read Status command causes the adapter to set all 0's into the data field of the IDCB and set all 0's into the diagnostic register. If condition code 5 is reported, the data in the IDCB data field is not valid, and the data in the diagnostic register is not changed.

Bits 30 and 31=10—This loads the adapter-to-device control line bits into the adapter diagnostic register during any subsequent device-directed command. Under this mode of operation, the data in the diagnostic register has the following format:



Adapter function, modifier, and device address are adapter control lines. The adapter function and modifier bits are equivalent to bits 1–3 and bits 4–7, respectively, of the command field in the IDCB. When a subsequent device-directed command is issued, the adapter responds, as follows:

1. A Write or Write Control command loads the adapter control-line bits into the adapter diagnostic register. The contents of the diagnostic register can then be read by issuing a Read Diagnostic Data command. If condition code 5 is reported to the Write or Write Control command, the data in the diagnostic register is not changed.
2. A Read or Read Status command causes the adapter to load all 0's into the data field of the IDCB, and the adapter-to-device control line bits into the diagnostic register. The contents of the diagnostic register can then be read by a Read Diagnostic Data command. If condition code 5 is reported to the Read or Read Status command, the data field of the IDCB is not valid, and the data in the diagnostic register is not changed.

Bits 30 and 31=11—This causes the adapter control lines described in the paragraph "Bits 30 and 31=10" to be logically ANDed with the data lines described in the paragraph "Bits 30 and 31=01." The result is loaded into the diagnostic register. When a subsequent device-directed command is issued, the adapter responds, as follows:

1. A Write or Write Control command loads the ANDed data into the diagnostic register. The contents of the diagnostic register can then be read by issuing a Read Diagnostic Data command. If condition code 5 is reported for the Write or Write Control command, the data in the diagnostic register is not changed.
2. A Read or Read Status command causes the adapter to load all 0's into the data field of the IDCB and the diagnostic register. The contents of the diagnostic register can then be read by issuing a Read Diagnostic Data command. If condition code 5 is reported for the Read or Read Status command, the data field of the IDCB is not valid, and the data in the diagnostic register is not changed.

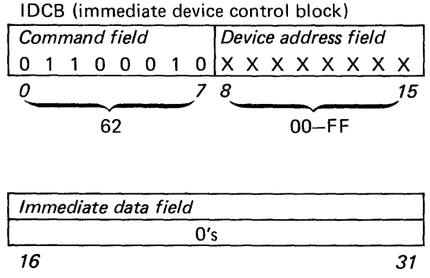
IDCB Bit 16=1. When bit 16 of the IDCB is 1, the Set Diagnostic Mode command is directed to the attached I/O devices; the diagnostic mode is called external-diagnostic mode. When the adapter is in external-diagnostic mode, device-directed commands are passed to the addressed devices, and the adapter lines to the devices remain active, as in normal operations. The 'diagnostic mode' line is active and remains active as long as the adapter is in external-diagnostic mode. Input- and output-parity error bits have the same meaning as in normal operation, and the diagnostic register is set to the value of 'data bus-in' from the devices. Under this condition, bits 30 and 31 have the following meanings:

Bit 30=1—This forces the 'Halt I/O' or 'machine check' reset line to go active and causes all I/O devices to take appropriate reset actions.

Bit 31=1—This sets the 'diagnostic mode modifier' tag line to the active state.

The uses of diagnostic mode and the diagnostic-mode modifier are device-dependent. The user can use them as programmable control lines to the attached devices.

Reset Diagnostic Mode



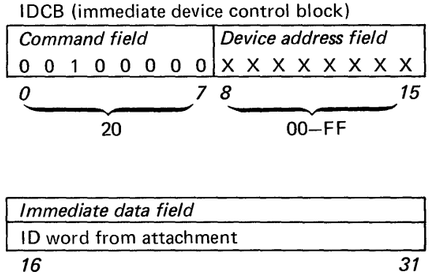
The Reset Diagnostic Mode command resets the adapter diagnostic mode and the diagnostic register. If the adapter is not in diagnostic mode, the command is accepted, but it has no effect on the adapter status and data. The immediate data field of the IDCB is not used, but it is checked for proper parity.

Condition code 0, 5, or 7 can be reported for this command. If condition code 0 or 5 is reported, the command is not executed.

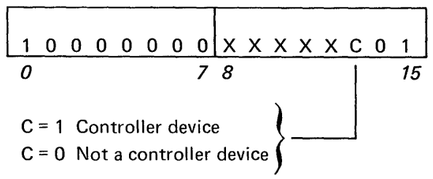
Device-Directed Commands

IBM defines two device-directed commands: Read ID and Device Reset. All other device-directed commands are *user-defined* for the connected user's device. Refer to "Designer-Defined Device-Directed Commands" in this chapter.

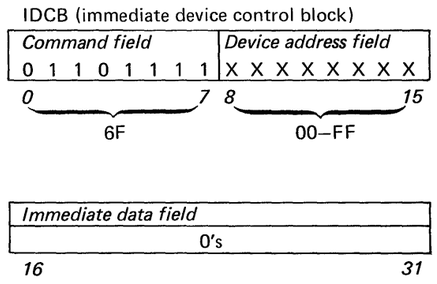
Read ID



The Read ID command transfers the ID word from the customer DPC adapter and the user's device to the immediate data field of the IDCB. The contents of the ID word are:



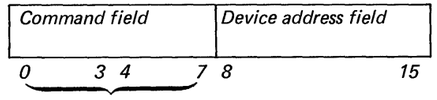
Device Reset



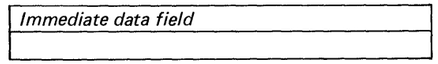
The Device Reset command resets the addressed device and any pending device interrupts.

Designer-Defined Device-Directed Commands

The following designer-defined commands (except those combinations of X's that result in IBM adapter-directed commands) are available for use with devices attached to the customer DPC adpater. Bits 4–7 of the command field are defined by the user to meet the design characteristics of the device.



Command field	Hex	Command type
0 0 0 0 X X X X	0X	Read Data
0 0 0 1 X X X X	1X	Read Data
0 0 1 0 X X X X	2X	Read Status
0 1 0 0 X X X X	4X	Write Data
0 1 0 1 X X X X	5X	Write Data
0 1 1 0 X X X X	6X	Write Control



Read Data. The Read Data commands transfer 16 bits of data from the addressed device to the immediate data field of the IDCB.

Read Status. The Read Status command transfers 16 bits of status from the addressed device to the immediate data field of the IDCB.

Write Data. The Write Data commands transfer 16 bits of data from the immediate data field of the IDCB to the addressed device.

Write Control. The Write Control command initiates a control action in the addressed device. A word transfer from the immediate data field of the IDCB is device-dependent, and may occur during command execution.

I/O Instruction Condition Codes

Condition codes are reported to the Series/1 processor in response to an Operate I/O instruction directed to the customer DPC adapter and to the attached user devices. The condition codes are related to conditions that can be detected during execution of the instruction command.

Hex	Command	I/O instruction condition code values (CC=) 0	1	2	3	4	5	6	7
0X	Read Data	X	X	X	X	X	X	X	X
1X	Read Data	X	X	X	X	X	X	X	X
20	Read ID	X					X		X
2X	Read Status	X	X	X	X	X	X	X	X
2E	Read Adapter Status Word	X					X		X
2F	Read Adapter Diagnostic Data	X					X		X
4X	Write Data	X	X	X	X	X	X	X	X
60	Prepare	X					X		X
61	Set Diagnostic Mode	X					X		X
62	Reset Diagnostic Mode	X					X		X
6X	Write Control	X	X	X	X	X	X	X	X

The condition codes have the following meanings:

Condition code (CC=)	Meaning	Reported by
0	Device not attached	Channel
1	Busy	Device**
2	Busy after reset	Device**
3	Command reject	Adapter/device**
4	Intervention required	Device**
5	Interface data check*	Channel/adapter/device**
6	Controller busy	Adapter
7	Satisfactory	Adapter/device**

* The user's device reports this code to the adapter only when the parity option is selected.

** Condition codes returned by a user's device are device-dependent (a device may not require use of the complete condition code set).

CC=0 (Device not attached). Reported by the channel when the addressed device is not attached to the system.

CC=1 (Busy). Reported by the device when it is unable to execute a command because it is in the busy state. The busy state is entered when an interrupt-causing command is accepted; it is exited when the processor accepts the interrupt. Certain devices enter the busy state when an external event, which results in an interrupt request, occurs.

CC=2 (Busy after reset). Reported by the device when it is unable to execute a command because of a reset from which the device has not yet returned to the quiescent state. No interrupt occurs.

CC=3 (Command reject). Reported by the adapter or device when it has received a command that is not in the valid command set, or when the adapter or device is in an improper state to execute the command.

CC=4 (Intervention required). Reported by the device when it is unable to execute a command because of a condition that requires manual intervention to correct (for example, no paper in a printer).

CC=5 (Interface data check). Reported by the channel, the adapter, or the device (if the parity option is selected) when a parity error occurs on a data bus. The adapter also reports this condition code when a parity error is detected on the device data bus during execution of a Write Data or Write Control command and the parity option is not selected.

CC=6 (Controller busy). Reported by the adapter to indicate that the adapter, and not the addressed device, is busy.

CC=7 (Satisfactory). Reported by the adapter or device when it successfully accepts the command.

I/O Interrupt

The I/O devices that attach to the customer DPC adapter may be designed as interrupting devices capable of performing operations that continue beyond the execution of the Operate I/O instruction. Interrupts are presented by these devices at the termination of the operation. The adapter allows the vectoring of interrupts for up to 16 user-attached devices, and presents these interrupts to the processor on the single priority level assigned to the adapter by the Prepare command.

The device presents its interrupt request on one of the 16 inbound 'interrupt request' lines. Refer to "Data and Control Lines to Attached Devices" in this chapter for a description of the 'interrupt request' lines.

When a device presents an interrupt, it also presents a condition code that at least specifies the general cause of the interrupt, and may present an interrupt status byte that specifies the *exact* cause of the interrupt.

The interrupts that can be presented by the adapter are:

- Controller-end interrupt
- Exception interrupt
- Device-end interrupt
- Attention interrupt
- Attention and exception interrupt
- Attention and device-end interrupt

Controller-End Interrupt

The controller-end interrupt is presented by the adapter after it has previously reported I/O instruction condition code 6 (controller busy) to an I/O instruction. Controller end signifies that the adapter is now free to accept I/O commands for the devices that it controls. The device address reported with the controller-end interrupt is the lowest numerical value of the addresses controlled by the adapter. The interrupt information byte (IIB) of the interrupt ID word is presented as 0.

Exception Interrupt

The exception interrupt is presented if an error or exception condition is associated with the interrupt. The condition is defined in the interrupt status byte (ISB) of the interrupt ID word and, if required, in the device-dependent status word.

Device-End Interrupt

The device-end interrupt is presented if no error, exception, or attention conditions occur during the I/O operation.

Attention Interrupt

The attention interrupt is presented if the interrupt was caused by an external event and not by the execution of an I/O command. If the event has this singular meaning, no further status recording is required.

Attention and Exception Interrupt

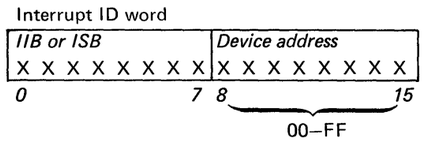
The attention and exception interrupt is presented if the attention and exception conditions occur simultaneously.

Attention and Device-End Interrupt

The attention and device-end interrupt is presented if the attention and device-end conditions occur simultaneously.

Interrupt ID Word

Acceptance of an interrupt causes the adapter to present an interrupt ID word to the Series/1 processor. This word is placed into register 7 of the interrupting level, and has the following format:



For interrupt condition codes 2 and 6, the interrupt status byte (ISB) is presented with the interrupt. For all other condition codes, presentation of the interrupt information byte (IIB) is device-dependent.

Interrupt Status Byte (ISB)

The ISB is a special format of the interrupt information byte (IIB), and contains detailed information about the cause of the interrupt. The ISB is presented for error or exception conditions only (interrupt condition code 2 or 6). The ISB bits are normally set as a result of status errors that occur during a DPC operation that cannot be reported via an I/O instruction condition code. After the processor has accepted the interrupt request, the device resets the ISB to 0.

The bits in the ISB have the following meanings:

Bit 0 — *Device-dependent status available.* This bit, when set to 1, indicates that additional status information is available from the device. The information content and method of reading this status are described in the individual device publications.

Bit 1 — *Delayed command reject.* This bit is set to 1 if the device cannot execute the command specified in the IDCB due to an incorrect parameter in the IDCB, or the device cannot execute the command due to its present state. For example, (1) the IDCB specifies an incorrect function/modifier combination, or (2) the device is temporarily not ready. The operation in progress is terminated, and interrupt condition code 2 or 6 is reported. Command reject is set in the ISB only if the device cannot report an I/O instruction condition code for the condition.

Bits 2–7 — *Device-dependent.*

I/O Interrupt Condition Codes

The condition code reported by the adapter at interrupt acceptance defines the type of interrupt, as follows:

Condition code value	Meaning
0	Controller-end interrupt*
1	Not reported
2	Exception interrupt
3	Device-end interrupt
4	Attention interrupt
5	Not reported
6	Attention and exception interrupt
7	Attention and device-end interrupt

* The controller is the adapter card control-logic circuitry.

Adapter Status Information

Adapter Status Word

The adapter status word is transferred from the adapter to the Series/1, and is stored in the second word of the IDCB when a Read Adapter Status command is executed. Definitions of the bits in the status word are:

Bit	Meaning
0	*Local-diagnostic mode.* The adapter is in local diagnostic mode as a result of executing a Set Diagnostic Mode command, with IDCB bit 16 equal to 0. Refer to "Adapter-Directed Commands" in this chapter for additional information.
1	*External-diagnostic mode.* The adapter is in external-diagnostic mode as a result of executing a Set Diagnostic Mode command, with IDCB bit 16 equal to 1. Refer to "Adapter-Directed Commands" in this chapter for additional information.
2	*Output parity error.* A parity error was detected on the channel data bus during a device-directed output operation, and condition code 5 (interface data check) was returned by the addressed device.
3	*Input parity error.* A parity error was detected during a device-directed input operation with condition code 7 (satisfactory) returned by the addressed device and condition code 5 (interface data check) set by the processor.
4	*Parity option selected.* This bit equals 1 when the parity-option jumper is installed on the adapter card. The attached devices check for parity on data bus-out and generate parity on data bus-in. This bit equals 0 when the parity-option jumper is not installed. The attached devices do not check or generate parity on the data buses; however, the adapter checks and generates parity for the channel data bus.
5	*Eight device addresses.* This bit equals 1 when the adapter is jumpered for an eight-device configuration.
6	*Four device addresses.* This bit equals 1 when the device is jumpered for a four-device configuration.
5 and 6	*Sixteen device addresses.* When bits 5 and 6 are equal to 0's, the adapter is jumpered for a 16-device configuration.
7	*Diagnostic interrupt masking.* This bit equals 1 when the diagnostic-interrupt-mask jumper is installed on the adapter card. Interrupts from the attached devices are masked during external-diagnostic mode.
8–15	*Not reported.* Always 0's.

Device Status Word

A device status word is transferred from the attached devices to the Series/1, and is stored in the second word of the IDCB when the device-directed Read Status command is executed. The device status word is device-dependent. Refer to the documentation provided with the device for definitions of bits in the device status word.

Status After Resets

The effects of the various reset conditions on the adapter functions are indicated in the following chart:

	Reset		
Condition	Diagnostic mode	Diagnostic register	Status register
Power-on reset	X	X	X
System reset	X	X	X
Halt-I/O command or machine check	X	X	X

Chapter 9. Two-Channel Switch Feature for 4959 I/O Expansion Unit

Description

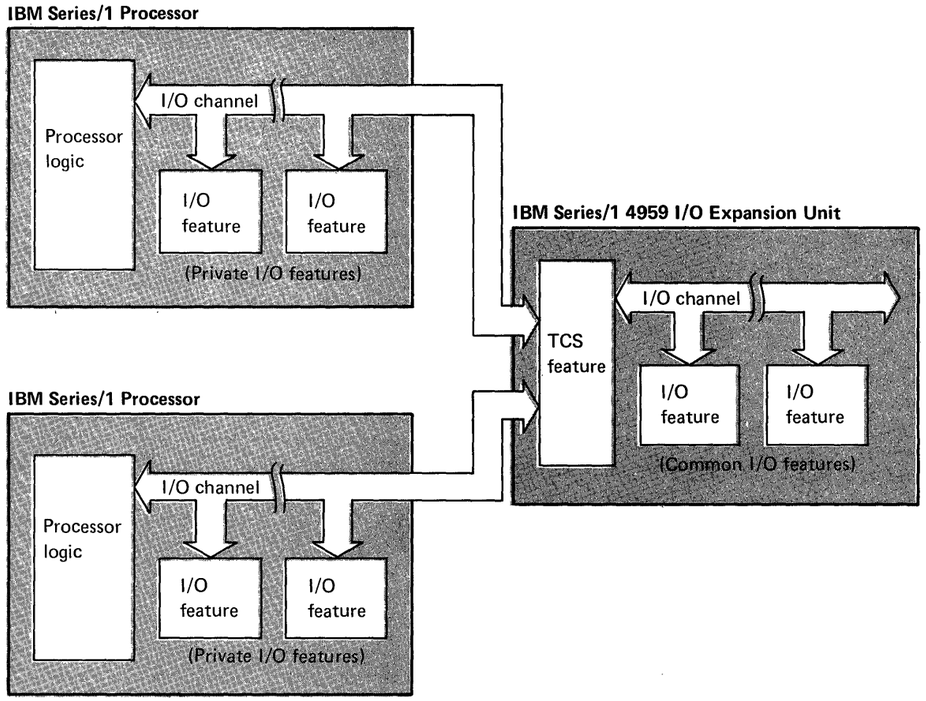
The Two-Channel Switch (TCS) feature, available as an optional feature in the 4959 I/O expansion unit, functions as an electronic switch and permits the attachment of a common set of I/O devices to two IBM Series/1 processors. At any given time, the TCS is logically connecting the common I/O devices to the I/O channel of one of the processors.

The TCS feature is designed to support a primary/backup type of operation. A processor-controlled timer in the TCS monitors the operation of the primary processor. If a time-out occurs, the TCS notifies the backup processor that a switchover is allowed, and the backup processor can assume control of the common I/O. The TCS requires manual intervention to allow switchover back to the primary processor.

The TCS feature is packaged on one four-wide, six-high, printed-circuit card, and must reside in the A-socket position of the 4959 I/O expansion unit that contains the common I/O devices. A TCS operator's console is mounted on the front of the 4959 unit.

It is necessary that the TCS feature and common I/O devices appear at the end of the I/O channel of each processor. This is to ensure that poll propagation for each processor's private I/O features is maintained when the processor is not logically connected to the common I/O via the TCS. A channel repower card should be used at the end of each processor's private I/O card file, but this is not always a requirement. Refer to "Channel Repower Feature" in the appropriate Series/1 processor theory diagrams manual for a description of the channel repower card. The channel repower card provides isolation between the outboard (common I/O) devices and inboard (private I/O) devices when the 4959 I/O expansion unit containing the common I/O is powered down.

The TCS feature provides contacts for user-connection to an external alarm device to indicate a processor-failure condition. The alarm device is supplied by the user.



Data Flow

The Two-Channel Switch feature is physically cabled to two Series/1 channels. Through either program or manual control, it selects and redrives one of the two channels for electrical connection to a set of common I/O devices. Once selection is made, the TCS is transparent to the processor and common I/O devices.

For descriptive purposes, the TCS can be divided into two functional units: the switch-control logic and the switch-and-repower matrix.

Switch Control Logic (A)

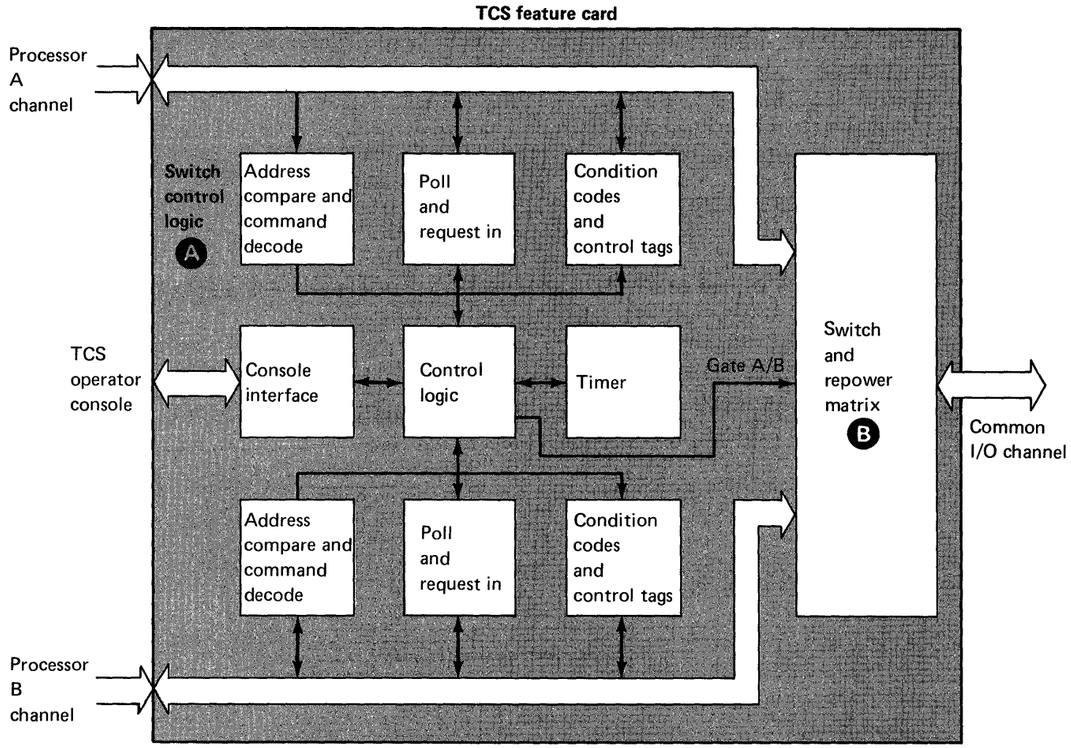
The switch-control logic determines which processor channel is connected to the common I/O devices. The switch-control logic of the TCS appears as an addressable device on each of the processor channels, and performs the following functions:

- Address compare—Two sets of address compare logic, one for each processor channel input to the TCS card, allow addressing of the TCS feature by either processor.
- Command decode—Two sets of command-decode logic, one for each processor channel, decode the commands sent to the TCS card.
- Channel tag sequence control—Two sets of tag-sequence control logic, one for each processor channel, decode and control the channel operations to and from the TCS card.
- Status and condition code generation—Two sets of status and condition-code logic, one for each processor channel, generate the status and condition-code input to the channels.
- Interrupt—Two sets of interrupt logic, one for each processor channel, control interrupt presentation to the channels.
- Timer control and time-out—A single timer on the TCS card is set and reset by the processor that is connected to the common I/O. This timer provides warning and time-out conditions, via interrupt presentation, to the processors.
- Path determination—The path determination logic selects the processor channel that is gated through the TCS to the common I/O, and determines which processor has control of the operations monitor.

Switch and Repower Matrix (B)

The switch-and-repower matrix logic of the TCS is controlled by the switch-control logic, and performs the following functions:

- Channel switch—The switch logic electrically connects the selected processor channel to the common I/O channel.
- Channel repower—The channel-repower logic provides channel repower.
- Channel gating—The switch-and-repower logic generates the directional gating signals for the bidirectional channel lines.

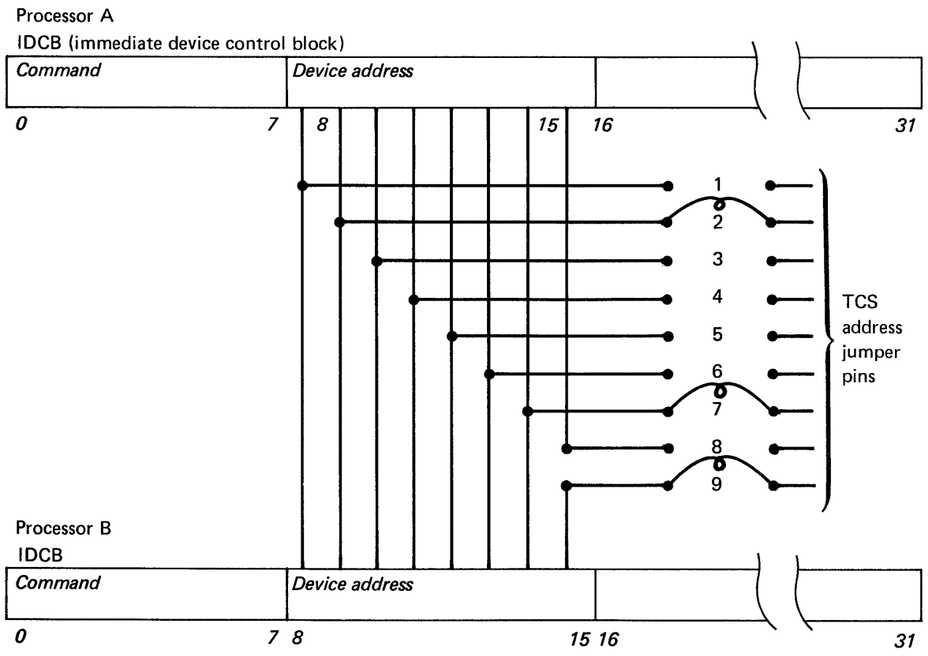


Addressing

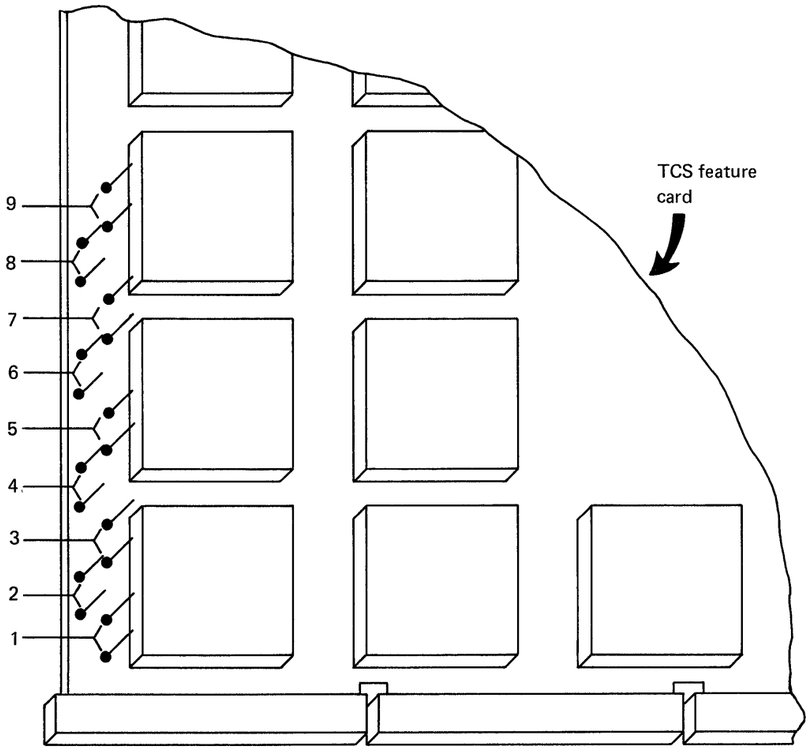
The TCS feature appears as an addressable device on the I/O channels of both processors. Nine pairs of address jumper pins, located on the TCS card, allow the user to specify the device addresses for both channel inputs. The address of the TCS can be in the range of 0–255, and can be the same to each processor or offset by 1.

Address jumper pins 1–7 correspond to the first seven bits of the device address field (bits 8–14 of the IDCB) of both processors. Jumper pin 8 corresponds to device address bit 15 of processor A, and jumper pin 9 corresponds to device address bit 15 of processor B.

In the following example, the TCS responds to address hex 42 from processor A, and to address hex 43 from processor B. If the jumper is removed from pin 9, the TCS responds to address hex 42 from either processor.



Device address jumper-pin locations



Operations Monitor

The operations monitor is a timer facility contained on the TCS feature card. The operations monitor provides the primary/backup capability of the TCS feature. In a typical application, the primary processor controls the timer. It starts the timer and responds to interrupts from the operations monitor to keep the timer from timing out. If a hardware or programming malfunction in the controlling (primary) processor allows the operations monitor to time out, the other (backup) processor is notified of this condition via an attention interrupt, and it can assume control of the common I/O devices.

The operations monitor provides two timing intervals:

- *Initial period*. This is the time interval from the starting (or reset) point to the warning point. An attention (warning) interrupt is posted to the controlling processor at this warning point.
- *Warning period*. This is the time from the warning interrupt to the point at which the operations monitor times out. An exception interrupt is posted to the controlling processor, and an attention interrupt is posted to the other processor, indicating that the time-out occurred.

The operations monitor timer is started by a Start Operations Monitor command issued by the controlling processor. Once started, the operations monitor cannot be stopped unless (1) it times out or stops in test mode, (2) a system reset occurs on the controlling processor, or (3) operator intervention occurs on the TCS console. At the end of the initial period, an attention interrupt, with the operations monitor warning bit (bit 4) set in the interrupt information byte (IIB), is issued to the controlling processor. Before the operations monitor reaches the end of the second timing period (warning period), the controlling processor must issue a Reset Operations Monitor command to restart the timer. If the timer is not reset and is allowed to time out, (1) an exception interrupt is presented to the controlling processor, with TCS status bit 5 (operations monitor time-out incurred) set on, and (2) an attention interrupt is presented to the other processor, with TCS status bit 2 (operations monitor time-out) and IIB bit 2 (connect go-ahead) set on.

Operations monitor commands are explained under "Commands" in this chapter.

Timing Jumper Options

Timing options for the timer initial period (TIP) and the timer warning period (TW) are selected by jumper options on the TCS card.

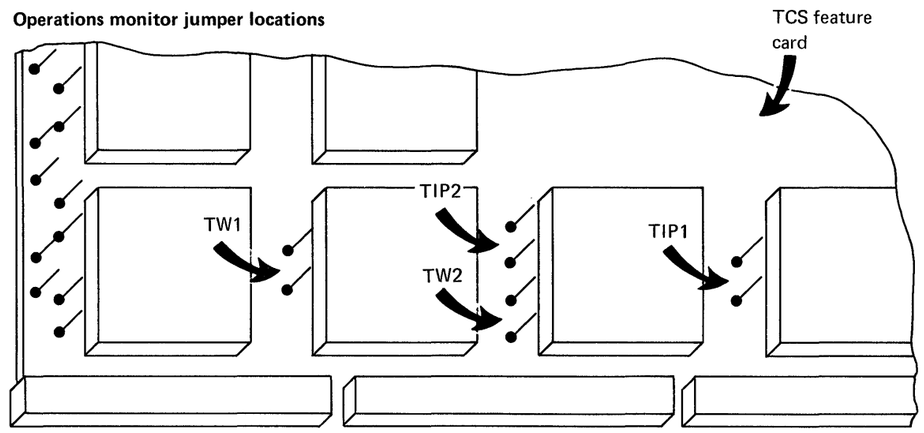
- Initial period (TIP jumpers)

	TIP Jumper 1	TIP Jumper 2
125 milliseconds	on	on
1 second	on	off
8 seconds	off	on
16 seconds	off	off

- Warning period (TW jumpers)

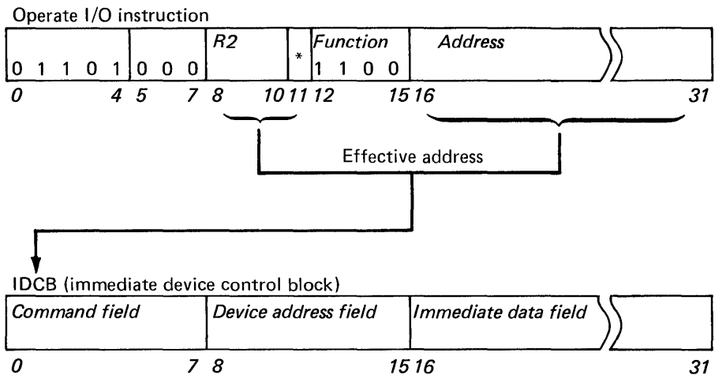
	TW Jumper 1	TW Jumper 2
0 seconds	on	on
125 milliseconds	off	on
1 second	off	off

Operations monitor jumper locations



Program Control

Program control of the TCS feature is accomplished through execution of Operate I/O instructions by the processors.



*Indirect address bit

The Operate I/O instruction generates an effective address that points to a main storage location containing an immediate device control block (IDCB). This IDCB contains a command field, a device address field, and an immediate data field.

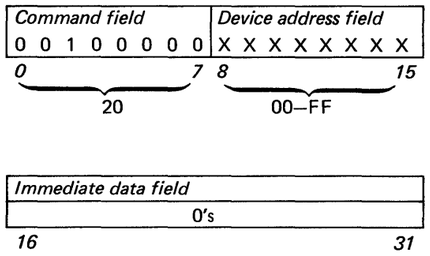
The TCS feature is a unique device in that it attaches directly to two IBM Series/1 processor channels and can accept commands from, and communicate with, either processor. The ability of the TCS to accept commands from the processors, and the types of interrupts, condition codes, and status returned to the processors are dependent on the immediate state of the TCS feature and the processors. For example, condition codes and status returned to the processors for certain TCS commands differ, depending on whether the processor issuing the command is the controlling or the backup processor.

Commands

The TCS command functions, hexadecimal values, and command decodes are given in the following table:

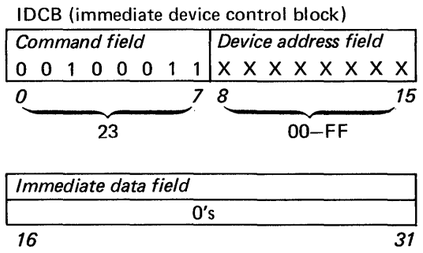
Function	Hex	Command decode
Read Status	20	Read Device ID
	23	Read Status Word
Write	50	Console Acknowledge
	53	Reserve
Control	60	Prepare
	63	Reset and Connect
	66	Start Operation Monitor
	6C	Reset Operation Monitor
	6F	Device Reset
	F0	Halt I/O

Read Device ID



The Read Device ID command transfers the device ID to the immediate data field of the IDCB of the issuing processor. The device ID of the TCS feature is hex 0030. The TCS can only report condition code 5 (interface data check) or condition code 7 (satisfactory) to this command. Condition code 1 (busy) is not reported. If condition code 5 is reported, the command is not executed.

Read Status Word



The Read Status Word command transfers the appropriate TCS device status word to the immediate data field of the IDCB of the processor issuing this command.

The 16 bits of the device status word have the following meanings:

Bit 0 — *Common I/O connected (CIO).* This bit, when set to 1, indicates that the common I/O channel and operations monitor timer facility are connected to the processor issuing this command. This bit may be changed by operator intervention on the TCS console, or by execution of a Reset and Connect command by the other processor.

Bit 1 — *Control mode in effect.* This bit, when set to 1, indicates that the TCS is in manual control mode. When set to 0, it indicates that the TCS is in automatic control mode. This bit may be changed by operator intervention on the TCS console.

Bit 2 — *Operations monitor time-out.* This bit, when set to 1, indicates that an operations monitor time-out has been incurred by the other processor. This bit is turned off by a system reset on the other processor, but it is not affected by a Halt I/O or Device Reset command issued by that processor. It is also turned off by operator intervention on the TCS console, and is held off in manual control mode.

Bit 3 *Reserve*. This bit, when set to 1, indicates that the other processor has executed a Reserve command. This bit is turned off by a system reset, or by a Halt I/O, Device Reset, or Reset and Connect command executed by the other processor. It cannot be reset by the controlling processor. It is also turned off by operator intervention on the TCS console, and is held off in manual control mode.

Bit 4 *Operations monitor run*. This bit, when set to 1, indicates that the operations monitor is running. It is turned off when the operations monitor is not running.

Bit 5 *Operations monitor time-out incurred*. This bit, when set to 1, indicates that a time-out occurred in the operations monitor while the operations monitor was connected to the processor issuing this Read Status Word command. It is reset by a system reset on the corresponding processor. It is turned off by operator intervention on the TCS console, and held off while in manual control mode. It is not affected by a Halt I/O or Device Reset command from the issuing processor.

Bit 6 *Not used*. Presented as 0.

Bit 7 *Not used*. Presented as 0.

Bit 8 *Common I/O connection alert*. Refer to bit 9.

Bit 9 *Control mode alert*. Bits 8 and 9, when set to 1's, indicate that the switch settings on the TCS console differ from the respective common I/O connection or control mode in effect, as signified by bits 0 and 1 of this status word. These bits are set by operator release of the Attn pushbutton on the TCS console. They are reset by (1) a system reset, (2) execution of a Read Status Word, Halt I/O, or Device Reset command from the issuing processor, or (3) manual operation of the Reset pushbutton on the TCS console.

Bit 10 *Initiate initial program load (IIPL) blocked*. This bit, when set to 1, indicates that the IIPL blocked jumper for this processor is installed on the TCS card. This means that this processor must receive its processor-initiated IPL from a private I/O device inboard of the TCS.

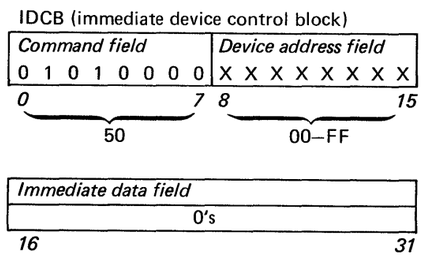
Bit 11 *Polarity*. This bit indicates the side (A or B) of the TCS feature to which this processor is connected. This bit, when set to 1, indicates connection to the A-side of the TCS feature.

Bits 12, 13 *Operations monitor initial period (TIP)*. These two bits reflect the jumper options for the TIP timing period. Bits 12 and 13, when set to 1's, indicate that TIP jumpers 1 and 2, respectively, are installed.

Bits 14, 15 *Operations monitor warning period (TW)*. These two bits reflect the jumper options for the TW timing period. Bits 14 and 15, when set to 1's, indicate that TW jumpers 1 and 2, respectively, are installed.

The Read Status Word command is not executed if the TCS has an interrupt pending (condition code 1, busy), or if an interface data check (condition code 5) occurs.

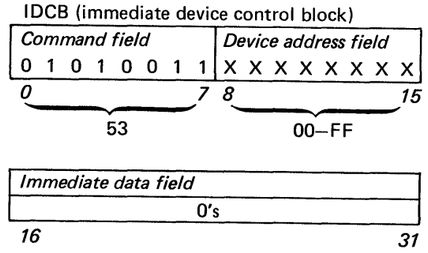
Console Acknowledge



The Console Acknowledge command turns on the acknowledge (Ack A/B) indicator (on the TCS console) corresponding to the processor issuing this command. If the light was previously on, it remains on. The Ack A/B indicator is turned off by operator action on the TCS console, a system reset, or execution of a Device Reset or Halt I/O command by the corresponding processor. The IDCB data word is not used and should be 0.

The TCS can report condition code 1 (busy), condition code 5 (interface data check), or condition code 7 (satisfactory) to this command. Condition code 1 is reported only if the TCS has an interrupt pending. The command is not executed if condition code 1 or 5 is reported.

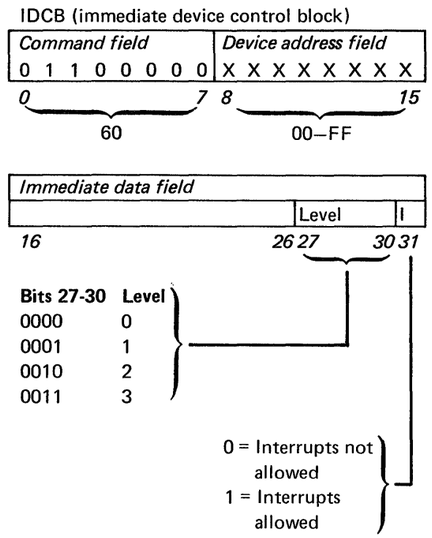
Reserve



The Reserve command causes bit 3 (reserve) of the TCS status word of the other processor to be set to 1. An attention interrupt is posted to the other processor, with bit 3 (ready) set to 1 in the interrupt information byte (IIB). No interrupts are posted to the issuing processor as a result of this command. If a Prepare command has not been executed by the other processor, the reserve bit is set, but the attention interrupt is not presented, and remains pending in the TCS. The IDCB data word is not used and should be 0.

Condition code 1 (busy) is reported if the TCS is busy or has an interrupt pending. Condition code 3 (command reject) is reported if the TCS is in manual control mode, or if the TCS is in automatic control mode and the common I/O channel is already connected to the processor issuing this command. Condition code 4 (intervention required) is reported if the TCS is in automatic control mode, the processor issuing this command is not connected to the common I/O channel, and the operations monitor has timed out. Condition code 5 (interface data check) is reported if a parity error occurs on the data bus of the issuing processor. The command is not executed if condition code 1, 3, 4, or 5 is reported.

Prepare

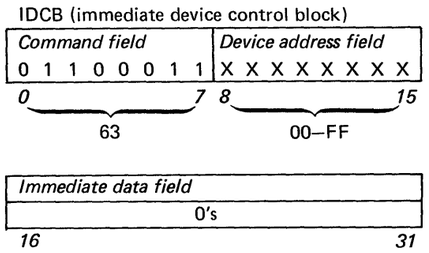


The Prepare command loads the interrupt level and I-bit from the immediate data field of the IDCB into the TCS prepare register corresponding to the issuing processor. The I-bit (bit 31) controls the capability of the TCS to present interrupts to the processor. The interrupt level (bits 27–30) is the level (0–3) on which the TCS can present interrupts.

The Prepare command does not cause an interrupt to the issuing processor; however, an interrupt may result if an interrupt pending condition exists in the TCS.

Condition code 5 (interface data check) or condition code 7 (satisfactory) can be reported for this command. If condition code 5 is reported, the command is not executed.

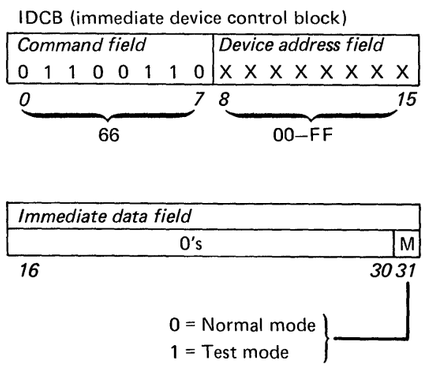
Reset and Connect



The Reset and Connect command causes a system reset to the common I/O channel, and connection of the common I/O channel to the processor issuing this command. This command is executed only if (1) the TCS is in automatic mode, (2) the processor issuing this command is not already connected to the common I/O channel, and (3) an operations monitor time-out has been posted by the other processor. The reset does not affect the private I/O devices inboard of the TCS, or the time-out status of the TCS operations monitor. The IDCB data word is not used and should be 0.

Condition code 1 (busy) is reported if the TCS is busy or has an interrupt pending. Condition code 3 (command reject) is reported if (1) the TCS is in manual control mode, (2) the common I/O is already connected to the processor issuing this command, or (3) the TCS is in automatic mode, the common I/O is not connected to the processor issuing this command, and an operations monitor time-out has not been posted by the other processor. Condition code 5 (interface data check) is posted if a parity error is detected on the data bus of the issuing processor. Condition code 7 (satisfactory) is reported for successful execution of the command. The command is not executed if condition code 1, 3, or 5 is reported by the TCS.

Start Operations Monitor



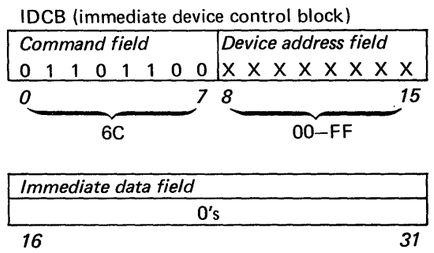
The Start Operations Monitor command, when issued by the processor connected to the common I/O channel, starts the operations monitor. Once started, the operations monitor cannot be stopped unless (1) it times out or stops in test mode, (2) a system reset occurs on the controlling processor, or (3) operator intervention on the TCS console occurs.

The operations monitor has two timing periods, the initial period and the warning period. At the end of the initial period, an attention interrupt with bit 4 (operations monitor warning) set on in the interrupt information byte (IIB) is issued to the controlling processor. Before the operations monitor reaches the end of the second timing period (warning period), the controlling processor must issue a Reset Operations Monitor command to reset and restart the operations monitor timer. If the timer is not restarted and allowed to time out, (1) an exception interrupt is presented to the controlling processor, with TCS status bit 5 (operations monitor time-out incurred) set on, and (2) an attention interrupt is presented to the other processor, with TCS status bit 2 (operations monitor time-out) and interrupt information byte bit 2 (connect go-ahead) set on.

Only bit 31 of the IDCB data word is used by this command. If bit 31 is 0, the operations monitor operates in normal mode, as described previously. If bit 31 is 1, the operations monitor operates in test mode. In test mode, the operations monitor does not post the time-out condition at the end of the warning period. Instead, a device-end interrupt is reported to the processor issuing the test mode command and the attention interrupt is not posted to the other processor.

Condition code 1 (busy) is reported for this command if the TCS is busy or has an interrupt pending. Condition code 3 (command reject) is reported if the TCS (1) is in manual control mode, or (2) is in automatic control mode and the processor issuing this command is not the connected processor. Condition code 4 (intervention required) is reported if (1) the TCS is in automatic control mode, (2) the processor issuing this command is the connected processor, and (3) an operations monitor time-out exists. Condition code 5 (interface data check) is reported if a parity error is detected on the data bus of the issuing processor. Condition code 7 (satisfactory) is reported for successful execution of this command. The command is not executed if condition code 1, 3, 4, or 5 is reported.

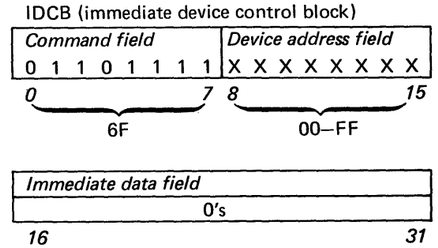
Reset Operations Monitor



The Reset Operations Monitor command causes the operations monitor to reset to the starting point. The operations monitor does not stop, but continues running from the reset/starting point. If the operations monitor has timed out, it cannot be restarted by this command. The IDCB data word is not used or checked for parity. If an operations monitor warning interrupt (bit 4 of the IIB) is pending, it is reset.

Only condition code 7 (satisfactory) is reported by the TCS for this command.

Device Reset



The Device Reset command resets the following functions of the TCS attachment side corresponding to the processor issuing this command:

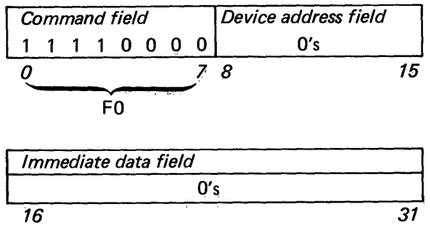
1. Pending interrupts
2. Ack A/B indicator on the TCS console
3. Bit 8 (common I/O connection alert) of the TCS status word
4. Bit 9 (control mode alert) of the TCS status word

The operations monitor is reset to the starting point, and continues to run if it had previously been started. Bit 3 (reserve) of the status word corresponding to the other processor is reset. The prepare register of the issuing processor is not reset. The IDCB data word is not used and is not checked for parity.

Only condition code 7 (satisfactory) is reported by the TCS for this command.

Halt I/O

IDCB (immediate device control block)



The Halt I/O command is a channel directed command that causes a halt of all I/O activity on the I/O channel of the issuing processor. The TCS attachment side corresponding to the issuing processor is reset. The prepare register of the TCS side corresponding to the issuing processor is not reset. The operations monitor is not affected, and it continues to run if it was previously started. If the issuing processor is the connected processor, the common I/O devices are also reset.

I/O Instruction Condition Codes

The TCS returns a condition code to the processor issuing the I/O instruction. This condition code reflects the ability of the TCS to execute the specified command. The meanings of the I/O instruction condition codes are:

CC=0 *Device not attached*. Reported by the channel if the TCS feature is not attached to the system.

CC=1 *Busy*. Reported by the TCS to the issuing processor if (1) the issuing processor is the connected processor, but the TCS is busy or has an interrupt pending, or (2) the issuing processor is not the connected processor, but the TCS has an attention interrupt pending to this processor.

CC=2 *Not reported*.

CC=3 *Command reject*. Reported by the TCS to the issuing processor if (1) the command is not a valid TCS command, (2) the processor/common I/O connection is improper in relation to the command, or (3) the TCS is not in the proper state to execute the command.

CC=4 *Intervention required*. Reported by the TCS to the issuing processor when operator intervention or IPL is required to reset a time-out condition.

CC=5 *Interface data check*. Reported by the TCS or channel when incorrect parity is detected on the data bus of the issuing processor.

CC=6 *Not reported*.

CC=7 *Satisfactory*. Reported by the TCS to the issuing processor when the TCS accepts the command.

		I/O instruction condition code values (CC=)							
Hex	Command	0	1	2	3	4	5	6	7
20	Read Device ID	X					X		X
23	Read Status Word	X	X				X		X
50	Console Acknowledge	X	X				X		X
53	Reserve	X	X		X	X	X		X
60	Prepare	X					X		X
63	Reset and Connect	X	X		X		X		X
66	Start Operations Monitor	X	X		X	X	X		X
6C	Reset Operations Monitor	X							X
6F	Device Reset	X							X

The condition code is determined from the value of the even, carry, and overflow bit positions of the level status register (LSR) in the processor issuing the command.

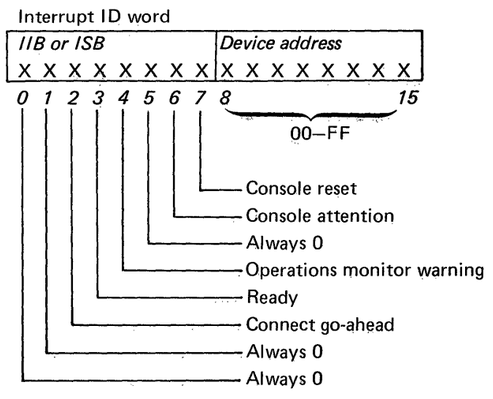
	LSR bits			
CC value	0 Even	1 Carry	2 Overflow	Description
0	0	0	0	Device not attached
1	0	0	1	Busy
2	0	1	0	Not reported
3	0	1	1	Command reject
4	1	0	0	Intervention required
5	1	0	1	Interface data check
6	1	1	0	Not reported
7	1	1	1	Satisfactory

I/O Interrupts

The TCS attachment can initiate I/O interrupts to the processors if the I-bit in the corresponding processor TCS prepare register has been set to 1 by a Prepare command. The interrupts initiated by the TCS attachment are:

- *Exception*. An operations monitor time-out has occurred while the operations monitor was operating in normal mode.
- *Device-end*. An operations monitor time-out has occurred while the operations monitor was operating in test mode.
- *Attention*. An event asynchronous to the program of the interrupted processor has occurred.
- *Attention and exception*. An event asynchronous to the program of the interrupted processor has occurred and an operations monitor time-out in normal mode exists.
- *Attention and device-end*. An event asynchronous to the program of the interrupted processor has occurred and an operations monitor time-out in test mode exists.

Additional information pertaining to specific interrupts is contained in either the interrupt information byte (IIB) or the interrupt status byte (ISB) of the interrupt ID word. The IIB and ISB have identical meanings in the TCS attachment. This information is presented in the interrupt information word when an interrupt with an interrupt condition code of 4, 6, or 7 is accepted by the processor. The interrupt ID word has the following format:



Bit 0 *Always presented as 0.*

Bit 1 *Always presented as 0.*

Bit 2 *Connect go-ahead*. This bit, when on, indicates that the other processor has incurred a time-out of the operations monitor. This bit reflects the setting of bit 2 (operations monitor time-out) in the TCS status word. This interrupt is reset when (1) the interrupt is accepted and (2) bit 2 (operations monitor time-out) of the TCS status word is reset by a system reset on the other processor or by operator intervention on the TCS console.

Bit 3 *Ready*. This bit, when on, indicates that the other processor has executed a Reserve command. This bit reflects bit 3 (reserve) of the TCS status word.

Bit 4 *Operations monitor warning*. This bit, when on, indicates that the operations monitor has reached the warning point (end of initial period).

Bit 5 *Always presented as 0.*

Bit 6 *Console attention*. This bit, when on, indicates that the operator has pressed and released the Attn pushbutton on the TCS console.

Bit 7 *Console reset*. This bit, when on, indicates that the operator has pressed and released the Reset pushbutton on the TCS console.

I/O Interrupt Condition Codes

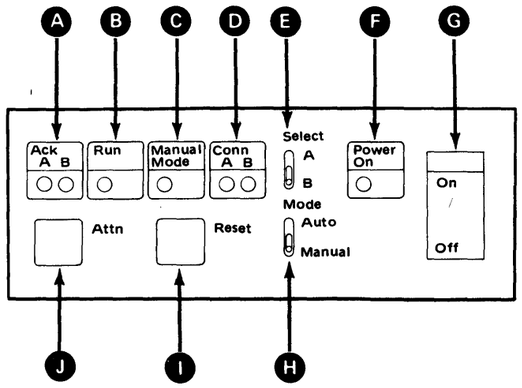
The specific type of interrupt can be determined from the interrupt condition code sent to the processor at interrupt-accept time. These condition codes are:

CC=2 Exception interrupt
CC=3 Device-end interrupt
CC=4 Attention interrupt
CC=6 Attention and exception interrupt
CC=7 Attention and device-end interrupt

TCS Operator Console

The TCS operator console is mounted on the front panel of the 4959 I/O expansion unit that contains the TCS feature card. The console allows the operator to:

- Select the manual or automatic control mode of operation.
- Select the TCS A- or B-side and its associated Series/1 processor that is to be connected to the common I/O.
- Interrupt and notify the processors that operator intervention is occurring.
- Manually switch the common I/O from one processor to another.
- Reset time-out conditions.
- Assist in returning the system to normal operation after manual intervention or a time-out has occurred.



The controls and indicators on the TCS console provide the following functions:

Ack A/B (A)

The Ack A or Ack B indicator is turned on by execution of a Console Acknowledge command by the corresponding processor on the A- or B-side of the TCS. The indicator is turned off by a system reset, or a Device Reset or Halt I/O command issued by the corresponding processor. Both indicators are turned off when the Attn or the Reset pushbutton is pressed.

Run (B)

When the operations monitor is running, this indicator is on. When the operations monitor is stopped, reset, or timed out, this indicator is off.

Manual Mode (C)

When manual mode is in effect, this indicator is on. When automatic (processor) mode is in effect, this indicator is off.

Conn A/B (D)

The appropriate Conn A/B indicator is turned on when the corresponding processor on the A- or B-side of the TCS is logically connected to the common I/O and operations monitor. If one of the indicators is blinking, an operations monitor time-out has occurred on the corresponding processor. Pressing the Reset pushbutton, while in automatic mode, turns off a blinking indicator, but has no effect on an indicator that is on. Pressing the Reset pushbutton, while in manual mode, turns on the Conn A/B indicator corresponding to the setting of the Select A/B switch.

Select (E)

When this switch is set to A, the A-side of the TCS is selected; when it is set to B, the B-side of the TCS is selected. No action is generated by this switch until the Reset or Attn pushbutton is pressed. During a power-up sequence, the initial selection is determined by this switch setting.

Power On (F)

When the correct voltage levels are available in the 4959 I/O expansion unit, this indicator is turned on. If the voltage levels are not correct, this indicator is off.

Power On/Off (G)

When this switch is set to On, power is applied to the 4959 I/O expansion unit card file. When all power levels are up, the Power On indicator is turned on. When this switch is set to Off, power is removed from the 4959 I/O expansion unit card file and the Power On indicator is turned off.

Mode (H)

When this switch is set to Auto, the automatic (processor control) mode is selected. When this switch is set to Manual, the manual mode is selected. No action is generated by this switch until the Reset or Attn pushbutton is pressed.

Reset (I)

When this pushbutton is pressed, the TCS attachment sides for both processors are placed in operator intervention mode. The Ack A/B indicators are turned off. The operations monitor timer is stopped and held in a reset state. If the operations monitor has previously timed out, the time-out condition is reset. The reserve bit in the TCS status word is reset. Additional actions occur, depending on the settings of the Mode and Select switches, as indicated in the following table:

Conditions existing when Reset key activated				Conditions after Reset key activated	
Conn A/B indicator	Select switch	Manual Mode indicator	Mode switch	Conn A/B indicator	Manual Mode indicator
A	A or B	On or off	Auto	A	Off
B	A or B	On or off	Auto	B	Off
A	A	On or off	Manual	A	On
B	B	On or off	Manual	B	On
A	B	On or off	Manual	B	On
B	A	On or off	Manual	A	On

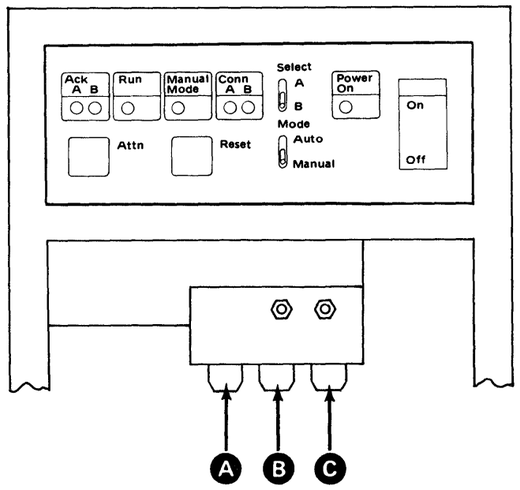
When the Reset pushbutton is released, the TCS exits operator intervention mode, and an attention interrupt is posted to both processors, with bit 7 (console reset) set on in the IIB. The Reset and Attn pushbuttons are not interlocked, and unpredictable results may occur if they are operated simultaneously. Pressing the Reset pushbutton while the common I/O is operational may cause I/O checks; therefore, the Attn pushbutton should be used to alert the programs of impending operator intervention prior to pressing the Reset pushbutton.

Attn (J)

When this pushbutton is pressed, the Ack A/B indicators are turned off. When it is released, an attention interrupt is posted to both processors with TCS status word bits 8 and 9 set to indicate the status of the Select and Mode switches if these switches differ from the common I/O connection or control mode already in effect. This pushbutton is used with the Select and Mode switches to (1) notify or alert the program to impending operator action in manual control mode, or (2) to request action from the programs in automatic control mode.

TCS Operator Console Card

The TCS operator console card contains the switches and indicators described in "TCS Operator Console" in this chapter. The card is mounted on a hinged gate on the right side of the 4959 if the TCS feature is installed.

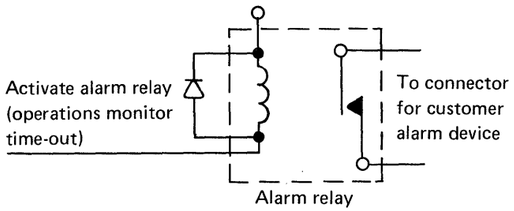


The console card has three connectors on the lower end for connecting the following signal cables:

- (A) *Power-on reset A*. This connector receives the power-on reset signal from the Series/1 processor that is connected to the TCS A-side. If this line becomes inactive, indicating that the processor has powered down, the TCS degates initiate IPL (HPL) and system reset from that processor.
- (B) *Power-on reset B*. This connector receives the power-on reset signal from the Series/1 processor that is connected to the TCS B-side. If this line becomes inactive, indicating that the processor has powered down, the TCS degates initiate IPL (IIPL) and system reset from that processor.
- (C) *Customer output alarm connector*. This connector allows a customer alarm device to be connected to the customer output alarm relay located on the TCS console card.

Customer Output Alarm Relay

A reed relay on the TCS console card is provided for customer use as an alarm relay. The alarm relay is activated by an operations monitor time-out that sets bit 5 (operations monitor time-out incurred) in the TCS status word. The alarm relay can be used to control an external (customer-installed) alarm device to signal a processor failure. The alarm relay is reset by pressing the Reset pushbutton on the TCS console.



Initial Program Load

Either processor attached to the TCS can initiate an IPL from a common I/O device, provided that the IIPL blocked jumpers are not installed. Operator intervention is necessary to IPL the processors from a common I/O device. This is accomplished by placing the TCS in manual mode, setting the Select A/B switch to the desired position, and pressing the Load pushbutton on the corresponding processor console. If the other processor is also to be IPLed from a common I/O device, the operator can change the Select A/B switch to the other processor and press the Attn pushbutton to alert the first processor that the switch is being changed. The processor program responds by turning on the appropriate Ack A/B indicator. The operator can then press the Reset pushbutton to make the switchover, and then IPL the second processor.

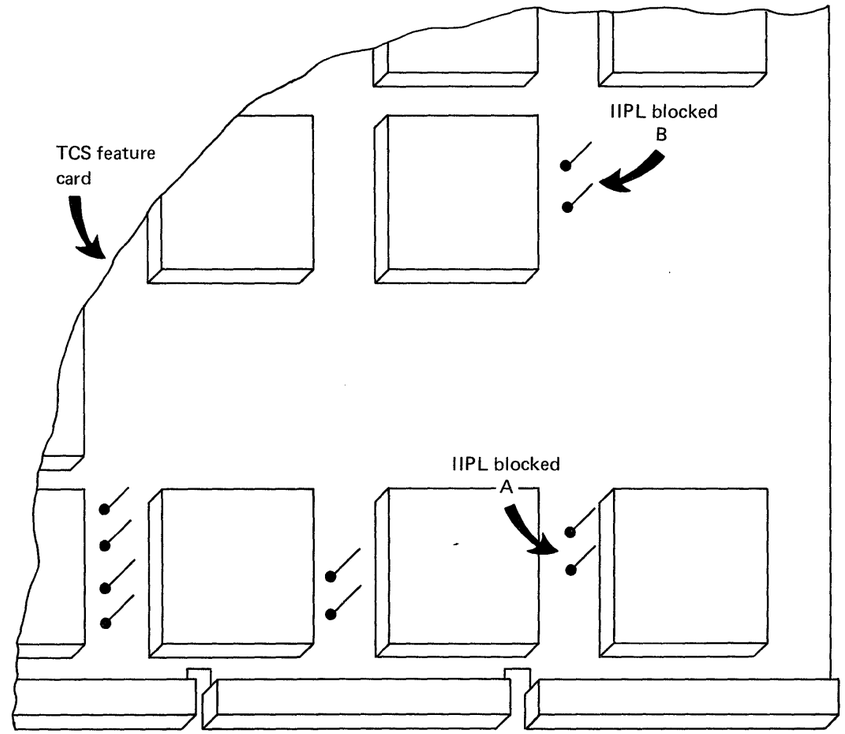
The operator can now select the processor that is to be connected to the common I/O, and then set the Mode switch to automatic mode.

IIPL Jumper Options

A jumper option is provided for each side of the TCS to block the IIPL (initiate initial program load) tag of a processor from being propagated to the common I/O devices. This jumper option allows an I/O device on the processor's private I/O channel, as well as a device on the common I/O channel, to be used for primary or alternate IPL. The status of the IIPL jumper is reflected in bit 10 of the TCS status word.

The IIPL blocked jumper, when installed, blocks the corresponding processor's IIPL tag from reaching the common I/O channel.

IIPL jumper locations



Status After Resets

The TCS feature is located in the 4959 I/O expansion unit that contains the common I/O card file, and it is subject to the reset controls of that unit. The TCS also connects to two Series/1 processor I/O channels and appears as an I/O device to each of the processors; therefore, it responds to resets issued on these channels.

The effects of the various reset conditions on the TCS are explained in the following paragraphs.

1. *Power-on resets*. A power-on reset issued from the 4959 expansion unit that contains the TCS causes both sides of the TCS to be reset. A power-on reset issued by one of the processors causes only the corresponding side of the TCS to be reset.
2. *System resets*. A system reset issued by a processor causes only the corresponding side of the TCS to be reset.
3. *Command resets*. Processor-issued commands (such as Halt I/O, Device Reset, Reset and Connect, and Reset Operations Monitor) affect only the TCS side corresponding to the issuing processor. The other side remains as it was; however, indications in its status word may change, and residual interrupts may exist.

The following table lists conditions that reset TCS controls and registers:

	Condition						
Control/register	**Power on**	**System reset**	**Halt I/O**	**Device reset**	**Reset operations monitor**	**Reset and connect**	**Read status word**
Acknowledge indicator (Ack A/B)	X	X	X	X	--	--	--
Reserve bit 3	X	X	X	X	--	X	--
Operations monitor time-out incurred	X	X	--	--	--	--	--
Connection alert and mode alert	X	X	X	X	--	--	X
Prepare register	X	X	--	--	--	--	--
Operations monitor (timer)	X[1]	X	--	X[2]	X[2]	--	--

X = reset
[1] Causes timer to stop.
[2] Resets timer to starting/reset point, but timer continues to run.

Interrupt Resets

A reset issued by one of the processors (such as a system reset, or a Halt I/O, Device Reset, or Reset Operations Monitor command) resets all pending interrupts on the corresponding TCS side. However, upon completion of the reset, two conditions that are asynchronous to the reset side of the TCS are resampled and the interrupt is reposted. These two interrupts are called persistent interrupts, and are reset only when accepted by the other processor. The following table lists the conditions that cause the TCS to reset pending interrupts:

	Condition				
Interrupt	**Power on**	**System reset**	**Halt I/O**	**Device reset**	**Reset operations monitor**
Connect go-ahead	X	X[1]	X[1]	X[1]	--
Ready	X	X[1]	X[1]	X[1]	--
Operations monitor warning	X	X	X	X	X
Device end	X	X	X	X	--
Exception	X	X	X	X	--
Console attention	X	X	X	X	--
Console reset	X	X	X	X	--

X = Reset
[1] Persistent interrupt

Chapter 10. Series/1-System/370 Channel Attachment Feature and IBM 4993 Model 1 Termination Enclosure

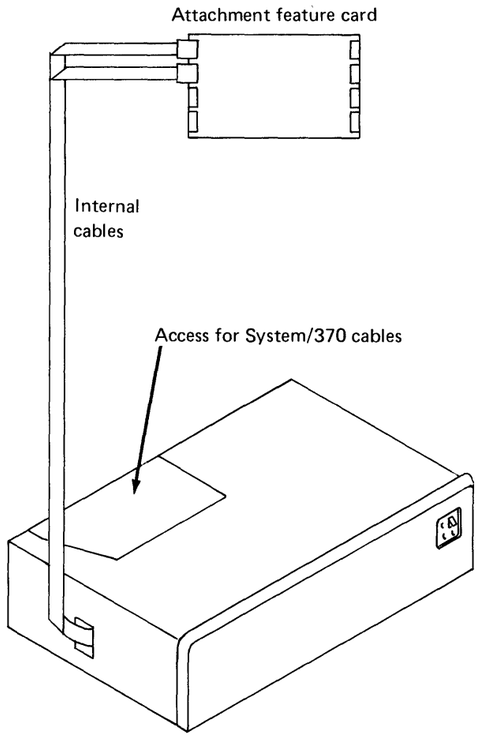
Description

The channel attachment (a feature card and the termination enclosure) provides a means for storage-to-storage communications between a Series/1 processor and any System/370 Model 135-168, or a 3031, 3032, or 3033 processor. The attachment connects to the I/O channel of both processors and responds to the limited command set defined in this chapter.

The attachment transfers data at the data rate of the slower channel up to a maximum of 300,000 bytes per second. The actual data transfer rate is affected by processor performance and software overhead of either system.

Up to eight Series/1-System/370 attachments can be connected to a single System/370 I/O channel. Any number of attachments can be installed on the Series/1 I/O channel, up to the addressing limit of the system and within physical limitations. Physical restrictions (due to 4993-1 location) limit the attachment to one 4993-1 per Series/1 4997 rack enclosure. Overall system performance (Series/1 and System/370) is a consideration when multiple attachments are installed.

The attachment feature is contained on one four-wide, six-high, printed-circuit card that can be plugged into any I/O slot of a Series/1 processor or 4959 I/O expansion unit. The 4993-1 termination enclosure must be installed concurrently with the feature card.



4993-1 termination enclosure

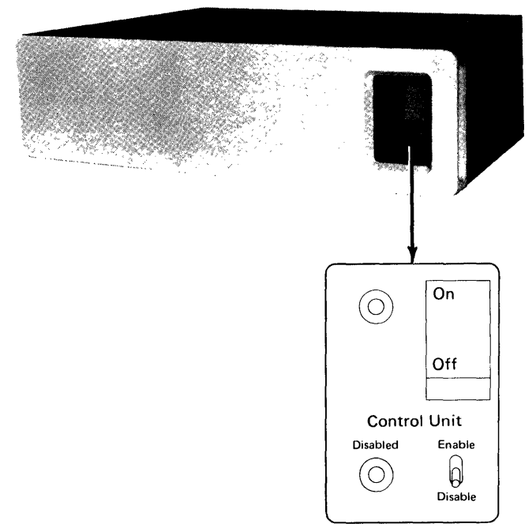
Switches and Indicators

Two switches and two LED indicators are located on the 4993-1 enclosure:

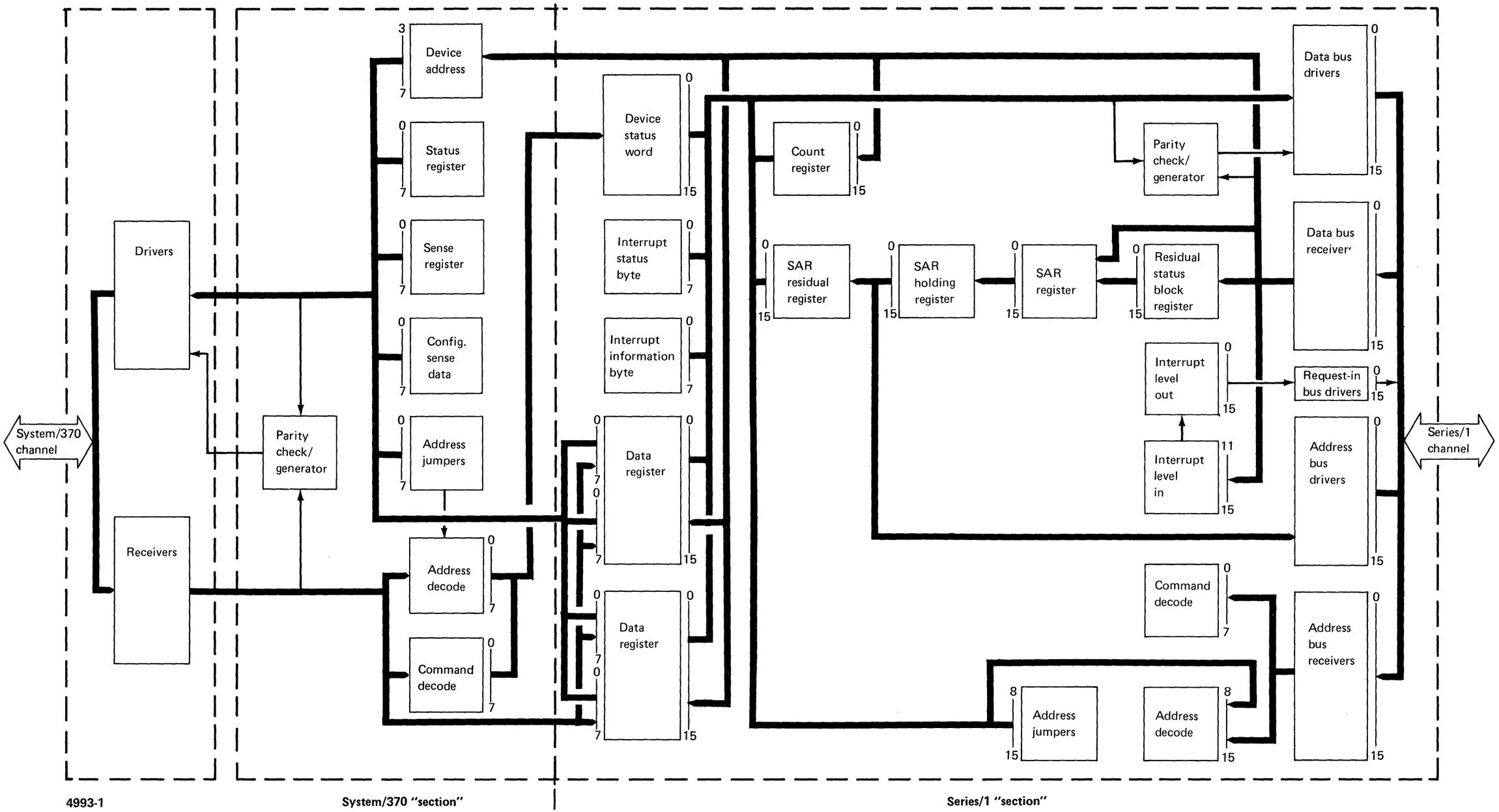
- Power On/Off switch
- Enable/Disable switch
- Power-on indicator
- Disabled indicator

The On/Off switch applies or removes incoming ac power to the 4993-1 (not to the attachment feature card). The Enable/Disable switch controls the on-line/off-line state of the attachment relative to the System/370. When the attachment is enabled (on-line), System/370 operations to the attachment can proceed in a normal manner. When the attachment is disabled (off-line), it cannot be selected by the System/370. The Disabled indicator is turned on when the attachment is in the disabled state.

The attachment must be switched off-line *before* removing power from the 4993-1, and it should be switched on-line *after* power is reapplied.



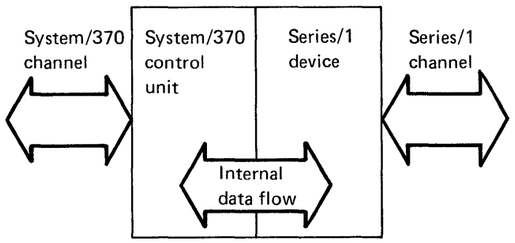
Data Flow Diagram



Series/1—System/370 channel attachment feature card

Data Flow

The Series/1-System/370 attachment may be conceptually divided into two different sections: the Series/1 section (a Series/1 I/O device) and the System/370 section (a System/370 control unit with 32 device addresses). There is a path through the attachment for transferring data between main storage of the Series/1 and main storage of the System/370.



Series/1-System/370 channel attachment feature

Series/1-System/370 Channel Attachment Feature Functional Units

Feature Card

The printed-circuit feature card contains the following logic circuits:

Sense and Status Information Registers. These registers contain information about the status of the attachment or the operation in process.

Interrupt Information and Status Registers. These registers contain information about the source of, and the reason for, an interrupt.

Interrupt Level Registers. These registers contain the current interrupt level assigned to the attachment by the Series/1 Prepare command and present this information to the Series/1 channel when requesting interrupt service.

Four-byte Data Buffer. The data being transferred between systems is stored and gated from this register under control of the attachment control logic associated with the Series/1 and System/370 channels.

Count Register. This register contains the byte count for the data transfer. The byte count is set into the register from the device control block (DCB) of the Series/1, and is decremented for each byte of data transferred. At the termination of an operation, the residual byte count can be read by a Start Cycle Steal Status command issued from the Series/1. Normal termination of a data transfer occurs when the byte count in this register equals 0.

Storage Address Register (SAR). The storage address for the Series/1 cycle-steal data transfer is loaded into the SAR register from the Series/1 DCB. This address is passed to the SAR holding register, and the SAR register is then incremented for each data transfer. The SAR holding register controls the addressing of Series/1 storage during the attachment cycle-steal operation. The SAR residual register can be read by a Start Cycle Steal Status command issued from the Series/1.

Command Decode. Two command decode circuits, one for each side of the attachment, decode commands from the associated processor channel.

Address Decode. Two address decode circuits, one for each side of the attachment, decode the address presented from the associated processor channel. Address jumper options on the attachment card must be plugged for the desired addresses.

Parity Check/Generator. Parity is checked by the attachment for data received from both processor channels. Parity is generated by the attachment before presenting data to the processor channels.

Drivers/Receivers. The driver/receiver circuits of the feature card convert the bidirectional Series/1 channel lines to/from the unidirectional attachment bus lines.

IBM 4993 Model 1 Termination Enclosure

The 4993-1 termination enclosure is a rack-mounted unit that occupies the full width of the standard Series/1 rack and is approximately 5 1/2 inches (139.7 millimeters) high. The 4993-1 contains:

System/370 Channel Cable Connectors. Four cable connectors, which are located on the rear of the unit, are provided for connecting the System/370 channel cables.

Driver/Receiver Converter Cards. Two driver/receiver cards, which are located in the 4993-1, convert the outgoing and incoming System/370 channel lines to the required voltage logic levels. If the 4993-1 is the last device on the System/370 channel string, standard System/370 channel terminators must be installed in the bus-out and tag-out receptacles.

Power Supply. A power supply, which is located in the 4993-1, supplies the power necessary for the driver/receiver cards, the Enable/Disable circuits, and the Disabled indicator.

Maintenance Test Pins. Test pins, which are located on the driver/receiver card assemblies, are provided for maintenance testing. During certain maintenance procedures, the MAPs require the checking of signal conditions on these test pins.

Power On/Off Switch. This switch, which is located on the switch panel, removes or applies incoming power to the 4993-1 (not the attachment feature card).

Power-on Indicator. This indicator, which is located on the switch panel, is turned on when the 4993-1 is powered on.

Enable/Disable switch. This switch, which is located on the switch panel, controls the on-line/off-line state of the attachment relative to the System/370. When this switch is in the Disabled position, and the Disabled indicator is on, the attachment is offline (logically disconnected from the System/370).

Disabled Indicator. This indicator, which is located on the switch panel, is turned on when the 4993-1 is off-line (Enable/Disable switch is in the Disable position).

Attachment Cables. Two flat cables, routed internally in the Series/1 rack enclosure, connect the 4993-1 to the attachment feature card.

Data Transfer Between Systems

The Series/1 section responds to Series/1 I/O commands, and operates as a cycle-steal device on the I/O channel of the Series/1. The System/370 section responds to a limited set of System/370 I/O commands, and appears to the System/370 as a control unit with 32 device addresses.

Prepare Attachment

The attachment must be on-line to the System/370 (the Enable/Disable switch on the 4993-1 is in the Enable position). The Series/1 program must prepare the attachment as follows:

1. Issue a Prepare command. This prepares the attachment to interrupt the Series/1 and assigns a specific interrupt level.
2. Issue an Enable System/370 Device Address command. This notifies the System/370 (via an interrupt) that a specific device (1 of 32) is now ready.

Transfer Data

All cycle-steal data transfer operations are initiated by the System/370. The System/370 program uses I/O commands such as Read Buffer or Write, and the Series/1 program must respond with a Start command. These System/370 commands generate an "attention" interrupt in the Series/1. The Series/1 program can then interrogate the attachment status word to identify what System/370 command has been received, and determine what type of response (read or write operation) is necessary. If the System/370 initiates a *read* operation, the Series/1 must respond with a *write* operation. The device control block (DCB) associated with the Series/1 Start command defines the appropriate read or write operation that is necessary to accomplish the data transfer. The operations are checked by the attachment to ensure a proper match; then the two systems are "connected" for the data transfer.

After the two systems are "connected," a byte of data is transferred from the storage of one system to the attachment, and then transferred to the storage of the other system. The attachment routes the data from one channel to the other channel, synchronizing itself to the channel discipline of each system. Normal termination for the data transfer occurs when the data count specified by the Series/1 DCB reaches 0. Ending status is presented to each system and the operation is terminated.

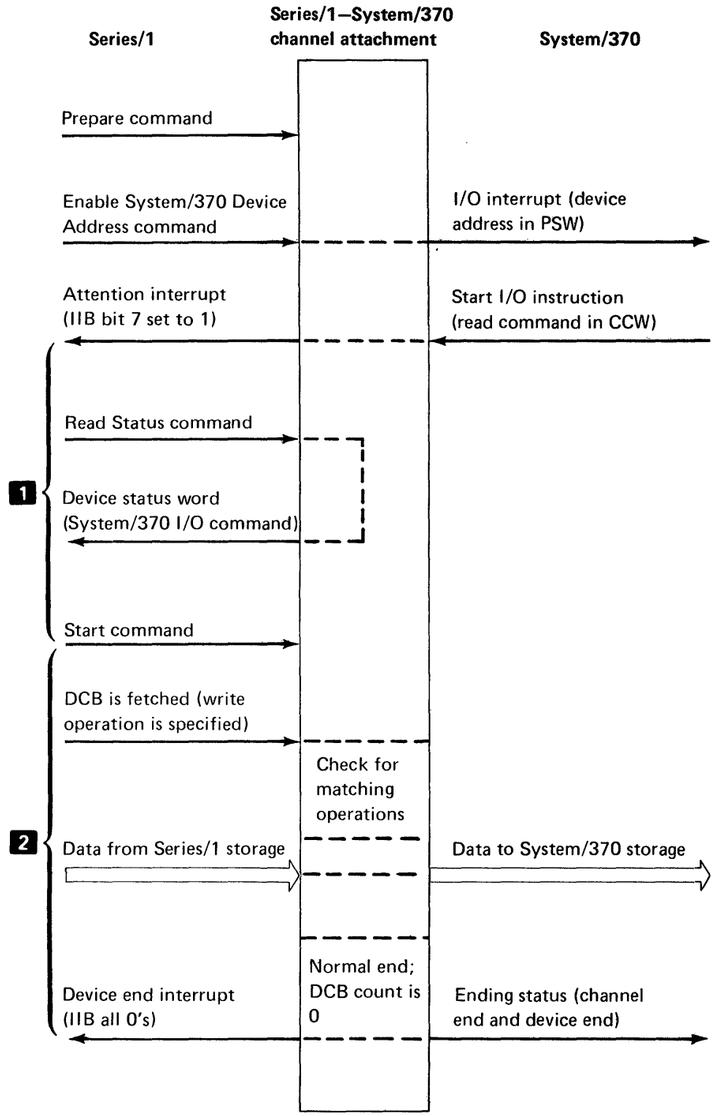
Matching operations

The attachment checks for *matching* operations when data is to be transferred between systems. To avoid an error condition, the Series/1 program must respond to System/370 commands as follows:

System/370 I/O command	*Series/1 I/O command*
Read Buffer	Start*
Read Modified	Start*
Diagnostic Read	Start*
Write	Start**
Erase/Write	Start**
Diagnostic Write	Start**

* The DCB must specify a write operation.
** The DCB must specify a read operation.

Note: Two additional System/370 commands (Select and Erase All Unprotected) require a matching command (Set System/370 Device End) from the Series/1. However, these two commands are not used for data transfer operations between systems.



1 Series/1 program execution affects the channel busy time of the System/370.

2 Series/1 channel throughput affects the channel busy time of the System/370. Data is transferred at the rate of the slower channel up to a maximum of 300,000 bytes per second.

Series/1-System/370 I/O Command Interaction

Some I/O commands issued to the attachment by one system cause events to occur in the other system. For example, a System/370 Write command causes an attention interrupt in the Series/1. The following two tables list the events that occur on the non-issuing system when the command is successfully executed by the attachment:

System/370 I/O Command Interaction

System/370 I/O command	*Series/1 event*
Test I/O	None
Write	Attention interrupt
Read Buffer	Attention interrupt
No-Operation	None
Sense	None
Erase/Write	Attention interrupt or IPL
Read Modified	Attention interrupt
Select	Attention interrupt
Diagnostic Write	Attention interrupt
Diagnostic Read	Attention interrupt
Erase All Unprotected	Attention interrupt
Subsystem Load Enable	None
Sense I/O	None

Note: The System/370 commands that cause an attention interrupt to the Series/1 are referred to as "attention" commands. The Series/1 device status word contains the necessary information about the attention interrupt generated by these commands.

Series/1 I/O Command Interaction

Series/1 I/O command	*System/370 event*
Read ID	None
Read Status	None
Prepare	None
Disable System/370 Device Address	None
Enable System/370 Device Address	I/O interrupt (device not enabled) None (device enabled)
Set System/370 Device End*	Status presented
Set Attention to System/370	I/O interrupt
Device Reset	I/O interrupt (systems "connected"); None (systems not "connected")
Start*	None
Start Diagnostic	None
Start Cycle Steal Status	None
Halt I/O	Status presented (systems "connected"); None (systems not "connected")

* These commands are issued in response to certain System/370 commands.

Time-Outs

The attachment uses an internal timer to establish a time limit (approximately 480 milliseconds) for certain operations or command sequences. If the time limit is exceeded, one of two time-outs can occur: command time-out or data transfer time-out. The attachment then terminates the operation in process.

Command Time-Out

All System/370 "attention" commands require a response from the Series/1. The appropriate command must be received by the attachment from the Series/1 within the established time limit; otherwise, a command time-out occurs. When the time-out occurs, the attachment terminates the operation and presents unit check status to the System/370. An attention interrupt is presented to the Series/1 with the time-out bit (bit 5) in the interrupt information byte (IIB) set to 1.

Data Transfer Time-Out

This condition can occur when the two systems are "connected" and data is being transferred between them, or when an IPL record is being transferred from the System/370 to the Series/1. This time-out indicates that the transfer time between successive bytes has exceeded the time limit. The data transfer time-out can also occur when the systems are "connected" and the data transfer did not begin before the time-out interval was exceeded.

During data transfer, this time-out causes the attachment to terminate the operation. Unit check status is presented to the System/370. An exception interrupt is presented to the Series/1 with the time-out bit (bit 5) in the device status word set to 1.

During IPL, this time-out causes the attachment to terminate the IPL data transfer and to present unit check status to the System/370. The attachment remains in the IPL state, and the System/370 program can retry the IPL command sequence.

Addressing

The Series/1-System/370 attachment connects to the Series/1 I/O channel and to a System/370 selector or block-multiplexer channel. The attachment can be addressed by either system.

Series/1 I/O Addressing

The Series/1 section of the attachment appears as a cycle-steal device on the Series/1 channel and is addressed by the processor via the 8-bit address field of the immediate device control block (IDCB) associated with the Series/1 Operate I/O instruction. The address is determined by address jumpers installed on the feature card.

Series/1 Device Address Jumpers

Jumper pins located on the attachment feature card allow the user to select any one of 256 addresses (hexadecimal 00-FF) as the Series/1 device address. Refer to the appropriate MLD logic page for jumper pin locations.

System/370 I/O Addressing

The System/370 section of the attachment appears as a control unit with 32 consecutive device addresses to the System/370 selector or block-multiplexer channel. The System/370 program addresses any one of these device addresses by using a Start I/O, Test I/O, or Halt Device instruction. The instruction identifies the I/O control unit and device (in this case, the attachment and a device address). The System/370 I/O instructions and I/O commands that are used by the attachment are explained in "System/370 Attachment Commands" in this chapter.

Only one System/370 device address in the attachment may be active at any one time. The control unit (attachment) is busy if selection of any of the other 31 addresses is attempted.

The Series/1 processor is able to control the "ready" or "not ready" status of any of the System/370 device addresses in the attachment by issuing an Enable System/370 Device Address command or a Disable System/370 Device Address command. These commands are explained in "Series/1 Attachment Commands" in this chapter.

The 32 System/370 device addresses must be consecutive and in a specific group selected by address jumpers installed on the attachment card.

System/370 Device Address Jumpers

Jumper pins located on the attachment feature card allow the user to select one of eight groups of 32 consecutive addresses, as follows:

Group address ranges (hex)	*Bits 0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*
00-1F	0	0	0	X	X	X	X	X
20-3F	0	0	1	X	X	X	X	X
40-5F	0	1	0	X	X	X	X	X
60-7F	0	1	1	X	X	X	X	X
80-9F	1	0	0	X	X	X	X	X
A0-BF	1	0	1	X	X	X	X	X
C0-DF	1	1	0	X	X	X	X	X
E0-FF	1	1	1	X	X	X	X	X

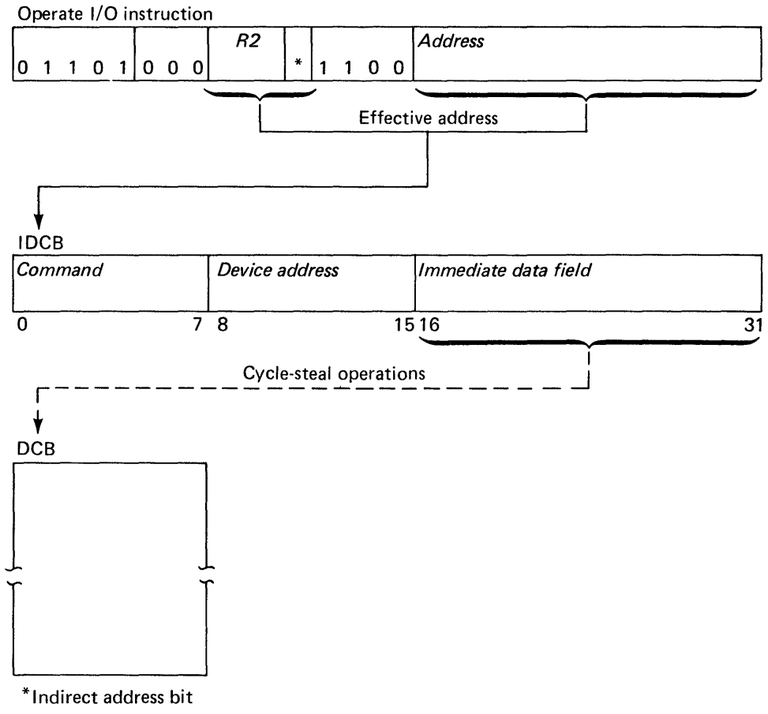
Note: These eight bits correspond to the eight bits of the device address field of the System/370 Start I/O instruction. An X indicates that there are no jumper pins on the attachment card; only the group-selection bits (0–2) have jumper pins.

Refer to the appropriate MLD logic page for jumper locations.

Attachment Program Control (Series/1)

The Series/1 section of the attachment can perform cycle-steal and direct program control (DPC) operations. These operations are initiated by execution of the Operate I/O instruction by the Series/1 processor.

Operate I/O Instruction



The Operate I/O instruction generates an effective address that points to an immediate device control block (IDCB) in main storage. The IDCB contains the command field, the attachment address, and an immediate data field. For DPC operations, the immediate data field is used as a data word. For cycle-steal operations, the immediate data field contains the address of a device control block (DCB) that provides the information needed by the attachment for the operation.

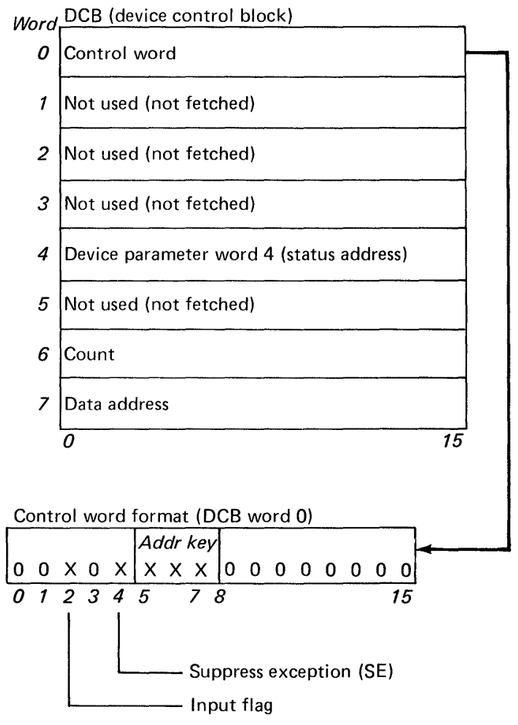
Series/1 Start commands (cycle-steal operations) require that a "matching" command be accepted previously by the attachment from the System/370.

If a System/370 command is not active, command reject (CC=3) is reported to the Series/1 processor. Command reject is also returned if the Series/1 responds with a "non-matching" command.

Device Control Block (DCB)

The attachment uses the DCB to specify the operation to be performed for cycle-steal commands. The DCB, an eight-word control block residing in main storage, contains the parameters for the cycle-steal operation. The address in the immediate data field of the IDCB points to word 0 of the DCB, and must be an even-byte address (bit 31 of the IDCB=0). If the address is not even, command reject (CC=3) is returned to the processor when the cycle-steal operation is initiated.

The address in the IDCB is transferred to the attachment during execution of any cycle-stealing command. The attachment uses this address to fetch (via cycle-steal) the DCB. The DCB parameters are checked for parity as they are fetched from main storage.



Device parameters 1, 2, 3, and 5 are not used and are not fetched by the attachment. The DCB words that are used have the following meanings:

Control Word (Word 0)

Bit 0 *Not used.* This bit must be set to 0. If it is set to 1, the attachment reports a DCB specification check.*

Bit 1 *Not used.* This bit must be set to 0. If it is set to 1, the attachment reports a DCB specification check.*

Bit 2 *Input flag.* This bit indicates the direction of data transfer to the attachment.
0 = Output (Series/1 main storage to the attachment);
1 = Input (attachment to Series/1 main storage).

Bit 3 *Not used.* This bit must be set to 0. If it is set to 1, the attachment reports a DCB specification check.*

Bit 4 *Suppress exception (SE).* This bit, when set to 1, allows the attachment to suppress reporting an incorrect length record to the Series/1 processor and causes the attachment to store a residual status block. (Refer to "Residual Status Block" in this chapter.) This bit must be set to 0 for a Start Diagnostic command or for a Start Cycle-Steal Status command. If it is set to 1 for a Start Diagnostic command, the attachment "hangs" in the busy state. If it is set to 1 for a Start Cycle Steal Status command, the attachment reports a DCB specification check.

Bits 5–7 *Cycle-steal address key.* The attachment presents this key to the Series/1 processor during the cycle-steal data transfer. These bits are used only with processors that contain the storage protect feature.

Bits 8–15 *Not used.* These bits are not used but should be set to 0's.

*These errors are not reported for a Start Diagnostic command. Refer to "Start Diagnostic" under "Series/1 I/O Commands" in this chapter for additional information.

Device Parameter (Word 4)

Word 4 is fetched on Start commands (except for a Start Cycle Steal Status command or a Start Diagnostic command). The use of this word depends on the setting of the suppress exception (SE) bit (bit 4) in the DCB control word:

SE bit=0. Word 4 is fetched and checked for parity, but is not used by the attachment.

SE bit=1. Word 4 is fetched; it must contain a main storage address on an even-byte boundary. This address, which is called the status address, is used by the attachment to store the residual status block following completion of the cycle-steal operation. Refer to "Residual Status Block" in this chapter.

Count Word (Word 6)

Word 6 contains the number of data bytes to be transferred for the cycle-steal operation. For a Start command, the count can be 0–65,535. For a Start Cycle Steal Status command, the count must be 8, or a DCB specification check is reported. For a Start Diagnostic command, the count must be 4, or the attachment "hangs" in the busy state.

Data Address Word (Word 7)

Word 7 contains the starting main storage address for the data transfer.

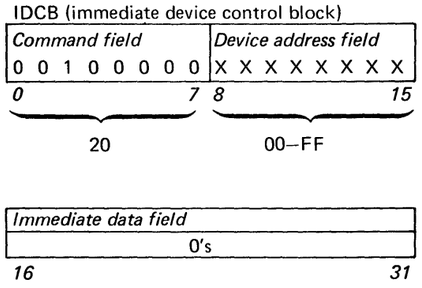
Series/1 I/O Commands

The attachment responds to the following I/O commands from the Series/1 processor:

Command code (hex)	*Name*
20	Read ID
21	Read Status
60	Prepare
62	Disable System/370 Device Address
63	Enable System/370 Device Address
64	Set System/370 Device End
65	Set Attention to System/370
6F	Device Reset
70	Start
71	Start Diagnostic
7F	Start Cycle Steal Status
F0	Halt I/O

Note: Operate I/O instruction condition codes are reported to the processor, by the attachment or processor channel, relating to conditions that can be detected during execution of the I/O commands. In the following descriptions of the attachment commands, the condition codes that may be reported during command execution are listed. If the condition that causes a condition code to be reported is unique to the command, it will be explained in detail; otherwise, the condition codes defined in "I/O Instruction Condition Codes Reported to Series/1" in this chapter apply.

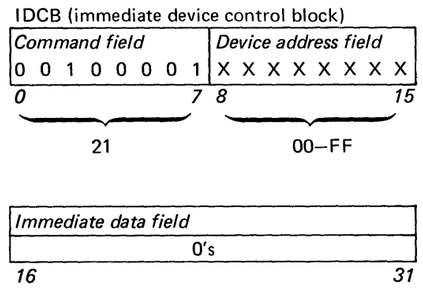
Read ID



The Read ID command causes a unique identification word to be transferred from the attachment to the data field of the IDCB. The ID word for the Series/1-System/370 attachment is 4002 (hex).

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition code 0 or 5 is reported.

Read Status



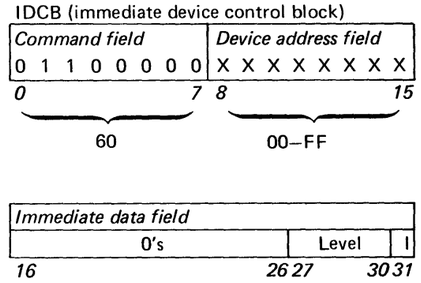
The Read Status command causes a 16-bit device status word to be transferred to the data field of the IDCB. The bits in the status word are:

Bit	*Name*
0	Not used (always 0)
1	On-line
2	System/370 busy or chaining
3	System/370 reset
4	System/370 interface disconnect
5	Time-out
6	System/370 error
7	Attention command
8–12	System/370 device address
13–15	System/370 command

Refer to "Device Status Word" in this chapter for a detailed description of the status bit meanings.

Condition code 0, 1, 2, 5, or 7 can be reported for this command. The command is not executed if condition code 0, 1, 2, or 5 is reported.

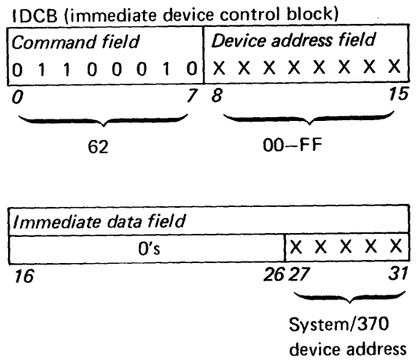
Prepare



The Prepare command transfers the IDCB data word to the Series/1 prepare register in the attachment. The binary value of the level field (bits 27–30) is used to assign the priority interrupt level to the attachment. The I-bit (bit 31) determines if the attachment is allowed to interrupt the Series/1 processor. If the I-bit equals 1, interrupts are allowed; if the I-bit equals 0, interrupts are not allowed.

Condition code 0, 5, or 7 can be reported for this command. The command is not executed if condition code 0 or 5 is reported.

Disable System/370 Device Address

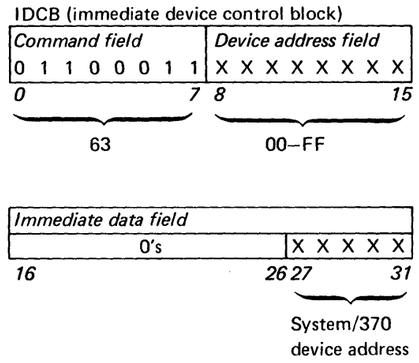


The Disable System/370 Device Address command causes the specified System/370 device address to become unavailable to (1) command selection from the System/370, and (2) a Set Attention to System/370 command from the Series/1. The command disables the device address by setting the appropriate "enable" bit to 0. The System/370 device address is specified in bits 27–31 of the IDCB data field. Note that only the five low-order bits of the address are used. These five bits encode a value of 0–31 to correspond to the 32 consecutive System/370 device addresses in the attachment. The three high-order bits of the address (bits 0–2) define the System/370 control unit address and are selected by jumper options on the attachment feature card. The address jumper options are explained in "System/370 Device Address Jumpers" in this chapter.

Execution of this command does not cause an interrupt to the Series/1 processor or to the System/370 processor.

Condition code 0, 1, 2, 3, 5, or 7 can be reported for this command. Condition code 3 is reported (1) if the attachment is responding to a System/370 command-chaining sequence when this command is received in the attachment or (2) if this command is executed in response to a System/370 "attention" command interrupt. The command is not executed if condition code 0, 1, 2, 3, or 5 is reported.

Enable System/370 Device Address



The Enable System/370 Device Address command causes the specified System/370 device address to become available for execution of commands from the Series/1 processor and the System/370 processor. The command enables the device address by setting the appropriate "enable" bit to 1. The System/370 device address is specified in bits 27–31 of the IDCB data field. Note that only the five low-order bits of the address are used. These five bits encode a value of 0–31 to correspond to the 32 consecutive System/370 device addresses in the attachment. The three high-order bits of the address (bits 0–2) define the System/370 control unit address and are selected by jumper options on the attachment feature card. The address jumper options are explained in "System/370 Device Address Jumpers" in this chapter.

When the attachment is on-line (Enable/Disable switch on the 4993-1 termination enclosure is in the Enable position) and this command is executed, the following events occur:

1. An interrupt (with device end status) is presented to the System/370 processor. The System/370 interrupt automatically stores the System/370 device address into its main storage. If the address was already enabled, this interrupt is not generated to the System/370.
2. When the System/370 accepts the interrupt, or if the device address is already enabled, a device end interrupt is presented to the Series/1 processor.

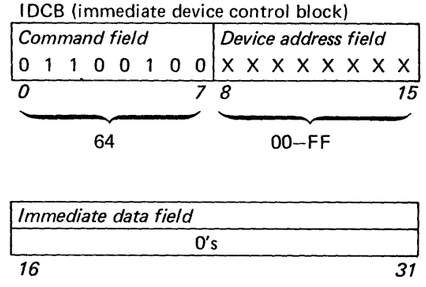
Once a System/370 device address is enabled, it remains enabled until one of the following events occur:

1. A Disable System/370 Device Address command is successfully executed.
2. The attachment is switched off-line to the System/370.
3. A system reset or a power-on reset occurs in the Series/1 processor.

Note: Execution of this command does not involve a data transfer between the two systems; however, the systems are "connected" following acceptance of this command by the attachment, and remain "connected" until the device-end interrupt is presented to the Series/1.

Condition code 0, 1, 2, 3, 4, 5, or 7 can be reported for this command. Condition code 3 is reported if the attachment is responding to a System/370 command-chaining sequence when this command is received in the attachment or if this command is executed in response to a System/370 "attention" command interrupt. Condition code 4 is reported if the attachment is off-line (the 4993-1 termination enclosure is Disabled). The command is not executed if condition code 0, 1, 2, 3, 4, or 5 is reported.

Set System/370 Device End

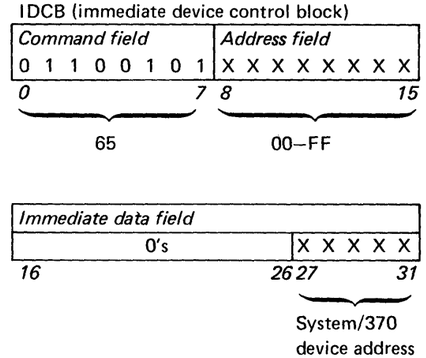


The Set System/370 Device End command causes the attachment to present device-end status to the System/370. This command is executed only in response to a Series/1 attention interrupt caused by a System/370 Select command or an Erase All Unprotected command.

The command, which does not cause an interrupt to the Series/1 processor, indicates ending status to the System/370 at completion of the System/370 Select command or the Erase All Unprotected command. The attachment will not accept any other commands from the Series/1 processor until this ending status is accepted by the System/370.

Condition code 0, 1, 2, 3, 4, 5, or 7 can be reported for this command. Condition code 3 is reported if this command is issued in response to any command other than a System/370 Select command or Erase All Unprotected command. Condition code 4 is reported if the attachment is off-line (the 4993-1 termination enclosure is Disabled). The command is not executed if condition code 0, 1, 2, 3, 4, or 5 is reported.

Set Attention to System/370

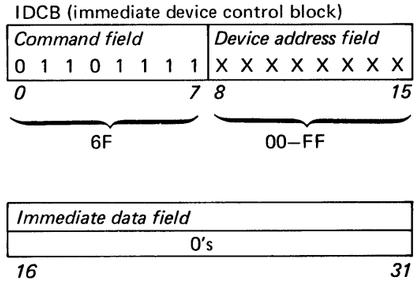


The Set Attention to System/370 command causes the attachment to generate an interrupt (with attention status) to the System/370. A device-end interrupt is presented to the Series/1 after acceptance of the attention interrupt by the System/370.

Note: Execution of this command does not involve a data transfer; however, the systems are "connected" following acceptance of this command by the attachment, and remain "connected" until the device-end interrupt is presented to the Series/1.

Condition code 0, 1, 2, 3, 4, 5, or 7 can be reported for this command. Condition code 3 is reported if the System/370 device address is not enabled or if the attachment is responding to a System/370 command-chaining sequence. Condition code 4 is reported if the attachment is off-line (the 4993-1 termination enclosure is Disabled). The command is not executed if condition code 0, 1, 2, 3, 4, or 5 is reported.

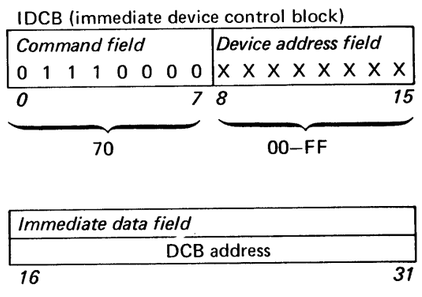
Device Reset



The Device Reset command causes all controls, status, and pending interrupts in the Series/1 section of the attachment to be reset. The prepare register is *not* reset. If the two systems are "connected," any operation between them is terminated, and an interrupt (with unit-check status) is presented to the System/370 to signal the termination. The attachment will be busy-after-reset until this interrupt is accepted by the System/370.

Condition code 0 or 7 can be reported for this command. The command is not executed if condition code 0 is reported.

Start

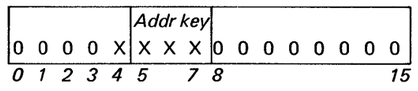


The Start command causes the attachment to "connect" to the System/370 if a System/370 read- or write-type command has been accepted and is pending in the attachment. The Start command initiates a cycle-steal operation between the attachment and the Series/1 processor to fetch the device control block (DCB) from storage. The DCB contains additional information about the type of operation to be performed. The control word (word 0) of the DCB is used to specify either a read or write operation. This operation must "match" the System/370 command that is pending. Refer to "Matching Operations" under "Data Transfer Between Systems" in this chapter.

The Start command is an interrupt-causing command. Upon acceptance of this command, the attachment goes into a busy state until the data transfer is completed, and then presents a device-end interrupt to the Series/1 processor. Error conditions that occur during the data transfer cause interrupts to both processors. These error interrupts are explained in "Series/1 Write Operation" and "Series/1 Read Operation."

Condition code 0, 1, 2, 3, 4, 5, or 7 can be reported for this command. Condition code 3 is reported if a System/370 read- or write-type command is not pending. Condition code 4 is reported if the attachment is off-line (the 4993-1 termination enclosure is Disabled). The command is not executed if condition code 0, 1, 2, 3, 4, or 5 is reported.

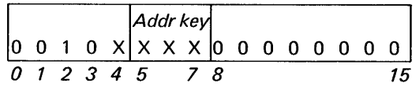
Series/1 Write Operation. A DCB specifying a Series/1 write operation is used to match a System/370 Read Buffer, Read Modified, or Diagnostic Read command. The DCB control word is:



The write operation causes data to be transferred from the Series/1 main storage to the System/370 main storage via cycle-stealing operations. Normal termination for the data transfer occurs when the DCB byte count reaches 0. Refer to "Start Command Termination" in this section for Start command termination conditions.

If a write-type DCB is fetched and it does not match the pending System/370 command, the operation is terminated. An exception interrupt is reported to the Series/1. Bit 0 (device-dependent status available) in the interrupt status byte is set to 1. Ending status (containing channel end, device end, and unit check) is reported to the System/370. Bit 4 (data check) and bit 5 (unit specify) in the System/370 sense byte are set to 1's.

Series/1 Read Operation. A DCB specifying a Series/1 read operation is used to match a System/370 Write, Erase/Write, or Diagnostic Write command. The DCB control word is:



The read operation causes data to be transferred from the System/370 main storage to the Series/1 main storage via cycle-stealing operations. Normal termination for the data transfer occurs when the DCB byte count reaches 0. Refer to "Start Command Termination" for Start command termination conditions.

If a read-type DCB is fetched and it does not match the pending System/370 command, the operation is terminated. An exception interrupt is reported to the Series/1. Bit 0 (device-dependent status available) in the interrupt status byte is set to 1. Ending status (containing channel end, device end, and unit check) is reported to the System/370. Bit 4 (data check) and bit 5 (unit specify) in the System/370 sense byte are set to 1's.

Start Command Termination. Execution of the Start command terminates when any of the following events occur:

Normal ending. The DCB count reaches 0 before the System/370 channel end occurs. The operation is terminated and channel end and device-end status are reported to the System/370. A device-end interrupt, with an interrupt information byte (IIB) =0's, is reported to the Series/1.

Incorrect length record (ILR). Termination of the data transfer occurs on the System/370 and the DCB count is not 0. An exception interrupt, with the ILR bit (bit 2) set in the interrupt status byte (ISB), is reported to the Series/1. This interrupt is suppressed if the suppress exception (SE) bit of the DCB control word is set to 1.

Series/1 error. An error is detected between the Series/1 main storage and the attachment. The data transfer is terminated, and channel-end, device-end, and unit-check status are reported to the System/370. An exception interrupt, with the error identified in the interrupt status byte (ISB), is reported to the Series/1.

Time-out. The amount of time between successive data transfers exceeded 480 milliseconds (±2%). A data transfer time-out occurs and an exception interrupt, with bit 0 of the interrupt status byte (ISB) set to 1 (indicating device-dependent status is available), is reported to the Series/1. The time-out bit is set to 1 in the device status word and in the cycle-steal status word. Channel-end, device-end, and unit-check status are reported to the System/370.

System/370 reset. A System/370 reset caused the operation to be terminated. An exception interrupt, with bit 0 of the interrupt status byte (IIB) set to 1 (indicating device-dependent status is available), is reported to the Series/1. The System/370 reset bit is set to 1 in the device status word and in the cycle-steal status word.

System/370 Interface disconnect. An interface-disconnect sequence occurred on the System/370 channel. An exception interrupt, with bit 0 of the interrupt status byte (ISB) set to 1 (indicating device-dependent status is available), is reported to the Series/1. The interface-disconnect bit is set to 1 in the device status word and in the cycle-steal status word.

System/370 error. This termination condition does not apply to a Series/1 write operation. An error is detected between main storage of the System/370 and the attachment. An exception interrupt, with bit 0 of the interrupt status byte (ISB) set to 1 (indicating device-dependent status is available), is reported to the Series/1. The System/370 error bit is set to 1 in the Series/1 device status word and cycle-steal status word. Channel-end, device-end, and unit-check status are reported to the System/370.

Start Diagnostic

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 0 0 0 1	X X X X X X X X
0 *7*	*8* *15*
71	00–FF

Immediate data field
DCB address
16 *31*

The Start Diagnostic command tests the internal operations of the attachment to verify attachment data flow from/to the Series/1 main storage, and the presentation of interrupts. The attachment must be off-line (the 4993-1 Enable/Disable switch in the Disabled position) to the System/370 when this command is issued.

The DCB used with this command can specify a "write" or a "read" operation and must specify a word count of 4. Any DCB error is considered to be a diagnostic error condition.

Once the IDCB is accepted by the attachment, any error incurred causes the attachment to "hang busy"; no end or exception interrupt is presented to the Series/1. The busy condition can be cleared by any Series/1 reset or the execution of a Device Reset command. A description of the tests performed by this command is in "Write Diagnostic Operation" and "Read Diagnostic Operation."

Condition code 0, 1, 4, 5, or 7 can be reported for this command. Condition code 4 is reported if the attachment is on-line (the 4993-1 termination enclosure is Enabled) to the System/370 when this command is executed. The command is not executed if condition code 0, 1, 4, or 5 is reported.

Write Diagnostic Operation. The write diagnostic operation checks the attachment timer and the attachment's ability to transfer data from the Series/1.

	Addr key	
0 0 0 0 0	X X X	0 0 0 0 0 0 0 0
0 1 2 3 4	*5* *7*	*8* *15*

The write diagnostic operation, specified in the DCB control word for the Start Diagnostic command, causes the attachment to transfer four bytes of data from the Series/1 main storage to the four-byte data buffer in the attachment. The attachment then cycles the timer and, when the timer has completed its cycle, the attachment presents an exception interrupt to the Series/1, with the time-out bit set to 1 in the device status word and in the interrupt status byte (ISB). The operation takes approximately 500 milliseconds, assuming that no other devices are active at this time.

The operation tests the attachment's data transfer logic, control logic, time-out timer, enable/disable timing (for select-out bypass), command decode, ability to cycle-steal from storage, and ability to present an interrupt.

Read Diagnostic Operation. The read diagnostic operation checks the attachment's ability to transfer data from the attachment to the Series/1.

	Addr key	
0 0 1 0 0	X X X	0 0 0 0 0 0 0 0
0 1 2 3 4	*5* *7*	*8* *15*

The read diagnostic operation, specified in the DCB control word for the Start Diagnostic command, causes the attachment to transfer four bytes of data from the four-byte data buffer in the attachment to the Series/1 main storage. If this operation is preceded by a write diagnostic operation to store the four data bytes, the data transferred to Series/1 storage is the one's complement of the original four data bytes with exception to the last 12 bits, which are random values and should be ignored. If this operation is not preceded by a write diagnostic operation, the data transferred from the buffer is in its true form. A device-end interrupt is presented to the Series/1 when the operation is completed.

This operation tests the attachment's ability to read and write data to Series/1 storage, data-flow, sequencing and control, and the ability to present the device-end interrupt.

Start Cycle Steal Status

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 1 1	X X X X X X X X
0 *7*	*8* *15*
7F	00–FF

Immediate data field
DCB address
16 *31*

The Start Cycle-Steal Status command initiates a series of cycle-steal operations to transfer eight bytes (four words) of status from the attachment to Series/1 storage. For a description of these status words, refer to "Cycle-Steal Status Words" in this chapter.

The DCB control word is:

	Addr key	
0 0 1 0 0	X X X	0 0 0 0 0 0 0 0
0 1 2 3 4	*5* *7*	*8* *15*

DCB word 6 must specify a count of 8. DCB word 7 specifies the starting storage address for the status words.

Condition code 0, 1, 2, 5, or 7 can be reported for this command. The command is not executed if condition code 0, 1, 2, or 5 is reported.

Halt I/O

IDCB (immediate device control block)

Command field	*Device address field*
1 1 1 1 0 0 0 0	0's
0 *7*	*8* *15*
F0	

Immediate data field
0's
16 *31*

The Halt I/O command, which is directed to the Series/1 channel, causes a halt of all I/O activity on the channel and resets any pending interrupts. The prepare register in the attachment is not reset. Bits 8–31 of the IDCB are not used, but should be set to 0's.

Only condition code 7 is reported for this command.

I/O Instruction Condition Codes Reported to Series/1

Condition codes are reported to the Series/1 processor in response to an Operate I/O instruction directed to the attachment. The codes are related to conditions that can be detected during execution of the instruction. The following chart shows the I/O commands and the I/O instruction condition codes that can be reported for each command:

I/O command	Hex	I/O instruction condition codes							
		0	1	2	3	4	5	6	7
Read ID	20	X					X		X
Read Status	21	X	X	X			X		X
Prepare	60	X					X		X
Disable System/370 Device Address	62	X	X	X	X		X		X
Enable System/370 Device Address	63	X	X	X	X	X	X		X
Set System/370 Device End	64	X	X	X	X	X	X		X
Set Attention to System/370	65	X	X	X	X	X	X		X
Device Reset	6F	X							X
Start	70	X	X	X	X	X	X		X
Start Diagnostic	71	X	X			X	X		X
Start Cycle Steal Status	7F	X	X	X			X		X
Halt I/O*	F0								X

*Channel-directed command

Note: Condition code 3 is reported if a command other than those listed above is directed to the attachment.

The condition codes have the following meanings:

CC value	*Meaning*
0	Device not attached
1	Busy
2	Busy after reset (refer to "Series/1 Resets")
3	Command reject
4	Intervention required
5	Interface data check
6	Not used
7	Satisfactory

I/O instruction condition codes are mutually exclusive and are reported on a priority basis, with condition code 0 having the highest reporting priority and condition code 7 having the lowest priority.

Series/1 Status Information

Device Status Word

The device status word is transferred from the attachment to the Series/1 and is stored in the second word of the IDCB when a Read Status command is executed. This word contains the status of the attachment. If a command is pending from the System/370, this word also contains the command and device address received from the System/370.

Bit definitions are:

Bit — *Meaning*

0 — *Not used.* Always 0.

1 — *On-line.* This bit indicates the on-line/off-line state of the attachment (4993-1 Enable/Disable switch position). It is set to 1 when the 4993-1 is powered on and enabled. When this bit goes to a logical 1, it presents an attention interrupt to the Series/1.

2 — *System/370 busy or chaining.* This bit is set to 1 when the attachment is busy in a command or chaining sequence to the System/370. It is set to 0 when device end (for the last CCW in the chain) is reported to the System/370.

3 — *System/370 reset.* This bit is set to 1 if the attachment detects a System/370 reset condition while the two systems are "connected." This bit is set to 0 by a Series/1 reset or by successful execution of the next Series/1 command to the attachment.

An exception interrupt is presented to the Series/1 when this bit changes from 0 to 1.

4 — *System/370 interface disconnect.* This bit is set to 1 if the attachment detects an interface disconnect sequence from the System/370 while the two systems are "connected." This bit is set to 0 by a reset from the System/370 or the Series/1, or by successful execution of the next Series/1 command to the attachment.

5 — *Time-out.* This bit is set to 1 when the attachment detects a time-out that is caused by the Series/1 processor taking excessive time between data transfers between the two systems. The time-out interval is 480 milliseconds (±2%). This bit is set to 0 by a Series/1 reset or by successful execution of the next Series/1 command to the attachment. It is also set to 0 by a System/370 reset or System/370 interface disconnect if the reset or disconnect occurs after the time-out while the two systems are "connected."

6 — *System/370 error.* This bit is set to 1 when a parity error is detected by the attachment during data transfer *from* the System/370. This bit is set to 0 by a Series/1 reset or by successful execution of the next Series/1 command to the attachment.

Note: A parity error detected by the System/370 channel is not reported to the attachment or indicated by this bit.

7 — *Attention command.* This bit is set to 1 when an "attention" command is received by the attachment from the System/370. (Refer to "Series/1-System/370 Command Interaction" in this chapter for the System/370 commands that cause an attention interrupt to the Series/1.) When set to 1, this bit indicates that bits 8–15 of this status word are valid and that they contain the last device address and command issued by the System/370. The "attention" command is encoded in bits 13–15 of this status word. A System/370 No-Operation, Test I/O, Sense, Sense I/O, or Subsystem Load Enable command does not affect the setting of this bit.

This bit is set to 0 by normal termination of the command or by a Series/1 reset. It is also set to 0 by a System/370 reset, an interface disconnect from the System/370, or a time-out condition.

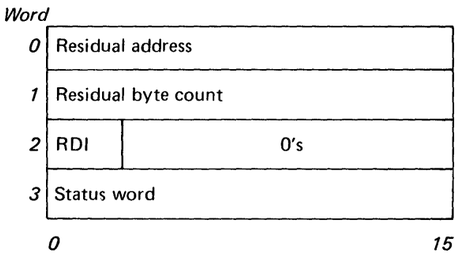
8–12 — *System/370 device address.* These bits are the five low-order bits of the last device address selected by the System/370. The address is a value of 0–31 and is not changed until the attachment receives a different device address.

13–15 — *System/370 command.* These bits contain the binary encoded value that indicates the last "attention" command received from the System/370. This command is valid only when bit 7 of this status word is set to 1. These bits are not changed until the attachment receives a subsequent command from the System/370.

Bit 13	*14*	*15*	*Command*
0	0	0	Read Buffer
0	0	1	Read Modified
0	1	0	Write
0	1	1	Erase/Write
1	0	0	Select
1	0	1	Erase All Unprotected
1	1	0	Diagnostic Read
1	1	1	Diagnostic Write

Cycle-Steal Status Words

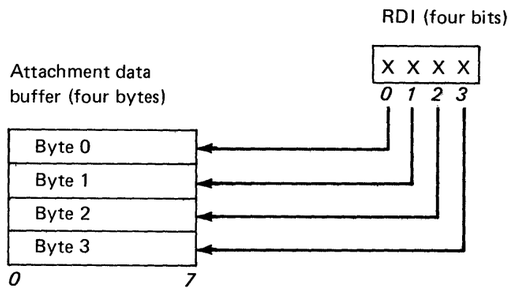
Four status words (eight bytes) are transferred to the Series/1 processor when a Start Cycle Steal Status command is executed. The format is:



Residual Address. This word contains the main storage address of the last attempted cycle-steal transfer associated with a Start command. The residual address can be a data address, a DCB address, or a residual-status-block address, and is updated upon execution of a cycle-steal transfer not associated with a Start Cycle Steal Status command. Execution of a Start Cycle Steal Status command does not alter the address. The address is set to 0000 (hex) by a power-on reset.

Residual Byte Count. When an operation is terminated, this word indicates any remaining byte count in the Series/1 section of the attachment. Execution of a Start Cycle Steal Status command does not alter this byte count.

Residual Data Indicator (RDI). Each RDI bit corresponds to one byte location in the attachment data buffer, as follows:



When a data transfer operation has ended, any bytes of data remaining in the buffer are indicated by setting the appropriate RDI bits to 1's. This is a flag to the Series/1 program that all data was not completely transferred. The RDI bits are set to 0's when no data remains in the buffer.

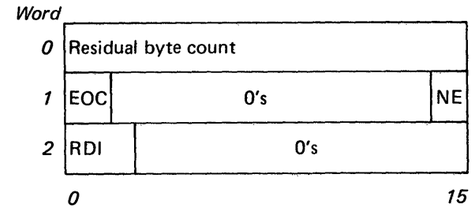
Status Word. This word is identical to the device status word. Refer to "Device Status Word" in this chapter for detailed bit definitions.

Bit	*Meaning*
0	Not used—always 0
1	On-line
2	System/370 busy or chaining
3	System/370 reset
4	System/370 interface disconnect
5	Time-out
6	System/370 error
7	Attention command
8–12	System/370 device address
13–15	System/370 command

Residual Status Block

When the suppress exception bit in the DCB control word is set to 1 for a Start command, the attachment stores the three-word residual status block into Series/1 storage after the data transfer specified in the DCB is completed. The starting storage address for the residual status block is specified in DCB word 4.

The format of the residual status block is:



EOC – End of chain (bit 0)
NE – No exception (bit 15)
RDI – Residual data indicator (bits 0–3)

Residual Byte Count. When an operation terminates, this word indicates any remaining byte count in the Series/1 section of the attachment.

End of Chain (EOC). This bit is always set to 1 when the residual status block is stored.

No Exception (NE). This bit is set to 0 when an incorrect-length record is detected; otherwise, it is set to 1.

Residual Data Indicator (RDI). These bits indicate residual bytes of data that remain in the attachment data buffer after a data transfer has ended. The four bits correspond, respectively, to the bytes of the four-byte attachment data buffer. Refer to "Cycle-Steal Status Words" in this chapter for additional information.

I/O Interrupts

If the I-bit in the prepare register has been set to 1 by a Prepare command, the attachment can present the following interrupts to the Series/1 processor:

- Exception interrupt
- Device-end interrupt
- Attention interrupt
- Attention and device-end interrupt

Exception Interrupt

The exception interrupt is presented to the Series/1 when an operation terminates abnormally, or after successful completion of a write diagnostic operation. If an error condition occurred, the interrupt status byte (ISB) of the interrupt ID word describes the type of error. If bit 0 of the ISB is set to 1 when the interrupt occurs, additional information about the error is available from the attachment. This additional information can be accessed via a Start Cycle Steal Status command or a Read Status command.

Device-End Interrupt

The device end interrupt is presented when the operation specified by the following commands is successfully completed:

- Start command
- Start Cycle Steal Status
- Start Diagnostic (read diagnostic only)
- Enable System/370 Device Address
- Set Attention to System/370

The interrupt information byte (IIB) of the interrupt ID word passes the information about the interrupt to the Series/1.

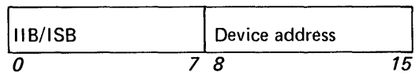
Attention Interrupt

The attention interrupt is presented to the Series/1 by the attachment when one of the following conditions occur:

- The attachment accepts an "attention" command from the System/370. System/370 commands that cause an attention interrupt are: Write, Read Buffer, Erase/Write, Read Modified, Select, Diagnostic Write, Diagnostic Read, and Erase All Unprotected.
- The attachment detects a System/370 reset or a System/370 interface disconnect when not "connected" (a matching pair of commands from the System/370 and Series/1 is not active in the attachment) to the System/370.
- The attachment is set on-line to the System/370 (4993-1 termination enclosure Enable/Disable switch being set to the Enable position). This interrupt occurs only once when the switch transition occurs.
- A time-out occurs following the acceptance of a System/370 "attention" command by the attachment.

Interrupt ID Word

Acceptance of an interrupt causes the attachment to present an interrupt ID word to the Series/1 processor. This word is placed in register 7 of the interrupting level, and has the following format:



IIB – Interrupt information byte
ISB – Interrupt status byte

The IIB (interrupt information byte) is presented when interrupt condition code 3, 4, or 7 is reported. The ISB (interrupt status byte) is presented when interrupt condition code 2 is reported. The device address field contains the Series/1 address assigned to the attachment.

Interrupt Information Byte (IIB)

The bits in the IIB have the following meanings:

Bit	*Meaning*
0	*Permissive device end.* This bit is set to 1 when an incorrect-length record (ILR) is detected and suppress exception (SE) is in effect. Suppress exception is active when the SE bit in the DCB control word is set to 1.
1	*On-line.* This bit is set to 1 when the attachment goes from an off-line to an on-line state (4993-1 termination enclosure Enable/Disable switch being set to the Enable position).
2	*Chaining device end.* This bit is set to 1 if System/370 chaining is indicated while the two systems are "connected." It is used to notify the Series/1 processor that chaining is in effect, and is presented (in the IIB) with a normal device end interrupt.
3*	*System/370 reset.* This bit is set to 1 if the attachment detects a system reset from the System/370 while the two systems are not "connected." This condition causes an attention interrupt to the Series/1 processor.
4*	*System/370 interface disconnect.* This bit is set to 1 if a System/370 interface disconnect sequence is detected while the two systems are not "connected." This condition causes an attention interrupt to the Series/1 processor.
5*	*Time-out.* This bit is set to 1 by a command time-out as follows: When an "attention" command is received from the System/370, the attachment presents an attention interrupt request to the Series/1 processor, sets IIB bit 7 to 1 (attention command), and starts a timer. The time-out interval is 480 milliseconds (±2%). If a time-out occurs before the interrupt is accepted, IIB bit 7 is reset to 0 and this time-out bit is set to 1. Setting this time-out bit terminates the System/370 command. A time-out can also occur after the "attention" command interrupt has been accepted, but before the Series/1 processor responds with a matching operation. In this case, another attention interrupt request, with the IIB time-out bit set to 1, is presented to the Series/1 processor. A third condition can occur where both the IIB time-out bit and the attention command bit (bit 7) are set to 1. This condition indicates that the attachment has received a System/370 command while a *time-out* attention interrupt is still active from a previous command.
6	*Chaining attention.* This bit is used, in conjunction with IIB bit 7 (attention command), to further define a System/370 chaining condition. The bit indicates that the System/370 command received by the attachment is either the beginning of a new chain or a continuation of chaining, as follows:

IIB bit 6	*IIB bit* 7	*Meaning*
1	1	Beginning of a new chain
0	1	Continuation of chaining

Bit 6 has meaning only when bit 7 is set to 1 and the command is involved in a chaining sequence. Refer to "System/370 Chaining" in this chapter for additional details.

7*	*Attention command.* This bit is set to 1 when an "attention" command is received from the System/370. This condition generates an attention interrupt to the Series/1 processor. A time-out condition, a System/370 reset, or a System/370 interface disconnect can reset this bit before it is presented to the Series/1. Refer to IIB bits 3, 4, and 5 for additional details. If this bit is a 1 with any of these conditions, it means that the System/370 command was the *last event* received in the status word, and the command is *still active*.

* IIB bits 3, 4, 5, and 7 are dynamically updated according to their priority before they are presented. Bit 3 has the highest priority, and proceeding sequentially, bit 7 has the lowest priority. If a higher priority event occurs after a lower priority event occurred and before the IIB is presented, the IIB bit representing the lower priority event is reset and the bit representing the higher priority event is set. If the beginning of the higher priority event coincides with the presentation of the lower priority IIB bit, the lower priority bit is reset and at the completion of the higher priority event that caused this condition, another attention interrupt is presented with its corresponding bit set to 1 in the IIB.

Interrupt Status Byte (ISB)

The ISB is presented to the Series/1 processor when an exception interrupt is reported. For a cycle-steal device, the bits within the ISB have standard definitions, as follows:

Bit	*Meaning*
0	Device dependent status available
1	Not used (always 0)
2	Incorrect-length record
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

Refer to the appropriate Series/1 processor theory diagrams manual for a complete description of the ISB.

I/O Interrupt Condition Codes Reported to Series/1

The condition code reported by the attachment at interrupt acceptance defines the type of interrupt, as follows:

Condition code value	*Meaning*
2	Exception interrupt
3	Device-end interrupt
4	Attention interrupt
7	Attention and device-end interrupt

Initial Program Load of Series/1 from System/370

The attachment is capable of executing a host system (System/370) IPL of the Series/1. The inhibit IPL jumper must be removed from the attachment feature card to allow this function. The System/370 program initiates the IPL by issuing two I/O commands in the proper sequence. This sequence is a Subsystem Load Enable command chained to an Erase/Write command. These commands must be issued to the device address that is the lowest address in the System/370 device address group assigned to the attachment.

Execution of the Subsystem Load Enable command causes the attachment to enter the IPL preparatory state. The preparatory state is exited following receipt of the next command, and the new state of the attachment is determined, as follows:

1. If the command is an Erase/Write (properly specified), the attachment enters IPL state.
2. If another command is presented or if the Erase/Write is improperly specified, the attachment terminates IPL preparation state and rejects the command. Unit check is returned to the System/370.

IPL State

In IPL state, data is transferred via the attachment from main storage of the System/370 to main storage of the Series/1 (beginning at location 0000 in the Series/1). The IPL record length (total byte count) is specified in the count field associated with the Erase/Write command. The maximum record length is 64K bytes. When all data has been transferred, IPL state is terminated and ending status is presented to the System/370. A device-end interrupt, using priority interrupt level 0, is presented to the Series/1.

If an error occurs during data transfer, the operation is terminated, but the attachment remains in IPL state. Unit check status is presented to the System/370 to indicate the error condition. The System/370 program must then retry the IPL sequence. The attachment rejects any commands other than those necessary for IPL retry.

IPL Retry

If an error occurs during an IPL operation, the System/370 program can retry by initiating the complete IPL command sequence again. This sequence is a Subsystem Load Enable command chained to an Erase/Write command. If the attachment is waiting in the IPL state (due to a previous IPL error), it rejects any other commands from the System/370.

Inhibit IPL Jumper

The feature card contains a jumper option for host IPL. The inhibit IPL jumper *must not* be installed on the attachment feature card if the user wishes to IPL the Series/1 from the System/370. Refer to the appropriate MLD logic page for the inhibit IPL jumper location.

Series/1 Resets to Attachment

Power-on Reset

A power-on-reset resets both the Series/1 and the System/370 sections of the attachment. The prepare register in the Series/1 section is reset. All System/370 device addresses are disabled, and the Series/1 residual address (in the cycle-steal status words) is set to 0000 (hex).

System Reset

The system reset causes the Series/1 section of the attachment, including the prepare register to be reset. All System/370 device addresses are disabled. If an operation is in process when this reset occurs, ending status, with a status byte indicating unit check, is presented to the System/370. The System/370 sense byte further defines the Series/1 reset condition. The Series/1 section of the attachment is in a busy-after-reset state until the System/370 accepts or clears the ending status.

Halt I/O Reset

The halt I/O reset is generated when a Series/1 Halt I/O command is executed. It is identical to a system reset, except that the prepare register and the System/370 device addresses are not reset.

Machine-Check Reset

The machine-check reset is generated when a machine-check interrupt (not caused by a storage parity error) is presented. It is identical to a system reset, except that the prepare register and the System/370 device addresses are not reset.

Device Reset

The device reset is generated when a Series/1 Device Reset command is executed. It is identical to a system reset, except that the prepare register and the System/370 device addresses are not reset.

Busy After Reset State

The busy after reset state is entered when the attachment detects a Series/1 reset while the two systems are "connected." The operation in process is terminated and an ending status (with unit check status) is presented to the System/370. The busy after reset state is exited when the status is accepted by the System/370 or when a System/370 reset occurs. During the busy after reset state, the attachment returns I/O instruction condition code 2 to most Series/1 commands. Refer to "I/O Instruction Condition Codes Reported to Series/1" in this chapter for a list of these commands.

Attachment Program Control (System/370)

The commands and status described in the following sections are for reference only as they apply to the Series/1-System/370 attachment feature. For a complete description of System/370 I/O operations, refer to the manual, *IBM System/370 Principles of Operation*, GA22-7000, available through the nearest IBM branch office.

System/370 Start I/O Instruction

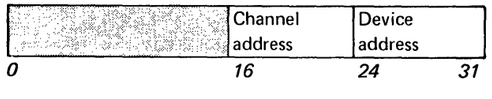
The System/370 program initiates I/O operations by using a Start I/O instruction. This instruction identifies the I/O control unit and device (in this case, the attachment and a device address), and causes the channel to fetch a channel address word (CAW) from a fixed location in main storage. The CAW must contain an address that points to the first channel command word (CCW) that is subsequently fetched by the channel. The CCW specifies the I/O command to be executed plus other necessary information. Once the attachment is selected, the I/O command (CCW bits 0–7) is sent to the attachment. An "initial" status byte is returned to the channel (by the attachment) to indicate if the command can be executed. For operations that involve a transfer of data, the attachment sends the channel a second status byte (called "ending" status) when the operation is terminated. This status indicates either a normal ending or, if errors are detected, an abnormal ending.

System/370 I/O commands that are used by the attachment are explained in "System/370 Attachment Commands" in this chapter. Status bytes are explained in "System/370 Status Information" in this chapter.

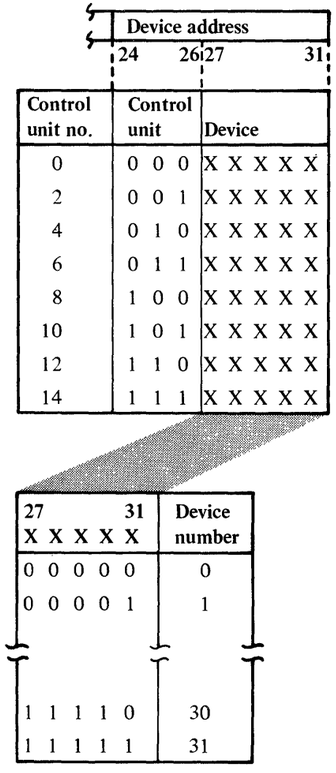
I/O Addressing

The Series/1-System/370 attachment responds to System/370 I/O instructions in the same manner as a control unit with 32 devices.

The System/370 I/O instruction generates an effective address that is used for a channel and device address. The format is:



For control units with 32 devices, the device address field is interpreted as follows:



Only one device address may be active at a time. A device is in the active state (busy) until the operation is completed and the ending status is accepted by the processor. During this period, the control unit (attachment) is busy if there is an attempt to select any of the other 31 addresses.

The System/370 device address is made available to the Series/1 processor via a Series/1 device status word. The Series/1 program has no need for the control unit addressing bits; therefore, only the five low-order bits (27–31) are contained in the status word.

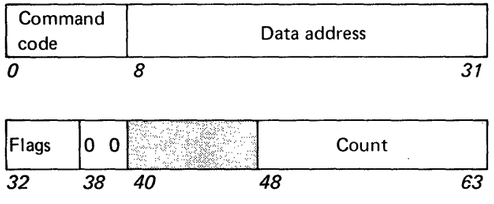
Device Address Enable and Disable. Each of the 32 device addresses has an enable bit (located in the attachment) associated with it. This bit controls the ready state of a device address relative to the System/370, and is set to 1 to indicate the "ready" state or is set to 0 to indicate the "not ready" state. When a device address is selected and the enable bit is set to 0 (not ready), the attachment returns an initial status of unit check to the System/370 for most commands. A sense byte, available to the program, indicates intervention required.

The enable bit is set to 1 or 0, under control of the Series/1 program, by two I/O commands: Enable System/370 Device Address and Disable System/370 Device Address. For a description of these two commands, refer to "Series/1 Attachment Commands" in this chapter.

Once a device address is enabled, it remains in that state until (1) a Disable System/370 Device Address command is executed by the Series/1, (2) the attachment is switched off-line to the System/370, or (3) a system reset or power-on reset occurs in the Series/1.

Channel Command Word

The Channel Command Word (CCW) is fetched by the System/370 channel, and it specifies the information necessary for an I/O operation to be executed. The format is:



The CCW fields and bits that are of special significance to attachment operations are:

Command code. This field specifies the System/370 I/O operation to be performed. These bits are sent to the attachment when the operation is initiated.

Flags. Bit 32 is the chain-data flag and bit 33 is the chain-command flag. For example, if bit 32 is set to 1, data chaining is specified; if bit 33 is set to 1, command chaining is specified. Command chaining affects attachment operations as explained in the section "System/370 Chaining" in this chapter.

System/370 Attachment Commands

This section describes the following System/370 I/O commands that are used with the attachment:

Command code (hex)	*Name*
00	Test I/O
01*	Write
02*	Read Buffer
03	No-Operation
04	Sense
05*	Erase/Write
06*	Read Modified
0B*	Select
0D*	Diagnostic Write
0E*	Diagnostic Read
0F*	Erase All Unprotected
33	Subsystem Load Enable
E4	Sense I/O

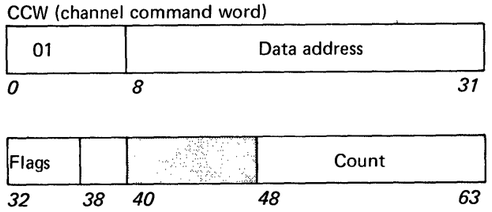
*"Attention" commands. These commands cause an attention interrupt to the Series/1 processor. The Series/1 program must respond before a time-out occurs.

Test I/O

The Test I/O *instruction* tests the state of the System/370 channel and the attached control units and devices. When Test I/O is directed to the Series/1-System/370 attachment, a condition code is set in the System/370 program status word (PSW) and bits are set in the System/370 channel status word (CSW) that indicate the status of the attachment and connecting channel. Refer to "System/370 Status Information" in this chapter for definitions of the condition codes and status bits.

Write

CCW (channel command word)



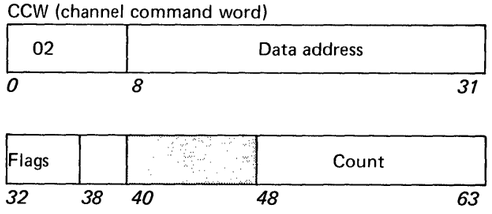
The Write command is used to "connect" the two systems for a data transfer to the Series/1. This command, when issued to the attachment, causes an attention interrupt to the Series/1. The Series/1 must respond with a "read operation" in order to establish the connection. Once the connection is established, data is transferred from main storage of the System/370 to main storage of the Series/1. The operation continues until (1) the count goes to 0 in either the Series/1 DCB or the System/370 CCW, (2) an error is detected, (3) a Series/1 reset occurs, or (4) a System/370 interface disconnect or a System/370 reset occurs.

Unit-check initial status is returned to the System/370 if the addressed device is not ready (not enabled).

Write is an "attention" command, and is subject to command time-out or data transfer time-out.

Read Buffer

CCW (channel command word)



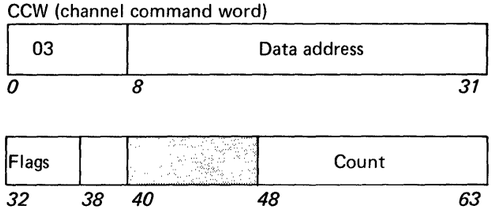
The Read Buffer command is used to "connect" the two systems for a data transfer to the System/370. This command, when issued to tha attachment, causes an attention interrupt to the Series/1. The Series/1 must respond with a matching "write operation" in order to establish the connection. Once the connection is established, data is transferred from main storage of the Series/1 to main storage of the System/370. The operation continues until (1) the count goes to 0 in either the Series/1 DCB or the System/370 CCW, (2) an error is detected, (3) a Series/1 reset occurs, or (4) a System/370 interface disconnect or a System/370 reset occurs.

Unit-check initial status is returned to the System/370 if the addressed device is not ready (not enabled).

Read Buffer is an "attention" command, and is subject to command time-out or data transfer time-out.

No-Operation

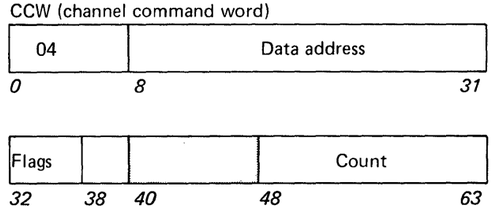
CCW (channel command word)



The No-Operation command performs no functional operation in the attachment, but it may be used to retrieve pending status. No-Operation is an immediate command; therefore, normal ending status is presented as initial status, assuming that the attachment is idle.

Sense

CCW (channel command word)



Execution of the Sense command causes the attachment to transfer one byte of sense data to the System/370. Sense should be issued in response to unit check status for further definition of the unit-check condition. The Sense command CCW should specify a byte count of 1, or an ILR (incorrect-length record) condition may result.

Bits in the sense byte are defined as follows:

Bit	*Meaning*
0	Command reject
1	Intervention required
2	Bus-out check
3	Not used (always 0)
4	Data check
5	Unit specify
6	Control check
7	Not used (always 0)

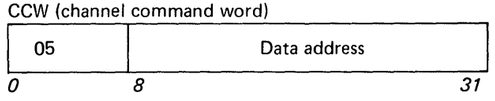
Refer to "Sense Data" in this chapter for complete definitions of the sense bits.

The attachment does not provide a separate sense byte for each System/370 device address. Any pending sense data associated with a device address is always cleared (and lost) if a different address is used for the next I/O operation. The sense data is also cleared if any command other than No-Operation, Sense, Sense I/O, or Test I/O is issued to the attachment.

To ensure valid sense data, the Sense command must be issued immediately following receipt of the unit check status, and must use the proper device address.

Erase/Write

CCW (channel command word)



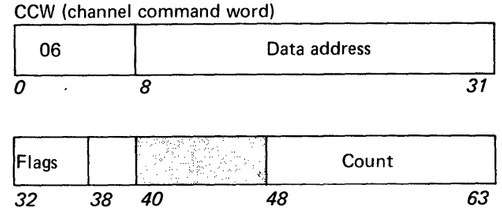
The Erase/Write command can be used for either of two operations:

1. If this command is chained from a Subsystem Load Enable command, it causes an IPL of the Series/1.
2. If this command is not chained from a Subsystem Load Enable command, its operation is identical to a Write command.

When used for an IPL operation, the CCW for the Erase/Write command must not specify chaining; if it does, the results are unpredictable. IPL is explained in "Initial Program Load of Series/1 from System/370" in this chapter.

Read Modified

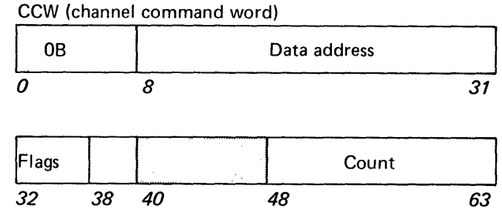
CCW (channel command word)



The Read Modified command functions in the same manner as a Read Buffer command. Refer to the "Read Buffer" command in this section.

Select

CCW (channel command word)



When the Select command is issued, the Series/1 program must respond with a Set System/370 Device End command. The initial status returned to the System/370 contains channel end.

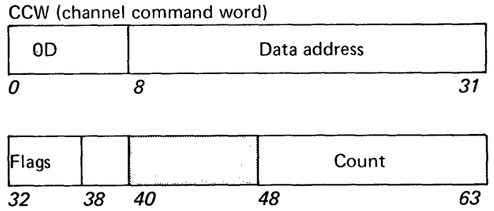
Execution of the Set System/370 Device End command causes an interrupt to the System/370, with a status byte that contains device end.

Unit-Check initial status is returned to the System/370 if the addressed device is not ready (not enabled).

The Select command can be terminated by a Series/1 reset.

Select is an "attention" command, and is subject to command time-out.

Diagnostic Write

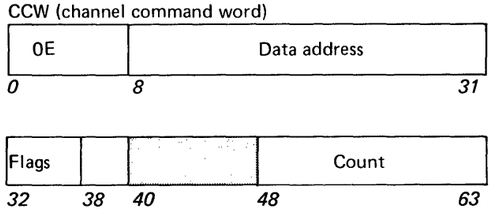


The Diagnostic Write command is used for diagnostic purposes and should only be used by a diagnostic program in the System/370. Its operation is identical to a Write command.

The Series/1 program can distinguish between a normal write operation and a diagnostic write operation by checking bits 13–15 of the Series/1 device status word.

Diagnostic Write is an "attention" command, and is subject to command time-out and data transfer time-out.

Diagnostic Read

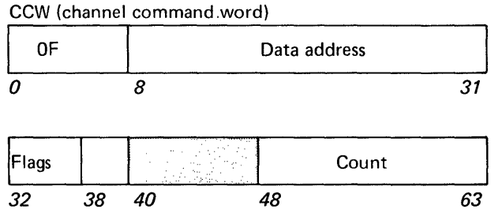


The Diagnostic Read command is used for diagnostic purposes and should only be used by a diagnostic program in the System/370. Its operation is identical to a Read Buffer command.

The Series/1 program can distinguish between a normal read operation and a diagnostic read operation by checking bits 13–15 of the Series/1 device status word.

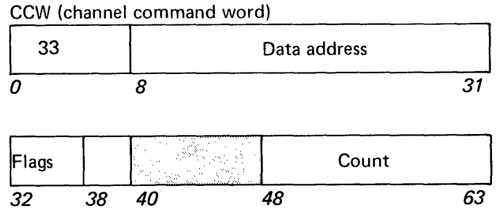
Diagnostic Read is an "attention" command, and is subject to command time-out and data transfer time-out.

Erase All Unprotected



Operation of the Erase All Unprotected command is identical to a Select command. Refer to the "Select" command in this section.

Subsystem Load Enable



The Subsystem Load Enable command prepares the attachment for IPL from the System/370. This command is executed when all of the following conditions are met:

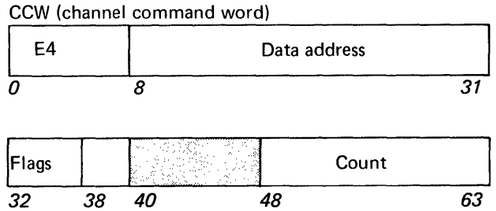
- The attachment is on-line (4993-1 enabled).
- The specified device address is the lowest address in the domain of the attachment.
- The inhibit IPL jumper is removed from the attachment card.

The initial status returned to the System/370 indicates channel end and device end.

Note: This command should be chained to an Erase/Write Command. The IPL begins when the Erase/Write command is executed.

If the Subsystem Load Enable command is chained to a command other than Erase/Write, the second command is rejected and IPL does not occur; the complete IPL sequence must be restarted. IPL is explained in "Initial Program Load of Series/1 from System/370" in this chapter.

Sense I/O



Execution of this command causes the attachment to transfer four bytes of sense data to the System/370. This data provides information about the Series/1 processor and indicates the condition (installed or no installed) of the inhibit IPL jumper. The Sense I/O CCW should specify a byte count of 4.

The Sense I/O command can be directed to any device address in the domain of the attachment.

The four bytes of data are:

Byte	*Data (hex)*
0	FF
1	49
2	50
3	0X

X = 1 Inhibit IPL jumper not installed;
= 0 Inhibit IPL jumper installed.

Refer to "Sense Data" in this chapter for additional information.

System/370 Chaining

When the channel has completed the operation specified by a CCW, it can continue the activity initiated by a Start I/O instruction by fetching a new CCW. Such fetching of a new CCW is called chaining, and the CCWs in such a sequence are said to be chained.

Two types of chaining can be specified in the current CCW: data chaining or command chaining. Bits 32 and 33 of the CCW flag field are used for this purpose, as follows:

CCW bit 32	*bit 33*	*Type*
1	0	Data chaining
0	1	Command chaining

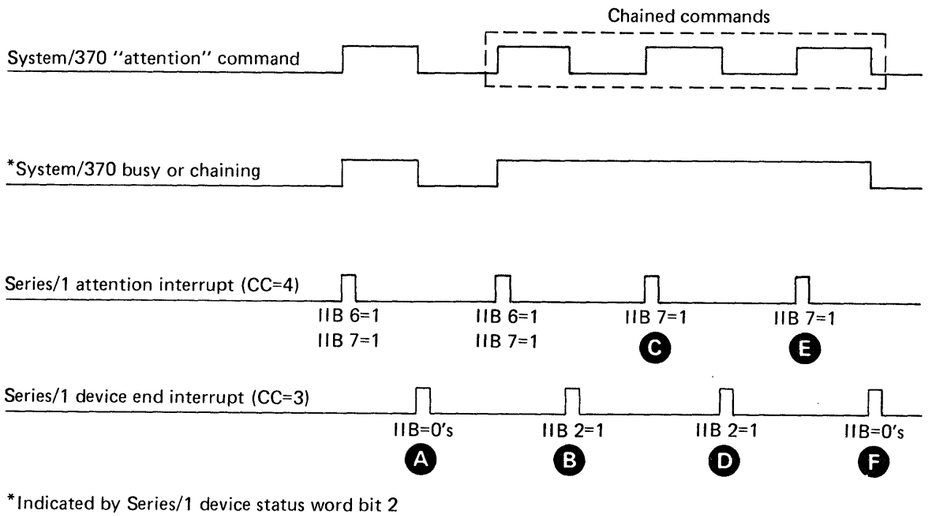
Data chaining is transparent to the Series/1-System/370 attachment. When chaining is referred to during attachment operations, the reference is to command chaining. During command chaining, each CCW initiates a new operation by specifying a new command and data address.

Chaining conditions are reported to the Series/1 program via bits 2, 6, and 7 in the interrupt information byte (IIB). Note that when chaining is indicated in the IIB (bit 2 set to 1), the Series/1 program can refer to the previous IIB (bits 6 and 7) for further definition of the chaining condition. Refer to "Interrupt Information Byte (IIB)" in this chapter for a complete definition of the IIB bits.

The chaining conditions in the following diagram are explained as follows:

- Ⓐ Chaining is not indicated (IIB bit 2 = 0). The previous IIB has no chaining significance.
- Ⓑ Chaining to the next command is indicated. The previous IIB indicates the beginning of a new chain.
- Ⓒ This command is a continuation of chaining.
- Ⓓ Chaining to the next command is indicated. The previous IIB indicates a continuation of chaining.
- Ⓔ This command is a continuation of chaining.
- Ⓕ Further chaining is not indicated.

When chaining is in effect, the Series/1 program must respond to each new command in the chain in the same manner as it would to unchained commands. Normal termination of chaining occurs when the operation specified by the last CCW in the chain is completed. Abnormal termination of the chaining sequence can occur if the attachment detects a condition that causes a System/370 unit check (for example, a Series/1 error or a time-out).



*Indicated by Series/1 device status word bit 2

Note: If attention and device end are presented together (CC=7), the IIB bits are ORed

System/370 Status Information

This section presents the System/370 status information relating to the Series/1-System/370 attachment feature. Status information consists of:

- Condition codes
- Sense data
- Status byte

Condition Codes

During execution of an I/O instruction, the System/370 channel returns one of four condition codes to the System/370 processor. This code indicates that the channel has performed the instruction or, if not, the reason for rejection. In most cases, the channel checks an initial status byte returned by the attachment in order to set the proper condition-code value. A condition code chart is included in this section for reference. Refer to "Status Byte" in this chapter for additional information about the initial status byte.

Input/output instruction	Condition code			
	0	**1**	**2**	**3**
Clear I/O	No operation in progress	CSW stored	Channel busy	Not operational
Halt Device	Interrupt pending, or busy	CSW stored	Channel working	Not operational
Halt I/O	Interrupt pending	CSW stored	Burst operation stopped	Not operational
Start I/O	Successful	CSW stored	Busy	Not operational
Start I/O Fast Release	Successful	CSW stored	Busy	Not operational
Store Channel ID	ID stored	CSW stored	Busy	Not operational
Test Channel	Available	Interrupt pending	Burst mode	Not operational
Test I/O	Available	CSW stored	Busy	Not operational

Sense Data

Two System/370 commands cause a transfer of sense data from the attachment to the System/370 processor: Sense and Sense I/O.

Data for a Sense Command

The sense command transfers one byte of data to the System/370. Bits within the byte are defined as follows:

Bit	*Meaning*
0	*Command reject.* This bit is set to 1 if any of the following conditions are detected: • An invalid System/370 command is issued to the attachment. • A Subsystem Load Enable command is issued and the inhibit IPL jumper is installed, or the device address is incorrect. • An improper command is issued following a Subsystem Load Enable command. *Note:* An improper command is any command other than Erase/Write or an Erase/Write command that is not chained from the Subsystem Load Enable command. • A command not involved in "IPL retry" is issued when the attachment is in the IPL state.
1	*Intervention required.* This bit is set to 1 if a command (other than those noted) is issued to the attachment and the addressed device is not ready. *Note:* Exceptions are the Sense, Sense I/O, Subsystem Load Enable, and Erase/Write (when used for IPL) commands.
2	*Bus-out check.* This bit is set to 1 if the attachment detects bad parity on any command byte or data byte received from the System/370 channel.
3	*Not used.* Always 0.
4	*Data check.* This bit is set to 1 when a Series/1 error (storage error or command mismatch) or a Series/1 reset is detected during execution of a command involving the Series/1.
5	*Unit specify.* This bit is set to 1 under the same condition as bit 4 (data check).
6	*Control check.* This bit is set to 1 when the attachment detects a time-out condition due to (1) excessive time between data transfers (data transfer time-out) or (2) excessive time for the Series/1 to respond to a System/370 "attention" command (command time-out).
7	*Not used.* Always 0.

After execution of a Sense command, all bits of this sense byte are set to 0.

Data for a Sense I/O Command

The Sense I/O command causes four bytes of data to be transferred to the System/370. This data represents (1) a Series/1 identification number and (2) the condition of the inhibit IPL jumper on the attachment feature card.

Inhibit IPL jumper not installed:

Byte	*0*	*1*	*2*	*3*
Data (hex)	FF	49	50	01

Inhibit IPL jumper installed:

Byte	*0*	*1*	*2*	*3*
Data (hex)	FF	49	50	00

Bytes 0, 1, and 2 are always as shown. Byte 3 indicates the status of the inhibit IPL jumper.

Status Byte

The attachment generates a status byte to inform the System/370 channel of attachment and device conditions. This status byte can be generated synchronously (while the attachment is selected and performing a command operation with the channel) or asynchronously (while the attachment is not selected). Synchronous status is passed to the channel as both initial status and ending status to a command. Asynchronous status reflects (1) ending status for certain commands, (2) an action that requires program intervention, or (3) an equipment malfunction.

Bits 32–39 of the channel status word (CSW) contain the status byte from the channel.

Bits within the status byte are:

Status bit	*CSW bit*	*Name*
0	32	Attention (A)
1	33	Status modifier (SM)
2	34	Control unit end (CUE)
3	35	Busy (B)
4	36	Channel end (CE)
5	37	Device end (DE)
6	38	Unit check (UC)
7	39	Unit exception UE)

For Series/1-System/370 attachment operations, the bits are defined as follows:

Attention. This bit is set to 1 when a Set Attention to System/370 command is executed by the Series/1. Attention is always presented as asynchronous status.

Status Modifier. This bit is set to 1 (with the busy bit) in initial status to indicate control unit (attachment) busy. This means that a device other than the one selected is currently active or that the attachment has pending status for a device other than the one selected.

Control Unit End. This bit is set to 1 to indicate that a previously reported busy condition (control unit busy) has been cleared, and that the attachment is now free to execute a new command.

Busy. This bit is set to 1 and presented alone in initial status when the addressed device is busy. This indicates that (1) the device has pending status and the present command is not Test I/O or (2) the device is executing an Erase All Unprotected command or a Select command.

The busy bit is set to 1 and presented with the status modifier bit to indicate control unit busy.

Channel End. This bit is set to 1 to indicate that all data transfers are complete. It is normally presented as synchronous status.

If channel end status is pending when the device operation is completed, it is presented (with the device-end bit) as asynchronous status.

Device End. This bit is set to 1 to indicate that the attachment has completed the specified operation and is now free to execute a new command.

Unit Check. This bit is set to 1 when an irregular program condition or equipment condition is detected by the attachment. Sense data in the attachment further defines the unit-check condition. Refer to "Data for a Sense Command" in this chapter for additional information.

Unit Exception. This bit is not used by the attachment; it is always 0.

Initial Status

Initial status is generated by the attachment in response to initial selection from the System/370. During the initial-selection sequence, the status is sent to the channel after the attachment receives a command.

Ending Status

When the attachment completes channel operations for a command, it sends ending status to the channel. Ending status indicates that the channel is now free for other operations.

Pending Status

When a status byte is awaiting transfer to the channel, it is called pending status. The attachment attempts to pass this status asynchronously to the channel. If the status byte is still pending when the next command is issued, it is passed to the channel as initial status, and the new command is not executed. In this case, the busy bit in the status byte is also set to 1.

System/370 Interface Disconnect

Under certain conditions, the System/370 channel can initiate an interface-disconnect sequence. The attachment responds immediately by terminating any operation in process. Normal ending status is presented to the System/370 channel.

If the disconnect occurs when the Series/1 is "connected" to the System/370, an exception interrupt is presented to the Series/1. If the two systems are not "connected," an attention interrupt is presented to the Series/1.

System/370 Reset

The System/370 reset, which is caused by either an I/O system reset or an I/O selective reset, causes a reset of the System/370 section of the attachment.

If the reset occurs when the Series/1 is "connected" to the System/370, an exception interrupt is presented to the Series/1. If the two systems are not "connected," an attention interrupt is presented to the Series/1.

	Normal status					
	Initial		Ending			
			Synchronous		Asynchronous	
System/370 command	Hex	Bits set to 1	Hex	Bits set to 1	Hex	Bits set to 1
Test I/O	*					
Write	00		08	CE	04	DE
Read Buffer	00		0C	CE, DE		
No-Operation	0C	CE, DE				
Sense	00		0C	CE, DE		
Erase/Write	00		08	CE	04	DE
Read Modified	00		0C	CE, DE		
Select	08	CE			04	DE
Diagnostic Write	00		08	CE	04	DE
Diagnostic Read	00		0C	CE, DE		
Erase All Unprotected	08	CE			04	DE
Subsystem Load Enable	0C	CE, DE				
Sense I/O	00		0C	CE, DE		

CE – Channel end
DE – Device end
* – Any pending status or 00

Chapter 11. Series/1–5250 Information Display System Attachment Feature

Purpose

The IBM Series/1–5250 Information Display System Attachment Feature allows the following display stations and printers to be locally attached to a Series/1 Processor:

- IBM 5251 Display Station, Models 1 and 11
- IBM 5252 Display Station, Model 1
- IBM 5256 Printer, Models 1, 2, and 3

Combinations of addressable stations can be connected to this attachment, with the following restrictions:

- Each 5252 counts as two addressable stations.
- No more than seven addressable stations may be connected to any one of the attachment's four twinaxial cables.
- The total number of addressable stations on all cables cannot exceed eight.
- The total length of twinaxial cable that attaches any work station cannot exceed 1500 meters (5000 feet).

This attachment supports the following features:

Feature	5251-1, 11	5252-1	5256-1, 2, 3
Keylock, display screen filter	X	X	
Typewriter keyboard layout (20 major language groups)	X	X	
Multinational character set	X	X	X
Cable-through	X	X	X
Magnetic stripe reader	X	X	
Spanish "n" w/tilde			X
Audible alarm, forms stands			X

Hardware Description

The 5250 Attachment feature is contained on two 4-wide by 6-high circuit cards, an attachment card and a driver/receiver (D/R) card, that are plugged into adjacent card sockets in either a Series/1 processor or an I/O expansion unit, where they connect directly to the Series/1 I/O channel. The attachment card should be plugged into the higher alphabetic socket; the driver/receiver card should be plugged into the lower alphabetic socket of the processor or I/O expansion unit. (The attachment card is on the right, and the driver/receiver card is on the left, as viewed from the front of the Series/1 unit.)

Note: Neither card may reside in a restricted voltage socket A on the Series/1 interface.

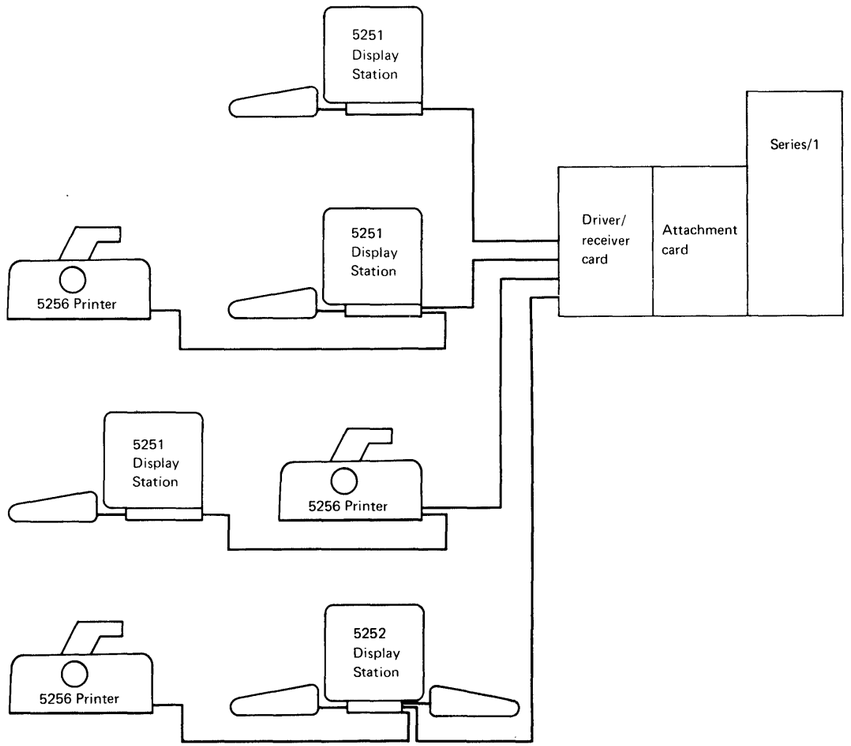
The attachment and D/R cards are connected by three SLT crossover cables in the W, X, and Y positions of both cards. The D/R card and the work stations are connected by a twinaxial cable assembly that contains four individual shielded twisted-pair cables. All four cables are terminated at one end by a single 2 x 12 Berg connector, and at the other end, each cable is terminated by a female twinaxial connector.

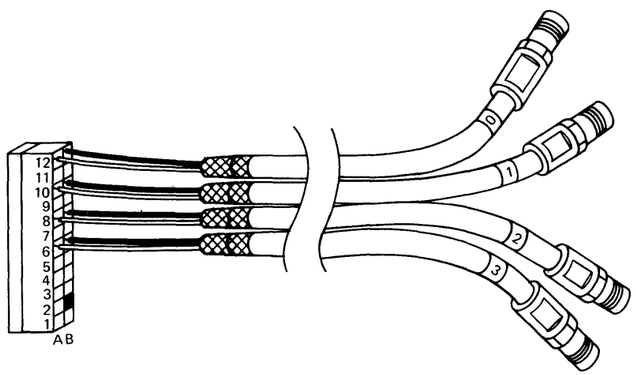
Each of the four cables can support up to seven addressable stations; however, the total number of addressable stations on all cables cannot exceed eight. (Each 5252 counts as two addressable stations.)

Note: Coaxial cable can be used instead of twinaxial cable, subject to the following restrictions:

- Special adapters must be used to connect the coaxial cable to the twinaxial cable assembly described above. (These adapters are available from IBM in the 5250 Information Display System Twinaxial/Coaxial Adapter kit.)
- The first work station on each port can be attached by coaxial cable not to exceed 600 meters (2000 feet).
- One additional work station can be attached by twinaxial cable not to exceed 30 meters (100 feet).

For additional cabling information, refer to *IBM 5250 Information Display System Planning and Site Preparation Guide*, GA21-9337.





Functional Description

The IBM Series/1—5250 Information Display System Attachment communicates with the Series/1 via the I/O channel. The attachment utilizes a single Series/1 device address and supports up to eight work stations by sub-addressing in the DCB for station-directed commands. The attachment performs the following major functions:

- Polls attached work stations.
- Receives and field checks operator keystrokes.
- Translates keystrokes to EBCDIC, using a translate table supplied during initialization.
- Transmits translated keystrokes to the CRTs for display.
- Handles all communications between the processor and the display stations.
- Provides input to the processor for data editing.
- Buffers print lines until the printer is able to receive new data.
- Provides retries to clear soft errors.

A set of attachment-directed commands is used to control station interrupt activity and to request interrupt and error status. The attachment supports cycle-stealing, command-chaining, and suppress-exception features of the Series/1 I/O architecture, but it is not a Series/1 IPL source. There is no default initialization state that would, by itself, require restrictions on the station configurations attachable to Series/1. This also means that no station can function as a default system console without attachment initialization. Attachment initialization is required prior to establishing logical connection to any of the stations.

The *attachment card* contains all the interface logic to the Series/1. This card presents a single unit load to the Series/1 I/O interface, and it services and controls the work stations for any workload that does not require processor service.

The *driver/receiver card* contains the logic necessary to adapt the microcontroller on the attachment card to the local electrical levels and timings of the attached work stations. This card is not connected to the Series/1 I/O interface signal lines except for the three lines required to receive and propagate the poll.

Attachment Card

The attachment card can be divided into the following functional units (refer to the figure):

(A) *Series/1 Interface*

This block represents all the logic required to interface to the Series/1 I/O channel.

(B) *Controller*

The controller is the primary functional unit of the attachment feature; it controls the communication between the Series/1 and the serial interface to the work stations. Hardware interrupts from the D/R card divert the controller from the mainline program to poll the work stations at a predetermined interval (about 30 milliseconds).

The controller I/O structure consists of three primary buses:

1. Controller Data Bus Out (CDBO) — eight data lines. All outbound data is sent from the controller on this bus.
2. Controller Data Bus In (CDBI) — eight data lines. All inbound data is sent to the controller on this bus.
3. Controller Address Bus Out (CABO) — eight command lines. All commands are sent from the controller on this bus.

(C) *Controller Data Storage*

This block represents 10K bytes of direct-access controller storage and the associated control logic.

(D) *Microcode (control and diagnostic programs)*

This block represents 8K bytes of read-only storage that houses the microcode to control the Series/1 interface and some diagnostic programs to check the operation of the attachment card. These diagnostic programs facilitate fault isolation between the two feature cards.

(E) *Storage Controls*

This section controls the flow of data out of the controller and into controller data storage (C).

(F) *Command Decode*

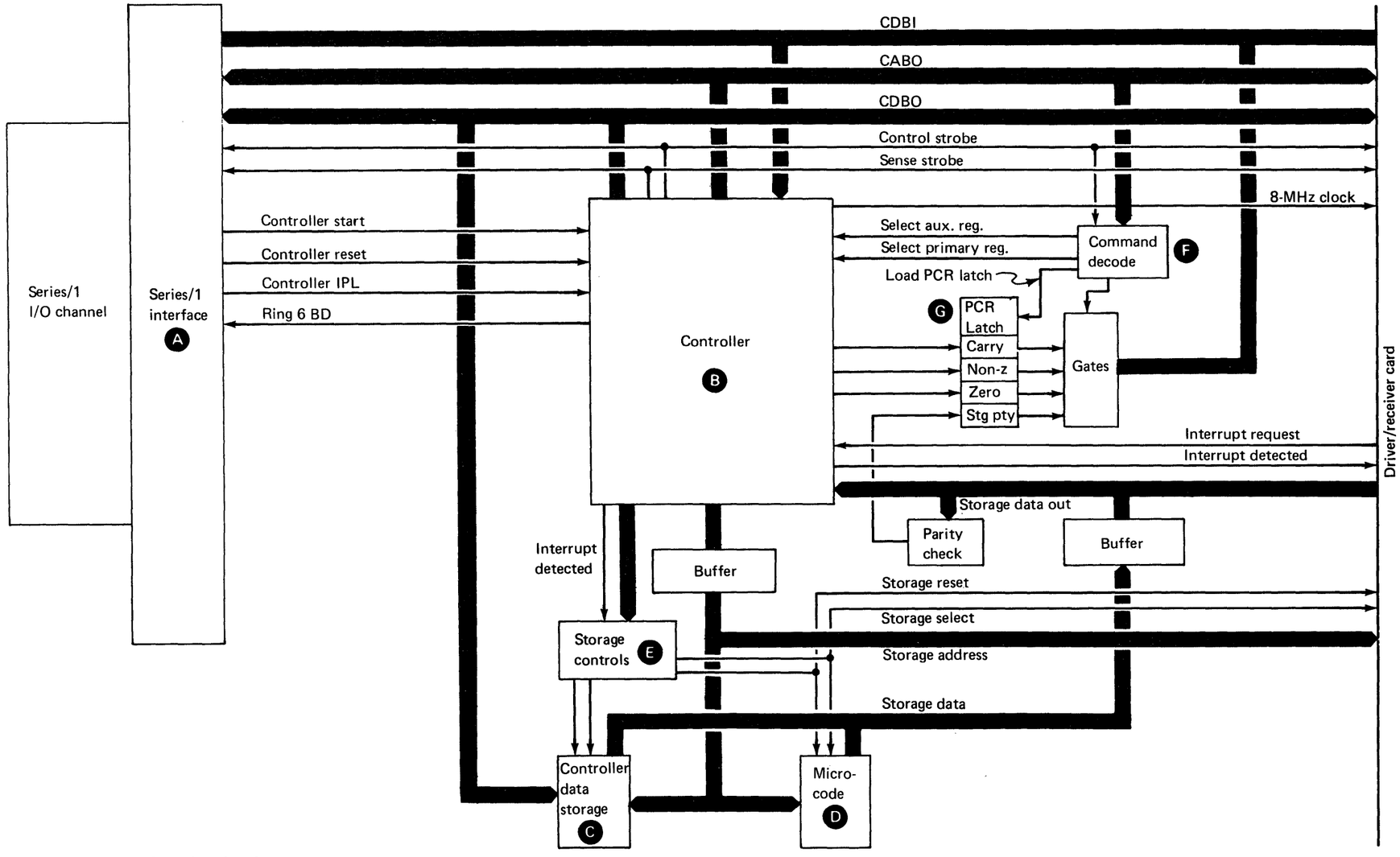
This section decodes the commands on the CABO bus. These commands control the miscellaneous logic on the attachment card. Two signals from this section are sent to the controller to select either the primary or auxiliary stack registers.

(G) *Program Condition Register Latches*

This block represents the latches that store the status of the controller program condition register (PCR) and the storage parity check latch. The PCR latches are loaded when the controller receives an interrupt request from the microinterrupt timer. The contents of these latches can be interrogated by the controller. Storage parity is checked only on storage reads. When a storage parity check occurs, the controller does not stop, nor is it interrupted by the microinterrupt timer. The latch output is available for interrogation and further action by the microcode, and the latch can also be reset by the microcode.

Miscellaneous Logic

The attachment card also contains the buffers necessary to power up the controller lines to be sent over the crossover cables to the D/R card.



Attachment card functional units

Driver/Receiver Card

The driver/receiver (D/R) card can be divided into the following functional units (refer to the figure):

(A) Controller Control Storage

This block represents 24K bytes of read-only storage. The address for this block of storage starts at hexadecimal 2000 and ends at hexadecimal 7FFF.

(B) Repower

The storage output from (A) is repowered in (B) and then sent to the attachment card.

(C) Controller Command Decode

This logic decodes the commands on the Control Address Bus Out (CABO).

(D) Microinterrupt Timer

The microinterrupt timer is a 5-bit decrementing timer that is loaded with a value from CDBO bits (0–4) and is decremented by a free-running 1-kHz clock. The signal from this timer is generated by dividing the frequency of an 8-MHz signal, which originates on the attachment card.

When the timer has decremented to 0 and if the enable microinterrupt latch in the command decode logic is set, the microinterrupt signal to the controller goes active. The timer is set to some value, such as 30 milliseconds, which causes the 'interrupt request' signal to go active every 30 milliseconds. This signal forces the controlled microprogram to some microroutine, such as a poll, which, in turn, checks each terminal keyboard for operator keystrokes.

(E) Multiplexer

This logic multiplexes data and status from different parts of the serial interface to the controller data bus in (CDBI) bus. The multiplexer gates data to the CDBI bus in response to the controller commands. These commands are decoded and sent to the multiplexer from the controller command decode logic (C).

Note: Serial Interface to Twinaxial Cables

Series/1 communicates with the work stations through the work station serial interface. This interface includes the serializer/deserializer (SERDES) (F), SERDES control (G), modulator/demodulator (H), cable address register (J), and driver/receiver circuits (K), (L), (M), and (N).

(F) Serializer/Deserializer (SERDES)

The serializer/deserializer (SERDES) is a 16-bit shift register that is loaded with parallel data. The parallel outputs from the SERDES are put into the CDBI buffers when 16-bits of data have been shifted into the SERDES on a receive operation. On a receive operation, 'serial in data' to the SERDES is generated from 'receive binary data.' On transmit operations, the SERDES is loaded in parallel from the CDBO bus by the controller output instruction, and 'serial out data' to the SERDES control becomes 'transmit binary data'.

(G) SERDES Control

The 'SERDES control' signals from the controller command decode logic (C) control the serial interface latches (located in the SERDES control). This is accomplished by setting or resetting transmit and receive latches and by setting or resetting a 'go' latch, which synchronizes the controller with the serial interface. The 'go' latch supplies SERDES status to the controller on the CDBI bus.

(H) Modulator/Demodulator

This logic serves as the modulator/demodulator for signals to and from the twinaxial lines.

(J) Cable Address Register

This 4-bit register is used to select one of four twinaxial driver/receivers for transmit or receive operations. This register is loaded from the CDBO bus.

(K) Driver/Receiver

There are four driver/receivers (K) on the D/R card — one for each cable attached to the system.

(L) Receiver Select

This logic continuously monitors the cable selected by the cable address register for serial receive data. On receive operations:

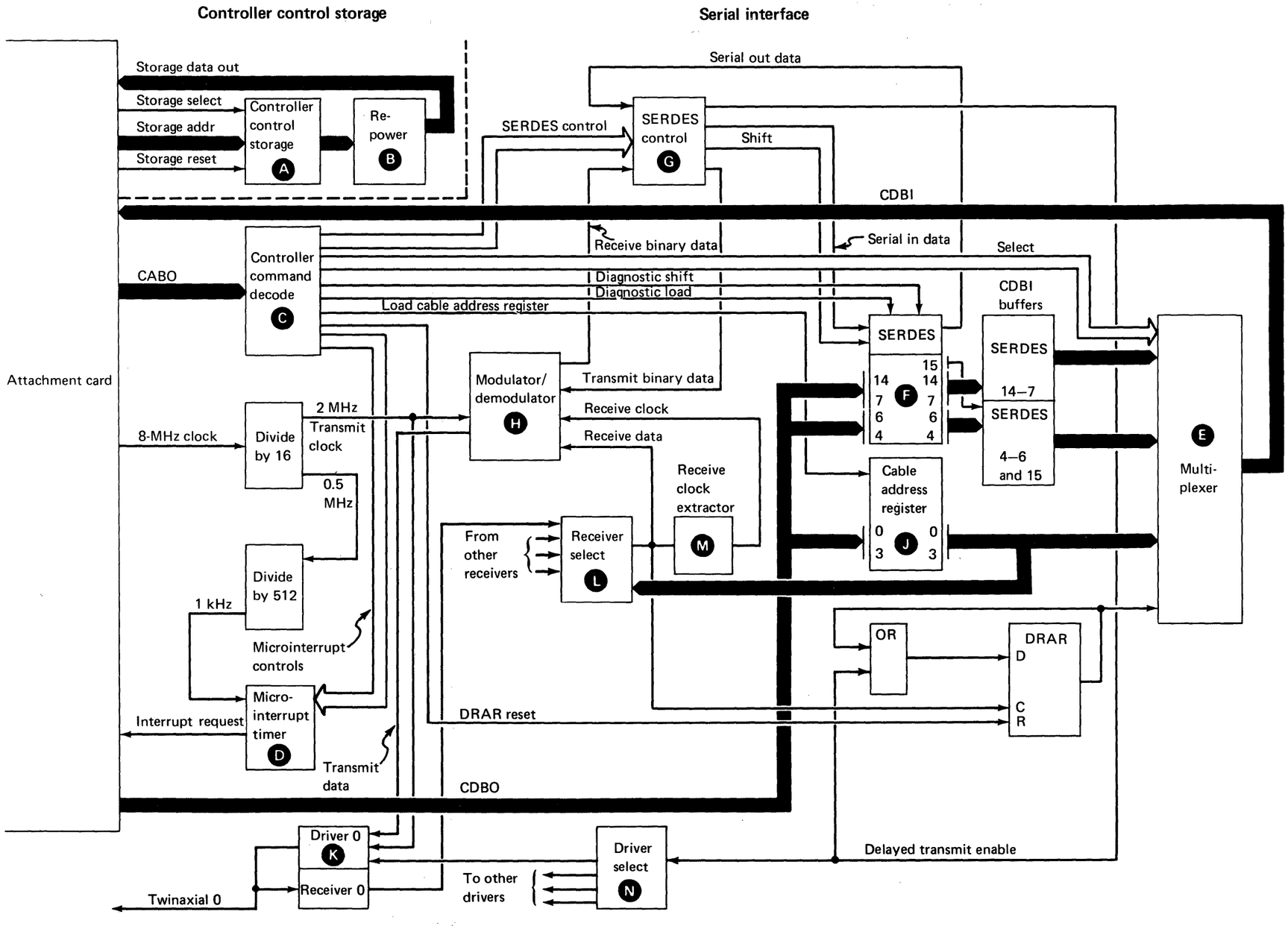
1. The 'receive data' output from receiver select is sent to the modulator/demodulator (H) and receive clock extractor (M).
2. 'Receive clock' from the extractor is sent to the modulator/demodulator.
3. The modulator/demodulator generates 'receive binary data' and sends it to the SERDES control logic.

(M) Receive Clock Extractor

'Receive data' is sent to this extractor, which then sends 'receive clock' to the modulator/demodulator.

(N) Driver Select

Outputs from the driver select logic are used on transmit operations. These signals are gated by the 'transmit enable' signals from the SERDES control. A selected driver (selected by cable address register (J)) uses 'transmit clock' and 'transmit data' to transmit serial data to the work station.



Driver/receiver card functional units

Cable Connections

This section describes the tab connections to the attachment and driver/receiver cards. Because the connections to Series/1 I/O channel are standard, they are not listed here.

There are three groups of connections to the attachment and driver/receiver (D/R) cards (other than Series/1 I/O channel):

- Three SLT crossover cables are used to connect the attachment and D/R cards. These cables are plugged into top card connectors W, X, and Y. (Pin assignments are the same on both cards.)
- Top card connector Z on the attachment card is used for test points.
- Top card connector Z on the D/R card provides the connections from the twinaxial cables to the work stations.

Connector pin assignments for these cables are given in the tables on this page.

Crossover connectors W, X, and Y

Signal name	Connector and pin
–Storage data bit 0	W23
–Storage data bit 1	X29
–Storage data bit 2	X02
–Storage data bit 3	W06
–Storage data bit 4	Y06
–Storage data bit 5	Y04
–Storage data bit 6	X33
–Storage data bit 7	X32
–Storage data bit parity high	X12
–Storage data bit 8	W32
–Storage data bit 9	W30
–Storage data bit 10	X31
–Storage data bit 11	W33
–Storage data bit 12	X30
–Storage data bit 13	X10
–Storage data bit 14	X24
–Storage data bit 15	W31
–Storage data bit parity low	Y05
+XSAR bit 0	X11
+XSAR bit 1	Y03
+XSAR bit 2	X09
+XSAR bit 3	X23
+SAR bit 0	Y22
+SAR bit 1	Y02
+SAR bit 2	Y24
+SAR bit 3	X05
+SAR bit 4	Y29
+SAR bit 5	Y12
+SAR bit 6	Y33
+SAR bit 7	Y13
+SAR bit 8	Y07
+SAR bit 9	Y26
+SAR bit 10	Y25
–Controller ABO bit 0	X06
–Controller ABO bit 1	X07
–Controller ABO bit 2	X26
–Controller ABO bit 3	X27
–Controller ABO bit 4	X22
–Controller ABO bit 5	Y23
–Controller ABO bit 6	X28
–Controller ABO bit 7	X04
(continued)	

Crossover connectors W, X, and Y (continued)

Signal Name	Connector and pin
–Interrupt detected	W04
–Interrupt request	W24
+Write storage high byte	W22
+Write storage low byte	W03
–Control strobe	W02
–Sense strobe	W12
–Controller reset	X03
+Ring 1 BD	W10
–Controller DBO bit 0	Y10
–Controller DBO bit 1	Y30
–Controller DBO bit 2	Y09
–Controller DBO bit 3	Y11
–Controller DBO bit 4	Y31
–Controller DBO bit 5	Y32
–Controller DBO bit 6	Y28
–Controller DBO bit 7	X25
–Controller DBO parity	Y27
+8-MHz osc	W05
–ROS reset	X13
–D/R ROS select	W27
–Controller DBI bit 0	W28
–Controller DBI bit 1	W11
–Controller DBI bit 2	W29
–Controller DBI bit 3	W25
–Controller DBI bit 4	W13
–Controller DBI bit 5	W09
–Controller DBI bit 6	W26
–Controller DBI bit 7	W07
Ground	W08
Ground	X08
Ground	Y08

Attachment card top card connector Z

Signal name	Connector and pin
–Op reg bit 0	Z23
–Op reg bit 1	Z22
–Op reg bit 2	Z32
–Op reg bit 3	Z02
+ALU out bit 0	Z24
+ALU out bit 1	Z05
+ALU out bit 2	Z06
+ALU out bit 3	Z26
+Ring 5 BD	Z04
+Write nibble	Z31
–Select regs	Z12
+Select nibble via A-field	Z13
+Select nibble via B-field	Z09
+Force stack 1 address	Z10
+Wait trigger	Z27
–Select aux regs	Z25
+Storage parity check latch	Z11
–Allow controller IPL	Z29
–Controller single cycle	Z28
–Controller reset	Z07
–Start controller	Z33
–Stop on storage parity check	Z30
+5 volts	Z03
Ground	Z08

Driver/receiver card top card connector Z

Signal or cable name	Connector pin	Test pin
Cable 0B (copper conductor)	12B	11B
Cable 0Y (tinned conductor)	12A	11A
Cable 1B (copper conductor)	10B	9B
Cable 1Y (tinned conductor)	10A	9A
Cable 2B (copper conductor)	8B	7B
Cable 2Y (tinned conductor)	8A	7A
Cable 3B (copper conductor)	6B	5B
Cable 3Y (tinned conductor)	6A	5A
–Delayed transmit enable (DXE)		1B
–Receive data		1A
Ground		3A
Ground		3B
Ground		4A
Ground		4B
No signal		2A
Blank slot		2B

Programming Input/Output (I/O) Operations

Data Transfer Operations

Data is transferred between the processor and the 5250 Attachment in a parallel operation (16 data bits plus 2 parity bits). The number of data words transferred and the direction in which they move is determined by the I/O command. The I/O command also determines whether data is transferred to or from processor storage under direct program control (DPC) only, or under direct program control and cycle-steal mode.

Direct Program Control (DPC)

Under direct program control, only one word of data moves to or from processor storage at a time. After moving the data, the processor continues processing other instructions. Moving data under DPC does not cause interrupt requests.

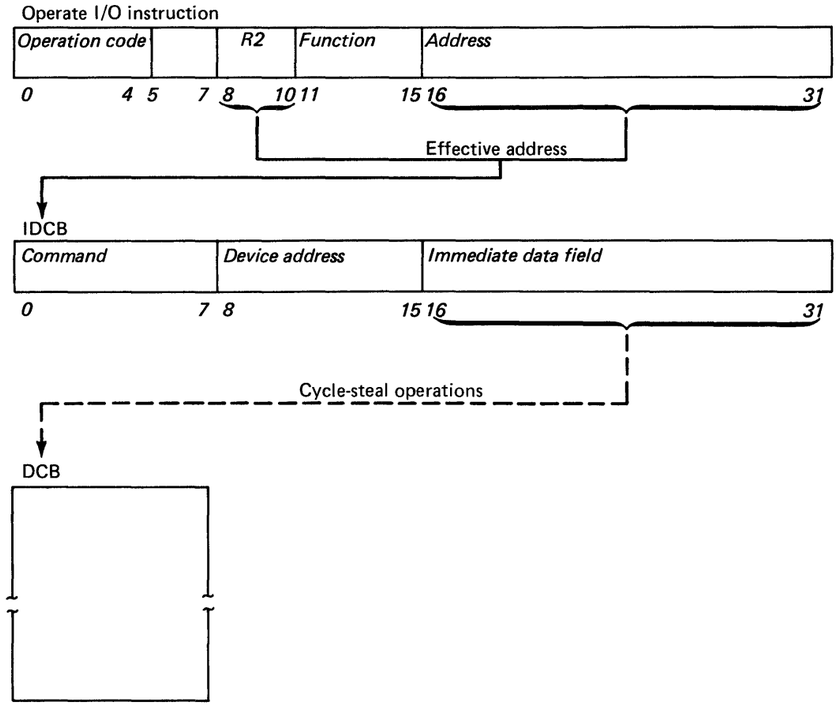
Cycle-Steal (CS)

When data is moved to or from processor storage by stealing storage cycles (cycle-steal mode), processing and I/O operations are overlapped. Overlapping multiple data transfers allow the processor to execute other instructions while the 5250 station is performing I/O operations.

Operate I/O Instruction

The following description is an overview of the Operate I/O instruction. For a more detailed description, refer to the appropriate processor description manual listed in the Preface of this publication.

All input/output operations from the processor to the 5250 Attachment are initiated by an Operate I/O instruction. An address field (bits 16–31) and the R2 field (bits 8–10) in the Operate I/O instruction (see figure) point to a processor storage location containing an immediate device control block (IDCB).

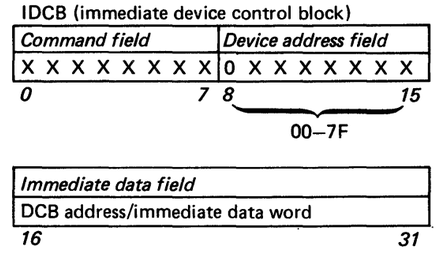


Operate I/O instruction

Using the IDCB

The IDCB is a two-word block of storage, that contains the device directed I/O commands. Before issuing the I/O instruction for an operation, the command field of the IDCB (Bits 0–7) must be set, along with a device address (bit 8–15), and any field of immediate data required by the command in the IDCB (bits 16–31). The information specified in the immediate field depends on the command to be performed. The device address of the 5250 Attachment can be one of 128 (0–127) possible device addresses. This address is determined by the device address field of the IDCB. Bit 8 of this field must be 0.

An immediate device control block (IDCB) is required for every I/O command issued to the 5250 Attachment. The format of the IDCB is shown in the figure below. Before issuing an I/O instruction, an I/O command must be stored in the associated IDCB. The immediate data field of the IDCB should contain either a data word or a DCB address. I/O commands that execute under direct program control require a data word, while the commands that execute in cycle-steal mode require a DCB address.



IDCB format

Input/Output Commands and 5250 Attachment Operations

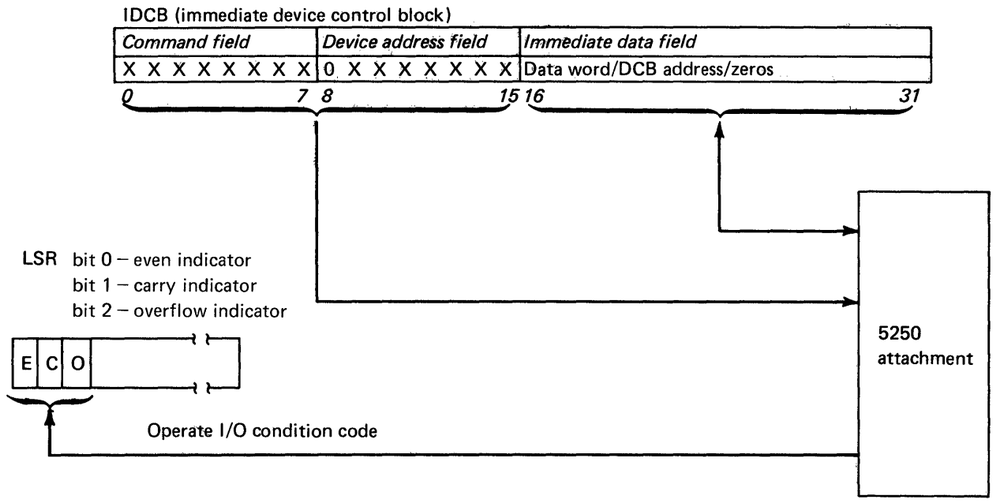
The I/O command stored in the IDCB determines whether a single word of data is transferred under direct program control only, or if following a direct program control operation, additional words of data are to be transferred to the processor under cycle-steal mode. The 5250 Attachment responds to the following I/O commands defined in the command field (bits 0–7) of the IDCB:

Direct Program Control (DPC)

1. Prepare
2. Device Reset
3. Read Device ID

Cycle-Steal Mode (CS)

1. Start I/O
2. Start Control Store
3. Start Cycle Steal Status



Command execution under DPC

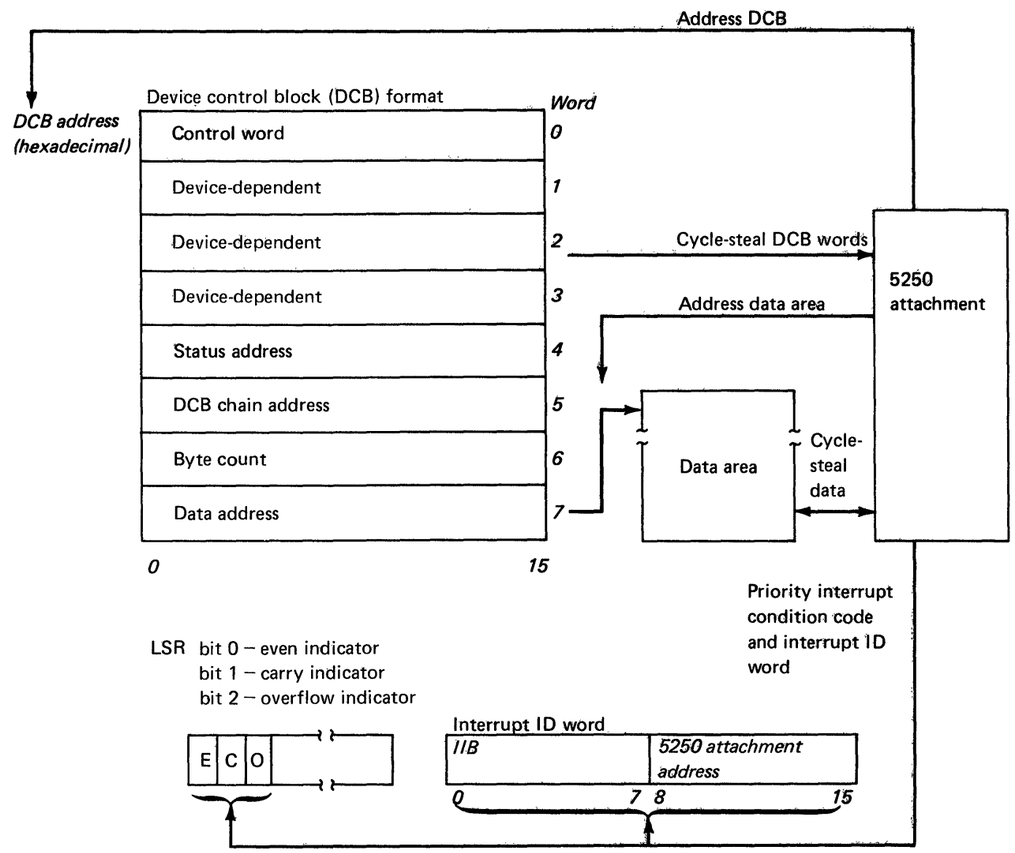
Command Execution Under DPC Mode

When the 5250 Attachment executes a Prepare, Device Reset, or Read ID command, a word of data is moved to or from the immediate data field of the IDCB in processor storage. These commands do not cause interrupt requests. After execution of the command, the 5250 Attachment reports a condition code that indicates whether the I/O operation succeeded or failed. Processing operations are halted while the I/O operation is in progress. The following figure shows command execution under DPC mode.

Command Execution in CS Mode

The Start I/O, Start Control Store, and the Start Cycle Steal Status commands are interrupt-causing commands, and move data under both direct program control and cycle-steal mode. When the 5250 Attachment receives and accepts any of these commands, it reports a condition code to the processor and begins command execution. The processor continues with other operations while the 5250 Attachment is "busy" with the I/O operation. When the I/O operation is completed, the 5250 Attachment sends an interrupt request to the processor. At interrupt presentation time the 5250 Attachment reports a condition code and transfers an interrupt identification word containing status information to the processor.

The immediate data field of an IDCB containing a Start I/O, Start Control Store, or a Start Cycle Steal Status command must point to a device control block (DCB). The DCB must contain the control information and device parameters that are required to execute an I/O operation in cycle-steal mode. The following figure shows command execution in cycle-steal mode.



Note: DCB format is shown for a Start command. The DCB format for a Start Cycle-Steal Status command appears later in this chapter.

Command execution in cycle-steal mode

Using the DCB

A device control block (DCB), comprised of eight contiguous words in processor storage, must be reserved for every I/O operation that moves data in cycle-steal mode. All Start commands, Start Cycle Steal Status commands, and operations included in a DCB command chaining sequence require a separate DCB. Device parameters that define and control the I/O operation must be stored in each DCB.

DCB (device control block)

Word	
0	Control word
1	Device-dependent
2	Device-dependent
3	Device-dependent
4	Status address
5	DCB chain address
6	Byte count
7	Data address

0 15

5250 Attachment Commands

The 5250 Attachment executes three classes of device-directed Operate I/O instructions. The bits are set in the command field of the IDCB as follows:

Meaning	Command field	Class
Prepare	01100000	Control
Device Reset	01101111	Control
Read Device ID	00100000	Read status
Start I/O	01110000	Start
Start Control Store	01110010	Start
Start Cycle Steal Status	01111111	Start

The 5250 Attachment also executes a channel directed command called Halt I/O. All other commands are invalid and cause either an immediate command reject, or an exception interrupt, with a delayed command reject set in the immediate status byte (ISB).

Prepare

Before the 5250 Attachment can execute interrupt-causing commands, it needs interrupt parameters. These parameters, stored in the IDCB immediate data field associated with a Prepare command, contain the level on which the 5250 Attachment is to interrupt (bits 27–30), and an interrupt enable bit (bit 31). These bits are transferred to the 5250 Attachment upon execution of Prepare commands. If the I-bit (bit 31) equals 1, the 5250 Attachment can interrupt; if the I-bit equals 0, it cannot. The Prepare command operates under DPC and does not cause an interrupt.

IDCB (immediate device control block)

Command field	Device address field
0 1 1 0 0 0 0 0	0 X X X X X X X
0 7	8 15
60	00–7F

Immediate data field		
Zeros	Level	I
16 26	27 30	31

Device Reset

Execution of Device Reset, Halt I/O, and System Reset commands results in the following:

1. The device enters the busy after reset state.
2. All pending interrupts are reset. The prepare register is unchanged for a Device Reset or Halt I/O; it is reset on a System Reset.
3. Cycle-stealing operations are terminated immediately. The residual address may be indeterminate, and the residual byte count is reset. The residual address and residual address key are unchanged.
4. Device-dependent cycle-steal status is reset.
5. The 5250 Attachment is disarmed. If the 5250 Attachment remains in the initialized state, station control bytes are set to X'30', the stations are placed in free key mode, and format tables and display attributes are reset to reflect free key mode of the stations.
6. The 5250 Attachment exits the initialized state if the reset occurs during the execution of any Start Control Store command with an IDCB modifier of 0010, or, if the last previously executed command was a Start Control Store command. Otherwise, the initialized state of the device is unaffected.
7. The contents of 5250 Attachment storage are affected. However, the storage remains valid with respect to parity. The 5250 Attachment remains initialized if the 5250 Attachment was in the initialized state upon execution of the reset and the last command executed was not a Start Control Store command.
8. The 5250 Attachment self checks are performed before exiting the busy-after-reset state.

The command code and device address supply all needed information. Although the immediate data field is not used or checked, these bits should be set to zero. The Device Reset command operates under DPC and does not cause an interrupt.

IDCB (immediate device control block)

Command field	Device address field
0 1 1 0 1 1 1 1	0 X X X X X X X
0 7	8 15
6F	00–7F

Immediate data field
Not used
16 31

Read Device ID

The Read Device ID command transfers the device ID word for the 5250 Attachment into the immediate data field of the immediate device control block (IDCB) associated with that command. If the 5250 Attachment is busy, or if an interrupt request is pending, condition code 1 is returned. The Read Device ID command operates under DPC and does not cause an interrupt.

IDCB (immediate device control block)

Command field	Device address field
0 0 1 0 0 0 0 0	0 X X X X X X X
0 7	8 15

Immediate data field
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
16 31

The device ID word that is transferred is the following:

Immediate data word			
0 0 0 0	0 1 0 0	0 0 0 1	0 1 1 0
0 3	4 7	8 11	12 15

This is equivalent to X'0416'.

Start Commands Overview

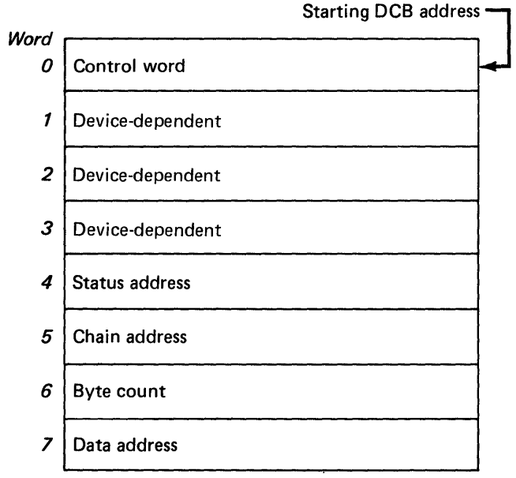
During the Start command, bits 0–15 of the data word portion of the IDCB (immediate device control block) are transferred into the address register of the device. This address defines the location of the DCB (device control block) in processor storage that the 5250 Attachment will fetch.

Subsequent action depends on the modifier field of the IDCB and the control parameters found in the DCB. The attachment will fetch the DCB, using address key 0.

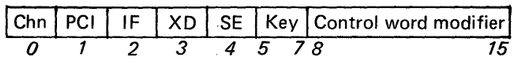
All Start commands cause the 5250 Attachment to go busy and remain busy until the acceptance of the end interrupt signaling command completion.

DCB Format.

The DCB contents are defined as follows:



Word 0—Control Word. This 16-bit word defines the attributes of the DCB. The format is:



Chn — Chaining flag—This bit indicates a DCB command chaining operation. After completing the current DCB operation, the attachment does not interrupt, but fetches and executes the next DCB in the chain. The next DCB is pointed to by the address in word 5 of the current DCB.

PCI — Reserved—This bit must be set to 0.

IF — Input flag—This bit must be set to 1 if the direction of data transfer is into processor storage.

XD — Reserved—This bit must be set to 0.

SE — Suppress Exception—When this bit is supported by the DCB and set to 1, certain exception conditions denoted in the specification are suppressed and reported in the residual status block (RSB) pointed to by the address in word 4.

Key — Cycle-steal address key—This is a three-bit key presented by the 5250 Attachment during data transfer. It is used to ascertain storage access authorization.

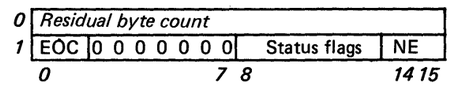
For all DCBs except Start Cycle Steal Status command DCBs, the following specifications apply: If the chn bit is on and the DCB does not support chaining, an exception interrupt occurs with DCB specification check set in the ISB. If the PCI or XD bits are on, an exception interrupt occurs with DCB specification check set in the ISB. If the SE bit is on and the DCB does not support suppress exception, an exception interrupt occurs with DCB specification check set in the ISB. Support of chaining and suppress exception will be indicated in the description of each DCB to follow. The Start Cycle Steal Status command has its own unique DCB specification with regard to its control word.

Control Word Modifier. Bits 8–15 are used to define operations for specific Start commands and are device-dependent. See each Start I/O command for specific definition. If these bits are not valid for the type of Start command, an exception interrupt will occur with DCB specification check set in the ISB.

Words 1, 2, 3—Device-Dependent. These words are used with Start commands and are dependent on the type of Start command. DCB words, which are specified herein as device-dependent and not used, are reserved and should be set to zero to avoid future code obsolescence. Additionally, the residual status block (RSB) should not be stored into their locations.

Word 4—Status Address. When the SE bit of the DCB that supports SE is set to 1, word 4 of the DCB contains the address of the residual status block (RSB) that will be stored in storage upon completion of execution of the command. If the status address is odd and the SE bit is specified, an exception interrupt occurs with DCB specification check set in the ISB. If the SE bit is off, word 4 is fetched, but is not used or checked, and an RSB is not posted.

The residual status block (RSB) contains information relative to suppressed exception conditions that may have occurred during execution of the command. It is stored using address key 0. The format of the residual status block is as follows:



The status address points to word 0 of the residual status block.

Residual byte count—word 0 of the RSB contains the residual byte count.

EOC — End of Chain. This bit is stored in the last RSB prior to presenting an interrupt.

NE — No Exception. This bit, if on, indicates that no suppressible exception occurred. This bit, if off, indicates that a suppressible exception occurred; the status flag field will be non-zero. Bit significance of the status flags are:

- 8 Presented as zero
- 9 Presented as zero
- 10 Short incorrect length record (ILR) suppressed
- 11 Presented as zero
- 12 Presented as zero
- 13 Presented as zero
- 14 Presented as zero

Certain types of short incorrect length records are type-3 suppressible exceptions; that is, they suppress exceptions and terminate data transfers. If this exception occurs, the reporting proceeds according to the following table:

Type-3 SE reporting table

DCB		RSB settings			
chn	**SE**	**EOC**	**NE**	**Status flag**	**Interrupt type action**
0	0	N/A		N/A	Exception; RSB not posted
0	1	1	0	Non-0	Device end with permissive device end bit set in IIB. Post RSB prior to interrupt
1	0	N/A		N/A	Exception; RSB not posted. Terminate operation; terminate chain
1	1	0	0	Non-0	None; terminate current DCB, but continue chaining. Post RSB prior to next DCB fetch

If SE is supported by the DCB, but the suppressible exception does not occur or cannot be reported in executing the operation specified then:

- If the SE bit is on, the RSB is still posted, the EOC bit reflects whether the DCB is the last DCB in the chain, the NE bit is 1, and the status flags are all 0's. Normal chaining is executed, depending upon the setting of the chn bit in the DCB.
- If the SE bit is off, the RSB is not posted. Normal device end interrupts or DCB chaining are executed, depending upon the setting of the chn bit in the DCB.

All other error types not designated as suppressible are nonsuppressible, and rank above all suppressible exceptions. If a nonsuppressable error occurs, the RSB is not posted and exception interrupt occurs; the operation and DCB chain terminate. Appropriate error conditions are posted in the ISB and cycle-steal status.

If an error occurs during the attempt to store the RSB itself, an exception interrupt occurs; however, the ISB reflects only the reporting of the exception that occurred during the attempt to store the RSB and not exception conditions suppressed by the RSB itself. The RSB that was attempted may be recovered from the cycle-steal status.

Word 5—Chain Address. This word contains the address of the next DCB in the chain to be fetched when the operation defined by the current DCB has completed successfully, and the chain flag is on in the current DCB. Suppressible exceptions allow chaining. Abnormal ending sequences that cause exception interrupts terminate chaining operations. If the chain address is odd and chaining is specified in the DCB, an exception interrupt occurs with DCB specification check set in the ISB. If chaining is not specified, word 5 is fetched, but is not used or checked.

Word 6—Byte Count. This 16-bit word contains an unsigned integer representing the count relative to the address pointer. The count is always specified in bytes and contains the count of the number of bytes to be transferred to or from Series/1 processor storage using the direction specified in the input flag (IF) bit in the DCB. If the byte count is zero, no data is transferred. If the byte count does not meet the constraints allowed for a particular operation, an exception interrupt will occur with DCB specification check set in the ISB.

Word 7—Address Pointer. A 16-bit word that contains an unsigned integer representing the starting storage address for data transfer. If the address pointer does not meet the constraints allowed for a particular operation, an exception interrupt occurs with DCB specification check set in the ISB.

Start I/O—IDCB Command 70

The 5250 Attachment executes the following Start I/O commands:

- Start Data
- Set Station Control Byte
- Read Station Interrupt Element and Arm
- Read Station Interrupt Element, Arm on Condition

These commands are identified by bits 8-15 of the DCB control word.

Start Data—Control Word Modifier X'00'

The Start Data command is a station-directed command used to transfer data to and from the 5250 stations. The format of the DCB for a Start Data command is as follows:

Word 0—Control Word. Bits 0–7 of the control word are described in "Word 0—Control Word" under "Start Commands Overview" in this chapter. Chaining and SE are supported with this command.

Bits 8–15 are the control word modifier and must all be set to zero to specify a Start Data command. If the 5250 Attachment is not initialized, the command is not executed. An exception interrupt is posted, with device-dependent status available set in the ISB.

Word 1. This word consists of two distinct byte fields: the station command modifier and the station address.

Byte 0 Station Command Modifier. Valid station command modifiers and their input flag bits for display stations are listed below:

Station command modifier		Input flag bit
X'A7', X'27'	Output Data Stream	0
X'02'	Save Tables	1
X'06'	Save Screen	1
X'42'	Read Input Fields	1
X'62'	Read Screen	1
X'33'	Turn on operator alert indicator	0
X'43'	Turn off operator alert indicator	0

Other commands provided within the output data stream itself are:

X'01'	Restore Tables
X'05'	Restore Screen
X'11'	Write Data
X'21'	Write Error
X'23'	Roll
X'40'	Clear Unit
X'50'	Clear Format Table

Data stream constructions provide for subchaining these display station commands under one output data stream command.

Note: X'27' is recommended for the output data stream command. The byte count specified in the DCB for data stream commands must include the entire data stream content, including control, data, and escape characters.

Valid station command modifiers and their input flag bits for the printer stations are listed below:

Station command modifier		Input flag bit
X'A7', X'27'	Output Data Stream	0
X'40'	Clear Unit	0

Print information is provided by means of the output data stream and consists of control characters, which are the SNA character string (SCS) codes in the range of X'00' to X'3F'.

Note: The byte count specified in the DCB for the printer data stream command must include all control and print characters of the data stream.

If the station command modifier is not one listed above or if the input flag bit in the DCB control word is not in agreement with the station command modifier with respect to the direction of data transfer, a DCB specification check results. The DCB byte count specifications with each of the station command modifiers are shown in the following list. Violation of these specifications results in a DCB specification check.

Display Stations

X'27', X'A7'	The byte count must be greater than zero.
X'02', X'06'	The byte count must be greater than zero.
X'42', X'62'	The byte count must be greater than zero.
X'33', X'43'	The byte count is not used or checked for these station commands.

Printer Stations

X'27'	The byte count must be greater than zero and must be less than or equal to 256.
X'40'	The byte count is not used or checked.

Byte 1 Station Address. Bits 0–7 are the station address field, which consists of two parts. Bits 0-3 are the cable address, and bits 5-7 correspond to the station address on that cable. Bit 4 is reserved and must be zero. The cable address is binary coded and must not exceed the value 3. The station address is also binary coded and must not exceed the value 6. If these conditions are not met, or if the station address does not match a valid station address entry (loaded into the 5250 Attachment during initialization), a DCB specification check results.

Words 2–3. These words are fetched by the 5250 Attachment, but are not used or checked.

Word 4—Status Address. Refer to "Word 4—Status Address" under "Start Commands Overview" in this chapter.

Word 5—Chain Address. Refer to "Word 5—Chain Address" under "Start Commands Overview" in this chapter.

Word 6—Byte Count. The byte count may be even or odd. Incorrect length record (ILR) may be reported to this command.

Word 7—Data Address. This address may be odd or even.

Exceptions Causing Incorrect-Length Record (ILR) Reporting

An ILR is an exception occurring after the data transfer associated with command execution begins, and is an error caused by a mismatch of the byte count with the amount of data transferred. The latter is defined by the amount of data implied by the format tables for the station in effect (pre-loaded) during command execution, or delimiters of data length defined in the block of data being transferred. A suppressible short ILR is reported if the residual byte count has not been exhausted and all of the defined data has been transferred successfully. Successful transfer of the data is contingent upon considerable checking of the data by the 5250 Attachment, using data from pre-loaded format tables and monitoring of the data for correct delimiters and proper sequences; therefore, no exception settings in the cycle-steal status are implied. If the SE bit is on and a suppressible short ILR occurs, the residual status block is the mechanism used to convey the residual byte count, RSB word 1 will have the Short ILR suppressed bit set and the NE bit will be zero. If the SE bit is off, and a suppressible short ILR occurs, an exception interrupt occurs. The ILR bit is set in the ISB, as is the device-dependent status available bit, the latter indicating that the residual byte count is available in the cycle steal status. The residual byte count is greater than zero and less than or equal to the byte count in the DCB, and is a useful delimiter of the data transferred for recovery purposes.

A nonsuppressible short ILR is an exception condition where the residual byte count is not zero and the data has not been successfully transferred, which implies that there are station-related exception settings in the cycle-steal status. The residual byte count is relevant to recovery. When a nonsuppressible short ILR occurs, an exception interrupt occurs. The ILR and device-dependent status bits are set in the ISB.

The ILR bit in the ISB is not set when the residual byte count is zero and there are exception settings in the cycle-steal status. Only device-dependent status available is set in the ISB. This is because station directed commands use inherently self-defining data, either in preloaded format tables or in data streams. The residual byte count in this context simply becomes a transfer delimiter used by 5250 Attachment checking of the data stream itself, and may cause station-related exception settings in the cycle-steal status, such as the data stream reject bit in the station operation checks byte. The original byte count in the DCB may be helpful in recovering from such situations.

Set Station Control Byte—Control Word Modifier X'04'

The Set Station Control Byte command is used to set a value of the station control byte into the 5250 Attachment for the station addressed in the DCB. The armed state of the 5250 Attachment, described later in "Read Station Interrupt Element and Arm Commands," is not affected by this command.

The DCB format is as follows:

Word 0—Control Word. Refer to "Word 0—Control Word" under "Start Commands Overview" earlier in this chapter.

The input flag bit must be zero; otherwise, a DCB specification check results. Chaining and SE are supported.

Bits 8-15 are the control word modifier and are set to X'04' to specify a set station control byte command. If the 5250 Attachment is not initialized the command is not executed. An exception interrupt occurs with device-dependent status available set in the ISB.

Word 1. The word consists of two distinct parts: the station control bytes and the station address.

Byte 0—Station Control Byte. The station control byte format for display stations is defined as follows:

Bit 0—Low Priority Attention ID (AID) Enable. This bit, if off, masks all station attention interrupts caused by any AID code other than Attn, Sys Req/Enter, Help, Resource Available, Test Request, or 5250 Attachment-detected (X'FF') error AID code. This bit must be on for a station to cause an attention interrupt or respond with a station interrupt element during 5250 Attachment execution of a Read Station Interrupt Element command for the conditions it enables.

Any low priority AID that is generated from the keyboard is queued and causes the keyboard to lock, regardless of the state of the AID mask bit.

If a station interrupt element is not stored in Series/1 storage from this station prior to the execution of another command to the station, the AID may be lost and a residual attention interrupt may occur.

Bit 1—Reserved. Not used or checked by 5250 Attachment; should be set to 0 to avoid future code obsolescence.

Bit 2—High Priority Attention ID (AID) Enable. This bit, if off, performs the masking function of the low priority AID mask, and in addition masks all station interrupts caused by Attn, Sys Req/Enter, Help (from operator error mode), Resource Available, Test Request, and 5250 Attachment-detected (X'FF') AID code. This bit must be on for the station to cause a station attention interrupt or respond with a station interrupt element during 5250 Attachment execution of the Read Station Interrupt Element command for the conditions it enables.

Bit 3—Online. This bit must be on to execute any Start Data commands directed to this station, to report any station interrupts, or to respond with a station interrupt element during 5250 Attachment execution of the Read Station Interrupt Element command. This bit, if off, clears the station attention interrupt queue for the addressed station and holds the queue in a clear condition.

Bits 4–7—Reserved. Not used or checked by the 5250 Attachment; should be set to 0 to avoid future code obsolescence.

The station control byte format for printers is defined as follows:

Bit 0—Reserved. Not used or checked by 5250 Attachment; should be set to 0 to avoid future code obsolescence.

Bit 1—Quiescent. Printer data streams are transferred from the Series/1 processor to the 5250 Attachment by means of the Start Data command with a station command modifier of X'27'. These data streams are buffered in the 5250 Attachment, then transferred out to the printer for the print operations. A device end interrupt is posted to the Series/1 upon successful transfer of the data stream from the processor to the 5250 Attachment. Subsequent status on print operations and availability of print buffers are reported by means of the Series/1 attention interrupt mechanism and reading of the station interrupt element. Data stream transfers and print operations proceed asynchronously and in an overlapped manner with 5250 Attachment operations after the successful transfer of the printer data stream to the 5250 Attachment.

The setting of the quiescent bit determines the set of AID codes used to report print buffer availability to the program, and the state of the 5250 Attachment, print buffers, and printer after printer operations are completed. If the quiescent bit is on, the X'E3' (Printer End) and the X'FF' (Error Detected) AID codes may be reported to the program. After printer operations are completed, normally or otherwise, the printer is removed from 5250 Attachment poll list until the appropriate ending AID code is reported to the program. When the AID code has been successfully reported, the 5250 Attachment places the printer back on the poll list. If the quiescent bit is off, X'E1', X'E2' buffer availability AID codes may additionally be reported to the program; the printer remains on the 5250 Attachment poll list.

The acceptance of Clear Unit command ties up all print buffers until the clear operation is successfully completed. Only the X'E3" availability AID code is reported in response to a Clear Unit command, regardless of the state of the quiescent bit.

Note: The value of the quiescent bit should not be changed while printer operations are in progress. (The program should ensure that a Printer End AID has been received and no further operations have been directed to the printer prior to changing quiescent bit values). Otherwise, the results may be unpredictable. The value of the quiescent bit does not take effect until a printer directed command is accepted subsequent to the execution of the Set Station Control Byte command that changed the quiescent bit.

Bit 2—AIDs Enable. This bit, if off, masks all station attention interrupts caused by an AID code from the printer including the 5250 Attachment-detected (X'FF') AID code. This bit must be on for the station to cause a station attention interrupt or respond with a station interrupt element during execution of Read Station Interrupt Element command for the conditions it enables.

If a station interrupt element is not stored in Series/1 storage from the printer prior to the execution of another command to the printer, the AID code may be lost and a residual attention interrupt may occur.

Bit 3—Online. This bit must on to execute any Start Data commands directed to the printer, to report any station attention interrupts, or to respond with a station interrupt element during execution of the Read Station Interrupt Element command. This bit, if off, clears the station attention interrupt queue for the addressed station and holds the queue in a clear condition.

Bits 4–7—Reserved. Not used or checked by 5250 Attachment; should be set to zero to avoid future code obsolescence.

Byte 1—Station Address. This byte has the same format as the station address field, DCB Word 1, byte 1 in the Start Data command.

Words 2–3. These words are fetched, but are not used or checked.

Word 4—Status Address. Refer to "Word 4—Status Address" under "Start Commands Overview" earlier in this chapter.

Word 5—Chain Address. Refer to "Word 5—Chain Address" under "Start Commands Overview" earlier in this chapter.

Words 6–7. These words are fetched, but are not used or checked.

Note: The execution of a Set Station Control Byte command with all enable bits set to zero causes station attention interrupts to remain queued in the 5250 Attachment, but they are masked.

Read Station Interrupt Element and Arm Commands—Control Word Modifier X'06' and Read Station Interrupt Element, Arm On Condition-Control Word Modifier X'07'

The Read Station Interrupt Element (RSIE) commands are used to read station interrupt elements (SIE), subject to the enabling bits in the station control bytes set in the 5250 Attachment and the byte count in the DCB.

A Station Interrupt Element (SIE) is an eight-byte block that completely describes a station-type attention interrupt. For the purposes of this description, an "active" SIE is an element that requires some form of Series/1 processing. The program may allocate up to eight 8-byte "areas" in Series/1 storage where the the SIEs will be stored, depending upon how many SIEs the Series/1 program is designed to process for each RSIE command. The number of "areas" is specified by the byte count of the DCB. When the RSIE command is executed, SIEs are stored in contiguous "areas," starting from the address specified in the address pointer field in the DCB.

The active SIEs correspond to stations requiring service. If all allocated areas are filled with SIEs and the number of areas allocated is less than the number of stations, more stations may need servicing. Those pending SIEs that are not processed by the Series/1 remain queued in the 5250 Attachment. The SIEs are stored in order and correspond to an ascending, but not necessarily contiguous, order of station addresses, starting at any valid station address, and wrapping over the set of valid station addresses. On any given execution of the RSIE command, station addresses may appear more than once in the SIEs stored. However, each multiple appearance of a particular station address implies that a complete round of the stations for pending SIEs was completed.

The DCB format for Read Station Interrupt Element commands is as follows:

Word 0—Control Word. Refer to "Word 0—Control Word" under "Start Commands Overview" earlier in this chapter.

The input flag (IF) bit must be on because this command is always an input operation; otherwise a DCB specification check results. Chaining and SE are supported with these commands.

Bits 8–15 are the control word modifier bits and must be set to X'06' to specify an RSIE and Arm command; and to X'07' to specify an "RSIE Arm On Condition command. If the attachment is not initialized, these commands are not executed. An exception interrupt is posted with device-dependent status available set in the ISB.

Bit 15 of the control word modifier differentiates the two RSIE commands. When this bit is off, station-type attention interrupts are unconditionally armed subject to the masks in the station control bytes. When this bit is on, station type attention interrupts are armed only if no active SIE elements are stored.

The RSIE Arm On Condition command allows the program to pace interrupts and to reduce interrupts during periods of high station activity. It also increases station and 5250 Attachment availability to the program by preventing device busy reporting to I/O commands in high activity situations, where the 5250 Attachment would normally be attempting to process many attention interrupts into the processor. In response to an attention interrupt, the program can issue an RSIE Arm on Condition command. When this command is executed:

- Station-type attention interrupts are disarmed if at least one SIE is stored.
- Station-type attention interrupts are armed if no SIEs are reported.

Note: A byte count of 0 in the DCB implies that no active SIEs will be stored and the attachment will be armed automatically.

Note that if this mechanism is used, the program would have to be designed to do event-driven polling of the 5250 Attachment to receive SIEs, because it would not be station-attention-interrupt driven. An "event" that can be used conveniently is the completion of servicing on SIEs. Thus, the program does not have to be designed for pure polling.

The disarmed state of the 5250 Attachment is equivalent to a summary mask of all enable bits in the station control bytes.

Words 1–3. These words are fetched, but are not used or checked.

Word 4—Status Address. Refer to "Word 4—Status Address" under "Start Commands Overview" earlier in this chapter.

Word 5—Chain Address. Refer to "Word 5—Chain Address" under "Start Commands Overview" earlier in this chapter.

Word 6—Byte Count. This word contains the number of bytes to be transmitted to storage. The byte count may be 0 or up to a maximum of X'40' (decimal 64), and must be a multiple of 8, because the SIE returned is always eight bytes. If these byte count conditions are not satisfied, a DCB Specification Check results. If the byte count is 0, no SIEs are transferred. ILR can be reported to this command.

Exceptions Causing ILR Reporting. A suppressible short ILR is reported if the residual byte count is not exhausted and all active SIEs are successfully transferred. If the SE bit is on and a suppressible short ILR occurs, the residual status block is the mechanism to convey the residual byte count. The residual byte count is subtracted from the byte count in the DCB; the result divided by 8 is the number of SIEs stored. If the SE bit is off, an exception interrupt occurs with ILR and device-dependent status available set in the ISB, the latter indicating that the residual byte count is available in the cycle-steal status.

If the DCB byte count is not sufficient to accommodate all active SIEs on the command, then this is not an exception condition. The residual byte count will be 0. Active SIEs that were not stored either remain queued in the 5250 Attachment and cause subsequent attention interrupts if the 5250 Attachment is armed, or they wait to be taken on the next RSIE command if the 5250 Attachment is disarmed.

The decision to change the armed state of the 5250 Attachment during RSIE execution is not influenced by the setting of the SE bit. Therefore, if a short ILR is reported, the arming mechanism is still invoked (based upon the number of SIEs stored), regardless of the SE bit setting in the DCB. If any other exception occurs on a RSIE command, the armed state of the 5250 Attachment is not affected.

Word 7—Address Pointer. Refer to "Word 7—Address Pointer" under "Start Commands Overview" earlier in this chapter.

SIE Returned to Series/1

The SIEs reported back to the processor have the following format and are described below:

Byte 0 – Reserved; presented as zero
Byte 1 – Station address
Byte 2 – Cable status checks
Byte 3 – Station checks
Byte 4 – AID code
Byte 5 – Station status 1
Byte 6 – Station status 2
Byte 7 – Reserved; presented as zero

Bytes 1–6 are further summarized below.

Byte 1—Station Address. This byte has the same format as the Station Address field, DCB word 1, byte 1 described in "Byte 1—Station Address" under "Start I/O—IDCB Command 70" earlier in this chapter.

Byte 2—Cable Status Checks. The bit definitions are as follows:

Bit 0 – Screen format error (display station only)
Bit 1 – No response time-out
Bit 2 – Transmit activity check
Bit 3 – Activate command failure
Bit 4 – Receive parity check
Bit 5 – Receive length check
Bit 6 – Presented as zero
Bit 7 – Even/odd response time-out

Byte 3—Station Checks. The bit definitions are as follows:

Bit 0 – Station busy time-out
Bit 1 – Line parity check
Bit 2 – Unit not available (printer only)
Bit 3 – Outstanding status (printer only)
Bit 4–6 – Encoded exception status
  000 – No exception status
  001 – Null or attribute error (display station only)
  010 – Invalid activate command
  011 – Reserved
  100 – Invalid command or station ID
  101 – Input queue or storage overrun
  110 – Invalid register value (display station only)
  111 – Power-on transition
Bit 7 – Even/odd response indicator

Byte 4—AID Code. This byte contains one of the following:

- X'FF', when a 5250 Attachment detected error is being reported. In this case, the actual error will be indicated in one or more of the SIE bytes.
- Any one of the AID codes listed under "Attention Identifier (AID) Codes" in this chapter.

Byte 5—Station Status 1, Byte 6—Station Status 2.

These bytes have different formats depending upon whether the reporting station is a display station or a printer. For display stations, the format of these two bytes is as follows:

Byte 5—Station Status 1 (Display Stations). This byte contains one of the following:

- An error code that further classifies certain errors that cause bits to be set in the cable status checks byte of the SIE, or in the station operation check or cable status checks bytes in the cycle-steal status when reported as a part of cycle-steal status.
- An invalid scan code, if station status 2 (below) is equal to hex 2X, where X represents any value.
- The two high-order digits of the operator error code, if the AID code is equal to X'FB' (Help Key AID from operator error mode).
- A value of X'00' or X'80', if the value of station status 2 (below) is equal to hex 9X, where X represents any value.

Byte 6—Station Status 2 (Display Stations). This byte contains the following:

- X'28' or X'20' if an invalid scan code is being reported and the Master Modified Data Tag (MDT) bit is on/off respectively.
- The two low-order digits of the operator error code if the AID code is equal to X'FB' (Help key AID from operator error mode).
- Hex 9X, if a magnetic stripe reader associated error is being reported. If the magnetic stripe reader is not installed, station status 1 is X'00'; if the reader is installed but does not have any data, station status 1 is X'80'.

Bit 4 of this byte is called the Master MDT bit. This bit is turned on whenever any input field on the screen has its MDT bit on. Thus the Master MDT is the logical 'OR' of all field MDT bits. This byte can contain the following values:

X'00' – Master MDT off
X'08' – Master MDT on

The Master MDT bit is valid only when returned in the SIE; it is not valid when returned in the cycle-steal status.

Note: Relevant bit settings of the station operation check and cable status checks bytes rank over an invalid scan code for purposes of interpreting the formats of the station status 1 and station status 2 bytes.

For the printer, the formats of these two bytes is as follows:

Byte 5—Station Status 1 (Printer). This byte contains one of the following:

- An error code that further classifies certain errors that cause bits to be set in the station operation checks byte of the cycle-steal status.
- A bit significant error field if bit 3, outstanding status, of station checks byte is set in the SIE or cycle-steal status. The format in this case is as follows:

  Bit 0—Invalid SCS control character
  Bit 1—Invalid SCS parameter
  Bit 2—Reported as zero
  Bit 3—Reported as zero
  Bit 4—Reported as zero
  Bit 5—Printer mechanism not ready
  Bit 6—End of forms
  Bit 7—Graphic error

Byte 6—Station Status 2 (Printer). This byte contains a bit-significant error field if bit 3 of the station checks byte is set in the SIE or cycle-steal status. The format is as follows:

Bit 0—Wire check
Bit 1—Slow speed check
Bit 2—Fast speed check
Bit 3—Emitter sequence check
Bit 4—No emitter
Bit 5—Left margin check
Bit 6—Forms stopped
Bit 7—Forms position lost

Note: Relevant bit settings in the station op checks byte rank over the setting of bit 3 in the station checks byte for purposes of interpreting the format of the station status 1 and station status 2.

Station Status 1 Settings

The following settings of Station Status 1 result from cycle-steal status station operation checks settings:

Error Code for Data Stream Reject

1. Premature termination of data stream
2. Invalid row/column address (SBA, IC, RA)
   a. Row equal to 0 or greater than 24
   b. Column equal to 0 or greater than 80
3. RA ADDR specified is less than current address counter value
4. Invalid data stream command
   a. Escape character missing
   b. Invalid command code
5. Invalid field parameter length; field length equal to 0 in start field order
6. Input field defined out of sequence; starting address equal to or greater than starting address of field already defined
7. Invalid restore command data; restore data sent to wrong device
8. Input field runs past end of display
9. Format table overflow
10. Data written past end of screen
11. Invalid start of header order length
12. Roll command parameter error
    a. Roll mag equal to 0
    b. Top line equal to 0
    c. Bottom line greater than 24
    d. Roll mag greater than bottom line—top line
    e. Top line greater than bottom line
13. Too many FCWs defined for input field

Error Code For Station Byte Count Inconsistency Error

1. Invalid command modifier in 5250 Attachment; reported under DCB specification check (DCBSC)
2. Invalid Byte Count in 5250 Attachment; reported under DCBSC
   a. Byte count equal to 0 (display)
   b. Byte count greater than 256 (printer)
3. Device address not found in SPLs; reported under CDBSC
4. Byte count/data Inconsistency
   a. Count equal to 0 before all data transferred on RDIF command
   b. RDIF command issued with no format table
   c. Count equal to 0 before all data is transferred on Save Table, Save Screen, or Read Screen command

Error Code For Resources Temporarily Unavailable

1. Command stream directed to printer and printer buffer is not available
2. Terminal defined as not operational by controller (in state where hung busy, invalid response to poll.)
3. Station offline (not in session)
4. Printer needs initialization data
5. State error (will send AID 'FA' when condition clears)
   a. Operator error mode
   b. System request mode
   c. Pre-help operator error mode
6. Keyboard not locked on read
7. Terminal not powered on
8. Save/Restore Screen command is not preceded by Save/Restore Table command; commands other than Clear Unit, Save/Restore Table, Save/Store Screen command are issued after Save/Restore Table is executed

The following settings of station status 1 result from cycle-steal status or SIE cable status check settings:

Error Code for Screen Format Error

1. Invalid field length detected while keystroke processing or read input fields.
   a. Field was 0 bytes in length
   b. Field had no ending attribute
   c. Signed numeric field equal to length of one
   d. Field was greater than 80 characters when defined but equal to or less than 80 characters when read
   e. Field was equal to or less than 80 characters when defined but greater than 80 characters when read
   f. Field length greater than 80 characters for SN FLD
2. Resequence error in format table:
   a. Resequence number equal to 0
   b. Resequence number defined a field greater than number of fields on screen
3. Check digit error; field greater than 32 characters

Printer Notes

Set Graphic Error Action. The 5256 printer takes action on values of the error stop control byte from X'00' to X'FF'. Some interim engineering change (EC) levels of the printer, such as those implementing the International Character Set Extension, will accept and take specific print action on codes X'02' and X'04' other than defaulting them into X'01' and X'03', respectively.

Backspace. The printer does not support the backspace feature command by SCS code X'16'. The printer returns invalid SCS parameter to this code.

Attention Identifier (AID) Codes

The following AID codes are generated by the 5250 Attachment for display stations and printers:

Display Station AID Codes

Key name	AID code
CMD 1	31
CMD 2	32
CMD 3	33
CMD 4	34
CMD 5	35
CMD 6	36
CMD 7	37
CMD 8	38
CMD 9	39
CMD 10	3A
CMD 11	3B
CMD 12	3C
Test Request	3D
Sys Req/Enter (two keys)	F0
Enter/Rec Adv	F1
Attn	F2
Help (not oper error mode)	F3
Roll Down	F4
Roll Up	F5
Print	F6
Reserved	F7
Record Backspace	F8
Reserved	F9
Resource Available	FA
Help (operator error mode)	FB
Error Detected	FF
CMD 13	B1
CMD 14	B2
CMD 15	B3
CMD 16	B4
CMD 17	B5
CMD 18	B6
CMD 19	B7
CMD 20	B8
CMD 21	B9
CMD 22	BA
CMD 23	BB
CMD 24	BC
Clear	BD

Printer AID Codes and Operation

Printer AID codes are listed below in order of priority of reporting to the processor. X'FF' is the highest priority AID code. Codes that may be reported with each state of the quiescent bit are also shown.

Name	AID code	Q on	Q off
Error Detected	FF	Yes	Yes
Cancel Request	D1	Yes	Yes
Printer End (Printer/all buffers available)	E3	Yes	Yes
Two 5250 Attachment print buffers freed	E2	No	Yes
One 5250 Attachment print buffer freed	E1	No	Yes

Multiple printer AID codes are queued in the 5250 Attachment for reporting to the processor as follows: The queue consists of three elements: one for X'FF', one for X'D1', and one for the X'E1'—X'E3' codes. In the latter element, with the Q bit off, a X'E3' will overlay X'E2' or X'E1', and a X'E2' will overlay a X'E1'. The queueing occurs up to the time of reporting to the processor, at which time the queue elements are processed by reporting priority. Therefore, the most recent value of the X'EX' codes are reported if no higher priority elements need to be reported.

The printer AID codes function as follows:

Error Detected X'FF'. This printer AID code can be reported in either the cycle-steal status or in the station interrupt element. An error-detected AID code is not necessarily an ending AID code, in the sense that the 5250 Attachment terminated print operations.

Cancel Request X'D1'. This AID code is reported in the Station Interrupt Element only. It signals that the operator has pressed the Cancel key on the printer panel. Neither the printer nor the 5250 Attachment takes any further action other than to post and report this code. A Cancel request does not end printer operations.

Printer End X'E3'. This code is reported in the station interrupt element only. It signals that the printer and all printer buffers have been cleared and are available to the program. It is sent in response to data stream commands after all pending printer operations have been completed successfully, or to a Clear Unit command when all buffers have been cleared successfully.

One or Two Print Buffers Freed X'E1'/X'E2'. These codes are reported only in the station interrupt element, and only in response to operations conducted with the quiescent bit off. They signal that the event of freeing one or two 5250 Attachment print buffers has occurred after successful transfer from the 5250 Attachment to the printer. These codes are not reported in response to a Clear Unit command.

Notes:

1. It is important to realize that there are actually six print buffers associated with the printer—two in the 5250 Attachment and four in the printer itself. The 5250 Attachment can only report on the availability of its two buffers by means of the X'E1' and X'E2' AID codes. All six buffers can be envisioned as a "FIFO queue" of six elements. Buffer loads are put into the queue when accepted by the 5250 Attachment and subsequently advance through it at a rate determined by such parameters as 5250 Attachment activity and buffer load contents. Buffer loads exit the queue when the printer has successfully completed operations on each load. However, the completion of each particular buffer load is not reported by the printer if there are still more elements in the queue to process. A printer end is reported by means of the X'E3' AID code only if the queue is successfully processed and empty. The X'E1' and X'E2' AID codes can then be envisioned as 5250 Attachment reports of *advances* of buffer loads through the queue, signifying to the program that it can accept one or two more loads as appropriate with the AID code. These codes also allow the program to keep track of the loads through the queue and, consequently, the exits (successful completions) of buffer loads from the queue. For error recovery purposes, the particular loads that may be affected by an error condition are those that are in the queue. Error reports, however, do not associate the error with a particular load, so all loads in the queue must be assumed to have been affected. Program design is still left with the choice of committing less than the maximum number of six loads to the queue at any given time to improve selectivity of error recovery or to simplify error recovery procedures.
2. If the program design elects to overdrive the queue input to keep the "FIFO queue" full by not keying on the buffer availability AID codes, then interrupts with resources temporarily unavailable reported, or residual interrupts, can be expected. A residual interrupt is an attention interrupt accepted by the processor, but the SIE is not stored on a subsequent RSIE command. This can occur, for example, when the 5250 Attachment has posted an X'E1' AID code, causing an attention interrupt. Then, if the 5250 Attachment accepts another buffer load prior to the SIE being read, the 5250 Attachment posting of X'E1' is changed to no buffers available, and at RSIE time, the SIE is inactive and not stored. In addition, resources temporarily unavailable interrupts terminate DCB chains. It is therefore recommended that program design "*event drive*" the printer buffers by keying on the buffer available and/or printer end AID codes as appropriate with the setting of the quiescent bit.

Operation of the printer with the quiescent bit on requires the following considerations:

- The program is provided the means to associate X'FF' and X'D1' AID reporting with posting when print operations are in progress, or posting when print operations are not in progress.
- Such operation generates fewer interrupts to the processor, because X'E1' and X'E2' are not reported.
- The programmer has the design choice of loading only one or two buffers at a time and waiting for a printer end to initiate each successive single or double load. Event-driven loading of the queue is not feasible with triple, quadruple, or more buffer load approaches.
- Such operation has the lower performance of the two basic modes of printer operation, because the program is interlocked with each printer end. Consequently, inherent delays of program turnaround and delays in transferring loads out to the printer are not performed concurrently with actual print operations.
- Program design must consider that buffer loads should be "complete," in the sense that SCS commands must not span buffer loads; otherwise, printer timeouts can occur. Also, print lines should not span buffer loads.

Operation of the printer with the quiescent bit off requires the following considerations:

- The program is not provided the means to associate FF and D1 reporting with print operations, because the printer is not removed from the 5250 Attachment poll list when posting AIDs.
- Such operation generates more interrupts to Series/1 because the E1 and E2 codes are reported.
- The programmer has the design choice of keeping up to six loads in the FIFO queue at any given time and retain event-driven loading of the queue.
- Such operation has the higher performance of the two modes of printer operation, because program turnarounds and transfer of buffer loads to the printer may be overlapped with actual print operations.
- Program design does not have to consider containing SCS commands and print lines within buffer load boundaries.

Help Message Overlay Service. If the operator responds to the four-character error message by pressing Help, the 5250 Attachment sends an AID byte and an error code to the program. The program may then obtain a message, which is a plain language explanation of the error code. This message can then be sent to the proper station and it overlays the operator error message area. When the operator presses the Error Reset key, the message area is restored.

Note: If the Help message overlay is used, the user must either not use the bottom row, or accept temporary replacement of data in the bottom row if an operator error occurs.

Start Control Store Commands—IDCB Command 72

The following Start Control Store commands are used in loading 5250 Attachment storage to initialize the 5250 Attachment:

- Load Control Store
- Load Control Store and Initialize

These commands are identified by bits 8–15 of the DCB control word.

The format of the DCB is as follows:

Word 0—Control Word. Refer to "Word 0—Control Word" under "Start Commands Overview" earlier in this chapter. The input flag (IF) bit 2 must be equal to zero. Otherwise, a DCB Specification check results. These commands are executed regardless of the initialized state of the 5250 Attachment. Chaining is supported; SE is not.

Bits 8–15 are the control word modifier bits and are set to X'00' to specify a Load Control Store command, and to X'01' to specify a Load Control Store and Initialize command.

During execution of the Load Control Store and Initialize command, the loading of control store is performed first; then a hardware signature compare and checksum is performed. If the signature does not match or a checksum cannot be performed successfully, the 5250 Attachment does not enter the initialized state. An exception interrupt occurs with device-dependent status available set in the ISB. Appropriate bits are set in the 5250 Attachment exception status word, and the 5250 Attachment operation checks byte in the cycle-steal status.

If valid hardware signature comparison and checksum calculations are made, the attachment enters the initialized state with the arm bit off. The attachment can exit the initialized state only on the following occurrences:

- Power On Reset
- The acceptance of a command that can potentially alter 5250 Attachment storage; that is, either of the two Load Control Store commands, regardless of the byte count specified. Note, however, that the successful execution of a Load Control Store and Initialize command results in the attachment becoming initialized upon completion of the operation.
- The execution of a Device Reset, Halt I/O, or System Reset occurring *during* execution of any Start Control Command, IDCB Modifier 0010, or *after execution of a Start Control command prior to execution of any other cycle-steal command.*

Word 1—5250 Attachment Storage Starting Address. This word specifies the starting 5250 Attachment storage address where the data is to be loaded. Loading proceeds in ascending order of 5250 Attachment storage addresses from the starting address. This starting address may be even or odd. This address is checked to determine if it is a valid 5250 Attachment address; if it is not valid, a DCB specification check results. Also, the 5250 Attachment storage starting address plus the byte count specified in the DCB may not exceed the maximum 5250 Attachment storage address; otherwise, a DCB specification check results.

Valid 5250 Attachment random access memory addresses are X'8040' through X'9FFF' and X'A800' through X'AFFF'.

Words 2–4. These words are fetched, but are not used or checked.

Word 5—Chain Address. Refer to "Word 5—Chain Address" under "Start Commands Overview" earlier in this chapter.

Word 6—Byte Count. The byte count may be even or odd. The byte count plus the contents of DCB word 1 must be within the range of valid addresses. In addition, the byte count, by itself, may not exceed X'0FFF'. Otherwise, a DCB specification check results. ILR is not reported for these commands.

Word 7—Address Pointer. This address may be even or odd.

Note: The Load Control Store and Initialize command with a byte count of zero allows an initialization to be performed without altering 5250 Attachment storage. The Load Control Store command with a byte count of zero allows the attachment to be "de-initialized".

Start Cycle Steal Status Command—IDCB Command 7F

The Start Cycle Steal Status command is a cycle-steal command used primarily for recovery or diagnostic procedures; however, it can be issued at any time. Only words 0, 6, and 7 of the DCB are fetched by the attachment.

The format of the DCB follows:

Word 0—Control Word. The input flag (IF) bit must be on. If it is not, a DCB specification check results. The key field is used. All other bits are not used or checked and must be 0's.

Words 1–5. Not fetched.

Word 6—Byte Count. The byte count must be even and less than or equal to X'0012' (decimal 18). If it is not, a DCB specification check results. ILR cannot be reported for this command.

Word 7—Address Pointer. This address must be even. If it is not even, a DCB Specification Check will result.

Cycle-Steal Status Format

The format of the nine words of cycle-steal status returned to storage is described below in ascending order of processor storage.

CSS Word 0—Residual Address. Contains the address of the last attempted cycle-steal transfer for data, DCB, or RSB transfers. It is not updated on data transfer of the cycle-steal status. The residual address is reset to X'0000' only on a power-on reset.

CSS Word 1—Residual Byte Count. The residual byte count is only relevant to data transfers, and it is equal to the DCB byte count minus the number of data bytes transferred. It is not updated on data transfers while fetching the DCB executing Start Cycle Steal Status command, or while storing the residual status block. The residual byte count is reset to all 0's during any reset or the acceptance of any interrupt-causing command. It is initialized on the fetch of the count field of a DCB.

CSS Word 2—RSB Status. Contains the same format information as word 1 of the residual status block (EOC bit, status flags, and NE bit). The reset state of this word is all 0's, and this state is assumed during any reset or acceptance of any interrupt-causing command. It is set to ending status on suppress-exception operations prior to storing the RSB. If an exception interrupt occurs with SE operations and the residual address and key lie within the boundaries of the RSB (as defined by the status address and fixed size of the RSB), this word and the residual byte count are indicative of the RSB that the 5250 Attachment attempted to store. On any other exception conditions, the contents of this word are not relevant.

CSS Word 3—Station Op Checks/Station Address. This word contains check conditions incurred while executing a station-directed command and the address of the station to which the command was directed. It is reset to all zeros during any reset or the acceptance of any interrupt-causing I/O command. It is reset to the ending status of the station addressed on completion of a station-directed command. For nonstation-directed commands, these indications are not set. The format of this word is as follows:

Byte 0—Station Operation Checks

Bit 0	–	Data stream reject
Bit 1	–	Station byte count inconsistency
Bit 2	–	Resources temporarily not available
Bit 3	–	Reserved; presented as 0
Bit 4	–	Reserved; presented as 0
Bit 5	–	Reserved; presented as 0
Bit 6	–	Reserved; presented as 0
Bit 7	–	Reserved; presented as 0

Byte 1—Station Address. This byte has the same format as the station address field in the DCB for the station-directed commands, Start Data and Set Station Control Bytes.

CSS Words 4, 5, 6. The reset state of these words is all zeros. This state is assumed during any reset, or the acceptance of any interrupt causing command. They are set to the ending status of the station addressed on completion of station directed-commands and are identical in format to SIE Bytes 2–7, described in "SIE Returned to Series/1" in this chapter. For commands that are not station-directed, these words will not be set.

CSS Word 7—5250 Attachment Exception Status.

Byte 0—Operation Checks. This byte has the following format:

Bit 0—Incorrect CSLM Checksum. This bit, if on, indicates that the checksum operation performed on a Load Control Store and Initialize command was unsuccessful. The most likely cause is that the contents of the control store load module have been altered or only partially loaded into the 5250 Attachment.

Bit 1—Controller Storage Load Module Incompatibility. This bit, if on, indicates that the controller storage load module loaded did not match the hardware signature in the 5250 Attachment during execution of a Load Control Store and Initialize command. The signature cannot be read by the program. The most likely cause of this exception is that the controller storage load module did not match the level of the 5250 Attachment hardware.

Bits 2–7—Reserved; presented as 0.

Byte 1—DCB Specification Checks. These bits further define the reason for a DCB specification check on an exception interrupt with DCB specification check set in the ISB.

X'00'	No DCB specification check
X'01'	Invalid DCB control word modifier
X'02'	Input flag (IF) bit of the DCB is incorrect with respect to the DCB control word modifier or station command modifier.
X'03'	PCI, XD, or SE bit on
X'04'	Odd chain or status address
X'05'	Byte count incorrect with respect to DCB specification
X'06'	Invalid 5250 storage starting address
X'07'	Odd 5250 Attachment storage starting address
X'85'	Byte count incorrect with respect to station command station command modifier specification
X'88'	Invalid station command modifier
X'89'	Invalid station address

There is no specific order of 5250 Attachment checking implied by the values of these DCB specification check codes. The remainder of the DCB specification check (DCBSC) codes not listed above are reserved and not reported.

X'00' is the reset state of the 5250 Attachment exception status word. This state is assumed during any reset or the acceptance of any interrupt-causing I/O command.

CSS Word 8—5250 Attachment Status/Residual Address Key.

Byte 0—5250 Attachment Status.

This byte has the following format:

Bit 0—Initialized. This bit, if on, indicates that the 5250 Attachment is initialized.

Bit 1—Armed. This bit, if on, indicates that the 5250 Attachment is armed.

Bits 2–3. Reserved; presented as 0.

Bits 4–7. Reserved; may be presented as non-0.

Byte 1—Residual Address key. This byte has the following format:

Bits 0–4. Presented as zero.

Bits 5–7—Residual Address Key.

These bits contain the key that was used corresponding to the residual address. The residual address key is reset to all zeros only on power-on reset.

Interrupt Presentation and Condition Code Settings

The following table shows the condition codes that may be reported in response to device directed commands for each function type. "N" signifies that the condition is not reported for this function. "X" signifies that the condition code may be reported for this function.

Function (Valid)	OIO condition code							
	0	1	2	3	4	5	6	7
Start I/O	X	X	X	N	N	X	N	X
Start Control Store	X	X	X	N	N	X	N	X
Start Cycle Steal Status	X	X	X	N	N	X	N	X
Prepare I/O	X	N	N	N	N	X	N	X
Device Reset	X	N	N	N	N	N	N	X
Read Device ID	X	X	X	N	N	X	N	X

Function (Invalid)	FN	Modifier	OIO condition code							
			0	1	2	3	4	5	6	7
Write*	00	All	X	X	X	N	N	X	N	X
Write*	01	All	X	X	X	N	N	X	N	X
Control	10	All but 0000 and 1111	X	X	X	X	N	N	N	N
Read	00	All	X	X	X	X	N	N	N	N
Read	01	All	X	X	X	X	N	N	N	N
Read Status	10	All but 0000	X	X	X	X	N	N	N	N
Start*	11	All but 0010 and 1111, 0000	X	X	X	N	N	X	N	X

* These invalid commands cause an exception interrupt (condition code=2) with delayed command reject (bit 1 in the ISB) set.

OIO condition codes that may be reported above are:

0 —Device not attached

1 —Busy

2 —Busy after reset

3 —Command reject

5 —Interface data check

7 —Successful

The following table identifies the condition codes that can be reported at interrupt presentation. The significance of the high-order byte of the interrupt ID is shown as well.

Condition Codes During Interrupts

CC	ECO	Meaning	Reported	Interrupt ID (bits 0–7)
0	0 0 0	Controller end	No	-
1	0 0 1	PCI	No	-
2	0 1 0	Exception	Yes	Contains ISB
3	0 1 1	Device end	Yes	Contains IIB
4	1 0 0	Attention	Yes	Contains IIB
5	1 0 1	Attention & PCI	No	-
6	1 1 0	Attention & exception	Yes	Contains ISB
7	1 1 1	Attention & device end	Yes	Contains IIB

On the normal completion of an interrupt-causing command, device end (CC=3) is reported. If an abnormal end occurs, exception (CC=2) is reported with the ISB contained in bits 0–7 of the interrupt ID.

Exception Interrupt ISB

The format of the ISB is as follows:

Bit 0—Device-Dependent Status Available.

Bit 1—Delayed Command Reject. Because this error is not state-dependent on the 5250 Attachment, the device-dependent status available bit is not set when this bit is on.

Bit 2—ILR—Incorrect Length Record. Incorrect length errors reported are non-suppressible short ILR or suppressable short ILR if the SE bit is off. This bit is not set if a suppressible short ILR occurs and the SE bit is on, or if the residual byte count is zero.

Bit 3—DCB Specification Check. Because DCB specification check errors are further resolved in the cycle-steal status, the device-dependent status available bit is also set in the ISB when a DCB specification check occurs on any operation other than a Start Cycle Steal Status. A DCB Specification check in response to a Start Cycle Steal Status command will have ISB bit 0 set to zero.

Bit 4—Storage Data Check.

Bit 5—Invalid Storage Address.

Bit 6—Protect Check.

Bit 7—Interface Data Check.

Device End IIB

The format of the IIB when reporting device end is as follows:

Bit 0—Permissive Device End.

Bits 1–7. Presented as zeros.

Attention Interrupt IIB

The format of the IIB when reporting attention is as follows:

Bit 0. Presented as zero.

Bit 1—5250 Attachment Hardware Check. This bit is set on if a 5250 Attachment hardware check occurs. The 5250 Attachment has attempted to reset the initialized bit. Subsequent 5250 Attachment operation may not be predictable, including start cycle status.

Bits 2–7. Presented as zero.

Attention and Exception ISB

The format of the ISB is the same as that given previously for the Exception Interrupt ISB. The Attention IIB contents do not conflict with the ISB and are zero.

Attention and Device End IIB

The format of the IIB when reporting device end and attention is as follows:

Bit 0 – same as device end IIB bit 0

Bit 1 – Same as attention IIB bit 1

Bit 2 – Presented as zero

Bit 3 – Presented as zero

Bit 4 – Presented as zero

Bit 5 – Presented as zero

Bit 6 – Presented as zero

Bit 7 – Presented as zero

Recovery Procedures

OIO Condition Codes

CC=0 Device not attached. Retry the command three times. If the problem persists, report the CC and address to the user.

CC=2 Busy after reset. Retry after four seconds. If still busy, report the condition code and device address to the user.

CC=3 Command reject. Retry the command three times. If the problem persists, report the condition code and the address of the failing instruction to the user.

CC=5 Interface data check. Retry the command three times. If the failure persists, report the condition code and the address of the failing instruction to the user.

CC=1,4,6 Codes not normally reported. Retry three times. If the error persists report the condition code and the address of the failing instruction to the user.

Interrupt Condition Code=2 (Exception)

ISB bit 7 Interface data check

or

ISB bit 4 Storage data check.

Examine the IDCB command word as follows:

1. If the IDCB command word equals 70 (start I/O or station read interrupt element), examine DCB word 1, byte 1.
   a. If DCB word 1, byte 1, equals X'A7' or X'27' (output data stream), execute Start Cycle Steal Status and examine the residual adress (word 0).

      If word 0 points to the DCB or RSB, retry the instruction three times. If the problem persists, report the address of the failing instruction condition code, the ISB, and the residual address to the user.

      If status word 0 points to data, retry the command three times.

      If any retry is successful, *immediately* issue a Clear Unit command to the terminal and restart the task. (Field format tables and screen/printer data are not reliable after this failure.)

      If all retries fail, report the address of the failing instruction, the condition code, the ISB, and the residual address to the user.

   b. If the IDCB command word equals X'70' but DCB word 1, byte 1, is neither X'A7' or X'27', continue with step 2.
2. For any other command, retry the instruction three times. If all retries fail, report the address of the failing instruction, the condition code, the ISB, and the residual address to the user.

ISB Bit 1. Delayed command reject.

Retry the instruction three times. If the problem persists, report the address of the failing instruction, the condition code, and the ISB to the user.

ISB bit 2 Incorrect length record

or

ISB bit 0 No other bits on; device-dependent status available.

Execute Start Cycle Steal Status and examine cycle-steal status word 3, byte 0 (station op checks).

1. If cycle-steal status word 3, byte 0, equals 0, examine status word 4. If status word 4 is not 0, see "Cable/Station Related Errors" later in this chapter.
2. If word 3, byte 0, equals 0, and word 4 equals 0, this is an error condition resulting from a suppressible short ILR. status word 1 contains the residual byte count. No retries are necessary.

   If DCB control word bit 4 (suppress exception) is on, this condition is reported as permissive device end (ICC equals 3, ISB equals 8X) and the residual status blocks are available.
3. If status word 3, byte 0, equals X'20' (resources temporarily unavailable), retry the command three times. If the problem persists, report the interrupt condition code, the address of the failing instruction, the ISB, and cycle-steal status words 3, 5, and 6 to the user.
4. If status word 3 equals X'80' (Data Stream Reject), issue a Clear Unit command to the terminal and restart the task.

Interrupt Condition Code 6—Attention and Exception

The procedure for this condition code is essentially the same as for interrupt condition code 2. The attention IIB contents are zero and do not conflict with the ISB. Exception error recovery takes precedence over attention interrupt servicing, which is station related.

Note: If an RSIE command associated with servicing the attention interrupt is executed prior to executing a Start Cycle Steal Status, the cycle-steal status is cleared of information relevant to recovery of the exception condition.

Cable/Station Related Errors

The status examined here can come from either the station interrupt element or the Start Cycle Steal Status. Therefore, all references are to SIE byte labels.

Examine SIEs and cycle-steal status for aid byte equal to FF (error aid).

If the aid byte equals FF:

1. Examine cable status checks.
   a. If only bit 3 is on (activate command failure), retry the last station-directed command for this address three times. If the problem persists, report the station address and cable status checks to the user.
   b. If any other bit is on in the cable status checks, report the station address and cable status checks to the user.
   c. If cable status checks equals 0, report the station address, cable status checks, station checks, aid byte, station status 1, and station status 2 to the user.

Status After Power Transitions and Resets

Device Reset, Halt I/O, and System Reset

Execution of these resets results in the following:

1. The device enters the busy-after-reset state.
2. All pending interrupts are reset. The prepare register is unchanged for a Device Reset or Halt I/O; it is reset on a System Reset.
3. Cycle-stealing operations are terminated immediately. The residual address may be indeterminate; the residual byte count is reset. The residual address and residual address key are unchanged.
4. Device-dependent cycle-steal status is reset. (Refer to "Start Cycle Steal Status Command—IDCB Command 7F" earlier in this chapter for the device-dependent bits that can be reset.)
5. The 5250 Attachment is in non-active status. If the 5250 remains in the initialized state, station control bytes are set to X'30', the stations are placed in free-key mode, and format tables and display attributes are reset to reflect the free-key mode of the stations.
6. The 5250 Attachment exits the initialized state if either:
   a. The reset occurs during the execution of any Start Control Store command—IDCB command 72; or
   b. The last previously executed command was a Start Control Store command.
7. The content of controller storage is affected; however, the storage remains valid with respect to parity. The 5250 Attachment remains initialized if it was in the initialized state upon execution of the reset.
8. The controller self-checks are invoked and are completed prior to exiting the busy-after-reset state.

Power-On Reset

A power-on reset is executed as follows:

1. The 5250 Attachment enters the busy-after-reset state.
2. All pending interrupts are reset. The prepare register is reset.
3. Cycle-stealing operations are terminated immediately. The residual byte count is reset. The residual address and residual address key are reset to zeros.
4. Device-dependent cycle-steal status, including the initialized bit, is reset.
5. The 5250 Attachment resets to the non-initialized state. Neither the active status of the 5250 Attachment nor the value of the station control bytes has any meaning if the attachment is not initialized.
6. The content of controller storage is validated only with respect to storage parity. User-loadable controller storage must be initialized by the program.
7. The controller self checks are invoked and will complete prior to exiting the busy-after-reset state.

Attention interrupts associated with controller operation asynchronous to the program may occur after the device has exited the busy reset state. Refer to "Interrupt Presentation and Condition Code Settings" earlier in this chapter.

Initialized and Active Status

The status of these two attachment states is reported in the cycle-steal status. Both states, which are associated with the attachment and not with the stations, are affected only by attachment-directed commands (that is, RSIE and Load Control Store commands) and resets, the latter being system or attachment-directed.

To support free-key mode, the attachment must at least be initialized and the program must be capable of reading SIEs. The notification of station interrupts and reading of SIEs is based upon the activation and RSIE mechanism chosen in program design. The station control bytes must at least reflect an online condition and high priority attention IDs enabled to support free-key mode. The station control byte values are set to X'30' upon entry into the initialized state upon the occurrence of a reset. In addition, the station control byte for a particular station is also set to X'30' state on occurrence of a power-up at that terminal. Therefore, the program need not execute any station-directed commands (for example,Set Station Control Byte) to establish communication with all stations in support of free-key mode.

Special Maintenance Tools

One diagnostic tool, the probe adapter, is available for this attachment. This is a Berg 2x12 shielded right angle header (IBM P/N 2731830) that mates with the Berg connector on the attachment cable and provides probe points for the CE to perform the Cable Quality Test MAP in the maintenance package.

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