IBM

Series/1

SY34-0044-1

IBM Series/1
4964 Diskette Unit
and Attachment Feature
Theory Diagrams

4964 DISKETTE THEORY

Second Edition (January 1978)

This revision of SY34-0044-0 contains extensive additions to all previously published material. Major areas of change include, but are not limited to, the diagrams and associated text in chapters 3 and 4.

Significant changes or additions to the contents of this publication will be reported in subsequent revisions or Technical Newsletters. Requests for copies of IBM publications should be made to your IBM representative or the IBM branch office serving your locality.

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Contents

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Preface

This manual describes all models of the IBM 4964 Disk Storage Unit, and the attachment features.

This manual is designed to be used in the classroom as an aid in teaching personnel that are to be involved in the maintenance of any models of the 4964. This manual may also be used in the field as a recall document.

Sequence charts and diagrams are intended for instructional purposes only and are not to be used in troubleshooting procedures. The 4964 machine logic diagrams (MLD) are to be used in diagnosing difficult and intermittent problems not found using the maintenance analysis procedures (MAPs) that accompany the 4964 maintenance information manual.

Related Publications

- *IBM Series/1 4953 Processor and Processor Features 4959 Input/Output Expansion Unit 4999 Battery Backup Unit Theory Diagrams,* SY34-0042
- *IBM Series/1 4955 Processor and Processor Features 4959 Input/Output Expansion Unit 4999 Battery Backup Unit Theory Diagrams,* SY34-0041
- *IBM Series/1 4964 Disk Storage Unit and Attachment Feature Maintenance Information,* SY34-0053
- *IBM Series/1 4964 Diskette Unit Parts Catalog,* S131-0601
- *IBM Series/1 Model 5 4955 Processor and Processor Features Description,* GA34-0021
- *IBM Series/1 Model 3 4953 Processor and Processor Features Description,* GA34-0021
- *IBM Series/1 4962 Disk Storage Unit and 4964 Diskette Unit Description,* GA34-0024
- *IBM Series/1 User's Attachment Manual,* GA34-0033

Acronyms and Abbreviations

ac alternating current
AM address mark
amp ampere

BH behind home

CCI condition code in
CRC cyclic redundancy check
CS cycle steal

DCB device control block
DPC direct program control
dc direct current
DE disk enclosure

FRU field replaceable unit

GB guardband

HZ hertz

IDCB immediate device control block
I/O input/output
ISB interrupt status byte

kg kilogram
kHz kilohertz

LED light emitting diode
LSR level status register
LZ landing zone

MAP maintenance analysis procedure
MIM maintenance information manual
MLD machine logic diagrams
us microsecond
mm millimeter
ms millisecond
mV millivolt

ns nanosecond

IO operate input/output

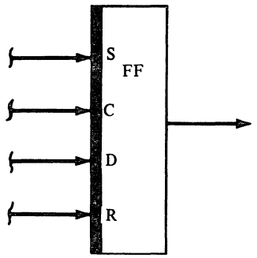
PC printed circuit
preamp preamplifier
PTS phototransistor

rpm revolutions per minute
R/W read/write

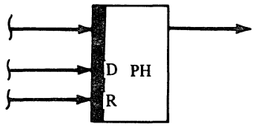
V volt
V ac volts, alternating current
V dc volts, direct current
VFO variable frequency oscillator
VOM volt/ôhmmeter

°C degree celsius
°F degree farenheit

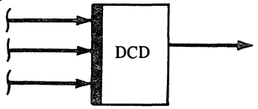
Legend



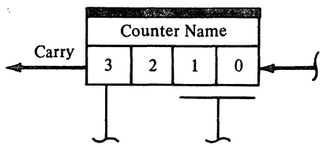
Flip Flop
The flip flop (FF) is a storage element that may have a set (S), reset (R), control (C), or controlled data (D) inputs.



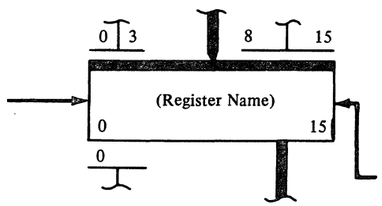
Polarity Hold
The polarity hold (FF) is a storage element that may have control (C), controlled data (D), or reset (R) inputs



Decode
The decode (DCD) block may have multiple inputs of individual lines, a bus input, or a combination of both.



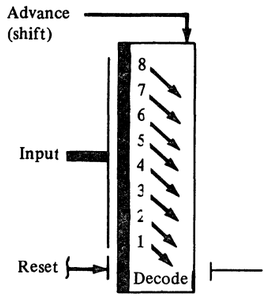
Counter
+1 for up
-1 for down



Register

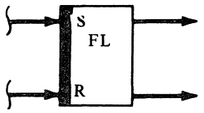
Input side is denoted by thick line. A partial transfer of contents is shown by numbered input and/or output lines.

Carry or increment



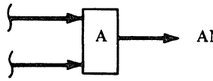
Shift registers

The shift registers are commonly used to seralize and deserialize data. Input side is denoted by the thick line. A partial transfer of contents is shown by numbered input/output lines.

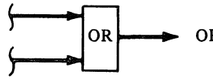


Flip latch

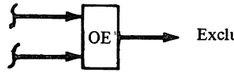
Input side is denoted by thick line. Circuit multiples shown by numeral in lower right corner.



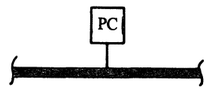
AND



OR



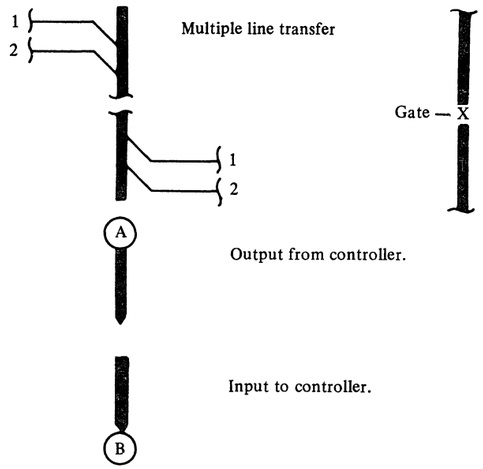
Exclusive OR

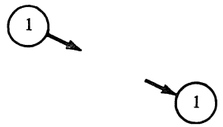


Parity check data bus

Parity generate data bus

Negator (invertor)



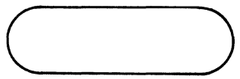


On page connector

Indicates connection between two parts of the same page. Arrow leaving symbol points (line-of-sight) to correspondingly-numbered symbol.

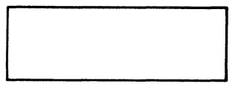
Off-page connector

Indicates connection between diagrams located on separate pages. Location of correspondingly-lettered symbol shown adjacent.



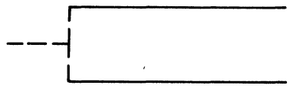
Terminal

Indicates beginning end or event.



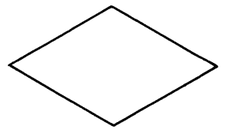
Process

Indicates a major function or event.



Annotation

Gives descriptive comment or explanatory note.



Decision

Indicates a point in a flowchart where a branch to alternate paths is possible.

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Chapter 1.
Introduction

General Description

The IBM 4964 Diskette Unit is a direct access storage device designed to exchange data with an IBM Series/1 processor. The diskette unit attaches to the Series/1 by means of the diskette unit Attachment Feature (3581). Location of the attachment feature card, which controls the transfer of information between the processor and the diskette unit, may be in either of the following system units:

- **IBM Series/1 Model 5, 4955 Processor**
- **IBM Series/1 Model 3, 4953 Processor**
- **IBM Series/1 4959 Input/Output Expansion Unit**

Diskette Unit

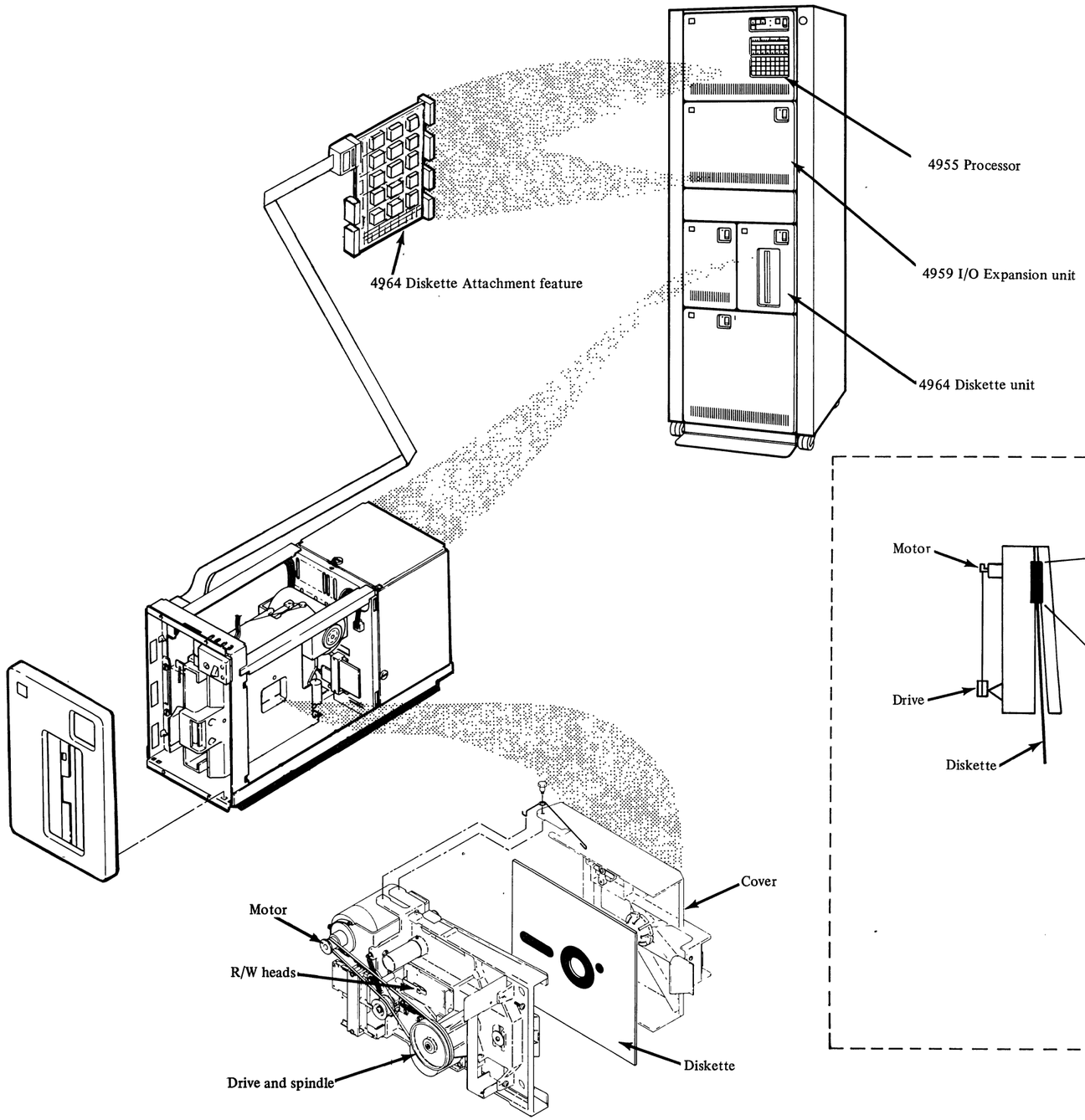
The diskette unit uses a flexible magnetic diskette as its storage medium. The diskette drive seeks, writes on, or reads from data tracks on the diskette.

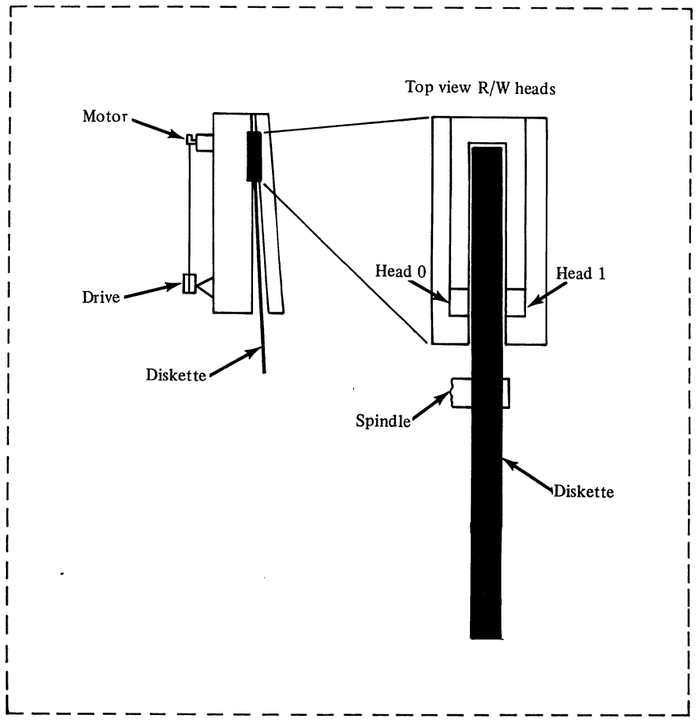
The diskette drive has a continuously turning spindle which engages the diskette. A stepper motor positions the read/write heads over the data tracks.

Commands from the channel initiate the read, write and seek operations in addition to performing various control functions. Records on the diskette are referenced from an index hole in the diskette.

Some typical uses include the temporary or permanent storage of:

- **System control programs**
- **Utility programs**
- **Diagnostic programs**
- **Application programs**
- **Data sets (groups of records).**





Diskette

The IBM diskette is a thin, flexible disk permanently mounted in a semi-rigid protective jacket. The diskette surfaces are coated with a magnetic recording material. The jacket protects the surfaces from handling damage and the disk rotates in the jacket. The diskette and the jacket together are referred to as a *diskette*.

There are two types of diskettes on which data can be recorded and retrieved.

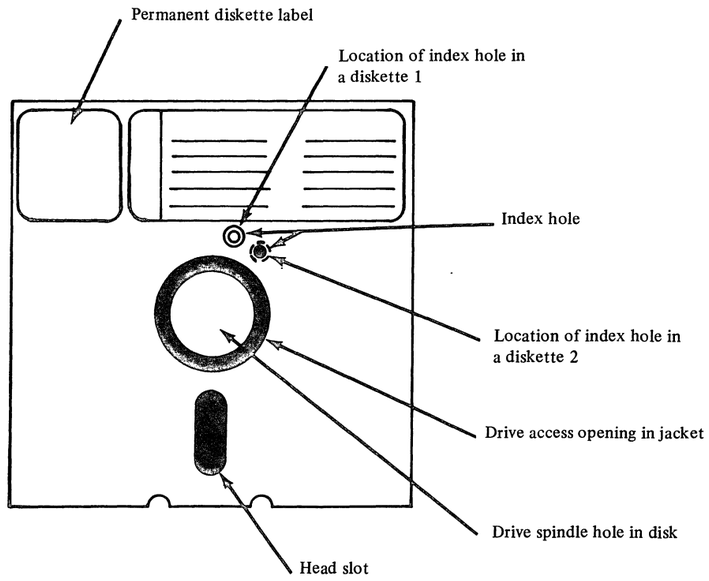
- Diskette 1 which has tracks formatted on side 0 only
- Diskette 2 which has tracks formatted on side 0 and side 1.

The two types of diskettes are identified by the physical location of the index hole. When a diskette 1 is inserted in the 4964, index detection circuitry prevents reading or writing on side 1.

For more information about the IBM diskette, see *The IBM Diskette General Information Manual,* GA21-9182.

Index

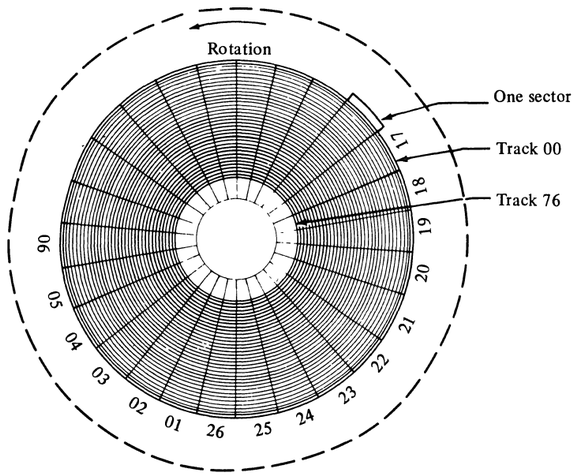
When the index hole in the diskette passes a light source an index timing pulse is generated. The index timing pulse begins track format operations and determines whether a diskette 1 or diskette 2 is installed in the diskette unit.



Diskette Format

There are 77 tracks on a diskette surface. Of the 77 tracks, only 74 tracks can be used as data tracks. Track 00 is a label track and tracks 75 and 76 are reserved as alternates to be used in place of tracks that become defective. Each track is divided into sectors. The content of each sector is described under "Sector Format." The data stored in one sector is called a record.

Because diskettes are formatted into tracks and sectors, each record on the diskette has a definite address consisting of a track and record address. Each record consists of two parts; the first part contains identification information and the second part contains data.



26 Sector diskette

Tracks

Diskette surfaces are divided into 77 tracks, numbered 00 through 76. Tracks are numbered from 00 (outermost) to 76 (innermost).

Each track is divided into fixed length sectors.

Cylinders

On a diskette 2, one or two tracks can be written or read without moving the heads. On one-sided diskettes, the terms cylinder and track are synonomous. On two-sided diskettes, a cylinder consists of the pair of tracks (one on each side) that can be read or written without moving the heads. Head 0 records or retrieves data from tracks on side 0 of the diskette, and head 1 records or retrieves data from tracks on side 1 of the diskette.

Sectors

A sector is a physical location on the diskette and can hold all or part of a record. If the record is shorter than the sector length, the unused bytes are filled with binary zeros. If a record is longer than the sector length, the record is written over as many sectors as its length requires.

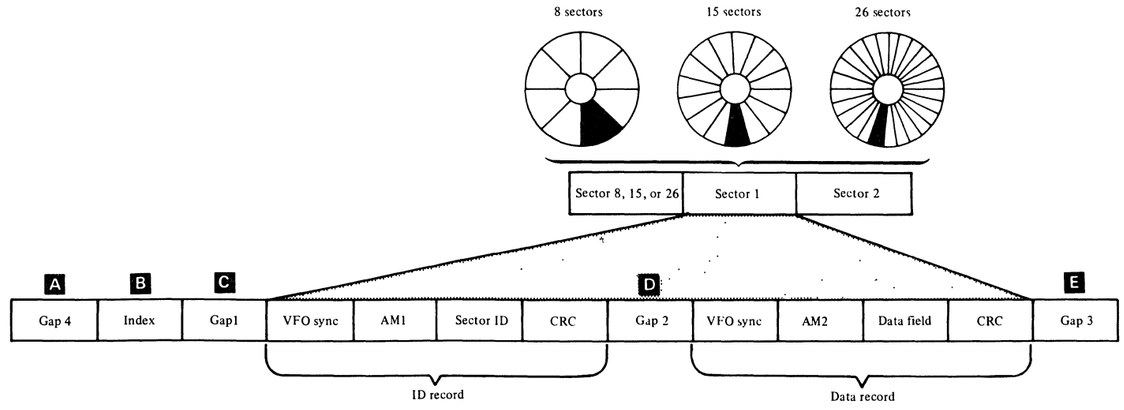
Sector size is specified in the sector ID. The ability to choose a sector size is especially useful if record length requirements change from job to job or from diskette to diskette. The sector size that provides the most efficient use of diskette space can be chosen from the following, depending on the record length required:

Sector size	*Sectors per track*	*Track storage*
128 bytes	26	3328 bytes
256 bytes	15	3840 bytes
512 bytes	8	4096 bytes

Synchronization

Synchronization is accomplished by the following gaps and fields:

- **A** Gap 4 the last record gap. All ones or zeros are found until an index pulse is encountered. The number of bytes in this gap will vary according to file speed variations and record size formats.
- **B** Index signals the beginning of a track
- **C** Gap 1 is the post-index gap required to accommodate index pulse timing variations. Gap 1 consists of 73 bytes of ones or zeros.
- **D** Gap 2 is the post-ID gap required to accommodate erase head delay and rotational tolerance. Gap 2 contains 11 bytes of ones or zeros
- **E** Gap 3 is the post data gap required for erase head delay and rotational tolerance. Gap 3 contains ones or zeros.
  - 27 ones for 128 byte sector
  - 42 ones for 256 byte sector
  - 58 ones for 512 byte sector

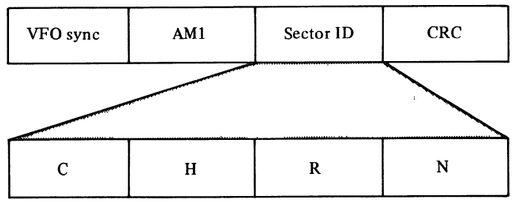


Sector Format

Each sector on a diskette has an identifier (ID) record and a data record. There is a sync field ahead of each ID and data field. This sync field is created during a write operation and synchronizes the data logic circuits during a read operation. An ID record consists of a sync field and an ID field. The data record consists of a sync field and a data field. The data field contains an address mark, 128, 256, or 512 data bytes, and two CRC bytes.

ID Record

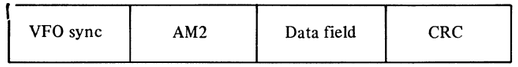
The ID record contains 13 bytes that are unique to each diskette sector.



- VFO (Variable Frequency Oscillator) sync. This byte consists of 6 bytes of zeros required for proper synchronization when reading from a diskette.
- AM1 (Address Mark). This byte (X'FE') signals the start of each ID field.
- C byte (Logical cylinder address). This byte contains a right-adjusted binary number that designates a specific diskette cylinder location from 00 to 76 (decimal).
- H byte (Head selection). This byte contains the side number as a hexidecimal value of X'00 or '01.'
- R byte (Record number). This byte identifies the sector number. It contains a right-adjusted binary number that represents a decimal value of 01 to 26 for 128-byte sectors, 01 to 15 for 256-byte sectors, and 01 to 08 for 512-byte sectors.
- N byte (Record length). This byte designates the byte length of each sector. It must have a hexidecimal value of X'00' (128 bytes), X'01' (256 bytes), or X'02' (512 bytes).
- CRC bytes (Cyclic redundancy check). A field of two bytes is appended to the ID field. The CRC field is created by the file attachment as it writes data on the diskette.

Data Record

Records are stored in the data portions of the sectors. If a record is less than the number of bytes used on a sector the remainder is padded with binary zeros, before the data field CRC bytes are written. If a record is longer than the number of bytes available on a sector, it is written over as many sectors as are required to complete the record.



- VFO (Variable Frequency Oscillator) sync. This byte consists of 6 bytes of zeros required for proper synchronization when reading from a diskette.
- AM2 (Address Mark). This byte will be either hex FB or F8. FB identifies the information that follows as being a data field and F8 identifies the field that follows as being a control field. The first byte of the control field can be D or F:
  D = deleted record
  F = defective record
- Data field. This field will have 128, 256 or 512 bytes of data depending on the sector size.
- CRC bytes (Cyclic redundancy check). A field of two bytes is appended to the data field. The CRC field is created by the attachment as it writes data on the diskette.

Specifications

- Data capacity—The chart below shows the capacity in formatted data bytes for the two diskette types in three formats.

Sector size in bytes	128	256	512
One-sided diskette	246,272[1]	284,160	303,104
Two-sided diskette	492,544[2]	568,320	606,208

[1] The basic data exchange format for an IBM Diskette 1.
[2] The basic data exchange format for an IBM Diskette 2.

- Data rate—250,000 bits (31,250 bytes) per second
- Cylinder to cylinder access time—5 ms (Head/carriage settle time is 35 ms for the last cylinder accessed. Therefore, the total access time is the number of cylinder crossings multiplied by 5 ms plus the 35 ms settle time.)
- Cylinders per diskette side—77 (Cylinder 00 is the label cylinder; cylinders 01 through 74 are data cylinders; cylinders 75 and 76 are reserved as alternate cylinders.)
- Records per track—8, 15, or 26, depending on the format scheme used.

Attachment Card

The attachment card is a single 4-wide, 6-high card which is mounted vertically in the processor card file or an I/O expansion file. The attachment card provides the data flow and control logic between the 4964 diskette unit and the processor channel.

Basic Data Flow

The processor I/O channel transfers data in parallel by word (16 data bits plus 2 parity bits). After checking for correct odd parity, the attachment card strips the parity bits, adds clock pulses, and transfers the data serially to the 4964 diskette unit. Data is transferred to or from storage in cycle steal mode or under direct program control (DPC). The I/O command determines the mode in which data is transferred and the direction of data movement.

There is one read and write channel common to both heads in the diskette. Only one operation (read or write/erase) is possible at a time, and on only one head at a time. Data read from a diskette is amplified and differentiated into file data pulses. These pulses are sent to the VFO logic where they are separated (clock from data) and transferred to the attachment card.

Maintenance

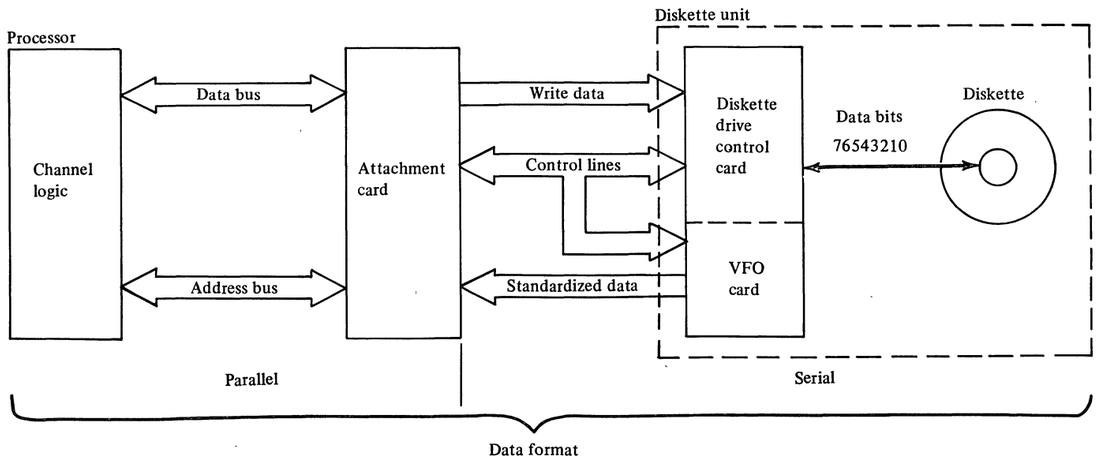
There is no scheduled maintenance for the 4964. To repair the drive, adjust internal components or replace field replaceable units (FRUs) as directed by the maintenance analysis procedures (MAPs) manual.

Diagnostics, repairs, adjustments, service checks, or verification of a problem can be done online using the system or offline isolated from the system. However, verification of a repair should always be done online using the system diagnostic programs.

For proper use of the MAPs and diagnostic programs, see the introductory pages of the MAPs and Diagnostic Users Guide.

CAUTION: The head/carriage assembly, the head timing block and the drive hub and pulley assembly are adjusted and tested at the factory. The head timing block assembly and the drive hub and pulley assembly are not field replaceable. If either assembly is damaged, the entire diskette drive should be replaced.

The head/carriage assembly is a FRU. However, do not clean or repair any part of this assembly.



Chapter 2.
Functional Units

Diskette Drive

Components of the diskette drive are:

- Cover Assembly
- AC Drive
- Stepper Drive

Cover Assembly

F Timing pins
G Cover assembly
H Collet
I Latch assembly

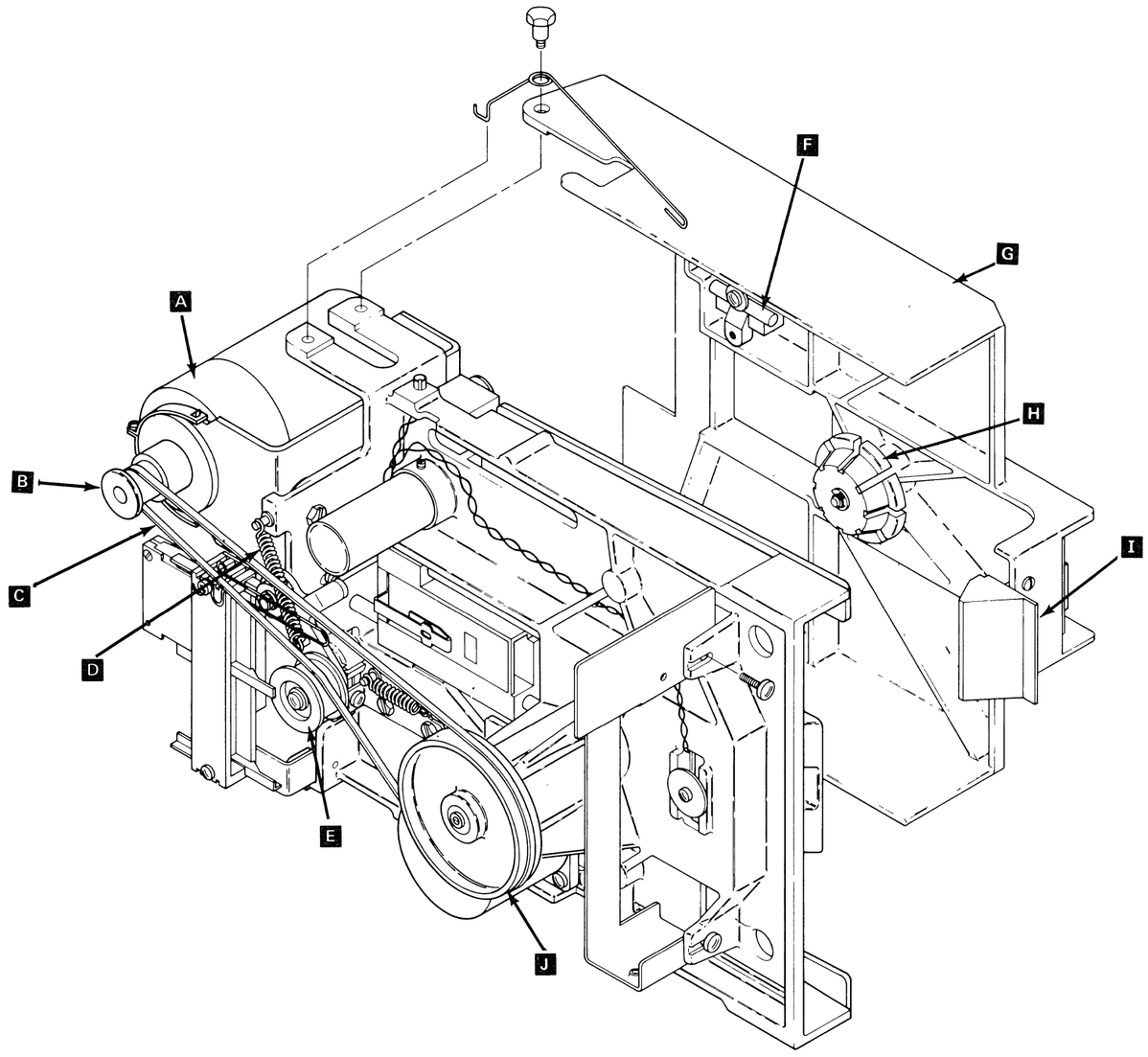
The diskette drive cover assembly pivots to accept the diskette. The diskette is automatically centered and clamped to the drive by the collet.

Two timing pins are stored in a holder located inside the cover assembly.

AC Drive Components

A Drive motor
B Drive Pulley
C Belt
D Idler spring
E Idler assembly
J Hub

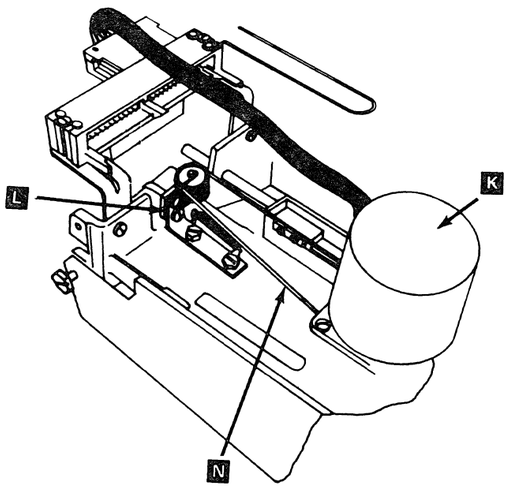
The motor rotates the diskette at a speed of 360 rpm with the heads loaded.

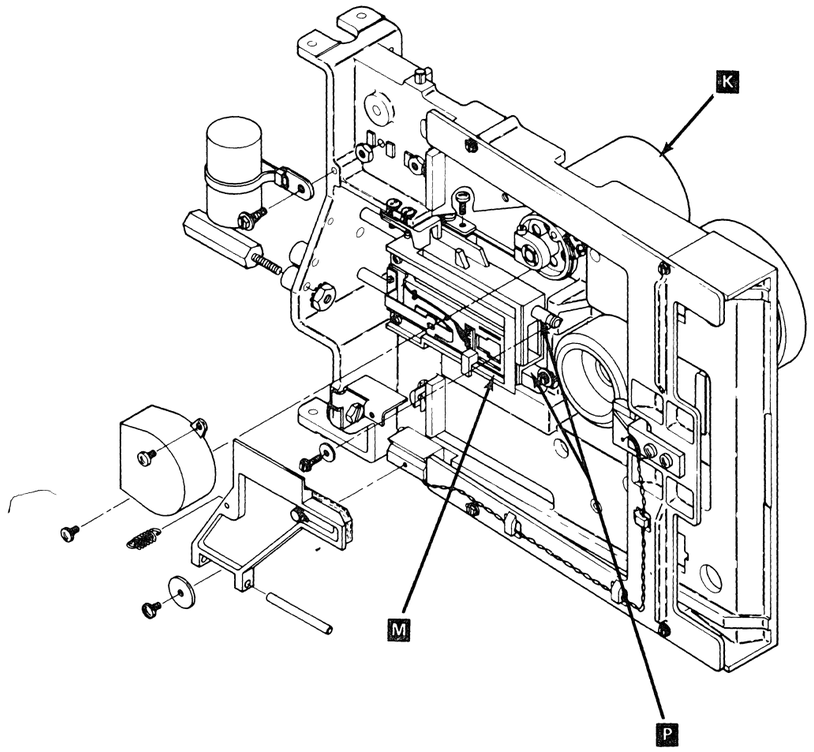


Stepper Drive Components

K Stepper motor
L Stepper idler assembly
M Head/carriage assembly
N Stepper drive band
P Guide rods

The stepper motor shaft turns in increments of 1.8° in either direction under control of access pulses. This motion causes the head/carriage assembly M to move along two guide rods P, moving the heads across the diskette surface a distance equal to one cylinder.





Stepper Motor

- The stepper motor is a sealed unit.
- The stepper motor is phase controlled by direct current.
- When not turning, the stepper motor locks in an electrically detented position.
- The sequence of the phase pulses from the logic circuits controls the direction of rotation.

The dc stepper motor consists of a permanent-magnetic rotor (armature) and a pair of two-phase stator windings. The motor is a sealed unit having no gears or commutators and requiring no maintenance.

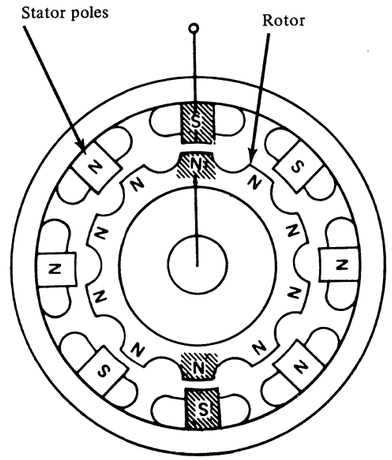
Shaft rotation is not continuous unless the stepper motor is continually pulsed. When current flows through the stator windings, a magnetic field set up in the stator pole acts on the permanent-magnet rotor to provide torque in the rotor shaft. This torque turns the rotor shaft only part of a revolution; then locks it in an electrically detented position. Electrical detenting is due to direct current in the stator windings acting on the permanent-magnet rotor.

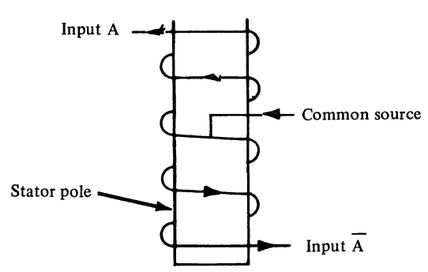
Note. The motor cannot be easily turned by hand with the power on. When the power is off, the residual detenting due to the permanent magnet may be felt as a drag or roughness, and heard as a clicking sound when the shaft is turned.

Stepper Motor Operation

For ease of understanding, the motor used in this example turns nine degrees per step, the actual is 1.8 degrees per step.

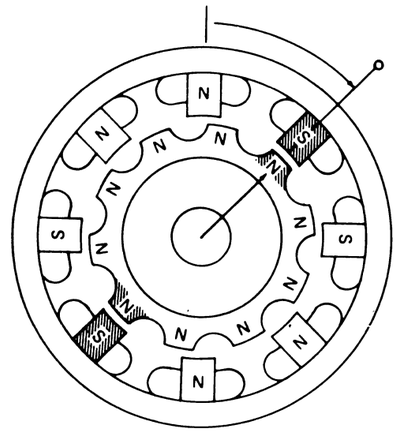
This simplified stepper motor consists of eight coilwound stator poles and a tenpole permanent-magnet rotor.





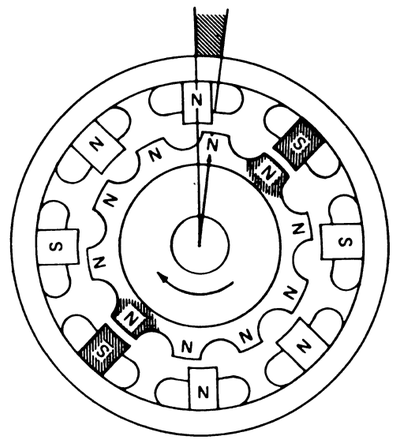
CAUTION: The permanent-magnet rotor is magnetized after assembly at the plant of motor manufacturer. Do not open or disassemble the motor. Disassembling the stepper motor reduces the magnetic flux of the rotor, which reduces the torque of the motor.

If you physically rotate the stator (in either direction), the rotor maintains its detented position and follows the stator as shown. (Both the stator poles and the rotor rotated clockwise 45 degrees.)



Note. Current flows only in one-half of the winding at a time. Polarity of the stator pole is determined by which half of the winding has current.

If, instead of physically rotating the stator, you electrically rotate its magnetic field (by switching current in the stator winding), the stator remains stationary and the rotor turns until the closest opposite-polarity (shaded) magnet poles attract each other into alignment. Note that polarity of the stator poles has rotated one position clockwise from that shown in the first illustration.

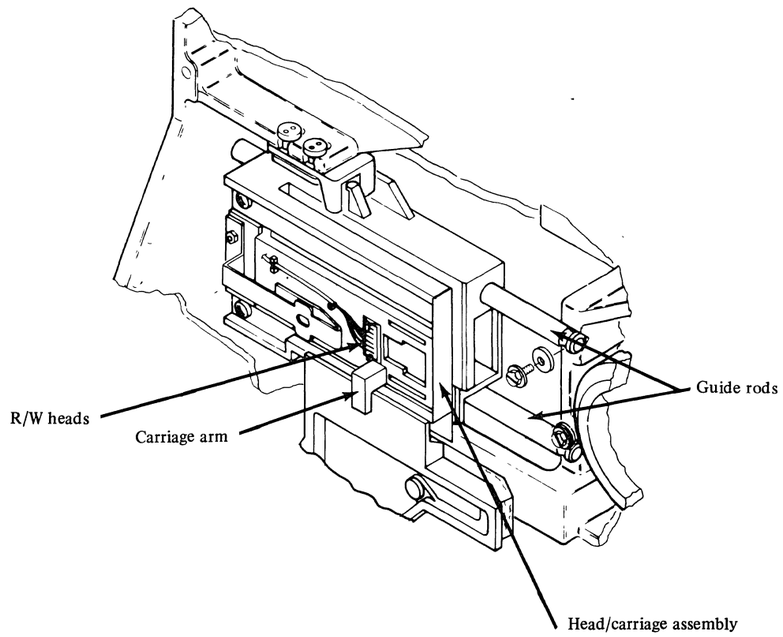


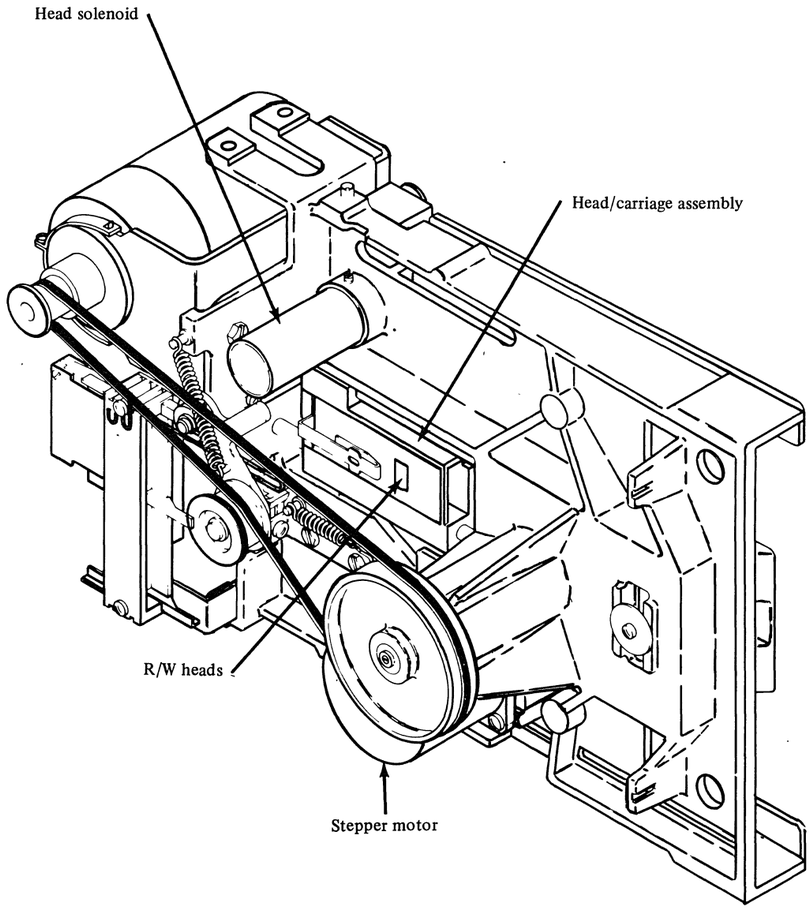
Direction of rotation depends on the sequence of stator magnet switching.

Head/Carriage Assembly

The head/carriage assembly consists of two read/write heads mounted on a common carriage. The assembly moves under control of the stepper motor. The read/write heads provide the read, write, and erase functions required to record and retrieve data from either side of the diskette.

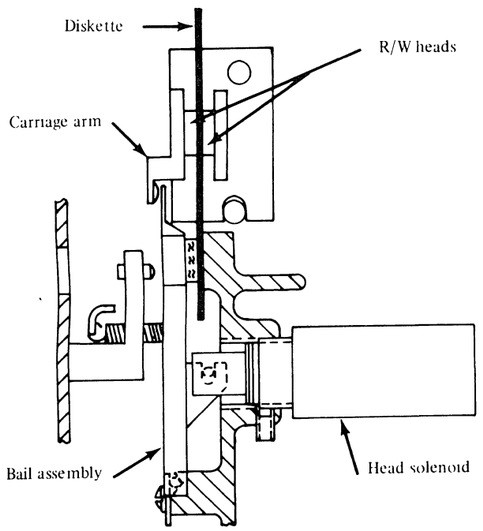
CAUTION: The head/carriage assembly is a factory adjusted and tested at the factory. Do not attempt to repair or clean any part of this assembly.



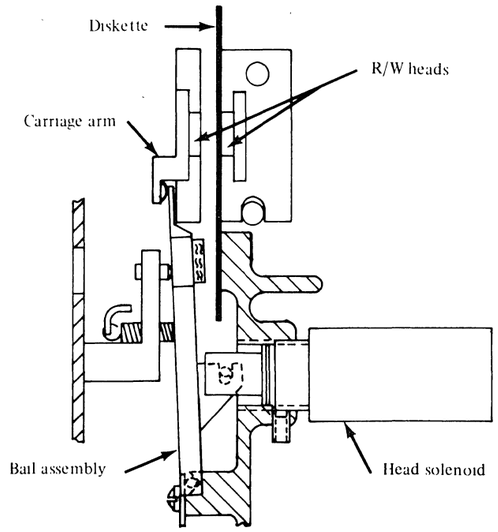


Head Load Solenoid/Bail Assembly

The head engage line controls the head load solenoid. When the head engage line is active, the head load solenoid is energized and the bail assembly closes allowing the heads to touch the diskette surface. At this time the heads are loaded. The heads are loaded before a read or write operation. The heads are unloaded after no more than one-half of a revolution if another read or seek operation is not executed. This reduces wear to the diskette and read/write heads.



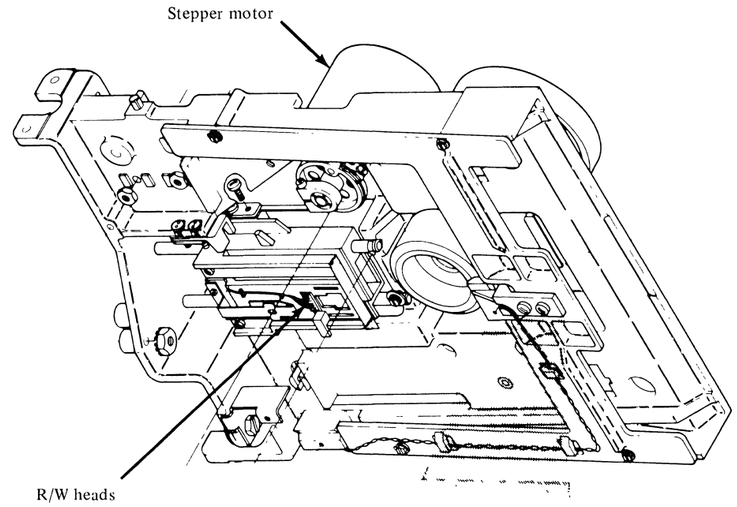
Heads-loaded

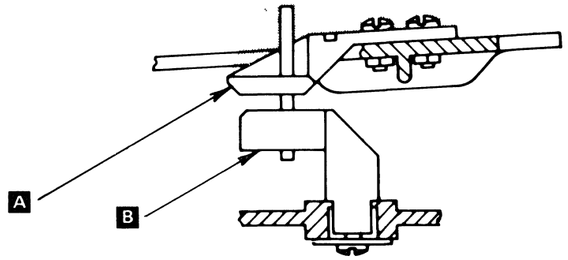


Heads-unloaded

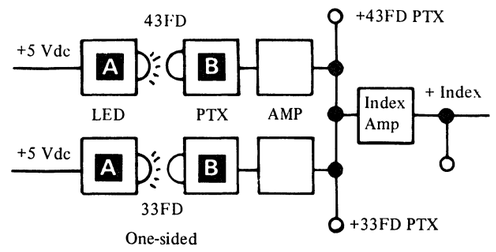
LED/PTX Assemblies

The light emitting diode (LED) and phototransistor (PTX) assemblies provide a means of detecting the diskette index and identifying the type of diskette inserted (diskette 1 or diskette 2).





Two-sided



LED/PTX Circuitry

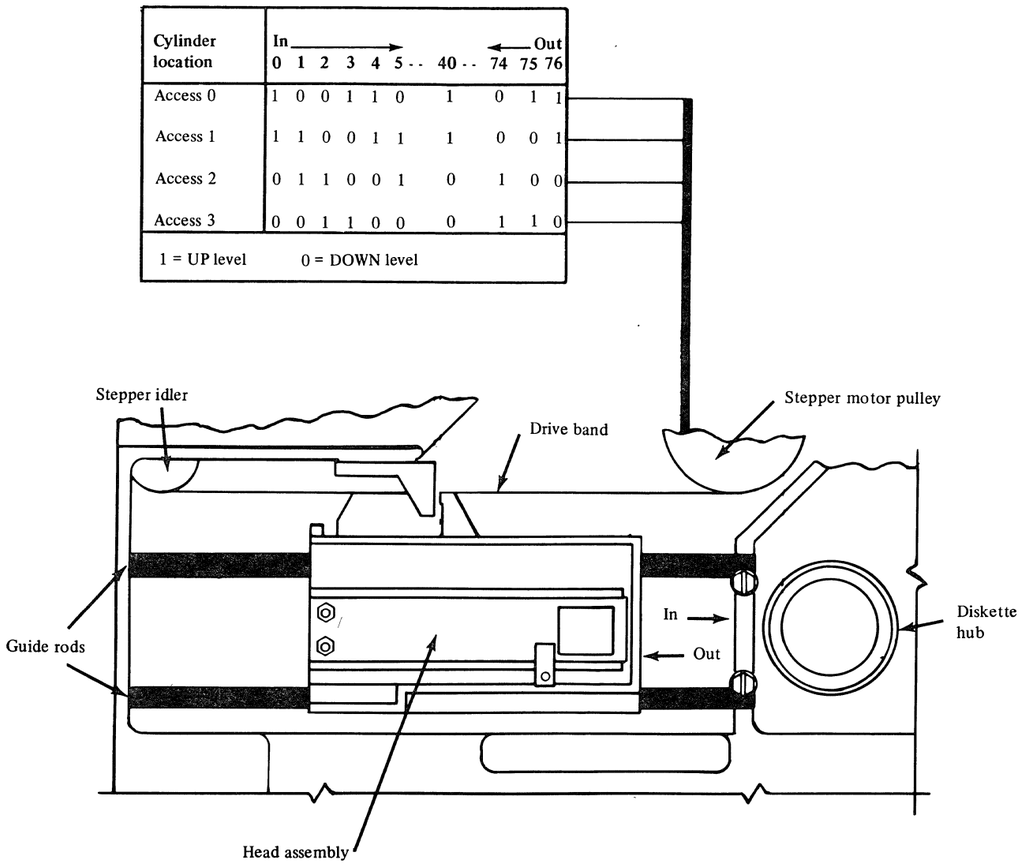
Head Access

There are four access lines, labeled 0 through 3. When sequenced, these lines move the head assembly by pulsing the stepper motor. The head assembly travels in towards the diskette hub and out away from the diskette hub along the guide rods.

Cylinder 0 is the home position for the head assembly. Accessing occurs at about 200 tracks per second or one cylinder every 5ms.

Cylinder location	In → 0	1	2	3	4	5	--	40	--	← Out 74	75	76
Access 0	1	0	0	1	1	0		1		0	1	1
Access 1	1	1	0	0	1	1		1		0	0	1
Access 2	0	1	1	0	0	1		0		1	0	0
Access 3	0	0	1	1	0	0		0		1	1	0

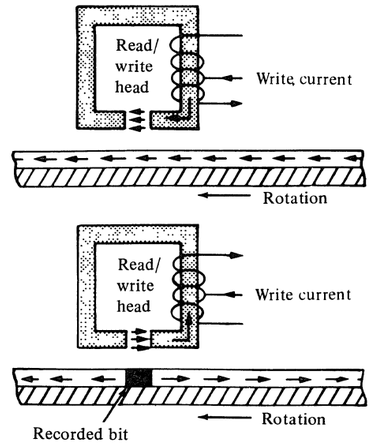
1 = UP level 0 = DOWN level



Read/Write Heads

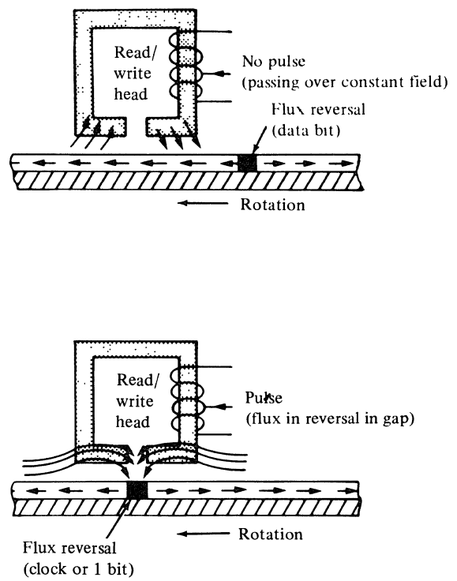
Writing

During a write operation, a clock or 1 bit is recorded by reversing the direction of the current in the coil, which reverses the flux direction in the pole piece and reverses the flux in the gap. At the instant that the flux in the pole piece gap reverses, the direction of magnetization changes on the disk surface. Each reversal represents a recorded clock or 1 bit.



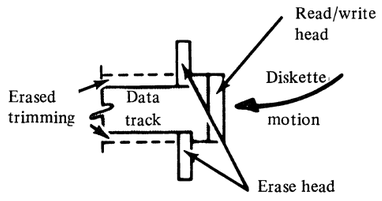
Reading

During a read operation, with the recording surface magnetized in one horizontal direction, constant flux flows and the coil registers no output voltage. However, when a recorded bit (180 degrees horizontal flux reversal) passes the gap, the flux flowing through the ring and coil also reverses and produces a voltage output pulse.



Controls

The write gate is active only during a write or format operation. This line allows current to flow through the read/write head and also degates the read circuits. When write gate is inactive, the write circuits are deconditioned and the read circuits are conditioned to read.

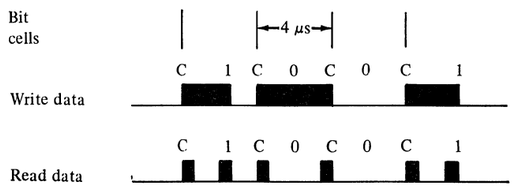


Erase gate is also active only during a write or format operation. This causes the edges of the data track to be erased. The edges are erased to provide a gap between tracks and to ensure that old data is completely erased.

Data Representation

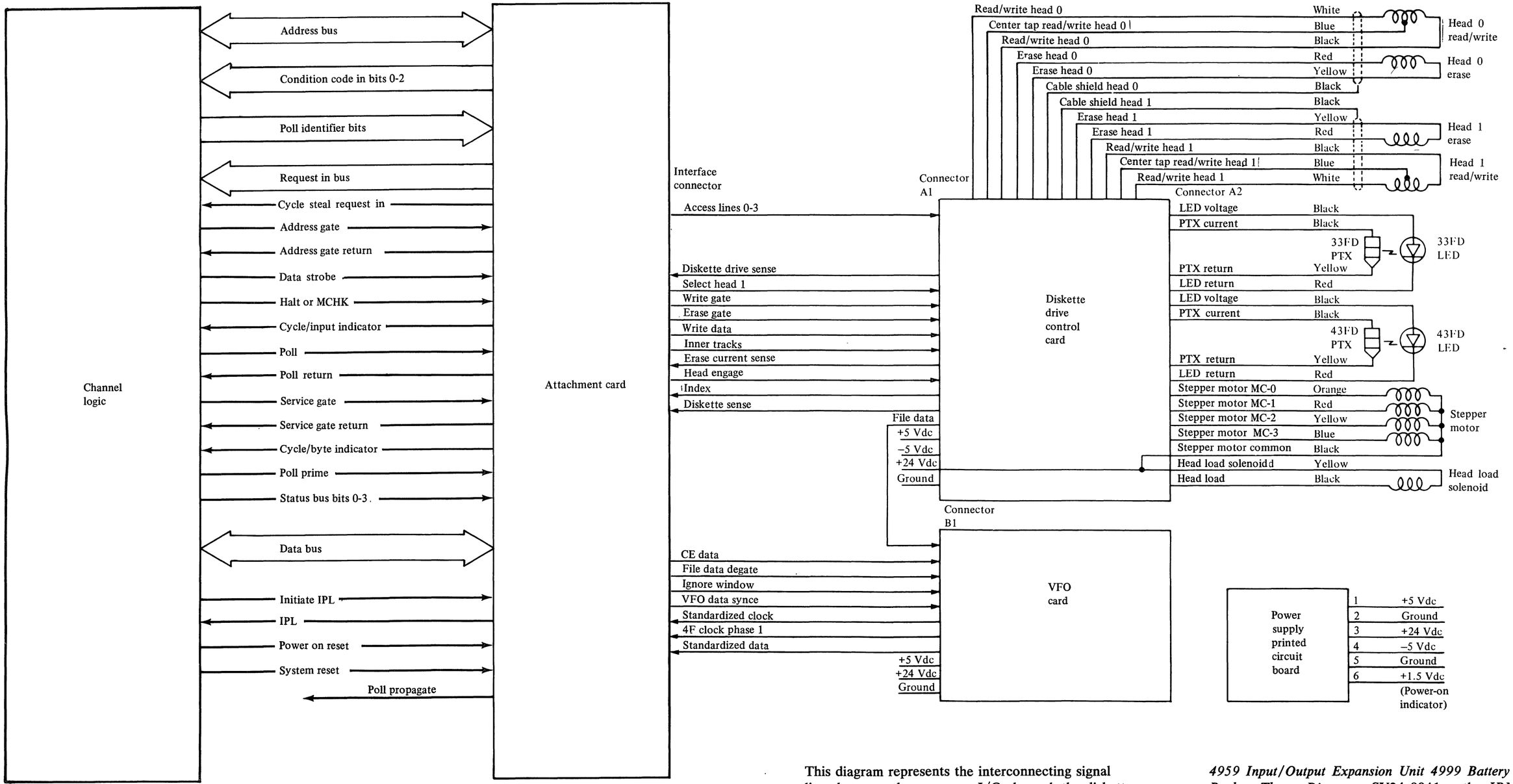
For each transition of the write data line, a clock bit or a 1 bit is written on the diskette. The absence of a change between clock bits represents a zero or a no-bit. Transitions of the write data line cause the current to be switched in the read/write head which results in a polarity change on the diskette track. Thus a polarity change on the diskette represents a clock bit or a 1 bit. The period of time from one clock bit to the next clock bit is known as a bit cell and is a nominal 4us in duration. Data bits are written in the middle of the data cell.

By comparison, bits represented on the write data line as transitions are represented on the read data line, when read as positive pulses with a nominal width of 150 ns. The separation of clock bits and data during a read operation takes place in the VFO card.



Chapter 3.
Circuit Functions

Attachment and Device Circuit Cards



This diagram represents the interconnecting signal lines between the processor I/O channel, the diskette attachment feature card, the diskette drive control card, and the diskette VFO card. The processor I/O channel lines are common to all Series/1 I/O attachment cards and are described in the *IBM Series/1 4955 Processor and Processor Features 4959 Input/Output Expansion Unit 4999 Battery Backup Theory Diagrams*, SY34-0041 or the *IBM Series/1 4953 Processor and Processor Features 4959 Input/Output Expansion Unit 4999 Battery Backup Unit Theory Diagrams*, SY34-0042. The remaining lines are defined in the following diagrams and associated text.

Attachment Feature Card

The attachment card is a single 4-wide, 6-high card which is mounted vertically in the processor card file or an I/O expansion file. The attachment card provides the data and logic communications between the 4964 diskette unit and the processor channel logic, and performs the following functions:

- Interprets and executes commands from the processor.
- Transfers data in parrallel by word.
- Furnishes status information to the processor and reports condition codes after I/O instruction and during an interrupt.
- Checks the accuracy of transferred data.
- Provides cyclic redundancy checking.
- Controls the sequencing of all data operations.
- Generates and stores all status and error conditions.
- Selects head that data is to be read or written with.
- Furnishes controls between the attachment feature card and the diskette unit.
- Provides a path for data between the attachment feature card and the diskette unit.
- Serializes and deserializes data.

The following diagrams and associated line definitions are for instructional purposes. They illustrate the diskette attachment feature card, diskette drive control card, and diskette VFO card.

Data Bus (Bits 0–15)

During a write operation, the data bits are loaded into the data register one word at a time. The bits are placed on controller 'Data In' by controller sets or resets. Bits 0–7 are placed first, then bits 8–15. The controller places the bits on its 'Data out' one byte at a time and they are loaded into the polarity hold (PH) buffers. The data is loaded one byte at a time into SER-DES. 'Write gate' loads the bits serially onto the 'write data' line which exits to the diskette unit.

During a read operation, the 'standardized data' line from the diskette unit is clocked into SER-DES by 'FCU clock.' The data is deserialized and loaded into the PH buffers a byte at a time. The controller places the data on its 'data in' lines. Byte 0 is placed on the 'data out' lines and loaded into data registers 0–7. Byte 1 is loaded into data registers 8–15.

Address Bus (Bits 0–15)

Address bus bits 0–7 are the command, and bits 8–15 are the device address. Bits 8–15 are compared to the address jumpers. If they compare and address bus bit 16 is on, the 'card select power' line is brought up. 'Card select power' gates bits 0–7 to circuits which decode the command.

To send a storage address to the controller, it is loaded in the data register and placed on the controller 'data in' lines one byte at a time. To send a storage address from the controller it is placed on the controller 'data out' lines one byte at a time and is loaded into the data register.

Request In Bus (Bits 0–15)

With a prepare command, data register bits 11–14 contain the level the device is to be prepared to (4 bits hex for a total of 16 levels). From the data register the four bits are gated to the level bit latches by the 'prepare' line that was decoded from the command field. When the 'interrupt request' line is raised, the four level bits are decoded and the proper line raised on the bus.

Address Gate and Address Gate Return

The 'address gate' line is OR'd with the 'data strobe' line. If either line is on when the correct device address is decoded, 'address gate return' is raised.

Data Strobe

'Data strobe' is AND'd with 'service gate capture' to set the cycle steal status latches. Data strobe is AND'd with 'prepare' line and 'not parity error' to set the level latches. 'Data strobe' is OR'd with 'address gate' to set 'address gate return' when the correct device address is decoded. 'Data strobe' OR'd with 'service gate' sets 'service gate return' when 'poll capture' is raised. 'Data strobe' also resets the 'controller reset IPL' line.

System Reset, POR, Halt or MCHK

These three lines are OR'd to form the 'interface resets' (I/F resets) line. 'I/F resets' activates 'controller reset' and the 'OR of resets' lines. These lines reset most of the latches.

'System reset' and 'power on reset' (POR) are also OR'd to make the 'reset I bit' line. 'Reset I bit' resets the 'poll capture,' 'I bit,' and 'level bit' lines.

Poll, Poll Prime, Poll Propagate, Poll Return

'Poll' and 'poll prime' are AND'd to make 'poll repower.' 'Poll repower' is AND'd with 'poll propagate' latch to make the 'poll propagate' interface line.

If there is no cycle steal request pending the 'poll repower' line sets the 'poll propagate' latch and is also AND'd with the 'poll propagate' latch to make the 'poll return' line.

Service Gate, Service Gate Return

'Service gate' is OR'd with 'date strobe' and the resulting line is AND'd with 'not data strobe' to reset 'poll capture.' This line also sets the 'service gate return' tag.

Initiate IPL, IPL

'Initiate IPL' sets the IPL latch which turns on the 'IPL interface' line. IPL latch also sets the I bit latch which is AND'd with an interrupt request to make the 'interrupt request' line.

Cycle Steal Status Bus (Bits 0–3)

'Service gate capture' AND'd with 'data strobe' gates this four bit buts into the cycle steal latches. The controller places the contents of the latches on the controller 'data in' bits 4–7.

Poll ID Bits (0–4)

Poll ID bits 0, 3, and 4 and 'cycle steal request' pending sets the 'cycle steal request' compare latch. This latch blocks the sending of 'poll propagate.'

Poll ID bits 1–4 are exclusive OR'd with level latches 0–3. These four outputs are AND'd. The output is AND'd with not poll ID bit 0. This output sets the interrupt request compare latch which blocks the sending of 'poll propagate.'

Condition Code in (Bits 0–2)

The 'service gate capture' and 'address gate return' lines are decoded with error latches to form the correct condition code.

A controller set or reset will load the controller 'data out' bits 5–7 into condition code latches. These latches are gated onto the condition code bus by AND'ing 'address compare' and address bus bit 16.

Cycle Input Indicator

A controller out command sets the cycle steal write latch. The output of this latch is AND'd with 'service gate capture' to make the 'cycle input indicator' line.

Cycle Byte Indicator

A controller set or reset turns the byte mode latch on. This latch is AND'd with 'service gate capture' and 'cycle steal request' to make the 'cycle byte indicator' line.

Access Lines 0–3

A controller set or reset is AND'd with controller 'data in' bits 0–3 to make the access lines.

Inner Tracks

A controller out command is AND'd with controller 'data in' bit 4 to make the 'inner tracks' line.

Select Head 1

A controller set or reset sets 'select head 1.'

Write Gate

A controller set or reset sets the write gate latch. This line is AND'd with 'not file date degate' to make the 'write gate' line.

Erase Gate

A controller set or reset sets the erase gate latch. This line is AND'd with 'not file data degate' to make the 'erase gate' line.

CE Data

A controller set or reset sets the block clock latch during a write operation. When 'block clock' is on, 'write clock sync' and 'serial data' are AND'd to make 'CE data.'

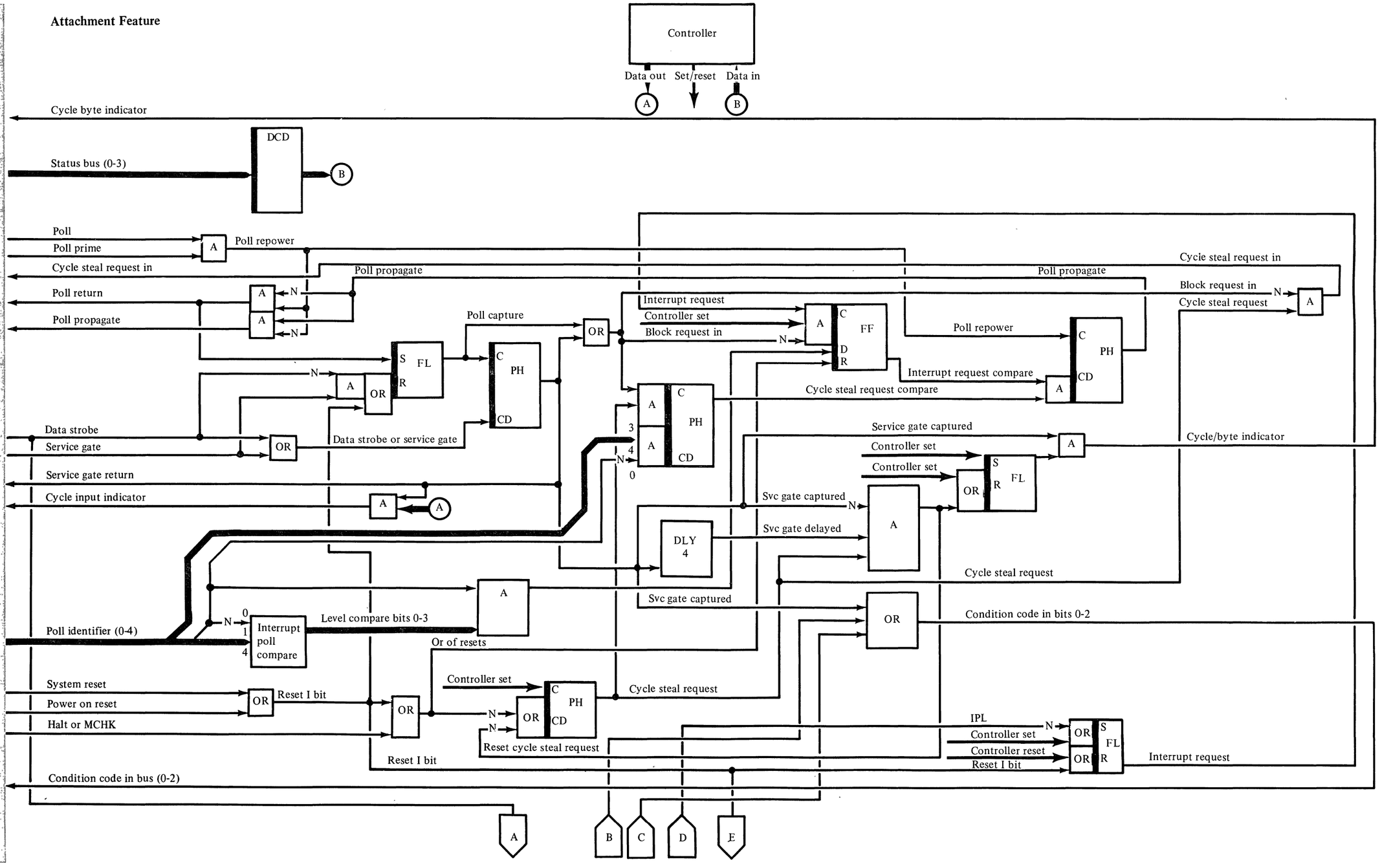
A controller set or reset resets the block clock latch. This allows the 'write clock (clock phase)' line to be on the 'CE data' line.

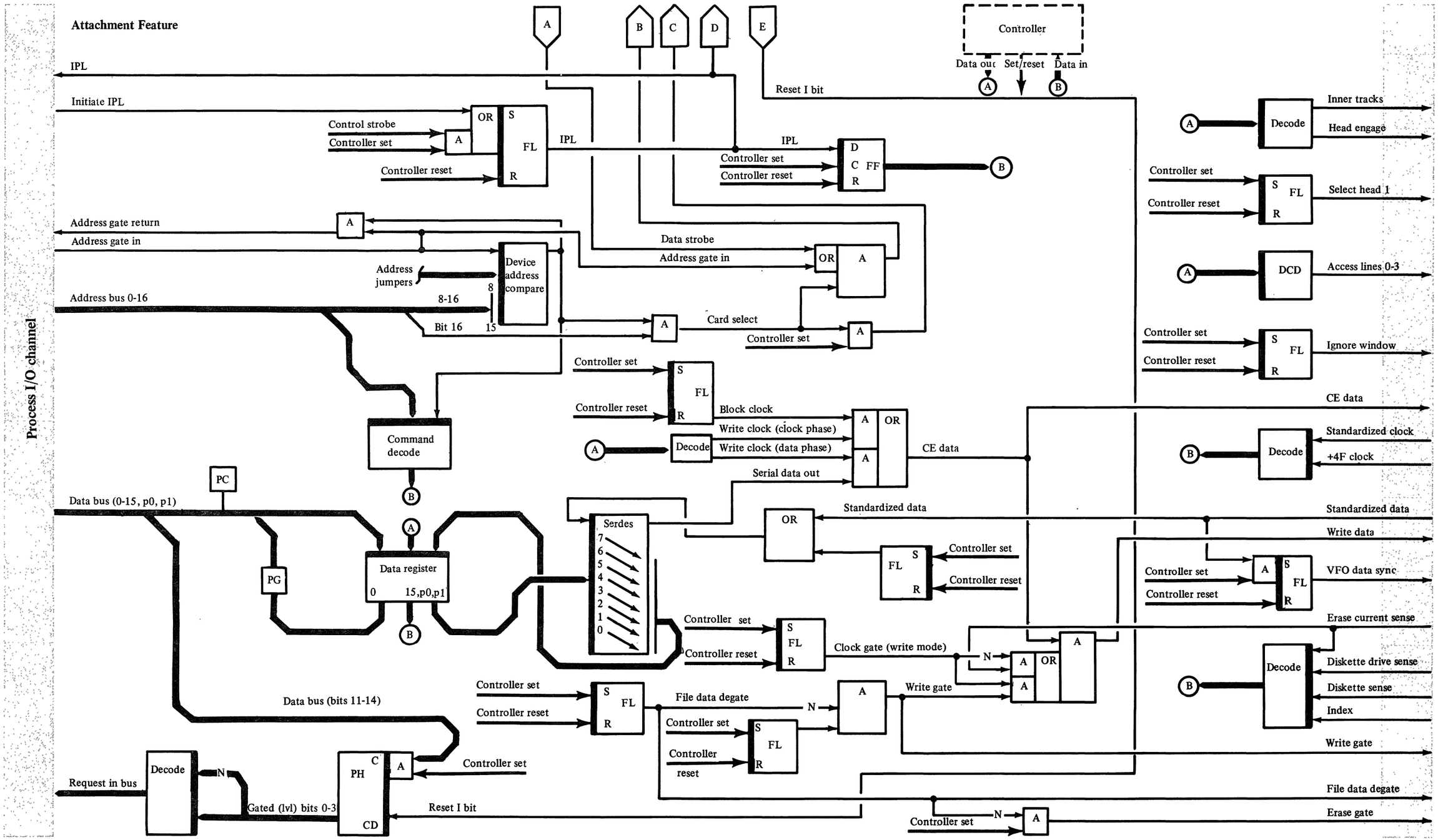
Write Data

'Erase current sense' is AND'd with 'not clock gate (write mode).' 'Write gate' is AND'd with 'clock gate (write mode).' The outputs of these two ANDs are OR'd and that output is AND'd with the 'CE data' line to make 'write data.'

Processor I/O channel

Attachment Feature




Process I/O channel
Attachment Feature
Diskete drive control card
IPL
Initiate IPL
Control strobe
Controller set
Controller reset
OR
A
S
FL
R
IPL
Reset I bit
Controller
Data out
Set/reset
Data in
D
C FF
R
Address gate return
Address gate in
Address jumpers
Device address compare
8
8-16
Address bus 0-16
Bit 16
15
Data strobe
Card select
Command decode
Controller set
Controller reset
Block clock
Write clock (clock phase)
Write clock (data phase)
Decode
Serial data out
CE data
PC
PG
Data bus (0-15, p0, p1)
Data register
0 15,p0,p1
Serdes
7
6
5
4
3
2
1
0
Standardized data
Clock gate (write mode)
N
Write gate
File data degate
Data bus (bits 11-14)
Request in bus
Gated (lvl) bits 0-3
PH
C
CD
Reset I bit
Erase gate
Inner tracks
Head engage
Select head 1
Access lines 0-3
Ignore window
Standardized clock
+4F clock
Write data
VFO data sync
Erase current sense
Diskette drive sense
Diskette sense
Index

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Ignore Window
A controller set or reset sets this line.

Data Sync
'Standardized data' is AND'd with 'AM search' to set the 'data sync' line.

File Data Degate
A controller set or reset and controller 'data out' bit 6 set the 'file data degate' line.

Head Engage
A controller set or reset and controller 'data out' bit 5 set the 'head engage' line.

Index
This line is inverted while activating a single shot. The single shot output is OR'd with the index trigger. The output of this OR is AND'd with a controller set or reset to make controller 'data in' bit 1.

Standardized Clock, 4F Clock
'Standardized clock' and '4F clock' trigger plus logic to form 'read clock (clock phase)' and 'read clock sync (data phase).' These clocks are used in the SER-DES to clock the data.

Attachment feature card

Diskette Drive Control Card

Read/write head 0 — White
Center tap read/write head 0 — Blue
Read/write head 0 — Black
Erase head 0 — Red
Erase head 0 — Yellow
Head 0
Cable shield head 0
Cable shield head 1
Erase head 1 — Yellow
Erase head 1 — Red
Read/write head 1 — Black
Center tap read/write head 1 — Blue
Read/write head 1 — White
Head 1

Write data
Inner tracks
Write gate
Select head 1
Write driver
Head select logic
Pre-amp
Differen-tiator
Detector
Line driver
File data
A

Erase gate
Erase driver

Erase current sense
Sense driver

Access lines 0-3
Access degate logic
A
A
A
A
Driver
Driver
Driver
Driver
Head load solenoid

Ground
Diskette drive sense
+24 V dc

Head engage
Pre-driver
Driver

+5 V dc

Index
Diskette sense
Driver
Driver
Logic
Amp
Amp
33FD PTX
Logic
PTX
LED
PTX
LED
43FD PTX return
43FD LED return
33FD PTX return
33FD LED return

Diskette Drive Control Card

The diskette drive control card *B* provides the drive circuits for the stepper motor, head load solenoid, and the write and erase functions. It also provides the amplifiers for the read heads and the LED/PTX circuitry. The diskette drive control card is supported by a card retainer located between it and the stepper motor.

Note. The diskette drive control card is oriented with the components and test pins facing out. This card does not have to be removed when probing test pins.

Diskette Drive Control Lines

Access Lines 0, 1, 2, 3. These four lines cause the head assembly to move to the desired track.

Diskette Drive Sense. This line is always at a down level.

Select Head 1. This line selects the proper head and side of diskette. A down level selects head 0 and an up level selects head 1.

Write Gate. When at an up level, this line conditions the write select and write current source circuits for a write operation.

Erase Gate. When at an up level, this line conditions the tunnel erase circuits for an erase operation.

Write Data. This line is active only during write operations. Whenever this line changes state, a 1 bit or a clock is recorded on the diskette.

Inner Tracks. This line selects the proper write current for the track being written or allows increased amplifier gain when inner tracks are being read.

Erase Current Sense. This line is at an up level if the erase driver circuits are on.

Head Engage. An up level on this line energizes the head load solenoid.

Index. This line is at an up level whenever the index hole passes the LED/PTX.

Diskette Sense. This line uses the index pulse to determine which diskette is in the diskette drive.

VFO Card

The variable frequency oscillator (VFO) card receives data from the diskette drive control card and sends standardized data to the attachment card. The VFO card receives control instructions for data separation from the attachment card.

VFO Control Lines

CE Data. This line provides a stream of input pulses from the attachment card. It can be used to check operation of the data separator.

File Data Degate. This line allows the attachment to select either File Data or CE Data as the input stream to the data separator.

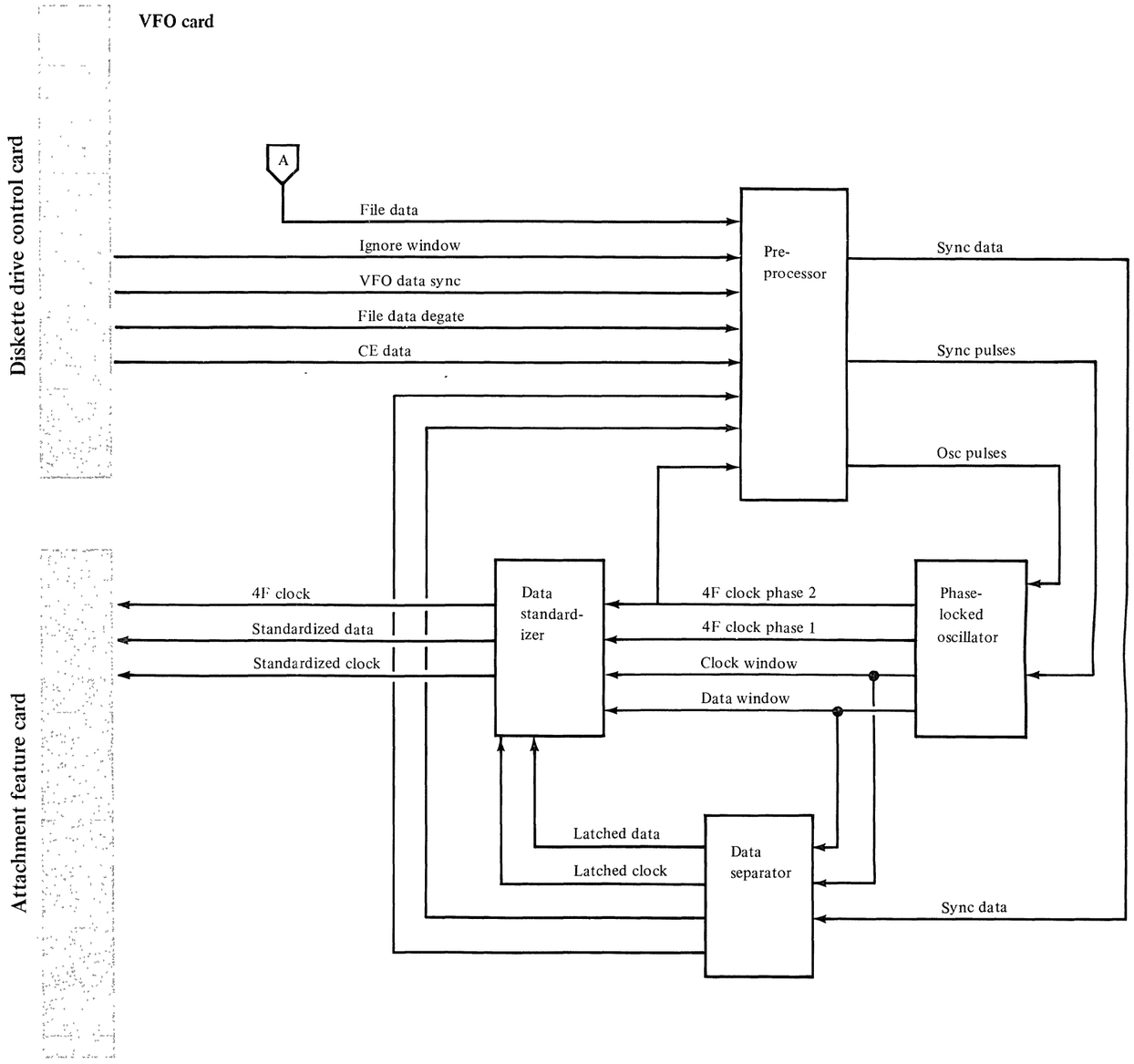
Ignore Window. This line is brought up by the attachment when start of VFO synchronization is desired.

VFO Data Sync. This line is raised so that pulses which fall within the Data Window are gated into the Phase Discriminator.

Standardized Clock. This line provides a clock pulse for each recorded magnetic transition that occurs during a clock window.

4F Clock Phase 1. This line provides a pulse to the attachment card that is coincident with a Standardized Data Pulse or a Standardized Clock Pulse.

Standardized Data. This line is the data channel output for the 4964 Diskette Unit.



Functions

Seek

A seek normally preceeds every data transfer operation to the diskette unit. A seek occurs when an operation requires a move of the R/W heads to another cylinder or a change in R/W head selection. This is accomplished by sequencing the four access lines, see (*Access lines*). The seek operation can be used to change: R/W head selection, only; cylinder location, only; or both. An interrupt request is sent to the processor when the diskette unit completes the operation. The types of seek operations are:

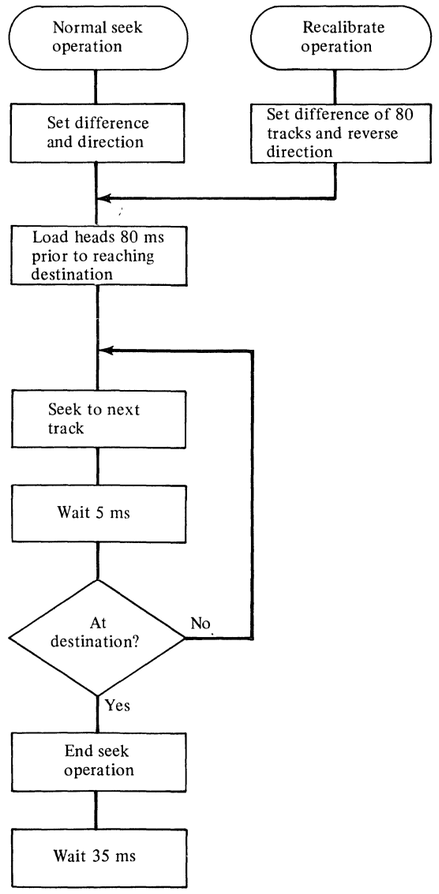
- Normal seek—seek from present known location to a specified destination track.
- Recalibrate—seek from the present location which (may be unknown) to track zero.

Seek Recalibrate

The recalibrate operation is necessary when the track location of the head is unknown. The attachment sets up a seek reverse of 80 tracks. Because there are only 77 tracks on the diskette, this is enough to drive the head to track zero from any location. After arriving at track zero, the access mechanism comes against a final stop and even though seek commands continue to be issued, the head remains at track zero.

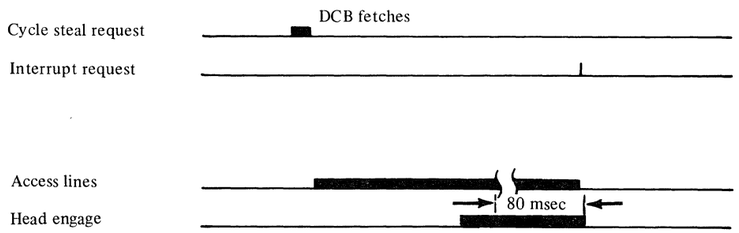
Seek Operation

The following flow chart shows seek and seek recalibrate operations.



Seek Timing

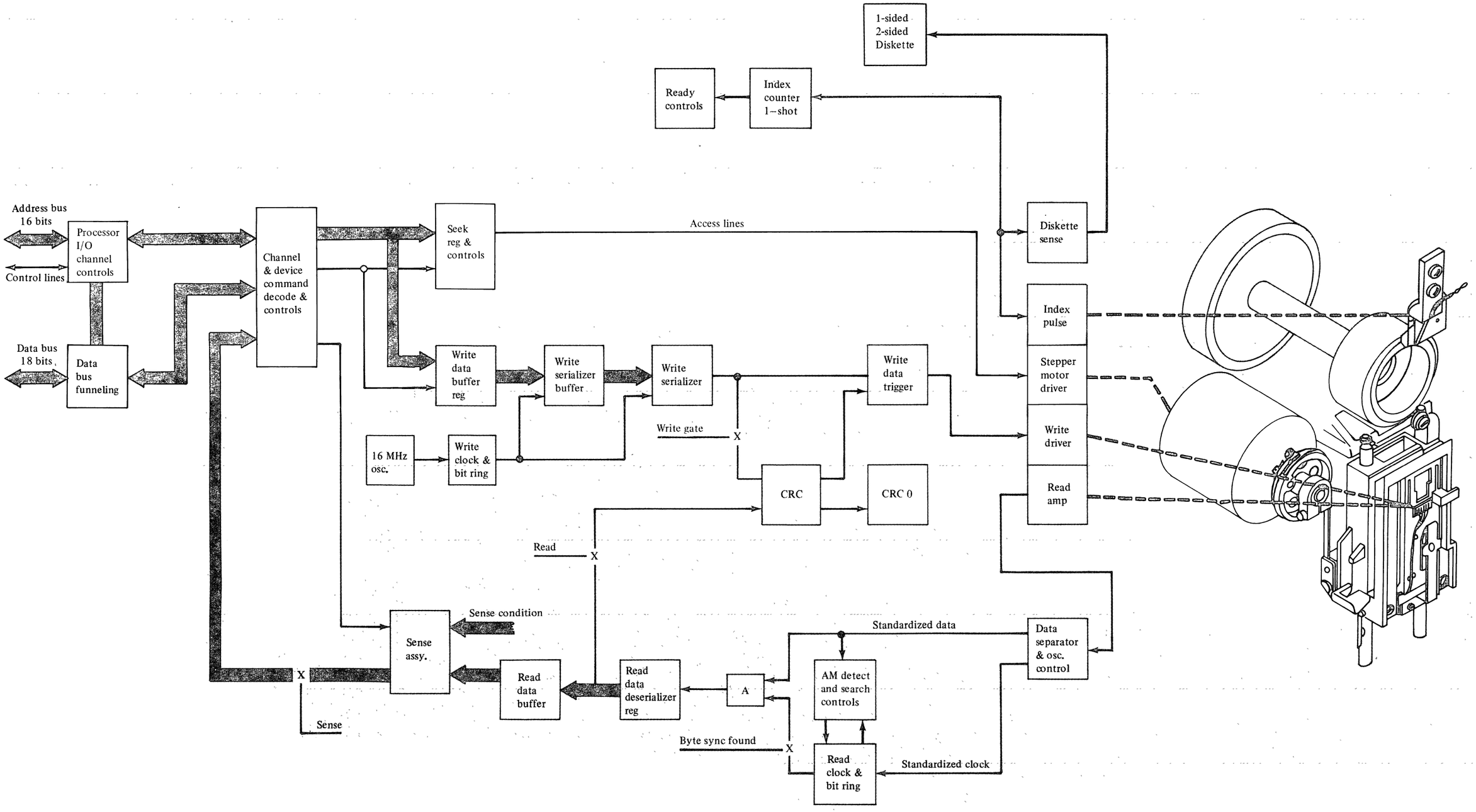
The following timing chart shows the relationship of the line sequencing during a seek operation.



Notes.

1. Seek time is 5 msec per track plus 35 msec for final track.
2. Heads remain loaded 80 msec after interrupt.
3. File can seek with heads loaded.

Seek Data Flow



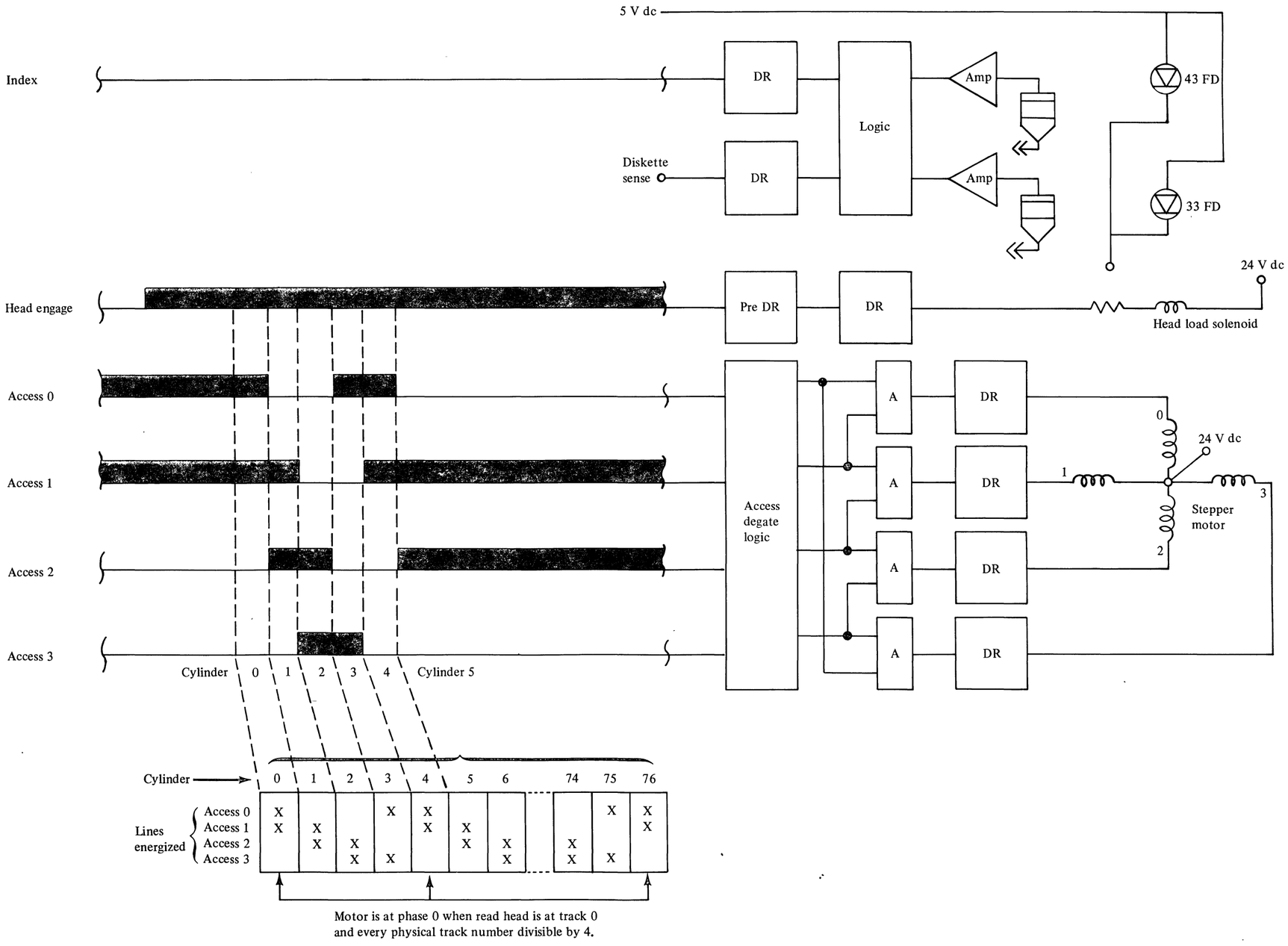
Access Lines

Access to the desired cylinder is accomplished by sequencing the four access lines to move the head/carriage assembly. The index pulse activates the ready controls to indicate that a diskette is in place and up to speed.

Before accessing, the heads are loaded by the head engage line. This energizes the head load solenoid. Head location is determined by reading the data address bytes of the first available ID field.

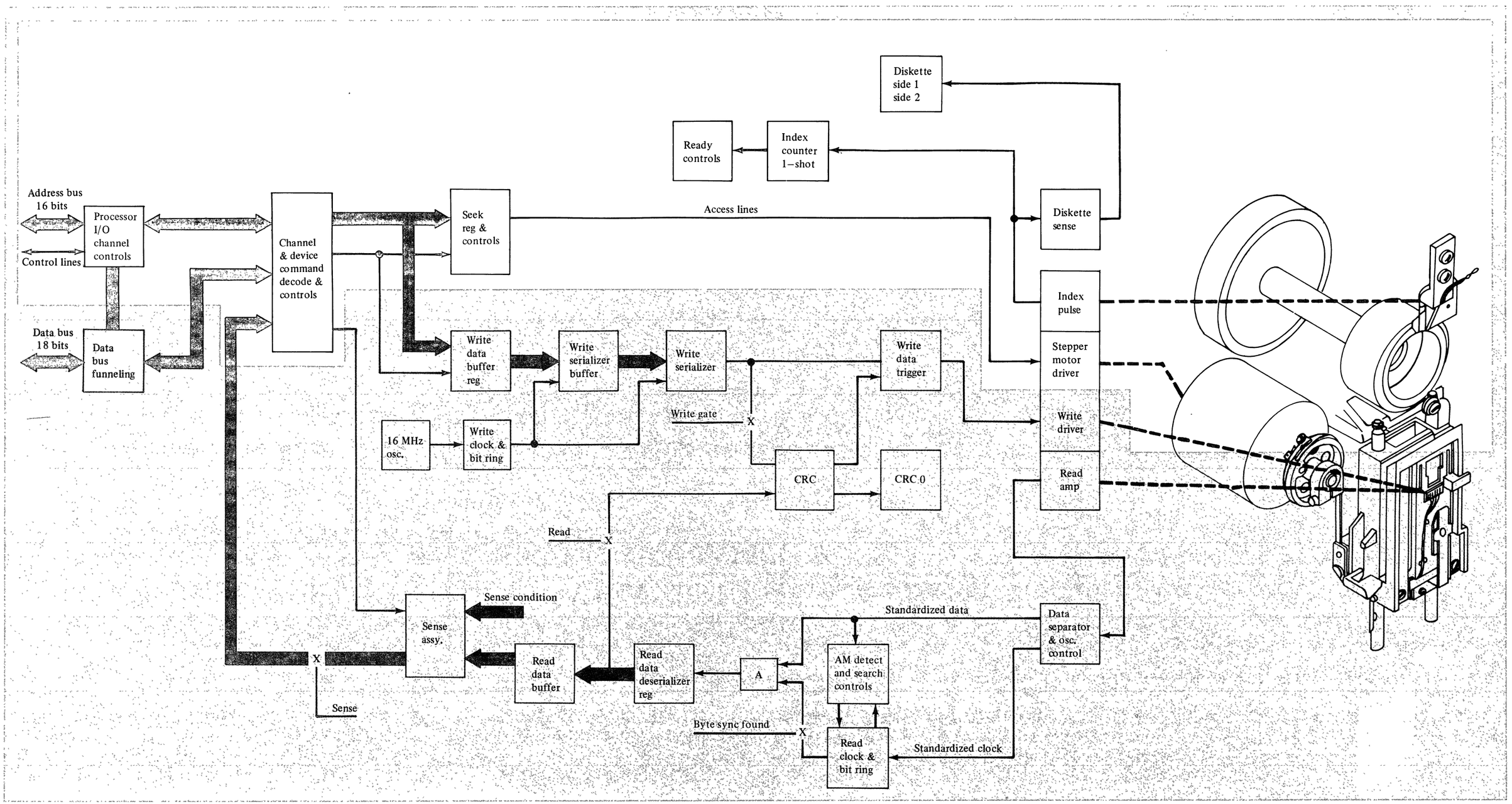
When the head engage line is activated, a minimum of 80 ms elapses before a read or write operation is performed. The heads are unloaded after no more than one revolution if a read, write, or seek is not executed.

Note. The heads must not be engaged unless a diskette is in place in the diskette drive.



Motor is at phase 0 when read head is at track 0 and every physical track number divisible by 4.

Access Data Flow



Read

During a read data operation, the attachment retrieves a data record stored in one or more sectors on the diskette and transfers the data into processor storage locations. Data is transferred in cycle steal mode and an interrupt request is sent to the processor when the operation is completed.

After the reading of bytes has started, the program must take the bytes at a nominal rate of one byte every 32 us. A failure to take the bytes fast enough causes a read overrun.

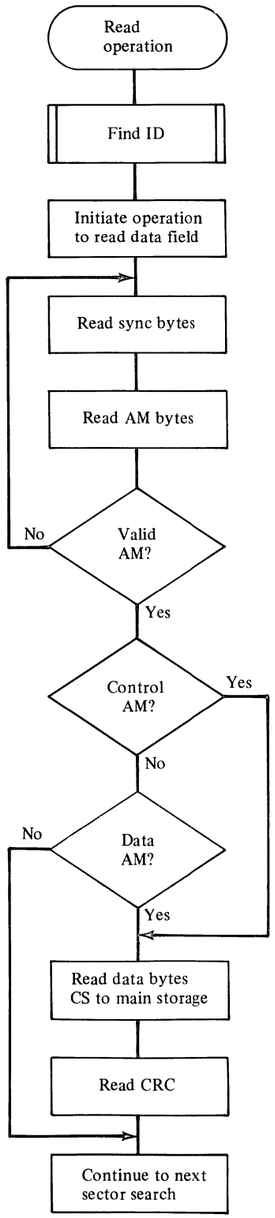
The major control in the attachment that defines the read operation is the AM search controls. These are on twice to read one sector, once to find and read the ID field, and once to find and read the data field. In both cases the controls remain on until the CRC bytes are read.

The read clock and read bit ring synchronize the attachment to the data being read. The read clock runs continuously except in diagnostic step mode. The read bit ring runs from the time an AM byte is found until after the CRC bytes have been read.

The sync byte found turns on when the first data bit of the AM is read, and remains on until the attachment has determined the byte being read is not a valid AM.

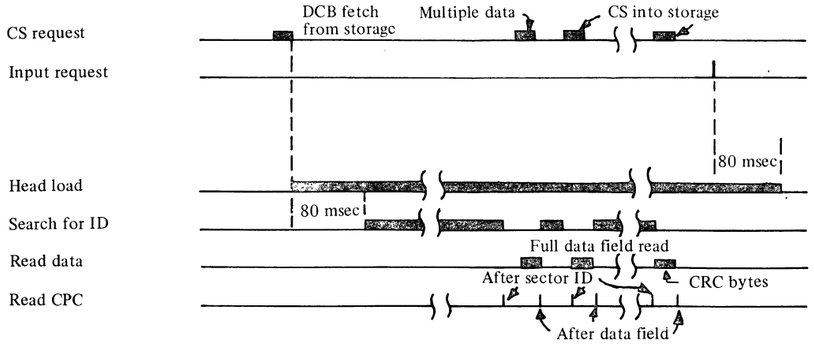
Reading a Sector

The following flow chart shows the reading of one sector from the diskette.



Timing

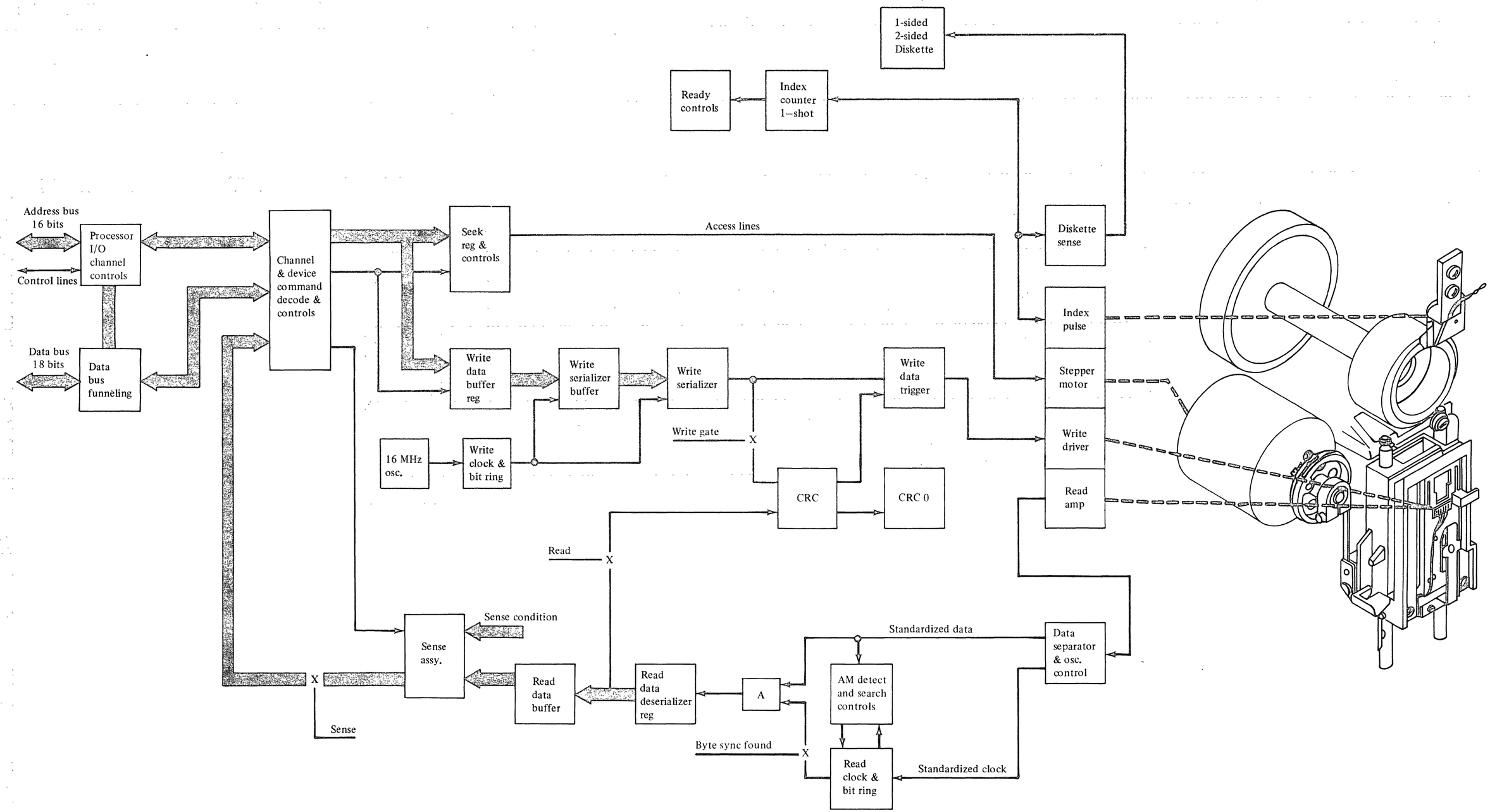
The following timing chart shows the relationship of the line sequencing during a read operation.



Notes.

1. Timing chart is the same for ID, data, or control AM.
2. On fractional sector, entire field is written with data then padded with zeros to end.
3. On presentation of interrupt, heads remain loaded for 80 msec.
4. If command is issued with heads already loaded, the 80 msec time out is not performed.

Read Data Flow



Write Data

Write data transfers a data record from contiguous even processor storage locations to one or more sectors on the diskette. Data is transferred in cycle steal mode to the sector location specified in the DCB. An interrupt request is sent when the operation is complete.

After the writing of data has started, the programs must supply data fast enough so that a word may be written every 48 us. Failure to provide data fast enough results in an overrun. Write gate remains active from the time the first sync byte is written until after the last CRC byte is written. The write clock and write bit ring run as long as write gate is active.

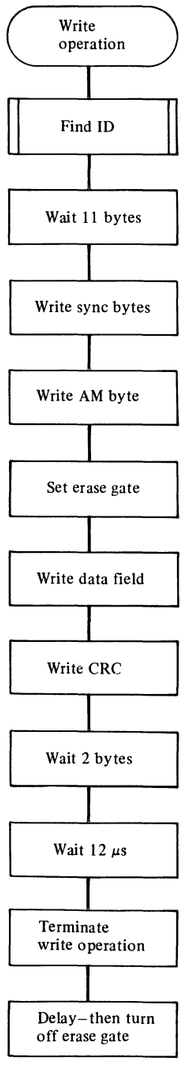
Read Verify

A read verify should be used after each write data to validate the previously written data. A read verify operation is similar to the read data in that each sector is read completely and the CRC bytes are checked to verify the operation. However, nothing is transferred to processor storage. When the verify operation is complete an interrupt is presented to the processor.

Verification of the write operation is accomplished by reading the record that was written and comparing it to the original data.

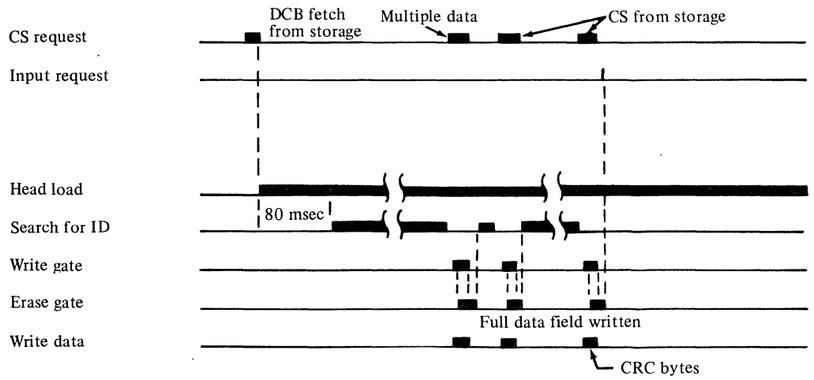
Writing a Sector

The accompanying flow chart describes the writing of one sector on the diskette. The structure of the fields written are controlled by the attachment. The attachment also controls the required delays. The data flow for the write operation is shown on the next page.



Timing

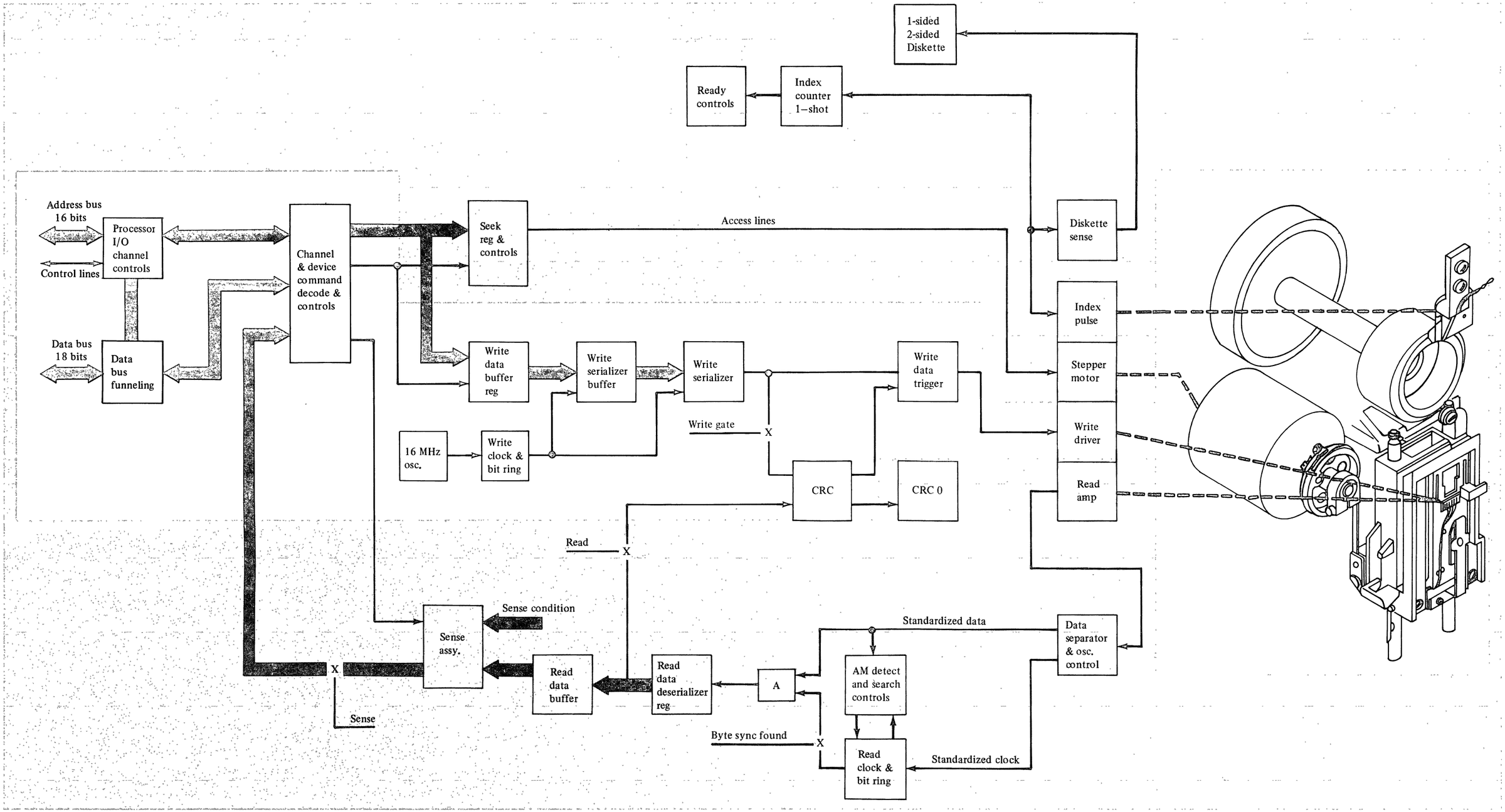
The following timing chart shows the relationship of the line sequencing during a write operation.



Notes.

1. Timing would be the same for read verify, except no CS after DCB fetch.
2. On fractional sector, entire data field is read but only first portion put in storage.
3. On presentation of interrupt, heads are loaded another 80 msec.
4. If command is issued with heads already loaded, the 80 msec time out is not performed.
5. CRC is appended as the last 2 bytes recorded as write data.

Write Data Flow



Write Gate

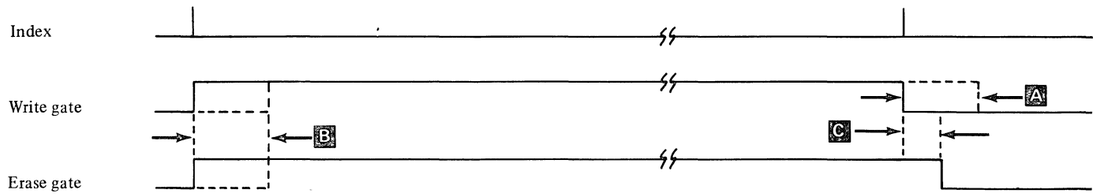
'Write gate' is active only while actually writing data. It is not active during head load, access, head selection, or idling operations. When active, it conditions the 'write select' and 'write current' lines.

The two write operations considered are:

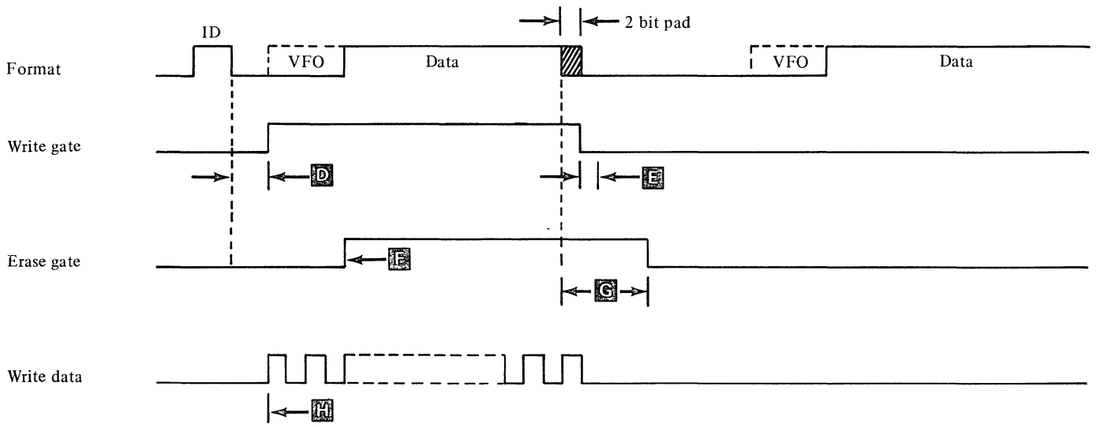
- Format write (replace all the gaps).
- Record write (or update write which acts upon individual data fields).

Format Write Operation. The format write operation is a full track write which replaces all the gaps, identifier fields (IDs), and data records on a track. The index to first ID field gap contains 73 8-bit bytes. 'Write gate' is raised at a point not greater than 50 bytes from the leading edge of the index pulse B and remains up for the entire revolution. It is dropped within 51 bytes after the leading edge of the next index pulse A.

Record (Update) Write Operation.
Update operations are performed on a data field and its VFO sync field only. IDs and gaps are not rewritten. 'Write gate' is raised 352 usec (11 bytes) from the end of the last character (or checking character, if used) of the ID field D. It is dropped E within 5 us maximum on all tracks after writing the last clock of the minimum 2-byte pad required at the end of the last character (or checking character).



Format write operation



Record (update) write organization

Erase Gate

When active, 'erase gate' conditions the tunnel erase circuits. 'Erase gate' is not active during read, head load, access, head selection, or idling operations.

The two operations requiring 'erase gate' are:

- Format write (replaces all the gaps).
- Record write (or update write which acts upon individual data fields).

Format Write Operations. 'Erase gate' is raised at the same time as 'write gate' B. This actual turn off of 'erase gate' occurs 537 us after the fall of 'write gate' C.

Record (Update) Write Operations. 'Erase gate' turn on F occurs 537 us after the rise of 'write gate.' 'Erase gate' turn off G occurs 537 us after the fall of 'Write gate.'

Note. The writing of the VFO sync H begins at the rise of 'write gate' unless compensated for by larger gaps.

Data Protection and Error Conditions

The diskette provides data protection logic to prevent the accidental destruction of data on a diskette. During accessing or reading, the 4964 attachment card prevents the write or erase lines from coming up. During a write operation, the 4964 senses the erase lines to make sure they are working properly.

The diskette unit detects errors during accessing, reading, and writing/erasing. When an error is detected, the diskette unit signals the attachment card to retry operation.

Error Conditions that may affect data protection are listed below. They are posted in cycle steal status word 1.

No Data Field Found

A no data field found is set by a read data or read verify command. It indicates that the correct sector ID was found, but no data field could be found. A noisy cable, a poorly written record or a defective diskette surface can cause a no data field found.

Read/Write Overrun

A read overrun occurs when another word of data is ready to be set into the read data buffer and the channel has not taken the previous byte soon enough. A write overrun occurs when the attachment is ready to write another byte on the diskette and the channel has not sent another byte soon enough.

File Not Ready

This indicates that the diskette unit is not ready to execute, or to continue executing a file directed command. Its presence means that a diskette is not inserted, is inserted backwards, or is not rotating because the file door is open or the drive belt is not engaging the file hub.

. A not ready condition also occurs when the diskette is turning too slowly and index pulses occur farther apart then every 167 ms.

No Record Found

A no record found error occurs when the desired record has not been found by the time two index pulses have been sensed.

If this occurs after a read sector ID it means that the sector ID could not be located on the track. An unformatted track is to be suspected. A no record found error after a read, verify, or write data command might indicate a defective track, a poorly written track, or an invalid search argument.

Write Gate Stuck Off and Erase Current Stuck On or Off

These checks occur if write gate is not active when it should be. They also detect if erase current is on or off when it should not be.

These checks occur if write gate or erase current is not active during a write operation. The circuits also detect if write current is active when a write operation is not in progress.

Due to the erase head being offset from the write head, erase gate and write gate are not turned on at the same time.

Index at Incorrect Time

A file speed error occurs when the diskette is turning too fast and index pulses occur more often than every 167 ms.

File Data Check

During a write operation the attachment feature card generates two cyclic redundancy check (CRC) bytes. These bytes are recorded as the last two characters of the sector ID field. These CRC bytes are compared with CRC bytes generated during a real operation. If the CRC bytes do not match, an error is detected and the operation is retried. When this happens after a read sector ID, the sector ID which was put into main storage may be invalid and the command should be repeated. If the error remains, an unformatted diskette or a defective track may exist.

Control AM

This indicates that a control AM was detected in front of the last data field during a read data operation. The read data operation will terminate at the completion of the sector in which the control AM was detected.

End of Track

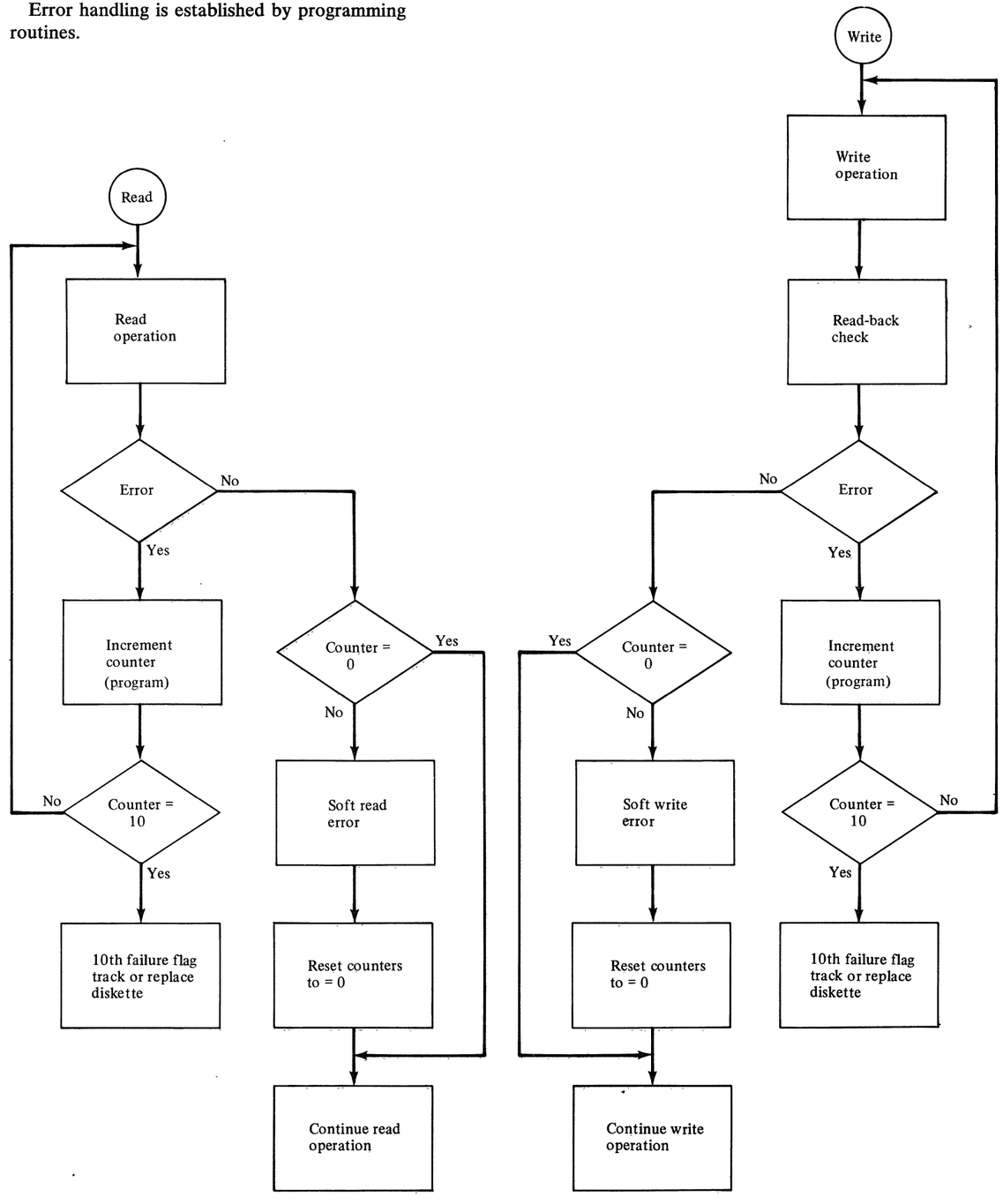
During a multiple sector operation (read, write, or verify) the last sector on the track has been accessed, and at least one more sector is required.

Invalid Diskette Side Selected

This indicates that diskette 1 is being used, and side one is selected.

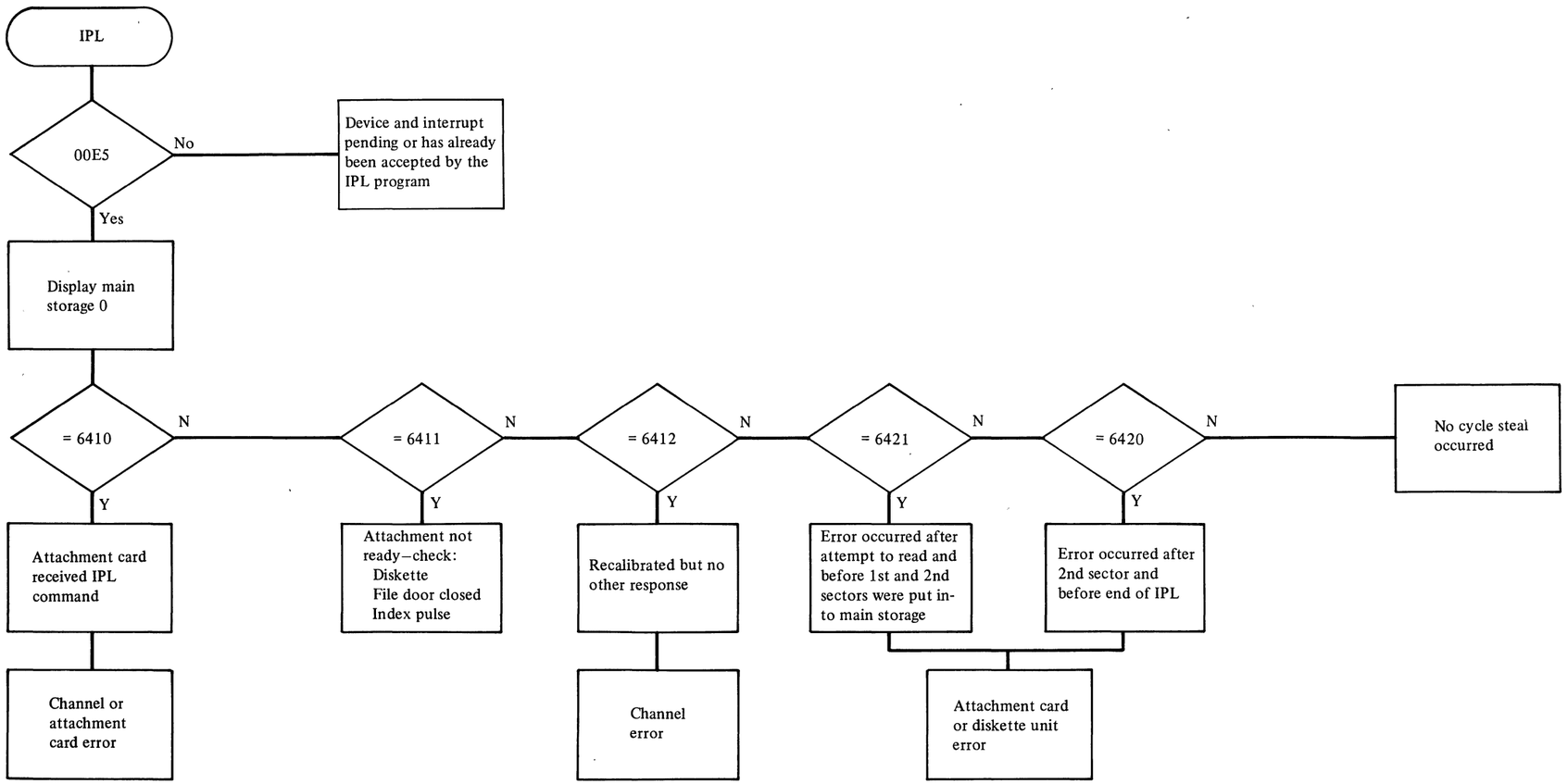
Note. For more information on error conditions see start cycle steal status and cycle steal status word one in Chapter 4.

Error handling is established by programming routines.



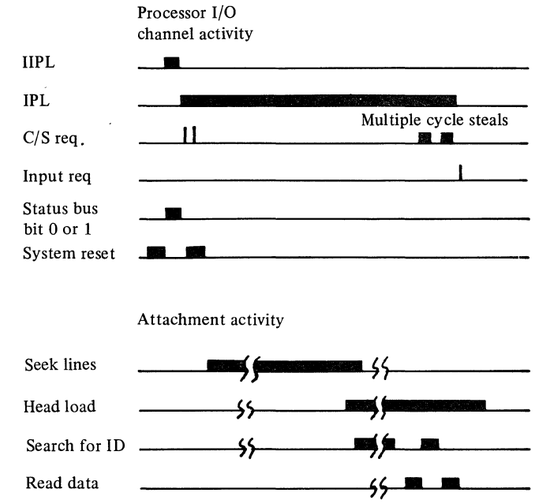
IPL

Initial Program Load (IPL) is a hardware initiated operation only. An IPL operation addressed to the attachment is normally used to load 256 bytes from cylinder 0, head 0, sectors one and two, into main storage starting at location zero. The last two bytes should be set to zero (bytes number 255 and 256). Should bytes 255 and 256 of the IPL record be Hex 83C4, the attachment will bring into the processor the remaining 24 sectors on cylinder 0, head 0. This would be a total of 3328 bytes with bytes 255 and 256 being set to zero in storage. This option of loading 26 sectors at IPL time is used only as a tool for loading diagnostics into the processor from a 'diagnostic' diskette. Following a successful IPL sequence, the attachment will present a device end interrupt on level 0. The following flow chart shows an IPL operation.



IPL Timing

The following timing chart shows the relationship of the line sequencing for an IPL operation.



Chapter 4.
Diskette Operations

Operate I/O Instruction Summary

All commands are initiated by an IO Instruction which points to an IDCB containing the command.

0	4	5	7	8	10	11	12	15	16	31
0 1 1 0 1				R2			1 1 0 0		IDCB address	

Commands \ IDCB	Command field (0–7)	Device address field (8–15)	Immediate data field (16–31)	Condition code
Prepare This command transfers a word containing interrupt parameters.	0 1 1 0 0 0 0 0	0 X X X X X X X	Zeros | Level | I Interrupt disabled = 0 Enable interrupt = 1	0,5,7
Device reset This command resets all pending interrupts and all previously established control and status conditions. The residual address and prepare registers are not reset by this command.	0 1 1 0 1 1 1 1	0 X X X X X X X	Zeros	0,7
Read device ID This command caused the diskette unit to load its device ID word into the immediate data field after execution.	0 0 1 0 0 0 0 0	0 X X X X X X X	Zeros (after execution X'0106')	0,1,2,5,7
Start This command initiates I/O operations to the diskette unit that 1) control the file or transfer data to or from storage in cycle steal mode, and 2) send an interrupt request to the processor when the operation is complete. The immediate data field must contain the DCB address.	0 1 1 1 0 0 0 0	X X X X X X X X	DCB address	0,1,2,5,7
Start diagnostic This command is used to check out the attachment and cycle steal the results into processor storage.	0 1 1 1 1 1 0 1	X X X X X X X X	DCB address Use diagnostic DCB	0,1,2,5,7
Start cycle steal status This command causes the attachment to transfer four words of status information into processor storage beginning at the address specified in the DCB.	0 1 1 1 1 1 1 1	X X X X X X X X	DCB address Use start cycle steal status DCB	0,1,2,5,7

Operate I/O Instruction Execution Time

CC Value	Meaning
0	Device not attached
1	Busy
2	Not reported
3	Command reject
4	Not reported
5	Interface data check
6	Not reported
7	Satisfactory

Interrupt Presentation Time

CC Value	Meaning
0	Not reported
1	Not reported
2	Exception — More information in ISB
3	Device end (satisfactory)
4	Attention
5	Not reported
6	Not reported
7	Not reported

Interrupt Status Byte

Bit Position	Meaning
0	Device status available — More information is CSS word 1
1	Not reported
2	Not reported
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protected check
7	Interface data check

Issue a Start Cycle Steal Status Command

Cycle Steal Status Word 1

Bit Position	Meaning
00	Not used
01	No data field found
02	Overrun
03	Control AM
04	File not ready
05	No record found
06	End of track
07	File data check
08	Incorrect index time
09	Invalid diskette surface
10	Not used
11	Not used
12	Not used
13	Erase current stuck off
14	Write gate stuck off
15	Erase current stuck on

DCB address	Start DCB (0–15)	Word
(hexadecimal)	Control word	0
(+2)	Seek control word	1
(+4)	Format data word	2
(+6)	Sector length | Cylinder	3
(+8)	Head selection | Sector number	4
(+A)	Chain address	5
(+C)	Byte count	6
(+E)	Data address	7

Operations	Mod bits
Format track	02
Write data/data AM	01
Write data/control AM	03
Read data	09
Read verify	0C
Read sector ID	0A
Seek	05
Recalibrate	07

Address	Diagnostic DCB	Word
(hexa-decimal)	0 0 1 0 0 X X X X X X X X X X X	0
(+2)	Not used	1
(+4)	Not used	2
(+6)	Not used	3
(+8)	Not used	4
(+A)	Not used	5
(+C)	Byte count (start CS = 0004 or 0008; start diag = 000E)	6
(+E)	Data address (even)	7

Status information summary

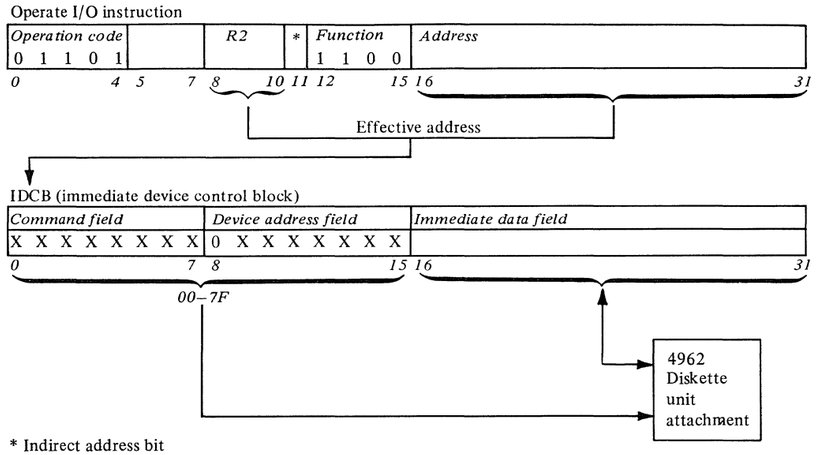
I/O Data Transfer

Diskette operations are initiated by an operate I/O ("IO" mnemonic) instructions issued by the processor program. Data is transferred on the processor I/O channel, between the processor and the attachment, in a parallel operation (16 bits plus 2 parity bits). The number of data words transferred and the direction in which they move on the channel is determined by the I/O command. The command also determines whether data is transferred to or from main storage, under direct program control (DPC) or in cycle steal mode.

Operate I/O Instruction

All I/O operations between the processor and the diskette are initiated by an IO instruction. An address field (bits 16–31) and the R2 field (bits 8–10) in the IO instruction point to a processor storage location containing an immediate device control block (IDCB).

For a more detailed description, refer to the *IBM Series/1 Model 5 4955 Processor and Processor Features Description*, GA34-0021 or the *IBM Series/1 Model 3 4953 Processor and Processor Features Description*, GA34-0022.



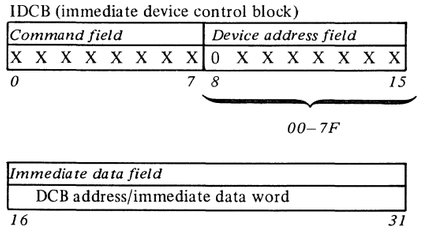
* Indirect address bit

Immediate Device Control Block

The storage location specified by the IO instruction contains the Immediate Device Control Block (IDCB). An IDCB is required for every command issued to the diskette unit and is always located on a word boundary.

The IDCB is a two-word block of storage that contains the device directed commands. Before issuing the IO instruction for an operation, the command field of the IDCB (bits 0–7) must be set, along with a device address (bits 8–15), and any field of immediate data required by the command in the IDCB (bits 16–31). The information specified in the immediate field depends on the command to be performed. The device address of the diskette is limited to 128 (0–127) possible device combinations. Bit 8 of the device address field in the IDCB must be zero.

The immediate data field of the IDCB should contain either a data word or a device control block (DCB) address. Commands that execute under DPC require a data word, while commands that execute in cycle steal mode require a DCB address.



Direct Program Control

When the diskette unit executes a prepare, device reset, or read ID command, a word of data is moved to or from the immediate data field of the IDCB in main storage using DPC. After execution of the command, the attachment reports a condition code that indicates whether the I/O operation succeeded or failed. Processing operations are halted while the I/O operation is in progress.

Note. The following commands do not cause interrupts.

Command	*IDCB Immediate Data Field*
Prepare	Interruption parameters
Device reset	Zeros
Read device ID	Device ID

Cycle Steal

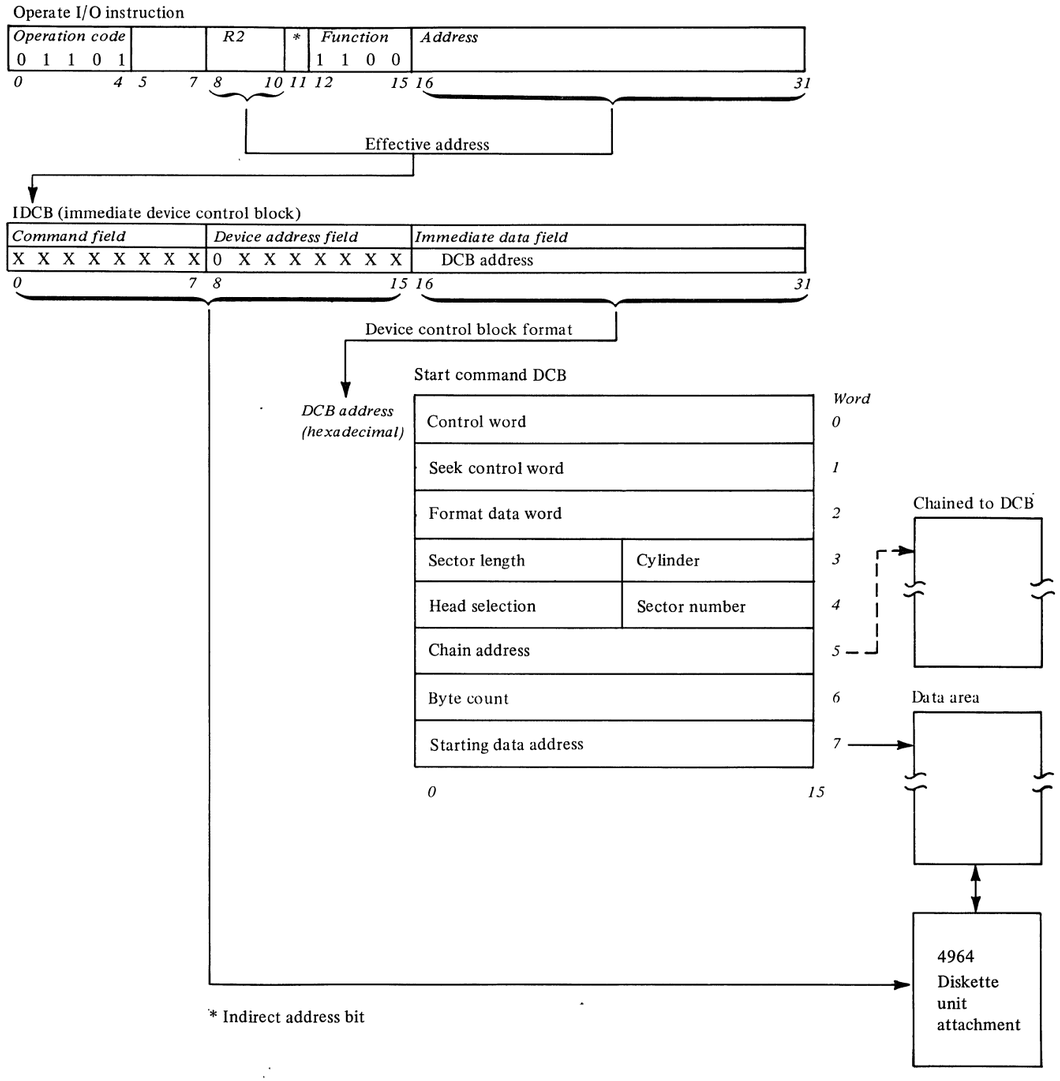
After the diskette attachment accepts a start or start cycle steal status command, a DCB is transferred from main storage to the attachment, and the processor can continue with other processing operations. Additional data transfers performed by the accepted command are made to or from main storage by stealing storage cycles from the processor. The processor and diskette operations are then overlapped. Overlapping allows the processor to continue with other processing operations while the diskette is executing an I/O operation.

Device Control Block

A device control block (DCB), comprised of eight contiguous words in main storage, must be reserved for every I/O operation that moves data in cycle steal mode. A separate DCB is required for:

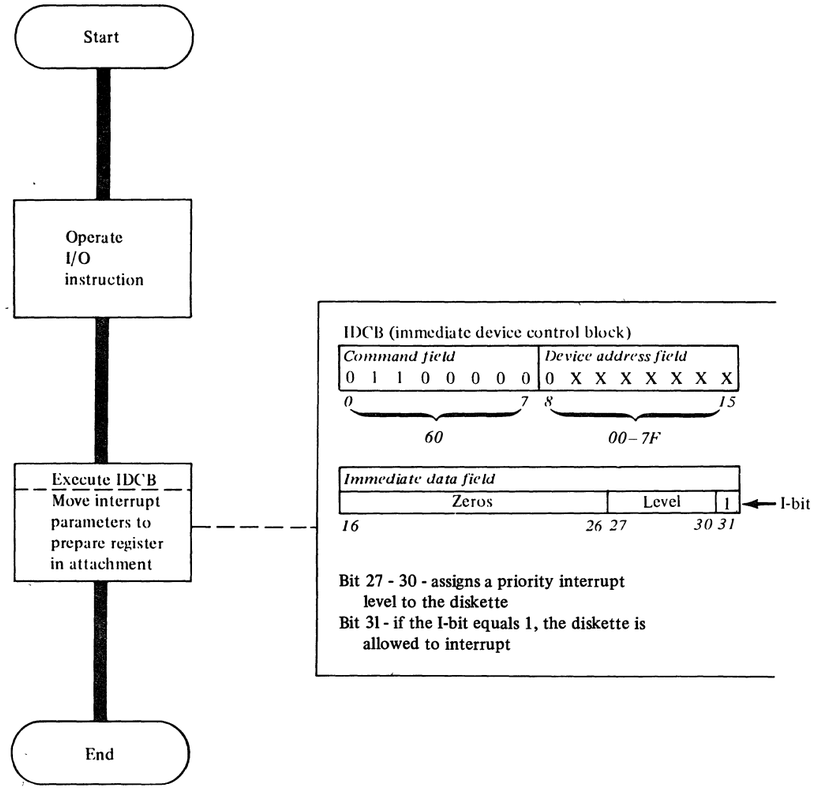
- A start command
- A start cycle steal status command
- All diskette operations included in a DCB command chaining sequence

Device parameters that define and control the I/O operation must be stored in each DCB. The bit significance of each DCB word is covered later in this chapter.



Commands

Prepare

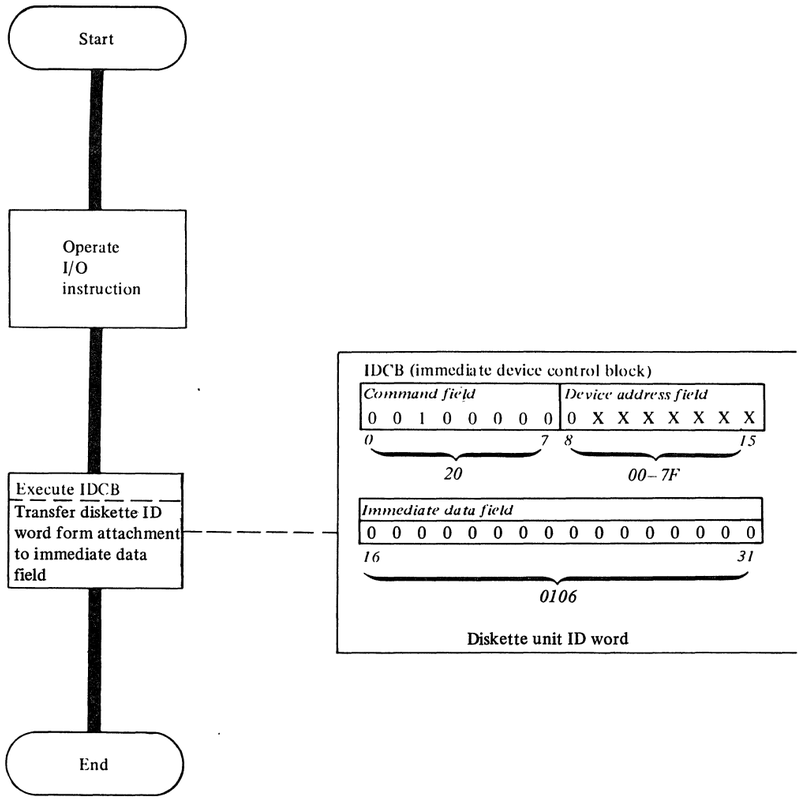


Prepare

Before the diskette unit, via the attachment, can execute interruptable commands, it needs interrupt parameters which control these commands. These parameters are stored in the IDCB immediate data field associated with a prepare command and contain the level on which the attachment is to interrupt (bits 27–30), and an interrupt enable (bit 31).

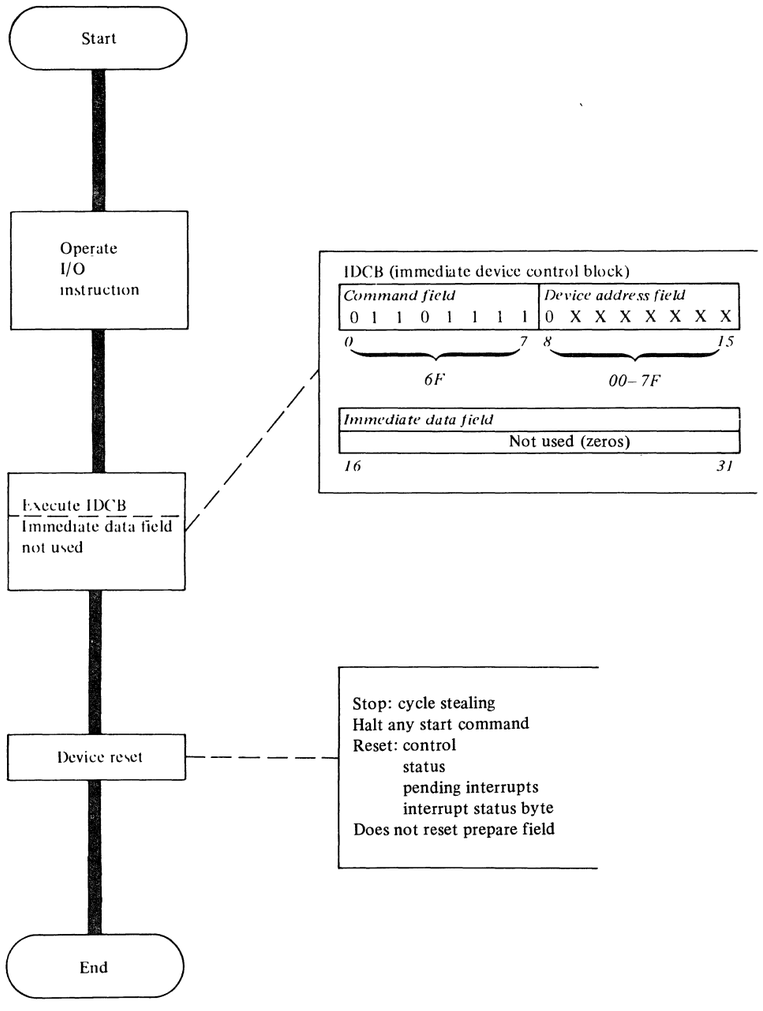
The prepare command operates under DPC and does not cause an interrupt.

Read Device ID



Read Device ID

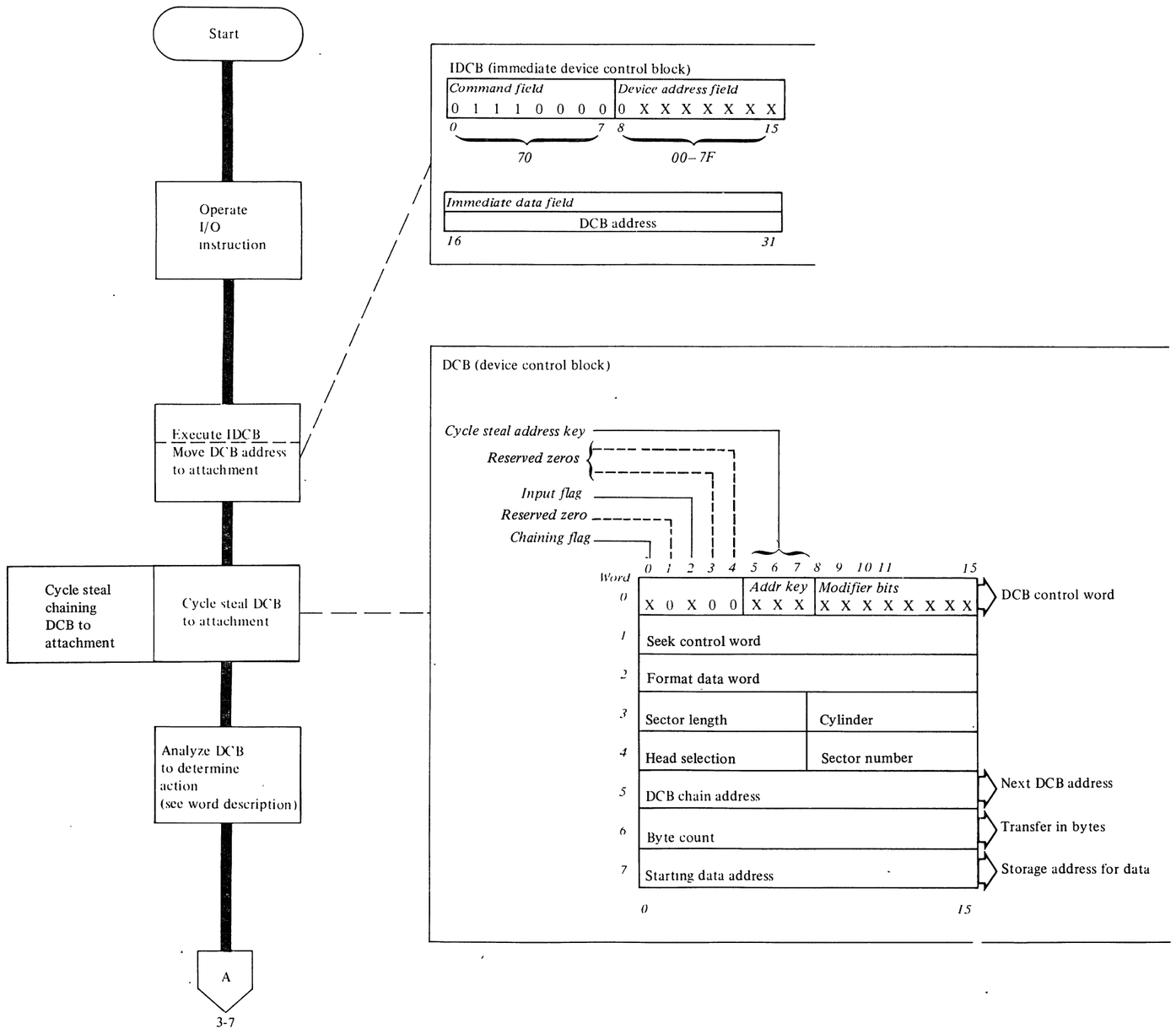
The read device ID command operates under DPC and transfers the device ID word for the diskette unit into the immediate data field of the IDCB associated with that command. If the diskette unit is busy or if an interrupt is pending, condition code 1 is returned.



Device Reset

The device reset command performs the functions shown in the illustration. This command does not use or check the immediate data field of the IDCB. The command code and device address supply all needed information.

Start



Start

Start commands initiate I/O operations that transfer data to or from main storage in cycle steal mode. The attachment presents an interrupt request to the processor when the operation is completed. An IO instruction must point to an IDCB containing each start command, and the IDCB immediate data field must contain the address of a DCB. The control information and parameters required for a particular diskette operation must be stored in the DCB associated with each start command. The diskette operations initiated with a start command are:

- Format track
- Write data/data AM
- Write data/control AM
- Read data
- Read verify
- Read sector ID
- Seek
- Seek recalibrate

When the IO instruction is issued, the start command is transferred under DPC from the IDCB to the attachment where it is checked for errors and validity. If the attachment accepts the command, a 'satisfactory' condition code (CC=7) is sent to the processor. The attachment enters the 'busy' state until the diskette operation is completed and the processor continues with other operations. Beginning at the DCB address specified in the IDCB, the eight words in the DCB are transferred from main storage to the attachment. The data is transferred in cycle steal mode one word at a time. The attachment decodes the DCB information and begins executing the diskette operation called for in the DCB control word (DCB word 0). When the operation is completed, the attachment presents an interrupt request to the processor. At interrupt presentation time, the attachment transfers a condition code and interrupt ID word containing status information to the processor.

A

Device Control Block

The DCB words associated with the diskette unit's start command must have the following format:

DCB Control Word (DCB Word 0)

This word occupies the first position of each DCB associated with a start or start cycle steal status or start diagnostic command. The DCB control word delineates the diskette operation.

The meaning of the bits is as follows:

Bit 0 (Chaining Flag). Set this bit to one to specify DCB command chaining. Only start commands may be chained. After the operation called for by the current DCB is completed, the attachment uses the chain address stored in DCB word 5 to select the next DCB in the chained sequence.

Bit 1 (Reserved). Set this bit to zero to avoid future code obsolescence. The attachment does not support a program controlled interrupt.

Bit 2 (Input Flag). Set this bit to 1 for diskette operations that transfer data to main storage. Set the bit to zero for diskette operations that transfer data from main storage.

Note. If the input flag setting is not consistent with the type of operation, the attachment terminates the operation and requests an interrupt. At interrupt presentation time, an exception condition and a DCB specification check are presented to the processor.

Bit 3 (Reserved). Set this bit to zero to avoid future code obsolescence. The attachment does not support burst mode operations.

Bit 4 (Reserved). Set this bit to zero to avoid future code obsolescence. The attachment does not support suppress incorrect length.

Bits 5–7 (Address Key). These bits represent the cycle steal address key the attachment must present for storage authorization at cycle steal request time.

Bits 8–15. The bits in this field are device dependent operation modifiers of the start command. Select a bit configuration that represents the diskette operation to be performed. The selected operation must be compatible with the setting of the input flag bit (bit 2). The hexadecimal designation for each diskette operation and the corresponding setting of bit 2 are shown as follows:

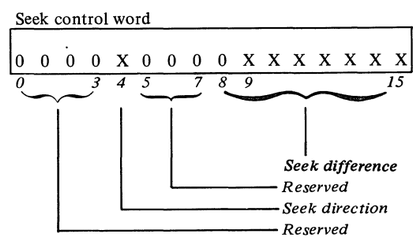
Bit 2	*Bits 8 9 10 11 12 13 14 15*	*Operation*	*DCB words used*
0	0 0 0 0 0 0 1 0	Format track	2, 3, 4, 5
0	0 0 0 0 0 0 0 1	Write data/data AM	3, 4, 5, 6, 7
0	0 0 0 0 0 0 1 1	Write data/control AM	3, 4, 5, 6, 7
1	0 0 0 0 1 0 0 1	Read data	3, 4, 5, 6, 7
0	0 0 0 0 1 1 0 0	Read verify	3, 4, 5, 6, 7
1	0 0 0 0 1 0 1 0	Read sector ID	5, 6, 7
0	0 0 0 0 0 1 0 1	Seek	1, 4, 5
0	0 0 0 0 0 1 1 1	Seek recalibrate	1, 5

Seek Control Word (DCB Word 1)

The seek control word is used in conjunction with the head address specified in the high-order byte of DCB word 4 to control seek operations. The seek control word specifies the direction of the seek—either toward the outer perimeter of the diskette or toward its center—and the number of cylinders to be crossed.

Notes:

1. The seek control word is used only for seek operations.
2. If the seek control word is set to zero for a seek operation, no seek movement occurs.
3. For all seek operations, set DCB words 3 and 6 to zeros. The search argument and byte count are not used in seek operations.



The meaning of the seek direction and seek difference fields are as follows:

Bit 4 (Seek Direction). Set this bit to zero to increase the cylinder number (seek toward the center of the diskette). Set this bit to one to seek to a lower cylinder number (toward the outer edge of the diskette).

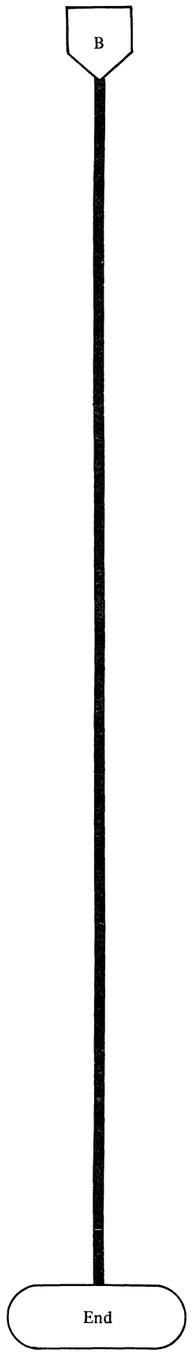
Bits 8–15 (Seek Difference). These eight bits specify the seek difference (the number of cylinders to be moved). If a seek difference of zero is specified, no movement occurs and the attachment reports a device end condition at interrupt presentation time.

Bits 0–3 and 5–6 in the seek control word are reserved; set them to zeros to avoid future code obsolescence.

Format Data Word (DCB Word 2)

The format data word contains the word of data to be written in every word of every sector on a track during a format track operation. The sector length and cylinder bytes in DCB word 3 must contain valid values. If the sector length byte contains binary 1111 0000, the entire track is formatted into 128-byte defective sectors. Set bits 4–7 to zeros to avoid future code obsolescence. See "Format Track" later in this chapter for more information.

B



Sector Length and Cylinder (DCB Word 3)

DCB word 3 consists of two one-byte fields: the sector length and cylinder.

Sector Length

The sector length field specifies the length of the sectors on the diskette. The field must contain one of the following binary values:

- 0000 0000 for 128-byte sectors
- 0001 0000 for 256-byte sectors
- 0010 0000 for 512-byte sectors
- 1111 0000 format track defective

The sector length field corresponds to the N-byte in the sector ID on the diskette. It is part of the search argument used by the diskette attachment to locate the required sector.

Cylinder

The cylinder field contains a right-adjusted binary number from 00 through 76 that indicates the number of the cylinder containing the desired sector. If the number specified does not fall within the acceptable range (00 through 76), the diskette attachment ends the operation immediately with an exception condition code and a DCB specification check set in the ISB at interrupt presentation time.

The cylinder byte corresponds to the C-byte in the sector ID on the diskette. It is used as part of the search argument to locate the required sector. On Format Track operations, the cylinder specified in this byte is written as part of the track sector IDs.

Head Selection and Sector Number (DCB Word 4)

DCB word 4 consists of two one-byte fields: head selection and sector number.

Head Selection

The head selection byte specifies which head is to be used to access the data. Specify 0000 0000 for head 0; specify 0000 0001 for head 1. Set bits 0–6 to zeros to avoid future code obsolescence. Specifying any other value will cause the diskette attachment to respond 'no record found' to all operations except Read Sector ID.

The head selection byte corresponds to the H-byte in the sector ID on the diskette. It is part of the search argument used by the attachment to locate the required sector.

The head selection byte is used during a seek operation to specify the head to be used for all succeeding data transfer operations; the head selected can be changed only by performing another seek. Seek Recalibrate operations automatically select head 0 but are not normally used to change head selection.

Sector Number

The sector number byte contains the number of the specific sector to be accessed. The range of valid values depends on the *sector length* specified in the first byte of DCB word 3. The valid values for sector length and sector numbers are:

Contents of sector length field (binary)	*Sector length*	*Possible values for sector number field (binary)*	*Decimal equivalent*
0000 0000	128 bytes	0000 0001 0001 1010	01 26
0001 0000	256 bytes	0000 0001 0000 1111	01 15
0010 0000	512 bytes	0000 0001 0000 1000	01 08

If the value stored in the sector number byte of DCB word 4 exceeds the acceptable range for the sector length indicated in the sector length field of DCB word 3, the diskette attachment ends the operation immediately with an exception condition code and a DCB specification check indicated at interrupt presentation time.

The sector number corresponds to the R-byte in the sector ID on the diskette. It is part of the search argument used by the diskette attachment to locate the required sector.

Chain Address (DCB Word 5)

To chain diskette operations, set the chaining flag bit in the DCB control word (DCB word 0) to one. The address of the next DCB in the chain must be specified in the chain address field. The address must be an even number. If the chained-to address is an odd number (bit 15 is on), no data is transferred, and a DCB specification check is set in the interrupt status byte and transferred to the processor at interrupt presentation time.

Byte Count (DCB Word 6)

The byte count specifies the number of bytes to be transferred between main storage and the diskette attachment. The byte count must be an even number for all data transfer operations. If bit 15 is set on (indicating an odd byte count), the attachment ends the operation immediately, without transferring the data, and requests an interrupt. It presents an exception condition (CC=2) with a DCB specification check in the ISB at interrupt presentation time.

The start cycle steal status command requires a byte count of either X'0004' or X'0008'; the Read Sector ID operation requires a byte count of X'0004.' Other data transfer operations (write data/data AM, write data/control AM, read data, or read verify) require a byte count that indicates the length of the record to be transferred. The diskette attachment uses the byte count in conjunction with the sector length (N-byte in DCB word 3) to determine the number of sectors required for the record. For example, if a 134-byte record is to be written, the byte count field must contain X'0086.' If the diskette is formatted into 128-byte sectors, the N-byte would be zero. The diskette unit would write 128 bytes of the record into the sector identified in the sector ID search argument; the last 6 bytes would be written in the next logical sector, and the remainder of the sector would be padded with binary zeros. When the record is subsequently read, the padded zeros are included in the data field CRC verification. However, only the number of data bytes specified in the DCB byte count are transferred into main storage.

Data Address (DCB Word 7)

This field contains the beginning address of the main storage location used in the data transfer. During a read operation, the first word read from the diskette is stored in this location; data is then transferred into succeeding main storage locations until the byte count has been fulfilled. During a write operation, the word stored at this location is written to the first word in the sector specified; words are then written in succeeding locations on the diskette until the byte count has been fulfilled.

The data address stored in this word must identify a storage location that is on an even address boundary. If the data address is odd (bit 15 is set to one), the attachment ends the operation and requests an interrupt. At interrupt presentation time, a DCB specification check is transferred to the processor.

DCB Command Chaining

DCB command chaining is obtaining a new DCB upon completion of the operation specified in the current DCB without issuing a new IO instruction. The DCBs belonging to such a sequence are said to be chained. DCB command chaining reduces the processing time required to execute I/O operations to the diskette unit.

When DCBs are chained, the first DCB in the chain contains the address of the next DCB. As each operation in a chained sequence is completed, the chain address stored in the current DCB is used to cycle steal the next DCB in the chain. The chained-to DCB is examined to determine which operation is next in the sequence and whether the associated device parameters are valid. DCB command chaining operations continue until a DCB is fetched that has the chaining bit in the control word (DCB word 0) set to 0, indicating the last operation in the chain. If an error occurs, chaining to succeeding DCBs is automatically suspended, and an interrupt request is sent to the processor. Normally, an interrupt is not requested until the diskette unit has completed the last operation in the chain.

For example, a single IO instruction can:

- Seek to a new cylinder location and change head selection
- Write a record
- Verify that the record was written properly
- Seek to a new cylinder location and change head selection
- Read a record, etc.

Seek

A seek must precede every I/O operation to the diskette unit that requires a move of the heads to another cylinder or a change in head selection. The seek operation may be used to change:

- Head selection
- Cylinder location
- Head selection and cylinder location

During a seek operation, DCB data is transferred in cycle steal mode. The attachment presents an interrupt request to the processor when the diskette unit completes the operation. When the processor services the interrupt request, the attachment transfers a condition code (CC) and an interrupt ID word to the processor.

The control information and parameters required for a seek operation must be stored in a DCB. The DCB must contain:

- A DCB control word defining a seek operation to the diskette unit (DCB word 0)
- A seek control word specifying the seek direction and number of cylinders to be crossed (DCB word 1)
- A head select byte specifying which head is to be used (high-order byte of DCB word 4)
- A chain address if DCB command chaining is specified in the DCB control word
- All unused DCB fields should be set to zero

Seek Recalibrate

The seek recalibrate operation automatically moves the access mechanism to cylinder 00 and selects head 0. Because a seek recalibrate operation requires 0.41 seconds to execute, it should only be used in error recovery or initialization routines. This operation can be used during initialization to return the heads to cylinder 00 from an indeterminate location. During a seek recalibrate operation, no data is transferred. The attachment presents an interrupt request to the processor when the diskette unit completes the operation. When the processor services the interrupt request, the attachment transfers a condition code (CC) and an interrupt ID word to the processor.

The control information and parameters required for a seek recalibrate operation must be stored in a DCB. The DCB must contain:

- A DCB control word that defines a seek recalibrate operation to the diskette unit (DCB word 0)
- A chain address in DCB word 5 if DCB command chaining is specified in the DCB control word for this operation

Although the data in the DCB seek control word is not needed for this operation, it is checked for proper parity. All unused DCB fields must be set to zero.

Read Sector ID Operation

The Read Sector ID operation should normally be used to determine which head is selected and on which track the head is located. After determining from the DCB control word (DCB word 0) that a Read Sector ID operation is called for, the diskette unit immediately begins to read data from the track under the selected head. The diskette attachment loads the first sector ID detected into a search argument register. The register contents (the N,C,H, and R-bytes) are transferred via cycle steal into storage beginning at the data address specified in the DCB.

When the diskette unit successfully completes the operation, the attachment posts a device end condition code (CC=3) and requests an interrupt.

Write Data/Data AM Operation

The write data/data address mark (AM) operation transfers a data record from contiguous main storage locations to one or more sectors on the diskette. When the diskette unit performs a write data/data AM operation, data from the main storage location specified in the DCB is transferred by the attachment in cycle steal mode to the location on the diskette specified by the search argument in the DCB. The diskette unit automatically writes a data address marker (AM) preceding the data in each sector written. A data AM indicates that the sector contains data. To write a sector of control information, see "write data/control AM operation."

If the last sector being written is not a full sector, the diskette unit writes the data bytes, then fills the sector to the end with zeros. The number of data bytes written for a partially filled sector is determined from the value stored in the low-order byte of the DCB byte count (DCB word 6).

The DCB for a write data/data AM operation must contain: a DCB control word, sector ID search argument (sector length, cylinder address, head selection, sector number), byte count, and data address. Specify the chain address in DCB word 5 and set the chaining flag in DCB word 0 to one when command chaining to another DCB. All unused DCB words and fields should be set to zeros.

Write Data/Control AM Operation

The Write Data/Control AM operation is similar to the Write Data/Data AM operation. The only difference between the two operations is the address marker that is written in the byte immediately preceding each sector data field. The Write Data/Control AM operation automatically writes X'F8' in the AM2 byte, which indicates that the data field contains control information.

Read Data

The read data operation retrieves a data record stored in one or more sectors on the diskette and transfers the data into contiguous main storage locations, beginning at the data address specified in the DCB. The read data operation transfers data in cycle steal mode and sends an interrupt request to the processor when the operation is completed.

When the diskette unit performs the read data operation, the read/write head (selected with a previous seek operation) immediately begins to search the diskette for the sector ID specified by the search argument in the DCB. When the diskette unit locates the sector, the information in the data field is transferred from the diskette to the attachment buffer. After reading the sector, the attachment verifies the data by recalculating the CRC bytes for the data field. If the sector being read is not a full sector, the attachment reads the sector to the end and verifies the CRC bytes. Only those bytes required to fulfill the DCB byte count are transferred to main storage.

The DCB for a read data operation must contain a DCB control word, sector ID search argument (sector length, cylinder address, head selection, sector number), byte count, and data address. Specify the chain address in DCB word 5 and set the chaining flag in DCB word 0 to one when command chaining to another DCB. All unused DCB words and fields should be set to zero.

Read Verify

The read verify operation should be used after each write data to validate the previously-written data. The read verify operation is similar to the read data operation in that each sector specified is read completely and the CRC bytes are checked to verify the data. However, the data is not transferred to main storage. When the operation is completed, the attachment presents an interrupt request to the processor.

With the exception of the control word (DCB word 0), the fields of the DCB for read verify should be the same as those for the previous write operation. The required DCB fields are the control word, sector ID search argument (sector length, cylinder address, head selection, sector number), byte count, and data address. Specify the chain address in DCB word 5 and set the chaining flag in DCB word 0 to one when command chaining to another DCB. All unused DCB fields should be set to zero.

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Format Track Operation

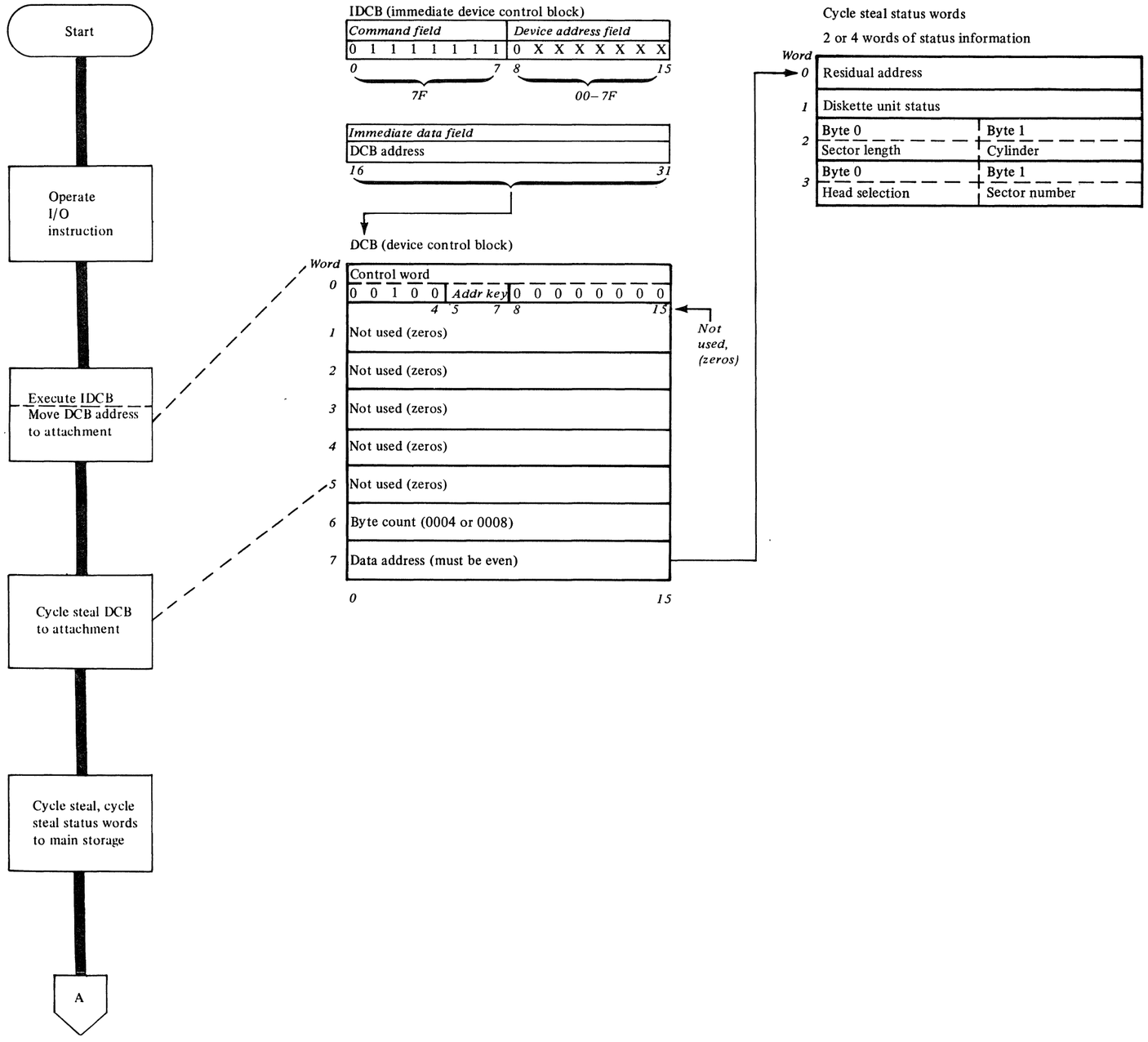
The format track operation is normally used to format a track on the diskette into twenty-six 128-byte sectors, fifteen 256-byte sectors, or eight 512-byte sectors. The format track operation can also be used to identify defective tracks by formatting the sector IDs with a unique data pattern. When 1111 0000 is specified in the N-byte of DCB word 3, the diskette attachment automatically formats the track with 128-byte sectors containing *one-bits* in every sector ID on the track.

The DCB for a format track operation must contain a DCB control word, a format data word, and a sector length and cylinder designation (DCB word 3).

Set the chaining flag in the DCB control word to one and specify a chain address in DCB word 5 when chaining to another DCB. All unused DCB words and fields should be set to zeros.

Store the data that is to be repeated for every word, on every record, on the track being formatted in the DCB format data word. The C-byte in DCB word 3 must contain the cylinder address of the track being formatted. The C-byte value is written in the sector ID of each sector formatted on the track. The C-byte value is checked for validity: it must be a binary number equal to 00 through 76 (decimal). The N-byte in DCB word 3 specifies the size of every sector being formatted on the diskette track. The N-byte must contain 0000 0000 for 128-byte sectors, 0001 0000 for 256-byte sectors, 0010 0000 for 512-byte sectors, or 1111 0000 for defective sectors. If X'F0' is specified in the N-byte, the track is formatted with 128-byte sectors containing *one-bits* in every sector ID on the track.

Start Cycle Steal Status



Start Cycle Steal Status

The start cycle steal status command causes the attachment to transfer two or four words of status information into main storage beginning at the data address location specified in the DCB. This information is available whenever the status available bit is set on in the ISB returned at interrupt presentation time. The information is used to determine why the command did not execute properly. The command operates in cycle steal mode and the attachment presents an interrupt request when execution is complete.

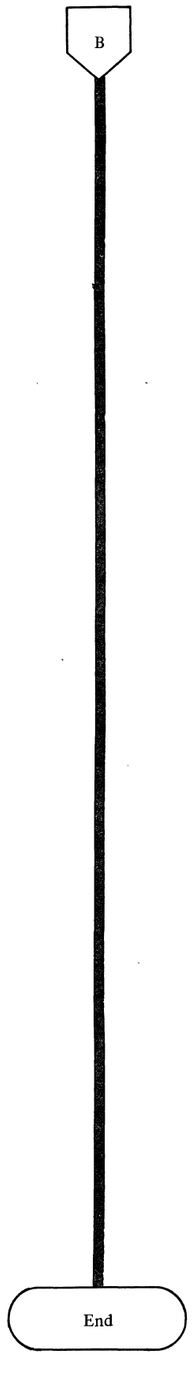
The start cycle steal status command requires an IO instruction with the address of an IDCB, an IDCB with the address of the DCB, and a DCB.

The DCB for a start cycle steal status command must contain: a DCB control word, a byte count (must be set to X'0004' or X'0008'), and a data address. The data address specifies the location in main storage into which the two or four words of status information are to be transferred. Set the chaining flag bit in DCB word 0 to zero. All unused DCB words and fields should be set to zero. For a detailed description of the DCB refer to the "Start" command section of this chapter.

The cycle steal status words transferred to main storage as a result of the start cycle steal status command contain the following information:

Cycle Steal Status Word 0

This word contains the residual address, which is the main storage location where the last cycle steal of data occurred on read operations. When write data operations terminate early because an error occurs, the attachment retains the ID of the last sector the diskette unit attempted to write. The residual address can be either the address of a word of data or the address of a word in the DCB. Execution of the start cycle steal status command does not affect this address.



Cycle Steal Status Word 1

Each bit in this word indicates a reason why the attachment could not produce a normal end-of-operation response to the previous start command. The bits have the following meanings.

Bit Position	*Meaning*
00	Not used
01	*No data field found.* This bit may be set by a Read Data or Read Verify operation. If the bit is set to one, the attachment located the correct sector ID but did not find the associated data field.
02	*Overrun.* During cycle steal transfer operations a cycle steal request by the diskette attachment must be serviced by the processor within 48 microseconds or the overrun bit is set on. This condition arises when demands for I/O activity exceed the capability of the channel.
03	*Control address marker (AM).* This bit is set to one if, during a Read Data operation, the diskette attachment detects a control AM in front of a sector data field. The attachment terminates the operation after the sector or portion thereof containing the control AM has been transferred to main storage. *Note.* The attachment does not monitor for the presence of control AMs during Read Verify Operations.
04	*File not ready.* This bit is set to one if the diskette unit is not ready to execute or drops ready while executing a Seek, Seek Recalibrate. Write Data, Read Data, Read Verify, Read Sector ID, or Format Track operation,
05	*No record found.* This bit is set to one if, after at least one rotation of the diskette, the attachment has not found a sector ID that compares 'equal' to the search argument sector ID in the DCB. If this bit is set to one after a Read Sector ID operation, it means the diskette attachment did not locate any sector IDs on the track (suspect an unformatted track).
06	*End of track.* If at least one but not all of the sectors in a multiple sector operation has been transferred and the end of the last logical sector on the track is detected, this bit is set to one.
07	*File data check.* This bit is set to one if the diskette attachment detects a data error on the diskette. The attachment uses CRC bytes, recorded at the end of every sector ID and data field, for error detection.
08	*Index pulse at incorrect time.* The diskette attachment detected an index pulse between the sector ID and the associated data field.
09	*Invalid diskette side selected.* Two types of diskettes are available for use in the diskette unit. One type is designed for data storage on only one surface (one-sided diskette), and the other type is designed for data storage on both surfaces (two-sided diskette). If a one-sided diskette is inserted in the diskette unit, head 0 must be selected for all seek operations. If head 1 is specified, the diskette attachment terminates the operation and sets the *invalid diskette side selected* bit to one.
10–12	Not used
13	*No erase current.* If this bit is set to one after a Write Data (Data AM or Control AM) or Format Track operation, the data that was written over and the data written are probably not retrievable. Retry *one time only* and then call for maintenance.
14	*No write gate.* Same as bit 13.
15	*Erase current stuck on.* If this bit is set to one after any diskette operation, *retry one time only* and then call for maintenance.

Cycle Steal Status Words 2 and 3

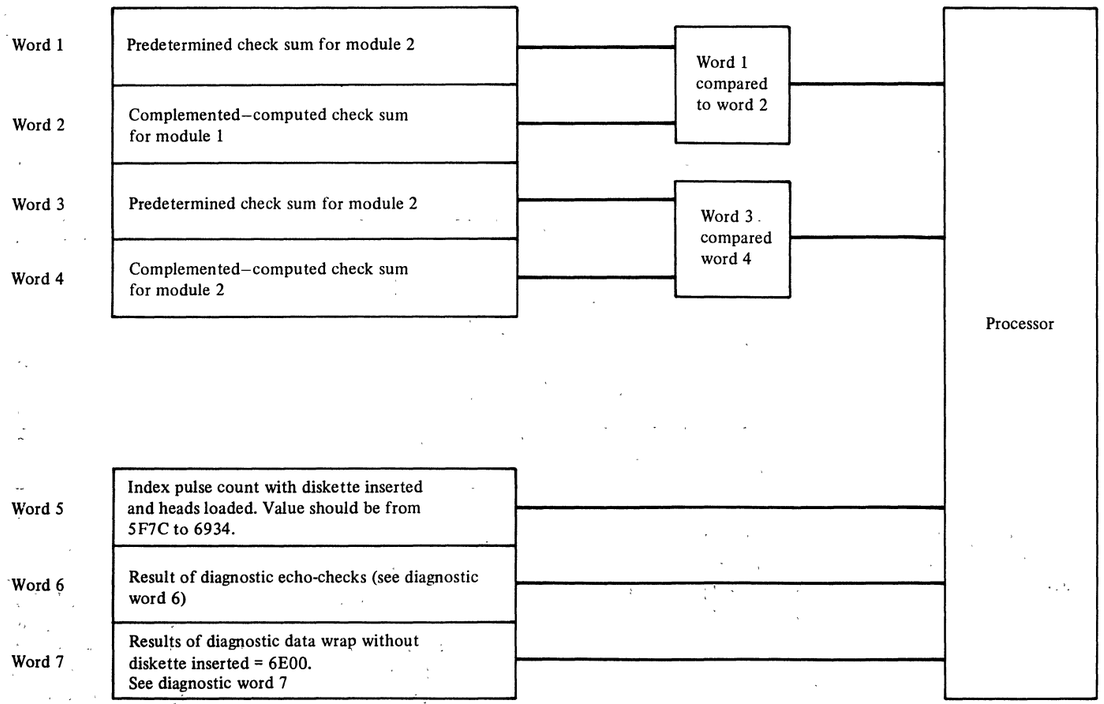
CSS words 2 and 3 contain the search argument data field access operation that resulted in the interrupt. The N, C, H, and R-fields returned in these two SCSS words point to the sector location that caused the error and ended the operation. The information is only useful if the preceding operation was a Write Data, Read Verify, or Read Data operation that failed because of a data field error. The information is especially useful if the I/O operation involved multiple sectors.

Start Diagnostic

Start diagnostic is used to check out the diskette attachment and cycle steal the results into main storage.

The first four words are put into storage for validating the diskette, read only storage, and local storage.

The next three words contain the result of diagnostic sequences executed by the diskette attachment.



Note. If no comparison is made the attachment will return a busy after reset to the next IO.

Diagnostic Word 6 Bit Significance

Bit significance in word 6 is structured such that if at least one of bits 8–15 is active a diagnostic error occurred requiring CE intervention. When bit 8 is active, bits 0–7 contain the value on which the SER-DES buffer error occurred (see following table). If bit 8 is not active the data returned in bits 0–7 is unspecified.

Bit Significance	*Meaning*
00–07	Contents of SER-DES buffer after error
08	SER-DES buffer error
09	Not used
10	Write gate latch stuck on
11	Erase gate latch stuck on
12	Inner bands latch miscompare
13	Access line miscompare
14	Write gate latch stuck off
15	Erase gate latch stuck off

Diagnostic Word 7

Word 7 contains the results of a diagnostics wrap test through the attachment card, cable, and data separator card. A value of 6E00 means the test is successful. For any other value, see the MAPs.

Status Information

Three types of status information are posted by the attachment to inform the processor of the results of input/output operations:

- Condition codes
- Interrupt status information
- Cycle steal status information

Condition Codes

Condition codes are posted after execution of each IO instruction. In case of commands that do not cause interrupts, the condition code posted after the instruction is executed is the only status information available or required. The attachment sets the appropriate condition code in the even, carry, and overflow bit positions of the *level status register* (LSR) in the processor. (Refer to "Prerequisite Publications" in the Preface of this manual for order numbers of IBM Series/1 processor unit description manuals.)

Note. The attachment posts a command reject (CC=3) if an invalid modifier value is stored in the modifier bits of the DCB control word and condition code values zero or one are not being reported.

For commands that cause interrupts, a condition code is also posted at interrupt presentation time. The CC values that can be reported at interrupt presentation time are:

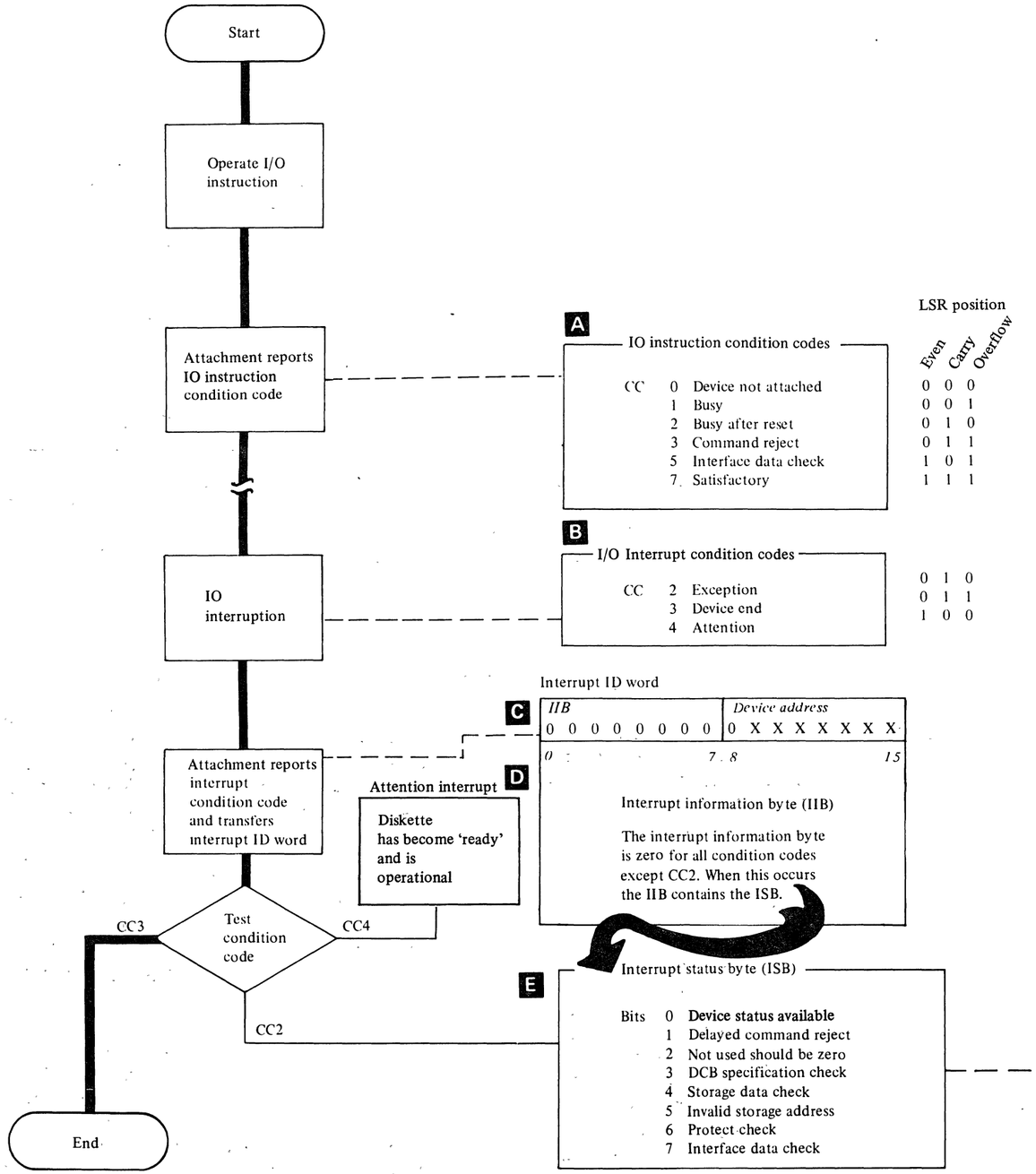
CC Value	*Meaning*
0	Not reported
1	Not reported
2	Exception
3	Device end (satisfactory)
4	Attention
5	Not reported
6	Not reported
7	Not reported

For exception conditions (CC=2), a second level of status is available in the Interrupt Status Byte (ISB) of the interrupt ID word. For condition code 3, the interrupt status byte contains binary zeros.

Command	*Condition code (CC) values*							
	CC0	*CC1*	*CC2*	*CC3*	*CC4*	*CC5*	*CC6*	*CC7*
Prepare	X					X		X
Device reset	X							X
Read device ID	X	X	X			X		X
Start	X	X	X			X		X
Start cycles steal status	X	X	X			X		X

CC value	*Meaning*
0	Device not attached
1	Busy
2	Busy after reset
3	Not reported
4	Not reported
5	Interface data check
6	Not reported
7	Satisfactory

Note. Condition code zero (CC = 0) is reported if the diskette unit is not attached to the channel or power is off the unit.



Bit 0	Device Dependent Status Available Set on when additional status information is available from the diskette attachment.
Bit 1	Delayed Command Reject. Set on when the diskette attachment cannot execute a command because of an incorrect parameter in the IDCB.
Bit 2	Not used. Should be zero.
Bit 3	DCB Specification Check Set on when the diskette attachment cannot execute the command because a parameter in the DCB is incorrectly specified to perform the desired operation.
Bit 4	Storage Data Check Set on when the storage location accessed during the current cycle steal output cycle contains bad parity.
Bit 5	Invalid Storage Address Set on as a result of a cycle steal I/O operation when the main storage address presented by the attachment for data or DCB access exceeds the storage size fitted on the system.
Bit 6	Protect Check Set on when the attachment attempts to access a cycle steal location without the correct cycle steal address key.
Bit 7	Interface Data Check Set on when a parity error is detected on a cycle steal data transfer. The condition can be detected by the attachment or by the channel.

Interrupts

The diskette unit attachment can interrupt the processor with two types of interrupts, end-of-operation and attention. Before either type of interrupt can be presented, however, the attachment must be prepared to interrupt by means of the prepare command described in this chapter.

Note. Hardware processing of an interrupt includes automatic branching to a service routine. The processor uses a reserved area in main storage for branch information. Refer to "Prerequisite Publications" in the Preface of this manual for processor description manuals that explain reserved storage and interrupt handling.

End-of-Operation Interrupts

When an operation initiated by any of the interrupt-causing commands ends normally or is terminated due to an error, the diskette unit requests an end-of-operation interrupt. The interrupt-causing commands are:

- Start
- Start cycle steal status
- Start diagnostic

When the attachment receives one of these commands, it enters the "busy" state. Until the diskette unit completes an operation initiated by an interrupt-causing command, the attachment responds "busy" to all other such commands. The attachment will, however, accept and execute the non-interrupt-causing commands; prepare, device reset, read ID, or halt I/O. The attachment reports a condition code for all interrupt-causing commands when the IO instruction is executed and when the interrupt request is serviced by the processor. The first condition code describes whether the command has been accepted. The second condition code is sent to the processor with interrupt status information at interrupt presentation time.

Interrupt status information is returned in the form of an interrupt ID word. The low-order byte of the interrupt ID word is the device address. The high-order byte is either an interrupt status byte (ISB) if the operation failed (CC=2), or an interrupt information byte (IIB) if the operation was successful (CC=3).

Interrupt Status Byte

When an exception interrupt is serviced by the processor, the attachment presents an interrupt ID word containing the device address and interrupt status byte (ISB). The ISB bit meanings are:

ISB Bit	*Meaning*
0	*Device status available.* Additional information about the operation is available when this bit is set to one. The information is stored in cycle steal status word 1. To obtain the information, issue a start cycle steal status command. See "Start Cycle Steal Status."
1	*Delayed command reject.* This bit, set to one, means that the attachment detected an error in the operate I/O instruction. An invalid I/O command or an odd DCB address in the IDCB can cause this kind of error.
2	*Not reported.* This bit is always set to zero.
3	*DCB specification check.* This bits, set to one, means the diskette operation failed because of an invalid DCB parameter. Any of the eight words in the DCB associated with the diskette operation can set this bit to one. The residual address stored in cycle steal status word 0 points to the DCB word containing the invalid parameter. To obtain the residual address, see "Start Cycle Steal Status Command" later in this chapter.
4	*Storage data check.* If data accessed from main storage during a cycle steal output operation is out of parity, this bit is set to one. A machine check condition does not occur, and the parity of the data in that storage location is not corrected.
5	*Invalid storage address.* When the main storage address specified in the DCB is outside the capacity of main storage, this bit is set to one. This bit can be set during either an input or output cycle steal operation. The operation is terminated immediately.
6	*Protect check.* When the attachment attempts to transfer data to a main storage location using an incorrect cycle steal address key, this bit is set to one. The operation is terminated immediately.
7	*Interface data check.* When a parity error is detected at the interface by either the attachment or the channel, this bit is set to one. The operation is terminated immediately.

Attention Interrupt

An attention interrupt request is sent to the processor only to notify the processor that the diskette unit has become 'ready' and is operational.

The diskette attachment is inhibited from requesting attention interrupts during Initial Program Load (IPL) operations. If the diskette unit is not ready when an IPL operation is attempted the attachment enters the 'wait' state until the diskette unit becomes operational and then continues with the IPL sequence. When the IPL operation ends, the attachment sends an end-of-operation request to the processor. At interrupt presentation time, a device end condition is reported to the processor. If an attention interrupt request is pending when an IPL is initiated, the interrupt request is reset.

Note. The diskette attachment does not send an attention interrupt request when 'ready' *drops*.

Resetting the Attachment

Several methods of resetting attachment controls and registers are available.

Power-on Reset

Resets: all controls and registers including the prepare register. The attachment remains busy for 12 seconds after a power-on reset.

System Reset

Resets: all controls and registers including the prepare register.

Initial Program Load

Resets: all controls and registers including the prepare register.

Halt I/O Command

Resets: all controls and registers except the prepare register.

Device Reset Command

Resets: all controls and registers except the prepare register.

Initial Program Load (IPL)

An initial program load (IPL) operation loads information from cylinder 00 on the head 0 side of the diskette into processor main storage beginning at location 0000. The information initializes the processor with the program data required to commence operations. Initial program load operations are hardware initiated only.

After the attachment responds to 'Initiate IPL' from the processor, it performs a seek recalibrate operation which locates the head access mechanism at cylinder 00 with head 0 selected. The attachment begins a Read Data operation with a DCB byte count of X'0100' (256 decimal) which implies a multiple sector data transfer (two sectors of 128 bytes each). The data is read from the first two sectors following the index and transferred into main storage in cycle steal mode. When the diskette unit has successfully completed the IPL sequence, the attachment presents a device end condition code on interrupt level 0 at interrupt presentation time. If the IPL operation fails to execute successfully, make sure the diskette is inserted properly in the diskette unit and that the POWER ON/OFF switch is in the ON position before attempting another IPL operation.

The 4964 Diskette Storage Unit and Diskette Attachment Feature can be used as either a primary or alternate IPL source.

Index

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