IBM

Series/1

GA34-0056-0

File No. S1-08

IBM Series/1
Two Channel Switch Feature
Description

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Two Channel Switch Feature
Description

First Edition (May 1978)

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This publication describes the operational and functional characteristics of the IBM Two Channel Switch (TCS) feature. The user must have a good understanding of data processing terminology and be familiar with binary and hexadecimal numbering systems. In addition, the user must have a good understanding of Series/1 programming. This publication is intended primarily as a reference manual for experienced programmers who require machine code information to plan, write, correct, and modify programs (written in assembler language) required to integrate the TCS into their data processing system.

Summary of Publication

- *Chapter 1. Introduction* contains a description of the general characteristics of the TCS. It also contains a functional description of the relationship of the TCS, IBM 4959 I/O Expansion Unit, and the Series/1 processor.
- *Chapter 2. Programming Information* describes the I/O commands and control words that are used to operate the TCS. Specific command and status word bit structures are described. Condition codes, status information, and interrupts related to the TCS operation are also included.
- *Chapter 3. Console* describes the controls and indicators of the TCS console. Operator intervention procedures for manually switching processors and alerting the program of impending operator action are also provided.
- *Appendix A. Reference Information* condenses the I/O commands, status words, and condition codes for quick reference. Specifications and reference information pertaining to the user's alarm device are included.

Prerequisite Publications

IBM Series/1 Model 5 4955 Processor and Processor Feature Description, GA34-0021 and/or *IBM Series/1 Model 3 4953 Processor and Processor Feature Description*, GA34-0022

Related Publications

Additional publications are listed in the *IBM Series/1 Graphic Bibliography*, GA34-0055.

Chapter 1. Introduction

The Series/1 Two Channel Switch (TCS) is a feature of the 4959 I/O Expansion Unit and is designed to switch common I/O devices between two Series/1 processors. Common application for the TCS is in a primary/backup system configuration. The capability of switching the common I/O devices reduces the need for redundant I/O devices in the overall system configuration, thereby, lowering the cost.

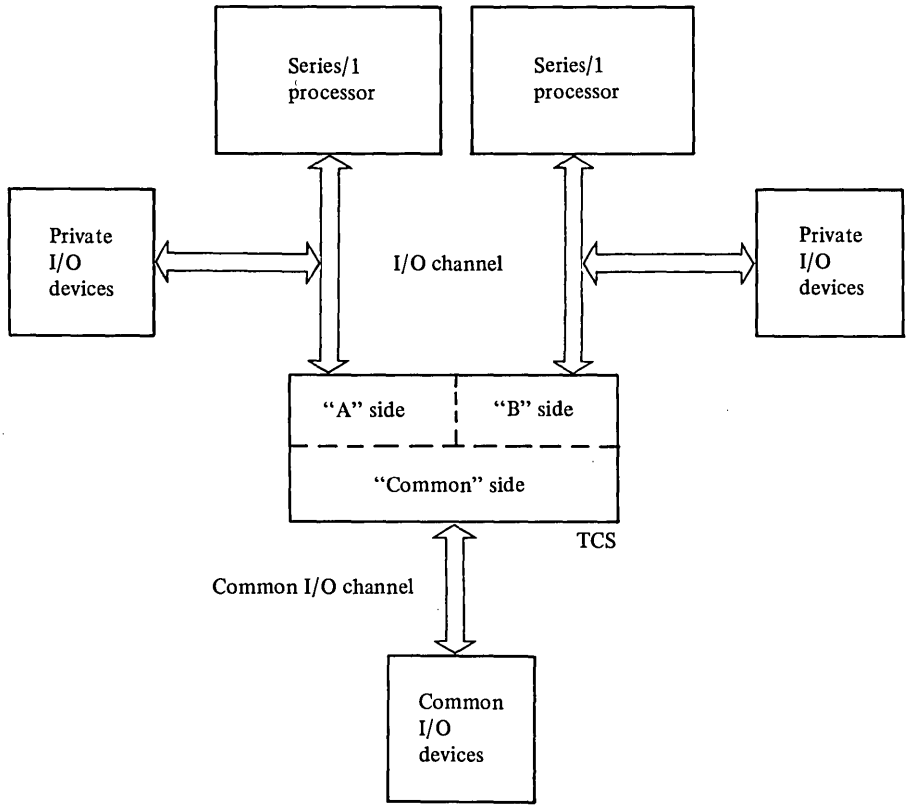
As shown in Figure 1-1, one Series/1 processor is cabled to the "A" side of the TCS with the other processor cabled to the "B" side. The common I/O devices are connected to the "common" side of the TCS. At any given time, the TCS connects the common I/O channel to one of the processors and also monitors the I/O channels of both processors.

Note. The initial connection of the common I/O to the primary processor must be made by the operator. This requires a manual operation from the TCS console. (See "Initial Connection" in Chapter 3.)

Once the TCS has connected the common I/O channel to one of the processors, the TCS is transparent to the common I/O devices.

The primary processor must be programmed to keep a TCS timer running in order to maintain control of the common I/O; otherwise, a time-out occurs and the TCS notifies the backup processor that a switchover should take place. The program in the backup processor then takes control of the common I/O. The I/O command used by the backup processor to cause a switchover does not execute unless a time-out condition has occurred. This provides a programming interlock to ensure that switchover is done at the proper time. Refer to "Processor Switchover" in Chapter 2.

The TCS requires operator intervention or a Host IPL from a host system to switch the common I/O back to the primary processor.



Note. Either processor can be designated as primary or backup and can be connected to either the "A" or "B" side of the TCS.

Figure 1-1. Block diagram of two Series/1 processors and the TCS

Either processor can receive its IPL from the common I/O provided the common I/O device has been designated as an IPL device and is connected to the processor.

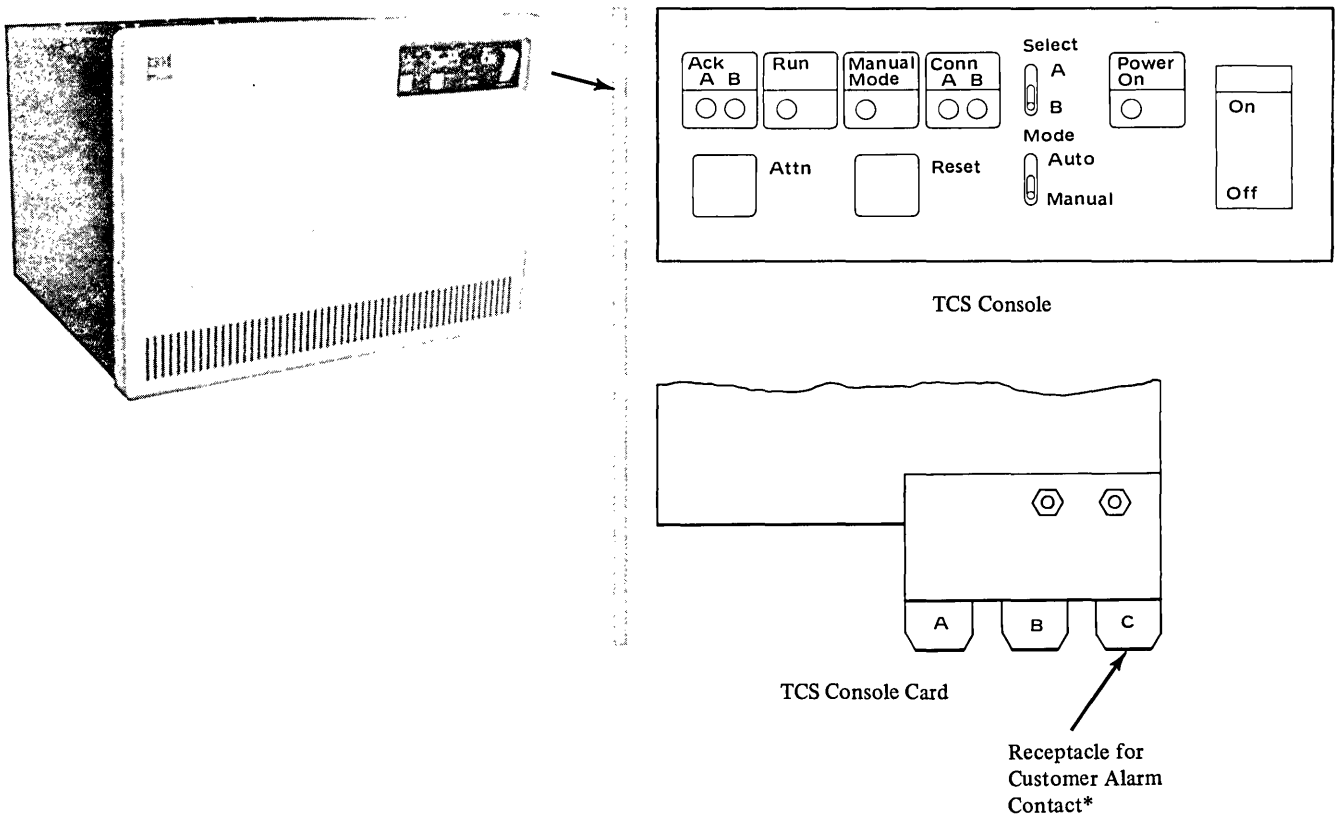
Functional Description

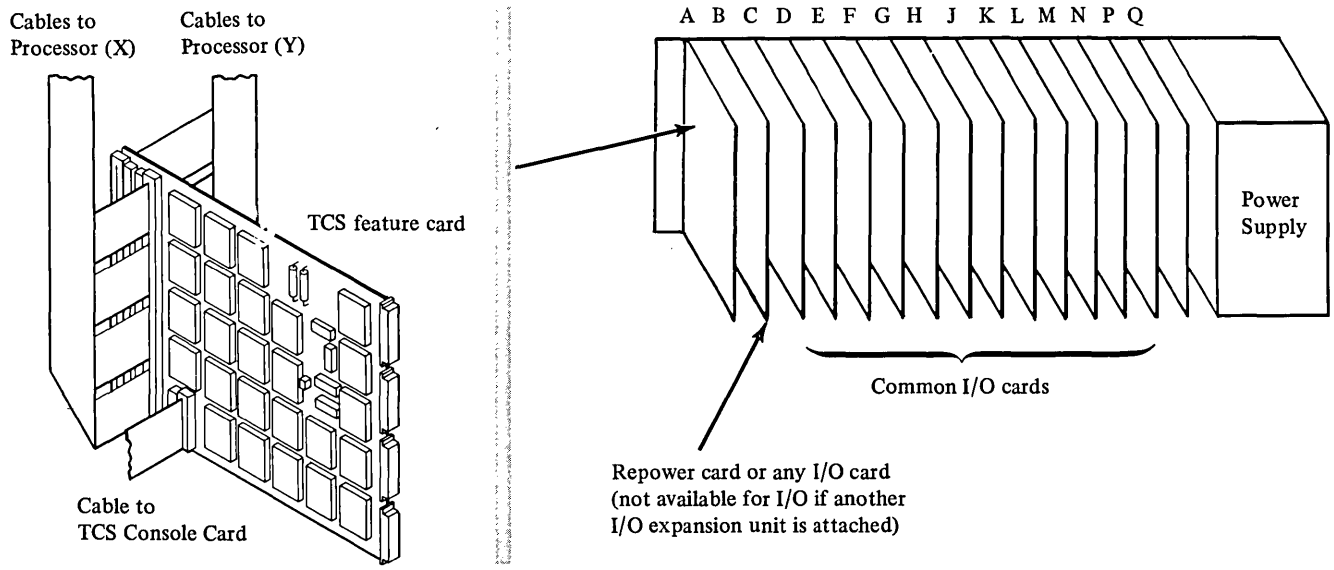
The IBM 4959 I/O Expansion Unit provides supplemental I/O attachment capability to the Series/1 processor. It occupies the full width of a 19-inch rack enclosure. A maximum of 14 I/O feature locations are contained in a 4959 I/O Expansion Unit.

The TCS is a field installable feature that is housed in the IBM 4959 I/O Expansion Unit. When the TCS feature is installed, the I/O features (in the associated 4959 I/O Expansion rack) become the common I/O devices for the system. The I/O expansion unit supplies power to the TCS feature card along with the common I/O feature cards.

The TCS feature is comprised of: the console control panel, the console card, the front cover, nine cables, and the TCS feature card. As shown in Figure 1-2, the TCS feature card resides in slot "A" of the IBM 4959 I/O Expansion unit and has eight cables for the processors (four cables to each processor) and one cable for the TCS console. Additional IBM 4959 I/O Expansion Units can be cabled to the common I/O channel (via the Channel Repower Feature) to increase the number of common I/O devices.

An output contact is provided on the TCS console card to allow a user to connect an external alarm device. The external alarm device is provided by the customer and is not part of the TCS feature. This device (audible alarm) can be used to alert the user that an exception condition has occurred. (Refer to "Appendix A" for a description of the output contact.)





* This receptacle is visible when the front cover is removed.

Figure 1-2. IBM 4959 I/O Expansion Unit with TCS feature installed

Configuration Description

Figure 1-3 shows two typical system configurations using the TCS feature.

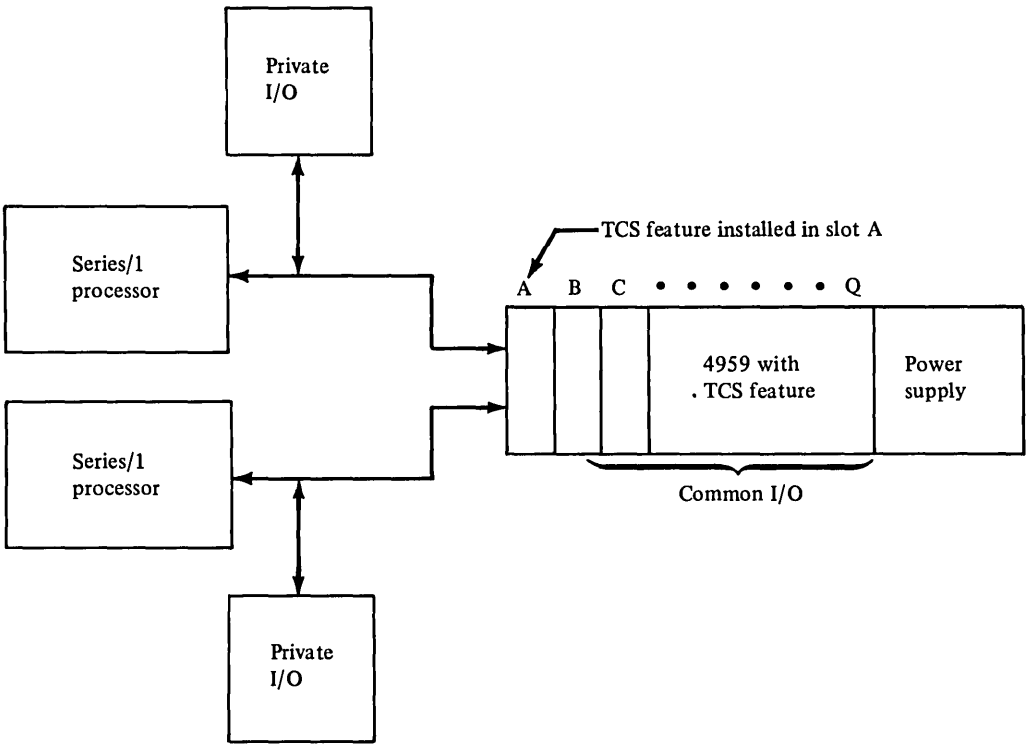
In the system configuration where one TCS is used, one set of common I/O can be switched from one processor to the other.

In the other system configuration, two TCS features are used. Each processor controls a set of common I/O. If processor (X) fails, its common I/O can be switched to processor (Y). Conversely, if processor (Y) fails, its common I/O can be switched to processor (X).

In both system configurations, additional IBM 4959 I/O Expansion Units can be cabled to the common I/O channels to increase the number of common I/O devices.

Note. The common I/O device addresses must not duplicate any of the private I/O device addresses.

System using one TCS feature



System using two TCS features

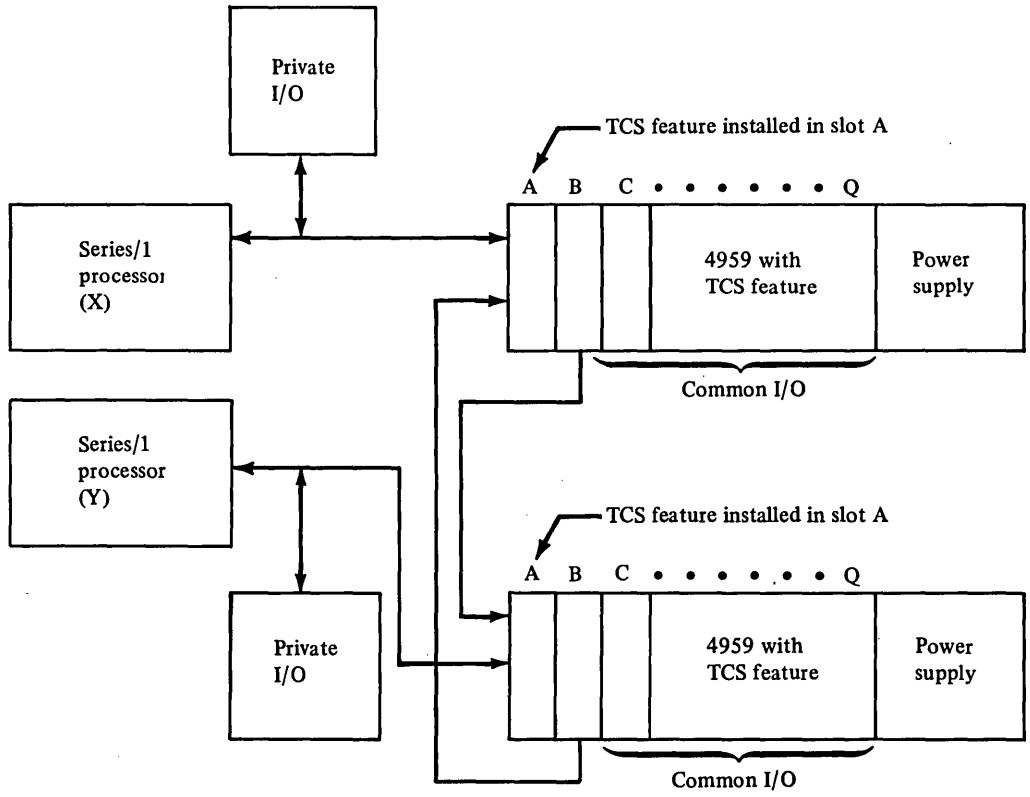


Figure 1-3. Typical system configurations using TCS feature

Chapter 2. Programming Information

This chapter describes the I/O commands and control words that are used to control the Two Channel Switch (TCS) operation. Condition codes, status information, interrupts, resets, and program switchover are also described in this chapter.

Note. I/O commands and operations related to the common and private I/O devices are described in the individual device publications.

Figure 2-1 shows a typical cabling arrangement for the TCS. Note that a processor is cabled to only one side ("A" or "B") of the TCS. Each side of the TCS contains a prepare register, a status word, channel control circuitry, condition codes, interrupt circuitry, and command decode circuitry that are dedicated to the cabled processor. The "common" side of the TCS contains the console panel, an operations monitor (timer), and the switching circuitry required to switch the common I/O channel to the "A" or "B" side of the TCS.

The private I/O devices connected to each processor's I/O channel are referred to as *inboard* of the TCS. The common I/O devices connected to the common I/O channel are referred to as *outboard* of the TCS.

I/O commands for the TCS are initiated by a processor and are directed to the side of the TCS that is cabled to the processor. Two sets of command decode circuitry (one for the "A" side and one for the "B" side) are provided, in the TCS, to accept and execute the corresponding processor-issued commands.

Data is transferred on the I/O channel in parallel form (16 bits plus 2 parity). The direction that the data moves on the channel is determined by the I/O command. The TCS responds to its own set of I/O

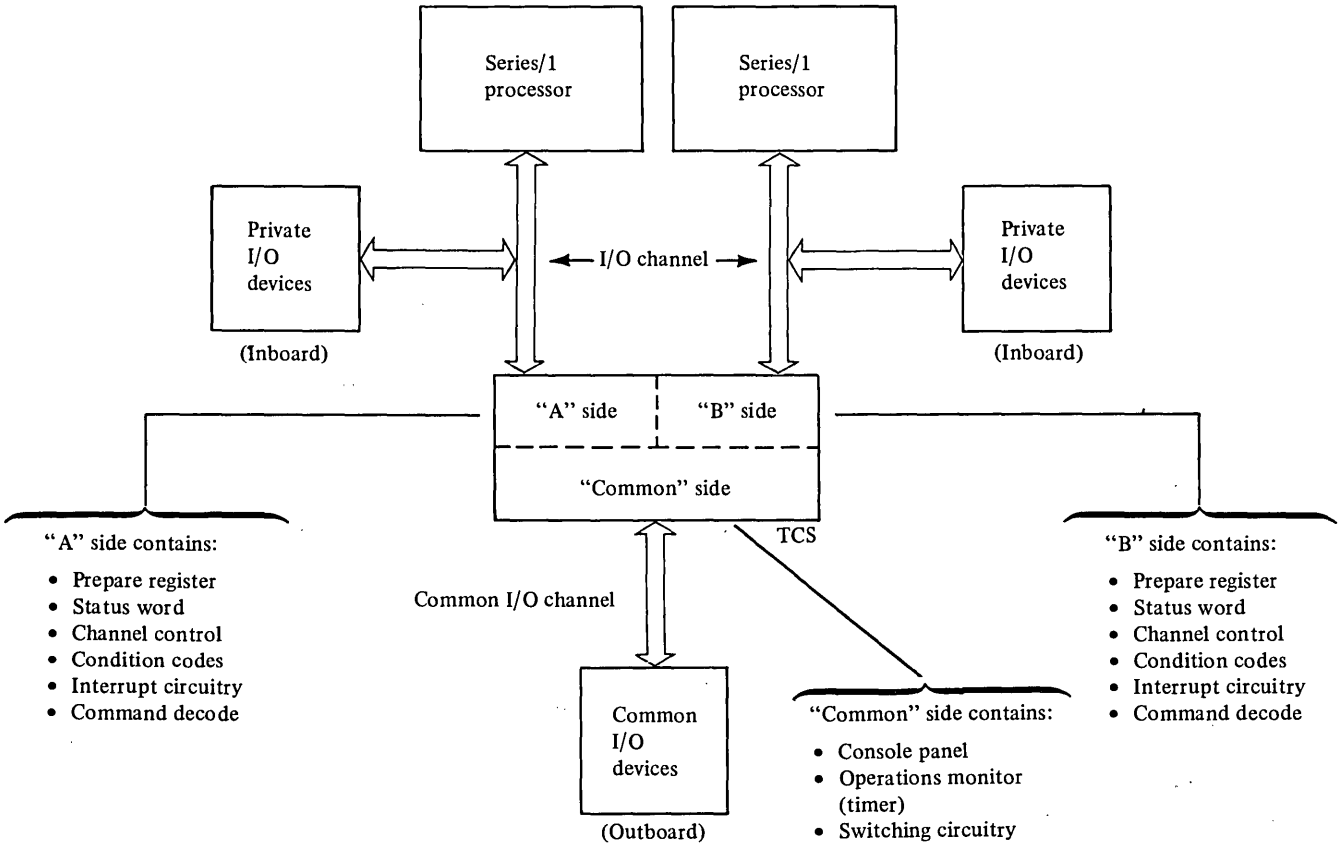


Figure 2-1. Block diagram of typical cabling arrangement

commands. These commands initiate Direct Program Control (DPC) operations only. Once the TCS establishes the connection between the common I/O and one of the processors, the TCS is transparent to the outboard I/O devices. The common I/O devices may operate in DPC mode or cycle steal mode.

Note. The initial connection of the common I/O to the primary processor must be made by the operator. This requires a manual operation from the TCS console. (See "Initial Connection" in Chapter 3.)

Initiating Two Channel Switch Operation

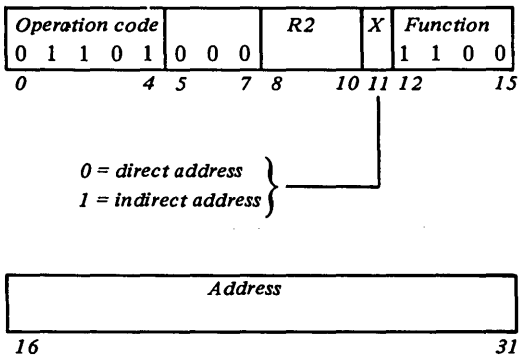
Every I/O operation directed to the TCS requires (in the corresponding processor's storage):

- An Operate I/O (IO) instruction
- An immediate device control block (IDCB) that contains an I/O command, a device address, and an immediate data field

These requirements are described in the following sections.

Operate I/O Instruction

The Operate I/O instruction initiates all I/O operations from the issuing processor. This instruction points to an immediate device control block (IDCB) in the processor's storage that contains an I/O command, device address, and immediate data field. Every Operate I/O instruction must have an associated IDCB. The format for the Operate I/O instruction is:

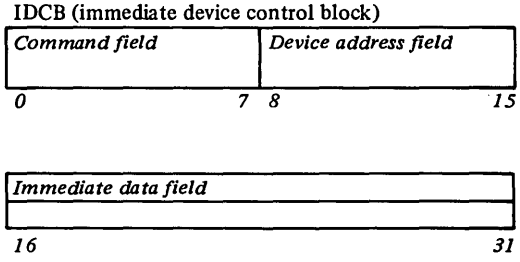


Note. A detailed description of the Operate I/O instruction can be found in the IBM Series/1 processor unit description manuals. Refer to the Preface of this manual for titles and order numbers.

Immediate Device Control Block (IDCB)

An immediate device control block (IDCB) is stored (in processor storage) for every I/O command issued to the TCS. Before issuing an Operate I/O instruction to the TCS, an I/O command is stored in the command field of the associated IDCB. The immediate data field of the IDCB (used for the TCS commands) contains either a data word or is all zeros. The format for the IDCB is:

IDCB (immediate device control block)



Note. A detailed description of the IDCB can be found in the IBM Series/1 processor unit description manuals. Refer to the Preface of this manual for titles and order numbers.

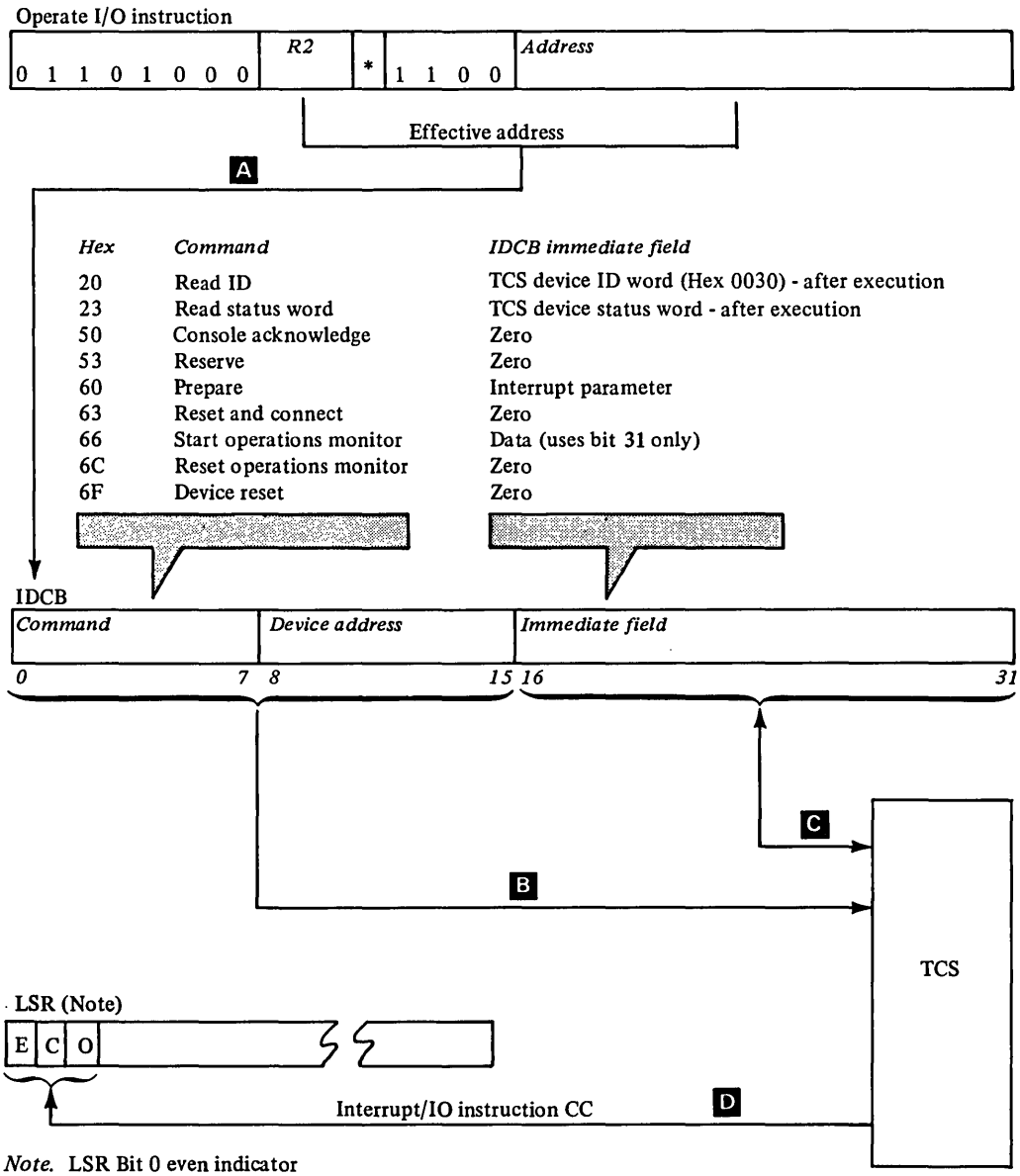
Direct Program Control (DPC) Operation

The TCS communicates with one of the processors (via its I/O channel) only in the DPC mode of operation. A DPC operation causes an immediate transfer of data or control information to/from the TCS. An Operate I/O instruction is executed for each data transfer and causes the following events to occur (refer to Figure 2-2):

- The Operate I/O instruction points to the IDCB in processor storage A.
- The addressed TCS uses the IDCB to determine which operation, defined by the command, is to be performed B.
- The I/O channel sends data to the TCS from processor storage, or from the TCS to processor storage C.
- The TCS sends an IO instruction condition code to the processor's level status register (LSR) D.

Notes.

1. The DPC operation can end with a priority interrupt. Refer to "I/O Interrupts" elsewhere in this chapter.
2. There are two types of condition codes: (a) the IO instruction condition code, and (b) the interrupt condition code. Refer to "Status Information" in subsequent paragraphs in this chapter.



Note. LSR Bit 0 even indicator
Bit 1 carry indicator
Bit 2 overflow indicator

*Indirect addressing bit

Figure 2-2. Direct program control I/O operation corresponding to the issuing processor

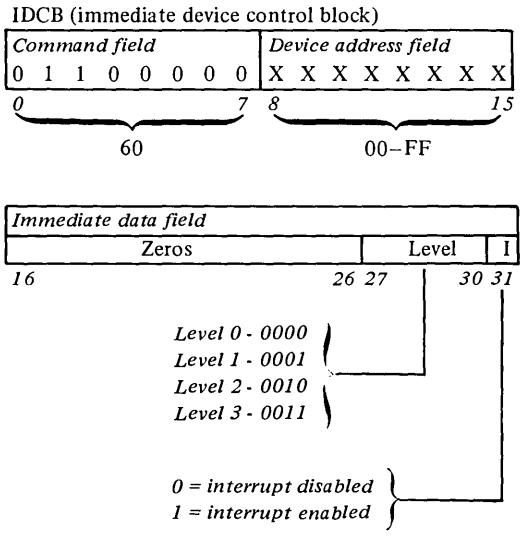
Command Execution

Commands directed to the TCS transfer a single word containing data or zeros to/from the immediate data field of an IDCB in the corresponding processor's main storage. Command execution is completed when a condition code (see "Status Information" in this chapter) is reported to the processor immediately following the DPC operation.

The following paragraphs describe the commands used by the TCS. The device address field contains X's since the address value must be determined at installation time. The command field (bits 0–7) of each IDCB shows the binary value of the TCS command. The appropriate IDCB is shown with each command description.

Prepare

This command transfers interrupt parameters from the immediate data field of the IDCB to the *prepare register* on the side of the TCS to which the issuing processor is cabled ("A" or "B" side). The format of the IDCB is:



A priority interrupt level is assigned to the TCS by the *level* field. The I-bit (device mask) controls the interrupt capability of the TCS. If the I-bit equals 0, the TCS is not allowed to interrupt. If the I-bit equals 1, the TCS is allowed to interrupt.

The Prepare command must be issued by a processor before the TCS can interrupt that processor. Otherwise, the interrupt presentation is blocked and the TCS remains in an interrupt pending condition until (1) the condition is cleared by a reset or (2) a Prepare command is issued by the appropriate processor.

The only valid condition codes returned by the TCS in response to a Prepare command are Interface Data Check (CC5) and Satisfactory (CC7). An interrupt may result if an interrupt pending condition existed before issuing the Prepare command.

Note. A detailed description of interrupt levels can be found in the IBM Series/1 processor unit description manuals. Refer to the Preface of this manual for titles and order numbers.

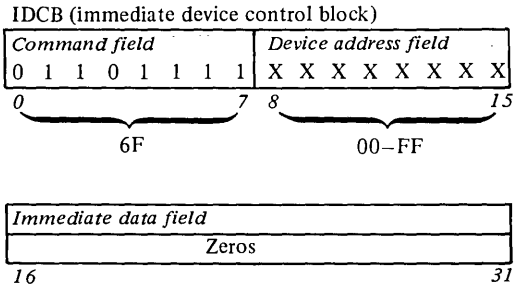
Device Reset

This command resets the side of the TCS cabled to the issuing processor. This reset applies to:

- All pending interrupts
- The acknowledge indicator (on the TCS console)
- The *reserve* bit (bit 3) of the status word for the other processor only
- The *control mode alert* bit (bit 9) and common I/O (CIO) connection alert bit (bit 8) of the status word
- The operations monitor (timer); however, the timer resets to the starting point and continues to run

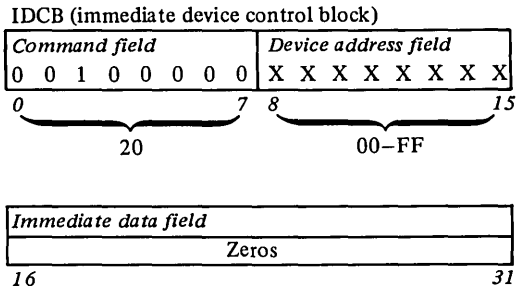
Note. Refer to "Read Status Word" for more information about the status word.

The Device Reset command does not reset the *prepare register* of the TCS and does not cause an interrupt. The TCS can only report Satisfactory (CC7) condition code to this command. The IDCB immediate data word is not used and should be set to zeros. The format of the IDCB is:

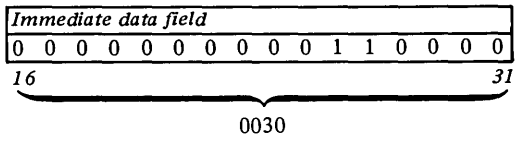


Read ID

This command transfers an identification (ID) word from the TCS to the immediate data field in the IDCB of the issuing processor. The TCS can only report Interface Data Check (CC5) and Satisfactory (CC7) condition codes to this command. If Interface Data Check (CC5) is reported, the command is not executed. The Read ID command does not cause an interrupt. The format of the IDCB is:



After execution of the Read ID command, the immediate data field of the IDCB contains:



Console Acknowledge

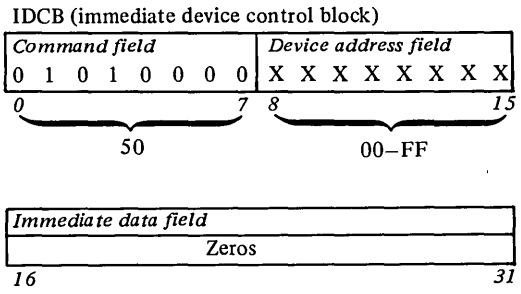
This command turns ON the Ack A or Ack B indicator, corresponding to the issuing processor, on the TCS Console (refer to Chapter 3). If the indicator was ON, it will remain in that state. Both indicators turn off when:

- An operator intervenes from the TCS console.
- A power-on-reset (from the TCS I/O expansion unit) occurs.

The indicator corresponding to the issuing processor turns off when:

- A Device Reset command is executed.
- A Halt I/O command is executed.
- A system reset occurs.

Condition codes that may be reported to this command are Busy (CC1), Interface Data Check (CC5), and Satisfactory (CC7). If Interface Data Check (CC5) is reported, the command is not executed. If the TCS has an interrupt pending, only Busy (CC1) is reported and the command is not executed. The Console Acknowledge command does not cause an interrupt. The IDCB data word is not used and should be set to zeros. The format of the IDCB is:



Reserve

This command causes an attention interrupt to the other processor with bit 3 of the interrupt information byte (IIB) set to 1. This notifies the other processor that the issuing processor is available for switchover. (If the Prepare command was not previously issued by the other processor, the Reserve command will execute; however, the attention interrupt cannot occur.) In addition, the reserve bit (bit 3) of the status word of the *other* processor is set to 1. If the reserve bit was previously set to 1, it will remain in that state. Execution of this command does not cause an interrupt to the issuing processor. The TCS can report Busy (CC1), Command Reject (CC3), Intervention Required (CC4), Interface Data Check (CC5), and Satisfactory (CC7) condition codes to this command.

If the following circumstances exist, the Reserve command is not executed:

- The TCS is busy or has an interrupt pending or is pending (Condition Code 1 is reported).
- The TCS is in manual control mode (Condition Code 3 is reported).
- The TCS is in automatic control mode and the common I/O is connected to the issuing processor (Condition Code 3 is reported).
- The TCS is in automatic control mode, the issuing processor is not connected to the common I/O, and the operations monitor has timed out (Condition Code 4 is reported).
- A parity error is detected (Condition Code 5 is reported).

Note. Automatic control mode means that the TCS is operating under processor control. Manual control mode means that the TCS is in manual mode caused by operator intervention (see Chapter 3).

The IDCB immediate data field is not used and should be set to zeros. The format of the IDCB is:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 0 1 0 0 1 1	X X X X X X X X
0 ... *7*	*8* ... *15*
53	00–FF

Immediate data field
Zeros
16 ... *31*

Start Operations Monitor

If the issuing processor is connected to the common I/O, this command causes the TCS to start the operations monitor timer.

There is only one timer in the TCS. The timer switches with the common I/O connection.

The operations monitor is comprised of two selectable timing periods: the initial period and the warning period. If 0 seconds are selected, the warning period does not occur. (Refer to "Operations Monitor Timing" in this chapter.)

The Start Operations Monitor command (or Reset Operations Monitor command) begins the initial period. The end of the initial period is marked by an attention interrupt. A warning period may then begin before a time-out condition occurs. (See Figure 2-3.)

After the Start Operations Monitor command has been issued, the operations monitor will step through the initial and warning periods. Before the operations monitor reaches the end of the warning period, the corresponding processor must issue a Reset Operations Monitor command (see subsequent paragraph) to prevent the operations monitor from timing out. If the processor fails to issue the Reset Operations Monitor command, the operations monitor times out (and remains stopped) and an exception interrupt is issued to the corresponding processor. This is the technique used to initiate switchover from one processor to the other under program control. Normally the other processor has issued its Reserve command before switchover. When the operations monitor times out, the following occurs:

1. The *operations monitor time-out incurred* status bit (bit 5 of the status word) for the connected processor is set to 1.
2. An exception interrupt is issued to the connected processor.
3. The *operations monitor time-out* status bit (bit 2 of the status word) for the other processor is set to 1.
4. An attention interrupt is issued to the other processor.
5. The *connect go-ahead* bit (bit 2) of the interrupt information byte (IIB) for the other processor is set to 1.

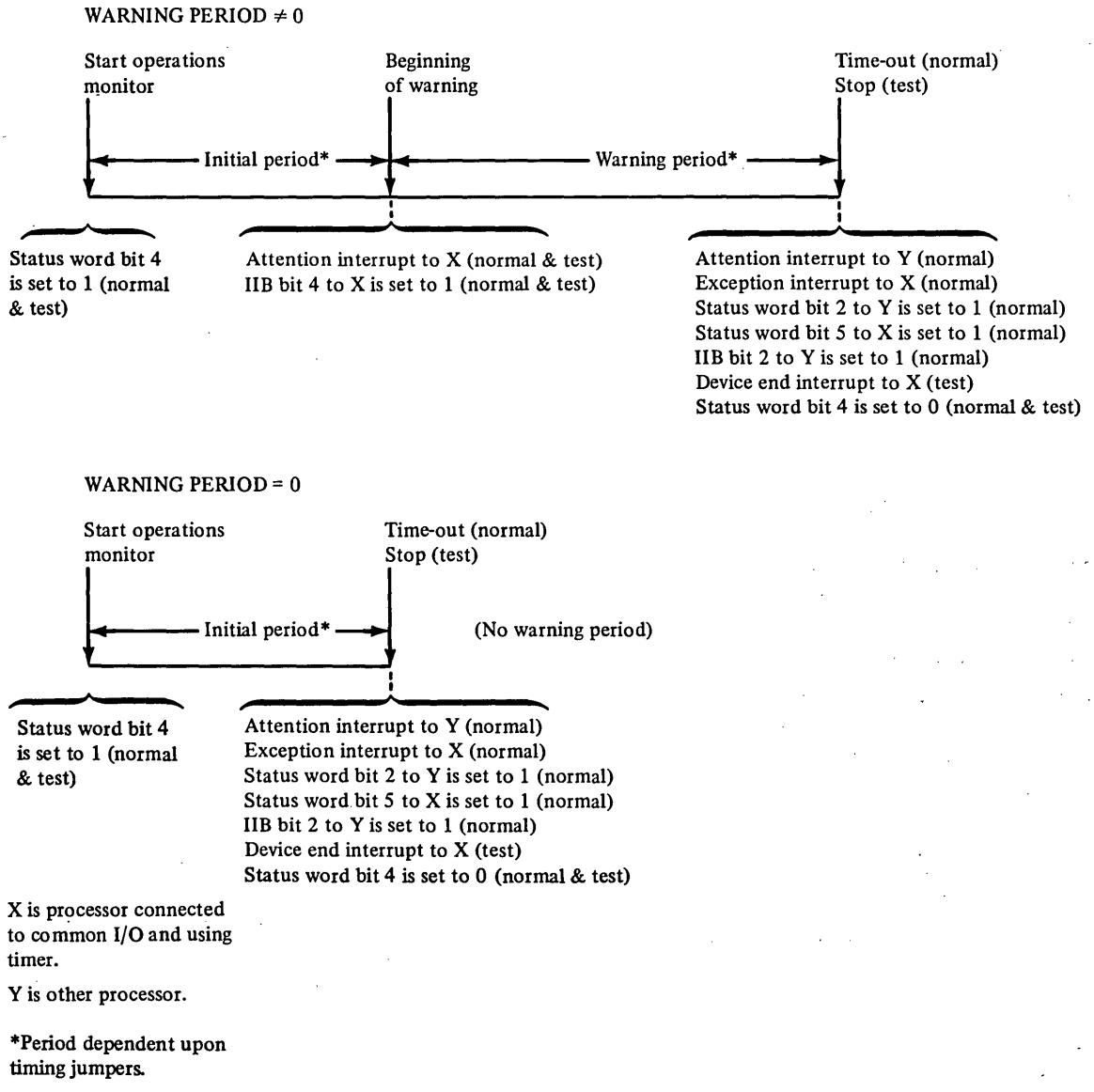


Figure 2-3. Initial/Warning period for normal and test modes

The Start Operations Monitor command is not executed if:

- The TCS is busy or has an interrupt pending (Condition Code 1 is reported).
- The TCS is in manual mode (Condition Code 3 is reported).
- The TCS is in automatic mode and the common I/O is not connected to the issuing processor (Condition Code 3 is reported).
- The TCS is in automatic mode, the common I/O is connected to the issuing processor, and the operations monitor has timed out (Condition Code 4 is reported).
- A parity error is detected (Condition Code 5 is reported).

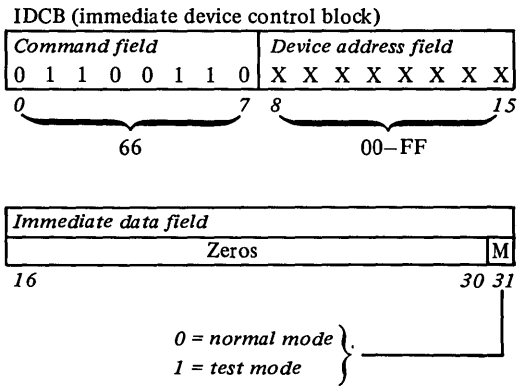
Note. Automatic mode and manual mode are explained in Chapter 3.

Operations Monitor in Normal/Test Mode

The IDCB immediate data word associated with the Start Operations Monitor command controls the running mode of the operations monitor. If bit 31 is set to 0, the operations monitor will operate in normal mode (as described in "Start Operations Monitor"). If bit 31 is set to 1, the operations monitor operates in test mode. The difference between normal mode and test mode (see Figure 2-3) is that, in test mode, the monitor stops but does not time-out as it does in normal mode. In addition, no operations monitor time-out is posted to either processor. *Operations monitor time-out* (bit 2 of the status word of the other processor) and *operations monitor time-out incurred* (bit 5 of the status word for the issuing processor) are not set in test mode. In addition, a device end interrupt request is presented to the issuing processor (indicating that the test mode has terminated normally) and the other processor is not presented with an attention interrupt request. Regardless of monitor mode, the effect of executing the Reset Operations Monitor command is the same.

Note. Attention interrupts may occur due to events asynchronous to the operations monitor. Refer to "I/O Interrupts" in this chapter.

The format of the IDCB is:



Reset Operations Monitor

This command must be issued periodically by the processor (connected to the common I/O) after the Start Operations Monitor command is issued, to ensure that the operations monitor does not time-out.

Execution of this command causes the operations monitor to reset to the starting/reset point (the operations monitor does not stop; it continues to run from the starting/reset point). If the operations monitor is stopped (has timed out), it remains in that state. This condition can cause a switchover to the other processor.

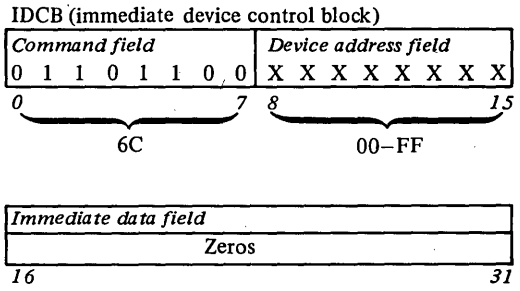
If the connected processor does not issue the Reset Operations Monitor command, the following events occur:

1. The operations monitor times out.
2. The *operations monitor time-out* status bit (bit 2 of the status word) for the other processor is set to 1.
3. The *operations monitor time-out incurred* status bit (bit 5 of the status word) for the connected processor is set to 1.
4. An exception interrupt is issued to the connected processor.
5. An attention interrupt is issued to the other processor.
6. The *connect go-ahead* bit (bit 2) of the interrupt status byte for the other processor is set to 1.

Note. Refer to Figure 2-3 for additional information on time-out in normal and test modes.

A pending *operations monitor warning* attention interrupt condition (bit 4 of the IIB) is reset when this command is executed if the warning period does not equal 0. (See "Interrupt Resets".) Only Satisfactory (CC7) condition code can be reported to this command.

The IDCB data word is not used and should be set to zeros. The format of the IDCB is:



Reset and Connect

This command causes a system reset to occur on the common I/O and then connects the common I/O to the issuing processor. This command is executed provided:

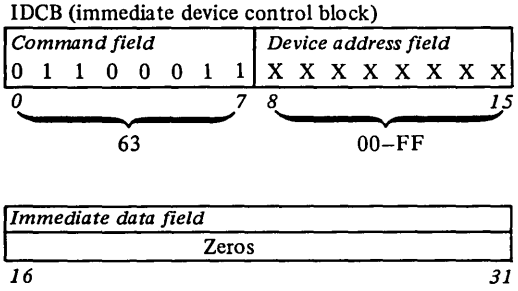
- The TCS is in automatic mode.
- The issuing processor is not connected to the common I/O.
- An operations monitor time-out is posted by the other processor.

The system reset to the common I/O does not affect private I/O devices inboard of the TCS. The time-out condition of the operations monitor is not reset and it remains in the time-out state after execution of this command. The Reset and Connect command is not executed and the common I/O is not switched if:

- The TCS is busy or has an interrupt pending (Condition Code 1 is reported).
- The TCS is in manual mode (Condition Code 3 is reported).
- The TCS is in automatic mode and the common I/O is not connected to the issuing processor but, an operations monitor time-out has not been posted by the other processor (Condition Code 3 is reported).
- The common I/O is already connected to the issuing processor (Condition Code 3 is reported).
- A parity error is detected (Condition Code 5 is reported).

The IDCB data word is not used and should be set to zeros. The IDCB format is:

IDCB (immediate device control block)



Read Status Word

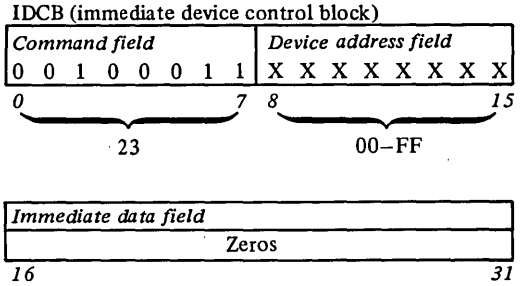
This command transfers a status word from the appropriate TCS side to the immediate data field of the IDCB of the issuing processor.

The Read Status Word command is not executed if:

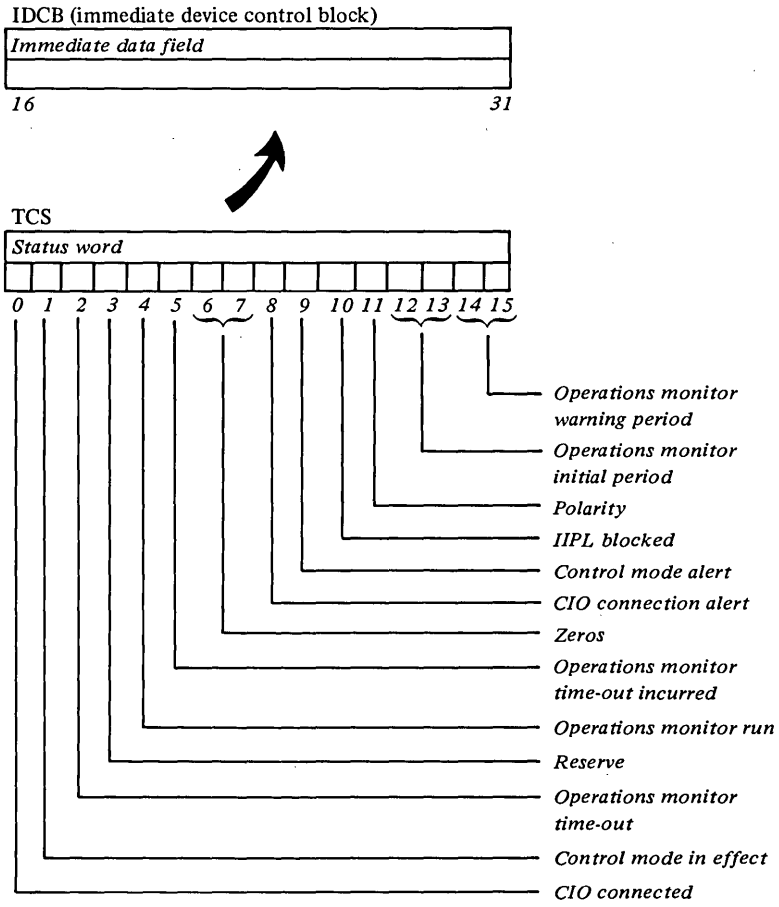
- The TCS has an interrupt pending (Condition Code 1 is reported).
- A parity error is detected (Condition Code 5 is reported).

The IDCB format is:

IDCB (immediate device control block)



After executing this command, the status word is transferred from the TCS to the IDCB as follows:



The status word bits have the following meanings:

Bit 0 *CIO connected.* This bit set to 1 indicates that the common I/O and timer are connected to the processor issuing the Read Status Word command. This bit is not affected by system reset, Halt I/O, or Device Reset; however, it can be changed by operator intervention (on TCS console) or by execution of the Reset and Connect command.

Bit 1 *Control mode in effect.* This bit set to 1 indicates that the TCS is in manual mode. This bit set to 0 indicates that the TCS is in automatic mode. This bit cannot be reset by either processor; however, it can be changed by operator intervention (on the TCS console).

Bit 2 *Operations monitor time-out.* This bit set to 1 indicates that an operations monitor time-out has been incurred by the other processor. This bit is set to 0 by a system reset on the other processor (but is not affected by a Halt I/O or Device Reset executed by the other processor). It cannot be reset by the issuing processor; however, it can be set to 0 by operator intervention (on the TCS console) and is held OFF in manual mode.

Bit 3 *Reserve.* This bit set to 1 indicates that the other processor has posted a reserve by executing a Reserve command. This bit is set to 0 by a system reset, Halt I/O, Device Reset, or a Reset and Connect command executed by the other processor. It can be set to 0 by operator intervention (on the TCS console) and is held OFF in manual mode.

Bit 4 *Operations monitor run.* This bit is set to 1 when the Start Operations Monitor command is executed and the operations monitor is running. This bit set to 0 indicates that the operations monitor has stopped in test mode or timed-out in normal mode.

Bit 5 — *Operations monitor time-out incurred.* This bit set to 1 indicates that the operations monitor has incurred a time-out while it was connected to the issuing processor. It is set to 0 by a system reset occurring on the issuing processor. This bit set to 1 also causes the alarm relay to be activated. It is set to 0 by operator intervention (on the TCS console) and is held OFF in manual mode. It is not affected by a system reset, Halt I/O or Device Reset on the issuing processor.

Bits 6–7 — Presented as zeros.

Bit 8 — *CIO connection alert.* If the Select switch setting on the TCS console differs from the common I/O connection indicated by status word bit 0, this bit is set to 1 when the operator releases the Attn key. This bit is set to 0 when the Select switch setting and common I/O connection agree and by: execution of the Read Status Word command, system reset, Halt I/O, or Device Reset by the issuing processor, or by operator intervention (pressing Reset on the TCS console).

Bit 9 — *Control mode alert.* If the Mode switch setting on the TCS console differs from the control mode in effect indicated by status word bit 1 this bit is set to 1, when the operator releases the Attn key. This bit is set to 0 when the Mode switch setting and the control mode agree and by: execution of the Read Status Word command, system reset, Halt I/O, or Device Reset by the issuing processor, or by operator intervention (pressing Reset on the TCS console).

Bit 10 — *Initiate initial program load (IIPL) blocked.* This bit set to 1 indicates that the Initiate IPL signal line is blocked to the common I/O. The issuing processor cannot Initial Program Load from the common I/O and must receive its processor initiated IPL from an I/O device inboard of the TCS. This bit set to 0 indicates that an IPL is permitted from the common I/O devices outboard of the TCS. This is selectable by jumper option. (See "Initial Program Load" paragraph in this chapter.)

Bit 11 — *Polarity.* This bit set to 1 indicates that the issuing processor is cabled to the "A" side of the TCS. This bit set to 0 indicates that the issuing processor is cabled to the "B" side of the TCS.

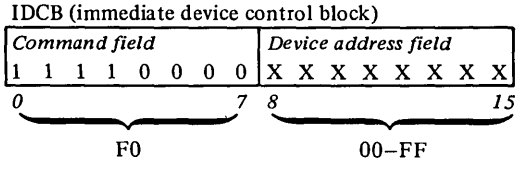
Bits 12–13 — *Operations monitor initial period.* Configuration of these bits reflect the jumper settings of the operations monitor initial period. (See "Operations Monitor Timing" in this chapter.)

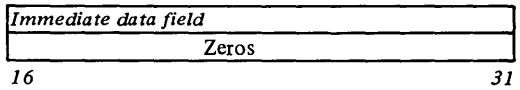
Bits 14–15 — *Operations monitor warning period.* Configuration of these bits reflect the jumper settings of the operations monitor warning period. (See "Operations Monitor Timing" in this chapter.)

Halt I/O

This is a *channel* directed command that causes a halt of all I/O activity on the I/O channel and resets the appropriate TCS side. All "connected" devices (including common I/O) are also reset. No data is associated with this command. All pending interrupts (on the appropriate TCS side) are cleared. The TCS priority-interrupt-level assignment and device mask (I-bit) are unchanged. This command does not alter the operations monitor. The format of the IDCB is:

IDCB (immediate device control block)





I/O Interrupts

The TCS is capable of interrupting both processors by using the following interrupts:

Exception—An operations monitor time-out in normal mode has occurred.
Device end—An operations monitor time-out in test mode has occurred.

Attention—An event asynchronous to the program of the accepting processor has occurred. Bits in the interrupt information byte (IIB) define the cause of interrupt.
Attention and exception—An event asynchronous to the program of the accepting processor has occurred and an operations monitor time-out in normal mode has occurred.
Attention and device end—An event asynchronous to the program of the accepting processor has occurred and an operations monitor time-out in test mode has occurred.

Each interrupt is defined by condition codes reported during interrupt acceptance time. Refer to "Interrupt Condition Codes" in a subsequent section of this chapter. Before these interrupts can be presented to the associated processor, the TCS must be prepared to interrupt. This is accomplished by the Prepare command. Refer to the "Prepare" command previously described in this chapter.

Additional information pertaining to specific interrupts is contained in either the interrupt information byte (IIB) or the interrupt status byte (ISB) of the interrupt ID word. Refer to "Interrupt ID Word" in a subsequent section.

An interrupt pending condition exists when the TCS has posted one of the interrupts but the interrupt has not been accepted by the associated processor.

An interrupt causes the Series/1 processor to suspend execution of its main line program and to initiate instructions that are designed to investigate the nature of the interrupt. Once the interrupt has been serviced, the processor will continue with its main line program. This allows the processor to immediately respond to an important event that occurs in the TCS without continually checking for its occurrence.

Status Information

Status information is provided by:

- IO Instruction Condition Codes
- Interrupt Condition Codes
- Status Words (see *Read Status Word* command in this chapter)
- Interrupt ID Word

Figure 2-4 presents an overall view of condition code reporting along with interrupt status information. Details of the condition codes and interrupt status information are described in subsequent paragraphs.

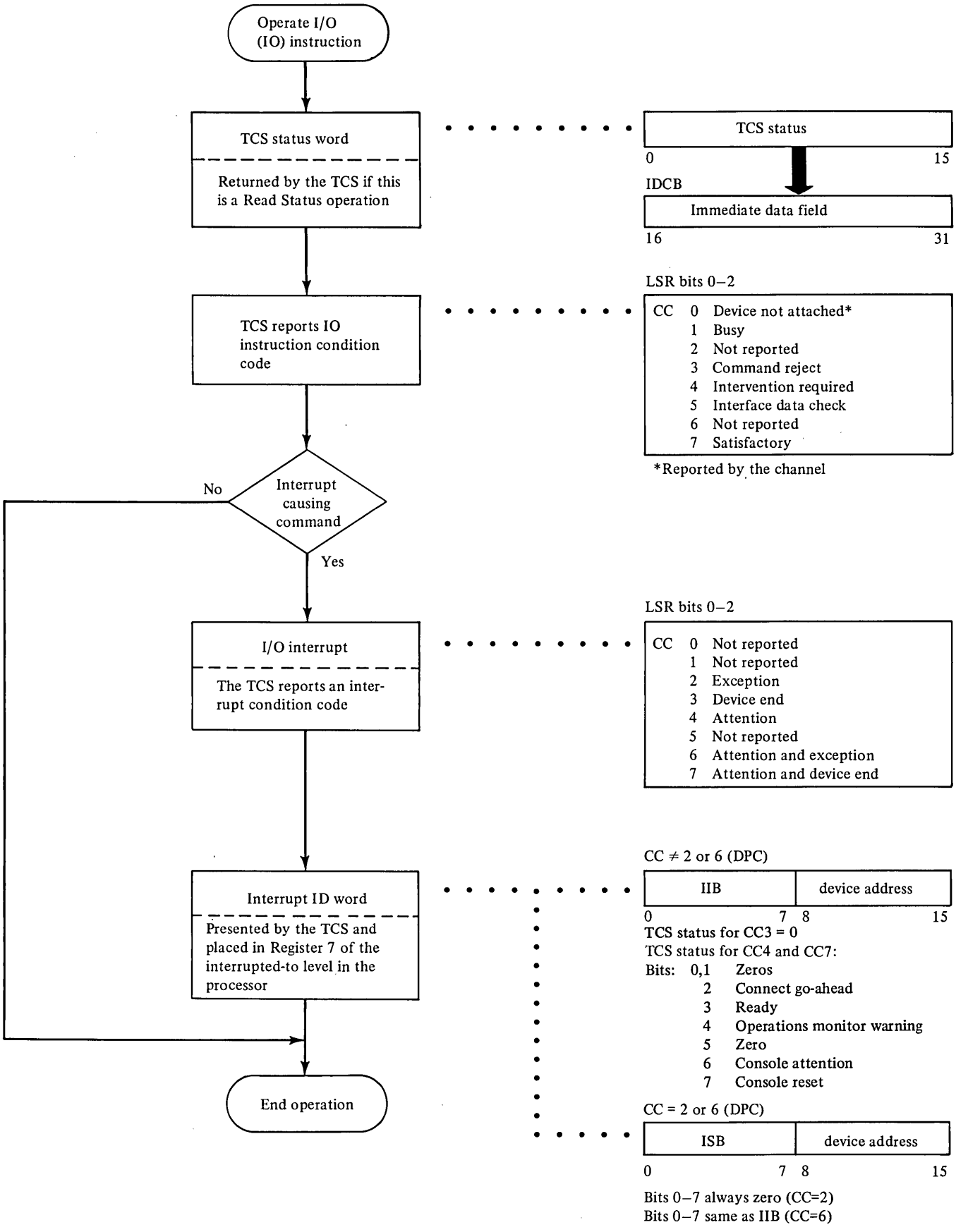


Figure 2-4. Condition codes and status sent to processor

IO Instruction Condition Codes

These condition codes (see Figure 2-5) are reported by the TCS during execution of each I/O command. The appropriate condition code is set in the even, carry, and overflow bit positions of the *level status register* (LSR) in the processor issuing the command. The condition codes are mutually exclusive and have a priority sequence. That is, beginning with CC=7 each successive condition code through CC=0 takes precedence over the previous code. For example, if the TCS cannot accept a command because it is busy, it reports CC=1, irrespective of error conditions encountered.

The meanings of the IO Condition Codes are:

CC=0 *Device not attached.* Reported by the channel if the addressed TCS is not attached.

CC=1 *Busy.* Reported by the TCS to the issuing processor:

- If the issuing processor is connected to the common I/O, this code is reported because of a busy or interrupt pending condition. Busy is reported to three commands when the operations monitor running. These commands are Start Operation Monitor, Reset and Connect, and Reserve. Interrupt pending is the result of an interrupt posted in the TCS but not accepted by the processor.
- If the issuing processor is not connected to the common I/O, this code is reported because of an attention interrupt pending condition.

CC=2 *Not reported.*

CC=3 *Command reject.* Reported by the TCS to the issuing processor if the command cannot be executed due to an improper state of the TCS or an incorrect parameter in the IDCB.

CC=4 *Intervention required.* Reported by the TCS to the issuing processor when operator or host processor intervention is required to reset a time-out condition.

CC=5 *Interface data check.* Reported by the TCS or channel when incorrect parity is detected on the I/O data bus of the issuing processor during data transfer.

CC=6 *Not reported.*

CC=7 *Satisfactory.* Reported by the TCS to the issuing processor when the TCS accepts the command.

	Condition code (CC) values							
Commands	*CC0*	*CC1*	*CC2*	*CC3*	*CC4*	*CC5*	*CC6*	*CC7*
Prepare	X					X		X
Device reset	X							X
Read ID	X					X		X
Console acknowledge	X	X				X		X
Reserve	X	X		X	X	X		X
Reset and connect	X	X		X		X		X
Start operations monitor	X	X		X	X	X		X
Reset operations monitor	X							X
Read status word	X	X				X		X

CC value	*E*	*C*	*O*	*Name*
0	0	0	0	Device not attached (channel reported)
1	0	0	1	Busy
2	0	1	0	Not reported
3	0	1	1	Command reject
4	1	0	0	Intervention required
5	1	0	1	Interface data check
6	1	1	0	Not reported
7	1	1	1	Satisfactory

E = Even indicator in LSR
C = Carry indicator in LSR
O = Overflow indicator in LSR

Figure 2-5. IO Condition Code responses to I/O commands

Interrupt Condition Codes

The interrupt condition codes are reported by the TCS when commands and changing status in the TCS cause interrupts. The specified condition code is transferred into the *level status register* (LSR) of the processor during interrupt acceptance time. The interrupt condition codes are mutually exclusive with each other but *do not* have a priority sequence. The interrupt condition codes are:

CC value	*E C O*	*Name*
0	0 0 0	Not reported
1	0 0 1	Not reported
2	0 1 0	Exception
3	0 1 1	Device end
4	1 0 0	Attention
5	1 0 1	Not reported
6	1 1 0	Attention and exception
7	1 1 1	Attention and device end

E = Even indicator in LSR.
C = Carry indicator in LSR.
O = Overflow indicator in LSR.

The meanings of the interrupt condition codes are:

CC=0 *Not reported.*

CC=1 *Not reported.*

CC=2 *Exception.* The operations monitor has reached the end of the warning period and timed out while operating in normal mode.

CC=3 *Device end.* The operations monitor has reached the end of the warning period and stopped while operating in test mode.

CC=4 *Attention.* Reported when (1) the interrupt was caused by an external event (asynchronous to the program of the accepting processor) rather than execution of an Operate I/O instruction, and (2) Exception or Device End interrupts have not been posted at interrupt accept time. See "Interrupt Information Byte" in this chapter for conditions that cause an attention interrupt.

CC=5 *Not reported.*

CC=6 *Attention and exception.* The exception condition and attention condition have both been posted. No information as to what order these conditions have occurred (before interrupt acceptance time) is provided.

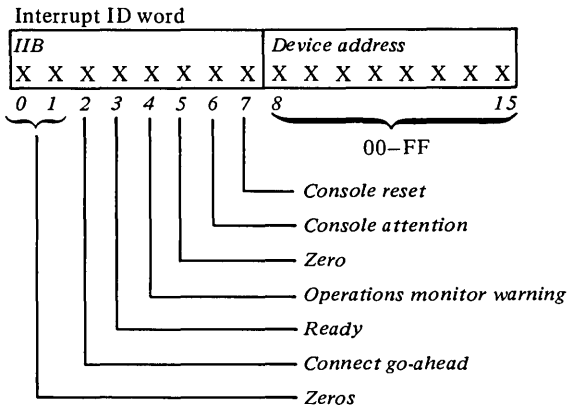
CC=7 *Attention and device end.* The attention condition and device end have both been posted. No information as to what order these conditions have occurred (before interrupt acceptance time) is provided.

Interrupt ID Word

Interrupt status information is also transferred to the processor in an interrupt ID word. The low-order byte of the interrupt ID word contains the address of the interrupting TCS; the high-order byte contains the interrupt information byte (IIB).

Interrupt Information Byte (IIB)

The IIB is used for interrupt condition codes CC3, CC4 and CC7. For CC3, the IIB is presented as zeros. For interrupt condition codes CC4 and CC7, the format and meanings of bits are:



Bit 0, 1 *Presented as zeros.*

Bit 2 *Connect go-ahead.* This bit set to 1 indicates that the other processor has incurred a time-out of the operations monitor. This reflects the setting of bit 2 in the status word. This bit is associated with a persistent interrupt (see "Persistent Interrupts").

Bit 3 *Ready.* This bit set to 1 indicates that the other processor has executed a Reserve command. This reflects the setting of bit 3 in the status word. This bit is associated with a persistent interrupt (see "Persistent Interrupts").

Bit 4 *Operations monitor warning.* This bit set to 1 indicates that the operations monitor has reached the warning point and caused an attention interrupt to the processor connected to the common I/O.

Bit 5 *Presented as zero.*

Bit 6 *Console attention.* This bit set to 1 indicates that the operator has pressed and released the Attn key on the TCS console.

Bit 7 *Console reset.* This bit set to 1 indicates that the operator has pressed and released the Reset key on the TCS console and has terminated the operator intervention mode.

Note. Bits 6 and 7 reflect interrupts to both processors.

Interrupt Status Byte (ISB)

The ISB is a special format of the interrupt information byte (IIB) and is used for CC2 and CC6. For CC2, the ISB is presented as zeros. For CC6, the meanings of bits 0–7 are the same as defined in the IIB section.

Resets

Control/register and interrupt resets are used by the TCS to ensure proper operation and proper communications between the two Series/1 processors and the TCS.

For both classes of resets, the power-on reset is brought into the TCS from the I/O expansion card file that the TCS is plugged. (Power-on reset is not brought in from either processor.) The TCS could be connected to a processor that is powered down and back up and still maintain connection to that processor and the common I/O (provided the operations monitor was not started; otherwise, a time-out could occur causing the common I/O to switch to the other processor).

Another situation could exist where both processors are powered up and the TCS powered down and back up which would cause the TCS to completely reset. For this situation, both processors would have to restart their operations with respect to the common I/O. The following paragraphs describe methods that are used to reset control/register settings and interrupt conditions. Refer to Chapter 3 for resets that occur from the TCS console.

Control/Register Resets

Figure 2-6 lists the conditions which cause the TCS to reset controls and registers. The power-on reset from the TCS I/O expansion unit affects both sides of the TCS. Any reset from one of the processors, such as, system reset, Halt I/O, Device Reset, or Reset Operations Monitor, only affects the corresponding side of TCS. The other side will remain as it was before the reset occurred; however, indications in its status word would change and residual interrupts may exist.

	Condition						
Control/register	*Power on*	*System reset*	*Halt I/O*	*Device reset*	*Reset operations monitor*	*Reset and connect*	*Read status word*
Acknowledge indicator (A/B)	X	X	X	X	--	--	--
Reserve bit 3	X	X	X	X	--	X	--
Operations monitor time-out bit incurred	X	X	--	--	--	--	--
CIO connection alert and mode alert	X	X	X	X	--	--	X
Prepare register	X	X	--	--	--	--	--
Operations monitor (timer)	X[1]	X[1]	--	X[2]	X[2]	--	--

X = Reset

[1] Causes timer to stop.

[2] Resets timer to starting/reset point but timer will continue to run.

Figure 2-6. Control/Register Resets

Interrupt Resets

Figure 2-7 lists the conditions that cause the TCS to reset pending interrupts. The power-on reset from the TCS I/O expansion unit affects both sides of the TCS.

Any reset from one of the processors, such as, system reset, Halt I/O, Device Reset, or Reset Operations Monitor, only affects the corresponding side of the TCS. All pending interrupts on that side are reset; however, upon completion of the particular reset, two conditions which are asynchronous to the reset side of the TCS are resampled (see Figure 2-7) and the interrupt conditions reposted. These two interrupts are called persistent interrupts.

Persistent Interrupts

Connect go-ahead. An operations monitor time-out has been incurred (bit 2 of the reset side's status word is set to 1) by the other processor and the processor on the reset side has not accepted the (Connect go-ahead) interrupt.

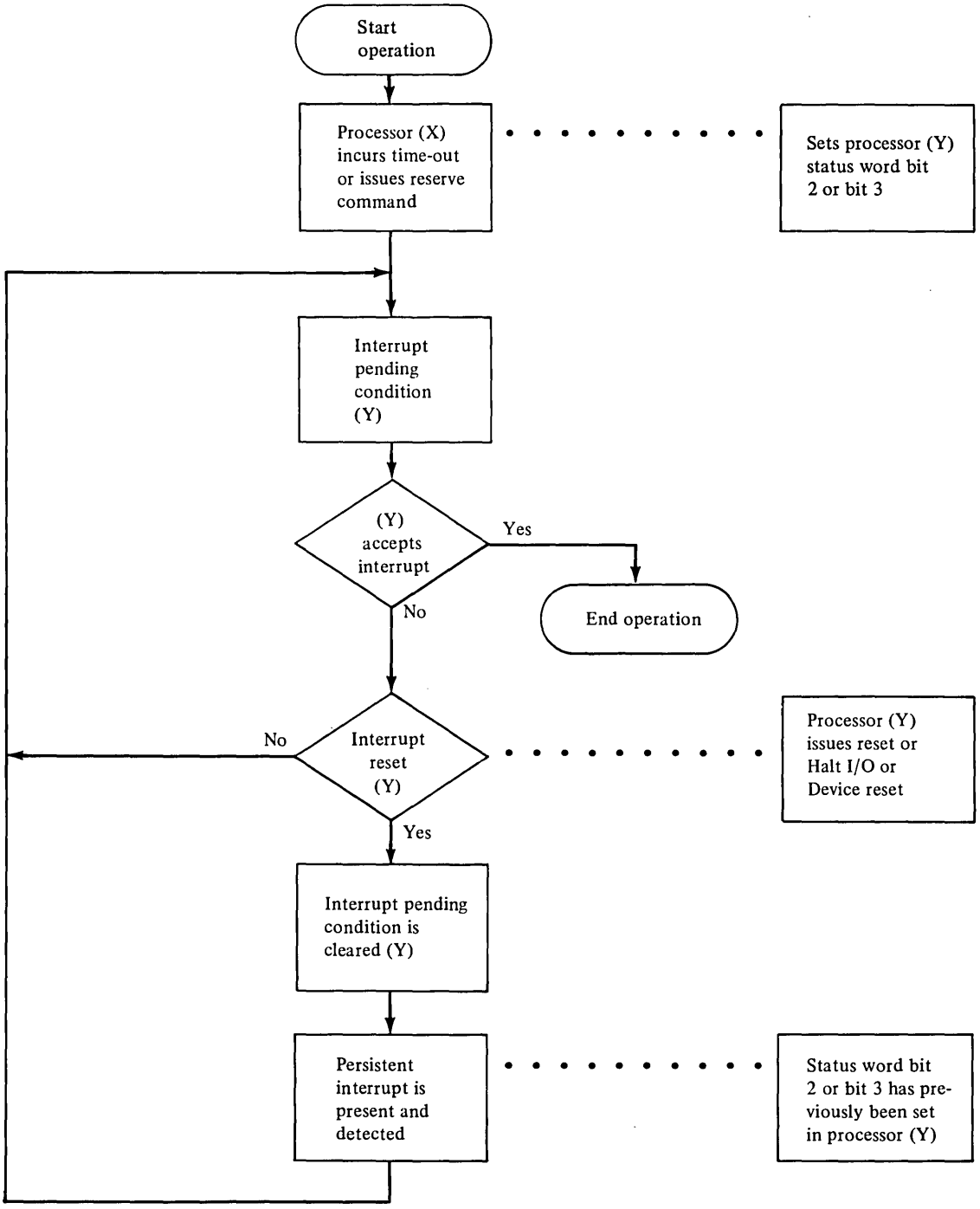
Ready. A reserve has been posted by the other processor (bit 3 of the reset side's status word is set to 1) and the processor on the reset side has not accepted the (Ready) interrupt.

The resampling of these interrupts results in an attention interrupt pending condition on the previously reset side of the TCS. Figure 2-8 illustrates the resampling and reposting of the persistent interrupts. In the example, processor (X) incurs either an operations monitor time-out or issues a Reserve command (which corresponds to the Connect go-ahead and Ready interrupts). This causes the operations monitor time-out (bit 2) or the reserve (bit 3) in the status word of processor (Y) to set to 1. These bits cannot be reset by processor (Y); therefore, they are used to determine if a persistent interrupt is present, after the interrupt pending condition was cleared (by the interrupt reset). This results in another interrupt pending condition to processor (Y) which is the previous reset side of the TCS. In this example, the persistent interrupts continue until processor (Y) accepts the interrupt which ends the interrupt reset operation.

	Condition				
Interrupt	*Power on*	*System reset*	*Halt I/O*	*Device reset*	*Reset operations monitor*
Connect go-ahead	X	X[1]	X[1]	X[1]	--
Ready	X	X[1]	X[1]	X[1]	--
Operations monitor warning	X	X	X	X	X
Device end	X	X	X	X	--
Exception	X	X	X	X	--
Console attention	X	X	X	X	--
Console reset	X	X	X	X	--

X = Reset
[1] Persistent interrupt.

Figure 2-7. Interrupt Resets



Note. For this example, it is assumed that processor (X) does not issue any resets.

Figure 2-8. Reset effects on persistent interrupts

Operations Monitor Timing

Jumpers on the TCS card are used to configure different time delays for the operations monitor initial period and the operations monitor warning period. These jumpers are configured according to customer specifications before the unit is shipped to the customer site. After the unit is installed, changes to these jumpers can be made, if desired. (See the Installation Instructions that are shipped with the unit.) The jumper configurations are indicated by status word bits 12–15 and can be read by execution of the Read Status Word command. Figure 2-9 lists the time delay settings, the jumpers ON/OFF, and the corresponding configuration of the status word bits.

Initial Program Load (IPL)

Both processors attached to the TCS can receive their IPL from a common I/O device; provided, the Initiate Initial Program Load (IIPL) blocked jumper for the respective processor *is not* installed in the TCS. These jumpers are configured according to customer specifications before the unit is shipped to the customer site. After the unit is installed, changes to these jumpers can be made; if desired. (See the Installation Instructions that are shipped with the unit.) The status of a jumper (installed or not) is indicated by bit 10 of the status word. These jumpers are independent of each other. Figure 2-10 shows the relationship between the jumpers (ON/OFF) and the corresponding setting of bit 10 of the status word for the respective processor.

The IPL function is described in the IBM Series/1 processor unit description manuals. Refer to the Preface of this manual for titles and order numbers. Also refer to "Manual IPL from a Common I/O Device" in Chapter 3 of this manual.

Period	*Setting*	*Tolerance in milliseconds* +	–	*Timing jumper 1*	*Timing jumper 2*	*Status word bits* 12	13	14	15
Initial	125 msec	125	0	ON	ON	ON	ON	X	X
	1 sec	200	0	ON	OFF	ON	OFF	X	X
	8 sec	500	0	OFF	ON	OFF	ON	X	X
	16 sec	1000	0	OFF	OFF	OFF	OFF	X	X
Warning	0 sec	0	0	ON	ON	X	X	ON	ON
	125 msec	75	75	OFF	ON	X	X	OFF	ON
	1 sec	75	75	OFF	OFF	X	X	OFF	OFF

Figure 2-9. Operations Monitor Initial/Warning Period Jumpers

Processor	*Jumper IIPL blocked*	*Status word setting*	*Remarks*
X	A(ON)	Bit 10 (ON)	IPL to processor X from common I/O device is not allowed.
X	A(OFF)	Bit 10 (OFF)	IPL to processor X from common I/O device is allowed.
Y	B(ON)	Bit 10 (ON)	IPL to processor Y from common I/O device is not allowed.
Y	B(OFF)	Bit 10 (OFF)	IPL to processor Y from common I/O device is allowed.

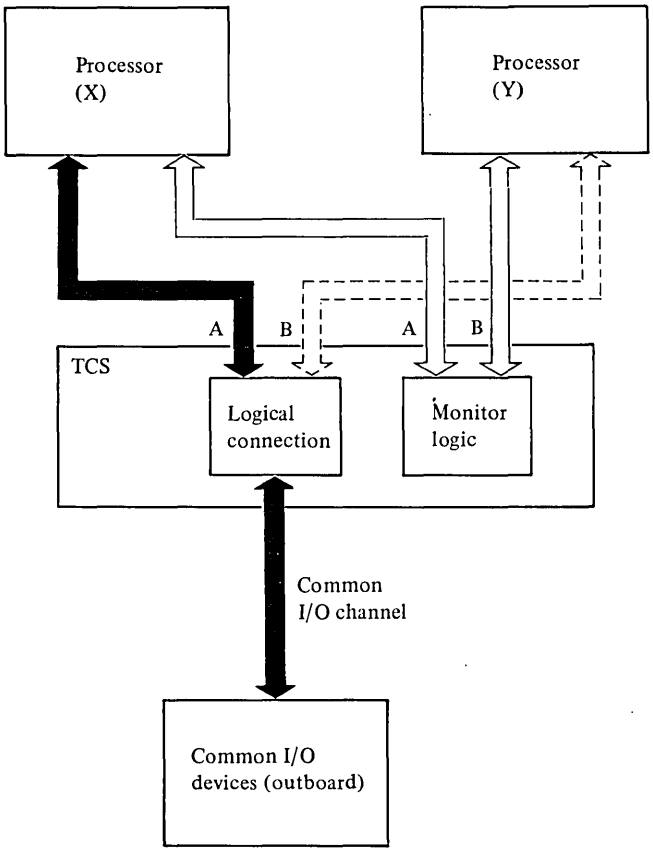
X = Processor connected to "A" side of TCS.
Y = Processor connected to "B" side of TCS.

Figure 2-10. Initiate Initial Program Load (IPL) Jumpers

Processor Switchover

The switchover process described in this section assumes that processor (X) is connected to the "A" side of the TCS and processor (Y) is connected to the "B" side of the TCS. Processor (Y) is the backup processor and obtains control of the common I/O when processor (X) incurs a time-out condition and processor (Y) issues a Reset and Connect command. In the following example, the time-out condition is caused when processor (X) fails to issue the Reset Operations Monitor command.

As shown below, processor (X) is connected to the common I/O and is processing jobs to/from its private I/O (inboard) and common I/O (outboard) devices. Processor (Y) is either in the wait state or processing jobs on its private I/O (inboard) devices.

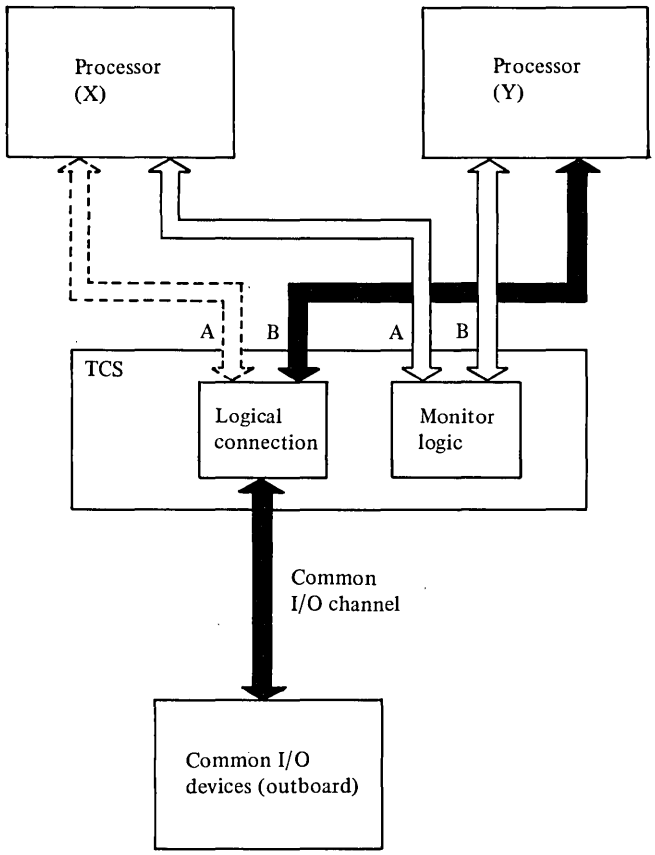


Notes.

1. Initial connection before switchover.
2. Private (inboard) devices not shown.

Both processors issue their Prepare command that provides the TCS with the capability to interrupt each processor. Processor (Y) issues a Reserve command that causes the TCS to notify processor (X) that processor (Y) is available for switchover or backup.

As shown in Figure 2-11, processor (X) issues a Start Operations Monitor command that causes the TCS to start the operations monitor. Once the operations monitor (timer) is running, processor (X) must prevent the timer from timing out by issuing the Reset Operations Monitor command. When processor (X) fails to issue the Reset Operations Monitor command, the timer will time-out. That causes the TCS to issue an exception interrupt to processor (X) and an attention interrupt to processor (Y). Processor (Y) checks the status word and determines that a time-out has occurred. Processor (Y) then issues a Reset and Connect command that resets the common I/O and connects it to processor (Y). As shown below, the switchover process is completed and the common I/O has been switched to processor (Y).



Notes.

1. Connection after time-out and switchover.
2. Private (inboard) devices not shown.

At this time, the operations monitor has timed out and cannot be restarted by processor (Y). The only way the operations monitor can be started again is by operator intervention or by processor (X) issuing a system reset and processor (Y) issuing a Start Operations Monitor command. To switchover to processor (X), intervention via the operator or a host IPL (from a host system) is required. (See Chapter 3, "Operator Intervention".)

Note. A detailed description of Host IPL can be found in the IBM Series/1 processor unit description manuals. Refer to the Preface of this manual for titles and order numbers.

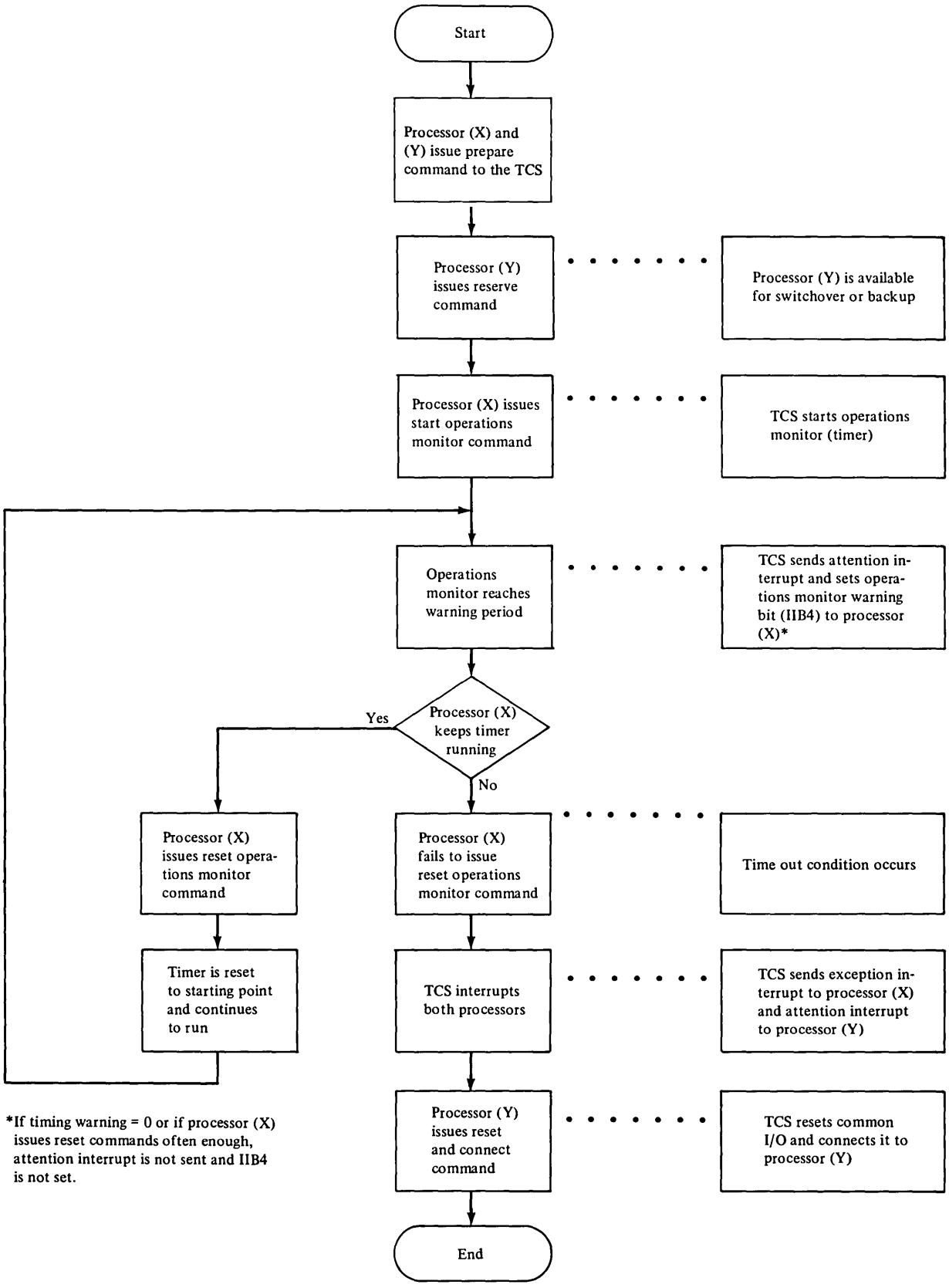


Figure 2-11. Program Control Switchover

Chapter 3. Console

Before using the TCS console, the operator must have a good understanding of the controls and indicators and must be familiar with the operating procedures described in this chapter.

The TCS console allows an operator:

- To select the manual or automatic control mode of operation
- To select the TCS side (A or B) and its associated Series/1 processor that is to be connected to the common I/O
- To interrupt the Series/1 processors and indicate (via status bits) that operator intervention is occurring
- To manually switch the common I/O from one Series/1 processor to the other
- To reset a time-out condition
- To assist in returning the system to normal operation

Note. Manual control mode means that the TCS is in manual mode caused by operator intervention. Automatic control mode means that the TCS is operating under processor control.

This chapter describes the TCS console's controls and indicators and provides general operator intervention information (also see *IBM Series/1 Operator's Guide*, GA34-0039).

Controls and Indicators

All controls and indicators are located on the front panel of the TCS I/O expansion unit and are described in the following sections. Each description is keyed to Figure 3-1 for reference.

A Power On/Off

When this switch is placed in the On position, power is applied to the TCS I/O expansion unit. After all power levels are up, the Power On indicator is turned on. When this switch is placed in the Off position, power is removed from the TCS I/O expansion unit and the Power On indicator is turned off.

B Select

When this switch is placed in the A position and the Mode switch is set to Manual, the "A" side of the TCS is selected, then when the Reset key is pressed the "A" side is connected to the common I/O. When placed in the B position and the Mode switch is set to Manual, the "B" side of the TCS is selected, then when the Reset key is pressed the "B" side is connected to the common I/O.

C Mode

When this switch is placed in the Auto position, the automatic mode is selected and the TCS is under processor control. In this mode, the operations monitor timer is under control of the processors and switchover is under control of operations monitor time-out. When this switch is placed in the Manual position, the manual mode is selected. In this mode, the operations monitor timer is held in the reset state and the operator can switch the common I/O to the "A" or "B" side of the TCS via the Select switch.

D Attn

When this key is pressed, the AckA/AckB indicators are turned OFF. When released, a console attention interrupt is posted to both processors. Status word bits 8 and 9 are posted. (See "Read Status Word Command" in Chapter 2.) This key is used with the Select and Mode switches to notify the processor of impending operator action in manual mode or to request processor action/responses in automatic mode.

E Reset

When this key is pressed, the AckA/AckB indicators are turned OFF, the operations monitor is reset and stopped, status bits 2 and 5 are set to 0 and the TCS is placed in operator intervention mode. (While the Reset key is held down, the entire TCS is in an interrupt pending condition.) In addition, this key enables the functions selected by the Select and Mode switches.

When the Reset key is released, a console attention interrupt is posted to both processors.

Note. When the Reset key is pressed while manually switching, the common I/O is reset. I/O checks may occur if the I/O channels are not quiesce (every I/O channel is in the inactive state).

F AckA/AckB

The appropriate AckA/AckB indicator is turned ON by execution of a Console Acknowledge command from the processor on the "A" or "B" side of the TCS. The AckA/AckB indicator is turned OFF by a

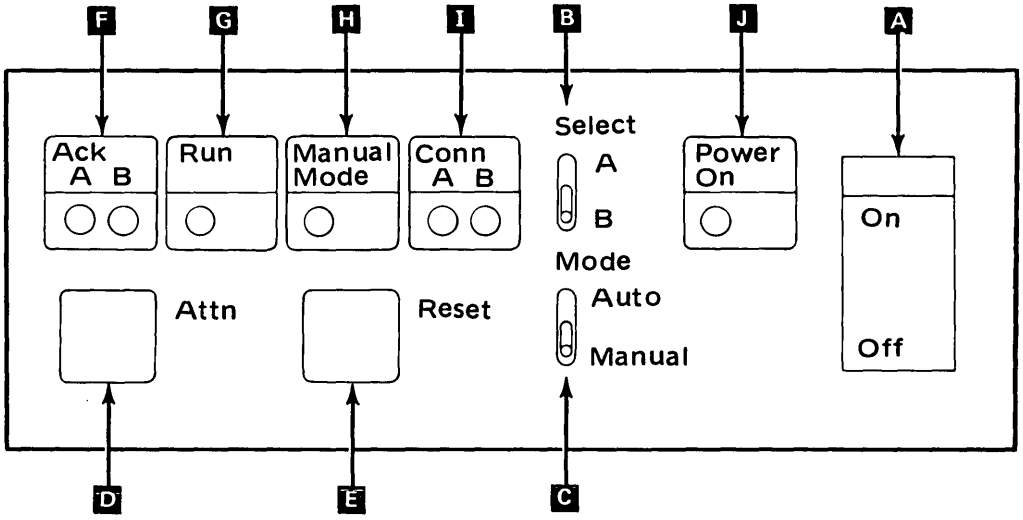


Figure 3-1. TCS Console Controls and Indicators.

device reset, system reset, or Halt I/O issued from the corresponding processor on the "A" or "B" side of the TCS. Both indicators are turned OFF when either the Attn or Reset key is pressed.

G Run

When the operations monitor is running, this indicator is turned ON. When the operations monitor is stopped, reset, or incurs a time-out, this indicator is turned OFF.

H Manual

When the manual mode is in effect, this indicator is turned ON. When the automatic mode is in effect, this indicator is turned OFF.

I ConnA/ConnB

The appropriate ConnA/ConnB indicator is turned ON when the corresponding processor on the "A" or "B" side of the TCS is connected to the common I/O (and operations monitor). When one of these indicators is blinking, an operations monitor time-out has occurred on the corresponding processor. In automatic mode, pressing the Reset key will not turn off an indicator that is on, but will turn off an indicator that is blinking. In manual mode the ConnA/ConnB indicator setting is determined by the SelectA/SelectB switch setting when the Reset key is pressed.

J Power On

When the proper power levels are available to the TCS I/O expansion card file, this indicator is turned ON. When they are not available, it is turned OFF.

Operator Intervention

A general description of operator intervention follows. For additional descriptions of operator procedures, refer to the *IBM Series/1 Operator's Guide*, GA34-0039.

Initial Connection

To establish the initial connection during power-up, the operator places the Select and Mode switches in the desired position and then places the Power On switch to the ON position.

Manual Switchover

To switch the common I/O from one processor to the other, the operator:

1. Selects manual mode (places the Mode switch to Manual position)
2. Selects the interface connection (places the Select switch to the desired position, A/B)
3. Presses the Reset key (causes TCS to enter operator intervention mode, reset and switch the common I/O) and releases the Reset key (causes the TCS to exit operator intervention mode and posts attention interrupts to both processors)
4. Selects automatic mode (places the Mode switch to Auto position)
5. Presses and releases the Reset key (completes the switchover process)

Notes.

1. When the TCS is in manual mode, the timer is held in a reset state and the TCS does not post interrupts except those caused by manual operations.
2. The operator may press the Attn key before pressing the Reset key (step 3) to allow additional time for each processor to quiesce its I/O channel (every I/O device in the inactive state).
3. The Reset and Attn keys are not interlocked; therefore, care should be taken to press each key individually. If these keys are pressed simultaneously, unpredictable results can occur.
4. A mode change from automatic to manual *without* common I/O switchover allows the operator to lock the common I/O onto the processor that is connected. In manual mode, ready and connect go-ahead interrupts *are not* presented from one processor to the other.

Manual Interrupts

The operator notifies or alerts the program of impending operator action (in manual mode) or requests program responses (in automatic mode) by using the Attn key. When the Attn key is released, a console attention condition (causes an attention interrupt) and status word bits 8 and 9 are posted to both processors. (See "Read Status Word" command in Chapter 2.) The Select and Mode switch settings can then be interpreted by the program as a notification of operator intentions.

The operator notifies the program that operator intervention is completed by pressing the Reset key. When released, a *console reset* condition (causes an attention interrupt) is posted to both processors and status word bits 8 and 9 of both processors are reset, if they were set.

Manual Resets

The TCS can be completely reset by the operator pressing the Reset key on the operator console; however, residual interrupts may be presented to either processor because of the asynchronous nature of operator intervention (with respect to either processor).

Pending interrupts to the processors *will not* be reset when the Reset key is pressed; although, the conditions that caused some interrupts are reset (i.e., operations monitor conditions or a reserve posted). The following conditions can occur when the Reset key is pressed and released:

- AckA/AckB indicators are turned OFF.
- *Operations monitor time-out* bit (status word bit 2) is set to 0.
- *Reserve* bit (status word bit 3) is set to 0.
- *Operations monitor time-out incurred* bit (status word bit 5) is set to 0.
- *CIO connect alert* bit (status word bit 8) and *control mode alert* bit (status word bit 9) are set to 0.
- Operations monitor is reset and stopped.

Note. The attention interrupts (console attention and console reset conditions) caused by operator intervention *cannot* be reset from the TCS console. They are reset by: a power on reset from the TCS I/O expansion card file, a system reset, a Halt I/O, or a Device Reset from the processors.

Manual IPL from a Common I/O Device

The operator can IPL either or both processors from a common I/O device as long as the IIPL blocked jumpers *are not* installed (refer to "Initial Program Load" in Chapter 2) and the device is designated as an IPL device.

To IPL the processors, the operator:

1. Selects one of the processors (see "Manual Switchover" in this chapter)
2 IPL's the selected processor.
3. Repeats steps 1 and 2 for the other processor when the Reset key is pressed.

Appendix A. Reference Information

I/O Commands

Hex	*Command*	*IO instruction CCs reported*
20	Read ID	0,5,7
23	Read Status Word	0,1,5,7
50	Console Acknowledge	0,1,5,7
53	Reserve	0,1,3,4,5,7
60	Prepare	0,5,7
63	Reset and Connect	0,1,3,5,7
66	Start Operations Monitor	0,1,3,4,5,7
6C	Reset Operations Monitor	0,7
6F	Device Reset	0,7

Device Status Word

Bit	*Meaning*
0	CIO connected
1	Control mode in effect
2	Operations monitor time-out
3	Reserve
4	Operations monitor run
5	Operations monitor time-out incurred
6,7	Zeros
8	CIO connection alert
9	Control mode alert
10	IIPL blocked
11	Polarity
12,13	Operations monitor initial period
14,15	Operations monitor warning period

Interrupt Condition Codes Reported

CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	*IIB contents*
2	DPC interrupt status byte (always zero)
3	Always zero
4	Bits 0,1 always zero Bit 2 Connect go-ahead Bit 3 Ready Bit 4 Operations monitor warning Bit 5 Always zero Bit 6 Console attention Bit 7 Console reset
6	DPC interrupt status byte Bits 0,1 always zero Bit 2 Connect go-ahead Bit 3 Ready Bit 4 Operations monitor warning Bit 5 Always zero Bit 6 Console attention Bit 7 Console reset
7	Same as CC4

Customer Output Alarm Relay Contact

An output contact is provided on the TCS console card to allow a user to connect an external alarm device. (See Figure 1-2 in Chapter 1.) If desired, the user can install the external alarm device so that an audible sound can be used to indicate a processor exception condition. The alarm relay (in the TCS) is activated by an operations monitor time-out that sets bit 5 of the connected processor's status word to 1. This condition indicates a processor exception condition.

Note. The external alarm device *is not* included with the TCS feature and *is* supplied by the user.

The electrical specifications for the alarm relay contacts are:

- 12 Vdc, 300 ma resistive or 24 Vdc, 150 ma resistive
- Terminated with the connector shipped with the TCS feature. (See the Installation Instructions that are shipped with the unit.)

CAUTION: If the user's external alarm device is electrically inductive, an appropriate arc suppression network should be used to protect the relay contacts; otherwise, damage to the contacts can occur.

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