

7090/7094 DATA PROCESSING SYSTEMS

IBM 7320 DRUM STORAGE

The IBM 7320 Drum Storage (Figure 1) provides IBM 7090 and 7094 Data Processing Systems with reduced access time, increased data channel utilization, and higher transmission rates to and from randomly stored data. When used in an IBM random-access storage subsystem, consisting of IBM 7320 Drum Storage units and IBM 1301 Disk Storage units, the 7320 permits expanded programming versatility, reduced system loading time, and increased operational efficiency. With its associated IBM 7631 File Control* (Figure 2), the 7320 contributes the following functions and applications to 7090/7094 random storage operations:

Program and Table Storage
Systems Programs--IBSYS Basic Monitor,
IBJOB Processor, and so on.

*(Serial 12000 and higher)

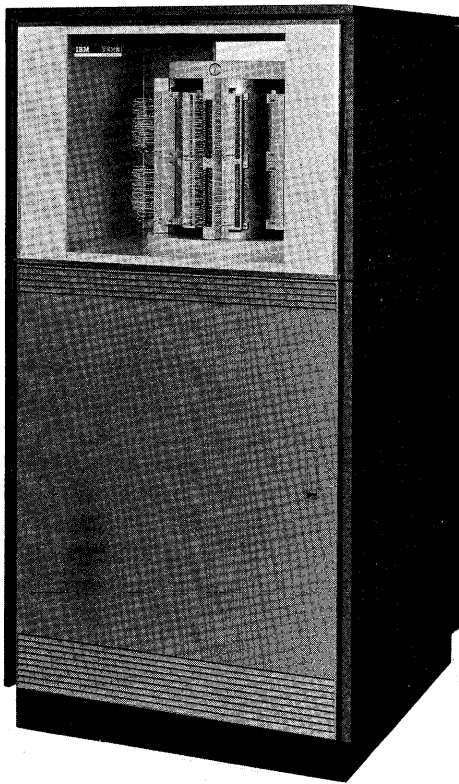


Figure 1. IBM 7320 Drum Storage

Operational Programs--Subroutines, monitors,
and control programs.

Reference Table Storage--Mathematical func-
tions and matrices.

Indexing Applications for Larger Capacity Random-
Access Storage Units

High Activity, Low Volume Random Access Storage
Temporary storage of master records
Real-time data collection operations

Intermediate Storage

Memory extension for large problems, problem
solutions, and so on
Program interrupts

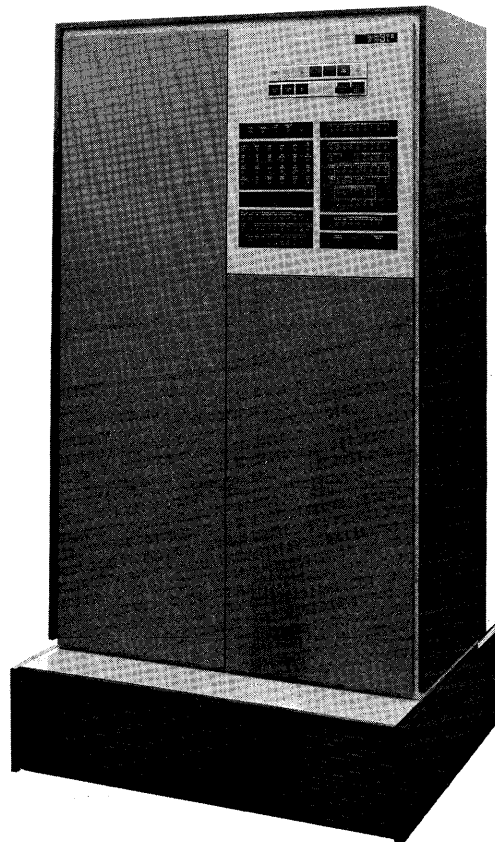


Figure 2. IBM 7631 File Control

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The 7320 provides random storage of 1,118,400 characters on 400 data tracks. In the normal six-bit data mode of the 7090/7094 systems, each data track provides bit and character capacities, for the recording of data as follows:

Data Bits	16,776
Characters	2,796 (6 bit)
Words	466 (36 bit)

For 7090/7094 operation, the 7631 File Control is available in one model, which provides the following services to the random-access storage subsystems:

Facilities for 7090/7094 system to locate and address blocks of data located in the 7320 or 1301 storage units.

Data transfer between the 7090/7094 system and the 7320/1301 random-access storage units.

Data can be transmitted in three ways: single record, full track, or cylinder mode.

File status information to the 7090/7094 systems, on command. Decoding and execution of system-coded orders for random-access storage subsystems.

The 7631 provides for connection of five random-access storage units. These units may be either 7320 Drum Storage or 1301 Disk Storage units and may be used in any combination, up to the five-unit limit for the system. Two 7631 File Controls may be used, but the limit of five random-access storage units still applies. See Figure 3.

DRUM STORAGE RECORDING

The 7320 Drum Storage consists of a vertically mounted drum--coated with a magnetic recording material--and its associated electronic circuitry. The drum rotates at a nominal speed of 3,490 revolutions per minute and is divided into 449 separate tracks (Figure 4):

- 400 Data Tracks
- 40 Alternate Tracks (may be substituted for regular data tracks by the customer engineer)
- 1 Clock Track
- 1 Format Track
- 7 Alternate Clock or Format Tracks

Each data track has its own read/write element, which is capable of recording and retrieving data. Because of the assignment of a read/write element to each data track, no access delay is encountered in seeking an addressed track. Rotational delay, required to locate the specific data record on the data track, averages 8.6 milliseconds.

The data read/write elements are mounted on 20 vertical racks that surround the drum. Special read/write heads are used with the pre-recorded

clock tracks and the program recorded and controlled format tracks.

The read/write elements contain tiny coil-wrapped magnetic cores. During writing operations, the cores convert electrical current into magnetic flux to magnetize defined spots on the drum surface. During reading operations, the action is reversed; the magnetized drum surface spots generate a magnetic flux, which is converted to an electrical signal and accepted by the wire coil around the magnetic core of the read/write element.

Information, in the form of binary bits, is handled serially by bit and is transmitted in serial-by-bit mode to or from the 7631. The 7631 collects and arranges the data for parallel transmission by six-bit characters to the 7090/7094 system.

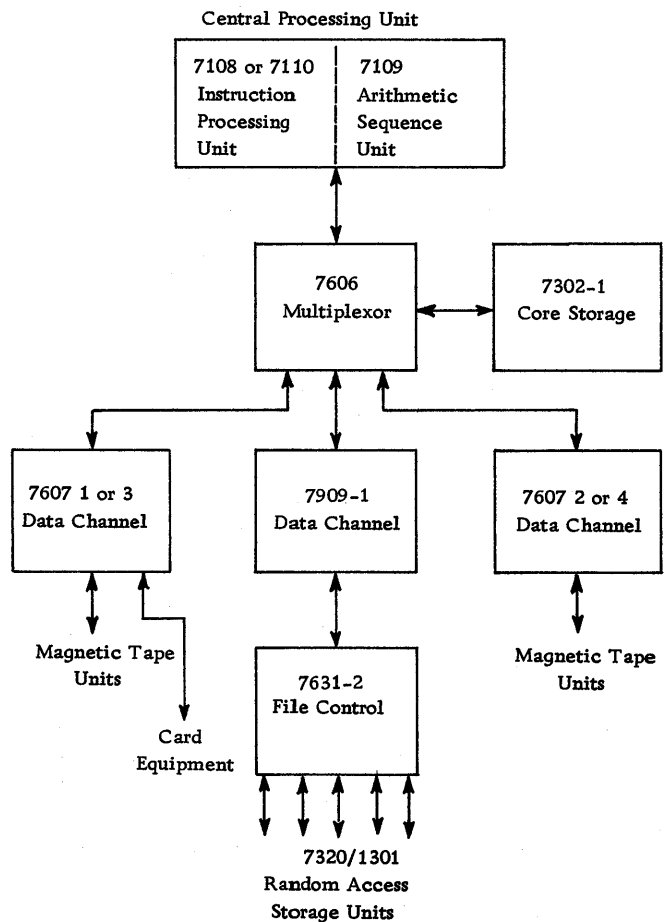
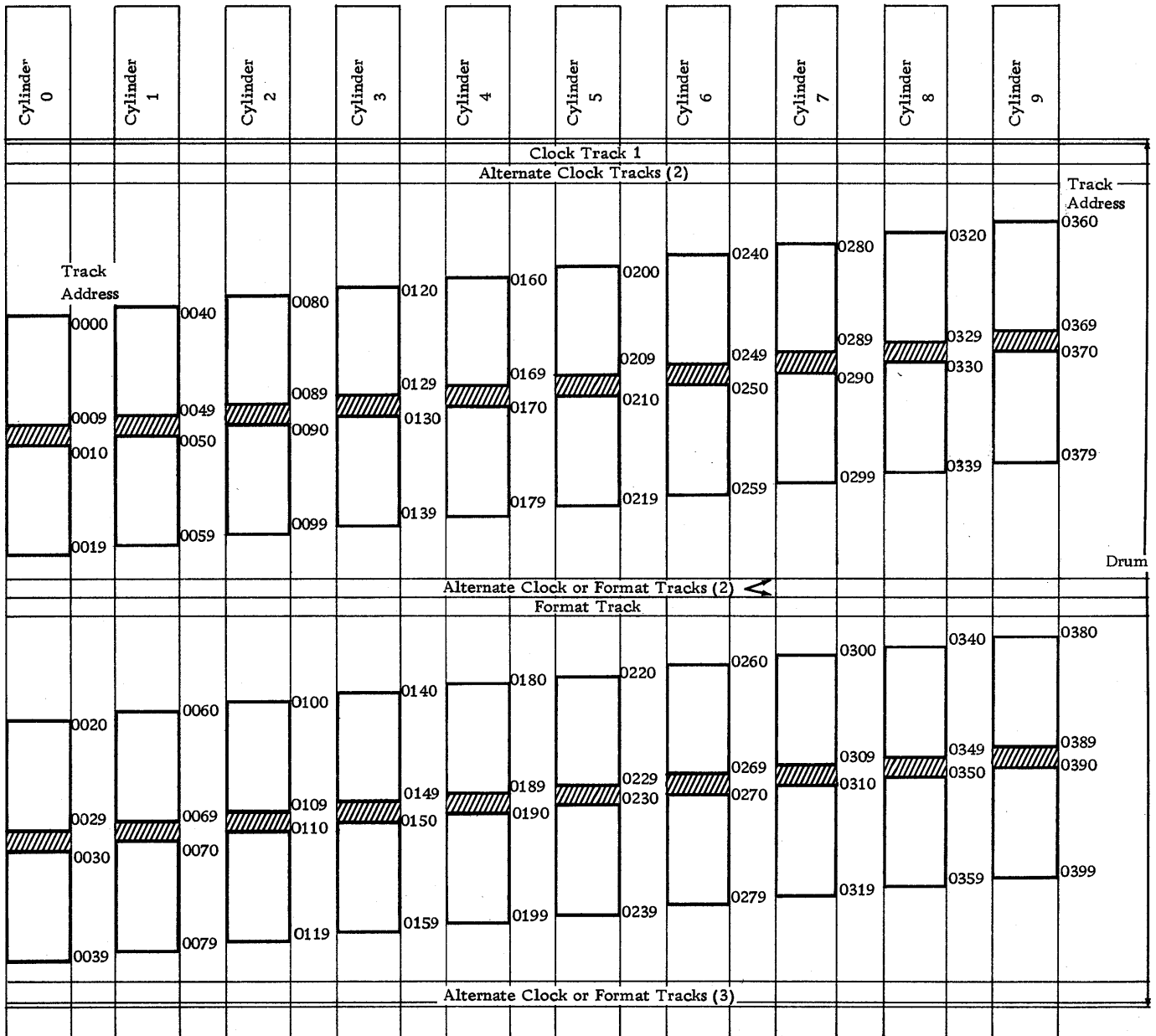


Figure 3. IBM 7090/7094 Systems with IBM 7320/1301 Random Access Storage Units



Spare Data Tracks



 2 per Rack
 4 per Cylinder

Figure 4. Track and Cylinder Layout, IBM 7320 Drum Storage

Recording and retrieval of 7320 data is at a nominal rate of 1,216,900 bits per second or 202,800 (202.8KC) characters per second for six-bit mode, and has a weight factor per channel of 43.0 for 7090 operation and 25.0 for 7094 operation. See IBM 7090 Data Processing System Reference Manual, Form A22-6528, or IBM 7094 Data Processing Reference Manual, Form A22-6703, for explanation of channel weight factors for other input-output components.

Data recorded on the 7320 may be read repetitively. Each time new data are recorded on the data tracks, the old data are automatically erased. The 7320 is primarily intended to provide randomly stored data of a temporary nature. Randomly stored, external data storage of more permanent disposition is provided in the IBM 1301 Disk Storage Unit (see IBM 1301 Disk Storage with IBM 7000 Series Data Processing Systems General Information Manual, Form D22-6576-2).

DATA TRACKS

Each data track (Figure 5) provides a fixed data recording area. This fixed area extends around the periphery of the drum within the confines of each track and may be used to store one record or many individual records. The complete track may not be used solely for recording data; a number of positions within each track are used for identification purposes and for distinguishing records, checking, and synchronizing.

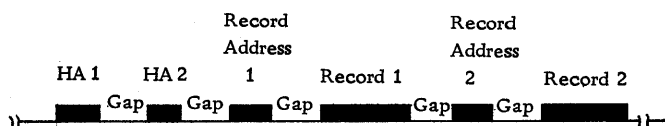


Figure 5. Drum Track Address and Data Layout

Identification Areas

Home Address 1 (HA 1) is a four-digit BCD number used to identify the physical location of any one of the 400 data tracks. Tracks are numbered from 0000 to 0399. (The high-order digit (always zero) is used for 7320/1301 compatibility and in address comparison operations.) The HA 1 area is prerecorded on each data track and cannot be written or altered by the user and is not read into or out of core storage.

Home Address 2 (HA 2) consists of two or more BCD alphanumeric digits (normally six for 7090/7094), which are assigned and written by the user. Only the first two characters are compared during address

verification operations. The HA 2 area follows the HA 1 area in each data track and is used as a home address identifier. HA 2 provides a means for the user to further define the address of each data track, and it can be written to serve any convenient purpose, such as tagging a particular category of records. HA 2 is used in full-track comparison operations but is not compared during home address operations. It is read into and out of core storage on home address operations only.

The record addresses are assigned and written by the user to fit any convenient addressing scheme. An address consists of six characters, which can be numeric, alphabetic, or special characters. Only numeric portions of the first four characters are compared during address verification operations. All bits of the fifth and sixth characters are compared during address verification operations.

Record Distinguishing Areas

Record Address (RA): The record address area precedes the data record on the data track and is used to distinguish records on the track.

Data Distinguishing, Checking, and Control: To distinguish between addresses and records, inter-record and inter-address gaps are automatically written between address and record areas, as well as between HA 1 and HA 2 areas. The gaps check characters and internal synchronization information for proper drum operation.

FORMAT TRACK

A format track provides a means of defining and monitoring the address, record, and gap areas of the data track. In the 7320, one format track serves 400 data tracks and can be written or rewritten, under program control, to permit control of the length and variations in format of data track records, in keeping with the changing needs of the user. An all "1's" (binary bit 1) pattern is written in specified areas of the format track to define the address and record portions of the data tracks. These binary 1's are interpreted by the 7631 for logical control of the read/write elements during data recording and retrieval.

To prevent unintentional erasure of the format track, a manually operated keylock switch is provided on the 7320. When the key is in the Write Format On position, the format write is under program control. When the key is in the Write Format Off position, the format track cannot be written. In either position, the format track is interpreted by the 7631, permitting a read or write data operation under control of the 7631.

Writing a Format Track

Before any data can be written on or read from a data track, the format track must be written to designate how the data track is to be allocated, identified, and used. The control characters to be used in the format track must first be organized in core storage. Programming is used to transmit the data from core storage to the addressed format track for format track recording. (Details on the actual writing of a format track are under "Write Format Track Operation").

CYLINDER MODE

Ten cylinders are provided on the 7320 Drum Storage. Each cylinder consists of 40 data tracks, which are numbered sequentially from the top to the bottom of the rotor. Cylinder mode of operation with the 7320 Drum Storage is provided by the cylinder mode optional feature in the 7631 and provides compatibility between the 7320 Drum Storage and up to ten cylinders of a 1301 Disk Storage.

IBM 7909 DATA CHANNEL

The IBM 7909 Data Channel (Figure 6) provides data transmission (synchronizing, buffering, data assembly and disassembly) as well as channel command execution between the 7090/7094 system and the 7631 File Control. Essentially, the 7909 provides the means to control quantity, destination, and format of all data transmitted between drum storage and core storage. As a stored program device, the 7909 uses its own data channel programs for the operation of the 7320/1301 random-access storage subsystem, independently of central processing unit (CPU) activity. The 7909 Data Channel is able to instruct and select the 7631 and to effect limited counting and testing operations without referring to the main system. With 7909 Data Channel programs, it is possible to perform core storage to core storage or drum storage to drum storage transmission (on the same 7909) independently of the CPU. The 7909 may also perform a limited search of information in core storage or the drum storage, again independently of the CPU.

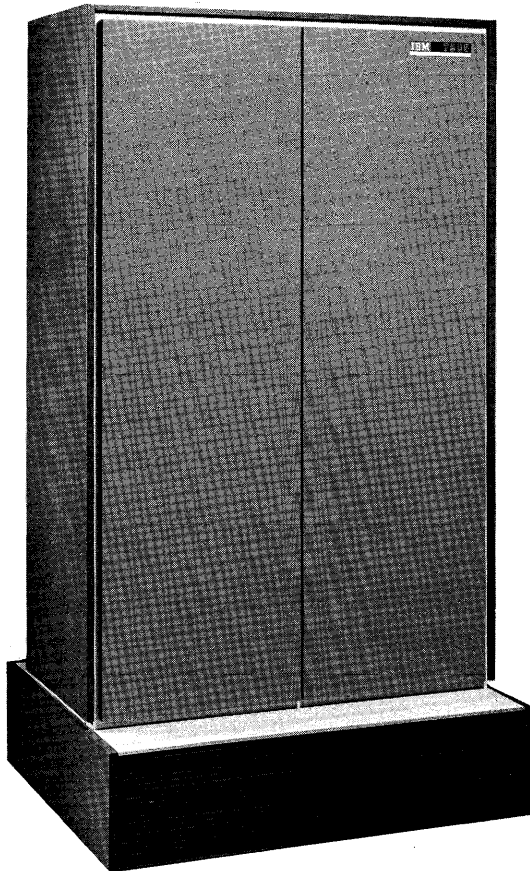


Figure 6. IBM 7909 Data Channel Unit

Although channel operation is asynchronous and independent of the CPU (except for data channel program initiation), the CPU supervises the 7909 operation. The CPU may interrogate, start, and reset the 7909 Data Channel with appropriate instructions. The 7909 may also signal the CPU of data channel activity, of total systems concern, by use of a channel trap command.

7909 DATA CHANNEL REGISTERS, SWITCHES, AND COUNTERS

Registers and data switches in the 7909 Data Channel (Figure 7) are:

Storage Bus Switches: These 36-position switches provide the data path to and from the 7606 Multiplexor for data and command entry into the 7909.

Data Register: This 36-position register serves as a buffer register for data flow between core storage and the assembly register. During a write (or control) operation, the data register is loaded with the next data word to be sent to the 7631 on a read (or sense) operation; the input data are kept in the data register until the data can be placed in core storage.

Assembly Register: This 36-position register assembles and disassembles data passing between the 7909 and the 7631.

Channel Registers: This seven-position (six data bits and a parity bit) register serves as a buffer for data passing between the assembly register and the character switches.

Channel Address Switches: This 15-position switch provides the 7606 with address information. The next word needed by the 7909 is obtained (1) by directing the address counter to the channel address switch if data are to be transmitted, or (2) from the command counter when a new command is required.

Operation and Control Registers: During a command word cycle, the storage bus switches are directed to the operation register, word counter, and address counter. Positions 8, 1, 2, 3, and 19 enter the operation register. These five bits are decoded and provide the 7909 with its next command. Positions 21-35 enter the address counter. During data operations, the address counter contains the location of the next data word. During transfer commands

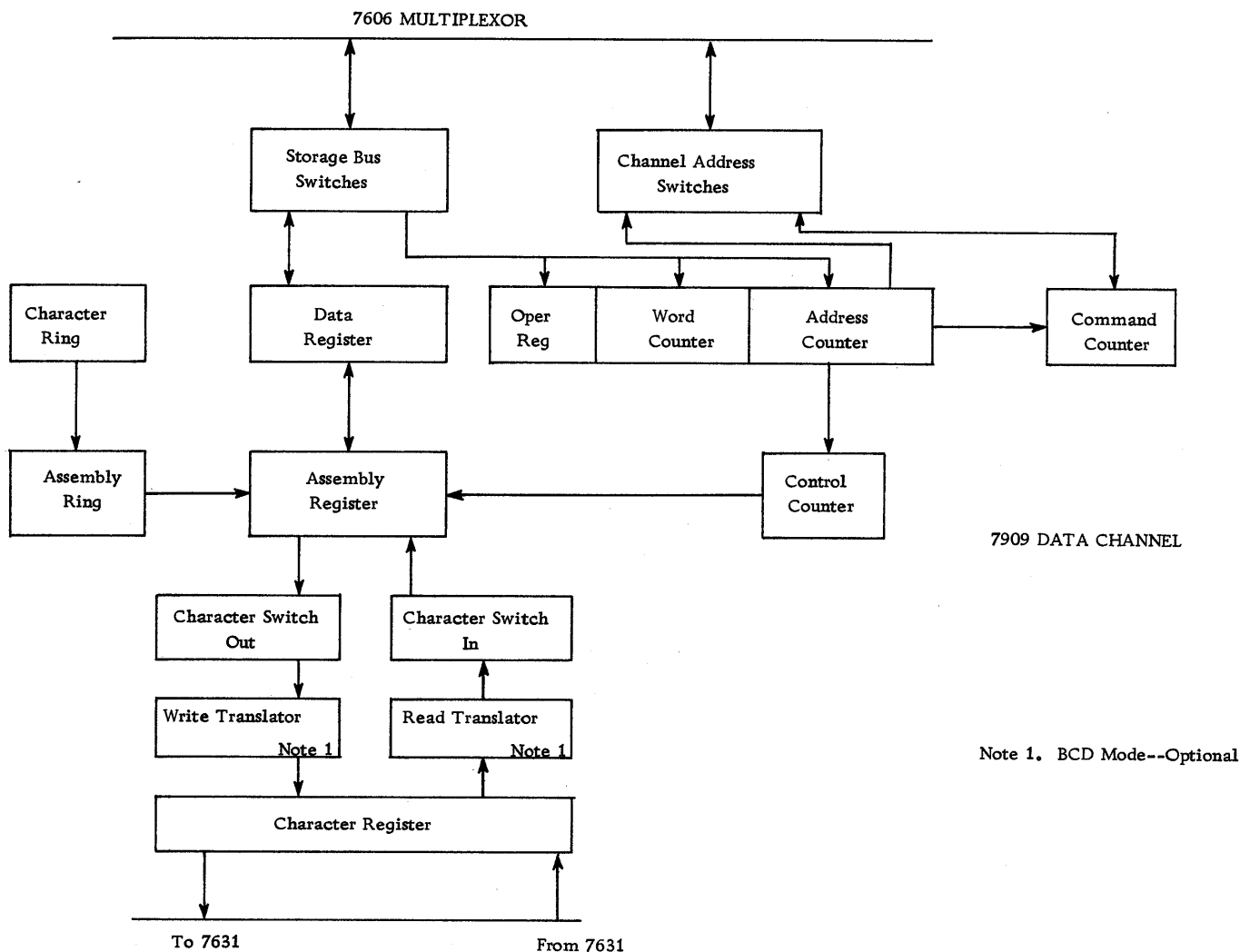


Figure 7. IBM 7909 Data Channel Data Flow

(TCM, TDC), the address counter contains the location of the next channel command. Positions 3-17 enter the word counter, which is used to control the number of words passed between the 7909 and core storage.

Command Counter: The command counter (15-positions) contains the location of the next 7909 command. The first operation performed during all command executions, except the trap and wait and wait and transfer commands, is to step the command counter to the next sequential command location. The command counter is reset and reloaded by execution of an RSC, TCH, LIP, or successful TCM or TDC command.

Character Ring: The character ring completes a cycle for each character transmitted. Its main use is to synchronize character-bit transmission.

Assembly Ring: The assembly ring serves as a character counter and passes data into or out of the assembly register. During data operations, data are sent to or received from the 7631, one 6-bit character at a time, through the character switches.

Control Counter: This six-position counter is for programming convenience. The counter contents may be changed or tested in a variety of ways as described under "IBM 7909 Data Channel Commands."

Read and Write Translators: These translators are optional and are used with the BCD optional feature. Their function is to translate characters going to or from the 7631 when operation is in BCD mode. The translators are not active during the transfer of control data.

Character Switches: These switches are used to transfer characters into and out of the six assembly register character positions.

DRUM OPERATIONS

Operations performed by the 7631 File Control, 7320 Drum Storage, and 7909 Data Channel are based on the execution of instructions, commands, and orders. Figure 8 shows simplified order format. Figure 9 shows the span of control and activity for execution of these instructions, commands, and orders in a 7090/7094 random access storage subsystem.

INSTRUCTIONS

Instructions are system-coded information that is decoded and executed by the central processing unit to perform specific operations such as the selection of data channels, resetting and loading of data channels, start data channels, and so on.

COMMANDS

Commands are systems-coded one-word "instructions" to the data channel. The commands are decoded and executed by the 7909 Data Channel to perform a specific operation in the data channel or between the data channel and the 7631 File Control.

Four basic commands are executed by the data channel and cause activity in the 7631. They are: read, write, sense, and control commands. Read and write commands set up control circuitry in the 7909 to permit information transmission between the drum storage and the main computer system through the 7631. Sense commands cause transmission of status data from the 7631 to the main computer system to indicate status conditions existing in the 7631 and the drum storage. The control command is used to transmit orders to the 7631 to supply the file control with one or more order words that contain operation and address information.

Reading and writing of drum storage data may be handled in five modes: home address operations, single address operations, track operations, track without addresses operations, and cylinder operations. Each mode causes a comparison activity, followed by a transfer of information activity (providing the comparison has been successful). The transfer activity effects transmission of data to or from the drum, according to the mode of data handling involved. The comparison is accomplished by a bit-by-bit verification of the address incorporated in the order, as received from core storage, and compared to the actual address selection of the drum storage unit. If the comparison is successful, data are transferred to or from specific areas of the drum storage unit (as determined by the mode of operation involved). If the comparison is unsuccessful,

ful, a no record found indication and an unusual-end signal are issued to the system by the 7631.

Home Address Operation: Comparing the physical home address (HA1) with the HA 1 in the order, followed by the transfer of the HA 2 plus all additional addresses and records on a given track.

Single Record Operation: Comparing the record address selected on the drum storage with the record address in the order, followed by the transfer of the associated single record only.

Track Operation: Comparing the entire home address (HA 1 and HA 2) of the selected home address on the drum storage with the home address in the order, followed by the transfer of all record addresses and records on a single track.

Track Without Addresses: Comparing the entire home address of the selected track on the drum storage with the home address in the order, followed by the transfer of all data records contained in the remainder of the track.

Cylinder Operation (Optional Feature): Comparing the entire selected home address of a particular track in a cylinder with the entire home address in the order, followed by the transfer of all records contained in the particular track and all succeeding tracks of higher address within that cylinder.

ORDERS

Orders, in the form of characters (Figure 8), are decoded and executed by the 7631 and specify what non-data operations will be performed and where they will be performed in the 7320. The orders are transmitted from core storage as one or two core

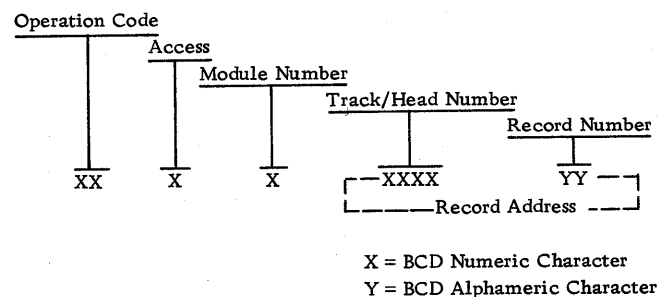
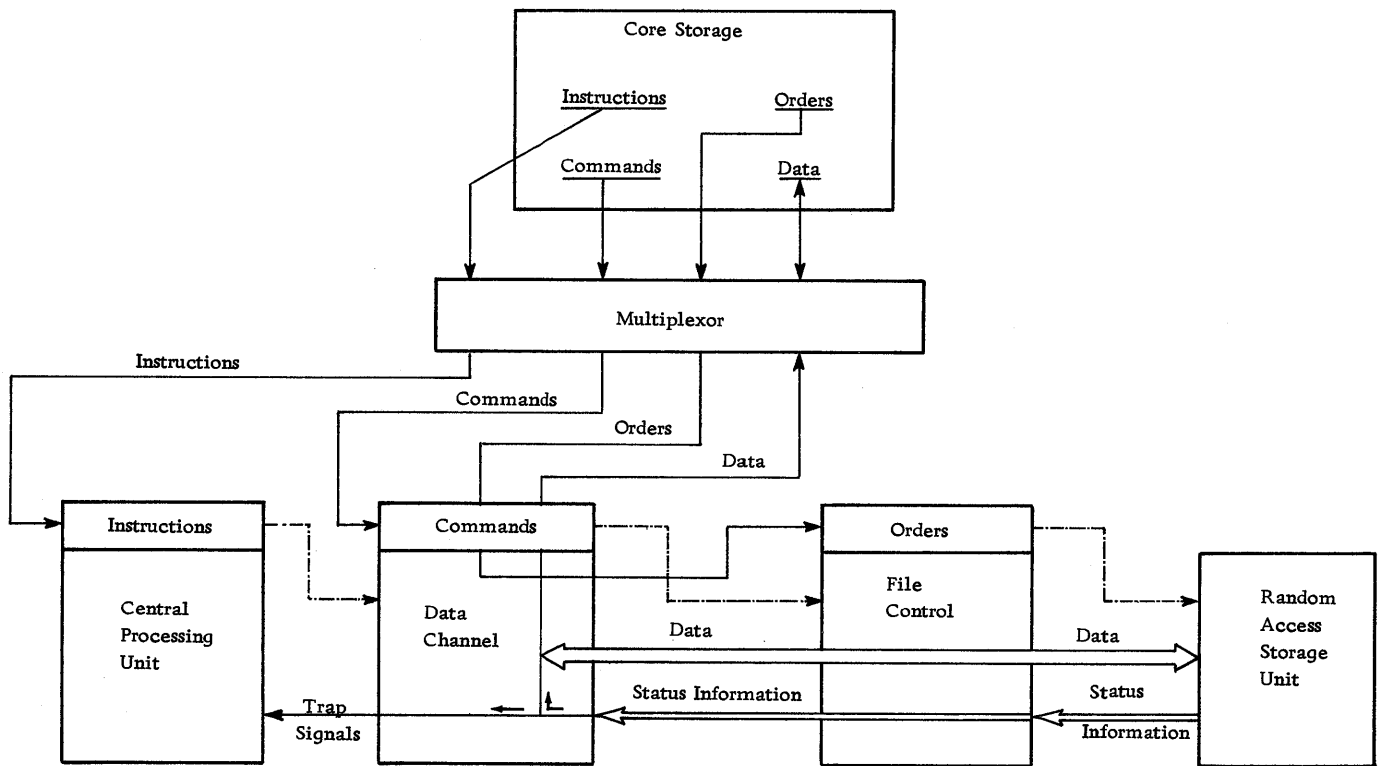


Figure 8. Simplified Order Format



Instructions

- Reset and Start Channel
- Start Channel
- Store Channel
- Enable
- Reset Channel
- Reset Channel Traps
- Store Channel Diagnostic

Commands

- Control
- Control and Read
- Control and Write
- Sense
- Wait and Transfer
- Transmit
- Transfer in Channel
- Leave Interrupt Program and Transfer
- Leave Interrupt Program
- Copy and Proceed
- Copy and Disconnect
- Trap and Wait
- Load Assembly Register
- Store Assembly Register
- Load Control Counter
- Transfer and Decrement Counter
- Insert Control Counter
- Transfer On Condition Met
- Set Mode and Select

Orders

- Disk/Drum - No Operate
- Disk/Drum - Release
- Disk - Seek
- Disk/Drum - Six-bit Mode
- Disk/Drum - Eight-bit Mode
- Disk/Drum - Prepare to Verify
- Disk/Drum - Prepare to Write Format
- Disk/Drum - Prepare to Verify (Track Without Address)
- Disk/Drum - Prepare to Verify (Track with Addresses)
- Disk/Drum - Prepare to Verify (Home Address)
- Disk/Drum - Prepare to Write Check
- Disk - Set Access Inoperative
- Disk/Drum - Cylinder Operation

----- Derived Activity

Figure 9. Span of Control-Instructions, Commands, and Orders

storage words, depending on the number of characters required in each order. Some orders require only two characters; other orders require a full complement of ten characters.

Operation Code: This is a two digit code, expressed as a BCD numeric character. The operation code is all that is required for such operations as drum/disk seek, drum/disk release, drum/disk eight-bit mode, and drum/disk six-bit mode.

Access and Module Number: These two positions of the order are always numeric. The access in a 7320 is always referred to as access 0. The module number is determined by which of the five cable connectors on the 7631 is connected to the drum storage unit:

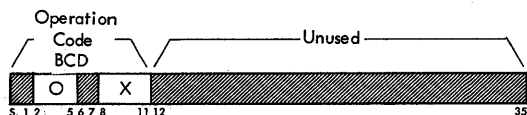
7631 Cable Connector	Drum Storage Module
First	0
Second	2
Third	4
Fourth	6
Fifth	8

Record/Home Address: The use of these character positions depends on the operation that is to be performed. In operations in which the address is not required, it is not necessary to use these positions. For operation codes that require addressing of the home address, these positions must contain the track/head number and record number. For operations affecting only a single record, these positions should contain the record address of the desired record. In a checking operation, these positions contain the home address or the record address used in the write operation to be checked.

Order Formats

Orders Using One Core Storage Word

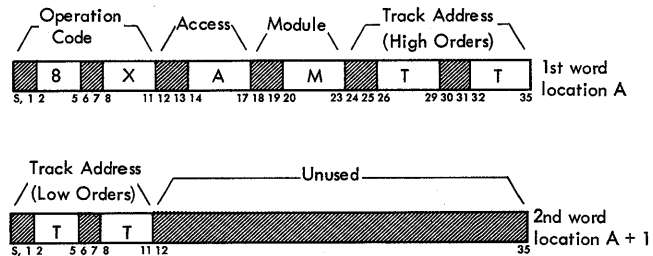
These orders require only one word of 7090/7094 storage: DNOP (00), DREL (04), DEBM (08), DSBM (09). They will assume the following format in core storage:



Orders Using Two Core Storage Words

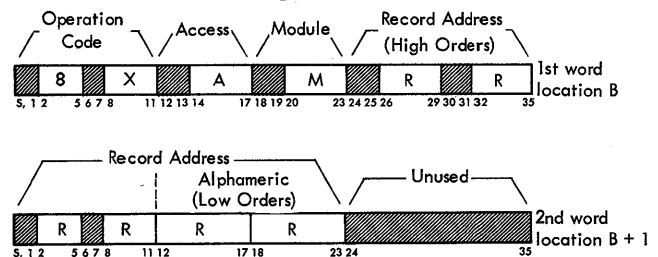
The following three groups of orders require two consecutive words of 7090/7094 storage:

Orders Requiring Eight Characters: DSEK (80), DWRF (83), DVHA (89) assume the following formats in core storage:

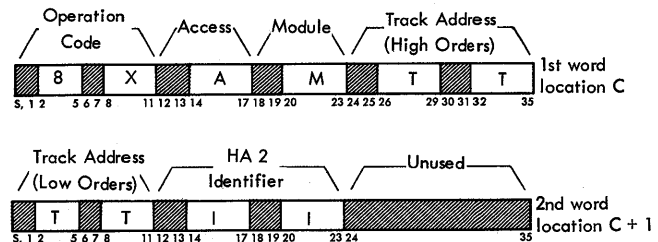


Orders Requiring Ten Characters are divided into two groups:

1. DVSR (82), DWRC (86)* assume the following formats in core storage:

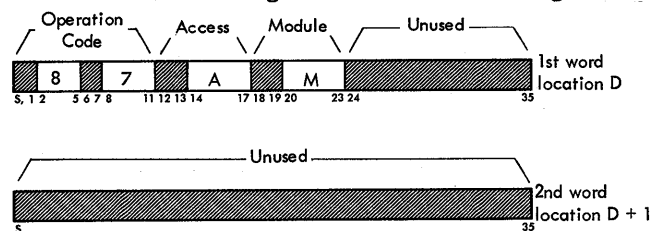


2. DVTN (84), DVTA (88), DVCY (85), DWRC (86)* assume the following formats in core storage:



Note: DWRC, write check, assumes the same format as the order that determined the mode of operation.

Orders Requiring Four Characters: DSAI (87) assumes the following formats in core storage:



The unused sections of the preceding formats are meaningless in that they are not examined by the 7631 File Control. All digits must be BCD numeric, or BCD alphameric where permitted; binary zeros are not acceptable.

The format in the following instruction descriptions and in the command descriptions in the next section uses the established formats used in the IBM 7090 Data Processing System, Reference Manual, Form A22-6528 and IBM 7094 Data Processing System Reference Manual, Form A22-6703. Execution timing is not included, because execution depends on organization of commands in storage and the status of the 7909 Data Channel when it is addressed. Symbols used are:

- C = Count Field
- F = Indirect Addressing Flag
- T = Index Register Tag
- Y = Address Field

RSCA--Reset and Start Channel A



Description: On execution of this instruction, the channel is selected and reset and takes its next command from location Y. The instruction is interlocked against channel activity; if the instruction is executed while the channel is busy, its execution is delayed until the channel is in wait status.

Indicators: None

Execution: If the selected channel is in wait status, the C(Y) S, 1-3 and 19 replace the channel operation register, C(Y) 3-17 replace the word counter, and C(Y) 21-25 replace the contents of the address counter. In addition, the number Y + 1 replaces the contents of the command counter. If the channel is not in wait status, the execution of the CPU program is delayed until the channel executes either a WTR or TWT command.

Instruction codes for other channels are:

- 0540 RSCB--Reset and Start Channel B
- +0541 RSCC--Reset and Start Channel C
- 0541 RSCD--Reset and Start Channel D
- +0542 RSCE--Reset and Start Channel E
- 0542 RSCF--Reset and Start Channel F
- +0543 RSCG--Reset and Start Channel G
- 0543 RSCH--Reset and Start Channel H

STCA--Start Channel A



Description: Execution of this instruction is delayed if the channel is not in wait status. If in wait status, the channel is started and takes its next command from the address part of the wait command.

Indicators: None

Execution: If the channel is in wait status, the command counter is reset and replaced with the contents of the address counter. The channel then executes the command at the location specified by the command counter and increments the command counter by one (adds one to the command counter contents).

Instruction codes for other channels are:

- 0544 STCB--Start Channel B
- +0545 STCC--Start Channel C
- 0545 STCD--Start Channel D
- +0546 STCE--Start Channel E
- 0546 STCF--Start Channel F
- +0547 STCG--Start Channel G
- 0547 STCH--Start Channel H

SCHA--Store Channel A



Description: Execution of this instruction causes the specified channel to be selected and that channel's command counter contents to be placed in positions 21-35 of location Y. The channel's address counter contents are placed in positions 3-17 of location Y. Positions S, 1, 2, 18, 19, and 20 of location Y are reserved, and their contents cannot be predicted.

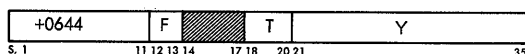
Indicators: None.

Execution: The C(Y) 21-35 are replaced by the contents of the command counter and C(Y) 3-17 are replaced by the contents of the address counter. The SCHA instruction may be executed at any time, regardless of whether the specified channel is in operation. The command counter may contain the location of the current command or of the next command to be executed.

Instruction codes for other channels are:

- 0640 SCHB--Store Channel B
- +0641 SCHC--Store Channel C
- 0641 SCHD--Store Channel D
- +0642 SCHE--Store Channel E
- 0642 SCHF--Store Channel F
- +0643 SCHG--Store Channel G
- 0643 SCHH--Store Channel H

SCDA--Store Channel Diagnostic - Channel A



Description: Execution of this instruction causes the specified channel to be selected and the specified channel's diagnostic indication to be stored in bit positions S-16 of location Y. Positions 17-35 are reserved, and their contents cannot be predicted.

<u>Channel Indicator</u>	<u>C(Y)</u>
Control Counter 1-6	S-5
I/O Check	6
Sequence Check	7
Unusual End	8
Attention 1	9
Attention 2	10
Adapter Check	11
Prepare to Read	12
Prepare to Write	13
Read Status	14
Write Status	15
Interrupt	16
Reserved	17-35

Indicators: None.

Execution: The (Y) S-16 are replaced by the channel indicators. The SCDA instruction may be executed at any time, whether the specified channel is in operation or not.

Instruction codes for other channels are:

- 0644 SCDB--Diagnostic Store Channel B
- +0645 SCDC--Diagnostic Store Channel C
- 0645 SCDD--Diagnostic Store Channel D
- +0646 SCDE--Diagnostic Store Channel E
- 0646 SCDF--Diagnostic Store Channel F
- +0647 SCDG--Diagnostic Store Channel G
- 0647 SCDH--Diagnostic Store Channel H

ENB--Enable from Y



Description: When this instruction is executed, the contents of location Y determine which signals may cause a trap operation. Execution of each enable instruction cancels the effect of previous enable instructions. The channel may be disabled (traps will not occur) by executing an enable instruction whose operand contains a zero in the proper position.

Indicators: None.

Execution: Trapping signals are controlled as follows:

<u>Signal Due to Control Word</u>	<u>Channel</u>	<u>Effective if a 1 in Position</u>
	A	0035
	B	0034
	C	0033
	D	0032
	E	0031
	F	0030
	G	0029
	H	0028

Execution of a trap inhibits all further traps until a new enable instruction is executed or a restore channel traps instruction is executed. Depression of the reset or clear key or execution of an RIC instruction also disables the data channel.

RICA--Reset Channel A



Description: This instruction, when executed, causes all conditions in the channel to be reset. The instruction is not interlocked against channel activity. If data transmission is taking place when an RIC occurs, validity of the data already transmitted cannot be guaranteed.

Indicators: None.

Execution: The RIC resets all conditions in the channel to normal initial status and also sends a reset pulse to the 7631 File Control. Modification of the address of the RIC may change the operation itself.

Instruction codes for the other channels are:

- +0760- 2350 RICB--Reset Channel B
- +0760- 3350 RICC--Reset Channel C
- +0760- 4350 RICD--Reset Channel D
- +0760- 5350 RICE--Reset Channel E
- +0760- 6350 RICF--Reset Channel F
- +0760- 7350 RICG--Reset Channel G
- +0760-10350 RICH--Reset Channel H

OTHER CPU INSTRUCTION INFORMATION

Operation of the CPU instructions IOT, RCT, TCNx, and TCOx is compatible with operation on the IBM 7607 Data Channel.

The BTT and ETT instructions always result in a skip, because neither indicator is turned on by the 7909 Data Channel. For the same reason, the TRC and TEF instructions never result in a transfer.

An RDC addressed to a 7909 Data Channel has no effect. Data select instructions (RDS and WRD) or non-data select instructions (BSR, BSF, WEF, REW, RUN, and SDN) addressed to a 7909 cause the 7909/7094 CPU to halt processing but have no effect on the 7909 Data Channel.

INTERRUPT

The 7909 Data Channel is capable of interrupting its stored program independently of the main computer and other data channels. This operation is separate and distinct from a data channel trap, which interrupts the CPU. On recognition of an interrupt condition, the 7909 channel stores the contents of the command and address counters in a fixed location and then executes the command located in another fixed location. This process is termed interrupt. When a 7909 Data Channel is attached to a 7090/7094 system, the channel tape check indicator for that channel (located on the IBM 7151 Console Control Unit) is used to display the status of the 7909 interrupt indicator.

If the 7909 channel is to be diverted from normal command execution sequence, the command in the fixed location must be one that will change the contents of the command counter (TCH, LIPT, or successful TDC or TCM). If this command is other than a successful transfer, the channel executes it and resumes operation at the location specified by adding one (1) to the value of the command counter as stored at the fixed interrupt locations. If the command at the second fixed location is a WTR or TWT, the channel suspends operation as described under "IBM 7909 Data Channel Command," but the command counter contains the same location that was stored when the interrupt occurred. If the interrupt occurred during the WTR command, the stored command counter is the location of the WTR command. If the interrupt occurred during any other command, the stored command counter is the location plus one (+1) of that command. The channel interrupt locations are assigned as follows:

<u>Channel</u>	<u>Store Command Counter At</u>	<u>Obtain Next Command From</u>
A	00042	00043
B	00044	00045
C	00046	00047
D	00050	00051
E	00052	00053
F	00054	00055
G	00056	00057
H	00060	00061

When the 7909 interrupts, the command and address counters are automatically stored in the assigned fixed core storage location. The address counter is

stored in positions 3-17 and the command counter in positions 21-35 of this location. If the contents of the fixed storage location for the address counter and command counter are modified by the program, care should be exercised to insure that positions S, 1, 2, 18, 19, or 20 do not contain bits; otherwise a halt in processing may occur when the 7909 executes an LIP command.

Interrupt conditions are stored in a six-position register in the data channel and may be examined with the TCM command. Any combination of interrupt conditions causes an interrupt; however, once interrupted, the channel is placed in interrupt mode and further attempts to set the interrupt condition or to interrupt are inhibited. The channel remains in interrupt mode until an LIP or LIPT command is executed by the channel or an RIC instruction is executed by the CPU. If a channel is in interrupt mode and an RSC instruction is executed by the CPU before the channel executes a LIP or LIPT command, the interrupt condition register is reset but the channel remains in interrupt mode. An LIP or LIPT command or an RIC instruction is the only program means available to cause the channel to exit from interrupt mode and become receptive to further interrupt conditions.

Interrupts are also inhibited if channel trap is in process on that channel. This inhibiting persists until either an RSC or STC instruction (depending on whether the channel was enabled) is executed by the CPU (see "TWT Descriptions").

Interrupt Conditions

Interrupt indications are stored in a six-position register in the data channel. The contents of this register may be examined by the TCM command. The positions of the register and the conditions they reflect are:

<u>Position</u>	<u>Condition</u>
1	Input-Output Check
2	Sequence Check
3	Unusual End
4	Attention 1
5	Attention 2
6	Adapter Check

Input-Output (I-O) Check

This condition occurs when the channel fails to obtain a storage reference cycle in time to satisfy demands of the attached I-O device. The condition is also monitored in the CPU and reflected by the I-O check light. The condition of the light may be tested by the CPU, using the IOT instruction. The input-output test (IOT) instruction execution turns the I-O check

light off in the CPU but will not affect the 7909 I-O check indicator. The channel I-O check indicator is turned off when an LIP or LIPT command is executed or when the CPU executes an RSC or RIC instruction.

The channel I-O check indicator being on indicates one of the following conditions:

1. During a write or control operation, the channel data register has not been loaded with a word from core storage by the time its contents are to be sent to the 7631.

2. During a read or sense operation, the channel data register has not been stored by the time new data are completely assembled in the assembly register.

When an I-O channel check occurs, the 7631 is disconnected and an interrupt occurs when the end signal is received from the 7631. The command counter contains the location plus one of the present command. The address counter contains the location plus one or two of the last word transmitted if the operation was a write or control, or the location plus one of the last word transmitted if the operation was a read or sense.

If an I-O check occurs while the channel is in interrupt mode, the I-O check is not recognized and is not saved.

Sequence Check

A sequence check indicates an invalid sequence of channel commands. Improper command sequences occurring while the channel is in interrupt mode may cause the 7909 to halt processing. If a sequence check occurs during data transmission, the 7631 is logically disconnected and the interrupt occurs when the end signal is received. In general, data transmission (read, write, or sense operations) may be started by one of the following sequences: A CTLR followed by a CPYP or CPYD; a CTLW followed by a CPYP or CPYD; or an SNS followed by a CPYP or CPYD. If transmission has been started with a CPYP, it must be ended with a CPYD. Between the first CPYP and the CPYD, transfers are possible but only four commands (CPYP, TCH, LIPT, or TDC) are permitted.

The following conditions cause a sequence check and a channel interrupt:

1. If a CTLW or CTLR, or SNS is followed by CTL, CTLW, CTLR, or SNS.
2. If a SNS or CPYP is followed by any command other than a CPYP, CPYD, LIPT, TCH, or TDC.
3. If a TCH, LIPT, or TDC following an SNS or CPYP transfers control to any command other than a CPYP, CPYD, TCH, or TDC.
4. If a CPYP or CPYD has not been properly preceded by a CTLW, CTLR, or SNS.

Unusual End

An unusual end indicates an error condition recognized by the 7631. This condition causes an immediate interrupt. The reason for the unusual end may be determined by sensing the 7631 error indicators (see "SNS--Sense Command").

Unusual-end interrupts may be disabled by the SMS command with a 1 bit in position 32. If unusual-end signals are inhibited and an unusual end is received, it is treated as a normal end, but the unusual-end indicator is set. A later SMS with a 0-bit in position 32 does not reset the indicator and, if not reset by other means--such as an LIP or LIPT command or a RIC instruction--the next end signal (normal or unusual) received from the 7631 causes an interrupt. The unusual-end interrupt does not occur automatically when the enabling SMS command is given. A halt in processing may occur during a CPYP operation if unusual-ends are disabled and an unusual end occurs. Examples of error indications that will cause this condition are:

- No Record Found
- File Control Circuit Check
- Disk/Drum Storage Circuit Check

If an I-O sequence, or adapter check occurs during a data transmission operation, the operation is immediately ended with a stop signal and an interrupt occurs when the end signal is received. If an unusual end occurs when transmission is ended, this condition is recognized. The channel does not interrupt twice but has both error indications available for examination during the interrupt routine. Data read or written during an operation that ended with an interrupt may be incomplete or invalid.

Attention Conditions

This is a signal indicating a change in status of the attached input-output device. During disk/drum operations, an attention signal is generated when an access mechanism has completed a seek operation. The access mechanism that generated this indication may be determined from sense data. Drum operations have only one access.

The single attention indicator in the 7631, common to all access mechanisms, is reset when the 7909 interrupts. The individual access bits are reset by giving a read, write, or control command to the individual access address.

There are two attention indicators in the 7909. Attention 1 indicates a signal from the device attached to position 1 of the data channel switch feature; attention 2 indicates a signal from the device attached to position 2.

Either or both attention interrupts may be disabled with the SMS command. If attention interrupts are inhibited, the status indicator is set but no interrupts occur and no attention response is sent to the 7631. When an SMS that enables an existing attention indicator is executed, the interrupt occurs at termination of the SMS, and the attention response is sent to the 7631.

Attention interrupts are serviced only at the logical termination of the command during which they occur. The logical termination of a read or write operation is the disconnect resulting from a CPYD. Attention signals occurring while the channel is in interrupt mode do not set the status indicators; however, a second interrupt, to service the adapter attention signal, occurs as soon as the channel leaves the interrupt mode. In this case, the channel executes the command following the LIP or LIPT command before interrupting on the second attention signal.

Adapter Check

An adapter check indicates an error recognized by the 7909 and does not necessarily indicate a 7631 malfunction. Conditions causing an adapter check are:

1. Failure in the 7909 character-handling circuitry.
2. The character rate of the attached I-O device exceeds the capability of the channel.
3. The 7631 is not operational. This type of indication occurs if power is off on the 7631 and an attempt is made to read, write, control, or sense. On shared disk/drum storage systems, this indication occurs if an attempt is made to read, write, control, or sense and the 7631 is in operation on the sharing system.

If an adapter check occurs while the control unit is selected, the 7631 is logically disconnected and the interrupt occurs when the end signal is received.

CTL--Control



Description: The control command is decoded in the channel. Information contained in C(Y) is sent to the file control, starting with the high-order character, and continues until an end signal is received from the file control. If more than one word location is necessary to transmit all data required by the channel, the next word is taken from location Y+1, etc. This process continues until an end signal is received; the next command is then taken from the storage location following the control command.

Execution: The contents of the address counter are replaced by Y, and the data register contents are replaced by C(Y). When the first data request is received from the 7631, data register contents enter the assembly register, and the C(Y+1) replace the contents of the data register.

The contents of the assembly register are sent to the 7631 character by character, beginning with the high-order character under control of the 7631. Successive words are sent to the 7631 until an end signal is received from the 7631.

CTLR--Control and Read



Description: This command causes the channel to transmit control information, as with the CTL, and also prepares the channel for a read operation. When an end signal is received from the 7631, the channel proceeds to the next sequential command (which must be a copy or a TCH to a copy if data transmission is expected). When a copy command is encountered, the channel is placed in read status, and data are transmitted to core storage under control of the copy command.

Execution: Execution is the same as with CTL except that the prepare to read indicator in the 7909 is turned on.

CTLW--Control and Write



Description: This command causes the channel to transmit control information in the same manner as with the control command and also prepares the channel for a write operation. When an end signal is received from the 7631 (signaling the end of the order), the channel proceeds to the next sequential command (which must be a copy or a TCH to a copy if data transmission is expected). When the copy command is encountered, the channel is placed in write status, and data are transmitted from core storage to the 7631 under control of the copy command.

Execution: Execution is the same as with CTL except that the prepare to write indicator in the 7909 is turned on.

SNS--Sense



Description: Execution of this command places the channel in sense status and then proceeds to the next sequential command (which must be a copy or a TCH to a copy if sense data transmission is expected). When a copy command is encountered, sense information is sent to core storage under control of the copy command.

Execution: Execution of the SNS turns on a sense indicator in the 7909, which causes the 7631 to transmit sense data. The channel then proceeds to the next sequential command. A copy (CPYP or CPYD) command is required to provide word count and address information to be used in storing the sense data. If the SNS is not followed immediately by a copy command or a TCH to a copy, a sequence check occurs. If the assembly register is filled before a copy command is encountered, an I-O check results.

A maximum of two sense data words are available from the 7631. Both words can be stored, or it is

possible to store only the first word by using a CPYD with a word count of 1. The meaning of each sense data-bit, as placed in core storage is:

<u>First Word</u>			
Bit		Bit	
<u>Position</u>	<u>Meaning if a 1</u>	<u>Position</u>	<u>Meaning if a 1</u>
1	Reserved	21	Access Not Ready
3	Program Check	22	Disk Circuit
4	Data Check		Check
5	Exception	23	File Circuit
	Condition		Check
7	Invalid Sequence	25	Reserved
9	Invalid Code	27	Six-Bit Mode
10	Format Check	28	Reserved
11	No Record Found	29	Reserved
13	Invalid Address	31	Access 0,
15	Response Check		Module 0
16	Data Compare	33	Access 0, Module
	Check		1 (1301 only)
17	Parity or Cyclic	34	Access 0,
	Code Check		Module 2
19	Access	35	Access 0, Module
	Inoperative		3 (1301 only)

<u>Second Word</u>			
Bit		Bit	
<u>Position</u>	<u>Meaning if a 1</u>	<u>Position</u>	<u>Meaning if a 1</u>
1	Access 0,	10	Reserved
	Module 4	11	Reserved
3	Access 0,Module	13	Reserved
	5 (1301 only)	15	Reserved
4	Access 0,	16	Reserved
	Module 6	17	Reserved
5	Access 0, Module	19	Reserved
	7 (1301 only)	21	Reserved
7	Access 0,	22	Reserved
	Module 8	23	Reserved
9	Access 0, Module		
	9 (1301 only)		

All bit positions (of both sense data words) not mentioned in the tables are not used but contain zeros.

CPYD--Copy and Disconnect



Description: This command, when decoded by a channel not prepared to read or write, causes a sequence check and, thus, a channel interrupt. If the channel is prepared to read or write, this command causes C words to be transmitted between the channel and core storage, starting with location Y. Data transmission continues until C is reduced to zero or an end signal is received by the channel. In either case, the channel read or write select is re-

set. If, while a CPYD is being executed, an end signal is received before the count is reduced to zero, the channel read or write select is reset, and the channel obtains a new command from the next sequential location.

If the next command is other than a copy, the channel executes that command. If the next command is a copy, the channel interrupts on a program sequence check.

If the count for the CPYD goes to zero before the end signal is received, the channel initiates a disconnect but does not get the next sequential command until an end or unusual-end signal is obtained. In general, when operating under CPYD control, the channel does not obtain the next sequential command until either an end or unusual end (signaling an error) occurs. In event of an unusual-end signal, an interrupt occurs.

Execution, Read or Sense Operation: Y replaces the contents of the address counter. If the channel is in prepare-to-read status, this condition is reset and the 7631 is signaled to begin transmission of data to core storage. If the read or sense indicator is on from a previous SNS or CPYP, data transmission is continued under control of the CPYD. When the assembly register is full, it is emptied into the data register and access to core storage is requested.

As each word is placed in core storage, the address counter is increased by one and the word counter is decreased by one. If the word count is reduced to zero before an end signal is received, a disconnect is initiated, and the channel obtains its next command when the end signal is received. If a word or partial word has been received, it is stored.

If an end signal is received before the word count is reduced to zero, the last word transmitted is stored and the channel gets the next sequential command.

Execution, Write Operation: Y replaces the contents of the address counter. If the channel is in prepare-to-write status, this condition is reset and the write indicator is turned on. The C(Y) are placed in the data register. When the first data request is received from the 7631, the data register contents are placed in the assembly register and the C(Y+1) replace the contents of the data register.

If the write indicator is on from a previous CPYP command, data transmission is resumed under control of the CPYD. As each word is transmitted to the 7631, the address counter is increased by one and the word counter is reduced by one.

Disconnect procedures are the same as for a read or sense operation. A CPYD with a word count of zero causes a disconnect without further data transmission.

CPYP--Copy and Proceed



Description: This command, when decoded by a channel not prepared to read or write, causes a sequence check and channel interrupt. If the channel is prepared to read or write, this command causes C words to be transmitted between the channel and core storage, starting with location Y. End signals from the 7631 are serviced, but the channel does not disconnect and data transmission continues until C is reduced to zero. The channel then does not disconnect but obtains the next sequential command. If this command is a TCH, TDC, or a copy, operation is normal and data transmission is resumed. If the next command does not satisfy these conditions, the channel disconnects and interrupts on a sequence error. If an unusual end occurs, the channel interrupts.

During a read operation, if an end signal is received during a CPYP command, the word or partial word assembled is stored and the 7631 is signaled to proceed. During a write operation, if an end signal is received during a CPYP command, the 7631 is signaled to proceed. Data transmission is resumed with the next sequential character. If, during writing the total word count of all CPYP commands is equal to or one greater than the length of the record, there is a possibility that the terminating CPYP command will be skipped, although the 7631 will have been logically disconnected.

Execution: End signals from the 7631 are serviced during a CPYP command. Following the end signal, however, the 7909 signals the 7631 to proceed (write, read, or sense). Unusual-end conditions cause a channel interrupt. A CPYP command may be followed by a CPYP, CPYD, or TCH or TDC to another copy command.

Use of the CPYP in 7631 operation should be carefully controlled. A normal end should never occur during 7631 operation using a CPYP command. If word counts are not properly controlled (that is, the total word counts of all CPYP commands in a write or read sequence are greater than the record length), or if the word count is equal to the record length and a CPYP or CPYD with a word count follows, data will be destroyed.

Consider a single record operation where the word count of the record is 100:

CTLW DVSR Verify single record
 CPYP A,,150 Write 150 words
 CPYD B,,10 Write 10 words

When 100 words have been written, the 7631 sends an end signal. The 7909 signals write again, and

the remaining 60 words are dumped on top of the first 100. The remaining 40 (of the original 100) are replaced with zeros and no errors are indicated. This condition is possible on all operations except write format. If an attempt is made to exceed the capacity of a format track, a format check results.

It is generally desirable to follow with a write check operation all write operations using CPYP. This assures error detection if a data wrap-around occurs. A routine that may be used to write and write check is:

Location	Operation	Address	Comment
	LCC	1	
WR	CTLW	DVSR	Verify single record
	CPYP	A,,150	Write 150 words
	CPYD	B,,10	Write 10 words
	TDC	*+2	Go to write check if control counter not zero
WC	WTR	*	End of write, write check
	CTLW	DWRC	Prepare to write check
	TCH	WR+1	

TCH--Transfer in Channel



Description: This command is the transfer command for all channels. When a TCH command is executed, command sequence control is transferred to location Y.

Execution: When a TCH command is executed, the data channel transfers to location Y. The command at location Y is loaded into the data channel and the command counter is increased to Y+1.

LAR--Load Assembly Register



Description: Execution of this command causes the contents of the assembly register to be replaced by the C(Y). The C(Y) remain unchanged. After execution, the channel proceeds to the next sequential command.

Execution: The contents of Y are sent through the storage bus switches and the data register to replace the contents of the assembly register.

SAR--Store Assembly Register



Description: Execution of the SAR causes the C(Y) to be replaced by the contents of the assembly register. Contents of the assembly register remain unchanged. After execution, the channel proceeds to the next sequential command.

Execution: The assembly register contents are stored in location Y, as specified by the address counter, in the same manner as for a read operation.

XMT--Transmit



Description: This command causes the C words immediately following the location of the XMT command to be transmitted to C locations starting at location Y. When the C field is reduced to zero and the Cth word has been transmitted, the channel obtains its next command from the location of the XMT command plus C, plus one. If the initial count field is zero, the XMT command is skipped and the channel proceeds to the next sequential command.

Execution: The command counter is increased by one and the first word is obtained from this location and brought to the data register. The command counter is then increased by one again. The data register contents are stored in location Y. The address counter is increased by one and the word counter is reduced by one. The second word is entered into the data register from the storage location specified by the command counter. This operation proceeds until the word count is reduced to zero. The channel then takes its next command from the location of the XMT command plus C plus one. The contents of the assembly register remain unchanged. The XMT command may be used to move blocks of data, commands, or entire subroutines from one area of core storage to another area.

LCC--Load Control Counter



Description: This command causes the contents of the channel control counter to be replaced by the six low-order positions of the count field of the LCC command. The channel then proceeds to the next sequential command. If the LCC is indirectly ad-

ressed, the contents of the control counter are replaced by the six low-order bits contained in the location specified by positions 21-35 of the LCC command.

Execution: The control counter is reset. The contents of positions 12-17 of the address counter are placed in positions 1-6 of the control counter. The channel then proceeds to the next command as specified by the command counter.

TDC--Transfer and Decrement Counter



Description: On execution of this command, the contents of the six-bit channel control counter are examined. If the contents are not zero, the counter is reduced by one and control is transferred to location Y. If the counter contents are zero, the channel proceeds to the next sequential command, leaving the counter contents unchanged.

Execution: If the control counter contains a count of zero, the channel proceeds to the next command as specified by the command counter. If the control counter is not zero, it is decreased by one. The command counter is reset and replaced by the contents of the address counter. The channel then takes the next command from location Y.

ICC--Insert Control Counter



Description: When the count field (C) of the ICC is not zero, this command causes the C field to specify one of the six characters in the assembly register to be replaced by the contents of the control counter. The remaining five characters are not affected. If C is zero, the sixth character of the assembly register is replaced by the contents of the SMS status indicators. In either case, the channel proceeds to the next sequential command after execution of the ICC. An ICC with a C field of seven functions as a no operation. The contents of the assembly register remain unchanged.

Execution: Word counter positions 3, 4, and 5 are decoded to specify a character of the assembly register. The selected character is reset and replaced by the control counter if the C field is one through six or by the SMS status indicators if the C field is zero.

TCM--Transfer on Condition Met



Description: When C is not zero, this command causes C to specify one of the six characters in the assembly register for comparison against the contents of the mask M. Comparison is achieved in either of two ways, depending on whether bit position 11 of this command contains a 1 or a 0.

If bit position 11 contains a 0, comparison is achieved when the specified character and the mask character are identical, bit for bit.

If bit position 11 contains a 1, comparison is achieved only when, for each bit in the mask that is a 1 bit, the corresponding bit position of the specified character is also a 1 bit.

If the comparison is achieved, the channel executes a transfer to location Y. If the comparison is not achieved, the channel proceeds to the next sequential command. If C is zero, the channel check condition register is compared against M in either of the two ways described above. Transfer conditions resulting from the comparison are as previously stated. When indirect addressing is used, control is transferred to the indirectly addressed location when the condition is met. If C is equal to seven, the results depend on mask contents. If all bits in positions 12-17 of the TCM are zero, the channel executes a transfer to location Y. Otherwise, the channel proceeds to the next sequential command.

Execution: Word counter contents (positions 3, 4, and 5) are decoded to find the count. Assembly register contents are divided into six characters with the first character in position S, 1-5 and the last character in positions 30-35. If the count field is a value one through six, one of the characters from the assembly register (specified by C) is compared with the M field of the TCM. If C is zero, the six-position check condition register is compared with M. If C is seven, a six-bit character of all zeros is compared with M. If a bit-for-bit comparison is achieved, the channel transfers control to location Y. The command counter is reset and replaced with the contents of the address counter. If a comparison is not achieved, the channel proceeds to the next sequential command. The contents of the assembly register and the check condition register remain unchanged.

SMS--Set Mode and Select



Description: Execution of this command causes the contents of positions 30-35 of this command to set or reset specific status indicators as follows:

Bit	Function
30*	Read Backward
31*	BCD Mode
32	Inhibit Unusual End Signals
33	Inhibit Attention 1 Signals
34*	Inhibit Attention 2 Signals
35*	Select 2 (1 is selected when reset)

* Optional Features

Bits 34 and 35 apply to the data channel switch optional feature following the "IBM 7909 Data Channel Commands." In all cases, the presence of the bit causes the status indicator to be set and the function to be enabled; absence of the bit resets the status indicator and disables the function. Machine and power-on resets also reset the indicators. With indirect addressing, the SMS command status indicators are set or reset with bits 30-35 of the location specified by bits 21-35 of the indirectly addressed command. After execution of the SMS, the channel proceeds to the next sequential command.

WTR--Wait and Transfer



Description: When this command is decoded, the channel stops operation and may be thought of as waiting. The channel location counter contains the location of the WTR command. When the channel is told to start, it takes its next command from the location specified by the Y of the WTR command. If an interrupt occurs while the channel is in wait status, return from the interrupt program by means of a LIP command puts the channel in wait status.

Execution: Execution of this command forces the channel to wait. The channel may be restarted by either an RSC or STC command or by an interrupt. The command counter is not changed and the address counter contains Y. If the WTR is indirectly addressed, the address counter contains the contents of the address portion of location Y.

TWT--Trap and Wait



Description: Upon decoding a TWT command, the channel suspends operation until either a reset and start or start channel instruction is executed by the

CPU, depending on conditions described below. If the channel is enabled for control word traps, the channel causes the CPU to trap to a fixed location. Particulars concerning this trap are described under "Data Channel Trap" in the IBM 7090 Data Processing System Reference Manual, Form A22-6528, and IBM 7094 Data Processing System Reference Manual, Form A22-6703.

If the channel is enabled and encounters a TWT command, start channel instructions are ignored until the trap is executed or a reset and start channel instruction is executed. If the channel is not enabled, either a reset and start or start channel instruction resets the trap and causes the channel to resume operation.

Channel interrupt signals are remembered but not executed until the channel brings in a command other than TWT. (An RSC resets these stored interrupt signals.) After the channel has stopped operation as a result of a TWT, the channel command counter contains the location of that command.

Assume that B is the location where the instruction counter contents are stored when a trap occurs on this particular channel and that CPU control is transferred to B+1. SUB is the entry point for the subroutine that the channel requests the CPU to execute.

Command Address Comment

XMT	B+1,,1	Moves the following TRA to location B+1.
TRA	SUB	
TWT	Y	Transfers control to CPU at location B+1.

Execution: When the TWT is decoded, the wait indicator is turned on, the channel trap demand is initiated, and the channel waits. The command counter is not changed, and the address counter contains Y. If the TWT is indirectly addressed, the address counter contains the contents of the address portion of location Y.

LIP--Leave Interrupt Program



Description: This command causes the channel to transfer control to the location contained in the address part of the channel's fixed "interrupt-to" location. The channel command counter is set to the value in the address portion of this fixed location. Execution of the LIP also cancels the inhibiting effect of a previous interrupt.

Execution: The interrupt and check condition indicators are reset and the contents of the address portion of the fixed interrupt-to location are entered in the command counter. The contents of the location specified by the command counter are loaded into the operation register, word counter, and address counter. The command counter is stepped to the location of the next command.

LIPT--Leave Interrupt Program and Transfer



Description: Execution of the LIPT command cancels the inhibiting effect of a previous interrupt and transfers channel control to location Y. Use of the LIPT permits returning from the interrupt subroutine to a program location other than the interrupt address.

Execution: When an LIPT command is executed, the interrupt and check condition indicators are reset and the channel proceeds to location Y for its next command. The command located at Y is loaded into the channel and the command counter is increased to Y+1.

Programming Example of LIPT Command:

<u>Location</u>	<u>Instruction or Command</u>	<u>Address</u>	<u>Comment</u>
100	XMT	RSTRT,,1	Store return address
101	PZE	102	in indirect address restart location.
102	CTLR	DVTN	Read 30 words using
103	CPYP	BEGIN,,10	track with no ad-
104	CPYD	END,,20	dresses.

RSTRT is a location used to store restart addresses. The XMT command stored PZE 102 at location RSTRT. Assume that an I-O check occurs during the CPYP command. The channel initiates a disconnect and interrupts. The command counter contains 104, the location of the next command. If the error routine decides to try again, an LIP command cannot be conveniently used, because the channel leaves the interrupt routine and transfers to location 104. A sequence check would occur, followed by another interrupt.

If the interrupt routine is ended with an indirectly addressed LIPT command (LIPT RSTRT, 4), rather than a LIP, the channel returns to the CTLR command and retries the failing section of the program.

OPTIONAL FEATURES

Data Channel Switch

The IBM 7909 Data Channel Switch permits simultaneous attachment of one or two input-output control units to one 7909 Data Channel. Thus, one 7631 File Control and one channel of a 7640 Hypertape Control may be attached to one 7909 Data Channel as shown in Figure 10.

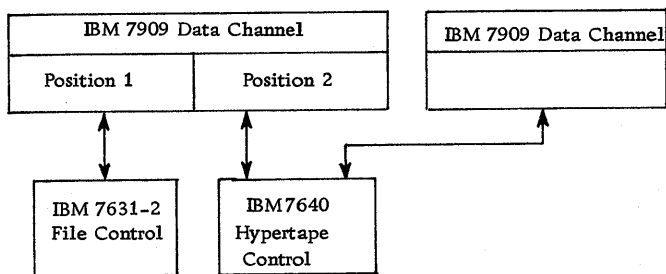


Figure 10. IBM 7909 Data Channel Switch Optional Feature

When the 7909 is equipped with the channel switch, data transmission occurs between the 7909 and one of the control units. Attention signals, however, are monitored from each control unit simultaneously. The 7909 is then able to select the control unit and determine priority of attention requests by means of its own stored program.

Unusual end and I-O check signals apply only to the control unit currently selected. Indicators are included to record attention signals from the non-selected control unit and to denote which control unit is currently selected. Attention interrupts occur on signal from either or both of the control units and are subject to the same limitations (described under "Interrupt Conditions") as without this feature.

BCD Translation

This feature provides automatic BCD translation for information transmitted between the 7631 File Control

and the 7909 Data Channel. After execution of an SMS command (with a 1 bit in position 31), data transfers between the 7909 and the 7631 are translated as shown in Figure 11. Control and sense data are not translated. An SMS command with a 0 bit in position 31 returns data transfer mode to binary.

This feature allows the 7090 and 7094 systems to share data with other systems. Translation of data is shown in Figure 11 with the characters divided into their bit configurations. Each character is shown as it appears in core storage and in disk or drum storage.

With the translation feature enabled, binary data may be written in BCD format and recovered by reading in the BCD mode. No indication will occur when data written in one mode are read in the other mode.

Home addresses and record addresses may be written using BCD format. This automatically provides the BCD format required in all address areas. Note, however, that subsequent attempts to verify an address written in BCD format will fail unless the 7631 orders are program-modified to conform to disk/drum storage BCD codes. Information sent to the 7631 during a control operation is not translated whether in BCD mode or not. This is a restriction only, where portions of the address are alphabetic characters. Numeric addresses must always be expressed in BCD format.

Core Storage	Drum Storage Disk Storage
B A 8 4 2 1	B A 8 4 2 1
0 0 0 0 0 0	0 0 1 0 1 0
0 0 1 0 1 0	0 1 0 0 0 0
0 0 (other)	0 0 (no change)
0 1 (any)	1 1 (no change)
1 0 (any)	1 0 (no change)
1 1 0 0 0 0	0 0 0 0 0 0
1 1 (other)	0 1 (no change)

Figure 11. IBM 7909 Data Channel
BCD Translations

The 7631 will decode and execute up to 13 orders transmitted from core storage by the control command. The 7631 decodes the transmitted order, accepts address information, performs the designated function, and then transmits an end or unusual end signal to the data channel. In the case of a seek order (which causes only electronic read/write head switching in the 7320 as compared to actual mechanical motion of the access mechanism in the 1301), the 7631 sends the end signal after decoding the order. At the completion of the seek operation, the 7631 sends an attention signal to the data channel.

ORDER BYTES

An order may require as many as ten characters to describe the operation to be performed. Ten 4-bit characters (bytes) make up the order, therefore two order words will be required to represent the order. Assume that B represents a four-bit byte; the complete order format is:

B1 B2 B3 B4 B5 B6 B7 B8 B9 B0

The bytes are defined according to position as follows:

- B1 and B2 Operation Code
- B3 Access Mechanism
- B4 Module Number
- B5-B8 Track/Head Number
- B9 and B0 Record Number

The 7631 File Control orders are shown in Figure 12 with mnemonics, operation name, byte configuration, and numeric code. Figure 13 shows the required order bytes by operations.

No Operation (DNOP-00)

Disk Operation: This order requires only a two-digit operation code. The order is accepted by the 7631 as a programming convenience only. No function is performed by the 7631 for this order.

Drum Operation: Same as disk operation.

Release (DREL-04)

Disk Operation: This order requires only a two-digit operation code. The order has meaning only for shared system operation. Whenever either system selects and gains control of the 7631, it remains in control of that system until the release order is

issued to permit the file control to be available for either system.

Drum Operation: Same as disk operation.

Mnemonic	Operation	Byte B1				Byte B2				Numeric Code
		8	4	2	1	8	4	2	1	
DNOP	No Operation	1	0	1	0	1	0	1	0	00
DREL	Release	1	0	1	0	0	1	0	0	04
DEBM	Eight-Bit Mode	1	0	1	0	1	0	0	0	08
DSBM	Six-Bit Mode	1	0	1	0	1	0	0	1	09
DSEK	Seek	1	0	0	0	1	0	1	0	80
DVSR	Prepare to Verify (Single Record)	1	0	0	0	0	0	1	0	82
DWRF	Prepare to Write Format	1	0	0	0	0	0	1	1	83
DVTN	Prepare to Verify (Track Without Address)	1	0	0	0	0	1	0	0	84
DVCY	Prepare to Verify (Cylinder Mode)*	1	0	0	0	0	1	0	1	85
DWRC	Prepare to Write Check	1	0	0	0	0	1	1	0	86
DSAI	Set Access Inoperative	1	0	0	0	0	1	1	1	87
DVTA	Prepare to Verify (Track With Address)	1	0	0	0	1	0	0	0	88
DVHA	Prepare to Verify (Home Address)	1	0	0	0	1	0	0	1	89
*Optional Feature										

Figure 12. Drum/Disk Storage Orders

Order	Order Bytes				
	Code	Access	Module	Track and Head	Record Number
DNOP	B1-B2				
DREL	B1-B2				
DEBM	B1-B2				
DSBM	B1-B2				
DSEK	B1-B2	B3	B4	B5-B8	B9-BO*
DVSR	B1-B2	B3	B4	B5-B8	B9-BO
DWRF	B1-B2	B3	B4	B5-B8	B9-BO*
DVTN	B1-B2	B3	B4	B5-B8	B9-BO*
DVCY	B1-B2	B3	B4	B5-B8	B9-BO*
DWRC	B1-B2	B3	B4	B5-B8	B9-BO
DSAI	B1-B2	B3	B4	B5-B8*	B9-BO*
DVTA	B1-B2	B3	B4	B5-B8	B9-BO*
DVHA	B1-B2	B3	B4	B5-B8	B9-BO*

* The characters used in these positions are at the programmers discretion.

Figure 13. Drum/Disk Order Bytes Required by Operation

Eight-Bit Mode (DEBM-08)

Disk Operation: This order requires only a two-digit operation code. The order conditions the 7631 to operate in the eight-bit mode. This mode of operation is required when the using system is operating in the packet format mode. 7090 and 7094 systems do not use packed format mode. The maximum data rate for eight-bit mode is 70.1 KC in data areas, with a maximum of 2,165 data bytes stored on the disk track.

Drum Operation: Same as disk operation. The maximum data rate for eight-bit mode is 152.1 KC in data areas, with a maximum of 2,372 data bytes stored on the drum track.

Six-Bit Mode (DSBM-09)

Disk Operation: This order requires the two-digit operation code only. The order conditions the file control to operate in the six-bit mode. The data rate for the 7631 when operating in the six-bit mode is 90,100 characters per second. Maximum track capacity is 2,796 characters. 7090/7094 systems normally exchange data in six-bit mode.

Drum Operation: Same as disk operation. The data rate for the 7631 operating in the six-bit mode is 202,800 characters per second. Maximum track capacity is 2,796 characters.

Seek (DSEK-08)

Disk Operation: The order for this operation causes the specified access mechanism of the addressed module to locate itself at the proper cylinder and to select the desired head. When the order has been received by the file control, it gives an end signal and allows the computer to continue with its own routine while disk storage executes the seek operation. A seek may be directed to other access mechanisms on the disk storage units attached to the same file control. An unusual end signal results if a seek is given to an access mechanism in motion or if the access mechanism is inoperative.

Drum Operation: In drum storage operation, there is no mechanical head switching. This means that, with the 7320 Drum Storage, the program interrupt generated when a seek is completed will always arrive during the seek. With drum storage operation, there is no mechanical motion, and therefore the access arms cannot be in motion; thus, the 7320 Drum Storage does not have provision for a not ready signal.

On completion of a seek operation, an attention signal is sent to the data channel. In addition, a bit associated with the access mechanism is set in status data to indicate this condition. This indication is sent as part of the status data transmitted in response to a sense command. The attention indicator is reset when the access is serviced by either a prepare to verify order or another seek order.

The seek order, preceding a cylinder or full track order, is not necessary when the current setting of the access mechanism corresponds to the desired address. Also, a seek order need not be repeated for consecutive single-record operations on the same track.

Prepare to Verify, Single Record (DVSR-82)

Disk Operation: The order for this operation conditions the 7631 for a single-record type of operation and to perform the following functions:

1. Select the desired module and access mechanism.
2. Specify the address to be verified.
3. Prepare to transmit data from or to the addressed record in response to a subsequent read or write command.

The order sent to the 7631 is used with the read or write command. Access and module number specify the unit to be selected. Since the access mechanism is already located and held in the track position and the desired head is selected by the previous seek operation, the remainder of the order is used only for verification.

The file control (in single-record mode) compares each record address, as it comes under the read head, against the address furnished by the order until the desired address is found.

Information can be read from or written into record areas only as defined by format tracks. Reading or writing continues until either a stop signal is issued by the computer or the 7631 recognizes the end of record, depending on whether a read or write command is being executed.

Drum Operation: Same as disk operation.

Prepare to Write, Format (DWRF-83)

Disk Operation: This order conditions the 7631 to write a format track for the cylinder specified by the address portion of the order (the last two positions of this order are insignificant). To address a format track, the format two-position key-lock switch must be in the Write position; the track address must be one of the track addresses of the cylinder associated with the format track. To write a format track, this order must precede the write command.

Drum Operation: Same as disk operation. To address a format track, the write format two-position key-lock must be in the Write Format On position; the track address may be any of the 400 data tracks.

Prepare to Verify, Track Without Addresses (DVTN-84)

Disk Operation: This order, followed by a read or write command, permits reading or writing only the records on a particular track; all addresses are skipped over. The address portion of this order must specify the home address.

This order instructs the 7631 to:

1. Select the desired module.
2. Supply the home address to be verified.
3. To receive or transmit only the records in response to a subsequent read or write command.

Reading or writing begins at the first record following the home address, and continues through the records, skipping over addresses until the computer signals stop or the 7631 recognizes the end of the data areas. Non-verification of the home address results in an unusual end signal, with no transmission of data to or from disk storage.

Drum Operation: Same as disk operation.

Prepare to Verify, Cylinder Operation (DVCY-85)

Disk Operation: This is an optional feature. It permits reading or writing of data (skipping over addresses), beginning at the first record after the home address of the addressed track and continuing through successive record locations and the tracks of the cylinder until either the end of cylinder is reached or the computer signals a stop. This order is always followed by a read or write command. The following functions are performed in the cylinder operation mode:

1. Select desired module and access mechanism.
2. Specify desired home address to be verified.
3. Transmit data after the subsequent read or write command has been given.

Drum Operation: Same as disk operation.

Prepare to Write Check (DWRC-86)

Disk Operation: This order is used with a write command to check any record, track, or cylinder of tracks of information. This order performs a bit-for-bit comparison, comparing the information recorded on the disk with the same information stored in core storage of the computer. If data agree, the order terminates with an end signal; if

data disagree, the order terminates with an unusual end signal. The sequence of commands and orders to write and check recorded data is:

Seek	-----
Prepare to Verify	
(Single, Track, Cylinder)	XXXXXXXX*
Write	-----
Prepare to Write Check	XXXXXXXX*
Write	-----

*Must be same address

The use of the write check operation is optional, depending on the application.

Drum Operation: Same as disk operation.

Set Access Inoperative (DSAI-87)

Disk Operation: This file control order causes the 7631 to disconnect the addressed access unit from the file control. (It permits the programmed disconnection of a faulty access unit from the system.) Any subsequent command to this access will result in an unusual end.

(Note: Reactivation of the inoperative access unit is accomplished manually by the customer engineer after the fault has been corrected.)

Drum Operation: This order causes an unusual end and invalid code sense indication.

Prepare to Verify, Track with Addresses (DVTA-88)

Disk Operation: This order, followed by a read or write command, permits reading or writing a full track of information, including record addresses and records. It makes use of the home address that defines the track address.

This order instructs the file control to:

1. Select the desired module and access mechanism.
2. Supply the home address to be verified.
3. Condition the 7631 to operate on a full-track basis and receive and transmit both record addresses and record areas in response to a subsequent read or write command.

The order is used whenever changes are to be made to record addresses and insertions or deletions are to be made on a track that contains randomly distributed records.

The execution of this order is similar to that performed by the prepare to verify (cylinder operation) in that only the home address is verified. If verification is successful, reading or writing begins at the following record address and continues through the records and the record address until the computer signals a stop or the 7631 recognizes the end of the data areas. Non-verification of the home

address results in an unusual end signal with no transmission of data to or from the disk storage.

Drum Operation: Same as disk operation.

Prepare to Verify, Home Address (DVHA-89)

Disk Operation: This order prepares the 7631 to read or write an entire track of data and addresses including the home address identifier (HA 2). The home address must be supplied for subsequent verification. For execution of this order, the home address switch must be on. (The switch is on the 7631 File Control.)

This operation is terminated by a stop signal from the computer or when the 7631 recognizes the index point.

Drum Operation: Same as disk operation.

SENSE COMMAND

The sense command instructs the file control to transmit status data to the computer to indicate error and unusual conditions as well as attention conditions. This operation is similar to a read command except that only the ten 6-bit characters are transmitted to the computer. The status data are transmitted to the data channel over the BCD A, 4, 2, and 1 bit lines. (The BCD B and 8 lines always contain zero.)

Status data are set in bit form for each read, write, and control operation performed by the 7631 and are available to the computer by means of the sense command. The status data should be called for by the computer before the initiation of the next read, write, or control command. (The initiation of the next command resets all error indications of the status data.)

Figure 14 shows the make-up of the status data transmitted to the data channel of the using system.

Status character 0 summarizes the type of check or condition; characters 1 and 2 give the type of check encountered; character 3 gives the different, exceptional conditions; character 4 gives the data mode; characters 5, 6, and 7 give attention conditions; and character 8 and 9 are reserved.

WRITE OPERATIONS

A write command must always be preceded by a prepare to write check, prepare to write format, or a prepare to verify order. A write command not preceded by one of these orders is terminated with an unusual end signal with no transmission of data to the file control. (A no operation order can be inserted between the prepare to . . . and the write command.)

Status Char	Bit No.	BCD Bit	Assignment	Comment
0	3	A	Reserved	Summary Byte
	5	4	Program Check	
	6	2	Data Check	
	7	1	Exceptional Condition	
1	3	A	Invalid Sequence	Program Check
	5	4	Invalid Code	
	6	2	Format Check	
	7	1	No Record Found	
2	3	A	Invalid Address	Data Check
	5	4	Response Check	
	6	2	Data Compare Check	
	7	1	Parity or Check Char Code Check	
3	3	A	Access Inoperative	Exceptional Condition
	5	4	Access Not Ready	
	6	2	Disk/Drum Storage Circuit Check	
	7	1	File Control Circuit Check	
4	3	A	Reserved	Data Mode
	5	4	Six-Bit Mode	
	6	2	Reserved	
	7	1	Reserved	
5	3	A	Module 0	Attention
	5	4	Module 1 (Disk Only)	
	6	2	Module 2	
	7	1	Module 3 (Disk Only)	
6	3	A	Module 4	Attention
	5	4	Module 5 (Disk Only)	
	6	2	Module 6	
	7	1	Module 7 (Disk Only)	
7	3	A	Module 8	Attention
	5	4	Module 9 (Disk Only)	
	6	2	Reserved	
	7	1	Reserved	
8,9			Reserved	

Figure 14. Status Data Bit Assignment

Write Format Track

To write a format track, three conditions must be met:

1. The format switch must be in the Write position; if not, no writing of the format track will take place.
2. A prepare to write format order with a track address of one of the tracks of the drum must be received and normally terminated by the 7631. Drum storage track address may be any of 400 tracks.
3. The prepare to write format order must be followed by a write command specifying a core storage location that contains the field of special characters used to write a format track.

During a format write operation, the 7631 legally accepts only four characters: BCD 1, BCD 2, BCD 3, and BCD 4. For operation in the six-bit mode, BCD 1's are used to write the character of all one bits; BCD 2's are used to write the character of all zero bits. For operation in the eight-bit mode, BCD 3's are used to write the character of all one bits; BCD 4's are used to write the character of all zero bits.

Figure 15 shows a typical core storage layout for n records in both the six-bit mode and eight-bit mode. When a data track is being organized in core storage, only the information that is to be recorded must be provided for; however, when a format track is being organized in core storage, the special BCD characters must be provided to write every character position. This includes the HA 1 area, as well as other addresses and gap areas to be used in defining the related areas for the associated data tracks.

When laying out a format track, the following points must be considered.

Format Track Capacity: The maximum character positions available when a format track is being written are:

Six-Bit Mode: 2,869 characters to control data tracks of 2,880 character positions for both disk and drum units.

Eight-Bit Mode: 2,234 characters to control data tracks of 2,245 character positions for both disk and drum units.

These figures represent the total track capacity of the format track. Exceeding the track capacity results in a format check indication.

Track Identification: This area immediately follows the index point and corresponds to the HA 1 pre-recorded data track area and consists of three parts: Gap 1 must contain three BCD 4's; HA 1 must contain nine BCD 3's; Gap 2 must contain a BCD 4 followed by ten BCD 3's and a BCD 4. The track identification area is always written in the eight-bit mode and is the same for all format track layouts.

Home Address Two (HA 2): This area must contain four more BCD 1's (six-bit mode) than the number of characters assigned for HA 2. The four character positions are needed for each record and each address area to provide space for internal synchronization information. For example, if HA 2 is a six-character home address identifier, then, ten BCD 1's must be used in this area. For operation in eight-bit mode, BCD 3's must be used instead of the BCD 1's.

X Gap: An X gap must precede every record address (RA). This gap is made up of 12 BCD 2's or 12 BCD 4's, depending upon the mode of operation.

Record Address (RA): This area must contain four more BCD 1's than the number of characters assigned for RA. For example, if RA contains six digits, then ten BCD 1's must be used. For operation in eight-bit mode, BCD 3 must be used instead of BCD 1. There must be as many record address areas on the format track as there are records.

Y Gap: A Y gap must follow every RA. For six-bit mode operation, this gap is made up of one BCD 2, followed by 10 BCD 1's and a BCD 2. For 8-bit mode, the Y gap is made up of one BCD 4 followed by 10 BCD 3's and another BCD 4.

Record Areas: There must be four more BCD 1's than there are characters in the record for the six-bit mode operation. For example, for an 80-character record, 84 BCD 1's must be provided. For the eight-bit mode, BCD 3's are to be used instead of the BCD 1's. This area must contain at least six characters, that is, a two character record plus the four extra BCD characters.

Gap 3: Gap 3 is a one-character gap that follows the last record area on the track. This character is either a BCD 2 or a BCD 4, depending on the mode of operation.

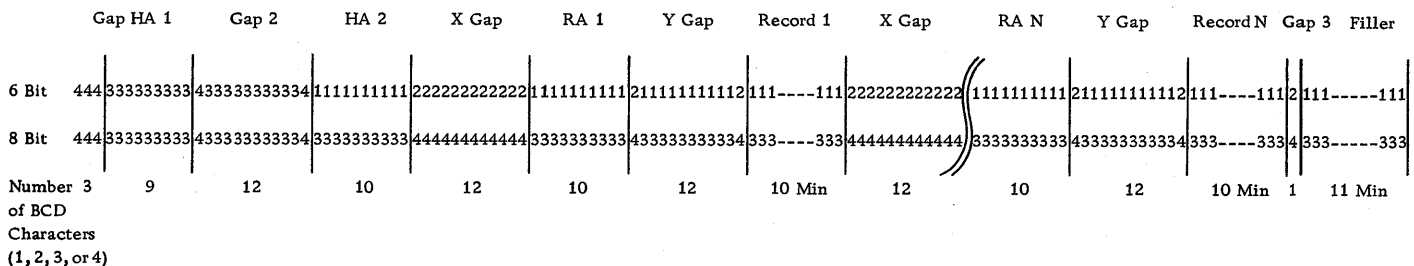


Figure 15. Format Track Layout

Filler: The filler is automatically written by the 7631 following Gap 3 and must be a minimum of 11 characters of BCD 1's or BCD 3's.

Format tracks can be written for either one mode of operation or the other, never as a mixture of both modes, excepting for the track identification area, which is always written in the eight-bit mode.

For 7090/7094 systems operations, it is desirable to use home address 2 (HA 2) and record addresses (RA) consisting of six characters (one word). All data record areas should also be multiples of 6 characters. To find the data capacity of a track, 46 characters must be subtracted from the total track capacity of 2,880 characters. The 46 characters subtracted consist of:

Track Identification	24 characters
HA 2, X Gap	<u>22</u> characters
	46 characters

In addition, 38 characters must be subtracted for each record address area as follows:

X Gap, RA, Y Gap	34 characters
Data Record Synchronization Characters	<u>4</u> characters
	38 characters

Or in the case of the last record:

RA, Y Gap	22 characters
Gap 3	1 character
Filler (inserted automatically by 7631)	11 characters (minimum)
Data Record Synchronization Characters	<u>4</u> characters
	38 characters

Example: Three records per track, six-bit mode.

$2880 - 46 - 38 (3) = 2720$ characters.

Word Capacity: $2720 \div 6 = 453\text{-}2/3$ words.

The $453\text{-}2/3$ words should be reduced to 453 words to provide full words, and this 453 word capacity may be allotted in any desired manner among the three records. The extra $2/3$ word will be provided for by increasing the filler area at the end of the track from 11 characters to 15 characters.

A program example of writing a format track may be found in the "Appendix."

Write Home Address

The conditions necessary for this operation are that the home address switch on the 7631 is on, a prepare to verify (home address) operation order is issued to the file control, and the write command immediately follows. The file control compares the physical address portion of the home address on the track and begins the write operation at the beginning of the HA 2 area. The first characters must be the home address identifier of the particular track. The home

address identifier must be a minimum of two characters. If desired, this area may be extended to six characters to match the word length of the 7090 and 7094 systems. The number of characters requested by the 7631 for the HA identifier is determined by the number of 1's that were previously written on the format. All characters of the HA identifier after the second are nonsignificant and are not a part of address compare.

This operation continues, with the file control detecting the gap between the HA 2 and the first record address. On detection of the gap, the file control writes the three-digit check character. The operation continues writing record addresses and records to the end of the track.

If a stop signal occurs before sensing the end of track, data transmission stops but the file control continues writing blanks to the end of the track.

Write Track with Addresses

Conditions necessary for this operation are a prepare to verify (track with addresses) order, followed by a write command. Under control of the prepare to verify (track) order, the file control searches the data track for a home address and compares this address bit for bit against the address previously issued with the prepare to verify (track) command. If the home address fails to compare, the file control issues an immediate unusual end and indicates in its status word a no-record-found bit. Upon a successful home address compare, the file control transfers the record address and proceeds in the usual manner. The file control continues filling the record area with data (both records and addresses) from the computer. The file control also supplies the check characters to be written at the end of each area. When the last check character area is reached, a normal end will be issued to the computer if no error conditions have been detected. Otherwise, unusual end results. If the computer signals a stop in the middle of a record, data transmission stops, but the file control writes blanks to the end of the record area in which it is operating, then writes the check characters, and signals normal end.

Write Single Record

Conditions necessary for this operation are that a prepare to verify (single record operation) order is issued to the file control, followed by a write command. The record address area is recognized in the file control by sensing the end of a long gap in the format. Upon finding a record address area, the file control reads off the address contained in the area and compares it bit by bit with the address previously

supplied to the 7631 during prepare to verify (single record). If the address does not compare, the file control continues searching succeeding address areas and comparing the address contained in each. If the file control passes the index point twice without comparing the address, it registers the no-record-found status bit and issues an unusual end to the computer without transmission of data. Upon an address compare true, the file control causes the 7320 to write over the record immediately following the compared address. Data are furnished by the system. The file control automatically transmits the code check characters following the end of the record area as defined by the format track.

If a stop signal is received at some point in the record area, the file control continues to write the record, with blanks, until the end of the formatted area is reached. After the check characters are recorded, a normal end is issued to the system unless a data check has occurred, in which case unusual end would result.

Write Track Without Addresses

The conditions necessary for this operation are that a prepare to verify (track without addresses) order is followed by a write command. The address received with the prepare to verify (track without addresses) order is compared with the home address transmitted from the 7320. If the home address fails to compare, the no-record-found bit is registered and unusual end is issued to the system. If the address compares true, the file control skips the first address area into the record area and writes the record. The file control continues skipping addresses and writing the records until the end of the last record on the track is sensed. A normal end is issued to the system if no error conditions occur during data transfer. In case of a parity error, the operation will be terminated at the end of the record in which the error was detected and unusual end is issued.

If the computer signals a stop in a record, data transmission stops, but the file control continues writing blanks to end of the record area in which it is operating, then writes the check characters and signals normal end.

Read or Write--Cylinder

Operation in the cylinder mode is an optional feature of the 7631. A cylinder mode read or write is set up by having the computer send a prepare to verify (cylinder operation) order to the file control. The address issued with the order is the home address of the track on which the operation is to start. The

home address is compared bit by bit in the 7631 after the read or write is received.

On a compare equal, the data transfer operation begins with all of the records on the addressed track being read or written and with the record addresses ignored in the same manner as a track-without-addresses operation. Rather than causing an end signal when the last record of the track has been processed, the 7631 sends a new head address to the 7320 and reading or writing continues. The head address sent to the 7320 is one address higher than the previous head address. By indexing one head address on each drum revolution, the 7631 continues reading or writing until the entire cylinder of information has been processed. The end signal is generated in the 7631 when the highest order head of the cylinder has been operated on.

If the computer signals a stop in a record, data transmission stops but, if reading, the file control continues to the end of record, and then compares check characters; if writing, the file control writes blanks to end of record in which it is operating, then writes the check characters and signals normal end.

No wraparound feature is included in cylinder operation to cause operation to begin again at the low-order head after the high-order head has completed its reading or writing.

Write Check

Each write operation has an associated write check operation, the use of which is optional and under program control. The operation requires the following sequence of orders and commands:

Prepare to Verify . . .	XXXXXXXXXX
Write	-----
Prepare to Write Check	XXXXXXXXXX
Write	-----

The 7631 compares the data recorded in the addressed record, bit by bit, with the write data from the system, at the same time generating check characters that will be compared with those previously generated and recorded on the track. The end of this operation is the same as a true write operation. A compare error during a write check sets the data compare check bit in the status data.

During a write check operation on a format track, the format gap detector circuits in the 7631 are checked to determine if they are within their specified tolerance. A file control circuit check is noted if the circuits do not meet specifications.

On reception of a stop signal, the 7631 continues comparing data already received, then continues till end of the record area and issues a normal end signal.

READ OPERATIONS

Read Home Address

This operation requires that a prepare to verify (home address) is sent to the 7631 and that a read command follows. The most useful application of this operation is to recover tracks of information in a file dump operation. The 7631 compares the physical address portion of the home address and begins reading with the home address identifier. All address and record data of the track are read. The termination of this operation occurs when the 7631 senses the index point. At that time either normal end or unusual end is issued, depending on the state of the data check. The computer may terminate the operation earlier by issuing a stop. Upon receipt of the stop, the 7631 terminates data transmission and internally completes reading of the record on which it was operating at the time of the stop. At the end of the particular record, the 7631 sends either normal end or unusual end, depending on the state of data check.

Read Track with Addresses

Conditions necessary for this operation are that a prepare to verify (track) order is issued to the 7631, followed by a read command. The file control begins the operation by comparing the home address that accompanied the prepare to verify (track) order against the recorded home address on the selected track. A failure to compare causes a no-record-found signal to be set in the status data and causes an unusual end to be issued to the system. A successful compare permits the 7631 to begin reading at the first record address area. The record address is read out in its entirety and sent to the system, followed by the record and then the next address and record, and so on. The operation terminates when the 7631 senses that it has completed comparing the check characters of the last record of a track. At that time, a normal end or unusual end is issued, depending on the state of data check. A stop signal prior to the logical end of this operation causes the 7631 to stop data transmission and signal a normal end at the end of the record on which it is operating at the time of the stop signal.

Read Single Record

This operation requires completion of a prepare to verify (single record) order and read command. As with write (single record) operation, the read (single record) operation has no predetermined starting point on the drum, that is, when the instruction is

received by the 7631, it immediately begins searching for a record address. Upon finding one, the 7631 does a bit-by-bit comparison. A failure to compare causes the control to continue searching on the next record address. No record found is registered if the 7631 passes the index point twice in its search for a particular record. Upon obtaining an address compare true, the 7631 causes the record immediately following that address to be read and the data to be sent to the system. The 7631 verifies the legality of the check characters following the end of the record and sends the normal end or unusual end at that time. A stop signal prior to the logical end of this operation causes the 7631 to stop data transmission and to signal a normal end at the end of the record.

Read Track without Addresses

This operation requires that a prepare to verify (track) and a read command, in that sequence, be executed. The 7631 waits for the home address area before beginning to compare the address supplied with the prepare to verify order against the recorded home address. A compare failure causes the 7631 to register no record found in the status word. If the address compares successfully, 7631 carries out the read-track operation by skipping over the first record address and reading the first record. The operation continues with addresses ignored by the 7631 and only record data being sent to the system. The operation ends when the 7631 finishes the last record of the track. At that time the appropriate end signal is issued. An early end may occur because of a system stop signal. In that case, the 7631 finishes the record on which it is operating and issues a normal end or unusual end, as the case may be.

CHECKING

The 7631 File Control checks for twelve individual error conditions possible in the operation of disk or drum storage. The sensing of any one of these conditions causes an unusual end signal to be sent to the computer.

Parity or Character Check: The 7631 is an odd-parity machine. As characters are transferred from the computer, the bit count of each is checked. If an even number is detected, this check bit as well as the summary data check bit, will be set into the status data. The character code check is made by generating three check characters for each address and record as bits are read from the surface during

a read operation. These newly generated characters are compared bit by bit with those previously generated and recorded in the gap following each address and each record during the write operation. Failure to compare will indicate the occurrence of an error.

Response Check: The response check indicates that a character from the system was not received by the 7631 within the allotted time. Response check can only occur as a result of a read or write operation.

Data Compare Check: Data compare check can occur only during a write check operation. The condition indicates that a compare error was detected somewhere during write check. During a write check operation, data are read from the surface and compared bit by bit with those transferred from the computer.

Format Check: The format check occurs during either format write or a write check of a format track. The cause may be either an illegal code (any but a BCD 1, BCD 2, BCD 3, or BCD 4) or because a stop signal was not sent to the file control before the index point was sensed.

No Record Found: The no-record-found indication occurs if the file control fails to locate the track or record address issued to it on a prepare to verify order.

Invalid Sequence: The invalid sequence condition can occur during write operations in two ways. In one case, it occurs when a write command is received by the file control without a preceding and properly executed prepare to verify or prepare to write format order. In the second case, invalid sequence occurs when a write check order is preceded by other than a prepare to verify order, prepare to write format order, and properly executed write command. During reading, a prepare to verify is the only legal order that can precede the read command.

Invalid Code: The invalid code indication occurs when the file control is given an order that cannot be performed.

Access Inoperative: This indication occurs when the access mechanism or drum fails to respond to an order. The unit may be mechanically out of order or may not exist.

Access Not Ready: The access not ready indication shows that the addressed 1301 access is in motion from some prior seek order. The 7320 drum cannot cause an access not ready indication.

Disk/Drum Storage Unit Circuit Check: This check indicates a circuit failure in the 1301 Disk Storage or 7320 Drum Storage.

File Control Circuit Check: This check occurs because of a malfunctioning gap detection circuit, address comparison circuit, check character code generator, format skew detector, or timing rings in the 7631.

Invalid Address: Invalid address is set when an address greater than 0399 is sent to the drum during a seek operation.

INSTRUCTION TIMES

Read and write operations vary in duration, depending on the length of the data field involved. In general, the 7320 Drum Storage should take one half the time taken by the identical read or write operation on the 1301 Disk Storage.

Service requests may occur as often as once every 4.8 microseconds with the 7320 Drum Storage when six-bit characters are transferred. The 7631 checks for an overrun condition 3.32 microseconds after service request.

Control and sense operations are of the same duration in the 1301 Disk Storage and the 7320 Drum Storage.

CONTROL PANEL

The control panel of the 7631 is primarily intended for maintenance simulation. The panel is mounted on the right front cover. The control panel has an exposed section, and a hidden section intended only for customer engineering usage. On the exposed segment are 122 indicator lights that reflect the status of data and controls within the 7631. Operator switches are available in a light and switch assembly above the indicator section of the control panel. The customer engineering section of the panel is covered and contains 35 switches for simulation of data, commands, and responses from the channel and responses from the drums or disks.

Switches and Lights

Power-On Key: This key supplies dc voltages to the 7631, 1301's, and 7320's and ac voltages to the disk storage and drum motors and blowers. When the switch is pressed, power is supplied to the first disk

or drum storage for a power-on sequence. When the first disk storage has completed its power-on sequencing, a signal is sent to the next one to start the power-on sequence, and so on.

Power-On Light: When on, this light indicates that power is supplied to the 7631, 1301's and 7320's.

Power-Off Key: This key removes dc and ac operating voltages from the 7631 File Control and the 1301 Disk Storage and 7320 Drum Storage units and

initiates a power-off sequence for the 1301 and 7320 units.

DC-Off Key: This key removes dc operating voltages from the 7631 File Control and the 1301 and 7320 units.

DC-On Light: When on, this light indicates that dc operating voltages are present on the 7631, 1301's and 7320's.

HAO Switch: This switch must be on for logical execution of a home address operation.

Write Inhibit Switch and Light: The write inhibit toggle switch allows the operator diagnostic programmer to perform a write sequence of operations without actual writing, thus not disturbing the customer's data. The associated light indicates that this write inhibit condition is present.

Thermal Light: This light in the 7631 is energized if the temperature in the gates exceeds 115°F. While the light is on, the power-on switch of the 7631 is not effective. Power is down until the temperature returns to specified limits.

Fuse Light: The fuse light indicates a blown fuse or tripped circuit breaker in the 7631.

Test Mode Light: This light is for customer engineering use; when on, it indicates that the 7631 and the attached 1301's and 7320's are not available for normal customer use.

WRITE A FORMAT AT CYLINDER 0000, SINGLE RECORD PER TRACK

CPU PROGRAM

00051	1	00000	0	00223	TCH CHECK	INTERRUPT TRANSFER
00100	0500	00	0	00320	START CLA TPAD1	SET UP TRAP
00101	0601	00	0	00021	STO 17	ADDRESS
00102	0564	00	0	00317	ENB ENCHD	ENABLE CHAN D
00103	-0541	00	0	00150	RSCD STFMT	START FORMAT
00104	2	00001	1	00104	PLAY TIX *,1,1	KEEP CPU
00105	1	77776	1	00104	TXI *-1,1,-2	BUSY
00106	0000	00	0	00000	HTR **	NEVER STOP HERE
00107	-0641	00	0	00307	TRAP1 SCHD TEMP1	CHECK FOR
00110	0500	00	0	00307	CLA TEMP1	CORRECT
00111	0340	00	0	00310	CAS SCHD1	CHANNEL
00112	0020	00	0	00114	TRA *+2	STOP
00113	0020	00	0	00115	TRA *+2	OK
00114	0000	00	0	00114	HTR *	ERROR
00115	0500	00	0	00321	CLA TPAD2	SET UP NEW
00116	0601	00	0	00021	STO 17	TRAP ADDRESS
00117	-0541	00	0	00143	RSCD WRCKF	START WRITE CHECK
00120	0760	00	0	00014	RCT	RESTORE
00121	0020	00	0	00104	TRA PLAY	CPU BUSY
00122	0000	00	0	00000	HTR **	NEVER STOP HERE
00123	0000	00	0	00123	TRAP2 HTR *	CORRECT STOP

CHANNEL PROGRAM

WRITE FORMAT TRACK

00124	0000	01	2	00312	WRFMT XMT RSTRT,,1	POST RESTART ADDRESSES
00125	0	00000	0	00126	PZE WRFMT+2	
00126	-2	40000	2	00055	LCC 45	SET UP FOR 460 WORDS
00127	2	40000	0	00260	CTLW DWRF	WRITE FORMAT CYL 000
00130	-0000	04	0	00262	COPYS CPYP FTWD1,,4	TRACK IDENTIFICATION
00131	-0000	04	0	00266	CPYP FTWD2,,4	HA2,X GAP,2 CHAR OF RA
00132	-0000	01	0	00266	CPYP FTWD2,,1	RA
00133	-0000	01	0	00272	CPYP FTWD6,,1	RA,4CHAR OF Y GAP
00134	-0000	01	0	00266	CPYP FTWD2,,1	Y GAP
00135	-0000	01	0	00273	CPYP FTWD7,,1	2 CHAR Y GAP,4 CHAR RCRD
00136	-0000	12	0	00274	CPYP FTWD8,,10	DATA RECORD AREA
00137	-2	40000	0	00136	TDC *-1	46 TIMES FOR 460 WORDS
00140	-0000	06	0	00274	CPYP FTWD8,,6	6 MORE DATA WDS FOR 466
00141	-1	00001	0	00306	CPYD FTWD9,,1	6 FOR 3 GAP
00142	3	40000	0	00142	WFEND TWT *	

WRITE CHECK FORMAT TRACK

00143	0000	01	2	00312	WRCKF	XMT RSTRT,,1	POST RESTART ADDRESS
00144	0	00000	0	00145		PZE WRCKF+2	
00145	-2	40000	2	00055		LCC 45	
00146	2	40000	0	00254		CTLW DWRC1	
00147	1	00000	0	00130		TCH COPYS	
00150	0000	01	2	00312	STFMT	XMT RSTRT,,1	POST RETURN ADDRESS
00151	0	00000	0	00155		PZE STFMT+5	
00152	0000	01	2	00311		XMT RET,,1	
00153	0	00000	0	00124		PZE WRFMT	
00154	-2	40000	2	00011		LCC 9	NUMBER OF RETRIES
00155	2	00000	0	00246		CTL DSEK1	SEEK ACC 0, MOD 0
00156	0000	00	0	00156		WTR *	WAIT FOR SEEK COMPLETE

CPU PROGRAM

00157	0564	00	0	00317	BEGIN	ENB ENCHD	ENABLE TRAP
00160	-0541	00	0	00165		RSCD GO	START CHANNEL D

CPU IS NOW FREE TO PERFORM OTHER TASKS WHILE THE 7909 FINDS THE RECORD AND PROCESSES IT

00161	2	00001	1	00161		TIX *,1,1	WAIT FOR TRAP
00162	1	77776	1	00161		TXI *-1,1,-2	
00163	0000	00	0	00163	DONE	HTR *	JOB COMPLETE
00164	0000	00	0	00164	HELP	HTR *	CPU STOPS HERE ON ERROR

CHANNEL PROGRAM

00165	0000	01	2	00311	GO	XMT RET,,1	POST RESTART ADDRESS
00166	0	00000	0	00173		PZE WRITE	
00167	0000	01	2	00312		XMT RSTRT,,1	
00170	0	00000	0	00171		PZE GO+4	

SEEK DRUM ADDRESS 0038 AND WAIT FOR ATTENTION SIGNAL

00171	2	00000	0	00250		CTL DSEK2	SEEK DRUM ADDRESS 0038
00172	0000	00	0	00172		WTR *	WAIT FOR ATTENTION
00173	-2	40000	2	00011	WRITE	LCC 9	NUMBER OF RETRIES
00174	0000	01	2	00312		XMT RSTRT,,1	RESTART ADDRESS
00175	0	00000	0	00176		PZE WRITE+3	

WRITE 466 WORDS AT RECORD ADDRESS 003800

00176	2	40000	0	00252		CTLW DVSR	VERIFY SINGLE RECORD
00177	-0003	43	0	10000		CPYP DATA1,,227	WRITE 466 WORDS
00200	-0002	43	0	15000		CPYP DATA2,,163	
00201	-1	00114	0	20000		CPYD DATA3,,76	

00202	3	00000	0	00313	LAR BRANC	CHECK FOR WRITE CHECK DONE
00203	-1	60001	2	00213	TCM READ,,1,6	GO TO READ
00204	3	00000	0	00316	LAR ONE	
00205	3	00000	2	00313	SAR BRANC	
00206	-2	40000	6	00173	WRCHK LCC WRITE,4	RELOAD NUMBER OF RETRIES
00207	0000	01	2	00312	XMT RSTRT,,1	RESTART ADDRESS
00210	0	00000	0	00211	PZE WRCHK+3	

WRITE CHECK RECORD AT RECORD ADDRESS 003800

00211	2	40000	0	00256	CTLW DWRC2	
00212	1	00000	0	00177	TCH WRITE+4	DO WRITE CHECK
00213	-2	40000	6	00173	READ LCC WRITE,4	RELOAD RETRIES
00214	0000	01	2	00312	XMT RSTRT,,1	RESTART ADDRESS
00215	0	00000	0	00216	PZE READ+3	

READ RECORD AT RECORD ADDRESS 003800

00216	2	00000	2	00252	CTLR DVSR	VERIFY SINGLE RECORD
00217	-1	00722	0	25000	CPYD DATA4,,466	READ FULL RECORD
00220	0000	01	2	00021	XMT 17,,1	
00221	0020	00	0	00163	TRA DONE	
00222	3	40000	0	00222	TWT *	WRITE-WRITE CHECK-READ COMPLETE - TRAP CPU FOR PROCESSING

7909 INTERRUPT ROUTINE

00223	-1	00004	2	00225	CHECK TCM *+2,,100	WAS THIS ATTENTION 1
00224	1	00000	0	00233	TCH ERROR	NO
00225	2	40000	2	00000	SNS	YES
00226	-1	00001	0	00314	CPYD SENSE,,1	GET FIRST SENSE WORD
00227	3	00000	0	00314	LAR SENSE	
00230	-1	60120	2	00232	TCM *+2,,1010000,6	ACCESS 0, MODULE 0
00231	-2	00000	2	00000	LIP	WAIT FOR CORRECT ATTENTION
00232	1	00000	6	00311	LIPT RET,4	START WRITE
00233	-2	40000	0	00240	ERROR TDC *+5	REDUCE TRIES
00234	0000	01	2	00021	XMT 17,,1	TEN TRIES DONE - TRAP CPU
00235	0020	00	0	00164	TRA HELP	FOR HELP
00236	3	40000	0	00237	TWT *+1	PREPARE TO RETURN WITH STC
00237	1	00000	6	00312	LIPT RSTRT,4	
00240	-1	00040	2	00245	TCM RTRN,,100000	CHECK FOR I-O CHECK
00241	-1	00020	2	00234	TCM ERROR+1,,10000	SEQU CHECK CALL CPU
00242	-1	00010	2	00245	TCM RTRN,,1000	UNUSUAL END
00243	-1	00001	2	00234	TCM ERROR+1,,1	ADAPTER CHECK CALL CPU
00244	1	00000	0	00234	TCH ERROR+1	POSSIBLE MULTIPLE CONDITION CALL CPU
00245	1	00000	6	00312	RTRN LIPT RSTRT,4	TRY AGAIN

7631 ORDERS

00246 +101212121212 DSEK1 OCT 101212121212 DSEK - 80
00247 +120112120000 OCT 120112120000 00-0001-00
00250 +101212121212 DSEK2 OCT 101212121212 DSEK - 80
00251 +031012120000 OCT 031012120000 00-0038-00
00252 +100212121212 DVSR OCT 100212121212 DVSR - 82
00253 +031012120000 OCT 031012120000 00-0038-00
00254 +100612121212 DWRC1 OCT 100612121212 DWRC - 86
00255 +120112120000 OCT 120112120000 00-0001-00
00256 +100612121212 DWRC2 OCT 100612121212 DWRC - 86
00257 +031012120000 OCT 031012120000 00-0038-00
00260 +100312121212 DWRF OCT 100312121212 DWRF - 83
00261 +120112120000 OCT 120112120000 00-0001-00

FORMAT AREAS

00262 040404030303 FTWD1 BCD 44443333333334333333333334
00263 030303030303
00264 040303030303
00265 030303030304
00266 010101010101 FTWD2 BCD 11111111
00267 010101010202 FTWD3 BCD 11111222
00270 020202020202 FTWD4 BCD 12222222
00271 020202020101 FTWD5 BCD 12222111
00272 010102010101 FTWD6 BCD 11121111
00273 010201010101 FTWD7 BCD 11211111
00274 010101010101 FTWD8 BCD 51111111111111111111111111111111
00275 010101010101
00276 010101010101
00277 010101010101
00300 010101010101
00301 010101010101 BCD 51111111111111111111111111111111
00302 010101010101
00303 010101010101
00304 010101010101
00305 010101010101
00306 020101010101 FTWD9 BCD 12111111

CONSTANTS

00307 0 00000 0 00000 TEMPL PZE
00310 0 00142 0 00142 SCHD1 PZE WFEND , ,WFEND
00311 0 00000 0 00000 RET PZE ** PROCEED ADDRESS
00312 0 00000 0 00000 RSTRT PZE ** CHANNEL RETURN ADDRESS
00313 0 00000 0 00000 BRANC PZE ** WRITE CHECK CONTROL
00314 00314 SENSE BSS 2 LOCATION FOR SENSE WORDS
00316 +0000000000001 ONE DEC 1
00317 +0000000000010 ENCHD OCT 10
00320 0020 00 0 00107 TPAD1 TRA TRAP1
00321 0020 00 0 00123 TPAD2 TRA TRAP2

VARIABLE RECORD LENGTH FORMULA AND
PARTIAL CAPACITY TABLE

Six-Bit Character Records

$$\frac{2834}{\text{Record Length} + 38} = \text{No. Records per Track}$$

<u>Record Length (Chars)</u>	<u>Record + Address (Chars)</u>	<u>Records per Track</u>	<u>Track Remainder</u>
6	44	64	18
12	50	56	34
18	56	50	34
24	62	45	44
30	68	41	46
60	98	28	90
90	128	22	18
120	158	17	148
240	278	10	54
360	398	7	48
480	518	5	244
720	758	3	560
1440	1478	1	1356
1800	1838	1	996
2400	2438	1	396
2796	2834	1	0

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