File No. 7040/7044-01
GA22-6649-6

IBM Systems Reference Library

IBM 7040-7044 Principles of Operation

This manual presents information about the operation and use of the IBM 7040 and 7044 Data Processing Systems. It provides a reference and guide for those familiar with these systems. The reader should be familiar with:

IBM 7040/7044 Systems Summary	A28-6288
IBM 7040/7044 Operator's Guide	A22-6741
IBM 7040/7044 Bibliography	A28-6289

Each section of the manual contains related machine or functional operations. The sections are independent and need not be used in the order in which they appear.

A list of both standard and optional features and units is included in the introduction. Detailed descriptions do not state whether a feature or unit is standard or optional.

SEVENTH EDITION

This is a reprint of Form A22-6649-5 incorporating changes released in the following Technical Newsletter:

FORM NUMBER	PAGES AFFECTED	DATE
N22-0206	52, 52.1	September 10, 1965

Specifications contained herein are subject to change from time to time. Any such changes will be reported in subsequent revisions of Technical Newsletters.

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This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. B98 PO Box 390, Poughkeepsie, N.Y. 12602. A form is provided at the back of this publication for reader's comments. If the form has been removed comments may be sent to the above address..

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IBM 7044 Data Processing System

The IBM 7040 and 7044 Data Processing Systems are highly flexible systems that may be applied to a wide range of data processing needs. Features that make the systems expandable as the user's needs grow include:

Processing Unit with Four Optional Instruction Sets
Core Storage with Optional Speed and Capacity
Optional Input-Output Device Configurations

The basic 7040 or 7044 system includes one input-output channel, data channel A, whose operation is not overlapped with processing unit operation. IBM punched card equipment, output printers, magnetic tape units, on-line IBM 1401 Data Processing Systems, and Tele-processing equipment may be attached to this channel.

Overlapped input-output and processing is available by using the IBM 7904 Data Channel. An IBM 1302 Disk Storage, 7320 Drum Storage, IBM 7750 or 7740 Programmed Transmission Control, Direct Data Connection, IBM Magnetic Tape Units, and Tele-processing equipment as well as IBM 7090, 7094, 7094 II systems may be attached to 7904 Data Channels.

The 7040 system uses the IBM 7106 Processing Unit, which has a basic core storage cycle of 8.0 microseconds. The 7044 system uses the IBM 7107 Processing Unit, which has a basic core storage cycle of 2.0 microseconds. Both the 7040 and 7044 systems use 37-bit words that are moved in parallel among the processing unit, core storage, and data channels. Each word contains 36 data bits and a check (parity) bit for that word.

Summary of Optional Units and Features

Processing Units

UNIT	WORD CAPACITY	BASIC CYCLE (MICROSECONDS)
7106-1 Processing Unit	4,096	8.0
7106-2 Processing Unit	8,192	8.0
7106-3 Processing Unit	16,384	8.0
7106-4 Processing Unit	32,768	8.0
7107-1 Processing Unit	8,192	2.0
7107-2 Processing Unit	16,384	2.0
7107-3 Processing Unit	32,768	2.0

OPTIONS	COMMENTS
Extended Performance Instruction Set	Three index registers and character-handling instructions
Floating Point Instruction Set	Single-precision instructions
Double-Precision Floating Point Instruction Set	Double-precision instructions; Floating Point option is prerequisite
Memory Protection	
Storage Clock — Interval Timer	
Channel A Adapters:	
1401 Data Processing System	Models B through F. Feature code 7080 (serial I/O adapter) required on 1401
1414-1, -2 or -7 Input/Output Synchronizer	One of these units only
1414-3, 4, 5, or 8 Input/Output Synchronizer, or 1622 Card Read Punch	Up to three of these units
7904 Data Channel Attachment	First channel (B) only
7904 Additional Data Channel Attachments	Maximum of three (channels C, D, and E)
IBM 7904-1 Data Channel	Single channel
IBM 7904-2 Data Channel	Double channel
7904 Data Channel Tape Systems	
1414 Tape Adapter	1414-1, -2, or -7 Input/Output Synchronizer
7904 Control Adapter	7631 File Control, 1414-6 Input/Output Synchronizer, or 7750 Programmed Transmission Control. Only one of these systems may be used on a 7904 Data Channel
Direct Data Adapter	One per 7904 Data Channel (four per system). Permits attachment of Analog to digital converters, Telegraph facilities, Telephone facilities, Telemetric devices, radar equipment as well as other computer systems to the 7040/7044.
Direct Couple	Permits direct coupling of 7040 to 7090/7094/7094 II Systems and 7044 to 7094/7094 II Systems (see A22-6803)

Input-Output Devices

OPTIONS	COMMENTS
1414-1 Input/Output Synchronizer	Tape Control Unit
729 II Magnetic Tape Unit 729 IV Magnetic Tape Unit 729 V Magnetic Tape Unit (with 800 CPI) 7330 Magnetic Tape Unit (with intermix feature)	Maximum of ten tape units (all models)
1414-2 Input/Output Synchronizer	Tape Control Unit
7330 Magnetic Tape Units	Maximum of ten
1414-3 Input/Output Synchronizer	Card control unit
1402-2 Card Read Punch 1403-1, -2, or -3 Printer	
1414-4 Input/Output Synchronizer	Card control unit (plus six serial buffers)

OPTIONS	COMMENTS
1402-2 Card Read Punch	
1403-1, -2, or -3 Printer	
1009 Data Transmission Unit	
1011 Paper Tape Reader	
1014 Remote Inquiry Unit	
Telegraph type units	
Column binary feature	
1414-5 Input/Output Synchronizer	Six serial buffers (channel A only)
1009 Data Transmission Unit	
1011 Paper Tape Reader	
1014 Remote Inquiry Unit	
Telegraph type units	
1414-6 Input/Output Synchronizer	Six serial buffers. (The 1414-6 may be attached to the 7904 Data Channel only.)
1009 Data Transmission Unit	
1011 Paper Tape Reader	
1014 Remote Inquiry Unit	
Telegraph type units	
1414-7 Input/Output Synchronizer	Tape Control Unit
729 II Magnetic Tape Unit	Maximum of ten tape units (all models)
729 IV Magnetic Tape Unit	
729 V Magnetic Tape Unit	
729 VI Magnetic Tape Unit	
7330 Magnetic Tape Unit (with intermix feature)	
1414-8 Input/Output Synchronizer	Printer Control Unit
1403-1, -2, or -3 Printer	
1622 Card Read Punch	Channel A only
7631 File Control, Models 2, 3, 4	Maximum of two per system
1301-1, -2 Disk Storage	1 array }
1302-1, -2 Disk Storage	2 arrays } (maximum of five)
7320 Drum Storage	
7750 Programmed Transmission Control	Tele-processing control
65/66 Data Transceiver	
1009 Data Transmission Unit	
1013 Card Transmission Unit	
7701 Magnetic Tape Transmission Terminal	At remote end
7702 Magnetic Tape Transmission Terminal	
Standard Telegraph Terminals	
1050 Communications Systems	
7741 Processing Unit (7740 System)	
1311 Disk Storage Units	
7701 Magnetic Tape Transmission Terminals	
7702 Magnetic Tape Transmission Terminals	
1009 Data Transmission Units	
1013 Card Transmission Units	
65/66 Data Transceivers	
Appropriate Telegraph Terminals	
1050 Data Communication Systems	
1060 Data Communication Systems	
7710 Data Communication Units	
7750 Programmed Transmission Control Unit	
Another 7740 Communication Control System	

Off-Line Operation

Both the IBM 1402 Card Read Punch and the IBM 1403 Printer may be used off-line when not being used by the computer. Thus, it is possible to perform a card-to-card or a card-to-printer operation without removing either unit from the system. With a card-to-card operation in off-line mode, the 1403 Printer may be used by the computer in an on-line operation. The IBM 1414 Input/Output Synchronizer, to which the 1402 and 1403 are attached, contains the necessary switches and keys to perform the operations. Actual step-by-step procedures are contained in the *IBM 7040/7044 Operator's Guide*, Form A22-6741.

The IBM 7106 and 7107 Processing Units are a combination of many units. Each 7106 and 7107 contains the arithmetic and control unit, core storage, operator's console, data channel A, overlapped channel adapters, and power equipment for the entire 7040 or 7044 system. Data flow within the arithmetic and control unit is shown in Figure 1 and uses:

Storage Register (SR): This 37-bit register serves as input to the CPU from core storage for both instructions and data. The information uses 36 bits; the check bit uses the 37th position.

Accumulator Register (AC): This register uses 38 positions for holding one factor during arithmetic operations and for receiving the result from the adders. The contents of the accumulator may be shifted to the right or left. Two overflow positions (Q and P) are used to retain adder overflows. The P position is also used as the high-order bit in logic operations.

Multiplier-Quotient Register (MQ): During multiplication, this 37-bit register holds the multiplier and receives the low-order portion of the product. During division, the MQ holds the low-order portion of the dividend and receives the quotient. The MQ can also be shifted in conjunction with the AC or rotated within itself. A 37th (check bit) position is used during channel A operations.

Adder (AD): A 37-bit adder is used for all arithmetic operations and for address modification with index registers.

Program Register (PR): This ten-bit register holds the operation and count portions of instructions during execution and serves as control input for program execution.

Shift Counter (SC): This eight-bit counter is used for shift and variable length operations and as a part of the PR for select instructions.

Instruction Counter (IC): This 15-bit counter provides sequential instruction execution. The IC can be reset or modified by a transfer or trap operation.

Address Register (AR): The AR contains 15 bit positions and is used in transmission of operand and instruction addresses to core storage.

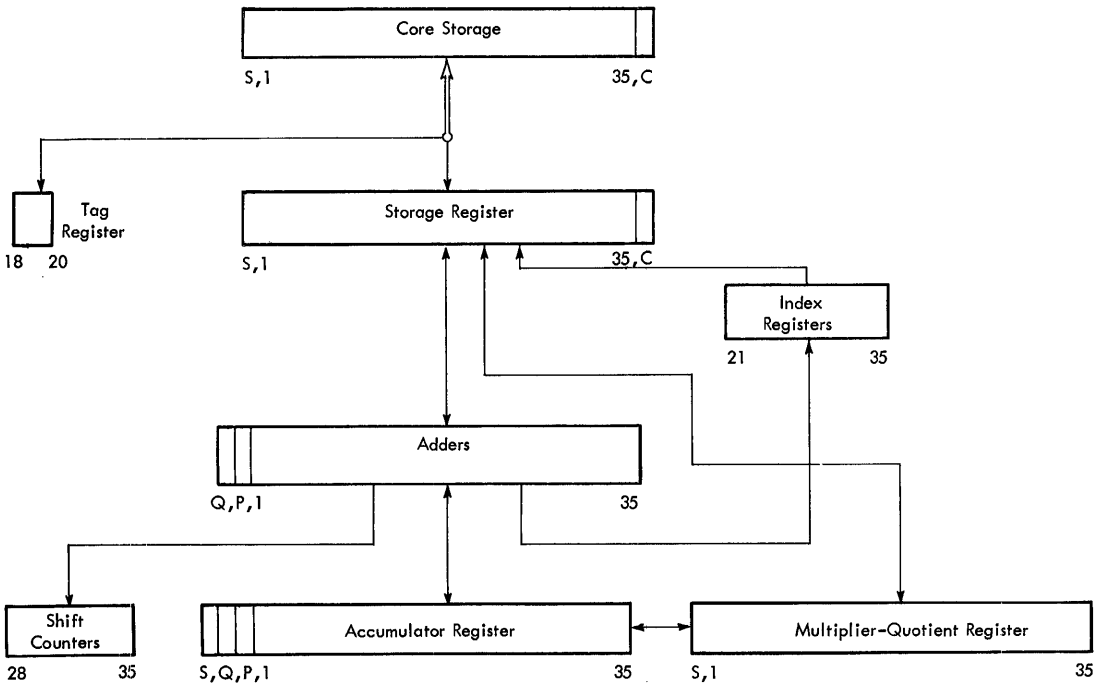


Figure 1. Simplified Processing Unit Data Flow

Index Registers (XR): Three 15-bit index registers are optional and are used for effective address modification and program control. The registers are called A, B, and C or 1, 2, and 4. The latter names are the octal addresses of the index registers. These addresses are in bit positions 18, 19, and 20 of the instruction and are called the tag field.

Tag Register (TR): This three-bit register holds the tag field of the instruction being executed.

Position Register: This register reflects positions 12-17 of the instruction being executed. Its uses include:

Position F (12-13):	Used to indicate indirect addressing
Position 14:	Used as a part of the operation code for select instructions
Positions 15-17:	Used with character handling instructions to specify which character is being used. Also used with select instructions to indicate interface addressing

Address Modification with Index Registers

One of the primary uses of index registers arises from their ability to modify instruction addresses. For modification to occur, the instruction must specify, by the appropriate bit configuration in the tag field, the register or registers that are to take part in the modifying activity. The instruction is then executed as if its address field contained the stated address minus the contents of the index register.

Assume that storage location 1000 contains the instruction ADD 2117 and that this instruction has a 2 in its tag field. If the contents of index register 2 are 117, the number stored in location 2000 (2117 minus 117) is added into the accumulator when the ADD instruction is executed. However, location 1000 still contains the instruction ADD 2117 in its original form. Address 2000 is called the effective address, and the process is called effective address modification; that is, the address of the instruction is modified in the CPU for execution purposes but is unaltered in storage.

Multiple Tag

An instruction may refer to more than one index register by placing multiple 1's in the tag field (Figure 2). Thus, a tag of three specifies index registers 1 and 2.

Tag Field		Index Registers Specified	
Binary	Octal		
000	0	None	
001	1	A	1
010	2	B	2
011	3	A & B	1 & 2
100	4	C	4
101	5	A & C	1 & 4
110	6	B & C	2 & 4
111	7	A & B & C	1 & 2 & 4

Figure 2. Multiple Tags

Care must be exercised when multiple tags are used. The use of multiple tags results in the "logical OR" of the contents of the specified index registers. For example, if a tag of three is given, the 15 positions of index register 1 are matched against the corresponding positions of index register 2. If *either* bit in a given position is a 1, the resulting logical sum will have a 1 in that position. If *both* positions are 0, the logical sum will have a 0 in that position.

Assume that index registers 2 and 4 contain 03204 (000011010000100) and 03061 (000011000110001), respectively. The instruction ADD 6521 with an index tag of 6 causes the number 03265 (000011010110101) to be subtracted from the address of the instruction and gives an effective address of 03234. Index register content remains unchanged except when the multiple tagged instruction deals directly with index registers, such as an SXA, PXA, TXI, etc. In this case, the *logical sum* of the index registers replaces the original contents of the registers.

Decrement Field

A group of instructions are used to test or alter the contents of an index register. The number used to test or alter an index register is contained in positions 3-17 of these instructions. These 15 bit positions are referred to as the decrement field.

Complement Arithmetic

When index registers are used for effective address modification, the contents of an index register are always subtracted from an instruction's address. Since neither the address of an instruction nor the content of an index register is associated with any algebraic sign, it is not possible to accomplish effective address modification by addition in any direct manner. This may be accomplished, however, by using complement arithmetic. The following definitions apply to this type of arithmetic:

1. The 1's complement of a binary number is the number that results by replacing each 1 in a number with a 0 and each 0 with a 1. Given the binary number 101, the 1's complement would be 010. Also, the sum of a binary number and its 1's complement is a binary number composed of all ones (101 + 010 − 111).

2. The 2's complement of a binary number is the 1's complement of a number increased by one. For the preceding example, the 2's complement of the binary number 101 would be 011. If the 2's *complement* of a number occupies an index register and is used to modify an address, the effective address is the *sum* of the index register contents and the address portion of the instruction. If the *true number* occupies the index register, the effective address is the *difference* between the index register contents and the address portion of the instruction.

Since both the contents of an index register and an instruction address are 15-bit numbers, all resulting carries to the sixteenth position will be lost.

Effective addresses are always formed in the computer by the addition of the 2's complement of the contents of the index register. This is an automatic feature. For example, if index register 4 contains the number 00005 and the instruction ADD 00015 with a tag of 4 is executed, the effective address is 00010:

2's complement of XR 4	111	111	111	111	011
ADD instruction address	000	000	000	001	101
Effective address (carry lost)	000	000	000	001	000

If index register 4 had contained the 2's complement of 00005 (that is, 77773), then the effective address would be 00022:

2's complement of XR 4	000	000	000	000	101
ADD instruction address	000	000	000	001	101
Effective address	000	000	000	010	010

Indirect Addressing

The concept of effective address modification is extended for a large group of instructions for which *indirect addressing* is provided. This extension is carried out in a simple way. Just as index registers are addressed with a tag, indirect addressing is specified or addressed by a *flag* (1 bits in both positions 12 and 13 of the instruction). With both positions 12 and 13 of an instruction containing ones, the instruction is executed in the following way:

An effective address is computed in the normal manner, by subtracting the contents of the specified index register, if one is specified, from the address part of the instruction. This is known as an *indirect effective* address. The computer then examines the location specified by *this* indirect effective address and uses the tag and address parts of this word to compute a *direct effective* address. The instruction is then executed as if its address field had contained this direct effective address with no flag or tag. The following examples illustrate this process.

Assume that the address part of location 00054 in core storage contains 00273. If the instruction ADD 00054 is executed, the contents of location 00054 will be added into the AC. However, if this same instruction had indirect addressing specified by 1 bits in both positions 12 and 13, the contents of location 00273 would be added into the AC.

Now, assume that index registers 1 and 2 contain 4 and 3, respectively, and that core storage location 00050 contains a 2 in its tag field and 00167 in its address part. If the instruction ADD 00054, with an index tag of 1 and indirect address flag specified, is executed, then the indirect effective address equals 00050 (address field of the ADD instruction minus the contents of XR 1). The direct effective address is 00164 (address part of location 00050 minus the contents of XR 2) and the contents of *this* location are added into the AC.

Data Channels

Data channels of the IBM 7040 and 7044 Data Processing Systems use a command word technique. In this technique, control of an I-O operation may pass from the central processing unit to the data channel, freeing the CPU to proceed with its stored program. The command word is the means of transferring control, and the I-O channel contains sufficient registers and counters to exercise this control. The channel is required to perform functions such as word counting, address changing, assembly of bytes into words, and disassembly of words into bytes.

Data Channel A Operation

Data channel A uses registers and data paths of the CPU to perform the I-O control function (Figure 3). No overlap exists between input-output and computer operation.

An I-O operation is started by a select instruction, which is decoded by the CPU. The output of the decoders is sent to the channel to select the input-output adapter and unit specified by the instruction. If the I-O unit is busy or not ready, the select instruction waits until it is free.

When selection is successfully completed, the channel ends operation on the select instruction and the CPU gets the next instruction for execution. This instruction is normally a reset and load channel (RCH) instruction, which specifies a location in storage that contains the channel command. Execution of the RCH places this command in the accumulator register (AC). The command specifies the number of words to be transmitted (word count positions 3-17) and the first storage address (positions 21-35) to be used for the read or write operation.

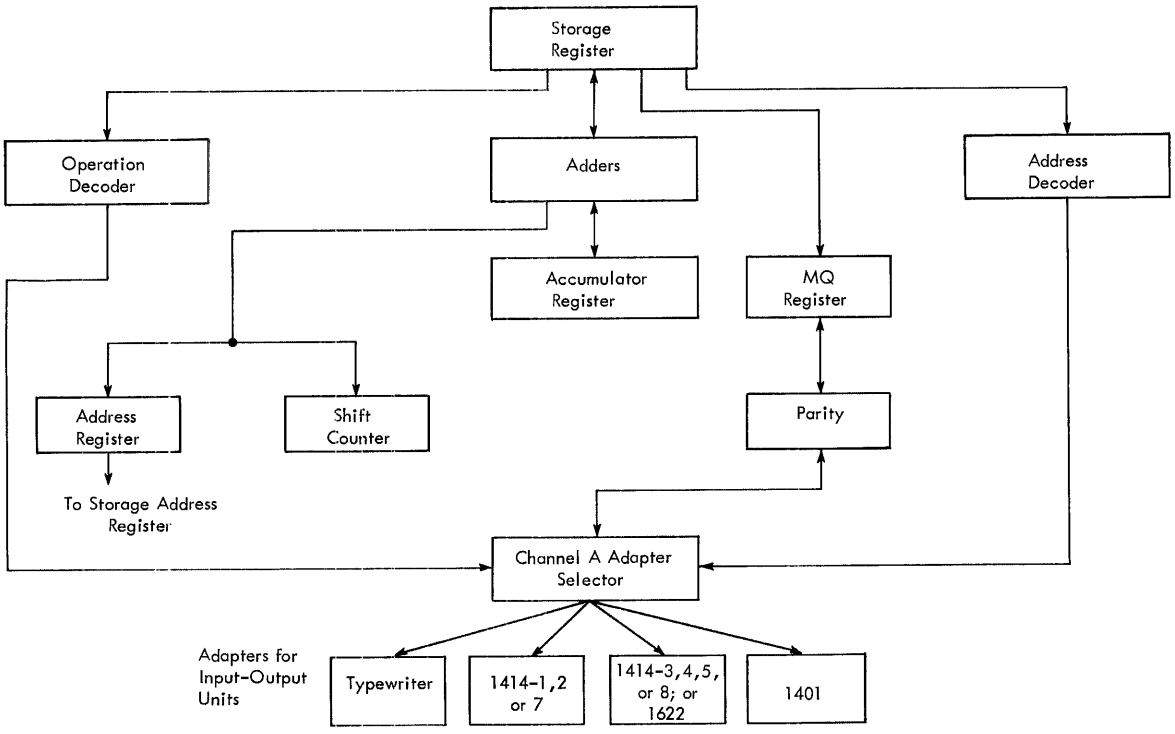


Figure 3. Data Flow for Channel A

The word count is tested for zero content and, when it is zero, the channel ends operation on the RCH and disconnects the input-output device. If the word count is not zero, the address part is sent to the address register (AR) and the shift counter (SC) is set to six. At this point, operation differs for read and write operations.

Read Operation: The I-O device sends seven-bit bytes (six data bits plus a parity bit) to the channel where the parity is checked and the parity bit is removed. The generated parity bits are accumulated to check word parity. If a parity check is detected, the channel redundancy check indicator is turned on and the I-O operation continues. The six data-bits are sent to the MQ register and placed in positions 30-35. The shift counter (set to six initially) is reduced by one and the next six data-bits are placed into MQ positions 30-35 as the MQ is shifted left six positions. Again the shift counter is reduced by one. This procedure continues until the shift counter is reduced to zero, which indicates that a full 36-bit word has been transferred to the MQ. The contents of the MQ are then placed in the storage register and stored at the address specified by the address register. Command modification is now accomplished by routing the data address to the adders, increasing the address by one, and returning the address to accumulator positions 21-35. The word count is reduced by one and returned to accumulator positions 3-17. If the word count is zero, the channel stops reading into storage and, when the end-of-record signal is received from the input device, the channel ends operation on the RCH and disconnects the input device. If the word count is not zero, the shift counter is again set to six and the channel repeats the procedure described.

Write Operation: A word is brought from the storage location specified by the address and is placed in the MQ register. MQ positions S, 1-5 are sent through parity generating circuits and then to the output device. The generated parity bits are accumulated to check word parity. After transmission of the first six data bits, the MQ is shifted left six positions and the shift counter is reduced by one. This procedure continues until the shift counter is stepped to zero, which indicates that 36 data bits have been transferred. Command modification is now accomplished by routing the data address to the adders, increasing the address by one, and returning the address to accumulator positions 21-35. The word count is reduced by one and returned to accumulator positions 3-17. The word count is tested for zero and, if it is zero, the channel ends operation on the RCH and disconnects the output device. If the word count is not zero, a new data word is required from storage; therefore, the address is sent to the address register and the shift counter is set to six. This procedure continues until the word count equals zero.

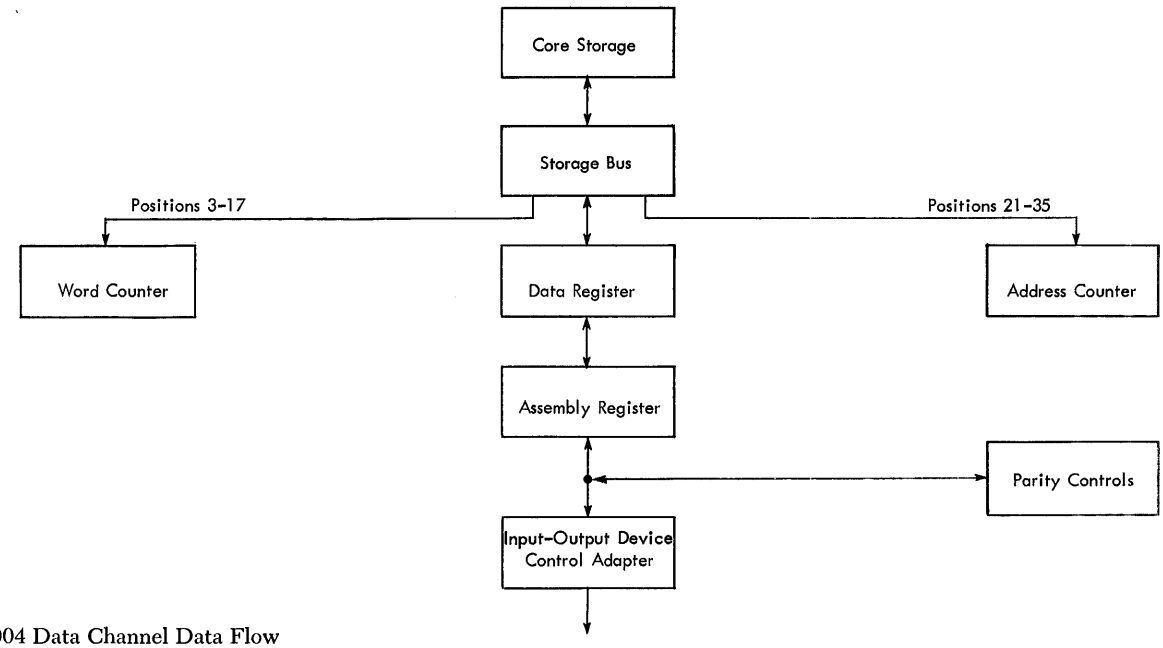


Figure 4. IBM 7904 Data Channel Data Flow

IBM 7904 Data Channel Operation

The IBM 7904 Data Channel is used with the 7040 and 7044 Data Processing Systems on channels B through E. These channels incorporate four registers to perform their function. Up to four 7904 Data Channels may be attached to a 7040 or 7044 system. Figure 4 shows data flow within the 7904 Data Channel. The registers used include:

Channel Data Register: This 37-position register acts as a buffer between core storage and the assembly register. The data register has inputs from the storage bus, direct data, and assembly register on a full-word basis.

Word Counter: This 15-position counter contains the number of words to be transmitted to or from the data channel. The counter is loaded from the storage bus before data transmission begins and is decreased by one for each word processed.

Address Counter: This 15-position counter contains the starting address in storage of the message to be stored or transmitted. The counter is loaded from the storage bus before data transmission begins and is increased by one for each word processed.

Assembly Register: This 36-position register serves as a buffer between the channel data register and input-output equipment. Data are assembled and disassembled in the register for transmission.

Read and write operation, using the 7904 channel, is much the same as with data channel A. The outstanding difference is that the CPU registers are not used for control functions with the 7904 and, therefore, the CPU and the 7904 Data Channels can operate independently of each other.

Processing Unit Traps

Automatic trapping of the program is used with the 7040/7044 systems to signal conditions requiring attention to the program without requiring special test instructions. With trapping, system status is constantly monitored and, when particular special conditions are detected, normal processing is interrupted and the program is transferred (trapped) to a trap routine.

To identify the causes of trapping and to allow for a return to normal processing, the instruction counter contents are stored at a fixed location in storage, usually with some trap identification data, when a trap is initiated. The program is then transferred to another fixed location.

Core storage locations assigned for trap operations (Figure 5) are, in order of priority:

TYPE OF TRAP	STORE LOCATION	TRAP LOCATION
Interval Timer Reset	00036	00037
Memory Protect Violation	00032	00033
Storage Parity	00040	00041
Instruction Traps:		
Store Location and Trap (STR)	00000	00002
Floating Point (underflow and overflow)	00000	00010
Release Protect Mode (RPM)	00032	00033
Set Protect Mode (SPM — protect mode already on)	00032	00033
Pre-interrupt Memory Protect	00032	00033
Interval Timer Overflow	00006	00007
Direct Data	00003	00004
Channel E	00022	00023
Channel D	00020	00021
Channel C	00016	00017
Channel B	00014	00015
Channel A	00012	00013

Delayed Traps

Pre-interrupt memory protect, interval timer overflow, direct data, and channel traps are prevented until after execution of the instruction following certain privileged instructions: RDS, PRD, SEN, WRS, PWR, CTR, ENB, RCT, ICT, or SPM. Also, none of the delayed traps can occur between the XEC instruction and the instruction to be executed. A trap can occur after execution of the instruction referred to by the XEC unless the instruction is a privileged instruction.

Halt and Proceed

If an interval timer reset, pre-interrupt memory protect, interval timer overflow, direct data, or channel trap request occurs after execution of an HPR instruction, the program stop light is turned off and the trap occurs. The location of the HPR instruction plus one is placed in positions 21-35 of the trap store location.

Trapping Priority

Interval timer reset, memory protect violation, and storage parity traps do not need to wait until completion of an instruction to cause a trap. Interval timer reset is the highest priority. Memory protect violation and storage parity trap are mutually exclusive in that if the store instruction has a parity error, it is not executed and, if a store is attempted in a protected area, the parity of the location is not checked. The next highest priority are instruction traps, which are all mutually exclusive because the system cannot be executing a floating point instruction and an STR, RPM, or a SPM instruction simultaneously. The same is true of the privileged instructions. SPM is considered a privileged instruction when it does not trap as a violation. Pre-interrupt memory protect trap has priority over interval timer overflow, direct data, and channel traps so that storage protect mode is never on during these trap routines. The data channel farthest from the CPU (cable connection) has the highest priority of the channels. Channel A, being in the CPU, has the lowest priority.

Interval Timer Reset

Every 16⅔ milliseconds, the interval timer requests two storage cycles to read out location 00005, add one to it, and store the result back in location 00005. These cycles can only occur:

1. Between instructions.
2. During the following instructions, if they have to wait for the channel: RDS, PRD, SEN, WRS, PWR, CTR, BSR, REW, RUN, WEF, and WBT.
3. Between unoverlapped cycles of an RCHA instruction.

Undefined instructions and error conditions exist that prevent the interval timer from getting its two storage

cycles. If the interval timer makes a second request before getting cycles for the first, an interval timer reset trap occurs.

The computer may halt operation indefinitely in any of the instructions mentioned, or trap inhibit can be left on. In this case, the interval timer still takes its cycles but an interval timer overflow trap cannot occur. When an interval timer overflow trap is requested, the overflow request is used to block more interval timer cycles until after the interval timer overflow trap or an interval timer reset trap occurs. Incrementing of location 00005 is not blocked when the computer is in true manual status. The interval timer overflow trap has about 33 milliseconds in which to trap or an interval timer reset trap occurs.

The interval timer reset trap does not allow completion of the instruction in process. It resets all data channels including channel A. It does not reset the AC or MQ registers. It stores the instruction counter contents (normally the present instruction location plus one) in positions 21-35 of location 00036 and the computer takes its next instruction from location 00037. Trap inhibit is turned on, inhibiting all other traps, and the two waiting interval timer cycle requests are reset. This means that the contents of location 00005 are two less than they should be when an interval timer reset trap occurs. Interval timer reset trap also resets the interval timer overflow trap request if it is on.

Memory Protect

A memory protect trap occurs if:

1. An RPM instruction is executed (RPM trap).
2. Memory protect mode is on when an SPM instruction is executed (violation trap), even if trap inhibit is on.
3. The program attempts to store in a protected area while memory protect mode is on and trap inhibit is off (violation trap).
4. Memory protect mode is on and trap inhibit is off and a channel, direct data, or interval timer overflow trap is requested (pre-interrupt memory protect trap).

NOTE: Input operations on any channel are allowed to store anywhere without causing a memory protect trap.

Any of the above traps turn off memory protect mode and store the location of the next instruction in sequence in the address part of location 00032. The computer then takes its next instruction from location 00033.

The following positions of location 00032 are used to identify the cause of the memory protect trap:

Bit 17 Pre-interrupt memory protect trap
Bit 16 Violation trap or SPM executed with protect mode on
Bit 15 RPM executed with protect mode on
Bit 14 RPM executed with protect mode off

Storage Parity

Possible types of core storage cycles are:

I cycle: A cycle to read out an instruction.

IA cycle: A cycle to read out an indirect address.

E cycle: A cycle to read or store in the execution of an instruction.

B cycle: A cycle to read out or store information to or from an input-output device on an overlap channel (the store cycle of an SCH and the read-out of an IORD in an RCH are E cycles, not B cycles).

U cycle: A cycle to read out or store information to or from an input-output device on channel A (the store cycle of an SCHA and the read-out of the IORD in an RCHA are E cycles, not U cycles).

C cycle: An interval timer cycle to either read out or store location 00005 contents.

Since no parity bit is kept within CPU registers, a word that is stored from the CPU has a parity bit generated as it is stored; therefore, CPU cycles are only checked during read cycles. This includes all I and IA cycles and E and C read cycles. If a parity error occurs during a read cycle, the word is placed in storage unchanged. Parity is checked during both read and store operations for B and U cycles. For a parity error on an input-output store cycle, the word is stored with a generated correct parity.

The following partial word store instructions require one I and two E cycles: STA, STL, SAC, SXA, SXD, STD, and TSL. The first E cycle is used to read out and check the location where the store is to take place. If a parity error is detected during this first E cycle, a parity trap occurs and the instruction is not completed. If no error is detected during the first E cycle, the storage word is placed in the SR and the required portion of the SR is replaced with the new information. During the second E cycle, the complete SR is stored and no parity error can occur.

If a parity error occurs during an I or IA cycle, with parity inhibit and trap inhibit off, the instruction is not executed. The location of the instruction in error, plus one, is stored in positions 21-35 of location 00040. The address of the location in error is stored in positions 3-17 of location 00040 and a bit is stored in position 18 to indicate that the error was either an I or IA cycle. The computer then takes its next instruction from location 00041.

If a parity error occurs during an E cycle with parity and trap inhibits off, the instruction is not executed and the location of the error instruction, plus one, is placed in position 21-35 of location 00040. The address of the location in error is placed in positions 3-17 of location 00040, and a bit is placed in position 19 to indicate that the error occurred during an E cycle. The computer takes its next instruction from location 00041.

If a parity error occurs during a C cycle with parity and trap inhibit off, the computer waits until the instruction being executed is completed; then, the location of the next instruction to be executed is placed in positions 21-35 of location 00040. A bit is placed in position 1 of location 00040 to indicate the error occurred during a C cycle. Nothing is placed in positions 3-17, because the location in error is 00005 for a C cycle error. The computer then takes its next instruction from location 00041.

If a parity error occurs during an I, IA, E, or C cycle when either parity inhibit or trap inhibit are on, execution of instructions is not interrupted until both parity and trap inhibits are off. At this time, the location of the next instruction to be executed is placed in positions 21-35 of location 00040, and a bit is placed in position S of location 00040 to indicate that a stacked error occurred. The location of the error is not placed in positions 3-17 of location 00040. Bits are placed in positions 1, 18, and 19 to indicate the type of cycle in which the stacked error occurred. More than one of these bits may be stored when multiple errors occur. The computer takes its next instruction from location 00041.

When a parity trap occurs, both parity and trap inhibits are turned on, preventing further traps. If it is desired to enable all traps except parity, a TRT instruction must be executed. To enable parity traps, a TRP instruction is used.

Parity trap occurs only when parity and trap inhibits are off. The positions of location 00040 indicate:

S	A bit in S indicates that an error occurred while trap inhibit and/or parity inhibit were on (stacked)
1	Indicates an interval timer cycle parity error
3-17	Indicates the location in error if the error is not stacked and is not an interval timer cycle error
18	Indicates that an error occurred during an I or IA cycle
19	Indicates that an error occurred during an E cycle
21-35	Indicates the location of the next instruction to be executed for stacked and interval timer errors. Indicates the location, plus one, of the instruction in error for I or IA, or E cycle error (not stacked)

Release Protect Mode

Execution of the release protect mode (RPM) instruction places the location of the RPM instruction, plus one, in positions 21-35 of location 00032. Positions S, 1-20 are replaced with zeros. The computer then takes its next instruction from location 00033. If the computer is in memory protect mode, this instruction turns the memory protect mode off and stores a one in position 15 of location 00032. If the computer is not in memory protect mode (or the feature is not installed) when this instruction is executed, a one is stored in position 14 of location 00032. Memory protect mode is also turned off by depression of the clear or reset keys. When a protect mode trap occurs, trap inhibit is turned on, preventing further traps. To enable traps, a TRP or TRT instruction is used.

Floating Point

During the execution of floating point instructions, the resultant characteristics in the AC and MQ may exceed eight bit positions (result too large for storage). The capacity is exceeded if the exponent goes beyond $+177_8$ or below -200_8; beyond $+177_8$ is termed overflow, below -200_8 is underflow.

Overflow and underflow may occur in either the AC or MQ registers. The computer, on sensing underflow or overflow, puts the address, plus one, of the instruction that caused the condition into the address portion of location 00000. A spill indication is stored in the decrement portion of location 00000 as follows:

BIT	MEANING
S	Double-precision instruction (on machine equipped with single-precision only)
12	Double precision address error
14	Single-precision divide instruction
15	Overflow in AC and/or MQ register
16	AC overflow or underflow
17	MQ overflow or underflow

The computer then takes its next instruction from location 00010. When a floating-point trap occurs, trap inhibit is turned on, preventing further traps. To enable traps, a TRP or TRT instruction is used.

Store Location and Trap

Execution of the store location and trap (STR) instruction places the location of the STR instruction, plus one, in positions 21-35 of location 00000. Positions S, 1-20 of location 00000 are replaced with zeros. The computer then takes its next instruction from location 00002. When a STR instruction is excuted, trap inhibit is turned on, preventing further traps.

Interval Timer Overflow

This feature allows the computer to be interrupted after a predetermined length of time. When the interval timer increments location 00005 and an overflow from position 1 occurs, a trap is requested. This trap cannot occur unless trap inhibit is off. The trap cannot occur between execution of a privileged instruction and the execution of the next instruction. If memory protect mode is on, then a pre-interrupt memory protect trap must occur before the interval timer overflow trap. The contents of the instruction counter (normally the location of the next sequential instruction to be executed in the main program) replaces positions 21-35 of location 00006 and the computer takes its next instruction from location 00007. When an interval timer overflow trap occurs, trap inhibit is turned on, preventing further traps.

When an interval timer overflow trap request is waiting, the interval timer is blocked from increasing location 00005 unless the computer is in true manual

status. If the interval timer overflow trap request waits more than 33 milliseconds, an interval timer reset trap occurs, which resets the interval timer overflow trap request.

Direct Data Trap

This feature allows the channels to signal or interrupt processing by trapping the program. When a direct data trap occurs, the contents of the instruction counter (normally the location of the next instruction to be executed) are stored in positions 21-35 of location 00003. Bits indicating which channels are requesting a direct data trap are stored in the decrement of location 00003. The computer then takes its next instruction from location 00004. The instruction at location 00004 must be an unconditional transfer instruction to be compatible with the IBM 7090, 7094, 7094 II Data Processing Systems.

A direct data trap may occur only when trap inhibit is off and channel trap control is on. A direct data trap cannot occur between execution of a privileged instruction and execution of the instruction following the privileged instruction. When memory protect mode is on, the direct data trap cannot occur until after a pre-interrupt memory protect trap. A direct data trap turns channel trap control off and trap inhibit on and prevents further traps from occuring until after the channel trap control is turned back on with an ENB or RCT instruction or RCT instruction and trap inhibit turned off with a TRP or TRT instruction.

Each channel has a mask register of four bits. One bit controls direct data interrupt requests from that channel. The mask bits can be set to zero or one by the ENB instruction. For each channel, there is also an indicator that can be turned on by the direct data device. A trap occurs if the indicator is on and the direct data mask bit for that channel is a one. When a direct data trap occurs and the indicator is on, a one is stored in its position of the decrement portion of the store location only if its mask bit is a one. When a direct data mask bit is a zero, the direct data indicator associated with it can be turned on, but a one is not stored in the decrement portion of location 00003 if a direct data trap occurs. The channel x direct data indicator is turned off by an RDCX or by the reset, clear, or load keys. Whenever a one is stored, the indicator is turned off. When a trap occurs and the mask bit is a zero, the indicator is not turned off. The following are the bit positions of location 00003 used to reflect indicator status.

Bit 16	Channel B
Bit 15	Channel C
Bit 14	Channel D
Bit 13	Channel E

Data Channel Traps

This feature allows the data channel to signal or interrupt processing by trapping the computer program. Channel traps may be initiated by:

Completion of any channel operation
Redundancy check
End of file
Word parity check
Unusual-end signal from a control adapter
Attention signal from an adapter
1401 attention signal
Tele-processing equipment interrupt signal (channel A only)
Unit record equipment interrupt signal (channel A only)

When a channel trap occurs, the contents of the instruction counter are stored in positions 21-35 of the trap store location. Bits indicating the conditions that caused the trap are stored in the decrement portion of the store location. The reminder of the store location is cleared to zeros. The computer then takes its next instruction from the location specified by the instruction counter. This instruction must be an unconditional transfer to be compatible with IBM 7090, 7094, 7094 II Data Processing Systems programs. The store locations and instruction locations for each channel are:

CHANNEL	STORE LOCATION	INSTRUCTION LOCATION
A	00012	00013
B	00014	00015
C	00016	00017
D	00020	00021
E	00022	00023

A channel trap may occur only when trap inhibit is off and channel trap control is on. A channel trap cannot occur between execution of a privileged instruction and execution of the following instruction. When memory protect mode is on, channel traps cannot occur until after a pre-interrupt memory protect trap. A channel trap turns channel trap control off and trap inhibit on and prevents further traps until after channel trap control is turned back on with an ENB or RCT instruction and trap inhibit turned off with a TRP or TRT instruction.

Each channel has a mask register, which controls conditions that can cause a channel trap. The mask bits can be set to either a one or zero by the ENB instruction. The clear, reset, or load keys set all mask bits to zero. An RDCX sets all four channel x mask bits to zero.

For each condition that can cause a channel trap there is an indicator that can be turned on and off by certain conditions. A trap occurs if the indicator is on and the mask bit with which it is associated is a one. When a trap occurs, and the indicator is on, a one

is stored in its position of the store location. When a mask bit is a zero, the indicator associated with it can be turned on and off but a one is not stored when a trap occurs. All indicators in channel x are turned off by execution of an RDCX. They are also turned off by the reset, clear, or load keys.

Whenever a one is stored, the indicator is turned off. When a trap occurs and the mask bit is a zero, the indicator is not turned off.

Channel Trap Stores

When a channel trap occurs, the following bits may be stored in the decrement of the store location. With each bit is a description of the indicator associated with the trap. More than one indicator may signal a trap and store its bit at the same time; therefore, all bit positions should be scanned rather than stopping at the first position that is found to be a one. The bit positions and indicator names are:

BIT POSITION IN THE STORE LOCATION	INDICATOR NAME	MASK BIT NAME
17	Operation Complete	Operation
16	Redundancy Check	Parity
15	End of File	Operation
14	Word Parity	Parity or Operation
12	Unusual End	Operation
11	1-0 Adapter Attention	Attention
10	1401 Attention	Attention
9	Tele-Processing Interrupt	Attention
8	Unit Record Interrupt	Unit Record

Bit 17, Operation Complete is turned on whenever the channel-in-use indicator is turned from on to off. This occurs at completion of every read, write, sense, and control operation (end of data transfer), or when the magnetic tape unit has completed a BSR, WBT, or WEF or started an REW or RUN. This indicator is turned off whenever the channel-in-use indicator is turned on. This indicator is masked by the operation mask bit.

Bit 16, Redundancy Check is turned on by a parity check received from the 1-0 device, or by byte parity check in the channel. When the channel x parity mask bit is a zero, this indicator may be tested and turned off by a TRCX. When the channel x parity mask bit is set to one, a TRCX does not transfer and does not turn off this indicator. Whenever the parity mask bit is a one and the redundancy check indicator is on, the channel stops the transfer of data to or from storage. The channel address register contains the address, plus one, of the last word transferred. A trap or store operation does not occur unless the channel is not in use. For read operations, the channel remains in use for the entire record, even though data are not transferred to storage. This indicator is masked by the parity mask bit.

Bit 15, End of File is turned on by the end-of-file signal from the 1-0 device. When the channel x operation mask bit is a zero, this indicator may be tested and turned off by a TEFX. When the operation mask bit is a one, the TEFX does not transfer and does not turn the indicator off. A trap or store operation does not occur unless the channel is not in use. This indicator is masked by the operation mask bit.

Bit 14, Word Parity is turned on by a word parity error during read or write (U or B) cycles to storage. It may also be turned on during channel write operations by checking the 37th bit of a word with the sum of the six parity bits of a disassembled word. Whenever the parity mask bit is a one and the word parity indicator is on, the channel stops data transfer to or from storage. The channel address register contains the address, plus one, of the last word transferred. Therefore, if the parity enable bit is a one when an invalid word is fetched from storage on a channel write operation, an SCHX stores one beyond the address of the invalid word. A trap or store operation does not occur unless the channel is not in use. When the channel is not in use, if either the parity mask bit or the operation mask bit is a one, the indicator may signal a trap and store. (NOTE: This bit may be stored under control of two different mask bits. The difference between the two is that the parity mask bit allows the channel to stop transmission when an error occurs.)

Bit 12, Unusual End (Tape Word Incomplete) is turned on at the end of a tape read or write operation if the total number of characters was not a multiple of six. A tape record that is not a multiple of six characters usually represents a tape read error. This indicator is not set when an end of file is read. If this condition occurs while writing tape, a malfunction is indicated. This indicator is also turned on by the 1-0 adapter unusual-end signal at completion of an IORD to indicate an unusual condition. A sense operation is usually required to determine the condition. This indicator is masked by the operation mask bit and cannot signal a trap unless the channel is not in use.

Bit 11, Attention is turned on by the 1-0 adapter attention signal. This indicator is masked by the attention mask bit and can signal a trap and store even when the channel is in use. This indicator is used with channels B through E.

Bit 10, 1401 Attention is turned on by the 1401 and masked by the attention mask bit. This indicator can signal a trap even when channel A is in use, but execu-

tion of an RCH cannot be interrupted. The indicator is used with channel A only.

Bit 9, Tele-Processing Interrupt is turned on whenever an inquiry buffer in the 1414-4 or 1414-5 has a message waiting, or when an output buffer has emptied. Included in this area are local inquiry, telegraph type units, and IBM 1009 Data Transmission Unit. This indicator is masked by the attention mask bit and can signal a trap even if the channel is in use. The indicator is used with channel A only.

Bit 8, Unit Record Interrupt is turned on whenever the following devices on the 1414-3 or 4 have completed their cycle: card reader buffer full, paper tape reader full, card punch buffer empty, or printer buffer empty. This indicator is masked by the unit record mask bit and cannot signal a trap unless the channel is not in use. This indicator is used on channel A only.

Trap Flow Chart

Figure 5 shows logical interaction of various traps and their results, including the conditions that initiate a trap, trap priority, and CPU action. Beginning at the START or "A" box in the upper left corner, it is possible to trace situations involving multiple trap request, privileged instructions, and so on, and determine the sequence and ultimate action of each condition.

Assume that a parity error occurs during an E cycle. Priority scan circuits pass the parity trap interrupt (from the parity trap box on the left side of Figure 5) out the YES leg. This results in inhibiting further parity trap requests (P output of parity trap box to P input of parity inhibit box), and inhibiting further traps (S output of parity trap box to S input of trap inhibit box). Contents of the instruction counter are placed in the address part of location 00040 (IC→(A)00040), the contents of the address register are placed in the decrement part of location 00040 (AR→(D)00040), and the location of the next instruction (00041) is placed in the instruction counter ((A)00041→IC). After this is accomplished, possible trap requests of the type listed on the right side of Figure 5, are tested (output B of parity trap to input B of interval timer reset). If none of these traps occurs, priority circuits again return to point A (START) and the scanning continues.

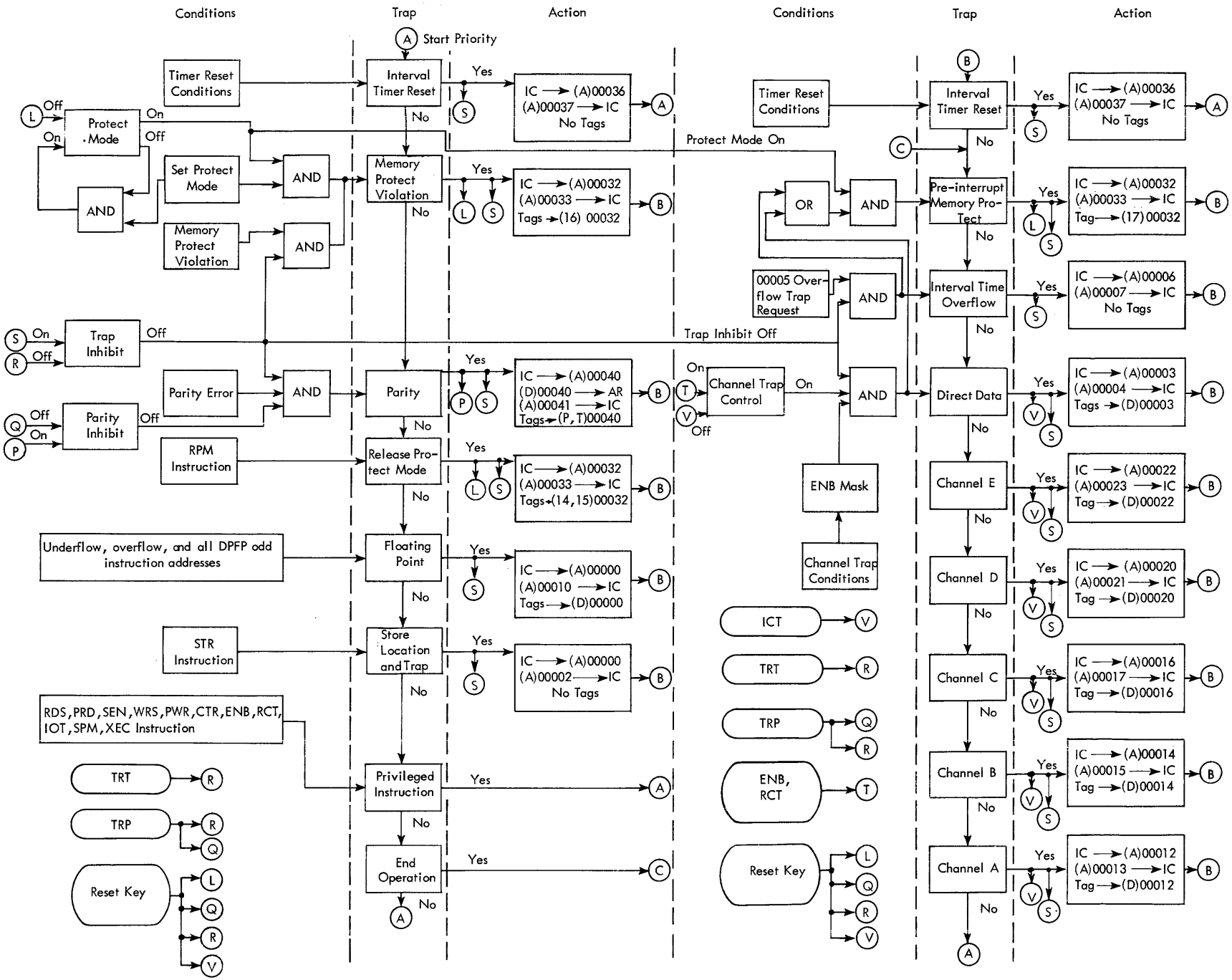


Figure 5. Trap Conditions, Priority, and CPU Action

This section defines all computer instructions and describes their execution, indicators that may be affected, and timing. A diagram representing the format of the instruction appears with each instruction. Preceding the diagram is the alphabetic code that identifies the instruction. The full name of the instruction is also given (Figure 6).

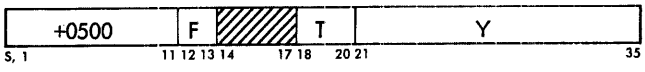


Figure 6. Sample Format of Instructions

The numeric operation code is shown in octal. This can be easily converted to the binary system for reference to the bit pattern interpreted by the computer. The numbers appearing beneath the diagram indicate the instruction word bit positions concerned with this particular instruction.

The symbol Y denotes the address part of the instruction. Y may stand for the address of a word in core storage, the length of a shift, or the address of an I-O device. For some index transmission instructions, Y may also represent a number to be loaded in true form into an index register. For some instructions, positions 21-35 are used to contain a part of the operation code; the appearance of octal numbers instead of Y in the address field distinguish this type of instruction from others. In all cases, the full operation code is shown by its octal representation.

Instructions for which indirect addressing may be specified have the symbol F (flag) appearing in positions 12 and 13 (Figure 6). This symbol represents 1-bits in both positions 12 and 13 of the instruction. The description of operations that can have indirect addressing is defined in terms of direct addressing.

For instructions that are subject to effective address modification by an index register, the diagram has the symbol T in the tag field of the instruction. This T is also used to specify any index register to be changed, stored, or tested. The description accompanying an instruction defines execution when the tag is zero.

Other symbols used in the instruction format are defined in the description part of the instruction. The shaded area in the diagrams represent fields that are not used in the instruction.

Instruction descriptions use special terms and definitions:

1. C(Y) denotes the contents of location Y, where Y refers to some location in core storage. C(AC), C(MQ), and C(SR) denote the contents of the accumulator, multiplier-quotient, and storage registers. Subscripts refer to individual bit positions of a register. For example, $C(MQ)_{S,1\text{-}17}$ is read "the contents of positions S, 1 through 17 of the MQ register." When subscripts are not used, the entire register is implied. For example, C(AC) denotes the contents of accumulator positions S,Q,P,1-35, inclusive.

2. With input-output operations, DC denotes data channel, CAC denotes a data channel address counter, and CWC denotes a data channel word counter.

3. When a register or part of a register, or a core storage location is cleared, the cleared part is reset to zeros.

4. The negative of a number is the number with its sign position reversed.

5. The magnitude of a number is the number with its sign position made positive (a zero in position S corresponds to a positive sign).

6. When the word store is used in the title of an instruction, the transmission of a word or part of a word from some register to some location in core storage is always implied.

7. When the word load is used in the title of an instruction, the transmission of a word or part of a word from some location in core storage to some CPU register is always implied.

8. When the word "place" is used in the title of an instruction, the AC is always one of the registers involved.

9. All logic operations interpret the sign position (S) of Y as a numeric binary bit corresponding to position P of the AC. The S position of the AC is either ignored or cleared by logic operations.

10. In the instructions alphabetic code:
   a. The letter Q designates the MQ register.
   b. The letter X in the second or third position designates use of an index register.
   c. The first letter of all transfer instructions is a T.

Instruction Timing

All instructions are listed in the Appendix by instruction set sequence. Timing is noted in machine cycles for both the 7040 and 7044 systems. The 7040 has a machine cycle of 8.0 microseconds; the 7044 has a machine cycle of 2.0 microseconds.

With indirect addressing, execution time of an instruction is increased one cycle from the times shown. No extra execution time is required for effective address modification with an index register.

When the execution time of an instruction is variable, an instruction type number is included in the instruction description and the instruction list. These types, for both the 7040 and 7044 systems are:

7040	7044
Type 1—ALS, ARS, LGL, LGR, LLS, LRS, and RQL	
These instructions are executed in 1 cycle if the extent of the shift is six places or less. Each additional six-place shift or portion thereof requires ⅓ cycle.	These instructions are executed in 2 cycles if the extent of the shift is six places or less. Each additional six-place shift or portion thereof requires 1 cycle.
Type 2 — DVP	
This instruction is executed in 7⅔ cycles unless a divide check occurs, in which case it requires 2 cycles.	This instruction is executed in 20 cycles unless a divide check occurs, in which case it requires 3 cycles.
Type 3 — MPY	
This instruction is executed in 4 cycles if the MQ contains two or fewer ones. Each additional 6 ones or portion thereof in the MQ requires ⅓ cycle. If the content of Y is zero, the instruction is completed in 2 cycles.	This instruction is executed in 9 cycles if the MQ contains two or fewer ones. Each additional 6 ones or portion thereof in the MQ requires 1 cycle. If the content of Y is zero, the instruction is completed in 3 cycles.
Type 4 — VDP	
This instruction is executed in 2 cycles if the count is zero or one. Each additional two quotient positions or portion thereof requires ⅓ cycle.	This instruction is executed in 2 cycles if the count is zero. It requires 3 cycles if the count is one. Each additional two quotient positions or portion thereof requires 1 cycle.
Type 5 — VLM	
This instruction is executed in 2 cycles if the count is zero or one or if the content of Y is zero. Each additional six steps or portion thereof requires ⅓ cycle. To determine the number of additional steps: add the number of zeros to twice the number of ones in the low-order C bits of the MQ; then subtract one.	This instruction is executed in 2 cycles if the count is zero. It requires 3 cycles if the count is one or if the content of Y is zero. Each additional six steps or portion thereof requires 1 cycle. To determine the number of additional steps: add the number of zeros to twice the number of ones in the low-order C bits of the MQ; then subtract one.
Type 6 — FAD and FSB	
These instructions are executed in a minimum of 2⅓ cycles and a maximum of 8⅔ cycles. In determining average speed, a number of representative programs were traced. The times shown are based on an analysis of several million operands. Execution times greater than 2⅓ cycles are a result of shifting to equalize exponents before adding and to normalize the result after adding. Shifting requires ⅓ cycle for each six places or portion thereof.	These instructions are executed in a minimum of 4 cycles and a maximum of 23 cycles. In determining average speed, a number of representative programs were traced. The times shown are based on an analysis of several million operands. Execution times greater than 4 cycles are a result of shifting to equalize exponents before adding and to normalize the result after adding. Shifting requires one cycle for each six places or portion thereof.
Type 7 — FDP	
This instruction is executed in 7 cycles unless a divide check occurs, in which case it requires 2 cycles.	This instruction is executed in 18 cycles unless a divide check occurs, in which case it requires only 3 cycles.
Type 8 — FMP and UFM	
These instructions are executed in a minimum of 3⅔ cycles and a maximum of 5 cycles. If C(MQ) fraction is zero, it requires only 2 cycles.	These instructions are executed in a minimum of 8 cycles and a maximum of 12 cycles. If C(MQ) fraction is zero, it requires only 2 cycles.
Type 9 — UFA and UFS	
Execution time is the same as for type 6, except maximum is 6⅓ cycles due to un-normalized operation.	Execution time is the same as for type 6, except maximum is 16 cycles due to un-normalized operation.
Type 10 — DFAD, DFSB	
These instructions are executed in a minimum of 4 cycles and a maximum of 11 cycles. The longer times are a result of shifting, as explained in Type 6.	These instructions are executed in a minimum of 7 cycles and a maximum of 28 cycles. The longer times are a result of shifting, as explained in Type 6.
Type 11 — DFMP	
This instruction is executed in a maximum of 13⅔ cycles. If C(AC) and C(MQ) are zero, the instruction requires 3 cycles.	This instruction is executed in a maximum of 36 cycles. If C(AC) and C(MQ) are zero, the instruction requires 3 cycles.
Type 12 — DFDP	
This instruction is executed in a maximum of 18⅓ cycles, and a minimum of 17 cycles. If a divide check occurs, this instruction may require as few as 3 cycles.	This instruction is executed in a maximum of 50 cycles, and a minimum of 46 cycles. If a divide check occurs, this instruction may require as few as 4 cycles.
Type 13 — BSR, ETT, PRD, PWR, RDS, REW, RUN, SEN, WBT, WEF, and WRS	
These instructions are executed in the times given if the channel is not busy and the device selected is ready and not busy. Otherwise, execution is delayed until these conditions do exist. If the channel is not busy and the on-line 1401 is selected, a programmed response is required from the 1401 before these instructions can complete execution.	These instructions are executed in the times given if the channel is not busy and the device selected is ready and not busy. Otherwise, execution is delayed until these conditions do exist. If the channel is not busy and the on-line 1401 is selected, a programmed response is required from the 1401 before these instructions can complete execution.
Type 14 — BSR, REW, RUN, and WEF	
These instructions complete execution in the times given, but the channel remains busy for the duration of the backspace or write end of file. The channel is busy on rewind instructions only long enough to pick relays in the tape unit.	These instructions complete execution in the times given, but the channel remains busy for the duration of the backspace or write end of file. The channel is busy on rewind instructions only long enough to pick relays in the tape unit.

Type 15 – VMA

This instruction is executed in 2 cycles if the count is zero or one. Each additional six steps or portion thereof requires ⅓ cycle. To determine the number of additional steps: add the number of zeros to twice the number of ones in the low-order C bits of the MQ; then subtract one.

This instruction is executed in 2 cycles if the count is zero; 3 cycles are needed if the count is one. Each additional six steps or portion thereof requires 1 cycle. To determine the number of additional steps: add the number of zeros to twice the number of ones in the low-order C bits of the MQ; then subtract one.

Basic Instruction Set

Arithmetic Instructions

In the following instruction descriptions, only indicators that may alter the course of a program through test instructions or by trapping are noted under the "Indicator" heading. All addresses and numbers, unless otherwise stated, are in the octal number system. When instructions are similar, only the differences are noted.

ACL – Add and Carry Logical Word

Description: The C(Y) are added to the C(AC) P, 1-35. The resultant sum replaces the C(AC) P, 1-35. The sign of Y is added to position P of the AC. A carry from AC(P) is added to AC(35). Positions S and Q of the AC are not affected. The C(Y) are unchanged.

Indicators: None

Timing: 7040 – 2 cycles
7044 – 2 cycles

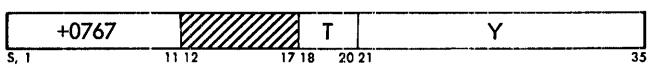
ADD – Add

Description: The C(Y) are algebraically added to the C(AC). The resulting sum is placed in the AC. The C(Y) are unchanged. Numbers of the same magnitude but different signs give a resultant sign the same as the sign of the original AC. A carry from adder 1 turns on AC overflow.

Indicators: AC overflow

Timing: 7040 – 2 cycles
7044 – 2 cycles

ALS – Accumulator Left Shift

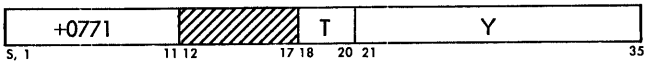


Description: This instruction causes the C(AC) Q, P, 1-35 to be shifted left the number of places specified in positions 28-35 of the address portion of the instruction. The sign position is unchanged. Vacated positions are filled with zeros. A one-bit shifted from position 1 turns on AC overflow.

Indicators: AC overflow

Timing: 7040 – 1 to 2⅔ cycles
7044 – 2 to 7 cycles
Type 1

ARS – Accumulator Right Shift

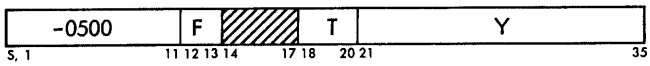


Description: The C(AC) Q, P, 1-35 are shifted right the number of places specified in positions 28-35 of the address portion of the instruction. The sign position is unchanged. Vacated positions are filled with zeros.

Indicators: None

Timing: 7040 – 1 to 2⅔ cycles
7044 – 2 to 7 cycles
Type 1

CAL – Clear and Add Logical Word

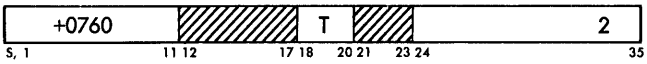


Description: The C(Y) replace the C(AC) P, 1-35. The sign of Y appears in position P of the AC. Positions S and Q of the AC are set to zeros. The C(Y) are unchanged.

Indicators: None

Timing: 7040 – 2 cycles
7044 – 2 cycles

CHS – Change Sign

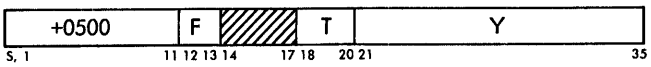


Description: If the AC sign is plus, it is made negative; if it is negative, it is made plus. Address modification by an index register may change the operation itself. C(AC) Q, P, 1-35 are unchanged.

Indicators: None

Timing: 7040 – 1 cycle
7044 – 2 cycles

CLA – Clear and Add



Description: The C(AC) S, 1-35 are replaced with the C(Y). Positions P and Q of the AC are set to zero. The C(Y) remain unchanged.

Indicators: None

Timing: 7040 – 2 cycles
7044 – 2 cycles

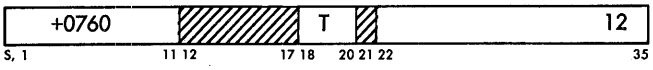
CLS — Clear and Subtract

Description: The negative of C(Y) replaces the C(AC) $_{S,\ 1\text{-}35}$. Positions P and Q of the AC are set to zero. The C(Y) are unchanged.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 2 cycles

DCT — Divide Check Test



Description: If the indicator is on, it is turned off and the computer takes the next sequential instruction. If the indicator is off, the computer skips the next instruction and proceeds from there. Address modification may result in changing the instruction itself.

Indicators: Divide Check

Timing: 7040 — 1 cycle
7044 — 2 cycles

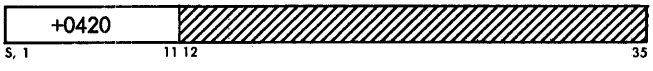
DVP — Divide or Proceed

Description: The C(AC) $_{Q,\ P,\ 1\text{-}35}$ and the C(MQ) $_{1\text{-}35}$ are treated as a 70-bit dividend, plus sign, and the C(Y) as a 35-bit divisor. If the magnitude of C(Y) is greater than the magnitude of C(AC), division takes place. A 35-bit quotient replaces the C(MQ) $_{1\text{-}35}$ and the remainder replaces the C(AC) $_{1\text{-}35}$. The MQ sign is the algebraic sign of the quotient, and the AC sign is the sign of the dividend. If the magnitude of the C(Y) is less than or equal to the magnitude of the C(AC), division does not occur, the divide check indicator is turned on, and the computer proceeds to the next instruction. The C(Y) are unchanged.

Indicators: Divide Check

Timing: 7040 — 7⅔ cycles
7044 — 20 cycles
Type 2

HPR — Halt and Proceed



Description: This instruction causes the computer to halt. The IC contains the location of the next sequential instruction. When the start key on the operator's console is depressed, the computer proceeds and executes the next sequential instruction. If the computer is enabled and I-O interrupt occurs, the computer goes into automatic, and the C(IC) are stored in the trap location.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 2 cycles

LBT — Low-Order Bit Test

Description: If the C(AC) $_{35}$ is a 1, the computer skips the next instruction and proceeds from there. If C(AC) $_{35}$ is a 0, the computer takes the next sequential instruction. Address modification may result in changing the instruction.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 2 cycles

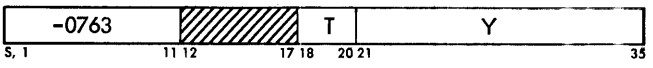
LDQ — Load MQ

Description: This instruction loads the C(Y) into the MQ. The C(Y) are unchanged.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 2 cycles

LGL — Logical Left Shift

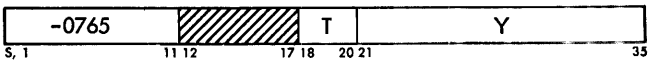


Description: The C(AC) $_{Q,\ P,\ 1\text{-}35}$ and the C(MQ) $_{S,\ 1\text{-}35}$ are treated as one register. Their contents are shifted left the number of places specified in positions 28-35 of the address portion of the instruction. The sign of the AC is unchanged. Vacated positions are filled with zeros.

Indicators: AC overflow

Timing: 7040 — 1 to 4⅔ cycles
7044 — 2 to 13 cycles
Type 1

LGR — Logical Right Shift



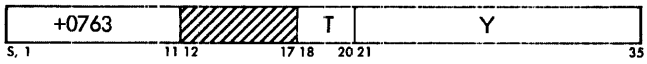
Description: The C(AC) $_{Q,\ P,\ 1\text{-}35}$ and the C(MQ) $_{S,\ 1\text{-}35}$ are treated as one register. Their contents are shifted right the number of places specified in positions 28-35 of the address portion of the instruction. The sign

of the AC is unchanged. Vacated positions are filled with zeros.

Indicators: None

Timing: 7040 – 1 to 4⅔ cycles
7044 – 2 to 13 cycles
Type 1

LLS – Long Left Shift

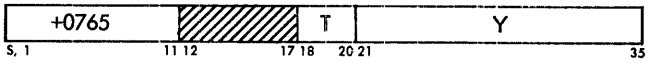


Description: The C(AC) $_{Q, P, 1-35}$ and the C(MQ) $_{1-35}$ are treated as one register. Their contents are shifted left the number of places specified in positions 28-35 of the address portion of the instruction. The MQ sign position is unchanged and the sign of the AC is made to agree with it. Vacated positions are filled with zeros. A one-bit shifted from AC_1 turns on AC overflow.

Indicators: AC overflow

Timing: 7040 – 1 to 4⅔ cycles
7044 – 2 to 13 cycles
Type 1

LRS – Long Right Shift

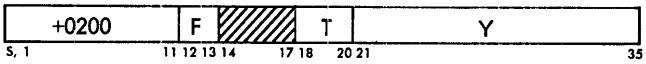


Description: The C(AC) $_{Q, P, 1-35}$ and the C(MQ) $_{1-35}$ are treated as one register. Their contents are shifted right the number of places specified in positions 28-35 of the address portion of the instruction. The AC sign is unchanged and the sign of the MQ is made to agree with it. Vacated positions are filled with zeros.

Indications: None

Timing: 7040 – 1 to 4⅔ cycles
7044 – 2 to 13 cycles
Type 1

MPY – Multiply

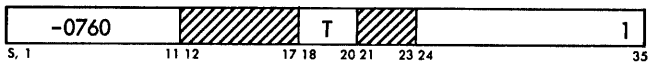


Description: The C(Y) are multiplied by the C(MQ). The 35 most significant bits of the 70-bit product replace C(AC) $_{1-35}$ and the least significant bits replace the C(MQ) $_{1-35}$. AC $_{Q, P}$ are cleared. The signs of the AC and MQ are set to the algebraic sign of the product. The number of bits to the right of the binary point of the first factor added to the number of bits to the right of the binary point of the second factor give the total number of bits to the right of the binary point in the product. C(Y) are unchanged.

Indicators: None

Timing: 7040 – 4 to 6 cycles
7044 – 9 to 15 cycles
Type 3

PBT – P Bit Test

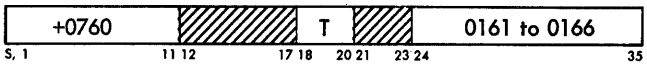


Description: If the C(AC) $_P$ is a 1, the computer skips the next instruction and proceeds from there. If C(AC) $_P$ contains a zero, the computer takes the next sequential instruction. Address modification may result in changing the instruction itself.

Indicators: None

Timing: 7040 – 1 cycle
7044 – 2 cycles

SWT – Sense Switch Test



Description: This instruction provides a means of testing the status of the sense switches on the operator's console. If the corresponding switch is in (ON), the computer skips the next instruction and proceeds from there. If the sense switch is out (OFF), the computer takes the next sequential instruction. Address modification may cause the operation code to be changed.

Indicators: Sense switches

Timing: 7040 – 1 cycle
7044 – 2 cycles

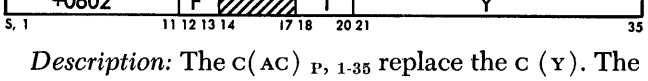
RQL – Rotate MQ Left

Description: The C(MQ) $_{S, 1-35}$ are shifted left the number of places specified by positions 28-35 of the address portion of the instruction. The instruction shifts bits from position S into position 35, and thus the register becomes a circular one. No bits are lost.

Indicators: None

Timing: 7040 – 1 to 2⅔ cycles
7044 – 2 to 7 cycles
Type 1

SLW – Store Logical Word

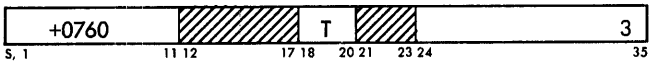


Description: The C(AC) $_{P, 1-35}$ replace the C (Y). The C(AC) are unchanged.

Indicators: None

Timing: 7040 – 2 cycles
7044 – 2 cycles

SSP — Set Sign Plus

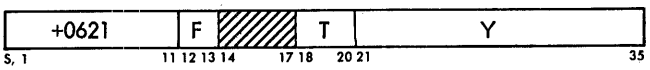


Description: The sign of the AC is set to plus (zero). Address modification by an index register may result in changing the operation itself.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 2 cycles

STA — Store Address

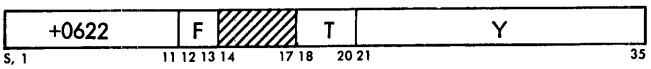


Description: The C(AC) $_{21\text{-}35}$ replace the C(Y) $_{21\text{-}35}$. The C(Y) $_{S,\ 1\text{-}20}$ and the C(AC) are unchanged.

Indicators: None

Timing: 7040 — 3 cycles
7044 — 3 cycles

STD — Store Decrement

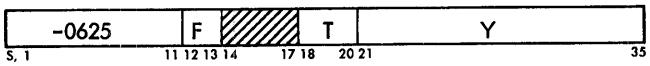


Description: The C(AC) $_{3\text{-}17}$ replace C(Y) $_{3\text{-}17}$. The C(Y) $_{S,\ 1,\ 2,\ 18\text{-}35}$ and the C(AC) are unchanged.

Indicators: None

Timing: 7040 — 3 cycles
7044 — 3 cycles

STL — Store Instruction Location Counter

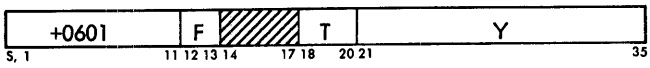


Description: The location of the STL instruction, plus 1, replaces the C(Y) $_{21\text{-}35}$. The C(Y) $_{S,\ 1\text{-}20}$ are unchanged.

Indicators: None

Timing: 7040 — 3 cycles
7044 — 3 cycles

STO — Store



Description: The C(AC) $_{S,\ 1\text{-}35}$ replace the C(Y). The C(AC) are unchanged.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 2 cycles

STQ — Store MQ

Description: The instruction places the contents of the MQ into the specified Y location. The C(MQ) remain unchanged.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 2 cycles

STR — Store Location and Trap

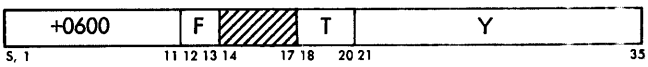
Description: The location of the STR instruction, plus one, replaces positions 21-35 of location 00000. Positions S, 1-20 of location 00000 are replaced by zeros. The computer then takes its next instruction from location 00002. The contents of positions 12-35 of the instruction are not interpreted by the 7040/7044. Operation codes +0000 and −0000 are similarly treated as a STR by the 7040/7044. (It should be noted that +0000 is the operation code for HTR (halt and transfer) on a 7090, 7094, 7094 II and should not be programmed on the 7040/7044 for an HTR).

Indicators: Trap Inhibit

Timing: 7040 — 2 cycles
7044 — 2 cycles

NOTE: This instruction and floating point trap both use location 00000.

STZ — Store Zero

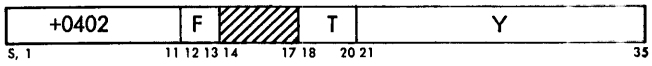


Description: The C(Y) $_{1\text{-}35}$ are replaced by zeros and the sign of Y is made plus.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 2 cycles

SUB — Subtract



Description: The C(Y) are algebraically subtracted from the C(AC). The difference replaces the C(AC). The C(Y) are unchanged.

Indicators: AC overflow

Timing: 7040 — 2 cycles
7044 — 2 cycles

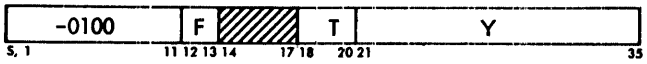
TMI — Transfer on Minus

Description: If the sign position of the AC is negative, the computer takes its next instruction from location Y and proceeds from there. If the sign position is positive, the computer takes the next sequential instruction.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 1 cycle

TNZ — Transfer on No Zero



Description: If the C(AC) Q, P, 1-35 are not zero, the computer takes its next instruction from location Y and proceeds from there. If they are zero, the next sequential instruction is taken.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 1 cycle

TPL — Transfer on Plus

Description: If the sign position of the AC is positive, the computer takes its next instruction from location Y and proceeds from there. If the sign position is negative, the computer takes the next sequential instruction.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 1 cycle

TOV — Transfer on Overflow

Description: If the AC overflow indicator is on, it is turned off and the computer takes its next instruction from location Y. If the indicator is off, the computer takes the next sequential instruction.

Indicators: AC overflow

Timing: 7040 — 1 cycle
7044 — 1 cycle

TRA — Transfer

Description: This instruction causes the computer to take its next instruction from location Y and proceed from there.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 1 cycle

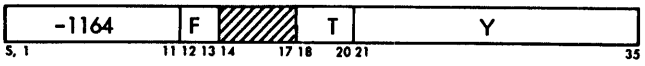
TRP — Transfer and Restore Parity and Traps

Description: Trap inhibit and parity inhibit are restored and the computer takes its next instruction from Y.

Indicators: Trap inhibit
Parity inhibit

Timing: 7040 — 1 cycle
7044 — 1 cycle

TRT — Transfer and Restore Traps



Description: Trap inhibit is turned off and the computer takes its next instruction from Y.

Indicators: Trap inhibit

Timing: 7040 — 1 cycle
7044 — 1 cycle

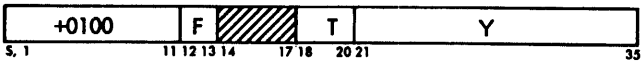
TSL — Transfer and Store Instruction Location Counter

Description: The location of the TSL instruction, plus one, is stored in positions 21-35 of Y. Positions S, 1-20 of Y are unchanged. The computer takes its next instruction from location Y+1.

Indicators: None

Timing: 7040 — 3 cycles
7044 — 3 cycles

TZE — Transfer on Zero

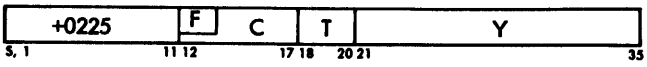


Description: If the C(AC) Q, P, 1-35 are zero, the computer takes its next instruction from location Y and proceeds from there. If they are not zero, the computer takes the next sequential instruction.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 1 cycle

VDP — Variable Length Divide or Proceed



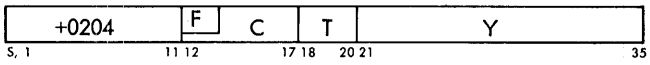
Description: This instruction is the same as DVP except that a C bit quotient with a sign replaces the C low-order position of the MQ. The remainder replaces

the C(AC) $_{1\text{-}35}$ and the 35−C high-order positions of the MQ. C rather than 43_8 is placed in the shift counter initially. If C is zero, the instruction is interpreted as no-operation and the computer proceeds directly to the next instruction in sequence. Indirect addressing may occur if C contains 1-bits in positions 12 and 13 of this instruction.

Indicators: Divide check

Timing: 7040 – 2 to 8⅔ cycles
7044 – 2 to 20 cycles
Type 4

VLM – Variable Length Multiply



Description: This instruction multiplies the C(Y) by the C low-order bits of the C(MQ) to produce a 35+C bit product. The 35 most significant bits of the product replace the C(AC) $_{1\text{-}35}$ and the C least significant bits replace C(MQ) $_{1\text{-}C}$. C(AC) $_{Q, P}$ are cleared. The remaining 35−C positions of the MQ will contain the original 35−C high-order bits of the MQ. The signs of the AC and MQ are set to the algebraic sign of the product.

If C is zero, the instruction is interpreted as no-operation and the computer proceeds to the next instruction in sequence, leaving the AC unchanged.

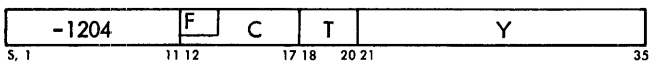
If C is not zero, but the C(Y) are zero, the C(AC) and C(MQ) are cleared. If the signs of the MQ and Y are the same, the signs of the AC and MQ are made positive; if the signs of the MQ and Y differ, the signs of the AC and MQ are made negative.

If C is 60_8 or larger, indirect addressing results. In general, counts larger than 43_8 are meaningless.

Indicators: None

Timing: 7040 – 2 to 6 cycles
7044 – 2 to 15 cycles
Type 5

VMA – Variable Length Multiply and Accumulate



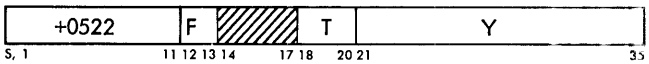
Description: This instruction is similar to the VLM instruction except that the C(AC) $_{Q, P, 1\text{-}35}$ are not cleared before the multiplication begins. This results in generating the sum of the magnitude of the C(AC) $_{Q, P, 1\text{-}35}$ and the magnitude of 35+C bit product. If AC $_{P, Q}$ both originally contain ones, a carry may be lost during the accumulation, and the overflow indicator will not be turned on. The C least significant bits of the product replace the C(MQ) $_{1\text{-}C}$. The 36 most significant bits replace the C(AC) $_{P, 1\text{-}35}$. AC $_Q$ is cleared. The remaining 35−C positions of the MQ contain the original 35−C high-order bits of the MQ. The signs of the AC and MQ are set to the algebraic sign of the product.

If C is zero, the instruction is interpreted as no-operation and the computer proceeds to the next instruction in sequence, leaving the AC unchanged. If C is not zero, but the C(Y) are zeros, the result will be an LRS of C places and the AC and MQ signs are set to the sign of the product of the C(Y)'s and the original C(MQ)'s. If C is 60_8 or larger, indirect addressing results. In general, counts larger than 43_8 are meaningless.

Indicators: None

Timing: 7040 – 2 to 6 cycles
7044 – 2 to 15 cycles
Type 15

XEC – Execute



Description: This instruction causes the computer to execute the instruction at location Y. Since the location counter is not altered (when Y contains any instruction other than a successful transfer or test instruction), the program advances to the next sequential instruction following the execute instruction after performing the instruction at location Y. If location Y contains a transfer instruction, it will be executed and program control is altered from the sequential process. If location Y contains a test instruction, the instruction following the execute instruction will be located relative to the execute instruction rather than the test instruction. Thus, any instruction which changes the instruction counter alters program control when that instruction is executed by the XEC instruction.

Indicators: None

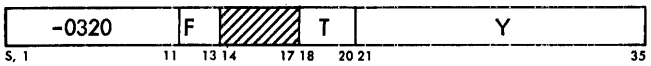
Timing: 7040 – 1 cycle
7044 – 1 cycle

Logical Operations

Instructions are provided to work on a 36-bit word or an individual character within a word.

All logical operations interpret the sign position (S) of Y as a numeric binary bit corresponding to position P of the AC. The S position of the AC is either ignored or cleared.

ANA — AND to Accumulator

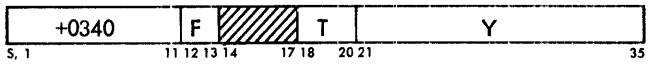


Description: Each bit of the C(Y) S, 1-35 is matched with the corresponding bit of the C(AC) P, 1-35. C(Y)S is matched with C(AC) P. When the corresponding bits of both location Y and the AC are ones, a one replaces the contents of that position in the AC. When the coresponding bit of either location Y or the AC, or both, is a zero, a zero replaces the contents of that position in the AC. The S and Q positions of the AC are cleared. The C(Y) are unchanged.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 2 cycles

CAS — Compare Accumulator with Storage



Description: If the C(AC) are algebraically greater than the C(Y), the computer takes the next sequential instruction. If the C(AC) are algebraically equal to the C (Y), the computer skips the next instruction and proceeds from there. If the C(AC) are algebraically less than the C(Y), the computer skips the next two instructions and proceeds from there.

NOTE: A plus zero is considered greater than a minus zero.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 3 cycles

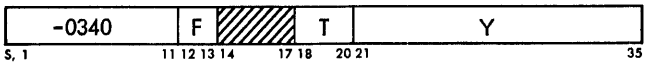
COM — Complement Magnitude

Description: All ones are replaced by zeros and all zeros are replaced by ones in the C(AC) Q, P, 1-35. The C(AC) S is unchanged. Address modification may change the instruction itself.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 2 cycles

LAS — Logical Compare Accumulator with Storage

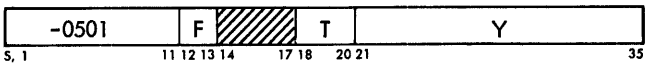


Description: The C(AC) Q, P, 1-35 are treated as an unsigned 37-bit number and are compared with the C(Y) S, 1-35, which are treated as an unsigned 36-bit quantity. If the C(AC) Q, P, 1-35 are greater than the C(Y), the computer takes the next sequential instruction. If the C(AC) Q, P, 1-35 are equal to the C(Y), the computer skips the next instruction and proceeds from there. If the C(AC) Q, P, 1-35 are less than the C(Y), the computer skips the next two instructions and proceeds from there.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 3 cycles

ORA — OR to Accumulator



Description: Each bit of the C(Y) S, 1-35 is matched with the corresponding bit of the C(AC) P, 1-35. C(Y) S is matched with the C(AC) P. When the corresponding bit of either location Y or the AC (or both) is a one, a one replaces the contents of that position in the AC. When the corresponding bits of both location Y and the AC are zeros, a zero replaces the contents of that position of the AC. The C(Y) and the S and Q positions of the AC are unchanged.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 2 cycles

ENK — Enter Keys

Description: This instruction places the contents of the console entry keys into the MQ register. Address modification may result in changing the operation. A depressed key is interpreted as a 1 bit.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 2 cycles

Extended Performance Set

Three index registers — called A, B, and C or 1, 2, and 4 — are available. The registers are selected by a bit in the tag field of an instruction. The tag field is always bits 18, 19, and 20 of the instruction. Bit 20 selects index register A, bit 19 selects B, and bit 18 selects C.

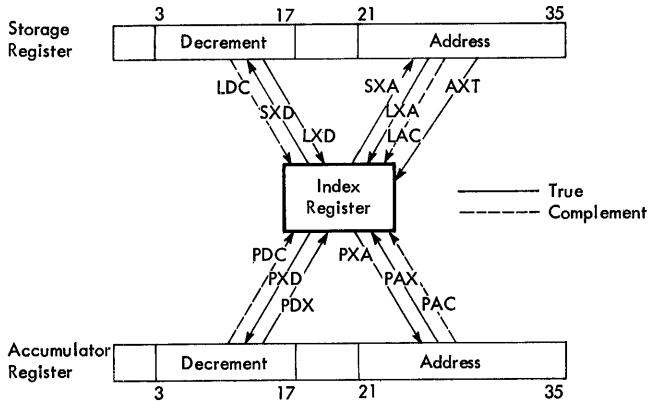
Temporary address modification is one of the primary uses of index registers. For this to occur, the instruction must specify index registers by bits in its tag field. The instruction is executed as if its address field contained the given address minus the contents of the index register.

Computer instructions, when tagged, are subject to address modification, except instructions that load, store, modify, or test the contents of an index register. These instructions use the tag field to specify the index registers affected.

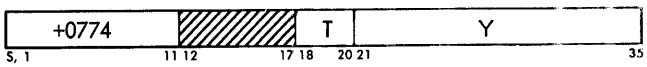
Index Transmission Instructions

The following instructions are used for index register servicing and testing.

A chart of index transmission instruction data flow between storage, accumulator, and the index registers is shown following. Both true and complement lines are shown with appropriate instructions.



AXT — Address to Index True

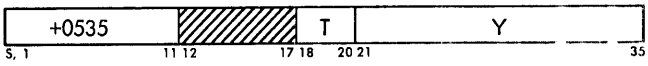


Description: Positions 21-35 of this instruction replace the contents of the specified index register. The instruction is unchanged. A tag of zero results in no-operation.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 1 cycle

LAC — Load Complement of Address in Index



Description: The 2's complement of C(Y) $_{21\text{-}35}$ replaces the contents of the specified XR. The C(Y) are unchanged. A tag of zero results in no-operation.

Indicators: None

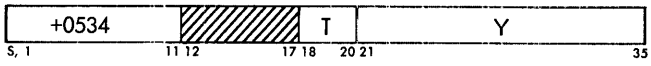
Timing: 7040 — 2 cycles
7044 — 2 cycles

LDC — Load Complement of Decrement in Index

Description: The 2's complement of C(Y) $_{3\text{-}17}$ replaces the contents of the specified XR. The C(Y) are unchanged. A tag of zero results in no-operation.

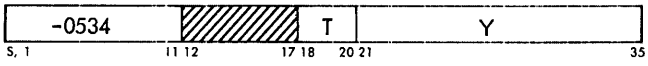
Indicators: None
Timing: 7040 — 2 cycles
7044 — 2 cycles

LXA — Load Index from Address



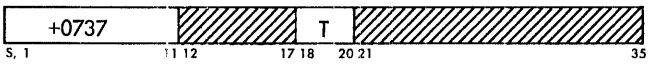
Description: The C(Y) $_{21\text{-}35}$ replace the contents of the specified index register. The C(Y) are unchanged. A tag of zero results in no-operation.
Indicators: None
Timing: 7040 — 2 cycles
7044 — 2 cycles

LXD — Load Index from Decrement



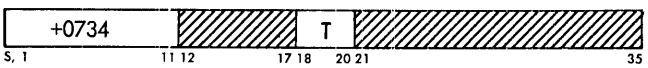
Description: The C(Y) $_{3\text{-}17}$ replace the contents of the specified index register. The C(Y) are unchanged. A tag of zero results in no-operation.
Indicators: None
Timing: 7040 — 2 cycles
7044 — 2 cycles

PAC — Place Complement of Address in Index



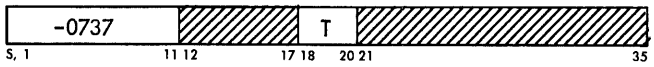
Description: The 2's complement of C(AC) $_{21\text{-}35}$ replace the contents of the specified index register. The C(AC) are unchanged. A tag of zero results in no-operation.
Indicators: None
Timing: 7040 — 1 cycle
7044 — 2 cycles

PAX — Place Address in Index



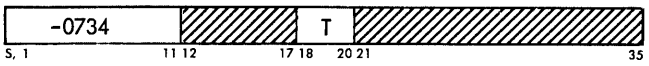
Description: The C(AC) $_{21\text{-}35}$ replace the contents of the specified index register. The C(AC) are unchanged. A tag of zero results in no-operation.
Indicators: None
Timing: 7040 — 1 cycle
7044 — 2 cycles

PDC — Place Complement of Decrement in Index



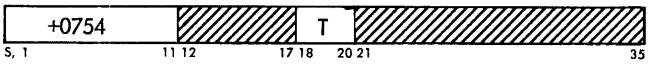
Description: The 2's complement of C(AC) $_{3\text{-}17}$ replace the contents of the specified index register. The C(AC) are unchanged. A tag of zero results in no-operation.
Indicators: None
Timing: 7040 — 1 cycle
7044 — 2 cycles

PDX — Place Decrement in Index



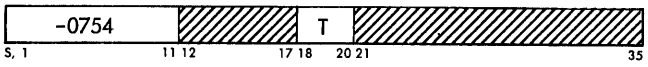
Description: The C(AC) $_{3\text{-}17}$ replace the contents of the specified index register. The C(AC) are unchanged. A tag of zero results in no-operation.
Indicators: None
Timing: 7040 — 1 cycle
7044 — 2 cycles

PXA — Place Index in Address



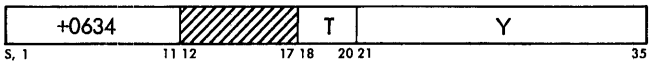
Description: The entire accumulator is cleared and the contents of the specified index register are placed in the address part of the AC $_{21\text{-}35}$. With a tag of zero, the C(AC) are set to zeros. The specified index register is unchanged.
Indicators: None
Timing: 7040 — 1 cycle
7044 — 2 cycles

PXD — Place Index in Decrement



Description: The entire accumulator is cleared and the contents of the specified index register are placed in the decrement part of the AC $_{3\text{-}17}$. With a tag of zero, the C(AC) are set to zeros. The specified index register is unchanged.
Indicators: None
Timing: 7040 — 1 cycle
7044 — 2 cycles

SXA — Store Index in Address

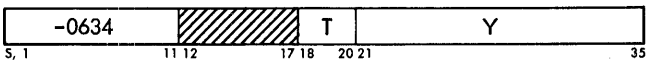


Description: The C(Y) $_{21\text{-}35}$ are replaced by the contents of the specified index register. The C(Y) $_{S,\ 1\text{-}20}$ are unchanged. With a tag of zero, the C(Y) $_{21\text{-}35}$ are set to zeros.

Indicators: None

Timing: 7040 — 3 cycles
7044 — 3 cycles

SXD — Store Index in Decrement

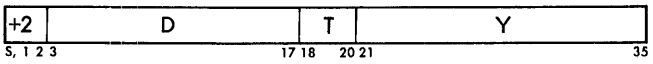


Description: The C(Y) $_{3\text{-}17}$ are replaced by the contents of the specified index register. The C(Y) $_{S,\ 1,\ 2,\ 18\text{-}35}$ are unchanged. With a tag of zero, the C(Y) $_{3\text{-}17}$ are set to zeros.

Indicators: None

Timing: 7040 — 3 cycles
7044 — 3 cycles

TIX — Transfer on Index

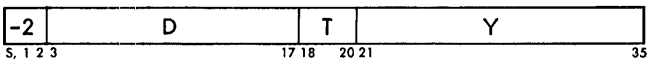


Description: If the C(XR) specified by T are greater than the D, the number in the index register is reduced by D and the computer takes its next instruction from Y. If C(XR) are less than or equal to D, the C (XR) are unchanged and the computer takes the next sequential instruction. With a tag of zero, no transfer occurs.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 2 cycles

TNX — Transfer on No Index

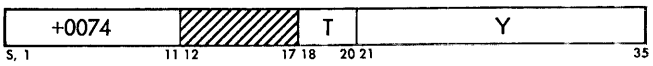


Description: If the C(XR) specified by T is greater than D, the C(XR) will be reduced by the amount D, and the computer will proceed to the next instruction in sequence. When C(XR) is equal to or less than D, no reduction is made, but the computer transfers to location Y. With a tag of zero, a transfer occurs.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 2 cycles

TSX — Transfer and Set Index

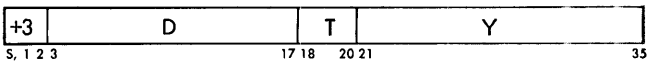


Description: This instruction places the 2's complement of the location of the TSX in the specified index register (T). The computer takes its next instruction from location Y.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 2 cycles

TXH — Transfer on Index High

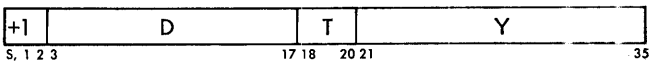


Description: If the C(XR) specified by T is greater than D, the computer takes its next instruction from location Y. If the number in the specified index register is less than or equal to D, the computer takes the next sequential instruction. With a tag of zero, no transfer occurs.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 2 cycles

TXI — Transfer with Index Incremented

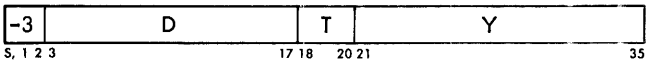


Description: This instruction adds D to the C(XR) specified by T and replaces the contents of the index register with the resulting sum. The computer then takes its next instruction from location Y.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 2 cycles

TXL — Transfer on Index Low or Equal



Description: If the C(XR) specified by T are less than or equal to D, the computer takes its next instruction from location Y. If C(XR) are greater than D, the computer takes the next sequential instruction. With a tag of zero, a transfer occurs.

Indicators: None

Timing: 7040 — 1 cycle
7044 — 2 cycles

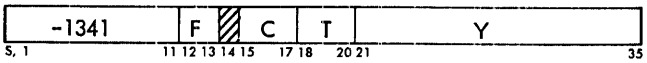
Character Handling Operations

Three character handling instructions are used to expedite six-bit character operations. In each of the character handling instructions, positions 15, 16, and 17 of

the instruction word specify which character of the word located at the effective address is to be used in the operation. Valid bit patterns for the position field are octal numbers from zero to five and specify the following characters:

OCTAL POSITION FIELD	CHARACTER TO BE USED
0	S, 1-5
1	6-11
2	12-17
3	18-23
4	24-29
5	30-35
6	See MSM and MIT
7	See MSP and PLT

CCS — Compare Character with Storage

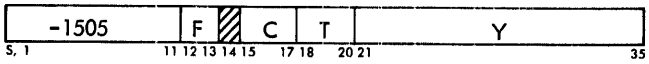


Description: The character specified by C in Y is compared with the C(AC) 30-35. The C(AC) S, Q, P, 1-29 are ignored. If the C(AC) 30-35 are greater than the character in Y, the computer takes the next sequential instruction. If the C(AC) 30-35 are equal to the specified character in Y, the computer skips the next instruction and proceeds from there. If the C(AC) 30-35 are less than the specified character in Y, the computer skips the next two instructions and proceeds from there. The C(AC) and C(Y) are unchanged.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 3 cycles

PCS — Place Character from Storage

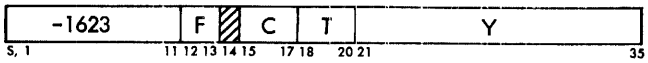


Description: The character specified by C in Y replaces the C(AC) 30-35. The C(AC) S, Q, P, 1-29 are unchanged. The C(Y) are unchanged.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 2 cycles

SAC — Store Accumulator Character



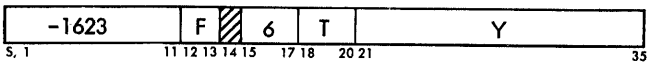
Description: The C(AC) 30-35 is stored in location Y in the character position specified by C. The remaining bits of the C(Y) are unchanged. The C(AC) are unchanged.

Indicators: None

Timing: 7040 — 3 cycles
7044 — 3 cycles

Sign Position Handling Instructions

MSM — Make Storage Sign Minus

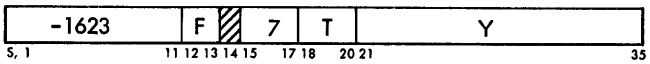


Description: The C(Y) S is replaced with a one bit (minus). The remainder of Y is unchanged. Positions 15-17 are part of the operation code.

Indicators: None

Timing: 7040 — 3 cycles
7044 — 3 cycles

MSP — Make Storage Sign Plus

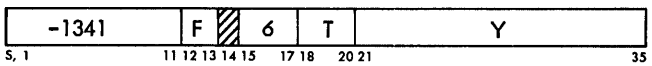


Description: The C(Y) S is replaced with a zero bit (plus). The remainder of Y is unchanged. Positions 15-17 are part of the operation code.

Indicators: None

Timing: 7040 — 3 cycles
7044 — 3 cycles

MIT — Storage Minus Test

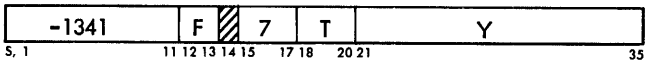


Description: If the C(Y) S is minus, the computer skips the next instruction and proceeds from there. If the C(Y) S is plus, the computer takes the next sequential instruction. Positions 15-17 are part of the instruction operation code.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 3 cycles

PLT — Storage Plus Test



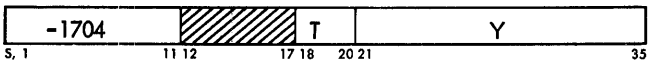
Description: If the C(Y) S is plus, the computer skips the next instruction and proceeds from there. If the C(Y) S is minus, the computer takes the next sequential instruction. Positions 15-17 are part of the instruction operation code.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 3 cycles

Data Transmission Instructions

TMT — Transmit



Description: This instruction uses the C(AC) $_{3\text{-}17}$ as a FROM address and C(AC) $_{21\text{-}35}$ as a TO address. The C (FROM) replace the C(TO), and the C(FROM) remain unchanged. Then the C(FROM + 1) replace the C(TO + 1); the C(FROM + 1) remain unchanged. This continues for the total number of words transmitted. Positions 28-35 of the address portion of the instruction are used to specify the number of words to be transferred. This provides a maximum transfer of 377_8 words. Any number larger than 377_8 is interpreted as modulo 400. Modulo 400 means that, given a transmit count, the actual number of words transmitted will be the remainder after dividing the count by 400. With indexing, the number is modified by positions 28-35 of the specified index register.

Execution:

1. Positions 28-35 of the instruction are modified by the specified index register and placed in the shift counter.
2. If the contents of the shift counter are zero, the instruction ends.
3. If the content of the shift counter is not zero, C(AC) $_{3\text{-}17}$ are used to address storage.
4. The contents of the location specified by C(AC) $_{3\text{-}17}$ are placed in the SR.
5. Positions C(AC) $_{21\text{-}35}$ are used to address storage.
6. The contents of the SR are stored in the location specified by C(AC) $_{21\text{-}35}$.
7. The C(AC) $_{3\text{-}17}$ and C(AC) $_{21\text{-}35}$ are both incremented by one.
8. The shift counter is decremented by one.
9. Execution returns to step 2.

At the completion of a TMT instruction, the C(AC) $_{3\text{-}17}$ contain the address of the last word read, plus one, and the C(AC) $_{21\text{-}35}$ contain the address of the last word stored, plus one. Another TMT instruction can be given if it is desired to transmit more than 377_8 words.

Indicators: None

Timing: 7040 — 1 + 2N cycles
7044 — 2 + 2N cycles
N is number of words transmitted.

Floating-Point Instructions

The following operations are divided into two groups to describe the processing of floating-point numbers in either normalized or unnormalized form. All conditions of underflow and overflow are discussed in the floating-point trap discussion.

FLOATING-POINT OPERATIONS

Eleven floating-point instructions are used in the IBM 7040 and 7044 systems. Enough similarities exist in the operation of the instructions so that, for study purposes, only four distinct instructions need be considered in single-precision and four in double-precision operations.

FLOATING-POINT NUMBERS

When the range of numbers anticipated during a calculation is either large or unpredictable, it becomes difficult to work with fixed-point instructions. An alternative set of floating-point instructions is available for such calculations. These instructions maintain the binary point automatically.

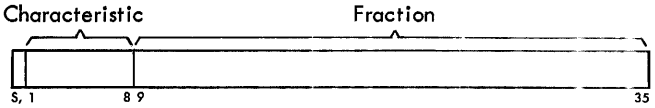
A floating-point decimal number X may be expressed as a signed proper fraction (N) multiplied by some integral power (n) of 10. The number is *normal* if the power of 10 (n) is chosen so that the decimal point is positioned to the left of the most significant digit of N. Examples:

X		N		10^n
−.010	=	−.10	×	10^{-1}
.140	=	.14	×	10^0
4.600	=	.46	×	10^1
88.000	=	.88	×	10^2

Likewise, a *floating-point binary number (X)* may be represented as a signed proper fraction *(B)* times some integral power *(b)* of 2. In the normalized case, the binary point is positioned to the left of the most significant digit of B. Examples:

X (BINARY)		B (BINARY)		2^b (DECIMAL)
−.001	=	−.100	×	2^{-2}
.100	=	.100	×	2^0
1.100	=	.110	×	2^1
110.000	=	.110	×	2^3

In the computer a floating-point number is stored in a word as shown. The fraction is contained in bit positions 9 through 35. A floating-point number with a 1-bit in position 9 is said to be normal. The sign of the fraction is contained in the S position of the word. The



Floating-Point Word Format

characteristic is formed by adding +128 to the exponent. For example, an exponent of −32 would be represented by a characteristic of 128 −32 or 96. An exponent of +100 would be represented by a characteristic of 100 +128 or 228. Since $128_{10} = 200_8$, the characteristic of a non-negative exponent always has a 1-bit in position 1, while the characteristic of a negative exponent always produces a 0-bit in position 1. A normal zero has no bits in both the characteristic and the fraction.

A procedure for converting numbers to floating-point notation can be illustrated.

Convert the Decimal Fraction .149 to Floating-Point Notation:

1. Convert to binary.
   $(1.49)_{10} = (.1142)_8 = (.001001100010)_2$
2. Enter this binary number into the fraction portion of the computer word with a zero (200_8) characteristic.
   10000000.001001100010 or $(200.1142)_8$
3. Normalize.
   1111110.100110001 or $(176.461)_8$ = answer

Convert the Decimal Integer 149 to Floating-Point Notation:

1. Convert to binary.
   $(149)_{10} = (225)_8 = 010010101$
2. Strike out leading zeros.
   10010101
3. Enter this binary number into the fraction portion of the computer word with a zero characteristic.
   10000000.10010101 or $(200.452)_8$
4. Add the octal number of binary digits in step 2 to the zero characteristic in the computer word.
   10001000.10010101 or $(210.452)_8$ = answer

FAD — Floating Add

Description: The floating-point numbers located in Y and the AC are added together. The most significant portion of the result appears as a normal floating-point number in AC. The least significant portion of the result appears in the MQ as a floating-point number with a characteristic 33 (octal) less than the AC characteristic. The signs of the AC and MQ are set to the sign of the larger factor. The sum in the AC and MQ is always normalized whether the original factors are normal or not. If $C(AC)_{1\text{-}35}$ contain zeros, the FAD may be used to normalize an unnormal floating-point number. C(Y) are unchanged.

Indicators: Floating-Point trap
Timing: 7040 — average 3 cycles
7044 — average 5.5 cycles
Type 6

FDP — Floating Divide or Proceed

Description: The C(AC) are divided by the C(Y). The quotient appears in the MQ and the remainder appears in the AC. If the magnitude of the AC fraction is greater than or equal to twice that of the $C(Y)_{9\text{-}35}$, or if the magnitude of the $C(Y)_{9\text{-}35}$ is zero, division does not occur and the computer takes the next instruction in sequence. The quotient is in normal form if both the dividend and divisor or in normal form. The sign of the MQ is the algebraic sign of the quotient. If the AC fraction is zero, the $C(AC)_{Q,\ P,\ 1\text{-}35}$ are cleared and the AC sign is set plus. C(Y) are unchanged.

Indicators: Floating-Point underflow, divide check
Floating-Point overflow
Floating-Point trap
Timing: 7040 — 7 cycles
7044 — 18 cycles
Type 7

FMP — Floating Multiply

Description: The C(Y) are multiplied by the C(MQ). The most significant part of the product appears in the AC and the least significant part appears in the MQ. The product of two normalized numbers is in normalized form. If either of the numbers is not normalized, the product may or may not be in normalized form. C(Y) are unchanged.

Indicators: Floating-Point trap
Timing: 7040 — average 4⅓ cycles
7044 — average 10 cycles
Type 8

FSB — Floating Subtract

Description: This instruction algebraically subtracts the floating-point number located in Y from the floating-point number in the AC, and normalizes the results. C(Y) are unchanged.

Indicators: Floating-Point trap
Timing: 7040 – average 3 cycles
7044 – average 5.5 cycles
Type 6

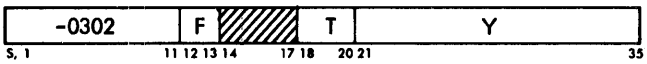
UFA – Unnormalized Floating Add

Description: This instruction algebraically adds two floating-point numbers contained in the AC and Y. The sum is not normalized. C(Y) are unchanged.
Indicators: Floating-Point trap
Timing: 7040 – average 2⅔ cycles
7044 – average 5.5 cycles
Type 9

UFM – Unnormalized Floating Multiply

Description: This instruction multiples the floating-point number at Y by the floating-point number in the MQ. The result is not normalized. C(Y) are unchanged.
Indicators: Floating-Point trap
Timing: 7040 – average 4⅓ cycles
7044 – average 10 cycles
Type 8

UFS – Unnormalized Floating Subtract



Description: This instruction algebraically subtracts the floating-point number located in Y from the floating-point number in the AC. The result is not normalized. C(Y) are unchanged.
Indicators: Floating-Point trap
Timing: 7040 – average 2⅔ cycles
7044 – average 5 cycles
Type 9

Floating-Point Trap

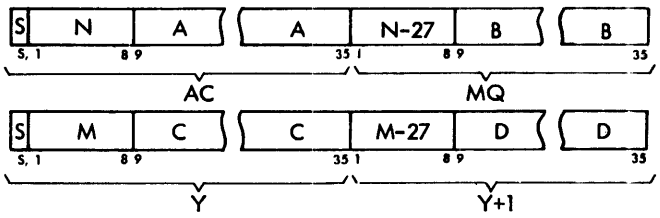
During the execution of floating-point instructions, the resultant characteristic in the AC and MQ may exceed eight bit positions (result is too large for storage). The capacity is exceeded if the exponent goes beyond +177 or below −200. Beyond +177 is termed overflow; below −200 is termed underflow. Overflow and underflow may occur in either the AC or the MQ register. The computer, on sensing an underflow or overflow, will put the address, plus one, of the instruction that caused the condition, into the address portion of location 00000. A spill indication is stored in the decrement portion of location 00000 as follows:

BIT	MEANING
S	Double-precision instruction (on machine equipped with single-precision only)
12	Double-precision Address Error
14	Single-precision Divide Instruction
15	Overflow in AC or MQ or Both
16	AC Overflow or Underflow
17	MQ Overflow or Underflow

The computer takes its next instruction from 00010. When a floating-point trap occurs, Trap Inhibit is turned on, preventing further traps. To enable trap, a TRP or TRT instruction is used.

Double-Precision Floating Point Instructions

Format:



Algorithms:

Add 1. B+D after equalizing n and m exponents.
2. +A addition of the smallest added first +C.

Multiply $(A^n + B^{n-27})(C^m + D^{m-27}) = AC^{n+m} + BC^{n-27+m} + AD^{n+m-27} + BD^{n-27+m-27}$

The last term of the above expansion is dropped, and the result is the sum of the first three terms.

Divide $\dfrac{A^n + B^{n-27}}{C^m + D^{m-27}}$

$$\frac{A+B}{C+D} = \frac{A+B}{C(1+D/C)}$$

$$= \frac{A+B}{C} - \frac{A+B}{C}\frac{(D)}{C}; \text{ Let } \frac{A+B}{C} = Q_1 + \frac{Ri}{C}$$

$$= Q_1 + \frac{Ri}{C} - (Q_1 + Ri/C)\frac{D}{C}$$

This can also be stated as:

$$= Q_1 + \frac{Ri}{C} - \frac{(Q_1 + Ri)}{C}\frac{D}{C}$$

$$= Q_1 + \frac{Ri}{C} - \frac{Q_1 D}{C} - \frac{Ri\,D}{C^2}$$

$$= Q_1 + \frac{Ri - Q_1 D}{C}; \text{ Let } \frac{Ri - Q_1 D}{C} = Q_2 + \frac{R_2}{C}$$

$$= Q_1 + Q_2$$

Final Answer $- Q_1^{n-m} + Q_2^{n-m-27}$

Four instructions are provided as an optional feature for handling double-precision floating-point arithmetic. The single-precision floating-point option is a prerequisite for this feature.

All double-precision numbers in memory must be located so that the high-order word is in an even location followed by the low-order word in the next higher odd location. If the effective address of a double-precision operation is odd, the instruction will be trapped as a floating-point trap (bit 12 will indicate this error). In this case, the operation will not be executed and the contents of the AC and the MQ remain unchanged. The rules for single-precision floating-point trap also exist. For overflow and underflow, the exponent of the major word of the result (in the AC) may not exceed $(+177)_8$ and the exponent of the minor word (in the MQ) may not be lower than $(-200)_8$. Double-precision instructions executed on a system with single-precision option only cause a trap operation.

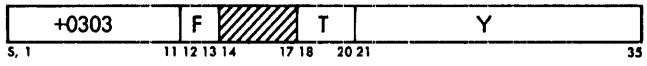
DFAD — Double-Precision Floating Add

Description: This instruction causes the double-precision number located at Y and Y + 1 to the number in the AC and MQ. The result is a normalized double-precision number with the major answer in the AC and the minor in the MQ. The sign of the AC and MQ will be that of the algebraic sign. C (Y and Y + 1) are unchanged.

Indicators: Floating-Point trap

Timing: 7040 — average 4⅓ cycles, signs alike
average 4⅔ cycles, signs unlike
7044 — average 8 cycles, signs alike
average 9 cycles, signs unlike
Type 10

DFSB — Double-Precision Floating Subtract

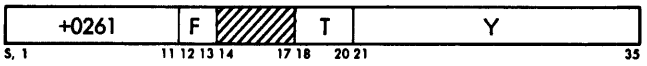


Description: This instruction is equivalent to DFAD with the sign of Y inverted.

Indicators: Floating-Point trap

Timing: 7040 — average 4⅔ cycles, signs alike
average 4⅓ cycles, signs unlike
7044 — average 9 cycles, signs alike
average 8 cycles, signs unlike
Type 10

DFMP — Double-Precision Floating Multiply

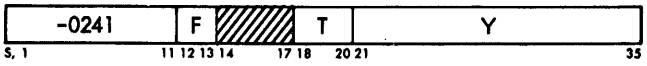


Description: This instruction causes the double-precision number in Y and Y + 1 to be multiplied by the number in the AC and MQ. The result is a normalized double-precision number in the AC and MQ with an associated algebraic sign. C (Y and Y + 1) are unchanged.

Indicators: Floating-Point trap

Timing: 7040 — average 12 cycles
7044 — average 31 cycles
Type 11

DFDP — Double-Precision Floating Divide or Proceed



Description: This instruction causes the double-precision number in the AC and MQ to be divided by the number of Y and Y + 1. The result is a normalized double quotient in the AC and MQ with an associated algebraic sign. Note that if C (see "Algorithm") is not normalized, there is a high probability that Q_2 will not be developed because of a divide check. In this instance, an end-operation will occur and the fraction portions of the AC and MQ will contain $R_1 - Q_1 D$. The sign and characteristic portions of the AC and MQ will contain intermediary information relating to the algorithm and, hence, will not be guaranteed. C (Y and Y + 1) are unchanged.

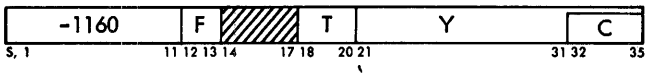
Indicators: Floating-Point trap, divide check

Timing: 7040 — average 17⅔ cycles
7044 — average 48 cycles
Type 12

Memory Protect Instructions

This feature provides a flexible means of protecting supervisory programs or subroutines from intrusions from untested object programs. Two auxiliary registers, set by the supervisory program, are compared against the high-order bits of an effective store address. One register, the count register, determines the number of high-order bits to be examined; the other register, the field register, determines the pattern of bits to be compared against. Violations — attempts to store data in a protected area — will cause trapping by either an equal or by an unequal compare result according to the selected protect mode. Two instructions are used.

SPM — Set Protect Mode



Description: This instruction will cause the field register to be set to the high-order seven positions of the effective address, and the count register to be set to the contents of the C field (positions 32-35). Bit 32 of the instruction controls the mode of protection, and bits 33-35 contain the count of the number of bits to be compared:

C FIELD (OCTAL)	BITS TO BE COMPARED IN EACH STORAGE SIZE 32K	16K	8K	4K	
0	None	None	None	None	
1	21	None	None	None	
2	21-22	22	None	None	
3	21-23	22-23	23	None	Trap if unequal compare result
4	21-24	22-24	23-24	24	
5	21-25	22-25	23-25	24-25	
6	21-26	22-26	23-26	24-26	
7	21-27	22-27	23-27	24-27	
10	None	None	None	None	
11	21	None	None	None	
12	21-22	22	None	None	
13	21-23	22-23	23	None	Trap if equal compare result
14	21-24	22-24	23-24	24	
15	21-25	22-25	23-25	24-25	
16	21-26	22-26	23-26	24-26	
17	21-27	22-27	23-27	24-27	

NOTE: A comparison of NO bits always results in an equal condition and hence never traps if the unequal mode is selected and always traps on a store operation if the equal mode is selected.

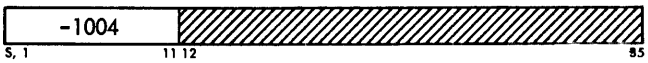
If the computer is already in the memory protect mode when the SPM instruction is given, the location of the SPM instruction, plus one, will be stored in the address part of location 32. Bit 16 will be set on (indicating a violation), protect mode will be turned off, Trap Inhibit will be turned on, and the computer will take its next instruction from location 33.

Indexing may be used to modify the effective address placed in the field register. The count register is not affected by indexing. If this instruction is indirectly addressed, the count register, field register, and tag register are replaced from the indirect location.

If an SPM instruction is given on a system that does not have the memory protect option, a no-operation results and the computer takes the next sequential instruction.

Indicators: Memory protect
Timing: 7040 — 1 cycle, no trap; 2 cycles, trap
7044 — 1 cycle, no trap; 2 cycles, trap

RPM — Release Protect Mode



Description: The location of the RPM instruction, plus one, replaces positions 21-35 of location 00032. Positions S, 1-20 of location 00032 are replaced by zeros. The computer then turns on Trap Inhibit and takes its next instruction from location 00033. If the computer is in memory protect mode, this instruction turns the memory protect mode off and stores a one in position 15 of location 00032. If the computer is not in memory protect mode when this instruction is given, a one is stored in position 14 of location 00032.

Indicators: Memory protect
Timing: 7040 — 2 cycles
7044 — 2 cycles

If this instruction is given on a system without the memory protect option, a normal RPM trap with memory protect off occurs. RPM trap, pre-interrupt trap, and violation memory protect trap all store in location 00032 and take their next instruction from 00033. Memory protect may also be released by the reset or clear keys. In this case no trap occurs.

Input-Output Instructions

Input-output instructions select and control input-output operations. They contain information necessary to accomplish the following functions:

Identify the I-O unit or buffer required and the channel to which it is attached.

Determine if the operation transmits data into core storage (read) or out of core storage (write). This information is contained in the operation code (positions S, 1-11) part of the select instruction.

Select appropriate code translators for serial-by-character devices (see "Code Translation").

Prepare the channel to accept a channel command word which is sent to the channel by a subsequent RCH instruction.

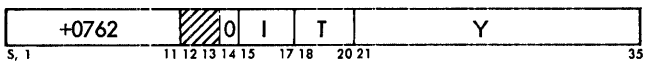
Start mechanical tape motion, if a magnetic tape unit is selected.

The I-O device, channel, I-O adapter, BCD address, and binary address used for all devices are:

DEVICE	CHAN.	ADAPT.	BCD MODE ADDRESS	BINARY MODE ADDRESS
Tape	A	0	01201-01212	01221-01232
	B		02201-02212	02221-02232
	C		03201-03212	03221-03232
	D		04201-04212	04221-04232
	E		05201-05212	05221-05232
Control Adapter	A		01000	01020
	B		02000	02020
	C		03000	03020
	D		04000	04020
	E		05000	05020
Direct Data Connection	B		02240	02260
	C		03240	03260
	D		04240	04260
	E		05240	05260
1622 Card Reader	A	3	01210	01230
1622 Card Punch	A	3	01211	01231
1402 Card Reader	A	3	01210	01230
1402 Card Punch	A	3	01211	01231
1403 Printer	A	3	01212	01232
Typewriter	A	4	01000	01020
1401 Data Processing System, On-line	A	5	01201-01212	01221-01232
1011 Paper Tape Reader (via 1414-4, 5)	A	3	01601	01621
1009 Data Transmission Unit (via 1414-4, 5)	A	3	01301	01321
1014 Remote Inquiry Unit (via 1414-4, 5)	A	3	01701-01702	01721-01722
Telegraph Type Units (via 1414-4, 5)	A	3	01401-01404	01421-01424

In the following instruction descriptions, Y signifies the address part of the word (positions 21-35). This field selects the channel and device to be used as shown in the table above. If a device is selected on channel A, additional information about the interface to be used is necessary. This information is contained in positions 15-17 and is designated by I. Positions 15-17 are not interpreted by overlapped channels B, C, D, and E. If the 1402 Punch is selected on Channel A, additional information about stacker selection is necessary. This information is contained in position 13 and is designated by S.

RDS — Read Select

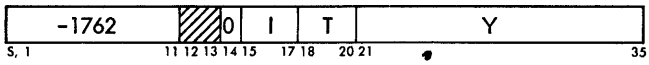


Description: This instruction causes the channel to prepare to read information from the I-O device specified by I and Y into core storage. Only positions 28-35 of the address part of the instruction are subject to effective address modification. Bit 14 must be a zero.

Indicators: Channel in use, redundancy check, end of file.

	729	7330	OTHER
Timing: 7040 —	2 cycles	4 cycles	1 cycle
7044 —	4 cycles	11 cycles	2 cycles
Type 13			

PRD — Prepare to Read



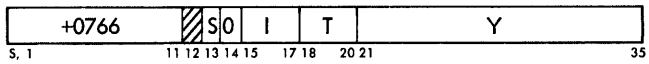
Description: On the 7040/7044 systems, this instruction is in all respects similar to RDS.

NOTE: If this instruction is executed on a 7090/7094/7094 II system, it will cause a store and trap, providing a convenient linkage to a routine that can simulate I-O functions not directly compatible with magnetic tapes from a 7090, 7094, or 7094 II system.

Indicators: Channel in use, redundancy check, end of file.

	729	7330	OTHER
Timing: 7040 —	2 cycles	4 cycles	1 cycle
7044 —	4 cycles	11 cycles	2 cycles
Type 13			

WRS — Write Select

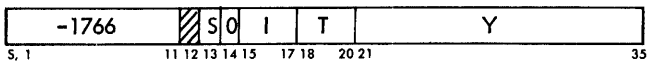


Description: This instruction causes the channel to prepare to write information from storage to the I-O device specified by I and Y. Only positions 28-35 are subject to effective address modification. Bit position 14 must contain a zero.

Indicators: Channel in use, redundancy check, end of file.

	729	7330	OTHER
Timing: 7040 —	2 cycles	4 cycles	1 cycle
7044 —	4 cycles	11 cycles	2 cycles
Type 13			

PWR — Prepare to Write

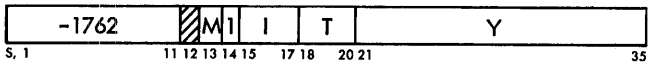


Description: On 7040/7044 systems, this instruction is in all respects identical to WRS. If this instruction is executed on a 7090, 7094, or 7094 II system, it will cause a store and trap, providing a convenient linkage to a routine that can simulate I-O functions not directly compatible with magnetic tapes from 7090, 7094 or 7094 II systems.

Indicators: Channel in use, redundancy check, end of file.

	729	7330	OTHER
Timing: 7040 —	2 cycles	4 cycles	1 cycle
7044 —	4 cycles	11 cycles	2 cycles
Type 13			

SEN — Sense Select



Description: This instruction causes the channel to prepare to read status data into core storage from the device specified by Y and I. Only positions 28-35 are subject to effective address modification. Bit position 14 must be a one. Refer to individual I-O device descriptions for status data received. When this instruction is used to sense a device on the 1414-3, 4, or 5, bit 13 denotes input-output buffers. A zero selects input buffers and a one selects output buffers.

NOTE: This instruction causes a store and trap operation on a 7090, 7094 or 7094 II system.

If this instruction addresses a device in the BCD mode, no translation occurs.

Indicators: Channel in use, redundancy check.

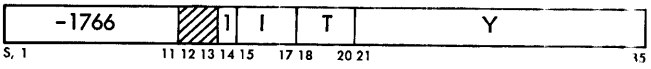
Timing: 7040 — 1 cycle
7044 — 2 cycles
Type 13

READY TEST

When a sense instruction addresses a device and is followed by an RCH that loads an IORD command with a word count greater than zero, the following sense data is stored by the channel in character zero of the first word (bits S, 1-5):

	BCD BIT	COMMENT
Tape on all Channels	B	Not Ready
	4	Rewinding (not ready is also on)
	1	Load point
Channel A		
1622 Card Reader	B	Not ready or busy
1622 Card Punch	B	Not ready or busy
1414-4	A	Forms busy
	B	Not ready
	8	Check status
	4	Busy
	2	Condition
	1	No transfer
	A	Not Used
Typewriter		None
1401	B	Not ready or busy
7904 Channels		
Control Adapter	B	Not operational
	A	
	4	Busy status
	2	Condition status
	1	No transfer status
	A	
	4	
	etc.	
Direct Data		None

CTR — Control Select



Description: This instruction causes the channel to prepare to send control information from core storage to the device specified by Y and I. Only positions 28-35 are subject to effective address modifications. Bit 14 must be a one. Refer to individual device descriptions for coverage of control orders and their effect. (This instruction will cause a store and trap on a 7090, 7094, or 7094 II system).

Indicators: Channel in use, redundancy check.

Timing: 7040 — 1 cycle
7044 — 2 cycles
Type 13

On-Line 1401 Select Instructions

Any select instruction specifying the on-line IBM 1401 Data Processing System destroys the C(MQ). The select instruction itself is transmitted to the 1401 as six BCD characters; the MQ is used for this operation.

Channel-in-Use Indicator

Each channel has associated a channel-in-use indicator with it. The indicator is turned on by any select instruction specifying that channel. Normally, this indicator remains on during the RCH to load the channel with a channel command and continues on throughout the execution of the channel command. It is then turned off at the completion of the channel command.

If a tape unit is selected by an RDS or WRS and an RCH instruction is not given in time, the tape unit automatically disconnects and the channel-in-use indicator is turned off. The critical times are listed under "Channel Control Instructions."

The channel-in-use indicator is also turned on by a BSR or WEF instruction and remains on for the duration of the backspace or end-of-file operation.

If a select, BSR, WEF, REW, or RUN instruction is given with the channel-in-use indicator on (as a result of a previous instruction), the execution of this instruction is delayed until the channel-in-use indicator is turned off.

Channel Control Instructions

After a select instruction has conditioned the channel to transmit information to or from a particular device, an RCH instruction must be given to deliver a command word to the channel. The command word contains a starting address and a word count to control the transmission of information to or from core storage.

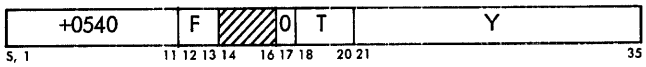
Since the select instruction initiates mechanical motion if a magnetic tape unit is specified, the RCH must be executed within a certain time after the select instruction. This time depends on the model of tape unit:

DEVICE	READ	WRITE
7330	3.7	6.2
729 II	4.0	6.5
729 IV	2.5	4.0
729 V	4.0	6.5
729 VI	2.5	4.0

All times are in milliseconds

Action is not initiated on devices other than tape units until the RCH is executed; hence, there is no limit to the time that may elapse between the select instruction and its associated RCH for these devices. If the RCH is not executed within the allowed time, the tape unit will disconnect, and the I-O check indicator will be turned on.

RCHA — Reset and Load Channel A



MNEMONIC	OP CODE	CHANNEL
RCHA	+0540	A
RCHB	−0540	B
RCHC	+0541	C
RCHD	−0541	D
RCHE	+0542	E

Description: If the channel has been conditioned by a select instruction, the C(Y) is sent to the channel as a channel command word. The channel is now prepared to transmit information to or from the selected device.

If the channel has not been conditioned by a select instruction, the I-O check indicator is turned on. The C(Y) is sent to the channel as a channel command word, but no transmission of information takes place.

If a second RCH instruction is given to a channel in operation, the C(Y) is sent to the channel and replaces the previous command word. Since the second RCH resets the data register of the selected channel, characters may be lost. This may also result in redundancy and word parity errors.

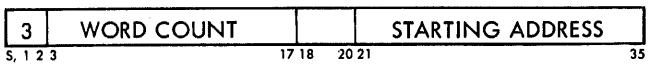
Because real-timing conditions vary widely among the data channels of the 7040/7044 and the 7090/7094/7094 II and also from nonoverlapped to overlapped channels on the 7040/7044, it is recommended that the channel be tested to be sure that it is no longer in use before using the data area assigned to the channel. This test may be done with a TCO instruction.

Indicators: I-O check

Timing: 7040 — 2 cycles
7044 — 2 cycles
On unoverlapped channel A, the execution of the RCH will not be completed until the channel-in-use indicator is turned off.

Channel Command

The RCH instruction causes a channel command word to be sent to the channel. Its format is:

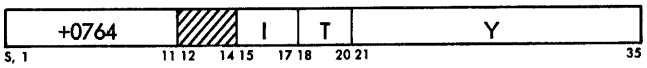


This word provides a 15-bit word count that specifies the length of the record and also a 15-bit starting address that specifies the location in core storage for the first word of the message. Additional words are taken from or sent to successively higher locations in storage until the end of the record on the I-O device or until the number of words specified in the word count have been transmitted, whichever occurs first.

The 7040/7044 systems do not interpret positions S, 1-2, and 18-20; however, the channels interpret the command as the 7090/7094/7094 II systems would if there were a three in S, 1-2, and zeros in 18-20.

Miscellaneous Data Channel Instructions

BSR — Backspace Record



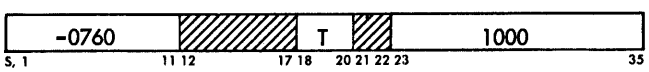
Description: This instruction causes the tape unit designated by I and Y to move backward until recorded information is reached. Tape motion is continued until an end-of-record gap or load point is encountered.

Execution: If the tape designated by I and Y is positioned at load point, the BSR is interpreted as a no-operation. Only positions 28-35 of the address part of this instruction are subject to effective address modification.

Indicators: Channel in use

	729	7330
Timing: 7040 —	2 cycles	4 cycles
7044 —	4 cycles	11 cycles
	Type 13,	Type 14

ETTA — End of Tape Test, Channel A



Description: This instruction is used to test the status of the data channel end-of-tape indicators. The channel

whose indicator is to be tested is specified by the address portion of the ETT instruction. The addresses for the channels are:

CHANNEL	ADDRESS
A	01000
B	02000
C	03000
D	04000
E	05000

If the end-of-tape indicator for data channel Y is on, the computer takes the next sequential instruction and turns the indicator off. If the indicator is off, the computer skips the next instruction and proceeds from there. The end-of-tape indicator is turned on when either a write select, write end of file, or erase tape causes the end-of-tape marker to be passed over.

Indicators: End of tape

Timing: 7040 — 1 cycle
7044 — 2 cycles

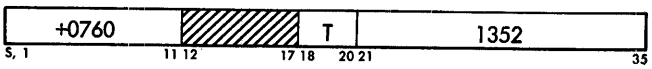
IOT — Input-Output Check Test

Description: If the I-O check indicator is on, the indicator is turned off and the computer takes the next sequential instruction. If the indicator is off, the computer skips the next instruction and proceeds from there. Any address modification may result in changing the operation itself.

Indicators: I-O Check

Timing: 7040 — 1 cycle
7044 — 2 cycles

RDCA — Reset Data Channel A



Description: This instruction resets all registers and indicators in the data channel specified by the address portion of the RDC instruction. Channel addresses are:

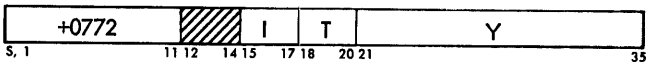
CHANNEL	ADDRESS
A	01352
B	02352
C	03352
D	04352
E	05352

All transmission is terminated and the selected units are immediately disconnected. If the instruction is executed while a tape is in motion, the tape is stopped *immediately* regardless of the position of the tape head with respect to the inter-record gap. All status indicators previously set by an enable instruction will be turned off. An RDC will cancel the effect of a previous select instruction.

Indicators: Channel in use, redundancy check, end of file, channel word parity, all trap requests, channel enable mask bits

Timing: 7040 — 1 cycle
7044 — 2 cycles

REW — Rewind



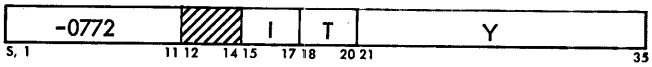
Description: This instruction causes the tape unit designated by I and Y to rewind its tape to the load-point position.

Execution: If the tape is positioned at its load point at the time the REW is interpreted, the instruction is treated as a no-operation. Only positions 28-35 of the address part of this instruction are subject to effective address modification. On a 7330 Magnetic Tape Unit, the instruction causes low-speed rewind.

Indicators: Channel in use

	729	7330
Timing:	7040 — 2 cycles	4 cycles
	7044 — 4 cycles	11 cycles
	Type 13, Type 14	

RUN — Rewind and Unload



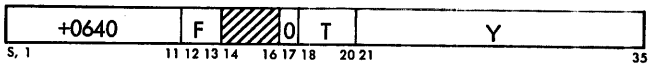
Description: The tape unit designated by I and Y will be rewound and then put into an automatic unload status.

Execution: This instruction will be executed in the same manner as a rewind instruction except that, after the rewind, a normal unload operation will occur. On a 7330 Magnetic Tape Unit, this instruction causes a high-speed rewind and unload. With 729 tapes at load point, this instruction causes an unload operation only. With 7330 tapes at load point, this instruction causes the channel to halt operation.

Indicators: Channel in use

	729	7330
Timing:	7040 — 2 cycles	4 cycles
	7044 — 4 cycles	11 cycles
	Type 13, Type 14	

SCHA — Store Channel A



MNEMONIC	OP CODE	CHANNEL
SCHA	+0640	A
SCHB	−0640	B
SCHC	+0641	C
SCHD	−0641	D
SCHE	+0642	E

Description: This instruction replaces the C(Y) 21-35 with the contents of the specified channel address counter. Positions 3-17 are replaced with the contents of the channel word counter. Positions S, 1, 2 and 18-20 are destroyed. Since channel A uses the AC 3-17 for its word counter and 21-35 for its address counter, it is necessary to give the SCHA before changing the AC after an RCHA. Note that the 7090/7094/7094 II systems do not store the word counter in positions 3-17 when an SCH is executed and, therefore, this portion of the stored word should not be used if compatibility is desired.

An SCHB instruction may be executed at any time, regardless of whether the specified channel is in operation. If the channel is in operation and the channel address register is in the process of being changed, the execution of the SCHB will be delayed until the change is completed.

The address register will be one greater than the storage location of the last word involved in data transmission.

Indicators: None

Timing: 7040 — 2 cycles
7044 — 2 cycles

TEFA — Transfer on End-of-File, Channel A

Description: If the end-of-file indicator for the specified channel is on, it is turned off and the computer takes its next instruction from location Y. If the indicator is off, the next sequential instruction is taken.

MNEMONIC	OP CODE	CHANNEL
TEFA	+0030	A
TEFB	−0030	B
TEFC	+0031	C
TEFD	−0031	D
TEFE	+0032	E

The end-of-file indicator in a data channel can be turned on by magnetic tape, a card reader, or the 1401 on-line system.

When an end-of-file is sensed during reading, the turning on of the channel end-of-file indicator logically disconnects the input-output device from the channel. The execution of the channel command is terminated immediately, even if it has not been completed.

If the channel IORD enable bit is a one, TEF will not transfer and will not turn off the end-of-file indicator.

Indicators: Channel end-of-file

Timing: 7040 — 1 cycle
7044 — 2 cycles

TCOA — Transfer on Channel A in Operation

Description: If the channel in use indicator is on for the specified channel, the computer will take its next instruction from location Y. Otherwise the next sequential instruction is executed. The operation of the channel is not affected.

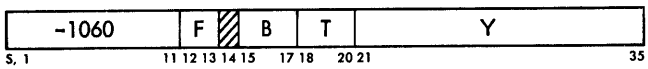
NOTE: TCOA is not a no-op. The channel in use indicator is turned on by a select instruction.

MNEMONIC	OP CODE	CHANNEL
TCOA	+0060	A
TCOB	+0061	B
TCOC	+0062	C
TCOD	+0063	D
TCOE	+0064	E

Indicators: Channel in use

Timing: 7040 — 1 cycle
7044 — 2 cycles

TDOA — Transfer on Channel A Device in Operation



Description: This instruction tests the busy status of individual I-O devices specified by the B character in bit positions 15 through 17.

B CHARACTER	DEVICE TESTED
1	Reader (1622 or 1402)
2	Punch (1622 or 1402)
3	Printer (1403)
4	Console Typewriter
5	On-line 1401

Execution: When the TDOA is given, the B character is sampled. The interface associated with the device is selected and the proper busy indication is sampled. If the device is in operation, the computer takes its next instruction from location Y. If the device is not in operation, the computer takes the next sequential instruction. This instruction will always transfer if Channel A is in use, regardless of the status of the device specified.

Indicators: Device busy indicators

Timing: 7040 — 1 cycle
7044 — 2 cycles

TRCA — Transfer on Redundancy Check, Channel A

Description: If the redundancy check indicator for the specified channel is on, it is turned off and the com-

puter takes its next instruction from location Y. If the indicator is off, the next sequential instruction is taken.

MNEMONIC	OP CODE	CHANNEL
TRCA	+0022	A
TRCB	−0022	B
TRCC	+0024	C
TRCD	−0024	D
TRCE	+0026	E

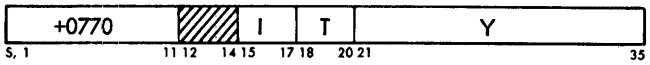
The redundancy check indicator is turned on by the channel if the channel detects a parity error on the data received during a read or sense operation. This indicator may also be turned on by the selected device. See input-output device descriptions.

If the channel parity enabled mask bit is set to one, the TRC does not transfer and does not turn the redundancy check indicator off.

Indicators: Channel redundancy check

Timing: 7040 — 1 cycle
7044 — 2 cycles

WEF — Write End-of-File



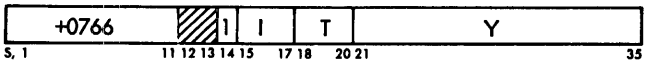
Description: This instruction causes the tape unit designated by I and Y to write an end-of-file gap followed by a tape mark (and its check character) on the tape.

Execution: If an end-of-tape reflective spot is passed over during execution of WEF, the end-of-tape indicator is turned on. Only positions 28-35 of the address part of this instruction are subject to effective address modification.

Indicators: End of tape, redundancy check, channel in use

	729	7330
Timing: 7040 — 1 cycle	4 cycles	
7044 — 4 cycles	11 cycles	
Type 13, Type 14		

WBT — Write Blank Tape



Description: If I and Y specify a magnetic tape unit, this instruction causes the tape to erase a long gap for approximately 3½ inches. This instruction is used to erase over bad spots in the tape which cannot be written over without a redundancy check. This instruction should not be followed by an RCH (except with an on-line 1401 where it *must* be followed by an RCH instruction).

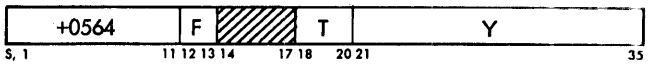
Indicators: End of tape, channel in use

	729	7330
Timing: 7040 — 2 cycles	4 cycles	
7044 — 4 cycles	11 cycles	
Type 13		

Trapping Instructions

The following instructions are used to condition data channel trap:

ENB — Enable from Y



Description: The contents of Y are used to set the channel mask bits to one or zero. Execution of each enable instruction cancels the effect of previous enable instructions. The enable instruction turns on channel trap control.

NOTE: Trap Inhibit must also be off to condition channel traps.

MASK BIT	CONDITIONS ENABLED	CHANNEL	EFFECTIVE IF A 1 IN BIT POSITION
Operation	Operation Complete, E O F, Word Parity, Unusual End, or End	A	35
Operation	Operation Complete, E O F, Word Parity, Unusual End, or End	B	34
Operation	Operation Complete, E O F, Word Parity, Unusual End, or End	C	33
Operation	Operation Complete, E O F, Word Parity, Unusual End, or End	D	32
Operation	Operation Complete, E O F, Word Parity, Unusual End, or End	E	31
Direct Data	Direct Data Interrupt	B	25
Direct Data	Direct Data Interrupt	C	24
Direct Data	Direct Data Interrupt	D	23
Direct Data	Direct Data Interrupt	E	22
Parity	Word Parity or Redundancy Check	A	17
Parity	Word Parity or Redundancy Check	B	16
Parity	Word Parity or Redundancy Check	C	15
Parity	Word Parity or Redundancy Check	D	14
Parity	Word Parity or Redundancy Check	E	13
Attention	1401 Interrupt or Teleprocessing Interrupt	A	8
Attention	Control Adapter Attention	B	7
Attention	Control Adapter Attention	C	6
Attention	Control Adapter Attention	D	5
Attention	Control Adapter Attention	E	4
Unit Record	Unit Record Interrupt	A	S

Execution of a trap or ICT instruction will inhibit all further traps until a new enable instruction is executed or a restore channel trap instruction is executed. Depression of the reset or clear keys, or execution of a

reset data channel instruction will set all mask bits in a channel to zero.

Note that use of ENB zero, although disabling all channel and direct data traps, prevents locating word parity errors in memory by use of the SCH instruction when a word parity error occurs on a channel write operation. It is wise, therefore, to use the ICT instruction when it is necessary to prevent channel traps.

RCT — Restore Channel Traps

Description: This instruction turns on channel trap control, allowing traps to occur as specified by the previous enable instruction. It cancels the inhibiting effect of an executed trap or an ICT instruction. The address part of this instruction is part of the operation code, and modification by an index register may change the operation itself.

NOTE: Trap Inhibit must also be off to condition channel traps.

Indicators: Channel trap control

Timing: 7040 — 1 cycle
7044 — 2 cycles

ICT — Inhibit Channel Traps

Description: This instruction turns off channel trap control, inhibiting all channel traps and direct data traps until an RCT instruction or a new ENB instruction is given. The address part of this instruction is part of the operation code and modification by an index register may change the operation itself.

Indicators: Channel trap control

Timing: 7040 — 1 cycle
7044 — 2 cycles

Direct Data Connection Instructions

The attachment of the direct data connection to any of the overlap channels (B, C, D or E) permits the attachment of many nonstandard I-O devices to the computer. Data are transmitted, a full word (36 bits) at a time, from the external device through the direct data connection to core storage. The external device has the ability, through the direct data connection, to interrupt normal computer operation when necessary to transfer data to or from core storage. Figure 7 shows the data flow.

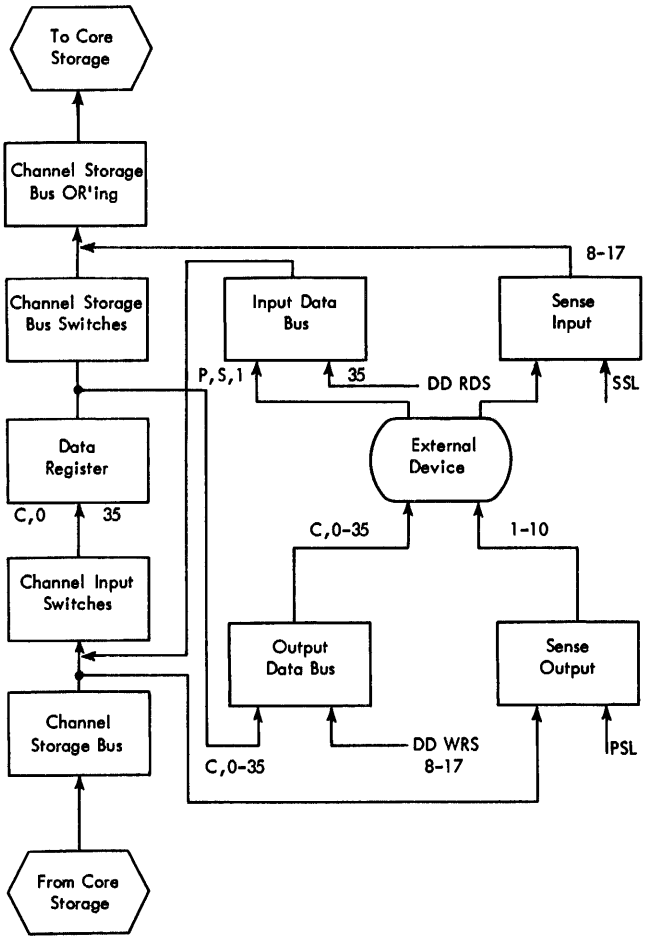


Figure 7. Data Flow, IBM 7904 Data Channel Direct Data

The external device is selected by an RDS or WRS with the address specifying a certain channel and direct data. Two new instructions are added to the instruction set for setting and testing the twenty sense lines to the external device. These sense lines are under program control.

PSLB — Present Sense Lines, Channel B

Description: A separate instruction is provided for each data channel and refers to positions 8 through 17 of the designated storage address Y. The instruction presents this bit configuration in pulse form to the direct data connection. The bit configuration is preceded by a reset pulse on a separate line.

Execution: Data channel designations with the proper operation codes are:

MNEMONIC	OP CODE	CHANNEL
PSLB	−0664	B
PSLC	+0665	C
PSLD	−0665	D
PSLE	+0666	E

Indicators: None

Timing: 7040 – 2 cycles
7044 – 2 cycles

SSLB — Store Sense Lines, Channel B

Description: A separate instruction is provided for each data channel. The instruction samples the static sense lines from the direct data I-O device and stores their information in positions 8 through 17 of the storage location specified by Y. A plus voltage level on the lines is decoded as a 1 bit.

Execution: Data channel designation with proper operation codes are:

MNEMONIC	OP CODE	CHANNEL
SSLB	−0660	B
SSLC	+0661	C
SSLD	−0661	D
SSLE	+0662	E

Indicators: None

Timing: 7040 – 2 cycles
7044 – 2 cycles

Input-Output Devices

This section describes the operation of input-output devices and associated control devices that may be attached to the IBM 7040 and 7044 Data Processing Systems.

The identifying number for input-output devices appears in the address part of the select instruction. For magnetic tape units, card machines, disk storage, and printers, the address part of the instruction specifies both the input-output device and the data channel to which it is attached. Channels A through E are specified by a number, 1 through 5, which appears as the first digit of a four-digit address. The last three digits specify the input-output device. If the device has either binary or BCD operation modes, the mode is also specified by the address.

On channel A, an input-output device is also associated with its adapter. The adapter is selected by an octal digit (0 through 5) in positions 15 through 17 of the select instruction. Position 13 of the select instruction is also used by certain input-output devices. When using the IBM 1414-3 Input-Output Synchronizer, for example, position 13 is used to select a stacker pocket on the 1402 card punch. The addresses of input-output devices and associated adapters are listed under "Input-Output Instructions."

Data Channels

Channel A Devices

Input-output devices and control units that may be attached to channel A include one each of the following:

1. One 1414-1, 2, or 7 Input-Output Synchronizer
2. Up to three 1414-3, 4, 5, or 8 Input-Output Synchronizers, or 1622 Card Read Punch.
3. One 1401 Data Processing System
4. One Console Typewriter (standard feature)

Each of the above units, with the exception of the 1622 card read punch and the console typewriter, may have individual input-output devices attached. Limitations of the number of these devices is as later stated in the description of each device.

Channel B Through E Devices

Each individual 7904 Data Channel has one input-output control adapter. This control adapter allows attachment of any one of the input-output devices designed to input-output control adapter interface specifications. Interface is defined as the actual signal, data, and control lines (and their precise cable connections) together with the necessary internal functions. In addition to the one input-output control adapter, each individual 7904 Data Channel may have one of the following devices:

1. One 1414-1, 2, or 7 Input-Output Synchronizer
2. One Direct Data Connection

The 7904 Input-Output Control Adapter allows attachment of any one of the following:

1. One 7631 File Control
2. One 1414-6 Input-Output Synchronizer
3. One 7750 or 7740 Programmed Transmission Control

IBM 1414-1, 2, and 7 Input-Output Synchronizers

These models of the 1414 perform a tape control function in the 7040/7044 systems. Up to ten tape units may be attached to any 1414 unit as follows:

1414-1	729 II and 729 IV, 729 V (if the 1414 is equipped with the 800 CPI feature), 7330 (if the 1414 is equipped with the tape intermix feature).
1414-2	7330 tape units
1414-7	729 II, IV, V, VI, and 7330 (if the 1414 is equipped with the tape intermix feature).

The tape units operate in either binary or BCD modes under program control, as specified in the address portion of the select instruction.

Ten select lines from the channel to the 1414 accomplish actual selection of an individual tape unit. The lines are activated by the address portion of the select instruction and, coupled with the setting of the tape unit's address selection switch, select a particular tape unit for use. The tape unit selected must be in a ready state.

When six-bit BCD characters are read from tape, the zone bits of some of the characters are altered. This alteration is performed so that the digits 0-9 and the characters A-Z are represented in core storage by six-bit binary numbers of increasing magnitude. The alteration of these zone bits is:

CHARACTER	IN CORE STORAGE		ON TAPE	
	B	A	B	A
Numeric	0	0	0	0
A to I	0	1	1	1
J to R	1	0	1	0
S to Z	1	1	0	1

The digits 1 through 9 or represented by the six-bit binary numbers 000001 through 001001 and the zone part of the digits is 00. The number zero is represented on tape by the bit configuration 001010. This number

is automatically altered to 000000 during reading in the BCD mode. During writing in the BCD mode, the alteration is reversed so that storage BCD characters are transformed to BCD tape format. The zone bits are altered and the number 000000 is replaced by 001010. For a complete description of translations, see "Character Coding and Translation."

END-OF-TAPE INDICATOR

When the strip signaling the physical end of tape is reached during a write operation, the end-of-tape indicator in the channel to which the tape unit is attached is turned on. No interruption in the writing process occurs; writing may be completed even though the end-of-tape strip has been passed over. If the indicator status is ignored, however, and writing continues, the tape may eventually be pulled from its reel. This indicator is never turned on during a read operation.

END-OF-FILE INDICATOR

The channel end-of-file indicator is turned on only when a single character tape mark record is read during a channel tape read operation. An end-of-file may be written on a tape at any time by the write end-of-file (WEF) instruction. The end-of-file indicator is not turned on when an end-of-file is written.

REDUNDANCY CHECK INDICATOR

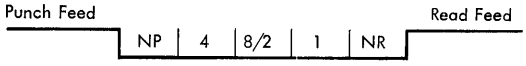
The channel redundancy check indicator may be turned on at any time during a tape read or write operation. Any of the 7 conditions in the 1414 turns on this indicator:

Read-write register – parity error	(read or write)
Longitudinal redundancy error	(read or write)
Skew register error	(read or write)
Read-write register-delay noise	(read or write)
Skew register A – parity error	(write only)
Skew register A and B compare	(write only)
Write echo error	(write only)

IBM 1622 Card Read Punch

This unit operates at a speed of 250 cards per minute while reading and 125 cards per minute while punching. The read and punch portions are separate and functionally independent, with separate switches, lights, checking circuits, and buffer storage. When the 1622 is attached to channel A, the 1414-3 or 4 synchronizer may not be used. Likewise, with a 1414-3 or 4, the system cannot have a 1622.

Two card stackers are provided for each feed unit; one for normal stacking and the other for error selected stacking. The physical locations of stacker pockets and their use by the 1622 are:



Pocket NP is for normal punch operation, pocket 4 is for error punch, pocket 8/2 is not used, pocket 1 is for error read, and pocket NR is for normal read operations.

Read Operation

Cards are read 9-edge first, face down, past two reading stations: check and read. The read buffer is initially loaded with 80 columns of card data during a start or load run-in operation. Thereafter, each card feed cycle is under program control. The reader can accept and translate card codes equivalent to the 64 combinations of six bits (with optional feature).

The channel transfers data to storage until 80 characters are read or until the word count is reduced to zero, whichever occurs first. This results in an efficient read operation, because reading one card per command allows the CPU to process while the mechanical card reading process is taking place.

A read select directed to the 1622 causes a read signal to be sent to the reader. If the read buffer is not ready, the read signal is delayed. On receipt of the signal, the 1622 takes a read buffer cycle and transmits one data byte. A service request is also sent to indicate the presence of the byte. The channel takes the byte into the MQ register and sends a response to the 1622. This response causes another read buffer cycle and another byte is transferred. This request and response process continues until the entire read buffer is emptied. The channel stops data transmission when the word count goes to zero but remains connected to the 1622 until the end-of-record signal occurs. The channel then ends operation and the 1622 proceeds to read the next card into the read buffer. The previous card is stacked in the NR pocket unless an error has occurred.

Special Read Conditions

1. Each card is read at two different places and the results of the readings are compared. An unequal comparison is called a hole check. If a hole check error is detected, the card feed stops, ready status is ended, and the reader check indicator is turned on. The card in error is placed in the error stacker. A transfer-on-device-in-operation directed to the reader results in a transfer, and the read select instruction causes the channel to halt operation. The channel redundancy indicator is not turned on and manual intervention is required. The error card is placed in pocket 1.

2. Each data byte is parity checked as it leaves the read buffer and, if a parity check is detected, the 1622 follows the same procedure as with the hole check. All conditions are the same, except the error card is placed in the normal stacker.

3. Each byte received by the channel is parity checked. If a parity check is detected, the channel redundancy indicator is turned on and the read operation continues to normal completion. The redundancy indicator should be checked by the program to assure that the transfer was valid.

4. An end-of-file signal is sent to the channel when the last card in the read feed has been transmitted. The signal turns on the channel end-of-file indicator when the next read select addressing the reader is given.

Write Operation

Cards are fed 12-edge first, face down, past the punch and check stations. All of the 64 combinations of six bits (with optional feature) can be translated and punched. Information is transferred from storage until 80 characters are written or until the word count is reduced to zero. A write select instruction addressing the 1622 results in a service request for the first byte. The 1622 stores this byte (when received) in its punch buffer and then requests the next byte. This request and response process continues until the entire punch buffer is filled. When the word count goes to zero, the channel stops sending words but continues sending blanks to the 1622 until an end-of-record signal is received. The channel now ends operation and the 1622 proceeds to punch the data just transferred. The card is placed in the NP pocket unless a parity or punch check occurs.

Special Write Conditions

1. The channel checks parity on all words sent from storage. If a parity error is detected, the channel word parity indicator is turned on and an error signal, which prevents the error record from being punched, is sent to the 1622.

2. The 1622 checks parity on all bytes received from the channel and on all bytes punched out of the punch buffer. If a parity error or a punch error is detected, a cycle delay is started and the punch is stopped one card feed cycle after punching the incorrect data. Ready status is terminated and the punch check light is turned on. A TDOA instruction directed to the punch will not transfer and a write select instruction fills the punch buffer, but no punching occurs. The next TDOA directed to the 1622 transfers, and a write select instruction will now halt operation. The channel redundancy check is not turned on and manual intervention is required to clear the condition. The error card is placed in pocket 4.

IBM 1414-3, 4, 5, and 8 Input/Output Synchronizers

These models of the 1414 provide data buffer storage and control functions for the following units:

1414-3
- 1402 Card Read Punch
- 1403 Printer

1414-4
- 1402 Card Read Punch
- 1403 Printer
- 1402 Column Binary Adapter. Two buffers are required (one adapter per 1414).
- 1009 Data Transmission Unit Adapter. One adapter controls one 1009. Two buffers are required (one adapter per 1414).
- 1011 Paper Tape Reader Adapter. One adapter controls one 1011. One buffer is required (One adapter per 1414).
- 1014 Remote Inquiry Unit Adapter. One adapter controls up to ten 1014's. Two buffers (one for input and one for output) are required for each adapter (maximum of two adapters per 1414).
- Telegraph Input-Output Feature Adapter. One adapter attaches two simplex circuits, or one half-duplex, or one full-duplex circuit. Two buffers are required for each adapter (one adapter per 1414).
- Additional Telegraph Input Feature Adapter. One adapter attaches one simplex, one half-duplex, or one full-duplex circuit, in conjunction with the additional telegraph output feature. One buffer is required for each adapter (maximum of two adapters per 1414).
- Additional Telegraph Output Feature Adapter. One adapter attaches one simplex circuit, one half-duplex, or one full-duplex circuit, in conjunction with the additional telegraph input feature. One buffer is required for each adapter (maximum of two adapters per 1414).

1414-5
- Only the communication-oriented input-output devices used on the 1414-4 are available on the 1414-5.

1414-8
- 1403 Printer

With communication-oriented devices, any combination of the optional adapters is permitted, provided that the limitation on the multiples of the same adapter and the limit of six data buffers per 1414 is not exceeded.

Read Operation — 1402

The read buffer is initially filled when cards are fed into the reader by the operator. Whenever a read operation is executed, the entire contents of the buffer are read out and a card feed cycle refills the buffer with the contents of the next card. The actual storing of data is under control of the IORD command. One IORD command is required for each card read, but up to 80 characters may be read from the card. Since each core storage location can contain six characters, 13 complete word locations are used and the 12 high-order

positions of a 14th location contain the 79th and 80th characters (Low-order positions are replaced with zeros). For a normal operation, the program uses an RDS instruction followed by an RCH, which loads the IORD command into channel registers. The RDS selects the read buffer, but no action is taken until the following RCHA. Hence, the time between the RDS and the RCHA is variable.

Special Read Conditions — 1402

1. The 1414-3 recognizes 64 valid characters. Any card code that does not result in a valid character causes a reader validity error. Channel A redundancy check is turned on when the RDS is given for that card, and the card is placed in the NR pocket.

2. When a card passes the read check station, the number of holes in the card are counted. As the card passes the read station, the number of holes is compared with those previously counted. A hole count check occurs if the comparison is not equal, and the channel A redundancy check is turned on when the RDS is given for that card. The card is placed in the NR pocket.

3. Data read from the buffer are checked for proper parity by the CPU. If a parity error is detected, the redundancy check indicator is turned on. The program should test this indicator for the corrective action required.

4. A not-ready condition results from reader out of cards and not end of file, reader in manual status (off-line), or reader power off. These conditions require operator intervention. When a read select instruction is executed for the reader, the CPU halts operation.

5. If a hole count or parity error is detected, the channel redundancy check indicator is turned on and may be tested by the program.

6. If the buffer is being filled, a read buffer busy condition exists. If a read select is given, the CPU waits for a not-busy condition.

7. The end-of-file indicator in the 1414 is turned on after data from the last card have been sent to core storage. On the next select instruction to the reader, the end-of-file indicator in the CPU is turned on and the end-of-file indicator in the 1414 is turned off.

Punch Operation — 1402

The punch buffer has a capacity of 80 characters plus parity. Words are sent to the punch in the same way as with the reader, except that a write select instead of a read select instruction is used. When C words have been sent to the punch, blanks are inserted in unfilled buffer positions. When the buffer is full, a punch card feed cycle is initiated. The channel is then disconnected and the CPU executes the next sequential instruction. For a normal punch operation, the program uses a WRS followed by an RCHA, which loads the IORD command into the channel registers. The WRS selects the buffer but no action occurs until the RCHA instruction is executed.

The program can select one of two pockets in the 1402 to stack the punched cards. If the write select instruction has a zero in position 13, the card is stacked in pocket 4. If the write select instruction has a one in position 13, the card is stacked in pocket 8/2. In either case, if a punch buffer parity check or a hole count check occurs, the card is stacked in the NP pocket.

Special Punch Conditions — 1402

1. The buffer contents are parity checked during punching and, if an error is detected, the buffer check indicator in the 1414 is turned on. On the next select punch instruction, the redundancy check indicator in the channel is turned on. If a punch buffer parity occurs, the card is placed in the NP pocket.

2. As the buffer is read out, a hole count is retained by the 1414. On the next card feed cycle, the card passes the punch check station and the holes are again counted and compared with the previous hole count. If the comparison is not equal, the hole count check indicator is turned on. If a select punch instruction is given and the hole count check is on, the redundancy check indicator in the CPU is turned on and the card is placed in the NP pocket.

3. Character parity is checked against word parity as the data are placed in the punch buffer. If an error is detected, the word parity indicator in the channel is turned on.

4. When a select instruction is given to the punch, the not-ready and busy conditions are the same as with the reader. If there has been a hole count or a parity error on the previous card feed cycle, the redundancy check indicator in the CPU is turned on and the card is placed in the NP pocket.

Print Operation — 1403

The IBM 1403 Printer has 100 printing positions per line, with an additional 32 positions available as an optional feature. Transfer of print characters is under control of the IORD command. If the word count is greater than 16 (or 22), only the first 100 (or 132) characters are transferred to the print buffer. If the word count is equal to or less than 16 (or 22), the print buffer is filled out with blanks. When the buffer is full, the channel signals to print the line. The channel is then disconnected and the CPU proceeds to the next sequential instruction. For a normal print operation, a WRS is used, followed by an RCHA, which loads the IORD command into the channel registers. The operation proceeds similar to the punch operation.

Carriage Control Operation

The printer carriage is controlled by a special control character. This character is sent to the printer by a control (CTR) followed by an RCHA, which loads the IORD command with a word count of one or more. A word count of zero causes a carriage return without printing. The character defined in bit positions S, 1-5 of the data word is used. The channel then disconnects and the CPU executes the next sequential instruction. The control characters are shown in Figure 8.

Control Character	Function: Immediate Skip to	Control Character	Function: Skip After Print to
1	Channel 1	A	Channel 1
2	Channel 2	B	Channel 2
3	Channel 3	C	Channel 3
4	Channel 4	D	Channel 4
5	Channel 5	E	Channel 5
6	Channel 6	F	Channel 6
7	Channel 7	G	Channel 7
8	Channel 8	H	Channel 8
9	Channel 9	I	Channel 9
0	Channel 10	?	Channel 10
#	Channel 11	.	Channel 11
@	Channel 12	□	Channel 12
	Immediate Space		After Print Space
J	1 Space	/	1 Space
K	2 Spaces	S	2 Spaces
L	3 Spaces	T	3 Spaces

Figure 8. BCD Carriage Control Characters

Special Print Conditions

1. Buffer contents are checked for parity during printing. If a parity error is detected, the buffer parity check indicator in the 1414 is turned on. On the next select printer operation, the redundancy check indicator in the CPU is turned on.

2. During printing, the printer circuitry determines if the proper character has been printed. If an error is sensed, the next printer select instruction turns on the redundancy check indicator in the CPU.

3. The printer-not-ready condition is caused by printer out of forms, printer in manual status (off-line), or printer power off. When the printer is selected by the CPU and is not ready, the CPU halts operation.

4. The printer-busy condition occurs when the printer is selected and the previous line is still being printed. If the printer is selected while in busy status, the CPU waits for a not-busy condition.

5. If a parity or print error has been detected by the 1414 during the preceding print cycle, the channel redundancy check indicator in the CPU is turned on.

6. Character parity is checked against word parity as the data are placed in the print buffer. If an error is detected, the word parity indicator in the channel is turned on.

IBM 1414-4 Input-Output Synchronizer

The 1414-4 combines the unit record equipment of the 1414-3 with an optional column binary feature and attachment of communication-oriented devices and paper tape devices. There are six 80-character buffers in addition to the buffers required for the unit record equipment assigned to specific input-output adapters.

The control instruction prepares the 1414-4 to receive orders in the form of data. The 1414-4 interprets these orders as select addresses and selects the desired I-O device. The sense instruction prepares the 1414-4 to send status data to the computer when the next RCH instruction is executed in the CPU.

Column Binary Feature

This optional feature permits reading or punching of column binary or BCD cards intermixed on the 1402 Card Read Punch. The column binary card is identified by 7 and 9 punches in card column 1. The 7-9 punches are sensed at the read check station of the 1402 Card Read Punch. The card is then read at the read station so that card rows 12-3 are read into one buffer and rows 4-9 are read into another buffer. If no 7-9 punches are sensed, the card is read in a normal fashion.

The reading of a column binary card into the buffers indicates to the computer the type of data to be received on the next read instruction. Execution of a read column binary operation takes the first character from rows 12-3 of card column 1, the second character from rows 4-9 of card column 1, the third character from rows 12-3 of card column 2, and so on, until all 80 card columns have been read. A maximum of 160 characters may be recorded.

Information transfer with a write punch operation places the transferred data into the buffers in the same manner as the data were taken out on the read operation. The 7-9 punches for card column 1 must be provided in the data to be recorded if they are to appear in the output cards.

The instruction sequence would be a sense instruction followed by a reset and load channel instruction, which loads the IORD command into the channel. When the RCHA is executed, sense data are placed in the six high-order bit positions of the word location specified by the IORD command. The six bit positions (when they contain 1's) and their meaning is shown in Figure 9.

The sensed data can be checked by the program so that it can issue the proper read select instruction (binary or BCD). An RCH instruction with the IORD command transmits the information and can be followed immediately by another sense instruction to determine the format of the next card.

IBM 1414-3, 4, 5, and 8 Input/Output Synchronizer Operation

Input Operation

Normal input operation from any input buffer uses an RDS or PRD instruction followed by an RCHA instruction that loads an IORD command into the channel. The select instruction selects the proper input buffer, but no action occurs until the RCHA is given. Therefore, no time limit exists between the select and the RCHA.

The select instruction also samples the check status of the input buffer. If a check exists on the record in the buffer, the channel A redundancy check indicator is turned on. During the RCHA, the characters are also checked for parity as they enter the channel and, if improper parity exists, the channel A redundancy check indicator is turned on.

Output Operation

Normal output operation to any of the output buffers uses a WRS or PWR instruction followed by an RCHA instruction which loads an IORD command into the channel. The select instruction selects the proper output buffer, but no action occurs until the next RCHA. Therefore, no time limit exists between the select and the RCHA. The select also samples the status of the output buffer. Normally, this is the status of the previous record; in a card punch operation, it is the status of the card punched before the previous card. If a check occurs on this record, the channel A redundancy check indicator is turned on.

During the output data transfer, the 1414 checks for proper parity on the data sent by the CPU. If an error occurs, the channel A redundancy check indicator is turned on. If the redundancy check indicator is on at the end of an output transfer, the output buffer is not emptied, and the data transfer from the 1414 is effectively cancelled.

Position	Condition
B-Bit	Card reader is not ready
4-Bit	Card is in process of filling the buffer
2-Bit	Card Reader end of file
1-Bit	Data in the buffer are in column binary format

Figure 9. Column Binary Feature Sense Data

Sense Operation

Each buffer has associated with it several status bits which can be examined by the sense (SEN) instruction. The SEN addresses the device to be sensed; a 1 bit in position 13 of the SEN specifies an output buffer and a 0 bit in position 13 specifies an input buffer. After the SEN, an RCHA that specifies the location of the IORD command to be loaded into the channel must be given. One character (containing the status bits) is sent to core storage and placed in the first six positions of the first word location specified by the command. The remainder of the word location is set to zero. Status bit positions and their names are:

BIT	POSITION CHARACTER	STATUS NAME
S	B	Not Ready
1	A	Forms Busy
2	8	Check
3	4	Busy
4	2	Condition
5	1	No Transfer

NOT READY

This bit indicates that operator intervention is needed to make the buffer operational. If a device is not ready and is selected by other than a SEN, the CPU waits until the device becomes not busy.

FORMS BUSY

Indicates that the forms character register has received a command and has not completed execution of that command.

CHECK

For an input buffer, this bit indicates that a check occurred during the filling of a buffer. A SEN turns this bit to a 0 bit except for a card read operation. If this bit is a 1 when a read select is given to the buffer, the channel A redundancy check indicator is turned on.

For an output buffer, this position indicates that a data transfer parity check occurred during the RCHA. If bit position 2 is a 1 bit, the channel A redundancy check indicator is turned on during the RCHA and bit position 2 is reset to a 0 bit. If channel A redundancy check indicator is on (regardless of when it was turned on) at the end of an RCHA to an output buffer, the CPU cancels the data transfer and the record is not sent from the buffer to the output device. The check status bit is never on (never contains a 1 bit) for an output device during the sense operation, and it will not be discussed with the output devices.

BUSY

This position indicates, for an input buffer, that the buffer is in the process of filling or being emptied. If a busy device is selected by other than a SEN, the CPU waits until the device becomes not busy.

CONDITION

For an output buffer, this position indicates that an error has occurred during transfer of the previous record from the buffer to the output device. With a card punch operation, this position refers to the card before the previous card. If this position contains a 1 bit (for an output buffer) when it is selected with a WRS or PWR, the channel A redundancy check indicator

is turned on. The condition status bit meaning varies for each input device. With a card reader, it indicates end of file, and a RDS or PRD selecting the card reader with a 1 bit in the condition status position turns on channel A end of file indicator. A SEN operation must be used to check the condition status bit contents.

NO TRANSFER

This position indication varies for each input-output device and is discussed under individual device descriptions.

Unit Record Interrupt

This interrupt, when enabled, can request a channel A trap to signal the program that one of the unit record devices has completed its cycle. The following conditions can request a unit record interrupt:

Card reader buffer is full
Paper tape reader buffer is full
Card punch buffer is empty
Print buffer is empty

The initial run-in of cards on the card reader or of paper tape on the paper tape reader does not request a unit record interrupt.

Communication Equipment Interrupt (Tele-processing)

On the 1414-4, this interrupt, when enabled, can request a channel A trap (even if the channel is in use) to signal the program that one of the communication device buffers is full or that an output buffer is empty (including the 1009, 1014, and telegraph input-output buffers).

On the 1414-6, these same devices use the corporate standard interface (CSI) control adapter attention condition to signal an interrupt from channels B through E.

Interrupt Operations — 1009 (Applies to 1414-4 and 1414-6)

OUTPUT OPERATION — CPU TO 1009 VIA 1414

1. A 50-character message uses one output buffer. Only one "buffer empty" trap will occur. The EOM indication (# #) must be used.

2. An 80-character message (card image records) uses two output buffers. When two output buffers are used, the difference between the 1414-4 and 1414-6 operation on the initial two write selects is as follows.

1414-6: After the first write select, 80 characters are transmitted to the first buffer. A "buffer empty" interrupt will occur because the second buffer is initially empty. (A sense instruction normally follows a buffer interrupt.) A second write select should then be given. The second buffer now contains the EOM (# #) indication in the first two character positions of the word transmitted to the 1414. This EOM suspends the interrupt normally expected due to the first buffer going empty. Suspension of the interrupt is maintained until both buffers have completed the transfer to the 1009. The EOM (# #) indication enters the 1414 but is not transmitted.

1414-4: The initial write select is given to the synchronizer. A "buffer empty" interrupt will not occur; instead, a second write select must be given. When the first buffer empties, an interrupt will be generated unless the second buffer contains the EOM.

NOTE: If the second write select does not follow the first write select before the emptying of the first buffer, another successive write select will be required.

Normal transmission will continue by writing to the 1414 every time a "buffer empty" interrupt occurs until an EOM is detected. The data will automatically enter an output buffer (no program control to determine which buffer is used).

INPUT OPERATION — 1009 TO CPU VIA 1414

1. A 50-character message uses one buffer. A trap will occur when the buffer becomes full.

NOTE: A second trap will occur "one-character-time" after the "buffer full" trap. The EOM bit will be set in the sense data for the 1414 synchronizer. The character time is a function of the speed selection switch located on the 1009.

2. An 80-character message uses one or two buffers, depending on the terminal device attached at the remote locations. For example, if the 7702, 1410, or 1401 is used as the terminal device, it will transmit 80 characters to the 7040. Two "buffer full" interrupts can be expected for each card image received; the second will be the EOM interrupt. If the 1013 card transmission terminal is used as the terminal device in fixed program operation, it will transmit 81 characters to the 7040; the eighty-first character is a group mark. The programmer should expect three interrupts. The group mark will require that a second read be given. The programmer can edit-out this group mark if it is not desired. This 1013 interrupt handling is common for both the 1414-4 and 1414-6. When operating with a 1013, the 1009 must be in BCD mode.

3. When any message length from 81 through 159 characters is defined and the first buffer is not read into the CPU before the second buffer fills, only two interrupts can be expected: a "buffer full" interrupt (for both buffers filling) and an EOM interrupt. The "busy" line status is turned off (generating a "buffer full" interrupt) when the first buffer is filled and is turned back on when a transfer scan (read-in) to the CPU occurs. ("Busy" is defined as a "buffer waiting to be filled" or "buffer is in the process of filling.") However, in this case, "busy" line status will stay off

until both buffers have been read into the CPU.

NOTE: The EOM interrupt cannot be set until the last buffer of any length message is read into the CPU.

A sense instruction should always follow the "buffer full" interrupt to decide which device is requesting service as determined by the "busy" line.

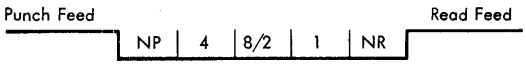
IBM 1402 Card Reader Operation

The 1414 storage buffers associated with the 1402 card reader are an 11-plane, 80 position storage unit. Cards are read 9-edge first in regular IBM card code, translated into 6-bit code plus parity, and stored in the read buffer.

When an RCHA is given, the contents of the card that had previously filled the buffer are transferred to the CPU. At the same time, card motion is started to feed in the next card. The card whose contents are being transferred to the CPU will be stacked in pocket 1 unless a hole-count check or reader validity for that card has occurred; in this case, the card is stacked in the NR pocket.

The physical locations of the stacker pockets on the 1402 are similar to those on the 1622. Stacker pocket uses are:

POCKET	COMMENT
NP	Error Punch
4	Normal Punch
8/2	Selected Punch
1	Normal Read
NR	Error Read



READER STATUS BITS

Not ready: The reader not ready status results when: the reader is out of cards but the end of file signal has not occurred, the reader is off-line, reader power is off, or the operator presses the stop key on the reader.

Check: Without 7 and 9 punches in column 1 of the card, or if the column binary feature is not installed, the 1414 recognizes 64 valid characters. Any card code that is not valid character causes a reader validity error, which sets the reader check status. When a card passes the read check station in the reader, the holes in the card are counted. As the card passes the read station (the next read station), the number of holes is compared; a hole-count check occurs if the counts are not equal, and the reader check status is set. Reader check status is not turned off with the SEN operation. If reader check status is on, the channel A channel check indicator is turned on when the RDS is given for that card. The card will be stacked in the NR pocket.

Busy: The read buffer busy status indicates that a card is filling the buffer.

Condition: This status bit indicates end of file and is turned on after the last card has been transferred from the buffer to the CPU if the end of file key has been pressed by the operator. This indicator may be sensed and turned off by the SEN. A read select instruction to the reader turns on the channel A end of file indicator and the indicator in the 1414 is reset. An RCHA given after the reader is selected with the channel A end of file indicator on results in an immediate disconnect, regardless of how the channel A end of file indicator was turned on.

No Transfer: This status bit is only used with the reader on the 1414-4 when the column binary feature is installed. The status indicates that the card in the read buffer has a 7-9 punch in column 1 and 160 characters of information are available.

IBM 1402 Card Punch Operation

On punch operations, 6-bit characters plus parity are accepted from the CPU and placed in the punch buffer. A signal from the CPU initiates a punch feed operation and the characters are scanned out of the buffer, translated to IBM card code, and punched 12-edge first.

PUNCH STATUS BITS

Not Ready: This status bit results from: the punch being out of cards, punch off-line, punch power off, or pressing the punch stop key.

Check: This bit is not used by the punch.

Busy: This busy status indicates that the punch is punching a card.

Condition: During the punch operation the buffer is checked for proper parity and the number of holes punched in each column. After the card is punched, the buffer waits until it is selected and filled to punch the next card. While the second card is being punched, the first card passes a read station where the holes in each column are counted and compared against the number that should have been punched. If there is a hole-count check on the first card or if a parity error was detected on the second card during punching, the punch condition indicator is turned on after the second card is punched. The card punched in error will be stacked in the NP pocket. The punch condition indicator may be turned off with a SEN instruction.

No Transfer: This bit is not used by the punch.

IBM 1403 Printer Operation

The print buffer is an 11-plane, 132-position core storage unit. On print operations, characters are read into the buffer in BCD form. The information is scanned out of the buffer at the speed and in the order required by the printer. Seven planes (CBA 8421) are used for storing characters to be printed, and the remaining planes are used for print error detection.

PRINTER STATUS BITS

Not Ready: The not ready condition results from: the printer being out of forms, printer off-line, printer power off, or pressing the printer stop key.

Forms Busy: Indicates that the forms character register has received a command and has not completed execution of that command.

Check: This bit is not used by the printer.

Busy: This status bit indicates that the printer is printing a line.

Condition: The condition status indicates one or more of the following: parity error was detected during a print scan, a print hammer failed to fire, or the printer timing circuit was out of synchronization with the print chain.

No Transfer: This status is not used by the printer.

IBM 1009 Data Transmission Unit

The 7040/7044 system, when equipped with a 1009 Data Transmission Unit, functions as a data processor and as a data transmitter or data receiver. Thus, the 1009 allows not only two-way communication between two remote computer systems (7040/7044), but also between 7040/7044 system and an IBM 7701 or 7702 Magnetic Tape Terminal, a 1013 Card Transmission Terminal, or another IBM system (1400-7000 series) equipped with a 1009. Data rates of 75, 150, 250, and 300 characters per second are used. One 1009 data transmission unit, using two of the possible six input-output buffers, may be attached to the 1414.

The two buffers in the 1414 synchronizer that are assigned to the 1009 are used for both input and output operation. These buffers should be regarded as a single 160 character buffer. It should be recognized that four characters will be lost every 14 transmitted words due to the 80 characters buffer length ($6 \times 14 = 84$). This must be taken into consideration when setting up a programmed message.

The maximum number of characters that can be transmitted per write select operation is 80 characters (14 words) and should not be exceeded. To terminate an output operation, the portion of the message from the last write select must contain the end of message indication (##) following the last data character. These indications enter the 1414 but are not transmitted.

IBM 1009 Input Status Indications 1414-4

B	Not Ready	1009 not on line, or power off.
8	Check	Parity error detected during the process of filling the buffer.
4	Busy	Buffer is being filled.
2	Condition	CPU did not empty buffer in time and a message has been lost.
1	No Transfer	End of message, or no message in the buffer.

IBM 1009 Output Status Indications 1414-4

B	Not Ready	1009 not on line, or power off.
4	Busy	Both buffers have data, one is emptying.
2	Condition	Last message sent had an error; transmitted to local 1009 but not successfully transmitted to remote 1009.
1	No Transfer	End of message.

IBM 1011 Paper Tape Reader

The IBM 1011 Paper Tape Reader is an input device controlled by the 7040/7044 in the same manner as other telecommunications devices attached through the 1414. Although not itself a telecommunications device, the IBM 1011 is included here because of the way it is attached to the 7040/7044 and because the paper tape processed through it commonly contains data received off lines from telegraph facilities. In this discussion, only five-level Baudot telegraph-code paper tape is considered. With it, the 1011 is an indirect link between the 7040/7044 and a communications network.

The reader operates at 500 paper-tape characters per second, using the telegraph (five-level) tape or eight-track IBM tape.

The 1011 Paper Tape Reader adapter in the 1414 controls one of the six communications buffers and serves one paper tape reader. One 1011 attachment for each 1414 is standard. The 1011 reads telegraph paper tape and, by control panel wiring, recodes characters into BCD code. The recoded characters feed serially into the assigned buffer of the 1414.

Once started, paper-tape reading continues until the synchronizer buffer becomes completely filled or until the end of a paper-tape record is reached, whichever occurs first. (In the latter case, unused buffer positions are filled with BCD blanks.) The General Information Manual, *IBM 1011 Paper Tape Reader,* Form D24-1044, describes the operator's panels, control panel, and other characteristics of the 1011.

IBM 1011 Input Status Indications 1414-4

B	Not Ready	1011 out of tape or power off.
8	Check	Parity error encountered while buffer was being loaded.
4	Busy	Buffer is being filled.
2	Condition	Not used.
1	No Transfer	Not used.

No output operation with 1011.

IBM 1014 Remote Inquiry Unit

From locations up to eight wire-miles from the 7040/7044, the IBM 1014 Remote Inquiry Unit, with typewriter input and output, may be used for system interrogation. It provides a means of rapid access to the contents of 7040/7044 core storage and all intermediate tape and disk storage in the system. It also provides a means of enabling an inquirer to request services to be rendered by the processing center or to influence or control operations executed by the entire system. The 1014 produces a printed output under 7040/7044 program control.

The 1014 has a maximum data rate of 12½ characters per second for inquiry requests, and a maximum of 15½ characters per second for inquiry reply. (NOTE: No time demand is made on the 7106 or 7107 Processing Unit during transfer of a message over a line.) The 1014 permits, on input, as many as 78 data characters plus a concluding group mark or, on output, as many as 79 characters (without a group mark). The first character placed in the 1414 input buffer contains the address of the particular inquiry unit involved (0 through 9); if the message contains fewer than 78 data characters, the position following the last data character in the input buffer contains a group mark entered automatically by the 1014 when the operator presses inquiry release. In this case, any remaining unused positions are filled with BCD blanks by the 1414.

NOTE: Units are addressed 1 through 9. Unit addressed with a zero, select unit number 10.

The 1414 may be equipped with one or two adapters for attachment of 1014 units. Each adapter uses two of the six communications buffers, one for input and one for output. From one to ten 1014 units are controlled by each adapter, but only one unit is operative at a time. The 1014 units may be cable-connected to the 1414 to a distance of fifty feet, or they can be connected by a user-provided or common-carrier wire facility consisting of two pairs of wires, permitting distances of 8 wire-miles to each remote unit. (A wire mile is a distance of one mile physically spanned by a line connecting a 1014 to a 1414. The line may actually consist of a parallel set of four wires or two pairs of wires. In either case, there must be a separate cable or line from each 1014 to an adapter.)

The sequence of operations for an IBM 1014 Remote Inquiry unit is:

1. An operator at a remote unit presses an inquiry-request key, signaling a desire to enter a request.
2. When the proceed light comes on, the operator types an inquiry request (78 characters or less) and presses the inquiry-release key. (When the proceed light comes on, the request light goes off, and the keyboard unlocks. Pressing the release key generates the terminating group-mark character and locks the keyboard.) If the operator lightly flicks a key, the keyboard may either lock completely or lock except for the key that has just been flicked. If such a keyboard lock occurs, the operator should first try to depress the key that was too lightly touched. If that does not un-

lock the keyboard, or if the check light is on, the operator must press cancel followed by inquiry-request and then re-enter the message. For format flexibility, the operator should use the inquiry release (carrier-return) key to start a new line, rather than using the right-hand margin stop to return the carrier.

3. The 1414 receives the message into the 1014 input buffer. When the buffer is full, the 7040/7044 program can read the message.

4. A 7040/7044 stored-program routine processes the inquiry message and places a reply message in the 1014 output buffer. The 1414 transmits the reply message when the addressed station is free.

5. A printed reply is obtained at the inquiry unit that was addressed.

Acceptance of inquiry request by the IBM 7040/7044, when more than one 1014 is attached to the same adapter in the 1414, is under control of an automatic sequencing device in the adapter. This device is part of a controlling circuitry of each 1014 adapter. The device continuously polls the inquiry units under its control, in a fixed sequence, for inquiry request. Transmission of an output message to any unit takes priority over the transmission of polling signals to solicit incoming messages. (On a 7040/7044 system using two 1014 adapters in the 1414, a reply message may be printing at an inquiry station controlled by one adapter while a request message is being sent to the 1414 from an inquiry station controlled by the other adapter.)

The inquiry unit consists of an input-output printer, with a control section located on the printer keyboard, and an indicator light panel – all mounted on a stand. The stand is designed for convenient handling of the forms. Pages or forms can be placed in the cabinet. The printer has an 8.5-inch writing line platen and a 9.375-inch feed platen.

The paper release permits an original and five copies to be adjusted easily. The printer has multiple copy control. An index selection lever permits either three or six lines per inch. The input-output printer is at normal typing height and is equipped with a 44-character keyboard (26 alphabetic, 10 numeric, and 8 special characters: & . - $ * , # / . All other special characters received from the 7040/7044 are printed as a pound sign (#). The control section contains the switch and keys needed to operate the unit.

Switch: The on-off switch furnishes power to the inquiry unit.

Inquiry Request Key: Signals inquiry unit adapter, located in the 1414, that a 1014 unit wants to have a message processed.

Inquiry Release Key: Operating this key:

1. Signals the 1014 adapter in the 1414 that the sending of the inquiry request message is completed. The adapter acknowledges message completion by turning off the inquiry unit proceed light and initiating a printer carrier-return operation.

2. Generates a group mark that is placed in the 1414 buffer following the last data character of the inquiry request.

3. A BFR full attention trap will be generated in the 1414 when the inquiry release key is operated on the 1014.

Inq Can Key: Operating the inquiry cancel key during an inquiry request operation prints an asterisk, releases the inquiry unit, and ends the processing of this inquiry request in the 1414. The 1014 adapter in the 1414 acknowledges the inquiry routine cancellation by turning off the inquiry unit proceed light and initiating a printer carrier-return. It also erases its input buffer. The key is also used to turn off the inquiry-unit check light or the exceed-speed light, or both, and to unlock the keyboard for normal use. The indicator light panel (located to the right of the printer) contains the lights needed by the operator to operate the unit properly.

Request Light: This white light comes on after depression of the inquiry request key. As soon as the 1414, in polling, returns a signal that it is ready to receive an inquiry, this light goes off and the proceed light comes on.

Proceed Light: This green light turns on when the 1014 input buffer in the 1414 is free to accept the inquiry request message. The light turns off when either the release or the cancel key is depressed.

Check Light: This red light indicates detection of a parity error in the inquiry unit during an inquiry request or inquiry reply operation. It also comes on if the release key is pressed before the operator has typed at least one legitimate character, or if the last position of the message is a space or tab character. It is then necessary to press the cancel key and restart the request procedure.

Exceed Speed Light: This red light comes on when the operator types faster than the maximum speed allowable (12.5 characters per second) or presses the space bar and the character key simultaneously. The keyboard locks as this light comes on. It is then necessary to press the cancel key and restart the request procedure.

Forms Light: This red light turns on when the inquiry unit is out of forms; however, several more lines can be printed before the forms clear the platen. Inserting more forms turns the light off.

In addition to manual cancellation of a message by use of the inquiry cancel key, an automatic timing feature in the 1014 terminates the inquiry request operation if thirty seconds elapse between the lighting of the proceed light and the first key stroke. The inquiry request must be re-initiated by pressing the inquiry request key. Whenever a cancellation occurs for

any reason, the 1414 synchronizer is freed to service other remote units, and the contents of the input buffer are erased. As soon as the message is completed correctly, the operator presses the release key to signal the 1414 that the message transmission is complete and to perform other operations described under "Inquiry Release Key."

Output messages can contain up to 79 data characters. The program must insert the number of the 1014 unit (0-9) in the first-character position and the group mark following the data if fewer than 79 data characters are used. The unit number is not printed at the remote unit. The group mark or the 79th character terminates the message and causes a printer carrier-return at the remote unit. Before the 7040/7044 program leaves its service-request processing for any 1014 message, it checks the success of the data transfer to the 1414 synchronizer. If the transfer was successful, the 7040/7044 starts performing other programmed operations. Data transmission from the 1414 to the remote inquiry unit takes place independently of the CPU. If a parity error is detected during the transfer occurring between the 1414 and the inquiry unit, the check light turns on at the inquiry unit. Pressing the cancel key, during or after the reply message transmission is completed, turns off the light. The parity error is visually indicated in the inquiry reply message as follows: An automatic backspace occurs, and the character in error has a # symbol printed over it. If such an error occurs, the operator decides whether to reenter the request (to receive a corrected reply). If a second reply contains an error, he should notify the customer engineer.

IBM 1014 Input Status Indicators 1414-4

B	Not Ready	1014 not on line or buffer power off.
8	Check	Error detected in process of filling the buffer.
4	Busy	Not used.
2	Condition	Not used.
1	No Transfer	No message in the buffer or buffer is in the process of being filled.

IBM 1014 Output Status Indicators 1414-4

B	Not Ready	1014 not on line or buffer power off.
4	Busy	Buffer is being emptied.
2	Condition	Error detected in process of sending previous message.
1	No Transfer	Previous message was not transmitted. Station addressed is inoperative.

TELEGRAPH INPUT-OUTPUT

Common carrier equipment may also be attached to the 1414 to serve as local input-output devices. The data transmission rate depends on the transmission rate of the common carrier equipment used. The maximum rate is approximately ten characters per second. In receive operation, the telegraph units communicate with the 1414 by means of a 5-bit telegraph code. The 1414 translates this into two parts: the administrative portion (destination, sending station, date, time, and so on) and the data portion (body of the message). The data portion to be stored in the 7040-7044 must be enclosed in parenthesis. The letters-shift, figures-shift, line feed, and blank characters are automatically deleted by the 1414 from the incoming message before the data goes to the buffer, and these characters do not enter the buffer. Optionally the carriage return and parenthesis may be deleted.

In transmit operation, reverse procedure is followed. Letters-shift and figures-shift are the only automatically inserted characters. The output message is brought from core storage to the buffer, translated into telegraph code, and sent to the selected telegraph unit when the line is ready to receive it.

The possibility of other priority sequenced operations makes it impossible to insure that subsequent buffer loads of input characters will receive computer attention within the 100 milliseconds (time between telegraph characters) allotted for servicing the buffer after it is filled. Therefore, it is strongly recommended that data portions to be stored be limited to 80 characters. Input messages then will overrun only if they encounter a buffer not transferred since a previous input message (administrative traffic can continue without regard to the status of the input buffer).

TELEGRAPH INPUT STATUS INDICATORS — 1414-4

B	Not Ready	Buffer not on line, or buffer power off.
8	Check	Parity error detected during the process of filling the buffer, or part of a message has been lost.
4	Busy	Buffer is in process of being filled.
2	Condition	CPU did not empty buffer in time and one or more messages have been lost.
1	No Transfer	There is no message in the buffer.

TELEGRAPH OUTPUT STATUS INDICATORS — 1414-4

B	Not Ready	Buffer not on line, or buffer power off.
4	Busy	Buffer is in the process of being emptied.
2	Condition	An error was detected during the transmission of the previous message.
1	No Transfer	Previous message was transmitted but received incorrectly or not at all because of invalid format line failure, or excessive delay in getting characters to the output line.

IBM 1414-6 Input-Output Synchronizer

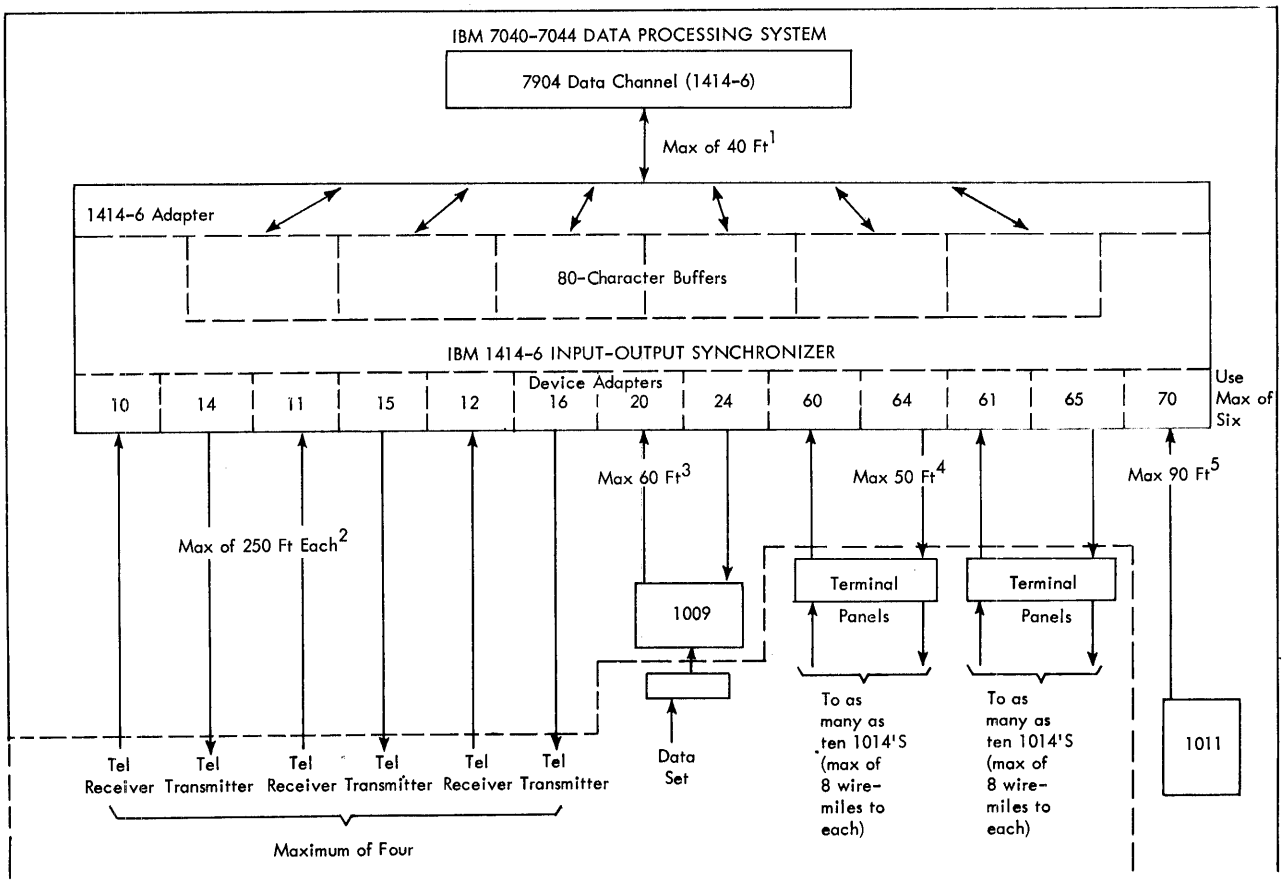
The 1414-6 attaches only the communication devices discussed under the 1414-4 synchronizer. The 1414-6 is

attached to the system through a 7904 Data Channel; as many as four 1414-6 units may be attached to the system. Six 80-character buffers are used, each assigned (through an adapter) to a specific input-output device or group of shared devices. These buffers can be addressed one at a time but operate simultaneously. Figure 10 shows the possible devices, data rates, and proximities for each type of device.

The 1414-6 is connected through the 7904 channel to the core storage part of the 7106 or 7107 processing unit and attaches to the input-output control adapter of the 7904 Data Channel. The functions performed by the 1414-6 result from execution of orders sent to the 1414 when any of four types of input-output instructions – read, write, control, and sense – are executed. The control instruction prepares the 1414-6 to receive orders in the form of data. The 1414-6 interprets these orders as select addresses and selects the desired device. The sense instruction prepares the 1414-6 to send status data and identification of the device whose address is in the address register when the next reset and load channel instruction is executed by the processing unit.

Addressing of Input-Output Devices

Each device adapter in the 1414-6 is assigned a two-digit address to identify it to the program. The first digit identifies the type of adapter; the second digit is the address of the adapter. The address also indicates whether it is an input or output (read or write) operation. Figure 11 shows possible input-output adapters, assigned addresses, and the number of buffers required for attachment. Any combination of adapters shown may be attached to the 1414, if the combined buffer requirements do not exceed six buffers.



Notes
1. Data Transfer Rate -- 11 Microseconds/Character
2. Maximum Data Transfer Rate -- Up to 10 Characters/Second
3. Possible Data Transfer Rates -- 75, 150, 250, 300 Characters/Second
4. Maximum Data Transfer Rates -- 12-1/2 Characters/Second (Inquiry Request)
   15-1/2 Characters/Second (Inquiry Reply)
5. Data Transfer Rate -- 500 Characters/Second

Figure 10. IBM 1414-6 Input-Output Synchronizer

Search then resumes as soon as the channel operation terminates; the attention, which was not responded to by a sense instruction, is then sent from the 1414-6. Since this search takes a variable amount of time (up to about 100 microseconds), the 7040/7044 program should delay 100 microseconds before executing the sense instruction in response to the attention (which was initiated before the control), allowing the address to be re-established. An earlier sense would result in a program check and would introduce additional delay in handling the operation.

The search stops: (1) when the 1414-6 sends an attention, (2) when the 7040/7044 executes control-and-sense instruction, control-and-read instruction, or control-and-write instruction, or (3) when an operation terminates with unusual end. The address is preserved following unusual end until the conditions leading to unusual end are sensed. As in the case of attention, a control takes precedence over an unusual-end signal from the 1414-6, but issuing a control instruction destroys the sense information.

The search resumes with the end of sense or the normal end of read or write. Any address displayed at the issuance of a control is nullified and the new address is set up. Only one attention is sent to the channel for each filled input buffer and one for each output buffer after it has gone empty. An exception exists where the attention-sense sequence is interrupted by a control operation. This attention will be reinitiated following the completion of the control-and-read or control-and-write sequence. A channel reset causes any outstanding full input buffers to be readdressed and attentions re-issued.

A nonstop search through the entire cycle of addresses takes about 112 microseconds, regardless of how many input-output devices are attached to the 1414-6.

A sense operation cannot result in unusual end, but an improper sense causes program check information to go back to the program during the execution of the instruction, i.e., if bit 4 of byte 1 (summary byte) and bit A of byte 2 (detail byte) appear in the status word. The two address bytes convey random numbers and the not-ready bit (bit A in byte 1) is usually on.

A power-off condition in the 1414 can force an attention or unusual-end signal, or both, in the channel to which it is attached.

Random manipulation of I-O devices can cause interrupts as attentions are forced by the filling of input buffers.

In debugging operations, if the customer engineer sets the off-line switch to off-line and the mode selector switch to interface, both of the above types of interrupts will not occur.

Programming for the IBM 1011 from the IBM 7040/7044 System

READ-PAPER-TAPE INSTRUCTIONS

CTR with 7904 data channel address.

RCH (B-E) with a Y portion referring to the IORD and a word count and the initial storage address of the control information (70, the address of the 1011 adapter) to be transmitted to the 1414-6.

PRD with channel and adapter addresses. The 1414-6 compares this instruction with the CTR for consistency and gives an unusual end (with a program check) if they are not consistent.

RCH to actually move data from the 1414-6 buffer to core storage.

DESCRIPTION

These instructions cause three events:

1. The contents of the paper-tape-reader buffer in the 1414 are transferred to 7040/7044 core storage in a block of 80 characters, occupying 13 full words and two high-order characters in a 14th word.
2. The 7040/7044 immediately proceeds to execute the next instruction of its stored program.
3. The reader receives a signal to resume reading data from paper tape into the now empty buffer in the 1414.

A maximum of 80 characters can be read from the tape by one read instruction. Records longer than 80 characters require more than one read instruction. When a tape record contains less than 80 characters, an EOR (end of record) character punched into tape causes the reader to stop. The remaining positions of the 80-character buffer transfer to the 7040/7044 as BCD blanks.

Any paper-tape character can be assigned as an end-of-record character by control-panel wiring at the paper tape reader. The end-of-record character, once assigned, must not be used as a data character on tape because it always causes an end-of-record signal. The paper-tape code assigned this function is wired from the appropriate decode exit hub to the EOR IN hub. The EOR OUT hub is wired to ENCODE ENTRY at the desired BCD character hub for translating. The BCD character chosen for the EOR function is chosen by the programmer to conform to the usual practice for the individual application.

SUGGESTED PROGRAM SEQUENCE

1. Define a receive area for 14 words.
2. Enable an attention trap from the 1414-6.
3. Upon getting an attention, TCO (B-E) to itself to make sure the channel is not in use.
4. AXT, followed by TIX to itself to produce a 100-microsecond delay.

5. Issue a sense instruction to verify that the 1011 adapter caused the attention.

6. If it did, issue the sequence of read-paper-tape instructions listed above.

7. Since the paper tape reader reads at 500 characters per second, it requires 160 milliseconds to fill the buffer. Any attention from the 1414-6 occurring before this 160-millisecond period can be assumed to come from another device adapter. As paper-tape input is not real-time and, therefore, is in no danger of being lost, program the paper tape reader to receive low attention priority.

Programming for the IBM 1014 Input to the IBM 7040/7044 System

READ INQUIRY INSTRUCTIONS

CTR with 7904 data channel address.

RCH (B-E) with a Y portion referring to the IORD, word count, and initial storage address of the control information (60 or 61, the addresses of the two possible 1014 input adapters) to be transmitted to the 1414-6.

PRD with channel and adapter addresses. The 1414-6 compares this instruction with the CTR for consistency and gives an unusual end (with a program check) if they are not consistent.

RCH to actually move data from the 1414-6 buffer to core storage.

DESCRIPTION

These instructions read from a 1014 input buffer (in the input-output synchronizer) that is designated by the IORD.

If the operator at a remote inquiry unit enters fewer than 78 characters, the 80 characters read into storage consist of:

Unit Identification Character (0-9), generated automatically by the 1014.

Operator's Message.

Group Mark, entered automatically by the 1014 into the next position after the last character of the operator's message. This group mark entry takes place when the operator presses the release key.

Enough BCD Blanks to fill the 80 positions of the buffer (entered automatically by the synchronizer when the message comes into its buffer).

If the operator at a remote inquiry unit enters exactly 78 characters, the 80 characters are the same as shown above, but without any blanks.

If the operator enters 79 characters, the message is in error, the proceed light goes off, and the keyboard locks. The buffer-load is read to the 7040/7044. However, the data check indicator comes on, indicating an erroneous message.

For flexibility in controlling the input format, the operator should use the inquiry-request key to cause a carrier-return and line feed, rather than using the right margin stop to perform these functions. The total number of characters in all lines should not exceed 78.

SUGGESTED PROGRAM SEQUENCE

Substituting the read-inquiry instruction and the input buffers for the 1014, use the same suggested programming sequence as for reading paper tape for Steps 1 through 6.

7. Since 1014 input is being keyed by an operator, the time at which the 1414 buffer for this input will be filled is unpredictable.

Programming for Output to the IBM 1014 from the IBM 7040/7044 System

WRITE-INQUIRY-RESPONSE (1014) INSTRUCTIONS

CTR with 7904 data channel address.

RCH (B-E) with a Y portion referring to the IORD, word count, and initial storage address of the control information (64 or 65, the addresses of the 1014 output adapters) to be transmitted to the 1414-6.

PWR with channel and adapter address. The 1414-6 compares this instruction with CTR for consistency and gives an unusual end (with a program check) if they are not consistent.

RCH to actually move data from core storage to the 1414-6 buffer.

DESCRIPTION

These instructions write 80 characters to the 1014 output buffer specified by the adapter address. An inquiry response cannot exceed one buffer load. The first character position must contain the station number to be addressed. (This character will not be printed at the station.) A group mark as the last character of the message terminates the reply print-out at the station and initiates a line feed and printer carrier-return. If the group mark is not inserted by the 7040/7044 program, the reply automatically stops after the 80th character (including the unprinted first-character station identifier) and causes a line feed and carrier-return.

The main program waits until transfer of 80 characters to the 1414 buffer has been made successfully and the remote station has been found operative. The program then continues while the buffer contents are being sent to the receiving station. If an error occurs during this transmission, the check light at the remote station turns on and the printer automatically backspaces once and prints a # over the character in question. The operator may then push the cancel key and enter a repeat request. To give the 7040/7044 program

PRD with channel and adapter addresses. The 1414-6 compares this instruction with the CTR for consistency and gives an unusual end (with a program check) if they are not consistent.

RCH to actually move data from the 1414-6 buffer to core storage.

DESCRIPTION

These instructions read from a 1014 input buffer (in the input-output synchronizer) that is designated by the IORD.

If the operator at a remote inquiry unit enters fewer than 78 characters, the 80 characters read into storage consist of:

Unit Identification Character (0-9), generated automatically by the 1014.

Operator's Message.

Group Mark, entered automatically by the 1014 into the next position after the last character of the operator's message. This group mark entry takes place when the operator presses the release key.

Enough BCD Blanks to fill the 80 positions of the buffer (entered automatically by the synchronizer when the message comes into its buffer).

If the operator at a remote inquiry unit enters exactly 78 characters, the 80 characters are the same as shown above, but without any blanks.

If the operator enters 79 characters, the message is in error, the proceed light goes off, and the keyboard locks. The buffer-load is read to the 7040/7044. However, the data check indicator comes on, indicating an erroneous message.

For flexibility in controlling the input format, the operator should use the inquiry-request key to cause a carrier-return and line feed, rather than using the right margin stop to perform these functions. The total number of characters in all lines should not exceed 78.

SUGGESTED PROGRAM SEQUENCE

Substituting the read-inquiry instruction and the input buffers for the 1014, use the same suggested programming sequence as for reading paper tape for Steps 1 through 6.

7. Since 1014 input is being keyed by an operator, the time at which the 1414 buffer for this input will be filled is unpredictable.

Programming for Output to the IBM 1014 from the IBM 7040/7044 System

WRITE-INQUIRY-RESPONSE (1014) INSTRUCTIONS

CTR with 7904 data channel address.

RCH (B-E) with a Y portion referring to the IORD, word count, and initial storage address of the control information (64 or 65, the addresses of the 1014 output adapters) to be transmitted to the 1414-6.

PWR with channel and adapter address. The 1414-6 compares this instruction with CTR for consistency and gives an unusual end (with a program check) if they are not consistent.

RCH to actually move data from core storage to the 1414-6 buffer.

DESCRIPTION

These instructions write 80 characters to the 1014 output buffer specified by the adapter address. An inquiry response cannot exceed one buffer load. The first character position must contain the station number to be addressed. (This character will not be printed at the station.) A group mark as the last character of the message terminates the reply print-out at the station and initiates a line feed and printer carrier-return. If the group mark is not inserted by the 7040/7044 program, the reply automatically stops after the 80th character (including the unprinted first-character station identifier) and causes a line feed and carrier-return.

The main program waits until transfer of 80 characters to the 1414 buffer has been made successfully and the remote station has been found operative. The program then continues while the buffer contents are being sent to the receiving station. If an error occurs during this transmission, the check light at the remote station turns on and the printer automatically backspaces once and prints a # over the character in question. The operator may then push the cancel key and enter a repeat request. To give the 7040/7044 program forms control, the following characters perform the designated function:

CHARACTER	7040/7044 CORE STORAGE CHARACTER (Octal)	(BCD Code) C B A 8 4 2 1	FUNCTION
Record Mark (≠)	72	0 0 1 1 0 1 0	Tab
Lozenge (⌑)	34	1 1 1 1 1 0 0	Carrier-return*
Blank	60	1 0 0 0 0 0 0	Space
Group Mark (≢)	37	0 1 1 1 1 1 1	EOR, Carrier Return

*Programmed carrier-return, rather than the right margin stop at the printer, should determine the right end of each line.

SUGGESTED PROGRAM SEQUENCE

1. Define an output area for 14 words. Place the identifying character (0-9) of the remote unit in the leftmost position of the area. Avoid placing group marks within the messages because they will terminate the print-out at the remote unit. Any character to the right of the first group mark and to the left of the 81st character will be transferred to the buffer in the 1414, but will not be printed out at the remote unit. Limit the output message to 80 characters (including the identifying number of the remote unit). If the message consists of fewer than 80 characters, place a group

mark in the next position to the right of the last data character of the message.

2. (This step is unnecessary for a single message or for the first message of a series being sent consecutively to one 1014 terminal. In this description, message is synonymous with line of printed data.) For the second and all subsequent messages to be transmitted as a complete inquiry response, enable an attention trap from the 1414-6 and, upon getting an attention signal, continue with the next step.

4. TCO (B-E) to itself to make sure the channel is not in use.

5. AXT, followed by TIX to itself to produce a 100-microsecond delay.

6. Issue a sense instruction to verify that the desired 1014 output adapter caused the attention.

7. If it did, issue the above write-inquiry-response instructions.

8. The emptying of the 1414-6 buffer causes an attention signal at its completion. This causes an attention trap for the channel to which the 1414-6 is attached. Therefore, an enable trap instruction is necessary following the write-inquiry-response instructions. When a trap occurs, the contents of the instruction counter are stored, and the next instruction is taken from a fixed location as follows:

CHANNELS	STORE THE IC AT:	NEXT INSTRUCTION FROM:
B	0014	0015
C	0016	0017
D	0020	0021
E	0022	0023

The first instruction after execution of a trap should be an unconditional transfer located at the odd locations 15-23. The trap is controlled by the enable and restore-channel-trap instructions.

9. Following an attention signal, use the 100-microsecond delay routine and then issue a sense instruction to determine the success of the last message transmitted to the 1014.

Sense Data — 1414-6

To determine what condition caused a trap, the program must selectively examine the conditions pertaining to each buffer. This is done by giving a sense instruction addressed to the buffer in question. When an RCH is executed, the sense lines are sampled and the six high-order bit positions of the channel assembly register receive the contents of these sense lines. The sense data are then stored in core storage at the address specified by the IORD command. Sense data available to the CPU and core storage are shown in Figure 12A. Note that byte 1 contains summary status information, byte 2 contains detail information, and bytes 3 and 4 contain the device adapter address to identify the status information. The bits in byte 2 have different meanings, depending upon which bit, or combination of bits, is on in byte 1 and which device the sense information applies to.

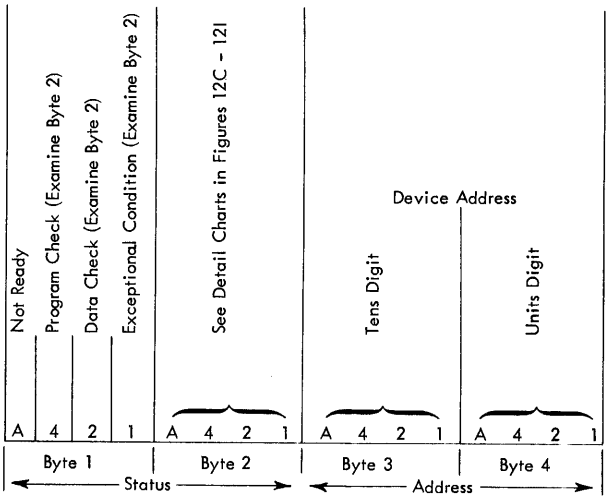


Figure 12A. Status Bytes – 1414-6

Figure 12B gives general interpretations and directions for analyzing the individual bytes of sense information. Figures 12C through 12I give a detailed interpretation of each bit in byte 2, related to the bit, (or bits) that are on in bytes 1, 3, and 4.

Figure 13 summarizes IBM 1414 Input-Output Synchronizer models, equipment attached to the 1414's and data channels having 1414 units.

IBM 1401 Data Processing System

Any IBM 1401 Data Processing System and its input-output devices may be connected to data channel A by using the 1401 special feature Serial Input-Output Adapter (SF 7080). Except for input-output instructions, computer instructions of both systems operate normally.

To start an input-output operation, the 7040 or 7044 must be synchronized with the 1401 program. Synchronization is possible when the 1401 program is in a mode that enables it to respond to a 7040/7044 instruction. The 1401 informs the 7040/7044 that it is in this mode by executing the KE instruction. This instruction sets an indicator (1401 in loop) in channel A. When the 7040/7044 executes a TDOA instruction for the 1401, the indicator status determines if the program transfers (if the indicator is off, the program transfers).

When any select instruction (RDS, WRS, CTR, BSR, WEF, REW, RUN) is directed to the 1401, that instruction causes the CPU to hang up if the in-loop indicator is off. If the indicator is on, the select instruction turns it off and sends a signal to the 1401. The 1401 program can sense this signal by executing the instruction B(AAA)2. If the signal is present, the 1401 branches to location (AAA); if the signal is not present, the 1401 executes its next sequential instruction. A basic synchronization loop in the 1401 program could be:

LOCATION	INSTRUCTION
X	KE
X +2	B(AAA)2
X +7	B(X)

When the instruction at X + 2 branches, the 1401 program should proceed to a routine that selects its serial I-O adapter to read six bytes. When the serial I-O adapter is selected, the 7040/7044 transfers its entire select instruction (without change) to the 1401. The 1401 decodes this instruction to determine the operation and unit involved. If the unit is tape, reader,

BCD Char Bits						BCD Byte No.	Interpretation
B	A	8	4	2	1	0	
	0		0	0	0		Normal Operation
	0		1	0	0		Program Check. See bytes 3 and 4 for address; then interpret byte 2 for detailed cause.
	0		0	1	0		Data Check. See bytes 3 and 4; then interpret byte 2.
	0		0	0	1		Presence of External Exceptional Condition. See bytes 3 and 4; then interpret byte 2.
	1		0	0	0		Not Ready Condition of the Device or Buffer Off Line. See bytes 3 and 4.
	1		0	0	1		Combination of Not Ready and External Exceptional Condition. See bytes 3 and 4 and correct the not-ready condition.
	1		0	1	0		Combination of Not Ready and Data Check. See bytes 3 and 4 and correct the not-ready condition.
	1		1	0	0		Combination of Not Ready and Program Check. See bytes 3 and 4 and correct the not-ready condition.
	A		4	2	1	1	
	0		0	0	0		Normal Condition
	1		0	0	0		See bytes 3 and 4 for address; then consult interpretation charts in Figures 12C through 12I.
	0		1	0	0		
	0		0	1	0		
	0		0	0	1		
	0		0	1	1		Possible Combination of Error or Overrun and End of Message (1009). See bytes 3 and 4 and interpretation in Figures 12C and 12D.
Not Used	A	Not Used	4	2	1	2	
	0		0	0	1		Address Tens Digit is 1 (telegraph).
	0		0	1	0		Address Tens Digit is 2 (IBM 1009).
	0		1	1	0		Address Tens Digit is 6 (IBM 1014).
	0		1	1	1		Address Tens Digit is 7 (IBM 1011).
	A		4	2	1	3	
	0		0	0	0		Address Units Digit is 0 (read).
	0		0	0	1		Address Units Digit is 1 (read).
	0		0	1	0		Address Units Digit is 2 (read).
	0		1	0	0		Address Units Digit is 4 (write).
	0		1	0	1		Address Units Digit is 5 (write).
	0		1	1	0		Address Units Digit is 6 (write).

Figure 12B. Interpretation of Sense Bits in Characters 1-4 of the Sense Field – 1414-6

SUMMARY (Byte 1)		DETAIL (Byte 2)			
		Bit A	Bit 4	Bit 2	Bit 1
Bit A	NOT READY (1009 power off or buffer off line). No data transfer.				
Bit 4	PROGRAM CHECK	Sense without prior attention, control, or unusual end. **	Read command following command to write.	Write command following control to read.	Read or write command without prior control command.
Bit 2	DATA CHECK			Parity check of the two-byte address sent to the 1414-6.	Parity check or 1414 machine check on data transfer to or from the processor.
Bit 1	EXCEPTIONAL CONDITIONS		Buffer being filled.	Buffer overrun or transmission error between buffer and remote 1009. *	End of message. *

Figure 12C. Interpretation of Sense Bytes 1 and 2 if Bytes 3 and 4 Represent IBM 1009 READ (Address 20) — 1414-6

SUMMARY (Byte 1)		DETAIL (Byte 2)			
		Bit A	Bit 4	Bit 2	Bit 1
Bit A	NOT READY (1009 power off, buffer not on line). No data transfer.				
Bit 4	PROGRAM CHECK	Sense without prior attention, control, or unusual end. **	Read command following control to write.	Write command following control to read.	Read or write command without prior control command.
Bit 2	DATA CHECK			Parity check of the two-byte address sent to the 1414-6.	Parity check or 1414 machine check on data transfer to or from the processor.
Bit 1	EXCEPTIONAL CONDITIONS		Buffer is being emptied.	Transmission error between buffer and remote 1009. *	End of message acknowledged. *

Figure 12D. Interpretation of Sense Bytes 1 and 2 if Bytes 3 and 4 Represent IBM 1009 WRITE (Address 24) — 1414-6

NOTES:
1. Detecting a bit in a bit-position of the first byte usually requires investigation of supplementary information provided by bits in the second byte.
2. When byte 1 indicates program check (bit 4) or data check (bit 2), exceptional conditions are suppressed so that bit 1 does not appear. If byte 1 indicates not-ready in combination with program check, data check, or exceptional condition check, correct the not-ready condition first.
3. a. Status bits marked (*) pertain to the acknowledgment of the most recent message to or from a particular device. The 7040/7044 will be alerted by an attention signal.
   b. Status bits marked (**) indicate to the 7040/7044 that the sense command currently being executed was improperly issued.
   c. All other status bits will appear on a sense command following unusual-end.
4. Both bits 1 and 2 may be on simultaneously, meaning that the end-of-message was received, but was in error.

SUMMARY (Byte 1)		DETAIL (Byte 2)			
		Bit A	Bit 4	Bit 2	Bit 1
Bit A	NOT READY (1011 power off or not attached, tape broken or out of tape, buffer off line). No data transfer.				
Bit 4	PROGRAM CHECK	Sense without prior attention, control, or unusual end.**	Read command following control to write.	Write command following control to read.	Read or write command without prior control command.
Bit 2	DATA CHECK			Parity check of the two-byte address sent to the 1414-6.	Parity check or 1414 machine check on data transfer to or from the processor.
Bit 1	EXCEPTIONAL CONDITIONS		Buffer filling.	Parity error in tape when control panel wired to drop the character or substitute another character.* Error between 1011 and buffer.	

Figure 12E. Interpretation of Sense Bytes 1 and 2 if Bytes 3 and 4 Represent IBM 1011 READ (Address 70) – 1414-6

NOTES:
1. Detecting a bit in a bit-position of the first byte usually requires investigation of supplementary information provided by bits in the second byte.
2. When byte 1 indicates program check (bit 4) or data check (bit 2), exceptional conditions are suppressed so that bit 1 does not appear. If byte 1 indicates not-ready in combination with program check, data check, or exceptional condition check, correct the not-ready condition first.
3. a. Status bits marked (*) pertain to the acknowledgment of the most recent message to or from a particular device. The 7040/7044 will be alerted by an attention signal.
   b. Status bits marked (**) indicate to the 7040/7044 that the sense command currently being executed was improperly issued.
   c. All other status bits will appear on a sense command following unusual-end.

SUMMARY (Byte 1)		DETAIL (Byte 2)			
		Bit A	Bit 4	Bit 2	Bit 1
Bit A	NOT READY (Buffer off line). (No data are transferred.)				
Bit 4	PROGRAM CHECK	Sense without prior attention, control, or unusual end. **	Read command following control to write.	Write command following control to read.	Read or write command without prior control command.
Bit 2	DATA CHECK			Parity check of the two-byte address sent to the 1414-6.	Parity check or 1414 machine check on data transfer to or from the processor.
Bit 1	EXCEPTIONAL CONDITIONS		Buffer being filled or no request.	Error during filling of buffer, or message exceeds 78 characters. *	

Figure 12F. Interpretation of Sense Bytes 1 and 2 if Bytes 3 and 4 Represent IBM 1014 READ (Address 60 or 61) – 1414-6

SUMMARY (Byte 1)		DETAIL (Byte 2)			
		Bit A	Bit 4	Bit 2	Bit 1
Bit A	NOT READY * or out of forms *; buffer off line. (No data transferred in last case.)				
Bit 4	PROGRAM CHECK	Sense without prior attention, control, or unusual end. **	Read command following control to write.	Write command following control to read.	Read or write command without prior control command.
Bit 2	DATA CHECK			Parity check of the two-byte address sent to the 1414-6.	Parity check or 1414 machine check on data transfer to or from the processor.
Bit 1	EXCEPTIONAL CONDITIONS		Buffer being emptied.	Transmission error between 1014 and buffer. *	

Figure 12G. Interpretation of Sense Bytes 1 and 2 if Bytes 3 and 4 Represent IBM 1014 WRITE (Address 64 or 65) – 1414-6

NOTES:
1. Detecting a bit in a bit-position of the first byte usually requires investigation of supplementary information provided by bits in the second byte.
2. When byte 1 indicates program check (bit 4) or data check (bit 2), exceptional conditions are suppressed so that bit 1 does not appear. If byte 1 indicates not-ready in combination with program check, data check, or exceptional condition check, correct the not-ready condition first.
3. a. Status bits marked (*) pertain to the acknowledgment of the most recent message to or from a particular device. The 7040/7044 will be alerted by an attention signal.
   b. Status bits marked (**) indicate to the 7040/7044 that the sense command currently being executed was improperly issued.
   c. All other status bits will appear on a sense command following unusual-end.

SUMMARY (Byte 1)		DETAIL (Byte 2)			
		Bit A	Bit 4	Bit 2	Bit 1
Bit A	NOT READY (Local telegraph station is not ready; buffer not on line). No data transfer.				
Bit 4	PROGRAM CHECK	Sense without prior ** attention, control, or unusual end.	Read command following control to write.	Write command following control to read.	Read or write command without prior control command.
Bit 2	DATA CHECK			Parity check of the two-byte address sent to the 1414-6.	Parity check or 1414 machine check on data transfer to or from the processor.
Bit 1	EXCEPTIONAL CONDITIONS		Buffer filling (or no input available).	Buffer overrun. * (Buffer not emptied in time.) Transmission error between buffer and remote station.	

Figure 12H. Interpretation of Sense Bytes 1 and 2 if Bytes 3 and 4 Represent Telegraph READ (Address 10, 11, or 12) – 1414-6

SUMMARY (Byte 1)		DETAIL (Byte 2)			
		Bit A	Bit 4	Bit 2	Bit 1
Bit A	NOT READY (Local telegraph station is not ready; buffer not on line). No data transfer.				
Bit 4	PROGRAM CHECK	Sense without prior ** attention, control, or unusual end.	Read command following control to write.	Write command following control to read.	Read or write command without prior control command.
Bit 2	DATA CHECK			Parity check of the two-byte address sent to the 1414-6.	Parity check or 1414 machine check on data transfer to or from the processor.
Bit 1	EXCEPTIONAL CONDITIONS		Buffer emptying.	Parity or translate * error out to line or transmission error between local and remote stations.	

Figure 12I. Interpretation of Sense Bytes 1 and 2 if Bytes 3 and 4 Represent Telegraph WRITE (Address 14, 15, or 16) – 1414-6

NOTES:
1. Detecting a bit in a bit-position of the first byte usually requires investigation of supplementary information provided by bits in the second byte.
2. When byte 1 indicates program check (bit 4) or data check (bit 2), exceptional conditions are suppressed so that bit 1 does not appear. If byte 1 indicates not-ready in combination with program check, data check, or exceptional condition check, correct the not-ready condition first.
3. a. Status bits marked (*) pertain to the acknowledgment of the most recent message to or from a particular device. The 7040/7044 will be alerted by an attention signal.
   b. Status bits (marked **) indicate to the 7040/7044 that the sense command currently being executed was improperly issued.
   c. All other status bits will appear on a sense command following unusual-end.

1414 Model	729 II	729 IV	729 V	729 VI	7330	Communication Devices	Unit Record	Column Binary	Data Chan A	7904 Data Channel
1	x	x	x (note 1)		x (note 2)				x	x
2					x				x	x
3							x		x	
4						x	x	x	x	
5						x			x	
6						x				x
7	x	x	x	x	x (note 2)				x	x
8							x (note 3)			

Note 1. With 800 cpi feature. Note 2. With intermix feature. Note 3. Printer only.

Figure 13. IBM 1414 Input-Output Synchronizer Characteristics

punch, or printer, the 1401 program sends status data to the 7040/7044. The status data represent conditions encountered while executing the operation; these conditions may be error, end of file, or end of tape.

After transmission of these conditions (or if no conditions exist), the 1401 executes the 1401 instruction KD to signal the 7040/7044 to end operation on its current select instruction. If the I-O operation requires data transfer, the 1401 program should proceed to a routine that selects its I-O adapter to read the record.

Data transfer proceeds when the 7040/7044 executes an RCHA instruction. The data are transferred at 11.5 microseconds per character and cease when the channel A word count goes to zero or upon an end-of-record signal from the 1401. The 1401 end-of-record signal occurs when the 1401 encounters a group-mark word-mark in its storage. When the data transfer is complete, the 1401 should send status data that represents any condition encountered during the data transfer. The end-operation signal (KD) causes the 7040/7044 to end operation on its current RCHA instruction.

When the 1401 program wishes to signal the 7040/7044, a KF may be given that turns on the 1401 attention trap request in the 7040/7044. If channel A attention is enabled, a channel A trap occurs.

When the 7040/7044 wishes to signal the 1401, a status line is turned on. This line may be tested in the 1401 by using the B(AAA)5 instruction. The alternate path of the branch instruction can then be used by the 1401 program to interrupt the 7040/7044 by turning on the 1401 attention indicator. Two different results occur when the 7040/7044 select instructions address the 1401:

1. Execution of a BSR, WBT, WEF, REW, and RUN instruction leaves the channel not-busy after the 1401 ends operation with its KD instruction.

2. Execution of a RDS, PRD, SEN, WRS, PWR, CTR, and instruction leaves the channel in use (busy) after the 1401 ends operation with its KD instruction, thus requiring an RCH instruction to complete the operation.

Two instructions are used to turn the 1401 status line off and on:

SLNA—Status Line On, Channel A

Description: Execution of this instruction turns the 1401 status line on. The line may be tested in the 1401 with a B(AAA) 5 branch instruction. If the line is on, the 1401 program branches. Since the Y part of the SLNA is a part of the operation code, modification by indexing may change the operation.

Indicators: 1401 status line

Timing: 7040 — 1 cycle
7044 — 2 cycles

SLFA—Status Line Off, Channel A

Description: Execution of this instruction turns the 1401 status line off. Since the Y part of the SLFA is part of the operation code, modification by indexing may change the operation.

Indicators: 1401 status line

Timing: 7040 — 1 cycle
7044 — 2 cycles

The following 1401 instructions are used to send various conditions to the 7040/7044 system:

KA	Turn on channel A channel check indicator
KB	Turn on channel A end of file indicator
KC	Turn on channel A end of tape indicator
KD	End of operation (terminates the 7040/7044 select or RCHA instruction and turns the 1401 ready indicator off).
KE	Turn on channel A 1401 ready indicator
KF	Turn on channel A 1401 attention trap request
L%A2BBB R	Select the 7040/7044 and read into 1401 storage starting at location BBB in load mode.
L%A2BBB W	Select the 7040/7044 and write from 1401 storage starting at location BBB in load mode.
M%A2BBB R	Select the 7040/7044 and read into storage starting at location BBB (1401 storage).
M%A2BBB W	Select the 7040/7044 and write from 1401 storage starting at location BBB.
B(AAA)1	Branch to location AAA if the 1401 detected an error during the input/output data transfer.
B(AAA)2	Branch to location AAA if the 7040/7044 is waiting with a select instruction.
B(AAA)5	Branch to location AAA if the 7040/7044 status line is on.

Direct Data Connection

The direct data connection permits connection of non-IBM input-output devices to an IBM 7040 or 7044 Data Processing System through any of the IBM 7904 Data Channels. Transfer of data between such devices and the 7040/7044 is the same as with standard IBM input-output units, with a full word being transferred at a time.

The direct data connection, when installed on the 7040/7044, provides a communication link with analog-digital converters, telegraph or telephone lines, radar, telemeters, microwave links, engine test stands, or display units. The direct data connection consists basically of direct data interrupt, 36 data transfer lines, two parity lines, 20 sense lines, and the necessary control lines. This feature permits real-time or direct transmission of data between core storage, via the 7904, and external devices at data transmission rates up to 62,500 or 166,666 words per second (7040 and 7044, respectively).

A direct data interrupt signal from the input-output device to the computer automatically interrupts normal program execution turns on Trap Inhibit and transfers program control to storage location 00004.

On interruption, the address of the next normal instruction to be executed replaces the address part of location 00003 so that re-entry to the normal program is possible after processing. The direct data interrupt signal is under control of the enable instruction.

Data transfer between any associated IBM channel input-output device and core storage of the 7040/7044 is accomplished over 36 data lines and one parity line. These lines are brought out to connectors that may be cable-connected to the direct data I-O device.

The sense lines, which are under program control, provide a data transfer between any core storage address and the direct data connection. Ten lines are provided for input control and another ten lines are provided for output control. The sense lines may be used for ten-bit data transfer, multiple I-O units control, coding or decoding units selected, or logic functions.

The direct data connection is installed on any IBM 7904 Data Channel and uses the data register of the data channel as its buffer. The IORD command is used with the direct data connection as in standard 7904 operation.

Computer-to-Computer Operation

The direct data connection may be used for high-speed communication between two 7040/7044 systems. Communication between the computers is started by a present sense lines (PSL) instruction from one computer to the other. Execution of the PSL causes a direct data interrupt at the other computer. The routine that services this direct data interrupt executes a store sense lines (SSL) instruction to determine what information the first computer is sending. The second computer may then respond by executing a PSL instruction, which causes a direct data interrupt in the first computer. By use of the sense lines and direct data interrupts in both computers, the two programs are initialized for communication over the 36-bit direct data interface.

One computer must be placed in read status and the other computer in write status. Once each computer has selected its direct data interface and set up controls for starting address and word count, data transfer automatically occurs between the systems on a demand and response basis without further programming intervention. When the word count in either computer is reduced to zero, the other computer receives an end-of-record signal and both channels disconnect. Word parity errors occurring in their computer set the redundancy check indicator in the other computer, allowing both programs to determine transmission accuracy.

General Programming Information

The fastest IBM input-output device available as standard equipment on the 7040/7044 System has a data rate of about one word every 66.66 microseconds. If the external device to be used with the direct data connection has a data rate no faster than these figures, no programming restrictions other than the standard rules are applicable. When data rates from these external devices exceed the fastest IBM data rates, other channel activity must be curtailed. To achieve the maximum data rate of 62,500 or 166,666 words per second (7040 and 7044, respectively), all other data channel operations must be stopped.

To determine the maximum data rate possible with a given computer I-O configuration, include two machine cycles for each channel in use (7040 and 7014) plus one machine cycle for the CPU (7044 only). Multiply the number of cycles by the basic cycle (8.0 for 7040, 2.0 for 7044) to obtain a figure in microseconds. Divide 1,000,000 by this figure to obtain the number of words per second. Allow a safety factor percentage for random fluctuations in computer timings.

IBM 1301/1302 Disk Storage, IBM 7320 Drum Storage and IBM 7631 File Control

The 7631 File Control executes any of four commands (read, write, sense, and control). Read and write commands permit transmission of data between disk/drum storage and the computer through the file control. The sense command causes transmission of status data from the file control to indicate status of the disk/drum system. The control command transmits orders to the file control. Orders are data sent to the file control for decoding and execution of non-data operations.

A detailed description fo the IBM 1301 and 1302 Disk Storage is in the manual *IBM1301, Models 1 and 2, Disk Storage and IBM 1302, Models 1 and 2, Disk Storage with IBM 7040 and 7044 Data Processing Systems,* Form A22-6768.

A detailed description of the IBM 7320 Drum Storage Unit is in the manual, *IBM 7320 Drum Storage with 7040 and 7044 Systems,* Form A22-6793.

Output Typewriter

The output typewriter, on the operator's console, prints all 64 BCD characters at 15 characters per second. Two sets of type are supplied; one to be used for programming language printing and the other for report writing. Information is printed serially by character. A blank character results in a space function, and automatic carriage return is provided at the end of every line and at the end of a record.

Write Operation

A PWR instruction with an interface character 4 selects the typewriter. When the RCHA is given, the channel starts data transfer by sending the first byte. The typewriter recognizes the presence of data and takes a print cycle. When the print cycle is completed, a service request is generated for the next byte. The write operation is completed when word count goes to zero and a carriage return is initiated.

Single Character Operation

To type a single character and not return the carriage, a CTR followed by an RCHA, which loads an IORD command, may be used. Bits S, 1-5 of the addressed data word are placed in the typewriter buffer and the RCHA ends operation. Channel A remains in use until the character is actually printed. An end operation trap then occurs. The next CTR and RCHA must be given within 28 milliseconds of this trap to maintain full typewriter speed. A carriage return does not occur until the end of line is reached.

Shifting

When shifting from lower case to upper case or upper case to lower case, an additional character print time is required. The blank character, interpreted as a space, does not require shifting. The following list shows upper-case characters.

REPORT	PROGRAMMING	REPORT	PROGRAMMING
b	b	@	'
:	:	⫼	⫼
>	>	¤	)
∨	∨	⌐	⌐
<	<	[	[
⫩	⫩	&	+
¯	¯	\	\
*	*	%	(
;	;	]	]
△	△		

Error Checking

The typewriter checks the parity of each character received from the channel. If a parity error is detected, an error signal is sent to the channel and the print cycle is completed. The channel redundancy check indicator is turned on when the error is signaled. If channel A parity is enabled, the channel disconnects and a trap is requested. If channel A is not enabled, operation continues.

Operator's Console

The operator's console has five panels (Figure 14) that contain keys, lights, and switches provided as operator aids. This area provides flexible, efficient communication between the computer and the operator. The description of console features starts with the top left corner of panel 1.

Panel 1

Channel Bit Density: Five density switches are used, one for each possible data channel, to select the magnetic tape densities used for recording. Each switch has three positions: 556/200, 800/200, and 800/556. Thus, a magnetic tape unit whose *channel* bit density switch is in the 800/556 position would record at 800 bits per inch if operating at high density, at 556 bits per inch if operating at low density.

Storage Clock: With this switch in the ON position, core storage location 00005 is incremented (added to) 60 times a second. Incrementing is stopped by placing the switch in the OFF position or by removing power from the system.

Step Mode Selector: This three-position rotary switch controls the operation mode when the single or multiple step keys are depressed. The three positions of

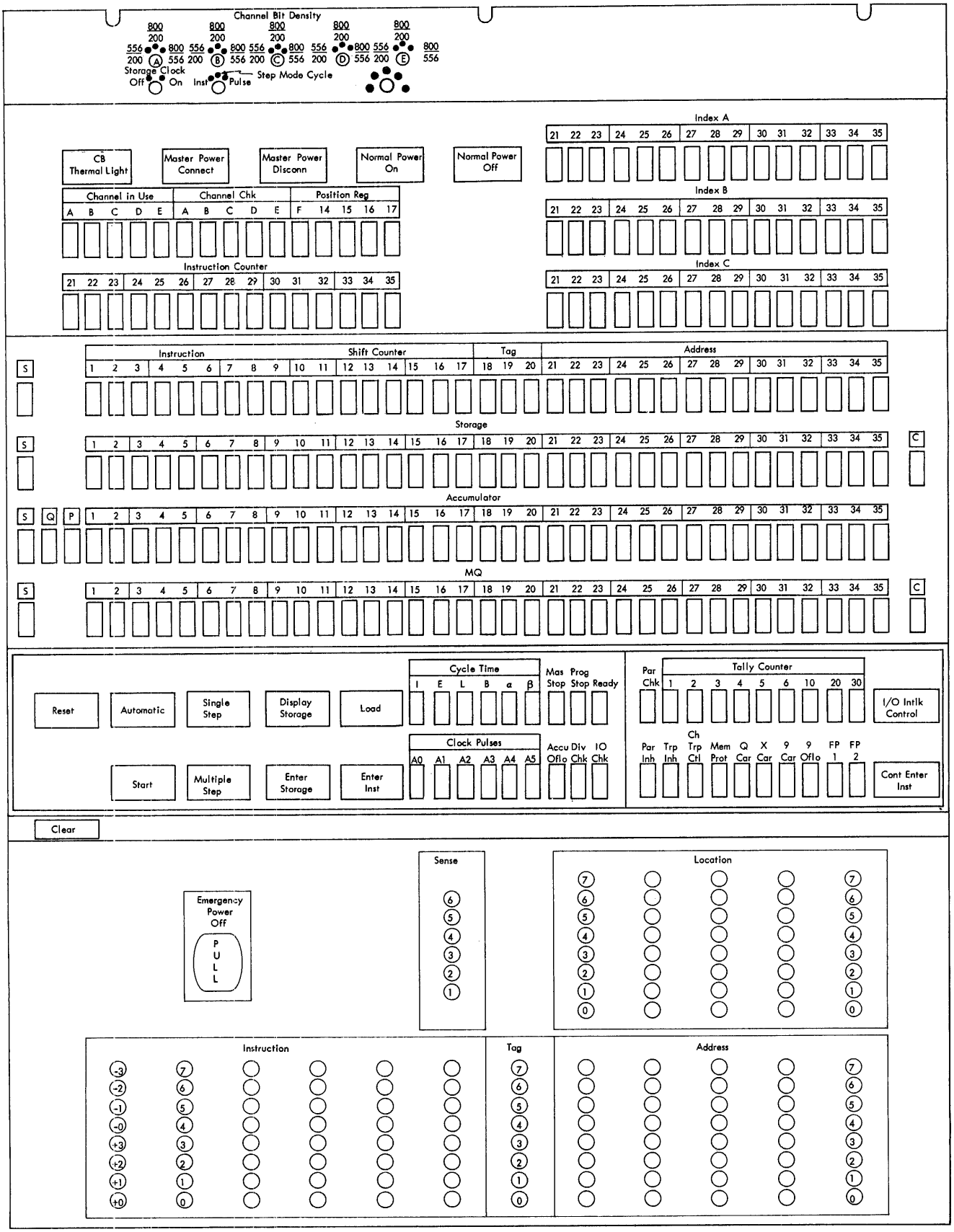


Figure 16. Operator's Console

the selector switch are: INSTRUCTION, CYCLE, PULSE. INSTRUCTION is the normal operation position and provides for execution of a single instruction at the time when the single step key is used. The CYCLE and PULSE positions are customer engineering aids and allow execution to be slowed to observe details of a single instruction.

Address Stop: This switch is used in conjunction with the entry (location) switches. It is a 5-position switch having the following selections:

1. OFF
2. I-Cycle
3. E-Store
4. Channel Store
5. Any

The address at which the operator wishes to stop is first placed in the entry (location) switches. The operator then selects the type of cycle on which to stop. When a coincidence of the selected address and the cycle occurs, the computer stops.

Panel 2

CB Thermal: This light is turned on whenever a circuit breaker, fuse, thermal, or airflow switch in the basic system or auxiliary equipment opens. Power is removed from the system if the opening switch is in the CPU. In auxiliary equipment, power is removed only from the unit.

Master Power Connect: When this switch is on (lit), power is supplied to the sequencing controls and the power-on and power-off switches are active.

Master Power Disconnect: This switch controls power circuits and power applied to the sequencing controls. All power components under control of the system are disconnected from the line power. The power-on switch has no effect in this condition. Pressing this switch (with the system operating) results in a sequenced power-off operation.

Normal Power On: Pressing this switch starts a power-on sequence for the CPU and auxiliary equipment under control of the power distribution unit.

Normal Power Off: Depressing the power-off switch removes all DC voltages and air blower circuits in sequence. The −48 volts control voltage and convenience outlet power remain on.

Channel in Use (A through E): The channel in use indicators, one for each channel, are on for each data channel that is in operation.

Channel Check (A through E): The channel check indicators, one for each channel, are on when a byte or word redundancy has been detected.

Position Register: These five lights reflect the contents of the indirect address trigger (F) and positions 14-17 of the instruction being executed. Positions 15-17 indicate which adapter is being used on a select instruction and the character selected on character-handling instructions.

Instruction Counter: These lights reflect the contents of the instruction counter.

Index A, B, and C: These lights, one for each position of each index register, reflect the contents of the index registers.

Panel 3

Internal CPU Registers: The contents of the instruction register, shift counter, tag register, address counter, storage register, accumulator register, and multiplier-quotient register are reflected by these lights.

Storage Register C: This light reflects the contents of the 37th bit of the word in the storage register.

MQ Register C: This light reflects the parity bit contents of the word being used in an input-output operation on data channel A.

Panel 4

Reset: Pressing this key resets all registers and indicators in the logic section of the processing unit. Core storage is not affected by the reset key, but all data channel registers and indicators are reset.

Automatic: This switch is lit when in AUTOMATIC position. Placing this switch in the MANUAL position stops the processing unit after it has completed execution of the instruction being processed, unless an input-output device is in use. In this case, the computer continues execution of instructions and remains in automatic status until all input-output devices have been disconnected. When the processing unit stops (with this switch in manual) the computer is in manual status. The storage clock continues to run.

Single Step/Multiple Step: When the CPU is in manual status, these keys enable the operator to proceed with this program either one step at a time or at a slow automatic speed. If the computer executes an instruction that causes an input-output unit to be selected, the computer operates in automatic mode until the input-output unit is disconnected. When the disconnect occurs, the computer returns to manual status.

Display Storage: With the CPU in manual status, pressing the display storage key, displays the contents of the core storage location addressed by the entry keys in panel 5 (in the storage register lights). If the storage clock is installed and turned on, the location may be displayed by holding the display storage key depressed. This causes the location to be repeatedly displayed.

Load: This key is active in automatic when the CPU is stopped and no channels are in operation. It is also

operative as a program reset any time the automatic key is not on. The following sequence occurs when the load key is pressed.

When the automatic key is not on (manual):

1. If an instruction is in process, it is given a brief period of time to complete.
2. At the end of this time, an interlock reset occurs even if the present instruction has not completed.

When the automatic key is on (automatic):

1. The instruction set up in the entry keys is executed.
2. The instruction should select a channel and put the channel in use. A channel command with a maximum word count and an address of 00100 is loaded into the selected channel. When the channel in use indicator is turned off, the computer transfers control to location 00101 and continues instruction execution from there.

Start: Pressing the start key continues operation at high speed if the computer has stopped at a program stop, or if the CPU has been returned to automatic after having been in manual status. The start key resets the program stop light, and operations start at the address specified by the contents of the instruction counter.

Enter Storage: With the CPU in manual status, pressing this key places the word in the word bank of the entry keys in core storage at the location set up in the location bank of the entry keys.

Enter Instruction: Pressing this key executes the instruction set up in the word bank of the entry keys. The CPU must be in manual status.

Cycle Timer (I, E, L, B, α, β): The cycle timer lights reflect the current machine cycle being executed. Status of the alpha and beta triggers are also reflected for a 7106 CPU.

Master Stop: This light is on whenever the master stop trigger is on (CPU is logically stopped).

Program Stop: This light is on whenever the computer executes a halt instruction.

Ready: This light is on after power is applied to the computer and remains on except when the computer is in automatic status and the continuous enter-instruction switch is on or the I-O interlock switch is in MANUAL.

Clock Pulses (A0 through A5): These lights reflect the state of the timing ring.

Accumulator Overflow: This light is on during any fixed-point or shifting operation that gives a carry out of position 1 of the accumulator. The light is turned off by execution of a TOV instruction or depression of the reset key.

Divide Check: This light is turned on in fixed-point division if the dividend (accumulator contents) is greater than or equal to the divisor (storage register contents). In floating-point operation, the light is on if the magnitude of the fraction of the dividend is greater than or equal to twice the magnitude of the divisor fraction. The light is tested and turned off by execution of the DCT instruction.

I-O Check: The I-O check light may be turned on by any of the following conditions:

1. If an RCH instruction is decoded and the specified data channel has not been selected.
2. If, during writing, a channel data register has not been loaded with a word from storage by the time its contents are to be sent to the output unit.
3. If, during reading, a channel data register has not transmitted its contents to storage by the time that new data are to be loaded into it from an input unit.
4. If, during reading or writing tapes, two select instructions are given without an RCH instruction between them.

The I-O check light may be turned off by execution of an IOT instruction.

Parity Check: This light is turned on when the parity circuits detect an error. It will be on when the CPU stops on error during storage test operations.

Tally Counter (1, 2, 3, 4, 5, 6, 10, 20, 30): The tally counter differentiates between the L cycles of a floating-point instruction and provides gating for their different operational steps. The counter is divided into two stages. Lights on the console reflect which stage the CPU is currently operating in. Positions 1 through 6 indicate the flow of single precision floating point and positions 10, 20, and 30 together with positions 1 through 6 indicate the flow of double precision floating point.

I-O Interlock Control: When the light in this switch is on, the switch is in MANUAL position; when the light is off the switch is in automatic position. The switch is used with the auto-manual switch as an aid in locating I-O problems. The switch functions as follows:

1. If an I-O unit is selected with the I-O interlock light off, system operation reverts to automatic status even though the auto-manual switch is in MANUAL.
2. If the I-O interlock light is on and the CPU is in manual status when an I-O unit is selected, the CPU executes the select and remains in manual status.

Parity Inhibit: This light is on whenever parity traps are inhibited as a result of a previous parity trap. The light is turned off by execution of a TRP instruction or a machine reset.

Trap Inhibit: This light is on when all interrupt traps are inhibited as a result of any trap. The light is turned off with execution of the TRT or TRP instructions or a machine reset.

Channel Trap Control: This light is off when channel traps are inhibited as a result of a trap or ICT instruction or a machine reset. It is turned on by execution of an RCT or ENB instruction.

Memory Protect: This light is on whenever the machine is operating in the memory protect mode.

Q Carry: This light reflects the condition of the Q-carry trigger. The trigger is turned on whenever a carry out of added Q position occurs.

X Carry: This light is on when the X-carry trigger is on as a result of a carry out of adder position 21.

9 Carry: This light is on whenever a carry occurs out of adder position 9.

9 Overflow: This light is on whenever accumulator position 9 equals 1 in an accumulator left shift or during a 9 carry in an adder to accumulator operation.

FP1 and FP2: The floating point (FP) 1 and 2 lights reflect the condition of floating-point 1 and 2 triggers. The triggers are used to store certain conditions throughout floating-point operations. The lights are customer engineering aids.

Continuous Enter Instruction: When the light in this switch is on, indicating continuous enter instruction mode, the CPU is forced to continuously execute the instruction set up in the entry keys in panel 5 if the CPU is in automatic status and the start key is depressed. It is a customer engineering aid.

Clear: With the computer in automatic status, pressing the clear key resets all areas of core storage to zeros and all registers in the CPU. The clear key also resets all channel registers and indicators. The key is inoperative when the computer is in true manual status.

Panel 5

Emergency Power Off: When this pull type switch is actuated, all power on the system and all auxiliary power are immediately removed. The switch must be mechanically restored. The on-line 1401 and its attached I-O equipment are not affected.

Sense: Six sense switches give the operator manual control over the program while it is being executed at high speed. At various points in the program, executing a sense switch test instruction causes the computer program to follow one of two courses, depending on whether the sense switch tested is depressed. The sense switches are also effective while the computer is in manual status.

Entry Switches: There are two banks of entry switches. The first is an 8 × 5 matrix of switches that allow the operator to enter a location into core storage in octal format. The second bank is an 8 × 12 matrix of switches that enable the operator to insert a word into the computer using octal format. This word is divided into sign, instruction, tag, and address. To enter a word into core storage, the octal representation of the location in core storage to be used is first placed into the location bank switches. Next, the octal representation of the actual word to be entered is placed in the word bank switches. The enter storage key is then pressed, which automatically stores the desired word in the desired location in core storage. These switches are only active when the computer is in manual status.

Machine Resets: The 7040/7044 system has several degrees of reset. In general, the various levels of reset are nested. In other words, the group of registers reset by one level of reset is a sub-group of each higher level reset. Levels of reset, their cause, and what components they reset are:

RESET NAME	CAUSE	COMPONENTS RESET
Clear	Clear Key	Computer Reset
Computer	Clear, Power On, or Reset Key	SR, AC, MQ, IC, and Index registers; IR overflow, AC overflow, Divide check Indicators. Also an interlock reset.
Program	Load Key in manual mode.	Causes an interlock reset and then transfers the IC contents to the address register.
Interlock	Computer or program reset, or load key in automatic mode with master stop trigger on.	AR, PR, position, tag, and SC registers; SR bit 36, trap inhibit, parity inhibit, program stop, memory protect, I/O check indicators. Also causes a channel reset on each channel.
Channel	Interlock reset, or an RDC instruction.	All registers and indicators in the channel.

Systems Compatibility

IBM 7040 and 7044 Data Processing Systems are designed so that as the user grows he can, with a minimum of effort, run a large portion of his program directly on the IBM 7090 or 7094 Data Processing Systems. To assure success, however, the programmer should take certain precautions. There are also certain restrictions to compatibility.

NOTE: All references to the 7094 apply equally to the 7094 II.

Compatible Features

1. Data and instruction word formats, addressing, indexing, indirect addressing, accumulator, multiplier-quotient registers, and the instruction counter are compatible.

Instructions that are compatible include:

Basic instruction set:

ACL	CLS	LGL	SSP	TMI
ADD	COM	LGR	STA	TNZ
ALS	DCT	LLS	STD	TOV
ANA	DVP	LRS	STL	TPL
ARS	ENK	MPY	STO	TRA
CAL	HPR	ORA	STQ	TZE
CAS	LAS	PBT	STZ	VDP
CHS	LBT	RQL	SUB	VLM
CLA	LDQ	SLW	SWT	XEC

Extended performance set:

AXT	LXD	PDX	SXD	TXH
LAC	PAC	PXA	TIX	TXI
LDC	PAX	PXD	TNX	TXL
LXA	PDC	SXA	TSX	

Single-precision floating-point set:

FAD	FMP	UFA	UFM	UFS
FDP	FSB			

Input-output instructions:

BSR	RCH	RUN	TEF	WEF
ETT	RDS	SCH	TRC	WRS
IOT	REW	TCO		

3. Direct data connection is compatible with a 7090 system equipped with RPQ M90976*.

4. Traps common to both 7040/7044 and 7090/7094 operate in the same manner: floating point, direct data, storage clock and interval timer, and channel traps. Adapter interface attention or unusual-end, unit record, or 1401 traps on channel A may not be available on the 7090 or 7094 systems.

*Request for price quotation; availability of this feature can be determined only by requesting a price quotation from IBM.

Incompatible Features

1. The following instructions are not available on the 7090. These instructions have a prefix of −1 (positions S, 1, and 2), which causes a store instruction counter and trap operation on the 7090 or 7094 systems:

Basic instruction set:

STR	TRP	TSL	VMA	

Extended performance set:

CCS	MIT	MSP	PLT	TMT
SAC	MSM	PCS		

Memory protect option:

RPM	SPM

Input-output instructions:

CTR	PWR	SEN	ICT	TDOA
PRD				

1401 option:

SLFA	SLNA

2. The 7040/7044 double-precision floating-point instructions are not available on the 7090 system. Program modification to include a calling sequence to an interpretive routine is required. These instructions are compatible with the 7094:

DFAD	DFSB	DFMP	DFDP

3. Memory parity checking is not available on the 7090 or 7094, but lack of this feature does not affect program execution.

4. Storage protection is not available on the 7090 or 7094. With proper simulation of the RPM and SPM instructions, lack of this feature will not affect normal program execution.

5. Core storage clock and interval timer is similar to RPQ F89349* but the interval timer reset trap is not available on the 7090 or 7094.

6. Input-output incompatibility:

7040/7044	7090/7094
Unoverlapped channel A	no
Console typewriter	no
On-line 1401	no
Disk instructions and traps differ	
12 tape units addressable on channel A	10
Channel word parity trap	no

Detailed Compatibility Information

The following approach to compatibility is not the only one. Note that the 7040 and 7044 are supported by assemblers and compilers that are largely compatible upward to the 7090 and 7094. Most customers, when

converting from 7040/7044 to 7090/7094, would eventually recompile to obtain the most efficient operation. The use of Input-Output Control Systems (IOCS) provides an additional interim direct compatibility approach. It is possible to substitute a functionally equivalent 7090/7094 IOCS for the 7040/7044 IOCS.

Programs and Routines Other than Input-Output

Programs and routines that do not involve I-O instructions can be operated directly on the 7090 or 7094 if a subroutine is used to simulate the 7040/7044 features not provided on the 7090/7094. Instructions common to both systems operate in the same manner on both systems, and 7040/7044 only instructions are provided with a prefix of −1 so that they operate as the STR (store location and trap) instruction when operated on the 7090/7094. This provides a linkage to a subroutine for interpreting and simulating these instructions.

RESTRICTIONS

1. Programs should be written for 32K core storage for proper indexing operation. This restriction also applies to compatibility between 4K, 8K, 16K, and 32K 7040/7044 systems. The index registers, address register, instruction counter, channel address registers and channel word counters are 15 bits, regardless of the storage size. The storage address register will only contain the significant bits, and high-order unused bits will be ignored when referencing a storage location.

2. There must be sufficient unused core storage to contain the simulation routine. A subset of this routine to handle the 7040/7044 STR (−1000) and zero trap (+0000) is necessary even when operating on the 7040/7044. None of the −1 type instructions should appear in this routine or traps on traps will occur in the 7090/7094.

3. Since the operating speeds of the systems differ, there should be no time dependency. This is true between any of the 7040, 7044, 7090, and 7094 systems.

4. The 7040/7044 memory protection feature cannot be functionally simulated. However, the simulation routine can handle RPM and SPM by setting a pseudo-memory protect cell so that these two instructions will behave as they do on the 7040/7044.

5. The 7090 and 7094 do not have word parity trap or interval timer reset traps. Since the TRT and TRP instructions should only occur in these trap routines, the 7090/7094 should never encounter them. These instructions can then be simulated as error halts on the 7090/7094.

6. Any routine that depends upon the interval timer reset trap will not operate on the 7090/7094 even with the RPQ, because this RPQ does not have the reset trap features.

7. The double-precision floating-point arithmetic feature of the 7040-44 is compatible with the 7090/7094 when normalized numbers are used. If un-normalized numbers are used, the results may not be identical.

8. To run a program containing double-precision floating-point on a 7090, it is necessary to reassemble, substituting a calling sequence to an appropriate subroutine for each double-precision instruction.

Tape-only Input-Output

Tape-only input-output routines can be operated directly on the 7090/7094 if the following conditions are met:

1. Channel A must be programmed as if it were overlapped (the 7090 must be assured that channel A is no longer in use by means of the TCOA instruction) before data in the I-O area are used.

2. The RCH (reset and load channel) instruction for a given select instruction must issue within the start time of the 7090 tape devices.

Message Printing

Message printing routines will not operate directly on the printer used with the 7090 and 7094 systems. For this reason, the PWR instruction has a prefix of −1 to cause an STR on the 7090 or 7094. To simplify the 7090/7094 simulation, the RCHA identifying the message should immediately follow the PWR instruction.

Card Input-Output

Card input-output routines will not operate directly on the card reader and punch used with the 7090 and 7094 systems. It is possible, with off-line equipment or with the 7040/7044 to prepare a unit-record tape corresponding to the card input and to punch cards from a tape prepared by the 7090/7094 in lieu of punching cards. In this case, the 7090/7094 will operate its tape I-O directly by means of the 7040/7044 card I-O instructions. This procedure is facilitated by the assignment of tape addresses to the 7040/7044 card equipment. If the card instructions are to properly operate tape on the 7090/7094, a TCOA instruction must be used as above to interlock the 7090 channel, and the RCHA must issue within the 7090/7094 tape start time. (New error routines may also be desired.)

On-Line Job Printing

On-line job printing routines may also be handled as tape operations using the 7040/7044 instructions directly, but a format routine is required. The CTR instruction used by the 7040/7044 for this purpose is provided with a prefix of −1 and will be interpreted

as an STR when operated on the 7090. The resulting trap may be used as a linkage to a routine for re-aligning the print line for off-line tape-to-printer conversion. Again, the TCOA and RCHA restrictions must be observed.

Disk Storage Input-Output

Disk storage input-output routines will not operate directly on the 7090 or 7094. For this reason, all disk file instructions are provided with a prefix of −1 to cause an STR operation in the 7090 or 7094. Through this media, the disk file instructions may be converted to 7909 commands to operate a disk file on the 7090 or 7094.

1401 Input-Output

If the 1401 I-O routines are a direct replacement for the card and/or tape routines, they are compatible upward as described. Compatibility is relinquished, however, if more than ten tape addressed units are used or if any on-line editing or other data modification is performed in the 1401.

1414-4 Devices

The 1414-4 serial I-O devices are only available on the 7090 or 7094 via the 7909 Data Channel interface adapter channel and 1414-6 interface adapter serial I-O buffer. Although a simulation routine is possible, in general, recompiling is easier and much more efficient. The controlling instructions SEN, PRD, and PWR are provided with a prefix −1 to cause a store and trap on the 7090 or 7094 if desired.

Programming Compatibility Notes

PRD, PWR

These two instructions, which are executed identically to RDS and WRS on the 7040 and 7044, should be used when it is desirable to substitute a different I-O routine on the 7090 or 7094 (for example, when using the control adapter or typewriter). It is recommended that the RCH always be given as the next sequential instruction to simplify the store and trap routine.

Note that on channel A, the interface adapter is used to select the card reader, card punch, printer, or 1401 but, if careful planning is used, each device can be given a different tape address so that the 7090 or 7094, which will ignore the interface adapter, will select a tape. In this case, the RDS and WRS can be used rather than PRD and PWR, and the program will be directly compatible.

SEN, CTR

These instructions, which prepare to sense or send control information are used in connection with the interface adapter or with the Tele-Processing equipment on channel A. In general, it is possible to simulate the interface adapter on a 7090 or 7094 with the interface adapter channel. The Tele-Processing equipment on channel A is not usually adaptable to simulation.

SCHA

An SCHA instruction in the 7040 or 7044 is executed as an SLW instruction. This allows the following sequence of instructions to be executed as a general routine for any channel on either the 7040, 7044, 7090, or 7094.

```
CAL     CHA SAV
RDS
RCHX
SLW     CHA SAV
.
.
.
TCOX*
.
.
.
CAL     CHA SAV
SCHX
```

If the RCH was not for channel A, the same thing is stored back in CHA SAV. If it is channel A, then the CHA SAV has the new channel store. This is reloaded with the CAL before the SCH is given, so if it is an SCHA, it will store the AC. Note that the routine also operates correctly on a 7090 or 7094, since the AC is ignored and the TCO (or its equivalent) has assured that the channel is not in use.

TDOA

There is no way to simulate this instruction on the 7090 or 7094, and it is recommended that it be simulated as a TCOA. The programmer should take this into consideration when using this instruction.

ICT

This instruction can only be simulated as an ENB (zero) instruction on the 7090 or 7094. In addition it must be remembered that several instructions will be executed before the ENB zero is executed. Therefore, if the following were given:

```
ENB         MASK
ICT
```

No channel traps could occur on a 7040 or 7044 between the ENB and ICT instructions, but channel traps

could occur on the 7090 or 7094. Note that if the following is given:

```
ICT
.
.
.
RCT
```

All channel traps would be left disabled after the RCT in the 7090 or 7094. If the following is given:

```
ICT
.
.
.
ENB          MASK
```

The above is corrected but, if a redundancy check occurs on the 7040 or 7044 during the instructions between the ICT and ENB, the channel would disconnect immediately. When run on the 7090 or 7094, it would not disconnect until after the ENB MASK instruction.

Trapping Notes

Trap Stores

All traps on the 7040 and 7044 use a full word to store information in the trap store location. On the 7090 and 7094, these stores do not affect the prefix or the tag.

Trap Execution

All traps on the 7040 and 7044 actually transfer to the instruction location. Channel traps and direct data traps on the 7090 and 7094 do not transfer but only execute the instruction at the instruction location. This means that on the 7090 and 7094, if the instruction at the instruction location does not change the contents of the instruction counter, the computer, after executing the instruction, will go back to where it was trapped from. It is necessary, therefore, on the 7040 or 7044 to make sure that this instruction does transfer.

Extra Channel Traps

Note that any operation that causes a channel to go in use will request a channel trap on the 7040 or 7044. On the 7090 or 7094, only an IORT or IOST will cause a trap at their completion, and then only when no LCH instruction is waiting. These extra traps may be used to advantage on the 7040 and 7044 without forsaking compatibility. To do this, it is necessary to never depend on a channel trap. For instance, do not use a transfer to itself waiting for a trap. Instead, when the program finds itself waiting for the completion of an operation, it is necessary to enter the normal trap routine and take over. This will result in slower operation on the 7090 and 7094.

Appendix A. Character Coding and Translations

Code Definitions

Four code structures are used with the 7040 and 7044 systems and input-output equipment. Each code is a specific system of representation of a group of numeric, alphabetic, and special characters. Each can be called a 6-bit code in the sense that 63 or 64 possible code characters exist. Figure 15 shows the four codes and relations between them.

Two sets of graphics are used. One is designed for report writing and the other for programming language. A print head for the console typewriter is available with each graphic set. For other input-output equipment, special character arrangement A agrees with the report writing set and special character arrangement H agrees with the programming language set.

Code headings in Figure 15 are:

H (standard IBM card code) defines the combination of punches used to represent each of the 64 code combinations.

9 (as used in 704, 709, 7040, 7044, 7090, 7094) shows the same characters as normally placed in internal

Report Writing Graphics	Programming Languages Graphics	H Code	9 Code	5 Code	14 Code
ø (zero)	ø	0	00	12	12
1	1	1	01	01	01
2	2	2	02	02	02
3	3	3	03	03	03
4	4	4	04	04	04
5	5	5	05	05	05
6	6	6	06	06	06
7	7	7	07	07	07
8	8	8	10	10	10
9	9	9	11	11	11
b	b	8-2	12	Note	20
#	=	8-3	13	13	13
@	'	8-4	14	14	14
:	:	8-5	15	15	15
>	>	8-6	16	16	16
√ (TM)	√	8-7	17	17	17
&	+	12	20	60	60
A	A	12-1	21	61	61
B	B	12-2	22	62	62
C	C	12-3	23	63	63
D	D	12-4	24	64	64
E	E	12-5	25	65	65
F	F	12-6	26	66	66
G	G	12-7	27	67	67
H	H	12-8	30	70	70
I	I	12-9	31	71	71
?	?	12-0	32	72	72
.	.	12-8-3	33	73	73
□	)	12-8-4	34	74	74
[	[	12-8-5	35	75	75
<	<	12-8-6	36	76	76
‡ (GM)	‡	12-8-7	37	77	77

Report Writing Graphics	Programming Languages Graphics	H Code	9 Code	5 Code	14 Code
-	-	11	40	40	40
J	J	11-1	41	41	41
K	K	11-2	42	42	42
L	L	11-3	43	43	43
M	M	11-4	44	44	44
N	N	11-5	45	45	45
O	O	11-6	46	46	46
P	P	11-7	47	47	47
Q	Q	11-8	50	50	50
R	R	11-9	51	51	51
I	I	11-0	52	52	52
$	$	11-8-3	53	53	53
*	*	11-8-4	54	54	54
]	]	11-8-5	55	55	55
;	;	11-8-6	56	56	56
△	△	11-8-7	57	57	57
blank	blank	No Punch	60	20	00
/	/	0-1	61	21	21
S	S	0-2	62	22	22
T	T	0-3	63	23	23
U	U	0-4	64	24	24
V	V	0-5	65	25	25
W	W	0-6	66	26	26
X	X	0-7	67	27	27
Y	Y	0-8	70	30	30
Z	Z	0-9	71	31	31
‡ (RM)	‡	0-8-2	72	32	32
,	,	0-8-3	73	33	33
%	(	0-8-4	74	34	34
↑	↑	0-8-5	75	35	35
\	\	0-8-6	76	36	36
++	++	0-8-7	77	37	37

Note: The octal combination 00 cannot exist in 5 code because it must be written on BCD tape and would be indistinguishable from blank tape. This means there are only 63 possible combinations in 5 code and that 5 code cannot be used directly to represent essentially binary information, such as programs, arithmetic quantities, and so on from the 7040/7044 system.

Code Translations

Provision is made in the 7040/7044 system for automatic translation from one code to another, as required, when data are transmitted to or from input-output devices. In some cases, it may be necessary to perform programmed translations (either in the 7040/7044 or in an off-line 1401) to achieve a desired result. Programmed translation is required to maintain compatible card formats when binary information is recorded in H code on cards and it is desired to read or punch the cards both on-line on a card reader and off-line via a card-to-tape or tape-to-card operation. Programmed translation can be avoided if the octal group 12 in 9 code can be omitted, since the information can use BCD tape (rather than binary tape) for off-line operations.

Figure 15. 7040 and 7044 Code Combinations

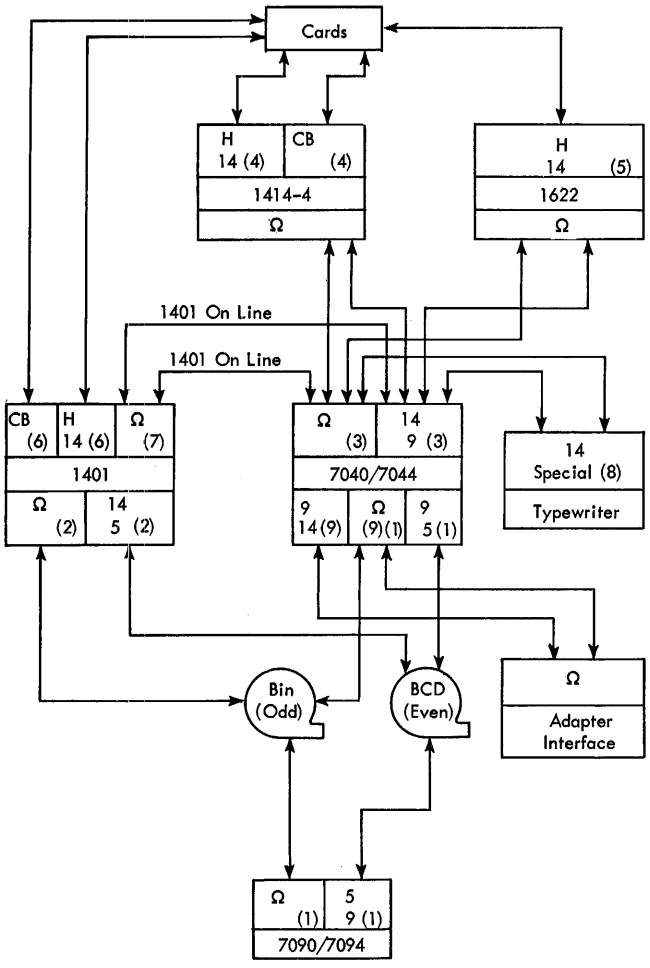
storage of the 7040 and 7044 systems. The six-bit code groups are represented as two octal digits.

5 (as used in the 705, 7080, and on BCD tape) shows the same characters as they normally appear on BCD tape for communication with other IBM magnetic tape equipment. Note that this representation permits only 63 code combinations, not 64.

14 (as used in the 1401, 1410, and 1414) shows the same characters as they normally appear in the internal storage of a 1401 or 1410 and as they exist in the input and output buffers of a 1414 used on the 7040 or 7044.

The octal code groups should be interpreted as representations of a 6-bit pattern in the order of: (B A 8) (4 2 1). For example, 101010 equals 52 octal. Figure 15 is in the order of 9 code. This is the same as the collating sequence on the 7040, 7044, 7090 and 7094 systems.

Figure 16 shows the possible information flow paths between major units of a 7040 or 7044 system and the translations that occur at each interface. The symbol Ω is used to designate no translation. The code group is identical on each side of an Ω interface.



Notes:

(1) The 7040, 7044, 7090, and 7094 Systems use bit 31 of the RDS or WRS instruction to select the Ω or 9-5 translator when reading or writing tape. The same bit also selects even parity or odd parity mode. If bit 31 is 0, even parity and the 9-5 translator are selected; if bit 31 is 1, odd parity and the Ω translator are selected. Note that it is not possible to write a tape record in one mode and read it in the other because solid parity errors will result.

(2) The 1401 system uses the U and B unit select characters (in position 3 of the instruction) to control tape parity and to select the Ω or 14-5 translator. The character U selects even parity and the 14-5 translator; the character B selects odd parity and the Ω translator.

(3) The 7040 and 7044 systems use bit 31 of the RDS and WRS instruction to select the Ω or 14-9 translator when reading or punching cards or transferring to the on-line 1401. Odd parity is used exclusively on transfers to and from the 1414-4, 1622, and the on-line 1401. If bit 31 is 0, the 14-9 translator is selected; if bit 31 is a 1, the Ω translator is selected. Note that it is possible to read a card in either mode regardless of the manner in which the card is punched; however, reading column-binary cards with a BCD read instruction or reading IBM coded cards with a binary read instruction will usually result in confusion. To eliminate this possibility, the programmer should test the status of the 1414 input buffer with the available test instruction before giving the RDS. The manner in which a card is punched is determined by bit 31 in the WRS instruction. A 0 punches cards in H code; a 1 punches column binary cards.

(4) While reading cards, the 1414-4 selects the H-14 or column binary mode on the basis of a 9-7 punch in column 1. If both the 9 and 7 holes are punched in column 1, column binary reading results; otherwise, H-14 reading results. Punching is controlled by the WRS instruction in the CPU as described in Note 3. If the 9-7 punch in column 1 is to appear in the punched card, it must be provided by the program as a part of the data to be punched.

(5) The 1622 will read and punch cards in the H-14 mode when equipped with Expanded Character Set Feature #3831.

(6) The 1401 system selects the column binary mode of reading and punching cards with special read and punch instructions that contain a d modifier character of C. The read column binary operation results in two card images in storage, one in H-14 form and the other in column binary form. The program must then test for a 9-7 punch in column 1 to determine which image to use.

(7) On-line transfers between the 1401 and 7040 systems are accomplished through the serial I-O adapter, which never translates codes. Either the Ω or 14-9 translator can be selected by bit 31 in the 7040 as described in Note 3.

(8) The console typewriter contains a mechanical translator from 14 code to a special tilt-rotate code that positions the printing mechanism.

(9) The 7040 and 7044 systems use bit 31 in the RDS or WRS instruction to select the Ω or 9-14 translator when reading or writing on adapter interface devices. Odd parity is always used with adapter interface devices. If bit 31 is 0, the 9-14 translator is selected; if bit 31 is 1, the Ω translator is selected. While it is possible to write a record in one mode and read it in the other, this practice will usually result in confusion.

Figure 16. Code Translation Data Flow

Appendix B: Instruction List

Instructions for the 7040 and 7044 systems are offered in several options to satisfy different performance requirements. The basic set has been carefully selected to satisfactorily operate a low-compute requirement system application. The extended performance option enhances the computing and compiling ability by providing automatic indexing, logical, character handling, and variable length operation. The automatic floating-point option significantly improves the performance of large number calculations and the double-precision floating-point option provides higher accuracy.

Indirect addressing ability is provided for all appropriate instructions, using the same method as in the 7090, 7094, and 7094 II systems.

With the optional indexing instructions, multiple tags operate in the same manner as the 7090 and 7094 systems.

The following table lists each instruction in the various options and gives average execution times in cycles required for both the 2.0 and 8.0 microsecond core storage.

To obtain the execution times in microseconds, multiply the number of cycles shown by the appropriate cycle time (2.0 or 8.0 microseconds).

Numbers in the TYPE column refer to the Instruction Timing section, which explains special or unusual conditions regarding the timing of the instructions.

INSTRUCT.	OP CODE	AVERAGE CYCLES 7040	7044	TYPE	PAGE
BASIC INSTRUCTION SET					
ACL	+0361	2	2		22
ADD	+0400	2	2		22
ALS	+0767	2	4	1	22
ANA	−0320	2	2		28
ARS	+0771	2	4	1	22
CAL	−0500	2	2		22
CAS	+0340	2	3		28
CHS	+0760 . . 002	1	2		22
CLA	+0500	2	2		22
CLS	+0502	2	2		23
COM	+0760 . . 006	1	2		28
DCT	+0760 . . 012	1	2		23
DVP	+0221	7⅔	20	2	23
ENK	0760 . . 004	1	2		28
HPR	+0420	1	2		23
LAS	−0340	2	3		28
LBT	+0760 . . 001	1	2		23
LDQ	+0560	2	2		23
LGL	−0763	2	4	1	23
LGR	−0765	2	4	1	23
LLS	+0763	2	4	1	24
LRS	+0765	2	4	1	24
MPY	+0200	5	12	3	24
ORA	−0501	2	2		28
PBT	−0760 . . 001	1	2		24
RQL	−0773	2	4	1	24
SLW	+0602	2	2		24
SSP	+0760 . . 003	1	2		25
STA	+0621	3	3		25
STD	+0622	3	3		25
STL	−0625	3	3		25
STO	+0601	2	2		25
STQ	−0600	2	2		25
STR	−1000	2	2		25
STZ	+0600	2	2		25
SUB	+0402	2	2		25
SWT	0760 . . xxxx	1	2		24
TMI	−0120	1	1		26
TNZ	−0100	1	1		26
TOV	+0140	1	1		26
TPL	+0120	1	1		26
TRA	+0020	1	1		26
TRP	−1165	1	1		26
TRT	−1164	1	1		26
TSL	−1627	3	3		26
TZE	0100	1	1		26
VDP	+0225	5	10	4	26
VLM	+0204	4	9	5	27
VMA	−1204	−	−	15	27
XEC	+0522	1	1		27
EXTENDED PERFORMANCE SET					
AXT	+0774	1	1		29
CCS	−1341	2	3		32
LAC	+0535	2	2		29
LDC	−0535	2	2		30
LXA	+0534	2	2		30
LXD	−0534	2	2		30
MIT	−1341	2	3		32
MSM	−1623	3	3		32
MSP	−1623	3	3		32
PAC	+0737	1	2		30
PAX	+0734	1	2		30
PCS	−1505	2	2		32
PDC	−0737	1	2		30
PDX	−0734	1	2		30
PLT	−1341	2	3		32
PXA	+0754	1	2		30
PXD	−0754	1	2		30
SAC	−1623	3	3		32
SXA	+0634	3	3		31
SXD	−0634	3	3		31
TIX	+2000	1	2		31
TMT	−1704	1+2N	2+2N		33
TNX	−2000	1	2		31
TSX	+0074	1	2		31
TXH	+3000	1	2		31
TXI	+1000	1	2		31
TXL	−3000	1	2		31

INSTRUCT.	OP CODE	AVERAGE CYCLES 7040	7044	TYPE	PAGE
SINGLE PRECISION FLOATING POINT SET					
FAD	+0300	3	5½	6	34
FDP	+0241	7	18	7	34
FMP	+0260	4⅓	10	8	34
FSB	+0302	3	5½	6	34
UFA	−0300	2⅔	5	9	35
UFM	−0260	4⅓	10	8	35
UFS	−0302	2⅔	5	9	35
DOUBLE PRECISION FLOATING POINT SET					
DFAD	+0301	4½	8½	10	36
DFDP	−0241	17⅔	48	12	36
DFMP	+0261	12	31	11	36
DFSB	+0303	4½	8½	10	36
MEMORY PROTECT SET					
RPM	−1004	2	2		37
SPM	−1160	1	1		37
DIRECT DATA SET					
PSLB	−0664	2	2		44
PSLC	+0665	2	2		44
PSLD	−0665	2	2		44
PSLE	+0666	2	2		44
SSLB	−0660	2	2		45
SSLC	+0661	2	2		45
SSLD	−0661	2	2		45
SSLE	+0662	2	2		45

INSTRUCT.	OP CODE	AVERAGE CYCLES 7040	7044	TYPE	PAGE
INPUT-OUTPUT INSTRUCTIONS					
BSR	+0764	2	4	13, 14	40
CTR	−1766	1	2		39
ENB	+0564	2	2		43
ETT	−0760 . . x2xx	1	2	13	40
ICT	−1760 . . 014	1	2		44
IOT	+0760 . . 005	1	2		41
PRD	−1762	2	4	13	38
PWR	−1766	2	4	13	38
RCHA	+0540	2	2		40
RCT	+0760 . . 014	1	2		44
RDC	+0760 . . x352	1	2		41
RDS	+0762	2	4	13	38
REW	+0772	2	4	13, 14	41
RUN	−0772	2	4	13, 14	41
SCH	+0640	2	2		41
SEN	−1762	1	2	13	39
TCO	+0060	1	2		42
TDOA	−1060	1	2		42
TEF	+0030	1	2		42
TRC	+0022	1	2		42
WBT	+0766	2	4	13	43
WEF	+0770	2	4	13, 14	43
WRS	+0766	2	4	13	38
1401 OPTION SET					
SLFA	−1760 . . 1501	1	2		67
SLNA	−1760 . . 1541	1	2		67

Appendix C. Powers of Two Table

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125

Appendix D. Octal-Decimal Integer Conversion Table

0000 (Octal)	0000 (Decimal)
to	to
0777 (Octal)	0511 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
0000	0000	0001	0002	0003	0004	0005	0006	0007
0010	0008	0009	0010	0011	0012	0013	0014	0015
0020	0016	0017	0018	0019	0020	0021	0022	0023
0030	0024	0025	0026	0027	0028	0029	0030	0031
0040	0032	0033	0034	0035	0036	0037	0038	0039
0050	0040	0041	0042	0043	0044	0045	0046	0047
0060	0048	0049	0050	0051	0052	0053	0054	0055
0070	0056	0057	0058	0059	0060	0061	0062	0063
0100	0064	0065	0066	0067	0068	0069	0070	0071
0110	0072	0073	0074	0075	0076	0077	0078	0079
0120	0080	0081	0082	0083	0084	0085	0086	0087
0130	0088	0089	0090	0091	0092	0093	0094	0095
0140	0096	0097	0098	0099	0100	0101	0102	0103
0150	0104	0105	0106	0107	0108	0109	0110	0111
0160	0112	0113	0114	0115	0116	0117	0118	0119
0170	0120	0121	0122	0123	0124	0125	0126	0127
0200	0128	0129	0130	0131	0132	0133	0134	0135
0210	0136	0137	0138	0139	0140	0141	0142	0143
0220	0144	0145	0146	0147	0148	0149	0150	0151
0230	0152	0153	0154	0155	0156	0157	0158	0159
0240	0160	0161	0162	0163	0164	0165	0166	0167
0250	0168	0169	0170	0171	0172	0173	0174	0175
0260	0176	0177	0178	0179	0180	0181	0182	0183
0270	0184	0185	0186	0187	0188	0189	0190	0191
0300	0192	0193	0194	0195	0196	0197	0198	0199
0310	0200	0201	0202	0203	0204	0205	0206	0207
0320	0208	0209	0210	0211	0212	0213	0214	0215
0330	0216	0217	0218	0219	0220	0221	0222	0223
0340	0224	0225	0226	0227	0228	0229	0230	0231
0350	0232	0233	0234	0235	0236	0237	0238	0239
0360	0240	0241	0242	0243	0244	0245	0246	0247
0370	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7
0400	0256	0257	0258	0259	0260	0261	0262	0263
0410	0264	0265	0266	0267	0268	0269	0270	0271
0420	0272	0273	0274	0275	0276	0277	0278	0279
0430	0280	0281	0282	0283	0284	0285	0286	0287
0440	0288	0289	0290	0291	0292	0293	0294	0295
0450	0296	0297	0298	0299	0300	0301	0302	0303
0460	0304	0305	0306	0307	0308	0309	0310	0311
0470	0312	0313	0314	0315	0316	0317	0318	0319
0500	0320	0321	0322	0323	0324	0325	0326	0327
0510	0328	0329	0330	0331	0332	0333	0334	0335
0520	0336	0337	0338	0339	0340	0341	0342	0343
0530	0344	0345	0346	0347	0348	0349	0350	0351
0540	0352	0353	0354	0355	0356	0357	0358	0359
0550	0360	0361	0362	0363	0364	0365	0366	0367
0560	0368	0369	0370	0371	0372	0373	0374	0375
0570	0376	0377	0378	0379	0380	0381	0382	0383
0600	0384	0385	0386	0387	0388	0389	0390	0391
0610	0392	0393	0394	0395	0396	0397	0398	0399
0620	0400	0401	0402	0403	0404	0405	0406	0407
0630	0408	0409	0410	0411	0412	0413	0414	0415
0640	0416	0417	0418	0419	0420	0421	0422	0423
0650	0424	0425	0426	0427	0428	0429	0430	0431
0660	0432	0433	0434	0435	0436	0437	0438	0439
0670	0440	0441	0442	0443	0444	0445	0446	0447
0700	0448	0449	0450	0451	0452	0453	0454	0455
0710	0456	0457	0458	0459	0460	0461	0462	0463
0720	0464	0465	0466	0467	0468	0469	0470	0471
0730	0472	0473	0474	0475	0476	0477	0478	0479
0740	0480	0481	0482	0483	0484	0485	0486	0487
0750	0488	0489	0490	0491	0492	0493	0494	0495
0760	0496	0497	0498	0499	0500	0501	0502	0503
0770	0504	0505	0506	0507	0508	0509	0510	0511

1000 (Octal)	0512 (Decimal)
to	to
1777 (Octal)	1023 (Decimal)

	0	1	2	3	4	5	6	7
1000	0512	0513	0514	0515	0516	0517	0518	0519
1010	0520	0521	0522	0523	0524	0525	0526	0527
1020	0528	0529	0530	0531	0532	0533	0534	0535
1030	0536	0537	0538	0539	0540	0541	0542	0543
1040	0544	0545	0546	0547	0548	0549	0550	0551
1050	0552	0553	0554	0555	0556	0557	0558	0559
1060	0560	0561	0562	0563	0564	0565	0566	0567
1070	0568	0569	0570	0571	0572	0573	0574	0575
1100	0576	0577	0578	0579	0580	0581	0582	0583
1110	0584	0585	0586	0587	0588	0589	0590	0591
1120	0592	0593	0594	0595	0596	0597	0598	0599
1130	0600	0601	0602	0603	0604	0605	0606	0607
1140	0608	0609	0610	0611	0612	0613	0614	0615
1150	0616	0617	0618	0619	0620	0621	0622	0623
1160	0624	0625	0626	0627	0628	0629	0630	0631
1170	0632	0633	0634	0635	0636	0637	0638	0639
1200	0640	0641	0642	0643	0644	0645	0646	0647
1210	0648	0649	0650	0651	0652	0653	0654	0655
1220	0656	0657	0658	0659	0660	0661	0662	0663
1230	0664	0665	0666	0667	0668	0669	0670	0671
1240	0672	0673	0674	0675	0676	0677	0678	0679
1250	0680	0681	0682	0683	0684	0685	0686	0687
1260	0688	0689	0690	0691	0692	0693	0694	0695
1270	0696	0697	0698	0699	0700	0701	0702	0703
1300	0704	0705	0706	0707	0708	0709	0710	0711
1310	0712	0713	0714	0715	0716	0717	0718	0719
1320	0720	0721	0722	0723	0724	0725	0726	0727
1330	0728	0729	0730	0731	0732	0733	0734	0735
1340	0736	0737	0738	0739	0740	0741	0742	0743
1350	0744	0745	0746	0747	0748	0749	0750	0751
1360	0752	0753	0754	0755	0756	0757	0758	0759
1370	0760	0761	0762	0763	0764	0765	0766	0767

	0	1	2	3	4	5	6	7
1400	0768	0769	0770	0771	0772	0773	0774	0775
1410	0776	0777	0778	0779	0780	0781	0782	0783
1420	0784	0785	0786	0787	0788	0789	0790	0791
1430	0792	0793	0794	0795	0796	0797	0798	0799
1440	0800	0801	0802	0803	0804	0805	0806	0807
1450	0808	0809	0810	0811	0812	0813	0814	0815
1460	0816	0817	0818	0819	0820	0821	0822	0823
1470	0824	0825	0826	0827	0828	0829	0830	0831
1500	0832	0833	0834	0835	0836	0837	0838	0839
1510	0840	0841	0842	0843	0844	0845	0846	0847
1520	0848	0849	0850	0851	0852	0853	0854	0855
1530	0856	0857	0858	0859	0860	0861	0862	0863
1540	0864	0865	0866	0867	0868	0869	0870	0871
1550	0872	0873	0874	0875	0876	0877	0878	0879
1560	0880	0881	0882	0883	0884	0885	0886	0887
1570	0888	0889	0890	0891	0892	0893	0894	0895
1600	0896	0897	0898	0899	0900	0901	0902	0903
1610	0904	0905	0906	0907	0908	0909	0910	0911
1620	0912	0913	0914	0915	0916	0917	0918	0919
1630	0920	0921	0922	0923	0924	0925	0926	0927
1640	0928	0929	0930	0931	0932	0933	0934	0935
1650	0936	0937	0938	0939	0940	0941	0942	0943
1660	0944	0945	0946	0947	0948	0949	0950	0951
1670	0952	0953	0954	0955	0956	0957	0958	0959
1700	0960	0961	0962	0963	0964	0965	0966	0967
1710	0968	0969	0970	0971	0972	0973	0974	0975
1720	0976	0977	0978	0979	0980	0981	0982	0983
1730	0984	0985	0986	0987	0988	0989	0990	0991
1740	0992	0993	0994	0995	0996	0997	0998	0999
1750	1000	1001	1002	1003	1004	1005	1006	1007
1760	1008	1009	1010	1011	1012	1013	1014	1015
1770	1016	1017	1018	1019	1020	1021	1022	1023

Octal-Decimal Integer Conversion Table

	0	1	2	3	4	5	6	7
2000	1024	1025	1026	1027	1028	1029	1030	1031
2010	1032	1033	1034	1035	1036	1037	1038	1039
2020	1040	1041	1042	1043	1044	1045	1046	1047
2030	1048	1049	1050	1051	1052	1053	1054	1055
2040	1056	1057	1058	1059	1060	1061	1062	1063
2050	1064	1065	1066	1067	1068	1069	1070	1071
2060	1072	1073	1074	1075	1076	1077	1078	1079
2070	1080	1081	1082	1083	1084	1085	1086	1087
2100	1088	1089	1090	1091	1092	1093	1094	1095
2110	1096	1097	1098	1099	1100	1101	1102	1103
2120	1104	1105	1106	1107	1108	1109	1110	1111
2130	1112	1113	1114	1115	1116	1117	1118	1119
2140	1120	1121	1122	1123	1124	1125	1126	1127
2150	1128	1129	1130	1131	1132	1133	1134	1135
2160	1136	1137	1138	1139	1140	1141	1142	1143
2170	1144	1145	1146	1147	1148	1149	1150	1151
2200	1152	1153	1154	1155	1156	1157	1158	1159
2210	1160	1161	1162	1163	1164	1165	1166	1167
2220	1168	1169	1170	1171	1172	1173	1174	1175
2230	1176	1177	1178	1179	1180	1181	1182	1183
2240	1184	1185	1186	1187	1188	1189	1190	1191
2250	1192	1193	1194	1195	1196	1197	1198	1199
2260	1200	1201	1202	1203	1204	1205	1206	1207
2270	1208	1209	1210	1211	1212	1213	1214	1215
2300	1216	1217	1218	1219	1220	1221	1222	1223
2310	1224	1225	1226	1227	1228	1229	1230	1231
2320	1232	1233	1234	1235	1236	1237	1238	1239
2330	1240	1241	1242	1243	1244	1245	1246	1247
2340	1248	1249	1250	1251	1252	1253	1254	1255
2350	1256	1257	1258	1259	1260	1261	1262	1263
2360	1264	1265	1266	1267	1268	1269	1270	1271
2370	1272	1273	1274	1275	1276	1277	1278	1279

	0	1	2	3	4	5	6	7
2400	1280	1281	1282	1283	1284	1285	1286	1287
2410	1288	1289	1290	1291	1292	1293	1294	1295
2420	1296	1297	1298	1299	1300	1301	1302	1303
2430	1304	1305	1306	1307	1308	1309	1310	1311
2440	1312	1313	1314	1315	1316	1317	1318	1319
2450	1320	1321	1322	1323	1324	1325	1326	1327
2460	1328	1329	1330	1331	1332	1333	1334	1335
2470	1336	1337	1338	1339	1340	1341	1342	1343
2500	1344	1345	1346	1347	1348	1349	1350	1351
2510	1352	1353	1354	1355	1356	1357	1358	1359
2520	1360	1361	1362	1363	1364	1365	1366	1367
2530	1368	1369	1370	1371	1372	1373	1374	1375
2540	1376	1377	1378	1379	1380	1381	1382	1383
2550	1384	1385	1386	1387	1388	1389	1390	1391
2560	1392	1393	1394	1395	1396	1397	1398	1399
2570	1400	1401	1402	1403	1404	1405	1406	1407
2600	1408	1409	1410	1411	1412	1413	1414	1415
2610	1416	1417	1418	1419	1420	1421	1422	1423
2620	1424	1425	1426	1427	1428	1429	1430	1431
2630	1432	1433	1434	1435	1436	1437	1438	1439
2640	1440	1441	1442	1443	1444	1445	1446	1447
2650	1448	1449	1450	1451	1452	1453	1454	1455
2660	1456	1457	1458	1459	1460	1461	1462	1463
2670	1464	1465	1466	1467	1468	1469	1470	1471
2700	1472	1473	1474	1475	1476	1477	1478	1479
2710	1480	1481	1482	1483	1484	1485	1486	1487
2720	1488	1489	1490	1491	1492	1493	1494	1495
2730	1496	1497	1498	1499	1500	1501	1502	1503
2740	1504	1505	1506	1507	1508	1509	1510	1511
2750	1512	1513	1514	1515	1516	1517	1518	1519
2760	1520	1521	1522	1523	1524	1525	1526	1527
2770	1528	1529	1530	1531	1532	1533	1534	1535

2000 to 2777 (Octal)	1024 to 1535 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
3000	1536	1537	1538	1539	1540	1541	1542	1543
3010	1544	1545	1546	1547	1548	1549	1550	1551
3020	1552	1553	1554	1555	1556	1557	1558	1559
3030	1560	1561	1562	1563	1564	1565	1566	1567
3040	1568	1569	1570	1571	1572	1573	1574	1575
3050	1576	1577	1578	1579	1580	1581	1582	1583
3060	1584	1585	1586	1587	1588	1589	1590	1591
3070	1592	1593	1594	1595	1596	1597	1598	1599
3100	1600	1601	1602	1603	1604	1605	1606	1607
3110	1608	1609	1610	1611	1612	1613	1614	1615
3120	1616	1617	1618	1619	1620	1621	1622	1623
3130	1624	1625	1626	1627	1628	1629	1630	1631
3140	1632	1633	1634	1635	1636	1637	1638	1639
3150	1640	1641	1642	1643	1644	1645	1646	1647
3160	1648	1649	1650	1651	1652	1653	1654	1655
3170	1656	1657	1658	1659	1660	1661	1662	1663
3200	1664	1665	1666	1667	1668	1669	1670	1671
3210	1672	1673	1674	1675	1676	1677	1678	1679
3220	1680	1681	1682	1683	1684	1685	1686	1687
3230	1688	1689	1690	1691	1692	1693	1694	1695
3240	1696	1697	1698	1699	1700	1701	1702	1703
3250	1704	1705	1706	1707	1708	1709	1710	1711
3260	1712	1713	1714	1715	1716	1717	1718	1719
3270	1720	1721	1722	1723	1724	1725	1726	1727
3300	1728	1729	1730	1731	1732	1733	1734	1735
3310	1736	1737	1738	1739	1740	1741	1742	1743
3320	1744	1745	1746	1747	1748	1749	1750	1751
3330	1752	1753	1754	1755	1756	1757	1758	1759
3340	1760	1761	1762	1763	1764	1765	1766	1767
3350	1768	1769	1770	1771	1772	1773	1774	1775
3360	1776	1777	1778	1779	1780	1781	1782	1783
3370	1784	1785	1786	1787	1788	1789	1790	1791

	0	1	2	3	4	5	6	7
3400	1792	1793	1794	1795	1796	1797	1798	1799
3410	1800	1801	1802	1803	1804	1805	1806	1807
3420	1808	1809	1810	1811	1812	1813	1814	1815
3430	1816	1817	1818	1819	1820	1821	1822	1823
3440	1824	1825	1826	1827	1828	1829	1830	1831
3450	1832	1833	1834	1835	1836	1837	1838	1839
3460	1840	1841	1842	1843	1844	1845	1846	1847
3470	1848	1849	1850	1851	1852	1853	1854	1855
3500	1856	1857	1858	1859	1860	1861	1862	1863
3510	1864	1865	1866	1867	1868	1869	1870	1871
3520	1872	1873	1874	1875	1876	1877	1878	1879
3530	1880	1881	1882	1883	1884	1885	1886	1887
3540	1888	1889	1890	1891	1892	1893	1894	1895
3550	1896	1897	1898	1899	1900	1901	1902	1903
3560	1904	1905	1906	1907	1908	1909	1910	1911
3570	1912	1913	1914	1915	1916	1917	1918	1919
3600	1920	1921	1922	1923	1924	1925	1926	1927
3610	1928	1929	1930	1931	1932	1933	1934	1935
3620	1936	1937	1938	1939	1940	1941	1942	1943
3630	1944	1945	1946	1947	1948	1949	1950	1951
3640	1952	1953	1954	1955	1956	1957	1958	1959
3650	1960	1961	1962	1963	1964	1965	1966	1967
3660	1968	1969	1970	1971	1972	1973	1974	1975
3670	1976	1977	1978	1979	1980	1981	1982	1983
3700	1984	1985	1986	1987	1988	1989	1990	1991
3710	1992	1993	1994	1995	1996	1997	1998	1999
3720	2000	2001	2002	2003	2004	2005	2006	2007
3730	2008	2009	2010	2011	2012	2013	2014	2015
3740	2016	2017	2018	2019	2020	2021	2022	2023
3750	2024	2025	2026	2027	2028	2029	2030	2031
3760	2032	2033	2034	2035	2036	2037	2038	2039
3770	2040	2041	2042	2043	2044	2045	2046	2047

3000 to 3777 (Octal)	1536 to 2047 (Decimal)

Octal-Decimal Integer Conversion Table

4000 to 4777 (Octal)	2048 to 2559 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
4000	2048	2049	2050	2051	2052	2053	2054	2055
4010	2056	2057	2058	2059	2060	2061	2062	2063
4020	2064	2065	2066	2067	2068	2069	2070	2071
4030	2072	2073	2074	2075	2076	2077	2078	2079
4040	2080	2081	2082	2083	2084	2085	2086	2087
4050	2088	2089	2090	2091	2092	2093	2094	2095
4060	2096	2097	2098	2099	2100	2101	2102	2103
4070	2104	2105	2106	2107	2108	2109	2110	2111
4100	2112	2113	2114	2115	2116	2117	2118	2119
4110	2120	2121	2122	2123	2124	2125	2126	2127
4120	2128	2129	2130	2131	2132	2133	2134	2135
4130	2136	2137	2138	2139	2140	2141	2142	2143
4140	2144	2145	2146	2147	2148	2149	2150	2151
4150	2152	2153	2154	2155	2156	2157	2158	2159
4160	2160	2161	2162	2163	2164	2165	2166	2167
4170	2168	2169	2170	2171	2172	2173	2174	2175
4200	2176	2177	2178	2179	2180	2181	2182	2183
4210	2184	2185	2186	2187	2188	2189	2190	2191
4220	2192	2193	2194	2195	2196	2197	2198	2199
4230	2200	2201	2202	2203	2204	2205	2206	2207
4240	2208	2209	2210	2211	2212	2213	2214	2215
4250	2216	2217	2218	2219	2220	2221	2222	2223
4260	2224	2225	2226	2227	2228	2229	2230	2231
4270	2232	2233	2234	2235	2236	2237	2238	2239
4300	2240	2241	2242	2243	2244	2245	2246	2247
4310	2248	2249	2250	2251	2252	2253	2254	2255
4320	2256	2257	2258	2259	2260	2261	2262	2263
4330	2264	2265	2266	2267	2268	2269	2270	2271
4340	2272	2273	2274	2275	2276	2277	2278	2279
4350	2280	2281	2282	2283	2284	2285	2286	2287
4360	2288	2289	2290	2291	2292	2293	2294	2295
4370	2296	2297	2298	2299	2300	2301	2302	2303

	0	1	2	3	4	5	6	7
4400	2304	2305	2306	2307	2308	2309	2310	2311
4410	2312	2313	2314	2315	2316	2317	2318	2319
4420	2320	2321	2322	2323	2324	2325	2326	2327
4430	2328	2329	2330	2331	2332	2333	2334	2335
4440	2336	2337	2338	2339	2340	2341	2342	2343
4450	2344	2345	2346	2347	2348	2349	2350	2351
4460	2352	2353	2354	2355	2356	2357	2358	2359
4470	2360	2361	2362	2363	2364	2365	2366	2367
4500	2368	2369	2370	2371	2372	2373	2374	2375
4510	2376	2377	2378	2379	2380	2381	2382	2383
4520	2384	2385	2386	2387	2388	2389	2390	2391
4530	2392	2393	2394	2395	2396	2397	2398	2399
4540	2400	2401	2402	2403	2404	2405	2406	2407
4550	2408	2409	2410	2411	2412	2413	2414	2415
4560	2416	2417	2418	2419	2420	2421	2422	2423
4570	2424	2425	2426	2427	2428	2429	2430	2431
4600	2432	2433	2434	2435	2436	2437	2438	2439
4610	2440	2441	2442	2443	2444	2445	2446	2447
4620	2448	2449	2450	2451	2452	2453	2454	2455
4630	2456	2457	2458	2459	2460	2461	2462	2463
4640	2464	2465	2466	2467	2468	2469	2470	2471
4650	2472	2473	2474	2475	2476	2477	2478	2479
4660	2480	2481	2482	2483	2484	2485	2486	2487
4670	2488	2489	2490	2491	2492	2493	2494	2495
4700	2496	2497	2498	2499	2500	2501	2502	2503
4710	2504	2505	2506	2507	2508	2509	2510	2511
4720	2512	2513	2514	2515	2516	2517	2518	2519
4730	2520	2521	2522	2523	2524	2525	2526	2527
4740	2528	2529	2530	2531	2532	2533	2534	2535
4750	2536	2537	2538	2539	2540	2541	2542	2543
4760	2544	2545	2546	2547	2548	2549	2550	2551
4770	2552	2553	2554	2555	2556	2557	2558	2559

5000 to 5777 (Octal)	2560 to 3071 (Decimal)

	0	1	2	3	4	5	6	7
5000	2560	2561	2562	2563	2564	2565	2566	2567
5010	2568	2569	2570	2571	2572	2573	2574	2575
5020	2576	2577	2578	2579	2580	2581	2582	2583
5030	2584	2585	2586	2587	2588	2589	2590	2591
5040	2592	2593	2594	2595	2596	2597	2598	2599
5050	2600	2601	2602	2603	2604	2605	2606	2607
5060	2608	2609	2610	2611	2612	2613	2614	2615
5070	2616	2617	2618	2619	2620	2621	2622	2623
5100	2624	2625	2626	2627	2628	2629	2630	2631
5110	2632	2633	2634	2635	2636	2637	2638	2639
5120	2640	2641	2642	2643	2644	2645	2646	2647
5130	2648	2649	2650	2651	2652	2653	2654	2655
5140	2656	2657	2658	2659	2660	2661	2662	2663
5150	2664	2665	2666	2667	2668	2669	2670	2671
5160	2672	2673	2674	2675	2676	2677	2678	2679
5170	2680	2681	2682	2683	2684	2685	2686	2687
5200	2688	2689	2690	2691	2692	2693	2694	2695
5210	2696	2697	2698	2699	2700	2701	2702	2703
5220	2704	2705	2706	2707	2708	2709	2710	2711
5230	2712	2713	2714	2715	2716	2717	2718	2719
5240	2720	2721	2722	2723	2724	2725	2726	2727
5250	2728	2729	2730	2731	2732	2733	2734	2735
5260	2736	2737	2738	2739	2740	2741	2742	2743
5270	2744	2745	2746	2747	2748	2749	2750	2751
5300	2752	2753	2754	2755	2756	2757	2758	2759
5310	2760	2761	2762	2763	2764	2765	2766	2767
5320	2768	2769	2770	2771	2772	2773	2774	2775
5330	2776	2777	2778	2779	2780	2781	2782	2783
5340	2784	2785	2786	2787	2788	2789	2790	2791
5350	2792	2793	2794	2795	2796	2797	2798	2799
5360	2800	2801	2802	2803	2804	2805	2806	2807
5370	2808	2809	2810	2811	2812	2813	2814	2815

	0	1	2	3	4	5	6	7
5400	2816	2817	2818	2819	2820	2821	2822	2823
5410	2824	2825	2826	2827	2828	2829	2830	2831
5420	2832	2833	2834	2835	2836	2837	2838	2839
5430	2840	2841	2842	2843	2844	2845	2846	2847
5440	2848	2849	2850	2851	2852	2853	2854	2855
5450	2856	2857	2858	2859	2860	2861	2862	2863
5460	2864	2865	2866	2867	2868	2869	2870	2871
5470	2872	2873	2874	2875	2876	2877	2878	2879
5500	2880	2881	2882	2883	2884	2885	2886	2887
5510	2888	2889	2890	2891	2892	2893	2894	2895
5520	2896	2897	2898	2899	2900	2901	2902	2903
5530	2904	2905	2906	2907	2908	2909	2910	2911
5540	2912	2913	2914	2915	2916	2917	2918	2919
5550	2920	2921	2922	2923	2924	2925	2926	2927
5560	2928	2929	2930	2931	2932	2933	2934	2935
5570	2936	2937	2938	2939	2940	2941	2942	2943
5600	2944	2945	2946	2947	2948	2949	2950	2951
5610	2952	2953	2954	2955	2956	2957	2958	2959
5620	2960	2961	2962	2963	2964	2965	2966	2967
5630	2968	2969	2970	2971	2972	2973	2974	2975
5640	2976	2977	2978	2979	2980	2981	2982	2983
5650	2984	2985	2986	2987	2988	2989	2990	2991
5660	2992	2993	2994	2995	2996	2997	2998	2999
5670	3000	3001	3002	3003	3004	3005	3006	3007
5700	3008	3009	3010	3011	3012	3013	3014	3015
5710	3016	3017	3018	3019	3020	3021	3022	3023
5720	3024	3025	3026	3027	3028	3029	3030	3031
5730	3032	3033	3034	3035	3036	3037	3038	3039
5740	3040	3041	3042	3043	3044	3045	3046	3047
5750	3048	3049	3050	3051	3052	3053	3054	3055
5760	3056	3057	3058	3059	3060	3061	3062	3063
5770	3064	3065	3066	3067	3068	3069	3070	3071

Octal-Decimal Integer Conversion Table

	0	1	2	3	4	5	6	7
6000	3072	3073	3074	3075	3076	3077	3078	3079
6010	3080	3081	3082	3083	3084	3085	3086	3087
6020	3088	3089	3090	3091	3092	3093	3094	3095
6030	3096	3097	3098	3099	3100	3101	3102	3103
6040	3104	3105	3106	3107	3108	3109	3110	3111
6050	3112	3113	3114	3115	3116	3117	3118	3119
6060	3120	3121	3122	3123	3124	3125	3126	3127
6070	3128	3129	3130	3131	3132	3133	3134	3135
6100	3136	3137	3138	3139	3140	3141	3142	3143
6110	3144	3145	3146	3147	3148	3149	3150	3151
6120	3152	3153	3154	3155	3156	3157	3158	3159
6130	3160	3161	3162	3163	3164	3165	3166	3167
6140	3168	3169	3170	3171	3172	3173	3174	3175
6150	3176	3177	3178	3179	3180	3181	3182	3183
6160	3184	3185	3186	3187	3188	3189	3190	3191
6170	3192	3193	3194	3195	3196	3197	3198	3199
6200	3200	3201	3202	3203	3204	3205	3206	3207
6210	3208	3209	3210	3211	3212	3213	3214	3215
6220	3216	3217	3218	3219	3220	3221	3222	3223
6230	3224	3225	3226	3227	3228	3229	3230	3231
6240	3232	3233	3234	3235	3236	3237	3238	3239
6250	3240	3241	3242	3243	3244	3245	3246	3247
6260	3248	3249	3250	3251	3252	3253	3254	3255
6270	3256	3257	3258	3259	3260	3261	3262	3263
6300	3264	3265	3266	3267	3268	3269	3270	3271
6310	3272	3273	3274	3275	3276	3277	3278	3279
6320	3280	3281	3282	3283	3284	3285	3286	3287
6330	3288	3289	3290	3291	3292	3293	3294	3295
6340	3296	3297	3298	3299	3300	3301	3302	3303
6350	3304	3305	3306	3307	3308	3309	3310	3311
6360	3312	3313	3314	3315	3316	3317	3318	3319
6370	3320	3321	3322	3323	3324	3325	3326	3327

	0	1	2	3	4	5	6	7
6400	3328	3329	3330	3331	3332	3333	3334	3335
6410	3336	3337	3338	3339	3340	3341	3342	3343
6420	3344	3345	3346	3347	3348	3349	3350	3351
6430	3352	3353	3354	3355	3356	3357	3358	3359
6440	3360	3361	3362	3363	3364	3365	3366	3367
6450	3368	3369	3370	3371	3372	3373	3374	3375
6460	3376	3377	3378	3379	3380	3381	3382	3383
6470	3384	3385	3386	3387	3388	3389	3390	3391
6500	3392	3393	3394	3395	3396	3397	3398	3399
6510	3400	3401	3402	3403	3404	3405	3406	3407
6520	3408	3409	3410	3411	3412	3413	3414	3415
6530	3416	3417	3418	3419	3420	3421	3422	3423
6540	3424	3425	3426	3427	3428	3429	3430	3431
6550	3432	3433	3434	3435	3436	3437	3438	3439
6560	3440	3441	3442	3443	3444	3445	3446	3447
6570	3448	3449	3450	3451	3452	3453	3454	3455
6600	3456	3457	3458	3459	3460	3461	3462	3463
6610	3464	3465	3466	3467	3468	3469	3470	3471
6620	3472	3473	3474	3475	3476	3477	3478	3479
6630	3480	3481	3482	3483	3484	3485	3486	3487
6640	3488	3489	3490	3491	3492	3493	3494	3495
6650	3496	3497	3498	3499	3500	3501	3502	3503
6660	3504	3505	3506	3507	3508	3509	3510	3511
6670	3512	3513	3514	3515	3516	3517	3518	3519
6700	3520	3521	3522	3523	3524	3525	3526	3527
6710	3528	3529	3530	3531	3532	3533	3534	3535
6720	3536	3537	3538	3539	3540	3541	3542	3543
6730	3544	3545	3546	3547	3548	3549	3550	3551
6740	3552	3553	3554	3555	3556	3557	3558	3559
6750	3560	3561	3562	3563	3564	3565	3566	3567
6760	3568	3569	3570	3571	3572	3573	3574	3575
6770	3576	3577	3578	3579	3580	3581	3582	3583

6000 to 6777 (Octal)	3072 to 3583 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
7000	3584	3585	3586	3587	3588	3589	3590	3591
7010	3592	3593	3594	3595	3596	3597	3598	3599
7020	3600	3601	3602	3603	3604	3605	3606	3607
7030	3608	3609	3610	3611	3612	3613	3614	3615
7040	3616	3617	3618	3619	3620	3621	3622	3623
7050	3624	3625	3626	3627	3628	3629	3630	3631
7060	3632	3633	3634	3635	3636	3637	3638	3639
7070	3640	3641	3642	3643	3644	3645	3646	3647
7100	3648	3649	3650	3651	3652	3653	3654	3655
7110	3656	3657	3658	3659	3660	3661	3662	3663
7120	3664	3665	3666	3667	3668	3669	3670	3671
7130	3672	3673	3674	3675	3676	3677	3678	3679
7140	3680	3681	3682	3683	3684	3685	3686	3687
7150	3688	3689	3690	3691	3692	3693	3694	3695
7160	3696	3697	3698	3699	3700	3701	3702	3703
7170	3704	3705	3706	3707	3708	3709	3710	3711
7200	3712	3713	3714	3715	3716	3717	3718	3719
7210	3720	3721	3722	3723	3724	3725	3726	3727
7220	3728	3729	3730	3731	3732	3733	3734	3735
7230	3736	3737	3738	3739	3740	3741	3742	3743
7240	3744	3745	3746	3747	3748	3749	3750	3751
7250	3752	3753	3754	3755	3756	3757	3758	3759
7260	3760	3761	3762	3763	3764	3765	3766	3767
7270	3768	3769	3770	3771	3772	3773	3774	3775
7300	3776	3777	3778	3779	3780	3781	3782	3783
7310	3784	3785	3786	3787	3788	3789	3790	3791
7320	3792	3793	3794	3795	3796	3797	3798	3799
7330	3800	3801	3802	3803	3804	3805	3806	3807
7340	3808	3809	3810	3811	3812	3813	3814	3815
7350	3816	3817	3818	3819	3820	3821	3822	3823
7360	3824	3825	3826	3827	3828	3829	3830	3831
7370	3832	3833	3834	3835	3836	3837	3838	3839

	0	1	2	3	4	5	6	7
7400	3840	3841	3842	3843	3844	3845	3846	3847
7410	3848	3849	3850	3851	3852	3853	3854	3855
7420	3856	3857	3858	3859	3860	3861	3862	3863
7430	3864	3865	3866	3867	3868	3869	3870	3871
7440	3872	3873	3874	3875	3876	3877	3878	3879
7450	3880	3881	3882	3883	3884	3885	3886	3887
7460	3888	3889	3890	3891	3892	3893	3894	3895
7470	3896	3897	3898	3899	3900	3901	3902	3903
7500	3904	3905	3906	3907	3908	3909	3910	3911
7510	3912	3913	3914	3915	3916	3917	3918	3919
7520	3920	3921	3922	3923	3924	3925	3926	3927
7530	3928	3929	3930	3931	3932	3933	3934	3935
7540	3936	3937	3938	3939	3940	3941	3942	3943
7550	3944	3945	3946	3947	3948	3949	3950	3951
7560	3952	3953	3954	3955	3956	3957	3958	3959
7570	3960	3961	3962	3963	3964	3965	3966	3967
7600	3968	3969	3970	3971	3972	3973	3974	3975
7610	3976	3977	3978	3979	3980	3981	3982	3983
7620	3984	3985	3986	3987	3988	3989	3990	3991
7630	3992	3993	3994	3995	3996	3997	3998	3999
7640	4000	4001	4002	4003	4004	4005	4006	4007
7650	4008	4009	4010	4011	4012	4013	4014	4015
7660	4016	4017	4018	4019	4020	4021	4022	4023
7670	4024	4025	4026	4027	4028	4029	4030	4031
7700	4032	4033	4034	4035	4036	4037	4038	4039
7710	4040	4041	4042	4043	4044	4045	4046	4047
7720	4048	4049	4050	4051	4052	4053	4054	4055
7730	4056	4057	4058	4059	4060	4061	4062	4063
7740	4064	4065	4066	4067	4068	4069	4070	4071
7750	4072	4073	4074	4075	4076	4077	4078	4079
7760	4080	4081	4082	4083	4084	4085	4086	4087
7770	4088	4089	4090	4091	4092	4093	4094	4095

7000 to 7777 (Octal)	3584 to 4095 (Decimal)

Appendix E. Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000	.000000	.100	.125000	.200	.250000	.300	.375000
.001	.001953	.101	.126953	.201	.251953	.301	.376953
.002	.003906	.102	.128906	.202	.253906	.302	.378906
.003	.005859	.103	.130859	.203	.255859	.303	.380859
.004	.007812	.104	.132812	.204	.257812	.304	.382812
.005	.009765	.105	.134765	.205	.259765	.305	.384765
.006	.011718	.106	.136718	.206	.261718	.306	.386718
.007	.013671	.107	.138671	.207	.263671	.307	.388671
.010	.015625	.110	.140625	.210	.265625	.310	.390625
.011	.017578	.111	.142578	.211	.267578	.311	.392578
.012	.019531	.112	.144531	.212	.269531	.312	.394531
.013	.021484	.113	.146484	.213	.271484	.313	.396484
.014	.023437	.114	.148437	.214	.273437	.314	.398437
.015	.025390	.115	.150390	.215	.275390	.315	.400390
.016	.027343	.116	.152343	.216	.277343	.316	.402343
.017	.029296	.117	.154296	.217	.279296	.317	.404296
.020	.031250	.120	.156250	.220	.281250	.320	.406250
.021	.033203	.121	.158203	.221	.283203	.321	.408203
.022	.035156	.122	.160156	.222	.285156	.322	.410156
.023	.037109	.123	.162109	.223	.287109	.323	.412109
.024	.039062	.124	.164062	.224	.289062	.324	.414062
.025	.041015	.125	.166015	.225	.291015	.325	.416015
.026	.042968	.126	.167968	.226	.292968	.326	.417968
.027	.044921	.127	.169921	.227	.294921	.327	.419921
.030	.046875	.130	.171875	.230	.296875	.330	.421875
.031	.048828	.131	.173828	.231	.298828	.331	.423828
.032	.050781	.132	.175781	.232	.300781	.332	.425781
.033	.052734	.133	.177734	.233	.302734	.333	.427734
.034	.054687	.134	.179687	.234	.304687	.334	.429687
.035	.056640	.135	.181640	.235	.306640	.335	.431640
.036	.058593	.136	.183593	.236	.308593	.336	.433593
.037	.060546	.137	.185546	.237	.310546	.337	.435546
.040	.062500	.140	.187500	.240	.312500	.340	.437500
.041	.064453	.141	.189453	.241	.314453	.341	.439453
.042	.066406	.142	.191406	.242	.316406	.342	.441406
.043	.068359	.143	.193359	.243	.318359	.343	.443359
.044	.070312	.144	.195312	.244	.320312	.344	.445312
.045	.072265	.145	.197265	.245	.322265	.345	.447265
.046	.074218	.146	.199218	.246	.324218	.346	.449218
.047	.076171	.147	.201171	.247	.326171	.347	.451171
.050	.078125	.150	.203125	.250	.328125	.350	.453125
.051	.080078	.151	.205078	.251	.330078	.351	.455078
.052	.082031	.152	.207031	.252	.332031	.352	.457031
.053	.083984	.153	.208984	.253	.333984	.353	.458984
.054	.085937	.154	.210937	.254	.335937	.354	.460937
.055	.087890	.155	.212890	.255	.337890	.355	.462890
.056	.089843	.156	.214843	.256	.339843	.356	.464843
.057	.091796	.157	.216796	.257	.341796	.357	.466796
.060	.093750	.160	.218750	.260	.343750	.360	.468750
.061	.095703	.161	.220703	.261	.345703	.361	.470703
.062	.097656	.162	.222656	.262	.347656	.362	.472656
.063	.099609	.163	.224609	.263	.349609	.363	.474609
.064	.101562	.164	.226562	.264	.351562	.364	.476562
.065	.103515	.165	.228515	.265	.353515	.365	.478515
.066	.105468	.166	.230468	.266	.355468	.366	.480468
.067	.107421	.167	.232421	.267	.357421	.367	.482421
.070	.109375	.170	.234375	.270	.359375	.370	.484375
.071	.111328	.171	.236328	.271	.361328	.371	.486328
.072	.113281	.172	.238281	.272	.363281	.372	.488281
.073	.115234	.173	.240234	.273	.365234	.373	.490234
.074	.117187	.174	.242187	.274	.367187	.374	.492187
.075	.119140	.175	.244140	.275	.369140	.375	.494140
.076	.121093	.176	.246093	.276	.371093	.376	.496093
.077	.123046	.177	.248046	.277	.373046	.377	.498046

Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000000	.000000	.000100	.000244	.000200	.000488	.000300	.000732
.000001	.000003	.000101	.000247	.000201	.000492	.000301	.000736
.000002	.000007	.000102	.000251	.000202	.000495	.000302	.000740
.000003	.000011	.000103	.000255	.000203	.000499	.000303	.000743
.000004	.000015	.000104	.000259	.000204	.000503	.000304	.000747
.000005	.000019	.000105	.000263	.000205	.000507	.000305	.000751
.000006	.000022	.000106	.000267	.000206	.000511	.000306	.000755
.000007	.000026	.000107	.000270	.000207	.000514	.000307	.000759
.000010	.000030	.000110	.000274	.000210	.000518	.000310	.000762
.000011	.000034	.000111	.000278	.000211	.000522	.000311	.000766
.000012	.000038	.000112	.000282	.000212	.000526	.000312	.000770
.000013	.000041	.000113	.000286	.000213	.000530	.000313	.000774
.000014	.000045	.000114	.000289	.000214	.000534	.000314	.000778
.000015	.000049	.000115	.000293	.000215	.000537	.000315	.000782
.000016	.000053	.000116	.000297	.000216	.000541	.000316	.000785
.000017	.000057	.000117	.000301	.000217	.000545	.000317	.000789
.000020	.000061	.000120	.000305	.000220	.000549	.000320	.000793
.000021	.000064	.000121	.000308	.000221	.000553	.000321	.000797
.000022	.000068	.000122	.000312	.000222	.000556	.000322	.000801
.000023	.000072	.000123	.000316	.000223	.000560	.000323	.000805
.000024	.000076	.000124	.000320	.000224	.000564	.000324	.000808
.000025	.000080	.000125	.000324	.000225	.000568	.000325	.000812
.000026	.000083	.000126	.000328	.000226	.000572	.000326	.000816
.000027	.000087	.000127	.000331	.000227	.000576	.000327	.000820
.000030	.000091	.000130	.000335	.000230	.000579	.000330	.000823
.000031	.000095	.000131	.000339	.000231	.000583	.000331	.000827
.000032	.000099	.000132	.000343	.000232	.000587	.000332	.000831
.000033	.000102	.000133	.000347	.000233	.000591	.000333	.000835
.000034	.000106	.000134	.000350	.000234	.000595	.000334	.000839
.000035	.000110	.000135	.000354	.000235	.000598	.000335	.000843
.000036	.000114	.000136	.000358	.000236	.000602	.000336	.000846
.000037	.000118	.000137	.000362	.000237	.000606	.000337	.000850
.000040	.000122	.000140	.000366	.000240	.000610	.000340	.000854
.000041	.000125	.000141	.000370	.000241	.000614	.000341	.000858
.000042	.000129	.000142	.000373	.000242	.000617	.000342	.000862
.000043	.000133	.000143	.000377	.000243	.000621	.000343	.000865
.000044	.000137	.000144	.000381	.000244	.000625	.000344	.000869
.000045	.000141	.000145	.000385	.000245	.000629	.000345	.000873
.000046	.000144	.000146	.000389	.000246	.000633	.000346	.000877
.000047	.000148	.000147	.000392	.000247	.000637	.000347	.000881
.000050	.000152	.000150	.000396	.000250	.000640	.000350	.000885
.000051	.000156	.000151	.000400	.000251	.000644	.000351	.000888
.000052	.000160	.000152	.000404	.000252	.000648	.000352	.000892
.000053	.000164	.000153	.000408	.000253	.000652	.000353	.000896
.000054	.000167	.000154	.000411	.000254	.000656	.000354	.000900
.000055	.000171	.000155	.000415	.000255	.000659	.000355	.000904
.000056	.000175	.000156	.000419	.000256	.000663	.000356	.000907
.000057	.000179	.000157	.000423	.000257	.000667	.000357	.000911
.000060	.000183	.000160	.000427	.000260	.000671	.000360	.000915
.000061	.000186	.000161	.000431	.000261	.000675	.000361	.000919
.000062	.000190	.000162	.000434	.000262	.000679	.000362	.000923
.000063	.000194	.000163	.000438	.000263	.000682	.000363	.000926
.000064	.000198	.000164	.000442	.000264	.000686	.000364	.000930
.000065	.000202	.000165	.000446	.000265	.000690	.000365	.000934
.000066	.000205	.000166	.000450	.000266	.000694	.000366	.000938
.000067	.000209	.000167	.000453	.000267	.000698	.000367	.000942
.000070	.000213	.000170	.000457	.000270	.000701	.000370	.000946
.000071	.000217	.000171	.000461	.000271	.000705	.000371	.000949
.000072	.000221	.000172	.000465	.000272	.000709	.000372	.000953
.000073	.000225	.000173	.000469	.000273	.000713	.000373	.000957
.000074	.000228	.000174	.000473	.000274	.000717	.000374	.000961
.000075	.000232	.000175	.000476	.000275	.000720	.000375	.000965
.000076	.000236	.000176	.000480	.000276	.000724	.000376	.000968
.000077	.000240	.000177	.000484	.000277	.000728	.000377	.000972

Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000400	.000976	.000500	.001220	.000600	.001464	.000700	.001708
.000401	.000980	.000501	.001224	.000601	.001468	.000701	.001712
.000402	.000984	.000502	.001228	.000602	.001472	.000702	.001716
.000403	.000988	.000503	.001232	.000603	.001476	.000703	.001720
.000404	.000991	.000504	.001235	.000604	.001480	.000704	.001724
.000405	.000995	.000505	.001239	.000605	.001483	.000705	.001728
.000406	.000999	.000506	.001243	.000606	.001487	.000706	.001731
.000407	.001003	.000507	.001247	.000607	.001491	.000707	.001735
.000410	.001007	.000510	.001251	.000610	.001495	.000710	.001739
.000411	.001010	.000511	.001255	.000611	.001499	.000711	.001743
.000412	.001014	.000512	.001258	.000612	.001502	.000712	.001747
.000413	.001018	.000513	.001262	.000613	.001506	.000713	.001750
.000414	.001022	.000514	.001266	.000614	.001510	.000714	.001754
.000415	.001026	.000515	.001270	.000615	.001514	.000715	.001758
.000416	.001029	.000516	.001274	.000616	.001518	.000716	.001762
.000417	.001033	.000517	.001277	.000617	.001522	.000717	.001766
.000420	.001037	.000520	.001281	.000620	.001525	.000720	.001770
.000421	.001041	.000521	.001285	.000621	.001529	.000721	.001773
.000422	.001045	.000522	.001289	.000622	.001533	.000722	.001777
.000423	.001049	.000523	.001293	.000623	.001537	.000723	.001781
.000424	.001052	.000524	.001296	.000624	.001541	.000724	.001785
.000425	.001056	.000525	.001300	.000625	.001544	.000725	.001789
.000426	.001060	.000526	.001304	.000626	.001548	.000726	.001792
.000427	.001064	.000527	.001308	.000627	.001552	.000727	.001796
.000430	.001068	.000530	.001312	.000630	.001556	.000730	.001800
.000431	.001071	.000531	.001316	.000631	.001560	.000731	.001804
.000432	.001075	.000532	.001319	.000632	.001564	.000732	.001808
.000433	.001079	.000533	.001323	.000633	.001567	.000733	.001811
.000434	.001083	.000534	.001327	.000634	.001571	.000734	.001815
.000435	.001087	.000535	.001331	.000635	.001575	.000735	.001819
.000436	.001091	.000536	.001335	.000636	.001579	.000736	.001823
.000437	.001094	.000537	.001338	.000637	.001583	.000737	.001827
.000440	.001098	.000540	.001342	.000640	.001586	.000740	.001831
.000441	.001102	.000541	.001346	.000641	.001590	.000741	.001834
.000442	.001106	.000542	.001350	.000642	.001594	.000742	.001838
.000443	.001110	.000543	.001354	.000643	.001598	.000743	.001842
.000444	.001113	.000544	.001358	.000644	.001602	.000744	.001846
.000445	.001117	.000545	.001361	.000645	.001605	.000745	.001850
.000446	.001121	.000546	.001365	.000646	.001609	.000746	.001853
.000447	.001125	.000547	.001369	.000647	.001613	.000747	.001857
.000450	.001129	.000550	.001373	.000650	.001617	.000750	.001861
.000451	.001132	.000551	.001377	.000651	.001621	.000751	.001865
.000452	.001136	.000552	.001380	.000652	.001625	.000752	.001869
.000453	.001140	.000553	.001384	.000653	.001628	.000753	.001873
.000454	.001144	.000554	.001388	.000654	.001632	.000754	.001876
.000455	.001148	.000555	.001392	.000655	.001636	.000755	.001880
.000456	.001152	.000556	.001396	.000656	.001640	.000756	.001884
.000457	.001155	.000557	.001399	.000657	.001644	.000757	.001888
.000460	.001159	.000560	.001403	.000660	.001647	.000760	.001892
.000461	.001163	.000561	.001407	.000661	.001651	.000761	.001895
.000462	.001167	.000562	.001411	.000662	.001655	.000762	.001899
.000463	.001171	.000563	.001415	.000663	.001659	.000763	.001903
.000464	.001174	.000564	.001419	.000664	.001663	.000764	.001907
.000465	.001178	.000565	.001422	.000665	.001667	.000765	.001911
.000466	.001182	.000566	.001426	.000666	.001670	.000766	.001914
.000467	.001186	.000567	.001430	.000667	.001674	.000767	.001918
.000470	.001190	.000570	.001434	.000670	.001678	.000770	.001922
.000471	.001194	.000571	.001438	.000671	.001682	.000771	.001926
.000472	.001197	.000572	.001441	.000672	.001686	.000772	.001930
.000473	.001201	.000573	.001445	.000673	.001689	.000773	.001934
.000474	.001205	.000574	.001449	.000674	.001693	.000774	.001937
.000475	.001209	.000575	.001453	.000675	.001697	.000775	.001941
.000476	.001213	.000576	.001457	.000676	.001701	.000776	.001945
.000477	.001216	.000577	.001461	.000677	.001705	.000777	.001949

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