

PAGE NO.	SH	TITLE	PART NO	EC NO.	FEATURE B/M OR B/MS
** LOGIC TYPE SYSTEM DIAGRAMS 0					
QM111		INVALID OPS	V000	5364792	255449
QM112		INVALID OPS	V000	5364920	255449
QN111		INVALID OP GROUP A-B-C-E	VC03	5379142	282229 .W. 5379137
QPG10		2ND LVL I FETCH FOR VFL	V000	5364794	255449
QP100		COMPARE LOGICAL	V000	5364795	255449
QP102		COMPARE LOGICAL	V000	5364904	255449
QP200		EDIT & MARK	VC03	5379160	282229 .W. 5379137
QP202		EDIT & MARK LEFT SOURCE DIG	V000	5364797	255449
QP203		EDIT & MARK RL SOURCE DIG	V000	5364798	255449
QP204		EDIT & MARK RL SOURCE DIG	V000	5364799	255449
QP205		EDIT & MARK STR FETCH PTRN	V000	5364800	255449
QP206		EDIT & MARK SET COND REG GE	V000	5364801	255449
QP800		LOGIC MOVE INST ADR TE	V000	5364802	255449
QP810		LOGIC MOVE INST MAIN L	V000	5364803	255449
QP820		LOGIC MOVE INST DV.LAP	V000	5364804	255449
QP830		LOGIC MOVE INST END RD	V000	5364805	255449
QP900		TRANSLATE TRANS TEST	V000	5364806	255449
QS010		DEC ARITH 2ND LEVEL I/F	V000	5364807	255449
QS110		DEC AD AP SUB AP FIRST	V000	5469499	258430
QS112		DEC ADD SUBTRACT OP2 A	V000	5364809	256498
QS114		DEC AD AP SUB SP ADD SU	V000	5469500	258430
QS116		DEC ADD AP SUBTRACT SPG	V000	5364811	255449
QS118		DEC ADD AP SUBTRACT SPG	V000	5364812	256907
QS120		DEC ADD AP SUBTRACT SPG	V000	5449079	258430
QS200		COMP DEC CP COMPAR	V000	5364814	255449
QS202		COMP DEC COMP 1ST WD OP	V000	5364815	257390
QS300		DIV DCML DP DIVIDEND AS	V000	5364816	255449
QS302		DIVIDE DEC DP SIGN INSE	V000	5364817	255449
QS304		DIVIDE DECIMAL DP DOUB	V000	5364818	255449
QS306		DIVIDE DECIMAL DP QUOT	V000	5364819	255449
QS308		DIVIDE DECIMAL DP REMAI	V000	5364820	255449
QS400		MULT DIV DEC MP DP OPND	V000	5364821	255449
QS402		MULT DIV DEC MP D DBL IN	V000	5364822	255449
QS404		MULT DEC SING DBL WD MP	V000	5364823	255449
QS406		MULTIPLY DECIMAL	V000	5364824	255449
QS500		PACK MOVE WITH OFFSET	V000	5364825	255449
QS502		PACK MOVE WITH OFFSET	V000	5364826	255449
QS600		UNPACK NON OVERLAPPED	V000	5364827	255449
QS601		UNPACK OP1 STR OP2 FETC	V000	5364828	255449
QS602		UNPACK OVERLAPPED FIELD	V000	5364829	255449
QS705		ZERO AND ADD	V000	5364905	255449
QS706		ZERO AND ADD	V000	5364906	255449

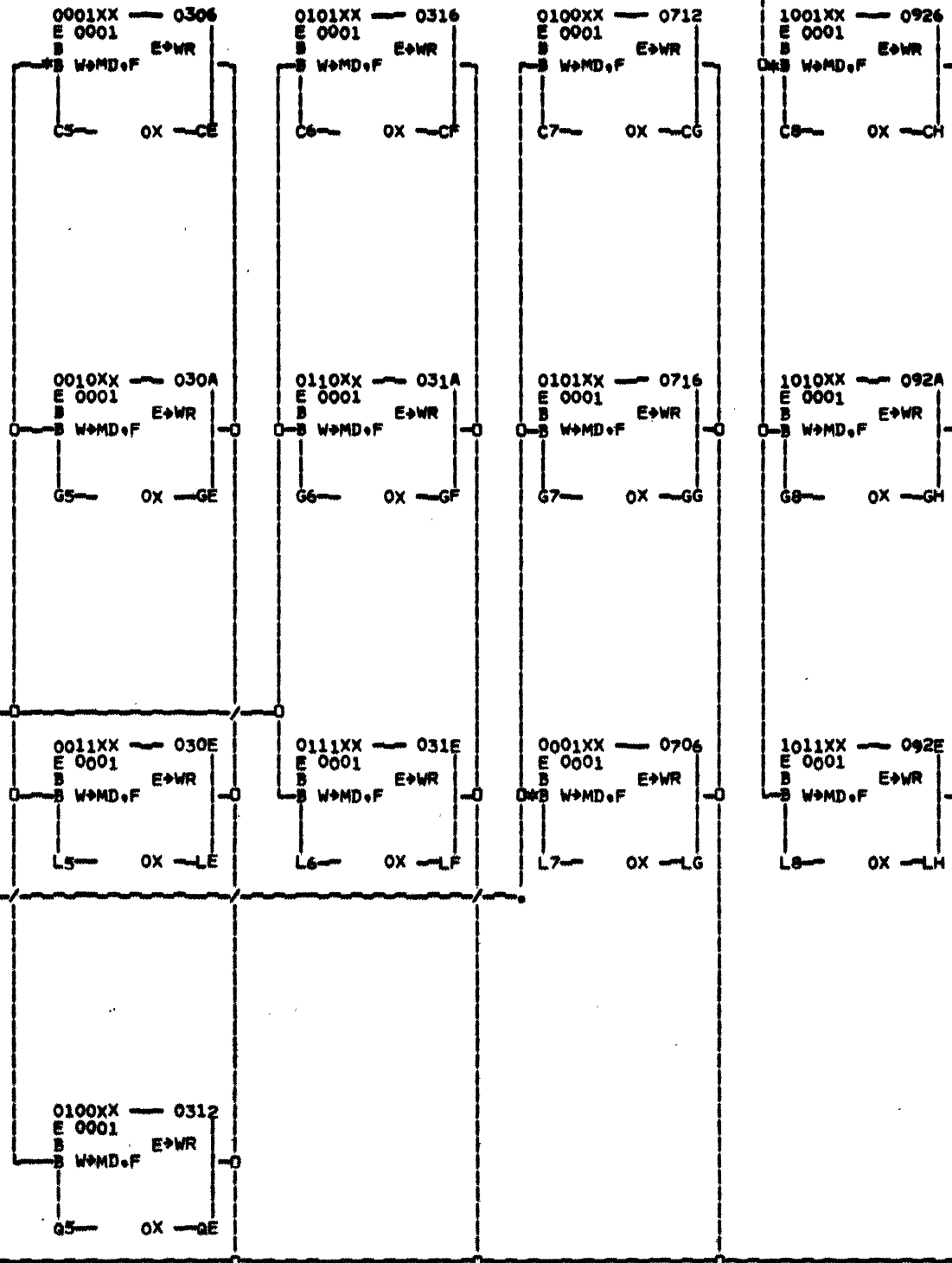
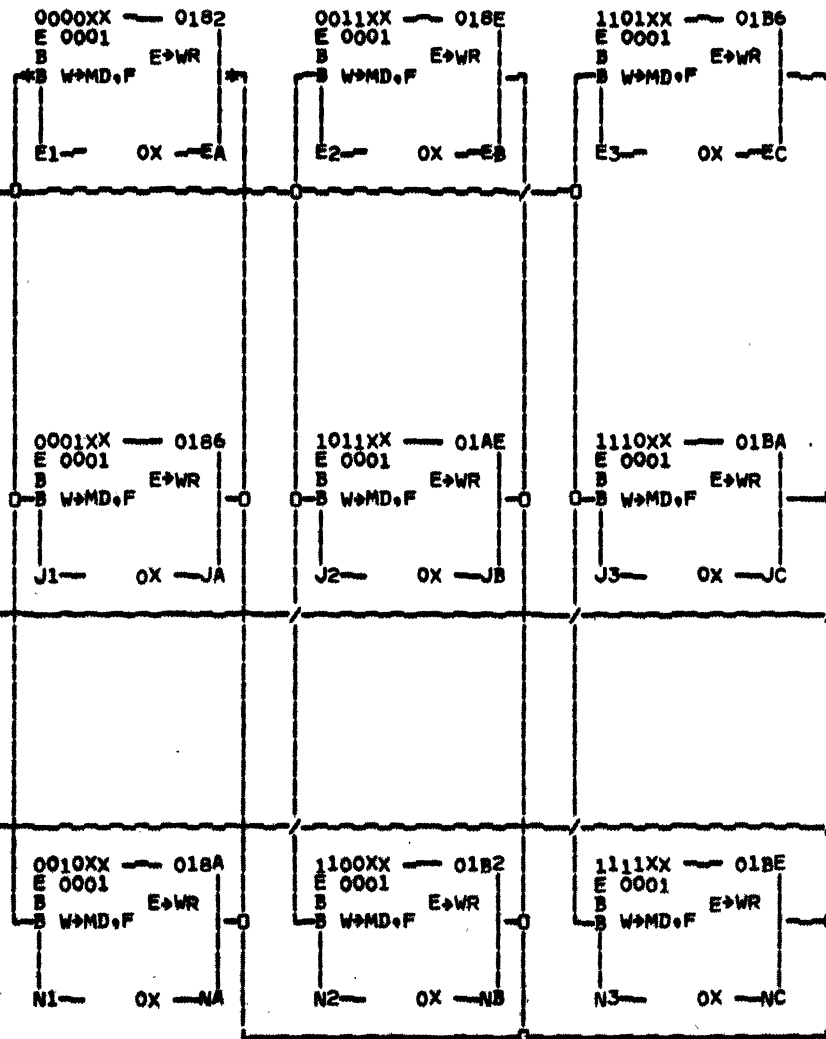
Dec 72

QJ011.LCE
 (1001XX)
 (1010XX)
 (1011XX)
 51

QA110.GBE
 (0000XX)
 (0001XX)
 (0010XX)
 (0011XX)
 (1011XX)
 (1100XX)
 (1101XX)
 (1110XX)
 (1111XX)
 RR CONTROL

QG010.AFE
 (0001XX)
 (0010XX)
 (0011XX)
 (0100XX)
 (0101XX)
 (0110XX)
 (0111XX)
 RX FLOAT PT

QJ011.AAE
 (0001XX)
 (0100XX)
 (0101XX)
 RS



0T310 EAE
 (OX)
 PROGRAM TRAP

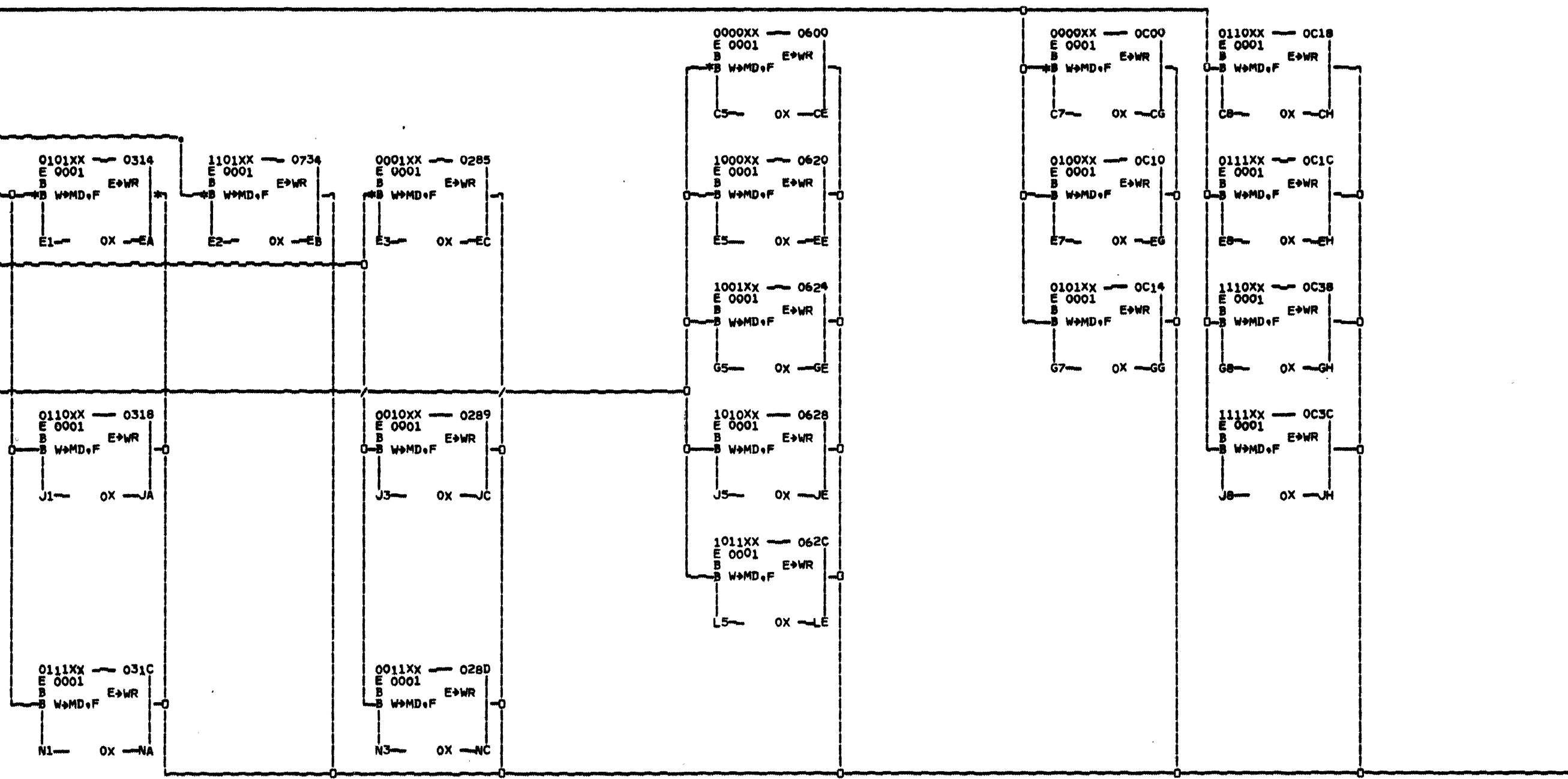
Q5010.NIE
 (0000XX)
 (0100XX)
 (0101XX)
 (0110XX)
 (0111XX)
 (1110XX)
 (1111XX)
 SS DECIMAL

QA110.CGE
 (1101XX)
 RX CONTROL

Q6010.JEE
 (0101XX)
 (0110XX)
 (0111XX)
 RR FLOAT PT

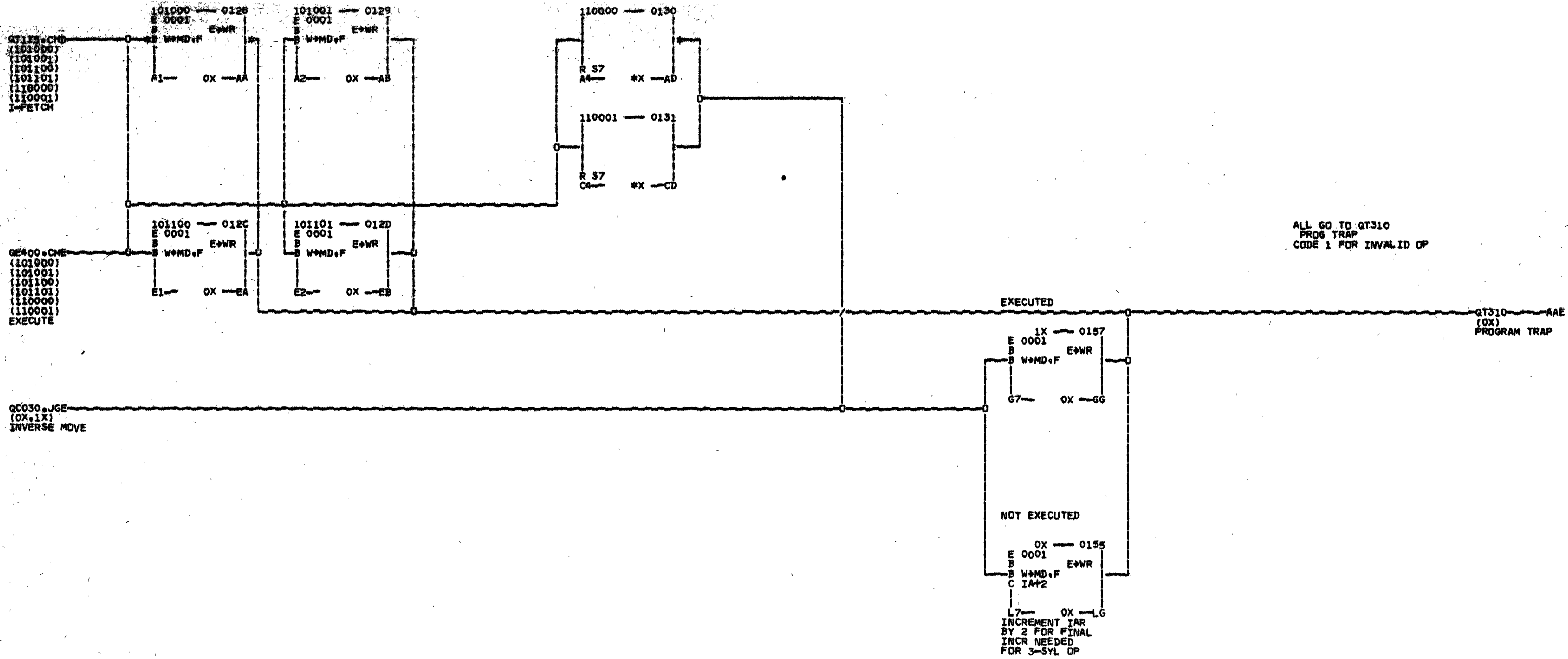
QA111.CGE
 (0001XX)
 (0010XX)
 (0011XX)
 RX FIXED PT

QP010.EHE
 (0000XX)
 (1000XX)
 (1001XX)
 (1010XX)
 (1011XX)
 SS LOGICAL



QT310 EAE
 (OX)
 PROGRAM TRAP

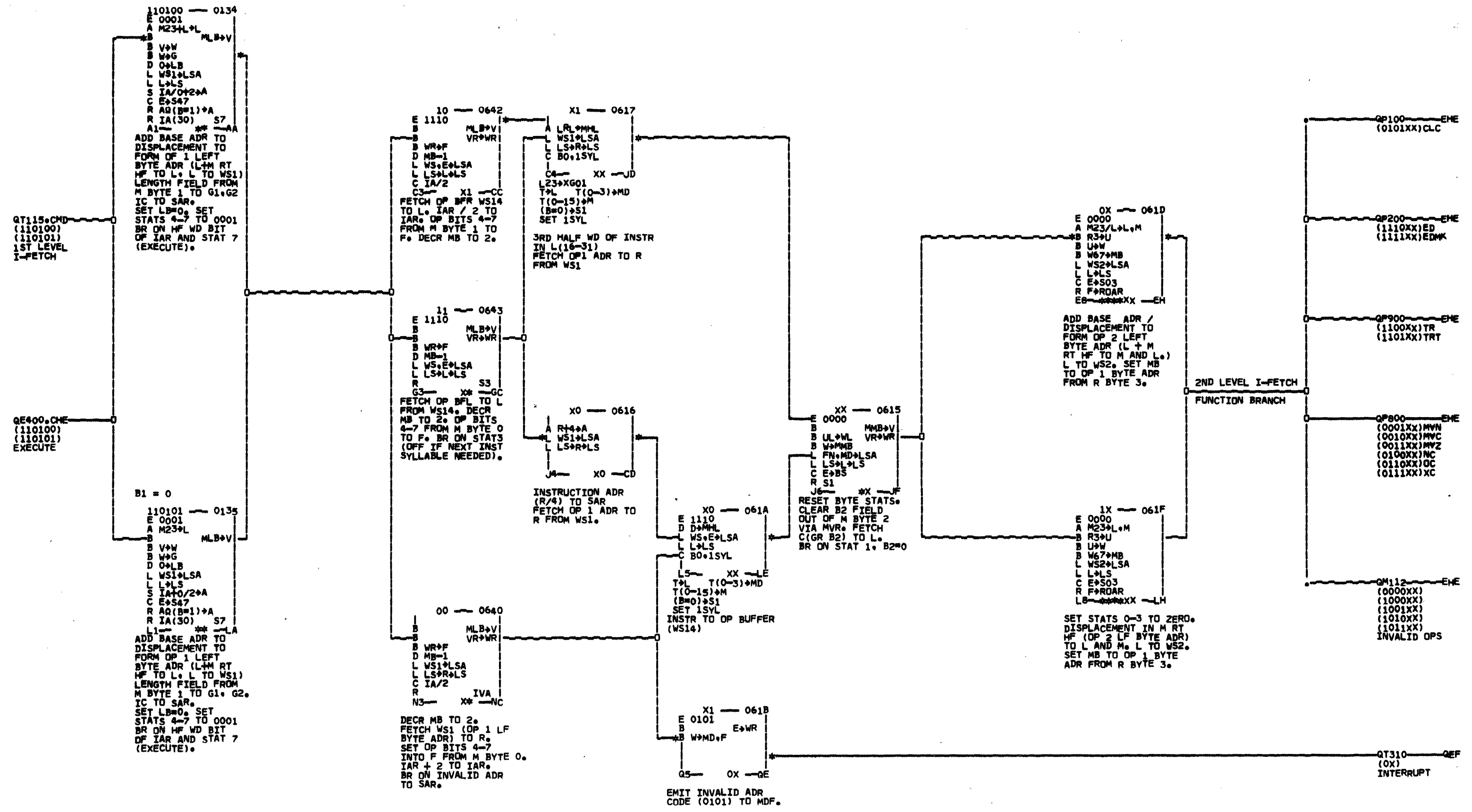
211-1-1

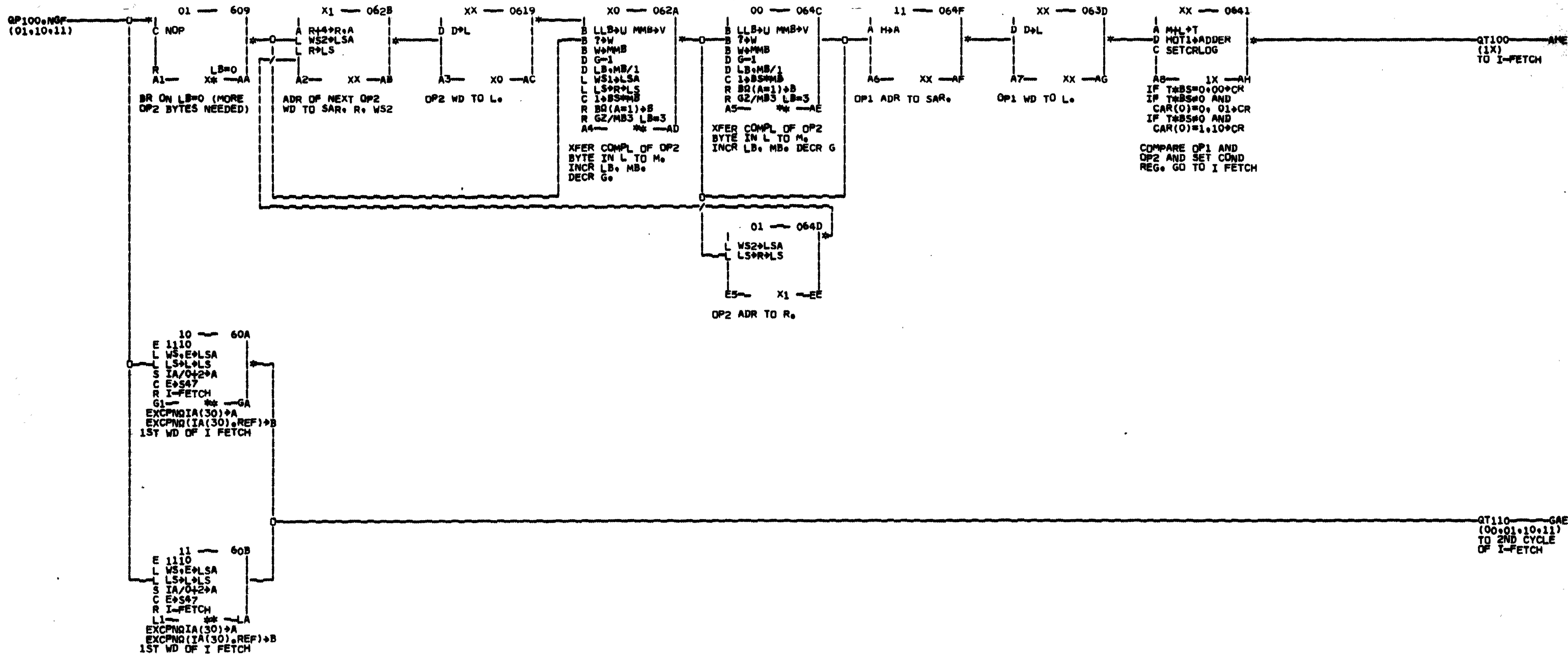


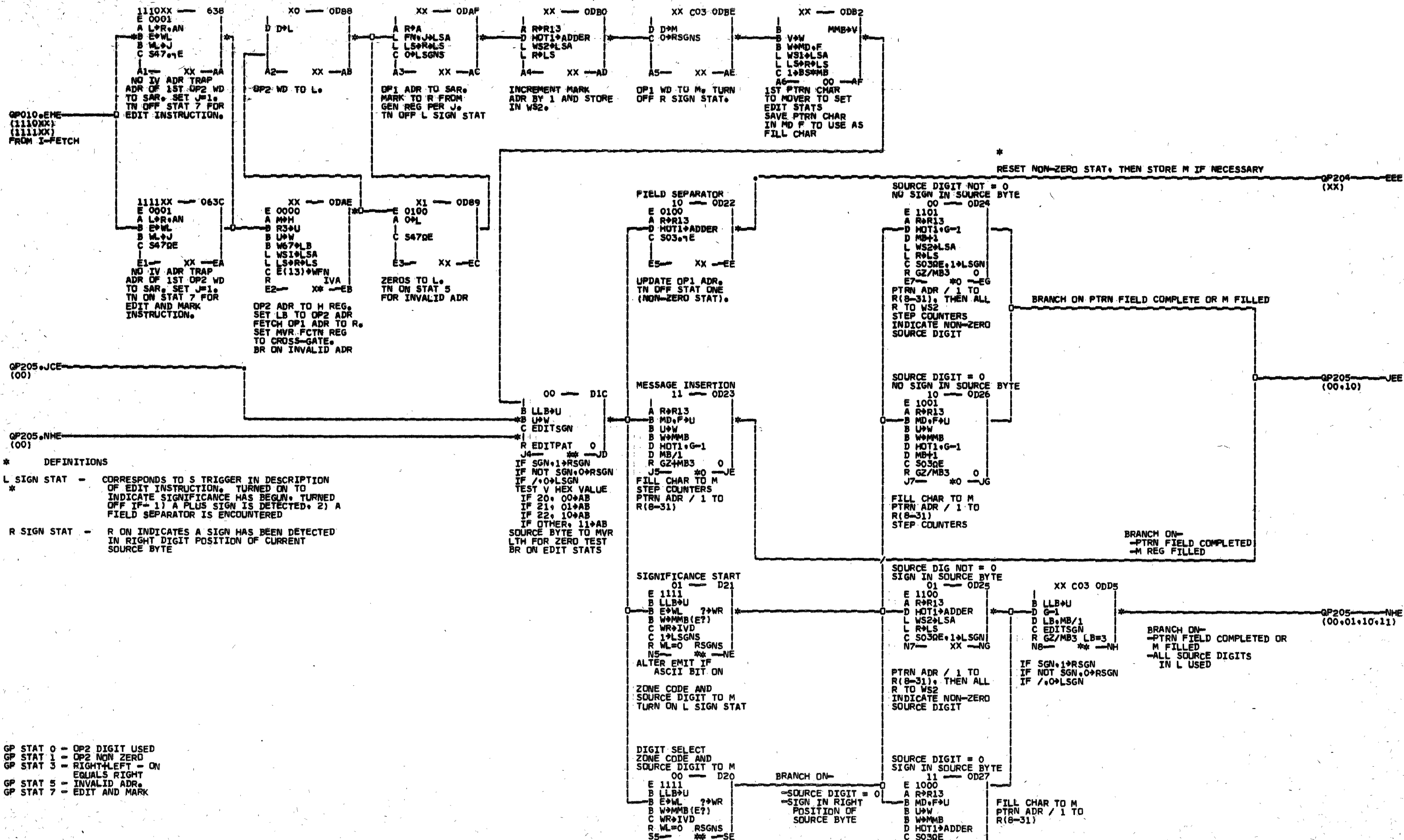
ALL GO TO GT310
 PROG TRAP
 CODE 1 FOR INVALID OP

1-11-20

01010





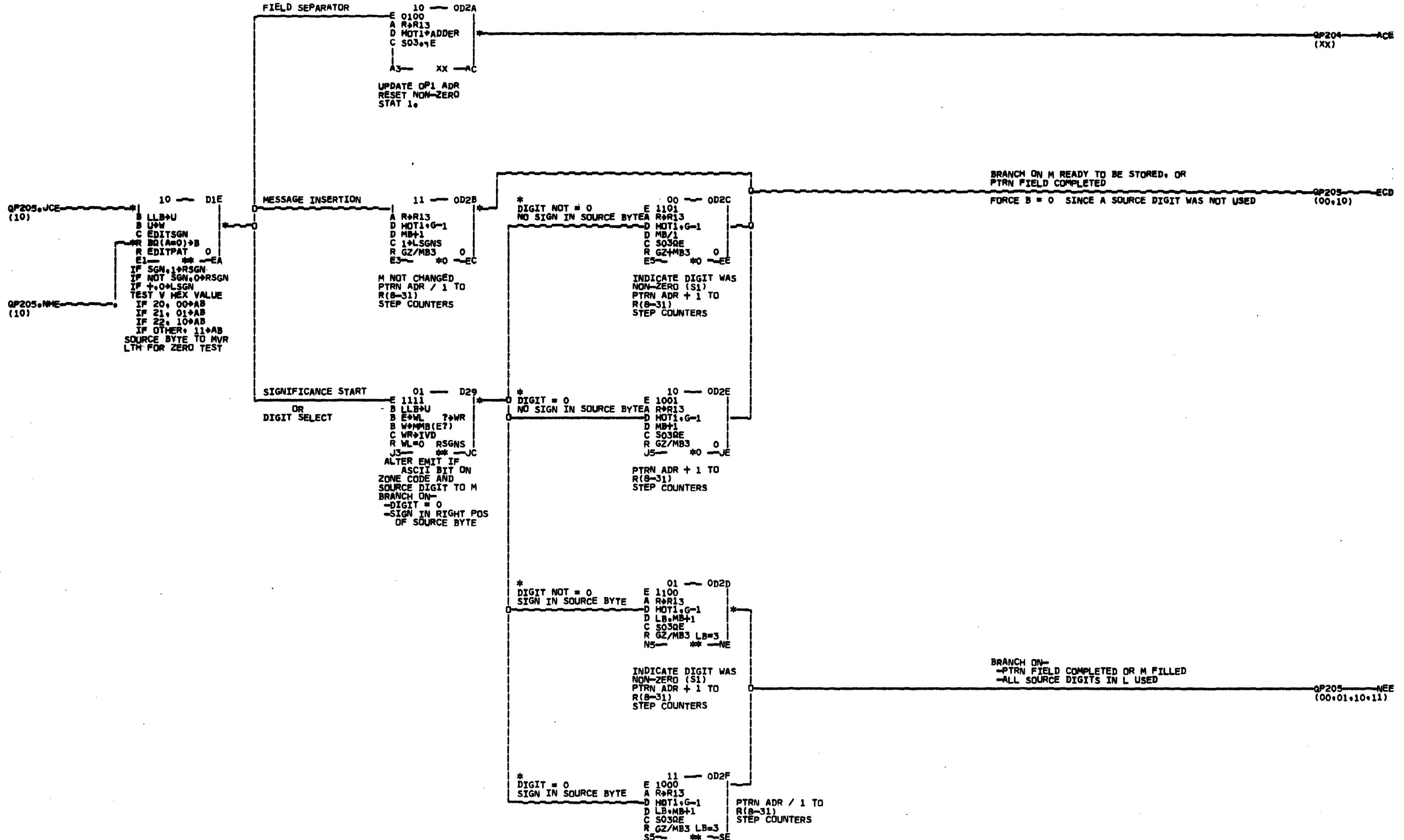


* DEFINITIONS

L SIGN STAT - CORRESPONDS TO S TRIGGER IN DESCRIPTION OF EDIT INSTRUCTION. TURNED ON TO INDICATE SIGNIFICANCE HAS BEGUN. TURNED OFF IF - 1) A PLUS SIGN IS DETECTED. 2) A FIELD SEPARATOR IS ENCOUNTERED

R SIGN STAT - R ON INDICATES A SIGN HAS BEEN DETECTED IN RIGHT DIGIT POSITION OF CURRENT SOURCE BYTE

GP STAT 0 - OP2 DIGIT USED
 GP STAT 1 - OP2 NON ZERO
 GP STAT 3 - RIGHT+LEFT - ON
 EQUALS RIGHT
 GP STAT 5 - INVALID ADR.
 GP STAT 7 - EDIT AND MARK



QP205.JCE (10)

10 D1E

B LLB+U
 B U+W
 C EDITSGN
 R BQ(A=0)+B
 R EDITPAT
 E1 ** EA
 IF SGN,1+RSGN
 IF NOT SGN,0+RSGN
 IF +,0+LSGN
 TEST V HEX VALUE
 IF 20, 00+AB
 IF 21, 01+AB
 IF 22, 10+AB
 IF OTHER, 11+AB
 SOURCE BYTE TO MVR
 LTH FOR ZERO TEST

QP205.NHE (10)

NONO

FIELD SEPARATOR 10 OD32 TURN OFF NON-ZERO STAT. THEN STORE M IF NECESSARY GP204 ACD (XX)

```

E 1001
A R→R13
D MDT1→ADDER
C E→S03
A3 XX AC
  
```

PTRN ADR+1 TO R(8-31).
 TN ON STAT0
 (DIGIT USED).
 RESET STAT1
 (NON-ZERO).
 TN ON STAT3
 (R/L TO RIGHT).

MESSAGE INSERTION 11 OD33 BR ON PTRN FIELD COMPLETED OR M FILLED GP205 ECD (00.10)

```

E 0001
A R→R13
B MD→F→U
B U→W
B W→MMB
D MDT1→G-1
D MB→1
C S03OE
R GZ/MB3 0
E3 →#0 EC
  
```

FILL CHAR TO M
 PTRN ADR / 1 TO R(8-31)
 STEP COUNTERS

SIGNIFICANCE START 01 OD31 DIGIT NOT = 0 0X OD8C BRANCH ON- PTRN FIELD COMPLETED OR M FILLED GP205 JEE (00.01.10.11)

```

E 1111
B LLB→U
B E→WL UR→WR
B W→MMB(E?)
C 1→LSGNS
R WR=0
J3 →#X JC
  
```

ALTER EMIT IF
 ASCII BIT ON
 ZONE CODE AND SOURCE
 DIGIT TO M
 TURN ON L SIGN STAT
 BR ON DIGIT = 0

```

E 0100
A R→R13
D MDT1→G-1
D LB→MB/1
L WS2→LSA
L R→LS
C S03OE.1→LSGN
R GZ/MB3 LB=3
J5 →#E
  
```

TURN ON NON-ZERO STAT
 PTRN ADR / 1 TO
 R(8-31). THEN R
 TO WS2
 STEP COUNTERS

BRANCH ON-
 -PTRN FIELD COMPLETED OR M FILLED
 -NEXT SOURCE WORD REQUIRED

DIGIT SELECT 00 OD30 *DIGIT = 0 1X OD8E

```

E 1111
B LLB→U
B E→WL UR→WR
B W→MMB(E?)
R WR=0
N3 →#X NC
  
```

ALTER EMIT IF
 ASCII BIT ON
 ZONE CODE AND SOURCE
 DIGIT TO M
 BR ON DIGIT = 0

```

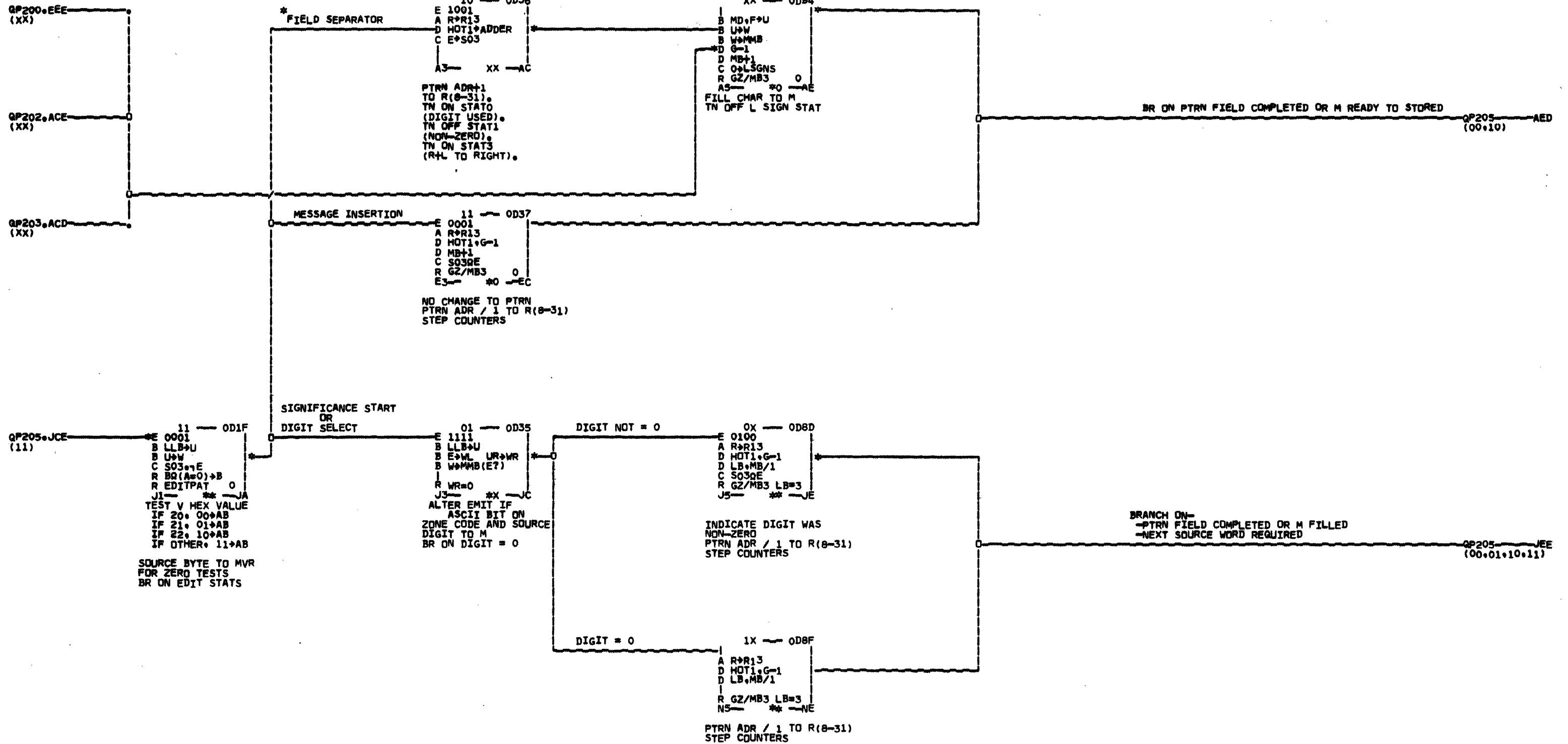
A R→R13
B MD→F→U
B U→W
B W→MMB
D MDT1→G-1
D LB→MB/1
R GZ/MB3 LB=3
NS →#E NE
  
```

FILL CHAR TO M
 PTRN ADR / 1 TO
 R(8-31)
 STEP COUNTER

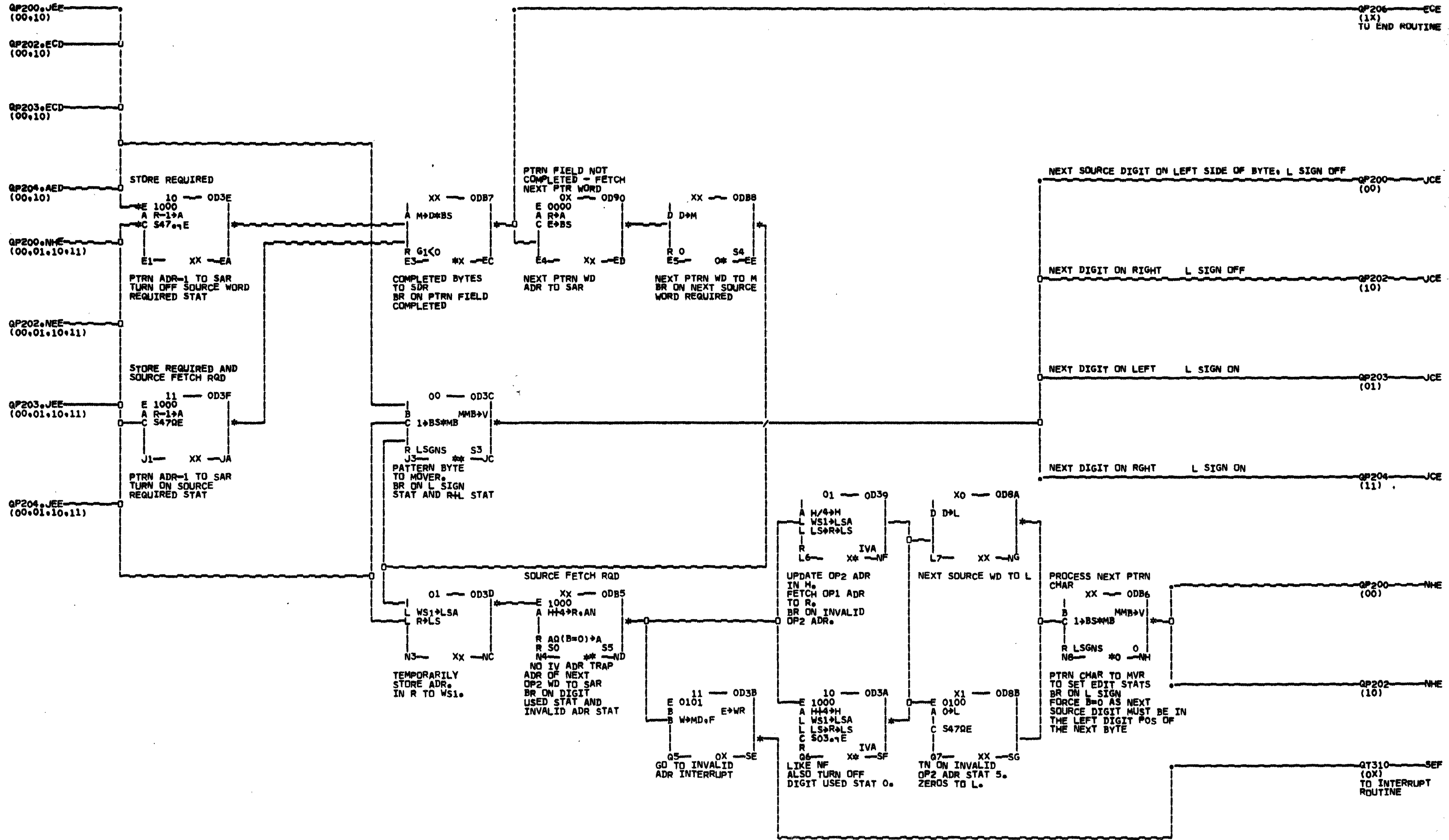
```

GP205.JCE (01)
E 0001
B LLB→U
B U→W
C S03→E
R EDITPAT 0
J1 →# JA
TEST V HEX VALUE
IF 20. 00→AB
IF 21. 01→AB
IF 22. 10→AB
IF OTHER. 11→AB
SOURCE BYTE TO MVR
FOR ZERO TEST
BR ON EDIT STATS
  
```

UNION



00000



254760

1X — OD92
 L WS2→LSA
 LS→R→LS
 R AQ(B=0)→A
 R SO S5
 A1 — ** —AA

FETCH MARK ADR
 TO R FROM WS2.
 BR ON DIGIT USED
 STAT 0 AND
 INVALID ADR
 STAT 5.

SOURCE WAS GTR
 THAN ZERO

01 — OD45
 E 0010
 C E(23)→CR
 R E2 X* —EB
 S7
 2 TO COND REG
 BR ON EDIT AND MARK

EDIT

X0 — OD94
 E 1110
 L WS→LSA
 LS→L→LS
 S IA/O+2→A
 C E→S47
 R I→FETCH
 E4 — ** —ED
 EXCPNQA(30)→A
 EXCPNQA(30),REF)→B
 DO NOT CHANGE GR1
 PREPARE FOR SPECIAL
 ENTRY TO I-FETCH

QT110 — EDD
 (00,01,10,11)
 TO 2ND CYCLE
 OF I-FETCH

SOURCE WAS ZERO

10 — OD46
 E 0000
 C E(23)→CR
 R J2 X* —JB
 S7
 0 TO COND REG
 BR ON EDIT AND MARK

EDIT AND MARK

X1 — OD95
 A R-1→L13
 L FN→LSA
 L L→LS
 J4 — 1X —JD

QT100 — JDD
 (1X)
 TO I-FETCH

01 — OD41
 L FN→LSA
 LS→L→LS
 R AQ(B=0)→A
 R LSGNS S1
 J1 — ** —JA

GEN REG PER J TO
 L REG. BR ON L
 SIGN STAT AND
 NON-ZERO STAT.

SOURCE WAS LESS
 THAN ZERO

11 — OD47
 E 0001
 C E(23)→CR
 R N2 X* —NB
 S7
 1 TO COND REG
 BR ON EDIT AND MARK

10 — OD42
 L FN→LSA
 LS→L→LS
 R AQ(B=0)→A
 R LSGNS S1
 N1 — ** —NA

LIKE ABOVE.

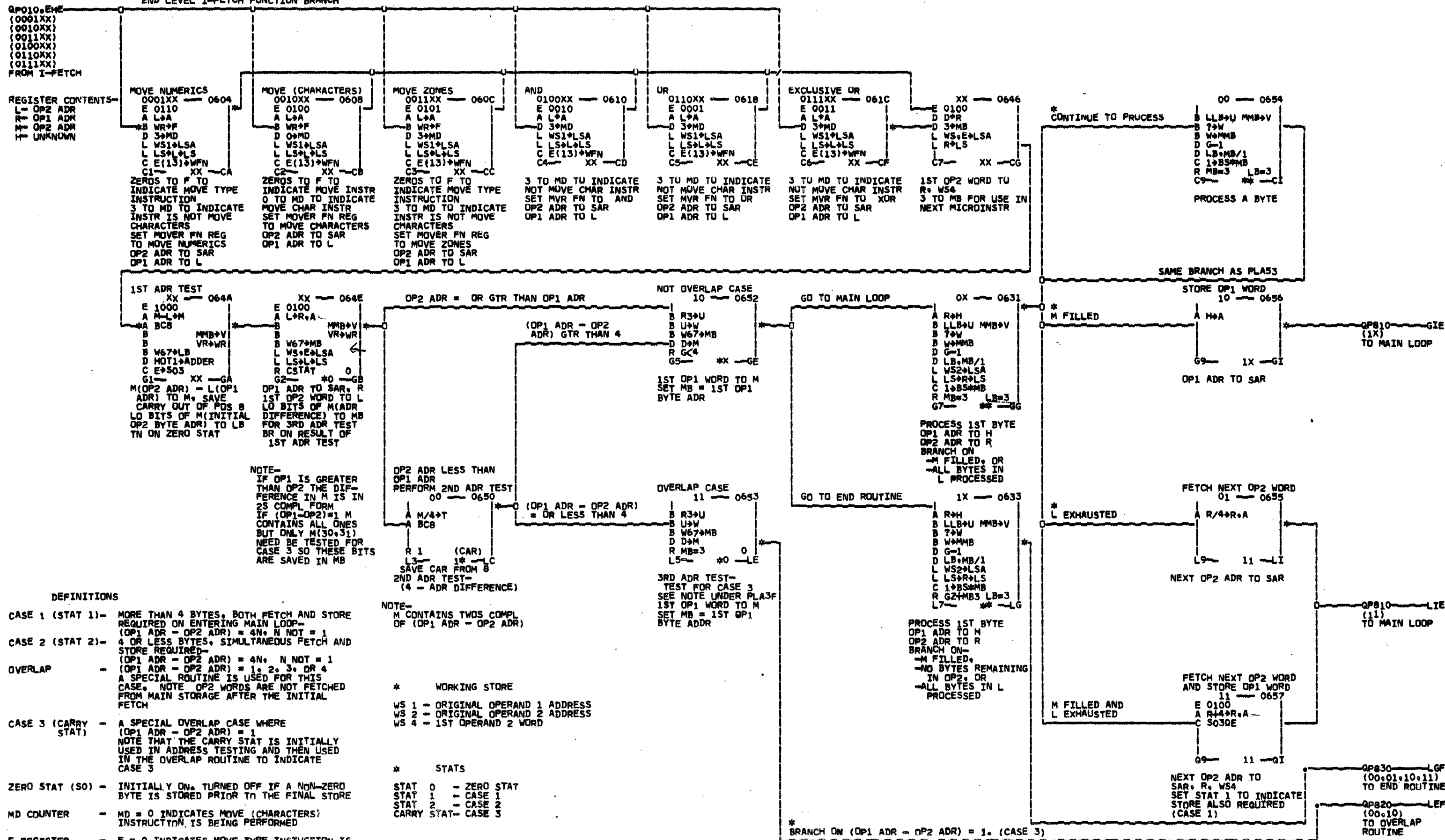
GO TO INVALID
 ADR INTERRUPT

11 — OD43
 E 0101
 B W→MD,F
 E→WR
 S1 — OX —SA

QT310 — SAD
 (OX)
 TO INTERRUPT
 ROUTINE

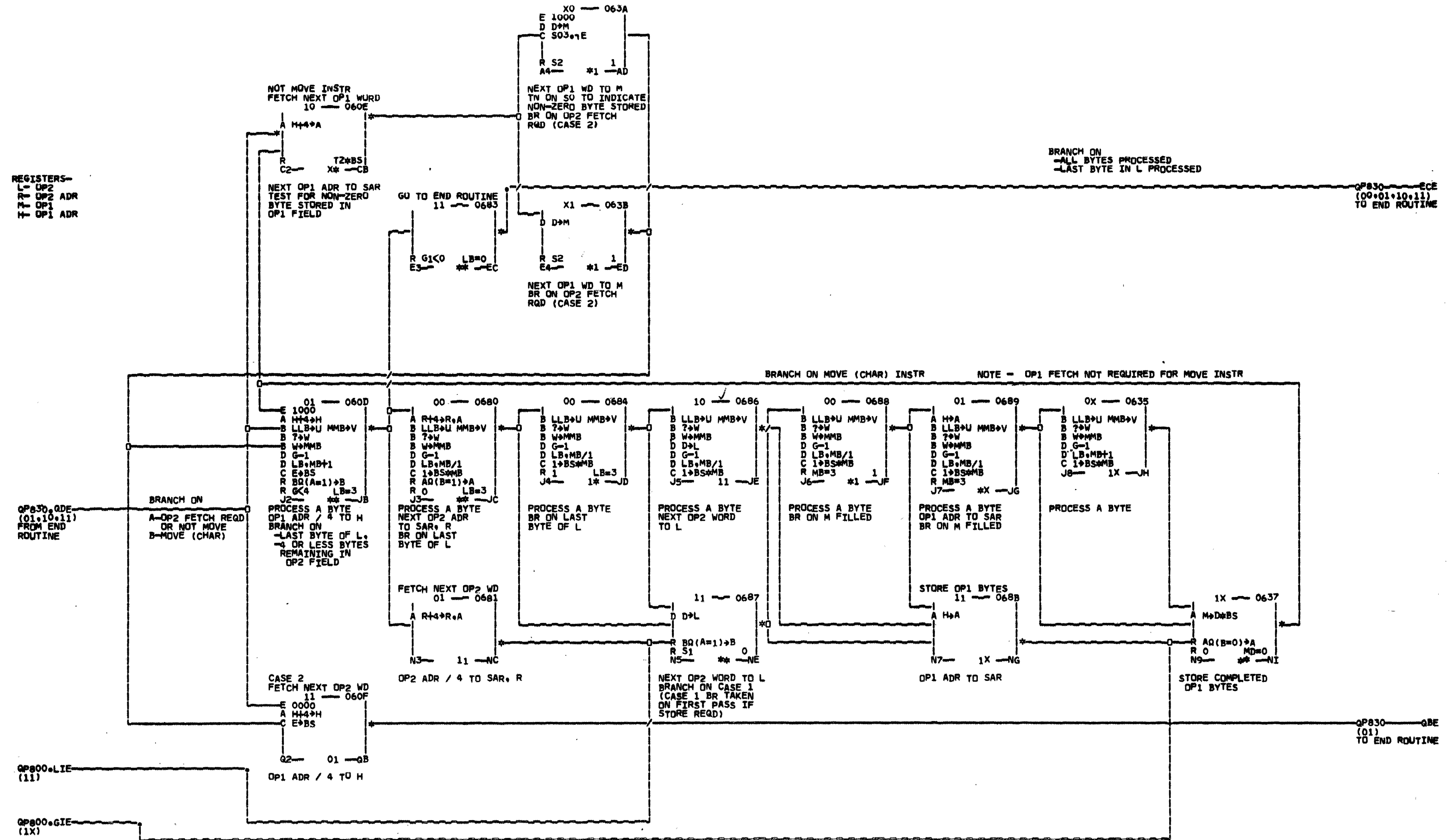
DANOS

2ND LEVEL I-FETCH FUNCTION BRANCH

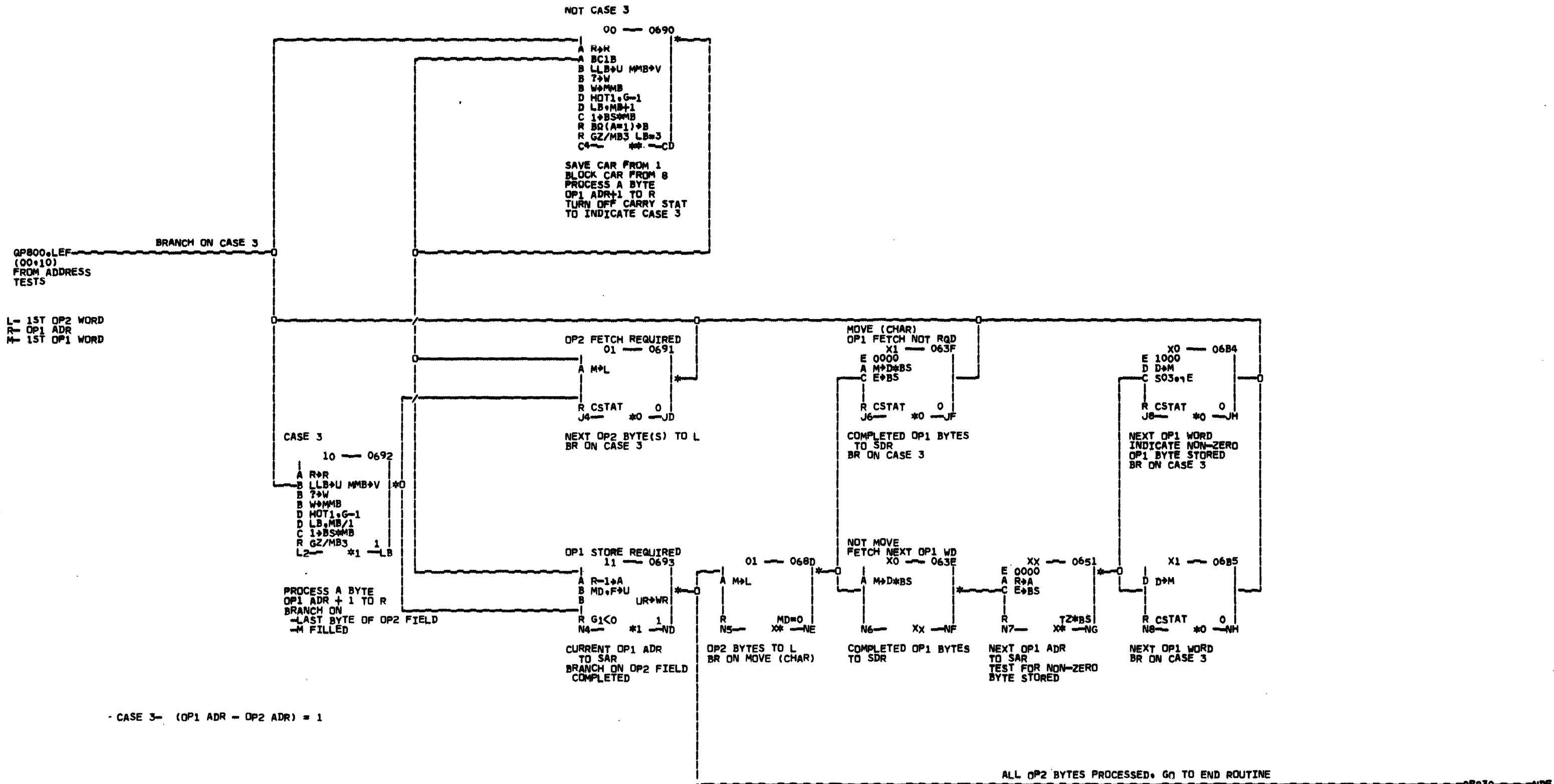


QP800

REGISTERS-
 L- OP2
 T- OP2 ADR
 T- OP1
 T- OP1 ADR



0-1870

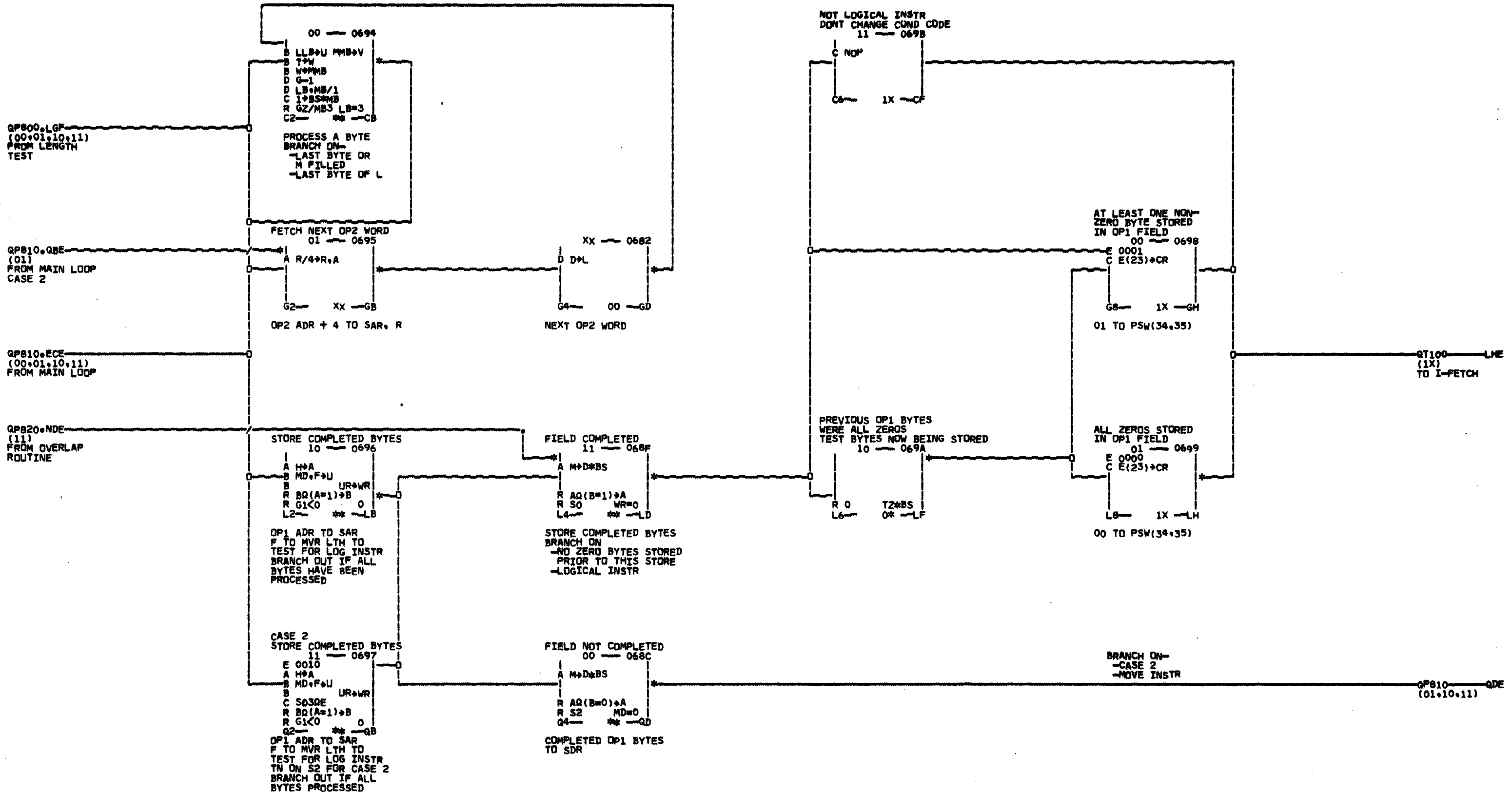


- CASE 3- (OP1 ADR - OP2 ADR) = 1

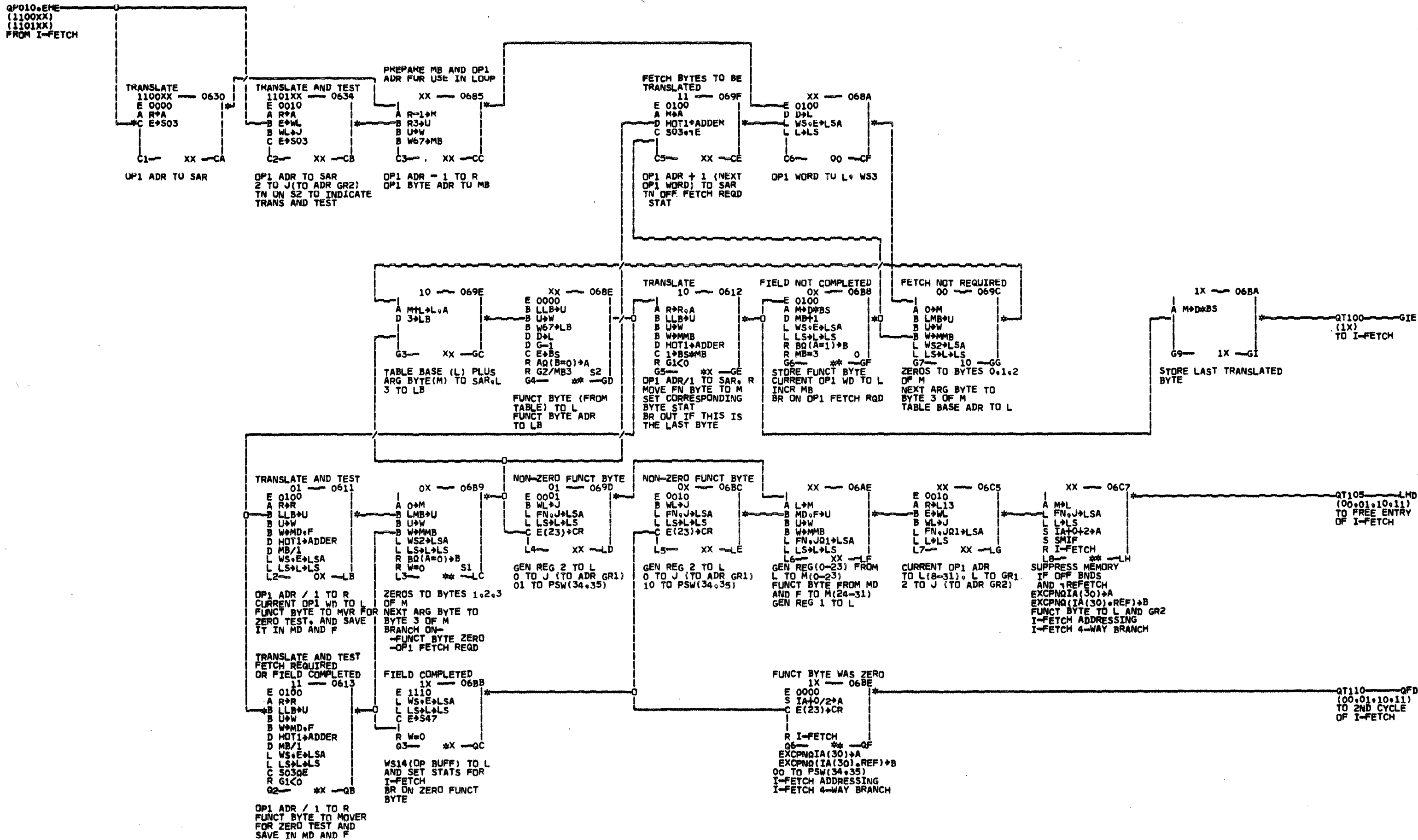
OP830 — NDE
(11)
TO END ROUTINE

ON 820

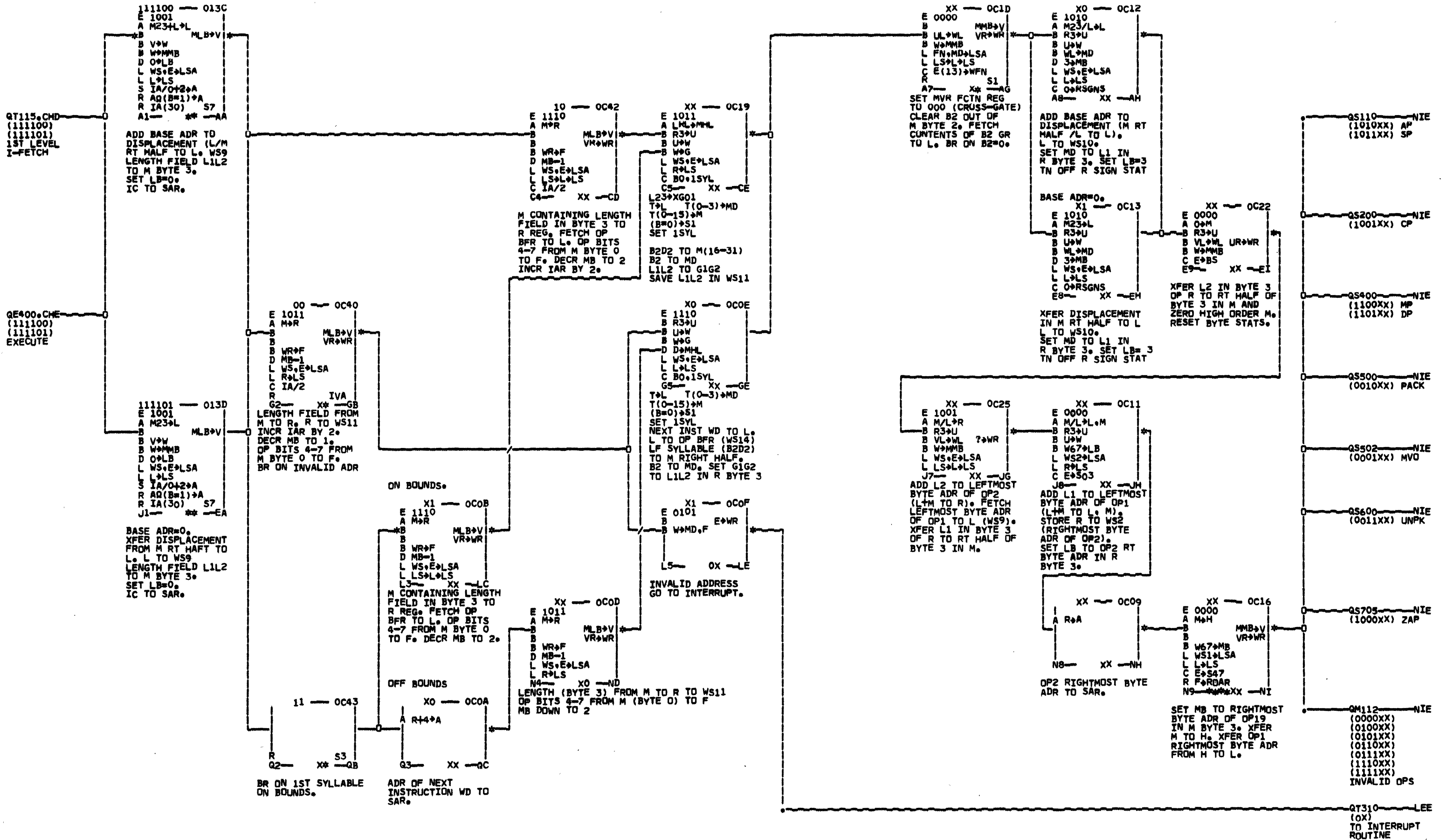
REGISTERS-
 L1 OP2
 R1 OP2 ADR
 T1 OP1
 T OP1 ADR



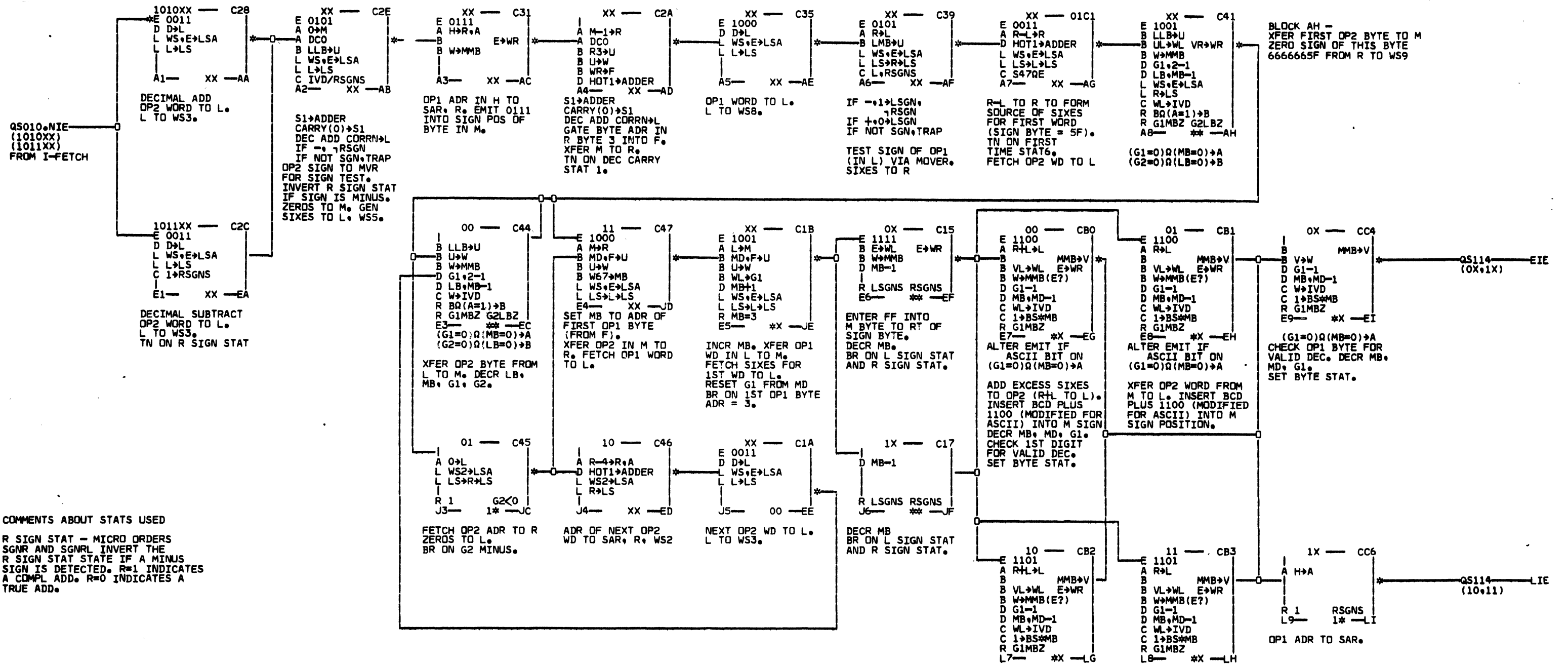
04870



0000



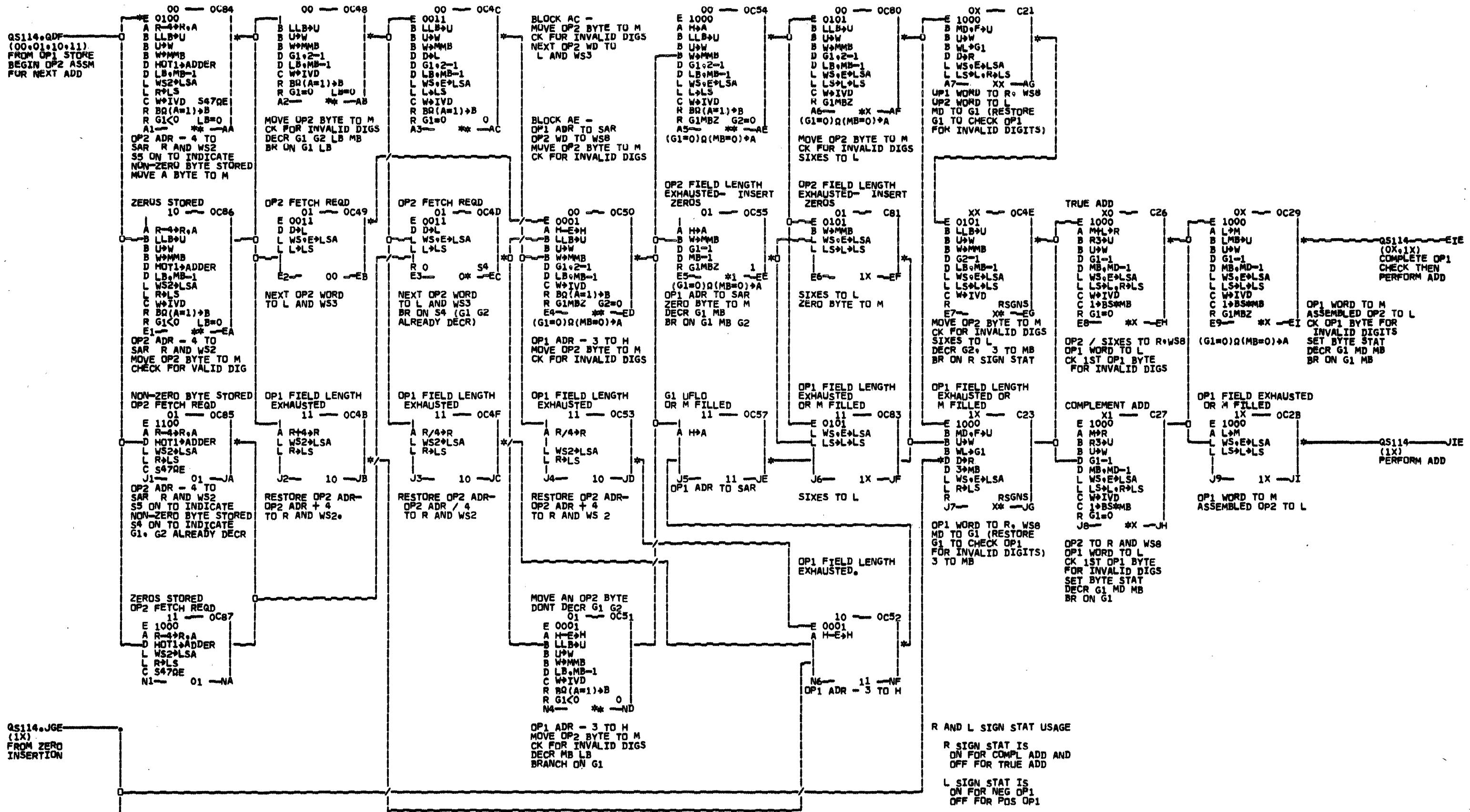
02048



COMMENTS ABOUT STATS USED
 R SIGN STAT - MICRO ORDERS
 SGNR AND SGNRL INVERT THE
 R SIGN STAT STATE IF A MINUS
 SIGN IS DETECTED. R=1 INDICATES
 A COMPL ADD. R=0 INDICATES A
 TRUE ADD.

COMMENTS ABOUT WORKING STORE
 LOCATIONS USED.
 WS3 = OP2 WORD
 WS5 = 66666666
 WS8 = OP1 WORD OR ASSEMBLED
 OP2 WORD
 WS9 = SOURCE OF SIXES WITH
 5F IN SIGN BYTE.
 WS11 = OP FIELD L1L2 IN
 BYTES 1 AND 3

STAT 0 = OVERFLOW OF OP1 FIELD.
 STAT 1 = DECIMAL CARRY.
 STAT 2 = RECOMPLEMENT.
 STAT 4 = G1, G2 DECREMENTED.
 STAT 5 = NON-ZERO RESULTS.
 STAT 6 = FIRST WORD.

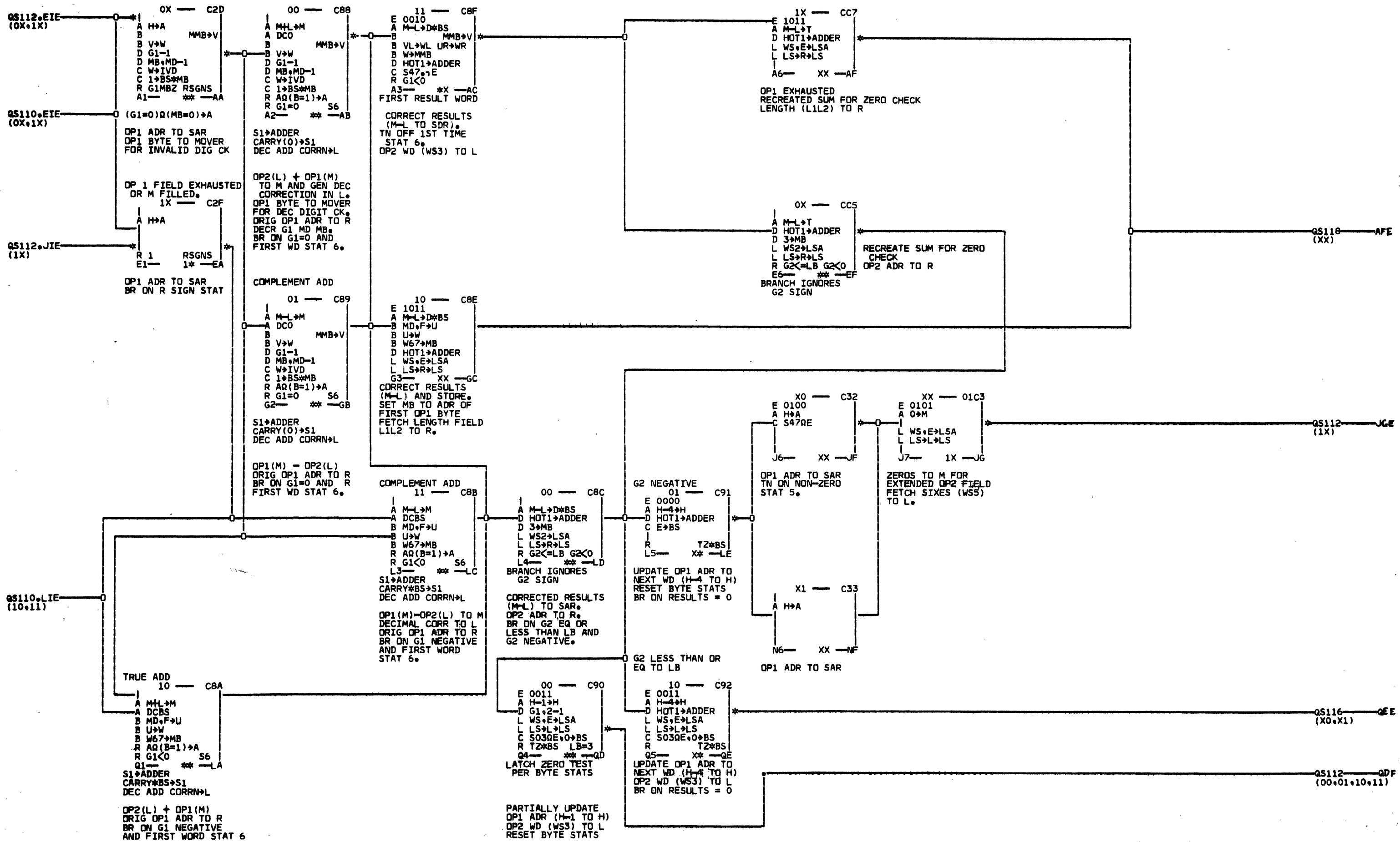


QS114.JGE
(1X)
FROM ZERO
INSERTION

QS116.GGE
(1X)
G2 LESS THAN 4

R AND L SIGN STAT USAGE
R SIGN STAT IS
ON FOR COMPL ADD AND
OFF FOR TRUE ADD
L SIGN STAT IS
ON FOR NEG OP1
OFF FOR POS OP1

21-58



4111

QS114.0EE
(X0.X1)
FROM MAIN LOOP

NUN-ZERO DIG STORED
X0 C3A
E 0100
A U+M
C 547QE
R 0 LB=3
C3 O* CC

ZERUS TO M
TN UN NUN-ZERO STAT
BR UN LB (FETCH REQD)

ZERUS STORED
X1 C3B
A O+M
R 0 LB=3
G3 O* GC

ZERUS TO M
BR ON LB EQ 3
(FETCH REQD)

FETCH NEXT OP2 WORD
01 C95
A R+R+A
D H0T1+ADDER
L WS2+LSA
R+LS
G4 XX GD

OP2 ADR - 4
TO SAR. R. WS2

XX C8D
E 0011
D D+L
L WS+E+LSA
L L+LS
G5 00 GE

LAST OP2 WORD TO L

00 C94
B LLB+U
B U+W
B W+MMB
D G1+2-1
D LB+MB-1
C W+IVD
C I+BS+MB
R AQ(B=1)+A
R G1=0 G2=0
C7 * * CG
OP2 BYTE TO M
CK FOR VALID DIGITS
SET BYTE STAT
DECR G1 G2 LB MB
BR ON G1 G2

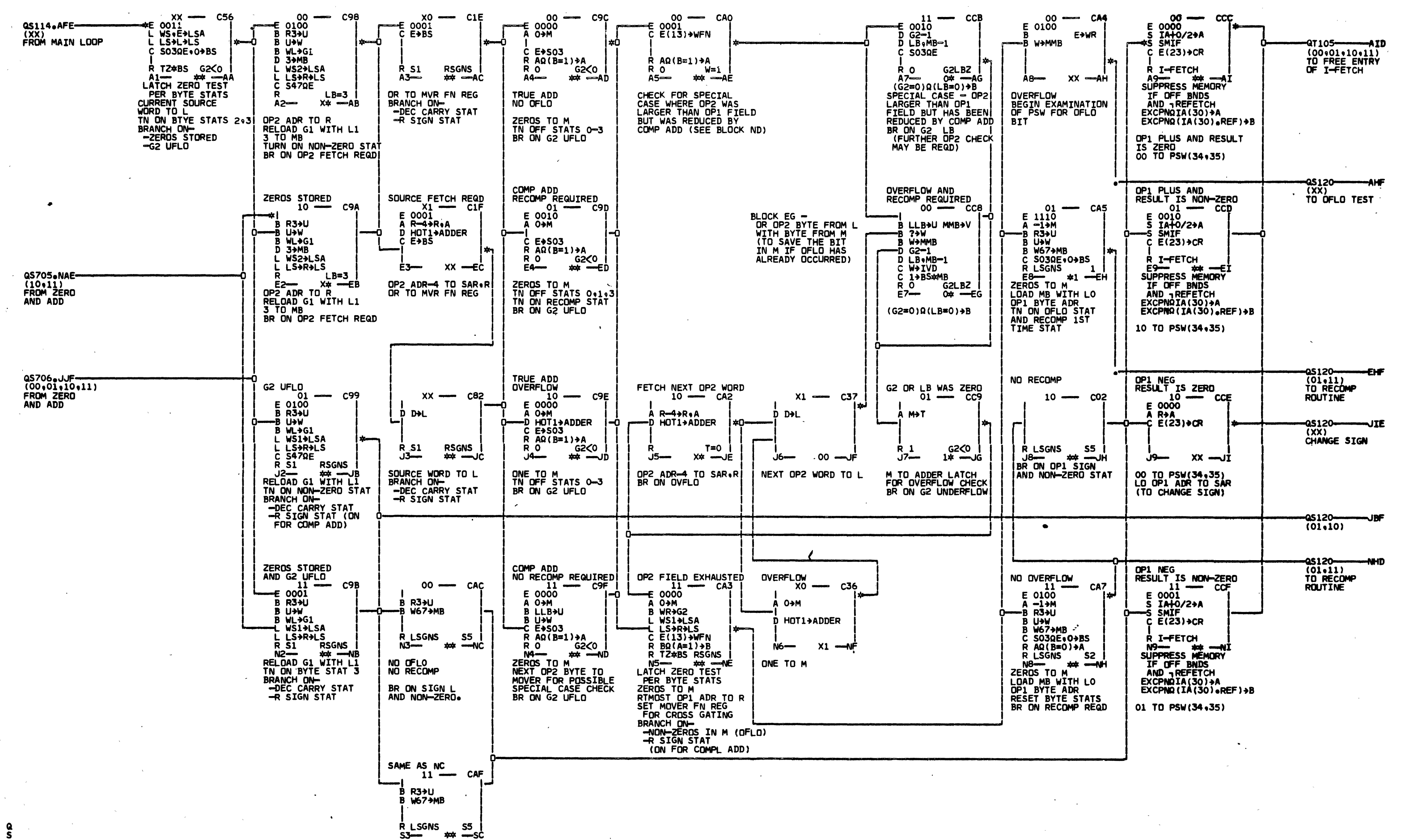
OP2 FIELD EXHAUSTED
10 C96
E 0101
A H+A
L WS+E+LSA
L LS+L+LS
G7 1X GG

OP1 ADR TO SAR
SIXES TO L

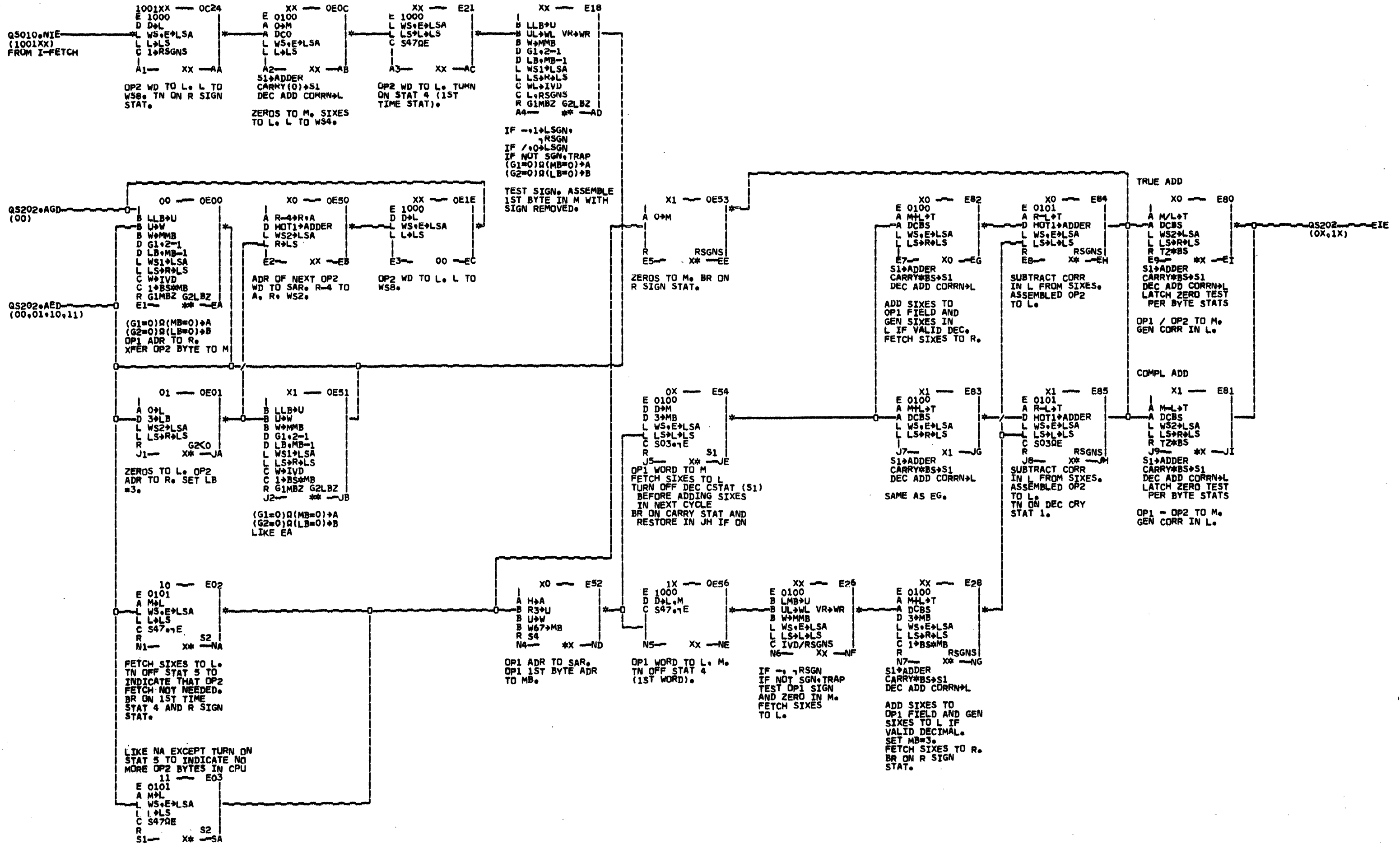
OP1 FIELD EXHAUSTED
(OP2 MAY ALSO BE
EXHAUSTED)
11 OC97
E 0101
A H+A
L WS+E+LSA
L LS+L+LS
L7 1X LG

OP1 ADR TO SAR
SIXES TO L

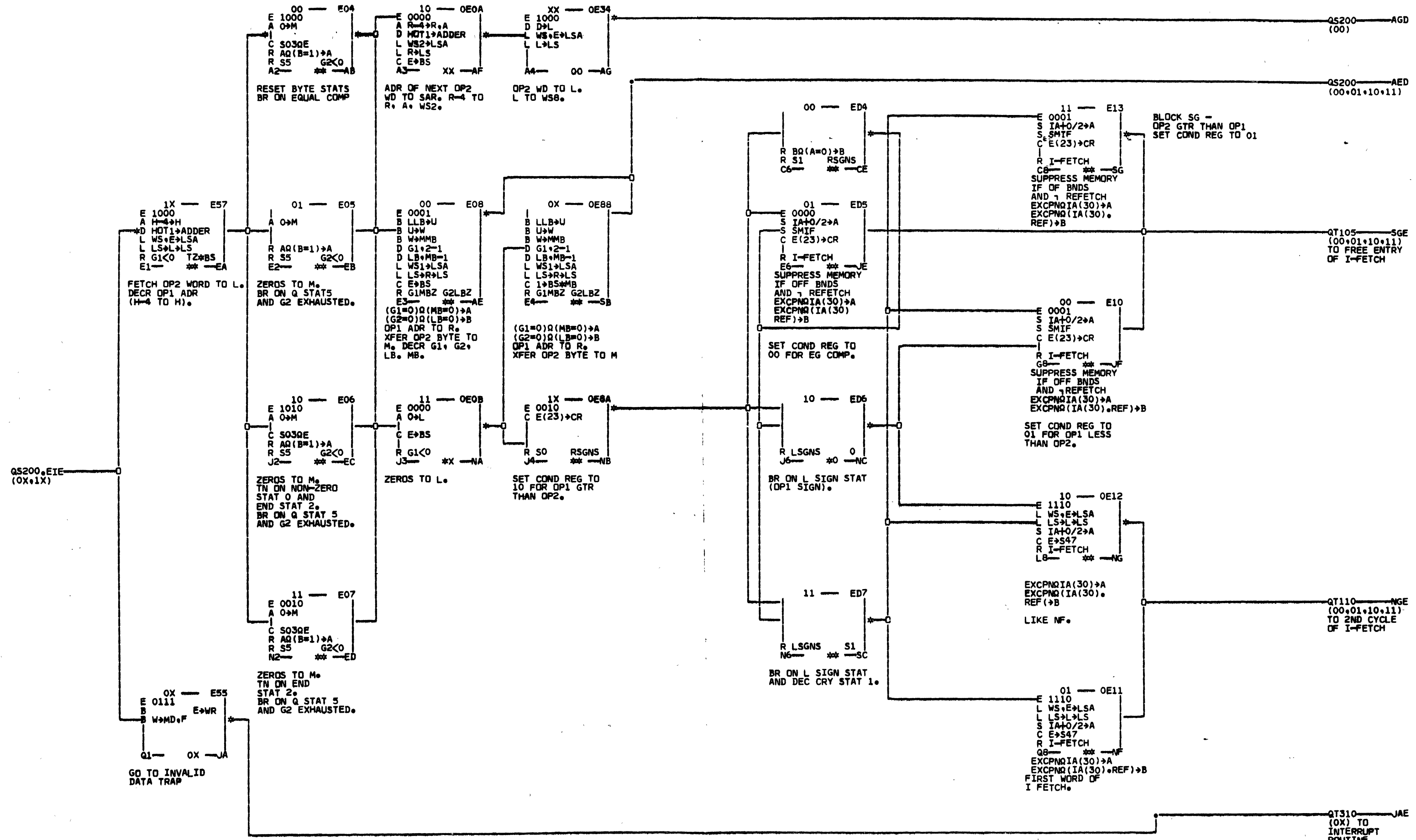
QS112 GGE
(1X)
CHECK OP1 FOR
VALID DECIMAL
DIGITS



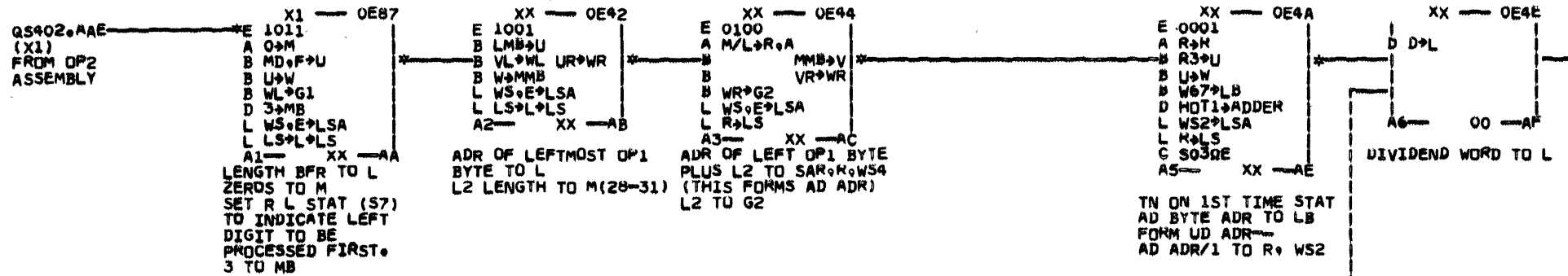
0111



000000



NONSP

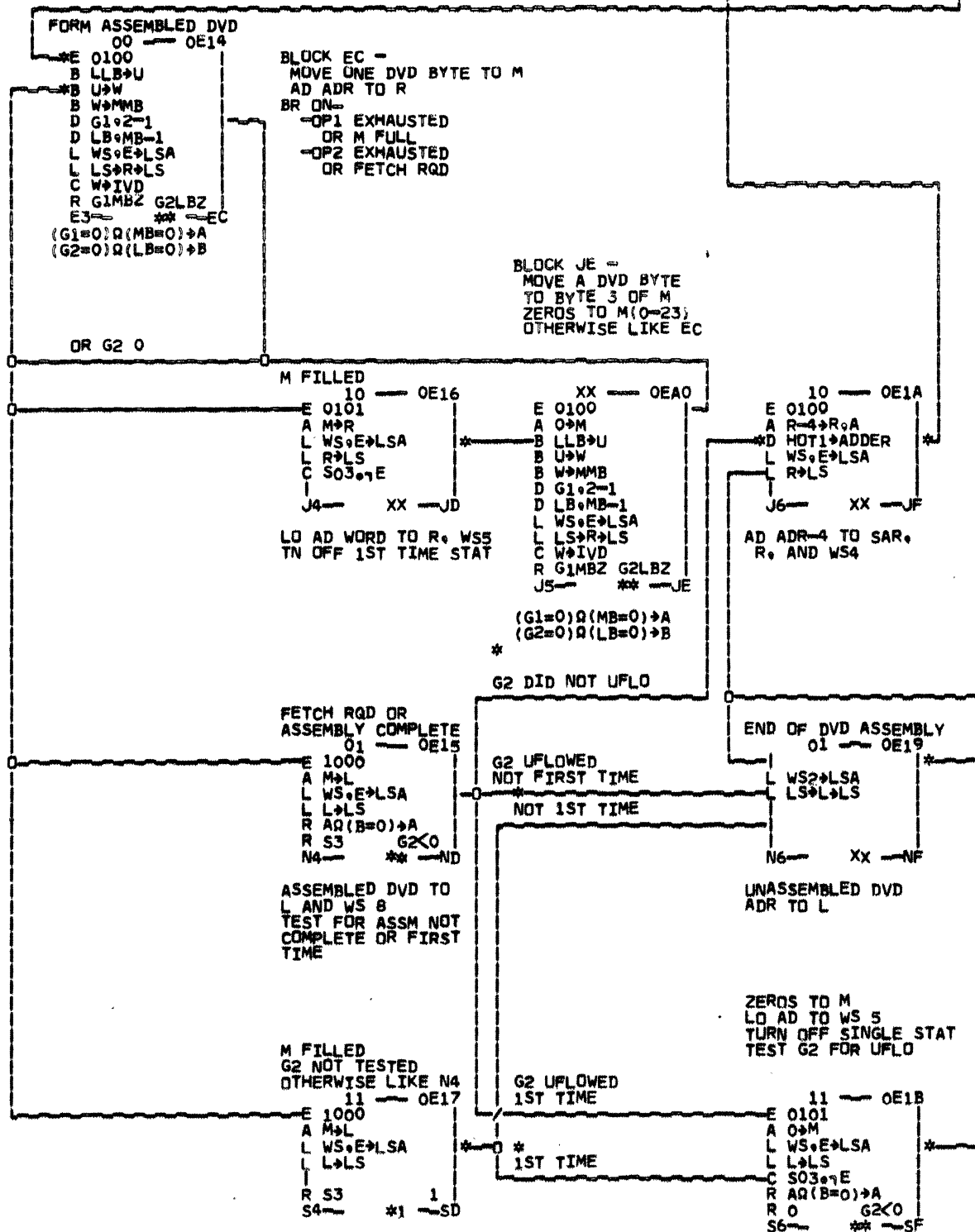


DIVIDING IS ACCOMPLISHED BY ASSEMBLING A NUMBER OF HIGH ORDER DIVIDEND BYTES EQUAL TO THE NUMBER OF DIVISOR BYTES (THIS WILL BE CALLED THE ASSEMBLED DIVIDEND OR AD); THEN SUBTRACTING THE DIVISOR (OPND2) REPEATEDLY UNTIL UNDERFLOW OCCURS. THEN THE DIVISOR IS ADDED BACK ONCE. THE HIGH ORDER QUOTIENT DIGIT IS EQUAL TO THE NUMBER OF REDUCTIONS MADE BEFORE UNDERFLOW OCCURRED. THE ASSEMBLED DIVIDEND IS THEN SHIFTED LEFT 1 DIG. THE NEXT DIGIT FROM THE UNASSEMBLED DIVIDEND IS INSERTED INTO THE LOW ORDER DIGIT POSITION. THE PROCESS IS REPEATED FOR EACH SUCCESSIVE LOWER ORDER DIGIT UNTIL A QUOTIENT L1-L2 IN LENGTH HAS BEEN GENERATED.

AD - ASSEMBLED DIVIDEND, REDUCED AND SHIFTED LEFT ONE DIGIT POSITION FOR EACH QUOTIENT DIGIT.
 AD ADR - INITIALLY THE ADDRESS OF THE RIGHTMOST BYTE OF THE FIELD TO BE USED FOR THE AD. SUBSEQUENTLY DECREMENTED BY 4 UNTIL DVD ASSEMBLY COMPLETE.
 UD - UNASSEMBLED DIVIDEND. THE PORTION OF THE OP1 FIELD NOT YET USED IN THE AD. THIS PORTION IS REDUCED IN SIZE BY ONE BYTE FOR EACH QUOTIENT BYTE GENERATED
 UD ADR - ADDRESS OF THE LEFTMOST BYTE OF THE UD

WORKING STORE FOR DIVIDE DECIMAL
 WS 0 - HIGH ORDER DIVISOR
 WS 1 - OPERAND 1 ADDRESS (INITIALLY RIGHTMOST ADR)
 WS 2 - OPERAND 2 ADDRESS OR UNASSEMBLED DIVIDEND ADDRESS
 WS 3 - UNASSEMBLED DIVIDEND
 WS 4 - ASSEMBLED DIVIDEND ADDRESS OR PARTIAL QUOTIENT
 WS 5 - LOW ORDER ASSEMBLED DIVIDEND
 WS 6 - LOW ORDER DIVISOR
 WS 8 - HIGH ORDER ASSEMBLED DIVIDEND
 WS 9 - OPERAND 1 ADDRESS (INITIALLY LEFTMOST ADR)
 WS10 - LOW ORDER DIVISOR + 6S
 WS11 - LENGTH BUFFER
 WS12 - HIGH ORDER DIVISOR / 6S

STATS FOR DIVIDE DECIMAL
 STAT 0 - OFF INDICATES DIVIDE INSTRUCTION.
 STAT 1 - DECIMAL CARRY STAT
 CONTROL FLOW THROUGH LOOP. ON STATE INDICATES THE LOW ORDER AD WORD IS BEING ASSEMBLED.
 STAT 5 - SINGLE STAT. ON STATE INDICATES A SINGLE WORD DIVISOR.
 STAT 7 - RIGHT-LEFT STAT. ON STATE INDICATES THE NEXT QUOTIENT DIGIT IS TO BE PLACED IN THE LEFT DIGIT POSITION OF THE NEXT BYTE. INITIALLY USED TO INDICATE SINGLE DIVIDE CK TEST REQUIRED



QS302 NFD (XX)

QS300

254770
254772
255449

02/01+65
02/23+65
09/20+65

MACH
NAME
MODE
P.No.
IBM CORP.

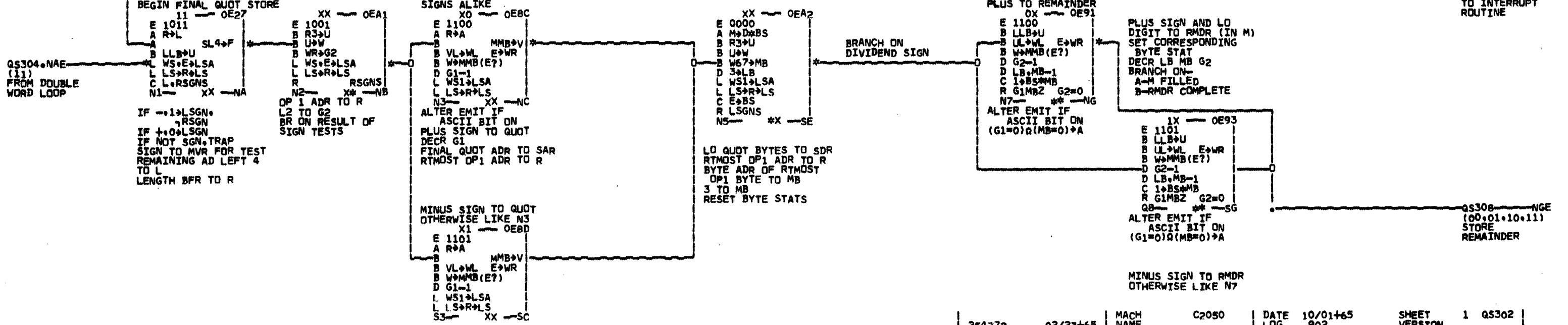
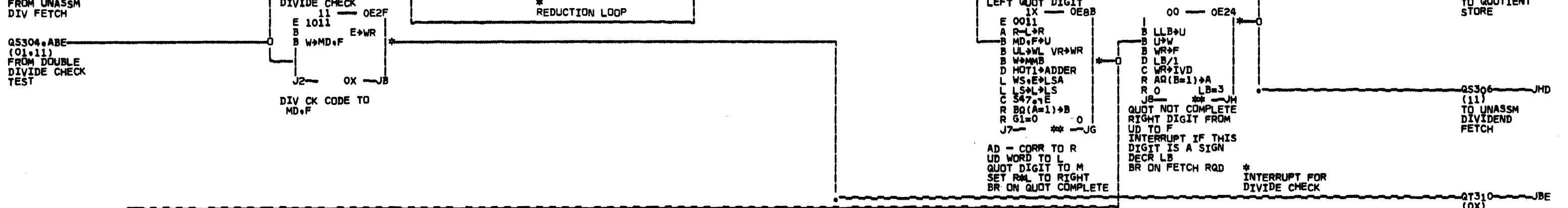
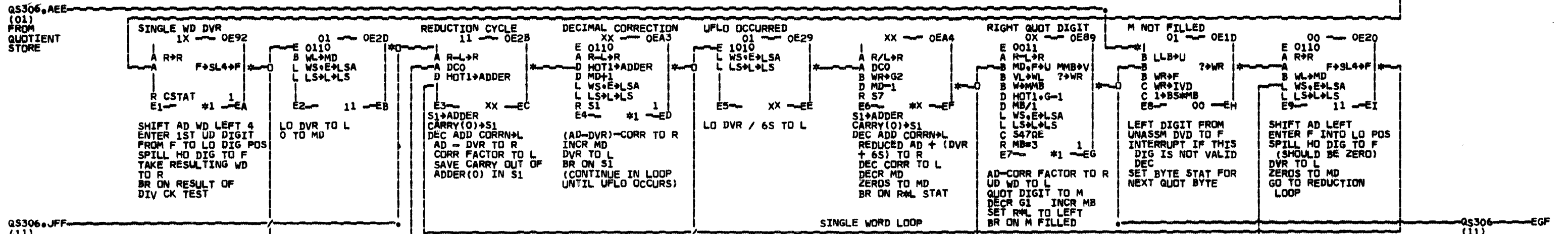
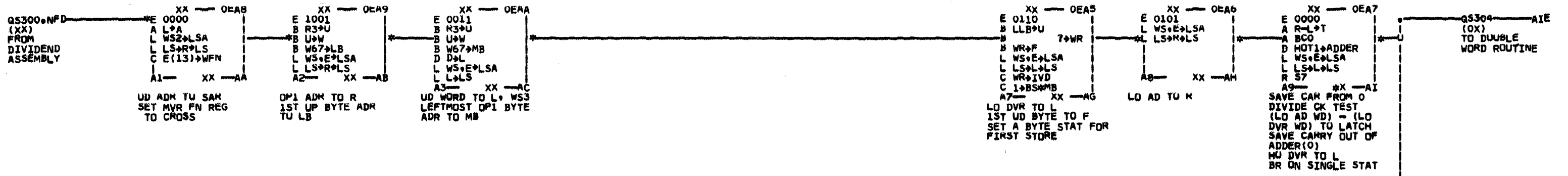
C2050
MANUAL
5364816
SND

DATE 10/01+65
LOG 902

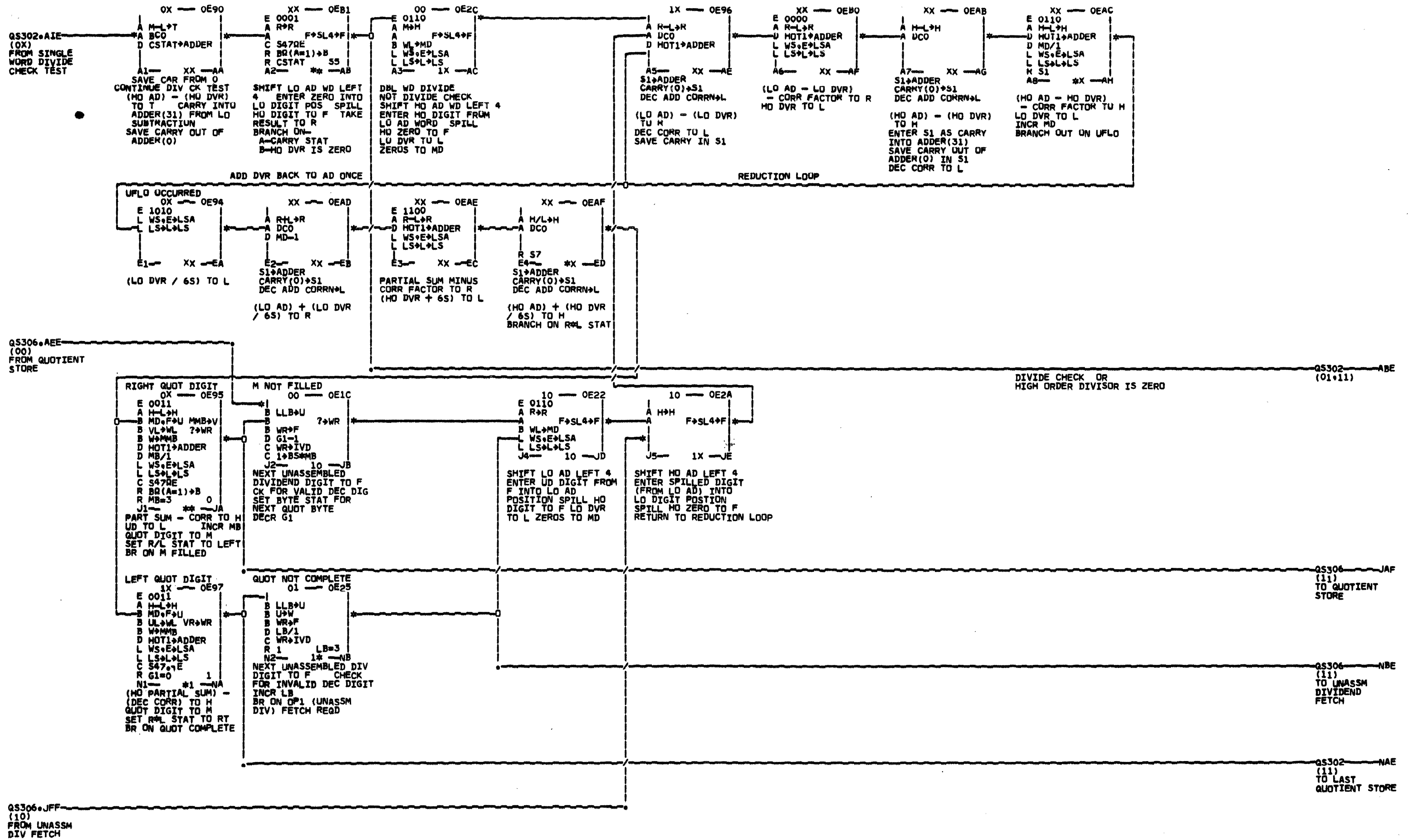
SHEET
VERSION

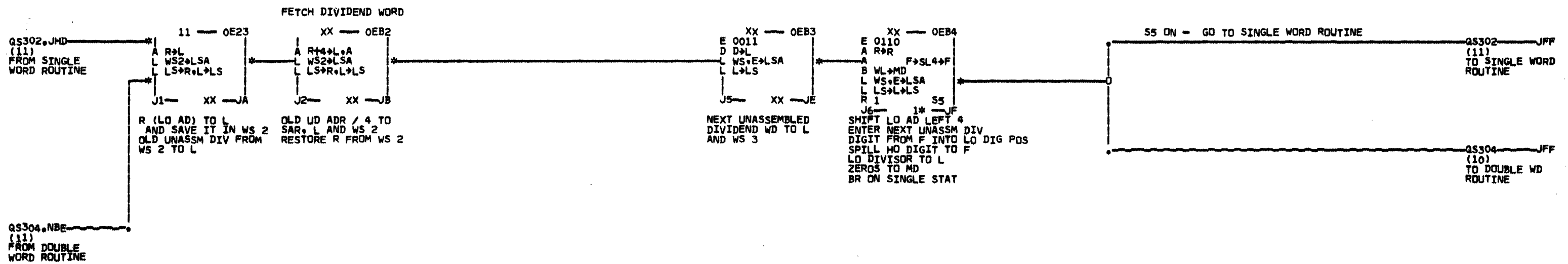
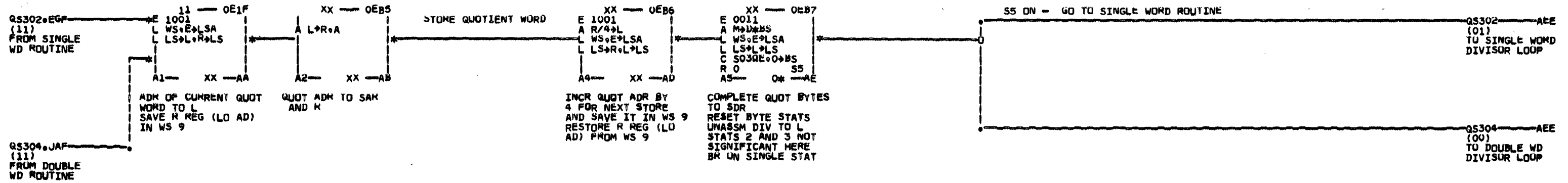
1 QS300

DIVIDE DECIMAL (DP)
DIVIDEND ASSEMBLY

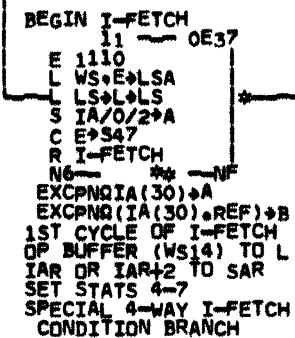
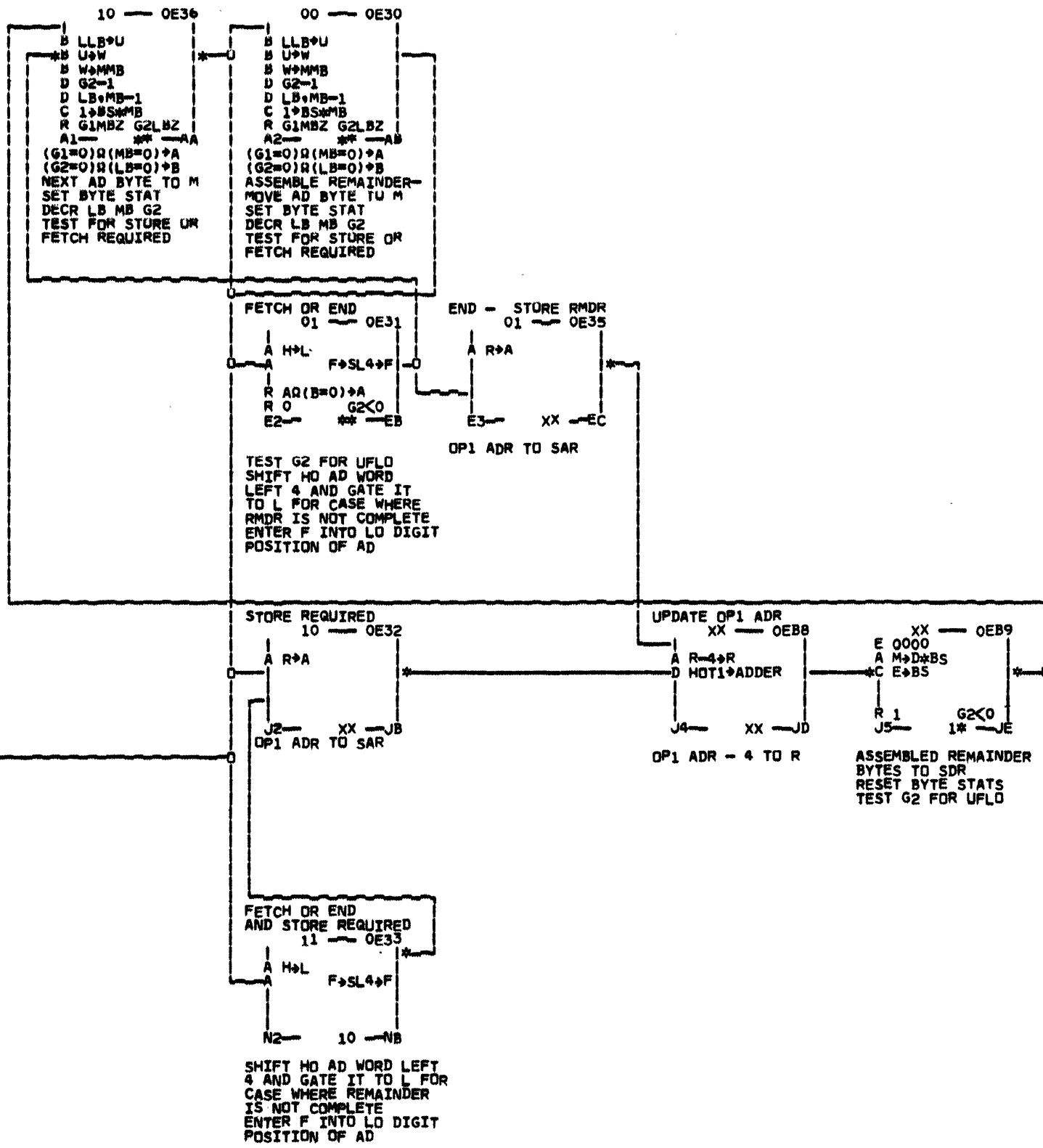


ROUND



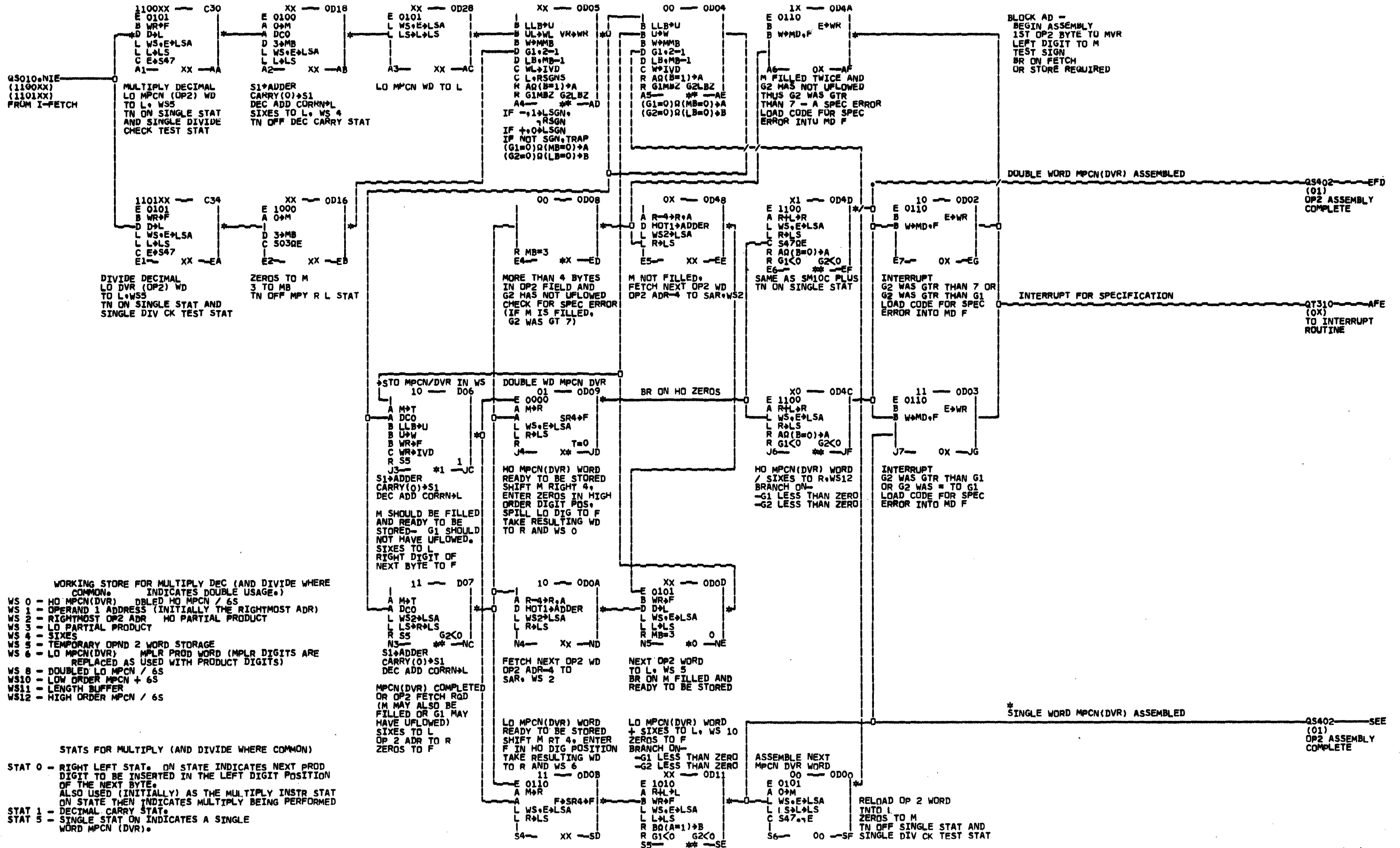


QS302,NGE
(00,01,10,11)
FROM FINAL
QUOTIENT STORE



QT110 NFE
(00,01,10,11)
TO 2ND CYCLE
OF I-FETCH

BOUSS

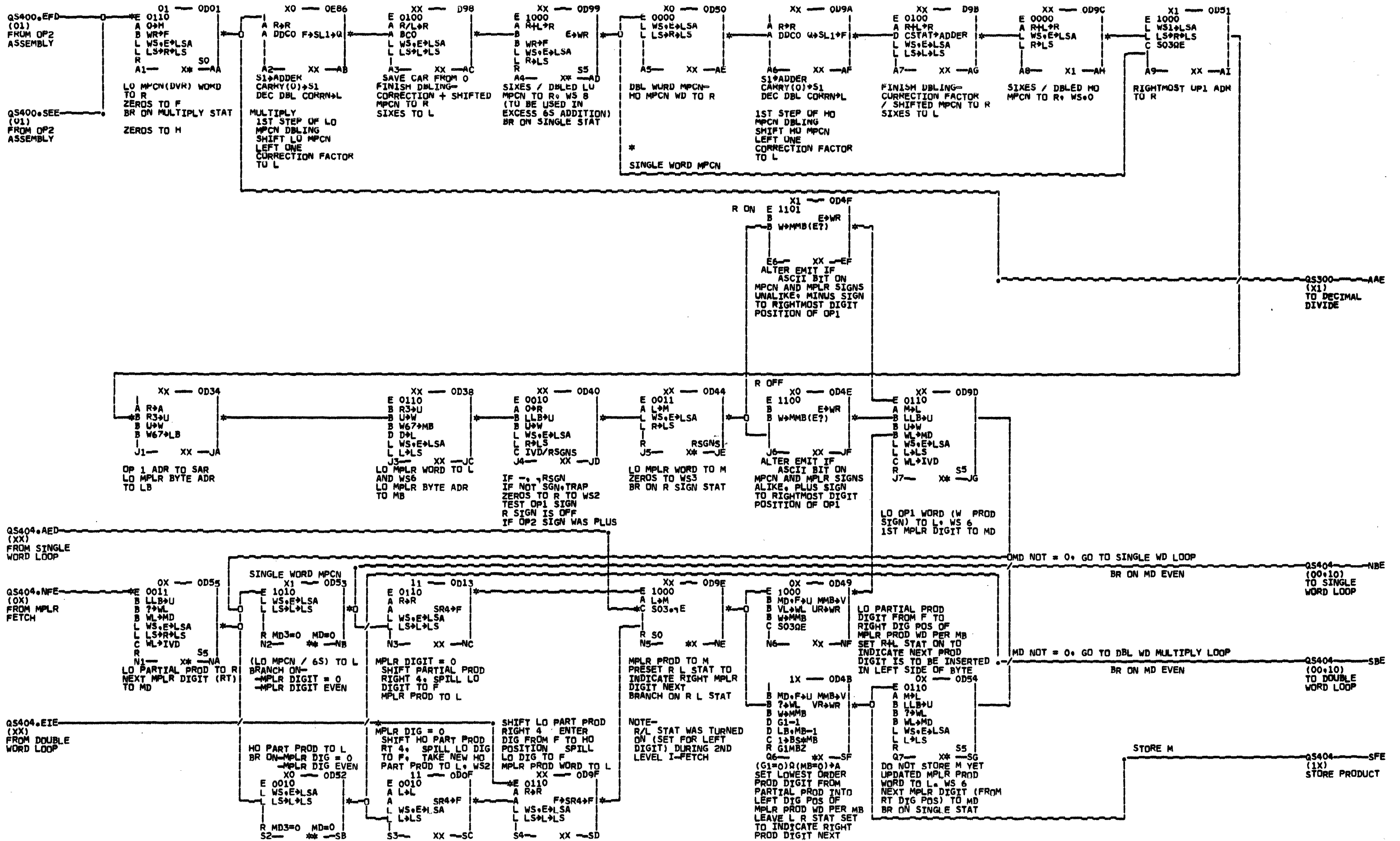


WORKING STORE FOR MULTIPLY DEC (AND DIVIDE WHERE COMMON. INDICATES DOUBLE USAGE.)

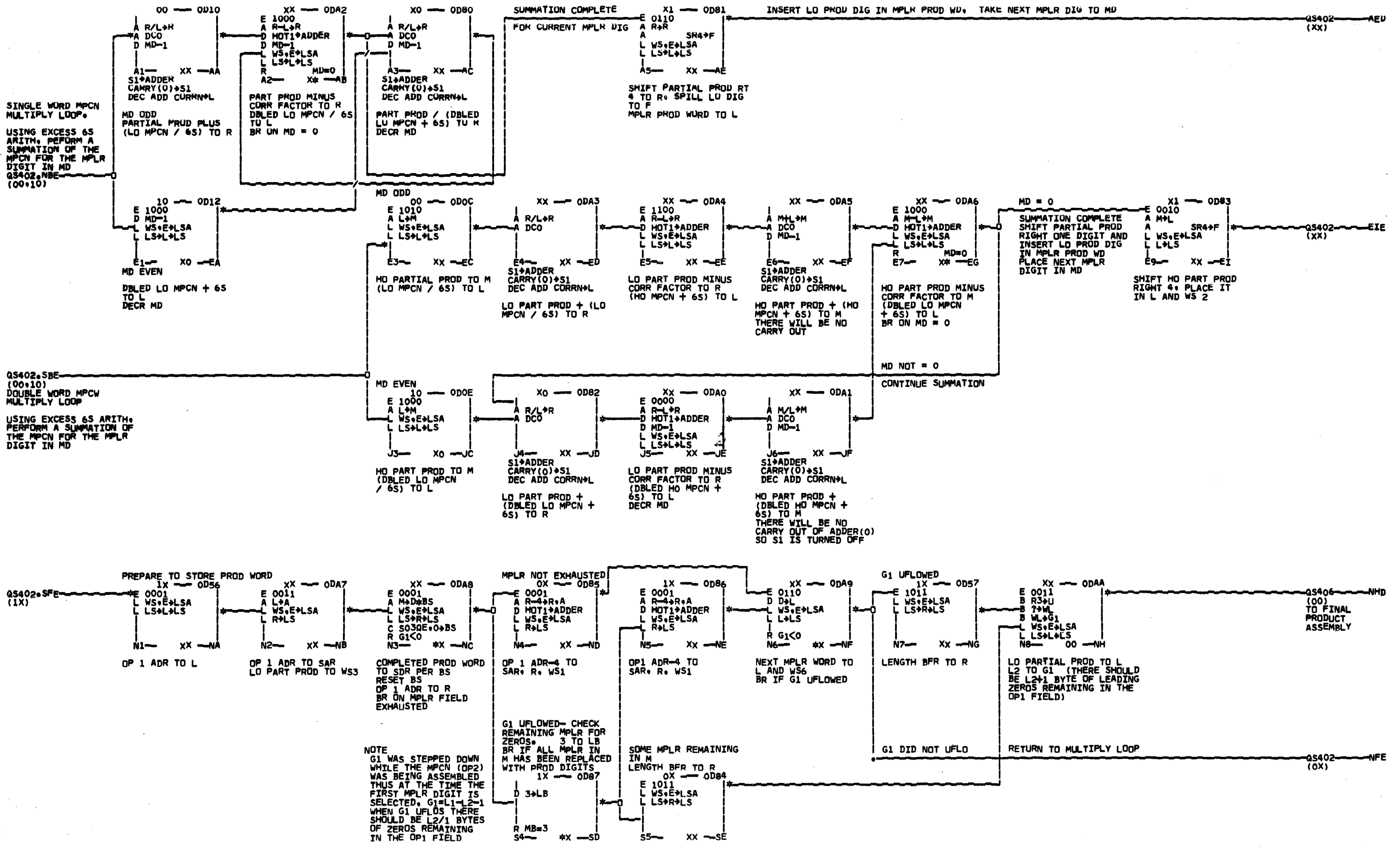
- WS 0 - HO MPCN(DVR) DBLED HO MPCN / 6S
- WS 1 - OPERAND 1 ADDRESS (INITIALLY THE RIGHTMOST ADR)
- WS 2 - RIGHTMOST OP2 ADR HO PARTIAL PRODUCT
- WS 3 - LD PARTIAL PRODUCT
- WS 4 - SIXES
- WS 5 - TEMPORARY OPND 2 WORD STORAGE
- WS 6 - LD MPCN(DVR) MPLR PROD WORD (MPLR DIGITS ARE REPLACED AS USED WITH PRODUCT DIGITS)
- WS 8 - DOUBLED LO MPCN / 6S
- WS10 - LOW ORDER MPCN + 6S
- WS11 - LENGTH BUFFER
- WS12 - HIGH ORDER MPCN / 6S

STATS FOR MULTIPLY (AND DIVIDE WHERE COMMON)

- STAT 0 - RIGHT LEFT STAT. ON STATE INDICATES NEXT PROD DIGIT TO BE INSERTED IN THE LEFT DIGIT POSITION OF THE NEXT BYTE. ALSO USED (INITIALLY) AS THE MULTIPLY INSTR STAT ON STATE THEN INDICATES MULTIPLY BEING PERFORMED
- STAT 1 - DECIMAL CARRY STAT
- STAT 5 - SINGLE STAT ON INDICATES A SINGLE WORD MPCN (DVR).

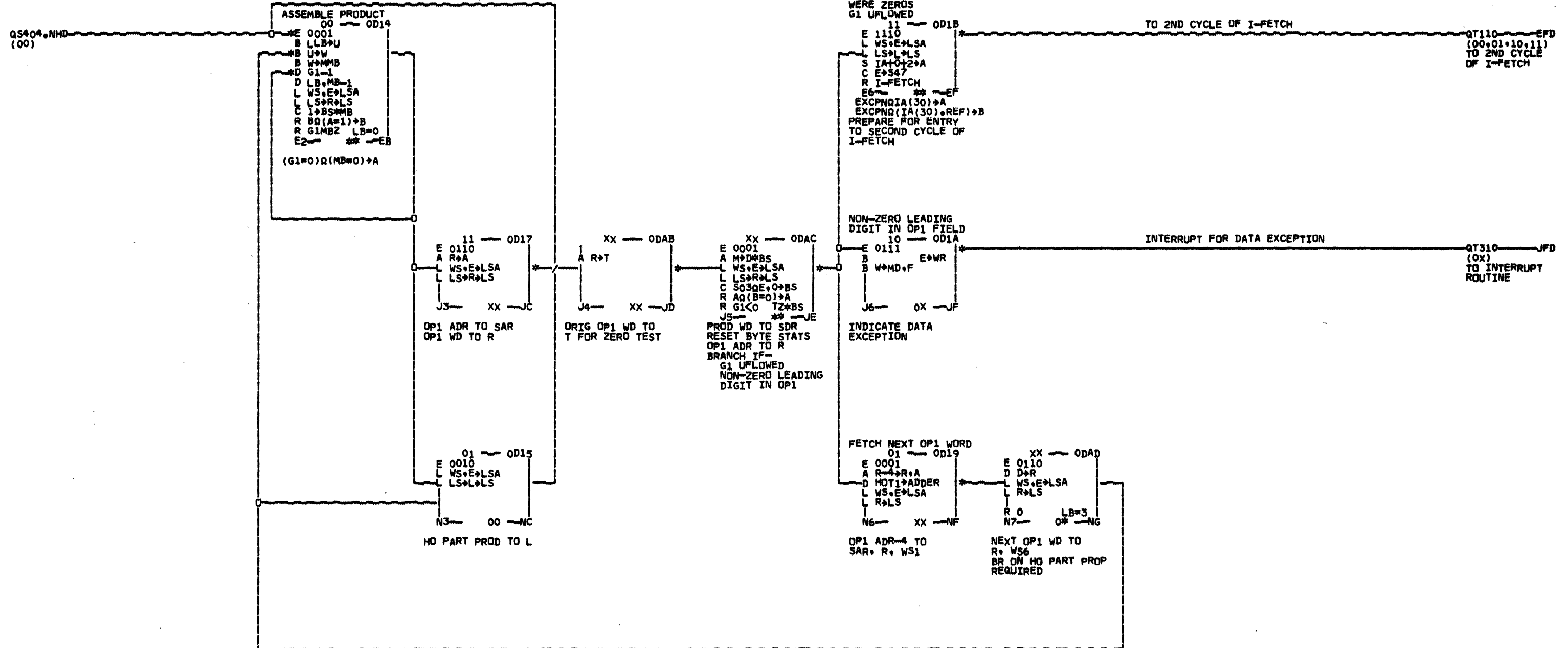


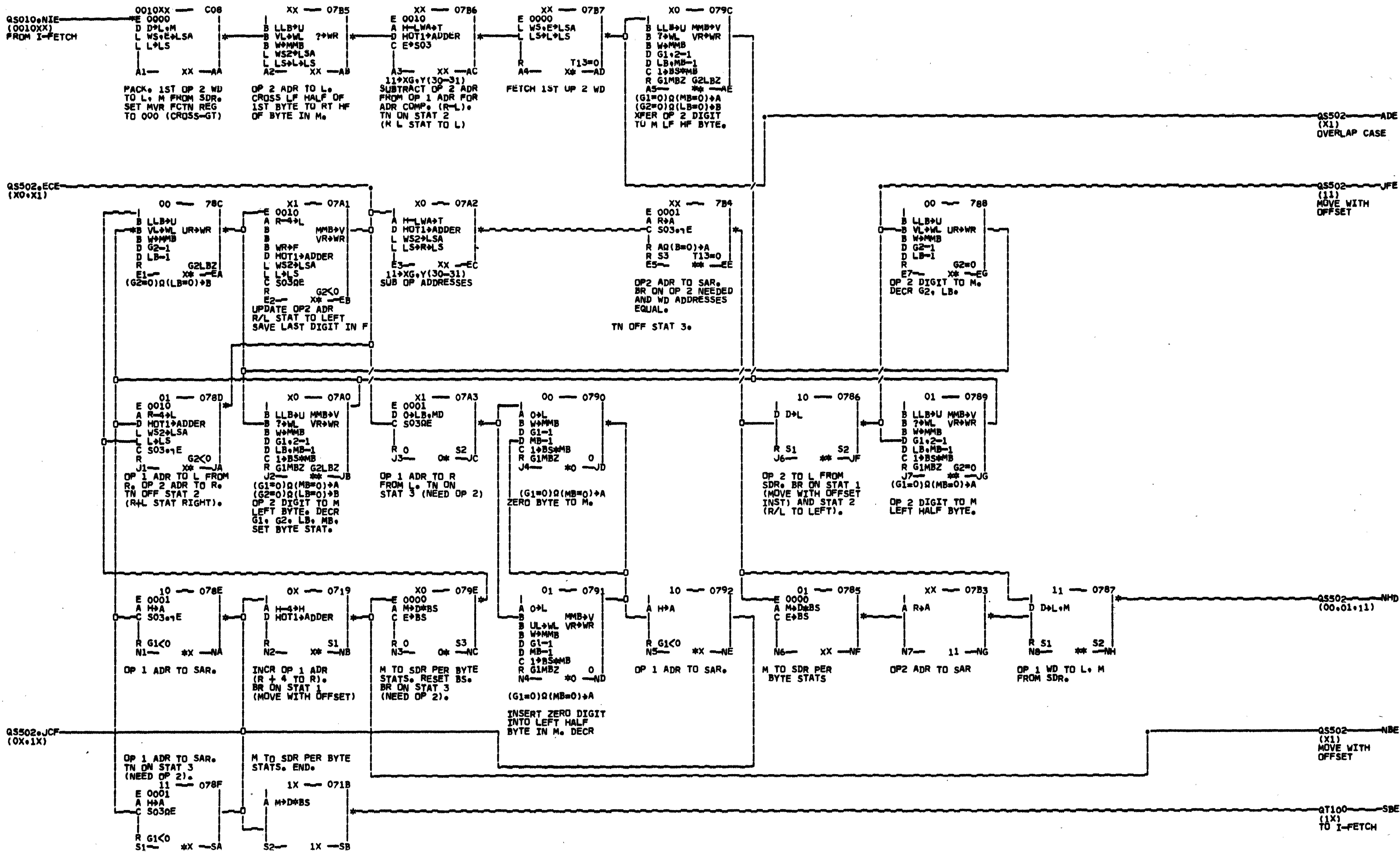
Q
S
4
0
2



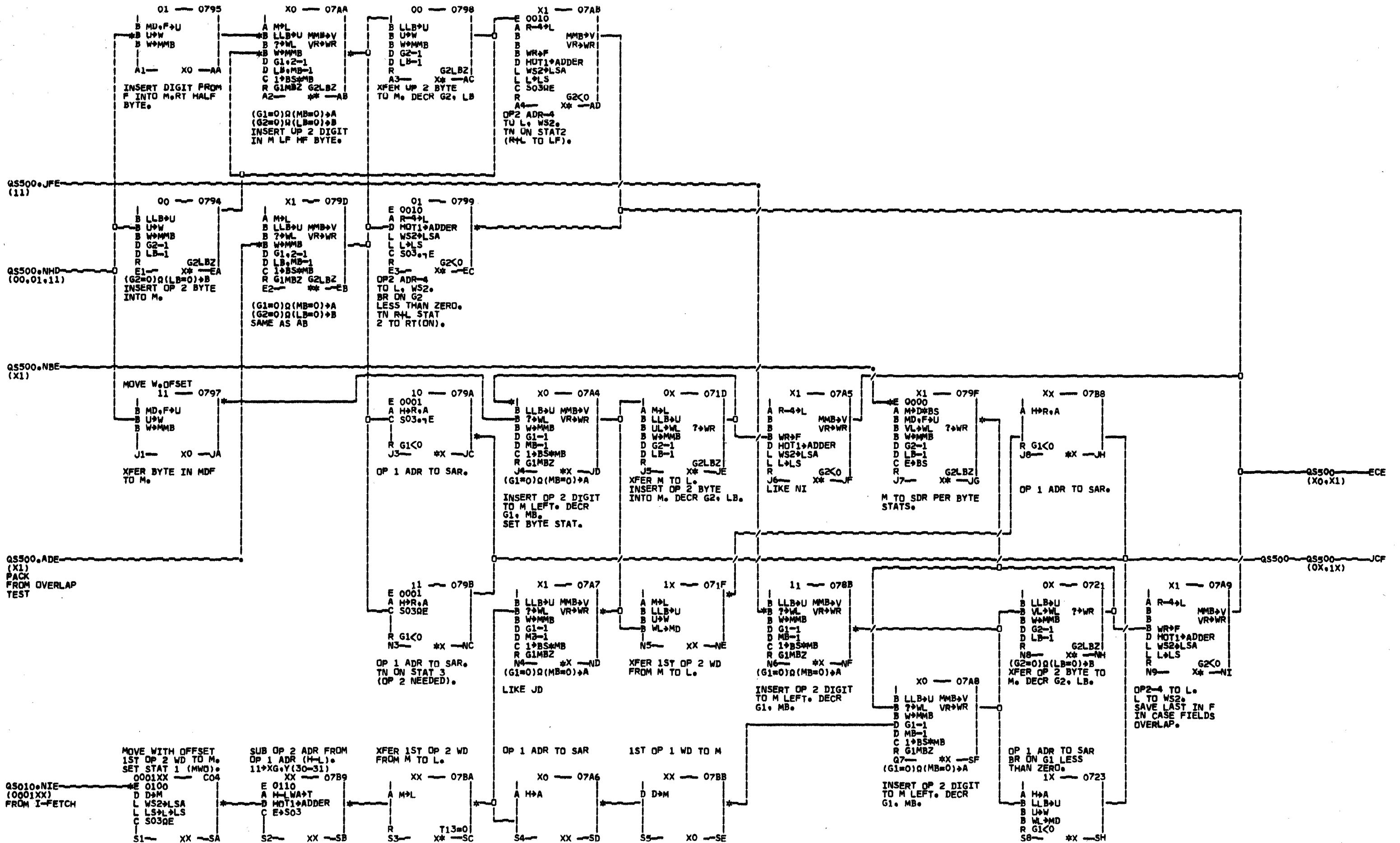
4040

BLOCK EB -
 MOVE A PRODUCT BYTE TO M
 AND SET BYTE STAT
 OP1 ADR TO R
 BRANCH ON -
 -G1=0 OR M FULL
 -NO PARTIAL PROD RQD



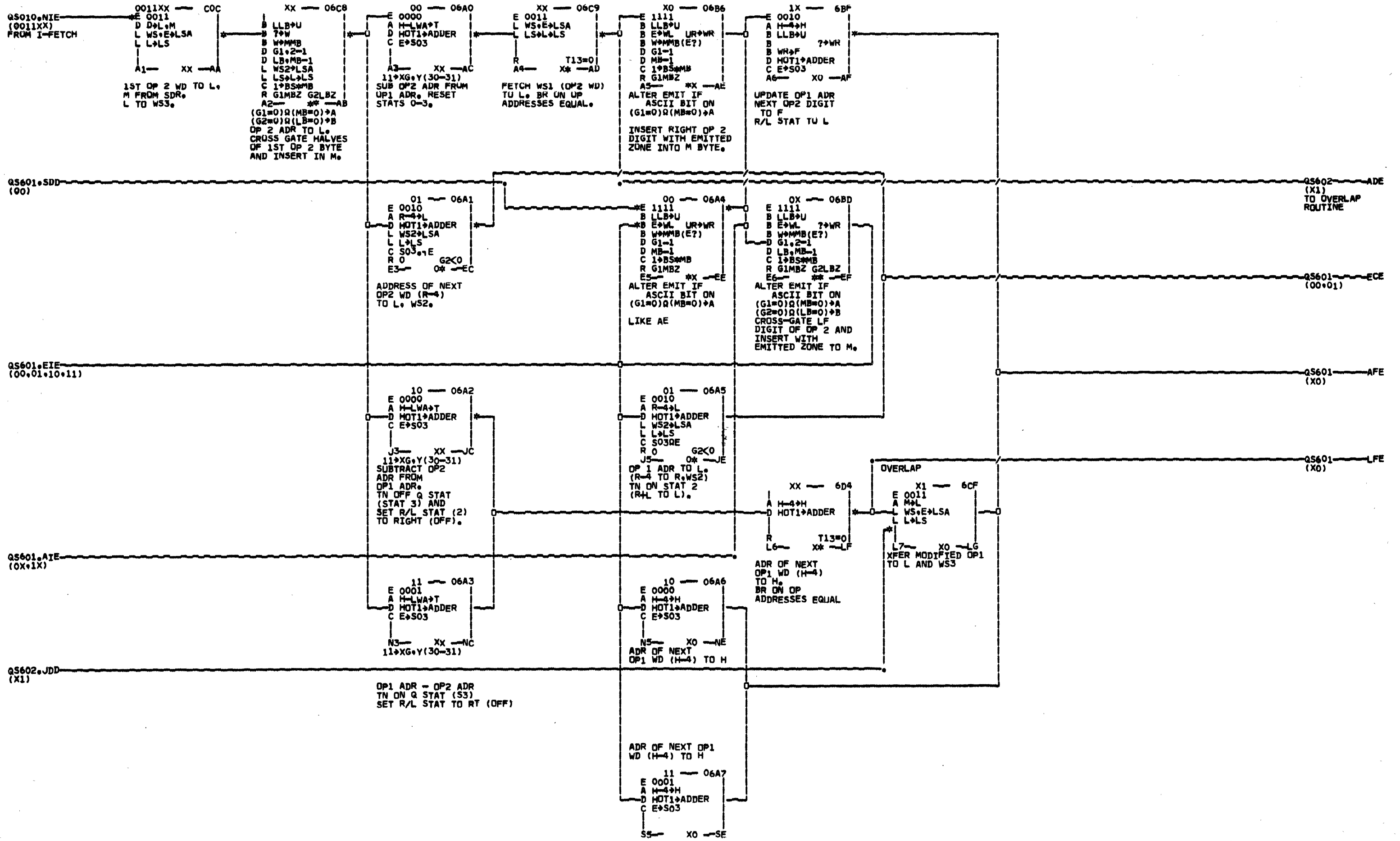


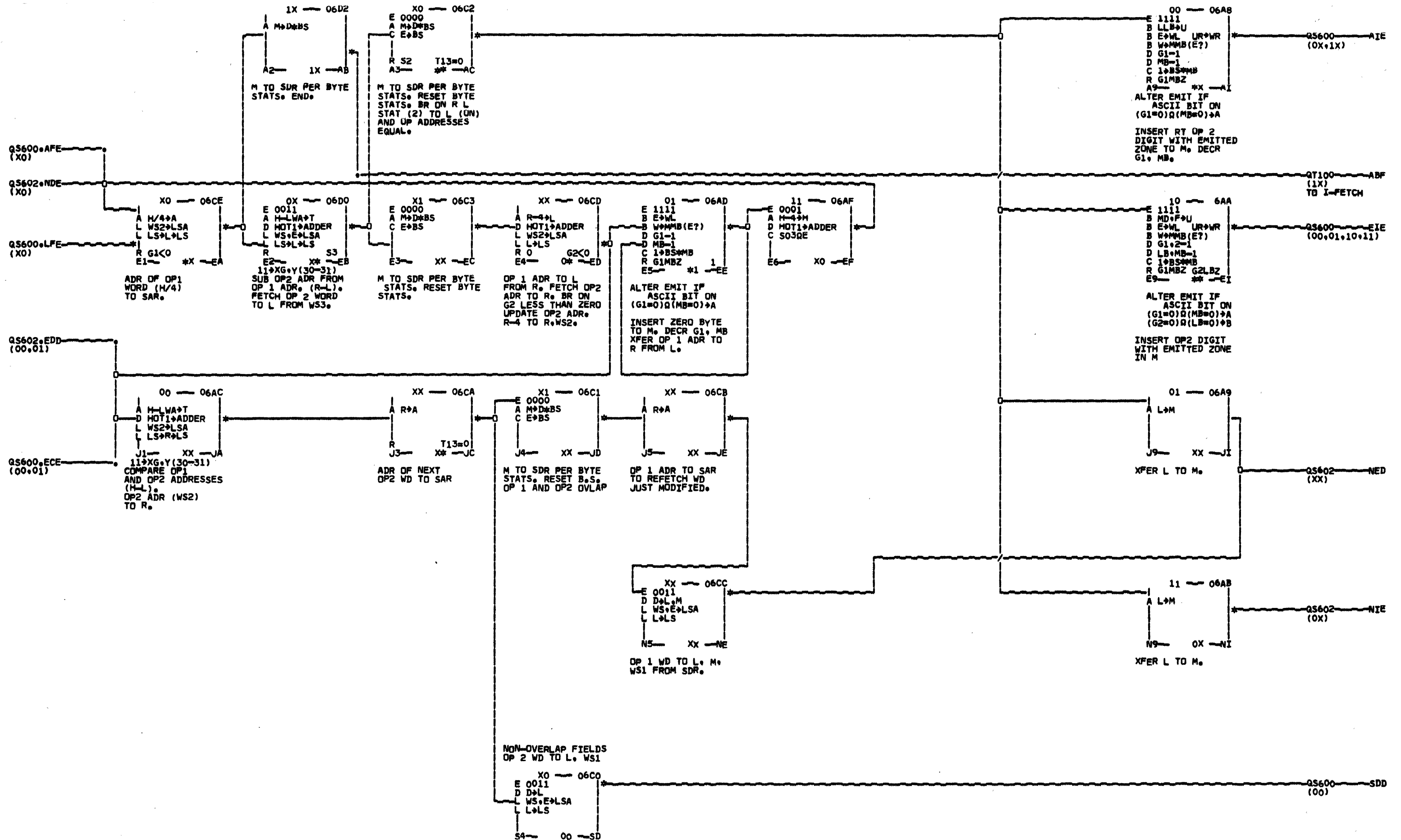
0000SD



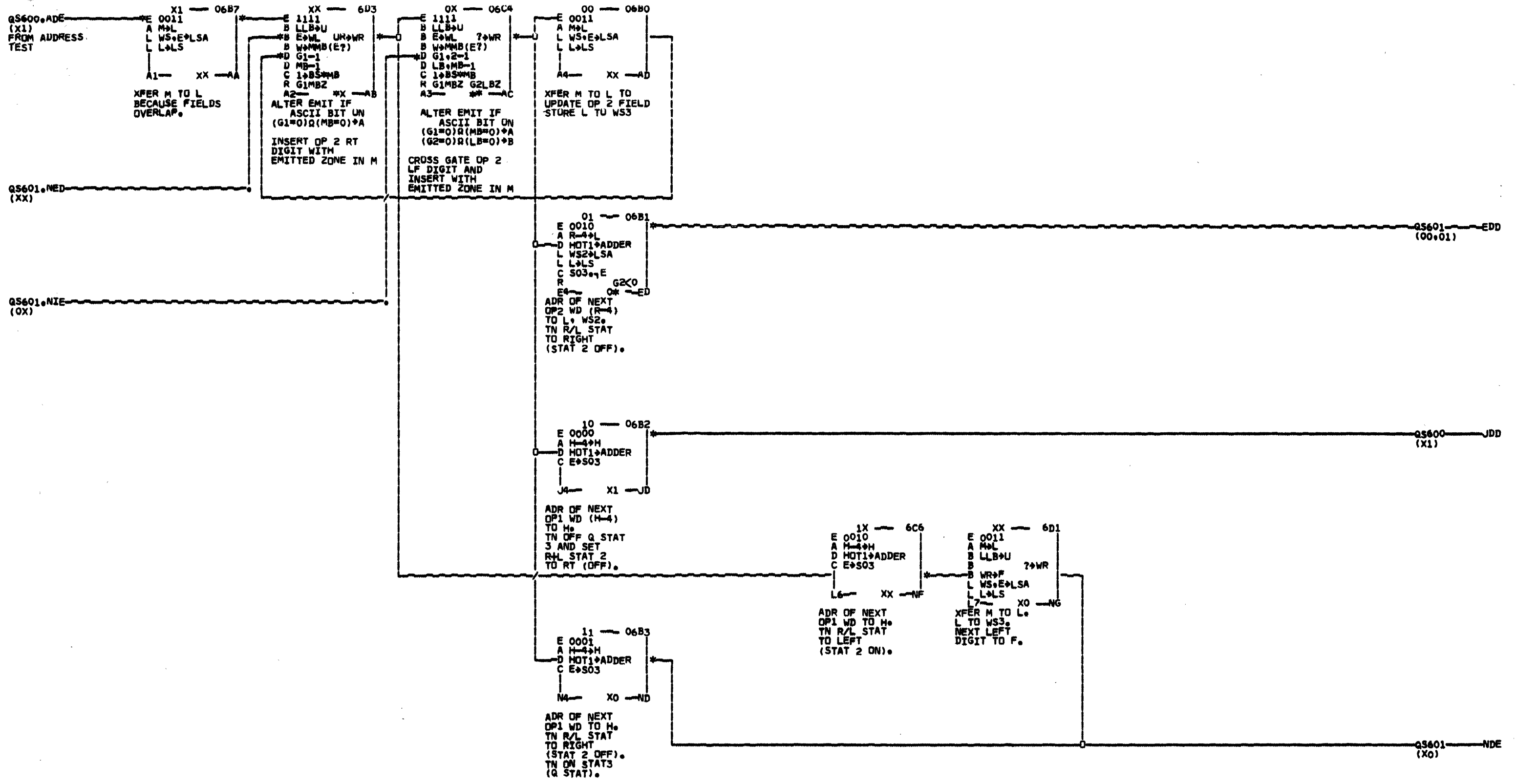
100000

PACK: MOVE WITH OFFSET





Q
S
6
0
1

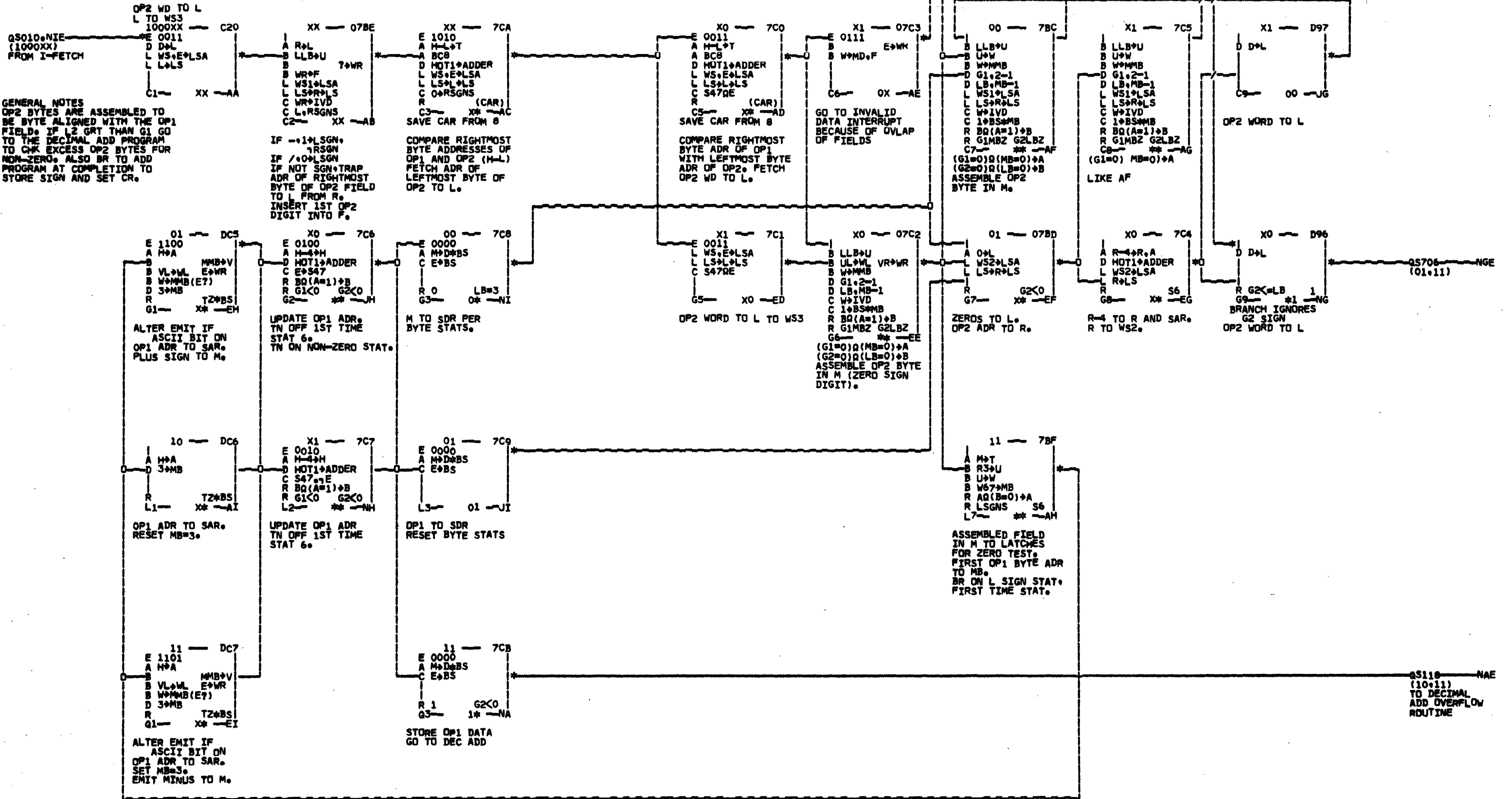


20090

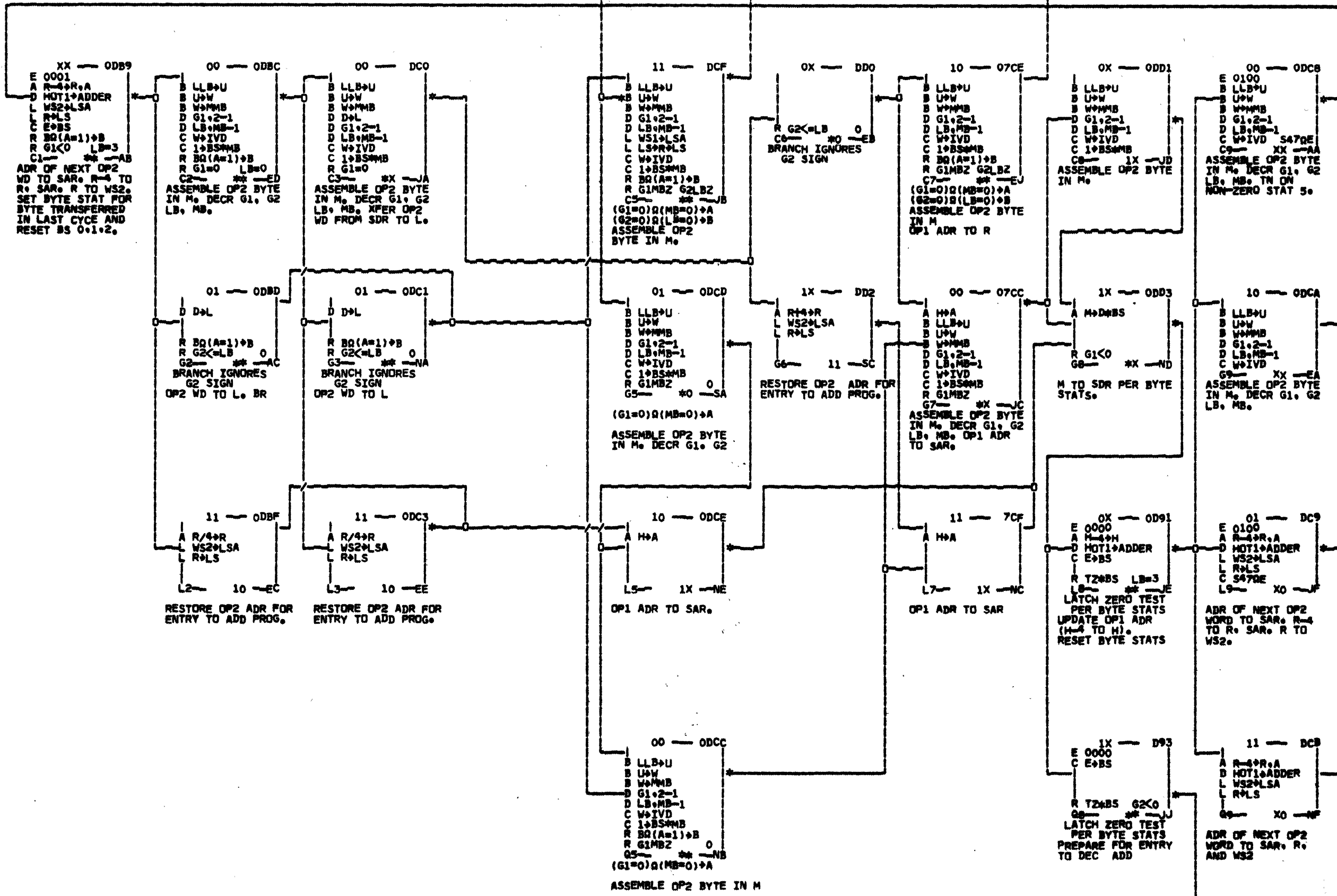
Q5706.JFE
(X0)

Q5706.JBD
(00+01+11)

Q5706.AED
(OX)
TO INTERRUPT
ROUTINE



30445



XX ODB9
 E 0001
 A R-4→R.A
 D NOT1→ADDER
 L WS2→LSA
 L R→LS
 C E→BS
 R BQ(A=1)→B
 R G1<0 L=3
 C1 → AB
 ADR OF NEXT OP2
 WD TO SAR. R-4 TO
 R. SAR. R TO WS2.
 SET BYTE STAT FOR
 BYTE TRANSFERRED
 IN LAST CYC AND
 RESET BS 0.1.2.

00 ODBC
 B LLB→U
 B U→W
 B W→M
 D G1.2-1
 D LB→MB-1
 C W→IVD
 C 1→BS→MB
 R BQ(A=1)→B
 R G1=0 LB=0
 C2 → ED
 ASSEMBLE OP2 BYTE
 IN M. DECR G1, G2
 LB, MB.

00 DCO
 B LLB→U
 B U→W
 B W→M
 D G1.2-1
 D LB→MB-1
 C W→IVD
 C 1→BS→MB
 R G1=0
 C3 → JA
 ASSEMBLE OP2 BYTE
 IN M. DECR G1, G2
 LB, MB. XFER OP2
 WD FROM SDR TO L.

11 DCF
 B LLB→U
 B U→W
 B W→M
 D G1.2-1
 D LB→MB-1
 L WS1→LSA
 L LS→R→LS
 C W→IVD
 C 1→BS→MB
 R BQ(A=1)→B
 R G1MBZ G2LBZ
 C5 → JB
 (G1=0)Q(MB=0)→A
 (G2=0)Q(LB=0)→B
 ASSEMBLE OP2
 BYTE IN M.

0X DDO
 R G2<LB 0
 C6 → EB
 BRANCH IGNORES
 G2 SIGN

10 07CE
 B LLB→U
 B U→W
 B W→M
 D G1.2-1
 D LB→MB-1
 C W→IVD
 C 1→BS→MB
 R BQ(A=1)→B
 R G1MBZ G2LBZ
 C7 → EJ
 (G1=0)Q(MB=0)→A
 (G2=0)Q(LB=0)→B
 ASSEMBLE OP2 BYTE
 IN M
 OP1 ADR TO R

0X ODD1
 B LLB→U
 B U→W
 B W→M
 D G1.2-1
 D LB→MB-1
 C W→IVD
 C 1→BS→MB
 C8 → JD
 ASSEMBLE OP2 BYTE
 IN M.

00 ODCB
 E 0100
 B LLB→U
 B U→W
 B W→M
 D G1.2-1
 D LB→MB-1
 C W→IVD S47QE
 C9 → AA
 ASSEMBLE OP2 BYTE
 IN M. DECR G1, G2
 LB, MB. TN ON
 NON-ZERO STAT 5.

01 ODBD
 D D→L
 R BQ(A=1)→B
 R G2<LB 0
 G2 → AC
 BRANCH IGNORES
 G2 SIGN
 OP2 WD TO L. BR

01 ODC1
 D D→L
 R BQ(A=1)→B
 R G2<LB 0
 G3 → NA
 BRANCH IGNORES
 G2 SIGN
 OP2 WD TO L

01 ODCD
 B LLB→U
 B U→W
 B W→M
 D G1.2-1
 D LB→MB-1
 C W→IVD
 C 1→BS→MB
 R G1MBZ 0
 G5 → SA
 (G1=0)Q(MB=0)→A
 ASSEMBLE OP2 BYTE
 IN M. DECR G1, G2

1X DD2
 A R-4→R
 L WS2→LSA
 L R→LS
 G6 → SC
 RESTORE OP2 ADR FOR
 ENTRY TO ADD PROG.

00 07CC
 A H→A
 B LLB→U
 B U→W
 B W→M
 D G1.2-1
 D LB→MB-1
 C W→IVD
 C 1→BS→MB
 R G1MBZ
 G7 → JC
 ASSEMBLE OP2 BYTE
 IN M. DECR G1, G2
 LB, MB. OP1 ADR
 TO SAR.

1X ODD3
 A M→D→BS
 R G1<0
 G8 → ND
 M TO SDR PER BYTE
 STATS.

10 ODCA
 B LLB→U
 B U→W
 B W→M
 D G1.2-1
 D LB→MB-1
 C W→IVD
 G9 → EA
 ASSEMBLE OP2 BYTE
 IN M. DECR G1, G2
 LB, MB.

11 ODBF
 A R-4→R
 L WS2→LSA
 L R→LS
 L2 → EC
 RESTORE OP2 ADR FOR
 ENTRY TO ADD PROG.

11 ODC3
 A R-4→R
 L WS2→LSA
 L R→LS
 L3 → EE
 RESTORE OP2 ADR FOR
 ENTRY TO ADD PROG.

10 ODCE
 A H→A
 L5 → NE
 OP1 ADR TO SAR.

11 7CF
 A H→A
 L7 → NC
 OP1 ADR TO SAR

0X OD91
 E 0000
 A R-4→R
 D NOT1→ADDER
 C E→BS
 R T2→BS LB=3
 L8 → E
 LATCH ZERO TEST
 PER BYTE STATS
 UPDATE OP1 ADR
 (H-4 TO H).
 RESET BYTE STATS

01 DC9
 E 0100
 A R-4→R.A
 D NOT1→ADDER
 L WS2→LSA
 L R→LS
 C S47QE
 L9 → X0
 ADR OF NEXT OP2
 WORD TO SAR. R-4
 TO R. SAR. R TO
 WS2.

11 ODC
 B LLB→U
 B U→W
 B W→M
 D G1.2-1
 D LB→MB-1
 C W→IVD
 C 1→BS→MB
 R BQ(A=1)→B
 R G1MBZ 0
 Q5 → NB
 (G1=0)Q(MB=0)→A
 ASSEMBLE OP2 BYTE IN M

1X D93
 E 0000
 C E→BS
 R T2→BS G2<0
 G8 → J
 LATCH ZERO TEST
 PER BYTE STATS
 PREPARE FOR ENTRY
 TO DEC ADD

11 DCB
 A R-4→R.A
 D NOT1→ADDER
 L WS2→LSA
 L R→LS
 G9 → X0
 ADR OF NEXT OP2
 WORD TO SAR. R.
 AND WS2

6-6168