GA22-7060-3
File No. S370-01

Systems

IBM 3033
Functional Characteristics

Third Edition (January 1979)
This edition obsoletes GA22-7060-2 and Technical Newsletter GN22-0565. Each significant technical change to the text or to an illustration is indicated by a vertical line to the left of the change. This edition includes material about the IBM 3033 Attached Processor Complex. Changes are continually made to the information herein; before using this publication in connection with the operation of IBM equipment, consult the *IBM System/370 Bibliography*, GC20-0001, for editions that are applicable and current.

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This manual describes the functional characteristics and features of the IBM 3033 Processor Complex, 3033 Attached Processor Complex, and 3033 Multiprocessor Complex. For management, programming, and operations personnel experienced in System/370 operation, this manual provides a fundamental understanding of each of the 3033 complexes.

The reader should have an understanding of data processing systems, including a fundamental knowledge of the IBM System/370 as defined in *IBM System/370 Principles of Operation,* GA22-7000.

Only information that is of particular concern to the users of the 3033 is discussed.

This publication contains six chapters and two appendixes:

- Chapter 1 introduces the 3033 Processor Complex, 3033 Attached Processor Complex, and 3033 Multiprocessor Complex, and describes their highlights from several aspects.
- Chapter 2 describes the standard and optional features.
- Chapter 3 describes the logical elements of the 3033 Processor from the viewpoint of function.
- Chapter 4 describes the controls and functions of the IBM 3036 Console Model 1.
- Chapter 5 describes the processor's channel characteristics, expanding on the channel information presented in Chapter 3.
- Chapter 6 describes the characteristics of the IBM 3033 Attached Processor Complex and Multiprocessor Complex, particularly how they differ from the 3033 Processor Complex.
- Appendix A contains a glossary and the abbreviations used in the manual.
- Appendix B contains deviations from the *IBM System/370 Principles of Operation*, GA22-7000, and the *IBM System/360 and System/370 I/O Interface Channel to Control Unit, Original Equipment Manufacturers' Information,* GA22-6974.

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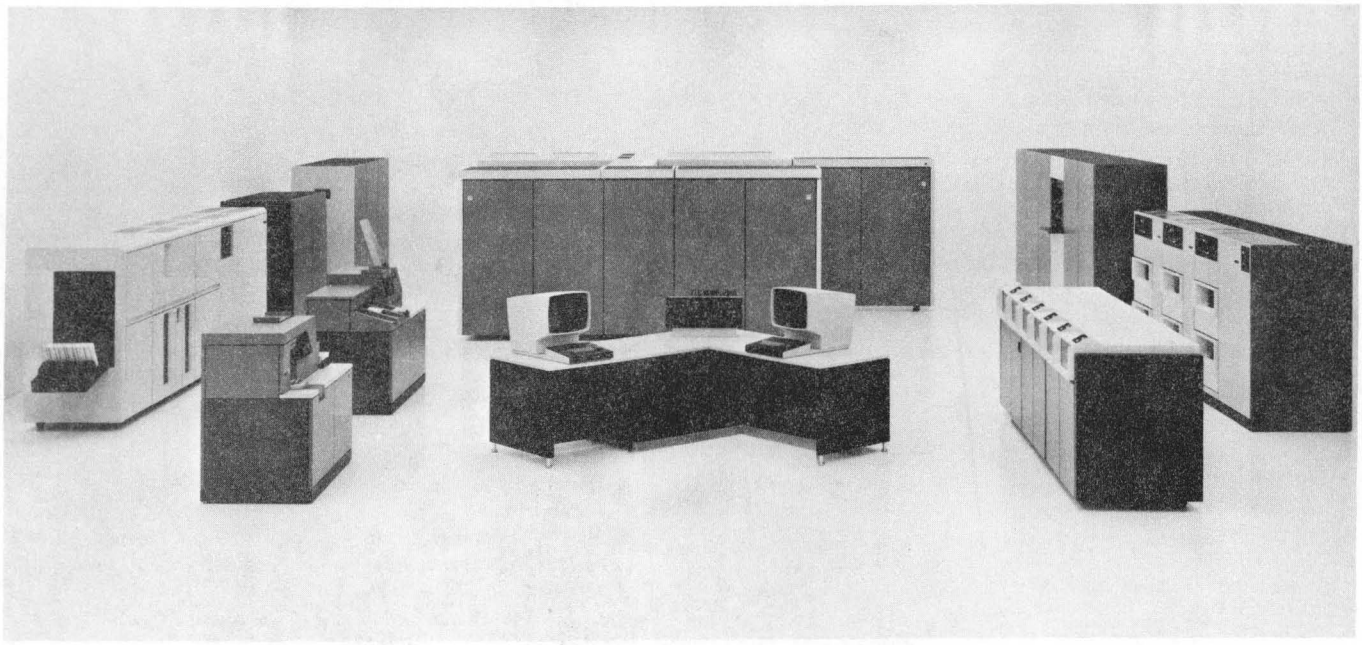
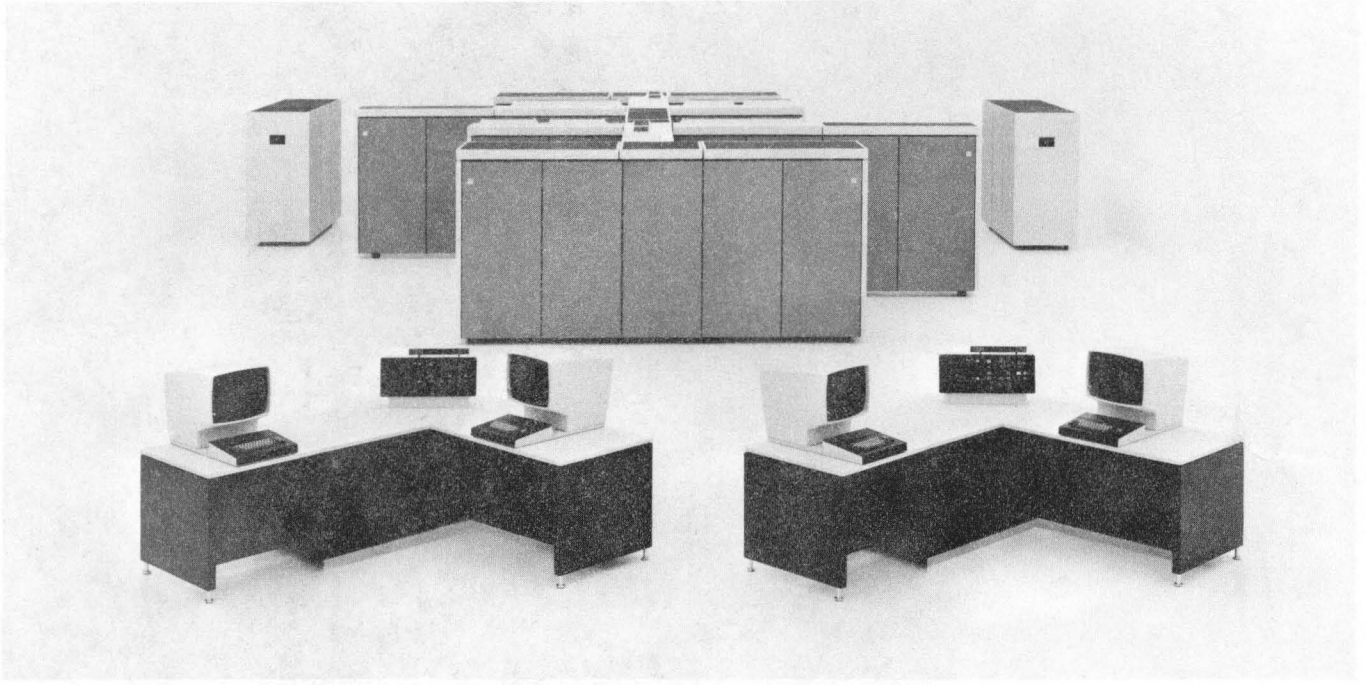


IBM 3033 Processor Complex with Representative Input/Output Devices (Design Models)



IBM 3033 Multiprocessor Complex (Design Models)

Chapter 1. Introduction

PROCESSOR COMPLEX HIGHLIGHTS

The IBM 3033 Processor Complex (Figure 1-1) expands the System/370 product line for high-speed, large-scale scientific and business applications, and provides an improved growth path for large-system users. The 3033's high efficiency, speed, and power result primarily from the use of large-capacity processor storage, dynamic address translation, and high-speed monolithic circuit technology, and from concurrent operations. The use of integrated channels and monolithic circuitry also significantly reduces system space requirements.

The 3033 Processor Complex consists of the IBM 3033 Processor, the IBM 3036 Console, and the IBM 3037 Power and Coolant Distribution Unit.

The 3033 Processor:

- Has a basic machine cycle time of 57 nanoseconds
- Has processor storage capacity of 4M, 8M, 12M, or 16M bytes (M equal to 1,048,576)
- Has a 64K-byte (65,536-byte) high-speed buffer that significantly reduces the effective storage access time
- Provides eight-way storage interleaving
- Overlaps the operations of instruction preprocessing and execution

ATTACHED PROCESSOR COMPLEX HIGHLIGHTS

The IBM 3033 Attached Processor Complex (Figure 1-1) has the advantages of the 3033 Processor Complex and, in addition, provides the user with significantly increased processing capability. In this complex, an IBM 3042 Attached Processor is physically and logically coupled to an A-series IBM 3033 Processor through an IBM 3038 Multiprocessor Communication Unit (MCU), which provides for coordination and communication between the two processors. Using just one system control program and the processor storage and channels of the 3033 Processor, the two processors can execute programs concurrently.

The attached processor complex is described in more detail in Chapter 6, particularly in how it differs from the 3033 Processor Complex.

MULTIPROCESSOR COMPLEX HIGHLIGHTS

The IBM 3033 Multiprocessor Complex (Figure 1-1) has the advantages of the 3033 Processor Complex and, in addition, can provide users with enhanced performance and availability. Essentially, this complex is made up of two 3033 Processor Complexes physically and logically joined through an IBM 3038 Multiprocessor Communication Unit, which provides for coordination and communication between the processors. Using the same system control programming, the two processors can execute programs simultaneously while sharing processor storage and data. The multiprocessor complex is described in more detail in Chapter 6, particularly in how it differs from the 3033 Processor Complex.

PROGRAMMING COMPATIBILITY

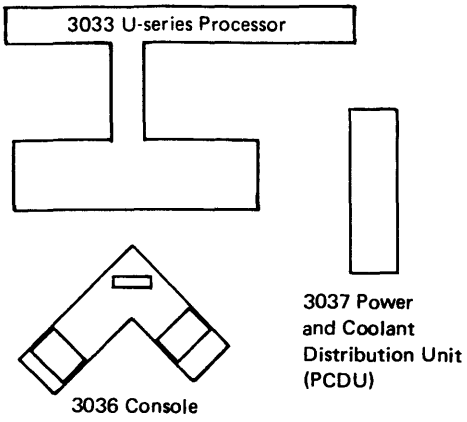
Any program written for System/370 operates in an IBM 3033 Processor Complex, Attached Processor Complex, or Multiprocessor Complex, provided that it:

- Does not depend on system facilities (such as storage capacity, I/O devices, or optional features) being present when the facilities are not included in the configuration. (For example, since the 3033 has volatile main storage, the program must not depend on data in main storage being preserved after system power goes off and is then restored.)
- Is not time dependent.
- Does not depend on results or functions defined in the *IBM System/370 Principles of Operation* to be unpredictable or model dependent.
- Does not depend on results or functions that are defined in this manual to be deviations from the *IBM System/370 Principles of Operation.* (See Appendix B for a description of the deviations.)
- Does not depend on system facilities being absent when the facilities are included in the 3033. (For example, the program should not depend on interruptions caused by the use of operation codes or command codes that in some models are not assigned or not installed.)
- Takes into account the fact that the Read Direct and Write Direct instructions, if used, require real addresses instead of logical addresses if the Invalidate Page Table Entry instruction is installed.

Any program written for System/360 operates in a 3033, if it follows the preceding rules and does not depend on functions that differ between System/360 and System/370. The System/370 functions that differ from System/360 functions are described in detail in Appendix B of the *IBM System/370 Principles of Operation.*

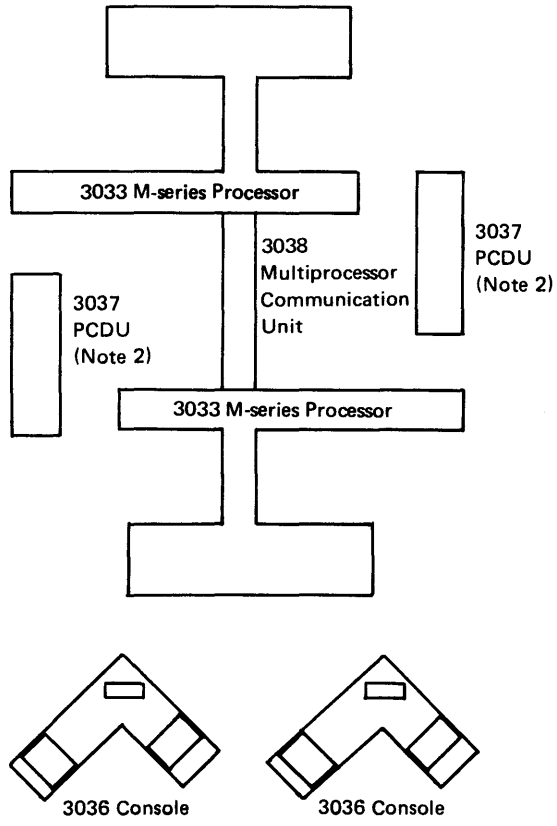
For more details about compatibility, refer to the *IBM System/370 Principles of Operation.*

IBM 3033 Processor Complex

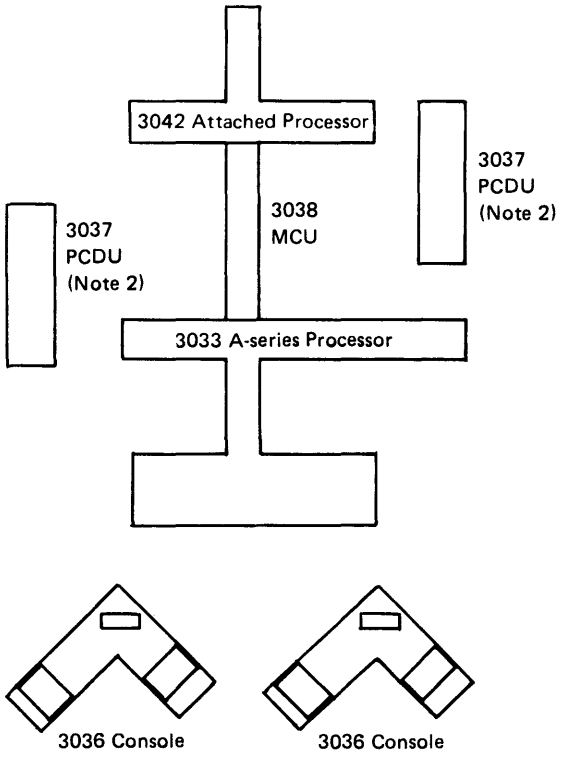


IBM 3033 Multiprocessor Complex

(Note 1)



IBM 3033 Attached Processor Complex



Notes:

1. In an MP system, each processor has at least 4M bytes of processor storage. In MP mode, as many as 16M bytes can be online at one time. In UP mode, as many as 16M bytes can be configured to each processor.
2. Each 3037 is equipped with a multiprocessing feature.

Figure 1-1. Representative 3033 Plan Views

SYSTEM CONTROL PROGRAMS

System control programs available for the 3033 complexes are as follows:

- For the 3033 Processor Complex:
  Single virtual storage (SVS)
  Multiple virtual storage (MVS)
  IBM Virtual Machine Facility/370 (VM/370)
  Operating System/Virtual Storage 1 (OS/VS1)
- For the 3033 Attached Processor Complex:
  MVS
  VM/370
- For the 3033 Multiprocessor Complex:
  MVS

SYSTEM EXTENSIONS PROGRAM PRODUCTS

Throughput can be improved through use of either of two system extensions program products:

- MVS/System Extensions program product, which enhances the performance and control of MVS and uses the System/370 extended facility.
- VM/System Extensions program product, which enhances the performance and control of VM/370.

DATA SECURITY

Data security is maintained through:

- Storage protection
- Console security keylock

Storage Protection

Both store protection and fetch protection are included. If store protection is violated, data is not stored into the protected area. If fetch protection is violated, data is not retrieved from the protected area of storage. Additional protection is provided for certain storage locations vital to operating-system availability.

Console Security Keylock

The console security key fits the console security keylock located on the right-hand side of the display. When the security key is removed or is in the vertical position, system data security is placed under program control. The operator is restricted to the currently displayed frame. Attempting to change frames causes an alarm to sound.

DATA VALIDITY

Data validity is maintained through:

- Data parity checking
- Storage error checking and correction (ECC)
- Instruction retry
- Channel retry
- CPU ID

Data Parity Checking

All data transfers, arithmetic operations, and logical operations include parity checking. Detection of even parity causes a machine-check interruption, when this type of interruption is allowed.

Storage Error Checking and Correction

When the processor storage control function (PSCF) is operating in diagnostic parity mode, each data byte in processor storage is maintained with odd parity. During store operations, data is checked for odd parity before it is stored. During read operations, data is checked as it is read out of storage. A machine check is signaled if even parity is detected. When the PSCF is operating in ECC mode, each doubleword includes an ECC check byte, which replaces the parity bits. The ECC check byte is used to detect and correct all single-bit errors and to detect all double-bit errors and some other multiple-bit errors. The ECC check byte is generated during store operations. All detections and corrections occur during read operations.

Instruction Retry

If a machine error is detected during instruction execution or interruption handling, an attempt is made to retry the instruction or interruption sequence. When retry is successful, the results are valid. When retry is not successful, no results are made available.

Channel Retry

If a machine error is detected during channel operations, the channel director that detects the error then attempts to retry the channel function when possible. For situations that cannot be retried, the channel requests an I/O interruption to indicate the error.

CPU ID

A CPU identifier (ID) is available for logouts and the Store CPU ID instruction.

VIRTUAL STORAGE

When the 3033 Processor is operating in extended control (EC) mode with dynamic address translation (DAT) invoked, all logical addresses within the System/370 24-bit addressing structure are available, regardless of the real storage capacity. Therefore, the maximum logical (virtual) address is 16777215.

The 3033 Processor, which supports the use of virtual storage, is not subject to the restraints normally imposed on programming applications by the amount of available real storage. Consequently, the operational flexibility of the installation is enhanced.

RELIABILITY, AVAILABILITY, AND SERVICEABILITY

System interruptions are reduced through automatic recovery facilities such as channel retry, instruction retry, and error checking and correction (ECC) for storage.

Availability is enhanced through reduction of system interruptions and through improved serviceability features, such as the concurrent service capability provided with the IBM 3036 Console. This capability permits customer engineers (CEs) to diagnose a failing channel group, for example, while the operator continues to use the rest of the system.

Availability of processing in the 3033 AP and MP Complexes is greater than that in the 3033 Processor Complex, and is discussed in Chapter 6 under "Processing Availability."

Chapter 2. Standard and Optional Features

The 3033 Processor and 3042 Attached Processor have numerous standard features. The 3033 Processor also offers several optional features. Figure 2-1 provides a concise view of the major standard and optional features.

Many of the standard and optional features are briefly described in this section. The *IBM System/370 Principles of Operation,* GA22-7000, describes most of the features in detail.

Some of the feature descriptions in this section may be better understood when considered with the function, element, or facility with which they are most closely associated.

STANDARD FEATURES

System/370 Universal Instruction Set

The System/370 universal instruction set contains 156 instructions and includes features such as key-controlled storage protection, byte-oriented operand, interval timer, time-of-day clock, and monitoring.

Key-Controlled Storage Protection

Key-controlled storage protection (for both stores and fetches) makes it possible to protect the contents of processor storage from undesired destruction or unauthorized use. Storage protection includes the privileged instructions Insert Storage Key (ISK) and Set Storage Key (SSK).

Byte-Oriented Operand

The byte-oriented operand allows the user to ignore, in part, the restriction that all operands in processor storage be aligned on integral boundaries (for example, halfword operands on halfword boundaries). A significant amount of programming time can be saved by using this feature, but performance is slightly degraded when it is used excessively.

Interval Timer

The interval timer is a counter that generates an external interruption request whenever it decrements to a negative value. The timer has a 15.5-hour cycle and a 3.33-millisecond resolution.

Time-of-Day (TOD) Clock

The TOD clock provides a consistent measure of elapsed time suitable for indication of time and date. The clock is updated each microsecond. Clock operation is not affected by system resets or by any system activity other than turn-off of power or execution of the Set Clock instruction. The clock runs when a processor is either in the wait state or stopped state, and when a processor is executing programs.

Monitoring

Monitoring, with the Monitor Call (MC) instruction, provides a means of selectively recording designated events in the execution of a program.

Limited Channel Logout

Limited channel logout allows the storing of detailed channel error information for recovery from channel errors.

Extended Channel Logout

Extended channel logout allows the storing of detailed channel-error information in a storage area designated by a pointer.

Extended-Precision Floating Point

Extended-precision floating point includes instructions that handle extended-precision (28 hexadecimal-digit) floating-point operands. Extended-precision operands may also be rounded off to long-precision operands, and long-precision operands may be rounded off to short-precision operands.

Direct Control

The direct-control feature provides the two privileged instructions Read Direct (RDD) and Write Direct (WRD), as well as six external interruption lines. The read and write instructions provide for the transfer of a single byte of information between an external device and processor storage. When active, each of the external signal lines sets up the conditions for an external interruption. When used with a 3033, these instructions use real addresses rather than logical addresses. For more information, see the *IBM System/360 and System/370 Direct Control and External Interruption Features, OEMI,* GA22-6845.

Processors: IBM 3033 Processor and IBM 3042 Attached Processor

Basic Machine Cycle Time: 57 nanoseconds

3033 and 3042 Standard Features

System/370 universal instruction set
Key-controlled storage protection
Byte-oriented operand
Interval timer
Time-of-day (TOD) clock
Monitoring
Extended-precision floating point
Direct control
CPU timer
Clock comparator
Dynamic address translation (DAT)
Program event recording
Extended control mode
System/370 extended facility
Recovery extensions
PSW key handling
Conditional swapping
Channel-set switching (not on U-series 3033 Processor)
High-speed buffer storage
Clear I/O
Instruction retry
Storage configuration control

3033-Only Standard Features

Channel retry
Command retry
Fast release
High-speed transfer
Channel indirect data addressing
Limited channel logout
Extended channel logout
Byte-multiplexer channels (Notes 1, 2, 3, and 4)
Block-multiplexer channels (Notes 1, 3, 4, and 5)

3033-Only Optional Features

Channel-to-channel adapter (Note 6)
Two-byte interface
Extended channels (Note 3)

Figure 2-1. IBM 3033 Configuration Guide

Processor Storage: Part of IBM 3033 Processor

Processor Model	*Storage Capacity (Bytes)*
A4, U4, M4	4M (4,194,304)
A8, U8, M8	8M (8,388,608)
A12, U12, M12	12M (12,582,912)
A16, U16, M16	16M (16,777,216)

Notes:

1. Attach as many as eight control units.
2. Operate in either burst mode or byte mode; multiplexing capability on bytes, groups of bytes, or blocks.
3. Each of the two standard channel groups provides one byte-multiplexer channel and five block-multiplexer channels. The optional extended channels feature provides a third channel group having either four block-multiplexer channels or three block-multiplexer channels and one byte-multiplexer channel.
4. Subchannels per standard channel group are as follows:

Byte-Multiplexer Subchannels		Block-Multiplexer Subchannels	
Without Sharing	With Sharing	Without Sharing	With Sharing
256	256 nonshared less 8, 16, or 32 for each subchannel configured for sharing.	1,280	Up to 40 per channel group. (Note 3)

5. Operate in burst mode only; multiplexing capability on blocks or multiple blocks.
6. The channel-to-channel adapter (two per system, attached to a byte- or block-multiplexer channel) permits interconnection of two channels. One control-unit position on a 3033 Processor channel can connect to one control-unit position on any other System/370 (or System/360) channel. Only one adapter is needed per connection; it counts as one control unit on both channels.

CPU Timer

The CPU timer provides a means for measuring elapsed processor time and for causing an external interruption when a prespecified length of time has elapsed. Unlike the TOD clock, the CPU timer does not run when the processor is in the stopped state but does provide accurate measurement of elapsed processor time.

Clock Comparator

The clock comparator causes an external interruption when the TOD clock reaches a value specified by the program.

Dynamic Address Translation

Dynamic address translation (DAT) provides the means for translating virtual addresses to absolute addresses. DAT is described in greater detail under "Processor Storage Control Function" in Chapter 3.

Channel Indirect Data Addressing

Channels do not use dynamic address translation. Channel command words (CCWs) in virtual storage must be translated by the control program before execution. This feature allows contiguous areas of virtual storage to be mapped into noncontiguous areas of real storage.

Program Event Recording

Program event recording (PER) is a valuable program debugging aid. It is enabled by turning on bit 1 of the EC-mode program status word (PSW). Control registers 9-11 control the selection of registers and storage locations. Note that processor performance is slightly decreased when PER is monitoring for instruction fetches.

Extended Control Mode

Extended control (EC) mode permits use of system facilities and functions not available with basic control (BC) mode, such as dynamic address translation and program event recording. EC mode is implemented with a modified PSW format and with permanently assigned areas of processor storage.

System/370 Extended Facility

The System/370 extended facility enhances the capabilities and performance of a 3033 MVS system when used with the MVS/System Extensions (MVS/SE) program product. This facility includes:

1. Low-address protection, whose use improves system reliability, availability, and serviceability by increasing the protection of low-address main storage (addresses 0 through 511) vital to the system control program.
2. The Invalidate Page Table Entry (IPTE) instruction and the common-segment bit, which increase the efficiency of dynamic address translation.
3. The Test Protection (TPROT) instruction, which performs tests for potential protection violations without causing program interruptions for protection exceptions.
4. The SVC Assist instruction, which reduces the time needed to enter MVS supervisory services, thereby improving processor performance.
5. The Fix Page instruction, six tracing instructions, and four lock-handling instructions, whose use improves processor performance.
6. Virtual-machine extended-facility assist, which permits the preceding 12 MVS/SE-dependent instructions (in items 4 and 5) to be executed directly by the virtual machine without requiring program interruptions, eliminating the need for simulation, thereby improving processor performance.

For more detailed information, see the *IBM System/370 Extended Facility,* GA22-7072.

Recovery Extensions

Recovery extensions consist of:

- The Clear Channel (CLRCH) instruction, which performs an I/O system reset in a channel and on the I/O interface associated with the channel.
- Machine-check extensions, consisting of a machine-check external damage code and an extended damage code validity bit, which provide a detailed indication of the cause of external damage.
- Limited channel logout extensions, consisting of two additional logout bits, which indicate whether the I/O interface is operative and whether the logout is valid.

PSW Key Handling

PSW key handling makes available the instructions Set PSW Key from Address (SPKA) and Insert PSW Key (IPK).

Conditional Swapping

Conditional swapping makes available the instructions Compare and Swap (CS) and Compare Double and Swap (CDS).

Command Retry

Command retry is a procedure initiated by the control unit to retry channel commands. No I/O interruptions are required. The number of retries is device dependent.

Fast Release

Fast release provides for early release of the processor by a channel during execution of the Start I/O Fast Release instruction. Fast release reduces the processor delay associated with the initiation of the I/O operation.

Clear I/O

Clear I/O provides the CLRIO function called for by the privileged instruction Clear I/O (CLRIO). The function causes discontinuance of the current operation with the addressed I/O device.

High-Speed Transfer

High-speed transfer, a feature for block-multiplexer channels, permits an increase of data transfer rates.

Storage Configuration Control

Storage configuration control permits processor storage to be configured from the console in 2M-byte (2,097,152-byte) increments.

Descriptions of Other Standard Features

The following features listed in Figure 2-1, but not described in this chapter, are described in Chapter 3:

- High-speed buffer storage in "High-Speed Buffer Storage"
- Instruction retry in "Instruction Retry"
- Channel retry in "Channel Retry"
- Byte-multiplexer channels in "Byte-Multiplexer Channels"
- Block-multiplexer channels in "Block-Multiplexer Channels"

Channel-set switching is described in Chapter 6 under "Processing Availability."

OPTIONAL FEATURES

The following optional features may be added to a 3033 Processor to provide additional facilities:

- Two-byte interface
- Channel-to-channel adapter
- Extended channels

Two-Byte Interface

The two-byte interface feature expands the channel interface to I/O and storage devices. The feature may be installed on the first block-multiplexer channel in each channel group. With the feature installed, the channel can accommodate a 3-megabyte per second data transfer rate by handling two bytes at a time instead of one.

Channel-to-Channel Adapter

The channel-to-channel adapter provides the data path and the synchronization for data transfers between two channels. This adapter, which runs in selector mode, can be connected to any type of channel on any System/360 or System/370. To a channel, the adapter appears as a control unit and responds to either channel the same as a control unit.

The adapter normally is connected between channels associated with different processors, thus establishing a loosely coupled multiprocessing system.

The data rate for an adapter is limited by the slower of the two communicating channels.

Extended Channels

Four additional channels (12 through 15) may be added as a group. These channels may be either all block multiplexer, or three block multiplexer and one byte multiplexer. These channels do not change the aggregate data rate of the other two channel groups. The two-byte interface feature is also available for the additional channels.

The IBM 3033 Processor has a 64K-byte (65,536-byte) high-speed buffer and includes the following logical elements (Figure 3-1):

- Instruction preprocessing function (IPPF)
- Execution function (E-function)
- Processor storage control function (PSCF)
- Maintenance function
- Processor storage (4,194,304 bytes in the basic 3033)
- 12 channels (six per channel group or director)

The naming of these logical elements is intended to aid understanding, but does not necessarily indicate separate packaging or isolated operation.

The IPPF fetches instructions and prepares them for execution by the E-function, determines priority, and makes fetch requests for operands.

The E-function executes the arithmetic and logical functions of the System/370 instructions.

The PSCF processes all requests for access to processor storage for storing data or fetching data, and converts virtual addresses into absolute storage addresses.

The maintenance function provides for instruction retry, processor resets, processing rate controls, processor trace function, and processor/console interaction for service and manual operations.

Processor storage provides real storage for the system.

The channels direct the flow of data between I/O devices and processor storage, relieve the processor of the task of communicating directly with the devices, and permit data processing to proceed concurrently with I/O operations.

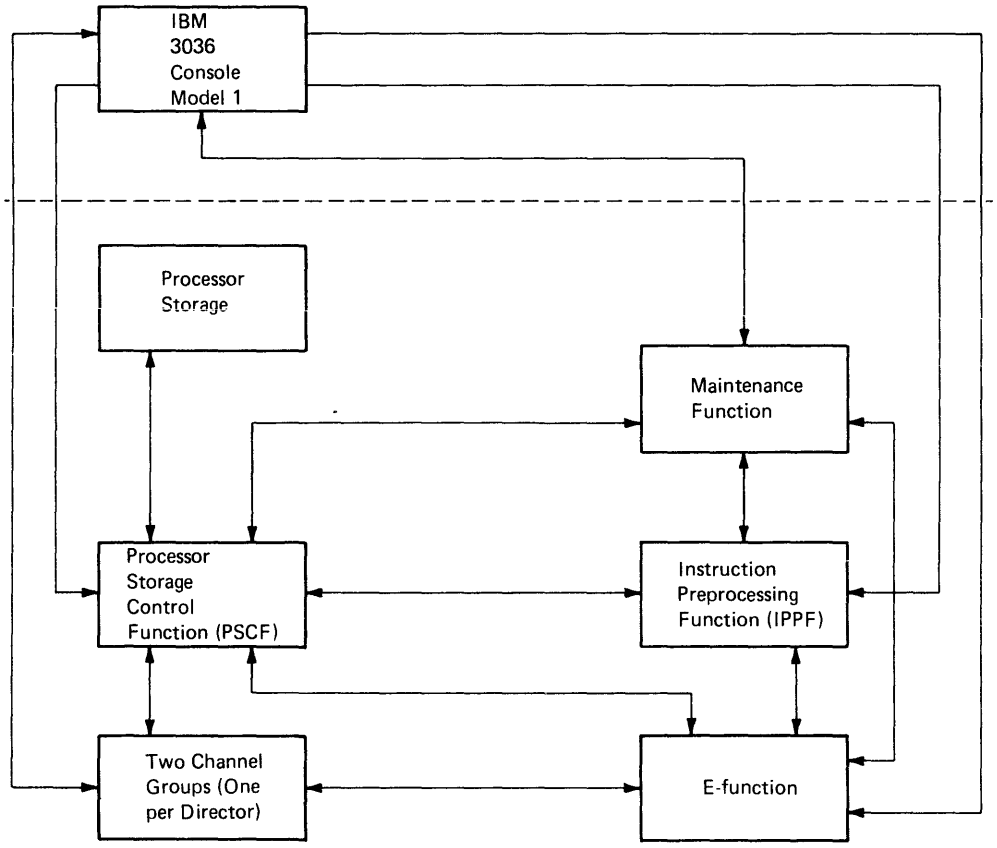


Figure 3-1. Logical Structure of the Basic IBM 3033 Processor with the IBM 3036 Console Model 1

INSTRUCTION PREPROCESSING FUNCTION

The IPPF fetches instructions and prepares them for execution by the E-function. In doing this, the IPPF performs several other functions, which include:

- Buffering as many as three instruction streams (the original stream and up to two branch streams) concurrently
- Estimating the success of branches
- Placing instructions in a queue and, when needed, taking them out in proper sequence for execution
- Pretesting instruction and operand addresses for exceptions
- Determining priority of storage requests made by the IPPF
- Making store and fetch requests for instructions and operands

The IPPF can process several instructions concurrently by dividing the processing of each instruction into multiple sequential steps, and performing these steps in assembly-line fashion.

The IPPF uses a variety of means to perform its operations. These means include:

Fifteen general registers, which duplicate the low-order three bytes of general registers 1-15 of the E-function, thereby permitting instruction decoding and address generation to be performed in the same machine cycle.

Three instruction buffers (each four doublewords wide), which temporarily hold prefetched nondecoded instructions.

An instruction register, which holds an instruction during its decoding.

Four instruction queuing registers, each of which can hold a decoded instruction ready for the E-function.

A 24-bit adder, which can accept three inputs and perform address calculations during decoding.

Six operand address registers, each of which can retain a calculated operand address for the E-function.

Three instruction address registers, each of which holds an address associated with one of the three instruction streams.

An address incrementer, which is used for calculating instruction addresses when needed, updating the instruction address registers needed for fetching instructions, stepping addresses through operand fields when those fields are prefetched by the IPPF, and performing address updates called for by the E-function.

A length incrementer, which is used for computing the end address of storage operands. End addresses may be used in testing for overlapped fields and/or for test fetches to look for access exceptions.

The IPPF detects and signals the E-function about the following interruption conditions:

- A specification due to an odd-numbered instruction address
- Access exceptions related to instruction fetching
- Access exceptions related to operand fetching
- PER instruction-fetching events
- PER storage-alteration events

E-FUNCTION

The E-function executes System/370 instructions. To support instruction execution, the E-function buffers the operands required for the execution, and either loads the results into local storage registers or initiates the storing of the results into processor storage.

The E-function also:

- Initiates channel and I/O operations
- Swaps PSWs for interruptions
- Provides the system timing facilities
- Provides the PSW and control registers used in controlling the system
- Handles direct-control communications
- Retries instructions and interruptions when retry controls permit it

E-function circuitry and facilities are shared by the maintenance function.

Control Storage

The E-function provides control storage that contains the microprograms used to control various E-function operations. Control storage contains 3,072 words (each with 108 bits) and 1,024 words (each with 126 bits) and is accessed once each machine cycle. This storage is not available for programming use.

Control storage is loaded by either a power on or a load control-storage request from the appropriate console display frame. Control storage is volatile; it therefore must be reloaded whenever power is interrupted.

PROCESSOR STORAGE CONTROL FUNCTION

The processor storage control function (PSCF) controls and processes all requests for storing data into processor storage or fetching data from it, and translates virtual addresses to absolute storage addresses by means of the dynamic address translation (DAT) facility.

Included within the PSCF are:

- High-speed buffer storage
- Translator
- Translation lookaside buffer (TLB)
- Channel bus controller

High-Speed Buffer Storage

Buffer storage provides high-speed access to instructions and data. A fetch from the buffer takes less than one-fourth of the time required for the same fetch from processor storage. Buffer action is transparent to the user. Although the buffer holds only a portion of processor storage contents, the objective of the buffer is to contain the portion that the program is currently using.

The high-speed buffer holds recently accessed storage data and is updated frequently. Buffer storage, with a 64K-byte capacity, is divided into 64-byte (eight-doubleword) blocks. (Default to a 32K-byte capacity is discussed briefly in the last paragraph of this description of buffer storage.) The buffer is conceptually organized into 64 columns, each containing 16 blocks (Figure 3-2). Correspondingly, processor storage is also conceptually organized into 64 columns, but the number of blocks in each column varies with the size of processor storage.

During system operation, a correspondence is set up that relates each block in buffer storage to a block in the corresponding column of processor storage. Each time the IPPF makes a fetch, buffer storage control determines whether there is an assigned buffer block corresponding to the addressed processor storage block. If none is found, then:

1. One of the 64-byte buffer blocks is automatically assigned to the processor storage block that was addressed.
2. The block address is placed in the buffer block's address array.
3. A buffer storage block load is requested.

While the block is being fetched, the address is made invalid until the fetch is complete.

When an IPPF or maintenance-function fetch initiates a block load, eight 8-byte overlapped accesses to processor storage are required. The first processor storage location selected is the one containing the data addressed. When the location is available, the data is sent directly to the IPPF and is also loaded into buffer storage. The remaining overlapped processor storage fetches needed to complete the block load are made one at a time on each succeeding cycle, if the required storage elements are not busy.

For a channel store operation, a check is made to determine whether the referenced data is in buffer storage; if it is, the buffer storage data is invalidated, and processor storage data is updated. If the referenced data is not in the applicable buffer storage, only processor storage is updated. Channel fetch requests are made only to processor storage.

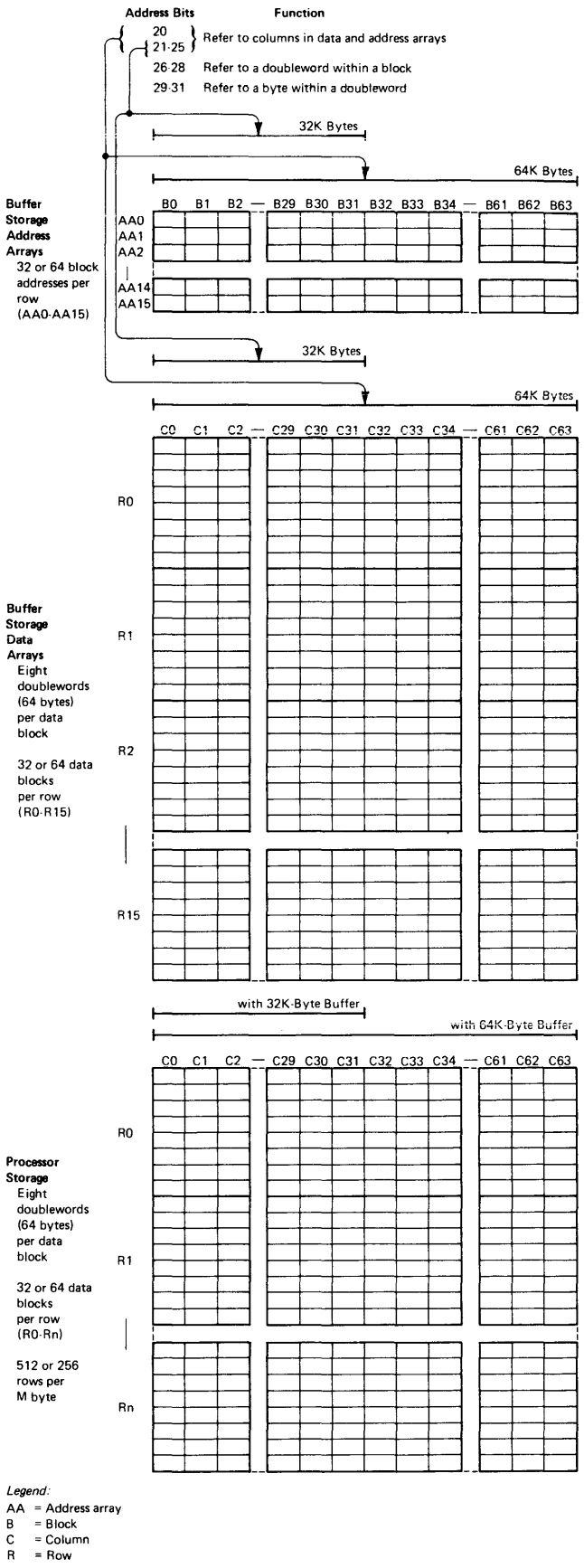


Figure 3-2. Organization of Buffer Storage and Processor Storage

Because buffer storage can contain only a portion of processor storage data at one time, any buffer block can be reassigned to any other block of the corresponding column in processor storage. Priority of reassignment is based on usage. Each time data within a buffer block is referred to by an IPPF fetch, that group of blocks is logically moved to the top of a logic-controlled activity list. Intervening blocks are logically moved down one position to fill the vacated slot. Note, however, that the logical movement of a block within the list involves no data transfer. When all 16 buffer blocks within a column are assigned and the IPPF makes a fetch request to a corresponding storage location not yet in buffer storage, a buffer block in the group lowest on the activity list is cleared and reassigned to the referenced processor storage block.

Store operations always update processor storage, but buffer storage is not updated unless the referenced processor storage block has a corresponding buffer storage block assigned. In summary, store operations do not cause reassignment, loading of a buffer storage block, or changing of the buffer storage block activity list.

The 64K-byte buffer is used in both basic control mode and extended control mode. When used in extended control mode with DAT active, 4K-byte paging is recommended. If a user's system control program requires 2K-byte paging, the buffer defaults to 32K-byte capacity. The buffer is automatically reset to 64K bytes when the system reverts to 4K-byte paging.

Translator

The translator translates virtual addresses to absolute addresses when the system is in DAT mode and during the execution of the Load Real Address (LRA) instruction. The translator also holds addresses for TLB searches and updates.

Translation Lookaside Buffer

To reduce the virtual-to-absolute address translation time once a translation is completed, the absolute address of a referenced page is stored in a group of registers called the translation lookaside buffer (TLB). Each absolute address stored in the TLB is identified as belonging to a particular virtual address by:

- The location in the TLB into which the absolute address is stored
- Storing bits 8-14 of the virtual address into the TLB entry

Thus, the TLB contains up to 128 virtual-absolute address pairs. Subsequent translations for the same addresses, and their multiple processor-storage references, are avoided because the absolute address required is available immediately from the TLB.

TLB Operation

Each virtual address supplied by the program causes access to both the high-speed buffer (to examine the address of data contained) and the TLB (to determine whether the absolute address and protection key are there).

If the virtual address has been previously translated, and its absolute address now resides in the TLB, then the address *may* be resolved in one machine cycle and have the data available on the following cycle. The absolute address is compared with addresses read out of the high-speed buffer address array to determine whether the data field required is there. The absolute address is also used to access processor storage if the operation requires it.

If the virtual address either has or has not been previously translated, but does not currently reside in the TLB, then a full translation must take place; the virtual address is translated and the TLB is updated with the newly translated address. Assuming no I/O interference, 10 to 40 machine cycles are required, depending on the locations of the segment- and page-table entries required for the translation.

The TLB can be purged with the program by issuing a Purge TLB (PTLB) instruction. The TLB may also be purged either by using SYSTEM RESET on the Operator display frame (OP frame), or by a system-generated reset.

TLB Operation Example: Assume that a given virtual address is requested by the IPPF.

Virtual address bits 9-20 select the entry line in the TLB. Virtual address bits 8-14 are compared against the entry from the TLB. If the TLB compare is unsuccessful, a full translation is performed. Before going to processor storage to do the full translation, a determination is made to see whether the required translation entries (or any part of them) are in the buffer. If they are, the translation is made, using the buffer entries. If only part (or none) of the entries is in the buffer, then part (or all) of the translation is made, using processor storage.

If the TLB compare is successful, no translation is required and the absolute address is transferred from the TLB to the buffer address array to determine whether the entry is in the buffer. This ultimately determines whether the fetch is made from the buffer or from processor storage.

Channel Bus Controller

The channel bus controller coordinates, processes, and controls all channel director requests for access to storage. The channel director of each channel group originates all such requests. To coordinate realtime storage requests from the channel directors with other PSCF requests, channel data is temporarily held in buffers. All channel addresses are real and therefore do not require translation.

MAINTENANCE FUNCTION

The maintenance function provides the buffering and restoring of the 3033's instruction retry, and provides for processor/console interaction for most service and manual operations.

Instruction Retry

The ability to recover from intermittent failures is provided through retry techniques, which increase the reliability of the 3033. Source data is saved before it is altered during an operation, thus making instruction retry possible. When an error is detected, a microprogram routine causes the E-function to return to the beginning of the operation or to a point in the operation that was correctly executed; the operation is then resumed. Retry procedures use both additional processor hardware and the retry microprograms.

Most operations in the basic processor can be retried. A machine-check error during I-fetch causes the I-fetch to be retried. The manner in which the instruction is retried depends on the instruction. Some instructions do not change the original data in the registers until the last cycle of execution; these instructions are retried from the beginning. Other instructions change source data in the registers and are retried from a checkpoint, using the intermediate results.

If an error occurs during the execution of an I/O instruction, the execution is checked to determine whether the instruction retry threshold has been passed. If the instruction execution has not passed this threshold, the instruction is retried automatically, without program assistance. For recording purposes, a machine-check interruption is taken at the completion of a successful retry.

If an I/O-instruction execution has progressed too far to be retried, an I/O interruption may be taken, or the condition code may be set to indicate that a CSW and limited channel logout (LCL) have been stored because the I/O operation was not started. The appropriate device-dependent error recovery routine can be scheduled to take the required recovery action. Usually, if an error in the execution of the Start I/O instruction occurs before the I/O device becomes involved on the I/O interface, instruction retry is still possible.

PROCESSOR STORAGE

Processor storage provides each 3033 Processor with eight-way interleaved real storage and is available in a choice of four capacities:

4M (4,194,304) bytes
8M (8,388,608) bytes
12M (12,582,912) bytes
16M (16,777,216) bytes

The 4M-byte capacity is standard.

Processor storage has a storage distribution element (SDE) that contains the logic for fetching or storing doublewords into the data arrays. The SDE and data arrays are divided into eight storage elements, so that storage operations may be overlapped by selecting different elements during each machine cycle.

Error checking and correction (ECC) bits are stored in the data arrays, along with the data. In a fetch operation, the ECC bits detect and correct single-bit errors, and detect double-bit errors.

Storage Protection

Storage protection prevents unauthorized access of information stored in processor storage. Each 2K (2,048) bytes of storage is protected by one of 15 possible key values (key bits 0-3). For store operations, protection-key bits 0-3 from the currently active PSW are compared with storage-key bits 0-3 from the processor storage protection array. If the keys do not match, the PSCF is notified of a protection violation, and the data is not stored. The same protection is active for processor storage fetch operations if bit 4 (the fetch-protect bit) is on.

The TLB holds the two protection keys corresponding to each 4K-byte absolute-address boundary held in the TLB tables. When the TLB does not have the absolute address and key, a protection check must be made. After the check is made, processor storage sends the keys to the TLB, so that checking can be done by the TLB the next time the same real address occurs.

Each protection key has a corresponding reference (R) bit and change (C) bit. The R-bit is turned on each time data is fetched from the corresponding 2K-byte block of storage. Both bits are turned on each time data is stored into the corresponding 2K-byte block of storage. Also, both bits indicate (to the storage management supervisor program) which pages of storage:

- Are not being used, and therefore can be replaced
- Have been altered and must be saved on an auxiliary storage device before being replaced in storage

CHANNELS

The 3033 Processor has integrated channels requiring less floor space than do stand-alone channels. The basic 3033 Processor has 12 channels, grouped into two sets of six channels. Each set of six channels is controlled by a channel director. Channel addresses are fixed, and therefore are not reassignable. Each of these two sets of channels has one byte-multiplexer channel and five block-multiplexer channels.

If more channels are needed, the extended channels feature is available. This optional feature permits the addition of another channel director with channels (four block multiplexer, or three block multiplexer and one byte multiplexer). This increases the number of block-multiplexer channels to either 13 or 14 and the total number of channels to 16.

Another optional feature (the two-byte interface) permits two block-multiplexer channels to have a two-byte data path rather than a one-byte data path. If the extended channels feature is installed, a third block-multiplexer channel may also have a two-byte data path.

The directors control all channel activity of the 3033 Processor, including channel-to-storage communications and channel-to-device communications.

Each block-multiplexer channel includes a group of registers and controls needed to maintain data transfer between I/O devices and storage once the data transfer operation begins.

Each director shares reloadable control storage (RCS) with the channels associated with it. Each director and each channel operates within its own microprogram, and shares logic by switching control at specified points in the microprograms. This change in control can be described as a break-in. When a break-in occurs, the current microprogram is halted temporarily while another microprogram is given control.

Block-Multiplexer Channels

Block-multiplexer channels are both microprogram controlled and hardware controlled. I/O-command execution, device-selection initiation, and interruptions are microprogram controlled, whereas interface data handling and command-chaining reselection are hardware controlled. The channel is under microprogram control for processor-storage data transfers.

Byte-Multiplexer Channels

Byte-multiplexer channels are microprogram controlled for I/O-command execution, interface data transfer, and interruptions, but are hardware controlled for device selection. Upon request by a device for service, the channel breaks in on the director, takes control with its own address register, services the device, sets up the conditions for subsequent break-ins for further service to the device, and eventually restores control to the director.

Any block-multiplexer channel can break in on a byte-multiplexer channel, so long as the break-in is not inhibited by the executing microprogram.

Because the byte-multiplexer channel can service several devices in byte mode, unit control words (UCWs) are available on a device-address basis.

Channel Retry

Channel retry enables each channel to retry channel functions when an error occurs. The information needed to retry channel functions is provided by affected channels and is held in a pair of microprogram-controlled registers called the threshold register and the retry-code register.

Channel Performance

Block-Multiplexer Channels

Each block-multiplexer channel may attain a data rate of 1.5 megabytes per second. A block-multiplexer channel with a bus extension feature installed may attain a data rate of 3.0 megabytes per second.

Channels 1 through 5 of each basic channel group can operate in a disconnected command-chaining mode (referred to as block multiplexing), which causes the channel to disconnect a device at channel-end time if command chaining occurs. During the interval between channel end and device end, another device on the channel can be started or can complete data transfer for an operation started earlier.

Byte-Multiplexer Channels

Byte-multiplexer channel performance is highly dependent on I/O-device interface transition response times. These device delays show wide variations among the devices attachable to a byte-multiplexer channel. Another factor to be considered in performance calculations is the effect of block-multiplexer channel interference, because block-multiplexer channel routines can always break in on a byte-multiplexer channel routine.

Note: For information on channel characteristics, see Chapter 5.

The IBM 3036 Console (Figure 4-1) is a two-station stand-alone unit that provides the manual control functions needed to:

- Select modes
- Display console messages and system information
- Enter data manually into the system
- Monitor and control system power

The console provides two physically separate operating stations. The dual-station design permits concurrent service and system operation. Each station is individually addressable and has a CRT display, a keyboard, a diskette drive, a microprogrammed console processor, and an I/O interface.

A control panel permits configuration for selecting station activity. The position of the display and keyboard on the right (console A) is fixed. However, the display and keyboard of the station on the left (console B) can be turned clockwise as much as 190° from their normal position. This permits them to be used from the other side of the console, thereby facilitating some service operations.

One station is selected to be used primarily for manual control of the operating system and is called the operator console. The other station then becomes the one used for monitoring and manually controlling the processor and channels, and is called the service support console.

Either one may be used by the operator or a customer engineer (CE). If one station becomes inoperative, the other may be used to continue operations. When the console is in maintenance mode, the operator can operate the system from one station, and a CE can run microdiagnostic programs on a portion of the system from the other station.

OPERATOR CONTROLS

The operator controls include the keyboard, control panel, display, and security keylock.

Keyboard

The keyboard (Figure 4-2) provides alphabetic characters A through Z (both uppercase and lowercase), numbers 0 through 9, and 26 graphic characters. In addition, eight keys are provided for cursor control, and eight keys provide additional special functions.

The keyboard provides the primary means of manually interacting with the system for certain functions. When a character is entered via the keyboard, that character is recognized by the console processor and is executed. The

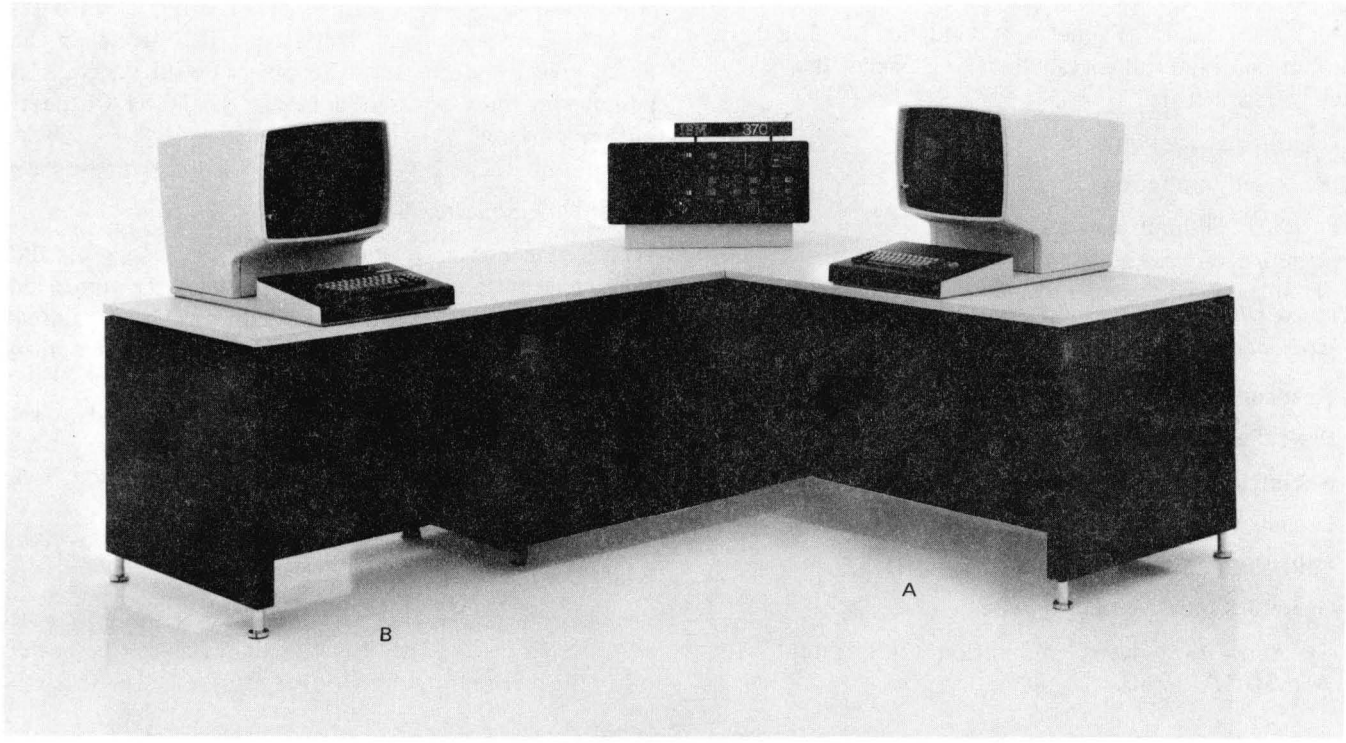


Figure 4-1. IBM 3036 Console Model 1 (Design Model)

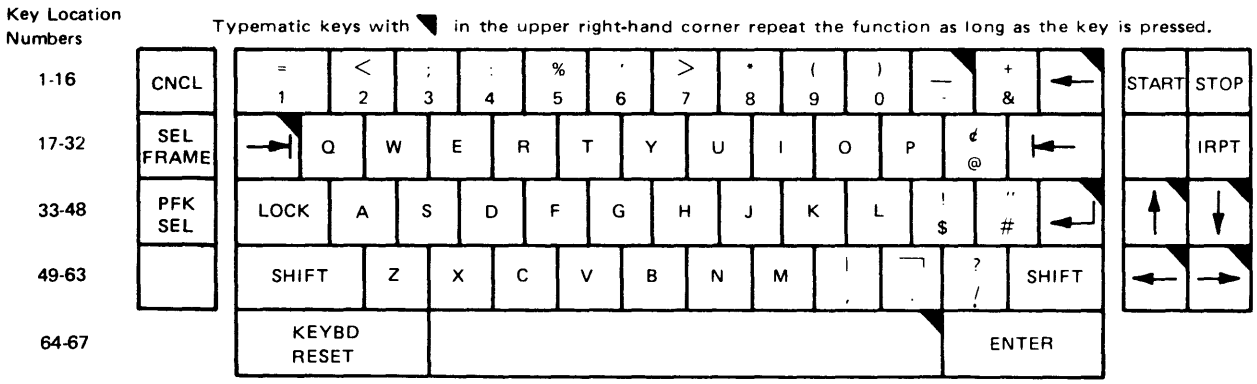


Figure 4-2. Console Keyboard

operator and service personnel functions for any particular display frame can be activated by entering the character for a desired function. When the character is entered, the microprogram invokes the appropriate routine to provide the action required. For example, the operator can invoke the restart function by displaying the Operator (OP) display frame and by entering the characters assigned to the restart function. The console processor then begins a restart.

Note that the key location numbers (1-67) run from far left to far right, and from top to bottom.

The function of each of the keys is shown in Figure 4-3. Some of the functions vary according to which frame is active.

Control Panel

The control panel (Figure 4-4) contains the switches, pushbuttons, and other functions not included on the keyboard, which are:

- Unit Emergency switch
- IPC Reset pushbutton
- Power On pushbutton (backlighted)
- Power Off pushbutton
- Power Off Pending indicator
- IMPL Pending indicator
- Microcode Power Control indicator
- Power Select switch
- I/O Interface switches (one for each console)
- Diagnostic on IMPL switches (one for each console)
- IMPL pushbuttons (one for each console)
- Operator Console on IMPL switch
- TP Active–Key Reset pushbutton (backlighted) with Activate TP keylock
- TOD Clock switch
- Alarm Volume control
- Meters
- Key switch for control of the meters

Unit Emergency Switch

When pushed down, the Unit Emergency switch quickly turns off all power to the console and processor, but not to the motor generator for the power distribution function of the 3037 PCDU.

When pushed down, this switch latches in the down position until it is reset by a customer engineer (CE).

IPC Reset Pushbutton

When console power is turned off, the IPC Reset pushbutton resets any power fault latches that are set in the initial power control (IPC). To power up the system, this pushbutton must be pressed before the Power On pushbutton is pressed.

Power On Pushbutton

Pressing the Power On pushbutton, after pressing the IPC Reset pushbutton, causes console power to be turned on and the microcode to be loaded into both console processors. If the Power Select switch is set to System, then the system is powered up; if this switch is set to Console, then only the console is powered up. When all power supplies are powered up and no check conditions exist, the console changes the backlighting of the pushbutton from red to white.

Power Off Pushbutton

Pressing the Power Off pushbutton starts the power-off sequence in the console. The console sequences the power off in the reverse order from power on.

Key Location Numbers	*Name*	*Description*
1	CNCL (Cancel)	Presents an attention interruption to the channel.
2-13, 19-29, 35-45, 51-60	Character Keys	Alphameric and special characters. (But keys 1 through 0, -, and & act as program function [PF] keys when the program [PR] frame is displayed and the PFK SEL key has been pressed.)
14	← (Backspace)	Moves the cursor backward one space.
15	START	Starts processor instruction execution.
16	STOP	Stops processor instruction execution.
17	SEL (Select) FRAME	Causes the selected frame to be displayed.
18	→| (Forward Tab)	Causes the cursor to space to the first character location of the next unprotected field. If the buffer is unformatted or if there are no unprotected fields, the cursor is repositioned to character location 0.
30	|← (Backward Tab)	If the cursor is located in the attribute character or the first alphameric character of an unprotected field or any character of a protected field, the cursor goes to the first alphameric character of the first preceding unprotected field. If the cursor is located in the character of an unprotected field other than the first, it is moved to the first character location of that field. If the buffer is unformatted or has no unprotected fields, the cursor is moved to character location 0.
32	IRPT (Interrupt)	Presents an external interruption to the processor.
33	PFK SEL (Select)	Makes keys 1 through 0, -, and & act as PF keys 1-12, while the program (PR) frame is displayed, until either a PF key or the KEYBD RESET key is pressed.
34	LOCK	Puts the keyboard in uppercase mode until the SHIFT key is pressed and released.
46	↵ (New Line)	If the buffer is formatted, then the cursor goes to the first unprotected character location of the next line containing unprotected characters. If there are no unprotected fields, the cursor goes to character position 0. If the buffer is unformatted, the cursor goes to the first character of the next line.
47,48, 62,63	↑ ↓ ← → (Cursor keys)	Control the horizontal and vertical movement of the cursor.
50,61	SHIFT	While this key is pressed, the keyboard is in uppercase mode.
64	KEYBD RESET	Resets the PFK SEL key, an inhibit keyboard condition, and a pending interruption condition, if the keyboard is not disabled because of an I/O operation in progress.
65-66	Spacebar	Enters a blank above the cursor location and moves the cursor forward one space. If the cursor was under a protected character, the keyboard becomes disabled.
67	ENTER	Causes an attention interruption on which device-independent display operator console support (DIDOCS) issues a Read Modified command to retrieve previously entered data.

Figure 4-3. Key Functions

Power Off Pending Indicator

Pressing the Power Off pushbutton turns on the Power Off Pending indicator and causes a power-off interruption to the console processor. When the console processor takes the interruption, system power is turned off.

IMPL Pending Indicator

The IMPL Pending indicator turns on during the power-on sequence, indicating that basic console power is available and that an initial microprogram load (IMPL) sequence was started.

Microcode Power Control Indicator

The Microcode Power Control indicator lights when the Power Select switch is turned to System, indicating that system power is under console control.

Power Select Switch

The Power Select switch determines whether power is turned on for the entire system or just for the console.

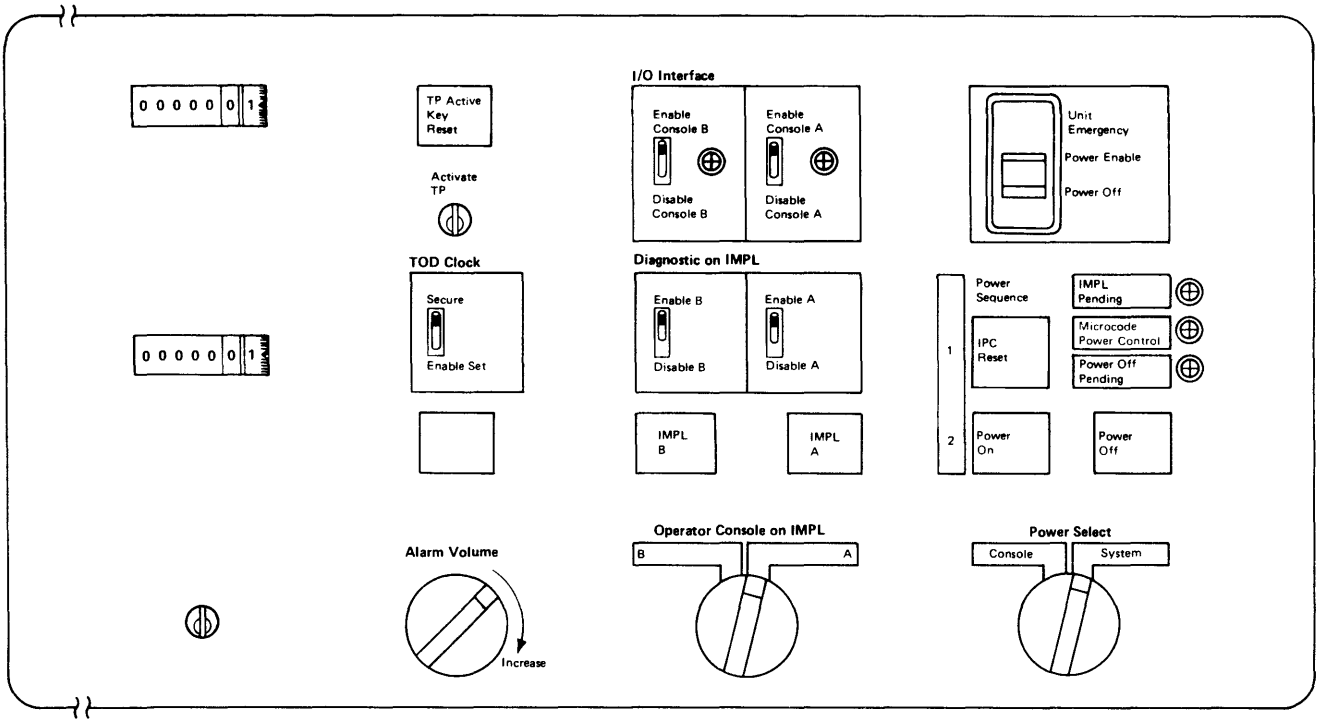


Figure 4-4. Control Panel of the IBM 3036 Console

I/O Interface Switches

Each of the two I/O Interface switches can either permit (enable) or inhibit (disable) the interface between the associated console and the corresponding channel. Both switches may be enabled at the same time.

Diagnostic on IMPL Switches

If the IMPL pushbutton for either console is pressed while the corresponding Diagnostic on IMPL switch is enabled, the console processor of the corresponding console executes the basic console microdiagnostic program before loading the control microprogram.

IMPL Pushbuttons

Pressing either the IMPL A or IMPL B pushbutton causes initial microprogram loading (IMPL) of the corresponding console, if that console's security key is turned on (horizontal). If the corresponding Diagnostic on IMPL switch is in the Enable position, console diagnostic programs can be run before the IMPL.

Operator Console on IMPL Switch

The Operator Console on IMPL switch is used in conjunction with the Configuration display frame (C1 frame) and the IMPL pushbuttons to reverse the configuration of the operator console and the service support console when required.

TP Active–Key Reset Pushbutton

The TP Active–Key Reset pushbutton is used in conjunction with the TP Link (TP) display frame for data communication (teleprocessing) operations. Enabling this pushbutton requires that the Activate TP key switch (located below the pushbutton) be turned on with the customer engineer (CE) key. When the key switch is turned on, the pushbutton is backlighted yellow, and the CE key may be removed. Pressing the pushbutton unlatches TP Active and causes all data communication operations to cease.

TOD Clock Switch

The TOD Clock switch provides an interlock, with the Set Clock (SCK) instruction, as a means of guarding against an improper change to the TOD clock. When the switch is held down, the instruction can change the clock. When this switch is in the normal (Secure) position, then the clock cannot be set and is referred to as being secure. The switch has a spring return; when released, it returns to the normal position.

Alarm Volume Control

The Alarm Volume control regulates the volume of the console alarm.

Meters and Key Switch

Two meters, which are not needed to operate the console, indicate time usage. The key switch, located below the meters, determines which meter is active.

Display

The display is the primary means for the system to communicate with the operator. The display operates in conjunction with the keyboard, which is the primary means for the operator to communicate with the system.

The display uses formatted display frames, each of which has a display area 25 lines long and 80 characters wide. The content of each display frame depends on its function. For example, the Operator (OP) frame (Figure 4-5) contains operator functions such as load, restart, system reset, and store status.

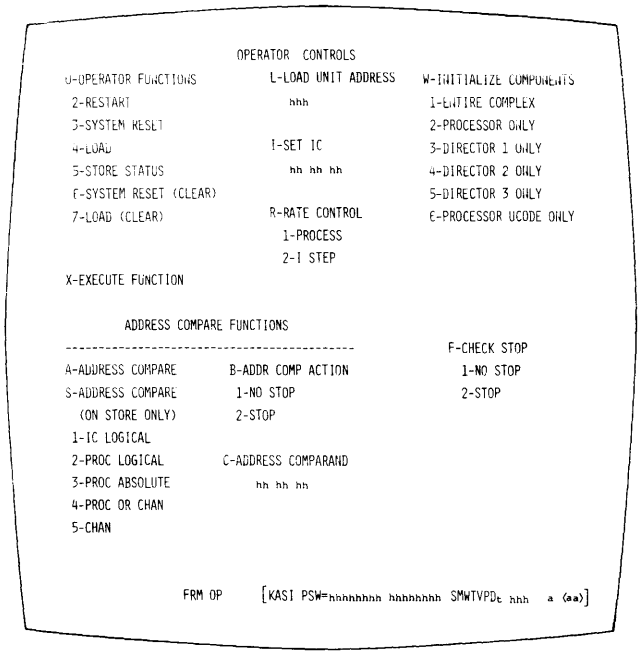


Figure 4-5. Operator (OP) Frame

Display Operation

All display operations use display frames, which are classed as either operator frames or service frames. Display frames are selected by the operator pressing the SEL FRAME key on the keyboard, then entering (keying in) the two-character frame identifier (ID). The operator frames are:

- Alter/Display (AD)
- Configuration (C1)
- Director Configuration (CD)
- Index (IN)
- Operator (OP)
- Program (PR)
- System Activity (SA)
- System Status Recording (SS)

Security Key

The security key fits the security keylock located on the right-hand side of each display. No frame changes are allowed if the security key is not turned on (horizontal). To be removed, the key must be turned off (vertical).

With the security key turned off or removed from either console, the IMPL pushbutton for that console is disabled, and system data security is under console microprogram control. The SEL FRAME key (on the keyboard) becomes inoperative, thereby precluding access to any other frames. By turning the security key on, the SEL FRAME key becomes operable and permits the operator to change the frame.

OPERATING-SYSTEM TERMINAL CHARACTERISTICS

The following information applies when a station is used as a terminal to communicate with the operating system.

Displaying the Program (PR) frame enables a programmer or operator to communicate with the operating system, which views the station as a terminal. Specifically, the station acts as an IBM 3277 Display Station Model 2, with a keyboard, attached to the system through an IBM 3272 Control Unit. Acting as such a terminal, the station obeys a subset of the 3277 commands and orders.

Commands

The station accepts the following commands:

Command	*Hexadecimal Code*
Test I/O (TIO)	00
Write	01
Read Buffer	02
No Operation (No-Op)	03
Sense	04
Erase/Write	05
Read Modified	06
Select	0B
Erase Unprotected	0F
Sound PDU/CDU Alarm	E3
Sense I/O	E4

The station rejects the following commands:

Copy	07
Diagnostic Write	09
Diagnostic Read	0A

Function Keys

The function keys are the KEYBD RESET key, the cursor control keys, and the forward and backward tab keys.

Program Access Keys

The program access keys are the ENTER key, the CNCL (cancel) key, and the program function (PF) keys.

Character Set

Ninety-six characters are specified for transfer to the station and for storage in the display buffer:

- 26 uppercase alphabetic characters (A-Z)
- 26 lowercase alphabetic characters (a-z)
- 10 numeric characters (0-9)
- Space
- 33 graphic characters (shown with their hexadecimal character codes)

Graphic Character	*Hexadecimal Code*	*Graphic Character*	*Hexadecimal Code*
¢	4A	↑	64
.	4B	↓	65
<	4C	→|	66
(	4D	|←	67
+	4E	↵	68
|	4F	,	6B
&	50	%	6C
!	5A	_	6D
$	5B	>	6E
*	5C	?	6F
)	5D	:	7A
;	5E	#	7B
¬	5F	@	7C
-	60	'	7D
/	61	=	7E
→	62	"	7F
←	63		

The station permits hexadecimal codes for four control-character representations and another graphic character. If the hexadecimal codes are transmitted to the display, they are stored in the buffer as data, but are displayed as blanks.

	Hexadecimal Code
NL (New Line)	15
EM (End of Medium)	19
DUP (Duplicate)	1C
FM (Field Mark)	1E
	6A

The display buffer does not provide for storage of hexadecimal character codes for any other characters or character representations. If other character codes are transferred to the display, the data characters stored and displayed are not defined. The character codes returned, as the result of a buffer read operation, may or may not be the same as the character codes transferred to the display.

Error Recovery Procedures

The 3277-2 error-recovery procedures apply to the station. They are described in the *IBM 3270 Information Display System Component Description*, GA27-2749.

CONSOLE CONFIGURATION

The two console processors can service as many as eight different access points (called *ports*) in different configurations, under control of a Configuration (C1) display frame in the service support console, as shown in Figure 4-6.

Console configuration also provides a means for system operation in case of failure of one of the console processors, displays, keyboards, I/O interfaces, or diskette drives. Special configuration for these conditions could result in a slight slowing of response to the operator when an exception condition (such as a channel error) occurs simultaneously with operator responses or requests. Configuration for these console conditions is referred to as maintenance mode.

The dedicated diskette drive on each console processor is the primary attached drive. The drive is also port-controlled and can be accessed by the console processor of either station. The primary drive is attached to its dedicated console processor on port 0. When the drive is accessed by the other console processor, the drive is attached to that console processor's port 1.

Normal Configuration

Figure 4-6 shows the normal configuration for the console.

Concurrent Service Configuration

The Configuration frame on the display also permits the console to be configured to provide service concurrent with system operations. Figure 4-7 shows the configuration for concurrent service of port 7.

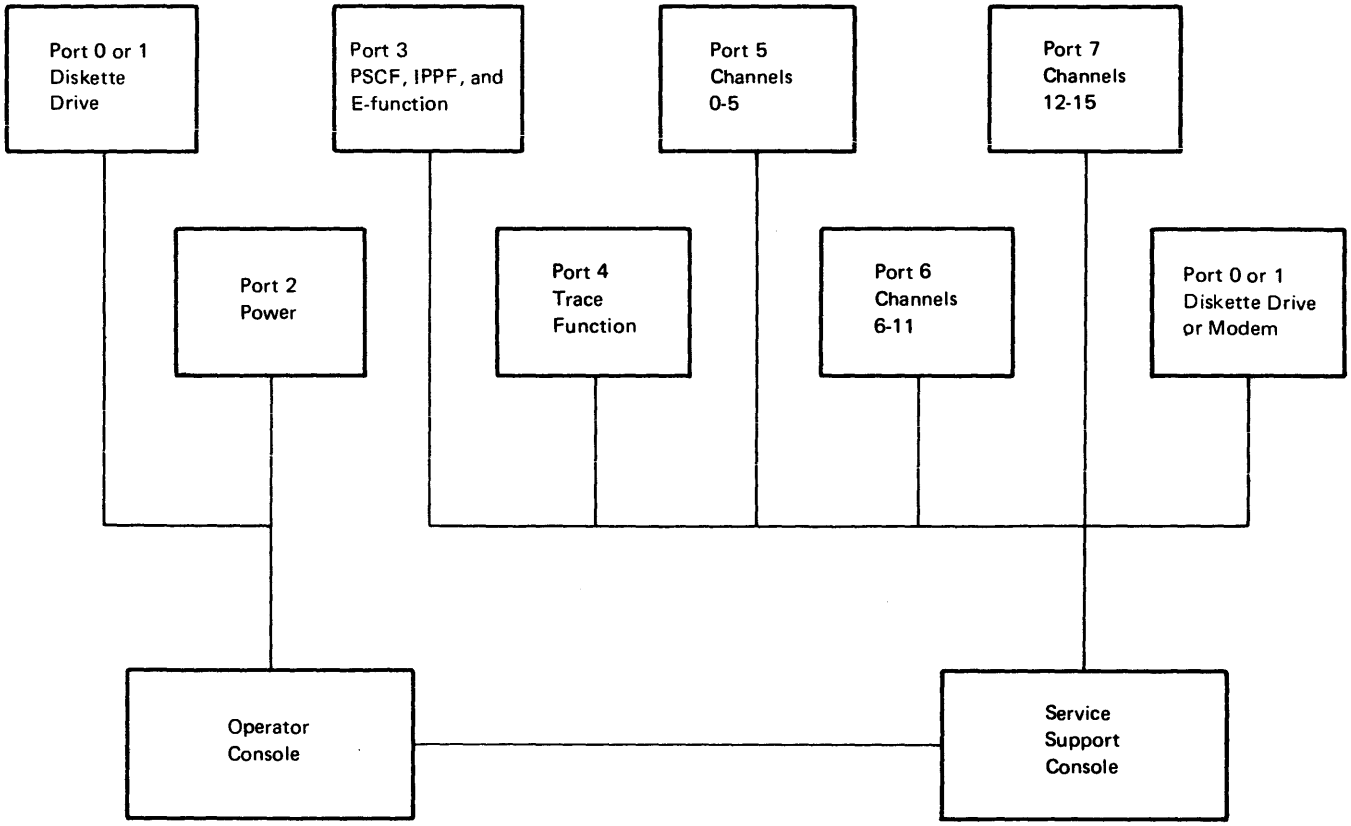


Figure 4-6. Normal Configuration

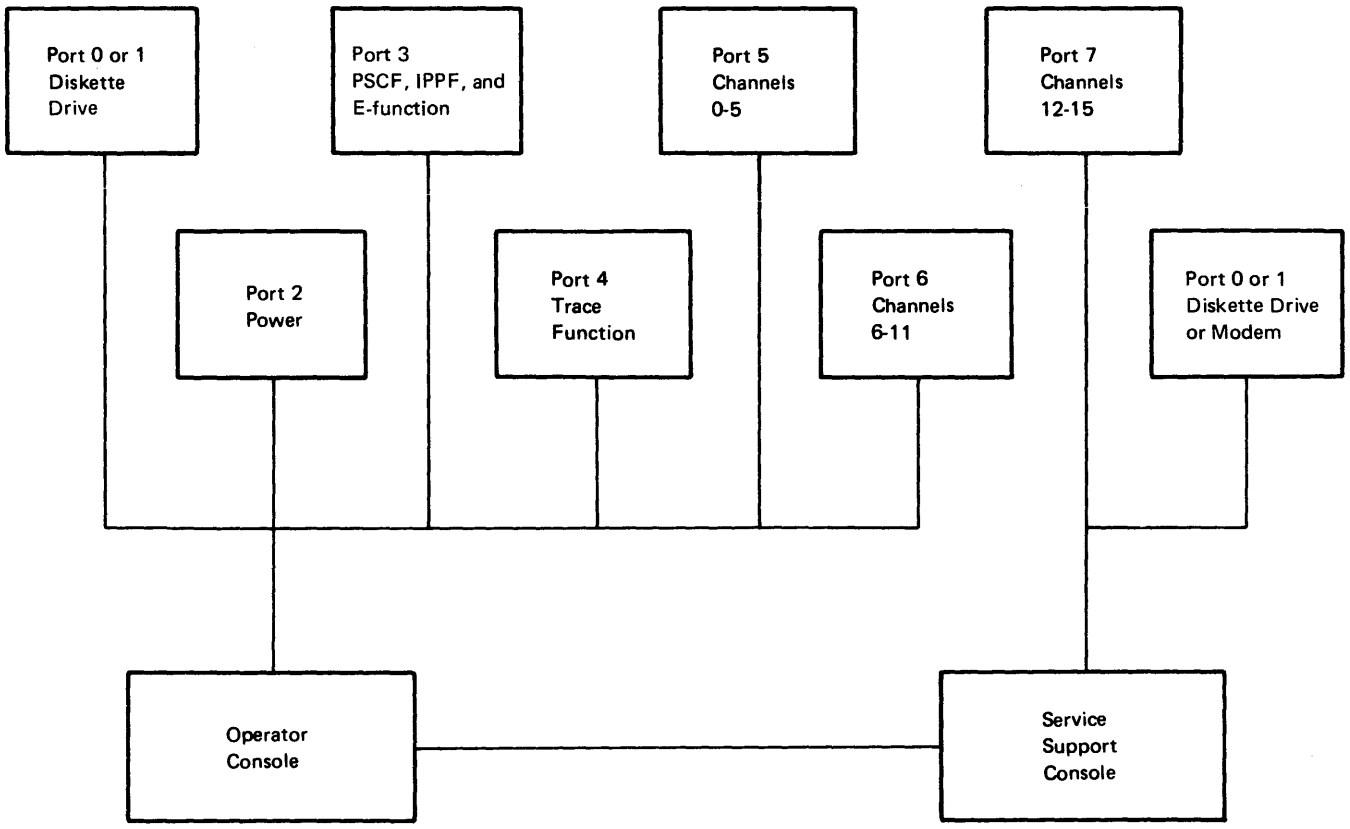


Figure 4-7. Configuration for Concurrent Service of Port 7

REMOTE SUPPORT FACILITY

If the system malfunctions, the remote support facility allows remote 3033 Processor support specialists to access machine maintenance data through a data communication (teleprocessing) network. The advantages of this support technique are evident; however, the customer's data security is subject to some exposure while the remote support facility is in use.

The security measures enlisted to ensure minimal exposure are as follows:

1. The customer's console security key is required to display the data-communication (teleprocessing) link display frame (TP frame).
2. The data-communication link is established only after thorough verification of the identity of both the customer and the remote support specialists.
3. Each mode of remote support (remote program, transmit logs/trace, and remote console) is initiated and identified at the customer's installation. Before establishing a data-communication link, service personnel must establish the customer's security level by selecting the remote options allowed by the customer. Any options selected are indicated on the TP frame by an asterisk to the left of the options selected. Any attempt to select unallowable options results in an error message on the TP frame.
4. Every operation initiated by the remote support specialists can be monitored by the customer.
5. The data-communication link can be disconnected at any time at the customer's installation by pressing the TP Active–Key Reset pushbutton on the control panel.

One of the following three modes of operation can be selected at the discretion of the service personnel and with the customer's approval:

1. *Remote Program*: This mode provides all of the online test executive program (OLTEP) security facilities. For example, to protect against accidental modification of customer data, OLTEP and OLTSEP diagnostic programs restrict writing to noncustomer volumes or to designated areas of customer volumes. Also, to protect against disclosure, OLTEP and OLTSEP diagnostic programs read and transmit the smallest amount of data that permits satisfactory diagnosis.
2. *Transmit Logs/Trace*: This mode allows the remote specialist to selectively copy the logout and trace data retained by the service support console for offline analysis.
3. *Remote Console*: In this mode, most console functions are available to the remote support specialists. The keyboard of the service support console is inoperative; however, the customer can terminate the operation by pressing the TP Active–Key Reset pushbutton on the control panel. Note that all modems on the system could be accessed by the remote support specialists; however, every operation initiated by the remote support specialists can be monitored by the customer.

All modes of operation are independent of operating system release levels. This facility does not depend on the processor, I/O devices, or channels being operational.

Chapter 5. Channel Characteristics

The channels transfer data between processor storage and I/O devices under control of a channel program executed independently of other operations being performed by the processor. The processor is free to resume its other operations after initiating an I/O operation.

At the end of an I/O operation, the channel signals an I/O interruption request to the processor. If not disallowed, an I/O interruption occurs that places the processor under control of the I/O new PSW. When I/O interruptions are disallowed, interruption requests are queued. Until honored, an I/O interruption condition is called a pending I/O interruption.

At the end of an I/O operation, a channel has information concerning the success of the operation, or has detailed information about any lack of success. This information is available to the control program.

Each channel group has facilities for performing the following functions:

- Accepting an I/O instruction from the processor
- Addressing the device specified by an I/O instruction
- Fetching the channel program from processor storage
- Decoding the channel command words (CCWs) that make up the channel program
- Testing each CCW for validity
- Executing CCW functions
- Placing control signals on the I/O interface
- Accepting control-response signals from the I/O interface
- Transferring data between an I/O device and processor storage
- Checking parity of bytes transferred
- Counting the number of bytes transferred
- Accepting status information from I/O devices
- Maintaining channel-status information
- Signaling interruption requests to the processor
- Sequencing interruption requests from I/O devices
- Sending status information to location 64 (decimal) when an interruption occurs
- Sending status information to location 64 (decimal) on processor request

CHANNEL CONTROL

A major feature of the channels is their common I/O interface connection to System/370 input/output control units. The I/O interface provides for attachment of a variety of I/O devices to a channel. The interface is governed by six basic channel commands and a common set of I/O instructions.

The I/O instructions are:

- *Start I/O,* which causes an operation to begin after a device is selected
- *Start I/O Fast Release,* which causes an operation to begin independently of device selection (when the SIOF function is performed)
- *Test Channel,* which elicits information about the addressed channel
- *Clear Channel,* which performs an I/O system reset in a channel and on the I/O interface associated with the channel
- *Test I/O,* which elicits information about a channel and a particular I/O device
- *Halt I/O,* which terminates any operation on the addressed channel, subchannel, or I/O device
- *Clear I/O,* which performs either the CLRIO function (causing discontinuance of the current operation with the addressed device) or the TIO function (described under Test I/O), depending on block-multiplexing control
- *Halt Device,* which terminates only operations associated with the addressed I/O device
- *Store Channel ID,* which places information identifying the designated channel in a specified location

All I/O instructions set the PSW condition code. Under certain conditions, all instructions except Test Channel may cause a channel status word (CSW) to be stored. Start I/O uses channel command words (CCWs).

A Start I/O instruction initiates execution of one or more I/O operations, and specifies a channel, a subchannel, a control unit, and an I/O device. Start I/O causes the channel to fetch the channel address word (CAW) from location 72 (decimal). The CAW contains the protection key and the address of the first channel command word (CCW) for the operation. The channel fetches and executes one or more CCWs, beginning with the first CCW specified by the CAW.

Six channel commands are used:

- Read
- Write
- Read Backward
- Control
- Sense
- Transfer in Channel

The first three commands are self-explanatory. Control commands specify such operations as set tape density, rewind tape, advance paper in a printer, or sound an audible alarm.

A Sense command brings information from a control unit into processor storage concerning unusual conditions detected during the last I/O operation and detailed status about the device.

A Transfer in Channel (TIC) command specifies the location in processor storage from which the next CCW in

the channel program is to be fetched. A TIC may not specify another TIC. Also, the CAW may not address a TIC.

Each CCW specifies the channel operation to be performed, and (for data transfer operations) specifies contiguous locations in processor storage to be used. One or more CCWs make up a channel program that directs a channel operation.

Command retry is a channel-to-control unit procedure that can cause a command to be retried without requiring an I/O interruption. Retry is initiated by the control unit. When the command being executed encounters an error that can be retried, the control unit presents retry status to the channel. If conditions permit, a normal device reselection occurs to reissue the previous command; if retry is not possible, any chaining is terminated and an I/O interruption follows.

CHANNELS AND SUBCHANNELS

The channel facilities required to sustain a single I/O operation are called a subchannel. Subchannels may be either nonshared or shared. A nonshared subchannel has the facilities to operate only one I/O device; a shared subchannel provides facilities to operate one of an attached set of I/O devices.

The channels maintain the following channel control information for each I/O device selected:

- Protection key
- Data address
- Identity of operation specified by command code
- CCW flags
- Byte count
- Channel status
- Address of next CCW

CHAINING

A single CCW may specify contiguous locations in processor storage for a data transfer operation, or successive CCWs may be chained to specify a set of noncontiguous storage areas. Chaining to the next CCW is caused by the presence of a flag bit in a CCW.

In data chaining, the address and count information in a new CCW is used; the command code field is ignored unless a TIC is specified.

Entire CCWs, including their command code fields, may also be chained for use in a sequence of channel operations. Such coupling is called command chaining, and it is specified by a different flag bit in a CCW.

Data chaining has no effect on a device, as long as the channel has sufficient time to perform both data chaining and data transfer for the device.

In this manual, when a device is said to chain data, it means that the channel program for the device specifies data chaining.

Fetching Channel Command Words

The channel must fetch a new CCW when a CCW specifies data chaining, command chaining, or transfer in channel (TIC). The extra control activity caused by these operations takes time, and diminishes the capability of the channel to do other work.

A data-chaining fetch operation usually occurs while a channel also has a data transfer load from the same device. The time required to fetch the new CCW necessarily limits the interval of time available for successive data transfers through the channel. An absence of data chaining ordinarily permits a channel to operate with a faster I/O device.

Data Chaining in Gaps

For direct access storage devices, such as an IBM 3330 Disk Storage or an IBM 2305 Fixed Head Storage, formatting write commands causes the control unit to create gaps between count, key, and data fields on the recording track. Read and write commands that address more than one of the fields may specify data chaining to define separate areas in processor storage for the fields.

The gaps on a track have significance to channel programming considerations for direct access storage devices. The channel does not transfer data during the time a gap is created or passes under the read/write head, and this time is sufficient for a 3033 Processor to perform a command-chaining or data-chaining operation.

Command chaining ordinarily occurs only during gap time, but data chaining may occur during gap time or while data is being transferred. A data-chaining operation occurring during gap time has a lesser impact on channel facilities than when data transfers also occur. If a channel program for a direct access storage device calls for data chaining only during gap time, the overall load of the device on channel facilities is significantly less.

When a direct access storage device is said to chain data in a gap, the reference is to a gap other than a gap following a data field. The latter gap causes a device-end indication and command chaining is used in such a gap if the transfer of more information is desired. A device-end condition occurring in the absence of a CCW specifying command chaining results in termination of the operation. When command chaining continues the operation, the status information available at the end of the operation relates to the last operation in the chain.

During a read operation, an attempt at chaining data in a gap following a data field causes an incorrect-length indication in the channel status byte.

Late Command Chaining

Operation of direct access storage devices, such as disk storage, requires the use of command chaining. Between certain operations, such as searching for a record identification key and reading a data field on a direct access storage

device, the control unit has a fixed time interval during which it must receive and execute a new command. Certain I/O devices (such as the IBM 3330 Disk Storage and the IBM 3350 Direct Access Storage) can cause a command retry operation without requiring an I/O interruption, if activity on other channels causes too much delay in initiation of the operation specified by the new command. For devices that do not incorporate command retry, the channel program is terminated and an I/O interruption condition occurs.

CHANNEL IMPLEMENTATION

Each channel may attach as many as eight control units and can address as many as 256 I/O devices. Control units are connected to all channels through the I/O interface.

Multiplexing refers to the ability of the channels and devices to disconnect and reconnect during an operation over the I/O interface. The block-multiplexer channel operates in burst mode and can multiplex between blocks of data; the byte-multiplexer channel operates either in burst mode or in byte mode, and can multiplex between bytes, groups of bytes, or blocks.

Burst Mode is defined as operation over the I/O interface in which the device and the channel remain connected for a relatively long period of time in terms of system operation.

Byte Mode is defined as byte-interleaved operation over the I/O interface in which the channel and any one device remain connected for a relatively short period of time, typically long enough to transfer one byte or a small number of bytes.

Byte-Multiplexer Channel

A byte-multiplexer channel has a single data path that may be monopolized by one I/O device (burst mode) or shared by many I/O devices (byte mode). The design of a control unit predetermines whether its operation on the byte-multiplexer channel is in burst or byte mode. In either case, data transfer between storage and an I/O device is controlled one byte at a time. Byte-multiplexer channel operation may overlap block-multiplexer channel operation.

When multiple I/O devices concurrently share byte-multiplexer channel facilities, the operations are in byte mode. Each device in operation is selected, one at a time, for transfer of a byte or a group of bytes to or from processor storage. Bytes from multiple devices are interleaved and routed to or from the desired locations in processor storage. Therefore, the byte-multiplexer channel data path is used by one device for transfer of one byte or a group of bytes, and then another device uses the same data path. The sharing of the data path makes each device appear (to the user) as if it has a data path of its own. This leads to calling a device's share of the data path a subchannel.

Block-Multiplexer Channel

Each block-multiplexer channel provides a path for moving data between storage and a selected I/O device. It has storage for control information and data buffering. Data moves to or from an I/O device one byte at a time, but it is buffered to a width of 16 bytes for communications with storage.

A block-multiplexer channel can operate in three different ways:

1. When operating in block-multiplex mode with a nonshared subchannel that has a UCW assigned, the channel follows all block-multiplexing rules. (These rules are in *IBM System/370 Principles of Operation*, GA22-7000.)
2. When operating in block-multiplex mode with a shared subchannel, and the subchannel block-multiplex bit is on, the channel follows the block-multiplexing rules. If the block-multiplex bit is off, the channel operates as a selector channel.
3. A block-multiplexer channel operates as a selector channel under control of the operating system, as determined by bit 0 in control register 0.

UNIT CONTROL WORDS

The initiation of multiple I/O operations with logic-controlled channel multiprogramming requires that the subchannels be provided channel storage to record the addresses, count, and status and control information associated with the I/O operation. In the 3033 Processor, the storage for a single set of such information is called a unit control word (UCW). UCWs are stored in a 32K-byte buffer that is referred to as UCW storage.

On both byte- and block-multiplexer channels, the channel-control information (for each I/O device selected) is maintained for each subchannel in opertion. When a particular subchannel is selected by a Start I/O instruction and a channel program is initiated, the UCW locations for the subchannel are loaded with the information necessary for operation of the subchannel.

At each cessation of activity in a subchannel, the UCW contains updated information, and the channel is available for operation of another subchannel.

Block-Multiplexer Channel UCW Assignment

Block-multiplexer channels assign devices to nonshared UCWs as needed. Shared UCWs are assigned during initial microprogram load (IMPL). There are as many as 40 shared UCWs for each basic channel group. Fewer may be specified, depending on customer requirements.

Assignment of the configuration is made by service personnel during system installation. This assignment can be easily changed if the system is reconfigured.

During installation or reconfiguration, the following parameters must be specified for each shared subchannel:

- Number of devices installed (8, 16, or 32) for each control unit
- Mode of operation (selector or block multiplex, for each control unit)

Each shared subchannel refers to a block of 16 or 32 contiguous device addresses of the following form:

X0 through X7	(for 8 addresses)
X8 through XF	(for 8 addresses)
X0 through XF	(for 16 addresses)
X0 through (X+1) F	(for 32 addresses)

Only one control unit can be attached to each shared subchannel.

CHANNEL INDIRECT DATA ADDRESSING

Channels do not implement dynamic address translation. CCWs in virtual storage must be translated by the control program before execution. To allow the designation of contiguous areas of virtual storage to be mapped into noncontiguous areas of real storage, channel indirect data addressing (CIDA) is provided. For further information concerning CIDA, see *IBM System/370 Principles of Operation,* GA22-7000.

CHANNEL PRIORITY

For normal operation, priority for allocation within each channel group is in the following order:

- Block-multiplexer channel data transfer
- Block-multiplexer channel command chaining
- Block-multiplexer channel data chaining
- Byte-multiplexer channel operations
- Director operations

Block-multiplexer channels receive data handling priority in numeric order within each channel group.

I/O interruption priority goes across channel groups, and is in order of channel number, with the highest priority given to the lowest-numbered channels.

Channel Available Interruption

The 3033 Processor implements the channel available interruption on block-multiplexer channels. The channel available interruption is not implemented on byte-multiplexer channels.

CHANNEL LOADING AND THROUGHPUT

Each I/O device in operation places a load on its channel facilities. The magnitude of the load (and consequently the throughput rate) depends on many factors, such as the device's channel programming, its data transfer rate, and the use of command chaining.

OVERRUN

Overrun occurs when a channel does not accept or transfer data within required time limits. This data overrun may occur when the total channel activity initiated by the program exceeds channel capabilities. Depending on the device, the channel may halt operation or may continue transferring data until the end of the block is reached.

An overrun may cause a unit-check indication to be presented to the channel and stored into the CSW. Chaining, if any, is suppressed and an I/O interruption condition is generated at the end of the operation. Certain control units, however, may initiate a command retry sequence without storing a CSW or requiring an I/O interruption.

Overrun occurs only on unbuffered I/O devices; buffered devices cannot overrun. Instead, when buffer service is not provided within required time limits, the device merely waits for channel service.

Devices such as the IBM 2501 Card Reader, the IBM 1419 Magnetic Character Reader, or the IBM 3705 Communications Controller (in emulation mode) may require operator intervention in overrun situations.

REDUCING CHAINING CHECKS AND OVERRUNS

Either chaining checks on read data-chaining operations or overruns on write data-chaining operations can be caused by:

- Data addresses not being on word boundaries
- Short byte counts in CCWs
- High device speed on a channel that is data chaining
- Command-chain reselection

To reduce the probability of chaining checks or of overruns during data-chaining operations:

- Data addresses should be on fullword, doubleword, or quadword boundaries
- The CCW byte count should be no less than 64S/1.2, where S is the device speed in megabytes per second

Chapter 6. Multiple-Processor Complexes

OVERVIEW

The 3033 is available as a multiple-processor complex in either of two versions:

- IBM 3033 Multiprocessor Complex
- IBM 3033 Attached Processor Complex

The characteristics and features of these two complexes are briefly described in this chapter, particularly in how they differ from the single-processor version, the 3033 Processor Complex.

Though the 3033 Multiprocessor (MP) Complex and the 3033 Attached Processor (AP) Complex also differ from each other in a number of significant respects, they also share a number of similarities in characteristics and functions. These are described under appropriate headings in this chapter.

The AP and MP complexes also share a number of similarities in their component devices. Both the AP and MP complexes have:

- Two processors
- Two IBM 3036 Consoles
- Two IBM 3037 Power and Coolant Distribution Units (PCDUs), each equipped with a multiprocessing feature
- One IBM 3038 Multiprocessor Communication Unit (MCU)

In both complexes, the two processors are tightly coupled. That is, the two processors:

- Operate under the control of the same system control program
- Share processor storage
- Communicate directly with each other

The two processors are physically and logically joined together through the 3038 MCU. Each processor is powered by its own 3037 PCDU and is operator-controlled and communicated with through its own 3036 Console.

3033 Processor

The 3033 Processors used in AP and MP complexes are identical. The two used in an MP complex are designated M-series processors; the one used in an AP complex is designated an A-series processor. All standard and optional features available for the U-series 3033 Processor are also available for the A-series and M-series 3033 Processor, with the same limitations and prerequisites. If a customer already has a U-series 3033 Processor (Model U4, U6[1], U8, U12, or U16), the processor can be converted to an A-series or M-series version at the customer's location.

Prefixing

Each processor, in both an AP complex and an MP complex, requires an area of main storage for permanently assigned locations and logout areas. Because there is only one set of absolute addresses in shared processor storage, a means of assigning addresses to two different areas (one for each processor) is necessary. The technique used is called *prefixing.*

Prefixing provides a means of assigning addresses 0 through 4095 to any 4,096-byte storage area, starting at any address that is a multiple of 4,096. (A 4,096-byte storage area that is assigned addresses 0 through 4095 for either processor is called a permanent storage area.) The prefix is a 12-bit number located in the prefix-value register of each processor. The contents of the register can be set by the Set Prefix (SPX) instruction and can be inspected by the Store Prefix (STPX) instruction. For a detailed discussion of prefixing, refer to the *IBM System/370 Principles of Operation,* GA22-7000, in the chapter entitled "Multiprocessing."

Signaling and Response between Processors

Signaling and response between the two processors of an AP complex and between the two processors of an MP complex are provided by the use of the Signal Processor (SIGP) instruction and the signaling and response facility. Both the instruction and the facility are described in detail in the *IBM System/370 Principles of Operation,* GA22-7000.

Malfunction Alert

When either of the processors of an AP complex, or either of those of an MP complex, enters the check-stop state or drops power, a malfunction-alert signal is sent to the other processor. This signal generates a request for an external interruption. The interruption request remains pending until the interruption is taken or until the complex is reset. If the interruption is taken, the address of the failing processor is stored in locations 132-133, with an interruption code of 1200 (hexadecimal) stored in locations 134-135.

[1] Model U6 is no longer available.

Time-of-Day Clock

In both the MP and AP complex, when both processors are running, the time-of-day (TOD) clock of one processor is synchronized by the TOD clock of the other processor. Once synchronized, the two clocks appear as one to the complex. (See "TOD Clock Synchronization" in the *IBM System/370 Principles of Operation,* GA22-7000, for more detailed information.)

Power Control

In both an AP complex and an MP complex, one 3036 Console is associated with each processor. The Power On pushbutton on each console's control panel is used in the power-on process of the associated processor, as well as of the half of the 3038 MCU associated with that processor.

Storage

The processor storage capacities of both the A-series and the M-series processors are:

3033 Processor Model	*Storage Capacity (Bytes)*
A4, M4	4M (4,194,304)
A8, M8	8M (8,388,608)
A12, M12	12M (12,582,912)
A16, M16	16M (16,777,216)

where 1M byte equals 1,048,576 bytes.

In either an AP or MP complex, as many as 16M bytes of processor storage can be online at one time.

Storage Control

To ensure proper sequence of data manipulation between processors when storage is shared, data stored by one processor and fetched by the other appears to the fetching processor to have been stored in the order indicated by the instruction sequence. For more information, see "Sequence of Storage References" in the *IBM System/370 Principles of Operation,* GA22-7000.

Storage Protection

In both the AP and the MP complex, all 2K-byte blocks of data in processor storage can be protected against both store and fetch violations.

Channels

Each basic A-series and M-series 3033 Processor has 12 channels (two byte-multiplexer and 10 block-multiplexer), just as on the basic U-series 3033 Processor. Through the extended channels feature, each 3033 Processor can have four more channels (either four block-multiplexer or one byte-multiplexer and three block-multiplexer).

IBM 3038 Multiprocessor Communication Unit

In both the AP and the MP complexes, the IBM 3038 Multiprocessor Communication Unit (MCU) provides for communication between the two processors and permits either processor and any channel to address processor storage. Each half of the 3038 may be powered down independently of the remaining components of the complex. Each half is associated with one processor and receives its power from the 3037 PCDU associated with that processor.

IBM 3033 ATTACHED PROCESSOR COMPLEX

In an IBM 3033 Attached Processor Complex (Figure 6-1), an IBM 3042 Attached Processor is physically and logically joined to an A-series IBM 3033 Processor through an IBM 3038 MCU. The 3033 Processor shares its storage and channel facilities with the 3042 Attached Processor.

This complex can be especially advantageous for the user who requires significantly more instruction processing capability than the 3033 Processor Complex can provide, but whose needs do not justify use of the 3033 Multiprocessor Complex.

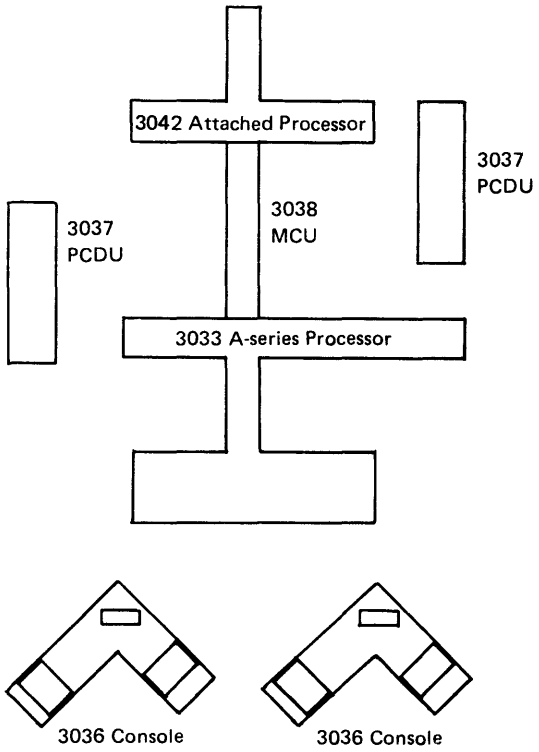


Figure 6-1. Plan View of an IBM 3033 Attached Processor Complex

Processing Availability

Continued system operation with a subset of total system resources can be achieved through:

- Alternate CPU recovery, an MVS facility that permits a functioning processor to attempt recovery of the work in process in a failing processor.
- Channel-set switching, a recovery aid that permits program-controlled switching of channel controls from the 3033 Processor to the 3042 Attached Processor, if the 3033 Processor still has power up, and if the data path to processor storage is still intact.
- Separate powering for the major components of the 3033 AP Complex, which permits limited independent maintenance of the 3042 Attached Processor.

IBM 3042 Attached Processor

The IBM 3042 Attached Processor provides processing capabilities similar to those of the 3033 Processor. Like the 3033, it has an IPPF, E-function, PSCF (with a 64K-byte buffer), and a maintenance function. Unlike the 3033, however, it has no processor storage or channel facilities of its own. The 3042 is metered, and can be taken offline either during periods of low use or for certain maintenance activities.

Processor Storage

Each 3033 AP Complex has at least 4M bytes of processor storage. Processor storage can be increased to a total of 16M bytes, in 4M-byte increments. All processor storage is part of the 3033 Processor, and all access to this storage is through the 3038 MCU.

Channels

The 3033 AP Complex can have either 12 or 16 channels, all of which are part of the 3033 Processor. The 3042 Attached Processor does not contain channels.

IBM 3033 MULTIPROCESSOR COMPLEX

In an IBM 3033 Multiprocessor Complex (Figure 6-2), two M-series 3033 Processors are physically and logically joined together through an IBM 3038 MCU. Each processor can share its processor storage and channel facilities with the other, and acts as the backup for the other. The MP complex offers the user significantly more instruction processing capability than the 3033 Processor Complex can provide, and it also offers improved storage, processing, and channel availability.

When the user so chooses, the two processors can also be configured to operate independently of each other in uniprocessor (UP) mode.

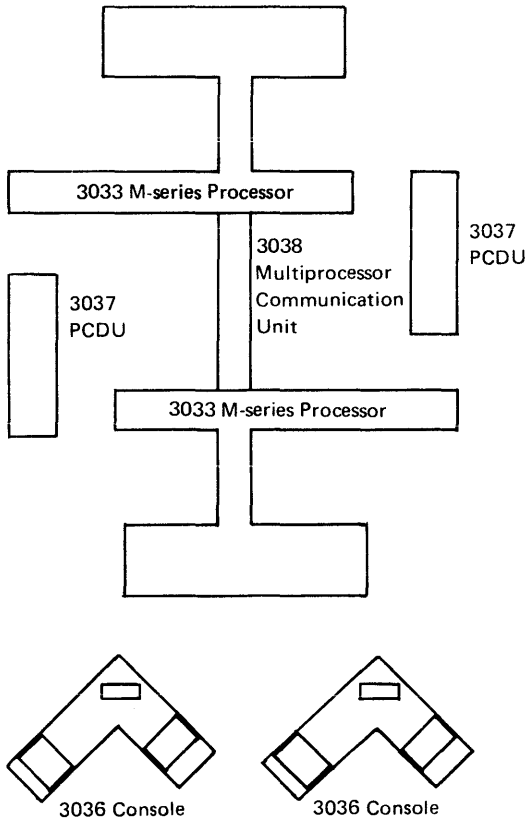


Figure 6-2. Plan View of an IBM 3033 Multiprocessor Complex

Processing Availability

Continued system operation with a subset of total system resources can be achieved through:

- Each processor acting as the backup for the other processor.
- Alternate CPU recovery, an MVS facility that permits a functioning processor to attempt recovery of the work in process in a failing processor.
- Channel-set switching, a recovery aid that permits program-controlled switching of channel controls from one processor to the other, if the failing processor still has power up, and if the data path to processor storage is still intact.
- Separate powering of the major components of the 3033 MP Complex, which permits certain elements to be configured out of the complex (varied offline) for service.

Processor Storage

In a 3033 MP complex, each 3033 Processor must have at least 4M bytes of storage. Processor storage capacity of each processor can be increased to a total of 16M bytes, in 4M-byte increments. In MP mode, the MP complex can have as many as 16M bytes online at one time.

Through use of the Configuration frame on the console display, a user can configure processor storage in three different ways:

- Completely self-contained, in which each processor accesses its own processor storage only
- Cross-configured, in which processor storage of one processor is configured to the other processor, but no processor storage is configured as common to both processors
- Completely shared, in which processors share all processor storage

Channels

Because the 3033 Multiprocessor Complex has two M-series 3033 Processors, the 3033 Multiprocessor Complex can have 24, 28, or 32 channels, with each processor having either 12 or 16 channels.

Appendix A. Glossary and Abbreviations

If the term you are seeking does not appear in this glossary, refer to *IBM Data Processing Glossary*, GC20-1699.

absolute address: An address that identifies a storage location or device without the use of any intermediate reference.

address: An identification of a storage location or an I/O device.

address compare: A technique to stop the processor at a specific address.

address modification: The process of changing the address part of a machine instruction via coded instructions.

address translation: The process of changing the address of an item of data or an instruction from its virtual storage address to its real storage address.

alphameric: Pertaining to a character set that contains letters, digits, and special characters.

AP: Attached processor.

attribute character: A character that describes the characteristics of the data field that follows it.

basic control (BC) mode: A mode in which the features of a System/360 and additional System/370 features (such as new machine instructions) are operational on a System/370.

BC mode: See *basic control mode.*

break-in: A change in control at a specified point in a channel or director microprogram.

C-bit: Change bit.

CCW: Channel command word.

CE: Customer engineer.

control registers: A set of registers used for operating system control of relocation, priority interruption, program event recording, error recovery, and masking operations.

CPU: Central processing unit.

CRT: Cathode-ray tube.

CSW: Channel status word.

CTCA: Channel-to-channel adapter.

cursor: A short line (underscore) displayed on the CRT display to indicate where the next character entered will be positioned.

DAT: See *dynamic address translation.*

DIDOCS: Device-independent display operator console support.

director: In any channel group, the element that controls the activity of the group's channels.

dynamic address translation (DAT): (1) The change of a virtual storage address to a real storage address during execution of an instruction. (2) A hardware feature that performs the translation.

E-function: Execution function.

EBCDIC: Extended binary-coded decimal interchange code.

EC mode: See *extended control mode.*

ECC: Error checking and correction.

extended control (EC) mode: A mode in which all the features of a System/370, including dynamic address translation, are operational.

FIFO: First in, first out.

ID: Identifier.

IMPL: Initial microprogram load.

initialize: To set counters, switches, addresses, or storage contents to 0 or to other starting values at the beginning of, or at the prescribed points in, a computer program.

IPL: Initial program load.

IPPF: Instruction preprocessing function.

K byte: 1,024 bytes of storage capacity.

LCL: Limited channel logout.

M byte: 1,048,576 bytes of storage capacity.

main storage: Program-addressable storage from which instructions and other data can be loaded directly into registers for subsequent execution or processing.

MCU: (IBM 3038) Multiprocessor Communication Unit.

MP: Multiprocessor.

MVS: Multiple virtual storage.

No-op: A no-operation instruction.

offline: Pertaining to resources with which the processor has no direct communication or control.

OLTEP: Online test executive program.

OLTSEP: Online test stand-alone executive program.

online: Pertaining to resources with which the processor has direct communications or control.

OS/VS: Operating system/virtual storage.

page: (1) A fixed-length block of instructions, data, or both that can be transferred between real storage and external page storage. (2) To transfer instructions, data, or both between real storage and external page storage.

page table: A table that indicates whether a page is in real storage and correlates virtual storage addresses with real storage addresses.

PCDU: (IBM 3037) Power and Coolant Distribution Unit.

PDU/CDU: See *PCDU*.

PER: Program event recording.

PFK or PF key: Program function key.

port: An access point for data entry or exit.

processor storage: The storage provided by one or more processors.

PSCF: Processor storage control function.

PSW: Program status word.

R-bit: Reference bit.

RAS: Reliability, availability, and serviceability.

RCS: Reloadable control storage.

real address: The address of a location in real storage.

SCP: System control programming.

SDE: Storage distribution element.

segment: A continuous area of virtual storage, which is allocated to a job or system task.

SVS: Single virtual storage.

TLB: Translation lookaside buffer.

TOD clock: Time-of-day clock.

TP: Teleprocessing. This term is synonymous with the term *data communications.*

UCW: Unit control word.

UP: Uniprocessor.

virtual address: An address that refers to virtual storage and that must be translated into a real storage address when it is to be used.

VM/370: IBM Virtual Machine Facility/370.

Appendix B. Deviations

DEVIATIONS FROM THE IBM System/370 Principles of Operation

Lost PER Instruction Fetch on Execute When Instruction Is Inaccessible

If a program-event recording (PER) instruction-fetching event is recognized in an Execute-instruction operation, but the subject instruction cannot be fetched either because of an access exception or because of an odd-numbered instruction address, then the event is not indicated along with the exception in the next program interruption.

Delayed Recognition of Clock-Comparator Interruption

The clock-comparator interruption-pending condition is tested as part of the TOD-clock and CPU-timer update, which occurs each microsecond. It is therefore possible to set a clock-comparator value that should generate an immediate interruption, but would execute one or more additional instructions before the interruption is actually taken. However, the delay until the interruption becomes pending is never more than 1 microsecond.

Reporting a Degradation Machine-Check Interruption Condition

The degradation machine-check interruption condition does not initiate a machine-check interruption, but it is held pending and is reported when a machine-check interruption is initiated by some other condition. This situation is visible when the system-recovery mask is 0 and a portion of high-speed buffer storage is deleted. When this buffer storage fails and the machine successfully deletes a portion of buffer storage and then successfully retries the affected instruction, both system recovery and degradation machine-check conditions are generated. However, if the system-recovery mask is 0, then no interruption for degradation is reported until some other machine-check condition occurs.

Two-Byte Interface Residual Count

If an I/O device terminates a write operation early, the channel detects the incorrect-length indication correctly. However, the residual count shown in the CSW may be one or two bytes lower than the actual residual count.

Ending Status Residual Count

Ending status received after initial status, but before any data is transferred, results in a residual count in a subsequent CSW which is one higher than the count in the original CCW.

Handling of Interruptions When a 3033 Leaves the Stopped State

If an I/O or external interruption is pending when a 3033 Processor leaves the stopped state through use of the START key, the interruption may be taken before, rather than after, the execution of the first instruction.

No-Op/Transfer-in-Channel Loops in Channel Programs

The use of No-Op/Transfer-in-Channel loops in channel programs results in degradation of director throughput and may cause time-out errors.

DEVIATIONS FROM THE IBM System/360 and System/370 I/O Interface Channel to Control Unit, OEMI

Channel-to-Channel Adapter (CTCA) Internal Cabling Resistance

The CTCA 'select out' and 'select in' internal cable resistance may exceed by as much as 0.1 ohm the 1.5-ohm resistance specified in the OEMI manual.

Partial Data Transfers on Output Operations through the Director Two-Byte Interface

Using the two-byte interface optional feature, partial data transfers are permitted on output operations, if:

- The first transfer request after a partial transfer is for a single byte on bus 1.
- All 'mark out' lines remain active during partial transfers.

IBM 3033 Functional Characteristics

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IBM 3033 Functional Characteristics (File No. S370-01) Printed in U.S.A. GA22-7060-3

International Business Machines Corporation
Data Processing Division
1133 Westchester Avenue, White Plains, N.Y. 10604

IBM World Trade Americas/Far East Corporation
Town of Mount Pleasant, Route 9, North Tarrytown, N.Y., U.S.A. 10591

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