IBM Field Engineering Maintenance Manual

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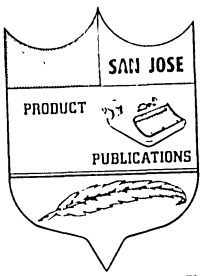

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1800 Data Acquisition and Control System

SY26-5956-6

IBM Field Engineering
Maintenance Manual

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1800 Data Acquisition and Control System

SY26-5956-6

Preface

This manual contains maintenance information for the following units of the IBM Data Acquisition and Control System:

IBM 1801 and 1802 Processor-Controllers
IBM 1803 Core Storage Unit
IBM 1826 Data Adapter Unit
IBM 1828 Enclosure
IBM 1851 Multiplexer Terminal
IBM 1856 Analog Output Terminal

The data processing input/output units used in the 1800 system are provided with separate maintenance manuals that contain information required to service those units. Other manuals that are used in servicing the 1800 system are listed in the *IBM Field Engineering Bibliography, 1800 Data Acquisition and Control System* (Order No. SY26-0560).*

It is assumed that the user of this manual is familiar with 1800 system programming techniques and that he understands the functional and operational aspects of all system areas. Hexadecimal numbers, if not otherwise identified, are preceded by a "slash" (e.g., /3000) to distinguish them from decimal numbers.

Service Aids included in this manual are 24, 25, 35, 44, 65, 66, 69, 129, 134, and 172.

*Manuals referred to in this publication that have an Order No. with a four character prefix are identical in content to the same manual without the initial prefix character. (e.g. SY26-xxxx is the same in content as Y26-xxxx.)

Seventh Edition (February, 1970)

This manual (Order No. SY26-5956-6) is a complete revision of, and makes obsolete, Order No. SY26-5956-5. Changes to the text, and small changes to illustrations, are indicated by a vertical line to the left of the change; changed or added illustrations are denoted by the symbol • to the left of the caption.

Significant changes or additions to the specifications contained in this publication are continually being made. When using this publication in connection with the operation of IBM equipment, check the latest FE Publications Systems Sequence Listing, Order No. SY20-0073, for revisions or contact the local IBM Branch Office.

The illustrations in this manual have a code number in the lower corner. This is a publishing control number and is not related to the subject matter.

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A form for reader's comments is provided at the back of this publication. If the form has been removed, send your comments to the address below.

This manual was prepared by the IBM Systems Development Division, Product Publications, Department G24, San Jose, California 95114.

Contents

Safety

PERSONAL SAFETY

Personal safety cannot be overemphasized. To ensure your own safety and the safety of co-workers, make it a practice to observe safety precautions at all times. You should be familiar with the general safety practices and procedures outlined in Order No. S229-1624, which is reproduced here.

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power AC and DC when removing or assembling major components, working in immediate area of power supplies, performing mechanical inspection of power supplies and installing changes in machine circuitry.
3. Wall box power switch when turned off should be locked or tagged in off position. "Do not Operate" tags, form 229-1266, affixed when applicable. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, the following precautions must be followed:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Rings, wrist watches, chains, bracelets, metal cuff links, shall not be worn.
   c. Only insulated pliers and screwdrivers shall be used.
   d. Keep one hand in pocket.
   e. When using test instruments be certain controls are set correctly and proper capacity, insulated probes are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc. — use suitable rubber mats purchased locally if necessary).
5. Safety Glasses must be worn when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Parts cleaning, using solvents, sprays, cleaners, chemicals, etc.
   f. All other conditions that may be hazardous to your eyes. REMEMBER, THEY ARE **YOUR** EYES.
6. Special safety instructions such as handling Cathode Ray Tubes and extreme high voltages, must be followed as outlined in CEM's and Safety Section of the Maintenance Manuals.
7. Do not use solvents, chemicals, greases or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles — this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. All safety devices such as guards, shields, signs, ground wires, etc. shall be restored after maintenance.

KNOWING SAFETY RULES IS NOT ENOUGH
AN UNSAFE ACT WILL INEVITABLY LEAD TO AN ACCIDENT
USE GOOD JUDGMENT — ELIMINATE UNSAFE ACTS
229-1264-1

Exposure to Environmental Hazards

The 1800 Data Acquisition and Control System is linked directly to the customer's process, and voltages can be introduced into the system from a number of sources. Even with power removed from the 1800 system, hazardous voltages may be present in the customer termination

12. Each Customer Engineer is responsible to be certain that no action on his part renders product unsafe or exposes hazards to customer personnel.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. All machine covers must be in place before machine is returned to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it (i.e., under desk or table).
16. Avoid touching mechanical moving parts (i.e., when lubricating, checking for play, etc.).
17. When using stroboscope — do not touch ANYTHING — it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CE's and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machines while performing and after completing maintenance.

Artificial Respiration

GENERAL CONSIDERATIONS

1. **Start Immediately, Seconds Count**
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim or apply stimulants.
2. **Check Mouth for Obstructions**
   Remove foreign objects — Pull tongue forward.
3. **Loosen Clothing — Keep Warm**
   Take care of these items after victim is breathing by himself or when help is available.
4. **Remain in Position**
   After victim revives, be ready to resume respiration if necessary.
5. **Call a Doctor**
   Have someone summon medical aid.
6. **Don't Give Up**
   Continue without interruption until victim is breathing without help or is certainly dead.

Reprint Courtesy Mine Safety Appliances Co.

Rescue Breathing for Adults Victim on His Back Immediately

1. **Clear throat** of water, food, or foreign matter.
2. **Tilt head back** to open air passage.
3. **Lift jaw up** to keep tongue out of air passage.
4. **Pinch nostrils** to prevent air leakage when you blow.
5. **Blow** until you see chest rise.
6. **Remove your lips** and allow lungs to empty.
7. **Listen** for snoring and gurglings, signs of throat obstruction.
8. **Repeat mouth to mouth breathings** 10-20 times a minute.

Continue rescue breathing until he breathes for himself.

14117 A

area. All customer lines are potentially dangerous and should be regarded as live circuits.

When entering any part of the customer's process area, observe all safety precautions and regulations. Check the following items with customer safety personnel:

1. The need for safety glasses, hard hats, or special clothing.
2. Particular route that must be taken to and from installation. Escort required?
3. Smoking restrictions.
4. Restrictions on use of electrical or other spark-producing tools.
5. Exposure to high voltages.
6. Exposure to heavy machinery or other equipment.
7. Exposure to splashing acids, molten metal, hot liquids, etc.
8. Exposure to toxic gases and vapors.
9. Warning alarms and emergency exits.

When servicing IBM units that are installed in customer consoles or racks, pay particular attention to nearby units or devices that can present a safety hazard.

Machine Warning Labels

Heed the warning labels placed in hazardous areas of the machines. They are placed there for your protection.

Power Supplies

Before working on any power supply, remove power from the unit and allow at least one minute for capacitors to discharge. Although all power supplies are provided with bleeder resistors to drain off capacitor charges when power is dropped, it is wise to check the dc output with a meter before attempting maintenance.

Power Cords

Check power cords periodically for safe condition and proper ground connections.

Line-Powered Equipment

Oscilloscopes and other line-powered equipment must always be grounded through the third-wire grounding conductor in the power cord.

EQUIPMENT PRECAUTIONS

Customer Interface

The 1800 system is an integral part of the customer's operation. *Do not,* under any circumstances, work on any part of the system without the knowledge and consent of the customer.

Be especially careful not to impulse a digital or analog output point that is connected to a process device.

Core Storage

Use extreme caution when working around core storage. Do not leave the core storage unit unattended when covers are removed.

Solid-State Components

Avoid operating the system for prolonged periods with the SLT card covers removed.

Care must be exercised when grounding signal lines, in order to prevent applying a voltage instead of a ground, or grounding the output of an emitter-follower circuit. Electrical overloads, for periods of even a few microseconds, can seriously damage or destroy transistors.

Because of the danger of shorting between adjacent cards, it is not advisable to remove or replace SLT cards with power on.

The following types of cards must never be removed with power on:

Drivers and amplifiers
Core storage cards
Power supply cards
Multiplexer cards

Relay Multiplexer Cards

Use care when removing and inserting multiplexer cards. Fingerprints, pencil marks, and other contaminants decrease the leakage resistance of these cards. Do not use cleaning solvents or card contact lubricants, and do not permit the protective coating on the card to become damaged.

Before a relay card is inserted in the card gate, it should be held upright and tapped lightly to clean the contacts of any excess mercury. Sharp blows should be avoided; do not tap the card against a hard surface or drive the card into its socket with a blow from the hand. Improper handling of relay cards can make the relay inoperable or cause it to operate outside specified limits.

If common-mode voltage in excess of 10 volts (ac or dc) is present on the customer input lines, or if there is a possibility of the occurrence of such voltage, the lines must be disconnected by the customer prior to removal or insertion of the multiplexer relay card in that channel. Mercury bridging of the relay points during removal or insertion of the card may impress the entire common-mode voltage across the flying capacitor, relay points, or amplifier, resulting in component damage.

Abbreviations

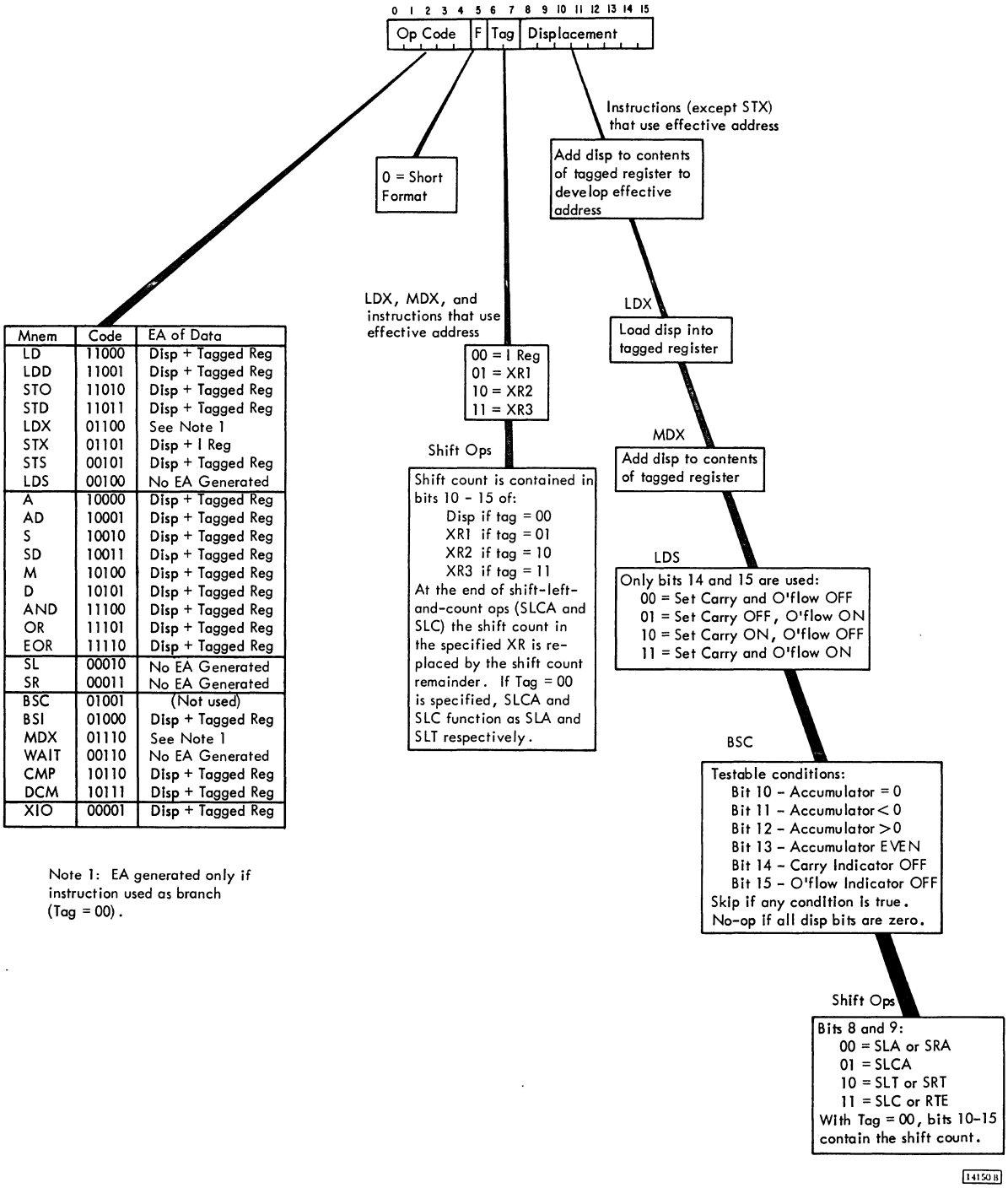
A-reg	accumulator register
ADA	analog driver amplifier
ADC	analog-to-digital converter
AI	analog input
ALD	automated logic diagram
AMAR	analog multiplexer address register
AO	analog output
ASCII	American standard code for information interchange
AWG	American wire gauge
aux	auxiliary
B-reg	storage buffer register
BCC	block check character
bfr	buffer
BO	branch out
BS	block switch
BSC	binary synchronous communications
BSM	basic storage module
CA	communications adapter
CAB	channel address buffer
CAF	customer assignment form
CAR	channel address register
CC	chain command
CCW	channel command word
CD	chain data
CEM	Customer Engineers Memorandum
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC-16	cyclic redundancy check (16 bits)
CRP	Card Read Punch (IBM 1442)
CS	cycle steal
CSA	cycle steal acknowledge
CSU	core storage unit
CSW	channel status word
D-reg	arithmetic factor register
DAC	digital-to-analog converter
DAO	digital and analog output
DAU	Data Adapter Unit (IBM 1826)
DC	data channel
DCU	data control unit
DDC	direct digital control
DET	double-emitter transistor
DI	digital input
DIMAL	disk maintenance library
DLE	data link escape
DO	digital output
DP	data processing
DPC	direct program control
DSW	device status word
EA	effective address
EBCDIC	extended binary-coded-decimal interchange code
EC	engineering change
ECA	engineering change announcement
ECAD	error check analysis diagram
ECO	electronic "contact" operate
ENQ	enquiry
EOC	end of conversion
EOT	end of table
EOT	end of transmission
EPO	emergency power off
ETB	end of transmission block
ETX	end of text
F-reg	format register
FC	feature code
FEALD	Field Engineering automated logic diagram
FESRR	Field Engineering Systems Reference Report
FET	field-effect transistor
FF	flip-flop
FL	flip-latch
hex	hexadecimal
HLSE	high-level, single-ended
HSDA	high-speed data acquisition
Hz	hertz (cycles per second)
I-reg	instruction register
I/A	indirect addressing
ICAR	instrument calibration and repair
ILSW	interrupt level status word
I/O	input/output
IOCC	input/output control command
IPL	initial program load
ITB	intermediate transmission block
LA	line adapter
LRC	longitudinal redundancy check
LSB	least significant bit
M-reg	storage address register
MAR-2	Manufacturing Assembly Report #2 (field use)
MDM	maintenance diagram manual
MES	miscellaneous equipment specification
MI	multi-input
MLC	machine level control
MLR	machine location report
Mod-reg	modify register
MPS	medium power standard

MPX	multiplex(er), R-relay, S-solid-state
MPX	Multiprogramming Executive (a programming system)
NAK	negative acknowledgment
Op-reg	operation code register
P	parity
PC	pulse counter
P-C	processor-controller
PCI	program control interruption
PI	process interrupt
PID	program identification
PISW	process interrupt status word
PO	pulse output
POC	process operator's console
PVR	precision voltage reference
Q-reg	accumulator extension register
RBT	resistance bulb thermometer
RO	register output
RPQ	request for price quotation
SAR	storage address register
S&H	sample-and-hold (amplifier)
SC	shift counter
SCR	silicon-controlled rectifier
SCRID	SCR indicator driver
SI	single instruction
SIO	start input/output
SLD	simplified logic diagram
SLI	suppress length indicator
SLT	solid logic technology
SMS	standard modular system
SOH	start of heading
SPD	sample pulse driver
SRL	Systems Reference Library
SS	singleshot (multivibrator)
SSC	single storage cycle
STX	start of text
SYN	synchronous idle
T-reg	tag register
tag	selector channel control line
TIC	transfer in channel
TSX	Time-Sharing Executive (a programming system)
TTD	temporary text delay
U-reg	temporary accumulator register
UDCD	unit data and control diagram
UJT	unijunction transistor
VRef	reference voltage (core storage)
VRC	vertical redundancy check
VSA	sense amplifier voltage (core storage)
WC	word counter
XIO	execute input/output
XR	index register
/	precedes hexadecimal numbers (base 16)

Chapter 1. Reference Data and Diagnostic Techniques

Section 1. Reference Data

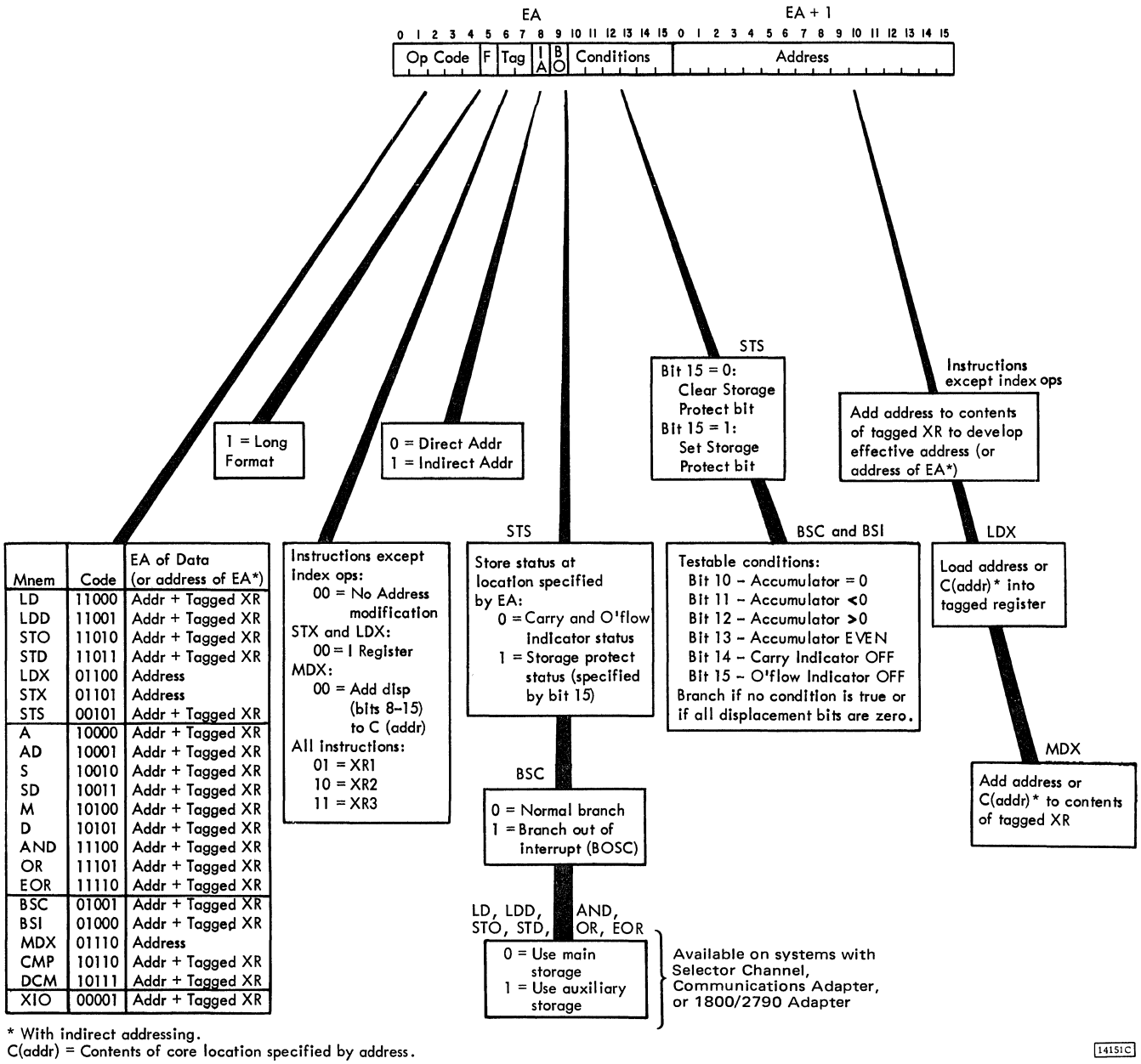
Figures 1-1 through 1-24 contain reference data for use in servicing the IBM 1800 Data Acquisition and Control System.



Mnem	Code	EA of Data
LD	11000	Disp + Tagged Reg
LDD	11001	Disp + Tagged Reg
STO	11010	Disp + Tagged Reg
STD	11011	Disp + Tagged Reg
LDX	01100	See Note 1
STX	01101	Disp + 1 Reg
STS	00101	Disp + Tagged Reg
LDS	00100	No EA Generated
A	10000	Disp + Tagged Reg
AD	10001	Disp + Tagged Reg
S	10010	Disp + Tagged Reg
SD	10011	Disp + Tagged Reg
M	10100	Disp + Tagged Reg
D	10101	Disp + Tagged Reg
AND	11100	Disp + Tagged Reg
OR	11101	Disp + Tagged Reg
EOR	11110	Disp + Tagged Reg
SL	00010	No EA Generated
SR	00011	No EA Generated
BSC	01001	(Not used)
BSI	01000	Disp + Tagged Reg
MDX	01110	See Note 1
WAIT	00110	No EA Generated
CMP	10110	Disp + Tagged Reg
DCM	10111	Disp + Tagged Reg
XIO	00001	Disp + Tagged Reg

Note 1: EA generated only if instruction used as branch (Tag = 00).

Figure 1-1. Short Instruction Format



● Figure 1-2. Long Instruction Format

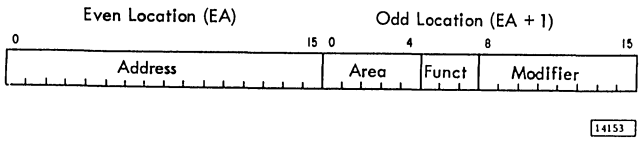


Figure 1-3. IOCC Format

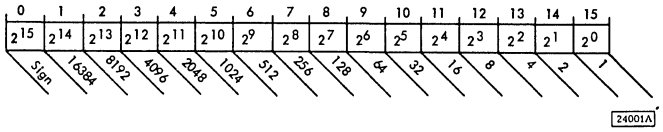


Figure 1-4. Single-Precision Data Word

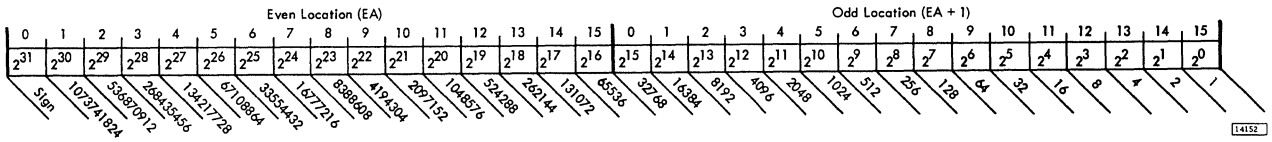


Figure 1-5. Double-Precision Data Word

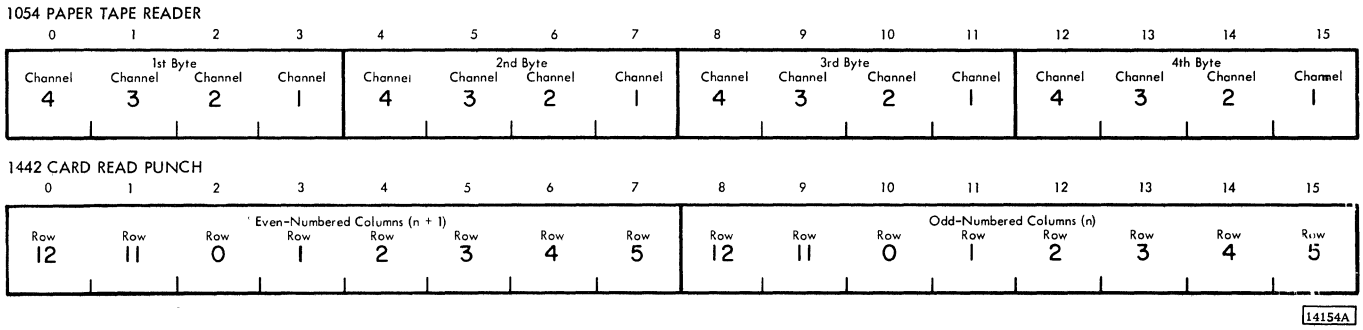


Figure 1-6. Data Words -- IPL Mode

Interrupt Level	Priority	Vector Address Hex	Vector Address Decimal	Interrupt Level Status Word Encode Bits * 10	11	12	13	14	15	Interrupt Poll	IN Bus Bit
Internal	1	0008	8	0	0	1	0	0	0	—	—
Trace	26	0009	9	0	0	1	0	0	1	—	—
CE	27	000A	10	0	0	1	0	1	0	B	15
0	2	000B	11	0	0	1	0	1	1	A	0
1	3	000C	12	0	0	1	1	0	0	A	1
2	4	000D	13	0	0	1	1	0	1	A	2
3	5	000E	14	0	0	1	1	1	0	A	3
4	6	000F	15	0	0	1	1	1	1	A	4
5	7	0010	16	0	1	0	0	0	0	A	5
6	8	0011	17	0	1	0	0	0	1	A	6
7	9	0012	18	0	1	0	0	1	0	A	7
8	10	0013	19	0	1	0	0	1	1	A	8
9	11	0014	20	0	1	0	1	0	0	A	9
10	12	0015	21	0	1	0	1	0	1	A	10
11	13	0016	22	0	1	0	1	1	0	A	11
12	14	0017	23	0	1	0	1	1	1	A	12
13	15	0018	24	0	1	1	0	0	0	A	13
14	16	0019	25	0	1	1	0	0	1	B	0
15	17	001A	26	0	1	1	0	1	0	B	1
16	18	001B	27	0	1	1	0	1	1	B	2
17	19	001C	28	0	1	1	1	0	0	B	3
18	20	001D	29	0	1	1	1	0	1	B	4
19	21	001E	30	0	1	1	1	1	0	B	5
20	22	001F	31	0	1	1	1	1	1	B	6
21	23	0020	32	1	0	0	0	0	0	B	7
22	24	0021	33	1	0	0	0	0	1	B	8
23	25	0022	34	1	0	0	0	1	0	B	9

*Only bits 11 through 15 are placed on the OUT bus for interrupt level decoding at device adapters. Note, therefore, that hex addresses 20, 21, and 22 are decoded as 0, 1, and 2 at the adapters.

14186 A

Figure 1-7. Interrupt Levels

Hex Address	Contents
0001	CE Interrupt (Start of Program)
0004	Interval Timer A
0005	Interval Timer B
0006	Interval Timer C
0008	Internal Interrupt
0009	Trace Interrupt
000A	CE Interrupt (Return Address)
000B	Interrupt Level 0
000C	Interrupt Level 1
000D	Interrupt Level 2
000E	Interrupt Level 3
000F	Interrupt Level 4
0010	Interrupt Level 5
0011	Interrupt Level 6
0012	Interrupt Level 7
0013	Interrupt Level 8
0014	Interrupt Level 9
0015	Interrupt Level 10
0016	Interrupt Level 11
0017	Interrupt Level 12 (Special Feature Group 1)
0018	Interrupt Level 13
0019	Interrupt Level 14
001A	Interrupt Level 15
001B	Interrupt Level 16
001C	Interrupt Level 17
001D	Interrupt Level 18 (Special Feature Group 2)
001E	Interrupt Level 19
001F	Interrupt Level 20
0020	Interrupt Level 21
0021	Interrupt Level 22
0022	Interrupt Level 23

14156

Figure 1-8. Reserved Main Storage Locations

Decimal/Hexadecimal Conversion Chart

The tables printed below are used to convert decimal numbers to hexadecimal and hexadecimal numbers to decimal. In the descriptions that follow, the explanation of each step is followed by an example in parentheses.

Decimal to Hexadecimal Conversion. Locate the decimal number (0489) in the body of the table. The two high-order digits (1E) of the hexadecimal number are in the left column on the same line, and the low-order digit (9) is at the top of the column. Thus, the hexadecimal number 1E9 is equal to the decimal number 0489.

Hexadecimal to Decimal Conversion. Locate the first two digits (1E) of the hexadecimal number (1E9) in the left column. Follow the line of figures across the page to the column headed by the low-order digit (9). The decimal number (0489) located at the junction of the horizontal line and the vertical column is the equivalent of the hexadecimal number.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00 _	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
01 _	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
02 _	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
03 _	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
04 _	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
05 _	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
06 _	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
07 _	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
08 _	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
09 _	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
0A _	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
0B _	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
0C _	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
0D _	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
0E _	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
0F _	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255
10 _	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
11 _	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
12 _	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
13 _	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
14 _	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0332	0333	0334	0335
15 _	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
16 _	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
17 _	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
18 _	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
19 _	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
1A _	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
1B _	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
1C _	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
1D _	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
1E _	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
1F _	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511
20 _	0512	0513	0514	0515	0516	0517	0518	0519	0520	0521	0522	0523	0524	0525	0526	0527
21 _	0528	0529	0530	0531	0532	0533	0534	0535	0536	0537	0538	0539	0540	0541	0542	0543
22 _	0544	0545	0546	0547	0548	0549	0550	0551	0552	0553	0554	0555	0556	0557	0558	0559
23 _	0560	0561	0562	0563	0564	0565	0566	0567	0568	0569	0570	0571	0572	0573	0574	0575
24 _	0576	0577	0578	0579	0580	0581	0582	0583	0584	0585	0586	0587	0588	0589	0590	0591
25 _	0592	0593	0594	0595	0596	0597	0598	0599	0600	0601	0602	0603	0604	0605	0606	0607
26 _	0608	0609	0610	0611	0612	0613	0614	0615	0616	0617	0618	0619	0620	0621	0622	0623
27 _	0624	0625	0626	0627	0628	0629	0630	0631	0632	0633	0634	0635	0636	0637	0638	0639
28 _	0640	0641	0642	0643	0644	0645	0646	0647	0648	0649	0650	0651	0652	0653	0654	0655
29 _	0656	0657	0658	0659	0660	0661	0662	0663	0664	0665	0666	0667	0668	0669	0670	0671
2A _	0672	0673	0674	0675	0676	0677	0678	0679	0680	0681	0682	0683	0684	0685	0686	0687
2B _	0688	0689	0690	0691	0692	0693	0694	0695	0696	0697	0698	0699	0700	0701	0702	0703
2C _	0704	0705	0706	0707	0708	0709	0710	0711	0712	0713	0714	0715	0716	0717	0718	0719
2D _	0720	0721	0722	0723	0724	0725	0726	0727	0728	0729	0730	0731	0732	0733	0734	0735
2E _	0736	0737	0738	0739	0740	0741	0742	0743	0744	0745	0746	0747	0748	0749	0750	0751
2F _	0752	0753	0754	0755	0756	0757	0758	0759	0760	0761	0762	0763	0764	0765	0766	0767
30 _	0768	0769	0770	0771	0772	0773	0774	0775	0776	0777	0778	0779	0780	0781	0782	0783
31 _	0784	0785	0786	0787	0788	0789	0790	0791	0792	0793	0794	0795	0796	0797	0798	0799
32 _	0800	0801	0802	0803	0804	0805	0806	0807	0808	0809	0810	0811	0812	0813	0814	0815
33 _	0816	0817	0818	0819	0820	0821	0822	0823	0824	0825	0826	0827	0828	0829	0830	0831
34 _	0832	0833	0834	0835	0836	0837	0838	0839	0840	0841	0842	0843	0844	0845	0846	0847
35 _	0848	0849	0850	0851	0852	0853	0854	0855	0856	0857	0858	0859	0860	0861	0862	0863
36 _	0864	0865	0866	0867	0868	0869	0870	0871	0872	0873	0874	0875	0876	0877	0878	0879
37 _	0880	0881	0882	0883	0884	0885	0886	0887	0888	0889	0890	0891	0892	0893	0894	0895
38 _	0896	0897	0898	0899	0900	0901	0902	0903	0904	0905	0906	0907	0908	0909	0910	0911
39 _	0912	0913	0914	0915	0916	0917	0918	0919	0920	0921	0922	0923	0924	0925	0926	0927
3A _	0928	0929	0930	0931	0932	0933	0934	0935	0936	0937	0938	0939	0940	0941	0942	0943
3B _	0944	0945	0946	0947	0948	0949	0950	0951	0952	0953	0954	0955	0956	0957	0958	0959
3C _	0960	0961	0962	0963	0964	0965	0966	0967	0968	0969	0970	0971	0972	0973	0974	0975
3D _	0976	0977	0978	0979	0980	0981	0982	0983	0984	0985	0986	0987	0988	0989	0990	0991
3E _	0992	0993	0994	0995	0996	0997	0998	0999	1000	1001	1002	1003	1004	1005	1006	1007
3F _	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
40 _	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
41 _	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
42 _	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
43 _	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
44 _	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
45 _	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
46 _	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
47 _	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
48 _	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
49 _	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
4A _	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
4B _	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
4C _	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
4D _	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
4E _	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
4F _	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
50 _	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
51 _	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
52 _	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
53 _	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
54 _	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359
55 _	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
56 _	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
57 _	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
58 _	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
59 _	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
5A _	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
5B _	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
5C _	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
5D _	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
5E _	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
5F _	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535
60 _	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
61 _	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
62 _	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
63 _	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
64 _	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
65 _	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
66 _	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
67 _	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
68 _	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
69 _	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
6A _	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
6B _	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727
6C _	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
6D _	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
6E _	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
6F _	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791
70 _	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807
71 _	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
72 _	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
73 _	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
74 _	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
75 _	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
76 _	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
77 _	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
78 _	1920	1921	1922	1923	1924	1925	1926	1927	1928	1929	1930	1931	1932	1933	1934	1935
79 _	1936	1937	1938	1939	1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951
7A _	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967
7B _	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
7C _	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
7D _	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
7E _	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
7F _	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047

20290

Figure 1-9. Decimal/Hexadecimal Conversion Table (Part 1 of 2)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
80_	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063
81_	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079
82_	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095
83_	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111
84_	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127
85_	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143
86_	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159
87_	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175
88_	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191
89_	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207
8A_	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223
8B_	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239
8C_	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255
8D_	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271
8E_	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287
8F_	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303
90_	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319
91_	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335
92_	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351
93_	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367
94_	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383
95_	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399
96_	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415
97_	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431
98_	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2443	2444	2445	2446	2447
99_	2448	2449	2450	2451	2452	2453	2454	2455	2456	2457	2458	2459	2460	2461	2462	2463
9A_	2464	2465	2466	2467	2468	2469	2470	2471	2472	2473	2474	2475	2476	2477	2478	2479
9B_	2480	2481	2482	2483	2484	2485	2486	2487	2488	2489	2490	2491	2492	2493	2494	2495
9C_	2496	2497	2498	2499	2500	2501	2502	2503	2504	2505	2506	2507	2508	2509	2510	2511
9D_	2512	2513	2514	2515	2516	2517	2518	2519	2520	2521	2522	2523	2524	2525	2526	2527
9E_	2528	2529	2530	2531	2532	2533	2534	2535	2536	2537	2538	2539	2540	2541	2542	2543
9F_	2544	2545	2546	2547	2548	2549	2550	2551	2552	2553	2554	2555	2556	2557	2558	2559
A0_	2560	2561	2562	2563	2564	2565	2566	2567	2568	2569	2570	2571	2572	2573	2574	2575
A1_	2576	2577	2578	2579	2580	2581	2582	2583	2584	2585	2586	2587	2588	2589	2590	2591
A2_	2592	2593	2594	2595	2596	2597	2598	2599	2600	2601	2602	2603	2604	2605	2606	2607
A3_	2608	2609	2610	2611	2612	2613	2614	2615	2616	2617	2618	2619	2620	2621	2622	2623
A4_	2624	2625	2626	2627	2628	2629	2630	2631	2632	2633	2634	2635	2636	2637	2638	2639
A5_	2640	2641	2642	2643	2644	2645	2646	2647	2648	2649	2650	2651	2652	2653	2654	2655
A6_	2656	2657	2658	2659	2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2670	2671
A7_	2672	2673	2674	2675	2676	2677	2678	2679	2680	2681	2682	2683	2684	2685	2686	2687
A8_	2688	2689	2690	2691	2692	2693	2694	2695	2696	2697	2698	2699	2700	2701	2702	2703
A9_	2704	2705	2706	2707	2708	2709	2710	2711	2712	2713	2714	2715	2716	2717	2718	2719
AA_	2720	2721	2722	2723	2724	2725	2726	2727	2728	2729	2730	2731	2732	2733	2734	2735
AB_	2736	2737	2738	2739	2740	2741	2742	2743	2744	2745	2746	2747	2748	2749	2750	2751
AC_	2752	2753	2754	2755	2756	2757	2758	2759	2760	2761	2762	2763	2764	2765	2766	2767
AD_	2768	2769	2770	2771	2772	2773	2774	2775	2776	2777	2778	2779	2780	2781	2782	2783
AE_	2784	2785	2786	2787	2788	2789	2790	2791	2792	2793	2794	2795	2796	2797	2798	2799
AF_	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809	2810	2811	2812	2813	2814	2815
B0_	2816	2817	2818	2819	2820	2821	2822	2823	2824	2825	2826	2827	2828	2829	2830	2831
B1_	2832	2833	2834	2835	2836	2837	2838	2839	2840	2841	2842	2843	2844	2845	2846	2847
B2_	2848	2849	2850	2851	2852	2853	2854	2855	2856	2857	2858	2859	2860	2861	2862	2863
B3_	2864	2865	2866	2867	2868	2869	2870	2871	2872	2873	2874	2875	2876	2877	2878	2879
B4_	2880	2881	2882	2883	2884	2885	2886	2887	2888	2889	2890	2891	2892	2893	2894	2895
B5_	2896	2897	2898	2899	2900	2901	2902	2903	2904	2905	2906	2907	2908	2909	2910	2911
B6_	2912	2913	2914	2915	2916	2917	2918	2919	2920	2921	2922	2923	2924	2925	2926	2927
B7_	2928	2929	2930	2931	2932	2933	2934	2935	2936	2937	2938	2939	2940	2941	2942	2943
B8_	2944	2945	2946	2947	2948	2949	2950	2951	2952	2953	2954	2955	2956	2957	2958	2959
B9_	2960	2961	2962	2963	2964	2965	2966	2967	2968	2969	2970	2971	2972	2973	2974	2975
BA_	2976	2977	2978	2979	2980	2981	2982	2983	2984	2985	2986	2987	2988	2989	2990	2991
BB_	2992	2993	2994	2995	2996	2997	2998	2999	3000	3001	3002	3003	3004	3005	3006	3007
BC_	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023
BD_	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039
BE_	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055
BF_	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C0_	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087
C1_	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103
C2_	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119
C3_	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135
C4_	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
C5_	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167
C6_	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183
C7_	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199
C8_	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215
C9_	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231
CA_	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
CB_	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263
CC_	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279
CD_	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295
CE_	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311
CF_	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327
D0_	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343
D1_	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359
D2_	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375
D3_	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391
D4_	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407
D5_	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423
D6_	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439
D7_	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455
D8_	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471
D9_	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
DA_	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503
DB_	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519
DC_	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535
DD_	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551
DE_	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567
DF_	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583
E0_	3584	3585	3586	3587	3588	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599
E1_	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615
E2_	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631
E3_	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647
E4_	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663
E5_	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679
E6_	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695
E7_	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711
E8_	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727
E9_	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743
EA_	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759
EB_	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775
EC_	3776	3777	3778	3779	3780	3781	3782	3783	3784	3785	3786	3787	3788	3789	3790	3791
ED_	3792	3793	3794	3795	3796	3797	3798	3799	3800	3801	3802	3803	3804	3805	3806	3807
EE_	3808	3809	3810	3811	3812	3813	3814	3815	3816	3817	3818	3819	3820	3821	3822	3823
EF_	3824	3825	3826	3827	3828	3829	3830	3831	3832	3833	3834	3835	3836	3837	3838	3839
F0_	3840	3841	3842	3843	3844	3845	3846	3847	3848	3849	3850	3851	3852	3853	3854	3855
F1_	3856	3857	3858	3859	3860	3861	3862	3863	3864	3865	3866	3867	3868	3869	3870	3871
F2_	3872	3873	3874	3875	3876	3877	3878	3879	3880	3881	3882	3883	3884	3885	3886	3887
F3_	3888	3889	3890	3891	3892	3893	3894	3895	3896	3897	3898	3899	3900	3901	3902	3903
F4_	3904	3905	3906	3907	3908	3909	3910	3911	3912	3913	3914	3915	3916	3917	3918	3919
F5_	3920	3921	3922	3923	3924	3925	3926	3927	3928	3929	3930	3931	3932	3933	3934	3935
F6_	3936	3937	3938	3939	3940	3941	3942	3943	3944	3945	3946	3947	3948	3949	3950	3951
F7_	3952	3953	3954	3955	3956	3957	3958	3959	3960	3961	3962	3963	3964	3965	3966	3967
F8_	3968	3969	3970	3971	3972	3973	3974	3975	3976	3977	3978	3979	3980	3981	3982	3983
F9_	3984	3985	3986	3987	3988	3989	3990	3991	3992	3993	3994	3995	3996	3997	3998	3999
FA_	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012	4013	4014	4015
FB_	4016	4017	4018	4019	4020	4021	4022	4023	4024	4025	4026	4027	4028	4029	4030	4031
FC_	4032	4033	4034	4035	4036	4037	4038	4039	4040	4041	4042	4043	4044	4045	4046	4047
FD_	4048	4049	4050	4051	4052	4053	4054	4055	4056	4057	4058	4059	4060	4061	4062	4063
FE_	4064	4065	4066	4067	4068	4069	4070	4071	4072	4073	4074	4075	4076	4077	4078	4079
FF_	4080	4081	4082	4083	4084	4085	4086	4087	4088	4089	4090	4091	4092	4093	4094	4095

Figure 1-9. Decimal/Hexadecimal Conversion Table (Part 2 of 2)

Dec	Bin	Hex	Dec	Bin	Hex
0	0000	0	8	1000	8
1	0001	1	9	1001	9
2	0010	2	10	1010	A
3	0011	3	11	1011	B
4	0100	4	12	1100	C
5	0101	5	13	1101	D
6	0110	6	14	1110	E
7	0111	7	15	1111	F

The table to the left gives the decimal, binary, and hexadecimal coding for the full range of four binary bits, from zero through F_{16} and 15_{10}.

To convert a four-digit hexadecimal number to decimal, determine the decimal value of the three low-order hexadecimal digits in the main table, and add the value for the high-order digit, as shown in the extended chart to the right.

For conversion of decimal values beyond the main table, deduct the largest number in the table at the right that will yield a positive result. The related digit is the high-order hexadecimal digit. Determine the three remaining hexadecimal digits by converting the product of the above subtraction in the main table.

Hex	Dec	Hex	Dec
1000	4096	9000	36864
2000	8192	A000	40960
3000	12288	B000	45056
4000	16384	C000	49152
5000	20480	D000	53248
6000	24576	E000	57344
7000	28672	F000	61440
8000	32768		

20291

Hexadecimal	Load and Store Instructions
	Load Accumulator (LD)
C0XX	Contents of CSL at EA (I+DISP) are loaded into A
C1XX	Contents of CSL at EA (XR1+DISP) are loaded into A
C2XX	Contents of CSL at EA (XR2+DISP) are loaded into A
C3XX	Contents of CSL at EA (XR3+DISP) are loaded into A
C400XXXX	Contents of CSL at EA (Addr) are loaded into A
C500XXXX	Contents of CSL at EA (Addr +XR1) are loaded into A
C600XXXX	Contents of CSL at EA (Addr +XR2) are loaded into A
C700XXXX	Contents of CSL at EA (Addr +XR3) are loaded into A
C480XXXX	Contents of CSL at EA (V in CSL at Addr) are loaded into A
C580XXXX	Contents of CSL at EA (V in CSL at "Addr +XR1") are loaded into A
C680XXXX	Contents of CSL at EA (V in CSL at "Addr +XR2") are loaded into A
C780XXXX	Contents of CSL at EA (V in CSL at "Addr +XR3") are loaded into A
	Double Load (LDD)
C8XX	Contents of CSL at EA (I + DISP) and EA+1 are loaded into A and Q
C9XX	Contents of CSL at EA(XR1 + DISP) and EA+1 are loaded into A and Q
CAXX	Contents of CSL at EA (XR2 + DISP) and EA+1 are loaded into A and Q
CBXX	Contents of CSL at EA (XR3 + DISP) and EA+1 are loaded into A and Q
CC00XXXX	Contents of CSL at EA (Addr) and EA+1 are loaded into A and Q
CD00XXXX	Contents of CSL at EA (Addr +XR1) and EA+1 are loaded into A and Q
CE00XXXX	Contents of CSL at EA (Addr +XR2) and EA+1 are loaded into A and Q
CF00XXXX	Contents of CSL at EA (Addr +XR3) and EA+1 are loaded into A and Q
CC80XXXX	Contents of CSL at EA (V in CSL at Addr) and EA+1 are loaded into A and Q
CD80XXXX	Contents of CSL at EA (V in CSL at "Addr +XR1") and EA+1 are loaded into A and Q
CE80XXXX	Contents of CSL at EA (V in CSL at "ADDR +XR2") and EA+1 are loaded into A and Q
CF80XXXX	Contents of CSL at EA (V in CSL at "Addr +XR3") and EA+1 are loaded into A and Q
	Store Accumulator (STO)
D0XX	Contents of A are stored in CSL at EA (I+DISP)
D1XX	Contents of A are stored in CSL at EA (XR1+DISP)
D2XX	Contents of A are stored in CSL at EA (XR2+DISP)
D3XX	Contents of A are stored in CSL at EA (XR3+DISP)
D400XXXX	Contents of A are stored in CSL at EA (Addr)
D500XXXX	Contents of A are stored in CSL at EA (Addr +XR1)
D600XXXX	Contents of A are stored in CSL at EA (Addr +XR2)
D700XXXX	Contents of A are stored in CSL at EA (Addr +XR3)
D480XXXX	Contents of A are stored in CSL at EA (V in CSL at Addr)
D580XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR1")
D680XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR2")
D780XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR3")
	Double Store (STD)
D8XX	Contents of A and Q are stored in CSL at EA (I+DISP) and EA+1
D9XX	Contents of A and Q are stored in CSL at EA (XR1 +DISP) and EA+1
DAXX	Contents of A and Q are stored in CSL at EA (XR2 +DISP) and EA+1
DBXX	Contents of A and Q are stored in CSL at EA (XR3 +DISP) and EA+1
DC00XXXX	Contents of A and Q are stored in CSL at EA (Addr) and EA+1
DD00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR1) and EA+1
DE00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR2) and EA+1
DF00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR3) and EA+1
DC80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at Addr) and EA+1
DD80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR1") and EA+1
DE80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR2") and EA+1
DF80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR3") and EA+1
	Load Index (LDX)
60XX	Load expanded DISP into the Instruction Register
61XX	Load expanded DISP into Index Register 1
62XX	Load expanded DISP into Index Register 2
63XX	Load expanded DISP into Index Register 3
6400XXXX	Load Addr into the Instruction Register
6500XXXX	Load Addr into Index Register 1
6600XXXX	Load Addr into Index Register 2
6700XXXX	Load Addr into Index Register 3
6480XXXX	Load contents of CSL at Addr into the Instruction Register
6580XXXX	Load contents of CSL at Addr into Index Register 1
6680XXXX	Load contents of CSL at Addr into Index Register 2
6780XXXX	Load contents of CSL at Addr into Index Register 3

See Instruction Set Section for Meaning of Symbols

Hexadecimal	Load and Store Instructions
	Store Index (STX)
68XX	Store I in CSL at EA (I+DISP)
69XX	Store XR1 in CSL at EA (I+DISP)
6AXX	Store XR2 in CSL at EA (I+DISP)
6BXX	Store XR3 in CSL at EA (I+DISP)
6C00XXXX	Store I in CSL at EA (Addr)
6D00XXXX	Store XR1 in CSL at EA (Addr)
6E00XXXX	Store XR2 in CSL at EA (Addr)
6F00XXXX	Store XR3 in CSL at EA (Addr)
6C80XXXX	Store I in CSL at EA (V in CSL at Addr)
6D80XXXX	Store XR1 in CSL at EA (V in CSL at Addr)
6E80XXXX	Store XR2 in CSL at EA (V in CSL at Addr)
6F80XXXX	Store XR3 in CSL at EA (V in CSL at Addr)
	Store Status (STS)
28XX	Store status of indicators in CSL at EA (I+DISP)
29XX	Store status of indicators in CSL at EA (XR1+DISP)
2AXX	Store status of indicators in CSL at EA (XR2+DISP)
2BXX	Store status of indicators in CSL at EA (XR3+DISP)
2C00XXXX	Store status of indicators in CSL at EA (Addr)
2D00XXXX	Store status of indicators in CSL at EA (Addr+XR1)
2E00XXXX	Store status of indicators in CSL at EA (Addr+XR2)
2F00XXXX	Store status of indicators in CSL at EA (Addr+XR3)
2C80XXXX	Store status of indicators in CSL at EA (V in CSL at Addr)
2D80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR1")
2E80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR2")
2F80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR3")
2C40XXXX	Clear storage protect bit in CSL at EA (Addr)
2C41XXXX	Write storage protect bit in CSL at EA (Addr)
2D40XXXX	Clear storage protect bit in CSL at EA (Addr +XR1)
2D41XXXX	Write storage protect bit in CSL at EA (Addr +XR1)
2E40XXXX	Clear storage protect bit in CSL at EA (Addr +XR2)
2E41XXXX	Write storage protect bit in CSL at EA (Addr +XR2)
2F40XXXX	Clear storage protect bit in CSL at EA (Addr +XR3)
2F41XXXX	Write storage protect bit in CSL at EA (Addr +XR3)
2CC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at Addr)
2CC1XXXX	Write storage protect bit in CSL at EA (V in CSL at Addr)
2DC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR1")
2DC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr +XR1")
2EC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR2")
2EC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr +XR2")
2FC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR3")
2FC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr +XR3")
	Load Status (LDS)
2000	Set CARRY and OVERFLOW indicators OFF
2001	Set OVERFLOW ON and CARRY OFF
2002	Set OVERFLOW OFF and CARRY ON
2003	Set CARRY and OVERFLOW indicator ON
	Arithmetic Instructions
	Add (A)
80XX	Add contents of CSL at EA (I+DISP) to A
81XX	Add contents of CSL at EA (XR1+DISP) to A
82XX	Add contents of CSL at EA (XR2+DISP) to A
83XX	Add contents of CSL at EA (XR3+DISP) to A
8400XXXX	Add contents of CSL at EA (Addr) to A
8500XXXX	Add contents of CSL at EA (Addr +XR1) to A
8600XXXX	Add contents of CSL at EA (Addr +XR2) to A
8700XXXX	Add contents of CSL at EA (Addr +XR3) to A
8480XXXX	Add contents of CSL at EA (V in CSL at Addr) to A
8580XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") to A
8680XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") to A
8780XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") to A
	Double Add (AD)
88XX	Add contents of CSL at EA (I+DISP) and EA+1 to A and Q
89XX	Add contents of CSL at EA (XR1+DISP) and EA+1 to A and Q
8AXX	Add contents of CSL at EA (XR2+DISP) and EA+1 to A and Q
8BXX	Add contents of CSL at EA (XR3+DISP) and EA+1 to A and Q
8C00XXXX	Add contents of CSL at EA (Addr) and EA+1 to A and Q
8D00XXXX	Add contents of CSL at EA (Addr+XR1) and EA+1 to A and Q
8E00XXXX	Add contents of CSL at EA (Addr+XR2) and EA+1 to A and Q
8F00XXXX	Add contents of CSL at EA (Addr+XR3) and EA+1 to A and Q
8C80XXXX	Add contents of CSL at EA (V in CSL at Addr) and EA+1 to A and Q
8D80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 to A and Q
8E80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 to A and Q

17323B

Figure 1-10. Instruction Set (Part 1 of 3)

Hexadecimal	Arithmetic Instructions
8F80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 to A and Q
	Subtract (S)
90XX	Subtract contents of CSL at EA (I+DISP) from A
91XX	Subtract contents of CSL at EA (XR1+DISP) from A
92XX	Subtract contents of CSL at EA (XR2+DISP) from A
93XX	Subtract contents of CSL at EA (XR3+DISP) from A
9400XXXX	Subtract contents of CSL at EA (Addr) from A
9500XXXX	Subtract contents of CSL at EA (Addr+XR1) from A
9600XXXX	Subtract contents of CSL at EA (Addr+XR2) from A
9700XXXX	Subtract contents of CSL at EA (Addr+XR3) from A
9480XXXX	Subtract contents of CSL at EA (V in CSL at Addr) from A
9580XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") from A
9680XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") from A
9780XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") from A
	Double Subtract (SD)
98XX	Subtract contents of CSL at EA (I+DISP) and EA+1 from A and Q
99XX	Subtract contents of CSL at EA (XR1+DISP) and EA+1 from A and Q
9AXX	Subtract contents of CSL at EA (XR2+DISP) and EA+1 from A and Q
9BXX	Subtract contents of CSL at EA (XR3+DISP) and EA+1 from A and Q
9C00XXXX	Subtract contents of CSL at EA (Addr) and EA+1 from A and Q
9D00XXXX	Subtract contents of CSL at EA (Addr+XR1) and EA+1 from A and Q
9E00XXXX	Subtract contents of CSL at EA (Addr+XR2) and EA+1 from A and Q
9F00XXXX	Subtract contents of CSL at EA (Addr+XR3) and EA+1 from A and Q
9C80XXXX	Subtract contents of CSL at EA (V in CSL at Addr) and EA+1 from A and Q
9D80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 from A and Q
9E80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 from A and Q
9F80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 from A and Q
	Multiply (M)
A0XX	Multiply contents of CSL at EA (I+DISP) by A
A1XX	Multiply contents of CSL at EA (XR1+DISP) by A
A2XX	Multiply contents of CSL at EA (XR2+DISP) by A
A3XX	Multiply contents of CSL at EA (XR3+DISP) by A
A400XXXX	Multiply contents of CSL at EA (Addr) by A
A500XXXX	Multiply contents of CSL at EA (Addr+XR1) by A
A600XXXX	Multiply contents of CSL at EA (Addr+XR2) by A
A700XXXX	Multiply contents of CSL at EA (Addr+XR3) by A
A480XXXX	Multiply contents of CSL at EA (V in CSL at Addr) by A
A580XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR1") by A
A680XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR2") by A
A780XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR3") by A
	Divide (D)
A8XX	Divide A and Q by contents of CSL at EA (I+DISP)
A9XX	Divide A and Q by contents of CSL at EA (XR1+DISP)
AAXX	Divide A and Q by contents of CSL at EA (XR2+DISP)
ABXX	Divide A and Q by contents of CSL at EA (XR3+DISP)
AC00XXXX	Divide A and Q by contents of CSL at EA (Addr)
AD00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR1)
AE00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR2)
AF00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR3)
AC80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at Addr)
AD80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR1")
AE80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR2")
AF80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR3")
	Logical And (AND)
E0XX	AND contents of CSL at EA (I+DISP) with A
E1XX	AND contents of CSL at EA (XR1+DISP) with A
E2XX	AND contents of CSL at EA (XR2+DISP) with A
E3XX	AND contents of CSL at EA (XR3+DISP) with A
E400XXXX	AND contents of CSL at EA (Addr) with A
E500XXXX	AND contents of CSL at EA (Addr+XR1) with A
E600XXXX	AND contents of CSL at EA (Addr+XR2) with A
E700XXXX	AND contents of CSL at EA (Addr+XR3) with A
E480XXXX	AND contents of CSL at EA (V in CSL at Addr) with A
E580XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR1") with A
E680XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR2") with A
E780XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR3") with A

Hexadecimal	Arithmetic Instructions
	Logical Or (OR)
E8XX	OR contents of CSL at EA (I+DISP) with A
E9XX	OR contents of CSL at EA (XR1+DISP) with A
EAXX	OR contents of CSL at EA (XR2+DISP) with A
EBXX	OR contents of CSL at EA (XR3+DISP) with A
EC00XXXX	OR contents of CSL at EA (Addr) with A
ED00XXXX	OR contents of CSL at EA (Addr+XR1) with A
EE00XXXX	OR contents of CSL at EA (Addr+XR2) with A
EF00XXXX	OR contents of CSL at EA (Addr+XR3) with A
EC80XXXX	OR contents of CSL at EA (V in CSL at Addr) with A
ED80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR1") with A
EE80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR2") with A
EF80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Logical Exclusive Or (EOR)
F0XX	EOR contents of CSL at EA (I+DISP) with A
F1XX	EOR contents of CSL at EA (XR1+DISP) with A
F2XX	EOR contents of CSL at EA (XR2+DISP) with A
F3XX	EOR contents of CSL at EA (XR3+DISP) with A
F400XXXX	EOR contents of CSL at EA (Addr) with A
F500XXXX	EOR contents of CSL at EA (Addr+XR1) with A
F600XXXX	EOR contents of CSL at EA (Addr+XR2) with A
F700XXXX	EOR contents of CSL at EA (Addr+XR3) with A
F480XXXX	EOR contents of CSL at EA (V in CSL at Addr) with A
F580XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR1") with A
F680XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR2") with A
F780XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Shift Instructions
	Shift Left Logical A (SLA)
10*X	Contents of A shift left the number of shift counts in DISP
1100	Contents of A shift left the number of shift counts in XR1
1200	Contents of A shift left the number of shift counts in XR2
1300	Contents of A shift left the number of shift counts in XR3
	Shift Left Logical A & Q (SLT)
10*X	Contents of A and Q shift left the number of shift counts in DISP
1180	Contents of A and Q shift left the number of shift counts in XR1
1280	Contents of A and Q shift left the number of shift counts in XR2
1380	Contents of A and Q shift left the number of shift counts in XR3
	Shift Left And Count A (SLCA)
10*X	Contents of A shift left the number of shift counts in DISP
1140	Contents of A shift left the number of shift counts in XR1
1240	Contents of A shift left the number of shift counts in XR2
1340	Contents of A shift left the number of shift counts in XR3
	Shift Left And Count A & Q (SLC)
10*X	Contents of A and Q shift left the number of shift counts in DISP
11C0	Contents of A and Q shift left the number of shift counts in XR1
12C0	Contents of A and Q shift left the number of shift counts in XR2
13C0	Contents of A and Q shift left the number of shift counts in XR3
	Shift Right Logical A (SRA)
18*X	Contents of A shift right the number of shift counts in DISP
1900	Contents of A shift right the number of shift counts in XR1
1A00	Contents of A shift right the number of shift counts in XR2
1B00	Contents of A shift right the number of shift counts in XR3
	Shift Right A & Q (SRT)
18*X	Contents of A and Q shift right the number of shift counts in DISP
1980	Contents of A and Q shift right the number of shift counts in XR1
1A80	Contents of A and Q shift right the number of shift counts in XR2
1B80	Contents of A and Q shift right the number of shift counts in XR3
	Rotate Right A & Q (RTE)
18*X	Contents of A and Q rotate right the number of counts in DISP
19C0	Contents of A and Q rotate right the number of counts in XR1
1AC0	Contents of A and Q rotate right the number of counts in XR2
1BC0	Contents of A and Q rotate right the number of counts in XR3

29070

Figure 1-10. Instruction Set (Part 2 of 3)

Hexadecimal	Branch Instructions
	Branch Or Skip On Condition (BSC or BOSC)
48*X	Skip the next one-word instruction if ANY condition is sensed
4C*XXXXX	Branch to CSL at EA (Addr) on NO condition
4D*XXXXX	Branch to CSL at EA (Addr+XR1) on NO condition
4E*XXXXX	Branch to CSL at EA (Addr+XR2) on NO condition
4F*XXXXX	Branch to CSL at EA (Addr+XR3) on NO condition
4C*XXXXX	Branch to CSL at EA (V in CSL at Addr) on NO condition
4D*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR1") on NO condition
4E*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR2") on NO condition
4F*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR3") on NO condition
	Branch And Store Instruction Register (BSI)
40XX	Store next sequential address in CSL at EA (I+DISP) and Branch to EA+1
41XX	Store next sequential address in CSL at EA (XR1+DISP) and Branch to EA+1
42XX	Store next sequential address in CSL at EA (XR2+DISP) and Branch to EA+1
43XX	Store next sequential address in CSL at EA (XR3+DISP) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR1) and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR2) and Branch to EA+1
47*XXXXX	If NO condition is true, store nextsequential address in CSL at EA (Addr+XR3) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR1") and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL a: "Addr+XR2") and Branch to EA+1
47*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR3") and Branch to EA+1
	Modify Index and Skip (MDX)
70XX	ADD expanded DISP to I (no skip can occur)
71XX	ADD expanded DISP to XR1
72XX	ADD expanded DISP to XR2
73XX	ADD expanded DISP to XR3
74XXXXXX	Add expanded positive DISP to CSL at Addr (Add to memory)
7500XXXX	Add Addr to XR1
7600XXXX	Add Addr to XR2
7700XXXX	Add Addr to XR3
74XXXXXX	Add expanded negative DISP to CSL at Addr (Add to Memory)
7580XXXX	Add V in CSL at Addr to XR1
7680XXXX	Add V in CSL at Addr to XR2
7780XXXX	Add V in CSL at Addr to XR3
	Wait (WAIT)
3000	WAIT until manual start or until completion of an interrupt subroutine
	Compare (CMP)
B0XX	Compare A with contents of CSL at EA (I+DISP)
B1XX	Compare A with contents of CSL at EA (XR1+DISP)
B2XX	Compare A with contents of CSL at EA (XR2+DISP)
B3XX	Compare A with contents of CSL at EA (XR3+DISP)
B400XXXX	Compare A with contents of CSL at EA (Addr)
B500XXXX	Compare A with contents of CSL at EA (Addr+XR1)
B600XXXX	Compare A with contents of CSL at EA (Addr+XR2)
B700XXXX	Compare A with contents of CSL at EA (Addr+XR3)
B480XXXX	Compare A with contents of CSL at EA (V in CSL at Addr)
B580XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR1")
B680XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR2")
B780XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR3")
	Double Compare (DCM)
B8XX	Compare A and Q with contents of CSL at EA (I+DISP) and EA+1
B9XX	Compare A and Q with contents of CSL at EA (XR1+DISP) and EA+1
BAXX	Compare A and Q with contents of CSL at EA (XR2+DISP) and EA+1
BBXX	Compare A and Q with contents of CSL at EA (XR3+DISP) and EA+1
BC00XXXX	Compare A and Q with contents of CSL at EA (Addr) and EA+1
BD00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR1) and EA+1
BE00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR2) and EA+1
BF00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR3) and EA+1
BC80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at Addr) and EA+1
BD80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr +XR1") and EA+1
BE80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr +XR2") and EA+1
BF80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr +XR3") and EA+1
	I/O Instructions
	Execute I/O (XIO)
08XX	Execute IOCC in CSL at EA (I+DISP) and EA+1
09XX	Execute IOCC in CSL at EA (XR1+DISP) and EA+1
0AXX	Execute IOCC in CSL at EA (XR2+DISP) and EA+1
0BXX	Execute IOCC in CSL at EA (XR3+DISP) and EA+1
0C00XXXX	Execute IOCC in CSL at EA (Addr)and EA+1
0D00XXXX	Execute IOCC in CSL at EA (Addr+XR1) and EA+1
0E00XXXX	Execute IOCC in CSL at EA (Addr+XR2) and EA+1
0F00XXXX	Execute IOCC in CSL at EA (Addr+XR3) and EA+1
0C80XXXX	Execute IOCC in CSL at EA (V in CSL at Addr) and EA+1
0D80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR1") and EA+1
0E80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR2") and EA+1
0F80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR3") and EA+1

Symbol	Meaning
A	Accumulator
Q	Accumulator Extension
Addr	Contents of the address portion of a two-word instruction
CSL	Core storage location
DISP	Contents of the displacement portion of a one-word instruction
EA	Effective address
EA + 1	Next higher address from the effective address
I	Contents of the Instruction Register
V	Value
XR1	Contents of Index Register 1
XR2	Contents of Index Register 2
XR3	Contents of Index Register 3
X	Hexadecimal value can be 0-F
*	Used for hexadecimal values that have limits

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Figure 1-10. Instruction Set (Part 3 of 3)

Compare Result	I Register Modification
A > C (EA)	I = I
A < C (EA)	I = I + 1
A = C (EA)	I = I + 2

14157

Figure 1-11. Results of Compare Instruction

Compare Result	I Register Modification
A and Q > C (EA) and C (EA + 1)	I = I
A and Q < C (EA) and C (EA + 1)	I = I + 1
A and Q = C (EA) and C (EA + 1)	I = I + 2

14158

Figure 1-12. Results of Double Compare Instruction

DESCRIPTION OF CHARTS

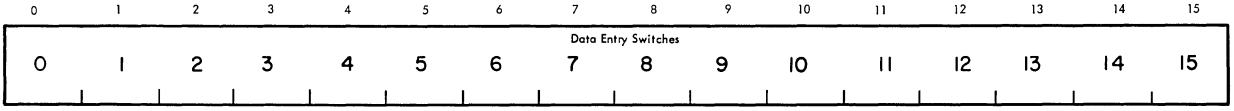
IOCC control word is given in hexadecimal form with function modifier shown when applicable. Control word is followed by functional description and data word(s). For all areas, Sense Interrupt command is 03XX; modifier XX (ILSW address) is placed on OUT bus automatically by Processor-Controller (see Figure 1-7).

C(IOCC address)=core storage location specified by IOCC address.

Internal (Area Zero)

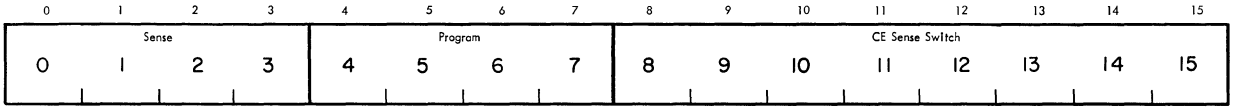
0240 Read Data Entry Switches: Store contents of switches at C(IOCC address).

Data Word



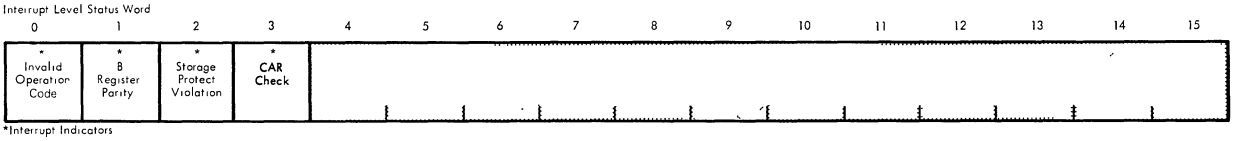
0260 Read Program Switches: Store contents of switches at C(IOCC address).

Data Word



0300 Sense Internal ILSW: Load status of indicators into A. Indicators are reset upon execution of this command.

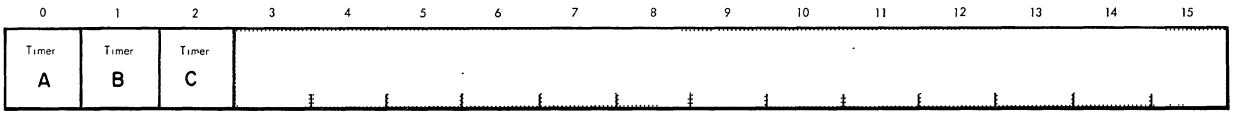
Interrupt Level Status Word



*Interrupt Indicators

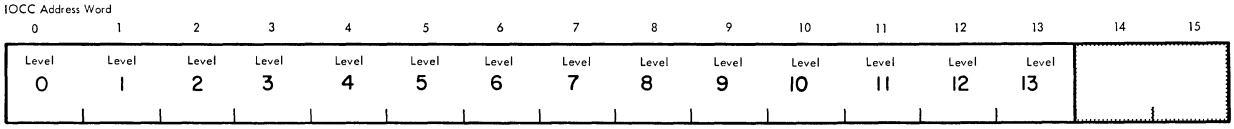
0420 Control Interval Timers: Start timer with "1" bit in designated position of IOCC address word; stop timer with "0" bit.

IOCC Address Word



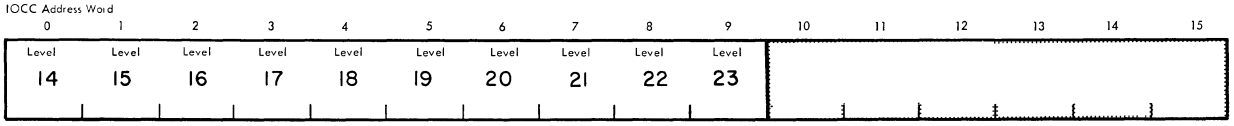
0480 Control Interrupt Mask Register 0-13: Mask interrupt level with "1" bit in designated position of IOCC address word; unmask interrupt level with "0" bit.

IOCC Address Word



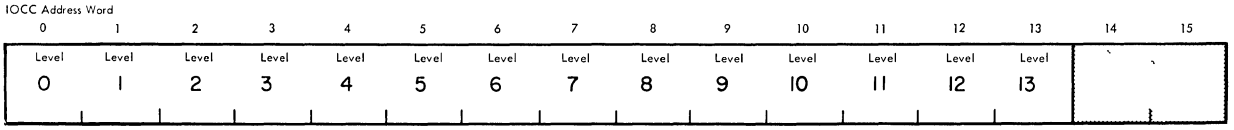
0481 Control Interrupt Mask Register 14-23: Mask interrupt level with "1" bit in designated position of IOCC address word; unmask interrupt level with "0" bit.

IOCC Address Word



04A0 Control Programmed Interrupt 0-13: Generate interrupt request with "1" bit in designated position of IOCC address word.

IOCC Address Word



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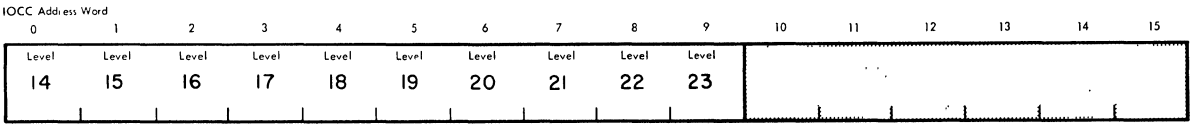
● Figure 1-13. XIO Operations (Part 1 of 15)

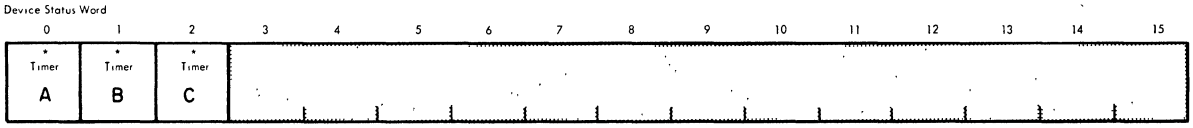
Internal (Area Zero) Continued

04A1 Control Programmed Interrupt 14-23: Generate interrupt request with "1" bit in designated position of IOCC address word.



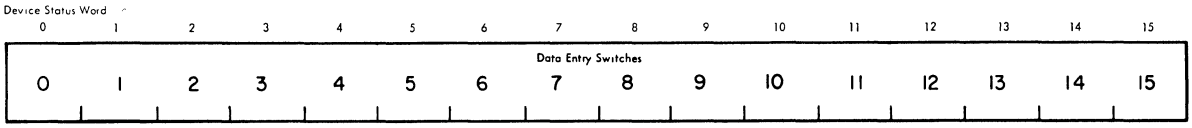
04E1 Control Operations Monitor: Reset monitor timer to full time period specified by Op Monitor switch. IOCC address word is not used.

0720/0721 Sense Interval Timer DSW: Load status of indicators into A. Indicators are reset by 0721 command only.

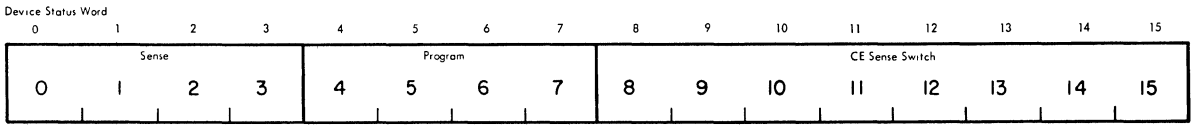


*Interrupt Indicators

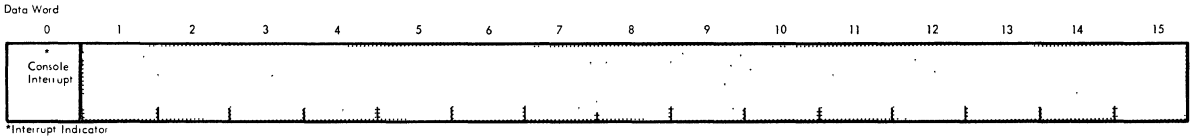
0740 Sense Data Entry Switches: Load contents of switches into A.



0760 Sense Program Switches: Load contents of switches into A.



07C0/07C1 Sense Console Interrupt DSW: Load indicator status into A. Indicator is reset by 07C1 command only.



*Interrupt Indicator

04A0 CE Cycle-Steal Test: Generate cycle-steal-request-test signal and cycle-steal-acknowledge-test signal. Signals are manually jumpered to desired cycle-steal level. See CE cycle-steal test description in text. IOCC address word is 0000.

1053 Printer and 1816 Printer-Keyboard

09XX (1st Adapter) **79XX** (2nd Adapter) Write: Load adapter buffer from C (IOCC address), analyze data, and send character signals to selected printer(s).

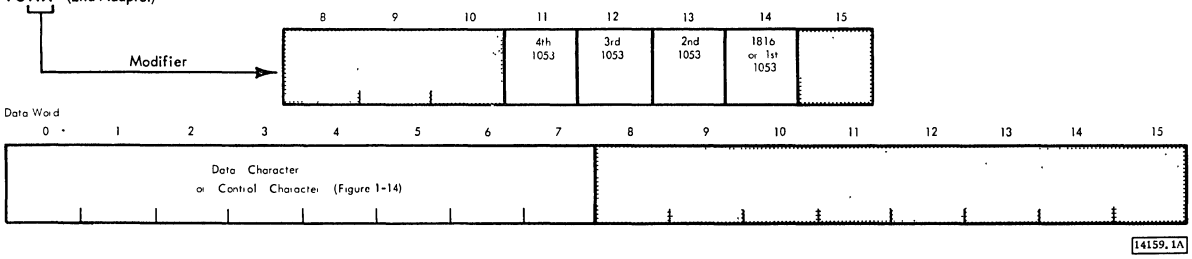


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Figure 1-13. XIO Operations (Part 2 of 15)

1053 Printer and 1816 Printer-Keyboard - Continued

0A02 (1st Adapter) **7A02** (2nd Adapter) Read: Store contents of keyboard contacts at C (IOCC address).

Data Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Keyboard Character (Figure 1-14)															

0C02 (1st Adapter) **7C02** (2nd Adapter) Control: Transmit signal from adapter to select (unlock) keyboard and turn on Proceed lamp. IOCC address word is not used.

0FXX (1st Adapter) **7FXX** (2nd Adapter) Sense DSW: Load status of device indicators into A.

Modifier →

8	9	10	11	12	13	14	15
			4th 1053	3rd 1053	2nd 1053	1816 or 1st 1053	1 = Reset † Indicators

Device Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
*† Printer Service Response	*† ① Keyboard Service Response	*† ① Keyboard Request		Printer Busy	Printer Not Ready	②① Keyboard Not Ready	† ① Storage Protect Violation	† ① Keyboard Parity Error	† Printer Parity Error			CE Busy	CE Not Ready		

*Interrupt Indicators ① Used by 1816 only ② If no 1816 in group, this indicator is active at all times

08XX (1st Adapter) **78XX** (2nd Adapter) Control CE Mode: Modifier bit 15 = 1 places selected device in CE mode. Modifier bit 15 = 0 removes device from CE mode. IOCC address word is not used.

Modifier →

8	9	10	11	12	13	14	15
			4th 1053	3rd 1053	2nd 1053	1816 or 1st 1053	1 = Set CE Mode 0 = Reset

1054 Paper Tape Reader and 1055 Paper Tape Punch

1900 Write: Load adapter punch buffer from C (IOCC address). Select punch magnet drivers from punch buffer data and energize punch clutch driver.

Data Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Channel 8	Channel 7	Channel 6	Channel 5	Channel 4	Channel 3	Channel 2	Channel 1								

1A00 Read: Store contents of adapter read buffer at C (IOCC address). Data word is same as for Write command.

1C10 Control: Load contents of tape sensing contacts into adapter read buffer. Energize reader clutch to advance tape one character position. IOCC address word is not used.

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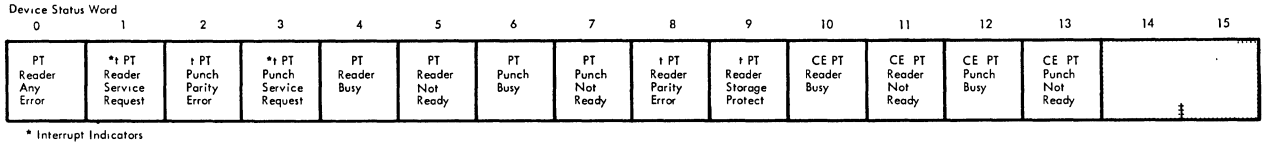
Figure 1-13. XIO Operations (Part 3 of 15)

1054 Paper Tape Reader and 1055 Paper Tape Punch - Continued

1F00 / 1F01 Sense DSW: Load status of device indicators into A. Indicators (t) are reset by 1F01 command only.

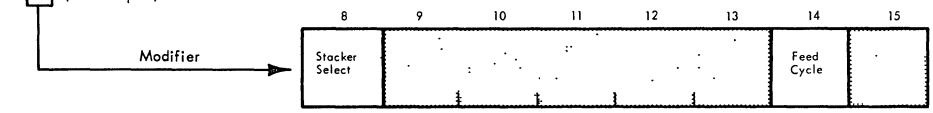


* Interrupt Indicators

1800 / 1801 Control CE Mode: 1801 command places 1054-1055 in CE mode. 1800 command removes 1054-1055 from CE mode. IOCC address word is not used.

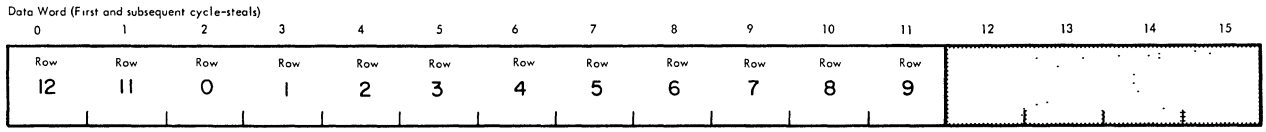
1442 Card Read Punch

14XX (1st Adapter) Control: Transmit control signals from adapter to CRP to perform a feed cycle and/or a stacker select operation. IOCC address word is not used.
8CXX (2nd Adapter)



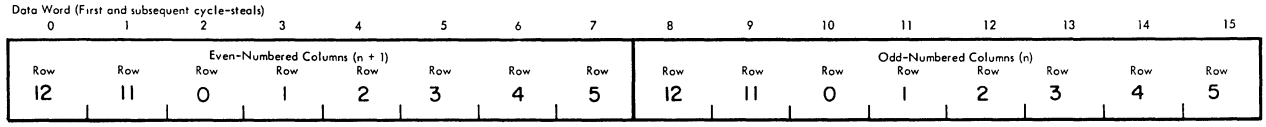
1500 (1st Adapter) Initialize Write: Set up adapter data channel controls for transferring data from core storage to the adapter on a cycle-steal basis. Load IOCC address word into CAR.
8D00 (2nd Adapter)

Note: 1442 adapter does not employ a word counter.

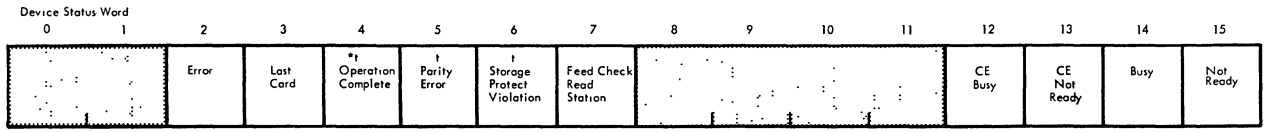


1600 (1st Adapter) Initialize Read (Card Image Mode): Set up adapter data channel controls for transferring data from the adapter to core storage on a cycle-steal basis. Load IOCC address word into CAR. Data word is same as for Initialize Write command.
8E00 (2nd Adapter)

1601 (1st Adapter) Initialize Read (Packed Mode): Set up adapter data channel controls for transferring data from the adapter to core storage on a cycle-steal basis. Load IOCC address word into CAR.
8E01 (2nd Adapter)



1700/1701 (1st Adapter) Sense DSW: Load status of device indicators into A. Indicators (t) are reset by modifier 01 only.
8F00/8F01 (2nd Adapter)



* Interrupt Indicator

1000/1001 (1st Adapter) Control CE Mode: Modifier 01 places 1442 in CE mode. Modifier 00 removes 1442 from CE mode. IOCC address word is not used.
8800/8801 (2nd Adapter)

14159.3A

Figure 1-13. XIO Operations (Part 4 of 15)

1443 Printer

3400 Control Carriage: Load IOCC address word (bits 2-7) into adapter print buffer, analyze data, and send carriage control signal to printer.

IOCC Address Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Control Character (Figure 1-15)															

3500 / 3501 Initialize Write: Set up adapter data channel controls for transferring data from core storage to the adapter on a cycle-steal basis. Load IOCC address word into CAR. 3501 command suppresses the line space after print.

Word-Count Word (First cycle-steal)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
									WC 64	WC 32	WC 16	WC 8	WC 4	WC 2	WC 1

Data Word (Second and subsequent cycle-steals)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Left Print Character (Figure 1-14)								**Right Print Character** (Figure 1-14)							
B	A	8	4	2	1			B	A	8	4	2	1		

3700 / 3701 Sense DSW: Load status of device indicators into A. Indicators (t) are reset by 3701 command only.

Device Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
*t Transfer Complete	Error	*t Printer Complete	Channel 9	Channel 12	Channel 1	t Parity				CE Carriage Busy	CE Printer Busy	CE Printer Not Ready	Carriage Busy	Printer Busy	Printer Not Ready

* Interrupt Indicators

3000 / 3001 Control CE Mode: 3001 command places 1443 in CE mode. 3000 command removes 1443 from CE mode. IOCC address word is not used.

1627 Plotter

2900 Write: Load adapter buffer from C (IOCC address). Actuate plotter controls from buffer data.

Data Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Pen Down	Drum Down	Drum Up	Carriage Right	Carriage Left	Pen Up										

2F00 / 2F01 Sense DSW: Load status of device indicators into A. Indicators (t) are reset by 2F01 command only.

Device Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
*t Service Response	t Parity Error											CE Busy	CE Not Ready	Busy	Not Ready

* Interrupt Indicator

2800 / 2801 Control CE Mode: 2801 command places 1627 in CE mode. 2800 command removes 1627 from CE mode. IOCC address word is not used.

14159.4A

Figure 1-13. XIO Operations (Part 5 of 15)

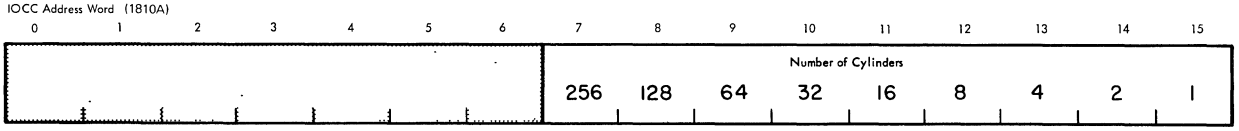
1810 Disk Storage

Model A

2400/2404 (1st Drive)
4400/4404 (2nd Drive)
4C00/4C04 (3rd Drive)

Control Carriage: Load IOCC address word into adapter word counter to specify number of cylinders to be accessed. Modifier 00 moves carriage forward. Modifier 04 moves carriage in reverse.

IOCC Address Word (1810A)

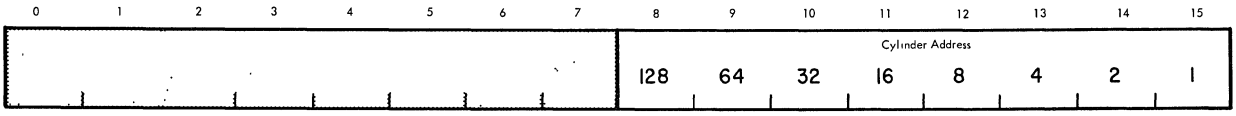


Model A

2400 (1st Drive)
4400 (2nd Drive)
4C00 (3rd Drive)

Control Carriage: IOCC address word specifies the absolute cylinder address.

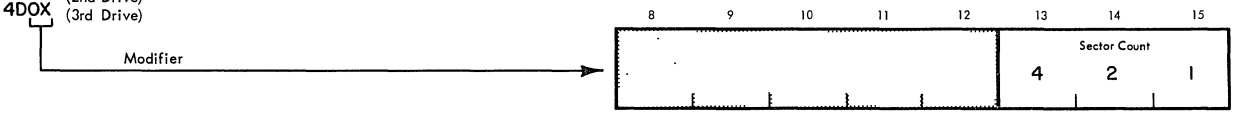
IOCC Address Word (1810B)



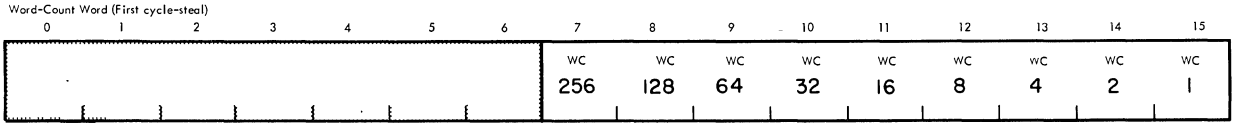
Models A and B

250X (1st Drive)
450X (2nd Drive)
4D0X (3rd Drive)

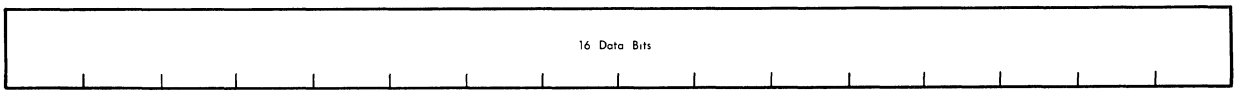
Initialize Write: Set up adapter data channel controls for transferring data from core storage to the adapter on a cycle-steal basis. Load IOCC address word into CAR.



Word-Count Word (First cycle-steal)



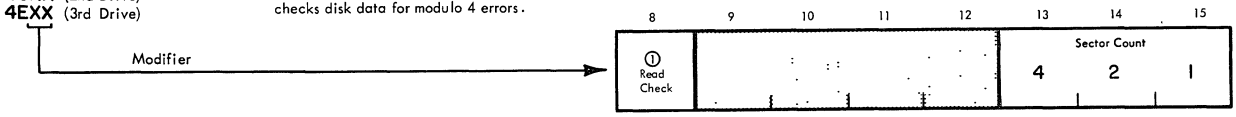
Data Word (Second and subsequent cycle-steals)



Models A and B

26XX (1st Drive)
46XX (2nd Drive)
4EXX (3rd Drive)

Initialize Read: Set up adapter data channel controls for transferring data from the adapter to core storage on a cycle-steal basis. Load IOCC address word into CAR. Word-count word and data word are same as for Initialize Write command. A read check operation does not read into core storage, it simply checks disk data for modulo 4 errors.



① 0 = Read into core, 1 = Read Check

Models A and B

2700/2701 (1st Drive)
4700/4701 (2nd Drive)
4F00/4F01 (3rd Drive)

Sense DSW: Load status of device indicators into A. Indicators (†) are reset by modifier 01 only. Indicator (‡) is reset by modifier 01 only if operation is complete.

Device Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
† Any Error	*† Operation Complete	Disk Not Ready	Disk Busy (R/W or Ctrl)	Carriage Home	† Parity Error	† Storage Protect Error	‡ Data Error	Write Select Error	† Data Overrun	‡ Seek Error 1810B	CE Not Ready	CE Busy	Fast Access 2310C	Sector Counter High	Sector Counter Low

* Interrupt Indicator

Models A and B

2000/2001 (1st Drive)
4000/4001 (2nd Drive)
4800/4801 (3rd Drive)

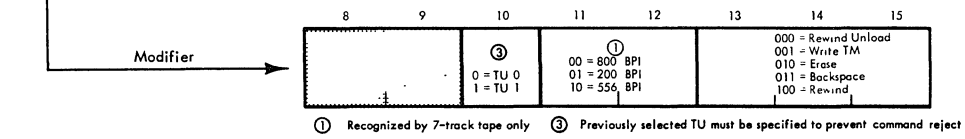
Control CE Mode: Modifier 01 places 1810 in CE mode. Modifier 00 removes 1810 from CE mode. IOCC address word is not used.

16265 A

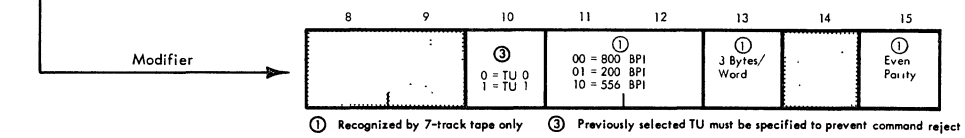
● Figure 1-13. XIO Operations (Part 6 of 15)

Tape Control Unit

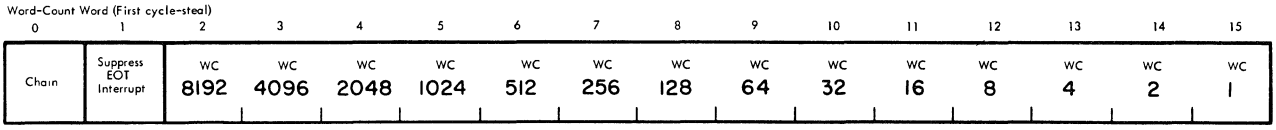
74XX Control: Transmit control signals to the tape unit to perform the designated control function. IOCC address word is not used.



75XX Initialize Write: Set up TCU data channel controls for transferring data from core storage to the TCU on a cycle-steal basis. Load IOCC address word into CAR.

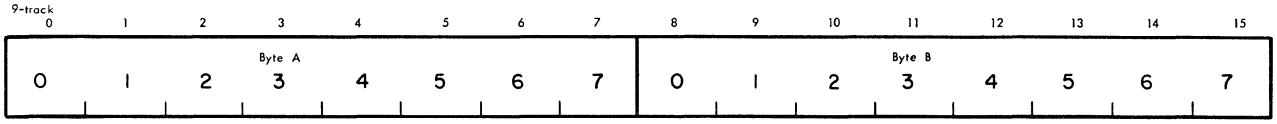


Word-Count Word (First cycle-steal)

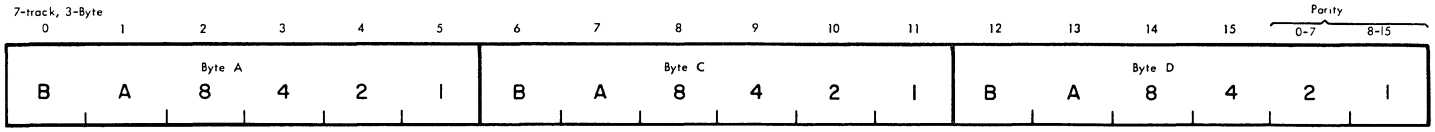


Data Words (Second and subsequent cycle-steals)

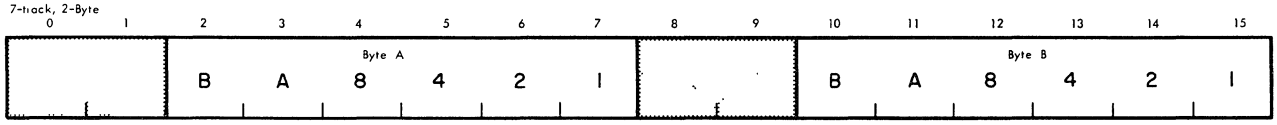
9-track



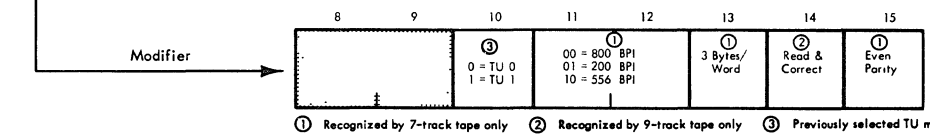
7-track, 3-Byte



7-track, 2-Byte



76XX Initialize Read: Set up TCU data channel controls for transferring data from the TCU to core storage on a cycle-steal basis. Load IOCC address word into CAR. Word-count word and data words are same as for Initialize Write command.



14159.6A

Figure 1-13. XIO Operations (Part 7 of 15)

Tape Control Unit - Continued

77XX Sense DSW: If bit 11=0, load status of device indicators into A. If bit 11=1, load contents of word counter into A.

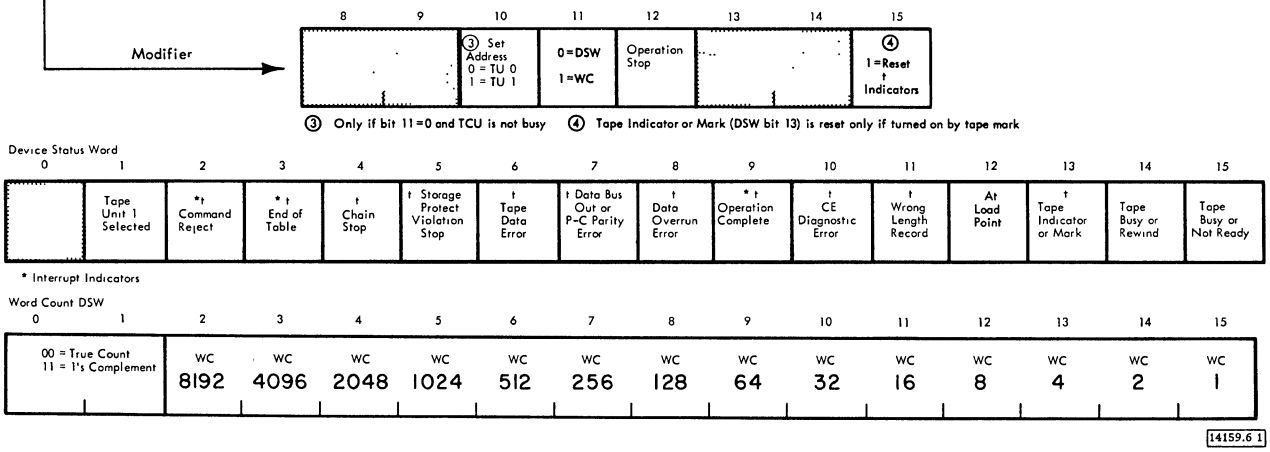


Figure 1-13. XIO Operations (Part 8 of 15)

System/360 Adapter

6C00 Control (Blast Reset): Generate a d-c reset to all adapter controls and registers. IOCC address word is not used.

6D00 Initialize Write: Load IOCC control word (6D00) into adapter buffer and set up adapter data channel controls for transferring data from 1800 core storage to the adapter on a cycle-steal basis. Load IOCC address word into CAR.

Word-Count Word (First cycle-steal)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Chain	Suppress EOT Interrupt	WC 8192	WC 4096	WC 2048	WC 1024	WC 512	WC 256	WC 128	WC 64	WC 32	WC 16	WC 8	WC 4	WC 2	WC 1

Data Word (Second and subsequent cycle-steals)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Byte 1								Byte 2							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7

6E00 Initialize Read: Load IOCC control word (6E00) into adapter buffer and set up adapter data channel controls for transferring data from the adapter to 1800 core storage on a cycle-steal basis. Load IOCC address word into CAR. Word-count word and data word are same as for Initialize Write command.

6FXX Sense DSW: If bit 8=0, load status of device indicators and 360 command byte into A. If bit 8=1, load contents of word counter into A.

Modifier

8	9	10	11	12	13	14	15
0 = DSW 1 = WC							1 = Reset t Indicators

Device Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
* † Command Reject	1800 Command Stored	* 360 ① Command Stored	* † Halt	* † Data Check	* † Storage Protect Violation	* † Transfer End	* † End of Table	360 Command							

*Interrupt Indicators ① Conditional Interrupt. Interrupt will be suppressed by 1800 Command Stored (bit 1 on) or by setting bit 5 of the 360 Read or Write command. If this indicator is set by 360 Read, Read Backward, or Write command, it remains on until transfer end.

Word Count DSW

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	WC 8192	WC 4096	WC 2048	WC 1024	WC 512	WC 256	WC 128	WC 64	WC 32	WC 16	WC 8	WC 4	WC 2	WC 1	

Analog Input

51XX (Basic) **81XX** (Expander) Write: Load AMAR with MPX address from C (IOCC address). Initiate conversion of selected input signal.

Modifier

8	9	10	11	12	13	14	15
External Sync			00 = 11-Bit Res 01 = 14-Bit Res 10 = 8-Bit Res				

Data Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			0 = Relay 1 = Solid-State			Multiplexer Address (Figure 1-19)									
						512	256	128	64	32	16	8	4	2	1

5200/5280 (Basic) **8200/8280** (Expander) Read: Store contents of ADC register at C (IOCC address). Modifier 80 increments AMAR and initiates conversion of input signal at new address (sequential operation).

Data Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ADC Neg	ADC 8192	ADC 4096	ADC 2048	ADC 1024	ADC 512	ADC 256	ADC 128	ADC 64	ADC 32	ADC 16	ADC 8	ADC 4	ADC 2	ADC 1	ADC Overload

14159.7A

Figure 1-13. XIO Operations (Part 9 of 15)

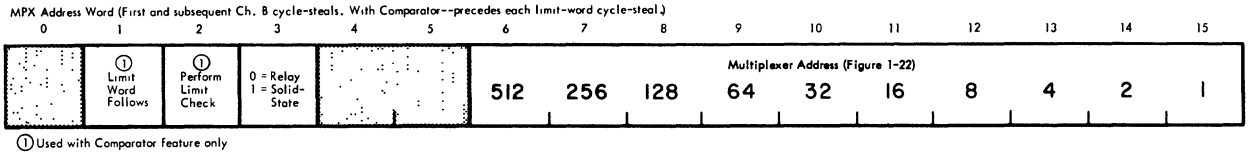
Analog Input - Continued

5400 (Basic) **8400** (Expander) Control (Blast Reset): Generate a d-c reset to all AI controls and registers except AMAR and Limit Error AMAR Buffer. IOCC address word is not used.

5500 (Basic) **8500** (Expander) Initialize Write: Set up data-channel-B controls for transferring MPX addresses and limit words ① from core storage to AMAR on a cycle-steal basis. Load IOCC address word into CAR-B.

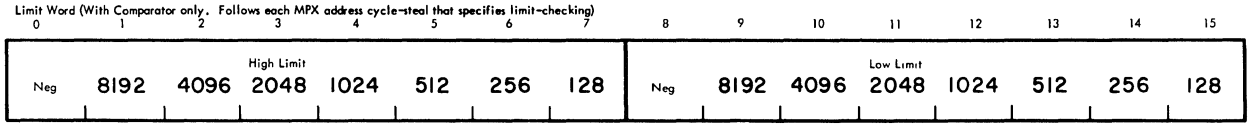
Note: Data-channel-B adapter does not employ a word counter.

MPX Address Word (First and subsequent Ch. B cycle-steals. With Comparator--precedes each limit-word cycle-steal.)

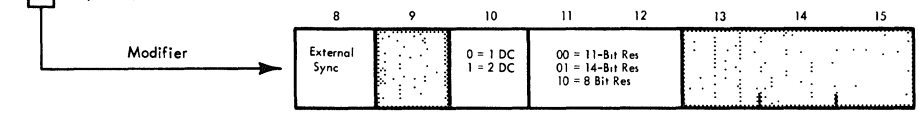


① Used with Comparator feature only

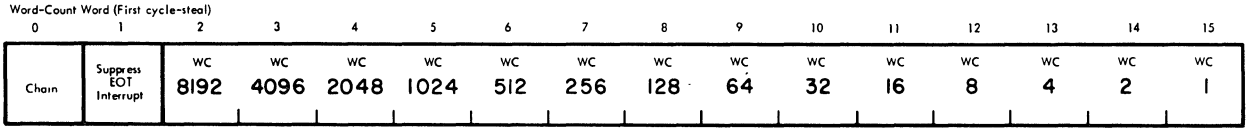
Limit Word (With Comparator only. Follows each MPX address cycle-steal that specifies limit-checking)



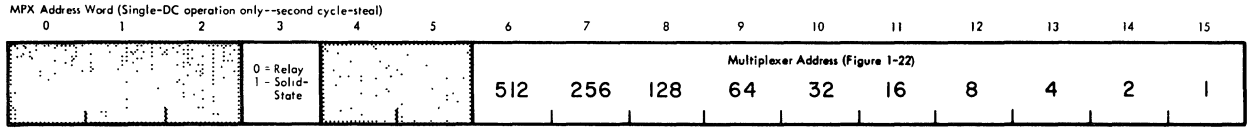
56XX (Basic) **86XX** (Expander) Initialize Read: Set up data-channel-A controls for transferring data from ADC register to core storage on a cycle-steal basis. Load IOCC address word into CAR-A.



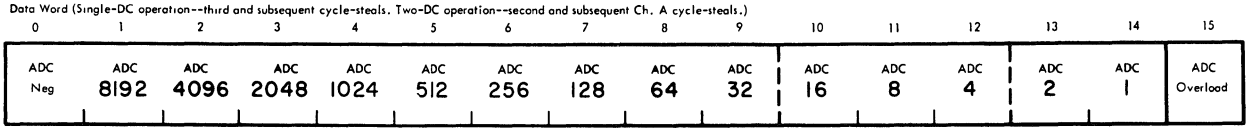
Word-Count Word (First cycle-steal)



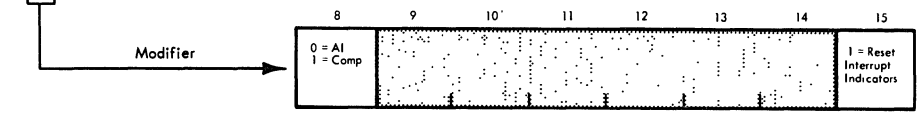
MPX Address Word (Single-DC operation only--second cycle-steal)



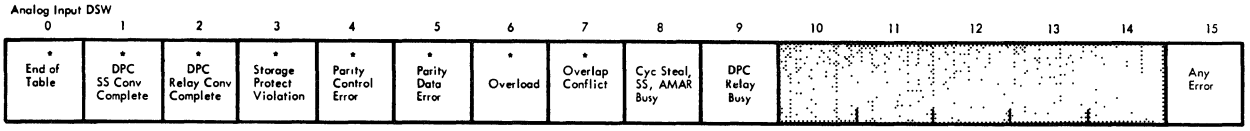
Data Word (Single-DC operation--third and subsequent cycle-steals. Two-DC operation--second and subsequent Ch. A cycle-steals.)



57XX (Basic) **87XX** (Expander) Sense DSW: Load status of device indicators into A.

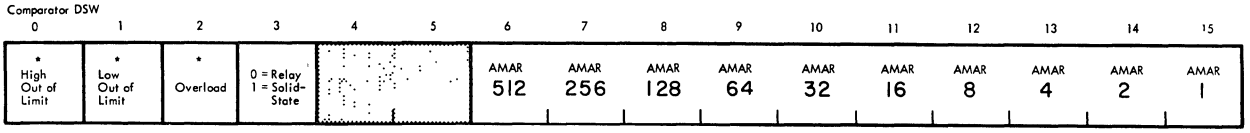


Analog Input DSW



* Interrupt Indicators

Comparator DSW



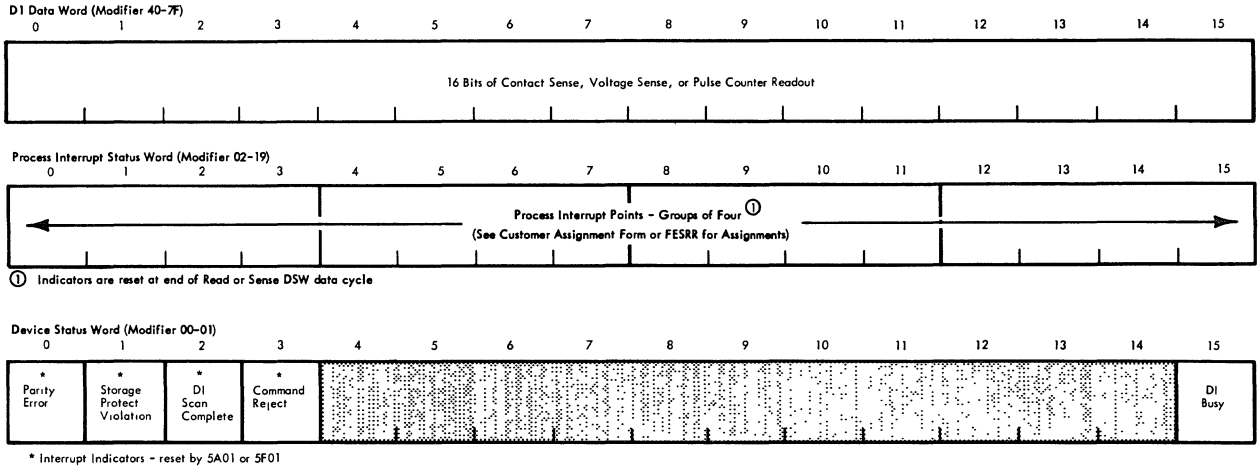
* Interrupt Indicators

14159 8

Figure 1-13. XIO Operations (Part 10 of 15)

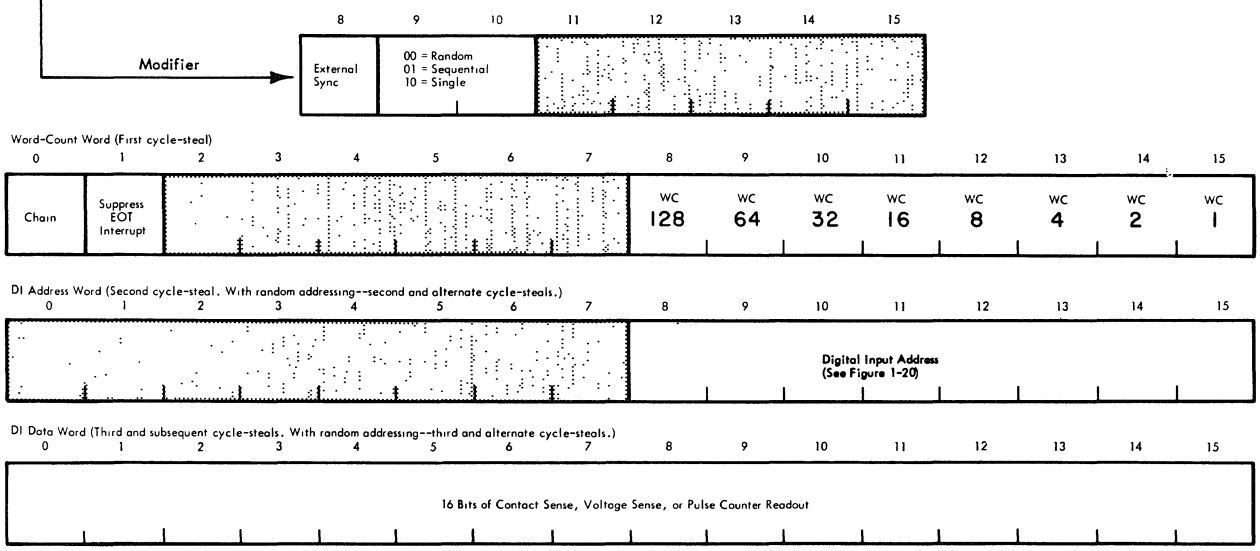
Digital Input

5AXX Read: Store digital input group specified by modifier XX (Figures 1-19 and 1-20) at C (IOCC address).



5C20 Control (Blast Reset): Generate a d-c reset to DI controls. IOCC address word is not used.

5EXO Initialize Read: Set up DI data channel controls for transferring data from a single address, sequential addresses, or random addresses to core storage on a cycle-steal basis. Load IOCC address word into CAR.



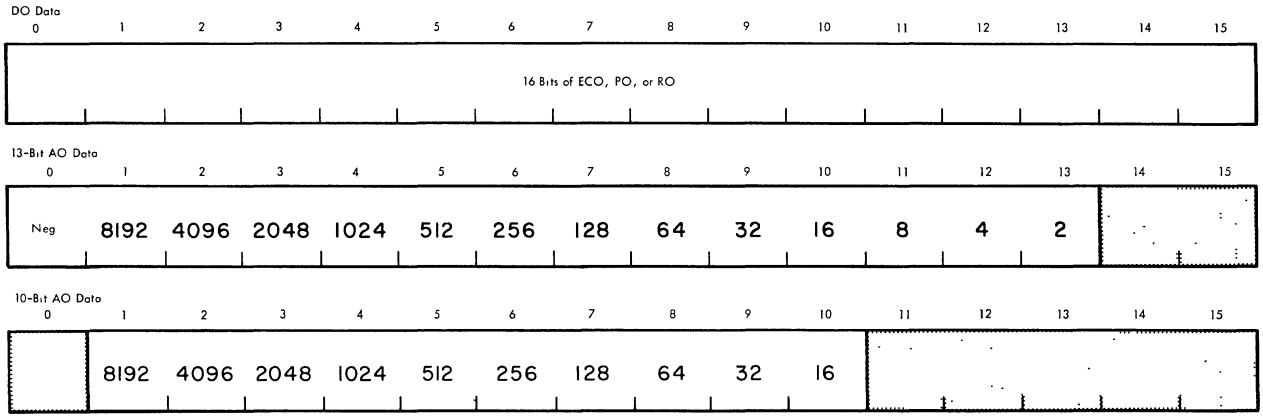
5FXX Sense DSW: Load digital input group specified by modifier XX (Figures 1-19 and 1-20) into A. Data words are same as for Read command.

14159 9

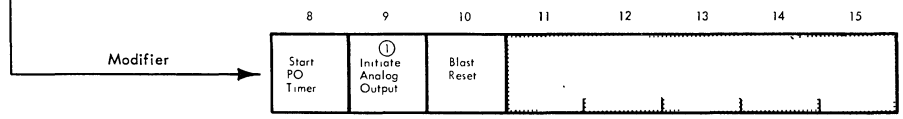
Figure 1-13. XIO Operations (Part 11 of 15)

Digital and Analog Output

61XX Write: Load DAO register specified by modifier XX (Figure 1-21) with data from C (IOCC address).

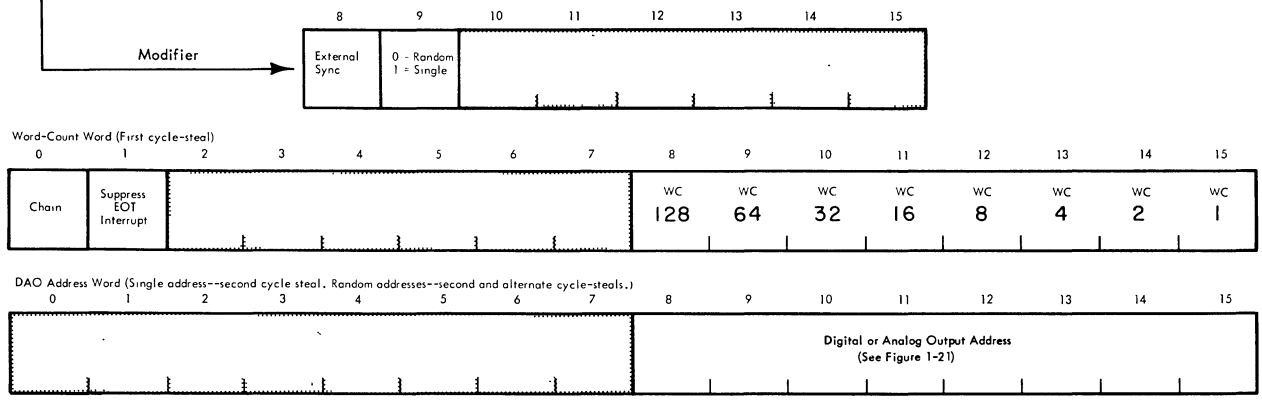


64X0 Control: Perform the control function specified by modifier bits. IOCC address word is not used.



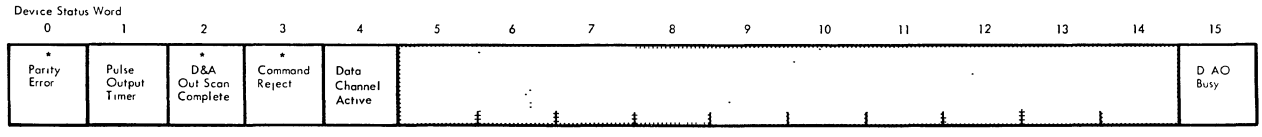
① Recognized only by DAC mod 3 or 4 with Buffer Register

65X0 Initialize Write: Set up DAO data channel controls for transferring data from core storage to DAO registers (single or random) on a cycle-steal basis. Load IOCC address word into CAR.



Data words are same as for Write command. (Single address--third and subsequent cycle-steals. Random addresses--third and alternate cycle-steals.)

6700 / 6701 Sense DSW: Load status of device indicators into A. Interrupt indicators are reset by 6701 command only.



* Interrupt Indicators

6400 / 6401 Control CE Test Pulse: Modifier bit 15 = 1 sets test pulse. Modifier bit 15 = 0 resets test pulse. IOCC address word is not used.

14159.10A

Figure 1-13. XIO Operations (Part 12 of 15)

Communications Adapter

ADXX (1st CA)
B5XX (2nd CA)
BDXX (3rd CA)
A5XX (4th CA)

Initialize: Prepare CA to transmit or receive (per bit 2 in byte count word of data table).

Modifier

8	9	10	11	12	13	14	15
Diag-nostic Mode	0=Line 0 1=Line 1	Continue Timer	Enable	Clear CA			

Byte Count Word (First cycle-steal)

0	1	2	3	4	5	6	7	8	11	12	13	14	15
Chaining	Suppr Table Comp Intrpt	0=Receive 1=Transmit	Suppr Timeout Intrpt	2048	1024	512	256	128	Byte Count 16	8	4	2	1

Data Word (Second and subsequent cycle-steals)

0	1	2	3	4	5	6	7	8	11	12	13	14	15
Character 1*									Character 2*				
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**3**	**4**	**5**	**6**	**7**

* EBCDIC characters shown.

AFXX (1st CA)
B7XX (2nd CA)
BFXX (3rd CA)
A7XX (4th CA)

Sense DSW: Load DSW (specified by modifier bits 13 and 14) into A register.

Modifier

8	9	10	11	12	13	14	15
Prog Receive Input	0=Line 0 1=Line 1	Continue Timer	Enable	Clear CA	Operating DSW =00 Diagnostic DSW =01 Byte Count DSW=10 Illegal =11		Reset Indicators

Operating Device Status Word

0	1	2	3	4	5	6	7	8	9	10	13	14	15
*† Channel Stop	*† Stor Prot Violation	*† Timed Out	*† End Char Decoded or Ringing	*† Table Complete	† Parity Check	† BCC Check	† Data Overrun	Data Set Ready	*† Command Reject	Carrier On			

* Causes Interrupt
† Reset by Sense DSW. Others reset by their status turn-off.

Diagnostic Device Status Word

0	1	2	3	4	5	6	7	8	9	10	13	14	15
* CE Jumperable	Char Phase	Char 1 FF	Not Clear to Send	Transparent Tr FF	Text Tr FF	End Tr FF	Transmit Line Bit			Serdes	0-7		

* If not jumpered, a 1 is set.

Byte Count Device Status Word

0	1	2	3	4	5	6	7	8	9	10	13	14	15
CE Jumperable*			Transmit Latch	2048	1024	512	256	128	64	32	4	2	1

* If not jumpered, 1's are set.

12465

● Figure 1-13. XIO Operations (Part 13 of 15)

Selector Channel

970X Sense Device: Load CSW-1,-2,-3, or -4 into A. IOCC address word not used.

Modifiers

12	13	14	15
Suppress Polling	CSW Selection	CSW Selection	Reset

13	14	
0	0	CSW - 1 to A
0	1	CSW - 2 to A
1	0	CSW - 3 to A
1	1	CSW - 4 to A

CHANNEL STATUS WORD (CSW)

CSW - 1 Selector Channel Status

0	1	2	3	4	5	6	7	8	11	12	13	14	15
* Not Operational	* Unit Status Pending	* Program Control Interrupt	* Program Check	Channel Data Check	Interface Control Check	Incorrect Length	Adapter Busy	Unit Operational		Not Used			

* Interrupt Indicators

CSW - 2 Unit Address/Status

0	1	2	3	4	7	8	9	10	11	12	13	14	15
Control Unit Address				Device	Address	Attention	Status Modifier	Control Unit End	Busy	Channel End	Device End	Unit Check	Unit Exception

Unit Address — Identifies the control unit and device specified in the last I/O operation executed or rejected.

Unit Status

CSW - 3 Command Address

0	1	2	3	4	5	6	7	8	11	12	13	14	15
Contents of CCW Address									Register				

The CCW Address Register contains an address 3 higher than the address of the CCW being executed or just completed.

CSW - 4 Byte Count

0	1	2	3	4	7	8	9	10	11	12	13	14	15
32,768	16,384	8,192		(Contents of	Byte Counter)			32	16	8	4	2	1

The byte counter contains the two's complement +1 of the actual byte count. Example byte count = /0004, byte counter = /FFFD.

94XX Halt I/O (control) Terminates I/O operation in progress; resets selector channel and/or I/O unit. IOCC address word not used.

8	9	10	11	12	13	14	15
Control Unit Address				Device Address			

Unit Address

95XX Start I/O Performs I/O operation specified by CCW. CCW located at address specified in IOCC address word.

8	9	10	11	12	13	14	15
Control Unit Address				Device Address			

Unit Address

12466.0

● Figure 1-13. XIO Operations (Part 14 of 15)

Selector Channel-Continued

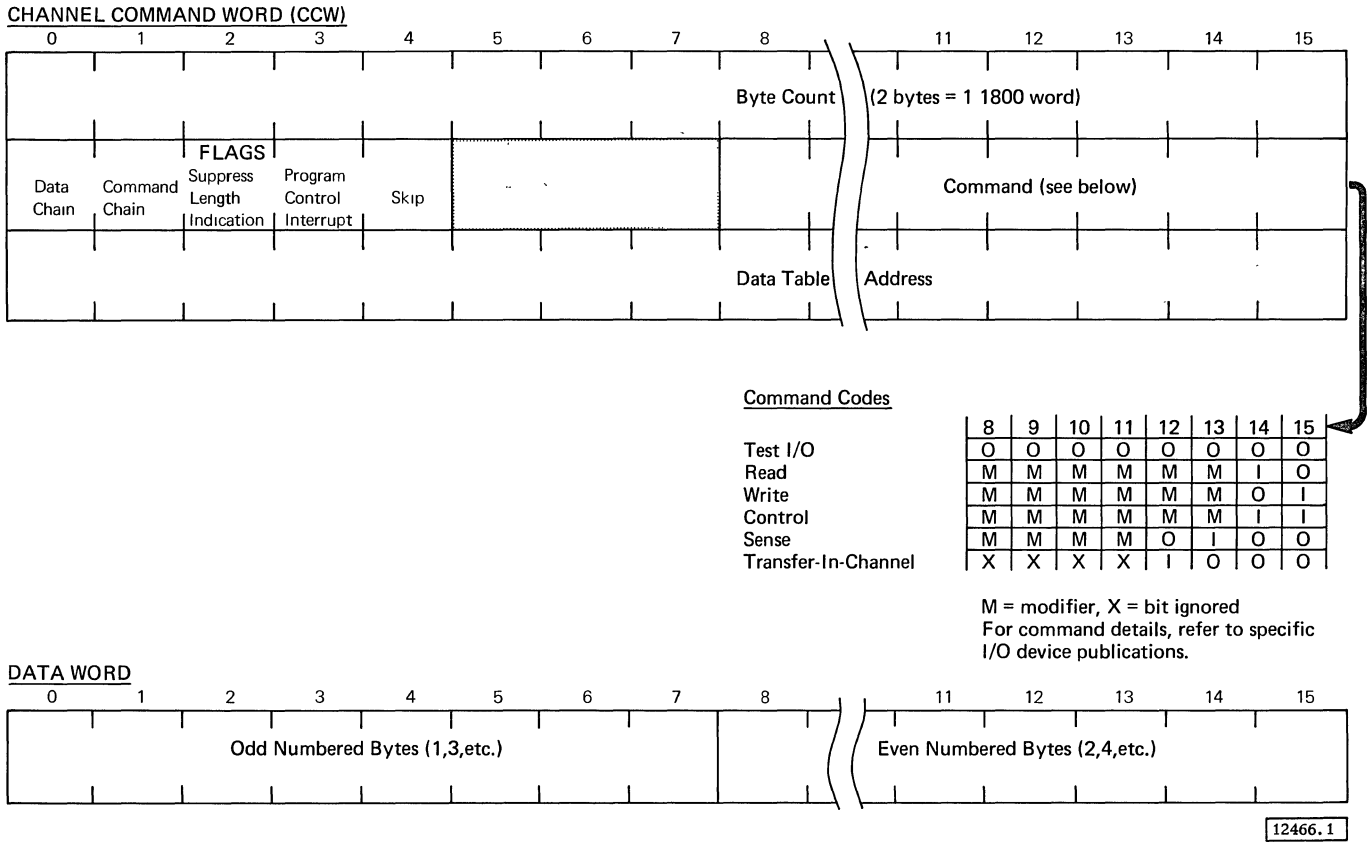


Figure 1-13. XIO Operations (Part 15 of 15)

Character	1053/1816 Printer		1816 Keyboard/1442		1443 Printer	
	Lower Case (hex)	Upper Case (hex)	Hex	IBM Card Code	Hex 2 Char/ Word	BCD
A	3C00	3E00	9000	12,1	31	B,A,1
B	1800	1A00	8800	12,2	32	B,A,2
C	1C00	1E00	8400	12,3	33	B,A,2,1
D	3000	3200	8200	12,4	34	B,A,4
E	3400	3600	8100	12,5	35	B,A,4,1
F	1000	1200	8080	12,6	36	B,A,4,2
G	1400	1600	8040	12,7	37	B,A,4,2,1
H	2400	2600	8020	12,8	38	B,A,8
I	2000	2200	8010	12,9	39	B,A,8,1
J	7C00	7E00	5000	11,1	21	B,1
K	5800	5A00	4800	11,2	22	B,2
L	5C00	5E00	4400	11,3	23	B,2,1
M	7000	7200	4200	11,4	24	B,4
N	7400	7600	4100	11,5	25	B,4,1
O	5000	5200	4080	11,6	26	B,4,2
P	5400	5600	4040	11,7	27	B,4,2,1
Q	6400	6600	4020	11,8	28	B,8
R	6000	6200	4010	11,9	29	B,8,1
S	9800	9A00	2800	0,2	12	A,2
T	9C00	9E00	2400	0,3	13	A,2,1
U	B000	B200	2200	0,4	14	A,4
V	B400	B600	2100	0,5	15	A,4,1
W	9000	9200	2080	0,6	16	A,4,2
X	9400	9600	2040	0,7	17	A,4,2,1
Y	A400	A600	2020	0,8	18	A,8
Z	A000	A200	2010	0,9	19	A,8,1
0	C400		2000	0	0A	8,2
1	FC00		1000	1	01	1
2	D800		0800	2	02	2
3	DC00		0400	3	03	2,1
4	F000		0200	4	04	4
5	F400		0100	5	05	4,1
6	D000		0080	6	06	4,2
7	D400		0040	7	07	4,2,1
8	E400		0020	8	08	8
9	E000		0010	9	09	8,1
#	C000		0420	8,3	2A	B,8,2
/	BC00		3000	0,1	11	A,1

Character	1053/1816 Printer		1816 Keyboard/1442		1443 Printer	
	Lower Case (hex)	Upper Case (hex)	Hex	IBM Card Code	Hex 2 Char/ Word	BCD
-(dash)	8400		4000	11	20	B
,(comma)	8000		2420	0,8,3	1B	A,8,2,1
&	4400		8000	12	30	B,A
$	4000		4420	11,8,3	2B	B,8,2,1
@	0400		0220	8,4	0C	8,4
.(period)	0000		8420	12,8,3	3B	B,A,8,2,1
(		FE00	8120	12,8,5	1C	A,8,4
)		F600	4120	11,8,5	3C	B,A,8,4
+		DA00	80A0	12,8,6	10	A
<		DE00	8220	12,8,4	3E	B,A,8,4,2
>		4600	20A0	0,8,6	0E	8,4,2
¬		F200	4060	11,8,7	2F	B,8,4,2,1
;		D200	40A0	11,8,6	2E	B,8,4,2
*		D600	4220	11,8,4	2C	B,8,4
"		E200	0060	8,7	1F	A,8,4,2,1
¦		C600	8060	12,8,7	3F	B,A,8,4,2,1
=		C200	00A0	6,8	0B	8,2,1
_(underscore)		BE00	2120	0,8,5	1D	A,8,4,1
?		8600	2060	0,8,7	0F	8,4,2,1
:		8200	0820	8,2	1E	A,8,4,2
!		4200	4820	11,8,2	2D	B,8,4,1
%		0600	2220	0,8,4	1A	A,8,2
¢		0200	8820	12,8,2	3D	B,A,8,4,1
'(apostrophe)		E600	0120	5,8	0D	8,4,1
¤					3A	B,A,8,2
0,8,2			2820	0,8,2		
Erase Char			0004			
Erase Field			0002			
End of Field			0008			
Space	2100		0000	blank		
Carrier Return	8100				For 1443 Carriage Control Characters See Figure 1-15	
Tabulate	4100					
Line Feed		0300				
Back Space	1100					
Shift to Red	0900					
Shift to Black	0500					

28077

Figure 1-14. Character Coding

Immediate Skip to	Hex	Skip after Print to	Hex
Channel 1	01	Channel 1	31
Channel 2	02	Channel 2	32
Channel 3	03	Channel 3	33
Channel 4	04	Channel 4	34
Channel 5	05	Channel 5	35
Channel 6	06	Channel 6	36
Channel 7	07	Channel 7	37
Channel 8	08	Channel 8	38
Channel 9	09	Channel 9	39
Channel 10	0A	Channel 10	3A
Channel 11	0B	Channel 11	3B
Channel 12	0C	Channel 12	3C
Immediate Space		Space after Print	
1 Space	21	1 Space	11
2 Spaces	22	2 Spaces	12
3 Spaces	23	3 Spaces	13

28078

Figure 1-15. 1443 Printer Carriage Control Characters

Hex Address (Modifier Bits 8 - 15)	Status Word	
00	DSW, without reset	
01	DSW, with reset	
02	PISW 1	
03	PISW 2	
04	PISW 3	
05	PISW 4	
06	PISW 5	(Interrupt points,
07	PISW 6	in groups of four,
08	PISW 7	are assigned to
09	PISW 8	PISW by customer)
0A	PISW 9	
0B	PISW 10	
0C	PISW 11	
0D	PISW 12	
0E	PISW 13	
0F	PISW 14	
10	PISW 15	
11	PISW 16	
12	PISW 17	
13	PISW 18	
14	PISW 19	
15	PISW 20	
16	PISW 21	
17	PISW 22	
18	PISW 23	
19	PISW 24	
1A - 3F	38 Addresses Reserved for RPQ	

14161A

Figure 1-16. Digital Input DSW and PISW Addresses

Hex Address (Modifier Bits 8-15)				
Digital Inputs			Pulse Counters	
Adapter	Group No. (16 pts ea)		Counter No. (2/Addr)*	Adapter
First	0	40	15-14	Eighth
	1	41	13-12	
	2	42	11-10	
	3	43	9-8	
	4	44	7-6	
	5	45	5-4	
	6	46	3-2	
	7	47	1-0	
Second	0	48	15-14	Seventh
	1	49	13-12	
	2	4A	11-10	
	3	4B	9-8	
	4	4C	7-6	
	5	4D	5-4	
	6	4E	3-2	
	7	4F	1-0	
Third	0	50	15-14	Sixth
	1	51	13-12	
	2	52	11-10	
	3	53	9-8	
	4	54	7-6	
	5	55	5-4	
	6	56	3-2	
	7	57	1-0	
Fourth	0	58	15-14	Fifth
	1	59	13-12	
	2	5A	11-10	
	3	5B	9-8	
	4	5C	7-6	
	5	5D	5-4	
	6	5E	3-2	
	7	5F	1-0	
Fifth	0	60	15-14	Fourth
	1	61	13-12	
	2	62	11-10	
	3	63	9-8	
	4	64	7-6	
	5	65	5-4	
	6	66	3-2	
	7	67	1-0	
Sixth	0	68	15-14	Third
	1	69	13-12	
	2	6A	11-10	
	3	6B	9-8	
	4	6C	7-6	
	5	6D	5-4	
	6	6E	3-2	
	7	6F	1-0	
Seventh	0	70	15-14	Second
	1	71	13-12	
	2	72	11-10	
	3	73	9-8	
	4	74	7-6	
	5	75	5-4	
	6	76	3-2	
	7	77	1-0	
Eighth	0	78	15-14	First
	1	79	13-12	
	2	7A	11-10	
	3	7B	9-8	
	4	7C	7-6	
	5	7D	5-4	
	6	7E	3-2	
	7	7F	1-0	

* Sixteen-bit counters use even numbers (one counter number per address)

14162A

Figure 1-17. Digital Input or Pulse Counter Addresses

Hex Address (Modifier Bits 8-15)								
Digital Output				Analog Output				
DO Control	DO Adapter	Group No. (16 points each)		DAC Mod 2 or 4 Output	DAC Mod 1 or 3 Output	DAC No. within 1856	1856	
Addresses 00-0F not available for DO			00	1st	1st	1	1st (Model 1)	
			01	2nd				
			02	1st	1st	2		
			03	2nd				
			04	1st	1st	3		
			05	2nd				
			06	1st	1st	4		
			07	2nd				
			08	1st	1st	1	2nd (Model 2)	
			09	2nd				
			0A	1st	1st	2		
			0B	2nd				
			0C	1st	1st	3		
			0D	2nd				
			0E	1st	1st	4		
			0F	2nd				
7*	28	3	10	1st	1st	1	3rd (Model 1)	
		2	11	2nd				
		1	12	1st	1st	2		
		0	13	2nd				
	27	3	14	1st	1st	3		
		2	15	2nd				
		1	16	1st	1st	4		
		0	17	2nd				
	26	3	18	1st	1st	1	4th (Model 2)	
		2	19	2nd				
		1	1A	1st	1st	2		
		0	1B	2nd				
	25	3	1C	1st	1st	3		
		2	1D	2nd				
		1	1E	1st	1st	4		
		0	1F	2nd				
6	24	3	20	1st	1st	1	5th (Model 1)	
		2	21	2nd				
		1	22	1st	1st	2		
		0	23	2nd				
	23	3	24	1st	1st	3		
		2	25	2nd				
		1	26	1st	1st	4		
		0	27	2nd				
	22	3	28	1st	1st	1	6th (Model 2)	
		2	29	2nd				
		1	2A	1st	1st	2		
		0	2B	2nd				
	21	3	2C	1st	1st	3		
		2	2D	2nd				
		1	2E	1st	1st	4		
		0	2F	2nd				
5	20	3	30	1st	1st	1	7th (Model 1)	
		2	31	2nd				
		1	32	1st	1st	2		
		0	33	2nd				
	19	3	34	1st	1st	3		
		2	35	2nd				
		1	36	1st	1st	4		
		0	37	2nd				
	18	3	38	1st	1st	1	8th (Model 2)	
		2	39	2nd				
		1	3A	1st	1st	2		
		0	3B	2nd				
	17	3	3C	1st	1st	3		
		2	3D	2nd				
		1	3E	1st	1st	4		
		0	3F	2nd				

* Not available when the first DO Control is in 1826
** Not available when the first DO Control is in 1801

Hex Address (Modifier Bits 8-15)								
Digital Output				Analog Output				
DO Control	DO Adapter	Group No. (16 points each)		DAC Mod 2 or 4 Output	DAC Mod 1 or 3 Output	DAC No. within 1856	1856	
4	16	3	40	1st	1st	1	9th (Model 1)	
		2	41	2nd				
		1	42	1st	1st	2		
		0	43	2nd				
	15	3	44	1st	1st	3		
		2	45	2nd				
		1	46	1st	1st	4		
		0	47	2nd				
	14	3	48	1st	1st	1	10th (Model 2)	
		2	49	2nd				
		1	4A	1st	1st	2		
		0	4B	2nd				
	13	3	4C	1st	1st	3		
		2	4D	2nd				
		1	4E	1st	1st	4		
		0	4F	2nd				
3	12	3	50	1st	1st	1	11th (Model 1)	
		2	51	2nd				
		1	52	1st	1st	2		
		0	53	2nd				
	11	3	54	1st	1st	3		
		2	55	2nd				
		1	56	1st	1st	4		
		0	57	2nd				
	10	3	58	1st	1st	1	12th (Model 2)	
		2	59	2nd				
		1	5A	1st	1st	2		
		0	5B	2nd				
	9	3	5C	1st	1st	3		
		2	5D	2nd				
		1	5E	1st	1st	4		
		0	5F	2nd				
2	8	3	60	1st	1st	1	13th (Model 1)	
		2	61	2nd				
		1	62	1st	1st	2		
		0	63	2nd				
	7	3	64	1st	1st	3		
		2	65	2nd				
		1	66	1st	1st	4		
		0	67	2nd				
	6	3	68	1st	1st	1	14th (Model 2)	
		2	69	2nd				
		1	6A	1st	1st	2		
		0	6B	2nd				
	5	3	6C	1st	1st	3		
		2	6D	2nd				
		1	6E	1st	1st	4		
		0	6F	2nd				
1	4**	3	70	1st	1st	1	15th (Model 1)	
		2	71	2nd				
		1	72	1st	1st	2		
		0	73	2nd				
	3**	3	74	1st	1st	3		
		2	75	2nd				
		1	76	1st	1st	4		
		0	77	2nd				
	2	3	78	1st	1st	1	16th (Model 2)	
		2	79	2nd				
		1	7A	1st	1st	2		
		0	7B	2nd				
	1	3	7C	1st	1st	3		
		2	7D	2nd				
		1	7E	1st	1st	4		
		0	7F	2nd				

Addresses 80-FF reserved for RPQ

14163 A

Figure 1-18. Digital or Analog Output Addresses

Numbering Within 1851		1851s With Multiplexer/S ← 1851s With Multiplexer/R →															
Block Switch Group	Point Number	Mpx Group 0				Mpx Group 1				Mpx Group 2				Mpx Group 3			
		1st 1851	2nd 1851	3rd 1851	4th 1851	5th 1851	6th 1851	7th 1851	8th 1851	9th 1851	10th 1851	11th 1851	12th 1851	13th 1851	14th 1851	15th 1851	16th 1851
	00	000	040	080	0C0	100	140	180	1C0	200	240	280	2C0	300	340	380	3C0
	01	001	041	081	0C1	101	141	181	1C1	201	241	281	2C1	301	341	381	3C1
	02	002	042	082	0C2	102	142	182	1C2	202	242	282	2C2	302	342	382	3C2
	03	003	043	083	0C3	103	143	183	1C3	203	243	283	2C3	303	343	383	3C3
	04	004	044	084	0C4	104	144	184	1C4	204	244	284	2C4	304	344	384	3C4
	05	005	045	085	0C5	105	145	185	1C5	205	245	285	2C5	305	345	385	3C5
	06	006	046	086	0C6	106	146	186	1C6	206	246	286	2C6	306	346	386	3C6
0	07	007	047	087	0C7	107	147	187	1C7	207	247	287	2C7	307	347	387	3C7
	08	008	048	088	0C8	108	148	188	1C8	208	248	288	2C8	308	348	388	3C8
	09	009	049	089	0C9	109	149	189	1C9	209	249	289	2C9	309	349	389	3C9
	10	00A	04A	08A	0CA	10A	14A	18A	1CA	20A	24A	28A	2CA	30A	34A	38A	3CA
	11	00B	04B	08B	0CB	10B	14B	18B	1CB	20B	24B	28B	2CB	30B	34B	38B	3CB
	12	00C	04C	08C	0CC	10C	14C	18C	1CC	20C	24C	28C	2CC	30C	34C	38C	3CC
	13	00D	04D	08D	0CD	10D	14D	18D	1CD	20D	24D	28D	2CD	30D	34D	38D	3CD
	14	00E	04E	08E	0CE	10E	14E	18E	1CE	20E	24E	28E	2CE	30E	34E	38E	3CE
	15	00F	04F	08F	0CF	10F	14F	18F	1CF	20F	24F	28F	2CF	30F	34F	38F	3CF
	16	010	050	090	0D0	110	150	190	1D0	210	250	290	2D0	310	350	390	3D0
	17	011	051	091	0D1	111	151	191	1D1	211	251	291	2D1	311	351	391	3D1
	18	012	052	092	0D2	112	152	192	1D2	212	252	292	2D2	312	352	392	3D2
	19	013	053	093	0D3	113	153	193	1D3	213	253	293	2D3	313	353	393	3D3
	20	014	054	094	0D4	114	154	194	1D4	214	254	294	2D4	314	354	394	3D4
	21	015	055	095	0D5	115	155	195	1D5	215	255	295	2D5	315	355	395	3D5
	22	016	056	096	0D6	116	156	196	1D6	216	256	296	2D6	316	356	396	3D6
	23	017	057	097	0D7	117	157	197	1D7	217	257	297	2D7	317	357	397	3D7
1	24	018	058	098	0D8	118	158	198	1D8	218	258	298	2D8	318	358	398	3D8
	25	019	059	099	0D9	119	159	199	1D9	219	259	299	2D9	319	359	399	3D9
	26	01A	05A	09A	0DA	11A	15A	19A	1DA	21A	25A	29A	2DA	31A	35A	39A	3DA
	27	01B	05B	09B	0DB	11B	15B	19B	1DB	21B	25B	29B	2DB	31B	35B	39B	3DB
	28	01C	05C	09C	0DC	11C	15C	19C	1DC	21C	25C	29C	2DC	31C	35C	39C	3DC
	29	01D	05D	09D	0DD	11D	15D	19D	1DD	21D	25D	29D	2DD	31D	35D	39D	3DD
	30	01E	05E	09E	0DE	11E	15E	19E	1DE	21E	25E	29E	2DE	31E	35E	39E	3DE
	31	01F	05F	09F	0DF	11F	15F	19F	1DF	21F	25F	29F	2DF	31F	35F	39F	3DF
	32	020	060	0A0	0E0	120	160	1A0	1E0	220	260	2A0	2E0	320	360	3A0	3E0
	33	021	061	0A1	0E1	121	161	1A1	1E1	221	261	2A1	2E1	321	361	3A1	3E1
	34	022	062	0A2	0E2	122	162	1A2	1E2	222	262	2A2	2E2	322	362	3A2	3E2
	35	023	063	0A3	0E3	123	163	1A3	1E3	223	263	2A3	2E3	323	363	3A3	3E3
	36	024	064	0A4	0E4	124	164	1A4	1E4	224	264	2A4	2E4	324	364	3A4	3E4
	37	025	065	0A5	0E5	125	165	1A5	1E5	225	265	2A5	2E5	325	365	3A5	3E5
	38	026	066	0A6	0E6	126	166	1A6	1E6	226	266	2A6	2E6	326	366	3A6	3E6
	39	027	067	0A7	0E7	127	167	1A7	1E7	227	267	2A7	2E7	327	367	3A7	3E7
2	40	028	068	0A8	0E8	128	168	1A8	1E8	228	268	2A8	2E8	328	368	3A8	3E8
	41	029	069	0A9	0E9	129	169	1A9	1E9	229	269	2A9	2E9	329	369	3A9	3E9
	42	02A	06A	0AA	0EA	12A	16A	1AA	1EA	22A	26A	2AA	2EA	32A	36A	3AA	3EA
	43	02B	06B	0AB	0EB	12B	16B	1AB	1EB	22B	26B	2AB	2EB	32B	36B	3AB	3EB
	44	02C	06C	0AC	0EC	12C	16C	1AC	1EC	22C	26C	2AC	2EC	32C	36C	3AC	3EC
	45	02D	06D	0AD	0ED	12D	16D	1AD	1ED	22D	26D	2AD	2ED	32D	36D	3AD	3ED
	46	02E	06E	0AE	0EE	12E	16E	1AE	1EE	22E	26E	2AE	2EE	32E	36E	3AE	3EE
	47	02F	06F	0AF	0EF	12F	16F	1AF	1EF	22F	26F	2AF	2EF	32F	36F	3AF	3EF
	48	030	070	0B0	0F0	130	170	1B0	1F0	230	270	2B0	2F0	330	370	3B0	3F0
	49	031	071	0B1	0F1	131	171	1B1	1F1	231	271	2B1	2F1	331	371	3B1	3F1
	50	032	072	0B2	0F2	132	172	1B2	1F2	232	272	2B2	2F2	332	372	3B2	3F2
	51	033	073	0B3	0F3	133	173	1B3	1F3	233	273	2B3	2F3	333	373	3B3	3F3
	52	034	074	0B4	0F4	134	174	1B4	1F4	234	274	2B4	2F4	334	374	3B4	3F4
	53	035	075	0B5	0F5	135	175	1B5	1F5	235	275	2B5	2F5	335	375	3B5	3F5
	54	036	076	0B6	0F6	136	176	1B6	1F6	236	276	2B6	2F6	336	376	3B6	3F6
	55	037	077	0B7	0F7	137	177	1B7	1F7	237	277	2B7	2F7	337	377	3B7	3F7
3	56	038	078	0B8	0F8	138	178	1B8	1F8	238	278	2B8	2F8	338	378	3B8	3F8
	57	039	079	0B9	0F9	139	179	1B9	1F9	239	279	2B9	2F9	339	379	3B9	3F9
	58	03A	07A	0BA	0FA	13A	17A	1BA	1FA	23A	27A	2BA	2FA	33A	37A	3BA	3FA
	59	03B	07B	0BB	0FB	13B	17B	1BB	1FB	23B	27B	2BB	2FB	33B	37B	3BB	3FB
	60	03C	07C	0BC	0FC	13C	17C	1BC	1FC	23C	27C	2BC	2FC	33C	37C	3BC	3FC
	61	03D	07D	0BD	0FD	13D	17D	1BD	1FD	23D	27D	2BD	2FD	33D	37D	3BD	3FD
	62	03E	07E	0BE	0FE	13E	17E	1BE	1FE	23E	27E	2BE	2FE	33E	37E	3BE	3FE
	63	03F	07F	0BF	0FF	13F	17F	1BF	1FF	23F	27F	2BF	2FF	33F	37F	3BF	3FF

14165 A

Figure 1-19. Multiplexer Addresses (Hexadecimal)

Error	Internal ILSW Bit	Check Stop ON			Check Stop OFF	
		Internal Interrupt	Error Sent to I/O via OUT Bus	Stop P-C Clock	Internal Interrupt	Error Sent to I/O via OUT Bus
Invalid Operation	0			X	X*	
B-Register Parity	1		X	X	X*	X
Stor Prot Violation	2		X	X	X*	X
CAR Check	3	X**	X		X**	X

* Except XIO data cycle, cycle-steal, or IPL mode

** E2 cycle CAR check only

14203A

Figure 1-20. Detection of Internal Errors

Cycle	Operation	Set Error Indicator		Ignore Data
		Control	Data	
Control	Set Area, Fctn, Modifier	X*		X
Write Data	Load AMAR	X		X
Read Data	Store ADC		X	
Init Rd Data	Load and Check CAR-A			X
Init Wr Data	Load and Check CAR-B			X
Ch A Cyc Steal	Load WCR, Load AMAR Load CAR-A, Check CAR-A	X		X
Ch B Cyc Steal	Load CAR-B, Check CAR-B	X		X
Ch B Cyc Steal	Load AMAR, Limit Compare		X	
Ch A Cyc Steal	Store ADC		X	

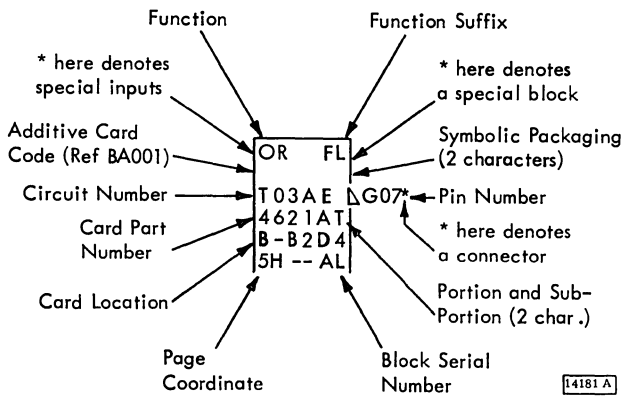
* Set by transmission parity error only (P-C parity OK)

14098B

Figure 1-21. AI Parity Error and CAR Check Detection

1.1 LOGIC DIAGRAMS

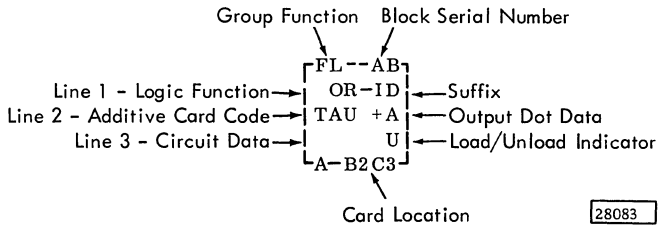
1.1.1 ALD Logic Block Symbology



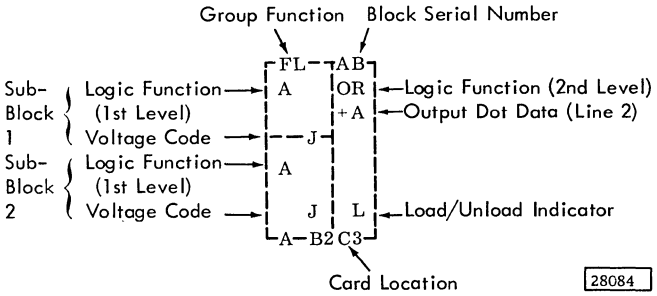
1.1.2 FEALD Logic Block Symbology

For detailed information concerning FEALD's see General CEM Index 1.

Basic Logic Block Format



Combinational Logic Block Format



1.1.3 Machine Frame and Gate Designations

Note: Board locations are given in paragraph 6.3.

Frames

The following frame numbers (Figure 1-22) are used in the ALD's to show the machine type in which the logic is contained. A different frame numbering system is used in the MLR and FESRR to show the frame location of installed features. (See paragraph 6.2.)

- 03 IBM 1803 Additional Core Storage
- 10 IBM 1810 Disk Storage
- 26 IBM 1826 Data Adapter Unit
- 28 IBM 1828 Enclosure
- 51 IBM 1851 Multiplexer Terminal
- 56 IBM 1856 Analog Output Terminal
- 60 IBM 1801/1802 Processor-Controller or identifies component that may be used in more than one frame
- 63 Core storage and I/O monitor unit

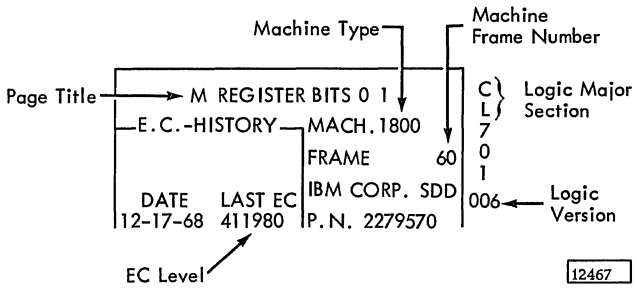


Figure 1-22. Logic Page Identification

Gates

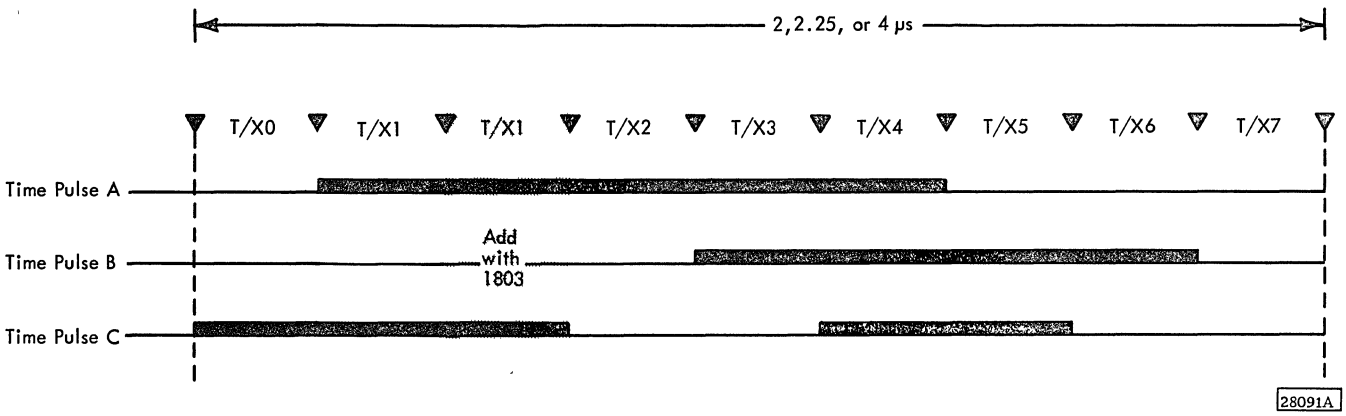
A–, B–, C-, D– SLT gates (A is also used for 1851 sub-enclosure)
F–, G– Integrator housings (1801/1802)
H– Channel terminator and mixer panel (1801/1802)
M– Mixer panel (1856)
N– Programmer's console (1801/1802)
Q – I/O Monitor interface panel (1801/1802)
R– Customer termination panel (1801/1826)
T– Signal tailgate
X–, Y–, Z– Identifies component that may be used in more than one gate (paragraph 6.3)

1.1.4 Logic Page Identification (Figure 1-22)

Major Section

The following listed page prefixes (major sections) are used in the system diagram manuals and maintenance diagram manuals.

Major Section	Logic
A–	Indexes
B–	Reference and cable
CA through CB	Console and indicators, op monitor
CC through CF	CPU controls
CH through CL	CPU registers and controls
CP	Channel control
CQ	Cycle steal, CAR, CAB, auxiliary storage, CE interrupt
CR	Timers, function register, area 0, console interrupt
CS	Interrupt levels
CT through CU	I/O interface
EA through EG	1816 Printer Keyboard and 1053 Printer
EJ through EL	1627 Plotter and 1443 Printer
EN	1442-6, 7 Card Read Punch
ES	1054 Paper Tape Reader and 1055 Paper Tape Punch
FA	1810-A1, A2, A3 Disk Storage
FC	1810-B1, B2, B3 Disk Storage
FS	Selector Channel
FV through FZ	System/360 adapter
GA through GW	Tape control unit
LA through LC	2790 adapter
MA through MM	Communications adapter
QC	1851 Multiplexer Terminal
QD	AI basic and ADC
PA	DI/DAO basic
PB	Digital and analog output basic
PC	DAO data channel adapter
PD	Digital input basic
PE	DI data channel adapter
RA	Digital input adapter



● Figure 1-23. Time Pulses, A, B, and C (CP111)

Major Section	Logic
RB	Pulse counter adapter
RC	Process interrupt adapter
SA and SD	Core storage
TA	1856 analog output terminal
TL	Digital output adapter
WA	I/O monitor
WX	1803 Core Storage Unit
WZ	Core storage interface
XA	Single disk storage
YA	1801/1802 power control
YB	1826 power control
YC	1810 power control
YF	DC power supplies
YS	1803 power control

With the exception of second-order products, such as core storage and single disk storage, only one set of logics is provided for multiple features within a machine type. For example, if the 1826 and the 1801 each contain two digital input adapters, two sets of RA logics will be sent with the system —— one for the 1826 and one for the 1801. Likewise, if a feature is not included in the machine type, no set of logics will be provided for that feature.

Version

The logic version number appears in the lower corner of the logic page. Logic version numbers 000–049 are reserved for basic system and basic system features. Non RPQ logic versions and associated applications are:

000 – Basic system
004 – Installed once with any of the following features: selector channel, communications adapter, 1800/2790 adapter, expanded core storage, expanded data channels
005 – Installed with core storage expansion beyond 32k (1803 attached)
006 – Installed with data channel expander (more than nine data channels)

The highest numbered version of logic always takes precedence according to the features installed on the system.

Note: Version numbers above 050 apply to RPQ's. Version numbers below 050 are used here to identify installed features. When RPQ's are incorporated in a system, ALD's are printed on green paper with a version number. Version priority is not related to the version number but is called out in the RPQ installation instructions.

RPQ Logic Pages

RPQ logic pages are printed on green paper. When an RPQ modifies the information on an existing logic page, the green RPQ logic page will be inserted with the existing page.

1.1.5 System Paperwork Binder

A system paperwork binder is included as part of the maintenance package provided with the 1800 system. The binder contains miscellaneous records and copies of listings pertaining to the individual system. Among these documents are:

1. Quality Assurance Shipping Check List
2. Final Test Shipping Check List (cables)
3. Machine History (hard card)
4. Machine Level Control (MLC) for core storage
5. Cable Order Form
6. Customer Assignment Form (CAF)
7. Summary of Order for System
8. Machine Location Report (MLR)
9. Additional CAF and MLR information for installed RPQ's
10. Field Engineering Systems Reference Report (FESRR)
11. Manufacturing Assembly Report (MAR–2)

The FESRR is a machine listing of all installed features, except RPQ features, showing board and terminal locations, IOCC addresses, and interrupt and data channel assignments. The MAR–2 forms are generated at the factory to identify all unique customer wiring. Both the FESRR and the MAR–2 must be updated by the customer engineer each time a wiring assignment is changed in the field. (See paragraph 1.2.)

1.2 MANUALLY CONTROLLED WIRING CHANGES

Manually controlled (special purpose) wiring is used in certain areas of the 1800 system to provide the flexibility required for customer assignments, options, and additive features. Manually controlled wiring relates to the unique wire connections that adapt the system to the specific needs of the customer or features. That wiring which is assignable by the customer is also referred to as "personality wiring."

Manual wiring connections, both special purpose and personality, are made with violet wire on the probe side of SLT boards or special mixer panels, using pin-to-pin wrapped terminations.

After the system is shipped, all changes and additions to manual wiring are controlled by the customer engineer.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Sign	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	Over-load

1st Hex Character

	Voltage
0	0.0000
1	0.6250
2	1.2500
3	1.8750
4	2.5000
5	3.1250
6	3.7500
7	4.3750
8	(1)
9	(1)
A	(1)
B	(1)
C	(1)
D	(1)
E	(1)
F	(1)

2nd Hex Character

	Voltage
0	0.0000
1	0.0391
2	0.0781
3	0.1172
4	0.1563
5	0.1954
6	0.2344
7	0.2735
8	0.3125
9	0.3516
A	0.3906
B	0.4297
C	0.4688
D	0.5079
E	0.5469
F	0.5860

3rd Hex Character

	Voltage
0	0.0000
1	0.0024
2	0.0049
3	0.0073
4	0.0098
5	0.0122
6	0.0147
7	0.0171
8	0.0195
9	0.0219
A	0.0244
B	0.0268
C	0.0293
D	0.0317
E	0.0342
F	0.0366

4th Hex Character

	Voltage
0	0.0000
1	(2)
2	0.0003
3	(2)
4	0.0006
5	(2)
6	0.0009
7	(2)
8	0.0012
9	(2)
A	0.0015
B	(2)
C	0.0018
D	(2)
E	0.0021
F	(2)

Obtain voltage value for each hex character. Sum of four voltage values equals ADC voltage reading. For low-level inputs, reading must be corrected to compensate for differential amplifier gain.

(1) Negative reading. Obtain two's complement (subtract hex reading from /FFFF and add 1) of ADC value and obtain equivalent positive value from chart.

(2) Overload bit is on. ADC value is meaningless.

28112

Figure 1-24. ADC Register Voltage Values

It is the CE's responsibility to update the system records after each change and to edit the diagnostic program decks as necessary.

For additional information on wiring changes, see 1800 Service Aid number 29.

1.2.1 Authorization for Wiring Changes

Customer assigned wiring can be changed by the CE at the customer's request when authorized by the FE branch manager. Other types of manually controlled wiring may be changed when authorized by an MES, RPQ, or engineering change. No altering of customer assignments will result from an engineering change. If an engineering change affects a net containing customer-assigned wiring, the field instructions will specify the action required to maintain the present assignments.

MES and RPQ Orders

These orders usually specify installation or removal of additive or special features and may necessitate rework of existing manual wiring, including customer assigned wiring.

The order will include a new Machine Location Report (MLR) and instructions for accomplishing manual wiring other than customer-assigned wiring. If additional installation information is required, an 1800 MES Requirements form will be supplied. (See 1800 Service Aid number 18.)

If the rework affects customer-assigned wiring, the CE must obtain the new assignments from the customer (see "Customer Request").

Types of feature wiring controlled by MES order include:

Pulse counter 8-bit or 16-bit option
DI (voltage) high-speed option
AO optional features
IPL wiring for first 1442 (or 1054 if no 1442)
Additive features (interrupts, data channels, I/O adapters, process I/O groups, etc.)
Communications adapter code (EBCDIC or USASCII) and data set clocking

Customer Request

Changes to customer-assigned wiring can be made at the customer's request without the need for an MES order. This provision results in minimum turnaround time for the change. The customer must submit a written request to the FE branch manager, who authorizes the CE to make the change. This request must be filed with the system records.

The following manual wiring assignments are controlled by customer request:

Data channel assignment
Interval timer bases
Interrupt level assignment
ILSW bit assignment
PISW bit assignment
System/360 adapter address and select-bypass
Communications adapter wiring to match customer's data sets

Assignments of interrupt level, ILSW bit, and PISW bit are indicated on the Customer Assignment Form provided with the system. Interval timer bases and data channel assignments are indicated in the MLR by 9xxx "specify" codes. The 9xxx codes associated with interval timers and data channel assignments are unique because they are not under machine level control and, therefore, do not require an MES order for authorization to change.

1.2.2 Data Channel Assignment

Initial assignment of an I/O device to a data channel is designated by the 9xxx specify code which is recorded on the MLR. Each device that can operate on a data channel has fifteen unique specify codes corresponding to the fifteen data channels.

Reassignment of a device to a data channel must be authorized by MES, RPQ, or customer request with FE branch manager approval.

Wiring Procedure

1. Determine present wiring assignments and make a wire delete list using CU992 and CU993, if marked, or the FESRR and MAR–2 listing. Compare this list against actual system wiring.
2. Make a list of the new cycle-steal assignments, by device, and compare assignments with the order given on BC101. If the new assignments accompany a feature installation, verify with the customer that the 9xxx specify codes listed in the new MLR are correct.
3. Using CT990 and the list of new assignments as a reference, assign the adapters to a CS request line (A–Q) on CU992 by writing the adapter name above the line to which it is assigned. Use existing assignments as much as possible. Erase any existing marks and write new assignments in pencil.
4. On CU992, draw in pencil the new level assignments. For example, if the 1443 is on line F and is to be assigned to level 6, draw a line from D–A1N7B05 to D–A1M4B05.
5. Hand mark CU993 to exactly agree with CU992. Pin numbers will vary, but the lines, mixing, and priority assignments must agree. When properly maintained, CU992 and CU993 reflect the data channel wiring of the system and can be used to develop a delete list for future changes in customer assignments.
6. Prepare new edit cards (or paper tape) for diagnostic monitor and diagnostic function tests as required. Refer to paragraph 1.2.7.

7. Perform wiring as drawn on CU992 and CU993, using violet wire (P/N 811696) only.
8. Run diagnostic tests with the new edit cards (or paper tape) to verify proper assignment and editing. Update disk maintenance library (DIMAL) if applicable.
9. Notify the customer that wiring has been completed and have the customer run test case with the new assignments.
10. Update FESRR and the applicable MAR–2 pages.
11. Use service code 31 to cover elapsed time.

1.2.3 Timer Interval Reassignment

Initial assignment of interval timer bases is designated by the 9xxx specify code which is recorded on the MLR. Reassignment of a time base can be authorized by MES or by customer request via the FE branch manager.

Wiring Procedure

1. Refer to system diagram BC150 and convert the 9xxx interval timer feature code to the corresponding time base, using Table E.
2. Develop delete list, using the MAR–2 wire list as a reference.
3. Develop add list by referring to Table A on BC150. The MAR–2 wire list, when updated, can serve as the add/delete list.
4. Prepare new edit cards (or paper tape) for diagnostic monitor and diagnostic function tests as required. Refer to paragraph 1.2.7.
5. Perform add/delete wiring. (Use only violet wire, P/N 811696.)
6. Run diagnostic tests with the new edit cards (or paper tape) to verify proper assignment and editing. Update disk maintenance library (DIMAL) if applicable.
7. Notify customer that wiring has been completed and have customer run test case with the new assignments.
8. Update FESRR and the MAR–2 page.
9. Use service code 31 to cover elapsed time.

1.2.4 Interrupt Assignments

Initial assignment of interrupt levels, ILSW bits, and PISW bits is indicated on the Customer Assignment Form.

After the system is shipped, all changes and additions to interrupt assignments (including those made in conjunction with a sales MES or RPQ) must be authorized by customer request approved by the FE Branch Manager.

Wiring Procedure –– System Interrupts

1. List the new interrupt levels and ILSW bit assignments per device.
2. Select the appropriate diagrams from the following table:

Device	Logic Page Reference	
Console and Timers	BC 150	CU 991
1053/1816	EA 001	EA 991
1054/1055	ES 001	ES 992
1442	EN001	EN991
1443	EJ 005	EJ 991
1627	EJ 001	EJ 991
1810	FA 001	FA 991
S/360 Adapter	FV 001	FZ 991
TCU (1802 only)	GA111	GB991
Analog Input	QD041	QD991
Dig & Anlg Output	PB 000	PA 991
Digital Input	PD 000	PA 991
Selector Channel	FS011	FS013
Communications Adapter	MA008	MB997

14191 A

3. Refer to the MAR–2 sheets and the wiring tables on the referenced diagrams and develop add/delete lists for the following assignments in each adapter affected:

   Interrupt level assignment
   ILSW bit assignment
   Sense ILSW decode
   Poll interrupt level

   The MAR–2 wire lists, when updated, can serve as the add/delete list.
4. Prepare new edit cards (or paper tape) for diagnostic monitor and diagnostic function tests as required. Refer to paragraph 1.2.7.
5. Perform add/delete wiring. (Use only violet wire, P/N 811696.)
6. Run diagnostic tests with the new edit cards (or paper tape) to verify proper assignment and editing. Update disk maintenance library (DIMAL) if applicable.
7. Notify customer that wiring has been completed and have customer run test case with the new assignments.
8. Update FESRR, Customer Assignment Form, and the applicable MAR–2 sheets.
9. Use service code 31 to cover elapsed time.

Wiring Procedure –– Process Interrupts

1. List the new interrupt levels, ILSW bit assignments, and PISW bit assignments for each board group.

   Note: Three 16-bit PI (contact or voltage) groups may be installed in the adapter. Process interrupts in each PI group are divided into four "board groups" of four bits. These board groups are numbered 1A, 1B, 1C, 1D, 2A . . . through 3D. Each board group can be

assigned to a unique interrupt level; however, the selected level must be within the range specified for the adapter —— either 0 through 11 or 12 through 23.

2. Refer to Note 1 on system diagram RC841 and determine the appropriate cable plugging for the desired interrupt range of the adapter.
3. Refer to the MAR—2 sheets and the wiring tables on the system diagrams given in the following list. Develop add/delete lists for the wiring assignments in each board group. Observe all notes on these pages. The MAR—2 wire lists, when updated, can serve as the add/delete lists.

Board Group	Logic Page Reference	
Interrupt Level	RC001	RC991*
Sense ILSW/PISW	RC002	RC971*
ILSW Bits	RC004	RC981*

* On current production, MAR-2 sheets are located in the System Paperwork Binder.

14192A

4. Prepare new edit cards (or paper tape) for diagnostic function tests as required. Refer to paragraph 1.2.7.
5. Perform add/delete wiring. (Use only violet wire, P/N 811696.)
6. Run diagnostic tests with the new edit cards (or paper tape) to verify proper assignment and editing. Update disk maintenance library (DIMAL) if applicable.
7. Notify customer that wiring has been completed and have customer run test case with the new assignments.
8. Update FESRR, Customer Assignment Form and MAR—2 sheets.
9. Use service code 31 to cover elapsed time.

1.2.5 System/360 Adapter Address Reassignment

The System/360 channel address of the System/360 adapter can be reassigned at the customer's request or as the result of an MES or RPQ order. Select-bypass jumpering for the adapter can also be reassigned by MES, RPQ, or customer request.

Wiring Procedure

1. Refer to the following system diagrams and determine the necessary jumper changes by comparing new assignments with present jumpering of the address-select/generate card and the select-bypass card.

System/360 Adapter	Logic Page Reference	
Address Select & Generate	FV005	FY101
Select In/Out Bypass	FV005	FV251

14193

2. Change placement of program caps on the cards to conform to new assignments.
3. Prepare new edit cards for System/360 diagnostics as required.
4. Run diagnostic tests (System/360) with the new edit cards to verify proper assignment and editing.
5. Notify customer that wiring has been completed and have customer run test case with the new assignments.
6. Indicate new assignments on the affected system diagrams.
7. Use service code 31 to cover elapsed time.

Diagnostic	PID	Features
Monitor	0801	All
Disk Maintenance Library Initial Loader	08B7	1810A
Meter Exerciser	08B6	1442
		1443
		1810
		2400
1053/1816 Function Test	0806	1053/1816
2400 Function Test	0807	2400
2400 Timing Test	08B9	2400
2400 Interchange and Skew Test	080B	2400
2400 Cyclic Redundancy Check	08BD	2400
1054/1055 Function Test	0804	1054
		1055
1627 Function Test	0805	1627
2315 Initialization	0808	1810A
1810 Function Test	0809	1810A
1443 Function Test	080A	1443
1442 Function Test	080F	1442
AI Data Channel (Random) Function Test	0821	AI, Interval Timers
AI Data Channel (Sequential) Function Test	0822	AI, Interval Timers
AI Direct Program Control Function Test	0823	AI, Interval Timers
DI Data Channel Function Test	0824	DI
DI Direct Program Control Function Test	0825	DI
		PI
AO Function Test	0826	AO
DO Function Test	0827	DO
System/360 Adapter - Section 1	0828	S/360 Adapter
System/360 Adapter - Section 2	0829	S/360 Adapter
Selector Channel Function Test	0810	Selector Channel
2841 Function Test	0811	Selector Channel
2311 Function Test	0812	Selector Channel
2841 Two-Channel Switch Function Test	0813	Selector Channel
2311 CE Pack Initialization	0814	Selector Channel
2841/2311 MPX On-Line Test	0892	Selector Channel
Comm Adapt Transmit-Receive	080D	Comm Adapt
Comm Adapt Wrap Around	080E	Comm Adapt
Comm Adapt MPX On-Line Test	0891	Comm Adapt
2790 Adapter	082B	2790
	082C	2790
	082D	2790

14194A

1.2.6 Communications Adapter and Line Adapter

Wiring assignments on the communications adapter (CA) and line adapter (LA) boards are determined by the data sets to

be used, the line type, and the desires of the customer. Reassignment of manual wiring can be authorized by MES or by customer request via the FE branch manager.

The CA and LA require personality wiring in addition to the usual data channel and interrupt assignments. See MA20151 for the purposes of all wired logic lines.

Wiring Procedure

1. Refer to system diagrams MA008, MK008, MB997, MB998, and MB999. Using the wiring tables on these diagrams, together with the MAR–2 list, develop add/delete list. The MAR–2 list, when updated, can serve as the add/delete list.
2. Prepare new edit cards (or paper tape) for diagnostic monitor and diagnostic function tests as required. Refer to paragraph 1.2.7.
3. Perform add/delete wiring. (Use only violet wire, P/N 811696.)
4. Run diagnostic tests with the new edit cards (or paper tape) to verify proper assignment and editing. Update disk maintenance library (DIMAL) if applicable.
5. Notify customer that wiring has been completed and have customer run test case with the new assignments.
6. Update FESRR and the MAR–2 sheet.
7. Use service code 31 to cover elapsed time.

1.2.7 Editing Diagnostic Programs

The editing procedure for each diagnostic program is outlined in the maintenance diagnostic programs manual. The first page of volume 1 of the maintenance diagnostic programs lists the volume in which the description for a program is located. Paragraph 6.1 of each description details the edit procedure.

The above table lists diagnostics and indicates which feature wiring will affect them.

Section 2. Diagnostic Techniques

1.3 ON–LINE SERVICING LIMITATIONS

Several maintenance features of the 1800 system are designed specifically to permit diagnosis and servicing while the customer program is operating from main storage. However, the customer must be notified prior to performing any on-line maintenance that might affect the process control operation, either directly (via an output device) or indirectly (via the operating program).

Limitations and precautions that should be observed during the on-line maintenance activity are defined in the following paragraphs.

Note: Operating limitations for the MPX On-Line Diagnostics are described in 1800 Service Aid 138 and in the 1800 Multiprogramming Executive Operating System Programmers Guide, Order No. GC26–3720.

1.3.1 Use of Auxiliary Storage

If the auxiliary storage program is destroyed, it is possible for the system to become locked in auxiliary storage. Therefore, the customer should be notified when the CE intends to use auxiliary storage, so that restart procedures can be planned in advance.

The customer option to place two devices on the same data channel imposes limitations on shared-time servicing. When one of these devices is to be serviced on-line from auxiliary storage, it will be necessary to take both devices from the customer and place the second device in a "not ready" condition by some manual means, such as removing power to the device.

If the 1442 shares a data channel with another device, both devices will have to be taken if it is necessary to load an auxiliary program.

See 2.6 for a more detailed explanation of auxiliary storage.

Care should be taken to ensure that any device to be serviced on line from auxiliary storage will not be needed by the operating system, causing the customer's program to hang up. The procedures that must be followed to allow the TSX operating system to select alternate devices are explained in "IBM 1800 TSX System Maintenance" of *IBM 1800 Time-Sharing Executive Operating Procedures,* Order No. GC26–3754.

1.3.2 Power Removal and Component Plugging

Power cannot be turned on or off at any 1800 system unit without the possibility of system interference.

On-line servicing that requires removal of power from any system unit, or removal and replacement of cables or pluggable components within these units, is not recommended if the customer has no reset-and-restart procedure. Even with the P–C stopped and placed in SI, SSC, load, or display mode (to prevent cycle stealing), there is still a possibility of upsetting the status of latches and flip-flops with transients created by interrupting electrical circuits.

To safely remove power from any 1800 system unit, without System/360 adapter (See 1.3.4), proceed as follows:

1. Power down the system.
2. Observe proper channel termination. (See 1.3.3)
3. Remove cables or power from system unit to be taken off line.
4. Restore power to system.

To return a system unit to on-line operation, follow the same procedure except that the unit is added rather than removed.

Removal of power places the unit in a "not ready" condition at the adapter interface.

CAUTION
Because of the danger of shorting between adjacent cards, it is not advisable to remove or replace SLT cards with power on. To prevent damage to components, the following types of cards must never be removed with power on:

Drivers and amplifiers
Core storage cards
Power supply cards
Multiplexer cards

1.3.3 Channel Termination

If an 1826, 1856–1, or 1810 containing channel terminator cards is taken off line, the terminator cards must be removed from the unit and installed in the outbound cable sockets of the preceding unit before starting the P–C program. Figure 1–25 lists the channel cables and the logic pages that indicate where cables and terminators can be positioned in each unit. If System/360 adapter is installed in the 1826 being taken off-line, see next paragraph.

1.3.4 System/360 Adapter

The 1800 system may be powered up or down while the System/360 is running if the proper procedure is followed. To power up:

1. Place the on system/off system/bypass-gated (bypass) switch, which is located on the A–gate of the 1826 housing the System/360 channel adapter boards, to the bypass-gated position.
2. Power up the system and the 1826. Verify that the off-system lamp, which is adjacent to the bypass switch, is on.
3. Move the switch to the on-system position. When the off-system lamp turns off, the channel adapter is on line.

To power down:

1. Place the bypass switch in the off-system position and wait for the off-system lamp to turn on.
2. With the off-system lamp on, place the bypass switch in the bypass-gated position and power down.

If frequent powering up and down is anticipated while servicing the 1800 system, or if the 1826 containing the System/360 adapter is to be taken off line, the 1800 system should be disconnected from the System/360 channel as follows:

1. Stop System/360.
2. a. If the System/360 adapter (in the 1826) terminates the System/360 channel, remove the terminators at the outbound serpent connectors on the 1826 signal tailgate and place them in the outbound cable positions of the preceding System/360 device.
   b. If the System/360 adapter does not terminate the System/360 channel, remove the inbound and outbound cables at the serpent connectors on the 1826 signal tailgate and butt together.
3. Restart System/360.

Note that this procedure is not necessary if the System/360 is the one being powered up/down.

1.4 MARGINAL CHECKING

Marginal checking of 1800 system circuits is not recommended as a routine PM procedure but may be an effective method of isolating certain types of intermittent failures.

Channel	Data	Cable	No. of Lines	Routing
I/O	Out Bus & Control	1A	20	CT990
		2A	20	CT990
		3A	20	CT990
	In Bus & Control	1B	20	CT990
		2B	20	CT990
		3B	20	CT990
	Cyc Steal & Control	1C	20	CT990
		2C	20	CT990
		3C	20	CT990
		3D	20	CT990
DAO	Address & Control	DO-1	12	TL091
		AO-1	12	TA091
	Data Bits	DO-2	16	TL092
		AO-2	16	TA092
DI/PC	Address & Control	U	10	PD091
	Data Bits	V	16	PD095
PI	Out Bus Bits	W	20	RC091
	Proc Intr Bits	X	20	RC092
	Intr Level 0-11	Y	12	RC093
	Intr Level 12-23	Z	12	RC094
S/360	Tags & Controls	Tag	14	——
	Bus In & Bus Out	Bus	18	——
See FESRR for adapter locations				

14202B

● Figure 1-25. Channel Cables

It must be realized that the intermittent circuit may be failing because it is sensitive to some parameter other than voltage (e.g., frequency, temperature, humidity). In this case, application of marginal voltage may cause failure of circuits other than the intermittent circuit being sought.

Marginal Check Procedure

Marginal checking of the 1800 system may be accomplished by varying the +3, −3, and +6 voltages ±4 percent in any combination while running the program which is causing failures. The following combinations have been found most effective for trouble analysis.

	Nominal Voltage	Marginal Voltage
Case 1	+3.00 +6.00 -3.00	+3.12 +6.24 -3.12
Case 2	+3.00 +6.00 -3.00	+3.12 +6.24 -2.88
Case 3	+3.00 +6.00 -3.00	+2.88 +5.76 -3.12
Case 4	+3.00 +6.00 -3.00	+2.88 +5.76 -2.88
Case 5	+3.00 +6.00 -3.00	+3.12 +5.76 -3.00
Case 6	+3.00 +6.00 -3.00	+2.88 +6.24 -3.00

16266-1

The charts in Figures 5–3 through 5-8 can be used to determine which power supplies provide voltages to the circuit being checked.

Adjust each voltage slowly to the marginal value by turning the adjustment screw (R1) on the applicable power supply. Measure voltage with a Weston 901 meter (0.5% accuracy) or equivalent. Voltage measurement points are listed on the following logic pages:

1801/1802	YA010
1826	YB140
1810	ZB101

The 1856 power pac voltages are measured at test jacks on the front of the unit.

On completion of testing, adjust each voltage as close as possible to the nominal value.

1.5 SLT MAINTENANCE

Maintenance procedures for standard SLT components are found in the Field Engineering Theory of Operation, *IBM Solid Logic Technology Packaging, Tools, Wire Change Procedure. (See FE Bibliography -- 1800 System,* Order No. SY26-0560.)

Voltage levels and delays for many released SLT circuits are listed in the Field Unit System Engineering Document (FUSED) in volume 0 of the 1801/1802 system diagrams.

1.5.1 SLT Contact Wear

Avoid unnecessary removal and replacement of pluggable SLT components. The gold contact surfaces of SLT cards, cable cards, and board pins are rated for 50 insertions. Voltage crossover assemblies and other back-panel connector blocks are rated for five insertions. Serpent connector contacts are rated for 500 insertions.

1.5.2 Wire Color Codes

SLT panel wiring in the 1800 system conforms to the standard SLT color code designations: yellow identifies wiring that is controlled by computer-generated rework instructions, blue/white identifies uncontrolled wiring, blue identifies temporary wiring installed by REA (Request for Engineering Action), and black and yellow twisted pair is used for temporary cable repairs.

In addition, two special colors are used in the 1800 system for the following types of discrete wiring: violet is used for manually controlled wiring (customer-assignable, manual listing or Feature II addition) that cannot be handled by computer-generated rework instructions, and red is used for all RPQ discrete wire adds. Repairs to nets that contain violet or red wire must always have that portion of the net restored completely, using the same color of special wire that existed before the repair. The part numbers for the special colors of No. 30 AWG solid copper wire are: violet, 811696; and red, 811693.

1.5.3 Machine Cable Installation

Cable reference drawings are included in the 1800 shipping group for use during system installation and when making cable repairs or engineering changes. Of particular importance are the diagrams that explain the coordinate system used for routing flat cables:

Frame	Reference Drawing
1801/1802	2195900 (sheets 6 and 9)
1828	2195901 (sheet 2)
1826	2195902 (sheet 2)
1810	2195903 (sheet 3)

Two types of 20-signal flat cables are used in the 1800 system: single-layer white (60 wires), and bonded yellow

(20 wires). The white cables may be precreased at each fold and marked with a transverse line at each clamp position. Bonded cables are unmarked and are not precreased.

Cables that are marked at the fold position should be folded so that the mark is inside the fold.

Note: The 33 AWG solid copper conductors in white flat cable can be broken by repeated folding and unfolding of the cable. Yellow bonded cables contain 22 AWG stranded wire that is not as susceptible to breakage.

The installation instructions shipped with field bills of material direct the routing of flat cables as per the following example: C–B1A6 via B1S2, B2B2, A2B2, A1V2, C1C7 (loop 10 inches), P1R7, P1F7, S1F7, S1A7, S4A3, S4B6 to power tailgate connector. In this example, C–B1A6 identifies the "from" location as gate C, board B1, connector A6. The "via" locations specify the locations of folds or clamps. The routing of this particular cable is illustrated in Figure 1–26.

The SLT Flat Cable List which is shipped with white flat cables designated fold and clamp positions at each "via" location by channel (CH) and node (ND). Thus, the "via" location B1S2 would be shown as channel B1, node S2. Each "via" location on the cable list also specifies the length of cable, in hundredths of an inch, from the last "via" location to the present one, and specifies the fold type (FT). Fold types are shown in Figure 1–27.

The cable list P/N appearing on the "from" label of each flat cable identifies the cable group to which the cable belongs. The sequence number on the "from" and "to" labels identifies the installation sequence of each cable in the group.

Cable retainers, X-type and straight-type, are supplied in the basic machine shipping group and should be used when installing additional cable groups.

There are occasions when random length white cables are sent to the field. The cable list information must be used to install these cables. Random length cables may be longer than necessary, but will never be shorter. Random length cables are identified by a marking near the cable label, indicating the excess length. For example, a marking of +4 indicates an excess length of 4 inches. The excess length must be taken up at loop positions or by folding back in the channel. Random length cables do not have fold or clamp marks but may be precreased. The precreasing on these cables is to be ignored.

If the "to" end of a cable must be twisted 180° for proper alignment of the connector, this can be accomplished by changing the fold at the last node from type A/B to type D/E or vice-versa. If a cable must be repositioned at the exit point of the channel this can be accomplished at the last fold as shown in Figure 1–28.

1.6 CRITICAL CIRCUITS AND LEVELS

1.6.1 Sample Pulse Drivers (SPD's)

Proper operation of circuits using gated SPD's as inputs requires that the SPD's have proper turn-on transition time and proper voltage shift. The typical transition time for the +3V to 0V shift is 10 to 20 nanoseconds. If the transition time is greater than 30 nanoseconds, intermittent failures may result. The magnitude of the voltage shift is also critical and should be in the range of 2.8 to 3.3 volts when the particular SPD is used as a gated input. A lesser amount of shift can cause failures to set or reset a multi-input trigger (flip-flop) or to fire an SPD. Greater shift magnitudes can erroneously set or reset a gated trigger when the gate it not conditioned or erroneously fire a gated SPD when the gate is not conditioned.

Because of differences in ac input impedances, a pulse with a fast transition and proper shift is required to fire a gated input SPD, while a slower pulse with less shift will set a multi-input trigger. Therefore, the most common failures are erroneous setting of multi-input triggers and failure to fire gated SPD's.

When scoping SPD's, to check for transition time and shift magnitude, it is essential to use a probe with the shield grounded at the tip.

Defective SPD's can sometimes be detected by marginal checking. (See 1.4 cases 5 and 6.) Figure 1–29 shows SPD waveforms.

1.6.2 Singleshots (SS)

Singleshots of the 1800 system may be positively triggered by jumpering the '–DC reset' signal to the turn-on of the singleshot. Each operation of the 1801/1802 console reset switch produces one pulse to trigger the singleshot. The 1800 remote switch box may also be used, and each operation of the IMMED STOP switch produces a pulse to trigger the singleshot.

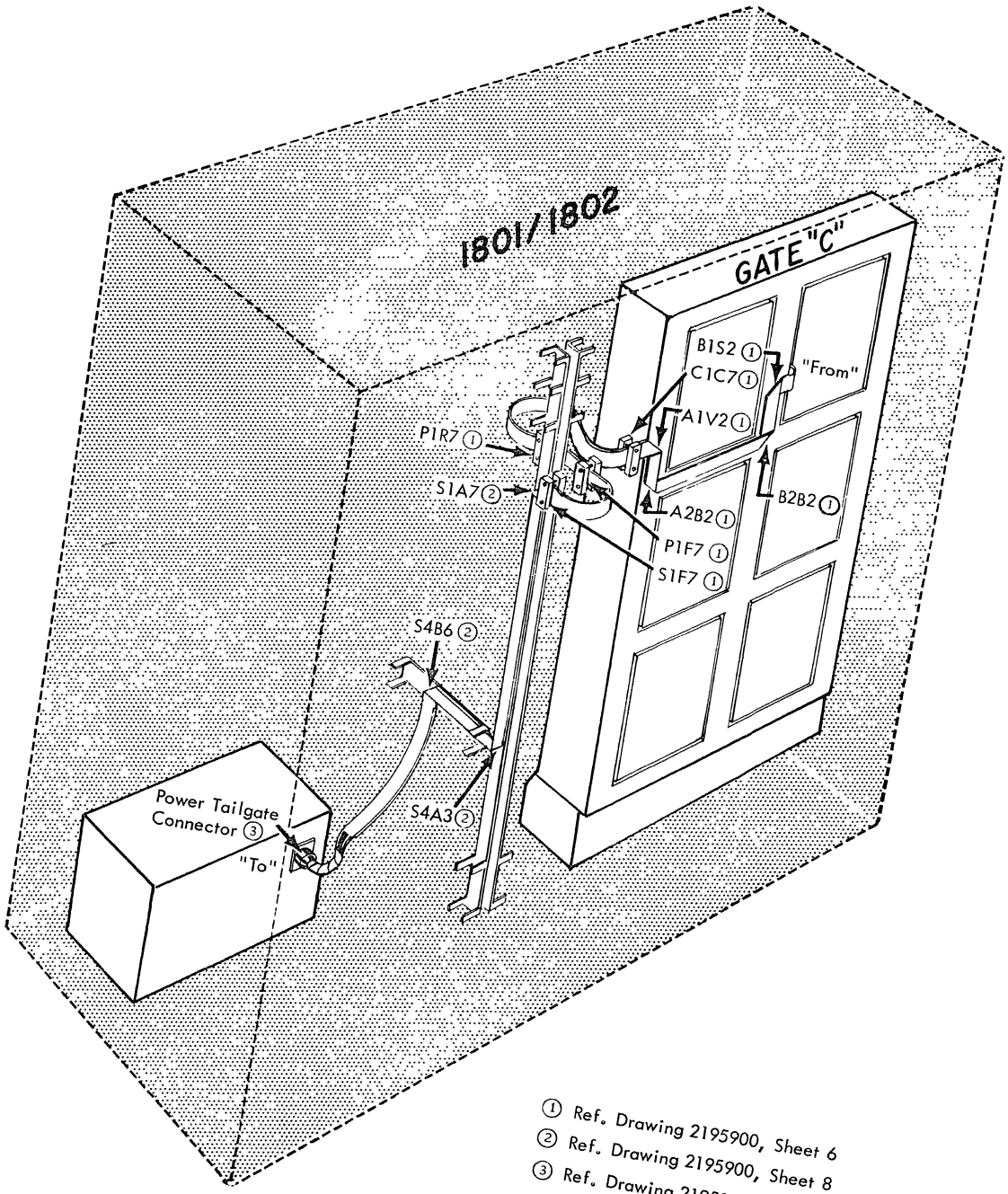
This method reduces the problem of multiple triggering which occurs when grounding singleshot inputs to trigger them.

CAUTION
Exercise normal SLT circuit caution to assure that the '–DC reset' line is not tied to the output of an emitter follower.

1.6.3 Phase A/B

The phase A/B adjustment is extremely important for proper CPU operation. Maladjusted phase A/B circuits can cause intermittent errors. Phase A/B problems usually appear first as unstable interval timer bases and failures in arithmetic circuits.

See 4.3.2 for phase A/B adjustment procedure.



① Ref. Drawing 2195900, Sheet 6
② Ref. Drawing 2195900, Sheet 8
③ Ref. Drawing 2195900, Sheet 3

14171

Figure 1-26. Flat Cable Routing

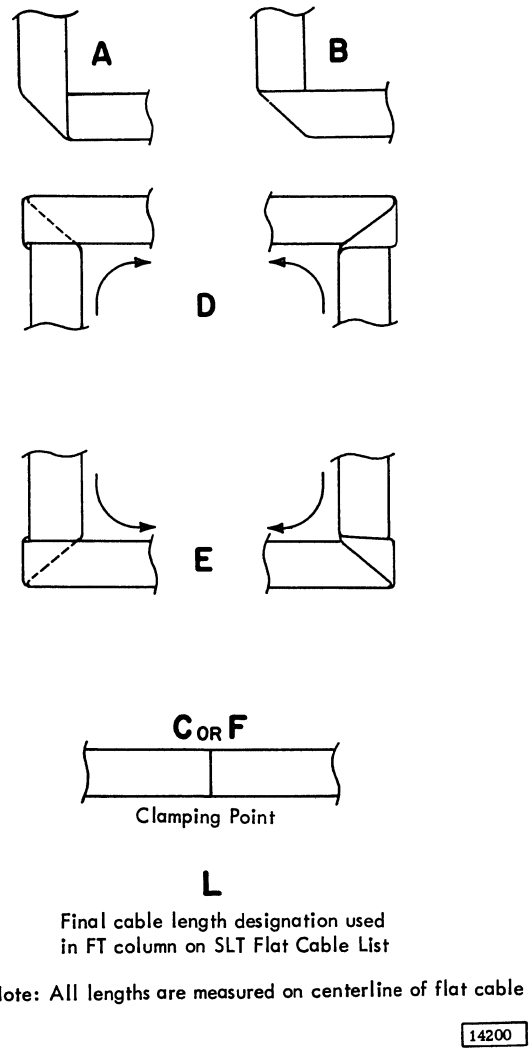


Figure 1-27. Cable Fold Types

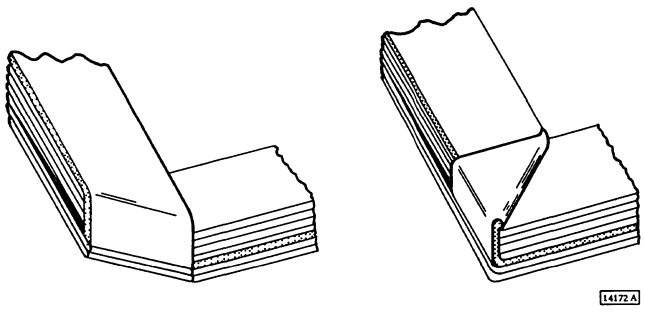


Figure 1-28. Methods of Repositioning Cable at "To" End

1.7 CORE STORAGE

1.7.1 Collection of Error Data

Request that the customer obtain all available data if parity errors occur. Record the B-reg, M-reg (SAR), I-reg, and, if the cycle-steal-service lamp is on, the channel address registers. It is also helpful to record the cycle (I, IA, E1, etc.) as well as the instruction and program. This information helps to reproduce the failure and aids in determining if a logic or instruction failure is associated with the problem.

Note: An 1800 Console Check Sheet is available to aid the customer in reporting intermittent failures. (See *FE Bibliography -- 1800 System,* Order No. SY26-0560.)

The following information will help prevent recording false and misleading data.

Locating Storage Positions With Parity Errors

The B-reg data is written into storage, even if a parity check occurs. This fact permits searching through storage to find any positions that have even parity.

To search for storage locations with parity errors:

1. Place mode switch in display position.
2. Turn check stop switch on.
3. Place write storage protect bits switch in no (off) position.
4. Place the display address register switch in the SAR position.
5. Display storage (clear storage in display mode).

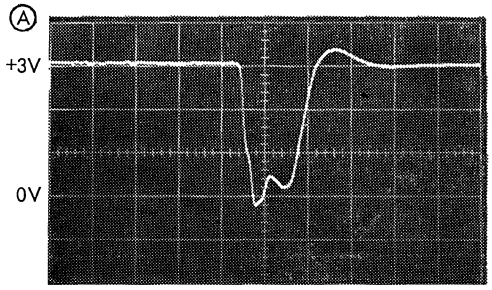
If a parity check stop occurs, the address register contains the location of the error. The B-reg contains the data in error. (The presence or absence of a storage protect bit and parity bit can be determined by their associated indicators.

Effect of Cycle-Stealing on SAR Display Lamps

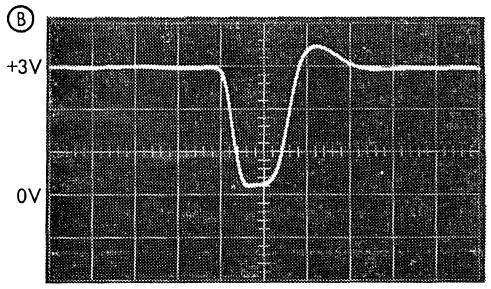
If a device initiates a cycle-steal operation after a check stop, the cycle-steal cycle will not occur, but the channel address register bits will be gated onto the storage address in bus and will be indicated in the SAR display lamps. If the SAR display is recorded under these conditions as the M-reg address that caused the check stop, erroneous results will be obtained.

As an example, many programs run with the interval timers as a source of program control. The timers function automatically when the program is at a "wait" or in run mode. They cannot function after a check stop, but the cycle steal used to update the interval timer can be attempted after the check stop. This attempt will prevent the true M-reg value from being indicated in the SAR display lamps.

If a parity error occurs and the cycle-steal-service lamp is on, search for the address that failed in display mode as

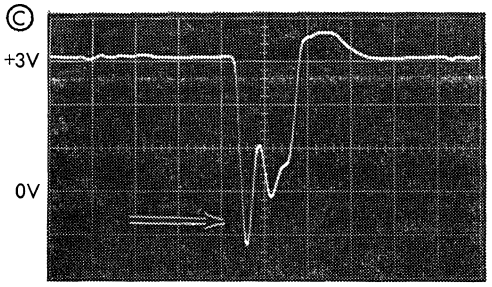


Signal: B-A2M3DO4 (CH111)
Sync: .....TO
Horiz: .....50 ns/div (0.5 μs with x10 Mag)
Vert: .....1V/div (grounded probe shield)



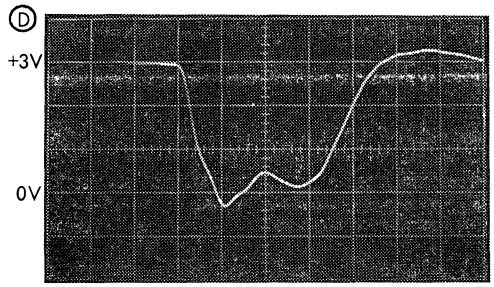
Same scope setup as Ⓐ

Views A and B show the different traces that can be encountered when the same pulse is viewed on different scopes. Wave form Ⓐ was viewed on a Tektronix 453. Wave form Ⓑ was viewed on a Tektronix 561S (note the loss of information in Ⓑ).



Signal: B-A2M3B05 (CH111)
Sync: ..... TO
Horiz: ..... 50 ns/div (0.5 μs with x10 Mag)
Vert: ..... 1V/div (grounded probe shield)

This is the load end of an SPD that is driven from one board to another. A pulse with a 4V shift such as this is acceptable only when driving a circuit with a grounded gate (see 1 .6).



Signal: B-B2J6D07 (CE311)
Sync: ..... TO
Horiz: ..... 20 ns/div (0.2 μs with x10 Mag)
Vert: ..... 1V/div (grounded probe shield)

This SPD pulse is shown on an expanded oscilloscope time base to show the turn-on transition time of 20 nanoseconds.

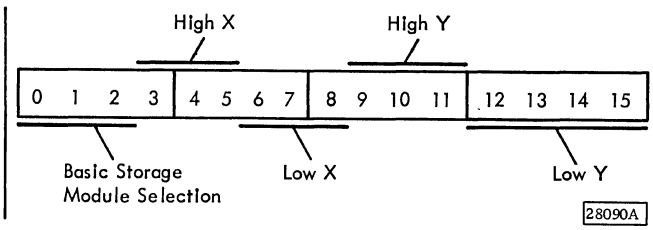
28086

Figure 1-29. SPD Waveforms

explained in "Locating Storage Positions with Parity Errors" (1.7.1). Failure to do so may result in working on the wrong storage module.

1.7.2 Main Storage Addressing and Selection

To detect a possible address failure pattern, the address must be analyzed in core storage address format.



Bit Function in Address Word

Bit 0: Bit 0 selects upper (on) or lower (off) 32k of storage if expanded core feature is installed.

Bits 0, 1, and 2: Bits 0, 1, and 2 select the basic storage module (BSM), which is an 8k increment of storage (one SLT board with cards, and array). This selection (Figure 1–30) is implemented by wired-logic jumpers (violet wires) on each core storage board.

Bits 3 through 8: Bit 3 selects the lower or upper 4k of the selected BSM. This bit is used for selecting the appropriate strobe pulse and sense amp and is part of the high-X decode. Bits 3 through 5 select high-X lines and bits 6 thru 8 select low-X lines. This results in a decode of one of 64 X lines.

Storage Capacity	Portion of Storage	Bit 0	Bit 1	Bit 2	BSM Location	Hand Wired Logic			
						Bit	From	2µs SA111 To	4µs SD331 To
4k	ALL	*	*	*	B-A3	1	*	*	*
						2	*	*	*
8k	ALL	*	*	*	B-A3	1	*	*	*
						2	*	*	*
16k	1st 8k	*	*	off	B-A3	1	*	*	*
						2	M1E09	N2G09	N2D02
	2nd 8k	*	*	on	B-B3	1	*	*	*
						2	M1E11	N2G09	N2D02
24k	1st 8k	*	off	off	B-A3	1	N1A09	N2G10	N2D06
						2	M1E09	N2G09	N2D02
	2nd 8k	*	off	on	B-B3	1	N1A09	N2G10	N2D06
						2	M1E11	N2G09	N2D02
	3rd 8k	*	on	*	A-B3	1	N1A11	N2G10	N2D06
						2	*	*	*
32k	1st 8k	*	off	off	B-A3	1	N1A09	N2G10	N2D06
						2	M1E09	N2G09	N2D02
	2nd 8k	*	off	on	B-B3	1	N1A09	N2G10	N2D06
						2	M1E11	N2G09	N2D02
	3rd 8k	*	on	off	A-B3	1	N1A11	N2G10	N2D06
						2	M1E09	N2G09	N2D02
	4th 8k	*	on	on	A-A3	1	N1A11	N2G10	N2D06
						2	M1E11	N2G09	N2D02
65k	1st 8k	off	off	off	1801/2 A-B3	1	N1A09	N2G10	Not available
						2	M1E09	N2G09	
	2nd 8k	off	off	on	1801/2 A-A3	1	N1A09	N2G10	
						2	M1E11	N2G09	
	3rd 8k	off	on	off	1801/2 B-B3	1	N1A11	N2G10	
						2	M1E09	N2G09	
	4th 8k	off	on	on	1803 B-A3	1	N1A11	N2G10	
						2	M1E11	N2G09	
	5th 8k	on	off	off	1803 B-B2	1	N1A09	N2G10	
						2	M1E09	N2G09	
	6th 8k	on	off	on	1803 B-A2	1	N1A09	N2G10	
						2	M1E11	N2G09	
	7th 8k	on	on	off	1803 B-B1	1	N1A11	N2G10	
						2	M1E09	N2G09	
	8th 8k	on	on	on	1803 B-A1	1	N1A11	N2G10	
						2	M1E11	N2G09	

* Not Wired

Note:
On Expanded Core Systems, the bit 1 and 2 wiring is as for two groups of 32k (lower 32k and upper 32k). Within the logic, bit 0 is used to select the lower or upper 32k groups. For systems with less than 65k (or if it is desired to wire for less than 65k in an emergency), the lower 32k is wired as shown. The upper 32k group is wired as a portion of a 32k group. Example: For a 49k system, wire BSM 1-4 as shown. Wire BSM 5 and 6 as 16k is wired on the basic 32k system.

28079A

● Figure 1-30. BSM Selection

Bits 9 thru 15: Bits 9 thru 11 select high-Y lines and bits 12 thru 15 select low-Y lines. This selection results in a decode of one of 128 Y lines.

Determining Address Failure Patterns

A single X or Y line is selected by the high-X or high-Y address at one end of the matrix, and by the low-X or low-Y address at the other end of the matrix. If both high X and low X are common to all or most failing addresses, an X line failure pattern is indicated. If only the high-X or low-X portion is common to the failing addresses a high-X or low-X address failure pattern is indicated. The same holds true for Y lines and addresses.

Wraparound Characteristics of Core Storage

The core storage address register (M-register) begins at /0000 and ends at /FFFF. Core storage addresses begin at /0000 but end at the highest addressable word (asterisked word in Figure 1–31). If an address is used that exceeds the size of available storage, the bits not needed to address the highest storage position are ignored. Thus, in a 16k system, address /FFFF or /3FFF selects the highest storage position. If either of these addresses is incremented, the lowest storage position is selected. This continuation in storage addressing is known as wraparound. Wraparound in storage addressing is illustrated in Figure 1–31.

In 24k systems, wraparound is different from that previously described. This difference is caused by bit 2 being ignored when selecting the third 8k module and decoded when selecting the first and second 8k modules. See figures 1–30 and 1–31.

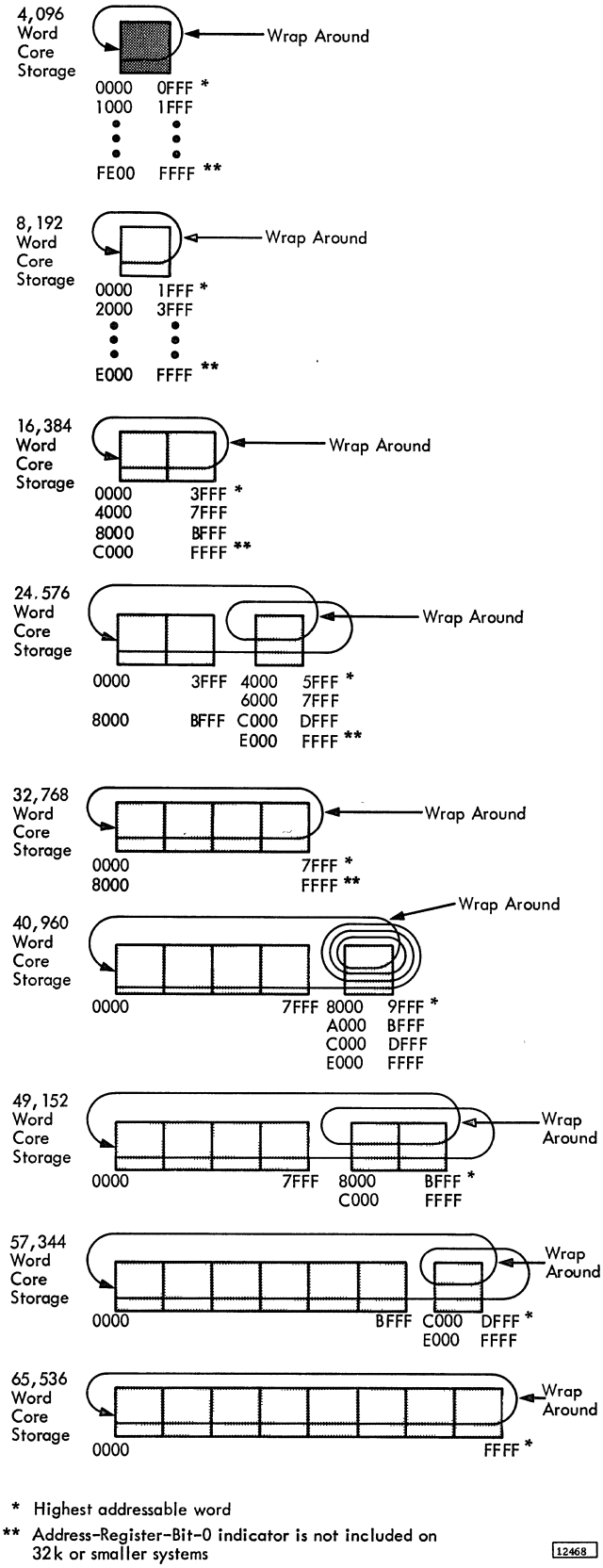
In 40k systems, bits 1 and 2 of upper 32k are not wired (ignored) when bit 0 selects the upper 32k of core storage. In this wraparound each word in the fifth 8k module is addressed four times as the address register goes from /0000 to /FFFF.

In 49k systems, bit 1 of the upper 32k is not wired (ignored) when bit 0 selects the upper 32k section of core storage. Each word in the fifth and sixth 8k modules is addressed twice as the address register goes from /0000 to /FFFF.

In 57k systems, bit 2 is not wired (ignored) when bits 0 and 1 address the upper 16k of the upper 32k words. Thus, the seventh 8k module words are addressed twice as the address register goes from /0000 to /FFFF.

1.7.3 Core Storage Display Procedure

The following procedure may be used to display core storage data between the execution of single instructions:



● Figure 1-31. Main Storage Wraparound

1. With the P–C in a stopped condition, position the mode switch to SI (single instruction).
2. Start switch depressions may now be used for single-instruction operations to get the program to the desired point for data display.
3. Record the address appearing in the I-register. The I-register is used to address the data to be displayed, and this recorded address will be needed to return the P-C to the next instruction upon completion of the display procedure.
4. Using the data-entry switches, set up the address of the core storage word to be displayed.
5. Position the mode switch to LOAD; press LOAD I.
6. Set WSPB switch to NO.
7. Position mode switch to DISPLAY.
8. Press START. The selected word is now displayed in the B-register indicator lamps. Successive start-key depressions will display succeeding core locations.
9. To display other areas of core storage, repeat steps 4 through 8.
10. To continue the program:
    a. Set data-entry switches to the address recorded in step 3.
    b. Position mode switch to LOAD; press LOAD I.
    c. Position mode switch to RUN; press START.

Core storage data cannot be displayed between single machine cycles of an instruction without losing the integrity of the P–C program.

1.7.4 Scoping Techniques

Clear Storage Approach

Clearing storage in run mode permits scoping while intermittent or solid failures exist. The data is transferred from the data entry switches to the B-reg at T3 time. Therefore, the correct data is known and can be traced all the way into core storage on the write cycle and all the way out to the B-reg on the read cycle. If an error occurs, the original data is restored at T3 time. In other modes of operation, after the error occurs, the erroneous data is regenerated, allowing the failure to occur only once. The clear-storage operation breaks this feedback loop, allowing the failure to recur.

Single Address Operation

Cycling the machine on a single address is an effective technique for scoping core storage. This technique can be used in conjunction with a clear-storage operation. In single address operation, the increment to the I-reg must be blocked by grounding the 'incr I Reg' SPD line at B–A2K6B03, thus forcing the machine to cycle at one address. Insert the ground jumper only when the machine is stopped.

Distinguishing Between Correct and Incorrect Waveforms

Make scoping comparisons between a failing storage module and a non-failing storage module to determine correct or incorrect conditions. See "Core Storage Waveforms" (1.7.8) for typical storage waveforms.

1.7.5 Swapping BSM Address Assignments

Because all BSM's are connected to the same storage interface, the address assignments of two BSM's can be swapped by changing the hand-wired logic on the storage boards.

Without 1803 Adapter

Each BSM (except 4k and 8k systems) has handwired logic (violet wire) to decode address bits 1 and/or 2 (Figure 1–30). By changing these decode wires to different pins on the storage board, the address assignments of two BSM's can be exchanged.

For example, on a 16k system it is only necessary to change one wire on each 8k BSM to swap the low- and high-order 8k portions of storage. The two wires are shown in Figure 1–30 as the bit 2 decode. On a 32k system, to swap the low- and high-order 8k portions of storage, two wires must be changed on each BSM (bits 1 and 2 decode).

Note: Physically exchanging the locations of any two BSM's will not change their positions in storage addressing. They will continue to represent the same addresses of main storage until their decode wires are changed.

With 1803 Adapter

The address assignment of a BSM in the upper (32-65k) BSM group cannot be swapped with one in the lower (0-32k) group because the physical position of BSM's in the system determines selection by bit zero position of the address. Bit 0 = 1 ('storage select 32-65' line, WZ20101) is sent from the P–C to the four BSM locations in the 1803 assigned to the upper 32k group (BSM V – VIII, Figure 6–16).

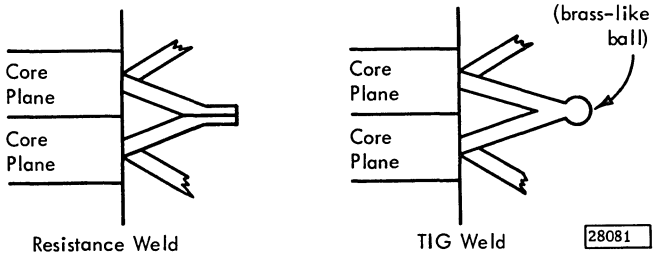
The single BSM of the lower 32k group assigned to a location in the 1803 (BSM IV) is selected by 'storage select SPD 24-32k' when bit 0 = 0. 'Storage select SPD 0-24k' selects the three remaining BSM's of the lower 32k group assigned to the 1801/2 when bit 0 = 0.

The upper 32k group can be operated as the lower 32k group or vice versa if the technique given on WZ331 is followed. Note, however, that the group that has not been reassigned cannot be addressed during this procedure.

BSM address assignments can be swapped within their own group except that no BSM in the 1803 may be assigned as BSM I. Because of line delays, the interval timers at location /0004, 5, and 6 (BSM I) operate incorrectly if located in the 1803.

1.7.6 Array Swapping (Physical)

Prior to September 1966 arrays were welded by a resistance welding technique. Since this date arrays have been welded by a method known as tungsten inert gas (TIG) welding. The TIG welded array can be identified by a brass-like ball at the weld.



The TIG welded arrays have slightly longer pins than the resistance welded arrays. The TIG welded array cannot be installed in a BSM that was previously fitted with a resistance welded array unless a check is made to ensure that the card guides above the array have had their lower edges cut off. The TIG welded array requires this extra clearance. Otherwise, 8k arrays are fully interchangeable. Array swapping is an effective troubleshooting technique but it must be done with care; 4 μs and 2 μs arrays are not interchangeable. See array removal procedure in section 4.4.4.

1.7.7 Trouble Diagnosis

When attempting to analyze core storage problems, determine if a failure pattern exists. To determine a failure pattern, console data must be accurately recorded for all failures.

Out-of-tolerance voltages and timings can give a misleading failure pattern. For example, a late strobe timing condition can cause one bit to fail. The earliest peaking core (core causing earliest sense line waveform peak) will fail first if strobe timing is late. The failure pattern for this condition would indicate a component that is common to only the failing bit, but the actual correction would be an adjustment of strobe time.

The Core Storage Diagnostic Guide (Figure 1–32) associates various failure patterns with possible failure causes. Review this entire section (1.7.7) before beginning trouble diagnosis.

1. Problems Common to All BSM's

A failure pattern including more than one BSM generally indicates a failure in the interface to the storage units rather than in the actual storage unit itself. The interface to core storage includes the B-reg, M-reg, CAB reg, channel

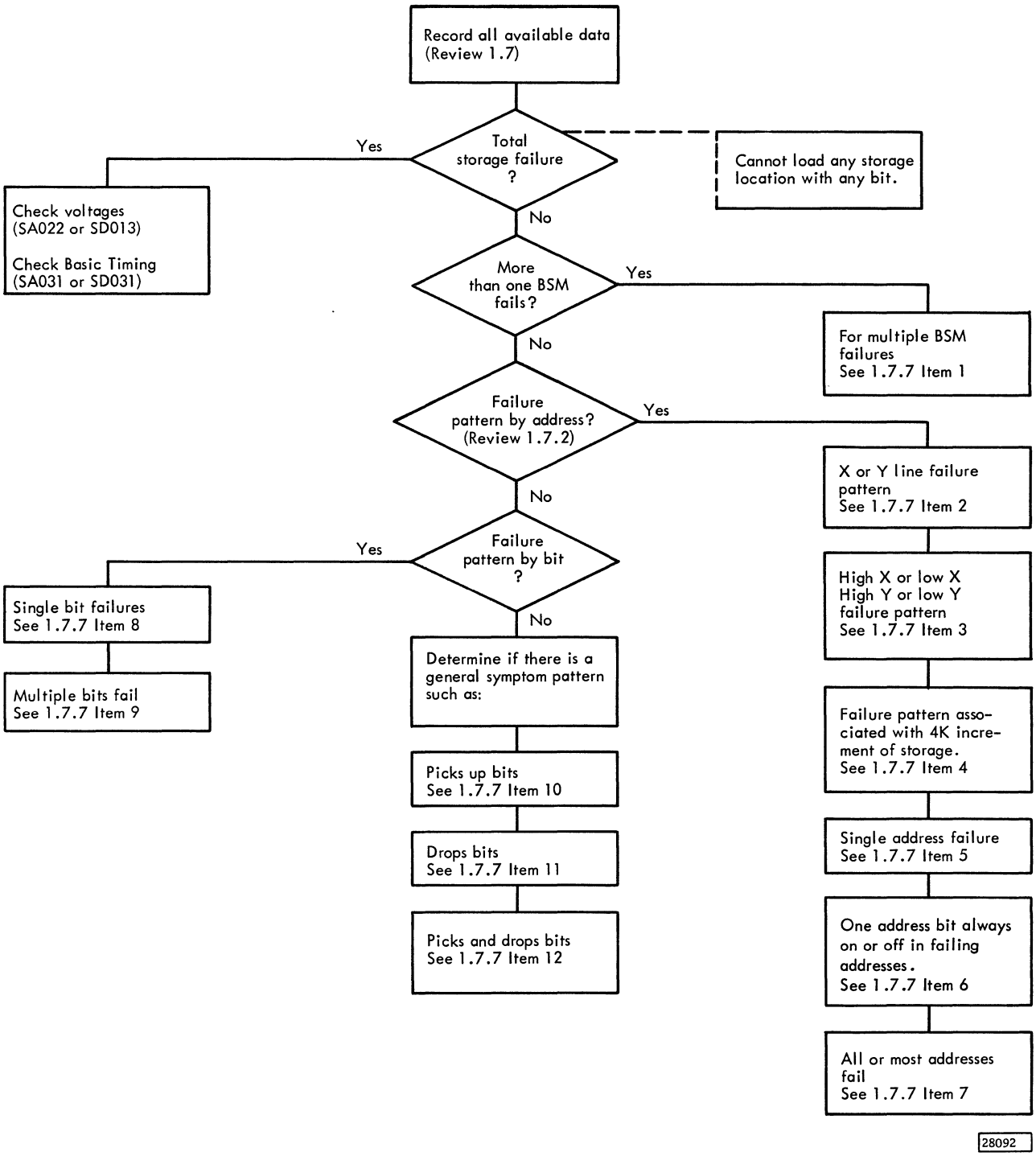


Figure 1-32. Core Storage Diagnostic Guide

address registers, cables, connectors, and general control signals.

Check address bits for proper timing and level. To check timing, clear storage to /6000. At storage location /0000 and /0001 enter /6400 and /7FFF respectively. Place mode switch in run, reset and push start. This permits scoping of the address bits (cannot be done in clear-storage mode). These bits have critical timing requirements. Bits 1 and 2 have earlier timings than the other bits and must be present (at decision level) before the 1.8V level of 'storage select' (2 μs) or 'read cycle' (4 μs) time. The other bits must be stable 25 nanoseconds after the 1.8V level of 'storage select' (2 μs) or 'read cycle' (4 μs).

Check basic core storage voltages (SA022 or SD013).

2. X or Y Line Failure Pattern

Check the driver and gate cards by substituting a new card or interchanging cards of the same type. To check for an open line or defective line weld, check continuity of the line through the array (line path example is given on SA012 or SD012).

The following are typical resistances for X or Y lines. The measurements are made from one end of the line to the other end of the line with no diodes in the circuit.

	8k	4k
Y-drive line:	5 ohms	2.5 ohms
X-drive line:	8.5 ohms	8.5 ohms

High resistance in the drive line can cause dropping of bits. The high resistance can be caused by poor line welds, high-resistance bottom board pins, poor connection in the connector block, or by a defective diode.

The most difficult drive line problem to diagnose is the defective diode, which can cause several different failure symptoms. There are two diodes associated with each drive line, one for read and one for write. Either can cause a problem but the read diode is more critical. A change in the diode response time will change the timing of the sense-line wave form. The read diode is more critical to response time because the sense line waveform must be timed properly to the strobe pulse.

A diode having improper resistance can usually be detected by a static resistance check. Compare the suspected diode with the readings of other diodes in the BSM. However, a diode with poor response time will usually measure good with a static check and will usually operate properly in a sequential addressing mode, such as display mode. However, it may fail to conduct properly in certain program loops. It may be possible to detect a faulty read diode by moving the strobe later by approximately 20 nanoseconds. If this adjustment improves operation, it is possible that a diode with poor response time has caused the core output to be later and more compatible with the later strobe. A write diode failure will not be affected by strobe timing.

A high-resistance or poor-response-time diode will have an X- or Y-drive line failure pattern. A shorted diode will have a failure pattern including most drive lines (Figures 1–36 and 1–45). If a problem can be related to a suspected diode, replace the diode. For diode replacement information, see 4.4.6.

Check for leakage between the X or Y line and a sense line as explained in item 8.

Scope the failing storage module using the techniques explained in 1.7.4.

3. High-X or Low-X, High-Y or Low-Y Failure Pattern

Possible causes are driver or gate cards, defective connector block, defective diode (see item 2), current balance (2 μs storage units), or bottom board leakage (see item 8).

Try replacing suspected card or connector. Scope failing addresses.

4. 4k Increment Failure Pattern

This could be associated with address bit 3 or the 'less than 4k' or 'greater than 4k' strobe. Check the strobe pulse and strobe timing.

If failure is bit-oriented it could be caused by a defective sense amp, inhibit driver, or sense line. There is one inhibit driver for each of the 18 bit positions in each 4k of storage. If an inhibit driver never conducts, that bit position enters 4k of storage continuously. If it always conducts, the bit can never be entered into that 4k. Any other 4k segment of core functions correctly. If there is a bit failure through 4k of core, replace the inhibit driver and sense amplifier cards for that bit position. If the trouble is not a card, but sense/inhibit failure is suspected, check the continuity of the sense/inhibit line. See item 8 for discussion of single bit failures and sense line resistance measurements.

5. Single-Address Failures

This kind of failure is often the result of a weak or early-peaking core whose output is made more marginal by low VRef (determines drive current level) or poor current balance (2 μs storage units). Other causes can be a late strobe, high Vsa - Ve (determines sense-amp threshold for 1 bit, adjustable only in 4 μs storage), or a large deviation from a nominal (60°F - 90°F) room environment.

As temperature increases, cores peak earlier and higher, but ideally the strobe does not change its timing. The strobed signal is therefore lower at increased temperatures because the strobe occurs later in the signal.

As temperature decreases, more current drive is required to obtain the same output. Occasionally, some cores give a very low output at low temperatures. The peak also occurs later at lower temperatures. In the 4 μs storage, low-output cores can cause a bit-dropping problem that is severe enough to warrant replacement of the storage unit. A possible temporary fix is to increase Vref, or drop Vsa (adjustable only in the 4 μs storage) to its lower limit.

To isolate the failure, BSM's and arrays may be swapped as explained in 1.7.5 and 1.7.6.

6. One Address Bit Always On or Off in Failing Addresses

Check the level and timing of the bit in question. See procedure for scoping address bits in item 1.

7. All Addresses or Most Addresses Fail

This condition generally indicates something basically wrong in the addressing (current drive) or sense system.

The best way to begin analysis is to scope the sense lines. This scoping indicates whether a current drive or sensing failure exists. Check all basic adjustments and timings. (See 4.4.3.) Review core storage waveforms as shown in Figures 1–32 through 1–44.

If all failing addresses are picking or dropping a common bit, see item 8.

8. Single Bit Failures

If the failure is relatively solid, determine and replace the sense amp (<4k or>4k) associated with the failing bit.

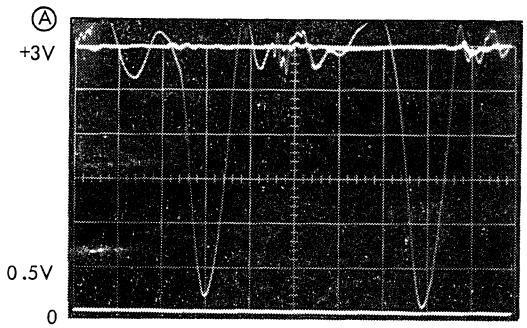
On intermittent problems sense amps can be swapped, but unless the trouble actually moves with the sense amp the results are inconclusive. Sense amps have an area of undefined output between the region of a guaranteed 1 and a guaranteed 0. Therefore, it is advisable to check basic adjustments on intermittent problems. (See 4.4.3.)

Check for continuity of the sense/inhibit winding. The sense/inhibit loop should measure approximately 8 ohms. Each side of the loop (through 2,048 cores) should measure approximately 4 ohms to the sense-line common. Pin locations for these measurements are shown on system diagrams SA061-062 (2 μs) and SD061-062 (4 μs). Unbalanced resistance can cause extra bits. Check the jumper block for high resistance. High resistance pin connections in the bottom board can cause an unbalanced sense line. This imbalance will cause picked bits.

Shorted sense/inhibit lines (between pairs of lines) can cause picking or dropping of one or both of the bits associated with the shorted lines. This condition can be detected by measuring between line pairs. With the sense/inhibit cards installed, the resistance will be low. With the cards removed, there should be at least 5 megohms resistance and normally 10 to 20 megohms resistance.

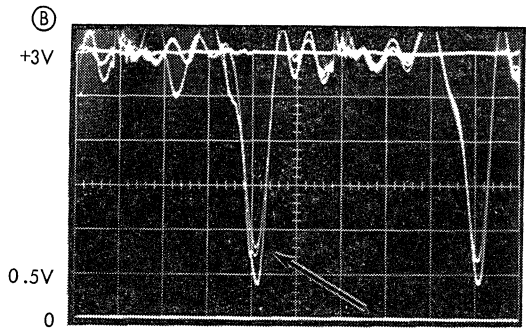
Note: To ensure accurate resistance measurements when checking for line leakage, use the following procedure:

a. Use a Simpson 260 meter or meter with equivalent battery potential.
b. Use x10k or x100k resistance scale.
c. Hold leads on plastic insulated areas only; body resistance can cause erroneous readings.



Signal: N2J02 (SA311)
Sync: T0
Horiz: ..... 0.2 μs/div
Vert: 0.5V/div

This is the output of the 1 μs delay line which provides base timing control pulses for the 2 μs storage. All delay line outputs should ressemble this. Note 60 ns or greater pulse width at 1V level and down level of 0.3V or lower.



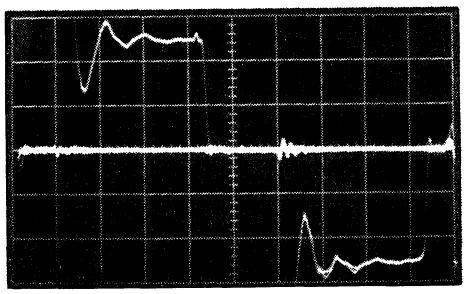
Same scope setup as Ⓐ .

This is an example of poor output from the 1 μs delay line (should be like Ⓐ). The 50 ns pulse width and marginal down level of 0.8V to 0.4V will cause failures to set and reset control flip-flops.

28100

Figure 1-33. 1-Microsecond Delay Line Output

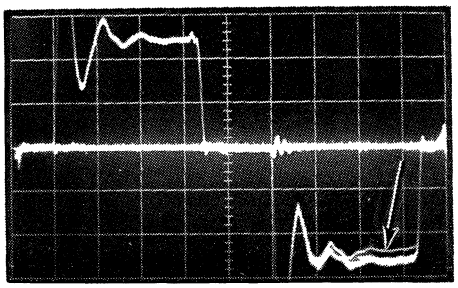
Ⓐ



Signal: K5B04 (SA421)
Sync: T0
Horiz: .....0.2 µs/div
Vert: .....100 mA/div (current probe)

This picture shows Y read and write current, compare with waveform Ⓑ.

Ⓑ



Same scope setup as Ⓐ

This current wave form is taken from the same point as Ⓐ. The arrow points out excessive (35 mA) write current oscillation. Any sink source card that exhibits more than 10 mA or write read current oscillation should be changed.

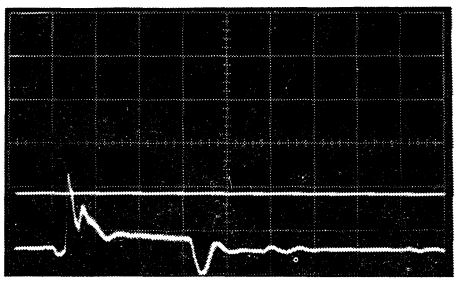
28088

Figure 1-34. Y-Current Waveforms (2 µs Storage)

Ⓐ

+3V

0V



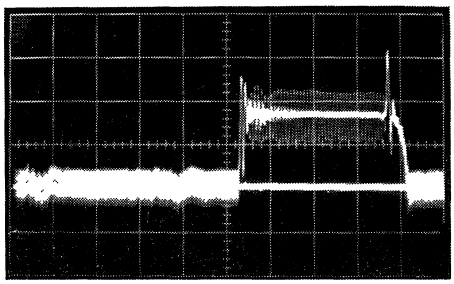
Signal: H2D09 SA411
Sync: ..... T0 or Read Cycle EIEII
Horiz: ..... 0.2 µs/div
Vert: 1V/div

This is a typical wave form for 'Y read source' or 'X read source' (J2D09 on SA411). 'X read source occurs 100 ns earlier.

Ⓑ

+3V

0V



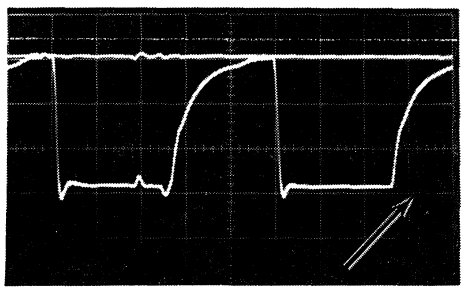
Signal: J2B12 SA411
Sync: ..... T0 or Read Cycle EIEII
Horiz: ..... 0.2 µs/div
Vert: 1V/div

This is a typical wave form for 'X write driver time'. 'Y write driver time' is similar but 100 ns later.

Ⓒ

+3V

0V



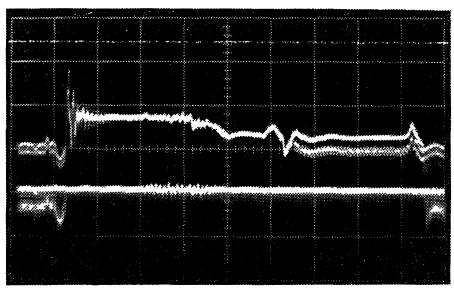
Signal: N2G02 SA311
Sync: .....T0 or Read Cycle EIEII
Horiz: .....0.2 µs/div
Vert: 1V/div

This is a properly operating short-time latch, which provides base timings for currents and strobe. If an insufficient reset pulse occurs, faint undertraces will be seen where the arrow points.

Ⓓ

+3V

0V



Signal: H2B1O SA411
Sync: ..... T0 or Read Cycle EIEII
Horiz: ..... 0.2 µs/div
Vert: 1V/div

This is a typical wave form for 'Y read gate time'. 'X read gate time' is similar but 100 ns earlier.

28087

Figure 1-35. Various Waveforms (2 µs Storage)

d. Allow meter to remain attached to points being measured for at least 30 seconds if less than several megohms is initially measured. If leakage does exist, a breakdown phenomenon can occur, causing reading to drop after a period of time.

Leakage can occur between a sense line and an X-drive line. Check this condition as follows:

a. Remove sense-line connector block associated with bit to be checked (SA061-062 or SD061-062).
b. Check for resistance between the sense line of the failing bit and the following driver gate pins:

2-Microsecond Storage Units
M3B12, L3D05, F2D05, F2B05

4-Microsecond Storage Units
J3D10, K3D06, J2D10, J2B05

BSM bottom board leakage can occur between a sense line and an X or Y line and will be related to a low- or high- order X or Y address. Check for this leakage as follows:

a. Remove sense line connector block associated with bit to be checked. (SA061-062 or SD061-062).
b. Check for resistance between the sense line of the failing bit and the following pins:

2-Microsecond Storage Units

Card Sockets	Pins in Each Socket
C3, D3	B12, D05
E3, F3	D10, D11
L3, M3	
G3, H3	B03, B04
J3, K3	B05, B12
	D04, D05
	D10, D11

4-Microsecond Storage Units

Card Sockets	Pins in Each Socket
C3, D3	B08, D05
E3, F3	D06, D10
J3, K3	
G3, H3	B04, B05
L3, M3	B08, B12
	B13, D05
	D06, D10

The readings obtained in the previous checks should be approximately 5 to 50 megohms. A unit with 100k ohms resistance will work but experience has shown that units with a leakage path lower than several megohms will continue to deteriorate and eventually cause intermittent parity errors. Defective units have also exhibited a momentary breakdown from 5 megohms to 5k ohms under heat, vibration, or extended operation.

Storage adjustment or card swapping can affect a problem caused by sense-line-to-sense-line or sense-line-to-drive-line leakage, but storage replacement is the only permanent solution. Before a storage unit is replaced for leakage, it should be thoroughly checked to ensure that leakage is not caused by external components such as connector pins or connector blocks.

9. Multiple Bits Fail

This condition generally suggests a basic problem in current drive or sensing. Determine whether failing bits share connectors or SLT cards. If no obvious cause is found, check strobe timing and sense line and current waveforms. For core storage waveforms see 1.7.8.

Determine if an address failure pattern exists.

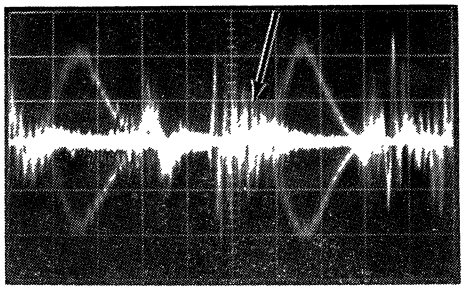
10. Picks Up Bits

a. Low Vsa - Ve (sense level control voltage - offset voltage, sets threshold of a 1 in sense amp).
b. Strobe early.
c. Unbalanced sense line (item 8).
d. Leakage from drive line. (See item 8.)
e. Double strobe (logic failure).
f. Current drive high. (Vref determines current level.)
g. Defective diode. (See item 2.)

11. Drops Bits

a. Weak core (one address, one bit).
b. High Vsa - Ve. (See item 10.)
c. Strobe late.
d. Leakage from drive line. (See item 8.)
e. Current drive low. (Vref determines current level.)
f. Defective diode. (See item 2.)

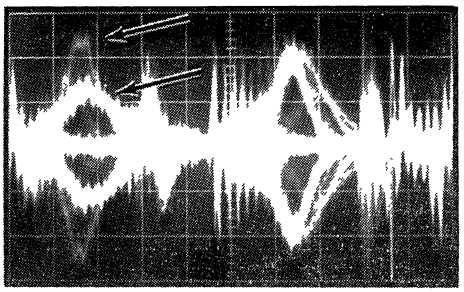
Ⓐ



Signal (Ch 1): M7B02 (SA561)
Signal (Ch 2): M7D02 (SA561)
Sync: T0
Horiz: .....0.2 μs/div
Vert (Ch 1): .....20 mV/div
Vert (Ch 2): .....20 mV/div (Inv)
Mode: .....Add (differential scope cable)

This photo shows a typical sense line while reading or writing all ones. Bit-14 sense line was used (< 4k) during a clear or display storage operation. The arrow points to noise coupled from the inhibit noise of other sense lines.

Ⓑ



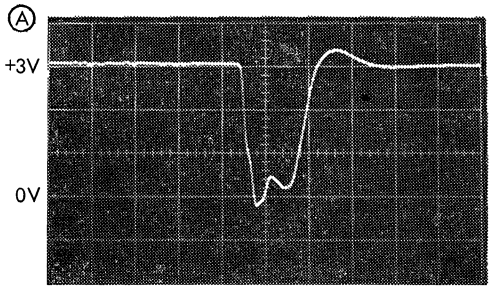
Same scope setup as Ⓐ .

This wave form was viewed with the conditions of clearing storage to all bits and having a shorted diode. Addresses that would normally cause diode to conduct have large signals. (< 50 mV), and addresses that would normally prevent conduction of diode have small signals (20 - 30 mV). This causes the picking-and-dropping-bits symptom that accompanies shorted diodes. Photo Ⓐ shows signal under normal conditions.

28085

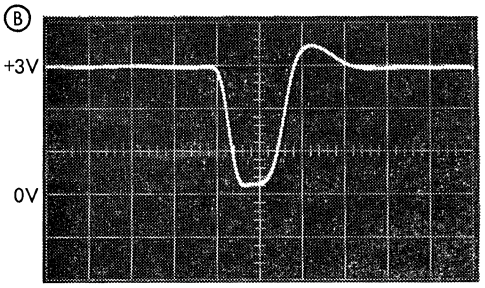
Figure 1-36. Effect of Shorted Diode on Sense-Line Waveform (2 μs Storage)

Ⓐ



Signal: B-A2M3DO4 (CH111)
Sync: T0
Horiz: .....50 ns/div (0.5 μs with x10 Mag)
Vert: .....1V/div (grounded probe shield)

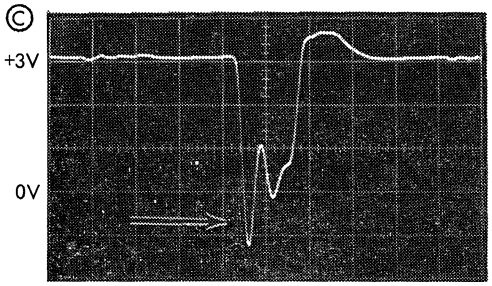
Ⓑ



Same scope setup as Ⓐ

Views A and B show the different traces that can be encountered when the same pulse is viewed on different scopes. Wave form Ⓐ was viewed on a Tektronix 453. Wave form Ⓑ was viewed on a Tektronix 561S (note the loss of information in Ⓑ).

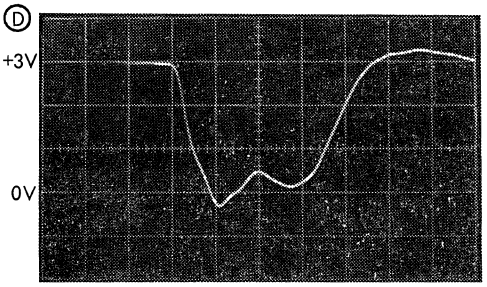
Ⓒ



Signal: B-A2M3B05 (CH111)
Sync: T0
Horiz: ..... 50 ns/div (0.5 μs with x10 Mag)
Vert: ..... 1V/div (grounded probe shield)

This is the load end of an SPD that is driven from one board to another. A pulse with a 4V shift such as this is acceptable only when driving a circuit with a grounded gate (see 1 .6).

Ⓓ



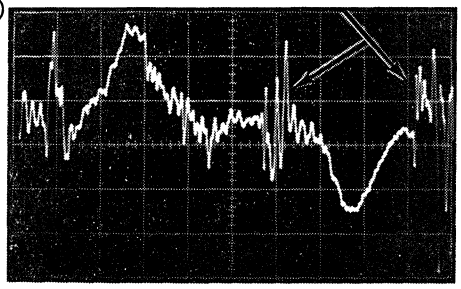
Signal: B-B2J6D07 (CE311)
Sync: T0
Horiz: ..... 20 ns/div (0.2 μs with x10 Mag)
Vert: ..... 1V/div (grounded probe shield)

This SPD pulse is shown on an expanded oscilloscope time base to show the turn-on transition time of 20 nanoseconds.

28086

Figure 1-37. Sense Line Waveform for Single-Bit, Single-Address Operation (2 μs Storage)

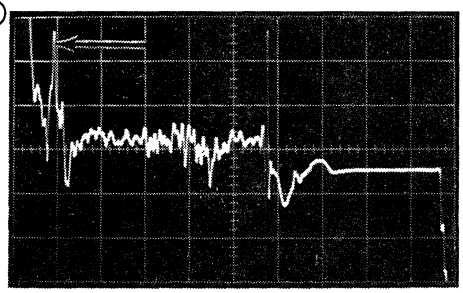
Ⓐ



Signal (Ch1):..... M7B02 (SA561)
Signal (Ch2):..... M7D02 (SA561
Sync: T0
Horiz: ..... 0.2 μs/div
Vert (Ch1): ..... 20 mV/div
Vert (Ch2): ..... 20 mV/div (Inv)
Mode: ..... Add (differential scope cable)

This is a typical sense line wave form of a one bit in a single address. The arrow points to the write noise coupled from other sense lines that are inhibiting bits. The data used is /FFFF.

Ⓑ



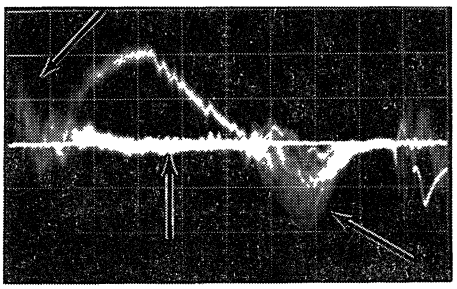
Same scope setup as Ⓐ .

This is a typical sense line wave form of all zero bits in a single address. It is the same sense line that is viewed in Ⓐ while sensing a one bit. This wave form illustrates the importance of strobe timing to ensure the noise present (see arrow) is not mistaken for a bit.

28096

Figure 1-38. Sense Line Waveform for Single-Address Operation (2 μs Storage)

Ⓐ

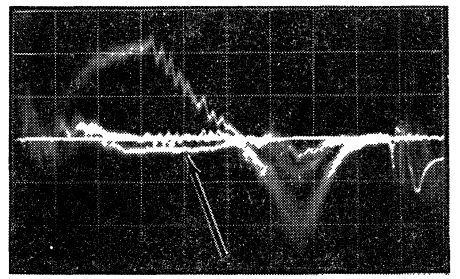


Signal (Ch 1): ... M7B02 (SA561)
Signal (Ch 2): ... M7D02 (SA561)
Sync: ... T0
Horiz: ... 0.1 μs/div
Vert (Ch 1): ... 20 mV/div
Vert (Ch 2): ... 20 mV/div (Inv)
Mode: ... Add (differential scope cable)

This is a typical read envelope while running core adjust program. Note that single polarity signals exist. Center arrow points to zero signals. Bright center trace results from another 4k increment being addressed. Left arrow shows decay of X, Y, and Z noise. The delta* noise above center arrow should decay to less than 7 mV at strobe time. Right arrow shows normal read-turn-off noise.

* Delta noise is signal on sense line from half selected cores (cores with either X or Y drive current but not both).

Ⓑ



Same scope setup as Ⓐ .

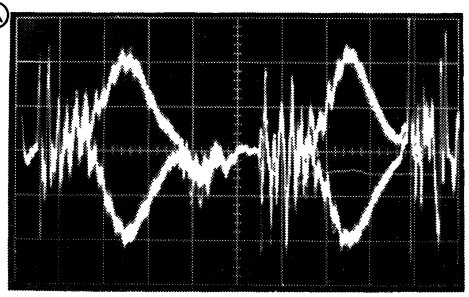
The discrete trace away from the center line in this photo is caused by magnetostrictive ringing. This condition is normal in 2 μs storage units and usually can be seen only while running the core storage adjust programs. This condition is associated with worst-case data patterns as in the storage adjust programs. The ringing can cause a bit picking and/or dropping problem. The symptoms would generally be high temperature associated failures and failures that follow a cycle having extended T-7 times. The condition can be aggravated by improper current balance (read > write). If magnetostrictive ringing is causing a problem and current balance is correct, try replacing the associated sense amp. Under severe conditions replace the storage unit.

28098

Figure 1-39. Sense Line Waveforms with Core Adjust Program (2 μs Storage)

Normal

Ⓐ



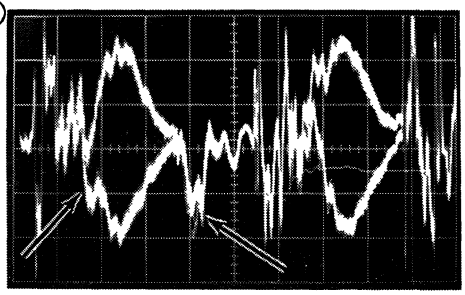
Signal (Ch 1): ... M7B02 (SA561)
Signal (Ch 2): ... M7D02 (SA561)
Sync: ... T0
Horiz: ... 0.2 μs/div
Vert (Ch 1): ... 20 mV/div
Vert (Ch 2): ... 20 mV/div (Inv)
Mode: ... Add (differential scope cable)

Program: Address Data
/0000 to /007E = /1002
/007F = /6000

This is a typical wave form for the bit-14 sense line while running the program given above (X00 address).

With Leakage

Ⓑ



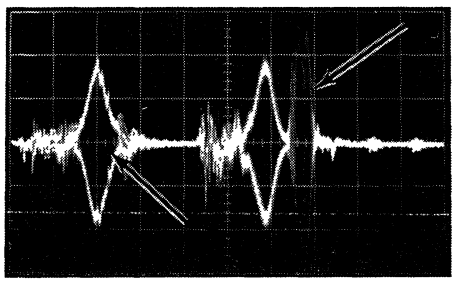
Same scope setup as Ⓐ

This is the bit-14 sense line viewed while running the program given in Ⓐ. Note the distortion in this picture as compared with Ⓐ. This distortion is caused by bottom board leakage.

28099

Figure 1-40. Effect of Bottom Board Leakage on Sense Line Waveform (2 μs Storage)

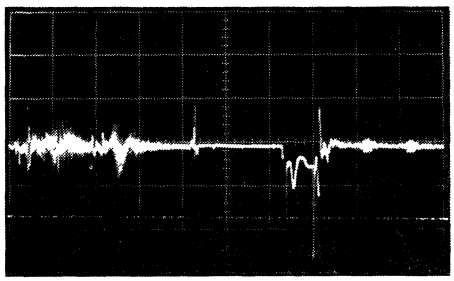
Ⓐ



Signal (Ch 1): M7B02 (SD781)
Signal (Ch 2): M7D02 (SD781)
Sync: T0
Horiz: .... 0.5 μs/div
Vert (Ch 1): .... 20 mV/div
Vert (Ch 2): .... 20 mV/div (Inv)
Mode: .... Add (differential scope cable)

This is a typical sense line wave form for all ones in <4k or >4k addresses. Absence or center trace (left-most arrow) during signal indicates that this is the only 4k segment of storage selected and all signals are ones. Right-most arrow points to write turn-off noise and inhibit turn-off noise from other lines. The amount of noise can vary depending on data.

Ⓑ



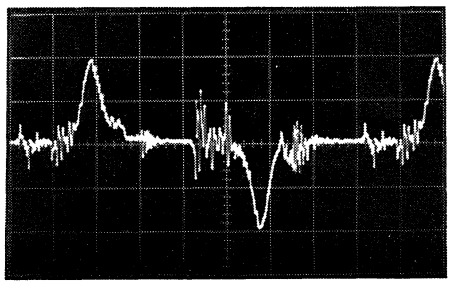
Same scope setup as Ⓐ

This is a typical sense line wave form for all zeros in <4k or >4k addresses. The strobe time is approximately 900 ns from left edge of scope face. Inhibit transients are shown in last half of trace.

28101

Figure 1-41. Sense Line Waveforms with Multi-Address Operation (4 μs Storage)

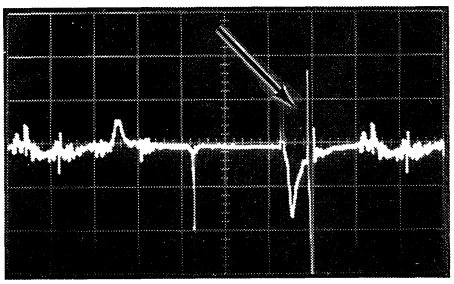
Ⓐ



Signal (Ch 1): .. M7B02 (SD781)
Signal (Ch 2): .. M7D02 (SD781)
Sync: .. T0
Horiz: .. 0.5 μs/div
Vert (Ch 1): .. 20 mV/div
Vert (Ch 2): .. 20 mV/div (Inv.)
Mode: .. Add (differential scope cable)

This is a normal wave form for reading and writing a one bit in a signal address. Compare to Ⓑ which shows same sense line while sensing a zero bit.

Ⓑ



Same scope setup as Ⓐ .

This is a normal wave form for reading and writing a zero bit in single address. Strobe time would be approximately 900 ns from left edge of trace. Arrow points to large Z turn-off transient.

28095

Figure 1-42. Sense Line Waveform with Single-Address Operation (4 μs Storage)

12. Picks and Drops Bits

a. Defective diode. (See item 2.)
b. Leakage from drive line (item 8).

1.7.8 Core Storage Waveforms

Typical timings for the 2- and 4-microsecond storage units are shown on ALD pages SA031 and SD031 respectively.

Actual photos of core storage waveforms are shown in Figures 1–33 through 1–45. Waveforms are shown for both correct and incorrect core storage conditions.

When scoping core storage, ground the scope shield at the probe tip. See 1.7.4 for core storage scoping techniques.

1.7.9 Current Measurement

Core storage current measurements are made only at the array connector block as described on system diagram SA031 or SD031. The appropriate array connector block must be replaced by the current probing card (2.13.4) for use with the oscilloscope current probe. Use the jumper block removal tool (P/N 2108860) to remove the array connector block.

Power down the system while exchanging connector blocks and current probing cards. If it is necessary to remove any minibus plugs, they should be carefully replaced prior to powering up the system for measurement.

Current drive cards are factory balanced and should be replaced if current balance is incorrect, provided that no lines through the array are shorted, grounded, or otherwise defective.

1.8 PROCESS INPUT/OUTPUT

1.8.1 Analog Input

Troubleshooting Techniques

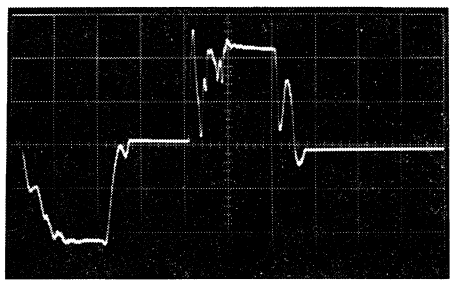
Control Parity Errors: A control-parity error activates the 'parity reset' line. 'Parity reset' resets the AI basic circuitry, thus concealing many of the conditions that existed at the time of the control-parity error. As a troubleshooting aid, 'parity reset' can be prevented by applying a ground jumper to A–B2J6B07 (QD241). Do not disable the 'parity reset' line while the customer is using AI, as program hang-ups can result.

Mode of Operation: Determine which modes of operation fail (direct program control, data channel random, etc.). Use the simplest mode for troubleshooting.

Programming Violations: Check for possible programming violations as described in 1.8.5.

Reducing Secondary Effects: It is sometimes helpful to ground a logic point or alter a program to prevent a complete sequence of events from taking place. This procedure reduces the secondary effects of a problem, making the problem easier to solve. For example, if an 'XIO read' instruction fails to reset the 'DPC solid state busy' flip-flop, the failure will not be noticed until the next 'XIO write' operation is rejected because of the busy condition. The failure to reset the busy condition would erroneously show up as

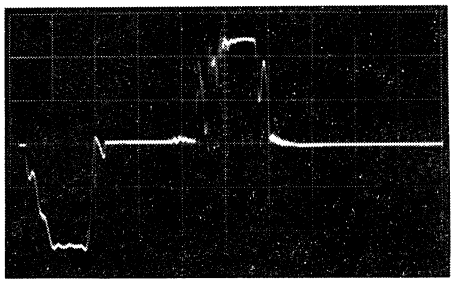
Ⓐ



Signal: J6B02 (SD561)
Sync: T0
Horiz: ..... 0.5 μs/div
Vert: ..... 100 mA/div (current probe)

This photo shows a typical X drive current wave form. Note long rise time of read drive, and chopped up rise time of write portion. The equivalent voltage signal is available at M2B09.

Ⓑ



Signal: K5B04 (SD471)
Sync: T0
Horiz: .....0.5 μs/div
Vert: .....100 mA/div (current probe)

This photo shows a typical Y drive current wave form. Note similarity to wave form Ⓐ . Differences are later turn on and shorter duration. The equivalent voltage signal is available at B2B09.

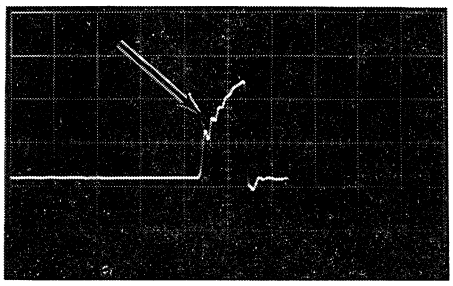
28094

Figure 1-43. X and Y Drive Current Waveforms (4 μs Storage)

Ⓐ

+3V

0V



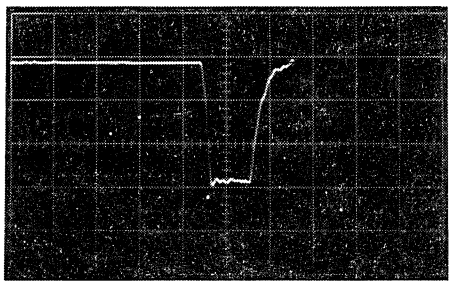
Signal: M7B07 (SD781)
Sync: T0
Horiz: ..... 0.1 μs/div
Vert: 1V/div

This is a typical strobe pulse at input to sense amp. This pulse is extremely important as it gates the sense line signal to the sense amp when there is maximum read signal and minimum noise present. The arrow points to portion of pulse that has varying shape depending on data that is read out.

Ⓑ

+3V

0V



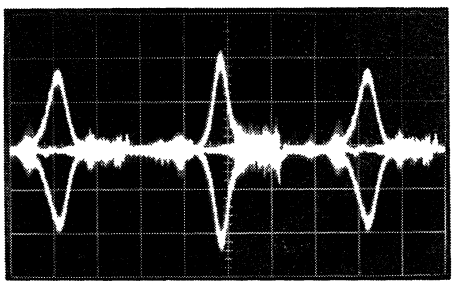
Signal: M7B04 (SD781)
Sync: T0
Horiz: ..... 0.1 usec/div
Vert: 1V/div

This is a typical sense amp output wave form indicating a bit has been read from corresponding sense line. Note saturated down-level.

28089

Figure 1-44. Sense Amp Waveforms (4 μs Storage)

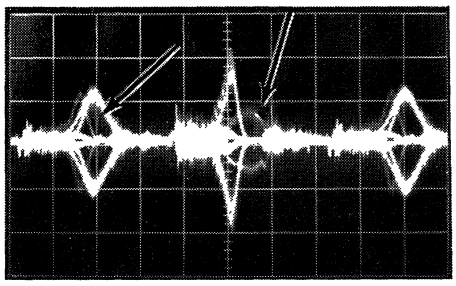
Ⓐ



Signal (Ch 1): ... M7B02 (SD781)
Signal (Ch 2): ... M7D02 (SD781)
Sync: ... T0
Horiz: ... 0.5 μs/div
Vert (Ch 1): ... 20 mV/div
Vert (Ch 2): ... 20 mV/div (Inv)
Mode: ... Add (differential scope cable)

This is a normal sense-line read and write wave form. Note that read signals are smaller than write signals. Compare with Ⓑ which is the same except for shorted diode.

Ⓑ



Same scope setup as Ⓐ .

This is a typical sense-line wave form with shorted diodes. The characteristics of multiple read and write envelopes is obvious. Compare to correct wave form as shown in Ⓐ .

28093

Figure 1-45. Effect of Shorted Diodes on Sense Line Waveforms (4 μs Storage)

a failure to accomplish an 'XIO write'. If the sequence was halted after each 'XIO read', the real cause of the problem would be more easily seen because the 'DPC solid state busy' indicator, which should be reset, would be left on.

Do not overlook the selective data trapping capabilities of the I/O monitor unit for such problems.

ADC Conversion Sequence

Regardless of the mode of operation, the following sequence occurs for every ADC conversion and can be quickly checked for possible failure.

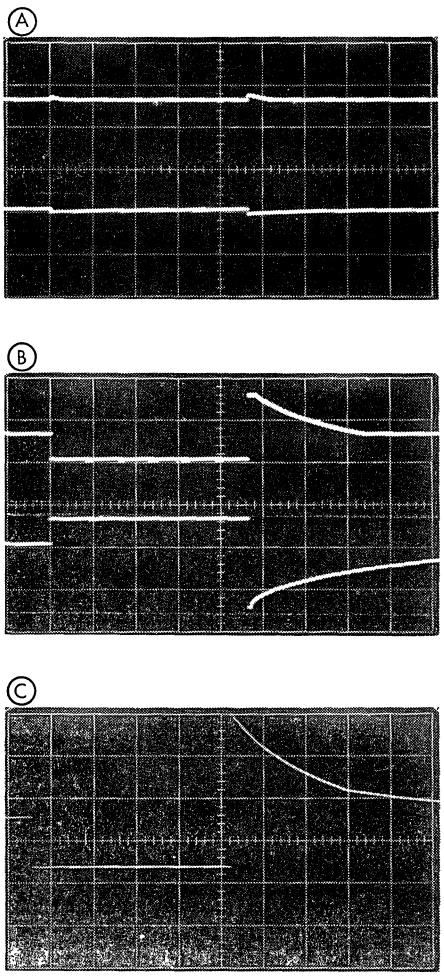
1. Load analog multiplexer address register (AMAR) and set 'AMAR busy' flip-flop to indicate that AMAR has been loaded (QD261, QD471, QD481, and QD491).
2. Get through either the solid-state or the relay interlock (QD261).
3. Load the solid-state or relay X and Y drivers and turn off the 'AMAR busy' flip-flop (QD261, QD601, and QD741).
4. Fire either the solid-state or relay multiplexer start-delay singleshots (QD271).
5. Perform the ADC conversion (QD821).
6. Receive the 'ADC end of convert' signal (QD821).
7. Reset the X and Y drivers. On Mod 2 ADC's, the solid-state drivers are reset at the start of the conversion (QD601, QD741).
8. Fire the multiplexer end-delay singleshot for relay or for solid-state (SS delay B). There is no solid-state end delay period with Mod 2 ADC's (QD271, QD930).
9. Request service by setting the conversion-complete flip-flop if in DPC mode, or request a cycle steal if in a data-channel mode (QD231, QD361).

Read All Bits —— Service Hint

To read all bits from the ADC, remove the connector from pin A–A1A1C11 on the ADC logic board. This connector brings the output of the ADC comparator to the ADC register reset circuits. When it is disconnected, the sign trigger cannot be set and no other trigger in the ADC register can be reset. This results in a positive overload. Tie down the overload bit by grounding A–A1D2B12; the maximum positive reading will then be obtained in the ADC reg. This procedure is helpful in troubleshooting many ADC problems; it is also helpful in troubleshooting data parity errors because it provides a constant ADC value which can be followed through the parity assignment circuits and into the processor-controller B-reg via the I/O in bus (QD891).

1.8.2 Analog Input Waveforms

Figures 1–46 through 1–54 show photos of various analog input waveforms. Oscilloscope setup information is given with each figure.



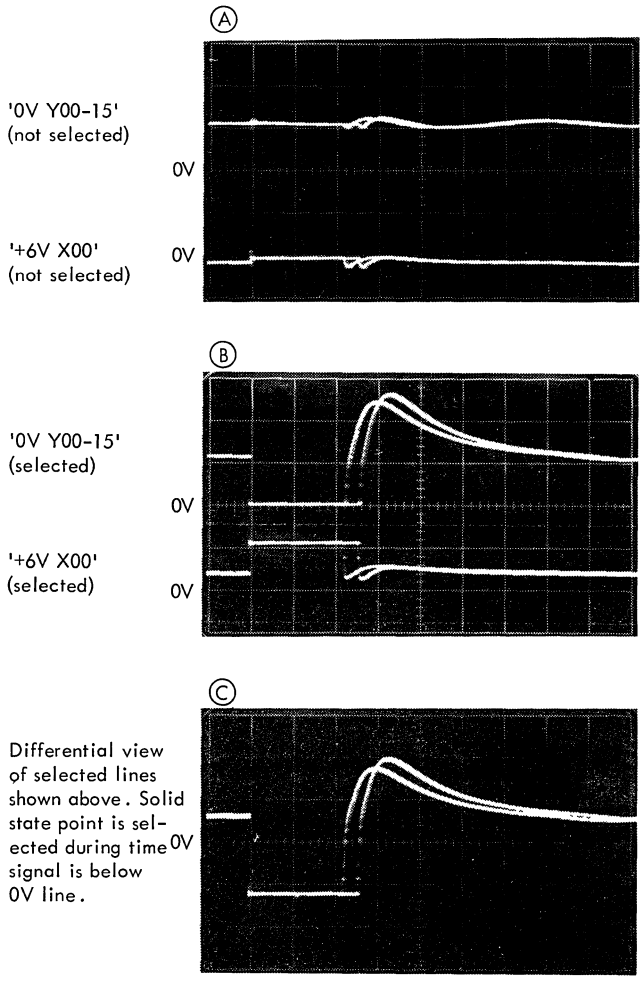
Setup:

Signal (ch 1):	A-A2B6B09 (QD631)
Signal (ch 2):	A-A2B7B08 (QD601)
Sync:	Int (delayed sweep was used to allow viewing of leading edge of wave form)
Horiz:	2 ms/div
Vert (ch 1):	20V/div
Vert (ch 2):	20V/div (inv for wave form Ⓒ)
Mode:	Chopped (add for wave form Ⓒ)

These photos show the X and Y drive lines for a relay multiplex point. Note that the inductive spike from the relay coil is clamped to ± 30V by diodes. X and Y must be selected to pick the relay.

28109A

Figure 1-46. Relay Multiplex Point Selection



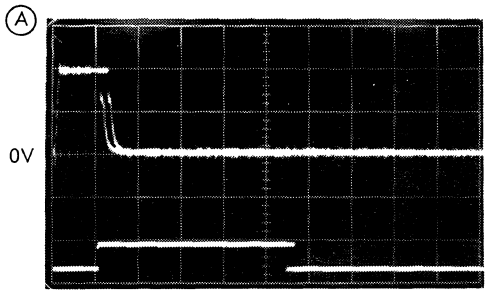
Setup:

Signal (ch 1):	A-A2J6B09 (QD771)
Signal (ch 2):	A-A2J7B08 (QD741)
Sync:	A-B2F3B02 (Write Function)
Horiz:	5 μs/div
Vert (ch 1):	5V/div
Vert (ch 2):	5V/div (inv for wave form Ⓒ)
Mode:	Alternate (add for wave form Ⓒ)

These photos show the X and Y drive lines for a solid-state multiplex point. The double traces are due to the free-running ADC clock. X and Y must be selected to select a solid-state input point.

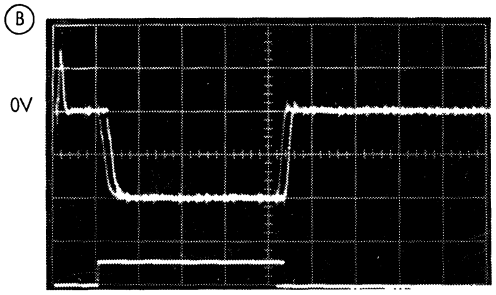
28110A

Figure 1-47. Solid-State Multiplex Point Selection

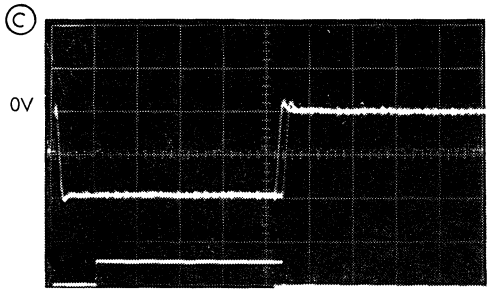


Signal (ch 1): Sample and hold (S & H) amp input A-A1A3G07 or G08 (QD940 or QD891)
Signal (ch 2): Conversion time A-A1E5D09 (QD821)

This photo illustrates S & H amp operation. Input voltage is not present during conversion time.



Signal (ch 1): S & H amp test point A-A1A3P04 (QD891)
Signal (ch 2): Same as (A)



Signal Ch 1: S & H amp output A-A1A3J12 (QD891)
Signal Ch 2: Same as (A)

This photo illustrates the S & H amp inversion and ability to hold input voltage. Compare with photo (A).

Setup: DPC sampling of + 2V on solid-state input point (mod 2 ADC)

Sync: +, A-B2L7D10 '+ amp or Solid-state Delay' (QD271)
Horiz: 10 µs/div
Vert (ch 1): 1V/div (upper trace)
Vert (ch 2): 5V/div (lower trace)
Mode: Alternate

28102A

Figure 1-48. Sample-and-Hold Amplifier Waveforms

1.8.3 Multiplexer Troubleshooting Techniques

Verifying AMAR

Use the I/O monitor (2.11.1) to verify that given addresses are being loaded into AMAR, and that AMAR is being incremented following each load. The increment AMAR signal occurs after the load X and Y drivers signal and is a good indication that the load drivers signal did occur.

If the system has the comparator special feature, AMAR can also be checked by programming to force an out-of-limits condition in the data-channel-random mode of operation. The comparator DSW, on an out-of-limits condition, contains the multiplexer address of the point that was out of limits.

Multiple Selections

Multiple selections cause many difficult-to-analyze failure patterns. For example, if a Y driver is shorted, the group using the shorted driver will work properly and all other groups will have erroneous readings. If an X driver is shorted, the points using the shorted driver will work properly and other points will have erroneous readings.

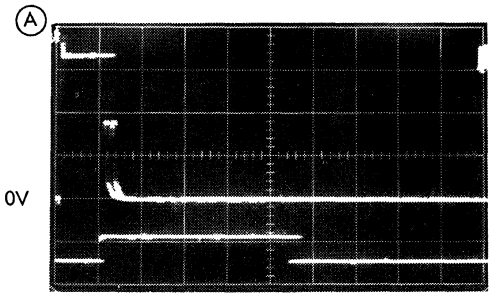
If multiple selections are suspected, they may be confirmed by removing all but the selected X and Y driver cards in the A–A2 panel or removing all but the selected multiplex card in the 1851. It may also be helpful to remove all coaxial cables from the analog-in bus except the one being used by the selected point.

Scoping Drivers

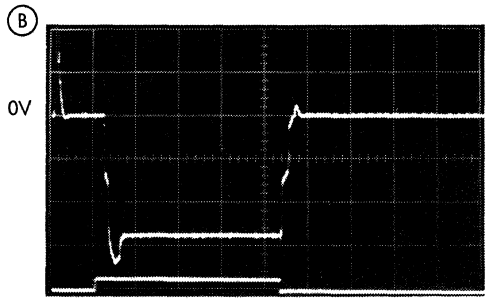
Scope the X and Y drivers. See Figures 1–46 and 1–47. Be aware that the solid-state multiplexer and amplifier-block-switch drivers are reset near the start of the ADC conversion in a Mod 2 ADC, and at the end of the conversion in a Mod 1 ADC. The relay drivers are always reset at the end of the conversion.

Open Relay or Pulse Transformer

If an open relay coil or solid-state pulse transformer is suspected, the X and Y drivers should be checked for cor-

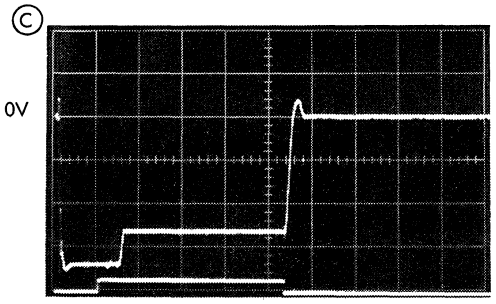


Signal (ch 1): S & H amp input A-A1A3G07 or G08 (QD940 or QD891)
Signal (ch 2): Conversion time A-A1E5D09 (QD821)



Signal (ch 1): S & H amp test point A-A1A3P04 (QD891)
Signal (Ch 2): Same as (A)

This photo illustrates S & H amp operation with an overload condition.



Signal (ch 1): S & H amp output A-A1A3J12 (QD891)
Signal (ch 2): Same as (A)

Setup: DPC sampling of 7V overload on solid state input point Mod 2 ADC
Sync: +, A-B2L7D10 '+ Amp or Solid State Delay' QD271
Horiz: 10 µs/div
Vert (ch 1): 2V/div (upper trace)
Vert (ch 2): 10V/div (lower trace)
Mode: Alternate

28103A

Figure 1-49. Sample-and-Hold Amplifier Waveforms with Overload

rect operation. A 300 ohm to 2k ohm resistor may be connected between the X and Y driver outputs to determine that the drivers are operating correctly by providing a resistive load which develops a clean waveform for scoping. This resistor can then be moved back to the 1851 end of the cable to check for opens in the X-Y driver path. When available, a current probe is useful in troubleshooting X or Y driver problems or open circuit problems. No current indicates a bad driver or open circuit.

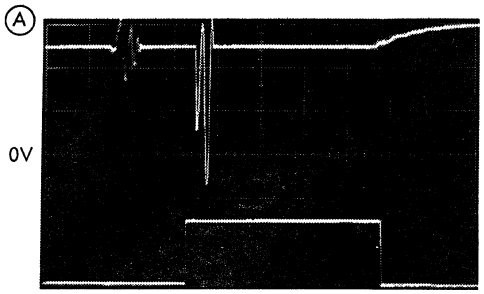
Current Limiter

In the multiplexer, the voltage to the X drivers is provided by a current limiter. The main functions of the limiter is to restrict the current to the X drivers under a fault condition. The solid-state multiplexer, because of back circuits, will operate marginally even if the current limiter card is removed. An X-driver output pulse of 5.2 to 6 volts indicates a properly operating current limiter card. If the X-driver pulse is not within these limits, the current limiter card should be replaced.

Block Switch

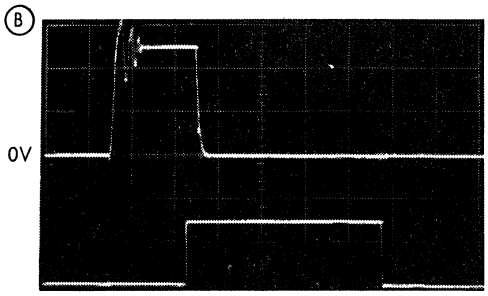
The function of the block switch is to reduce leakage paths between groups of input points. Each group of 16 input points contains four multiplexer cards. The first card in each group contains the block switch. The card containing the block switch has five relays or five transformers (solid state); the other three cards each have four relays or transformers.

If trouble is suspected in the block switch area, the block switch card can be swapped with another card in the group to help isolate the problem. When a multiplexer card not having a block switch is used in place of a card with a block switch, the block switch points are bypassed. The system will perform satisfactorily in this configuration on a temporary basis, but care should be taken to ensure that the proper filter elements are present for each customer input point. For emergency repairs, block-switch cards and non-block-switch cards may be interchanged until the correct part is available.



Signal (Ch 1): Relay 1851 input to amp block switch, upper pin N (QC400)
Signal (Ch 2): Conversion time (lower trace) A-A1E5D09 (QD821)

This photo shows transients at amp block switch select and deselect times and the signal beginning to float when the relay block switch is opened.



Signal (Ch 1): Relay 1851 output of amp block switch, upper pin S (QC400)
Signal (Ch 2): Same as (A)

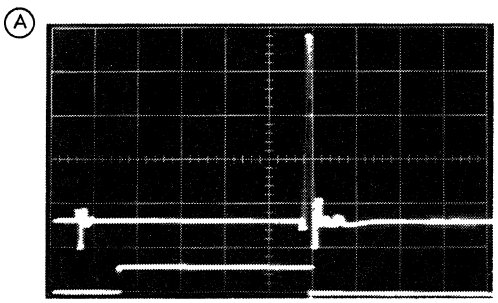
This photo shows the multiplexed input voltage as applied to a Mod 2 ADC.

Setup: Program in DPC mode sampling + 9 mV applied to a 10 mV input point on a Mod 2 ADC.

Sync:	+, A-B2D7D04 start of overlap delay (QD271)
Horiz:	50 µs/div and 10 µs/div using delayed sweep
Vert (Ch 1):	2V/div
Vert (Ch 2):	2V/div
Mode:	Alternate

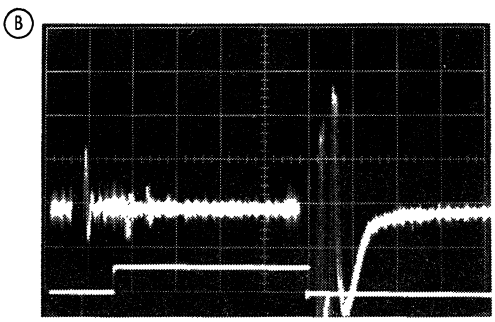
28107

Figure 1-50. Amplifier Block Switch Input and Output



Vert (ch 1): 0.5V/div
Signal (ch 1): Buffer amp output A-A1A2D02 (QD891)
Signal (ch 2): Conversion time A-A1E5D09 (QD821)

This photo illustrates large overshooting at multiplex select and deselect time.



Vert (ch 1): 20 mV/div
Signal (ch 1): Buffer amp output A-A1A2D02 (QD891)
Signal (ch 2): Same as (A)

This photo shows the input voltage as seen by the ADC during the conversion. Note the noise level.

Setup:	DPC sampling of short on solid-state input points.
Sync:	+, A-B2C3D12 function write (QD221)
Horiz:	50 µs/div and 10 µs/div using delayed sweep
Vert (ch 1):	Stated with photo (upper trace)
Vert (ch 2):	5.0V/div (lower trace)
Mode:	Alternate

28104A

Figure 1-51. Input to ADC

Failure Area

To locate the failure area, insert shorts one at a time at various points in the analog path. Refer to system diagram QC050 for test points and additional information. Disconnect the customer voltage from the input point being tested before the shorts are applied. This procedure is helpful in troubleshooting cable and connector failures.

A 1.5V dry cell provides a floating voltage source that can be quickly applied to a high-level input point to locate a failure if the shorted input fails to indicate the problem. By removing the shorting switch drive card (A–A1B4, QD826), the multiplex circuitry can be bypassed and the voltage applied directly to the ADC input.

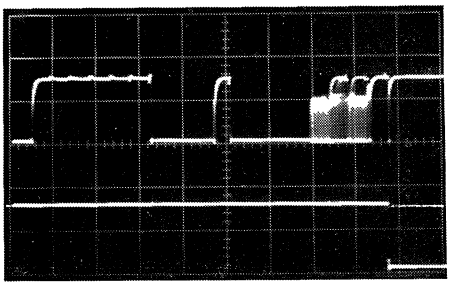
1.8.4 1851 Service Voltages

DC voltages for multiplexer components are supplied via a flat power cable from the A–B2 board in the 1801, 1802, or 1826 model 1. These voltages are listed in Figure 1–55 and are measured with a Weston 901 meter (0.5% accuracy) or equivalent. See 5.5 to determine power supplies used.

1.8.5 Programming Rules and Restrictions

Many difficult-to-analyze AI problems are caused by programming errors. Understanding the following limitations and rules of AI programming should precede an attempt to diagnose an AI problem.

1. An 'XIO read' or an 'XIO blast reset' instruction must be executed for every 'XIO write' instruction given. Failure to do this will result in the 'relay conversion' flip-flop remaining on for direct program control (DPC) relay operations, or the 'DPC solid state busy' flip-flop remaining on for solid-state operations.
2. An 'XIO sense device' instruction with reset must be executed, following every interrupt request, to reset the interrupting condition.
3. To obtain the best analog performance, a single relay address should be sampled no more than three times per second.
4. An 'XIO read' performed during an analog-digital conversion may result in a data parity error. The ADC data word is stored in memory regardless of whether the parity is good.
5. If an 'XIO initialize read' is given while either the 'AMAR busy' or 'DPC solid state busy' is on, the 'initialize read' instruction will be ignored with no error indicators set.
6. If an 'XIO write' instruction is given when either 'cycle steal busy' or 'DPC solid state busy' is on, the 'XIO write' will be ignored with no error indication other than a missing interrupt because of the failure to perform the write.
7. When a program attempts to store an ADC value into a storage-protected memory location, a 'storage protect violation' interrupt will occur in analog input basic. A meaningless data parity error in analog input basic may also occur.
8. In overlap operation, having a relay point selected inhibits a solid-state operation from changing the

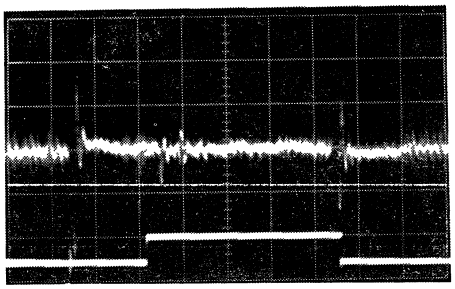


Signal (ch 1): Error amp output A-A1B5J07 (QD881)
Signal (ch 2): Conversion time (lower trace) A-A1E5D09 (QD821)
Sync: +, A-A1C6B04 ADC clock A0 (QD841)
Horiz: 5 µs/div
Vert (ch 1): 2V/div
Vert (ch 2): 2V/div

This photo shows a typical ADC conversion. For this conversion ADC Reg bits S, 8192, 4096, 2048, and 128 remained on; bits 1024, 512, 256, 64, 32, 16, and 8 were reset off; and bits 4, 2, and 1 were indecisive, resulting in a repeatability of three digits. A DPC conversion of + 0.586V, applied to a solid-state input point with a Mod 2 ADC, was used.

28108A

Figure 1-52. Typical ADC Conversion

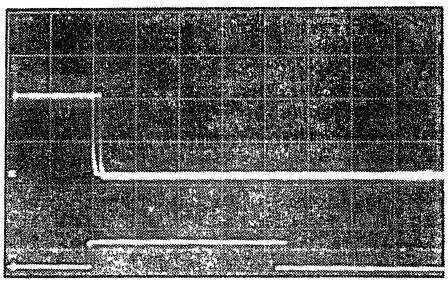


Signal (Ch 1): Buffer amp output (upper trace) A-A1A2D02 (QD891)
Signal (Ch 2): Conversion time A1E5D09 (QD821)
Sync: +, A-B2L7D10, start of amp block switch delay (QD271)
Horiz: 10 µs/div
Vert (Ch 1): 20 mV/div
Vert (Ch 2): 5V/div
Mode: Alternate

This photo shows multiplex switching transients and typical noise level with a short on the input of a 10 mV differential amp. Wave forms are from a Mod 1 ADC in DPC mode.

28106

Figure 1-53. ADC Input with Shorted Differential Amplifier Input



Signal (Ch 1):	Calibrate point X drive (upper trace) A-A2F7D07 (QD741)
Signal (Ch 2):	Conversion time (lower trace) A-A1E5D09 (QD821)
Sync:	+, A-B2G5B04 AMAR busy (QD261)
Horiz:	10 μs/div
Vert (Ch 1):	5V/div
Vert (Ch 2):	5V/div
Mode:	Alternate

This photo shows the X drive wave form while addressing CE calibrate address in DPC mode with a Mod 2 ADC.

28105

Figure 1-54. X-Drive for CE Calibrate Point

ADC resolution. The resolution can be changed after the relay conversion is complete, or if the solid-state operation is initiated during the 'relay end delay' period.

9. In relay external-sync mode, the relay operation is performed as usual up to the time of the 'amplifier block switch delay' (18 μs singleshot). At this time a 'ready' signal is sent to the customer's device. When the customer's device 'sync start' pulse is returned, the operation proceeds to completion. However, it must be realized that the value that is converted is the value that was saved in the flying capacitor at the beginning of the relay multiplexer operation. The 'sync start' pulse must be returned within 330 milliseconds to assure no more than 0.01% error due to capacitor discharge.
10. The last point of a data table must not be a relay point if one is using random data channel mode with the overlap special feature installed. The last data table entry being a relay point will prevent proper completion of the data channel cycle-steal operation.

Voltage	Limits	Measure
+6	+5.5 to +5.9	L02H to L02F
+12	+11.4 to +12.6	L02J to L02F
+30	+28.5 to +31.5	L02R to L02F
-30	-28.5 to -31.5	L02P to L02F

14083C

Figure 1-55. 1851 Service Voltages

1.8.6 Analog Input Repeatability

Repeatability is the ability to consistently repeat a value of digital output for several conversions of a fixed analog input. AI diagnostic programs provide repeatability and accuracy measurements (Figure 1–56).

There are three general areas that can cause repeatability problems: the ADC, the multiplexer, and the input source.

Single Point: If only a single point has repeatability problems, the ADC and multiplexer are usually functioning properly. The cause of the problem is either the individual multiplexer point or the input source. The easiest way to determine the cause is to replace the multiplexer card in the failing circuit. If replacing the multiplexer card does not eliminate the problem, the trouble is probably associated with the input source.

If the input source is suspected of being in error, the calibration source or a short can be applied to the input terminals of the failing circuit to confirm correct operation of the analog input path. The input source can cause repeatability problems if there is a high level of noise or ac common-mode voltage present.

Note: Common-mode voltage and AI repeatability and accuracy specifications are described in the *IBM 1800 Data Acquisition and Control System Installation Manual – Physical Planning* (see *FE Bibliography, 1800 System,* Order No. SY26-0560).

In all such cases, the customer should be consulted, as the failure area is not within the customer engineer's responsibility.

The main cause for repeatability problems on solid-state inputs is the voltage source. The most common type of input is an amplifier whose purpose is to provide isolation and signal gain. A limitation with most amplifiers is that they cannot be multiplexed. The multiplexing operation creates transient loading of the amplifier, thus causing the amplifier to become unstable and not settle out in time for the ADC conversion. This type of problem can be corrected by obtaining amplifiers (customer requirement) that meet the specifications covered in the 1800 system physical planning manual.

All Input Points: If all or many of the analog input points fail to meet repeatability specifications, the trouble is usually in the ADC or multiplexer units. Noise induced on the system ground wire causes repeatability problems; refer to the 1800 physical planning manual for proper grounding procedures.

Determine if the ADC is functioning properly. With the input cable removed and the input shorted, check the performance for zero input. With the short removed and the calibration cable attached to the ADC input, check the operation with the plus and minus calibration supply voltages.

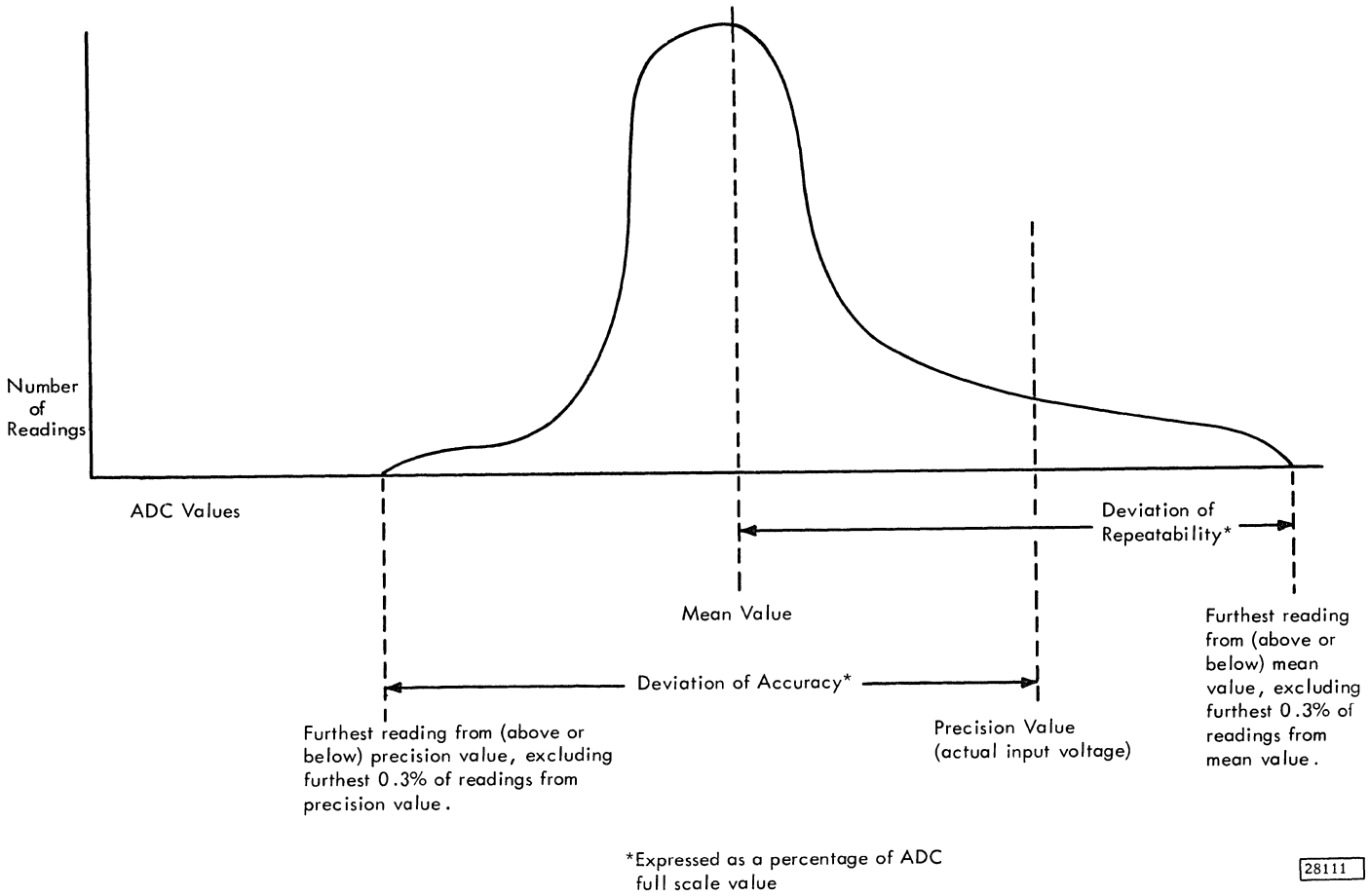


Figure 1-56. AI Repeatability and Accuracy

If the ADC fails to operate properly with the input shorted, short the output of the buffer (or sample-and-hold) amplifier. This test, with the input and output of the amplifier shorted, eliminates the amplifier, and the ADC should operate with a repeatability of approximately two digits. This procedure of shorting the input and, if necessary, both the input and output of the buffer or sample and hold amplifier, should isolate the problem area. If the problem is associated with the amplifier or ADC, a complete readjustment (4.14.3) should be attempted before troubleshooting begins.

Multiplexer problems can be diagnosed only after it is determined that the ADC is functioning properly. For multiplexer troubleshooting techniques, see 1.8.3.

1.8.7 Analog Output

Analog output service information is given on system diagram TA002.

1.9 DATA PROCESSING INPUT/OUTPUT

1.9.1 DP I/O Trouble Diagnosis

For locating DP I/O failures, the I/O monitor unit can be used in conjunction with customer programs, diagnostic function tests, or auxiliary exerciser programs for all but the 1816, 1053, and 1627 units. Some functions of the 1816, 1053, and 1627 units can be tested with the I/O monitor unit by using the channel interface.

If the trouble is traced to a DP I/O unit, refer to the FE maintenance manual for that unit to find the correct diagnostic procedure. The 1053/1816 and 2401/2402 can be operated off-line with external service aids (testers).

1.9.2 1442 Card Read Punch

Power-Down Procedure

All cards should be run out of the card read punch before removing power. Removing power from the card read punch when the card punch is loaded with cards results in lacing of a card column.

Chapter 2. Console and Maintenance Features

2.1 PROGRAMMER'S CONSOLE

The programmer's console (Figure 2-1) provides the means for manual control of the processor-controller during troubleshooting or operating phases.

The basic operating features and controls provide the facility to:

1. Start or stop instruction execution.
2. Set up and store data or instructions.
3. Communicate with the program via sense and program switches.
4. Indicate machine conditions and status.
5. Display core storage words and register data.
6. Write or clear storage-protect bits.
7. Initial program load.
8. Trace each instruction.
9. Interrupt the program manually.
10. Control the cycling rate by the run, single-storage-cycle, single-instruction, or single-step mode.
11. Clear core storage.
12. Reset all control circuitry.
13. Turn power on and off.

2.1.1 Switches and Message Lamps

There are two rows of pushbutton switches and message lamps. One row is at the top of the console and one row is at the bottom.

Clear Storage

This pushbutton switch has four functions (Figure 2-2). However, none of the four functions can be executed until CLEAR STORAGE (CA151) is held pressed, then START is pressed. This dual action requirement prevents the accidental clearing of storage. Note in Figure 2-2 that each clear-storage function is dependent on the positions of the mode switch and the write-storage-protect-bits switch.

The P-C continuously cycles through all core storage addresses during the clear-storage operation.

Program Load

This pushbutton switch (CA151) is used to load an IPL card (1442) or IPL tape record (1054) into main or auxiliary storage. The IPL card or tape record must contain instructions that will load the remaining cards or tape records, unless the entire program is contained in the IPL card or tape record. (See paragraph 2.2, "Initial Program Load.")

Ready

When on, this lamp (YA141) indicates that power is supplied to all P-C circuits and that the P-C is ready to operate. This lamp does not indicate the ready status of individual DP I/O units.

On

This pushbutton switch (YA140) is used to power-up the 1800 system. Pressing the on button starts the power-on sequence (1.7 seconds to ready condition) and generates a power-on reset signal.

Off

This pushbutton switch (YA140) is used to power-down the 1800 system. Presssing the off button drops all power in the system with the exception of the 115-Vac convenience outlets, the 24-Vac sequencing voltage, and line voltage at the 1053 Printer and 1816 Printer-Keyboard, which have their own power cords.

Power On

This lamp (YA141) is turned on when the on button is pressed. The lamp remains on to indicate that power is delivered to the P-C power supplies and blowers, and to external units that receive their power from the P-C.

Lamp Test

This pushbutton switch (CA151) is pressed to test the operation of all SCRID-actuated lamps (the small, round indicator lamps on the console).

Wait

When on, this lamp (CA151) indicates that the P-C is in either load or display mode, or that it has been halted by a 'wait' instruction.

Run

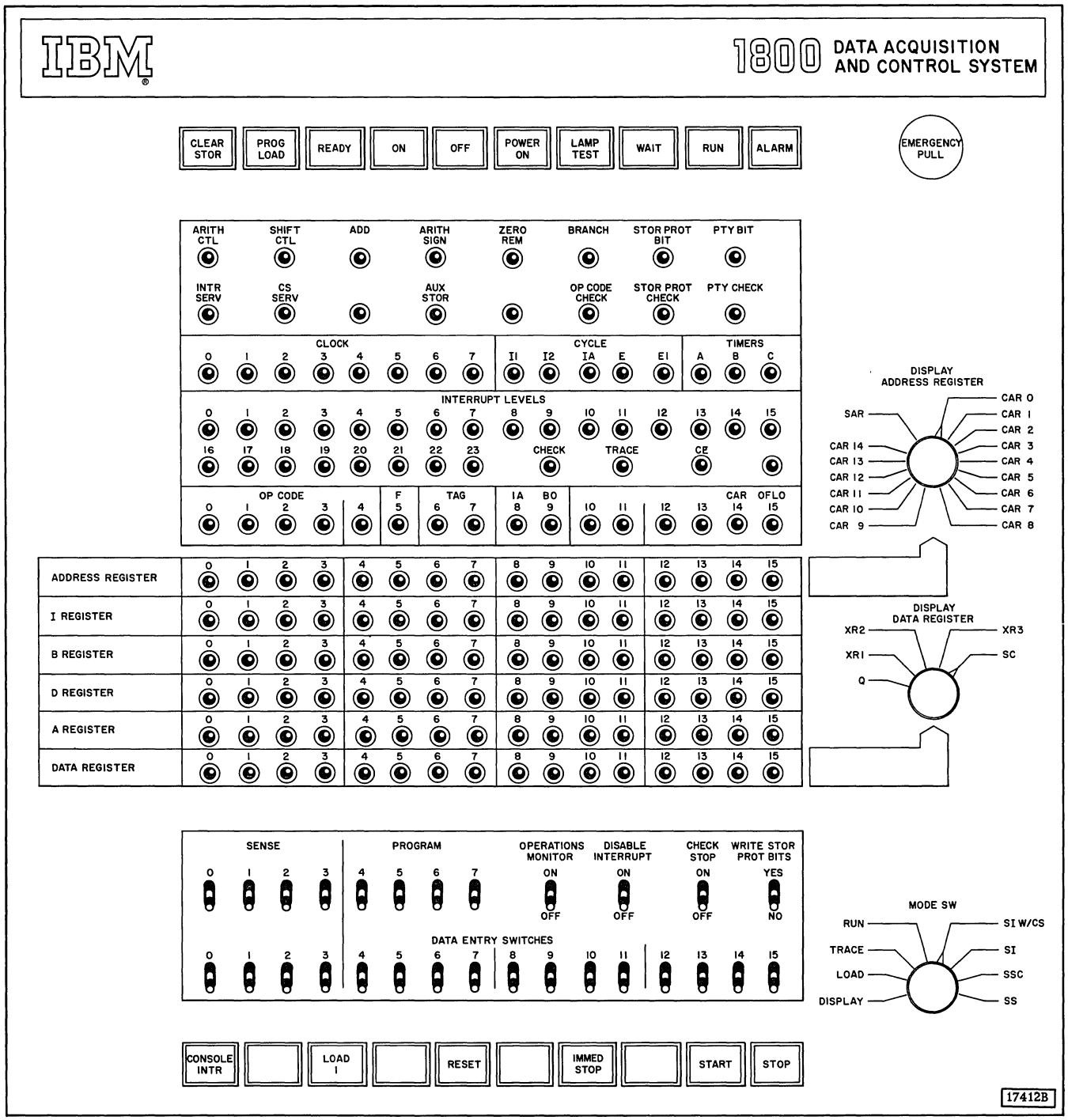
When on, this lamp (CA151) indicates that the P-C is operating under program control.

Alarm

This lamp (YA141) turns on to indicate that the operations monitor preselected time interval has expired. The lamp remains on until the operations-monitor switch is turned off.

Emergency Pull

This switch (YA140) is for emergency use only. If pulled off, all electrical power (except 24-Vac sequencing voltage) is immediately removed from all system units except the 1053 Printer and 1816 Printer-Keyboard, which have their own power cords.



● Figure 2-1. Programmer's Console

Function	Mode Switch	WSPB Switch
1. Store Contents of Data Entry Switches in all Core Storage Locations. Storage-Protect Bits are Removed and Parity is Corrected as Required Because of Bit Removal. If All Data Entry Switches Are Off, Only Parity Bits are Left in Storage.	Run	Yes
2. Store Contents of Data Entry Switches in Each Core Storage Location that is Unprotected. Locations having Protect Bits are Unchanged.	Run	No
3. Clear Storage Protect Bits. All Other Data Remains Unchanged. Parity is Automatically Corrected in Each Word in Storage.	Display	Yes
4. Search for Parity Errors. The P-C Cycles Through Storage Until Stopped by the Stop Key or a Parity Error. The Check Stop Switch Must be on for a Parity Error to Cause a Stop.	Display	No

17415 A

Figure 2-2. Clear Storage Functions

To reset the switch after it has been pulled off, it is necessary to open the panel and remove the plastic console cover to gain access to the spring in the rear of the switch that locks it in the off position.

Console Interrupt

This pushbutton switch (CA151) enables the operator to interrupt P-C operation. The console interrupt level is assigned by the customer. The program switches may be used in conjunction with the console-interrupt switch to specify the console interrupt routine. However, this relationship between the program switches and the console interrupt switch exists only by virtue of the program.

Load I

This pushbutton switch (CA111) is used with the mode switch in the load position to transfer the contents of the data-entry switches into the I-register. The P-C is in the stopped condition when it terminates the load-I operation.

Reset

This pushbutton switch (CA151) is used to reset all basic timing, controls, registers (except index registers and address registers), and I/O devices (except DI and DAO registers). The interrupt-mask register is reset with all bits on. The reset switch is active only when the P-C is stopped (not run).

Immediate Stop

This pushbutton switch (CA151) stops the P-C at the end of the 2, 2.25 or 4 μs core storage cycle in operation when the immediate-stop contacts close.

All basic timing, controls, registers (except index registers and address registers), and I/O devices (except DI and DAO registers) are reset. The immediate-stop switch also ends data-channel (cycle-stealing) operation.

Start

This pushbutton switch (CA151) initiates P-C operation as specified by the mode switch.

Stop

This pushbutton switch (CA111) stops the P-C (T-clock) at the end of the instruction in operation. Cycle-steal operations (X-clock) are not affected.

If, at the same time the stop key is pressed, an interrupt occurs that can force a BSI (i.e., on an unmasked level higher than any in progress), the stop key must be pressed again to be effective. Pressing the start key causes the program to resume operation.

Mode Switch

This eight-position rotary switch (CA111) is used with the start key to extend operator control of the P-C.

Single Instruction with Cycle Steal (SI W/CS): A start key depression with the mode switch on SI W/CS causes the execution of one instruction. Data-channel operations can occur in this mode.

Note: Parity checks may occur during cycle steal cycles on 4 microsecond systems when operating in SI W/CS mode.

Single Instruction (SI): A start key depression with the mode switch on SI causes the execution of one instruction. Data-channel operations are prevented.

Single Storage Cycle (SSC): A start key depression with the mode switch on SSC causes one core storage cycle (2 μs, 2.25 μs or 4 μs). Single-storage-cycle operations can be used in conjunction with the cycle lights to step through instructions and to analyze P-C operation.

Data-channel operations are prevented in this mode.

Single Step (SS): In this mode, each depression of the start key advances the T-clock (or X-clock) one step. (T1 and X1 are two steps long when an 1803 is attached.) One depression of the start key is required for each extended T-7 time. (See "Indicator Lamps, Clock.")

Once single-stepping has begun, the clock cycle should be stepped past T4 or X4 time before pressing the reset key or switching out of SS mode.

The SS mode is normally used with direct program control. This mode can be used with data channel operations; however, data overruns can usually be expected.

Run: A start key depression with the mode switch on run initiates normal program operation of the P-C.

Trace: This position of the mode switch causes a trace interrupt after the execution of each instruction (except XIO).

The trace interrupt is a unique interrupt. It has no device status word and no interrupt level status word, and it cannot be masked. The trace interrupt is the lowest priority customer interrupt. Once initiated, it is delayed by the occurrence of any other interrupt. It cannot occur while other interrupts are being serviced. When the trace interrupt occurs, the P-C executes the forced BSI and branches to the routine whose address is stored at /0009.

Data-channel operations can occur in trace mode.

Load: A start key depression with the mode switch on load causes the contents of the data-entry switches to be stored at the address specified by the I-register. (The P-C must be in a stopped condition.) The I-register is incremented following each load operation caused by pressing the start key.

A load-I key depression with the mode switch on load causes the contents of the data-entry switches to be stored in the I-register.

Data-channel operations are prevented in load mode.

Display: A start key depression with the mode switch on display causes the data at the I-register address to be displayed in the console B-register lights. The I-register is incremented after each display. Successive words are displayed with successive depressions of the start key.

Data-channel operations are prevented in display mode.

2.1.2 Toggle Switches

Sense and Program

The contents of these eight switches (CA221) may be stored in bit positions 0-7 of the A-register or a core storage location. An XIO instruction with a function of 'read' stores the contents of the sense and program switches at the core storage address specified by the IOCC. A function of 'sense device' stores the switch data in the A-register.

Operations Monitor

This switch (CA151) is used to start the operations monitor. The off position disables the operations monitor.

Disable Interrupt

This switch (CA151) is used to suspend all interrupts, including internal errors. While the switch is on, any interrupt that is not masked will latch its 'level' flip-flop in the normal manner, but the active output of the flip-flop will be inhibited. When the switch is turned off, the latched interrupts will be serviced on a priority basis.

Check Stop

When the check-stop switch (CA151) is on, the P-C program will be stopped by any of the following internal errors: invalid operation, B-reg parity error, or storage-protect violation. Each of these errors turns on an associated indicator (red lamp) on the console.

The stop occurs at the end of the core storage cycle in which the error is detected. All operations, including cycle-stealing, are suspended during the check-stop. START must be pressed to restart the system; reset is not necessary. (A check-stop can also be activated via the I/O channel wired interface when the I/O monitor unit is used to trap data. See paragraph 2.11.1.)

The check-stop switch can be used during a clear-storage operation to stop the P-C if a B-reg parity error is detected. (See Figure 2-2.)

When the check-stop switch is off, and the disable-interrupt switch is off, an internal error will cause an internal-level interrupt except on data transfer cycles. (See Figure 1-20.) The P-C program continues to run, and the internal ILSW indicates to the program the cause of the interrupt.

Note in Figure 1-20 that the check-stop switch has no control over the functions of a CAR-check error.

Write Storage Protect Bits

This switch (CA151) enables the writing or clearing of storage-protect bits using the 'store status' instruction or the clear-storage pushbutton (Figure 2-2). This switch must not be operated while the P-C is running or a parity error may result.

Data Entry Switches

The contents of these 16 toggle switches (CA211) can be stored by either manual or program control. Manual control is described under "Mode Switch, Load." Program control requires an XIO (area 0), 'read' or 'sense device' instruction (Figure 1-13, Part 1).

2.1.3 Indicator Lamps

These lamps show the status of significant controls and indicators in the P-C.

Arithmetic Control (ARITH CTL)

On during arithmetic operations (CB511), including effective address generation. Driven by 'arithmetic control' flip-flop.

Shift Control (SHIFT CTL)

On during shift operations (CB511).

Add

On during add operations (CB511). Driven by 'add' flip-flop. Subtract operations are indicated by the ARITH CTL lamp being on and the add lamp being off.

Arithmetic Sign (ARITH SIGN)

On when bit position 0 in the A-register does not initially equal bit position 0 in the B-register (CB511).

Zero Remainder (ZERO REM)

On when the A-register contains a zero balance during a divide operation (CB511).

Branch

On during extended T7 time of a branch instruction (CB511).

Storage Protect Bit (STOR PROT BIT)

On when a storage-protect bit is transferred with the 16 data bits between the B-register and core storage (CB511).

Parity Bit (PTY BIT)

On when a parity bit is transferred with the 16 data bits between the B-Register and core storage (CB511).

Interrupt Service (INTR SERV)

Turned on when any interrupt level is active (CB521).

Cycle Steal Service (CS SERV)

On when any cycle-steal level is active (CB521).

Auxiliary Storage (AUX STOR)

On when auxiliary storage is being used (CB521).

Op Code Check

Turned on when an invalid op code is placed in the op register. The op-code-check indicator (CB521) is turned off and the check indicator is turned on (internal interrupt) at the end of the cycle in which the error is sensed, allowing the op-code-check indicator to indicate any subsequent error.

Storage Protect Check (STOR PROT CHECK)

Turned on when an attempt is made to write into a storage-protected location, except location /000A in conjunction with a CE interrupt, or locations /0004, /0005, and /0006 during interval timer updating.

The storage-protect-check indicator (CB521) is turned off and the check indicator is turned on (internal interrupt) at the end of the cycle in which the error is sensed. This is to allow the storage-protect-check indicator to indicate any subsequent storage-protect error.

Parity Check (PTY CHECK)

Turned on when a parity error (even number of bits) is detected in the 18-bit word transfer between the B-register and core storage. The presence or absence of storage-protect and parity bits in each word is indicated by their respective console indicators.

The parity-check console indicator (CB521) is turned off and the check indicator is turned on (internal interrupt) at the end of the cycle in which the error is sensed, allowing the parity-check indicator to indicate any subsequent parity error.

Clock

These eight lamps (0-7, shown on CB631) indicate the status of the T-clock or X-clock. Normally used during start-key depressions when the mode switch is on single-step (SS).

Cycle

These five lamps (I1, I2, IA, E, and E1, shown on CB651) indicate the progress of an instruction that is being single-stepped (SS mode) or single-cycled (SSC mode).

Timers

These three lamps (A, B, and C, shown on CB651) indicate the status of their respective interval timers. An on condition indicates that the timer is in operation.

Interrupt Levels

An interrupt-level indicator (CB681) is turned on for each interrupt level requesting service or being serviced. Once on, an interrupt-level indicator can be reset by either of two instructions:

1. A 'mask' instruction that is executed before servicing of the interrupt begins. (The interrupt request is not lost but merely detained until the interrupt level is unmasked, at which time the indicator is turned back on. The only exception to this is 'programmed interrupt.')
2. A 'branch out of interrupt' (BOSC) instruction is executed to complete servicing of the interrupt.

Both of the above instructions are quasi-instructions; that is, they are variations of the XIO and BSC instructions.

The last three interrupt-level indicators – CE, trace, and check (internal interrupt) – cannot be masked. The CE interrupt (2.7) can be initiated only from the P-C monitor interface panel or from a device operating in CE mode.

Operation Code (OP CODE)

These five lamps (0-4, shown on CB751) display the op code of each instruction.

Format (F)

On when a two-word instruction is specified (CB751).

Tag

These two lamps indicate the register (XR-1, XR-2, XR-3, or I-register) specified in the instruction. (See Figures 1-1 1-2 and page CB751.)

Indirect Addressing (IA)

On when there is a bit in position 8 of the long-format instruction, which indicates indirect addressing. (See Figure 1-2 and page CB751.)

Branch Out (BO)

On when there is a bit in position 9 of the instruction. In a BSC instruction, this bit specifies a 'branch out of interrupt' (BOSC). (See Figure 1-2 and page CB751.)

Carry (CAR)

On when there is a carry condition in the A-register (CB751).

Overflow (OFLO)

On when an overflow occurs in the A-register (CB751).

2.1.4 Register Display Lamps and Switches

Six rows of indicators and two rotary switches facilitate the display of data registers in the P-C.

Address Register

These 16 lamps (CB781) display the contents of the storage-address register (M-register) or one of the channel-address registers, depending on the position of the display-address rotary switch. The selected register is displayed each time the P-C comes to a stop or wait condition.

Note: Under certain conditions, a channel address register may be displayed while the display-address rotary switch is in the SAR position. See 'Effect of Cycle-Stealing on SAR Display Lamps" (1.7.1).

Display Address Register Switch

This 10- or 16-position rotary switch (CA111) is used to select the storage-address register (M-register) or a channel-address register for display in the address-register lamps.

Permanent Register Displays: I (CB821), B (CB861), D (CB-901), and A (CB941)

The contents of these four registers are always displayed.

Data Register

These 16 lamps (CB981) are driven directly from the A-register-in bus. Each time the P-C is stopped at the end of a cycle (T-7 end-op or X-7 time), the lamps display the contents of the register selected by the display-data register rotary switch. In single-step mode, the lamps display the data that is present on the A-register in bus at each step of the cycle in progress.

Display Data Register Switch

This five-position rotary switch (CA111) is used to select the Q-register, an index register, or the shift counter for display in the data-register lamps. (See "Data Register.")

2.2 INITIAL PROGRAM LOAD (IPL)

In the 1800 system, the first 1442 Card Read Punch is always wired as the IPL device. If there is no 1442 in the system, the 1054 Paper Tape Reader is wired as the IPL device.

The IPL program can be loaded into either main storage or auxiliary storage, depending upon the position of the force-auxiliary switch on the P-C monitor interface panel (2.5.2).

2.2.1 1442 Standard IPL Procedure

When the 1442 is used for initial program load, it operates in packed mode, reading the 80 columns of the first card into the first 40 core storage locations (/0000/0027). Each core storage location stores the binary data from two card columns. For example, binary data from card column 1 (rows 12-5) is read into bit positions 8-15 or core storage location /0000 and binary data from card column 2 (rows 12-5) is read into bit positions 0-7 of the same core storage location. Rows 6-9 of the card are not read into core storage.

The remainder of the first card is entered in the same manner, entering all odd numbered card columns into bit positions 8-15 of their respective core storage locations, and entering all even numbered card columns into bit positions 0-7 of their respective core storage locations.

1. Place program deck in 1442 hopper and press 1442 start key to cause a run-in cycle.
2. Press RESET on P-C console.
3. Set console mode switch to RUN (or SI W/CS) and press PROGRAM LOAD.

After the first card is read into core storage, the P-C begins (at /0000) executing the instructions that were stored from the first card if in run mode. The first card must contain instructions to load the remainder of the program cards.

2.2.2 1054 Standard IPL Procedure

When the 1054 Paper Tape Reader is used for initial program load, tape data is loaded into core storage, starting at location /0000 and loading successively higher core storage locations until an end-of-record punch is sensed in the tape. Each core storage location stores the binary data from four tape characters. For example, binary data from the first tape character (channels 4-1) is stored in bit positions 0-3 of core storage location /0000 and binary data from the fourth tape character (channels 4-1) is stored in bit positions 12-15 of core storage location /0000. Channels 5-8 of the paper tape are not loaded into core storage during initial program load.

The remainder of the tape data is entered in the same manner (four characters per word) until a channel-5 punch is sensed (any channel-5 punch except when it is in a delete character). The channel-5 punch is the end-of-record character and is not read into core storage. An entire program may be loaded from paper tape in IPL mode.

Interrupt requests from the 1054 are suppressed while in IPL mode.

1. Load IPL tape.
2. Press RESET on P-C console.
3. Set console mode switch to RUN and press PROGRAM LOAD.

After the IPL tape record is read into core storage, the P-C begins (at /0000) executing the instructions that were stored in IPL mode. If the entire program was not included in the IPL tape record, the IPL record must contain instructions for loading the remainder of the tape records (program).

2.2.3 IPL into Any Core Location

In IPL mode, the I-register setting specifies the starting address for the program-load operation. When the console reset key is pressed, the I-register is reset to address /0000. However, the contents of the I-register can be set to any desired starting address before loading the program. This choice of starting address makes it possible to load a small program, one that uses displacement addressing exclusively, into an area of core storage without disturbing the contents of the normal IPL area.

Method 1 -- Loading But Not Executing the Program

1. Insert IPL-type program into IPL device and ready device.
2. Press RESET on P-C console.
3. Set I-register to desired load address.
4. Set console mode switch to SI and press PROGRAM LOAD. The program will IPL into the location specified by the I-register and then will stop.

Method 2 -- Loading and Executing the Program

1. Insert IPL-type program into IPL device and ready device.
2. Record contents of core locations /0000 and /0001, then load /4C00 into location /0000.
3. Load desired IPL load address into location /0001.
4. Press RESET on P-C console.
5. Set I-register to desired load address.
6. Set console mode switch to RUN and press PROGRAM LOAD. The program will IPL into the location specified by the I-register and then will branch to /0000 for its first instruction, which is a BSC to the loaded program whose address is in location 0001.
7. Restore contents of locations /0000 and /0001 recorded in step 2.

2.3 ERROR CHECK CIRCUITS

Within the processor-controller, all data is parity checked as it is written from the B-reg to storage. The P-C also checks for invalid operation codes appearing in the op-code register, and it checks for an attempt to write into a storage-protected position of core storage.

Channel address register (CAR) checking is provided to ensure that the first word addressed by a selected CAR is the first word of the correct data table.

A CAR check is made for all devices after the address from the IOCC word is transferred to the selected CAR. During the E2 data cycle, a bit-by-bit comparison is made between the contents of the selected CAR (channel address bus) and the contents of the B-register (channel data bus). If any of the corresponding bits are not equal, a CAR check error has occurred. This E2-cycle CAR check error terminates subsequent cycle-steal requests for the assigned I/O device and initiates an internal interrupt. The I/O device cannot request a cycle steal until the interrupt level status word for the internal interrupt is sensed and the I/O device is reinitialized by another XIO instruction.

Another CAR check is made for chaining each time the I/O device chains to a different data table. The CAR check at the beginning of the second data table and all subsequent data tables in the chain is accomplished as follows: The first word of the data table (second data table, third data table, etc.) must contain its own address. After the first word of the data table is addressed and loaded into the B-register, a bit-by-bit comparison is made between the contents of the selected CAR (channel address bus) and the contents of the B-register (channel data bus). If any of the corresponding bits are not equal, a chaining CAR check error has occurred. Subsequent cycle-steal requests are terminated and a bit is set in the DSW of the device.

The action taken by the processor-controller when an internal error is detected depends on the type of error and the position of the check-stop switch. (See Figure 1-20).

The B-reg parity error, storage-protect violation, and CAR-check error are sent to each I/O adapter via the out bus. If one of these errors occurs while a device is selected, the I/O adapter may take one or more of the following actions:

1. Initialize a device interrupt.
2. Reject the command.
3. Ignore the data.
4. Indicate the error in the device status word.

The I/O adapters also contain checking circuits. The outputs of these circuits are the sensed indicators which make up the device status word. The DSW, through proper programming, can be used to identify the type of error and to guide corrective action in the operating program. The DSW can also be used to log errors during customer run time for later analysis by the customer engineer.

The device status word indicates three types of information: (1) error or exception interrupts, (2) normal data or service interrupts, and (3) routine status. By means of the I/O monitor (2.11.1) these signals can be displayed and identified.

Error check analysis diagrams (ECAD) are provided in the maintenance diagram manual to assist in tracing errors to their source.

2.4 MAINTENANCE DIAGNOSTIC PROGRAMS

The maintenance program system was developed to test, as completely as possible, all machine functions – including data transfer, checking circuits, timings, adjustments, and I/O interaction. In addition, the programs provide fault detection, degrees of localization, and indications of machine status to assist the CE in diagnosing troubles rapidly.

The maintenance programs are provided on cards and paper tape and are fully documented in the diagnostic program manuals provided with the system.

Note: The MPX on-line diagnostics are described in 1800 Service Aid 138 and in the *1800 Multiprogramming Executive Operating System Programmer's Guide,* Order No. GC26-3720.

2.4.1 Program Tests

The following types of maintenance programs are available for the 1800 system:

1. Basic non-monitor programs.
2. Monitor-controlled programs.
3. Auxiliary exercisers.
4. I/O scope routines.
5. Non-monitor timing programs.
6. Utility programs.
7. Disk maintenance library.
8. RPQ monitor-controlled programs.

Basic Non-Monitor Programs

These programs include the monitor header and basic CPU programs (interrupt, interval timer, core, P-C function test, etc.). The monitor header program is used for initial checkout to verify correct operation of the processor-controller.

Monitor-Controlled I/O Function Tests

These tests operate under control of the diagnostic monitor and may be overlapped. Errors are indicated by error messages printed out on the assigned monitor logging device (1443, 1816, or 1053).

Programs can be run one at a time, run in a predetermined sequence, or run simultaneously in any combination, except as limited by core size. Program selection is via the data-entry switches on the console.

The monitor program controls the I/O function tests and incorporates the functions of housekeeping, program loading and execution, interrupt handling, error handling, and customer engineer communication, such as printouts.

A brief description summarizing the objectives of each program is contained in the "System Summary" part of the diagnostic test documentation.

Auxiliary Storage Programs or Exercisers

These programs allow DP I/O device functions to be exercised with minimum interference or dependence on the operating program. The auxiliary programs can be loaded and run from auxiliary storage concurrently with customer operation.

The auxiliary storage loading operation requires a resident loader which can be reloaded if necessary by the CE, but not concurrently with customer operation.

I/O Scope Routines

These are a series of one-card programs that provide the customer engineer with the ability to exercise all DP and process I/O devices with simplified routines. These programs are easily modified when desired and are fully documented with descriptions, flow charts, listings, and service hints.

Timing Programs

These are special purpose input/output programs, each of which is designed to measure some specific parameter, such as the length of inter-record gap, or to facilitate the manual adjustment of mechanical clearance, linkage, speed, etc.

CE Utility Programs

A comprehensive package of utility programs is provided specifically for the customer engineer. These programs include: one-card hex loader, hex dump (core), punch IPL

card, 1053 Dump (core), 80-80 reproduce, 80-80 aux list (aux program to list cards on 1443), and trace-address stop. The utility programs do not provide any testing function in themselves.

Disk Maintenance Library (DIMAL)

On systems with an 1810A only, the DIMAL system generates a disk maintenance library of diagnostic function tests for the 1800 system and provides a method of bringing these tests into core storage for program execution.

The DIMAL system performs the following functions:

1. Loads monitor and non-monitor programs onto the CE disk.
2. Loads selected programs from disk storage into core storage and executes the programs.
3. Makes edit changes.
4. Lists edit table and program directory.

RPQ Monitor - Controlled Programs

The RPQ monitor and associated programs are shipped with all RPQ systems. The programs provide the capability of running RPQ features in overlap mode with all standard system features and I/O devices. The package consists of basic exerciser programs and provides ease of operation (simple printouts). All cards are in hex format, providing ease in program modification and ability to run CE-originated programs under RPQ monitor control.

The RPQ monitor can also be useful on non-RPQ systems. The RPQ monitor package can be obtained by ordering B/M 2147778.

2.4.2 Documentation

The documentation provided for the maintenance program system is contained in two parts.

Program Description

The purpose, requirements, operating parameters, and operating instructions for each of the programs are given in the section titled "System Summary." The basic operating instructions for each program are summarized in the section titled "Operation Summary." Both sections are arranged by PID (program identification) number.

Program Listings

The listings are written in the standard assembler program format and include comments, explanations, and detailed descriptions to help the CE understand and follow the program operation.

2.4.3 Diagnostic Approach

When a trouble is reported in some area of the system, the available programs to test that area can be found in the "System Summary" section of the documentation.

If the failure is in a DP I/O device that the customer does not need while he is running his process, and the customer wishes to continue running the process, the auxiliary program should be used if one is available for that device.

If auxiliary storage is not to be used, select the simplest program that will provide the desired diagnostic or exerciser functions.

CAUTION
Before testing digital and analog output functions, take necessary precautions to ensure that the tests will not interfere with the customer's process.

Since all I/O programs assume that the processor-controller is working properly, whenever the monitor program is to be used, it should be preceded by a test using the basic loader and the monitor header programs to verify correct functioning of the P-C.

When a program is selected for use, a summary of its function can be found in the "Operation Summary" section of the documentation. More detailed information can be obtained by referring to the program write-ups that accompany the program listings.

2.5 I/O MONITOR INTERFACE PANELS

The I/O monitor interface panels are provided for Field Engineering use in servicing the 1800 system. The interface panel in the 1801 or 1802 Processor-Controller is shown in Figure 2-3. It contains manual controls and signal interface connections to permit the use of the various diagnostic facilities. Interface panels are also provided in the 1826 Data Adapter Unit (for AI expander and System/360 adapter) and in the 1810 Disk Storage; however, these panels contain only the requisite interface connectors and no controls.

2.5.1 Interface Connectors

Each interface panel contains a power connector (except 1826-2) and signal connectors for attachment of the I/O monitor unit (paragraph 2.11.1). The power connector delivers SLT voltages and ground to the monitor. Each device attachment that employs the I/O monitor unit provides three signal connectors (A, B, and C) on the interface panel. The following device attachments are monitored via signal connectors on the 1801 or 1802 interface panel:

I/O channel
Analog input
Digital and analog output
Digital input
1443 Printer
1054/1055 Paper Tape
1442 Card Read Punch
2401/2402 Tape Control Unit

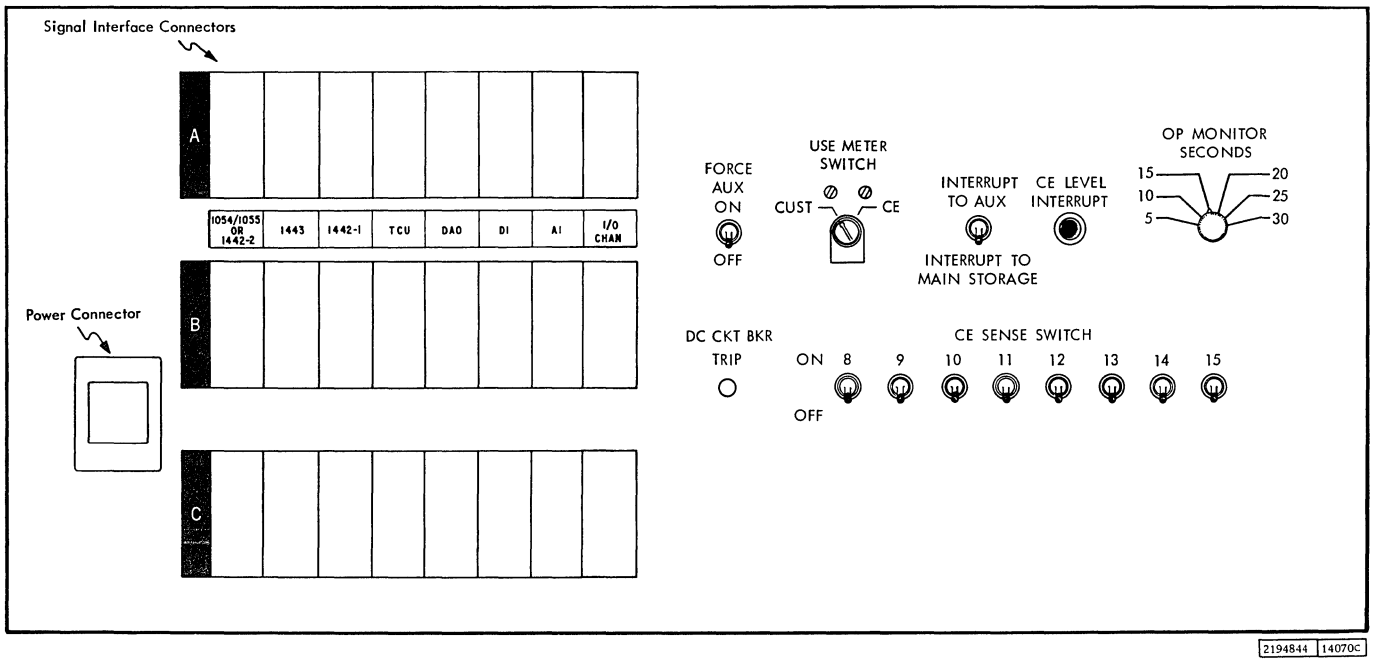


Figure 2-3. I/O Monitor Interface Panel 1801/1802

The signal selection capability of the I/O channel interface makes it possible to use the I/O monitor unit with the 1816, 1053, or 1627.

The 1810 Disk Storage attachment circuits are monitored from the signal connector panel in the 1810. A power connector is provided, and one set of signal connectors (A, B, and C) is provided for each single disk storage. Thus, an 1810 may have one, two or three sets of signal connectors depending upon the model (A1, A2, A3, B1, B2, or B3).

The 1826 Data Adapter Unit includes monitor connections for the AI expander, System/360 adapter, selector channel, or communications adapter if these features are installed. These features are monitored from panel "P" in the 1826 (system diagram YB650). The panel contains one power connector and sets of signal connectors (A, B, and C) for each adapter.

The signal interface lines on the various I/O monitor interface panels provide a convenient means of delivering prime test point data to the I/O monitor unit from the device under test. Some devices also receive manual control signals from the monitor via the signal interface lines.

2.5.2 Functions of Switches -- 1801/1802 Interface Panel

Force Auxiliary On/Off: This toggle switch (number 9, CA311) is set to the on position to initially load (from card or paper tape into auxiliary storage) a resident loader program for diagnostic routines. The entire processor-controller is used, but main core storage cannot be addressed. After the loader program is in auxiliary storage, the switch is turned off and the manual CE interrupt is used to load the diagnostic program into auxiliary storage.

Use Meter Switch: In the customer position, this key-operated switch (CA311) enables the use meters in DP I/O equipment. In the CE position, this switch disables all use meters.

The switch must be in the CE position whenever a DP I/O device is being serviced, unless CE mode is utilized. (See paragraph 2.8.)

Interrupt to Auxiliary/Main Storage: In the auxiliary position, this toggle switch (number 10 on CA311) will cause a CE interrupt branch vector into auxiliary storage address /0001. The return address is stored in 000A of main storage. In the main-storage position, this switch will cause a CE interrupt branch vector into main storage address /0001. The return address is stored in /000A of main storage.

CE Level Interrupt: This pushbutton switch (CA311) causes a CE interrupt into auxiliary storage or main storage, depending upon the position of the interrupt-to-auxiliary/main-storage switch.

DC Circuit Breaker Trip: This lamp (YA145) turns on if an overcurrent CB trips in any MPS (medium power standard)

power supply in the 1801/1802 or 1826. The +48V supply and the power-failure-protect supply are not MPS power supplies and have no circuit breakers.

CE Sense Switches: These eight toggle switches (CA311) are used to direct diagnostic exercises in conjunction with sense and program switches on the programmer's console. On a 'read' command or 'sense device' command, the information contained in the CE sense switches is placed in bit positions 8 through 15 of the data word, and the information contained in the sense and program switches is placed in positions 0 through 7.

Operations Monitor: This rotary switch (CA321) is used to select one of six time intervals (5, 10, 15, 20, 25, 30 seconds) by which to check P-C operations. Once the operations monitor is activated by the switch on the programmer's console, an 'XIO control' instruction (reset timer) must be executed during programmed operations at appropriate intervals to prevent timing out. If the reset command is not given during the selected time interval, the timer expires and the alarm circuit is activated. Timeout can also be caused by a power failure, program hangup, looping, or departure from predicated sequence.

2.6 AUXILIARY STORAGE

Auxiliary storage provides the capability of removing a DP I/O device from control of the customer's program for the purpose of operating the device with an exerciser program. The auxiliary storage program, plus the resident loader and any required control, are limited to 256 words. These short exerciser routines can be loaded and run from auxiliary storage concurrently with the customer's program in main storage.

The loader program for the exerciser is entered into auxiliary storage from the card or paper tape IPL device (2.2) by means of the force-auxiliary switch on the I/O monitor interface panel. Thereafter, auxiliary storage is entered by means of a CE interrupt with the interrupt-to-auxiliary main-storage switch in the auxiliary position. The CE interrupt may be initiated from the CE level interrupt switch or from the I/O device attachment operating in CE mode. The CE interrupt is serviced in auxiliary storage by the exerciser program; then control is returned to the main program by an indirect BOSC (branch out) instruction.

No interrupt polling takes place while operating in auxiliary storage; therefore, only internal interrupts can occur until after exiting auxiliary storage.

Note: If an internal interrupt occurs while in aux storage, the CE interrupt level will be reset and the system will branch to the main storage internal interrupt routine. Upon completion of the routine, instead of returning to the aux storage address in use at the time of the internal interrupt, a BOSC indirect instruction will branch to the corresponding main storage address. Thus, any program that branches out of an internal interrupt routine will return to an address undefined by the program if the interrupt routine was entered from aux storage.

When a data channel operation is initiated in auxiliary storage, an additional CAR register flip-flop is set along with the CAR register. There is an auxiliary CAR bit for each CAR register, and when cycle stealing occurs, this auxiliary CAR bit controls cycle stealing into auxiliary storage. Thus, cycle stealing into auxiliary storage can occur during the main program, and cycle-stealing into main storage can occur during the auxiliary program.

2.7 CE INTERRUPT

The CE interrupt is used specifically for calling diagnostic routines in either auxiliary storage or main storage.

There are two ways that a CE interrupt can be initiated:

1. Depressing the CE-level-interrupt pushbutton on the I/O monitor interface panel.
2. A device previously placed in CE mode has been selected and is attempting its normal interrupt.

The CE interrupt is on the lowest priority level in the system and does not respond to a sense-interrupt command. The CE interrupt is not program maskable; however, all interrupts can be suppressed by the disable-interrupt switch on the programmer's console.

The CE interrupt entry differs from the normal interrupt in the following ways:

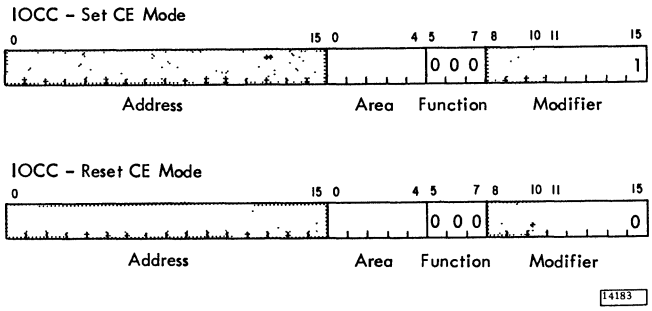
1. The program will branch to location /0001 in either main or auxiliary storage, as determined by the setting of the interrupt-to-auxiliary/main-storage switch.
2. The return address (for the mainline program) is stored in location /000A of main storage regardless of the setting of the interrupt-to-auxiliary/main-storage switch.

2.8 CE MODE

The CE mode of operation allows a DP I/O device to be serviced on-line with minimum interference with the customer's program. While in CE mode, the device will place its interrupt request on the CE interrupt level and not on its regularly assigned level. No provision is made for operating the process I/O features or the tape control unit in CE mode.

A device must be placed in CE mode for proper operation with the exerciser program in auxiliary storage. The device is placed in CE mode, usually at the start of the auxiliary

program, by executing a special XIO instruction. The IOCC contains the device area code, a function code of 000, and modifier bit 15=1. The device is removed from CE mode by the same instruction with modifier bit 15=0.



Modifier bits 11 through 14 are used only for 1816 and 1053 selection as follows:

Bits 11-14	Device
0001	1816 or first 1053
0010	Second 1053
0100	Third 1053
1000	Fourth 1053

Only one device is placed in CE mode at one time.

In addition to placing its interrupt request on the CE interrupt level during CE mode, the device adapter changes its device status word in the following manner:

1. The ready status bit is forced into a "not ready" condition.
2. The busy status bit is forced into a "not busy" condition.

When the device is not in CE mode, the true ready and busy conditions are presented by the standard indicators, and the two special indicators remain off (zero).

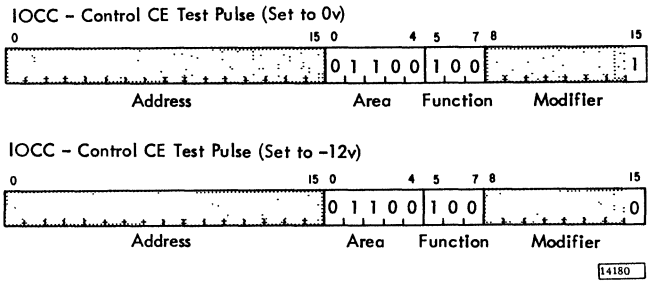
The reset key on the programmer's console will remove devices from CE mode.

2.9 PROGRAMMABLE TEST LATCH (CE TEST PULSE)

A programmable test latch (system diagram PC071) provides a −12V to 0V signal for use as an external sync or as an impulse to the pulse counters. The test signal is carried on black-and-yellow twisted pair from the DAO basic board to the external-sync terminal block (TB19) in the 1801/1802. The signal is available at TB19-12 and dc common at TB19-13.

Test pulses are generated by alternately setting and resetting the test latch with a DAO 'control' command.

Note: The test latch is a feature of DAO basic and requires that the system have DAO capability.



Console reset or power-on reset conditions the test signal to −12V. The /6401 command drives the signal to 0V and the /6400 command restores it to −12V. The pulse duration and repetition rate are controlled by the program.

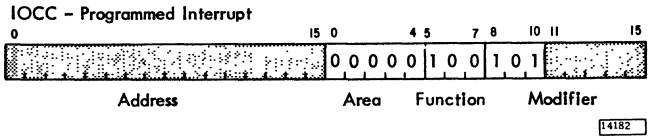
For pulse counter testing, the programmable test signal is used in conjunction with diagnostic program 08C8. After first removing the customer's pulse input, terminals TB19-12 and TB19-13 are jumpered to the desired pulse-counter input terminals on gate R of the 1801 or 1826. (The analog-input twisted-pair test cable can be used for this purpose.)

Note: The customer shall assume responsibility for disconnecting his terminals.

The test signal is made available at remote 1826 units by jumpering terminals TB19-12 and TB19-13 to the CE phone line (paragraph 2.11.6), then connecting jumpers from the phone line to the pulse-counter input terminals at the remote unit.

2.10 CE CYCLE-STEAL TEST

Provision is made for the CE to selectively test the cycle-steal control circuits with the area-0 programmed interrupt (XIO control function).



The instruction does not set any interrupt level flip-flops but does turn on the 'program interrupt selected' line.

On the XIO data cycle, the 'program interrupt selected' line generates a 'cycle steal request test' signal and a 'cycle steal acknowledge test' signal. The 'cycle steal request test' signal is manually jumpered to the desired 'CS request level'

terminator (system diagram CT971), and the 'cycle steal acknowledge test' signal is manually jumpered to the corresponding 'CS level acknowledge' terminator (system diagram CT971).

The CAR exerciser program 08B5 is designed to be used with the CE cycle-steal test function.

2.11 GENERAL TEST EQUIPMENT

A list of tools and test equipment necessary to service the 1800 Data Acquisition and Control System is given in the Appendix.

2.11.1 I/O Monitor Unit

The I/O monitor unit is a service tool capable of displaying the status of registers, latches, and control signals in I/O device attachments while the I/O device is stopped or in operation.

Information concerning the I/O monitor unit is in the Field Engineering Theory-Maintenance Manual, *IBM 1800 Data Acquisition and Control System, I/O Monitor Unit (See FE Bibliography -- 1800 System,* Order No. SY26-0550.)

2.11.2 Oscilloscope

The scope used on the 1800 system should meet or exceed the specifications of the Tektronix Model 453 Oscilloscope.

2.11.3 CE Indicator Latch Card (P/N 5801358)

An optional CE indicator latch card (Figure 2-4) is available from Mechanicsburg as a troubleshooting aid for SLT machines. Thirty-three inch jumpers (P/N 4203785) with SLT connectors for use with the latch card and replacement lamp assembly (P/N 5711078) are also available as needed.

The CE latch is a 2-12 SLT card which plugs into the pin side of the SLT board. It can be plugged into any two vertically adjacent locations *except* edge connectors. The card is intended for use in socket locations with no discrete wiring; however, with care, it can be used in socket locations with no more than one discrete wire wrap on any pin. If the card is left on the SLT board for extended lengths of time, normal machine vibrations may cause it to work out on the pins and lose contact.

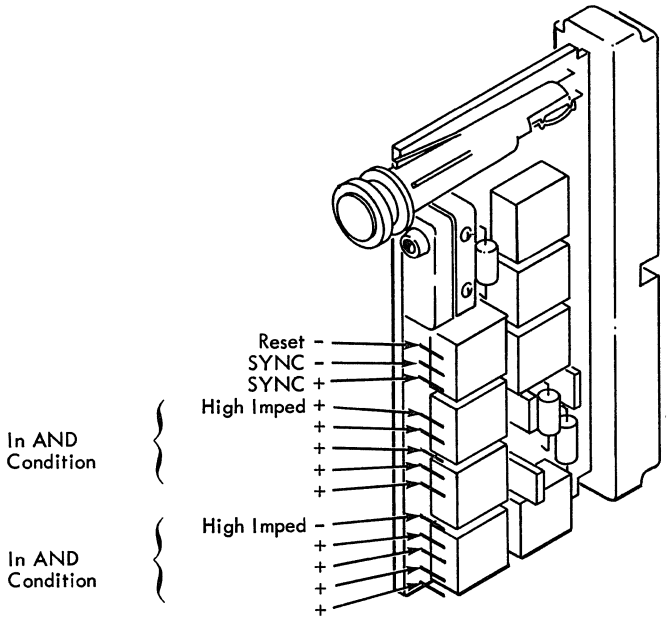
Plugging the card into the board provides voltages (+3, −3, +6) and ground only. The card was designed for use with medium- and high-speed SLT circuits which require +3 volts on pin D03.

CAUTION

Slow-speed circuits have +12 volts on pin D03. If there is any doubt, measure pin D03 with a voltmeter or scope.

The card must be plugged in with the lamp on top and the modules on the right. If the card is plugged in upside down or in the card side of the board, circuit damage may result.

The card extends far enough to cause damage if gates are closed with card installed.



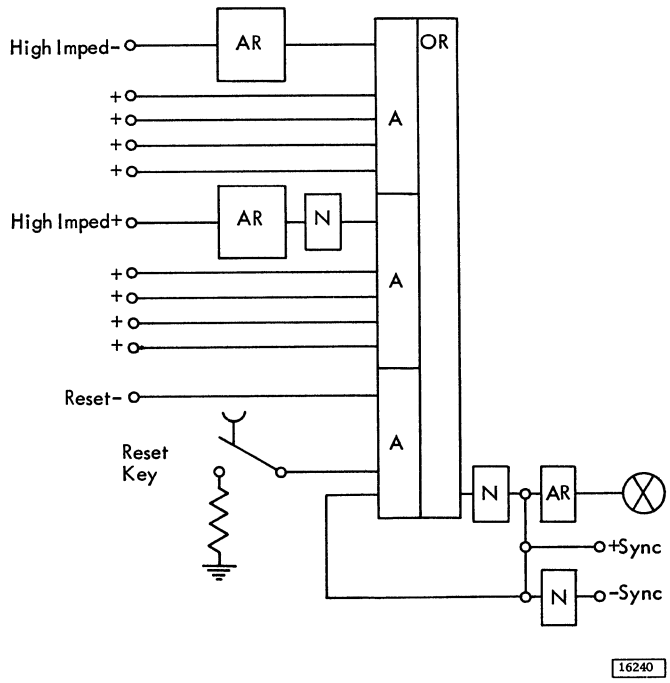


Figure 2-4. CE Indicator Latch Card

The CE latch has an indicator bulb, a reset switch, a reset line, plus and minus sync points for scope triggering, and two five-legged AND blocks ORed to turn on the latch. Inputs are brought to the card by jumpers.

Note: If only one input to an AND block is to be used, it must go to the high-impedance input. If two or more inputs are used, one must go to the high-impedance input. These high-impedance inputs are so designed that the CE latch is not set if the input is floating.

The CE latch can be used in a variety of ways. Some of them, with examples, are listed below.

1. *Baby Sitter:* To find out if several inputs are all plus at the same time, plug the card into the pin side of the SLT board and jumper the suspected lines to one of the AND blocks. Be sure that one of the jumpers goes to the high-impedance input. If all the lines go plus together, the latch will turn on and light the indicator. Reset the latch by pressing the reset button on the card.
2. *Meter or Scope Substitute:* A scope may show a line at or near ground level which may or may not be floating. Jumper the line to the appropriate high-impedance input. If the line is floating, the latch will *not* set. If the line is not floating, the latch will set.
3. *One-Time Pulse Detection:* If a line should not change during a particular sequence of events, jumper the line to the appropriate high-impedance input. For example, if the line is plus and should never go minus, jumper it to the minus high-impedance input. If the line changed value or had a pulse on it, the latch will turn on.
4. *Scope Sync Point:* The necessary signal lines for the syncing condition can be jumpered to one of the AND blocks. Jumper a reset signal, such as a clock pulse, to the reset line on the card. The latch will then turn on with the ANDing conditions and turn off under control of the reset line, furnishing a stable sync point. The scope sync lead is plugged into the plus or minus sync point on the latch card.
5. *Temporary Fix:* Turn the latch on and reset as described in item 4. Use either the plus or minus sync output to condition circuit requiring the temporary fix.

2.11.4 Extender Card

Having available logic blocks to develop sync signals etc. is often helpful in servicing the 1800 system. The extender card (Fig. 2-5) is used to connect spare SLT cards to the pin side of an SLT board.

Use jumper wires to connect signals to the input pins of the spare card. The output pins make the newly developed signal available for use with the CE indicator card (2.11.3), I/O monitor (2.11.1), oscilloscope, etc. Use any spare SLT card that contains the desired functions; two extender cards are needed to connect a double SLT card. Four common SLT cards and their input and output pins are shown in Figure 2-6.

Part numbers:

Extender card - 5808354
Jumper 15" - 2197864
Jumper 36" - 2200079

CAUTION

Exercise care to ensure proper orientation of extender card and spare SLT card (Figure 2-5).

The CE indicator latch card *must not* be plugged into the extender card. The voltage pins on the CE latch card are *only* oriented for SLT backpanel plugging.

Do not plug the extender card into a cable connector position on the SLT board as the proper voltages are not present.

2.11.5 Seven—Position Binary Counter

Intermittent errors may be simplified or localized by means of this counter. Sequential movements of clocks or rings or the logical progression of an adapter can be studied by this method of diagnosis.

As an example, Figure 2-7 shows the necessary connections to determine the failing column on a 1442 data error problem. Because the counter starts at 0 and the card columns are numbered from 1, the number of the failing column will be one more than the accumulated count.

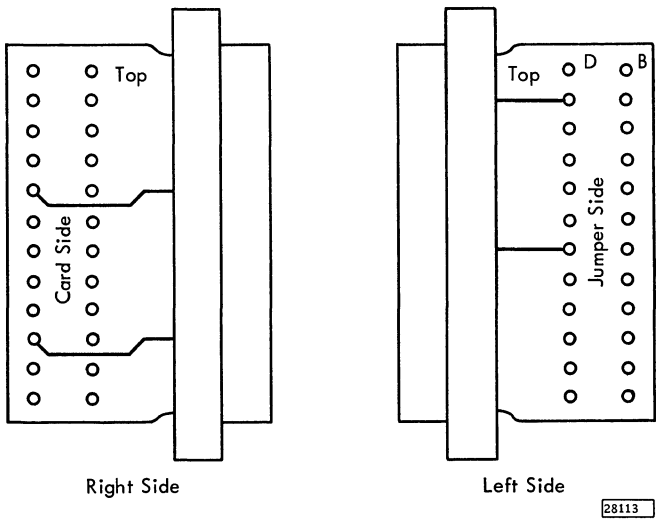
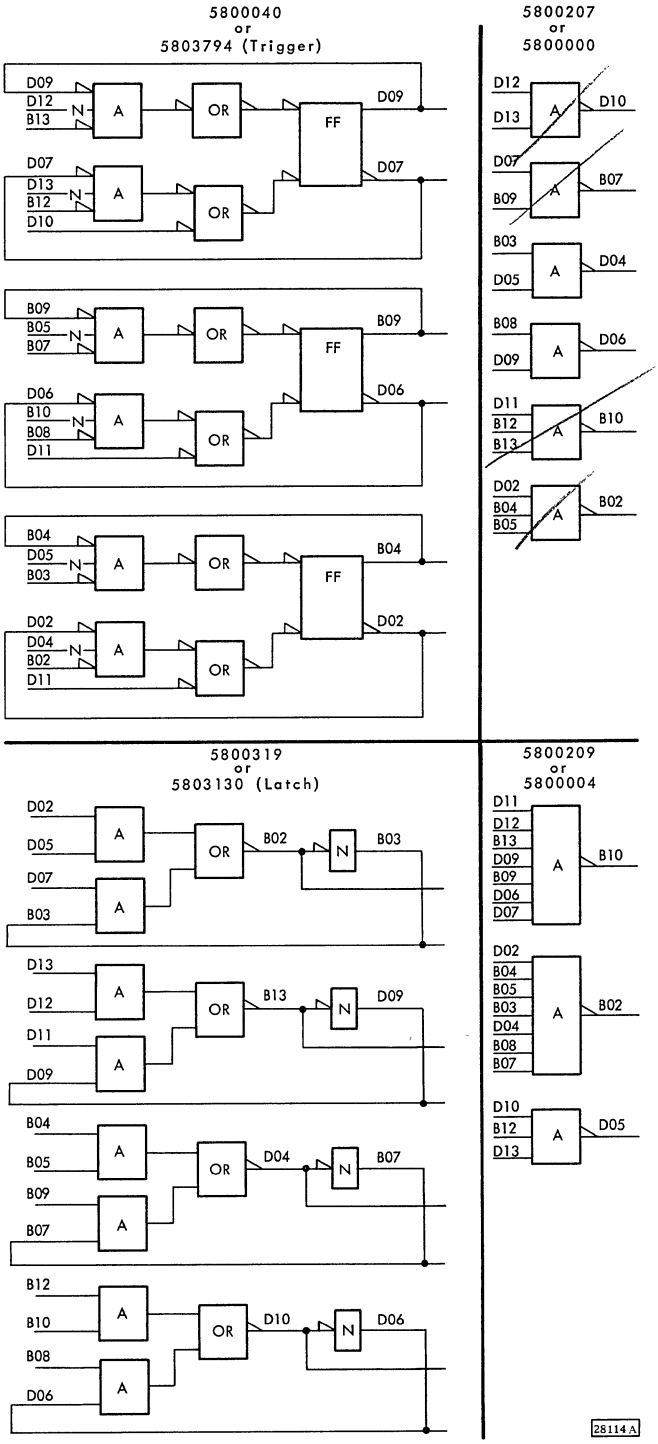


Figure 2-5. Extender Card



● Figure 2-6. Common SLT Cards

Part numbers:

AND/OR card	-	5800000
Seven-position binary counter	-	5803793
Light indicator card	-	5803975

2.11.6 Remote Switch Box

The remote switch box (P/N 2105671) permits limited control of the processor-controller from remote locations. The switch box is provided with a 30-foot cable that can be connected to the 1801/1802, 1826-1, or 1828-1. The 1826-1 and and the 1828-1 are free-standing units that can be located at distances up to 100 feet from the processor-controller.

The remote switch box contains four control keys: start, stop, immediate stop (causes dc reset), and CE interrupt. These keys perform the same functions as do their counterparts in the 1801/1802.

Cable connections for the remote start circuit are shown in Figure 2-8. Connections for the stop and CE interrupt are similar. The immediate-stop circuit uses only the normally open and common connections.

Three connectors, A, B, and C, are provided on the 1801/1802 power tailgate. The connectors are wired in parallel and can be used interchangeably. Cables to the remote units are normally plugged into connectors A and C, and a shorting plug is placed in connector B. At each remote location, two interchangeable connectors are provided to receive the cable from the 1801/1802 and the cable from the remote switch box.

To use the remote switch box, the shorting plug is removed and the remote switch box is plugged into the available connector at the 1826-1 or 1828-1, or it may be plugged into the 1801/1802 connector vacated by the shorting plug.

The remote switch box cable must be disconnected when it is not being used, and the shorting plug must be replaced in the 1801/1802 connector.

CAUTION

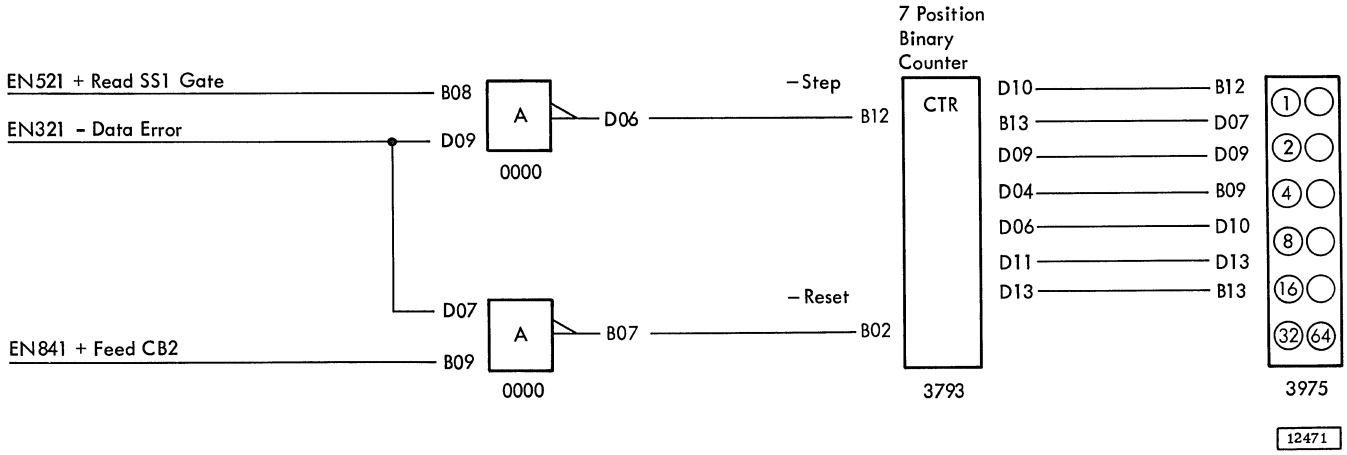
The processor-controller switches that are duplicated by the remote switch box should not be used when the remote box is connected, as their operation will be unpredictable.

CE Phone Line

A two-conductor phone line is included in the signal cable to the remote switch box connectors. The line is terminated at phone jacks adjacent to the remote switch box connectors in the 1801/1802, 1826-1, and 1828-1.

The phone line permits voice communication between customer engineers at widely separated units, using IBM sound-powered phones.

With the phones disconnected, the phone line can be used as an extension of the meter leads for checking continuity of interconnecting machine cables. For external-sync or pulse-counter testing, the phone lines can be jumpered to TP19-12 and TB19-13 in the processor-controller to make the programmed test signal available at the remote 1826.



● Figure 2-7. Seven-Position Binary Counter

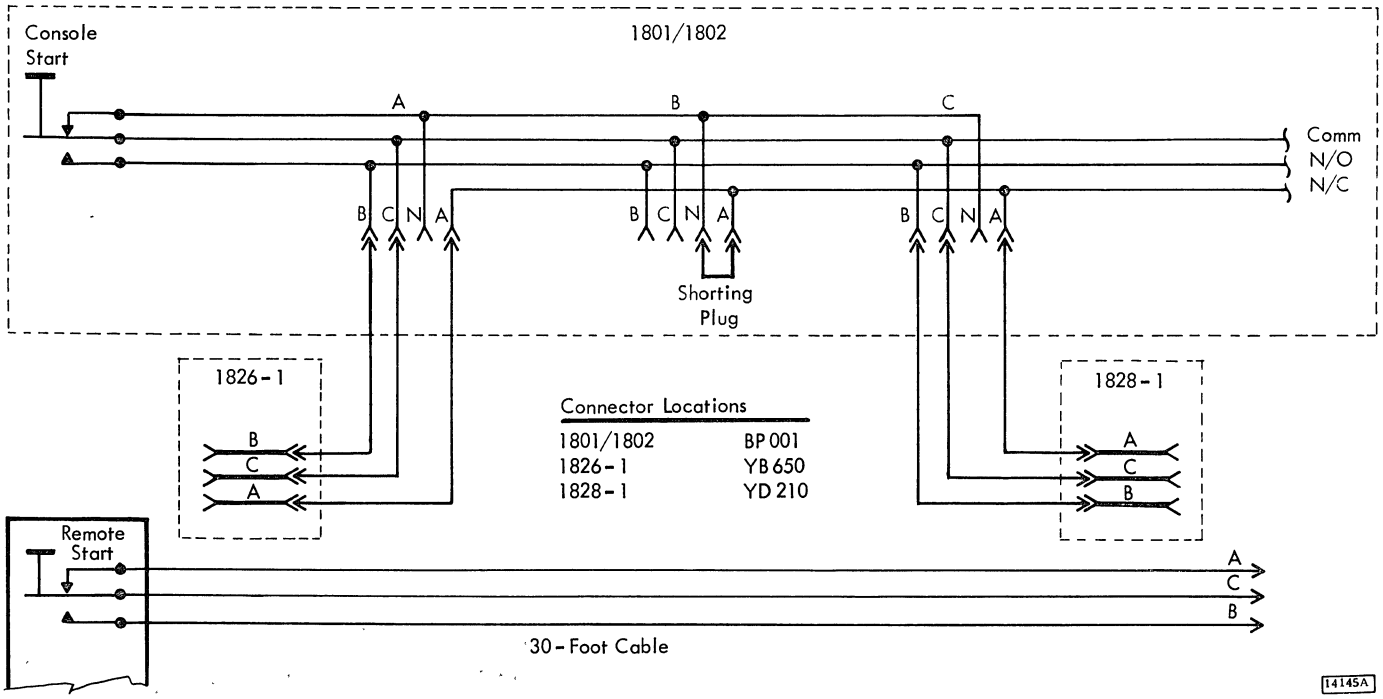


Figure 2-8. Cable Connections to Remote Start Circuit

2.12 PROCESS I/O TEST EQUIPMENT

2.12.1 Fluke* DC Differential Voltmeter

The analog output features are calibrated using a Fluke 885A/AA Precision Voltmeter (Figure 2-9) obtainable from the area ICAR center.

The Fluke meter is a general-purpose, precision voltmeter that operates on 115 Vac. It compares the input voltage with a self-contained reference voltage by means of a high-input-impedance null detector.

An instruction booklet is included with the meter.

*Trademark of John Fluke Mfg. Co., Seattle, Washington

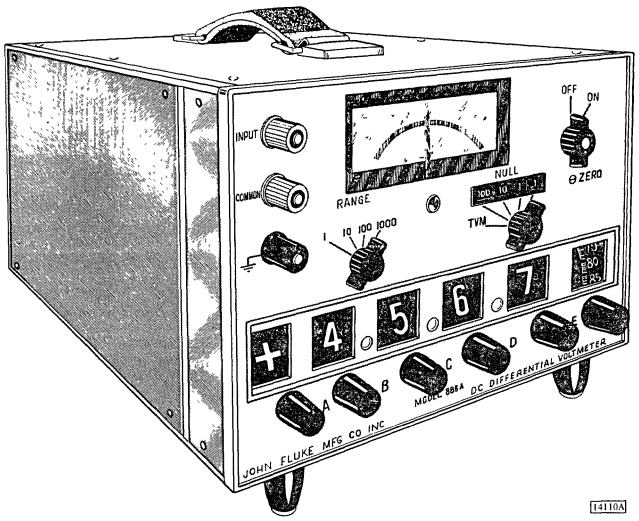


Figure 2-9. Fluke Precision Voltmeter (P/N 453191)

2.12.2 Analog Input Calibration Facility

The analog input calibration facility (Figure 2-10) is housed in the 1828-2 Enclosure that abuts the 1801, 1802, or 1826 containing the AI basic boards. The calibration facility is mounted inside the upper right-hand side of the 1828-2 frame and is accessible from the rear of the enclosure.

Primary power is supplied to the calibration facility through the AI calibration switch on the left side of the 1828 bonnet.

The calibration facility consists of a 30-volt ungrounded power supply, a precision voltage reference unit of 6.3 volts, a resistive divider network, and a high-level solid-state multiplex switch. The circuit schematic is shown on system diagram YD120.

The calibration facility provides the following dc reference voltages (nominal) for calibration of AI features:

+5 volts	100 mV
−5 volts	50 mV
500 mV	20 mV
200 mV	10 mV

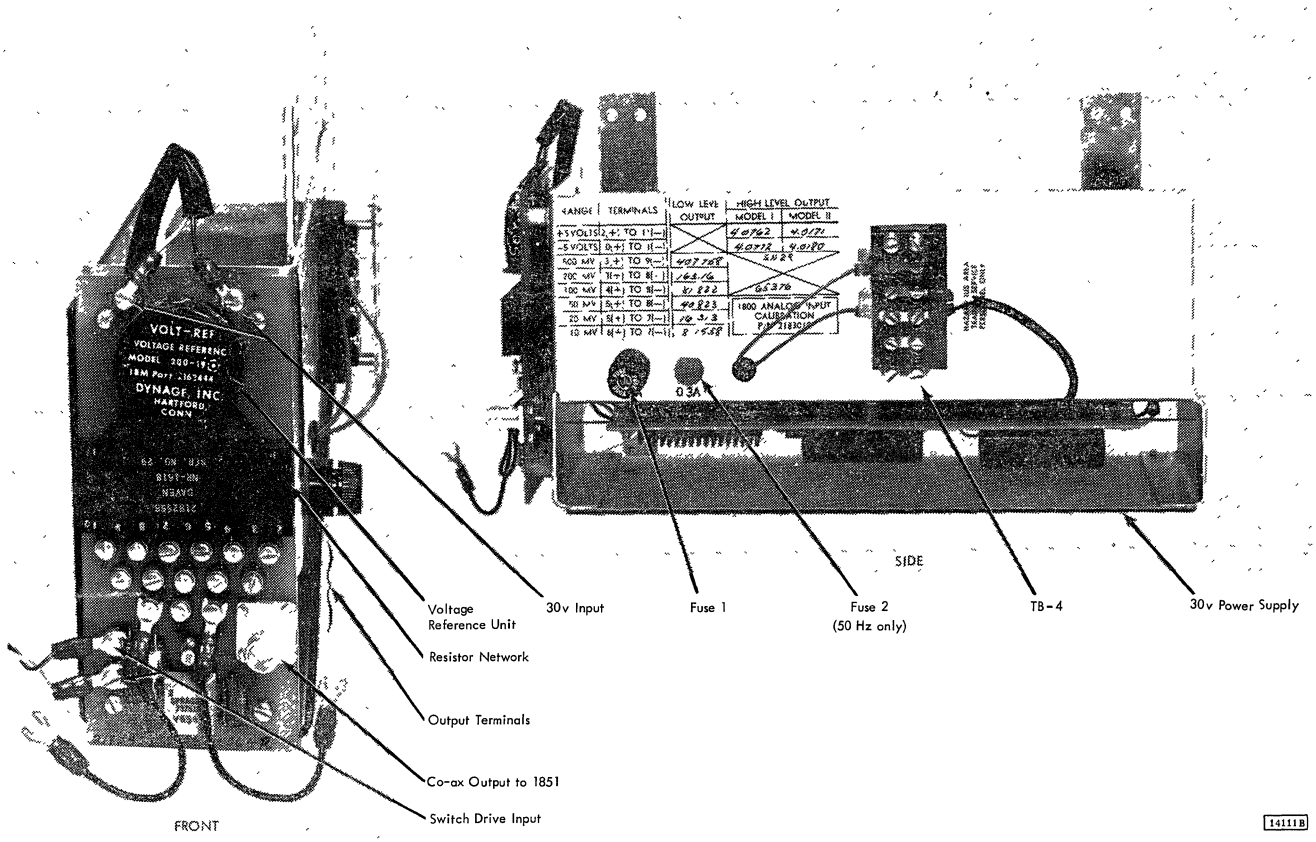


Figure 2-10. Analog Input Calibration Facility

Exact voltages between terminals are measured at the factory and are recorded (to five significant digits) on the reference unit.

The analog reference voltage can be connected to the special multiplex switch (terminals A and C) for direct switching onto the analog input coaxial cable under program control. The coaxial output of the calibration facility connects to the AI coaxial input cable at the "T" connector (terminal 5) of the last 1851 Multiplexer Terminal installed in the 1828. The special multiplex switch is selected by multiplexer address /13E8, which is outside the normal range of MPX/S addresses. (Actually, any address /13xx will select the special switch.)

When the analog reference voltage is not being used for calibration, the coaxial cable is left connected for +5V switched input to the analog input bus, and the AI calibration switch is left on. The multiplexed calibration point can be addressed at any time by the customer program or diagnostic program for an operational check on the ADC.

For ADC calibration, and for checking accuracy and repeatability on systems with MPX/S inputs, the output of the multiplexed calibrate point (terminals A and B) is connected directly to the input terminal block on the ADC board. The coaxial cable is disconnected at each end and is replaced by a twisted-pair cable that is provided with the calibration facility.

For calibration of differential (low-level) amplifiers, the analog reference voltage is disconnected from the multiplex switch input and is connected via twisted pair from the appropriate low-level output terminals on the calibrate card to an unused MPX/R input point assigned to the amplifier being calibrated. The reference voltage is connected in this same manner when running accuracy and repeatability checks on systems with MPX/R inputs.

Precautions

The following precautions should be observed to prevent damage to the calibration source or impairment of its accuracy.

1. Do not connect calibration source to customer terminals until current element and customer lines have been removed by customer.
2. Do not connect calibration source to more than one analog input at a time.
3. Do not permit prolonged shorting of calibration source output terminals.
4. Because of impedance mismatch, accurate measurements are not possible if the calibration source is connected directly to a solid-state input point.

2.12.3 Digital Input Test Card

The digital-input test card (P/N 2195669) is used in conjunction with diagnostic programs 0824 and 0825 to test the digital-input and process-interrupt features. The test card provides a known digital-input bit configuration to any desired DI or PI group (16 points) for reading by the program.

The DI test card consists of a specially wired SLT connector card fitted with two 12-inch leads. Lead 1 is connected to bit positions 0-2-4-6-8-10-12-14 of the test card, and lead 2 is connected to bit positions 1-3-5-7-9-11-13-15.

For testing digital inputs or process interrupts, the input cable from the "R" gate is disconnected at the socket on the adapter board, and the test card is plugged onto the pins of the same socket on the reverse (pin) side of the board.

CAUTION
The SLT board can be destroyed if the test card is installed upside down. The card is labeled to indicate proper orientation.

DI Group	PI Group	Socket
0	1	N2
1	2	N3
2	3	N4
3		N5
4		N6
5		N7
6		A6
7		A7

The test leads are connected to either +3V (D03 pin) or −3V (B06 pin), depending on the bit pattern desired. Pin connections for various bit patterns are shown in the following table.

Pin Connection		Resulting Bit Pattern	Hex
Lead 1	Lead 2		
D03	B06	1010101010101010	AAAA
B06	D03	0101010101010101	5555
D03	D03	1111111111111111	FFFF
B06	B06	0000000000000000	0000

14179

2.12.4 Digital Output Test Cable

The digital-output test cable (P/N 2195696) is used in conjunction with diagnostic program 0827 to test the digital output feature.

The DO test cable consists of a 10-foot cable with a serpent connector on one end and an SLT connector card on the other end.

For testing a digital output group (16 points), the signal cable that connects the DO adapter to the "R" gate is disconnected at the socket on the adapter board, and the test cable is plugged onto the pins of the same socket on the reverse (pin) side of the board. Do not disconnect the *return* cable used with ECO and PO groups.

DO Group	Signal Cable
0	A6
1	A7
2	N2
3	N6

The other end of the test cable is plugged to either the A or B signal cable of the I/O monitor unit. (The I/O monitor unit power cable must be connected to the monitor interface panel.)

The data that is sent to the DO group by the program will appear in the monitor display lamps as the *true value* for register output, and as the *1's complement* value for electronic "contact" operate and pulse output.

2.12.5 1856 DAC/PVR Extender

The DAC/PVR extender (P/N 2182700) allows access to the components in a DAC or PVR module while the module is connected into the system. The extender (Figure 2-11) is a hollow shell that occupies one unit space in the 1856. Connectors at each end of the extender are wired together internally.

In use, the extender is plugged into the 1856 in place of the module to be extended, and the module is then plugged into, and supported by, the extender.

Note: The extender is intended for diagnostic purposes only. Do not use extender when calibrating the analog output features.

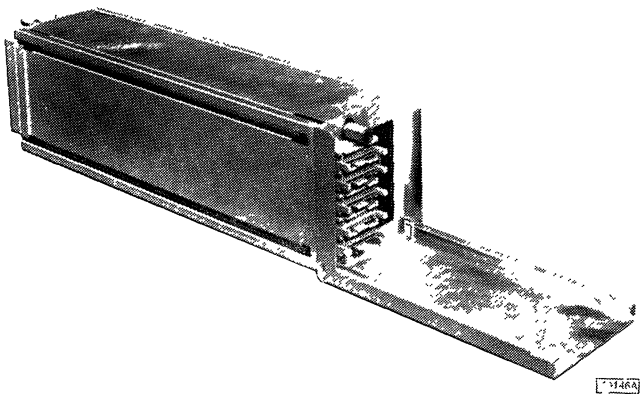


Figure 2-11. 1856 DAC/PVR Extender (P/N 2182700)

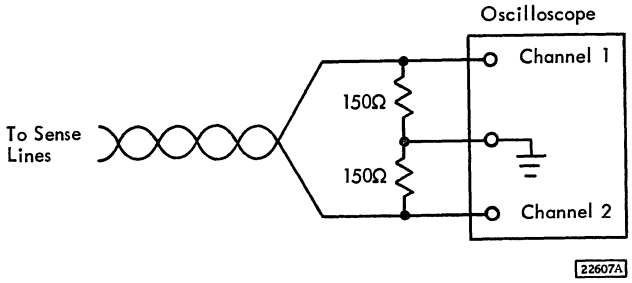
2.13 CORE STORAGE TEST EQUIPMENT

2.13.1 Oscilloscope

The scope used for troubleshooting and adjusting core storage should meet or exceed the specifications of the Tektronix Model 453. Scopes not meeting this requirement should be used in an emergency only.

2.13.2 Differential Scope Cable

The differential scope cable (P/N 218907 is a shielded, twisted pair with 150-ohm termination to scope ground. It is used to scope sense lines differentially, with the scope in "Ch. 1 added to Ch. 2 (INV)" mode.



These leads can pick up noise even though they are twisted and shielded. They should be plugged and removed from the sense amps only when the machine is stopped, or extra bits will result. The leads should not be left attached to the core storage unit during long-term tests, because of impedance characteristics and noise pickup. Do not leave only one lead attached to a sense line.

2.13.3 Current Probe

The Tektronix P6016 current probe (P/N 451213), or equivalent, should be used to scope core storage waveforms. The terminator (P/N 451214) must be used with the probe. Fuzzy signals will sometimes be seen when using a current probe; this condition is normal and is caused by the dc flux buildup in the probe.

2.13.4 Core Storage Current Probing Card

The current probing card (P/N 2182906) is used with the oscilloscope current probe for measuring X- and Y-drive currents. The current probing card consists of a card offset that is wired with 3-inch jumpers to provide current loops in the core drive lines.

When it is necessary to measure core storage drive currents, the array connector block containing the desired drive lines is removed with the jumper block removal tool (P/N 2108860) and replaced with the current probing card (Figure 2-12).

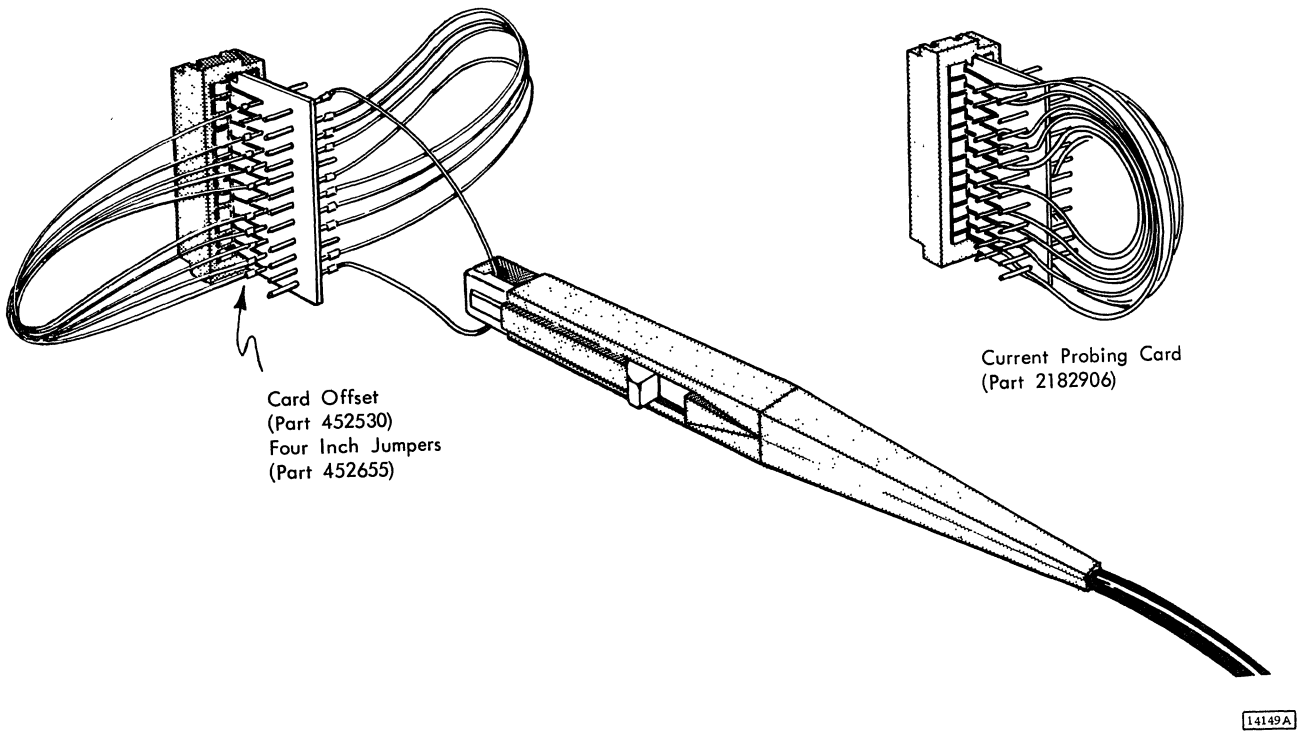


Figure 2-12. Core Storage Current Probing Cards

CAUTION
System power must be removed when removing or installing connector blocks. Excessive connector-block removals must be avoided (see 1.5.1). Insert probing card with red wires on left (D pins).

2.13.5 Card Offset and Four-Inch Jumpers

The card offset (P/N 452530) with 4 inch jumpers (P/N 452655) is an unassembled version of the core storage probing card (P/N 2182906). The jumper block and jumpers provide flexibility to the CE, allowing X- or Y-drive lines to be swapped at the block or between several blocks (Figure 2-12).

CAUTION
Extreme care should be exercised to prevent destructive shorting when using the jumper block. This tool should not be used on sense lines because of excessive noise pickup. See 2.13.4 for information concerning connector-block removal.

2.13.6 Thermometer

The thermometer (P/N 5392366) is recommended as an on-site tool for 2- and 4-microsecond systems. The thermometer is used to set the temperature tracking voltages to the actual intake air temperature at the core storage unit being adjusted (see 4.4.3).

2.13.7 Meter (Weston 901)

The Weston 901 (P/N 460879) has an accuracy of 0.5%. A meter with equivalent or greater accuracy should be used to set core storage voltages. A less accurate meter should be used in emergencies only.

Chapter 3. Preventive Maintenance

The 1800 system is designed for minimum routine maintenance, as shown in Figure 3-1.

Filter cleaning and replacement is the primary preventive maintenance function. In a relatively clean and air-conditioned environment, filters should not require changing more often than the six-month interval. In particularly dusty environments, it will be necessary to check and replace filters on a schedule learned by experience on the particular system.

Fans and blower motors in the SLT gates and power supplies have sealed bearings that are permanently lubricated.

Electromechanical DP I/O units require maintenance according to their published schedules. As with filter replacement, these schedules will have to be adjusted according to the dictates of usage, rate of wear, and environment.

It should not be necessary to run diagnostic programs on a scheduled basis. The exception is where the customer's programming detects the possibility of failures of a specific or nonspecific nature or where the diagnostic program is utilized as a calibration or adjustment check.

Code U	Code R	Location or Operation	Freq	Operation	Reference
0		Filter, Blower	As Req	Check for dirty filters; replace as required. Check cooling fans for proper operation.	Sections 4.2.2 5.4.3
8		ADC	6	Check ADC accuracy and repeatability and recalibrate if necessary. Refer to system logics for calibrate procedure.	System Diagrams QD810, QD815
3		Amplifier		Check and recalibrate, if necessary, the buffer or sample and hold amplifier in the 1801/1802/1826 and the differential amplifiers in 1851's. Refer to system logic for calibrate procedure.	
1		Analog Output		Check and recalibrate, if necessary, the Analog Output feature. Note: Fluke 885 A/AA Precision Voltmeter is required and can be obtained from Area ICAR Center.	System Diag TA002
9		Misc		Inspect for loose connectors, SLT boards, modules, etc. Check system grounding network and line cord for correct operation and safe condition.	

14147D

● Figure 3-1. 1800 System Preventive Maintenance Chart (Series 4)

Chapter 4. Checks, Adjustments, and Removals

Section 1. Basic Unit

4.1 PANEL LAMPS

Indicator lamps and message lamps used in the IBM 1800 Data Acquisition and Control System are removable from the front of the panel.

4.1.1 Indicator Lamp Removal/Replacement

1. Grasp burned-out lamp with thumb and forefinger and pull straight out.
2. Insert new lamp in socket. The lamp and socket are keyed for correct alignment.

4.1.2 Message Lamp Removal/Replacement

1. Remove message button by pulling straight out.
2. Remove old lamp and insert new one, using tool, P/N 461163.
3. Reinstall message button by pressing straight in.

4.2 GATE BLOWERS

4.2.1 Blower Removal/Replacement

The gate blower assemblies are designed for quick removal. Blower motor lubrication is not required.

1. Remove mainline power.
2. Disconnect the blower power plug at the hinge end of the gate.
3. Support the blower assembly with one hand. Turn the latch (Figure 4-1) counterclockwise and uncouple the latch.
4. Support the blower assembly with both hands and pull the assembly away from the hinge end of the gate.
5. Replace the blower assembly by reversing the removal procedure.
6. Turn on mainline power and check blower for proper operation.

4.2.2 Filter Replacement

All blower assemblies in the SLT gates contain replaceable filters. These filters must be inspected regularly on a schedule dictated by the environment and replaced whenever air flow is obviously being restricted. It is not necessary to remove power when replacing gate filters; however, care must be taken not to contact electrical connections with filters that have metal frames.

1. Open SLT gate.
2. Grasp sides of filter at end of gate opposite gate hinges and pull down to release filter from the plunger retainer.
3. Pull filter from the lip on the hinge end of the gate and lift out.

Note: Plastic filters can be cleaned by vacuuming or by washing in warm water that contains a mild soap or detergent. If filters are cleaned by washing, a system of rotation should be set up whereby a thoroughly dry filter is available to replace the one that is presently removed. Filters that are cleaned by vacuuming should be reinstalled so that the direction of airflow is the same as it was before removal. Discard any filter that shows signs of deterioration.

4. Install clean, dry filter by inserting under lip at hinge end of gate and snapping into position.

4.3 CENTRAL PROCESSING UNIT

4.3.1 Service Check

The diagnostic monitor header program 0800 provides a quick check of basic CPU functions, and indicates those areas that require further checking.

4.3.2 Phase A/B Adjustment

Phase A and phase B pulse durations should be equal within 10%. Favor a shorter phase B pulse duration. Adjustment is made at the 1-volt level of positive transition.

Set up scope as follows:

Vert (Chan 1 and 2): 1 V/div
Horizontal: 50 ns/div (2 μs); 100 ns/div (4 μs)
Sync: –, B phase
Mode: Alternate

To adjust:

1. Place mode switch in run position.
2. Scope '+A phase power' at B-B2F2J05 (system diagram CC021).
3. Scope '+B phase power' at B-B2F2J10.
4. Adjust oscillator potentiometer at B-B2J4 for correct phase-A and phase-B pulse widths.

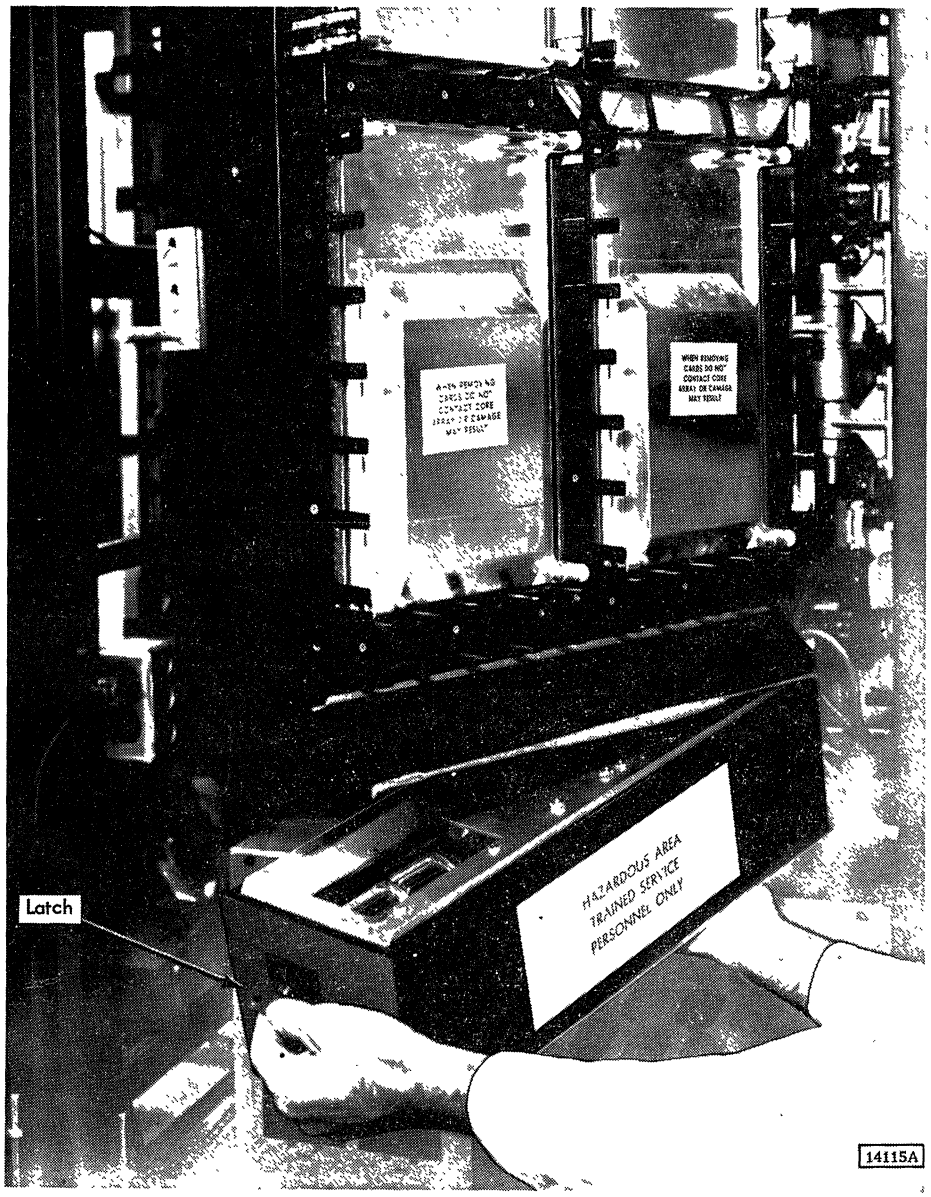


Figure 4-1. Gate Blower Removal

5. After adjustment, check interval-timer time bases for proper duration and run CPU diagnostics.

4.3.3 Operations Monitor

Service Check

Use the following procedure to check the monitor time periods.

1. Turn off operations-monitor toggle switch to reset the timer circuit.
2. Select time period with the op-monitor rotary switch on the I/O monitor interface panel.
3. Turn on operations-monitor toggle switch and measure the time required for the alarm lamp to turn on. Time periods should measure within ±10% of the selected value.

Adjustment

If any time period requires adjustment, use the procedure outlined in the Service Check and adjust the corresponding pot on the card at B-A1L5 to obtain the correct timing within ±10%.

The following table lists the pot locations on the card. If any time interval is adjusted, each succeeding time interval must also be adjusted in the order given.

Op Monitor Period (seconds)	B-AIL5 Pot (Top to Bottom)
5	1
10	2
15	3
20	4
25	5
30	6

4.4 CORE STORAGE

4.4.1 General Precautions

1. Do not remove a core storage card with system power on.
2. Do not apply power to the system with a core storage card removed.
3. When removing or inserting SLT cards adjacent to the core array, take care not to disturb the pressure contacts on the sides of the array.
4. Do not disturb the core planes.
5. Do not leave the array unit unattended when the covers are removed.
6. Do not remove minibus plugs unless absolutely necessary to the maintenance procedure. Use extreme caution when replacing plugs; plugging to the wrong pins can damage the core array.
7. Use an SLT scope-probe tip when probing with power on. Shorting of adjacent pins can cause circuit damage.

4.4.2 Service Check

Core function tests 08CA, 08CB, and 08CC are nonmonitor programs that verify proper operation of core storage.

Core adjustment programs 08C0 and 08C1 exercise core storage for adjustment purposes.

The core adjustment programs (08C0, 08C1) should be run if the function tests fail to show a suspected core storage problem.

4.4.3 Core Storage Adjustments

Core Storage adjustments are set for optimum core storage operation. Do not change these adjustments unless a card is changed that contains a core storage adjustment pot, or failure patterns indicate that adjustments are needed (review section 1.7). For adjustment procedures, see logic page SD013 at EC731503A or later for 4-microsecond storage units, or logic page SA022 at EC731506C or later for 2-microsecond storage units.

A sealing compound has been added to core storage adjustment pots to maintain integrity of factory settings. The seal can be broken whenever adjustment is required in the field.

To avoid shorting to adjacent components, use the plastic alignment screwdriver, P/N 460811, when adjusting pots in the core storage circuits.

Refer to paragraph 2.13.4 for information on the current probing card provided for scoping X and Y drive lines.

Proper operation of core storage temperature tracking circuits requires that the core storage cover be closed except for brief periods of time. New production machines include a hole in the cover to allow adjustment of the VRef pot while the cover is closed. An 1800 Service Aid (number 67) explains how to install holes in existing covers.

4.4.4 Array Removal/Replacement

1. Remove all power to the system.
2. Remove adjacent cards.
3. On the wiring side of the board, remove the minibus connectors to allow removal of the array connector blocks.
4. Remove the array connector blocks.
5. Remove the four clamping screws that secure the array to the board.
6. Pull array out straight to prevent damage to pins and land patterns on the core unit. Place the array in a safe and secure working area.
7. Replace the array in the reverse order.

4.4.5 Core Storage Board (BSM) Removal/Replacement

When it is necessary to replace the core storage unit, the core array and board are replaced as an assembly.

1. Remove all voltage crossover connections to the laminar bus.
2. Remove temperature tracking wires as required:
   a. Four-microsecond core storages – none.
   b. Two-microsecond core storages and no 1803 – from board at B-A3.
   c. System with 1803 – from boards at B-B3 in 1801/1802 and at B-B2 in 1803.
3. Unplug SLT flat cables at board connectors.
4. Remove cable clamp on outer edge of board (card side) and remove SLT cards in outer columns of board.
5. Remove eight mounting screws with allen wrench, P/N 2018490.
6. Carefully withdraw core storage unit from gate directing the assembly away from the laminar bus so as to clear the voltage crossover wires.
7. Replace the assembly in the reverse order.

4.4.6 Core Storage Diodes Removal/Replacement

Diodes are field replaceable. To remove, cut the leads as close to the defective diode pack as possible. Solder the new diode pack to the existing leads. Diode pack part numbers are:

	Formed leads	Unformed leads
Common anode	2192714	2391100
Common cathode	2192721	2391101

A discrete GY diode (P/N 2414891) may be used in an emergency if the diode packs are not available. This diode can be used to replace the single diode that is failing.

4.5 CHANNEL CONTROL

4.5.1 Service Check - - Interval Timers

Diagnostic program 08B2 is a non-monitor program that verifies correct operation of the interval timers.

4.5.2 Service Check - - Interrupt

Diagnostic program 08B3 is a non-monitor program that verifies correct operation of the interrupt circuits.

Section 2. Features

When any maintenance is performed on a DP I/O unit, its use meter must be disabled by setting the use-meter switch (1800 monitor interface panel) to the CE position.

4.6 1816–1053 ADAPTER

4.6.1 Service Check

Diagnostic program 0806 is a monitor-controlled function test that checks the performance of all 1053/1816 printers on the system.

Auxiliary program 08A4 tests the operation of the 1816 Printer-Keyboard. Auxiliary program 08A5 exercises the printing functions of the 1053 or 1816 by printing a programmed test pattern.

4.6.2 Singleshot Adjustments

Adjust singleshots with the CE alignment screwdriver, P/N 460811. Adjust each singleshot duration to that specified in the system diagrams. Figure 4-2 is a list of 1816/1053 adapter singleshots, their durations, limits, pin locations, and logic page locations.

For adjustment service hint see paragraph 1.6.2.

4.7 1054–1055 ADAPTER

4.7.1 Service Check

Diagnostic program 0804 is a monitor-controlled function test that verifies proper operation of the status indicators and data handling by the paper-tape reader and punch.

Auxiliary program 08A8 tests the reading function of the 1054 Paper Tape Reader and the punching function of the 1055 Paper Tape Punch.

4.7.2 Singleshot Adjustments

Adjust each singleshot duration to that specified in the system diagrams. Figure 4-3 is a list of the 1054-1055 adapter singleshots, their durations, pin locations, and system diagram page numbers. For adjustment service hint see paragraph 1.6.2.

Single - Shot	Duration		Pin Location *	Logic Page
	Nominal	Limits		
Keyboard Restore (Upper Pot)	25 ms	22.5 - 27.5 ms	H6 D11	EC 701
Keyboard Service Request (Lower)	25 ms	22.5 - 27.5 ms	H6 D12	EC 701
* Board C-A1 for 1st adapter; Board D-B1 for 2nd adapter				

14103 B

Figure 4-2. 1816/1053 Singleshots

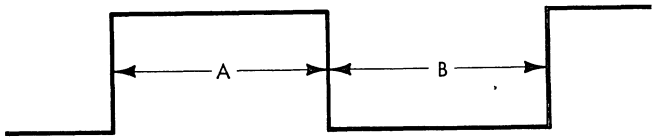
Singleshot	Duration	Pin Location	System Diagram
Top Pot	5 milliseconds	D-A1J3B03	ES281
Bottom Pot	30 milliseconds	D-A1J3B07	ES181

28115

Figure 4-3. 1054–1055 Singleshots

4.7.3 Oscillator Adjustment

While scoping the oscillator flip-flop output (D-A1F3B09, system diagram page ES242), adjust the two pots on the oscillator card (D-A1G6) for a symmetrical waveform as shown:



A = B = approximately 4.2 ms

28116

4.8 1442 ADAPTER

4.8.1 Service Check

Diagnostic program 080F is a monitor-controlled function test that verifies correct operation of the 1442 Card Read Punch and adapter circuitry.

Auxiliary program 08A9 tests the operation of the CRP, using the image read mode. Auxiliary program 08AA tests the operation of the CRP, using the 8-8 (packed) read mode.

4.8.2 Singleshot Adjustments

Adjust 'read SS1 gate' and 'punch CB1 gate' singleshots per logic page EN521. For adjustment service hint see paragraph 1.6.2.

4.8.3 Read Emitter Strobe Timing

Adjust read emitter strobe timing per EN70121, items 19 and 20.

4.9 1443 ADAPTER

4.9.1 Service Check

Diagnostic program 080A is a monitor-controlled function test that verifies proper operation of the 1443 Printer and adapter circuitry.

Auxiliary program 08AB checks character selection and ripple registration of the printer.

4.10 1627 ADAPTER

4.10.1 Service Check

Diagnostic program 0805 is a monitor-controlled function test that executes the various movements of the plotter and permits checking of cables for correct adjustment.

Auxiliary program 08A6 is a registration exerciser. Auxiliary program 08A7 is a stress exerciser.

4.10.2 Plotter Speed

Plotter speed is not adjustable. If, for any reason, there is a need to change the speed of the plotter, contact Plant FE Technical Operations (San Jose).

4.11 1810 DISK STORAGE

Service checks, adjustments, and removals for the 1810 Disk Storage are in the Field Engineering Theory-Maintenance, *IBM 1810 (2310) Disk Storage, Models A and C.* (See *FE Bibliography - - 1800 System,* Order No. SY26-0560.)

Service Check

Diagnostic program 0809 is a monitor-controlled function test of the 1810 Disk Storage and adapter circuitry.

4.12 MAGNETIC TAPE CONTROL (1802 ONLY)

4.12.1 Service Check -- Tape Control Unit

Diagnostic program 0807 is a monitor-controlled function test that checks for proper operation of the magnetic tape control.

Diagnostic program 080B is a monitor-controlled function test that verifies the ability of tape units to write varying length records and read them back correctly on the same or another drive.

Diagnostic program 08B9 is a non-monitor timing test that verifies proper adjustment of the magnetic tape drive.

Diagnostic program 08BD is a non-monitor function test that verifies proper operation of the tape error correction function.

No auxiliary programs are available for the TCU because it cannot be operated in CE mode.

4.12.2 Oscillator Timing

The oscillators listed in Figure 4-4 provide drive pulses to operate the control clocks for character densities of 200 bpi (bytes per inch), 556 bpi, and 800 bpi and to provide motion control for 112.5-ips (inches per second), 75.0-ips, and 37.5-ips tape units.

4.12.3 Service Check - - Read Clock Timing

The read clock consists of three binary flip-flops stepping in a cyclic fashion. (For each stepping pulse only one flip-flop changes state.) Figure 4-5 lists specifications for the gated outputs.

Oscillator	Type	Period (μsec)		Function
		Nominal	Limits	
5.0 kc	Xtal	200.0	199.8-200.2	DC Msec Control
1.0 mc	Gated	1.0000	0.9174-1.0526	RC 556 BPI
1.0 mc	Xtal	1.0000	0.9990-1.0010	WC, DC μsec Control 556 BPI
1.44 mc	Xtal	0.6944	0.6938-0.6951	WC, DC μsec Control 800 and 200 BPI
1.40 mc	Gated	0.7143	0.6557-0.7519	RC 800 and 200 BPI

24137A

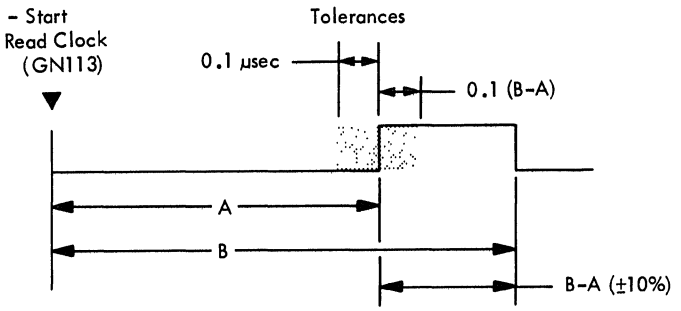
Figure 4-4. Tape Control Unit Oscillators

4.12.4 Service Check - - Write Clock Timing

The write clock consists of four binary flip-flops stepping in a cyclic fashion. (For each stepping pulse only one flip-flop changes state.) Figure 4-6 lists specifications for the gated outputs.

4.12.5 Service Check - - Delay Counter Timing

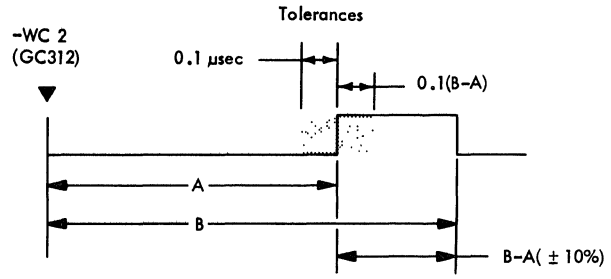
The delay counter consists of nine binary flip-flops stepping in a cyclic fashion. (For each stepping pulse only one flip-flop changes state.) Figures 4-7 and 4-8 list specifications for the gated output in microsecond and millisecond modes.



Read Clock Signal	Logic Page	Pulse Timing in Microseconds by Tape Unit Model		
		Model 1	Model 2	Model 3
800 BPI		Start (A) - End (B)	Start (A) - End (B)	Start (A) - End (B)
RC 0 and 1	GC232	0 - 4.2	0 - 2.1	0 - 1.4
RC 2	GC232	4.2 - 6.4	2.1 - 3.2	1.4 - 2.1
RC 4 Not Check Char	GM213	8.6 - 10.8	4.3 - 5.4	2.9 - 3.6
RC 6	GC232	12.8 - 15.0	6.4 - 7.5	4.3 - 5.0
RC 7	GC232	15.0 - 15.4	7.5 - 7.9	5.0 - 5.4
RC Reset Read	GC232	15.4 - 15.7	7.9 - 8.2	5.4 - 5.7
Skew Gate and RC Reset Write	GC232	21.4 - 21.7	10.7 - 11.0	7.1 - 7.4
Skew Gate Set	GC233	10.8 - 12.8	5.4 - 6.4	4.3 - 5.0
556 BPI				
RC 0 and 1	GC232	0 - 6.0	0 - 3.0	0 - 2.0
RC 2	GC232	6.0 - 9.0	3.0 - 4.5	2.0 - 3.0
RC 4 Not Check Char	GM213	12.0 - 15.0	6.0 - 7.5	4.0 - 5.0
RC 6	GC232	18.0 - 21.0	9.0 - 10.5	6.0 - 7.0
RC 7	GC232	21.0 - 21.4	10.5 - 10.9	7.0 - 7.4
RC Reset Read	GC232	21.4 - 21.7	10.9 - 11.2	7.4 - 7.7
Skew Gate and RC Reset Write	GC232	30.0 - 30.3	15.0 - 15.3	10.0 - 10.3
Skew Gate Set	GC233	12.0 - 15.0	6.0 - 7.5	4.0 - 5.0
200 BPI				
RC 0 and 1	GC232	0 - 16.8	0 - 8.4	0 - 5.6
RC 2	GC232	16.8 - 25.2	8.4 - 12.6	5.6 - 8.4
RC 4 Not Check Char	GM213	34.6 - 43.0	17.3 - 21.5	11.5 - 14.3
RC 6	GC232	51.6 - 60.0	25.8 - 30.0	17.2 - 20.0
RC 7	GC232	60.0 - 60.4	30.0 - 30.4	20.0 - 20.4
RC Reset Read	GC232	60.4 - 60.7	30.4 - 30.7	20.4 - 20.7
Skew Gate and RC Reset Write	GC232	85.2 - 85.5	42.6 - 42.9	28.4 - 28.7
Skew Gate Set	GC233	34.6 - 43.0	17.3 - 21.5	11.5 - 14.3

24138A

Figure 4-5. Read Clock Timings



All timings measured at 10% and 90% points

Write Clock Signal	Logic Page	Pulse Timing in Microseconds by Tape Unit Model		
		Model 1	Model 2	Model 3
800 BPI		Start (A) - End (B)	Start (A) - End (B)	Start (A) - End (B)
WC 5	GC312	6.3 - 8.4	3.1 - 4.2	2.1 - 2.8
WC 8 and 9	GC312	12.6 - 16.8	6.3 - 8.4	4.2 - 5.6
Write Pulse (WC 6-10)	GC312	8.4 - 18.9	4.2 - 9.4	2.8 - 6.3
WC 14 and 15	GC312	24.9 - 29.1	12.5 - 14.6	8.3 - 9.7
WC 2	GC312	33.3 - 35.4	16.7 - 17.7	11.1 - 11.8
556 BPI				
WC 5	GC312	9.0 - 12.0	4.5 - 6.0	3.0 - 4.0
WC 8 and 9	GC312	18.0 - 24.0	9.0 - 12.0	6.0 - 8.0
Write Pulse (WC 6-10)	GC312	12.0 - 27.0	6.0 - 13.5	4.0 - 9.0
WC 14 and 15	GC312	36.0 - 42.0	18.0 - 21.0	12.0 - 14.0
WC 2	GC 312	48.0 - 51.0	24.0 - 25.5	16.0 - 17.0
200 BPI				
WC 5	GC312	25.2 - 33.6	12.4 - 16.8	8.4 - 11.2
WC 8 and 9	GC312	50.4 - 66.8	25.2 - 33.6	16.8 - 22.4
Write Pulse (WC 6-10)	GC312	33.6 - 75.6	16.8 - 37.6	11.2 - 25.2
WC 14 and 15	GC312	99.6 - 116.4	50.0 - 58.4	33.2 - 38.8
	GC312	133.2 - 141.6	66.8 - 70.8	44.4 - 47.2

24139B

Figure 4-6. Write Clock Timings

4.12.6 Service Check -- Signal Acceptance and Rejection Levels

The signal acceptance and rejection levels shown in Figure 4-9 are the criteria for correct operation of the final amplifiers. The signal levels of each channel are measured by scoping the output of the final amplifier (high and low clip pulse lines) shown on GD111, 112, and 113. For the read operation, a master signal-level tape (P/N 432152) should be run to obtain a standard amplitude signal.

4.12.7 Singleshot Adjustment

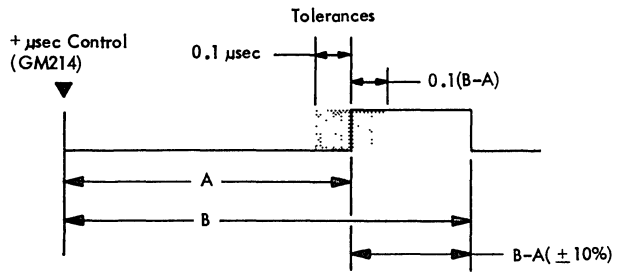
Adjust singleshots with CE alignment screwdriver, P/N 460811. Adjust each singleshot duration to that specified in the system diagrams. Figure 4-10 is a list of magnetic tape control singleshots, their durations, limits, pin locations, and logic page locations.

For adjustment service hint see paragraph 1.6.2.

4.12.8 Final Amplifier Read/Write Adjustment

If a TCU final amplifier card (P/N 5807218 or 5806835) is replaced, all the following checks and adjustments must be performed. All voltages are to be measured with a Weston 901 meter (0.5% accuracy) or equivalent.

For these checks and adjustments, the tape unit must be attached with power on, and there must be no signal input to the amplifier (tape not moving). Room temperature must be between 60° F and 90° F.

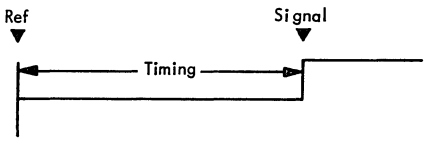


Delay Signal		Logic Page	Timings in Microseconds by Tape Unit Model		
			Model 1	Model 2	Model 3
800 BPI			Start (A) - End (B)	Start (A) - End (B)	Start (A) - End (B)
WDD 19-26	(Shift CRCR)	GN123	39.6 - 56.1	19.8 - 28.1	13.2 - 18.7
WDD 47-78	(Write CRC Char)	GN123	97.8 - 164.4	48.9 - 82.2	32.6 - 54.8
WDD 47-78	(Set WR Pulse Control)	GM132	97.8 - 164.4	48.9 - 82.2	32.6 - 54.8
WDD 95-159	(Set WR Pulse Control)	GM132	198.0 - 331.2	99.0 - 165.6	66.0 - 110.4
WDD 51-58	(Write Pulse CRCR)	GM131	106.2 - 123.0	53.1 - 61.5	35.4 - 41.0
WDD 53	(Write LRC Char)	GM131	(112.3-113.0) *	(56.5-57.2) *	(37.9-38.6) *
WDD 117	(Write LRC Char)	GM131	(247.1-247.8) *	(124.1-124.8) *	(83.1-83.8) *
WDD 403	(End WDD 117 + 286)	GM131	------	------	280.0
RDD 19-36	(Lost Character)	GN122	40.0 - 75.0	20.0 - 37.5	13.3 - 25.0
RDD 36-37	(Set 1st Check Character)	GN123	75.0 - 79.2	37.5 - 39.6	25.0 - 26.4
RDD 95-158	(Set 2nd Check Character)	GN123	198.0 - 330.0	99.0 - 165.0	66.0 - 110.0
RDD 159-162	(EPR to Skew Reg)	GN121	330.0 - 339.0	165.0 - 169.5	110.0 - 113.0
RDD 164-165	(Reset EPR)	GN122	342.0 - 346.2	171.0 - 173.1	114.0 - 115.4
RDD 167-170	(Set 1 in EPR)	GN121	348.0 - 356.4	174.0 - 178.2	116.0 - 118.8
RDD 159-222	(Gate to find track)	GN121	330.0 - 465.0	165.0 - 232.5	110.0 - 155.0
RDD 159-175	(Sample LRCR-CRCR)	GM133	330.0 - 366.6	165.0 - 183.3	110.0 - 122.2
RDD 383	(Op Complete)	GM133	798.0	399.0	266.0
556 BPI					
WDD 47-78	(Set WR Pulse Control)	GN123	14.1 - 247.0	70.5 - 123.5	47.0 - 79.0
WDD53	(End WDD and Write LRCR)	GM131	(160.0-161.0) *	(80.5-81.5) *	(54.0-55.0) *
RDD 19-36	(Lost Character)	GN122	57.0 - 108.0	28.5 - 54.0	19.0 - 36.0
RDD 36-37	(Set 1st Check Char)	GN123	108.0 - 114.0	54.0 - 57.0	36.0 - 38.0
RDD 95-158	(Set 2nd Check Char)	GN123	285.0 - 477.0	142.5 - 238.5	95.0 - 159.0
RDD 159-175	(Sample LRCR)	GM133	477.0 - 525.0	238.5 - 262.5	159.0 - 175.0
RDD 383	(Op Complete)	GM133	1149.0	574.4	383.0
200 BPI					
WDD 47-78	(Set WR Pulse Ctrl)	GN123	391.2 - 651.6	195.6 - 325.8	130.4 - 217.2
WDD 53	(End WDD & Write LRCR)	GM131	(447.1-447.8) *	(223.9-224.6) *	(149.5-150.2) *
RDD 19-36	(Lost Character)	GN122	160.0 - 300.0	80.0 - 150.0	53.2 - 100.0
RDD 36-37	(Set 1st Check Char)	GN123	300.0 - 316.8	150.0 - 158.4	100.0 - 105.6
RDD 95-158	(Set 2nd Check Char)	GN123	742.0-1320.0	396.0 - 660.0	264.0 - 440.0
RDD 159-175	(Sample LRCR)	GM133	1320.0-1466.0	660.0 - 733.2	440.0 - 488.8
RDD 383	(Op Complete)	GM133	3192.0	1596.0	1064.0

*Limits of start time

24140C

Figure 4-7. Delay Counter Timings - - Microsecond Mode



Delay Signal	Logic Page	Function	Reference	Timings in Milliseconds 9-Track	Timings in Milliseconds 7-Track
Model 3 Tape Unit				Min. Max.	Min. Max.
End WDD	GM 131	Reset Go on Write	+ MS Control GM214	See Note 1	1.7 - 2.0
D31 or 53 MS not LP	GM132	End WD not LP	Rise of Go GM215	5.2 - 5.8	5.2 - 5.8
D160 TA	GM133	Set Go in Backspace	+ MS Control GM214	15.9 - 17.6	15.9 - 17.6
D96 TA	GM133	Set Bkwd RD or WR	+ MS Control GM214	9.5 - 10.3	9.5 - 10.3
End Read Delay	GM132	End RD not LP	Rise of Go GM215	1.4 - 1.6	2.7 - 3.1
		End RD Backspace	Rise of Go GM215	1.1 - 1.3	1.1 - 1.3
		End RD LP	Rise of Go GM215	15.9 - 17.6	15.9 - 17.6
Bksp Reset Rd Cond.	GM131	Reset Rd. Cond & Go on Bksp	+RDD GM213	0.6 - .8	1.9 - 2.2
WD 320	GM133	End WD OP	Rise of Go GM215	31.9 - 35.2	31.9 - 35.2
WD 32	GM132	Set Read Cond On	Rise of Go Write	3.1 - 3.5	3.1 - 3.5
Mode 2 Tape Unit					
End WDD	GM131	Reset Go on Write	See Note 2	Check Char	Check Char
D31 or 53 MS not LP	GM132	End WD not LP	Rise of Go GM215	6.1 - 6.8	6.1 - 6.8
D160 TA	GM133	Set Go in Bksp	+MS Control GM214	31.9 - 35.2	31.9 - 35.2
D96 TA	GM133	Set Bkwd RD or Wr	+ MS Control GM214	19.1 - 21.1	19.1 - 21.1
End Read Delay	GM132	End RD not LP	Rise of Go GM215	3.4 - 3.7	6.1 - 6.8
		End RD Bksp	Rise of Go GM215	1.5 - 1.6	1.5 - 1.6
		End RD LP	Rise of Go GM215	20.5 - 22.7	20.5 - 22.7
Bksp Reset Rd Cond	GM131	Reset Rd. Cond & Go on Bksp	+RDD GM213	2.1 - 2.4	4.1 - 4.6
WD 320	GM133	End WD LP	Rise of Go GM215	63.9 - 70.4	63.9 - 70.4
WD 17	GM214	Set Read Cond on Write	Rise of Go GM215	3.3 - 3.7	3.3 - 3.7
Model 1 Tape Unit					
End WDD	GM131	Reset Go on Write	See Note 2	Check Char	Check Char
D31 or 53 MS not LP	GM132	End WD not LP	Rise of Go GM215	12.3 - 13.6	12.3 - 13.6
D160 TA	GM133	Set Go in Bksp	+ MS Control GM214	63.9 - 70.4	63.9 - 70.4
D96 TA	GM133	Set Bkwd RD or WR	+ MS Control GM214	38.3 - 42.2	38.3 - 42.2
End Read Delay	GM132	End RD not LP	Rise of Go GM215	6.7 - 7.5	12.3 - 13.6
		End RD Bksp	Rise of Go GM215	1.9 - 2.2	1.9 - 2.2
		End RD LP	Rise of Go GM215	41.1 - 45.3	41.1 - 45.3
Bksp Reset Rd Cond	GM131	Reset Rd Cond & Go on Bksp	+RDD GM213	5.5 - 6.2	9.5 - 10.6
WD 320	GM133	End WD LP	Rise of Go GM215	127.9 - 140.8	127.9 - 140.8
WD 17	GM214	Set Read Cond on Write	Rise of Go GM215	6.7 - 7.5	6.7 - 7.5

Notes 1: End WDD for 9-track model 3 occurs with **WDD 403.**
2: WDD ends with the reset of write release, Go falls with the set of first check characters with Model 1 or Model 2.

24141B

Figure 4-8. Delay Counter Timings - - Millisecond Mode

Operation	Acceptance Levels (Minimum Volts, p-p)		Rejection Levels (Maximum Volts, p-p)	
	7-Track	9-Track	7-Track	9-Track
High-Clip Write	3.25	3.25	2.75	2.75
High-Clip Read	2.75	2.25	2.25	1.75
Low-Clip Read	1.55	——	1.05	——

14178

Figure 4-9. Signal Acceptance and Rejection Levels

Single-Shot (See Note)	Duration (Nanoseconds)		Pin Location	Logic Page
	Nominal	Limits		
R-W Check Gate (U)	200	180-220	B3 H2B02	GC113
Gate Byte A (L)	350	315-385	B3 H2D02	GC113
R-W Gate (U)	300	270-330	B3 C2B02	GC111
Reset R-W Register (L)	150	135-165	B3C2D02	GC111
RC 7 (U)	350	315-385	A2L3B02	GC232
RC Reset (L)	350	315-385	A2L3D02	GC232
DC Reset (U)	350	315-385	A2C6B02	GM124
Read Clock VRC (L)	200	180-220	A2C7D02	GE221
Write Clock VRC (U)	200	180-220	A2C7B02	GE231
Delay Counter VRC (L)	200	180-220	A2C6D02	GE241

Note: Letters refer to pot position on card (U = Upper, L = Lower)

14104B

Figure 4-10. Magnetic Tape Control Singleshots

The I/O monitor unit may be attached to indicate signal status at each step of the adjustment procedure.

Integrator Voltage Level Check:

1. Voltage from D-B3C4D05 to dc common should measure +3.5V (±10%) if model 1 or 2 tape unit is attached.
2. Voltage from D-B3C4D05 to dc common should measure +12V (±10%) if model 3 tape unit is attached.
   If voltage is incorrect, replace the card (P/N 5807219) at D-B3C4 and recheck voltage.

Low-Clip "Fixed" Setting, Seven-Track Read: Disregard this check if seven-track feature is not installed.

1. Press reset key on P-C console or I/O monitor unit.
2. Measure voltage between D-B3C5B03 (−12V) and the following emitter test points (shown on GD111, 112, 113). All readings must be within 0±0.02 Vdc.

   D-B3C5D07 D-B3F5D07 D-B3J5D07
   D-B3D5D07 D-B3G5D07 D-B3K5D07
   D-B3E5D07 D-B3H5D07 D-B3L5D07

3. If the reading on any card is not within the limits of 0±0.02 Vdc, replace the card (P/N 5806835), then recheck the voltage at its test point.

High-Clip "Fixed" Setting, Nine-Track Read:

1. Connect jumper between D-B3M5D13 (GB114) and dc common.
2. Press reset key on P-C console or I/O monitor unit.
3. Measure voltage between D-B3C5B03 (−12V) and the following emitter test points. If all readings are within 0.6 to 1.2 Vdc, proceed to "High-Clip Adjustment, Seven-Track Read."

   D-B3C5B09 D-B3F5B09 D-B3J5B09
   D-B3D5B09 D-B3G5B09 D-B3K5B09
   D-B3E5B09 D-B3H5B09 D-B3L5B09

4. If the reading on any card is not within the limits of 0.6 to 1.2 Vdc, replace the card (P/N 5806835). Then remove the jumper (step 1) and repeat checks and adjustments, beginning with "Low-Clip 'Fixed' Setting, Seven-Track Read."

High-Clip Adjustment, Seven-Track Read: Disregard this adjustment if seven-track feature is not installed.

1. Remove jumper between D-B3M5D13 and dc common. Connect jumper between D-B3M5D12 and dc common.
2. Press reset key on P-C console or I/O monitor unit.
3. Connect voltmeter (+) lead to D-B3C5B09 and (−) lead to D-B3C5B03 (−12V).
4. Adjust upper pot on card at D-B3C4 until the meter reads 1.75V. If this is not possible, replace card (P/N 5807219) at D-B3C4 and adjust upper pot for 1.75V.
5. Measure voltage between D-B3C5B03 (−12V) and the following emitter test points. All readings must be within 1.65 to 1.85 Vdc.

   D-B3C5B09 D-B3F5B09 D-B3J5B09
   D-B3D5B09 D-B3G5B09 D-B3K5B09
   D-B3E5B09 D-B3H5B09 D-B3L5B09

6. If all readings are within the limits of 1.65 to 1.85 Vdc, proceed to "Write Adjustment." If any reading is outside these limits, determine the voltage spread between the lowest and highest readings.
   a. If the maximum spread is within 0.2V, adjust the upper pot on card at D-B3C4 to bring all output readings (step 5) within the specified range.
   b. If the maximum spread is greater than 0.2V, record the readings, then delete only those readings

necessary to bring the spread of the remaining readings within 0.2V. Replace the cards (P/N 5806835) in the channels whose readings were deleted. Then remove the jumper (step 1) and repeat the entire adjustment procedure, beginning with "Low-Clip 'Fixed' Setting, Seven-Track Read."

Write Adjustment:

1. Remove jumper between D-B3M5D12 and dc common. Connect jumper between D-B2E5B13 (GB341) and dc common.
2. Press reset key on P-C console or I/O monitor unit.
3. Connect voltmeter (+) lead to D-B3C5B09 and (–) lead to D-B3C5B03 (–12V).
4. Adjust lower pot on card at D-B3C4 (level-setter) until the meter reads 2.5V. If this is not possible, replace card (part 5807219) at D-B3C4 and adjust for 2.5V, then repeat adjustments, beginning with "High-Clip Adjustment, Seven-Track Read."
5. Measure voltage between D-B3C5B03 (–12V) and the following emitter output pins. All readings must be within 2.4 to 2.6 Vdc.

D-B3C5B09	D-B3F5B09	D-B3J5B09
D-B3D5B09	D-B3G5B09	D-B3K5B09
D-B3E5B09	D-B3H5B09	D-B3L5B09

6. If all readings are within the limits of 2.4 to 2.6 Vdc, proceed to step 7. If any reading is outside these limits, determine the voltage spread between the lowest and highest readings.
   a. If the maximum spread is within 0.2V, adjust the lower pot on the card at D-B3C4 to bring all output readings (step 5) within the specified range.
   b. If the maximum spread is greater than 0.2V, record the readings, then delete only those readings necessary to bring the spread of the remaining readings within 0.2V. Replace the cards (P/N 5806835) in the channels whose readings were deleted. Then remove the jumper (step 1) and repeat the entire adjustment procedure, beginning with "Low-Clip 'Fixed' Setting, Seven-Track Read."
7. Remove jumper between D-B2E5B13 and dc common.
8. Run diagnostic program 0807. If test does not perform correctly, check signal acceptance and rejection levels (paragraph 4.12.6).

4.13 SYSTEM/360 ADAPTER

4.13.1 Service Check

Diagnostic programs test the operation of I/O commands, status indicators, data buffer, drivers, and gating controls.

Description

1. PID 08CD enables the CE to test the 1800 side of the adapter while it is off-line to the System/360 channel. The System/360 reset line has to be tied down on the 1826 boards to run this test.
2. PID F4D4 may be used to test the System/360 side of the adapter when the 1800 channel has been reterminated or has bypassed the System/360 adapter feature by means of special jumper boards (P/N 2242726). Routines A and B of this section test the transfer of data between the two systems provided that tiedown jumpers are installed as called for on the System/360 printouts when execution of these routines is called for by setting section switch 2 or by instructing the diagnostic monitor to cycle routines A, B, or A and B.
3. PID's 08CE for the 1800 and E4D5 for the System/360 running concurrently, will test all the functions of the adapter. The System/360 CPU must have available 16k bytes of storage for this test and requires the use of DMA 4, DMA 8-9, DME, or DM44. PID 08CE does not use the 1800 monitor, but uses the relocatable loader.

4.13.2 Singleshot Adjustments

Adjust the 'transfer' singleshot and the 'tag sample' singleshot per the following procedure. Use the CE alignment screwdriver, P/N 460811.

1. Refer to FY141 and connect a jumper from 26A-B3F2D11 to 26A-B3L3D10. With P-C clock running, scope pin 26A-B3L3B13 and adjust *bottom* pot on card at 26A-B3L3 so that 'tag sample' pulse (negative) is 300 (±30) nanoseconds wide.
2. Refer to FY201 and connect a jumper from 26A-B3F2D11 to 26A-B3L3B07. Scope pin 26A-B3L3D13 and adjust *middle* pot on card at 26A-B3L3 so that 'transfer SS' pulse (negative) is 300 (±30) nanoseconds wide.
3. Refer to FV250 and connect a jumper from 26A-B3F2D11 to 26A-B3L3D02. Scope pin 26A-B3L3D12 and adjust the *top* pot on card at 26A-B3L3 so that the output pulse (negative) is 300 (±30) nanoseconds wide.
4. Remove jumpers attached in steps 1, 2, and 3.
5. While running PID 08CD, do the following:
   a. Scope pin 26A-A3H7B07 and adjust bottom pot on card at 26A-A3H7 for a 30-millisecond negative pulse.
   b. Scope pin A26-A3H7B03 and adjust top pot on card at 26A-A3H7 for a 30-millisecond negative pulse. (Refer to ALD FW902 for preceding adjustments.)

4.14 ANALOG INPUT

4.14.1 Precautions

1. Do not remove or install a card in the 1851 Multiplexer Terminal with system power on.

2. If common-mode voltage in excess of 10 volts (ac or dc) is present on the customer input lines, or if there is a possibility of the occurrence of such voltage, the lines must be disconnected by the customer prior to removal or insertion of the multiplexer relay card in that channel. Mercury bridging of the relay points during removal or insertion of the card may impress the entire common-mode voltage across the flying capacitor, relay points, or amplifier, resulting in component damage.
3. Multiplexing cards and amplifier cards in the 1851 units must be kept dry and free from contamination. Do not allow the protective coating on the cards to become damaged.
4. Handle the cards only by the edges. Fingerprints, pencil marks, and other contaminants will decrease the leakage resistance of the cards and impair the accuracy of the analog input subsystem.
5. Do not use cleaning solvents on cards or components in the low-level circuits.

4.14.2 Service Checks

Diagnostic program 0821 is a monitor-controlled function test that checks the analog input feature under two-data-channel (random) control.

Diagnostic program 0822 is a monitor-controlled function test that checks the analog input feature under single-data-channel (sequential) control.

Diagnostic program 0823 is a monitor-controlled function test that checks the analog input feature under direct program control.

Accuracy and Repeatability

Specifications for system accuracy and repeatability are given in the *IBM Data Acquisition and Control System Installation Manual -- Physical Planning.* (See *FE Bibliography -- 1800 System,* Order No. SY26-0560.) Accuracy and repeatability can be checked with diagnostic program 0823.

4.14.3 Analog Input Calibration

The ADC calibration procedure is given on system diagram QD810. The differential amplifier calibration procedure is given on QD815. The following reference drawings are provided: ADC analog board on QD935, differential amplifier on QC935, sample-and-hold amplifier on QD931. Information on the AI calibration facility is given in paragraph 2.12.2.

4.14.4 Singleshot Adjustments

The analog input singleshot adjustment procedures are given on system diagram QD930. Adjust singleshots with the CE alignment screwdriver, P/N 460811.

For adjustment service hint see paragraph 1.6.2.

4.14.5 Resistance Bulb Thermometer (1851 Model 2)

The RBT assembly is mounted on the rear surface of the isothermal terminal block. The resistive element is sealed in a tubular metal case and the leads are brought out to a terminal plate. Padder resistors are mounted on the underside of the terminal plate and are factory calibrated to make the RBT fit a linear resistance-temperature curve.

The RBT circuit requires no service or adjustment during normal operation. If circuit failure occurs, matching elements may be changed without affecting accuracy. However, the RBT element and its padder resistors mounted on the isothermal block are a matched set, and failures in any one of the components therein will require replacement of the entire set.

A check to verify correct operation of the RBT, the analog input path, and the ADC can be made as follows:

1. With the ADC, read the RBT output voltage V_{rbt} (the second address in the 1851-2 containing the RBT) and record this value.
2. With the ADC, read the RBT reference voltage V_{ref} (the first address in the 1851-2 containing the RBT) and record this value.
3. Using one of the following formulas, determine the temperature of the 1851-2 isothermal terminal block.

$$T_{rbt}(^{o}F) = 51.876 \frac{V_{rbt}}{V_{ref}} + 41.0$$

$$T_{rbt}(^{o}C) = 28.82 \frac{V_{rbt}}{V_{ref}} + 5.0$$

The computed temperature should be within approximately 10°F of the room in which the 1851-2 is installed.

4.15 ANALOG OUTPUT

4.15.1 Service Check

Diagnostic program 0826 is a monitor-controlled function test that exercises and tests the reliability of the AO registers in all modes. Proper operation is verified by scoping.

4.15.2 Analog Output Calibration

Analog output calibration is performed using the Fluke 885/AA Precision Voltmeter obtainable from the area ICAR center. (See 2.12.1.)

The analog output calibration procedure is given on system diagram TA002. A reference drawing for this calibration is provided on TA004.

4.15.3 1856 Blower Removal/Replacement

The two blower assemblies in the rear compartment of the 1856 must be removed for access to terminals and connectors.

Removal

1. Remove ac power to the 1856 unit.
2. Disconnect blower power connector located above blower assembly.
3. Support blower assembly with one hand and disconnect the two quarter-turn fasteners by turning counterclockwise with a screwdriver.
4. Using care not to bend or loosen any connectors, pull blower assembly straight back.

Replacement

The blower assemblies rest against some of the cables in the rear of the 1856. All cables must be properly positioned before the blower assembly is installed.

1. Insert the blower power plug.
2. Carefully insert the blower assembly so that the blower exhaust ports enter the 1856 plenums.
3. Secure the two fasteners (at the top of the assembly) by turning clockwise.
4. Check that no connectors become bent or loosened when the blower assembly is pushed against the flat cables to permit closing the rear cover.

4.15.4 1856 Blower Filter Replacement

Each blower assembly (Figure 4-11) contains a plastic foam filter that wraps around the blower motor.

1. Turn off the 1828 mainline switch.
2. Grasp filter and remove by pulling straight out.

Note: Plastic filters can be cleaned by vacuuming or by washing in warm water that contains a mild soap or detergent. If filters are cleaned by washing, a system of rotation should be set up whereby a thoroughly dry filter is available to replace the one that is presently removed. Filters that are cleaned by vacuuming should be reinstalled so that the direction of air flow is the same as it was before removal. Discard any filter that shows signs of deterioration.

3. Install clean, dry filter by feeding the ends fully into the channels on the blower assembly.

CAUTION
Exercise care that cables under filter are not disturbed.

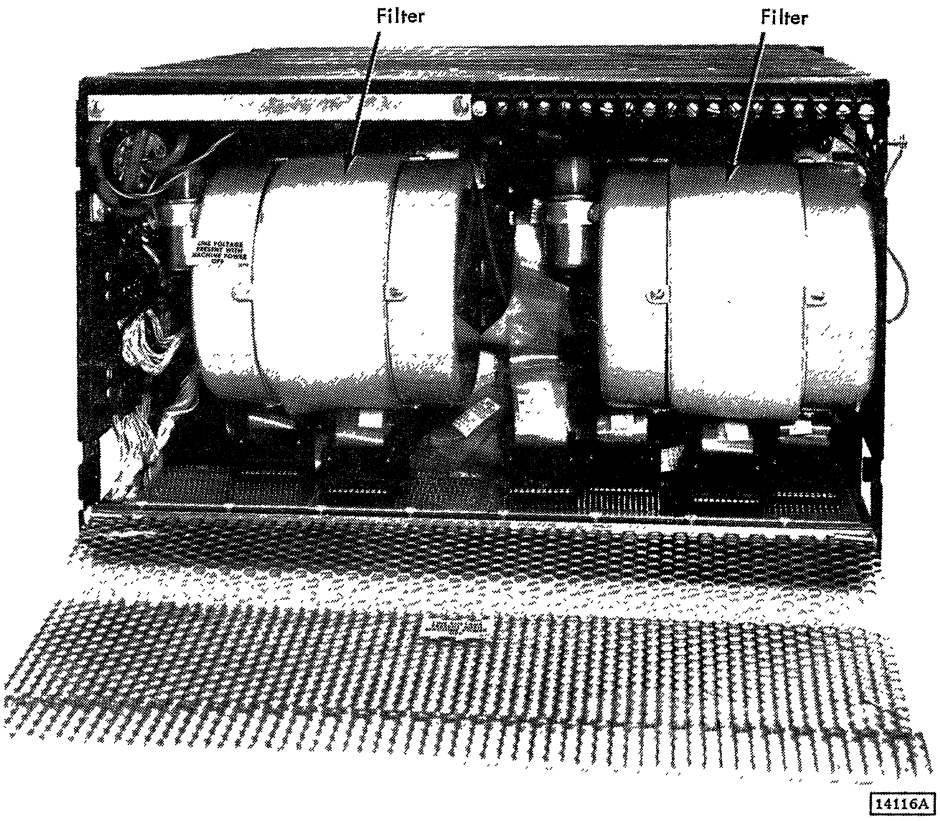


Figure 4-11. 1856 Analog Output Terminal - - Filter Replacement

4.16 DIGITAL INPUT

4.16.1 Service Check - - Digital Input and Process Interrupt

Diagnostic program 0824 is a monitor-controlled function test that checks the operation of digital input features under data-channel control.

Diagnostic program 0825 is a monitor-controlled function test that checks operation of digital input features under direct program control.

The digital-input test card (paragraph 2.12.3) is used with each of these tests to provide a known input bit configuration.

4.16.2 Service Check - - Pulse Counter

Diagnostic program 08C8 (I/O scope routine) is used in conjunction with the programmable CE test pulse (2.9) to check pulse counter operation.

4.17 DIGITAL OUTPUT

4.17.1 Service Check

Diagnostic program 0827 is a monitor-controlled function test that exercises the digital output registers in all modes.

The digital-output test cable (2.12.4) is used with the function test to permit displaying the DO group (16 bits) on the I/O monitor unit.

4.17.2 Singleshot Adjustments

Adjust singleshots with CE alignment screwdriver, P/N 460811. Adjust each singleshot duration to that specified in the system diagram. Figure 4-12 is a list of digital output singleshots, their durations, limits, pin locations, and logic page locations.

For adjustment service hint see paragraph 1.6.2.

4.18 SELECTOR CHANNEL

4.18.1 Service Check

The following monitor-controlled function tests are provided for checking the operation of the selector channel:

Single-Shot	Duration		Pin Location	Logic Page
	Nominal	Limits		
PO Busy (Lower Pot)	1.5 ms	1.35-1.65 ms	B3 E3 D04	PB 051
PO Busy Reset (Lower Pot)	1.5 ms	1.35-1.65 ms	B3 E4 D04	PB 051
PO Reset (Upper Pot)	1.5 μsec	1.35-1.65 μsec	B3 E2 B02	PB 051

14102 A

Figure 4-12. Digital Output Singleshots

0810 - Selector channel function test
0811 - 2841 function test
0812 - 2311 function test
0813 - Two-channel switch function test
0814 - CE pack initialization
0892 - 2841/2311 MPX on-line test

4.18.2 Singleshot Adjustments

The selector channel singleshot adjustments are given on system diagram FS011. Adjust singleshots with the CE alignment screwdriver, part number 460811.

4.19 COMMUNICATIONS ADAPTER

4.19.1 Service Check

The following monitor-controlled function tests are provided for checking the operation of the communications adapter:

080E - Communications adapter Wraparound
080D - Communications adapter transmit/receive
0891 - Communications adapter MPX on-line test

4.19.2 Adjustments

No adjustments are required for the communications adapter feature.

Chapter 5. Power Supplies

Power on/off sequencing for the 1800 system is described in the *FE Theory of Operation, Processor-Controller,* and is shown graphically in the maintenance diagram manual (FEMDM).

Section 1. Basic Unit

The 1800 system operates from one three-phase mainline power cord. The primary voltage input is 208/230 Vac (+10%; -8%) at 60 Hz, or 195/220/235/380/408 Vac (+10%; −8%) at 50 Hz.

Primary power enters the 1801 or 1802 through a line filter and a 50-amp mainline power circuit breaker (CB1) and is sequenced to all system units except the 1053 Printer and the 1816 Printer-Keyboard. The 1053 and 1816 have their own mainline power cords.

For all normal maintenance operations, the circuit breakers on the 1801 or 1802 power sequence box are left on and the system is powered up and down from the on and off switches on the programmer's console. The circuit breakers are provided for isolation of branch circuit overloads, but they may also be tripped manually as a safeguard against power being restored to a unit that has been shut down for servicing.

5.1 PRECAUTIONS

1. Before connecting or disconnecting ac power cables in any system unit, remove primary power as directed in paragraph 1.3.2.
2. Before working on any power supply, remove power from the unit and allow at least one minute for capacitors to discharge. Check the dc output voltage with a meter before attempting maintenance.
3. Remove power before replacing power supply regulator cards.
4. Each power supply heat sink is at an electrical potential when power is on. Do not permit heat sinks to become shorted to one another or to the machine frame.
5. Do not defeat the functions of power sequence relays or sense relays by picking them manually or by jumpering the points, as damage to solid-state components may result.
6. Do not operate power supplies without at least 25% rated load. (See 5.5.1.)

5.2 SYSTEM POWER-ON PROCEDURE

1. Check that operations-monitor switch is off.
2. If System/360 adapter is installed, check that System/360 is in a stopped condition.
3. Press the on button. Power-on lamp should light and gate blowers should operate in all units. After a delay of several seconds, the ready lamp should turn on to indicate that dc voltages are present and the system is ready for operation.
4. The lamp-test button may be pressed to check operation of all console indicator (small) lamps.

5.3 SYSTEM POWER-OFF PROCEDURE

1. If System/360 adapter is installed, see 1.3.4.
2. Turn off operations-monitor switch.
3. Press the off button. The off button drops all power in the system with the exception of the 115-Vac convenience outlets and the 24-Vac sequencing voltage. In the 1828 Enclosure, the 115 Vac is used to power the AI calibration facility, and the 24 Vac is used to power the PVR-2 zener reference supply.

5.4 ADJUSTMENT AND REMOVAL PROCEDURES.

With the exception of the 48-Vdc supplies and several special-purpose supplies, the 1800 system uses standard MPS (medium power standard) power supplies. They are housed in vertically mounted tubs at the rear of each unit. Servicing access is by opening the rear cover of the bay and by opening the swinging gates at the front.

5.4.1 MPS Power Supply Adjustment

It will be necessary to adjust a power supply output voltage if the regulator card is replaced or if the setting of the voltage adjustment has been changed for marginal checking purposes (1.4) or as a result of vibration.

Before adjusting or replacing a power supply whose output voltage is incorrect, determine that the input voltage at the primary of the power supply transformer is within +10%, −8% of the nominal value.

An adjustment pot (R1) on each MPS power supply permits adjusting the output voltage at least ±8%. The lock nut on the adjustment shaft should be tight enough to prevent the shaft from turning due to vibration, but not so tight that the shaft cannot be turned with a screwdriver. Tightening the lock nut after adjustment may cause the shaft to turn and change the voltage setting.

Voltages should be adjusted as close as possible to the nominal value and should be measured with a Weston 901 meter (0.5% accuracy), or equivalent, at the points specified on the following logic pages:

1801/1802	YA010
1803	YS240
1826-1 or 2	YB140
1826-3	YB240

Voltage measurements are considered valid only after power has been on for at least 15 minutes to allow temperatures to stabilize.

The output of each MPS power supply is adjusted at installation and will change only slightly with aging of regulator components. A change in output voltage in conjunction with a machine failure is often a result of the failure rather than the cause. Do not attempt to correct the trouble by adjusting the power supply voltage.

5.4.2 MPS Power Supply Removal/Replacement

1. Remove mainline power and take necessary measures to prevent its being restored. Wait at least one minute for capacitors to discharge.
2. Disconnect external leads to the power supply terminal board.
3. Remove the two retaining clips (one at the top, one at bottom) on the exposed ends of the power supply rails. Slide the supply out of the machine.
4. Reverse this procedure to install the supply.

CAUTION

If power supply is being replaced, make certain that correct input transformer is provided (50 or 60 Hz) and that transformer primary is wired correctly for the input voltage.

5.4.3 Power Supply Filter Replacement

Fans are mounted at the bottom of each power supply tub. The fan housing contains a replaceable plastic filter (Figure 5-1) that must be periodically inspected, and replaced as required.

Plastic filters can be cleaned by vacuuming or by washing in warm water that contains a mild soap or detergent. If filters are cleaned by washing, a system of rotation should be set up whereby a thoroughly dry filter is available to replace the one that is presently removed. Filters that are cleaned by vacuuming should be reinstalled so that the direction of

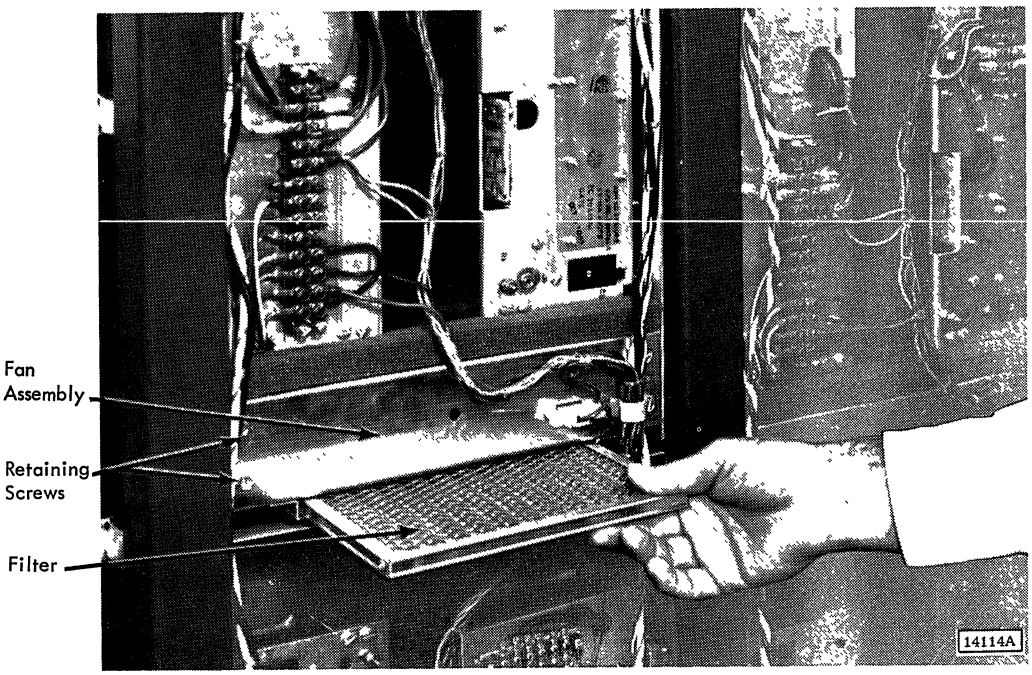


Figure 5-1. Power Supply Fan Assembly and Air Filter

air flow is the same as it was before removal. Discard any filter that shows signs of deterioration.

5.5 TROUBLESHOOTING PROCEDURES

The recommended troubleshooting procedure for 1800 system power malfunctions is shown in Figure 5-2. Figures 5-3 through 5-7 show the dc voltage distribution from power supplies in the various system enclosures. These tables are useful in tracing program-detected failures to a particular power supply.

5.5.1 Power Supply Overload

Problems related to loading of dc power supplies can be analyzed by application of Ohm's law. The minimum load resistance to be expected can be found by dividing the power supply output voltage by the rated output current. For example, a 6V, 4 amp power supply can safely supply power to a load of 1.5 ohms.

The power supply and regulator circuit are designed to accommodate moderate overloads of short duration. If the overload exceeds 25 to 50% of rated load, the overcurrent CB will trip or the fuse in the primary circuit will open. Surge-type overloads usually cause the CB to trip before the fuse opens.

A power supply can be overloaded by any condition that causes excessive current to be drawn from the supply. This could result from a sudden rise in input voltage, failure of the regulator circuit, or a decrease in load resistance.

Some power supplies in the 1800 system have load requirements that vary according to the number of machine features installed. Each of these supplies has the maximum load rating, and the regulator circuit maintains the initial voltage setting over wide variations of load. However, the regulator circuit does not function properly if the supply is operated with less than 25% rated load. To counter this condition, preload resistors are connected in the output circuits of the supplies as described on YA010 (1801/1802) and YB140 (1826).

Section 2. Features

5.6 POWER PAC - - 1856 ANALOG OUTPUT TERMINAL

DC service voltages for the analog output modules are listed in Figure 5-8. These five voltages are supplied by the power pac module, which receives 208V or 230V at 60 Hz (or 220V at 50 Hz) from the power outlet bus in the 1828 Enclosure.

The power pac contains a power on/off switch and two line fuses. Each dc supply has a voltage adjustment screw and an overcurrent fuse mounted adjacent to the voltage test jack on the front of the power pac. The regulator cards (SMS) for each supply voltage are accessible from the front of the power pac and are positioned in the same vertical relationship as the corresponding test jacks.

CAUTION
Turn off power pac switch before replacing regulator cards. Refer to 1.3.2.

5.6.1 Power Pac Voltage Adjustment

DC voltages supplied by the power pac are measured and adjusted on the front panel of the power pac module, using the same procedure outlined for MPS power supplies in 5.4.1.

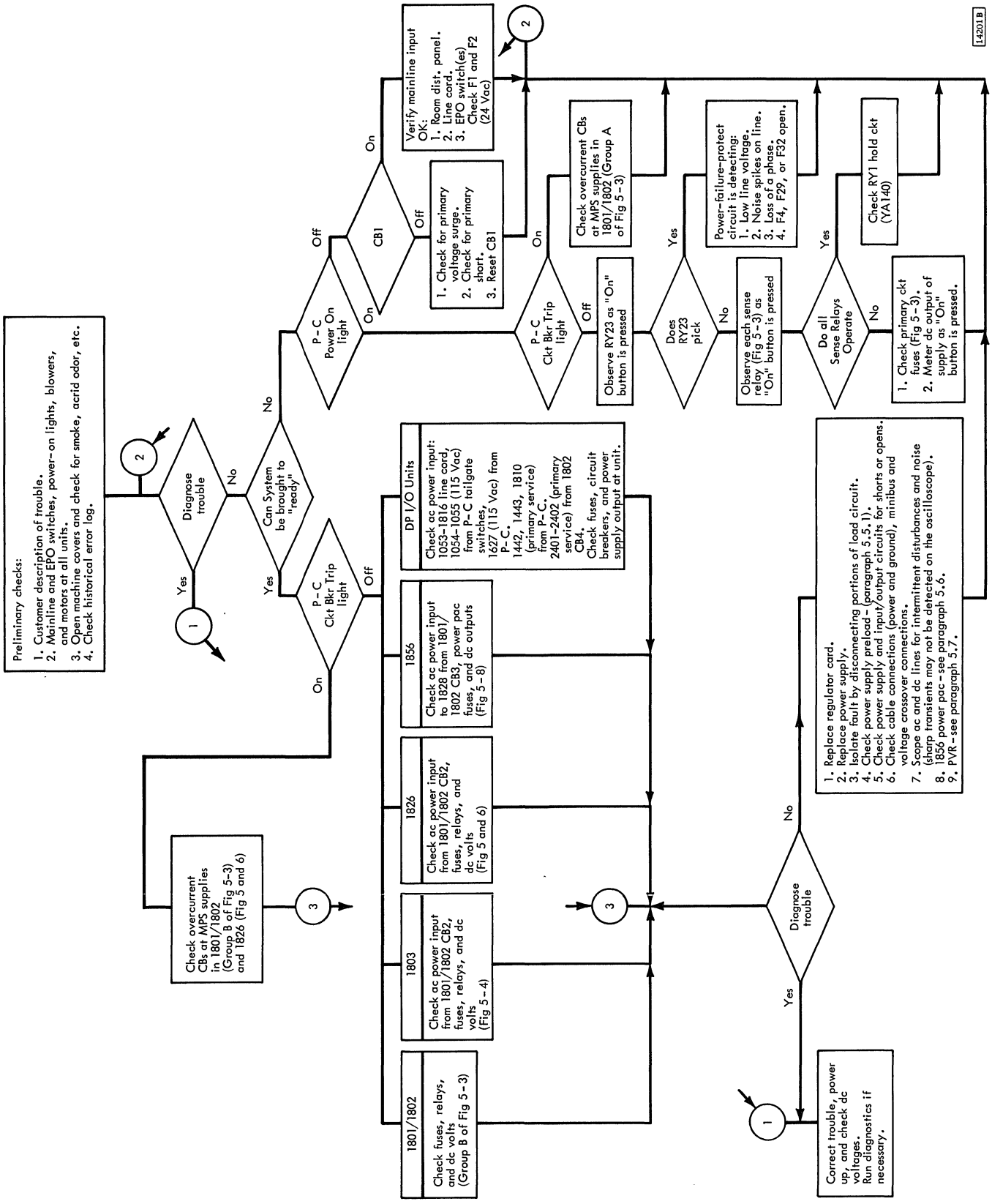
5.7 PRECISION VOLTAGE REFERENCE

The PVR model 1 receives +30V from the power pac module and supplies a +20V (nominal) reference voltage for operation of unipolar digital-analog converters, model 1 and model 2. The PVR model 2 receives +30V and −30V from the power pac module and supplies +20V and −20V (nominal) reference voltages for operation of bipolar digital-analog converters, model 3 and model 4. The PVR-2 also receives 24 Vac from the processor-controller to power a circuit that maintains temperature stability of the zener reference during power-off periods.

Note: From a cold start, a warmup period of approximately 24 hours is required for the zener reference in the PVR-2 before accuracy will meet specifications.

PVR output voltages can be checked at the test jacks on the front of the PVR and DAC modules; however, voltage adjustment must be performed using the analog output calibration procedure given on system diagram TA002.

The PVR short-circuit protect feature (installed on EC 411740) senses either a drop in output voltage or excessive current in the PVR output circuit, and drops the output voltage to zero if either condition exists. To reset the short-circuit protect feature, it is necessary to turn off the power pac ac switch for approximately 5 seconds. When the switch is turned on, PVR output voltage will be restored only if the fault condition has been removed.



● Figure 5-2. Power Supply Troubleshooting Guide

Group (Ref Fig. 5-2)	Power Supply	DC Volts	TB	Pri Ckt via CB1, K1, K2			Sense Relay	1801/1802 Distribution	Other
				K4 F34	F35	F36			
A	1 ⑥	+ 6	12-1			F11	8	Gate A (top bus 8, bottom bus 6 ③④ , 12 ④)SLT diode-gate voltage, MPX solid-state X drivers	1442, I/O monitor, 1851: solid-state block switches
	2	+ 3	13-1			F12	4	Gate C (bus 12) SLT collector voltage; Gate N (console) Lamp Test switch	1442
	3	+ 6	12-3			F13	9	Gate B (bus 6 ③ , 8) diode-gate voltage; Gate Q (CE Panel) CE Sense switches	
	5	+12	12-10	F10			14	Gate A (bottom bus 4 ④) core storage; Gate B (bus 4) core storage and op monitor; Gate C (bus 4) 1627 drivers; Gate D (bus 4) TAU; Gate N switches and message lamps	1054, 1055, 1816, 1053
	7	+ 3	13-3			F16	5	Gate B (bus 12) SLT collector voltage; Gate H I/O channel termination	
	9 ⑥	+ 3	7-13			F31	22	Gate A (top bus 12, bottom bus 8 ④) SLT collector voltage	
	10	+ 3	13-5			F18	6	Gate D (bus 12) SLT collector voltage and digital I/O subchannel termination	I/O monitor
	12	+ 6	12-6		F20		10	Gate C (bus 8) SLT diode-gate voltage Gate D (bus 8) SLT diode-gate voltage (1801 boards A1, B1; 1802 all boards)	1442, I/O monitor, 1851 (if supply #1 is not installed)
	13	+ 6	12-8		F21		11	Gate D (bus 6) SLT diode-gate voltage (boards A2, B2, A3, B3)	
	15	- 3	13-7		F23		7	Gates A, B, C, D (bus 10) SLT bias voltage; Gates F and G integrators (1816-1053)	1442, I/O monitor
	16	-15	13-12	F7			12	Gate A (bottom bus 6 ④) and Gate B (bus 6) two-usec core storage	
	17	-9 to -12	13-11	F8			13	Gate A (bottom bus 2 ④) and Gate B (bus 2) two-usec core storage	
B	6 ①	+36	13-14			F14	-	Gate D (bus 2) contact-sense source voltage (via +36V overvoltage-protect circuit)	
	6 ②	-12	13-13			F15	-	Gate D (bus 2) tape adapter unit	
	8 ⑤	+30	7-4 via RY17, RY18, RY19			F17	17	Gate A (top bus 2) AI amplifiers and current source card	1851: differential amplifiers, RBT
	11	-30	7-8 via RY17, RY18, RY19		F19		18	Gate A (top bus 6) AI amplifiers, current source card, sync-ready driver; Gate C (bus 6) DI and DAO sync-ready drivers	1851: differential amplifiers
	14 ⑤	+12	12-12 via RY17, RY18, RY19	F22			-	Gate A (top bus 4) S&H or buffer amplifier, MPX relay X drivers	1851: relay block switches
	18	+48	8-2 via F24 and RY16	F9			-	Gate C (TB11) 1054-1055 magnet drivers; Gate D (TB18) 1816-1053 magnet drivers	1054, 1055, 1816, 1053

① 1801 only ② 1802 only ③ Four-usec core storage only ④ 32k core storage only ⑤ AI only ⑥ AI or 32k core storage only

14196A

Figure 5-3. DC Voltages - - 1801/1802 Processor Controller

Power Supply	DC Voltage	TB	Sense Relay	Distribution
1	+12	4-4	K-2	Gate B Bus 4
2	+ 6	4-3	K-2	Gate B Bus 8
3	- 3	4-2	K-2	Gate B Bus 10
4	+ 3	4-1	K-2	Gate B Bus 12
5	-15	4-5	①	Gate B Bus 6
6	-10	4-6	①	Gate B Bus 2

① Ready indicator on from -10V and -15V supplies after K-1 is picked by K-2.

12463

● Figure 5-4. DC Voltages - - 1803 Core Storage Unit

Power Supply	DC Volts	TB	Pri Ckt via CB2 (1801/2) & Mainline Switch	Sense Relay	1826 Distribution	Other
1	+ 6	4-4	F1	-	Gate A (bus 8 ②) SLT diode-gate voltage, MPX solid-state X drivers; Gate B (bus 8) SLT diode-gate voltage (boards A1, B1)	I/O monitor ① 1851: Solid-state block switches
2	- 3	4-3	F5	-	Gate A (bus 10 ②) and Gate B (bus 10) SLT bias voltage	I/O monitor ①
3	+ 3	4-1	F3	-	Gate B (bus 12 ③ , 4 ④) SLT collector voltage and digital I/O subchannel termination	I/O monitor ①
4	+ 6	4-5	F2	-	Gate B (bus 6) SLT diode-gate voltage (boards A2, B2, A3, B3)	
5 ⑤	+ 3	4-2	F4	-	Gate A (bus 12) SLT collector voltage and I/O channel termination (1800 and 360); Gate B (bus 4 ④)	
6	+36	4-6	F6	-	Gate B (bus 2) contact-sense source voltage (via +36v overvoltage-protect circuit)	
7 ⑥	+12	5-2 via RY3	RY4 F8	-	Gate A (bus 4) S&H or buffer amplifier, MPX relay X drivers	1851: relay block switches
8 ⑥	+30	4-14 via RY1, RY2, RY3	F9	1	Gate A (bus 2) AI amplifiers and current source card	1851: differential amplifiers, RBT
9 ⑥	-30	4-13 via RY1, RY2,RY3	F10	2	Gate A (bus 6) AI amplifiers, current source card, sync-ready driver	1851: differential amplifiers
9 ⑦	-12	4-14	F10	-	Gate A (bus 2)	-

① Model 1 1826 only ② AI Expander or System/360 Adapter only ③ Boards A1, B1, A3, B3
④ Boards A2, B2 (from supply 3 if supply 5 is not installed) ⑤ Used for AI Expander, System/360 Adapter, or when more than eight groups of DO are installed ⑥ AI Expander only ⑦ Communication Adapter only

14197 A

● Figure 5-5. DC Voltages - - 1826 Data Adapter Unit, Models 1 and 2

Power Supply	DC Voltage	TB	Pri ckt via CB2 (1826/2) & Mainline Sw	Sense Relay	1826-3 Distribution	Other
1	-12	4-4	F1	-	Gate A Bus 2 Gate B Bus 2	
2	+6	4-3	F2	-	Gate B Bus 8 Gate A Bus 8	I/O Monitor Plug A1
3	-3	4-2	F3	-	Gate A or B Bus 10	I/O Monitor Plug A12
4	+3	4-1	F4	-	Gate B Bus 12	I/O Monitor Plug A3
5	+3	4-6	F6	-	Gate A Bus 12	

12464

Figure 5-6. DC Voltages - - 1826-3 Data Adapter Unit

Power Supply*	1856 Distribution
+30v	DAC voltage switches, analog driver amplifier, PVR mod 1, PVR mod 2
-30v	DAC voltage switches, analog driver amplifier, PVR mod 2
+ 6v	SLT diode-gate voltage, 0.45a drivers
+ 3v	SLT collector voltage (1)
- 3v	SLT bias voltage

* Measure voltage from test jack to logic-common jack

(1) DAO subchannel termination on last 1856 only.

14199A

Figure 5-8. Power Pac DC Voltages – 1856 Analog Output Terminal

Power Supply	TB	Pri Ckt via Mainline Sw and Fuse		1810 Distribution	Other
		2310A F10	2310C F4		
+ 6v	2-5	F5	F5	Gate A (bus 8) and each Single Disk Storage (TB1-3), SLT diode-gate voltage	I/O monitor
- 3v	2-3	F6	F6	Gate A (bus 10) and each Single Disk Storage (TB1-2), SLT bias voltage	I/O monitor
+ 3v	2-1	F7	F7	Gate A (bus 12) SLT collector voltage and I/O channel termination; Each Single Disk Storage (TB1-1) SLT collector voltage	I/O monitor
+48v	2-7 via F9 and RY1	F4	F9 F10 F11	Each Single Disk Storage (TB1-5) operator switches and lamps, magnet voltage, access and detent controls, +35v regulator (for write drivers)	

14198A

Figure 5-7. DC Voltages - - 1810 Disk Storage

Chapter 6. Locations

6.1 LOCATIONS SHOWN IN SYSTEM DIAGRAMS

6.1.1 System

Card Feature Codes and Locations, BA001
I/O Channel Interface Cable Routing, CT990-997

6.1.2 1801 and 1802 Processor-Controllers

Analog Board Adjustment and Test Points, QD935
Channel Interface to I/O Monitor, CU901-931
Core Storage Board, Four-Microsecond:
- Bottom Board Terminals, 4k, SD072
- Bottom Board Terminals, 8k, SD071
- Core Storage Board Connectors, SD012
- Diodes on Diode Board, 4k, SD082
- Diodes on Diode Board, 8k, SD081
- Sense Connections, 4k, SD062
- Sense Connections, 8k, SD061

Core Storage Board, Two-Microsecond:
- Bottom Board Terminals, 4k, SA072
- Bottom Board Terminals, 8k, SA071
- Core Storage Board Connectors, SA012
- Diodes on Diode Board, 4k, SA082
- Diodes on Diode Board, 8k, SA081
- Sense Connections, 4k, SA062
- Sense Connections, 8k, SA061

DI Adapter Location Assignment, RA000
DO Adapter Location Assignment, TL000
Gate Power Distribution, YA159
PC Adapter Location Assignment, RB000
PI Assignment Chart, RC000
Power and Signal Connectors, BP001
Programmer's Console Assembly, BL001
S&H Amplifier Adjustment Points, QD931
Special Voltage Distribution, YA231-232
1054 Adapter Interface to Reader, ES821-831
1055 Adapter Interface to Punch, ES871-881
1442 Adapter Interface to CRP, EN831-891
1443 Adapter Interface to Printer, EL121, 221, 401, 421, 431, 441
1627 Adapter Interface to Plotter, EK271
1816-1053 External Connections, EG101

6.1.3 1826 Data Adapter Unit

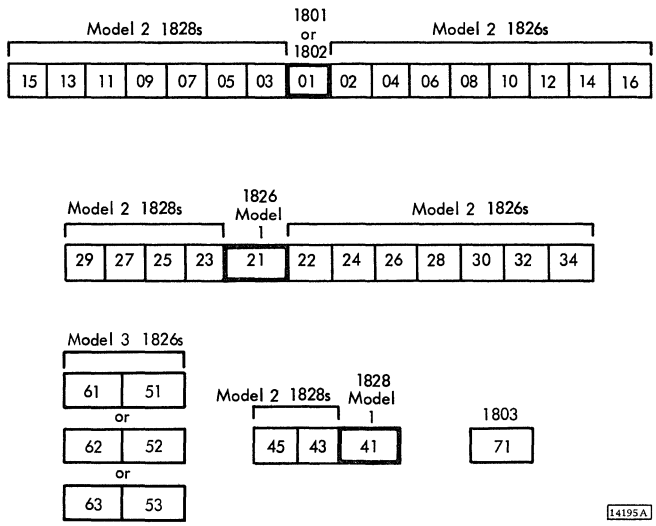
Analog Board Adjustment and Test Points, QD935
CA Data Set Interface MK031
CA Personality Wiring MA008, MK008
DI Adapter Location Assignment, RA000
DO Adapter Location Assignment, TL000
PC Adapter Location Assignment, RB000
PI Assignment Chart, RC000
S&H Amplifier Adjustment Points, QD931
Selector Channel Interface FS021-061
Signal and Power Tailgates, YB650
System/360 Adapter Interface, FV201-271, FV401-411

6.1.4 1828 Enclosure

Signal and Power Tailgates, YD210
1851 Card Receptacle Wiring, QC110-120
1851 Differential Amplifier Adjustment and Test Points, QC935
1851 Mixer Panel, QC100
1851 Multiplexer Addresses, QC060
1851 Multiplexer Configuration, QC040
1851 Multiplexer Drive Line Tracing Chart, QC130
1851 Terminal Location and Range, QC070
1856 AO Assignment Chart, TA000
1856 AO Configuration, TA003-004
1856 AO to Customer Terminal, TA007
1856 Tailgate Area, TA950

6.2 FRAME NUMBERING SYSTEM

System enclosures are identified in the MLR and FESRR by the following frame numbers.



6.3 BOARD LOCATIONS

In the following tables, board locations for expandable features are listed in order of installation priority within each frame. For locations (such as 01D-B3) that are shared

by digital I/O features, installation priority is (1) digital output, (2) process interrupt, (3) digital input, (4) pulse counter.

1801, 1802, 1826-1

ALD Block Symbol	Board Description	Locations 1801	1802	1826
02D-A2	TCU Controls		D-A2	
02D-A3	TCU Clocks, Regs		D-A3	
02D-B2	TCU Channel		D-B2	
02D-B3	TCU Final Amps		D-B3	
26A-A3	360 Adapter, Data			A-A3
26A-B3	360 Adapter, Control			A-B3
60A-A1	ADC	A-A1	A-A1	A-A1
60A-A2	Al Comp, Matrix Dr	A-A2	A-A2	A-A2
60A-B1	Channel, Al Basic	A-B1	A-B1	A-B1
60A-B2	Analog In Basic	A-B2	A-B2	A-B2
60B-A1	Channel	B-A1	B-A1	
60B-A2	CPU Registers	B-A2	B-A2	
60B-B1	Channel	B-B1	B-B1	
60B-B2	CPU Control	B-B2	B-B2	
*60C-A1	1816/1053 Adapter #1	C-A1	C-A1	
	1816/1053 Adapter #2	D-B1	D-B1	
60C-A2	Digital In Basic	C-A2	C-A2	
60C-A3	DI-DAO Basic	C-A3	C-A3	
60C-B1	1443/1627 Adapter	C-B1	C-B1	
*60C-B2	1442 Adapter #1	C-B2	C-B2	
	1442 Adapter #2	D-A1	D-A1	
60C-B3	Dig & Anal Out Basic	C-B3	C-B3	
60D-A1	1054/1055 Adapter	D-A1	D-A1	
60E-A1	Core Storage Mixer	E-A1	E-A1	
60H-A1	Cycle-Steal Mixer	H-A1	H-A1	
60X-X5	1816/1053 Integrators #1	F-A1	F-A1	
	1816/1053 Integrators #2	G-A1	G-A1	
60X-Y1	Digital Out Adapter	D-A3		B-A3
		D-B3		B-B3
				B-B2
				B-A2
60Y-V1	Proc Intrpt Adapter	D-A2		B-B2
		D-B3		B-A2
60Y-W1	Pulse Ctr Adapter	D-A2		B-A1
		D-B3		B-B2
				B-A2
60Y-X1	Digital In Adapter	D-B2		B-B1
		D-B3		B-A1
				B-A2
63Z-Z1	Core Storage 4k/8k	B-A3	B-A3	
	2nd 8k	B-B3	B-B3	
	3rd 8k	A-B3	A-B3	
	4th 8k	A-A3	A-A3	

* Although board can be used in two locations, only the location of the first adapter board is shown in ALD block.

14174C

ALD Block Symbol	Description	Locations (factory build) 1826-2	1826-3
26A-B3	S/360 Adapter, Control	A-B3	
26A-A3	S/360 Adapter, Data	A-A3	
26Z-Z1	Selector Channel (Bd 1)	A-A1	A-A1
Z2	Selector Channel (Bd 2)	A-A2	A-A2
Z3	Selector Channel (Bd 3)	A-A3	A-A3
26Z-X3	Line Adapter 0 of 1st Comm Adapter	A-B3	A-B3
X1	Line Adapter 1 of 1st Comm Adapter	A-B1	A-B1
X2	1st Comm. Adapter	A-B2	A-B2
	Line Adapter 0 of 2nd Comm Adapter	A-A3	A-A3
	Line Adapter 1 of 2nd Comm Adapter	A-A1	A-A1
	2nd Comm. Adapter	A-A2	A-A2
	Line Adapter 0 of 3rd Comm Adapter		B-A3
	Line Adapter 1 of 3rd Comm Adapter		B-A1
	3rd Comm. Adapter		B-A2
	Line Adapter 0 of 4th Comm Adapter		B-B3
	Line Adapter 1 of 4th Comm Adapter		B-B1
	4th Comm Adapter		B-B2
26Y-B1	1st 2790 Adapter (Bd 1)	A-B1	B-A1
A1	1st 2790 Adapter (Bd 2)	A-A1	B-B1
B2	1st 2790 Adapter (Bd 3)	A-B2	B-A2
A2	1st 2790 Adapter (Bd 4)	A-A2	B-B2
	2nd 2790 Adapter (Bd 1)		A-B1
	2nd 2790 Adapter (Bd 2)		A-A1
	2nd 2790 Adapter (Bd 3)		A-B2
	2nd 2790 Adapter (Bd 4)		A-A2
60X-Y1	1st Digital Output Adapter	B-A3	
	2nd Digital Output Adapter	B-B3	
	3rd Digital Output Adapter	B-B2	
	4th Digital Output Adapter	B-A2	
60Y-V1	1st Process Interrupt Adapter	B-B2	
	1st or 2nd Process Interrupt Adapter	B-A2	
60Y-X1	1st Digital Input Adapter	B-B1	
	2nd Digital Input Adapter	B-A1	
	3rd Digital Input Adapter	B-A2	
60Y-W1	1st Pulse Counter Adapter	B-A1	
	1st or 2nd Pulse Counter Adapter	B-B2	
	1st, 2nd, or 3rd Pulse Counter Adapter	B-A2	

12451

1851, 1856

ALD Block Symbol	Board Description	Locations 1851	1856
51A ---	Multiplexer	A ---	
51A -X3	Mixer Board	A ---	
56M-X1	Mixer Board #1		M-G8
	#2		M-H8
56M-X2	Mixer Board		M-E8
56M-X3	Mixer Board		M-F8
56Y -A7	DAC Conn Socket		Y-A7
56Y -B7	DAC Conn Socket		Y-B7
56Y -B8	Terminal Boards		Y-B8
56Y -C1	Prec Volt Ref - 2		Y-C1
56Y -C7	PVR Conn Socket		Y-C7
56Y -D1	Power Pac		Y-D1
56Y -D7	Pwr Pac Conn Socket		Y-D7
56Y -D8	Terminal Boards		Y-D8
56Y -E7	DAC Conn Socket		Y-E7
56Y -F7	DAC Conn Socket		Y-F7
56Y -G1	Anlg Chan Control		Y-G1
56Y -Y7	DAC #1		Y-A1
	#2		Y-B1
	#3		Y-E1
	#4		Y-F1
56Y -Y8	Prec Volt Ref - 1		Y-C1

14175B

6.4 WIRED LOGIC (WL) JUMPERING

6.4.1 Interrupt, Cycle Steal, IPL

Analog Input and Comparator, QD041, QD042, QD991
Cycle Steal (Channel Board), BC101, CU991, CU995
Cycle Steal (Mixer Board), BC101, CT997
| Communications Adapter, MA008, MB997
Digital and Analog Output, PB000, PA991
Digital Input, PD000, PA991
Interrupt (Additional Levels), BC150, CU995
Interval Timers and Console, BC150, CU991, CU995
| Selector Channel, FS011, FS013
System/360 Adapter, FV001, FZ991
Tape Control Unit, GA111, GB991
1053-1816 Printer and Printer-KB, EA001, EA991
1054-1055 Paper Tape Reader-Punch, ES001, ES992
1442 Card Read Punch, EN001, EN991
1443 Printer, EJ005, EJ991
1627 Plotter, EJ001, EJ991
1810A Disk Storage, FA001, FA991, FA992
| 1810B Disk Storage, FC001, FC991

6.4.2 Other

AO Addressing, TA001, TA051
AO Optional Features, TA001, TA661, TA631, TA991
Core Storage Module Selection, 2-μs, SA111
Core Storage Module Selection, 4-μs, SD331
| Communications Adapter, MA008, MB997, MB998, MB999
DI Group Addressing, RA002, RA021
DI High-Speed Voltage Input, RA111-821
DO Control, TL001, TL051
DO Group Addressing, TL001, TL110, TL120, TL130, TL140
Interval Timer (Time Selection), CU991
| Line Adapter, MK008, MM998, MM999
PC Coupler, RB991
PC Group Addressing, RB005, RB021
PI High-Speed Input, RC111-821
PI ILSW Bit Jumpering, RC004, RC981
PI Level Decode Jumpering, RC002, RC981
PI Request Jumpering, RC001, RC991
System/360 Adapter Address Decode, FV005, FY101
System/360 Adapter Select-Bypass, FV005, FV251
| 2790 Adapter LA005, LC991

6.5 COMPONENT LOCATIONS INDEX

6.5.1 1801 and 1802 Processor-Controllers

Console switches and lamps are shown on BL001, BL005, and BL009. ALD page locations of other components are shown on YA700-710.

Fuses (YA700)

F1 thru F36	Figure 6-3, 6-4
F37	Figure 6-1
F38, F39	Figure 6-2

Relays (YA700)

RY1 thru RY16	Figure 6-5
RY17 thru RY19	Figure 6-6
RY20 thru RY23	Figure 6-5

Contactors (YA710)

K1 thru K4	Figure 6-3, 6-4
K5	Figure 6-4

Circuit Breakers (YA700)

CB1 thru CB4	Figure 6-3, 6-4

Edge Connectors (YA710)

EC1 thru EC12	Figure 6-5
EC15 thru EC20	Figure 6-1

Terminal Boards (YA710)

TB1 thru TB6	Figure 6-3, 6-4
TB6B	Figure 6-4
TB7	Figure 6-6
TB8	Figure 6-5
TB9	Figure 6-3, 6-4
TB10	Figure 6-1
TB11	Figure 6-2
TB12, TB13	Figure 6-6
TB14, TB15, TB16	BL001
TB17	Figure 6-1
TB18 thru TB20	Figure 6-2
TB21	Figure 6-3
TB22	Figure 6-2
TB23	Figure 6-1

6.5.2 1803 Core Storage Unit

Lamps

CB	Figure 6-13	YS210
Power on Neon	Figure 6-14	YS210
Ready	Figure 6-13	YS240

Fuses

F1 through F7	Figure 6-14	YS210

Contactors

K1	Figure 6-14	YS210
K2	Figure 6-14	YS240

Edge Connectors

EC1 and 2	Figure 6-15	
Mainline CB	Figure 6-14	YS210
Terminal Board		
TB1 and 2	Figure 6-14	YS210
TB4	Figure 6-15	YS240

6.5.3 1826 Data Adapter Unit, Models 1 and 2

Fuses

F1 thru F10	Figure 6-18

Relays

RY1 thru RY3	Figure 6-19
RY4, RY5	Figure 6-18

Edge Connectors

EC1	Figure 6-18

Terminal Boards

TB1 thru TB3	Figure 6-18
TB4, TB5	Figure 6-19
TB6	Figure 6-18

6.5.4 1826-3 Data Adapter Unit

Lamps

CB	Figure 6-23	YB220
Power On Neon	Figure 6-24	YB210

Fuses (YB110)

F1 through F7	Figure 6-24

Relays (None)

Contactors (None)

Circuit Breakers (None)

Main Line Switch	Figure 6-23	YB210
Edge Connector		
EC1	Figure 6-25	
Terminal Boards		
TB1	Figure 6-24	YB210
TB2	Figure 6-24	YB210, YB220 and YB250
TB4	Figure 6-25	YB240

6.5.5 1828 Enclosure

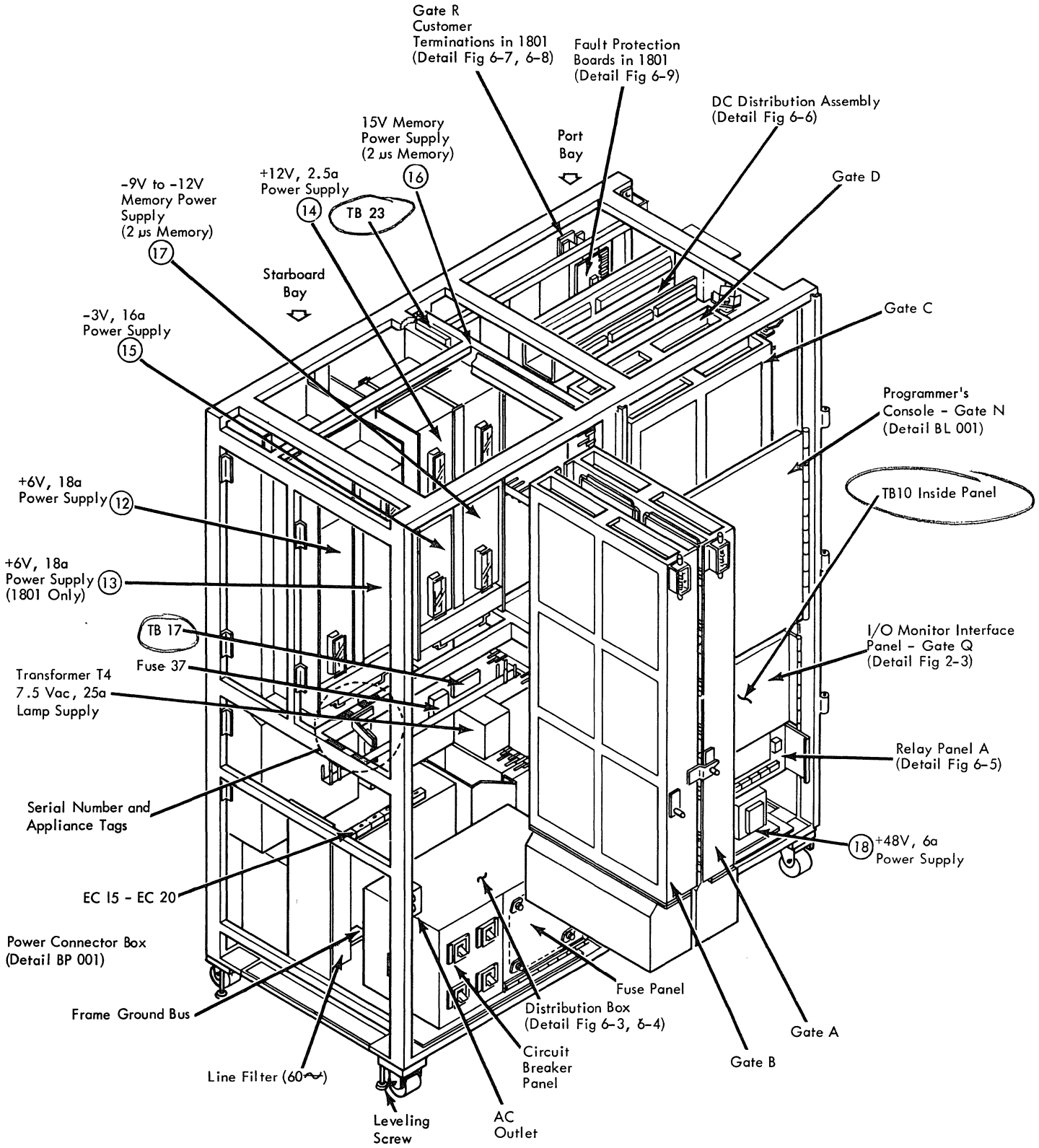
Fuses

F1, F2	Figure 2-28

Terminal Boards

TB1, TB2	YD210
TB4	Figure 2-28

6.6 LOCATIONS FIGURE LISTING

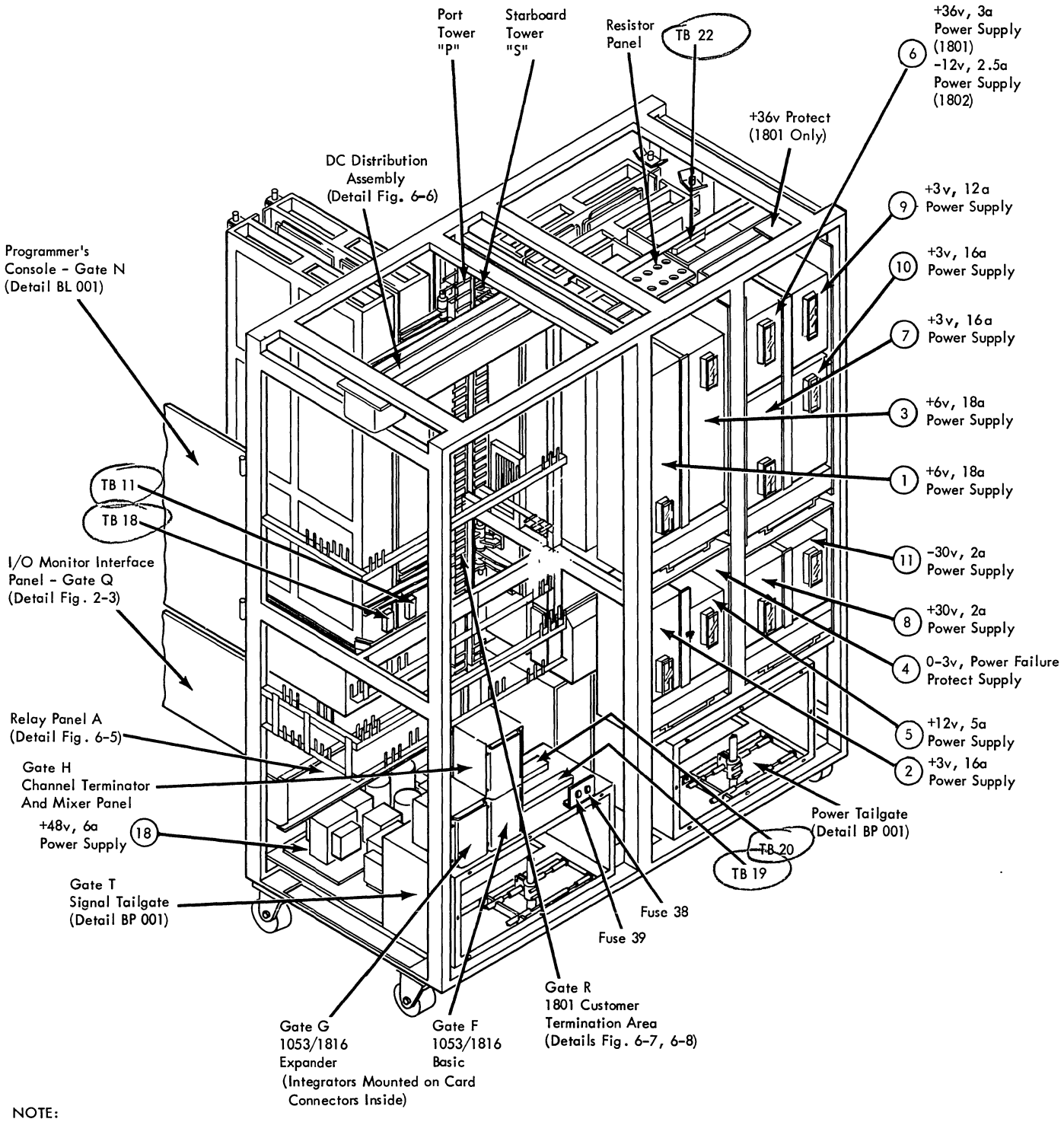


Note:

Circled numbers are used to identify the corresponding power supply in the System Diagrams. See Figure 5-3 for power distribution to gates.

2194902 | 14037D

Figure 6-1. 1801/1802 Processor Controller (Front)



NOTE:

Circled numbers are used to identify the corresponding power supply in the System Diagrams. See Figure 5-3 for power distribution to gates.

2194902 14038D

Figure 6-2. 1801/1802 Processor-Controller (Rear)

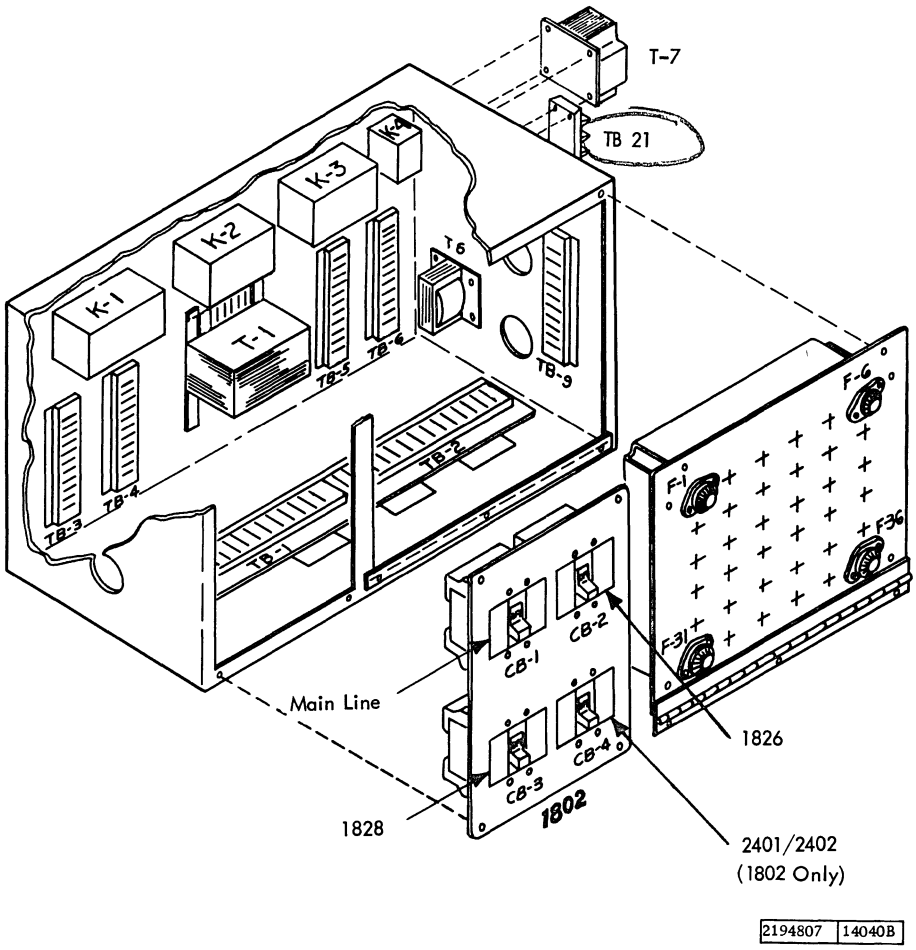


Figure 6-3. 1801/1802 AC Power Distribution Assembly (60 Hz)

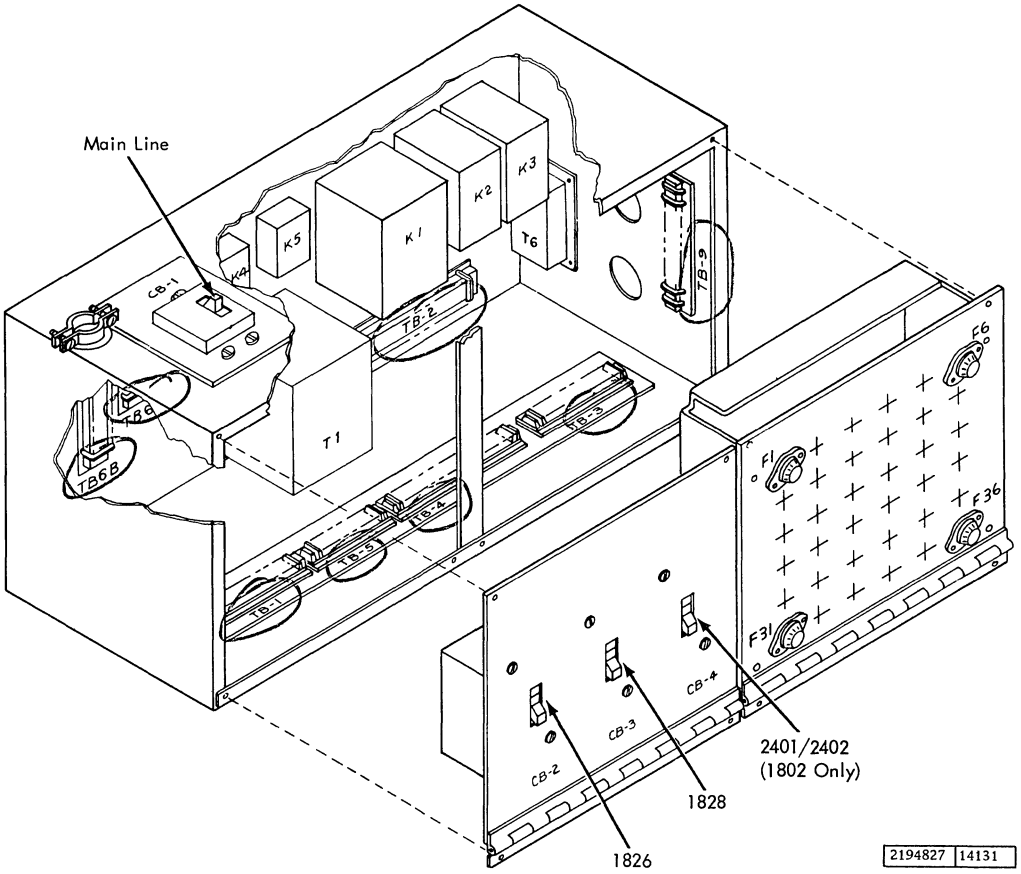


Figure 6-4. 1801/1802 AC Power Distribution Assembly (50 Hz)

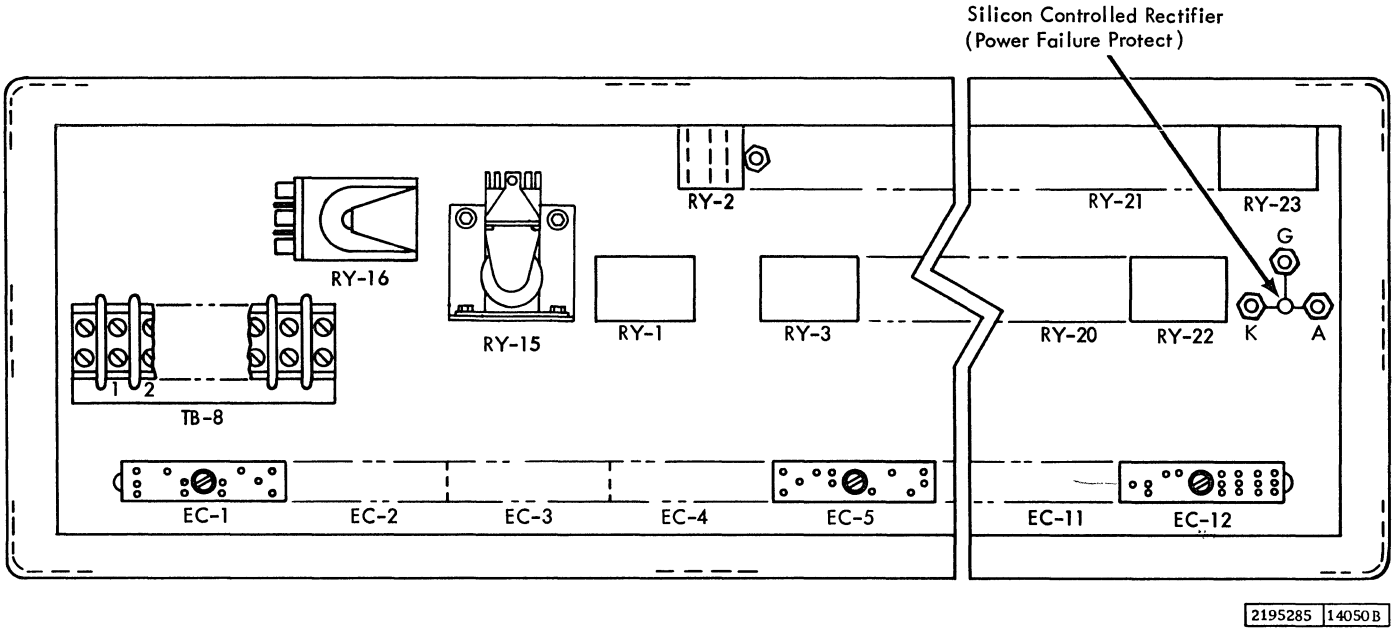


Figure 6-5. 1801/1802 Power Sequence Relay Panel A

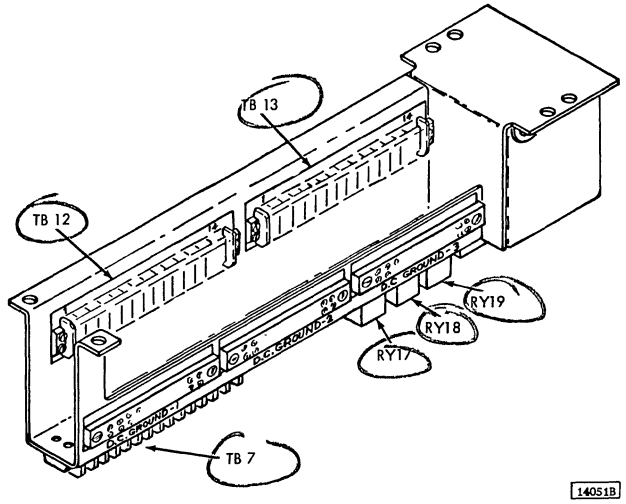


Figure 6-6. 1801/1802 DC Distribution Assembly

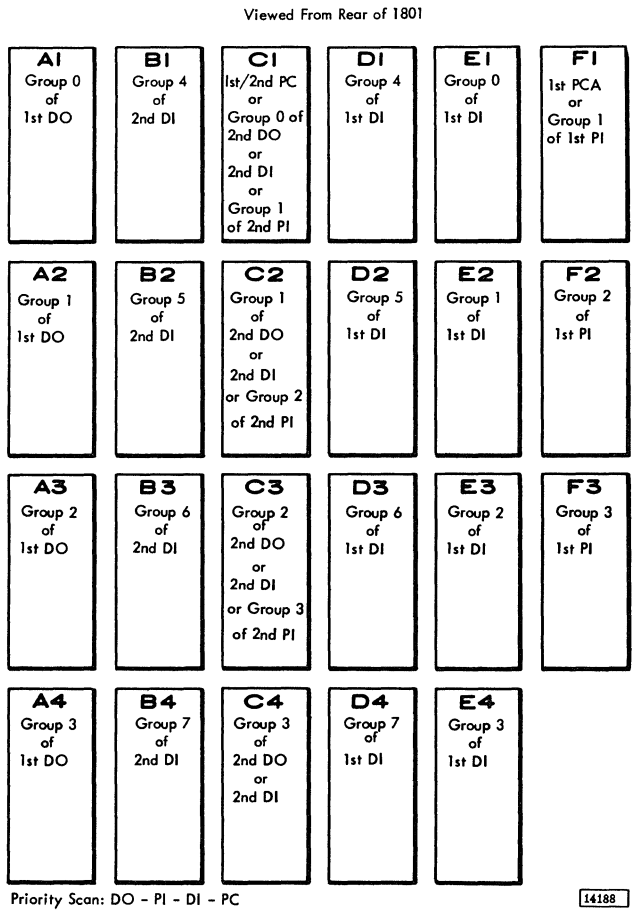


Figure 6-7. 1801 Customer Termination Area

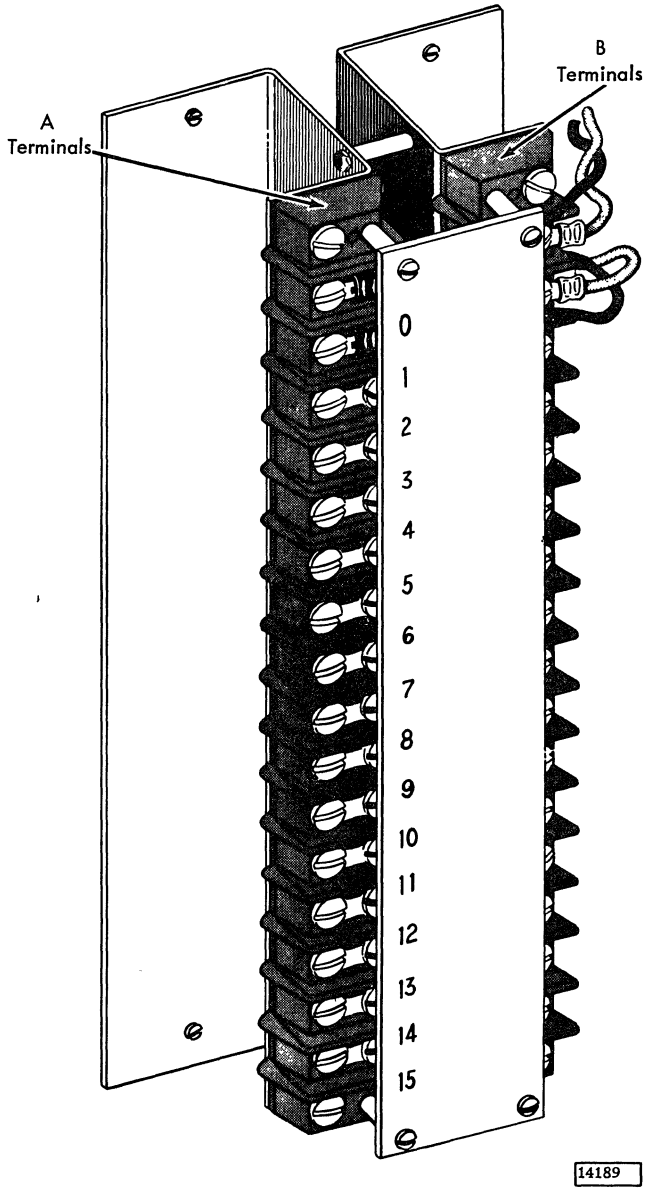
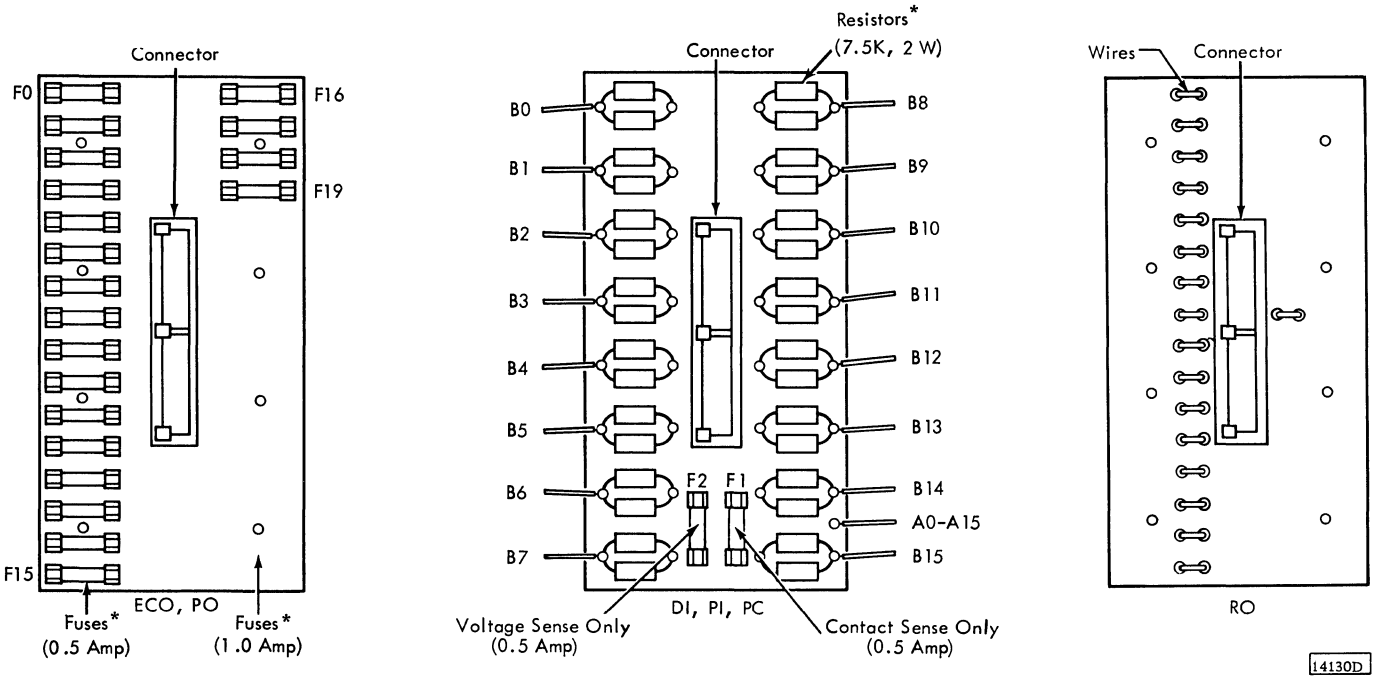
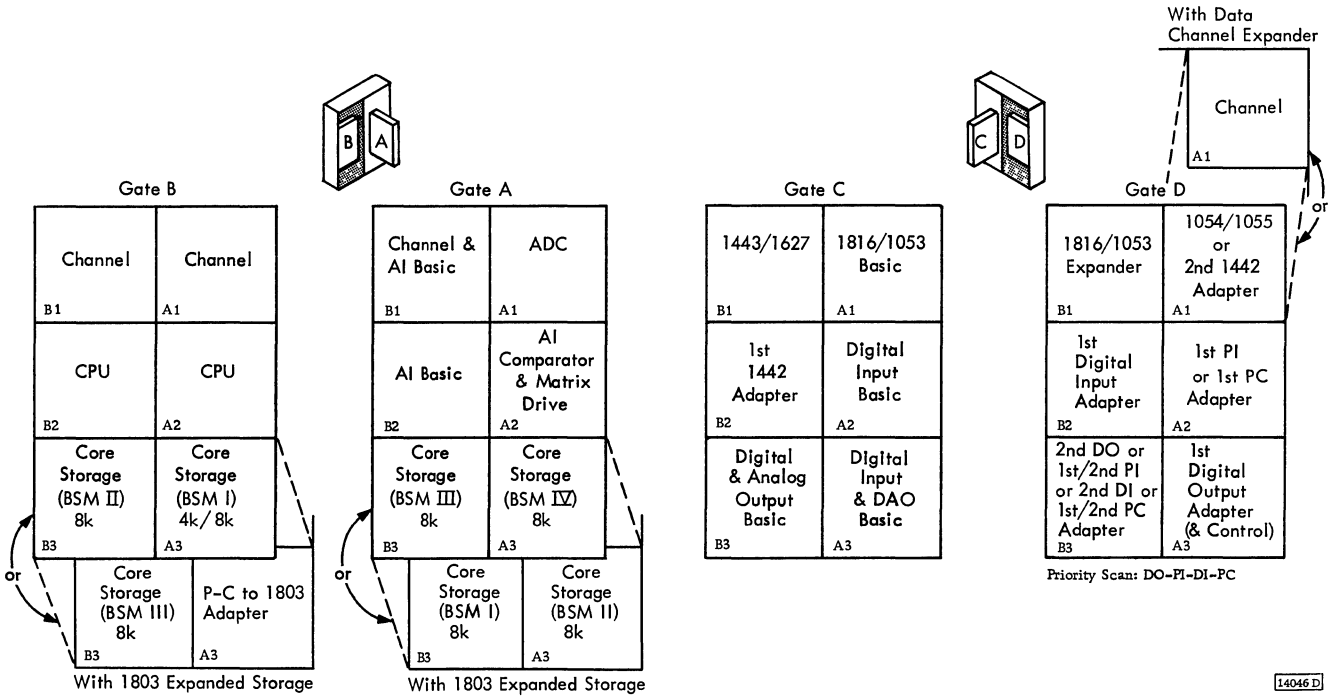


Figure 6-8. Customer Terminal Block (Digital I/O)

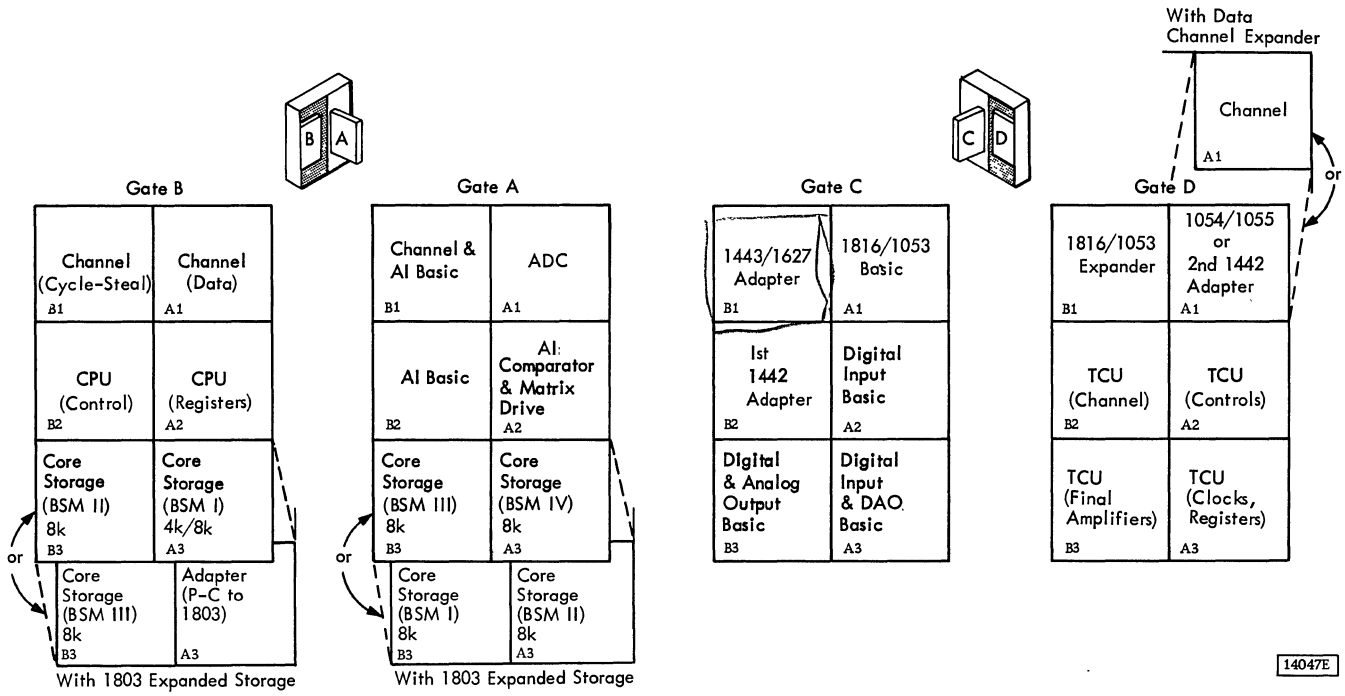


*On later EC level boards, the resistors and fuses are connected differently. Their locations remain the same.

Figure 6-9. Fault Protection Boards (Digital I/O)



● Figure 6-10. 1801 SLT Board Locations



● Figure 6-11. 1802 SLT Board Locations

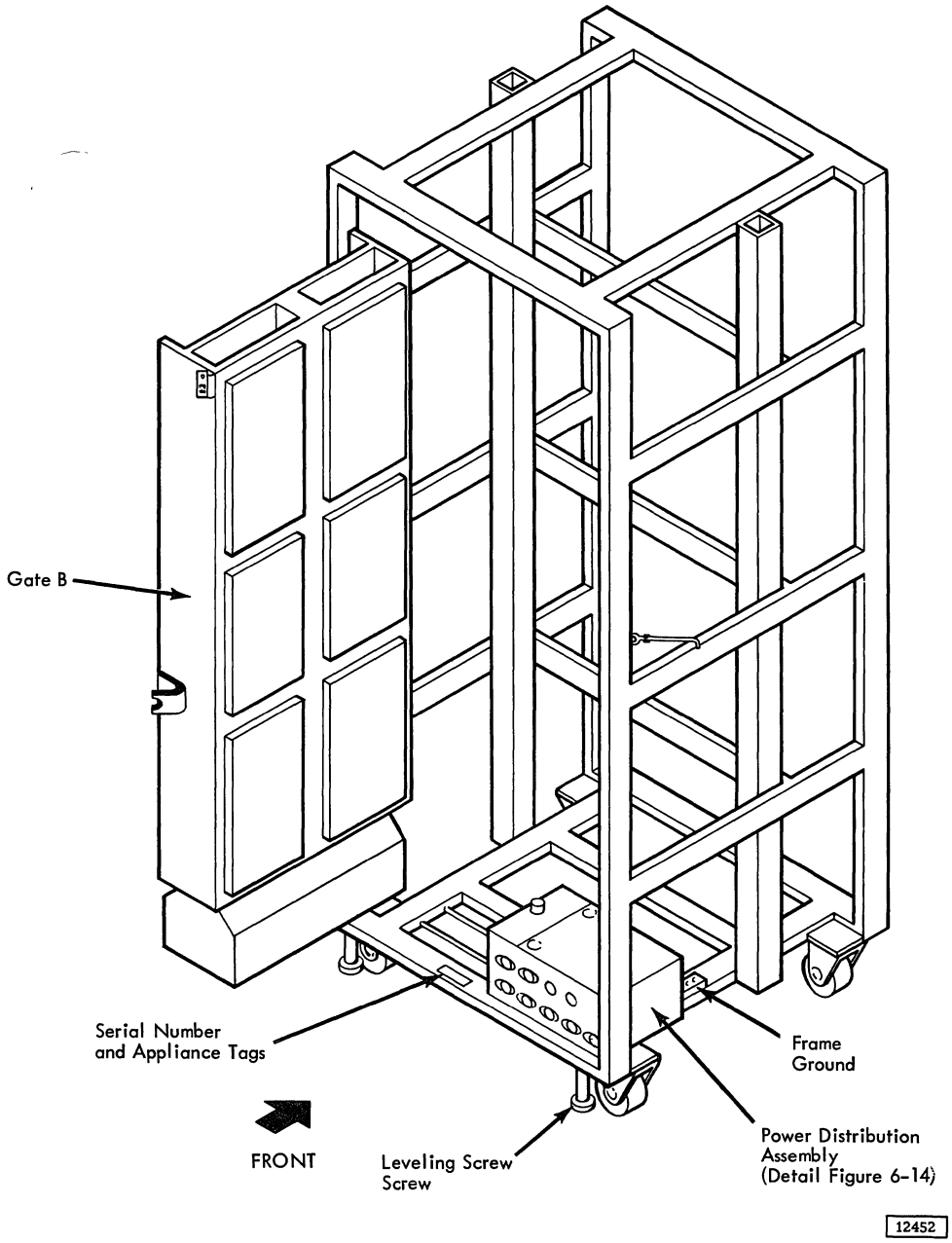


Figure 6-12. 1803 Core Storage Unit (Front)

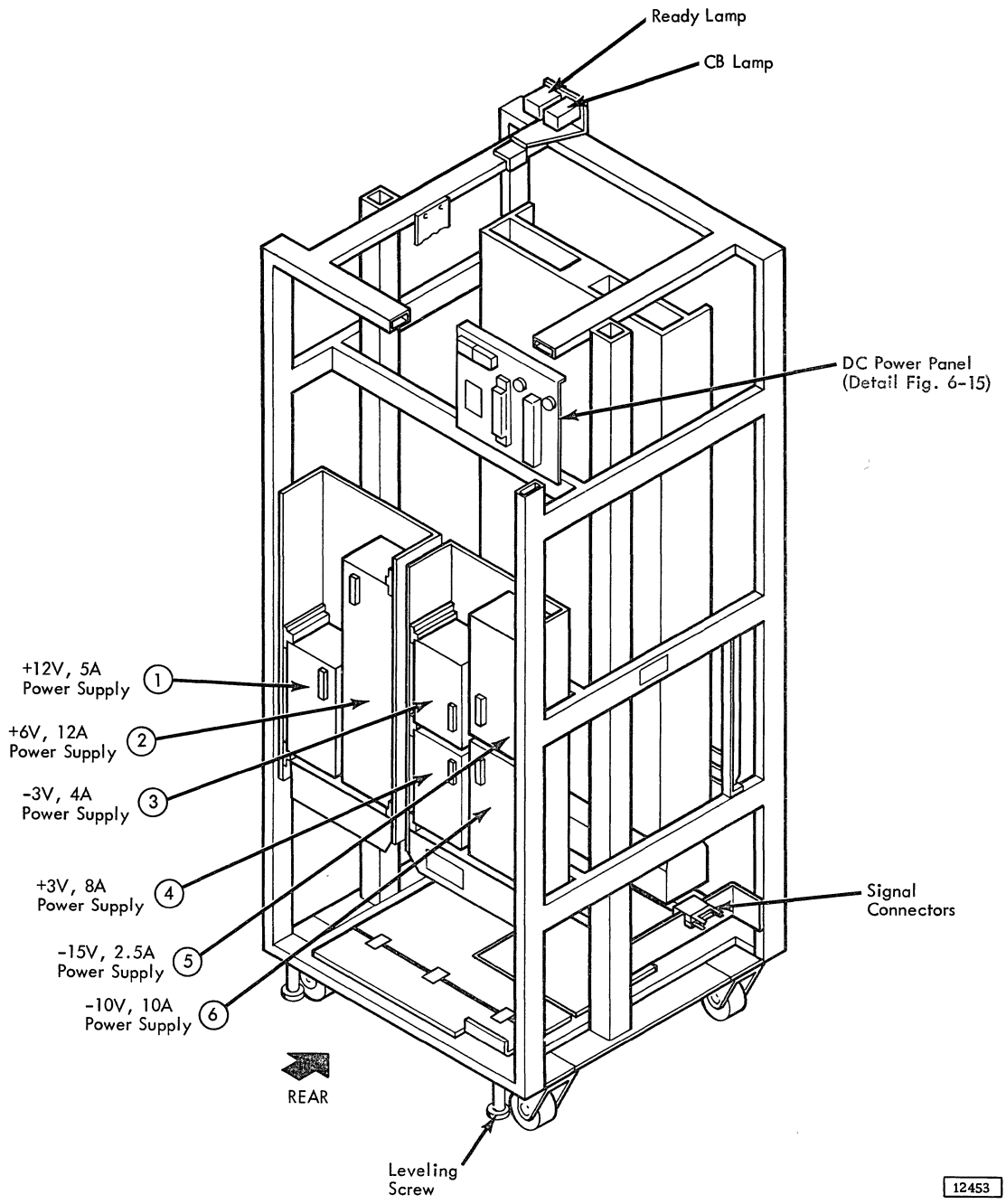


Figure 6-13. 1803 Core Storage Unit (Rear)

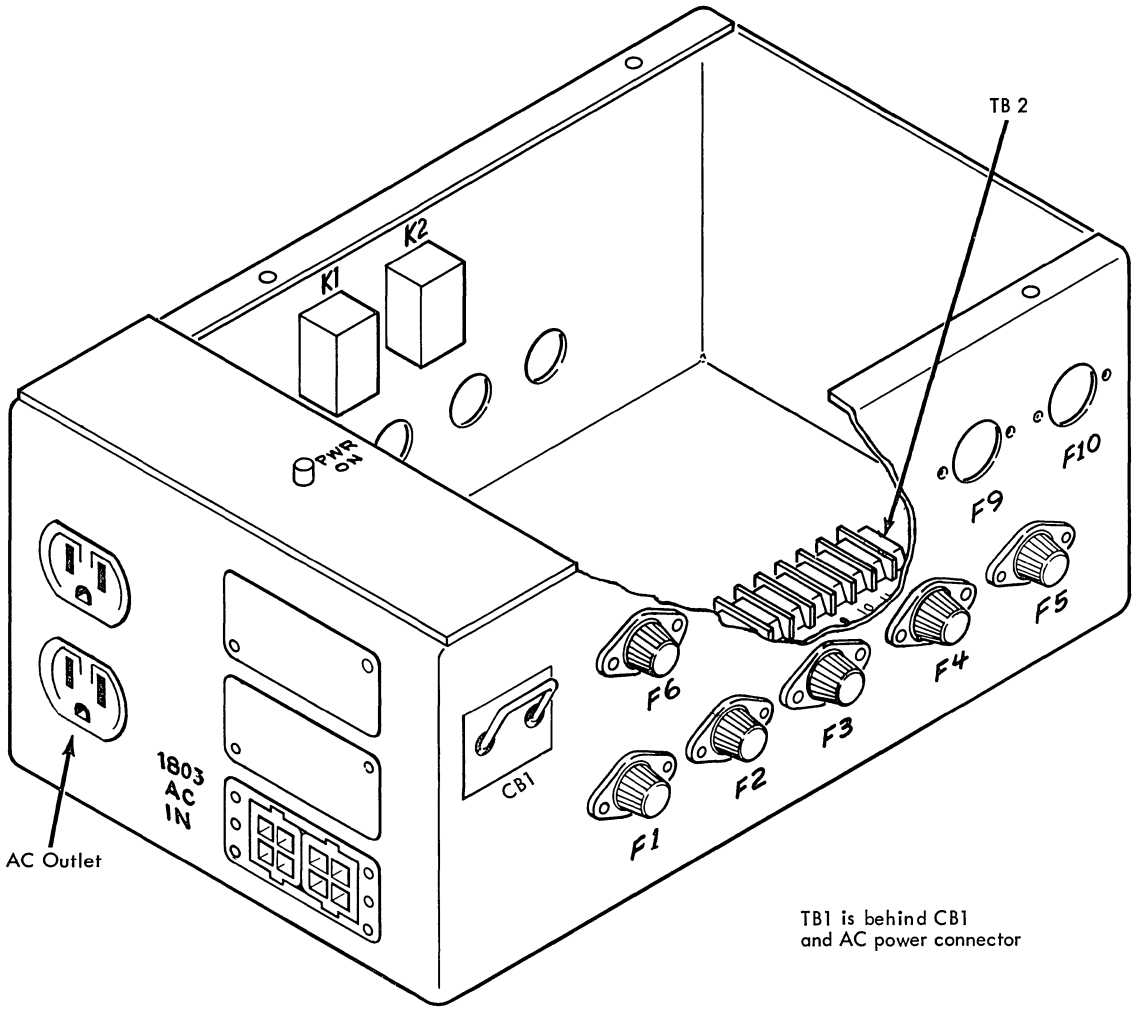
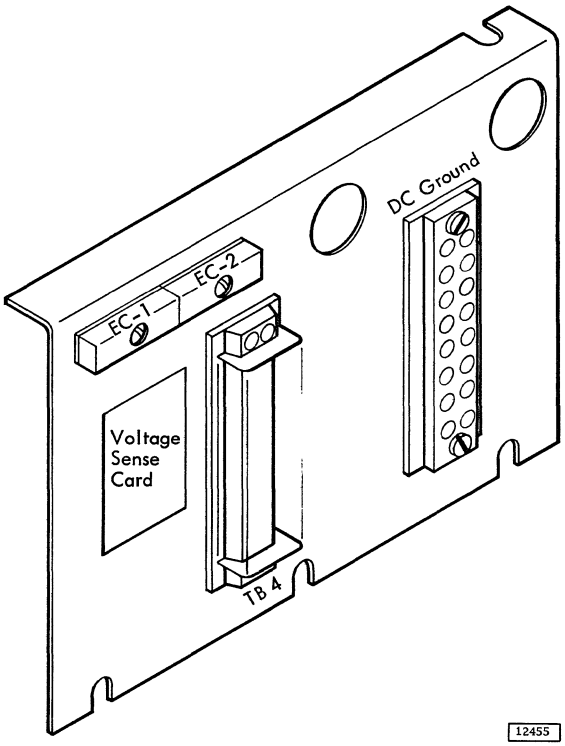


Figure 6-14. 1803 AC Power Distribution Assembly



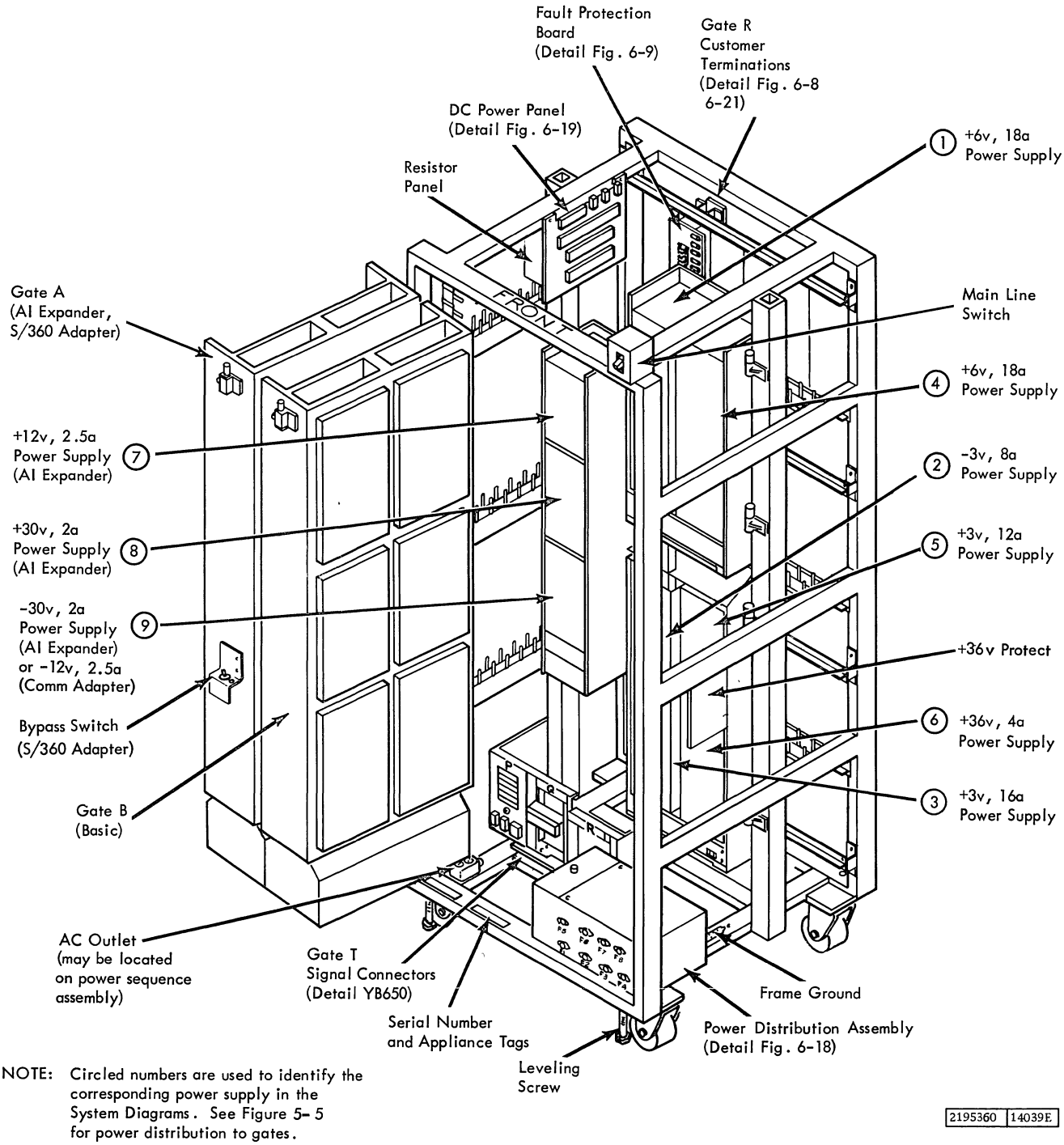
● Figure 6-15. 1803 DC Power Panel

Gate B

Core Storage (BSM VII) B1	Core Storage (BSM VIII) A1
Core Storage (BSM V) B2	Core Storage (BSM VI) A2
1803 to P-C Adapter B3	Core Storage (BSM IV) A3

12456

● Figure 6-16. 1803 SLT Board Locations



NOTE: Circled numbers are used to identify the corresponding power supply in the System Diagrams. See Figure 5-5 for power distribution to gates.

Figure 6-17. 1826 Data Adapter Unit, Models 1 and 2

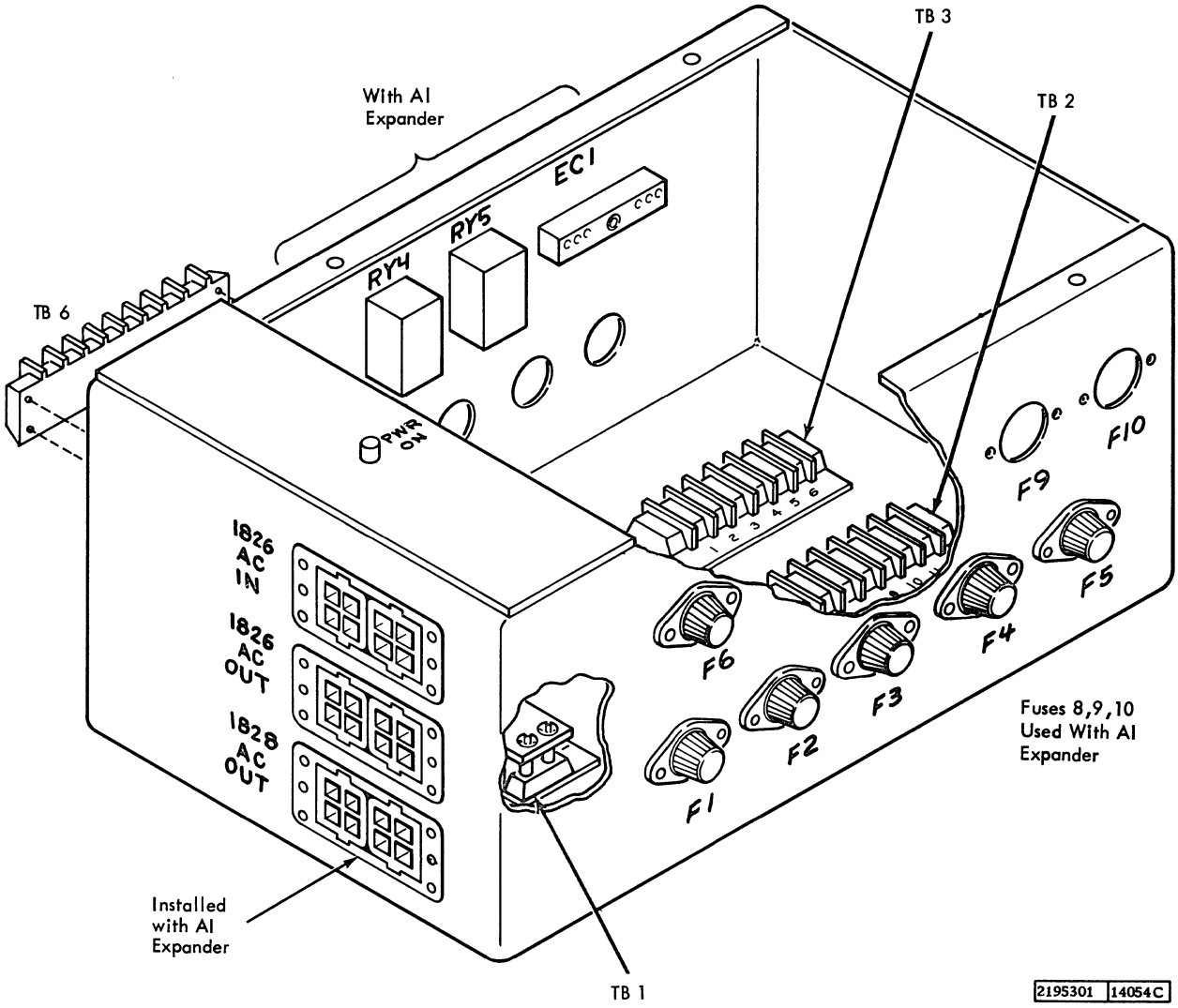


Figure 6-18. 1826–1, –2 AC Power Distribution Assembly

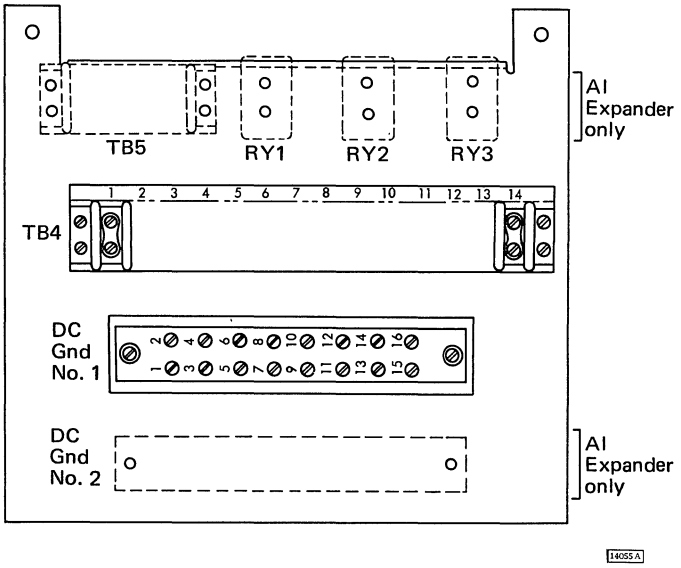


Figure 6-19. 1826–1, –2 DC Power Panel

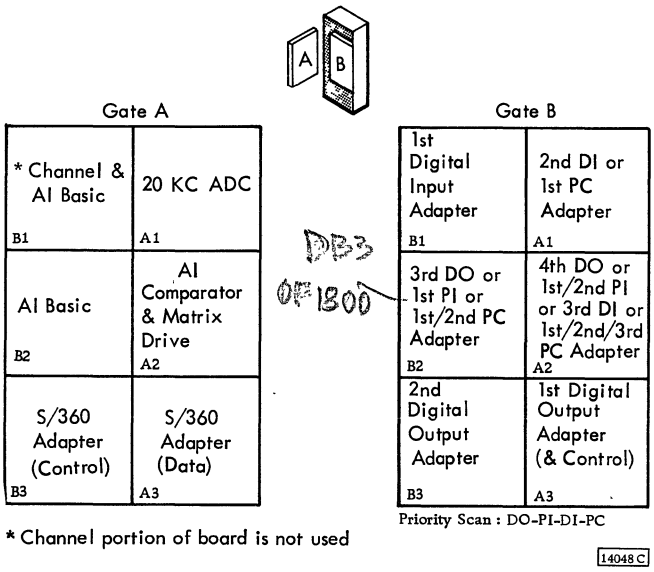


Figure 6-20. 1826–1 SLT Board Locations

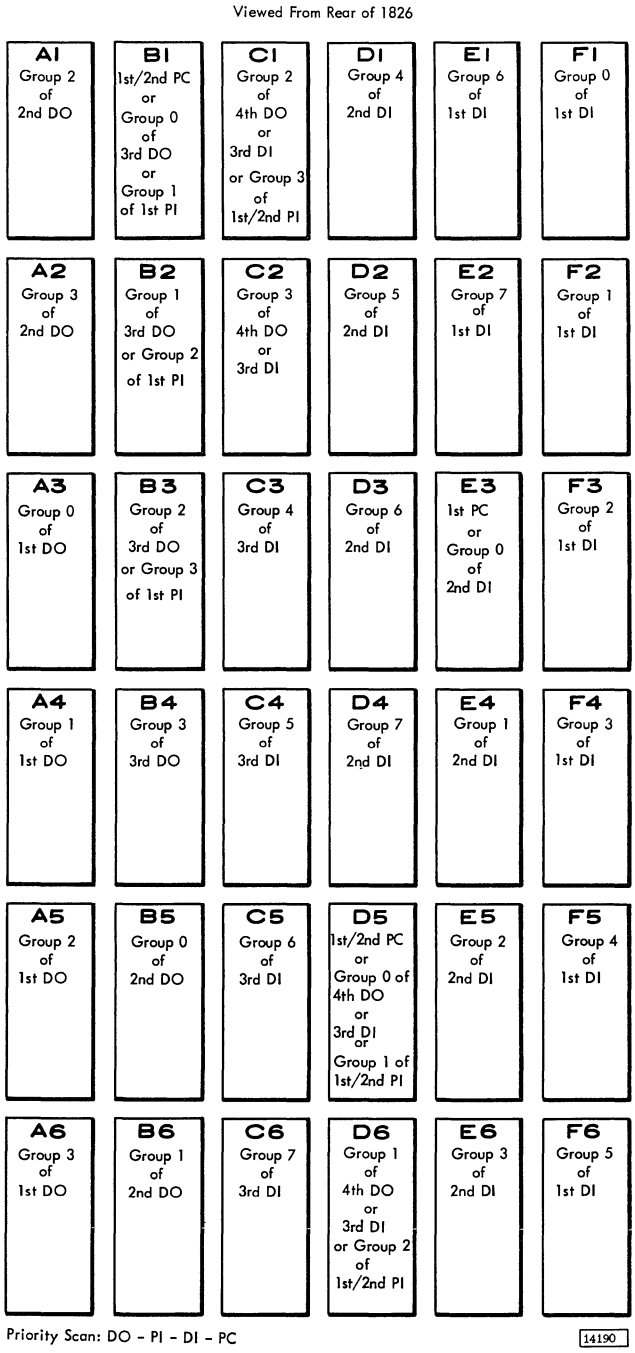
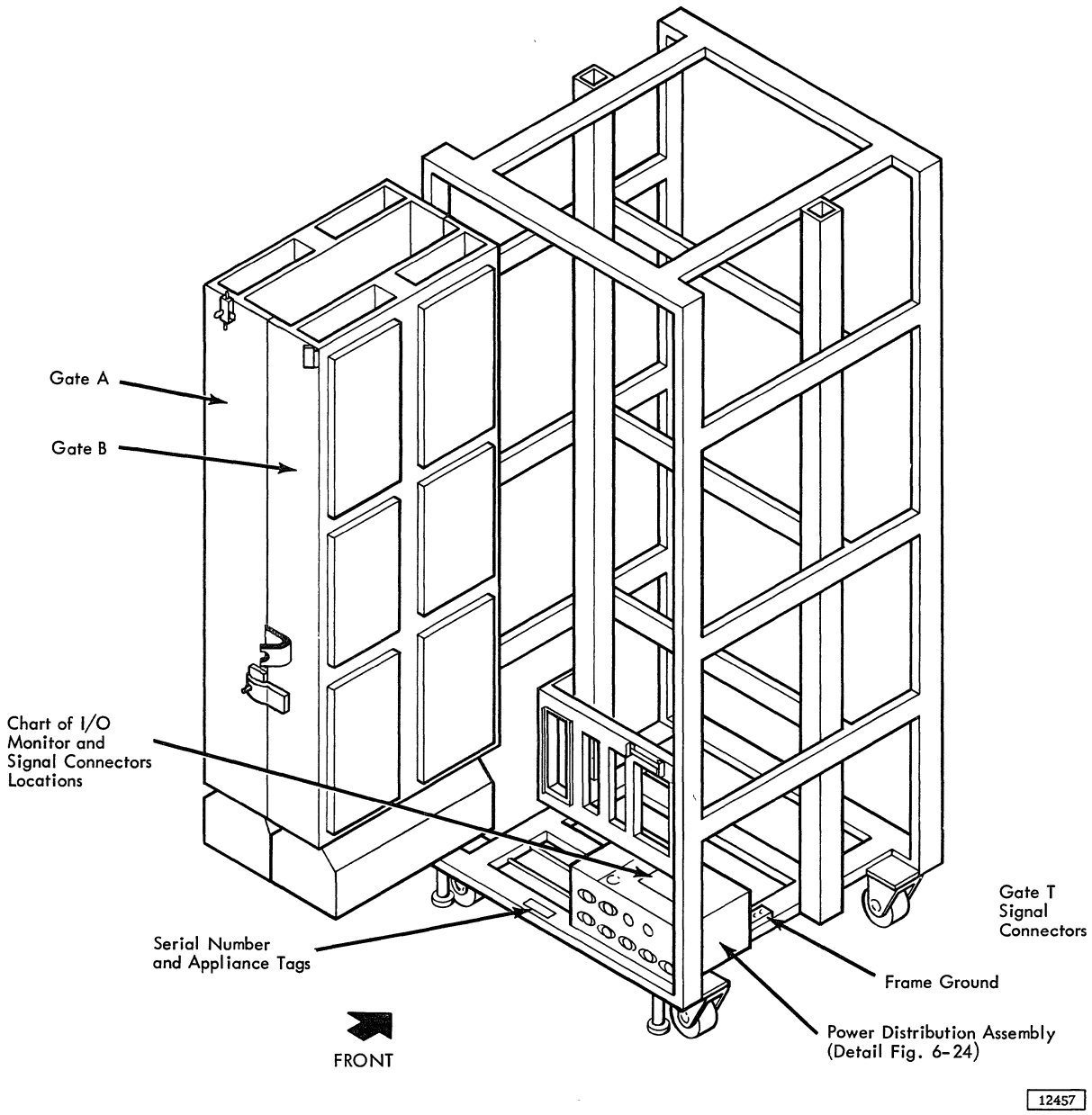
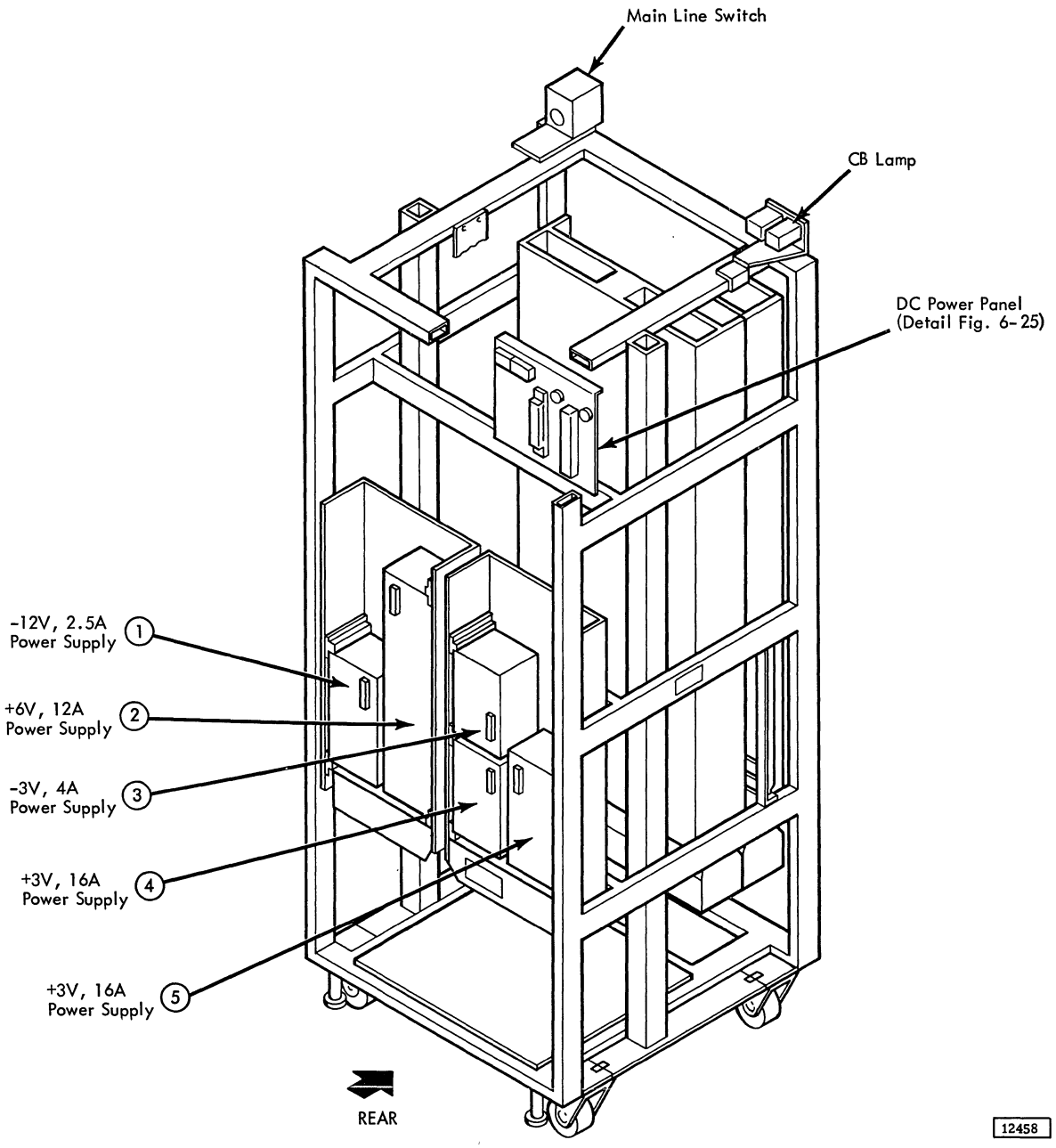


Figure 6-21. 1826 Customer Termination Area



● Figure 6-22. 1826 Data Adapter Unit, Model 3 (Front)



● Figure 6-23. 1826 Data Adapter Unit, Model 3 (Rear)

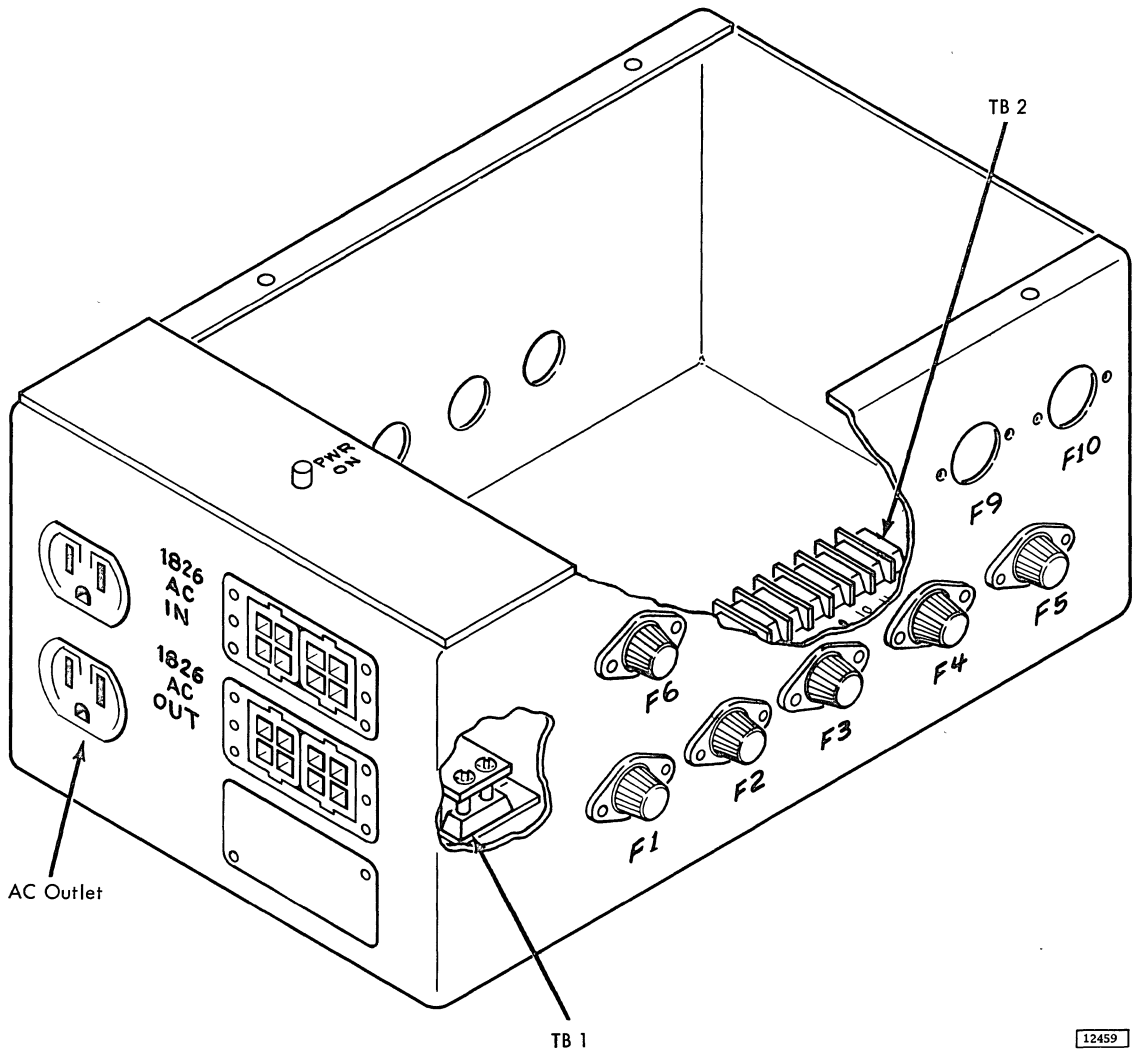


Figure 6-24. 1826–3 Power Distribution Assembly

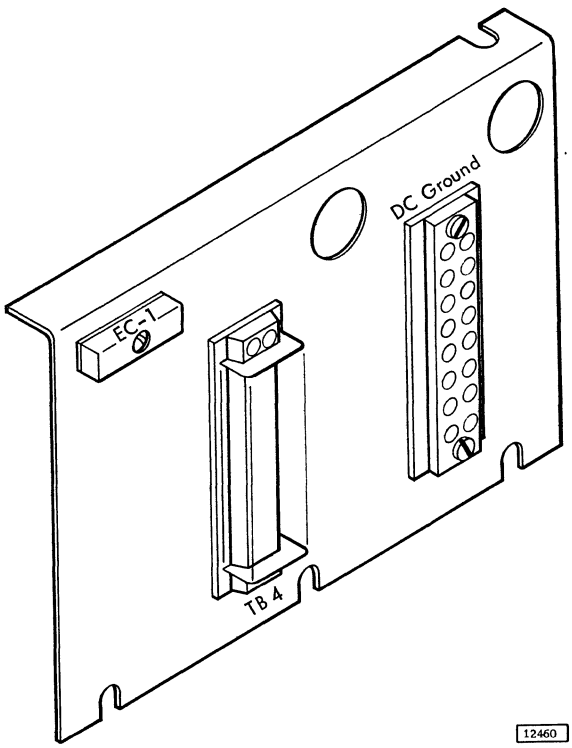


Figure 6-25. 1826–3 DC Power Panel

Gate A

2nd Line Adapter of 1st Comm Adapt or 2790 Adapter (Bd 1) B1	Sel Chan (Bd 1) or 2nd Line Adapt of 2nd Comm Adapt or 2790 Adapter (Bd 2) A1
1st Comm Adapter or 2790 Adapter (Bd 3) B2	Sel Chan (Bd 2) or 2nd Comm Adapt or 2790 Adapter (Bd 4) A2
S/360 Adapt (Bd 1) or 1st Line Adapt of 1st Comm Adapt B3	S/360 Adapt (Bd 2) or Sel Chan (Bd 3) or 1st Line Adapt of 2nd Comm Adapt A3

Priority Scan: S/360, Sel Chan, Comm Adapt, 2790

Gate B

1st Digital Input Adapter B1	2nd DI or 1st PC Adapter A1
3rd DO or 1st PI or 1st/2nd PC Adapter B2	4th DO or 1st/2nd PI or 3rd DI or 1st/2nd/3rd PC Adapter A2
2nd Digital Output Adapter B3	1st Digital Output Adapter (& Control) A3

Priority Scan: DO, PI, DI, PC

12461

Figure 6-26. 1826–2 SLT Board Locations

Gate A

2nd Line Adapter of 1st Comm Adapt or 2nd 2790 Adapt (Bd 1) B1	Sel Chan (Bd 1) or 2nd Line Adapt of 2nd Comm Adapt or 2nd 2790 Adapt (Bd 2) A1
1st Comm Adapter or 2nd 2790 Adapt (Bd 3) B2	Sel Chan (Bd 2) or 2nd Comm Adapt or 2nd 2790 Adapt (Bd 4) A2
1st Line Adapter of 1st Comm Adapt B3	Sel Chan (Bd 3) or 1st Line Adapt of 2nd Comm Adapt A3

Priority Scan: Sel Chan, Comm Adapt, 2790

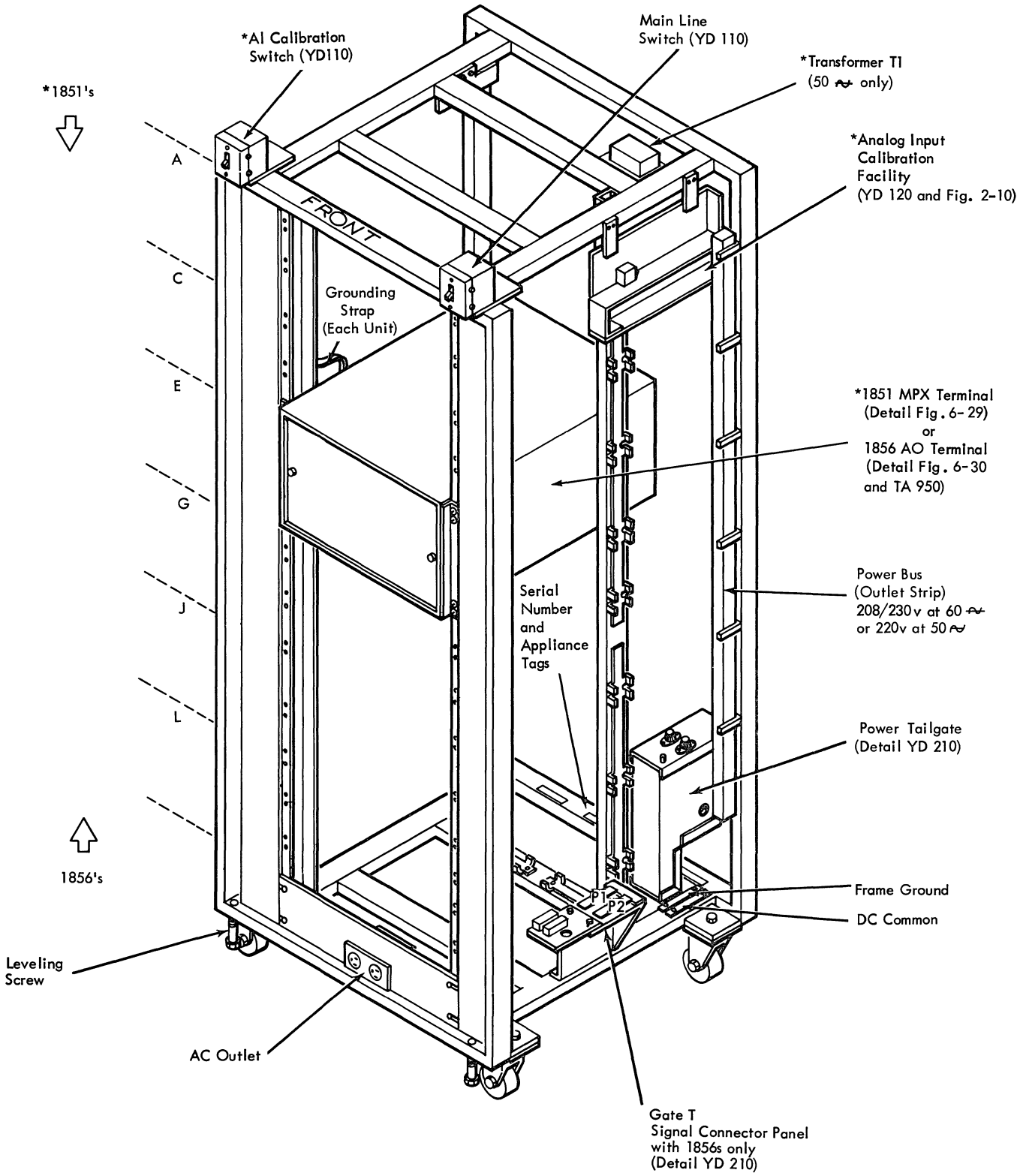
Gate B

2nd Line Adapter of 4th Comm Adapt or 1st 2790 Adapt (Bd 2) B1	2nd Line Adapter of 3rd Comm Adapt or 1st 2790 Adapt (Bd 1) A1
4th Comm Adapter or 1st 2790 Adapt (Bd 4) B2	3rd Comm Adapter or 1st 2790 Adapt (Bd 3) A2
1st Line Adapter of 4th Comm Adapt B3	1st Line Adapter of 3rd Comm Adapt A3

Priority Scan: Comm Adapt, 2790

12462

Figure 6-27. 1826–3 SLT Board Locations



*1828 Model 2 Only

2195700 | 14041E

Figure 6-28. 1828 Enclosure

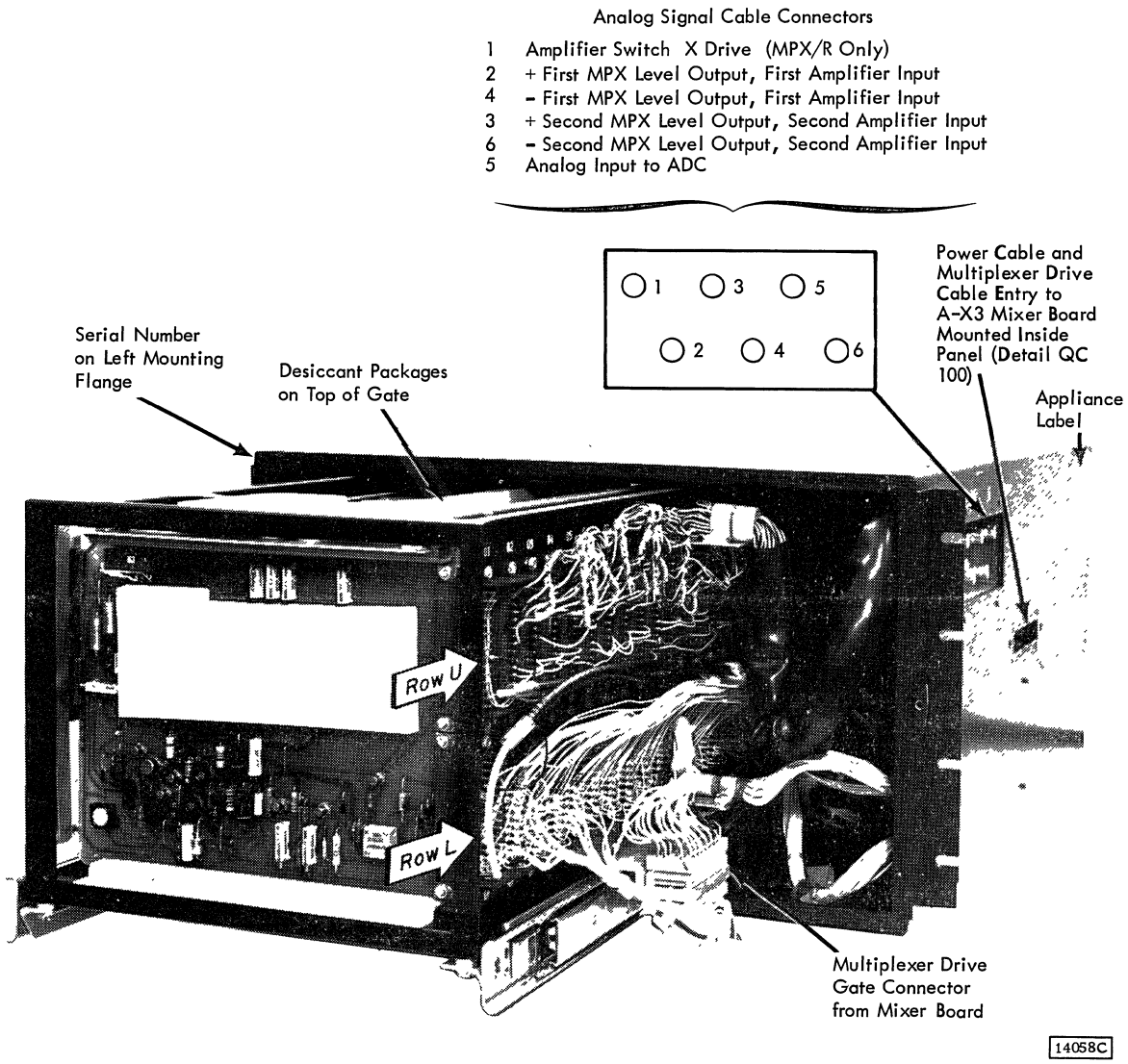


Figure 6-29. 1851 Multiplexer Terminal (Front)

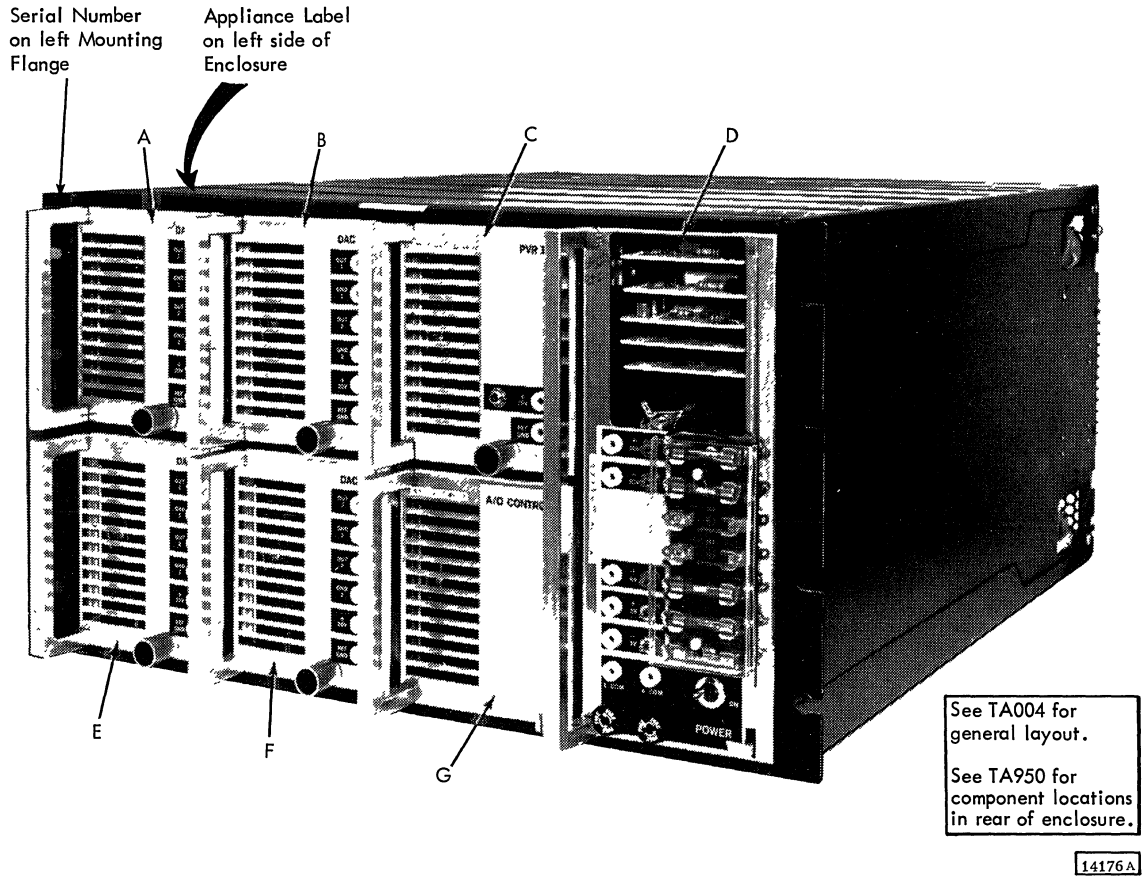


Figure 6-30. 1856 Analog Output Terminal (Front)

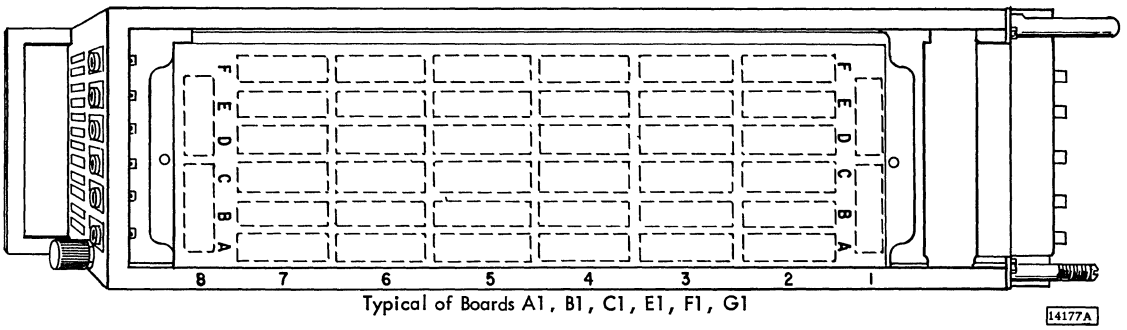


Figure 6-31. 1856 AO Board Coordinates

Appendixes

APPENDIX A. SPECIAL CIRCUITS

This manual makes no distinction between special and standard circuits.

APPENDIX B. WORLD TRADE

World Trade differences are covered in their logical places in the manual.

APPENDIX C. TOOLS AND TEST EQUIPMENT

Shipped with System

Description	P/N
I/O Monitor – shipped with each 1801/1802	2194933
Analog input calibrate facility – shipped in 1828 nearest the ADC	N/A
Portable start/stop box – shipped with each 1801/1802	N/A
Digital output test cable (if system has DO feature)	2195696
Digital input test card	2195669
Jumper assembly – core storage adj.	2182906
Cable assembly – differential scope leads	2182907
DAC extender (if system has 1856)	2182700

Not Shipped with System

Description	P/N
Hand wrap tool, 30 gauge or	452527
Power bit and sleeve (to be used with existing wire wrapping guns)	453090
Deletion tool with check light	452533
Wire stripper, 30 gauge	452528
Wire gripper	452529
Card offset extender (2)	452530
Probe tip (3)	452531
Pin aligner, card side	452535
Pin aligner, probe side	452536
Pin replacement kit	453158
Card extender, 6 pak	452554
Card extender, 12 pak	452555
Light, trouble	450147
Manual cart (holds 36 volumes)	453147
Headset, telephone, sound power (if system has remote 1826 or 1828 units) (2)	460260
Adapter cord – 1 for each headset	2108538
Adapter cord – 40 ft. (used to extend phone to System/360 console when system has System/360 channel to channel adapter feature)	460261
Adapter cord – used to connect two adapter cords (460261) together when System/360 console is over 40 feet away	2183478
Probe, plastic	453101
Wire caddy	453106
Thermometer	5392366
Indicator removal tool	461163
Scope, Tektronix 453 (The 453 is the recommended scope for the 1800)	453047
Current probe	451213
Probe termination	451214
Simpson Meter Model 260	450497
Weston 901 DC Meter (must have 3V and 15V range)	460879
Fluke Meter – (see 2.12.1)	453191
CE Indicator Latch Card	5801358
32 Inch SLT Jumpers	4203785
Core Jumper Block Removal Tool	2108860
4" SLT Jumpers	452655
CE Alignment screwdriver	460811
Jumperboards	2242726

Index