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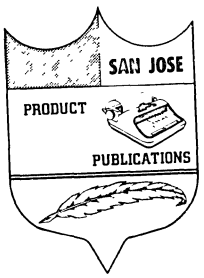

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1800 Data Acquisition and Control System Processor–Controller

SY26-5912-4

IBM Field Engineering

Theory of Operation

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Preface

System diagrams (logics) at the engineering change level of the 1800 system are included in each system shipment.

To fully understand the material presented in this manual, the reader should have a general knowledge of Process Control Systems and should be familiar with Solid Logic Technology (SLT) packaging and documentation.

This manual contains a comprehensive introduction to the IBM 1800 Data Acquisition and Control System, and specific descriptions of the IBM 1801 and 1802 Processor-Controllers. The input/output features and adapters are described in these additional manuals: IBM Field Engineering Theory of Operation, 1800 Data Acquisition and Control System, Data Processing Input/Output Features, Order No. SY26-3617, IBM Field Engineering Theory of Operation, 1800 Data Acquisition and Control System, Process Input/Output Features, Order No. SY26-5959, and IBM Field Engineering Maintenance Diagrams, 1800 Data Acquisition and Control System, Volume 1, Order No. SY26-4128, and Volume 2, Order No. SY26-4129.

The Maintenance Diagram Manual supplied with the 1800 system is intended to be used with this manual, The Maintenance Diagram Manual contains text, flow charts, timing charts, and various supplementary diagrams that assist in understanding the logical operations described in this manual. Page references, shown as (CS50101), refer to page numbers in the FEMDM. Page coordinates, e.g., E4, may follow the page reference. Page references which have only five characters, shown as (SA041), refer to page numbers in the ALDs.

Maintenance information for the Processor-Controller and its adapters is available in the IBM FE Maintenance Manual, 1800 Data Acquisition and Control System, Order No. SY26-5956.

Other Manuals, useful in understanding and maintaining the 1800 system, are listed in the IBM Field Engineering Bibliography, 1800 Data Acquisition and Control System, Order No. SY26-0560.

The appendixes of this manual contain special circuit descriptions, and other information of a supplementary nature.

Fifth Edition (February 1970)

This manual revises and makes obsolete the previous edition, Order No. SY26-5912-3. Changes to the text and illustrations are not indicated because of extensive rearrangement. Material was added for the 1803 Core Storage Unit, Communications Adapter, Selector Channel and Expanded Data Channel. Review the entire manual with emphasis on added material and addressing of auxiliary core storage with modifier bit 9. The MPX (Programming System) utilizes modifier bit 9 to address auxiliary storage with the following instructions: Store Accumulator, Load Accumulator, Logical AND, Logical OR, and Logical Exclusive OR.

Manuals referred to in this publication that have an Order No. with a four character prefix are identical in content to the same manual without the initial prefix character. (e.g. SY26-xxxx is the same in content as Y26-xxxx.)

Significant changes or additions to the specifications contained in this publication are continually being made. When using this publication in connection with the operation of IBM equipment, check the latest FE Publications Systems Sequence Listing, Order No. SY20-0073, for revisions or contact the local IBM Branch Office.

The illustrations in this manual have a code number in the lower corner. This is a publishing control number and is not related to the subject matter.

Copies of this and other IBM publications can be obtained through IBM Branch Offices.

A form for reader's comments is provided at the back of this publication. If the form has been removed, send your comments to the address below.

This manual was prepared by the IBM Systems Development Division, Product Publications, Department G24, San Jose, California 95114.

Contents

Abbreviations

A-reg.	accumulator register
ADA	analog driver amplifier
ADC	analog-to-digital converter
AI	analog input
ALD	automated logic diagram
AMAR	analog multiplexer address register
AO	analog output
ASCII	American standard code for information interchange
AWG	American wire gauge
aux	auxiliary
B-reg	storage buffer register
BCC	block check character
bfr	buffer
BO	Branch Out
BS	block switch
BSC	binary synchronous communications
BSM	basic storage module
CA	Communications Adapter
CAB	channel address buffer
CAF	customer assignment form
CAR	channel address register
CC	chain command
CCW	channel command word
CD	chain data
CEM	Customer Engineers Memorandum
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC-16	cyclic redundancy check (16 bits)
CRP	Card Read Punch (IBM 1442)
CS	cycle steal
CSA	cycle steal acknowledge
CSU	core storage unit
CSW	channel status word
D-reg	arithmetic factor register
DAC	digital-to-analog converter
DAO	digital and analog output
DAU	Data Adapter Unit (IBM 1826)
DC	data channel
DCU	data control unit
DDC	direct digital control
DET	double-emitter transistor
DI	digital input
DIMAL	disk maintenance library
DLE	data link escape
DO	digital output
DP	data processing
DPC	direct program control
DSW	device status word
EA	effective address
EBCDIC	extended binary-coded-decimal interchange code
EC	engineering change
ECA	engineering change announcement
ECAD	error check analysis diagram
ECO	electronic "contact" operate
ENQ	enquiry
EOC	end of conversion
EOT	end of table
EOT	end of transmission
EPO	emergency power off
ETB	end of transmission block
ETX	end of text
F-reg	format register
FC	feature code
FEALD	Field Engineering automated logic diagram
FEMDM	FE Maintenance Diagram Manual
FEMM	FE Maintenance Manual
FESRR	Field Engineering Systems Reference Report
FET	field-effect transistor
FETOM	FE Theory of Operation Manual
FF	flip-flop
FL	flip-latch
hex	hexadecimal
HLSE	high-level, single-ended
HSDA	high-speed data acquisition
Hz	hertz (cycles per second)
I-reg	instruction register
I/A	indirect addressing
ICAR	instrument calibration and repair
ILSW	interrupt level status word
I/O	input/output
IOCC	input/output control command
IPL	initial program load
ITB	intermediate transmission block
LA	line adapter
LRC	longitudinal redundancy check
LSB	least significant bit

M-reg	storage address register
MAR-2	Manufacturing Assembly Report #2 (field use)
MDM	maintenance diagram manual
MES	miscellaneous equipment specification
MI	multi-input
MLC	machine level control
MLR	machine location report
Mod-reg	modify register
MPS	medium power standard
MPX	multiplex(er), R-relay, S-solid-state
MPX	Multiprogramming Executive (Programming System)
NAK	negative acknowledgement
Op-reg	operation code register
P	parity
PC	pulse counter
P-C	processor-controller
PCI	program control interruption
PI	process interrupt
PID	program identification
PISW	process interrupt status word
PO	pulse output
POC	process operator's console
PVR	precision voltage reference
Q-reg	accumulator extension register
RBT	resistance bulb thermometer
RO	register output
RPQ	request for price quotation
SAR	storage address register
S&H	sample-and-hold (amplifier)
SC	shift counter
SCR	silicon-controlled rectifier
SCRID	SCR indicator driver
S/D	serializer/deserializer
serdes	serializer/deserializer
SI	single instruction
SIO	start input/output
SLD	simplified logic diagram
SLI	suppress length indicator
SLT	solid logic technology
SMS	standard modular system
SOH	start of heading
SPD	sample pulse driver
SRL	Systems Reference Library
SS	single-shot (multivibrator)
SSC	single storage cycle
STX	start of text
SYN	synchronous idle
T-reg	tag register
tag	selector channel control lines
TIC	transfer in channel
TSX	Time-Sharing Executive (Programming System)
TTD	temporary text delay
U-reg	temporary accumulator register
UDCD	unit data and control diagram
UJT	unijunction transistor
VRef	reference voltage (core storage)
VRC	vertical redundancy check
VSA	sense amplifier voltage (core storage)
WC	word counter
XIO	execute input/output
XR	index register
/	precedes hexadecimal numbers (base 16)

Chapter 1. Introduction

- The IBM 1800 Data Acquisition and Control System is designed to handle a wide variety of real-time applications, including process control and high-speed data acquisition.

- Extensive modularity permits customized configurations to satisfy both large and small system requirements.

- The use of solid logic technology (SLT) makes the system flexible and reliable and reduces maintenance requirements.

- The high-speed binary processor-controller can be used for editing, supervisory control, direct control or data analysis.

- Data-processing input/output attachments include magnetic tape units, disk storage units, graph plotters, printers, typewriters, and card and paper tape I/O units.

- Process input/output features permit both analog and digital communication between the 1800 system and the process.

The ever increasing pace of technology, industry, and business has created a need for timely, accurate, and reliable measurement of data at its source for rapid evaluation and control. The 1800 Data Acquisition and Control System has been designed to handle widely divergent real-time applications and to provide any degree of control from data logging and analysis to complete closed-loop control. Each system is individually tailored with modular components that are easily integrated to meet specific system requirements.

Components of the 1800 system are functionally separated into three categories: Processor-Controller (P-C), Data Processing Input/Output (DP I/O), and Process Input/Output. The Processor-Controller is the name given to the computer subsystem which includes the central processing unit (CPU), core storage, and I/O channel controls. The CPU employs a small, binary, stored-program computer which provides the means for evaluating the acquired data and controlling the acquisition process. Within its basic design, the CPU has interrupt and cycle-stealing capabilities for on-line, real-time operating environment. Index registers and indirect addressing are provided to facilitate address modification and programming.

Components of the IBM 1800 Data Acquisition and Control System can be used in three basic configurations:

1. The 1800 system process I/O equipment attached to the processor-controller with any necessary data processing I/O units. The minimum system will satisfy initial control and analysis requirements and can be expanded to support medium-scale applications.
2. The 1800 system process I/O equipment attached directly to a System/360, Model 25, 30, 40, 44 or 50. This configuration is well suited to medium-scale, real-time applications involving substantial data processing loads.
3. One or more 1800 systems (processor-controllers, each with appropriate process I/O equipment) attached via channel adapters to a System/360. This configuration is suited to large-scale, real-time applications and can be expanded to supply almost any combination of data processing capability and real-time input/output channel capacity.

SYSTEM DATA FLOW

- Data is processed in fixed-length 16-bit words for fast parallel manipulation.

- The I/O devices are linked to the processor-controller via a standard I/O interface.

- Adapter circuitry for each I/O device performs the necessary conversion, buffering, and control functions.

- Cycle-stealing capability permits high-speed transfer of data.

In the 1800 system, a standard I/O data interface is used between the processor-controller and all input/output devices. Adapter circuits to accommodate each type of I/O device are installed in the 1800 system as

required. The adapters provide the necessary buffer registers and controls to permit on-line operation of the associated device.

Figure 1-1 shows the data flow between the processor-controller and the various I/O devices. In a closed-loop control system, process conditions are monitored and analyzed continuously, and controlling signals are sent to the devices that control the process. Input data is obtained directly from measuring devices in the process area without the need for off-line conversion equipment. Electrical signals are accepted in analog or digital form from such devices as thermocouples, pressure transducers, digital voltmeters, and contacts. Signal conditioning, multiplexing, and conversion functions are performed by the input circuits. The input data, in digital form, is retained in registers until called for entry into core storage.

After the input data has been read and analyzed by the processor-controller, the program may select a process control function. Both digital and analog output data are available for controlling equipment such as set-point positioners, displays, and telemetry systems. Data processing information can be entered and retrieved in a variety of forms through the Data Processing I/O units and their adapter circuits.

Adapters are available which permit the attachment of other systems and I/O devices. The System/360 adapter permits the attachment of the 1800 system to a channel of a System/360 model 25, 30, 40, 44, or 50. Each system may regard the other as an I/O device capable of requesting service on a random basis. The 1800 selector channel allows the attachment of the 2841 storage control unit with up to eight 2311's attached and other System/360 I/O control unit/devices by RPQ. The communications adapter permits attachment of one or two communications lines to allow communication between the 1800 system and remote systems or devices which operate in binary synchronous communications mode. The 1800/2790 adapter establishes the 1800 system as the "system controller" in a 2790 Data Communication System.

The interrupt capability makes it possible to suspend the normal program in order to service priority conditions that arise within the system or the process. Thus, when an I/O device is ready to send or receive data, it can notify the processor-controller by issuing an interrupt request. The program identifies the source of the interrupt by sensing the status of indicators associated with each interrupt.

The processor-controller services the interrupt by sending the appropriate I/O command to the device. I/O commands always place a "control word" on the out-bus to specify the input/output device and the function to be performed. Depending on the intrinsic data rate of the I/O device receiving the control word, the transfer of data between core storage and the device can take place under direct program control or on a data channel. A data channel transfers data on a high-speed, cycle-stealing basis using a data table and core storage for flexibility of scanning rates and patterns. The cycle-stealing capability makes it possible to delay the program for one machine cycle and to use this cycle to transfer the data word between core storage and the I/O device. Cycle stealing and interrupt servicing are conducted by the channel control logic on a priority basis. This makes it possible to simultaneously control combinations of real-time input/output devices.

PHYSICAL DESCRIPTION

- System units employ drip-proof, splash-proof industrial enclosures.
- The 1801 or 1802 Processor-Controller is a two-bay enclosure that houses the basic system components.
- The 1803 Core Storage Unit is a single-bay enclosure that houses additional core storage modules.
- The 1826 Data Adapter Unit is a single-bay enclosure that provides additional space for feature expansion.
- The 1828 Enclosure is a single-bay enclosure that provides rack mounting for analog input/output subenclosures.
- The 1810 Disk Storage is a single-bay enclosure that houses 1, 2, or 3 Single Disk Storage units and their adapter circuits.
- All components except cable terminations and power supplies are accessible from the front of each unit.
- Customer signal cables are connected to screw-down terminals at the rear of the unit.
- DP I/O equipment provides its own enclosures which are cabled to the basic two-bay enclosure.

The enclosures for the processor-controller and the process I/O features of the 1800 system are designed

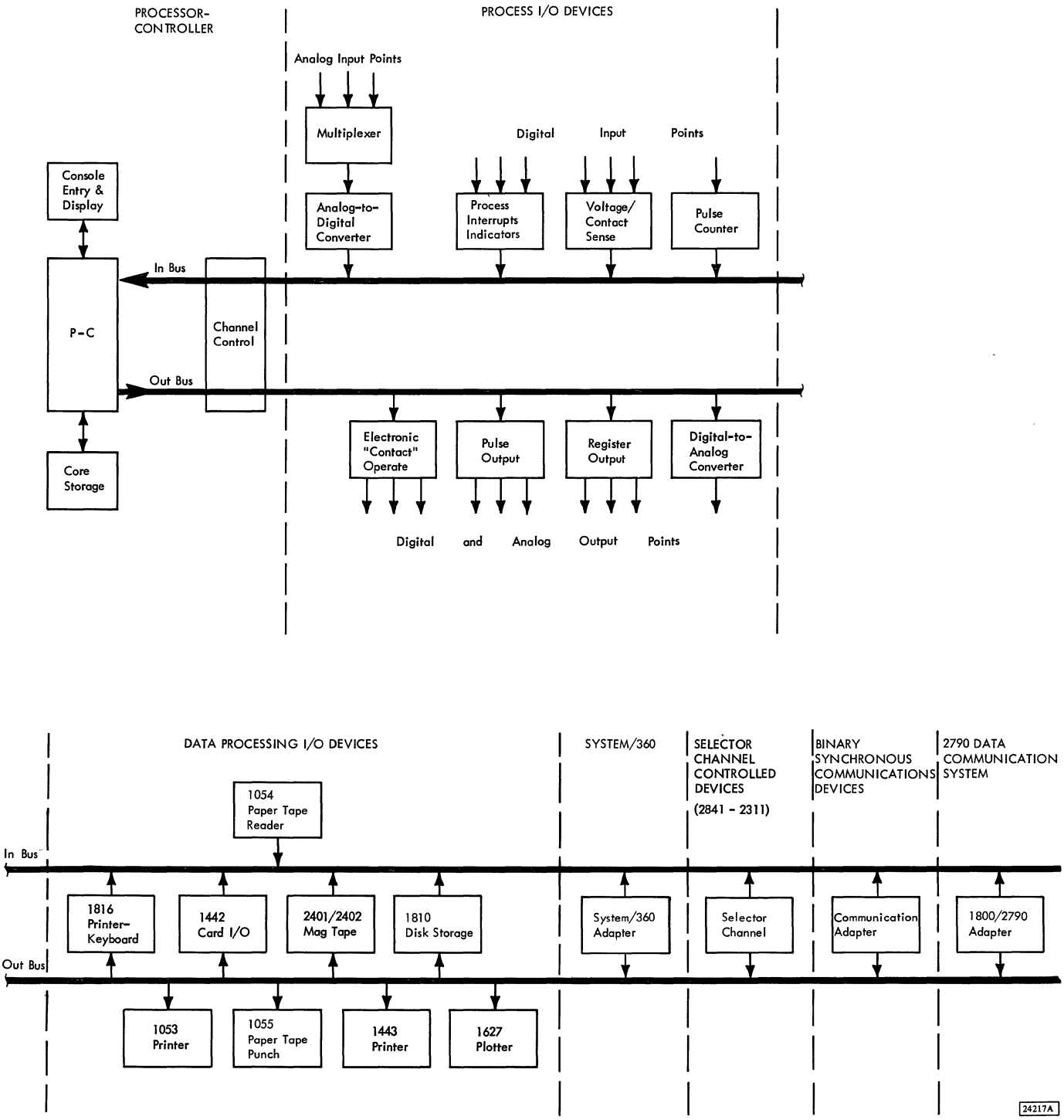

Figure 1-1. IBM 1800 Data Acquisition and Control System I/O Interface

specifically for industrial application. Interconnecting machine cables are supplied by IBM for use between separated units and are connected in a designated connector area near the bottom of each enclosure. Cables are either pluggable or quick-disconnect type with provision for bottom or back entry as required. Customer wiring terminates in designated customer access areas at the rear of the enclosures. All customer signal termination is designed for use with two-wire twisted pair.

The basic two-bay enclosure is 76" high, 33" deep, and 61-1/2" wide. The single-bay enclosures are 76" high, 33" deep, and 31-1/2" wide. The single-bay enclosures bolt to each other or to the two-bay enclosure by removing the side cover. The cabling between abutted units is internal.

The design of the enclosures permits mounting two swing-out, 3 x 2 SLT gates in tandem for front accessibility in each bay. The single-bay enclosures also permit stacked installation of rack-type subenclosures (as in the 1828) or slide-out Single Disk Storage units (1810).

Selective features and units of the 1800 system are packaged as discrete functional assemblies, thus permitting disconnection or attachment to the system without affecting the performance of other features or units.

IBM 1801 and IBM 1802 Processor-Controller (Two-Bay Enclosure)

Figures 1-2 and 1-3 illustrate the relative placement of components in these two-bay enclosures. The power supplies are mounted in vertical tubs at the rear of the left bay. The programmer's console and the I/O monitor interface (CE panel) swing open from the front to provide access to the SLT gates in the right bay. In the 1801, a customer access area is

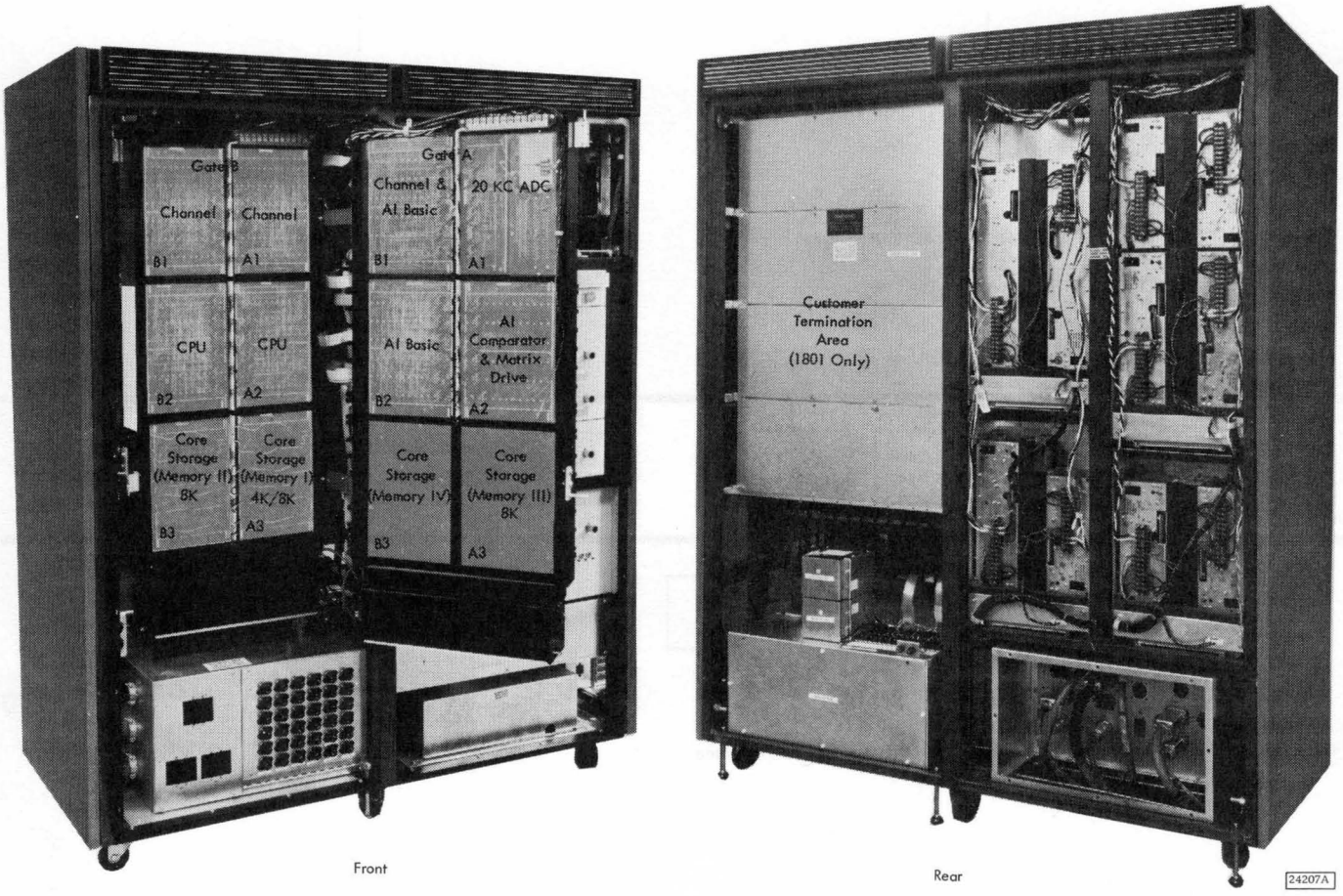

Figure 1-2. 1801 or 1802 Processor-Controller, Gates A and B

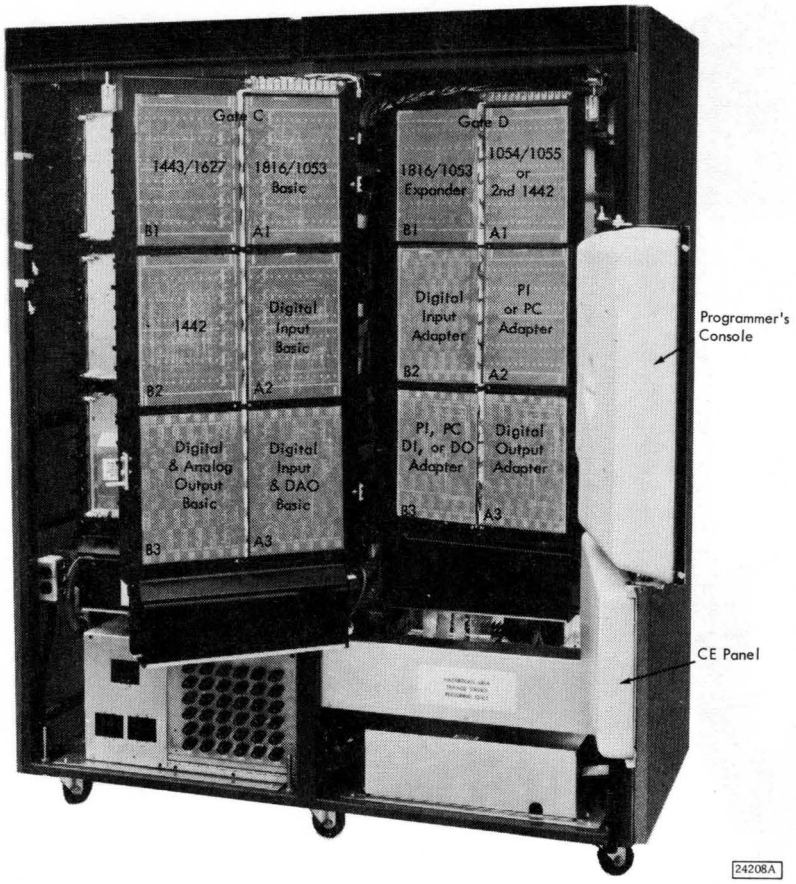

Figure 1-3. 1801 Processor-Controller, Gates C and D

provided at the rear of the right bay to permit customer termination of process wiring for digital I/O features.

The 1802 Processor-Controller is identical to the 1801 except that the tape control unit usurps all the space allocated for digital I/O in the 1801 (Figure 1-4).

IBM 1803 Core Storage Unit (Single-Bay Enclosure)

The IBM 1803 Core Storage Unit is a free standing unit designed to allow for expansion of core storage size above the 32,768 words available in the 1801 or 1802 Processor-Controller. With the additional storage feature, 24,576 core storage words are contained in the 1801 or 1802 with the additional storage in the 1803. The 1803 is available with 16,384 to 40,960 core storage words, in increments of 8192 words, for a maximum system core storage capacity of 65,536 words.

IBM 1826 Data Adapter Unit (Single-Bay Enclosure)

When the feature capacity of the basic enclosure is exceeded, additional single-bay enclosures are employed. The 1826 Data Adapter Unit is supplied in three models. Models 1 and 3 are free-standing, connected by external cables to the processor-controller. Model 2 bolts directly to the operator's right of the 1826-1, the processor-controller, or another 1826-2, and all cabling to attached units is internal. Several 1826-2 bays may be bolted to an 1826-1 as a stand-alone unit cabled to the

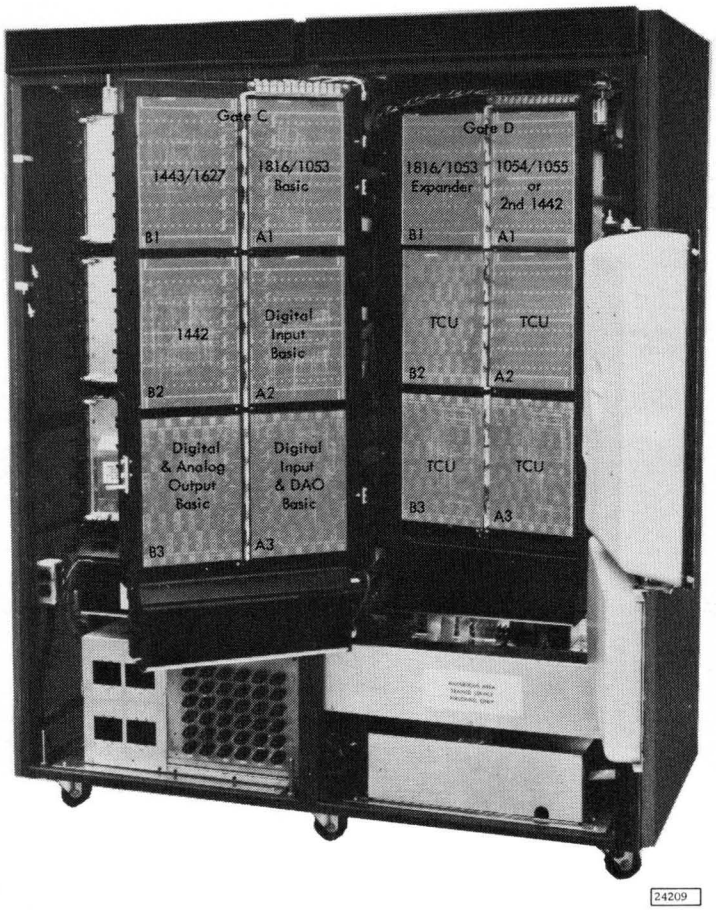

Figure 1-4. 1801 Processor-Controller, Gates C and D

processor-controller. The cabling distance may be up to 100 feet. In addition, several 1826-2 enclosures may be bolted to the left of the 1826-1 Data Adapter Unit. Each 1826 bay accommodates two SLT gates with front access, and provides a customer access termination area at the rear. Figure 1-5 illustrates the space allocation for features within the enclosure.

IBM 1828 Enclosure (Analog I/O Single-Bay)

This single-bay enclosure is dimensionally the same as the 1826, but is designed expressly for accepting special subenclosures for analog input and analog output features. The 1828 Enclosure is supplied in two models. Model 1 is a free-standing enclosure for analog output features and is externally cabled to the processor-controller at distances up to 100 feet. Model 2 is a bolt-on enclosure for analog input and analog output features, and all cabling to attached units is internal. The 1828-2 may be bolted directly to the operator's left of the 1828-1, the 1826-1, the processor-controller, or another 1828-2. Figure 1-6 illustrates this enclosure.

IBM 1851 Multiplexer Terminal (Subenclosure)

This unit provides termination for analog input lines and mounting for multiplexer cards. The 1851 model 1 is used for standard (non-thermocouple) signals.

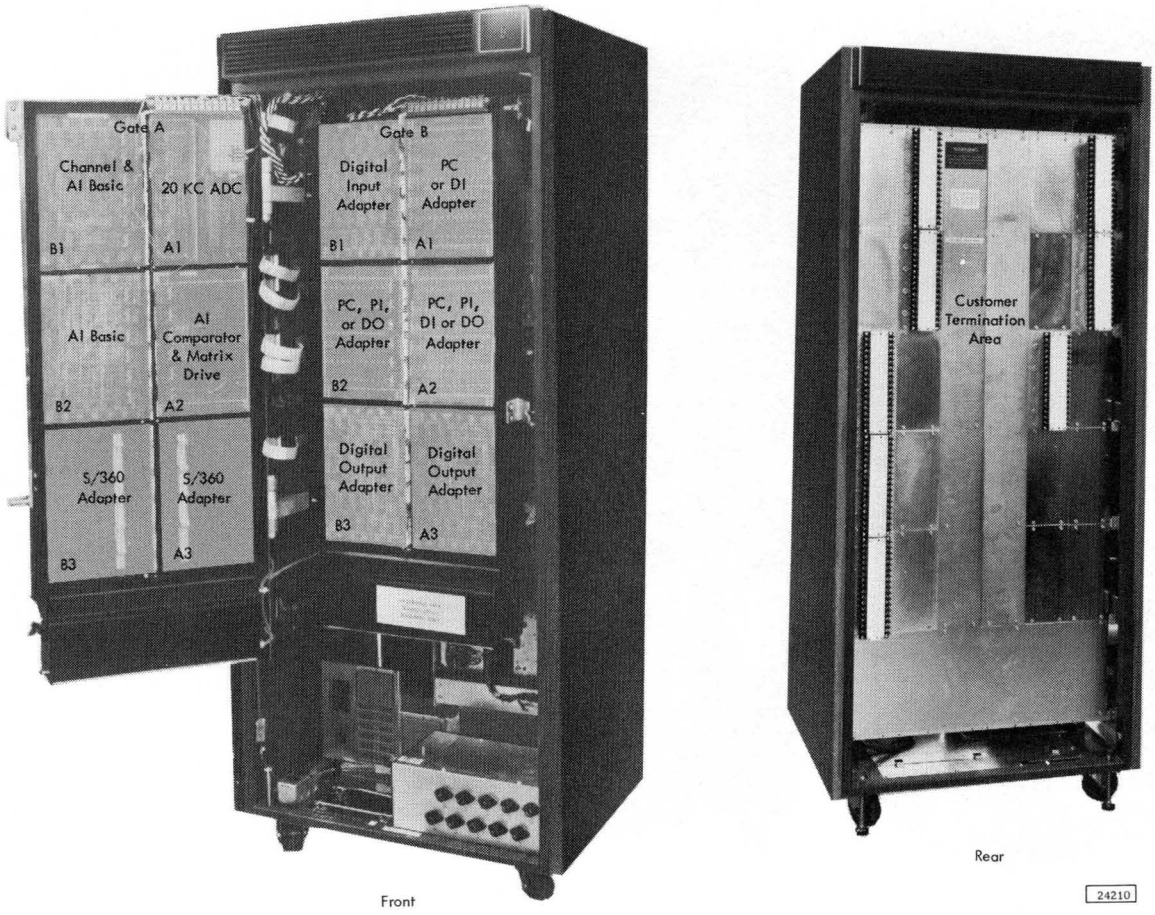

Figure 1-5. 1826 Data Adapter Unit

The 1851 model 2 may be used for both standard and thermocouple signals. A card gate slides out from the front of each unit for access to the special-size component cards used in the multiplexer circuits.

These units feature standard 19" rack mounting dimensions. Up to six units may be stacked in a single 1828 Enclosure.

IBM 1856 Analog Output Terminal (Subenclosure)

This unit provides termination, power, and housing for analog output features. The features which are housed in the 1856 are plug-in modules that fill 1/8 or 1/4 of the unit space. The 1856 unit dimensions are the same as the 1851.

IBM 1810 Disk Storage (Single-Bay Enclosure)

The 1810 Disk Storage (Figure 1-7) is available in three models. In the model A1 or B1, the single-bay enclosure contains power supplies, a 3 x 1 SLT gate, and one Single Disk Storage. In the model A2 or B2, a second Single Disk Storage is added, and in Model A3 or B3 a third Single Disk Storage is added. The models are free-standing and are connected by external cables to the processor-controller.

SLT Board Locations

The modular design of the 1800 system allows some flexibility in the assignment of board and

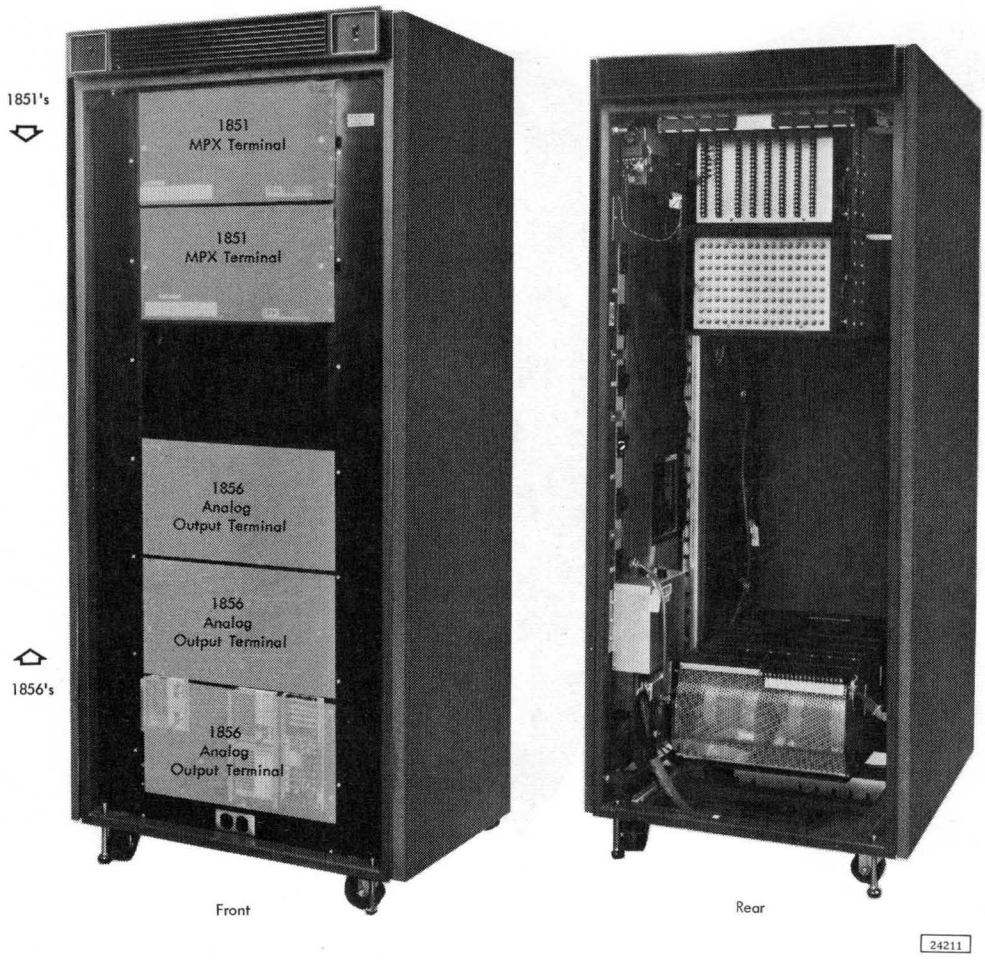

Figure 1-6. 1828 Enclosure, Model 2

subenclosure locations to suit various system requirements. For this reason, the following nomenclature has been established for use in the System Diagrams:

1. If a board location is confined to a single frame, it carries that frame designation. The last two numbers of the machine type are used as frame designation; i.e., 1803 = 03, 1826 = 26, 1810 = 10, etc. If a board can be located in more than one frame or in the 1801/1802 main frame, it carries a frame designation of "60".
2. If a board location is confined to a single gate, it carries that gate designation. If the board can be located on more than one gate, it carries a pseudo gate designation of X, Y, or Z.
3. If the board position on a gate is fixed, it carries that board designation by column and row coordinates. If the board can be located at more than one position on a gate, it carries a pseudo column designation of V, W, X, Y, or Z; the row number designation is used in this case only to provide a unique number for each board.

In most cases, pseudo designations serve no purpose other than to indicate that the board has multiple locations. It is then necessary to consult the gate configuration charts in the System Diagrams and locate the board by its name.

PROCESSOR-CONTROLLER

- The 1801 and 1802 Processor-Controllers are stored program computers, consisting of a

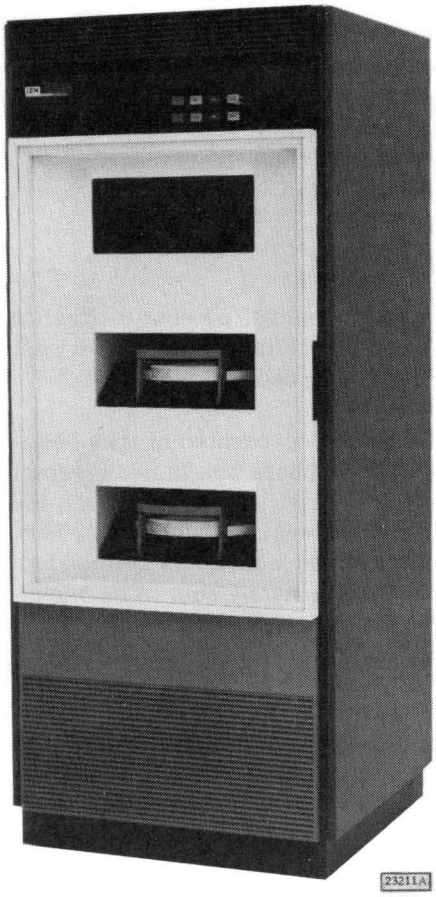

Figure 1-7. 1810 Disk Storage, Model A2

central processing unit (CPU), core storage, and I/O channel control circuits.

- The 1802 differs from the 1801 only in that it contains control circuitry for magnetic tape operation.
- The 1801 or 1802 Model 1 basic machine cycle time is four microseconds.
- The 1801 or 1802 Model 2 basic machine cycle time is two microseconds.
- When a system includes an 1803, the basic machine cycle time is 2.25 microseconds.
- Either model of 1801 or 1802 is available with core storage capacity of 4,096 (4K); 8,192 (8K); 16,384 (16K); 24,576 (24K); or 32,768 (32K) 18-bit words.
- Standard features of the processor-controller include:
  - Three index registers
  - Twelve levels of interrupt
  - Three data channels
  - Three interval timers
  - An operations monitor
  - A programmer's console
- Input/Output interface accommodates adapter circuitry for attaching data processing I/O equipment and process I/O equipment.
- The registers and control circuits that make up the CPU are contained on two SLT boards.
- The basic machine clock cycle of 4 microseconds or 2 microseconds is divided to fetch a word from storage (storage read cycle) and then replace the same word or a new word (storage write cycle).
- Core storage words can be instructions that control the operation or data to be operated upon.

STORED PROGRAM CONCEPT

- The stored program consists of all words in core storage that are addressed by the contents of the instruction register.
- Instructions are normally stored and executed sequentially, beginning with address 0000_{16}.
- Sequential execution of a program can be altered by changing the contents of the instruction register.
- Program instructions can be modified by conditions set forth in the program.
- Program is loaded initially from a designated card or paper-tape input unit, or manually from console switches.
- Additional instructions can be entered into core storage during the course of a program.
- There can be any number or degree of subroutines within the main program.

The entire series of instructions required to complete a given procedure is known as a program. In the 1800 system, the program is stored internally in magnetic cores and the system has access to the instructions at electronic speeds.

The possible variations of a stored program provide the computer with almost unlimited flexibility. Once the basic program is loaded, the computer has the ability to initiate a change in the program in response to conditions encountered during an operation. Consequently, the computer exercises some degree of selection within the framework of the possible operations that can be performed.

The program is initially loaded into core storage from an IBM 1442 Card Read Punch or an IBM 1054 Paper Tape Reader. One of these units is specified as the "initial program load" (IPL) device.

There are no particular areas of core storage reserved for instructions only. In most cases they are grouped together and placed in ascending sequential locations in the normal order in which they are to be executed by the computer. The instructions are addressed sequentially from an instruction register (counter) that is advanced with each instruction cycle. The order of execution may be varied at any point in the program by a "branch" instruction that changes the contents of the instruction register.

An instruction in core storage is literally indistinguishable from data. The only thing that actually distinguishes an instruction from data is the time at which it is brought from core storage. If a word is read out of core storage during an instruction cycle, it goes to the control registers and is interpreted as an instruction. If a word is read out of core storage during any other cycle, it is considered to be data. This makes it possible to operate on instructions in storage and modify them as though they were data.

Additional instructions and/or data may be read into core storage from any system input device or read out of storage into any system output device.

MACHINE LANGUAGE

- Data and instructions are handled in binary form in 16-bit words.
- Hexadecimal notation is used to represent the machine language.
- Two-word format allows data and instruction words of 32 bits.
- Negative numbers are handled and stored in two's complement form.

The binary system enables the representation of numbers by any bi-stable means such as the on or off state of a flip-flop, the up or down level of a signal line, or the direction of the field about a magnetic device. In core storage, each bit value is stored in a magnetic core; in data registers, each bit value is stored as the on/off condition of a flip-flop or flip-latch.

The binary representation of data best facilitates the parallel manipulation of fixed-length words and is the most efficient method of processing scientific data.

Data Format

In the 1800 system, the standard, or single-precision data word (Figure 1-8) is 16 bits in length. Bit positions 0 through 15 represent decimal values of 2^{15} through 2^0 respectively.

Positive numbers are represented in true binary form, whereas negative numbers are in two's complement form. The sign bit (position 0) is always 0 for positive numbers and 1 for negative numbers. The two's complement of a binary number is defined as its one's complement increased by one. The one's complement of a binary number is that number that results by replacing each 1 in the number with a 0, and each 0 with a 1.

The largest single-precision positive number that can be represented is $2^{15}-1$, or 32,767 (a sign bit of 0, and 1's in all other bit positions). The largest negative number is -2^{15} or -32,768 (a sign bit of 1, and 0's in all bit positions). The number 0 is represented by all bits being 0; there is no negative 0.

A double-precision number of 32 bits can be used to give a number range from +2,147,483,647 to -2,147,483,648 ($2^{31}-1$ to -2^{31}). Two adjacent words must be used in storage with the high-order word at an even address, and the low-order word at the next higher odd address (Figure 1-9).

Instruction Format

The instruction defines the basic operation to be performed and contains the factors necessary for developing a core storage address. This core storage address is called the effective address (EA).

Two basic instruction formats are used: a single-word instruction and a two-word instruction (Figure 1-10). The two-word instruction contains the full

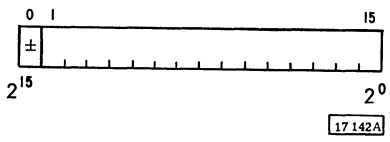

Figure 1-8. Single Precision Data Word

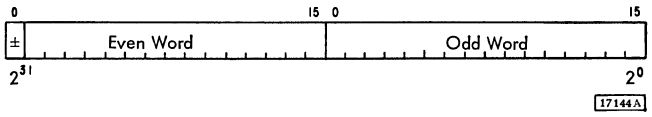

Figure 1-9. Double Precision Data Word

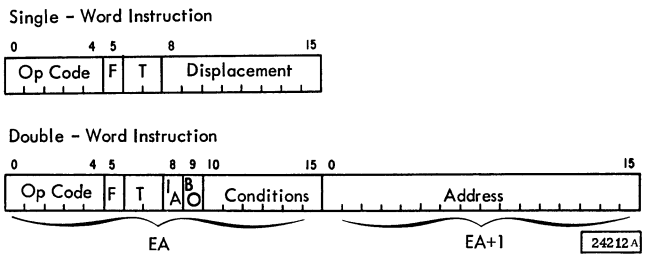

Figure 1-10. Instruction Word Format

core storage address in the 16 bits of the low order word. The single-word instruction is used when it is not necessary to furnish the full core storage address, but only to modify (displace) a base address already existing in a designated 16-bit register. The displacement bits, 8 through 15, can be used to address a range of core storage locations from 127 addresses above the base address to 128 addresses below the base address.

The address portion of a two-word instruction can also be modified by adding to the contents of a designated 16-bit index register.

The bits within the instruction are used in the following manner:

Op Code

The operation to be performed by the instruction is defined by these five bits. There are 26 valid op codes.

Format (F)

This bit selects the instruction format. A "0" indicates a single-word instruction and a "1" indicates a two-word instruction.

Tag (T)

These are the index tag bits used to select a register for address modification.

Displacement

These eight bits define the displacement value and are added to the register specified by the tag bits to develop the effective address (EA). Displacement may be in either a positive or negative direction as determined by the sign of the displacement value. A negative displacement value will be in two's complement form with a bit in position 8.

Indirect Address (IA)

This is the indirect address bit in the two-word instruction format except in the modify-index-and-skip instruction with a tag 00 specified. If "0", addressing is direct. If "1", addressing is indirect.

Branch Out (BO)

This bit is used to specify that the branch-or-skip-on-condition instruction is to be interpreted as "branch-out-of-interrupt routine."

Conditions

These six bits specify the indicators to be tested on a branch-or-skip-on-condition instruction.

Address

These 16 bits usually specify a core storage address in a two-word instruction. The address can be modified by the contents of an index register or used as an indirect address if the IA bit is on.

Instruction Set

The 1800 instruction set is shown in Figure 1-11. Each instruction falls into one of five classes. Note that the instructions which may be modified with indirect addressing are indicated in the indirect addressing column. Some instructions perform multiple uses as specified by their control bits.

Functions of each instruction are given in the Principles of Operation chapter of this manual.

CORE STORAGE ADDRESSING AND DATA FLOW

- Program instruction and data are stored in core storage and are manipulated through the registers shown in FEMDM CC10101.
- The storage control circuitry and a core array (4K or 8K) are contained on one SLT board. A maximum of eight core storage SLT boards can be included in each system.
- Core storage is addressed by circuits that are activated by a decode of the storage address register (M register).
- Core storage is also addressed by the channel address register during data channel (I/O) operations.
- Information read from storage is stored in a storage buffer register (B register) until needed.
- The information written into core storage is controlled by the contents of the B register.

When the processor-controller power is turned on, a power-on-reset pulse resets the control circuitry and most of the registers in the processor-controller.

Class	Instruction	Indirect Addressing	Mnemonic
Load and Store	Load Accumulator	Yes	LD
	Double Load	Yes	LDD
	Store Accumulator	Yes	STO
	Double Store	Yes	STD
	Load Index	**	LDX
	Store Index	Yes	STX
	Load Status	No	LDS
	Store Status	Yes	STS
Arithmetic	Add	Yes	A
	Double Add	Yes	AD
	Subtract	Yes	S
	Double Subtract	Yes	SD
	Multiply	Yes	M
	Divide	Yes	D
	And	Yes	AND
	Or	Yes	OR
	Exclusive Or	Yes	EOR
Shift	Shift Left Instructions		
	Shift Left Logical (A) *	No	SLA
	Shift Left Logical (AQ)*	No	SLT
	Shift Left and Count (AQ)*	No	SLC
	Shift Left and Count (A) *	No	SLCA
	Shift Right Instructions		
	Shift Right Logical (A)*	No	SRA
	Shift Right Arithmetically (AQ)*	No	SRT
	Rotate Right (AQ)*	No	RTE
Branch	Branch and Store I	Yes	BSI
	Branch or Skip on Condition	Yes	BSC(BOSC)
	Modify Index and Skip	**	MDX
	Wait	No	WAIT
	Compare	Yes	CMP
	Double Compare	Yes	DCM
I/O	Execute I/O	Yes	XIO

* Letters in parentheses indicate registers involved in shift operations.
** See the section for the individual instruction (MDX and LDX)

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Figure 1-11. Instruction Set

The clock is stopped, but the basic oscillator is running and generating phase A and phase B pulses.

For the computer to perform any program operation, instructions must be in core storage. Instructions can be stored, one at a time, from the console data-entry switches, but an input device capable of initial program load (IPL) can quickly load an entire program.

With instructions stored in core storage, pressing the reset key sets the instruction register to 0000 (reset does not affect the contents of core storage or index registers). Now, when the start key is pressed, the computer brings out the word from core storage location 0000 and places it in a register. This storage read-out occurs on the first half of the cycle. This 16-bit word is the first computer instruction word. Portions of this word are placed in the Operation, Format, Tag, and Modifier registers. The contents of these registers determine what will happen during the next cycle.

On the second half of the cycle, the word is saved by writing it back into core storage.

The first major function, then, in any machine cycle is to read the contents of a core storage location and place them in a buffer register. In order to read a predetermined word from core storage, an address must be stored in a register from which core storage can be addressed. The M register performs this function (Figure 1-12). Positions 3 through 15 of the M register are sufficient to address up to 8K of core storage. M register positions 3 through 8 are decoded by the X decode circuits; positions 9 through 15 are decoded by the Y decode circuits.

During the first half of the core storage cycle, the X and Y decode circuits control the read drivers. The read drivers that are controlled by the X decode circuits cause current to flow in one direction through the X drive lines of the core array. The read drivers that are controlled by the Y decode cause current to flow in the same direction through the Y drive lines of the core array. Due to the address decoding, these currents coincide and flow through the cores in the addressed word only. The magnetic field of each core that is set to a 1-bit condition is reversed to the 0-bit condition by the read drive current. This change in the magnetic field causes a signal to be induced on a third winding, called the sense/inhibit winding. There is a sense/inhibit winding for each bit position. During the first half of the cycle, this winding is used to conduct the induced sense pulse to the buffer (B) register. Each active sense winding turns on its respective position of the B register.

During the first half cycle, the computer has addressed one core storage word and placed that word in the B register.

Remember that the read drive current reversed the magnetic field of all the cores in the addressed word to the 0-bit condition. In order to retain this data, the second half of the core storage cycle writes the contents of the B register back into the same core storage word. The address in the M register is unchanged, therefore the same X and Y decode circuits are active.

During the second half of the core storage cycle, the X and Y decode circuits activate the write drivers to cause current to flow in the same windings, but in a direction opposite to that caused by the read drivers.

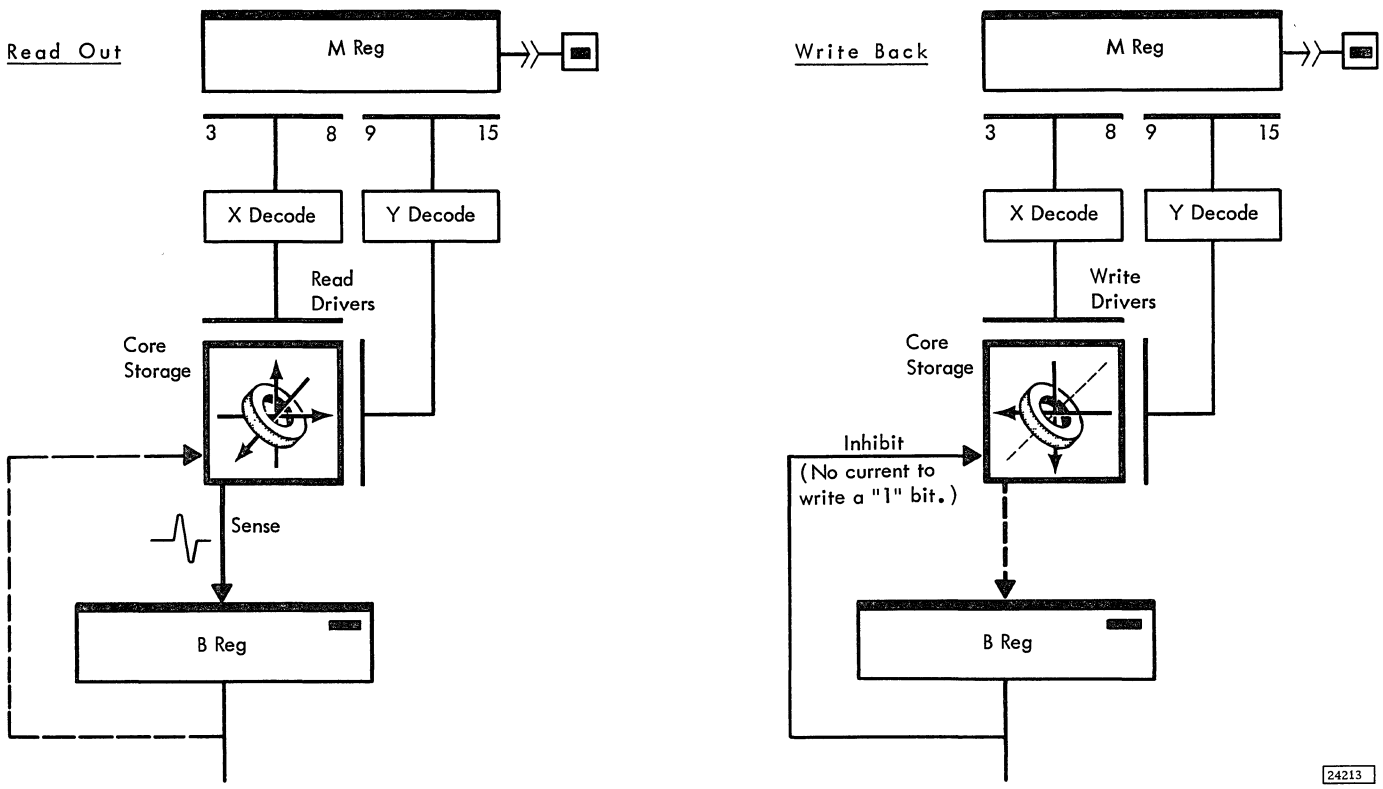


Figure 1-12. Core Storage Read-Write Cycle

This current is sufficient to cause all the cores in the addressed word to be magnetized in the one-bit condition.

Because only the bits that are active in the B register are to be written, nothing is done to prevent these bits from being set to the 1-bit condition. At the same time, however, circuits cause a current to flow in the third winding (sense/inhibit winding) of the bits whose B register positions are inactive. This current is in a direction opposite to the current flowing in the X drive lines. This inhibit current cancels the effect of the X drive current and prevents setting those cores, whose B register positions are inactive, to a 1-bit condition.

The contents of the B register are not changed by this write-back operation. Therefore, at the end of this core storage cycle, the contents of the addressed core storage location are in the B register and are unchanged in the original core storage location.

This basic read-write operation occurs every core storage (machine) cycle. This first cycle after a reset is an instruction cycle. The purpose of the first instruction cycle of any operation is to analyze the instruction word to determine the operation to be performed and to set up the registers that control the operation. These control registers are loaded with the contents of the B register during the first half of the cycle.

The control registers include the operation register, the format and tag registers, the shift counter, and the modifier register. A decode of the operation code activates the lines that gate information from the B register to other registers. The format register defines the operation as a one word or two word instruction. The tag register specifies one of the three index registers or the I register to be used during this instruction.

The shift counter is a dual-purpose register. For most instructions, it is loaded by hardware means, rather than from the B register, to indicate the number of cycles necessary for the specified operation. For shift operations, it is loaded from the B register or from an index register to control the number of shifts to be performed. It is decremented with each cycle or with each shift to accomplish its function.

The modifier register (bit 8-IA and bit 9-BO) is used by some operations to specify various functions to be performed by one op code.

Being a stored-program system, the 1800 system must execute instructions, stored in core storage, in

a prescribed sequence. A register must be provided to keep track of the address of the next instruction to be performed. This register is the instruction register (I register). At the beginning of each instruction cycle, when an instruction word must be read from core storage, the contents of the I register are transferred to the M register. Immediately after I is transferred to M, the I register is incremented one address, so that it always contains the address of the next instruction to be performed.

If the address that is to be used to address core storage, the effective address, is to be generated during one I cycle, it is generated by adding part of the instruction word contained in the B register to the contents of the I register, or to the contents of one of the three index registers. An adder of some sort is therefore required. All additions are made to the accumulator (A register). An additional register is required to contain the other factor of an add operation. This arithmetic factor register is called the D register.

Unique circuit connections and controls between the D register and the accumulator enable add and subtract operations.

To generate an effective address in one I cycle for a short format instruction, the CPU must be able to transfer the contents of the I register or one of the index registers to the accumulator. The other factor of the addition is a part of the instruction word contained in the B register, therefore, the D register is located between the B register and the accumulator. The contents of the D register are then added to the contents of the accumulator and the result (effective address) remains in the accumulator at the end of the I cycle.

At the beginning of the cycle which uses this effective address, the contents of the accumulator are transferred to the M register to address core storage.

Some instructions require that more than 16 bits be operated upon during the E cycles of one instruction. Therefore, another 16-bit register is connected to the accumulator. This register is called the accumulator extension register or Q register. Binary bits in the accumulator can be shifted from the low order position of the accumulator into the Q register, or the entire 16-bit word can be transferred from the accumulator to the Q register, or from the Q register to the accumulator.

The objectives of some operations are to modify a data word that has been previously loaded into the accumulator. Because the accumulator is used to generate an effective address during the I cycle, a temporary storage is needed for the accumulator word. This temporary storage register is called the U register. Sixteen-bit words can be transferred from the accumulator to the U register, and from the U register to the accumulator.

The basic data flow for internal CPU operations consists of the 16 data bits that are sensed in core storage and set into the B register and into the Op, format, tag, and modifier registers during the instruction cycle. The contents of these registers determine what will happen during execution cycles.

During execution cycles, data is manipulated between the B, D, A, Q, and U registers and then written into a predetermined core storage location, or left in the accumulator.

The next instruction, specified by the I register, is addressed by the M register and read from core storage and the program continues.

Some instructions require only one I cycle to perform the complete operation. For example, the load status instruction sets the condition of the carry and overflow indicators according to the information contained in two positions of the B register (Figure 1-13). The second half of the I cycle merely gates positions 14 and 15 of the B register into the carry and overflow indicators and the operation is complete.

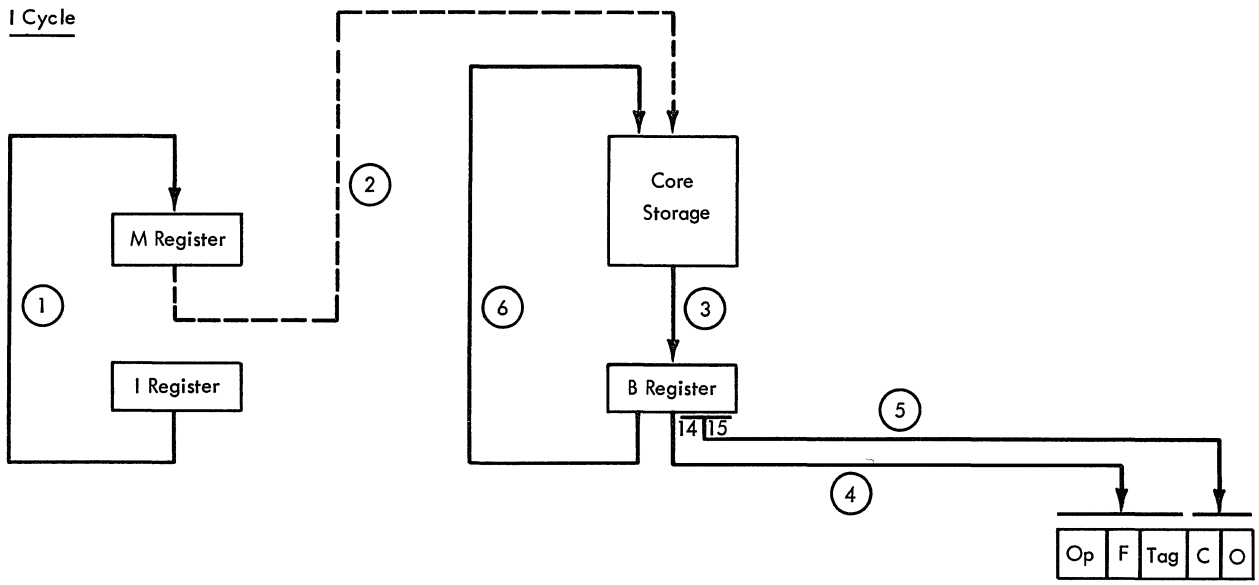
Other instructions require an instruction cycle followed by an execution cycle. For example, the load accumulator instruction generates an effective address during the I cycle and reads a data word from core storage and places that word in the 16-bit accumulator during the E cycle (Figure 1-14).

STANDARD FEATURES

- The following features are basic to the 1801 and 1802 Processor-Controllers.
- Details of these features are in the Functional Unit chapter of this manual.
- A complete list of the system's special features is given in Appendix B.

Parity Checking

- Enables checking for single-bit failures of core storage and I/O circuits.
- Odd parity is maintained in core storage, the B register, and the I/O bus.
- Parity is not maintained throughout the remainder of the processor-controller data flow.
- The parity-bit flip-flop, along with the storage-protect-bit flip-flop, acts as an extension of the B register.



1. Transfer instruction address from I to M.
2. Address core storage from M register.
3. Read instruction word from core storage. Load into B register.
4. Load operation, format, and tag registers.
5. Load carry and overflow indicators with bit 14 and 15 of instruction word.
6. Write-back instruction word into core storage. End operation.

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Figure 1-13. Load-Status Data Flow

- A parity error causes a program stop if the console check stop switch is on, and causes a program interrupt if the check stop switch is off.

- FEMDM page CC30101 shows the parity check circuits.

Each core storage word consists of 18 bits: 16 are data bits which can represent either data or instructions; one bit is used for the storage protect feature; and one bit is used for a parity bit. A parity bit is required in any word that otherwise contains (including the storage protect bit) an even number of bits. Each word that is received from an input device is checked for odd parity. If odd parity does not exist and the core storage position into which the word is to be written does not contain a storage protect bit, the parity-bit flip-flop is turned on. When the word is written into core storage, the parity-bit flip-flop is compared with B-register-parity-required condition and storage protect bit. The parity-bit flip-flop controls an inhibit line, just as the B register positions control inhibit lines, to set the parity bit of that core storage word to a one bit condition.

When a word is read from core storage, the 16 data bits are parity checked to see if a parity bit is required to produce odd parity. If a parity bit is required, and the storage-protect-bit flip-flop is not on, and, the parity bit flip-flop is not on, the parity-error flip-flop is turned on to indicate a parity check.

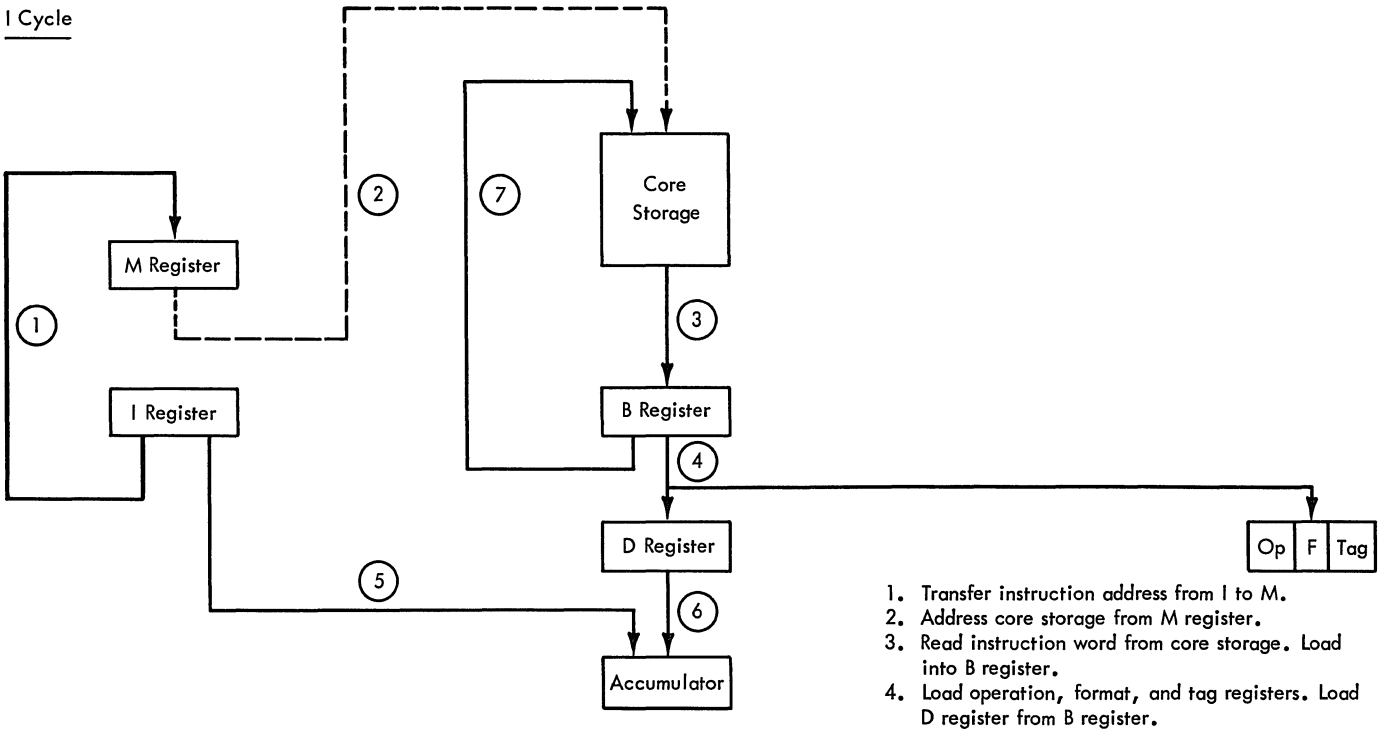
Storage Protect

- Permits the designation of portions of core storage as "read only" and checks for attempts to write into these designated storage locations.

- One storage-protect-bit position is provided with each word in core storage.

- The storage-protect-bit flip-flop, along with the parity-bit flip-flop, acts as an extension of the B register.

The storage-protect-bit flip-flop is controlled by a sense amplifier, from a core-storage-bit plane, just as the 16 data bits and the parity bit are. The storage protect bit is considered when checking or generating parity. The storage protect bit is not carried through the processor-controller data flow, or provided on the input/output buses. Storage protect bits can be set or cleared by a programmed operation in combination with



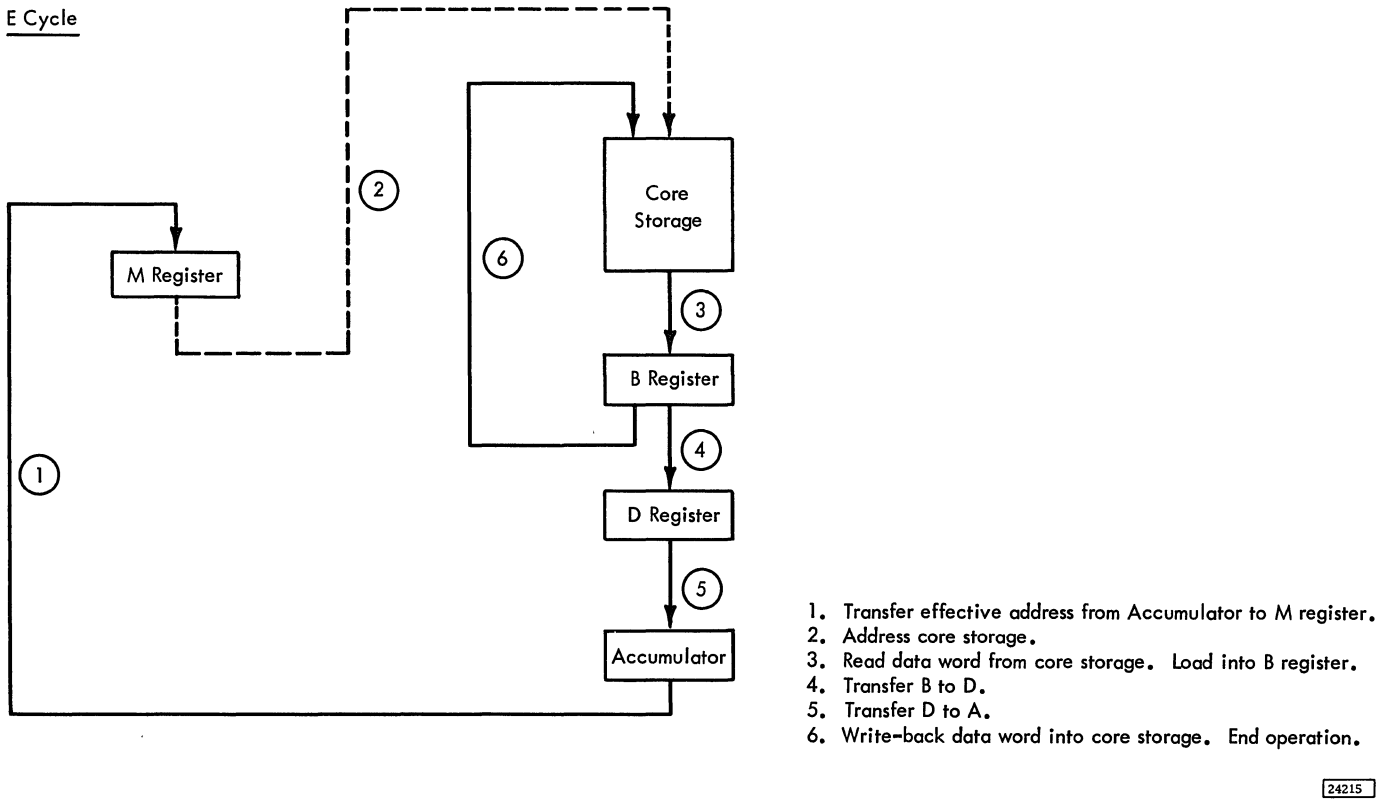


Figure 1-14. Load-Accumulator Data Flow

with a console switch. They can be cleared, but not set, by console switches.

An attempt by the processor-controller to write into a storage protected location of core storage causes a storage protect check which stops the processor-controller if the check stop switch is on. If the check stop switch is off, a storage protect check causes a program interrupt.

Index Registers

- Three 16-bit index registers are provided as a standard feature.
- Indexing an instruction causes the contents of a specified index register to be added to the instruction address to form the desired effective address for that instruction.

Indexing enables the use of one instruction to operate on data stored in various core storage locations without altering the instruction word itself. When specified by the instruction word tag bits, the contents of the specified index register are added to the instruction address during the instruction cycle. Therefore, at the beginning of the execute cycle, the effective address that is in the accumulator has been modified by the index register.

There are instructions that load, store, and modify any of the three index registers.

Indirect Addressing

- Used in two word instructions only (F = 1).
- Causes the address portion of the instruction word (plus the contents of an index register if specified) to specify the core storage location of an address word that is the effective address.

The direct address can be generally defined as the location of data in core storage. An indirect address can then be defined as the address of a direct address. For most instructions, the effective address that is generated during I1 and I2 cycles is a direct address.

However, the presence of a "1" in the bit-8 position of a long format instruction indicates that the effective address is really an indirect address. This indirect address is the core storage location of a direct address.

Only one level of indirect addressing is available in the 1800 system. This means that the indirect address of an instruction always selects a direct address, never another indirect address.

Indirect addressing requires an additional I cycle, called the IA cycle. The IA cycle reads the direct address from the core storage location specified by the indirect address and places the direct address in the accumulator.

Interrupt

- Provides an automatic branch in the normal program sequence, based upon external conditions.
- Interrupt conditions are assigned levels according to the customer's requirements.
- Twelve levels of interrupt are provided for program usage and twelve additional levels are available as special features.
- Three additional levels are provided: CE interrupt, trace interrupt, and the check (error) interrupt.

Some typical interrupt conditions are: the interval timer reaching a preset time interval, an I/O device being ready to transfer data, an illegal operation code, or an external process condition that needs attention.

When an interrupt condition exists, and the bus lines can transfer the request, the assigned interrupt level is activated in a priority circuit. When the present program instruction is completed, the highest priority interrupt level that is active initiates a branch to an interrupt subroutine.

This branch is implemented by a hardware-generated branch-and-store-instruction-register (BSI) instruction. This forced BSI contains a hardware-generated indirect address that specifies a position of a table of direct addresses. The instruction register, containing the location of the next instruction in the main line program, is stored at the core storage location specified by the direct address (EA) and the branch is executed to EA + 1. EA + 1 is the location of the first instruction in the subroutine that services the interrupting device.

At the completion of the sequence of interrupt service subroutines, an indirect-addressed branch is executed with the indirect address being EA. Because EA contains the instruction register contents that were stored during the BSI, the effective address of this branch is the next instruction in the main line program.

Example: Keyboard Operation

As an example, consider a keyboard operation. The processor-controller must have a stored program

including a keyboard-read routine. When the keyboard request key is pressed, an interrupt request is activated on the interrupt level assigned to the keyboard. When the processor-controller can service that level, a forced BSI is executed to a routine that determines the device and reason for the interrupt.

Because this interrupt was activated by the request key, the processor-controller executes an instruction that activates the keyboard and signals the operator to enter a character. After executing this instruction, a branch is executed back to the main line program.

When a character key is operated, another interrupt request is executed. This is a different kind of interrupt. When the processor-controller can service this request, a forced BSI is executed to a routine that again determines the device and reason for the interrupt.

Because this interrupt was caused by the operation of a character key, the processor-controller executes an instruction that transfers the keyboard character to core storage. The character is manipulated according to the interrupt routine and a branch is executed back to the main line program.

If another keyboard character is to be entered, the instruction to activate the keyboard must be executed and the same procedure repeated.

Data Channel

- Provides an Input/Output channel for the higher speed I/O devices on the system.
- These I/O devices transfer data to or from core storage by a method called "cycle stealing."
- Each such device is assigned a cycle-steal level to provide priority. Fifteen levels are available; 3 are standard, 12 are additional features.
- Each cycle steal affects processor-controller operations only by a one-cycle delay.
- Once initiated, data transfers are controlled completely by data channel circuits.

This method of data transfer differs from the direct program controlled operations in that once initiated, no further programmed instructions are necessary for data transfer.

Initializing the data channel sets up a data table address in a register assigned to that level. This register is the channel address register (CAR). Initializing also sets up a word count in the device adapter to control the length of the record to be transferred. (The 1442 is an exception; a complete card is read or punching is terminated by a bit 12 in a punch data word and therefore no word count is required.)

When the device is ready to send or receive data, it requests a cycle-steal cycle on its assigned level. At the end of the present machine cycle, the highest priority level that is active causes the cycle-steal clock to take control from the processor-controller clock for one cycle. Core storage is addressed by the channel address register to address the data table for the transfer of the data word. The channel address register is advanced to contain the address of the next position of the data table for the next data transfer. At the end of this core storage cycle-steal cycle, control is returned to the processor-controller and the main line program continues.

Data channel operations on some devices can be chained, that is, addressing continues from one data table to another, or the same data table addressing is repeated. This eliminates the need of a program instruction to re-initialize the data channel.

Example: Card Punch Operation

As an example of a data channel operation, consider the 1442 punch operation. The card-punch instruction and a table of data words must be in core storage and the 1442 punch must be ready.

The program executes an instruction that specifies the 1442 punch and initializes the data channel to which the 1442 punch is assigned. This operation loads the channel address register with the address of a data table and starts the advance of a card, in the 1442, to the punch station.

The execution of this instruction requires two or three instruction cycles and two execution cycles. The processor-controller then continues its program.

When the card reaches the punch station, a cycle-steal request is activated. When the processor-controller can service the request, a cycle-steal cycle is taken. The channel address register addresses core storage to read a data word from the data table. The data word is transferred to the 1442 and punched. The channel address register is advanced to contain the address of the next data word. After this cycle-steal cycle, the processor-controller program continues.

When the card advances the next column to the punch station, another cycle-steal request is activated and another cycle-steal cycle transfers the next data word to be punched. A bit 12 in a punch output data word terminates punching.

Between cycle-steal cycles (card columns), thousands of program instructions and other cycle-steal operations can be executed.

Interval Timers

- Three interval timers are provided to supply real-time information to the program.
- Each timer has one permanent time base which can be selected from several time base periods.
- The time base periods that are available for Model 1 are: 0.25, 0.5, 1, 2, 4, 8, 16, 32, 64, and 128 milliseconds. The time base periods that are available for Model 2 are: 0.125, 0.25, 0.5, 1, 2, 4, 8, 16, 32, and 64 milliseconds.
- Core storage words 0004, 0005, and 0006 are reserved for Timers A, B, and C.

The timers can be started or stopped under program control. Once started, they are automatically incremented, one count at a time, by the cycle stealing facility of the processor-controller. A count is added each time the assigned time base period is completed. This counting is automatic and does not require a program.

When the 16-bit interval-timer word is incremented to contain all one bits, the next increment (65,536 from a zero count) steps the word to all zeros. When the count reaches zero, an interrupt is requested on the level assigned to the timers.

The program can specify the time interval by placing a count in the interval-timer word in core storage.

Operations Monitor

- A device which causes closure of a contact upon completion of a preset time out period.
- Completion of time out is normally prevented by execution of an instruction in the processor-controller program.
- A separately powered alarm or indicator may be operated by closure of the contact.

This device is used to notify the process operator when the processor-controller is not executing a predicted sequence of instructions. This condition could be caused by power failure, computer hangup, program looping, etc.

Initial Program Load

- Provides a means of automatically loading and executing a group of instructions.
- The 1442 Card Read Punch and the 1054 Paper Tape Reader are both capable of initial program load. Only one of these units in a system can be wired for this feature.
- If the system includes one or two 1442's, the first 1442 is the IPL device.

Because reading data from an input device normally requires program instructions, a means must be available to initially enter the load program that will read the entire program. Making the 1442 or 1054 ready, resetting the P-C, and pressing the Program Load key places the processor-controller in the initial-program-load (IPL) mode. IPL mode enters all the IPL data as instructions beginning at the core storage location specified by the I register (normally reset to 0000) and automatically branches to 0000 to execute the instructions.

Auxiliary Storage

- Provides the ability to operate an I/O device under control of a diagnostic program while the customer's program is running.
- The 4K array contains 256 words designated as auxiliary storage.
- Each 8K array contains 512 words of auxiliary storage.
- The auxiliary storage portion of the first array is reserved for CE use.
- The Multiprogramming Excutive (MPX) Operating System logs certain I/O errors in a portion of auxiliary storage not reserved for CE use.

CE exerciser programs, designed to operate in auxiliary storage, are provided as a maintenance feature. These diagnostics can be loaded into and run from auxiliary storage concurrently with the customer's program in main storage.

Programs are loaded into auxiliary storage by an initial program load operation and the interrupt to Auxiliary/Main Storage switch, on the I/O monitor interface panel, in the Auxiliary position. Auxiliary storage is accessed, for program operation, by means of the CE interrupt when the switch is in the Auxiliary position.

I/O devices capable of operating in CE mode can be placed in this mode by a program instruction. When in CE mode, a device interrupts on the CE

interrupt level. With the Interrupt to Auxiliary/ Main Storage switch in the Auxiliary position, a CE level interrupt causes a branch to a subroutine in auxiliary storage. The last instruction in the auxiliary storage interrupt routine branches back to the next instruction in main storage.

If a system interrupt occurs during an auxiliary routine, control is returned to the main program.

When a data channel operation is initiated in auxiliary storage, any subsequent cycle-steal operation on that level (data channel) accesses auxiliary storage.

The program instructions which address the auxiliary storage from the main program are included in the Load and Store Operations and Arithmetic Instructions in Chapter 3.

The Multiprogramming Executive (MPX) Operating System provides the following error information:

1. Error logs for CA, 2790 Adapters, and Selector Channel.
2. Error Statistics table for each CA line adapter.
3. A CA trace buffer.

For error logging tables, refer to MPX programming documentation.

I/O Monitor Unit

- A portable service aid that provides:
  - On-line monitoring.
  - Console type displays.
  - Data and signal comparing.
  - Scope sync generation.
  - Manual device controls.
- Registers, latches, and control signals of the I/O adapters and channel control are pluggable to the I/O Monitor.

The I/O Monitor can be used to display static conditions or to monitor operations of a desired system component. A valuable feature is its ability to trap intermittent failure. This is accomplished by latching displays and controls that permit the displays to be selectively set and reset.

The I/O Monitor connects to the I/O Monitor interface panel on the 1801, 1802, 1826, or 1810 (Figure 1-15). A set of signal connectors are provided for each I/O feature that has an I/O Monitor interface. The I/O Monitor cables attach to the desired set of signal connectors and to a power connector. Plastic overlays on the front panel of the I/O Monitor label the indicators and switches for the I/O device being monitored.

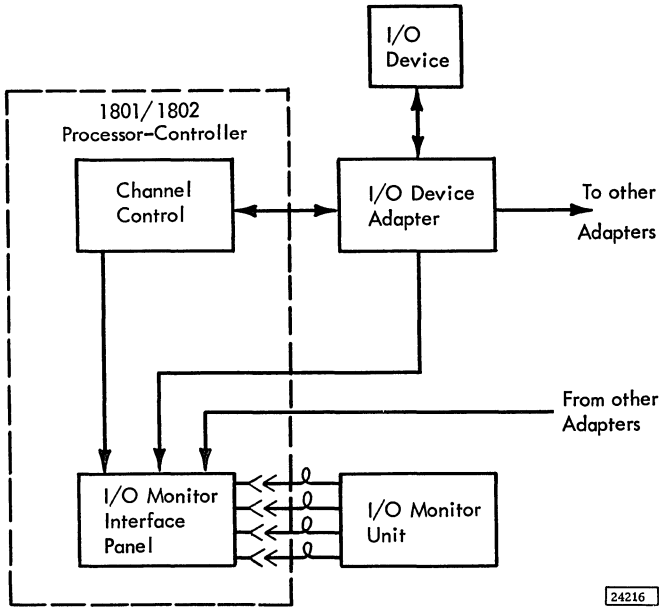


Figure 1-15. I/O Monitor Unit Attachment, 1801/1802

DATA PROCESSING I/O UNIT ATTACHMENT FEATURES

- Adapters and controls are available for attaching a wide variety of data processing I/O units.

Data processing I/O units function with an external document such as a punched card or a reel of magnetic tape. To provide the logical and buffering capabilities necessary for operation on 1800 systems, a control (adapter) feature is available for each I/O unit.

The following I/O units can be attached to the 1800 system via the data processing I/O adapters:

1816 Printer Keyboard (Modified IBM SELECTRIC®).
1053 Printer.
1054 Paper Tape Reader.
1055 Paper Tape Punch.
1442 Card Read Punch.
1443 Printer.
1627 Plotter.
1810 Disk Storage.
2401/2402 Magnetic Tape Unit.

The 1816/1053 adapter is a basic feature that accommodates four 1053's or one 1816 and three 1053's.

PROCESS INPUT/OUTPUT FEATURES

- Modular features are available to match the 1800 system with the process requirements.
- Analog Input feature converts bipolar voltage or current signals to digital values for use by the computer.
- Digital Input feature accepts binary information represented by contact closures or voltage levels.
- Analog Output feature converts digital values to precise voltage levels for operating process devices.
- Digital Output feature provides binary data to the process in the form of "contact" closures or voltage levels.

Analog input features include analog-to-digital converters, multiplexers, amplifiers and signal conditioning equipment to handle various types of process analog input signals. System conversion rates to 24,000 samples per second are provided, with program selectable resolution and external synchronization. Analog input capacity is 256 solid-state (high-speed) multiplexer points or 1,024 relay multiplexer points plus 192 solid-state multiplexer points. A second analog-to-digital converter can be added to double system analog input performance and capacity.

The digital input features provide up to 384 process interrupt points, and up to 1,024 bits of contact sense, digital input, high-speed register input, or binary pulse counter positions.

Analog output features provide up to 128 analog output points for individual or simultaneous operation of a wide range of customer devices.

The digital output features provide up to 2,048 bits of pulse output, electronic "contact" operate, and high-speed register output.

PROGRAMMING SYSTEMS SUMMARY

The IBM 1800 Data Acquisition and Control System Card/Paper Tape and TSX Programming Systems are described briefly in the following paragraphs.

IBM 1800 Card/Paper Tape Programming System

The IBM 1800 Card/Paper Tape System is made up of four sets of programs that support all announced features of the IBM 1800 Data Acquisition and Control System. These programs and their descriptions are as follows:

ASSEMBLER: The 1800 Assembler permits the programmer to write (code) source programs in a symbolic language that is more meaningful and easier to handle than the binary machine language. The assembler language includes macro capability for communication with subroutines.

FORTRAN: The 1800 FORTRAN compiler allows the user to state his problem in a mathematically oriented language. The compiler produces, as output, a machine language program. It provides scientists and engineers with a method of communication that is more familiar to them and is much easier to use than the actual machine language.

UTILITY: The 1800 card/paper tape utility routines perform various input/output functions required for programming system operations. Also included are routines which aid the user in debugging his programs.

SUBROUTINE LIBRARY: The 1800 subroutine library provides the user with arithmetic and functional, I/O, conversion, and miscellaneous subroutines. These subroutines allow the user to perform real number and integer operations, move data in or out of the system, convert data from one code to another, and trace or dump data on output devices.

IBM 1800 Time-Sharing Executive System

The IBM 1800 Time-Sharing Executive System is a real-time, process-control programming system that affords the user an easy means of generating, testing, and executing a complete process control program. The user's process programs are built in the non-process monitor mode, tested by the TSX simulator, and executed in the on-line, process-control mode.

With the TSX system, the user can:

1. Write nonprocess or process-control programs in FORTRAN or 1800 assembler language.
2. Execute nonprocess and process-control programs concurrently.
3. Call IBM supplied executive programs which aid in the control of the various process functions.
4. Simulate process interrupts and analog input/output to enable testing of process programs without using the actual physical process.

IBM 1800 Multiprogramming Executive System (MPX)

The 1800 Multiprogramming Executive System is a real-time multiprogramming operating system capable of increasing the efficiency and throughput

of the IBM 1800 Data Acquisition and Control System computer.

To increase throughput, MPX enables programs, core storage space, input-output facilities and control of the processor-controller to be allocated and concurrently shared among several process functions. These facilities permit multiprogramming, that is, they permit several process functions to be performed concurrently and to share the basic resources of the computing system.

The system also provides for queuing of I/O operations and allows the user to achieve maximum overlap of I/O and computing. On the lowest level of operation, a batch processing monitor is provided. With the batch processing monitor, assemblies, FORTRAN compilations, and user programs can be executed in a stacked job mode.

With the MPX system, the advantages are:

1. High throughput.
2. Fast response.
3. Efficient use of processor-controller time.
4. Ease in time-scheduling program execution.
5. Ability to modify in-core user written routines on-line.
6. Ability to modify IBM processors on-line.
7. Ability for the IBM Customer Engineer to run on-line diagnostics for the 1442, 1443, 1810, 1053, Communications Adapter, Selector channel, and analog input (Direct Program Control).
8. Time-sharing of foreground and background (batch processing monitor) operations.

Chapter 2. Functional Units

CENTRAL PROCESSING UNIT

Multi-Input Trigger

This circuit is used in clock, counter, and register circuits and as a standard flip-flop. Much of the 1800 system logic design utilizes the characteristics of this flip-flop and its associated input circuits. A circuit description of the flip-flop is in the Appendix.

INPUT GATING CHARACTERISTICS: The gate level of this flip-flop must be present at least 170 nanoseconds (4 μsec system) before the shift pulse. The gate input remains at an operating level for about 90 nanoseconds after the fall of the signal.

Some flip-flop inputs are conditioned by gate and shift signals that occur simultaneously. For example, the data-cycle flip-flop turn-on is conditioned by E1 cycle (gate) and T0 (shift)(Figure 2-1). The flip-flop does not turn on during the E1 cycle because the gate is not present before the shift. The gate actually falls at the same time the next shift pulse arrives; however, due to the capacitive delay in the gate circuit, the flip-flop is turned on by this T0 shift pulse.

Clock and Timing

- The basic pulse generator for the 1801 Model 1 or 1802 Model 1 (4-μsec cycle) is a 2-megacycle free-running oscillator.

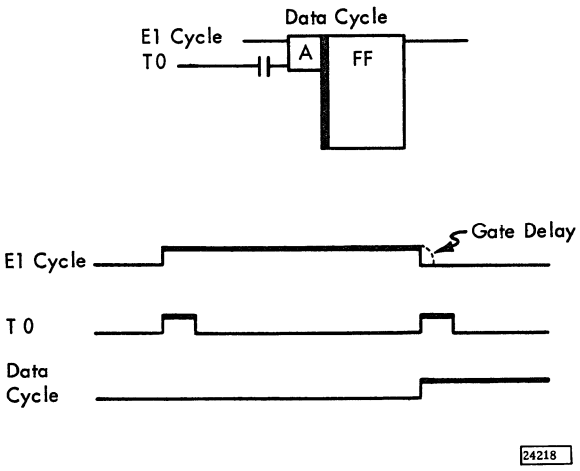


Figure 2-1. Input Gating Characteristics

- The basic pulse generator for the 1801 Model 2 or 1802 Model 2 (2-μsec cycle) is a 4-megacycle free-running oscillator.
- When an 1803 unit is included in the system, a 2.25-μsec cycle is developed by doubling the duration of T1 for each machine cycle.
- Clock advance circuits and the clock ring are shown in Figure 2-2.
- The phase flip-flop is turned on and off by the oscillator to time the clock advance circuits and to provide sub-clock-step pulses (A phase and B phase) for the system.
- The advance flip-flop is turned on by the first B-phase pulse after the Start key is operated.
- The delay flip-flop is turned on by the advance flip-flop and the next B-phase or by an initial-program-load request.
- The run flip-flop is turned on by the delay flip-flop or by an interrupt.
- Clock-advance pulses occur at every A-phase time after the run flip-flop is turned on.
- The clock ring consists of eight triggers, T0 through T7.
- A basic machine cycle is one complete cycle of the clock ring.
- A cycle is extended for various operations by holding on the T7 flip-flop.

The P-C clock is reset or "latched" with the T7 flip-flop on. When certain arithmetic and shift operations require more steps than one cycle provides, the clock is stepped to T7 and then clock advances are prevented, holding on T7 while the phase flip-flop output provides timing pulses for the operation. Advancement from T7 requires the run flip-flop being on and the absence of any of the clock-extending conditions. Once T7 is turned off, the

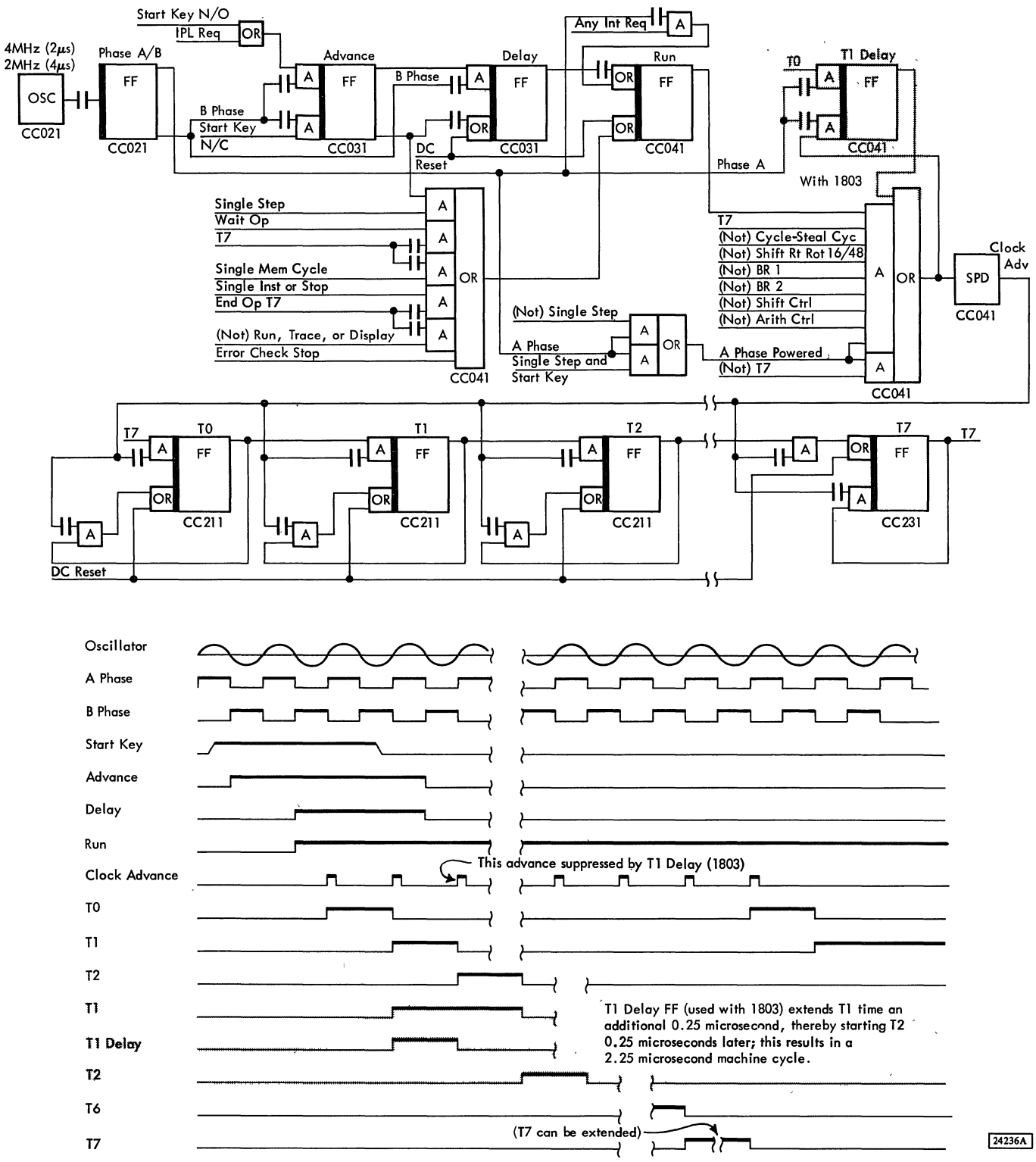


Figure 2-2. P-C Clock and Clock Advance

clock advances unless the P-C is in the Single-Step mode.

The clock is stopped at T7 after one cycle (basic or extended) if the P-C is in the Single-Cycle mode or performing a Wait operation. The clock is stopped at the last T7 of an operation (End Op T7) if the P-C is in the Single-Instruction mode or if the Stop key is operated.

Single-Step mode prevents clock advances by blocking the A-phase pulse except when the Start key is operated.

Cycle Timer

- Composed of six flip-flops: I1, I2, IA, E, E1, and E3.
- Specifies the type of cycle being performed.
- Gates the necessary circuits for that type of cycle.
- Functions of the various cycles are described in the I and E Cycles section of Chapter 3.
- Figure 2-3 is a flow chart of I and E cycles.
- Figure 2-4 shows the development of E cycles.

I1

- This flip-flop is dc reset on to begin the first operation with I1 cycle.
- Turned on after the last cycle of every operation (end-op, T0).
- Turned off at the next T0 if not end-op.

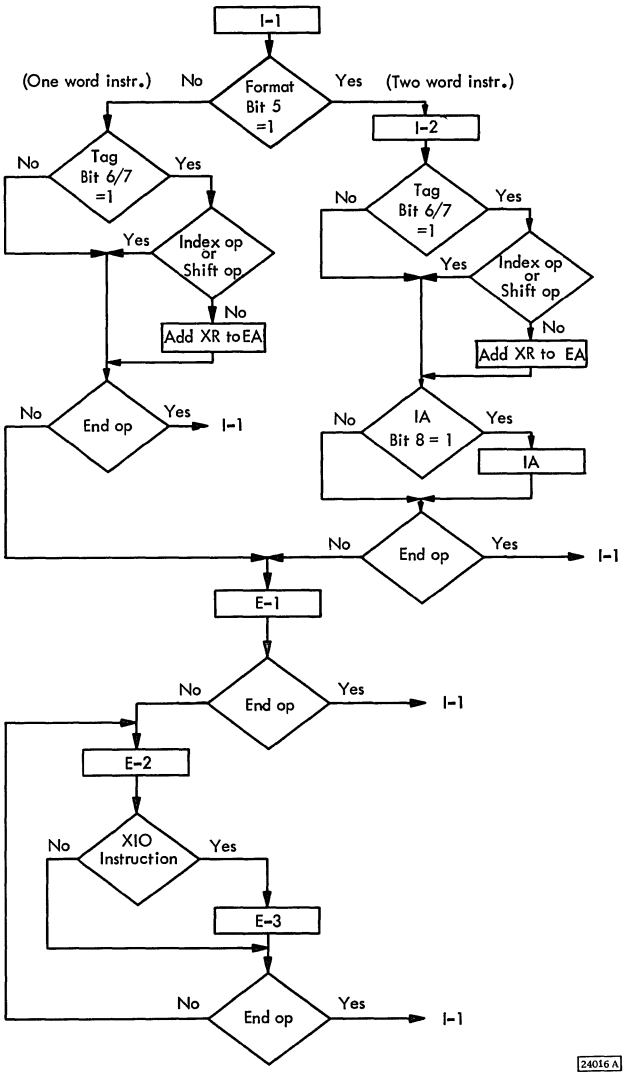


Figure 2-3. I and E Cycles

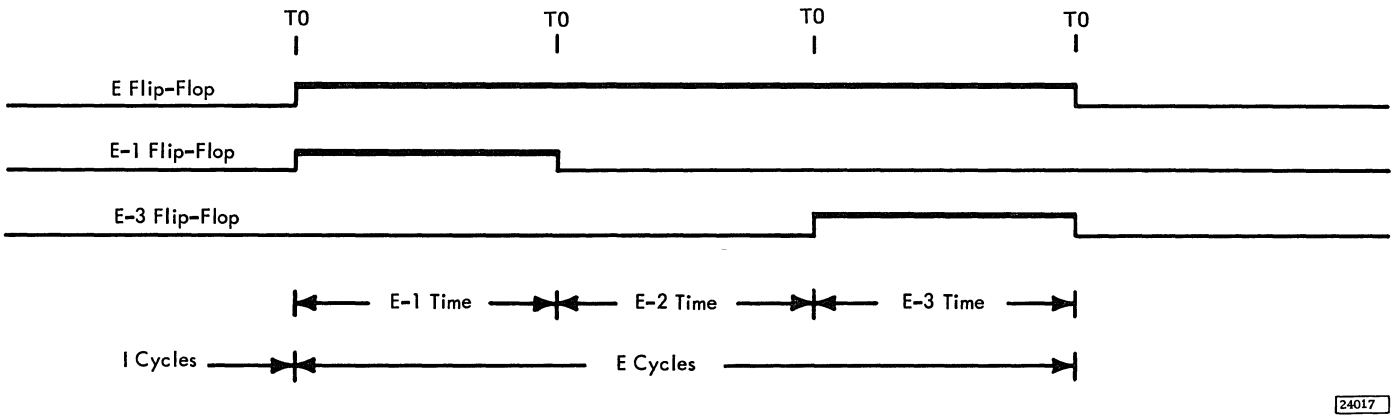


Figure 2-4. Development of E Cycles (CC331)

I2

- This flip-flop is turned on at T0 following I1 if the format bit (bit 5 of instruction word, read on I1) is a one.
- Turned off at next T0.

IA

- This flip-flop is turned on at T0 of a two-word instruction (bit 5 = 1) if the IA bit (bit 8) is a one.
- Turned off at next T0.

E

- This flip-flop is turned on at T0 following any I cycle if the following do not exist: end-op or conditions to turn on I2 or IA.
- Turned off at T0 with end-op. Remains on for E1, E2, and E3 times.

E1

- This flip-flop is turned on with E flip-flop.
- Turned off with next T0. The off condition is ANDed with the E flip-flop output to provide E2 time.

E3

- This flip-flop is turned on at T0 with an XIO read/write instruction and E2 time.
- Turned off at the next T0.

Registers

- The following characteristics apply to all the processor-controller registers.

The output is independent of the triggering action. It can be set and sampled at the same time. The gate must be present 170 nanoseconds before the set pulse.

Registers are used at different cycle times and for different purposes during the various instructions. The times and conditions are explained for each instruction in Chapter 3 of this manual.

Data flow through the processor-controller registers is shown in CC10101.

Storage Buffer Register (B)

- B register consists of 16 flip-flops.
- Data and instruction words read out of core storage are set into the B register.
- DC reset, also reset at every T0 or X0 time.
- B register contents determine data to be written into core storage.
- Odd parity in respect to the contents of the B register is generated or checked during each core storage cycle.
- Inputs to the B register are from:
  - Sense Amplifiers (from core storage)
  - I-register
  - Accumulator
  - In-Bus (via channel data bus)
  - Data Entry switches (via channel data bus)
- Outputs from the B register go to:
  - Inhibit circuits (to core storage)
  - D register
  - Out-Bus (via channel data bus)
  - I-register
  - Op register (B_0 - B_4)
  - Format Register (B_5)
  - TAG register (B_6, B_7)
  - Mod. register (B_8, B_9)
  - Shift Control Register (B_{10} - B_{15})
- o Contents are continually displayed on the console.

Arithmetic Factor Register (D)

- D register consists of 16 flip-flops.
- Stores one factor for arithmetic and logic operations; the other factor is in the accumulator.
- The D register and the accumulator have unique interconnections that implement arithmetic and logical operations.
- The other input to the D register is from the B register.

- Positions 0 through 7 are set to ones when a negative displacement is loaded into positions 8 through 15.

- Load D_{14}, D_{15} to carry/overflow indicators at T4 in load status operation.

- Contents are continually displayed on the console.

Accumulator (A)

- Stores one factor of an arithmetic operation; the D register contains the other factor.

- Contains the result of any arithmetic operation.

- Contents can be shifted right or left.

- Contents are continually displayed on the console.

The accumulator is a 16-position register with unique connections that enable arithmetic and shift operations.

It can be loaded from core storage by a Load Accumulator instruction. This operation is executed to set up one factor of an arithmetic operation or to set up a data word to be shifted.

An XIO instruction with a sense command can load the accumulator with a sense word from an I/O adapter. The program can then analyze the sense word by a shift operation.

The accumulator contents can be stored in core storage by a Store Accumulator instruction. Its contents can also be stored in the temporary accumulator (U register) to allow the subsequent use of the accumulator. For example, before the effective address is generated (requires the accumulator for an add operation) the contents of the accumulator which might be data to be used in the operation, are transferred to the U register. At the beginning of the E1 cycle, the original contents are transferred back to the accumulator.

The accumulator's only input from the D register is conditioned by the add-sub-OR-EOR gate. Therefore, any operation that requires a D to A transfer, even though it is not an arithmetic operation, must activate this line.

The gating of the input and output of the accumulator are conditioned by the various operations as shown in the description of the operations in Chapter 3. A summary of the inputs and outputs follows:

Inputs:

A_0-A_{15}
- D register
- I register
- Q register
- U register
- Index registers 1, 2, and 3

A_0
- Q_{15} (rotate right operation)
- Multiply sign entry

A_{10}-A_{15}
- Shift Counter

A_{15}
- Overflow indicator
- Double precision carry
- Q0 (shift left operation)

Outputs:

A_0-A_{15}
- Q register
- U register
- B register
- M register
- Index register 1, 2, and 3

A_{15}
- Q_0 (shift right operation)

Adder

- There is no discrete functional unit called the adder.

- The "adder" is composed of the D register, the accumulator, and their unique interconnection and control.

- The circuit connections and timing diagram for the add and subtract operations are shown on CC50101.

An add or subtract operation must be preceded by an operation that loads the accumulator with one factor. The add or subtract operation brings the other factor from core storage and places it in the D register.

The D factor is added to the A factor in parallel. Figure 2-5 shows an example of an add operation. If D_n is a one, the state of A_n (same bit position as D_n) is changed. If A_n changes from a one to a zero,

	0 0 1 0 1 1 0 1	D
Start	0 0 0 1 0 1 1 1	A
Carries	0 0 0 0 1 0 1 0	D'
Partial Sum	0 0 1 1 1 0 1 0	A'
	0 0 0 1 0 1 0 0	D"
	0 0 1 1 0 0 0 0	A"
	0 0 1 0 0 0 0 0	D^{III}
	0 0 1 0 0 1 0 0	A^{III}
	0 1 0 0 0 0 0 0	D^{IV}
	0 0 0 0 0 1 0 0	A^{IV}
	0 0 0 0 0 0 0 0	D^{V}
Result	0 1 0 0 0 1 0 0	A^{V}

Sum Rule: Each 1 in D changes value of corresponding bit in A.

Carry Rule: A change from 1 to 0 in A sets next higher-order position in D to 1.

24031 A

Figure 2-5. Add Operation Example

the next higher order of D (that is, D_{n+1}) is set to a one. If not, D_{n+1} is set to a zero. The pulse that causes this action, reset-D-register, occurs at phase-A time of clock steps T4 through T7.

The add is complete when the D register contains all zeros. The D register is checked for all zeros at phase-B time of the same clock steps that cause the adding, T4 through T7.

If the operation requires more than four add cycles (T4 – T7), T7 is extended until the add is complete. (The A and B phase pulses continue.)

Negative numbers are handled in two's complement form.

Subtraction is accomplished by activating the subtract-gate-A-register line (CC50101). In A_n changes from a zero to a one, the next higher order of D (D_{n+1}) is set to a one. If not, D_{n+1} is set to a zero.

Temporary Accumulator Register (U)

- Temporary storage for the contents of the accumulator; 16 positions.
- Input and output is from the corresponding positions of the accumulator.
- Contents cannot be displayed on the console.
- Used for storage only; not capable of other accumulator functions.
- Saves the contents of the accumulator during effective address generation of an instruction cycle.
- Saves the contents of the accumulator during E cycles of a compare instruction.

Accumulator Extension Register (Q)

- An extension of the low-order end of the accumulator; 16 positions.
- Inputs are from the corresponding positions of A and the two adjacent positions of Q; the Q_0 position has an input from A_{15}.
- Outputs are to the corresponding positions of A and, for shift operations, the two adjacent positions of Q.
- Contents can be displayed only at the end of a cycle, under control of the Display-Data-Register switch.
- Stores the 16 least significant bits of a multiplication product.
- Stores the remainder of a divide operation.

Instruction Address Register (I)

- Sixteen-position register, connected as a counter to maintain the address of the next instruction.
- Contents are transferred to the M register at T0 time of I1 and I2.
- Contents are then increased by one for the next sequential address.
- Contents are transferred to the accumulator for effective address generation during each one-word instruction cycle.
- Contents are continually displayed on the console.

I REGISTER INCREMENTING: The 16 flip-flops of the I register are connected as a binary counter (Figure 2-6). All the flip-flops are gated by the increment-gate line except during the operations in which incrementing is not needed. The pulse that turns on or off I-15 is active every end-op-T0 time (I to M pulse). I-15 going off turns on or off I-14; I-14 going off turns on or off I-13.

This binary-counter method is used for all the flip-flops except positions I-11, I-7, and I-3 which are turned on or off by all the previous (lower order) positions being on and then going off.

Storage Address Register (M)

- M register consists of 16 flip-flops.
- Positions 0, 1, and 2 of the M register select one of eight core storage units.
- Positions 3 through 15 of M register select the word within the addressed 8k core storage array.
- Loaded from the I-register or the accumulator.
- Output is inhibited for some operations.
- During data channel operations, output is replaced by the Channel Address Register output.
- Position 15 output is forced on during double precision instructions.
- Contents can be displayed, at the end of a cycle, under control of the Display-Address-Register switch.

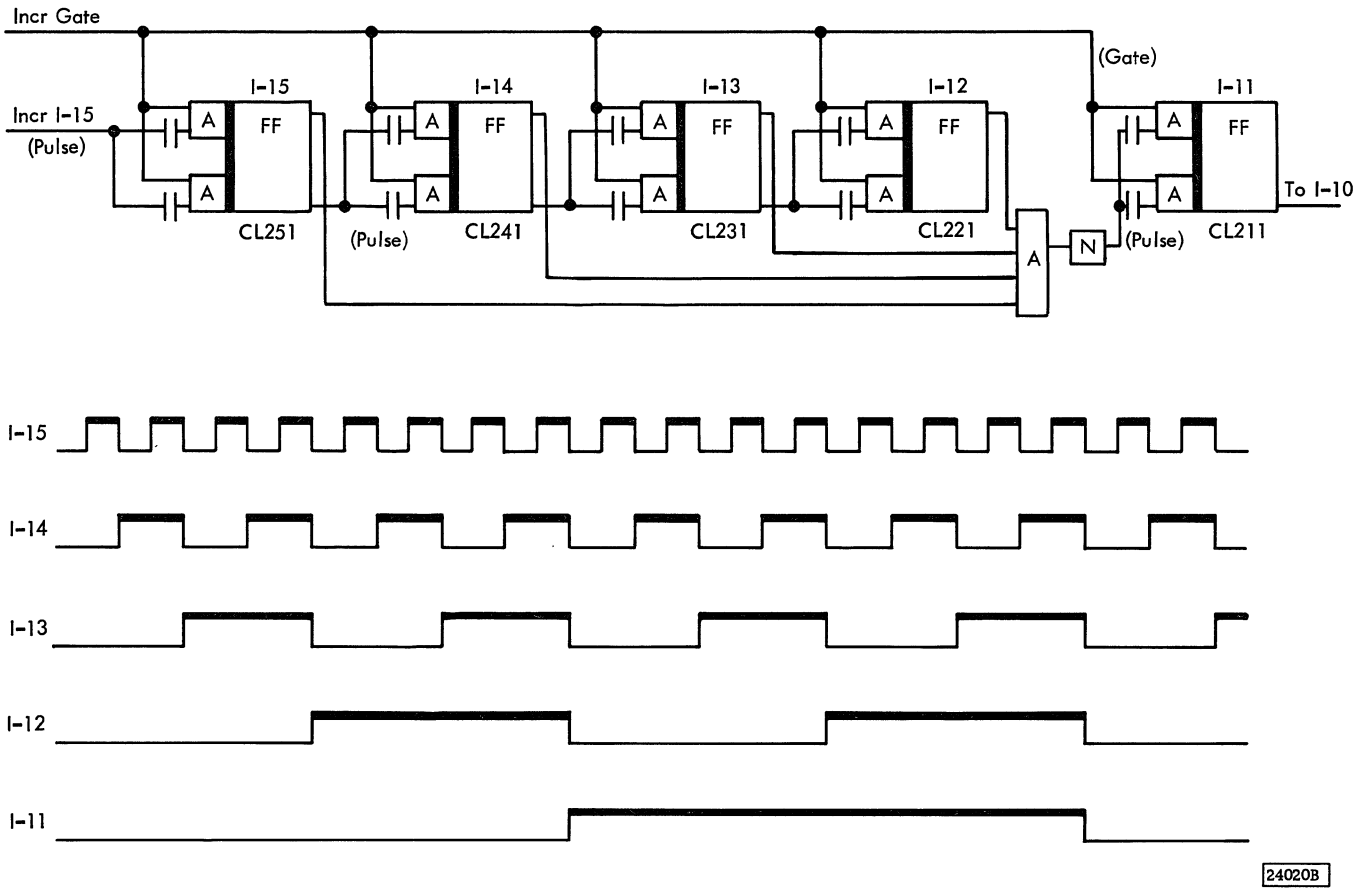


Figure 2-6. I Register Incrementing

Shift Counter (SC)

- Six position binary counter.
- Loaded at the beginning (I1, T5) of every operation to control the number of cycles to be taken.
- Loaded at the beginning of a shift instruction to control the number of positions to be shifted.
- Decremented at T1 of each execute cycle (Figure 2-7).
- Shift count = 0 causes the operation to end.
- Contents can be displayed, at the end of a cycle, by use of the Display Data Register switch.

The shift counter consists of six flip-flops; SC-1, SC-2, SC-4, SC-8, SC-16, and SC-32. It can be set to a count of 1, 16, or 18 by circuitry; or it can be loaded from the B-register or any index register. The output is tested for a count-equal-zero condition. Figure 2-7 shows the shift counter set to a count of 18 and decremented to zero.

Index Registers (XR)

- Three hardware index registers are standard features.
- Used for address modification.
- XR's are selected by the instruction word TAG bits (bits 6 and 7) as follows:

Bits 6 and 7	XR
01	1
10	2
11	3

- Contents can be changed by LDX, MDX, or SLC instructions only.
- All XR outputs can be gated to the accumulator.
- XR bits 10-15 can be gated to the shift counter for shift operations.

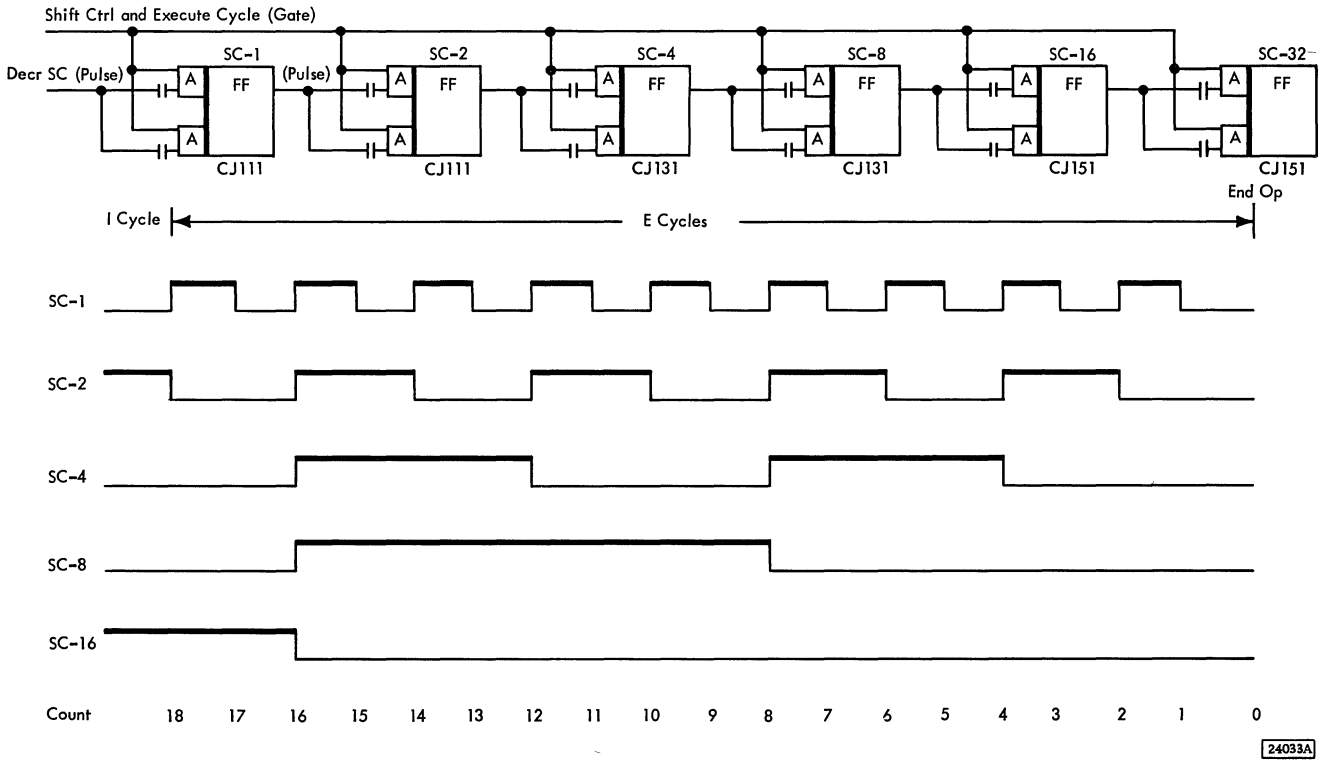


Figure 2-7. Shift Counter Decrementing from 18

- The XR specified by the TAG bits is reset at the beginning of an SLC operation.
- XR's are not reset by DC reset.
- Contents can be displayed, at the end of a cycle, under control of the Display-Data-Register switch.

Three index registers, consisting of 16 flip-flops each, are included in the 1801 and 1802 Processor-Controllers. The set gates for the XR's are conditioned by the TAG bits of the instruction word (bits 6 and 7) and are activated by LDX, MDX, or SLC instructions at E-cycle-entry time. The following XR positions are gated to the shift counter:

XR 1, 2 or 3 Position	Shift Counter Position
15	1
14	2
13	4
12	8
11	16
10	32

CORE STORAGE

- The core storage unit, 4K or 8K, is self-contained on a single SLT board.
- There are two core storage units available: 4μsec and 2μsec.
- SD011 is a block diagram of the 4μsec core storage.
- SA011 is a block diagram of the 2μsec core storage.
- When an 1803 adapter is installed, the system operates with a cycle time of 2.25 μsec.

Magnetic Core Theory

A magnetic core is a small doughnut-shaped ring that is uniformly constructed of ferrite particles bonded together by a ceramic material. The ferrite particles have good magnetic properties and the core has a high retentivity of the magnetic flux lines after the magnetizing force is removed. It is this property of retentivity that makes a magnetic core useful as a storage device.

The operation of a magnetic core can best be described by reference to its hysteresis curve, Figure 2-8. This curve is a plot of the relationship between a magnetizing current and the flux density of the core.

A magnetic core is capable of maintaining indefinitely one of two stable magnetic states, either at point A or at point D on the hysteresis curve. Because the core has two stable states, it can be used as a binary storage device. At point A the core has a residual flux in a negative direction, and at point D a residual flux in the positive direction. These two directions can be arbitrarily assigned as binary "zero" and binary "one," respectively. I_m is the amount of current necessary to change the state of the core. Plus I_m is the amount of current required to "flip" the core from binary zero to binary one. Minus I_m is the same amount of current in the opposite direction required to flip the core from binary one to binary zero.

On the hysteresis curve, it can be observed that a magnetizing current of plus I_m will change the magnetism of the core from point A, a binary zero, to a value in the positive direction at point C. When the current is removed, the total amount of magnetization drops back to point D (binary one). If, instead of the full magnetizing current I_m, a current of $I_m/2$ were applied, the flux would change only the small amount from point A to point B on the curve, and when the current returned to zero, the flux would return to its original value.

A reverse current, minus I_m, develops flux of opposite polarity and, if the core is in the "one" state, changes the magnetic state of the core from point D to point F. When the driving current is removed, the magnetization drops back to point A (binary zero).

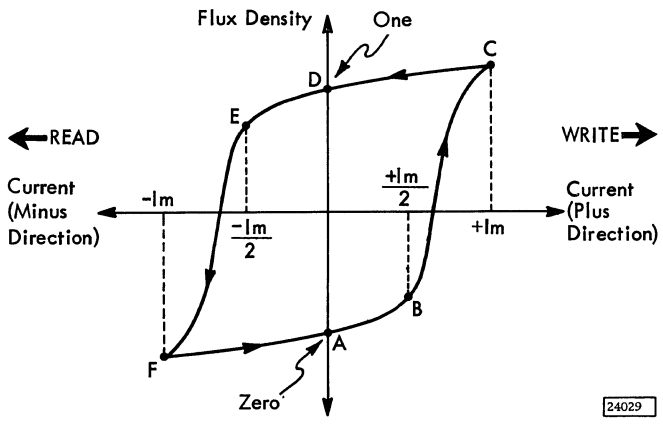


Figure 2-8. Hysteresis Curve of Magnetic Core

Writing Into Core

The magnetic properties of the core make it ideally suited for use in a storage matrix employing X and Y drive lines. Each core of the matrix is threaded by three windings (Figure 2-9). One winding is an X drive line that carries a current $I_m/2$ and one winding is a Y drive line that carries a current $I_m/2$ in the same direction. A coincidence of current in these two windings occurs at one core storage position (18 cores) thereby "selecting" that word.

The third winding is the inhibit/sense winding. When writing into a core storage position, each core that is not to receive a "one" bit is inhibited by a current $I_m/2$ flowing in its inhibit/sense winding in a direction opposite that flowing in the X and Y drive lines. The magnetic field produced by the inhibit/sense winding effectively cancels half the field produced by the X and Y drive lines. The resulting magnetic field is insufficient to flip the core to the "one" state.

Reading Out of Core

When information is to be read out of a core storage position, the currents $I_m/2$ in the X and Y windings are reversed (Figure 2-9). Each core that flips from a "one" to a "zero" state induces a pulse into its inhibit/sense winding. The inhibit/sense winding at each core does not carry inhibit current and is used instead to detect the change in state of the magnetic flux. The sensed bits are set into the corresponding positions of the B register.

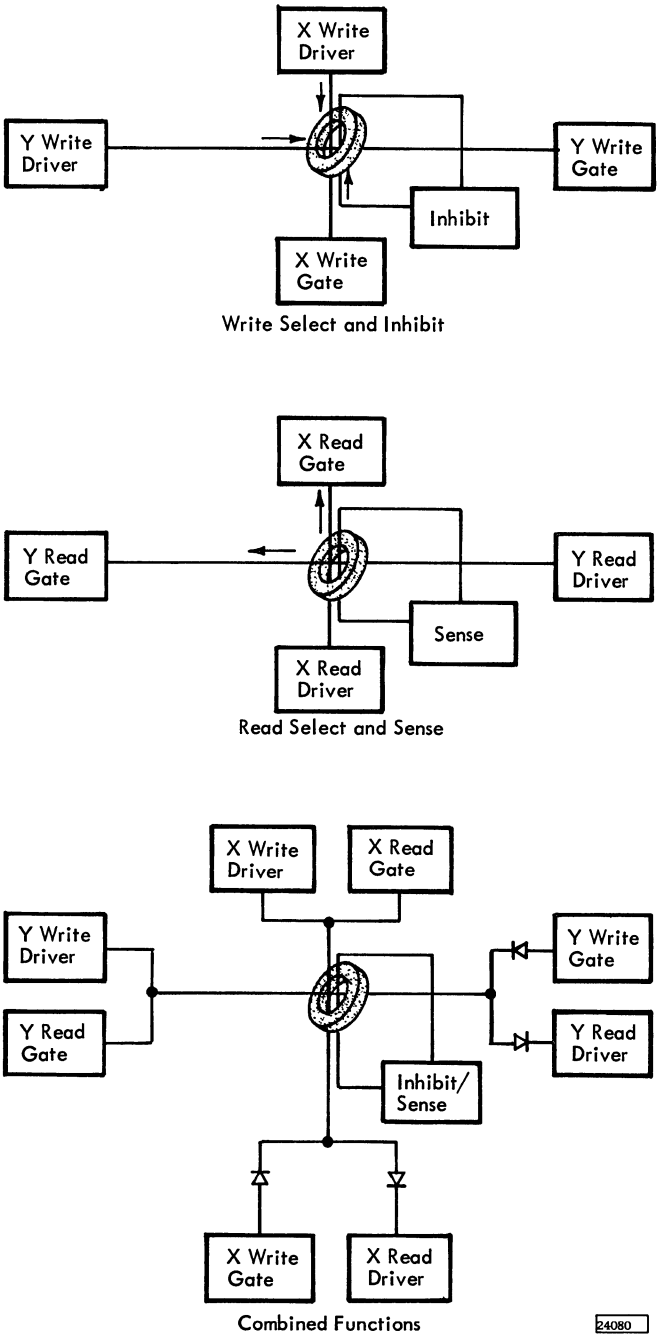


Figure 2-9. Core Storage Write and Read (4-usec Storage)

Addressing

- One X drive line and one Y drive line are activated by selecting both ends of the lines.
- Each active drive line carries half-select current.
- The two drive lines intersect at one core in each bit plane (18 cores) to provide full select current at that one word.

8K Addressing

The magnetic cores are arranged in matrices of 128 x 64 cores, called planes. (Each plane is actually 128 x 68, providing 512 positions of auxiliary storage that are not program addressable and are described in another section.) The 8K array consists of 18 of these planes with each plane assigned to one bit position of a core storage word. Corresponding core positions in each plane are addressed simultaneously by the X and Y drive lines to select one 18-bit word. Since there are 8192 cores in each plane, the 8K array has a capacity of 8192 words.

The 128 x 64 matrix in SD041 represents one plane of the 4-μsec core storage, 8K array. 8K addressing for the 2-μsec core storage is shown in SA041. It differs from the 4-μsec core storage only in the drive circuits which are described in another section. The one core that is shown is selected by the address in the 13 positions of the address register (M register).

At side A, the 64 X drive lines, which run through all planes, are divided into eight groups of eight lines each. One group is activated by a decode of M register positions 3, 4, and 5. At the other end of the X lines, actually the other end of the array, one line in each group of eight is activated by a decode of M register positions 6, 7, and 8. Thus, a single X line is activated and carries half-select current.

At side B, the 128 Y lines which run through all planes, are divided into eight groups of 16 lines each. One group of 16 lines is activated by a decode of M register positions 9, 10, and 11. At side D, actually the other end of the array, one line in each group of 16 is activated by a decode of M register positions 12, 13, 14 and 15. A single Y line is thereby activated and carries half-select current.

In each plane, the core at the intersection of the active X and Y drive lines receives full-current and is the only core in the plane that is selected.

4K Addressing

One plane of the 4-μsec core storage 4K array is shown in SD042. 4K addressing for the 2-μsec core storage is shown in SA042. The 4K and 8K arrays occupy the same area of the SLT board. The core planes used in the 4K array are identical to those used in the 8K array but only nine planes are used. For addressing purposes, each 128 x 64 plane is divided into two 128 x 32 half-planes. Each of the 18 half-planes is assigned to one bit position of the core storage word. Since there are 4,096 cores in each half-plane, the 4K array has a capacity of 4,096 words. (An auxiliary storage of 256 words is actually part of the 4K array; it is described in another section.) The 32 X drive lines are divided into four groups of eight lines each (one-half as many groups as in the 8K array). The X lines run through the nine B half-planes, then loop back through the nine D half-planes. One group is activated by a decode of M register positions 4 and 5 (position 3 is not used with 4K core storage). At the other end of the X lines, one line in each group is activated by a decode of M register positions 6, 7, and 8. A single X line is thereby activated and carries half-select current. The 128 Y drive lines are divided into eight groups of 16 lines each, as in the 8K array, and run through all nine planes. One group of 16 lines is activated by a decode of M register positions 9, 10, and 11. At the other end of the array, one line in each group of 16 is activated by a decode of M register positions 12, 13, 14, and 15. This active Y line intersects the active X line at two cores in each plane; therefore, nine planes provide 18 bits for each of 4096 words.

Module Selection

- One module (one SLT board) of core storage can contain a 4096- or 8192-core array.
- Address register bit 0, bit 1, and bit 2 lines select the module.
- Module selection lines are connected through wired-logic (WZ20100).

The circuits that activate the core storage clock and timing circuit, and therefore select the unit, require a specific combination of address-register-bit, -1 and -2 lines. These lines connect from the M-register output to the core storage circuits through wired logic. Figure 2-10 shows the combinations required to activate each module through 32K. Address selection for 32K through 65K is shown in the FEMM and in WZ20101.

Addressing – Auxiliary Storage

- Auxiliary storage can be selected by CE switches or by an I/O device operating in CE mode
- Program access to auxiliary storage is provided by certain data communication features.

System Storage Capacity	Module Wiring			
	8K	16K	24K	32K
8K	No Connections			
16K	- Bit 2	+ Bit 2	No Connections	
32K	- Bit 2 - Bit 1	+ Bit 2 - Bit 1	- Bit 2 + Bit 1	+ Bit 2 + Bit 1

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Figure 2-10. Core Storage Module Selection

Auxiliary core storage is selected in an array when the address-register-bit-auxiliary line from the P-C is active. Auxiliary core storage addresses are shown in the following table.

	System Storage in 8K Increments							
	1st	2nd	3rd	4th	5th	6th	7th	8th
CE Storage Addresses in Hex	0000 ↓ 00FF	2000 ↓ 20FF	4000 ↓ 40FF	6000 ↓ 60FF	8000 ↓ 80FF	A000 ↓ A0FF	C000 ↓ C0FF	E000 ↓ E0FF
	1100 ↓ 11FF	3100 ↓ 31FF	5100 ↓ 51FF	7100 ↓ 71FF	9100 ↓ 91FF	B100 ↓ B1FF	D100 ↓ D1FF	F100 ↓ F1FF

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The storage-address-bit-auxiliary line (CQ991) is activated when:

1. CAB-bit auxiliary flip-flop is on and the gate-channel-storage-address line is active. This operation takes place when I/O units operate from programs stored in the auxiliary portion of core storage.
2. Gate-M-register-storage-address line ANDs with one of the following lines.
   a. Auxiliary-storage-select line. This line is the result of FORCE AUX in the on position. Only the auxiliary portion of storage is addressed and main storage is inaccessible.
   b. CE-auxiliary-storage-select line. This line is activated by the CE-interrupt-auxiliary-storage flip-flop. The flip-flop is set when the interrupt-to-auxiliary switch is on and the momentary CE-level-interrupt switch is pressed or when a device in CE mode interrupts.
   c. Load-store-auxiliary flip-flop. The flip-flop is set by the main program instructions to log errors in auxiliary storage. This feature is available with CA, 2790 Adapter, or Selector Channel. A modifier bit 9=1 in a two-word instruction operating with the MPX program addresses auxiliary storage. These instructions are load accumulator, load double, store accumulator, double store, logical AND, logical OR, and logical exclusive OR.

Core Storage Arrays

- Core storage arrays are available in two sizes, 4096 (4K) words and 8192 (8K) words.
- Each word consists of 18 bits.
- Both arrays consist of core planes in a 168 x 68 matrix (168 x 64 program-addressable).
- The 8K array contains 18 physical planes, each of which contains one bit-position for each word.
- The 4K array contains 9 physical planes, each of which contains two bit-positions for each word.

2-μsec and 4-μsec Core Storage Arrays

Because the 2-μsec and 4-μsec core storage units use different address drive circuits and different inhibit/sense circuits, the use of the array terminals is different. The 8K and 4K array descriptions given here are based on the 4-μsec storage. It applies to the 2-μsec storage arrays except for references to the drive circuits. The differences can be seen by comparing bottom-board and diode-board diagrams for the two units. The ALD numbers for the 4-μsec storage begin with SD; the corresponding diagrams for the 2-μsec storage have the same page number except they begin with SA. The inhibit/sense terminals for the two units are shown in SA/SD061. The 1803 uses two-μsec storage units.

8K Array

The 8K core storage array consists of a bottom board, 18 core planes, and a diode board. The bottom board plugs into the SLT board and provides connection from the SLT circuits to the X, Y, and inhibit/sense lines of the array. SD012 shows the 4-μsec core storage SLT board with an 8K array disconnected and indicates the path of typical address and inhibit/sense lines.

SD071 shows the land pattern for the bottom-board terminals; the connectors are not shown. The even-addressed Y write driver and read gate lines go from the connectors, through the land pattern, to terminals B4-35 and B46-77; the odd-addressed lines go to terminals D4-35 and D46-77. The even-addressed X write driver and read gate lines go to terminals C2-17 and C20-35; the odd-addressed lines to terminals A2-17 and A20-35. The write driver/read gate windings of Bit 17 plane connect directly to the bottom-board terminals.

The X and Y write gate and read driver lines go from the connectors, through the bottom-board land-pattern, to the following terminals: even-addressed lines to B1-3, B36-45, and B78-80; odd-addressed lines to D1-3, D36-45; and D78-80. The lines then go along the sides of the array to the corresponding terminals of the diode board. The diode-board

land-pattern (SD081) connects the lines to the common terminals of the diode packs. From the individual diodes, the land pattern connects to the terminals at the sides of the diode board.

DIODE BOARD TERMINALS: Note that the storage address register SD081 is divided into X and Y High Order and Low Order positions. If the X portion of the specified address is even (pos. 8 = 0), the active X terminal is on side C of the array. If the X portion of the address is odd (pos. 8 = 1), the active X terminal is on side A of the array.

If the Y portion of the address is even (pos. 15 = 0), the active Y terminal is on side B of the array; if odd (pos. 15 = 1), the active Y terminal is on side D.

Locate the specified terminals by finding the group of lines associated with the X and Y high order positions of the address. The relative position of the line within the group is the same for all low order values and is identified in the enlarged drawing (within broken lines) for each side of the diode board.

ARRAY WINDINGS: The diode-board terminals can be related to the terminals on each plane and the lines can be traced through the array by referring to Figure 2-11. This figure shows the relative location of the 18 cores that form the word at core storage address 0000_{16}. Note that the Y address line for this address enters Bit 0 plane at side B and is activated by positions 9, 10, and 11 (Y high order) of the address register. The X line enters the Bit 0 plane at side C and is activated by positions 3, 4, and 5 (X high order) of the address register. The two lines go through every plane, intersecting at the core at location 0000_{16} in each plane.

At Bit 17 plane, the Y line exits at side B and is activated by positions 12-15 (Y low order) of the address register. The X line exits at side C and is activated by positions 6, 7, and 8 (X low order) of the address register.

The X and Y lines for an odd address enter Bit 0 plane and exit Bit 17 plane at the sides of the array opposite those for an even address, as shown in Figure 2-11 inset. The inhibit/sense lines for an 8K array are shown in Figure 2-12. The lines for plane 1 (bit 0) connect to bottom board terminals at side C; alternate planes connect to sides A and C. The bottom board connects the lines to the inhibit/sense cards through the land patterns and connector blocks (SD012).

BOTTOM BOARD TERMINALS: From the terminals of Bit 17 plane, the lines go to the bottom board terminals (SD071), through the land pattern to the connectors (not shown), and through the SLT board land-pattern to the drivers and gates.

The bottom board also provides connection from the inhibit/sense connectors (not shown) that plug into the SLT board, to terminals 1S-54S at sides A and C.

4K Array

The 4K array consists of a bottom board, 9 core planes, and a diode board. As described in the addressing section, the core planes used in the 4K and 8K arrays are the same. The Y windings in the two arrays are connected in the same way but the X windings are connected differently. Because each physical plane must provide two bit-planes, the X windings go through the B-half of each plane in the array and then through the D-half. SD072 shows the land pattern of the 4K bottom board. Note that at sides A and C the four groups of X lines in the B-half are common to the four groups in the D-half.

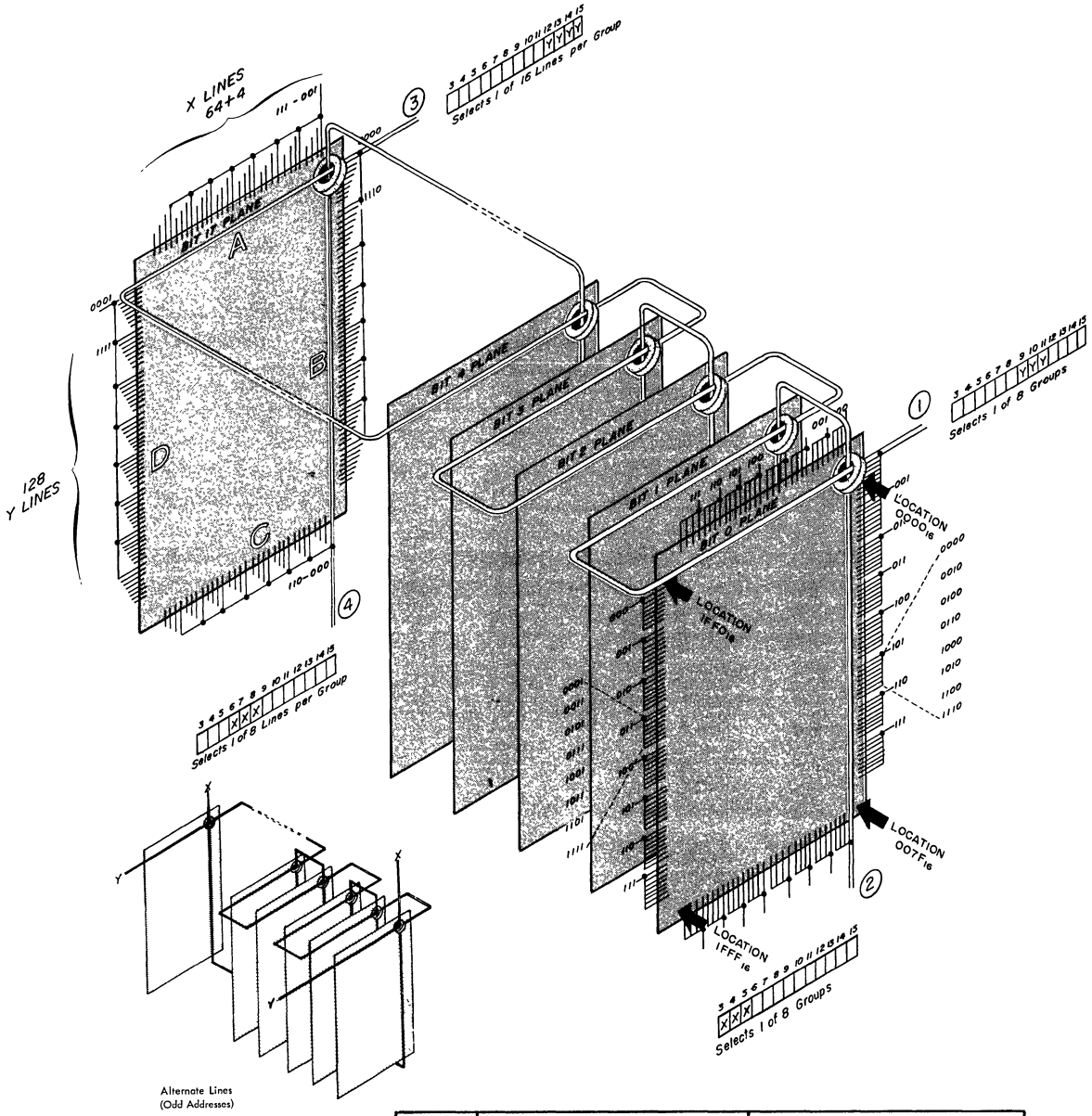
The Bit 16 and 17 X lines shown in Figure 2-13 connect to the bottom-board terminals at side A and C. Side A of the bottom-board land-pattern thus provides the "jumpers" for the even-addressed X lines between Bit 16 and 17 and side C provides the "jumpers" for the odd-addressed X lines. The MDM shows the land pattern for the terminals; the connectors are not shown.

The X and Y write driver and read gate lines go from the connectors, through the bottom-board land-pattern, to terminals at the sides of the array. The write driver/read gate windings of Bit 16 and 17 planes connect directly to the bottom board terminals.

The X and Y write gate and read driver lines go from the connectors, through the bottom-board land-pattern to the indicated terminals, and along the sides of the array to the corresponding terminals of the diode board. The diode-board land-pattern (SD082) connects the lines to the common terminals of the diode packs. From the individual diodes, the land pattern connects to the terminals at the sides of the diode board.

DIODE BOARD TERMINALS: The function of the 4K diode board (SD082) is the same as the previously described 8K diode board. One-half of the X read driver/write gate diode-packs are not used because there are half as many X drive lines in the array. The terminals are numbered differently and sides A and C are used differently.

The B-half of sides A and C provide connection from the diodes to the X read driver/write gate lines in groups of eight lines as do the corresponding terminals of the 8K diode board. The D-half of sides



Note	Four μsec Storage	Two μsec Storage
①	Y Read Driver/Write Gate	Y Read Gate/Write Driver
②	X Read Driver/Write Gate	X Read Gate/Write Driver
③	Y Read Gate/Write Driver	Y Read Driver/Write Gate
④	X Read Gate/Write Driver	X Read Driver/Write Gate

Figure 2-11. X and Y Address Lines for Location 0000, 8-K Array

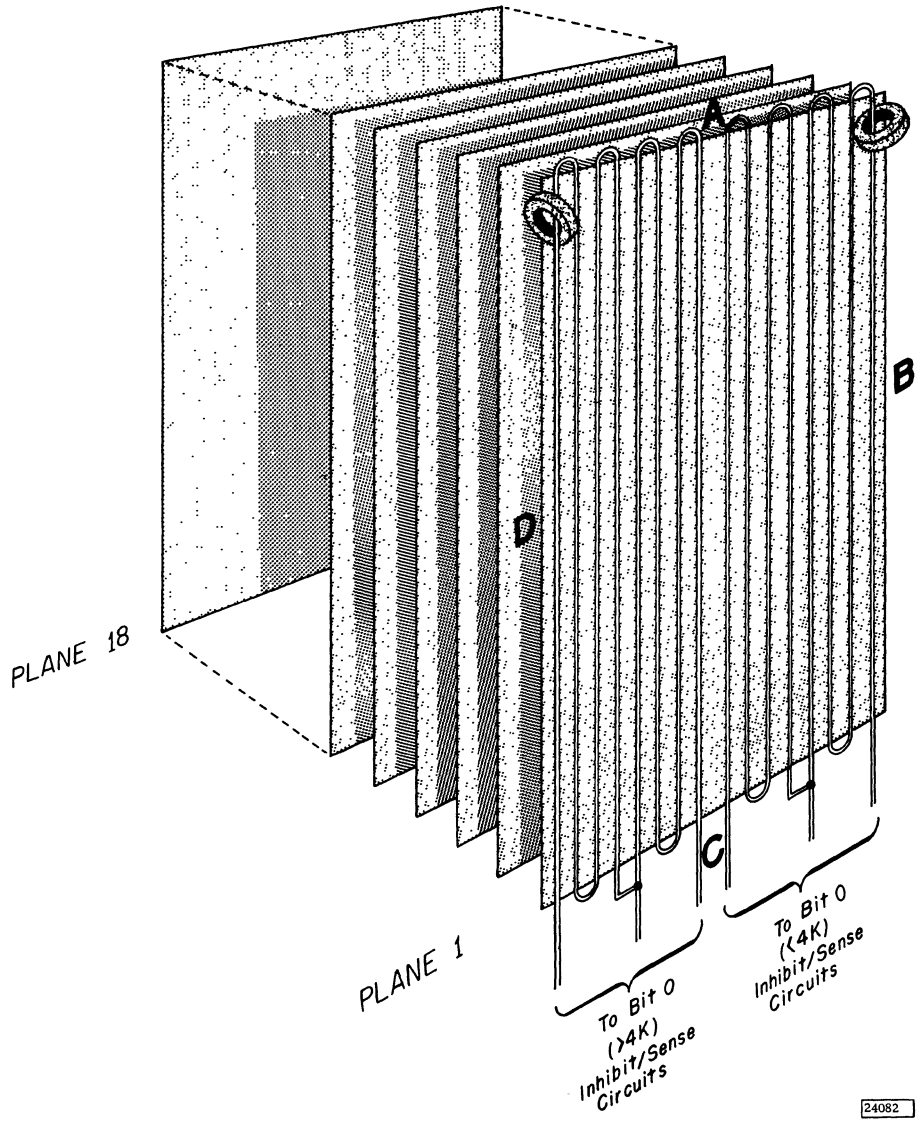
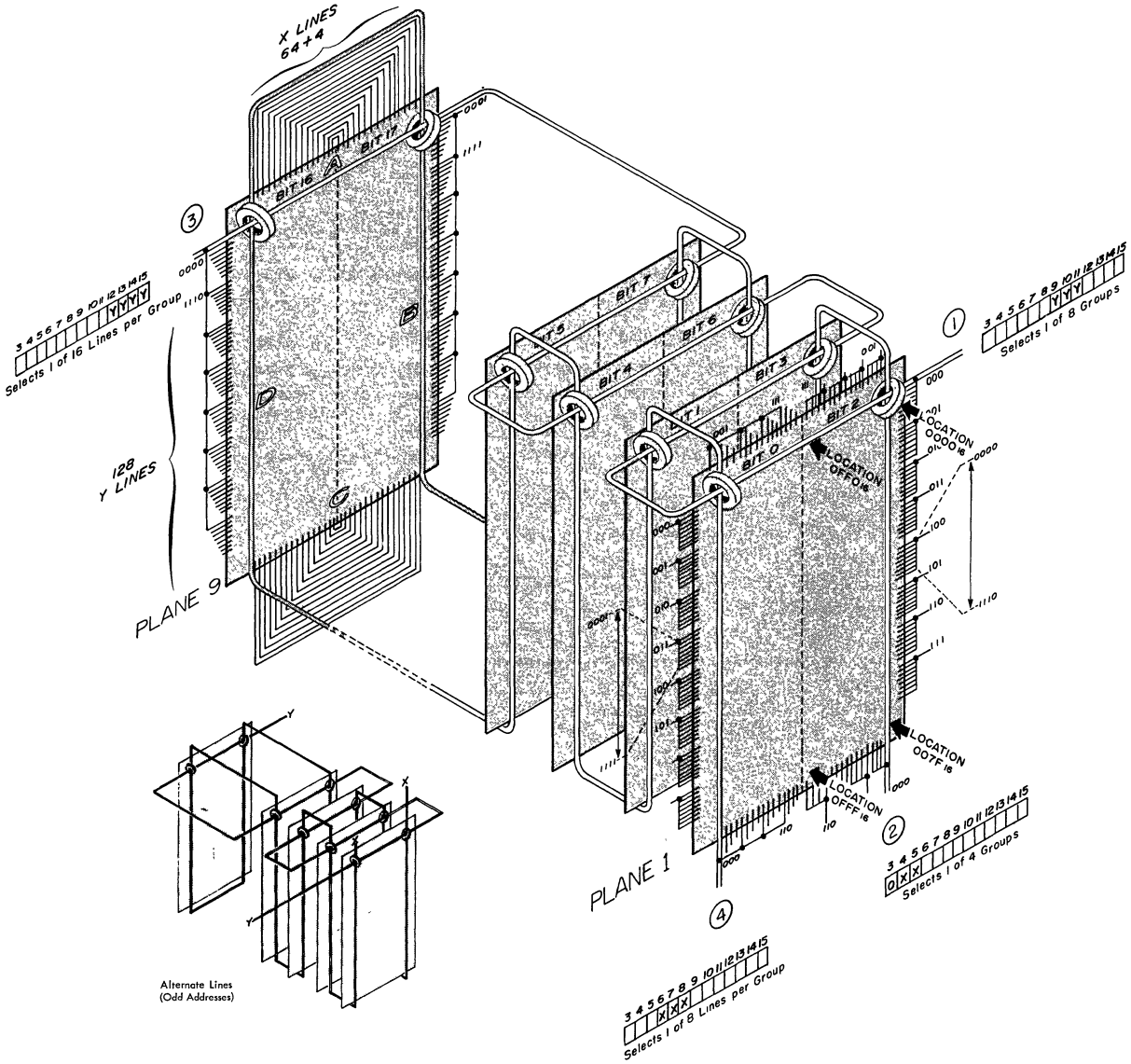


Figure 2-12. Inhibit/Sense Lines for Bit 0, 8-K Array

A and C provide connection from the other end of the lines to the X read gate/write driver lines within the groups.

ARRAY WINDINGS: Figure 2-13 illustrates the 4K array bit-plane layout, the paths of the X and Y windings, and the relation of the windings to the terminals of the bottom board and diode board. The windings within the planes are the same as those in the planes of the 8K array; it is the bottom board and diode board that cause the array to function as 4096 eighteen-bit words.

The even-addressed Y lines, from the read driver/write gate circuits, enter plane 1 through the Bit-2-plane half (side B), go through every plane, and exit plane 9 at the Bit-16 plane half (side D). Odd-addressed Y lines (Figure 2-13 inset) enter plane 1 at side D and exit plane 9 of side B. Even-addressed X lines, in four groups of eight each, enter plane 1 at the B-half of side C, go through the B-half of every plane, and loop back (by the bottom-board land-pattern) to the D-half of plane 9. The lines then go through the D-half of every plane and exit plane 1 at side C to connect to the diode board.



Note	Four μsec Storage	Two μsec Storage
①	Y Read Driver/Write Gate	Y Read Gate/Write Driver
②	X Read Driver/Write Gate	X Read Gate/Write Driver
③	Y Read Gate/Write Driver	Y Read Driver/Write Gate
④	X Read Gate/Write Driver	X Read Driver/Write Gate

Figure 2-13. X and Y Address Lines for Location 0000, 4-K Array

The lines are connected, through the diode board and the bottom board, to the X read gate and write driver circuits.

Odd-addressed X lines (Figure 2-13 inset) enter plane 1 at side A, go through every plane, loop back (by side C of the bottom board), and exit plane 1 at side A.

The inhibit/sense lines for a 4K array are shown in Figure 2-14. The lines for plane 1 (bit 0 and 2) connect to bottom board terminals at side C; alternate planes connect to sides A and C. The bottom board connects the lines to the inhibit/sense cards through the land patterns and connector blocks (SD012).

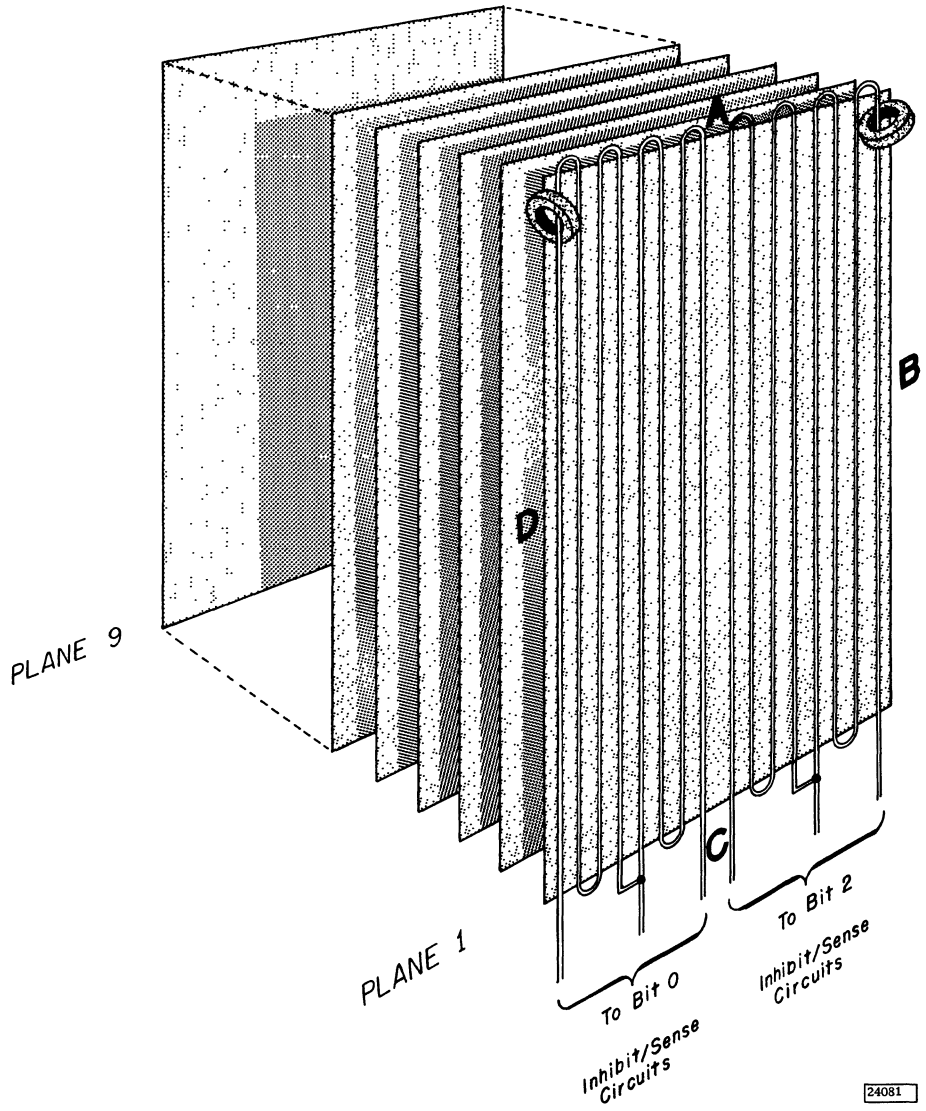


Figure 2-14. Inhibit/Sense Lines for Bit 0 and 2, 4-K Array

Drive Current Generation — 4 usec Storage

- Gate and driver circuits direct the drive current through the array.
- The current control circuit provides a constant current (current sink) for the array.
- A temperature compensated voltage reference is applied to the current control circuit.

The direction in which the half-select current flows in the X and Y address drive-lines is controlled by the driver and gate circuits. These circuits are conditioned by timing, for read and write positions of the cycles, and by the address lines. The block diagram of the 4-μsec core storage (SD011) shows the read and write drivers and gates controlled by the M register lines. Timing control is implemented through the current control block at the top of the diagram.

SD042 shows more detail of the drive line circuits. Looking at the one X drive line shown, note that address lines 3, 4, and 5 condition eight decode circuits. One decode circuit (decode 000 is shown) conditions both an X write gate circuit and an X read driver circuit. During read time, X read driver control will further condition the X read driver

to allow current to flow through the read driver to the X read sink. This X read driver activates a group of eight X lines.

One of the eight active lines is also activated at the other end of the array by an X read gate circuit. The read gate is conditioned by a decode of address lines 6, 7, and 8 (decode 111 is shown). The read gate is further conditioned by X read gate control and current is allowed to flow from the 8.3 volt source through the X drive line. This read gate activates one line in each group of eight but only one line is activated at both ends.

During write time, the same address decodes are still conditioned (the address lines do not change between read and write time). The X read driver control is no longer active; the X write gate control becomes active and conditions the X write gate to activate the same group of eight lines. At the other end of the array, the X write driver is conditioned by the same address decode and by X write driver control to allow current to flow to the X write sink. Half-select current now flows in the same line as during read time but in the opposite direction.

SD043 shows still more detail of the driver and gate circuits. In this diagram, read current flow is shown by the heavy lines. The controlling circuits, identified by broken lines, must be conducting to activate the read gate and read driver circuits.

When the read or write timing pulses are not conditioning the control circuits (quiescent state), current flow is in the driver control and gate control circuits only. The center transistors of these two circuits are forward biased by the 1.4 volts at their bases; the only current flow is through these transistors.

The read gate circuit conducts when all the address-line (low-order bits) inputs are positive and the read gate control circuit is conditioned by the read-timing inputs.

The read driver circuit conducts when all the address-line (high-order bits) inputs, located in the write gate portion of the diagram, are positive and the read driver control circuit is conditioned by the read-timing inputs.

The current in the read gate control circuit places a bias on the emitter of the center transistors of the driver control and gate control circuits, cutting them off.

Half-select current is now flowing through the selected X and Y drive lines in a direction to flip the cores from the "one" state to the "zero" state or "read" the addressed position of core storage.

The circuits return to the inactive state, current flows in the gate control and driver control circuits only, after the read timing pulses fall. When the write timing pulses rise, current is switched to the write gate and write driver circuits and therefore flows through the array in the same drive line but in the opposite direction. This X and Y half-select current causes the selected cores to flip to the "one" state, thus writing into the addressed position of core storage.

The V-Reference voltage applied to the current control circuit is temperature compensated, causing the X-Y drive current to track along its optimum value over a specified temperature range.

Drive Current Generation — 2 usec Storage

- Gate and driver circuits direct the drive current through the array.
- The read source circuit provides a constant current for the array during the read cycle.
- The write sink circuit provides a constant current for the array during the write cycle.
- A temperature compensated voltage reference is applied to both the read source and write sink circuits.

As in the 4-μsec core storage, the direction in which the half-select current flows in the X and Y address line is controlled by the driver and gate circuits. These circuits are conditioned by timing, for read and write portions of the cycle, and by address lines.

Comparison of the 4-μsec addressing diagrams with the 2-μsec storage addressing diagrams (SA041 and SA042) shows two basic differences.

The driver and gate circuit locations are reversed; that is, where the 4-μsec storage uses the Y write gate, the 2-μsec storage uses the Y read gate. The other basic difference that can be seen in these diagrams is the current source and sink. The 4-μsec storage current flow (conventional current flow, pos. to neg.) is from a +8.5V to the array current sink (-3V) for both read and write currents. The 2-μsec storage read current flow is from the read source to -15V and the write current flow is from ground to the write sink.

SA043 is a detailed diagram of the 2-μsec storage drive circuits. Conventional current flow for

the read portion of the cycle is from the read source circuit (+12V), under control of read timing signals, through the read gate circuit that is selected by a decode of the address lines. The current flows through an isolation diode and the drive line that is connected to the active read driver at the other end of the array. The read driver is conditioned by a decode of the address lines and by a read timing pulse. The current flow is through the driver to -15 volts.

Write current flow is from ground, through the active write gate - activated by write timing pulse and an address decode. Current flows through the array line that is in the group of lines connected to the active write driver. Current flows through the write driver, activated by write timing pulses and an address decode, to the write sink circuit and -15V.

The current magnitude is controlled by a temperature controlled reference voltage, (V Ref) that is applied to both the read source and write sink circuits.

The array termination, consisting of a resistor at the common of each group of isolation diodes, provides a characteristic impedance to the array lines. These circuits absorb the discharge pulse from the non-selected array lines and any reflected waves that build up on the lines.

Inhibit/Sense — 4 usec Storage

- The inhibit/sense winding is common to every core in one plane in the 4K array; common to every core in one-half of one plane in the 8K array.

- During read time, the inhibit/sense windings c conduct pulses, caused by the "flipping" of selected cores, to the sense amplifier circuits.

- During write time, the inhibit/sense winding carries inhibit current to prevent the "flipping" of selected cores.

Each inhibit/sense winding passes through 4096 cores of one plane. The 8K array has two inhibit/sense windings per bit-plane; the 4K array has one per bit-plane. Figure 2-12 shows the inhibit/sense scheme for the 8K array. Figure 2-14 shows the inhibit/sense scheme for the 4K array.

The functions of the inhibit/sense winding are explained in the Magnetic Core Theory section of this chapter.

Inhibit Driver

SD051 shows the 4-μsec storage inhibit/sense circuits; SD051 shows some of the timing pulses of these circuits. The inhibit driver has two outputs that drive a center-tapped winding. Each output supplies approximately 200 ma of inhibit current. Data from the CPU B-register is gated to the inhibit drivers by a storage timing pulse. When the inhibit driver is conducting, inhibit current prevents the writing of a "one" in the selected core storage location.

Sense Amplifier

The sense amplifier has a differential input and a single-ended output. The sense control voltage determines the sensitivity of the amplifier and compensates for voltage supply and temperature variations. The first stage of this three stage amplifier is deactivated during the write cycle by the emitter-strobe pulse.

The first stage is kept out of saturation by a 0.7 volt offset voltage that is applied to the second stage. During the read cycle, the output of the second stage is gated to the final stage by the sense strobe. When a "one" is sensed, the output of the final stage is a negative pulse.

Inhibit/Sense — 2 usec Storage

- The 4- and 2-μsec storage inhibit/sense windings serve the same purpose, as described in the magnetic core theory section of this chapter.

- The connections on the array are different for the two units as shown in SA/SD061.

- The 2-μsec storage inhibit/sense circuits are shown in SA051.

Inhibit Driver

Three inputs condition the inhibit drivers, as follows: data, timing, and an address line. The data inputs are the Not lines from the B register that allow inhibit current to flow in the bit planes in which a "one" bit is not to be written. The timing input is the inhibit time pulse, described in the Timing section

that follows. The address line is the M-register-bit-3 line that separates inhibit drivers into less than 4K and greater than 4K circuits.

The inhibit driver output attaches to the inhibit/sense lines at the center point of 4096 cores. The two end-points of these lines connect to ground. Each inhibit circuit provides control for one bit-plane in a 4K array or for one-half a bit-plane (<4K or >4K) in an 8K array.

Inhibit current flow is from ground, through 2048 cores, through the inhibit driver that is conditioned, to -V Inhibit (V_Z). V_Z is a temperature responsive voltage that ranges from -9 to -12 volts.

Sense Amplifier

As in the 4-μsec storage, the 2-μsec storage sense amplifier has a differential input from the two ends of the inhibit/sense line for 4096 cores. The center point of this line connects to the corresponding inhibit driver.

The first stage collectors contain a transformer circuit that eliminates any dc unbalance to provide an equal detection-threshold for both polarities of signal. This stage does not require the emitter strobe that the 4-μsec sense amplifier requires. The 0.8 volts at the emitter of the second stage keeps the first stage out of saturation.

The sense-strobe pulse gates the output of the second stage to the final stage. A negative pulse output of the final stage results when a "one" bit pulse is conducted from the array to the sense amplifier input.

Timing — 4-usec Storage

- SD031 shows the timing pulses for the four-μsec storage.
- X read gates and drivers are conditioned at T0 time for a duration of approximately one μsec.
- X write gates and drivers are conditioned at T4 time for a duration of approximately one μsec.
- The conditioning of Y read and write gates and drivers is delayed to allow X drive line noise to subside.
- 4-μsec storage timing-pulse generation is initiated by the transition of the CPU read/write cycle.

Figure 2-15 represents the 4-μsec storage "clock" and timing circuits. The CPU provides the following signals to the storage timing circuits: read cycle, write cycle, storage select, and the M-reg-3 address line. The following timing pulses are generated by the "clock" circuit: long time, short time, and strobe. Combinations of the CPU signals and the generated timing pulses provide read and write gate and driver control, strobe pulses for less than and greater than 4K, emitter strobe pulse, and inhibit pulses for less than and greater than 4K.

Note in the timing chart (SD031) that Y write current and Y read current rise after X read current and X write current.

The delay of the Y currents minimizes the effect of excess noise at the rise of the X current pulse. This noise is caused by the discharge of array capacitance.

4-usec Storage Clock (Figure 2-15)

- A time delay "clock" circuit develops the necessary timing pulses for addressing, reading from, and writing into core storage.
- Long time: a time delay circuit provides a 1-μsec pulse at T0 (read cycle) and at T4 (write cycle).
- Short time: a latch provides a pulse that begins after the rise of long time and ends with the fall of long time.
- Strobe: a single shot, activated by short time, provides a pulse that is ANDed with read cycle and an address line.
- Inhibit time: long time and write cycle are ANDed to develop inhibit time.

Time Delay Circuit (Figure 2-16). Read cycle and write cycle are connected to opposite ends of a 1 μsec delay line. The low resistance of the delay line causes the levels at the inputs (points 1 and 2) to balance. For example, if read cycle is 0 volts and write cycle is +3 volts, points 1 and 2 balance at +1.5 volts.

When read cycle and write cycle change levels (at T0 and T4 time), the input points reflect the respective levels for 1 μsec then balance again. The same effect is evident at the taps (points 3 and 4) except for a shorter duration.

Timing — 2 usec Storage

- SA031 shows the timing pulses for the 2-μsec storage.

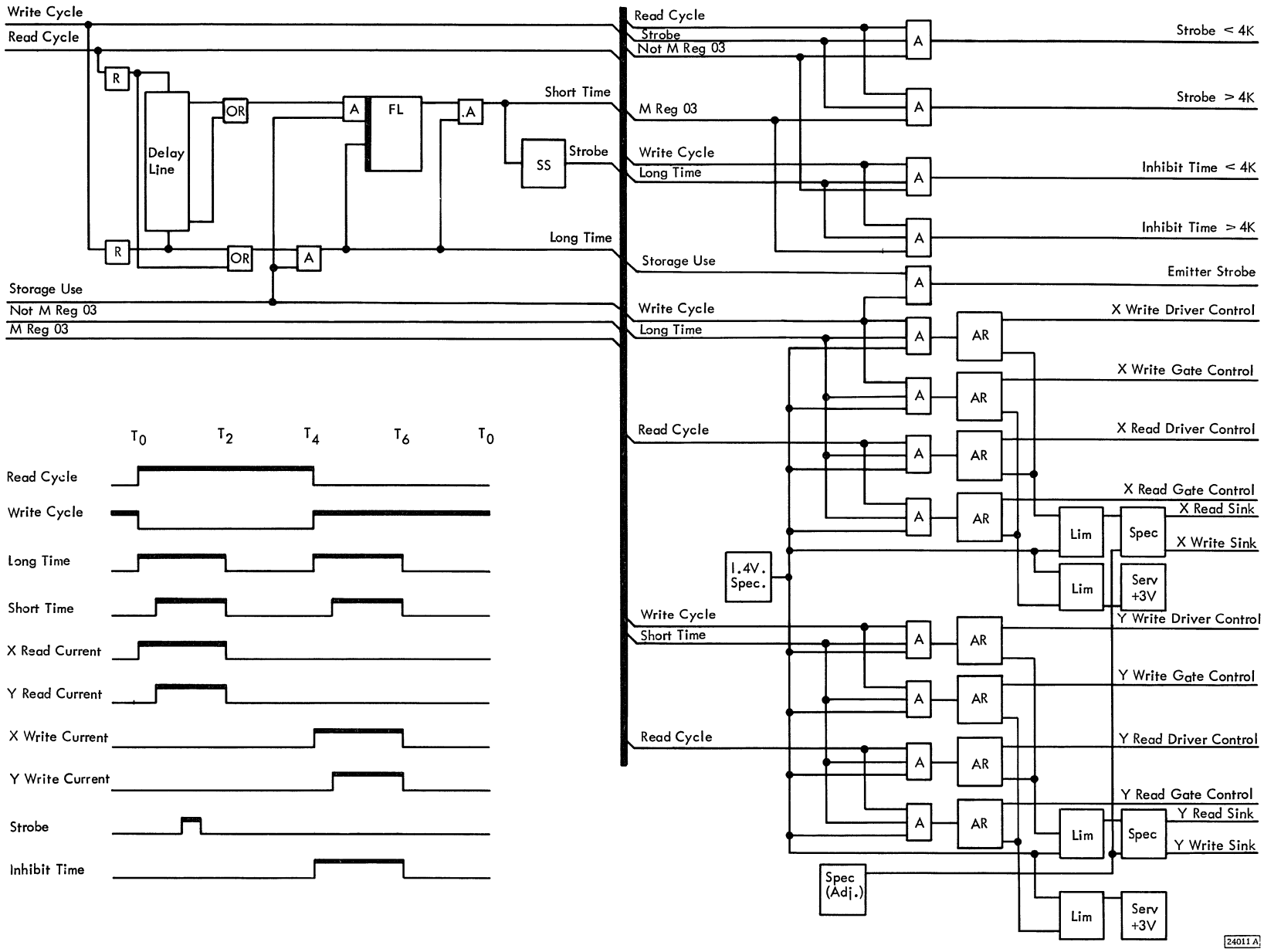


Figure 2-15. Four-Microsecond Core Storage Clock

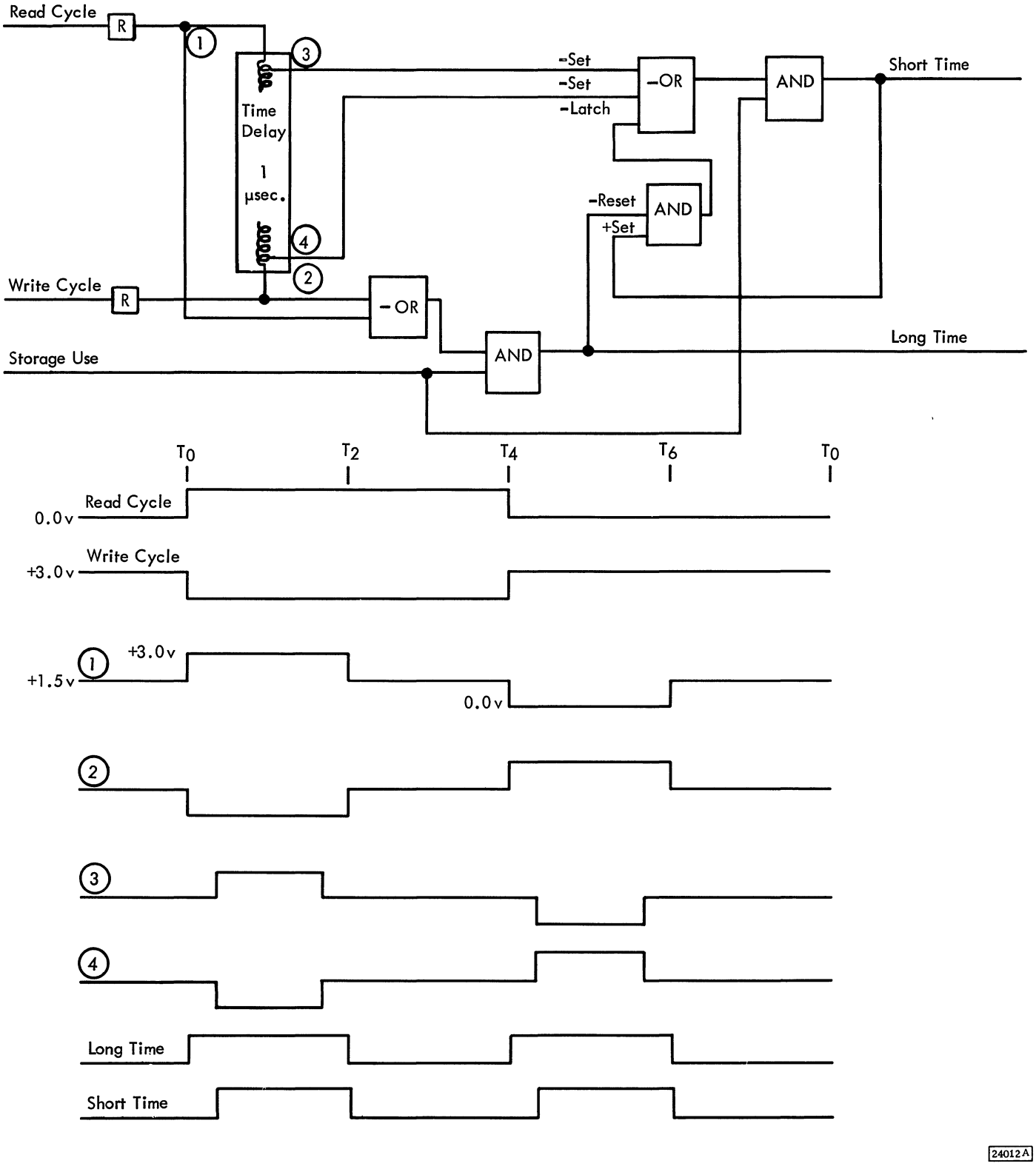


Figure 2-16. Time Delay Circuit, Four-Microsecond Storage Clock

- WZ20100 shows the 2-μsec storage "clock" and pulse generation circuits.
- X read gates and drivers are conditioned at T0 time for approximately 750 nsec.
- X write gates and drivers are conditioned at T4 time for approximately 750 nsec.
- Y read drivers and write gates are conditioned at the same time as the X drivers and gates.
- The conditioning of Y read gates and write drivers is delayed 100 nsec after the X drivers and gates to allow X drive line noise to subside.

The 2-μsec "clock" consists of a time delay circuit three latches, and two single-shots. The timing pulse generation is initiated by the storage-select pulse from the CPU. Storage-select, which is a 100-nsec pulse at T0 and T4 or X0 and X4, turns on the long-time latch and the inhibit-time latch. Storage-select is also connected to the input of a time delay circuit for the following; the 100-nsec delayed output turns on the short-time latch, the 600-nsec output turns off long-time and short-time, and the 650-nsec output turns off inhibit-time.

The timing chart shows theoretical and actual timing for each signal. It shows long time coming up soon after T0 time, falling at the 750-nsec point, rising again soon after T4 time, and falling 750 nsec later. The inhibit-time latch is turned on at the same time that long-time is but the timing shown is inhibit-timing, after it has been ANDed with write cycle.

Short-time rises 100 nsec after long-time and falls at the same time. Strobe is a 330-nsec pulse generated by two single-shots that are started by short-time.

Long-time and short-time are ANDed, in various combinations, with read-cycle and write-cycle to produce X and Y gate/driver timing. The X read and write gate and driver circuits are conditioned by long-time. The Y read driver and write gate is also conditioned by long-time; but, the Y read gate and write driver are conditioned by short-time.

Strobe is ANDed with not-inhibit-timing and address-register-bit-3 to produce sense-strobe-8K; not-address-register-bit-3 is used to produce sense-strobe-4K.

In the timing chart (SA031), the Y current (low order end) shows a pulse at T0 and T4 time. This pulse is present, due to the initial charging of array capacitance, although the Y line is not conditioned at the other end at this time. The Y read current (high order end) and Y write current (high order end) begins at short time, when both ends of the line are conditioned.

Inhibit-time is ANDed with write-cycle to produce inhibit-timing, shown in the timing chart. Inhibit-timing is ANDed with the data lines and address-register-bit-3 or not-address-register-bit-3 (not shown in the diagram) to activate the inhibit drivers for less than and greater than 4K.

CHANNEL CONTROL

- Consists of four major areas:
  1. Basic channel circuits.
  2. Interrupt circuits.
  3. Data channel circuits.
  4. Interval timer circuits.
- Provides a means of controlling I/O devices attached to the 1800 system.
- Provides direct access to core storage (cycle stealing) for the higher speed I/O devices.
- Provides interrupt and interval timer capabilities.

There are two methods of transferring data to or from the processor-controller. Direct program control is a method in which each data word transfer requires an individual Execute I/O instruction. The interrupt circuits implement this method.

Cycle stealing is a method in which the device, when ready to transfer data, takes one processor-controller cycle to access core storage. Data channel circuits control this operation.

Basic Channel Circuits

- Decode IOCC function code and control channel data flow accordingly.
- Provide timing pulses for channel operations.

I/O operations are initiated by an XIO instruction that references an Input/Output Control Command (IOCC). The XIO instruction reads the IOCC control word from core storage and places it on the out bus. The basic channel control circuits decode the function code for all I/O commands and control the channel operation for direct-program-control

commands. Figure 2-17 shows the data flow in the basic channel circuits.

Function Register

- Stores the three-bit function code received from the B register via the channel data bus.
- Decoded output controls the I/O operation.

Three flip-flops are set by B register bits 5, 6, and 7 gated by XIO control cycle at T5 or X5 time. The reset occurs at the end of the data cycle. The output is decoded by seven AND circuits as follows:

Function Register Position 5	6	7	Decoded Function
0	0	1	Write
0	1	0	Read
0	1	1	Sense Interrupt
1	0	0	Control
1	0	1	Initialize Write
1	1	0	Initialize Read
1	1	1	Sense Device

Basic Channel Timing

- Execution of the XIO instruction consists of control and data cycles.
- The control cycle flip-flop is on during the first E cycle to designate the control cycle.
- The data cycle flip-flop is on during the second E cycle of all I/O operations except the read and write commands; for these two commands, it is on during the third cycle.
- Three timing pulses are sent to the I/O device adapters: time pulse-A, -B, and -C.

All I/O commands require a control cycle to transfer the IOCC control word to the I/O adapters. Control, sense interrupt, and sense device commands transfer control or sense data on the second E cycle (designated the data cycle). Read and write commands use the second E cycle to read the IOCC address word from core storage and load it into the accumulator to address core storage for the data word. The third E cycle of the read and write commands transfers the data word and is therefore designated the data cycle.

The initialize read and initialize write commands read the IOCC address word from core storage and load it into the channel address register during the E2 (data) cycle. Data is transferred during cycle steal cycles for these two commands.

CONTROL AND DATA CYCLES: XIO control and XIO data cycles are designated by two flip-flops (Figure 2-18). The control cycle flip-flop is turned on at the beginning of the first E cycle of any XIO operation. It is reset at T7 of the same cycle. Its output conditions channel and I/O adapter circuits during the control cycle.

The data cycle flip-flop operation varies with the I/O command function, decoded during the control cycle. If the function is a command other than read or write, the data cycle flip-flop is turned on at T0 of the E2 cycle. The turn-on is conditioned by E1 cycle but the shift pulse (T0) is not available in time for this cycle (see multi-input trigger, Appendix A).

If the function is read or write, the data cycle flip-flop is conditioned by E2 cycle and the shift input is T0. The flip-flop is therefore turned on at T0 time of the E3 cycle. It is reset at T7 time.

The data cycle flip-flop output (XIO data cycle) conditions circuits in the channel and in the I/O adapters during the data cycle.

CHANNEL TIMING PULSES: Three timing pulses are generated in the channel control circuits. The I/O adapters use these timing pulses to synchronize the device operation with the processor-controller operation. These pulses, time pulse -A, -B, and -C, are generated by three flip-flops (Figure 2-19) that are controlled by the processor-controller (T) clock and the channel (X) clock pulses.

Time Pulse A and Time Pulse B flip-flops are turned on by the same line, T1, T3, X1, X3. The pulse on this line occurs at two times in each cycle. Only the pulse at T1 or X1 affects the Time Pulse A flip-flop; it is already on when the second pulse, T3 or X3, occurs.

The time pulse B flip-flop input is further conditioned by the on status of time pulse A. Time pulse B is therefore turned on at T3 or X3 time.

The turn-off of both time pulse A and time pulse B are conditioned by the same line, T5, T7, X5, X7. Time pulse B turn-off is further conditioned by the off condition of time pulse A.

The time pulse C flip-flop is operated in a binary fashion from T clock and X clock pulses 0, 2, 4, and 6. It turns on at 0 time, off at 2, on at 4, and off at 6.

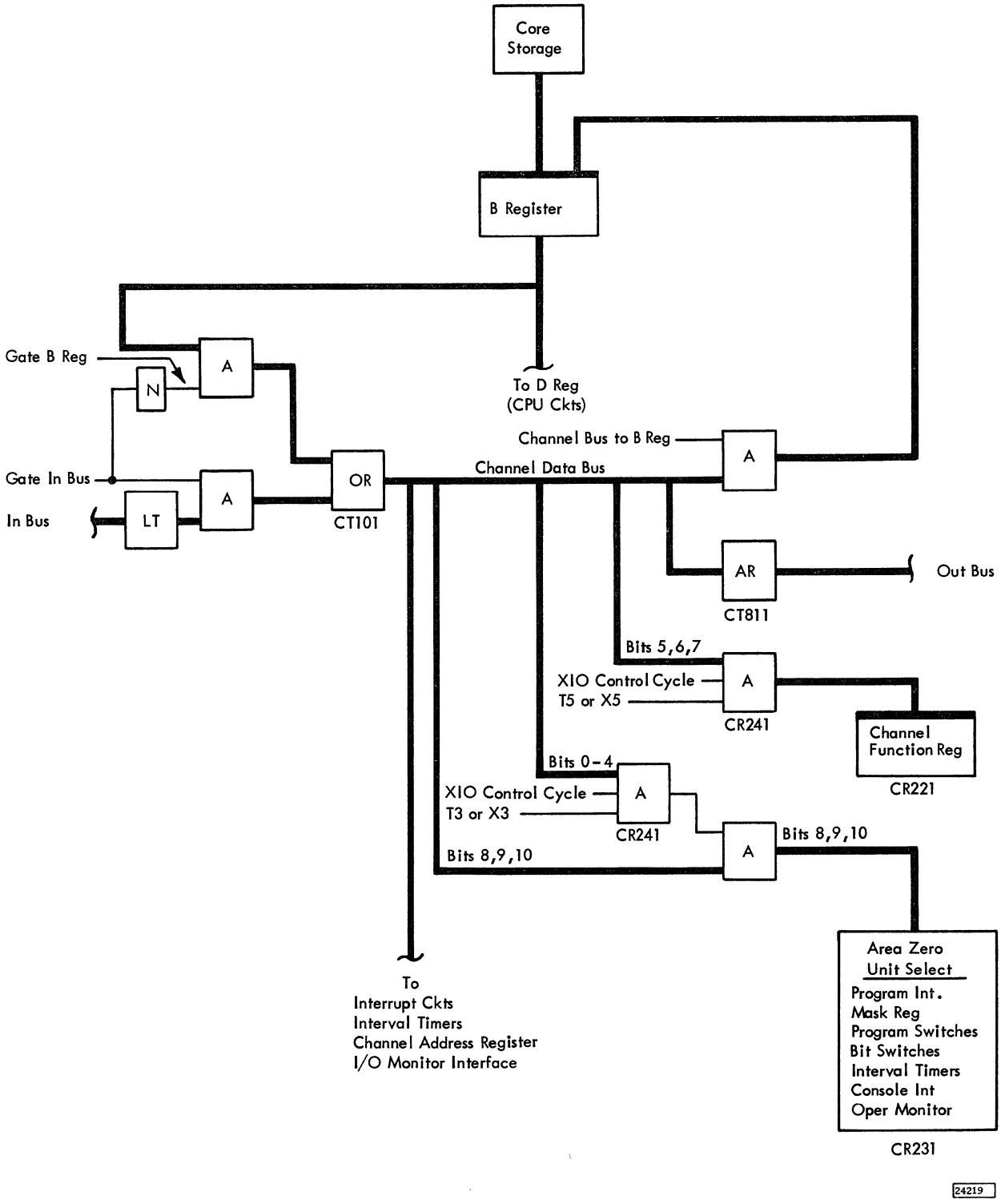


Figure 2-17. Basic Channel Data Flow

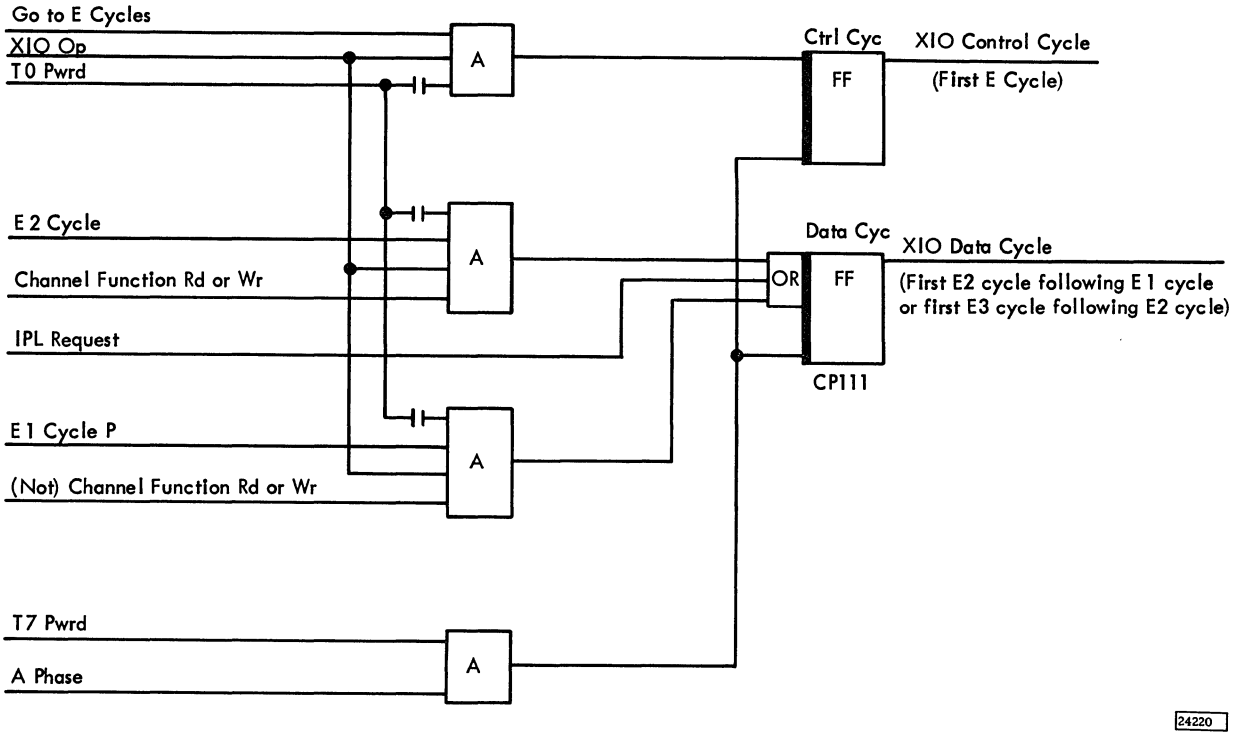


Figure 2-18. XIO Data and XIO Control Cycle Generation

Note: X1 and T1 are doubled in duration when operating with an 1803. Refer to 'X Clock Delay' (CR241) and 'T1 Delay' (CC041).

Interrupt Circuits

- The interrupt circuits detect the interrupt condition, and initiate the interrupt sequence.
- The interrupt polling circuits determine when an interrupt can be detected.
- The interrupt register stores the interrupt level until servicing is completed.
- The interrupt controls generate the interrupt BSI instruction and address.
- CS50100 is a simplified logic diagram of interrupt operation; CS60101 is a flow chart of the Interrupt BSI instruction; CS70101 is a timing chart of the interrupt sequence.

Interrupting conditions in the I/O devices are assigned to interrupt levels according to customer requirements (CS50100, Sheet 1, C3). Because there are 27 interrupt levels and only 16 in-bus lines to conduct the interrupt requests to the processor-controller, these lines must be shared. This is accomplished by gating internal level and levels 0 through 13 onto the in bus (CS50100, Sheet 1, D3) at one time and levels 14 through 23, trace, and CE onto the in bus at another time.

Interrupting conditions can occur at any time relative to the processor-controller program. Therefore, interrupt requests must be gated onto the in-bus lines when these lines are not being used for data transfer. This interrupt request gating is called interrupt polling.

Interrupt polling in the 1800 system is accomplished by means of two polling signals, interrupt poll level 0 through 13 and interrupt poll level 14 through 23. These signals are generated by the interrupt polling circuits at T1 and T5 time and are gated to the I/O devices via two unique lines in the channel cables (CS50100, Sheet 1, A5). In the I/O device adapter these polling signals gate the interrupt request from the adapter to the interrupt circuits in the processor-controller via the in-bus (Figure 2-20). Whenever an interrupt condition is detected in an I/O device, the interrupt request from the adapter sets the associated interrupt-level

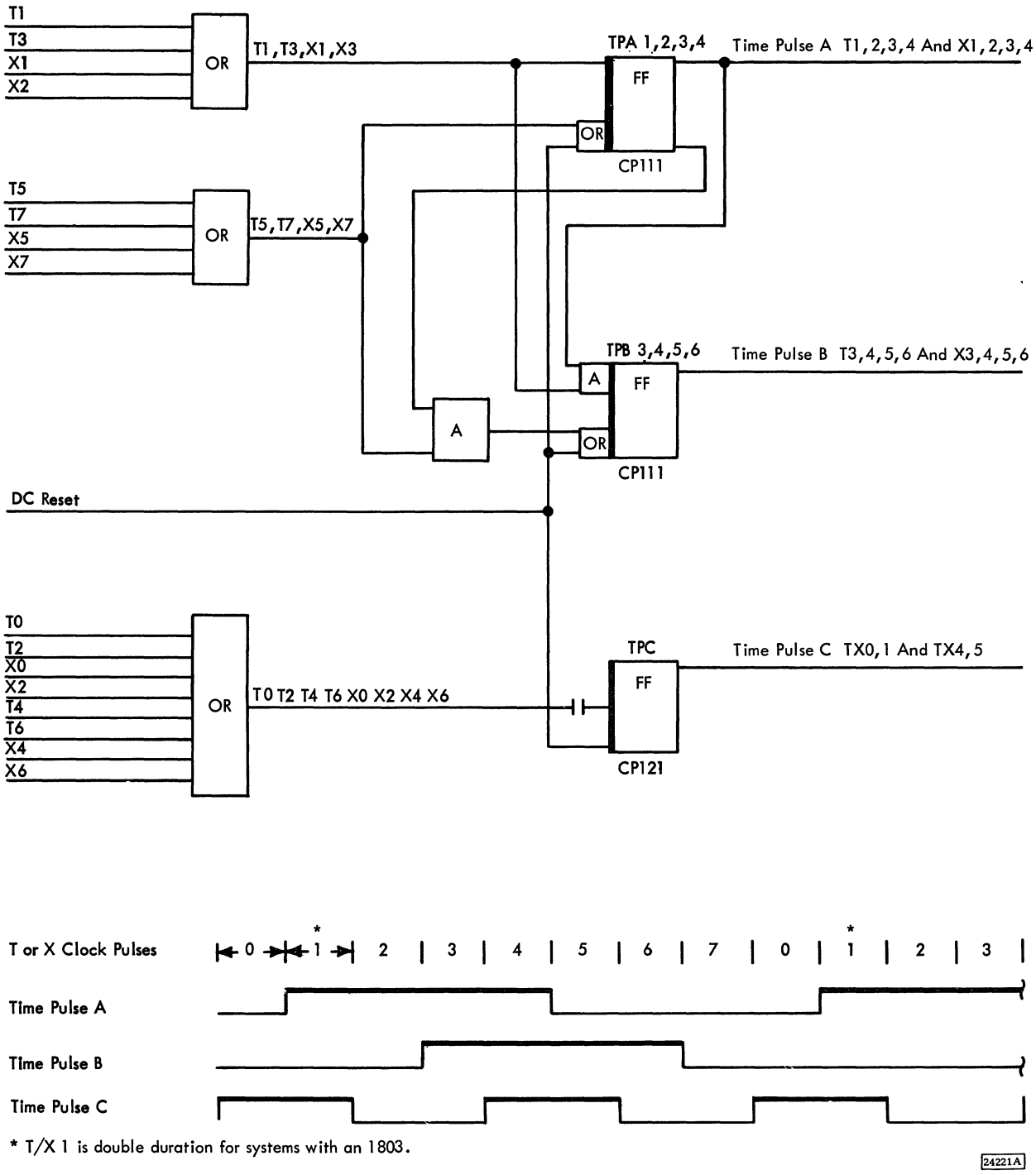


Figure 2-19. Basic Channel Timing

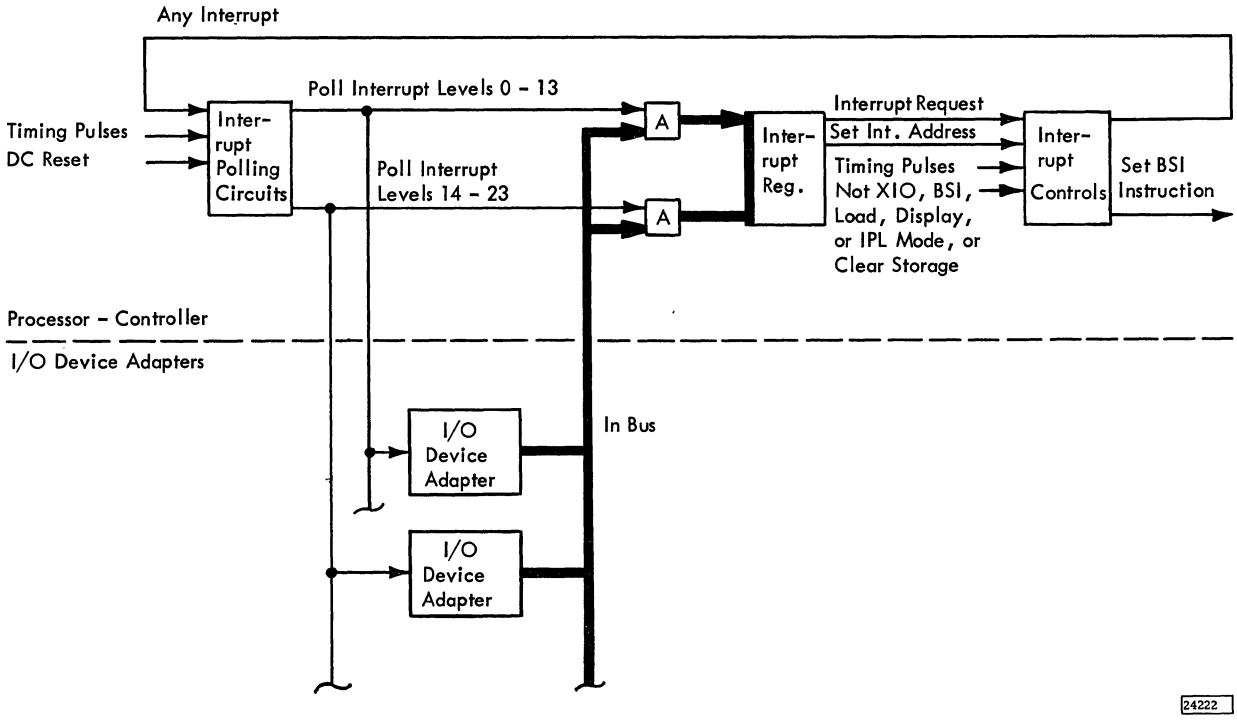


Figure 2-20. Interrupt Circuits - Block Diagram

flip-flop in the interrupt register (CS50100, sheet 1, B5). The interrupt level flip-flops can be masked (CS50100, sheet 1, C4) by instruction from the P-C. When an interrupt level flip-flop has been masked by the P-C, the interrupt request from the associated device cannot set the interrupt level flip-flop, and no interrupts are generated for that device.

Whenever an interrupt is detected, and the interrupt-level flip-flop is set, the interrupt-request line is activated to the interrupt controls. This line generates the any-interrupt line (CS50100, sheet 2, D3) to the interrupt polling circuits, and inhibits interrupt polling (CS50100, sheet 1, A2). On completion of the instruction in which the interrupt was detected, the interrupt controls generate the BSI instruction (CS50100, sheet 2, D4). This instruction is wired into the machine and generated automatically on detection of an interrupt. The interrupt BSI instruction is a BSI, long, indirect instruction, with three peculiarities.

These are:

1. The instruction is generated by circuits within the interrupt controls and therefore access to core storage is not required during the I1 cycle.
2. The address is also determined by circuits within the interrupt control and interrupt register, and does not require the accessing of core storage during the I2 cycle.
3. The instruction register is not incremented during the I1 or I2 cycle.

Interrupt Polling Circuits

- Consist of two flip-flops, polling and gate poll (CS50102, A6 and E6).
- DC reset turns the gate-poll flip-flop off and sets the polling flip-flop to poll B (interrupt levels 14-23).
- Polling occurs only if gate-poll is on.
- Interrupts are polled at T1 and T5 time during most instructions. During an I1 cycle, polling occurs at T5 only.
- Interrupts continue to be polled during a wait instruction.

- Polling is inhibited during:
  XIO or BSI instructions;
  load, display, or IPL mode;
  clear storage operation.

The gate-poll flip-flop conditions the poll-interrupt level lines to the I/O devices, and the poll A/B flip-flop determines which interrupt levels are to be polled. Following a dc reset the polling sequence is: interrupt levels 0 through 13 polled from T1 to T5 and sampled at T5; interrupt levels 14 through 23 polled from T5 to T1 and sampled at T1. The gate poll and poll A/B flip-flops (CS50102, E6 and A6) are set on at T1 after a dc reset. Poll A (gate for 0 through 13) is effective when the poll A/B flip-flop is on. When the poll A/B flip-flop changes to off, the set interrupt level 0 through 13 pulse ANDS with any bits present on the in bus to turn on the corresponding interrupt level flip-flop (CS50101). An interrupt can not be set if it is masked. Any interrupt turns off the gate poll flip-flop, maintaining the status of the poll A/B flip-flop and preventing interrupt polling. An interrupt request timing chart is shown on CS70101.

Interrupt polling is inhibited by several conditions: an XIO instruction or a BSI instruction and by the display load, or initial program load modes, and also by the clear storage operation. At these times, the gate-poll flip-flop (CS50102, E6) remains off. An exception to this is the XIO and BSI instructions during which the gate-poll flip-flop is reset at T4 time. Polling is also inhibited in the second half of the BSC instruction if a branch out occurs (D2). This condition occurs at T4 time and inhibits the second poll during that instruction.

The wait instruction requires a special polling sequence, because the T and X clocks are not running (stopped at T7, X7). In this case, the 4-μsec-timer-clock signal (B4) provides the shift to turn on the gate-poll flip-flop and to complement the poll flip-flop. This shift occurs every 8-μsec in the 2-μsec system and every 16-μsec in the 4-μsec system.

There are five conditions which reset the gate-poll flip-flop: DC reset, a shift count of 0 at T0 time, an XIO, Interrupt Level CE Active, or a BSI operation at T4 time. If an interrupt has been detected, the gate-poll flip-flop will be reset at T2 time or at T5 time after request-interrupt-level is activated.

Interrupt Register

- Consists of:
  Mask flip-flops
  Interrupt level flip-flops
  Interrupt level request flip-flops
  Priority AND circuits

- Interrupt levels 0 through 23 are masked following a dc reset.

- The interrupt-level and interrupt-request flip-flops are turned off by dc reset.

- The mask flip-flops are individually set by an XIO control instruction with the mask register selected.

- Interrupt levels 0 through 23 can be programmed with an XIO control instruction with the interrupt level register selected.

The interrupt register provides a means of storing interrupts until servicing has been completed, determines interrupt priority, and permits inhibiting interrupts. The interrupt register consists of 27 interrupt-level and interrupt-level-request flip-flops, and 24 mask flip-flops. Three interrupt levels cannot be masked, interrupt level check (internal), interrupt level trace, and interrupt level CE. The only way in which interrupt level internal, trace, or CE can be inhibited is by turning on the disable interrupt switch (CS50101, C7). This switch inhibits all interrupts in the 1800 system.

The disable interrupt switch effectively delays the interrupts. The interrupting indicators in the I/O adapters remain active unless they are reset by a sense-device command. When the disable interrupt switch is turned off, all the active interrupt requests are gated to the interrupt circuits by their respective polling pulse.

The dc reset line performs the following functions in the interrupt register:

Mask flip-flops 0 through 23 are set on.
The interrupt-level flip-flops and the interrupt-level-request flip-flops are turned off.

Following a dc reset, all interrupt levels (except check, trace, and CE) are masked by the mask flip-flops and must be enabled with an XIO control

instruction. This instruction selects the interrupt mask register, clearing all mask flip-flops, and then sets individual mask flip-flops.

The primary difference between the interrupt mask and the disable interrupt switch is that the interrupt mask is set to inhibit any corresponding interrupt from setting the interrupt-level and request flip-flops. The disable interrupt switch prevents the level flip-flop from setting the level-request flip-flop. Interrupts from the I/O devices are recorded by the level flip-flops, but the interrupts are not serviced at this time since the request flip-flop is not set. If an interrupt has been masked with a mask flip-flop, the level flip-flop is not set and no record of the interrupt is made in the CPU. The interrupting indicator in the device adapter may remain active.

The interrupt-level flip-flops are set at the end of each polling sequence (T5 and T1 time) if an interrupt has been detected in an I/O device. The interrupt request from the device and the set-interrupt pulse generated by the fall of the polling signal turns on the interrupt-level flip-flop. Turning the interrupt-level flip-flop on generates the turn-on for the interrupt-level-request flip-flop. Unless the output of the interrupt-level-request flip-flop is inhibited by the disable-interrupt switch or an interrupt of a higher priority, the any-interrupt line is activated (CS50101). The interrupt-level-active circuit consists of an AND circuit conditioned by the interrupt-level flip-flop, the not-disable-interrupt line, and the not-any-higher-interrupt line. The priority sequence for the interrupts is check, 0, 1, 2, etc. through 23, trace, and CE.

The interrupt level flip-flops can also be programmed on. This is accomplished by the generation of an XIO control instruction with the interrupt level register selected and a special code. This sequence is called the program interrupt selected. This actually consists of two instructions. The two instructions are distinguished by the IOCC control word bit 15 = 0 and bit 15 = 1. Bit 15 = 0 enables setting interrupt levels 0 through 13, and bit 15 = 1 enables setting interrupt levels 14 through 23 (CS50102, C2). This instruction forces the generation of the set-interrupt pulse at T5 time of the XIO data word cycle. Once the interrupt-level flip-flops are set by this instruction the interrupt circuits perform as in a normal interrupt.

The interrupt-level flip-flops alert the interrupt controls that an interrupt has been detected. The output of the level-request flip-flop is gated only when this particular interrupt is the highest level interrupt requesting service. The level flip-flop records the existence of an interrupt and the level-request flip-flop indicates that this is the highest level requiring service. If a lower level interrupt has also been set, this interrupt cannot generate an interrupt request until the higher level interrupts have been serviced.

Interrupt Controls

- Activated by the interrupt-level and level-request flip-flops from the interrupt registers.
- Inhibit interrupt polling during an XIO or interrupt BSI instruction.
- Generate a BSI instruction and address after detecting an interrupt.
- Reset the level-request flip-flop on completion of the interrupt forced BSI instruction and reset the interrupt-level flip-flop on completion of interrupt servicing (branch out).

The interrupt controls (including the interrupt-request flip-flops) are activated by the highest level interrupt-level and its corresponding level request from the interrupt registers (CS50101). The generation of the interrupt BSI instruction and address, and the interrupt level and level-request flip-flop resets are generated by the interrupt controls. The interrupt controls also inhibit the use of core storage, increment the instruction register, and generate interrupt polling. The interrupt controls consist of the interrupt request flip-flop and the required AND circuits which generate the timing pulses used in the generation of the interrupt BSI instruction. The interrupt-request flip-flop is set by any interrupt, a shift count of zero, and T7 B phase (CS50100, sheet 2, E3).

Any-interrupt is generated by the interrupt registers at T5 or T1 time following the polling cycle. When an interrupt is detected, the interrupt registers are set at T5 or T1 time, and the interrupt request flip-flop is set at T7 B time (end of operation). If the interrupt registers are set at T1 time, the polling sequence ending at T5 time is inhibited before the interrupt-request flip-flop is set. When an interrupt request has been generated by the interrupt registers, interrupt polling is inhibited by the any-interrupt line (CS50102, A3).

INTERRUPT REQUEST: The interrupt-request flip-flop is set at T7 B time of an end of operation following any interrupt (CS50103, B4). This flip-flop remains set until T7 time of the I2 cycle of the interrupt BSI instruction. The interrupt-request flip-flop generates the BSI instruction during the I1 cycle

and the indirect address for the BSI instruction during the I2 cycle (CS70101, Lines 10 and 11). The set-interrupt-BSI-operation and the gate-interrupt-address lines are generated immediately following the set of the interrupt-request flip-flop. These lines remain active throughout the I1 and I2 cycles of the BSI instruction and enable the interrupt controls to generate the required bits for the interrupt BSI instruction and the interrupt address.

INTERRUPT BSI INSTRUCTION: The interrupt BSI instruction is generated automatically by the processor-controller on detection of an interrupt (CS60101). Two different BSI instructions are generated: the CE interrupt generates an operation code 4400_{16} and all other interrupts generate an operation code 4480_{16}. Three cycles are required to generate and execute the CE BSI (I1, I2, and E1). When the BSI operation code is 4480_{16} (not a CE interrupt) an IA cycle is required after the I2 cycle and before the E1 cycle. The interrupt BSI differs from a programmed BSI in that the interrupt BSI does not access core storage during the I1 and I2 cycles or increment the I register.

The interrupt BSI instruction is gated to the channel data bus at T7 B time. At T0 time the channel data bus is gated to the B register.

The generation of the operation code bits (4480_{16} or 4400_{16}) is controlled by the shift-counter-equals-zero line (end operation). If a bit is required, the shift-count-equals-zero line is wired to that position. Bit position 8 has an additional condition (CE interrupt request-CT091) which inhibits the generation of this bit on a CE interrupt.

At T5 time of the I1 cycle the shift counter is set to 1 (this is a normal function) deconditioning the BSI instruction bits and allowing the interrupt-request-level to generate the interrupt BSI address bits during the I2 cycle. Each interrupt level generates a unique address as determined by the interrupt address generator. The interrupt address uses bits 10 through 15 and always sets bits 0 through 9 to zeros. Addresses 8_{16} through 22_{16} are reserved for this instruction.

At T7 time of the I2 cycle the IA bit is checked. If this bit is a one, the IA-cycle flip-flop is set and a normal IA cycle is performed. When the IA bit is a zero the interrupt BSI is for a CE interrupt and the E and E1-cycle flip-flops are set.

Setting the IA-cycle flip-flop resets the set interrupt BSI sample flip-latch at T0 time and initiates an IA cycle.

Following the IA cycle the interrupt BSI initiates a normal E1 cycle. This cycle stores the contents of the I register in the core storage location (effective address) specified by the IA cycle. At T3 time the M register is transferred to the I register where the effective address is incremented by one (EA+1). The E1 cycle is terminated at T7 time by an end-operation pulse. At T0 time (following the end operation) the I register is transferred to the M register and the first instruction of the interrupt routine is addressed.

The CE interrupt stores the contents of the instruction register at core storage location $000A_{16}$ in main core storage and branches to location 0001 in main storage or in auxiliary storage, depending on the position of the interrupt to aux/main switch. The branching is accomplished by resetting, then incrementing the I register.

Data Channel

- Provides a direct access to core storage for high speed I/O devices.
- Requires a single machine cycle to transfer a data word between core storage and an I/O device.
- Does not disturb the contents of, or require the use of, internal CPU registers other than the core storage buffer register.
- Must be initialized by an XIO instruction, initialize write or initialize read.
- Consists of priority controls, channel address registers and buffer, and cycle steal controls.
- Data channel addressing and data flow is shown on CQ40100.

High-speed I/O devices, such as magnetic tape units and disk storage units are able to control the transmission of data to and from core storage on a "cycle-stealing" basis. The registers, data paths, and control required for this function are called a data channel.

The operation of a data channel is initiated by the execution of an XIO instruction which references an I/O control command (IOCC) having a function of initialize write or initialize read. Once started, the data channel has the responsibility for controlling the quantity and destination of all data transmitted between core storage and the attached I/O device. Because of the independent operation of the data channel, large blocks of data can be transferred between core storage and an I/O device while many program instructions are performed between I/O control commands.

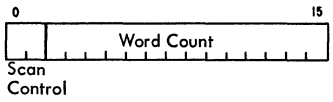
Since the P-C and data channel share core storage, the execution of the main-line program is automatically suspended for a minimum of one cycle each time the data channel is activated by a cycle steal request. Once the data channel takes control of the P-C, the data channel operation must be completed before control reverts to the P-C. The operation of the data channel does not interfere with data contained in the internal P-C registers since the data channel contains its own address registers and word counters, and has direct access to the core storage buffer register.

A maximum of 15 data channels are available with the 1800 system. Since all data channels share the data channel controls, a priority system is required to prevent multiple data channels from accessing core storage simultaneously. The priority of a device is assigned by the user, and is not programmed.

Data channel operations are initialized with an XIO instruction. The first cycle steal request from any data channel reads the word count and scan control bits for that data channel from core storage and transfers this information to the word count register (WCR) and the scan control register (SCR) in the device adapter. The word count and scan control bits are contained in a single 16-bit word (Figure 2-21).

The ability to chain in a continuous scan of the same or several different tables is a function of the individual device. A device need not have the chaining function in order to interrupt at the conclusion of the data transmission in the table.

The device requests references to core storage at a rate depending upon its requirements and independently of program execution. The cycle steal,



Bit 0	Bit 1	
0	0	Single scan and stop with an interrupt at the end of the data table.
0	1	Single scan and stop with no interrupt.
1	0	Continuous scan (chaining) with an interrupt at the end of this data table.
1	1	Continuous scan (chaining) with no interrupt.

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Figure 2-21. Data Channel Word Count Format

in response to the request, utilizes the next available core storage cycle and sends, through the data channel, the contents of the addressed location. During this cycle the address is incremented and the word count (if required) in the device adapter is decremented by one.

The above sequence continues until the data channel makes the last core-storage reference of the current message. This last reference is sensed by the word count becoming zero during the cycle or through some indicator in the device. If the device does not have chaining ability, no more requests for core storage reference are made until the device is reinitialized.

The following general description of chaining applies to devices other than the selector channel. (A description of chaining for the selector channel appears on FS10110.)

For a device with chaining ability, another request is made if a continuous scan is indicated by the scan control register. The data which comes from storage is the address of the next message. This address may be the starting address of the same data table or that of a new data table. Instead of incrementing the address, the data from core storage is loaded into the channel address register.

The chaining control then requests the first word of the new message. This word must be the address of its own core storage location. This address is compared with the contents of the specified channel address register. If they are not equal, a CAR check (error) is indicated. The chaining control requests a third cycle-steal cycle to read out the second word of the data table. This word contains a word count and two bits for scan control. The word count is loaded into the word count register and the two bit control field is stored in the scan control register for use at the end of the data table. If the word count as read from storage is zero, the operation is terminated immediately.

The length of time between data transfer cycles in a chaining operation is a maximum of two P-C cycles for a device connected to cycle-steal priority zero, unless that device is a selector channel. (A description of chaining for the selector channel appears on FS10110.) The time for devices of lower cycle-steal priorities may be greater, depending on what other cycle-steal requests are active.

Priority Controls

- Prevent multiple data channels from addressing core storage simultaneously.
- Consist of a flip-flop and channel address register control circuits for each cycle steal level.

- Cycle-steal level 0 is highest in priority and level 14 is lowest in priority.

When an I/O device requires a cycle-steal cycle, the cycle-steal-request level for that device is activated. The cycle-steal-request line sets the associated cycle-steal-priority flip-flop (CQ40120, B5, 1442) in the data channel and initiates the cycle-steal cycle. The following functions are gated by the priority circuits during a cycle-steal cycle:

1. Channel address register (CQ40121, A7, level 0) is gated to channel address buffer (CQ40120, A8) and core storage by time pulses 7, 0, and 1 of the cycle-steal (X) clock.
2. CAR is reset at X3 time (cycle-steal-control-0 inactive and cycle-steal-control-1 active - Figure 2-22). This action occurs during load CAR cycles only.
3. CAR is incremented at X4 time (cycle-steal-control-0 active, cycle-steal-control-1 inactive, and cycle-steal-control-2 active).

The cycle-steal-request line is activated by the I/O device, indicating that the device requires a data transfer. At the fall of T6 or X6 time, the priority flip-flop is set. If a device of a higher priority is requesting service, the active line for the lower level request(s) is inhibited and the 0, 1, and 2 flip-flops are reset (off). The active level is returned to the requesting I/O device, via the wired logic and mixer board, as the cycle-steal-acknowledge signal to indicate that that device is controlling data channel operations (Figure 2-23). The cycle-steal-acknowledge line also gates CAR to core storage and sets the any-cycle-steal latch in the cycle-steal controls.

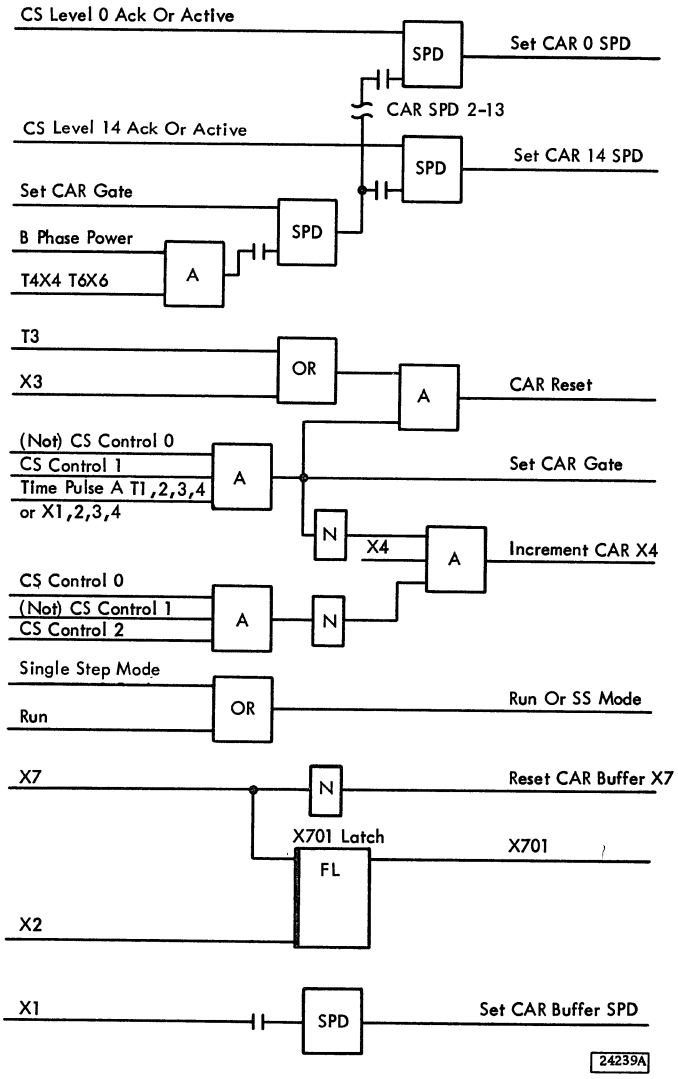
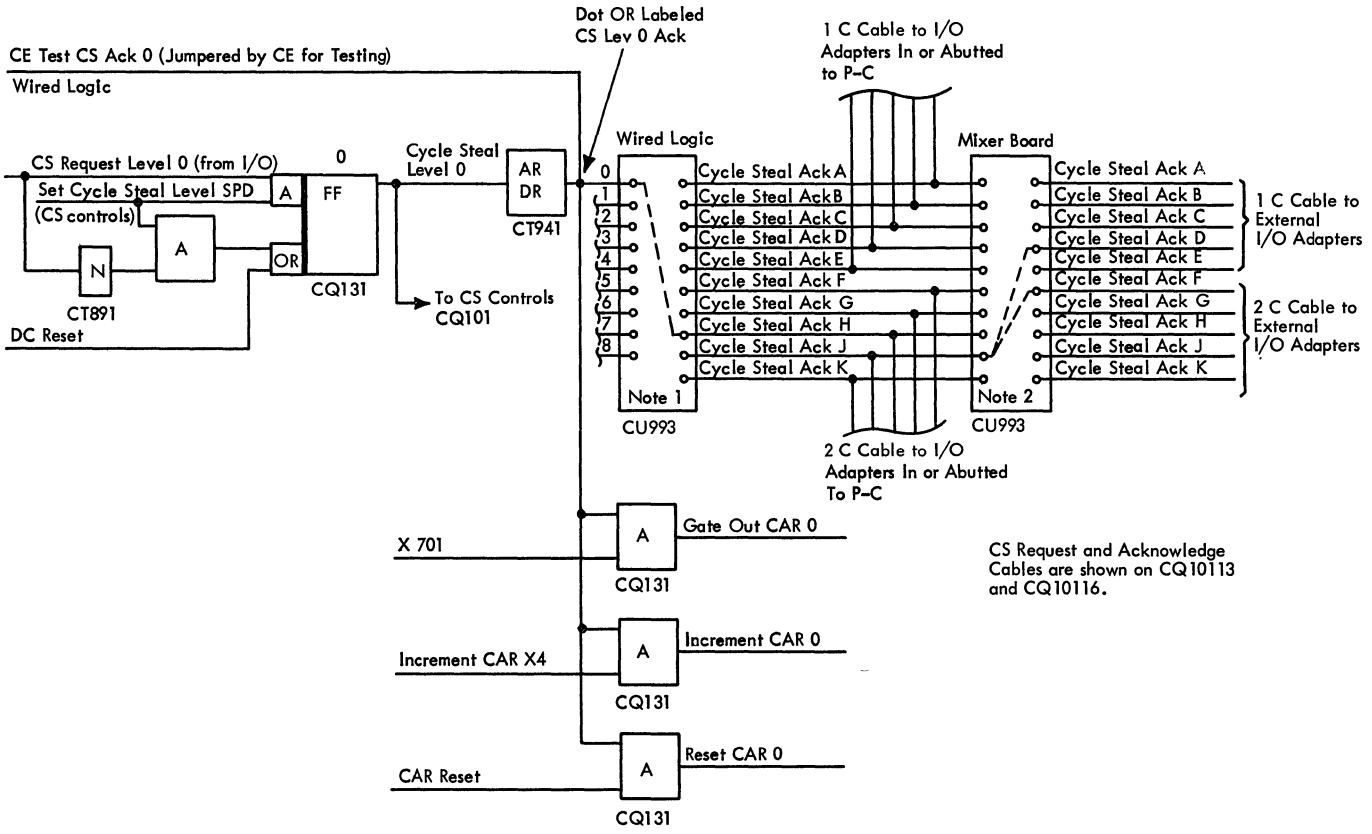


Figure 2-22. Cycle-Steal Sequence Control

Channel Address Registers and Buffer

- Each data channel has a sixteen-bit channel address register (CAR) for storing the cycle-steal address.
- Each cycle-steal cycle increments CAR.
- CAR is initially loaded with the address portion of the IOCC word from core storage.
- During a cycle steal-cycle, CAR is gated to CAB and core storage at X7, 0, and 1 time.
- CAR addresses core storage until channel address buffer (CAB) is loaded (X1).
- CAB addresses core storage during the remainder of the cycle-steal cycle.
- CAB is reset at X7 time.

The function of the fifteen channel address registers for the data channel is similar to that of the I register for the CPU. The CAR is loaded from core storage when the data channel is initialized and incremented each time the data channel requests a cycle steal thereafter. During the CAR increment, CAR functions as a binary ring. The increment pulse complements bit position 15, turning off bit 15 complements bit position 14, and so on (Figure 2-24). The increment pulse occurs at X4 time of a cycle-



Note 1: Any CS Lev X Ack can be wired to any Cycle Steal Ack line or lines, in the wired logic. However, each CS Lev X Ack line must be terminated to a Cycle Steal Ack line in the wired logic.

Note 2: Any Cycle Steal Ack Level from the wired logic can be terminated to any Cycle Steal Ack line, or lines, in the Mixer/Board. This permits any I/O device to be connected to any Cycle Steal level.

24240A

Figure 2-23. Cycle Steal Acknowledge Generation (Basic System)

steal cycle unless inhibited by the cycle-steal-control lines from the I/O device adapter.

The channel address buffer is similar in function to the M register in the CPU. The CAB is always loaded from CAR and provides the data channel with a direct access to the core storage address circuits (Figure 2-24). The purpose of CAB is to by-pass the core storage M register during a cycle-steal cycle and to hold the address while CAR is incremented. The CAB is set to the value of the selected CAR at X1 time of a cycle-steal cycle and reset at X7 time.

Cycle Steal Controls

- Control the starting, stepping, and stopping of the cycle-steal (X) clock.
- With the X clock, generates the sequence control lines which control all cycle-steal cycles.
- A scan is made at the end of each T6 or X6 time to determine if a device requires a cycle-steal cycle.

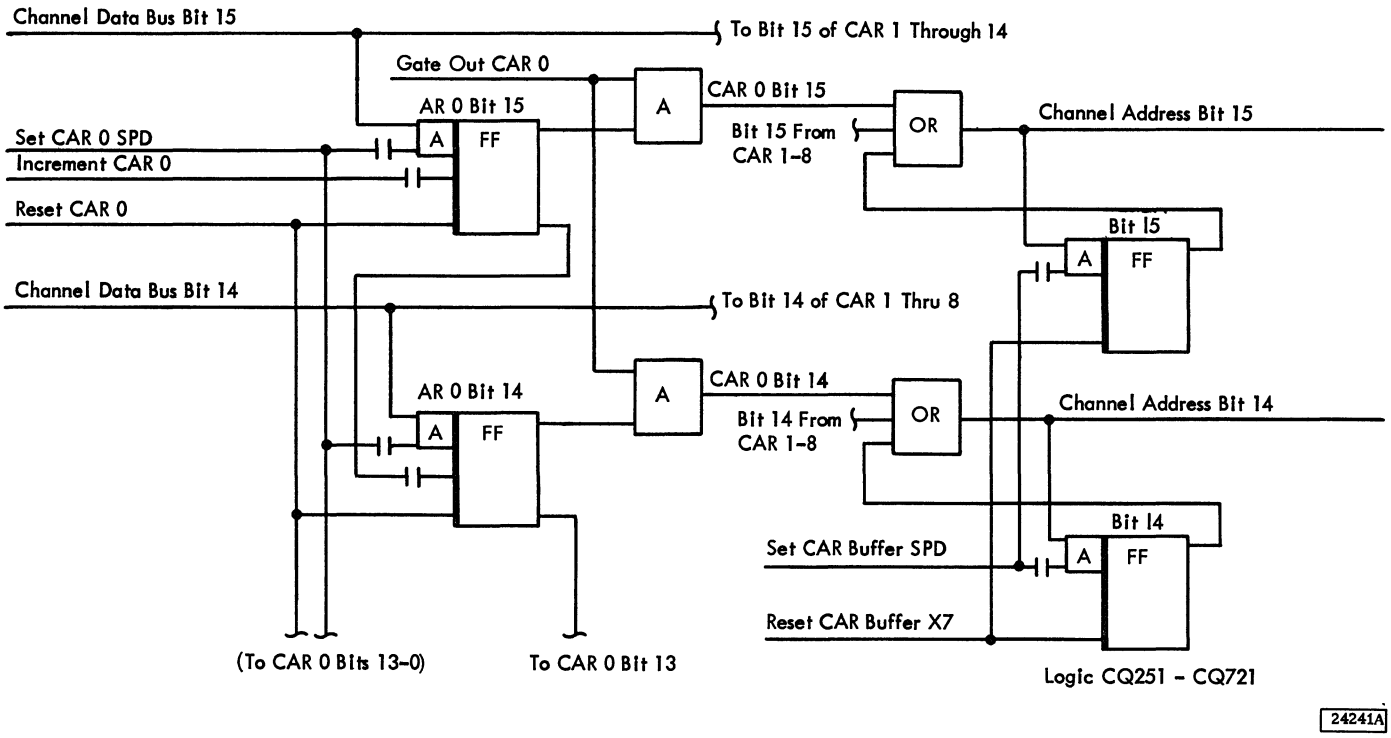


Figure 2-24. Channel Address Register and Buffer

- A simplified diagram of the set-cycle-steal-request and X-clock-advance circuits is on CQ50101.

At the conclusion of each machine cycle, the cycle-steal controls scan the cycle-steal-request lines from the I/O devices. If a request is detected, the appropriate cycle-steal-request flip-flop is set and the any-cycle-steal line is activated.

The any-cycle-steal line stops the T clock advance at T7 time, starts the X clock, and inhibits the M register from addressing core storage.

The set-cycle-steal-level line initiates all cycle-steal cycles in the data channel. This line is activated at every clock 7 time (T7 or X7) except when in load, display, or IPL mode, or during the clear storage sequence. At clock 6 time (T6 or X6), the cycle-steal-polling latch is turned on. The output of this latch conditions the gate input to the set-cycle-steal-level sample pulse driver (SPD). The shift input to the SPD is generated by ANDing the latch output with a phase A pulse (AND 5N). AND 5N produces two pulses during clock 6 time. The second pulse fires the set-cycle-steal-level SPD, which initiates the cycle-steal scan.

If a cycle-steal request is conditioned, the cycle-steal priority latch is set and the any-cycle-steal line is activated. This line inhibits the normal CPU storage cycle, and inhibits the T clock advance. Any-cycle-steal also starts the X clock and activates the cycle-steal-gate-storage-address line. The cycle-steal-gate-storage-address line and the gate-out-CAR line gate the contents of the channel address register to the storage address bus in the CPU, selecting the address for the cycle-steal data transfer.

The oscillator phase-B pulse turns off the cycle-steal polling latch (AND 1J) and enables the following phase-A pulse to generate the X-clock-advance pulse.

The X-clock-advance level fires the X-clock-advance SPD unless inhibited by the turn-on of the X-clock-delay flip-flop. The X-clock-delay flip-flop delays the stepping of the X clock for one clock time each time it is set. This delay extends the X7 time following the execution of an XIO operation (X7, X7, X0, X1, etc.) or, X1 time during a timer cycle-steal cycle (X7, X0, X1, X1, X2, etc.). The X7 delay allows the I/O bus to settle following an XIO instruction; the X1 delay allows the input gating of the I register to settle before the B- to I-register transfer during a timer cycle-steal cycle.

At X1 time the CAB is set with the contents of CAR. The CAB maintains the channel address on the storage address bus until X7 time. X2 time deconditions the gate-out-CAR line and allows X4 time to increment CAR without changing the address on the storage address bus.

At X6 time the cycle-steal-polling latch is set. The cycle-steal-request lines are scanned and the corresponding level flip-flops are set or reset (cycle-steal-request sets the flip-flop and not-cycle-steal-request resets the flip-flop). If a cycle-steal-request is not detected, the T clock is started at 7 time and the X clock is stopped.

The X clock which controls the data channel functions during a cycle-steal cycle is similar to the T clock in the CPU. The X and T clocks are interlocked so that both clocks cannot run concurrently. Whenever a cycle-steal request is detected, the data channel controls inhibit the T clock and start the X clock.

The lines which control the set, increment, and reset of CAR are generated by the cycle-steal sequence controls. These lines are also controlled by the I/O devices attached to the data channel. The I/O device also controls the generation of the CAR check. The CAR check compares the data on the channel data bus to the contents of CAR and generates a check signal if the data does not compare. The I/O device controls these lines by controlling the cycle steal control 0, 1, and 2 lines (CQ40121, F5). Figure 2-25 lists these lines and their functions.

Interval Timer Circuits

- Three timers provide real-time information to the program.
- They are stored in core storage locations 0004, 0005, and 0006.
- Each timer has a permanent time base which can be selected by the customer from those listed in Figure 2-26.
- The time bases are generated by dividing the P-C oscillator frequency by a binary counter.
- The interval timer circuits consist of:
  An 18-position binary counter (Timer Clock)
  Cycle-Steal Request Circuits
  Interrupt Request Circuits
  Timer Cycle Control
  Storage Addressing Circuits
- The relationship and objectives of these circuits are shown on CR40101. A block diagram is shown on CR20101. A timing diagram is on CR70101.

The timers can be started or stopped under program control. Once started they are automatically incremented one count at a time through the cycle stealing facility of the P-C. A count is added each time the assigned time base period is completed.

If the interval-timer word is zero to begin with, it is incremented 65,536 times before it contains all zeros again. In any case, when it is incremented to contain all zeros, an interrupt-request flip-flop is turned on for the respective timer and an interrupt is requested on the level assigned to the timers. (All three timers are on the same interrupt level, assigned by the user.) The timer continues to operate after the zero value has been reached.

The timers, once operating, continue to record time correctly when the P-C is in the Run or Trace mode. A Wait instruction may also be executed by the program without affecting the timer's ability to record time correctly.

Timer Clock

- Eighteen-position binary counter; continually stepped by the B-phase flip-flop.

Cycle Steal Control Line Codes

Line 0 1 2	Action	Incr CAR
0 0 0	B-Reg ⟶ Out Bus	Yes
0 0 1	In Bus ⟶ B-Reg	Yes
0 1 0	B-Reg ⟶ CAR	No
0 1 1	In Bus ⟶ CAR	No
1 0 0	B-Reg ⟶ Out Bus	Yes
1 0 1	B-Reg ⟶ Out Bus	No
1 1 0	CAR Check	Yes
1 1 1	B-Reg ⟶ Out Bus	Yes

12469

Figure 2-25. Cycle Steal Control Lines

Core Storage Cycle Times	Available Time Bases (In Milliseconds)									
2 μsec	.125	.25	.5	1	2	4	8	16	32	64
4 μsec	.25	.5	1	2	4	8	16	32	64	128

17408

Figure 2-26. Interval Timer Time Bases

- The counter is modified to provide a 0.125 millisecond (2 μsec P-C) or 0.25 millisecond (4-μsec P-C) output at the ninth position.

- The ninth through the eighteenth positions provide the clock output of multiples of 0.125 milliseconds.

The first position of the counter that is used as a timer output is the ninth position (Figure 2-27). In a normal binary counter, the output of the ninth position would be 128 μsec in duration. The interval timer clock is a modified binary counter. The on output of the ninth position is connected back to turn on position three and four. The next time the second position goes off, both the third and fourth positions are turned off. This action effectively cuts three microseconds off the duration of the ninth position, making its output the desired 0.125 milliseconds.

Mask Flip-Flops

- Three flip-flops (not labeled in ALDs): for Timers A, B, and C.

- DC reset on.

- Must be off to allow the first-cycle flip-flops to be turned on (CR40101).

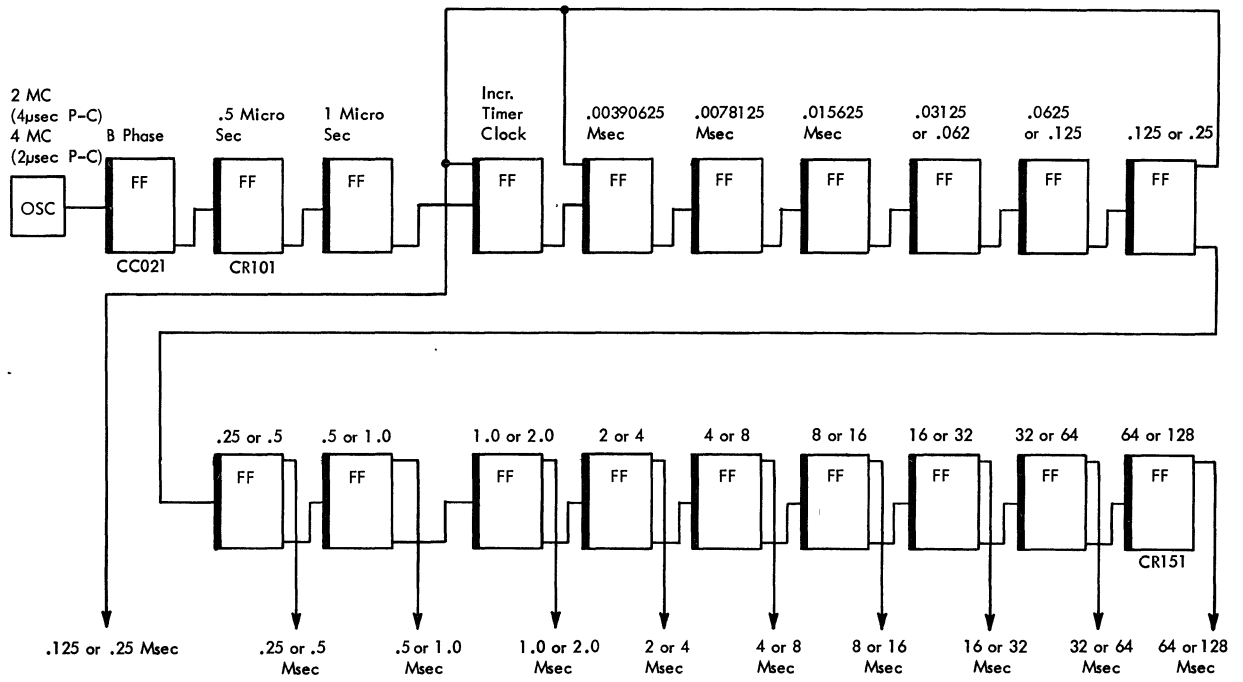
- Turned off by an XIO instruction with a control command.

An XIO instruction, referencing an IOCC with a control function and the interval timer selected, activates the timer-control-function line at time pulse A time. The fall of this line, at T5 time, turns on, or off, the mask flip-flop. If the IOCC address-word bit 0 = 1, the mask flip-flop for timer-A is turned off. If bit 0 = 0, the timer-A mask flip-flop is turned on. Address-word bit 1 and 2 control timers B and C mask flip-flops.

The off condition of the mask flip-flop allows the interval timer clock output to turn on the first cycle flip-flop to advance the timer.

First Cycle Flip-Flops

- Three flip-flops: for timers A, B, and C.



Timings shown are for 4 usec or 2 usec Processor-Controller models.
Shorter time intervals (.125 - 64) are for 2 usec models.

24225-1

Figure 2-27. Interval Timer Clock

- Turned on by the output of the timer clock at the specified interval if the corresponding mask flip-flop is off.
- Turned off at X7 time or dc reset.
- When on, conditions the turn-on of the corresponding cycle-steal-request and interrupt-request flip-flops.

The turn-on input is wired to the assigned output of the timer clock. It is conditioned by the off condition of the corresponding mask flip-flop. When it is turned on by the clock reaching the assigned interval, the cycle-steal-request and the interrupt-request flip-flops are conditioned.

The cycle-steal-request flip-flop initiates a cycle steal to advance the timer word in core storage. This advancement is accomplished by placing the interval-timer word in the I register, incrementing the I register, and placing the word back in core storage. It further conditions the interrupt-request flip-flop to be turned on when the timer word reaches zero, indicated by I register = 0. The cycle-steal-request flip-flop for each timer also generates a core storage address for the timer word.

Operations Monitor

- An independent device; does not use the interval timer or any P-C timing circuits.
- Causes a contact to close when a preset time period is completed.
- Completion of the timeout is normally prevented by execution of a program instruction.
- A separately powered alarm or indicator may be operated by the contact closure.
- Used to notify the process operation when the processor-controller is not executing a predicted sequence of instructions.

The operations monitor is a basic device for the 1800, serviced by a unit address in area zero. The alarm device and its powering are furnished by the customer.

The device has a time-period selector switch on the I/O monitor interface panel with a range of from 5 seconds to 30 seconds in six equal steps. It is possible for the operator to manually disable the operations monitor timing circuit by turning off the operations monitor toggle switch on the programmer's console.

The monitor timing circuit is normally reset by an XIO instruction executed in the 1800. It is the user's responsibility to ensure that this command is executed frequently enough in the program to prevent timeout during normal operation. If the reset command is not given during the selected interval, timeout will occur and the alarm circuit will close. Timeout could be caused by computer hangup or any departure from the predicted instruction sequence in the program. A power failure will close the alarm circuit regardless of the position of the operations monitor toggle switch.

To reset the timing circuit, an XIO instruction is executed with an area code of 0000, a function of control, a unit address of seven, and bit 15 = 1. An indicator is available at the programmer's console to indicate an alarm condition.

Functional Description

The alarm indicator and the customer's alarm device operate when relay 20 drops (Figure 2-28). Relay 20 is held energized by an amplifier that is operated by a special circuit. The special circuit includes a capacitor that charges through a resistor to + 12 volts. The amount of resistance, and therefore the charge time, is selected by the Operations Monitor rotary switch. If the capacitor charges to a "firing" level, relay 20 drops. Normally-closed points of relay 20 light the alarm indicator and complete the customer's alarm circuit.

The Operations Monitor toggle switch in the OFF position prevents the charge of the capacitor and therefore disables the timer. When this switch is on, the XIO-control command must be executed to discharge the capacitor before the charge time elapses.

A description of the Operations Monitor special circuit is in the Appendix.

Channel Interface

- All adapters in the 1800 system share a standard channel interface.
- The channel interface consists of two or three sets of signal and control lines.

The I/O channel interface is routed from the P-C channel control to each I/O adapter in sucession. The signals are carried on two or three I/O channels (1, 2, and 3) to the adapters. Channels 1 and 2, which are standard, consist of three cables (A, B, and C) each, which are routed through the P-C internal adapters, the mixer board (H-gate),

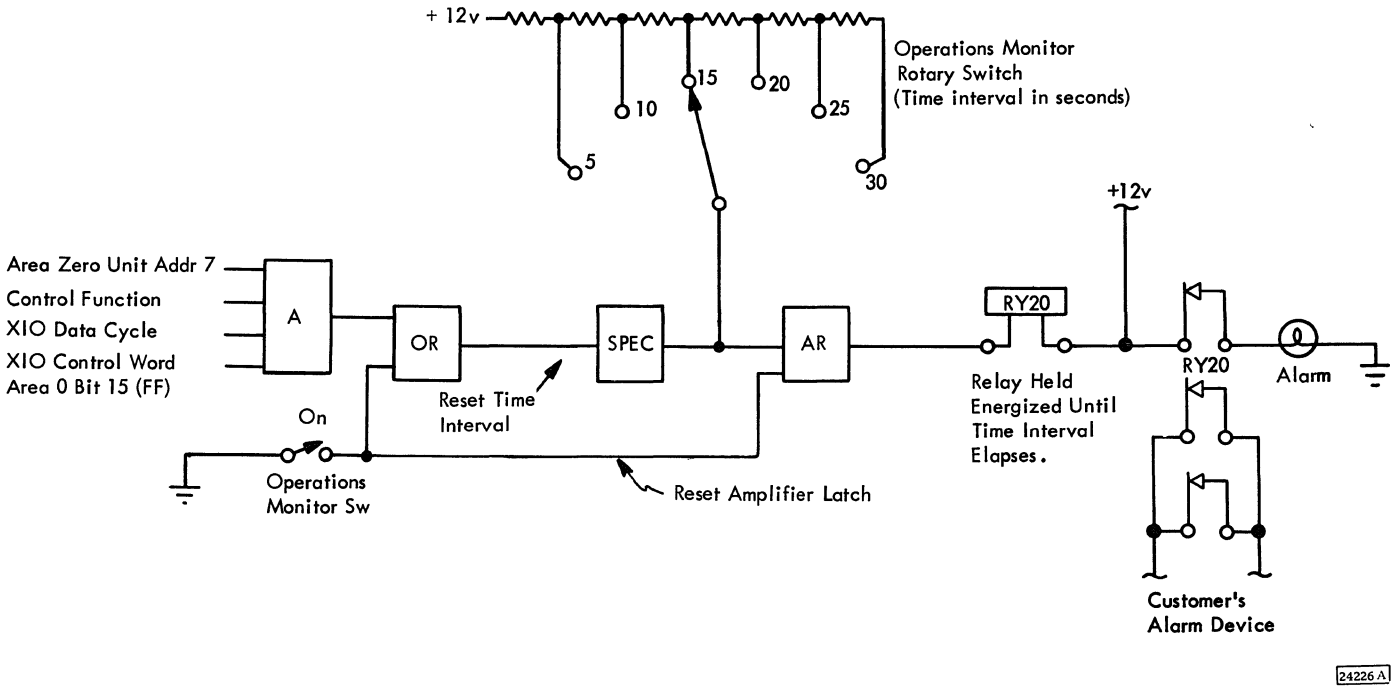


Figure 2-28. Operations Monitor

and to the external adapters. I/O channel 3 (expanded data channels) contains four cables (A, B, C, and D) and is routed to external adapters only.

The A and B cables of each I/O channel contain signal (bus in and bus out) and control lines.

The C cables contain control lines and cycle-steal request and acknowledge lines. Cable 1C contains CS request and acknowledge lines A through E; cable 2C contains CS request and acknowledge lines F through K; cable 3C contains CS request and acknowledge lines L through Q. Cable 3D contains ten CS request and acknowledge lines to provide additional CS request and acknowledge lines to I/O channels 1 and 2 through mixing, and to supplement cable 3C when a Communications Adapter is installed.

CQ10116 shows the prescribed I/O cable routing sequence of cables 1C, 2C, 3C, and 3D for systems with expanded data channels. In this diagram, an example of a CS request line in I/O channels 1 and 2 is routed from the channel control personality wired terminals, through the internal adapters, the mixer board (H-gate) and the tailgate connectors to the external adapters. Cable 3D however, is routed from channel control to the F-gate. Normally cable 3D will be terminated at the F-gate if a Communications Adapter is not installed. The CS acknowledge lines will always be routed the same as the CS request lines. For further information on data channel mixing and assignment wiring refer to BC101.

Signal Cable Termination

- All I/O interface lines must be terminated (CQ10111-CQ10116).
- If no external (outside 1801/1802) adapters are installed, the I/O signal cables are terminated at the Channel Terminator and Mixer Panel (gate H and/or gate F).
- If external adapters are installed, the I/O signal cables are terminated at the last adapter board in the sequence.

In the 1801 or 1802, the six cables terminate at the connector panel in gate H. If the system includes an 1810, the channel interface continues from connectors 1A, 1B, and 1C in gate H to the adapter boards in the 1810. If the system includes an 1826, the channel interface continues from connectors 2A, 2B, and 2C in gate H to adapter boards in the 1826. At the last adapter in the 1810 or 1826, a terminator card is installed on each cable. If the system does not

include an 1810 or 1826, the terminator cards are installed at the cable connectors in gate H of the 1801 or 1802.

The terminator cards supply the +3V "off" level for each line in the interface. Because the "on" level of a line is represented by 0V, the chain must be continuous from the channel control board to the terminator cards. If the terminator cards are installed in an 1810 or an 1826, power must be on at that unit to supply the +3V terminating voltage.

I/O Channel Interface Lines

OUT BUS BITS 0-15: Transmit information (data, I/O device addresses, commands, control information) from the channel to the I/O adapters.

IN BUS BITS 0-15: Transmit information (data, selected I/O device identification, status information, sense data, and interrupt requests) from the adapters to the channel.

PARITY BITS 0-7 and 8-15: These two channel lines transfer parity bits both directions, to an adapter from the P-C or to the P-C from an adapter. Parity for bits 0-7 (lower or left) and parity for bits 8-15 (upper or right) are generated at the B register (CC30101, B4) in the P-C or at the data register in an adapter, such as the 1442 (A5). When data is gated to the out bus, parity bits 0-7 and parity bits 8-15 are gated to the channel. Likewise, when data is gated to the in bus, parity bits 0-7 and parity bits 8-15 are gated to the P-C.

When data is sent to the P-C, parity bits 0-7 and parity bits 8-15 lines are exclusively ORed (C2) to set the parity bit flip-flop (D4) associated with the B register if an even number of data bits are to be stored in cores. The parity bit flip-flop receives a reset pulse if an odd number of bits are to be stored.

From the data received, the adapter generates left and right parity. The adapter-generated parity bits are exclusive-ORed (A5) with those from the P-C. A discrepancy at either exclusive OR sets the 1442 parity check flip-flop (A9).

If a bit is dropped during a data transfer to the 1442 adapter, only the parity check flip-flop in the adapter is set. A programming routine initiates corrective action if the 1442 adapter parity check flip-flop is on.

A bit dropped during a data transfer to the P-C from the 1442 adapter is recognized by setting the P-C parity error flip-flop (D7). This error condition is returned to set the adapter parity check flip-flop (A8) over the CAR check/parity error channel line. The P-C is stopped by a parity error if CHECK STOP is on. This is accomplished by resetting the run flip-flop to off (C7).

CYCLE STEAL REQUEST A-E, F-K, and L-Q: These fifteen lines are used by the device to request a cycle-steal cycle from the processor-controller. The request must be removed from the line by X4 time of the last desired consecutive cycle. Lines A-E are in the 1C cable; lines F-K are in the 2C cable; lines L-Q are in the 3C cable.

CYCLE STEAL ACKNOWLEDGE A-E, F-K, and L-Q: These fifteen lines are bidirectional. During the XIO data cycle, the adapter activates one of these lines to indicate the level to be used and thereby selects the channel address register to be loaded. When a cycle-steal request from an adapter can be serviced by the data channel (cycle-steal level flip-flop turned on), the channel activates the cycle-steal-acknowledge line to signal the adapter to proceed. Lines A-E are in the 1C cable; lines F-K are in the 2C cable; lines L-Q are in the 3C cable.

CYCLE-STEAL CONTROL 0, 1, and 2: These three input lines condition channel circuits to perform various functions depending upon the code of the three lines. See Figure 2-25 for listing of these codes.

INTERRUPT POLL 0-13 and 14-23: These two lines are activated by the channel circuits to gate any interrupt requests onto the in bus. Polling occurs every cycle except when the in bus is being used for data transfer (XIO, cycle steal) and during part of the BSI instruction.

IPL MODE: This line is used during the initial program load sequence. The Program Load key on the programmer's console activates this line. The P-C loads data from the IPL device into the core storage location specified by the I register (normally reset to 0000). Bit 15 on the channel data bus signals a request to store data. If bit 14 is activated at least 250 nanoseconds (ns) before bit 15, the IPL line is deactivated. Channel data bus bits 14 and 15 lines are activated by the IPL device. The P-C then executes the instruction at core location zero.

CC50103 shows the use of this line.

USE-METER GATE; This line indicates the status of the processor-controller to the I/O devices. The

line is activated by a 400 millisecond single-shot at T1 or X1 of every cycle except an interval timer cycle-steal cycle.

TIME PULSE A, B, and C: These three lines are generated by the processor-controller (T) clock and the channel (X) clock (CP111). The lines are used by the I/O adapters to synchronize the device operations to the processor-controller operations. The timings of these three lines are such that any of the eight clock times can be decoded by the adapters.

PARITY ERROR: The parity generated from the B register is utilized in the same manner by the XIO data cycle and the cycle-steal cycle. If the function is an XIO write or cycle-steal-write cycle, the generated parity from the left-half word (Bits 0-7) and right-half word (Bits 8-15) is transmitted with the data word on the out bus. The adapter regenerates parity bits for each of the half-words. The regenerated parity is compared against the parity received with the half words (CC30101, A6). If the parity conditions do not compare, a parity error signal indicates a parity error. This signal sets an error indicator in the receiving adapter during the cycle in which the error occurred (Parity Check flip-flop, 1442, CC30101, A9). When the indicator is off, it assures each device of correct data at the B register on each data transmission. When the indicator is on, it identifies the parity error to a failure within the data cycle of a particular device.

If the function is an XIO read or a cycle-steal read cycle, the left-half odd parity and right-half odd parity is gated onto the in bus with the data word. The left- and right-half parity bits are then exclusively ORed in the P-C (CC30101, D2) and set in the parity flip-flop, (D7), along with the data word in the B register. This data word with parity is then written into core storage. During the write-to-storage, parity is generated on the 16 bits in the B register and is compared with the interface. If the parity does not compare, the parity error circuit indicates to the adapter that a parity error was detected at the B register, and sets the adapter parity check flip-flop (A9). When off, this indicator assures each device that correct data was received by the B register for each data transmission. When on, the indicator identifies the parity error as a failure on the data cycle associated with the particular device.

STORAGE PROTECT VIOLATION: During an XIO (read) instruction or a cycle-steal-request (read) while the data cycle takes place, the word contained in storage is checked for the presence or absence of a storage protection bit. If the bit is absent, execution proceeds without change and the read information is set into the B register from where it is written into storage. If the protect bit is present, the read information is not set into the B register, and the storage-protection-violation line (CC30102, D4) on the I/O interface is conditioned. This signal is detected by the adapter which caused the storage violation and turns on an indicator in that adapter.

XIO CONTROL CYCLE: This line is active during the E1 cycle of an XIO instruction. It is used by the I/O adapters to condition circuits to accept and decode the IOCC control word.

XIO DATA CYCLE: This line is active during the E2 cycle of an XIO instruction with a function of initialize read, initialize write, control, sense device, or sense interrupt. It is active during the E-3 cycle of an XIO instruction with a function of read or write. This line signals the addressed I/O adapter to accept or transfer the data word. During an initialize read or write command, the data cycle (E-2) is used to load the IOCC address word into the specified channel address register (data is transferred during the cycle-steal cycles).

The XIO data-cycle line is also activated by IPL request to implement the initial program load sequence.

RESET: This line is active as long as the console reset key is pressed if the run flip-flop is not on, or, if the power-on reset or alarm-stop reset is active. This line causes a general reset in all I/O adapters.

Chapter 3. Principles of Operation

INSTRUCTION TIME

- Used to read and interpret the instruction at the core storage location specified by the instruction register.
- Decodes the instruction format bit to determine whether the instruction is one or two words in length.
- Decodes the instruction tag bits to determine if the instruction is an indexed instruction.
- Decodes the instruction IA bit to determine if the instruction has an indirect address.
- Instruction cycle 1 (I1) is used by all instructions.
- Instruction Cycle 2 (I2) is used by all double-word-format instructions.
- A third I cycle, indirect addressing cycle (IA), is used by indirect addressing instructions.

In the performance of the stored program instructions, the computer proceeds through instruction time (I-Cycles), and generally through execution time (E-Cycles) for each operation. The functions of instruction time are: (1) read the instruction from core storage, (2) store the instruction in control registers (3) decode the registers to set up the necessary controls for the operation, and (4) develop an effective address.

Instruction word format is described in Chapter 1. The six types of instructions and the machine cycles required for each type are shown in Figure 3-1.

The address portion of the instruction word(s) does not always represent the actual address of the data. To provide programming flexibility and to conserve core storage space, several methods of address modification are available.

The address that references core storage to accomplish the objectives of the instruction is called the effective address. The generation of the effective address depends upon the type of instruction specified. It can be generated during the I1, I2, or IA cycle. Effective address generation is shown in the flow chart on MDM page CC 60101 and is included in the following description of the types of I cycles.

	Cycles Required		
Type of Instruction	I-1	I-2	I-A
Single-Word	X		
Single-Word with Indexing	X		
Double-Word	X	X	
Double-Word with Indexing	X	X	
Double-Word with Indirect Addressing	X	X	X
Double-Word with Indexing and Indirect Addressing	X	X	X

24035

Figure 3-1. Instruction Cycle Requirements

Instruction Cycle 1 (I1)

- Used by all instructions.
- Stores the 16 bits of the first word of the instruction in control registers.
- Decodes the contents of the control registers to determine the operation to be performed.
- Develops the effective address if the instruction is a one-word instruction.
- Reference CC60102

Description

This cycle reads the instruction data from core storage at the address specified by the instruction register. The core storage word is read into the B register, distributed to the various control registers (Figure 3-2), and decoded to indicate the operation to be performed.

There are four major types of I1 cycles.

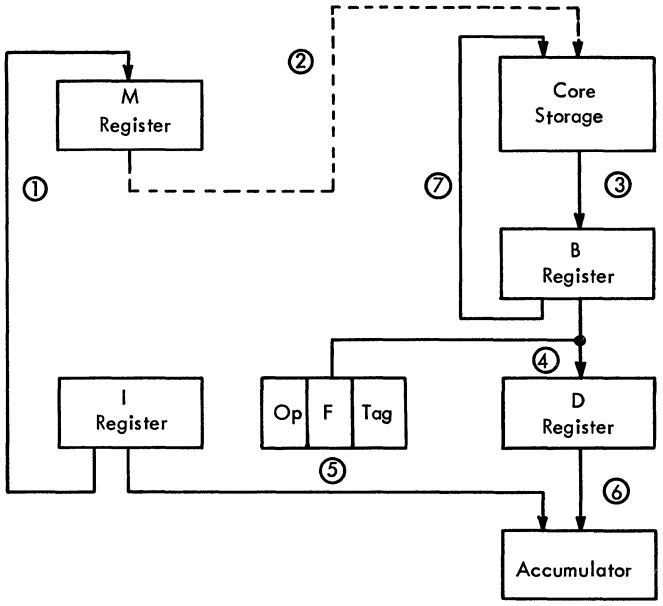
1. I1 used for single-word instructions without indexing (F = 0, T = 00).
2. I1 used for single-word instructions with indexing (F = 0, T $\neq$ 00).
3. I1 used for double-word instructions without indexing (F = 1, T = 00).
4. I1 used for double-word instructions with indexing (F = 1, T $\neq$ 00).

In addition to the functions previously described, each type of I1 cycle performs specific functions to

B Register Bits	Register
0 - 4	Operation Code (OP)
5, 6, 7	Format-TAG (F-T)
8 and 9	Modifier (MOD)
10 - 15	Shift Counter (SC)
14 and 15	Carry-Overflow

24036

Figure 3-2. B Register to Control Register Transfer



1. Transfer instruction address from I to M.
2. Address core storage from M register.
3. Read instruction word from core storage; load into B register.
4. Load operation, format, and tag registers with B register bits 0-7. Load D register with B register bits 8-15.
5. Transfer I register to Accumulator.
6. Add D register to Accumulator. Effective address is now in Accumulator.
7. Write-back instruction word into core storage.

24244

Figure 3-3. I1 Cycle, Single Word, Without Indexing

generate or help generate the effective address. The functions of the four types of I1 cycles are shown in Figures 3-3 through 3-6.

Instruction Cycle 2 (I2)

- Used by all long format instructions.
- Reads the second word (16 bits) of the instruction and loads it into the accumulator.
- CC60104 is a flow chart of the I2 cycle.

The second word in a long format instruction is the effective address unless it is modified by indexing or indirect addressing. Figures 3-5 and 3-6 show the I1 cycle of double word instructions. During the I1 cycle, the I register contents or the contents of an index register are loaded into the accumulator.

If the instruction does not specify indexing, the I2 cycle reads the address from core storage and loads it into the accumulator (Figure 3-7). The I-register contents, loaded into the accumulator during the I1 cycle, are not used.

If the instruction specifies an index register, the contents of that index register were loaded into the accumulator during the I1 cycle. The I2 cycle then reads the address word from core storage and adds it to the index register contents in the accumulator.

Indirect Addressing Cycle (IA)

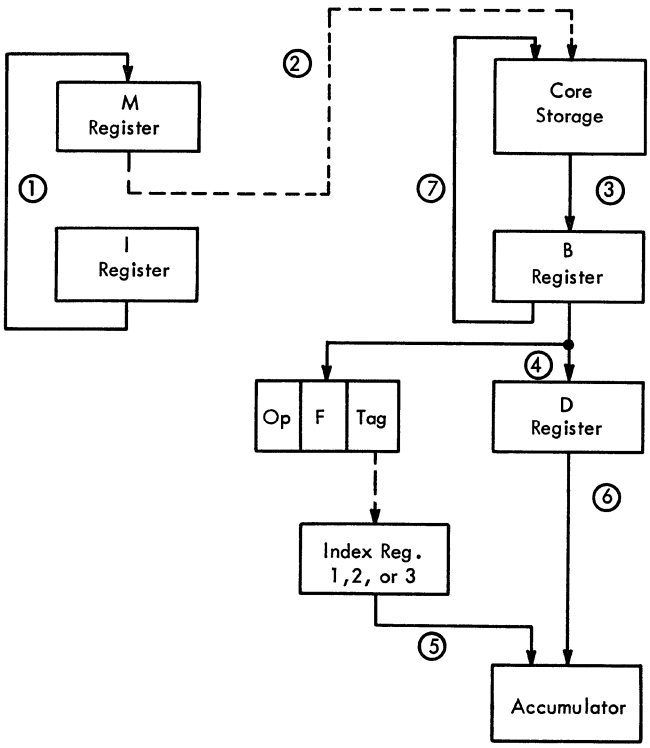
- Used by double-word instructions only.
- Reads a direct address from the core storage location specified by the indirect address placed in the accumulator during the I2 cycle.
- Transfers the direct address to the accumulator to replace the indirect address.
- Reference CC60105.

A direct address can be generally defined as the location of data in core storage. An indirect address can then be defined as the address of a direct address. For most instructions, the effective address that is generated during I1 and I2 cycles is a direct address.

However, the presence of a "one" in the bit 8 position of the instruction indicates that the effective address is really an "indirect" address.

This "indirect" address is the core storage location of a "direct" address.

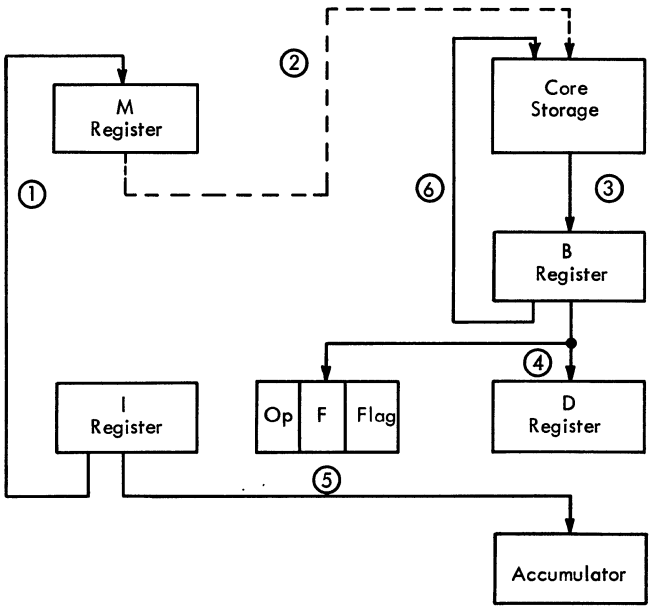
The preceding I2 cycle loaded the indirect address into the accumulator. This indirect address may be the address word (Figure 3-7) or the address word plus the contents of an index register. The IA cycle loads the indirect address into the M register, reads the direct



1. Transfer instruction address from I to M.
2. Address core storage from M register.
3. Read instruction word from core storage; load into B register.
4. Load operation, format, and tag registers with B register bits 0-7. Load D register with B register bits 8-15. Extend displacement sign (bit 8) in D register.
5. Transfer Index register, selected by Tag bits, to Accumulator.
6. Add D register to Accumulator. Effective address is now in Accumulator.
7. Write-back instruction word into core storage.

24245

Figure 3-4. I1 Cycle, Single Word, with Indexing



1. Transfer instruction address from I to M.
2. Address core storage from M register.
3. Read instruction word from core storage; load into B register.
4. Load operation, format, and tag registers with B register bits 0-7. Load D register with B register bits 8-15. Extend displacement sign (bit 8) in D register.
5. Transfer I register to Accumulator.
6. Write-back instruction word into core storage.

D register and Accumulator Contents will not be used. I2 cycle will read address word from core storage and place it in the Accumulator.

24246

Figure 3-5. I1 Cycle, Double Word, Without Indexing

address from the core storage location specified by M, and transfers the direct address to the accumulator via B and D registers (Figure 3-8).

Only one level of indirect addressing is available in the 1800 system. This means that the indirect address of an instruction always selects a direct address, never another indirect address.

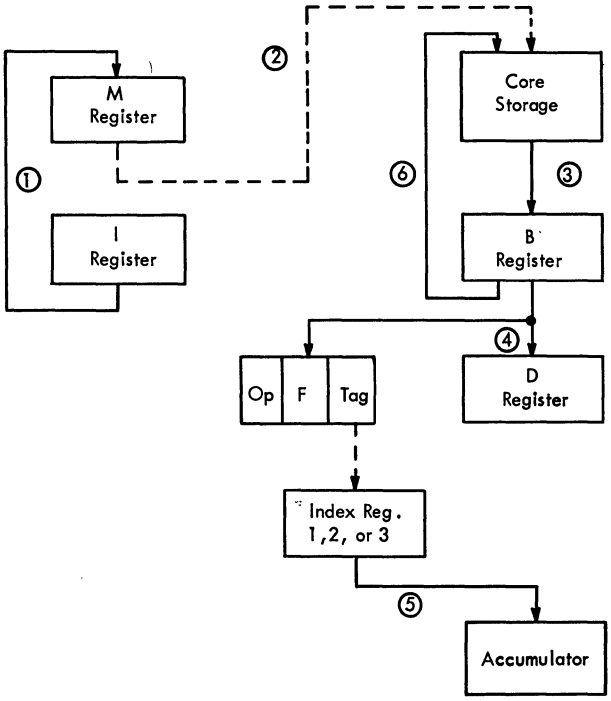
EXECUTION TIME

- Execute the instruction read from core storage and interpreted during the associated instruction time.
- Execution time consists of a number of machine cycles (E-cycles) under the control of E-cycle triggers and the Shift Counter.
- Some instructions do not require any execution time.

The performance of a computer operation is normally divided into two parts, instruction time (I cycles) and execution time (E-cycles).

Each execution time is immediately preceded by its associated instruction time during which the instruction is read from core storage and interpreted.

The function of execution time is to accomplish the objectives of the particular operation specified by the instruction. The required number of machine



1. Transfer instruction address from I to M.
2. Address core storage from M register.
3. Read instruction word from core storage; load into B register.
4. Load operation, format, and tag registers with B register bits 0-7. Load D register with B register bits 8-15. Extend displacement sign (bit 8) in D register.
5. Transfer Index register, selected by Tag bits, to Accumulator.
6. Write-back instruction word into core storage.

D register contents will not be used. I2 cycle will read the address word into the D register and add it to the index word in the accumulator.

24247

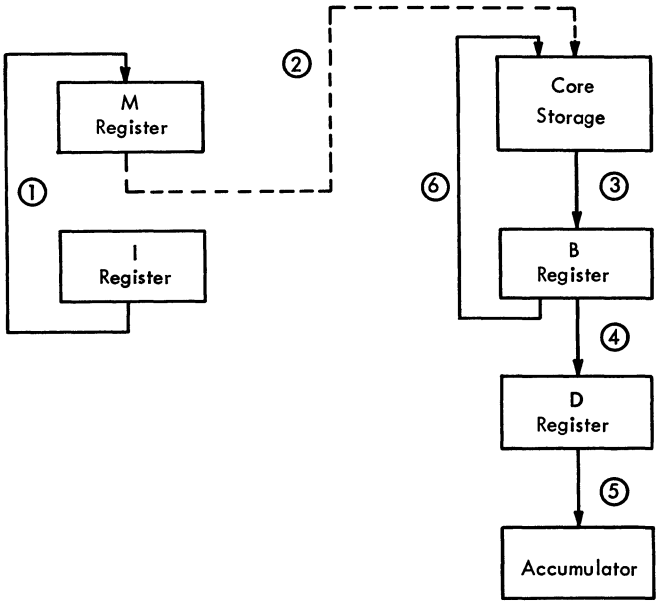
Figure 3-6. I1 Cycle, Double Word, With Indexing

cycles depends upon the specific operation to be performed (Figure 3-9).

The following instructions are complete at the end of their instruction time and require no execution cycles.

1. Wait.
2. Shift Right/Left.
3. Load Status
4. Branch or Skip on Condition.
5. Load index if no index register is specified.

When the execution time for an operation is complete, the computer is directed to enter the instruction time for the next instruction in sequence.



1. Transfer address-word address from I to M.
2. Address core storage from M register.
3. Read address word from core storage; load into B register.
4. Transfer B to D.
5. Transfer D (address word) to Accumulator.
6. Write-back address word into core storage.

24248

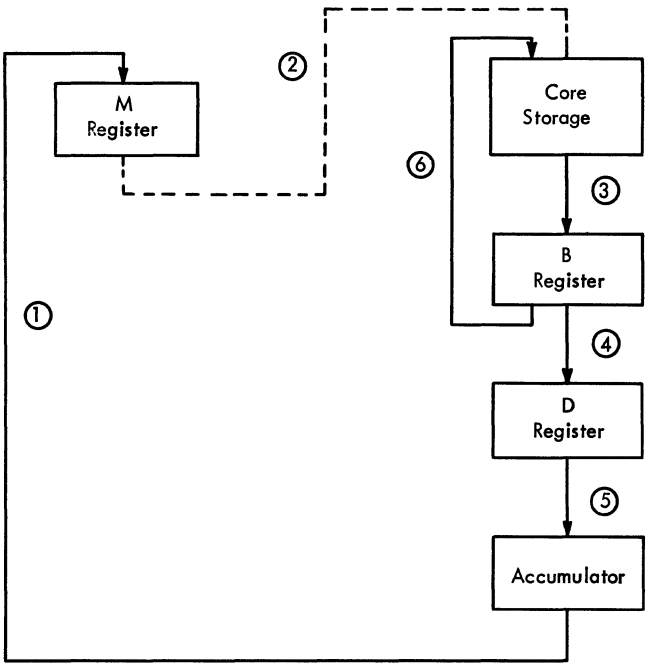
Figure 3-7. I2 Cycle, Double Word, Without Indexing

E-Cycle Flip-Flops

In general, each E-cycle flip-flop controls all of the functions which must be accomplished during the machine cycle for which it is on. At the beginning of the following machine cycle it serves to turn on the next E-cycle flip-flop which is to assume control, and then it is turned off by a T0 clock pulse.

Because identical or similar functions are accomplished during the execution of two or more different computer operations, the E-cycle flip-flops are used with more than one operation, and more than once in any specific operation. For example, the Load Double operation is executed in two execute cycles, using E-cycle flip-flops E1 and E2 (Figure 3-10). The Load Accumulator operation is executed in one execute cycle, using E-cycle flip-flop E1. E1 flip-flop is used with both operations to accomplish a similar function, that of reading a 16-bit word from core storage and loading into the accumulator.

The functions of individual E-cycle flip-flops are described as they are used to accomplish the objectives of the various operations. However, each has normal functions and objectives. These normal functions and



1. Transfer indirect address, loaded into accumulator during I2 cycle, to M register.
2. Address core storage from M register.
3. Read direct address from core storage; load into B register.
4. Transfer B to D.
5. Transfer D to A.
6. Write-back direct address into core storage.

24249

Figure 3-8. IA Cycle

objectives are performed each cycle that the flip-flop is on except during the cycles that they are specifically blocked. These normal functions and objectives are:

T0: Transfer the effective address that was generated during I-cycles from the accumulator to the M register and read core storage. Load core storage word into B register.

T1:
1. Transfer the contents of the temporary accumulator storage register (U) to the accumulator (A). (The contents of A are placed in U at the beginning of instruction time, and are returned to A at the beginning of the first E cycle of an instruction.)
2. Decrement the Shift Counter. The Shift Counter is set during instruction time for the number of cycles required to complete the operation.

T2: Transfer B to D.

OP	CYCLE					
	I-1	I-2	I-A	E-1	E-2	E-3
WAIT	X	-	-	-	-	-
XIO	X	/	/	X	X	/
SLA	X	-	-	-	-	-
SRA	X	-	-	-	-	-
LDS	X	-	-	-	-	-
STS	X	/	/	X	-	-
BSI	X	/	/	X	-	-
BSC	X	/	/	-	-	-
LDX	X	/	/	-	-	-
STX	X	/	/	X	-	-
MDX	X	/	/	/	/	-
A	X	/	/	X	-	-
AD	X	/	/	X	X	-
S	X	/	/	X	-	-
SD	X	/	/	X	X	-
M	X	/	/	X	-	-
D	X	/	/	X	X	-
CMP	X	/	/	X	-	-
DCM	X	/	/	X	X	-
LD	X	/	/	X	-	-
LDD	X	/	/	X	X	-
STO	X	/	/	X	-	-
STD	X	/	/	X	X	-
AND	X	/	/	X	-	-
OR	X	/	/	X	-	-
EOR	X	/	/	X	-	-

X Cycle is used.
- Cycle is not used.
/ Cycle may or may not be used.

24037B

Figure 3-9. Instruction Usage of I and E Cycles

T3: Set Arith Ctrl and add flip-flops if required.

T4:
1. Store the contents of B back into the core storage location specified by M.
2. Depending upon the operation code; transfer, compare, or add D to the contents of the accumulator, or, store or shift the contents of the accumulator.

T5, T6, T7:
1. Continue the compare, shift, or add operation if required.

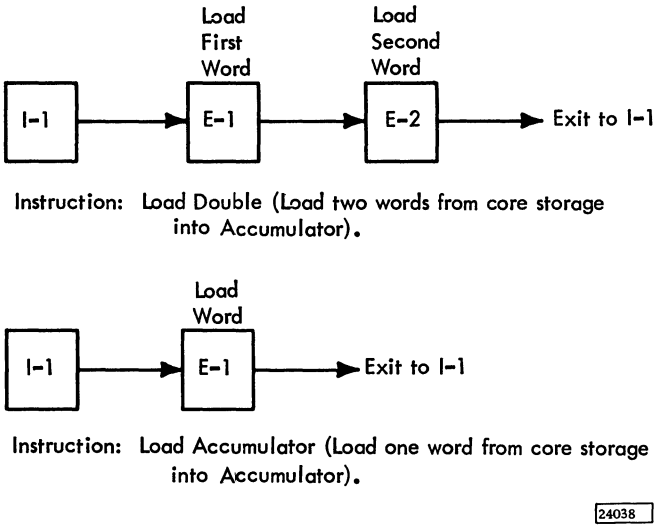


Figure 3-10. Load Accumulator Instructions

2. Extend T7 time if required (if add or subtract and D $\neq$ 0, or if shift and shift counter $\neq$ 0).

The sequential advance from one numbered E-Cycle to another is controlled by operation code gating. At the beginning of each machine cycle, the operation code and the conditions of the operation gate on the next cycle flip-flop. The previous cycle flip-flop is turned off by a T0 clock pulse.

Auxiliary Flip-Flops

Auxiliary flip-flops are used to establish or recognize conditions within the computer which must be considered to properly execute an instruction.

Functions of the most commonly used execution auxiliary flip-flops are described here. These and other auxiliary flip-flops are described in detail in the sections of this manual where they are used in the various computer operations.

Overflow

1. This flip-flop and its associated indicator are turned on by:
   a. An Add, Subtract or Divide operation that produces a result larger than can be accurately represented in the accumulator.
   b. A Load Status instruction that specifies the turn on of the Overflow indicator.
2. This flip-flop and its associated indicator are turned off by:
   a. A Branch or Skip on Condition instruction that tests the Overflow flip-flop.
   b. A Load Status instruction that specifies the turn off of the Overflow indicator.

Carry

1. This flip-flop and its indicator are turned on by:
   a. Arithmetic and shift operations, to indicate a one bit in the high order position of the accumulator or a carry out of the high order position of the accumulator.
   b. A Load Status instruction that specifies the turn on of the Carry flip-flop.
   c. A Shift Left and Count instruction if: BR-1 and BR-2 are on and the Shift Counter is not equal to zero.
2. This flip-flop and its associated indicator are turned off by:
   a. A Branch or Skip on Condition instruction that tests the Carry flip-flop.
   b. A Load Status instruction that specifies the turn off of the Carry flip-flop.
   c. A Shift Left and Count instruction if: BR-1 and BR-2 are on and the Shift Counter is equal to zero.

INSTRUCTION SET

The 1800 instruction set is shown in Figure 3-11. An invalid code (0000) enables the programmer to detect an inadvertent branch to a blank area of core storage. Each instruction falls into one of five classes. Note that the instructions which may be used with indirect addressing are indicated in the Indirect Addressing column. Some instructions perform multiple uses, as specified by their control bits. A more complete breakdown of instructions, including hexadecimal representations, is found in the description of each instruction and in the FEMM.

The following descriptions of the instructions include the instruction formats, the objectives, the effect on the carry and overflow indicators, and the hexadecimal representation for each instruction.

The details of each operation are in the 1800 system Maintenance Diagram Manual. The description for each instruction references the necessary diagram.

Class	Instruction	Indirect Addressing	Mnemonic
Load and Store	Load Accumulator	Yes	LD
	Double Load	Yes	LDD
	Store Accumulator	Yes	STO
	Double Store	Yes	STD
	Load Index	**	LDX
	Store Index	Yes	STX
	Load Status	No	LDS
	Store Status	Yes	STS
Arithmetic	Add	Yes	A
	Double Add	Yes	AD
	Subtract	Yes	S
	Double Subtract	Yes	SD
	Multiply	Yes	M
	Divide	Yes	D
	And	Yes	AND
	Or	Yes	OR
	Exclusive Or	Yes	EOR
Shift	Shift Left Instructions		
	Shift Left Logical (A) *	No	SLA
	Shift Left Logical (AQ)*	No	SLT
	Shift Left and Count (AQ)*	No	SLC
	Shift Left and Count (A)*	No	SLCA
	Shift Right Instructions		
	Shift Right Logical (A)*	No	SRA
	Shift Right Arithmetically (AQ)*	No	SRT
	Rotate Right (AQ)*	No	RTE
Branch	Branch and Store I	Yes	BSI
	Branch or Skip on Condition	Yes	BSC(BOSC)
	Modify Index and Skip	**	MDX
	Wait	No	WAIT
	Compare	Yes	CMP
	Double Compare	Yes	DCM
I/O	Execute I/O	Yes	XIO

* Letters in parentheses indicate registers involved in shift operations.
** See the section for the individual instruction (MDX and LDX)

17151 D

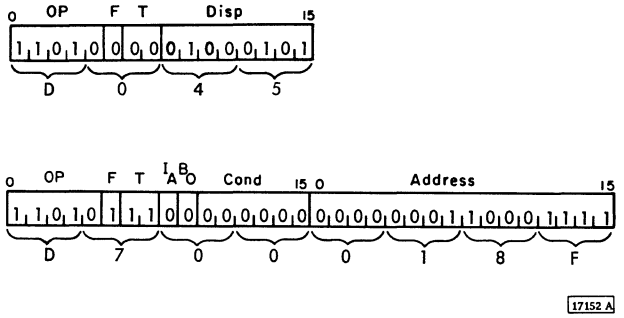
Figure 3-11. Instruction Set

Instruction Format Symbology

Symbols are used to describe the instruction format and objectives. The symbols and their meanings are:

Symbol	Meaning
A	Accumulator
Q	Accumulator Extension
ADDRESS or Addr	Contents of the Address portion of a two-word instruction.
C(xx)	Contents of core storage at the location specified by XX.
DISP	Contents of the Displacement portion of a one-word instruction.
EA	Effective Address
EA + 1	Next higher address from the Effective Address.
I	Contents of the Instruction Register.
XR1	Contents of Index Register 1
XR2	Contents of Index Register 2
XR3	Contents of Index Register 3
X	Hexadecimal value can be 0-F.
*	Used for hexadecimal values that have limits. The limits are given below each group of hexadecimal instructions.

Hexadecimal Representation



17152 A

The hexadecimal version(s) of each instruction is provided with its description. The hexadecimal number is derived by dividing each word into groups of four bits each and assigning a hexadecimal value corresponding to the decimal (BCD) value of each group. The above illustration shows a hexadecimal value for each group of four binary bits. Conversion from hexadecimal to decimal can be obtained from Appendix A. For example, the decimal value of the Address (018F) in the long format instruction is 399.

LOAD AND STORE OPERATIONS

- Load operations normally transfer data from core storage to the machine register specified in the instruction.
- Store operations normally transfer data from the machine register specified in the instruction to core storage.

Load and Store operations are used to transfer data within the system and to set up factors for arithmetic operations.

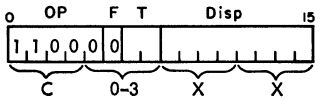
The word "Load" can be interpreted as "transfer data into a register." For example, the instruction, Load Accumulator, means transfer data into the accumulator. The instruction, Load Index Register, means transfer data into an index register.

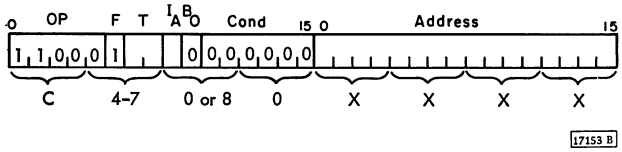
The word "Store" can be interpreted as "transfer data into core storage." For example, the instruction, Store Accumulator, means transfer data out of the accumulator into core storage. The instruction, Store Index Register, means transfer data out of the index register into core storage.

Combinations of these instructions are used to transfer data from one core storage location to another or from one register to another.

The Processor-Controller is an add-to-accumulator machine, therefore, one factor of each arithmetic or logical operation must be loaded into the accumulator before the actual arithmetic or logical instruction is executed.

Load Accumulator (LD)





- Transfers the contents of the core storage location specified by the effective address (EA) into the accumulator (A).
- The contents of the core storage location are unchanged.
- Modifier bit 9 = 1 selects auxiliary storage section of addressed core storage module.
- Reference CC60192.

One–Word Instruction

- Load C(EA) into A.

Hexadecimal Representation	Effective Address
C0XX	I + Disp
C1XX	XR1 + Disp
C2XX	XR2 + Disp
C3XX	XR3 + Disp

Two–Word Instruction, Direct Address

- Load C(EA) into A.

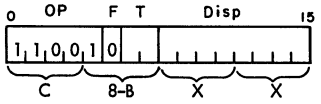
Hexadecimal Representation	Effective Address
C400XXXX	Addr
C500XXXX	Addr + XR1
C600XXXX	Addr + XR2
C700XXXX	Addr + XR3

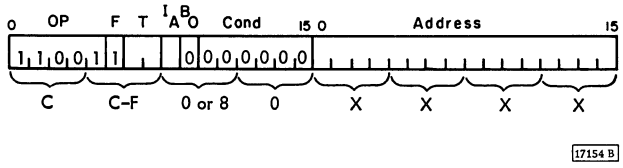
Two–Word Instruction, Indirect Address

- Load C(EA) into A.

Hexadecimal Representation	Effective Address
C480XXXX	C(Addr)
C580XXXX	C(Addr + XR1)
C680XXXX	C(Addr + XR2)
C780XXXX	C(Addr + XR3)

Double Load (LDD)





- Load the contents of core storage specified by the EA and the contents of the next higher core storage location into the accumulator and its extension (Q), respectively.

- This instruction provides double precision load for use with the double precision arithmetic.
- The EA of the instruction must be an even address for correct operation.
- If the EA is odd, the contents of that location will be entered into both the accumulator and its extension.
- The contents of core storage remain unchanged.
- Modifier bit 9 = 1 selects auxiliary storage section of addressed core storage module.
- Reference CC60193.

One–Word Instruction

- Load C(EA and EA + 1) into A and Q.

Hexadecimal Representation	Effective Address
C8XX	I + Disp
C9XX	XR1 + Disp
CAXX	XR2 + Disp
CBXX	XR3 + Disp

Two–Word Instruction, Direct Address

- Load C(EA and EA + 1) into A and Q.

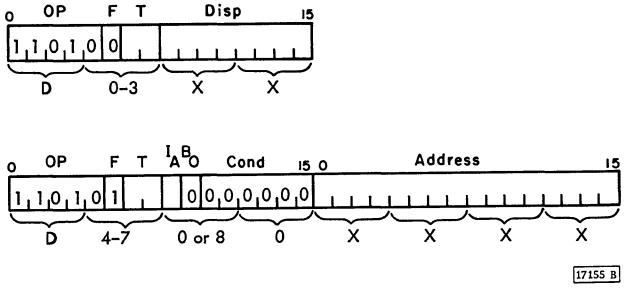
Hexadecimal Representation	Effective Address
CC00XXXX	Addr
CD00XXXX	Addr + XR1
CE00XXXX	Addr + XR2
CF00XXXX	Addr + XR3

Two–Word Instruction, Indirect Address

- Load C(EA and EA + 1) into A and Q.

Hexadecimal Representation	Effective Address
CC80XXXX	C(Addr)
CD80XXXX	C(Addr + XR1)
CE80XXXX	C(Addr + XR2)
CF80XXXX	C(Addr + XR3)

Store Accumulator (STO)



- Stores the contents of the accumulator at the core storage location specified by the effective address.
- The contents of the accumulator are unchanged.
- Modifier bit 9 = 1 selects auxiliary storage section of addressed core storage module.
- Reference CC60194.

One–Word Instruction

- Store A at EA.

Hexadecimal Representation	Effective Address
D0XX	I + Disp
D1XX	XR1 + Disp
D2XX	XR2 + Disp
D3XX	XR3 + Disp

Two–Word Instruction, Direct Address

- Store A at EA.

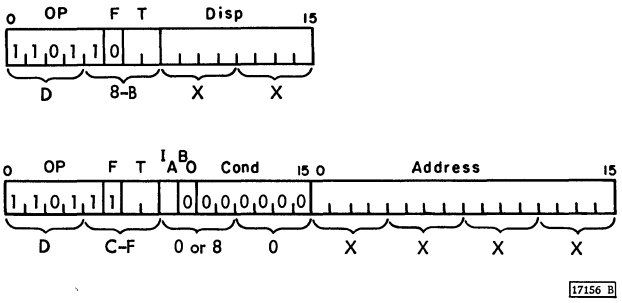
Hexadecimal Representation	Effective Address
D400XXXX	Addr
D500XXXX	Addr + XR1
D600XXXX	Addr + XR2
D700XXXX	Addr + XR3

Two–Word Instruction, Indirect Address

- Store A at EA.

Hexadecimal Representation	Effective Address
D480XXXX	C(Addr)
D580XXXX	C(Addr + XR1)
D680XXXX	C(Addr + XR2)
D780XXXX	C(Addr + XR3)

Double Store (STD)



- Store the contents of the accumulator (A) and its extension (Q) into the core storage locations specified by the effective address (EA) and the EA + 1.
- This instruction provides double precision store for use with double precision arithmetic.
- The EA of this instruction must be an even address for correct operation.
- If the EA is odd, the contents of the accumulator are stored at the EA and the contents of the accumulator extension will not appear in core storage.
- The contents of A and Q remain unchanged.
- Modifier bit 9 = 1 selects auxiliary storage section of addressed core storage module.
- Reference CC60195.

One–Word Instruction

- Store A and Q at EA and EA + 1.

Hexadecimal Representation	Effective Address
D8XX	I + Disp
D9XX	XR1 + Disp
DAXX	XR2 + Disp
DBXX	XR3 + Disp

Two–Word Instruction, Direct Address

- Store A and Q at EA and EA + 1.

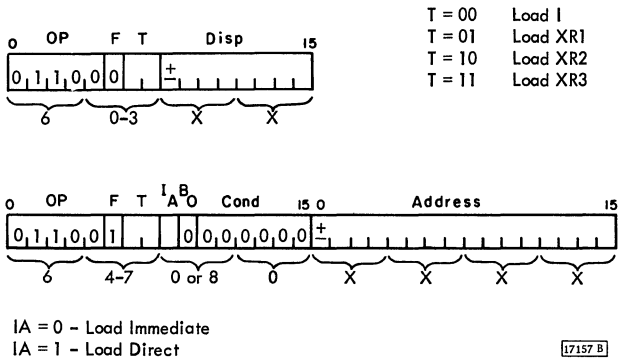
Hexadecimal Representation	Effective Address
DC00XXXX	Addr
DD00XXXX	Addr + XR1
DE00XXXX	Addr + XR2
DF00XXXX	Addr + XR3

Two–Word Instruction, Indirect Address

- Store A and Q at EA and EA + 1.

Hexadecimal Representation	Effective Address
DC80XXXX	C(Addr)
DD80XXXX	C(Addr + XR1)
DE80XXXX	C(Addr + XR2)
DF80 XXXX	C(Addr + XR3)

Load Index (LDX)



- If F = 0, TAG = 00: load I with DISPLACEMENT.
- If F = 0, TAG ≠ 00: load XR with DISPLACEMENT.
- If F = 1, TAG = 00, IA = 0: load I with ADDRESS.
- If F = 1, TAG ≠ 00, IA = 0: load XR with ADDRESS.
- If F = 1, TAG = 00, IA = 1: load I with word at location specified by ADDRESS.
- If F = 1, TAG ≠ 00, IA = 1: load XR with word at location specified by ADDRESS.
- When the DISPLACEMENT is used, the eight high-order positions of the specified register are filled with the value of the sign bit (bit position 8 of instruction) to complete the 16-bit word.
- Reference CC60161.

One–Word Instructions

60XX	Load DISP into the Instruction Register.
61XX	Load DISP into Index Register 1.

62XX Load DISP into Index Register 2
63XX Load DISP into Index Register 3

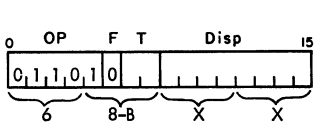
Two—Word Instruction, Direct Addressing

6400XXXX Load Addr into the Instruction Register
6500XXXX Load Addr into Index Register 1
6600XXXX Load Addr into Index Register 2
6700XXXX Load Addr into Index Register 3

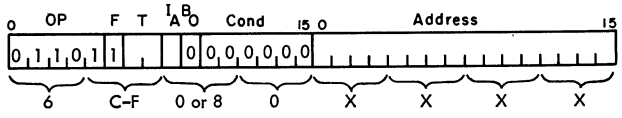
Two-Word Instruction, Indirect Addressing

6480XXXX Load contents of core storage at Addr into Instruction Register
6580XXXX Load contents of core storage at Addr into Index Register 1
6680XXXX Load contents of core storage at Addr into Index Register 2
6780XXXX Load contents of core storage at Addr into Index Register 3

Store Index (STX)



T = 00 Store I
T = 01 Store XR1
T = 10 Store XR2
T = 11 Store XR3



- If TAG = 00: store I at location specified by EA.
- If TAG ≠ 00: store XR at location specified by EA.
- Reference CC60162.

One—Word Instruction

68XX Store I at EA (I+DISP)
69XX Store XR1 at EA (I+DISP)
6AXX Store XR2 at EA (I+DISP)
6BXX Store XR3 at EA (I+DISP)

Two—Word Instruction, Direct Addressing

6C00XXXX Store I at EA (Addr)
6D00XXXX Store XR1 at EA (Addr)
6E00XXXX Store XR2 at EA (Addr)
6F00XXXX Store XR3 at EA (Addr)

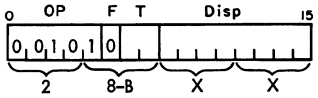
Two—Word Instruction, Indirect Addressing

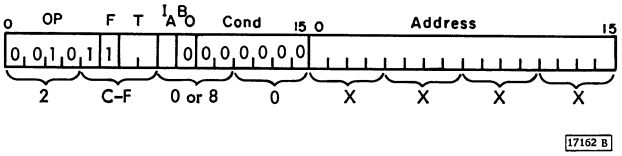
6C80XXXX Store I at EA. EA = C(Addr)
6D80XXXX Store XR1 at EA. EA = C(Addr)
6E80XXXX Store XR2 at EA. EA = C(Addr)
6F80XXXX Store XR3 at EA. EA = C(Addr)

Store Status (STS)

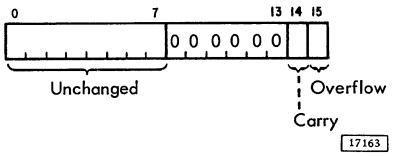
- The Store Status instruction can be used in two ways: store indicator status and store memory protect status.
- Reference CC60142.

Indicator Status





- Store the on/off status of the Carry and Overflow indicators in bits 14 (Carry) and 15 (Overflow) of the word at the effective address (EA).
- Bits 0 through 7 of the word remain unchanged and bits 8 through 13 are reset to zero.
- Carry and Overflow indicators are reset as they are stored.



One—Word Instruction

- Store status of indicators at EA.

Hexadecimal Representation	Effective Address
28XX	I + Disp
29XX	XR1 + Disp
2AXX	XR2 + Disp
2BXX	XR3 + Disp

Two–Word Instruction, Direct Address

- Store status of indicators at EA.

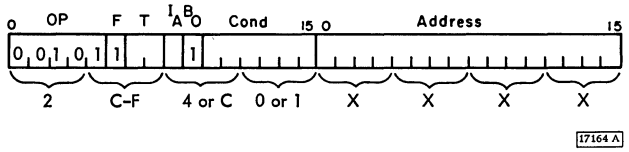
Hexadecimal Representation	Effective Address
2C00XXXX	Addr
2D00XXXX	Addr + XR1
2E00XXXX	Addr + XR2
2F00XXXX	Addr + XR3

Two–Word Instruction, Indirect Address

- Store status of indicators at EA.

Hexadecimal Representation	Effective Address
2C80XXXX	C(Addr)
2D80XXXX	C(Addr + XR1)
2E80XXXX	C(Addr + XR2)
2F80XXXX	C(Addr + XR3)

Storage Protect Status



- Sets or clears the storage protection bit in the specified core storage word if the Write Storage Protection Bit switch is on.

The storage protection bit, which is not part of the 16-bit word, can be altered in any word. The Write Storage Protect Bit switch must be in the Yes position. The storage protect bit is cleared to zero if bit 15 = 0. The storage protect bit is set to one if bit 15 = 1.

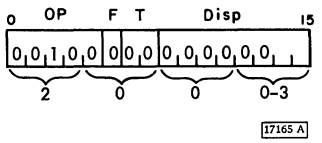
TWO-WORD INSTRUCTION, DIRECT ADDRESSING:

2C40XXXX	Clear storage protect bit at EA (Addr)
2C41XXXX	Write storage protect bit at EA (Addr)
2D40XXXX	Clear storage protect bit at EA (Addr + XR1)
2D41XXXX	Write storage protect bit at EA (Addr + XR1)
2E40XXXX	Clear storage protect bit at EA (Addr + XR2)
2E41XXXX	Write storage protect bit at EA (Addr + XR2)
2F40XXXX	Clear storage protect bit at EA (Addr + XR3)
2F41XXXX	Write storage protect bit at EA (Addr + XR3)

TWO-WORD INSTRUCTION, INDIRECT ADDRESSING:

2CC0XXXX	Clear storage protect bit at EA EA = C(Addr)
2CC1XXXX	Write storage protect bit at EA EA = C(Addr)
2DC0XXXX	Clear storage protect bit at EA EA = C(Addr + XR1)
2DC1XXXX	Write storage protect bit at EA EA = C(Addr + XR1)
2EC0XXXX	Clear storage protect bit at EA EA = C(Addr + XR2)
2EC1XXXX	Write storage protect bit at EA EA = C(Addr + XR2)
2FC0XXXX	Clear storage protect bit at EA EA = C(Addr + XR3)
2FC1XXXX	Write storage protect bit at EA EA = C(Addr + XR3)

Load Status (LDS)



- This instruction uses the single-word format only.
- Load the Carry and Overflow indicators with the on/off status of the bits in positions 14 (Carry) and 15 (Overflow) of the instruction.
- The Carry and Overflow status is normally stored into this instruction by a previous Store Status instruction.
- Core storage is not changed.
- Carry and Overflow indicators are set according to the bits at positions 14 and 15.
- Reference CC60141.

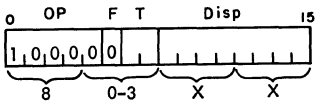
ONE-WORD INSTRUCTION (ONLY):

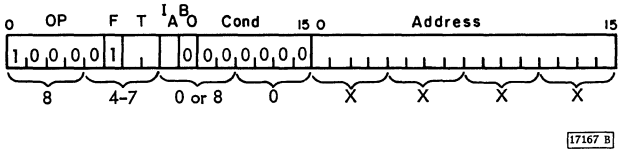
2000	Set CARRY and OVERFLOW indicators OFF
2001	Set OVERFLOW ON and CARRY OFF

2002	Set OVERFLOW OFF and CARRY ON
2003	Set CARRY and OVERFLOW indicator ON

ARITHMETIC INSTRUCTIONS

Add (A)





- Add the 16-bit word specified by EA to the 16-bit word in A.
- Two's complement arithmetic is used; that is, negative operands and/or negative sums will be in two's complement form.
- The sum replaces the contents of A.
- Factor in D register is reduced to zero.
- Core storage remains unchanged.
- The operation of the D register and accumulator, for the add operation, is described in Chapter 2.
- A flow chart and timing diagram for the add instruction are on CC60171.

INDICATORS: The Overflow indicator is turned ON if the magnitude of the sum is too large to be represented in the Accumulator; that is, greater than $+2^{15} - 1$ or less than -2^{15} (this is detected by a resultant carry out of one and only one of the two high-order bit positions of the accumulator). If overflow was previously ON, it is not changed. (Overflow can be reset by testing, or a Load Status or Store Status instruction. See Branch or Skip on Condition instruction.) The Carry indicator is set by a carry out of the high-order bit position of the accumulator.

One–Word Instruction

- Add C(EA) to A.

Hexadecimal Representation	Effective Address
80XX	I + Disp
81XX	XR1 + Disp
82XX	XR2 + Disp
83XX	XR3 + Disp

Two–Word Instruction, Direct Address

- Add C(EA) to A

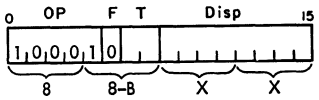
Hexadecimal Representation	Effective Address
8400XXXX	Addr
8500XXXX	Addr + XR1
8600XXXX	Addr + XR2
8700XXXX	Addr + XR3

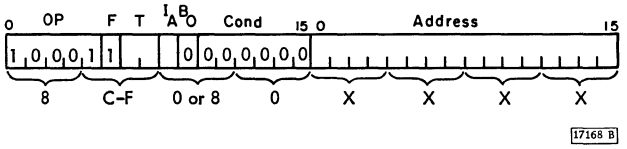
Two–Word Instruction, Indirect Address

- Add C(EA) to A.

Hexadecimal Representation	Effective Address
8480XXXX	C(Addr)
8580XXXX	C(Addr + XR1)
8680XXXX	C(Addr + XR2)
8780XXXX	C(Addr + XR3)

Double Add (AD)





- EA should be even.
- Add the 32-bit word specified by EA and EA + 1 to the 32-bit word in the accumulator and its extension.
- The sum replaces the contents of the accumulator and its extension.
- Core storage remains unchanged.
- Reference CC60172.

This instruction provides double precision addition where the accumulator and its extension are considered as one 32-bit accumulator.

The effective address formed by this instruction must be an even address for correct operation. If EA is odd, the word at the EA location is added to both the accumulator and its extension, and may be added incorrectly into the accumulator.

INDICATORS: When the instruction is completed, the Carry indicator represents the results of this instruction — not previous instructions. The Carry indicator is set ON by detection of a carry out of the high-order position of the accumulator.

The Overflow indicator is turned ON by this instruction if the magnitude of the sum is greater than $+2^{31} - 1$ or less than -2^{31}. If this indicator was ON before the instruction, no change occurs. If OFF, it is turned ON when the magnitude of the number is too large to be represented (this is detected by a carry out of one and only one of the two high-order bits of the accumulator).

One–Word Instruction

- Add C(EA and EA + 1) to A and Q.

Hexadecimal Representation	Effective Address
88XX	I + Disp
89XX	XR1 + Disp
8AXX	XR2 + Disp
8BXX	XR3 + Disp

Two–Word Instruction, Direct Address

- Add C(EA and EA + 1) to A and Q.

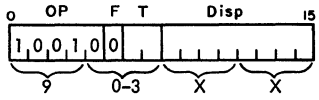
Hexadecimal Representation	Effective Address
8C00XXXX	Addr
8D00XXXX	Addr + XR1
8E00XXXX	Addr + XR2
8F00XXXX	Addr + XR3

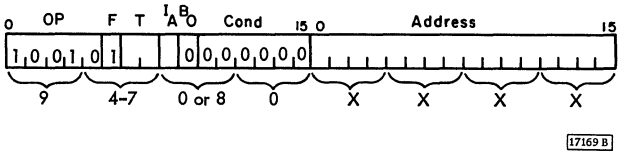
Two–Word Instruction, Indirect Address

- Add C(EA and EA + 1) to A and Q.

Hexadecimal Representation	Effective Address
8C80XXXX	C(Addr)
8D80XXXX	C(Addr + XR1)
8E80XXXX	C(Addr + XR2)
8F80XXXX	C(Addr + XR3)

Subtract (S)





- Subtract the word at the core storage location specified by the effective address from the word in the accumulator.
- The result replaces the contents of the accumulator.
- Two's complement arithmetic is used; that is, both negative operands and negative differences will be two's complement form.
- Core storage remains unchanged.
- Reference CC60171.

INDICATORS: The Overflow indicator is turned ON if the magnitude of the difference is too large to be represented in the accumulator; that is, greater than $+2^{15} - 1$ or less than -2^{15}. If Overflow was previously ON, it is not changed. (Overflow can be reset by testing or a Load or Store Status instruction. See Branch of Skip on Condition Instruction.) This is detected by a borrow from one and only one of the two high-order bit positions of the accumulator. The Carry indicator is set on if an attempt is made to borrow from a nonexistent position by the high order position (A0) of the A register (A0 through A15).

One–Word Instruction

- Subtract C(EA) from A.

Hexadecimal Representation	Effective Address
90XX	I + Disp
91XX	XR1 + Disp
92XX	XR2 + Disp
93XX	XR3 + Disp

Two–Word Instruction, Direct Address

- Subtract C(EA) from A.

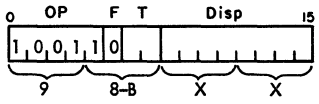
Hexadecimal Representation	Effective Address
9400XXXX	Addr
9500XXXX	Addr + XR1
9600XXXX	Addr + XR2
9700XXXX	Addr + XR3

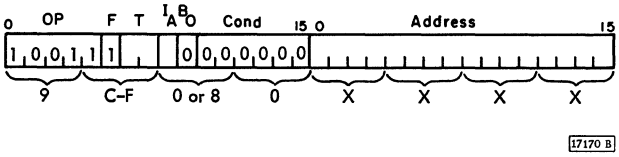
Two–Word Instruction, Indirect Address

- Subtract C(EA) from A.

Hexadecimal Representation	Effective Address
9480XXXX	C(Addr)
9580XXXX	C(Addr + XR1)
9680XXXX	C(Addr + XR2)
9780XXXX	C(Addr + XR3)

Double Subtract (SD)





- EA should be even.
- Subtract the 32-bit word specified by EA and EA + 1 from the 32-bit word in the accumulator and its extension.
- The difference replaces the contents of the accumulator and its extension.
- Core storage remains unchanged.
- Reference CC60172.

The contents of the core storage location specified by the instruction and the next higher memory location are subtracted arithmetically from the contents of the accumulator (A) and its extension (Q). This provides double precision subtraction where the accumulator and its extension are considered as one 32-bit accumulator. The difference replaces the contents of A and Q. Core storage remains unchanged. The effective address formed by the instruction must be an even address for correct operation. If the effective address is odd, the contents of that location are subtracted from both the accumulator and its extension, and may be incorrect in the accumulator.

INDICATORS: The Overflow indicator is turned ON if the magnitude of the difference is too large to be represented in the accumulator (A) and its extension (Q), or more specifically, greater than $+2^{31} - 1$ or less than -2^{31}. This is detected by a borrow from one and only one of the two high-order bit positions of the accumulator. If Overflow was previously ON, it is not changed. (Overflow can be reset by testing or by a Load or Store Status instruction. See Branch or Skip on Condition instruction.) The Carry indicator is set on if an attempt is made to borrow from a nonexistent position by the high order position (A0) of the A register (A0 through A15).

One–Word Instruction

- Subtract C(EA and EA + 1) from A and Q.

Hexadecimal Representation	Effective Address
98XX	I + Disp
99XX	XR1 + Disp
9AXX	XR2 + Disp
9BXX	XR3 + Disp

Two–Word Instruction, Direct Address

- Subtract C(EA and EA + 1) from A and Q.

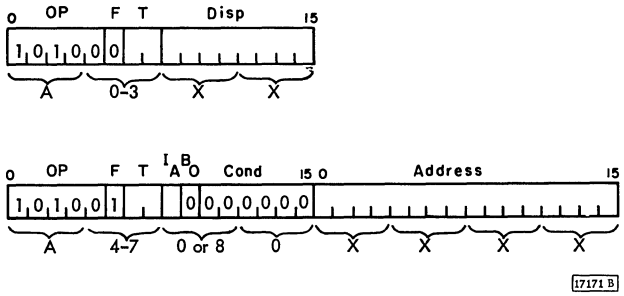
Hexadecimal Representation	Effective Address
9C00XXXX	Addr
9D00XXXX	Addr + XR1
9E00XXXX	Addr + XR2
9F00XXXX	Addr + XR3

Two–Word Instruction, Indirect Address

- Subtract C(EA and EA + 1) from A and Q.

Hexadecimal Representation	Effective Address
9C80XXXX	C(Addr)
9D80XXXX	C(Addr + XR1)
9E80XXXX	C(Addr + XR2)
9F80XXXX	C(Addr + XR3)

Multiply (M)



- Multiply the 16-bit word at the EA by the 16-bit word in the accumulator.
- Place the 32-bit product into the accumulator and its extension.
- Core storage is not changed.
- Overflow and Carry indicators are not changed.
- Reference CC60174.

The word at the core-storage location specified by the effective address (multiplicand) is multiplied algebraically by the word in the accumulator (multiplier). The 32-bit product replaces the contents of the Accumulator (A) and its extension (Q). The most significant bits of the product are in the accumulator. The product is in the double precision format.

Multiplication in the 1800 System depends on the fact that any binary number may be represented by powers of two.

Thus it is not necessary to form the partial product by adding for each bit position. The machine may examine the multiplier (two lowest order bits at a time) to determine when to add the multiplicand, when to subtract, or when to just shift the multiplier.

This system of multiplication permits the 1800 to use fewer add cycles than would be possible with conventional multiplication.

Multiply E2 cycles are entered when an examination of the Q15 bit indicates that it is desired to add or subtract the multiplicand to/from the accumulator partial product.

Multiplier Q14	Multiplier Q15	Previous Operation	New Action	Explanation
0	0	Add	Shift	No Action
0	1	Add	Add, Shift	Single One In String of Zeros
1	0	Add	Shift	No Action
1	1	Add	Sub, Shift	Start String of Ones
0	0	Sub	Add, Shift	End of String of Ones
0	1	Sub	Shift	No Action
1	0	Sub	Sub, Shift	Single Zero In String of Ones
1	1	Sub	Shift	No Action

In the first part of the E2 cycle the Q14 bit is examined to determine whether addition or subtraction is desired.

In the second part of the E2 cycle shifting is continued until the Q15 bit indicates that arithmetic action is again required.

The largest product that can be developed is 2^{30}. This occurs when the multiplier and multiplicand are both the largest negative numbers -2^{15}.

INDICATORS: Neither the Overflow nor the Carry indicators are changed.

Overflow and Carry conditions cannot exist, because multiplying two 16-bit factors cannot produce a result larger than can be represented in the Accumulator and its extention.

One–Word Instruction

- Multiply C(EA) by A.

Hexadecimal Representation	Effective Address
A0XX	I + Disp
A1XX	XR1 + Disp
A2XX	XR2 + Disp
A3XX	XR3 + Disp

Two–Word Instruction, Direct Address

- Multiply C(EA) by A.

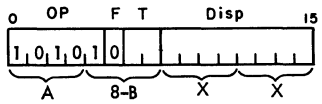
Hexadecimal Representation	Effective Address
A400XXXX	Addr
A500XXXX	Addr + XR1
A600XXXX	Addr + XR2
A700XXXX	Addr + XR3

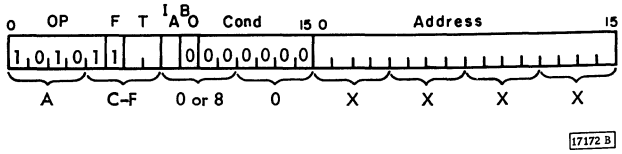
Two–Word Instruction, Indirect Address

- Multiply C(EA) by A.

Hexadecimal Representation	Effective Address
A480XXXX	C(Addr)
A580XXXX	C(Addr + XR1)
A680XXXX	C(Addr + XR2)
A780XXXX	C(Addr + XR3)

Divide (D)





- Divide the 32-bit word in the accumulator and its extension by the 16-bit word at the location specified by the EA.
- Place the quotient in the accumulator.
- Place the remainder in the accumulator extension (Q).
- The sign of the remainder is the same as the sign of the dividend.
- Carry indicator is not changed.
- Reference CC60181.

The word in the accumulator and its extension (a 32-bit double-precision dividend) is divided by the word at the core storage location specified by the effective address. The quotient replaces the contents of the accumulator and the remainder replaces the contents of the accumulator extension. The "sign" of the remainder will be the same as the dividend.

The largest dividend that can correctly be operated upon is $2^{30} + 2^{15} - 1$ if divided by largest negative divisor (-2^{15}).

The division operation is similar to the multiplication operation in that a predetermined number (16) of shift, add, or subtract cycles are taken. Early in each of these sixteen reduction cycles, a comparison of the sign of the divisor and the sign of the accumulator determine whether the operation on this cycle is add or subtract. The same comparison determines whether or not to set a quotient bit. Next, the A and Q are shifted left and the add/subtract operation performed.

Two more cycles follow the 16 reduction cycles. During the 17th cycle both quotient and remainder are tested for the necessity of correction. If the remainder needs correction, it is also accomplished on cycle 17. During the 18th cycle, the accumulator (remainder) and accumulator extension (quotient) are exchanged. If quotient correction is required, it is accomplished on cycle 18, and the operation ends.

This shift-add/subtract procedure is illustrated as follows:

Divide binary 00111001 (57) by 0101 (5).

		Quotient
Shift and sub:	0 0 1 1 1 0 0 1 0 1 0 1	
	+0 0 0 1 0 0 0 1	1
Shift and sub:	0 1 0 1	
	-1 1 1 1 1 1 0 1	0
Shift and add:	0 1 0 1	
	0 0 0 0 0 1 1 1	1
Shift and sub:	0 1 0 1	
	+0 0 0 0 0 0 1 0	1

Answer: Quotient 1011 (11) remainder 0010 (2).

INDICATORS: The Overflow indicator is turned ON if a divide-by-zero operation is attempted or if a quotient-overflow condition is detected. A quotient overflow occurs when the factors are such that the quotient would exceed the range of -2^{15} to $+2^{15} - 1$. An overflow condition leaves the accumulator and its extension in an undefined state.

One–Word Instruction

- Divide A and Q by C(EA).

Hexadecimal Representation	Effective Address
A8XX	I + Disp
A9XX	XR1 + Disp
AAXX	XR2 + Disp
ABXX	XR3 + Disp

Two–Word Instruction, Direct Address

- Divide A and Q by C(EA).

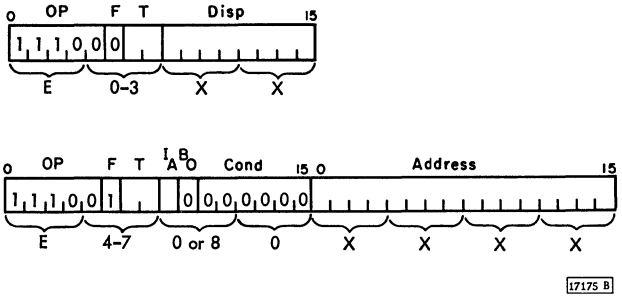
Hexadecimal Representation	Effective Address
AC00XXXX	Addr
AD00XXXX	Addr + XR1
AE00XXXX	Addr + XR2
AF00XXXX	Addr + XR3

Two–Word Instruction, Indirect Address

- Divide A and Q by C(EA).

Hexadecimal Representation	Effective Address
AC80XXXX	C(Addr)
AD80XXXX	C(Addr + XR1)
AE80XXXX	C(Addr + XR2)
AF80XXXX	C(Addr + XR3)

Logical AND (AND)



- AND the word specified by the effective address with the word in the accumulator.
- Positions in the accumulator that have a matching bit in the core storage word are left on; all other accumulator positions are reset.
- Core storage is not changed.
- Modifier bit 9 = 1 selects auxiliary storage section of addressed core storage module.
- Reference CC60191.

DESCRIPTION: The contents of the core storage location specified by the instruction are ANDed bit by bit with the contents of the accumulator. The following table defines the AND operation.

AND

Memory	1	1	0	0
Accum	1	0	1	0
Result	1	0	0	0

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The result replaces the contents of the accumulator. Core storage remains unchanged.

One–Word Instruction

- AND C(EA) with A.

Hexadecimal Representation	Effective Address
E0XX	I + Disp
E1XX	XR1 + Disp
E2XX	XR2 + Disp
E3XX	XR3 + Disp

Two–Word Instruction, Direct Address

- AND C(EA) with A.

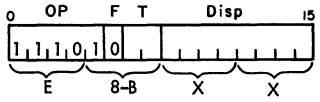
Hexadecimal Representation	Effective Address
E400XXXX	Addr
E500XXXX	Addr + XR1
E600XXXX	Addr + XR2
E700XXXX	Addr + XR3

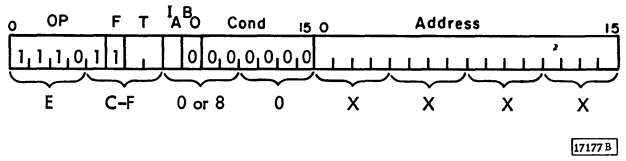
Two–Word Instruction, Indirect Address

- AND C (EA) with A.

Hexadecimal Representation	Effective Address
E480XXXX	C(Addr)
E580XXXX	C(Addr + XR1)
E680XXXX	C(Addr + XR2)
E780XXXX	C(Addr + XR3)

Logical OR (OR)





- OR the word specified by the effective address with the word in the accumulator.
- "Bits" in the accumulator remain on; "bits" in the core storage word turn on associated bits in the accumulator; all other positions remain off.
- Core storage is not changed.
- Modifier bit 9 = 1 selects auxiliary storage section of addressed core storage module.
- Reference CC60191.

DESCRIPTION: The contents of the core storage location specified by the instruction are ORed bit by bit with the contents of the accumulator. The following table defines the OR operation:

OR

Memory	1	1	0	0
Accum	1	0	1	0
Result	1	1	1	0

17178

The result replaces the contents of the accumulator. Core storage remains unchanged.

One–Word Instruction

- OR C(EA) with A.

Hexadecimal Representation	Effective Address
E8XX	I + Disp
E9XX	XR1 + Disp
EAXX	XR2 + Disp
EBXX	XR3 + Disp

Two–Word Instruction, Direct Address

- OR C(EA) with A.

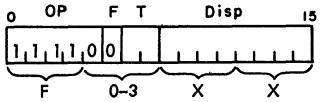
Hexadecimal Representation	Effective Address
EC00XXXX	Addr
ED00XXXX	Addr + XR1
EE00XXXX	Addr + XR2
EF00XXXX	Addr + XR3

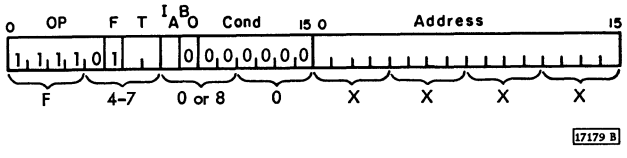
Two–Word Instruction, Indirect Address

- OR C(EA) with A.

Hexadecimal Representation	Effective Address
EC80XXXX	C(Addr)
ED80XXXX	C(Addr + XR1)
EE80XXXX	C(Addr + XR2)
EF80XXXX	C(Addr + XR3)

Logical Exclusive OR (EOR)





- Exclusively OR the word specified by the effective address with the word in the accumulator.
- "Bits" in the accumulator without matching bits in the core storage word, remain on.
- "Bits" in the accumulator, with matching bits in the core storage word, are turned off.
- "Bits" in the core storage word without matching bits in the accumulator word, turn on accumulator bits.
- All other accumulator positions remain off.
- Core storage remains unchanged.
- Modifier bit 9 = 1 selects auxiliary storage section of addressed core storage module.
- Reference CC60191.

DESCRIPTION: The contents of the core storage location specified by the instruction are Exclusive ORed bit by bit with the contents of the accumulator. The following table defines the Exclusive OR operation:

Exclusive OR

Memory	1	1	0	0
Accum	1	0	1	0
Result	0	1	1	0

17180

The result replaces the contents of the accumulator. Core storage remains unchanged.

INDICATORS: The Carry and Overflow indicators are not changed by this operation.

One–Word Instruction

- Exclusively OR C(EA) with A.

Hexadecimal Representation	Effective Address
F0XX	I + Disp
F1XX	XR1 + Disp
F2XX	XR2 + Disp
F3XX	XR3 + Disp

Two–Word Instruction, Direct Address

- Exclusively OR C(EA) with A.

Hexadecimal Representation	Effective Address
F400XXXX	Addr
F500XXXX	Addr + XR1
F600XXXX	Addr + XR2
F700XXXX	Addr + XR3

Two–Word Instruction, Indirect Address

- Exclusively OR C(EA) with A.

Hexadecimal Representation	Effective Address
F480XXXX	C(Addr)
F580XXXX	C(Addr + XR1)
F680XXXX	C(Addr + XR2)
F780XXXX	C(Addr + XR3)

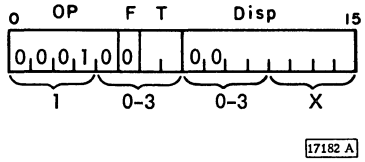
SHIFT OPERATIONS

- All shift instructions are single word format only (F = 0).
- Index registers or displacement specify number of shifts required.
- If the shift count is zero, the instruction performs as a No-Op.
- Shift instructions are divided into classes by Op code and into subclasses by bit positions 8 and 9.

Shift instructions are divided into two major classes: Shift Left and Shift Right. These major classes are defined by the operation code of the instruction. Each of these major classes is divided into subclasses. These subclasses are defined by decoding bits 8 and 9 of the instruction (Figure 3-12).

The location of the shift count is defined by the TAG bits of the instruction (Figure 3-13).

Shift Left Logical A (SLA)



- Shift the accumulator bits to the left the number of positions specified by the shift count.

INSTRUCTION	B8	B9
Shift Left (Code 02)		
Shift Left A	0	0
Shift Left A & Q	1	0
Shift Left and Count A	0	1
Shift Left and Count A & Q	1	1
Shift Right (Code 03)		
Shift Right A	0	0
Shift Right A & Q	1	0
Rotate Right A & Q	1	1

24041

Figure 3-12. Shift Instruction Modifiers

- Fill all vacated positions of the accumulator with zeros.
- Shift bits out of high-order of the accumulator into the Carry indicator.
- Core storage and the accumulator extension are not changed by the instruction.
- If the shift count is zero, the instruction performs a No-Op.
- Reference CC60121.

The accumulator (A) is shifted left the number of spaces specified by the Shift Count. Vacated bit positions are set to zero. Bits leaving the high-order (bit 0 of A) position are shifted into the Carry indicator. (See Indicators below.) The extension (Q) is not affected. Note that bit positions 8 and 9 must be 00.

INDICATORS: The Carry indicator is turned on for each one and off for each zero shifted left from the high-order position of A. The Overflow indicator is unaffected.

Tag	Shift Count Determined By:
00	Low-Order 6 Bits of Disp
01	Low-Order 6 Bits of XR1
10	Low-Order 6 Bits of XR2
11	Low-Order 6 Bits of XR3

17181

Figure 3-13. Shift Count Location

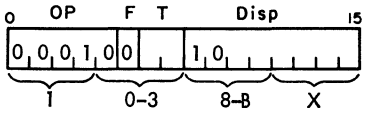
Hexadecimal Representation

One-Word Instructions (Only)

10*X	Contents of A shift left the number of shift counts in DISP.
1100	Contents of A shift left the number of shift counts in XR1.
1200	Contents of A shift left the number of shift counts in XR2.
1300	Contents of A shift left the number of shift counts in XR3.

*The third from the high order position can be 0, 1, 2, or 3, depending on the value of the shift count.

Shift Left Logical A & Q (SLT)



17184 A

- Shift the accumulator and its extension to the left the number of positions specified by the shift count.
- Fill all vacated positions of the accumulator and its extension with zeros.
- Shift bits out of high-order of the accumulator into the Carry indicator.
- Core storage is not changed.
- Reference CC60121.

The accumulator (A) and its extension (Q) are shifted left as a 32-bit double precision register. Vacated bit positions are set to zero. Bits leaving the high-order position (bit position 0 of A) are shifted into the Carry indicator.

INDICATORS: The Carry indicator is turned on for each one and off for each zero shifted left from high-order position of A. The Overflow indicator is unaffected.

Hexadecimal Representation

One-Word Instructions (Only)

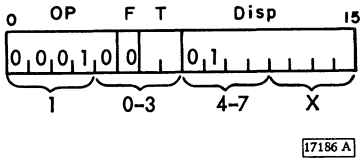
10†X	Contents of A and Q shift left the number of shift counts in DISP.
1180	Contents of A and Q shift left the number of shift counts in XR1.

1280 Contents of A and Q shift left the number of shift counts in XR2.

1380 Contents of A and Q shift left the number of shift counts in XR3.

†The third from the high-order position can be 8, 9, A, or B depending on the value of the shift count.

Shift Left and Count A (SLCA)



- If TAG bits = 00, this instruction performs like a Shift Left A instruction.
- If TAG bits ≠ 00, shift the accumulator to the left, one position at a time.
- Stop shifting when a 1 bit is detected in Bit 0 position of the accumulator if SC ≠ 0 or when the shift counter is decremented to zero.
- Set all vacated positions to zero.
- Carry indicator is turned on at the end of the operation if SC ≠ 0.
- Overflow indicator is not effected.
- Hexadecimal Op codes for this instruction are: 10 (No XR), 11 (XR-1), 12 (XR-2), 13 (XR-3).
- Set shift counter remainder into addressed index register position 8-15.
- Reference CC60121.

A TAG of 00 causes this instruction to be performed as a Shift Left A instruction. A TAG specifying one of the index registers causes the shift count to be transferred from the low-order six bits of the specified register to the shift counter. This count is decremented by one for each position that the contents of the accumulator (A) are shifted to the left. Vacated bit positions are set to zero.

The shift terminates either when an attempt is made to shift a one from the high-order position of A (the "1" remains in the high-order position after the instruction has terminated) or when the shift count has been decremented to zero. The decremented count is then loaded back into the six low-order bit positions of the index register (bits 10-15) and bits 8 and 9 are reset to zero. Bit positions 0-7 of the index register remain unchanged at completion of the instruction. If the shift count is initially zero or if the high order position of the accumulator (Bit 0) is initially a one bit, the instruction performs as a No-Op.

INDICATORS: The Carry indicator will be OFF at the end of the operation if the shift is terminated by the detection of the count reaching zero. The Carry indicator will be ON at the end of the operation if the shift is terminated by the detection of a 1 in bit 0 of the accumulator before the shift count reaches zero. If T = 00 the Carry indicator is set as in Shift Left instruction. The Overflow indicator is unaffected.

SLCA EXAMPLES: For the four examples below, assume the Index register was previously loaded by an LDX instruction. Only the low-order bit positions (10-15) of the Index register (XR) are shown and only the high-order bit positions (0-5) of the accumulator (A) are shown. Those bit positions containing an X can be zero or one.

Example Number	1	2	3	4
XR before SLCA	000011	000100	000101	000110
XR after SLCA	000000	000000	000001	000010
A before SLCA	00001X	00001X	00001X	00001X
A after SLCA	010000	100000	100000	100000
Carry Indicator after SLCA	OFF*	OFF*	ON**	ON**

*If no one bits were contained in the field defined by the Index register (Examples 1 and 2), the program can determine the value of accumulator bit 0 only by testing the accumulator sign. (Carry Indicator is OFF and the Index register is zero.)

**If a one bit was contained in the field defined by the Index register (Examples 3 and 4), the SLCA instruction was terminated when an attempt was made to shift the one out of the high order position, leaving the Carry Indicator ON and the Index register at a non-zero condition. (The one bit remains in the high-order position.)

Hexadecimal Representation

One-Word Instructions (Only)

10#X Contents of A shift left the number of shift counts in DISP.

1140 ≠Contents of A shift left the number of shift counts in XR1.

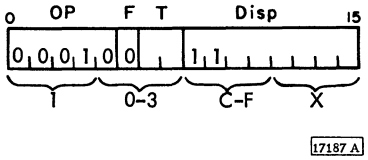
1240 ≠Contents of A shift left the number of shift counts in XR2.

1340 ≠Contents of A shift left the number of shift counts in XR3.

The third from the high-order position can be 4, 5, 6, or 7, depending on the value of the shift count.

≠ These instructions are terminated either when an attempt is made to shift a one bit from the high-order position of the accumulator (with a non-zero shift count remaining) or when the shift count has been decremented to zero.

Shift Left and Count A & Q (SLC)



- If TAG bits = 00, this instruction performs like a Shift Left A & Q instruction.
- If TAG bits ≠ 00, shift the accumulator and its extension to the left one position at a time.
- Bits shifted out of the high-order position of the extension are transferred into the low-order position of the accumulator.
- Stop shifting when shift counter is decremented to zero or when a "one" bit is detected in the high-order position of the accumulator.
- Set shift counter remainder into addressed index register.
- Set all vacated positions to zero.
- Carry indicator is turned on at the end of the operation if SC ≠ 0.
- Overflow indicator is not affected.
- Reference CC60121.

This instruction is the same as the Shift Left and Count A except that both the accumulator (A) and its extension (Q) are shifted. Bit position 0 of Q is shifted into bit position 15 of A and vacated positions at the right of Q are set to zero.

INDICATORS: The Carry indicator will be OFF at the end of the operation if the shift is terminated by the detection of the count reaching zero. The Carry indicator will be ON at the end of the operation if the shift is terminated by the detection of a 1 in the bit zero position of the accumulator before the shift count reaches zero. If T = 00 the Carry indicator is set as in Shift Left instruction.

The Overflow indicator is unaffected.

Hexadecimal Representation

One-Word Instructions (Only)

10*X Contents of A and Q shift left the number of shift counts in DISP.

11C0 **Contents of A and Q shift left the number of shift counts in XR1.

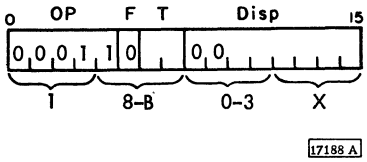
12C0 **Contents of A and Q shift left the number of shift counts in XR2.

13C0 Contents of A and Q shift left the number of shift counts in XR3.

*The third from the high-order position can be C, D, E, or F, depending on the value of the shift count.

**These instructions are terminated either when an attempt is made to shift a one bit from the high-order position of the accumulator (with a non-zero shift count remaining) or when the shift count has been decremented to zero.

Shift Right Logical A (SRA)



- Shift the accumulator bits to the right the number of positions specified by the shift count.
- Fill all vacated positions of the accumulator with zeros.
- Low-order bits of the accumulator are lost.
- Core storage and the accumulator extension are not changed by this instruction.
- Reference CC60131.

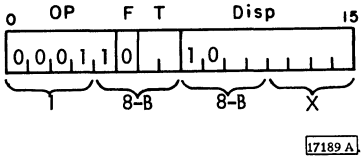
Hexadecimal Representation

One-Word Instructions (Only)

18*X	Contents of A shift right the number of shift counts in DISP.
1900	Contents of A shift right the number of shift counts in XR1.
1A00	Contents of A shift right the number of shift counts in XR2.
1B00	Contents of A shift right the number of shift counts in XR3.

*The third from the high-order position can be 0, 1, 2, or 3, depending on the value of the shift count.

Shift Right A & Q (SRT)



- Shift the accumulator and its extension to the right the number of positions specified by the shift count.
- The accumulator and extension are shifted right as a 32-bit double precision register.
- Fill all vacated positions with the sign of the accumulator (1 bit if negative, 0 bit if positive).
- Low-order bits of the accumulator extension are lost.
- Core storage is not changed.
- Reference CC60131.

Hexadecimal Representation

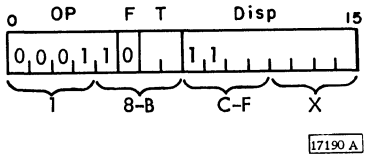
One-Word Instruction (Only)

18†X	Contents of A and Q shift right the number of shift counts in DISP.
1980	Contents of A and Q shift right the number of shift counts in XR1.
1A80	Contents of A and Q shift right the number of shift counts in XR2.
1B80	Contents of A and Q shift right the number of shift counts in XR3.

†The third from the high-order position can be 8, 9, A, or B, depending on the value of the shift count.

Rotate Right A & Q (RTE)

- Rotate the accumulator and its extension to the right.



- Bits from position 15 of the accumulator are transferred to position 0 of the extension.
- Bits from position 15 of the extension are transferred to position 0 of the accumulator.
- Carry and Overflow indicators are unaffected.
- Core storage is not changed.
- If SC = 16 or 48, exchange A and Q.
- Reference CC60131.

DESCRIPTION: The accumulator and extension are rotated to the right as a 32-bit double precision register the number of bit positions specified by the shift count. Bit position 15 of the extension is linked to bit position 0 of the accumulator to form a continuous loop so that the high-order positions of the accumulator pick up the bits dropped from the low-order position of the extension.

Hexadecimal Representation

One Word Instruction (Only)

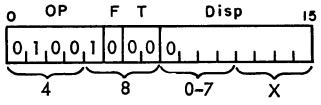
18#X	Contents of A and Q rotate right the number of counts in DISP.
19C0	Contents of A and Q rotate right the number of counts in XR1.
1AC0	Contents of A and Q rotate right the number of counts in XR2.
1BC0	Contents of A and Q rotate right the number of counts in XR3.

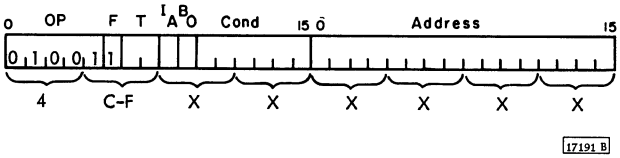
#The third from the high-order position can be C, D, E, or F, depending on the value of the shift count.

BRANCH AND SKIP OPERATIONS

- Branch instructions are used in a program to permit alteration of the sequential execution of the program.

Branch or Skip on Condition (BSC or BOSC)





- If F = 0: skip next sequential instruction if any specified condition is present.
- If F = 1: branch to the instruction at the location specified by the ADDRESS if no specified condition is present.
- Must be sequentially followed by a single-word instruction if this instruction is a single word.
- Core storage and accumulator extension are not changed by this instruction.
- Overflow indicator is reset if tested.
- Carry indicator is not reset.
- Accumulator is not changed by testing.
- Six conditions associated with the accumulator can be tested.
- Reference CC60152.

There are six testable conditions associated with the accumulator. These conditions may be tested by the desired bit pattern in the DISPLACEMENT of the instruction.

The six accumulator conditions that can be tested are shown by bit position in Figure 3-14.

When F = 0, the instruction executed is a Skip on Condition when one or more of the conditions specified is true. This enables the program to skip over the next one word instruction. If none of the conditions specified are true, the next instruction in sequence is executed.

Displacement Bit Position	Condition Tested
15	Overflow Indicator Off
14	Carry Indicator Off
13	Accumulator Even
12	Accumulator Plus (>0)
11	Accumulator Negative (<0)
10	Accumulator = Zero

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Figure 3-14. Test Conditions

When F = 1, the instruction executed is a Branch to the Effective Address (EA) when none of the conditions specified are true. If any one of the conditions specified in bit positions 10-15 is true, the next instruction in sequence is executed. Examples are shown in Figure 3-15.

The EA is calculated as follows:

F = 1 IA = 0 T = 00 EA = ADDR
T = 01 EA = XR1 + ADDR
T = 10 EA = XR2 + ADDR
T = 11 EA = XR3 + ADDR

Bit Positions: / ACC Conditions:	10 Zero	11 Minus	12 Plus	13 Even	Skip (F = 0)	Branch (F=1)
Test Conditions	1	1	1	0	Always	Never
	0	0	0	0	Never	Always
	0	0	1	0	Plus	Not Plus
	1	1	0	0	Not Plus	Plus
	0	1	0	0	Minus	Not Minus
	1	0	1	0	Not Minus	Minus
	1	0	0	0	Zero	Not Zero
	0	1	1	0	Not Zero	Zero
	0	0	0	1	Even	Odd
	0	0	1	1	Even or Plus	Odd and Minus
	0	1	0	1	Even or Minus	Odd and Plus

Notes: 1. ACC Zero IS NOT a plus condition.
2. Skip and Branch columns specify action or ACC condition required for Skip or Branch.
3. Skip on Odd condition, Carry ON, or Overflow ON are not possible.

17441 A

Figure 3-15. BSC Examples

When the IA bit is equal to a one (IA = 1), this instruction enables the program to return to a mainline program from a program subroutine of interrupt routine. This is accomplished by making the EA of this instruction identical to the EA of a previously executed Branch and Store Instruction Register (BSI) instruction. The EA as calculated below is loaded into the Instruction register.

F = 1	IA = 1	T = 00	EA = C(Addr)
		T = 01	EA = C(Addr + XR1)
		T = 10	EA = C(Addr + XR2)
		T = 11	EA = C(Addr + XR3)

PROGRAMMING NOTE: When an interrupt request has been detected by a priority level, the program is directed to service the request by interrupting. During the servicing, all interrupt requests of equal or lower status are effectively delayed from interrupting while the servicing of the higher priority is in progress. However, if a request is detected for a higher priority level than is presently in progress, the program is immediately interrupted again. This is frequently called Nesting of Interrupts.

At the completion of servicing any level of interrupt, it is necessary to signal the priority hardware to reset the priority-status of the highest level that is on. This reset permits lower priority requests that may have been temporarily inhibited but recorded to be accepted once again by the P-C. This is effected by making Bit 9 = 1 in the BSC instruction. A BSC instruction with Bit 9 = 1 is called a Branch Out of Interrrupts (BOSC). This programmed recognition of waiting interrupts should not be confused with a normal subroutine linkage back to a mainline program in which Bit 9 should be set to zero.

The BSC is a conditional instruction. When Bit 9 = 1, the reset of the interrupt level occurs only if the Branch or Skip occurs. If the Branch or Skip does not occur, the interrupt level is not reset.

INDICATORS: The Overflow indicator is reset when tested. The Carry indicator is not reset by testing. The contents of the accumulator are not changed by testing. If no conditions are specified, a Skip does not occur on the Skip instruction (F = 0) or a branch does occur on the Branch instruction (F = 1).

One–Word Instruction

48*X Skip the next one-word instruction if any specified condition is sensed.

*The third from the high-order position can be 0, 1, 2, or 3 (BSC) or 4, 5, 6, or 7 (BOSC), depending on the conditions being tested.

Two–Word Instruction, Direct Addressing

- Branch to EA on NO condition.

Hexadecimal Representation	Effective Address
4C#XXXXX	Addr
4D#XXXXX	Addr + XR1
4E#XXXXX	Addr + XR2
4F#XXXXX	Addr + XR3

#The third from the high-order position can be 0, 1, 2, or 3 (BSC) or 4, 5, 6, or 7 (BOSC). These hexadecimal values are determined by the conditions being tested.

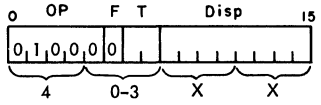
Two–Word Instruction, Indirect Addressing

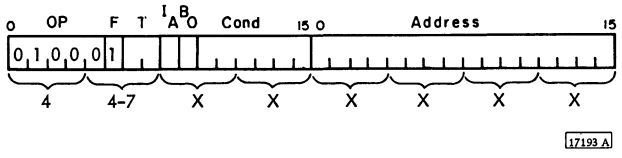
- Branch to EA on NO condition.

Hexadecimal Representation	Effective Address
4C≠XXXXX	C(Addr)
4D≠XXXXX	C(Addr + XR1)
4E≠XXXXX	C(Addr + XR2)
4F≠XXXXX	C(Addr + XR3)

≠The third from the high-order position can be 8, 9, A, B (BSC) or C, D, E, or F (BOSC). These hexadecimal values are determined by the conditions being tested.

Branch and Store Instruction Register (BSI)

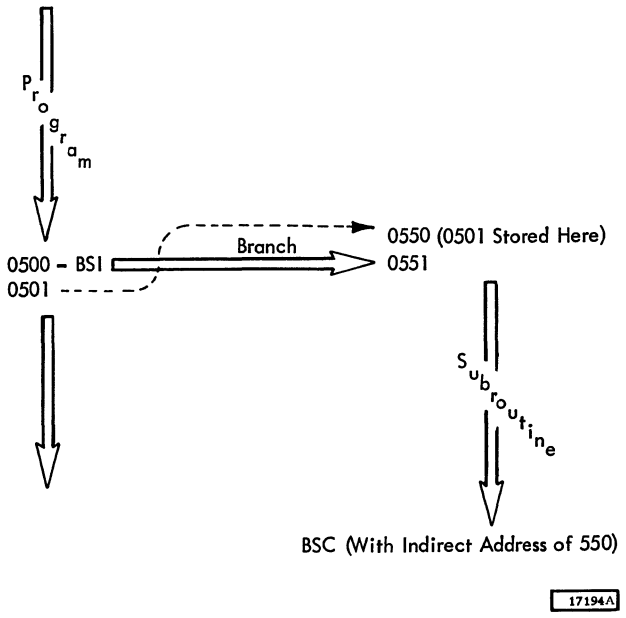




- Store contents of Instruction register at the core storage location specified by the effective address.
- Branch by setting Instruction register to the value of the effective address plus one.

- If F = 0, branch and store functions are unconditional.
- If F = 1, branch and store functions are performed only if none of the BSC skip conditions (Figure 3-15) specified by the displacement are present.
- Overflow indicator is reset if tested.
- Carry indicator is not reset.
- Accumulator is not changed by testing.
- Six conditions associated with the accumulator can be tested.
- Reference CC60151.

DESCRIPTION: When F = 0 (one word format), the contents of the Instruction register are stored in the core storage location specified by the effective address. The stored address is that of the next instruction in the normal sequence. The Instruction register is then set to the value of the effective address plus one, and program execution proceeds from that point. For example, a BSI instruction located at core storage address 0500, with an effective address of 0550, would store the address 0501 at location 0550 and then branch to 551.



A BSC instruction with an IA bit of one and an Address of 0550 would be used to return from the subroutine.

When F = 1 (two word instruction format), the above function is conditionally executed depending on the condition bits specified in the displacement. These accumulator condition bits are defined in the preceding BSC instruction. If any one of the conditions specified is true, the previously explained branch does not occur. Instead, the next instruction in sequence is performed. If none of the conditions are true, the Instruction register is stored at the effective address (specified by the ADDRESS) and the branch is to EA + 1.

Internal, CE, and external level interrupts are suppressed for the first instruction following a BSI instruction. Therefore, the Mask register (See Interrupt section) may be set without the possibility of an interrupt immediately following the BSI instruction.

INDICATORS: When F = 0, the status of the indicators is unchanged. When F = 1, the Overflow indicator is reset if tested.

One–Word Instruction

- Store I at EA; branch to EA + 1.

Hexadecimal Representation	Effective Address
40XX	I + Disp
41XX	XR1 + Disp
42XX	XR2 + Disp
43XX	XR3 + Disp

Two–Word Instruction, Direct Address

- If no condition is true, store I at EA and branch to EA + 1.

Hexadecimal Representation	Effective Address
44*XXXXX	Addr
45*XXXXX	Addr + XR1
46*XXXXX	Addr + XR2
47*XXXXX	Addr + XR3

*The third from the high-order position can be 0, 1, 2, or 3, depending on the conditions being tested.

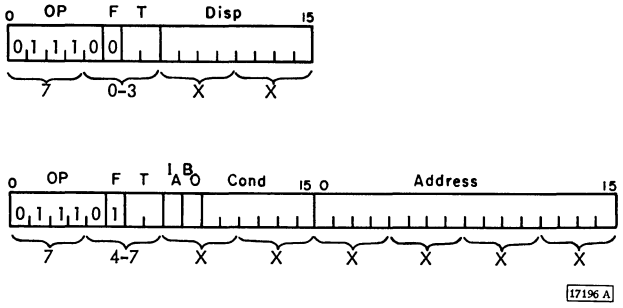
Two–Word Instruction, Indirect Address

- If no condition is true, store I at EA and branch to EA + 1.

Hexadecimal Representation	Effective Address
44#XXXXX	C(Addr)
45#XXXXX	C(Addr + XR1)
46#XXXXX	C(Addr + XR2)
47#XXXXX	C(Addr + XR3)

#The third from the high-order position can be 8, 9, A, or B, depending on the conditions being tested.

Modify Index and Skip (MDX)



- Modifies the I register, a specified Index register (XR), or a core storage word.
- The modifying factor can be the Displacement, the Address word, or a specified core storage word.
- The following table summarizes the MDX functions:

Format	Tag	IA	Add	Skip
0	00	-	Displ. to I	Unconditional
0	01		Displ. to XR-1	Conditional *
0	10	-	Displ. to XR-2	
0	11	-	Displ to XR-3	
1	00	-	Displ. to Contents of core storage (specified by Address word).	
1	01	0	Address word to XR-1	
1	10	0	Address word to XR-2	
1	11	0	Address word to XR-3	
1	01	1	Contents of core storage specified by Addr. word to XR-1	
1	10	1	C (Addr.) to XR-2	
1	11	1	C (Addr.) to XR-3	

* Skip following MDX if modified factor reaches zero or changes sign while being modified.

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MDX, F = 0, Tag = 0

- Add displacement to I register.
- Place modified factor back into I register to cause an unconditional skip.
- Requires only one cycle (I1).
- Reference CC60163.

The displacement is loaded into the D register, the contents of the I register are loaded into the accumulator, and the factors are added; all as normal I1 cycle functions. The Branch-1 and Branch-2 flip-flops cause the modified factor to be transferred from the accumulator to the M register and then to the I register. The next I1 cycle will use this modified I register thereby effecting an unconditional branch.

MDX, F = 0, Tax ≠00

- Add Displacement to specified Index register.
- Place modified factor back into XR.
- Skip the next instruction location if XR reached zero or changed sign while being modified.
- Requires only one cycle (I1).
- Reference CC60163.

The Displacement is loaded into the D register, the specified XR is loaded into the accumulator, and the two factors are added; all normal I1 cycle functions. Branch-1 and Branch-2 causes the modified factor to be transferred back into the XR. If during the modification the accumulator equals zero or changes sign (A0 ≠ B0), the I register is advanced one to skip the next instruction word in sequence.

MDX, F = 1, Tag = 00

- Add Displacement to the contents of core storage at the location specified by the address word of the MDX instruction.
- Store the modified word back into core storage.
- Skip the next instruction word if the modified word reaches zero or changes sign.
- Reference CC60164.

A normal I1 cycle is taken except that the add-to-storage-interlock and the Mod-8-bit flip-flops are turned on.

An I2 cycle reads the address word and loads it into the accumulator. Add-to-storage causes I and M to be exchanged to save the MDX address. Add-to-storage-interlock is turned off.

An IA cycle is taken because the Mod-8-bit flip-flop was forced on. The address word, loaded into A during I2 cycle is transferred to the M register to address the core storage word to be modified. The core storage word is loaded into the accumulator and the add-to-storage-interlock flip-flop is turned on again.

An E1 cycle is taken. I and M are again exchanged to restore the MDX instruction address to the M register. The Displacement is read from core storage, loaded into the D register, and added to the core storage word that was loaded into the accumulator during IA cycle.

E2 cycle: I and M are exchanged, I is incremented if Accum = 0 or if A0 ≠ B0 as determined by comparison with the B0 latch. The modified factor in the accumulator is transferred to the B register and stored into core storage at its original location (EA + 1). The I register is incremented for the next instruction.

MDX, F = 1, Tag ≠ 00

- If bit 8 (IA) of the MDX instruction word equal zero, add the address word to the contents of the specified XR.
- If bit 8 (IA) of the MDX instruction word equal one, add the contents at core storage location specified by the address word to the contents of the specified XR.
- Store the modified word back into the specified XR.
- Skip the next instruction word if the modified word reaches zero or changes sign.
- Reference CC60166.

Normal I1 and I2 cycles load the address word into the D register. If bit 8 of the MDX instruction word is a one, an IA cycle is taken to load the D register with the core storage word at the location specified by the address word. During the I2 cycle, or IA if taken, the contents of the specified XR are loaded into the accumulator and the two factors are added. Branch-1 and Branch-2 flip-flops are turned on to implement the incrementing of the I register if the skip condition exists and to transfer the modified factor back into the specified XR. If accumulator = 0 or A0 ≠ B0 (B0 latch), increment the I register.

This operation enables the addition, to an Index register, of a value greater than that which can be represented by the Displacement.

Hexadecimal Representation

One-Word Instructions

70XX	Add Disp to I (no skip can occur)
71XX	Add Disp to XR1
72XX	Add Disp to XR2
73XX	Add Disp to XR3

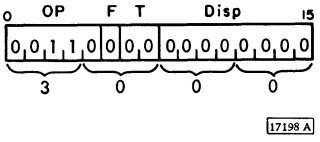
Two-Word Instruction, Bit 8 is 0

74XXXXXX	Add Positive Disp to the contents of core storage at Addr (Add to memory)
7500XXXX	Add Addr to XR1
7600XXXX	Add Addr to XR2
7700XXXX	Add Addr to XR3

Two-Word Instruction, Bit 8 is 1

74XXXXXX	Add negative Disp to the contents of core storage at Addr (Add to Memory)
7580XXXX	Add contents of core storage at Addr to XR1
7680XXXX	Add contents of core storage at Addr to XR2
7780XXXX	Add contents of core storage at Addr to XR3

Wait (WAIT)



- One word format only.
- Turns off the run flip-flop, stops clock advance pulses.
- The run flip-flop can be turned back on by a manual start or an interrupt.

- Cycle steal operations can function in the wait condition.
- Reference CC60141.

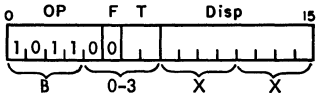
This instruction is a one word format instruction only. The P-C stops in a wait condition with the I register stepped to the wait instruction plus one. It can be restarted manually or by detection of an interrupt. Following completion of an interrupt subroutine, the instruction immediately following the Wait instruction is executed if the Branch Out of Interrupt (BOSC) is the normal indirect subroutine linkage. Data channel and Timer operations continue during the wait condition.

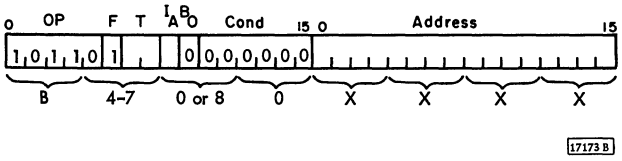
Hexadecimal Representation

One-Word Instruction (only)

3000	WAIT until manual start or until completion of an interrupt subroutine

Compare (CMP)





- The word in the accumulator is algebraically compared with the word in core storage specified by the effective address.
- The contents of the accumulator remain unchanged.
- Core storage remains unchanged.
- The Overflow indicator is unaffected.
- The Carry indicator may be changed by this operation.
- Reference CC60185.

The I register is modified according to the result of the comparison as follows:

Compare Result	I Register Modification
A > C(EA)	I = I
A < C(EA)	I = I + 1
A = C(EA)	I = I + 2

One-Word Instruction

- Compare A with C(EA).

Hexadecimal Representation	Effective Address
B0XX	I + Disp
B1XX	XR1 + Disp
B2XX	XR2 + Disp
B3XX	XR3 + Disp

Two-Word Instruction, Direct Address

- Compare A with C(EA).

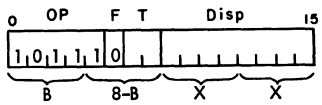
Hexadecimal Representation	Effective Address
B400XXXX	Addr
B500XXXX	Addr + XR1
B600XXXX	Addr + XR2
B700XXXX	Addr + XR3

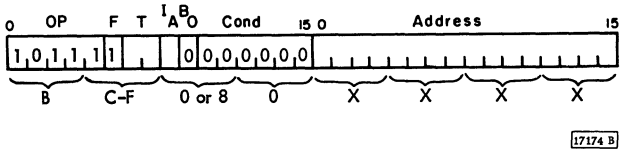
Two-Word Instruction, Indirect Address

- Compare A with C(EA).

Hexadecimal Representation	Effective Address
B480XXXX	C(Addr)
B580XXXX	C(Addr + XR1)
B680XXXX	C(Addr + XR2)
B780XXXX	C(Addr + XR3)

Double Compare (DCM)





- EA must be even.
- The 32-bit word in the accumulator and the extension register is compared with the 32-bit word at the core storage location specified by EA and EA + 1.
- The contents of A and Q remain unchanged.
- Core storage remains unchanged.
- The Overflow indicator is unaffected.
- The Carry indicator may be changed.
- Reference CC60187.

The Instruction Register is modified according to the result of the comparison as follows:

Compare Result	I Register Modification
A, Q > C(EA) , C(EA + 1)	I = I
A, Q < C(EA) , C(EA + 1)	I = I + 1
A, Q = C(EA) , C(EA + 1)	I = I + 2

One–Word Instruction

- Compare A and Q with C(EA and EA + 1) .

Hexadecimal Representation	Effective Address
B8XX	I + Disp
B9XX	XR1 + Disp
BAXX	XR2 + Disp
BBXX	XR3 + Disp

Two–Word Instruction, Direct Address

- Compare A and Q with C(EA and EA + 1) .

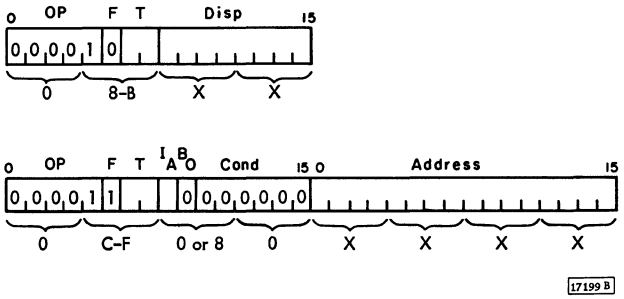
Hexadecimal Representation	Effective Address
BC00XXXX	Addr
BD00XXXX	Addr + XR1
BE00XXXX	Addr + XR2
BF00XXXX	Addr + XR3

Two–Word Instruction, Indirect Address

- Compare A and Q with C(EA and EA + 1) .

Hexadecimal Representation	Effective Address
BC80XXXX	C(Addr)
BD80XXXX	C(Addr + XR1)
BE80XXXX	C(Addr + XR2)
BF80XXXX	C(Addr + XR3)

EXECUTE I/O (XIO)



- Effective Address must be an even address for proper operation.
- XIO instruction addresses a two-word I/O Control Command (IOCC) which selects the I/O device, specifies the function to be performed, and provides the data address.
- XIO operations are performed by either direct program control or by a data channel.
- Reference CC60111.

This instruction is used for all I/O operations; it may be either one or two words in length, as specified by the F-bit. In the two-word instruction, the address is either a direct or indirect address, as specified by the IA bit. For proper operation, the effective address must be an even address. The effective address is used to select a two-word I/O control command (IOCC) from storage.

Internal, trace, CE, and external interrupts are suppressed for the first instruction following an XIO instruction. Therefore, the mask register (See Interrupt section) may be set without the possibility of an interrupt.

One–Word Instruction

- Execute IOCC at EA and EA + 1.

Hexadecimal Representation	Effective Address
08XX	I + Disp
09XX	XR1 + Disp
0AXX	XR2 + Disp
0BXX	XR3 + Disp

Two–Word Instruction, Direct Address

- Execute IOCC at EA and EA + 1.

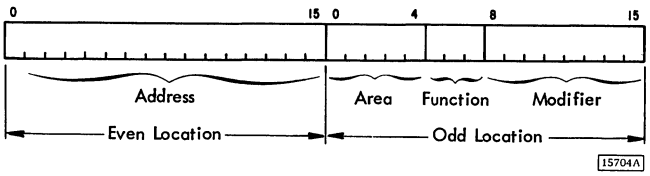
Hexadecimal Representation	Effective Address
0C00XXXX	Addr
0D00XXXX	Addr + XR1
0E00XXXX	Addr + XR2
0F00XXXX	Addr + XR3

Two–Word Instruction, Indirect Address

- Execute IOCC at EA and EA + 1.

Hexadecimal Representation	Effective Address
0C80XXXX	C(Addr)
0D80XXXX	C(Addr + XR1)
0E80XXXX	C(Addr + XR2)
0F80XXXX	C(Addr + XR3)

I/O Control Commands



The I/O control command (IOCC) consists of an address word at EA and a control word at EA + 1. The control word, consisting of the area, function, and modifier, is placed on the out bus first - during the E-1 cycle. The area, function, and modifier bits are decoded at each I/O device to set up the necessary controls for the operation.

Function

The following eight basic I/O functions can be specified by the three-bit function code.

Code	Function
000--	CE Mode This command places the selected device in the CE mode if modifier bit 15 is a one; it removes the device from the CE mode if bit 15 is a zero. The CE mode indicates, through the DSW, that the device is being checked by one of the diagnostic features. The CE mode also causes the device to interrupt on the CE-interrupt level (lowest priority) rather than on the assigned level.
001--	Write This code is used to transfer a single word from core storage to an I/O unit. The address of the core storage location is provided by the Address field of the I/O Control Command.
010--	Read This code is used to transfer a single word from an I/O unit to core storage. The address of the core storage location is provided by the Address field of the I/O Control Command.
011--	Sense Interrupt This code directs the I/O devices requesting interrupt recognition on the interrupt level specified by the Modifier field of the I/O Control Command to make their interrupt status available.
100--	Control This code causes the selected device to interpret the Modifier or Address field as a specific control action.
101--	Initialize Write This code initiates a Write operation on a device or unit which will subsequently make data transfers from core storage via a Data Channel.
110--	Initialize Read This code initiates a Read operation from a device or unit which will subsequently make data transfers to core storage via a Data Channel.
111--	Sense Device This code directs the selected device to make its current indicator status available for automatic placement into the P-C Accumulator.

Area

This five-bit field specifies the device to be used in the I/O operation. In some cases, the area specifies a group of devices (magnetic tape units, printers, etc.), and the modier field then designates the specific device.

Modifier

This field is used to extend or qualify the meaning of the area or function codes.

Address

The address word is read from core storage during the E-2 cycle.

The meaning of this 16-bit field is dependent upon the function of the I/O control command and the device adapter. Some examples are:

1. If the function is Initialize Write (101) or Initialize Read (110), the Address specifies the starting address of a table in storage (an I/O Block). This table contains data words and control information. Initialize Write and Initialize Read functions are used only with data channel control.
2. If the function is Control (100), and the Area specifies a disk storage device, the Address indicates the number of tracks the access must be moved.
3. If the function is Sense Device (111) or Sense Interrupt (011), the Address field is ignored. Instead, an increment of time, equivalent to a core storage cycle, is taken during which the selected I/O device or interrupt level places its status code into the P-C accumulator.
4. If the function is Write (001) or Read (010), the Address specifies the core storage location of the data word. These functions are used only with direct program control. The basic differences between a direct program control operation and a data channel operation are shown in Figure 3-16.

Cycle	Direct Program Control	Data Channel
E-1	Transfer Control Word to I/O Adapter	Same
E-2	Address word to Accumulator	Address word to Channel Address Register (CAR). Terminate Op.
E-3	Transfer data word to or from I/O Adapter using M register address. Op complete. Interrupt to I/O subroutine for subsequent data word transfers	None
Cycle Steal	None	Transfer data word to or from I/O Adapter using CAR address. Take C.S. cycles when needed for subsequent data word transfers.

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Figure 3-16. Direct Program Control and Data Channel Operations

Direct Program Controlled Operation

- Initiated by an Execute I/O (XIO) instruction with an I/O control command (IOCC) function of Control, Sense Interrupt, Sense Device, Read, or Write.
- Each data transfer or control operation requires an individual XIO instruction.
- The P-C channel data flow of a direct program controlled operation is shown in Figure 3-17.

I/O devices operating under direct program control in the 1800 system include:

1816 Printer Keyboard	Console Bit Switches
1053 Printer	Analog Input
1627 Plotter	Digital Input
1054 Paper Tape Reader	Analog and Data Output
1055 Paper Tape Punch	

Read/Write Function

When the function specified is a read or write, the address word provides the storage address, from or to which data will be transferred. At the conclusion of the storage cycle for data transfer, the XIO instruction is terminated and the next sequential instruction is executed.

I-CYCLE: Loads the accumulator with the effective address (see I cycle description). An XIO effective address (EA) must be an even address.

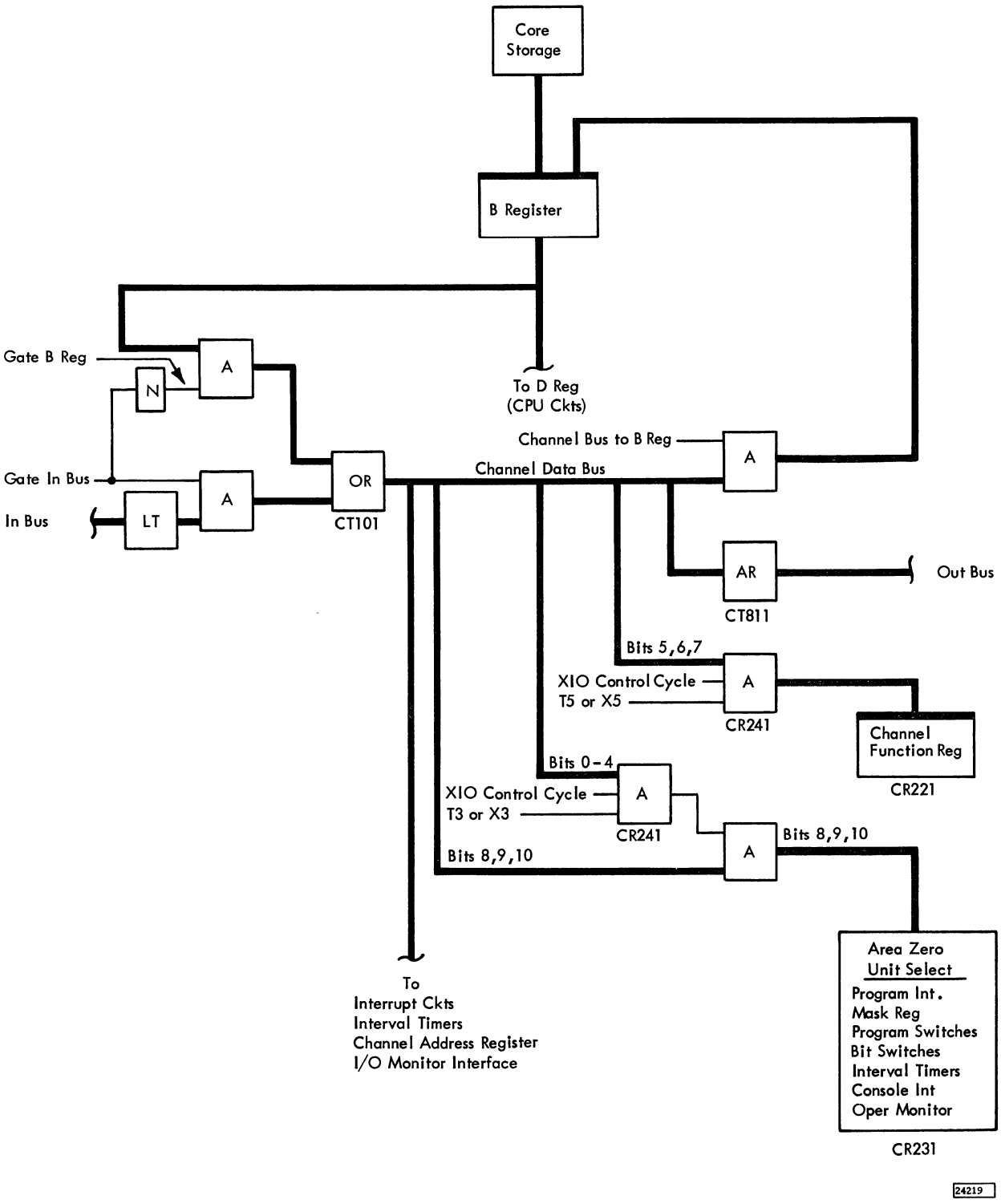


Figure 3-17. Basic Channel Data Flow

E1-CYCLE: Transfers EA to the M register and forces on the M_{15} bit. This causes the core storage location at EA + 1 (odd address) to be selected. The word at this location is loaded into the B register. This word (EA + 1) is the control word of the I/O control command; it contains the area, function, and modifier bits. It is placed on the out bus to be analyzed by the I/O adapters.

E2-CYCLE: Loads the accumulator with the address word portion of the IOCC (located at EA).

E3-CYCLE: Transfers the address word from the accumulator (loaded during E2 Cycle) to the M register. Using this M register address, the data word is transferred to or from the I/O adapter via the out or in bus.

Normally, transmission of several words is required to complete the data or message transfer. This is accomplished by allowing the P-C to respond to an interrupt request from the device when the device cycle has been completed and a subsequent data word is required. At an appropriate time, the P-C acknowledges the interrupt, identifies the request with a particular device, and by another XIO instruction, transmits the next sequential word of the message as specified by the IOCC.

It is the responsibility of the program subroutine answering the device interrupt request to modify the Address Word of the IOCC, provide table look-up to translate to the device character set if required, and maintain a program word count to indicate the end of message if necessary. At the completion of each interrupt subroutine sequence, the program must exit form the subroutine, utilizing a Branch or Skip on Condition instruction (BSC) with B9 = 1 which branches out of the interrupt program to the mainline program. (Refer to Branch or Skip on Condition instruction description.) This is necessary to restore the interrupt logic so that future interrupt requests at the same or lower interrupt levels can be acknowledged.

Control Function

With a specified function of control, the modifier field specifies to the device, the particular control operation to be executed. Examples of such control operations are start pulse-output timer, feed card, load interrupt mask register.

I-CYCLE: Same as Read/Write function.

E1-CYCLE: Same as Read/Write. Set up Area, Function, and Modifier decode circuits in I/O adapter. Some I/O adapters use this cycle to perform a particular control function.

E2-CYCLE: Certain I/O adapters interpret the Address Word at EA to determine the particular function and initiate that function during this cycle. For other I/O adapters, this may be a dummy cycle.

E3-CYCLE: Not used with a Control function.

Sense Interrupt

This command transfers the active interrupt level status word (ILSW) to the P-C accumulator. The ILSW represents the status of the interrupts assigned to the specified level. The P-C program analyzes the ILSW to determine the area or device requesting the interrupt. Modifier bits 10 through 15 are placed on the out bus by the interrupt circuits during the forced BSI operation (see MDM page CS60101). The forced BSI operation is described in Chapter 2, Interrupt Circuits.

I-CYCLE: Same as other functions.

E1-CYCLE: Same as other functions.

E2-CYCLE: The interrupt level status word, placed on the in-bus by the I/O adapter is loaded into the B register, then transferred to the accumulator.

E3-CYCLE: Not used with the sense interrupt function.

Sense Device

After the device causing an interrupt has been identified from data in the Interrupt Level Status Word (ILSW), it is necessary to determine the indicator(s) within the particular device causing the interrupt. This is accomplished by issuing a subsequent XIO sense device command with an area assignment corresponding to that of the device being interrogated.

Modifier bit 15 = 1 causes the status indicators associated with that particular device be reset after the information has been gated onto the in-bus. The information gated onto the bus and loaded into the accumulator in this instance is referred to as the device status word (DSW). The DSW contains one bit of information for each indicator within the device.

It is possible for a device to contain many conditions which may cause an interrupt on the same interrupt level. When this condition exists, it is usual that each of the interrupt conditions is logically ORed

and then gated to a particular bit of the in-bus. The identification of the interrupting condition within the device is accomplished by sensing the device status word and then analyzing it with the shift left and count instruction or a shift left and BSC combination.

I-CYCLE: Same as for other XIO functions.

E1-CYCLE: Same as for other XIO functions.

E2-CYCLE: The device status word, placed on the in bus by the device adapter, is loaded into the B register, then transferred to the accumulator.

E3-CYCLE: Not used with the sense device command.

Data Channel Operation

- Initiated by an Execute I/O (XIO) instruction with a function of initialize read or initialize write.
- Whenever a data channel requires core storage access to transfer data ("cycle steal" operation), the P-C operation is suspended for one core storage cycle.
- CQ40100 shows the data flow for a data channel operation.
- CQ40110 is a data channel operation flow chart.
- CQ60101 is a flow chart of the cycle steal request operation.
- CQ40120 is a diagram of data channel circuits.

The operation of a data channel is initiated by the execution of an XIO instruction which references an I/O control command (IOCC). Once started, the data channel operates independently of the main program being executed by the P-C provided the P-C is in the run, or trace mode. The data channel has the responsibility for controlling the quantity and destination of all data transmitted between core storage and the attached I/O device. Because of the independent operation of the data channel, large blocks of data can be transferred between core storage and an I/O device while many program instructions are performed between I/O control commands.

Since the P-C and data channel cannot take a storage reference cycle at the same time, the execution of an instruction in the main program will be delayed at least one cycle when the data channel reference is made. Once such a delay occurs, all of the time needed by the data channel will be taken before the main program execution is resumed. Such delays are imposed automatically and do not interfere with the internal registers or calculations in the P-C.

Scan Control

A Scan Control register is provided in each device that has chaining ability. Scan Control bits must be stored in the first word of the first data table (bit positions 0 and 1) and in the second word (bit positions 0 and 1) of the second data table and all subsequent data tables in a chain. The following is a list of the devices that have a Scan Control register.

I/O Device

2401/2402
Digital or Pulse Counter Input
Digital-Analog Output
Analog Input

The Scan Control register controls the I/O device and the Data Channel operation at the end of the data table as follows:

Bit 0	Bit 1	
0	0	Single scan of data table and stop with an interrupt
0	1	Single scan of data table and stop (no interrupt).
1	0	Continuous scan of this data table or a different data table with an interrupt at the end of this table.
1	1	Continuous scan of this data table or a different data table with no interrupt.

Operational Sequence

The numbered steps that follow correlate with the circled numbers in Figures 3-18 and 3-19. These steps apply to either non-chaining devices or the first data table of a chaining device.

1. XIO references the IOCC-control word first, then address word.
2. The area Code and Modifier select the I/O device. Function specifies the type of operation (Initialize Read or Initialize Write, etc).

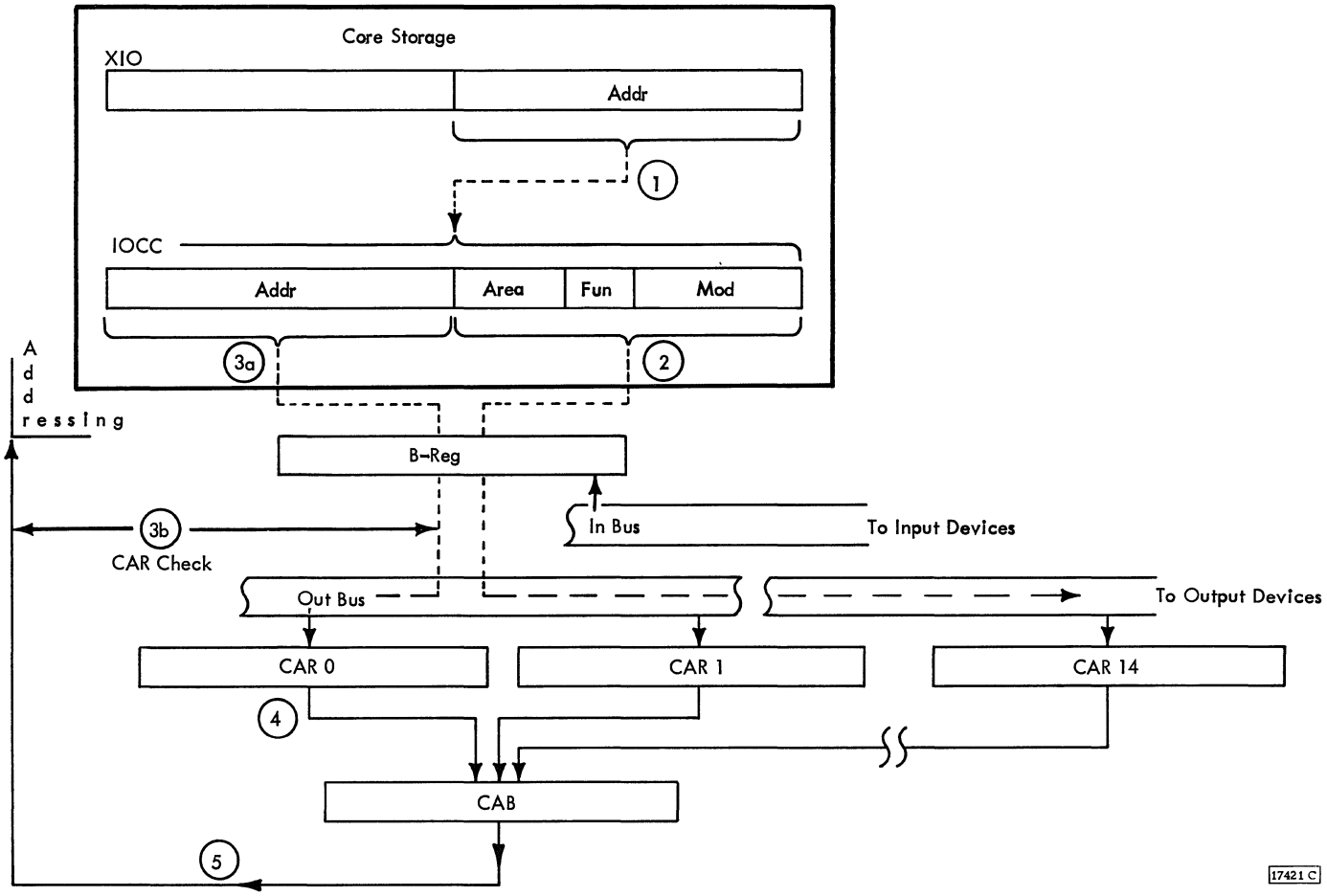


Figure 3-18. Data Channel Operation

3a. The Address portion of the IOCC word is stored in CAR for the selected Data Channel (I/O device).

3b. CAR Check made between selected CAR and B-register (CC30101).

4. Cycle steal requested.

5. CAR addresses core storage during X0, X1, and X2 time. CAR is transferred to CAB. CAB addresses core storage while CAR is incremented.

6. The first word of the data table contains
   a. Scan Control bits (bit positions 0 and 1)
   b. Word Count (bit position 2-15)
   These are transferred to their respective registers in the I/O device. This is the end of the first cycle-steal cycle.

7. When another cycle steal request occurs, CAR, which was incremented in step 5, now transfers the next higher address to CAB. CAB then addresses core storage while CAR is being incremented.

8. The first data word is transferred to or from the I/O device via the B-register and Data Channel. The word count in the I/O device is decreased by one. This is the end of the second cycle-steal cycle.

Steps 7 and 8 now continue on a cycle-steal basis; that is, they occur as the I/O device requests data transfers. Between cycle steals, the P-C continues program operation. The CAR is incremented with each data transfer and the word count is decremented. This sequence continues until the last data word of the data table is transferred. The last word transfer is sensed by the word count reaching zero or through some indicator in the device. If the device does not have chaining ability, no more demands for data transfer are made until the device is reinitialized with another XIO instruction.

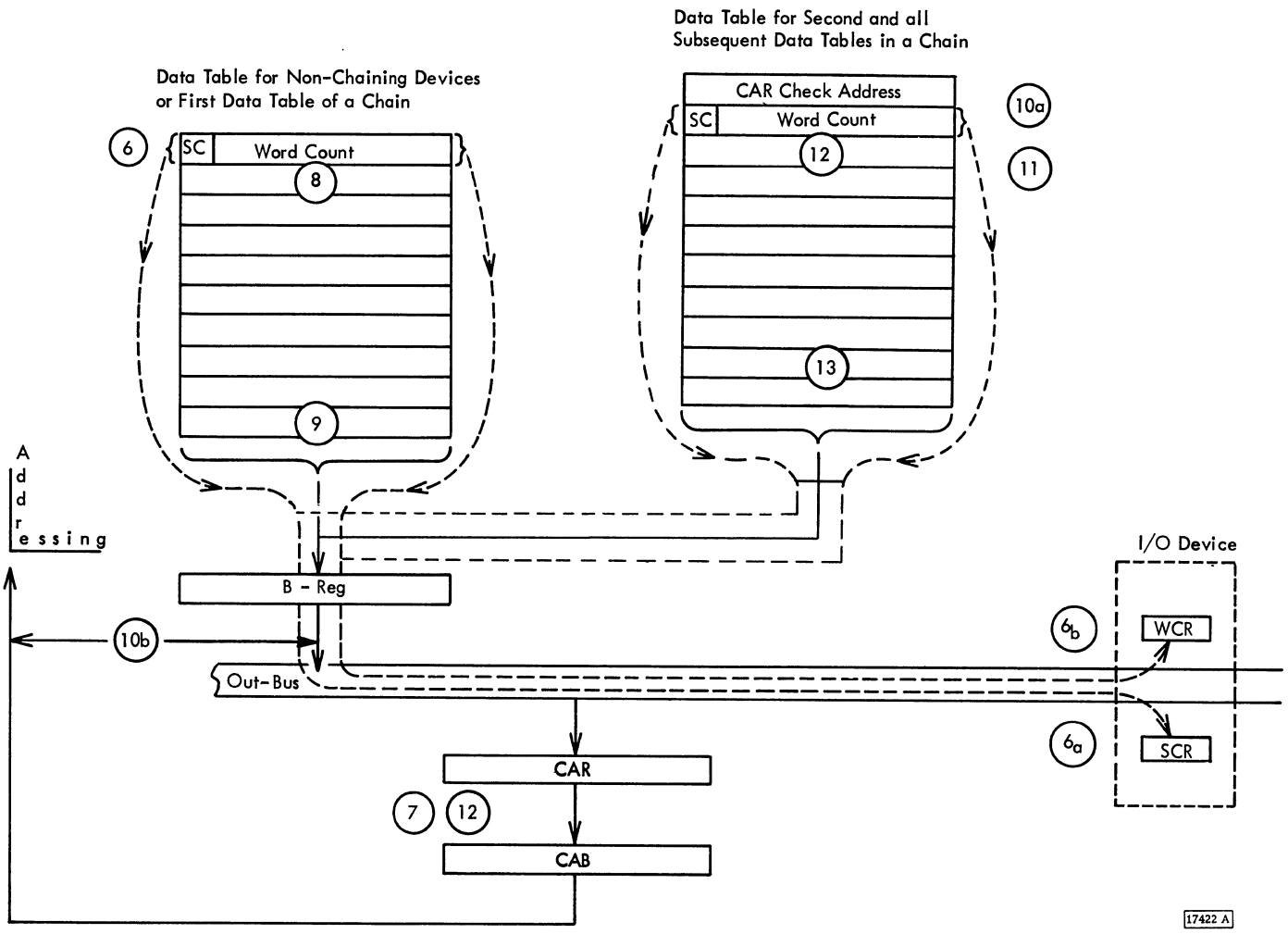


Figure 3-19. Data Channel Chaining

Data Chaining

When a continuous scan is indicated by the Scan Control register (SCR) in a device having chaining ability, the data channel takes three cycles after the word count has reached zero at the end of the first data table. The first cycle is used to transfer the word following the data table to the CAR. The address in this word is the address of the next table of data. The second cycle addresses the first word of the data table and performs the CAR check. The first word of the data table must contain its own address. The third cycle addresses the second word of the data table and transfers its contents (Word Count and Scan Control) to their respective registers. The I/O device is then ready for independent data channel operation. In this manner, the data channel can operate in a scatter read-write mode. This method of using the data channel in a continuous mode is called "data chaining" because the data tables are essentially connected together. The length of time between data transfer cycles on a data chaining operation is a maximum of three core-storage cycles on a device connected to the highest priority data channel. It may be greater than this for devices of lower cycle steal priorities, depending on whether they must wait for higher data channel priorities to be serviced.

Data Channel Operation (Chaining)

If the Scan Control register contains the bits for a continuous scan, the following numbered steps correlate to the circled numbers in Figure 3-19. These steps are for the second and all subsequent data

tables. See the previous Operational Sequence for steps 1 through 8 (first data table).

9. The contents of the word following the last data word in the first data table are transferred to CAR. This word must contain the address of the next data table.

10a. When the next cycle is requested, CAR addresses core storage, then CAR is transferred to CAB to address core storage and CAR is incremented. The contents of the first word of the next data table are transferred to the B-register. This word must contain the address of itself.

b. CAR Check is performed.

CHAIN CAR CHECK: When a data table is being chained, the first word in that table must contain its own core storage address. This first word is read from core storage and compared with the contents of the channel address register (CC30101). If these two addresses do not compare, a CAR check is indicated in the cycle-stealing I/O device adapter. The chain CAR check is initiated by the cycle-steal-control 0, 1, and 2 lines from the adapter.

11. When the next cycle steal is requested, CAR is transferred to CAB and CAB addresses core storage. The Scan Control bits and Word Count bits are transferred from the second word of the data table to their respective registers. CAR is incremented by one.

12. Data is transferred to (from) the I/O device on a cycle steal basis via the B-register and the Data Channel. CAB addresses core storage to transfer a data word to the B-register. Each time CAB addresses core storage, CAR is incremented by one. When the next cycle steal request occurs, CAR is transferred to CAB. The Word Count register is decremented for each word transferred.

13. When the last data character is transferred (Word Count is decremented to zero), operation will continue as specified by the Scan Control register. See section for Scan Control.

Data Table

Figure 3-20 is an illustration of two data tables with Scan Control (SC) bits to initiate chaining from the first data table to the second data table.

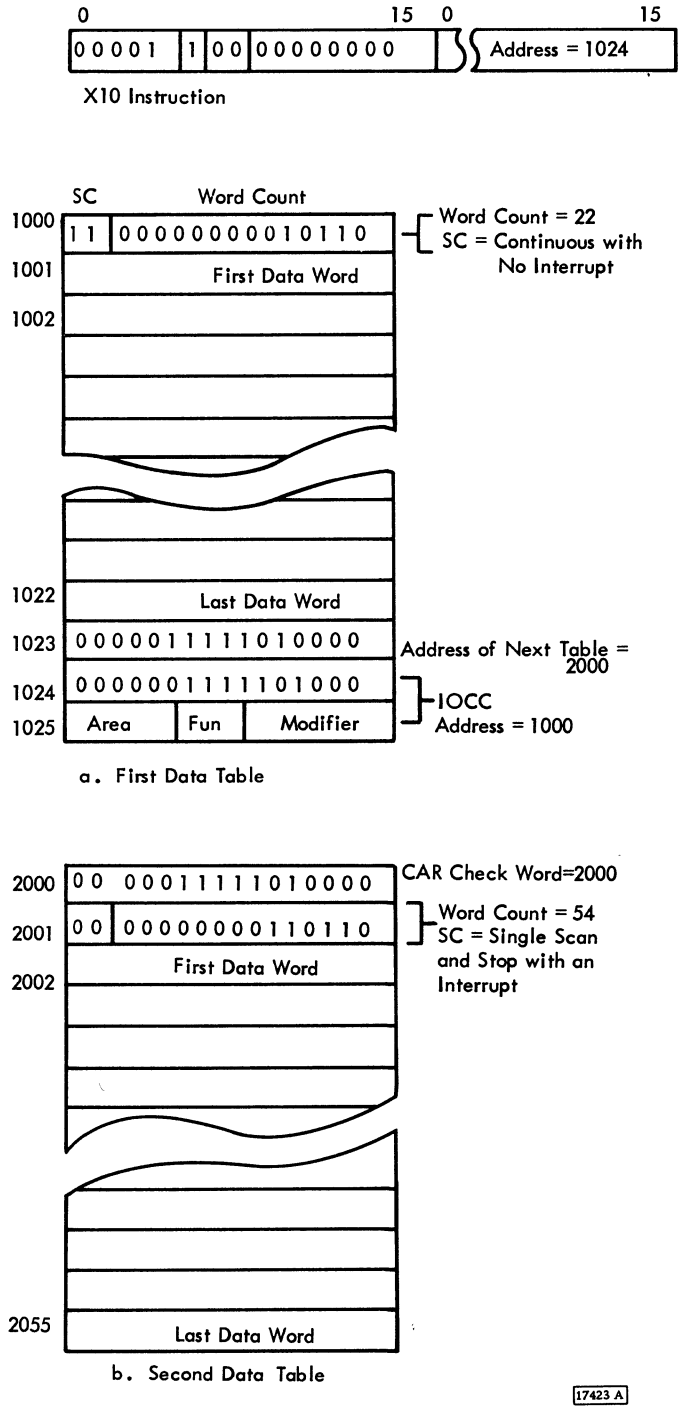


Figure 3-20. Data Tables for Chaining

XIO Instruction Execution

I CYCLE: Loads the accumulator with the effective address (see I cycle description). An XIO effective address (EA) must be an even address.

E1 CYCLE: Transfers EA to the M register and activates the output of M_{15} bit flip-flop. This causes the core storage location at EA + 1 (odd address) to be selected. The word at this location, which is the control word of the I/O control command, is loaded into the B register. The control word contains the Area, Function, and Modifier bits. This word is placed on the out-bus to be analyzed by the I/O adapter.

E2 CYCLE: The Address Word at EA is loaded into the B register, placed on the Out-Bus and loaded into the Channel Address Register (CAR) associated with the Data Channel to be used. A CAR check is made at this point to check for proper loading of CAR. The XIO operation is then terminated.

Cycle–Steal Cycle

Whenever an I/O unit requires core storage access, it activates a cycle-steal-request signal. The CS-level flip-flop, assigned to the level used by that I/O unit, is turned on at T7 time of any operation (CQ50101). The channel clock (X clock) begins advancing at the end of T7 if the P-C is in run or single-step mode and any cycle-steal level is active. If the cycle steal is from the interval timer, the timer gate (delayed) must be active.

One cycle is required to complete a normal cycle steal operation; therefore, the T clock is blocked for one cycle. (The interval-timer cycle-steal operation requires two cycles.) The M register output is blocked to permit core storage addressing from the data channel. From X0 to X2 core storage is addressed directly from the CAR associated with the highest priority level requesting a cycle steal. At X1 the contents of CAR are transferred to channel address buffer (CAB) and from X2 to X7 core storage is addressed from the CAB. The channel address buffer is used so that CAR can be incremented (at X4 time) to maintain the next address to be used by that level. The output of CAR is placed directly on the address-in bus to avoid the effect of circuit delays in loading CAB.

During the first cycle-steal cycle, the address in CAR is the location of the word count. (The 1442 operation does not use a word count.) The word count is placed on the out-bus and loaded into the adapter word count register in complement form.

During subsequent cycle-steal cycles, the data word is either read from core storage at the CAR address and placed on the out-bus (initialize-write function) or it is taken from the in-bus and stored at the CAR address (initialize-read function).

The word count register is decremented and tested for a zero condition. (Some adapters increment their word count register and test for a full condition.) If the word count equals zero, an interrupt request is made to signal the end of the data table. If another cycle-steal level flip-flop is on, that level will be serviced (highest priority level first) before returning to the program operation.

INTERNAL I/O OPERATIONS

- Read command is used to transfer the status of console bit switches to core storage.
- Sense-interrupt command is used to transfer the ILSW to the accumulator for identifying the source of an interrupt.
- Sense-device command is used to transfer the status of console bit switches, console interrupt status, or interval timer status to the accumulator.
- Control command is used to start and stop interval timers, reset the operations monitor, and set or mask interrupts.

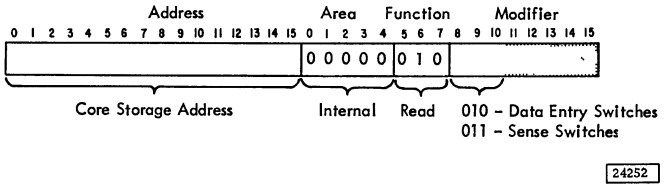
XIO instructions are used for direct program control of devices within the processor-controller. An area code of 00000 is assigned to these devices and is fixed for all 1800 systems.

The status of bit switches on the programmer's console can either be sensed (loaded into the accumulator) or read into core storage.

Read

- The console switch data is transferred to core storage.

Input/Output Control Command



ADDRESS: The address specifies the core location at which the data word is to be stored.

AREA: These five bits contain the processor-controller internal area code (00000).

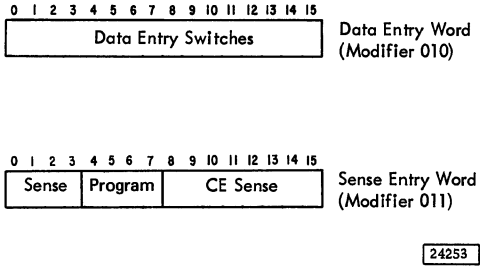
FUNCTION: Code 010 specifies the read function.

MODIFIER: Bits 8, 9, and 10 specify the group of switches whose status is to read.

010 console data entry switches
011 console sense, program, and CE sense switches

Other bit positions have no significance.

Data Words



The data word contains the requested status to be stored at the core location specified by the IOCC address word. Bit positions of the data word define the off/on (zero/one) status of the selected switches.

Description

E1 CONTROL CYCLE: The word at EA-plus-one is loaded into the B register and placed on the out bus. Function bits 5, 6, and 7 are registered by the P-C channel control and are decoded to select the read function. Area and modifier bits are registered by the area-zero control and are decoded to select the desired input data.

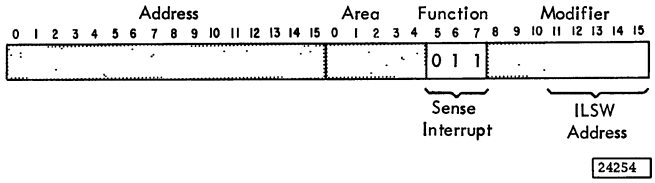
E2 DATA CYCLE: The word at EA (address portion of IOCC) is loaded into the B register, then transferred to the accumulator.

E3 DATA CYCLE: The address word is transferred from the accumulator to the M register. The selected device data word is gated into the B register by the read function, then entered into core storage at the address specified by the M register.

Sense Interrupt

- The ILSW defined by the interrupting level is loaded into the accumulator.
- The timer interrupts are assigned collectively to one bit position of a selected ILSW and the console interrupt is assigned to one bit position of a selected ILSW.
- The internal (check) interrupts --- invalid operation, parity error, storage protect violation, and CAR check --- are assigned respectively to bit positions 0, 1, 2, and 3 of the internal-level (sub-zero) ILSW.

Input/Output Control Command



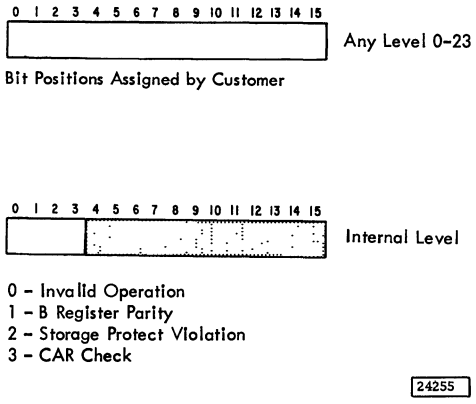
ADDRESS: Not used.

AREA: Not used.

FUNCTION: Code 011 specifies the sense-interrupt function.

MODIFIER: Bits 11 through 15, containing the ILSW address, are generated automatically by the processor-controller to define the interrupting level. These bits are placed on the out bus during the XIO control cycle and are decoded by each I/O device to address those device interrupts which are assigned to this ILSW. The area-zero interrupts, however, are addressed directly from the interrupt level flip-flops at the level to which they are assigned.

Interrupt Level Status Words



The timer interrupts are logically ORed to provide a single interrupt request. The interrupt request is assigned by the customer to a selected interrupt level (0-23) and to one bit position (0-15) of the associated ILSW. The sense-interrupt command must be followed by a sense-device command to identify the particular timer that summoned the interrupt.

The console interrupt is also customer-assigned to an interrupt level and an ILSW bit position. Console interrupt status is given directly by the sense-interrupt command; however, it is necessary to execute a sense-device command with a bit in position 15 of the IOCC modifier in order to reset the indicator.

Each internal error interrupt has a fixed bit assignment in the internal-level (highest priority) ILSW. Indicator status is given directly by the sense-interrupt command and the indicators are reset upon execution of the command. A sense-device command is not required for these indicators and no DSW is provided (no area code is assigned).

Bit positions of the internal-level ILSW define the off/on (zero/one) status of the following interrupt indicators:

Invalid Operation (bit 0) is turned on to request an interrupt if an undefined operation code is detected. Of the 32 op codes available in the five bits of the operation field, the following six are undefined:

00000	01011
00111	01111
01010	11111

B Register Parity (bit 1) turns on to request an interrupt if the B register parity check circuits detect an error when reading into or writing out of core storage. The error condition is ORed with the CAR check line and transmitted to all I/O devices so that the device sending or receiving the data can set its own parity error indicator on the same cycle that the error is detected.

Storage Protect Violation (bit 2) turns on to request an interrupt if an attempt is made to write into a storage-protected position of core storage. The error condition is transmitted to all input devices so that the device sending the data can set its own storage-protect-violation indicator on the same cycle that the error is detected.

CAR Check (bit 3) turns on to request an interrupt if a CAR check occurs during data channel operation. The error condition is ORed with the parity error line and transmitted to all I/O devices so that the device using the data channel can set its parity error indicator on the same cycle that the CAR check is detected.

Description

E1 CONTROL CYCLE: The word at EA-plus-one is loaded into the B register and placed on the out bus. Function bits 5, 6, and 7 are registered by the P-C channel control and are decoded to select the sense-interrupt function.

E2 DATA CYCLE: If the interrupt was summoned by an interval timer or console interrupt, the active interrupt level is ANDed with the sense-interrupt function to gate the ILSW bit into the assigned bit position of the B register. This bit position, together with bit positions assigned to other I/O devices on the same interrupt level, make up the interrupt-level status word which is transferred to the accumulator.

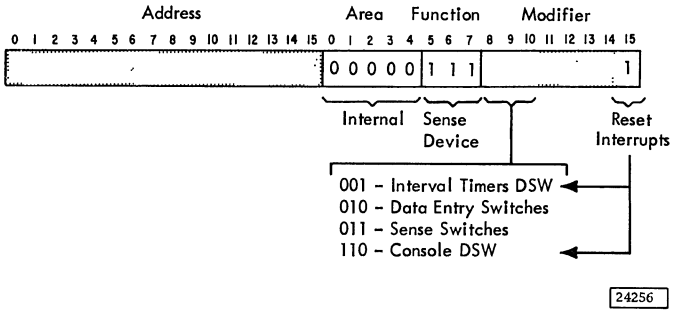
If the interrupt request was summoned by an internal error condition, the subzero level is activated and inhibits the recognition of all other interrupt levels. The error indicator status is gated into the B register by the sense-interrupt function, then transferred to the accumulator.

The E3 cycle is not used with the sense function.

Sense Device

- The console switch data, console status word, or interval timer status word is loaded into the accumulator.

Input/Output Control Command



ADDRESS: Not used.

AREA: These five bits contain the processor-controller internal area code (00000).

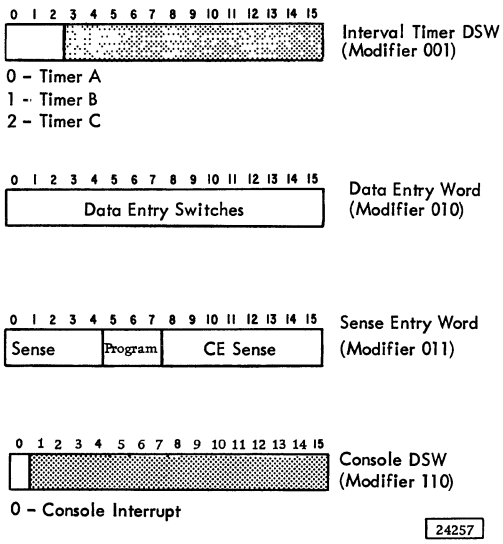
FUNCTION: Code 111 specifies the sense-device function.

MODIFIER: Bits 8, 9, and 10 specify the internal (area zero) device status to be sensed as follows:

001	interval timers DSW (interrupt indicators)
010	console data entry switches
011	console sense, program, and CE sense switches
110	console DSW (interrupt indicator)

Bit 15 is used when addressing the interval timer DSW or the console DSW. Bit 15=1 specifies that interrupt indicators are to be reset after sensing. Other modifier bits have no significance.

Status Words



The status words contain the requested device status to be loaded into the accumulator. Bit positions of the status word define the off/on (zero/one) status of the selected console bit switches or interrupt indicators.

The console DSW contains the status of the console interrupt indicator in bit position 0. Other bit positions are not used. The console interrupt indicator turns on to request an interrupt when the console interrupt key is operated. The indicator will be reset upon sensing only if there is a bit in position 15 of the IOCC modifier.

The interval timer DSW contains the status of interval timer interrupt indicators A, B, and C in bit positions 0, 1, and 2 respectively. An interval timer indicator turns on to request an interrupt when the preselected fixed time interval expires. Indicators will be reset upon sensing if there is a bit in position 15 of the IOCC modifier.

Description

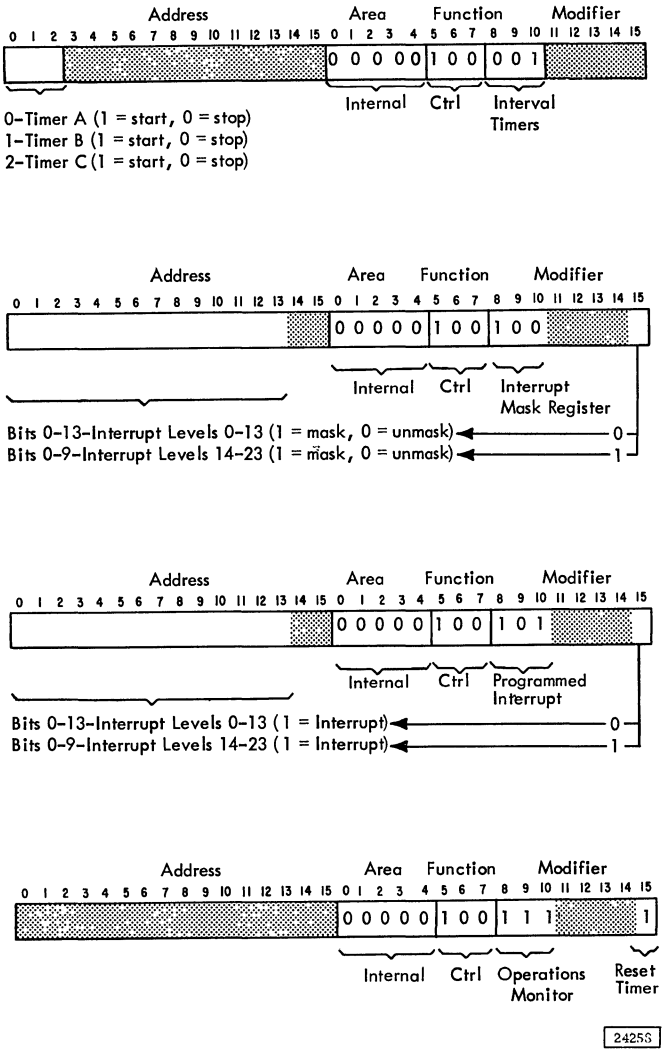
E1 CONTROL CYCLE: The word at EA-plus-one is loaded into the B register and placed on the out bus. Function bits 5, 6, and 7 are registered by the P-C channel control and are decoded to select the sense-device function. Area and modifier bits are registered by the area-zero controls and are decoded to select the desired input data.

E2 DATA CYCLE: The selected device status word is gated into the B register by the sense-device function, then transferred to the accumulator. If the IOCC modifier contained a bit in position 15, the interrupt indicators will be reset after their status is sensed. The E3 cycle is not used with the sense function.

Control

- Performs the control function specified by the modifier.
- Used to start and stop interval timers, reset the operations monitor, and set or mask interrupts.

Input/Output Control Commands



ADDRESS: When the control function is specified, the IOCC address word at EA does not contain a core storage address, but may contain data to be sent to the device on the E-2 data cycle for use in the control operation. The function of these bits depends upon the area-zero device specified by the modifier bits.

For controlling the interval timers, bit positions 0, 1, and 2 of the address word are used to start or stop timers A, B, and C respectively. A "1" bit turns on the timer and a "0" bit turns off the timer.

For controlling the masking of interrupt levels 0-23, bit positions 0 through 13 of the address word are used to set or reset positions 0 through 13 of the interrupt mask register when modifier bit 15 = 0. When modifier bit 15 = 1, bit positions 0 through 9 of the address word are used to set or reset positions 14 through 23 of the interrupt mask register. A "1" bit sets the associated flip-flop and a "0" bit resets the associated flip-flop.

For program initiation of interrupts, a "1" bit in any position 0-13 of the address word turns on the respective interrupt level 0-13 when modifier bit 15 = 0, when modifier bit 15 = 1, a "1" bit in any position 0-9 of the address word turns on the respective interrupt level 14-23.

The address word is not used in the IOCC that controls the resetting of the operations monitor.

AREA: These five bits contain the processor-controller internal area code (00000).

FUNCTION: Code 100 specifies the control function.

MODIFIER: Bits 8, 9, and 10 designate the internal (area zero) device to be controlled as follows:

Bits 8	9	10	
0	0	1	interval timers
1	0	0	interrupt mask register
1	0	1	interrupt level register
1	1	1	operations monitor

Bit 15 is used when addressing the interrupt mask register or the interrupt level register. Bit 15 = 0 specifies the use of address bits 0-13 to control positions 0-13 of the register. Bit 15 = 1 specifies the use of address bits 0-9 to control positions 14-23 of the register.

Bit 15 is also used to control the resetting of the operations monitor. Bit 15 = 0 does not reset the monitor; bit 15 = 1 resets the monitor to the full time period specified by the Operations Monitor switch on the I/O monitor interface panel.

Description

E1 CONTROL CYCLE: The word at EA-plus-one is loaded into the B register and placed on the out bus. Function bits 5, 6, and 7 are registered by the P-C channel control and are decoded to select the control function. Area and modifier bits are registered by the area-zero control and are decoded to select the internal device or the positions of the device to be controlled.

E2 DATA CYCLE: The word at EA is loaded into the B register, then the appropriate bits are gated to the timer mask register, the interrupt mask register, or the interrupt level register.

If the interval timers have been selected by the control function, the status of bits 0, 1, and 2 are loaded into positions A, B, and C of the interval timer mask register.

If the interrupt mask register has been selected, the status of bits 0-13 or 0-9, depending on modifier bit 15, are loaded into positions 0-13 or 14-23 of the interrupt mask register. Any positions of the interrupt level register that are on when their related mask register flip-flops turn on will be reset.

If the interrupt level register has been selected, the bits in positions 0-13 or 0-9, depending on the status of modifier bit 15, are used to set positions 0-13 or 14-23 of the interrupt level register, but only if the designated positions of the register are not masked.

Note: The programmed-interrupt control function (modifier 101) may also be used by the customer engineer to test cycle-steal-request and cycle-steal-acknowledge. The address portion of the IOCC is not used, nor is bit 15 of the modifier. The cycle-steal level to be tested is selected manually by wire jumper placement. This test procedure is described in the 1800 system maintenance manual (see FE Bibliography – 1800 system, Order No. SY26-0560).

INTERRUPT OPERATION

- Some condition, external to the mainline program, causes an automatic branch to a subroutine that results in correcting or servicing the condition.

- Interrupts are grouped into priorities, 12 levels of which are standard; 12 additional levels are available.

- Interrupt levels can be masked and unmasked by the program.

- In addition to the 24 customer interrupt levels, three levels are used for internal or CE functions.
  1. Internal (check) interrupt is sub-zero level (highest priority) and is initiated by an invalid op code, a parity check, a CAR check, or a storage protect violation.
  2. Trace level is a lower level priority than any customer assigned level. It causes a branch prior to each program instruction.
  3. CE interrupt level enables the initiation of an interrupt by the CE Interrupt key on the console, or by a device operating in CE mode.

The interrupt function provides an automatic branch in the normal program sequence based upon an external condition. Examples of conditions which would normally be utilized to cause interrupts follow:

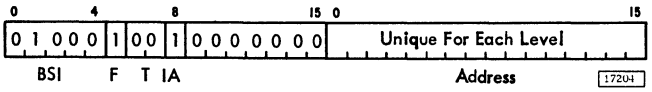
1. The interval timer has concluded the recording of a preset time interval.
2. The magnetic tape unit initialized and selected on a data channel has completed the required data transfer and signals the P-C with a scan complete.
3. An undefined operation code has been detected during the P-C instruction readout and therefore cannot be executed.
4. The device operating on direct program control has completed the transfer of the previous character and requests a subsequent character.
5. An external process condition has been detected which requires an immediate change in the program execution.

Because of the large number and widely varying types of interrupt requests, it is often not possible to cause a branch to a unique address for each condition. For the same reason, it is not desirable to cause the same branch for all interrupt requests and require the program to determine the individual request(s) requiring service. Therefore, it is convenient to group the many individual request lines into a lesser number of priority levels. This accomplishes two very important functions. First, it allows all interrupt requests common to a specific interrupt level to interrupt immediately if the only requests present are of a lower priority level. Conversely, it permits interrupt requests connected to a higher priority level to delay the servicing on a lower level and immediately interrupt to the higher priority and return to the initial request only after all higher level requests have been serviced. Second, since a unique branch can be defined for each interrupt priority level, it is possible to combine many interrupt requests on a common priority level and therefore utilize a common interrupt subroutine to service many requests.

Three important operating characteristics of the 1800 interrupt system are as follows:

1. When more than one request is connected to any one priority level, it is necessary that the program identify the individual request(s) causing the priority level to be active.

2. The first request that is recognized on a given priority level prevents future requests on that or lower priority levels from interrupting until the completion of servicing the first interrupt is signaled by a branch out operation. (See "Branch or Skip on Condition" instruction.) However, interrupts that occur on the same level for which an interrupt is being serviced can be recognized and serviced by the program if the Interrupt Level Status Word (ILSW) is interrogated again before the branch out is executed. The ILSW is explained in detail towards the end of this Chapter.
3. When an interrupt request is recognized, the processor-controller inhibits normal access to core storage, generates the BSI instruction with indirect addressing, and places it in the B-register. The format of this forced BSI instruction is shown in the following illustration. The content of the address portion of the BSI instruction is unique for each interrupt level and denotes the core storage location containing the indirect address (interrupt vector) for that level.



Interrupt Levels

As shown in Figure 3-21 a maximum of 24 external interrupt levels are available. Twelve external interrupt levels are standard, as are the Internal, Trace, and CE interrupt levels. Note that the priority level of each interrupt, as well as its unique core storage address, is listed in decimal form. Note also that all but the Trace and CE interrupts have an Interrupt Level Status Word (ILSW). The ILSW, which is explained in detail later, is used to identify the specific condition causing its interrupt level to request service. No external interrupt can occur at the end of an XIO or BSI instruction (until another instruction is taken).

Internal (Check) Interrupt

The Internal interrupt is a P-C interrupt that occurs when any one of four error conditions occur in the P-C (CC30102):

1. An invalid op code is detected.
2. A parity error (even number of bits) is detected in the B-register during data transfer to or from core storage.

Interrupt	Priority Level	Core Storage Location		ILSW	
		Decimal	Hex		
Internal	1	8	8	Yes	
Trace	26	9	9	No	
** CE	27	10	A	No	
*External 0	2	11	B	Yes	
1	3	12	C	Yes	
2	4	13	D	Yes	
3	5	14	E	Yes	
4	6	15	F	Yes	Basic
5	7	16	10	Yes	
6	8	17	11	Yes	
7	9	18	12	Yes	
8	10	19	13	Yes	
9	11	20	14	Yes	
10	12	21	15	Yes	
11	13	22	16	Yes	
12	14	23	17	Yes	
13	15	24	18	Yes	
14	16	25	19	Yes	Special
15	17	26	1A	Yes	Feature
16	18	27	1B	Yes	Group 1
17	19	28	1C	Yes	
18	20	29	1D	Yes	
19	21	30	1E	Yes	Special
20	22	31	1F	Yes	Feature
21	23	32	20	Yes	Group 2
22	24	33	21	Yes	
23	25	34	22	Yes	

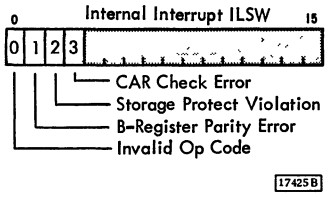
* External interrupt cannot occur at the end of an XIO or BSI instruction.

** A CE interrupt stores the return link in core storage location /000A and starts execution at core storage location /0001. Interrupts are prevented in the same manner as for the standard forced BSI.

Figure 3-21. Interrupt Levels 17424C

3. A storage protect violation occurs from an attempt to write into a "read-only" core storage position.
4. CAR-check error occurs either as a CAR check or as the result of a parity error having caused a command reject.

The Internal interrupt cannot be masked. However, an XIO or BSI instruction prevents the Internal interrupt for one instruction. Its ILSW is reset when it is sensed to determine the interrupting condition. The four error conditions are assigned to the ILSW as follows:



Trace Interrupt

The Trace interrupt occurs after every instruction if the P-C is in program operation with the console mode switch on Trace (CS50101, A3). The Trace interrupt cannot be masked (no mask flip-flop at C3) and does not have an ILSW. However, an XIO or BSI instruction prevents a Trace interrupt for one instruction.

CE Interrupt

The CE interrupt can be initiated from the CE panel or from a device operating in CE mode (CS50130, B6). It cannot be masked (no mask flip-flop--CS50101, C2) and does not have an ILSW. The CE level is not polled on an XIO or BSI instruction. It has the lowest interrupt priority and therefore must wait for service until all other levels are serviced.

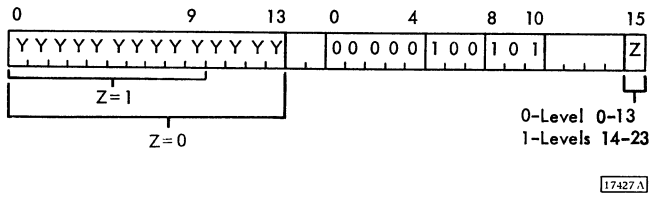
CE interrupt differs in operation from other interrupts in that the contents of the I register (customer's program) is always stored at address $000A_{16}$ and the branch is direct, instead of indirect, to address 0001_{16}. This branch may be to main or auxiliary storage, depending on the Interrupt to Main/Aux switch. The BOSC to end CE interrupt returns to the mainline program via the address stored at $000A_{16}$.

External Interrupts

External interrupt level flip-flops are set during polling by bits on the channel data bus. At this time, the channel is not moving data. Channel data bus bits originate from I/O adapters, the interval timers or a programmed XIO control command. All external interrupts can be masked (suppressed) if the individual mask flip-flop is on. All masks are set on by a dc reset and must be reset (unmasked) by an XIO control command before interrupts are honored. An XIO control command can set or reset a mask(s) under program control.

EXTERNAL INTERRUPT POLLING: Two polling cycles are required to sample all 24 interrupt level requests. Interrupt levels 0 through 13 are polled, as a group, on one cycle, and interrupt levels 14 through 23 are polled, as a group, on another cycle. The group that is polled on any given cycle is not readily predictable because the first group polled after an interrupt will be the group that was being polled when the interrupt occurred. Therefore, unmasking an interrupt level for one instruction, that takes only one core-storage cycle (MDX, LDX, LDS, etc), would not poll all 24 interrupt level requests. This one core-storage cycle instruction would poll only one group, and the group could be either 0-13 or 14-23.

PROGRAMMED INTERRUPTS: External interrupt levels can be programmed. An XIO control command is used to turn on individual external interrupt levels within either of two groups 0-13 or 14-23, depending on the status of modifier bit position 15 of the IOCC. Two instructions must be executed to turn on interrupt levels in both of these groups. The IOCC is shown below:



Note that the area is 00000 and that modifier bits 8-10 must be 101.

The status of address bits 0-9 or 0-13, depending on modifier bit 15 (Z), determine whether individual interrupts within priority levels 0-13 and 14-23 will be turned on (CS50102, C2):

A 1-bit turns on the corresponding external interrupt level.

A 0-bit does not turn on the corresponding external interrupt level.

Programmed interrupts will not occur if the corresponding interrupt level is masked prior to the time the XIO command is executed.

If a programmed interrupt level is turned on but the hardware forced BSI instruction has not occurred, an XIO instruction to mask or unmask any interrupt level will turn the programmed interrupt level off. Another programmed-interrupt XIO instruction would be needed to reinitiate the programmed interrupt after the specified interrupt level is unmasked.

INTERRUPT LEVEL MASKING: A mask register exists for the masking and unmasking of external interrupt levels (CS50101, B4 through B6). An interrupt level that is masked cannot initiate a request for service until it has been unmasked.

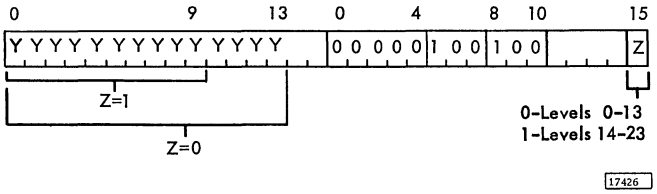
Programmed interrupts will not occur if the corresponding interrupt is masked prior to the time the XIO command for programmed interrupt is executed.

Device status words (DSW) and process interrupt status words (PISW) are not affected by the mask operation.

The XIO control command is used to simultaneously mask and unmask external interrupt levels

0-13 or 14-23, depending on modifier bit 15 of the IOCC. Two XIO control commands are required to mask/unmask the maximum of 24 external interrupts. (All external interrupts are automatically masked when electrical power is first applied to the P-C.) The execution of this instruction does not affect the contents of the accumulator.

The IOCC for the mask instruction is shown below:



Note that the area is 00000 and that modifier bits 8-10 must be 100.

The status of address bit positions 0-13 or 0-9, depending on modifier bit 15 (Z), determine whether external interrupt levels 0-13 or 14-23 are masked or unmasked:

A 1-bit masks the corresponding interrupt level.

A 0-bit unmasks the corresponding interrupt level.

STATUS WORDS

The I/O devices on the 1800 system and some of the system features contain "status" indicators. The on/off condition of each status indicator reveals to the operating program an operation status or condition of the device associated with the indicator. Status indicators are also contained in the process being monitored/controlled by the 1800 system. Both system and process oriented indicators project their individual conditions to the processor-controller via the in-bus for program interrogation.

Some of the status indicators may reflect a condition in the device or process that requires a program response. These indicators are assigned to interrupt levels and initiate interrupt requests when they are turned on.

The status words used in the 1800 are:

- Device Status Words (DSW). (The status word for the Selector Channel is known as the Channel Status Word (CSW). It is functionally the same as a DSW).
- Process Interrupt Status Words (PISW).
- Interrupt Level Status Words (ILSW).

Device Status Word Indicators

DSW indicators usually fall into three general categories:

1. Error or exception interrupt conditions.
2. Normal data or service required interrupts.
3. Routine status conditions.

These indicators are always read into the A-register with an XIO Sense Device instruction. The indicators can then be interrogated under program control. A unique DSW exists for each device. Some devices have more indicators than can be contained in one word. Therefore more than one status word may be associated with a particular device. The area and modifier bits of the IOCC control word specify the device whose DSW is to be sensed and if the device has more than one status word, the particular word desired. The format of the DSW(s) for each I/O device is shown in Chapter 1 of the FE Maintenance Manual.

Some of the indicators in a DSW can be reset under program control. Modifier bit 15 being on (1) in a Sense Device IOCC specifies reset of all program resettable indicators in the DSW sensed. Indicators in a DSW that cannot be reset by the program are turned off when the respective conditions in the device are reset. The functions of each indicator in a DSW is explained in the respective section for each device.

Process Interrupt Status Word Indicators

PISW latches are physically located in the 1800 system (PD50110, sheet 1, C5). They are turned on by the closing of a contact or the shifting of a voltage in a remote customer process.

PISW's are read into the processor-controller with an XIO Sense Device or XIO Read instruction (B3). The difference between the two instructions is where the PISW is stored. An XIO Read instruction stores the PISW at the core storage location specified by the address word of the IOCC. The XIO Sense Device instruction stores the PISW in the A- register. When a PISW is read using either of these two instructions, all indicators in the PISW read are unconditionally reset (C5).

Assignment of PISW Bit Positions

Process interrupt points are terminated on 16-position terminal blocks within the 1800 system

(PD50110, Sheet 1, D2). The terminal block positions are assigned to PISW's as specified by the customer on a PISW assignment form. The following paragraphs define assignment restrictions.

Eight process interrupt adapters are available. Each adapter operates three 16-point groups (RC009). This combination provides a total of 24 16-point groups or a total of 384 interrupt points. Each of these 16-point groups is divided into four sets of four points each for PISW assignment. The sets in each 16-point group are 0 through 3, 4 through 7, 8 through 11, and 12 through 15. All sets of a group can be assigned to the same PISW or to different PISW's. However, the four points in a set must be assigned to the same PISW.

Each PISW can have 16 points assigned (four sets of four points each), and the positions of the PISW correspond to the positions of the points assigned. As shown in Figure 3-22 for example, terminal block positions 0 through 3 may be assigned to bit positions 0 through 3 of one PISW; terminal block positions 4 through 7 may be assigned to bit positions 4 through 7 of a second PISW; etc,. In a like manner, terminal block positions 0 through 7 could be assigned to bit positions 0 through 7 of one PISW and terminal block positions 8 through 15 could be assigned to bit positions 8 through 15 of a second PISW. However, no cross assignment such as position 0 of the terminal block to bit position 1 of a PISW is permitted. Position 0 must be assigned to bit position 0, 1 to 1 ... and 15 to 15.

Process Interrupt Status Word Address Assignment

PISW's are considered to be digital inputs but each PISW has its own unique address (PD20101, A4). Twenty-four PISW's are available and are numbered 1 through 24. The PISW's are assigned addresses 2 through 25 respectively. PISW's are addressed by the IOCC modifier bits of an XIO Sense Device or XIO Read instruction.

Interrupt Level Status Words

The interrupt facility includes one 16-position Interrupt Level Status Word (ILSW) for each interrupt level. (Trace and CE interrupt levels are exceptions as they are unique interrupts and require no ILSW for interrupt request identification.)

As shown in Figure 3-23, each ILSW bit is assigned to a PISW or a specific device. PISW indicators are ORed into the assigned ILSW bit position. Similarly, all DSW interrupt indicators from the assigned device are ORed into the single ILSW bit position assigned to the device. Whenever any one of the ORed interrupt indicators from a PISW or DSW is active, the respective ILSW bit is turned on causing the interrupt level to request service.

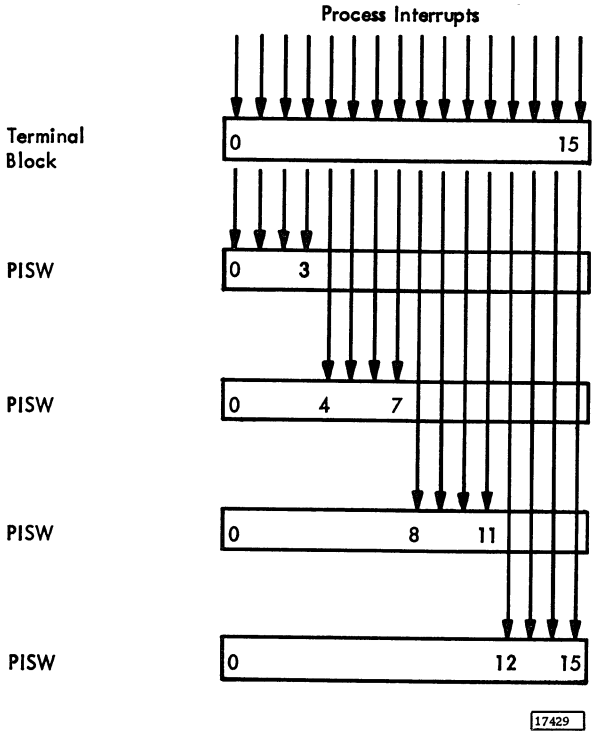


Figure 3-22. Bit Positions Assignment of PISW's (typical)

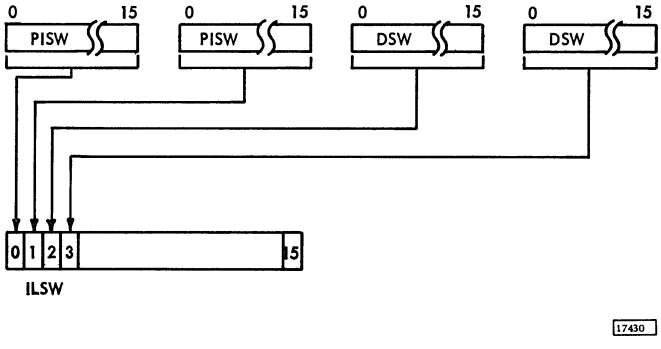


Figure 3-23. Relationship of Status Words

An ILSW is read into the A-register by an XIO Sense Interrupt Level instruction. The programmer does not specify the particular ILSW in the XIO Sense Interrupt Level instruction used to read an ILSW. This specification is fixed; that is, each ILSW is hardware assigned to its interrupt level. The XIO Sense Interrupt operation places the ILSW of the highest priority level requesting service into the A-register.

After a request for service has been recognized and the ILSW of the requesting interrupt level has been read into the A-register by an XIO Sense Interrupt Level instruction, the program determines which bit position in the ILSW caused the interrupt. This bit position identifies the DSW or PISW that has the interrupt-initiating indicator. The DSW or PISW is then analyzed by the program to determine which indicator in the DSW or PISW caused the interrupt.

Note that, except for internal interrupts, none of the DSW/PISW interrupt indicators ORed into ILSW bit positions are reset when the ILSW is read into the A-register. The indicators in a DSW are not reset until they are read into the A-register with an XIO Sense Device instruction with reset (IOCC modifier bit 15 on). Indicators in a PISW are unconditionally reset when read by an XIO Sense Device or XIO Read instruction.

Interrupt Level Status Word Assignment

Each external interrupt level has its own 16-position Interrupt Level Status Word (ILSW) to reflect the status of interrupt requests connected to the interrupt level. Each device or PISW is assigned to a specific ILSW and a particular bit position in that ILSW by the customer. Since each interrupt level has a fixed priority, the customer essentially assigns interrupt priority when he assigns a device or PISW to an ILSW bit position. Devices and PISW's are assigned to ILSW bit positions on the Interrupt Level Status Word assignment form. Assignment of devices or PISW's to ILSW's should begin with the leftmost bit position (bit 0) and progress to the next higher bit position for each additional device or PISW assigned to the ILSW. The following paragraphs describe restrictions on ILSW assignment.

A device (DSW) or PISW must be assigned to one and only one ILSW bit position. For example, each device in the first group of four 1816/1053's must be assigned to a different ILSW bit position for the same interrupt level. Similarly, each device in the second group of four 1816/1053's must be assigned to a different ILSW bit position for the same interrupt level. (It can be the same interrupt level as the first group.)

If the process interrupt routine in the Time Sharing Executive System or Multiprogramming Executive Operating System is used, each PISW must be assigned to its corresponding ILSW. For example, PISW 1 must be assigned to ILSW 0, PISW 2 must be assigned to ILSW 1,... and PISW 24 must be assigned to ILSW 23. Three PISW's are provided with each process interrupt adapter. The PISW's for any one process interrupt adapter must be assigned within either 0 through 11 or 12 through 23 interrupt level groupings. In addition, only one area code may be represented by any one ILSW bit.

The following interrupt requests must be assigned to an ILSW for all systems:

TI	Timer interrupt (combined interrupt from all three interval timers)
Typ-1	First 1053 or 1816 (circuits basic in processor-controller)
2401/2	1802 processor-controller only
CI	Console interrupt (can be assigned to any unused bit position on any available interrupt level)

Other interrupt requests must be assigned to an ILSW only if the feature is ordered for the system.

INTERRUPT SERVICING

The 1800 system is programmed to service interrupt requests in several ways, depending on interrupt level assignments. Examples follow:

1. A PISW and other interrupt requests are intermixed on the same interrupt level. If a process interrupt request occurs, the ILSW is interrogated first and the PISW is interrogated subsequently.
2. PISW's and other interrupt requests are intermixed on the same interrupt level, but the PISW's are to be given priority on that level. In this case, the PISW's (typically one) are interrogated directly prior to interrogating the ILSW.
3. An interrupt level is completely reserved for PISW's. In this case, the ILSW is interrogated to determine which PISW contains the actual interrupt request.

4. An interrupt level is reserved for only one PISW. In this case, the program can go directly to interrogation of the PISW.

In general, an interrupt occurs at the completion of the instruction being executed when the interrupt request occurs. However, the interrupt cannot occur when any of the following conditions exist:

1. The instruction being executed when the interrupt request occurs is either an XIO instruction, or an interrupt-forced or normal Branch and Store Instruction Register (BSI) instruction. These instructions effectively mask all interrupts during their execution and the execution of the next instruction.
2. The interrupt request level is masked. The request will be retained by the device adapter for recognition when the interrupt level is unmasked. Programmed interrupts are not retained if masked prior to the execution of the forced BSI instruction for that interrupt.
3. The interrupt request is on the same or lower priority level than an interrupt being serviced.

Programming Details

When an interrupt request is recognized, an interrupt-forced BSI instruction with indirect addressing is generated and executed. The address portion of the forced BSI instruction is unique for each interrupt level as shown in Figure 3-21. Program operation from this point is shown in Figure 3-24 and described in the following paragraphs. The circled numbers in Figure 3-24 correspond to the numbered descriptions.

(1) The interrupt request occurs during execution of the main line program.

(2) The forced BSI instruction with indirect addressing stores the contents of the I-register at the effective address (EA) and causes a branch to the interrupt subroutine at EA + 1. The EA is the address that the user stores at the interrupt vector.

(3) The interrupt subroutine stores all data and/or index registers that it will use. Prior to subroutine completion, the subroutine restores the same data and/or index registers.

(4) The last instruction of the interrupt subroutine is a Branch or Skip on Condition (BOSC) instruction (bit 9 = 1) that returns the program to the address previously stored at the EA of the forced BSI instruction (step 2). This address is the location of the next sequential instruction in the main line program. The BOSC instruction also resets the interrupt level so that other lower priority levels can be recognized.

If a Wait instruction is operative when the interrupt request occurs, the Wait instruction is considered complete when the interrupt request is recognized. Following completion of the interrupt subroutine, the instruction immediately following the Wait instruction is executed.

Interrupt Request Identification

Because a number of interrupt requests can be assigned to any one priority level it may be necessary for the program to analyze the ILSW of the requesting interrupt level to determine the source of the interrupt request signal. This analysis is

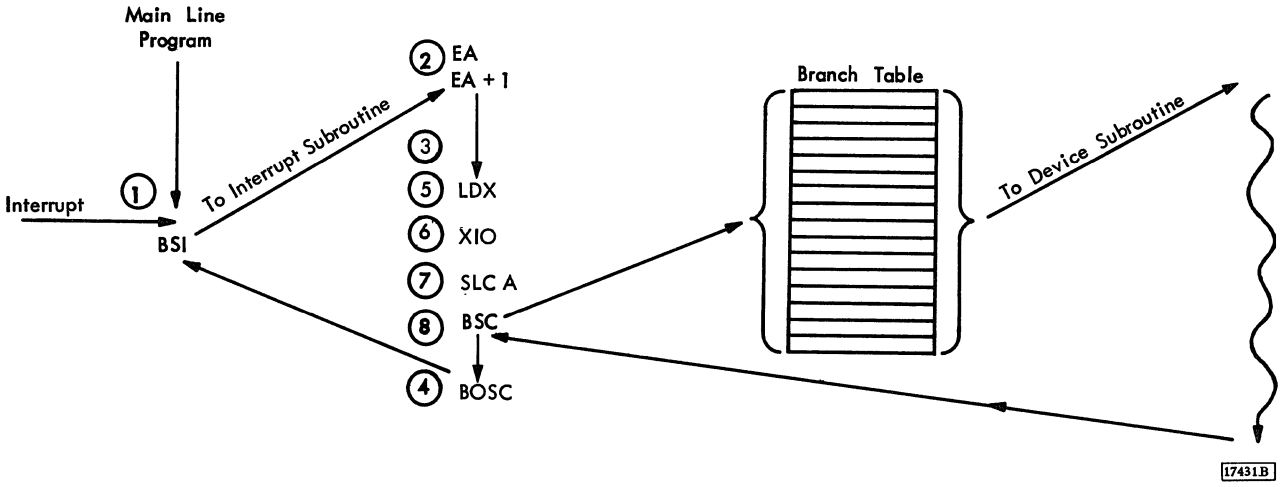


Figure 3-24. Program Identification of Interrupts

accomplished within the interrupt subroutine as described in the following paragraphs. (The numbered descriptions relate to the circled numbers in Figure 3-24.)

(5) A Load Index Register (LDX) instruction loads an index register with the number of interrupt request signals assigned to the ILSW.

(6) An XIO Sense Interrupt Level instruction causes the ILSW of the interrupt level being serviced (highest priority level on) to be set in the A-register. Only the function field of the IOCC need be specified. The other fields of the IOCC are not used. The status of the indicators in the devices or PISW's assigned to the ILSW are not affected.

(7) A Shift Left and Count A (SLCA) instruction is executed with the index register loaded in step 5 specifying the number of shift counts. The resulting count in the index register corresponds to the first non-zero ILSW bit in the A-register.

(8) A Branch or Skip on Condition (BSC) instruction with indirect addressing and indexing is executed. The index register used contains the count corresponding to the first non-zero bit in the A-register. The address portion of the BSC instruction contains the address of the first word of a branch table.

The branch table (Figure 3-25) consists of a table of addresses. Each address is related to an interrupt request position in the ILSW and specifies the location of a subroutine for that particular interrupt request. For example, if ILSW bit position zero is on (1), the last word of the branch table is used and the BSC branch is to the address stored in the last word of the table. If ILSW bit position one is on (1), the BSC branch is to the address stored in the next to the last word of the branch table, etc.

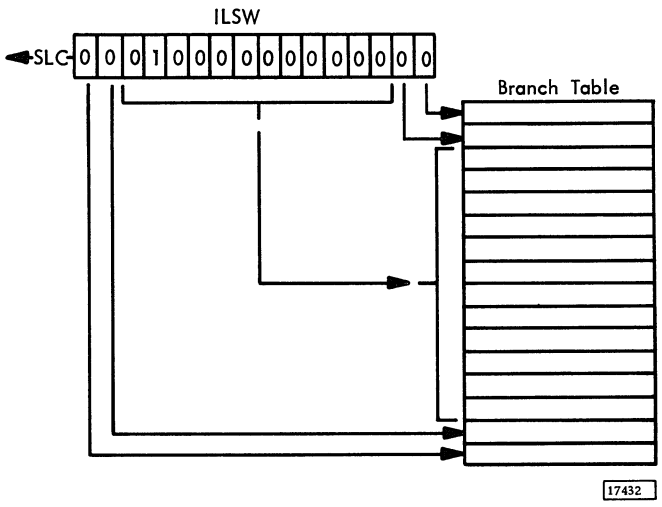
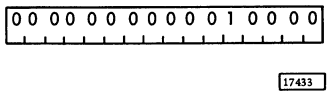


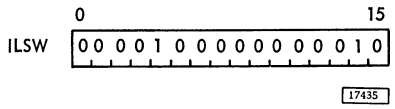
Figure 3-25. Figure ILSW Branch Table

EXAMPLE OF IDENTIFICATION: The preceding sequence of instructions locates the specific subroutine for the ILSW bit that initiated the interrupt. It should be noted that each time the A-register is shifted (step 7), the shift count is decreased by one. As the shift count is decreased, the indexed address for the BSC instruction is decreased. Effectively, the branch address of the BSC instruction begins with the address located in the last word of the branch table and progresses toward the first word of the branch table each time the A-register is shifted. The following is an example of interrupt request identification, with the circled numbers corresponding to those in Figure 3-24:

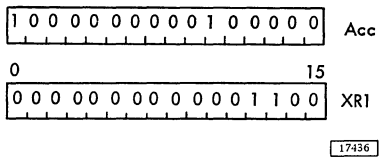
(5) Load Index Register: Index register one (XR1) is loaded with 16 or the maximum number of interrupt request signals connected to the level which caused the interrupt. (In this example, assume 16 request lines are connected to the interrupting level.) XR1 appears as shown in the following illustration.



(6) Execute I/O: The XIO instruction references a Sense Interrupt Level IOCC. This causes the ILSW of the interrupting priority level to be loaded into the A-register. The A-register (for this example) appears as follows:



(7) Shift Left and Count: This instruction normalizes the A-register and leaves a remainder count in the index register. Note in the following illustration that four shifts have reduced the value in XR1 from 16 to 12. Also note that bit position 8 and 9 in the index register are set to zero regardless of their previous status and bit position 0 through 7 remain unchanged.



(8) Branch or Skip on Condition. This instruction, with both indexing and indirect addressing, provides a branch to a subroutine. The location of the subroutine is specified by the EA of the instruction (the contents of a word in the branch table). The address of the desired word in the branch table is the sum of the address of the first word in the table (address portion of the instruction) and the contents of XR1 (12, in this example).

Device Indicator Identification

If the device or PISW requesting service has more than one possible interrupt condition, it is necessary for the program to determine which indicator in the DSW or PISW is responsible for the interrupt request. This identification can be made in almost the same manner as previously described in steps 5 through 8, with the following differences:

1. The LDX instruction (step 5) loads the index register with the maximum number of indicators assigned to the DSW or PISW instead of the number of interrupt request signals assigned to the ILSW.
2. An XIO Sense Device instruction is executed in step 6 instead of an XIO Sense Interrupt Level instruction. The area and/or modifier codes must specify the device or the status word.
3. SLCA and BSC instructions (steps 7 and 8) should be programmed so that all possible interrupting conditions are checked; i.e., even if one condition is on (1), the other conditions are not assumed to be off (0).

Interrupt Programming Notes

If an interrupt subroutine can be entered from more than one interrupt level, there can be a significant problem in loss of data (return addresses and intermediate subroutine results) unless care in programming is exercised.

It should also be noted that if only one device or PISW (one interrupt request signal) is assigned to an interrupt level, the program can be written so that only the DSW or PISW is read into the A-register and interrogated. Since only one interrupt request is assigned to the interrupt level, the ILSW need not be interrogated.

Chapter 4. Features

- A list of the IBM 1800 system special features is in Appendix B of this manual.

- An introduction to each of the following features is included in this chapter:
  System/360 to 1800 system adapter
  1800 system communications adapter
  1800 system selector channel

- P-C features that are expansions of the standard features are described with the standard features in this manual.

- Data processing I/O and process I/O features are described in the FE Theory of Operation manuals pertaining to those features.

System/360 Adapter

- Permits two-way exchange of data between the 1800 processor-controller and the System/360 (Model 25, 30, 40, 44, or 50).

- In the System/360, the adapter requires an available position of a multiplexor or selector channel.

- In the 1800 system, the data channel feature is required.

This feature provides the ability to transfer blocks of data between System/360 core storage and 1800 system core storage. Each system regards the other as an I/O device capable of requesting service on a random basis.

The adapter consists of standard SLT circuits of the 30-nsec family and, therefore, requires the three standard supply voltages: +3V, -3V, and +6V. The adapter is housed in, and powered from, the 1826 Data Adapter Unit, model 1 or model 2.

FUNCTIONAL DESCRIPTION

- The adapter has two device addresses, one of which responds to the System/360 and the other to the 1800 system.

- The adapter acts as a burst-mode control unit on the System/360 and performs in cycle-steal mode on the 1800 system data channel.

- Control command information, including modifier bits, from either system is loaded into the adapter buffer and made available to the other system by use of their respective sense commands.

Data transfers to or from the 1800 consist of one 16-bit word, and transfers to or from the System/360 channel consist of two eight-bit bytes. A sixteen bit (plus 2 parity bits) buffer register is provided in the adapter for serializing and deserializing the data bytes. The left-hand byte of the buffer, corresponding to the more significant byte of the 1800 word, is the first to be loaded or transferred over the System/360 channel.

A word count (1800) and a byte count (360) must be specified for a data transfer operation. Whichever count is least will terminate the transfer (one word count equals two byte counts). If the word count and byte count reach zero simultaneously, the 1800 will terminate the transfer. If the System/360 terminates with an odd byte count, the last byte will be lost. A word count of zero or a byte count of zero or one is invalid.

The priority of the System/360 Adapter is selected for the 1800 by assigning a particular interrupt level and a particular data channel priority to the device. Control unit priority for the System/360 is governed by its position on the channel.

If the System/360 wishes to stack attention, channel-end, or device-end, it may do so by responding to status-in with command-out.

Suppress-out may be used to keep the System/360 channel from being overrun during chain data operations, or at any time the channel needs to slow the operation for some other reason. The adapter will not request service from a channel while suppress-out is up.

SYSTEM/360 COMMANDS

The S/360 adapter decodes and responds to the following I/O commands from the S/360 program:

Start I/O (SIO).
Test I/O.
Halt I/O.

All valid command codes from the System/360 are acceptable to the adapter, hence undefined operations as established for each application must be rejected at the programming level in the 1800 system. The System/360 Adapter rejects undefined command functions from the 1800 and identifies this occurrence by a command-reject status bit presented in the device status word.

Start I/O

The 'start-I/O' command references a channel command word (CCW) which is similar in function to the IOCC in the 1800. The CCW's can be chained, allowing one SIO to initiate more than one I/O operation. Each CCW defines the command as being one of the following commands:

XXXXXM01	Write
XXXXXM10	Read
XXXXX111	Control Immediate
XXXX0 100	Sense
XXXX1 100	Read Backward
XXXXX 011	No Operation

The M-bit modifier = 1 in the read and write commands is used to suppress the 1800 interrupt normally caused by a System/360 command when loaded into the buffer. See timing chart (FV70101) and flow chart (FV60130) for initial selection sequence.

Control Immediate

Control, as used with the adapter, is always an immediate command. This means that channel-end status is sent to the System/360 channel in response to the initial command-out if the command is accepted, thus freeing the channel during the start-I/O operation if a chain flag was not present. A control command may be rejected because the 1800 system had previously commanded the adapter with an initialize-read or initialize-write.

The modifier bits in the control command byte may be used to communicate the particular type of transfer requested by the System/360. The control command is normally chained to a subsequent read or write command as required, to complete the transfer. See flow chart (FV60130).

CONTROL TO IDLE ADAPTER: Control-immediate is used as the initial command in a System/360 initiated data transfer. The complete control command byte, including modifiers, is latched in the adapter buffer. The adapter responds to the command with channel-end status and initiates an interrupt in the 1800. After identifying the source of the interrupt, the 1800 executes a sense-device command which loads its accumulator with the device status word containing the System/360 command byte from the buffer, then the adapter sends a device-end status to the System/360.

CONTROL TO BUSY ADAPTER: There are three busy responses to a System/360 control command:

1. Busy status alone is the response to the control command if the System/360 channel has previously issued a control command that is still latched in the adapter.
2. Busy and device-end status is the response to a control command if a previously issued control command has been cleared but the device-end has not yet been accepted by the System/360 channel. This clears the device-end status and leaves the adapter idle.
3. Busy and attention status is the response to a control command from System/360 if the 1800 has previously issued an initialize-read or initialize-write. The attention, after being accepted in this way, no longer attempts to interrupt the System/360; but if another command, such as control, is issued from System/360, the response will still be busy and attention.

Sense

The sense command is the normal System/360 response to attention status resulting from an 1800 initiated transfer. The sense command places in core storage, at the address specified in the CCW, one or two eight-bit bytes of sense data under control of the byte count.

The sense data (Figure 4-1) consists of the contents of the System/360 Adapter buffer latches. The System/360 channel receives an initial status of zero and an ending status of device-end and channel-end. If the adapter contains an uncomplemented 1800 command (an initialize read or initialize-write that has not yet been serviced by the System/360 channel), the ending status will also include attention.

Command Previously Issued from 1800	High-Order Buffer (A)		Low-Order Buffer (B)
	Byte 1		Byte 2
	Area	Fctn	Modifier
Initialize-Read	0 1 1 0 1	1 1 0	X X X X X X X X
Initialize-Write	0 1 1 0 1	1 0 1	X X X X X X X X
Control	0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0
Adapter Idle	Undefined		

24268A

Figure 4-1. Sense Data Presented to Adapter from 1800 System

The only exception is encountered when the System/360 issues a sense command to the adapter before a previous control from the System/360 channel has been cleared. If the control has not been answered by a sense command from the 1800, then the System/360 sense command receives a busy status in response. If the control has been answered, but the device-end has not been taken, or has been stacked , then the System/360 sense command receives busy and device-end status. This clears the device-end from the adapter and leaves it idle. See flow chart (FV60140).

Read or Read Backward

The adapter controls recognize no difference between read and read-backward from the System/360 channel. In both cases, the primary function of the adapter is the transmission of data bytes to the System/360 from the 1800. See flow chart (FV60145).

READ TO IDLE ADAPTER: When the read command is issued to an idle adapter, the System/360 channel receives zero status response and then holds up until the 1800 executes an initialize-write command. An interrupt is immediately set up to signal the 1800 that an operation is waiting, unless suppressed with the M bit. The complete read command byte is latched in the adapter buffer and is available to a sense-device command from 1800. Note that the M bit cannot be used with the read-backward command.

READ TO A WAITING INITIALIZE-WRITE: If a read issued by System/360 encounters a previously issued initialize-write from the 1800, both operations are performed. The System/360 channel receives zero status from the adapter. The operation continues until either the System/360 responds to its service-in with a stop command (byte count reduced to zero), or the adapter word count is reduced to zero with no 1800 data chaining indicated.

When a stop command is received from the System/360 or the word counter reaches 0, status containing channel-end and device-end is issued to the System/360 channel. The acceptance of the status by the System/360 channel frees the adapter and returns it to idle.

READ TO BUSY ADAPTER: There are three busy responses to a System/360 read command:

1. Busy status is the response to the read command if the System/360 has previously issued a control command that is still in the adapter.
2. Busy and device-end status is the response to a read command if a previously issued control command has been cleared but the device-end has not been accepted. This clears the device-end and leaves the adapter idle.
3. Busy and attention status is the response to a read command from System/360 if the 1800 has previously issued an initialize-read. If the attention has not been previously accepted by the System/360 channel, this clears it as an interrupting condition, although it will continue to appear as a response to further read commands until the initialize-read is satisfied.

Write

The primary function of the System/360 Adapter on a write command is the transmission of data from the System/360 to the 1800. The operation of the write command is similar to the read command except for the direction of transfer. See flow chart (FV60150) and timing chart (FV70120).

WRITE TO IDLE ADAPTER: When the write command is issued to an idle adapter, the System/360 channel receives zero status response and then holds up until the 1800 executes an initialize-read command. An interrupt is immediately set up to signal the 1800 that an operation is waiting, unless the interrupt has been suppressed with the M bit. The complete write command byte is latched in the adapter buffer and is available to a sense command from the 1800.

WRITE TO A WAITING INITIALIZE-READ: If a write command issued by System/360 encounters a previously issued initialize-read from the 1800, both operations will be performed. The System/360 channel receives zero status. The operation continues until System/360 responds to a service-in with a stop command (byte count reduced to zero) or the adapter word count is reduced to zero with no 1800 data chaining indicated.

When the byte count, or the adapter word count, is reduced to zero, status containing channel-end

and device-end is issued to the System/360 channel. The acceptance of the status by the System/360 channel frees the adapter and returns it to idle.

WRITE TO BUSY ADAPTER: There are three busy responses to a write command issued by the System/360 channel:

1. Busy status is the response to the write command if a previously issued control command is still in the adapter.
2. Busy and device-end status is the response to a write command if a previously issued control command has been cleared but the device-end has not been accepted. This clears the device-end and leaves the adapter idle.
3. Busy and attention status is the response to a write command from System/360 if the 1800 has previously issued an initialize-write. If the attention has not been previously accepted by the System/360 channel, this clears it as an interrupting condition, although it will continue to appear as a response to further write commands until the initialize-write is satisfied.

Test I/O

A test-I/O may be used by the programmer to determine the status of the System/360 Adapter any time the channel is free. The status received indicates the condition of the adapter as follows:

1. Zero status indicates that the adapter was idle at the time of response.
2. Busy status indicates that a control previously issued has not been accepted by the 1800 channel.
3. Attention status indicates that the 1800 has previously issued an initialize-read or initialize-write.
4. Device-end status indicates that a previously issued control has been accepted, but that the final interrupting condition has not been accepted by the System/360 channel. This clears the device-end status and leaves the adapter idle.
5. Channel-end and device-end status indicates that a data transfer has been terminated but that the final interrupting condition has not been accepted. This clears the status and leaves the adapter idle.

No-Operation

The no-operation command as used with the System/360 Adapter does not affect the contents of the adapter latches. It is always handled as an immediate command.

NO-OPERATION TO IDLE ADAPTER: If a no-op command is issued to an idle adapter, the System/360 channel receives a status response containing channel-end and device-end. No interrupt occurs in the 1800.

NO-OPERATION TO BUSY ADAPTER: There are three busy responses to a no-operation from the System/360 channel:

1. Busy status is the response to the no-op command if a previously issued control command is still in the adapter.
2. Busy and device-end status is the response to a no-op command if a previously issued control command has been cleared but the device-end has not been accepted by the System/360 channel. This clears the device-end status and leaves the adapter idle.
3. Busy and attention status is the response to a no-op command from System/360 if the 1800 has previously issued an initialize-read or initialize-write.

Halt I/O

When the System/360 Adapter recognizes the halt-I/O condition, its response is immediate. It terminates the operation, sets channel-end and device-end in its status, and waits for a chance to send the status to the System/360 channel. The 1800 receives halt status via interrupt and the sense command.

If halt-I/O is issued while an unserviced System/360 control is latched in the adapter, the control will be busy-rejected. If halt-I/O is issued to an idle adapter, no status is developed.

1800 SYSTEM COMMANDS

- Reference FV60110 (flow chart).

The System/360 Adapter decodes and responds to the following 1800 system commands:

101	Initialize-Write
110	Initialize-Read
111	Sense Device
011	Sense Interrupt
100	Control (Blast Reset)

The adapter rejects undefined command functions from the 1800 and identifies this occurrence by the command-reject status bit presented in the sense word.

Sense Device Status Word

- Reference FV60120 (flow chart) and FV70140 (timing chart).

An unmodified sense-device command ("zero" in bit 8 of the control word) to the adapter causes the device status (8 bits) and the current contents of the low-order buffer (8 bits) to be placed in the sense word for transfer to the P-C accumulator. The sense data presented under alternative conditions are listed in Figure 4-2.

Sense Word Count

- Reference FV60120 (flow chart) and FV70140 (timing chart).

A modified sense-device command ("one" in bit 8 of the control word) causes the current word count of the 1800 data channel (14 bits) to be placed in the sense word in true binary form for transfer to the P-C accumulator.

Sense Interrupt

- Reference FV70140 (timing chart) and FV60110 (flow chart).

The 1800 responds to the adapter interrupt by executing a sense-interrupt command to identify the source of the interrupt. Having established the adapter as the source of the interrupt, the 1800 program issues a sense-device command (unmodified) to the adapter to identify the specific interrupting condition.

Initialize-Read

- Reference FV70110 (timing chart) and FV60110 (flow chart).

Command Previously Issued from S/360	Device Status Word	Low-Order Buffer (B) Command Byte
Read	0 0 1 0 0 0 0 0	X X X X X M 1 0
Read Backward	0 0 1 0 0 0 0 0	X X X X 1 1 0 0
Write	0 0 1 0 0 0 0 0	X X X X X M 0 1
Control	0 0 1 0 0 0 0 0	X X X X X 1 1 1
Adapter Idle	Undefined	

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Figure 4-2. Sense Data Presented to Adapter from System/360

INITIALIZE-READ TO IDLE ADAPTER: Execution of this function latches the 16-bit control word of the IOCC containing the area, function, and modifier into the adapter buffer, loads the adapter word counter and scan control latches, and raises attention status to notify the System/360 that an operation is waiting.

INITIALIZE-READ TO A WAITING WRITE: This command, issued in conjunction with a write command from the System/360, loads word counter and initiates data transfer from the System/360 to the 1800. The operation continues until either the System/360 byte count is zeroed or the adapter word count is zeroed. Terminating status is transfer-end. If the System/360 byte count goes to zero before the adapter word count, terminating status will also contain halt.

INITIALIZE-READ TO BUSY ADAPTER: There are two busy responses to an initialize-read command:

1. Busy rejection is caused by issuing the command to a previously issued uncompleted command from the 1800. The condition can be interrogated with a sense-device command which will indicate command-reject and 1800-command-stored status.
2. An initialize-read to the adapter which contains a previously issued System/360 read or control command will be rejected and will indicate command-reject and 360-command-stored status.

Initialize-Write

- Reference RV70110 (timing chart) and FV60110 (flow chart).

Issued to a waiting read command from the System/360, initialize-write loads the adapter word counter and initiates data transfer. If the adapter is idle, attention status is raised and the buffer is loaded with the IOCC control word. Busy responses are as indicated under initialize-read with the read/write relationships reversed.

Control

The control function provides the Customer Engineer with a means of re-cycling a failing operation when

servicing the System/360 Adapter. Execution of this function resets the adapter (including the CS-request flip-flop) in the same manner as a selective reset (System/360) or a master reset (System/360 or 1800). The adapter is not available to either system for the duration of the reset.

If the System/360 is using the adapter at the time of reset, an interface control check may occur in the System/360. See flow chart (FV60110).

DEVICE STATUS

System/360 Status Byte

The System/360 Adapter presents the following device status information to the System/360:

Status Condition	System/360 Status Byte Bit Position
Attention	0
Busy	3
Channel End	4
Device End	5

The status definition and use of those bits presented to the System/360 are as defined in the System/360 Field Engineering Theory of Operation manual.

Attention (bit 0), when on, indicates that a prior read or write command function has been issued from the 1800 but has not yet been recognized by the System/360 channel.

Busy (bit 3) is off when the System/360 Adapter is idle. Busy-on indicates that the device has been selected by the System/360 and either an operation is pending or a transfer is in progress.

Channel End (bit 4) is presented to the System/360 channel during initial selection sequence for control-immediate or no-op, or with device-end during the ending sequence for all others.

Device End (bit 5) is presented to the System/360 channel during initial selection sequence for no-op, or after an 1800 sense command response to control-immediate, or at the end of the data transfer for all others.

1800 Device Status Word

The System/360 Adapter presents the following status information to a sense command from the 1800:

Status Condition	DSW Bit Position
Command Reject*	0
1800 Command Stored	1
360 Command Stored*	2
Halt*	3
Data Check*	4
Storage Protect*	5
Transfer End*	6
End of Table*	7
360 Command Byte	8 - 15

*Interrupting Condition

Command Reject (bit 0), when on, indicates that the System/360 Adapter refused an 1800 command for one of the following reasons:

1. Invalid op code.
2. An initialize-read or initialize-write was issued before a previous initialize-read or initialize-write had been cleared.
3. An initialize-read was issued after the System/360 had issued a read or control command.
4. An initialize-write was sent after the System/360 had issued a write or control command.

Command reject causes an unconditional 1800 interrupt. It also causes an 1800 internal interrupt due to CAR-check failure. This indicator is reset after an 1800 sense-device command with bit 15 on.

1800 Command Stored (bit 1) turns on when the System/360 Adapter has accepted an initialize-read or initialize-write from the 1800. It is reset when transfer-end occurs.

360 Command Stored (bit 2), when on, indicates that the System/360 has issued a read, read-backward, write, or control command which was accepted by the System/360 adapter.

This is a conditional interrupt because the indicator may be turned on without causing an interrupt if the M bit is set in a System/360 read or write command, or if a read, read-backward, or write command was preceded by a complementary 1800 command (status bit 1 on). The interrupting condition can be cleared by an 1800 sense-device command with bit 15 on.

If the System/360 command was read, read-backward, or write, this indicator remains on until transfer-end occurs. If the command was control, this indicator is turned off after an 1800 sense-device command with bit 15 on.

Halt (bit 3) turns on and causes an unconditional 1800 interrupt if the System/360 stops data transfer with either a normal stop or an interface disconnect sequence. Bit 6 (transfer-end) will also be on. This indicator is reset after an 1800 sense-device command with bit 15 on.

Data Check (bit 4) indicates that the 1800 detected a parity error during a cycle-steal or the adapter detected a System/360 bus-out parity error. The data check causes an unconditional interrupt in the 1800 and is reset by an 1800 sense-device command with bit 15 on.

If the error is detected during the first cycle-steal of the operation (load-word-count cycle) and there is no complementary System/360 command stored, the adapter is reset and the 1800 can reinitialize the data transfer operation.

If a parity error is detected during any subsequent cycle of the operation, an immediate ending procedure is initiated. The adapter issues device-end and channel-end to the System/360, and data-check and transfer-end to the 1800.

If incorrect parity is detected during the control or data cycle, the adapter ignores the command. The data check indicator does not turn on, but an 1800 internal error results.

Storage Protect (bit 5), when on, indicates that the System/360 attempted to store data in a protected area of 1800 core storage on a System/360 write/1800 read data transfer cycle. This causes the System/360 Adapter to initiate an ending procedure, sending channel-end and device-end to the System/360, and storage-protect and transfer-end to the 1800. An unconditional interrupt is given to the 1800. This indicator is reset by an 1800 sense-device command with bit 15 on.

Transfer End (bit 6), when on, indicates that no additional data is to be transferred. This status can result from any of the following conditions:

1. The 1800 word count goes to zero and no chaining is indicated.
2. The System/360 responds to service-in with command-out (byte count = zero).
3. The System/360 issues a halt-I/O instruction or executes an interface-disconnect sequence.
4. Parity error is detected.
5. A storage protect violation has occurred.

Transfer-end causes an unconditional 1800 interrupt. It is reset by an 1800 sense-device command with bit 15 on. (An 1800 initialize-read or write is rejected if the transfer-end status is on.) The '360 command stored' (bit 2) may be on at the same time, indicating that the System/360 has initiated a new command.

End of Table (bit 7) turns on and causes an 1800 interrupt during the cycle-steal that the 1800 word count goes to zero, but only if requested by the scan-control bits in the first word of the 1800 data table.

End-of-table status is reset by an 1800 sense-device command with bit 15 on.

System/360 Command Byte (bits 8-15). If bit 2 is on ('360 command stored') and bit 1 is off (no 1800 command stored), these eight bits contain the issued System/360 command byte. (See Figure 4-2.)

Communications Adapter

DESCRIPTION

- Allows communication between an 1800 system and other devices or systems in binary synchronous communications (BSC) mode.
- Can control the operation of two line adapters concurrently.
- Uses one or two data channels of the 1800 system.

The communications adapter (CA) includes the SLT circuits required to control communication in BSC with these other devices or systems:

A System/360 via a 2701 data adapter unit with the synchronous data adapter II feature.
A System/360 via a 2703 transmission control unit with synchronous features.
A System/360 model 25 via the integrated communications attachment equipped for synchronous operation.
Another 1800 system with a CA.
An 1130 with its synchronous communications adapter operating in BSC mode.
A 2770 data communications system.
A 2780 data transmission terminal.

Each CA can control one or two line adapters, and up to four communications adapters can be included in an 1800 system. A data channel of the 1800 system is required for each line adapter which is to be included in the system. The maintenance diagram manual MA10101 shows system data flow as well as other information concerning adapter limitations and requirements.

Additional information concerning BSC operations and data communications in general is included in the following manuals:

IBM Communications Primer, Order No. C20-1668.
IBM Binary Synchronous Communications, Order No. GA27-3004

Additional information concerning the 1800 communications adapter is included in the following manuals:

IBM 1800 Functional Characteristics, Order No. GA26-5918
IBM Field Engineering Maintenance Diagrams, 1800 Data Acquisition and Control System, Volume 2-FV through YD, Order No. SY26-4129

TRANSMISSION CODES

- Extended binary-coded-decimal interchange code (EBCDIC) or American standard code for information interchange (ASCII) is used.
- For 1800 CA operation, the ASCII code has a parity position added.

The CA operates on the basis of eight-bit characters which are set into 1800 core storage two per word. Code charts for both codes which can be used are shown on MA10131. If a CA is controlling two line adapters, both line adapters must use the same transmission code. However, if the system has more than one CA, it is not required that all CA's use the same transmission code.

EBCDIC has eight bit positions in its standard form, and any character can have either an even or odd number of 1's. ASCII, in its standard form, contains seven bit positions. For 1800 CA operations, an eighth position is added. The eighth position is set to 1 only when the other seven positions contain an even number of 1's. Consequently, ASCII characters processed by the CA always have an odd number of 1's.

CONTROL CHARACTERS AND SEQUENCES

- Control characters and sequences, as well as program instructions, control the operations of the CA.

Certain characters and sequences (two characters each) can be sensed by the CA circuits. The functions of these characters and sequences (MA10141) are described in the following paragraphs.

SYN--SYNCHRONOUS IDLE: Used by the CA to establish and maintain synchronism in the absence of any other character.

SOH--START OF HEADING: Precedes a block of heading data. The CA performs the same functions as when sensing an STX character. Any special processing of heading data is under program control.

STX--START OF TEXT: Precedes a block of text data. The first STX (or SOH if there is heading data) in a message establishes text mode. Any later SOH or STX is processed as regular data, unless the program directs otherwise.

ITB--INTERMEDIATE TRANSMISSION BLOCK: Indicates the end of a block of heading or text data. The block check character (BCC) follows the ITB character, but no change occurs in the direction

of transmission. In other words, no "turnaround" occurs following an ITB.

ETB--END OF TRANSMISSION BLOCK: Indicates the end of a block of text data. The BCC follows the ETB, and a turnaround occurs. The station that had been receiving a message is expected to transmit an acknowledgement after receiving the BCC.

ETX--END OF TEXT: In the 1800 system CA, accomplishes the same functions as an ETB. However, ETX is usually used only at the end of the last text data of a message. The BCC follows an ETX and turnaround occurs.

EOT--END OF TRANSMISSION: Indicates the conclusion of a message transmission. Decoding this character when the CA is in text mode has no effect. EOT is used after acknowledgement of the receipt of the last text data.

ENQ--ENQUIRY: Used as a request for a response that indicates the remote station status. No BCC follows the ENQ, but a turnaround is expected.

NAK--NEGATIVE ACKNOWLEDGEMENT: Indicates that the previous block of data was unacceptable and that the receiver is ready to accept a retransmission of the erroneous block. It is also the not ready reply to a station selection. Like EOT, decoding this character when the CA is in text mode has no effect.

DLE--DATA LINK ESCAPE: Used as the first character in two-character sequences that provide additional line-control functions. For example, DLE STX initiates transparent text and DLE followed by ETX, ETB, ITB, or ENQ terminates transparent text. In the latter instance, the sequence must be located at the end of the data table.

PAD CHARACTERS: Two are used by the CA. The pre-SYN pads are provided by the CA circuits (bit configuration 01010101 or hex 55) and precede the SYN characters at the start of a message. The ending pad (bit configuration 11111111 or hex FF) must be placed in the transmit data table and follows any turnaround character or sequence.

DLE STICK SEQUENCES: Consist of a DLE followed by a stick character. Decoding the stick character (see chart, MA10131) when the CA is in text mode has no effect. In non-text mode, a DLE stick sequence causes an end to the current operation. Any further use of the sequence is dependent on the program.

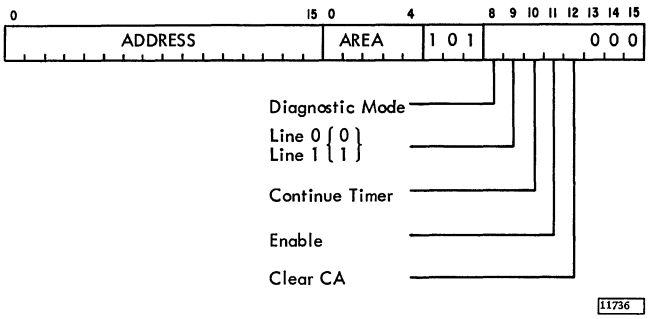
INPUT/OUTPUT CONTROL COMMANDS

- Operations of the CA are initiated by execute input/output (XIO) instructions in the processor-controller (P-C) program.
- Three input/output control commands (IOCC's) are used for the CA--initialize, sense interrupt, and sense device.

Execution of an XIO instruction in the P-C program obtains the two-word IOCC from core storage during the XIO control cycle and the XIO data cycle. This is the standard operation of the P-C. Only three IOCC's are required, in addition to the control characters and sequences appearing within the data, to control the operation of the CA.

Initialize CA

The IOCC sets up the circuits of the CA to start an operation. In addition, during the XIO data cycle, a cycle-steal request calls for the transfer of the byte count word from core storage to the CA. The format of the IOCC is:



A description of each part of the IOCC follows:

ADDRESS: This field (a complete word), located at an even core location, contains the core storage address of the first word of the data table, which is the byte count word.

AREA: The area code specifies which CA is to respond. The area codes are assigned as follows:

CA	Code
1	21 (10101)
2	22 (10110)
3	23 (10111)
4	20 (10100)

FUNCTION: 101 - Three-bit field that designates an initialize operation.

MODIFIER: The modifier bits expand the Initialize CA command as follows:

Bit 8 Diagnostic Mode: When bit 8 is a 1, the operation of the CA is changed as follows:

1. The send data line to the data set is also looped back to the input of SERDES in transmit mode.
2. All characters are read from or stored in the low order core bits 8-15.
3. After each character while transmitting, and before each character while receiving, the diagnostic DSW word is stored. This is accomplished automatically by the adapter on a cycle-steal basis.

MA30306 shows the setup of diagnostic transmit and receive data tables.

Bit 9 Line Selection: When bit 9 is a 0, line 0 is designated; when bit 9 is a 1, line 1 is designated.

Bit 10 Continue Timer: When bit 10 is a 1, the 3-second timeout is changed to 2 seconds and the timer is started. This new timeout period remains effective until:

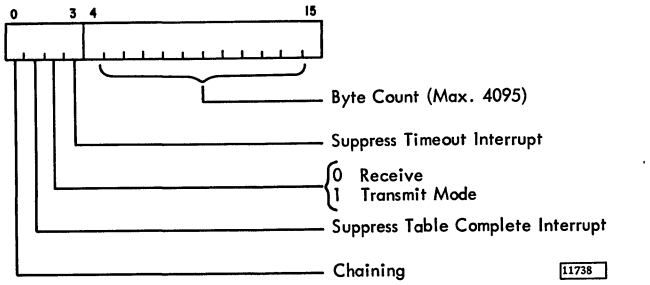
1. A timeout interrupt occurs.
2. A change from receive to transmit, or vice versa, occurs.
3. A Clear CA is given.

Note: A cold start Initialize CA command or an Initialize CA command that changes modes resets the continue timer. Continue Timer is used when the program is not ready to send or receive the next record. In the case of a transmit, as a master station, the program should send TTD after the timeout. In case of a receive, as a slave station, WACK should be sent.

Bit 11 Enable: The action of this bit is covered under the 'sense device' command.

Bit 12 Clear CA: When on (1), this bit resets selected triggers and latches in the addressed line adapter to enable a restart from a known condition. The contents of serdes, which are readable by a 'sense device' command, are not reset by this command.

After the XIO data cycle, when cycle-steal priority allows, a cycle-steal (CS) cycle occurs. The address from the channel address register (CAR) is used to address core storage. This is standard data channel operation. In this first CS cycle, the byte count word is available to the CA on the out bus. The format of the byte count word is:



A description of the contents of the byte count word follows:

CHAINING-BIT 0: When this bit is a 1, an automatic chain to a new table occurs when the end of table is reached. The last word of the "chained-from" table must contain the address of the "chained-to" table. The first word of the "chained-to" table must contain its own address. A hardware check is made on this first word. If it is not its own address, a CAR check occurs. The second word of the new table is a new byte count word. The chain rules are shown on MA30156.

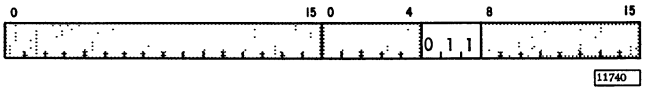
SUPPRESS TABLE COMPLETE INTERRUPT-BIT 1: When this bit is a 1, the table complete interrupt does not occur when the byte count goes to zero.

RECEIVE/TRANSMIT-BIT 2: When this bit is a 1, the CA is conditioned for transmit mode and characters are sent to the data set. When this bit is a 0, the CA is conditioned for receive mode and characters are received from the data set.

SUPPRESS TIMEOUT INTERRUPT-BIT 3: When this bit is a 1, no timeout interrupt can occur before the next turnaround.

BYTE COUNT-BITS 4-15: The byte count is set to the number of 8-bit characters in the table. All characters including the pad and "anything" characters are counted. If an odd byte count is specified, the first character (bits 0-7) after the byte count word is not used or counted and may be anything. Maximum byte count is 4095_{10}.

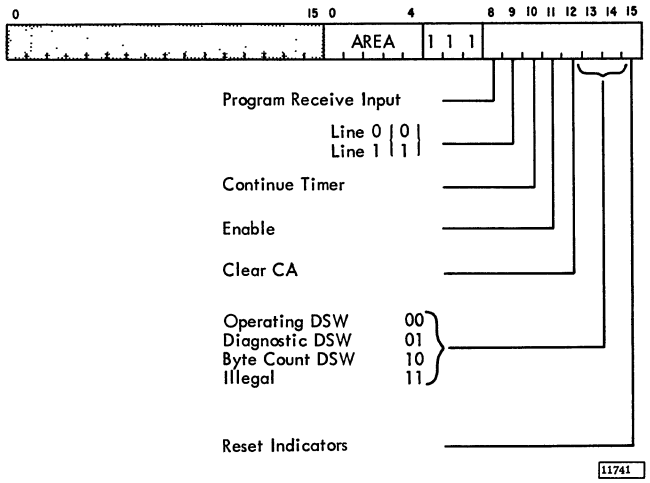
Sense Interrupt



This command loads the interrupt level status word (ILSW) of the highest priority interrupt pending into the accumulator. If the CA is controlling two line adapters, both are assigned to the same level, which is predetermined by the customer. In the ILSW each line adapter is assigned a bit position, also predetermined by the customer. Thus the line adapter which caused the interrupt is indicated in the ILSW by a 1 in its assigned position.

Sense Device

This IOCC causes loading of one of the three device status words (DSW's) into the P-C accumulator. In addition other functions can be accomplished as selected by the modifier bits. The format of the IOCC is:



A description of the IOCC follows. Note that three of the modifier bits (9, 10, and 11) have the same meaning in a sense device command as in an initialize command.

FIRST WORD: Not used in execution of this command. In the XIO data cycle, the selected DSW is set in the P-C accumulator.

AREA: Selects the CA for which the DSW is to be sensed or the operation modified.

FUNCTION: 111- This code specifies the 'sense device' command.

MODIFIERS: The modifiers expand the 'sense device' command as follows:

Bit 8 — Programmed Receive Input: This bit position provides program control of the receive data line for the selected line adapter by complementing a flip-flop (FF) in the circuits. The FF is cleared to its off position, so the first command with bit 8=1 turns on the 'programmed receive input' FF. The FF being on causes a space (0) level on the receive data line. Each later command with bit 8=1 changes the state of the 'programmed receive input' FF. Thus the receive input data can be controlled with a series of commands appropriately timed.

Note: The data set cable switch must be in the test position if interference with actual input data is to be avoided.

Bit 9 — Line Selection: 0=line 0; 1=line 1.

Bit 10 — Continue Timer: Action of this bit is identical to its use in the 'initialize CA' command.

Bit 11 — Enable: When bit 11 is a 1, a latch is set on, which "enables" the line adapter. While "enable" is active, an 'end-character or ringing' interrupt occurs when the data set indicates a ringing condition and the CA is not initialized. This latch is turned off by issuing another sense command with bit 11 off (0) and bit 15 on (1).

Note: If the line adapter is initialized, a ringing interrupt cannot occur. This function is therefore prevented when attempted with the 'initialize CA' command.

Bit 12 — Clear CA: This bit performs the same function as it does when given during the 'initialize CA' command. In addition,

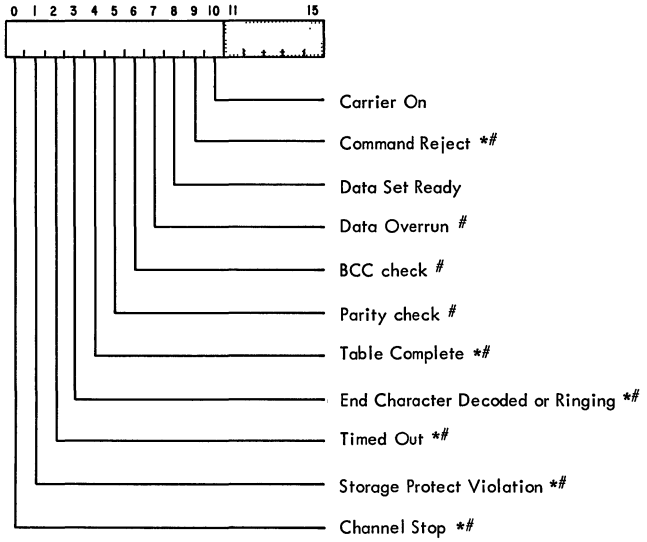
the data set will go "on hook" (data set ready reset) when a switched network is being used. The actual reset of the data set ready line is dependent on the delay encountered with the type of data set used.

Bits 13 and 14 — DSW Selection: These bits determine which DSW is loaded into the P-C accumulator as follows:

13	14	DSW
0	0	Operating
0	1	Diagnostic
1	0	Byte Count
1	1	Illegal

Bit 15 — Reset Indicators: If this bit is a 1 when the sense operating DSW is given, the latches associated with bits 0 through 7 and bit 9 are reset.

Operating DSW



* Causes Interrupt.

\# Indicator reset by a sense DSW (Other indicators are reset by their status turnoff).

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When bits 13 and 14 of the 'sense device' command select the operating DSW, it is set into the P-C accumulator as shown. The significance of a 1 in the indicated positions of the operating DSW is described in the following paragraphs.

CHANNEL STOP-BIT 0: Indicates that a parity error, a CAR check error, or a storage protect violation has turned on the 'channel stop' flip-latch (FL). CS cycles are prevented and an interrupt is requested.

STORAGE PROTECT VIOLATION-BIT 1: This indicator is turned on and causes a channel stop interrupt when the CA tries to store received data into a storage protected word of core.

TIMEOUT-BIT 2: This indicator is turned on and causes an interrupt if a double SYN or DLE SYN is not detected for 3 seconds after CA initialization, or SYN's or DLE SYN's have been on a line continuously for over 3 seconds, in normal mode or transparent mode respectively.

A timeout also occurs in 3 seconds in transmit mode if the 'clear to send' line is not activated by the data set in response to the 'request to send' signal. If continue timer was previously specified, the timeout occurs in 2 seconds. The timeout also occurs if a table complete with no chaining condition exists in transmit mode, and a receive table has not been initiated.

The timeout interrupt can be suppressed within a data table by setting a 1 in bit 3 position of the corresponding byte count word.

END CHARACTER DECODED OR RINGING-BIT 3: Indicates that the 'end character or ringing' FL is on, and an interrupt has been requested. This flip-latch can be turned on by either of two means.

1. Detection of a turnaround character during a receive operation. The interrupt is delayed until after the pad character is stored. Turnaround characters are ENQ, NAK, DLE STICK, EOT, ETX and ETB. For EOT and NAK, at least four 1's of the following pad character must be received for the character to be recognized as a turnaround.

   DLE STICK, EOT and NAK do not cause an interrupt if they appear in text after SOH/STX is received. After the pad character is stored, further CS requests by the same line adapter are prevented. The remaining byte count can be used to calculate the location the turnaround character in storage.
2. A ring indicator signal from the data set if the CA is enabled and not initialized. If the CA is in the initialized state, the ring indicator signal cannot turn on the 'end character or ringing' FL.

For the program to know which condition (turnaround or ring indicator) turned on the flip-latch, the program must keep track of whether or not the CA is initialized.

Note: The CA (line adapter) must be initialized or disabled before a ringing interrupt can be reset by the 'sense device' command. (This inhibits the ring indicator from causing another interrupt.)

TABLE COMPLETE-BIT 4: Indicates that the byte count reaching 0 has turned on the 'table complete' FL and caused an interrupt request. This action can be suppressed by a 1 in bit position 1 of the byte count word at the start of the table.

In a receive operation, 'end character or ringing' and 'table complete' can be turned on at the same time, if the data table ends with the pad character as the last byte. Therefore, determining the location of the end character may be difficult when chaining receive data tables.

DATA PARITY CHECK-BIT 5: This indicator is turned on when a parity error is detected during core storage data transfers or when a VRC error is detected in ASCII mode.

In ASCII mode, a transmit or receive VRC error sets this bit on. The detection of the VRC error blocks the loading of the accumulated BCC to the line during a transmit. Transmission continues, but the BCC sent contains all 1's which the receiving station detects as an error.

DATA BCC CHECK-BIT 6: This indicator is turned on if a BCC error is detected when the accumulated BCC's are compared with the incoming (received) BCC's. For EBCDIC, the BCC's are 2 CRC characters (16 bits). For ASCII, the BCC is an LRC character (8 bits).

DATA OVERRUN-BIT 7: This bit is turned on if a cycle steal request for a character transfer is not acknowledged before an overrun condition occurs. An overrun occurs if the bit counter steps to 1 before the CS cycle required for data transfer occurs.

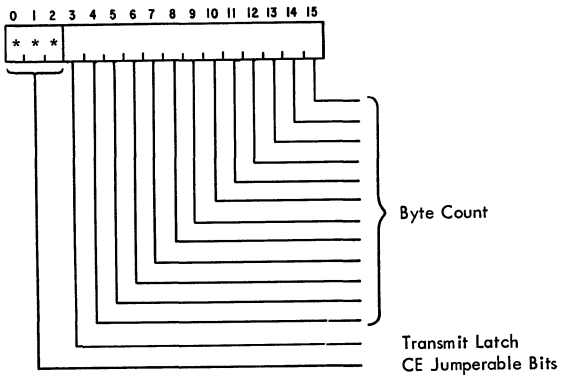
This error blocks the loading of the accumulated BCC to the line during transmit. Transmission continues, but the BCC sent contains all 1's which the receiving station detects as an error.

DATA SET READY-BIT 8: Indicates that the 'data set ready' line from the data set is activating the 'interlock' line in the CA.

COMMAND REJECT-BIT 9: This bit is set to 1 and causes an interrupt when the CA is given an 'initialize CA' command with the clear CA bit (bit 12) off while the line selected is either in transmit mode or in receive mode and character phase.

CARRIER ON-BIT 10: Indicates that the 'data carrier detector' line from the data set is activating the 'carrier on' line. For 4-wire networks, the bit is always on. For 2-wire switched networks, the bit is on only when a carrier is being received from a transmitting station.

Byte Count DSW



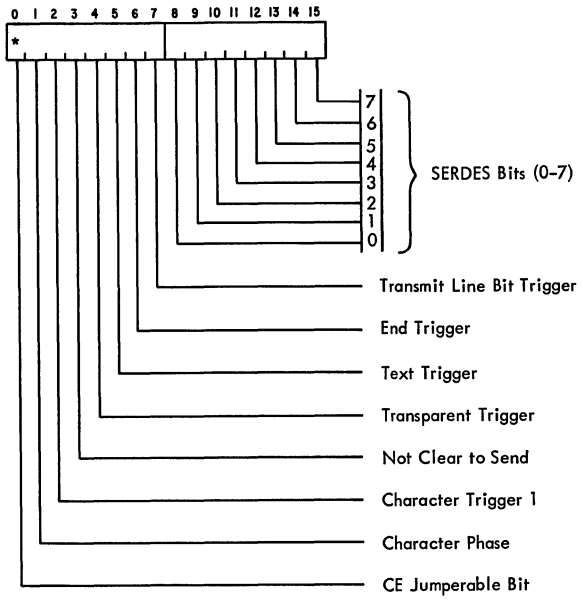
When bits 13 and 14 of the 'sense device' command select the byte count DSW, it is set into the P-C accumulator as shown. The significance of 1's is in the byte count DSW is described in the following paragraphs.

CE-JUMPERABLE BITS-BITS 0-2: These bits are available to the CE for diagnostic purposes. If they are unjumpered, they are read as 1's.

TRANSMIT LATCH-BIT 4: Indicates that the CA is in transmit mode when the DSW is sensed.

BYTE COUNT-BITS 4-15: Indicate the remaining byte count in 1's complement form at the time of the 'sense device' command.

Diagnostic DSW



When bits 13 and 14 of the 'sense device' command select the diagnostic DSW, it is set into the P-C accumulator as shown. This DSW has the same configuration as the DSW that is transferred automatically to the P-C for each character in a diagnostic mode operation. The significance of 1's in the diagnostic DSW is described in the following paragraphs.

CE JUMPERABLE BIT-BIT 0: This bit is available to the CE for diagnostic purposes. If not jumpered, it is read as a 1.

CHARACTER PHASE-BIT 1: Indicates that the CA is operating in character phase, when the 'sense device' command is given. In a transmit operation, character phase is not established until after sending the pre-SYN pad and SYN characters. In a receive operation, character phase starts after recognition of the first two consecutive SYN characters.

CHARACTER TRIGGER 1-BIT 2: Indicates the state of the units position flip-flop in the character counter (a two-position counter). This counter is held reset except when receiving or transmitting the following:

1. The initial Pre-SYN PAD and SYN characters.
2. SYN characters in the data stream.
3. Characters following an end character.

NOT CLEAR TO SEND-BIT 3: Indicates that the 'clear to send' line from the data set is not active. This position is a 1 at all times except when the data set is transmitting.

TRANSPARENT TRIGGER-BIT 4: Indicates that the CA is operating in transparent mode.

TEXT TRIGGER-BIT 5: Indicates that the CA is processing text data (data following an SOH or STX). After the first SOH or STX of a message has turned on the 'text trigger' FF, it remains on until the next turnaround or 'clear CA' command.

END TRIGGER-BIT 6: Indicates that an end character has been sensed in the data. The end character can be:

1. ETB, ETX, ITB, or ENQ in text data.
2. NAK, EOT, or DLE STICK in non-text data (not preceded by an SOH or STX).

In transparent mode, only the first four characters are sensed, and they must be preceded by a DLE character and in the proper data table location.

A character count of 3 during a data CSA cycle turns off the 'end trigger', or 'clear CA' command can also turn it off.

TRANSMIT LINE BIT TRIGGER-BIT 7: Indicates the status of the 'line bit' FF in serdes.

SERIALIZER/DESERIALIZER (Serdes)-BITS 8-15: Indicate the contents of serdes at the time the 'sense device' command is given.

DATA FLOW THROUGH THE COMMUNICATIONS ADAPTER

- Transmit data transfer requires two CS cycles to load serdes twice from each P-C core storage word.
- Characters shift through serdes toward the bit 8 position which controls the level of the line to the data set.
- Receive data enters serdes bit 0 position and shifts right until serdes 0-7 is filled with one character.
- Characters to be stored in core storage 0-7 positions (left byte) are first stored in the CA buffer during a dummy CS cycle.

- Character to be stored in core storage 8-15 positions (right byte) is transferred directly from serdes via the common bus. Both the left and right bytes are transferred to P-C core storage during the same CS cycle.

- Unit data flow diagram is on Maintenance Diagram MA10111.

In transmit operations (and not diagnostic mode), during the data transfer CS cycle (also called "cycle-steal acknowledge cycle" or CSA cycle), a word from the P-C core storage is available on the 'bus out' lines. The word contains two characters.

If the byte count is even at the start of the CSA cycle, the left byte is gated to the 'common bit' lines. Common bits 0-7 are used to load serdes 0-7 positions, and common bit parity controls the 'transmit parity check' FF. CAR is not incremented when the byte count is even.

If the byte count is odd at the start of the cycle, the right byte is loaded into serdes in the same manner. In this case, though, CAR is incremented.

To start transmission of the character just loaded, all bits in serdes are shifted one position to the right. Bit 7 shifts to the line bit position which controls the level of the 'transmit data' line to the data set. At each succeeding shift time the next data bit is sent via the data set and communications lines.

In receive operations, the 'receive data' line from the data set is sampled each bit time and set into serdes bit 0 position. At the same time, bits already in serdes shift one position to the right (toward the bit 7 end). After eight shifts, serdes 0-7 positions contain a complete character, ready for storing.

If the byte count is even at the start of the CSA that is taken to store the character, the character is gated to set the buffer register. (This character is to form the left byte of the core storage word.) During the receiving of any character, the 'receive parity' FF generates odd parity for that character. When the character is set in the buffer register, the state of the 'receive parity' FF controls the setting of the buffer register 'parity bit' FF. CAR is not incremented during the CSA cycle when the byte count is even.

If the byte count is odd at the start of the CSA cycle that is taken to store the character, serdes is gated to the common bus. The 'receive parity' FF is gated to the 'common bit parity' line. Then the common bits control the bus in 8-15 and parity lines, while the buffer register output lines control the bus in 0-7 and parity, during the CSA cycle. Thus, both the left and right bytes are transferred to core storage in the same cycle.

OPERATION SEQUENCES

- Sequence of operations is dependent upon the program in the P-C, the control characters and sequences in the data stream, and the transmission code being used by the CA.

- Typical message sequences are shown in Maintenance Diagrams MA10121 and MA30101.

The combination of program controls, message content, and to some extent the transmission code itself determines the sequence of operations that occur in the CA.

The program must provide the following functions:

1. Proper sequencing of commands.
2. Translation to and from data codes.
3. Interpreting sense and status information.
4. Initiation and termination of operations.
5. Establishment of proper message formats (data tables, for example).
6. Data table chaining.
7. Differentiation between control characters when these characters result in the same CA circuit operation (ETB and ETX, for example).

A description of the functions of the IOCC's applicable to the CA has been given in preceding paragraphs. Note that CA operations are started by an XIO instruction which obtains an IOCC with the function code, 'initialize CA'. Further operation depends on control characters and sequences in the data stream and/or further commands.

In a transmit operation, transfers from the data table start after the CA sends the pre-SYN pads and at least two consecutive SYN characters. Data transfers occur during CS cycles. The transmit operation may be intended to send text data or to send an acknowledgement that the CA has received a message. Recognition by the CA of an SOH or an STX establishes the fact that the following data is text data. For all text data, the CA generates a block check character (BCC) to be transmitted following the end character. After sensing the end character, the CA operation depends on what end character is sensed, whether or not data chaining has been programmed, and what other commands are given. Additional details of the transmit operation are in the maintenance diagram manual (MA30123 through MA30153).

In a receive operation, transfers to the data table start when the CA has received the first data character following the synchronization sequence. Data transfers occur during CS cycles. The receive data may be either text data or an acknowledgement that the remote terminal has received a previous transmission. Recognition by the CA of an SOH or an STX establishes the fact that the following data is text data. For all text data, the CA generates a block check character (BCC). At the end of the block of text data, the BCC generated during the receiving of this block of data is compared with the BCC that is received. After checking the BCC, the following pad character is stored. Then further operation depends on the program. Additional details of the receive operation are in the maintenance diagram manual (MA30165 through MA30189).

As mentioned previously, acknowledgements are transmitted and received in non-text modes. That is, they do not start with an SOH or STX. The end characters for acknowledgements, which can only be recognized in non-text mode, are the NAK, EOT, and DLE STICK characters.

The transmission code used affects the operation of the CA only in the generation and loading of BCC's. In EBCDIC operation, a 16-bit cyclic redundancy check (CRC-16) code is accumulated. This check code is transmitted and received as two 8-bit block check characters. In ASCII operation, an 8-bit longitudinal redundancy check (LRC) code is accumulated. This check code is transmitted and received as a single BCC. Examples of BCC accumulation are in the maintenance diagram manual (MA20121 and MA20131).

Transparent Mode Control

Transparent mode makes the full 256 character codes in EBCDIC available for transmission. A special character, DLE, must precede any control characters in the message; otherwise, all characters are accepted as text. There is no provision for transparent mode in ASCII. These controls are used when binary information or external codes are to be sent or received. The CA enters transparent mode following a DLE STX sequence. See MA30201.

In transparent mode, the transmitting adapter inserts a second DLE after each data DLE from core, and the receiving adapter deletes the first DLE from the data sent to core. DLE SYN sequences are used to maintain synchronization in transparent mode in place of the SYN SYN characters used in normal mode. Frequency of insertion is dependent on line speed.

Exit from transparent mode during transmission is done by inserting a DLE END character sequence in the third and second character positions from the end of each data table. (END is defined as any of the characters ETB/ITB/ETX/ENQ.) Only when the DLE is in this position of the data table can it be transmitted without having a second DLE inserted.

Receiving a single DLE followed by an ETB, ITB, ETX or ENQ control character causes the line adapter to leave transparent mode.

Timeout Controls

Timeouts are used to ensure efficient utilization of the communications line and to prevent tie-ups due to false sequences or missed turn-around characters.

Some timeout conditions cause an interrupt, but the program has the option to suppress the timeout interrupt.

Transmit Timeout (No Interrupt)

This timeout is used to automatically insert the synchronous idle sequence in the output data stream.

1. Normal mode and transparent mode with data set clocking -- a SYN SYN or DLE SYN sequence is inserted every 1.00 (±0.15) sec.
2. Transparent mode with business machine clocking -- a DLE SYN sequence is inserted at intervals depending on the line speed:

   600 baud-900 (±100) milliseconds (WTC only)
   1200 baud-475 (±50) milliseconds
   2000 or
   2400 baud-255 (±25) milliseconds
   4800 baud-106 (±12) milliseconds (domestic only)

The timeout period used in transparent mode is preset by jumper. Insertion of the synchronous idle sequence is delayed when insertion would occur between:

A DLE and its following control character.
An END character and the following BCC's.
Two block check characters.

In the case of all non-ITB ending sequences, insertion is abandoned.

The timeout is restarted when the synchronous idle sequence (SYN SYN or DLE SYN) is detected in the message stream.

Timeout (Interrupt)

This timeout has the following purposes:

1. Limits the waiting time allowed for a transmitting station to receive a reply (3 seconds).
2. Monitors incoming or outgoing data for SYN patterns. A timeout interrupt will occur in 3 seconds if any of the following occurs in the data stream:
   a. A double SYN (SYN SYN) sequence is not decoded in normal mode.
   b. Continuous SYN characters are decoded in normal mode.
   c. A DLE SYN sequence is not decoded in transparent mode.
   d. Continuous DLE SYN sequences are decoded in transparent mode.

A timeout interrupt occurs in 3 seconds if the data set fails to activate 'clear to send' in that time in response to a 'request to send.'

A continue timer (nominal 2 seconds) is implemented by using a modifier bit in an 'initialize' or 'sense' command.

The timeout interrupt can be suppressed if a 1 is inserted in bit 3 of the byte count word.

Actual time periods are as follows:

Time Period	Secondary Station	Primary Station
3 second timer	3.0 seconds	2.7 seconds
2 second continue timer	2.0 seconds	1.9 seconds
all times ± 100 milliseconds		

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Selector Channel

The selector channel provides for the attachment of System/360 I/O devices and operates in a manner similar to that in which a System/360 selector channel operates. Standard 1800 MPX programming systems provide for the attachment of an IBM 2841 Storage Control with as many as eight IBM 2311 Disk Storage Drives. Other System/360 devices are available on an RPQ basis. The selector channel is housed in an IBM 1826 Data Adapter Unit, Model 2 or Model 3.

A description of selector channel theory of operation is contained in FEMDM Volume One beginning on page FS10100.

MODE OF OPERATION

The selector channel operates in burst mode only and uses the cycle-stealing facilities of a data channel. The maximum data rate that can be handled by the combination of selector channel, 2841, and 2311 is 15,625 bytes per second. This assumes that the attached control unit does not have a buffer and the selector channel is assigned to the highest priority data channel. The actual data rate of any one configuration depends on the control unit, I/O device, and mode of operation.

PROGRAMMING COMPATIBILITY

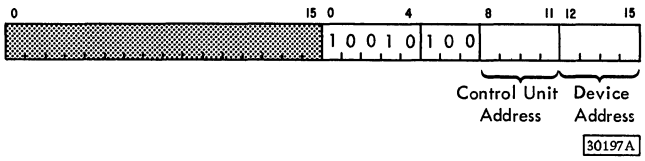
The selector channel is controlled by the 1800 execute I/O (XIO) instruction. The control concepts of the selector channel are the same as for the System/360 channel; that is a channel command word (CCW), channel status word (CSW), start I/O, and halt I/O are used. However, the formats of these differ from those used with System/360 programming. Therefore, 1800 programming and System/360 programming for the same devices are not compatible.

This section of this manual describes programming and operating characteristics of the selector channel. The disk storage concepts, programming, and actual CCW command codes used for 2841/2311 operations are described in the SRL publication IBM System/360 Components Description -- DASD for 2841, Order no. GA26-5988. Although the CCW's described in the 2841 SRL are in System/360 format, the functions of the various fields described are the same for the corresponding fields in the 1800 CCW format. For example, the flag and command code fields in both CCW formats provide the same functions.

SELECTOR CHANNEL PROGRAMMING

The selector channel utilizes a data channel to communicate with the processor-controller (P-C). Data and commands are both transferred between the selector channel and P-C via data channel operations. The execute I/O (XIO) instruction is used to effect control of selector channel operations. An input/output control command (IOCC) referenced by an XIO must have an area code of 10010 to address the selector channel. The following IOCC's are used to effect control of selector channel operations.

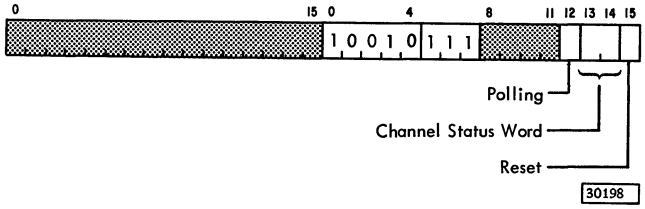
Halt I/O



This command causes termination of the current I/O operation at the selector channel. If the channel is not busy, the device specified by the modifier bits is selected and signaled to terminate the current operation without further data transfer. If the channel is busy, the operation is terminated and the device currently using the channel is immediately disconnected. In this case, the modifier bits are ignored. A unit status pending interrupt caused by channel end/device end occurs after the channel and/or device is cleared.

If a program check occurs, a Halt I/O should be given to reset the selector channel.

Sense Device



This command causes one of the four words comprising the selector channel status word (CSW) to be read into the accumulator. Modifier bits 13 and 14 specify the word to be read and modifier bit 15 controls reset of the program resettable indicators in the CSW. If modifier bit 15 is on, the reset function

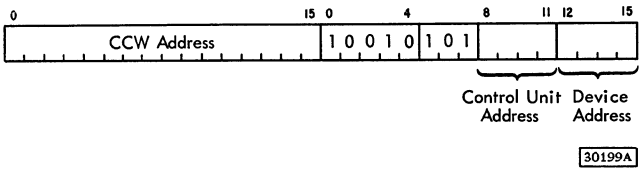
is performed. If modifier bit 15 is off, the reset function is not performed. The individual words of the CSW, interrupt indicators, and program resettable indicators are described under Channel Status Word (FS10120) Modifier bit 12 of an XIO sense device controls the channel polling function. If modifier bit 12 is on, polling is suppressed. If modifier bit 12 is off, polling is allowed.

Polling is the ability of the selector channel to acknowledge a request for service from a control unit. Polling is suppressed by: (1) an XIO sense device with modifier bit 12 on, (2) initiation of a start I/O operation, or (3) the selector channel accepting a request for service from a control unit. Polling remains suppressed until: (1) an XIO sense device with modifier bit 12 off is given, (2) a halt I/O is given, or (3) RESET on the P-C console is pressed.

A request for service from a control unit is usually the result of device end or attenuation turning on in the unit status portion of the CSW. If polling is not suppressed and a control unit requests service, the unit address-status portion of the CSW is transferred from the control unit to the selector channel and a unit status pending interrupt is given to the P-C. The selector channel suppresses further polling until the program reads the status word and reinitiates polling.

Polling should be reinitiated following completion of a start I/O operation by issuing an XIO sense device with modifier bit 12 set to zero.

Start I/O



This command initiates all selector channel I/O operations. The address field contains the core storage address of a channel command word (CCW). The CCW specifies the operation to be performed by the channel, control unit, and device as well as the core storage area associated with the operation. IOCC modifier bits 8 through 11 select the control unit and modifier bits 12 through 15 select the device to which the operation pertains.

Once the IOCC area code, function, and modifiers have been sent to the selector channel and the CCW address has been loaded into the data channel address register (CAR), the P-C is released. The selector channel continues the operation via data channel (cycle steal) operation by fetching the addressed CCW from core storage.

If a start I/O is given while the selector channel is busy, it is ignored and no indication is given to the program.

CHANNEL COMMAND WORD

The channel command word (CCW) contains the information that directs selector channel I/O operations. The CCW consists of three 16-bit words and may be located in any three contiguous core storage locations. The information in a CCW is separated into various fields as follows:

Byte Count
Flag
Command Code
Data Address

Byte Count

The byte count is located in word 1 of the CCW (Figure 4-3) and specifies the length (in 8-bit bytes) of the input or output field. The maximum length which can be specified is 65,535 bytes. Two 8-bit bytes are contained in each core storage word. Therefore, data transfer between the selector channel and core storage is performed two bytes at a time (one core storage word). If an odd byte count is specified for a write operation, the byte in bit positions 8 through 15 of the last core storage word is not used even though it is transferred to the channel. If an odd byte count is specified for a read or sense operation, the byte in bit positions 8 through 15 of the last core storage word is not used for data, but is reset to zero.

All CCW's, except those specifying transfer-in-channel, but including those specifying immediate commands, must have a non-zero byte count. Although data is not transferred during an immediate command and the CCW specifies a non-zero byte count, incorrect length is not indicated in the CSW.

Flags

The flag field consists of bit positions 0 through 4 in word 2 of the CCW (Figure 4-3). The bits in the flag field further define the operation as follows:

Chain Data (CD): When on, this flag specifies chaining of data. Data chaining causes the selector channel to automatically fetch the next sequential CCW when the byte count of the present CCW is decremented

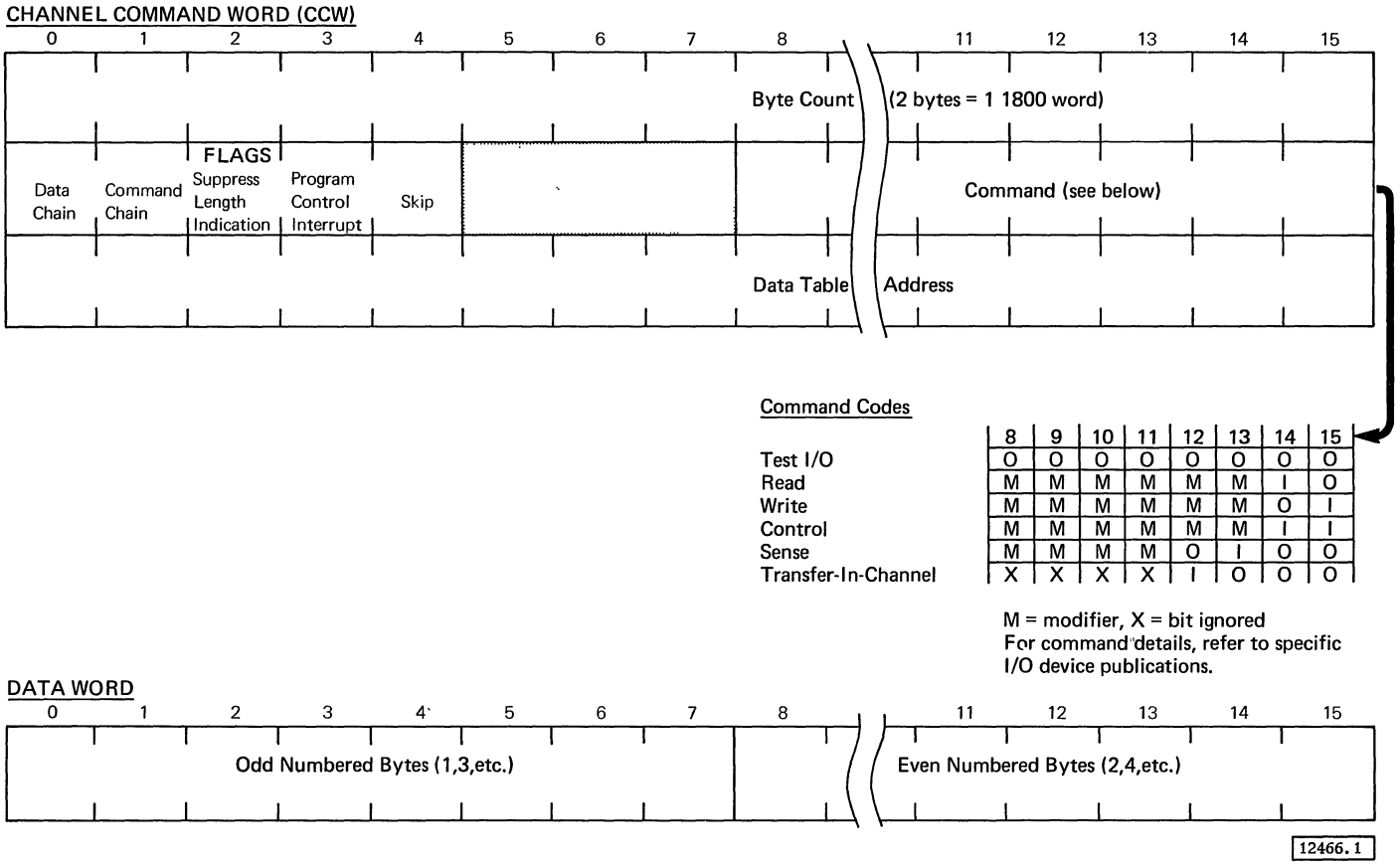


Figure 4-3. Channel Command Word and Data Word

to zero. The new CCW is fetched from the three contiguous core storage locations beginning with the next higher location following the last CCW. The command code in the new CCW is ignored unless it specifies transfer-in-channel. However, the byte count, flags, and data address are used to continue the operation specified by the first CCW. Data chaining continues until a CCW with the CD flag off is encountered and the byte count of that CCW reaches zero, or until the device terminates the operation by presenting ending status.

Note that data chaining (CD flag is on) suppresses command chaining.

Chain Command (CC): When on, this flag specifies chaining of commands. Command chaining causes the selector channel to automatically fetch the next sequential CCW when device end is given signalling completion of the current CCW operation. The new CCW is fetched from three contiguous core storage locations beginning with the next higher location following the last CCW. All fields in the new CCW are used to initiate a new I/O operation. Command chaining continues until a CCW with the CC flag off is encountered and the operation specified by that CCW is completed.

It should be noted that data chaining takes precedence over command chaining; that is, if the CD and CC flags are both on, data chaining is performed and command chaining is suppressed.

Suppress Length Indication (SLI): This flag is used to determine if occurrence of an incorrect length condition is to be indicated to the program. An incorrect length condition occurs if the number of bytes designated by the byte count in a CCW is not

equal to the number of bytes requested or offered by an I/O device.

Indication of an incorrect length condition is suppressed if the SLI flag is on and the CD flag is off in the CCW. If the SLI flag and CC flag are both on in a CCW, the incorrect length indication is suppressed and command chaining takes place regardless of an incorrect length condition. Incorrect length indication is also suppressed if a CCW specifies an immediate command, even though the byte count must be non-zero.

When an incorrect length condition occurs, an indication is always given to the program if the SLI flag is off, or the CD flag is on in the CCW. In the latter case, indication of an incorrect length condition is given even if the SLI flag is on.

Program Control Interruption (PCI): When on, this flag causes the selector channel to generate an interrupt upon fetching the CCW. The capability allows the program to detect when specific chained commands are about to be performed.

Skip: When on, this flag suppresses data transfer to core storage during a read or sense operation. When the skip flag is off, normal data transfer occurs.

Command Code

The command code field consists of bit positions 8 through 15 in word 2 of the CCW (Figure 4-3). The two low order bits (14 and 15), or if these two bits are off, the four low order bits (12 through 15) of the command code identify the operation to the selector channel. The selector channel has four basic operations:

Output (write or control)
Input (read or sense)
Branch (transfer-in-channel)
Test I/O

All eight bits of the command code are transferred to the control unit. The high-order bits are modifiers which indicate to the device how the command is to be executed. The exact configuration of the modifier bits depends on the I/O device. Command codes and descriptions for the 2841/2311 are given in IBM System/360 Components Description -- DASD for 2841, Order No. GA26-5988. The basic commands for the selector channel are described under "Selector Channel Commands".

Data Address

The data address is located in word 3 of the CCW (Figure 4-3). For commands that transfer data (read, sense, write, etc.), the data address specifies the core storage address of the first two data bytes (two bytes per core storage word) in the input/output data field. For a transfer-in-channel command, the data address specifies the core storage address of the new (transferred to) CCW.

SELECTOR CHANNEL COMMANDS

Figure 4-3 shows the configurations for the basic selector channel commands.

Test I/O

This command causes the device addressed to send its current status to the selector channel. After the channel has received the unit status, a unit status pending interrupt is given to the P-C.

A test I/O terminates command chaining even if the CC flag is on, and therefore, should not be included within a chain of CCW's that specify command chaining.

A test I/O need not be given prior to initiating a start I/O with a specific device. The selector channel automatically checks the unit status when initiating a start I/O operation. If the status is not acceptable, it is presented to the program via an interrupt.

Note that a test I/O does not place the unit status into the accumulator, but makes it available in the selector channel. An XIO sense device which specifies word 2 of the channel status word must be given to read the unit address-status into the accumulator.

Read

This command causes data to be transferred to core storage from the device specified by the modifier bits in the IOCC of the start I/O. Data is read (two) bytes per word) into ascending core storage locations beginning with the address specified in the CCW data address field. The number of bytes transferred during the operation is specified by the byte count in the CCW.

The read operation continues until the specified number of bytes have been transferred, or until the I/O device terminates the operation. If the byte count is odd, the last byte transferred is placed in bit positions 0 through 7 of the last core storage word. Bit positions 8 through 15 in this word are all reset to zero.

Write

This command causes data to be transferred from core storage to the device specified by the modifier bits in the IOCC of the start I/O. Data is transferred (two bytes per word) from ascending core storage locations beginning with the address specified in the CCW data address field. The number of bytes transferred during the operation is specified by the CCW byte count field.

The write operation continues until the specified number of bytes have been transferred, or until the I/O device terminates the operation. If the byte count is odd, the last byte transferred is obtained from bit positions 0 through 7 of the last core storage word. Bit positions 8 through 15 in this word are ignored.

If an incorrect length condition occurs during a write operation, the incorrect length indication is given to the program with the ending status unless the suppress length indication (SLI) flag is on in the CCW.

Control

This command causes the device specified by the modifier bits in the IOCC of the start I/O to initiate a control operation. The operation proceeds similar to a write, except that the command code modifier bits received by the control unit are decoded to determine the specific control function to be performed.

In cases where the particular control function can be performed without any data transfer (immediate command), the control unit signals channel end as soon as it receives the command. The device signals device end after it has completed the control function.

A control command in which all six of the modifier bits in the command code are off performs as a NO-OP (no operation). A NO-OP causes the control unit to respond with channel end and the device to respond with device end without causing any action. This ending status causes a unit status pending interrupt to be generated. The unit address-status portion (word 2) of the channel status word (CSW) is available in the selector channel and may be read by an XIO sense device.

Sense

This command performs in the same manner as a read, except that the data is obtained from status indicators rather than from a record source.

The status information is transferred to ascending core storage locations beginning with the address specified by the CCW data address field. Two bytes of status information are placed in each core storage word. The number of sense bytes transferred is specified by the CCW byte count and should be limited to the number of sense bytes available in the I/O device.

Data transferred during a sense operation provides information concerning unusual conditions detected during the last operation and the current status of the I/O device. The device status provides a more detailed definition of the conditions which may cause a unit check indication in the unit status portion of the CSW.

Transfer-In-Channel (TIC)

This command causes the selector channel to automatically fetch the next CCW from three contiguous core storage locations beginning with the address specified by the data address field in the TIC CCW. TIC does not initiate any I/O operations and the control unit is not aware of the command. The byte count portion of the CCW is not used.

TIC provides a means of chaining between CCW's not located in adjacent three word areas of core storage. TIC performs as an unconditional branch regardless of the status of the chain data (CD) flag in the CCW.

Chapter 5. Power Supplies and Control

- Input voltage is three-phase, 208/230 volts at 60 Hz or 195/220/235/380/408 volts at 50 Hz.
- AC primary power is sequenced to 1800 system units from the processor-controller.
- DC power supplies provide system service voltages and special voltages for core storage and process I/O features.
- Interlocks are provided for critical voltages.

The 1800 system operates from one three-phase line cord. Primary power enters the 1801 or 1802 through a line filter and a 50-amp mainline power circuit breaker (CB1) and is sequenced to all system units except the 1053 Printer and the 1816 Printer-Keyboard. The 1053 and 1816 have their own power cords.

1801 AND 1802 PROCESSOR-CONTROLLERS

Power-On Sequence

- The power-on sequence for 60 Hz systems is shown on YA 90110; for 50 Hz systems on YA 90120.
- DC power distribution to SLT gates is shown on System Diagram YA 159.

Three-phase primary power is supplied through CB1 to contactor K1 which is controlled by the Emergency Power Off (EPO) switch, and to transformer T1 which provides the 24V ac sequencing voltage. The 24V ac sequencing voltage is supplied to the 1828 (for the 1856 units) through isolation transformer T6.

From K1, primary power is distributed to contactors K2, K3, K4, and to transformer T3. Transformer T3 supplies 115V ac to convenience outlets in the 1801 or 1802, 1803, 1826, 1828, 1442, 1810 and 2401 or 2402.

Pressing the ON button turns on the Power On lamp and starts the power-on sequence:

1. Supply primary power via K3 to CB2 (1826) and CB3 (1828).
2. Supply primary power via K2 to
   (a) gate blowers and power supply fans in the processor-controller;
   (b) 1442, 1443, 1810, and CB4 (2401 or 2402);
   (c) transformer T2: 115V ac power to 1054 and 1055 (via switches on P-C power tailgate), 1627, and gate fans in the 1442;
   (d) transformer T4; 7.5V ac lamp voltage to P-C console and 1442;
   (e) transformer T7; power-failure-protect circuit;
   (f) power supplies, 1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, and 15 in the processor-controller (P-C power supplies are shown on System Diagram YA159).
3. When voltages are available at power supplies 1, 2, 3, 7, 9, 10, 12, 13 and 15, supply primary power via K4 to power supplies 5, 14, 16, 17, and 18 in the processor-controller.

The power-on reset line is held at 0V (active level) during the power-on sequence. The power-on reset ends approximately 1.7 seconds after pressing the ON button, at which time the Ready lamp turns on to indicate that dc voltages are present.

Resistors are employed in the output circuits of ADC power supplies 8(+30V), 11(-30V), and 14(+12V) to limit the initial surge current. When the ready condition is reached, the current limiting resistors are shunted by relay RY19 points.

Power-Off Sequence

- Power-off sequence for 60 Hz systems is shown on YA 90101; for 50 Hz systems on YA 90130.

The OFF push button is used to power-down the 1800 system. Pressing the OFF button drops all power in the system with the exception of the 115V ac convenience outlets and the 24V ac sequencing voltage.

The use of the OFF push button ensures that power supplies will be cycled down in the following order:

1. Power supply 18 (+48V magnet voltage).
2. Power supply 14 (+12V ADC), and power supplies 5, 16, and 17 (core storage).
3. All other power supplies.

Power supplies in items 1 and 2 are controlled by K4, which is the last contactor to pick and the first to

drop. The +48V is removed before other voltages by opening the output of power supply 18 with relay points. Power supplies in item 3 are controlled by K2 and loss of any of these voltages (except supply 6, 8, or 11) will immediately drop K4.

Loss of dc voltage from any P-C power supply. except supplies 6, 8, 11, 14, and 18, will drop system power in the same manner as operating the OFF switch. Loss of voltage from supply 6, 8, 11, 14, or 18 will not drop system power and will be indicated only by program detection of failure or by visual observation.

Power supplies 8 and 11 (+30V and -30V) are interlocked so that loss of either supply will drop the output of both these supplies and will also drop supply 14 (+12V).

If loss of voltage is caused by tripping the overcurrent circuit breaker in any MPS (medium power standard) power supply, the condition will be indicated by turning on the dc CKT BKR TRIP lamp on the I/O monitor interface panel.

Power Failure Protect Circuit

- Ensures proper cycling down of the power supplies after loss of primary power.

Figure 5-1 shows a simplified block diagram of the power failure protect circuit. Power supply #4, the power failure protect supply, constantly senses the line voltage through transformer T7 (24V ac). Upon detecting a power loss or reduction of 25 to 50 percent, power supply #4 produces a +3V dc signal for a minimum of 100 ms. This signal fires an SCR (Silicon Controlled Rectifier) that picks relay RY 23 initiating a power down sequence. This signal also sets the Alarm Stop flip-flop in the P-C, holding the system reset at X7/T7 so that the machine will be in a static condition when power is sequenced down.

The processor-controller remains in a power-on state for power drops to the system up to one cycle in duration (15 to 17 ms). The power failure sequencing enables the processor to complete the core storage cycle that is in progress at the time of failure.

1826 DATA ADAPTER UNIT

- Power-on sequence is shown on YB 90101.

Single-phase primary power is supplied to the blower motors and power supplies in the 1826 from the 1801 or 1802. A mainline switch is mounted on the right side of the upper front panel of the 1826 to remove power, except 115V ac convenience outlets, for off-line servicing. Main line power can also be disconnected at the power circuit breaker (CB2) in the 1801 or 1802. A Power On neon is provided on the 1826 power sequence assembly to indicate the presence of primary power.

The dc voltages required for SLT gates are provided by the MPS power supplies within the 1826. These supplies are listed on System Diagram YB 140. No voltage sensing of power supplies is provided in the basic 1826 unit, and loss of a single voltage will not drop other dc voltages.

Power supplies 5 (+3V), 7 (+12V), 8 (+30V), and 9 (-30V) are installed with the AI Expander feature. The +30V and -30V supplies are interlocked so that loss of either supply will drop the output of both of these supplies and also supply 7 (+12V).

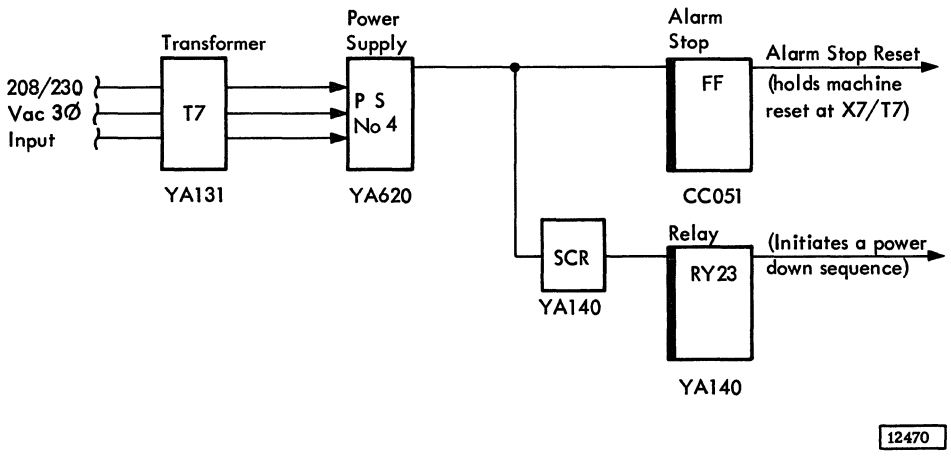


Figure 5-1. Power Failure Protect Circuit

When the 24V ac sequencing voltage picks contactor K4 in the processor-controller, it is also made available at the 1826. The processor-controller power sequencing circuit ensures that +12V from supply 7 will be the last voltage supplied to the ADC during the power-on sequence and the first to be removed during the power-off sequence.

Resistors are employed in the output circuits of power supplies 7, 8, and 9 to limit the initial surge current. When the dc power supplies in the 1826 are ready, the current limiting resistors are shunted by relay RY3 points.

If primary power to the system is interrupted, the power-failure-protect circuit in the processor-controller disconnects the sequencing voltage to the 1826, thereby removing the +12V ADC voltage before the other dc voltages can drop.

Each power supply in the 1826 has an overcurrent circuit breaker. If any circuit breaker trips, the condition will be indicated by turning on the dc CKT BKR TRIP lamp on the 1801 or 1802 I/O monitor interface panel.

1828 ENCLOSURE

- Power-on sequence is shown on YD 90101.

All ac power is supplied to the 1828 from the 1801 or 1802. Single-phase primary power is available on the internal power bus for 1856 units and can be disconnected at the mainline switch on the right side of the upper front panel for off-line servicing. Primary power can also be disconnected at the power circuit breaker (CB3) in the 1801 or 1802. A Power On neon is provided on the 1828 power tailgate to indicate the presence of primary power.

115V ac and 24V ac are available continuously, except for emergency power off, in order to power precision voltage supplies which require several hours warm-up. The 115V ac power is available at the convenience outlet and is also used by the analog input calibration facility in the first 1828 that houses an 1851 Multiplexer Terminal. The 115V ac can be disconnected from the calibration facility with the switch on the left side of the upper front panel. The 24V ac power is supplied through an isolation transformer (T6 in the processor-controller) and is used by each Mod 2 Precision Voltage Reference in an 1856 unit.

Each 1856 unit plugs into the internal power bus and receives primary line voltage for operation of blower motors and special modular power pacs. Each power pac contains its own fuses and power on/off switch for CE use. No voltage sensing of these power supplies is provided.

DC voltages of +6V, +12V, +30V, and -30V are required for operation of multiplexer components in the 1851 units. These voltages are supplied to the 1851 units directly from MPS power supplies located in the 1801, 1802, or 1826 Model 1.

1803 CORE STORAGE UNIT

- Power-on sequence is shown on YS90101.

Single phase power is supplied to the 1803 mainline CB from contactor K2 (YA110) in the P-C. The -15 and -10V dc power supplies are energized (K1, YS220) after sensing circuits indicate the presence of the other four dc voltages.

Convenience outlet power is available from the P-C regardless of the 1803 mainline CB.

The power-on neon indicates only that ac power is available from the mainline CB. The CB indicator is on if one of the six power supply circuit breakers is tripped.

1810 DISK STORAGE

- Power-on sequence is shown on YC90101.

Single-phase primary power is supplied to the 1810 Disk Storage from the 1801 or 1802 via contactor K2. A main line switch is provided on the 1810 power sequencing assembly for removing primary power. The convenience outlet receives 115V ac from the 1801 or 1802 continuously except for emergency power off.

The dc voltages required for the SLT gates and Single Disk Storage units are provided by power supplies in the bottom of the 1810. No voltage sensing of power supplies is provided, and loss of a single voltage will not drop other dc voltages.

1053 PRINTER AND 1816 PRINTER-KEYBOARD

Mainline power for motors in the 1053 and 1816 is controlled by switches on these units.

Two dc voltages, +12V and +48V, are required by the 1053 and 1816. These voltages are supplied by power supplies 5 and 18 in the processor-controller.

1054 PAPER TAPE READER AND 1055 PAPER TAPE PUNCH

The paper tape units operate from 115V ac supplied from the 1801 or 1802 via contactor K2 and transformer T2. Power can be removed from either unit by means of an AC switch mounted beside the power connector on the P-C power tailgate.

Two dc voltages, +12V and +48V, are required by the 1054 and 1055. These voltages are supplied by power supplies 5 and 18 in the 1801 or 1802.

1442 CARD READ PUNCH

Single-phase primary power for the drive motor is supplied to the 1442 from the processor-controller via contactor K2. The 1442 main line switch permits removal of primary power for off-line servicing.

The convenience outlet receives 115V ac from the 1801 or 1802 continuously except for emergency power off.

Fan voltage of 115V ac is supplied to the 1442 from the processor-controller via K2 and transformer T2.

Lamp voltage of 7.5V ac is supplied to the 1442 from the P-C via K2 and transformer T4.

The following dc voltages are supplied to the 1442 directly from the MPS power supplies in the processor-controller:

DC Voltage	Supply
+6V	1
+3V	2
-3V	15

1443 PRINTER

Single-phase primary power is supplied to the 1443 from the processor-controller via contactor, K2. The 24V ac sequencing voltage, under control of the P-C Emergency Power Off switch, is used to pick the main line contactor in the 1443. The 24V ac start circuit in the 1443 is actuated in parallel with contactor K4 in the processor-controller.

DC voltages required by the 1443 are provided by self-contained power supplies.

1627 PLOTTER

The plotter receives 115V ac from the processor-controller via contactor K2 and transformer T2. A power on/off switch is provided on the plotter.

2401 OR 2402 MAGNETIC TAPE UNIT

Three-phase primary power is supplied to the 2401 or 2402 from the 1802 Processor-Controller via contactor K2, and can be disconnected at the power circuit breaker (CB4) on the 1802 power sequence assembly. Convenience outlets in the 2401 or 2402 receive 115V ac from the 1802 continuously except for emergency power off.

I/O MONITOR UNIT

The dc voltages required by the I/O monitor unit (+6V, +3V, and -3V) are supplied to the interface panel in the 1801, 1802, 1826, and 2310 from MPS power supplies located in those units.

MPS POWER SUPPLIES

- Provide regulated service voltages ranging from 3V dc to 36V dc.

With the exception of the 48V dc supplies and several special purpose supplies, the 1800 system uses standard MPS power supplies. The MPS power supplies are a family of supplies which are designed to provide all the standard dc voltages required by SLT components as well as a number of special voltages.

MPS power supplies can be operated from single-phase voltages of 115/208/230 volts at 60 Hz or 195/220/235 volts at 50 Hz. Primary (ac) voltage regulation is not normally required with these supplies. The series regulator circuit of the MPS supply provides regulation within ±2% at the power supply terminals.

The MPS power supply (Figure 5-2) consists of a transformer, silicon rectifiers, associated filter networks, an overcurrent circuit breaker, and the series regulator circuit. The regulator amplifier is contained on an SMS card that plugs into the power supply module.

The regulator circuit continuously samples the output voltage and compares it with the reference voltage from a zener supply. Any change in output voltage is immediately detected and amplified to produce a change in the base voltage of the series transistor. The series transistor compensates for the change in output voltage by adjusting its resistance accordingly.

Remote sense connections allow the regulator input to be taken from a remote load, thus compensating for line drop. Remote sensing is not used in the 1800 system; therefore, jumpers are installed to allow the output to be sampled within the module.

An adjustment pot on each MPS supply permits adjusting the output voltage a minimum of ±8%. The MPS supplies should not be operated without at least 25% load.

Marginal Checking

No routine marginal checking of the system is recommended. The 6V MPS power supply used in the system for powering SLT circuits does have a jack for connection of a portable marginal check box. This can be used when all other methods of isolating intermittent failures have been exhausted; but only with the understanding that circuits failing under margin are not necessarily the intermittent circuits being

sought. The portable marginal check box is not shipped with the system.

Cooling

MPS power supplies have germanium transistors which must maintain junction temperatures below 95°C. To maintain allowable limits on power supplies, they are operated at less than 80% load, located in columns less than 26" in height, and are supplies with cooling air.

A continuously running fan is mounted in the bottom of each power supply tub and draws the cooling air in through a replaceable filter.

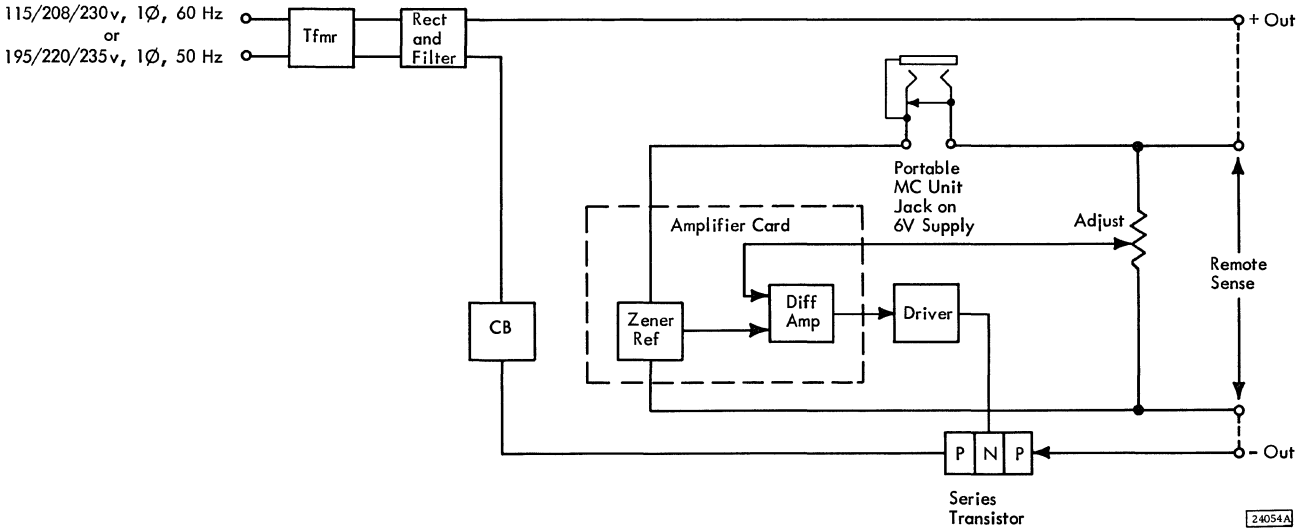


Figure 5-2. MPS Power Supply

Chapter 6. Console and Maintenance Features

SECTION 1. CONSOLE

This section presents a circuit description of the console lights and switches; a functional description of the console is in the 1800 System Maintenance Manual (see FE bibliography – 1800 System, Order No. SY26-0560). Figure 6-1 shows the console.

Switches and Lights (Top Row)

Clear Storage

- This push-button switch provides a means of resetting core storage to a value set in the data-entry switches.
- Provides a means of parity checking core storage.
- Function varies with the setting of the Mode switch and the Write Storage Protect Bits switch.

The Clear Storage push-button switch has four functions (Figure 6-2). None of the four functions can be executed, however, until Clear Storage is first held pressed and then Start is pressed. This dual action requirement prevents the accidental clearing of storage. Note in Figure 6-2 that each Clear Storage function is dependent on the positions of two console switches, the rotary Mode switch and the Write Storage Protect Bits toggle switch.

The processor-controller cycles completely through all core storage addresses during the execution of each Clear Storage function.

A simplified diagram of the clear storage circuits is in Figure 6-3.

FUNCTION 1: Holding the clear-storage key depressed and pressing the start key turns on the clear-storage flip-flop because the mode switch is not in the display position (must be in the run position). The I/O to B register gate line is activated. This line turns off the parity-sample flip-flop to disable parity checking for this function. Because the storage-protect switch is on, the clear-storage flip-flop output turns off the storage-protect-bit flip-flop. This removes all storage protect bits from core storage as core storage is cycled. The off condition of the storage-protect-bit flip-flop and the I/O-to-B register-gate line activates the channel-bus-to-B-register line. This line gates the contents of the data-entry switches to all positions of core storage.

FUNCTION 2: Because the mode switch is in the run position, the on condition of the clear-storage flip-flop activates the I/O-to-B-register- gate line. This line turns off the parity-sample flip-flop to disable parity checking. Because the storage-protect switch is off for this function, the clear-storage flip-flop output does not turn off the storage-protect-bit flip-flop. This flip-flop is on when any protected position of core storage is read. Therefore, the I/O-to-B-register-gate line activates the channel-bus-to-B-register-line only for unprotected positions of core storage.

FUNCTION 3: Because the mode switch is in the display position the I/O-to-B-register-gate line will not be activated for this function. Therefore, the channel-bus-to-B-register line will not be active. The on condition of the clear-storage flip-flop and the storage-protect-switch line turn off the parity-sample flip-flop to disable parity checking and turn off the storage-protect-bit flip-flop to remove all storage protect bits from core storage as it is cycled.

FUNCTION 4: The I/O-to-B-register-gate line is not activated. Therefore, core storage data is not altered. The storage-protect switch is off, therefore the storage-protect-bit flip-flop is not affected and the storage-protect-bits in core storage are not altered. The parity-sample flip-flop is not affected because the storage-protect switch is off. Therefore, as core storage is cycled all positions are parity checked.

Program Load

- Provides a means of initially entering a program into the system.
- Stores the instructions beginning at the core storage location specified by the I register (normally

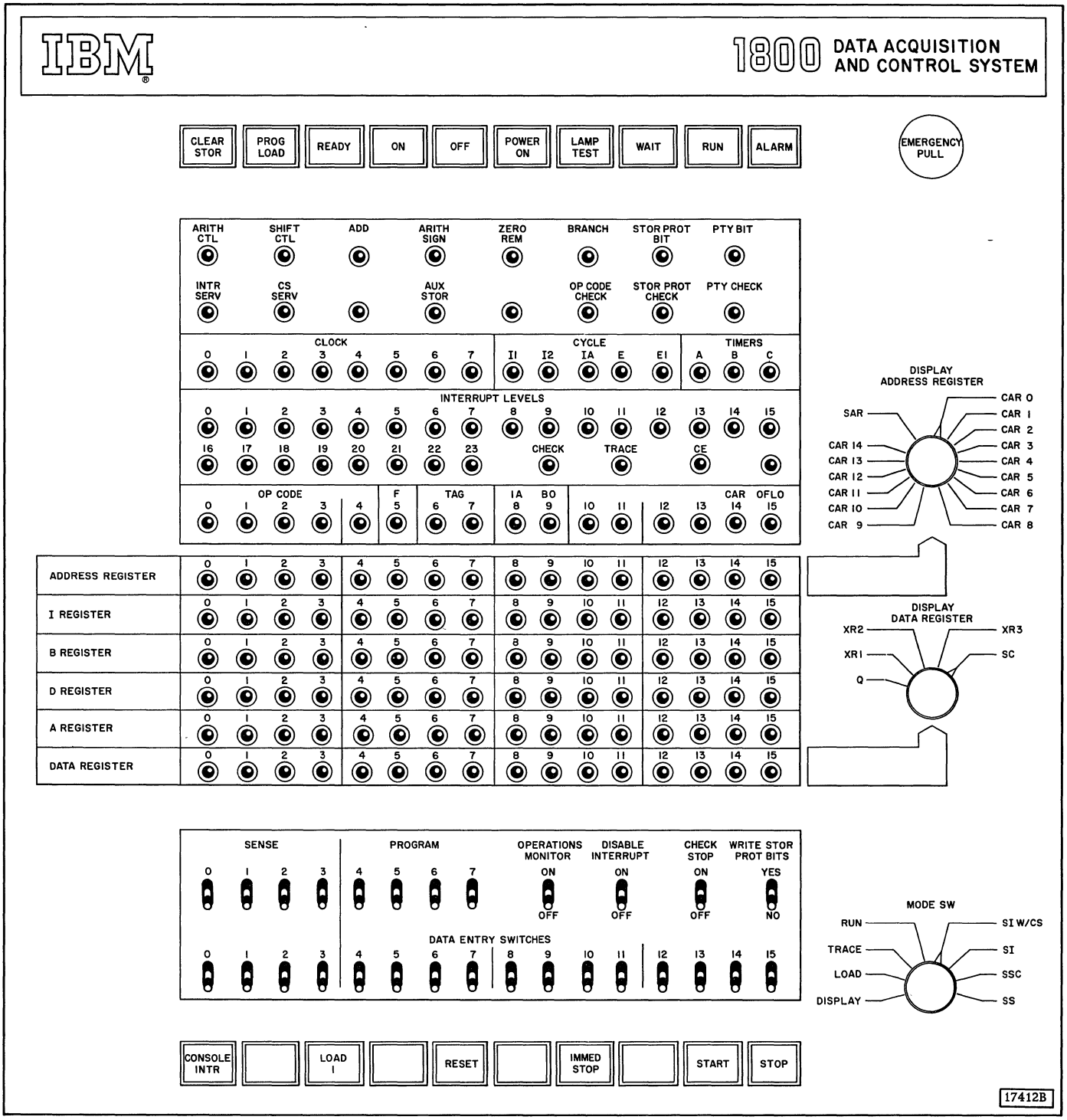


Figure 6-1. Programmers Console

Function	Mode Switch	WSPB Switch
1. Store Contents of Data Entry Switches in all Core Storage Locations. Storage-Protect Bits are Removed and Parity is Corrected as Required Because of Bit Removal. If All Data Entry Switches Are Off, Only Parity Bits are Left in Storage.	Run	Yes
2. Store Contents of Data Entry Switches in Each Core Storage Location that is Unprotected. Locations having Protect Bits are Unchanged.	Run	No
3. Clear Storage Protect Bits. All Other Data Remains Unchanged. Parity is Automatically Corrected in Each Word in Storage.	Display	Yes
4. Search for Parity Errors. The P-C Cycles Through Storage Until Stopped by the Stop Key or a Parity Error. The Check Stop Switch Must be on for a Parity Error to Cause a Stop.	Display	No

17415A

Figure 6-2. Clear Storage Functio

reset to zero) and automatically branches to location zero to execute the program.

- The 1054 paper tape reader and the 1442 card read punch are both capable of initial program load.
- Only one unit in the system can be wired for initial program load.

PAPER TAPE SYSTEM: Paper tape channels 1 through 4 are read in groups and loaded into a buffer. The contents of the buffer are transferred to the P-C as one 16-bit word and loaded into core storage beginning at location zero. The paper tape characters continue to be read until a punch is detected in channel 5. At this time loading stops and an automatic branch is executed to location zero.

CARD READ PUNCH SYSTEM: Rows 12 through 5 of the load card are read in packed mode (two columns per word) and are stored in core storage beginning at the location specified by the I register (normally reset to zero).

INITIAL PROGRAM LOAD CIRCUITS: Maintenance Diagram Manual (MDM) page CC50103 is a simplified logic diagram of the processor-controller IPL circuits. The program-load pushbutton turns on the IPL-switch flip-flop, which conditions the turn on of the IPL-mode flip-flop. IPL mode and an IPL interrupt line from the 1054 or the 1442 turn on the IPL-request flip-flop. IPL-request activates the I/O-to-B-register-gate line. This line turns off the parity-sample flip-flop to disable parity checking during the IPL operation. IPL-request also turns on the start-advance flip-flop which, in turn, turns on the run circuit. IPL-request also forces the wait-operation line active, causing the T7 pulse to turn off the run flip-flop. The IPL-request flip-flop is turned off at each T6 time and is turned on again for each column interrupt from the IPL device. The feed-interlock line from the 1442 or the channel-5-interrupt-request line from the 1054 turns on a flip-flop that turns off the IPL-mode flip-flop at T5 time. The off condition of the IPL-mode flip-flop and the on condition of the IPL-request flip-flop activate a line that resets the I register and blocks the wait-op line to allow the clock to run, causing a branch to core storage location 0.

Ready

- This lamp indicates that the system power is in a ready condition.

The ready lamp is lighted by relay 21, the power-ready relay. Relay 21 is energized by relay 15, 17 seconds after the power-on push button is operated.

On

- The power-on push button applies power to the entire 1800 system.

Operating the power-on push button picks relay 1 which initiates the power-on sequence shown on ALD page YA 140.

Off

- The power-off push button removes power from the entire 1800 system.

Operating the power-off push button drops relay 1 and initiates the power-off sequence shown on ALD page YA 140.

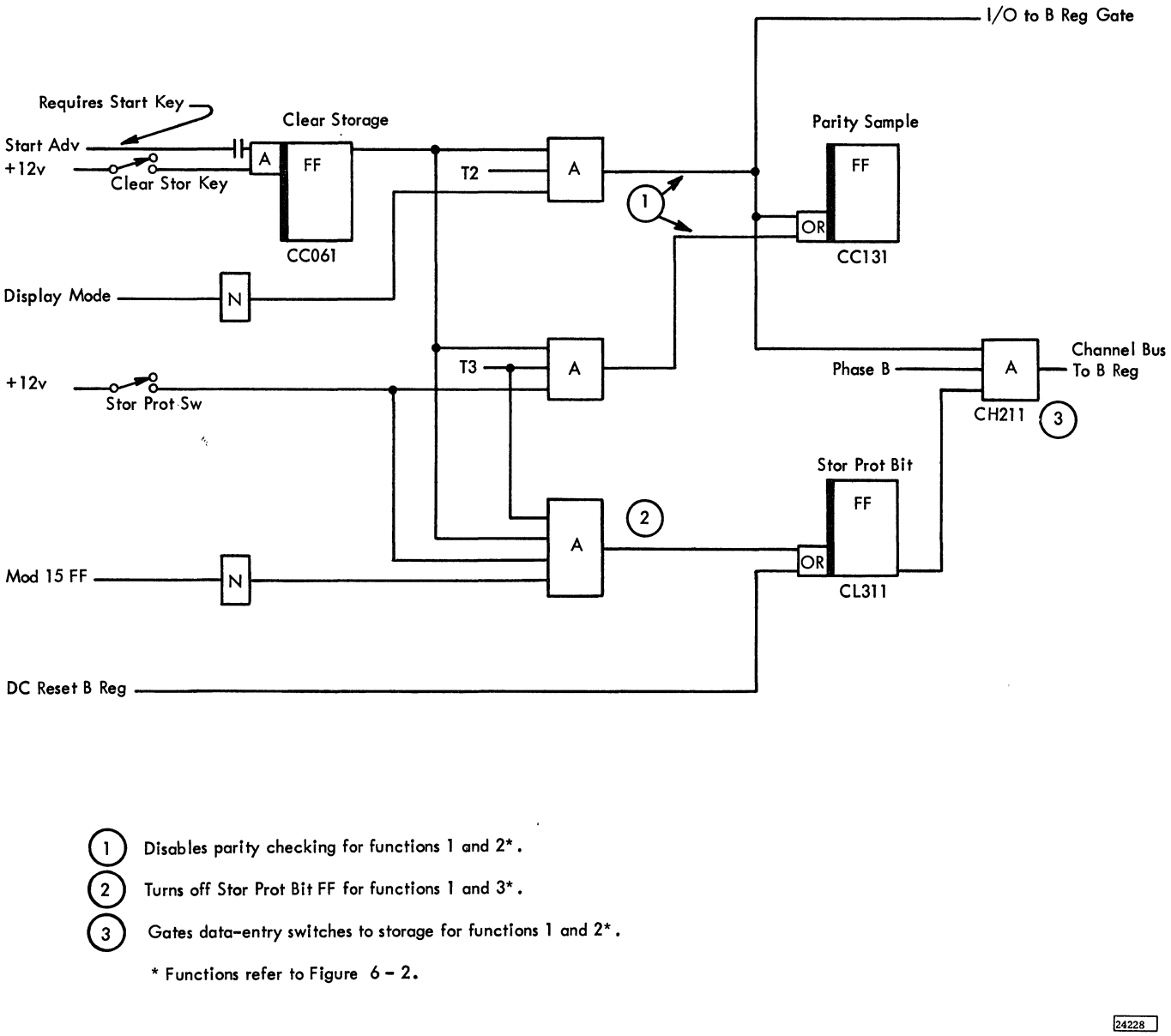


Figure 6-3. Clear Storage Circuits

Power On

- The power-on lamp indicates that power is supplied to all units of the 1800 system.

This lamp is lighted by relay 3, the processor-controller on-off relay. Relay 3 is energized at the same time contactor K3 is energized by relay 1.

Lamp Test

- This push button switch checks the condition of all console lamps.

Operation of this switch applies +3 volts directly to all console lamps.

Wait

- This lamp indicates that the program has been halted by a wait instruction.

The wait-op lamp driver is activated by the op-decode circuit for the wait operation. Load, display, and wait also activate the wait op line and the wait-op lamp driver.

Run

- The run lamp driver is activated directly from the on side of the run flip-flop. The run flip-flop is on when the processor-controller is operating under program control.

Alarm

- This lamp indicates that the operations monitor time interval has expired.
- The alarm light remains on until the operations monitor switch is turned off.

The alarm lamp is operated from the normally closed (N/C) points of relay 20, the operations monitor relay. Relay 20 drops when the operations monitor time interval has expired, or when the plus 12 volts is lost.

Switches and Lights (Bottom Row)

Console Interrupt

- This push button switch provides an operator-initiated interrupt to a customer-assigned level.

The console interrupt is assigned to an interrupt level and an ILSW bit position. Console interrupt status is given directly by the sense-interrupt command; however, it is necessary to execute a sense-device command with an area code of zero and a bit in position 15 of the IOCC modifier in order to reset the indicator. The console interrupt routine can be programmed to interrogate the program toggle switches to specify a particular routine.

The console interrupt switch turns on the console interrupt request flip-flop (Figure 6-4). The console interrupt request flip-flop turns on the console interrupt flip-flop, the output of which activates the assigned bit and the ILSW, bit 0 in the console interrupt DSW, and activates the console interrupt request line to the assigned interrupt request level.

The console interrupt flip-flop is turned off by the sense-device command with an area code zero, and bit 15 = 1.

Load I

- This push button switch loads the contents of the B register into the I register.
- The mode switch must be in the Load position for the Load I operation.
- The Load I operation leaves the processor-controller in the stopped condition.

The mode switch being in the Load position gates the bit switches into the B register. The Load I switch operating point is connected directly to the Load position of the mode wafer switch. Operation of the Load I switch gates the contents of the B register into the I register.

Reset

- This push button switch resets all basic timing, controls, registers (except index registers and address registers), and I/O devices.
- The interrupt mask register is reset to the ON condition.
- This switch does not reset Digital or Analog Output registers.

The reset switch is ORed with the power-on-reset and the alarm-stop-reset lines to activate the DC reset line if the run flip-flop is off.

Immediate Stop

- Stops the processor-controller at the end of the core storage cycle in operation.
- Resets the basic timing, controls, registers (except index registers, DAO registers, and address registers), and I/O devices.

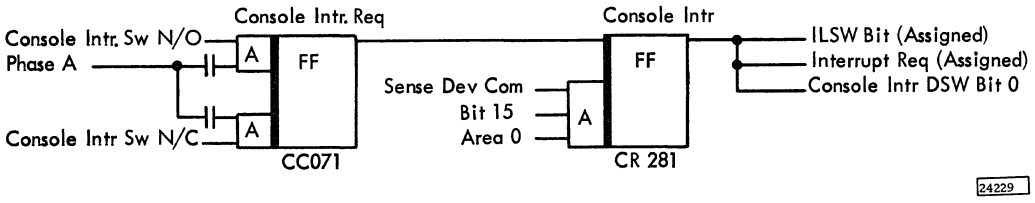


Figure 6-4. Console Interrupt Switch

The immediate stop switch turns on the alarm stop flip-flop at T7 or X7 time. The output of the alarm stop flip-flop activates the DC reset line throughout the CPU and the channel circuits.

Start

- Causes the program to start or continue from its present state according to the setting of the mode switch.

The function of the start switch in the various modes is described in the mode-switch description. The start push button conditions the turn on and turn off of the advance flip-flop. Advance is turned on by the fall of the phase-A pulse and is turned off by the fall of the next phase-A pulse. The output of the advance flip-flop activates the clock advance circuits to run the processor-controller T clock.

Stop

- Stops the processor-controller at the end of the instruction in operation.

- Data channel operations can be stopped only by pressing the immediate-stop push button.

If at the same time the stop key is pressed an interrupt occurs that can force a BSI, the stop key must be pressed again to be effective. Pressing the start key causes the program to resume operation. Operating the stop push button conditions the run flip-flop to be turned off by the next end-op-T7 pulse.

Pull Switch and Rotary Switches

Emergency

- This pull switch is for emergency use only.

- Removes all power from the 1801/1802, including power to the blowers.

- This switch must be reset by an IBM Customer Engineer.

Pulling the emergency power off switch drops contactor K1 and removes voltage from the power supply sense relays that are holding relay 1 energized.

Display Address Register

- Allows continuous display of the storage address register (M register) or any channel address register, as selected, in the address register display lights.

This rotary switch gates the contents of the selected address register to the address register indicator lamps, at T7 time.

Display Data Register

- Selects the Q register, an index register, or the shift counter for display in the data register lamps.

The selected line from this rotor switch ANDs with the display console line to gate the output of the selected register to the data register lamps, at T7 time, END OP.

Mode

- Defines the function of the start switch.

RUN: Pressing the start switch with the mode switch in the run position initiates the normal program operation.

The run mode disables the end-op T-7 turn off of the run flip-flop. The run mode enables the cycle steal request circuit and the X clock advance circuit. The run mode also keeps the interrupt polling and interrupt request circuits conditioned.

SINGLE INSTRUCTION WITH CYCLE STEAL (SI W/ CS): Pressing the start key with the mode switch on SI W/CS causes the execution of one instruction. Data channel operations can occur during execution of the instruction.

Position 1 of the mode switch activates the single-instruction-or-stop line which conditions the run flip-flop to be turned off with end-op-T-7, causing the processor-controller to stop after executing one instruction. Position 1 of the mode switch is jumpered to position 4 to activate the SS-or-SI-with-cycle-steal line which deconditions the turn off of the mode-set flip-flop, keeping the interrupt polling and interrupt request circuits conditioned (ALD page CS 121). The SS-or-SI-with-cycle-steal line also conditions the cycle steal request and X clock advance circuits on ALD page CQ 101.

SINGLE INSTRUCTION (SI): Pressing the start switch with the mode switch on SI causes the execution of one instruction. Data channel operations are prevented.

Position 2 of the mode switch activates the single-instruction-or-stop line which conditions the turn off of the run flip-flop with end-op-T-7, causing the processor-controller to stop after executing one instruction. This position of the mode switch conditions the interrupt but not the cycle steal circuits.

SINGLE STORAGE CYCLE (SSC): Pressing the start switch with the mode switch on SSC causes one core storage cycle. Single storage cycle operations (usually called single cycle operations) can be used in conjunction with the console cycle lights to step through instructions and to analyze processor-controller operation.

Position 3 of the mode switch activates the single-storage-cycle-mode line which conditions the turn off of the run flip-flop at T-7 time, and note that this turn off is not conditioned by end-op; therefore, the processor-controller executes one core storage cycle only. The single-storage cycle line prevents the turn off of the mode set flip-flop (ALD page CS121) to keep the interrupt polling and interrupt request circuits conditioned. This mode does not allow cycle stealing.

SINGLE STEP (SS): Pressing the start switch with the mode switch on SS causes one processor-controller clock step (T0 through T7 or X0 through X7). The single-step-mode line (mode switch position 4) conditions the turn off of the run trigger with the fall of start advance. The start key turns on the start-advance flip-flop and the B phase from the oscillator turns off start advance, therefore the run flip-flop is on for one clock step. Single step mode conditions the A-phase-power line to be active only while the delay flip-flop is on, and the B-phase-power line to be active only when the delay flip-flop is off. Single step mode also conditions the cycle steal circuits and the interrupt circuits.

TRACE: This position of the mode switch causes a trace interrupt after the execution of each instruction. The trace interrupt is a unique interrupt. It has no device status word, no interrupt level status word, and cannot be masked. The trace interrupt is the lowest priority customer interrupt. Once initiated, it is delayed by the occurrence of any other interrupt. It cannot occur while other interrupts are being serviced. When the trace interrupt occurs, the processor-controller executes the forced BSI and branches to the routine whose address is stored at 0009 (see interrupt section).

The trace mode (mode switch position 11) ANDs with not-branch-out to turn on the interrupt-level-trace flip-flop. Position 11 is jumpered to positions 9 and 12 to decondition the end-op-T-7 turn off of the run flip-flop to allow the processor-controller to operate as in the run mode. This line also conditions the interrupt request, interrupt polling, and cycle steal circuits.

LOAD: Pressing the start switch with the mode switch in the load position causes the contents of the data entry switches to be stored at the address specified by the I register (the processor-controller must be in a stopped condition and there must be no storage-protect-bit in the core storage word). The I register is incremented during each load operation.

Pressing the Load I switch with the mode switch in the load position causes the contents of the data entry switches to be loaded into the I register. The load mode (mode switch position 10) activates the I/O-to-B-register-gate line. This line turns off the parity-sample flip-flop to disable parity checking during this operation. The load-mode line also deconditions the turn on circuits for the parity-error flip-flop. The I/O-to-B-register-gate line activates the channel-bus-to-B-register line to gate the contents of the data entry switches into the B register. The load-mode line activates the load-display-IPL-or-core-storage line which forces up the wait-op line. Wait-op conditions the run flip-flop to be turned off at T 7 time, causing the processor-controller to run for one cycle to load the contents of the B register (data entry switches) into the core storage.

The operating point of the load I push button connects to position 10 of the mode switch to activate the set-I-register line. The set-I-register line activates the B-to-I-register-gate line to load the contents of the B register (data entry switches) into the I register.

DISPLAY: Pressing the start switch with the mode switch in the display position causes the data at the I register address to be displayed in the console B register lights. The I register is incremented during the operation. Successive words are displayed with successive depressions of the start key. Position 9 of the mode switch activates the display-mode line. This line activates the load-display-IPL-or-clear-storage line which forces up the wait-op line. Wait-op conditions the run flip-flop to be turned off at T 7, allowing the processor-controller to run for one cycle only. This cycle will leave the data at the core storage location specified by the I register displayed in the B register.

The interrupt circuits and the cycle steal circuits are not conditioned during this operation.

Data Control Indicators

Arithmetic Control

- On during arithmetic operations including effective address generation.

- Indicates the on condition of the arithmetic-control flip-flop.

The arithmetic-control flip-flop is turned on by:

1. T3 time of any I1 cycle that requires an effective address generation,
2. The I1 cycle of the store index operation,
3. The E1 cycle of any arithmetic operation other than multiply,
4. The E1 cycle of the modify index operation,
5. During the I2 cycle if the tag bits are not equal to zero and an index operation is not specified,
6. During the modify index operation I2 or IA cycle if the format bit equal one and the tag bits are not equal to zero.

The arithmetic-control flip-flop is turned off at T0 time by the DC-reset-op-register line.

During the divide operation it is turned off by the divide reset A register line or when the shift counter equals 0 or 1. It is also reset when the D register equals 0 and the double precision carry line falls. The timing charts for the various arithmetic operations show the turn on and turn off times for the arithmetic control flip-flop.

Shift Control

- This indicator is on when the shift control flip-flop is on.

The shift control flip-flop is turned on at T3 time when the op decode circuits decode a shift operation and at T3 time of multiply operation E cycles. It is turned off by DC-reset-op-register or during I cycles if the shift counter equals zero. It is also turned off by a B-phase pulse during a shift operation when the shift counter equals zero or the shift left and count bit is detected.

Add

- This indicator is on when the add flip-flop is on, which is for any arithmetic operation and for I cycles that require effective address generation.

The add flip-flop is turned on at T3 time of any cycle that requires the D register to be added to the A register. (It is not on for a subtract operation.) It is reset at T0 of I cycle 1 by the DC-reset-op-register line. During the divide operation, E cycle 1, it is turned off when the arithmetic-sign flip-flop is turned off.

Arithmetic Sign

- During an arithmetic operation this lamp indicates that the signs of the two factors were not initially equal.

The arithmetic-sign flip-flop is turned on at T2 time of a divide E cycle if the A register, bit 0, is equal to one. It is turned on at T3 time of an add or subtract E cycle if the signs of the two factors are not equal. It is turned on at T3 time of a divide E cycle if the B-register-bit-0-latched flip-flop is on. It is also turned on at T3 time of a multiply E cycle if the B-register-bit-0-latched flip-flop is on. The arithmetic-sign flip-flop is reset by the next T3 time if any of the turn-on conditions are still active, at T1 time of a divide E cycle, or by the DC-reset-op-register line.

Zero Remainder

- This indicator is on at the end of a divide operation if the accumulator indicates a zero balance or if a quotient correction is not required.

The zero-remainder flip-flop is turned on at T3 time of a divide operation E cycle when the shift counter has reached a count of one (17th cycle). If the arithmetic-sign flip-flop is off (like signs) the zero-remainder flip-flop is turned off at T3 time of a divide E cycle when the shift counter equal one and if the B-register-bit-0-latched flip-flop is on. It is also turned off by the DC-reset-op-register line.

Branch

- This indicator is on when the branch-2 flip-flop is on.
- Branch-2 flip-flop is on during T7 time of the branch or skip on condition operation, the modify index instruction, the load index instruction or the shift left and count instruction.

The branch-2 flip-flop is used to extend the T7 cycles of instructions other than arithmetic instructions.

It is turned on at T7 time of the cycle in which the branch-1 flip-flop is turned on. The branch-1 flip-flop is turned on at T6 time of a shift left and count instruction, an LDX instruction, and MDX instruction, or a BSC with format equal one. The branch-2 flip-flop is reset when the branch-1 flip-flop is reset or by DC reset. The branch-1 flip-flop is reset after one cycle.

Storage Protect Bit

- This lamp is on when the storage-protect-bit flip-flop is on.

- Storage-protect-bit flip-flop is turned on when the storage protect bit sense amplifier is activated from core storage or at T3 time when the storage-protect-set-gate is activated.

- The storage-protect-bit flip-flop is turned off by DC-reset-B-register or at T3 time when the storage-protect-reset-gate is active.

During any core storage read cycle, the storage protect bit sense amplifiers will turn on the storage-protect-bit flip-flop if there is a storage protect bit stored in the addressed position of core storage. The storage-protect-set-gate, which conditions the turn on of the storage-protect-bit flip-flop, is activated if the mod-15 flip-flop is on, the write-storage-bit toggle switch is on, and a store status instruction (with format equal 1 and modify bit nine equal 1) is being executed. The storage-protect-reset-gate which turns off the storage-protect-bit flip-flop is activated when the mod-15 flip-flop is off, the write-storage-protect-bit toggle switch is on, and the store status instruction (with format = 1 and mod bit 9 = 1) is being executed. This line is also activated if the mod-15 flip-flop is off, the write-storage-protect-bit toggle switch is on and the clear-storage push button is being held depressed.

Parity Bit

- This lamp is on when the parity-bit flip-flop is on.

- The parity-bit flip-flop is turned on by the parity bit sense amplifiers, the in bus parity generator, or the parity generator for the out bus.

- The parity-bit flip-flop is turned off by the DC-reset-B-register or by either of the parity generators.

The parity-bit flip-flop is effectively an extension of the B register. During the core storage read cycle it is turned on by the parity bit sense amplifier if the parity bit of the addressed core storage word contains a one bit. During the write cycle, this flip-flop, if active, controls the inhibit drivers to write a one bit in the addressed position of core storage.

Interrupt Service

- This lamp is on during the I-1 and I-2 cycle of the forced BSI instruction.

The interrupt service indicator is on when the any-interrupt-request line is active. Any-interrupt-request is active when the master interrupt-request flip-flop is on, and the other conditions exist that enable an interrupt. The master interrupt-request flip-flop is turned off at T7 of the I 2 cycle when the shift counter equal zero.

Cycle Steal Service

- This lamp is on when the any-cycle-steal-cycle flip-latch is on.

The any-cycle-steal-cycle flip-latch is turned on by any cycle steal level 0 through 8 or the interval timer cycle steal cycle. It is turned off at the end of a cycle steal cycle.

Auxiliary Storage

- This lamp is on when the auxiliary storage is being addressed.

The auxiliary storage indicator is on when the storage address bit AUX line is active. This line is activated by the force auxiliary switch on the I/O monitor interface panel or by the CE interrupt with the interrupt to auxiliary/main storage switch in the auxiliary position.

Op Code Check

- This indicator is on when an invalid op code is in the op register.

The op code check lamp is operated by the illegal-op flip-flop which is turned on at T4 time of an I-1 cycle if the op register contains an invalid op code, as shown on MDM page CC30102. The illegal-op flip-flop is turned off by the DC-reset-op-register line.

Storage Protect Check

- Turned on when an attempt is made to write into a "read-only" location.

- This indicator is lighted directly from the storage-violate flip-flop.

The storage-violate flip-flop is turned on if the B register gate is active, indicating a storage write operation, and the storage protect bit is active, indicating a read-only core storage location is being addressed. The storage-violate flip-flop is turned off by the DC-reset-B-register line.

When the storage-violate flip-flop is turned on, if an XIO data cycle is not active, the check indicator (interrupt level) is turned on. The storage-violate flip-flop can then be turned back on to indicate any subsequent storage protect error.

Parity Check

- Turns on when a parity error (even number of bits) is detected in the B register.

The parity check indicator is operated directly from the parity-error flip-flop. The parity-error flip-flop is turned on when conditioned by the parity-sample flip-flop and the storage-write-use line, if the parity generator from the B register indicates the parity bit is required and the parity-bit flip-flop is not on. The parity bit flip-flop is also turned on if the parity generator indicates that a parity bit is not required and the parity flip-flop is on. The parity-error flip-flop is turned off by the DC-reset-B-register line.

When the parity-error flip-flop is turned on, if an XIO data cycle is not active, the check indicator (interrupt level) is turned on. The parity-error flip-flop can then be turned back on to indicate any subsequent parity error.

Clock 0 through 7

- These eight lamps are on when their respective T clock or X clock flip-flops are on.

These indicators show the advance of the processor-controller clock (T) or the cycle steal clock (X) during start-key depressions when the mode switch is in the single step (SS) position.

Cycle

- These five lamps (I1, I2, IA, E, and E1) indicate the part of an instruction that is being executed by the processor-controller.

I1: This lamp shows that a new instruction is being set up for execution. This lamp is operated directly from the I1 flip-flop which is DC reset on, or is turned on after the last cycle of every operation (end op T0). It is turned off at the next T0 if not end op.

I2: This lamp shows that the second word of a double word instruction is being set up for execution. The lamp is operated directly from the I2 flip-flop. The I2 flip-flop is turned on at T0 following I1 if the format bit is a one. It is turned off at the next T0 time.

IA: This indicator shows that the instruction being set up is a double word instruction that has an indirect address. The indicator is on while the indirectly addressed word is being read out of storage. The lamp is operated directly from the IA flip-flop, which is turned on at T0 time of a two word instruction (bit 5 = 1). If the IA bit (bit 8) is a one it is turned off at the next T0.

E: This indicator shows that the instruction set up during I time has been defined by the op code and is now being executed. The lamp is operated directly from the E flip-flop, which is turned on at T0, following any I cycle if end op is not active or if conditions do not exist to turn on I2, I3, or IA. It remains on for any E1, E2, or E3 cycles and is turned off with end op T0.

E1: This lamp is operated directly from the E1 flip-flop which is turned on with the E flip-flop. It is turned off with the next T0 pulse.

If the E cycle stays on for the following cycle, that cycle is an E2 cycle. The third E cycle is an E3 cycle (XIO instruction only). There are no E2 and E3 console indicators.

Timers

- Three lamps (A, B, C), when on, indicate that their respective interval timers are in operation.

The timer A lamp is operated from the off side of the timer-A flip-flop. The timer-A flip-flop is turned

off by a control function with an IOCC modifier bit 0 = 1. This condition enables the interval-timer-A to operate. The timer-A flip-flop is turned on (lamp off) by a timer control function with an IOCC modifier bit 0 = 0.

Interrupt Levels

- Twenty seven indicators (0 through 23, check, trace, and CE) indicate when an interrupt is being requested (if not masked) or serviced.

The interrupt level lamps are operated directly from the level flip-flops which are turned on by requests from the interrupting devices. However, if the mask flip-flop is on, the level flip-flop cannot be turned on. It is turned off by a branch out of interrupt (BOSC) instruction executed at the end of the interrupt routine for that level.

Op Code

- Five indicators (0 through 4) display the op code of each instruction in a binary form.

These lamps operate directly from the op register flip-flops. These flip-flops are turned on by B register bits 0 through 4 at T2 time of the I1 cycle. They are reset at T0 time of the next I1 cycle.

F (Format)

- Indicates that a two word instruction is specified.

This lamp is operated directly from the format-bit-5 flip-flop which is turned on at T2 time of an I1 cycle if the B-register bit 5 = 1. It is turned off at T0 time of the next I1 cycle.

Tag

- Two lamps indicate the index register specified for modification of the instruction addressed.

The tag register indicator lamps are operated directly from the tag register bit 6 and 7 flip-flops. These flip-flops are turned on at T2 time of an I1 cycle if B register bit 6 or 7 = 1. They are turned off at T0 of the next I1 cycle.

IA (Indirect Address)

- For double word instructions, except BOSC operations and a modify index operation, indicates that the effective address is an indirect address.
- For BOSC operations, used with bit 9 to modify the instruction.
- For the modify index operation, indicates an add to storage function.

The indirect address indicator is operated from the modifier register bit-8 flip-flop. This flip-flop is turned on at T2 time of an I1 cycle if the B register bit 8 = 1. It is also turned on by the add-to-storage-interlock flip-flop during a modify index operation. It is turned off by the DC-reset-op-register line.

BO (Branch Out)

- During a BSC instruction, this lamp indicates a branch-out-of-interrupt (BOSC).

This lamp is operated from the modifier register bit-9 flip-flop, which is turned on at T2 time of an I1 cycle if B register bit 9 = 1. It is turned off by the DC-reset-op-register line.

CAR (Carry)

- During an arithmetic operation, this lamp indicates a carry out of high order position of the accumulator.
- During a shift-left operation, this lamp indicates that the high order position of the accumulator = 1.
- During a load status instruction, this lamp indicates that the carry flip-flop was turned on.
- During a shift-left and count instruction, this lamp indicates that a shift into the high order position of the accumulator occurred before the shift counter reached a count of zero.

The carry indicator is operated by the carry flip-flop. This flip-flop is turned on during an arithmetic operation if a temporary-carry flip-flop is on. During a shift-left operation, it is turned on when the A register bit 0 = 1. During a load status instruction, it is turned on if the D register bit-14 = 1. During a shift-left and count operation, it is turned on if the

branch-1 and branch-2 flip-flops are on and the shift counter is not equal to 0. The carry flip-flop is turned off by: a BSC instruction that tests the carry flip-flop, a load status instruction that specifies the turn off of the carry flip-flop, or an SLC operation if the branch-1 and the branch-2 flip-flops are on and the shift counter is equal to 0.

Overflow

- During an add, subtract, or divide operation this lamp indicates that the operation has produced a result larger than can be accurately represented in the accumulator.

- During a load status instruction, this lamp indicates that a turn on of the overflow indicator is specified.

The overflow indicator is operated directly from the overflow flip-flop. The turn on circuits for the overflow flip-flop are shown in MDM page CC50102. This flip-flop and its associated indicator are turned off by: a BSC instruction that tests the overflow flip-flop, or a load status instruction that specifies the turn off of the overflow flip-flop.

Data Flow Indicators

Address Register

- These 16 lamps indicate the contents of the storage address register (M register) or any channel register as selected by the display-address-register switch.

These lamps are turned on by the active condition of their respective positions of the storage address in bus. This bus is gated during the storage address cycle and by the display-console line, which is active when the clock is stopped.

I, B, D, A Registers

- These lamps continually display the contents of their respective registers.

Data Registers

- These 16 lamps display the contents of the Q register, any index register, or the shift counter as selected by the display data register rotary switch.

The contents of the selected register are gated to these lamps by the display-console line, which is active when the processor-controller is in a stop or a wait condition, at T7 time.

Toggle Switches

Sense and Program

- The contents of these 8 switches can be stored in bit position 0 through 7 of the A register or a core storage location.

An XIO instruction specifying an IOCC with an area code of 0, a function of read, and a unit address (bits 8, 9, and 10) of 011, stores the contents of the sense and program switches at the core storage address specified by the IOCC. An IOCC with area code 0, a function of sense device, and a unit address (bits 8, 9, and 10) of 011 load the contents of the sense and program switches into the accumulator.

Operations Monitor

- Operating this switch to the on position starts the operations monitor. The off position disables the monitor.

The normally closed contacts of the operation monitor toggle switch applies a minus level to disable the operations monitor circuits. Turning on this switch activates the operations-monitor-coil line. This line starts the operations monitor timing out in the time interval selected by a rotary switch on the I/O monitor interface panel.

Disable Interrupt

- Masks all interrupt levels including internal (check) errors.

This switch can be used during servicing to choose the time at which the program may be interrupted. The highest, unmasked, level that is active is serviced when the switch is turned off. The normally open contacts of this switch must be inactive (switch off) to gate the output of the interrupt level flip-flops to turn on the interrupt request flip-flops.

Check Stop

- When on, stops the processor-controller when one of the following errors occur: invalid operation, parity error, or storage protect error.

- The stop occurs at the end of the core storage cycle in which the error is detected.
- The start key must be pressed to restart the system.
- When the check stop switch is off, an internal error initiates an internal interrupt.

A channel address register (CAR) check internal error initiates an internal level interrupt regardless of the position of the check stop switch.

The check stop switch, when active (switch on), ANDs with parity error, storage violate, or illegal ops to activate the error-check-stop line. This line, when activated, turns off the run flip-flop and inhibits any interrupts. The error-check-stop line also ANDs with a not run condition and the X7 pulse to inhibit further advance of the X clock.

Write Storage Protect Bits

- This switch enables the writing or clearing of storage protect bits in core storage.

The normally open side of this switch, when active, (switch in YES position) is used with the clear storage switch or with the store status instruction to activate the storage protect set gate or storage protect reset gate, depending upon the condition of the mod-15 flip-flop. The normally open line is also used to turn off the parity-sample flip-flop for the clear storage or store status operations (see clear storage switch description, this section). Operation of this switch during P-C operation may cause a parity error.

Data Entry Switches

- The contents of these 16 switches (bit 0 switch-bit 15 switch) can be stored by either manual or programmed control.
- Contents can be loaded into the I register by the load I key, when in load mode.
- The contents of the switches can be loaded into the accumulator by a sense device command.

The contents of the data entry switches are gated onto the channel data bus by the gate-bit-switches line, which is activate by the load mode switch, or by the XIO read command or XIO sense command with the bit switches selected. The channel data bus lines are gated into the B register. If the operation is an XIO read command, the B register contents are stored into core storage. If the operation is an XIO sense device command, the B register contents are gated into the accumulator. If the mode switch is in the load position, and the load I key is pressed, the B-to-I-register-gate line is activated and the contents of the B register (data entry switches) is loaded into the I register.

SECTION 2. MAINTENANCE FEATURES

- Hardware and program checks enable on-line servicing.
- Non-vital units can be program-disconnected for off-line servicing without serious interruption of the customer's process.

The primary objective of the maintenance plan is to provide the customer with the maximum usage of those system components necessary to control his process. To accomplish this, hardware and programmed checks have been provided to allow continued operation of vital components in spite of transient failures.

Hardware and programmed checks are also provided to permit detection of solid failures of non-vital components. When a non-vital component fails it can be program-disconnected for off-line servicing without severely jeopardizing the application. In general, it is assumed that items such as paper tape readers and punches, card readers and punches, and high speed printers are not essential to the control of the process.

By the above expedient, the system will go down only when it is severely degraded by frequent transient errors, or a solid failure has occurred in a vital function or component.

The plan also incorporates the ability to tolerate certain solid failures within the vital components. An example of this would be a multiplexer point which fails in the open condition. Failure of a single multiplex point is considered to be a failure for which the customer will not relinquish control of his system. Therefore these units will be repaired only after multiple failures have occurred.

Failure of critical areas of the system will necessitate an immediate interruption to customer use of the system. Rapid repair is essential in these instances. To minimize the amount of down time, the 1800 System is functionally assembled to permit rapid diagnosis, isolation, and repair. Each of the selective features is packaged as a discrete functional assembly, permitting disconnection or attachment to the system without affecting the performance of any other feature or unit.

Hardware Checks

Within the processor-controller, all data is checked when read from core storage. The P-C also checks

for illegal operation codes in the Op code register, and it checks for an attempt to write into a storage-protected word in storage. These latter two checks detect both faulty programming and faulty circuits. All of the above checks cause a highest-level interrupt on error. Examination of the device status word (DSW) for the processor-controller indicates the cause of the interrupt.

The I/O adapters also contain checking circuits. The outputs of these circuits are the sensed indicators which make up the device status word. The DSW, through proper programming techniques, can be used to identify the type of failure and to guide corrective action in the operating program. The DSW can also be used to log errors during customer run time for later analysis by the Customer Engineer.

Programmed Checks

For rapid diagnosis and highest reliability, programmed checks should be placed at frequent intervals throughout the operating program. When an error is detected, the program should include a restart procedure to prevent an unscheduled interruption, and should include complete error logging of all pertinent facts for use as a diagnostic tool by the Customer Engineer.

Diagnostic Programs

The 1800 system diagnostic programs include function tests, auxiliary exercisers, one-card scope routines, timing tests, and utility programs.

The function tests include basic CPU checkout and I/O function tests. The auxiliary exercisers provide on-line (shared operation with customer's program) exercising of I/O units. Scope routines are short loop programs designed specifically for scoping. Timing programs test a specified timing or facilitate an adjustment. Utility programs assist in using the diagnostic test programs.

The maintenance diagnostic programs are described in the 1800 system maintenance manual (see FE bibliography 1800 system, Form Y26-0560) and are fully documented in the diagnostic program manuals provided with the system. The diagnostic program manuals include a system summary, an operation summary, and the program listings.

I/O Monitor Interface Panel

- The interface panel (Figure 6-5) contains connectors and manual controls for servicing the 1800 system.

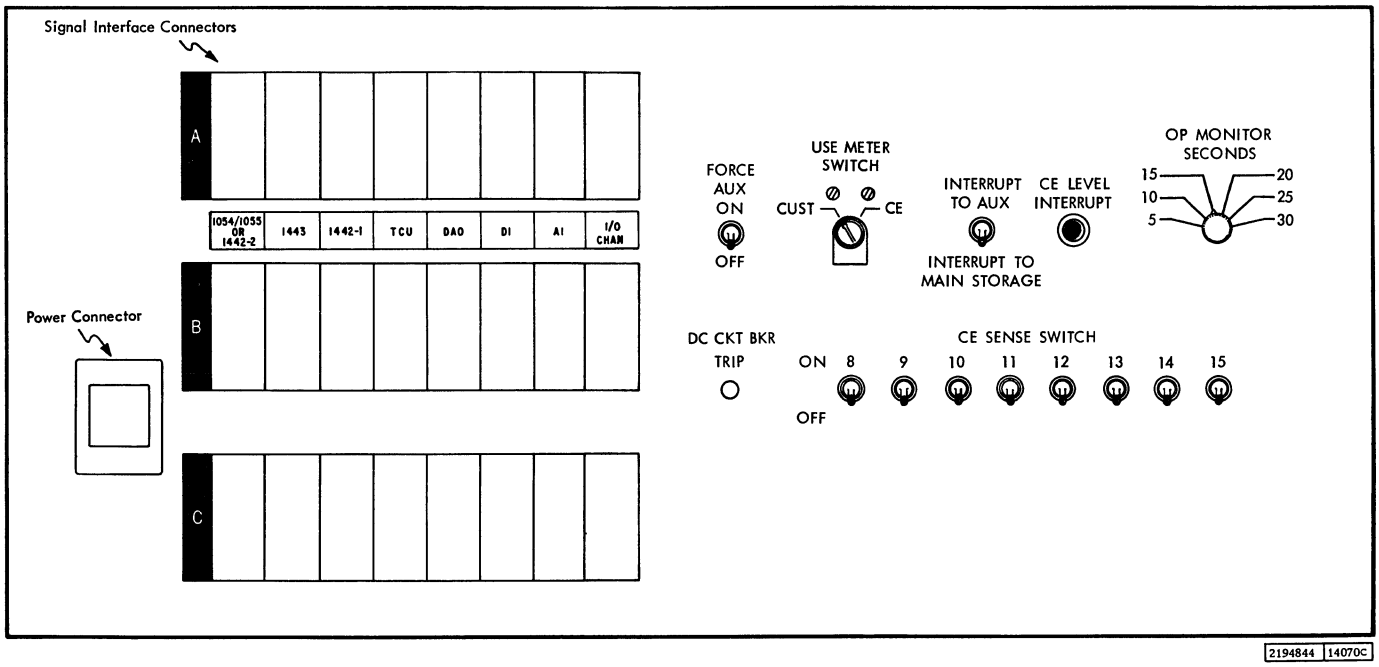


Figure 6-5. I/O Monitor Interface Panel (1801 or 1802)

Interface Connectors

- A power connector provides SLT voltages to the I/O monitor unit.

- There are three signal connectors (A, B, and C) for channel and for each device attachment that employs the I/O monitor unit.

Channel control and the following device attachments are monitored via signal connectors on the interface panel:

Analog Input
Digital and Analog Output
Digital Input
1443 Printer
1054/1055 Paper Tape
1442 Card Read Punch
2401/2402 Tape Control Unit

The number of signal connectors and the arrangement on the panel will vary according to the system configuration. Decals are used to identify the connectors.

The signal interface lines provide a convenient means of delivering prime test point data to the I/O monitor unit from the device under test.

Force Auxiliary On/Off Switch

- This toggle switch enables the initial loading from card or paper tape into auxiliary storage.

The resident loader program for diagnostic routines can be loaded into auxiliary storage through the initial program load function when this switch is on. The entire processor-controller is used but main core storage cannot be addressed.

The normally open side of the force auxiliary switch activates the auxiliary-storage-select line, which activates the auxiliary-storage-bit line to select auxiliary storage (Figure 6-6).

Interrupt to Auxiliary/Main Storage

- This toggle switch, in the auxiliary position, causes a CE interrupt branch vector into auxiliary storage address 0001_{16}. The return address is stored in $000A_{16}$ of main storage.

- In the main storage position, this switch causes a CE interrupt branch vector into main storage address 0001_{16}. The return address is stored at $000A_{16}$ of main storage.

The normally open side of the interrupt to auxiliary/main storage switch activates the auxiliary-CE-interrupt line. This line conditions the CE-interrupt-auxiliary-storage flip-flop to be turned on at end op T7 time if the CE interrupt level is active (Figure 6-6). The CE-interrupt-auxiliary-storage flip-flop activates the auxiliary-storage-bit line which selects auxiliary storage.

CE Level Interrupt

- This push-button switch causes a CE interrupt into auxiliary storage or main storage, depending upon the position of the interrupt to auxiliary/main storage switch.

Pressing this switch turns on the CE-interrupt-shaper flip-flop which turns on the CE-interrupt-request flip-flop (Figure 6-7). The CE-interrupt-request flip-flop output is ORed with the polled I/O bit 15 from an I/O device that is in the CE mode to turn on the level CE flip-flop in the interrupt register.

CE Sense Switches

- These eight toggle switches are used with the console sense and program switches to direct diagnostic exercises.

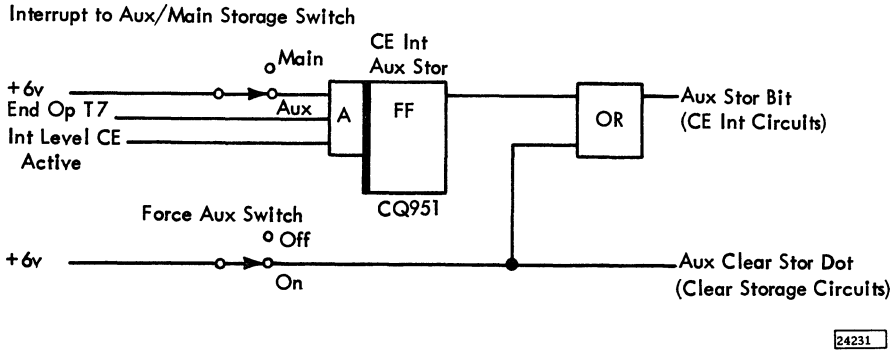


Figure 6-6. Interrupt to Aux/Main Storage and Force Aux Switches

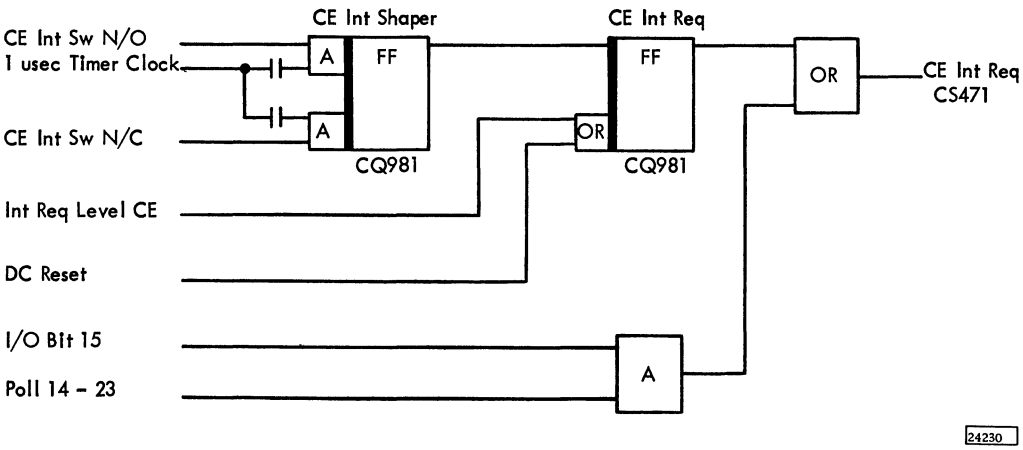


Figure 6-7. CE Interrupt Switch

- On a sense-device command, these switches enter bit positions 8-15 of the DSW.
- On a read command, these switches enter core storage in the location specified by the I register.

The normally open side of the CE sense switches is gated to the channel data bus by the gate-program-switches line.

NOTE: This circuit uses negative logic. That is, when the sense switch is on and the gate-program-switches line is active an AND circuit is deconditioned, then inverted to activate the channel-data-bus-bit line (ALD page CT141). The channel data bus lines are gated into the B register by an XIO input function at T3 time of the XIO data cycle. If the XIO command is a sense device, the B register contents are loaded into the accumulator. If the XIO command is a read command, the B register contents are stored in core storage at the location specified by the I register.

DC Circuit Breaker Trip

- This lamp turns on if an overcurrent CB trips in any MPS (medium power standard) power supply in the 1801/1802 or 1826.
- The +48v supply and the power-failure-protect supply are not MPS power supplies and have no circuit breakers.

The overcurrent circuit breaker normally-open points are connected in parallel (Figure 6-8) so that if any circuit breaker is activated, this lamp will light.

Use Meter Switch

- A key switch, operated by the Customer Engineer's use-meter key.
- In Customer position, this switch conditions the use meter circuits in the I/O units.
- In CE position, this switch deconditions the use meter circuits in the I/O units.

The Use Meter switch, located on the I/O Monitor Interface panel, can be operated only by the CE use-meter key. The use meters, in the I/O units, are conditioned by the normally-closed contacts of this switch and by a signal line, such as "busy", that indicates the unit is being used.

When turned to the CE position (normally-open), the switch prevents the use meters from accumulating time. The switch must be in the Customer position to remove the key.

I/O Monitor Unit

- The I/O monitor is a portable service aid containing three latching display registers.
- Controls on the monitor permit the setting and resetting of these registers.
- The status of device signals can be examined at any point in the device cycle.

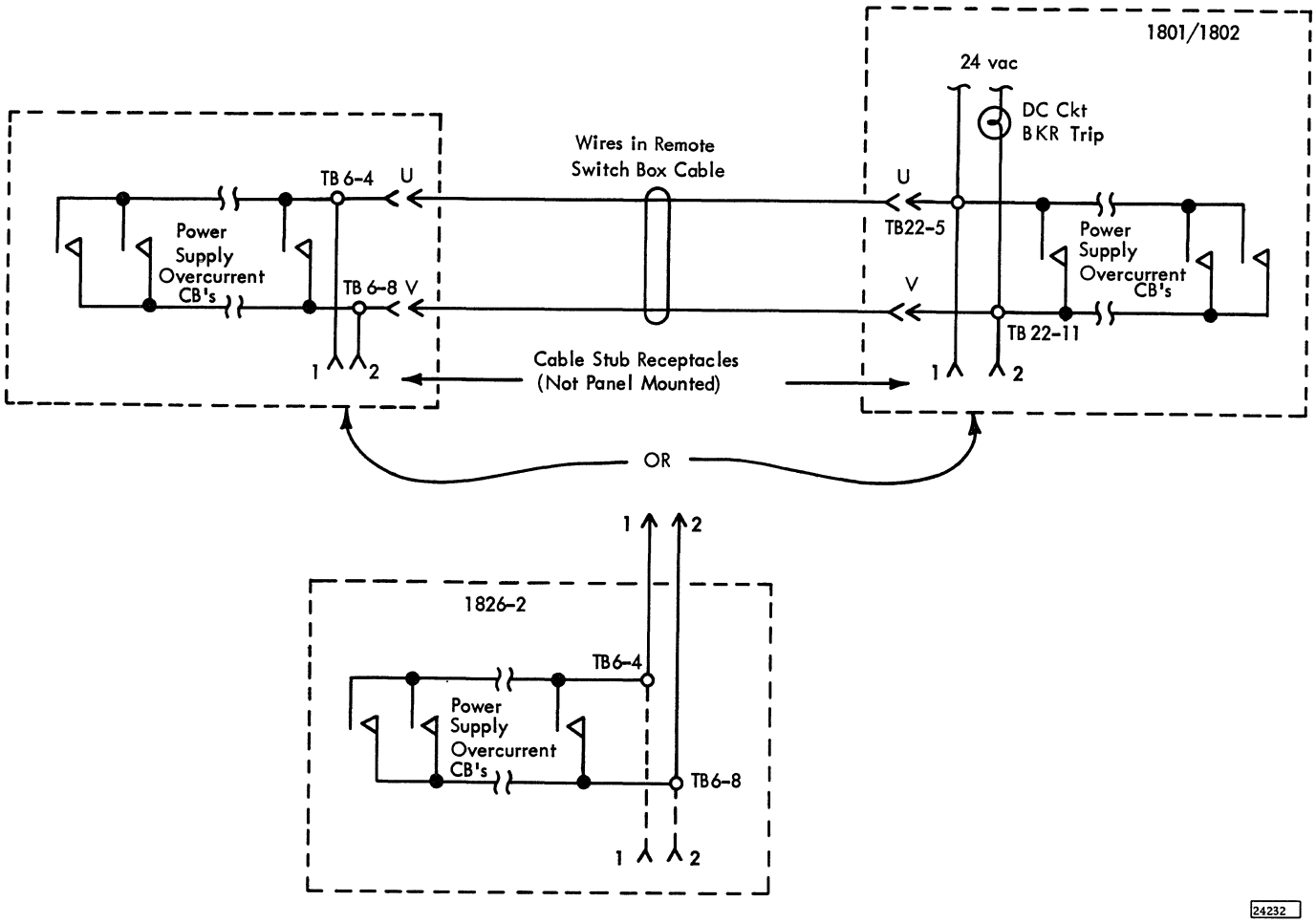


Figure 6-8. DC Circuit Breaker Trip Lamp

- This unit also provides a means for comparing or analyzing display data to enable error detection or data searching.
- A sync probe can be used to set the display registers with SLT signals.
- Data is brought to the three display registers via pluggable connectors, one for each display register.
- MDM page WA40101 shows the I/O Monitor circuits.

The monitor can be used as a simple display unit or it can be used in a dynamic manner to trap intermittent fault data, to cause address or data stopping of the processor-controller, or to generate scope sync pulses.

Applications

Operation of the I/O Monitor unit is described in the 1800 system maintenance manual (see FE bibliography 1800 system, Order No. SY26-0560).

One method of checking an I/O operation is by comparing the timing chart in the system MDM pages with the I/O Monitor unit indicators.

The Console mode of operation provides a means of checking devices which can be single cycled or which are hung up.

The Sampled and Gated modes provide a check of devices which cannot be single cycled or any device being operated by the customer. This ability provides a method for detecting and capturing intermittent or solid fault data.

The syncing features permit the selection of the operation and time for a check-out operation. The modes of operation (Sampled or Gated) provide the

ability to check a specific cycle within the operation or an over-all summarized check.

The B-Register Compare switches provide a method for automatic analysis of display data. In effect, these switches eliminate the need to observe each display to decide if the operation is proper. The proper operation data is set into these switches and each display cycle is automatically checked.

The features which provide automatic check-out also provide processor stopping on addresses or other desired conditions, scope sync generation, and other useful functions.

Operating Philosophy

The I/O Monitor permits the trapping of events occurring any time within a device operation, and trapping events which occur prior to error detection. For this type of trapping, most dynamic display operations employ a fixed sequence of events:

1. Latch displays ON at sync time.
2. Hold (trap) the latched display data if an error is detected subsequent to sync time.
3. Automatically reset the displays if no error is detected by the end of the operation cycle being monitored.

The trapping of display data is accomplished by inhibiting the automatic reset of data which was latched on at display sync time.

The following sections describe the syncing, holding and resetting of the various display modes. Figure 6-9 is a block diagram of the I/O Monitor registers and controls.

Display Set Up Modes

- There are three basic types of displays which can be set up (latched on) in the I/O Monitor.

CONSOLE DISPLAY: In this mode, the indicator lamps will follow the interface signal line status. When a signal line is up, its indicator is on. When a signal line is down, its indicator is off.

This mode of operation is used during manual cycling or when a hang up occurs.

SAMPLED DISPLAY: This mode of operation provides a "snap shot" type of display. It enables the CE to observe or analyze signal line status as of some specific time within an operation. This mode can be used for address stopping, scope sync generation, data analysis, etc.

GATED DISPLAY: This mode provides a "time exposure" type of display. It enables the CE to observe or analyze the signal lines which come up during an over all operation.

This mode of operation is usually used to analyze control type signals to verify that only the appropriate control lines come up or failed to come up during the operation.

The Sampled and Gated Type displays are dynamic displays. They can be utilized while the system is operating. They do not necessarily require that a diagnostic program be operating. They can be utilized during normal customer operation.

Display Hold (Trapping) and Reset Modes

- The monitor provides the following options for holding or resetting displays under automatic controls.

GATED MODE DISPLAY: With this display mode, the monitor can trap all events which occurred prior to error detection time or all events which occurred at error detection time and subsequently.

SAMPLED MODE DISPLAY: With this display mode, the monitor can trap a desired sample of the events which occurred prior to the error, or the status of the signal lines at error detection time.

Note: When attempting to trap a sample ahead of an error, if the error occurs prior to the defined sample time, the monitor traps with no display indicators on.

TRAPPING A DISPLAY BY ANALYZING THE DISPLAY DATA: With either the sampled or gated display mode, data can be latched into the displays, then analyzed with the B-Display Compare feature and either held or reset depending upon the outcome of the comparison.

SETTING AND TRAPPING A DISPLAY BY COMPARING B-DISPLAY DATA: In the Sampled Mode only, it is possible to utilize the B-Compare feature to scan for a desired address or data combination. When the output of the comparison is as specified, the displays can be both set and trapped.

Scope Sync Generation and Processor-Controller Stopping

SCOPE SYNC GENERATION: Immediately following the setting of displays in both the sampled and gated modes, the B-Compare feature is tested. If the compare result is true, a 150 nanosecond positive pulse

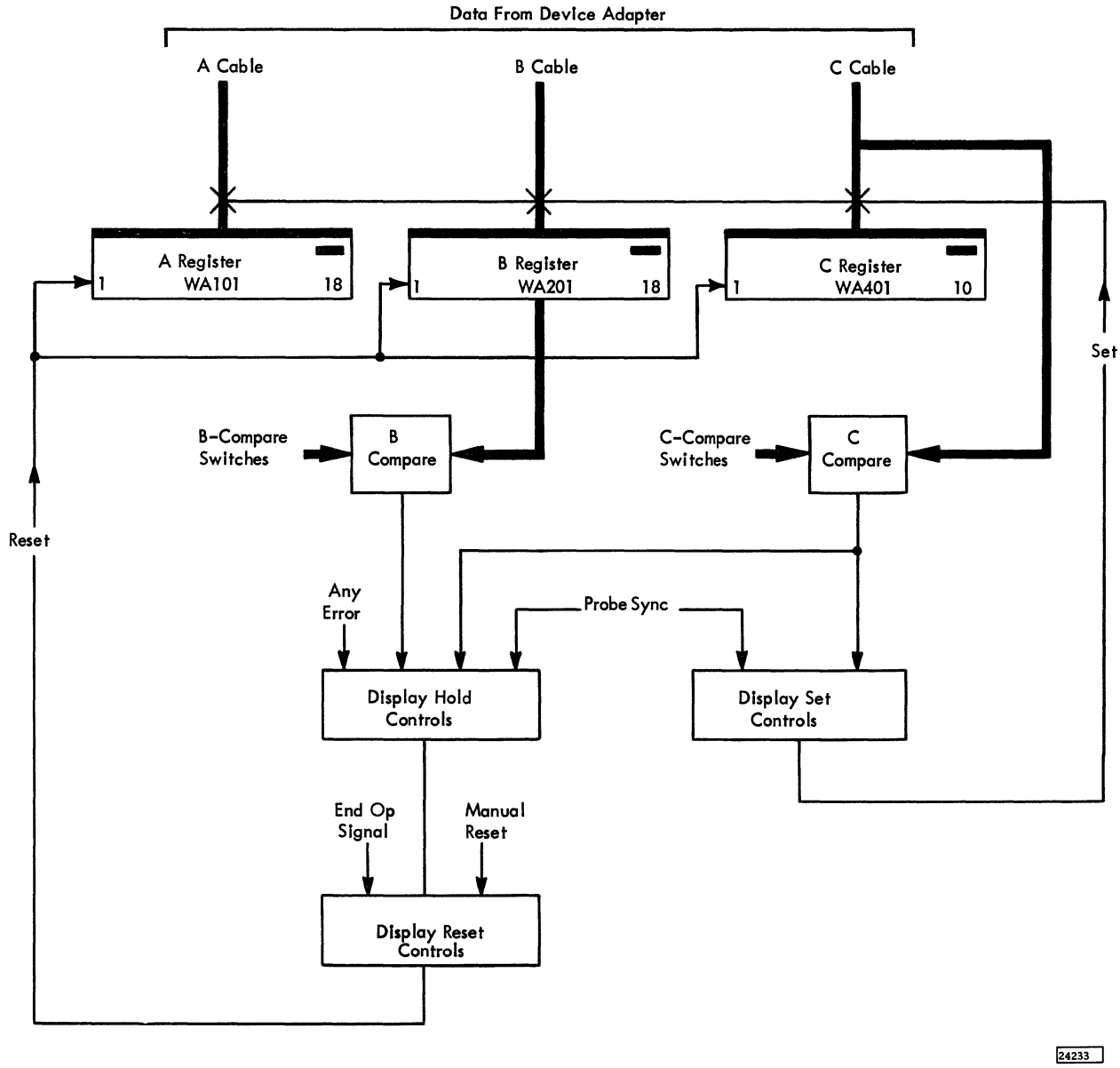


Figure 6-9. I/O Monitor Data Trapping Facilities

is emitted from the B-Compare Exit hub. This pulse can be used as a scope sync.

PROCESSOR STOPPING: By applying a jumper on the processor-controller back panel, the processor Error-Stop circuit is activated when the I/O Monitor display-hold latch comes on.

This procedure, described in the IBM 1800 Data Acquisition and Control System Field Engineering Maintenance Manual (see FE Bibliography - 1800 System, Order No. SY26-0560), is effective only if the I/O Monitor C-Display cable connector is plugged to the Channel Interface C-Connector.

Functional Description

A-DISPLAY REGISTER: This is an 18-position latching display register. Signal lines are brought to the display latches via the A-interface cable connector. This register has no data analysis (comparing) ability.

B-DISPLAY: This is an 18-position latching display register. Signal lines are brought to the display latches via the B-interface cable connector.

B-DISPLAY COMPARE SWITCHES: There is a 3-position toggle switch associated with each indicator

position of the B-display register. These switches are tested at compare time. If the switch settings are the same as the indicator latch status (ON or OFF), a compare-equal condition is generated. When a switch is set to the NULL position, its indicator latch is excluded from the comparison. Each switch in the NULL position renders a compare equal condition for its indicator.

C-DISPLAY: This is a ten position, latching display register. Signal lines are brought to the display latches via the C-interface cable connector.

C-DISPLAY COMPARE SWITCHES: There is a 3-position toggle switch associated with each C-display signal line. When the signal line status (up = ON, down = OFF) agrees with the switch settings (ON or OFF), a C-Compare-Equal condition is generated. The NULL position of each switch provides a means for excluding a signal line from the comparison. Any nulled switch is interpreted as equal in the comparison.

The C-compare-equal condition is employed in the control of the set lines to all display latches. No display can be set in the sampled or gated mode when C-compare is unequal. By setting all C-compare switches to NULL, a continuous C-compare-equal is generated, effectively turning C-compare OFF to enable displays to be set by other syncing means.

The signal lines brought to the C-display are those which are anticipated to be the most frequently used display sync lines.

Notice that the comparison is made directly from the incoming signal lines. This differs from the B-compare method which compared the data in the display latches.

Display Set Control Switches

DISPLAY SET TYPE: This three-position switch selects the basic type of display desired.

Gated Display - This is the "time exposure" type of display. With the switch in this position, the set lines to all display latches come up when the display-set-sync rises and stay up until the display-set-sync falls or is dropped by a device detected error (see Any Error Hold Switch). The display-set-sync is generated by a C-display-compare-equal ANDed with the sync probe input.

While the display-latch-set lines are up, any signal line which comes up causes its display latch to turn on and stay on even though the signal line falls at a later time during the "gated" period.

Sampled Display - This is the "snapshot" type of display. With the switch in this position, the set lines for all display latches come up when the display-set-sync rises. The display-set lines fall 150 nanoseconds after the rise of the display-set-sync.

Only those display latches whose signal lines are up during the 150 nanosecond set-pulse time are latched on.

The display-set-sync is normally generated by a C-display-compare-equal ANDed with the Sync Probe. An exception to this rule exists when the B-Display Compare feature is also ANDed with the above sync generation media (See B-Compare Switch under Display Hold Control).

Console Display - This is the conventional indicator type of display wherein all indicators follow their respective input signal lines (UP = ON, Down = OFF).

In this mode, the display latches are not latched. Both the display set and reset lines to all display latches are continuously held up. Therefore, the signal data flows directly through each latch to the indicator.

With the switch in this position, all other control switches are ineffective and require no set up.

Sync Probe - This three-position switch provides a means for activating or deactivating the sync probe. Remember that the sync probe is always ANDed with the C-compare switches to generate a sync. When the probe is not used, this switch must be in the OFF position or no sync can be generated. In the OFF position, the probe leg of the sync AND circuit is always satisfied.

The Plus In and Minus In settings of this switch activate the sync probe and define the desired level which is to satisfy the probe leg of the sync AND circuit.

The sync probe attaches immediately below this switch. Only a compensated 10:1 probe should be used.

Display Hold Control Switches

B-COMPARE: These switches serve to define the desired B-Compare status ($\neq$ or =) and what is to be done when the desired status occurs.

HOLD: When the leftmost 3-position switch is in this position, the compare "true" status is used to set the display-hold latch on and thereby causes the data in the display latches to be trapped. Once the display-hold latch is on, the automatic reset of the display latches is blocked.

OFF: With the switch in this position, there is no use of the B-Compare result within the I/O Monitor.

SYNC: In this position, the B-compare-true result is ANDed with the C-display-compare and sync-probe input in the generation of the display-set-sync.

Note: The Type switch must be in the Sampled setting to utilize this mode of operation.

In this mode of operation, the display indicators can appear to flash prior to the actual display set time. This flashing results from the method whereby this function is implemented. Recall that the B-compare switches compare the display data in the display latches. They do not make the comparison directly upon the incoming signal line as does the C-compare feature. Therefore, the display set and reset lines are held up during the "searching" operation so that the signal data can "flow through" the B-display latches to the compare switches.

When a B-compare "True" condition occurs at the time C-compare is equal and the sync-probe input is present, the display-reset lines fall and a 150-nanosecond set pulse causes the display latches to be set. The display-hold latch is also set to prevent the trapped display from being automatically reset.

Note: The term B-compare "True" is used because the CE can employ either an equal or unequal B-compare status in his set up.

B-Compare Exit Hub

This hub emits a 150-nanosecond positive pulse each time the B-compare is true. This occurs regardless of the setting the B-Compare (Hold, OFF, SYNC) switch.

At the fall of the display-set lines, B-Compare is always tested and if it is "true", the B-Compare Exit hub emits a pulse.

Notice that it is not necessary to cause the I/O Monitor to trap if only the B-Compare exit pulse is required.

Any Error

Each device interface provides a line which indicates to the I/O Monitor that the device has detected an error. This line does not define the type of error. For this reason the I/O Monitor uses this error line in two ways. It is always brought to the tenth position of C-Display in all device interfaces. This positioning permits the error line to be incorporated into the display-set-sync if desired. The same error line is brought to the Display-Hold-Control, Any-Error switch. When this switch is in the OFF position, the any-error signal is ignored. In the Hold position, the rise of this error line:

1. Causes the display-hold latch to be set on.
2. Once the Hold latch is on, this line prevents the display-set lines from coming up. If they are up at the time the hold latch is on, they are dropped immediately.

Display Reset Controls

AUTO RESET: Each device interface provides two discrete lines in the I/O Monitor interface which define two separate end-op times. For example, a serial card reader could provide one line to denote completion of each column read. The second line could identify the completion of a card read.

These lines permit the automatic monitoring of device operations. For example, for each column or card read, data can be latched into the displays. If the I/O Monitor B-compare feature or the any-error line does not cause the display-hold latch to be set on, the displays can be reset by an end-op so that the next column or card may be automatically monitored.

The three-position Auto Reset switch provides the means for selecting the desired automatic-reset time (End Op I or II). The overlay provided for each device identifies the end-op lines. In the OFF position, with the type switch set to Sampled, no automatic resetting occurs.

In the OFF position, with the type switch set to Gated, an automatic reset occurs immediately following the fall of the display-set-gate if B-compare is not true.

The above exception to the automatic reset rule is necessary to permit the complete monitoring of operations with the gated mode. For example, assume that a column read operation is being monitored and the device circuitry is designed so that the end-op signal rises before the read latch is reset. The I/O Monitor would therefore be reset by the end-op signal before it had completed its display setting and analysis.

Note: Always turn the Auto Reset switch OFF when using the Gated display. This assures proper reset timing.

MANUAL RESET BUTTON: This button provides a means for resetting all I/O Monitor display latches and controls. This is the only means whereby a trapped display can be reset.

Note: Holding this button down does not hold all displays off when the monitor is attached to an operating device. It holds the display-hold latch off because this button applies a DC reset to this latch. A momentary reset pulse is applied to all other display latches when this button is pressed and the sync-interlock latch is on.

Circuit Description

SAMPLE INTERLOCK: This latch and its associated indicator come on when a display-set-sync occurs. Once on, the latch blocks any further display-set-sync generation.

The latch is turned off by either the automatic reset or manual reset.

DISPLAY HOLD: This latch and its associated indicator are set on whenever display data is trapped (see Display Hold Control).

Once on, this latch blocks all automatic resets and prevents any further display-set-sync generation. This latch is turned off only by manual reset.

Signal Lines to Device Adapters

SWITCHES 1-4: These 4 two-position toggle switches are used to send signal levels from the I/O Monitor to the device adapter interface. When these switches are used by the adapter, the device overlay describes their function.

ON - In this position, the interface line associated with the switch is raised to the plus level.

OFF - In this position the interface line associated with the switch is held down.

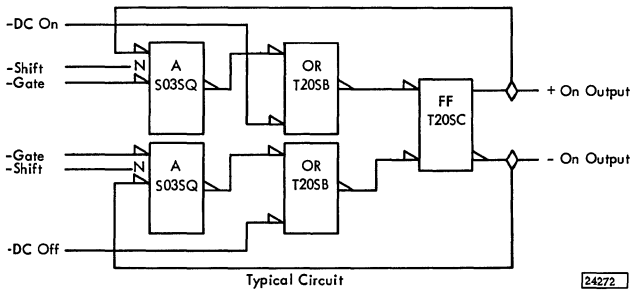
Push Buttons

Button 5 - When pressed, this push button applies to the associated device interface line. If a device employs this button, its function is described on its overlay.

Reset - When pressed, this push button transmits a reset pulse over the associated interface line. This pulse is ORed with the DC reset circuitry in the device adapter.

Note: Do not operate this switch if customer is using the device attached to the I/O Monitor.

MULTI-INPUT (MI) TRIGGER



The MI trigger is used in clock, counter, and register circuits and as a standard flip-flop. Direct-coupled emitter followers are used for the triggering action and inverters are used for the output functions. The trigger may be connected for binary operation, single-gated ac input, dual-gated ac input, or dc set input. Both in-phase and out-of-phase outputs are provided.

AC SET INPUT: External RC packs are used for gated input pulse triggering. The set pulse is a 3V negative shift (+3V to 0.3V) with a minimum duration of 30 nsec. The gate must be conditioned (at 0.3V) for at least 170 nsec before arrival of the set pulse. The gate input remains at an operating level, due to a capacitor charge, for about 90 nanoseconds after the fall of the signal.

DC SET INPUT: For dc triggering, a down level of 0.3V is applied to the dc set input. The down input signal must be at least 30 nsec in duration. For ac set operation, the dc input must be at up (+3V) level.

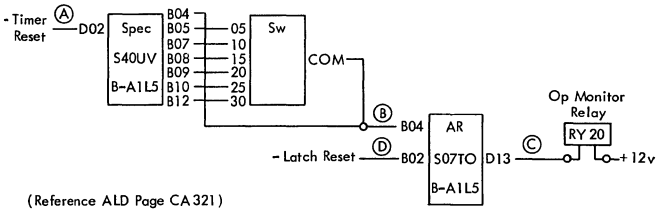
BINARY OPERATION: The trigger can be adapted for binary operation. The binary input pulse is applied to the two ac inputs. The ac gates may be connected to an external gate or tied to 0V.

It is important to note that should another gated ac set pulse be applied to the ON input while the trigger is on, a narrow positive pulse is generated at the OFF output. Likewise, when the trigger is off, a gated ac set pulse applied to the OFF input causes a positive pulse at the ON output.

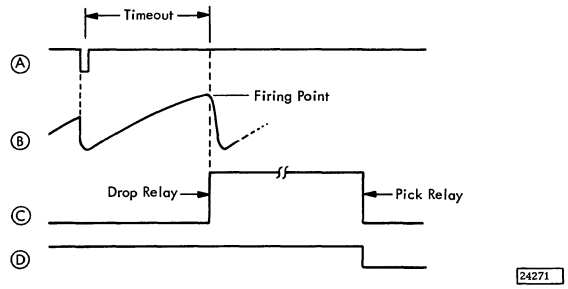
For applications where the "reflected" pulses must be suppressed, the circuit is provided with internal gating that requires the trigger to be OFF before it can be turned on, and vice versa. Circuits with this internal gating can be identified in the ALDs by the output-to-input connections.

OPERATIONS MONITOR

- Provides an adjustable timer which can be reset by an XIO-control command.
- Failure to reset the timer allows the selected time interval to expire and drop the monitor relay.



(Reference ALD Page CA321)



The operations monitor, described in Chapter 2, contains a special circuit that, through an amplifier, holds a relay energized to prevent activation of the alarm circuit. The special circuit contains a capacitor that charges through a resistor to +12 volts.

The amount of resistance, and therefore the charge time, is selected by the Op Monitor rotary switch. These selectable resistors are field adjustable for the correct time intervals. The adjustment procedure is contained in the FE maintenance manual for the 1800 system.

The circuit also contains a silicon controlled rectifier (SCR) and a unijunction transistor. The SCR is turned on by a minus level at pin D02 and provides a discharge path for the capacitor. The unijunction transistor controls the amplifier.

If the capacitor charges to a level sufficient to fire the unijunction transistor, the amplifier allows the relay to drop. The normally-closed points of the relay activate the alarm circuit.

Once the monitor circuit has timed out, the amplifier is latched off and can be reset (on) only by turning off the Operations Monitor toggle switch which connects to pin B02. Through external circuits, this switch also connects to pin D02 to keep the SCR conducting and prevent the capacitor charge.

Appendix B. System Special Features

PROCESSOR-CONTROLLER FEATURES

INTERRUPT LEVELS: There are two groups of six levels available as special features. The basic P-C has 12 levels standard, giving a maximum of 24.

DATA CHANNELS: Provides I/O control to allow data to enter or exit core storage on a cycle-stealing basis. A total of twelve can be installed as special features. The basic P-C has three standard for a total of 15.

SEVEN TRACK COMPATIBILITY (1802 ONLY): Required for writing or reading in seven track mode on the 2401 or 2402 Magnetic Tape Units.

ADDITIONAL CORE STORAGE: Up to 32k words may be added in 8k word increments to a 32k word system for a total capacity of 65k words. Additional modules are housed in the 1803 core storage unit. When the 1803 is added, the 25-32K module is placed in the 1803, with all additional modules.

DATA PROCESSING I/O FEATURES

1054/1055 ADAPTER: Required for attachment of the IBM 1054 Paper Tape Reader and/or the 1055 Paper Tape Punch. (Maximum - one per system.)

1442 ADAPTER: Required for attachment of the IBM 1442, Model 6 or 7. (Maximum - two per system; maximum of one if 1054/1055 is attached.) Requires one data channel for each adapter.

1443/1627 ADAPTER: First prerequisite for attachment of the IBM 1443 and/or 1627 (one adapter accepts both). (Maximum - one per system.)

1443 CONTROL: Second (final) prerequisite for attachment of the IBM 1443. (Maximum - one per system.) Requires data channel.

1627 CONTROL: Second (final) prerequisite for attachment of the IBM 1627. (Maximum - one per system.)

1053 ADAPTER: Required for attachment of second, third, or fourth 1053 Printers. Also a prerequisite for attachment of sixth, seventh, and eighth 1053 Printer when the Output Printer Expander feature is used. (Note: the basic P-C provides for attachment of the first typewriter which can be either the 1816 or 1053.) Maximum - six per system.

OUTPUT-PRINTER EXPANDER: Required for attachment of the second 1816 or the fifth through eighth 1053 Printers. (Maximum - one per system.)

MAGNETIC TAPE ADAPTER: Attaches as many as two 2401 magnetic tape units to the 1802. Note that the seven-track compatibility feature may also be required.

SELECTOR CHANNEL: Provides the capability of attaching the IBM 2841 Storage Control Unit and IBM 2311 Disk Storage Units designed for System/360's to an 1800 System. Other System/360 I/O devices are added by RPQ only.

2790 ADAPTER: Required to attach the 2790 Data Communication System. This adapter is housed in an 1826 model 2 or 3.

COMMUNICATIONS ADAPTER: Required for the attachment of one or two line adapters and their associated data sets and communication lines. One communications adapter can control two line adapters, although, for overlapped operation, each line adapter must have its own data channel. Maximum - four communications adapters (eight line adapters) per system.

PROCESS I/O FEATURES

ANALOG-DIGITAL CONVERTER -- MOD 1: Provides analog-to-digital conversion at system rates to 11K conversions per second. This model includes a buffer amplifier. It accepts bipolar inputs and has program selectable resolution of 8, 11, or 14 bits. (System maximum - two Mod 1 or Mod 2 ADCs in any combination.)

ANALOG-DIGITAL CONVERTER -- MOD 2: Provides analog-to-digital conversion at system rates to 24K conversions per second. This model includes a sample-and-hold amplifier. It accepts bipolar inputs and has program selectable resolution of 8,

11, or 14 bits. (System maximum - two Mod 1 or Mod 2 ADCs in any combination.)

MULTIPLEXER/R CONTROL: Provides multiplexer control for 256 relay points. Prerequisite for Additional Multiplexer/R Control. (Maximum - one per ADC.)

ADDITIONAL MULTIPLEXER/R CONTROL: Provides multiplexer control for additional 256 relay points. (Maximum - three per ADC.)

MULTIPLEXER/S CONTROL: Provides multiplexer control for 256 solid-state points. (Maximum - one per ADC.)

MULTIPLEXER OVERLAP: Provides for simultaneous selection of solid-state and relay multiplexer points. (Maximum - one per ADC.)

ANALOG INPUT DATA CHANNEL ADAPTER 1: Required for analog input operation on one or two Data Channels. (Maximum - one per ADC.)

ANALOG INPUT DATA CHANNEL ADAPTER 2: Required for analog input operation on two Data Channels. (Maximum - one per ADC.)

COMPARATOR: Required for automatic range checking on converted analog input values. (Maximum - one per ADC.) Requires ADC Mod 1 or Mod 2 and AI Data Channel Adapter 1 and 2.

DIGITAL INPUT ADAPTER: Required for control for up to eight Digital Input-Contact, Digital Input - Voltage, or Digital Input - Voltage (High Speed) in any combination. (System maximum - eight Digital Input or Pulse Counter Adapters in any combination.)

DIGITAL INPUT - CONTACT: Termination and sensing for 16 bits of digital information from contacts. (Maximum - 64 per system. See note 1 at end of Appendix B.)

DIGITAL INPUT - VOLTAGE: Termination and sensing for 16 bits of digital information from voltage levels. (Maximum - 64 per system. See note 1 at end of Appendix B.)

DIGITAL INPUT - VOLTAGE (HIGH SPEED): Termination and sensing for 16 bits of digital information from voltage levels for reading at high repetitive speeds. (Maximum - 64 per system. See note 1 at end of Appendix B.)

PULSE COUNTER ADAPTER: Required for control for up to 128 bits of capacity of Pulse Counter - 8 bit, or Pulse Counter - 16 bit, in any combination. (System maximum - eight Pulse Counter or Digital Input Adapters in any combination.)

PULSE COUNTER - 8 BIT: Termination and 8-bit counter for counting input voltage pulses. (Maximum - 128 per system. See note 1 at end of Appendix B.)

PULSE COUNTER - 16 BIT: Termination and 16-bit counter for counting input voltage pulses. (Maximum - 64 per system. See note 1 at end of Appendix B.)

PROCESS INTERRUPT ADAPTER: Required for adaption of Process Interrupts - Contact and Process Interrupts - Voltage. This feature provides for 48 interrupt points. (Maximum - eight per system.)

PROCESS INTERRUPT - CONTACT: Termination and latching circuits for sensing and interrupting due to a change in status of up to 16 customer contacts. (System maximum - 24 Process Interrupt - Contact or Voltage - in any combination.)

PROCESS INTERRUPT - VOLTAGE: Termination and latching for sensing and interrupting due to a change in level of up to 16 customer voltage inputs. (System maximum - 24 Process Interrupt - Contact or Voltage - in any combination.)

DIGITAL INPUT DATA CHANNEL ADAPTER: Required for digital input operation on a Data Channel. (Maximum - one per system.)

DIGITAL OUTPUT ADAPTER: Required for control for up to four Pulse Output, Electronic "Contact" Operate, and Register Output in any combination. This feature provides for maximum of 64 points. (Maximum - four per Digital Output Control.)

DIGITAL OUTPUT CONTROL: Required for control of Digital Output Adapters that are housed in same enclosure as DO Control. (System maximum - eight Digital Output or Analog Output Controls in any combination.)

PULSE OUTPUT: Termination and circuits for momentary (3 ms) switching of 16 customer lines carrying up to 45V dc at 450 mA. (Maximum - 128 per system. See note 2 at end of Appendix B.)

ELECTRONIC "CONTACT" OPERATE: Termination and circuits for switching and latching of 16 customer lines carrying up to 45V dc at 450 ma. (Maximum - 128 per system. See note 2 at end of Appendix B.)

REGISTER OUTPUT: Termination and line drivers for high-speed transfer of 16-bit data words to customer registers. (Maximum - 128 per system. See note 2 at end of Appendix B.)

DIGITAL AND ANALOG OUTPUT DATA CHANNEL ADAPTER: Required for digital and analog output operation on a Data Channel. (Maximum - one per system.)

1826 Data Adapter Unit

This unit provides for expansion of Digital Input, Digital Output, Process Interrupt, Pulse Counter Points, and Analog Input. There are two models. Either Model 1 or Model 2 is required for the System/360 Adapter.

Model 1. This unit contains a 2 x 3 SLT gate and is free-standing from the P-C. It is externally cable connected. This unit is required for the Analog Input Expander.

Model 2. This unit is the same as Model 1 but is bolted on and internally cabled to the 1826 Model 1, 1801 or 1802.

Model 3. This unit contains a 2 x 3 SLT gate and is free-standing from the P-C. It is connected by external cables. The unit may contain Selector Channel, Communications Adapter or the 2790 Adapter.

ANALOG INPUT EXPANDER: Required for installation of a separated ADC or an additional ADC. Provides also for attachment of all other analog input features available on the 1801 or 1802. This provides a second 2 x 3 SLT gate in the 1826 DAU and the additional power supplies. (Maximum - one per system.)

SYSTEM/360 ADAPTER: Required for attachment of the 1800 system to a channel of the System/360 model 25, 30, 40, 44, or 50 via a standard interface. Each system may regard the other as an I/O device capable of requesting service on a random basis. (Maximum - one per system.)

1828 Enclosure

This provides an enclosure for mounting up to six of the 1851 Multiplexer Terminal and 1856 Analog Output Terminal. There are two models:

Model 1. This unit is free-standing from the P-C. It is externally cable connected.

Model 2. This unit is the same as the Model 1 but is bolted on and internally cabled to the 1801, 1802, 1826, or another 1828 Model 1 or 2.

1851 Multiplexer Terminal

There are two models of this unit:

Model 1. Provides non-thermocouple termination and multiplexing capacity for a maximum of 64 analog input points.

Model 2. Provides both thermocouple and non-thermocouple termination and multiplexing capacity for a maximum of 62 analog input points.

Either Relay or Solid State multiplexing points can be installed in an 1851 Multiplexer Terminal but they cannot be intermixed within a unit. (Maximum - 19 1851s per ADC.)

MULTIPLEXER/R: Provides for relay multiplexing of low-level differential or high-level (-0.5 to +5.0 volts) analog input signals. (Maximum - 1024 points per ADC.)

MULTIPLEXER/S: Provides for solid-state high-speed multiplexing of high-level single-ended inputs. (Maximum - 256 points per ADC.)

DIFFERENTIAL AMPLIFIER: A time-shared amplifier to raise low-level signals to the ±5 volt range of the ADC and convert from differential to single-ended inputs. (Maximum - 16 per ADC.)

SIGNAL CONDITIONING ELEMENTS: Provide passive signal conditioning of each analog input signal. There are seven types of elements:

Filter Element
Voltage/R Element
Voltage/S Element
Current Element
Current/HL Element
Connector Element
Custom Element

Current elements are installed on the customer side of the 1851 terminals. Other elements are installed on Multiplexer/R or Multiplexer/S cards. Custom Elements provide a base for customer mounting of components. (Required - one per analog input point.)

1856 Analog Output Terminal

There are two models of this unit:

Model 1. Provides power and housing for 8 points of analog output, and control for 16 points of analog output. The model 1 is repeated for each multiple of 16 points required.

Model 2. Provides power and housing for 8 points of analog output. One model 2 can be installed for each model 1 if the additional points are required.

(System maximum - eight 1856 Model 1s and eight Model 2s.)

Digital-Analog Converter

There are four models of this feature which are installed in the 1856:

Mod 1. Provides digital to analog conversion (10-bit) unipolar for one analog output point.

Mod 2. Provides 10-bit unipolar conversion for two independent analog output points.

Mod 3. Provides 13-bit bipolar conversion for one analog output point.

Mod 4. Provides 13-bit bipolar conversion for two independent analog output points.

(Maximum - 128 analog output points per system. See NOTE 2 at end of Appendix B.)

BUFFER REGISTER - SINGLE 13 BIT: Provides buffered input to a DAC Mod 3 for simultaneous control of more than one analog output point. (Maximum - one per DAC Mod 3.)

BUFFER REGISTER - DOUBLE 13 BIT: Provides independent buffered input to both converters of the DAC Mod 4 for simultaneous control of more than one output point. (Maximum - one per DAC Mod 4.)

ANALOG DRIVER AMPLIFIER: Provides a 10-volt output with low impedance for one analog output point to drive a wide variety of loads. (maximum-one per DAC Mod 1 or 3, two per DAC Mod 2 or 4.)

Precision Voltage Reference (PVR)

This feature provides precision reference voltage for use with the DAC. One feature serves 8 points of analog output. The PVR is installed in the 1856 which will accept one PVR feature.

Mod 1. Provides a unipolar voltage reference for DAC's converting 10 bit input.

Mod 2. Provides a bipolar voltage reference for DAC's converting 10 or 13 bit input.

(Maximum - 16 per system.)

Note 1: A maximum of 64 of the following features in combination can be installed:

Digital Input - Contact
Digital Input - Voltage
Digital Input - Voltage (High Speed)
Pulse Counter - 8 Bit (Two count for one of the 64 maximum)
Pulse Counter - 16 Bit

If any one feature is installed to its maximum, none of the others can be installed.

Note 2: The following feature or feature groups cannot singly, or in combination, exceed 128:

Electronic Contact Operate
Pulse Output
Register Output (High Speed)
DAC
Mods 1 and 3 count for 1 of the 128 max.
Mods 2 and 4 count for 2 of the 128 max.

(CA) Communications Adapter (Sel) Selector Channel (S/360) System/360 Adapter

(CA) Communications Adapter (Sel) Selector Channel (S/360) System/360 Adapter

(CA) Communications Adapter (Sel) Selector Channel (S/360) System/360 Adapter

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FE System Maintenance Library

System

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