Bill Meck

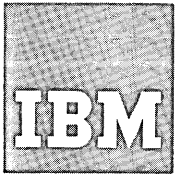# IBM Systems Reference Library

IBM 1800 Functional Characteristics

This manual provides basic programming and operating
information for the IBM 1800 System. The manual in-
cludes typical application areas, Processor-Controller
instruction set, digital and analog input/output, and
System/360 interface. The Appendixes provide hexa-
decimal to decimal conversion, summary tables of the
instruction set and instruction execution times.

PREFACE

This manual provides the basic programming and
operating information for the IBM 1800 System.

Reference Publications

The following Systems Reference Library publications
provide additional information about the 1800 System.

IBM 1800 Data Acquisition and Control System:

1. System Summary (Form A26-5920)
2. Data Processing I/O Units (Form A26-5969)
3. Installation Manual – Physical Planning
    (Form A26-5922)
4. Configurator (Form A26-5919)

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The ever increasing pace of technology, industry, and business continues to demand more and more reliable, up to date information. History is a good teacher, true, but its compression within the past few decades of progress has taught us that today's problems require real-time answers, not a history of past performances. Data of almost every conceivable nature—available from a myriad of sources—must be collected, analyzed, and translated into terms that can be used to optimize today's performance.

IBM's answer to the demand for real-time data acquisition, analysis, and control is the IBM 1800 Data Acquisition and Control System. The 1800 System is designed to handle a wide variety of real-time applications, process control, and high-speed data acquisition. Each system is individually tailored with modular building blocks that are easily integrated to meet specific system requirements. A large family of real-time process input/output (I/O) devices is included, such as analog input, analog output, digital input, digital output; as well as data processing I/O units, such as magnetic tape, disk storage, line printer, graph plotter, card and paper tape input and output. Data is received and transmitted on either a high-speed cycle-steal basis or under program control, depending on the intrinsic data rate of the I/O device. These capabilities not only meet today's requirements, but those of the future as well.

The 1800's Processor-Controller (P-C) can be used for editing, supervisory control, direct control, or data analysis. A control and data path provides for the attachment of the IBM System/360 where more powerful supervision is required. For example, the System/360 may be used to integrate the commercial aspects of an application with the controlling operations exercised by the 1800. This multiprocessor system's capability enables the handling of real-time applications of any size or complexity.

APPLICATIONS

The 1800 is capable of accepting electrical signals, both analog and digital, from such devices as thermocouples, pressure and temperature transducers, flow meters, analytical instruments, and contacts.

It provides electrical on/off and analog control signals for the customer's controlling devices. Typical applications exist in the area of process control and high speed data acquisition.

PROCESS CONTROL

Industrial processing applications are wide and varied, as are the degrees of control that individual processes may require. Some general process control application areas are:

> Primary Metals Production
> Primary Metals Finishing
> Power Generation
> Power Dispatching
> Pipeline Transmission
> Paper Production
> Glass Production
> Cement Production
> Environmental Control
> Pilot Plants
> Chemical Processes
> Petroleum Refining

The IBM 1800 Data Acquisition and Control System provides maximum flexibility in the types of process data that it can accept and the variety of output signals and data format that it can produce. Some of the degrees of control that an 1800 may exercise follow in order of increasing complexity:

Data Gathering. Process data is gathered by the 1800 System, converted into digital information, and printed to provide: (a) operating records for accounting and supervisory purposes; or (b) a record of experimental data in process research.

Data Collection and Analysis. Process data is collected by the P-C for mathematical analysis. Current performance figures are compared with those obtained in the past, and the results are printed for process operator and management evaluation.

Data Evaluation and Operator Guidance. Process data is collected, analyzed, and evaluated with respect to previously stored guidance charts. Control instructions are then typed out for the process and control room operator, and messages and log sheets are provided for management review.

Process Study: The P-C rapidly collects the process data that is necessary for the development of a model of the process. The model is developed by using a combination of empirical techniques and observing past methods of running the process. When a more complete and more precise description of the process is required, a model is constructed by using such mathematical techniques as correlation analysis and regression analysis. The process control program is then tested on the mathematical model prior to its use on the process. Extensive operator guide information is obtained. In addition, the model represents considerable progress toward complete supervisory control.

Process Optimization: An extensive P-C program, based on the model of the process, directs the 1800 System. Process data is continuously collected and analyzed for computation of optimum operating instructions. These instructions are given to the process operator via an on-line printer.

Supervisory Control: The P-C communicates messages and commands to the operator and, if desired, directly to the process equipment and instrumentation. The sensors that measure process conditions are continuously monitored by the P-C. The P-C program analyzes this information and then generates the required output information.

Messages from the P-C to the operator may be displayed by several methods in the operator's working area. These messages guide the operator in adjusting the status of instruments located at the point of control. Data messages based upon visual observation of the process and its instrumentation are sent back to the P-C or the process operator. These messages are evaluated by the P-C to provide additional output, if required, for continued process operator guidance. Communication between the control room operator and the process is maintained through the P-C.

When the P-C supervisory program computes new set point values, it may—at the discretion of the operator—automatically adjust the set points of the controlling instrumentation to the new values.

HIGH SPEED DATA ACQUISITION

A High Speed Data Acquisition (HSDA) System may be thought of as a monitoring and controlling facility that is used to acquire, evaluate, and record data developed during the testing of a system (or assembly, subassembly, or component). The system here

refers to anything from an anesthetized rodent in the research laboratory to a Saturn V booster on its test stand.

Many types of HSDA Systems are used. Some merely stream data directly from instrumentation to magnetic tape with a minimum of "quick look" information and data editing or checking. However, as experimental work on large systems has become more complex and time consuming, a trend has been observed toward HSDA Systems with more sophisticated data reduction and real-time display requirements. HSDA Systems most readily meet these requirements when the system design is based on a digital computer.

Many aerospace applications, for example, now require control signals to modify the test as a result of out-of-limit conditions or evaluation of sample test data. Thus we find a direct parallel with the historical development of process control systems. They began with data gatherings; progressed to operator guide control; and where the applications required it, automatically applied system output commands directly to the process equipment.

The following are typical HSDA application areas for the 1800 System:

Missile Check Out
Wind Tunnels
Static Test Stands
Missile Telemetery
Nuclear Reactor Research
Particle Physics Control and Acquisition
Environmental Chambers
Flight Simulators
Hybrid Systems
Medical Research
Medical Analysis—Clinical

OTHER ACQUISITION AND CONTROL

The 1800 System has been designed to handle widely divergent applications which involve real-time processing abilities. Inputs may include signals from only digital sources or from both digital and analog sources   If desired, the results of analyzing the required data may be displayed in analog or digital form, or used to cause direct functions.

These applications cover a wide range, including the following areas:

General Research
Traffic Control (vehicle, railways, etc.)
Engine Testing

Component Testing
Quality Control
Information Display
Material Dispatching
Marine Operating Systems

SYSTEM DESCRIPTION

Components of the IBM 1800 Data Acquisition and
Control System can be used in three basic configurations:

1. The 1800 System process I/O equipment attached
    to the Processor-Controller, with any necessary
    data-processing I/O units. The minimum system
    will satisfy initial control and analysis
    needs and can be expanded to support medium-
    scale applications.
2. The 1800 System process I/O equipment attached
    directly to an IBM System/360, Model 30, 40,
    44, or 50. This configuration is well suited to
    medium-scale, real-time applications involving
    substantial data processing loads.
3. One or more 1800 Systems (Processor-
    Controllers, each with appropriate process I/O
    equipment) attached via channel adapters to a
    System/360. This configuration is suited to
    large-scale, real-time applications, and can be
    expanded to supply almost any combination of
    data processing capability and real-time input/
    output channel capacity.

PROCESSOR-CONTROLLER (P-C)

● Central Processing Unit provides arithmetic,
   logic, and control functions for the 1800 System.

● Stored program controls input/output and proc-
   essing.

● Standard features include three Index Registers,
   12 levels of Priority Interrupt, three Data
   Channels, three Interval Timers, an Operations
   Monitor, and an Operator's Console.

● Design includes basic circuitry and controls for
   attachment of process input/output equipment.

The Processor-Controller contains a binary stored-
program Central Processing Unit (CPU). Within its
basic design, it has interrupt and cycle-stealing
capabilities which are used in controlling the various

I/O devices to be attached to the using system.
Index Registers and Indirect Addressing are pro-
vided to facilitate address modification and pro-
gramming.

A complete instruction set with powerful options
gives the computer very high performance for tasks
normally encountered in data acquisition and control
applications.

Two Processor-Controllers are available: the
IBM 1801 and the IBM 1802. Each has eight models
based on speed and size of the core storage. The
1801 has no provision for magnetic tape, while the
1802 includes the Tape Control Unit for the IBM
2401 and IBM 2402 Magnetic Tape Units.

The System/360 Adapter is available as a
special feature of the Processor-Controller to link
together the 1800 System and the System/360 Model
30, 40, 44, or 50. With this feature, data can be
transferred from one system to the other on a
channel-to-channel basis.

PROCESS INPUT/OUTPUT FEATURES

● Modular features are available to match the
   1800 System with the process requirements.

● Analog Input converts bipolar voltage or current
   signals to digital values for use by the computer.

● Digital Input accepts binary information repre-
   sented by contact closures or voltage levels.

● Analog Output converts digital values to precise
   voltage levels for operating process devices.

● Digital Output provides binary data to the proc-
   ess in the form of "contact" closures or voltage
   levels.

Analog Input features include analog-to-digital conver-
ters, multiplexers, amplifiers, and signal condition-
ing equipment to handle all types of process analog
and input signals. System conversion rates to 20,000
samples per second are provided, with program select-
able resolution and external synchronization. Analog
input capacities are 1,024 relay multiplexer points and
256 solid-state (high-speed) multiplexer points. A
second analog-to-digital converter can be added to
double system analog input performance and capacity.

The Digital Input features provide up to 384
process interrupt points; up to 1,024 bits of contact
sense, digital input, high-speed parallel register
input; or 128 high-speed pulse counters.

Analog Output features provide up to 128 analog output points for individual or simultaneous operation of a wide range of customer devices.

The Digital Output features provide up to 2,048 bits of pulse output, electronic "contact" operate, and high-speed register output.

DATA PROCESSING I/O UNITS

● Adapters and controls are available for attaching a wide variety of Data Processing I/O Units.

Data Processing I/O Units function with an external document such as a punched card or a reel of magnetic tape. To provide the logical and buffering capabilities necessary for operation on the 1800 System, a control (adapter) feature is available for each I/O Unit.

The following I/O Units can be attached to the 1800 System via the Data Processing I/O attachment features:

    1816 Printer-Keyboard (Modified SELECTRIC®)
    1053 Printer
    1442 Card Read Punch
    1054 Paper Tape Reader
    1055 Paper Tape Punch
    1443 Printer
    1627 Plotter
    2310 Disk Storage
    2401/2402 Magnetic Tape Unit

SYSTEM DATA FLOW

● Data is stored and processed in fixed-length 18-bit words for fast parallel manipulation of data.

● The I/O devices are linked to the Processor-Controller via a standard I/O interface.

● Adapter circuitry at each I/O device performs the necessary conversion, buffering, and control functions.

● Cycle-stealing capability permits high-speed transfer of data.

A standard I/O interface is used between the Processor-Controller (P-C) and all input/output devices. Adapter circuitry to accommodate each type of I/O device is installed in the 1800 System as required. The adapters provide the necessary buffer registers and controls to permit operation on the system.

Configuration 1 shows the data flow between the P-C and the various I/O devices. In a closed-loop system, process conditions are monitored and analyzed continuously, and controlling signals are sent to the devices that control the process. Input data is obtained directly from measuring devices in the process area without the need for off-line conversion equipment. Electrical signals are accepted in analog or digital form from such devices as thermocouples, pressure transducers, digital voltmeters, and contacts. Signal conditioning, multiplexing, and conversion functions are performed by the input circuits. The input data, in 1800 System format, is held in registers until called for entry into core storage.

After the input data has been read and analyzed by the Processor-Controller, the program may select a process control function. Both digital and analog output data can be generated for controlling equipment such as set-point positioners, displays, and telemetry systems. Data processing information can be entered and retrieved in a variety of forms through the DP I/O units and their adapter circuitry.

When a Process I/O device or a DP I/O device is ready to send or receive data, it can notify the Processor-Controller by issuing an interrupt request. The program identifies the source of the interrupt by sensing the status of indicators associated with each I/O device. The program responds to the interrupt by sending the appropriate I/O command to the device. Each I/O command always places a control word on the Out-Bus to specify the input/output device and the function to be performed. Depending on the intrinsic data rate of the I/O device receiving the control word, the transfer of data between core storage and the device can take place under direct program control, or on a Data Channel operation. A Data Channel transfers data on a high-speed cycle-steal basis, using a data table in core storage for flexibility of scanning rates and patterns. The cycle-stealing capability makes it possible to delay the program for one machine cycle and to use this cycle to transfer the data word between P-C storage and the I/O device. Cycle-stealing and interrupt servicing are conducted by the P-C on a priority basis. This makes it possible to simultaneously control combinations of real-time input/output devices.
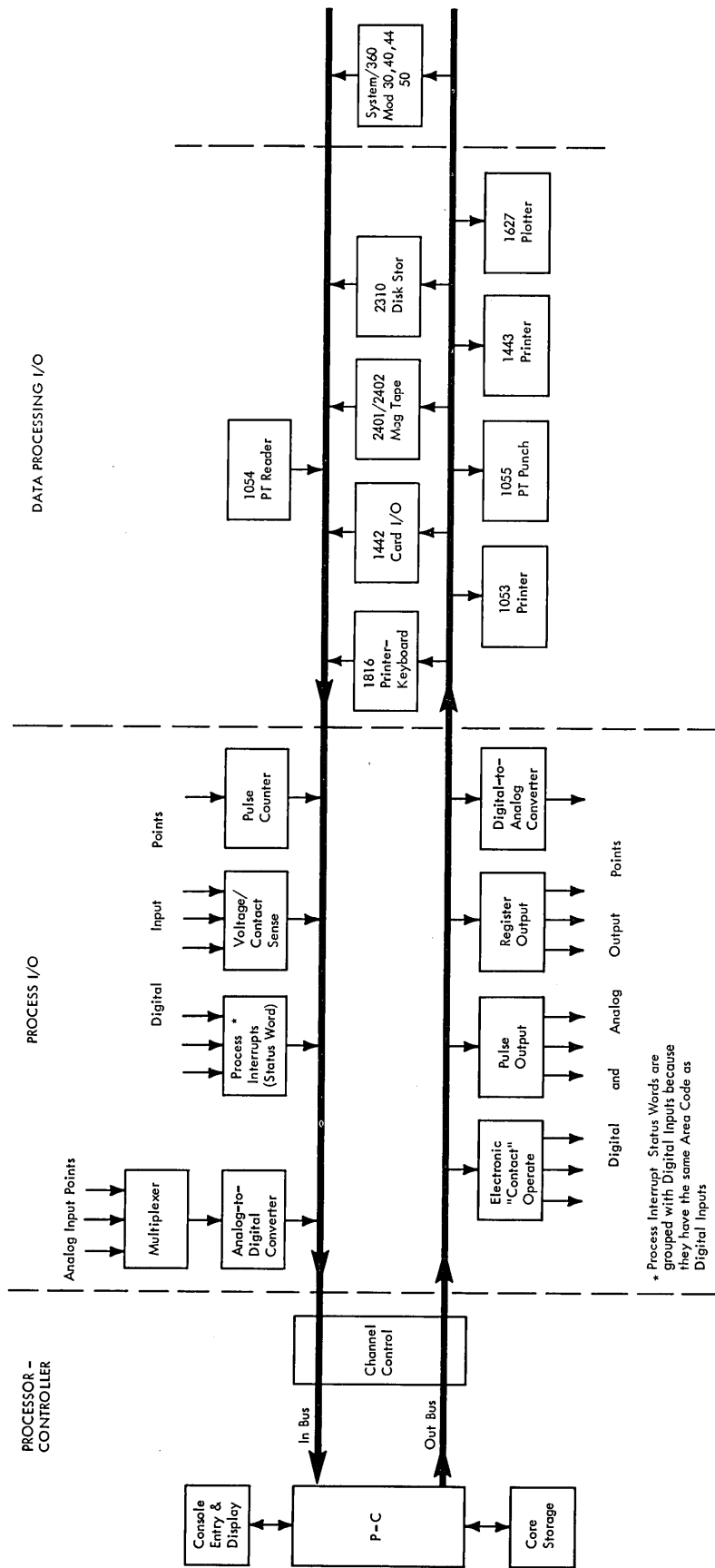
Configuration 1. IBM 1800 Data Acquisition and Control System

Note: The illustrations in this manual have a code number in the lower corner.
This is a publishing control number and is unrelated to the subject matter.

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A brief description of 1800 features and units follows. This description will facilitate an understanding of the P-C instruction set. More detailed descriptions are provided at appropriate sections of the manual. The data processing I/O units (card, paper tape, etc.) are described in the Systems Reference Library publication IBM 1800 Data Acquisition and Control System, Data Processing I/O Units.

PROCESSOR-CONTROLLERS

The Processor-Controllers (1801 and 1802 models), are fixed-word-length, binary computers. Four memory sizes are available—4, 8, 16, or 32K words of 18 bits each—with memory cycle times of 2 or 4 microseconds (μsec). Two of the 18 bits are used for (1) storage protection and (2) parity check. There are 16 data bits in each word. A repertoire of instructions (many of which serve multiple functions) includes arithmetic instructions that manipulate both 16-bit and 32-bit words (16 data bits are handled in parallel). The 2 μsec system can perform high-speed I/O operations during cycle steal operations via Data Channels at rates up to 500,000 words (or 8,000,000 bits) per second in burst mode. Both indirect addressing and index registers (3) are provided for address modification. Other P-C features include a multi-level interrupt system, three high-resolution interval timers, storage protection, an auxiliary storage for on-line diagnostics, operations monitor, and an operator's console.

Data Representation

The standard or single precision data word is 16 bits in length.
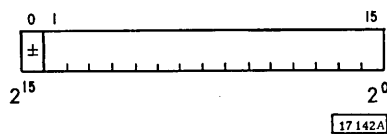
Positive numbers are always in true binary form, whereas negative numbers are in two's complement form. The sign bit (position 0) is always 0 for positive numbers and 1 for negative numbers. The 2's complement of a binary number is defined as its 1's complement increased by one. The 1's complement of a binary number is that number that results by

Decimal	Binary	1's Comp	2's Comp
15	0 1 1 1 1	1 0 0 0 0	1 0 0 0 1
9	0 1 0 0 1	1 0 1 1 0	1 0 1 1 1
3	0 0 0 1 1	1 1 1 0 0	1 1 1 0 1

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Figure 1. Binary 1's and 2's Complement

replacing each 1 in the number with a 0 and each 0 with a 1. The decimal numbers are shown in Figure 1 with their binary equivalents and 1's and 2's complements:

Bit positions 1 through 15 represent decimal values of 2^{14} through 2^0 respectively. Thus the largest single precision positive number that can be represented is $2^{15} - 1$ or 32,767 (a sign bit of 0 and 1's in all other bit positions). The largest negative number is -2^{15} or $-32,768$ (a sign bit of 1 and 0's in all bit positions). The number zero is represented by all bits being zero. There is no negative zero.

A double precision number of 32 bits can be used to give a number range from +2,147,483,647 to $-2,147,483,648$ ($2^{31}-1$ to -2^{31}). Two adjacent words must be used in memory with the left-most word at an even address and the right-most word at the next higher odd address.
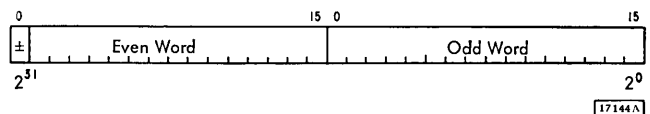
CORE STORAGE

Core storage sizes of 4096; 8192; 16,384; or 32,768 words are available. Storage cycle times — that is, the time required to transfer a word to or from a memory address — of 4 or 2 μsec are available.

Each word consists of 18 bits: 16 are data bits which can be either data or instructions; one bit is used for the Storage Protect feature; one bit is used for odd bit parity. Parity includes the 16 data bits and the Storage Protect bit. The parity bit cannot be affected by the program. Detection of a parity check causes an interrupt to the internal interrupt level. See Interrupt section.

Core storage addresses 0001 and 0002 are reserved for CE Interrupt; addresses 0004, 0005, and 0006 are reserved for the Interval Timers; addresses 0008 through 0034 are reserved for interrupt addresses.

Addressing

Core storage addresses begin at 0000 and end at 4095; 8191; 16,383; or 32,767 depending on storage size. Storage wrap around exists; that is, the next sequential address above the highest numbered address is always 0000.

Although core storage addresses have been expressed in decimal (base 10) form up to now, the 1800 P-C uses a binary (base 2) form. Internal addressing and console displays are in 16-bit binary form. For example.

$$4095_{10} \quad \text{equals} \quad 0000111111111111_2$$

$$8191_{10} \quad \text{equals} \quad 0001111111111111_2$$

$$16,383_{10} \quad \text{equals} \quad 0011111111111111_2$$

$$32,767_{10} \quad \text{equals} \quad 0111111111111111_2$$

Greater ease of operation is realized when hexadecimal (base 16) representation is used. Programming Systems for the 1800 make use of this notation. A description of binary and hexadecimal number systems is provided in the Number Systems section.

NOTE: When an instruction is excuted, the instruction register (I) contains the address of the next sequential instruction.

Arithmetic

The arithmetic operations of the P-C include add, subtract, multiply, and divide. Negative data is always stored and operated upon in 2's complement form. Addition and subtraction can be done in single or double precision. Multiplication operates on two single precision words to provide a double length product. Division allows the dividend to be double length and uses a single precision divisor to provide a single precision quotient and a single precision remainder.

Overflow and Carry Indicators

The two indicators associated with the Accumulator are Overflow and Carry. The Overflow indicator can be turned on by add, subtract, or divide, and indicates a result larger than can be represented in the Accumulator. The Overflow indicator can also be turned ON by a Load Status instruction. Once Overflow is on, it will not be changed except by testing the indicator, or by a Load Status or Store Status instruction. The Carry indicator provides the information that a carry (or borrow) from the high order position of the Accumulator has occurred.

The Carry indicator is dynamic and changes with each add or subtract operation. The Carry indicator is also affected by Shift Left, Load Status, Store Status, and Compare instructions.

Indirect Addressing

Indirect addressing is a standard feature of the 1800. One level of indirect addressing is provided. Indirect addressing cannot be used with one word instructions. The instructions that can be modified by indirect addressing are indicated in the Instruction Set section. The recognition in the instruction of an Indirect Address control bit (position 8, two-word instruction only) causes the address portion to be treated as an indirect address. The address after indexing (if specified) gives the location of the effective address. An additional memory cycle is required for indirect addressing.

Index Registers

Three index registers (XR) are standard features. The XRs are addressed by the TAG (positions 6 and 7 in the instruction), as follows:

Bits 6 & 7	XR
01	1
10	2
11	3

Operations on the XR, such as load, store, modify and skip, are accomplished through instructions in the basic instruction set. The contents of an Index Register or the Instruction Register are usually used to perform address arithmetic.

Data Channels

Data Channels give the P-C the ability to delay the execution of a program while an I/O device communicates with core storage. For example, if an input unit requires a memory cycle to store data that it has collected, the data channel with its "cycle stealing" capability makes it possible to delay the program during execution of an instruction and store the data word without changing the logical condition of the P-C. After the data is stored, the P-C continues executing the program which was delayed by the "cycle-stealing." This capability should not be confused with interrupt which changes the contents of the Instruction Register.

Cycle stealing by the Data Channels can occur at the end of any core storage cycle. Maximum delay before cycle stealing can occur is 2.25 μs for the 2 μs system and 4.5 μs for the 4 μs system.

A WAIT instruction, which halts the P-C, will not stop the operations of Data Channels.

Interrupt

The interrupt facility provides an automatic branch in the normal program sequence based upon external conditions (those in the process) or internal conditions (those within 1800). Examples of such conditions are:

- The detection of an external process condition that requires immediate attention.

- A P-C Interval Timer has concluded the recording of a preset time interval.

- A magnetic tape drive has completed a data transfer previously requested and is ready for another request.

- An operator has initiated an interrupt from the P-C console.

These devices and conditions are assigned priority levels by the user. An interrupt request is not honored while the level of the request itself or any higher level is being serviced or if the level requested is masked. A request is honored if the level is not masked and no interrupt is being serviced or if any lower level than that of the request is being serviced. A Wait instruction does not prevent interrupts from being serviced.

INSTRUCTION FORMATS

Two basic instruction word formats are used (Figures 2 and 3). The bits within the instruction words are used in the following manner:

OP	These five bits define which operation is to be performed by the P-C.
F	This format bit controls the instruction format. A "zero" indicates a single word instruction and a "one" indicates a two word instruction.
T	These two Index Tag bits specify the base register (XR, I or ADDRESS) used in address modification or the location (XR or DISP) of the shift count.
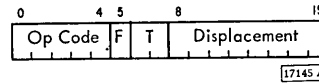
Figure 2. One-Word Instruction Format

DISP	These eight bits are called the displacement and, with one word instructions only, are usually added to the Instruction Register or the index register specified by T. The modified address is defined as the effective address (EA). If T is 00, the displacement is added to the Instruction Register (then EA= I + DISP). The displacement is in 2's complement form if negative, with the sign in bit 8. The bit in position 8 is automatically extended to the higher ordered bits (0-7) when the displacement is used in EA generation, or as an add to memory operand.
IA	The Indirect Addressing bit is used in the two word instruction format. If "zero", addressing will be direct. If a "one", addressing will be indirect. See the Load Index and Modify Index and Skip Instructions for exceptions.
BO	This bit is used to specify that the Branch or Skip on Condition (BSC) instruction is to be interpreted as a "Branch Out" (BOSC) when used in an interrupt routine.
COND	Specifies the condition of indicators that are interrogated on a BSC or BSI instruction.
ADDRESS	These 16 bits usually specify a core storage address in a two word instruction. The address can be modified by the contents of an index register or used as an indirect address if the IA bit is on.
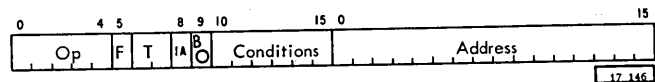
Figure 3. Two-Word Instruction Format

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Table 1. Determining Effective Addresses

	F = 0 (Direct Addressing)	F = 1, IA = 0 (Direct Addressing)	F = 1, IA = 1 (Indirect Addressing)
T = 00	EA = I+Disp ① ②	EA = Address	EA = C (Address) ③
T = 01	EA = XR1+Disp	EA = Address+XR1	EA = C (Address+XR1)
T = 10	EA = XR2+Disp	EA = Address+XR2	EA = C (Address +XR2)
T = 11	EA = XR3+Disp	EA = Address +XR3	EA = C (Address+XR3)

① Contents Of Instruction Register Or Index Register.

② May Be True Positive Quantity Or Negative
2's Complement Quantity.

③ C Specifies "Contents" At Location Specified By Address or Address +XR1, 2, or 3.

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Effective Address Generation

The effective address (EA) is developed as shown in Table 1 for most instructions. (Exceptions are noted in the Instructions section.)
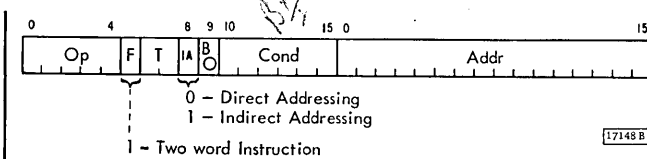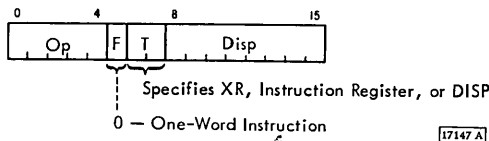
P-C REGISTERS

The following registers are used in the manipulation of data within the P-C and may be displayed on the P-C console.

Storage Address Register (SAR)

All P-C program references to storage are under direct control of this 16-bit register. Data Channel (DC) references to storage use the Channel Address Register (CAR) of the active DC. See Data Channel section.

Instruction Register (I)

This 16-bit counter register holds the address of the next sequential instruction. It is automatically incremented for sequential operation of instructions.

Storage Buffer Register (B)

This 16-bit register is used for buffering all word transfers with core storage.

Arithmetic Factor Register (D)

This 16-bit register is used to hold one operand for arithmetic and logical operations. The Accumulator provides the other factor.

Accumulator (A)

This 16-bit register contains the results of any arithmetic operation. It can be loaded from or stored into core storage, shifted right or left, and otherwise manipulated by specific arithmetic and logical instructions.

Accumulator Extension (Q)

This register is a 16-bit low order extension of the Accumulator. It is used during multiply, divide, shifting, and double precision arithmetic.

Shift Control Counter (SC)

This six-bit counter is used primarily to control shift operations.

OP Register (OP)

This five-bit register is used to hold the operation code portion of an instruction.

NOTE: The above registers are also used uniquely in specific operations described later.

P-C DATA FLOW

As shown in the simplified P-C Data Flow block diagram (Figure 4), all instructions and data entering and leaving core storage do so via the B-register. Input devices send data and instructions to the B-register via the In-Bus. Output devices receive data from the B-register via the Out-Bus. As each stored program instruction is selected, its various parts (op code, format bit, etc.) are directed to the Control registers via the B-register and the Out-Bus. The Control registers decode and interpret each instruction before the instruction is executed.

Except for Data Channel operations (see I/O Control section), all instructions and data must first be addressed by the Storage Address Register (SAR)

before leaving core storage. SAR obtains the core storage address from the I-register or the A-register. The contents of the I-register are developed by one of the following means, depending on the P-C operation:

1. The I-register is incremented for each instruction during sequential operation of the stored program instructions.
2. The effective address of each instruction is developed in the accumulator (A-register) and then transferred to SAR. The contents of the accumulator are saved in an auxiliary (U) register during effective address computation. If the instruction was a branch, the contents of SAR is transferred to the I-register.

Data Transfer, 18 Bits

Each word in core storage comprises 18 bits: 16 data bits, a parity bit (P), and a storage protect bit (S). During P-C operation, the P bit is automatically added or removed to maintain odd parity. The S bit is added or removed by the Store Status instruction, depending on whether a "read only" condition is desired. The 16 data bits enter or leave core storage via the B-register. The P and S bits do so via
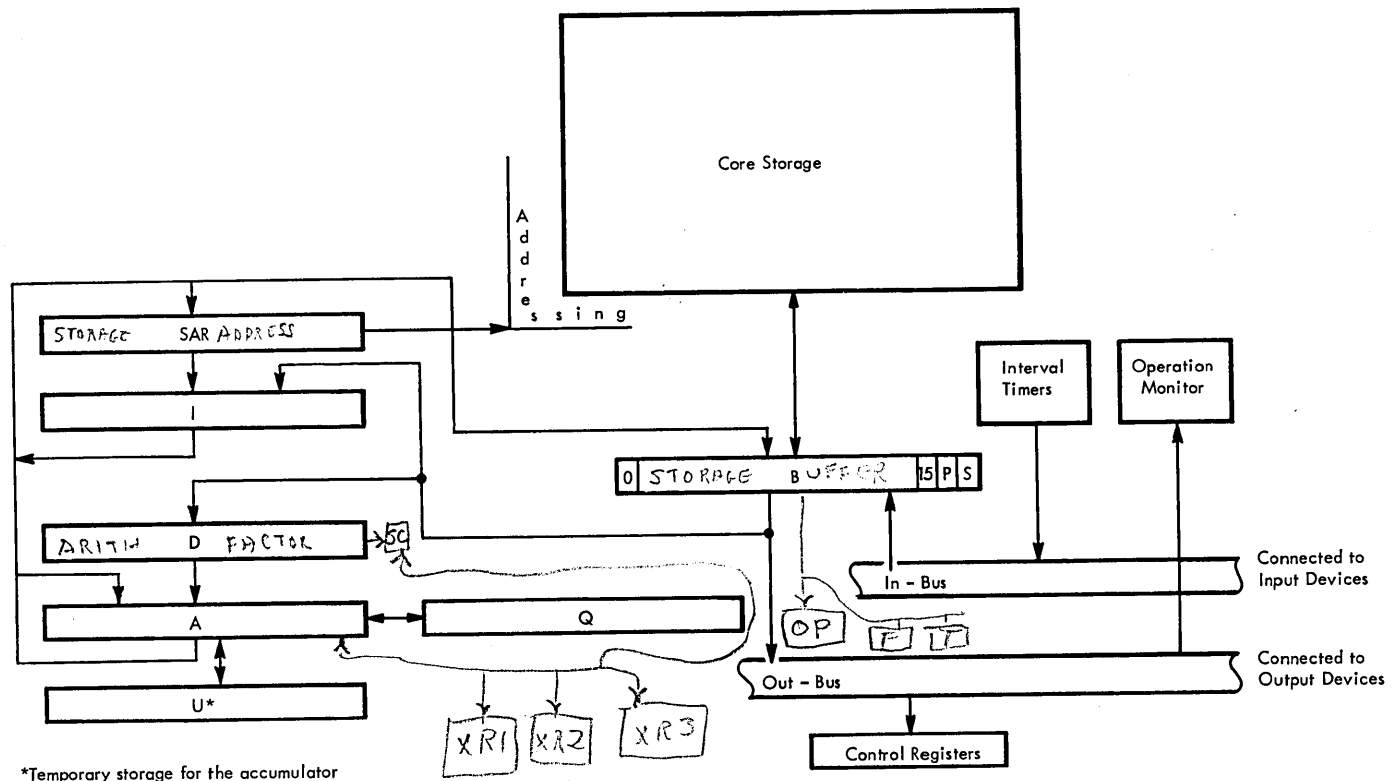
Figure 4. 1800 P-C Data Flow

individual latches. The latches and the B-register together enable the transfer of 18 bits to and from core storage. The In-Bus and the Out-Bus contain 16 data lines and 2 parity lines. Thus, 18 bits can be transferred between the P-C and the magnetic tape units. (See "Data Formats" in the magnetic tape units section of the 1800 I/O manual.)

DATA FLOW EXAMPLES

The following three examples illustrate the data flow for the Load Accumulator (LD) instruction including an example for each type of addressing (one-word format; two-word format, Direct and Indirect addressing). Circled numbers in each illustration correspond to the numbered items included for that illustration.

One-Word Instruction
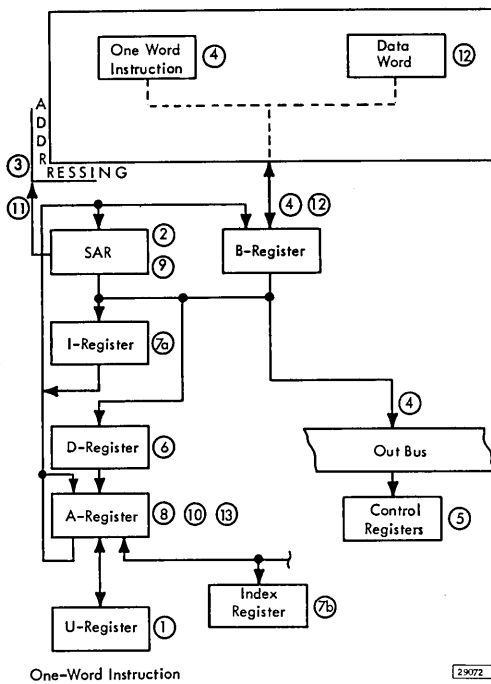
One-Word Instruction

Instruction Cycle

1. A-register transfers to U-register.
2. I-register transfers to SAR (I-register is then incremented).

3. SAR addresses the core-storage location containing the instruction.
4. Core-storage location transfers to the B-register and out-bus.
5. Control registers store various parts of the instruction (op-code, format, and tag).
6. Displacement is stored in the D-register.
7. a. If tag = 00, I register transfers to A-register.
   b. If tag ≠ 00, the specified XR transfers to A-register.
8. Displacement (D-register) is added to A-register.

Execute Cycle

9. A-register transfers to SAR (effective address).
10. U-register transfers to A-register.
11. SAR addresses data word.
12. Data word transfers to B-register.
13. B-register loads into A-register (through D-register).
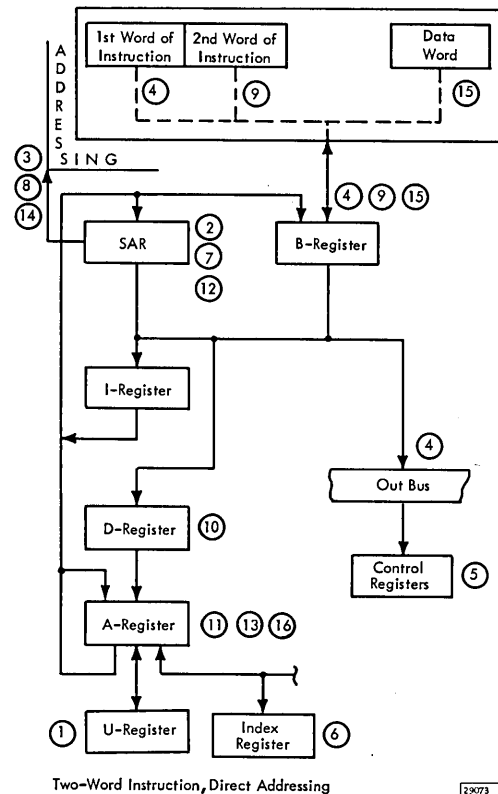
Two-Word Instruction, Direct Addressing

11

Two-Word Instruction, Direct Addressing

Instruction Cycle 1

1. A-register transfers to U-register.
2. I-register transfers to SAR (I-register is then incremented).
3. SAR addresses the core-storage location containing the instruction (1st word).
4. Core-storage location transfers to B-register and out-bus.
5. Control registers store various parts of the instruction (op code, format, and tag).
6. If tag ≠ 00, the specified XR transfers to A-register.

Instruction Cycle 2

7. I-register transfers to SAR (I-register is then incremented).
8. SAR addresses second word of instruction.
9. Second word of instruction (address) is read into B-register.
10. Address (from B-register) is stored in D-register.
11. a. If tag = 00, D-register transfers to A-register.
    b. If tag ≠ 00, D-register is added to A-register (A-register contains contents of XR).

Execute Cycle

12. A-register transfers to SAR (effective address).
13. U-register transfers to A-register.
14. SAR addresses core-storage at effective address (data word).
15. Data word transfers to B-register.
16. B-register loads into A-register (through D-register).
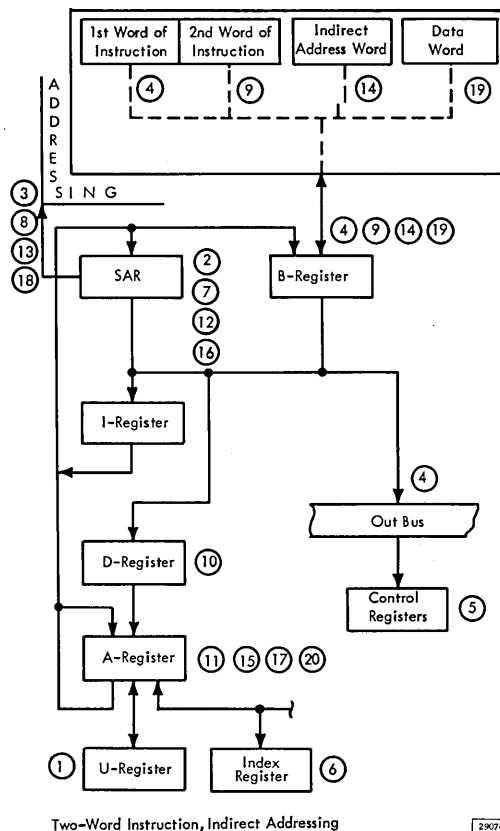
Two-Word Instruction, Indirect Addressing

Two-Word Instruction, Indirect Addressing

Instruction Cycle 1

1. A-register transfers to U-register.
2. I-register transfers to SAR (I-register is then incremented).
3. SAR addresses core-storage location containing the instruction (1st word).
4. Core-storage location transfers to B-register and out-bus.
5. Control registers store the various parts of the instruction (op-code, format, and tag).
6. If tag ≠ 00, the specified XR transfers to A-register.

Instruction Cycle 2

7. I-register transfers to SAR (I-register is then incremented).
8. SAR addresses second word of the instruction.
9. Second word of the instruction (address) is read into B-register.
10. Address (from B-register) is stored in D-register.
11. a. If tag = 00, D-register transfers to A-register.
    b. If tag $\neq$ 00, D-register is added to A-register. (A-register contains contents of XR.)

Indirect Addressing Cycle

12. A-register transfers to SAR.
13. SAR addresses core-storage location at address (or address +XR).
14. Core-storage location transfers to B-register.
15. B-register transfers to A-register (through D-register).

Execute Cycle

16. A-register transfers to SAR.
17. U-register transfers to A-register.
18. SAR addresses core storage at effective address (data word).
19. Data word transfers to B-register.
20. B-register loads into A-register (through D-register).

NUMBER SYSTEMS

This section is provided for those unfamiliar with binary and hexadecimal number systems. By way of review, it is well to remember that in any number system no single integer can exceed the value of the number system base minus one. For example, nine is the largest integer that can exist in any decimal (base 10) number; one is the largest integer that can exist in any binary (base 2) number; and the integer representing 15 (F) is the largest value integer that can exist in any hexadecimal (base 16) number.

It is also well to remember that any number can be expressed in powers of its base number. For example, 1375_{10} can be expanded or expressed as

$$1 \times 10^3 + 3 \times 10^2 + 7 \times 10^1 + 5 \times 10^0$$

or

$$1000 + 300 + 70 + 5$$

(Any number to the zero power equals one.)

Binary

Binary data consists of two digits: zero and one. Thus, the decimal digits 0 through 9 are expressed in binary form:

DECIMAL	BINARY	DECIMAL	BINARY
0	0000	5	0101
1	0001	6	0110
2	0010	7	0111
3	0011	8	1000
4	0100	9	1001

Note that a one in the rightmost position of the binary number is equivalent to a decimal one; a one in the second position is equivalent to decimal 2; a one in the third position, to 4; a one in the fourth position, 8; if there were a fifth position, a one in that position would be equivalent to 16; a one in the sixth, 32, and so on. The decimal equivalent of each position is twice that of the position to its right. See Appendix F for Powers of Two Table.

Hexadecimal

Hexadecimal data is expressed to the base 16 and is related to decimal numbers:

Decimal   0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Hexadecimal   0 1 2 3 4 5 6 7 8 9 A B C D E F

Thus, hexadecimal numbers proceed from 0 through F (0 through 15 decimal), 10 through 1F (16 through 31 decimal), 20 through 2F (32 through 47 decimal), etc.

Binary to Hexadecimal Conversion

Binary numbers can be separated into four-position groups for conversion to hexadecimal. For example, the binary number 010101011111 can be separated as follows:

0101	0101	1111
5	5	F

Thus,

$$010101011111_2 = 55F_{16}$$

Hexadecimal to binary conversion is, of course, simply the reverse of binary to hexadecimal. For example, the hexadecimal number 1FFF equals 0001111111111111_2 ($F_{16} = 15_{10} = 1111_2$):

1	F	F	F
0001	1111	1111	1111

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000-	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
001-	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
002-	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
003-	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
004-	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
005-	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
006-	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
007-	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
008-	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
009-	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
00A-	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
00B-	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
00C-	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
00D-	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
00E-	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
00F-	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255
010-	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
011-	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
012-	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
013-	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
014-	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0332	0333	0334	0335
015-	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
016-	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
017-	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
018-	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
019-	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
01A-	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
01B-	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
01C-	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
01D-	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
01E-	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
01F-	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511

17150 A

Figure 5. Hexadecimal - Decimal Conversion

Hexadecimal to Decimal Conversion

Hexadecimal numbers can be converted to decimal numbers by expanding each position in the manner previously shown. For example,

$$55F_{16} = 5 \times 16^2 + 5 \times 16^1 + 15 \times 16^0$$

$$= 5 \times 256 + 5 \times 16 + 15 \times 1$$

$$= 1280 + 80 + 15$$

$$= 1375_{10}$$

Appendix A is a table for the conversion of hexadecimal to decimal and vice versa. It is partly reproduced here (Figure 5) for explanatory purposes. Note that the decimal number 0489 is boxed in the table and that the two high-order significant hexadecimal numbers found to the extreme left are 1E. The low-order-hexadecimal number (9) is found above ($0489_{10} = 1E9_{16}$). Note also that the binary repretation is shown above the table as it would appear in a console register (0000000111101001).

Thus, from the table in Figure 5, it can be seen that the hexadecimal numbers 1F0 and 1FF equal the decimal numbers 496 and 511. Or, starting from inside the table again, the decimal numbers 50 and 63 equal the hexadecimal numbers 32 and 3F.

14

The 1800 instruction set is shown in Table 2. An invalid code (0000) enables the programmer to detect an inadvertent branch to a blank area of core storage. Each instruction falls into one of five classes. Note that the instructions which may be used with indirect addressing are indicated in the Indirect Addressing column. Some instructions perform multiple uses, as specified by their control bits. A more complete breakdown of instructions, including hexadecimal representations, is found in sections for each instruction and in Appendix B. Execution times are provided in Appendix C.

Table 2. Instruction Set

Class	Instruction	Indirect Addressing	Mnemonic
Load and Store	Load Accumulator	Yes	LD
	Double Load	Yes	LDD
	Store Accumulator	Yes	STO
	Double Store	Yes	STD
	Load Index	**	LDX
	Store Index	Yes	STX
	Load Status	No	LDS
	Store Status	Yes	STS
Arithmetic	Add	Yes	A
	Double Add	Yes	AD
	Subtract	Yes	S
	Double Subtract	Yes	SD
	Multiply	Yes	M
	Divide	Yes	D
	And	Yes	AND
	Or	Yes	OR
	Exclusive Or	Yes	EOR
Shift	Shift Left Instructions		
	Shift Left Logical (A) *	No	SLA
	Shift Left Logical (AQ)*	No	SLT
	Shift Left and Count (AQ)*	No	SLC
	Shift Left and Count (A) *	No	SLCA
	Shift Right Instructions		
	Shift Right Logical (A)*	No	SRA
	Shift Right Arithmetically (AQ)*	No	SRT
	Rotate Right (AQ)*	No	RTE
Branch	Branch and Store I	Yes	BSI
	Branch or Skip on Condition	Yes	BSC(BOSC)
	Modify Index and Skip	**	MDX
	Wait	No	WAIT
	Compare	Yes	CMP
	Double Compare	Yes	DCM
I/O	Execute I/O	Yes	XIO

* Letters in parentheses indicate registers involved in shift operations.
** See the section for the individual instruction (MDX and LDX)

17151 D

Hexadecimal Representation
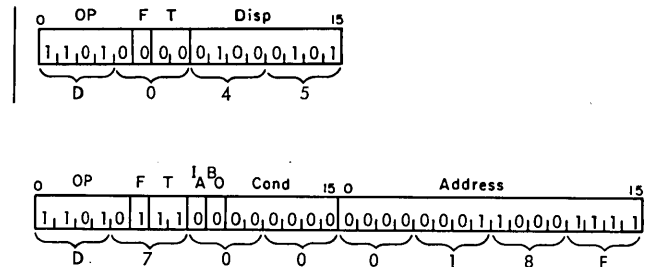
17152 B

The hexadecimal version(s) of each instruction is provided with its description. The hexadecimal number is derived by dividing each word into groups of four bits each and assigning a hexadecimal value corresponding to the decimal (BCD) value of each group. See Numbering Systems section for hexadecimal values and their corresponding decimal (BCD) values. The above illustration shows a hexadecimal value for each group of four binary bits. Conversion from hexadecimal to decimal can be obtained from Appendix A. For example, the decimal value of the Displacement (45) in the one-word instruction is 69.

Instruction Format and Operation Symbology

The following descriptions of 1800 P-C instructions include the instruction format(s) that can be used with each instruction, the effect of the instruction on the carry and overflow indicators, and the hexadecimal representations of each instruction. Symbols are used to describe the objective of each hexadecimal representation of instructions. The symbols and their meanings are:

Symbol	Meaning
A	Accumulator
Q	Accumulator Extension
ADDRESS or Addr	Contents of the Address portion of a two-word instruction.
CSL	Core Storage Location
DISP	Contents of the Displacement portion of a one-word instruction.
EA	Effective Address (see Table 1)
EA +1	Next higher address from the Effective Address

I	Contents of the Instruction Register	X	Hexadecimal value can be 0-F.
V	Value	*	Used for hexadecimal values
XR1	Contents of Index Register 1		that have limits. The limits are
XR2	Contents of Index Register 2		given below each group of hexa-
XR3	Contents of Index Register 3		decimal instructions.

LOAD AND STORE INSTRUCTIONS

LOAD ACCUMULATOR (LD)

```
 0   OP    F  T    Disp      15
|1,1,0,0,0|0,  |          |
    C      0-3   X      X
```
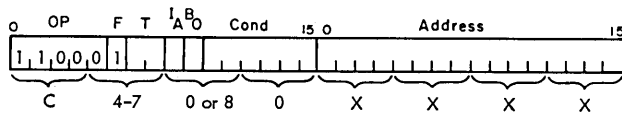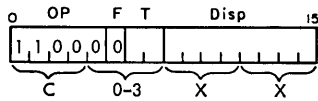
```
 0   OP   F T IA B O  Cond   15 0      Address        15
|1,1,0,0,0|1, | | |      |  0|                        |
    C      4-7  0 or 8  0    X    X    X    X
```
[17153 A]

Description: The contents of the core storage location specified by the effective address (EA) of the instruction replace the contents of the Accumulator (A). The contents of the core storage location are unchanged.

Indicators: The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representation

One-Word Instruction

C0XX	Contents of CSL at EA (I+DISP) are loaded into A
C1XX	Contents of CSL at EA (XR1+DISP) are loaded into A
C2XX	Contents of CSL at EA (XR2+DISP) are loaded into A
C3XX	Contents of CSL at EA (XR3+DISP) are loaded into A

Two-Word Instruction, Direct Addressing

C400XXXX	Contents of CSL at EA (Addr) are loaded into A
C500XXXX	Contents of CSL at EA (Addr +XR1) are loaded into A
C600XXXX	Contents of CSL at EA (Addr +XR2) are loaded into A
C700XXXX	Contents of CSL at EA (Addr +XR3) are loaded into A

Two-Word Instruction, Indirect Addressing

C480XXXX	Contents of CSL at EA (V in CSL at Addr) are loaded into A

C580XXXX	Contents of CSL at EA(V in CSL at "Addr +XR1") are loaded into A
C680XXXX	Contents of CSL at EA (V in CSL at "Addr +XR2") are loaded into A
C780XXXX	Contents at EA (V in CSL at at "Addr +XR3") are loaded into A

DOUBLE LOAD (LDD)

```
 0   OP    F  T    Disp      15
|1,1,0,0,1|0,  |          |
    C      8-B   X      X
```
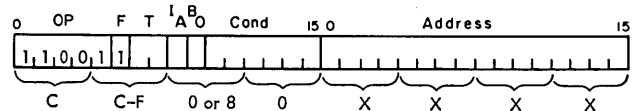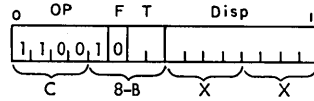
```
 0   OP   F T IA B O  Cond   15 0      Address        15
|1,1,0,0,1|1, | | |      |  0|                        |
    C      C-F  0 or 8  0    X    X    X    X
```
[17154 A]

Description: The contents of the core storage location specified by the instruction (EA) and the next higher core storage location (EA+1) are loaded into the Accumulator (A) and its extension (Q), respectively. This provides double precision load for use with the double precision arithmetic. The EA of the instruction must be an even address for correct operation. If the EA is odd, the contents of that location are entered into both the Accumulator and its extension. The contents of core storage remain unchanged.

Indicators: The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representation

One-Word Instruction

C8XX	Contents of CSL at EA (I + DISP) and EA+1 are loaded into A and Q
C9XX	Contents of CSL at EA (XR1 + DISP) and EA+1 are loaded into A and Q
CAXX	Contents of CSL at EA (XR2 + DISP) and EA+1 are loaded into A and Q
CBXX	Contents of CSL at EA (XR3 + DISP) and EA+1 are loaded into A and Q

Two-Word Instruction, Direct Addressing

CC00XXXX	Contents of CSL at EA (Addr) and EA+1 are loaded into A and Q
CD00XXXX	Contents of CSL at EA (Addr +XR1) and EA+1 are loaded into A and Q

CE00XXXX   Contents of CSL at EA (Addr +XR2) and EA+1 are loaded into A and Q

CF00XXXX   Contents of CSL at EA (Addr +XR3) and EA+1 are loaded into A and Q

Two-Word Instruction, Indirect Addressing

CC80XXXX   CSL at EA (V in CSL at Addr) and EA+1 are loaded into A and Q

CD80XXXX   CSL at EA (V in CSL at "Addr +XR1") and EA+1 are loaded into A and Q

CE80XXXX   CSL at EA (V in CSL at "Addr +XR2") and EA+1 are loaded into A and Q

CF80XXXX   CSL at EA (V in CSL at "Addr +XR3") and EA+1 are loaded into A and Q

STORE ACCUMULATOR (STO)

Description: The contents of the Accumulator replace the contents of the core storage location specified by the effective address. The contents of the Accumulator are unchanged.

Indicators: The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representations

One-Word Instruction

D0XX   Contents of A are stored in CSL at EA (I+DISP)

D1XX   Contents of A are stored in CSL at EA (XR1+DISP)

D2XX   Contents of A are stored in CSL at EA (XR2+DISP)

D3XX   Contents of A are stored in CSL at EA (XR3+DISP)

Two-Word Instruction, Direct Addressing

D400XXXX   Contents of A are stored in CSL at EA (Addr)

D500XXXX   Contents of A are stored in CSL at EA (Addr +XR1)

D600XXXX   Contents of A are stored in CSL at EA (Addr +XR2)

D700XXXX   Contents of A are stored in CSL at EA (Addr +XR3)

Two-Word Instruction, Indirect Addressing

D480XXXX   Contents of A are stored in CSL at EA (V in CSL at Addr)

D580XXXX   Contents of A are stored in CSL at EA (V in CSL at "Addr +XR1")

D680XXXX   Contents of A are stored in CSL at EA (V in CSL at "Addr +XR2")

D780XXXX   Contents of A are stored in CSL at EA (V in CSL at "Addr +XR3")

DOUBLE STORE (STD)

Description: The contents of the Accumulator (A) and its extension (Q) are stored at the core storage locations specified by the effective address (EA) and the EA+1. This provides double precision store for use with the double precision arithmetic. The EA of the instruction must be an even address for correct operation. If the EA is odd, the contents of the Accumulator are stored at the EA and the contents of the Accumulator Extension (Q) will not appear in core storage. The contents of A and Q remain unchanged.

Indicators: The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representation

One-Word Instruction

D8XX	Contents of A and Q are stored in CSL at EA (I+DISP) and EA+1
D9XX	Contents of A and Q are stored in CSL at EA (XR1 +DISP) and EA+1
DAXX	Contents of A and Q are stored in CSL at EA (XR2 +DISP) and EA+1
DBXX	Contents of A and Q are stored in CSL at EA (XR3 +DISP) and EA+1

Two-Word Instruction, Direct Addressing

DC00XXXX	Contents of A and Q are stored in CSL at EA (Addr) and EA+1
DD00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR1) and EA +1
DE00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR2) and EA+1
DF00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR3) and EA+1

Two-Word Instruction, Indirect Addressing

DC80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at Addr) and EA+1
DD80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR1") and EA +1
DE80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR2") and EA +1
DF80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR3") and EA+1

LOAD INDEX (LDX)
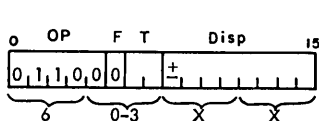
T = 00	Load I
T = 01	Load XR1
T = 10	Load XR2
T = 11	Load XR3
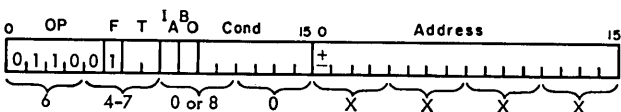
IA = 0 - Load Immediate
IA = 1 - Load Direct

17157 A

Description: An Index Register (XR) or the Instruction Register (I) is loaded by the DISPLACEMENT, the ADDRESS, or the contents of the location specified by the ADDRESS. The T bits indicate which Register is loaded and the F and IA (2-word instruction only) bits determine the source of data.

If the F bit is 0, the register specified by T is loaded with the DISPLACEMENT. The eight high-order positions of the specified register are filled with the value of the sign bit (bit position 8 of instruction) to complete the 16-bit word.

If, however, the F bit is 1, the loading of the register is dependent on the IA bit of the instruction. If the IA bit is 1, the register is loaded with the contents of the word specified by the ADDRESS; if 0, the register is loaded with the ADDRESS portion of the instruction.
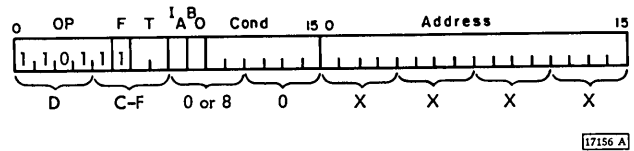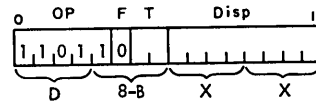
Indicators: The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representation

One-Word Instructions

60XX	Load DISP into the Instruction Register
61XX	Load DISP into Index Register 1
62XX	Load DISP into Index Register 2
63XX	Load DISP into Index Register 3

Two-Word Instruction, Direct Addressing

6400XXXX	Load Addr into the Instruction Register
6500XXXX	Load Addr into Index Register 1
6600XXXX	Load Addr into Index Register 2
6700XXXX	Load Addr into Index Register 3

Two-Word Instruction, Indirect Addressing

6480XXXX	Load contents of CSL at Addr into Instruction Register
6580XXXX	Load contents of CSL at Addr into Index Register 1
6680XXXX	Load contents of CSL at Addr into Index Register 2
6780XXXX	Load contents of CSL at Addr into Index Register 3

STX
STS
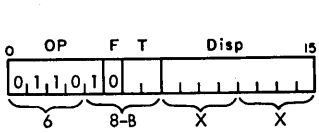
T = 00	Store I
T = 01	Store XR1
T = 10	Store XR2
T = 11	Store XR3

```
 0   OP    F  T      Disp      15
  |0,1,1,0,1|0| |  ,  ,  ,  ,  |
      6   8-B     X        X
```

```
 0   OP    F  T  I A B O  Cond  15 0        Address             15
  |0,1,1,0,1|1| | | |  ,  ,  , |  |  ,  ,  ,  ,  ,  ,  ,  ,  ,  |
      6   C-F  0 or 8   0      X    X    X    X
```
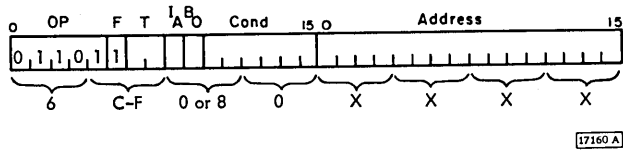
17160 A

Description: An Index Register, or the Instruction
Register, is stored in core storage at the Effective
Address (EA). The T bits specify which register is
stored and bits 5 (F bit) and 8 (IA) govern the genera-
tion of the Effective Address.

Indicators: The Carry and Overflow indicators are
not affected.

Hexadecimal Representation

One-Word Instruction

68XX	Store I in CSL at EA (I+DISP)
69XX	Store XR1 in CSL at EA (I+DISP)
6AXX	Store XR2 in CSL at EA (I+DISP)
6BXX	Store XR3 in CSL at EA (I+DISP)

Two-Word Instruction, Direct Addressing

6C00XXXX	Store I in CSL at EA (Addr)
6D00XXXX	Store XR1 in CSL at EA (Addr)
6E00XXXX	Store XR2 in CSL at EA (Addr)
6F00XXXX	Store XR3 in CSL at EA (Addr)

Two-Word Instruction, Indirect Addressing

6C80XXXX	Store I in CSL at EA (value in CSL at Addr)
6D80XXXX	Store XR1 in CSL at EA (value in CSL at Addr)
6E80XXXX	Store XR2 in CSL at EA (value in CSL at Addr)
6F80XXXX	Store XR3 in CSL at EA (value in CSL at Addr)

Description: Depending on bit 9 (BO), the Store Sta-
tus instruction is used in either of two operations:

1. Store the status of the Carry and Overflow
    indicators.

```
 0   OP    F  T      Disp      15
  |0,0,1,0,1|0| |  ,  ,  ,  ,  |
      2   8-B     X        X
```

```
 0   OP    F  T  I A B O  Cond  15 0        Address             15
  |0,0,1,0,1|1| , | |0| ,  , | |  ,  ,  ,  ,  ,  ,  ,  ,  ,  |
      2   C-F  0 or 8   0      X    X    X    X
```
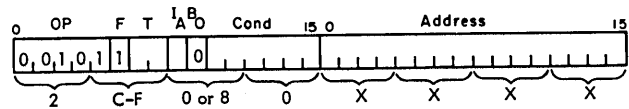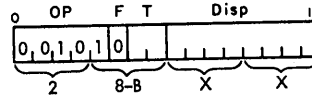
17162 A

Bit 9 (BO) in the two word instruction must equal
zero. The conditions of the Carry and Overflow in-
dicators are stored in the low-order bits of the word
specified by the effective address: Carry indicator
at bit 14 and the Overflow indicator at bit 15.

Bits 0 through 7 of the word at the effective
address remain unchanged and bits 8 through 13 are
reset to zero. The indicators are reset. An ON
status stores a one bit; and OFF status a zero bit.

```
 0              7 8      13 14 15
  |  ,  ,  ,  ,  |  |0 0 0 0 0 0| | |
      Unchanged              Overflow
                            Carry
```

17 163
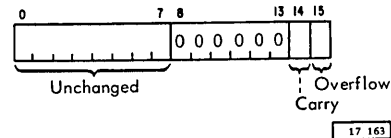
Indicators: The Carry and Overflow indicators are
reset as they are stored.

Hexadecimal Representation

One-Word Instruction

28XX	Store status of indicators in CSL at EA (I+DISP)
29XX	Store status of indicators in CSL at EA (XR1+DISP)
2AXX	Store status of indicators in CSL at EA (XR2+DISP)
2BXX	Store status of indicators in CSL at EA (XR3+DISP)

Two-Word Instruction, Direct Addressing

2C00XXXX   Store status of indicators in CSL at EA (Addr)

2D00XXXX   Store status of indicators in CSL at EA (Addr+XR1)

2E00XXXX   Store status of indicators in CSL at EA (Addr+XR2)

2F00XXXX   Store status of indicators in CSL at EA (Addr+XR3)

Two-Word Instruction, Indirect Addressing

2C80XXXX   Store status of indicators in CSL at EA (V in CSL at Addr)

2D80XXXX   Store status of indicators in CSL at EA (V in CSL at "Addr +XR1")

2E80XXXX   Store status of indicators in CSL at EA (V in CSL at "Addr +XR2")

2F80XXXX   Store status of indicators in CSL at EA (V in CSL at "Addr +XR3")

2.   Write or clear the storage protect bit from the core storage address specified by the instruction.
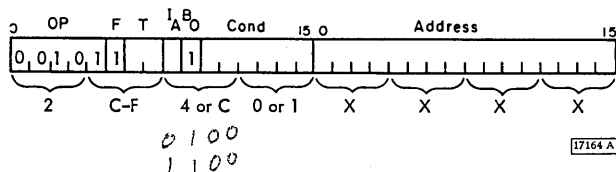
The following conditions must exist:

1.   A two word instruction (F bit equals 1) must be used.
2.   Bit 9 (BO) must equal 1.
3.   The Write Storage Protection Bit switch must be on to change storage protection bits.

Then, bit 15 determines whether the storage protect bit for the word specified by the effective address of the instruction is written or cleared:

   B15 is zero -- Storage protect bit is cleared.
   B15 is one -- Storage protect bit is written.

As long as the Write Storage Protection Bit switch remains in the on position the program continues to have the ability to write or clear storage protection bits. If the switch is off this instruction performs as a NO-OP (No-Operation).

Hexadecimal Representation

Two-Word Instruction, Direct Addressing

2C40XXXX   Clear storage protect bit in CSL at EA (Addr)

2C41XXXX   Write storage protect bit in CSL at EA (Addr)

2D40XXXX   Clear storage protect bit in CSL at EA (Addr +XR1)

2D41XXXX   Write storage protect bit in CSL at EA (Addr +XR1)

2E40XXXX   Clear storage protect bit in CSL at EA (Addr +XR2)

2E41XXXX   Write storage protect bit in CSL at EA (Addr +XR2)

2F40XXXX   Clear storage protect bit in CSL at EA (Addr +XR3)

2F41XXXX   Write storage protect bit in CSL at EA (Addr +XR3)

Two-Word Instruction, Indirect Addressing

2CC0XXXX   Clear storage protect bit in CSL at EA (V in CSL at Addr)

2CC1XXXX   Write storage protect bit in CSL at EA (V in CSL at Addr)

2DC0XXXX   Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR1")

2DC1XXXX   Write storage protect bit in CSL at EA (V in CSL at "Addr +XR1")

2EC0XXXX   Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR2")

2EC1XXXX   Write storage protect bit in CSL at EA (V in CSL at "Addr +XR2")

2FC0XXXX   Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR3")

2FC1XXXX   Write storage protect bit in CSL at EA (V in CSL at "Addr +XR3")

LOAD STATUS (LDS)
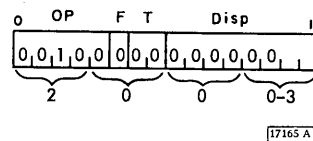
Description: This instruction applies to the single word format only. The Carry and Overflow indicators are loaded with the status of the bits in positions 14 (Carry) and 15 (Overflow) of the instruction. Normally this status was stored into this instruction by a previous Store Status instruction. Core Storage remains unchanged. A one bit causes an indicator ON condition and a zero bit an indicator OFF condition.

X10 INST
CYCLE STEAL

OTHER THAN X10
INSTR

BIT 2 OF I/O DSW IS SET TO 1
NO INTERRUPT OCCURS

INTERNAL INTERRUPT OCCURS
IF CHECK STOP ON MACHINE STOPS

21

Indicators: The Carry and Overflow indicators are set according to the bits at positions 14 and 15.

Hexadecimal Representation

One-Word Instruction (only)

2000	Set CARRY and OVERFLOW indicators OFF	
2001	Set OVERFLOW ON and CARRY OFF	
2002	Set OVERFLOW OFF and CARRY ON	
2003	Set CARRY and OVERFLOW indicator ON	

ARITHMETIC INSTRUCTIONS
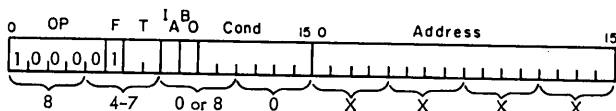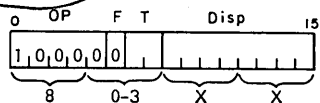
ADD (A)

Description: The contents of the core storage location specified by the instruction are added to the contents of the accumulator. Two's complement arithmetic is used; that is, both negative operands and sums are in two's complement form. The contents of the core storage remains unchanged. See Appendix C for details of "data addition."

Indicators: The Overflow indicator is turned ON if the magnitude of the sum is too large to be represented in the Accumulator; that is, greater than $+2^{15} - 1$ or less than -2^{15} (this is detected by a resultant carry out of one and only one of the two high-order bit positions of the accumulator). If overflow was previously ON, it is not changed. (Overflow can be reset by testing, or a Load Status or Store Status instruction. See Branch or Skip on Condition instruction.) The Carry indicator is set by a carry out of the high-order bit position of the accumulator.

Hexadecimal Representation

One-Word Instruction

80XX	Add contents of CSL at EA (I+DISP) to A
81XX	Add contents of CSL at EA (XR1+DISP) to A
82XX	Add contents of CSL at EA (XR2+DISP) to A
83XX	Add contents of CSL at EA (XR3+DISP) to A

Two-Word Instruction, Direct Addressing

8400XXXX	Add contents of CSL at EA (Addr) to A
8500XXXX	Add contents of CSL at EA (Addr+XR1) to A
8600XXXX	Add contents of CSL at EA (Addr+XR2) to A
8700XXXX	Add contents of CSL at EA (Addr+XR3) to A

Two-Word Instruction, Indirect Addressing

8480XXXX	Add contents of CSL at EA (V in CSL at Addr) to A
8580XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") to A
8680XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") to A
8780XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") to A

DOUBLE ADD (AD)
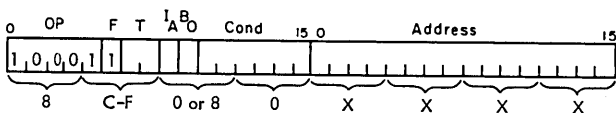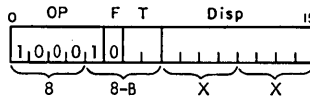
Description: The contents of the core storage location specified by the instruction and the next higher addressed location are added to the contents of the Accumulator (A) and its extension (Q). This provides double precision addition where the Accumulator and its extension are considered as one 32 bit accumulator. The sum replaces the contents of A and Q. Core Storage remains unchanged.

The effective address formed by the instruction must be an even address for correct operation. If the effective address is odd, the contents of the location are added to both the Accumulator and its extension, and may be added incorrectly into the Accumulator.

Indicators: When the instruction is completed, the Carry indicator represents the results of this instruction — not previous instructions. The Carry indicator is set ON by detection of a Carry out of the high-order position of the Accumulator.

The Overflow indicator is turned ON by this instruction if the magnitude of the sum is greater than $+2^{31} - 1$ or less than -2^{31}. If this indicator was ON before the instruction, no change occurs. If OFF, it is turned ON when the magnitude of the number is too large to be represented (this is detected by a carry out of one and only one of the two high-order bits of the Accumulator).

Hexadecimal Representation

One-Word Instruction

88XX	Add contents of CSL at EA (I+DISP) and EA+1 to A and Q
89XX	Add contents of CSL at EA (XR1+DISP) and EA+1 to A and Q
8AXX	Add contents of CSL at EA (XR2+DISP) and EA+1 to A and Q
8BXX	Add contents of CSL at EA (XR3+DISP) and EA+1 to A and Q

Two-Word Instruction, Direct Addressing

8C00XXXX	Add contents of CSL at EA (Addr) and EA+1 to A and Q
8D00XXXX	Add contents of CSL at EA (Addr+XR1) and EA+1 to A and Q
8E00XXXX	Add contents of CSL at EA (Addr+XR2) and EA+1 to A and Q
8F00XXXX	(Add contents of CSL at EA (Addr+XR3) and EA+1 to A and Q

Two-Word Instruction, Indirect Addressing

8C80XXXX	Add contents of CSL at EA (V in CSL at Addr) and EA+1 to A and Q
8D80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 to A and Q
8E80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 to A and Q
8F80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 to A and Q

SUBTRACT (S)

Description: The contents of the core storage location specified by the instruction are subtracted from the contents of the Accumulator. The result replaces the contents of the Accumulator. Two's complement arithmetic is used; that is, both negative operands and differences are in two's complement form. Core Storage remains unchanged.

Indicators: The Overflow indicator is turned ON if the magnitude of the difference is too large to be represented in the Accumulator; that is, greater than $+2^{15} - 1$ or less than -2^{15}. If Overflow was previously ON, it is not changed. (Overflow can be reset by testing or a Load or Store Status instruction. See Branch or Skip on Condition Instruction.) This is detected by a borrow from one and only one of the two high-order bit positions of the accumulator. The Carry indicator is set by a borrow from the high-order position.

Hexadecimal Representation

One-Word Instruction

90XX	Subtract contents of CSL at EA (I+DISP) from A
91XX	Subtract contents of CSL at EA (XR1+DISP) from A
92XX	Subtract contents of CSL at EA (XR2+DISP) from A
93XX	Subtract contents of CSL at EA (XR3+DISP) from A

Two-Word Instruction, Direct Addressing

9400XXXX	Subtract contents of CSL at EA (Addr) from A

9500XXXX   Subtract contents of CSL at EA
            (Addr+XR1) from A
9600XXXX   Subtract contents of CSL at EA
            (Addr+XR2) from A
9700XXXX   Subtract contents of CSL at EA
            (Addr+XR3) from A

Two-Word Instruction, Indirect Addressing

9480XXXX   Subtract contents of CSL at EA
            (V in CSL at Addr) from A
9580XXXX   Subtract contents of CSL at EA
            (V in CSL at "Addr+XR1")
            from A
9680XXXX   Subtract contents of CSL at EA
            (V in CSL at "Addr+XR2")
            from A
9780XXXX   Subtract contents of CSL at EA
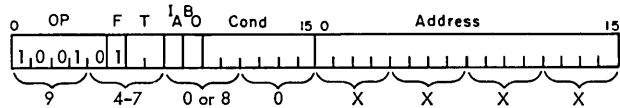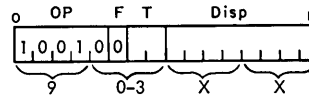   (V in CSL at "Addr+XR3")
            from A
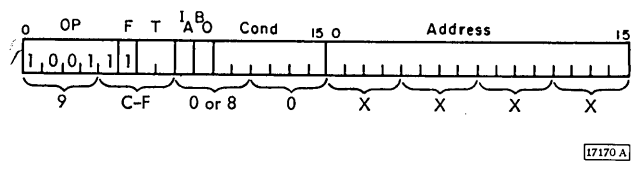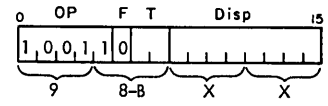
DOUBLE SUBTRACT (SD)

Description: The contents of the core storage loca-
tion specified by the instruction and the next higher
memory location are subtracted arithmetically from
the contents of the Accumulator (A) and its extension
(Q). This provides double precision subtraction where
the Accumulator and its extension are considered as
one 32-bit accumulator. The difference replaces the
contents of A and Q. Memory remains unchanged.
The effective address formed by the instruction must
be an even address for correct operation. If the ef-
fective address is odd, the contents of that location
are subtracted from both the Accumulator and its ex-
tension, and may be incorrect in the Accumulator.

Indicators: The Overflow indicator is turned ON if
the magnitude of the difference is too large to be rep-
resented in the Accumulator (A) and its extension
(Q), or more specifically, greater than $+2^{31} - 1$ or
less than -2^{31} . This is detected by a borrow from
one and only one of the two high-order bit positions
of the Accumulator. If Overflow was previously
ON, it is not changed. (Overflow can be reset by
testing or by a Load or Store Status instruction.
See Branch or Skip on Condition instruction.) The
Carry indicator is set by a borrow from the high-
order position.

Hexadecimal Representation

One-Word Instruction

98XX   Subtract contents of CSL at EA (I+DISP)
        and EA+1 from A and Q
99XX   Subtract contents of CSL at EA
        (XR1+DISP) and EA+1 from A and Q
9AXX   Subtract contents of CSL at EA
        (XR2+DISP) and EA+1 from A and Q
9BXX   Subtract contents of CSL at EA
        (XR3+DISP) and EA+1 from A and Q

Two-Word Instruction, Direct Addressing

9C00XXXX   Subtract contents of CSL at EA
            (Addr) and EA+1 from A and Q
9D00XXXX   Subtract contents of CSL at EA
            (Addr+XR1) and EA+1 from A and Q
9E00XXXX   Subtract contents of CSL at EA
            (Addr+XR2) and EA+1 from A and Q
9F00XXXX   Subtract contents of CSL at EA
            (Addr+XR3) and EA+1 from A and Q

Two-Word Instruction, Indirect Addressing

9C80XXXX   Subtract contents of CSL at EA
            (V in CSL at Addr) and EA+1
            from A and Q
9D80XXXX   Subtract Contents of CSL at EA
            (V in CSL at "Addr+XR1") and
            EA+1 from A and Q
9E80XXXX   Subtract contents of CSL at EA
            (V in CSL at "Addr+XR2") and
            EA+1 from A and Q
9F80XXXX   Subtract contents of CSL at EA
            (V in CSL at "Addr+XR3") and
            EA+1 from A and Q

25

M
D

MULTIPLY (M)

```
  0   OP    F  T      Disp      15
  ┌──────────────────────────────┐
  │ 1 0 1 0 0 0 │  │              │
  └──────────────────────────────┘
       A     0-3    X         X
```

```
  0   OP    F  T  I A B O  Cond  15 0      Address           15
  ┌────────────────────────────┐┌───────────────────────────┐
  │ 1 0 1 0 0 1 │ │ │          ││                            │
  └────────────────────────────┘└───────────────────────────┘
       A     4-7  0 or 8   0     X     X        X        X
```
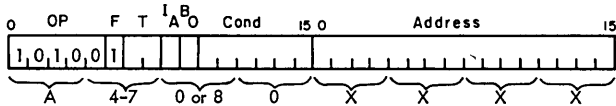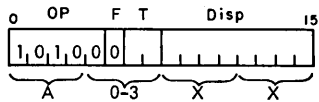
[17171 A]

Description: The contents of the core storage location specified by the instruction (multiplicand) are multiplied algebraically by the contents of the Accumulator (multiplier). The 32-bit product replaces the contents of the Accumulator (A) and its extension (Q). The most significant bits of the product are in the Accumulator. Core storage remains unchanged. The product is in the double precision format.

Indicators: Neither the Overflow nor the Carry indicators are changed.

Programming Note: The largest product that can be developed is 2^{30}. This occurs when the multiplier and multiplicand are both the largest negative numbers, -2^{15}.

Hexadecimal Representation

One-Word Instruction

A0XX Multiply contents of CSL at EA (I+DISP) by A

A1XX Multiply contents of CSL at EA (XR1+DISP) by A

A2XX Multiply contents of CSL at EA (XR2+DISP) by A

A3XX Multiply contents of CSL at EA (XR3+DISP) by A

Two-Word Instruction, Direct Addressing

A400XXXX Multiply contents of CSL at EA (Addr) by A

A500XXXX Multiply contents of CSL at EA (Addr+XR1) by A

A600XXXX Multiply contents of CSL at EA (Addr+XR2) by A

A700XXXX Multiply contents of CSL at EA (Addr+XR3) by A

Two-Word Instruction, Indirect Addressing

A480XXXX Multiply contents of CSL at EA (V in CSL at Addr) by A

A580XXXX Multiply contents of CSL at EA (V in CSL at "Addr+XR1") by A

A680XXXX Multiply contents of CSL at EA (V in CSL at "Addr+XR2") by A

A780XXXX Multiply contents of CSL at EA (V in CSL at "Addr+XR3") by A

DIVIDE (D)

```
  0   OP    F  T      Disp      15
  ┌──────────────────────────────┐
  │ 1 0 1 0 1 0 │  │              │
  └──────────────────────────────┘
       A     8-B    X         X
```

```
  0   OP    F  T  I A B O  Cond  15 0      Address           15
  ┌────────────────────────────┐┌───────────────────────────┐
  │ 1 0 1 0 1 1 │ │ │          ││                            │
  └────────────────────────────┘└───────────────────────────┘
       A     C-F  0 or 8   0     X     X        X        X
```
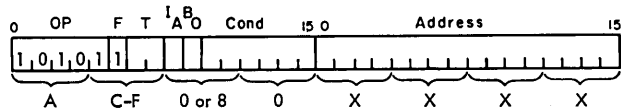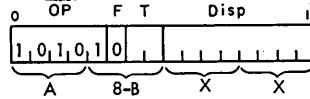
[17172 A]

Description: The contents of the Accumulator and its extension (a 32-bit double precision word) are divided by the contents of the core storage location specified by the instruction. The quotient and remainder replace the contents of the Accumulator and the Accumulator extension, respectively. The "sign" of the remainder is the same as the dividend.

The largest dividend that can correctly be operated upon is $2^{30} + 2^{15} - 1$ if divided by the largest negative divisor (-2^{15}).

Indicators: The Overflow indicator is turned ON when division by zero is attempted or when the quotient overflow condition exists. A quotient overflow occurs when the factors are such that the quotient would exceed the range of -2^{15} to $+2^{15} - 1$. An overflow causes the accumulator and its extension (Q) to be left in an undefined state. Divide by zero leaves the Accumulator and its extension unchanged.

Hexadecimal Representation

One-Word Instruction

A8XX Divide A and Q by contents of CSL at EA (I+DISP)

A9XX Divide A and Q by contents of CSL at EA (XR1+DISP)

AAXX Divide A and Q by contents of CSL at EA (XR2+DISP)

ABXX Divide A and Q by contents of CSL at EA (XR3+DISP)

Two-Word Instruction, Direct Addressing

AC00XXXX Divide A and Q by contents of CSL at EA (Addr)

AD00XXXX Divide A and Q by contents of CSL at EA (Addr+XR1)

AE00XXXX Divide A and Q by contents of CSL at EA (Addr+XR2)

AF00XXXX Divide A and Q by contents of CSL at EA (Addr+XR3)

Two-Word Instruction, Indirect Addressing

AC80XXXX Divide A and Q by contents of CSL at EA (V in CSL at Addr)

AD80XXXX Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR1")

AE80XXXX Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR2")

AF80XXXX Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR3")

LOGICAL AND (AND)

Description: The contents of the core storage location specified by the instruction are ANDed bit by bit with the contents of the Accumulator. The following table defines the AND operation.

AND

Memory	1	1	0	0
Accum	1	0	1	0
Result	1	0	0	0

The result replaces the contents of the Accumulator. Core storage remains unchanged.

Indicators: The Carry and Overflow indicators are not changed by this operation.

Hexadecimal Representation

One-Word Instruction

E0XX   AND contents of CSL at EA (I+DISP) with A

E1XX   AND contents of CSL at EA (XR1+DISP) with A

E2XX   AND contents of CSL at EA (XR2+DISP) with A

E3XX   AND contents of CSL at EA (XR3+DISP) with A

Two-Word Instruction, Direct Addressing

E400XXXX AND contents of CSL at EA (Addr) with A

E500XXXX AND contents of CSL at EA (Addr+XR1) with A

E600XXXX AND contents of CSL at EA (Addr+XR2) with A

E700XXXX AND contents of CSL at EA (Addr+XR3) with A

Two-Word Instruction, Indirect Addressing

E480XXXX AND contents of CSL at EA (V in CSL at Addr) with A

E580XXXX AND contents of CSL at EA (V in CSL at "Addr+XR1") with A

E680XXXX AND contents of CSL at EA (V in CSL at "Addr+XR2") with A

E780XXXX AND contents of CSL at EA (V in CSL at "Addr+XR3") with A

LOGICAL OR (OR)
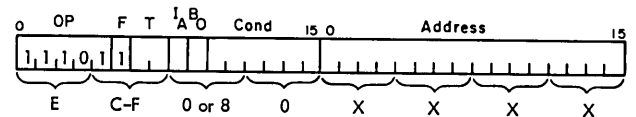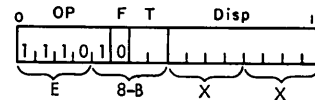
Description: The contents of the core storage location specified by the instruction are ORed bit by bit with the contents of the Accumulator. The following table defines the OR operation:

OR

Memory	1	1	0	0
Accum	1	0	1	0
Result	1	1	1	0

The result replaces the contents of the accumulator. Core storage remains unchanged.

Indicators.: The Carry and Overflow indicators are not changed by this operation.

Hexadecimal Representation

One-Word Instruction

E8XX	OR contents of CSL at EA (I+DISP) with A
E9XX	OR contents of CSL at EA (XR1+DISP) with A
EAXX	OR contents of CSL at EA (XR2+DISP) with A
EBXX	OR contents of CSL at EA (XR3+DISP) with A

Two-Word Instruction, Direct Addressing

EC00XXXX	OR contents of CSL at EA (Addr) with A
ED00XXXX	OR contents of CSL at EA (Addr+XR1) with A
EE00XXXX	OR contents of CSL at EA (Addr+XR2) with A
EF00XXXX	OR contents of CSL at EA (Addr+XR3) with A

Two-Word Instruction, Indirect Addressing

EC80XXXX	OR contents of CSL at EA (V in CSL at Addr) with A
ED80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR1") with A
EE80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR2") with A
EF80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR3") with A

LOGICAL EXCLUSIVE OR (EOR)

Description: The contents of the core storage location specified by the instruction are Exclusive ORed bit by bit with the contents of the Accumulator. The following table defines the Exclusive OR operation:

Exclusive OR

Memory	1	1	0	0
Accum	1	0	1	0
Result	0	1	1	0

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The result replaces the contents of the Accumulator. Core storage remains unchanged.

Indicators: The Carry and Overflow indicators are not changed by this operation.

Hexadecimal Representation

One-Word Instruction

F0XX	EOR contents of CSL at EA (I+DISP) with A
F1XX	EOR contents of CSL at EA (XR1+DISP) with A
F2XX	EOR contents of CSL at EA (XR2+DISP) with A
F3XX	EOR contents of CSL at EA (XR3+DISP) with A

Two-Word Instruction, Direct Addressing

F400XXXX	EOR contents of CSL at EA (Addr) with A
F500XXXX	EOR contents of CSL at EA (Addr+XR1) with A
F600XXXX	EOR contents of CSL at EA (Addr+XR2) with A
F700XXXX	EOR contents of CSL at EA (Addr+XR3) with A

Two-Word Instruction, Indirect Addressing

F480XXXX	EOR contents of CSL at EA (V in CSL at Addr) with A
F580XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR1") with A
F680XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR2") with A
F780XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR3") with A
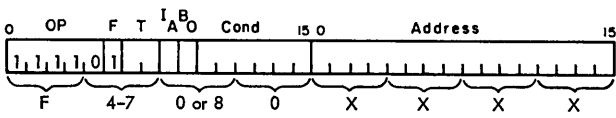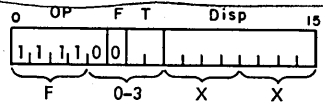
SHIFT INSTRUCTIONS

All shift instructions are single word format only
(F = 0). They are divided into subclasses as de-
fined by bit positions 8 and 9. Those that have their
shift count defined by the TAG bits shift as shown in
Table 3.

Table 3. Shift Count

Tag	Shift Count Determined By:
00	Low-Order 6 Bits of Disp
01	Low-Order 6 Bits of XR1
10	Low-Order 6 Bits of XR2
11	Low-Order 6 Bits of XR3

17 181

If the shift count is zero, the instruction performs
a No-OP.

SHIFT LEFT LOGICAL A (SLA)
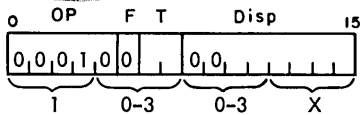
17182 A

Description: The Accumulator (A) is shifted left
the number of spaces specified by the Shift Count
(Table 3). Vacated bit positions are set to zero.
Bits leaving the high-order (bit 0 of A) position are
shifted into the Carry indicator. (See Indicators
below.) The Extension (Q) is not affected. Note
that bit positions 8 and 9 must be 00.

Indicators: The Carry indicator is turned on for
each one and off for each zero shifted left from the
high-order position of A. The Overflow indicator
is unaffected.

Hexadecimal Representation

One-Word Instructions (Only)

    10*X   Contents of A shift left the number of
              shift counts in DISP
    1100   Contents of A shift left the number of
              shift counts in XR1
    1200   Contents of A shift left the number of
              shift counts in XR2

    1300   Contents of A shift left the number of
              shift counts in XR3

*The third from the high order position can be 0, 1,
2, or 3, depending on the value of the shift count.

SHIFT LEFT LOGICAL A & Q (SLT)
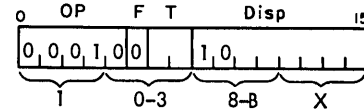
17184 A

Description: The Accumulator (A) and its extension
(Q) are shifted left as a 32-bit double precision
register. Vacated bit positions are set to zero.
Bits leaving the high-order position (bit position 0
of A) are shifted into the Carry indicator.

Indicators: The Carry indicator is turned on for
each one and off for each zero shifted left from
high-order position of A. The Overflow indicator
is unaffected.

Hexadecimal Representation

One-Word Instructions (Only)

    10*X   Contents of A and Q shift left the num-
              ber of shift counts in DISP
    1180   Contents of A and Q shift left the num-
              ber of shift counts in XR1
    1280   Contents of A and Q shift left the num-
              ber of shift counts in XR2
    1380   Contents of A and Q shift left the num-
              ber of shift counts in XR3

*The third from the high-order position can be 8, 9,
A, or B depending on the value of the shift count.

SHIFT LEFT AND COUNT A (SLCA)

17186 A

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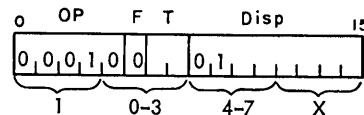
Description: A TAG of 00 causes this instruction to be performed as a Shift Left A instruction. A TAG specifying one of the index registers causes the shift count to be transferred from the low-order six bits of the specified register to the shift counter. This count is decremented by one for each position that the contents of the Accumulator (A) are shifted to the left. Vacated bit positions are set to zero.

The shift terminates either when an attempt is made to shift a one from the high-order position of A (the "1" remains in the high-order position after the instruction has terminated) or when the shift count has been decremented to zero. The decremented count is then loaded back into the six low-order bit positions of the index register (bits 10-15) and bits 8 and 9 are reset to zero. Bit positions 0-7 of the index register remain unchanged at completion of the instruction. If the shift count is initially zero or if the high order position of the accumulator (Bit 0) is initially a one bit, the instruction performs as a NO-OP.

Indicators: The Carry indicator will be OFF at the end of the operation if the shift is terminated by the detection of the count reaching zero. The Carry indicator will be ON at the end of the operation if the shift is terminated by the detection of a 1 in bit 0 of the Accumulator before the shift count reaches zero. For T = 0 the Carry indicator is set as in Shift Left instruction. The Overflow indicator is unaffected.

SLCA Examples: For the four examples below, assume the Index Register was previously loaded by an LDX instruction. Only the low-order bit positions (10-15) of the Index Register (XR) are shown and only the high-order bit positions (0-5) of the Accumulator (A) are shown. Those bit positions containing an X can be zero or one.

Example Number	1	2	3	4
XR before SLCA	000011	000100	000101	000110
XR after SLCA	000000	000000	000001	000010
A before SLCA	00001X	00001X	00001X	00001X
A after SLCA	01XXXX	1XXXXX	1XXXXX	1XXXXX
Carry Indicator after SLCA	OFF*	OFF*	ON**	ON**

*If no one bits were contained in the field defined by the Index Register (Examples 1 and 2), the program can determine the value of Accumulator bit 0 only by testing the Accumulator sign. (Carry Indicator is OFF and the Index Register is zero.)

**If a one bit was contained in the field defined by the Index Register (Examples 3 and 4), the SLCA instruction was terminated when an attempt was made to shift the one out of the high order position, leaving the Carry Indicator ON and the Index Register at a non-zero condition. (The one bit remains in the high-order position.)

Hexadecimal Representation

One-Word Instructions (Only)

10*X	Contents of A shift left the number of shift counts in DISP
1140	**Contents of A shift left the number of shift counts in XR1
1240	**Contents of A shift left the number of shift counts in XR2
1340	**Contents of A shift left the number of shift counts in XR3

*The third from the high-order position can be 4, 5, 6, or 7, depending on the value of the shift count.

**These instructions are terminated either when an attempt is made to shift a one bit from the high-order position of the Accumulator (with a non-zero shift count remaining) or when the shift count has been decremented to zero.

SHIFT LEFT AND COUNT A & Q (SLC)
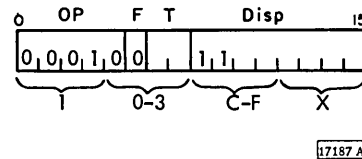
Description: This instruction is the same as the Shift Left and Count A except that both the Accumulator (A) and its Extension (Q) are shifted. Bit position 0 of Q is shifted into bit position 15 of A and vacated positions at the right of Q are set to zero.

Indicators: The Carry indicator will be OFF at the end of the operation if the shift is terminated by the detection of the count reaching zero. The Carry indicator will be ON at the end of the operation if the shift is terminated by the detection of a 1 in the bit zero position of the Accumulator before the shift count reaches zero. For T = 0 the Carry indicator is set as in Shift Left instruction.

The Overflow indicator is unaffected.

Hexadecimal Representation

One-Word Instructions (Only)

10*X	Contents of A and Q shift left the number of shift counts in DISP
11C0	**Contents of A and Q shift left the number of shift counts in XR1
12C0	**Contents of A and Q shift left the number of shift counts in XR2
13C0	Contents of A and Q shift left the number of shift counts in XR3

*The third from the high-order position can be C, D, E, or F, depending on the value of the shift count.

**These instructions are terminated either when an attempt is made to shift a one bit from the high-order position of the Accumulator (with a non-zero shift count remaining) or when the shift count has been decremented to zero.

SHIFT RIGHT LOGICAL A (SRA)
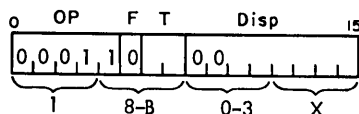
17188 A

Description: The Accumulator (A) is shifted right the number of places indicated by the Shift Count. Zeros are entered in all vacated spaces. The Extension (Q) is undisturbed. Low-order bits of A are lost.

Indicators: The Carry and Overflow indicators are not affected.

Hexadecimal Representation

One-Word Instructions (Only)

18*X   Contents of A shift right the number of shift counts in DISP

1900   Contents of A shift right the number of shift counts in XR1

1A00   Contents of A shift right the number of shift counts in XR2

1B00   Contents of A shift right the number of shift counts in XR3

*The third from the high-order position can be 0, 1, 2, or 3, depending on the value of the shift count.

SHIFT RIGHT A & Q (SRT)
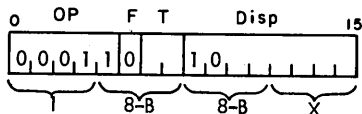
17189 A

Description: The Accumulator (A) and Extension (Q) are shifted right as a 32-bit double precision register. The value of the Sign (bit position 0 and A) is entered

in all vacated spaces. Low-order bits of Q are lost.

Indicators: The Carry and Overflow indicators are not changed.

Hexadecimal Representation

One Word Instruction (Only)

18*X   Contents of A and Q shift right the number of shift counts in DISP

1980   Contents of A and Q shift right the number of shift counts in XR1

1A80   Contents of A and Q shift right the number of shift counts in XR2

1B80   Contents of A and Q shift right the number of shift counts in XR3

*The third from the high-order position can be 8, 9, A, or B, depending on the value of the shift count.

ROTATE RIGHT A & Q (RTE)
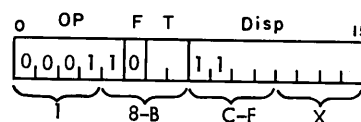
17190 A

Description: The Accumulator (A) and Extension (Q) are rotated to the right as a 32-bit double precision register the number of bit positions specified the Shift Count. Bit position 15 of the Extension (Q) is linked to bit position 0 of the Accumulator (A) to form a continuous loop so that the high-order positions of the Accumulator pick up the bits dropped from the low-order position of the Extension.

Indicators: The Carry and Overflow indicators are not changed.

Hexadecimal Representation

One Word Instruction (Only)

18*X   Contents of A and Q rotate right the number of counts in DISP

19C0   Contents of A and Q rotate right the number of counts in XR1

1AC0   Contents of A and Q rotate right the number of counts in XR2

1BC0   Contents of A and Q rotate right the number of counts in XR3

*The third from the high-order position can be C, D, E, or F, depending on the value of the shift count.

31

BSC
BOSC

BRANCH INSTRUCTIONS

BRANCH OR SKIP ON CONDITION (BSC or BOSC)
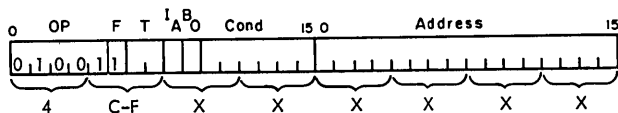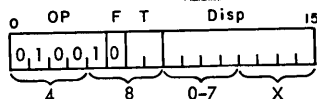
Description: There are six testable conditions associated with the Accumulator. These conditions may be tested by indicating the bit pattern in the DISPLACE-MENT of the instruction.

The six Accumulator conditions that can be tested are shown by bit position.

Bit	Condition
15	Overflow OFF
14	Carry OFF
13	Accumulator Even
12	Accumulator Plus (greater than zero)
11	Accumulator Negative
10	Accumulator Zero

When $F = 0$, the instruction executed is a Skip on Condition when one or more of the conditions specified is true. This enables the program to skip over the next one word instruction. If none of the conditions specified are true, the next instruction in sequence is executed.

When $F = 1$, the instruction executed is a Branch to the Effective Address (EA) when none of the condition(s) specified are true. If any one of the condition(s) specified in bit positions 10-15 is true, the next instruction in sequence is executed. Examples are shown in Figure 6.

The EA is calculated as follows:

$F = 1$ $IA = 0$ T = 00   EA = ADDR
          T = 01   EA = XR1 + ADDR
          T = 10   EA = XR2 + ADDR
          T = 11   EA = XR3 + ADDR

When the IA bit is equal to a one ($IA = 1$), this instruction enables the program to return to a mainline program from a program subroutine of interrupt routine. This is accomplished by making the EA of this instruction identical to the EA of a previously executed Branch and Store Instruction Register (BSI) instruction. The EA as calculated below is loaded into the Instruction Register.

$F = 1$ $IA = 1$ T = 00   EA = *C(ADDR)
          T = 01   EA = C(XR1 + ADDR)
          T = 10   EA = C(XR2 + ADDR)
          T = 11   EA = C(XR3 + ADDR)

NOTE: *C means "Contents of"

Programming Note: When an interrupt request has been detected by a priority level, the program is directed to service the request by interrupting. During the servicing, all interrupt requests of equal or lower status are effectively constrained from interrupting while the servicing of the higher priority is in progress. However, if a request is detected for a higher priority level than is presently in progress, the program is immediately interrupted again. This is frequently called Nesting of Interrupts.

At the completion of servicing any level of interrupt, it is necessary to signal the priority hardware to reset the priority-status of the highest level that is on. This reset permits lower priority requests that may have been temporarily constrained but recorded to be accepted once again by the P-C. This is effected by making Bit 9 = 1 in the BSC instruction. A BSC instruction with Bit 9=1 is called a Branch Out of Interrupts (BOSC). This programmed recognition of waiting interrupts should not be confused with a normal subroutine linkage back to a mainline program in which Bit 9 should be set to zero.

The BSC is a conditional instruction. When Bit 9 = 1, the reset of the interrupt level occurs only if the Branch or Skip occurs. If the Branch or Skip does not occur, the interrupt level is not reset.

Indicators: The Overflow indicator is reset when tested. The Carry indicator is not reset by testing. The contents of the Accumulator are not changed by testing. If no conditions are specified, a Skip does not occur on the SKIP instruction ($F = 0$) or a branch does occur on the BRANCH instruction ($F = 1$).

BSI

Bit Positions: 10 11 12 13 ACC Conditions: Zero Minus Plus Even					Skip (F = 0)	Branch (F=1)
Test Conditions	1	1	1	0	Always	Never
	0	0	0	0	Never	Always
	0	0	1	0	Plus	Not Plus
	1	1	0	0	Not Plus	Plus
	0	1	0	0	Minus	Not Minus
	1	0	1	0	Not Minus	Minus
	1	0	0	0	Zero	Not Zero
	0	1	1	0	Not Zero	Zero
	0	0	0	1	Even	Odd
	0	0	1	1	Even or Plus	Odd and Minus
	0	1	0	1	Even or Minus	Odd and Plus

Notes: 1. ACC Zero is not a plus condition.

2. Skip and Branch columns specify action or ACC condition required for Skip or Branch.

3. Skip on Odd condition, Carry ON, or Overflow ON are not possible.

17441A

● Figure 6. BSC Examples

Hexadecimal Representation

One-Word Instruction

48*X   SKIP the next one-word instruction if ANY condition is sensed

*The third from the high-order position can be 0, 1, 2, or 3 (BSC) or 4, 5, 6, or 7 (BOSC), depending on which conditions are tested.

Two-Word Instruction, Direct Addressing

4C*XXXXX   Branch to CSL at EA (Addr) on NO condition
4D*XXXXX   Branch to CSL at EA (Addr+XR1) on NO condition
4E*XXXXX   Branch to CSL at EA (Addr+XR2) on NO condition
·4F*XXXXX   Branch to CSL at EA (Addr+XR3) on NO condition

*The third from the high-order position can be 0, 1, 2, or 3 (BSC) or 4, 5, 6, or 7 (BOSC). These hexadecimal values are determined by the conditions being tested.

Two-Word Instruction, Indirect Addressing

4C*XXXXX   Branch to CSL at EA (V in CSL at Addr) on NO condition
4D*XXXXX   Branch to CSL at EA (V in CSL at "Addr+XR1") on NO condition
4E*XXXXX   Branch to CSL at EA (V in CSL at "Addr+XR2") on NO condition
4F*XXXXX   Branch to CSL at EA (V in CSL at "Addr+XR3") on NO condition

*The third from the high-order position can be 8, 9, A, B (BSC) or C, D, E, or F (BOSC). These hexadecimal values are determined by the conditions being tested.

BRANCH AND STORE INSTRUCTION REGISTER (BSI)

17193 A

Description: When F = 0 (one word format), the contents of the Instruction Register are stored in the core storage location specified by the effective address. The stored address is that of the next instruction in the normal sequence. The Instruction Register is then set to the value of the effective address plus one, and program execution proceeds from that point.

For example, a BSI instruction located at core storage address 0500, with an effective address of 0550, would store the address 0501 at location 0550 and then branch to 0551.
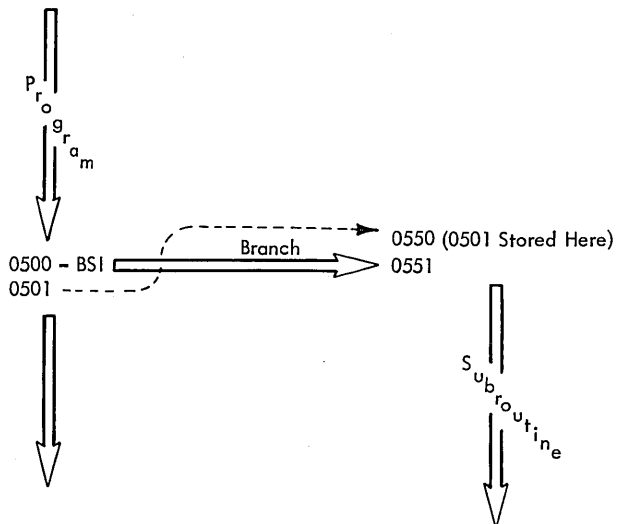
BSC, Indirect (With Address of 550)

17194B

A BSC instruction with an IA bit of one and an ADDRESS of 0550 would be used to return from the subroutine.

When F = 1 (two word instruction format), the above function is conditionally executed depending on the condition bits specified in the Displacement. These Accumulator condition bits are defined in the preceding BSC instruction. If any one of the conditions specified is true, the previously explained branch does not occur. Instead, the next instruction in sequence is performed. If none of the conditions are true, the Instruction Register is stored at the effective address (specified by the ADDRESS) and the branch is to EA + 1.

Internal, CE, and external level interrupts are suppressed for the first instruction following a BSI instruction. Therefore, the Mask Register (See Interrupt section) may be set without the possibility of an interrupt other than trace immediately following the BSI instruction.

Indicators: When F = 0, the status of the indicators is unchanged. When F = 1, the Overflow indicator is reset if tested.

Hexadecimal Representation

One-Word Instruction

40XX	Store next sequential address in CSL at EA (I+DISP) and Branch to EA+1
41XX	Store next sequential address in CSL at EA (XR1+DISP) and Branch to EA+1
42XX	Store next sequential address in CSL at EA (XR2+DISP) and Branch to EA+1
43XX	Store next sequential address in CSL at EA (XR3+DISP) and Branch to EA+1

Two-Word Instruction, Direct Addressing

44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR1) and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR2) and Branch to EA+1
47*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR3) and Branch to EA+1

*The third from the high-order position can be 0, 1, 2, or 3, depending on the conditions being tested.

Two-Word Instruction, Indirect Addressing

44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR1") and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR2") and Branch to EA+1
47*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR3") and Branch to EA+1

*The third from the high-order position can be 8, 9, A, or B, depending on the conditions being tested.

MODIFY INDEX AND SKIP (MDX)
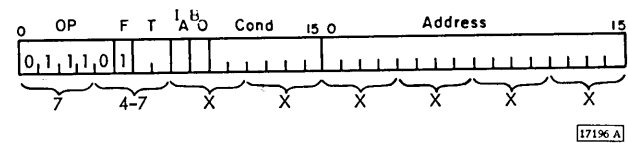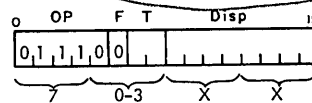
Description: The Modify Index and Skip instruction has many uses. The specific operation and the registers involved depend upon the instruction format. An Index Register, the Instruction Register, or a core storage word* may be modified by a value; this value may be the expanded Displacement*, the Address, or the contents of the core storage location specified by Address.

*Core storage can only be modified by expanded displacement.

The Displacement is automatically expanded to a 16-bit value by duplicating bit position 8 (sign bit) in the left 8 positions.

In no case is the Accumulator (A) or its Extension (Q) modified.

If T is not zero, the Index register specified is modified. The Instruction Register is incremented an additional time to cause a skip whenever the Index Register specified is zero after the operation is complete or has changed sign during the operation. Therefore, the MDX instruction with T=non-zero should be followed by a one-word instruction.

If T is zero and the MDX instruction is short (F=0), the Instruction Register is modified by the contents of the Displacement. The Instruction Register is not incremented an additional time if the Instruction Register is zero after the operation is complete. Note that the Instruction Register has no sign as such, but is treated as a 16-bit logical value.

If T is zero and the MDX instruction is long (F=1), the core storage location specified by Address is modified by the expanded Displacement. The Instruction Register is incremented an additional time if the content of the specified location is zero after the operation is complete or has changed sign during the operation. Therefore the MDX instruction with T=zero and F = non-zero should be followed by a one-word instruction.

The MDX instruction $70FF_{16}$ can be used as a dynamic wait instruction. This instruction will cause the instruction register to be modified so that this same instruction will be repeated continuously, allowing interrupts to be serviced and returning to the MDX instruction (dynamic wait). Unless an interrupt subroutine alters the stored return address, the program will return to the MDX instruction at the end of the interrupt subroutine. An exit from the dynamic wait condition can be made manually by the following procedure.

1. Change the Mode switch to Display.
2. Press console Start.
3. Change Mode switch to Run.
4. Press console Start.
5. The program starts with the instruction following the MDX instruction.

Indicators: The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representation

One-Word Instructions

70XX	ADD Expanded DISP to I (no skip can occur)
71XX	ADD Expanded DISP to XR1
72XX	ADD Expanded DISP to XR2
73XX	ADD Expanded DISP to XR3

Two-Word Instruction, Bit 8 is 0

74XXXXXX	Add Expanded Positive DISP to CSL at Addr (Add to memory)
7500XXXX	Add Addr to XR1
7600XXXX	Add Addr to XR2
7700XXXX	Add Addr to XR3

Two-Word Instruction, BIT 8 is 1

74XXXXXX	Add Expanded negative DISP to CSL at Addr (Add to Memory)
7580XXXX	Add V in CSL at Addr to XR1
7680XXXX	Add V in CSL at Addr to XR2
7780XXXX	Add V in CSL at Addr to XR3

WAIT (WAIT)
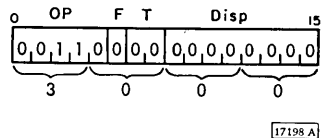
Description: This instruction is a one word format instruction only. The P-C stops in a wait condition. It can be restarted manually or by detection of an interrupt. Following completion of an interrupt subroutine, the instruction immediately following the Wait instruction is executed if the Branch Out of Interrupt (BOSC) is the normal indirect subroutine linkage. Data channel or Timer operations continue during the wait condition.

Another method of accomplishing the WAIT function is described under the heading Modify Index And Skip (MDX).

Indicators: The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representation

One-Word Instruction (only)

30000 WAIT until manual start or until completion of an interrupt subroutine

COMPARE (CMP)

35
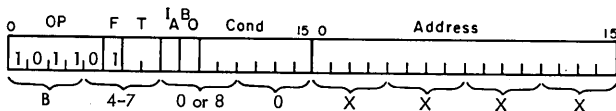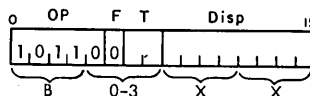
Description: The contents of the Accumulator (A) are algebraically compared against the contents of the word at the effective address, and the Instruction Register (I) is modified according to the result of the comparison as shown below:

   if A > C(EA)   then I = I
   if A < C(EA)   then I = I + 1
   If A = C(EA)   then I = I + 2

The contents of A and Q and core storage are unchanged at the end of the instruction execution.

Indicators: The Overflow indicator is unaffected by this instruction. The Carry indicator may be altered.

Hexadecimal Representation

One-Word Instruction

B0XX	Compare A with contents of CSL at EA (I+DISP)
B1XX	Compare A with contents of CSL at EA (XR1+DISP)
B2XX	Compare A with contents of CSL at EA (XR2+DISP)
B3XX	Compare A with contents of CSL at EA (XR3+DISP)

Two-Word Instruction, Direct Addressing

B400XXXX	Compare A with contents of CSL at EA (Addr)
B500XXXX	Compare A with contents of CSL at EA (Addr+XR1)
B600XXXX	Compare A with contents of CSL at EA (Addr+XR2)
B700XXXX	Compare A with contents of CSL at EA (Addr+XR3)

Two-Word Instruction, Indirect Addressing

B480XXXX	Compare A with contents of CSL at EA (V in CSL at Addr)
B580XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR1")
B680XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR2")
B780XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR3")

DOUBLE COMPARE (DCM)
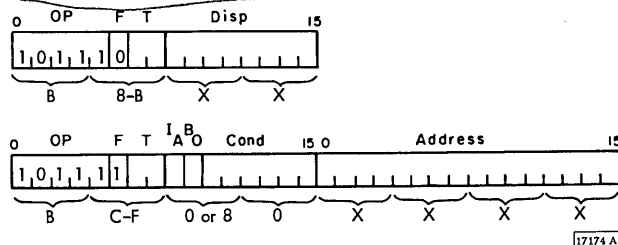
Description: The contents of the Accumulator (A) and its Extension (Q) are compared against the contents of the effective address (EA Must be an Even address) and the effective address plus one (Odd). The Instruction Register (I) is modified as follows:

   if A, Q > C(EA), C(EA + 1), then I = I
   if A, Q < C(EA), C(EA + 1), then I = I + 1
   if A, Q = C(EA), C(EA + 1), then I = I + 2

Indicators: The Overflow indicator is unaffected by this instruction. The Carry indicator may be altered.

Hexadecimal Representation

One-Word Instruction

B8XX	Compare A and Q with contents of CSL at EA (I+DISP) and EA+1
B9XX	Compare A and Q with contents of CSL at EA (XR1+DISP) and EA+1
BAXX	Compare A and Q with contents of CSL at EA (XR2+DISP) and EA+1
BBXX	Compare A and Q with contents of CSL at EA (XR3+DISP) and EA+1

Two-Word Instruction, Direct Addressing

BC00XXXX	Compare A and Q with contents of CSL at EA (Addr) and EA+1
BD00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR1) and EA+1
BE00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR2) and EA+1
BF00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR3) and EA+1

Two-Word Instruction, Indirect Addressing

BC80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at Addr) and EA+1
BD80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr +XR1") and EA+1
BE80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1
BF80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1

EXECUTE I/O (XIO)

```
  0  OP   F T    Disp      15
 |0,0,0,0,1|0| |  ,  ,  ,  |
     \__/  \_/   \_/  \_/
      0    8-B    X    X
```

```
  0  OP   F T I A B O  Cond  15  0       Address        15
 |0,0,0,0,1|1| | | |  ,  ,  |   |  ,  ,  ,  ,  ,  ,  ,  |
     \__/  \___/  \_/  \_/       \_/  \_/  \_/  \_/
      0    C-F   0 or 8  0        X    X    X    X
```

[17199 A]
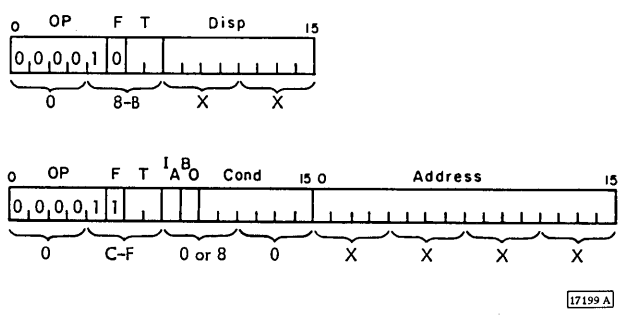
Description: This instruction is used for all I/O operations; it may be either one or two words in length, as specified by the F-bit. In the two-word instruction, the Address is either a direct or indirect address, as specified by the IA bit. For proper operation, the Effective Address must be an even address. The Effective Address is used to select a two-word I/O Control Command (IOCC) from storage.

Internal, Trace, CE, and External interrupts are suppressed for the first instruction following an XIO instruction. Therefore, the mask register (See Interrupt section) may be set without the possibility of an interrupt.

Hexadecimal Representation

One-Word Instruction

08XX Execute IOCC in CSL at EA (I+DISP) and EA+1

09XX Execute IOCC in CSL at EA (XR1+DISP) and EA+1

0AXX Execute IOCC in CSL at EA (XR2+DISP) and EA+1

0BXX Execute IOCC in CSL at EA (XR3+DISP) and EA + 1

Two-Word Instruction, Direct Addressing

0C00XXXX Execute IOCC in CSL at EA (Addr) and EA+1

0D00XXXX Execute IOCC in CSL at EA (Addr+XR1) and EA+1

0E00XXXX Execute IOCC in CSL at EA (Addr+XR2) and EA+1

0F00XXXX Execute IOCC in CSL at EA (Addr+XR3) and EA+1

Two-Word Instruction, Indirect Addressing

0C80XXXX Execute IOCC in CSL at EA (V in CSL at Addr) and EA+1

0D80XXXX Execute IOCC in CSL at EA (V in CSL at "Addr+XR1") and EA+1

0E80XXXX Execute IOCC in CSL at EA (V in CSL at "Addr+XR2") and EA+1

0F80XXXX Execute IOCC in CSL at EA (V in CSL at "Addr+XR3") and EA+1

The IOCC specifies the I/O operation, I/O device, and core storage address. The format of the two-word IOCC follows, with an explanation of the assigned fields:

```
 0                  15 0   4 5  7 8        15
 |  Address          |  Area | Fun | Modifier |
 _____/          _____/
 IOCC     at EA              at EA + 1   [17 200]
      (even location)
```
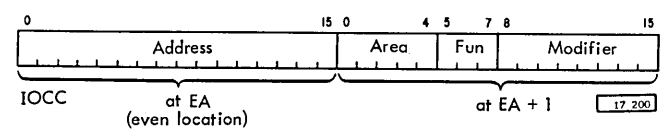
Area

This 5-bit field specifies a unique segment of I/O which may be a single device (1442 Card Read-Punch, 1443 Printer, etc.) or a group of several units (magnetic tape drives, serial I/O units, contact sense units, etc.). (See Appendix D.)

Area 00000 is used to address such devices as the Console and the Interrupt Mask Register. (See Area Code Zero following XIO Data Flow.)

Function

The primary I/O functions are specified by the 3-bit function code of the IOCC:

000 – This code is used to remove an I/O device from on-line status and place it in CE mode. It can also be used to restore the on-line status and remove the I/O device from CE mode.

001 – Write
This code is used to transfer a single word from storage to an I/O unit. The address of the storage location is provided by the Address field of the I/O Control Command.

010 – Read

This code is used to transfer a single word from an I/O unit to storage. The address of the storage location is provided by the Address field of the I/O Control Command.

011 – Sense Interrupt Level

This code directs the I/O devices requesting interrupt recognition to make their status available in the Accumulator as the Interrupt Level Status word. (See Interrupt section.)

100 – Control

This code causes the selected device to interpret the Address word or modifier of the IOCC as a specific control action. (See Area Code Zero following XIO Data Flow.)

101 – Initialize Write

This code initiates a WRITE operation on a device or unit which will subsequently make data transfers from storage via a Data Channel.

110 – Initialize Read

This code initiates a READ operation from a device or unit which will subsequently make data transfers to storage via a Data Channel.

111 – Sense Device

This code causes the selected device to make its current status available in the Accumulator as the Device Status Word or Process Interrupt Status Word (PISW).

If Area 00000 is specified, the Console status or Interval Timer status may be brought into the Accumulator as specified by a unit address code in the Modifier field.

Programming Note: The current contents of the Accumulator are destroyed by the execution of Sense Interrupt Level, Sense Device, Initialize Read, Initialize Write, Read, or Write. Therefore, it is the programmer's responsibility to save the Accumulator contents if necessary.

Modifier

This 8-bit field provides additional detail for either Function or Area. For example, if the Area specifies a Disk Storage Drive, and if the Function specifies Control (100) then a particular modifier code specifies the direction of the Seek operation. In this case, the Modifier serves to extend the Function.

If, however, the Area specifies a group of serial I/O devices, and if the Function specifies Write (001), then the particular unit address is specified by the Modifier. (See Appendix D.)

Address

The meaning prescribed for this 16-bit field is dependent upon the Function specified by this I/O Control Command:

1. If Function = Initialize Write (101) or if Function = Initialize Read (110), then Address specifies the starting address of a table in storage (an I/O block). The contents of this table are data words and control information.
2. If Function = Control (100) and if, for example, Area specifies the 1443 Printer, the Address may specify a specific control action.
3. If Function = Sense (011) or (111), the Address field is ignored. Instead, an increment of time equivalent to a memory cycle is taken, during which the selected I/O device or Interrupt Level places its status word in the Accumulator.
4. If Function = Write (001) or if Function = Read (010), the Address specifies the storage location of the data word.

XIO Execution Data Flow

The circled numbers in Figure 7 correlate with the data flow sequence that follows:

1. The EA of the XIO is developed in the Accumulator (A) and routed to the Storage Address Register (SAR) to locate the IOCC.
2. Bit position 15 of SAR is forced on to select the EA + 1 where the IOCC Area, Function, and Modifier are found.
3. The Area, Function, and Modifier are routed through the B-register to the Out-Bus to the I/O Adapter of the device specified by the Area.
4. Bit position 15 of SAR is turned off to allow the Address portion of the IOCC word to be transferred, from the core-storage location specified by the Effective Address (EA), to the B-register.
5. If the Function is an Initialize Read, Initialize Write, or Control, the Address part of the IOCC is routed through the B-register to the Out-Bus. The address part of the Initialize Read/Write IOCC goes to the Channel Address Register (CAR) of the Data Channel. If the Function is Read or Write, the Address is routed from the B-register through the A-register to the SAR. SAR addresses the storage location to or from which data is transmitted.
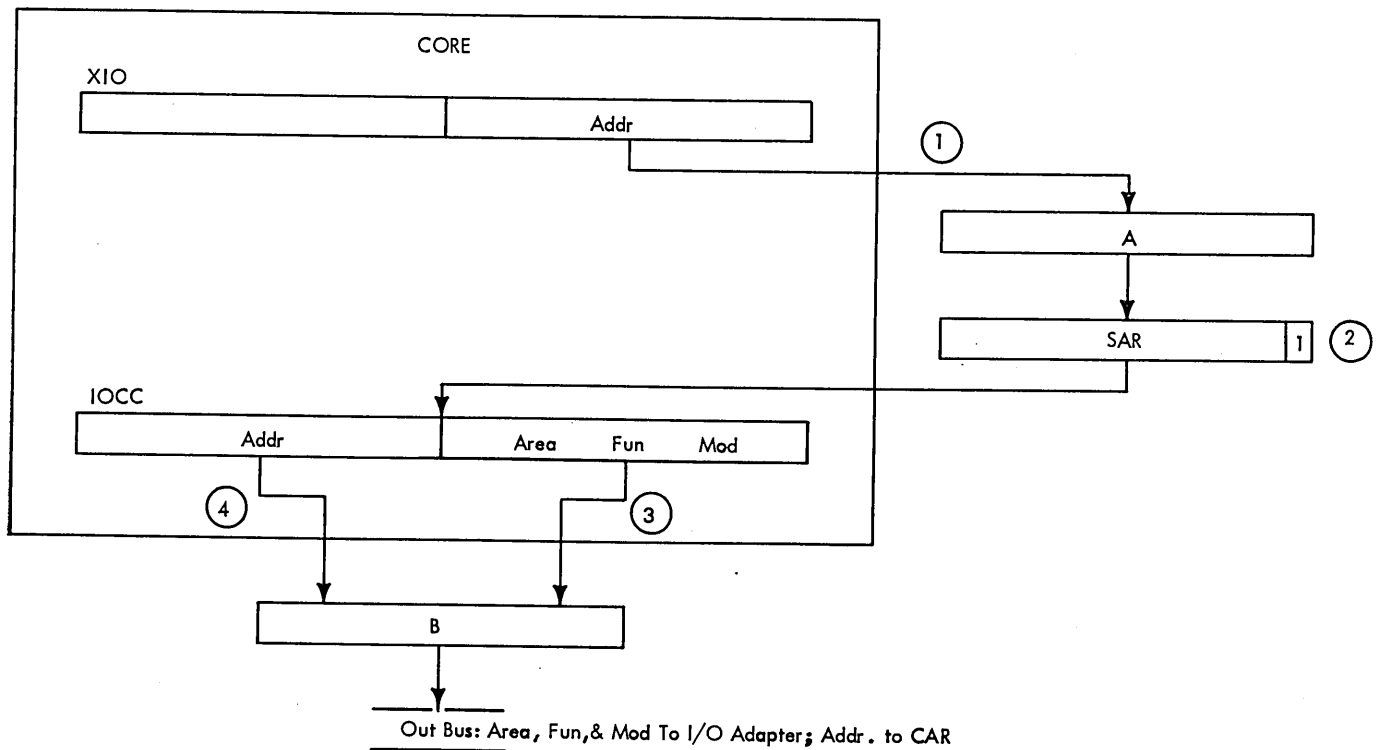
Figure 7. XIO Data Flow

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AREA CODE ZERO

The IOCC Area code 00000 is used with Modifier bits 8-10 to specify the particular feature or register listed below. These bits are fixed for all 1800 systems:

Feature/Register	Bits 8-10
Interval Timers	001
Console Data Entry Switches	010
Console Sense and Program Select Switches, and CE Switches	011
Interrupt Mask Register	100
Programmed Interrupt	101
Console Interrupt	110
Operations Monitor	111

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The IOCC for each operation follows. Note that the Function specifies the operation. Those bit positions left blank are not used.

Interval Timers

This IOCC is used to start or stop the interval timers. See Interval Timers section.
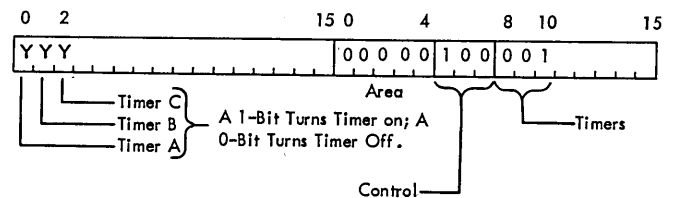
17399

Console Data Entry Switches
Console Sense and Program Switches

The following IOCC's are used to read the console switches into the accumulator or core storage.

17400

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Diagram 17401 A — Core Storage Address | 0 0 0 0 0 | 0 1 0 | 0 1 0
- Area
- Read
- Data Entry Switches: The status of these switches is read into Core Storage (Bit Positions 0-15)

Diagram 17402 A — Not Used | 0 0 0 0 0 | 1 1 1 | 0 1 1
- Area
- Sense Device
- CE Switches: The status of these switches is read into Accumulator Bit Positions 8-15
- Sense and Program Switches: The status of these switches is read into the Accumulator Bit Positions 0-7

Diagram 17403 A — Core Storage Address | 0 0 0 0 0 | 0 1 0 | 0 1 1
- Area
- Read
- Sense And Program Switches: The status of these switches is read into Core Storage (Bit Positions 0-7)
- C E Switches: The status of these switches is read into Core Storage Bit Positions 8-15.

Interrupt Mask Register

This IOCC is used to mask or unmask customer interrupt levels 0-23. Internal check level, Trace, and CE interrupts cannot be masked.

Diagram 17404 — Y Y Y Y Y Y Y Y Y Y Y Y Y Y | 0 0 0 0 0 | 1 0 0 | 1 0 0 | Z
- Z=1 (positions 0-13), Z=0 (positions 0-9)
- Area
- Control
- Interrupt Mask Register
- 0-Interrupt Levels 0-13
- 1-Interrupt Levels 14-23
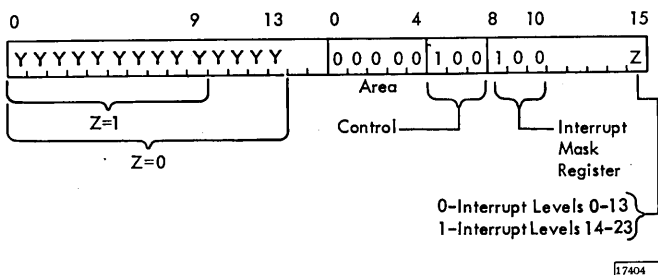
Y - The status of bit positions 0-13 or 0-9, depending on Z, is copied into bit positions 0-13 or 14-23 of the 24-bit Interrupt Mask register.

A 1-bit turns the corresponding Mask register bit on. This bit prevents the external interrupt on that particular level from being acknowledged until the mask is changed to unmask. A 1-bit prevents a Programmed Interrupt for its corresponding interrupt level.

A 0-bit causes the Mask register bit to be set off, which enables the particular interrupt level.
The execution of this instruction does not destroy the contents of the accumulator.

NOTE: Pressing the Console Reset key masks interrupt levels 0-23.

Programmed Interrupt

This IOCC is used to initiate an interrupt (or interrupts) from within the program. Programmed interrupts do not turn on bits in the ILSW. See Interrupt section for details of programmed interrupt.

Diagram 17405 — Y Y Y Y Y Y Y Y Y Y Y Y Y Y | 0 0 0 0 0 | 1 0 0 | 1 0 1 | Z
- Z=1 (positions 0-13), Z=0 (positions 0-9)
- Area
- Control
- Programmed Interrupt
- 0-Interrupt Levels 0-13
- 1-Interrupt Levels 14-23
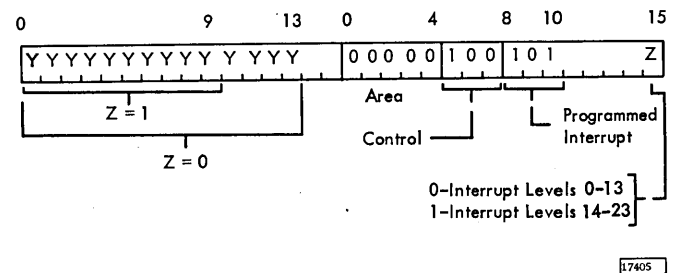
Y - A 1-bit in positions 0-13 or 0-9, depending on Z, turns on corresponding interrupt level 0-13 or 14-23 unless this level is masked or becomes masked prior to the forced BSI due to this instruction.

Console Interrupt

This IOCC is used to read the Console Interrupt Device Status Word (DSW) into the accumulator.

Diagram 17406 A — Not Used | 0 0 0 0 0 | 1 1 1 | 1 1 0 | Z
- Area
- Sense Device
- Console Interrupt
- 0-Do not reset DSW indicator
- 1-Reset DSW (Device Status Word) Indicator.

```
0                          15
1 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0
```
DSW for Console Interrupt   [29063]
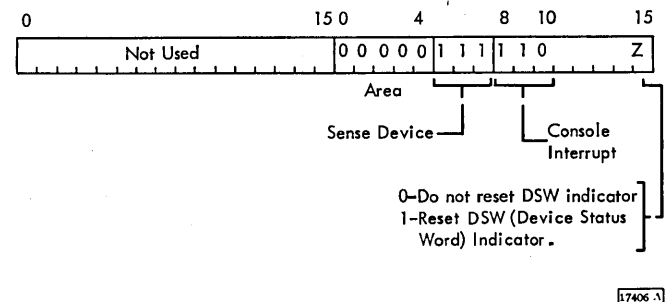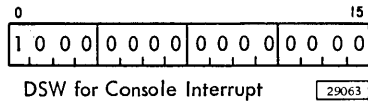
Operations Monitor

This IOCC is normally used to reset the Operations Monitor timer, thereby preventing its time-out and the resulting alarm that would otherwise occur. See Operation Monitor section for more detail.

```
0                        15 0      4      8  10        15
|        Not Used         | 0 0 0 0 0 | 1 0 0 | 1 1 1 |  Z |
                            Area
                            Control
                                              Operations
                                              Monitor
         0-Timer Not Reset
         1-Timer Reset to Time-Out
            Period Indicated by Switch.
```
[17407]
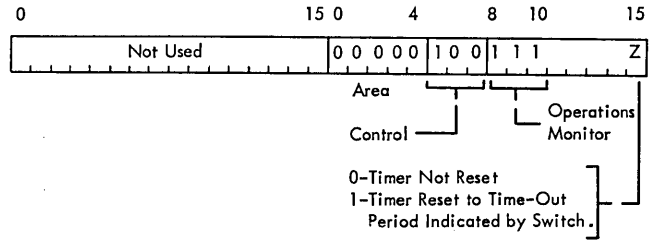
Three timers are provided to supply real-time information to the program. They are in core storage locations 0004 (timer A), 0005 (timer B), and 0006 (timer C). Each timer has a permanent time base which can be selected by the customer (Table 4). All three timers can operate at different time periods.

Table 4. Interval Timers

Core Storage Cycle Times	Available Time Bases (In Milliseconds)									
2 μsec	.125	.25	.5	1	2	4	8	16	32	64
4 μsec	.25	.5	1	2	4	8	16	32	64	128

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The timers can be started or stopped under program control. Once started, they are automatically incremented one count at a time through the cycle stealing facility of the P-C. A count is added each time the assigned time base period is completed. This count is automatic and does not require a program. The count of the timers proceeds in the positive direction. When the count reaches the largest positive value ($2^{15}-1$), the count continues to the most negative value and then through the negative numbers (two's complement) toward zero. When the count reaches zero, an interrupt is requested on the level assigned to the timers. (All three timers are on the same interrupt level which is assigned by the user.) The timer continues to operate after the zero value has been reached.

The timers, once operating, continue to record time correctly when the P-C is in the Run, Trace, or SI W/CS mode. (See Console Mode Switch section.) Further, a WAIT instruction may also be executed by the program without affecting the timers ability to record time correctly.

The timers are started by means of the XIO instruction with the Function of Control referring to Area zero. The IOCC used to start and stop the timer has the following form.

0	15	0	4	8	9	10	11	12	13	14	15
Y Y Y X X X XX X X XX X XX		0 0 0 0 0	1 0 0	0 0 1				XX X X			
Address		Area	Fun	Modifier							

17 201
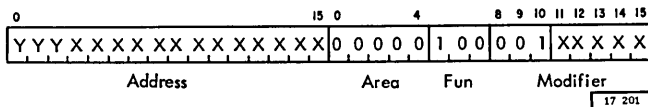
X - Unused

Y - This information is copied into the Timer Control. A one (1) causes the timer to be turned ON and a zero turns the timer OFF. Bit position 0 of the address corresponds to Timer A, Bit position 1 - Timer B, and Bit position 2 - Timer C.

Modifier 001 - Unit Address of Timers

The IOCC used to sense the DSW and reset the interrupt assigned to the timers is:

0	15	0	4	8	15
Not Used		0 0 0 0 0	1 1 1	0 0 1 X X X X Z	
		Area	Fun	Modifier	

17 202 A
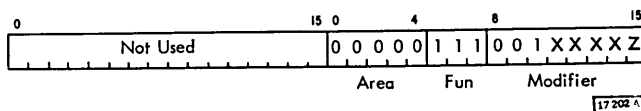
Modifier 001 - Unit Address of Timers

X - Unused

Z - A 1-bit resets the DSW indicators; a 0-bit does not reset them.

The DSW has the following bit significance:

B0	Timer A
B1	Timer B
B2	Timer C
B3-15	Not Used

The bit being ON indicates that the timer has initiated an interrupt.

NOTE: The timers continue to increment correctly if they are protected with a Storage Protect Bit. However, any other attempt by the P-C or an I/O device to alter the data in a protected timer will cause a Storage Protect Violation.

The Storage Protection facility protects the contents of specified locations of core storage from change due to the erroneous storing of information during the execution of a program. This protection is achieved by providing each location in core storage with a Storage Protect bit. The status of each storage location is identified as "read only" or "read/write" by the condition of the Storage Protect bit.

"Read only" is indicated by the bit being set to one (ON). "Read only" is defined as the ability to access a protected location, read the contents into the B-register and regenerate into the storage the contents that were read out. Under program control, any location in core storage may be designated as "read only". Since each location has its own Storage Protect bit, each location is conditioned individually by means of the Store Status instruction.

The Store Status instruction, with bit nine equal 1, is used to Write or Clear storage protect bits. See Instruction Set section for Store Status. The execution of this instruction is under control of the Write Storage Protect Bits switch on the P-C Console. When this switch is ON, the Store Status instruction can change the storage protect bits. When the Write Storage Protect Bits switch is OFF, this instruction (Store Status with bit nine equal 1) performs as a NO-OP.

Although the Storage Protect bit, the parity bit, and the 16 data bits result in an 18 bit word, only the 16-bit data word need be considered for instruction and data flow purposes. The odd parity bit covers the 16 data bits and the Storage Protect bit. Loss of any one of the 18 bits in a location is detected by a Parity Check.

Any attempt by the program to write into a "read only" protected location results in a storage protect violation which causes the Internal interrupt (highest priority interrupt). A 2-bit is placed in the Interrupt Level Status Word (ILSW) of the Internal Interrupt. The data in the protected location is not changed.

By Storage Protecting the word following the last word in input data tables, the Storage Protect bit can be employed to detect word count program errors. This can be especially beneficial during the check out of new programs. A word count in excess of the number of words available in the input table can cause the loss of data in words following the table.
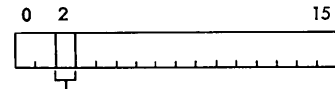
Storage Protect Violate Bit Position in ILSW for the Internal Interrupt.

17409 A

If an XIO or cycle steal operation attempts to write into a protected location, the protected data remains intact and the Storage Protect Violation indicator is set in a bit position of the Device Status Word (DSW) associated with the device operating on the Data Channel. No internal level interrupt occurs.

The Check Stop switch being ON causes the P-C to stop at the end of the core-storage cycle in which any Storage Protect Violation is detected. If the Check Stop switch is in the OFF position, a Storage Protect Violation causes the P-C to initiate an internal interrupt or set the Storage Protect Violation indicator in the appropriate DSW as described above.

The Disable Interrupt toggle switch on the P-C Console being ON prevents an internal interrupt.

Any attempt by the program to read from a core storage location having incorrect (even) parity or to write a word having incorrect parity will result in an Internal Interrupt. This includes initialization cycles (and loading CAR) of an XIO instruction. Reading from core storage takes place as an instruction is read out to be executed, as an address is read out, etc. In these circumstances a parity error will <u>not</u> prevent instruction execution. Therefore, programmed recovery may not be possible.

If a parity error causes an I/O device to reject the XIO command (Initialize Read or Write only) during the XIO control cycle, a CAR check will also occur since CAR is not selected to be loaded. If a parity error is detected during a data cycle (cycle steal) the Device Status Word of the device will have the parity error indicator set. The core storage word in error can be found by using a routine such as the following that loads data (from core) into the A Register and detects the error at the time the internal interrupt occurs. A parity error during a data cycle resulting from an XIO instruction, does <u>not</u> cause an Internal interrupt. This parity error results in setting the parity indicator in the Device Status Word (DSW) for the I/O device being used. It is the responsibility of the program operating that

```
          .              .
          .              .
          .              .
       LDX    L1     INTRP         Setup Interrupt Branch Address
       STX    L1     8
       LDX    L1     +32,767       XR1=Core Storage Size
LOOP   LD     1      0
       MDX    1      -1
       MDX           LOOP
          .              .
          .              .
          .              .
INTRP  DC            0             Internal Interrupt Branch
          .              .                XR1=Address of Error Word
          .              .
          .              .
       BOSC   I      INTRP         Check Next Word
```

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device to initiate retries or other error recovery procedures.

The Check Stop switch being ON causes the P-C to stop at the end of the core-storage cycle in which any Parity error is detected. If the Check Stop switch is in the OFF position, a Parity error causes the P-C to initiate an internal interrupt or set the Parity indicator in the appropriate DSW as described above.

The Disable Interrupt toggle switch being ON prevents an internal interrupt.

OPERATIONS MONITOR

This basic feature of the 1800 System can be used to check program operation. If the 1800 P-C fails to execute a predetermined sequence of instructions, within a pre-selected time interval, an alarm circuit is activated. The alarm may be audible and/or visual (an indicator light is located at the 1800 console). Both the alarming device and the power required to operate it must be furnished by the customer. (Customer power is limited to 30 volts and 1 ampere.)

The Operations Monitor includes an internal timer and manual controls on the 1800 console. The operator may select any one of six time intervals: 5, 10, 15, 20, 25, or 30 seconds. (The selection switch is located on the CE panel underneath the console.) Once the Operations Monitor has been activated by the operator, a reset Monitor timer command must be executed during program operation at intervals frequent enough to prevent the timer from timing out. If the reset command is not given during the selected time interval, the timer runs out and the alarm circuit is activated. Once the Operations Monitor alarm is on, it cannot be reset off by the P-C program executing a XIO control instruction; reset can only be accomplished by manually turning the Operations Monitor toggle switch off. The cause of the timeout should be identified before the switch is turned back on. Timeout can also be caused by a power failure, computer hang-up, computer looping, or any departure from the predicted instruction sequence in the program.

Programming Note

The use of the Operations Monitor depends on the positions of two switches:

1. The time interval selection switch on the CE panel.
2. The Operations Monitor on-off toggle switch on the P-C console. The first time interval is initiated when this switch is turned on.

With these two switches correctly positioned and the P-C in programmed operation, the Operations Monitor timer must be reset at intervals frequent enough to prevent it from timing out and causing an alarm. An XIO instruction with the IOCC described below is used to reset the timer:
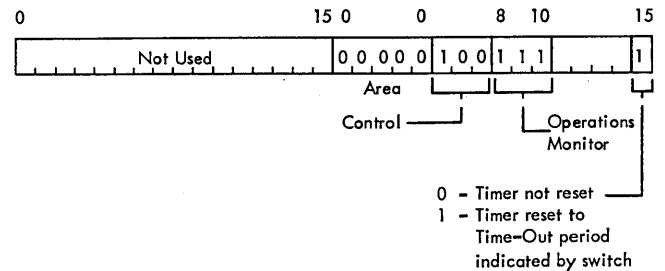
POWER FAILURE PROTECT

In the event of an emergency power failure, circuitry is provided which permits the P-C to complete execution of the instruction in progress prior to termination of program control. The program is automatically terminated and the system reset at the completion of the cycle in progress.

The P-C console (Figure 8) provides the means for manual control of the Processor-Controller during debugging or operating phases.

The basic operating features and controls provide the facility to:

1. Start or stop instruction execution.
2. Address memory.
3. Set-up and store data or instructions.
4. Communicate with the program via Sense or Program Select switches.
5. Control the cycling rate in the Run, Single Memory Cycle, Single Instruction, or Single Stop modes.
6. Interrupt the program manually.
7. Trace each instruction.
8. Reset all control circuitry and storage.
9. Turn power on and off.
10. Indicate basic machine conditions and status.
11. Display memory words and register data.
12. Write or clear storage protect bits.
13. Clear core storage.

PUSH-BUTTON SWITCHES AND LIGHTS

There are two rows of push-button switches and lights. One row is at the top of the console (Figure 9) and one row is at the bottom (Figure 10). Descriptions of their functions follow:

Clear Storage

This push-button (P.B.) switch has four functions (Table 5). None of the four functions can be executed, however, until Clear Storage is first held pressed and then Start is pressed. This dual action requirement prevents the accidental clearing of storage. Note in Table 5 that each Clear Storage function is dependent on the positions of two console switches, the rotary Mode switch and the Write Storage Protect Bits (WSPB) toggle switch.

The P-C cycles completely through all core storage addresses during the execution of each Clear Storage function.

Program Load

The program load push-button switch (Figure 8) is used to load the first 1442 card or 1054 tape record into core storage. The Reset push-button switch must be pressed prior to pressing the program load switch. The input device must be in a "ready" condition. The first card or tape record loaded must contain instructions that will initiate loading the remainder of the cards or tape records. (P-C must be in Run Mode for program operation.) Only one input device can be used for Initial Program Load. The first 1442 on the system will be used for Initial Program Load (IPL). The 1054 is used for IPL when there is no 1442 on the system.

The program load operation does not alter the status of the interrupt mask register.

When the 1442 is used for Initial Program Load, it operates in Packed Mode, reading the 80 columns of the first card into core-storage locations 0000-0039 (0000_{16} - 0027_{16}). Each core-storage location stores the binary data from two card columns. For example, binary data from card column 1 (Rows 12-5) is read into core-storage location 0000 (bit positions 8-15) and binary data from card column 2 (rows 12-5) is read into the same core-storage location (bit positions 0-7). Rows 6-9 of the card are not read into core storage. The remainder of the first card is entered in the same manner, entering all odd numbered card columns in bit positions 8-15 of their respective core-storage location, and entering all even numbered card columns in bit positions 0-7 of their respective core-storage location.

After the first card is read into core storage, the P-C begins (at 0000) executing the instructions that were stored in core storage from the first card. The first card must contain instructions to load the remainder of the program cards.

When the 1054 Paper Tape Reader is used for Initial Program Load, tape data is loaded into core storage, starting at location 0000 and loading successively higher core-storage locations until an end-of-record punch is sensed in the tape. Each core-storage location stores the binary data from four tape characters. For example, binary data from the first tape character (channels 1-4) is stored in core-storage location 0000 (bit positions 0-3, ... , binary data from the fourth tape character (channels 1-4) is stored in core-storage location 0000 (bit positions 12-15). The remainder of the tape data is entered in the same manner (four characters per word) until a channel 5 punch is sensed. (Any channel 5 punch except when it is in a delete character.) The channel 5 punch is the end-of-record character and is not read into core storage.

IBM® 1800 DATA ACQUISITION AND CONTROL SYSTEM

| CLEAR STOR | PROG LOAD | READY | ON | OFF | POWER ON | LAMP TEST | WAIT | RUN | ALARM | | EMERGENCY PULL |

ARITH CTL   **SHIFT CTL**   **ADD**   **ARITH SIGN**   **ZERO REM**   **BRANCH**   **STOR PROT BIT**   **PTY BIT**

INTR SERV   **CS SERV**   **AUX STOR**   **OP CODE CHECK**   **STOR PROT CHECK**   **PTY CHECK**

CLOCK 0 1 2 3 4 5 6 7   **CYCLE** I1 I2 IA E EI   **TIMERS** A B C

INTERRUPT LEVELS 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
16 17 18 19 20 21 22 23   CHECK   TRACE   CE

OP CODE 0 1 2 3 4 **F** 5 **TAG** 6 7 **1A** 8 **BO** 9 10 11 12 13 **CAR** 14 **OFLO** 15

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ADDRESS REGISTER															
I REGISTER															

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
B REGISTER																
D REGISTER																
A REGISTER																
DATA REGISTER																

DISPLAY ADDRESS REGISTER SAR / CAR 0 / CAR 1 / CAR 2 / CAR 3 / CAR 4 / CAR 5 / CAR 6 / CAR 7 / CAR 8

DISPLAY DATA REGISTER XR2 / XR3 / XR1 / SC / Q

SENSE 0 1 2 3   **PROGRAM** 4 5 6 7   **OPERATIONS MONITOR** ON/OFF   **DISABLE INTERRUPT** ON/OFF   **CHECK STOP** ON/OFF   **WRITE STOR PROT BITS** YES/NO

DATA ENTRY SWITCHES 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

MODE SW RUN / TRACE / LOAD / DISPLAY / SI W/CS / SI / SSC / SS

| CONSOLE INTR | | LOAD 1 | | RESET | | IMMED STOP | | START | STOP |

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Figure 8. P-C Console

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CLEAR STOR | PROG LOAD | READY | ON | OFF | POWER ON | LAMP TEST | WAIT | RUN | ALARM | EMERGENCY PULL

RED P.B.   BLUE P.B.   GREEN LENS GREEN P.B.   RED P.B.   WHITE LENS WHITE P.B.   WHITE LENS GREEN LENS RED LENS

Figure 9.   Console Lights and Switches, Top Row

The 1054 interrupt requests are suppressed while in IPL mode.

Delete characters are characters containing punches in channels 1-7 and are not read into core storage while in IPL mode.

Channels 5-8 of the paper tape are not loaded into core storage during Initial Program Load.

The P-C then begins (at 0000) executing the instructions stored in core storage from the first tape record. If the entire program was not included in the first tape record, the first record must contain instructions for loading the remainder of the tape records (program).

Ready

This light is on when the P-C is in an operative condition.

Off

This push-button switches is used to shut down the power supplies within the P-C.

On

This push-button switch is used to turn on the power supplies within the P-C.

Power On

This light is used to indicate that the P-C power supplies are operative.

Lamp Test

This push-button switch is pressed to apply lamp voltage to all console lamps. Its use is to verify operation of all console lamps.

Wait

This light is used to indicate that the P-C: is in either Load or Display Mode; has been halted by a Wait Instruction; has been halted by the operator pushing the Stop or Immediate Stop switch.

Run

This light is used to indicate that the P-C is operating under program control.

Alarm

This light is used to indicate that the Operation Monitor has timed out. The customer may install an audible alarm to operate in conjunction with the Alarm light. See Operation Monitor section.

EMERGENCY PULL SWITCH

This pull-switch is for emergency use only. If pulled off, all electrical power within the 1801/1802 is turned off, including power to the blowers that cool the electronic circuitry. Turning the blowers off in this manner may damage some of the circuitry. This switch must be reset by an IBM Customer Engineer.

Console Interrupt

This push-button switch enables the operator to interrupt P-C operation. The console interrupt level is assigned by the customer. The Program toggle switches may be used in conjunction with Console Interrupt to specify the console interrupt routine. However, this relationship between the Program switches and Console Interrupt would exist only by virtue of the program. There is no internal relationship between the two.

The Console Interrupt IOCC is provided in the Area Code Zero section of the description for the Execute I/O instruction.

CONSOLE INTR | | LOAD I | | RESET | | IMMED STOP | | START | STOP

BLUE P.B.   BLUE P.B.   BLUE P.B.   RED P.B.   GREEN P.B. RED P.B.
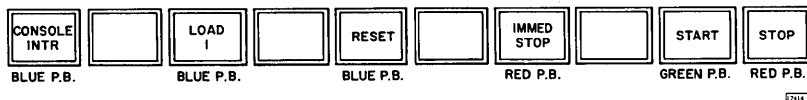
Figure 10.   Console Lights and Switches, Bottom Row

Table 5. Clear Storage Functions

Function	Mode Switch	WSPB Switch
1. Store Contents of Data Entry Switches in all Core Storage Locations. Storage-Protect Bits are Removed and Parity is Corrected as Required Because of Bit Removal. If All Data Entry Switches Are Off, Only Parity Bits are Left in Storage.	Run	On
2. Store Contents of Data Entry Switches in Each Core Storage Location that is Unprotected. Locations having Protect Bits are Unchanged.	Run	Off
3. Clear Storage Protect Bits. All Other Data Remains Unchanged. Parity is Automatically Corrected in Each Word in Storage.	Display	On
4. Search for Parity Errors. The P-C Cycles Through Storage Until Stopped by the Stop Key or a Parity Error. The Check Stop Switch Must be on for a Parity Error to Cause a Stop.	Display	Off

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Load I

This push-button switch is used with the rotary Mode switch in the Load position to transfer the contents of the Data Entry toggle switches into the I-register of the P-C. The P-C is in the stopped condition when it terminates the Load I operation.

Reset

This push-button switch is used to reset all basic timing, controls, registers (except Index Registers and Address Registers), and I/O devices. The interrupt mask register is reset with all bits "on". The Digital Input and Digital-Analog Output registers are not reset.

Immediate Stop

This push-button switch stops the P-C at the end of the 2 or 4 μsec core-storage cycle in operation when the immediate Stop contacts close.

All basic timing, controls, registers (except Index Registers and Address Registers), and I/O devices are reset. The Immediate Stop switch can also be used to stop data channel (cycle stealing) operations that are no longer under program control.

Stop

This push-button switch stops the P-C without resetting the P-C registers or I/O devices, at the end of the instruction in operation when the stop contacts close. Data channel operations can be stopped only by pressing Immediate Stop.

If, at the same time the stop key is pressed, an interrupt occurs that can force a BSI (i.e., on an unmasked level higher than any in progress), the stop key must be pressed again to be effective. Pressing of the start key causes the program to resume operation.

Start

This push-button switch initiates P-C operations, if the Ready light is on, as specified by the Rotary Mode switch.

Mode Switch

This eight-position rotary switch (Figure 11) is used with the Start switch to extend operator control of the P-C.

Single Instruction with Cycle Steal (SI W/CS): A Start switch depression with the Mode switch on SI W/CS causes the execution of one instruction. Data channel operations can occur during execution of the instruction.

Single Instruction (SI): A Start switch depression with the Mode switch on SI causes the execution of one instruction. Data Channel operations are prevented.

Single Storage Cycle (SSC): A Start switch depression with the Mode switch on SSC causes one memory cycle (2 μsec or 4 μsec). Single Storage Cycle operations (usually called Single Cycle operations) can be used in conjunction with the console Cycle lights to step through instructions and analyze P-C operation.

Single Step (SS): A Start switch depression with the Mode switch on SS causes one basic P-C clock cycle. (See console Clock Lights.)

Run: A Start switch depression with the Mode switch on Run initiates normal program operation of the P-C.
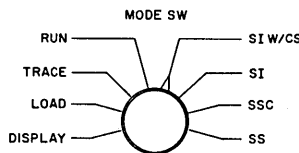
Figure 11. Console Mode Switch

Trace: This position of the Mode switch causes a Trace interrupt after the execution of each instruction. The Trace interrupt is a unique interrupt. It has no device status word, no interrupt level status word, and cannot be masked. The Trace interrupt is the lowest priority customer interrupt. Once initiated, it is delayed by the occurrence of any other interrupt. It cannot occur while other interrupts are being serviced. When the Trace interrupt occurs, the P-C executes the forced BSI and branches to the routine whose address is stored at 009. (See Interrupt section).

Load: A Start switch depression with the Mode switch on Load causes the contents of the Data Entry Switches to be stored at the address specified by the I-register. (The P-C must be in a stopped condition.) The I-register is incremented following each Load operation caused by pressing Start.

A Load I switch depression with the Mode Switch on Load causes the contents of the Data Entry switches to be stored in the I-register of the P-C.

Display: A Start switch depression with the Mode switch on Display causes the data at the I-register address to be displayed in the console B-register lights. The I-register is incremented after each display. Successive words are displayed with successive depressions of Start.

TOGGLE SWITCHES

See Figure 12.

Sense and Program

The contents of these eight switches may be stored in bit positions 0-7 of the A-register or a core storage location. An XIO instruction with an IOCC function of Read stores the contents of the Sense and Program switches at the core storage address specified by the IOCC. (See Area Code Zero in the description of the XIO instruction.) A function of Sense Device stores the switch data in the A-register.

Operations Monitor

This switch is used to start the Operations Monitor. The off position disables the Monitor.

Disable Interrupt

This switch is used to mask all interrupt levels, including Internal errors. It is especially useful during program analysis when the operator wants to choose the time at which the program may be interrupted. The highest level interrupt on and unmasked is serviced when the switch is turned off.

Check Stop

The switch is used to stop the P-C when one of the following errors occurs: invalid operation, parity error or storage protect error. The stop occurs at the end of the 2 or 4 microsecond core-storage cycle in which the error is detected. The appropriate error light will be on. Start must be pressed to restart the system.

An internal error initiates an Internal interrupt when Check Stop is OFF.

The Channel Address Register (CAR) Check internal level error is an exception to the above description of the Check Stop operation. A CAR Check error will initiate an internal level interrupt regardless of the position (ON or OFF) of the Check Stop switch.

A Clear Storage function is stopped when Check Stop is on and a parity error is detected (Table 5).

Write Storage Protect Bits

This switch enables the writing or clearing of storage protect bits. (See Store Status instruction and Clear Storage functions, Table 5). A parity error may occur if the position of this switch is changed while the P-C is running.

Data Entry Switches

The contents of these 16 toggle switches can be stored by either manual or program control. See Area Code Zero in the description of the XIO instruction for program control. The description of the Load position under Mode Switch describes manual control.
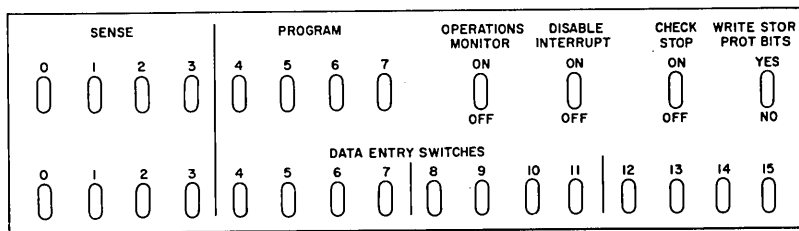
Figure 12. Console Toggle Switches
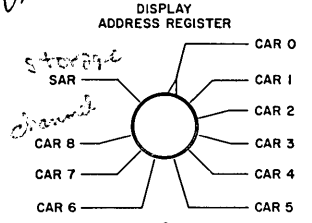
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ARITH CTL   SHIFT CTL   ADD   ARITH SIGN   ZERO REM   BRANCH   STOR PROT BIT   PTY BIT

INTR SERV   CS SERV   AUX STOR   OP CODE CHECK   STOR PROT CHECK   PTY CHECK

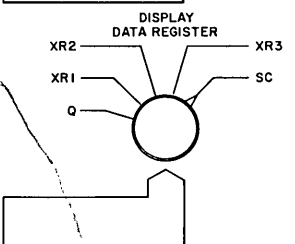CLOCK   0 1 2 3 4 5 6 7   CYCLE   I1 I2 IA E E1   TIMERS   A B C

INTERRUPT LEVELS   0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

16 17 18 19 20 21 22 23   CHECK   TRACE   CE

OP CODE   0 1 2 3 4   F 5   TAG 6 7   IA 8   BO 9   10 11 12 13   CAR 14   OFLO 15
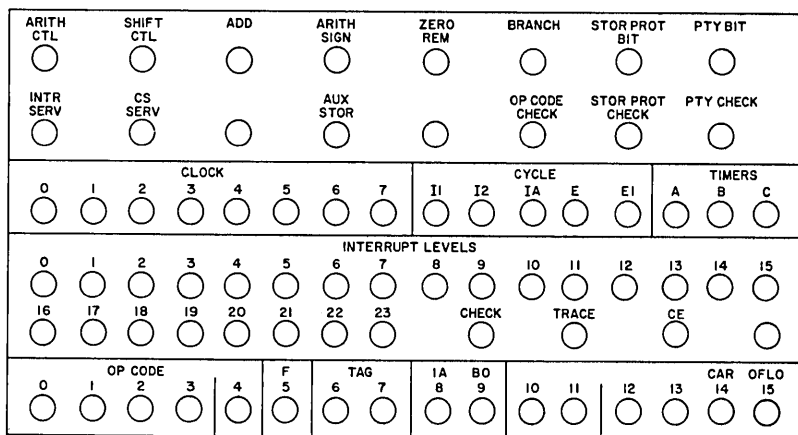
Figure 13. Console Indicators

CONSOLE INDICATORS

These indicators (Figure 13) show the status of various P-C functions and operations.

Arithmetic Control: On during arithmetic operations.

Shift Control: On during shift operations.

Add: On during add operations.

Arithmetic Sign: On when bit position zero in the A-register (accumulator) does not initially equal bit position zero in the B-register.

Storage Protect Check: Turned on when an attempt is made to write into a "read-only" location.

The Storage Protect Check Console indicator is turned off and the Check Console indicator is turned on when the next core storage cycle is initiated, allowing the storage protect indicator to indicate any subsequent storage protect error. (See Storage Protect section.)

Parity Check: Turned on when a parity error (even number of bits) is detected in the 18-bit word transfer between the B-register and core storage. The presence or absence of storage protect and parity bits in each word is indicated by their respective console indicators.

The Parity Check console indicator is turned off and the Check Console indicator is turned on when the next core storage cycle is initiated, allowing the parity indicator to indicate any subsequent parity error. (See Parity section.)

Zero Remainder: On when the A-register contains a zero balance during a divide instruction.

Branch: On during branch instructions.

Interrupt Service: Turned on when the hardware BSI instruction is being executed for the highest level interrupt that is on and not masked.

Cycle Steal Service: On during cycle steal operations for the highest priority data channel requiring service.

Op Code Check: On when an invalid Op code is placed in the Op register. The Op Code Check console indicator is turned off and the check console indicator is turned on when the next core-storage cycle is initiated, allowing the Op Code Check indicator to indicate any subsequent error.

The Op Code Check error causes an internal interrupt if the Disable Interrupt switch is off and causes a check stop if the Check Stop switch is on.

Auxiliary Storage: Auxiliary storage (256 words) is provided for IBM Field Engineering use. The indicator is on when auxiliary storage is being used.

Storage Protect Bit: On when a storage protect bit is transferred with the 16 data bits between the B-register and core storage.

Parity Bit: On when a parity bit is transferred with the 16 data bits between the B-register and core storage.

Clock

These eight indicators (0-7) show the advance of the basic P-C clock during Start key depressions when the rotary Mode switch is on Single Step (SS). Normally, eight start key depressions with the Mode switch on SS is equivalent to one Start key depression with the Mode switch on Single Storage Cycle (SSC).

Cycle

These five indicators (I1, I2, IA, E, and E1) show the progress of an instruction that is being Single Stepped or Single Storage Cycled; that is, advanced by successive Start key depressions with the rotary Mode switch on SSC or SS.

I1   shows that a new instruction is being set up for execution. It is turned on at the beginning of all single word instructions and for the first word of all double word instructions.

I2   shows that the second word of a double word instruction is being set up for execution.

IA   shows that the instruction being set up is a double word instruction that has an indirect address. The indicator is on while the indirectly addressed word is being read out of storage.

E   shows that the instruction set up during I-time has been defined by the Op code and is now being executed.

E1   is turned on with the E indicator. Its on condition shows that instruction execution control circuitry has progressed to the E1 cycle point. E1 is turned off at the next clock zero (0) time. Instruction can then progress through E2 and E3 time. (There are no E2 and E3 console indicators.)

Timers

These three indicators (A, B, and C) show the status of their respective interval timers. An on condition indicates that the timer is in operation.

Interrupt Levels: An Interrupt Level indicator is on for each interrupt level requesting service or being serviced. Once on, an Interrupt Level indicator can be reset by either of two instructions:

1. A mask instruction that is executed before servicing of the interrupt begins. (The interrupt request is not lost but merely detained until the interrupt level is unmasked, at which time the indicator is turned back on.)
2. A branch-out-of-interrupt (BOSC) instruction is executed to complete servicing of the interrupt.

Both of the above instructions are quasi instructions; that is, variations of the XIO and BSC instructions.

The last three interrupt level indicators — Customer Engineering, Trace, and Check (Internal Interrupt) -- cannot be masked. The CE interrupt can be initiated only from the CE panel or from a device operating in CE mode.

Operation Code

These five indicators (0-4) display the Op code of each instruction.

Format (F)

This indicator is on when a two-word instruction is specified.

Tag

The status of these two indicators reflect the instruction register or index register modification of the instruction address   (the on condition of the indicators is shown by a 1):

Indicators 6	7	Register
0	0	I-Reg
0	1	XR-1
1	0	XR-2
1	1	XR-3

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Indirect Addressing

The IA (Bit 8) indicator is on when the instruction contains this bit, which usually indicates indirect addressing.

Branch Out

The BO (Bit 9) indicator is on when there is a bit in position 9 of an instruction. When on in a BSC instruction, a branch-out-of-interrupt (BOSC) is specified.

Carry and Overflow

These two indicators are turned on individually when their respective conditions occur in the accumulator (A-register).

DATA FLOW DISPLAYS

Six rows of indicators and two rotary switches (Figure 14) facilitate the display of data flow in the P-C. A review of the P-C Data Flow section and the Data Channel section is recommended at this point.

Address Register

These 16 indicators display the data in the Storage Address Register (SAR) or the selected Channel
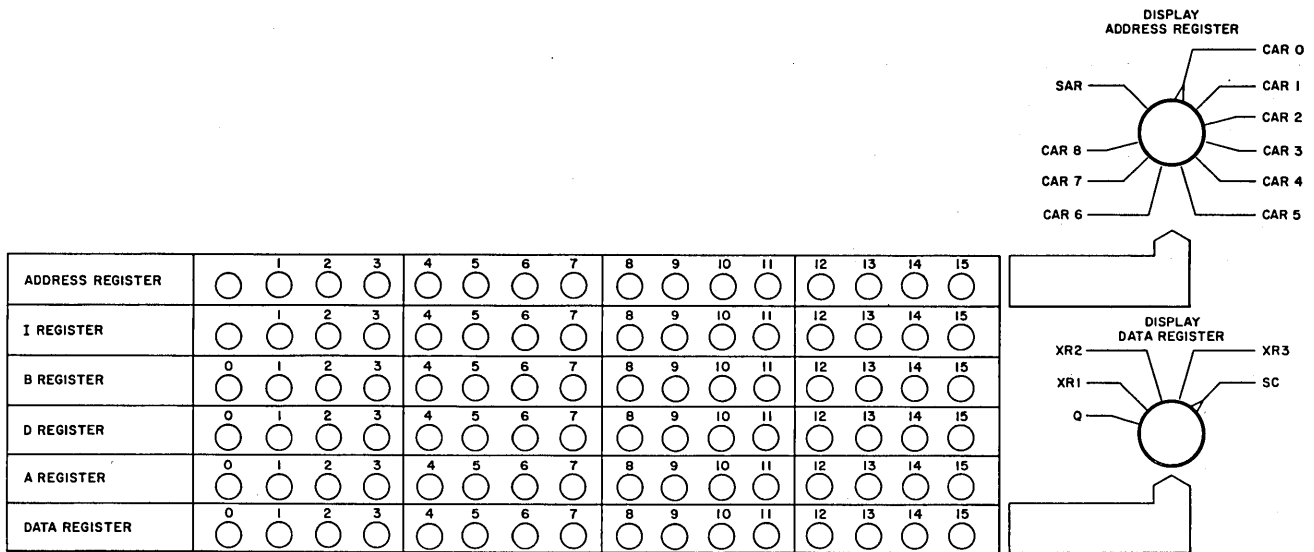
Figure 14. Data Display Lights and Switches

Address Register (CAR), depending on the position of the Display Address Register rotary switch. The selected register is displayed each time the P-C comes to a stop or wait condition. (The clock will be at 7.)

Display Address Register Switch

This 10-position rotary switch is used to select a CAR or SAR for display in the Address Register.

Permanent Register Displays: I, B, D, and A

The contents of these four registers are always displayed.

Data Register

These 16 indicators display the contents of the Q-register, which is the accumulator or A-register extension, the index registers (XR1, XR2, or XR3), or the shift counter (SC), depending on the position of the Display Data Register rotary switch. The selected register is displayed each time the P-C comes to a stop or wait condition. (The clock will be at 7.)

Display Data Register Switch

This 5-position rotary switch is used to select the Q-register, an index register, or the shift counter for display in the Data Register.

DISPLAY PROCEDURES

The following procedure may be used to display core storage data between the execution of single instructions:

1. With the P-C in a stop condition, position the rotary Mode switch to SI (Single Instruction).
2. Start switch depressions may now be used for single instruction operations to get the program to the desired point for data display.
3. Record the address in the I-register. (The I-register is used in Display mode and this recorded address is needed to return the P-C to the next instruction.)
4. Set the address of the core storage word to be displayed in the Data Entry Switches.
5. Position the Mode switch to Load.
6. Press Load I switch.
7. Position Mode switch to Display.
8. Press Start. The selected word is now displayed in the B-register indicators.

9. To display other core storage words, repeat steps 4 through 8.
10. To continue the program:
    a. Set Data Entry Switches to address recorded in step 3.
    b. Position Mode switch to LOAD.
    c. Press Load I switch.
    d. Position Mode switch to RUN.
    e. Press START.

To display core storage data between single core storage cycle operations:

1. With the P-C in a stop condition, position the Mode Switch to SSC (Single Storage Cycle).

2. Press Start repeatedly until the desired cycle in the execution of the instruction is reached.
3. Perform steps 3 through 10 of the preceding Single Instruction execution procedure.

PROGRAM FAILURE—RESTART

Program restart points should be written into programs to allow recovery of the system or a complete restart of the system. This recovery procedure must consider the nature of the process and the operational philosophy of the customer.

There are two basic methods of transmitting and/or
receiving data to or from the P-C. First, specific
low speed devices are controlled directly by the pro-
gram. In this Direct Program Control operation,
each character or word of data is transmitted to or
from the P-C core storage by means of separate
Execute I/O (XIO) instructions. The program con-
tinues transmission, character by character, or
word by word, by responding to "Service Request"
interrupts. Devices operating under Direct Program
Control (DPC) include:

    1816 Printer Keyboard
    1053 Printer
    1627 Plotter
    1054 Paper Tape Reader
    1055 Paper Tape Punch
    Process I/O Devices such as analog-to-digital
      converters, contact sense, voltage level
      sense, pulse counters, etc.

The second method of transferring data is trans-
fer via the Data Channels. Data channel (DC) opera-
tions are initialized by a single XIO instruction. The
transfer of data words then proceeds under control of
the specified DC, completely asynchronous to pro-
gram operation.

The Data Channel's method of accessing core
storage provides a powerful means of I/O communi-
cation with the core storage. Whenever the DC re-
quires core storage access, the P-C operation is
suspended for one core storage cycle time. During
this cycle, the data is taken from or placed into
core storage. Access by the DC can occur at the
end of any memory cycle. It does not require that
an instruction be completed. As soon as the DC has
been satisfied, which normally takes one cycle, the
stored program execution proceeds. The logical
state of the P-C is not changed by the DC's access
to core storage. This method of access is some-
times referred to as "cycle stealing" since a cycle
is taken from the stored program execution cycles
at any time.
    Devices operating under DC control include:

    2401/2402 Magnetic Tape Drive
    2310 Disk Storage Drive
    1443 Printer
    1442 Card Read-Punch
    System/360 Adapter

Some devices operate under DC or DPC control, de-
pending on their characteristics and the configuration
of the 1800 system. These devices include:

    Analog Input
    Analog Output
    Digital Input
    Digital Output

ON-LINE SERVICING CONSIDERATIONS

The 1800 System provides a means for On-Line
servicing of Input/Output devices without the require-
ment for the customer to terminate his operations.
    The feature which makes this service approach
possible is a 256 word Auxiliary Core Storage unit
which provides the Customer Engineer with storage
for the programs and data necessary.
    This auxiliary storage unit is designed to prohibit
the possibility of alterations of the main core storage
during service operations. The auxiliary storage
cannot read or write in the main storage, and the
main storage cannot read or write in the auxiliary
storage.
    When an Input/Output device is in the CE Mode
and is being exercised by an auxiliary program, the
main storage programs are impacted only by the exe-
cution time of the auxiliary instruction. Because the
CE Mode operates on the lowest interrupt priority,
service programs will execute only when the main
storage programs are not operating on interrupt
routines.
    To permit this service approach, it is necessary
to reserve words 1, 2, and A_{16} in main storage. It
is also necessary for main storage programs to have
the ability to program disconnect any Input/Output
device that requires servicing.
    The CE interrupt to an auxiliary program has
been designed with the knowledge that it is quite pos-
sible for an occasion to arise which could require a
change of the main storage program while the system
is executing an auxiliary program. In such an event,
it could be mandatory for the auxiliary program to
branch out to a different return instruction address.
    When the above occasion occurs, it is necessary
only to write the desired return address into the
Auxiliary Storage Return Address location — word A
in main storage. Branching out of auxiliary storage
always sets the Instruction Counter to the address

stored in word A in Main Storage. On an interrupt to auxiliary storage, the I-counter return address is automatically written into word A.

An auxiliary program can utilize the Arithmetic and Index registers. All service programs restore these registers to their original state before branching out.

It is necessary for the customer to realize that an auxiliary service program can possibly interrupt from a Wait instruction in main storage. When this occurs, the branch out from this auxiliary program will be to the instruction at the address following the Wait Instruction.

CE Mode

CE Mode is enabled by a CE diagnostic program with the execution of an XIO Instruction. The IOCC of the XIO must contain the area code of the device being placed in CE Mode; the function code will be 000 and bit 15 must be on. CE Mode is disabled by the same Instruction with Bit 15 off.

When in CE Mode, the device status word of the device is made to appear to be not ready and not busy which is off line status. The true status of ready and/or busy is located elsewhere in the device status word and is to be used for diagnosis. The action initiated in the CE diagnostic program interrupts on the CE level and not on the normal assigned level of the device. The CE Mode uses the assigned core-storage addresses $(0001, 0002,$ and $000A)_{16}$. The interrupt on CE level stores the instruction register at location $000A_{16}$ in main storage (even if this location is storage protected) and branches to execute location 0001 in main storage or to location 0001 in auxiliary storage depending on the position of the aux/main storage switch on the CE panel. The Branch out of CE Interrupt branches indirectly to location A_{16} for return to the program. If an overlay of a program is required, a change of location A_{16} can direct the return if a return is required to the correct program location.

DIRECT PROGRAM CONTROL OPERATION

DPC operation of I/O devices proceeds on a one for one basis; that is, an XIO instruction is executed for each data word transferred to or from core storage. The XIO instruction for DPC specifies an I/O Control Command (IOCC) with a function of Control, Sense Interrupt Level, Sense Device, Read or Write. (See description of XIO instructions.)

Control: An IOCC with a function of Control uses the IOCC address and modifier to specify the particular device and the operation to be executed. Examples of Control operations are Feed Card, and Load Interrupt Mask Register.

Sense: An IOCC with a function of Sense Interrupt Level or Sense Device is used to read the "status words" associated with the device: the Device Status Word (DSW), the Process Interrupt Status Word (PISW), and the Interrupt Level Status Word (ILSW). These status words are explained in detail in the Interrupt section. Generally, DSW's are associated with data processing I/O units (card reader, card punch, etc.) and PISW's are associated with industrial processing interrupts (excessive temperature, overflowing tank, etc.). An ILSW is provided for each interrupt level.

Read or Write: An IOCC with a function of Read or Write uses the IOCC address to determine the core storage address receiving or providing the single data word. Immediately following the one word transfer to or from storage, the XIO instruction is terminated and the next sequential instruction is executed. Normally, several data words must be transferred to complete the message transfer. This is accomplished by P-C recognition of a device interrupt each time the device is ready to send or receive a data word. P-C recognition of the interrupt causes a branch to a program subroutine associated with the device interrupt. The interrupt subroutine includes the XIO instruction to read or write the next data word. This subroutine must also modify the address portion of the IOCC for the next data word, provide "table look up" for translation of the device character if required, and maintain a program word count to indicate the end of message if necessary.

The exit from the interrupt subroutine must be accomplished with a BSC instruction that has a one in its Bit 9 position. This Branch-Out-of-Interrupt (BOSC) operation restores the interrupt hardware so that future interrupt requests at the same or lower priority levels can be acknowledged.

Device Busy

It is possible for the program sequence to execute an XIO instruction to a device that is busy responding to a previous XIO instruction. Each device that can have this condition will provide a Busy indicator in the DSW. This indicator signals that the device cannot accept data or control information, and that should it be sent it will be lost. It is up to the program to ensure, by testing the Busy indicator, that data will not be lost. Usually no hardware indication is given to signal incorrect use of the device.

Data Overrun

It is possible for a device operating asynchronously to the program to request a data word transfer before

the program sequence is ready to service the request. This can be true for both input and output. Devices with this potential provide a "program check" indicator that will enable the P-C to know if a data overrun occurs.

DATA CHANNEL (DC)

Data channels are used to transfer data between P-C core storage and high-speed I/O devices. The P-C initializes each DC with a single XIO instruction. The DC then takes control of the data transfer while the P-C continues program operation. The DC has priority to the extent that when the I/O device is ready to send or receive a data word, the P-C is stopped while the word transfers to or from core storage. This transfer takes 2 or 4 μsec, depending on the core storage cycle time, and is referred to as a cycle steal. P-C data and conditions are undisturbed except for the core storage locations that receive data from an input device.

Three DC's are standard on the 1800 system; six more are available on an individual basis. Thus, it is possible to have more than one I/O device requesting core storage cycles at the same time. When this occurs, the DC control circuitry stops the P-C and services the requesting devices according to their DC priority. This priority is a hardware priority assigned by the user and is not related in any way to the Interrupt feature. Data Channel priority is assigned by the user when ordering the system.

The maximum time before service of the highest priority DC (level zero) is 2.25 or 4.5 μsec, depending on the cycle time of core storage. After all requesting devices have been serviced, the P-C continues with the program.

I/O devices that are to be operated concurrently must be on separate DC's. Those that do not require concurrent operation can be on the same DC. When multiple devices are assigned to the same data channel, the Busy indicator of all these devices must be tested before an operation can be given to any of these devices.

The XIO instruction for DC specifies an I/O control command (IOCC) with a function of Initialize Read or Initialize Write. However, even though a device operates on a data channel, XIO instructions for DPC can be used to sense device status and for control. (See description of XIO instructions.)

Data Channel Functional Components

Channel Address Register

A Channel Address Register (CAR) is a 16 bit register used to store the core-storage address of the next word that will be addressed (by the Channel Address Buffer) for an operation with its associated Data Channel. Each Data Channel is assigned to a particular I/O device (assigned by the user when ordering the system) and has its own Channel Address Register.

A Data Channel and its associated CAR are selected when their assigned I/O device is selected by the Area Code and Modifier of an IOCC word. CAR is incremented by one after each transfer of its contents to CAB.

Channel Address Buffer

One Channel Address Buffer (CAB) is used by all Channel Address Registers to address core storage. When a cycle steal request occurs, the CAR for the requesting I/O device is transferred into the Channel Address Buffer.

Channel Address Register Check

Channel Address Register (CAR) checking is provided to ensure that the first word addressed by a selected CAR is the first word of the correct data table. The CAR check will be performed in one of two ways, depending on the type of I/O device (chaining or non-chaining).

Non-chaining devices are the
    1442
    2310
    1443

Chaining devices are the
    Analog Input
    Digital-Analog Output
    Digital Input
    2401/2402
    System/360 Adapter

A CAR check is made for all devices after the Address from the IOCC word is transferred to the selected CAR. A bit by bit comparison is made between the contents of the selected CAR and the contents of the B-register. If any of the corresponding bits are not equal, a CAR check error has occurred. This CAR check error terminates subsequent cycle steal requests for the assigned I/O device and initiates an internal interrupt. The I/O device cannot request a cycle steal until the Interrupt Level Status Word for the internal interrupt is sensed and the I/O device is reinitialized by another XIO instruction.

Another CAR check is made for chaining devices each time the I/O device chains to a different data table. The CAR check at the beginning of the second

data table and all subsequent data tables in the chain is accomplished as follows: The first word of the data table (second data table, third data table, etc.) must contain its own address. After the first word of the data table is addressed, a bit by bit comparison is made between the contents of the selected CAR and the contents of the B-register. If any of the corresponding bits are not equal, a CAR check error has occurred. Subsequent cycle steal requests are terminated and a bit is set in that device's DSW.

I/O Device Functional Components

Word Count Register

A Word Count Register is provided in each I/O device assigned to a Data Channel (except the 1442). The Word Count register is loaded with the contents of the word count portion (bit positions 2 - 15 maximum 14 bits) of the data table and is decremented each time a data word is transferred from (to) the data table. Word Count capacity for the attachments:

Device	Number of Bits Available	Bit Positions in Word Count Location	Max Count Accepted by Device
1443	7	9-15	60 or 72
2310	9	7-15	321
2400	14	2-15	16,383
DI	8	8-15	255
DAO	8	8-15	255
AI	14	2-15	16,383
System/360 Adapter	14	2-15	16,383
1442	-	-	-

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For I/O devices without chaining ability, the word count must be stored in the first word of the data table. For devices with chaining ability, the word count must be stored in the first word of the first data table and in the second word of all subsequent data tables in the chain.

Scan Control Register

A Scan Control register is provided in each device that has chaining ability. Scan Control bits must be stored in the first word of the first data table (bit positions 0 and 1) and in the second word (bit positions 0 and 1) of the second data table and all subsequent data tables in a chain. The following is a list of the devices that have a Scan Control register.

I/O Device

2401/2402
Digital or Pulse Counter Input
Digital-Analog Output
Analog Input

The Scan Control register controls the I/O device and the Data Channel operation at the end of the data table as follows:

Bit 0	Bit 1	
0	0	Single scan of data table and stop with an interrupt
0	1	Single scan of data table and stop (no interrupt)
1	0	Continuous scan of this data table or a different data table with an interrupt at the end of this table.
1	1	Continuous scan of this data table or a different data table with no interrupt.

DATA CHANNEL OPERATION

The numbered steps that follow correlate with the circled numbers in Figures 15 and 16. These steps apply to either non-chaining devices or the first data table of a chaining device.

1. XIO references the IOCC word.
2. The Area Code and Modifier select the I/O device. Function specifies the type of operation (Initialize Read or Initialize Write, etc.).
3a. The Address portion of the IOCC word is stored in CAR for the selected Data Channel (I/O device).
3b. CAR Check made between selected CAR and B-register.
4. Cycle steal requested. CAR transfers to CAB.
5. CAB addresses core storage for the first word of data table while CAR is being incremented by one.
6. The first word of the data table contains
   a. Scan Control bits (bit positions 0 and 1)
   b. Word Count (bit position 2-15)
   These are transferred to their respective registers in the I/O device. This is the end of the first cycle steal cycle.
7. When another cycle steal request occurs, CAR, which was incremented in step 5, now transfers the next higher address to CAB. CAB then addresses core storage while CAR is being incremented.
8. The first data word is transferred to or from the I/O device via the B-register and Data Channel. The Word Count register in the I/O device is decremented by one. This is the end of the second cycle steal cycle.

Steps 7 and 8 now continue on a cycle steal basis; that is, they occur as the I/O device requests data transfers. Between cycle steals, the P-C continues program operation. The CAR is incremented with each

Core Storage

XIO

	Addr

(1)

IOCC

Addr	Area	Fun	Mod

(3a) (2)

Addressing

B-Reg

(3b)

CAR Check

In Bus — To Input Devices

Out Bus — — — — — — To Output Devices

CAR 0	CAR 1	CAR 8

(4)

CAB

(5)
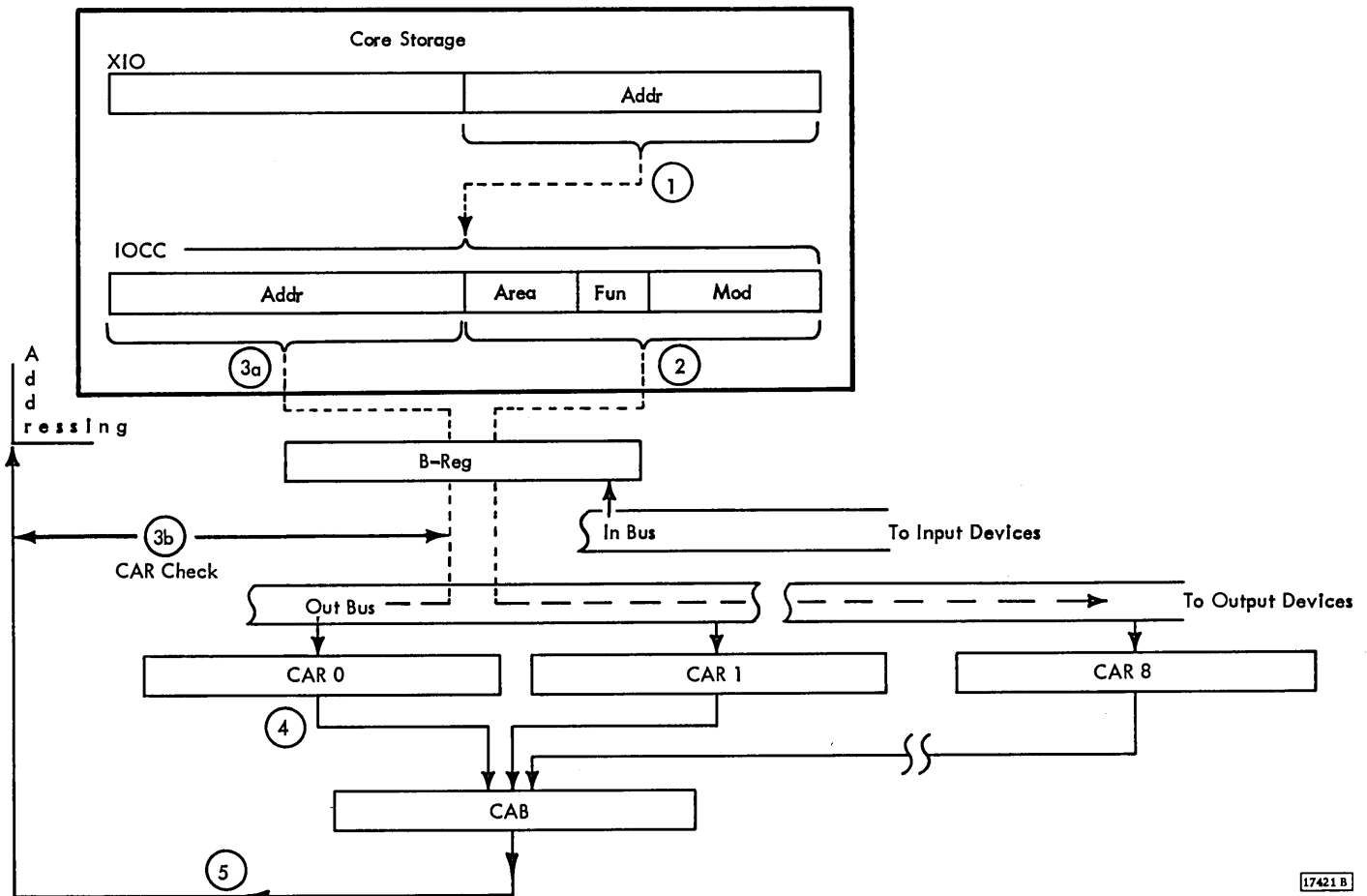
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Figure 15. Data Channel Operation

data transfer and the WCR is decremented. This sequence continues until the last data word of the data table is transferred. The last word transfer is sensed by the WCR reaching zero or through some indicator in the device. If the device does not have chaining ability, no more demands for data transfer are made until the device is reinitialized with another XIO instruction.

Data Chaining

When a continuous scan is indicated by the Scan Control Register (SCR) in a device having chaining ability, the DC takes three cycles after the WCR has reached zero at the end of the data table. The first cycle is used to transfer the word following the

data table to the CAR. The address in this word is the address of the next table of data. The second cycle addresses the first word of the data table and performs the CAR check. The first word of the data table must contain its own address. The third cycle addresses the second word of the data table and transfers its contents (Word Count and Scan Control) to their respective registers. The I/O device is then ready for independent Data Channel operation. In this manner, the DC can operate in a scatter read-write mode. This method of using the DC in a continuous mode is called "data chaining" because the data tables are essentially connected together. The length of time between data transfer cycles on a data chaining operation is a maximum of three core-storage cycles on a device connected to the highest priority DC. It may be greater than this for devices
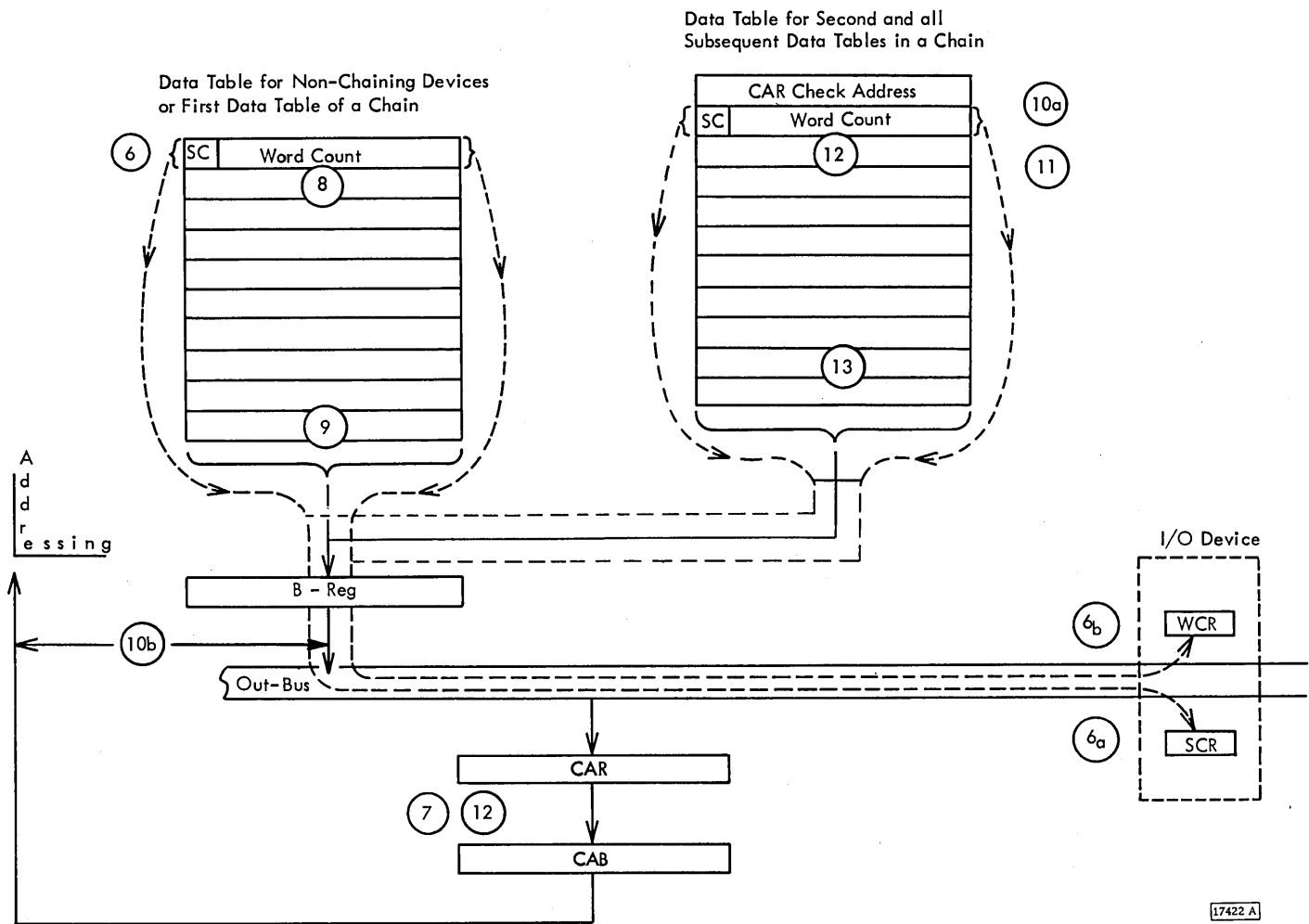
Figure 16. Data Channel Operation

of lower cycle steal priorities, depending on whether they must wait for higher DC priorities to be serviced.

Data Channel Operation (Chaining)

If the Scan Control register contains the bits for a continuous scan, the following numbered steps correlate to the circled numbers in Figure 16. These steps are for the second and all subsequent data tables. See section Data Channel Control for steps 1 through 8 (first data table).

9. The contents of the word following the last data word in the first data table are transferred to CAR. This word must contain the address of the next data table.

10a. When the next cycle is requested, CAR is transferred to CAB to address core storage. The contents of the first word of the next data table are transferred to the B-register. This word must contain the address of itself.

   b. CAR Check is performed and CAR is incremented by one.

11. When the next cycle steal is requested, CAR is transferred to CAB and CAB addresses core storage. The Scan Control bits and Word Count bits are transferred from the second word of the data table to their respective registers. CAR is incremented by one.

12. Data is transferred to (From) the I/O device on a cycle steal basis via the B-register and the Data Channel. CAB addresses core storage to transfer a data word to the B-register. Each

time CAB addresses core storage, CAR is incremented by one. When the next cycle steal request occurs, CAR is transferred to CAB. The Word Count register is decremented for each word transferred.

13. When the last data character is transferred (Word Count is decremented to zero), operation will continue as specified by the Scan Control register. See section for Scan Control Register.
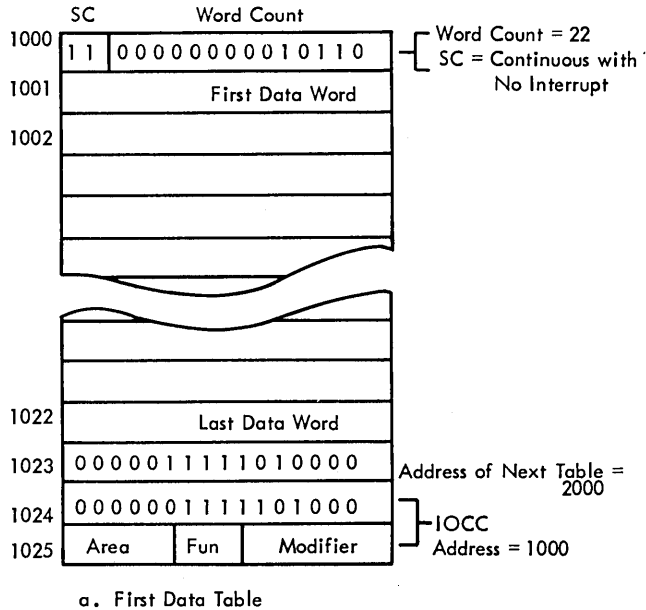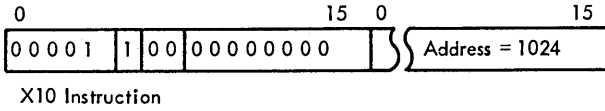
Data Table

Figure 17 is an illustration of two data tables with Scan Control (SC) bits to initiate chaining from the first data table to the second data table.
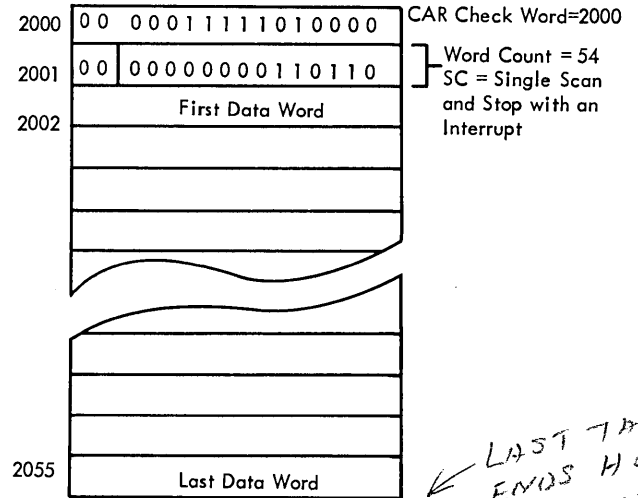
Figure 17. Data Tables for Chaining

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The Interrupt feature provides an automatic branch from the normal program sequence. The branch is based upon an external condition. Examples of conditions which would normally be used to cause interrupts follow: (1) The Interval Timer has concluded the recording of a preset time interval. (2) The Magnetic Tape drive initialized and selected on a Data Channel has completed the required data transfer and signals the P-C with a Scan Complete. (3) An undefined operation code has been detected during the P-C instruction readout and therefore cannot be executed. (4) A device, such as the Printer Keyboard, has completed the transfer of the previous character and requests a subsequent character. (5) An external process condition has been detected which requires an immediate change in the program execution.

Interrupt Philosophy

Because of the large number and widely varying types of interrupt requests, it is often not desirable to cause a branch to a unique address for each condition. For the same reasons, it is frequently not desirable to cause one branch for all interrupt requests and to require the program to determine the individual request(s) requiring service. Therefore, it is expedient to group the many individual request lines into a lesser number of priority levels. This accomplishes two very important functions: First, it allows all interrupt requests common to a specific interrupt level to have the privilege of interrupting immediately if the only requests present are of a lower priority level. Conversely, it permits interrupt requests connected to a higher priority level to temporarily terminate the servicing on a lower level and to immediately interrupt to the higher priority. Service is returned to the initial request only after all higher level requests have been serviced. Second, since a unique branch can be defined for each interrupt priority level, it is possible to combine many interrupt requests on a common priority level and therefore use a common interrupt subroutine to service many requests.

There are two important operating characteristics of the interrupt system. (1) When more than one request line is connected to any priority level, it is necessary by programming means to identify the individual request(s) causing the priority level to be energized. (2) The first request that is recognized on a given priority level prevents future requests on that or lower priority levels from interrupting until the completion of servicing the first interrupt is signaled

by a Branch Out Operation (see Branch or Skip on Condition-BSC). However, interrupts that occur on the same level for which an interrupt is being serviced can be interrogated and serviced by programming if the Interrupt Level Status Word (ILSW) is interrogated again before the "Branch Out" is executed. The ILSW is explained in detail towards the end of this section.

INTERRUPT LEVELS

As shown in Table 6 a maximum of 24 external interrupt levels are available. Twelve external interrupt levels are standard, as are the Internal, Trace, and CE interrupt levels. Note that the priority level of each interrupt, as well as its unique core storage address, is listed in decimal form. Note also that all but the Trace

● Table 6. Interrupts

Interrupt	Priority Level	Core Storage Location		ILSW
		Decimal	Hex.	
Internal	1	8	8	Yes
Trace	26	9	9	No
** CE	27	10	A	No
*External 0	2	11	B	Yes
1	3	12	C	Yes
2	4	13	D	Yes
3	5	14	E	Yes
4	6	15	F	Yes — Basic
5	7	16	10	Yes
6	8	17	11	Yes
7	9	18	12	Yes
8	10	19	13	Yes
9	11	20	14	Yes
10	12	21	15	Yes
11	13	22	16	Yes
12	14	23	17	Yes
13	15	24	18	Yes
14	16	25	19	Yes — Special Feature Group 1
15	17	26	1A	Yes
16	18	27	1B	Yes
17	19	28	1C	Yes
18	20	29	1D	Yes
19	21	30	1E	Yes — Special Feature Group 2
20	22	31	1F	Yes
21	23	32	20	Yes
22	24	33	21	Yes
23	25	34	22	Yes

* External Interrupt cannot occur at the end of an XIO or BSI instruction.

** A CE Interrupt Stores the return link in core location 10 (decimal) and starts execution at core location 0001. Interrupts are prevented in the same manner as for the standard forced BSI.

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and CE interrupts have an Interrupt Level Status Word (ILSW). The ILSW, which is explained in detail later, is used to identify the specific condition causing its interrupt level to request service. No external interrupt can occur at the end of an XIO or BSI instruction (until another instruction is taken).

Internal Interrupt

The Internal Interrupt is a P-C interrupt that occurs when any one of four error conditions occur in the P-C:

1. An invalid Op code is detected.
2. A parity error (even number of bits) is detected in the B-register during data transfer to or from core storage.
3. A storage protect violation occurs from an attempt to write into a "read-only" core storage position.
4. CAR Check error occurs either as a CAR Check or as the result of a parity error having caused a command reject.

The Internal interrupt cannot be masked. However, an XIO or BSI instruction prevents the internal interrupt for one instruction. Its ILSW is reset when it is sensed to determine the interrupting condition. The four error conditions are assigned to the ILSW as follows:
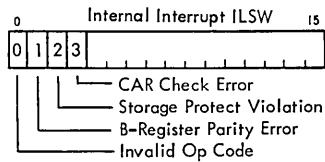
Trace Interrupt

The Trace interrupt occurs after every instruction if the P-C is in program operation with the console mode switch on Trace. The Trace interrupt cannot be masked and does not have an ILSW. However, an XIO instruction prevents a Trace interrupt for one instruction.

CE Interrupt

The CE interrupt can be initiated from the CE panel or from a device operating in CE mode. It cannot be masked and does not have an ILSW. The CE level is not polled on an XIO or BSI instruction

Interrupt Level Masking

A mask register exists for the masking and unmasking of external interrupt levels. An interrupt level that is masked cannot initiate a request for service until it has been unmasked.

Programmed interrupts will not occur if the corresponding interrupt is masked prior to the time the XIO command for programmed interrupt is executed or before the forced BSI occurs.

Device status words and PISWs are not affected by the mask operation.

The XIO Control instruction is used to simultaneously mask and unmask external interrupt levels 0-13 or 14-23, depending on Modifier bit 15 of the IOCC. Two XIO Control instructions are required to mask/unmask the maximum of 24 external interrupts (All external interrupts are automatically masked when electrical power is first applied to the P-C.) The execution of this instruction does not affect the contents of the A-register.

The IOCC for the Mask instruction is shown below:
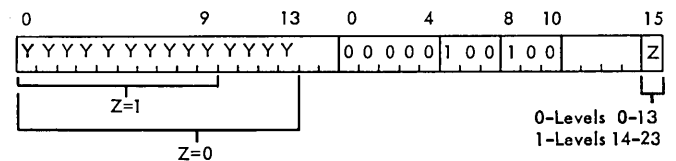
Note that the Area is 00000 and that Modifier bits 8-10 must be 100.

The status of Address bit positions 0-13, or 0-9, depending on Modifier bit 15 (Z), determine whether external interrupt levels 0-13 or 14-23 are masked or unmasked:

A 1-bit masks the corresponding interrupt level.
A 0-bit unmasks the corresponding interrupt level.

External Interrupt Polling

Two polling cycles are required to sample all 24 interrupt level requests. Interrupt levels 0 through 13 are polled as a group and interrupt levels 14 through 23 are polled as another group. The group that is polled on any given cycle is not readily predictable because the first group polled after an interrupt will be the group that was being polled when the interrupt occurred. During any core-storage cycle, other than the first core-storage cycle of an instruction, both groups of interrupt levels are polled. Therefore, unmasking an interrupt level for an instruction that takes only one core-storage cycle (MDS, LDX, LDS, etc.), would not poll all 24 interrupt level requests. This one core-storage cycle instruction would poll only one group, and the group could be either 0-13 or 14-23. Polling is inhibited during:

- XIO and BSI instructions.
- Load, display, or IPL modes.
- Clear storage operations.

Programmed Interrupts

External interrupt levels can be programmed. An
XIO Control instruction is used to turn on individual
external interrupt levels within either of two groups
(0-13 or 14-23) depending on the status of Modifier
bit position 15 of the IOCC. Two instructions must
be executed to turn on interrupt levels in both of
these groups. The IOCC is shown below:

```
0               9   13  0     4   8  10      15
 Y Y Y Y Y Y Y Y Y Y Y Y Y Y   00 000 100 101        Z
 |_____|                               |_|
      Z = 1                          0-Level 0-13
 |_____|         1-Levels 14-23
          Z = 0
```
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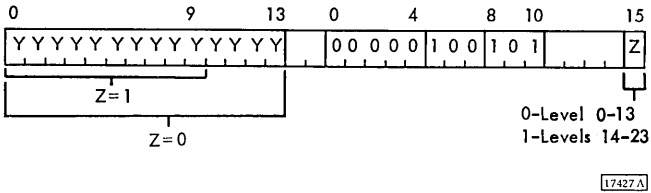
Note that the Area is 00000 and that Modifier bits
8-10 must be 101.

The status of Address bits 0-9 or 0-13, depend-
ing on Modifier bit 15 (Z), determine whether individ-
ual interrupts within priority levels 0-13 and 14-23
will be turned on:

> A 1-bit turns on the corresponding external
> interrupt level.

> A 0-bit does not turn on the corresponding
> external interrupt level.

Programmed interrupts will not occur if the
corresponding interrupt level is masked prior to the
time the XIO command is executed.

If a programmed interrupt level is turned on but
the hardware forced BSI instruction has not occurred,
an XIO instruction to mask or unmask any interrupt
level will turn the programmed interrupt level off.
Another Programmed Interrupt XIO instruction would
be needed to reinitiate the programmed interrupt
after the specified level is unmasked.

Programming Note

A BOSC instruction following an XIO instruction which
turns on a programmed interrupt for a level as high or
higher than the level currently being serviced will reset
the programmed interrupt just turned on. For example,
while in a routine servicing interrupt level 4 an XIO in-
struction to set program interrupt to level 2, followed
by a BOSC instruction would reset interrupt level 2 and
not reset level 4. To prevent this condition the follow-
ing technique can be used for program set interrupts.

XIO	MSK1	} Prevent All Interrupts
XIO	MSK2	
BOSC	+ -Z	Clear Current Interrupt Level
NOP		
XIO	UMSK1	} Restore Interrupt Mask Register
XIO	UMSK2	
XIO	PROGI	Set Program Interrupt
BSC	I EXIT	Exit Current Level

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STATUS WORDS

The I/O devices of the 1800 system and some of the
system features contain "status" indicators. The on/
off condition of each status indicator reveals to the
operating program an operational status or condition
of the device in which the indicator is located. Status
indicators are also contained in the process being
monitored and/or controlled by the 1800 system.
These indicators, both system and process oriented,
project their individual conditions into the system
via the In-Bus. Those process and system indicators
assigned to interrupt levels initiate interrupt requests
when they are turned on.

An XIO Sense Device instruction, which specifies
a particular device, is used to read into the A-register
the on/off condition of each indicator located in the
specified device. Once the indicators of the specified
device are read into the A-register, the contents of
the A-register is considered a Device Status Word
(DSW) or a Process Interrupt Status Word (PISW),
depending on whether the device is located within the
system or in the process. The contents of the A-
register is considered a DSW when the bits represent
the status of indicators from a system device. The
contents of the A-register is considered a PISW when
the bits represent the status of the process interrupts.
Refer to Digital Input Units and Features for Process
Interrupt description.

DSW Indicators

DSW indicators usually fall into three general
categories:

1. Error or exception interrupt conditions.
2. Normal data or service required interrupts.
3. Routine status conditions.

The assignment of indicators to DSW bit posi-
tions is usually specified from left to right in the
following manner:

```
0                                    15
 Error...     Normal...    Routine
 Conditions   Interrupts   ...Conditions
```
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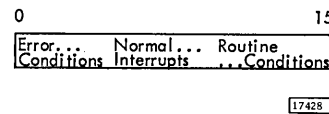
All DSW's are shown in Table 7.

When the DSW indicators are read into the A-
register by an XIO Sense Device instruction, bit
position 15 of the IOCC referenced by the XIO Sense
Device instruction determines whether the indicators
are reset when their status is read into the A-
register. If a bit is present in position 15 of the
IOCC, the selected indicators are reset.

● Table 7. Device Status Words

AREA	FEATURE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Console Interrupt	*Interrupt Request															
0	Interval Timers	Timer A	*Timer B	*Timer C													
0	Data Entry Switches	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Sense Switches	← Sense →				← Program →				← CE Sense →							
1- / 15-	1816 Printer-Keyboard / 1053 Printer —In First Group —In Second Group	*Printer Service Response	*Keyboard Service Response (1816)	*Keyboard Request (1816)		Printer Busy	Printer Not Ready	Keyboard Not Ready (1816)	Storage Protect Violation (1816)	Keyboard Parity Error (1816)	Printer Parity Error			†CE Busy	†CE Not Ready		
2- / 17-	1442 Card Read Punch —First —Second			Error	Last Card	*Operation Complete	Parity Error	Storage Protect Violation	Feed Check Read Station					†CE Busy	†CE Not Ready	Busy	Not Ready
3	1054/1055 Paper Tape Reader/Punch	PT Reader Any Error	*PT Reader Service Request	PT Punch Parity Error	*PT Punch Service Request	PT Reader Busy	PT Reader Not Ready	PT Punch Busy	PT Punch Not Ready	PT Reader Parity Error	PT Reader Storage Protect	†CE PT Reader Busy	†CE PT Reader Not Rdy	†CE PT Punch Busy	†CE PT Punch Not Rdy		
4- / 8- / 9-	2310 Disk Storage First Drive, Second Drive, Third Drive	Any Error	*Operation Complete	Disk Not Ready	Disk Busy (R/W or Ctrl)	Carriage Home	Parity Error	Storage Protect Error	Data Error	Write Select Error	Data Overrun					Sector Count High	Sector Count Low
5	1627 Plotter	*Service Response	Parity Error				Channel 1	Parity					†CE Not Ready	†CE Busy	†CE Not Ready	Busy	Not Ready
6	1443 Printer	*Transfer Complete	Error	*Printer Complete								†CE Carriage Busy	†CE Printer Busy	†CE Printer Not Ready	Carriage Busy	Printer Busy	Printer Not Ready
10- / 16-	Analog Input —Basic —Expander	End of Table	DPC SS Conv Complete	DPC Rly Conv Complete	*Storage Protect Violation	*Parity Control Error	*Parity Data Error	Overload	*Overlap Conflict	Cyc Steal SS, AMAR Busy	DPC Relay Busy						Any Error
10- / 16-	Comparator —AI Basic —AI Expander	High Out of Limit	Low Out of Limit	*Overload	AMAR SS MPX			AMAR 512	AMAR 256	AMAR 128	AMAR 64	AMAR 32	AMAR 16	AMAR 8	AMAR 4	AMAR 2	AMAR 1
11	Digital Input	*Parity Error	*Storage Protect Violation	*DI Scan Complete	*Command Reject												DI Busy
	PISW	←——— Process Interrupt Points (Customer Assigned Groups) ———→															
12	Digital and Analog Output	*Parity Error	Pulse Output Timer	*D & A Out Scan Complete	*Command Reject	Data Channel Active											D/AO Busy
13	S/360 Adapter	*Command Reject	1800 Command Stored	360 Command Stored	*Halt	*Data Check	*Storage Protect Violation	*Transfer End	*End of Table	←——— 360 Command Byte ———→							
13	Adapter Word Counter	←——————— Word Count (1's Complement) ———————→															
14	Tape Control Unit		Tape Unit 1 Select	*Command Reject	*End of Table	Chain Stop	Storage Protect Violation Stop	Tape Data Error	Data Bus Out or P-C Parity Error	Data Overrun Error	*Operation Complete	CE Diagnostic Indicator	Wrong Length Record	At Load Point	Tape Indicator or Mark	Tape Busy or Rewind	Tape Busy or Not Ready
14	TCU Word Counter	←——————— Word Count ———————→															

00 = True Count
11 = 1's Complement

SYSTEM WILL BE INTERRUPTED

* Interrupt Conditions
† Active Only in CE Mode

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PISW Indicators

The PISW indicators, which are physically located in the 1800 System, are turned on by contact closures or voltage shifts in the process. The principal differences between PISW indicators and DSW indicators are:

1. When an XIO Sense Device instruction reads the specified PISW, the indicators are unconditionally reset. (Bit 15 of the IOCC is used to determine reset of the DSW indicators.)
2. There are restrictions on the assignment of PISW bit positions. This is because of the manner in which process interrupts are terminated in the 1800 system.

Assignment of PISW Bit Positions

Process interrupts are terminated on 16-position terminal blocks within the 1800 system. The terminating circuitry restricts the assignment of process interrupts to the bit positions within each PISW:

1. Terminal block positions 0 through 15 must be assigned to corresponding PISW bit positions 0 through 15. There can be no cross assignment, such as position 0 of the terminal block to position 1 of the PISW. Position 0 must be assigned to position 0, 1 to 1, ... 15 to 15.
2. Terminal block positions can be separated in groups of four and assigned to one, two, three, or four PISW's.

For example, as shown in Figure 18, terminal block positions 0-3 may be assigned to bit positions 0-3 of one PISW; terminal block positions 4-7 may be assigned to positions 4-7 of a second PISW; terminal block positions 8-11 to 8-11 of a third PISW; and terminal block positions 12-15 to 12-15 of a fourth PISW. In like manner, terminal block positions 0-7 could be assigned to 0-7 of one PISW, and terminal block positions 8-15 to 8-15 of a second PISW.

Twenty-four PISW's exist in the 1800. They are addressed individually by the modifier of the XIO Sense Device instruction. PISW decimal addresses in the modifier are 2 through 25.

Interrupt Level Status Word

The Interrupt facility includes one 16-position Interrupt Level Status Word (ILSW) for each interrupt level (The Trace and CE interrupts are exceptions; they are unique interrupts and require no ILSW.) Like the PISW and the DSW, the ILSW is not actually a word
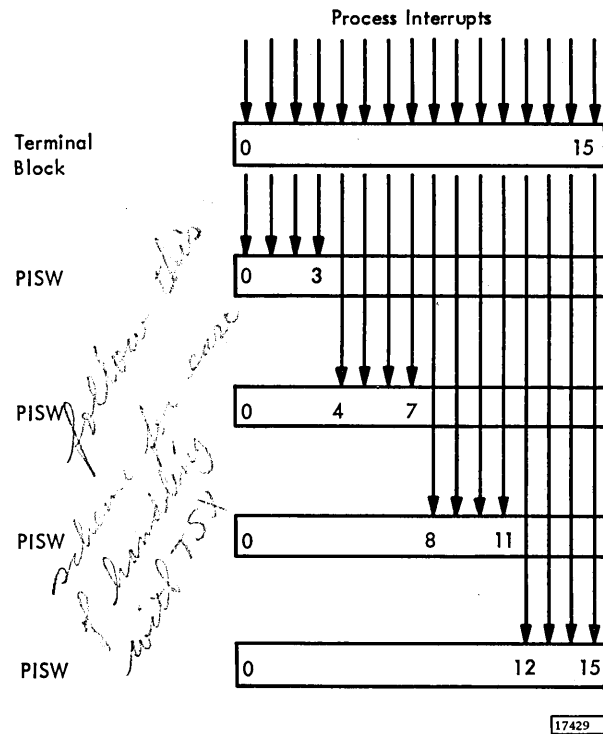
Figure 18. Bit Positions Assignment of PISW's

until it is read into the A-register. Prior to its entry into the A-register, an ILSW is simply 16 signal lines, each of which has OR'ed to it indicators from a status word (PISW or DSW). This relationship is shown in Figure 19.

Each interrupt level requests service when any one of the 16 bits in its ILSW is turned on. When the P-C program recognizes the interrupt request, it executes an XIO Sense Interrupt Level instruction to read the ILSW of the requesting interrupt level into the A-register. The P-C program then determines which bit position in the ILSW caused the interrupt. This bit position identifies the DSW or PISW that has the interrupt initiating indicator. The DSW or PISW is then analyzed by the P-C program to determine which indicator in the DSW or PISW caused the interrupt.

The programmer does not specify the ILSW in the XIO Sense Interrupt Level instruction used to read the ILSW into the A-register. This specification is fixed; that is, each ILSW is hardware assigned to its interrupt level. The Sense Interrupt operation provides the ILSW of the highest priority level requesting service. Except for the P-C Internal interrupts, none of the DSW and/or PISW interrupt indicators ORed into ILSW bit positions are reset when the ILSW is read into the A-register. The indicators are not reset until their respective DSW or PISW is read into the A-register with an XIO Sense Device instruction.
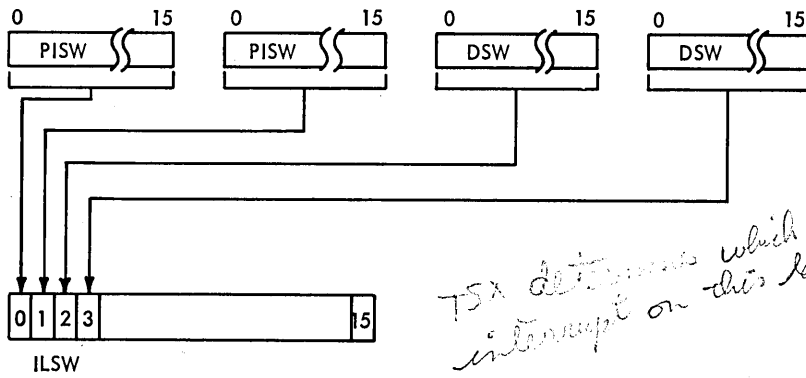
Figure 19. Relationship of Status Words

Figure 19 also shows that each PISW may be assigned to one bit position of an ILSW. If this practice were carried to its extreme, all 24 PISW's could be assigned to only two ILSW's, which would restrict all process interrupts to two interrupt levels. Conversely, only one PISW could be assigned to each ILSW, which would provide the maximum number of interrupt levels for process interrupts. Interrupt level assignments for any one Process Interrupt Adapter must be to interrupt levels 0-11 or 12-23.

PROGRAMMED OPERATION

The 1800 system may be programmed to service interrupt requests in several alternative manners:

1. Process and other interrupts are intermixed on the same level. The ILSW is interrogated first and the PISW is interrogated subsequently.
2. Process and other interrupts are intermixed on the same level, but process interrupt is given priority on that level so that the PISW's (typically one) are sensed directly and checked before the ILSW is sensed and checked.
3. An interrupt level is completely reserved for process interrupts and interrogation of the ILSW determines which PISW contains the actual interrupt.
4. An interrupt level is completely reserved for process interrupts and the number of PISW's on that level is restricted to one. In this case, the program can go directly to the PISW containing the interrupting condition.

In general, an interrupt request is recognized at the completion of the instruction being executed when the interrupt request occurs. Exceptions to this practically instantaneous recognition occur when:

1. The instruction being executed when the interrupt request occurs is either an interrupt forced or normal Branch and Store Instruction Register (BSI) instruction or an XIO instruction. These instructions effectively mask all interrupts during their execution and the execution of the next instruction.
2. The interrupt request level is masked. The request will be retained by the device − not the 1800 − for recognition when the interrupt level is unmasked. (Programmed interrupts are not retained if masked prior to their execution.)
3. The interrupt request is of the same or a lower priority level than an interrupt level being serviced.

When an interrupt request is recognized, the P-C inhibits the normal access to core storage and generates into the B-register a BSI Indirect Addressing instruction. The format of this forced hardware instruction is:
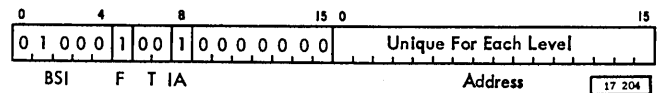
Programming Details

The Address of the forced BSI Indirect instruction is unique for each interrupt level, as specified in Table 6. Program operation from this point is shown in Figure 20 and described below. The circled numbers in Figure 20 correspond to the numbered descriptions below:
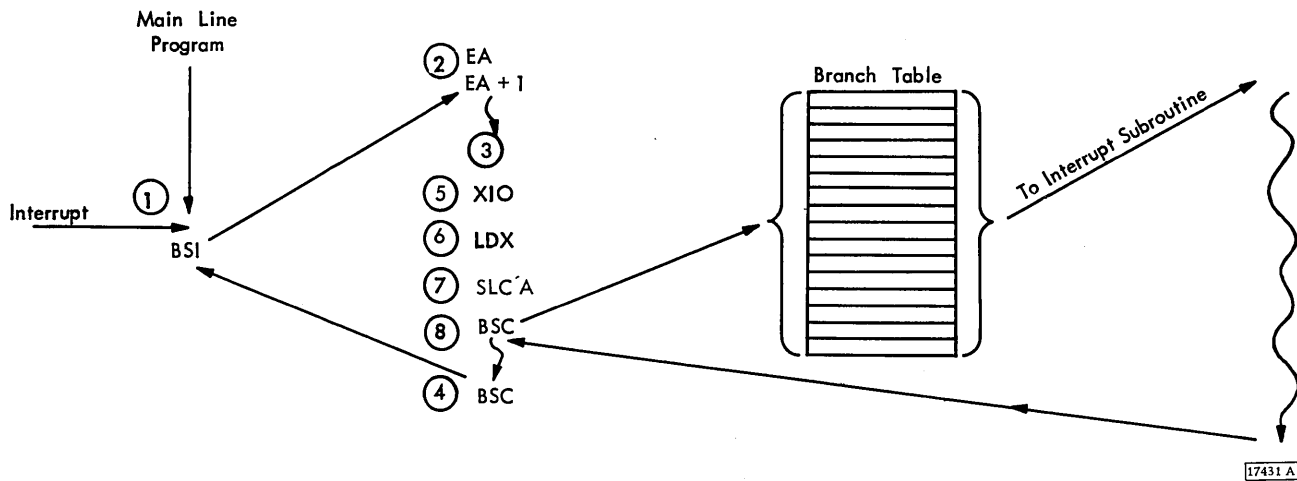
Figure 20. Program Identification of Interrupts

1. The interrupt request occurs during operation of the main line program.

2. The forced BSI Indirect instruction stores the contents of the I-register at the Effective Address (EA) of the instruction. The EA is the address that the user stores at the interrupt level's unique address (Table 6). The forced BSI Indirect instruction then branches to the address of the interrupt subroutine (EA + 1).

3. The interrupt subroutine stores all data and/or index registers that it will use and then prior to subroutine completion restores the same data and/or index registers.

4. The last instruction of the interrupt subroutine is a Branch or Skip on Condition (BOSC) instruction (Bit 9 = 1) that returns the program to the address previously stored at the EA (step 2). This address is the location of the next instruction in the main line program. The BOSC instruction also resets the interrupt level so that other lower priority levels can be recognized.

If a Wait instruction is operative when the interrupt request occurs, the Wait instruction is considered complete when the interrupt request is recognized. Following completion of the interrupt subroutine, the instruction immediately following the Wait instruction will be executed.

Because a number of interrupt requests can be assigned to any one priority level, program analysis of the requesting interrupt level's ILSW is necessary to determine the source of the interrupt request signal. This analysis is accomplished within the interrupt subroutine in the following manner (the numbered descriptions that follow relate to the circled numbers in Figure 20):

5. An XIO Sense Interrupt Level instruction causes the ILSW for the interrupt level being serviced (the highest priority level on) to be read into the A-register. Only the Function of the IOCC need be specified. No other parts of the IOCC are used. The status of the indicators in the devices assigned to the ILSW are not reset.

6. A Load Index Register (LDX) instruction loads an index register with the number of interrupt signals assigned to the ILSW.

7. A Shift Left and Count (SLCA) instruction is executed. The resulting count in the index register corresponds to the first non-zero bit of the ILSW in the A-register.

8. A BSC instruction is executed. This instruction is both indirect and indexed with the index register containing the count corresponding to the first non-zero bit in the A-register. The Address of the BSC instruction is related to the top word of the Branch Table (Figure 21).

The Branch Table is a table of addresses. Each address is the location of an interrupt subroutine that is related to an interrupt request assignment in the ILSW. Thus, if bit position zero of the ILSW is on, the last word of the table is used, and the BSC branch is to the address stored in the last word of the table.

If bit position one of the ILSW is on, the BSC branch is to the address stored in the second to last word of the Branch Table, etc.

Thus, the above sequence of instructions locates the interrupt subroutine for the ILSW bit that initiated the interrupt. Each time the A-register is shifted, the shift count is decreased by one. As the shift
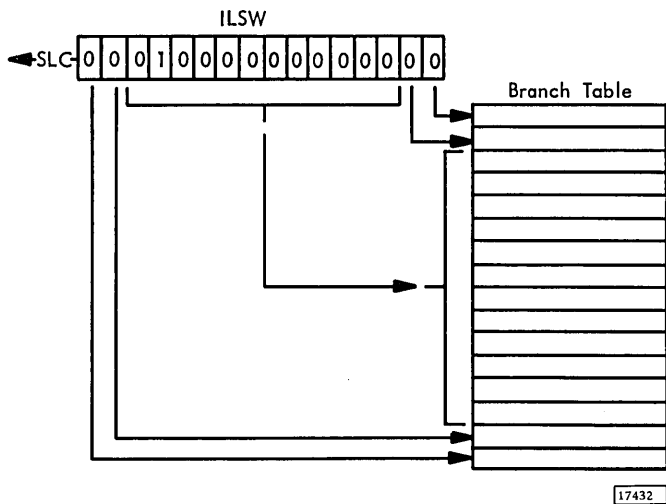
Figure 21. ILSW Branch Table

count is decreased, the indexed address for the BSC instruction is decreased. Effectively, the branch address of the BSC instruction begins at the bottom of the Branch Table and progresses up the Branch Table as the A-register is shifted. For example:

1. Load Index Register
    Index Register one (XR1) is loaded with sixteen or the maximum number of interrupt request lines connected to the level which caused the interrupt. (In this example, assume sixteen request lines are connected to the interrupting level.)
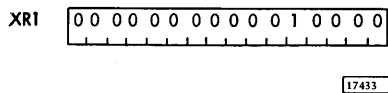
2. Execute I/O (Sense Interrupt Level)
    An XIO instruction is executed which senses the ILSW of the interrupting level into the A-register.
3. I/O Control Command
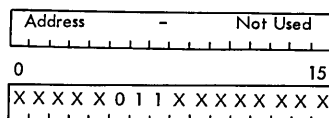
    X - Unused bits

In this example, the ILSW appears in the A-register as follows:
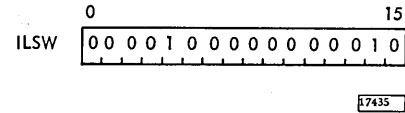
4. Shift Left and Count
    A Shift Left and Count normalizes the A-register and leaves a remainder count in the index register. Note that four shifts have reduced the value in XR1 from 16 to 12. Also, regardless of the status of bit positions 8 and 9 in the index register, they are set to zero and bit positions 0-7 will be unchanged.
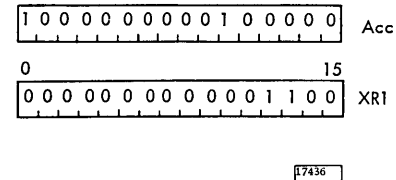
5. Branch or Skip on Condition
    An indexed branch instruction with an indirect bit permits a unique branch to a table of addresses which contains an entry for each bit of the accumulator.

EA = C (XR1 + ADDR)
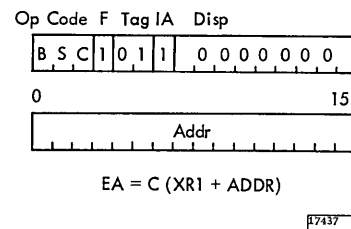
Indicator Identification

If the device requesting service is assigned to a DSW or PISW, it is necessary to determine which indicator in the DSW or PISW is responsible for the interrupt request. This identification can be made in an almost identical manner to the previously described program steps 1 through 8 of Figure 20:

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1. An XIO Sense Device instruction is executed in step 5 instead of an XIO Sense Interrupt Level instruction. The area and/or modifier must specify the device or the status word.

2. The LDX instruction (step 6) loads the index register with the maximum number of indicators assigned to the DSW or the PISW instead of the number of interrupt request signals assigned to the ILSW.

3. SLCA and BSC (in steps 7 and 8) should be programmed in such a manner that all possible interrupting conditions are checked; i.e., even if one condition is on, the other conditions are not assumed to be off.

Programming Note

If a subroutine can be called from two or more priority levels there can be a significant problem in the loss of data (return addresses and intermediate subroutine results) unless care in programming is exercised.

NOTE: If only one device (one interrupt) is on an interrupt level, the program can be written so that only the DSW is sensed into the A-register and its indicators are interrogated. Since only one interrupt is on the interrupt level, the ILSW need not be interrogated.

Industry, science, research, government — all are faced with the need for collecting increasing amounts of data within decreasing time scales. Physical measurements must be monitored and quantified with greater speed and accuracy than every before. The collection of analog data and its conversion for presentation to the digital Processor-Controller is the function of the Analog Input features.

A physical phenomenon is first sensed and converted to an analog electrical signal by sensors or transducers, such as thermocouples or strain gages. Electrical signals from sensors or transducers may be in the millivolt, volt, or milliampere range. Low voltage signals (less than 1 volt) must be amplified to a level acceptable for conversion to digital form. All customer lines from transducers are terminated at the control system on screw-down terminals. The signals are also conditioned at the terminals, including the filtering of extraneous signals, known as noise.

Conversion of analog signals from a voltage level to digital information is accomplished by an Analog-to-Digital Converter (ADC). Such converters, however, are complex enough so that if multiple sources of analog signals are to be converted, they share the use of one ADC. The switching is accomplished by a multiplexer. The data path from sensor or transducer to processor is shown by Figure 22.

ANALOG INPUT UNITS AND FEATURES

The Analog Input Units and features provide modular packaged equipment used to convert voltage or current signals to digital values. The modules used to accomplish the conversions include analog-to-digital converters, multiplexers, amplifiers, and other signal conditioning equipment.

The units and features that accomplish the analog input function are briefly introduced below, followed by more detailed descriptions. A description of the operation of analog input and its relation to the P-C is given later in the Programmed Operation section.

As shown in Figure 23, customer input signals are routed through termination, signal conditioning elements, multiplexer switches, an amplifier (low level signals only), and into the analog-to-digital converter (ADC). The output of the ADC is presented to the P-C via the I/O control or the Data Channel from the ADC output register.

1851 Multiplexer Terminal — Model 1: A modular chassis which mounts in an 1828 Model 2 enclosure; up to 64 analog input multiplexer points (2 wire), signal conditioning elements for each point, and up to two differential amplifiers can be mounted in each terminal.

1851 Multiplexer Terminal — Model 2: Similar to Model 1: However, thermocouples can also be directly connected and 62 multiplexer points are the maximum. A cold-junction temperature indicator device (RBT) is included in the terminal.

Multiplexer (Relay): The relay multiplexer provides switching for both high-level differential inputs and low-level differential inputs, allowing all Mpx/R inputs to use a common Analog-Digital Converter (ADC). Up to 100 points per second switching rate can be attained.

Figure 22. Data Path From Signal Source to P-C

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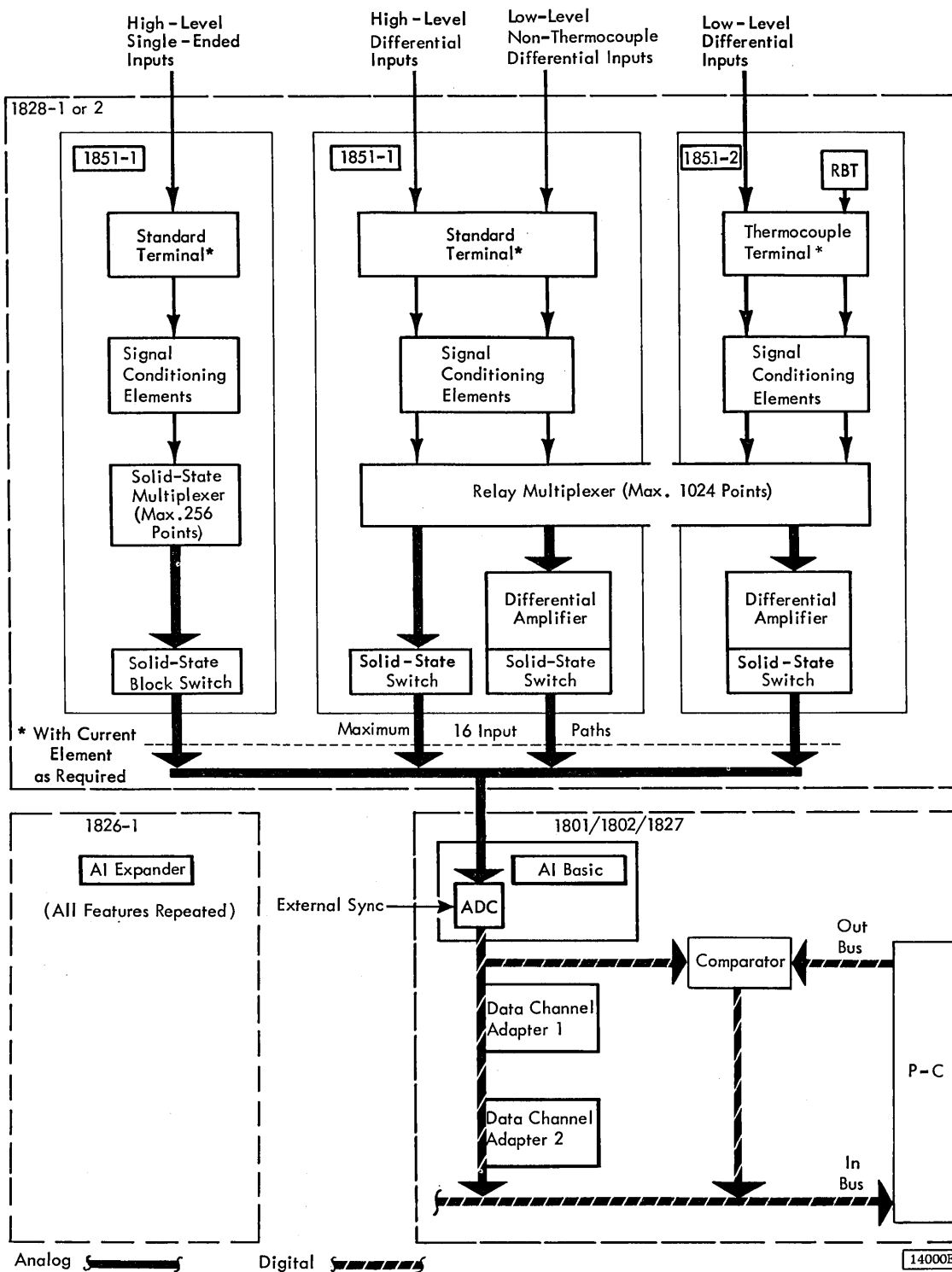
● Figure 23. Interconnection of Analog Input Features

Multiplexer/S (HLSE): A solid state, high-level single-ended (HLSE) multiplexer to provide high-speed switching of analog input signals to allow use of a common analog-to-digital converter.

Multiplexer Overlap: This feature allows overlap of solid state and relay multiplexing.

Multiplexer/R Control and Multiplexer/R Control Additional: These features provide the necessary control circuitry to operate the Multiplexer/R points. Each feature can control up to 256 points.

Multiplexer/S Control: Control circuitry to operate the Multiplexer/S points is provided by this feature.

Differential Amplifier: A time shared amplifier to raise each low level signal to the 5 volt level of the ADC. Up to 256 Multiplexer/R points can use the same amplifier. It has one range setting: ±10 mv, ±20 mv, ±50 mv, ±100 mv, ±200 mv, or ±500 mv.

ADC – Model 1: Converts analog signals (±5 volt range) to digital values (8, 11, or 14 bits plus sign). This model provides a nominal 10 kc system conversion rate.

ADC – Model 2: Similar to ADC Model 1 but includes a Sample and Hold Amplifier for increased system conversion rates. The nominal system conversion rate is 20 kc for this model.

AI Data Channel Adapter – 1: Allows Chained Sequential mode of analog input (AI) operation by connecting a Data Channel to the analog input interface.

AI Data Channel Adapter – 2: Allows Random mode of analog input operation by connecting a second Data Channel to the analog input interface.

Comparator: Performs range checking on digital values developed by the ADC. The high and low limits are selectively obtained from the Processor-Controller for those values to be checked. When values are determined to be out-of-limit, then an interrupt informs the P-C. Only one P-C cycle is required for each value to be limit checked.

Analog Input Expander. Allows a complete analog input system to be configured around the 1826 Data Adapter Unit. Thus, a second ADC or simply a separated ADC may be added to any 1800 System.

Multiplexer/R and Multiplexer/S Maximums and Ranges: Although the maximum number of Multiplexer/R points and Multiplexer/S points are 1024

and 256, respectively, both maximums cannot be installed within the same system. The simultaneous maximums for each system are dependent upon the number of analog input ranges.

Number of Mpx/S * Groups	Mpx/R * Points (Maximum)	Number of Differential Amplifiers (Maximum)	Number of Low Level Ranges (Maximum)
0	256 HL +768 LL	15	6
	No HL +1024 LL	16	6
1	256 HL +768 LL	14	6
	No HL +1024 LL	15	6
2	256 HL +768 LL	13	6
	No HL +1024 LL	14	6
3	256 HL + 768 LL	12	6
	No HL +1024 LL	13	6
4	256 HL +768 LL	11	6
	No HL +1024 LL	12	6
5	256 HL +768 LL	10	6
	No HL +1024 LL	11	6
6	256 HL +768 LL	9	6
	No HL +1024 LL	10	6
7	256 HL +768 LL	8	6
	No HL +1024 LL	9	6
8	256 HL +768 LL	7	6
	No HL +1024 LL	8	6
9	256 HL +768 LL	6	6
	No HL +1024 LL	7	6
10	256 HL +768 LL	5	5
	No HL +1024 LL	6	6
11	256 HL +768 LL	4	4
	No HL +1024 LL	5	5
12	256 HL +768 LL	3	3
	No HL +1024 LL	4	4
13	256 HL +512 LL	2	2
	No HL +768 LL	3	3
14	256 HL +256 LL	1	1
	No HL +512 LL	2	2
15	256 HL + No LL	0	0
	No HL +256 LL	1	1
16	No HL + No LL	0	0

* Multiplexer/R input ranges are ± 10, ± 20, ± 50, ± 100, ± 200, and ± 500 millivolts for input to a differential amplifier, and ± 5.0 volts for direct input to the ADC. The only Multiplexer/S input range is ± 5.0 volts for direct input to the ADC. [17442A]

1851 MULTIPLEXER TERMINAL

The 1851 Multiplexer Terminal is a modular chassis in which multiplexing and signal conditioning features can be mounted. The 1851 terminals are mounted in a 1828 enclosure. Up to 19 terminals can be included

for any one ADC in a system. Multiplexer/R and Multiplexer/S cannot be installed in the same 1851 terminal unit.

There are two models of the Multiplexer Terminal. The Model 1 provides for the insertion of up to 64 multiplexer points in groups of 16 points. Customer wires are terminated on screw down terminals. The Matching Elements are available for each Multiplexer Terminal. Up to two Differential Amplifiers can also be mounted in each terminal.

The Model 2 is a modified terminal to allow for thermocouple termination, cold junction thermal stabilization, and a Resistance Bulb Thermometer (RBT) circuit. These elements are used to determine cold-junction temperature. Thus, thermocouple wires can be connected directly to the terminals and the cold-junction temperature can be computed by the P-C. The maximum capacity of the Model 2 is 62 multiplexer points. Two multiplexer addresses are used for the cold-junction temperature signal measurement (00 is RBT reference; 01 is RBT bridge output voltage).

These are the first two addresses that are installed in any 1851 Model 2.

NOTE: Therefore, the first Multiplexer/R group has only 14 analog input multiplexer points available for external source signals. The ranges for this group must be ±10, ±20, or ±50 millivolt.

It is important that both readings be taken at intervals which are small compared with significant ambient temperature change intervals. Separate readings are required for each Model 2 Multiplexer Terminal.

All other functions of the Model 2 Terminal are the same as the Model 1 Terminal. Thus nonthermocouple signals may be terminated in the Model 2 (if required by the System configuration).

MULTIPLEXER/R

The Multiplexer/R feature provides for relay multiplexing of high or low level analog inputs at a maximum speed of 100 points per second. The equipment is card-mounted and plugs into the Multiplexer Terminal in groups of 16. Up to 16 groups can be combined to form the input to one differential amplifier providing up to 256 input points per amplifier. Each amplifier has a fixed range. The full scale input range for any group of Multiplexer/R points depends on the range of the amplifier to which it is connected. Ranges available are: ±10 mv, ±20 mv, ±50 mv,

±100 mv, ±200 mv, and ±500 mv. High level inputs (-0.5 to +5.0 volts) do not require an amplifier.

The Multiplexer/R can operate with a maximum of 200 volts common mode (DC or peak to peak AC).

MULTIPLEXER/S (HLSE)

The Multiplexer/S feature provides for solid-state multiplexing of high-level, single-ended (HLSE) analog inputs. System speeds are dependent upon the ADC, amplifier, etc., used in any particular system. The Multiplexer Overlap feature allows the overlapping of Multiplexer/R and Multiplexer/S associated with any single ADC on a system. Groups of Multiplexer/S are mounted in the Multiplexer Terminal-Model 1 and cannot be intermixed with Multiplexer/R points within a terminal.

The input voltage range is ±5 volts full scale. When used with the ADC Model 1, conversion rates can be as high as 10,000 conversions per second with about 50 microseconds sample time.

A Sample and Hold Amplifier in the ADC Model 2 permits conversion rates to be increased to as much as 20,000 conversions per second with about 12 microseconds sample time.

Multiplexer Overlap

Several methods of overlapping Multiplexer/R and Multiplexer/S are possible.

Overlap Without Special Feature

There are two conditions by which overlapping can occur without the overlap special feature.

1. Using the direct programmed control mode of operation, the selection of a point in the relay multiplexer may be started and then a series of conversions of solid state points may be performed while the relay point is being selected.

    When the relay multiplexing is complete, it obtains use of the ADC for conversion of the relay point. When the conversion of the signal at the point is completed and the resultant data in the ADC register is available, an interrupt is activated. Solid state and relay point interrupts are differentiated by programmed interrogations of the Analog Input, Device Status Word (DSW).

    An interrupt resulting from the completion of an input point conversion (either relay or solid-state point) suspends selection of another point until the converted value has been read into core storage.

2. If a discrete conversion of a relay point is started under programmed control, a sequence of conversions of solid state points can be started on Data Channels. When the relay multiplexing is complete, it obtains use of the ADC for conversion of the relay point. When the resultant converted data is available in the ADC register, an interrupt is activated. This is the normal "DPC conversion complete" interrupt utilized for discrete conversions under programmed control. If the solid state conversions have not been completed when the relay multiplexer control captures the ADC, then the solid state conversions are continued as soon as the ADC Register has been cleared. No further discrete conversion may be started until the solid state conversions are complete.

Overlap With Special Feature

With the Multiplexer Overlap special feature another means of overlapping is possible. Under two-Data-Channel operation, relay addresses can be interleaved with solid-state multiplexer addresses.

These addresses do not have corresponding ADC values placed in the ADC converted data table. The relay point addresses are latched by the relay multiplexer control, and the interface control requests a further cycle to obtain the next solid-state multiplexer address from P-C memory. Random conversions proceed asynchronously until the relay multiplexer is ready. When the relay multiplexer is ready, the relay multiplexer takes control. The next point converted will be a relay point and an Interrupt will allow the P-C to transfer the value in the ADC Register to core storage under XIO-Read control, after which conversions are continued under Data Channel control. If another relay address is recognized before the first relay point has been converted, an interrupt occurs. This interrupt informs the P-C that a relay point was mislocated in the address table. The mislocated relay point will not be converted. A relay point cannot be the last word in a data table when the overlap special feature is installed.

Efficient use of overlapping of relay and solid state multiplexing depends upon correct placement of addresses in the Multiplexer Address Data Table. Enough solid state multiplexer addresses must be included between relay addresses to ensure that

sufficient time is always taken so that the first relay point is converted and relay multiplexer control is ready. Approximately 100 Mpx/S points can be converted with ADC Model 1 and 200 Mpx/S points with ADC Mod 2 while one Mpx/R point is being selected.

SIGNAL CONDITIONING ELEMENTS

Signal Conditioning Elements listed below provide passive signal conditioning of each analog input signal at the terminal. For specifications and characteristics of each element, see 1800 Data Acquisition and Control System Installation Manual, Physical-Planning.

1. Current Element. 4 − 20 ma current input signals are converted into either 0.1 to 0.5 volt or 1 to 5 volts. Current elements can be installed with Multiplexer/S or Multiplexer/R. A current element cannot be used with a voltage element.
2. Filter Element (Multiplexer/R only. A low-pass passive filter to reject normal mode ac noise. Filter elements cannot be installed for use with Multiplexer/S.
3. a. Voltage Element (Multiplexer/S). Provides 2:1 voltage attenuation. This element provides for intermixing 10 volt and 5 volt signals within the same Multiplexer/S group.
   b. Voltage Element (Multiplexer/R). Provides 2:1 voltage attenuation. For example, this allows intermixing of 100 millivolt signals and 50 millivolt signals in the same Multiplexer/R group. Voltage elements for Multiplexer/R provide the filtering function described under Filter Element. A Filter Element cannot be installed on points for which a Voltage Element is ordered.
4. Connector Element. Is wired for straight through connection with no signal conditioning.
5. Custom Element. Is available for customer mounting of special conditioning circuits to meet a particular requirement.

DIFFERENTIAL AMPLIFIER

This is a time-shared amplifier used in conjunction with the Multiplexer/R, to raise analog signals to the ADC input level of ±5 volts.

Gains available are: 500, 250, 100, 50, 25, and 10. These allow input voltage ranges of Multiplexer/R points to be specified for: ±10, ±20, ±50, ±100, ±200 and ±500 millivolts.

A single amplifier can service up to 256 input points (16 blocks of 16 multiplexer relays). Up to two amplifiers can be mounted in one Multiplexer Terminal. Thus, multiple amplifiers can be used for voltage range changing in place of passive Voltage Elements.

ANALOG-DIGITAL CONVERTER (ADC)

The ADC provides the 1800 with the ability to convert bipolar analog signals (±5 volt signal range) to digital values. Two models are available: Model 1 includes a buffer amplifier and has program selectable resolutions of 8, 11, and 14 bits. Model 2 is similar to the Model 1 except that it includes a sample and hold amplifier which provides for increased system speed of conversion.

The ADC conversion time depends only upon the number of bits of output that are to be developed. Conversion times are as follows: 8 bits, $29\,\mu sec$; 11 bits, $36\,\mu sec$; and 14 bits, $44\,\mu sec$. Therefore, ADC conversion rates are 23,000 to 35,000 conversions per second (not including amplifier settling time). The input impedances of the ADC Model 1 and Model 2 are 10 megohms and 0.1 megohms, respectively.

The 1800 System conversion rates will vary from 9,000 to 24,000 samples per second (dependent upon equipment installed and mode of operation).

Analog Input Calibration

The analog input calibration facility is housed in the 1828 Enclosure that is abutted to the 1801, 1802, or 1826 containing the Analog Basic.

Power is supplied to the calibration facility through the power switch on the front left side of the 1828.

The calibration facility provides the following dc reference voltages for calibration of AI features when the calibration facility is connected directly to an appropriate 1851 input terminal pair:

+5 volts	100 mv
-5 volts	50 mv
500 mv	20 mv
200 mv	10 mv

Exact voltages are measured at the factory and are recorded (to five significant digits) on the reference unit. Note that connections for +5 volt and -5 volt ranges are different.

A special high-level input point is selected by multiplexer address $13E8_{16}$ (which is outside the normal range of Mpx/S addresses) for ADC calibration only. The multiplexed calibration point can be addressed at any time by the customer program or diagnostic program for an operational check of the ADC. The reference voltage to be addressed is selected by changing connections on a terminal strip. An IBM Customer Engineer changes the connections on the terminal strip.

Data Word

The data word developed in the ADC Register is compatible with 1800 word format as shown below. The data word allows for sign plus 14 bits resolution. Conversion by the stored program of the value presented by the ADC should assume a position for the binary point. This position of the binary point does not change when the format (14, 11, or 8 bit) is changed. Only the number of significant bits in the ADC converted value changes. Negative numbers are in 2's complement form.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
14 Bit Format	±	X	X	X	X	X	X	X	X	X	X	X	X	X	X	I
11 Bit Format	±	X	X	X	X	X	X	X	X	X	X	X	1	0	0	I
8 Bit Format	±	X	X	X	X	X	X	X	X	1	0	0	0	0	0	I

NOTES:

1. ± is the sign of the data: a zero bit is positive, and a one bit is negative.

2. The X's indicate that a one or zero bit may appear to represent the converted value. In the 11 and 8 bit formats, the 0's indicate that only a zero will appear in these positions.

3. I is the overload indication bit. The presence of a one bit indicates an overload condition; that is, the signal was outside the ±5 volt range. Bit 15 is a one when a positive value has all one bits in bit positions 1-8 (11 or 14) or when a negative value has all zero bits in bit positions 1-8 (11 or 14).

4. The one bit in bit position 9 of the eight bit format and bit position 12 of the 11 bit format are provided for half-adjust of the quantizing error. Half-adjust of the 14 bit format quantizing error is accomplished by the ADC circuitry.

29128

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14 BIT RESOLUTION EXAMPLE	Bit Positions 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Normal Positive Binary Value	0,0,0,0,0,0,0,1,0,1,1,1,0,1,1,0
Decimal Equivalent	+187
Maximum Positive Value without Overload	0,1,1,1,1,1,1,1,1,1,1,1,1,1,0,0
Decimal Equivalent	+16382
Normal Negative Binary Value	1,1,1,1,1,1,1,0,1,0,0,0,1,0,1,0
Decimal Equivalent	-187
Maximum Negative Value without Overload	1,0,0,0,0,0,0,0,0,0,0,0,0,0,1,0
Decimal Equivalent	-16383
Positive Overload Condition	0,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1
Negative Overload Condition	1,0,0,0,0,0,0,0,0,0,0,0,0,0,0,1

Note:
Decimal equivalents assume that the binary point is between bits 14 and 15.

17220A

Buffer Amplifier

The Buffer Amplifier is a single-ended operational amplifier and is an integral part of the Model 1 ADC. The amplifier provides high-input-impedance (10 megohms) buffering of the ADC on a time-shared basis for those applications where it is unnecessary to provide a time-shared sample-and-hold input characteristic.

Sample-and-Hold Amplifier

The Sample-and-Hold Amplifier is an integral part of the Model 2 ADC; it is a single-ended amplifier capable of providing a short aperture time in the sampling of high-level analog signals and of providing a high accuracy hold function. The amplifier has an input impedance of 100K ohms. The P-C program must consider the reversed polarities obtained from sample-and-hold input points.

External Sync

The operation of the ADC can be controlled by an external timing (sync) pulse. When the Relay Multiplexer is used, a "ready" condition is transmitted to the external timing device after the Relay Multiplexer and relay block switches have settled. When the Solid-State Multiplexer is used, a "ready" condition is transmitted before the solid-state switches are actuated. The external device provides a sync start pulse which allows the solid-state switches in either type multiplexer to be actuated and then conversion of the selected signal begins.

An "8" bit in the modifier of an IOCC, either "Write" or "Initialize Read," sets up the external sync mode. The absence of an "8" bit in the modifier of either a "Write" or "Initialize Read" command terminates the external sync mode.

External sync cannot be used during overlap (special feature) operations.

COMPARATOR

The Comparator performs selective checking on the digital values converted by the ADC. A range type check is made to confirm that the converted values are within specified limits. The limits are obtained from the Multiplexer Address Table (one P-C cycle delay allows both limits to be acquired) whenever a check is required. The P-C is informed of an out-of-limits condition by interrupt. The two Analog Input Data channel adapter features are a prerequisite to this feature.

Operational Description

In order that a range comparison can be made, both a high limit and a low limit must be set. In converting many analog input source signals, it may be necessary to monitor each signal to assure that the signal remains within specified bounds. Normally, a number of these signals are redundant and other signals need only be checked occasionally. To allow for flexibility of checking input signals, a separate control (in Multiplexer Address word) is added to instruct the Comparator to perform checking when required.

It should be noted that limit words need not remain static. For example, when a particular high limit is exceeded, then a single change will permit

recognition of the return of the signal within the former limits. The high limit is substituted for the low limit and the maximum value is set for the high limit. If the interval timer is read after each limit is exceeded, then the time interval that the signal was out-of-limits is known.

Limit Words

The high and low limits are stored in P-C storage within the Multiplexer Address Table (See Figure 24). These limit values are expressed in eight bits (seven bits plus sign) with negative numbers represented in two's complement form. The Comparator is only used under the Random Mode of Operation (see Programmed Operation section). A limit word follows each Multiplexer Address entry that is to be checked. The Multiplexer Address entry contains two control bits in addition to the analog input point address. These bits are stored in bit positions one and two of the multiplexer address word. The L bit, stored in bit position one, indicates the presence of a limit word as the next word in memory. The K bit, stored in bit position two, indicates whether or not a comparison is to be performed.

Figure 24 shows a sample Multiplexer Address table. The word count and scan control bits are obtained from the data table that receives the converted values. The chain address from this table is used to provide unique chaining. If the Multiplexer Overlap feature is installed, a limit word cannot follow Multiplexer/R addresses.
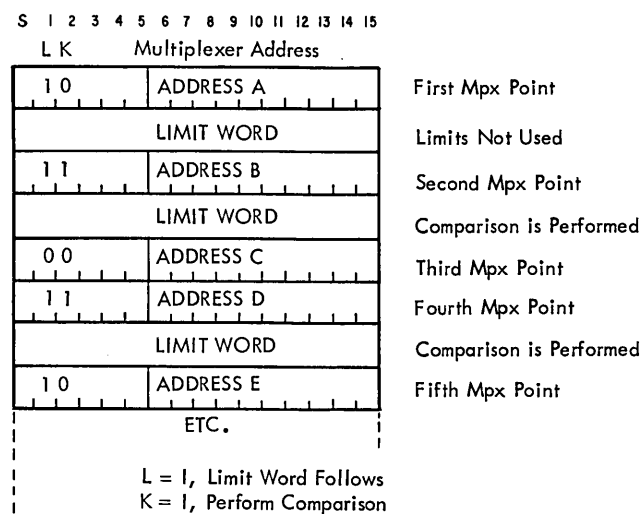
Comparison Cycle (L = 1, K = 1)

When the ADC register is filled with the value to be limit checked (7 high-order bits plus sign during conversion), the limit word is acquired from storage and the limit comparison is performed.

Out-of-Limits Conditions

When the comparator determines that an out-of-limits condition exists, then bits identifying the multiplexer point and the type of condition involved are saved in the comparator. An interrupt unique to the comparator is activated to alert the processor-controller, and further comparisons are suppressed. This suppression has an identical effect to the recognition of zero K bit in the multiplexer address.

Comparison to limits in step with multiplexing is automatically restarted when the Comparator Status Word has been sensed by the processor-controller. The Comparator Status Word enters the accumulator upon execution of a sense instruction.

The out-of-limit conditions are

● High out-of-limit — when ADC value is equal to or greater than the high limit.

● Low out-of-limit — when ADC value is less than the low limit.

ANALOG INPUT EXPANDER

This feature provides two prinicpal advantages:

1. It doubles the capacity of the analog input features.
2. It allows the analog input features to be structured separate from the Processor-Controller.

The Analog Input Expander is a feature of the 1826 Data Adapter Unit, which provides the basic capability for attachment of an ADC, Comparator, Multiplexer Terminals, etc. This second analog input system attaches to I/O Control and Data Channels in a manner similar to the first analog input system. Thus the system conversion rates can be doubled, neglecting I/O interaction.

PROGRAMMED OPERATION

This section describes the control modes that are available for the selection of analog input points, conversion of the selected analog signal to a digital

S 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
L K   Multiplexer Address

1 0	ADDRESS A	First Mpx Point
	LIMIT WORD	Limits Not Used
1 1	ADDRESS B	Second Mpx Point
	LIMIT WORD	Comparison is Performed
0 0	ADDRESS C	Third Mpx Point
1 1	ADDRESS D	Fourth Mpx Point
	LIMIT WORD	Comparison is Performed
1 0	ADDRESS E	Fifth Mpx Point
	ETC.	

L = 1, Limit Word Follows
K = 1, Perform Comparison

17221B

● Figure 24. Multiplexer Address Table with Limit Words

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value, and the transfer of the digital value to the P-C.

There are three basic control modes for the input of analog data: (1) Programmed, (2) Chained Sequential, and (3) Random. They are described in detail below. Essentially the Programmed mode requires the execution of at least one XIO instruction (see I/O Control) for each value that is read into the P-C. The Chained Sequential mode uses one Data Channel and allows any number of groups of sequentially addressed values to be read into the P-C with the execution of one instruction (XIO). Sequentially addressed values are those which are developed from multiplexer addresses in sequence. That is, values with multiplexer addresses 23, 24, ... 46 would constitute a sequential group of 24 points.

The Random mode uses two Data Channels and allows each point to be addressed uniquely. Any number of groups of points may be addressed, converted, and read into the P-C with the execution of two XIO instructions.

Programmed Control

Using the Direct Program Control (DPC) mode of operation, two Execute Input/Output (XIO) instructions are used. The first instruction, an XIO Write, addresses the multiplexer and selects the analog input point which is to be converted. Upon completion of multiplexing, an internal signal is sent to the ADC to start the point conversion. When the ADC has completed the conversion, an interrupt signal is sent from the ADC to the P-C. The P-C initiates a subroutine (for interrupt description, see Interrupt section) to determine the cause of interrupt, if necessary, and provides the second instruction, an XIO Read, to transfer the data to storage. This mode of converting data from analog signal to digital value in storage is a discrete addressing method; that is, two instructions result in the acquisition of data from one input point.

Sequential Programmed Control: A standard operation requires the execution of only one XIO Write instruction for many XIO Read instructions if the subsequent analog input points to be converted are in sequence. A bit in position 8 of the IOCC addressed by the XIO Read instructs the multiplexer to increment by one the address previously converted and then to perform the next cycle. A cycle here is composed of selecting the analog input point, converting the selected analog signal, and initiating an interrupt to inform the P-C that the converted value is in the

ADC register ready to be read into P-C storage. The absence of a bit in position 8 of a Read IOCC terminates the operation.

Chained Sequential Control

Using a single Data Channel, a sequence of analog inputs can be scanned, converted, and stored in core storage with one XIO Initialize Read instruction to initiate the action. The two word IOCC contains the core storage address where the Scan Control bits and the Word Count are stored for the operation. The Word Count is one greater than the number of input signals to be converted in the sequence. The Scan Control bits determine if an interrupt is given and whether or not chaining or termination of the operation is effected when the Word Count reaches zero.

The Word Count is in the first word of the first Data Table (Figure 25a). Note that the Word Count precedes the multiplexer address word which is at location 3000 in this example. The Data Channel "writes" this multiplexer address word to the Analog Multiplexer Address Register (AMAR) which initiates the selection of analog points and conversion to digital values. At the completion of each conversion, the converted data is read into sequential storage locations. After each transfer of data, the Word Count is decremented by one and the previous address in the AMAR is incremented by one. The new address causes the next sequential point to be selected. This operation continues until the word Count reaches zero.

Figure 25 illustrates two data tables which are in core storage and could be used for Chained Sequential Operation. The IOCC word that initiates this analog input function is located in storage locations 3042 and 3043 (Figure 25b). The IOCC initializes the multiplexer and the ADC and then places the address of the Word Count (the first word in the table) in the Channel Address Register (CAR) of the Data Channel. In this example, the Word Count is located in storage location 2999.

The ADC now requests a cycle to place the word count into the Word Count Register (WCR). In this example, the word count is 12. CAR is incremented by one so that now CAR contains the address 3000. On the next cycle, the initial multiplexer address is transferred from location 3000 to the AMAR. When multiplexing is complete, a signal is sent to the ADC to start conversion. At the completion of conversion, the ADC register contains a digital value and a cycle request is made. CAR (now containing address 3001) addresses core storage and the digital value in the ADC output register is transmitted to location 3001.

2999	SC 11 | Word Count = 12
3000	Multiplex Address
3001	Value 1
3011	Value 11
3012	Starting Table Address(3015)

Location

3015	Car Check Word = 3015
3016	SC 00 | Word Count = 25
3017	Multiplex Address
3018	Value 12
3041	Value 35
3042	Starting Table Address (2999)
3043	A/I - Initialize Read

IOCC

17209 A
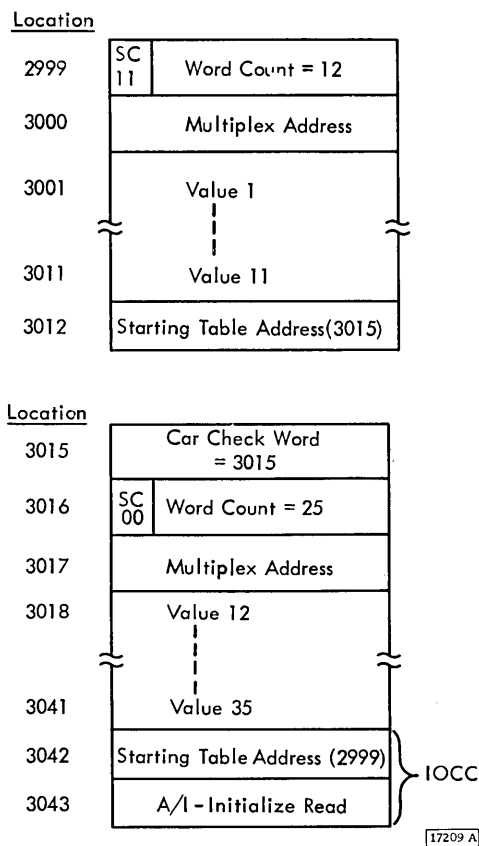
Figure 25. Data Table, Chained Sequential Control

The above procedure is repeated and continues until the WCR reaches zero. At this time, the Scan Control bits are monitored and it is discovered that they indicate continued scanning (11). When continuous scan is indicated by the Scan Control Register, the Data Channel takes four cycles to initialize the I/O device for the next data table. The first cycle transfers the word following the first data table to CAR (this word contains the core-storage location of the next table). The second cycle addresses core storage and transfers the contents of the first word to the B-register. A CAR check is then made (see section Channel Address Register Check). The third cycle transfers the Word Count and Scan Control bits from the second word of this data table to their respective registers in the I/O device. The fourth cycle transfers the Multiplexer address from the third word of the data table to the analog Multiplexer Address Register (AMAR). Data transfers then resume on a cycle steal basis.

When the Word Count Register again reaches zero, the Scan Control bits indicate that the operation will be terminated (00 also indicates an

interrupt). The operation is terminated and a new XIO instruction is required to initiate further operation.

Random Control

In this mode of operation, the multiplexer addresses are transmitted on one Data Channel and the ADC data is transmitted on a second Data Channel. The operation is initiated with two XIO instructions. The first instruction sets up the controls for transferring converted data from the ADC to storage on one channel and loads the Scan Control Register (SCR) and the Word Count Register (WCR) for the operation. The Word Count is equal to the number of converted values to be stored.

The second instruction initiates the transfer of the multiplexer addresses from core storage to the Analog Multiplexer Address Register (AMAR) on the other Data Channel.

When the first analog input point has been selected, a start impulse is given to the ADC. At the completion of the first conversion, a memory cycle transfers the converted data to the set-up Data Table in the P-C. Alternate P-C cycle requests bring in the multiplexer addresses on one channel and transfer the converted data to storage on the other channel. This operation continues until the WCR is decremented to zero. When the WCR reaches zero, the Scan Control bits are interrogated to determine if an interrupt is to be given and whether the operation is to continue or terminate.

Figures 26 and 27 illustrate the multiplexer address and ADC storage tables which are to perform a random addressing operation. An XIO instruction referencing location 3524 initiates ADC action. Another XIO instruction referencing location 3122 initiates multiplexing.

In this example (Figures 26 and 27), 119 points are being read and converted in a random sequence The two ADC tables are chained together while the multiplexer table is chained to itself. The Scan Control bits cause an interruption at the end of each ADC table. The number of multiplexing addresses set up in the Multiplexer Address table must equal the word count set up in the ADC table. Comparator limit words are not included in the word count.

Systems with two Data Channels may convert values using any mode. The mode is selected by appropriate bits in the Function or Modifier of the IOCC. In the Chained Sequential Mode (with two Data Channels), the Data Channel used by the Multiplexer is not used, and the operation is the same as that previously described under Chained Sequential Order.

Location

Location	
3000	This word contains its own address
3001	MPX Address (47)
3002	MPX Address (82)
3119	MPX Address (14)
3120	Starting Table Addr. (3000)
	(Not Used)
3122	Starting Table Addr. (3001)
3123	A/I-Int. WR

} IOCC

17210 A
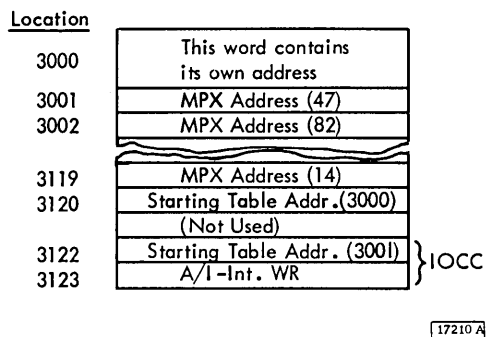
Figure 26. Multiplexer Address Table, Random Addressing

Location		
3201	This word contains its own address	
3202	SC (00)	Word Count (119)
3203	ADC Value (47)	
3204	ADC Value (82)	
3321	ADC Value (14)	

Location		
3402	SC (10)	Word Count (119)
3403	ADC Value (47)	
3404	ADC Value (82)	
3521	ADC Value (14)	
3522	Starting Table Addr. (3201)	

Starting IOCC 3524	Starting Table Addr. (3402)
	A/I – Int. Rd.

} IOCC

17211 A
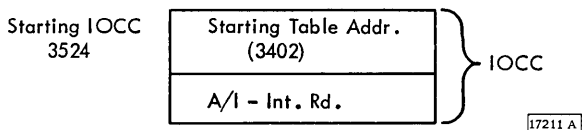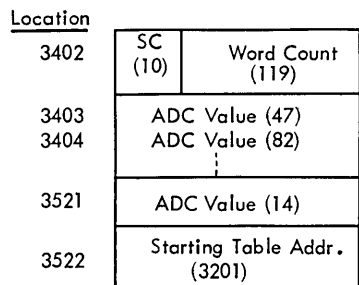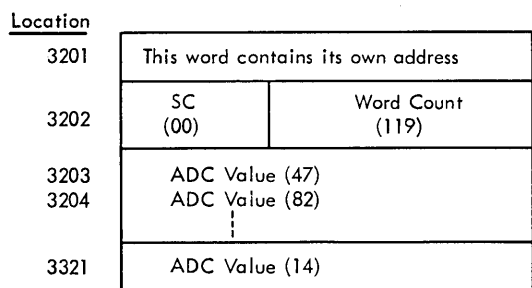
Figure 27. ADC Storage Tables, Random Addressing

A one in bit position 10 of the Initialize Read IOCC specifies random mode, and a zero in bit position 10 of the IOCC specifies sequential mode.

If the overlap feature is used, the ADC word count is equal to the number of solid state points. Since relay points are read by Direct Program Control, they are not stored in the ADC Storage table.

I/O CONTROL COMMANDS – ANALOG INPUT

DIRECT PROGRAM CONTROL

Multiplexer Address Location — 0 1 0 1 0 | 0 0 1 | E X X L H X X X
Write
17 212

ADC Reading Location — 0 1 0 1 0 | 0 1 0 | S X X X X X X X
Read
17 213

Not Used — 0 1 0 1 0 | 1 0 0 | X X X X X X X X
Control
29064

Not Used — 0 1 0 1 0 | 1 1 1 | C X X X X X X R
Sense Device
17 214

DATA CHANNEL

First Data Table Location — 0 1 0 1 0 | 1 1 0 | E X T L H X X X
Initialize Read
17 215

1st Mpx Addr Table Location — 0 1 0 1 0 | 1 0 1 | X X X X X X X X
Initialize Write
17216 A
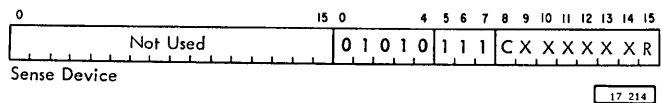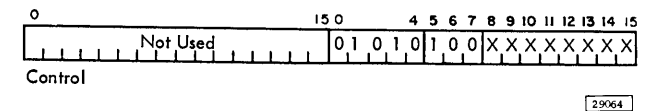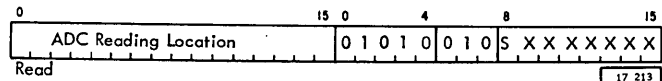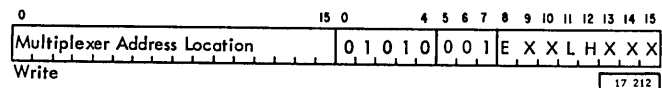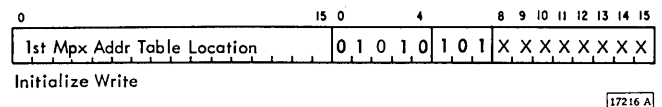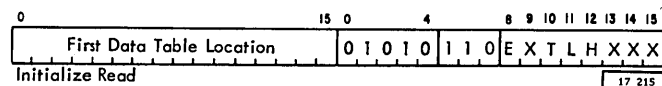
where:

01010   is the assigned Area for Analog Input.
XX   is not used.
C   a one bit specifies Comparator status word;
          no bit specifies Analog Input status word.
E   a one bit means External Synchronized.
L   a one bit specifies Low Resolution – 8 bit
          plus sign.
H   a one bit specifies High Resolution – 14 bit
          plus sign.
R   a one bit resets indicators.
S   a one bit specifies Sequential Programmed
          Mode.
T   a one bit specifies Two Data Channel
          Operation, Random Mode.

NOTES: 1. No L or H bit specifies 11 bit resolu-
tion. 2. The Area Code (01010) is replaced by
Area Code (10000) when AI Expander is used.

Data Table Formats

First Entry   17217
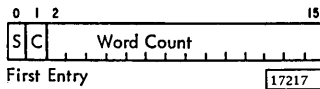
where SC are the Scan Control Bits

S   One bit causes chaining to occur.
C   No bit causes interrupt at end of Table.

Data Word   17235
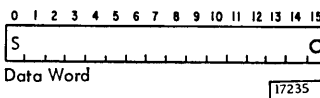
where:

S   Sign bit.
O   One bit indicates Overload.

Multiplexer Address   17 218
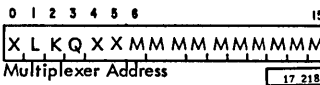
where:

X   Means not used.
K   a one bit means Perform Comparison (see
          Comparator).

L   a one bit means Limit Word follows
          (see Comparator).
Q   a one bit signifies Solid State Multiplexer;
          No bit, Relay Multiplexer.
M–M   Multiplexer Address.

Limit Word
(See Comparator)   17 219
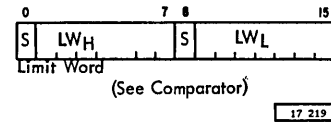
where:

S   is the sign bit.
LW_L is the Low Limit.
LW_H is the High Limit.

Device Status Format

The execution of an XIO Sense Device instruction
with the area code specifying Analog Input (01010)
or AI Expander (10000), when C (bit 8 of the
modifier) is a zero bit, will cause the Device Status
Word to be read into the accumulator. The bits of
the Device Status Word are:
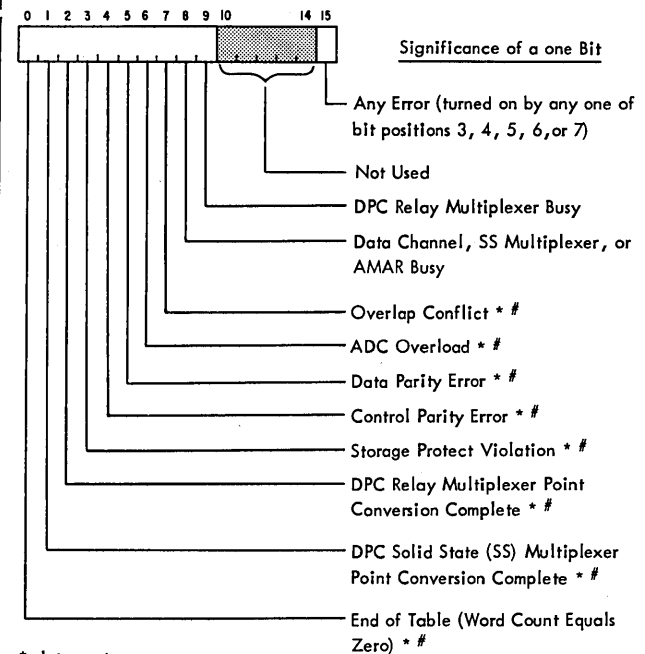
Significance of a one Bit

Any Error (turned on by any one of bit positions 3, 4, 5, 6, or 7)
Not Used
DPC Relay Multiplexer Busy
Data Channel, SS Multiplexer, or AMAR Busy
Overlap Conflict * #
ADC Overload * #
Data Parity Error * #
Control Parity Error * #
Storage Protect Violation * #
DPC Relay Multiplexer Point Conversion Complete * #
DPC Solid State (SS) Multiplexer Point Conversion Complete * #
End of Table (Word Count Equals Zero) * #

* Interrupt
# Indicator reset by a Sense DSW
  when IOCC bit 15 = 1.
  Other indicators are reset by
  their status turnoff.   23403

With a Comparator, an additional Device Status Word
is addressed by an XIO instruction (IOCC) with C (bit
8 of the modifier) as a one bit:

82

```
     0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
```
Significance of a one Bit

Multiplexer Point Address

Not Used

Solid State Multiplexer

Overload * #

Low out-of-limit * #

High out-of-limit * #

* Interrupt
# Indicator reset by a Sense DSW
  when IOCC bit 15 = 1.

`23404`
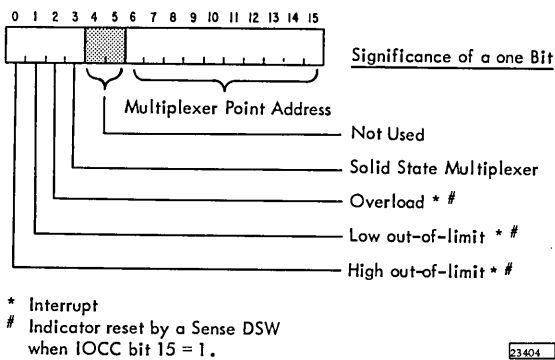
NOTE: All Analog Input basic interrupts are com-
bined into one interrupt signal assigned to an inter-
rupt level and ILSW bit; all Analog Input Expander
interrupts are combined into one interrupt signal
assigned to the same interrupt level as AI basic but
to a different ILSW bit. All Comparator (AI basic)
interrupts are combined into one signal assigned to
an interrupt level and ILSW bit; all Comparator (AI
Expander) interrupts are combined into one interrupt
signal assigned to the same interrupt level as AI
basic Comparator but to a different ILSW bit. Analog
Input and Comparator interrupts can be assigned to
the same or different interrupt levels.

Analog Input Indicators

End of Table: Turned on and causes an interrupt
when: (1) the end of a table is reached during a
Data Channel operation, and (2) the Scan Control
bits have specified an interrupt at the end of table.

DPC SS Conversion Complete: Turned on and causes
an interrupt in a Direct Program Control (DPC) op-
eration when a Solid State (SS) Multiplexer point con-
version is complete and the converted data is ready
to be transferred to core storage.

DPC Relay Conversion Complete: Turned on and
causes an interrupt in a DPC operation when a Relay
Multiplexer point conversion is complete and the con-
verted data is ready to be transferred to core storage.

Storage Protect Violation: Turned on and causes an
interrupt when the program tries to store converted
ADC data into a "read only" core storage location.
Analog input operations are halted.

Parity Control Error: Turned on and causes an inter-
rupt when a parity error is detected in control com-
mands and words. Analog input operations are halted.

Parity Data Error: Turned on and causes an inter-
rupt if a parity error is detected when multiplexer
address or converted data are transmitted between
the P-C and analog input interface.

ADC Overload: Turned on and causes an interrupt
when input to the ADC exceeds the range of the ADC
and the Comparator is not used. (See Comparator
Overload.)

Overlap Conflict: Turned on and causes an interrupt
when a second relay point is addressed before the
first relay point has been converted during a two
data channel overlap operation.

Data Channel SS, Mpx, or AMAR Busy: Turned on
when the SS Multiplexer is addressed, or during a
DC operation (relay or SS), or when the analog multi-
plexer address register (AMAR) is busy. The indi-
cator is turned off when the word count equals zero
with no chaining, or a DPC solid-state conversion is
completed, or AMAR is no longer busy. No new in-
struction can be initiated except Sense Interrupt Level,
Sense Device, or Control when this indicator is on.

DPC Relay Busy: Turned on when a Relay Multiplexer
is addressed by a Write function, or when a Relay
Multiplexer is sequenced by the sequence bit in the
modifier of a Read function. The indicator is turned
off 1.5 milliseconds after the relay conversion is
complete. A new relay point can be initiated after the
DPC Relay Conversion Complete interrupt has been
serviced. However, AMAR Busy is on for the 1.5
milliseconds. The SS Multiplexer can be used with
the Overlap feature when this indicator is on.

Comparator Indicators

High Out-of-Limit: Turned on and causes an inter-
rupt when the Comparator indicates an ADC reading
equal or above limits.

Low Out-of-Limit: Turned on and causes an inter-
rupt when the Comparator indicates an ADC reading
below limits.

Overload (Comparator): Turned on during a compare
operation if the input to the ADC exceeds its range.

Indicator Reset

Device Status Word indicators are reset when they
are sensed by a Sense Device XIO instruction, if bit
15 of the Sense Device IOCC is a one.

Blast Instruction

Analog Input Operations can be halted by executing a
control function. This control function XIO instruc-
tion resets all ADC basic controls and registers, the
ADC, Multiplexer and Comparator. If any XIO in-
struction was not completed, it is terminated, releas-
ing the AI subsystem for the next XIO instruction.

ANALOG INPUT EXECUTION TIMES

The following are typical times required for reading a series of analog input points. Note that times are shown for both core storage cycle times, 2 and 4 μsec. ADC conversion time is for 14-bit resolution. Eleven or 8-bit resolution is 8 and 15 μsec per point faster, respectively. The Comparator has no appreciable effect (one core storage cycle) on these times unless an out-of-limit occurs. No time is included for whatever program housekeeping may be necessary.

DIRECT PROGRAM CONTROL OPERATIONS

Multiplexer/R − ADC Model 1

Per Point	2 μsec	4 μsec
XIO Write	.010 ms	.020 ms
MPLX Relay	9.947	9.937
ADC Conversion	.043	.043
Interrupt	.110	.220
XIO Read	.010	.020
	10.0 ms	10.0 ms

Multiplexer/S (HLSE) − ADC Model 1

Per Point	2 μsec	4 μsec
XIO Write	10 μsec	20 μsec
SS MPLX and Buffer Amplifier	10	10
ADC Conversion	43	43
Interrupt	110	220
XIO Read	10	20
	183 μsec	313 μsec

Multiplexer/S (HLSE) − ADC Model 2

Per Point	2 μsec	4 μsec
XIO Write	10 μsec	20 μsec
SS MPLX and S & H Amplifier	10	10
ADC Conversion	43	43
Interrupt	110	220
XIO Read	10	20
	183 μsec	313 μsec

DATA CHANNEL OPERATIONS

One DC − MPLX/S − ADC Model 1

Initialize	2 μsec	4 μsec
XIO Initialize Read	8	16
Cycle Steal (CS) Word Count	4	8
CS Initialize MPLX ADDR	2	4
	14 μsec	28 μsec

Per Point		
SS MPLX and Buffer Amplifier	10.0 μsec	10.0 μsec
ADC Conversion	43.0	43.0
Wait	50.0	50.0
CS Read Data	2.5	5.0
	105.5 μsec	108.8 μsec

Chaining		
CS New ADDR	4 μsec	8 μsec
CS CAR Check	4	8
CS Word Count	4	8
CS MPLX ADDR	4	8
	16 μsec	32 μsec

One DC − MPLX/S − ADC Model 2

Initialize and Chaining times are the same as those for the preceding One DC − MPLX/S − ADC Model 1 times.

Per Point		
SS MPLX and S & H Amplifier	10 μsec	10 μsec
ADC Conversion	43	43
CS Read Data	2.5	5
	55.5 μsec	58 μsec

Two DC's − MPLX/S − ADC Model 1

Initialize		
XIO Initialize Read	8 μsec	16 μsec
XIO Initialize Write	8	16
CS Word Count	4	8
CS MPLX ADDR	2	4
	22 μsec	44 μsec

Per Point

SS MPLX and Buffer		
Amplifier	10.0 μsec	10 μsec
ADC Conversion	43.0	43
Wait	50.0	50
CS Read Data	2.5	5
	105.5 μsec	108 μsec

Chaining

CS New ADDR	2 μsec	4 μsec
CS CAR Check	4	8
CS New ADDR	4	8
CS CAR Check	4	8
CS Word Count	4	8
CS MPLX ADDR	4	8
	22 μsec	44 μsec

Two DC's — MPLX/S — ADC Model 2

Initialize and Chaining times are the same as those
for the preceding Two DC's — MPLX/S — ADC
Model 1 times.

Per Point

SS MPLX/S and S & H		
Amplifier	10.0 μsec	10 μsec
ADC Conversion	43.0	43
CS Read Data	2.5	5
	55.5 μsec	58 μsec

THERMOCOUPLE OPERATION

A thermocouple is a temperature-measuring device.
It develops an analog voltage which is related to the
temperature differential between the thermocouple
measuring junction and the thermocouple reference
junction. Therefore, the following information is
needed to measure a temperature with a thermo-
couple:

1. The millivolt output of the thermocouple circuit.
2. The temperature of the reference junction.
3. The calibration data for the thermocouple.

Because of the interrelationship of these three quan-
tities, care must be taken in correlating the meas-
ured signal to the actual temperature that it repre-
sents.

An 1851 Model 2 terminal is used to terminate
the thermocouple signal and provide thermal stability
to the reference junctions. An RBT (Resistance Bulb
Thermometer) is provided to determine this tempera-
ture. The calibration data for the thermocouple is
available from the manufacturer or from testing
laboratories.

Measuring Thermocouple Signals with the 1800

The 1800 is connected to each process thermocouple
via the 1851 Model 2 Multiplexer Terminal. The
thermocouple measuring junction is located in the
process area where temperature sensing is desired,
and the reference junction is located on the 1851
Model 2 terminal block. The reference junction ter-
minations are extended to signal conditioning elements
in the 1851. From this point, the multiplexer selec-
tively connects these signals to the ADC to be con-
verted to a digital value.

Resistance Bulb Thermometer (RBT)

Essentially, an RBT is a wire-wound resistor whose
electrical resistance varies with temperature. The
resistor is electrically connected to a precision ref-
erence voltage and a Wheatstone bridge (balanced
circuit). A temperature variation causes a change in
resistance and a consequent unbalance of the bridge
circuit. The RBT circuit provides two signals for
1800 program evaluation; the voltage produced by the
unbalance of the bridge circuit and the RBT reference
voltage. Thus, not only are thermocouple signals
compensated for reference junction temperature
changes, but the reference voltage value itself is read
by the computer to permit temperature compensation
for the RBT supply voltage variations that occur be-
cause of these temperature changes.

Thermocouple Programming and Conversion

The conversion of a thermocouple signal to a meaning-
ful and accurate temperature value is performed as
part of the 1800 Processor-Controller program. The
signal from the thermocouple circuit, the two signals
from the RBT at the reference (cold) junction, plus
the related thermocouple and RBT operating charac-
teristic data provide the parameters for correlating
these signals to temperature values.

Thermocouple operating characteristic data
is supplied in a graph or table forms for each
thermocouple type. This data is expressed as a
hot junction temperature-to-millivolt relationship
at a specified, and constant, cold junction tem-
perature. Data for the RBT supplied with the

1851 Model 2 Thermocouple Terminating Block is
given below in Step 5.

Three points should be stressed about the con-
version procedure which follows:

1. It is recognized that there are other means to
    convert thermocouple signals,
2. The procedure below is valid only when the RBT
    supplied with the 1851 Model 2 is used, and
3. Each thermocouple type must be separately cor-
    related, i.e., their curves and operating ranges
    are different.

Figure 28 depicts the operating curve of an iron-
constantan thermocouple. Normally, a thermocouple
graph shows only one curve at a stated reference
junction temperature. Here, two curves are in-
cluded to show the relative influence of the cold junc-
tion temperature on the measured signal.

For a computer conversion procedure, it is de-
sirable to consider a curve as being formed by a
series of short, straight line segments. This seg-
mentation is required because thermocouple millivolt
output is not a straight line relationship with respect
to measured temperature, particularly at the upper
end of the thermocouple temperature range. Smaller
segments, of course, provide a closer approximation
within each segment.

Study the thermocouple temperature-to-millivolt
curve (or table) and determine the number of seg-
ments or divisions that must be made to obtain the
desired degree of accuracy. For example, the iron-
constantan thermocouple curve shown in Figure 28
covers a temperature range of -50 to +850°C. This
range may be divided into nine segments as follows:

          -50 to +50
           50 to 150
          150 to 250
          250 to 350
          350 to 450
          450 to 550
          550 to 650
          650 to 750
          750 to 850

In order to correlate this operational curve to an
actual temperature by computer programming,
several intermediate values must be determined.
The following steps will accomplish this task. Steps
1 through 4 are done once for each thermocouple
type in the system.

At this point, it is well to have two relationships
well in mind. First, the relationship of amplifier
gain v.s. amplifier range (see section for Differential
Amplifier), and second, how the value read out of an
ADC is represented in Core Storage (see section for
Analog-Digital Converter).

1. Since all thermocouple signals are converted to
    digital values, the use of ADC digital values,
    rather than millivolt values, facilitates the com-
    putation of actual temperatures.

    The relationship of the ADC digital value to
    the thermocouple voltage is expressed as:

    $$Q = \frac{V_T \, G}{K_{ADC}}$$

Where:

Q	= ADC reading in binary digits
V_T	= the voltage in the thermocouple cir- cuit in millivolts.
G	= gain of the differential amplifier used. G will be 500, 250 or 100.
K_{ADC}	= 0.30518 millivolts (a constant and equal to an ADC digital value of one bit).

2. Solve for the slope (A) of each segment

    $$A = \frac{\Delta \text{ degrees}}{\Delta \ Q}$$

Where:

Both Δ degrees and ΔQ are the included values
for each segment.
ΔQ was obtained in Step 1.
A has a dimension of "degrees per digit".

3. Solve for Y axis intercept (B) of each segment

    T   Temperature $= A\,(Q) + B$ or
                 $B = $ Temperature $-AQ = T-AQ$

where:

a. This is the equation of a segment referred to
    the temperature (or Y) axis.
b. "A" and "Q" were obtained previously.
c. "B" has a dimension of "degrees".

Temp.   Temp
  F   C

1652°   900° ▶
1472°   800° ▶
1292°   700° ▶
1112°   600° ▶
 932°   500° ▶
 752°   400° ▶
 572°   300° ▶
 392°   200° ▶
 212°   100° ▶
  32°   0° ▶
-148° -100° ▶

25°C (Reference)

0°C (Reference)

Signal in Millivolts

0   5   10   15   20   25   30   35   40   45   50

17603A
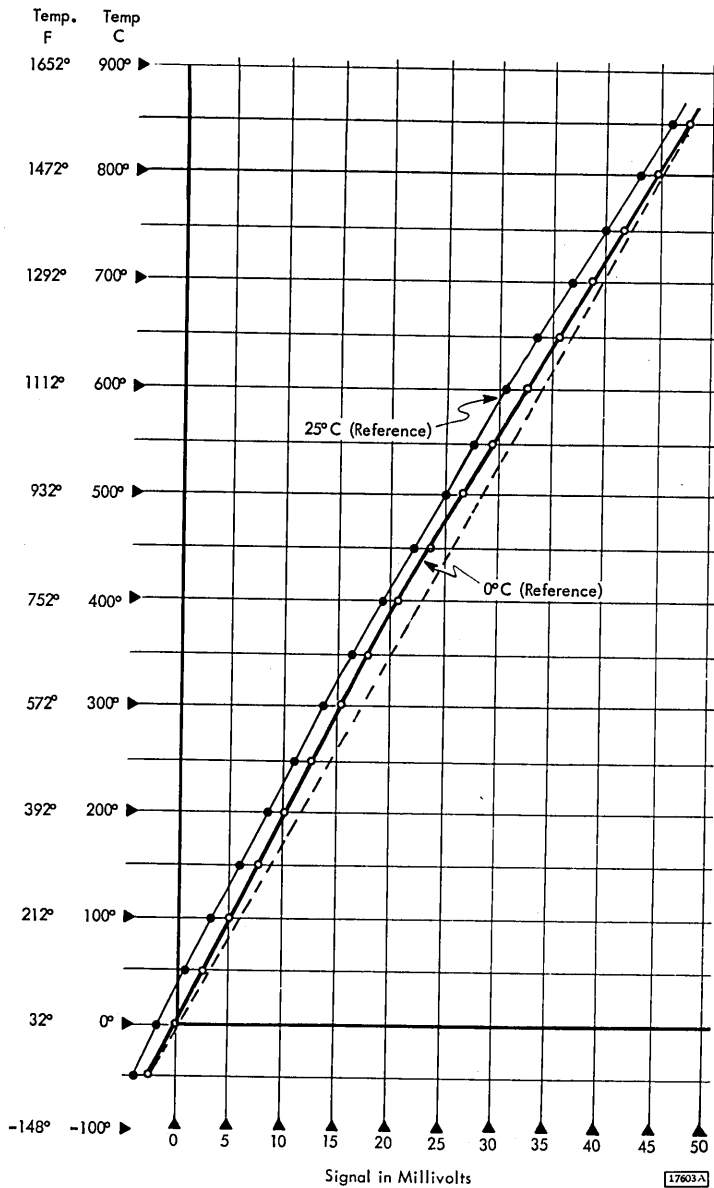
Figure 28. Iron-Constantan Thermocouple for -50°C to +850°C Range

d. T is in degrees corresponding to the same end points as Q.

4. For the segment that includes 25°C (approximate room temperature), solve for:

a. $C = \dfrac{1}{A}$

b. $D = \dfrac{-B}{A}$

Constants C and D define this segment relative to the signal (or X) axis.

"C" has a dimension of "digits per degree".

"D" has a dimension of "digits".

The above steps provide a "program image" of the thermocouple curve. Each thermocouple type used in a system must be similarly defined and correlated.

The following steps are the repetitive parts of the thermocouple signal-to-temperature conversion procedure. Steps 5 and 6 need to be made as frequently as the 1851 Model 2 ambient air temperature changes indicate and for the accuracy of measurement desired. Steps 7 and 8 are performed for each point on each multiplexer scan.

In the equations which follow:

T_{rbt} = RBT temperature

V_{rbt} = Q for RBT signal

V_r = Q for RBT reference voltage signal

R_{rbt} = Adjusted Q for T_{rbt}

V_{tc} = Q for thermocouple signal

R_{tc} = Adjusted Q for V_{tc}

T_{tc} = thermocouple temperature

5. Determine the temperature of the 1851 Model 2 terminating block. This is necessary to determine the influence that this temperature has on the:

   a. RBT reference voltage power supply

   b. RBT resistance element

Read both signals of the RBT circuit and use their Q values in the formula

$$T_{rbt} \, (^\circ C) = 28.82 \, \frac{V_{rbt}}{V_r} + 5.0$$

or

$$T_{rbt} \, (^\circ F) = 51.876 \, \frac{V_{rbt}}{V_r} + 41.0$$

to solve for the "RBT Temperature (T_{rbt})."

   c. At an amplifier gain of 100 (±50 mv range), typical magnitude ranges are:

      1) V_{rbt} from -1.0 mv to +50 mv.

      2) V_R from 15 mv to 25 mv.

   d. The values 28.82 and 5.0 (expressed in degrees centigrade) or 51.876 and 41.0 (expressed in degrees Fahrenheit) are constants for the RBT supplied with the thermocouple block.

6. Use the formula:

$$R_{rbt} = C(T_{rbt}) + D$$

   a. To obtain an adjusted Q value for the RBT (R_{rbt}), C and D were obtained in Step 4; T_{rbt} was obtained in Step 5.

   b. The digital value that will be algebraically included in the hot junction digital reading is obtained from this step.

7. Read the thermocouple signal, and use its Q value in the formula:

$$R_{tc} = V_{tc} + R_{rbt}$$

to obtain an "adjusted Q value (R_{tc})".

This step:

   a. Adjusts the hot junction digital reading by the amount of the influence due to the temperature of the cold junction.

   b. Establishes the correct segment of the thermocouple curve in which the true temperature value lies.

8. Use the formula:

$$T_{tc} = A(R_{tc}) + B$$

to compute the actual thermocouple temperature (T_{tc}). A and B are selected according to the Q value of R_{tc}, i.e., whatever segment the value of R_{tc} falls into, the A and B values are used from that segment.

Example of Thermocouple Conversion

Example: An iron-constantan (Type J) thermocouple is installed in a temperature region of 800°C. The signal range of the thermocouple is ±50 mv, therefore, the amplifier gain is 100. The A and B values for the segment that includes 800°C are: A = 0.04764, B = 89.6. The A and B values for the segment that includes 25°C are: A = .0609, B = -1.49. From Step 4: C = 16.42 and D = 24.47. Assume the RBT temperature (T_{rbt}) is 25°C; then from Step 6:

$$R_{rbt} = 434.97$$

Assume the Q value of the thermocouple is 15132:

$$R_{tc} = 15,567$$

and from Step 8:

$$T_{tc} = 831.21^\circ C$$

These features enable the Processor-Controller of the 1800 to accept real-time digital information in a digital format. The modular design of the feature permits individual system tailoring as to type and quantity of digital input data, such as:

Contact Sense	Mechanical Counters
Voltage Level Sense	Electronic Counters
Contact Interrupt	Rotary Switches from
Voltage Level Interrupt	operator
Digital Voltmeters	Sense Switches from
Special Analog-to-	operator
Digital Converters	Pulse Tachometers
Turbine Flowmeters	Frequency Meters
Shaft Encoders	Watt-Hour Meters
Electronic Register	Vibration Detectors
e.g., Telemetry	Weighing Devices

Digital Input is brought into the system in 16-bit groups. The format may be in any form. For example:

> Unrelated bits from Contact or Voltage levels
> Binary numbers
> Binary-coded-decimal digits
> Decimal digits
> Gray code digits

Any mixture of digital formats can be handled. Conversion from one base to another can be easily and quickly implemented by the P-C. Data input is via Direct Program Control or a Data Channel. One instruction is used in Direct Program Control to bring 16 bits of data into core storage. Where a Data Channel is used, one instruction initiates a cycle stealing operation that brings many 16-bit groups of data into core storage (one group per core storage cycle). The number of groups read – sequentially, randomly, or single address – as well as synchronization of the P-C to the input data is handled automatically.

Interrupt conditions from the process are a type of digital input. These Process Interrupts are brought into the P-C in 16-bit groups, with up to four priority levels of interrupt and four interrupt conditions per level for each 16-bit group.

High-speed 8-bit or 16-bit binary electronic pulse counters are available as special features. Counters are read into core storage as digital input groups, 16 bits at a time (two 8-bit counters or one 16-bit counter).

As shown in Figure 29 the combined capacity of the Digital Input and Pulse Counter features is 1024 bits, as follows:

> Digital Input
> 8 adapters x 8 Digital Input groups
> x 16 bits per group = 1024.

> Pulse Counter
> 8 adapters x 128 Pulse Counter bits
> per adapter (Pulse counters can be
> 8-bit or 16-bit counters) = 1024.

Any combination of the above may be used within the capacity of 1024 bits.

The capacity of the Process Interrupt feature is 24 priority levels or 384 bits, as follows:

> 8 adapters x 3 Process Interrupt groups
> (24 levels)
> x 16 bits per group = 384
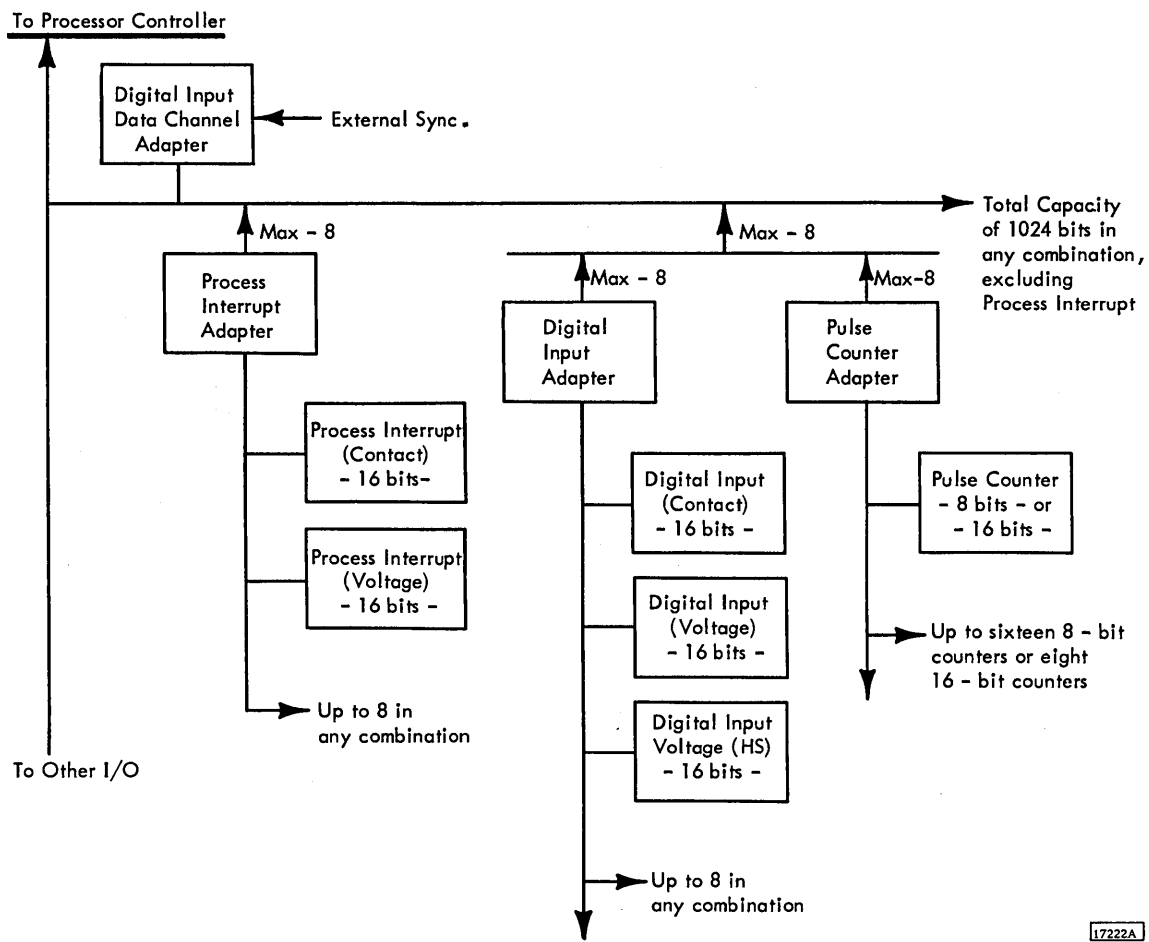
Figure 29. Digital Input Schematic

1826 DATA ADAPTER UNIT

This unit provides housing expansion of Digital Input and Digital Output points. There are two models: Model 1 is free standing, externally connected by cable. Model 2 is directly connected to a Model 1 or the Processor-Controller. Several Model 2's may be connected together.

DIGITAL INPUT UNITS AND FEATURES

The following units and features may be added to the system to provide Digital Input functions: For specifications, see 1800 Data Acquisition and Control System Installation Manual — Physical Planning.

DIGITAL INPUT DATA CHANNEL ADAPTER

This feature adapts digital input to a P-C Data Channel to enable digital input in the cycle stealing mode of operation.

Operation With External Sync

The Digital Input Data Channel Adapter provides the external sync function. An XIO instruction (Initialize Read-Synchronized) is executed to develop an external sync ready signal. When the external device senses the ready signal, it must transfer data to the addressed digital input group and then send an external sync signal to the Digital Input Data Channel Adapter. The external sync signal initiates a core-storage cycle to read the data into a core-storage word and turns off External Sync Ready.

An 8-bit in the modifier of an IOCC sets up the external sync mode.

The Digital Input feature will be interlocked under external sync until word count equal to zero for last external sync is obtained; however the P-C can execute instructions while the Digital Input feature is interlocked.

Operation Without External Sync

This mode of operation is initiated by execution of an XIO Initialize Read instruction when modifier bit 8 of the IOCC is zero. The speed of the digital input read operation is that of core storage, therefore the input operation will be completed prior to execution of the next instruction in the P-C.

DIGITAL INPUT

Digital input in the form of 16-bit groups can be handled by the Digital Input Adapter. Any logical grouping of 16 bits can constitute a Digital Input group. For example:

- 16 bits of status information
- 4 4-bit BCD digits
- 1 10-bit coded decimal digit and 6 bits of status
- 1 16-bit binary number

Two types of Digital Input bits can be terminated in groups of 16. One type operates in conjunction with a customer supplied process contact. The second type senses the level of a voltage supplied from the customer's equipment.

Screw-down type terminations are provided to terminate the customer's input wires. Input groups of 16 bits are available up to a total of 64 groups. Data comes in on two wires per bit. An input channel 16 bits wide for special consoles and other low speed devices can be made by selection of devices onto the channel via the Digital Output features.

An XIO command (IOCC) received by the Digital Input feature contains the address (Modifier) of a Digital Input group and selects the group to be read into core storage or the Accumulator. If a process contact is closed or the voltage level is positive, a one bit is placed in the designated bit position of that word. An open contact or negative level results in a 0 bit being sent. The first sense bit is located in bit position zero, the second sense bit in bit position one. This continues through the 16th bit which is in bit position 15 of the word. The Read function of the XIO instruction brings the addressed group into a core storage word and the Sense function brings the addressed group into the A-register (Accumulator). The Sense function is also used to read the digital input status word into the Accumulator. The status word contains the indicators for Digital Input.

Digital Input Adapter

The Digital Input Adapter is a prerequisite feature for Digital Input (Contact), Digital Input (Voltage), and High-Speed Digital Input. Each Digital Input Adapter provides for 128 bits of digital input. Each system can have a maximum of eight Digital Input Adapters.

Digital Input (Contact)

Digital Input (Contact) is available in groups of 16 two-wire contact input terminations. Read speeds up to 500,000 words per second are possible in burst mode when a Data Channel is used and a two micro-second core storage cycle is present. When an XIO instruction initiates reading a group of contacts, each closed contact reads a one bit into its respective bit position and each open contact reads a zero into its respective bit position.

Digital Input (Voltage)

Digital Input (Voltage) is available in groups of 16 two-wire voltage input terminations. Read speeds of up to 500,000 words per second are possible in burst mode when a Data Channel is used and a two micro-second core storage cycle is present. When an XIO instruction initiates reading a group of voltage inputs, each positive input reads a one bit into its respective bit position and each negative reads a zero into its respective bit position.

An optional high speed feature provides high repetitive reading speed for Digital registers. For example, telemetry registers may be coupled to the system using one or more modified voltage level groups, depending on register size and the number coding of the register. Conversion of the various number bases is accomplished via programming.

High-speed Telemetry Receiver registers may be read using the program mode of control (DPC) and an external interrupt for synchronization. Registers may be read by using a Data Channel synchronized by an external customer supplied sync signal.

Repetitive reading of the same group can proceed at rates up to 100,000 words per second.

Digital Input Channel

Process Operator Console (POC) input devices, such as decade switches and sense switches, and other low-speed inputs can be brought into the system by the formation of a Digital Input Channel using Electronic Contact Operate to select various groups of 16 bits over a single Digital Input Group. POC input devices and cabling are handled via RPQ.

PULSE COUNTER

Pulse Counter Adapter

The Pulse Counter Adapter is a prerequisite for adaptation of pulse counters. This feature provides for a maximum of sixteen 8-bit or eight 16-bit Pulse Counter features. A maximum of 8 adapters is available for each system.

A maximum of 128 eight bit (or 64 sixteen bit) Pulse Counters per system is available.

Pulse Counter

The Pulse Counter accepts discrete pulses as input information and advances by one per received pulse. The customer pulse is terminated by two-wire screw down termination at the individual counter terminal. These counters are read into the P-C in the same manner as a Digital Input group. Two 8-bit counters (or one 16-bit) are read from one address. (See section for Address Assignment for individual address assignments.) Either 8-bit or 16-bit binary counters are available. The counters are reset when they are read out.

PROCESS INTERRUPT

Process Interrupt Adapter

The Process Interrupt Adapter (see Interrupt section of manual) is a prerequisite for adaption of Process Interrupts (Contact) and Process Interrupts (Voltage). Each Process Interrupt Adapter provides for 48 interrupt points (Maximum - 8 Adapters per system).

Process Interrupt (Contact): Termination and sensing of 16 customer contacts associated with up to 4 levels of interrupt (Maximum - 24 groups per system).

Process Interrupt (Voltage): Termination and sensing of 16 customer voltage levels associated with up to 4 levels of interrupt latches (Maximum 24 groups per system).

Process inputs may exist in the form of isolated dry contact closures, [called Process Interrupt (Contact)], whereby IBM provides the sensing voltage for the contact, or if the form of a voltage level, [called Process Interrupt (Voltage)]. An interrupt is initiated by a contact closing, or a voltage level changing from negative to positive (0 bit to 1 bit). See Interrupt section of this manual.

DIGITAL INPUT ADDRESSING

An Address (IOCC Modifier) is assigned to each digital input group (16 points) and to each pulse counter (2 consecutive counters are assigned to each address) when the system is manufactured. Addresses assigned to Digital Input and Pulse Counters are 64-127. See the section for Address Assignment for the individual addresses assigned to digital input and pulse counter groups.

Digital Input

Digital input groups are assigned an address (IOCC Modifier) starting with address 64 for group 0 (16 points of the first Digital Input Adapter (DIA). Address 65 is assigned to group 1. This sequence of assignment continues through address 127 which is assigned to group 7 of the eighth Digital Input Adapter. Since Digital Input and Pulse Counters share the same group of addresses (IOCC Modifier), the total number (8 Adapters) of the two features is defined by the available addressing capacity (64 addresses): If 4 DIAs are ordered, a maximum of 4 Pulse Counter Adapters can be ordered.

Pulse Counter

Pulse Counters are assigned an address (IOCC Modifier) starting with address 127 being assigned to counters 0 and 1 (8-bit counters) or counter 0 (16-bit counter) of the first Pulse Counter Adapter. Address 126 is assigned to counters 2 and 3 (8-bit counters) or counter 2 (16-bit counter) of the first Pulse Counter Adapter. This sequence of assignment continues through address 64 for counters 14 and 15 (8-bit) or counter 14 (16-bit) of the eighth Pulse Counter Adapter. See the section Digital Input for maximum Pulse Counter Adapters.

Process Interrupt

Digital input from process interrupt occurs via the Process Interrupt Status Word (PISW) as described in the section for Interrupts. An address (IOCC Modifier) is assigned to each PISW when the system is manufactured. When ordering the system, the customer must specify (on the Process Interrupt Status Word Assignment Form) which 16 Process interrupt points (4 groups of 4 each) will be used with each PISW. See section Fixed Assignment for address assignment.

PROGRAMMED OPERATION

Digital input is processed by Direct Program Control (DPC) and/or the Data Channel (DC). When both operations exist, DPC may be used when the DC has completed its scan of the data table. The Digital Input Busy indicator is used to determine the status of the DC. DPC operation requires one XIO instruction for each Digital Input group (16 bits) to be transmitted to the Accumulator or core storage location. If a pulse counter is specified, the counter is reset.

When Digital Input is under DC one XIO function can be used. This function performs the following operation.

INITIALIZE READ
The Digital Input group(s), addressed by address word(s), in the data table(s) is read into core storage. If a Process Interrupt group is addressed, the data read in for that group will be blank.

When Digital Input is under DPC, three XIO functions can be used. These functions perform the following operations:

READ
The Digital Input group (or Process Interrupt Status word) addressed by the Modifier field is read into core storage.

SENSE
The Digital Input group (or Process Interrupt Status word) or the Device Status Word addressed by the Modifier field is placed in the Accumulator.

BLAST INSTRUCTION

DI operations can be halted by executing a control function. This XIO instruction resets all basic controls. If any operation is not completed, that operation is terminated, releasing the DI Subsystem and Data Channel for the next XIO instruction.

I/O CONTROL COMMANDS – DIGITAL INPUT

DIRECT PROGRAM CONTROL

0		15 0	4 5	7 8	10	15
	Address for Input Data	0 1 0 1 1	0 1 0	X A A A	A A A A	

Read

`17237`

0		15 0	4	8	15
	Not Used	0 1 0 1 1	1 1 1	X B B B B B B B	

Sense Device

`17239A`

0		15 0	4	8	15
	Not Used	0 1 0 1 1	1 0 0	X X 1 X X X X X	

Control

`29065`

DATA CHANNEL

0		15 0	4	8	15
	Address of Data Table	0 1 0 1 1	1 1 0	R R R X X X X X	

Initialize Read

`17240`
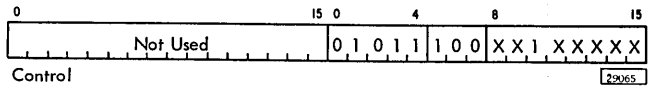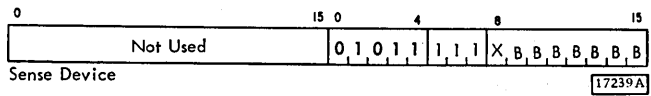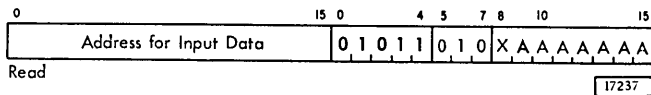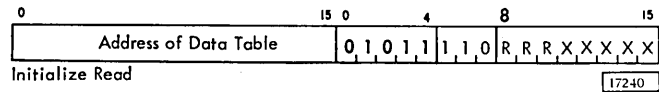
where:

01011   is the assigned Area code for Digital Input

X   is not used.

AA...A   is the address of the Digital Input Group or PISW. These addresses range from 64_{10} through 127_{10} for Digital Input groups and 2_{10} through 25_{10} for Process Interrupt Status words. See the section Address Assignment.

BB...B   0000000 and 0000001 are the addresses of the Digital Input Device Status Word. The indicators are reset by 0000001. Addresses 2_{10} through 25_{10} are assigned to the Process Interrupt Status Words. Addresses 64_{10} through 127_{10} are assigned to Digital Input and Pulse Counter groups. See the section Address Assignment.

RRR   These bits have the following meaning:

000   Read Random
001   Read Sequential
010   Read Single Address
100   Read Random and External Sync
101   Read Sequential with External Sync
110   Read Single Address with External Sync

Overlap of operations can be done in that Process Interrupts and status indicators (modifier addresses 0_{10} through 25_{10}) may be read or sensed via DPC during a DC operation on Digital Input groups. Note that this overlap can occur only during Data Channel operations with external sync since otherwise the Data Channel operation will be completed before any P-C instructions can be executed. The following points should be considered when programming such an overlap.

- An Initialize Read will terminate the Data Channel operation in progress and set the Command Reject indicator.

- A Read (DI-modifier address 64 through 127) will set the Command Reject indicator and will not be executed.

- A Read (PI-modifier address 2 through 25) will set the Command Reject indicator but will be executed correctly.

- A Parity error which causes an internal level interrupt as an XIO is being executed will terminate the Data Channel operation in progress.

Data Table Formats

First Entry

Address

16-bit Counter
or
Digital Input

Odd numbered Counter (8-bit)
Even numbered Counter (8-bit)
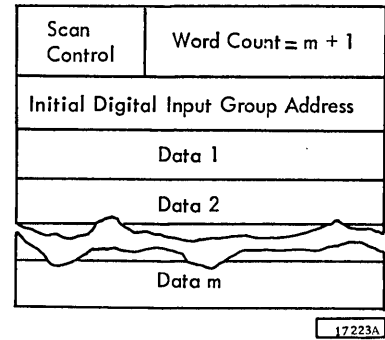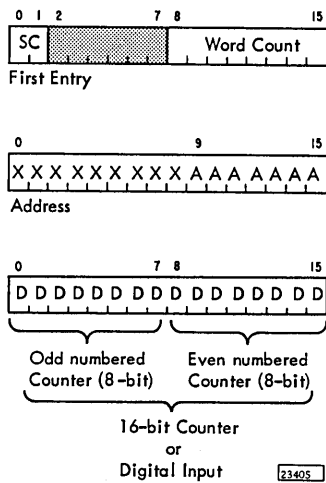
where:

SC	are the Scan Control bits.
X	is not used.
AA...A	is the address of the Digital Input group. The first group has an address of 64_{10}, the 64th group has an address of 127_{10}.
D	is data. For pulse counters: odd numbered counters bits 0 through 7 (8-bit counter); even numbered counters bits 8 through 15 (8-bit counter) or bits 0 through 15 (16-bit counter).

Data Table Layouts

The Address field of the IOCC used with the Data Channel operation specifies the location of the first word of the table. There are several table layouts which are described below. The first word in the table contains the word count and the chaining control.

When operating in the Sequential or Single Address mode, the second word in the table contains the initial Digital Input group to be read into core storage, and the succeeding table locations receive the data read over a Data Channel as shown in the following table.

Scan Control	Word Count = m + 1
Initial Digital Input Group Address	
Data 1	
Data 2	
Data m	

17223A

When READ Single Address is specified, the Initial Digital Input group is read over and over and placed in succeeding words of the table, until the word count reaches zero. When External Sync is specified, the cycle steal is initiated based on the External Sync pulse.

When operating in the Random mode, succeeding alternate words supply digital input addresses and receive data as shown in the following table.

Scan Control	Word Count = 2m
Digital Input Group Address$_1$	
Data 1	
Digital Input Group Address$_2$	
Data 2	
Digital Input Group Address$_m$	
Data m	

17224A
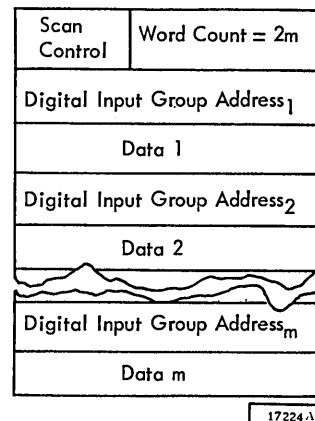
When the word count reaches zero, normal Scan Control applies as described in the I/O Control section of the manual. If chaining is used, a chain address (address of next table) word must follow the table. The first word of the next table must contain its own address to satisfy the CAR check as described in the Section for Data Channel Operation. An interrupt may be generated at the completion of the scan. The interrupt is called Digital Input Scan Complete.

TIMING: Digital Input groups will be read at the maximum rate of the channel unless a higher priority Data Channel request is honored. But timing restrictions due to filtering and customer load should be observed.

CAUTION: Chaining can lock out the P-C.

Device Status Word

An XIO Sense, specifying the Digital Input Area code (01011) and modifier address (00000 or 00001) will cause the Device Status word to be read into the Accumulator. The DSW bits are

Parity — turned on if even parity is encountered during data transfers to and from core storage or if a P-C parity error is detected during a chaining operation for any Digital Input instruction (Pulse Counter, Digital Input, Process Interrupt). This error terminates the operation.

Storage Protect — turned on if an attempt is made to write into a "read only" location. This error terminates the operation.

DI Scan Complete — turned on and causes an interrupt when the word count goes to zero in a DC operation and the Scan Control bits specify an interrupt.

DI Busy — Turned on when DI is in use on a DC as the result of an XIO Initialize Read instruction. Turned off when the DC is not busy. An XIO (Read or Initialize Read) executed when this indication (DI Busy) is on causes a command reject interrupt. If the XIO Read addressed a PI group, that group was read even though the command reject indicator was on.

Digital Input (DI) Device Status Word Format:
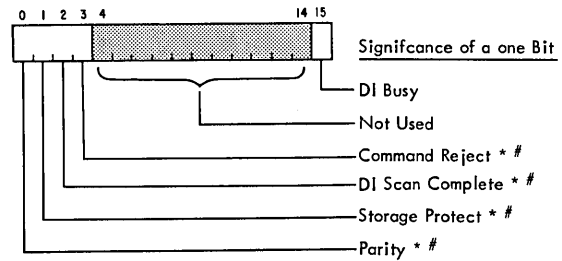
* Interrupt
# Indicator reset by a Sense DSW when IOCC bit 15 = 1. Other indicators are reset by their status turnoff.

96

The Digital and Analog Output (DAO) feature provides versatile control capability for the 1800 System. DAO features enable computer control over the many types of auxiliary devices required in a data acquisition or control system. Equipment that can be controlled includes set point positioners, displays, trend recorders, motor operated valves, and telemetry systems. The control outputs available with the DAO include the following:

1. Pulse Output (PO)
2. Electronic "Contact" Operate (ECO)
3. High-Speed Digital Register Output (RO)
4. High-Speed Analog Voltage Output (AO)

Pulse chaining and pulse-duration outputs are accomplished by programming.

The DAO features can communicate with the 1800 system via Direct Program Control (DPC) or a Data Channel (DC). A customer "external sync" pulse can be used to initiate DC operation.

Organization

The DAO features are organized as shown in Figure 30 and as described below:

1. The 1800 Processor-Controller (P-C) provides the basic control for the DAO features.
2. The DAO Data Channel Adapter enables communication between the P-C and DAO devices via a Data Channel (maximum of one Data Channel Adapter per system).
3. The Digital Output Control and the Analog Output Control provide the interface between the P-C and the output registers. A maximum of eight Controls, in any combination, can be attached:
    a. Each Digital Output Control can accommodate 16 output registers. Note in Figure 30 that a Digital Output Adapter is required for each 4 output registers. (The Digital Output features may be installed in either the P-C or the 1826 Data Adapter Unit.)
    b. Each Analog Output Control can accommodate 8 Digital-to-Analog Converters. (The Analog Output features are connected to the Processor-Controller through 1856 Analog Output Terminals.)

External Sync (Electronic)

This function is provided by the DAO Data Channel Adapter feature. An XIO instruction (initialize write-synchronized) is executed to load the addressed group with the data word. When the data word has been loaded, the External Sync Ready signal is turned on, signaling the external device that data is available.

The external device reads the data and then sends an External Sync signal to the DAO adapter, resetting the External Sync Ready signal and signaling that the external device is ready for another data word. This initiates a cycle steal request. At the completion of the cycle steal operation, the ready signal is turned "on" again.

When the last data word of a data table has been loaded (determined by the Word Count register in the DAO Adapter), normal scan control operations are inhibited until an External Sync signal is received from the external device, acknowledging that the word has been read by the external device.

The DAO busy indicator is on during the last data word until the last External Sync signals the adapter that the last word has been read.

An "8-bit" in the modifier of an IOCC sets up the external sync mode. The absence of an "8-bit" in the modifier terminates the external sync mode.

For specifications, see IBM 1800 Data Acquisition and Control System Installation Manual-Physical Planning.

System Capacity

The system capacity of DAO points depends on the combination of Digital Output (DO) and Analog Output (AO) points installed. Selection begins with the DO and AO Controls, maximum of eight:

1. If the maximum number of DO points are desired, seven DO Controls are installed. Each DO Control interfaces a maximum of four DO Adapters (2 adapters in 1801), providing a maximum of 26 DO Adapters. Each DO Adapter accommodates a maximum of four 16-bit registers, which is 104 registers, or 1664 bits. Installation of the DO maximum eliminates the possibility of AO points.
2. If the maximum number of AO points is desired, eight AO Controls are installed. Each AO Control interfaces eight Digital-to-Analog
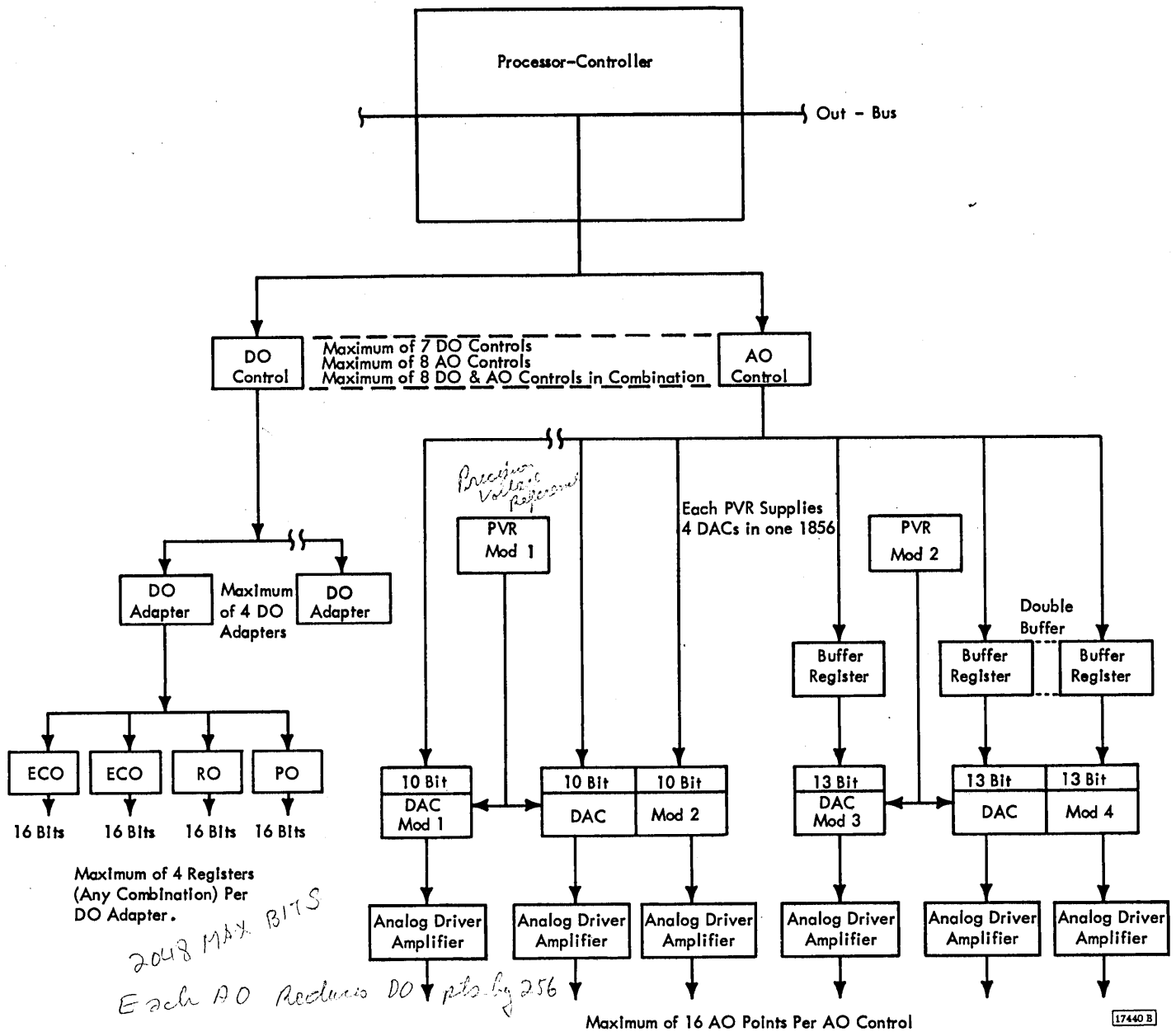
● Figure 30. Schematic of Digital and Analog Output Features

Converters (DAC's), with a maximum of 16 AO points. Each DAC provides one or two AO points, depending on the DAC mod. Thus, a maximum number of 128 AO points can be installed. Installation of the maximum number of AO points eliminates the possibility of DO points.

Note that one AO point equals one 16-bit digital output register and that a total system limit of 128 (AO points plus DO registers) exists.

Installation of single point DACs reduces the maximum of 128. Each DAC Mod 1 and each DAC Mod 3 provides only one AO point, reducing the 128 maximum by one for each mod 1 and 3 installed.

DIGITAL OUTPUT

Three types of digital output are available: Electronic "Contact" Operate, Pulse Output, and Register Output. For specifications see IBM 1800 Data Acquisition and Control System Installation Manual-Physical Planning.

Electronic "Contact" Operate .

ECO is used to operate alarms, console indicator lights and displays; and operating process equipment such as relays, solenoid valves, and DC motors. ECOs are provided in groups of 16 points (maximum 104 groups). The 16 points are set by a data transfer to the 16-bit register and remain latched until changed by another data transfer to the 16 bit register. A data bit of 1 corresponds to closed (conducting) and a data bit of 0 corresponds to open (nonconducting).

Process Operator Console (POC) output devices such as lights, digital displays, and other low speed outputs can be operated by the formation of a "Digital Output Channel" using Electronic "Contact" Operate to select various groups of 16 bits over a single group of Electronic "Contact" Operate. POC Output devices and cabling are handled via RPQ.

Pulse Output

The primary use of this output is to provide for pulse trains to operate such devices as latches, set point positioners, and other stepping motor devices. Pulse Outputs are provided in groups of 16 points (maximum 104 groups) and these are driven from each 16-bit register. The 16 points are set by a data transfer to the 16-bit registers. A data bit of 1 corresponds to closed (conducting) and data of "0" corresponds to open (nonconducting).

The outputs (with a data bit of 1) are "closed" immediately when the registers are loaded, and all are "opened" by the timing out of a 3-ms timer. The timer is started by using a separate XIO Control Function. In this manner pulse chains are accomplished by programming.

Specifications for Pulse Output are similar to ECO except for the duration of switch closure. The effective duration of switch closure can be increased or decreased by loading a 16-bit register before (increase duration) or after (decrease duration) the 3-ms timer is started. All pulse output points are

"opened" simultaneously. Repeated loading of a 16-bit register prior to the timer reset will cause the bits to be ORed in the data word previously loaded.

Register Output

Digital data is transferred from core storage to the Register Output feature. The Register Output feature has a maximum of 104 sixteen bit groups. The content of each output register is then transmitted to customer-owned devices, such as telemeter registers, for a register to register transfer.

ANALOG OUTPUT

There are two basic types of analog voltage outputs. The first type, DAC Mods 1 and 2 (10 bit), is a fast response unipolar DAC utilizing digital storage of a single level. The second type, DAC Mods 3 and 4 (13 bit), is a bipolar high speed, high accuracy DAC utilizing digital storage with a standard single level of buffering, and an option of double register buffering. Both types have the option of an Analog Output Driver Amplifier to provide low output impedance to match a wider variety of loads than the standard feature.

For both the 10-bit and 13-bit types, the Output Channel Register is force loaded to minimize DAC switching transients. This force loading means that the register goes directly from the previous value to the new value without being reset to zero in between.

DIGITAL-TO-ANALOG CONVERSION

There are four DAC Mods:

1. Mod 1 - Provides 10-bit digital-to-analog conversion for one analog output point.
2. Mod 2 - Provides two 10-bit converters for two analog output points.
3. Mod 3 - Provides 13-bit + sign conversion for one analog output point.
4. Mod 4 - Provides two 13-bit + sign converters for two analog output points.

A Precision Voltage Reference, Mod 1 or 2, is required to supply the DAC reference voltage.

Pulse output   3 ms pulses

XIO CONTROL STARTS 3ms Timer

XIO   "   TRANSFERS DATA WORD   1 BIT= PULSE   0 BIT No PULSE

3 ms TIMEOUT RESETS ALL POINTS STOPPING PULSE

DAC Mods 1 and 2

Installed in 1856 Terminals, DAC Mods 1 and 2 pro-
vide unipolar analog output from 10-bit resolution,
suitable for operating analog controllers, strip chart
recorders, and other displays. Mod 1 provides one
analog output point for a maximum of 64 points.
Mod 2 provides two separate Digital to Analog Con-
verters in one housing with separate output points
for each converter (maximum 128 output points).

DAC Mods 3 and 4

Installed in 1856 Terminals, DAC Mods 3 and 4 pro-
vide bipolar analog output from a resolution of 13
bits plus sign, suitable for hybrid systems. Nega-
tive numbers are handled in two's complement form.
Mod 3 provides one output point, for a maximum of
64 points. Mod 4 provides two separate Digital to
Analog Converters in one housing, with separate
output points for each converter (maximum 128 out-
put points). It is frequently a requirement in hybrid
computing and often an advantage in other applica-
tions to operate with several new values simultane-
ously. The Buffer Registers (one per analog output
point) are loaded as the data is received from the
P-C. An XIO Control instruction with a 9 bit is then
executed to transfer the contents of all buffer regis-
ters to their respective analog output registers
simultaneously.

Precision Voltage Reference (PVR)

The PVR feature is required to provide the precision
voltage reference to the DAC . It is installed in the
1856 Analog Output Terminal.
  Each Precision Voltage Reference supplies eight
analog output channels in the 1856. The PVR Mod 2
may be used with eight 10- or 13-bit resolution
analog outputs when it is desired to mix the two kinds
of outputs in a single terminal. It is more economi-
cal, however, to use the 10-bit resolution PVR Mod
1 for each full group of eight 10-bit output points.

Analog Output Driver Amplifier

The AO Driver Amplifiers provide a ±10 volt analog
output and permit operation of AO points with a wide
range of load impedances. The output impedance
of the DAC's is 10K ohms. To match loads differ-
ing greatly from this value, an output driver ampli-
fier having an output impedance of less than 0.6 ohm

may be used. This driver amplifier is applied on a
per point basis to provide load impedance matching
and voltage amplification. The driver amplifier is
also used to increase the DAC analog output voltage
from its normal 5 volts to 10 volts.

1856 Analog Output Terminals

There are two models of the 1856:
    Model 1 provides power and housing for four
    DAC's. It provides as many as eight AO points
    if only DAC Mods 2 and 4 are installed; and as
    few as four AO points if only DAC Mods 1 and 3
    are installed.
        The 1856 Model 1 provides control circuitry
    for eight DAC's, any mod. Thus, an 1856 Model
    1 is required for each multiple of eight DAC's.

    The 1856 Model 2 provides power and housing
    for four DAC's, any mod. One 1856 Model 2 can
    be installed for each 1856 Model 1 when the
    additional AO points are required. An 1856
    Model 2 cannot be installed without an 1856
    Model 1.

    A maximum of sixteen 1856s can be installed in
an 1800 system.

DAO PROGRAMMED OPERATION

Digital and Analog Output (DAO) data are handled
either by Direct Program Control (DPC) or Data
Channel (DC) control. For DPC operation one Output
Register is selected, and the digital data is transfer-
red from core storage to the register of the output
device using an XIO Write instruction. For DC opera-
tion a series of points are selected and data is trans-
ferred on a cycle steal basis using one XIO Initialize
Write instruction to initiate the operation.

I/O CONTROL COMMANDS - DIGITAL AND ANALOG OUTPUT

DIRECT PROGRAM CONTROL

0	15	0	4	8 9	15
Address of Output Data		0 1 1 0 0	0 0 1	X A A A A A A A	
Write					17243

```
0                    15 0    4    8 9        15
┌──────────────────┐  ┌──────────────────────┐
│     Not Used     │  │ 0 1 1 0 0 │ 1 0 0 │P B│C X X X X T│
└──────────────────┘  └──────────────────────┘
Control                                  17244B
```

```
0                    15 0    4    8          15
┌──────────────────┐  ┌──────────────────────┐
│     Not Used     │  │ 0 1 1 0 0 │ 1 1 1 │X X X X X X X Z│
└──────────────────┘  └──────────────────────┘
Sense Device                             17245A
```

DATA CHANNEL

```
0                        15 0    4    8        15
┌────────────────────┐  ┌──────────────────────┐
│ Address of Data Table│  │ 0 1 1 0 0 │ 1 0 1 │R R R X X X X X│
└────────────────────┘  └──────────────────────┘
Initialize Write                         17246
```
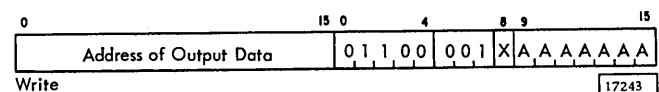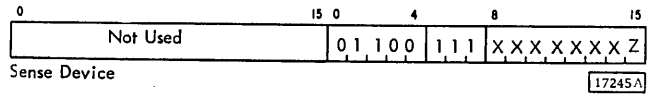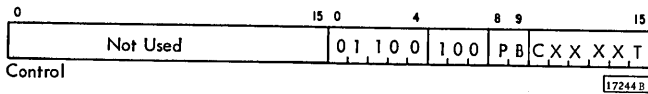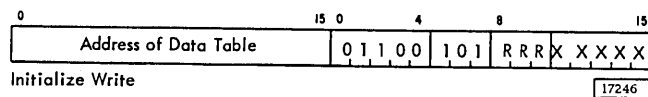
where:

01100	is the assigned Area code for Digital and Analog Output.
X	is not used.
AA...A	is the address of the digital or analog output register. (See Address Assignment section).
P	a one bit means initiate reset timer for all Pulse Output points.
B	a one bit means initiate simultaneous transfer from Buffer Registers to all analog output points operating with the Buffer Register feature.
RRR	these bits have the following meaning:
	000 – Write Random
	010 – Write Single Address
	100 – Write Random with External Sync
	110 – Write Single Address with External Sync
C	A one bit means reset all basic DAO controls, terminating any DAO operation in progress and releasing the Data Channel
Z	A one bit means reset interrupt indicators.
T	Test latch for Customer Engineer (diagnostic)

DATA TABLE FORMATS

```
0 1          7 8        15
┌──┬─────────┬───────────┐
│SC│░░░░░░░░░│ Word Count│
└──┴─────────┴───────────┘
First Entry          17247A
```

where SC are the Scan Control bits.

```
0                8 9        15
┌─────────────────────────┐
│X X X X X X X X X A A A A A A│
└─────────────────────────┘
Address                17248
```

```
0                            15
┌─────────────────────────────┐
│D D D D D D D D D D D D D D D D│
└─────────────────────────────┘
Digital Output Data
```

```
0              10      15
┌─────────────────────────┐
│X D D D D D D D D D X X X X X│
└─────────────────────────┘
10-Bit Analog Output Data
```

```
0                  13  15
┌─────────────────────────┐
│± D D D D D D D D D D D D X X│
└─────────────────────────┘
13-Bit Analog Output Data
                        29075
```
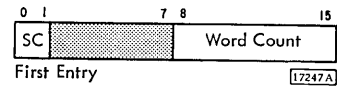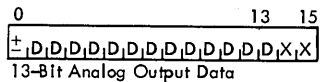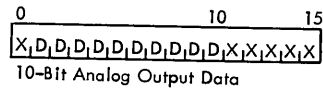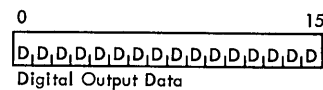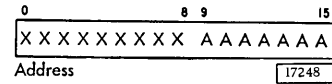
where X is not used, D is Data, and AA...A is the address of the digital or analog output register.

DATA TABLE LAYOUTS

The Address field of the IOCC used with Data Channel operation specifies the location of the first word of the table. There are several table layouts which are described below.

Write Random

When Write Random is specified, the first word in the table contains the word count (equal to two times the number of data words to be written) and the Scanning Control. The second word in the table contains the starting Digital or Analog Output address of the sequence of addresses to be scanned. The succeeding table locations contain the data to be converted and the DAO address, alternately, as shown in the following table:

101

Scan Control	Word Count = 2n
Initial D or A Output Address	
Data$_1$	
D or A Output Address	
Data$_2$	
~~	
D or A Output Addresses	
Data$_3$	
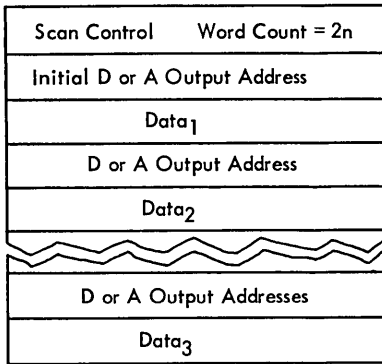
17228A

The total number of data and addresses transferred is specified by the word count. Data and Output Addresses are interleaved in the Table.

Write Single Address

When Write Single Address is specified, the word count equals the number of data words to be written plus one. The Output point is written over and over with succeeding words of data from the table until the word reaches zero as shown in the following table:

Scan Control	Word Count = n + 1
D or A Output Address	
Data 1	
Data 2	
~~	
Data n	
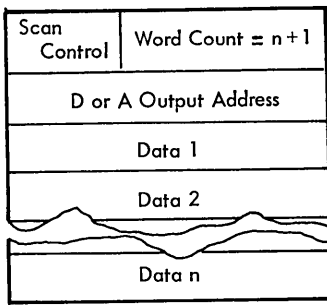
17229A

When external sync is specified, the cycle steal is initiated based on the external sync pulse.

When the word count reaches zero, the normal Scan Control chaining applies as described in the I/O Control section of this manual. An interrupt can be generated at the completion of the scan, depending on the scan control bits. The interrupt is called DAO Complete.

TIMING: Digital Output words can be written up to the maximum rate of the channel. The actual output data rate to customer devices is limited by the device characteristics and the repetition rate to the same outputs or to single outputs.

The rate can be controlled either by external synchronization or by programming, as specified by the output feature.

NOTE: Chaining can lock out the P-C.

Device Status Word

An XIO Sense, specifying the Area code of the DAO, will cause the Device Status word to be read into the Accumulator. The DSW indicators are:

Parity - Indicator is on if even parity is encountered during data transfers to and from core storage or if a P-C parity error is detected during a chaining operation. Causes an interrupt and terminates the DAO operation.

Pulse Output Timer - indicator is on whenever the pulse output timer is on.

DAO Scan Complete - turned on and causes an interrupt when the word count goes to zero in a Data Channel operation and the scan control bits specify an interrupt; turned off by XIO Sense Device instruction.

Command Reject - turned on if any XIO Write or Initialize Write instruction is issued while the DAO Busy indicator is on.

Data Channel Active - Indicator is active only with external sync operation. Turned on when DAO is in use on a Data Channel. Turned off (Data Channel is released) when the last word of the last data table has been transferred (prior to receipt of external sync).

DAO Busy - Turned on when DAO is in use on a Data Channel. Turned off when the last word of the last data table has been transferred and receipt of data is acknowledged if external sync is used.

Note: DAO Busy and Data channel active indicators turn off at same time unless external sync mode is specified.
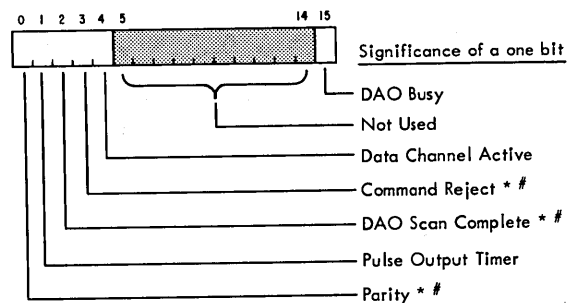
```
  0 1 2 3 4 5              14 15
 ┌──┬─────────────────────────┐
 │  │░░░░░░░░░░░░░░░░░░░░░░░░░░│   Significance of a one bit
 └──┴─────────────────────────┘
  │ │ │ │ │ │               └── DAO Busy
  │ │ │ │ │ └───────────────── Not Used
  │ │ │ │ └─────────────────── Data Channel Active
  │ │ │ └───────────────────── Command Reject * #
  │ │ └─────────────────────── DAO Scan Complete * #
  │ └───────────────────────── Pulse Output Timer
  └─────────────────────────── Parity * #
```

* Interrupt
# Indicator reset by a Sense DSW when IOCC bit 15 = 1. Other indicators are reset by their status turnoff.

23407

Blast Instruction

Digital and Analog output operations can be halted by executing a Control Function, XIO instruction. This instruction resets all basic controls (DO and AO output registers are not reset). If any Digital or Analog output external sync operation is not complete, that operation is terminated and the Digital-Analog subsystem, including the Data Channel, is released. Another XIO instruction can then reinitialize the Digital or Analog output operation.

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The wide variety of I/O devices that can be ordered with the 1800 system make I/O device assignment an important part of ordering the system. This section provides information about assignments that are fixed (preassigned by IBM) and assignments that are to be made by the customer. The assignment forms listed below must be completed before an 1800 system can be manufactured.

- Process Interrupt Status Word Assignment Form

- Interrupt Level Status Word Assignment Form

In the sections that follow, address assignment is given for the maximum of each type I/O device.

FIXED ASSIGNMENT

Area Codes are preassigned by IBM to each type of I/O device that can be ordered for the system. The following is a list of those devices and their area codes. The numbers in parenthesis under Area Code are the binary values of the area codes.

I/O Device	Area Code
Console Operations	0 (00000)
1816/1053 Printers (First 4)	1 (00001)
1442 Card Read Punch (First)	2 (00010)
1054/1055 Paper Tape Units	3 (00011)
2310 Disk Storage (A1)	4 (00100)
2310 Disk Storage (A2)	8 (01000)
2310 Disk Storage (A3)	9 (01001)
1627 Plotter	5 (00101)
1443 Printer	6 (00110)
Analog Input (Basic)	10 (01011)
Digital Input (Digital and Pulse Count)	11 (01011)
Digital and Analog Output (DO, ECO, RO, AO)	12 (01100)

System/360 Adapter	13 (01101)
2401 or 2402 Magnetic Tape Units	14 (01110)
1816/1053 Printers (Second 4)	15 (01111)
1442 Card Read Punch (Second)	17 (10001)
Analog Input Expander	16 (10000)

Digital Input devices (Digital Input and Pulse Counters) use a preassigned group of addresses (IOCC Modifiers). The decimal value of these addresses ranges from 64 through 127. This group of addresses is shared by both Digital Input and Pulse Counters (Figure 31).

Address 64 is assigned to the first Digital Input group of the first Digital Input adapter. Address 65 is assigned to the second Digital Input group of the first Digital Input adapter. This sequence of assignment continues through address 127 which is assigned to the last Digital Input group of the eighth Digital adapter.

If Pulse Counters are ordered, Address 127 is assigned to counters 0 and 1 (8-bit counters) or to counter 0 (16-bit counter) in the first Pulse Counter adapter. Address 126 is assigned to counters 2 and 3 (8-bit counters) or to counter 2 (16-bit counter) in the first Pulse Counter adapter. (Eight-bit counters use two numbers per address; sixteen-bit counters use only one, even-numbered, counter per address.) This sequence of assignment continues through address 64 which is assigned to counters 14 and 15 (8-bit counters) or to counter 14 (16-bit counter) in the eighth Pulse Counter Adapter.

Each adapter ordered is assigned eight addresses in the manner given above. If an adapter is ordered but is not completely populated (for example, only four groups of points are ordered for an adapter), the remainder of the eight addresses for that adapter are not available to be used in another adapter.

Process Interrupt Status Words (PISWs) are a digital input but have their own group of addresses

Decimal Address				
Digital Inputs		↓	Pulse Counters	
Adapter	Group No. (16 pts. ea.)		Counter No. (2/Addr.)*	Adapter
First	0	64	15-14	Eighth
	1	65	13-12	
	2	66	11-10	
	3	67	9-8	
	4	68	7-6	
	5	69	5-4	
	6	70	3-2	
	7	71	1-0	
Second	0	72	15-14	Seventh
	1	73	13-12	
	2	74	11-10	
	3	75	9-8	
	4	76	7-6	
	5	77	5-4	
	6	78	3-2	
	7	79	1-0	
Third	0	80	15-14	Sixth
	1	81	13-12	
	2	82	11-10	
	3	83	9-8	
	4	84	7-6	
	5	85	5-4	
	6	86	3-2	
	7	87	1-0	
Fourth	0	88	15-14	Fifth
	1	89	13-12	
	2	90	11-10	
	3	91	9-8	
	4	92	7-6	
	5	93	5-4	
	6	94	3-2	
	7	95	1-0	
Fifth	0	96	15-14	Fourth
	1	97	13-12	
	2	98	11-10	
	3	99	9-8	
	4	100	7-6	
	5	101	5-4	
	6	102	3-2	
	7	103	1-0	
Sixth	0	104	15-14	Third
	1	105	13-12	
	2	106	11-10	
	3	107	9-8	
	4	108	7-6	
	5	109	5-4	
	6	110	3-2	
	7	111	1-0	
Seventh	0	112	15-14	Second
	1	113	13-12	
	2	114	11-10	
	3	115	9-8	
	4	116	7-6	
	5	117	5-4	
	6	118	3-2	
	7	119	1-0	
Eighth	0	120	15-14	First
	1	121	13-12	
	2	122	11-10	
	3	123	9-8	
	4	124	7-6	
	5	125	5-4	
	6	126	3-2	
	7	127	1-0	

*Sixteen-bit counters use even numbers (one counter number per address).

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●Figure 31. IOCC Modifiers for DIAs and PCAs

(IOCC Modifiers). 24 PISWs (16 points per PISW) are available. Address 2 is assigned to PISW 1. Address 3 is assigned to PISW 2. This sequence continues through address 25 which is assigned to PISW 24. Process interrupt points are assigned to a PISW on the Process Interrupt Status Word assignment form. See the section Additional Assignments.

Digital and Analog Output devices share a group of addresses (IOCC Modifiers). The decimal value of these addresses is 00 through 127. Each Digital Output Control ordered is assigned 16 addresses starting with address 127 for the first group of 16 points and address 126 for the second group of 16 points. This sequence of assignment continues through address 16 assigned to the last group of 16 points (in the seventh control). See Figure 32 for addresses.

The first and all odd numbered 1856s ordered must be Model 1. The second and all even numbered 1856s must be Model 2. Each 1856 Model 1 supplies controls to the next higher numbered 1856 Model 2. Address assignment is made for each 1856 Model 1. Sixteen addresses are assigned for each 1856 Model 1 ordered. Eight addresses are assigned to the 1856 Model 1 and eight addresses are assigned to the next higher numbered 1856 Model 2. If a Model 2 is not ordered, the addresses that would be assigned to the Model 2 are not available to be used by Digital Output. Addresses 00 through 15 are assigned to the first 1856 Model 1 and the first 1856 Model 2. Addresses 16 through 31 are assigned to the second 1856 Model 1 and the second 1856 Model 2. This sequence of assignment continues through Addresses 112 through 127 which are assigned to the eighth 1856 Model 1 and the eighth 1856 Model 2 (Figure 32).

Interval Timers are assigned a fixed location in core storage. The core storage locations are:

- 0004_{10} Interval Timer A

- 0005_{10} Interval Timer B

- 0006_{10} Interval Timer C

Interrupt Levels are assigned a fixed core-storage location. Each interrupt level has its own unique core-storage location which is used as the indirect address of a hardware forced BSI instruction. All interrupt levels except the Trace and CE interrupts have their own Interrupt Level Status Word:

Decimal-Address (Modifiers) — Left

DO Control	DO Adapter	Group No. (16 points each.)	Addr	DAC Mod 2 or 4 Output	DAC Mod 1 or 3 Output	DAC No. within 1856	1856
	Addresses 00 – 15 not available for DO		00	1st	1st	1	1st (Model 1)
			01	2nd			
			02	1st	1st	2	
			03	2nd			
			04	1st	1st	3	
			05	2nd			
			06	1st	1st	4	
			07	2nd			
			08	1st	1st	1	2nd (Model 2)
			09	2nd			
			10	1st	1st	2	
			11	2nd			
			12	1st	1st	3	
			13	2nd			
			14	1st	1st	4	
			15	2nd			
*7	28	3	16	1st	1st	1	3rd (Model 1)
		2	17	2nd			
		1	18	1st	1st	2	
		0	19	2nd			
	27	3	20	1st	1st	3	
		2	21	2nd			
		1	22	1st	1st	4	
		0	23	2nd			
	26	3	24	1st	1st	1	4th (Model 2)
		2	25	2nd			
		1	26	1st	1st	2	
		0	27	2nd			
	25	3	28	1st	1st	3	
		2	29	2nd			
		1	30	1st	1st	4	
		0	31	2nd			
6	24	3	32	1st	1st	1	5th (Model 1)
		2	33	2nd			
		1	34	1st	1st	2	
		0	35	2nd			
	23	3	36	1st	1st	3	
		2	37	2nd			
		1	38	1st	1st	4	
		0	39	2nd			
	22	3	40	1st	1st	1	6th (Model 2)
		2	41	2nd			
		1	42	1st	1st	2	
		0	43	2nd			
	21	3	44	1st	1st	3	
		2	45	2nd			
		1	46	1st	1st	4	
		0	47	2nd			
5	20	3	48	1st	1st	1	7th (Model 1)
		2	49	2nd			
		1	50	1st	1st	2	
		0	51	2nd			
	19	3	52	1st	1st	3	
		2	53	2nd			
		1	54	1st	1st	4	
		0	55	2nd			
	18	3	56	1st	1st	1	8th (Model 2)
		2	57	2nd			
		1	58	1st	1st	2	
		0	59	2nd			
	17	3	60	1st	1st	3	
		2	61	2nd			
		1	62	1st	1st	4	
		0	63	2nd			

Decimal-Address (Modifiers) — Right

DO Control	DO Adapter	Group No. (16 points each.)	Addr	DAC Mod 2 or 4 Output	DAC Mod 1 or 3 Output	DAC No. within 1856	1856
4	16	3	64	1st	1st	1	9th (Model 1)
		2	65	2nd			
		1	66	1st	1st	2	
		0	67	2nd			
	15	3	68	1st	1st	3	
		2	69	2nd			
		1	70	1st	1st	4	
		0	71	2nd			
	14	3	72	1st	1st	1	10th (Model 2)
		2	73	2nd			
		1	74	1st	1st	2	
		0	75	2nd			
	13	3	76	1st	1st	3	
		2	77	2nd			
		1	78	1st	1st	4	
		0	79	2nd			
3	12	3	80	1st	1st	1	11th (Model 1)
		2	81	2nd			
		1	82	1st	1st	2	
		0	83	2nd			
	11	3	84	1st	1st	3	
		2	85	2nd			
		1	86	1st	1st	4	
		0	87	2nd			
	10	3	88	1st	1st	1	12th (Model 2)
		2	89	2nd			
		1	90	1st	1st	2	
		0	91	2nd			
	9	3	92	1st	1st	3	
		2	93	2nd			
		1	94	1st	1st	4	
		0	95	2nd			
2	8	3	96	1st	1st	1	13th (Model 1)
		2	97	2nd			
		1	98	1st	1st	2	
		0	99	2nd			
	7	3	100	1st	1st	3	
		2	101	2nd			
		1	102	1st	1st	4	
		0	103	2nd			
	6	3	104	1st	1st	1	14th (Model 2)
		2	105	2nd			
		1	106	1st	1st	2	
		0	107	2nd			
	5	3	108	1st	1st	3	
		2	109	2nd			
		1	110	1st	1st	4	
		0	111	2nd			
1	**4	3	112	1st	1st	1	15th (Model 1)
		2	113	2nd			
		1	114	1st	1st	2	
		0	115	2nd			
	**3	3	116	1st	1st	3	
		2	117	2nd			
		1	118	1st	1st	4	
		0	119	2nd			
	2	3	120	1st	1st	1	16th (Model 2)
		2	121	2nd			
		1	122	1st	1st	2	
		0	123	2nd			
	1	3	124	1st	1st	3	
		2	125	2nd			
		1	126	1st	1st	4	
		0	127	2nd			

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* Not available when the first DO Control is in 1826.

** Not available when the first DO Control is in 1801.

● Figure 32. IOCC Modifiers for DOCs and 1856s

Interrupt Level	Priority	Core Storage Location
Internal	1	0008_{10}
Trace	26	0009_{10}
CE	27	0010_{10}
0	2	0011_{10}
1	3	0012_{10}
2	4	0013_{10}
3	5	0014_{10}
4	6	0015_{10}
5	7	0016_{10}
6	8	0017_{10}
7	9	0018_{10}
8	10	0019_{10}
9	11	0020_{10}
10	12	0021_{10}
11	13	0022_{10}
12	14	0023_{10}
13	15	0024_{10}
14	16	0025_{10}
15	17	0026_{10}
16	18	0027_{10}
17	19	0028_{10}
18	20	0029_{10}
19	21	0030_{10}
20	22	0031_{10}
21	23	0032_{10}
22	24	0033_{10}
23	25	0034_{10}

ADDITIONAL ASSIGNMENTS

Initial Program Load

(IPL) is assigned to <u>one</u> of two input devices:

    First 1442 Card Read Punch
    1054 Paper Tape Reader (if 1442 is not on
      system)

<u>Interval Timers</u> each must be assigned a time increment when the system is ordered (all three timers). Table 4 of this manual lists time increments that can be designated.

Data Channel Assignment

Data Channel (cycle steal) priorities are assigned by the customer when the system is ordered. The highest two priorities should be assigned to the 2401/2402 and the 2310 (first priority to the unit having the fastest data rate). This assignment is recommended to prevent the possibility of data loss or overrun for these two devices.

    If two Data Channels are assigned to one Analog-Digital Converter (Random Control or Comparator), Analog Input Data Channel Adapter 2 must have a higher priority than Analog Input Data Channel Adapter 1. I/O devices can share a Data Channel but devices sharing a Data Channel cannot be operated concurrently. I/O devices are assigned in two groups within the system and any devices sharing a Data Channel MUST be within the same group. The groups are:

1.   2401/2402 Magnetic Tape Units
    2310-A1 Disk Storage
    2310-A2 Disk Storage
    2310-A3 Disk Storage
    Analog Input Data Channel Adapter 1 (1801/2)
    Analog Input Data Channel Adapter 2 (1801/2)
2.   1442 Card Read Punch (Second)
    1443 Printer
    System/360 Adapter
    1442 Card Read Punch (First)
    Digital Input Data Channel Adapter
    Digital and Analog Output Data Channel Adapter
    Analog Input Data Channel Adapter 1 (1826)
    Analog Input Data Channel Adapter 2 (1826)

    The IBM systems programs assume that no Data Channel is shared.

    These are I/O devices that require a Data Channel.

- 2401/2402 Magnetic Tape Units

- 2310 Disk Storage, Models A1, A2, A3

- 1442 Card Read Punch

- 1443 Printer

- System/360 Adapter

I/O devices that do not use a Data Channel:

- 1816 Printer-Keyboard

- 1053 Printer

- 1627 Plotter

- 1054/1055 Paper Tape Reader and Paper Tape Punch

I/O devices that can be ordered with or without Data Channel operation:

- Digital Input

- Digital or Analog Output

- Analog Input

Process Interrupt Status Word Assignment

Process Interrupt points are assigned, in sets of four, to a Process Interrupt Status Word (PISW). Twenty-four groups (16 points each) of Process Interrupt are available. Each of these 16 point groups is divided into four sets of four points each for PISW assignment (0-3, 4-7, 8-11, and 12-15). Each set of four can be assigned to the same or to a different PISW. Each PISW can have 16 points assigned (4 sets of 4 each), and the positions of the PISW will correspond to the positions of the points assigned. For example: If the first four points (0-3) of a Process Interrupt group are assigned to PISW 1, they are assigned to positions 0-3 of the PISW 1. Once these four positions are assigned from one Process Interrupt group, they cannot be assigned to PISW 1 again from any other Process Interrupt group. Other groups of four points (4-7, 8-11, or 12-15) from the same or different Process Interrupt group(s) can be assigned PISW 1. Each PISW has its own address (IOCC Modifier) which is preassigned. See the sections Fixed Assignment and Interrupt.

Interrupt Level Status Word

Each external interrupt level has its own Interrupt Level Status Word (ILSW). An interrupt level requests service when one of the 16 positions of its ILSW contains a one bit. Since each interrupt level has a fixed priority (see the section Fixed Assignment), the customer can assign interrupt priority when he assigns devices to ILSW bit positions.

Devices are assigned to ILSW bit positions on the Interrupt Level Status Word assignment form. When a device is assigned to an ILSW bit, all of the interrupt conditions in the device's Device Status Word (DSW) are ORed into that ILSW bit. Thus, any interrupt condition in the DSW will change the assigned ILSW bit to a one. This is true for Process Interrupt Status Words (PISWs) also. Each PISW is assigned to an ILSW bit position, and an interrupt condition in any of the 16 PISW bits will set its ILSW bit to one.

A PISW or DSW must be assigned to one and only one ILSW bit position. For example, in the first group of four 1816/1053s, each device must be assigned to a different ILSW bit position of the same interrupt level and in the second group of four 1816/1053s each device must be assigned to a different ILSW bit position of the same interrupt level (can be the same level as the first group).

All IBM subroutines (except subroutines under the Time-Sharing Executive System) require that like devices be assigned to the same interrupt level. If the process interrupt routine in the Time-Sharing Executive program is used, each PISW must be assigned to its corresponding ILSW. For example, PISW 1 assigned to ILSW 0, PISW 2 assigned to ILSW 1, . . . and PISW 24 assigned to ILSW 23. The PISWs for any one Process Interrupt Adapter must be assigned within Interrupt level grouping of either 0-11 or 12-23. In addition, no more than one area code may be assigned to any one ILSW bit.

Console interrupt can be assigned any unused ILSW bit position on any available interrupt level.

The following interrupts must be assigned for all systems:

TI	Timer interrupt (combined interrupt signal from three interval timers)
Typ-1	First 1816 or 1053 (circuitry is basic in P-C)
2401/2	1802 only
CI	Console interrupt

The following interrupts must be assigned if any of the associated features are ordered for the system:

Typ-2		
Typ-3	1053s	
Typ-4		
Typ-5	1816 or 1053	Output Printer
Typ-6		Expander
Typ-7	1053s	
Typ-8		
DAO	Digital Analog Output	
DI	Digital Input (DI, PC, or PI)	

1442-1 First 1442 Adapter
1442-2 Second 1442 Adapter
1054/5 1054/1055
1627 1627 Controls
1443 1443 Controls
2310-1 2310 (first drive) Model A1, A2, or A3
2310-2 2310 (second drive) Model A2 or A3
2310-3 2310 (third drive) Model A3
360/CA System/360 Adapter
AIB Analog Input Basic (any ADC in 1801/2)
AIBC Analog Input Basic with Comparator (in 1801/2)
AIE Analog Input Expander (in 1826)
AIEC Analog Input Expander with Comparator (in 1826)

Assignment of devices to ILSWs should begin with the leftmost bit position (bit 0) and progress to the next higher bit position for each device assigned to that ILSW.

Analog Input (1851)

There are 1024 (0-1023) decimal addresses (Multiplexer Addresses) available for use with Analog Input. The first 256 addresses (0-255) are used by both Multiplexer/S and Multiplexer/R. Since these 256 addresses have a dual use, bit 3 of each Multiplexer Address Word is used to specify which multiplexer is being addressed (Multiplexer/S or Multiplexer/R). When bit 3 is a zero, Multiplexer/R is addressed. When bit 3 is a one, Multiplexer/S is addressed.

All Multiplexer/S groups are installed in the lowest numbered 1851s (1851s 1-4). Multiplexer/S will be followed by Multiplexer/R in the sequence listed below.

1. High Level
2. ±10 mv range
3. ±20 mv range
4. ±50 mv range
5. ±100 mv range
6. ±200 mv range
7. ±500 mv range

Addresses for each point within an 1851 are shown in Figure 33 for Multiplexer/S and Figure 34 for Multiplexer/R. Each 1851 ordered is assigned the 64 addresses shown in these two illustrations.

Multiplexer/S groups are installed in an 1851 in the following sequence: Group 0, group 1,

group 2, and group 3. For example, if two groups of Multiplexer/S are ordered, they are installed

Numbering Within 1851		1851s With Multiplexer/S			
Group Number	Point Number	1st 1851	2nd 1851	3rd 1851	4th 1851
0	00	00	64	128	192
	01	01	65	129	193
	02	02	66	130	194
	03	03	67	131	195
	04	04	68	132	196
	05	05	69	133	197
	06	06	70	134	198
	07	07	71	135	199
	08	08	72	136	200
	09	09	73	137	201
	10	10	74	138	202
	11	11	75	139	203
	12	12	76	140	204
	13	13	77	141	205
	14	14	78	142	206
	15	15	79	143	207
1	16	16	80	144	208
	17	17	81	145	209
	18	18	82	146	210
	19	19	83	147	211
	20	20	84	148	212
	21	21	85	149	213
	22	22	86	150	214
	23	23	87	151	215
	24	24	88	152	216
	25	25	89	153	217
	26	26	90	154	218
	27	27	91	155	219
	28	28	92	156	220
	29	29	93	157	221
	30	30	94	158	222
	31	31	95	159	223
2	32	32	96	160	224
	33	33	97	161	225
	34	34	98	162	226
	35	35	99	163	227
	36	36	100	164	228
	37	37	101	165	229
	38	38	102	166	230
	39	39	103	167	231
	40	40	104	168	232
	41	41	105	169	233
	42	42	106	170	234
	43	43	107	171	235
	44	44	108	172	236
	45	45	109	173	237
	46	46	110	174	238
	47	47	111	175	239
3	48	48	112	176	240
	49	49	113	177	241
	50	50	114	178	242
	51	51	115	179	243
	52	52	116	180	244
	53	53	117	181	245
	54	54	118	182	246
	55	55	119	183	247
	56	56	120	184	248
	57	57	121	185	249
	58	58	122	186	250
	59	59	123	187	251
	60	60	124	188	252
	61	61	125	189	253
	62	62	126	190	254
	63	63	127	191	255

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Figure 33. Multiplexer/S Addresses

Numbering Within 1851		1851s With Multiplexer/R															
Group Number	Point Number	1st 1851	2nd 1851	3rd 1851	4th 1851	5th 1851	6th 1851	7th 1851	8th 1851	9th 1851	10th 1851	11th 1851	12th 1851	13th 1851	14th 1851	15th 1851	16th 1851
0	00	00	64	128	192	256	320	384	448	512	576	640	704	768	832	896	960
	01	01	65	129	193	257	321	385	449	513	577	641	705	769	833	897	961
	02	02	66	130	194	258	322	386	450	514	578	642	706	770	834	898	962
	03	03	67	131	195	259	323	387	451	515	579	643	707	771	835	899	963
	04	04	68	132	196	260	324	388	452	516	580	644	708	772	836	900	964
	05	05	69	133	197	261	325	389	453	517	581	645	709	773	837	901	965
	06	06	70	134	198	262	326	390	454	518	582	646	710	774	838	902	966
	07	07	71	135	199	263	327	391	455	519	583	647	711	775	839	903	967
	08	08	72	136	200	264	328	392	456	520	584	648	712	776	840	904	968
	09	09	73	137	201	265	329	393	457	521	585	649	713	777	841	905	969
	10	10	74	138	202	266	330	394	458	522	586	650	714	778	842	906	970
	11	11	75	139	203	267	331	395	459	523	587	651	715	779	843	907	971
	12	12	76	140	204	268	332	396	460	524	588	652	716	780	844	908	972
	13	13	77	141	205	269	333	397	461	525	589	653	717	781	845	909	973
	14	14	78	142	206	270	334	398	462	526	590	654	718	782	846	910	974
	15	15	79	143	207	271	335	399	463	527	591	655	719	783	847	911	975
1	16	16	80	144	208	272	336	400	464	528	592	656	720	784	848	912	976
	17	17	81	145	209	273	337	401	465	529	593	657	721	785	849	913	977
	18	18	82	146	210	274	338	402	466	530	594	658	722	786	850	914	978
	19	19	83	147	211	275	339	403	467	531	595	659	723	787	851	915	979
	20	20	84	148	212	276	340	404	468	532	596	660	724	788	852	916	980
	21	21	85	149	213	277	341	405	469	533	597	661	725	789	853	917	981
	22	22	86	150	214	278	342	406	470	534	598	662	726	790	854	918	982
	23	23	87	151	215	279	343	407	471	535	599	663	727	791	855	919	983
	24	24	88	152	216	280	344	408	472	536	600	664	728	792	856	920	984
	25	25	89	153	217	281	345	409	473	537	601	665	729	793	857	921	985
	26	26	90	154	218	282	346	410	474	538	602	666	730	794	858	922	986
	27	27	91	155	219	283	347	411	475	539	603	667	731	795	859	923	987
	28	28	92	156	220	284	348	412	476	540	604	668	732	796	860	924	988
	29	29	93	157	221	285	349	413	477	541	605	669	733	797	861	925	989
	30	30	94	158	222	286	350	414	478	542	606	670	734	798	862	926	990
	31	31	95	159	223	287	351	415	479	543	607	671	735	799	863	927	991
2	32	32	96	160	224	288	352	416	480	544	608	672	736	800	864	928	992
	33	33	97	161	225	289	353	417	481	545	609	673	737	801	865	929	993
	34	34	98	162	226	290	354	418	482	546	610	674	738	802	866	930	994
	35	35	99	163	227	291	355	419	483	547	611	675	739	803	867	931	995
	36	36	100	164	228	292	356	420	484	548	612	676	740	804	868	932	996
	37	37	101	165	229	293	357	421	485	549	613	677	741	805	869	933	997
	38	38	102	166	230	294	358	422	486	550	614	678	742	806	870	934	998
	39	39	103	167	231	295	359	423	487	551	615	679	743	807	871	935	999
	40	40	104	168	232	296	360	424	488	552	616	680	744	808	872	936	1000
	41	41	105	169	233	297	361	425	489	553	617	681	745	809	873	937	1001
	42	42	106	170	234	298	362	426	490	554	618	682	746	810	874	938	1002
	43	43	107	171	235	299	363	427	491	555	619	683	747	811	875	939	1003
	44	44	108	172	236	300	364	428	492	556	620	684	748	812	876	940	1004
	45	45	109	173	237	301	365	429	493	557	621	685	749	813	877	941	1005
	46	46	110	174	238	302	366	430	494	558	622	686	750	814	878	942	1006
	47	47	111	175	239	303	367	431	495	559	623	687	751	815	879	943	1007
3	48	48	112	176	240	304	368	432	496	560	624	688	752	816	880	944	1008
	49	49	113	177	241	305	369	433	497	561	625	689	753	817	881	945	1009
	50	50	114	178	242	306	370	434	498	562	626	690	754	818	882	946	1010
	51	51	115	179	243	307	371	435	499	563	627	691	755	819	883	947	1011
	52	52	116	180	244	308	372	436	500	564	628	692	756	820	884	948	1012
	53	53	117	181	245	309	373	437	501	565	629	693	757	821	885	949	1013
	54	54	118	182	246	310	374	438	502	566	630	694	758	822	886	950	1014
	55	55	119	183	247	311	375	439	503	567	631	695	759	823	887	951	1015
	56	56	120	184	248	312	376	440	504	568	632	696	760	824	888	952	1016
	57	57	121	185	249	313	377	441	505	569	633	697	761	825	889	953	1017
	58	58	122	186	250	314	378	442	506	570	634	698	762	826	890	954	1018
	59	59	123	187	251	315	379	443	507	571	635	699	763	827	891	955	1019
	60	60	124	188	252	316	380	444	508	572	636	700	764	828	892	956	1020
	61	61	125	189	253	317	381	445	509	573	637	701	765	829	893	957	1021
	62	62	126	190	254	318	382	446	510	574	638	702	766	830	894	958	1022
	63	63	127	191	255	319	383	447	511	575	639	703	767	831	895	959	1023

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Figure 34. Multiplexer/R Addresses

in group 0 and group 1. Addresses are assigned to each 1851, so that in the above example, 32 addresses are assigned to group 0 and 1, and 32 addresses are reserved for groups 2 and 3.

Addresses for 1851s containing Multiplexer/R (Multiplexer/S and Multiplexer/R are not installed in the same 1851) are assigned as shown in Figure 34.

Multiplexer/R groups are installed in an 1851 in one of the following sequences, depending on the system configuration.

1. 1851s containing all high-level inputs or all the same low level range are installed in the following sequence: Group 0, group 1, group 2, and group 3.
2. 1851s containing high-level inputs and one low-level input range (maximum two ranges per 1851) are installed in the following sequence: High-level starting with group 0 and ascending, low-level starting with group 3 and descending. For example, if one group of high-level and three groups of ±10 mv range are ordered for the same 1851, the one group of high level is installed in group 0 and the three groups of ±10 mv range are installed in groups 3, 2, and 1. An exception to this sequence occurs when the groups of high-level inputs are installed in an 1851 Model 2. Since points 00 and 01 are reserved for reference voltage and RBT respectively in an 1851 Model 2, high-level groups are installed starting with group 3 and descending, and the thermocouple inputs are installed starting with group 0 and ascending (opposite of the above example). An 1851 Model 2 must have ±10 mv, ±20 mv, or ±50 mv range specified for group 0.
3. 1851s containing two ranges of low-level inputs have the first range installed in ascending order starting with group 0. The second range is installed in descending order starting with group 3. For example, if two groups of ±10 mv range and two groups of ±20 mv range are ordered, the two groups of the ±10 mv range are installed in groups 0 and 1, and the two groups of ±20 mv range are installed in groups 3 and 2.

The System/360 Adapter (located within the 1826) permits communication between the 1800 P-C and the System/360. Each system regards the other as an I/O device capable of requesting service on a random basis. The System/360 Adapter is functionally equivalent to the corresponding System/360 device, the channel-to-channel adapter.

The channel provides the ability to transfer blocks of data and/or programs at rates up to 250 kb (kilobytes) between the System/360 and the 1800 system.

Exercise caution when powering the 1800 system up or down to ensure that the System/360 Channel is not active. Failure to stop the System/360 before the power transition will force channel failures. If the System/360 Adapter happens to be the terminating (last) device on the channel, the channel will be inoperable during the entire power down time.

Addressing

The System/360 Adapter has two device addresses: one of which responds to the System/360 and one which responds to the 1800. The System/360 address is assigned at installation time. The 1800 address is fixed, area code of 01101. Each assignment conforms to the requirements of the two systems' channels.

Mode of Operation

The System/360 Adapter acts as a burst mode control unit on the System/360 channel and operates on a Data Channel with the 1800.

Data is transferred to or from the 1800, two 8-bit bytes at a time; data transfer to or from the System/360 channel occurs one 8-bit byte at a time. An 18-bit (16 data bits plus 2 parity bits) buffer register is provided for serializing and deserializing the data bytes. The left-hand byte of the buffer, corresponding to the more significant byte of the 1800 word, is loaded or transferred first over the System/360 channel.

The priority of the System/360 Adapter is selected for the 1800 by assigning a particular interrupt level and a particular Data Channel priority to the device. Control unit priority for the System/360 is governed by its position on the channel as defined in the System Reference Library publication, IBM System/360 Principles of Operation.

COMMANDS

The System/360 Adapter decodes and responds to seven System/360 commands and five 1800 commands. (See Table 8.)

The Read, Read Backward, Write, and Control command bytes, including modifier bits, of the System/360 and the Initialize Read or Initialize Write control words of the 1800, after being presented to the idle Adapter, are available to the programmer of the other system by use of their respective Sense commands.

The M bit being on in the System/360 Read or Write commands (Table 8) will suppress the 1800 interrupt normally caused by a System/360 command when loaded into the buffer. For example, the program for a System/360 initiated transfer may involve first, a Control command which identifies the desired operation via the modifier bits, then a Read or Write to complete the operation. These may or may not be chained. Both commands could be accepted by the Adapter buffer, and hence cause two interrupts in the 1800 system. The second interrupt (from the accepted Read or Write command) would be caused if the 1800 system response to the indicated operation (coded in the Control modifier bits) were delayed, either by the interrupt being masked, or perhaps a required intervening disk storage Seek operation. Thus, at the time the command byte following the Control arrives at the Adapter from the System/360, the Adapter would be in an idle condition and would latch the second command in the Adapter buffer. This operation normally causes an 1800 system interrupt to establish the presence of a command byte. The M-bit modifier then, is provided to suppress the interrupt for a Read or Write which could cause unnecessary interrupts in an exchange sequence such as described above.

The R bit being on the 1800 Sense DSW (Table 8), will reset the interrupting DSW bit.

● Table 8. Commands

1800 System Commands			System/360 Commands	
Func	Mod.			
101	XXXXXXXX	Initialize Write	Test I/O	XXXX0000
110	XXXXXXXX	Initialize Read	Write	XXXXXM01
111	0XXXXXXR	Sense DSW	Read	XXXXXM10
111	1XXXXXXX	Sense Word Count	Control	XXXXX111
011	XXXXXXXX	*Sense Interrupt Level	Sense	XXXX0100
100	XXXXXXXX	Control (Reset)	Read Backward	XXXX1100
			No Operation	XXXXX011

* Area Code not required to execute　　172308

NOTE: The interrupt due to the Read Backward command cannot be suppressed.

DEVICE STATUS

System/360 Status Byte

The System/360 Adapter presents the following device status information to the System/360:

Status Condition	System/360 Status Byte Bit Position
Attention	0
Busy	3
Channel End	4
Device End	5

In addition, the System/360 channel develops a status byte. The definition of these channel status bits are as defined in the Systems Reference Library publication, IBM System/360 Principles of Operation.

Attention: Indicates the condition, if on, that a prior Read or Write command function has been issued from the 1800 but that the System/360 has not issued the required complementary command.

Busy: The busy indication is off when the System/360 Adapter is idle. Busy on indicates that the device has been selected by the System/360 and an operation is pending, a transfer is in progress, or ending status has not been accepted.

Channel End: Presented to the System/360 during initial selection sequence for Control or No Op, or with Device End during the ending sequence for all other SIO commands.

Device End: Presented to the System/360 during the initial selection sequence for No Op, after an 1800 Sense DSW (with bit 15 on) command response to Control, or at the end of the data transfer for all other SIO commands.

1800 Device Status Word

The System/360 Adapter presents the following status information to a Sense DSW command from the 1800:

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

360 Command Byte

Significance of a one bit

End of Table * #
Transfer End * #
Storage Protect * #
Data Check * #
Halt * #
360 Command Stored * +
1800 Command Stored +
Command Reject * #
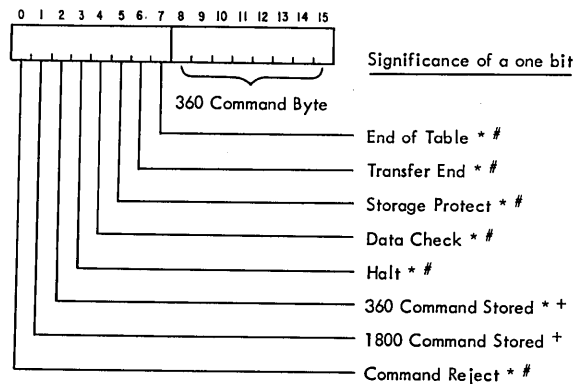
* Interrupt
\# Indicator reset by a Sense DSW when IOCC bit 15 = 1.
\+ Indicators reset by Transfer End indicator being turned on. 360 Command Stored is reset by Sense DSW (IOCC bit 15 = 1) only when command stored is a Control command.

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Command Reject: This bit on indicates that the System/360 Adapter refused an 1800 command for one of the following reasons:

1. Invalid Op Code.
2. An Initialize Read or Initialize Write was issued before a previous Initialize Read or Initialize Write had been cleared.
3. An Initialize Read was issued after the System/360 had issued a Read, Read Backward, or Control command.
4. An Initialize Write was sent after the System/360 had issued a Write or Control command.

This bit causes an 1800 interrupt and is reset after an 1800 Sense DSW with bit 15 on. This condition also causes an 1800 internal level interrupt.

If a Command Reject occurs when no 1800 command is stored, the word count register is reset to its maximum value. Such a reset can occur when Transfer End has been issued but not yet accepted.

1800 Command Stored: This bit is on whenever the System/360 Adapter has accepted an Initialize Read or Initialize Write from the 1800. It is reset when Transfer End occurs.

360 Command Stored: This bit on indicates that the System/360 has issued a Read, Read Backward, Write, or Control Command to the Adapter.

If the command is Read or Write, this bit will cause an interrupt in the 1800 unless suppressed by the System/360 command M bit being on or by a complemetary 1800 command waiting in the Adapter. An 1800 Sense DSW with bit 15 on will reset the interrupt. Transfer End resets the indicator bit.

If the command is Read Backward the response is identical to Read, as described above, except that the interrupt cannot be suppressed with the command M bit.

If the command is Control, this bit forces an interrupt in the 1800. An 1800 Sense DSW with bit 15 on will reset the interrupt and the indicator bit.

The 360 Command Stored indicator can be on at the same time as Transfer End, indicating that a new operation has been initiated by the System/360.

Halt: This bit causes an interrupt if the System/360 stops data transfer either with a normal stop or an interface disconnect sequence. Bit 6 (Transfer End) will also be on. This bit is reset after an 1800 Sense DSW with bit 15 is on.

Data Check: This bit on indicates that the 1800 detected a parity error during a cycle steal or the Adapter detected a System/360 bus out parity error. The Data Check causes an interrupt in the 1800 and is reset by an 1800 Sense DSW with bit 15 on.

If the error is detected during the first cycle steal of the operation (load word count cycle) and there is no complementary System/360 command stored, the Adapter is reset and the 1800 can reinitialize the data transfer operation.

If a parity error is detected during the first cycle steal operation (load word count cycle) and there is a complementary System/360 command stored or the parity error is detected during any subsequent cycle of the operation, an immediate ending procedure is initiated. The Adapter issues Device End and Channel End to the System/360, and Data Check and Transfer End to the 1800.

If the 1800 detects incorrect parity during the execution of the XIO command, the Adapter ignores the command and initiates no interrupts to either the 1800 or the System/360. This error causes an 1800 internal interrupt.

Storage Protect: This bit on indicates that the System/360 attempted to store data in a protected area in 1800 core storage on a 360 Write/1800 Read data cycle. This causes the System/360 Adapter to initiate an ending procedure, sending Channel End and Device End to the System/360, and Storage Protect

and Transfer End to the 1800. An interrupt is given to the 1800. This bit is reset by an 1800 Sense DSW with bit 15 on.

Transfer End: This bit on indicates that no additional data is to be transferred. This condition can be caused by any of the following conditions:

1. The 1800 Word Count goes to zero and no chaining is indicated.
2. The System/360 byte count has gone to zero.
3. The System/360 issues a Halt I/O instruction or executes an interface disconnect sequence.
4. Parity error is detected.
5. A storage protect violation has occurred.

This bit is reset by an 1800 Sense DSW with bit 15 on. (An 1800 Initialize Read or Write is rejected if the Transfer End status is on.)

End of Table: This bit will be turned on (if requested by the Scan Control bits) causing an interrupt, when the 1800 word count in the System/360 Adapter goes to zero. This bit is reset by an 1800 Sense DSW with bit 15 on.

360 Command Byte: If Bit 2 is on (360 Command stored) and Bit 1 is off (no 1800 command stored), bits 8 - 15 contain the issued 360 command byte. (See Table 8.) Note: These bits can be assumed to be zero only after a reset.

PROGRAMMED OPERATION

The System/360 Adapter performs with respect to the System/360 channel as described in the System Reference Library publication IBM System/360 Principles of Operation with the exception described below.

The System/360 Sense command stores in core storage at the address specified in the CCW up to two bytes of sense data under control of the byte count. The first byte contains the area and function of the 1800 I/O control word from the high order byte of the System/360 Adapter buffer. The next byte, from the low order buffer byte, contains the modifier bits of the I/O control word. All valid command codes from the System/360 are acceptable to the System/360 Adapter. The System/360 adapter rejects undefined command functions from the 1800 and identifies this occurrence by the Command Reject status bit presented in the device status word.

The following descriptions of System/360 I/O commands include statements regarding the resulting condition code. For the definition and application of these condition codes refer to the System Reference Library publication IBM System/360 Principles of Operation.

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CONTROL (SYSTEM/360)

Control as used in the System/360 Adapter is always
an immediate command. This means that Channel
End status is sent to the System/360 in response to
the initial selection (if the command is accepted),
thus freeing the channel if a chain flag is not pres-
ent. A Control from the System/360 may be re-
jected because the 1800 had previously commanded
the System/360 Adapter with an Initialize Read or
Write.

The modifier bits in the Control command byte
may be used to communicate the particular type of
transfer requested by the System/360. The Control
command is normally chained to a subsequent Read
or Write command, depending on the operation
necessary to complete the transfer.

Control to Idle Adapter: The System/360 initiated
the Control command. The complete command byte,
including modifiers, is latched in the Adapter. The
Adapter responds to initial selection with Channel
End status, thus freeing the System/360 channel,
and initiates an interrupt in the 1800. The condition
code in the System/360 resulting from the command
is status stored (1). The 1800, when interrupted,
can accept the request by executing an XIO Sense
DSW command to the Adapter. The XIO Sense DSW
command loads into the 1800 accumulator the Device
Status Word (DSW) containing the System/360 com-
mand byte from the buffer. A Device End status is
then sent to the System/360.

Control to a Busy Adapter: A Control from the
System/360 may be Busy rejected by one of three
conditions:

1. The Control could be issued by the System/360
   before a previous Control from the System/360
   had been cleared. The Adapter response would
   be Busy status causing a condition code of busy
   (2) for the SIO Control.
2. The Control could be issued by the System/360
   after a previous Control had been cleared but
   before the Device End had been accepted by the
   System/360. The response would be Busy and
   Device End status causing a condition code of
   status stored (1) for the SIO Control. This
   would clear the Device End from the Adapter
   and leave it idle.
3. The Control might be issued by the System/360
   after the 1800 had issued an Initialize Read or
   Initialize Write command to the Adapter. The
   Adapter would respond with Busy and Attention

status to the System/360 causing a condition
code of status stored (1) for the SIO Control.
The Attention, after being accepted in this way,
would no longer attempt to interrupt the System/
360. If another command, such as Control,
were issued from the System/360, the re-
sponse would still be Busy and Attention.

SENSE (SYSTEM/360)

The Sense command is the normal response to Atten-
tion status (an 1800 initiated transfer). The initial
status will be zero and ending status will be Device
End and Channel End. If the Adapter contains an un-
complemented 1800 command, the ending status will
also contain Attention. When a Sense command is
received by the Adapter, one or two 8-bit bytes are
transmitted to the System/360. The sense bytes
consist of the contents of the System/360 Adapter
buffer latches.

The Sense command data presented under alter-
native conditions is:

Condition	High-Order Buffer	Low-Order Buffer
	BYTE 1	BYTE 2
Adapter Idle	Undefined	Undefined
1800 Previously Issued:		
Initialize Read	Area/Function	Modifier
Initialize Write	Area/Function	Modifier
Control	Zero	Zero

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The only exception to the above is encountered when
the System/360 issues a Sense command to the
Adapter before a previous Control from the System/
360 had been cleared. If the Control had not been
answered by a Sense from the 1800, then the SIO
Sense command would receive Busy status, condition
code 2. If the Control had been answered, but the
Device End had not been taken, or had been stacked,
the Sense command would receive Busy and Device
End status causing a condition code 1, status stored.
This would clear the Device End from the Adapter
and leave it idle.

READ OR READ BACKWARD (SYSTEM/360)

The Adapter recognizes no difference between Read
and Read Backward from the System/360. In both

cases, the primary function of the Adapter is the transmission of data bytes to the System/360 from the 1800.

Read to an Idle Adapter: When the Read command is issued to an idle Adapter, the System/360 receives zero status response (condition code 0, operation initiated) and is then held up until the 1800 responds with an Initialize Write command. Unless suppressed with the M bit, a interrupt is set up to signal the 1800 that an operation is waiting. The complete Read command byte is latched in the Adapter buffer and is available to a Sense DSW command from the 1800.

Read to a Waiting Initialize Write: If a Read, issued by the System/360, encounters a previously issued Initialize Write from the 1800, both operations are performed. The System/360 receives zero initial status (condition code 0, operation initiated) whether the Attention is accepted or not. The operation continues until the System/360 byte count is zeroed, the Adapter word count is zeroed, or an error condition is detected. If neither channel is data chaining, status containing Channel End and Device End is issued to the System/360. The acceptance of the status by the System/360 frees the Adapter and returns it to idle.

Read to a Busy Adapter: There are three Busy responses to a Read command:

1. Busy status alone responds to the Read command if the System/360 had previously issued a Control command that was still in the Adapter. Condition code 2, busy.
2. Busy and Device End status is the response to a Read command if a previously issued Control command was cleared but the Device End had not been accepted. This clears the Device End and leaves the Adapter idle. Condition code 1, status stored.
3. Busy and Attention status is the response to a Read command from the System/360 if the 1800 had previously issued an Initialize Read. If the Attention was not previously accepted by the System/360, this clears it as an interrupting condition, although it would still appear as a response to another Read until the previously issued command from the 1800 is satisfied. Condition code 1, status stored.

WRITE (SYSTEM/360)

The function of the Write command is the transmission of data from the System/360 to the 1800.

Write to an Idle Adapter: When the Write command is issued to an idle Adapter, the System/360 will receive zero status response (condition Code 0, operation initiated) and will then be held up until the 1800 responds with Initialize Read.
    Unless suppressed by the M bit, an interrupt is generated to signal the 1800 that an operation is waiting. The Write command is latched in the Adapter and is available to a Sense DSW command from the 1800.

Write to a Waiting Initialize Read: If a Write command issued by the System/360 encounters a previously issued Initialize Read from the 1800, both operations are performed. System/360 receives Zero status (condition code 0, operation initiated) in response to its command. The operation continues until the System/360 byte count is zeroed, the Adapter word count is zeroed, or an error condition is detected. If neither channel is data chaining, ending status containing Channel End and Device End is issued to the System/360.
    The acceptance of the status by the System/360 frees the Adapter and returns it to idle.

Write to a Busy Adapter: There are three Busy responses to a Write issued by the System/360.

1. Busy status alone responds to the Write command if a previously issued Control command is still in the Adapter. Condition code 2, busy.
2. Busy and Device End status are the response to a Write command if a previously issued Control command was cleared but the Device End had not been accepted. This clears the Device End and leaves the Adapter idle. Condition code 1, status stored.
3. Busy and Attention status are the response to a Write command from the System/360 if the 1800 previously issued an Initialize Write. If the Attention had not been previously accepted by the System/360, this clears it as an interrupt condition, although it still appears as a response to another Write until the previously issued command from the 1800 is satisfied. Condition code 1, status stored.

TEST I/O (SYSTEM/360)

A Test I/O may be used by the programmer to determine the status of the System/360 Adapter any time the channel is free. The status received indicates the condition of the Adapter as follows:

1. A Zero status indicates that the Adapter is idle at the time of response. Condition code 0, available.
2. A Busy status indicates to the System/360 that a Control previously issued had not been accepted. Condition code 2, busy.
3. An Attention status indicates to the System/360 that the 1800 previously issued an Initialize Read or Initialize Write. Condition code 1, status stored.
4. A Device End status indicates that a previously issued Control was accepted, but that the final interrupting condition had not been accepted by the channel. This clears the Device End status and leaves the Adapter idle. Condition code 1, status stored.
5. Channel End and Device End status indicates that a data transfer has been terminated but that the final interrupting condition had not been accepted. This clears the status and leaves the Adapter idle. Condition code 1, status stored.

NO-OPERATION (SYSTEM/360)

The No-Operation command as used with the System/360 Adapter does not affect the contents of the Adapter latches. It is always handled as an immediate command.

No-Operation to an Idle Adapter: If a No-Operation is issued to an idle Adapter, the System/360 will receive a status response containing Channel End and Device End. No interrupt will occur in the 1800. Condition code 1, status stored.

No-Operation to a Busy Adapter: A No-Operation from the System/360 may be Busy rejected by one of the following three conditions:

1. A No-Operation could be issued by the System/360 before a previous Control is cleared. The Adapter response is Busy status (condition code 2, busy).

2. A No-Operation could be issued by the System/360 after a previous Control is cleared, but before Device End is accepted. The response is Busy and Device End. This clears the Device End and leaves the Adapter idle. Condition code 1, status stored.
3. The No-Operation might be issued by the System/360 after the 1800 had issued an Initialize Read or Initialize Write command to the Adapter. The adapter responds with Busy and Attention status to the System/360 (condition code 1, status stored).

HALT I/O (SYSTEM/360)

If Halt I/O is issued while a System/360 Read, Read Backward, Write, or Sense command is latched in the Adapter, the response is immediate. It terminates the operation, (condition code 2, burst operation terminated) sets Channel End and Device End in its status, and waits for a chance to send the status to the System/360. If the 1800 is operating with the Adapter, it receives Halt and Transfer End status via interrupt and a Sense DSW command.

If Halt I/O is issued while an unserviced System/360 Control is latched in the Adapter it will be Busy rejected (condition code 1, status stored).

If Halt I/O is issued to an idle Adapter, zero status is developed (condition code 1, status stored).

Status Summary (System/360)

The following chart summarizes the status information presented to the System/360 during initial selection.

360 Issues	Initial Status Presented			
	Idle	360 Control	1800 Read	1800 Write
Read or Read Backward	Zero	Busy and Device End*	Busy and Attention	Zero
Write	Zero		Zero	Busy and Attention
Control	Channel End		Busy and Attention	Busy and Attention
No-Operation	Channel End and Device End		Busy and Attention	Busy and Attention
Sense	Zero		Zero	Zero
Test I/O	Zero	Busy or Device End*	Attention	Attention

* Device End is conditional, refer to text. [23411]

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SENSE (1800)

Three Sense commands are recognized by the Adapter when issued by the 1800 system. A Sense function executed by the 1800 always presents 16 bits of information which are placed in the accumulator.

Sense Device Status Word (DSW): When the I/O control word bit 8 is equal to zero, the 1800 Device Status Word is presented. The various conditions and the corresponding information appearing in the 1800 accumulator in response to the unmodified Sense function are:

Condition	High-Order Accumulator	Low-Order Accumulator
Adapter Idle	Device Status	Undefined
System/360 has previously issued: Control Read Backward Read Write	Device Status	Command Byte
HALT I/O	Device Status	Zero
Transfer of Data	Device Status	Data Byte from Low - Order Buffer Byte
1800 has previously issued: Initialize Read Initialize Write	Device Status	IOCC Modifier

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The 1800 always responds to the Adapter interrupt by executing a Sense DSW command to identify the specific interrupt condition. Command bytes from the System/360 appear as follows in the eight low-order bits of the accumulator. This command resets all status bits except 1 and 2 if IOCC bit 15 is on.

Low Order Bits

System/360 has previously issued:	8	9	10	11	12	13	14	15
Control	X	X	X	X	X	1	1	1
Read Backward	X	X	X	X	1	1	0	0
Read	X	X	X	X	X	M	1	0
Write	X	X	X	X	X	M	0	1

Sense Word Count: A modified Sense command ("one" in bit position 8 of the control word) is provided to present the current word count of the 1800 Data Channel. The word count will be in true binary format. Following a reset, the word counter will contain maximum value, i.e., bits 2 through 15 on.

Sense Interrupt Level: Identification of a particular interrupt on any level is accomplished with a Sense Interrupt Level command.

INITIALIZE READ (1800)

This command, issued in conjunction with a Write command from the System/360, initiates data transfer from the System/360 to the 1800.

Initialize Read to Idle Adapter: Execution of this function latches the 16-bit portion of the IOCC containing the Area/Function/Modifier into the Adapter buffer, loads the Adapter word count, and raises Attention status to notify the System/360 that an operation is waiting.

Initialize Read to a Waiting Write: If an Initialize Read issued by the 1800 encounters a previously issued Write from the System/360, both operations are performed. The operation continues until either the System/360 byte count is zeroed, the Adapter word count is zeroed, or an error condition is detected. Terminating status will be Transfer End. The terminating status will also contain Halt if the System/360 terminated the data transfer.

Initialize Read to a Busy Adapter: There are two Busy responses to an Initialize Read command issued by the 1800:

1. Busy rejection is caused by issuing the command to a previously issued uncompleted command from the 1800. The resulting DSW condition is Command Reject and 1800 Command Stored; 360 Command Stored will also be on if a data transfer is in progress.
2. An Initialize Read to the Adapter, which contains a previously issued System/360 command other than Write is rejected. A sense DSW indicates Command Reject and 360 Command Stored.

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INITIALIZE WRITE (1800)

Issued to a System/360 Read command, Initialize
Write initiates data transfer. If the Adapter is idle,
the buffer is loaded with the I/O control word, the
word counter is loaded, and Attention is raised to
System/360. Busy and DSW response are the same
as those indicated under Initialize Read with the
Read/Write relationships reversed.

CONTROL (1800)

An 1800 Control command performs a reset of the
Adapter. The Adapter is not available to either
system for the duration of the reset.

NOTE: If the System/360 is using the Adapter
at the time of the reset, this command may cause
an Interface Control Check in the System/360.

The table in this appendix provides for direct conversion of decimal and hexadecimal numbers in these ranges:

HEXADECIMAL	DECIMAL
000 to FFF	0000 to 4095

For numbers outside the range of the table, add the following values to the table figures:

HEXADECIMAL	DECIMAL
1000	4096
2000	8192
3000	12288

HEXADECIMAL	DECIMAL
4000	16384
5000	20480
6000	24576
7000	28672
8000	32768
9000	36864
A000	40960
B000	45056
C000	49152
D000	53248
E000	57344
F000	61440
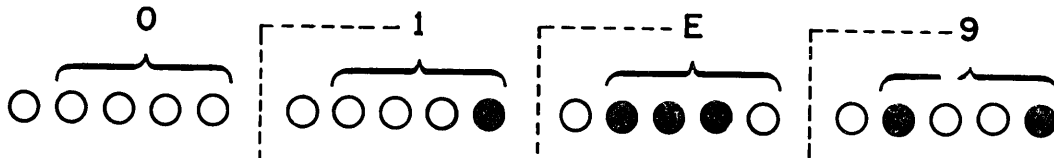
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00_	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
01_	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
02_	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
03_	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
04_	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
05_	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
06_	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
07_	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
08_	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
09_	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
0A_	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
0B_	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
0C_	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
0D_	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
0E_	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
0F_	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255
10_	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
11_	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
12_	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
13_	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
14_	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0332	0333	0334	0335
15_	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
16_	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
17_	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
18_	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
19_	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
1A_	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
1B_	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
1C_	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
1D_	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
1E_	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
1F_	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511

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	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
20_	0512	0513	0514	0515	0516	0517	0518	0519	0520	0521	0522	0523	0524	0525	0526	0527
21_	0528	0529	0530	0531	0532	0533	0534	0535	0536	0537	0538	0539	0540	0541	0542	0543
22_	0544	0545	0546	0547	0548	0549	0550	0551	0552	0553	0554	0555	0556	0557	0558	0559
23_	0560	0561	0562	0563	0564	0565	0566	0567	0568	0569	0570	0571	0572	0573	0574	0575
24_	0576	0577	0578	0579	0580	0581	0582	0583	0584	0585	0586	0587	0588	0589	0590	0591
25_	0592	0593	0594	0595	0596	0597	0598	0599	0600	0601	0602	0603	0604	0605	0606	0607
26_	0608	0609	0610	0611	0612	0613	0614	0615	0616	0617	0618	0619	0620	0621	0622	0623
27_	0624	0625	0626	0627	0628	0629	0630	0631	0632	0633	0634	0635	0636	0637	0638	0639
28_	0640	0641	0642	0643	0644	0645	0646	0647	0648	0649	0650	0651	0652	0653	0654	0655
29_	0656	0657	0658	0659	0660	0661	0662	0663	0664	0665	0666	0667	0668	0669	0670	0671
2A_	0672	0673	0674	0675	0676	0677	0678	0679	0680	0681	0682	0683	0684	0685	0686	0687
2B_	0688	0689	0690	0691	0692	0693	0694	0695	0696	0697	0698	0699	0700	0701	0702	0703
2C_	0704	0705	0706	0707	0708	0709	0710	0711	0712	0713	0714	0715	0716	0717	0718	0719
2D_	0720	0721	0722	0723	0724	0725	0726	0727	0728	0729	0730	0731	0732	0733	0734	0735
2E_	0736	0737	0738	0739	0740	0741	0742	0743	0744	0745	0746	0747	0748	0749	0750	0751
2F_	0752	0753	0754	0755	0756	0757	0758	0759	0760	0761	0762	0763	0764	0765	0766	0767
30_	0768	0769	0770	0771	0772	0773	0774	0775	0776	0777	0778	0779	0780	0781	0782	0783
31_	0784	0785	0786	0787	0788	0789	0790	0791	0792	0793	0794	0795	0796	0797	0798	0799
32_	0800	0801	0802	0803	0804	0805	0806	0807	0808	0809	0810	0811	0812	0813	0814	0815
33_	0816	0817	0818	0819	0820	0821	0822	0823	0824	0825	0826	0827	0828	0829	0830	0831
34_	0832	0833	0834	0835	0836	0837	0838	0839	0840	0841	0842	0843	0844	0845	0846	0847
35_	0848	0849	0850	0851	0852	0853	0854	0855	0856	0857	0858	0859	0860	0861	0862	0863
36_	0864	0865	0866	0867	0868	0869	0870	0871	0872	0873	0874	0875	0876	0877	0878	0879
37_	0880	0881	0882	0883	0884	0885	0886	0887	0888	0889	0890	0891	0892	0893	0894	0895
38_	0896	0897	0898	0899	0900	0901	0902	0903	0904	0905	0906	0907	0908	0909	0910	0911
39_	0912	0913	0914	0915	0916	0917	0918	0919	0920	0921	0922	0923	0924	0925	0926	0927
3A_	0928	0929	0930	0931	0932	0933	0934	0935	0936	0937	0938	0939	0940	0941	0942	0943
3B_	0944	0945	0946	0947	0948	0949	0950	0951	0952	0953	0954	0955	0956	0957	0958	0959
3C_	0960	0961	0962	0963	0964	0965	0966	0967	0968	0969	0970	0971	0972	0973	0974	0975
3D_	0976	0977	0978	0979	0980	0981	0982	0983	0984	0985	0986	0987	0988	0989	0990	0991
3E_	0992	0993	0994	0995	0996	0997	0998	0999	1000	1001	1002	1003	1004	1005	1006	1007
3F_	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
40_	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
41_	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
42_	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
43_	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
44_	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
45_	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
46_	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
47_	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
48_	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
49_	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
4A_	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
4B_	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
4C_	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
4D_	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
4E_	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
4F_	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
50_	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
51_	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
52_	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
53_	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
54_	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359
55_	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
56_	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
57_	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
58_	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
59_	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
5A_	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
5B_	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
5C_	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
5D_	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
5E_	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
5F_	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535

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	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
60 _	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
61 _	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
62 _	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
63 _	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
64 _	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
65 _	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
66 _	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
67 _	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
68 _	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
69 _	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
6A _	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
6B _	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727
6C_	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
6D_	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
6E_	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
6F_	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791
70 _	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807
71 _	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
72 _	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
73 _	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
74 _	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
75 _	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
76 _	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
77 _	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
78 _	1920	1921	1922	1923	1924	1925	1926	1927	1928	1929	1930	1931	1932	1933	1934	1935
79 _	1936	1937	1938	1939	1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951
7A _	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967
7B _	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
7C_	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
7D_	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
7E_	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
7F_	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
80 _	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063
81 _	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079
82 _	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095
83 _	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111
84 _	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127
85 _	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143
86 _	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159
87 _	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175
88 _	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191
89 _	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207
8A_	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223
8B_	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239
8C_	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255
8D_	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271
8E_	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287
8F_	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303
90 _	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319
91 _	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335
92 _	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351
93 _	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367
94 _	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383
95 _	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399
96 _	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415
97 _	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431
98 _	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2443	2444	2445	2446	2447
99 _	2448	2449	2450	2451	2452	2453	2454	2455	2456	2457	2458	2459	2460	2461	2462	2463
9A_	2464	2465	2466	2467	2468	2469	2470	2471	2472	2473	2474	2475	2476	2477	2478	2479
9B_	2480	2481	2482	2483	2484	2485	2486	2487	2488	2489	2490	2491	2492	2493	2494	2495
9C_	2496	2497	2498	2499	2500	2501	2502	2503	2504	2505	2506	2507	2508	2509	2510	2511
9D_	2512	2513	2514	2515	2516	2517	2518	2519	2520	2521	2522	2523	2524	2525	2526	2527
9E_	2528	2529	2530	2531	2532	2533	2534	2535	2536	2537	2538	2539	2540	2541	2542	2543
9F_	2544	2545	2546	2547	2548	2549	2550	2551	2552	2553	2554	2555	2556	2557	2558	2559

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	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
A0 _	2560	2561	2562	2563	2564	2565	2566	2567	2568	2569	2570	2571	2572	2573	2574	2575
A1 _	2576	2577	2578	2579	2580	2581	2582	2583	2584	2585	2586	2587	2588	2589	2590	2591
A2 _	2592	2593	2594	2595	2596	2597	2598	2599	2600	2601	2602	2603	2604	2605	2606	2607
A3 _	2608	2609	2610	2611	2612	2613	2614	2615	2616	2617	2618	2619	2620	2621	2622	2623
A4 _	2624	2625	2626	2627	2628	2629	2630	2631	2632	2633	2634	2635	2636	2637	2638	2639
A5 _	2640	2641	2642	2643	2644	2645	2646	2647	2648	2649	2650	2651	2652	2653	2654	2655
A6 _	2656	2657	2658	2659	2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2670	2671
A7 _	2672	2673	2674	2675	2676	2677	2678	2679	2680	2681	2682	2683	2684	2685	2686	2687
A8 _	2688	2689	2690	2691	2692	2693	2694	2695	2696	2697	2698	2699	2700	2701	2702	2703
A9 _	2704	2705	2706	2707	2708	2709	2710	2711	2712	2713	2714	2715	2716	2717	2718	2719
AA _	2720	2721	2722	2723	2724	2725	2726	2727	2728	2729	2730	2731	2732	2733	2734	2735
AB _	2736	2737	2738	2739	2740	2741	2742	2743	2744	2745	2746	2747	2748	2749	2750	2751
AC _	2752	2753	2754	2755	2756	2757	2758	2759	2760	2761	2762	2763	2764	2765	2766	2767
AD _	2768	2769	2770	2771	2772	2773	2774	2775	2776	2777	2778	2779	2780	2781	2782	2783
AE _	2784	2785	2786	2787	2788	2789	2790	2791	2792	2793	2794	2795	2796	2797	2798	2799
AF _	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809	2810	2811	2812	2813	2814	2815
B0 _	2816	2817	2818	2819	2820	2821	2822	2823	2824	2825	2826	2827	2828	2829	2830	2831
B1 _	2832	2833	2834	2835	2836	2837	2838	2839	2840	2841	2842	2843	2844	2845	2846	2847
B2 _	2848	2849	2850	2851	2852	2853	2854	2855	2856	2857	2858	2859	2860	2861	2862	2863
B3 _	2864	2865	2866	2867	2868	2869	2870	2871	2872	2873	2874	2875	2876	2877	2878	2879
B4 _	2880	2881	2882	2883	2884	2885	2886	2887	2888	2889	2890	2891	2892	2893	2894	2895
B5 _	2896	2897	2898	2899	2900	2901	2902	2903	2904	2905	2906	2907	2908	2909	2910	2911
B6 _	2912	2913	2914	2915	2916	2917	2918	2919	2920	2921	2922	2923	2924	2925	2926	2927
B7 _	2928	2929	2930	2931	2932	2933	2934	2935	2936	2937	2938	2939	2940	2941	2942	2943
B8 _	2944	2945	2946	2947	2948	2949	2950	2951	2952	2953	2954	2955	2956	2957	2958	2959
B9 _	2960	2961	2962	2963	2964	2965	2966	2967	2968	2969	2970	2971	2972	2973	2974	2975
BA _	2976	2977	2978	2979	2980	2981	2982	2983	2984	2985	2986	2987	2988	2989	2990	2991
BB _	2992	2993	2994	2995	2996	2997	2998	2999	3000	3001	3002	3003	3004	3005	3006	3007
BC _	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023
BD _	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039
BE _	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055
BF _	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C0 _	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087
C1 _	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103
C2 _	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119
C3 _	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135
C4 _	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
C5 _	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167
C6 _	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183
C7 _	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199
C8 _	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215
C9 _	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231
CA _	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
CB _	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263
CC _	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279
CD _	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295
CE _	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311
CF _	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327
D0 _	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343
D1 _	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359
D2 _	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375
D3 _	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391
D4 _	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407
D5 _	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423
D6 _	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439
D7 _	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455
D8 _	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471
D9 _	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
DA _	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503
DB _	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519
DC _	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535
DD _	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551
DE _	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567
DF _	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583

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	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E0 _	3584	3585	3586	3587	3588	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599
E1 _	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615
E2 _	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631
E3 _	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647
E4 _	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663
E5 _	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679
E6 _	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695
E7 _	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711
E8 _	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727
E9 _	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743
EA _	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759
EB _	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775
EC _	3776	3777	3778	3779	3780	3781	3782	3783	3784	3785	3786	3787	3788	3789	3790	3791
ED _	3792	3793	3794	3795	3796	3797	3798	3799	3800	3801	3802	3803	3804	3805	3806	3807
EE _	3808	3809	3810	3811	3812	3813	3814	3815	3816	3817	3818	3819	3820	3821	3822	3823
EF _	3824	3825	3826	3827	3828	3829	3830	3831	3832	3833	3834	3835	3836	3837	3838	3839
F0 _	3840	3841	3842	3843	3844	3845	3846	3847	3848	3849	3850	3851	3852	3853	3854	3855
F1 _	3856	3857	3858	3859	3860	3861	3862	3863	3864	3865	3866	3867	3868	3869	3870	3871
F2 _	3872	3873	3874	3875	3876	3877	3878	3879	3880	3881	3882	3883	3884	3885	3886	3887
F3 _	3888	3889	3890	3891	3892	3893	3894	3895	3896	3897	3898	3899	3900	3901	3902	3903
F4 _	3904	3905	3906	3907	3908	3909	3910	3911	3912	3913	3914	3915	3916	3917	3918	3919
F5 _	3920	3921	3922	3923	3924	3925	3926	3927	3928	3929	3930	3931	3932	3933	3934	3935
F6 _	3936	3937	3938	3939	3940	3941	3942	3943	3944	3945	3946	3947	3948	3949	3950	3951
F7 _	3952	3953	3954	3955	3956	3957	3958	3959	3960	3961	3962	3963	3964	3965	3966	3967
F8 _	3968	3969	3970	3971	3972	3973	3974	3975	3976	3977	3978	3979	3980	3981	3982	3983
F9 _	3984	3985	3986	3987	3988	3989	3990	3991	3992	3993	3994	3995	3996	3997	3998	3999
FA _	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012	4013	4014	4015
FB _	4016	4017	4018	4019	4020	4021	4022	4023	4024	4025	4026	4027	4028	4029	4030	4031
FC _	4032	4033	4034	4035	4036	4037	4038	4039	4040	4041	4042	4043	4044	4045	4046	4047
FD _	4048	4049	4050	4051	4052	4053	4054	4055	4056	4057	4058	4059	4060	4061	4062	4063
FE _	4064	4065	4066	4067	4068	4069	4070	4071	4072	4073	4074	4075	4076	4077	4078	4079
FF _	4080	4081	4082	4083	4084	4085	4086	4087	4088	4089	4090	4091	4092	4093	4094	4095

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Hexadecimal	Load and Store Instructions
	Load Accumulator (LD)
C0XX	Contents of CSL at EA (I+DISP) are loaded into A
C1XX	Contents of CSL at EA (XR1+DISP) are loaded into A
C2XX	Contents of CSL at EA (XR2+DISP) are loaded into A
C3XX	Contents of CSL at EA (XR3+DISP) are loaded into A
C400XXXX	Contents of CSL at EA (Addr) are loaded into A
C500XXXX	Contents of CSL at EA (Addr +XR1) are loaded into A
C600XXXX	Contents of CSL at EA (Addr +XR2) are loaded into A
C700XXXX	Contents of CSL at EA (Addr +XR3) are loaded into A
C480XXXX	Contents of CSL at EA (V in CSL at Addr) are loaded into A
C580XXXX	Contents of CSL at EA (V in CSL at "Addr +XR1") are loaded into A
C680XXXX	Contents of CSL at EA (V in CSL at "Addr +XR2") are loaded into A
C780XXXX	Contents of CSL at EA (V in CSL at "Addr +XR3") are loaded into A
	Double Load (LDD)
C8XX	Contents of CSL at EA (I + DISP) and EA+1 are loaded into A and Q
C9XX	Contents of CSL at EA(XR1 + DISP) and EA+1 are loaded into A and Q
CAXX	Contents of CSL at EA (XR2 + DISP) and EA+1 are loaded into A and Q
CBXX	Contents of CSL at EA (XR3 + DISP) and EA+1 are loaded into A and Q
CC00XXXX	Contents of CSL at EA (Addr) and EA+1 are loaded into A and Q
CD00XXXX	Contents of CSL at EA (Addr +XR1) and EA+1 are loaded into A and Q
CE00XXXX	Contents of CSL at EA (Addr +XR2) and EA+1 are loaded into A and Q
CF00XXXX	Contents of CSL at EA (Addr +XR3) and EA+1 are loaded into A and Q
CC80XXXX	Contents of CSL at EA (V in CSL at Addr) and EA+1 are loaded into A and Q
CD80XXXX	Contents of CSL at EA (V in CSL at "Addr +XR1") and EA+1 are loaded into A and Q
CE80XXXX	Contents of CSL at EA (V in CSL at "ADDR +XR2") and EA+1 are loaded into A and Q
CF80XXXX	Contents of CSL at EA (V in CSL at "Addr +XR3") and EA+1 are loaded into A and Q
	Store Accumulator (STO)
D0XX	Contents of A are stored in CSL at EA (I+DISP)
D1XX	Contents of A are stored in CSL at EA (XR1+DISP)
D2XX	Contents of A are stored in CSL at EA (XR2+DISP)
D3XX	Contents of A are stored in CSL at EA (XR3+DISP)
D400XXXX	Contents of A are stored in CSL at EA (Addr)
D500XXXX	Contents of A are stored in CSL at EA (Addr +XR1)
D600XXXX	Contents of A are stored in CSL at EA (Addr +XR2)
D700XXXX	Contents of A are stored in CSL at EA (Addr +XR3)
D480XXXX	Contents of A are stored in CSL at EA (V in CSL at Addr)
D580XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR1")
D680XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR2")
D780XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR3")
	Double Store (STD)
D8XX	Contents of A and Q are stored in CSL at EA (I+DISP) and EA+1
D9XX	Contents of A and Q are stored in CSL at EA (XR1 +DISP) and EA+1
DAXX	Contents of A and Q are stored in CSL at EA (XR2 +DISP) and EA+1
DBXX	Contents of A and Q are stored in CSL at EA (XR3 +DISP) and EA+1
DC00XXXX	Contents of A and Q are stored in CSL at EA (Addr) and EA+1
DD00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR1) and EA+1
DE00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR2) and EA+1
DF00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR3) and EA+1
DC80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at Addr) and EA+1
DD80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR1") and EA+1
DE80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR2") and EA+1
DF80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR3") and EA+1
	Load Index (LDX)
60XX	Load DISP into the Instruction Register
61XX	Load DISP into Index Register 1
62XX	Load DISP into Index Register 2
63XX	Load DISP into Index Register 3
6400XXXX	Load Addr into the Instruction Register
6500XXXX	Load Addr into Index Register 1
6600XXXX	Load Addr into Index Register 2
6700XXXX	Load Addr into Index Register 3
6480XXXX	Load contents of CSL at Addr into the Instruction Register
6580XXXX	Load contents of CSL at Addr into Index Register 1
6680XXXX	Load contents of CSL at Addr into Index Register 2
6780XXXX	Load contents of CSL at Addr into Index Register 3

Hexadecimal	Load and Store Instructions
	Store Index (STX)
68XX	Store I in CSL at EA (I+DISP)
69XX	Store XR1 in CSL at EA (I+DISP)
6AXX	Store XR2 in CSL at EA (I+DISP)
6BXX	Store XR3 in CSL at EA (I+DISP)
6C00XXXX	Store I in CSL at EA (Addr)
6D00XXXX	Store XR1 in CSL at EA (Addr)
6E00XXXX	Store XR2 in CSL at EA (Addr)
6F00XXXX	Store XR3 in CSL at EA (Addr)
6C80XXXX	Store I in CSL at EA (V in CSL at Addr)
6D80XXXX	Store XR1 in CSL at EA (V in CSL at Addr)
6E80XXXX	Store XR2 in CSL at EA (V in CSL at Addr)
6F80XXXX	Store XR3 in CSL at EA (V in CSL at Addr)
	Store Status (STS)
28XX	Store status of indicators in CSL at EA (I+DISP)
29XX	Store status of indicators in CSL at EA (XR1+DISP)
2AXX	Store status of indicators in CSL at EA (XR2+DISP)
2BXX	Store status of indicators in CSL at EA (XR3+DISP)
2C00XXXX	Store status of indicators in CSL at EA (Addr)
2D00XXXX	Store status of indicators in CSL at EA (Addr+XR1)
2E00XXXX	Store status of indicators in CSL at EA (Addr+XR2)
2F00XXXX	Store status of indicators in CSL at EA (Addr+XR3)
2C80XXXX	Store status of indicators in CSL at EA (V in CSL at Addr)
2D80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR1")
2E80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR2")
2F80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR3")
2C40XXXX	Clear storage protect bit in CSL at EA (Addr)
2C41XXXX	Write storage protect bit in CSL at EA (Addr)
2D40XXXX	Clear storage protect bit in CSL at EA (Addr +XR1)
2D41XXXX	Write storage protect bit in CSL at EA (Addr +XR1)
2E40XXXX	Clear storage protect bit in CSL at EA (Addr +XR2)
2E41XXXX	Write storage protect bit in CSL at EA (Addr +XR2)
2F40XXXX	Clear storage protect bit in CSL at EA (Addr +XR3)
2F41XXXX	Write storage protect bit in CSL at EA (Addr +XR3)
2CC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at Addr)
2CC1XXXX	Write storage protect bit in CSL at EA (V in CSL at Addr)
2DC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR1")
2DC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr +XR1")
2EC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR2")
2EC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr +XR2")
2FC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR3")
2FC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr +XR3")
	Load Status (LDS)
2000	Set CARRY and OVERFLOW indicators OFF
2001	Set OVERFLOW ON and CARRY OFF
2002	Set OVERFLOW OFF and CARRY ON
2003	Set CARRY and OVERFLOW indicator ON

Hexadecimal	Arithmetic Instructions
	Add (A)
80XX	Add contents of CSL at EA (I+DISP) to A
81XX	Add contents of CSL at EA (XR1+DISP) to A
82XX	Add contents of CSL at EA (XR2+DISP) to A
83XX	Add contents of CSL at EA (XR3+DISP) to A
8400XXXX	Add contents of CSL at EA (Addr) to A
8500XXXX	Add contents of CSL at EA (Addr +XR1) to A
8600XXXX	Add contents of CSL at EA (Addr +XR2) to A
8700XXXX	Add contents of CSL at EA (Addr +XR3) to A
8480XXXX	Add contents of CSL at EA (V in CSL at Addr) to A
8580XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") to A
8680XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") to A
8780XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") to A
	Double Add (AD)
88XX	Add contents of CSL at EA (I+DISP) and EA+1 to A and Q
89XX	Add contents of CSL at EA (XR1+DISP) and EA+1 to A and Q
8AXX	Add contents of CSL at EA (XR2+DISP) and EA+1 to A and Q
8BXX	Add contents of CSL at EA (XR3+DISP) and EA+1 to A and Q
8C00XXXX	Add contents of CSL at EA (Addr) and EA+1 to A and Q
8D00XXXX	Add contents of CSL at EA (Addr+XR1) and EA+1 to A and Q
8E00XXXX	Add contents of CSL at EA (Addr+XR2) and EA+1 to A and Q
8F00XXXX	Add contents of CSL at EA (Addr+XR3) and EA+1 to A and Q
8C80XXXX	Add contents of CSL at EA (V in CSL at Addr) and EA+1 to A and Q
8D80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 to A and Q
8E80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 to A and Q

Hexadecimal	Arithmetic Instructions
8F80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 to A and Q
	Subtract (S)
90XX	Subtract contents of CSL at EA (I+DISP) from A
91XX	Subtract contents of CSL at EA (XR1+DISP) from A
92XX	Subtract contents of CSL at EA (XR2+DISP) from A
93XX	Subtract contents of CSL at EA (XR3+DISP) from A
9400XXXX	Subtract contents of CSL at EA (Addr) from A
9500XXXX	Subtract contents of CSL at EA (Addr+XR1) from A
9600XXXX	Subtract contents of CSL at EA (Addr+XR2) from A
9700XXXX	Subtract contents of CSL at EA (Addr+XR3) from A
9480XXXX	Subtract contents of CSL at EA (V in CSL at Addr) from A
9580XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") from A
9680XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") from A
9780XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") from A
	Double Subtract (SD)
98XX	Subtract contents of CSL at EA (I+DISP) and EA+1 from A and Q
99XX	Subtract contents of CSL at EA (XR1+DISP) and EA+1 from A and Q
9AXX	Subtract contents of CSL at EA (XR2+DISP) and EA+1 from A and Q
9BXX	Subtract contents of CSL at EA (XR3+DISP) and EA+1 from A and Q
9C00XXXX	Subtract contents of CSL at EA (Addr) and EA+1 from A and Q
9D00XXXX	Subtract contents of CSL at EA (Addr+XR1) and EA+1 from A and Q
9E00XXXX	Subtract contents of CSL at EA (Addr+XR2) and EA+1 from A and Q
9F00XXXX	Subtract contents of CSL at EA (Addr+XR3) and EA+1 from A and Q
9C80XXXX	Subtract contents of CSL at EA (V in CSL at Addr) and EA+1 from A and Q
9D80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 from A and Q
9E80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 from A and Q
9F80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 from A and Q
	Multiply (M)
A0XX	Multiply contents of CSL at EA (I+DISP) by A
A1XX	Multiply contents of CSL at EA (XR1+DISP) by A
A2XX	Multiply contents of CSL at EA (XR2+DISP) by A
A3XX	Multiply contents of CSL at EA (XR3+DISP) by A
A400XXXX	Multiply contents of CSL at EA (Addr) by A
A500XXXX	Multiply contents of CSL at EA (Addr+XR1) by A
A600XXXX	Multiply contents of CSL at EA (Addr+XR2) by A
A700XXXX	Multiply contents of CSL at EA (Addr+XR3) by A
A480XXXX	Multiply contents of CSL at EA (V in CSL at Addr) by A
A580XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR1") by A
A680XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR2") by A
A780XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR3") by A
	Divide (D)
A8XX	Divide A and Q by contents of CSL at EA (I+DISP)
A9XX	Divide A and Q by contents of CSL at EA (XR1+DISP)
AAXX	Divide A and Q by contents of CSL at EA (XR2+DISP)
ABXX	Divide A and Q by contents of CSL at EA (XR3+DISP)
AC00XXXX	Divide A and Q by contents of CSL at EA (Addr)
AD00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR1)
AE00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR2)
AF00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR3)
AC80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at Addr)
AD80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR1")
AE80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR2")
AF80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR3")
	Logical And (AND)
E0XX	AND contents of CSL at EA (I+DISP) with A
E1XX	AND contents of CSL at EA (XR1+DISP) with A
E2XX	AND contents of CSL at EA (XR2+DISP) with A
E3XX	AND contents of CSL at EA (XR3+DISP) with A
E400XXXX	AND contents of CSL at EA (Addr) with A
E500XXXX	AND contents of CSL at EA (Addr+XR1) with A
E600XXXX	AND contents of CSL at EA (Addr+XR2) with A
E700XXXX	AND contents of CSL at EA (Addr+XR3) with A
E480XXXX	AND contents of CSL at EA (V in CSL at Addr) with A
E580XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR1") with A
E680XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR2") with A
E780XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR3") with A

Hexadecimal	Arithmetic Instructions
	Logical Or (OR)
E8XX	OR contents of CSL at EA (I+DISP) with A
E9XX	OR contents of CSL at EA (XR1+DISP) with A
EAXX	OR contents of CSL at EA (XR2+DISP) with A
EBXX	OR contents of CSL at EA (XR3+DISP) with A
EC00XXXX	OR contents of CSL at EA (Addr) with A
ED00XXXX	OR contents of CSL at EA (Addr+XR1) with A
EE00XXXX	OR contents of CSL at EA (Addr+XR2) with A
EF00XXXX	OR contents of CSL at EA (Addr+XR3) with A
EC80XXXX	OR contents of CSL at EA (V in CSL at Addr) with A
ED80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR1") with A
EE80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR2") with A
EF80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Logical Exclusive Or (EOR)
F0XX	EOR contents of CSL at EA (I+DISP) with A
F1XX	EOR contents of CSL at EA (XR1+DISP) with A
F2XX	EOR contents of CSL at EA (XR2+DISP) with A
F3XX	EOR contents of CSL at EA (XR3+DISP) with A
F400XXXX	EOR contents of CSL at EA (Addr) with A
F500XXXX	EOR contents of CSL at EA (Addr+XR1) with A
F600XXXX	EOR contents of CSL at EA (Addr+XR2) with A
F700XXXX	EOR contents of CSL at EA (Addr+XR3) with A
F480XXXX	EOR contents of CSL at EA (V in CSL at Addr) with A
F580XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR1") with A
F680XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR2") with A
F780XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Shift Instructions
	Shift Left Logical A (SLA)
10*X	Contents of A shift left the number of shift counts in DISP
1100	Contents of A shift left the number of shift counts in XR1
1200	Contents of A shift left the number of shift counts in XR2
1300	Contents of A shift left the number of shift counts in XR3
	Shift Left Logical A & Q (SLT)
10*X	Contents of A and Q shift left the number of shift counts in DISP
1180	Contents of A and Q shift left the number of shift counts in XR1
1280	Contents of A and Q shift left the number of shift counts in XR2
1380	Contents of A and Q shift left the number of shift counts in XR3
	Shift Left And Count A (SLCA)
10*X	Contents of A shift left the number of shift counts in DISP
1140	Contents of A shift left the number of shift counts in XR1
1240	Contents of A shift left the number of shift counts in XR2
1340	Contents of A shift left the number of shift counts in XR3
	Shift Left And Count A & Q (SLC)
10*X	Contents of A and Q shift left the number of shift counts in DISP
11C0	Contents of A and Q shift left the number of shift counts in XR1
12C0	Contents of A and Q shift left the number of shift counts in XR2
13C0	Contents of A and Q shift left the number of shift counts in XR3
	Shift Right Logical A (SRA)
18*X	Contents of A shift right the number of shift counts in DISP
1900	Contents of A shift right the number of shift counts in XR1
1A00	Contents of A shift right the number of shift counts in XR2
1B00	Contents of A shift right the number of shift counts in XR3
	Shift Right A & Q (SRT)
18*X	Contents of A and Q shift right the number of shift counts in DISP
1980	Contents of A and Q shift right the number of shift counts in XR1
1A80	Contents of A and Q shift right the number of shift counts in XR2
1B80	Contents of A and Q shift right the number of shift counts in XR3
	Rotate Right A & Q (RTE)
18*X	Contents of A and Q rotate right the number of counts in DISP
19C0	Contents of A and Q rotate right the number of counts in XR1
1AC0	Contents of A and Q rotate right the number of counts in XR2
1BC0	Contents of A and Q rotate right the number of counts in XR3

See Instruction Set Section for Meaning of Symbols

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Hexadecimal	Branch Instructions
	Branch Or Skip On Condition (BSC or BOSC)
48*X	Skip the next one-word instruction if ANY condition is sensed
4C*XXXXX	Branch to CSL at EA (Addr) on NO condition
4D*XXXXX	Branch to CSL at EA (Addr+XR1) on NO condition
4E*XXXXX	Branch to CSL at EA (Addr+XR2) on NO condition
4F*XXXXX	Branch to CSL at EA (Addr+XR3) on NO condition
4C*XXXXX	Branch to CSL at EA (V in CSL at Addr) on NO condition
4D*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR1") on NO condition
4E*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR2") on NO condition
4F*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR3") on NO condition
	Branch And Store Instruction Register (BSI)
40XX	Store next sequential address in CSL at EA (I+DISP) and Branch to EA+1
41XX	Store next sequential address in CSL at EA (XR1+DISP) and Branch to EA+1
42XX	Store next sequential address in CSL at EA (XR2+DISP) and Branch to EA+1
43XX	Store next sequential address in CSL at EA (XR3+DISP) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR1) and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR2) and Branch to EA+1
47*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR3) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR1") and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR2") and Branch to EA+1
47*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR3") and Branch to EA+1
	Modify Index and Skip (MDX)
70XX	ADD expanded DISP to I (no skip can occur)
71XX	ADD expanded DISP to XR1
72XX	ADD expanded DISP to XR2
73XX	ADD expanded DISP to XR3
74XXXXXX	Add expanded positive DISP to CSL at Addr (Add to memory)
7500XXXX	Add Addr to XR1
7600XXXX	Add Addr to XR2
7700XXXX	Add Addr to XR3
74XXXXXX	Add expanded negative DISP to CSL at Addr (Add to Memory)
7580XXXX	Add V in CSL at Addr to XR1
7680XXXX	Add V in CSL at Addr to XR2
7780XXXX	Add V in CSL at Addr to XR3
	Wait (WAIT)
3000	WAIT until manual start or until completion of an interrupt subroutine
	Compare (CMP)
B0XX	Compare A with contents of CSL at EA (I+DISP)
B1XX	Compare A with contents of CSL at EA (XR1+DISP)
B2XX	Compare A with contents of CSL at EA (XR2+DISP)
B3XX	Compare A with contents of CSL at EA (XR3+DISP)
B400XXXX	Compare A with contents of CSL at EA (Addr)
B500XXXX	Compare A with contents of CSL at EA (Addr+XR1)
B600XXXX	Compare A with contents of CSL at EA (Addr+XR2)
B700XXXX	Compare A with contents of CSL at EA (Addr+XR3)
B480XXXX	Compare A with contents of CSL at EA (V in CSL at Addr)
B580XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR1")
B680XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR2")
B780XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR3")
	Double Compare (DCM)
B8XX	Compare A and Q with contents of CSL at EA (I+DISP) and EA+1
B9XX	Compare A and Q with contents of CSL at EA (XR1+DISP) and EA+1
BAXX	Compare A and Q with contents of CSL at EA (XR2+DISP) and EA+1

Hexadecimal	Branch Instructions
BBXX	Compare A and Q with contents of CSL at EA (XR3+DISP) and EA+1
BC00XXXX	Compare A and Q with contents of CSL at EA (Addr) and EA+1
BD00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR1) and EA+1
BE00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR2) and EA+1
BF00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR3) and EA+1
BC80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at Addr) and EA+1
BD80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1
BE80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1
BF80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1
	I/O Instructions
	Execute I/O (XIO)
08XX	Execute IOCC in CSL at EA (I+DISP) and EA+1
09XX	Execute IOCC in CSL at EA (XR1+DISP) and EA+1
0AXX	Execute IOCC in CSL at EA (XR2+DISP) and EA+1
0BXX	Execute IOCC in CSL at EA (XR3+DISP) and EA+1
0C00XXXX	Execute IOCC in CSL at EA (Addr) and EA+1
0D00XXXX	Execute IOCC in CSL at EA (Addr+XR1) and EA+1
0E00XXXX	Execute IOCC in CSL at EA (Addr+XR2) and EA+1
0F00XXXX	Execute IOCC in CSL at EA (Addr+XR3) and EA+1
0C80XXXX	Execute IOCC in CSL at EA (V in CSL at Addr) and EA+1
0D80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR1") and EA+1
0E80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR2") and EA+1
0F80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR3") and EA+1

See Instruction Set Section for Meaning of Symbols

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Appendix C. Average Instruction Execution Times*
(The times below pertain to the 2 μsec core storage.
Add 2 μsec to Execution Times When Indirect Addressing
is Specified)

		F = 0		F = 1	
		T=0	T≠0	T=0	T≠0
	LD	4 1/4	4 1/4	6	6 1/4
	STO	4 1/4	4 1/4	6	6 1/4
	LDD	6 1/4	6 1/4	8	8 1/4
	STD	6 1/4	6 1/4	8	8 1/4
①	A	4 1/2	4 1/2	6 1/4	6 1/2
	S	4 1/2	4 1/2	6 1/4	6 1/2
	AD	6 3/4	6 3/4	8 1/2	8 3/4
	SD	6 3/4	6 3/4	8 1/2	8 3/4
	M	15 1/4	15 1/4	17	17 1/4
	D	42 3/4	42 3/4	44	44 1/2
	AND	4 1/4	4 1/4	6	6 1/4
	OR	4 1/4	4 1/4	6	6 1/4
	EOR	4 1/4	4 1/4	6	6 1/4
②	BSI	2-4 1/4	2-4 1/4	2-6	2-6 1/4
	BSC	2	2	2-4	2-4 1/4
③	SLA	2 + N/4	2 + N/4	-	-
	SLT	2 + N/4	2 + N/4	-	-
④	SLCA	2 + N/4	④ 2 1/2 + N/4	-	-
	SLCAQ	2 + N/4	2 1/2 + N/4	-	-
③	SRA	2 + N/4	2 + N/4	-	-
⑤	RTE	2 + N/4	2 + N/4	-	-
	WAIT	2	2	2	2
⑥	XIO	6 1/4 - 8 1/4	6 1/4 - 8 1/4	8-10	8 1/4 - 10 1/4
	LDX	2 1/4	2 1/4	4 1/4	4 1/4
	STX	4 1/4	4 1/4	6	6
	MDX	2 1/2	2 1/2	10 1/4	4 3/4
	LDS	2	2	-	-
	STS	4 1/4	4 1/4	6	6 1/4
①	CMP	4 1/2	4 1/2	6 1/4	6 1/2
	DCM	6 3/4	6 3/4	8 1/2	8 3/4

① Execution Times Include an Average Add Time of 2 1/4 μsec.

② If a Skip or Branch is not Executed, the Instruction Performs as a NOP with
an Execution Time of 2.0 us. If the Skip or Branch is Executed, the Second
Execution Time is Applicable.

③ N = P – 4, where P is the Number of Positions Shifted, and N must be
Positive or Zero.

④ If T ≠ 0 and More Than Four (4) Shifts Occur, then 1/2 μs is Added to the
Execution Time as Shown to Restore the Specified Index Register from the
Shift Counter.

⑤ A Shift of 1, 2, 3 or 4 Positions Requires 2 μsec, with 1/4 μsec Added for
Each Additional Shift Position up to 15. Therefore, a Shift of 5 Positions
Takes 2.25 μsec, a shift of 6 Positions Takes 2.5 μsec, etc., up to 15
Positions which Takes 4.75 μsec.

A Shift of 16, 17, 18, or 19 Positions Requires 2.25 μsec, with 1/4 μsec
Added for Each Additional Shift Position up to 31. Therefore, a Shift of
21 Positions Takes 2.5 μsec, a Shift of 22 Positions Takes 2.75 μsec, etc.,
up to 31 Positions Which Takes 5 μsec.

⑥ The longer times apply to the Read and Write functions,
the shorter times to all other functions.

*Double these times for the 4 μsec core storage. [17439 B]

Internal Add Operation

The arithmetic section of the 1801/1802 P-C per-forms additions in successive machine cycles that are 1/4 μsec (2 μsec core storage) or 1/2 μsec (4 μsec core storage) in duration. The number of ma-chine cycles required to complete the addition de-pends on the numbers being added and the resulting "carries." As shown in Figure C-1, the augend

Machine Cycles	AUGEND (A-reg) and ANDEND (D-reg) Contents 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
	A_0	0 1 1 0 1 1 1 0 0 0 1 1 1 0 1 0
	D_0	1 1 1 1 0 0 1 1 0 0 0 1 1 1 0 1
*First	A_1	1 0 0 1 1 1 0 1 0 0 1 0 0 1 1 1
	D_1	1 1 0 0 0 1 0 0 0 0 1 1 0 0 0 0
*Second	A_2	0 1 0 1 1 0 0 1 0 0 0 1 0 1 1 1
	D_2	0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0
*Third	A_3	0 1 0 1 0 0 0 1 0 1 0 1 0 1 1 1
	D_3	0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
*Fourth	A_4	0 1 0 0 0 0 0 1 0 1 0 1 0 1 1 1
	D_4	0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
**Fifth	A_5	0 1 1 0 0 0 0 1 0 1 0 1 0 1 1 1
	D_5	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

*Occurs during the 2 or 4 μsec core storage cycle required to read the addend from core storage.

** Extra 1/4 or 1/2 μsec machine cycle.

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Figure C-1. Data Addition Example

(A register) and addend (D register) are "Exclusive ORed" and "ANDed" each machine cycle. (The Ex-clusive OR and AND functions are explained in the Arithmetic Instructions section of the manual.) The results of the Exclusive OR function are placed in the A register. The results of the AND function are ig-nored except for any carries that may occur. The carries are shifted one position to the left and placed in the D register. (These bits represent carries that would result from a normal binary add operation.) Each time a carry occurs, another machine cycle is initiated in which the A and D registers are Exclusive ORed and ANDed again. This process continues until there are no further carries, at which time the cor-rect sum exists in the A register.

The length of each carry chain depends on the numbers involved and varies from 0 to 15. In Figure C-1, a carry chain of four (bit positions 2 through 5) caused five machine cycles. The first four of these cycles were included in the core storage cycle that read the addend from core storage. Only carry chain lengths of four and greater cause extra 1/4 or 1/2 μsec machine cycles.

Total Execution Time

Two core storage cycles are required in the execution of an Add instruction: one for instruction readout and effec-tive address computation, and one for data readout and data addition. Figure C-2 is a sequence chart for the "average" add operation in which F = 0, T $\neq$ 0, and the carry chain length does not exceed four.
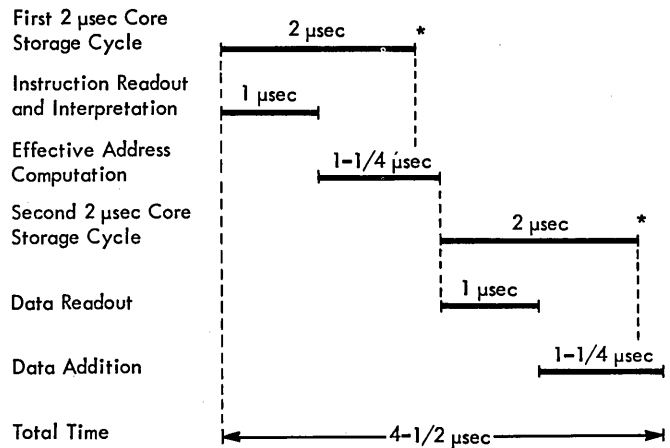
*Cycle steals can occur here without stopping effective address computation or data addition.

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Figure C-2. Add Instruction Sequence Chart

Time Probabilities for the Addition of Data to the Accumulator

Table C-1 shows a mathematical analysis of all possible number pairs that can be added with the A and D registers:

Table C-1. Mathematicl Analysis of Addition of all Possible Number Pairs

Carry Chain Length	Probability (%)	Cumulative (%)	Time (μsec)
0	1.3363	1.3363	2.00
1	9.8892	11.2255	2.00
2	27.0115	38.2370	2.00
3	27.7178	65.9548	2.00
4	17.3702	83.3250	2.25
5	8.9237	92.2487	2.50
6	4.2404	96.4891	2.75
7	1.9485	98.4376	3.00
8	0.8789	99.3165	3.25
9	0.3906	99.7071	3.50
10	0.1709	99.8780	3.75
11	0.0732	99.9512	4.00
12	0.0305	99.9817	4.25
13	0.0122	99.9939	4.50
14	0.0046	99.9985	4.75
15	0.0015	100.0000	5.00

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The Carry Chain Length column lists all possible carry chain lengths up to the maximum of 15.

The Probability column contains percentage figures which are related to the Carry Chain Length. For example, a carry chain length of four occurs during 17.37% of all add operations.

The Cumulative column is merely a progressive summation of the Probability percentages. For example, 83.32% of all add operations involve carry chain lengths of four or less; which, incidentally, is the basis for the Average Execution Time given in this appendix for Add instructions.

The Time column shows the time required for Data Readout and Data Addition (see Figure C-2) with a 2 μsec core storage. The average Data Readout and Data Addition time for adding all possible numbers at random is 2.16 μsec.

APPENDIX D. I/O DEVICE ADDRESSING

The Area, Function, and Modifier codes listed below are required for 1800 I/O operations (x indicates an unused bit position):

	AREA	FUN	MODIFIER
Console Data Entry Switches			
<u>Sense Device</u> - switch data to A-reg.	0 0 0 0 0	1 1 1	0 1 0 x x x x x
<u>Read</u> - switch data to core.	0 0 0 0 0	0 1 0	0 1 0 x x x x x
Console Sense, Program Switches and CE Switches			
<u>Sense Device</u> - switch data to A-reg.	0 0 0 0 0	1 1 1	0 1 1 x x x x x
<u>Read</u> - switch data to core.	0 0 0 0 0	0 1 0	0 1 1 x x x x x
Console Interrupt			
<u>Sense Device</u> - console DSW to A-reg; indicators not reset	0 0 0 0 0	.1 1 1	1 1 0 x x x x 0
- console DSW to A-reg; reset indicators	0 0 0 0 0	1 1 1	1 1 0 x x x x 1
Operations Monitor			
<u>Control</u> - timer not reset	0 0 0 0 0	1 0 0	1 1 1 x x x x 0
- reset timer	0 0 0 0 0	1 0 0	1 1 1 x x x x 1
Interval Timers			
<u>Control</u> - timers started or stopped according to bits 0-2 of IOCC Address word.	0 0 0 0 0	1 0 0	0 0 1 x x x x x
Interrupt Mask Register			
<u>Control</u> - mask or unmask interrupt levels 0-13, depending on IOCC Address word bit positions 0-13.	0 0 0 0 0	1 0 0	1 0 0 x x x x 0
- mask or unmask interrupt levels 14-23, depending on IOCC Address word bit positions 0-9.	0 0 0 0 0	1 0 0	1 0 0 x x x x 1
Program Interrupt			
<u>Control</u> - turn on interrupt levels 0-13, depending on IOCC Address word bit positions 0-13.	0 0 0 0 0	1 0 0	1 0 1 x x x x 0
- turn on interrupt levels 14-23, depending on IOCC Address word bit positions 0-9.	0 0 0 0 0	1 0 0	1 0 1 x x x x 1
ILSW			
<u>Sense</u>	0 0 0 0 0	0 1 1	0 0 0 0 0 0 0 0

NOTE: For Process Interrupt see Digital Input.

	AREA	FUN	MODIFIER

1053 Printer:

First four 1053's:

    Write - individual 1053 specified by IOCC modifier bits 11-14.

    Sense Device - 1816/1053 DSWs to A-reg. Individual units specified by IOCC bits 11-14; bit 15 determines reset of indicators.

	AREA	FUN	MODIFIER
Write	0 0 0 0 1	0 0 1	x x x y y y y x
Sense Device	0 0 0 0 1	1 1 1	x x x y y y y y

Second four 1053's: Area code is 01111.

1816 Printer - Keyboard

    Read - single character to core storage.

    Sense Device - 1816/1053 DSWs to Accumulator. Individual units specified by IOCC bits 11-14; bit 15 determines reset of indicators.

    Control - places keyboard in Ready status

	AREA	FUN	MODIFIER
Read	0 0 0 0 1	0 1 0	x x x x 0 0 1 0
Sense Device	0 0 0 0 1	1 1 1	x x x y y y y R
Control	0 0 0 0 1	1 0 0	x x x x 0 0 1 0

1442 Card Read - Punch

First 1442:

    Initialize Read - card columns to core storage. Where P is Packed Mode.

    Initialize Write - core storage to card columns.

    Control - IOCC bits 8 and 14 specify function. Where Y is Stacker Select F is Feed Cycle.

    Sense Device - DSW to Accumulator; bit 15 determines reset of indicators.

	AREA	FUN	MODIFIER
Initialize Read	0 0 0 1 0	1 1 0	x x x x x x x P
Initialize Write	0 0 0 1 0	1 0 1	x x x x x x x x
Control	0 0 0 1 0	1 0 0	Y x x x x x F x
Sense Device	0 0 0 1 0	1 1 1	x x x x x x x R

Second 1442: Area code is 10001.

1054 and 1055 Paper Tape

    Read - one character from tape buffer to core storage.

    Write - core storage to tape.

    Control - One character from tape to tape buffer.

    Sense Device - DSW to Accumulator; bit 15 determines reset of indicator.

	AREA	FUN	MODIFIER
Read	0 0 0 1 1	0 1 0	x x x x x x x x
Write	0 0 0 1 1	0 0 1	x x x x x x x x
Control	0 0 0 1 1	1 0 0	x x x 1 x x x x
Sense Device	0 0 0 1 1	1 1 1	x x x x x x x R

	AREA	FUN	MODIFIER

2310 Disk Storage Drive

First 2310:

	AREA	FUN	MODIFIER
Initialize Read-into-memory: yyy specify disk sector.	0 0 1 0 0	1 1 0	0 x x x x y y y
Initialize Read-check	0 0 1 0 0	1 1 0	1 x x x x y y y
Initialize Write	0 0 1 0 0	1 0 1	x x x x x y y y
Control – seek as specified by IOCC address and modifier bit 13.	0 0 1 0 0	1 0 0	x x x x x S x x
Sense Device – DSW to A-reg; bit 15 determines reset of indicators.	0 0 1 0 0	1 1 1	x x x x x x R

Second and Third 2310's require Area codes of 01000 and 01001, respectively.

1627 Plotter

	AREA	FUN	MODIFIER
Write – core storage to plotter.	0 0 1 0 1	0 0 1	x x x x x x x
Sense Device – DSW to A-reg; bit 15 determines reset of indicators.	0 0 1 0 1	1 1 1	x x x x x x R

1443 Printer

	AREA	FUN	MODIFIER
Initialize Write – bit 15 is used for space suppress.	0 0 1 1 0	1 0 1	x x x x x x x y
Control – carriage control	0 0 1 1 0	1 0 0	x x x x x x x x
Sense Device – DSW to A-reg; bit 15 determines reset of indicators.	0 0 1 1 0	1 1 1	x x x x x x R

Analog Input

Direct Program Control:

	AREA	FUN	MODIFIER
Write – AI point to ADC; Address word of IOCC specifies the core-storage location of the multiplexer address; where E is External Sync. L is 8-bit resolution. H is 14-bit resolution.	0 1 0 1 0	0 0 1	E x x L H x x x
Read – ADC to core storage; Address word of IOCC is core-storage location specifying where the ADC reading will be stored; where S is Sequential Program mode.	0 1 0 1 0	0 1 0	S x x x x x x x

	AREA	FUN	MODIFIER
<u>Sense Device</u> - DSW to A-reg; where C specifies Comparator or AI status word. R bit resets indicators.	0 1 0 1 0	1 1 1	C x x x x x x R
<u>Control</u> (Blast Instruction)	0 1 0 1 0	1 0 0	x x x x x x x x

Data Channel Control:

	AREA	FUN	MODIFIER
<u>Initialize Read</u> - ADC readings to core storage; where T specifies a two DC operation.	0 1 0 1 0	1 1 0	E x T L H x x x
<u>Initialize Write</u> - Address from core storage to multiplexer	0 1 0 1 0	1 0 1	x x x x x x x x

The AI Expander Area code is 10000.

Digital Input

Direct Program Control:

	AREA	FUN	MODIFIER
<u>Read</u> - DI or PI group to core storage; Bits 9-15 are DI addresses 64_{10} through 127_{10} or PI addresses 2_{10} through 25_{10}.	0 1 0 1 1	0 1 0	x A A A A A A A
<u>Sense Device</u> - DSW, DI, or PISW to A-register; Bits 11-15 are DSW addresses 00000 or 00001 (reset indicators), PISW addresses 2_{10} through 25_{10} or DI addresses 64_{10} through 127_{10}.	0 1 0 1 1	1 1 1	x B B B B B B B
<u>Control</u> (Blast Instruction)	0 1 0 1 1	1 0 0	x x 1 x x x x x

Data Channel Control:

	AREA	FUN	MODIFIER
<u>Initialize Read</u> - where bits 8-10 specify the read mode.	0 1 0 1 1	1 1 0	R R R x x x x x

Digital and Analog Output

Direct Program Control:

	AREA	FUN	MODIFIER
<u>Write</u> - core storage to DAO device; where bits 9-15 are device addresses 0_{10} through 127_{10}.	0 1 1 0 0	0 0 1	x A A A A A A A
<u>Control</u> - where bit 9 initiates simultaneous transfer from buffer registers, bit 8 initiates timing pulse for Pulse Output, and bit 10 resets all DAO controls (Blast Instruction).	0 1 1 0 0	1 0 0	P B R x x x x x
<u>Sense Device</u> - DSW to A-reg; bit 15 determines reset of the indicators.	0 1 1 0 0	1 1 1	x x x x x x x R

Data Channel Control:

	AREA	FUN	MODIFIER
<u>Initialize Write</u> - core storage to DAO registers. Bits 8-10 specify write mode.	0 1 1 0 0	1 0 1	R R R x x x x x

	AREA	FUN	MODIFIER
System/360 Adapter			
Initialize Write	0 1 1 0 1	1 0 1	x x x x x x x x
Initialize Read	0 1 1 0 1	1 1 0	x x x x x x x x
Sense Status	0 1 1 0 1	1 1 1	0 x x x x x x R
Sense Word Count	0 1 1 0 1	1 1 1	1 x x x x x x x
Control (Reset)	0 1 1 0 1	1 0 0	x x x x x x x x
2401 or 2402 Magnetic Tape			
Initialize Read - where bits 10-15 specify:	0 1 1 1 0	1 1 0	x x Y Y Y Y Y Y
10 Address Tape Unit 0 or 1	0 1 1 1 0	1 1 0	x x T Y Y Y Y Y
11,12 Bit density for 7-track (ignored for 9-track)			
Bits 11 and 12 equal 00 for 800 BPI	0 1 1 1 0	1 1 0	x x Y 0 0 Y Y Y
Bits 11 and 12 equal 01 for 200 BPI	0 1 1 1 0	1 1 0	x x Y 0 1 Y Y Y
Bits 11 and 12 equal 10 for 556 BPI	0 1 1 1 0	1 1 0	x x Y 1 0 Y Y Y
13 "Packed-format" for 7-track (ignored for 9-track)	0 1 1 1 0	1 1 0	x x Y Y Y F Y Y
14 Read-while-correcting (ignored for 7-track or for initial 9-track record read)	0 1 1 1 0	1 1 0	x x Y Y Y Y C Y
15 Even parity for 7-track (ignored for 9-track)	0 1 1 1 0	1 1 0	x x Y Y Y Y Y P
Initialize Write - where modifier bits specify:	0 1 1 1 0	1 0 1	x x Y Y Y Y x Y
10 Address Tape Unit 0 or 1	0 1 1 1 0	1 0 1	x x T Y Y Y x Y
11,12 Bit density for 7-track (ignored for 9-track)			
Bits 11 and 12 equal 00 for 800 BPI	0 1 1 1 0	1 0 1	x x Y 0 0 Y x Y
Bits 11 and 12 equal 01 for 200 BPI	0 1 1 1 0	1 0 1	x x Y 0 1 Y x Y
Bits 11 and 12 equal 10 for 556 BPI	0 1 1 1 0	1 0 1	x x Y 1 0 Y x Y
13 "Packed-format" for 7-track (ignored for 9-track)	0 1 1 1 0	1 0 1	x x Y Y Y F x Y
15 Even parity for 7-track (ignored for 9-track)	0 1 1 1 0	1 0 1	x x Y Y Y Y x P
Control Bit 10 addresses the tape unit, bits 11-12 specify the bit density for 7-track (11-12 ignored for 9-track)			
Rewind and unload	0 1 1 1 0	1 0 0	x x T x x 0 0 0
Write Tape mark	0 1 1 1 0	1 0 0	x x T D D 0 0 1
Erase	0 1 1 1 0	1 0 0	x x T D D 0 1 0
Backspace	0 1 1 1 0	1 0 0	x x T 0 1 0 1 1
Rewind	0 1 1 1 0	1 0 0	x x T x x 1 0 0
Sense Device			
Select tape Unit "T" and Read DSW into A-register (1)	0 1 1 1 0	1 1 1	x x T 0 0 x x 0
Select tape unit "T", Read DSW into A-register, and reset indicators (2)	0 1 1 1 0	1 1 1	x x T 0 0 x x 1

	AREA	FUN	MODIFIER
Read Tape Channel word count into A-register (3)	0 1 1 1 0	1 1 1	x x x 1 0 x x x
Operation Stop (free tape channel) with bits T, Y, and R also performing functions 1, 2, and 3 above.	0 1 1 1 0	1 1 1	x x T Y 1 x x R

Meaning of symbols in 2401/2402 IOCC modifiers above:

Symbol	Meaning
C	Read-while-correcting
D	Density
F	Packed Format
P	Even Parity
R	DSW Reset
T	Tape Unit
x	Not Used
Y	Variable

AREA	FEATURE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Console Interrupt	Interrupt Request															
	Interval Timers	*Timer A	Timer B	*Timer C													
	Data Entry Switches																
	Sense Switches	0	1	2	3	4	5 ←Program	6	7	8	9	10	11	12 ←CE Sense	13	14	15
1-, 15-	1816 Printer-Keyboard / 1053 Printer / -In First Group / -In Second Group	*Printer Service Response	*Keyboard Service Response (1816)	*Keyboard Request (1816)		Printer Busy	Printer Not Ready	Keyboard Not Ready (1816)	Storage Protect Violation (1816)	Keyboard Parity Error (1816)	Printer Parity Error				†CE Not Ready		
2-, 17-	1442 Card Read Punch / -First / -Second			Error	Last Card	*Operation Complete	Parity Error	Storage Protect Violation	Feed Check Read Station					†CE Busy	†CE Not Ready	Busy	Not Ready
3	1054/1055 Paper Tape Reader/Punch	PT Reader Any Error	*PT Reader Service Request	PT Punch Parity Error	*PT Punch Service Request	PT Reader Busy	PT Reader Not Ready	PT Punch Busy	PT Punch Not Ready	PT Reader Parity Error	PT Reader Storage Protect	†CE PT Reader Busy	†CE PT Reader Not Rdy	†CE PT Punch Busy	†CE PT Punch Not Rdy		
4-, 8-, 9-	2310 Disk Storage / First Drive / Second Drive / Third Drive	*Any Error	*Operation Complete	Disk Not Ready	Disk Busy (R/W or Ctrl)	Carriage Home	Parity Error	Storage Protect Error	Data Error	Write Select Error	Data Overrun		†CE Not Ready	†CE Busy	†CE Not Ready	Busy	Not Ready
5	1627 Plotter	*Service Response	Parity Error												†CE Not Ready	Busy	Not Ready
6	1443 Printer	*Transfer Complete	Error	*Printer Complete	Channel 9	Channel 12	Channel 1	Parity				†CE Carriage Busy	†CE Printer Busy	†CE Printer Not Ready	Carriage Busy	Printer Busy	Printer Not Ready
10-, 16-	Analog Input / -Basic / -Expander	*End of Table	*DPC SS Conv Complete	DPC Rly Conv Complete	*Storage Protect Violation	*Parity Control Error	*Parity Data Error	*Overload	*Overlap Conflict	Cyc Steal SS, AMAR Busy	DPC Relay Busy						Any Error
10-, 16-	Comparator / -AI Basic / -AI Expander	*High Out of Limit	Low Out of Limit	*Overload	AMAR SS MPX			AMAR 512	AMAR 256	AMAR 128	AMAR 64	AMAR 32	AMAR 16	AMAR 8	AMAR 4	AMAR 2	AMAR 1
11	Digital Input	*Parity Error	*Storage Protect Violation	*DI Scan Complete	*Command Reject												DI Busy
	PISW						Process Interrupt Points (Customer Assigned Groups)										
12	Digital and Analog Output	*Parity Error	Pulse Output Timer	*D & A Out Scan Complete	*Command Reject	Data Channel Active					*Operation Complete	CE Diagnostic Indicator					D/AO Busy
	S/360 Adapter	*Command Reject	1800 Command Stored	360 Command Stored	*Halt	*Data Check	*Storage Protect Violation	*Transfer End	*End of Table	Data Overrun Error			360 Command Byte →				
13	Adapter Word Counter							Word Count (1's Complement)			Word Count →						
14	Tape Control Unit		Tape Unit 1 Select	*Command Reject	*End of Table	Chain Stop	Storage Protect Violation Stop	Tape Data Error	Data Bus Out or P-C Parity Error	Data Overrun Error	*Operation Complete	CE Diagnostic Indicator	Wrong Length Record	At Load Point	Tape Indicator or Mark	Tape Busy or Rewind	Tape Busy or Not Ready
	TCU Word Counter	00 = True Count / 11 = 1's Complement						Word Count →									

* Interrupt Conditions
† Active Only in CE Mode

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2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125

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