IBM Field Engineering Maintenance Manual

1130 Computing System

IBM®

Field Engineering Maintenance Manual

Issued to: _____

Branch Office: _____

Department: _____

Address: _____

If this manual is misplaced, it should be returned to the above address.

1130 Computing System

PREFACE

This manual contains all maintenance procedures required to service the IBM 1130 Data Processing System.

This manual assumes that the CE has limited experience and/or training on the system and is familiar with the material contained in the Field Engineering Theory of Operation (Instruction Manual) manuals listed in the Bibliography (Appendix A).

The users of this manual are cautioned that specifications are subject to change at any time and without prior notice by IBM. Wiring diagrams (logics) at the engineering change level of that specific machine are included in each machine shipment.

This manual (Form 227-5977-1) is a major revision of Form 227-5977-0. The latter is made obsolete by this revision.

Copies of this and other IBM publications can be obtained through IBM Branch Offices.
A form has been provided at the back of this publication for readers' comments.
If the form has been detached, comments may be directed to:
IBM, Product Publications Department, San Jose, Calif. 95114

CONTENTS

WARNINGS

Core Storage

Be extremely cautious when working around the core array. Avoid disturbing individual planes. Sense and select wires are welded to pins at the perimeter of the array. Bending these pins can fracture welds or cause shorts between adjacent pins. Use the handles provided and exercise care to prevent the sides from striking the frame of SLT cards whenever it is necessary to remove the array. Do not leave core storage unit unattended when covers are removed.

Oscilloscope

Core Storage

Direct probing of the core planes is not advised. Because core is a current device, no valuable information can be obtained with voltage measurements in this area and considerable damage could result. Due to physical construction of the core array the current probe cannot be used directly. Techniques for obtaining current and voltage wave shapes are detailed in section 1.4.6 of this manual.

General

The SLT probe tip should be used when scoping to prevent shorting of voltage pins. Probing with alligator clips or uninsulated tips should be avoided.

Power Supplies

When the system is in a power-off status, 24 vac is present in the power supply area.

SLT Components

Turn off power whenever an SLT card is removed or replaced. Turn off power to the system when wrapping or unwrapping wire or when testing for continuity.

Avoid operating the system for prolonged periods of time with the SLT card covers removed.

Servicing

Clear core storage after servicing the processor to prevent returning the system to the customer with an invalid word in core storage. An invalid word results in a data error when the word is read from core.

Tying input and output logic functions to the ground or to 0 volt level can be helpful in troubleshooting. Exercise care in the disk storage unit to prevent destroying disk storage data when tying lines to the 0 volt level. Some logic blocks can be tied to the +3 volt level. It is necessary to evaluate the physical construction of the component circuits, both input and output, on a line before it can be determined whether the +3 volt level will be effective. Information about the component circuits is not now available in the field. In general, use a 0 volt level and work back to an input or an output which gives the required +3 volt level.

Power supply voltages are present on some pins. Exercise care not to ground these pins.

NOTE: Insert a 470Ω resistor to act as a load limiting resistor in the jumper used for tying down lines.

Card Reader I/O

Run all cards out of the card reader punch before powering down. Powering down the card reader punch when the card punch is loaded with cards results in a card laced in column one. Use the provided diagnostic tests as masters and reproduce the deck before using the deck to reduce exposure to having to re-keypunch cards. Make customer aware of the lacing of cards.

SAFETY

Personal safety cannot be over-emphasized. To ensure your own safety, make it an every day practice to follow safety precautions at all times. Become familiar with and use the safety practices outlined in the pocket-size cards, IBM Forms 124-0002 and MO 4-8401, issued to all Customer Engineers.

Voltages

Potential difference within the electronic gates, printed cards, and display back panel is +48v dc to -3v dc. Do not remove or replace circuit cards when dc power is on. Do not short out or bypass safety features.

Power Supplies

Extreme care must be exercised when servicing or inspecting the power supply even though the voltage range on the machine is low. Dangerous voltages and currents are present even when the system is in a power-off status. If it is necessary to connect a test instrument within the power supply, or to reach into it for any reason, disconnect the main-line cord. Discharge capacitors before working near them. Each heat sink is at an electrical potential. Do not short heat sinks to each other or to the machine frame.

Grounding

Convenience outlets for Customer Engineers are provided in the 1131, 1132, and 1442.

Machine grounding is required. Three-wire grounded power cords are provided. The third wire is for grounding and must not carry current from any source. IT IS IMPORTANT TO THE SAFETY OF PERSONNEL THAT IF ANY MACHINE OF A GROUP IS GROUNDED, ALL OTHER EQUIPMENT OF THE GROUP MUST BE GROUNDED. Grounded machines must be placed so that it is not possible for a person to touch both a grounded machine and any ungrounded metal equipment. Grounded machines do not present a hazard in themselves; the real hazard is from ungrounded electrical equipment.

Console Printer (Modified IBM SELECTRIC ®)

Working in certain areas of the typewriter is particularly hazardous due to the positive action of the typewriter. Follow safe working practices. Because it is not possible to foresee each individual area of exposure, the following general rules serve as a guide when working on this equipment.

1. At the completion of a service call, replace gear guards and dust shields. These safety guards are installed to prevent the operator from placing his hands too near moving parts. Because most operators do not have a complete knowledge of the mechanical workings of the machine, the only way they can be adequately protected is to place guards over the exposed areas. Be cautious when servicing this machine during the time the rear guards and dust shields are removed.
2. When lubricating, replacing parts, etc., make sure the machine is turned off. It is a good idea to remove the motor plug from the socket after turning the switch to the off position.
3. Exercise caution when handling the motor. The shaded-pole motor used in this machine runs considerably hotter than the capacitor type motor used in the Model B typewriter.
4. Be particularly careful to avoid injury to the hands from sharp edges on stamped parts, springs, links, etc. when picking up and handling all types of machines. Although the safety of the operator and the CE is one of the prime considerations in the design of the product, mass production techniques do not permit separate operations on each part to provide a smooth edge.
5. Wear safety glasses when performing any work that could result in parts, lubricants, cleaning solvents, or any other materials contacting the eyes.

NOTE: The word CAUTION is used in this manual to indicate procedures that require extra precautions to ensure personal safety.

DIAGNOSTIC TECHNIQUES

1.1 TROUBLESHOOTING

1.1.1 Introduction

The service philosophy of the 1130 system is based on the effective use of diagnostic programs and techniques. These programs and techniques depend heavily on the multiple modes of operation of the processor and of the console indicators to define problem areas. It must be recognized that the programs and techniques cannot always eliminate the need for detailed pulse and voltage checking, but they are designed to reduce this detailed evaluation to a minimum.

When a failure occurs, note all pertinent information. Record the contents of all registers and console panel indicators on a check sheet for later reference. Try to localize the failure before removing the machine from productive work.

The +12 and +48 volt supplies do not power down the system if either has a power failure. The system does not run if these voltages are missing and the supplies should be checked first to determine their condition.

The increased realiability of electronic components suggests that the majority of general service problems are electro-mechanical in nature. These problems are caused by mechanical adjustments, mechanical wear, electrical timing, and loose connections.

Diagnostic procedures have been provided to assist in isolating troubles between the electronics of the processor and the functions of electro-mechanical peripheral devices.

Keep in mind two other problem sources, program troubles and electrical noise troubles. Because the 1131 processor depends completely on programming for all input and output functions as well as for processing, program timing errors and incorrect data can appear as electronic processor or I/O problems. The diagnostic programs are designed to exercise and examine the functions of the processor and I/O devices. In general, the tests provide the assurance needed to guide problem analysis to the machine or the program. Electrical noise can be a problem due to the low level signals used in this and other solid state systems. Critical evaluation during test assures that the system is free from electrical noise interference anticipated in most environments. Suppression circuits have been designed into the system to reduce exposure to both internal and external interference. However, there is always the possibility of unique external conditions or of the failure of grounding or suppression circuits. While there are no unique tests or tools available to pinpoint electrical noise, the diagnostic section of this manual does provide some analysis procedures which can assist trouble analysis when electrical interference is suspected.

Note: For problems that do not seem to lend themselves to analysis, check that all cards and interboard connectors are in place and seated.

1.1.2 Error Detection

All data entering core storage has odd parity added to each half word. The parity is checked when reading out of core storage. A parity error in core results in the processor stopping at the end of the core storage cycle in which the parity error condition is detected. Parity bypass is under CE switch control, not under program control.

The I/O devices have checking circuits with error checks which can be recognized by programmed interrogation of the corresponding Device Status Word (DSW); Disk Storage, 1132 Printer, and 1442-6 or 7 Card Reader-Punch. Each of these devices, except Disk Storage, uses a visual indicator to alert the operator to the fact that an error has occurred. System diagnostic programs provide for error handling techniques for program recognizable input data errors, and supply printouts to aid in diagnosing troubles.

1.1.3 Error Isolation

The CE switches under the right hand top cover provide specific functions for processor error isolation. Bit switch data can be written into core and then read back for parity verification. Bit switch data can be cycled through the processor and registers without reference to storage. Interrupt request can be inhibited. Indicator lamps can be mass tested.

In addition to the CE switches, four modes of operation (single step, single cycle, single instruction, and interrupt run) are available at the console. These modes are described in detail in section 1.1.5.

To further assist error isolation, the single disk storage can be disconnected from the system and operated in the read mode under CE switch control. The processor can also be operated independently of the disk storage when it has been disconnected from the system.

The I/O devices are capable of limited mechanical operation independently of the processor. In general, independent mechanical operation of the devices cannot be performed without affecting processor performance.

It is possible to remove the devices from the system by disconnecting their signal connectors. In some cases it is necessary to ground interrupt level lines to permit operation of the processor with the device removed. The following chart indicates which lines must be grounded, if the I/O device is removed from the system, to maintain processor operation.

Device	To Block	Tie Down	Logic Page
1442	Level 0	B-A1J7-B13 to GND.	KM201
	Level 4	None *	
1132	Level 1	B-A1G7-D11 to GND.+	KM301
1627	Level 3	None	
1055	Level 4	None *	
1134	Level 4	None *	
1055	Level 4	A-C1G4-D02 to GND.	KT201
Disk Storage	Level 2	B-A1G6-D12 to GND.	KM311
Console Printer	Level 5	None *+	
Cycle Steal	CS Level 0	B-A1F7D10 to GND.**	
	CS Level 1	B-A1F7D11 to GND.**	

\+ Note: Forms Check Light On.

* No tie down on these levels are required if some other device using that level is also attached to the system.

** No tie down required unless cycle steal feature is not installed.

The console I/O printer cable connections are identical to those on a 1053 except for one wire and can be tied into the OLSA tester by interchanging the wire from H7 to R8 at H7 with the wire on H8. The 1053 jumper card part 747579 is needed to attach the female plug on the I/O printer cable to the female connector in the OLSA. The console printer must be returned to normal before the system is returned to the customer.

If an I/O device is removed from the system, the program must not address that unit or the program may hang up waiting for a device interrupt.

If it is desired to bypass the error stop when a 1442 read error occurs, isolate pin D05 of the card in location A-B1H2 (logic page XR291). If it is desired to bypass a punch error, isolate pin B05 of the same card. This allows operation of the 1442 in spite of the error condition. Be sure the circuit is restored to normal before returning the system to the customer.

1.1.4 Dynamic Detection

Within the processor, all data is parity checked when being read from core storage. A parity error results in an immediate stop of the processor if the parity run switch is off. Parity errors can be bypassed for CE analysis.

The most basic dynamic detection tools are the system diagnostic programs. Function, unit, and timing tests provide error handling capabilities and error looping routines to facilitate problem analysis. Within the diagnostic programs, unit device failures are handled with device status word bits. The sensing of these bits under program control results in printouts or halts which can be analyzed to identify the unit and type of failure and guide corrective action.

Intermittent error logging is a useful tool. Such logging can provide data to evaluate system integrity. It can also assist off line analysis and reduce system downtime to a minimum. Logging facilities can be designed into customer programs but are presently not available as a part of the system programming packages.

1.1.5 Static Detection (CE Control)

The following modes of operation are under switch control to assist the CE in analyzing and detecting machine failures.

Run Mode: The system functions as a normal processor. Program detectable errors under diagnostic test operation result in halts, print out routines, punch out routines, or a combination of these. Diagnostic tests provide for looping within specific functional areas under console entry switch control during the main diagnostic program. Diagnostic tests are built from basics and increase in complexity, providing a high degree of serviceability.

Run Interrupt Mode: A level five interrupt occurs after each main line instruction. This mode can be used for tracing main line, branch, or sub-routine operations.

Single Instruction Mode: The processor stops after each instruction is executed. The start key controls the advance.

Single Machine Cycle: The processor executes a single clock cycle T0-T7, E, I, IX, IA, etc., under control of the start key. SMC can be used to investigate CPU functions with every cycle taken by memory.

Single Step: The processor executes a single clock step, i.e., T1 under control of the start key. Pressing the single step key results in the generation of an A pulse, the release of the key results in a B pulse.

Exercise care when using single step because core data can be destroyed if the processor is reset or if the mode switch is changed between T0 and T6 time.

1.1.6 Special Techniques

Failure to Program Load (card system): (Figure 1-1) The initial problem is to define whether the card reader or the processor is at fault. The following procedure can assist diagnosis:

1. Try one card programs. If these do not lead to an immediate fault location, load core with hex 7000 (MDX) using the bit switches and the storage load switch. Press reset and start the program by pressing the start key. This causes the processor to perform a no-op operation. By changing the displacement through core, the instruction operates as a branch. If the MDX instruction operates properly, enter hex C000 (load accumulator) in location 0000. Enter hex D000 (store accumulator) in location 0001. Reset the CPU and press the start key. This simple routine loops and sets hex D000 in every core location. If these routines run, check the system using the following flow chart.
2. An incorrectly adjusted read emitter causes intermittent loss of interrupts. In this case the last words in the read in area are blank and the data read is in adjacent positions. Failure to read a column (assuming an interrupt occurs) results in blank words within the 80-word field causing a read register check or a feed check.

Double incrementing of the I counter on program load causes blank words in core on program load.

Card Feeding (no program): A technique for causing the 1442 to feed cards without a program in the machine is sometimes needed. This technique is

1. Load the read hopper with cards.
2. Turn the mode switch to single step.
3. Press the program load key.

Cards continue to feed as long as the program load key is held. The program load key may be blocked down and the feeding controlled by the 1442 start and stop keys.

1.2 THE MAINTENANCE DIAGRAM MANUAL (MDM)

The following paragraphs define the organization and contents of this manual.

1.2.1 IBM 1130 Configurator

- Defines the maximum system configuration.

1.2.2 System Data Flow Diagram

- Shows over-all data flow of the 1130.
- Shows exits and entries to I/O.

1.2.3 Unit Data and Control Diagram (UDCD)

- Expands each unit contained within the system data flow diagram to include major controls.

1.2.4 I/O Operations Diagrams

- Shows the over-all functions of I/O operations in positive logic diagrams.

1.2.5 Simplified Logic Diagrams (SLDs)

- Contains logic diagrams, arranged in an understandable manner, of those complex areas of the system where an additional level of logic is desired for clarity.

1.2.6 Logic Flow Charts (CLFC)

- Shows in condensed form, the concept of a particular operation.

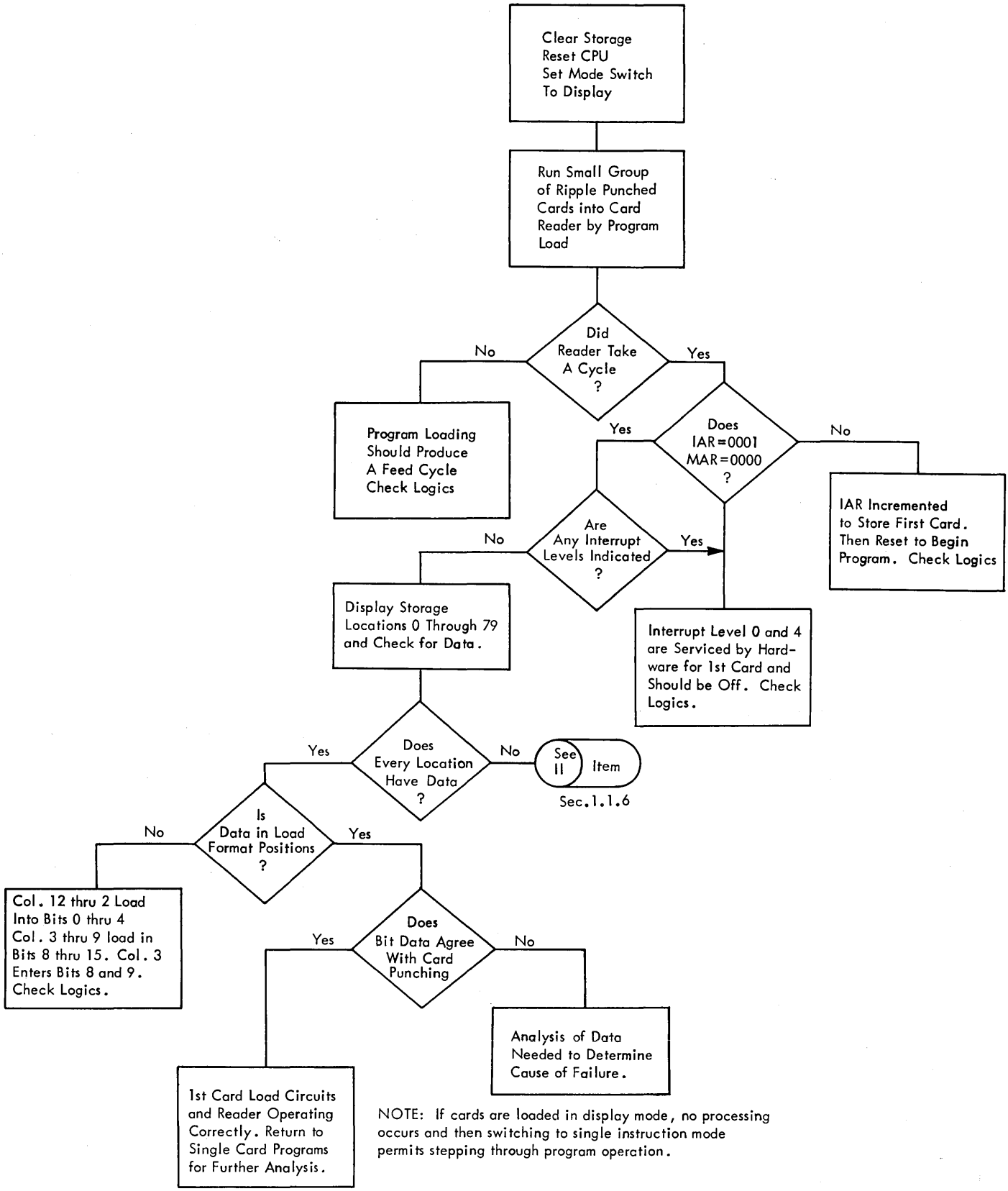


Figure 1-1. Program Load-Flow Chart

*NOTE: The illustrations in this manual have a code number in the lower corner. This is a publishing control number and is not related to the subject matter.

1.2.7 Timing Charts (T)

- Contains diagrams depicting the timing conditions of applicable operations.

1.3 DIAGNOSTIC PROGRAMMING AND MACHINE CHECK OUT

Diagnostic programs provide rapid diagnosis of many system troubles. The console panel is useful for controlling manually entered tests used when diagnostic programs cannot be run.

1.3.1 Maintenance Diagnostic Programs

- The information on the diagnostic programs presented here is for general use only. Detailed descriptions of the programs and their use are provided with the programs.

The maintenance programming system was developed to test and check, as completely as possible, the data paths, checking circuits, control functions, timing relationships, registers, mechanical adjustments, and I/O interaction.

The various programs that test the individual machine functions provide detection, degrees of localization, and communicate to the CE those indications of machine status which assist him in repairing the problem rapidly.

1.3.2 Program Language

The maintenance program system is programmed using the 1800/1130 standard assembler program language. The listings follow the standard assembler program format and include comments and explanations to help the CE understand and follow the program operation.

1.3.3 Program Control

Manual control of the maintenance program system is provided as follows:

1. Stop or continue on error.
2. Loop program, loop routine, loop function, or loop on error.
3. Bypass or allow error type out.
4. The program can bypass or allow manual intervention requests.

1.3.4 Error Messages and Documentation

These items are included in either the error messages or documentation, or both.

1. The location in the program of the failing routine or function.
2. The cause of the program halt or error message.
3. The function or functions that failed.
4. A comparison of the actual results to the expected results.

1.3.5 Program Loading

The maintenance programs are provided on cards and paper tape.

1.3.6 Tests for Device Interaction

The diagnostic monitor has the facility for controlling up to six test programs simultaneously, depending on core size, to provide overlapped or interaction operation of devices.

1.3.7 Operation Modes

The maintenance programs are designed to run in one of two modes, independent mode or dependent mode.

1.3.7.1 Independent Processor Tests

These programs assume complete control of the system and run independently of any other program. All I/O functions and interrupt controls are handled within the program. Errors are indicated by error halts which are described in the documentation.

Function Tests: These tests are engineered specifically to exercise and evaluate each of the functions of the system.

The function tests are designed to provide thorough fault detection (data, sequence and interaction related problems may not necessarily be detected by a function test), with short run time and minimal program size.

These programs use the building block approach, that is, the simplest instruction is tested first and no instruction is used to test another instruction until it has been fully tested itself. The procedures for running the tests are given in the CPU test index in the test documentation.

Tests included in the independent mode are:

1. CPU function test
2. Core storage function test
3. Core storage adjustment test
4. Basic diagnostic loader
5. One card diagnostic programs (7)
6. Program load manual tests
7. Interrupt test

The program load manual tests are used when none of the other function tests will load. To diagnose this type of trouble, the CE must use the test facilities provided on the console. To optimize his performance in the use of these facilities, a program load diagnostic guide, in the test documentation, has been developed. Instructions are entered one at a time through the bit switches and the instruction operation can be evaluated by the CE.

1.3.7.2 Monitor Controlled I/O Tests

These programs run under control of the diagnostic monitor and may be overlapped. Errors are indicated by error messages printed out on the 1131 Console Printer.

All I/O programs run under control of this monitor. Under this control, programs can be run one at a time, run in a predetermined sequence, or run simultaneously in any combination, except as limited by core size.

Two versions are available; card and paper tape. Program selection is via the bit switches.

This program controls the I/O function tests and incorporates the functions of housekeeping, program loading and execution, interrupt handling, error handling and customer engineer communication, such as printouts. The documentation provides an I/O monitor test index to aid in running these tests.

The following programs are provided:

1. Paper tape reader/punch function test
2. 1131 Console/keyboard function test
3. 1132 function test
4. 1442 function test
5. 1442 timing test
6. 1627 function test
7. Disk storage function test
8. Disk initialization program

1.3.7.3 1130 Maintenance Diagnostics Part Numbers

The chart below gives the part numbers of the diagnostic programs and the documentation for the programs.

Program	Program Listing	Card Deck or Paper Tape	Documentation	Flow Charts
1. Monitor	2191200	2191201	2191202	2191203
2. CPU function test	2191204	2191205	2191206	2191207
3. Core storage function test	2191208	2191209	2191210	2191211
4. Disk storage function test	2191212	2191213	2191214	2191215
5. Disk initialization program	2191216	2191217	2191218	2191219
6. 1132 function test	2191220	2191221	2191222	2191223
7. 1442 function test	2191224	2191225	2191226	2191227
8. 1442 timing test	2191228	2191229	2191230	2191231
9. Paper tape function test	2191232	2191233	2191234	2191235
10. 1627 function test	2191236	2191237	2191238	2191239
11. Console/keyboard printer function test	2191240	2191241	2191242	2191243
12. Core adjustment test	2191244	2191245	2191246	2191247
13. Meter test	2191248	2191249	2191250	2191251
14. Basic diagnostic loader	2191252	2191253	2191254	2191255
15. One card diagnostic programs	2191260	2191261	2191262	2191263
16. Program load manual test	-	-	2191266	-
17. Interrupt function test	2191268	2191269	2191270	2191271
18. Maintenance routines	2191272	2191273	2191274	2191275

1.4 SERVICE CHECK LIST

1.4.1 General Information

1. On what operation does the machine fail?
   a. Diagnostic test.
   b. Customer work (Fortran, etc.)
   c. Op code during which failure occurred.
2. What is the frequency of error?
   a. Time of day.
   b. Environment (temperature, etc.)
   c. Does customer power fluctuate at certain time of day? (welder, heavy machinery, etc.)

1.4.2 General Check List

1. Have connectors and cards been checked for looseness or for bent contacts?
   a. Edge connectors
   b. Laminar bus (pins and terminals)
   c. TB connectors (power supply, power sequence, etc.)
2. Have grounds been checked? (1.9.1)
   a. DC isolated ground
   b. AC isolated ground
   c. Ground straps (check contact from the gate to the frame)
3. Have power supplies been checked?
   a. Voltage levels
   b. Ripple
4. Have fans and blowers been checked?
   a. Power supply fans
   b. Gate fans and blowers
5. Does the machine fail on margins?
   a. Normal margins ± 4%.

1.4.3 Core Storage Check List

1. Which lights are on?
2. Has indicator lamp test switch been checked?
3. What is the pattern of the failure?
   a. Greater or less than 4K; odd or even, etc.
   b. Picking or dropping bits
   c. What bits are affected?
4. Is the trouble in B register rather than core storage?
5. Core storage air flow correct?
6. Has component substitution been tried?
7. Have the sense lines been scoped?

WARNING: Use an insulated probe tip when scoping core as shorts in the core area can damage the core array. When adjusting pots in the core circuits, use the plastic alignment screw driver, part 460811, to avoid shorting to other cards.

Adjustments of the core storage timings and voltages should not be changed until proven to be out of tolerance.

1.4.3.1 Solid Core Failure, Limited Area of Failure

1. Record mode of failure.
   a. Bit pickup or drop out.
   b. Addressing failure.
2. Record pattern of failure.
   a. Build table of failures.
   b. If Y drive line is open, replace cards.
   c. If X drive line is open, replace cards.
   d. Make continuity check for open drive or sense lines.
   e. Check diodes on array.
   f. Remove array and check welds, and wires visually.
   g. If core is bad, replace array.

1.4.3.2 Solid Core Failure, General Failure

1. All addresses or all bits
   a. Turn on the storage load CE switch.
   b. Turn on all bit switches.
   c. System cycles through all of core and tries to enter all bits.
   d. Check SLT voltages to core (+6, +3, -3).
   e. Check +12v and output of regulator voltage at 8.5v.
      1. Adjust voltages if out.
      2. Replace regulator cards.

Note: Do not replace regulator cards if the output is ground, as the new card will be shorted out.

   f. Check timing signals
      1. Read/write, long time, short time, strobe, emitter strobe.
   g. Check V reference and VSA voltages.
   h. Check X and Y current by scoping voltage test points.

1.4.3.3 Core Failure, Intermittent

1. Check SLT voltages to core (+6, +3, -3).
2. Check +12v and output of regulator voltage at 8.5v.
3. Check timing signals.
4. Check V reference and VSA voltages.
5. Check X and Y current by scoping voltage test points.

1.4.4 Addressing Failure Check List

Addressing failures can be very elusive, due to the branching, indirect addressing, and effective addressing features of the CPU.

This list will help the CE isolate such failures.

1. Record all console indications of the failure (IAR, M register, and B register).
2. If cycle steal addressing trouble is suspected, it may be necessary to statically check the addressing circuits. The CE indicators can be wired to help evaluate the addressing circuits.
3. Using the core service techniques, try to evaluate whether the trouble is in core storage or in the addressing circuits.
4. Trace routines using the interrupt run mode of operation should be considered.

A simple routine which stores the IAR and returns to the mainline program on any branch or instruction is helpful to see how far the program progressed before it failed.

Be aware that this kind of operation can be misleading if the first branch is to data which is acted upon as an instruction.

1.4.5 Core Storage Console Isolation

1. Load system to all bits.
   a. Turn on the storage load CE switch.
   b. Turn on all bit switches.
   c. Turn the mode switch to load.
   d. Press the start key.
2. Stop and reset the system.
3. Turn off storage load CE switch.
4. Turn on storage display CE switch.
5. Turn function switch to display.
6. Press the start key.
7. Machine stops with a parity error.
8. Storage address register bits on indicate the failing X-Hi-or-Low, Y-Hi-or-Low driver. Example,

   M register 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

   The bad driver is Y-Hi-RD/write gate 011 at B-C1G3 according to the core unit plugging chart, SD021.

If B register does not contain all bits, the trouble is in a sense/inhibit card. Picking bits may be checked by changing step 1-b to: No bit switches on.

In the event of an intermittent failure, a recording of each failure must be made, indicating the M register address and B register contents and parity bits.

An M register bits on pattern should develop if the failure is in X or Y line circuits.

If no M register pattern is evident, examine the words in B register for a pattern. Remember that parity bits indicate which half of the word is wrong. A failure indicates a failing sense amplifier or an inhibit driver (same card).

No pattern in either area indicates a problem in address or strobe time generation.

1.4.6 Current Scoping of Core

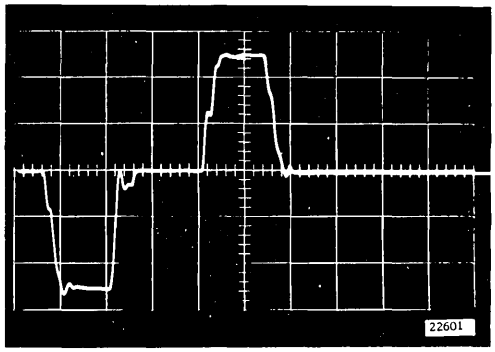
1.4.6.1 Initial Oscilloscope Set Up

1. If a particular address is in question, load MDX *-1 (hex 70FF) into that address, using CE and bit switches, to provide a one instruction loop.
2. Oscilloscope
   a. Current probe in channel 1
   b. Time Base: 05 μs/div.
   c. Vertical input channel 1: 0.1v/div.
   d. Sync on rise of T0: +DC, external B-A1J2B13.
3. Core set up.
   a. Remove jumper block for position desired, using removal tool part 2108860 and pulling straight out.
   b. Install ten 4" jumpers in place of the jumper block following the printed circuit pattern on the back of the block.
   c. Hang current probe on specific jumper.

1.4.6.2 Core Array Waveforms

The following examples of core storage waveforms were obtained using a 561A oscilloscope plus the oscilloscope and core set up described in the section above, and hex address 0000.

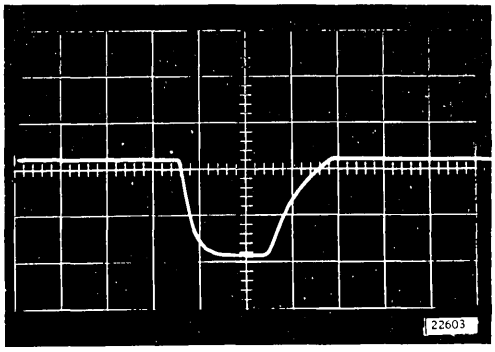
Y-Line Current



Oscilloscope set up:

1. Initial set up.
2. Channel 1 - Y read gate, write driver B-C1K5B04.
3. Block at C1K5 removed and jumpered.
4. Reference SD221.

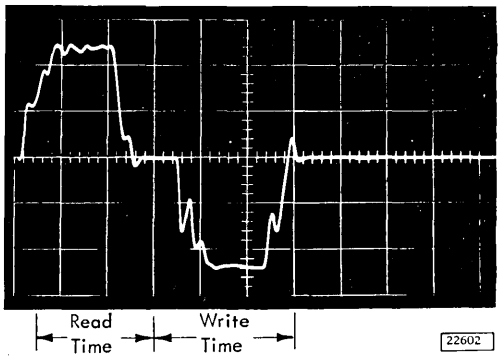
Inhibit Drive Current



Oscilloscope set up:

1. Initial set up.
2. Channel 1 - Inhibit bit 4 (bit 4 = 0) B - C1E7D04.
3. Block C1E7 removed and jumpered.
4. Reference SD403.

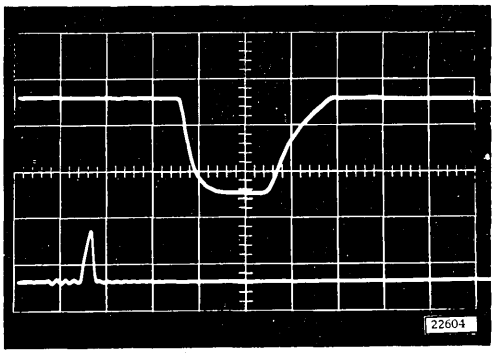
X-Line Current



Oscilloscope set up:

1. Initial set up.
2. Channel 1 - X - read gate, write driver B-C1J6B02.
3. Block at C1J6 removed and jumpered.
4. Reference SD222

Sense Line With No Bit

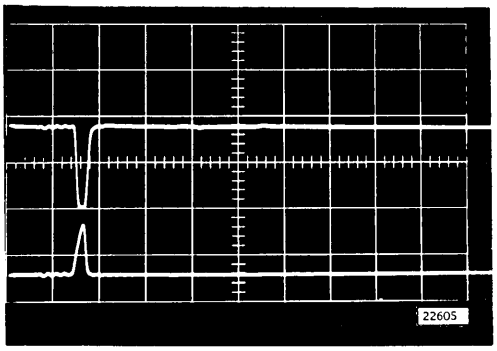


Oscilloscope set up:

1. Initial set up.
   a. Channel 2 - voltage probe.
   b. Channel 2 set to 0.2v/div.
   c. Mode switch set to ALT.
2. Channel 1 - inhibit/sense bit 4 (bit 4 = 0) B-C1E7D04.

3. Channel 2 - strobe pulse B-C1B6B07.
4. Block C1E7 removed and jumpered.
5. Reference SD403.

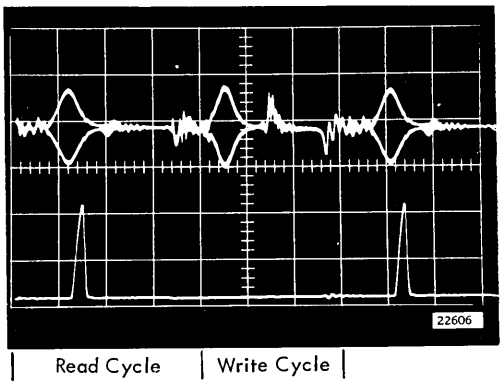
Sense Amplifier with a One Bit



Oscilloscope set up:

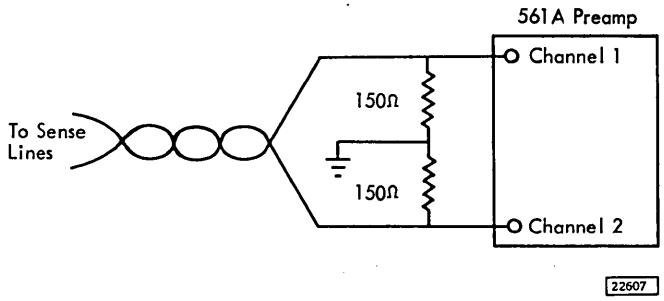
1. Initial set up
   a. Channel 1
      1. Voltage probe
      2. 0.05v/div.
   b. Channel 2
      1. Voltage probe
      2. 0.2v/div.
2. Channel 1 - sense amplifier one bit (bit 9 = 1) B-C1B3B10 (SD403).
3. Channel 2 - strobe B-C1H2B09.

Inhibit Sense Lines - Bit 3 = 1



Set up:

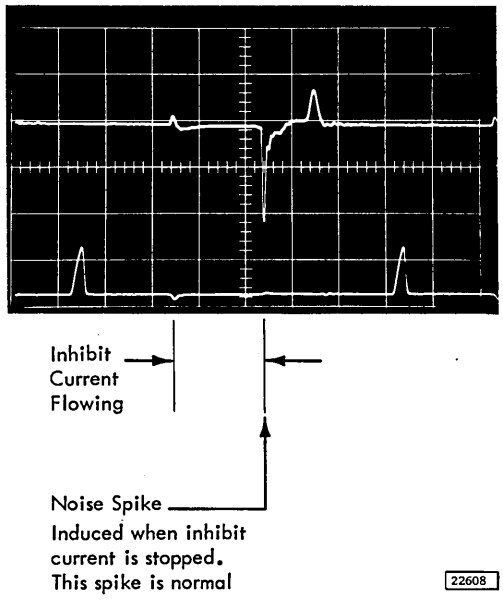
1. Console set up.
   a. Storage load and cycle switch on.
   b. Bit switch 3 on.
2. Oscilloscope set up.
   a. Channel 1 and 2 set on AC input and 0.05v/cm.
   b. Vertical mode switch set to added.
   c. Input to channels 1 and 2 are twisted pair wires set up as shown.



   d. Sweep set to 0.5 μs/div.
   e. Sync + DC external on T0 B-A1J2B13.
   f. Connect twisted pair to B-C1B5B02 and B-C1B5D02 (SD403).

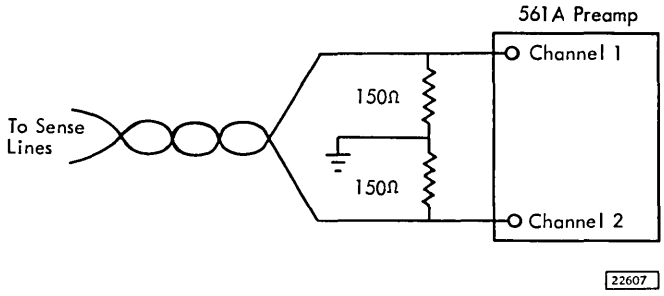
The first two envelopes are read cycle and write cycle respectively. The lower trace is strobe, and is shown for reference only and cannot be obtained without special equipment.

Inhibit Sense Lines - Bit 3 = 0.



Set up:

1. Console set up.
   a. Turn on the storage load and cycle switch.
   b. Turn on bit switch 3.
2. Oscilloscope set up.
   a. Channel 1 and 2 set on AC input and 0.5 v/cm.
   b. Vertical mode switch set to added.
   c. Input to channels 1 and 2 are twisted pair wires set up as shown.



   d. Sweep set to 0.5 μs/div.
   e. Sync +DC external on T0 B-A1J2B13.
   f. Connect twisted pair to B-C1B5B02 and B-C1B5D02 (SD 403).

1.4.7 Core Diagnostic Aids (Figure 1-2)

1. Core wave forms are the same while cycling core with either the CE storage load or display switch on. With the storage load switch on, parity errors do not stop the machine. Core is read out to the B register and read back in from the bit switches. With the display switch on, and the parity run switch off parity errors stop the machine. Core is read out to the B register and is read in from B register. Any bits dropped in this mode are lost. For analyzing a failure from the console, the display mode is probably best.
2. Current control card failures cause errors at random core addresses. Some addresses fail more often, but this is only because of circuit characteristics. To check the current control cards, turn on the CE storage load switch. Turn on the bit switches to the desired configuration and press the start key to cycle core. Scope B2B09 to check for Y dimension. X dimension (M2B09) duration corresponds to long time, Y dimension is short time. The amplitude of X and Y are equal and approximately 2v to 2.5v. This amplitude is a function of the V-Ref voltage. V-Ref can be checked against the voltage reading recorded on the core voltage label to see if it is correct.
3. Scoping the current control card test point (M2B09 for X, B2B09 for Y) shows if all read/write drivers are conducting. If a driver fails to conduct, there is a light trace across the bottom of the pulse for that dimension. If two drivers are conducting at the same time, however, these test points look normal.

   Two drivers conducting together split the current for that dimension, resulting in neither address reading or writing correctly. When the defective driver is addressed, it works correctly because no other driver is conducting. When a good driver is addressed, the defective driver conducts also, causing both to fail. If this failure is suspected, stop the increment of the I register (IAR) (jumper BA1M2G13 to D08) and cycle core in a failing address. Using a current probe, scope the X and Y dimension drive line for that address. (See current scoping technique, Item 4.) There should be 210 to 265 MA through the lines. If one dimension has only half enough current, the failing driver is in that dimension. Analyze the failing addresses to find the defective driver.
4. Current loops are required in order to scope current on the 1131 core storage. The current loop block is put onto the pin side of the large board in place of the array connector block for the desired lines. Make up a current loop block using a single card extender, or offset, and the 4-inch SLT jumpers. Install the jumpers to the same configuration as the array connector block jumpers (SD021).
5. There is one inhibit driver for each bit in each 4K of storage. If an inhibit driver never conducts, that bit enters 4K of storage continuously. If it always conducts, the bit can never be entered into that 4K. Any other 4K segment of core functions correctly. If there is a bit failure through 4K of core exchange the inhibit driver and sense amplifier cards for that bit with another bit. If the trouble is not a card, but sense/inhibit failure is suspected, check the continuity of the sense/inhibit line.
6. There is one sense amplifier for each bit in each 4K of core. The variable sense amplifier

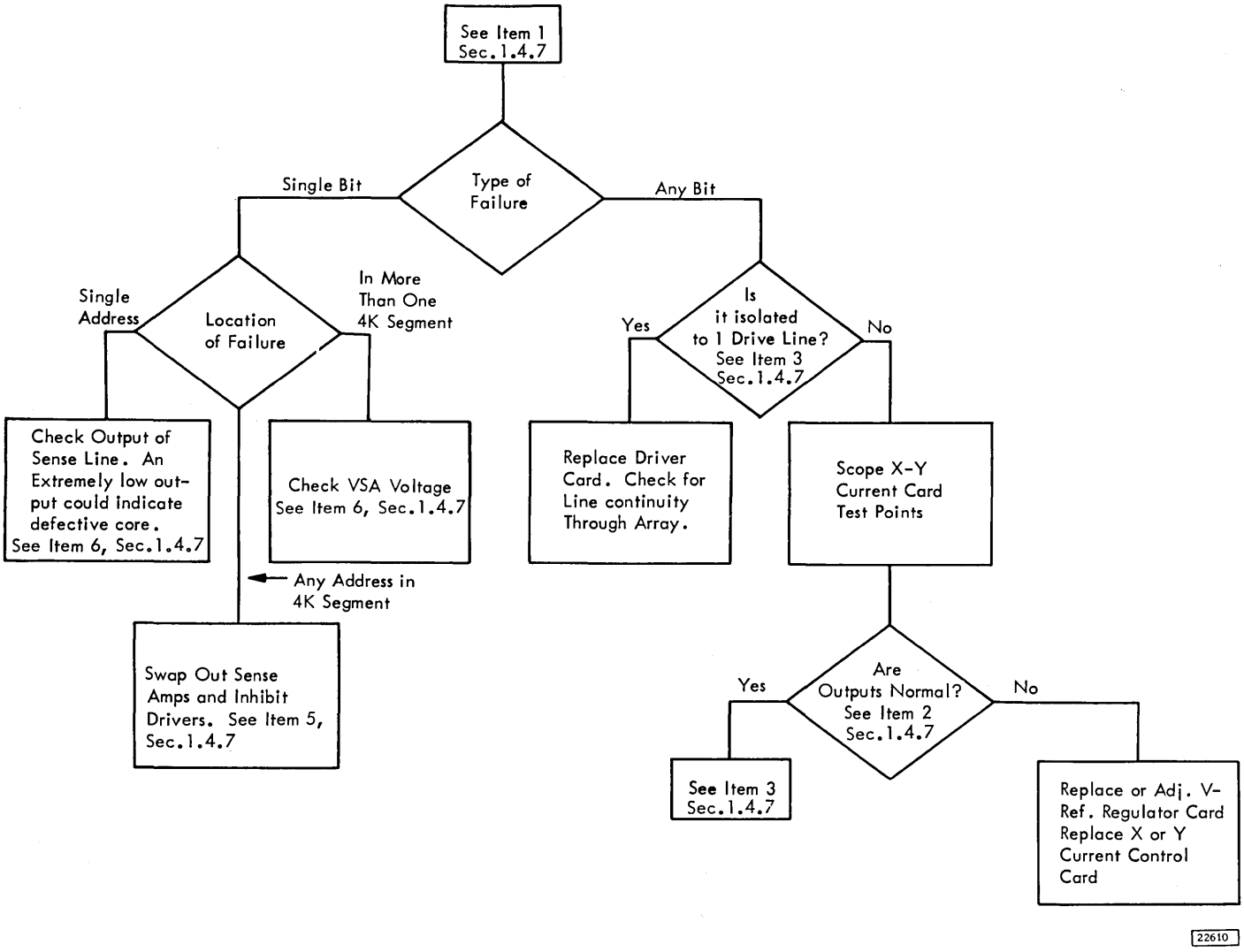


Figure 1-2. Core Flow Chart

(VSA) voltage controls sensitivity of the sense amplifiers. The factory setting is recorded on the core voltage label. Scope the output of the sense line to the sense amplifier using a differential amplifier as shown in section 1. 4. 6. 2. With the strobe single shot properly adjusted, The strobe output should coincide with the sense line output.

1. 4. 8 Transient Power Line Noise

Power line noise is characterized by lack of pattern. If transient noise is suspected, alert the physical planning representative to the situation. Some symptoms that have been noted in the field are:

1. Highly intermittent failures.
2. Failure defies any analysis by pattern.
3. Failures occur mostly during the day (commonly related to the start or end of a work day when large numbers of equipment are being turned on or off.
4. Week-end performance relatively trouble free.

1. 4. 8. 1 Methods of Determining Noise

1. Scope with the oscilloscope grounded on the power supply common.
   a. Suspected line.
   b. Ground pins on SLT boards containing failures (noise level should be less than 1 volt peak to peak).
   c. AC input lines of contractors.

2. Indicator - A latch or line level can be wired into a CE indicator. The line may need to be gated to indicate only the transient pulse.

1.4.8.2 Methods of Aggravating Noise Problems

1. Determine what other equipment is on the 1130 line. Run a program while turning on and off the power switches on this equipment, i.e., air-conditioning, units, heaters, other DP equipment, etc. (Check with customer first.)
2. Separate AC and DC isolated ground from machine frame.

1.4.8.3 Areas to investigate if noise problems are encountered or suspected:

1. Is system on separate power line?
2. Does system have a good ground return to power source?

1.5 CONSOLE PANEL

The console bit switches and associated circuitry provide the ability to store in or read out from core storage data and programs. A complete description of the console panel and its uses are in Chapter 2.

1.6 CE PANEL

The CE panel has switches to aid the CE in his diagnostic procedures. Details on their use are given in Chapter 2.

1.7 CONSOLE PRINTER

1.7.1 Console Printer Diagnostic Aids (Figure 1-3)

1. Determine which data or control functions are failing. To determine which data functions of tilt or rotate are failing, check which characters are failing and use Figure 1-4 as a reference.

   Example: Tilt 2 and tilt 3 characters do not fail. Tilt 3 characters print for tilt 1 characters. Tilt 2 characters print for tilt 0 characters. These conditions indicate the function of T2 is at fault.

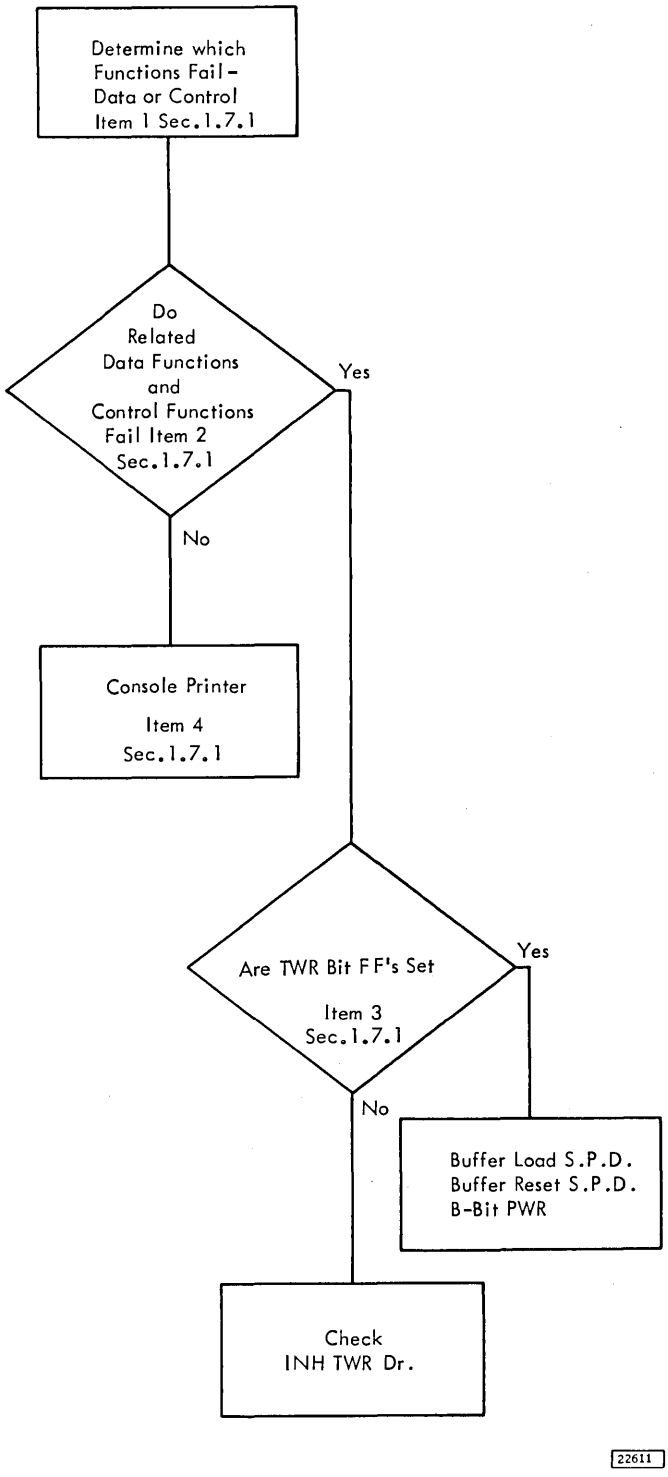


Figure 1-3. Console Printer Flow Chart

ROTATE

Clockwise ← → Counter Clockwise

Rotate Magnets	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5
UC LC 2A	1 E	3 E	5 @ E	7 > E	8 L	0 b L	2 E	4 : E	6 5 E	9 L	# - L
UC LC 2	E	T E	V % L	X ' L	Y L	‡ ¢ L	S E	U = L	W " L	Z L	, L
UC LC 1	J E	L . L	N * E	P ; L	Q E	! - L	K L	M) E	O Δ L	R E	$ L
UC LC .-5	A E-L	C E-L	E □ E-L	G < E-L	H E-L	? & E-L	B	D (	F ‡	I	. V

Tilt Magnet T1	Tilt Magnet T2	Tilt
E	E	0
L	E	1
E	L	2
L	L	3

E = Magnet Energized L = Latched on Bail

Note: For a +5, tilt 3 character the auxiliary magnet is the only magnet energized.
Head - Part number 1167969
Last three numbers of part number on the head.

22612

Figure 1-4. Typehead Chart

2. If there are failures in both data functions and control functions, determine if there is any relation between the failures, using Figure 1-5 as a reference.

   Example: The data function T2 and control function of carrier return are failing. These two functions are related in that they both use character word bit 0.

3. If there is a relation between data functions and control functions, check the associated TWR bit FF to determine if it is being turned on. If it is being turned on, the INH TWR DR line should be checked. If it is not being turned on, check the TWR buffer load SPD, TWR SPD, and the associated B-bit PWR line.
4. Investigate the console printer if one of the following is true:
   a. Data functions fail and control functions do not.
   b. Control functions fail and data functions do not.
   c. There is no relation between data function and control function failures.

1.8 MARGINAL CHECKING

There is no marginal check supply on the 1130 system. However, the logic supplies (+3v and +6v) may be varied by ±4% and the system should still operate trouble free. Consider power supply variation only after other isolation techniques have been exhausted.

Voltage settings on the 1130 system are critical. A precision meter is required to set voltages initially. The CE meter can be used for varying voltages if care is taken to record the initial setting and point of

Character Word Bit	Data Function	Control Function
0	T2	Carrier Return
1	T1	Tabulate
2	R1	Space
3	R2A	Backspace
4	R2	Shift to Red
5	R5	Shift to Black
6	Upper Case	Line Feed
7	Used for Control Function	

22613

Figure 1-5. Console Printer Word Chart

measurement and then to return to that setting after varying the voltage. Voltage swing is limited to ± 4% of the initial reading.

1.9 MISCELLANEOUS TECHNIQUES

1.9.1 Locating Grounds

1. Remove the green (or black) wire between dc isolated ground and frame ground.
2. Remove the green (or black) wire between ac isolated ground and frame ground.
3. Measure the resistance between any ground pin and the frame. The resistance should be in megohms. If not
   a. Isolate each gate by taking off ground terminal.
   b. Isolate each row by removing the wire that connects the row to the ground cable.

1.9.2 Locating Marginal SLT Cards

If an error shows when running the machine under marginal conditions, the SLT card giving the trouble can be found by isolating the gate where the problem is located by analysis of the circuit failing, i.e., I/O control, printer, CPU, etc.

WARNING: When a gate that appears to be giving trouble is located, the CE may find that the actual marginal card is the card which is driving the card located in the gate found by test. The marginal driving card may be in another gate.

1.9.3 Signal Levels

Acceptable signal levels are:

0v	range +0.0v to +0.3v
+3v	range +2.88v to +3.12v

These values are to be used only as a guide. They are expressed in general terms only and are not true for all circuits. However, circuits operating outside of these ranges should be suspect.

If interchanging a card does not affect a level which appears to be marginal, consider the driving and driven circuits connected to the card.

Special voltages have been noted in the line titles.

1.9.4 Transistor Delay Times

The transistors in the 1130 have an inherent delay time; that is, it requires time to saturate the transistor and time to unsaturate the transistor. In general, it takes longer to unsaturate than to saturate a transistor. These delay times are known as turn-on delay and turn-off delay. They are a function of the type of logic block being considered and the rising or falling of the output.

The total delay in a series of logic blocks is the sum of the individual transistor delays. If too long a delay is experienced in a series of logic blocks, the individual logic blocks should be scoped to see which block has too long a delay.

SLT cards have transistors internally connected to form a series of logic blocks. Because these circuits are all mounted on one card and connected internally, there may be no external check points between logic blocks (no input or output pins are shown in the systems diagrams).

Note: Turn-off delays (unsaturating) are generally the longest.

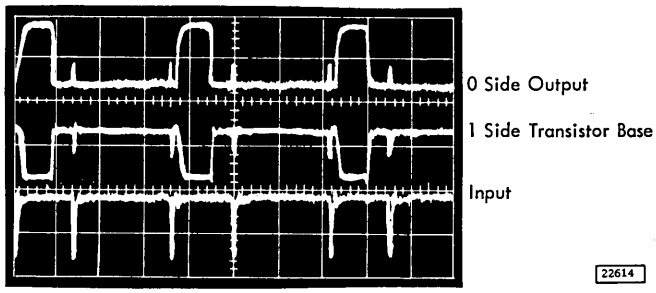
1.9.4.1 Measuring Transistor Delay Time

Transistor delays (slow response) can cause intermittent machine failures that are difficult to diagnose. A slow card may cause delays on either the rise or the fall of a pulse. A method for measuring transistor delay follows:

1. Sync Oscilloscope on the input to the card in question (while clock is running).
2. Probe the input and note the rise and fall time of the pulse.
3. Probe the output and compare with input pulse. The difference between the rise and fall times is the turn-on delay, and turn-off delay, respectively.

1.9.5 Multi-Input Flip-Flop's

Spikes are sometimes observed in the output lines of multi-input FFs. When multi-input FFs are in one state and inputs are given to drive the FF into the same state, a spike is reflected in the off side output.



These spikes are normal and the circuit design has taken them into consideration.

BASIC MACHINE

2.1 MANUAL CONTROLS AND INDICATORS

2.1.1 Objectives

- Provide manual operation for program and system analysis.
- Provide visual indication of machine and program status under the various system modes.
- Supplement areas which the program cannot check.

2.1.2 Control Switch Panel

2.1.2.1 System Reset

Function: Reset processor registers to their initial state, with the exception of the M register.

Operation:

1. Data or instructions in core storage is not affected.
2. Reset is active in all modes of operation except run mode.
3. In single step mode, it is necessary to be at T7 time to prevent loss of data or instructions when using reset.

2.1.2.2 Program Stop

Function: Causes a level five interrupt for the console. With appropriate sub-routines, this stop is used to cycle down the processor and I/O devices to a stop.

WARNING: If these routines are not in the program, use of the program stop key may cause loss of information.

Operation:

1. The program stop key is pressed and a level 5 interrupt is developed.
2. The bit-zero of the console keyboard-device-status-word is a one, indicating to the program that a program stop is requested.
3. A user-supplied programmed wait loop is required to block main line operations until the operator intervenes.
4. The interrupt routine should allow the program to continue when the start key is pressed.

2.1.2.3 IMM Stop

Function: Stops the processor immediately. Interrupt and cycle stealing occurs at T7 of the cycle in which the IMM Stop occurs.

Operation:

1. Data from I/O devices are lost if the devices are operating at the time of the stop.
2. A complete program restart is required.

2.1.2.4 Program Start - Push Button

Function: Causes the program to start or continue from its present state. The program continues according to the setting of the mode switch.

Operation:

1. If a program start routine is in the program and the start key is pressed after completing a program stop operation, the instruction being processed continues as though no program stop had occurred.
2. If the start key is pressed after reset, the instruction specified by the instruction counter (normally zero) is the first one executed. By using the load IAR function and entering a new instruction address, a different starting address can be manually inserted after reset.
3. Each time the start key is pressed the instruction address register advances when the machine is in load or display mode. When in single step, single memory cycle, or single instruction mode, the processor advances a single increment of the specified mode each time the start key is pressed.

2.1.2.5 Load IAR - Push Button

Function: In the load mode position, data entered in the bit switches is loaded directly into the instruction address register via the storage buffer register.

Operation:

1. The key is functional only when the processor is in the load or display mode.
2. When in the load mode, an address set in the bit switches is entered in the instruction address register when the load IAR key is pressed.
3. Display: When in this mode, the contents of the B register enter the IAR when the load IAR key is pressed.

2.1.2.6 Program Load - Push Button

Function: Provides a means for entering a program into the system.

Operation:

1. Paper Tape System
   a. Pressing the load key causes groups of four, four-bit characters (16 bit words) to be loaded into core consecutively, beginning at location zero.
   b. Groups continue to be read until a punch in the fifth channel is encountered.
   c. When a punch in the fifth channel is encountered, loading stops and control transfers to word zero.
2. Card Reader-Punch System
   a. Pressing the key causes a card to advance from pre-read through the read station.
   b. The contents of each column is stored consecutively in storage locations beginning at location zero.
   c. The 12 bits are split into five operation bits and eight displacement bits, two of which are sign bits.
   d. At completion of the card cycle, an automatic branch to 0000 is executed.

Note: If the card reader is installed, program load is not active on the paper tape. The system can be ordered without program load installed.

2.1.2.7 Console/Keyboard-Toggle Switch

Function: Sets bit position 3 in the keyboard/printer device status word (DSW) to indicate to the program that the keyboard is the source of input data during program control.

Operation: In the console position, the bit switches are the source of input data. In the keyboard position, the keyboard is the source of input data.

2.1.3 Mode Switch

- Rotary switch to control mode of machine operation.

2.1.3.1 Load Position

Function: Provides for manual entry of data or instructions from the bit switches to core storage or I register.

Operation:

1. In load mode, operation of the load IAR key transfers bit switch data (2-15) to the I register.
2. When in load mode, pressing the start key enters the bit switch data (0-15) into core storage at the address indicated in the I register. The I register is incremented by 1.
3. Switching from load to any other mode of operation does not affect storage or result in reset of any set conditions.
4. During machine operation, IMM stop or program stop keys must be pressed prior to switching to load mode to preserve the integrity of the data in core storage and to preserve the program.
5. It is not necessary to reset prior to switching to load mode. Such switching does not affect any set conditions other than the B register.

2.1.3.2 Display

1. Function: To display the data at any location in core storage.
   Operation: In display, pressing of the start key displays, in the B register, the data at the address specified in the I register prior to pressing of the start key.
   Pressing the start key successively displays sequentially increasing addresses. That is, the I register is incremented each time the start key is pressed.
2. Function: Load the I register with the contents of the B register.
   Operation: Depressing the load IAR key transfers the B register contents into the I register.

2.1.3.3 Run

Function: To condition the system for the start of programmed operation.

Requirements:

1. Pressing the start key in run mode results in program operation beginning at the address specified by the I register.
2. Pressing the IMM stop key halts machine processing at the end of the active cycle at T7 time.
3. Switching from run mode to any other mode requires IMM stop or program stop prior to switching to insure integrity of the core data.

2.1.3.4 Interrupt Run - (Int Run)

Function: Forces a level five interrupt after completion of each instruction.

Operation:

1. A level five interrupt occurs after the end of each instruction execution.
2. Higher level interrupts are handled automatically during this operation.
3. An interrupt-run program which stops on the level 5 interrupt and starts with the start key, is required to use this mode of operation effectively.

2.1.3.5 Single Step (SS)

Function: Pressing the start key advances the processor one clock cycle.

Operation:

1. Pressing the start key in this mode causes a T (X), phase A, pulse to be generated. Releasing the start key causes a T (X), B pulse.
2. Pressing the reset key in a single step mode causes loss of storage integrity unless the clock is in time T5, T6 or T7 and of program integrity unless in T7 time.

2.1.3.6 Single Machine Cycle (SMC)

Function: Advances the processor one complete machine cycle (T7 to T7) under control of the start key.

Operation:

1. Pressing the start key causes one machine clock cycle.

2.1.3.7 Single Instruction

Function: To advance the processor one complete instruction at a time under control of the start key.

Operation:

1. Pressing the start key causes a complete instruction to be executed.
2. I/O operations are completed to the point of interrupt request.
3. Switching to another mode of operation does not affect instructions or data.

2.1.4 Console Bit Switches

Function: Provide for manual entrance of a machine language instruction or binary data into core storage, an instruction address in the I register, or manual control by program interrogation.

Operation:

1. Data set in the bit switches can be loaded into core storage under program control.
2. When the machine is in load mode, the bit switches are gated directly into the B register.
3. The bit switches have no effect on the processor under any other mode except as addressed by an I/O command.

2.1.5 CE Panel

2.1.5.1 Storage Load

Function: Provides a starting point for isolating problems and checking the storage circuits.

Operation:

1. Data, as set up in the bit switches, cycles through all of core storage. Setting this switch allows cycling of memory by turning on the run controls and incrementing the I register.

2.1.5.2 Storage Display

Function: Provides for checking the core storage circuits.

Operation: The core storage contents are displayed in the B register console lights in a sequential manner. Setting this switch allows core storage to cycle by turning on the run controls and incrementing the I register. A parity error results in an immediate halt if the parity run switch is off.

2.1.5.3 Non-Storage Load and Cycle

Function: Allows console data (bit) switches to be used as a source of data in place of core storage.

Operation: With non-storage load and cycle (NSLC) switch on, the input and output to core storage is crippled. Input to the B register comes from the bit switches only.

An operation may be entered and executed from the bit switches, either in single step, single instruction, or run modes. If a valid operation code is entered and the mode switch is in run, the 1131 cycles through the operation code, incrementing the IAR and cycling again. This permits scoping of I cycles, E cycles and controls without disturbing the contents of storage. If an invalid operation code is entered, it is decoded as a wait command and the 1131 stops.

Example #1

a) Machine fails on any long instruction. By single stepping a double word instruction, it is found that there never is an I-2 cycle.
b) 1. Turn on the NSLC switch.
   2. Turn the mode switch to run.
   3. Set load accumulator long instruction in the bit switches (hex C400).
   4. Press the start key. The 1131 cycles and the I-2 circuits may be scoped dynamically for the failure.

Example #2:

In order to examine an XIO instruction and IOCC in single step or single machine cycle mode, the following technique may be used:

1. Turn on the NSLC switch.
2. Turn the mode switch to single step or single machine cycle.
3. Set up XIO instruction in the bit switches (hex 0800).
4. Step through the I1 cycle to E1, T0 time by pressing the start key.
5. Change the bit switches to the desired IOCC word, i.e. device, function codes.
6. Continue to step through the IOCC operation.
7. If the function of the IOCC was a sense command, the DSW is brought into the A register. If the device had been a 1442, with a feed command, a card would have fed from the hopper, etc.

2.1.5.4 Interrupt Delay

Function: Blocks Interrupt.

Operation: The interrupt delay switch, when on, inhibits setting of the interrupt request circuits.

2.1.5.5 Parity Run

Function: Provide a means of bypassing the error when an out of parity character is read out of core storage.

Operation: When the parity run switch is in the on position, errors do not stop the system. When the parity run switch is in the off position, the system stops at the end of the cycle in which the error is detected.

WARNING: This switch must be returned to the off position before the system is returned to the customer.

2.1.5.6 Lamp Test

Function: Tests all lamps to see if they are in good condition.

Operation: Pressing the lamp test switch lights all indicator lamps.

2.1.6 Miscellaneous Switches

2.1.6.1 Power ON/OFF

Function: Provide for removing or applying power to the entire system. When off, 24 vac is still up and the convenience outlet power is off.

2.1.6.2 Disk Storage ON/OFF

Function: Provides for removing or applying AC power to the disk drive unit.

Operation:

1. Controls the drive motor.
2. Provides, indirectly, the head load and unload facility.

2.1.6.3 Emergency Power Off

Function: Removes power to every unit of system including convenience outlet but not to the 24 vac supply.

Operation:

1. Requires CE intervention to reset.

2.1.6.4 Power Supply Voltage Potentiometer

Function: Provides ability to set each dc voltage accurately. It can be used to help isolate marginal circuit conditions. Located on each supply.

Operation:

1. Allow voltage variation of processor dc voltages ±4%, one at a time. This is not considered a normal trouble shooting procedure.

CAUTION: The potentiometer is not mechanically stopped to prevent over voltage loss of power.

2.1.7 Indicators

2.1.7.1 Power

The ready light on the keyboard console indicates power ON/OFF.

2.1.7.2 Console

Instruction Address Register (IAR) has 14 positions and provides full time indication.
Storage Address Register (SAR) has 14 positions and provides full time indication.
Storage Buffer Register (B) has 16 positions and provides full time indication.
Arithmetic Factor Register (D) has 16 positions and provides full time indication.
Accumulator Register (A) has 16 positions and provides full time indication.
Accumulator Extension Register (Q) has 16 positions and provides full time indication.
Operation Register (OP) has 5 positions and provides full time indication.
Operation Tags has Flag bit 5, Tag bits 6 and 7, Mod bits 8 and 9.
Condition Register has 2 positions and provides full time indication of carry and overflow.
Cycle Control Counter has 6 positions and full time indication.
Interrupt Levels has 5 positions and indicates interrupt level.
Machine Cycle Indicators has 7 positions, indicates type of I or E cycle and provides full time indication.
Clock Cycle Indicators has 8 positions, displays T Clock position when in Single Cycle operation and provides full time indication.
Special Arithmetic Indicators has 6 positions and provides full time indication. Add, Arith Control (AC), Shift Control (SC), Accumulator Sign (AS), Accumulator Carry (TC), Zero Remainder (ZR).

CE Indicators: There are 12 indicating lamps located in the lower portion of the lamp panel. These can be used to indicate circuit conditions as needed.

Input to each lamp is shown on logic page ZL101. The input level must be plus to light the indicator.

The lamps require no external driver. Therefore, any normal signal level may be used as an input without concern for loading the circuit excessively.

Example:

While stepping through a program, if indication is desired each time the accumulator equal zero flip-flop comes on (KG221), wire CE indicator #1 to the FF so that it indicates the on condition. To accomplish this, wire B-A1E2-B04 to B-A1A3-B13.

Location of Terminals

CE Lamp 1	B-A1A3B13	CE Lamp 7	B-B1M2B13
CE Lamp 2	B-A1A3D13	CE Lamp 8	B-B1M2D13
CE Lamp 3	B-A1A4B12	CE Lamp 9	B-B1N2D13
CE Lamp 4	B-A1A4D12	CE Lamp 10	B-B1N2B13
CE Lamp 5	B-A1A4B13	CE Lamp 11	B-B1N4B12
CE Lamp 6	B-A1A4D13	CE Lamp 12	B-B1N4D12

X7 Clock Indicator has 1 position, displays X clock 7 when in single cycle operation and provides full time indication.
Wait is on when CPU is in wait condition.
P1-P2 has 2 positions, uses parity bits to indicate when the half word read from core storage is even.
Index Register displays index register address.

2.1.7.3 Keyboard Console

Forms Check is on if console printer is out of paper.
Keyboard Select is on when request for keyboard interrupt has been serviced and keyboard is ready to operate.

Alpha Shift is on when the keyboard is in the alpha mode.

Numeric Shift is on when the keyboard is in the numeric mode.

Parity Check is on with the recognition of a parity error; either halfword read out of core storage is even and the parity bit is not on.

Ready is on as soon as +48v power comes up. Indicates power on and processor ready.

Run is on with the CPU in run mode and the start key pressed.

Disk Unlock goes off with a cartridge in place and the heads loaded and at 000.

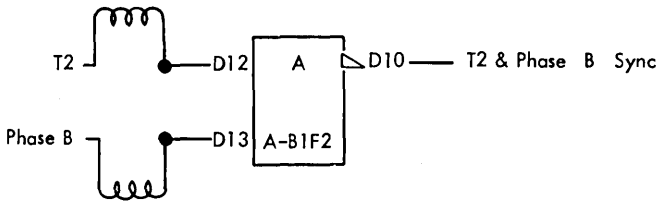
2.2 CE CARD

A CE card has been furnished in location A-B1F2. The card contains six circuits which can be used as minus OR's or plus AND's. Each circuit may be wired, by using jumpers, as needed to aid in diagnosing problems or setting up multiple conditions for syncing a scope. Two or more circuits may be wired together to form a latch, etc. for diagnostic purposes.

Example #1.

The CE desires to sync the oscilloscope on B phase of T2 time.

1. Place T2 time into one leg on a CE AND circuit by jumpering B-A1D4B2 to A-B1F2D12.
2. Condition the other leg on the AND circuit with phase B by jumpering B-A1C4J10 to A-B1F2D13.
3. The sync output is taken off at A-B1F2D10 as a minus pulse.



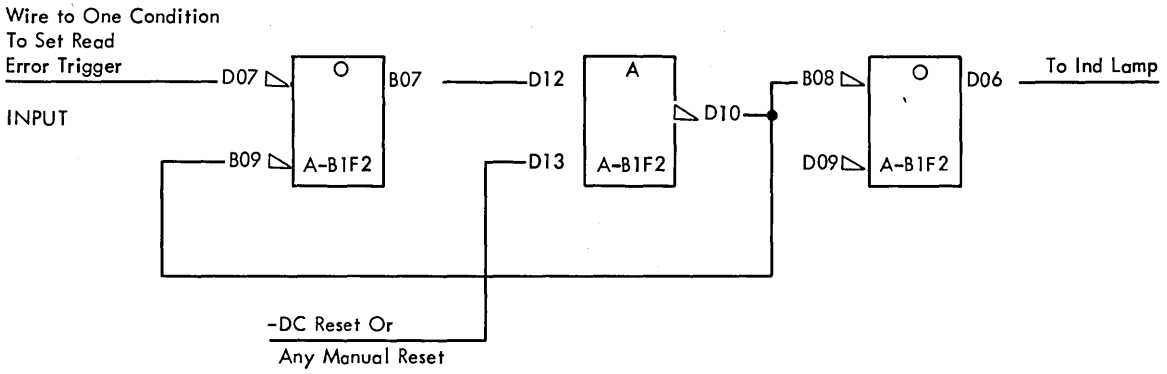
22615

Example #2.

In some cases of highly intermittent failures, it is desirable to have a circuit to monitor circuit conditions at the time of the failure.

On logic page XR291, there are several lines that give a read error. In the case of an intermittent failure, watching each line on an oscilloscope would be a tedious job.

The CE may wire a circuit monitor, as shown below, to do this watching for him.



22616

When the input to the latch goes negative, the latch turns on and the second OR block inverts the minus output from the AND block for a plus input to the CE indicator lamp. The latch remains on until the reset key is pressed. When the indicator comes on the line giving the read error has been found. The reset leg may be wired to a plus voltage level so that the latch cannot be turned off by the operator. In this manner, an error condition is indicated as long as power is not turned off.

2.3 CONSOLE PRINTER AND KEYBOARD

- The printer is mounted allowing 90° rotation for access to the base of the printer.
- CE can disconnect printer signal and power for problem isolation and replacement ease.
- Printer is capable of OLSA operation for installation test out and off line maintenance when feasible.
- Keyboard is mounted so tilting does not affect contacts or adjustments.
- The CE can disconnect keyboard signal cable for isolation.

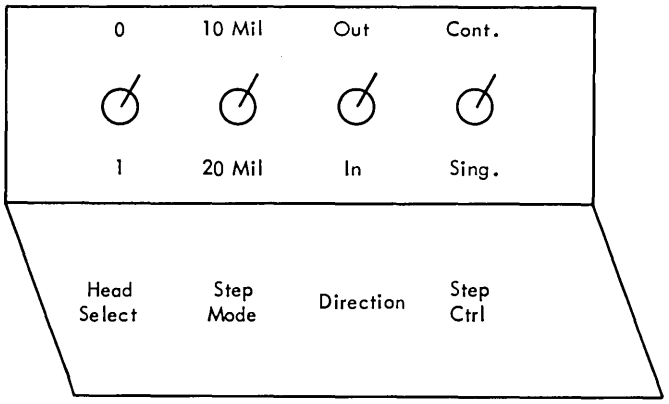
2.4 DISK STORAGE

- Can be taken off line by disconnecting the signal cable.
- CE switches function only off line.
- CPU can operate while unit is off line.
- Attachment provides for modulo 4 checking of write and read data.
- Access location must be verified by the program.

2.4.1 Manual Controls and Indicators

2.4.1.1 CE Switches

The CE switches located on the back of the drive are inoperative when the machine is on line. When the signal cable is disconnected, the drive is placed in read select mode of operation and the disk storage may be controlled by the switches.



Head Select. This toggle switch allows the CE to select either head as input to the read circuit.

Step Control. This switch is a momentary contact type when moved in the single direction. The carriage makes one step each time the switch is operated in the single direction.

The step control switch locks into continuous when operated and causes the carriage to step continuously at a 15 ms rate. This operation is particularly useful when performing adjustments on the two access control SLT cards.

Stepping Mode. This switch controls the number of tracks moved for each actuator step. When in the 10 mil position, each step of the carriage moves the heads one track position. When in the 20 mil position, each step moves the heads two track positions.

Direction. This toggle switch allows the CE to select the direction of carriage movement when stepping. Select forward when motion toward the spindle is desired, and reverse when the opposite direction is desired.

More details on the diagnostic procedures for the disk storage may be found in the FEMM IBM Single Disk Storage (Serial 00000-39999).

FEATURES

2.5 1442 READER PUNCH

- On line service only.
- Punch and Read error checking takes place in the attachment.
- The DSW provides error indication to the program and lights on the 1442 provide indication to the operator.
- Data read or punch errors drop ready on the 1442 but do not stop the system except by program control.
- Any error stops the 1442 operation and signals the program by the DSW.

2.5.1 CE Switch

The CE switch controls the ac power to the 1442 so that mechanical adjustment may be made while the system power is up.

2.5.2 Controls and Indicators

This section describes the switches, indicators, and their functions in the 1442 operations.

2.5.2.1 Start Key:

To run in:

1. Turn power switch on.
2. Check that the card path is empty.
3. Place cards in the hopper.
4. Press the start key to feed one card.
5. The ready light comes on.

To restore the machine to ready status after manual stop, press the start key.

2.5.2.2 Stop Key.

Removes the machine from ready status.

2.5.2.3 Non-Process Runout Key:

This key causes cards to be ejected from the card path without being processed. The key is ineffective unless the reader punch is removed from ready status and the hopper is empty.

2.5.2.4 Power On Light:

Indicates that the ac and dc power is applied to the reader punch control circuits.

2.5.2.5 Ready Light:

Indicates that the reader punch is prepared to accept instructions from the processing unit. The following conditions are required.

1. Power must be on.
2. Cards are registered at the read station.
3. Cards are in the hopper.
4. Stacker is not full.
5. Check light is off (no card jam or feed failure conditions).
6. Chip box is not full or removed.

2.5.2.6 Check Light:

Indicates that one of the following error conditions displayed on the backlighted panel has occurred. Any one of these removes the 1442 from the ready status.

1. Hopper - Indicates that a card failed to feed from the hopper.
2. Read Station - Indicates a read station jam or a defective photo transistor or lamp.
3. Punch Station - Indicates a jam at the punch station.
4. Transport - Indicates a jam in the stacker transport area.
5. Feed Clutch - Indicates that the clutch failed to latch up; thus, causing an extra feed cycle to be taken.
6. Read Registration - Indicates the first two readings of each card hole were not equal during the read cycle.
7. Punch - Indicates that the punch echo data did not equal the punch data.

The check light along with the corresponding error condition is turned off by the following action:

1. Remove jammed cards, if any, from the card path with the CE switch turned off.
2. Mispositioned card, or read, or punch error - run out cards with NPRO key.

2.5.2.7 Chip Box Light:

Indicates that the punch chip box is full or has been removed.

2.6 1132 PRINTER

- On line service only.
- Error checking is done in the attachment circuits.
- Error indication is provided to the program by the DSW, and the operator by lights on the 1132.

2.6.1 Manual Control and Indicators

- Provide manual operation of some printer functions which are independent of the program.
- Provide visual indication of some purely printer functions.

2.6.1.1 Controls

Power On Off - This switch controls power to the main printer drive motor and to the 48 volt magnet supply.

Start Key - Initiates the printer ready status.

Stop Key - Takes the printer out of ready status at the completion of the current program step.

Carriage Space Key - Pressing of the key single spaces the printer paper carriage.

Carriage Restore Key - Restores the paper carriage to the hole in channel #1.

Carriage Stop Key - Stops the carriage.

2.6.1.2 Indicators

Power On - The light on indicates that the motor is on and the 48 volts power is up.

Ready - Light comes on with power on, forms in place, and start key pressed.

Form Check - Indicates need for more paper forms on the printer.

Print Scan Check - Set when printer cycle steal cycles are taken before the program has completely set up the print scan field.

CE Switch. Controls ac power to the main printer drive motor and to the 48 volt magnet supply.

2.7 1627 PLOTTER

- Provides manual operation of plotter functions independently of programming.
- Mounted on front panel of the 1627.

2.7.1 Controls

Power On/Off: The power on/off switch connects 115 volts AC from the P5 connector on the rear of the recorder to the cooling fan and the power supply transformer. A neon indicator, located directly below the switch, is lighted whenever the switch is on.

Carriage Fast Run: The carriage fast run switch allows the pen carriage to be stepped rapidly to the left or right at the rate of 120 steps per second. The switch may be used to move the carriage to any desired area of the graph, or for operational checkout of the carriage control circuits and the carriage step motor.

Carriage Single Step: The carriage single step switch allows the pen carriage to be moved in single step (1/100") increments either to the left or right. This control, in combination with the drum single step control, permits the operator to accurately align the carriage on a point or fixed coordinate on the graph.

Chart Drive On/Off: The chart drive on/off switch allows the operator to disable the front and rear chart takeup motors. This permits the use of single sheets of graph paper in place of the paper rolls.

Pen Up/Down: The pen up/down switch provides a means of manually raising and lowering the pen from the surface of the drum.

When the recorder is first turned on, or if the pen is removed and replaced when the pen is in the up position, the pen can remain down. When this occurs, turn the switch first to the down position, then to the up position.

Drum Fast Run: The drum fast run switch allows the drum to be stepped rapidly up or down at the rate of 120 steps per second. The switch is used in the same manner as the carriage fast run control to move the pen to any desired area of the graph, or for operational checkout of the drum control circuits and the drum step motor.

Drum Single Step: The drum single step switch allows the drum to be moved in single step (1.100") increments either up or down. This control, in combination with the carriage single step control, permits the operator to accurately align the pen on a point or fixed coordinate on the graph.

Carriage Scale Factor Adjustment (Model 2 Only): A carriage travel scale factor adjustment is provided for the purpose of varying the carriage travel to compensate for stretch or shrinkage in the graph paper.

2.8 1134 PAPER TAPE READER

- Provides on line service only.

2.9 1055 PAPER TAPE PUNCH

- Provides manual punching of feed holes.

2.9.1 Controls

Feed Key: Pressing the feed key energizes the punch and the feed hole magnets.

Delete Key: Pressing the delete key energizes the punch clutch, the feed hole magnets, and all data punches except the channel 8 punch.

BASIC MACHINE

3.1 APPROACH TO SCHEDULED MAINTENANCE

The prime objective of any maintenance activity is to provide maximum availability to the customer. Every scheduled maintenance operation should assist in realizing this objective. Unless a scheduled maintenance operation cuts machine downtime, it is unnecessary.

NOTE: Do not adjust or disassemble a unit that is working properly, even if tolerances vary from specification.

3.1.1 Visual Inspection

Visual inspection is the first step in every scheduled maintenance operation. Always look for corrosion, dirt, wear, cracks, binds, burnt contacts, and loose connections and hardware. Alertness in noticing these items may save later machine downtime.

3.1.2 Electronic Circuits

Diagnostic programs are the basic tools used in scheduled maintenance of the 1130 system.

Do not adjust pulses unless the condition of the machine warrants it.

3.1.3 Mechanical Units

The three basic scheduled maintenance steps performed on every mechanical or electromechanical machine are clean, lubricate, and inspect. Remember not to do more than recommended scheduled maintenance on equipment that is operating satisfactorily.

3.1.4 Scheduled Maintenance Procedures

The Scheduled Maintenance Chart (Figure 3-1) lists details of scheduled maintenance operation. During normal scheduled maintenance, perform only those operations listed on the chart for that scheduled maintenance period. Observe all safety practices.

CODE		LOCATION OPERATION	FREQ.	OPERATION
U	R			
0		FILTERS & CONSOLE LIGHTS	1	Check for dirty filters. Replace as required. Check cooling fans for proper operation. Check console lights.
2		CONSOLE PRINTER		For detailed information refer to FEMM I/O Printer (Modified IBM Selectric ®) form #225-3207.
8		TESTS	4	Run diagnostic tests and meter verification test.
9		MISC.	6	Inspect for loose terminal board connections on SLT panels. Check ground connections. Check line cord for safe condition and proper grounding. Depending on keyboard useage check operation and lubrication of the keyboard.
7		POWER SUPPLIES	12	Check line voltage and power supply voltages at SLT large boards. Check cables and wiring for loose terminals and overheated insulation.

22142A

* Trademark, Kimberly Clark Corporation

Figure 3-1. Scheduled Maintenance Chart

3.1.5 Console Printer Preventive Maintenance

The Keyboardless I/O Printer FE Maintenance Manual covers preventive maintenance for the Console Printer.

3.1.6 Console Keyboard Preventive Maintenance

Figures 3-2 and 3-3 cover preventive maintenance for the Console keyboard.

3.1.7 Disk Storage Preventive Maintenance

The FE Maintenance Manual for the IBM Single Disk Storage (Serial 00001-39999) covers preventive maintenance for the disk storage drive.

Area	LUBRICATION CHART Item	IBM Lubricant 6	17	22
Keyboard	A sharp pointed instrument (large needle or scribe) is useful in lubricating with IBM 6. Avoid using excess oil.			
	Key stem at bellcrank and retaining wire	X		
	Key stem bellcrank pivots	X		
	Permutation bar pivot	X		
	Bail contact pivots	X		
	Permutation bar at bail stop plate	X		
	Restoring magnet armature pivot	X		
	Hook channel at points of contact with latch pull bar			X
	Restoring bail where it contacts latches			X

22618

Figure 3-2. Lubrication Chart-Keyboard

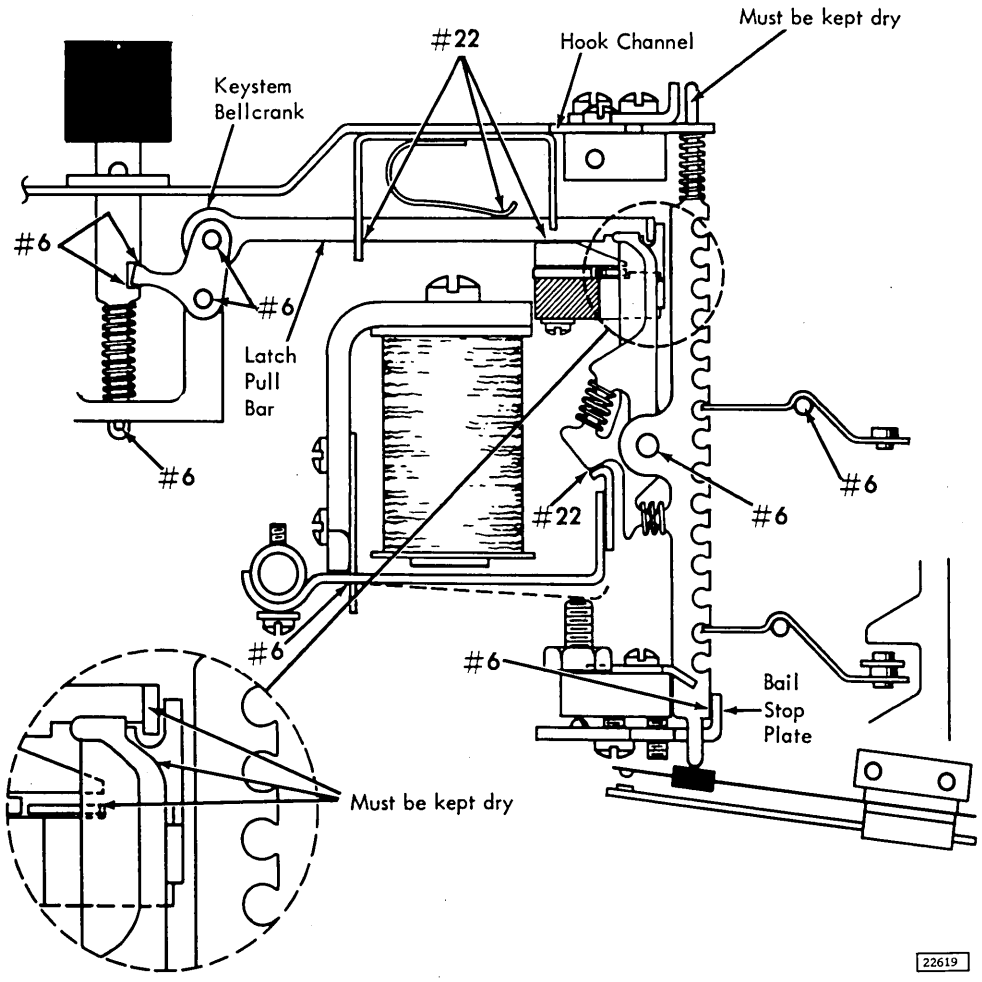


Figure 3-3. Keyboard Lubrication

3.2 PREVENTIVE MAINTENANCE OF I/O DEVICES

3.2.1 1132 Preventive Maintenance

The FE Maintenance Manual 1132 Printer contains detailed information.

3.2.2 1442 Preventive Maintenance

The FE Maintenance Manual for the 1442 covers preventive maintenance of the 1442.

3.2.3 1134 Preventive Maintenance

The FE Maintenance Manual for the 1134 covers preventive maintenance for the 1134.

3.2.4 1055 Preventive Maintenance

The FE Maintenance Manual for the 1054/1055 covers preventive maintenance of the 1055.

3.2.5 1627 Preventive Maintenance

The FE Instruction-Maintenance Manual for the 1627 covers preventive maintenance of the 1627.

BASIC MACHINE

4.1 SOLID LOGIC TECHNOLOGY MAINTENANCE

All normal maintenance procedures for solid logic technology components are found in IBM Field Engineering Manual of Instruction SLT Packaging. This manual includes information regarding:

Wrapped Wire Connections
Crimped Connections
Soldered Connections
Wiring Change Procedures
SLT Service Tools
SLT Card Maintenance
Measurements
Ventilating Systems
SLT Components and Packaging
SLT Service Techniques

4.1.1 SLT Cards

The lettering within a logical block on a systems diagram page gives the location of that block in the card gates. It also indicates other pertinent data as described in the SLT Packaging FEMI. Identification of pins, panels, rows, and columns, is shown in the SLT Packaging FEMI.

Logic block locations within the system diagrams are shown on system diagram card location charts.

The system diagram index gives the machine features indexing of ALD's and maintenance diagrams.

4.1.2 Single Shots

The single shots are adjusted with the CE alignment screwdriver, part 460811, or jewelers screwdriver, part 2108286.

Adjust each of the single shots so that the time from the input pulse to the output pulse is equal to the time specified in the system diagrams for the individual single shot.

4.2 CORE STORAGE UNIT

WARNING: Be extremely cautious when working around core storage. Do not disturb the core planes. Do not leave the core storage unit unattended when the covers are removed.

4.2.1 Removal

1. Remove all power to the system.
2. Remove cards around unit.
3. Unplug the connecting assemblies (on the wiring side of the large board), using pulling tool, part 2108860, by pulling straight out.
4. Unlock the four retainers that secure the array to the large board.

Note: Pull out straight to prevent damage to pins and land patterns on the core unit.

5. Remove core array from machine and place array in a safe and secure working area.

WARNING: Do not leave the unit unattended as the connections and pins can be damaged. Do not place unit with pins down as the outside pins may be bent as array is picked up.

4.2.2 Adjustment procedure for Core Storage

The storage unit contains three potentiometers which must be adjusted to optimize storage performance.

These potentiometers set the reference voltage level (array current magnitude), position the sense amplifier strobe, and set the sense amplifier sensitivity.

Load the core storage with the core adjustment diagnostic test, which contains a worse-case pattern program. After the pattern is loaded, the program stops. Using the maintenance switches, the system is set in automatic display mode and parity check. In this mode, the CPU cycles through the storage at the maximum speed (continuous read/write) and regenerates the data read out. If parity errors are detected, the processor stops and displays a parity check.

If the core adjustment test will not load, set all of core storage with an alternating bit pattern with the bit switches. After loading, make the core adjustments. After the adjustments are made, load the core adjustment test and remake the adjustments.

The parity is restored at the faulty location by:

1. Note the address in IAR
2. Set the bit switches to the IAR address minus 1.
3. Set the mode switch to load.
4. Press the load IAR switch.

5. Set the bit switches to a correct parity word.
6. Set the storage load switch on, and the display switch off. Set run and storage load switches off, and the display switch on.
7. Press the start switch.
8. Set the mode switch to run and the storage load switch off, display switch on.
9. Press the start switch. The processor should again cycle through storage without errors.

It should be noted that VSA-VE varies if the -3v supply is varied; but once adjusted, it remains at the optimum value of operation even if -3v is varied. It is suggested that the adjustment procedure described below should be used after every card replacement.

SLT voltages -3, +3, +6, and the special voltage, +12v, should be set to within 1% of their nominal values, with a Weston 901 meter or equivalent i.e., -3, ±0.03v, +3 ±0.03v, +6 ±0.06v, and +12 ±0.12v, respectively, measured at the core storage large board with the system operating.

4.2.2.1 Strobe Adjustment

Scope setup:

1. Channel A and B -1v/div.
2. Time per division 0.5 micro-seconds/div.
3. Alternate sweep.

Adjustment:

Measure time interval between positive shift of short time (SD111) on pin N2-B13 and positive shift of sample pulse (SD111) on pin N2-B05. These are to be measured at 1 volt above the reference line on the scope. Adjust to 400 nanoseconds, ±20 nanoseconds using potentiometer located on card N2 (reference diagram SD021).

4.2.2.2 V-Reference - VSA Adjustment

WARNING: Do not use a scope for this adjustment as the reference is to -3v not ground.

1. Set the reference voltage, V-Ref, (G2B02) referenced to -3V (G2B06) to the value given in the following table by adjusting the V-Ref potentiometer (upper) of the V Ref and sense control card (Reference diagram SD021). This is an initial adjustment. The final adjustment is defined in Item 4.

Room Temperature		V-REF
C	F	(Reference to -3V)
40-52°	104-124°	1.7V
30-40°	86-104°	1.8V
20-30°	68-86°	1.9V
10-20°	50-68°	2.0V
4-10°	39-50°	2.1V

2. Press the Stop Key. With the clock stopped, adjust -3v supply to give -2.70v measured between -3v emitter strobe (G2B12) and ground. Set the sense control voltage to 2.14v ± 0.02v (G2B07) referenced to offset voltage G2B09 (SD211) by adjusting the VSA potentiometer (lower) on the V-Ref and Sense Control card G2. Restore -3 volt supply to -3 ± 0.03v.
3. Decrease the sense control voltage (G2B07) (SD211) referenced to (G2B09) until failure occurs (parity error) by adjusting the VSA potentiometer (G2 lower) on the V Ref and sense control card. Then set the sense control voltage to 0.1 volt above the value recorded at the failure point.
4. After operations 1, 2, and 3 are completed, continue to cycle the storage and determine the reference voltage limits by varying the V-Ref potentiometer (G2 upper) on the V-Ref and sense control card (Reference diagram SD021). Adjust reference voltage, V-Ref (G2B02), referenced to -3V (G2B06) to the midpoint between the limits of operation.
5. If the V-Ref and sense control card is replaced, repeat section 4.2.2.2. If the clock-strobe card is replaced, repeat section 4.2.2.1.

4.3 OSCILLATOR

- The frequency of the 1131 oscillator is 2.25 megacycles ± 11.25 kilocycles and is not adjustable.

4.3.1 Oscillator Phase Adjustment

Objective: Set up initial adjustment when oscillator is replaced.

Adjustment:

1. Set the mode switch to run and the CE switch to storage display and press the start key.
2. Sync on + oscillator trigger, B-A1C4D13 (KA101).

3. Display + A Phase, B-A1C4J05 (KA111) and + B Phase B-A1C4J10 (KA101).
4. Adjust pot on card (B-A1E5)(KA101) for 450 nanosecond/cycle for both A and B phases.

4.4 CONSOLE KEYBOARD

4.4.1 Keyboard Removal

To remove the keyboard for servicing:

1. Unlock table top and tilt to the front (screwdriver in slot under left end of table top).
2. Remove four nuts on welded studs.
3. Raise and tilt back cover, switches and lights.
4. Remove four screws, and keyboard is free for service.
5. To remove keyboard from machine disconnect paddle connectors.
6. Assemble in reverse order.

4.4.2 Keyboard-Printer Single Shots

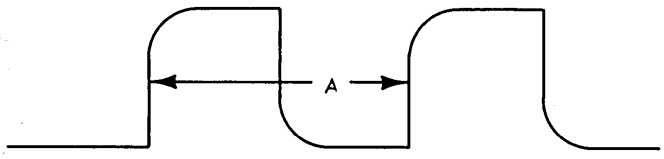
Objective: Set up initial adjustments of single shots when they are replaced.

Adjustment:

1. Load and execute a printer ribbon shift loop from the diagnostics.
2. Synch on + XIO Write, A-C1H7B04 (XW101).
3. Display the outputs of the printer single shots, A-C1F5B03 and A-C1F5B07 (XW101).
4. Adjust pots on cards for pulse width of 24 ms ± 3 ms.

Note: If keyboard single shots are to be adjusted, perform items 5, 6, and 7.

5. Interchange keyboard single shots, A-C1E3, (XK101) with printer single shots, A-C1F5 (XW101).



A=.45 μsec ± .045 μsec

22620

Figure 4-1. Oscillator Phase

6. Adjust as in item 4.
7. Replace cards.

4.4.3 Keyboard Assembly

4.4.3.1 Contacts

Keyboard contacts should be inspected for air gap, tension, and contact rise. Check contact surfaces for nodes and pits caused by burning. Insufficient air gap in latch contacts can cause false error indications. Note the condition of these contacts, particularly if the keyboard has been jarred or dropped.

4.4.3.2 Adjustment

Bail Contacts: With bail contact assemblies out of the machine, form each contact strap to require a pressure of 9 grams to 11 grams to close points (measure at contact point). Position the contact plates for contact air gap of .018 inch to .028 inch with all latch assemblies restored (Figure 4-2).

Latch Contacts: Form the operating strap to require 18-grams to 24-grams pressure to close contacts. Measure at contact pad. Pivot contact assembly mounting bar to obtain .018-inch to .028-inch contact air gap across the unit. Stationary contacts may be formed for individual air gap.

Restoring Bail Contacts: Form the operating strap to require 48-grams to 52-grams pressure to open the contacts. Position the contact bracket for .007 minimum to .015 maximum clearance between movable strap and operating insulator disk on restoring bail. It is very important to have clearance between the contact strap and the disk. After all restoring-magnet adjustments are made correctly, restoring-bail contacts should have a minimum of .010-inch air gap when restoring magnets are energized.

Note: It is important that restoring bail contacts open before the latch or bail contacts.

Key Stem Contacts: The N/O contacts should have a 1/32-inch minimum air gap. The N/C contacts must open with the minimum pressure of 15 grams at the end of the strap and with minimum movement (1/64 inch) of stationary strap when opening.

1. When the keyboard restore key is pressed 3/32 inch ± 1/64 inch, the upper contact must break. Further depression of 1/32 inch will cause the lower contact to make.

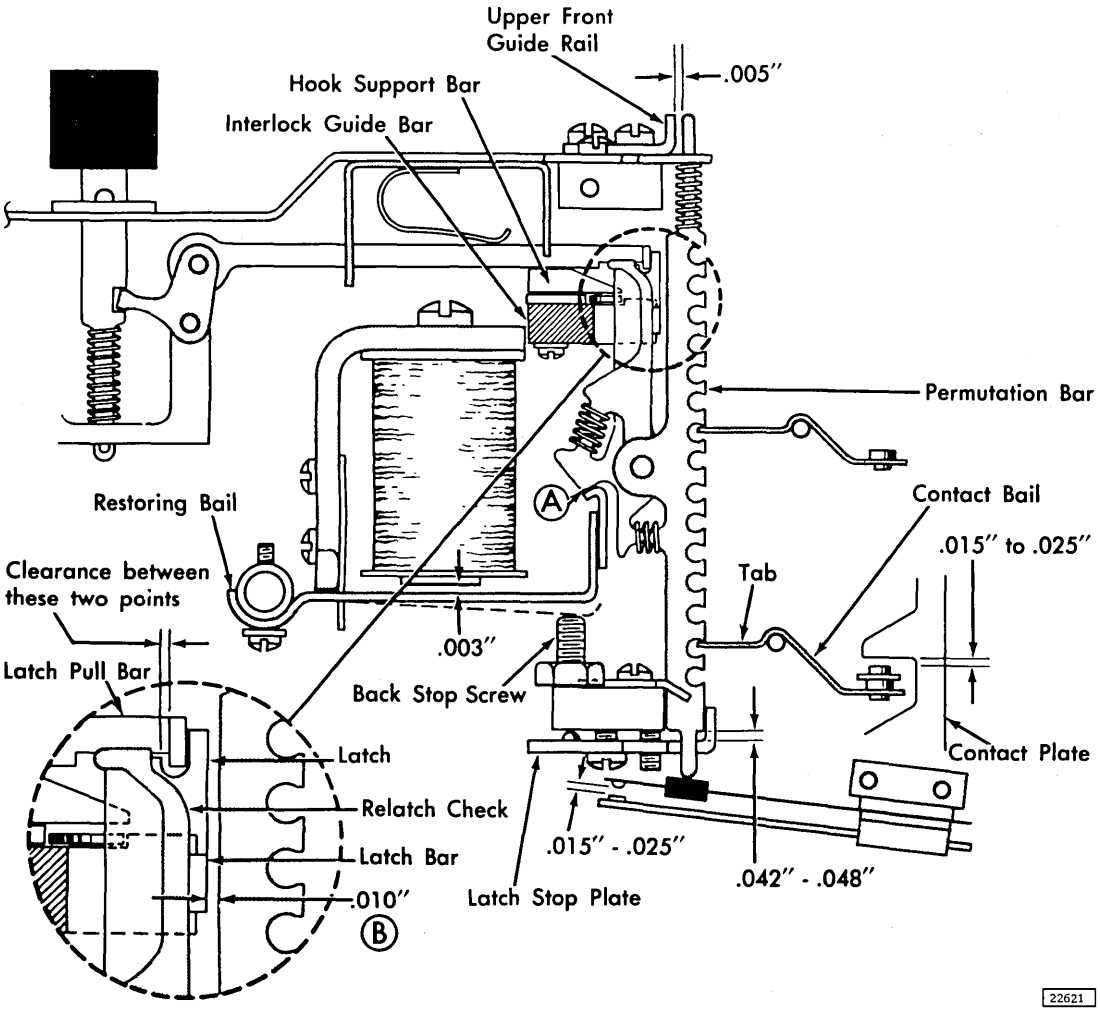


Figure 4-2. Keyboard Adjustment

2. ALPH key contact must close when the key is depressed 3/32 inch, ±1/32 inch. If the operator's palm strikes the ALPH key, increase the contact air gap.
3. The NUM contact must open when the key is depressed 3/32 inch, ±1/64 inch.

Contact Bails: When a new bail (Figure 4-3) is installed, form all tabs on each bail for zero to .005-inch clearance to associated operation ears on permutation bar, with latch assemblies in restored position. This may be checked on a keyboard with its covers removed. Check tension required to just open a closed bail contact for each key operating that bail. Tension should be at least 15 grams. Bail-contact air gap and tension on operated strap affects this tension and should be checked before a measurement is attempted.

Hook Support Bar: Bar must be within .008 inch of and parallel to the interlock guide bar, directly beneath it, along their longest edges. This is to prevent binding the latch.

Permutation Bar: Adjust the four setscrews positioning the latch stop plate to allow bars to drop .042 inch to .048 inch. Measure on a bar near each holding screw. To measure, lay a 6-inch rule across the top of the permutation bars. If the bar whose travel is to be measured is lower than the 6-inch rule, measure this amount and add it to the .042 inch to .048 inch given above. Trip the latch and measure the distance that the top of this bar is below the edge of the rule.

Restoring Magnet:

1. With all latch assemblies restored, insert .003-inch gage between armature and magnet core and

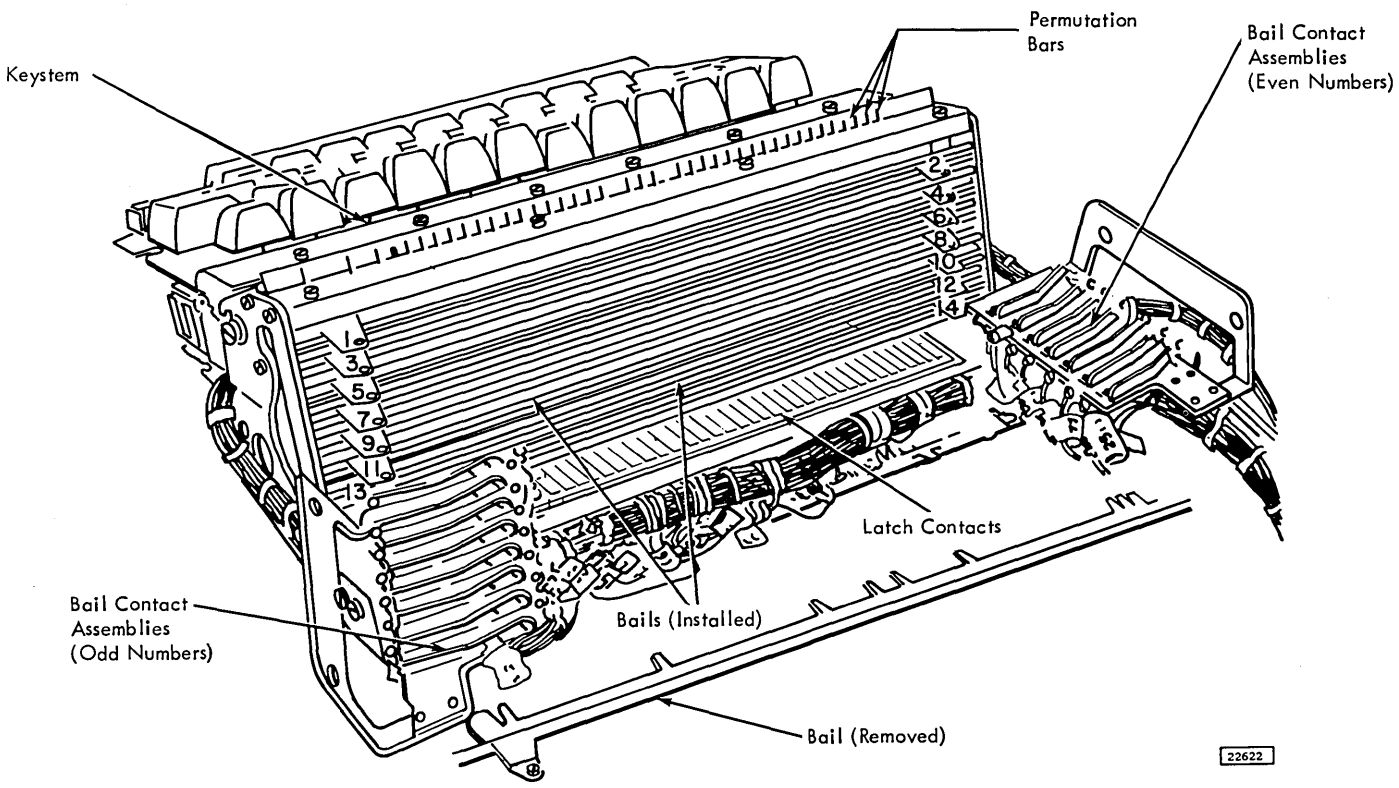


Figure 4-3. Keyboard Permutation Unit - 1

hold them sealed. Position magnet brackets evenly until restoring bail meets all latches at A, Figure 4-2. This should result in .010-inch maximum overtravel of latching point with gage removed.

2. With magnets de-energized, adjust the two backstop screws for clearance between each armature and its magnet core of .030-inch, measured at the centerline of core. (Use special .030-inch gage issued to measure clearance between feed and idler roll on this machine.)
3. Check adjustment of permutation bar travel and adjustments 1 and 2 by tripping, one at a time, several latches across the unit. Clearance between closest tripped latch and restoring bail should be at least .002 inch. Remake adjustments if this condition is not present.
4. Adjust restoring bail pivots so that the restoring bail operates freely but has a minimum of clearance in the pivots.

Upper Permutation Support: Note that die-cast supports are not adjustable.

1. Loosen the two end screws in the upper front guide rail and the four screws holding the switch mounting plate comb.
2. Position the comb for .010-inch (± .005-inch) clearance between latch bar and permutation bars (B, Figure 4-2).
3. Position upper front guide rail evenly for .005-inch clearance to permutation bars.

Key Unit:

1. Loosen the four screws that hold the key unit to the permutation unit.
2. With key plate level, and with no interlocks (Figure 4-4) affected, a 50- to 80-gram weight on any key top except erase field, NUM, ALPH, and the space bar, must be sufficient to trip its latch assembly. The key must return to its normal position with a 10-gram minimum weight resting on the key top, when its latch assembly has been previously restored.
3. With key plate level, and with no interlocks affected, a 75- to 100-gram maximum weight on the space bar must be sufficient to trip its latch assembly. The bar must return to its original position with a 10-gram weight resting on it when its latch assembly has been previously restored.
4. With key plate level, and with interlocks affected, 90-grams maximum weight on any key

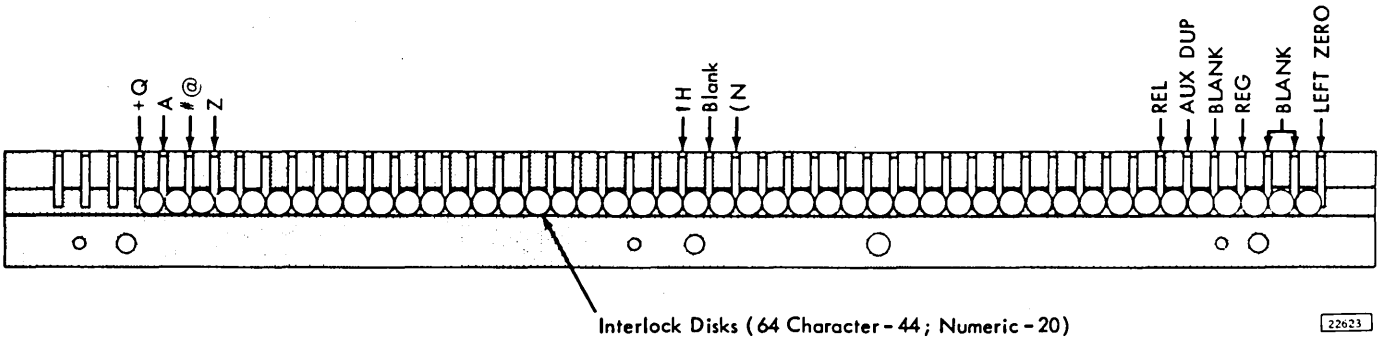


Figure 4-4. Keyboard Interlock Disk

top described in 2 above must be sufficient to trip its latch assembly.

5. NUM, and ALPH keys must travel .125 with 50- to 80-grams key pressure.
6. With any latch assembly dropped, no hook should slip off its latch when its key top is struck a quick sharp blow with the finger.

4.4.3.3 Removals

Key Unit: To separate the keyboard into its major units, remove the four screws as shown in Figure 4-6. Be careful when sliding the key unit out of permutation unit: the Y pull bar may hook on the center support screw. It is not necessary to remove any wires if the removal is merely for inspection. Untie the nylon key-stop wire at the end where it is fastened to the permutation unit.

Note: Do not oil or grease the hook ends of the latch pull bars. On reassembly, check clearance of latch to pull bar (Figure 4-2).

Key Stem:

1. Remove the nylon retaining wire to free the desired key stem. (Use a follow wire to aid reassembly.)
2. Lift the key from the unit while the end of the latch pull rod is held up and clear of latch. Be careful that the key stem spring does not drop into the unit. Refer to Figure 4-2.
3. Reassemble the unit. Hold the latch pull rod free of the latch and allow the key stem bell crank to rotate into the key stem. Be sure the spring is assembled on the key stem.
4. Test the position for binds.

Contact Bails:

1. Remove the two bail contact assemblies shown in Figure 4-3. Each assembly is held by two screws and may be shimmed away from the side frame. Note the position of these shims.

CAUTION: As each bail contact assembly is removed, cover pivot end of contact bails with cellulose acetate tape to keep bails from falling out.

2. Punch a hole in the tape and remove the desired contact bail.

Latch Assembly:

1. Separate the key and the permutation units (Figures 4-5 and 4-6.)
2. Remove wires from all stem contacts and the two restoring magnets (Figure 4-6).
3. Loosen the two mounting screws and remove the restoring bail contact assembly.
4. Remove restoring bail by taking out one screw from one of the pivots and turning pivot block away from the armature.
5. Remove the two bail contact assemblies shown in Figure 4-3.
6. Remove the toggle switches from the mounting plate.
7. Remove the contact bails; they are numbered 1 to 15, top to bottom (Figure 4-3).
8. Remove the latch contact mounting bar.
9. Remove the four screws from the latch-stop plate (Figure 4-5).

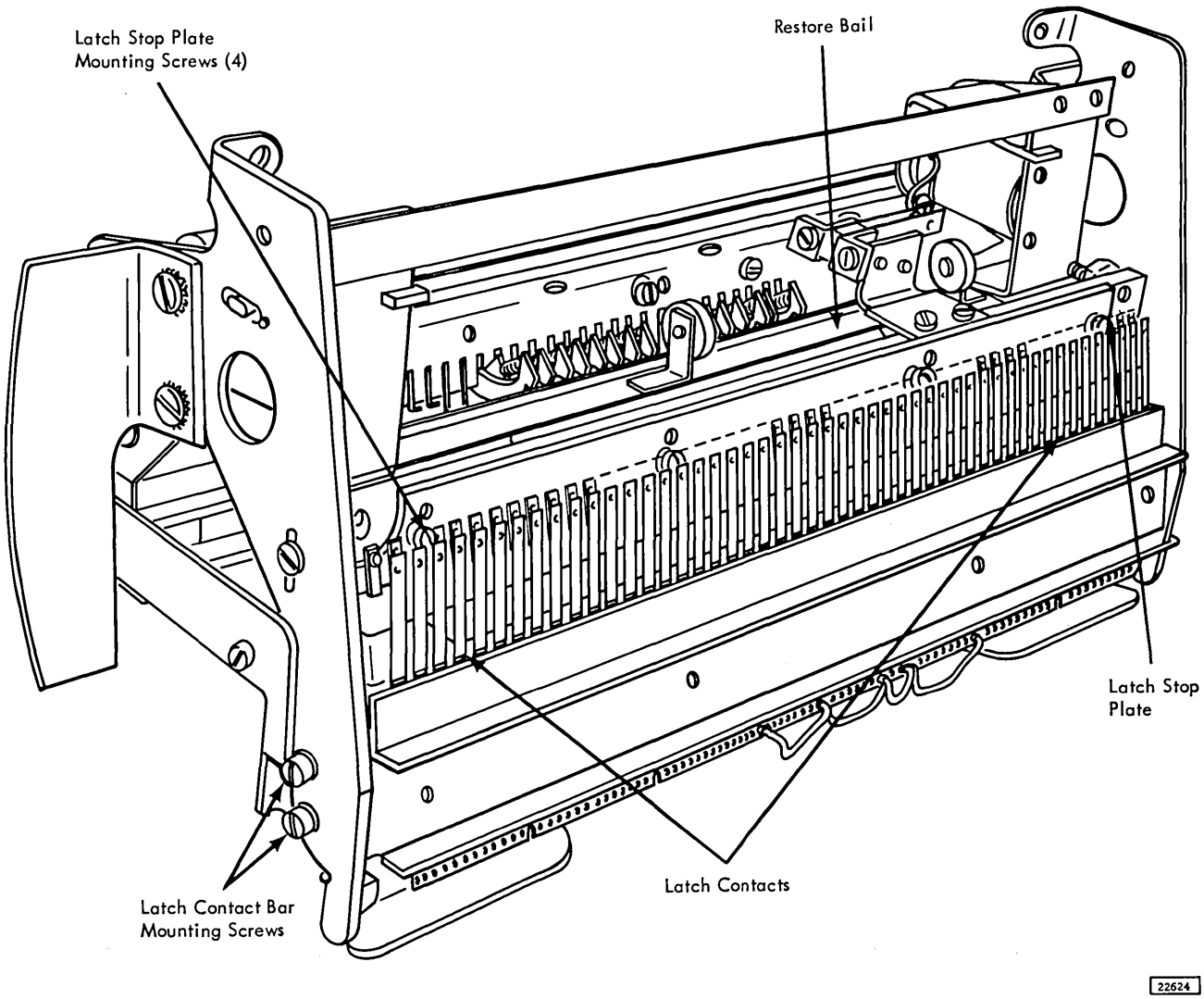


Figure 4-5. Keyboard Permutation Unit - 2

10. Remove the two springs on the latch assembly to be taken out. The longer spring belongs between the latch and the relatch check lever.
11. Remove the center support screw from the upper latch assembly guide (Figure 4-6).
12. Set the unit on its back. Hold the hook support bar (Figure 4-6) while removing the three screws that hold it. Also, remove the pivot screw.
13. Still holding the hook support bar, set the permutation unit right side up.
14. Slide the hook support bar off, exposing the interlock disks.
15. Lift out the interlock disks adjacent to the latch assembly to be removed. Latch is free to come out of bottom. Note carefully the difference between the release-key latch and other latch assemblies. The release-key latch is cut away at the point where the latch would contact the interlock disks. The release key is not interlocked. Figure 4-4 shows the correct position of the 44 interlock disks.

CAUTION: When an interlock is removed, all latches tripped off the latch bar can fly out. All parts in direct contact with interlocks, including latches that strike interlocks must be free of oil or grease.

After reassembly, check all adjustments. When replacing contact bails, stand permutation unit on one end after covering pivot holes with tape to keep contact bails from falling out.

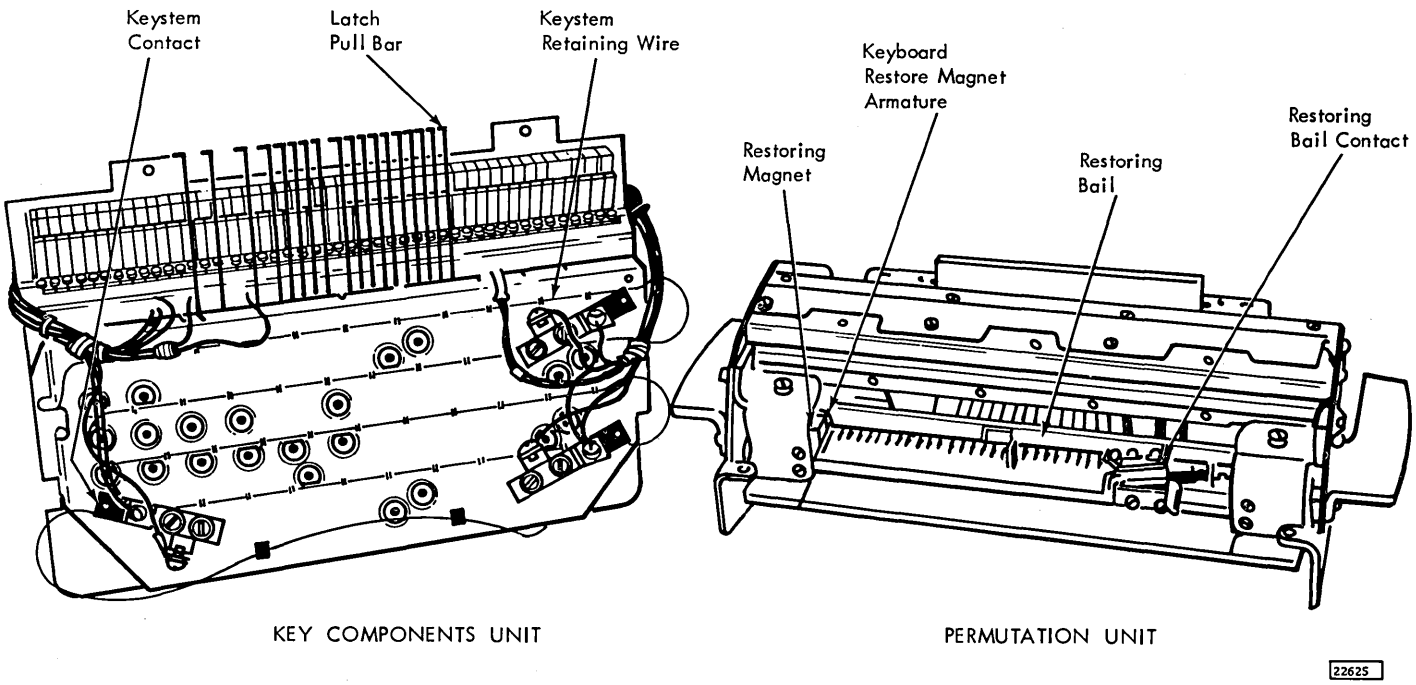


Figure 4-6. Keyboard Permutation Unit - 3

Latch Pull Bar:

1. Separate the key and permutation units; see Key Unit.
2. To replace a pull bar in the top row, remove the key stem in the defective position. If the defective latch pull bar is not in the top row, remove all key stems and the top plate.
3. Remove the defective latch pull bar from the pivot rod (a follow rod will aid in reassembly).
4. Replace the top plate and key stems. Check the clearance of the latch to the pull bar.

4.5 CONSOLE PRINTER

4.5.1 General Information

The console printer used with the 1130 system is an IBM SELECTRIC ® typewriter modified for data processing equipment. The Field Engineering Maintenance Manual, I/O Printer (Modified IBM SELECTRIC*), explains all adjustments, lubrication, and maintenance procedures.

The invalid typewriter character (▮) prints on any bit combination that does not select a valid character. It does not necessarily indicate incorrect parity.

The usage of the typewriter on the IBM 1130 is usually very high. Therefore, the typewriter must be kept well lubricated. Lubrication procedures are given in the I/O Printer Maintenance Manual.

4.5.2 Service Checks

To ensure reliable 1130 operation, all typewriter contacts must be carefully adjusted for proper contact air gap, adequate strap tension, and sufficient overtravel when made.

4.5.3 Removal

1. Unlock table top with screwdriver in slot under left front end of table top and tilt back. Remove side covers by removing nut on the front.
2. Slide console printer to the front.
3. Remove covers, if needed.
4. The console printer may now be tilted on its face or back for service, or removed by disconnecting the cables.
5. Assemble in reverse order.

4.6 I/O CABLES

Intermachine power and signal cables for the 1132 and 1442 are attached to the 1131 by means of multiple contact connectors.

Power and signal cables for the console printer and keyboard, 1134, 1055 and 1627 are attached by paddle connectors.

4.7 DISK STORAGE UNIT

- Maintenance procedures for the disk storage are described in the IBM Single Disk Storage (Serial 00001-39999) Field Engineering Maintenance Manual.

4.7.1 Removal

1. Remove the table top.
2. Remove the top, front, right end and right rear covers.
3. Remove the top cover from the unit.
4. Remove the cartridge.
5. Remove the air duct from rear of the unit.
6. Remove the cable from the switch panel by unplugging from the TB on top of unit.
7. Remove the dc cable from the TB on the rear of the unit and the ac cable from the sequence box under the right front of unit.
8. Remove four nuts from mounting studs on bottom of the unit.
9. Open the SLT gate.
10. Remove the connector holder.
11. Remove the signal connector from X-A1 A2.
12. Remove the signal connector holding clip as the cable leaves box.
13. Remove block from the cable.
14. Pull the cable from the box.
15. Now the unit is ready to be removed. This takes two men, one at the front and one at the rear of the unit. Reach down from the top and lift straight up.
16. Assemble in reverse order.

4.7.2 File Read-Write Single Shot

Objective: To delay the start of writing data so that a disk written on one system may be read on another system.

Adjustment:

1. Turn on the disk storage on/off switch.
2. Synch scope on + sector pulse, pin A-C1M6G10 (XF181).
3. Adjust the potentiometer on card, A-C1M6, so that the single shot output, A-C1M6J13, is negative for 250 ± 28 microsecond.

4.8 MISCELLANEOUS UNITS

4.8.1 Table Top

4.8.1.1 Removal

1. Unlock the table with a screwdriver in the slot under right end of table top and tilt to the front.
2. Remove the two screws on the stay brace.

Note: Do not remove holding screws on the adjustable bracket.

3. Tilt, to the front, the stop bracket on the right end of the table top.
4. Slide the table top to the right and remove.
5. Assemble in reverse order.

4.8.2 Gate Blowers

4.8.2.1 Removal

1. Drop the power with the CE switch.
2. Swing the gates out full.
3. Remove the mounting screws on the TB's.
4. Remove the two screws on each end of the housing.
5. Swing the housing out and place on its side.
6. Remove the wires to the fan from the TB.
7. Remove the holding screws.
8. Remove the fan.
9. Place the new fan in position.
10. Assemble in reverse order.

4.8.3 Filters

4.8.3.1 Cleaning

1. Remove the filter by sliding it forward.
2. Clean in clear water.
3. Shake dry.
4. Replace

4.8.4 Console Lamps

- Test with lamp test CE switch.

4.8.4.1 Lamp Removal

1. Drop power.

2. Remove the back cover of console.
3. Pull the bank of lights to the rear.

Note: Be careful not to damage the wires and connectors.

4. Remove the wire terminals from the individual lamp holder.
5. Remove the old lamp from the holder.
6. Replace the new lamp in place and clip the leads.
7. Replace the wries in the holder.
8. Be sure that the leads are not shorted or grounded.
9. Power on.
10. Test the lamps with the lamp test CE switch.
11. Power down.
12. Replace the bank of lamps in the panel.
13. Replace the back cover.
14. Power up.
15. Test the lamps with the lamp test CE switch.

4.8.4.2 Lamp Driver Removal

1. Turn off power.
2. Remove the back cover from the console.
3. Pull the bank of lamps to the rear.

Note: Be careful not to damage the wires and connectors.

4. Remove the lamp terminal from the driver.
5. Remove the signal connector from the driver.
6. Unsolder two leads to bus board and remove driver.
7. Form two outside leads on new driver down at 90°.
8. Place on bus board and solder in place.
9. Replace signal connector on driver.
10. Replace lamp terminal in driver.
11. Turn on power.
12. Test lamps with lamp test switch.
13. Turn off power.
14. Replace bank of lamps in console.
15. Replace rear cover.
16. Turn on power.
17. Test lamps with lamp test switch.

4.8.5 Status Indicator Panel

4.8.5.1 Lamp Removal

1. Pull up the lamp cover and remove.
2. Install the new lamp.
3. Replace cover.

FEATURES

4.9 1442 ATTACHMENT

4.9.1 Read Single Shot

Objective: Allow each column of the card to be read twice for read registration checking.

Adjustment:

1. Program load the read diagnostics in order to read cards while making the adjustment.
2. Display the output of the single shot, synch internal. A-B1K3B03 (XR301).
3. Adjust potentiometer (upper potentiometer) on the card, A-B1K3 for a 100 ±12 microsecond pulse on models 6 and 7.

4.9.2 Punch Gate Single Shot

Objective: Provide a delay gate to allow the 1442 to accept punch data.

Adjustment:

1. Program load the punch diagnostics in order to punch cards while making the adjustment.
2. Display the output of the single shot, synch internal, A-B1K3B07 (XR301).
3. Adjust lower potentiometer on the card, A-B1K3 for a 500 ±60 microsecond pulse on model 7 or 1000 ±120 microsecond pulse for model 6.

4.10 PAPER TAPE ATTACHMENT

4.10.1 Paper Tape Reader Single Shot

Objective: Set timing for transfer of information to the attachment.

Adjustment:

1. Load the paper tape reader program.
2. Synch oscilloscope minus internal on single output on board A-B1G6B07 (XT301).
3. Adjustable potentiometer is the lower of the 2 on the card (toward card row 7).
4. Adjust single shot output to 500 microseconds ±60 μs.

4.10.2 Paper Tape Punch

- There are no adjustments on the punch attachment.

4.10.3 1134 Attachment Oscillator

Symmetry: Adjust the plus oscillator FF signal (bottom potentiometer) on A-B1H7B09 (XT331) for 4.5 ±0.5 milliseconds duration.

Frequency: Adjust the plus oscillator FF signal (top potentiometer) on A-B1H7B09 (XT331) for 8.3 ±0.25 milliseconds between pulses.

4.11 1132 PRINTER ATTACHMENT

- There are no adjustments on the printer attachment.

4.12 1627 PLOTTER ATTACHMENT

- There are no adjustments on the plotter attachment.

Note: Attachment contains jumpers that are changed for Model I and Model II (XG101).

4.13 1132 PRINTER

The Field Engineering Maintenance Manual .132 Printer describes maintenance procedures for the IBM 1132 Printer.

4.14 1627 PLOTTER

The Field Engineering Maintenance Manual 1627 Plotter describes maintenance procedures for the IBM 1627 Plotter.

4.15 1134 PAPER TAPE READER

The Field Engineering Instruction Maintenance Manual 1134 Paper Tape Reader describes maintenance procedures for the IBM 1134 Paper Tape Reader.

4.16 1055 PAPER TAPE PUNCH

The Field Engineering Maintenance Manual 1054/1055 Paper Tape Reader/Punch describes maintenance procedures for the IBM 1055 Paper Tape Punch.

4.17 1442 SERIAL READER PUNCH

The Field Engineering Maintenance Manual 1442 Serial Reader Punch models 6 and 7 describes maintenance procedures for the IBM 1442 Serial Reader Punch.

BASIC MACHINE

5.1 GENERAL INFORMATION

CAUTION: Exercise extreme care when servicing or inspecting the power supply area. Dangerous voltages and currents are present even when the system is in a power-off status. If necessary to connect a test instrument within a power supply, or to reach into it for any reason, disconnect the main line cord. Discharge capacitors before working near them. Each heat sink is at an electrical potential. Do not short heat sinks to each other or to the machine frame.

5.1.1 Power Distribution and Sequencing

Power supplies are designed as high reliability units. Individual troubles in these areas, therefore, usually result in high service time for that system. To control these high service time calls, certain basic hardware checking is provided (Figure 5-1).

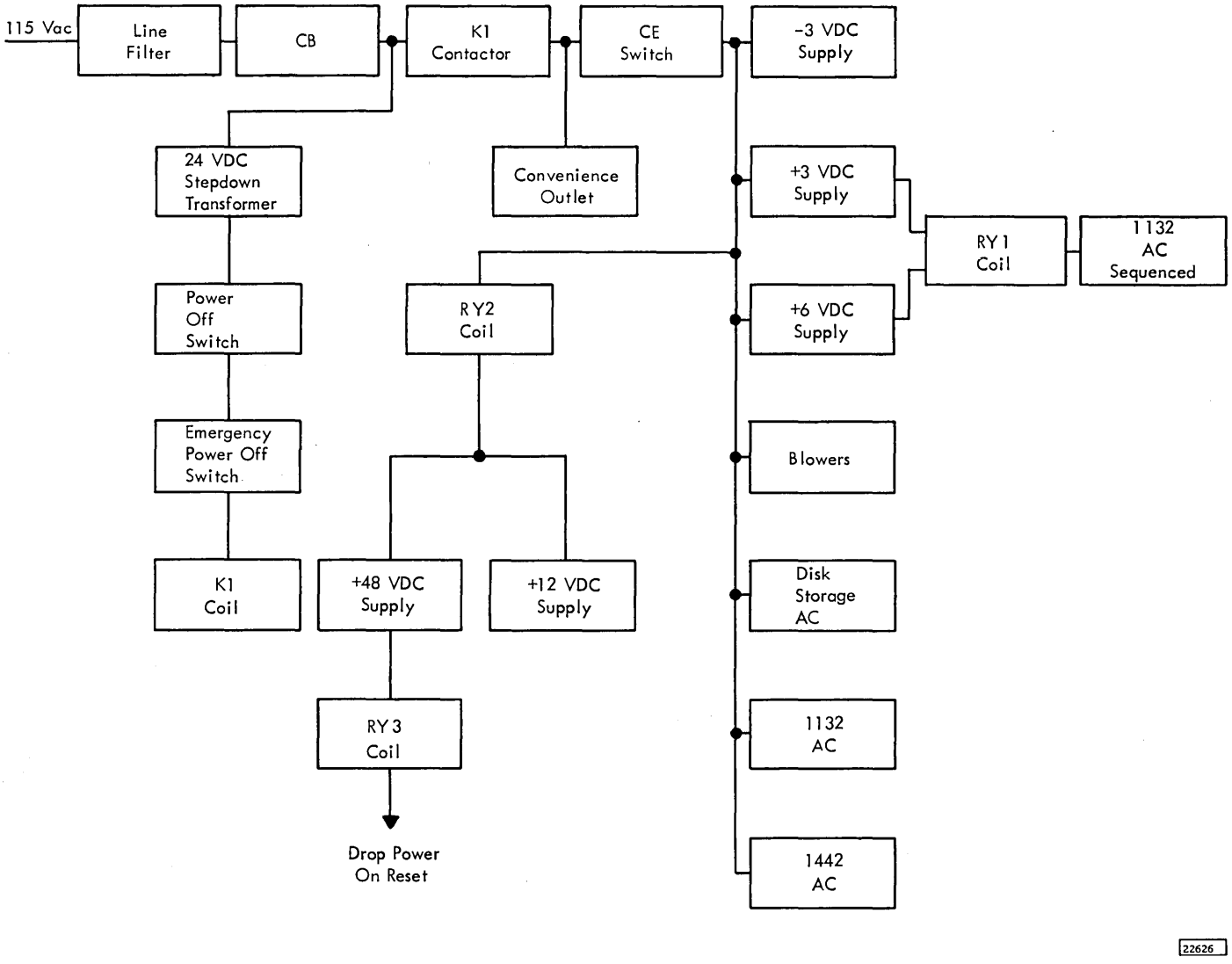


Figure 5-1. Voltage Distribution

5.1.2 Switches

Emergency Power Off: (not customer resettable). Turns off all primary transformer power in the processor, except the 24 vac power. Drops all power to I/O machines.

Power On/Off: Same as emergency power off except resettable.

Disk On/Off: Controls ac power to the disk storage drive.

5.1.3 CE Power Switches

Processor: Removes all primary power to system except processor convenience outlets.

Printer: Removes primary power in printer. Removes power to motors except chassis cooling fans. Leaves convenience outlets on.

Reader Punch: Same function as for printer.

5.1.4 Indicators

Ready: Indicates when power is up.

5.1.5 Voltage Variation

Those voltages which can provide an indication of a deteriorating component condition can be varied within ±4% to assist in isolating extreme difficulties. See table section 5.1.9.

5.1.6 Convenience Outlet

A 115v convenience outlet is provided in the CPU. It is fused at 6.25 amps.

5.1.7 Voltages Present Under Normal Power Off Conditions

1. 24 vac circuits.
2. 115 vac in sequence box.

5.1.8 Input Power Specifications

60 cycle: The IBM 1130 System operates from a 115v, 60 cycle, single phase, three wire service line.

Input voltage may have a total variation of ±10% of the rated voltage. Line frequency must be 60 ±0.5 CPS.

The mainline CB is designed to trip when the input current is excessive. It must be reset manually.

50 cycle: The 50 cycle version of the 1130 requires an input voltage of 195v ac, 220v ac, or 235 v ac, single phase, three wire service line.

Input voltage may have a total variation of ±10% of the rated voltage. Line frequency must be 50 ±0.5 cps.

5.1.9 Individual Power Supplies

Operating Limits: For normal operation, the dc power supplies must be maintained within the tolerances specified below. All voltages must be measured at the SLT large card pins.

Voltage	Allowable Range of Voltage
-3	- 2.88 to - 3.12
+3	+ 2.88 to + 3.12
+6	+ 5.76 to + 6.24
+12	+ 11.16 to + 12.84
+48	+ 44.16 to + 51.84

The dc voltage tolerances include regulation and ripple and are measured at the voltage bus on 01B-C1 board for +12v, +6v, +3v, and -3v. The +48v is measured at the TB2 block on the A gate.

5.1.10 Core Storage Voltages

Current Requirements:

	Storage in Use	Storage Stand By
+6v	4.0a	2.5a
+3v	.6a	.4a
-3v	1.5a	.5a
+12v	.5a	0.0a

Voltage Limit: In order to prevent damage to the storage circuits, the supply voltages should never exceed -8.0v, +8.0v, +9.0v and +15v for -3, +3, +6, and +12 voltages, respectively. Transient voltages greater than 10% above nominal must be less than 50 milliseconds duration. Under voltage does not damage the storage.

Marginal Checking: There is no provision for marginal checking of storage voltages.

Power Sequencing: The special voltage, +12v, is applied to the storage large card after the SLT

voltages have been established. It also is the first voltage to go down in case of failure of any SLT voltages (+6, +3, -3). The voltage +12 must be removed no more than 100 milliseconds after the failure.

Frequency Limits: The minimum period between the leading edges of a + read cycle and a + write cycle (and vice versa) is 1.75 microseconds. The minimum period for a full read/write cycle is 3.5 microseconds.

Adjustment: Adjustments for core storage voltage are covered in Section 4.2.

5.2 SERVICE CHECKS AND HINTS

1. All dc voltages should be within ±4%, including all noise and ac ripple, of their labeled values.
2. Loose wires at voltage distribution connectors can cause loss of or low voltage to the gates while the voltmeter indicates correctly.
3. A tripped power supply circuit breaker indicates a possible short in the output of the supply. Check the output for shorts to other supplies as well as to ground. These shorts are normally dead (near zero resistance) shorts. The minimum resistance to be expected can be determined by dividing the supply voltage by the maximum output current (E/I = R).
4. D.C. voltages should be measured at the SLT large boards.

5.3 CLEANING

The heat sinks must be clean to provide for heat dissipation and to prevent shorts.

5.4 ADJUSTMENTS AND REMOVAL PROCEDURE

5.4.1 Removal

1. Turn off the mainline switch. Remove the line cord. Bleed the capacitors.
2. Disconnect the leads to the particular supply to be removed.
3. Remove the holding clips on the power supply. Slide the supply forward and out of the machine (+3 must come out through the top).

5.4.2 Adjustment

For normal operation the DC power supplies must be adjusted within the tolerances specified in the following table. All voltages must be measured at the SLT large card pins.

Voltage	Allowable Range of Voltage
-3	- 2.88 to - 3.12
+3	+ 2.88 to + 3.12
+6	+ 5.76 to + 6.24
+12	+ 11.16 to + 12.84
+48	+ 44.16 to + 51.84

The dc voltage tolerances include regulation and ripple and are measured at the voltage bus on 01B-C1 board for +12v, +6v, +2v, and -3v. The +48v is measured at the TB2 block on the A gate.

5.5 DIAGNOSTICS

If one or more circuit breakers trip to the off position when power is applied, check their outputs for shorts to other voltage levels, as well as to ground.

NOTE: A good ohmmeter that can peg to zero resistance on the R x 1 scale must be used because of the very low total resistance of the circuits. Look for dead shorts. The minimum resistance to be expected can be found by dividing the supply voltage by the maximum output current. If trouble is in an individual power supply, some of the following points may be useful:

1. On the logic diagrams, those parts enclosed within dotted or broken lines are located on the circuit cards or in the overvoltage device.
2. Series power supply transistors are those other than the ones on the power supply circuit cards.
3. With the power supply removed, 110v ac can be wired into TB pins (check diagrams). Output may not reach full value, but should be close and adjustable (remove overvoltage device or overvoltage circuit card).
4. Visually inspect the unit for crimped wires or cable chafing (unit may work in opened position, but not in a closed position).
5. If the voltage is too high and cannot be varied by the adjusting control, check for shorted series power supply transistors (located on the large power supply heat sink), or for a bad power supply circuit card.
6. If the output voltage is high and CB did not trip, replace the overvoltage protective device or overvoltage card (if supply is so equipped).
7. An open diode in the rectifier circuit shows up as low voltage under load. This can be detected by feeling the diodes: they are quite warm when operating normally. If one is cold, it is probably open.
8. A shorted diode in the rectifier circuit should trip the circuit breaker in the primary of the

input transformer. It may also trip the overcurrent CB due to overvoltage spikes on the output. With the overvoltage device removed, the spikes can be scoped at the output terminals.

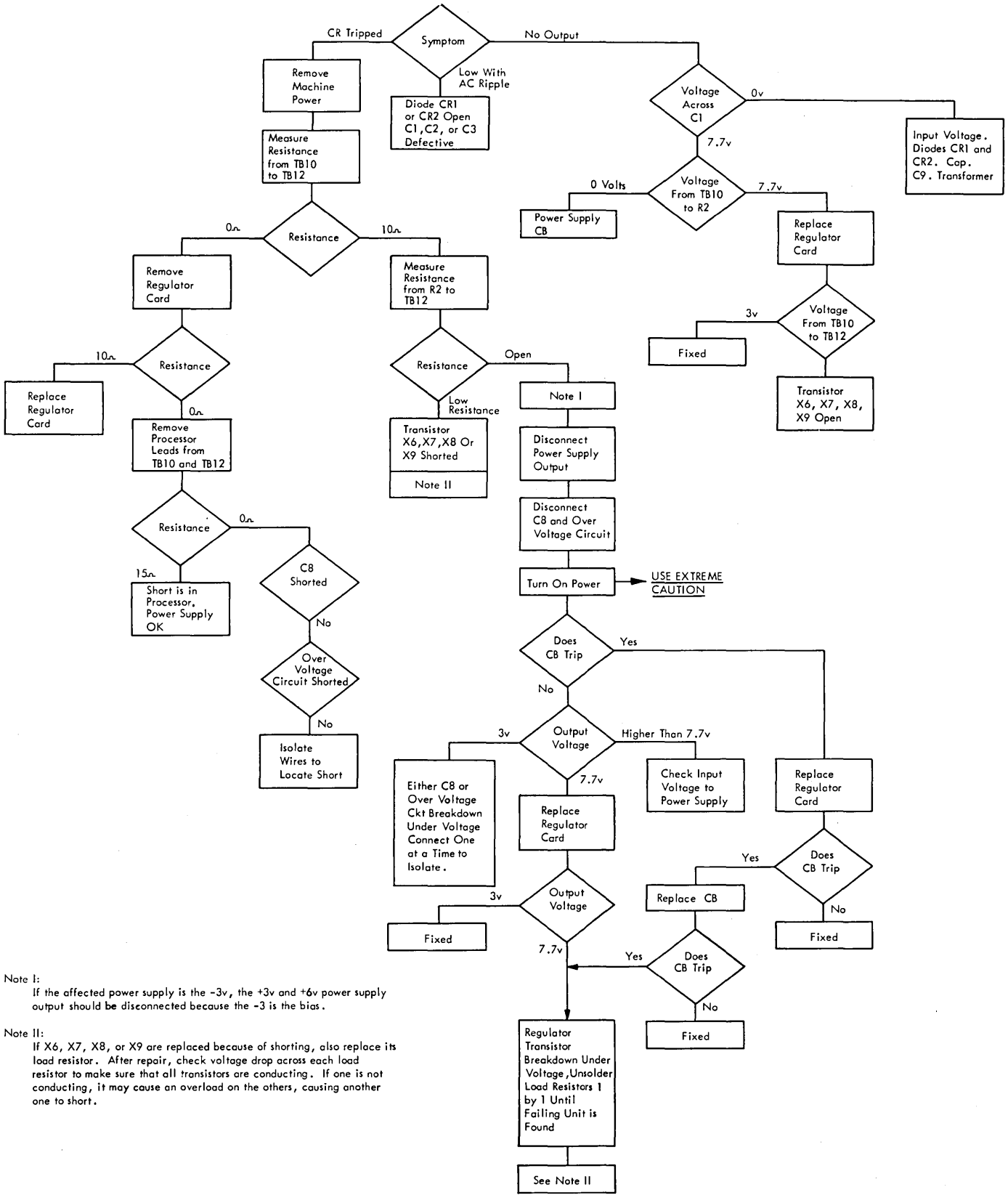
9. Shorted or open series power supply transistors can be detected by scoping or by checking the resistors in the emitter circuit for heat.
10. Check voltages after the machine has been on for 15 minutes. Voltage may drift slightly between cold and warm states.
11. Do not ground the meter or scope to the heat sink. Instead, ground to the holding screws at the corners of the unit.
12. If the system powers down immediately after a power up and the voltage of the various power supplies are correct, remove the overvoltage device from the power supplies one at a time and repeat the power up sequence. If power up is successful, the power supply voltage is wrong or the overvoltage device is faulty.

5.5.1 Power Supply Trouble Symptom Analysis Chart

Analysis techniques for the +3V, -3V, +6V supplies are the same even though some of the components are different. The 3v supply, logic YP003 was used for this chart (Figure 5-2).

NOTE I: If the affected power supply is the -3V, the +3V and +6V power supply output should be disconnected because the -3 is the bias.

NOTE II: If X6, X7, X8, or X9 is replaced because of shorting, replace its load resistor also. After repair, check voltage drop across each load resistor to make sure that all transistors are conducting. If one is not conducting, it may cause an overload on the others, causing another one to short.



Note I:
If the affected power supply is the -3v, the +3v and +6v power supply output should be disconnected because the -3 is the bias.

Note II:
If X6, X7, X8, or X9 are replaced because of shorting, also replace its load resistor. After repair, check voltage drop across each load resistor to make sure that all transistors are conducting. If one is not conducting, it may cause an overload on the others, causing another one to short.

Figure 5-2. Power Supply Flow Chart

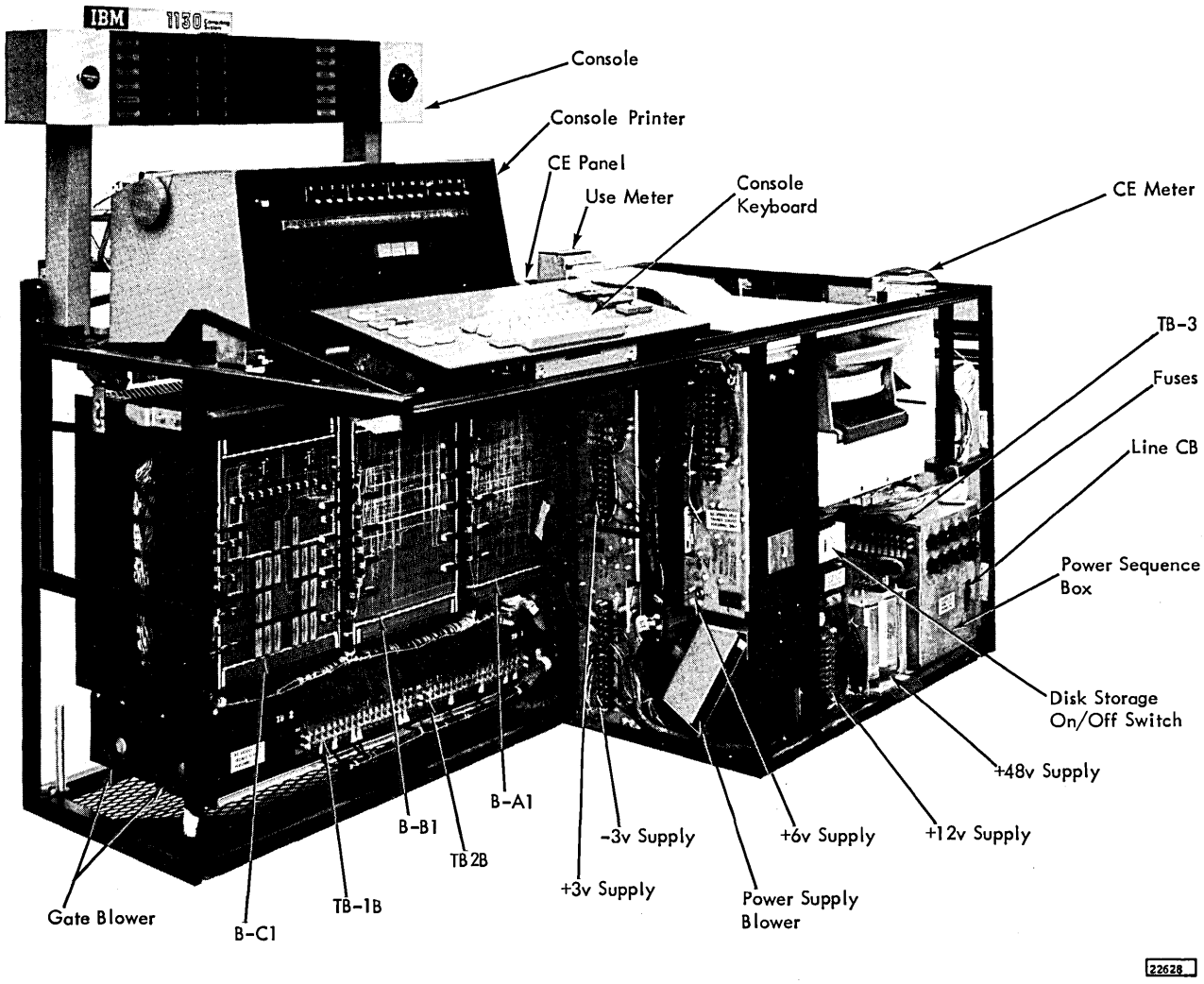


Figure 6-1. 1131 Central Processing Unit - Left Front View

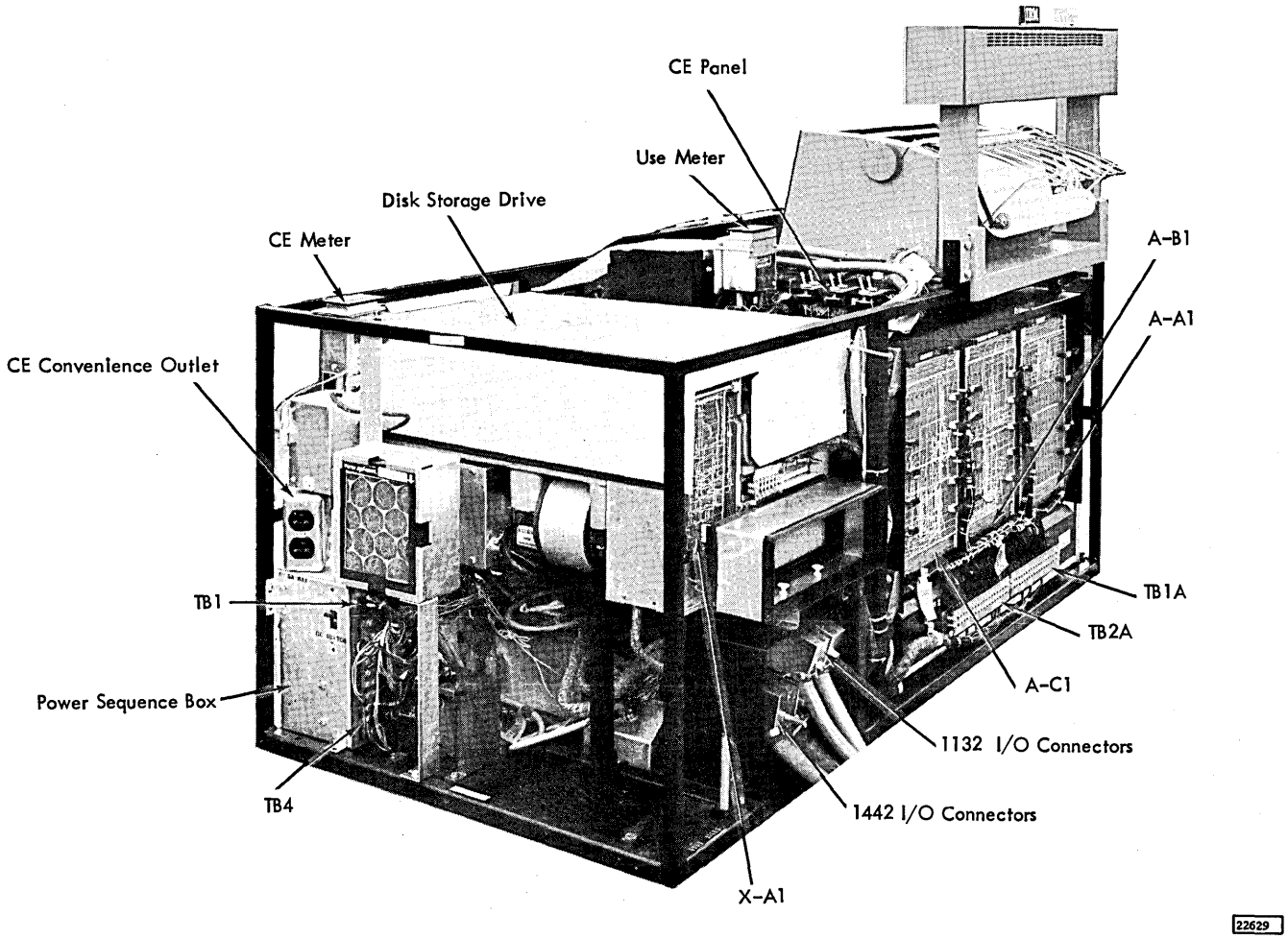


Figure 6-2. 1131 Central Processing Unit - Right Rear View

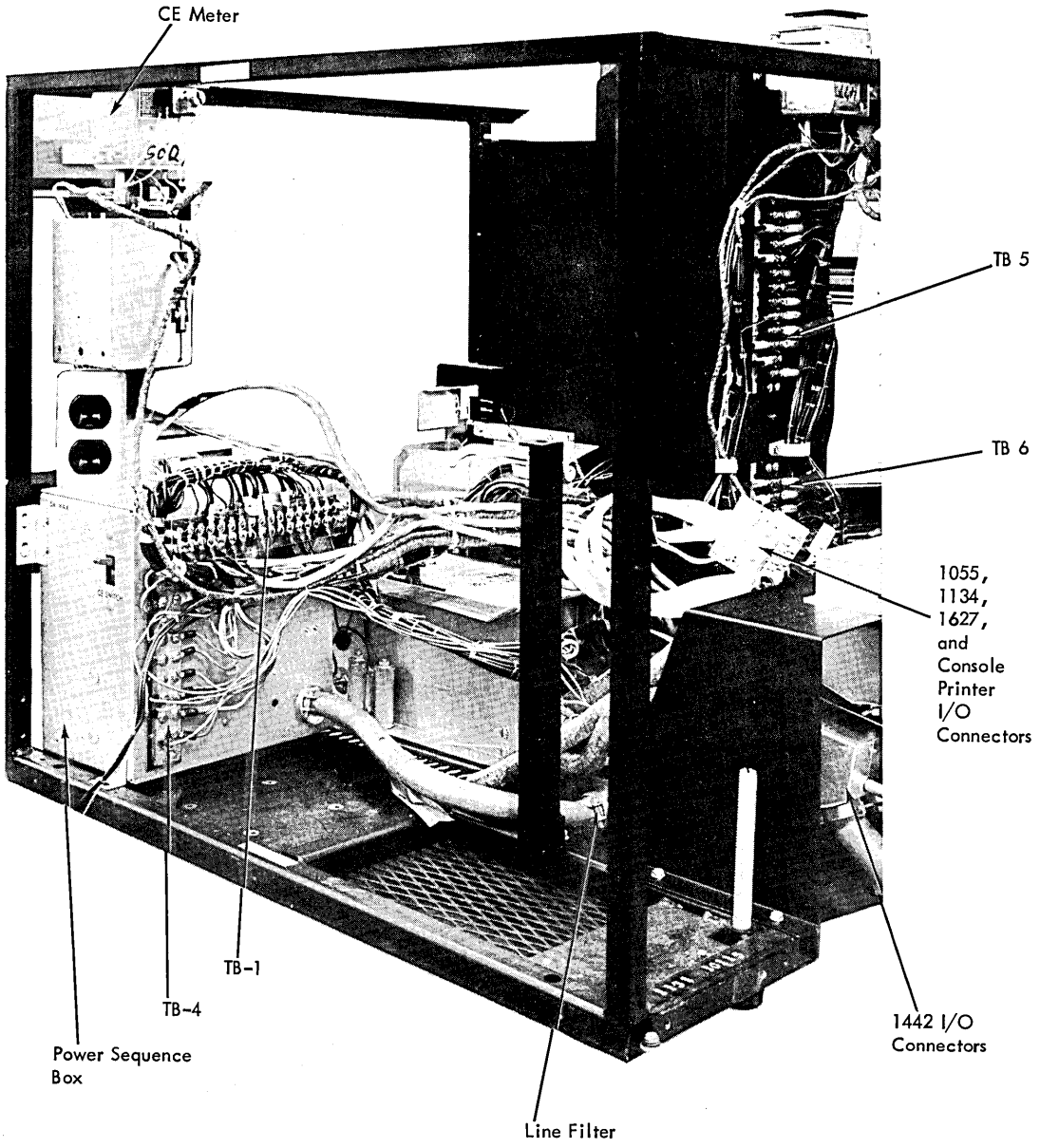


Figure 6-3. 1131 Central Processing Unit - I/O Connectors

22630

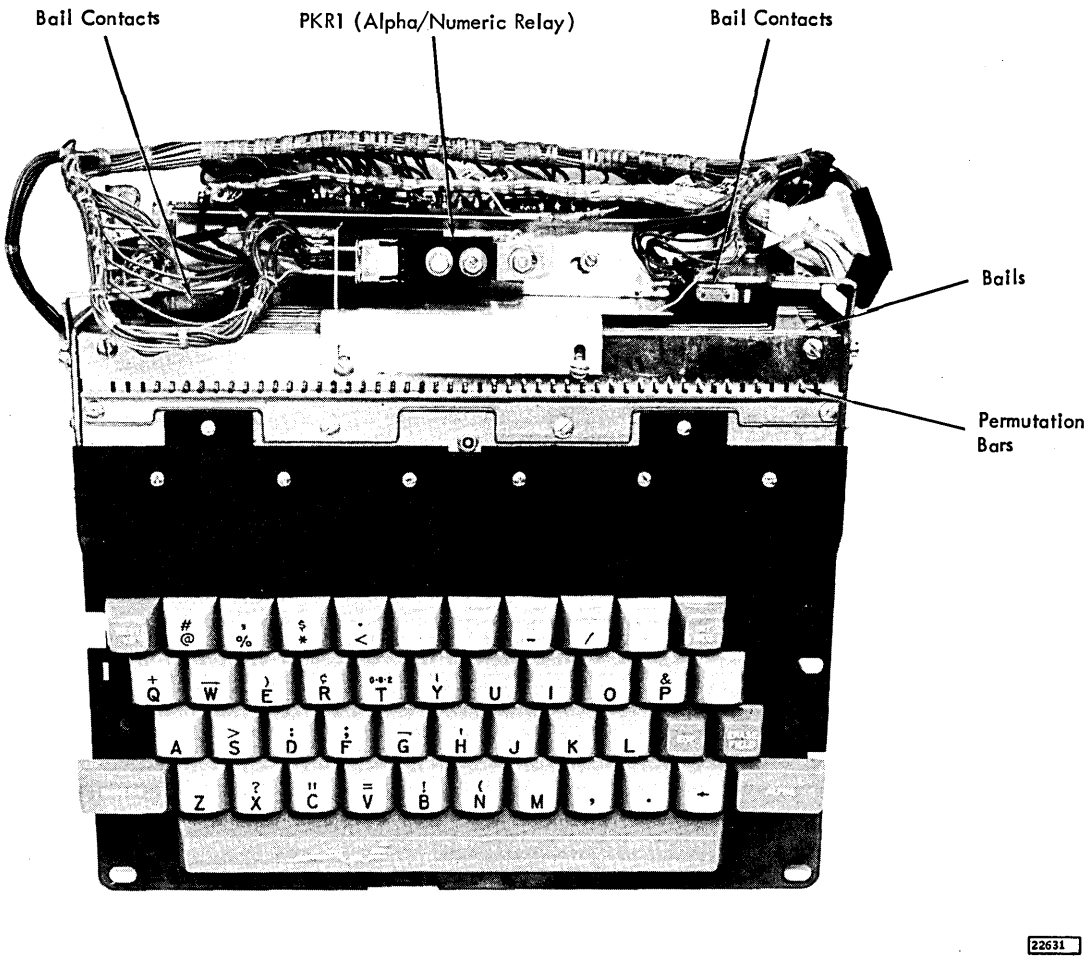


Figure 6-4. Keyboard - Top View

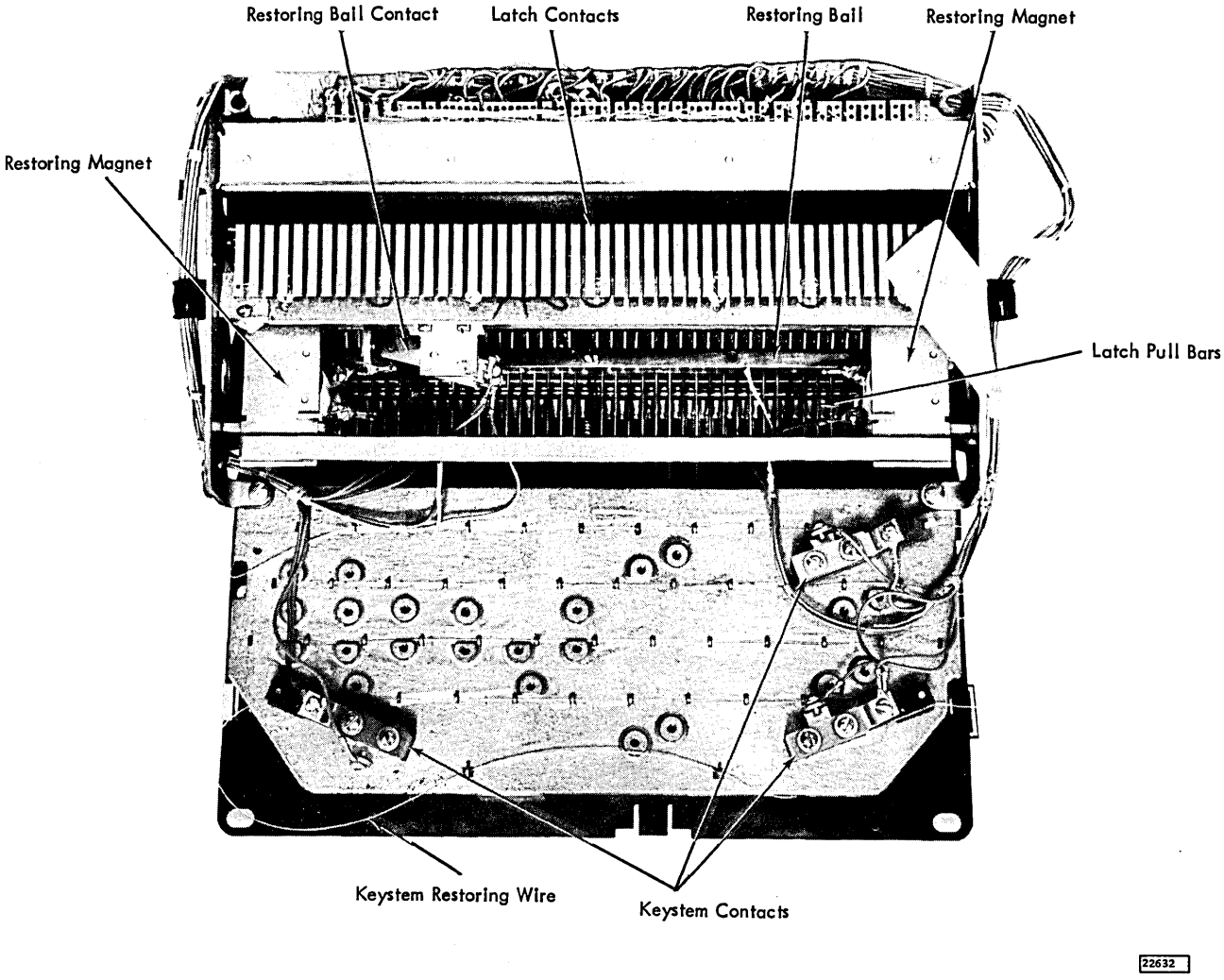


Figure 6-5. Keyboard - Bottom View

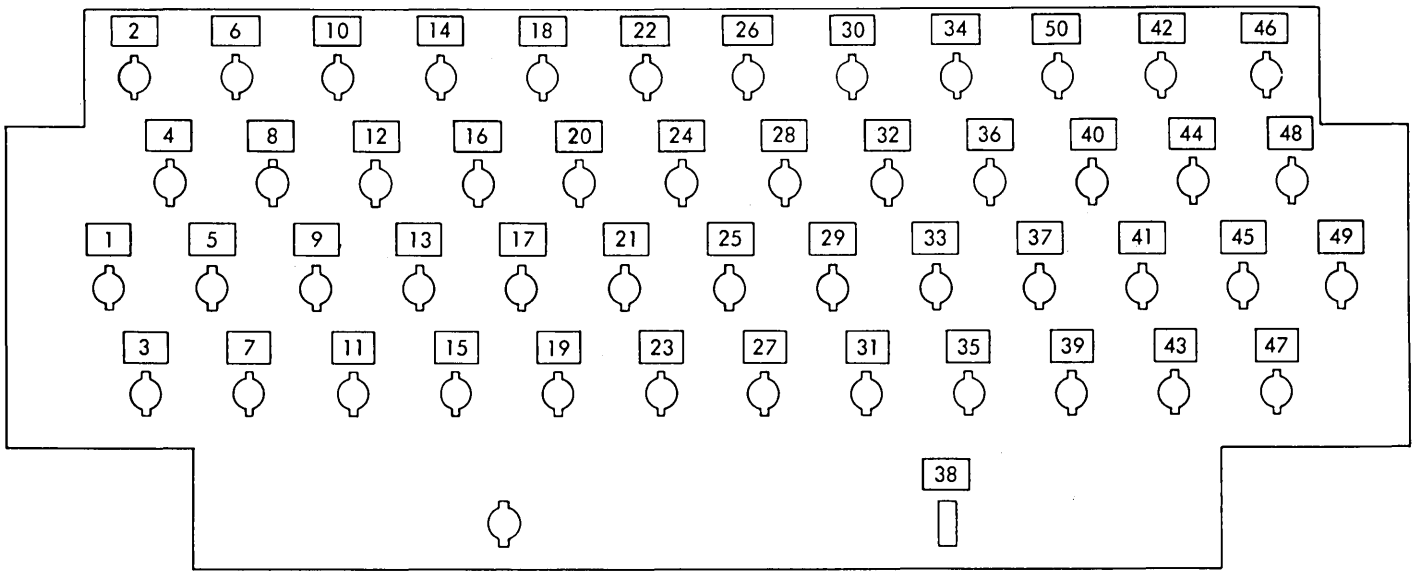


Figure 6-6. Keyboard Keystem Numbering

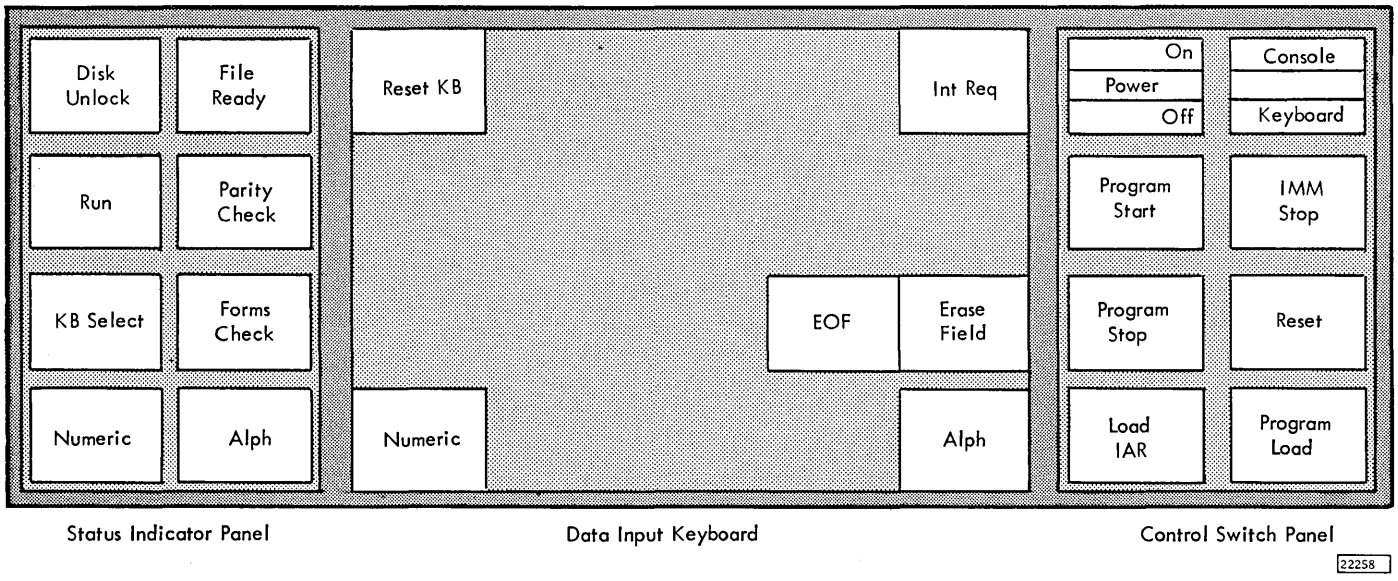


Figure 6-7. Console Keyboard

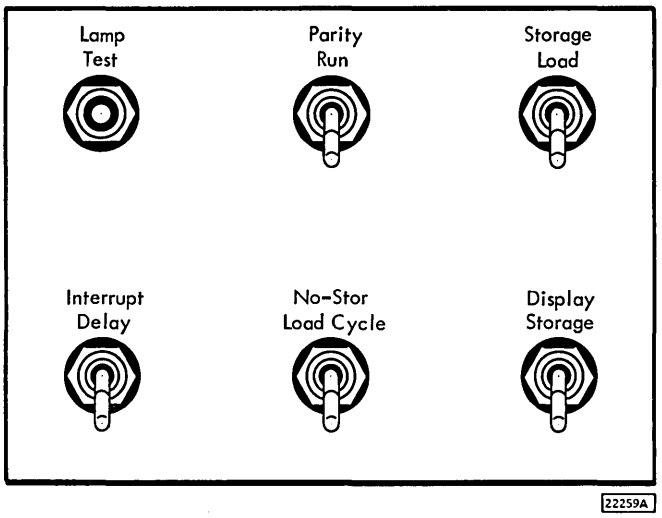


Figure 6-8. CE Panel

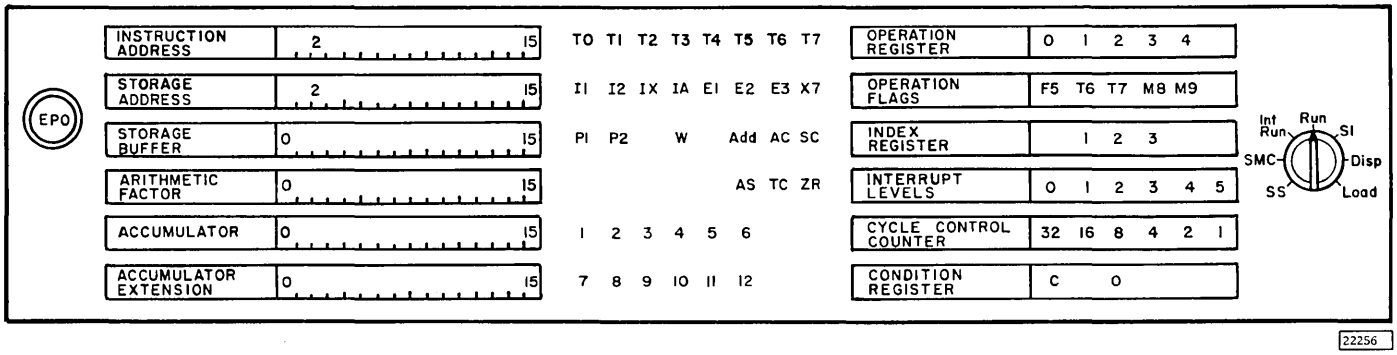


Figure 6-9. Console Display Panel

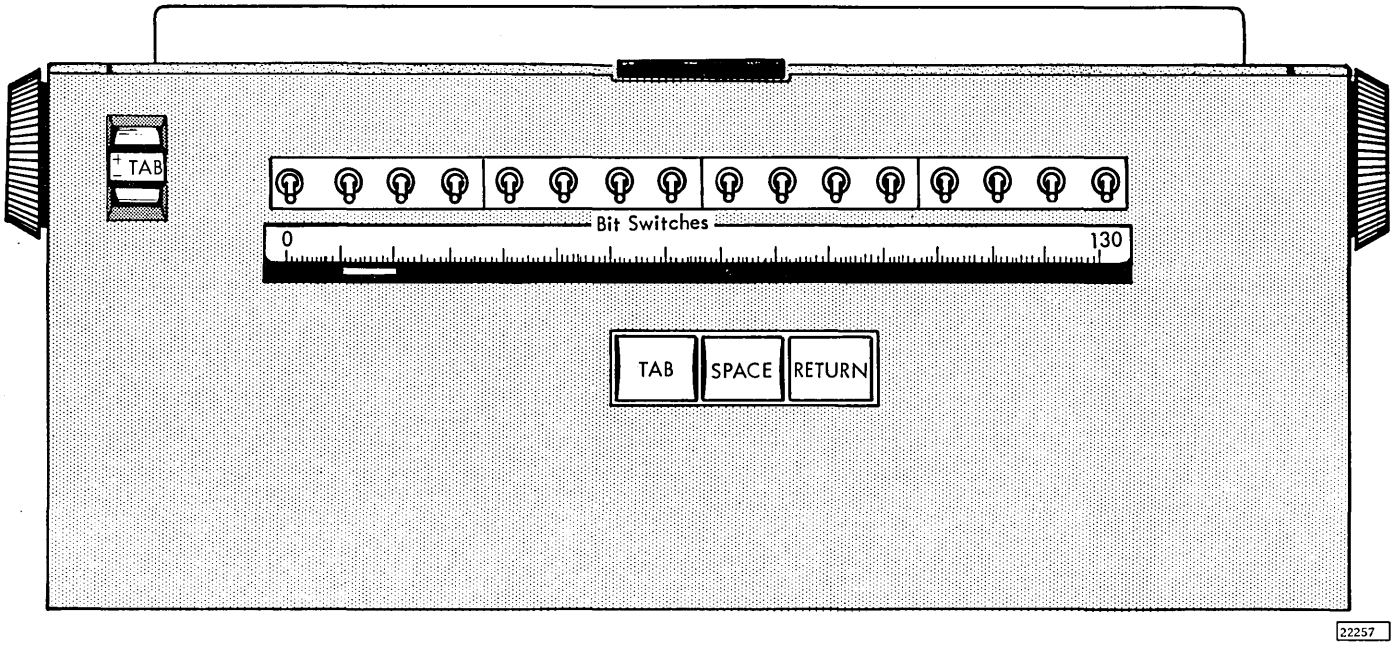


Figure 6-10. Console Printer

This is a list of manuals that contain information that is of value in servicing the IBM 1130 Computing System.

Manual Name	Type	Form Number
IBM 1130 Computing System Functional Characteristics	SRL	A26-5881
IBM 1130 Computing System	FETO	227-5978
Includes: IBM 1131 Central Processing Unit		
IBM Disk Storage Feature		
IBM 1130 Computing System - Features	FETO	227-3670
Include: IBM 1442 Card Read Punch Feature		
IBM 1132 Printer Feature		
IBM 1627 Plotter Feature		
IBM 1134/1055 Paper Tape Reader-Punch Feature		
IBM 1130 Computing System	FEMM	227-5977
IBM 1130 Computing System	PC	127-0808
I/O Printer (Modified IBM SELECTRIC®)	FEMI	225-6595
I/O Printer (Modified IBM SELECTRIC®)	FEMM	225-1726
IBM 1130 Reference Card		X26-3566
Solid Logic Technology Packaging	FEIM	
Solid Logic Technology Component Circuits	FEMI	
Tektronix Oscilloscopes	FEMI	223-6725
Transistor Component Circuits	FEMI	223-6889
Transistor Theory Illustrated	FEMI	223-6794
Transistor Theory and Application	FEMI	223-6783
SLT Power Supplies	FEMI	223-2799
IBM Serial Reader-Punch	FEMM	321-0026
IBM 1442 Card Read-Punch	PC	121-0518
IBM Serial Reader-Punch	FEMI	231-0025
IBM 1442 Models 6 and 7	FEMI	231-0091
IBM 1442 Models 5, 6, and 7	FEMM	231-0098
IBM Single Disk Storage (Serial numbers 00001 through 39999)	FEMM	227-3668
IBM Single Disk Storage (Serial numbers 00001 through 39999)	FETO	227-3669
IBM 1134 Paper Tape Reader	FEIM	227-3662
IBM 1134 Paper Tape Reader	PC	123-0452
IBM 1132 Printer	FEMM	227-3621
IBM 1132 Printer	PC	127-0806
IBM 1132 Printer	FEMI	227-3622
IBM 1627 Plotter	FEIM	227-5980
IBM 1627 Plotter	PC	127-0780
IBM 1055 Paper Tape Punch	FEMM	225-3178
IBM 1055 Paper Tape Punch	PC	124-0062
IBM 1055 Paper Tape Punch	FEMI	225-3082

FEMI = Field Engineering Manual of Instruction
FEMM = Field Engineering Maintenance Manual (Formerly Reference Manual)
FEIM = Field Engineering Instruction - Maintenance
FEISD = Field Engineering Instructional System Diagrams
PC = Parts Catalog
FEILD = Field Engineering Intermediate Level Diagrams
FES = Field Engineering Manual Supplement
FESI = Field Engineering Service Index
FEDM = Field Engineering Diagram Manual
FETO = Field Engineering Theory of Operation

INDEX

CUT ALONG LINE

READER'S COMMENT FORM

FROM:

NAME _____ DATE _____

OFFICE/DEPT. _____

CHECK ONE OR MORE OF THE COMMENT BLOCKS AND EXPLAIN IN THE SPACE PROVIDED.

☐ ADDITION: PAGE(S) FIGURE(S)

☐ DELETION: PAGE(S) FIGURE(S)

☐ ALTERATION: PAGE(S) FIGURE(S)

FOLD FOLD

EXPLANATION:

FOLD FOLD

NO POSTAGE NECESSARY
IF MAILED IN U.S.A.

FOLD ON TWO LINES,
STAPLE, AND MAIL

STAPLE

STAPLE

FOLD

FIRST CLASS
PERMIT NO. 2078
SAN JOSE, CALIF.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN U. S. A.

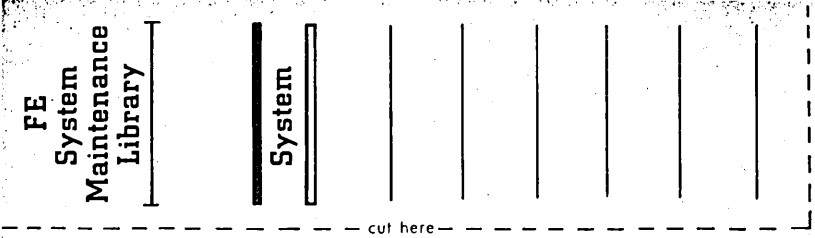
POSTAGE WILL BE PAID BY

IBM CORPORATION
MONTEREY & COTTLE RDS.
SAN JOSE, CALIFORNIA
95114

ATTN: PRODUCT PUBLICATIONS DEPT. 455

CUT ALONG LINE

FOLD



227-5977-1

IBM 1130 Printed in U. S. A. 227-5977-1

IBM
International Business Machines Corporation
Field Engineering Division
112 East Post Road, White Plains, N.Y. 10601