HP 13255

BACKPLANE MODULE

Manual Part No. 13255-9115R

REVISED

APR-26-78

HEWLETT PACKARD

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

This section contains design and application information for the Backplane Module and establishes the rules for interfacing between the various functional modules and the backplane (terminal data bus). The backplane is a printed-circuit board mounted to the bottom of the terminal base and contains a power supply connector and a number of printed circuit edge connectors. In addition to providing power to the functional modules, it supplies the 4.915 MHz System Clock (SYS CLK) and System Power On (PWR ON) signals. Data, address, and control signals for communication between the various functional modules is is also supplied by the Backplane Module. The bus is the primary data path between the processor and memory, display and memory, and the processor and peripherals (such as the keyboard, data comm, display, printer, and the CTU). All communication on the bus occurs in a serially shared mode, with each byte transfer being an independent non-interruptable transaction.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Backplane Module is contained in tables 1.0 through 3.2.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60153	Backplane PCA (9 Slot)	6.3 x 5.3 x 0.8	0.56
02640-60002	Backplane Extender PCA (6 Slot)	5.3 x 3.7 x 0.6	0.38
02640-60158	Backplane PCA (15 Slot)	9.8 x 5.3 x 0.8	0.81
02645-60005	Mainframe Assembly-2645	N/A	N/A

Number of Backplane Slots Required: NOT APPLICABLE

Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B ( ) Other:
Restrictions:	Type tested at product level
Failure Rate:	0.377 (percent per 1000 hours)

Table 3.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
J1 on 02640-60153 and 02640-60158		
Pins 1	+5V	TO POWER SUPPLY PCA
-2	+5V	
-3	GND	
-4	GND	
-5	+12V	
-6	SYS CLK	
-7	-12V	
-8	PWR ON	
-9		Not Used
-10	GND	

Table 3.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
J2 thru J10 on 02640-60153 J2 thru J16 on 02640-6015B		
Pins 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6

Table 3.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
J2 thru J10 on 02640-60153 J2 thru J16 on 02640-60158		
Pins 12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-20	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 3.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
J2 thru J10 on 02640-60153 J2 thru J16 on 02640-60158		
Pins A	GND	Ground Common Return (Power and Signal)
-B	$\overline{\text{POLL}}$	Negative True, Polled Interrupt Identification Request
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6

Table 3.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
J2 thru J10 on 02640-60153 J2 thru J16 on 02640-6015B		
Pins N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R	$\overline{\text{ATN2}}$	Negative True, CTU and Polled Interrupt Request
-S	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V	$\overline{\text{PROC ACTIVE}}$	Negative True, Processor Active (Controlling Bus)
-W	$\overline{\text{BUSY}}$	Negative True, Bus Currently Busy (Not Available)
-X	RUN	Allow Processor to Access Bus
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-7	$\overline{\text{ATN}}$	Negative True, Data Comm Interrupt Request

Table 3.2 Connector Information

Connector and Pin No.	Signal Name	Signal Description
J17 on 02640-60158		
Pins 1	+5V	———
2	GND	——— To Power Supply PCA
3	+12	———
P1 on 02640-60153		
Pins 1	+5V	+5 Volt Power Supply
-2	+5V	+5 Volt Power Supply
-3	GND	Ground Common Return (Power and Signal)
-4	SYS CLK	4.915 MHz System Clock
-5	-12V	-12 Volt Power Supply
-6	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-7	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-8	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-9	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-10	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-11	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5

Table 3.2 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1 on 02640-60153		
Pins 12	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-13	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-14	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-15	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-16	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-17	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-18	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-19	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-20	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-21	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-22	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-23	GND	Ground Common Return (Power and Signal)
-24	GND	Ground Common Return (Power and Signal)

Table 3.2 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1 on 02640-60153		
Pins A	+5V	+5 Volt Power Supply
-B	GND	Ground Common Return (Power and Signal)
-C	$\overline{\text{POLL}}$	Negative True, Polled Interrupt Identification Request
-D	+12V	+12 Volt Power Supply
-F	PWR ON	System Power On
-F	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-H	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-J	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-K	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-L	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-M	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5

Table 3.2 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1 on 02640-60153		
Pins N	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-P	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-R	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-S	$\overline{\text{ATN2}}$	Negative True, CTU and Polled Interrupt Request
-T	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
-U	PRIOR OUT	Bus Controller Priority Out
-V	+5V	+5 Volt Power Supply
-W	$\overline{\text{PROC ACTIVE}}$	Negative True, Processor Active (Controlling Bus)
-X	$\overline{\text{BUSY}}$	Negative True, Bus Currently Busy (Not Available)
-Y	RUN	Allow Processor to Access Bus
-Z	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-AA	$\overline{\text{ATN}}$	Negative True, Data Comm Interrupt Request
-BB	GND	Ground Common Return (Power and Signal)

3.0 FUNCTIONAL DESCRIPTION - SIGNALS. Refer to the schematic diagrams (figures 1, 2, and 3), typical memory module interface (figure 4), typical I/O module interface (figure 5), bus controller circuit (figure 6), bus controller states (figure 7), bus controller timing diagram (figure 8), and parts lists, (02640-60153, 02640-60002, 02640-60158, and 02645-60005) located in the appendix.

3.1 $\overline{\text{ADDR0}}$ through $\overline{\text{ADDR15}}$. These signals are defined as module address lines 0 through 15 and are used to define which module is being addressed, and which function (for an I/O module) or which byte (for a memory module) within the addressed module is being addressed. Bit assignments are as follows with $\overline{\text{ADDR0}}$ being the least significant bit.

MEMORY ADDRESS SIGNALS	$\overline{A15}$	$\overline{A14}$	$\overline{A13}$	$\overline{A12}$	$\overline{A11}$	$\overline{A10}$	$\overline{A9}$	$\overline{A8}$	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$
I/O MODULE ADDRESS SIGNALS	-	-	-	-	$\overline{M2}$	$\overline{M1}$	$\overline{M0}$	$\overline{X4}$	$\overline{X7}$	$\overline{X6}$	$\overline{X5}$	$\overline{M3}$	$\overline{X3}$	$\overline{X2}$	$\overline{X1}$	$\overline{X0}$

M's = I/O Module Select Code Bits
X's = I/O Module Subfunction Strobe Bits
A's = Memory Module Address Bits

3.2 $\overline{\text{BUS0}}$ through $\overline{\text{BUS7}}$. These signals are defined as data bus bits 0 through 7. $\overline{\text{BUS0}}$ is the least significant bit. All eight bits are transferred without modification over the bus. There is no parity check or other verification.

3.3 SYS CLK. This signal is the 4.915 MHz System Clock used to synchronize bus operations. All bus control signals must be changed only on negative transitions of this clock. This is a 50 per cent duty cycle TTL signal.

3.4 $\overline{\text{I/O}}$. This is the input output/memory signal and when low, indicates that address lines are to be interpreted as I/O module addresses and strobes. When high, it indicates that addresses are to be interpreted as memory references.

3.5 $\overline{\text{WRITE}}$. When low, this signal indicates that the current bus cycle is a write or output operation (data going out of the processor, to the modules). When high, it indicates that a read or input operation is in progress (data going into the processor from the modules).

3.6 PWR ON. System Power On will be low for the first 50 milliseconds after power is turned on; then it goes high and remains high as long as power is on. The PWR ON line should be used to initialize any circuits whose beginning states are important. It can be pulled manually low with power still on by pressing the RESET TERMINAL key on the keyboard. (RESET TERMINAL is a switch contact which pulls the line low for as long as the switch is depressed.) (Refer to module section 13255-91018 for the exact function of RESET TERMINAL key.)

3.7 RUN. This signal can be used to halt the processor. When pulled low, it prevents the processor from accessing the bus again, thus keeping the processor in a waiting state. When the RUN line is released, the processor will resume running again. This line is not normally used, and is provided primarily for use with diagnostic and debugging aids to implement run/halt and processor single-cycle operations.

3.8 $\overline{\text{PROC ACTIVE}}$. Processor Active indicates that the bus cycle currently in progress is being controlled by the processor. This line is not normally used, and is provided primarily for debugging and diagnostic purposes to implement processor single-cycle and processor instruction flow monitoring; and so that a sampler module can monitor bus operations and be able to distinguish processor transactions from display memory access (DMA) or other transactions.

3.9 PRIOR IN. When high, the Priority In line indicates to a bus controller that no higher priority device is contending for control of the bus. When PRIOR IN is low, it indicates that a higher priority controller is attempting to get the bus.

3.10 PRIOR OUT. The Priority Out line is used by a controller to signal other lower priority controllers that they must wait before attempting to take control of the bus. A low level indicates that the bus is not available. This signal is directly connected to PRIOR IN of the next lower priority module in a daisy-chain from module to module.

3.11 $\overline{\text{BUSY}}$. When low, $\overline{\text{BUSY}}$ indicates to all other controllers that the bus is currently being controlled and is not available. This is the method by which a low priority controller maintains control while a high pri-

ority controller is attempting to gain control. The priority chain is used to resolve which of the multiple controllers simultaneously contending for control will gain the control when the bus becomes not busy (bus is available).

3.12 $\overline{\text{REQ}}$. Request is the signal which indicates to the addressed module that the data on the bus is valid. Data being output by the processor is valid before $\overline{\text{REQ}}$ goes low, while it is low, and after it goes high. Therefore, $\overline{\text{REQ}}$ may be used to clock a flip-flop on either rising or falling edges, or to enable a latch. If data is being read into the processor, $\overline{\text{REQ}}$ is used to signal an addressed module to drive data onto the bus. When $\overline{\text{REQ}}$ again goes high, data should immediately be removed from the bus. The processsor will provide address and data setup and hold time for data being sent to a module, but will sample the data lines only at the trailing (rising) edge of $\overline{\text{REQ}}$ when reading data from a module.

3.13 $\overline{\text{WAIT}}$. $\overline{\text{WAIT}}$ may be pulled low by an addressed module to signal a controller that the module will be unable to respond to a 400 nanosecond $\overline{\text{REQ}}$. $\overline{\text{WAIT}}$ causes the controller to hold $\overline{\text{REQ}}$ low in increments of 200 nanoseconds until the addressed module releases $\overline{\text{WAIT}}$, then $\overline{\text{REQ}}$ will go high at the next SYS CLK falling edge. An addressed module should release $\overline{\text{WAIT}}$ as soon as valid data is put on the bus, but just after a falling SYS CLK edge, so that the data will have at least 200 nanoseconds to settle before being sampled (at the end of $\overline{\text{REQ}}$).

3.14 $\overline{\text{ATN}}$. Attention (interrupt request), is used by a module to request service from the processor. After the processor has read the status of the interrupting module, the module should release the $\overline{\text{ATN}}$ line.

3.15 $\overline{\text{ATN2}}$. $\overline{\text{ATN2}}$ is similar to $\overline{\text{ATN}}$, but causes the processor to trap to a different address. $\overline{\text{ATN2}}$ is the preferred line to request service for a polling interrupt operation.

3.16 POLL. The POLL line is used to signal pollable interrupting modules that an identification cycle is coming up. After acknowledging an $\overline{ATN2}$ interrupt request, the processor will pull $\overline{POLL}$ low to indicate that it wants to identify the source of the interrupt. Modules that have interrupts pending should monitor $\overline{POLL}$. When $\overline{POLL}$, $\overline{I/O}$, and $\overline{REQ}$ are low and $\overline{WRITE}$ is high, interrupting modules identify themselves by pulling a single bus data line low. The bit to be pulled must be decided by agreement between hardware and firmware, and should be jumperable on hardware boards.

4.0 DC RULES.

Bus signals are generally negative true logic levels. The exceptions are RUN, PWR ON, PRIOR IN, and PRIOR OUT. All bus lines with the exception of $\overline{POLL}$ and $\overline{ATN2}$ have 500-ohm pullup resistors installed on the Backplane PCA. All bus lines except PRIOR IN and PRIOR OUT are connected in parallel to all backplane edge connectors. PRIOR IN is pulled up with 500 ohms at the power supply end of the bus.

4.1 OFF THE BUS. No module may put more than two low-power Schottky input loads on any bus signal; modules needing more must buffer the signals. The only exception to this is PRIOR IN as it will be loaded, at most, by only one module.

4.2 ONTO THE BUS. A bus driver must be capable of driving 28 low-power Schottky loads (14 slots x 2 loads per slot) plus the 500-ohm pullup resistor (which amounts to 22 milliamperes at 0.4 volts). The recommended driver is a 74LS38, although Tri-State may be used.

5.0 TIMING RULES.

5.1 SYS CLK. The 4.915 MHz system clock synchronizes all bus transactions. Bus drivers will change control signals only on the falling edge of the clock. Responding devices are expected to reply immediately upon detecting their addresses, to allow sufficient time for the signals to settle before the next falling clock edge.

5.2 PRIORITY IN/PRIORITY OUT. The rules for SYS CLK in section 5.1 above, must also be applied to the priority chain. The priority signal may have to ripple through many modules to reach the last one which might be bidding for the bus at the same time as the first module. The first module must be able to disable the last one by propagating the priority signal down the entire chain within 200 nanoseconds (plus the setup time of the la. module). The results are not predictable if an attempt is made to t. e control of the bus at other than immediately (less than 50 nanoseconds) after a falling clock edge. Modules which are not controllers must tie PRIOR IN to PRIOR OUT in order to preserve the continuity of the chain.

5.3 $\overline{\text{WAIT}}$. This signal is used to prolong the bus $\overline{\text{REQ}}$ state. The release of $\overline{\text{WAIT}}$ tells the controller that the $\overline{\text{REQ}}$ state can be terminated at the next clock. In order for this to operate properly, data must be stable before the end of $\overline{\text{REQ}}$ (implying that data is driven onto the bus 200 nanoseconds before the end of $\overline{\text{REQ}}$). In addition, $\overline{\text{WAIT}}$ should only be allowed to go high at a clock edge, and data should be valid and starting to drive the bus at the same time. Thus, data need not be valid and settled, but it must be valid and starting to drive the bus when $\overline{\text{WAIT}}$ is released. This must occur immediately (less than 50 nanoseconds) after a clock edge in order to allow sufficient settling time for the data lines, which have more loading than the $\overline{\text{WAIT}}$ line.

5.4 $\overline{\text{ATN}}$/$\overline{\text{ATN2}}$. These lines are sampled asynchronously by the processor and have no particular setup requirements. However, for the sake of convention, it has been agreed that an interrupting module will release interrupt request as soon as the processor reads the status of the interrupting module and this must occur within 200 nanoseconds after the end of the status read.

5.5 $\overline{\text{POLL}}$. The $\overline{\text{POLL}}$ line is driven only by the processor and is programmed by the firmware. Typically, three instructions must be executed by the processor in order to perform the poll function. The first instruction causes $\overline{\text{POLL}}$ to be driven low, then an I/O read is performed to obtain

the results of the parallel poll, and finally, an instruction is executed to reset $\overline{POLL}$ high. Therefore, there will be a minimum of 1.6 microseconds setup and hold time before and after the input instruction which does the parallel poll.

5.6 $\overline{PROC\ ACTIVE}$. This line also is driven only by the processor and the timing is the same as the timing used to drive $\overline{ADDR}$, $\overline{WRITE}$, $\overline{I/O}$, and bus data lines (all these lines will have 200 nanoseconds setup before $\overline{REQ}$ and 200 nanoseconds of hold after $\overline{REQ}$).

5.7 RUN. RUN is sampled by the processor to determine whether to begin a bus bid state by its controller. If at the time the processor is ready to begin a bus cycle, the RUN line is low, it will cause a holdoff of the cycle until RUN goes high. When RUN goes high, the Bus Bid state will be entered at the next clock edge, and the bus cycle will then complete normally. Once begun, the cycle will complete. RUN prevents the processor from beginning backplane bus cycles, but cannot stop a cycle already in progress. It might be possible to use $\overline{WAIT}$ to hold a cycle in progress; but if it is a cycle accessing dynamic RAMs, it could cause a refresh failure if the cycle is not allowed to complete at its natural speed.

5.8 $\overline{BUSY}$. $\overline{BUSY}$ must be pulled low by a controller as soon as the Bus Bid state has been successful. This prevents other controllers from taking control while the bus is in use. $\overline{BUSY}$ should be released at the end of $\overline{REQ}$, so that other controllers can use the 200 nanosecond period after $\overline{REQ}$ to perform their bus bids. In this way, all clock periods can be utilized for data transfer and no time is lost performing purely control functions on the bus.

6.0 RULES FOR SLAVE MODULES.

6.1 MEMORY MODULES. Refer to figure 4, Typical Memory Module Interface (8K ROM). A memory module will usually contain a sizable contiguous block of memory address space. The module will usually try to have its block

starting address lie on an address which is an integral multiple of the block size. For example, a board with 8K bytes of storage could begin at 0, at 8K, at 16K, at 24K, etc. This results in a board select detector consisting of a 3-bit comparator between $\overline{\text{ADDR15}}$, $\overline{\text{ADDR14}}$, $\overline{\text{ADDR13}}$, and the output of a 3-bit module address switch or jumper on the module. This is ANDed together with $\overline{\text{I/O}}$ high and $\overline{\text{REQ}}$ low to select the module. The direction of transfer is indicated by WRITE, and the less significant address lines ($\overline{\text{ADDR12}}$ through $\overline{\text{ADDR0}}$) select the addressed byte within the module.

6.1.1 If the module cannot operate with a 400-nanosecond $\overline{\text{REQ}}$, then it should utilize $\overline{\text{WAIT}}$ to force $\overline{\text{REQ}}$ to last as long as required, consistent with the rules for $\overline{\text{WAIT}}$ outlined in section 5.3. It is not necessary to use $\overline{\text{WAIT}}$ if the module is fast, nor is it necessary that $\overline{\text{WAIT}}$ be pulled the same length of time for reading as for writing. The individual module may take account of its own requirements.

.1.2 If a module contains mixed speeds or types of memory, the various logical blocks should be considered logically separate units, with separate address detectors and separate data drivers. Again, the module may put no more than two active loads on any bus line, and if multiple blocks are loading the same lines, it may be necessary to buffer some lines to comply with these rules.

6.2 I/O. Refer to figure 5, Typical I/O Module Interface. I/O modules are addressed differently than memory modules. There are 16 module addresses coded into $\overline{\text{ADDR11}}$, $\overline{\text{ADDR10}}$, $\overline{\text{ADDR9}}$, and $\overline{\text{ADDR4}}$. Eight other address lines ($\overline{\text{ADDR8}}$ through $\overline{\text{ADDR5}}$ and $\overline{\text{ADDR3}}$ through $\overline{\text{ADDR0}}$), are driven by the processor and can be used for any purpose agreed upon consistently between the hardware and firmware. It is expected that these other lines (sometimes called "strobes") act as further address qualifiers or subfunction selectors, although it is not necessary to view them in that manner.

6.2.1 In order for a module to recognize its address, it must compare the four module address bits ($\overline{\text{ADDR11}}$, $\overline{\text{ADDR10}}$, $\overline{\text{ADDR9}}$, and $\overline{\text{ADDR4}}$), and then compare that with $\overline{\text{I/O}}$ low and $\overline{\text{RFO}}$ low. This establishes that the module is currently being addressed, and $\overline{\text{WRITE}}$ again establishes the direction of transfer.

6.2.2 There is no current provision for multiple modules to share the same module address (with 16 addresses and only 15 physical backplane slots it is unnecessary to share addresses). If it becomes desirable in the future, it should be considered as a special situation outside of the normal bus rules and handled very carefully.

6.2.3 A module which wants to interrupt must pull one or the other ($\overline{\text{ATN}}$/$\overline{\text{ATN?}}$) low. As soon as the processor interrogates status from the interrupting module, the module should assume that the processor is about to service the interrupt and it should release $\overline{\text{ATN}}$/$\overline{\text{ATN?}}$ at that time. This is independent of the polling identification requirements for pollable interrupting modules. It is not necessary to release $\overline{\text{ATN}}$/$\overline{\text{ATN?}}$ as a result of a polling operation. (Refer to section 5.4)

6.2.4 A pollable interrupting module which has an interrupt pending (requested but not yet acknowledged) may be polled by the processor. The processor will pull $\overline{\text{POLL}}$ low, and shortly thereafter will perform an input operation at some module address which is unable to respond to an input (read from the display, for example). During this pseudo-input operation, a pollable module which has an interrupt pending, must pull down on one bus data line. The line which is pulled identifies the requesting module to the processor. Since there are eight data lines, up to eight modules may be handled by this method. By agreement, the Cartridge Tape Module pulls on $\overline{\text{BUS7}}$. (Refer to section 3.16)

7.0 RULES FOR BUS CONTROLLER MODULES.

7.0.1 A bus controller requires provision for deriving all the timing and control signals used to transfer data between itself and a slave module, as well as resolving control conflicts between itself and other controller modules. At a minimum, this implies a bus control circuit (figure 6) including control, address, data drivers and/or data receivers. There are other possible bus control circuit designs, but the one shown is the simplest which is suitable for all purposes. All of the features of this circuit may not be needed in all cases. (Refer to section 7.0.4 for the bus controller states, bus controller state diagram (figure 7), and bus controller timing diagram (figure 8) for an explanation of state transitions.)

7.0.2 The bus controller circuit shown in figure 6 is suitable for the main processor in the system. This element has two requirements not placed on any other controller--they do the driving of $\overline{\text{PROC ACTIVE}}$ when that module is controlling the bus (driving address lines) and they respond to RUN to hold off transition from Idle to Bus Bid states.

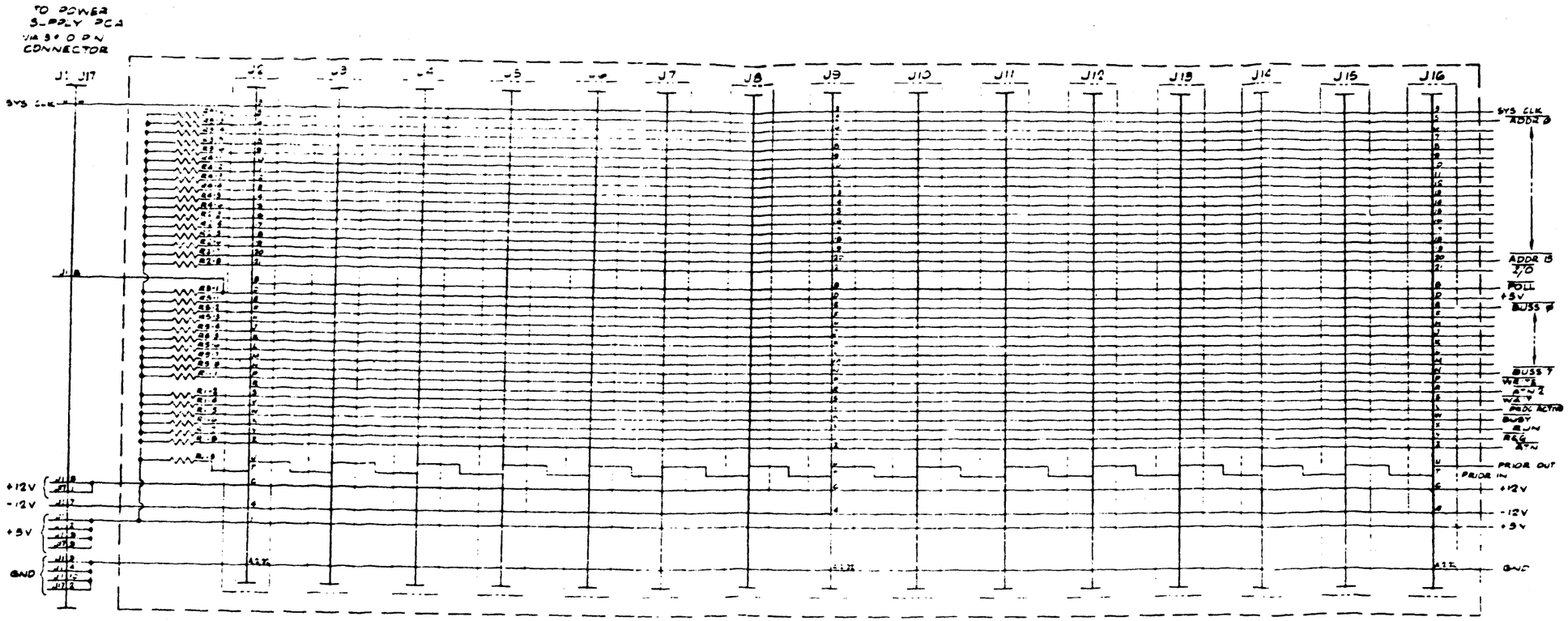
7.0.3 Modules other than the processor do not need to use these signals. They must not drive $\overline{\text{PROC ACTIVE}}$ because this would prevent single-step processor cycles from operating predictably. It is not important for non-processor controllers to respond to RUN.

7.0.4 RUN and Start Cycle must be present at the same time as a SYS CLK edge, otherwise the cycle start request will be missed. If Start Cycle is a pulse, it may have to be latched (the latch can be cleared by the B flip-flop, which will be set when the bus has been obtained). If the module does not use RUN, and if Start Cycle is a pulse of longer duration that one period of SYS CLK, it is not necessary to latch Start Cycle.

Name	ABC	Signals Driven
IDLE	000	-
BUS BID	100	PRIOR OUT
BUS OBTAIN	110	PRIOR OUT, $\overline{\text{BUS0}}$ thru $\overline{\text{BUS7}}$ (if $\overline{\text{WRITE}}$), $\overline{\text{ADDR0}}$ thru $\overline{\text{ADDR15}}$, $\overline{\text{BUSY}}$, $\overline{\text{PROC ACTIVE}}$ (if main processor), $\overline{\text{WRITE}}$ (if write operation), $\overline{\text{I/O}}$ (if not memory operation)
REQUEST	111	Same as 110 above, plus $\overline{\text{REQ}}$
WAIT	011	$\overline{\text{ADDR0}}$ thru $\overline{\text{ADDR15}}$, $\overline{\text{REQ}}$, $\overline{\text{BUSY}}$, $\overline{\text{BUS0}}$ thru $\overline{\text{BUS7}}$ (if $\overline{\text{WRITE}}$), $\overline{\text{WRITE}}$ (if write operation), $\overline{\text{PROC ACTIVE}}$ (if main processor)
RELEASE	001	$\overline{\text{ADDR0}}$ thru $\overline{\text{ADDR15}}$, $\overline{\text{BUS0}}$ thru $\overline{\text{BUS7}}$ (if $\overline{\text{WRITE}}$) $\overline{\text{WRITE}}$ (if write operation), $\overline{\text{I/O}}$ (if not memory operation), $\overline{\text{PROC ACTIVE}}$ (if main processor)
IDLE	000	-

7.0.5 The priority chain gate between PRIOR IN and PRIOR OUT functions as a negative OR gate, whose output is low when either input is low. When PRIOR IN is low, the controller is prevented from obtaining the bus (if it is in the Bus Bid state) by the 3-input AND gate between the A and B flip-flops. The signal must also be passed down the priority chain to other lower priority modules which might also be requesting the terminal bus at the same time. (This is true whether this controller is active or not, and hence the gate to pass low PRIOR IN directly to a low PRIOR OUT.)

7.0.6 Slave modules are entitled to expect that data and address lines will be valid and stable before, during, and after $\overline{\text{REQ}}$ is low. They use $\overline{\text{REQ}}$ to gate their data onto the bus during a read cycle (involving that data will be changing very shortly after $\overline{\text{REQ}}$ changes). The rise times may be slow since all bus lines are open-collector. To prevent loss of the data, it must be latched up by the controller module. Thresholds may vary, and the rise times of $\overline{\text{REQ}}$ may be slow. Therefore, it is recommended that another, faster version of $\overline{\text{REQ}}$ be generated locally, in parallel with the version used to drive the bus. This fast version of $\overline{\text{REQ}}$ can be a totem pole driver having a fast rise time, and therefore, will occur predictably before $\overline{\text{REQ}}$ on the bus has had a chance to disable the data drivers in the slave module. The drivers provide the required timing for control, address, and data lines. All address, data, I/O, and write signals should be present for longer than the control signals, in order to preserve the desired timing.


TO POWER SUPPLY PCA VIA 90 PIN CONNECTOR
J1
J17
J16
J15
SYS CLK
+12V
-12V
+5V
GND
SYS CLK
ADDR B
ADDR B 7-0
ROLL
+5V
BUSS B
BUSS T
WE B
A-N 2
WE T
PROC ACTIVE
BUSY
RUN
REQ
ATN
PRIOR OUT
PRIOR IN
+12V
-12V
+5V
GND

LANE PCA

IN CONNECTOR

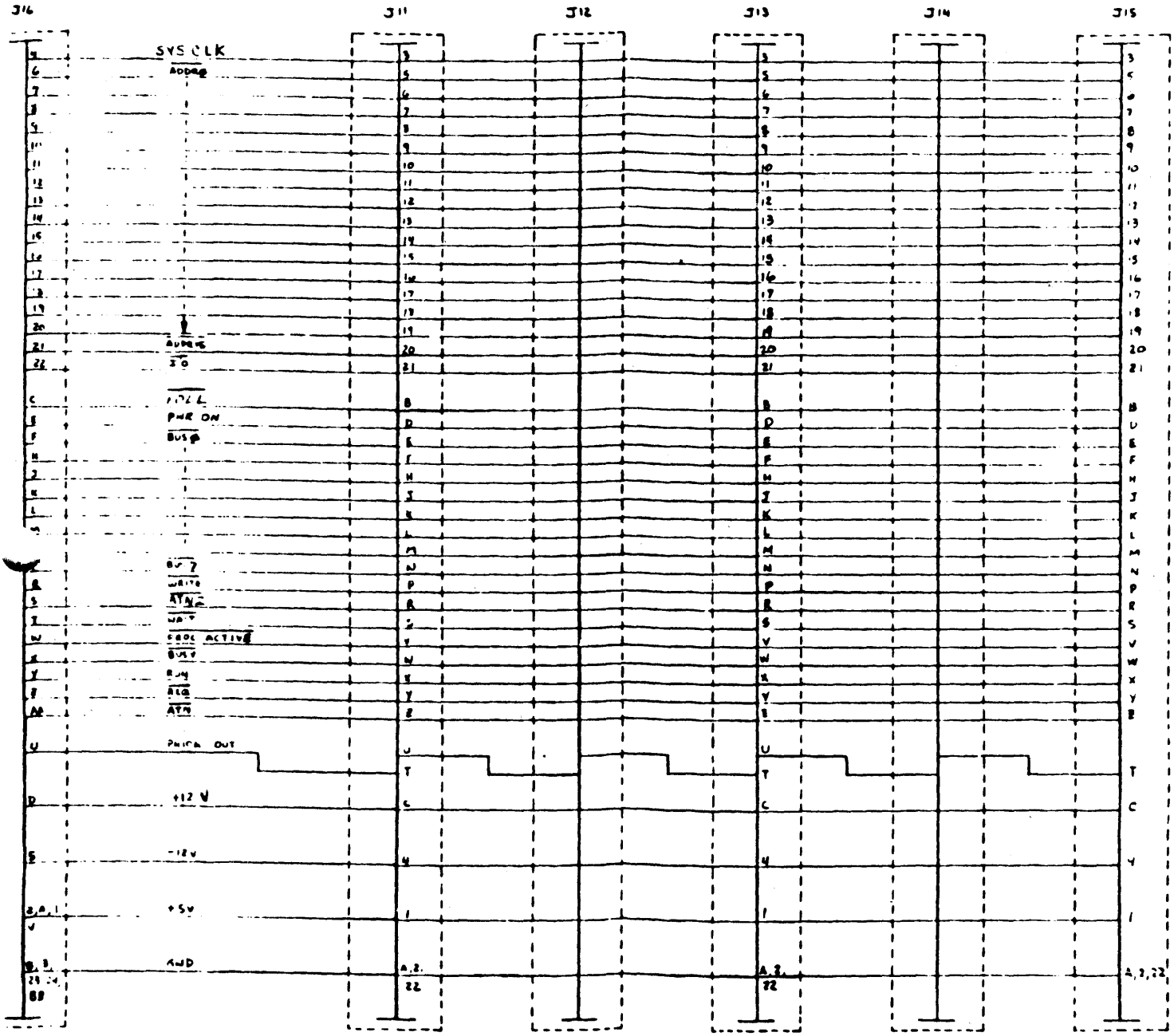


Figure 2
Backplane Extender PCA (6 Slot) Schematic Diagram
APR-26-78 **13255-91158**

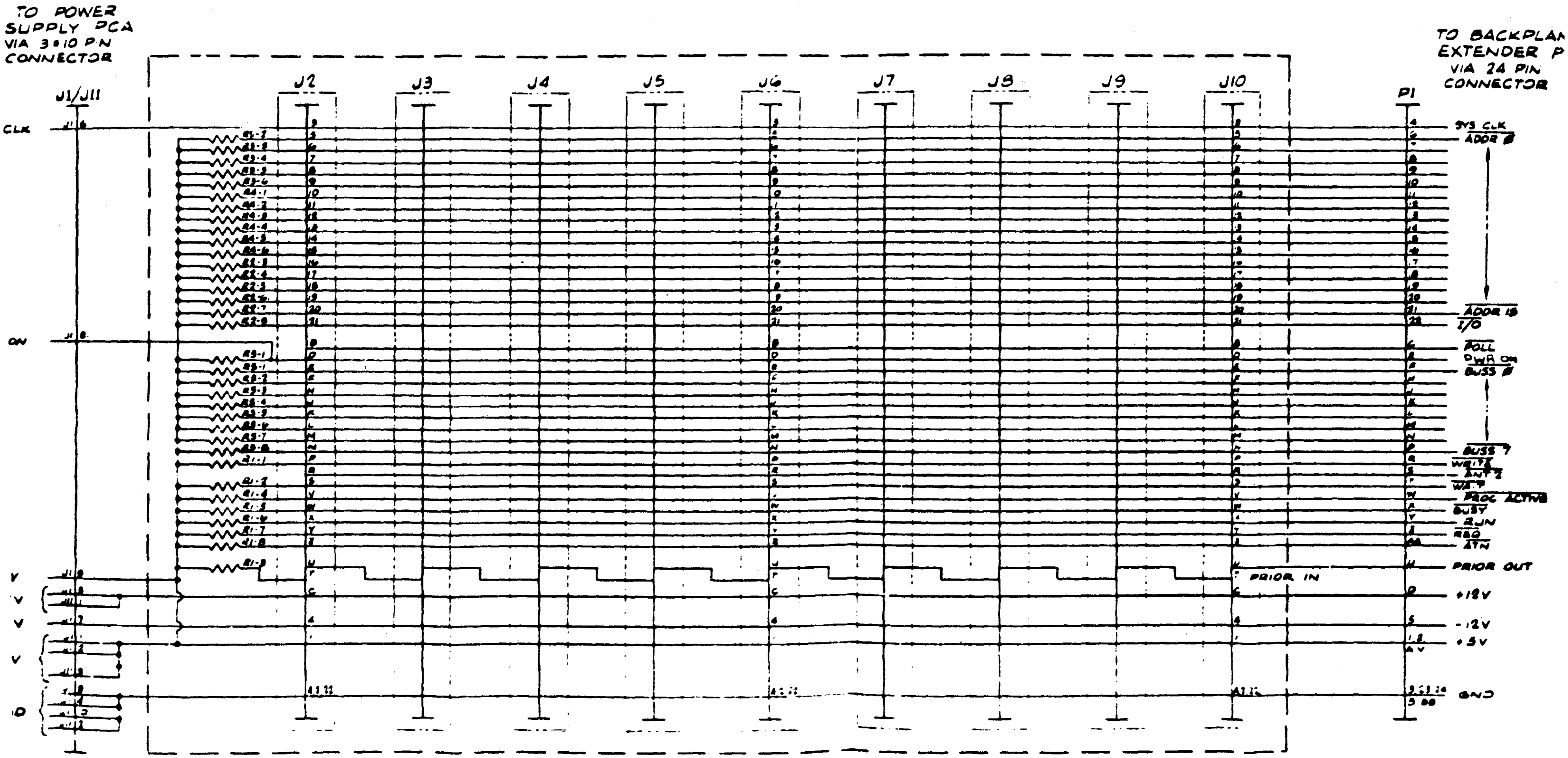


Figure 1
Backplane PCA (9 slot) Schematic Diagram
[illegible]-26078 [illegible]

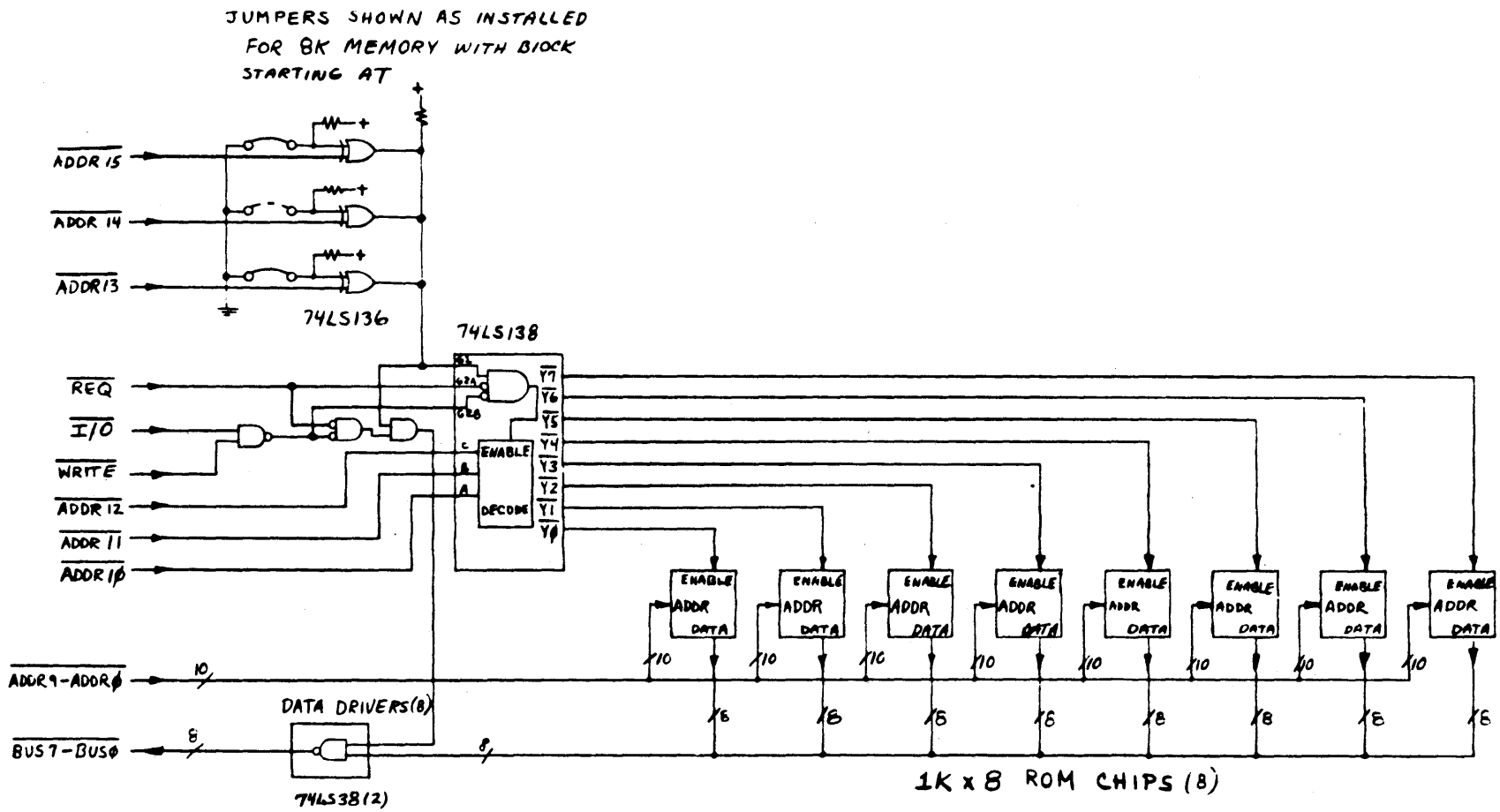


Figure 5
Typical Memory Module Interface Diagram
APR-26-78 13255-91158

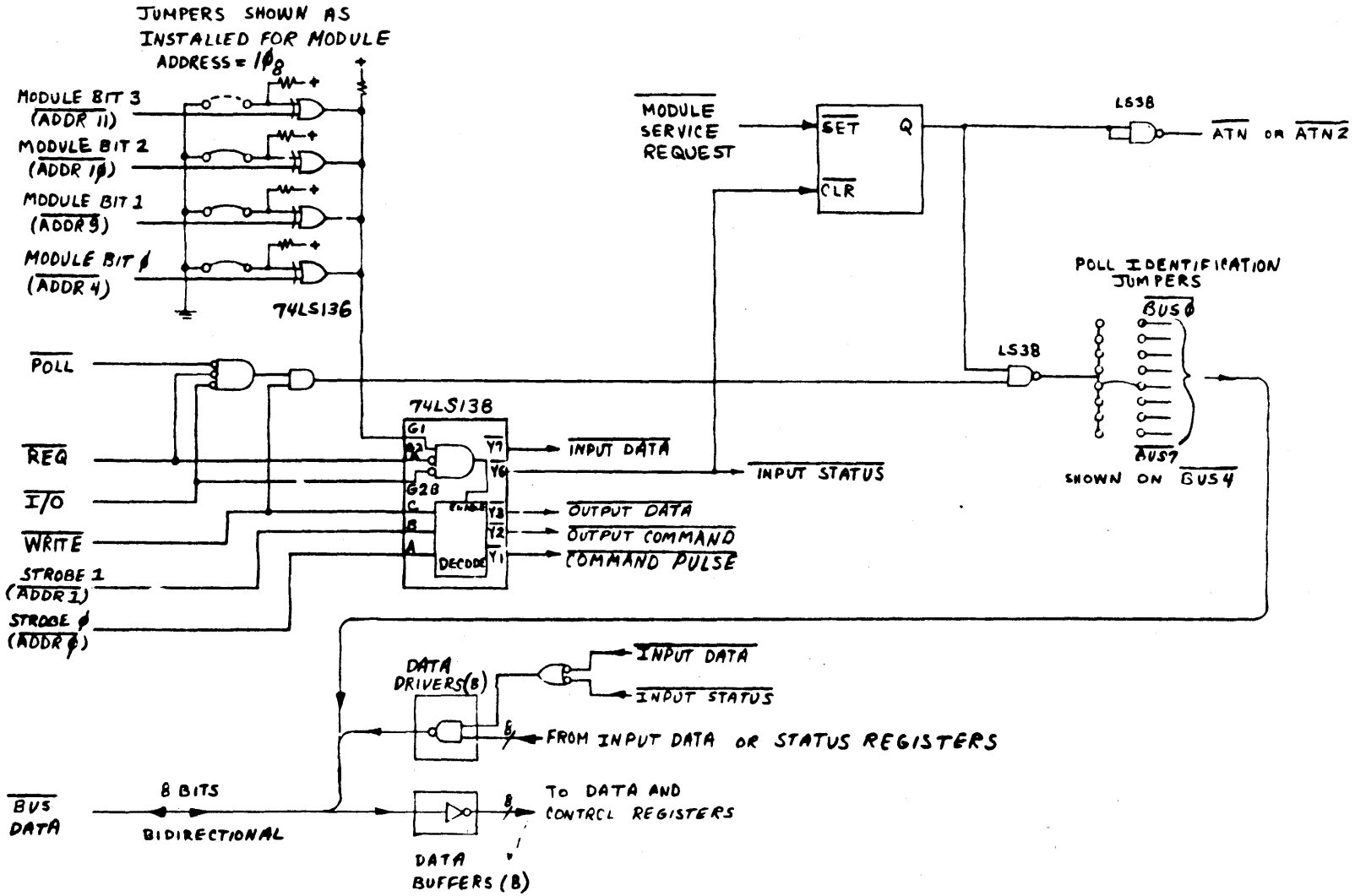
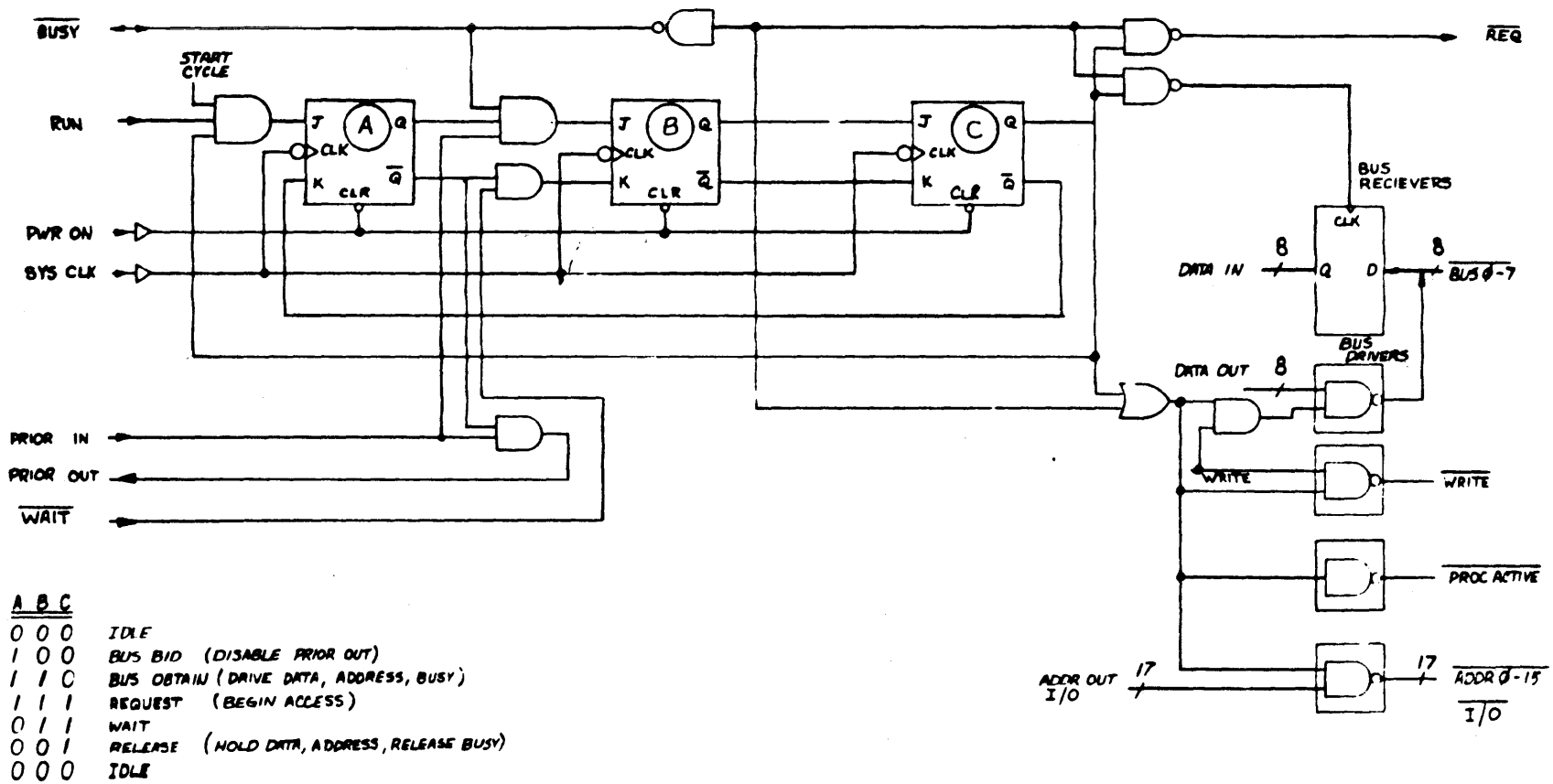


Figure 6
Typical I/O Module Interface Diagram
APR-26-78 13255-9115P



A	B	C	
0	0	0	IDLE
1	0	0	BUS BID (DISABLE PRIOR OUT)
1	1	0	BUS OBTAIN (DRIVE DATA, ADDRESS, BUSY)
1	1	1	REQUEST (BEGIN ACCESS)
0	1	1	WAIT
0	0	1	RELEASE (HOLD DATA, ADDRESS, RELEASE BUSY)
0	0	0	IDLE

Figure 7
Bus Controller Circuit Diagram
APR-26-78 13255-9115A

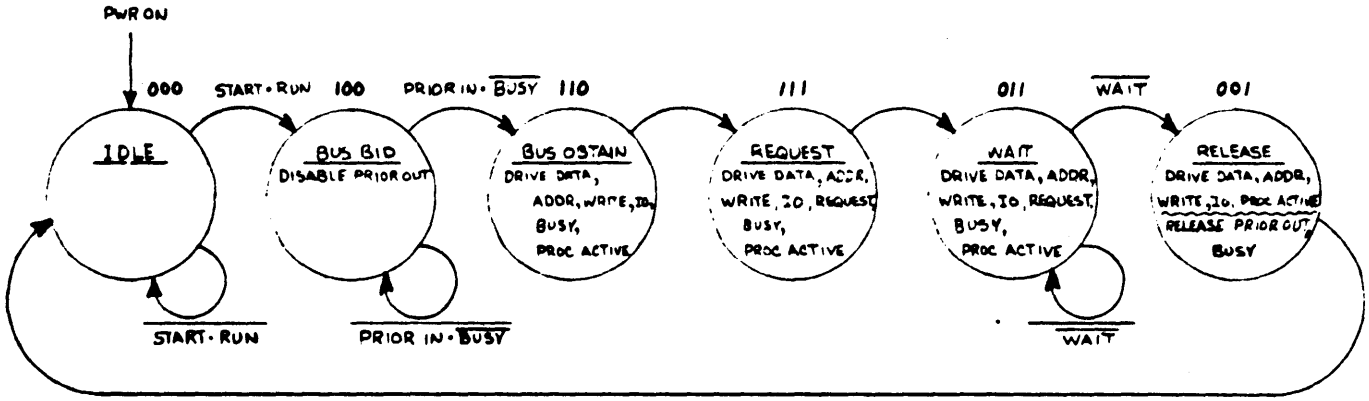


Figure 8
Bus Controller State Diagram
APR-26-78 13255-9115A

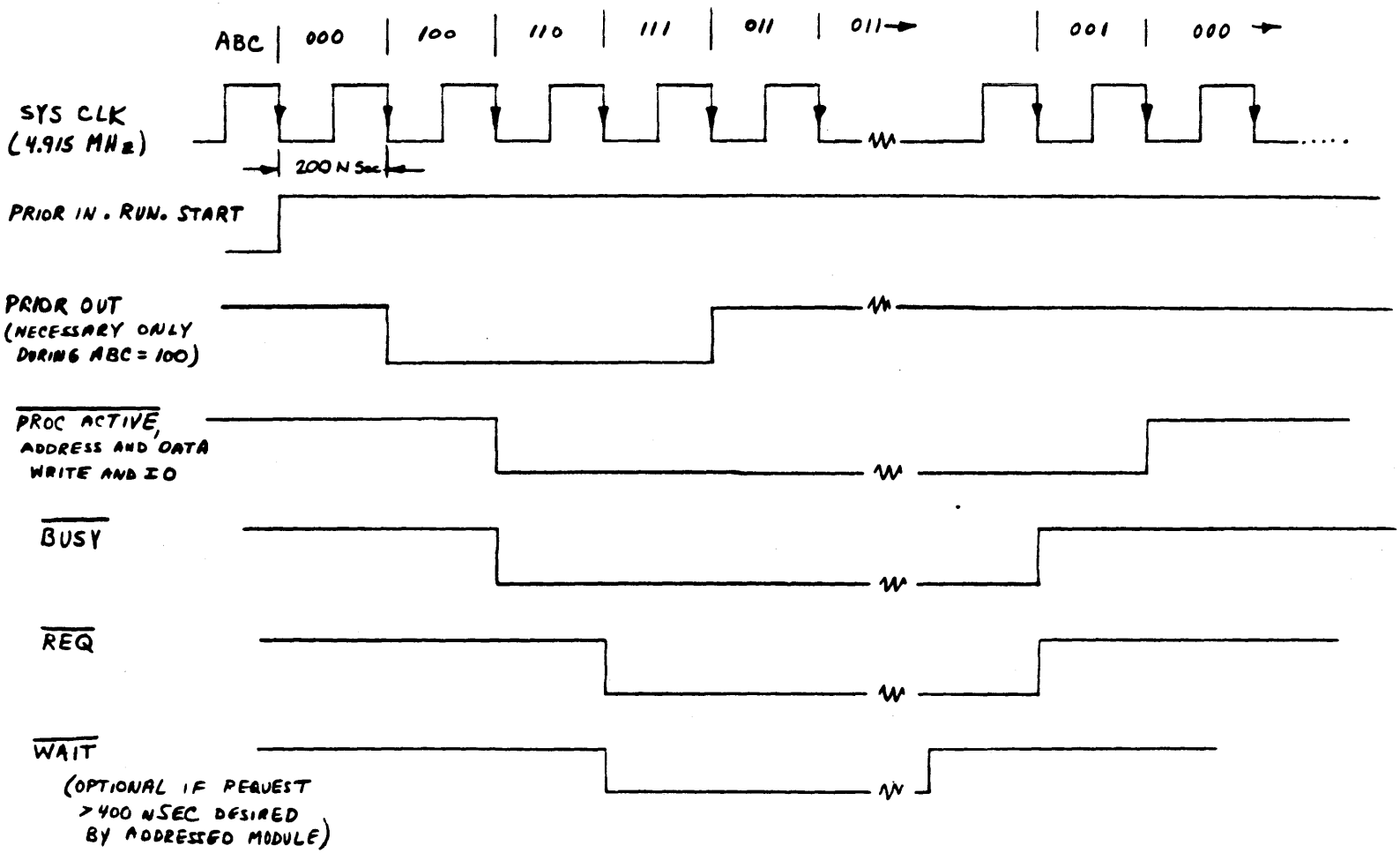


Figure 9
Bus Controller Timing Diagram
APR-26-78 13255-91158

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02640-60153	4		ASSEMBLY, BACKPLANE	28480	02640-60153
J1	1251-3319	4	1	CONNECTOR 10-PIN M POST TYPE	28480	1251-3319
J2	1251-1887	7	8	CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J3	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J4	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J5	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J6	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J7	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J8	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J9	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J10	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	A2640-60002	2		BACKPLANE ENT.	28480	A2640-60002
J11	1251-1887	7	5	CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J12	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J13	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J14	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J15	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J16	1251-3207	9	1	CONNECTOR-PC EDGE 24-CONT/ROW 2-ROWS	28480	1251-3207

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02640-60158	9	1	ASSEMBLY, BACKPLANE 15	28480	02640-60158
J1	1251-3319	4	1	CONNECTOR 10-PIN M POST TYPE	28480	1251-3319
J2	1251-1887	7	15	CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J3	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J4	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J5	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J6	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J7	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J8	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J9	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J10	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J11	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J12	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J13	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J14	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J15	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J16	1251-1887	7		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
J17	1251-3675	5	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-3675
R1	1810-0132	9	5	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	91637	CSP09C-07-501J
R2	1810-0132	9		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	91637	CSP09C-07-501J
R3	1810-0132	9		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	91637	CSP09C-07-501J
R4	1810-0132	9		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	91637	CSP09C-07-501J
R5	1810-0132	9		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	91637	CSP09C-07-501J

Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	02645-60005	0	1	ASSEMBLY, MAINFRAME	28480	02645-60005
	0403-0285	9	4	BUMPER FOOT-ADH MTG 12.7-MM-AD	28480	0403-0285
	0403-0345	2	2	BUMPER FOOT-ADH MTG .25-IN-AD	28480	0403-0345
	0570-0528	8	2	STUD, PASIN 5/16	28480	0570-0528
	0570-0585	5	1	STUD, RETAINER	28480	0570-0585
	1390-0326	1	1	LATCH, ADJ PANL	28480	1390-0326
	1390-0327	2	1	LATCH, ADJ PANL	28480	1390-0327
	2190-0918	4	8	WASHER-LK HLCL NO. 8 .141-IN-ID	28480	2190-0918
	2360-0196	1	8	SCREW-MACH 8-32 .375-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
	2360-0197	2	8	SCREW-MACH 8-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	3050-0066	8	8	WASHER-FL MTLC NO. 8 .187-IN-ID	28480	3050-0066
	3050-0228	4	2	WASHER-FL MTLC NO. 8 .156-IN-ID	28480	3050-0228
	3110-0100	9	1	HINGE, RIGHT	28480	3110-0100
	3110-0101	0	1	HINGE, LEFT	28480	3110-0101
	02640-00010	6	1	SUPPORT	28480	02640-00010
	02640-00025	3	2	SUPPORT, HINGE	28480	02640-00025
	02640-20019	7	1	DOOR, REAR	28480	02640-20019
	02640-40001	9	1	MAINFRAME, SHELL	28480	02640-40001
	02640-60158	9	1	BACKPLANE ASSEMBLY	28480	02640-60158
	02640-60203	5	1	POWER SUPPLY ASSEMBLY	28480	02640-60203