HP 13255

GENERAL PURPOSE ASYNCHRONOUS DATA COMM MODULE
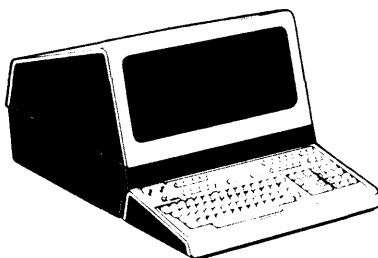
Manual Part No. 13255-91089

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DATA TERMINAL
TECHNICAL INFORMATION

HEWLETT **hp** *PACKARD*

1.0 INTRODUCTION.

The General Purpose Asynchronous Data Communications Module provides a general purpose EIA RS232C or 20 mA dc current loop link from the terminal to an external device. The GP Async Data Comm PCA transmits and receives bit serial data to and from the external device through an interface cable assembly, provides parallel-to-serial and serial-to-parallel conversion, and transmits and receives bit parallel data to and from the terminal through the Backplane Assembly (data bus). Refer also to the Operating and Service Manual (HP Part No. 02640-90042) for additional information. Parts lists for 02640-60043, 02640-60058, 02640-60059, 02640-60077, 02640-60131, and 02645-60002 are contained in module section 13255-91086.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the GP Async Data Comm Module is contained in tables 1.0 through 6.5.

Table 1.0   Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60043	103/102 Cable Ass'y	N/A	N/A
02640-60058	12531/12880 Cable Ass'y	N/A	N/A
02640-60059	RS232C Cable Ass'y	N/A	N/A
02640-60077	Test Hood Asembly	N/A	N/A
02640-60089	GP Async Data Comm PCA	12.9 x 4.0 x 0.6	0.50
02640-60097	Current Loop Cable Ass'y	N/A	N/A
02640-60098	RS232C Cable (Male) Ass'y	N/A	N/A
02640-60099	RS232C Cable (Female) Ass'y	N/A	N/A
02640-60131	US Modem Cable Ass'y	N/A	N/A
02645-60002	DC Self Test Hood	N/A	N/A
02645-60003	Current Loop Self Test Hood	N/A	N/A

Number of Backplane Slots Required: 1

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NOTE: This document is part of the 264XX DATA TERMINAL product
series Technical Information Package (HP 13255).

1.0   INTRODUCTION.

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          general purpose EIA RS232C or 20 mA dc current loop link from the ter-
          minal to an external device. The GP Async Data Comm PCA transmits and
          receives bit serial data to and from the external device through an
          interface cable assembly, provides parallel-to-serial and serial-to-
          parallel conversion, and transmits and receives bit parallel data to
          and from the terminal through the Backplane Assembly (data bus). Refer
          also to the Operating and Service Manual (HP Part No. 02640-90042) for
          additional information. Parts lists for 02640-60043, 02640-60058,
          02640-60059, 02640-60077, 02640-60131, and 02645-60002 are contained
          in module section 13255-91086.

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02645-60002	DC Self Test Hood	N/A	N/A
02645-60003	Current Loop Self Test Hood	N/A	N/A

Number of Backplane Slots Required: 1

Table 2.0   Reliability and Environmental Information

```
======================================================================
I                                                                    I
I  Environmental:     ( X ) HP Class B      (   ) Other:             I
I                                                                    I
I                                                                    I
I  Restrictions:  Type tested at product level                      I
I                                                                    I
I                                                                    I
I                                                                    I
I======================================================================I
I                                                                    I
I         Failure Rate:    1.502    (percent per 1000 hours)         I
I                                                                    I
======================================================================
```

Table 3.0   Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

```
======================================================================
I              I               I               I                    I
I +5 Volt Supply I +12 Volt Supply I -12 Volt Supply I -42 Volt Supply I
I              I               I               I                    I
I @ 300 mA     I  @  40 mA     I  @  20 mA     I   @     mA         I
I              I               I               I                    I
I              I               I               I   NOT APPLICABLE   I
I==============================================I=====================I
I                              I                                    I
I         115 volts ac         I          220 volts ac             I
I                              I                                    I
I          @     A             I           @     A                  I
I                              I                                    I
I       NOT APPLICABLE         I         NOT APPLICABLE             I
I==============================================================I
I                                                                    I
I         Clock Frequency:  4.915   MHz                              I
I                                                                    I
I                                                                    I
======================================================================
```

Table 4.0   Switch Definitions

PCA Designation	Function
A11,A10,A9,A4	Module Address Selection (see section 4.0)
FC0 thru FC7	Firmware Control Word - Function depends on firmware application

CBE	Custom Baud Rate Enable
	  Closed - The custom baud rate generator is enabled when the baud rate switch is in the EXT position
	  Open - The custom baud rate generator is disabled

B0 thru B11	Custom Baud Rate Selection (see section 4.1)
S0,S1,S2	Split Baud Rate Selection (see section 4.2)

134	134.5 Baud
	  Closed - Enable 134.5 baud and 6-bit data word when baud rate switch is in 150 position
	  Open - Disable 134.5 baud

2SB	Two Stop Bits
	  Closed - Transmit and receive data with two stop bits at all baud rates
	  Open - Transmit and receive data with one stop bit at all baud rates except 110 (two stop bits)

THE	Transmit Handshake Enable
	  Closed - Enable transmit handshake circuit
	  Open - Disable transmit handshake circuit

RHE	Receive Handshake Enable
	  Closed - Enable receive handshake circuit
	  Open - Disable receive handshake circuit

IAT	Inhibit $\overline{ATN}$
	  Closed - Disable Data Comm Interrupt from this module
	  Open - Enable Data Comm Interrupt from this module

Table 5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{ADDR0}$	Negative True, Address Bit 0
-6		Not Used
-7	$\overline{ADDR2}$	Negative True, Address Bit 2
-8	$\overline{ADDR3}$	Negative True, Address Bit 3
-9	$\overline{ADDR4}$	Negative True, Address Bit 4
-10	$\overline{ADDR5}$	Negative True, Address Bit 5
-11	$\overline{ADDR6}$	Negative True, Address Bit 6
-12		}
-13		} Not Used }
-14	$\overline{ADDR9}$	Negative True, Address Bit 9
-15	$\overline{ADDR10}$	Negative True, Address Bit 10
-16	$\overline{ADDR11}$	Negative True, Address Bit 11
Pin -17 through Pin -20		} } Not Used }
-21	$\overline{I/O}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	
-D	PWR ON	System Power On
-E	$\overline{BUS0}$	Negative True, Data Bus Bit 0
-F	$\overline{BUS1}$	Negative True, Data Bus Bit 1
-H	$\overline{BUS2}$	Negative True, Data Bus Bit 2
-J	$\overline{BUS3}$	Negative True, Data Bus Bit 3
-K	$\overline{BUS4}$	Negative True, Data Bus Bit 4
-L	$\overline{BUS5}$	Negative True, Data Bus Bit 5
-M	$\overline{BUS6}$	Negative True, Data Bus Bit 6
-N	$\overline{BUS7}$	Negative True, Data Bus Bit 7
-P	$\overline{WRITE}$	Negative True, Write/Read Type Cycle
-R		}
		} Not Used
-S		}
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		}
		}
-W		} Not used
		}
-X		}
-Y	$\overline{REQ}$	Negative True, Request (Bus Data Currently Valid)
-Z	$\overline{ATN}$	Negative True, Data Comm Interrupt Request

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	$\overline{ENCL}$	Negative True, Current Loop Enable
- 2	$\overline{INI}$	Negative True, Invert Current Loop Received Data
- 3	CL+12	Power Source for Current Loop Active Receiver
- 4	CL+	Current Loop Receiver Positive Input
- 5	CL-	Current Loop Receiver Negative Input
- 6	CLA	Current Loop Transmitter Current Sourcing Terminal
- 7	CLP	Current Loop Transmitter Current Sinking Terminal
- 8	$\overline{INO}$	Negative True, Invert Current Loop Transmitted Data
- 9	PON	Power On Clear
-10	$\overline{ISB}$	Negative True, Invert the Sense of SB
-11	XECL	Programmable Control Signal
-12	TTYIN	Teletype Current Loop Receiver Input
-13		}
-14		} Not Used
-15	TEST	9650 Test Point

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P2, Pin A	GND	Signal Ground
-B	BA	Transmitted Data Out
-C	BB	Received Data In
-D	CA	Request to Send
-E	CB	Clear to Send
-F		Not Used
-H	GND	Signal Ground
-J	CF	Carrier Received
-K	X8 OUT	Clock of 8 X the Transmit Baud Rate
-L	X16 OUT	Clock of 16 X the Transmit Baud Rate
-M	SA	Secondary Channel Transmitted Data
-N	SB	Secondary Channel Received Data
-P	CD	Data Terminal Ready
-R		Not Used
-S	X16 IN	Clock of 16 X the Receive Baud Rate

Table 6.0   Module Bus Pin Assignments

Function Performed: Output Data Character for Transmission	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)	X	ADDR 12
Switch Selectable (0001)=Data Comm	A11	ADDR 11
(0101)=Printer	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR5 = 1	X	ADDR 8
ADDR6 = 1	X	ADDR 7
	1	ADDR 6
	1	ADDR 5
	A4	ADDR 4
	X	ADDR 3
	X	ADDR 2
Data Bus Bit Interpretation:	X	ADDR 1
	X	ADDR 0
B7 Data Output Bit 7	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
B6 Data Output Bit 6	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
B5 Data Output Bit 5	B0	BUS 0
	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
B4 Data Output Bit 4	X=Don't Care	
B3 Data Output Bit 3		
B2 Data Output Bit 2		
B1 Data Output Bit 1		
B0 Data Output Bit 0		

Table 6.1 Module Bus Pin Assignments

Function Performed: Read Firmware Control Word (FC Switches)	Value	Bus Signal
Poll Bit: Not Applicable	X	ADDR 15
	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)	X	ADDR 12
Switch Selectable (0001)=Data Comm	A11	ADDR 11
(0101)=Printer	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR5 = 0	X	ADDR 8
ADDR6 = 1	X	ADDR 7
	1	ADDR 6
Data Bus Bit Interpretation:	0	ADDR 5
	A4	ADDR 4
B7 Switch FC7	X	ADDR 3
0 = Switch Closed	X	ADDR 2
1 = Switch Open	X	ADDR 1
	X	ADDR 0
B6 Switch FC6	B7	BUS 7
0 = Switch Closed	B6	BUS 6
1 = Switch Open	B5	BUS 5
B5 Switch FC5	B4	BUS 4
0 = Switch Closed	B3	BUS 3
1 = Switch Open	B2	BUS 2
	B1	BUS 1
B4 Switch FC4	B0	BUS 0
0 = Switch Closed		
1 = Switch Open	1=Logical 1=Bus Low	
B3 Switch FC3	0=Logical 0=Bus High	
0 = Switch Closed	X=Don't Care	
1 = Switch Open		
B2 Switch FC2		
0 = Switch Closed		
1 = Switch Open		
B1 Switch FC1		
0 = Switch Closed		
1 = Switch Open		
B0 Switch FC0		
0 = Switch Closed		
1 = Switch Open		

Table 6.2 Module Bus Pin Assignments

Function Performed: Input Module Status Byte	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)	X	ADDR 12
Switch Selectable (0001)=Data Comm	A11	ADDR 11
(0101)=Printer	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR5 = 1	X	ADDR 8
ADDR6 = 0	X	ADDR 7
A0 = 0 Read Standard Status	0	ADDR 6
A0 = 1 Read Alternate Status	1	ADDR 5
	A4	ADDR 4
Data Bus Bit Interpretation:	X	ADDR 3
Alternate status is the same as the	X	ADDR 2
standard status unless noted otherwise	X	ADDR 1
	A0	ADDR 0
B7 Not Used	B7	BUS 7
	B6	BUS 6
B6 0 = SB On	B5	BUS 5
1 = SB Off	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
B5 0 = CB On	B1	BUS 1
1 = CB Off	B0	BUS 0

| 1=Logical 1=Bus Low |
| 0=Logical 0=Bus High |
| X=Don't Care |

B4   0 = CF On
     1 = CF Off

B3   0 = No Parity Error
     1 = Parity Error

B2   0 = No Overrun Error
     1 = Overrun Error

                                                                    (Alternate)

B1   0 = Transmit Holding Register Full   0 = Transmission in
     1 = Transmit Holding Register Empty   Progress
                                               1 = Transmission Complete

B0   0 = Receiver Register Empty
     1 = Receiver Register Full

Table 6.3 Module Bus Pin Assignments

Function Performed: Read Received Data Character		Value	Bus Signal
		X	ADDR 15
Poll Bit: Not Applicable		X	ADDR 14
		X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)		X	ADDR 12
Switch Selectable (0001)=Data Comm		A11	ADDR 11
(0101)=Printer		A10	ADDR 10
		A9	ADDR 9
Function Specifier: ADDR5 = 0		X	ADDR 8
ADDR6 = 0		X	ADDR 7
		0	ADDR 6
		0	ADDR 5
		A4	ADDR 4
		X	ADDR 3
		X	ADDR 2
Data Bus Bit Interpretation:		X	ADDR 1
		X	ADDR 0
B7	Data Input Bit 7		
		B7	BUS 7
		B6	BUS 6
		B5	BUS 5
B6	Data Input Bit 6	B4	BUS 4
		B3	BUS 3
		B2	BUS 2
		B1	BUS 1
B5	Data Input Bit 5	B0	BUS 0
		1=Logical 1=Bus Low	
		0=Logical 0=Bus High	
B4	Data Input Bit 4	X=Don't Care	
B3	Data Input Bit 3		
B2	Data Input Bit 2		
B1	Data Input Bit 1		
B0	Data Input Bit 0		

Table 6.4   Module Bus Pin Assignments

Function Performed: Output Control Register Bits	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)	X	ADDR 12
Switch Selectable (0001)=Data Comm	A11	ADDR 11
(0101)=Printer	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR5 = 0	X	ADDR 8
ADDR6 = 1	X	ADDR 7
	1	ADDR 6
	0	ADDR 5
	A4	ADDR 4
	X	ADDR 3
	X	ADDR 2
Data Bus Bit Interpretation:	X	ADDR 1
	X	ADDR 0
B7 Not Used	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
B6 0 = No Break	B4	BUS 4
1 = Break	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
B5 0 = Enable Parity	B0	BUS 0
1 = Inhibit Parity	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
B4 0 = Odd Parity	X=Don't Care	
1 = Even Parity		

RECEIVE BAUD RATE

	Ext Clk	110	150	300	1200	2400	4800	9600
B3	0	0	0	0	1	1	1	1
B2	0	0	1	1	0	0	1	1
B1	0	1	0	1	0	1	0	1

B0   0 = CA on
          1 = CA off

Table 6.5   Module Bus Pin Assignments

Function Performed: Input instruction to Set/Reset Data Terminal Ready (CD) and Set/Reset External Control signal (XECL)	Value	Bus Signal
	X	ADDR 15
	X	ADDR 14
Poll Bit: Not Applicable	X	ADDR 13
	X	ADDR 12
Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)	A11	ADDR 11
Switch Selectable (0001) = Data Comm	A10	ADDR 10
(0101) = Printer	A9	ADDR 9
	X	ADDR 8
Function Specifier: ADDR5 = 1	X	ADDR 7
ADDR6 = 1	1	ADDR 6
A2 = 0, XECL = Low	1	ADDR 5
A2 = 1, XECL = High	A4	ADDR 4
	A3	ADDR 3
A3 = 0, CD On	A2	ADDR 2
A3 = 1, CD Off	X	ADDR 1
	X	ADDR 0
Data Bus Bit Interpretation: Not Applicable	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
	B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

3.0   FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), component location diagram (figure 3), current loop configurations (figure 4), and parts lists (02640-60089, 02640-60097, 02640-60098, 02640-60099, and 02645-60003) located in the appendix.

     The functional description of this module is detailed in blocks as shown on the block diagram.

3.1   UART. The UART is an MOS/LSI device used for interfacing a serial asynchronous data path to a parallel data path. The baud rate, number of stop bits, and parity configuration of the received and transmitted serial characters can be programmed. (For details of the UART, consult Western Digital's TR1602B specification sheet.)

3.1.1   Transmitted and received characters can have 6, 7, or 8 data bits (excluding parity). All characters have one start bit. Characters have one stop bit unless 110 baud is selected or the 2SB Switch is closed, in which case two stop bits are used. Six or seven-bit data words can have even or odd parity. Eight-bit data words have no parity.

3.1.2   When the 134 Switch is closed and control register bits 3, 2, and 1 are "010", then 134.5 baud, six data bits, one start bit, and one stop bit are selected.

3.2   I/O INSTRUCTION DECODER.

3.2.1   The I/O instruction decoder is a circuit which decodes terminal data bus signals into hardware control signals on the PCA. It consists of a module address decoder (U46) and a 3-to-8 decoder (U45). The module address decoder is composed of four exclusive OR gates which can be programmed with switches. When the proper module address is present on $\overline{ADDR11}$, $\overline{ADDR10}$, $\overline{ADDR9}$, and $\overline{ADDR4}$, an enable signal is provided to the 3-to-8 decoder.

3.2.2   The 3-to-8 decoder provides control signals to the other functional

blocks. Address lines $\overline{ADDR0}$, $\overline{ADDR2}$, $\overline{ADDR3}$, $\overline{ADDR5}$, $\overline{ADDR6}$, and $\overline{WRITE}$ and

$\overline{I/O}$ are decoded and strobed by $\overline{REQ}$ to realize control pulses. The fol-
lowing control signals are activated as shown whenever the proper
module address is selected.

$\overline{I/O}$	$\overline{WRITE}$	$\overline{ADDR0}$	$\overline{ADDR2}$	$\overline{ADDR3}$	$\overline{ADDR5}$	$\overline{ADDR6}$	$\overline{REQ}$	
0	0	X	X	X	1	0	+	Load control register from data bus.
0	0	X	X	X	0	0	+	Load character into transmit half of UART.
0	1	X	X	X	1	0	0	Gate firmware control word onto data bus.
0	1	1	X	X	0	1	0	Gate status word onto data bus.
0	1	0	X	X	0	1	0	Gate modified status word onto data bus.
0	1	X	X	X	1	1	0	Gate received data from UART to data bus. Reset UART's Data Ready flip-flop
0	1	X	0	X	0	0	+	Set XECL high
0	1	X	1	X	0	0	+	Set XECL low
0	1	X	X	0	0	0	+	Turn CD off
0	1	X	X	1	0	0	+	Turn CD on

X = Don't Care
+ = Rising Edge

3.3   CONTROL REGISTER.

3.3.1   The control register is a 7-bit latch that contains the control state
          of the PCA. The control bits set the parity, baud rate, and RS232C
          control signals.

3.3.2   The register is composed of seven D-type flip-flops. Data is latched
          in this register from the data bus. The register's output controls the
          RS232C control lines and programs the UART and baud rate generator.

          When latched in the control register, $\overline{BUS1}$, $\overline{BUS2}$, and $\overline{BUS3}$ program the

          baud rate generator receive multiplexer. $\overline{BUS4}$ and $\overline{BUS5}$, in conjunction
          with the 134 and 2SB Switches, control the PI, SBS, WLS2, WLS1, and EPE
          signal inputs to the UART.

3.4   BAUD RATE GENERATOR.

3.4.1   The baud rate generator provides the timing for data reception and con-
          trol. It consists of two parts--a standard baud rate generator and a
          custom baud rate generator.

3.4.2   The standard baud rate generator is composed of three 4-bit binary
          counters (U37, U26, and U36) and associated presetting logic. The
          standard baud rates are derived by dividing the bus System Clock to a
          rate of 16 times the desired baud rate. The standard baud rates are:
          110 baud (1.76 kHz), 150 baud (2.4 kHz), 300 baud (4.8 kHz), 1200 baud
          (19.2 kHz), 2400 baud (38.4 kHz), 4800 baud (76.8 kHz), and 9600 baud
          (153.6 kHz). The counter preset function is only used when 110 or
          134.5 baud is selected.

The select inputs of the receive baud rate multiplexer (U35) are driven
by the control register. The proper X16 clock rate is selected to
drive the UART receiver. The receive baud rates are selected as fol-
lows:

CONTROL REGISTER 3	2	1	RECEIVE BAUD RATE	
1	1	1	9600	
1	1	0	4800	
1	0	1	2400	
1	0	0	1200	
0	1	1	300	
0	1	0	150	(If 134 Switch Open)
			134.5	(If 134 Switch Closed)
0	0	1	110	
0	0	0	External Clock	(If CBE Switch Open)
			Custom Baud Rate	(If CBE Switch Closed)

3.4.3   The custom baud rate generator also consists of three 4-bit binary
counters (U27, U17, and U14). These counters are programmed with 12
switches to produce the desired baud rate. The counters get preset
when the TC (Pin 15) output of all three counters is true. The TC out-
put of the last counter is gated with the bus System Clock to prevent
glitching and routed through a D-type flip-flop to square the signal.

The transmit baud rate multiplexer (U25) is programmed with the split-
rate (S0, S1, and S2) switches and selects a frequency to clock the
UART at the desired baud rate. The transmit baud rates are selected as
follows:

S2	S1	S0	TRANSMIT BAUD RATE
SC	SC	SC	Custom Baud Rate
SO	SO	SC	4800
SO	SC	SO	2400
SO	SC	SC	1200
SC	SO	SO	300
SC	SO	SC	150
SC	SC	SO	9600
SO	SO	SU	Selected Receive Baud Rate

SC = Switch Closed
SO = Switch Open

3.5   TRANSMIT HANDSHAKE.

3.5.1   The transmit handshake circuit provides the capability of handshaking
            transmitted data with an RS232C control line. When the transmit hand-
            shake circuit is enabled (THE Switch closed), the device receiving the
            transmission has the capability of signaling a "busy" condition on the
            CB or SB control lines and thus temporarily stopping data transmission.
            Transmission is halted by turning off the Transmit Clock (TBC) to the
            UART.

3.5.2   This circuit is a 2-state, synchronous machine that is clocked at 16
            times the transmit baud rate. CB and SB must be stable at the middle
            of the last sixteenth of the last stop bit of a character with at least
            150 nanoseconds of setup time. The Off state of CB signals a "busy"

            condition. The On state of SB signals a "busy" condition unless $\overline{ISB}$
            (P2, Pin 10) is grounded, in which case the Off state of SB signals a
            "busy" condition. If a "busy" signal appears on CB, SB, or both, then
            the transmission will be held off.

3.6   RECEIVE HANDSHAKE.

3.6.1   The receive handshake circuit provides the capability of handshaking
            received data with an RS232C control line.

3.6.2   When the receive handshake circuit is enabled (RHE Switch closed), CD
         is driven by the DR output of the UART. When DR is active (a character
         is in the receiver holding register of the UART), CD is turned off. CD
         is turned off at the nominal center of the first stop bit of each re-
         ceive character. When the character is read by the processor (DR
         cleared), CD is turned on. It should be noted that the mandatory dis-
         connect feature (ESCf) cannot be used when the receive handshake
         circuit is enabled.

3.6.3   To use the receive handshake function, the IAT (Inhibit $\overline{\text{ATN}}$) Switch
         must be closed. The PCA will not generate interrupts and must be
         scanned for received data.

3.7   STATUS.

3.7.1   The status circuit is used to gate RS232C control signal information
         (CF, CB, and SB) and UART status signals (DR, THRE, OE, and PE) to the
         terminal data bus. When the proper address is decoded, this circuit

         gates seven bits of status information onto the data bus while $\overline{\text{REQ}}$ is
         low. (Refer to table 6.2 for detailed explanation of data bit inter-
         pretation.)

3.8   FIRMWARE CONTROL WORD. The firmware control word circuit consists of
         drivers that gate an 8-bit firmware control word to the terminal data
         bus when enabled by the I/O instruction decoder. When the proper ad-
         dress is decoded, Switch FC0 through FC7 information is gated onto the

         data bus while $\overline{\text{REQ}}$ is low. A closed switch produces a logic 0 on the
         data bus and an open switch generates a logic 1.

3.9   CURRENT LOOP. The current loop circuits (In and Out) provide the capa-
         bility of transmitting and receiving data in a 20-mA dc current loop.
         (Refer to figure 4 for current loop configurations.)

3.9.1   The current loop receiver (In) is enabled when $\overline{\text{ENCL}}$ (P2, Pin 1) is low
         (grounded). The receiver can be configured as a floating, passive re-
         ceiver or as a non-floating, active receiver.

3.9.1.1   In the floating configuration, the transmitter sources current. The
          current path is into the CL+ (P2, Pin 4) terminal and out the CL- (P2,
          Pin 5) terminal. When a teletype is the transmitter, the TTY IN (P2,
          Pin 12) input should be used instead of the CL+ input. In the non-
          floating configuration, CL+12 (P2, Pin 3) and CL+ are connected, and
          CL- is connected to ground. (A passive transmitter should be used with
          this configuration.) The current path is from +12V into CL+ and out of
          CL- to ground. The transmitter can then short the CL+ and CL- termi-
          nals and make the path from +12V to ground directly.

3.9.1.2   The output current of the 5082-4352 opto-isolator (U11) is converted to
          a voltage with a 2.2K resistor and sensed with a 74LS132 (U19). From
          a distortion standpoint, the ideal 0-to-20 mA or 20 mA to 0 transition
          sense level is 10 mA. However, noise considerations dictate that some
          hysteresis should be incorporated into the design. The current transfer
          ratio of the opto-isolator and the thresholds of the 74LS132 are the
          primary factors in determining the current thresholds of the receiver.
          The 0-to-20 mA transition is sensed between 8.2 mA and 13.4 mA. The
          20 mA to 0 transition is sensed between 7.4 mA and 9.4 mA. There is
          always at least 0.82 mA of hysteresis in the receiver.

3.9.1.3   Current flowing in the receiver is interpreted as a mark. By grounding

          $\overline{INI}$ (P2, Pin 2), current flowing in the receiver can be interpreted as
          a space.

3.9.2   The current loop transmitter (Out) consists of a 20-mA dc current
          source and a 20-mA dc current sink.

3.9.2.1   The transmitter circuits are switched on and off to provide a high out-
          put impedance 20-mA dc current loop transmitter. The CLA line (P2, Pin
          6) will source 20 mA when on. The current path is from the +12V supply
          out the CLA pin, and into the receiver. The return path is ground.
          The CLP line (P2, Pin 7) will sink 20 mA dc when on. The current path
          is from the receiver into the CLP pin, and into the -12V supply. The
          return path is ground. This transmitter will source current into +7.5V
          to -12V (referenced to ground) or sink current from +12V to -7.5V (ref-
          erenced to ground).

3.9.2.2   The first stage of the transmitter consists of an NPN (2N4401) and a
          PNP (2N4403) transistor Q2 and Q1, respectively. This circuit shifts
          the data from TTL levels to the 12V levels required to turn the 20 mA
          current controllers on and off. The second stage controls the sourced
          and sunk current when on, and presents a high impedance to the line
          when off. The CLA and CLP output pins are protected with series di-
          odes. The output current is controlled by impressing a constant
          voltage across the 0.15K and 0.10K resistors that are in series with
          the output. This voltage is maintained by the 1.5K, 8.2K, 1.5K voltage
          divider. When the transmitter is on, 24V is impressed across these re-
          sistors. The two diodes in series with these resistors are used to
          reduce current variations due to temperature changes.

3.9.2.3   A mark is transmitted as current in the line. By grounding $\overline{INO}$ (P2,
          Pin 8), a space can be transmitted as current in the line.

3.9.3   Current Loop Specifications.

	Min	Max	Units
Passive Receiver, Floating			
Marking Current	15.0	25.00	mA
Spacing Current	0.0	5.00	mA
Voltage Drop, Marking	1.4	1.80	volts
Active Receiver, Non-floating			
Marking Current	0.0	10.00	mA
Spacing Current	20.0	25.00	mA
Open Circuit Voltage	1.4	1.80	volts
Active Transmitter			
Marking Current Sourced	17.0	25.00	mA
Marking Current Sunk	25.0	35.00	mA
Spacing Current	0.0	0.01	mA
Receiver Voltage			
(receiver sourcing)	- 7.5	12.00	volts
(receiver sinking)	-12.0	7.50	volts

4.0   MODULE ADDRESS STRAPPING.

The module address is a unique 4-bit value (2 octal digits) used to
address a particular module on the terminal data bus. The GP Async
Data Comm PCA can be straped to respond to any module address from 00
17. To determine the configuration of the A4, A11, A10, and A9
Switches, the following is required:

a) Convert the octal address to a binary address as shown below.

		Switch			
		A4	A11	A10	A9
Module Address	12	1	0	1	0
	3	0	0	1	1

b) Close a switch wherever a "0" appears in the binary
module address.

The data comm driver uses module address 10 and the RS232C printer
driver uses module address 12.

4.1   CUSTOM BAUD RATE STRAPPING.

The custom baud rate generator provides a clock that is 16 times the desired baud rate. The range of baud rates is from 37.5 to 2400 baud (within 1.0 percent). In addition, certain rates from 2400 to 19.2K baud are also provided.

The baud rate switches are configured as follows. (The example configuration is for 110 baud selection.)

    a) Divide 153600 by the desired baud rate.

       153600/110 = 1396.36

    b) Round the quotient to the nearest integer.

       1396.36 becomes 1396

    c) Subtract one from the rounded quotient.

       1396-1 = 1395

    d) Convert the decimal number to a 12-bit binary number.

SWITCH	MSB B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	LSB B0
1395	0	1	0	1	0	1	1	1	0	0	1	1

    e) Close a switch in every position that has a "1". The
       remaining switches are left open.

    f) To calculate the actual generated baud rate, divide
       153600 by the result of step b, above.

       153600/1396 = 110.03

             (Note: The actual rate may not be exactly
                     equal to the desired rate.)

To clock the receive half of the UART with a custom baud rate, the CBE Switch must be closed and bits, 1, 2, and 3 of the control register must be "0" (External Clock).

4.2 SPLIT BAUD RATE STRAPPING.

Baud rate selection is controlled by bits 1, 2, and 3 of the control register and the S0-S2 Switches. Bits 1, 2, and 3 of the control register, in conjunction with the 134 and CBE switches, determine the receive baud rate. If the S0-S2 Switches are all open the transmit baud rate will always be equal to the receive baud rate. The following chart shows the available split rates and corresponding switch configurations.

TRANSMIT BAUD RATE

RECEIVE BAUD RATE			EXT	CUSTOM	110	150	300	1200	2400	4800	9600	134.5	BIT.3	BIT.2	BIT.1	
		EXT	X		X	X	X	X	X	X	X		0	0	0	
		CUSTOM		X		X	X	X	X	X	X		0	0	0	CBE Switch Closed
R	B	110	X	X	X	X	X	X	X	X			0	0	1	
E	A	150	X			X	X	X	X	X	X		0	1	0	
C	U	300	X			X	X	X	X	X	X		0	1	1	
E	D	1200	X			X	X	X	X	X	X		1	0	0	
I		2400	X			X	X	X	X	X	X		1	0	1	
V	R	4800	X			X	X	X	X	X	X		1	1	0	
E	A	9600	X			X	X	X	X	X	X		1	1	1	
	T	134.5										X	0	1	0	134 Switch Closed
	E	S2	SO	SC	SO	SC	SC	SO	SO	SO	SC	SO				
		S1	SO	SC	SO	SO	SO	SC	SC	SO	SC	SO				
		S0	SO	SC	SO	SC	SO	SC	SO	SC	SO	SO				

      X = Available Split Rate
     SC = Switch Closed
     SO = Switch Open

Note: a) If all S0-S2 Switches are open, the transmit baud rate will equal the receive baud rate.
b) The 134 Switch must be closed to get 134.5 baud.
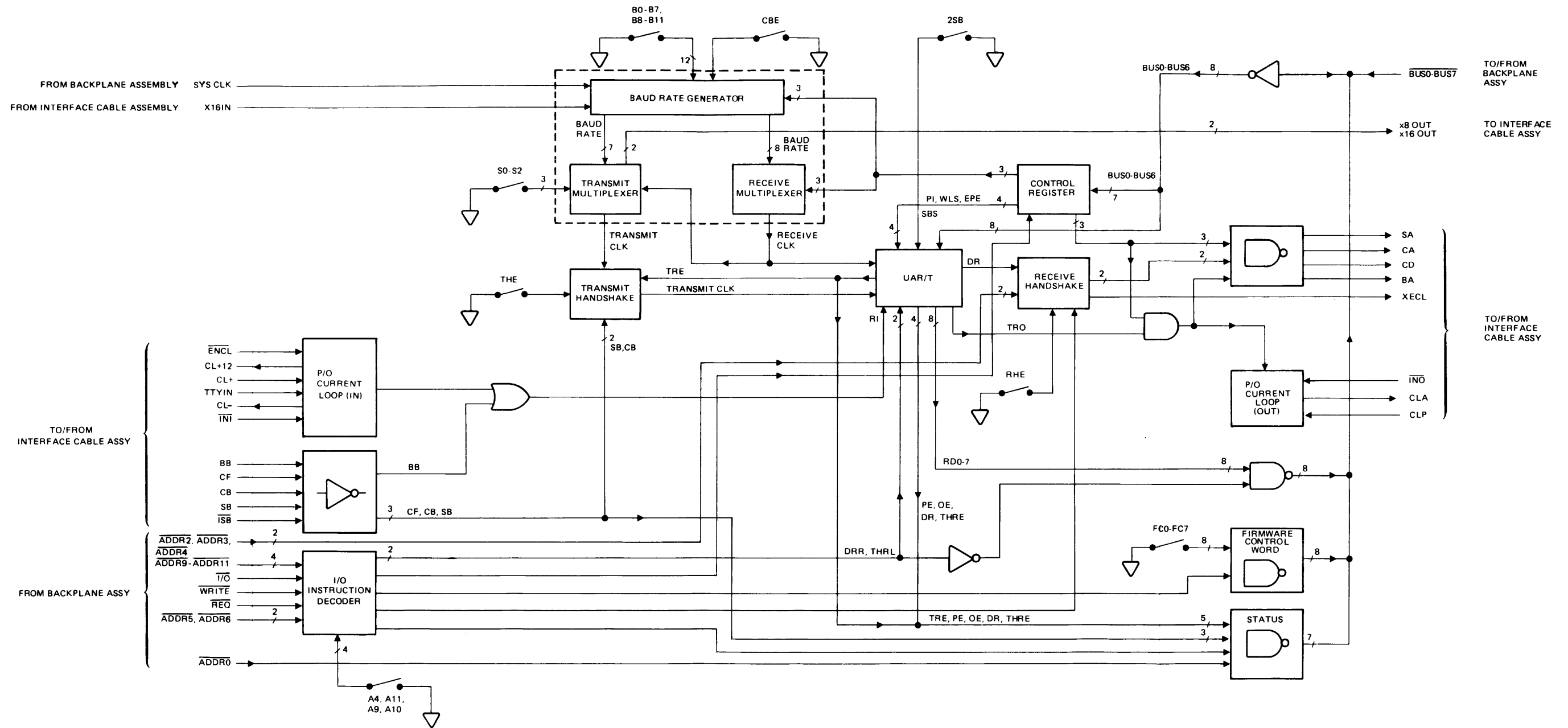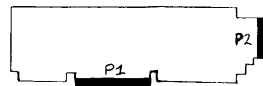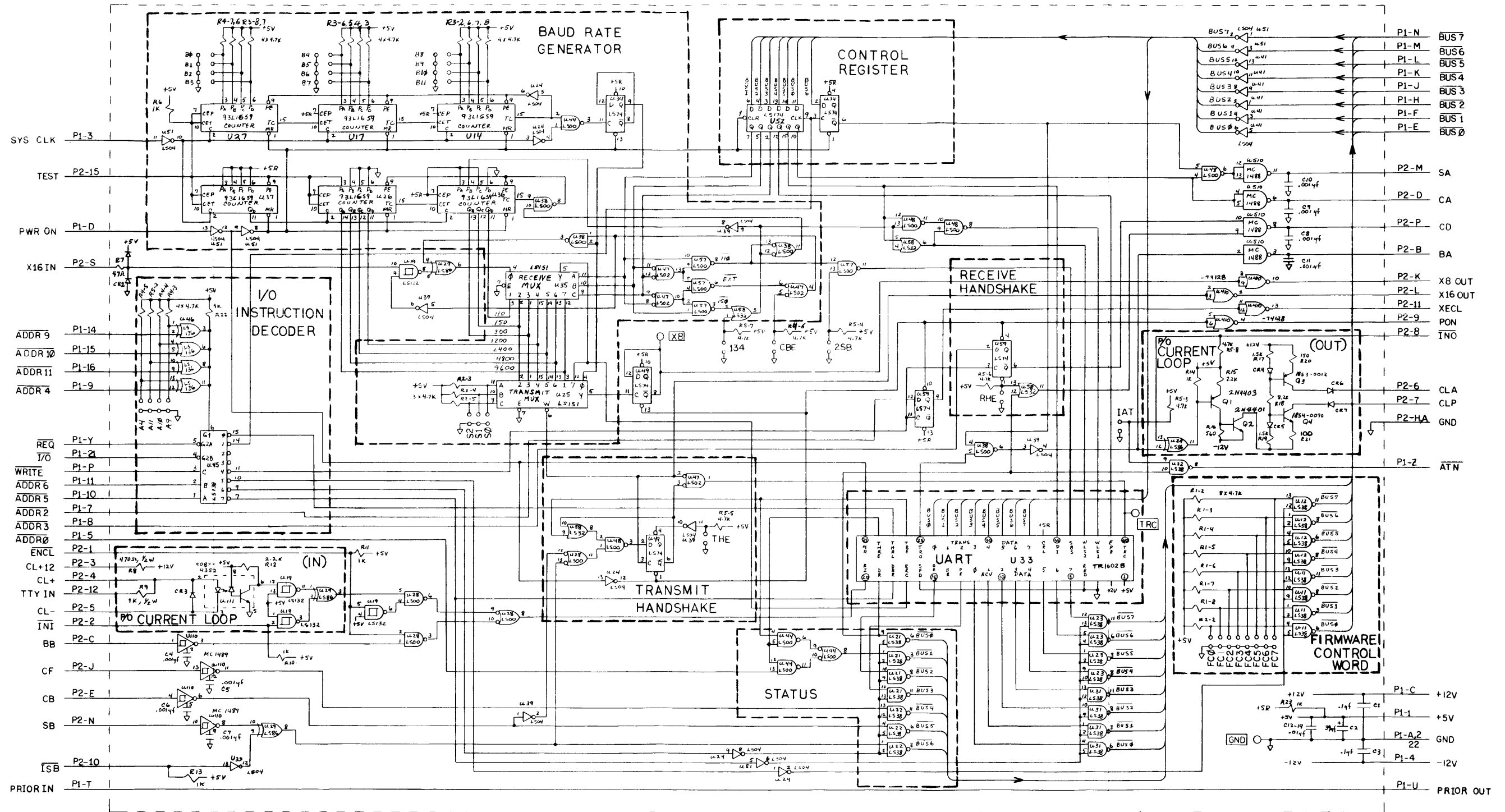c) The CBE Switch must be closed to get a custom baud rate.

Figure 1
GP Asynchronous Data Comm Block Diagram
AUG-01-76   13255-91089

Figure 2
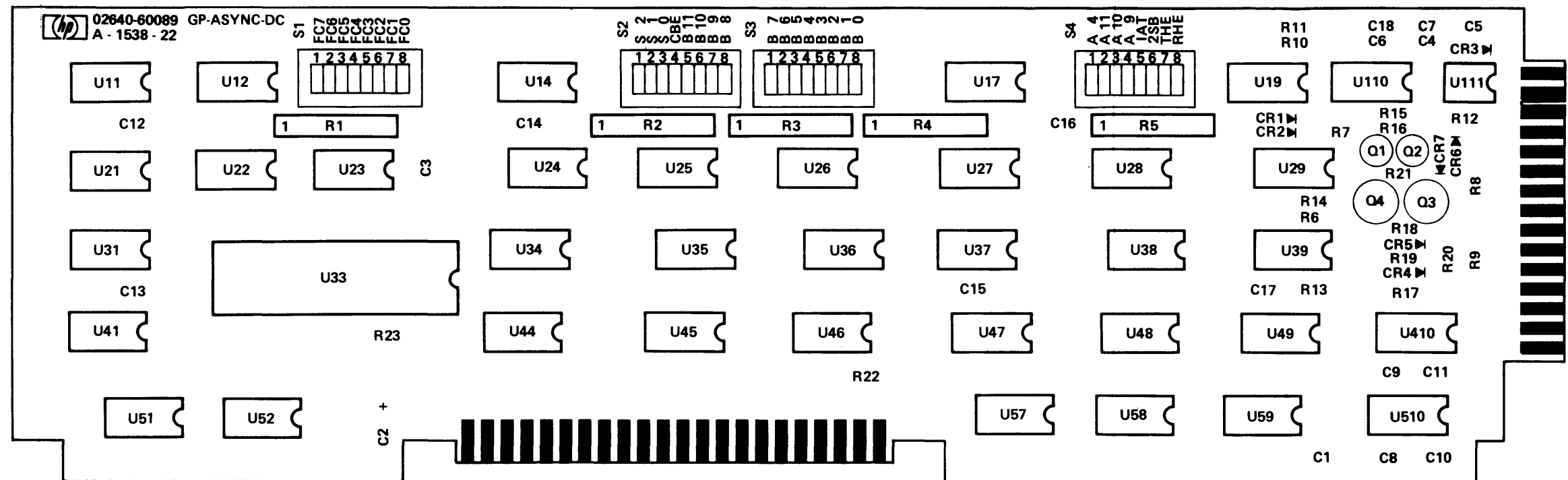GP Asynchronous Data Comm PCA Schematic Diagram
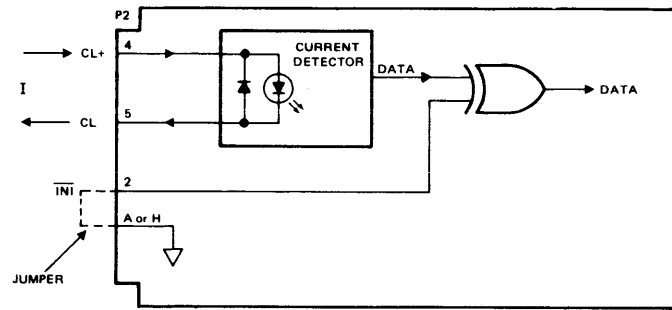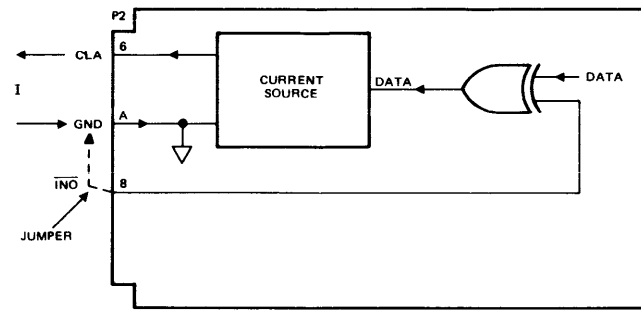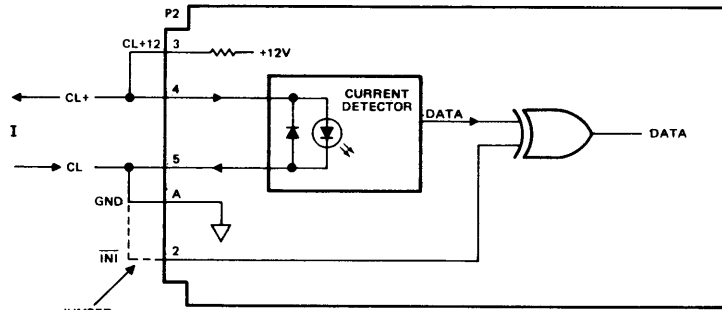AUG-01-76
13255-91089

Figure 3
GP Asynchronous Data Comm PCA
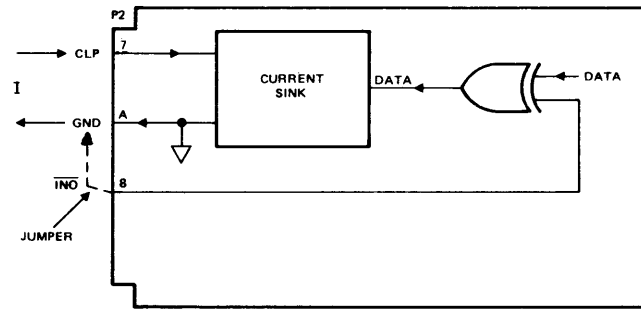Component Location Diagram
AUG-01-76   13255-91089

FLOATING PASSIVE RECEIVER

NON-FLOATING ACTIVE RECEIVER

SOURCING TRANSMITTER

SINKING TRANSMITTER

Figure 4
Current Loop Configuration Diagram
AUG-01-76   13255-91089

Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02645-60003	1	CURRENT LOOP SELF TEST HOOD ASSEMBLY REVISION DATE: 05-14-76	28480	02645-60003
	0624-0098	2	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0099
	1251-0159	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	71785	251-15-30-261
	1251-4339	1	POLARIZING KEY-PC EDGE CONN	28480	1251-4339
	2200-0091	1	SCREW-MACH 4-40 .562-IN-LG PAN-HD-POZI	28480	2200-0091
	2260-0002	1	NUT-HEX-DBL-CHAM 4-40-THD .062-THK	28480	2260-0005
	3030-0009	1	SCREW-SET 6-32 .375-IN-LG SMALL CUP-PT	28480	3030-0009
	8150-2344		WIRE 24AWG BK 300V PVC 7X32 80C	28480	8150-2344
	5040-6003	1	CLAMP	28480	5040-6003
	5040-6072	1	MOUNTING BLOCK	28480	5040-6072
	5040-6086	1	HOOD, CONNECTOR	28480	5040-6086

Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60089	1	G.P. A-SYNC DATA COMM ASSEMBLY DATE CODE: A-1538-22 REVISION DATE:08-13-76	28480	02640-60089
C1	0150-0121	2	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C2	0180-0393	1	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C3	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C4	0160-3456	8	CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C5	0160-3456		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C6	0160-3456		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C7	0160-3456		CAPACITOR-FXD 1000PF +-10% 100CWVDC CER	28480	0160-3456
C8	0160-3456		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C9	0160-3456		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C10	0160-3456		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C11	0160-3456		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C12	0160-2055	7	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C17	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C18	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
CR1	1901-0040	7	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR2	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR3	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR4	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DC-35	28480	1901-0040
CR5	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR6	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DC-35	28480	1901-0040
CR7	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
	0360-0124	3	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
Q1	1853-0271	1	TRANSISTOR PNP 2N4403 SI TO-92 PD=310MW	04713	2N4403
Q2	1854-0467	1	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q3	1853-0012	1	TRANSISTOR PNP 2N2904A SI TO-5 PD=600MW	01295	2N2904A
Q4	1854-0090	1	TRANSISTOR NPN SI TO-39 PD=1W FT=100MHZ	28480	1854-0090
R1	1810-0125	5	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R2	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R3	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R4	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R5	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R6	0683-1025	7	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R7	0683-4705	1	RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R8	0686-4715	1	RESISTOR 470 5% .5W CC TC=0+529	01121	EB4715
R9	0686-1025	1	RESISTOR 1K 5% .5W CC TC=0+647	01121	EB1025
R10	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R11	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R12	0683-2225	2	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
R13	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R14	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R15	0683-2225		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
R16	0683-5615	1	RESISTOR 560 5% .25W FC TC=-400/+600	01121	CB5615
R17	0683-1525	2	RESISTOR 1.5K 5% .25W FC TC=-400/+700	01121	CB1525
R18	0683-8225	1	RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
R19	0683-1525		RESISTOR 1.5K 5% .25W FC TC=-400/+700	01121	CB1525
R20	0683-1515	1	RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
R21	0683-1015	1	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R22	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R23	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
S1	3101-1983	4	SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	81073	76YY2078
S2	3101-1983		SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	81073	76YY2078
S3	3101-1983		SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	81073	76YY2078
S4	3101-1983		SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	81073	76YY2078
U11	1820-1209	6	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U12	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U14	1820-0778	6	IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
U17	1820-0778		IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
U19	1820-1425	1	IC-DIGITAL SN74LS132N TTL LS QUAD 2 NAND	01295	SN74LS132N
U21	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U22	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U23	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U24	1820-1199	4	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U25	1820-1217	2	IC-DIGITAL SN74LS151N TTL LS 8	01295	SN74LS151N

Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			G.P. A-SYNC DATA COMM ASSEMBLY (Cont'd.)		
U26	1820-0778		IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
U27	1820-0778		IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
U28	1820-1197	5	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U29	1820-1211	1	IC-DIGITAL SN74LS86N TTL LS QUAD 2	01295	SN74LS86N
U31	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U33	1820-1219	1	IC-DIGITAL TR1602B TTL*	0026W	TR1602B
U34	1820-1112	3	IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U35	1820-1217		IC-DIGITAL SN74LS151N TTL LS 8	01295	SN74LS151N
U36	1820-0778		IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
U37	1820-0778		IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
U38	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U39	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U41	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS06N
U44	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U45	1820-1216	1	IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
U46	1820-1215	1	IC-DIGITAL SN74LS136N TTL LS QUAD 2	01295	SN74LS136N
U47	1820-1144	1	IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
U48	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U49	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U51	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U52	1820-1196	1	IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
U57	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U58	1820-1208	1	IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U59	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U110	1820-0990	1	IC-DIGITAL MC1489AL DTL QUAD NAND	04713	MC1489AL
U111	1990-0544	1	OPTO-ISOLATOR LED-PDIO/XSTR IF=50MA-MAX	28480	1990-0544
U410	1820-1074	1	IC-DIGITAL SN74128N TTL QUAD 2 NOR	01295	SN74128N
U510	1820-0509	1	IC-DIGITAL MC1488L DTL QUAD LINE	04713	MC1488L
	4330-0145		BEADS, INDIAN	28480	4330-0159
	1200-0185	2	PAD-MTG TO5		

Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60097	1	CURRENT LOOP CABLE ASSEMBLY REVISION DATE: 06-11-76	28480	02640-60097
	0362-0317	4	TERMINAL-CRIMP SPD-FK-FLG #6 22-18-AWG	98410	A-515-06-T
	0624-0098	2	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0099
	1251-0159	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	71785	251-15-30-261
	1251-4339	1	POLARIZING KEY-PC EDGE CONN	28480	1251-4339
	2200-0149	3	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	28480	2200-0149
	2260-0002	1	NUT-HEX-DBL-CHAM 4-40-THD .062-THK	28480	2260-0005
	3030-0009	1	SCREW-SET 6-32 .375-IN-LG SMALL CUP-PT	28480	3030-0009
	8120-1871		CABLE-UNSHLD 22AWG 5-CNDCT JGK-JKT	28480	8120-1893
	5040-6003	1	CLAMP	28480	5040-6003
	5040-6072	1	MOUNTING BLOCK	28480	5040-6072
	5040-6086	1	HOOD, CONNECTOR	28480	5040-6086

Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60098	1	RS232 CABLE ASSEMBLY REVISION DATE: 05-15-76	28480	02640-60098
	0624-0098	2	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0099
	1251-0159	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	71785	251-15-30-261
	1251-0352	1	CABLE BUSHING-CIRC STD CONN	71468	CA18220-6
	1251-2417	1	CONNECTOR 25-PIN M D SERIES	71468	D8C-25P-F0
	1251-3250	7	CONTACT-CONN MALE CRP .04-IN-CONT-SZ	71468	030-1952-000
	1251-3320	1	ACCESSORY-SUBMIN D CONN	71468	018-5008-167
	1251-3328	2	ACCESSORY-SUBMIN D CONN	71785	423-42-22-022
	1251-4339	1	POLARIZING KEY-PC EDGE CONN	28480	1251-4339
	2150-0078	2	WASHER-LK HLCL NO.-4 .115-IN-ID	28480	2190-0078
	2200-0149	1	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	28480	2200-0149
	2200-0757	2	SCREW-MACH 4-40 .688-IN-LG PAN-HD-POZI	28480	2200-0757
	2220-0010	2	SCREW-MACH 4-40 .5-IN-LG FIL-HD-SLT	28480	2220-0010
	2260-0001	2	NUT-HEX-DBL-CHAM 4-40-THD .094-THK	28480	2260-0002
	2260-0002	1	NUT-HEX-DBL-CHAM 4-40-THD .062-THK	28480	2260-0005
	3030-0009	1	SCREW-SET 6-32 .375-IN-LG SMALL CUP-PT	28480	3030-0009
	8120-1857		CABLE-UNSHLD 22AWG 10-CNDCT JGK-JKT	28480	8120-1857
	5040-6003	1	CLAMP	28480	5040-6003
	5040-6072	1	MOUNTING BLOCK	28480	5040-6072
	5040-6086	1	HOOD, CONNECTOR	28480	5040-6086

Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60099	1	RS232 CABLE ASSEMBLY REVISION DATE: 03-13-76	28480	02640-60099
	0624-0098	2	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0099
	1251-0159	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	71785	251-15-30-261
	1251-0352	1	CABLE BUSHING-CIRC STD CONN	71468	CA18220-6
	1251-2416	1	CONNECTOR 25-PIN F D SERIES	71468	DBC-25S-FO
	1251-3252	7	CONTACT-CONN FEM CRP .04-IN-CONT-SZ	71468	030-1953-000
	1251-3320	1	ACCESSORY-SUBMIN D CONN	71468	018-5000-167
	1251-3328	2	ACCESSORY-SUBMIN D CONN	71785	423-42-22-022
	1251-4339	1	POLARIZING KEY-PC EDGE CONN	28480	1251-4339
	2150-0078	2	WASHER-LK HLCL NO.-4 .115-IN-ID	28480	2190-0078
	2200-0149	1	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	28480	2200-0149
	2200-0757	2	SCREW-MACH 4-40 .688-IN-LG PAN-HD-POZI	28480	2200-0757
	2220-0010	2	SCREW-MACH 4-40 .5-IN-LG FIL-HD-SLT	28480	2220-0010
	2260-0001	2	NUT-HEX-DBL-CHAM 4-40-THD .094-THK	28480	2260-0002
	2260-0002	1	NUT-HEX-DBL-CHAM 4-40-THD .062-THK	28480	2260-0005
	3030-0009	1	SCREW-SET 6-32 .375-IN-LG SMALL CUP-PT	28480	3030-0009
	8120-1857		CABLE-UNSHLD 22AWG 10-CNDCT JGK-JKT	28480	8120-1857
	5040-6003	1	CLAMP	28480	5040-6003
	5040-6072	1	MOUNTING BLOCK	28480	5040-6072
	5040-6086	1	HOOD, CONNECTOR	28480	5040-6086