HP 13255

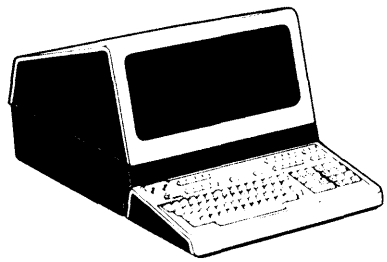
+4K MEMORY MODULE

Manual Part No. 13255-91065

PRINTED

AUG-01-76

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The +4K Memory Module allows modular expansion of 264XX Data Terminal memory capacity. This read/write memory is accessible through the terminal bus and is organized in 4,096 by 8-bit bytes. The module uses dynamic N-Channel MOS RAM chips organized 4K by 1-bit.

2.0 OPERATING PARAMETERS.

A summary of operating paramaters for the +4K Memory Module is contained in tables 1.0 through 5.0.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60065	4K Memory PCA	12.5 x 4.0 x 0.5	0.44
Number of Backplane Slots Required: 1			

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

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Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B ( ) Other:
Restrictions:	Type tested at product level
Failure Rate:	1.634 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 120 mA	@ 200 mA	@ 20 mA	@ mA
			NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 4.915 MHz +/-0.1%

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
W1		
RAM START ADD		
4K	Add 0 to Start Address of Module.	Add 4K to Start Address of Module.
8K	Add 0 to Start Address of Module.	Add 8K to Start Address of Module.
16K	Add 0 to Start Address of Module.	Add 16K to Start Address of Module.
32K	Add 0 to Start Address of Module.	Add 32K to Start Address of Module.
	(All in is Start Address of 0)	(All out is Start Address of 62K)
W2	(Note: This jumper must always be installed for proper operation of the PCA.	
-5	Applies -5V to RAM Array	Disconnects Self Generated -5V from RAM Array and Permits Substitution of a Variable Voltage.

Table 5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-20	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	+12 volt Power Supply
-D		Not Used
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R		Not used
-S	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		Not Used
-W		Not used
-X		Not Used
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z		Not used

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), timing diagrams (figures 3 and 4), component location diagram (figure 5), and parts list (02640-60065) located in the appendix.

The +4K Memory Module consists of 4K bytes of RAM, an address comparator, timing and control logic, refresh logic circuits, and address multiplexing and buffers.

3.1 4K RAM.

3.1.1 The memory portion of the module is comprised of eight 22-pin LSI RAM chips (U21 through U28). Each memory chip has 12 address inputs ($\overline{\text{ADDR0}}$ through $\overline{\text{ADDR11}}$), Data In ($\overline{\text{DI}}$), Data Out (DO), Chip Enable Clock (CE CLOCK), Read/Write control (R/$\overline{\text{W}}$), $\overline{\text{CS}}$ or Chip Select (always low = selected), and four power connections (+12V, +5V, -5V, and GND). The RAM chips have TTL-compatible inputs and outputs with the exception of CE CLOCK (+12V to GND).

3.1.2 A read operation on the memory array requires that R/$\overline{\text{W}}$ (Pin 12) be high and that all address inputs be stable when CE CLOCK (Pin 17) goes high (+12V). Data Out (DO) at Pin 7 is then routed to the terminal bus through bus drivers (U19 and U110). (Refer to figure 3 for read/write timing explanations.)

A write is the same as a memory read operation, except that R/$\overline{\text{W}}$ is low (true) and $\overline{\text{DI}}$ (Pin 6) comes directly from the terminal bus signals ($\overline{\text{BUS0}}$ through $\overline{\text{BUS7}}$). $\overline{\text{DI}}$ must be stable prior to CE CLOCK.

3.2 ADDRESS COMPARATOR.

3.2.1 Jumpers on the +4K Memory PCA are used to specify which 4K partitions out of the possible 64K spaces that the +4K Memory PCA will represent.

3.2.2 Bus address inputs are controlled by $\overline{I/O}$ and $\overline{WRITE}$. The memory module uses the $\overline{WRITE}$ signal to determine read or write access and uses $\overline{I/O}$ to inhibit memory access during input/output operations. Another signal, $\overline{REQ}$, is also used and is equivalent to an execute signal which starts the memory access.

The most significant four address inputs ($\overline{ADDR15}$, $\overline{ADDR14}$, $\overline{ADDR13}$, and $\overline{ADDR12}$) go to the address comparator logic which is comprised of a comparator (U215) and an address configuration jumper network (W1). The remaining 12 address inputs ($\overline{ADDR11}$ through $\overline{ADDR0}$) go to the memory chips through multiplexers (U210 and U211) and four AND gates (U29), which buffer the address lines according to bus rules. When the address comparator logic at U215, Pin 3 (ADDR=) indicates an equal condition (high) and $\overline{I/O}$ is false (high), MODULE SELECT is generated at U313, Pin 11 and a memory access is started as soon as $\overline{REQ}$ is asserted.

3.3 TIMING AND CONTROL LOGIC.

3.3.1 The timing and control logic determines if the module is being accessed by checking the Address Compare signal (ADDR=) and bus control information. If it is, the logic generates all the timing and control signals necessary to access the memory chips and operate the bus signals in response to a memory access.

3.3.2 When the address comparator determines that the +4K Memory Module is selected for a $\overline{MEMORY\ REQUEST}$ (U213, Pin 3) the J-K flip-flops (SFF0 and SFF1) begin a sequence which generates the timing for the memory read or write ($R/\overline{W}$) signal at U214, Pin 11.

The SFF0 and SFF1 flip-flops determine the sequence of events in a memory access. They decode three states and create the timing for the terminal bus signal $\overline{\text{WAIT}}$ at U214, Pin 6. After $\overline{\text{MEMORY REQUEST}}$ is asserted, two states are required to bring $\overline{\text{WAIT}}$ high again (SFF0 and SFF1 = 00, 10) and the state flip-flops stay in the last state (SFF's = 11) until $\overline{\text{MEMORY REQUEST}}$ goes low again.

The remaining logic determines when $\overline{\text{R/W}}$ (U214, Pin 11) is to be low for a write operation and when data is gated to the bus on memory reads.

3.4 REFRESH LOGIC.

3.4.1 Dynamic MOS memories require pseudo memory cycles periodically so that the internal data storage circuits do not lose data. The refresh logic performs this function by initiating pseudo read cycles (data not gated to the bus) when the +4K Memory Module is not busy. Refresh is accomplished by performing 64 pseudo read cycles (every 2 milliseconds) to the memory chips. The PCA does this in a cycle-stealing manner by initiating one refresh cycle every 32 microseconds when the memory is not being accessed. The least significant six bits of the address are derived from the refresh address counter (U111 and U112) which is gated to the memory array during a refresh cycle.

3.4.2 Two additional counters (U314 and U315) generate the 32-microsecond interval which sets the Refresh Request flip-flop at U114, Pin 8. One counter is a divide-by-10; the other is a divide-by-16 which derives the 32-microsecond pulse at U315, Pin 15 after 160 counts of the 4.915 MHz System Clock.

Three flip-flops then control the timing necessary to refresh one row of the memory chip: REFRESH REQUEST (U114, Pin 8), REF ADDRESS (U212, Pin 8), and REFRESH IN PROGRESS (U212, Pin 6).

A refresh cycle begins when the Refresh Request flip-flop at U114, Pin 8 is set. (Refer to figure 4 for refresh cycle timing explanations.) If a memory access is not in progress, then the Refresh Address flip-flop is set on the next clock rising edge (approximately 100 nanoseconds later). The Refresh In Progress flip-flop is set which

begins a memory cycle at U213, Pin 6, and turns off the Refresh Request flip-flop. The state flip-flops count normally until SFF1 is set. Flip-flop SFF1 turns off the CE CLOCK immediately (a 400-nanosecond pulse total). Then the Refresh Address flip-flop changes on the next positive clock edge, followed by the Refresh In Progress flip-flop on the next negative edge. This causes the bus address to be restored and the refresh row counter to be incremented by one at U112, Pin 2. Finally, SFF0 and SFF1 go off, finishing a refresh cycle.

If a memory access to the +4K Memory Module begins during a refresh cycle, $\overline{\text{WAIT}}$ will immediately go low (true) and the refresh will be completed. This will be followed immediately by a normal memory read or write operation. If the Refresh Request flip-flop goes high during a memory access, the refresh will be initiated immediately after the memory read/write is finished.

3.5 ADDRESS MULTIPLEXING AND BUFFERS. When a refresh operation is in progress, the refresh address counter (U111 and U112) is gated to the six least significant bits of the memory array by multiplexers U210 and U211. If a refresh is not in progress, the normal bus address is gated to the memory chips. One-half of U211 and U29 set the most significant address bits to a low during refresh and buffer the bus address during a memory request. It should be noted that regular TTL address multiplexers are used at U29, U210, and U211 and therefore it is necessary to limit the number of +4K Memory Modules that may be placed in a terminal to seven.

4.0 TEST POINTS. Several test points are available on the PCA for examaning critical signals and for automatic test purposes.

- o CE CLK - Chip Enable Clock
- o RFRST - Refresh Restart resets all refresh counters and logic to "0"
- o RFDIS - Refresh Disable presets timing counters to 158 count (one count away from 32 microsecond pulse, which helps shorten automatic testing)
- o GND - Ground
- o -5 - This test point provides a convenient means for varying the -5 volt bias during initial test of the RAMs.

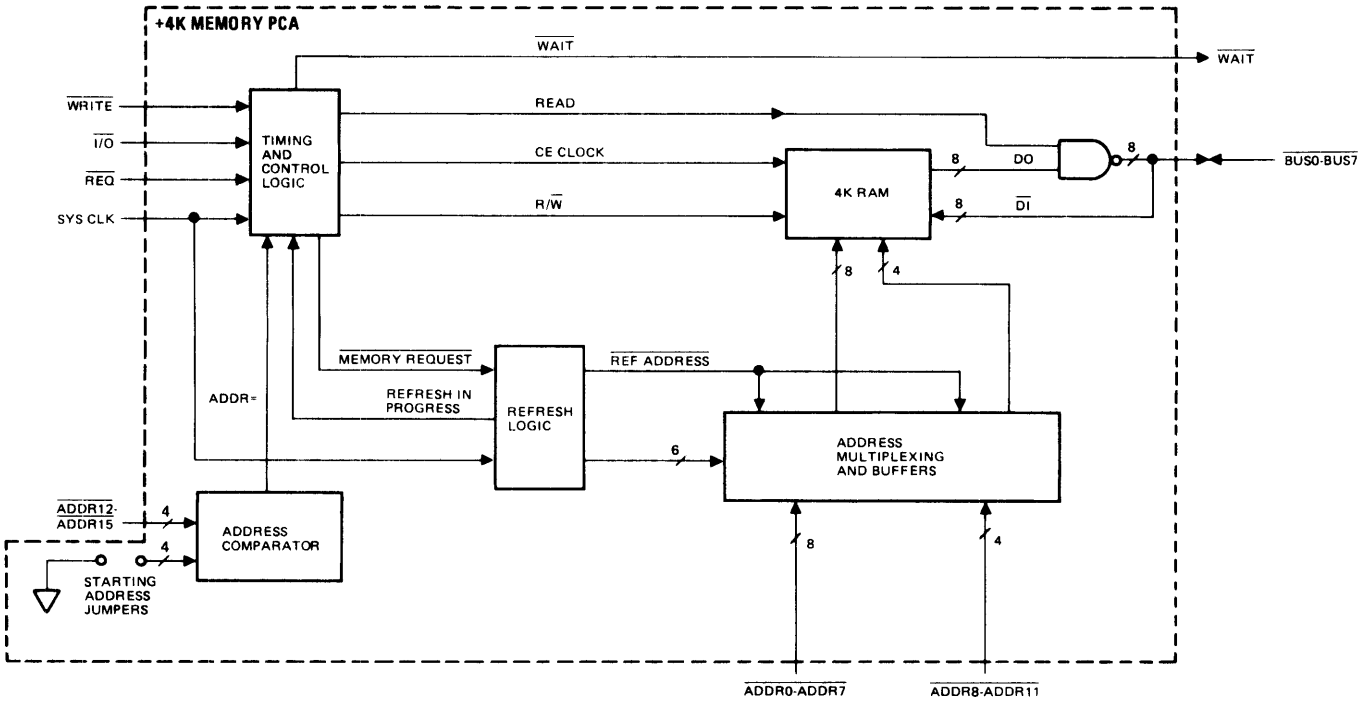

Figure 1
+4K Memory Block Diagram
AUG-01-76 13255-91065

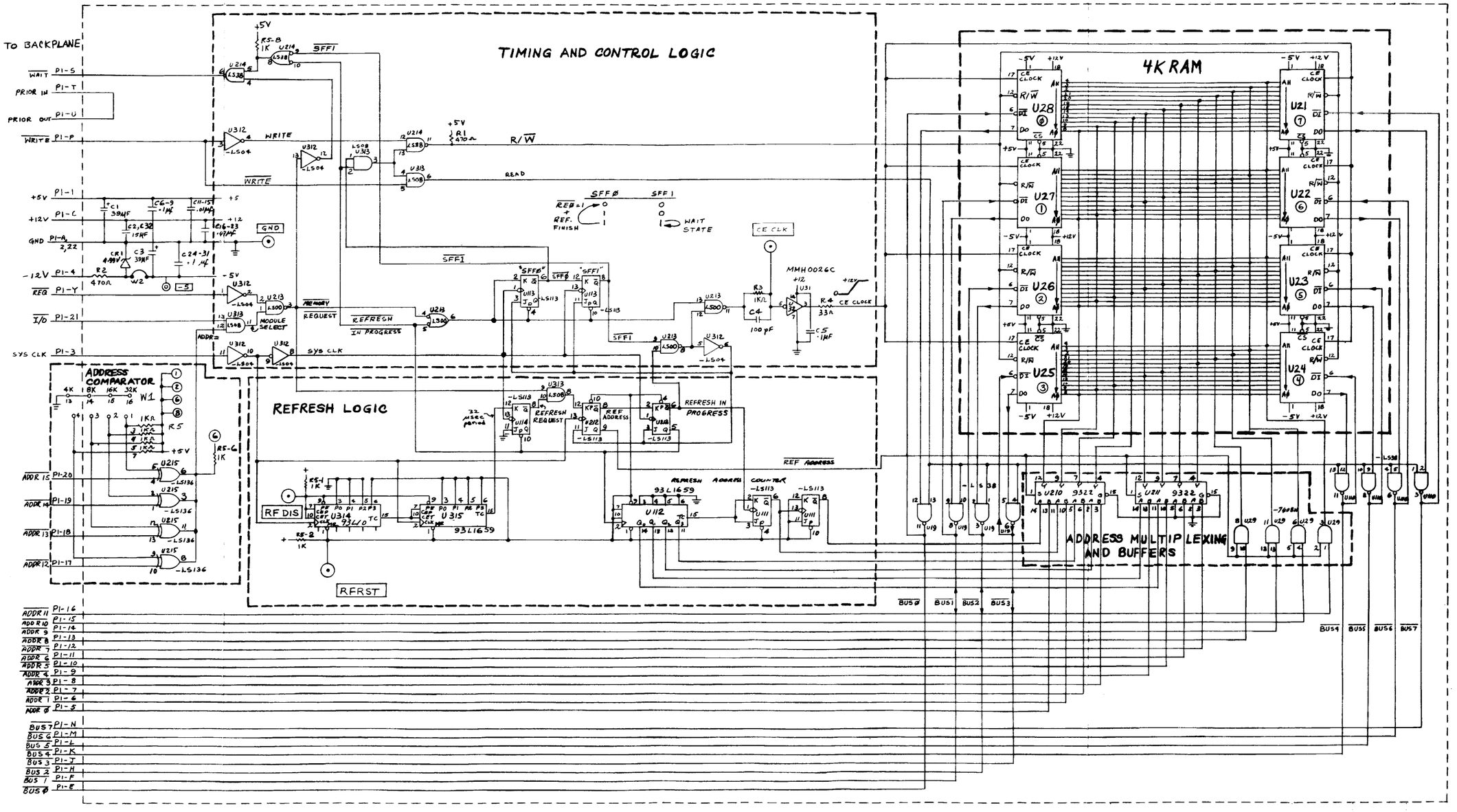

Figure 2
+4K Memory PCA Schematic Diagram
AUG-01-76 13255-91065

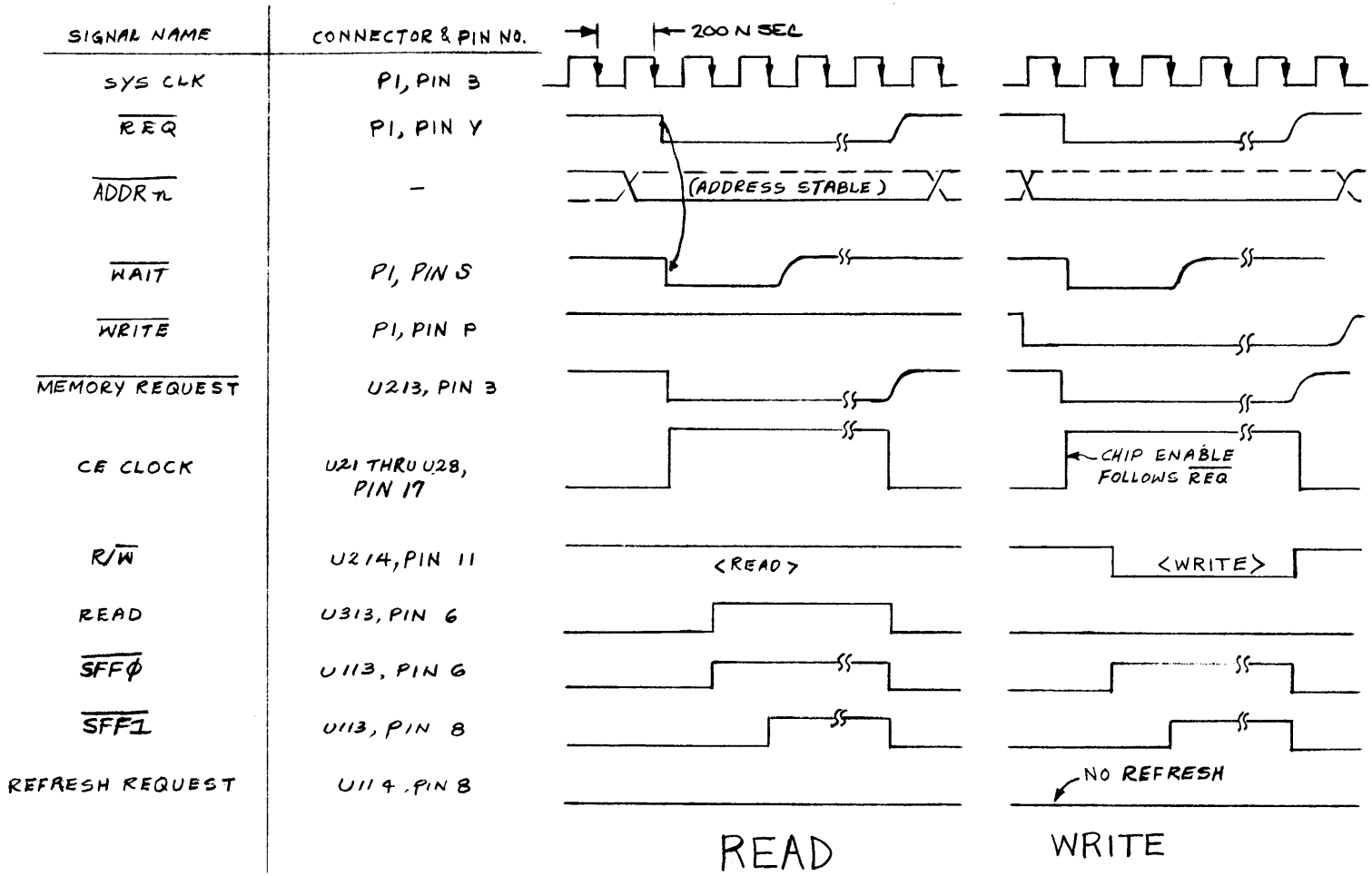

Figure 3
+4K Memory Read/Write Timing Diagram
AUG-01-76 13255-91065

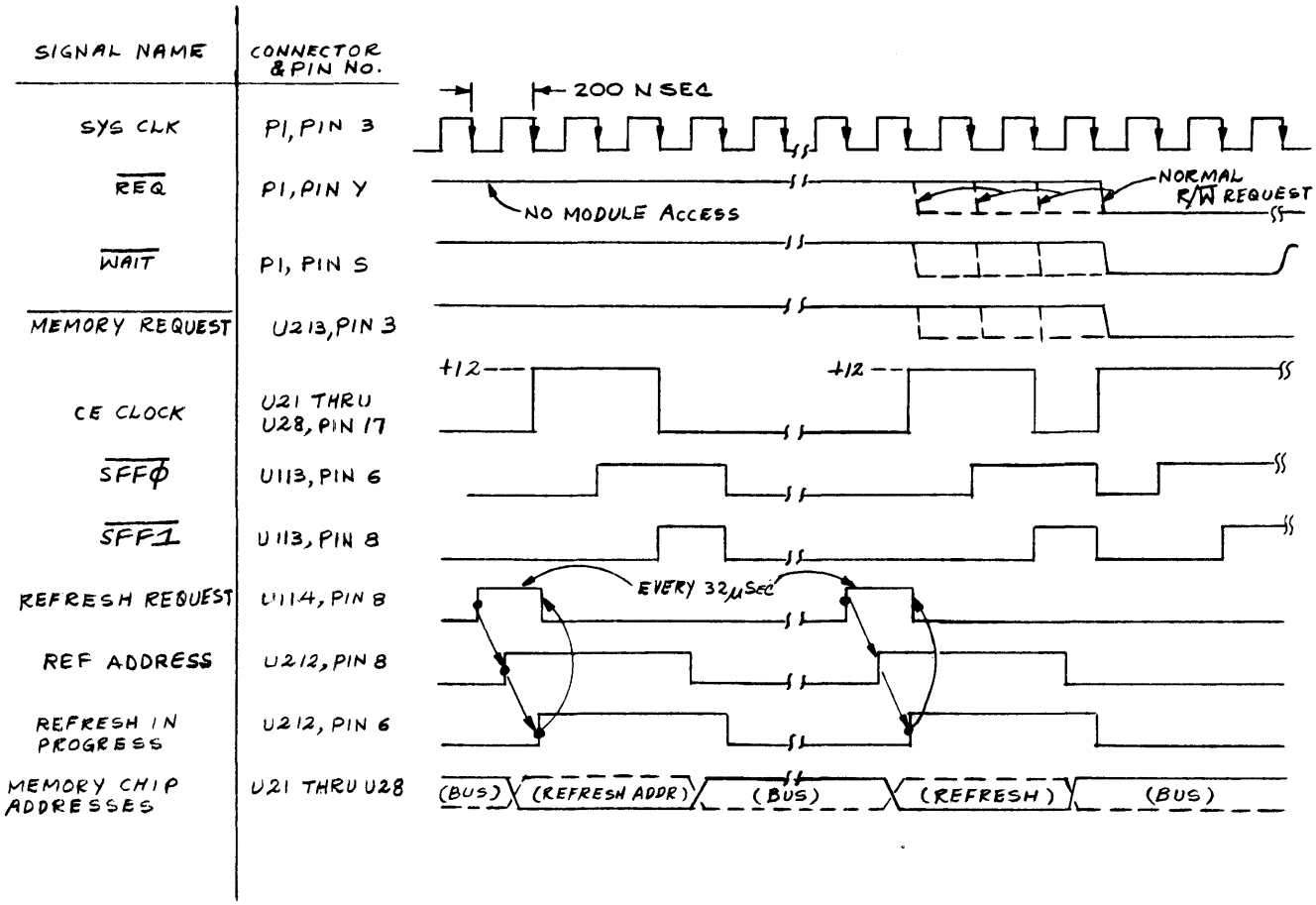

Figure 4
+4K Memory Refresh Timing Diagram
AUG-01-76 13255-91065

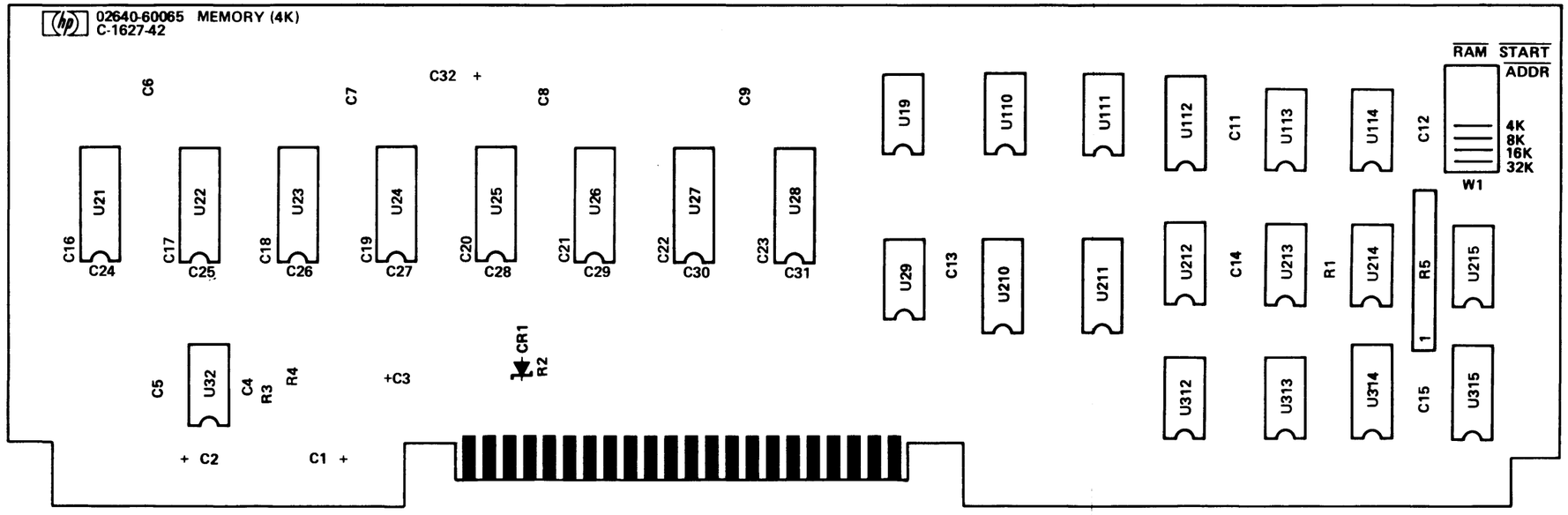

Figure 5
+4K Memory PCA Component Location Diagram
AUG-01-76 13255-91065

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60065	1	4K MEMORY ASSEMBLY DATE CODE: C-1627-42 REVISION DATE: 06-30-76	28480	02640-60065
C1	0180-0393	2	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0180-1746	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C3	0180-0393		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C4	0160-2204	1	CAPACITOR-FXD 100PF +-5% 300WVDC MICA	28480	0160-2204
C5	0150-0121	13	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C6	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C7	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C8	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C9	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C11	0160-2055	5	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-0174	8	CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
C17	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
C18	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
C19	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
C20	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
C21	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
C22	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
C23	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
C24	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C25	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C26	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C27	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C28	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C29	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C30	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C31	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C32	0180-1746		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
CR1	1902-3092	1	DIODE-ZNR 4.99V 2% DO-7 PD=.4W TC=-.012%	04713	SZ 10939-96
E1	0360-0124	4	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E4	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
J1	1251-0697	2	CONNECTOR-SGL CONT SKT .022-IN-BSC-SZ	22526	75540-001
J2	1251-0697		CONNECTOR-SGL CONT SKT .022-IN-BSC-SZ	22526	75540-001
R1	0683-4715	2	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R2	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R3	0683-1025	1	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R4	0683-3305	1	RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
R5	1810-0121	1	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
U19	1820-1209	3	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U21	5080-9785	8	4K RAM 22-PIN HR	28480	5080-9785
U22	5080-9785		4K RAM 22-PIN HR	28480	5080-9785
U23	5080-9785		4K RAM 22-PIN HR	28480	5080-9785
U24	5080-9785		4K RAM 22-PIN HR	28480	5080-9785
U25	5080-9785		4K RAM 22-PIN HR	28480	5080-9785
U26	5080-9785		4K RAM 22-PIN HR	28480	5080-9785
U27	5080-9785		4K RAM 22-PIN HR	28480	5080-9785
U28	5080-9785		4K RAM 22-PIN HR	28480	5080-9785
U29	1820-0511	1	IC-DIGITAL SN7408N	01295	SN7408N
U32	1820-1288	1	IC-DIGITAL MMH0026CL TTL/MOS 1 CLOCK	04713	MMH0026CL
U110	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U111	1820-1213	4	IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U112	1820-0778	2	IC-DIGITAL 93L16DC TTL L 8IN SYNCHRO	07263	93L16DC
U113	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U114	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U210	1820-0616	2	IC-DIGITAL 9322DC TTL QUAD	07263	9322DC
U211	1820-0616		IC-DIGITAL 9322DC TTL QUAD	07263	9322DC
U212	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U213	1820-1197	1	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U214	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U215	1820-1215	1	IC-DIGITAL SN74LS136N TTL LS QUAD 2	01295	SN74LS136N
U312	1820-1199	1	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U313	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U314	1820-0669	1	IC-DIGITAL 93L10DC TTL L BCD SYNCHRO	07263	93L10DC

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			4K MEMORY ASSEMBLY (CONT'D.)		
U515	1820-0778		IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
	1200-0482	1	SOCKET-IC 16-CONT DIP-SLDR	91506	516-AG11D
W1A	1258-0124	5	PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1B	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1C	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1D	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W2	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1