

**HP E2409B
Intel 80286
Preprocessor Interface**

User's Guide

HP E2409B Intel 80286 Preprocessor Interface User's Guide

**for the HP 1650A, HP 1650B, HP 16510A, HP 16510B, HP 1652B,
HP 16511B, HP 16540/16541A,D, and HP 16550A Logic Analyzers**



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Introduction

The HP E2409B Preprocessor Interface, when installed in the HP 10269C General Purpose Probe Interface, provides a complete interface between an 80286 target system and the HP 1650A, HP 1650B, HP 16510A, HP 16510B, HP 1652B, HP 16511B, HP 16540/16541A,D, and HP 16550A Logic Analyzers. The preprocessor interface connects the signals from the 80286 target microprocessor to the logic analyzer inputs and generates all status and clock signals required by the logic analyzer for inverse assembly of the 80286 instruction set.

The HP E2409B Preprocessor Interface operates in two modes: state and timing. In the state mode, all bus cycles, including prefetches, are sent to the logic analyzer as they occur. All coprocessor (80287) cycles on the local bus will also be captured.

In the timing mode, all signals excepts CLK are sent to the logic analyzer for timing relationship measurements. In this mode the signals are not latched, to preserve the timing relationship between signals.

The 80286 configuration software on the flexible disk sets up the format specification of the logic analyzer for compatibility with the 80286 microprocessor. It also loads the inverse assembler routine for obtaining displays of 80286 data in assembly language mnemonics.

Logic Analyzers Supported

The following logic analyzers are supported by the HP E2409B Preprocessor Interface:

HP 1650A, HP 1650B, HP 16510A, HP 16510B, and HP 1652B

These logic analyzers provide 1 k of memory depth with either 80 channels of 35 MHz state analysis (25 MHz state analysis for the HP 1650A or HP 16510A) or 80 channels of 100 MHz timing analysis.

HP 16511B

This logic analyzer combination provides 1 k of memory depth with either 160 channels of 35 MHz state analysis, or 80 channels of 35 MHz state analysis and 80 channels of 100 MHz timing analysis.

HP 16540A,D with one or two HP 16541A,D Expansion Cards

This logic analyzer combination provides 4 k of memory depth with up to either 64 or 112 channels of 100 MHz state or timing analysis.

HP 16550A

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz of timing analysis. The logic analyzer will also support various combinations of mixed state/timing analysis.

How to Use This Manual

This manual is organized into three chapters and one appendix:

- Chapter 1 explains how to install and configure the HP E2409B Preprocessor Interface for state or timing analysis with the supported logic analyzers.
- Chapter 2 provides reference information on the format specification and symbols configured by the HP E2409B software. It also provides information about the inverse assembler and status encoding.
- Chapter 3 provides additional reference information including the characteristics and interface requirements for the HP E2409B Preprocessor Interface. It also contains information on servicing.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

Setting Up the HP E2409B

Introduction

This chapter explains how to install and configure the HP E2409B Preprocessor Interface for state or timing analysis with the supported logic analyzers.

Duplicating the Master Disk

Before you use the HP E2409B software, make a duplicate copy of the HP E2409B master disk. Then store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidentally deleted.

To make a duplicate copy, use the Duplicate Disk operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

Equipment Supplied

The HP E2409B Preprocessor Interface and Inverse Assembler consists of the following equipment:

- The preprocessor interface hardware, which includes the preprocessor interface circuit board and cable assembly.
 - The inverse assembly software on a 3.5-inch disk.
 - This user's guide.
-

Minimum Equipment Required

The minimum hardware for analysis of an 80286 target system consists of the following equipment:

- An HP 1650A, HP 1650B, HP 16510A, HP 16510B, HP 1652B, HP 16511B, HP 16540/16541A,D or HP 16550A Logic Analyzer.
- The HP 10269C General Purpose Probe Interface, which connects the preprocessor interface to the logic analyzer.
- The 80286 Preprocessor and Inverse Assembler (HP E2409B).

Available Options

The following options are available for the HP E2409B Preprocessor Interface:

- Option 1CB which is a PLCC (Plastic Leaded Chip Carrier) adapter for the preprocessor interface cable.
- Option 1CA which is an LCC (Leaded Chip Carrier) adapter for the preprocessor interface cable.



You must specify an option when ordering the HP E2409B to receive either or both options. Otherwise, the preprocessor interface will only work with PGA (Pin Grid Array) sockets.

Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the HP E2409B Preprocessor Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

1. Install the 80286 Preprocessor Interface (HP E2409B) into the HP 10269C General Purpose Probe Interface (see page 1-4).



To prevent equipment damage, remove power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

2. Connect the HP E2409B Preprocessor Interface cable to the target system (see page 1-6).
3. Plug the logic analyzer probes into the HP 10269C General Purpose Probe Interface as listed in tables 1-1 or 1-2.
4. Set the State/Timing switch of the preprocessor interface to the appropriate position (see page 1-12).
5. Configure the logic analyzer by loading the appropriate file from the disk (see page 1-14). The configuration files are listed below the logic analyzers in tables 1-1 and 1-2.

Table 1-1. Connections and Configuration Files for HP 16540/16541A,D Logic Analyzers

HP 16540A,D with one HP 16541A,D card (state)	HP 16540A,D with one HP 16541A,D card (timing)	HP 16540A,D with two HP 16541A,D cards (state or timing)	(Into)	HP 10269C Connector
Master Card, Pod 1	no connection	Master Card, Pod 1		1**
* Exp. Card 1, Pod 1	* Exp. Card 1, Pod 1	* Exp. Card 1, Pod 1		2***
* Exp. Card 1, Pod 2	* Exp. Card 1, Pod 2	* Exp. Card 1, Pod 2		3***
no connection	* Exp. Card 1, Pod 3	* Exp. Card 1, Pod 3		4****
no connection	Master Card, Pod 1	* Exp. Card 2, Pod 1		5****
Configuration Files				
E80286S	E80266T1	E80286S (state) E80286T (timing)		
<p>Two HP 16541A,D Expander Cards allows the user to switch from state to timing without having to change connections. * For the HP 16541A,D Expander Cards, Exp. Card 1 refers to the physically highest HP 16541A,D card in your frame, and Exp. Card 2 refers to the next physically highest HP 16541A,D card (see figure 1-1).</p>				

Table 1-2. Connections and Configuration Files for Other Logic Analyzers

HP 16511B Logic Analyzer	HP 16550A Logic Analyzer	All Other Logic Analyzers	(Into)	HP 10269C Connector
Lower Card, Pod 1	Pod 1	Pod 1		1**
Lower Card, Pod 2	Pod 3	Pod 2		2***
Lower Card, Pod 3	Pod 4	Pod 3		3***
Lower Card, Pod 4	Pod 5	Pod 4		4****
Lower Card, Pod 5	Pod 6	Pod 5		5****
Configuration Files				
D80286S (state)	F80286S (state)	C80286S (state)		
D80286T (timing)	F80286T (timing)	C80286T (timing)		

** This connector is only used for state analysis.

*** These connectors are used for both state and timing analysis.

**** These connectors are only used for timing analysis.

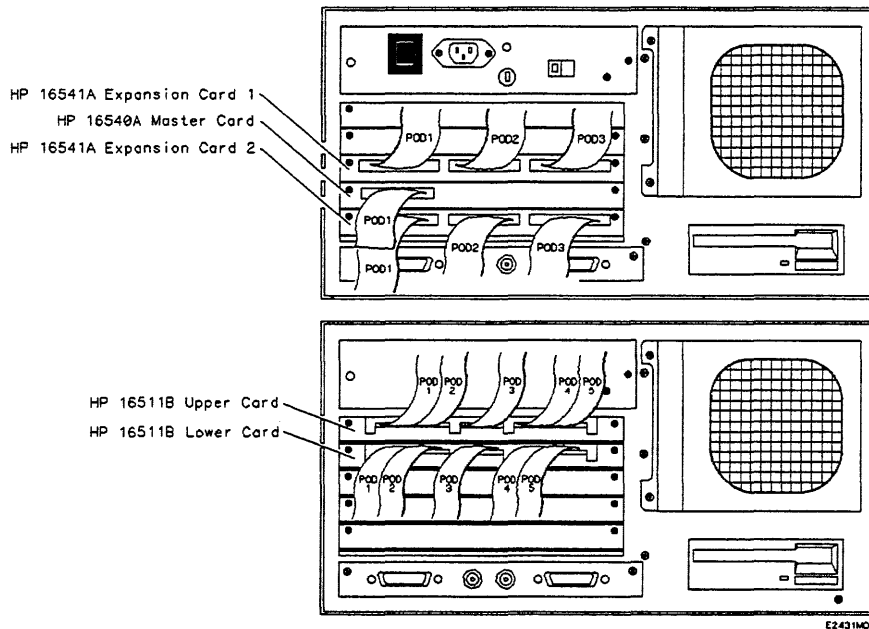


Figure 1-1. Logic Analyzer Card Locations
 (relative locations, actual slots used may vary)

Installing the HP E2409B in the HP 10269C

The HP 10269C General Purpose Probe Interface routes the signals from the HP E2409B Preprocessor Interface and provides the correct mechanical connections for the logic analyzer probes. To install the HP E2409B Preprocessor Interface board on the underside of the HP 10269C General Purpose Probe Interface:

1. Insert the metal tabs of the preprocessor interface board in the slots of the probe interface as shown in figure 1-2.
2. Connect the two internal cables of the probe interface to the preprocessor interface board.
3. Gently fold the preprocessor interface board into the probe interface. Then fasten the cable end of the preprocessor interface board to the probe interface with the two captive screws on the preprocessor interface board.

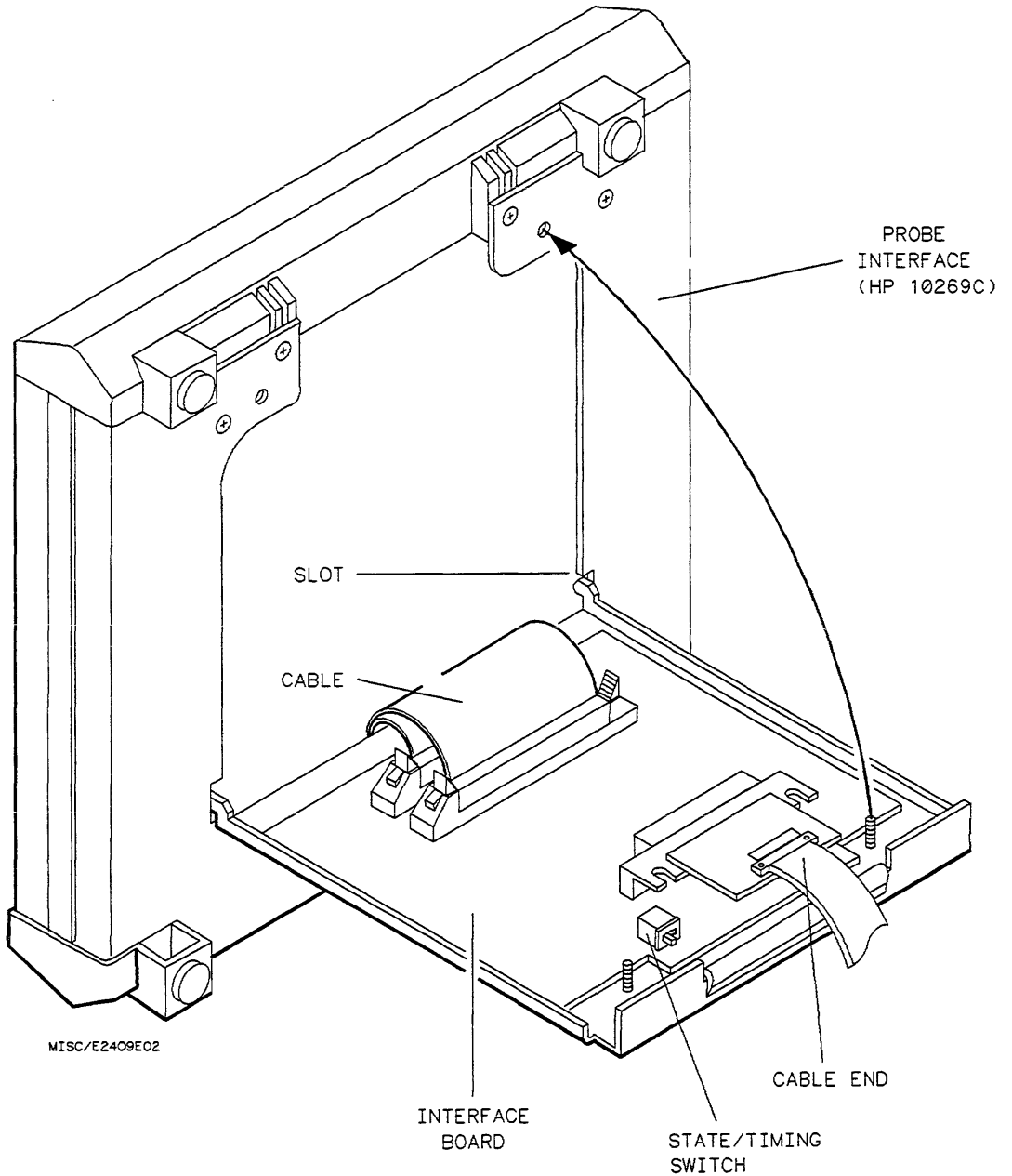


Figure 1-2. Installing the HP E2409B in the HP 10269C

Connecting to the Target System

The microprocessor connector on the preprocessor cable will connect directly to a PGA socket on the target system or, with the appropriate option, connect to a PLCC (page 1-8) or LCC (page 1-10) style socket. Option 1CB is the PLCC adapter and option 1CA is the LCC adapter.

Caution

To prevent equipment damage, remove power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

Note

PROTECT AGAINST STATIC DISCHARGE

The preprocessor interface contains devices that are susceptible to damage by Electrostatic Discharge (ESD). Therefore, precautionary measures should be taken before handling the microprocessor connector attached to the end of the interface cable. If precautionary measures are not taken, the internal components of the preprocessor interface may be damaged by static electricity.

Installing the Interface Cable in a PGA Socket Assembly

To connect the microprocessor connector to the target system using a PGA socket assembly:

1. Remove the 80286 microprocessor from the microprocessor socket on the target system.
 2. Store the microprocessor in a protected environment.
-

Caution

Serious damage to the target system or preprocessor interface can result from incorrect connection. Take care to note the position of pin 1 on the interface connector and the target system socket prior to inserting the connector in the socket. Also, take care to align the preprocessor connector with the target system socket so that all microprocessor pins are making contact.

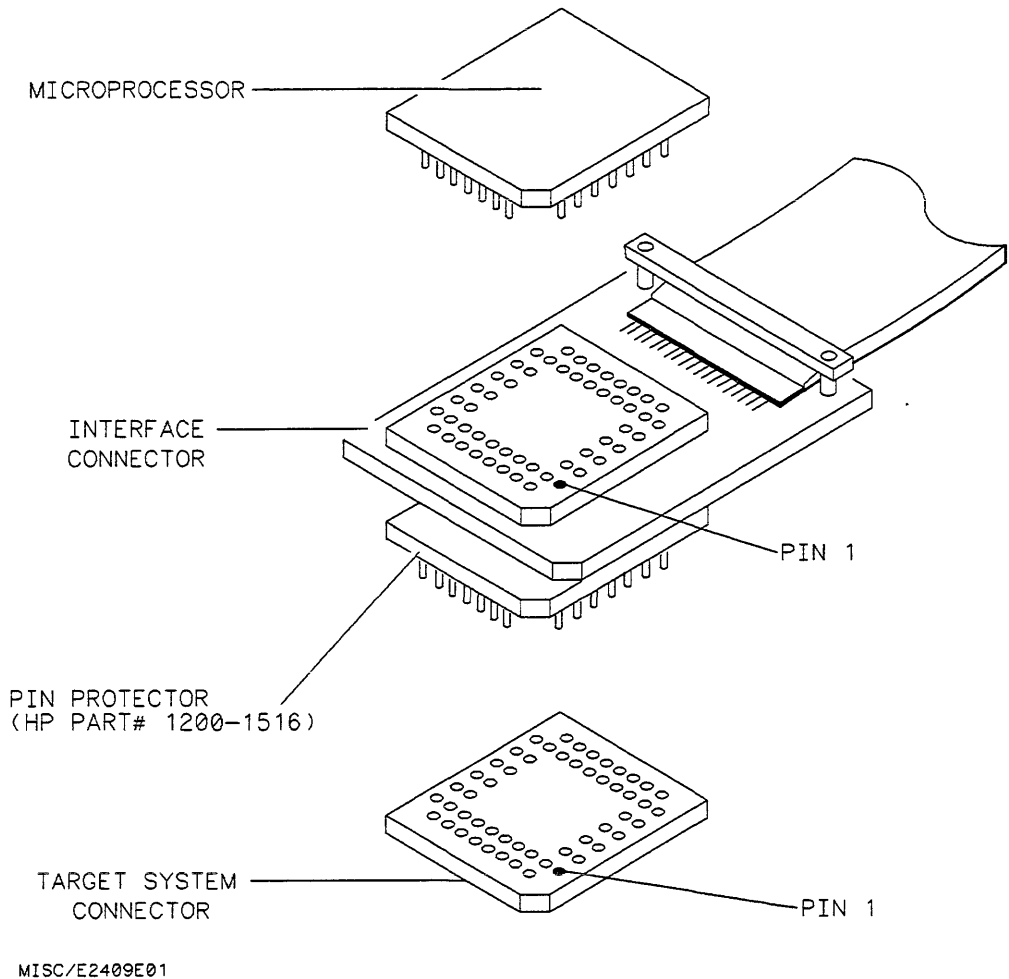


Figure 1-3. Installing the Cable in a PGA Socket

3. Place the interface connector, attached to the end of the cable from the preprocessor interface, in the microprocessor socket on the target system (see figure 1-3).
4. Noting the position of pin 1, place the microprocessor in the socket on the target end of the preprocessor cable.

Installing the Interface Cable in a PLCC Socket Assembly

The PLCC adapter (option 1CB, which includes the PLCC extractor tool) is designed to plug into a standard PLCC socket assembly. To connect the microprocessor connector to a PLCC target system:

1. Using the PLCC extractor tool, remove the 80286 microprocessor from the microprocessor socket on the target system.
-

Caution

Be careful not to damage the PLCC socket or 80286 microprocessor when removing the microprocessor from the socket.

2. Store the microprocessor in a protected environment.
 3. Noting the position of pin 1, place the PLCC adapter in the microprocessor socket on the target system (see figure 1-4).
-

Caution

Serious damage to the target system or preprocessor interface can result from incorrect connection. Take care to note the position of pin 1 on the interface connector, PLCC adapter, and target system socket prior to inserting the connector in the socket. Also, take care that all microprocessor pins are making contact.

4. Place the interface connector, attached to the end of the cable from the preprocessor interface, in the PLCC adapter socket.
 5. Using one of the following methods, install the microprocessor:
 - If a PGA style 80286 is available, note the position of pin 1 and place the PGA style 80286 microprocessor in the socket on the target end of the preprocessor cable.
 - If a PGA style 80286 microprocessor chip is unavailable, a PLCC style device can be installed by first installing the PLCC socket, supplied with option 1CB. Note the position of pin 1 and install the socket in the socket on the target end of the preprocessor cable. Then install the PLCC style 80286 microprocessor in the PLCC socket (see figure 1-4).
-

Note

For PLCC style microprocessors, the PLCC socket adds capacitance to the circuit, but should not affect microprocessor performance.

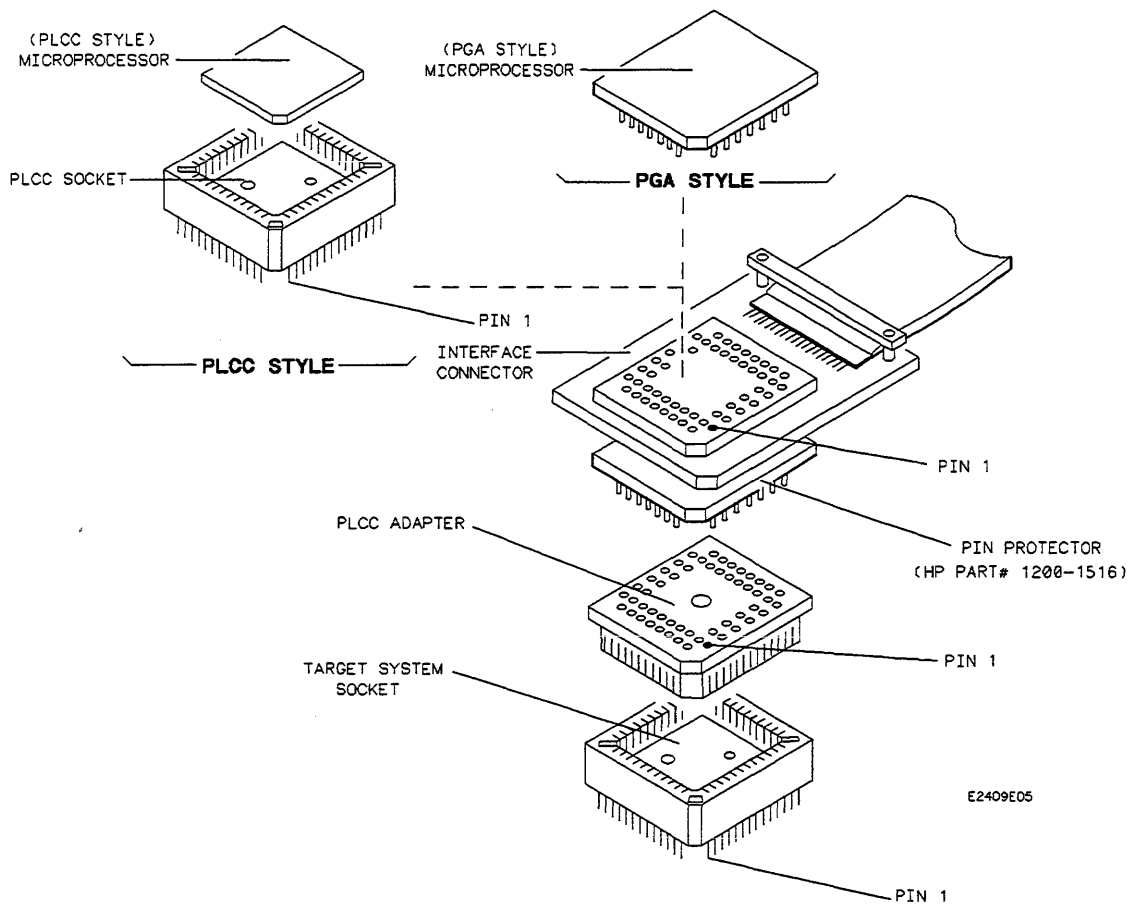


Figure 1-4. Installing the Cable in a PLCC Socket

Installing the Interface Cable in an LCC Socket Assembly

The LCC adapter (option 1CA) is designed to plug into a standard LCC socket assembly. To connect the microprocessor connector to a target system using an LCC socket assembly:

1. Remove the 80286 microprocessor from the target system.
2. Store the microprocessor in a protected environment.
3. Noting the position of pin 1, place the LCC adapter in the microprocessor socket on the target system (see figure 1-5).

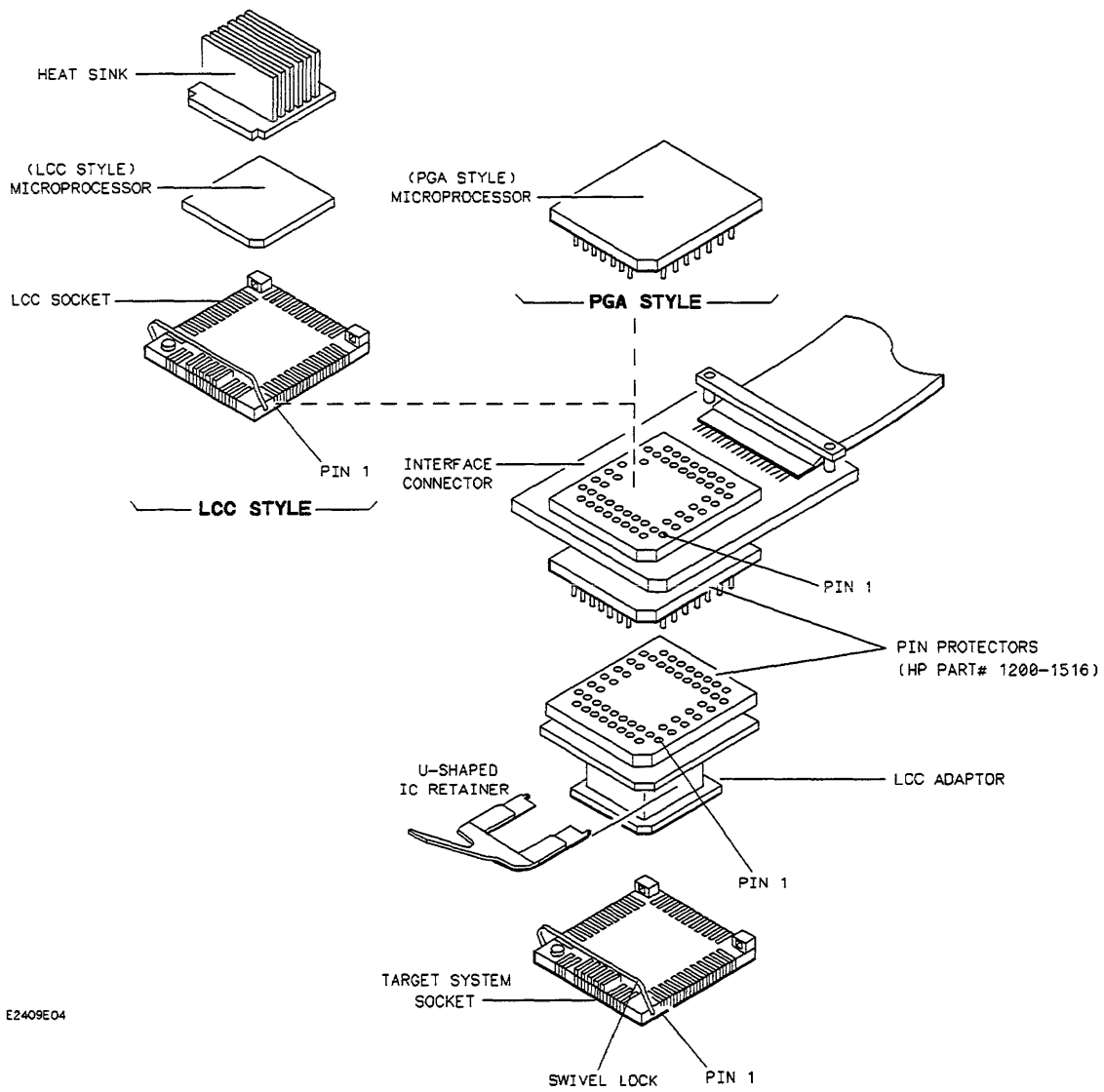


Serious damage to the target system or preprocessor interface can result from incorrect connection. Take care to note the position of pin 1 on the interface connector, LCC adapter, and target system socket prior to inserting the connector in the socket. Also, take care that all microprocessor pins are making contact.

4. Install the U-shaped IC retainer on top of the bottom board of the LCC adapter. Then secure it by swinging the swivel lock up and over the end of the U-shaped IC retainer.
5. Place the interface connector, attached to the end of the cable from the preprocessor interface, in the LCC adapter socket.
6. Using one of the following methods, install the microprocessor:
 - If a PGA style 80286 is available, noting the position of pin 1, place the PGA style 80286 microprocessor in the socket on the target end of the preprocessor cable.
 - If a PGA style 80286 is unavailable, an LCC style device can be installed by first installing the LCC socket (option 1CA). Note the position of pin 1 and install the socket in the socket on the target end of the preprocessor cable. Then install the LCC style 80286 in the LCC socket. Install the heat sink, supplied with the option 1CA, in place of the U-shaped IC retainer that goes on top of the microprocessor. Secure the heat sink by swinging the swivel lock up and over the end of the heat sink.



For LCC style microprocessors, the LCC socket adds capacitance to the circuit, but should not affect microprocessor performance.



E2409E04

Figure 1-5. Installing the Cable in an LCC Socket

Connecting to the HP 10269C

Connect the logic analyzer pods to the HP 10269C General Purpose Probe Interface as shown in tables 1-1 or 1-2 (page 1-3), according to which logic analyzer you are using. For the HP 16540A,D with one HP 16541A,D Expander Card, the connections also depend on whether you are making state or timing measurements.

Setting the State/Timing Switch

The State/Timing switch of the HP E2409B Preprocessor Interface board allows you to configure the HP E2409B for either state or timing analysis. This switch is accessed through the slot in the metal cover for the interface cable (see figure 1-6). For more information on the State/Timing switch, refer to the section "Interface Description" in chapter 3.

State Analysis

To use the preprocessor interface for state analysis, set the State/Timing switch to STATE (away from the cable). Ensure that you load the appropriate state configuration file.

Timing Analysis

To use the preprocessor interface for timing analysis, set the State/Timing switch to TIMING (toward the cable). Ensure that you load the appropriate timing configuration file.



The State/Timing switch is labeled on the bottom cover of the HP E2409B assembly for easier access.

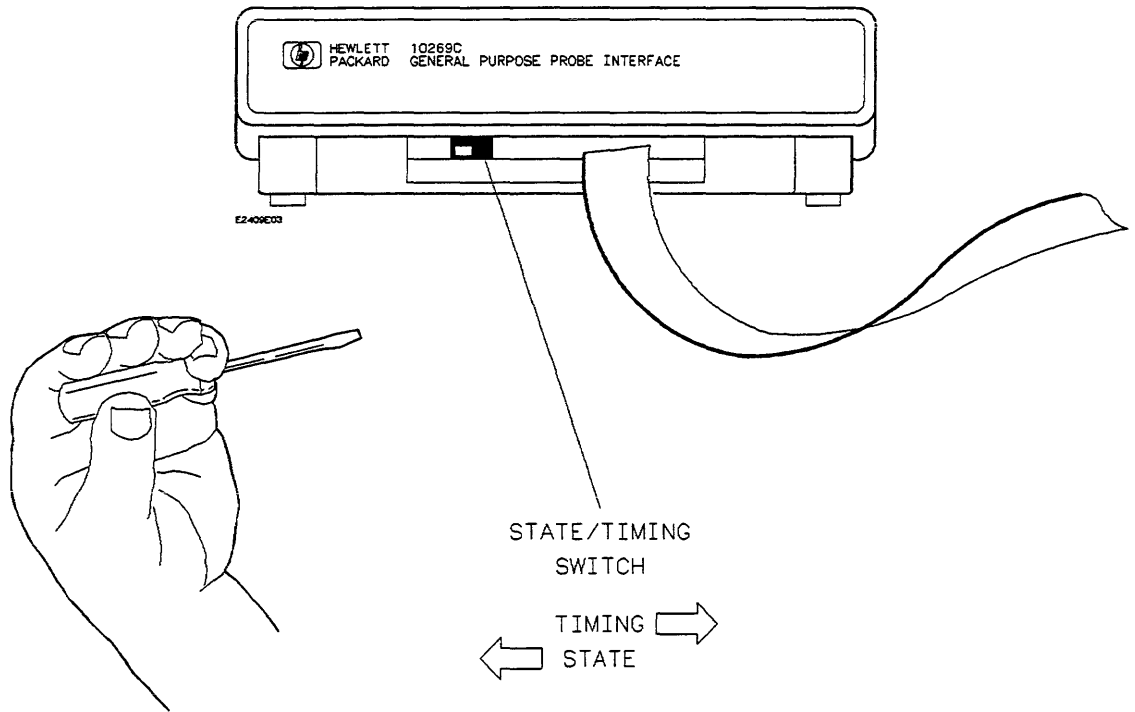


Figure 1-6. Accessing the State/Timing Switch

Setting Up the Analyzer from the Disk

The logic analyzer can be configured for 80286 analysis by loading the appropriate configuration file from the flexible disk. Loading a state configuration file will also automatically load the inverse assembler. To load a configuration file:

1. Install the HP E2409B flexible disk in the front disk drive of the logic analyzer.
2. Select one of the following menus:
 - For the HP 1650 series logic analyzers, select the I/O Disk Operations menu;
 - For the HP 16500 series logic analyzers, select the System Front Disk menu.
3. Configure the menu to "Load" the analyzer from one of the files listed in table 1-3.
4. For the HP 16500 series logic analyzers, select the configuration file with the knob, then touch "All" and select the correct module.
5. Execute the load operation to load the file into the logic analyzer.

Table 1-3. Configuration Files

Logic Analyzer	State	Timing
HP 1650A, HP 1650B, HP 1652B, HP 16510A, or HP 16510B	C80286S	C80286T
HP 16511B	D80286S	D80286T
HP 16540A,D with one HP 16541A,D Expander Card	E80286S	E80286T1
HP 16540A,D with two HP 16541A,D Expander Cards	E80286S	E80286T
HP 16550A	F80286S	F80286T

Analyzing the Intel 80286

Introduction

This chapter provides reference information on the format specifications and symbols configured by the HP E2409B software. It also provides information about the inverse assembler and status encoding.

State Format Specification

The 80286 Inverse Assembler file contains predefined format specifications (see figure 2-1). These format specifications include all labels for monitoring the 80286 microprocessor and any coprocessors connected directly to the microprocessor.

Note 

For those logic analyzers which have a Clock Period field (HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, and HP 16511B), the Clock Period field in figure 2-1 should remain in the current selection (> 60 ns) for proper HP E2409B operation. For more information on the Clock Period field, refer to your logic analyzer reference manual.

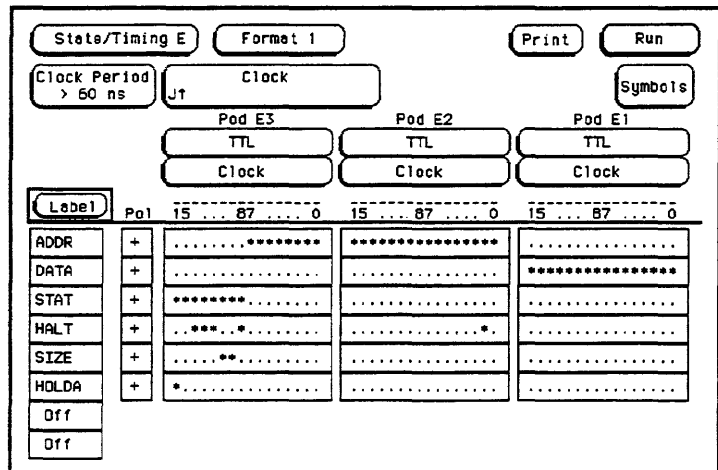


Figure 2-1. State Format Specification

Symbols

The Symbol Table of the format specification menu is set up with names to identify values of the status label (see table 2-1).

Additional labels have been defined in the format specification to make triggering on specific 80286 cycles easier. Labels that may be of interest are:

- The "SIZE" label which indicates the size of the transfer on the DATA bus (byte or word transfer) and which byte in the word of a byte transfer is valid.
- The "HALT" label which differentiates between a halt cycle caused by executing the HALT instruction and a shutdown cycle caused by an execution while attempting to process a double fault exception.

Some symbol tables use a blank character string to represent a signal in its negated (or de-asserted) state. This makes the listing menu easier to read by making the active samples stand out compared to normal negated states.

Table 2-1. HP E2409B Symbols

Label	Symbol	Pattern
STAT	INTERRUPT ACK HALT/SHUTDOWN MEMORY READ MEMORY WRITE I/O READ I/O WRITE OPCODE FETCH	xx000xx0 xx010xx0 xx011xx0 xx010xx1 xx101xx0 xx100xx1 xx111xx0
HALT	SHUTDOWN HALT	01000 01001
SIZE	WORD TRANSFER LOW BYTE XFER HIGH BYTE XFER	00 01 10

Table 2-1. HP E2409B Symbols (Continued)

Label	Symbol	Pattern
HOLDA	CPU	0
	DMA	1
BHE	ENABLED H_BYTE	0
	DISABLED H_BYTE	1
M/IO	IO PORT	0
	MEMORY	1
COD/IN	INTR ACKNOWLEDGE	0
	OPCODE	1
LOCK	LOCK	0
	(blank)	1
S0	S0	0
	(blank)	1
S1	S1	0
	(blank)	1
READY	READY	0
	(blank)	1
RESET	(blank)	0
	RESET	1

Listing Menu

Captured data is displayed as shown in figures 2-2 and 2-3 in the following sections. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

The 80286 Inverse Assembler

The 80286 inverse assembler has been designed to support the 80286 microprocessor with or without coprocessors. The following paragraphs explain the operation of the inverse assembler and the results you can expect in certain situations.

The 80286 can fetch instructions of up to two bytes (16 bits) in a single bus cycle. However, the microprocessor does not provide enough status information to discriminate between the first code fetch cycle of an instruction and subsequent code fetch cycles. You must point to the state that contains the first byte of an opcode fetch. Once synchronized, the inverse assembler will disassemble from this state through the end of the screen.

Use the following steps to synchronize the inverse assembler:

1. Identify a line on the display that you know contains the first byte of an opcode fetch.
2. Roll this line to the top of the screen. Note that the cursor location is not the top of the screen. In figure 2-2, line -7 is the top of the screen.
3. Select the "Invasm" field at the top of the display. The listing will inverse assemble from the top line down. Any data before this screen is left unchanged.

Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the screen by entering a new line number, you must re-synchronize the inverse assembler by repeating steps 1 through 3.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Interpreting Data

Unless followed by a lower-case letter, all numeric output from the inverse assembler is in the hexadecimal format. A lower-case "o" following a numeric value indicates an octal representation (the ESC instruction for example). Decimal values are indicated by a lower-case "d" (as in the INT instruction).

Two instructions may be displayed for a single analyzer state because the 80286 fetches a word with two instruction bytes from program memory. If the least significant byte of this word contains a single-byte instruction, the next sequential instruction begins in the upper byte. In this case, the two instructions displayed on a single line are separated by the delete symbol (␣). Since instructions may begin in either the lower or upper byte, the last byte of a multiple-byte instruction may also occur in the lower byte, with a second instruction beginning in the upper byte. In this instance, the delete symbol is displayed in the left-most position of the mnemonic display field. Thus, the following definition: Any instruction appearing to the right of the delete symbol begins in the upper byte of the fetched word.

Examples:

<code>PUSH DX ␣ ADC BX,DX</code>	(PUSH occupies the lower byte; ADC begins in the upper byte.)
<code>␣ CMP AX,#53E6</code>	(An instruction shown on a previous line uses the lower byte; CMP begins in the upper byte.)
<code>JO OFLOW_CTL</code>	(JO begins in the lower byte and uses the upper byte as well.)

Pound signs (#) in the inverse assembler output indicate that the numbers following the pound sign (#) are immediate operands.

Asterisks (*) in the inverse assembler output indicate a portion (or portions) of an instruction was not captured by the analyzer as shown in line -3 of figure 2-2. Missing opcodes occur frequently and are primarily due to microprocessor prefetch activity. Storage qualification, or the use of storage windows, can also lead to such occurrences.

State/Timing E		Listing I		Invasm		Print		Run	
Markers		Off							
Label>	ADDR	80286 Mnemonic							
Base>	Hex	hex							
-7	04075A	3076 memory read						MEMOR	
-6	030BE3	■ JPF	s	30B99				OPCOD	
-5	030BE4	nu ■ ADD	BX,DX					OPCOD	
-4	030BE6	nu ■ SAL/SHL	BX,1					OPCOD	
-3	030BE8	nu ■ ADD							OPCOD
-2	030B99	■ MOV	BX,#0120					OPCOD	
-1	030B9A	0120 code fetch						OPCOD	
0	030B9C	XOR DX,DX						OPCOD	
1	030B9E	MOV DI,#0010						OPCOD	
2	030BA0	MOV AX,CS						OPCOD	
3	030BA2	DIV DI						OPCOD	
4	030BA4	OR DX,#0030						OPCOD	
5	030BA6	30CA code fetch						OPCOD	
6	030BA8	■ CMP	DL,#3A					OPCOD	
7	030BAA	3AFA code fetch						OPCOD	
8	030BAC	JL/NGE 30BB1						OPCOD	

Figure 2-2. State Listing Display

The 80286 microprocessor can perform word transfers as well as byte transfers between microprocessor registers and memory. Furthermore, byte transfers may occur on either the upper eight bits or the lower eight bits of the 16-bit data bus. The inverse assembler makes a distinction between these conditions by displaying "xx" (don't care) for the byte of the transfer that was ignored by the microprocessor. In this way, it is possible to determine exactly which byte was used by the microprocessor:

- 28B3 memory write (word transfer)
- xxB3 memory write (byte transfer on lower 8 bits)
- 28xx memory write (byte transfer on upper 8 bits)

Prefetching Instructions in the Queue (nu/nu?)

The 80286 microprocessor is a prefetching microprocessor. That is, it fetches up to four instruction words while the last opcode is still being executed. When a program executes an instruction that causes a branch, prefetched words are not used and will be discarded by the microprocessor. Unused prefetches are indicated by the prefix "nu" (not used) in the inverse assembly listing.

The logic analyzer captures prefetches, even if they are not executed. Care must be taken when you are specifying a trigger condition or a storage qualification and the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches at most four words, one technique to avoid unwanted triggering from unused prefetches is to add "8" to the trigger address. This trigger condition will only be satisfied if the branch is not taken.

On line 15 of figure 2-3, the inverse assembler could determine that the conditional jump was taken to line 20. This was determined when the increment by two address sequence was broken. In this case, the inverse assembler prefixes lines 16, 17, 18, and 19 with "nu" to indicate that these lines were not used.

Label>		ADDR	80286 Mnemonic	STAT
Base>		Hex	hex	Bina
7	01040E	4444	code fetch	01111
8	010410	CMP	DH,DL	01111
9	010412	JNE/NZ	1041A	01111
10	010414	nu? MOV	AX,#5555	01111
11	010416	nu? MOV	BX,#6666	01111
12	010418	nu? 6666	code fetch	01111
13	01041A	MOV	CX,#7777	01111
14	01041C	MOV	CH,CL	01111
15	01041E	JE/Z	10427	01111
16	010420	nu MOV	AX,#8888	01111
17	010422	nu 8888	code fetch	01111
18	010424	nu MOV	BX,#9999	01111
19	010426	nu MOV	CX,#AAAA	01111
20	010427	MOV	CX,#AAAA	01111
21	010428	AAAA	code fetch	01111
22	01042A	CMP	CH,CL	01111

Figure 2-3. State Listing Display

In some cases, it is impossible to determine from bus activity whether or not a branch was taken or a prefetch was executed. In these cases, the inverse assembler will prefix the disassembled line with "nu?"

On line 9 of figure 2-3, the inverse assembler cannot determine if a conditional jump was taken because the 80286 address counter would sequence the same way whether or not the conditional jump was taken. Because of this, lines 10, 11, and 12 are prefixed with "nu?"

Instruction Type

The 80286 instruction set contains groups of instructions defining the instruction type in the second opcode byte, rather than in the first byte. In this case, if the second opcode byte is not stored in analyzer memory, only the group where an instruction resides can be determined. Therefore, the group name, rather than an instruction mnemonic, is displayed in the mnemonic display field. These group names are defined as follows:

- **Immed** - Contains the following instructions when used with immediate source operands:

ADD	AND
OR	SUB
ADC	XOR
SBB	CMP

- **Shift** - Contains the following logical and arithmetic shifts and rotates:

ROL	SHL/SAL
ROR	SHR
RCL	SAR
RCR	

- Grp_1 - Contains the following instructions:

TEST	IMUL
NOT	DIV
NEG	IDIV
MUL	



The TEST instruction is included only when the instruction concerns an immediate source operand.

- Grp_2 - Contains the following groups of instructions:

INC	when the instruction concerns memory operands on 8-bit registers.
DEC	when the instruction concerns memory operands on 8-bit registers.
CALL	indirect operand.
JMP	indirect operand.
PUSH	when the instruction concerns 16-bit memory operands.

- 2-byte - Contains the following instructions or groups of instructions:

LAR	2 byte Grp1
LSL	2 byte Grp2
CLTS	

The 80286 instruction set contains two groups of instructions where the instruction type is defined in the third byte. In this case, if the third byte is not stored in analyzer memory, only the group where an instruction resides can be determined. Therefore, the group name, rather than an instruction mnemonic, is displayed in the mnemonic display field. These groups are defined as follows:

- 2 byte Grp1 - Contains the following instructions:

SLDT	LTR
STR	VERR
LLDT	VERW

- 2 byte Grp2 - Contains the following instructions:

SGDT	LGDT
SIDT	LIDT
SMSW	LMSW

Abbreviations Listed below are several abbreviations for normal programming syntax that have been adopted to reduce the width of the inverse assembler display field.

dwp	- DWORD PTR
wp	- WORD PTR
bp	- BYTE PTR
fp	- FAR PTR
np	- NEAR PTR
s	- SHORT

These symbols are displayed only if the operation size cannot be determined from the instruction itself.

To further reduce the field width of the inverse assembler, LOCK and REPEAT prefixes appear on the line before the instruction to which they apply.

Physical Addresses Physical, rather than logical addresses, are used to perform symbolic address mapping. Most instructions, however, specify a 16-bit intrasegment offset and may indicate a segment different from the default segment for that particular instruction. Since the physical address cannot be determined from this information alone, the inverse assembler must attempt to locate the resulting bus cycle so that the physical address may be obtained. If a bus cycle of the type indicated by the initiating instruction is not found, the physical address cannot be determined and an unmapped logical address (segment override, if any, and the 16-bit intrasegment offset) is displayed instead of a mapped physical address.

Coprocessor Support The HP E2409B Preprocessor Interface fully supports the 80287 coprocessor. The 80287 instructions are inverse assembled and all 80287 operand transfers are decoded as I/O reads and writes.

Time Count The HP E2409B Preprocessor Interface will send all bus transactions by both the microprocessor and coprocessor to the logic analyzer. The time count will accurately reflect the time between the bus cycles on the logic analyzer display.

Status Encoding Each of the eight bits in the STATUS label are described in table 2-2. Table 2-3 lists the meaning of each bit for all types of 80286 microprocessor cycles. Bit 0 is the least significant bit of the 8-bit field.

Table 2-2. STATUS Label Bits

Bit	Description
0	device status bit S1.
1	device status bit BHE.
2	device address bit A0.
3	device status bit S0.
4	device status bit M/IO.
5	device status bit COD/INTA.
6	device status bit LOCK.
7	device status bit HLDA.

Table 2-3. Status Field Encoding

80286	Status Bit 7 6 5 4 3 2 1 0
Cycle Type	
Interrupt Acknowledge	x x 0 0 0 x x 0
Halt/Shutdown	x x 0 1 0 x x 0
Memory Read	x x 0 1 1 x x 0
Memory Write	x x 0 1 0 x x 1
I/O Read	x x 1 0 1 x x 0
I/O Write	x x 1 0 0 x x 1
Opcode Fetch	x x 1 1 1 x x 0
Valid bytes in Transfer (from BHE and A0)	
Word (both bytes valid)	x x x x x 0 0 x
Low Byte	x x x x x 0 1 x
High Byte	x x x x x 1 0 x
Other Cycle Information	
Lock	x 0 x x x x x x
Hold Acknowledge	1 x x x x x x x

Note: x = don't care

Timing Format Specification

When the preprocessor interface is used for timing analysis, the format specification is set up similar to those shown in figures 2-4 and 2-5. The formats may be slightly different, depending on which logic analyzer you are using.

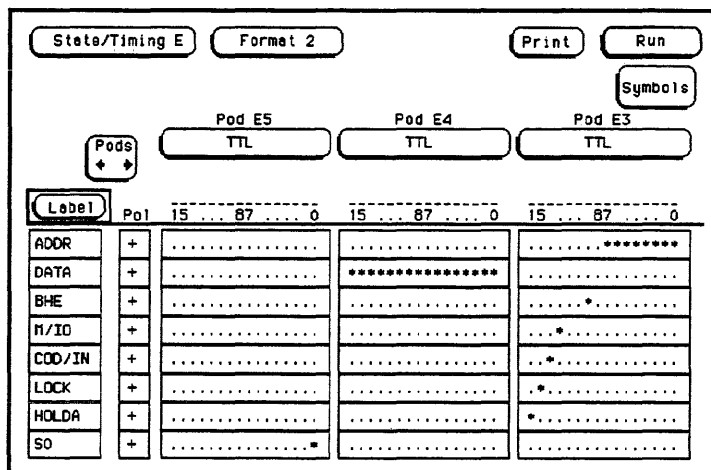


Figure 2-4. Timing Format Specification (Pods 3-5)

Note 

In figures 2-4 and 2-5 additional labels are listed offscreen. To view these signals on your logic analyzer, select the Label field and rotate the knob on the front panel clockwise.

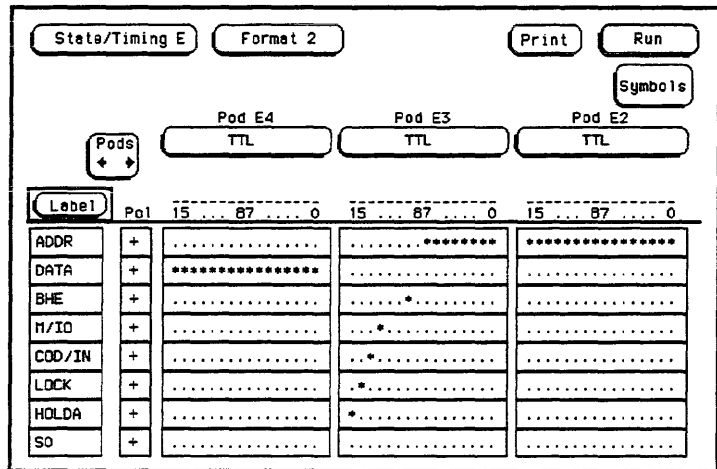


Figure 2-5. Timing Format Specification (Pods 2-4)

Waveforms Display

Captured timing data is displayed in the Waveforms menu as shown in figure 2-6.

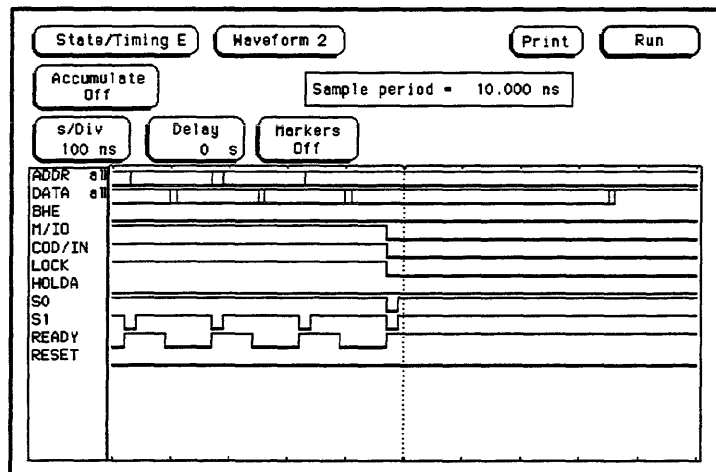


Figure 2-6. Timing Waveforms Display

General Information

Introduction

This chapter provides additional reference information including the characteristics and interface requirements for the HP E2409B Preprocessor Interface.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2409B Preprocessor Interface. These characteristics are included as additional information for the user.

**Microprocessor
Compatibility:**

Intel 80286 and all microprocessors made by other manufacturers that comply with Intel 80286 specifications.

Microprocessor Package:

68-contact PGA.

68-contact PLCC (with option 1CB adapter).

68-contact LCC (with option 1CA adapter).

Accessories Required:

HP 10269C.

Maximum Clock Speed:

25 MHz clock output (50 MHz clock input).

Note 

In the state mode, the preprocessor interface may not meet the 80286 specification for hold time. For more information, see "Violations of the 80286 Hold Time" in this chapter.

Signal Line Loading:

1 "F" TTL load plus approximately 40 pF on the following lines:

A0-A23, BHE, M/IO, COD/INTA, LOCK, HLDA, D0-D15.

1 "F" TTL load plus approximately 5 pF on the following lines:

S0, S1, READY, RESET, CLK.

PLCC Adapter Loading: Approximately 3.5 pF.

LCC Adapter Loading: Approximately 3.5 pF.

Microprocessor Operations Displayed: Memory Read/Write
I/O Read/Write
Opcode Fetch
Interrupt Acknowledge
Halt
Hold Acknowledge
Lock
Transfer to 80287 Coprocessor

Timing Analysis: All of the 80286 signals are buffered through the preprocessor. The following signals have a maximum of 14 ns (7 ns typical) of skew:

S0, S1, READY, and RESET.

All other signals have a maximum of 6 ns (3 ns typical) of skew.

Power Requirements: 0.66 A at +5 Vdc maximum, supplied by the logic analyzer.

Logic Analyzer Required: HP 1650A, HP 1650B, HP 16510A, HP 16510B, HP 1652B, HP 16511B, HP 16540/16541A,D, or HP 16550A.

Environmental

Temperature: Operating: +20 to +45° C
(+68 to +113° F)

Nonoperating: -40 to +75° C
(-40 to +167° F)

Altitude: Operating: 4,600 m (15,000 ft)

Nonoperating: 15,300 m (50,000 ft)

Humidity: Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

Interface Description

The primary function of a preprocessor interface is to connect the target microprocessor to the logic analyzer through the general purpose probe interface, and to perform any functions unique to that particular microprocessor. The HP E2409B Preprocessor Interface performs this primary function by:

- Latching and buffering the address, status, and data bus of the 80286 microprocessor so that address, status, and data can be sent to the logic analyzer at the same time.
- Generating the logic analyzer clock from the appropriate 80286 microprocessor signals and bus conditions. See figure 3-1 for a block diagram of the preprocessor interface.

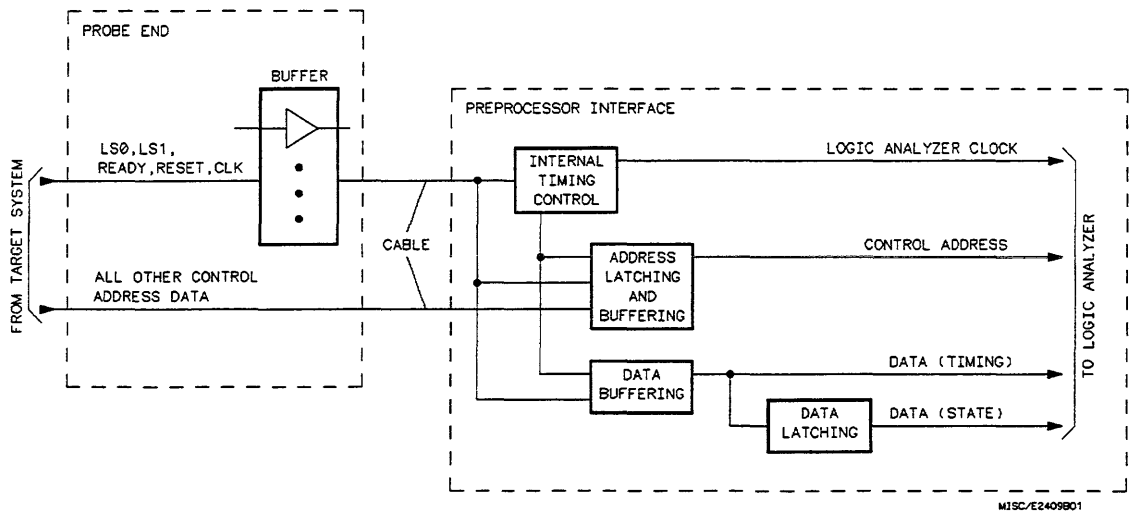


Figure 3-1. HP E2409A Block Diagram

State and Timing Modes

Some of the signal connections that are made through pods 1 through 5 of the HP 10269C General Purpose Probe Interface change when you switch between state and timing modes. In the state mode, pods 4 and 5 are not used and the data bus is monitored on pod 1. The state configuration files set up the logic analyzer for the correct pod connections for state analysis.

In the timing mode, the data bus is monitored on pod 4 and S0, S1, READY, and RESET are monitored on pod 5. Pod 1 is not used in the timing mode. The timing configuration files set up the logic analyzer for the correct pod connections for timing analysis. For more information on the signal routing, refer to table 3-1 at the end of this chapter.

State Analysis

The preprocessor interface detects the start of an 80286 bus cycle when the S0 or S1 status line goes true. The preprocessor interface clocks in S0 and S1 at this point, then latches address and status at the end of the Ts state of the bus cycle. At the end of the first Tc state of the bus cycle, the interface samples the READY signal and, if found true, the bus cycle is terminated and the logic analyzer is clocked at the starting of the next bus state. If the READY signal is not sampled true at the end of the first Tc state, it is sampled at the end of each subsequent Tc state until it is found true (each extra Tc state is equivalent to adding one wait state). The preprocessor interface samples data on every falling edge of the clock and the data is transferred to the secondary latches on every rising edge of the clock. When data on the secondary latches is determined to be good, the data is clocked into the logic analyzer along with the address and status previously latched. The HP E2409B Preprocessor Interface operates with an 80286 microprocessor clocked at rates up to 50 MHz (system clock).

Data is latched by the falling edge of the CLK signal. The CLK signal is delayed by a buffer on the probing end of the preprocessor interface cable. This delay plus the hold time of the data latches requires that the data be valid for at least 9.5 ns after the end of the bus cycle.

Timing Analysis

All of the 80286 signals are buffered through the preprocessor interface. This causes some skew between signals due to differences in the propagation delay of the buffers. There are four signals that are buffered twice with the addition of the 74F244 that is on the target end of the preprocessor interface cable. These signals are S0, S1, READY, and RESET. They have a maximum of 14 ns (7 ns typical) of skew from all of the other timing signals coming from the HP E2409B Preprocessor Interface.

All other timing signals have a maximum skew of 6 ns (3 ns typical). These signals include ADDRESS, DATA, HOLDA, COD/INTA, M/IO, BHE, and LOCK

Violations of the 80286 Hold Time

For analysis with the HP E2409B Preprocessor Interface, sampled data signals must be valid 10 ns after the bus cycle terminates. The termination of the bus cycle is referenced from the falling edge of the 80286 clock. If the signals are invalid before the specified time, incorrect data may be captured by the logic analyzer. The HP E2409B Preprocessor Interface typically latches the data bus 6 ns (9.5 ns maximum) after the falling edge of the 80286 input clock.

The high duration of the input clock should not be less than 8 ns. The low duration of the input clock should not be less than 6 ns.

80286 Signal to HP E2409B Connector Mapping

The following table describes the electrical interconnections implemented with the HP E2409B Preprocessor Interface. Since the logic analyzer pods may be numbered differently than the 10269C pods, refer to table 1-1 or 1-2 to correlate the pod numbers.

Table 3-1. 80286 Signal List

CPU Signal	CPU Pin	Label	10269C Pod	Logic Analyzer Bit
A0	34	ADDR	2	0
A1	33	ADDR	2	1
A2	32	ADDR	2	2
A3	28	ADDR	2	3
A4	27	ADDR	2	4
A5	26	ADDR	2	5
A6	25	ADDR	2	6
A7	24	ADDR	2	7
A8	23	ADDR	2	8
A9	22	ADDR	2	9
A10	21	ADDR	2	10
A11	20	ADDR	2	11
A12	19	ADDR	2	12
A13	18	ADDR	2	13
A14	17	ADDR	2	14
A15	16	ADDR	2	15
A16	15	ADDR	3	0
A17	14	ADDR	3	1
A18	13	ADDR	3	2
A19	12	ADDR	3	3
A20	11	ADDR	3	4
A21	10	ADDR	3	5
A22	8	ADDR	3	6
A23	7	ADDR	3	7

Table 3-1. 80286 Signal List (Continued)

CPU Signal	CPU Pin	Label	10269C Pod	Logic Analyzer Bit
D0	36	DATA	1	0
D1	38	DATA	1	1
D2	40	DATA	1	2
D3	42	DATA	1	3
D4	44	DATA	1	4
D5	46	DATA	1	5
D6	48	DATA	1	6
D7	50	DATA	1	7
D8	37	DATA	1	8
D9	39	DATA	1	9
D10	41	DATA	1	10
D11	43	DATA	1	11
D12	45	DATA	1	12
D13	47	DATA	1	13
D14	49	DATA	1	14
D15	51	DATA	1	15
S1	4	STAT	3	8
BHE	1	STAT	3	9
A0	34	STAT	3	10
S0	5	STAT	3	11
M/IO	67	STAT	3	12
COD/INTA	66	STAT	3	13
LOCK	68	STAT	3	14
HLDA	65	STAT	3	15
(Note 1)	--	CLOCK	1	J CLK

Note 1: This signal clocks the logic analyzer. It is a combination of several microprocessor signals.

Table 3-1. 80286 Signal List (Continued)

CPU Signal	CPU Pin	Label	10269C Pod	Logic Analyzer Bit
D0	36	T_DATA	4	0
D1	38	T_DATA	4	1
D2	40	T_DATA	4	2
D3	42	T_DATA	4	3
D4	44	T_DATA	4	4
D5	46	T_DATA	4	5
D6	48	T_DATA	4	6
D7	50	T_DATA	4	7
D8	37	T_DATA	4	8
D9	39	T_DATA	4	9
D10	41	T_DATA	4	10
D11	43	T_DATA	4	11
D12	45	T_DATA	4	12
D13	47	T_DATA	4	13
D14	49	T_DATA	4	14
D15	51	T_DATA	4	15
S0	5	T_CONT	5	0
S1	4	T_CONT	5	1
READY	63	T_CONT	5	2
RESET	29	T_CONT	5	3

Note 

The signals shown on pods 4 and 5 in table 3-1 are for timing analysis only.

Servicing

The repair strategy for the HP E2409B is board replacement. However, table 3-2 lists the cables and some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Table 3-2. Replaceable Parts

HP Part Number	Description
E2409-69503	Exchange Board Assembly
E2409-66503	Circuit Board Assembly
E2409-04102	Cover
E2409-61601	Cable
1390-0393	TS Screw Captive
1200-1516	Pin Protector IC Socket
5081-7702	PGA-LCC Adapter
5081-7703	PGA-PLCC Adapter
E2409-68703	Disk Pouch Software Package

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface are not installed properly, or they are not making electrical contact.

- Verify that the microprocessor and the preprocessor interface are properly rotated and aligned.
- Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.
- Reduce the number of extender sockets (see also "Capacitive Loading").

"Slow or Missing Clock" HP 16540/16541A,D State:

The HP 16540/16541A,D Master Card is not receiving any clocks.

- Ensure that the target system is On.
- Ensure that Pod 1 of the HP 10269C is connected to pod 1 of the Master Card.

HP 16511B State:

The HP 16511B expander card is not receiving state clocks.

- Ensure that the pod 1 cable from the expander (lower) HP 16511B card is connected to Pod 1 of the HP 10269C.

HP 1650A,B, HP 16510A,B, or HP 1652B State:

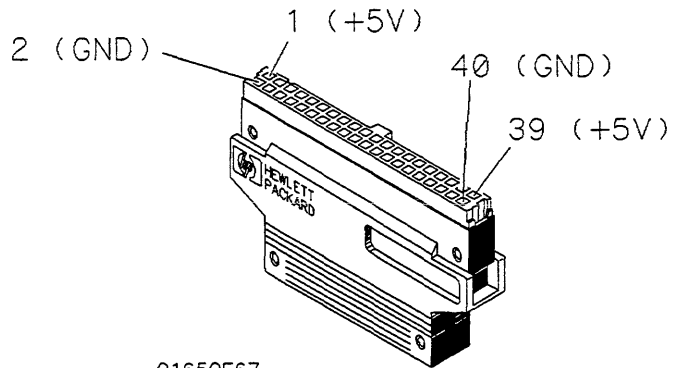
The logic analyzer is not receiving state clocks.

- Ensure that the pod 1 cable from the logic analyzer is connected to Pod 1 of the HP 10269C.
- For HP 1650A and HP 16510A Logic Analyzers, check the preprocessor interface power fuse in the logic analyzer.

Slow Clock If you have the preprocessor interface hooked up and running and observe a slow clock or no activity from the interface board, the +5 V supply coming from the analyzer may not be getting to the interface board.

To check the +5 V supply coming from the analyzer, disconnect one of the logic analyzer cables from the HP 10269C and measure across pins 1 and 2 or pins 39 and 40 (see figure A-1, next page).

- If +5 V isn't observed across these pins, check the internal preprocessor fuse or current limiting circuit on the logic analyzer. For information on checking this fuse or circuit, refer to the service manual for your logic analyzer.
- If +5 V is observed across these pins and you feel confident that the +5 V is getting to the preprocessor interface, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.



01650E67

Figure A-1. Pinout of the Logic Analyzer Cable

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500 disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading an appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

No Inverse Assembly

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display and pressing the "Invasm" key (see "Inverse Assembler" in Chapter 2).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that all microprocessor caches and memory managers have been disabled. In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly but the execution trace is lost.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

No Activity on Activity Indicators

On the HP 1650A, HP 1651A, and HP 16510A Logic Analyzers if there is no activity the fuse which allows power to the preprocessor interface is probably blown. Check the fuse in the logic analyzer. On the other logic analyzers, if there is no activity one of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading.

One technique to reduce the capacitive loading is to remove as many pin protectors, extenders, and adapters as possible.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

Note

The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to < 60 ns. If this error message is observed with the Clock Period set to > 60 ns, or with the HP 16540/16541A,D, Logic Analyzer, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches. Add the prefetch queue depth to the trigger address to avoid this problem.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set, this message indicates for an HP 1650A,B, HP 1652B, or HP 16510A,B Logic Analyzer that the pattern duration is probably set to less than (<) instead of greater than (>). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins

Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

**"Time from Arm
Greater Than
41.93 ms."**

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

**No Setup/Hold
Field on Format
Screen**

The HP 16540/16541A,D Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

**"Default
Calibration
Factors Loaded"
(16540/16541A,D)**

The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16540A,D and HP 16541A,D cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.

Your Comments Please

HP E2409B

Your comments assist us in meeting your needs better. Please complete this questionnaire and return it to us. Feel free to add any additional comments that you might have. All comments and suggestions become the property of Hewlett-Packard. Omit any questions that you feel would be proprietary.

- | | Yes | No |
|--|---------------|-------------|
| 1. Did you receive your product when expected? | [] | [] |
| 2. Were you satisfied with the operation of the preprocessor interface at turn-on? | [] | [] |
| 3. Were the proper accessories supplied with your product? | | |
| If not, what was missing? | | |
| Cables [] | Manual(s) [] | Other _____ |

4. What measurements will this preprocessor interface be used to make?

5. Which logic analyzer are you using?

Type _____

6. What do you like most about the preprocessor interface? .

7. What would you like to see changed or improved? _____

8. Which sections of the manual(s) have you used?

- Installation Quick Reference
- Step-By-Step Procedures
- Characteristics

9. Please rate the manual(s) on the following:

4 = Excellent 3 = Good 2 = Adequate 1 = Poor

- Breadth and depth of information
- Ability to easily find information
- Ability to understand and apply the information provided in the manual

Please explain: _____

10. What is your experience with logic analyzers and preprocessor interfaces?

- No previous experience
- Less than 1 year experience
- More than 1 year's experience on one model
- More than 1 year's experience on several models

Name _____ Company _____

Address _____ Zip Code _____

Phone _____ Instrument Serial # _____

THANK YOU FOR YOUR HELP

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Your cooperation in completing and returning this form
will be greatly appreciated. Thank you.

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