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User's Guide

HP E2403A
Intel 80486
Universal Interface

HP E2403A
Intel 80486 Universal Interface User's Guide

for the HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, HP 16511B, HP 16515A/16516A, and HP 16540A/16541A Logic Analyzers

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Contents

Introduction

The HP E2403A Universal Interface provides a complete interface between any 80486 target system and a variety of HP logic analyzers. The 80486 configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the 80486 microprocessor.

Logic Analyzers Supported

The following logic analyzers are supported by the HP E2403A Universal Interface:

HP 1650A, HP 1650B, HP 16510A, HP 16510B, and HP 1652B

These logic analyzers provide 1 k of memory depth with either 80 channels of 35 MHz state analysis (25 MHz state analysis for the HP 1650A or HP 16510A) or 80 channels of 100 MHz timing analysis.

HP 16511B

This logic analyzer combination provides 1 k of memory depth with either 160 channels of 35 MHz state analysis or 80 channels of 35 MHz state analysis and 80 channels of 100 MHz timing analysis.

HP 16540A with two HP 16541A Expansion Cards

This logic analyzer combination provides 4 k of memory depth with 112 channels of 100 MHz state or timing analysis.

HP 16515A/16516A

This logic analyzer combination provides 8 k of memory depth with 32 channels of 1 GHz timing analysis.

The 80-channel logic analyzers do not provide all of the auxiliary status and control information available with the HP 16511B and HP 16540A/16541A logic analyzers.

How to Use This Manual

Each chapter in this manual addresses a specific set of topics:

- **Chapter 1** - discusses the HP E2403A Universal Interface and explains its key features.
- **Chapter 2** - explains how to install and configure the universal interface for timing or state analysis with the supported analyzers.
- **Chapter 3** - provides additional information to consider when making measurements.
- **Chapter 4** - guides you through solutions to some possible difficulties that may be encountered while making measurements. It also contains information on servicing.
- **Appendix A** - contains information on how the 80486 signals are routed to connector pins on the universal interface board.
- **Appendix B** - explains how to make measurements across multiple modules using the intermodule capabilities of the HP 16500A Logic Analysis System.

1

General Information

Introduction

The HP E2403A Universal Interface provides a convenient mechanical and electrical connection between an 80486 microprocessor and a variety of HP logic analyzers. Specifically, the HP E2403A Universal Interface supports logic analysis with the HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, HP 16511B, HP 16515A/16516A, and HP 16540A/16541A logic analyzers.

Note

This product does not contain 1 GHz Termination Adapters which are used with the HP 16515A/16516A 1 GHz Timing Analyzer. If you plan to use this product with the HP 16515A/16516A timing analyzer, order one 1 GHz Termination Adapter (HP part number 16515-63202) for each HP 16515A or HP 16516A card.

Since the HP E2403A Universal Interface board passively probes the 80486, this universal interface can be used for timing analysis as well as state analysis. During state analysis, the logic analyzer samples the 80486 signals on every rising edge of the CLK signal and the logic analyzer sample rate equals the microprocessor clock rate. This state-per-clock capability is especially useful for hardware debugging and analysis.

The software included in the HP E2403A Universal Interface provides configuration files for all of the supported analyzers. These configuration files contain pre-defined labels, symbol tables, and default displays that allow you to make measurements quickly and easily. These files can be used independently of one another, or they can be combined in a variety of ways to allow optimum use of the analyzers available.

Duplicating the Master Disk

Before you use the HP E2403A software, use the Duplicate Disk operation in the disk menu of your logic analyzer to make a duplicate copy of the HP E2403A master disk. Store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidentally deleted.

Equipment Supplied

The HP E2403A Universal Interface consists of the following items:

- The universal interface board (HP part number E2403-66501).
- Three pin protectors (HP part number 1200-1512).
- Seven 100 kOhm Termination Adapters (HP part number 01650-63203).
- The configuration software on a 3.5-inch disk.
- This user's guide.

Equipment Required

The minimum hardware required for analysis of an 80486 target system consists of the following equipment:

- The 80486 Universal Interface (HP E2403A).
- An HP 16515A/16516A, HP 16511B, HP 16510A, HP 16510B, HP 1650A, HP 1650B, HP 1652B, or HP 16540A/16541A logic analyzer.
- One 1 GHz Termination Adapter per HP 16515A or HP 16516A card (HP part number 16515-63202).

Caution 

To prevent equipment damage, remove the power from the target system whenever the universal interface or microprocessor is being connected or disconnected.

Features and Functions

Figure 1-1 shows the features of the HP E2403A Universal Interface board. The following paragraphs describe some of the features of the HP E2403A. These include the following items:

- Switch S1 for minimizing signal loading.
- Connector J8 which provides the correlation reference signal for deskewing measurements across multiple modules.

Minimizing Signal Loading

A five-station DIP switch (S1) controls the routing of the CLK and ADS# signals from the 80486 to various logic analyzer pod connectors. This provides you with the convenience of having the universal interface board connect the signals to the correct connectors while giving you the ability to remove the probe's capacitive loading from the target system.

The first station of the switch (closest to the PGA socket) is labeled DATA_L.CLK1. When this switch is closed, the CLK signal is probed by the pod connected to the DATA_L connector (J2) as a sample clock input for the logic analyzer. Similarly, when the second station of the switch, labeled STAT_1.CLK1, is closed, the CLK signal is probed by the pod connected to the STAT_1 connector (J7) as a sample clock input for the logic analyzer.

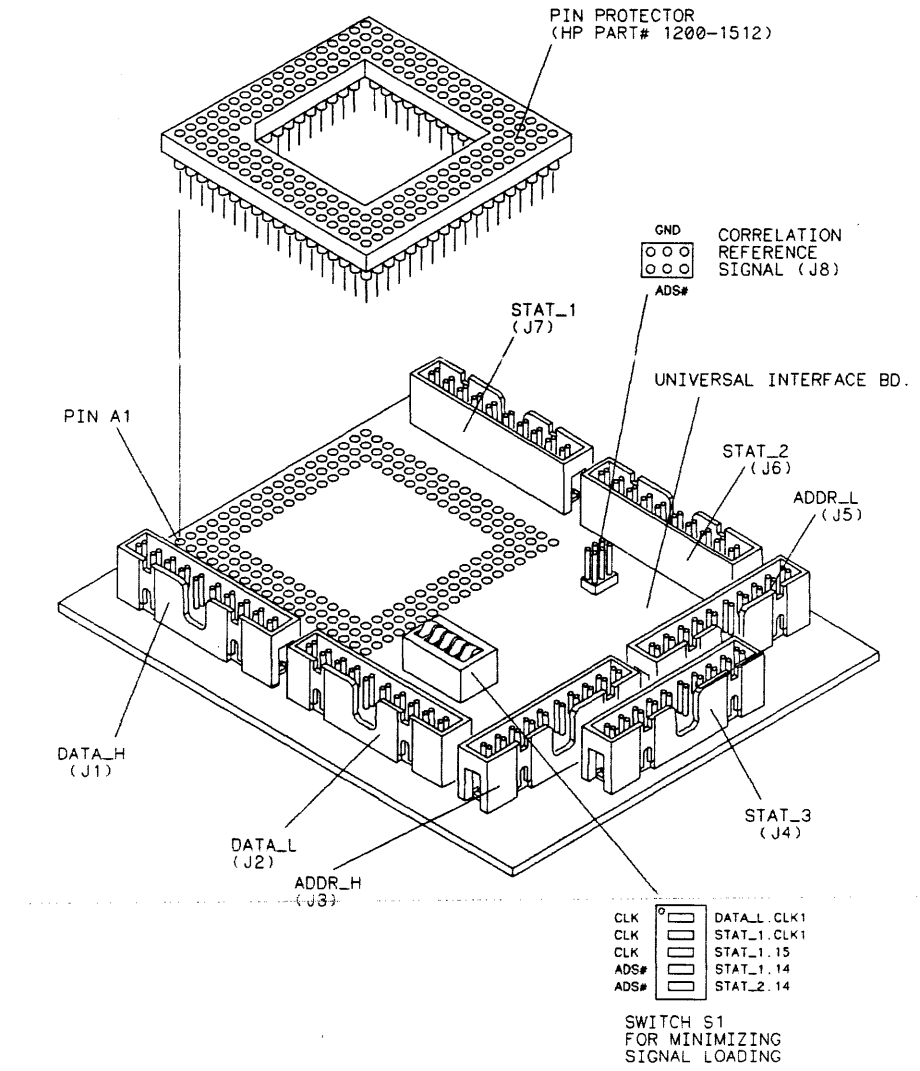


Figure 1-1. HP E2405A Assembly

When the third station of the switch, labeled STAT_1.15, is closed, the CLK signal is probed as data bit 15 of the pod connected to the STAT_1 connector (J7). For state analysis, the third station can be left open since no meaningful information is obtained by probing the CLK signal as a data channel. Likewise, during timing analysis, the first and second stations can be left open because a timing analyzer does not require an external clock.

The fourth station of the switch is labeled STAT_1.14. When this switch is closed, it connects the ADS# signal to data bit 14 of the STAT_1 connector (J7). The STAT_1.14 connection is usually left closed for both state and timing analysis on ADS#.

The last station of the switch is labeled STAT_2.14. It connects ADS# to data bit 14 of the STAT_2 connector (J6). The STAT_2.14 connection is only closed when ADS# is being used as a correlation reference signal.

Refer to the section "Measurement Configurations" in chapter 2 for switch settings for specific measurements. Figure 1-2 shows the electrical connections to the switch.

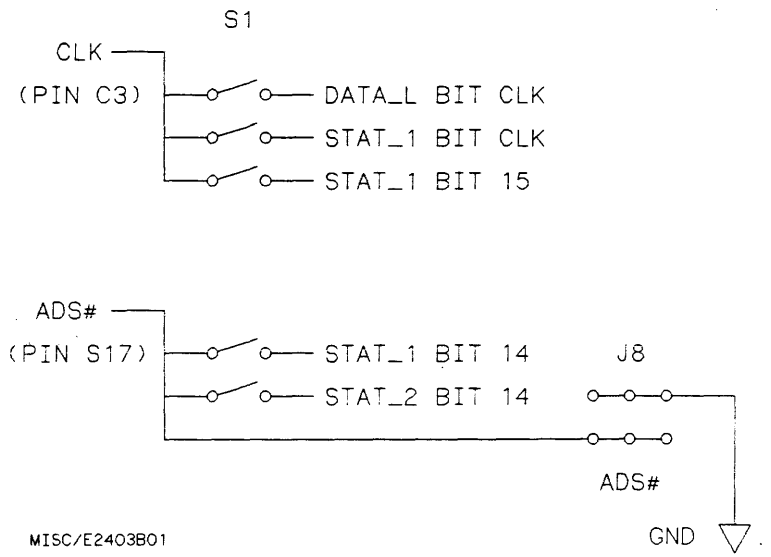


Figure 1-2. Schematic of Switch S1

Probing the Correlation Reference Signal

The ADS# signal from the 80486 is used as a reference signal for deskewing measurements taken across multiple modules. The 16500A mainframe can resolve the time between triggers of individual modules with 10 ns resolution. This can be lowered to 1 ns by probing ADS# with each module and deskewing after each measurement.

The universal interface board provides connections from ADS#, via S1, to connectors STAT_1 and STAT_2. The two-by-three pin post connector at J8 provides an opportunity for analyzers that are not probing STAT_1 or STAT_2 to probe ADS#. The 0.100 inch centered spacing of the pins makes it easy to connect the blue probe tips from a HP 16515A/16516A timing analyzer directly to J8.

Caution 

To avoid shorting the 80486's ADS# signal to ground via the logic analyzer probing system, observe the GND labelling on the universal interface board and on the HP 16515A/16516A probe tips.

For more information on making intermodule measurements with the HP E2403A Universal Interface, refer to appendix B.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2403A Universal Interface. These characteristics are included as additional information for the user.

Microprocessor Compatibility: Intel 80486 and all microprocessors made by other manufacturers that comply with Intel 80486 specifications.

Microprocessor Package: 168-pin PGA.

Accessories Required: One - 1 GHz Termination Adapter for each HP 16515A or HP 16516A card (HP part number 16515-63202).

Maximum Clock Speed: 33 MHz CLK input for state analysis with the HP 1650B, HP 1652B, HP 16510B, HP 16511B or HP 16540A/16541A.

25 MHz CLK input for state analysis with the HP 16510A and HP 1650A.

Setup/Hold Time Required: For state analysis with the HP 16540A/16541A, a 4 ns setup time and 0 s hold time, referenced to the rising edge of the CLK signal, is required of all 80486 signals.

For state analysis with the HP 16511B, HP 16510A, HP 16510B, HP 1650A, HP 1650B, or HP 1652B, a 10 ns setup time and 0 s hold time, referenced to the rising edge of the 80486 CLK signal, is required for each signal sampled.

Note 

Some 80486 signals may not meet the setup and hold requirements for the analyzer. For specific information, see "Violations of the Logic Analyzer Setup Time Specification" in chapter 3.

Signal Line Loading: For analysis with the HP 16511B, HP 16510A, HP 16510B, HP 1650A, HP 1650B, HP 1652B, or HP 16540A/16541A:

6 pF, plus 12 pF in parallel with 100 kΩ, for each signal probed.

For analysis with the HP 16515A/16516A:

6 pF, plus 9 pF in parallel with 10 kΩ, for each signal probed.

Power Requirements: None.

Logic Analyzer Required: HP 16515A/16516A, HP 16511B, HP 16510A, HP 16510B, HP 1650A, HP 1650B, HP 1652B, or HP 16540A/16541A.

Number of Probes Used: HP 16515A/16516A - 32 to 80 single-channel probes.

HP 16511B - Six 16-channel probes.

HP 16540A/16541A - Seven 16-channel probes.

HP 16510A, HP 16510B, HP 1650A, HP 1650B, and HP 1652B - Five 16-channel probes.

Environmental Temperature:	Operating:	0 to +55° C (+32 to +131° F)
	Nonoperating:	-40 to +75° C (-40 to +167° F)
Altitude:	Operating:	4,600 m (15,000 ft)
	Nonoperating:	15,300 m (50,000 ft)

Humidity: Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

2

Measurement and Installation

Introduction

This chapter provides two different types of information. First, the quick reference section immediately following this introduction gives you a high-level description of the installation and measurement process. Second, the sections following the quick reference section contain detailed low-level information about the various steps listed in the quick reference section. To help you find detailed information, use the page references in the quick reference section.

Measurement and Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the HP E2403A Universal Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

1. Select the type of measurement you want to perform (state, timing, across multiple modules, etc.).
2. Decide which signals you want to monitor (see pages 2-4 to 2-20).
3. Select the analyzer type that will best suit your needs (see page 2-2).
4. With the information from the previous three steps, select the appropriate configuration file (see pages 2-4 to 2-20).
5. Load the appropriate configuration file (see page 2-22).
6. Set the five switches on the universal interface board to the appropriate positions (see pages 2-8, 2-10, 2-12, 2-16, 2-19, or 2-21).
7. Connect the 1 GHz Termination Adapters (HP part number 16515-63202) or 100 kOhm Termination Adapters (HP part number 01650-63203) to the logic analyzer probes and cables (see page 2-26).

8. Connect the HP E2403A Universal Interface board to the target system (see page 2-27).
9. Connect the termination adapters to the appropriate connectors on the universal interface board (see page 2-30).
10. Run the measurement.

Measurement Configurations

The HP E2403A Universal Interface supports logic analysis with several HP logic analyzers. The type of measurement desired may influence the choice of the logic analyzer.

State Analysis

For state analysis, the following logic analyzers are supported:

HP 16511B

This analyzer provides 160 channels of 35 MHz state analysis. It allows you to monitor all 80486 signals at 80486 clock (CLK) speeds of up to 35 MHz.

HP 16510B, HP 1650B, or HP 1652B

These analyzers provide 80 channels of 35 MHz state analysis. They allow you to monitor a subset of 80486 signals at 80486 clock (CLK) speeds of up to 35 MHz.

HP 16510A or HP 1650A

These analyzers provide 80 channels of 25 MHz state analysis. They allow you to monitor a subset of 80486 signals at 80486 clock (CLK) speeds of up to 25 MHz.

Note 

For a 33 MHz 80486, certain signals may not meet the 10 ns setup time required by the above logic analyzers. Refer to "Violations of Logic Analyzer Setup Time Specification" in chapter 3 for more information.

HP 16540A/16541A

With two HP 16541A expansion cards this analyzer provides 112 channels of 100 MHz state analysis. It allows you to monitor all 80486 signals at 80486 clock (CLK) speeds of up to 100 MHz. The HP 16540A/16541A has a 4 ns setup time and 0 s hold time.

Timing Analysis

The 80486 clock (CLK) speed is not a factor for timing analysis. For timing analysis, the following logic analyzers are supported:

HP 16515A

This analyzer provides 16 channels of 1 GHz timing analysis. It allows you to monitor a subset of 80486 signals.

HP 16515A/16516A

This analyzer provides 32 channels of 1 GHz timing analysis. It allows you to monitor a subset of 80486 signals.

HP 16511B, HP 16510A, HP 16510B, HP 1650A, HP 1650B, or HP 1652B

These analyzers provide 80 channels of 100 MHz timing analysis. They allow you to monitor a subset of 80486 signals.

Note 

Wider timing analysis can be accomplished by using multiple modules and correlating their measurements with the intermodule capabilities of the HP 16500A Logic Analysis System. For more information on intermodule measurements, refer to appendix B.

HP 16540A/16541A

With two HP 16541A expansion cards this analyzer provides 112 channels of 100 MHz timing analysis. It allows you to monitor all 80486 signals.

HP 16515A and HP 16516A Configurations

The first seven configuration files provided on the disk support the HP 16515A 1 GHz timing analyzer (16 channels). The next four configuration files support the master/expansion combination of the HP 16515A and HP 16516A timing analyzer (32 channels). In some measurements, an HP 16515A/16516A analyzer is more powerful than two single HP 16515A analyzers. For example, 32-bit pattern recognition is possible with the HP 16515A/16516A, but only 16-bit pattern recognition is possible with the HP 16515A analyzers. The following table lists the 80486 signals probed by each configuration file and the mapping of logic analyzer pods to connectors on the HP E2403A Universal Interface board.

Table 2-1. HP 16515A/16516A Configurations

80486 Signals	Analyzer Labels	HP E2403A Connector Number	HP E2403A Connector Name	Analyzer Pod	Configuration File
D31 - D16	DATA_H	J1	DATA_H	M1, M2	UI_486_01
D15 - D0	DATA_L	J2	DATA_L	M1, M2	UI_486_02
A31 - A16	ADDR_H	J3	ADDR_H	M1, M2	UI_486_03
FLUSH# A20M# IGNNE# FERR# PCD PWT	FLUSH A20M IGNNE FERR PCD PWT	J4	STAT_3	M1, M2	UI_486_04
A15 - A2	ADDR_L	J5	ADDR_L	M1, M2	UI_486_05
DP3-DP0 PCHK# LOCK# AHOLD	DP PCHK LOCK AHOLD	J6	STAT_2	M1, M2	UI_486_06 (continued)

Pods M1 and M2 refer to pods 1 and 2 of an HP 16515A 1 GHz Timing Analyzer master card. This card is always located in the lower of the two slots that the HP 16515A/16516A analyzer set occupies.

Pods E1 and E2 refer to pods 1 and 2 of an HP 16516A 1 GHz Timing Analyzer expansion card. This card is always located in the upper of the two slots that the HP 16515A/16516A analyzer set occupies.

Table 2-1. HP 16515A/16516A Configurations (Continued)

80486 Signals	Analyzer Labels	HP E2403A Connector Number	Name	Analyzer Pod	Configuration File
EADS#	EADS				UI_486_06 (continued)
BREQ	BREQ				
HOLD	HOLD				
BOFF#	BOFF				
INTR	INTR				
NMI	NMI				
ADS#	ADS				
RESET	RESET				
CLK	CLK	J7	STAT_1	M1, M2	UI_486_07
ADS#	VALIDS				
RDY#	VALIDS				
BRDY#	VALIDS				
M/IO#	CYCLE				
D/C#	CYCLE				
W/R#	CYCLE				
BE3#-BE0#	BE				
BS8#	SIZE				
BS16#	SIZE				
ADS#	ADS				
RDY#	RDY				
BRDY#	BRDY				
BLAST#	BLAST				
KEN#	KEN				
W/R#	W/R				
D/C#	D/C				
M/IO#	M/IO				
HLDA	HLDA				
BS16#	BS16				
BS8#	BS8				

Pods M1 and M2 refer to pods 1 and 2 of an HP 16515A 1 GHz Timing Analyzer master card. This card is always located in the lower of the two slots that the HP 16515A/16516A analyzer set occupies.

Pods E1 and E2 refer to pods 1 and 2 of an HP 16516A 1 GHz Timing Analyzer expansion card. This card is always located in the upper of the two slots that the HP 16515A/16516A analyzer set occupies.

Table 2-1. HP 16515A/16516A Configurations (Continued)

80486 Signals	Analyzer Labels	HP E2403A Connector Number	Name	Analyzer Pod	Configuration File
A31 - A2	ADDR	J3 J5	ADDR_H ADDR_L	M1, M2 E1, E2	UI_486_08
D31 - D0	DATA	J1 J2	DATA_H DATA_L	M1, M2 E1, E2	UI_486_09
CLK	CLK	J7	STAT_1	M1, M2	UI_486_10
M/IO#	CYCLE				
D/C#	CYCLE				
W/R#	CYCLE				
BE3#-BE0#	BE				
BS8#	SIZE				
BS16#	SIZE				
ADS#	ADS				
BRDY#	BRDY				
BLAST#	BLAST				
KEN#	KEN				
HLDA	HLDA				
W/R#	W/R				
D/C#	D/C				
M/IO#	M/IO				
BS16#	BS16				
BS8#	BS8				
ADS#	VALIDS				
RDY#	VALIDS				
BRDY#	VALIDS				(continued)

Pods M1 and M2 refer to pods 1 and 2 of an HP 16515A 1 GHz Timing Analyzer master card. This card is always located in the lower of the two slots that the HP 16515A/16516A analyzer set occupies.

Pods E1 and E2 refer to pods 1 and 2 of an HP 16516A 1 GHz Timing Analyzer expansion card. This card is always located in the upper of the two slots that the HP 16515A/16516A analyzer set occupies.

Table 2-1. HP 16515A/16516A Configurations (Continued)

80486 Signals	Analyzer Labels	HP E2403A Connector Number	Name	Analyzer Pod	Configuration File
EADS# DP3-DP0 PCHK# AHOLD EADS#	VALIDS DP PCHK AHOLD EADS	J6	STAT_2	E1, E2	UI_486_10 (continued)
D31 - D16	DATA_H	J1	DATA_H	M1, M2	UI_486_11
DP3-DP0 PCHK# LOCK# AHOLD EADS# BREQ HOLD BOFF# INTR NMI ADS# RESET	DP PCHK LOCK# AHOLD EADS BREQ HOLD BOFF INTR NMI ADS RESET	J6	STAT_2	E1, E2	

Pods M1 and M2 refer to pods 1 and 2 of an HP 16515A 1 GHz Timing Analyzer master card. This card is always located in the lower of the two slots that the HP 16515A/16516A analyzer set occupies.

Pods E1 and E2 refer to pods 1 and 2 of an HP 16516A 1 GHz Timing Analyzer expansion card. This card is always located in the upper of the two slots that the HP 16515A/16516A analyzer set occupies.

Switch Settings

The switch settings required for timing analysis with an HP 16515A/16516A are listed below:

Signal	Switch	Position
CLK	DATA_L.CLK1	open
CLK	STAT_1.CLK1	open
CLK	STAT_1.15	closed
ADS#	STAT_1.14	closed
ADS#	STAT_2.14	closed*

* Close the connection from ADS# to bit 14 of pod STAT_2 only if you desire to use ADS# as the correlation reference signal.

State clocking is not required for timing configurations, so both of the connections from the CLK signal to the analyzer clock inputs can be left open. The connection from the CLK to bit 15 of pod STAT_1 is closed to allow for timing analysis of the CLK signal.

The connection from ADS# to bit 14 of pod STAT_1 is closed to allow for timing analysis of the ADS# signal.

Extra Connections

To provide ADS# as a correlation reference signal to modules which are not probing the STAT_1 or STAT_2 connectors, one signal from each analyzer needs to probe ADS# instead of a signal normally probed on that analyzer. The recommended signals to re-dedicate to ADS# are A31, bit 0 which connects to ground as an address bus place holder, and D31.

The post connections of J8 are provided for these connections. While observing the signal and ground markings on the blue analyzer probe tips and the universal interface board, slide the probe tip directly on to the post connector.

HP 16511B Configurations

Two configuration files are provided for the HP 16511B Logic Analyzer:

- File "UI_486_12" configures the HP 16511B for state analysis of most of the 80486 signals.
- File "UI_486_13" configures the HP 16511B for timing analysis of most of the 80486 signals.

Note

The previous references to "most of the 80486 signals" refer to the analyzer's ability to work with up to 20 groups of labels at one time. The files configure the HP 16511B to monitor the most important 80486 signals within this 20 label capability.

The following tables summarize the 80486 signals probed in each configuration and the mapping of logic analyzer pods to connectors on the HP E2403A Universal Interface board.

Table 2-2. HP 16511B State Configurations

80486 Signals	Analyzer Labels	HP E2403A Connector Number	Name	Analyzer Pod	Configuration File
A31 - A2	ADDR	J5 J3	ADDR_L ADDR_H	E2 E3	UI_486_12
D31 - D0	DATA	J2 J1	DATA_L DATA_H	M5 E1	
M/IO# D/C# W/R# BE3#-BE0# BS8# BS16# KEN# BLAST# BRDY#	CYCLE CYCLE CYCLE BE SIZE SIZE KEN BLAST BRDY	J7	STAT_1	E5	(continued)

Pods E1 through E5 refer to pods 1 through 5 of an HP 16510B Logic Analyzer (expander) located in the lower of the two slots that the HP 16511B analyzer set occupies.

Pod M5 refers to pod 5 of an HP 16510B Logic Analyzer (master) located in the upper of the two slots that the HP 16511B analyzer set occupies.

Table 2-2. HP 16511B State Configurations (Continued)

80486 Signals	Analyzer Labels	HP E2403A Connector Number	Name	Analyzer Pod	Configuration File
RDY#	RDY				UI_486_12 (continued)
ADS#	ADS				
W/R#	W/R				
D/C#	D/C				
M/IO#	M/IO				
HLDA	HLDA				
ADS#	VALIDS				
RDY#	VALIDS				
BRDY#	VALIDS				
EADS#	VALIDS	J6	STAT_2	E4	
DP3-DP0	DP				
PCHK#	PCHK				
AHOLD	AHOLD				
EADS#	EADS				
HOLD	HOLD				

Pods E1 through E5 refer to pods 1 through 5 of an HP 16510B Logic Analyzer (expander) located in the lower of the two slots that the HP 16511B analyzer set occupies.

Switch Settings

The switch settings required for state analysis with an HP 16511B are listed below:

Signal	Switch	Position
CLK	DATA_L.CLK1	closed
CLK	STAT_1.CLK1	closed
CLK	STAT_1.15	open
ADS#	STAT_1.14	closed
ADS#	STAT_2.14	open

The HP 16511B requires that the probing system supply the same clocking signal to the same numbered pod on the upper and lower cards of the set. Both of the connections from the CLK signal to the analyzer clock inputs are closed to meet this requirement.

The connection from CLK to bit 15 of pod STAT_1 is left open, since it will always sample as a 0 for state analysis.

The connection from ADS# to bit 14 of pod STAT_1 is closed to allow state analysis of the ADS# signal. The connection from ADS# to bit 14 of pod STAT_2 is left open since the signal is already being monitored on pod STAT_1.

Table 2-3. HP 16511B Timing Configurations

80486 Signals	Analyzer Labels	HP E2403A Connector Number	Name	Analyzer Pod	Configuration File
A31 - A2	ADDR	J5 J3	ADDR_L ADDR_H	E2 E3	UI_486_13
D31 - D16	DATA_H	J1	DATA_H	E1	
CLK	CLK	J7	STAT_1	E5	
M/IO#	CYCLE				
D/C#	CYCLE				
W/R#	CYCLE				
BE3#-BE0#	BE				
BS8#	SIZE				
BS16#	SIZE				
KEN#	KEN				
BLAST#	BLAST				
BRDY#	BRDY				
RDY#	RDY				
ADS#	ADS				
W/R#	W/R				
D/C#	D/C				
M/IO#	M/IO				
HLDA	HLDA				
ADS#	VALIDS				
RDY#	VALIDS				
BRDY#	VALIDS				
EADS#	VALIDS	J6	STAT_2	E4	
DP3-DP0	DP				
PCHK#	PCHK				
AHOLD	AHOLD				
EADS#	EADS				

Pods E1 through E5 refer to pods 1 through 5 of an HP 16510B Logic Analyzer (expander) located in the lower of the two slots that the HP 16511B analyzer set occupies.

Switch Settings

The switch settings required for timing analysis with an HP 16511B are listed below:

Signal	Switch	Position
CLK	DATA_L.CLK1	open
CLK	STAT_1.CLK1	open
CLK	STAT_1.15	closed
ADS#	STAT_1.14	closed
ADS#	STAT_2.14	open

No state clocking is used for this timing configuration, so both of the connections from the CLK signal to the analyzer clock inputs are left open.

The connection from CLK to bit 15 of pod STAT_1 is closed to allow timing analysis of the CLK signal.

The connection from ADS# to bit 14 of pod STAT_1 is closed to allow timing analysis of the ADS# signal.

HP 16510A, HP 16510B, HP 1650A, HP 1650B, and HP 1652B Configurations

Five configuration files are provided for the HP 16510A, HP 16510B, HP 1650A, HP 1650B, and HP 1652B logic analyzers:

- File "UI_486_14" configures the logic analyzers for state analysis on the address bus, the high word of the data bus, and most of the status and control signals.
- File "UI_486_15" configures the logic analyzers for state analysis on the address bus, the entire data bus, and some of the status and control signals.
- File "UI_486_16" configures the logic analyzers for timing analysis on the same signals as the "UI_486_14" file.
- File "UI_486_17" configures the logic analyzers for timing analysis on the same signals as the "UI_486_15" file.
- File "UI_486_18" configures the logic analyzers for timing analysis on the signals that "UI_486_16" does not probe. This is particularly convenient if you want to probe all of the signals and have two 100 MHz timing analyzers available.

Note 

The previous references to "most" refer to the analyzer's ability to work with up to 20 groups of signals (called labels) at once. The files configure the logic analyzers to monitor the most important 80486 signals within this 20 label capability.

If you want to improve the correlation between the data of the measurements made with UI_486_16 and UI_486_18, you will want to manually probe ADS# as a correlation reference for the analyzer using the UI_486_18 configuration. Put a Probe Tip Assembly (HP part number 01650-61608) on to pod 3. Probe ADS# at the J8 post connector using pod 3 bit 0, and add the label ADS to the format menu.

The following tables summarize the 80486 signals probed in each configuration and the mapping of logic analyzer pods to connectors on the HP E2403A Universal Interface board.

Table 2-4. HP 16510A/B, HP 1650A/B, HP 1652B State

80486 Signals	Analyzer Labels	HP E2403A Connector Number	Name	Analyzer Pod	Configuration File
A31 - A2	ADDR	J5 J3	ADDR_L ADDR_H	3 4	UI_486_14
D31 - D16	DATA_H	J1	DATA_H	2	
M/IO#	CYCLE	J7	STAT_1	5	
D/C#	CYCLE				
W/R#	CYCLE				
BE3#-BE0#	BE				
BS8#	SIZE				
BS16#	SIZE				
KEN#	KEN				
BLAST#	BLAST				
BRDY#	BRDY				
RDY#	RDY				
ADS#	ADS				
W/R#	W/R				
D/C#	D/C				
M/IO#	M/IO				
HLDA	HLDA				
ADS#	VALIDS				
RDY#	VALIDS				
BRDY#	VALIDS				
EADS#	VALIDS	J6	STAT_2	1	
DP3-DP0	DP				
PCHK#	PCHK				
AHOLD	AHOLD				
EADS#	EADS				
HOLD	HOLD				

Table 2-4. HP 16510A/B, HP 1650A/B, HP 1652B State (Continued)

80486 Signals	Analyzer Labels	HP E2403A Connector Number	Name	Analyzer Pod	Configuration File
A31 - A2	ADDR	J5 J3	ADDR_L ADDR_H	3 4	UI_486_15
D31 - D0	DATA	J2 J1	DATA_L DATA_H	1 2	
ADS#	VALIDS	J7	STAT_1	5	
RDY#	VALIDS				
BRDY#	VALIDS				
M/IO#	CYCLE				
D/C#	CYCLE				
W/R#	CYCLE				
BE3#-BE0#	BE				
BS8#	SIZE				
BS16#	SIZE				
KEN#	KEN				
BLAST#	BLAST				
BRDY#	BRDY				
RDY#	RDY				
ADS#	ADS				
W/R#	W/R				
D/C#	D/C				
M/IO#	M/IO				
HLDA	HLDA				

Switch Settings

The switch settings required for state analysis with an HP 16510A, HP 16510B, HP 1650A, HP 1650B, or HP 1652B are listed below:

Signal	Switch	Position
CLK	DATA_L.CLK1	open
CLK	STAT_1.CLK1	closed
CLK	STAT_1.15	open
ADS#	STAT_1.14	closed
ADS#	STAT_2.14	open

The connection from CLK to the CLK1 bit of pod STAT_1 is closed to provide the sampling clock to the state analyzer. The connection to the CLK1 bit of pod DATA_L is left open since that pod is not probed in this configuration.

The connection from CLK to bit 15 of pod STAT_1 is left open, since it will always sample as a 0 for state analysis.

The connection from ADS# to bit 14 of pod STAT_1 is closed to allow for state analysis of the ADS# signal. The connection from ADS# to bit 14 of pod STAT_2 is left open since the signal is already being monitored on pod STAT_1.

Table 2-5. HP 16510A/B, HP 1650A/B, HP 1652B Timing

80486 Signals	Analyzer Labels	HP E2403A Connector Number	Name	Analyzer Pod	Configuration File
A31 - A2	ADDR	J5 J3	ADDR_L ADDR_H	3 4	UI_486_16
D31 - D16	DATA_H	J1	DATA_H	2	
CLK	CLK	J7	STAT_1	5	
M/IO#	CYCLE				
D/C#	CYCLE				
W/R#	CYCLE				
BE3#-BE0#	BE				
BS8#	SIZE				
BS16#	SIZE				
KEN#	KEN				
BLAST#	BLAST				
BRDY#	BRDY				
RDY#	RDY				
ADS#	ADS				
W/R#	W/R				
D/C#	D/C				
M/IO#	M/IO				
HLDA	HLDA				
ADS#	VALIDS				
RDY#	VALIDS				
BRDY#	VALIDS				
EADS#	VALIDS	J6	STAT_2	1	
DP3-DP0	DP				
PCHK#	PCHK				
AHOLD	AHOLD				
EADS#	EADS				

Table 2-5. HP 16510A/B, HP 1650A/B, HP 1652B Timing (Continued)

80486 Signals	Analyzer Labels	HP E2403A Connector Number	Name	Analyzer Pod	Configuration File
A31 - A2	ADDR	J5 J3	ADDR_L ADDR_H	3 4	UI_486_17
D31 - D0	DATA	J2 J1	DATA_L DATA_H	1 2	
CLK ADS# RDY# BRDY# M/IO# D/C# W/R# BE3#-BE0# BS8# BS16# KEN# BLAST# BRDY# RDY# ADS# W/R# D/C# M/IO# HLDA	CLK VALIDS VALIDS VALIDS CYCLE CYCLE CYCLE BE SIZE SIZE KEN BLAST BRDY RDY ADS W/R D/C M/IO HLDA	J7	STAT_1	5	
D15 - D0	DATA_L	J2	DATA_L	5	UI_486_18
FLUSH# A20M# GNNE# FERR# PCD PWT	FLUSH A20M IGNNE FERR PCD PWT	J4	STAT_3	4	

Switch Settings

The switch settings required for timing analysis with an HP 16510A, HP 16510B, HP 1650A, HP 1650B, or HP 1652B are listed below:

Signal	Switch	Position
CLK	DATA_L.CLK1	open
CLK	STAT_1.CLK1	open
CLK	STAT_1.15	closed
ADS#	STAT_1.14	closed
ADS#	STAT_2.14	open

No state clocking is used for this timing configuration, so both of the connections from the CLK signal to the analyzer clock inputs are left open.

The connection from CLK to bit 15 of pod STAT_1 is closed to allow for timing analysis of the CLK signal.

The connection from ADS# to bit 14 of pod STAT_1 is closed to allow for timing analysis of the ADS# signal.

HP 16540A/ 16541A Configurations

One configuration file is provided for the HP 16540A/16541A logic analyzer:

- File UI_486_19 configures the HP 16540A/16541A for state analysis of all 102 channels available from the HP E2403A.

For timing analysis with the HP 16540A/16541A, select "Timing" in the HP 16540A configuration menu, and set the HP E2403A switch settings for timing as specified on page 2-21.

Table 2-6. HP 16540A/16541A State Configurations

80486 Signals	Analyzer Labels	HP E2403A Connector Number	Name	Analyzer Pod	Configuration File
A31 - A2	ADDR	J5	ADDR_L	A1	UI_486_19
		J3	ADDR_H	A2	
FLUSH#	FLUSH	J4	STAT_3	A3	
A20M#	A20M				
GNNE#	IGNNE				
FERR#	FERR				
PCD	PCD				
PWT	PWT				
D31 - D0	DATA	J2	DATA_L	C1	
		J1	DATA_H	C2	
EADS#	VALIDS	J6	STAT_2	C3	
DP3-DP0	DP				
PCHK#	PCHK				
AHOLD	AHOLD				
EADS#	EADS				
CLK	CLK	J7	STAT_1	B1	
ADS#	VALIDS				
RDY#	VALIDS				
BRDY#	VALIDS				
M/IO#	CYCLE				
D/C#	CYCLE				
W/R#	CYCLE				
BE3#-BE0#	BE				
BS8#	SIZE				
BS16#	SIZE				
KEN#	KEN				
BLAST#	BLAST				
BRDY#	BRDY				
RDY#	RDY				
ADS#	ADS				
W/R#	W/R				
D/C#	D/C				
M/IO#	M/IO				
HLDA	HLDA				

Pods A1 to A3 refer to pods 1 to 3 of the upper HP 16541A expander card.

Pods C1 to C3 refer to pods 1 to 3 of the lower HP 16541A expander card.

Pod B1 refers to a pod on the HP 16540A master card.

Switch Settings

The switch settings required for state and timing analysis with an HP 16540A/16541A are listed below:

Signal	Switch	State Position	Timing Position
CLK	DATA_L.CLK1	open	open
CLK	STAT_1.CLK1	closed	open
CLK	STAT_1.15	open	closed
ADS#	STAT_1.14	closed	closed
ADS#	STAT_2.14	open	open

State

For state analysis, the connection from CLK to the CLK1 bit of pod STAT_1 is closed to provide the sampling clock to the state analyzer. The connection to the CLK1 bit of pod DATA_L is left open since that clock is not needed in this configuration.

The connection from CLK to bit 15 of pod STAT_1 is left open, since it will always sample as a 0 for state analysis.

The connection from ADS# to bit 14 of pod STAT_1 is closed to allow for state analysis of the ADS# signal. The connection from ADS# to bit 14 of pod STAT_2 is left open since the signal is already being monitored on pod STAT_1.

Timing

No state clocking is used for this timing configuration, so both of the connections from the CLK signal to the analyzer clock inputs are left open.

The connection from CLK to bit 15 of pod STAT_1 is closed to allow for timing analysis of the CLK signal.

The connection from ADS# to bit 14 of pod STAT_1 is closed to allow for timing analysis of the ADS# signal.

Configuring the Analyzer from the Disk

The logic analyzer can be configured for 80486 analysis by loading the appropriate 80486 configuration file. To load the configuration file:

1. Install the flexible disk labeled "80486 Configuration Files" in the front disk drive of the logic analyzer.
2. Select one of the following menus:
   - For the HP 1650A, HP 1650B, or HP 1652B, select the I/O Disk Operations menu;
   - For the HP 16515A/16516A, HP 16511B, HP 16510A, HP 16510B, or HP 16540A/16541A, select the System Front Disk menu.
3. Configure the menu to "Load" the analyzer from the appropriate file. Refer to the previous tables 2-1 through 2-6 for your file selection.
4. Execute the load operation to load the file into the analyzer.

Special Labels and Symbols

The configuration files provided with the HP E2403A contain predefined labels and symbols to clarify the displayed information. The labels closely resemble the name of the signals they contain, but the "#" symbol appended to active-low signal names does not appear with the labels. All labels are defined with a positive polarity, so active-low signals will be displayed as a "0" when they are asserted. Also, symbols defined for active-low signals use the pattern 0 for the asserted condition.

Symbol tables have been created for all labels that are not interpreted numerically. By displaying a character string instead of a "1" or "0," symbol tables help avoid any misunderstanding about whether a "1" represents only a high logic level or a signal assertion.

The symbol tables for some labels use a blank character string to represent a signal in its negated (or de-asserted) state. This makes the listing menu easier to read by making the active samples stand out compared to normal negated states.

The following symbol tables describe the composition of labels that are composed of more than one signal and are not interpreted numerically.

Table 2-7. Symbols for the CYCLE Label

Symbol	M/IO#	D/C#	W/R#
INT ACKNOWLEDGE	0	0	0
HALT/SPECIAL	0	0	1
I/O READ	0	1	0
I/O WRITE	0	1	1
OPCODE FETCH	1	0	0
MEM READ	1	1	0
MEM WRITE	1	1	1

Three versions of the symbol table for the VALIDS label are used:

- A three bit version is used when only STAT_1 is being probed.
- A four bit version is used when both connectors STAT_1 and STAT_2 are probed.
- For the HP 16540A/16541A a slightly different four bit version is used when both STAT_1 and STAT_2 are probed. The symbols and bits are the same, but they are in a different order.

Refer to the connection tables for each analyzer to determine when STAT_1 and STAT_2 are probed.

The symbols for the VALIDS label were chosen to convey the maximum amount of information about the validity of the address and data busses in the minimum amount of screen space.

Table 2-8 lists the symbols for the VALIDS label when STAT_2 is probed. Table 2-9 lists the symbols for the VALIDS label when STAT_2 is not probed.

The first column describes the validity of the address bus:

(blank)	not valid.
A	valid Address from the 80486.
EA	valid External cache invalidation Address to the 80486.
PEA	valid address from the 80486 microprocessor (ADS# and EADS# are low) which is also being used to invalidate the cache.

Table 2-8. Symbols for the VALIDS Label (with STAT_2)

Symbol		ADS#	RDY#	BRDY#	EADS#
PEA	RBD	0	0	0	0
A	RBD	0	0	0	1
PEA	D	0	0	1	0
A	D	0	0	1	1
PEA	BD	0	1	0	0
A	BD	0	1	0	1
PEA		0	1	1	0
A		0	1	1	1
EA	RBD	1	0	0	0
	RBD	1	0	0	1
EA	D	1	0	1	0
	D	1	0	1	1
EA	BD	1	1	0	0
	BD	1	1	0	1
EA		1	1	1	0
(blank)		1	1	1	1

The second column describes the validity of the data bus:

(blank)	not valid.
D	valid Data.
BD	valid Burst Data.
RBD	valid Data with RDY# asserted low and BRDY# asserted low.

Table 2-9. Symbols for VALIDS Label (without STAT_2)

Symbol		ADS#	RDY#	BRDY#
A	RBD	0	0	0
A	D	0	0	1
A	BD	0	1	0
A		0	1	1
	RBD	1	0	0
	D	1	0	1
	BD	1	1	0
(blank)		1	1	1

Table 2-10. Symbols for the SIZE Label

Symbol	BS8#	BS16#
8 BIT TRANSFER	0	x
16 BIT TRANSFER	1	0
32 BIT TRANSFER	1	1

Connecting the Termination Adapters to the Analyzer

The 1 GHz Termination Adapter (HP part number 16515-63202) allows the probes of the HP 16515A/16516A 1 GHz Timing Analyzer to be easily connected to the HP E2403A Universal Interface board.

The 100 kOhm termination adapter (HP part number 01650-63203) properly terminates the HP 16511B, HP 16510A, HP 16510B, HP 1650A, HP 1650B, HP 1652B, and HP 16540A/16541A logic analyzer probes. The adapter also allows the probes to be easily connected to the HP E2403A Universal Interface board.

Connecting the HP 16515A/16516A

The proper connections for the HP 16515A/16516A probes are shown on the 1 GHz Termination Adapter. Connect bits 0 through 7 of pod 1 to the first 8 data pins (D0 - D7) on the 1 GHz Termination Adapter, starting with bit 0 and ending with bit 7. Bits 0 through 7 of pod 2 should connect to the next 8 data pins (D8 - D15) of the 1 GHz Termination Adapter in a similar order. There should be one set of pins left unconnected between pins D7 and D8, and between pins D15 and CLK1 (see figure 2-1). These pins are left unconnected to compensate for the width of the HP 16515A/16516A probes.

Caution

Make sure the ground pin (GND) of the HP 16515A/16516A probe is facing toward the label side of the 1 GHz Termination Adapter and aligned with the proper pins before connecting it to the 1 GHz Termination Adapter. Reversing this connection may cause damage.

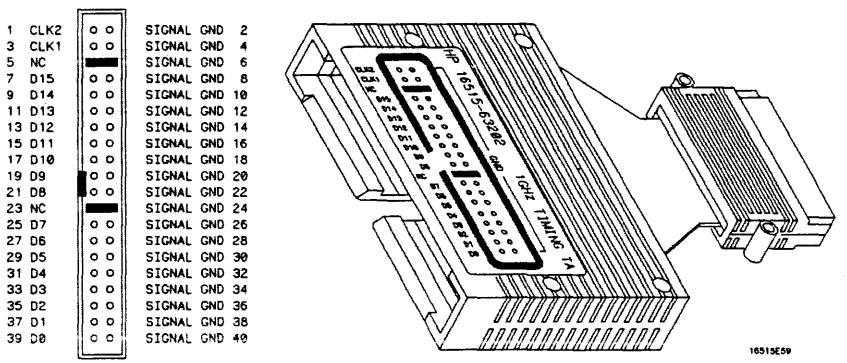


Figure 2-1. 1 GHz Termination Adapter Pinouts

Connecting the HP 16511B

For state analysis with the HP 16511B logic analyzer, connect 100 kOhm Termination Adapters to pod 5 of the master card and to pods 1 through 5 of the expander card.

For timing analysis, connect 100 kOhm Termination Adapters to pods 1 through 5 of the expander card.

Connecting the HP 16510A, HP 16510B, HP 1650A, HP 1650B, and HP 1652B

For state and timing analysis with an HP 16510A, HP 16510B, HP 1650A, HP 1650B, or HP 1652B logic analyzer, connect 100 kOhm Termination Adapters to pods 1 through 5.

Connecting the HP 16540A/16541A

For state or timing analysis with the HP 16540A/16541A logic analyzer, connect one 100 kOhm Termination Adapter to each of the seven pods.

Connecting to the Target System

1. Remove the 80486 microprocessor from its socket on the target system and store it in a protected environment.
2. Plug the universal interface board into the microprocessor socket on the target system. If the universal interface connector interferes with components of the target system or if a higher profile is required, add additional plastic pin guards.

Caution

To prevent equipment damage, remove the power from the target system whenever the universal interface or microprocessor is being connected or disconnected.

Caution

To prevent misalignment or damage, care must be taken to align pin A1 of the connector assembly with pin A1 of the microprocessor socket on the target system. Pin A1 of the connector assembly socket is identified on the universal interface board and shown in figure 2-2.

Note

Plastic pin guards can be ordered from Hewlett-Packard using the part number 1200-1512. However, any 168-pin PGA IC socket with an 80486 footprint and gold- plated pins can be used.

3. Plug the 80486 microprocessor into the socket of the universal interface board. The socket on the universal interface board is designed with low insertion force pins to allow you to install or to remove the microprocessor with a minimum amount of force.

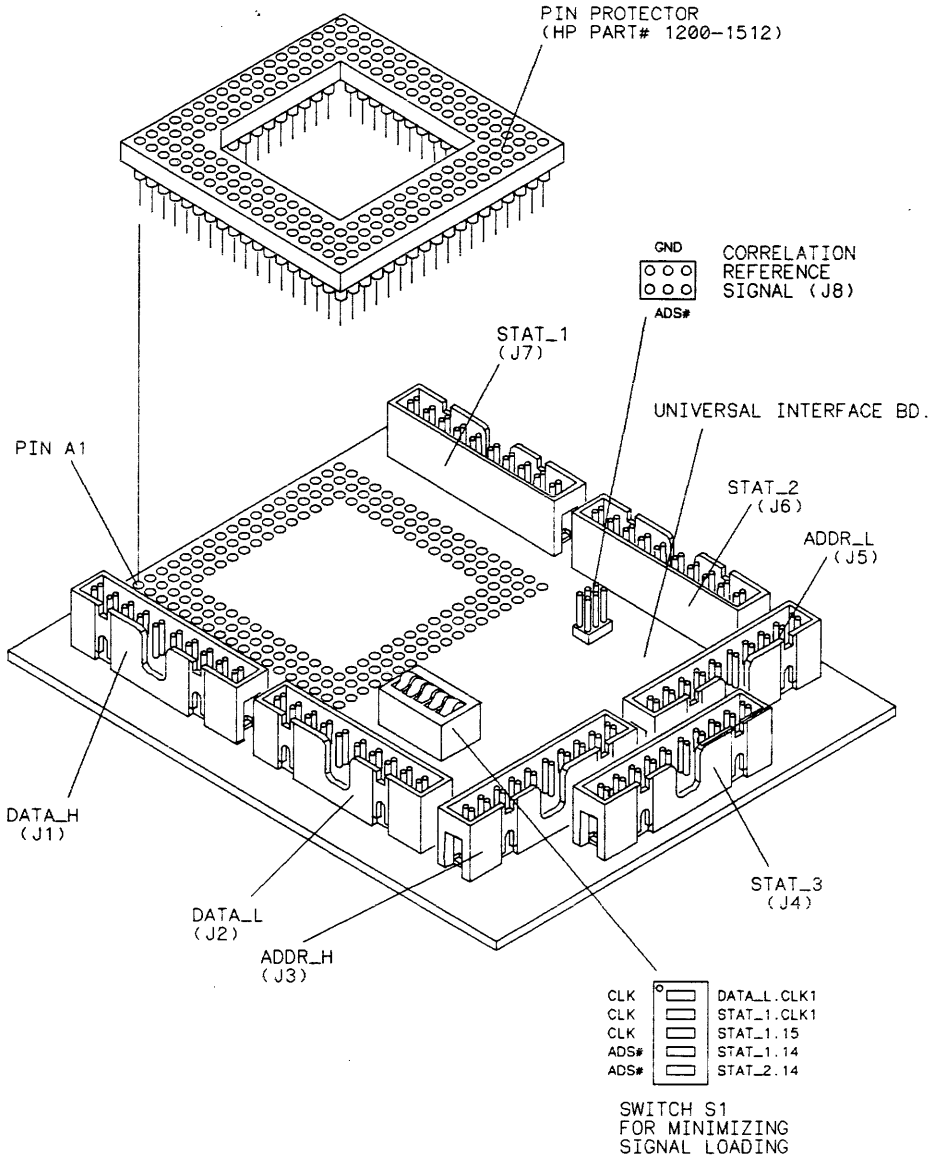
Caution

To avoid damaging the traces on the board, care must be used when removing a microprocessor or socket from the universal interface board.

Note

The universal interface socket assembly pins, shown in figure 2-2, are covered at the time of shipment with either a conductive foam wafer or a conductive plastic pin protector. This is done to protect the delicate gold-plated pins of the assembly from damage due to impact.

When you're not using the universal interface, protect the socket assembly pins from damage by covering them with the foam or plastic pin protector.



MISC/E2403E01

Figure 2-2. HP E2403A Assembly

Connecting the Termination Adapters to the HP E2403A

To connect either the 1 GHz Termination Adapters or 100 kOhm Termination Adapters to the universal interface board:

1. Align the key on the 20-pin connector of the termination adapter with the slot on the appropriate 20-pin connecter on the universal interface board.
2. Push the termination adapter into the connector.
3. Repeat steps 1 and 2 for each termination adapter.

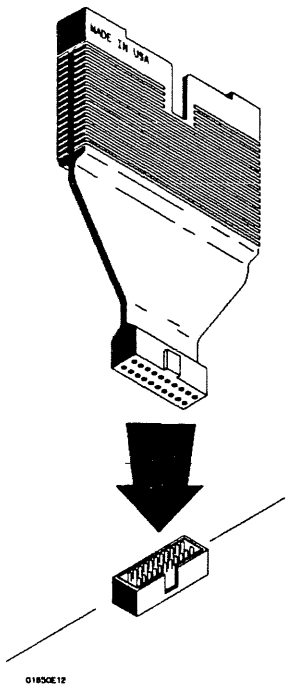


Figure 2-3. Connecting Termination Adapters

3

Additional Information

Introduction

This section contains additional information to consider when making measurements. The chapter is broken down into the following specific sections:

- Disabling the Cache Memory.
- Disabling the Address Translation.
- Violations of the Logic Analyzer Setup Specification.
- The Clock Period Field in the State Format Specification.
- Interpreting Displays in State Analysis.
- Specifying Patterns and Ranges for the ADDR Label.
- Modifying the Trace Specification for a Measurement.
- Time Resolution Between Modules.
- Probing Other 80486 Signals.
- Using "Pattern at Marker" in Waveform Displays.

Disabling the Cache Memory

In some measurements it may be desirable to disable the cache memory in the 80486. For example, while executing a program loop from its cache, the 80486 will not initiate any valid bus activity. To observe external bus transactions you may want to disable the cache. Refer to 80486 documentation for descriptions of techniques available to disable the cache memory.

Disabling the Address Translation

Since logic analyzers can only probe the physical pins of a microprocessor, the addresses sampled by an analyzer are physical addresses. The 80486 segmentation and paging units operate on the effective and logical addresses that the programmer is familiar with to create the physical address that the logic analyzer sees. It may be desirable to minimize or disable the effect of the segmentation and paging units for some measurements. Refer to your 80486 documentation for descriptions of techniques available to disable the segmentation and paging units.

Violations of the Logic Analyzer Setup Time Specification

For state analysis with the HP 16511B, HP 16510A, HP 16510B, HP 1650A, HP 1650B, or HP 1652B logic analyzer, sampled signals must be valid 10 ns before the sample clock transition occurs. These signals must remain valid until the sample clock occurs, which corresponds to a 0 ns hold time. The HP 16540A/16541A has a 4 ns setup and 0 s hold time.

To determine whether or not your state analyzer will take valid samples, compare the analyzer's setup and hold times to the setup and hold times provided by your version of the 80486 and your target system. Table 3-1 is an example of this comparison for a 33 MHz 80486. It is based on data provided in Intel's *i486 Microprocessor* manual, order number 240440-002, dated November, 1989.

The minimum state clock period for the logic analyzer is listed below:

- 40 ns for the HP 1650A and HP 16510A with no tagging.
- 28.57 ns for the HP 1650B, HP 1652B, HP 16511B, and HP 16510B with no tagging.
- 60 ns with time or state tagging.
- 10 ns for the HP 16540A/16541A with or without tagging.

HP 1650A and HP 16510A Speed Limit

The maximum state clock frequency for the HP 1650A/510A is 25 MHz, while the HP 1650B/510B and HP 1652B increase the frequency to 35 MHz. Since the 80486 CLK signal drives the state analysis clocking directly, the HP 1650A and HP 16510A can only be used with 80486 CLK speeds of up to 25 MHz.

Table 3-1. Example Timing Comparisons

	setup	hold
HP 16540A/16541A	≥ 4 ns	≥ 0 ns
All other logic analyzers	≥ 10 ns	≥ 0 ns
80486 (33 MHz):		
address, data (write), most cntl.	≥ 16 ns	≥ 3 ns
address, data, (read), DPn	≥ 5 ns	≥ 3 ns
HOLD, AHOLD	≥ 6 ns	≥ 3 ns
BOFF#	≥ 8 ns	≥ 3 ns
RESET, FLUSH#,	≥ 5 ns	≥ 3 ns
A20M#, NMI, INTR, IGNNE# EADS#, KEN#, BS8#, BS16#, RDY#, BRDY#	≥ 5 ns	≥ 3 ns
PCHK#	≥ 8 ns	≥ 3 ns

Example Timing Comparisons

Table 3-1 shows that the sampling window required by the 80486 for read cycles on the data bus is only 5 ns, while all the logic analyzers except the HP 16540A/16541A require a minimum of 10 ns. As long as memory systems return data to the microprocessor on read cycles an extra 5 ns earlier than the microprocessor requires, this configuration will sample correctly. A similar discussion holds for the other input signals to the microprocessor, including cache invalidation addresses, RDY#, BRDY#, EADS#, KEN#, BS8#, BS16#, HOLD, AHOLD, BOFF#, FLUSH#, A20M#, NMI, INTR, and IGNNE#.

In this example, the PCHK# output is not guaranteed to be valid for 10 ns or even 4 ns before rising CLK edges and therefore, may not be sampled correctly by the analyzers.

The Clock Period Field in a State Format Specification

Since the 80486 CLK signal functions as the logic analyzer sample clock for state analysis, time tagging, state tagging, and state analysis "prestore" features are not available at 80486 speeds greater than 16.67 MHz. To utilize these features you must operate the microprocessor at less than 16.67 MHz and set the Clock Period field to >60 ns. The HP E2403A configuration files set the analyzer for a clock period of less than 60 ns. This does not apply to the HP 16540A/16541A logic analyzer, because it operates at 100 MHz.

Interpreting Displays in State Analysis

Not withstanding the setup and hold time differences previously shown in this chapter, state analysis samples are taken at every rising CLK edge. This means that some samples will not contain any ADS#, EADS#, RDY#, or BRDY# asserted low. When these signals are not asserted low, samples do not contain valid information on either the address or data busses. When some of these signals (but not all) are asserted low, only the address or the data bus (but not both) may have valid samples.

Specifying Patterns and Ranges for the ADDR Label

When specifying patterns or ranges for the ADDR or ADDR_L label, be sure to enter numbers that end in a hexadecimal digit of 0, 4, 8, C, or X (don't care). Patterns ending in other digits will never be matched because the two least significant bits of the ADDR_L connector (J5) are connected to Vss as placeholders.

Connecting the two least significant bits of ADDR_L to Vss allows the logic analyzer to sample the 80486 address bus in a manner that provides the expected representation for displays. This also eliminates the need for you to logically shift the displayed address to the left two bits to interpret it correctly.

Modifying the Trace Specification for a Measurement

The configuration files provided with this product define a trace specification that allows you to make a measurement immediately after the RUN button is pressed. That is, the trigger condition consists of all "don't care" terms. Additionally, the state analysis measurements specified by the software do not qualify stored states, and a sample is stored on every rising edge of the 80486 CLK signal.

Two common situations arise that may motivate you to modify this trace specification for a given measurement.

- First, you might want to trigger a measurement on a certain address. This can be accomplished by specifying one of the following trigger specifications:

Timing Analysis -	**CLK edge:**	**rising edge**
	ADS pattern:	**"VALID ADDRESS" symbol**
	ADDR pattern:	**desired value**
State Analysis -	**ADS pattern:**	**"VALID ADDRESS" symbol**
	ADDR pattern:	**desired value**

- Second, you might want to avoid storing states that have neither valid address nor valid data. The VALIDS label is a collection of all of the signals that describe the validity of the address and data busses. Specify a pattern, "a" for example, that has all of the labels, except for VALIDS, set to "don't care". Set the pattern on the VALIDS label to " " (the choice that is blank). This represents the pattern across the two address strobes and two ready signals where neither the address bus nor the data bus is valid. Now change the "store" terms on each sequence level of the measurement to "store 'not equal' a". All states stored will now have at least a valid address or valid data, if not both.

Time Resolution Between Modules

The HP 16500A Logic Analysis System can display measurement data from more than the current module on a single screen. For example, an HP 16515A/16516A timing analyzer can display waveforms from not only its own 1 GHz measurement, but also from a 100 MHz HP 16510A or HP 16510B timing measurement coordinated with it. This requires that the HP 16500A mainframe keep track of the time between the triggers of each of the modules that participate in an intermodule measurement.

During intermodule measurements, the 16500A Logic Analysis System can resolve time between triggers of individual modules with 10 ns resolution. This can be lowered to 1 ns resolution by probing the ADS# signal with each module and using the intermodule menu to deskew the measurement. This should be done after each measurement. For more information, refer to appendix B.

For modules that do not probe the STAT_1 (J7) or STAT_2 (J8) connectors, the ADS# signal must be probed instead of a signal normally probed by a module. In these situations, you must add a label to the format specification for the ADS# signal. Do not delete the ADS# bit from the other labels. This would force you to logically shift displayed values to interpret them correctly.

Probing Other 80486 Signals

Each logic analyzer except the HP 16540A/16541A has the ability to look at up to 20 groups of signals (called labels). The HP 16540A/16541A can look at up to 60 labels. In some configurations, there are more than 20 groups of signals that are being probed. Use the data in appendix A, "80486 Signal to HP E2403A Connector Mapping" to replace an existing label that does not apply to your measurement. Consider updating the new label's symbol table right away. Symbols often help avoid confusion about how to interpret the ones and zeros.

Using "Pattern at Marker" in Waveform Displays

You may find it convenient to use the "Pattern at Marker" feature of the waveform displays to make data interpretation easier. Select "Markers/Time." Fields appear allowing selection of a marker (X or O) and a label. Once these are set, the pattern displayed will be updated as the selected marker is moved. This feature is particularly useful when you monitor the CYCLE label (to get a description of the type of bus cycle) or the VALIDS label (to determine when the address and data busses have valid information on them).

Pattern at Marker is also used to compress a wide bus, like address or data, into a single waveform line. This gives you additional waveform lines while allowing the value to be read using "Pattern at Marker".

4

Troubleshooting

Introduction

If you encounter problems or difficulties while making measurements, use this chapter to guide you through some possible solutions. Each section in this chapter lists a problem or difficulty you may encounter, along with a possible solution.

Timing: No Activity on CLK

There is no activity on the CLK line during timing analysis:

- Make sure the CLK/STAT_1.15 switch is closed.

Timing: No Activity on ADS

There is no activity on the ADS line during timing analysis:

- Make sure the STAT_1.14 switch is closed.

"Slow or Missing Clock"

HP 16511B State:

Neither of the HP 16511B cards is receiving state clocks.

- Confirm that the CLK/DATA_L.CLK1 and CLK/STAT_1.CLK1 switches are both CLOSED.
- Confirm that the pod 5 cable from the master (upper) card is connected to connector DATA_L (J2).
- Confirm that the pod 5 cable from the expander (lower) card is connected to connector STAT_1 (J7).
- Confirm that the 80486 CLK signal (pin C3 of the 80486) is active.

HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, or HP 16540A/16541A State:

- Confirm that the CLK/STAT_1.CLK switch is CLOSED.
- Confirm that the pod 5 cable from the logic analyzer is connected to connector STAT_1 (J7).
- Confirm that the 80486 CLK signal (pin C3 of the 80486) is active.

"Slow Clock or Waiting for Arm"

This error is similar to "Slow or Missing Clock". However, if the analyzer is being armed by another machine or module, it is likely that this analyzer is waiting for its arm before it starts processing at sequence level 1. Otherwise, refer to the suggested actions for "Slow or Missing Clock".

"Waiting for Trigger"

With a don't care trigger condition for an HP 16511B state analyzer:

Only one of the two cards is receiving its state clock. Refer to the suggested actions for "Slow or Missing Clock" on the HP 16511B.

With a don't care trigger condition for an HP 16515A/16516A, HP 1650A, HP 1650B, HP 16510A, or HP 16510B timing analyzer:

Pattern duration is probably set to less than (<) instead of greater than (>). Since a "don't care" pattern is always true, the less than condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

With the HP 16540A/16541A:

If the "Waiting for Trigger" error occurs with the HP 16540A/16541A, the trigger did not occur.

"Selected File is Incompatible"

This message is displayed when you try to load a configuration file from one type of module into another type of module. For example, the message appears if you try to load an HP 16510B configuration into an HP 16511B. Files created for one type of module are generally not loadable into other module types. You can load files created from different slots or with different numbers of expansion cards into similar modules.

"Time from Arm to Trigger Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"State Clock Violates Overdrive Specification"

At least one 16 channel pod in the state analysis measurement stored a different number states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzers that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this condition. Be sure that the CLK signal meets all of the specifications regarding the shape of the signal. For the exact specifications, refer to your logic analyzer manual or data sheet.

Note

The error message "State Clock Violates Overdrive Specification" should only occur with the Clock Period set to < 60 ns. If this error message is observed with the Clock Period set to > 60 ns, or with the HP 16540A/16541A logic analyzer, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

Servicing

The repair strategy for the HP E2403A is board replacement. However, table 4-1 lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

Table 4-1. Replaceable Parts

HP Part Number	Description
E2403-66501	Circuit Board
1200-1512	Pin Protectors
01650-63203	100 kOhm Termination Adapters

A

80486 Signal to HP E2403A Connector Mapping

The following table describes the electrical interconnections implemented with the HP E2403A Universal Interface board. For interconnection information on the DIP switch or post connector, refer to chapter 1 of this manual.

Table A-1. 80486 to HP E2403A Interconnections

80486 Signal	80486 Pin	Connector Name	Connector Designator	Connector Pin #	Pod Bit #
CLK	C3	STAT_1	J7	3	Clk1 *
CLK	C3	STAT_1	J7	4	15 *
ADS#	S17	STAT_1	J7	5	14 *
RDY#	F16	STAT_1	J7	6	13
BRDY#	H15	STAT_1	J7	7	12
BLAST#	R16	STAT_1	J7	8	11
KEN#	F15	STAT_1	J7	9	10
BS8#	D16	STAT_1	J7	10	9
BS16#	C17	STAT_1	J7	11	8
HLDA	P15	STAT_1	J7	12	7
BE3#	F17	STAT_1	J7	13	6
BE2#	J15	STAT_1	J7	14	5
BE1#	J16	STAT_1	J7	15	4
BE0#	K15	STAT_1	J7	16	3
M/IO#	N16	STAT_1	J7	17	2
D/C#	M15	STAT_1	J7	18	1
W/R#	N17	STAT_1	J7	19	0
Vss	E17	STAT_1	J7	20	gnd

* These signals are connected through switch S1.

Table A-1. 80486 Signals to HP E2403A Interconnections (Continued)

80486 Signal	80486 Pin	Connector Name	Connector Designator	Connector Pin #	Pod Bit #
RESET	C16	STAT_2	J6	4	15
ADS#	S17	STAT_2	J6	5	14 *
NMI	B15	STAT_2	J6	6	13
INTR	A16	STAT_2	J6	7	12
BOFF#	D17	STAT_2	J6	8	11
HOLD	E15	STAT_2	J6	9	10
BREQ	Q15	STAT_2	J6	10	9
EADS#	B17	STAT_2	J6	11	8
AHOLD	A17	STAT_2	J6	12	7
PLOCK#	Q16	STAT_2	J6	13	6
LOCK#	N15	STAT_2	J6	14	5
PCHK#	Q17	STAT_2	J6	15	4
DP3	A5	STAT_2	J6	16	3
DP2	H3	STAT_2	J6	17	2
DP1	F1	STAT_2	J6	18	1
DP0	N3	STAT_2	J6	19	0
Vss	P17	STAT_2	J6	20	gnd
A15	R7	ADDR_L	J5	4	15
A14	S5	ADDR_L	J5	5	14
A13	Q10	ADDR_L	J5	6	13
A12	S7	ADDR_L	J5	7	12
A11	R12	ADDR_L	J5	8	11
A10	S13	ADDR_L	J5	9	10
A9	Q11	ADDR_L	J5	10	9
A8	R13	ADDR_L	J5	11	8

* These signals are connected through switch S1.

Table A-1. 80486 Signals to HP E2403A Interconnections (Continued)

80486 Signal	80486 Pin	Connector Name	Connector Designator	Connector Pin #	Pod Bit #
A7	Q13	ADDR_L	J5	12	7
A6	S15	ADDR_L	J5	13	6
A5	Q12	ADDR_L	J5	14	5
A4	S16	ADDR_L	J5	15	4
A3	R15	ADDR_L	J5	16	3
A2	Q14	ADDR_L	J5	17	2
Vss	S11	ADDR_L	J5	18	1
Vss	S10	ADDR_L	J5	19	0
Vss	S14	ADDR_L	J5	20	gnd
PWT	L15	STAT_3	J4	14	5
PCD	J17	STAT_3	J4	15	4
FERR#	C14	STAT_3	J4	16	3
IGNNE#	A15	STAT_3	J4	17	2
A20M#	D15	STAT_3	J4	18	1
FLUSH#	C15	STAT_3	J4	19	0
Vss	S12	STAT_3	J4	20	gnd
A31	Q1	ADDR_H	J3	4	15
A30	P3	ADDR_H	J3	5	14
A29	P2	ADDR_H	J3	6	13
A28	R1	ADDR_H	J3	7	12
A27	S1	ADDR_H	J3	8	11
A26	S2	ADDR_H	J3	9	10
A25	R2	ADDR_H	J3	10	9
A24	Q6	ADDR_H	J3	11	8
A23	S3	ADDR_H	J3	12	7
A22	Q7	ADDR_H	J3	13	6
A21	Q5	ADDR_H	J3	14	5
A20	Q8	ADDR_H	J3	15	4

Table A-1. 80486 Signals to HP E2403A Interconnections (Continued)

80486 Signal	80486 Pin	Connector Name	Connector Designator	Connector Pin #	Pod Bit #
A19	Q4	ADDR_H	J3	16	3
A18	R5	ADDR_H	J3	17	2
A17	Q3	ADDR_H	J3	18	1
A16	Q9	ADDR_H	J3	19	0
Vss	S8	ADDR_H	J3	20	gnd
CLK	C3	DATA_L	J2	3	Clk1 *
D15	F3	DATA_L	J2	4	15
D14	K3	DATA_L	J2	5	14
D13	D2	DATA_L	J2	6	13
D12	G3	DATA_L	J2	7	12
D11	C1	DATA_L	J2	8	11
D10	E3	DATA_L	J2	9	10
D9	D1	DATA_L	J2	10	9
D8	F2	DATA_L	J2	11	8
D7	L3	DATA_L	J2	12	7
D6	L2	DATA_L	J2	13	6
D5	J2	DATA_L	J2	14	5
D4	M3	DATA_L	J2	15	4
D3	H2	DATA_L	J2	16	3
D2	N1	DATA_L	J2	17	2
D1	N2	DATA_L	J2	18	1
D0	P1	DATA_L	J2	19	0
Vss	Q2	DATA_L	J2	20	gnd
D31	B8	DATA_H	J1	4	15
D30	C9	DATA_H	J1	5	14
D29	A8	DATA_H	J1	6	13
D28	C8	DATA_H	J1	7	12

* These signals are connected through switch S1.

Table A-1. 80486 Signals to HP E2403A Interconnections (Continued)

80486 Signal	80486 Pin	Connector Name	Connector Designator	Connector Pin #	Pod Bit #
D27	C6	DATA_H	J1	8	11
D26	C7	DATA_H	J1	9	10
D25	B6	DATA_H	J1	10	9
D24	A6	DATA_H	J1	11	8
D23	A4	DATA_H	J1	12	7
D22	A2	DATA_H	J1	13	6
D21	B2	DATA_H	J1	14	5
D20	A1	DATA_H	J1	15	4
D19	B1	DATA_H	J1	16	3
D18	C2	DATA_H	J1	17	2
D17	D3	DATA_H	J1	18	1
D16	J3	DATA_H	J1	19	0
Vss	M1	DATA_H	J1	20	gnd

B

Intermodule Measurements

Introduction

To monitor all of the signals available on the universal interface, it may be necessary to use multiple HP 16515A/16516A, HP 16510A, or HP 16510B analyzer modules. This appendix explains how to use the Intermodule menu of the HP 16500A Logic Analysis System to make intermodule measurements between these modules.

The basic functions of the HP 16500A Intermodule menu give you the ability to do the following:

- Configure modules to run simultaneously.
- Set up arming sequences between modules.
- Adjust skew between modules.
- Synchronize with external equipment.
- Display resulting waveforms and state listings for several modules together on one screen.

For more information on Intermodule measurements, refer to the *HP 16500A Reference Manual*.

Defining an Intermodule Measurement

Intermodule measurements are set up in the Intermodule menu of the HP 16500A by arranging the modules for the needed intermodule sequences. Each module may be used only once and any unused modules will run independently of the intermodule measurement.

Selecting the Intermodule Menu

To select the Intermodule menu:

1. Touch the module field (System) in the upper-left corner of the display.
2. When the pop-up appears, touch **Intermodule** to bring up the Intermodule menu.

Defining the Arming Sequence

After entering the Intermodule menu, an arming sequence can be defined for the desired measurement. The arming sequence is displayed graphically as a tree with the large Group Run field at the base. Two options are available for the large Group Run field:

- Group Run - The intermodule measurement is armed immediately after the Group Run/Stop field in the upper-right corner is touched.
- Group Run Armed from PORT IN - After the Group Run/Stop field in the upper-right corner is touched, the intermodule measurement is armed from an external signal input through the BNC connector on the rear panel of the HP 16500A mainframe.

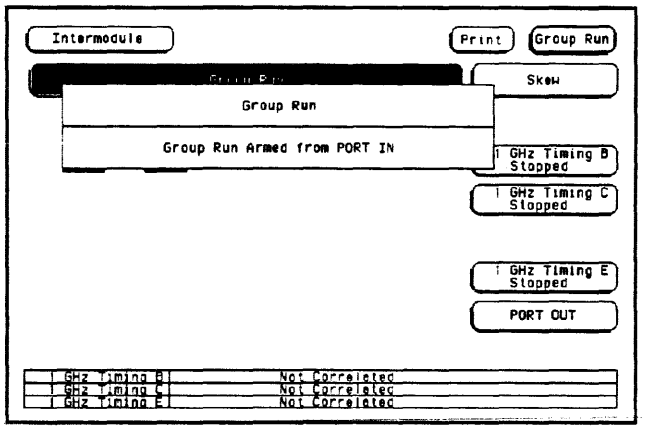


Figure B-1. Group Run Pop-Up

From the large Group Run field, the intermodule arming sequence is built as the modules on the right of the menu are added to the configuration. When one of the module fields is touched, a pop-up appears displaying the possible locations for the module in the arming sequence:

- **Independent** - allows the module to run independently of the other modules and removes it from the arming sequence.
- **Group Run** - places the module directly below the large Group Run field. If the large Group Run field is set to Group Run, the module is armed immediately after the Group Run/Stop field in the upper-right corner is touched. If the large Group Run field is set to Group Run from Port In, the module is armed after the Group Run/Stop field in the upper-right corner is touched and an arming signal is received via the PORT IN BNC on the rear panel of the HP 16500A mainframe.
- Other modules - touching one of these fields places the current module below a module that is already part of the arming sequence. The current module is armed when the preceding module is triggered.

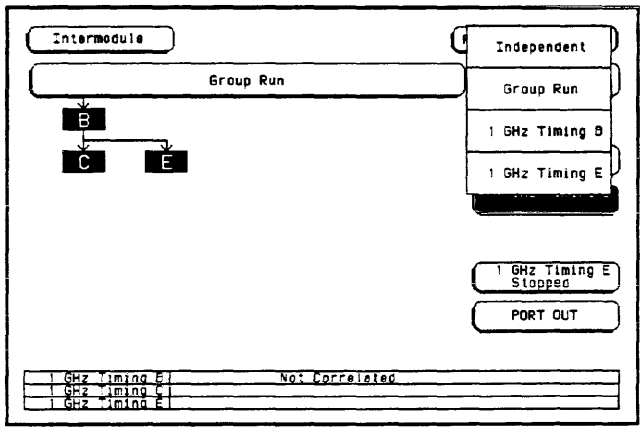


Figure B-2. Module Pop-Up

Note

The letters A, B, C, D, or E in the boxes that make up the intermodule arming sequence represent the slot location for the corresponding module.

As soon as an intermodule arming sequence contains at least one module, the PORT OUT field appears on the lower right side of the screen. PORT OUT refers to the PORT OUT BNC on the rear panel of the HP 16500A mainframe. This feature can be used to arm external equipment.

The pop-up menu for the PORT OUT field allows you to turn off PORT OUT or place PORT OUT below a module in the arming sequence. When PORT OUT is part of the arming sequence, a TTL signal is output through the PORT OUT BNC on the rear panel when the preceding module is triggered. For more information on PORT OUT, refer to the *HP 16500A Reference Manual.*

Running an Intermodule Measurement

When an intermodule arming sequence contains at least one module, the Group Run/Stop field appears in the upper-right corner of the Intermodule menu. Additionally, the Run/Stop field for each module in the arming sequence changes to Group Run/Stop. This allows the intermodule measurement to be started or stopped from either the Intermodule menu or any module in the intermodule arming sequence.

If you touch and hold the Group Run/Stop field, a pop-up appears with your choices for acquiring data.

- Single, which is the default, allows you to run the measurement once.
- Repetitive allows you to run the measurement as many times as you want to collect data for statistical measurements, etc. Press Stop when you want to stop collecting data.
- Cancel allows you to cancel the measurement.

Note

You must select the Single, Repetitive, or Cancel while you are still touching the Group Run/Stop field. Releasing the Group Run/Stop field before making your selection or without changing the current selection results in the instrument running the measurement according to the last input to this field.

When an intermodule measurement is started, the following sequence of events occurs:

1. The status indicators that appear below the names of the modules in the Intermodule menu change to Running for each module involved.
2. The status of modules that appear below other modules is checked until their pre-store qualifications are satisfied.
3. When the pre-store qualifications of the lower modules are satisfied, the modules that appear directly below the large Group Run field are armed and their appropriate measurements are run.
4. When the upper modules trigger, the modules below them are simultaneously armed.
5. When a module completes its measurement, the module's status changes to Stopped.
6. When all of the modules involved in the intermodule measurement have completed their measurements, the time correlation bars at the bottom of the Intermodule menu display the start and stop acquisition window of each module relative to the other modules.

Note

For State analysis, the Count field of the State/Timing analyzer Trace menu must be set to Time for proper time correlation.

Displaying Multiple Module Data on One Screen

When all of the modules involved in the intermodule measurement have completed their measurements, the data for each module is displayed in the individual waveform or display menus of the modules. However, you can display the resulting waveforms or state listings for several modules together on one screen if the data is correlatable. Correlatability requires the following:

- Each module records the time between samples. For state analyzers, the Clock Period field in the Format menu must be set to >60 ns and the Count field in the Trace menu must be set to Time.
- The HP 16500A mainframe records the time between the triggers of each module. This is done automatically for all modules involved in an intermodule measurement.

To display the waveform data for multiple timing modules:

1. Touch the module field in the upper-left corner of the screen.
2. When the pop-up appears, select one of the modules that you want to be included in the display.

Note 

Before you select the module, consider any waveforms which may need to be examined with markers. Pattern at Marker, Markers/Pattern, and Markers/Statistics are only valid for waveforms in this current module. They are not available for waveforms brought in from other modules. Markers/Time is valid for all waveforms.

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3. When the menu appears, select the Waveforms menu.
4. Touch the channel label field to the left of the waveform display.
5. When the Waveform Selection pop-up appears, delete any unwanted labels from the display.
6. If the label you want to add is not in the current module, touch the field displaying the current module.

7. Select the appropriate module from the pop-up menu. After the pop-up disappears, the labels for the channels of the selected module will be listed on the left side of the Waveform Selection pop-up.
8. Modify the Channel Mode (Individual, Sequential, or Overlay) if necessary.
9. Touch the label for the channel that you want displayed.
10. Repeat steps 6 through 9 as needed for other labels.
11. Touch DONE and the Waveform Selection pop-up will disappear, allowing you to view the waveforms.

It is also possible to view timing waveforms from different modules with a state listing on the same screen. However, the following steps must be taken before running the measurement:

1. Configure a State/Timing module so that one of the analyzers is a timing analyzer and the other is a state analyzer.
2. Assign at least one pod to each analyzer.
3. Set the Count field in the Trace menu of the state analyzer to Time.

Note 

The sample clock for the state analyzer must have a period of greater-than 60 ns (a frequency of less-than 16.67 MHz) to view the state listing and timing waveforms on the same screen.

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4. Include the State/Timing module in the arming sequence of the intermodule measurement.
5. Run the intermodule measurement.

After completing the previous steps, the state listing can be displayed with the timing waveforms by performing the following steps:

1. Select the appropriate State/Timing module.
2. Enter the Mixed Display menu to view the state listing with the timing waveforms.
3. Configure the timing waveform section of the screen to display signals from any timing module included in the intermodule measurement.

Deskewing an Intermodule Measurement

The data from different modules involved in an intermodule measurement may be skewed from one module to another. This skew is the result of several variables:

- Delays from the time that a module receives an arming signal to the time that the module is actually armed.
- Delays from the time the module is triggered to the time that the module generates an arming signal for other modules.
- The 10 ns resolution with which the time between module triggers is recorded.

To deskew data from multiple module, perform the following steps:

1. Probe a common signal with each analyzer in the measurement.
2. Select the Skew menu of the Intermodule menu and set the skew value for each module to zero.
3. Run the intermodule measurement.
4. Display the common signal inputs from each module together on a single display.
5. Adjust the Delay and s/Div as needed to show the same transition (rising edge or falling edge) of the signal from each module.
6. Choose a reference module and place the O marker on the selected transition of the reference signal for this module. The skew for this module will be 0 s.

7. Place the X marker on the same transition of the reference signal for one of the other modules. The value shown in the X to O field is the amount of skew for that module.
8. Select the Intermodule menu and touch the Skew field in the upper-right corner of the menu.
9. Select the field displaying the name of the module measured in step 7.
10. Enter the value of skew that was displayed in the X to O field.
11. After entering the value, touch Done.
12. Repeat steps 7 through 11 for each module.

Note 

Since the skew value for each module will vary each time the measurement is run, the deskewing process should be repeated after each measurement.

Typical Intermodule Measurements with the HP E2403A

Increasing Channel Count for Timing Analyzers

Although the HP 16515A/16516A provides you with 32 channels of 1 GHz timing analysis, more channels might be desirable in some situations. In this example, a 1 GHz timing measurement is made across the address bus and all status signals. To deskew these modules after the measurement is run, you must probe a common signal with both analyzers. ADS# is provided for this purpose, but the module probing the address bus, as configured by file UI_486_08, does not normally probe the ADS# signal. As a result, the channel that normally probes the least significant bit of the address bus will be used to probe ADS#, and the configuration of the module will be modified. The measurement is triggered on some specified address.

The following procedure describes the basic steps involved in making a measurement with two HP 16515A/16516A analyzers:

1. Install two sets of HP 16515A/16516A timing analyzers (a total of four cards) with the masters in slots B and D of an HP 16500A Logic Analysis System.

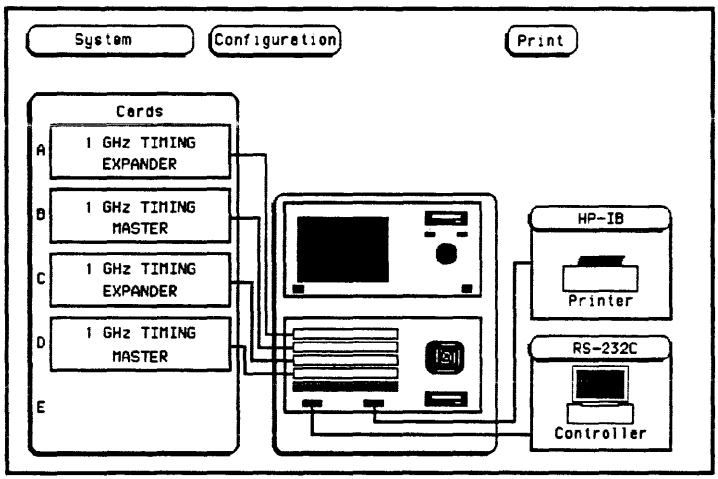

Figure B-3. HP 16500A System Configuration Menu

2. Load the configuration file UI_486_08 into the 1 GHz Timing Analyzer in slot B.

3. Load the configuration file UI_486_10 into the 1 GHz Timing Analyzer in slot D.

4. Select the Format menu for 1 GHz Timing Analyzer in slot B and add the label ADS_B, for the correlation reference signal.

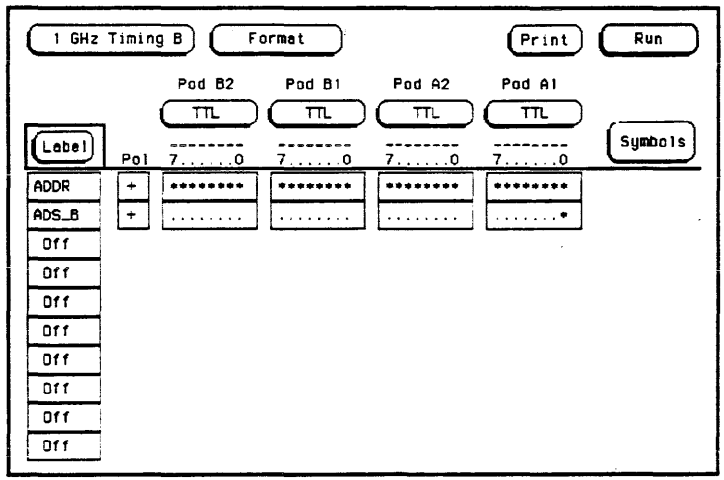

Figure B-4. Format Specification

5. Define the label ADS_B to contain bit 0 of Pod A1.
6. Set the switches on the universal interface board to the appropriate position. For more information, see "Switch Settings" on page 2-7 of chapter 2.
7. Install the universal interface board in the target system.
8. Connect the 1 GHz Termination Adapters to the timing analyzers, but leave the probe for bit 0 of Pod A1 disconnected.
9. Connect the 1 GHz Termination Adapters to the universal interface board as described in table 2-1.
10. Connect the probe for bit 0 of Pod A1 to the post connector J8 on the universal interface board. Be careful to observe the polarity of the probe and connector.

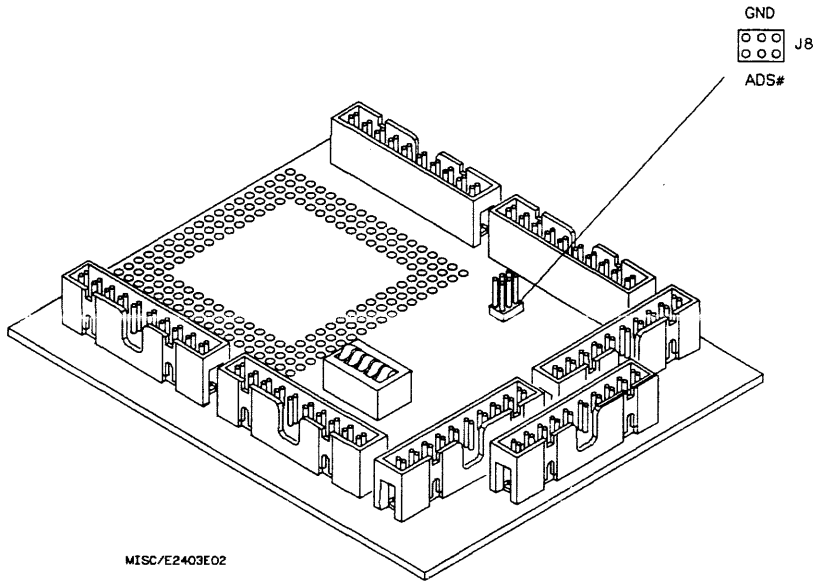

Figure B-5. Connector J8 on the HP E2403A

11. Select the Intermodule menu.
12. Place the 1 GHz Timing Analyzer in slot B under the large Group Run field.
13. Place the 1 GHz Timing Analyzer in slot D under the 1 GHz Timing Analyzer in slot B.

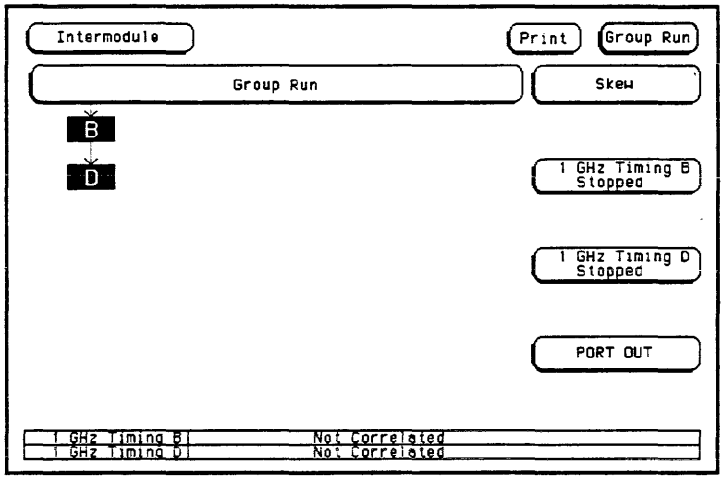

Figure B-6. HP 16500A Intermodule Menu

14. Select the Trace menu for the 1 GHz Timing Analyzer in slot B.
15. Set the trigger pattern to the desired value of ADDR with the least significant bit as an X ("don't care").
16. Specify the pattern for ADS as 0.

Note The trigger pattern for the 1 GHz Timing Analyzer in slot D is defined by the configuration file UI_486_10 as all "don't care" terms. This will allow the module to trigger immediately after it is armed by 1 GHz Timing Analyzer in slot B.

---

17. Touch the Group Run field in the upper-right corner to run the measurement.
18. Enter the Waveforms menu for the 1 GHz Timing Analyzer in slot D.
19. Display the ADS_B waveform from the 1 GHz Timing Analyzer in slot B.

20. Select Markers/Time, and place the O marker on the rising edge of the ADS waveform of the 1 GHz Timing Analyzer in slot D.

21. Place the X marker on the rising edge of the ADS_B waveform of the 1 GHz Timing Analyzer in slot B.

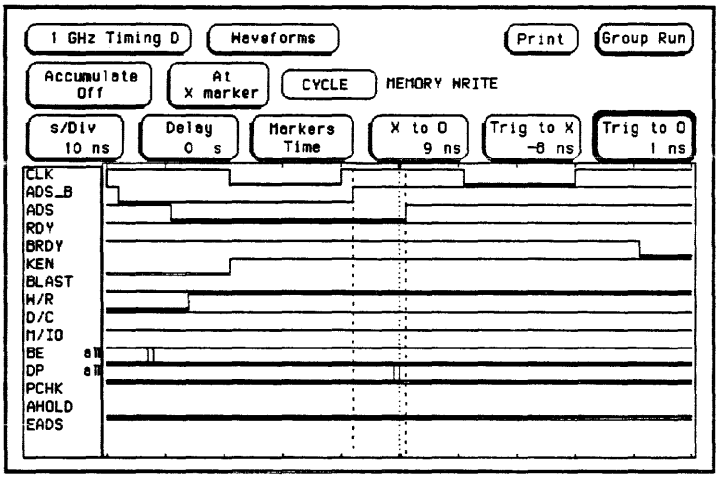

Figure B-7. Waveforms Menu

22. Record the skew value for the 1 GHz Timing Analyzer in slot B. This value is displayed in the X to O field.

23. Select the Intermodule menu, and touch the Skew field in the upper-right corner.

24. Touch the field displaying 1 GHz Timing B.

25. Enter the skew value for the 1 GHz Timing Analyzer in slot B.

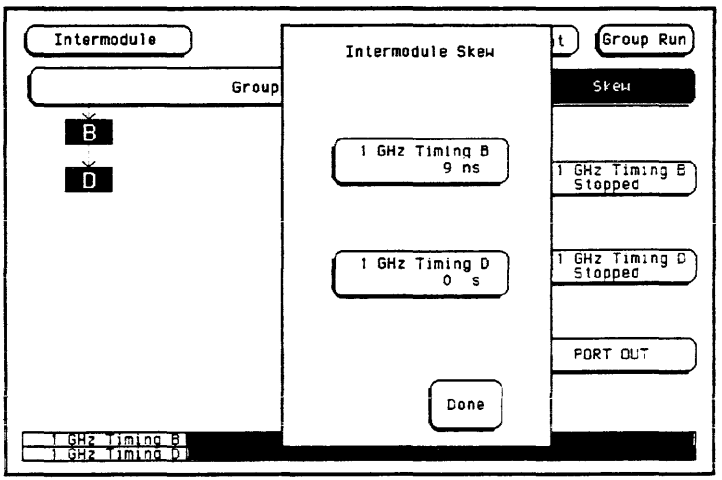

Figure B-8. Intermodule Skew Menu

26. Select the Waveforms menu for the 1 GHz Timing Analyzer in slot D. The waveforms for ADS and ADS_B should now be deskewed.

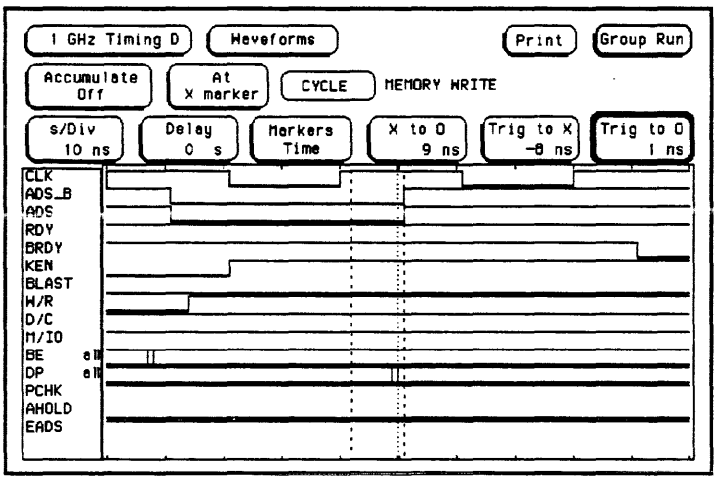

Figure B-9. Waveforms Menu

27. Configure the display to show all of the waveforms required for your measurement. You can now make time interval measurements across both 1 GHz timing analyzers with less than 2 ns resolution (1 ns resolution of 1 GHz timing analyzer plus 1 ns of resolution of the skew value).

Triggering a Timing Measurement on a State Condition

In the previous example, a 1 GHz Timing analysis measurement is made on the status lines when a specified address occurs. All 64 channels can be correlated to within 2 ns so that any 2 signals can be compared with 2 ns accuracy. However, you might not need to observe the address bus as part of the displayed data. In this example, a 1 GHz timing measurement is made on the status signals when a state analyzer (the HP 16510B) is triggered on a specified address. The following procedure describes the basic steps involved in making this measurement.

1. Install an HP 16515A/16516A 1 GHz Timing Analyzer in the HP 16500A mainframe with the master in slot B.
2. Install an HP 16510B Logic Analyzer in slot E of the HP 16500A mainframe.

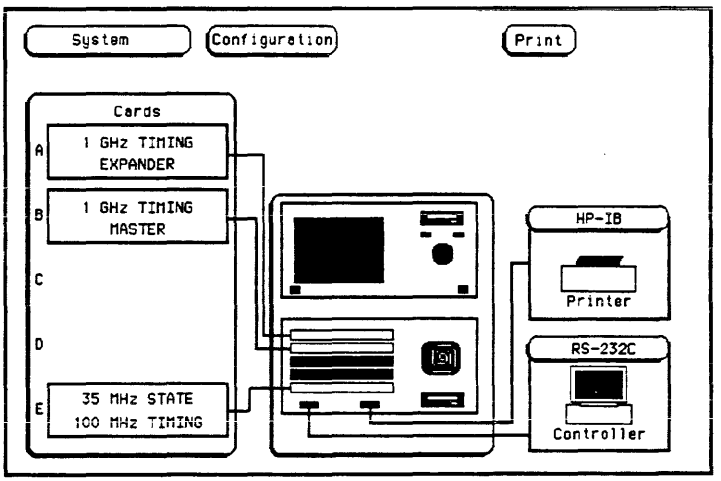

Figure B-10. HP 16500A System Configuration Menu

3. Load the configuration file UI_486_10 into the 1 GHz timing analyzer in slot B.
4. Load the configuration file UI_486_15 into the logic analyzer in slot E.

5. Set the switches on the universal interface board to the following positions:

Signal	Switch	Position
CLK	DATA_L.CLK1	open
CLK	STAT_1.CLK1	closed
CLK	STAT_1.15	closed
ADS#	STAT_1.14	closed
ADS#	STAT_2.14	closed

   This is a combination of the switch settings for the two configuration files used in this example. For more information, see "Measurement Configurations" in chapter 2.

6. Connect a general purpose lead set (HP part number 01650-61608) to Pod E5.

7. Connect the probe for bit 14 of Pod E5 to the post connector J8 on the universal interface board. Be careful to observe the polarity of the probe and connector. A label for ADS is already defined by the configuration file UI_486_15 as bit 14 of Pod E5.

8. Install the universal interface board in the target system.

9. Connect 1 GHz Termination Adapters to the 1 GHz timing analyzer.

10. Connect 100 kOhm Termination Adapters to Pod E1, Pod E3, and Pod E4 of the HP 16510B Logic Analyzer. Pods E3 and E4 will be used to probe the ADDR_L and ADDR_H connectors. Pod E1 will probe connector DATA_L to bring in the CLK signal. Pod E2 will not be used in this measurement.

11. Connect the three 100 kOhm Termination Adapters to the universal interface board as described in table 2-4 for the configuration file UI_486_15.

12. Connect the two 1 GHz Termination Adapters to the universal interface board as described in table 2-1 for the configuration file UI_486_10.

13. Select the Intermodule menu.

14. Place the logic analyzer in slot E under the large Group Run field.

15. Place the 1 GHz timing analyzer in slot B under the logic analyzer in slot E.

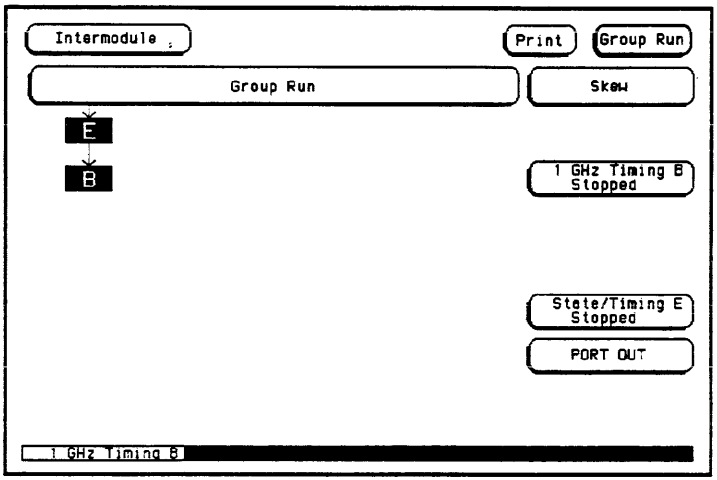

Figure B-11. HP 16500A Intermodule Menu

16. Select the State/Timing E Format menu.

17. Change the active clock edge from rising N clock to rising J clock.

18. Enter the Trace menu for the logic analyzer in slot E.

19. Set the trigger pattern to the desired value of ADDR, and specify the pattern for ADS as the symbol "VALID ADDRESS."

Note 

The trigger pattern for the 1 GHz timing analyzer in slot B is defined by the configuration file UI_486_10 as all "don't care" terms. This will allow the module to trigger immediately after it is armed by the logic analyzer in slot E.

---

20. Touch the Group Run field in the upper-right corner to run the measurement.

21. Enter the Waveforms menu for 1 GHz timing analyzer in slot B to view the timing waveforms.

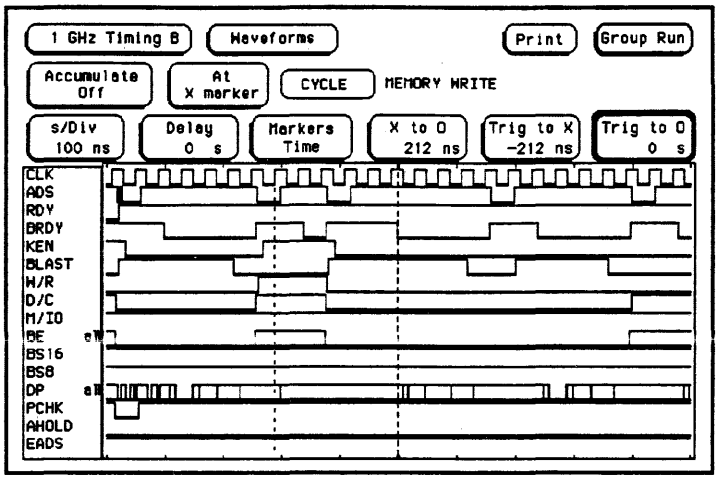

Figure B-12. Waveforms Menu

Due to pipelining in the HP 16510B logic analyzer, the arming of the 1 GHz timing analyzer is delayed with respect to the trigger point of the HP 16510B. As a result, the trigger point for the 1 GHz timing analyzer shown in the waveform display actually occurs after the specified address triggered the HP 16510B. The approximate delay is determined by the setting of the Clock Period field in the Format menu of the HP 16510B.

If the Clock Period field is set to < 60 ns, the delay equals the time elapsed during the 4 state samples immediately following the state trigger (4 CLK cycles in this example) plus 50 ns.

If the Clock Period field is set to > 60 ns, the delay equals 200 ns to 240 ns.

In this example, the Clock Period field is set to < 60 ns, so the delay equals the time elapsed during the 4 state samples immediately following the state trigger (4 CLK cycles) plus 50 ns. Each CLK cycle equals 40 ns, so the delay equals 4 times 40 ns plus 50 ns.

Delay = 4(40 ns) + 50 ns = 210 ns

To find the exact trigger point of the HP 16510B, locate the nearest rising edge of the 80486 CLK signal 210 ns before the 1 GHz timing analyzer trigger where ADS is low.

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