HEWLETT-PACKARD

HP-HIL

Technical

Reference Manual

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HEWLETT PACKARD
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First Edition.....January 1986

PREFACE

This manual provides detailed technical information on the Hewlett-Packard Human Interface Link (HP-HIL), what the system capabilities and protocols are, and gives design hints. It is intended to aid in the development of HP-HIL hardware and software products which become part of, or work in conjunction with HP's personal computers and CPUs.

Refer to the documentation supplied with your HP personal computer for more information on related HP-HIL products.

User Level: Use of this information assumes a background in hardware logic and programming. To design HP-HIL hardware, you should be knowledgeable in the areas of RFI, EMI, and product safety regulations. Also, you should be knowledgeable about appropriate grounding, shielding, and electrostatic discharge techniques.

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Proprietary ICs: The integrated circuits which are the hardware basis of HP-HIL are proprietary. They are available ONLY to organizations which have OEM relationships with an HP division capable of supporting HP-HIL development activities. Organizations interested in HP-HIL projects for specific HP computers should write the marketing department of the HP division responsible for that product.

Support: Because of the specialized nature of this information and the importance of design strategy for successful implementation of products at this level, assistance in the use of this manual is provided through local consulting. Contact your local HP Sales and Service Office -- ask for Personal Computer Systems Engineering.

MANUAL OVERVIEW

This manual consists of the following sections and appendices:

Section 1 - Introduction provides an overview of HP-HIL.

Section 2 - Interface Specifications provide HP-HIL specifications and information for systems, devices, cables, and connectors.

Section 3 - HP-HIL Hardware contains detailed information on HP-HIL system and device hardware. Also included are HP-HIL hardware design recommendations.

Section 4 - HP-HIL Protocol provides information on HP-HIL commands, basic Link operation, device characteristics, and advanced features.

Appendix A - HP-HIL Command Reference contains HP-HIL commands and detailed functional descriptions.

Appendix B - Device ID Byte provides a list of HP-HIL device ID numbers and keyboard localization information.

Appendix C - Describe Record provides a detailed discussion of the data associated with the IDD command.

Appendix D - Extended Describe Record provides a detailed description of the data associated with the EXD command.

Appendix E - Poll Record provides a detailed description of the data associated with the POL command.

Appendix F - HP-HIL Character Set Definitions provide keycode listings for keyboards. An ASCII reference table is included.

Appendix G - Write Register Record provides a detailed description of the data associated with the WRG command.

Appendix H - Report Security Code Record provides a detailed description of the data associated with the RSC command.

Appendix I - HP-HIL Master Link Controller Data Sheet provides specifications for the HP-HIL Master Link Controller chip.

Appendix J - HP-HIL Slave Link Controller Data Sheet provides specifications for the HP-HIL Slave Link Controller chip.

Appendix K - Glossary of Terms defines HP-HIL terminolgy used in this document.

Index - Provides an alphabetic listing of the items covered in this manual.

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

INTRODUCTION

SECTION 1

OVERVIEW

The Hewlett-Packard Human Interface Link (HP-HIL), is the Hewlett-Packard standard interface for linking human-input devices with a Host computer or terminal (hereafter referenced as the Host or System). HP-HIL is an intelligent interface which supports a single input device or multiple input devices. The protocol simplifies device connection so that the user does not have to worry about configuring the Host, setting switches correctly, or hunting for an I/O slot or port. The user may connect one or several different types of input devices, in any order. A typical HP-HIL System is shown in Figure 1-1.

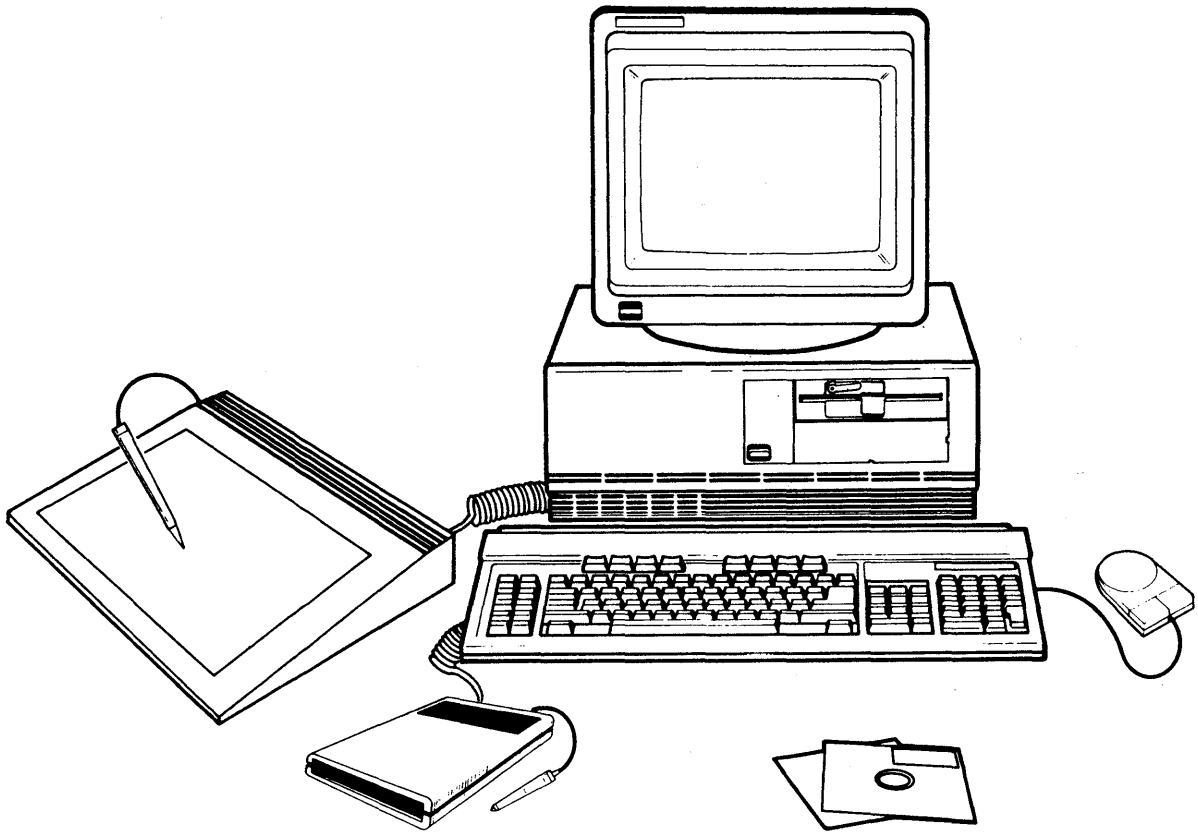


Figure 1-1. A Typical HP-HIL System

The interface hardware is built around two HP standard integrated circuits which support the HP-HIL protocol. The Master Link Controller (MLC) integrated circuit serves as the Link controller, and interfaces to the Host microprocessor. The Slave Link Controller (SLC), is incorporated into each HP-HIL input device, serving as the HP-HIL interface to the device microprocessor. Devices are interconnected via four-conductor, shielded cables which provide power, ground, data in, and data out lines optimized for Electro-Static Discharge (ESD) immunity and low Radio Frequency Interference (RFI) levels. Since the Host supplies power to the devices through the interface cable, the HP-HIL input devices are smaller, simpler, and cheaper. Also, there are no power cords, simplifying cable management.

What is HP-HIL?

As its name implies, HP-HIL is used for linking input devices to a system. Typically, the System will be a single user workstation, personal computer, portable computer, or desktop computer. To accommodate these systems, HP-HIL was designed for flexibility, ease of use, and low cost. First, the user can connect a single or multiple devices in a linked (daisy-chained) connection. This allows the user to add input devices to the System at any time without worrying about ports, I/O slots, or option cards. Second, because HP-HIL does not require special configuration by the user when devices are added or taken away from the Link, it becomes very easy for the user to tailor the System for maximum ease of use. Third, HP-HIL was integrated such that only two ICs (processor and communications ICs) are needed to handle the interface protocol in a system or a device.

The HP-HIL protocol and hardware have been designed for efficient data collection from a variety of input devices. Typical input devices are used to provide the Host with character, position, or status information.

Character data is used to describe a variety of input device reports. Devices such as keyboards return data in the form of keyswitch transitions. A typical key press results in the keyboard reporting a down transition for that particular key, followed by an up transition when the key is released. Several different keycode sets are supported by HP-HIL. ASCII characters may come from a barcode reader. Other types of character data, such as binary data, are also accommodated.

Position information may be reported as either absolute coordinates or movement relative to a previous position. Digitizing tablets and touchscreens are absolute positioners. They return return absolute coordinates where the position of the stylus or finger is fixed with respect to a known origin. The mouse or trackball, on the other hand, does not possess a fixed coordinate system, and reports data instead in units of distance traveled from the previous position, with no assumed origin. Mice and trackballs are commonly referred to as relative positioners.

Status information consists of device capabilities (resolution information, special command support, read/write register support, etc.), a device name, or

status bytes which are specific for a particular device. Generally, status information is any information which is not position or character data.

Both absolute and relative positioners also typically report a special type of keyswitch known as a "button". Devices report down and up transitions for up to seven different buttons. An eighth button with less general application is defined as "proximity in/out". The HP 150C Touchscreen device reports "proximity in" when a finger or other object enters its active area and "proximity out" when the object is removed. Tablets use proximity to indicate that the stylus or cursor is sufficiently close to the tablet surface to determine its position.

Data collection from these devices typically occurs at 60 Hz which is sufficient for human input, i.e., cursors and characters can be updated quickly enough so that a speed or time lag is not detectable by the user.

Although designed for data collection, HP-HIL can be used for data output in special applications. Data is reported and transmitted over the Link such that different functions can reside in a single physical device. For example, a keyboard could have LEDs and an audible transducer as part of the design. The LEDs and transducer are actually for output, so this example keyboard would have both input (keys) and output (LEDs and speaker) capabilities.

HP-HIL is not suitable for long distance data transmission (e.g. RS-232 or RS-422) nor is it suitable for high speed data collection as might be used with instrumentation. It is not intended for networking multiple CPUs and is not to be confused with HP-IL (Hewlett-Packard Interface Loop) or HP-IB (Hewlett-Packard Interface Bus). HP-IL and HP-IB are distinct and separate interfaces with different applications. HP-HIL is superior for interfacing human speed input devices to workstations or other systems.

Scope of this Document

This document covers all aspects of the HP-HIL System interface specifications, hardware design, and software/firmware specifications. Included in the appendices are detailed information on HP-HIL commands, data records, HP-HIL standard ICs, and a glossary of terms used in this manual.

Purpose of this Document

The HP-HIL Technical Reference Manual is intended to provide complete technical information needed for System and device development. It will serve as the interface specification for anyone developing or working with HP-HIL applications or HP-HIL devices.

WHY HP-HIL?

Proliferation of Input Devices

During recent years, there has been a major increase in the use of personal computers (PCs) and a corresponding increase in the diversity of their application. As PCs have become more powerful, flexible, and capable of processing data faster, many applications which were found only on large, dedicated, and expensive systems have now moved into the realm of PCs. One such area is graphics and CAD applications. There are now many general purpose drafting, design, schematic preparation, printed circuit layout, and other graphics programs available for many different PCs.

Along with the increase of graphics application software on PCs has been an increased need for devices which facilitate pointing, locating, selecting, or moving objects within these applications. Cursor keys located on the keyboard were typically used in the past, but now users demand a more ergonomic interface which allows for easy and quick interaction with a machine or application.

The most common devices to emerge which are used today with graphics (and alpha) based applications are graphics tablets (digitizers), mice, joysticks, trackballs, and variations thereof. Although there is a large number of devices available, the devices have their own unique characteristics, applications, benefits, and of course, drawbacks.

For example, a graphics tablet is an absolute device whereas a mouse is a relative device. Both can be used for menu selection, drawing, etc. However, for accurate drawing or digitizing, a graphics tablet is superior, but it is more expensive than a mouse. Eventually, the experienced user discovers that there is no one input device that does everything. The most desirable setup is to have several different input devices on the same system so that the preferred input device is available for the job. This is further reinforced by the fact that PCs are used for many different jobs.

Common Hardware System Connection Difficulties

A user can be faced with many challenges when trying to connect multiple devices to a system (PC). First, there has to be a dedicated I/O port for each device. This means adding additional RS-232 I/O and/or "black boxes" to the PC to support the input devices. Adding I/O cards may be a limitation in itself. If I/O card slots are limited, then so will be the number of input devices which can be attached. Adding I/O cards usually implies some disassembly of the unit, which some users will not want to attempt. Second, when the I/O cards are installed, and the devices attached, the configuration process begins. This means the user will have to read documentation to determine what and how baud rates and/or dip switches should be set. This can be one of the most frustrating aspects of PCs. Third, if the user is limited on the number of devices he can attach, then to alternate between different devices can be an exercise in repeating much of the above. If available RS-232 ports are used, the user may not be able to have more than one of the devices active at a time. So again to switch between devices, some reconfiguration may be necessary. Fourth, the physical connection of multiple devices can become very cumbersome. Most devices require their own external power source which means an AC line cord in addition to the interface cable for the device. Thus the issue of cable management and workspace congestion develops.

Common Software Interface Difficulties

There are three areas where communications between applications and input devices are often less than optimal. First, input devices typically have different data reporting formats for a given set of devices. What this means is that for an application to support a variety of devices requires the drivers to support a variety data formats and reporting methods. Thus the device driver(s) for an application becomes large and complex. Second, device hardware connections usually do not report to the device driver the device type and its characteristics. This information is usually in a config menu. If the user wants to change devices, then the config menu must be changed. Third, because the hardware connections to the input devices are ususally varied, the device drivers are not able to support multiple devices operating at the same time.

Ergonomic Considerations

Many input devices offered today are less than ideal for their ease of use. Because most input devices have to be connected to an option card, the actual cable must be routed to the rear of the PC. A connection on the front of the unit would be much more ideal. HP-HIL mostly solves this since many PCs supporting HP-HIL provide the connector on the front of the unit. For units with the HP-HIL connector on the rear of the unit, the problem is greatly lessened since a keyboard is usually the first device connected. Any other devices can then be plugged into the keyboard (which resides at the front of the unit and usually can remain connected to the System).

As previously mentioned, most input devices require their own separate AC power and hence a power cord. The extra cables can subtract greatly from the freedom the user has to move and rearrange devices in the work area. Since HP-HIL devices receive their power from the Host, the AC power cords are eliminated. Also, the extra bulk associated with the power supply is gone so that HP-HIL devices can be smaller, lighter weight, and easier to use and move around.

Types of Interface Structures

The type of interface structure for input devices has many implications in performance and cost. The first consideration is to determine whether a parallel or serial data transfer method is more suitable.

A parallel interface typically has 8-16 data lines and some number of control lines. A simple diagram of a parallel interface is shown in Figure 1-2. The data lines handle the transfer of data from one device to another. The control lines are used for "handshaking", which is the synchronization and control which must occur for an orderly transfer of data. For a data transfer to occur, Device A will signal Device B that it has data ready for transfer. Device B will signal Device A when it is ready to accept data. When this happens, Device A will put the data on the data lines and signal Device B that the data on the data lines is valid. Device B will then acknowledge that the data has been received by use of the appropriate control line.

One advantage of a parallel interface such as this is that data transfer can occur at high speeds and in both directions, i.e., from Device A to

Device B or Device B to Device A. A disadvantage is that the physical connection (the cabling) can be cumbersome since individual wires are required for the data lines plus control lines. For a byte (8 bits) wide data path, a minimum of 12 lines would be needed, 8 lines for data and 4 or more for control.

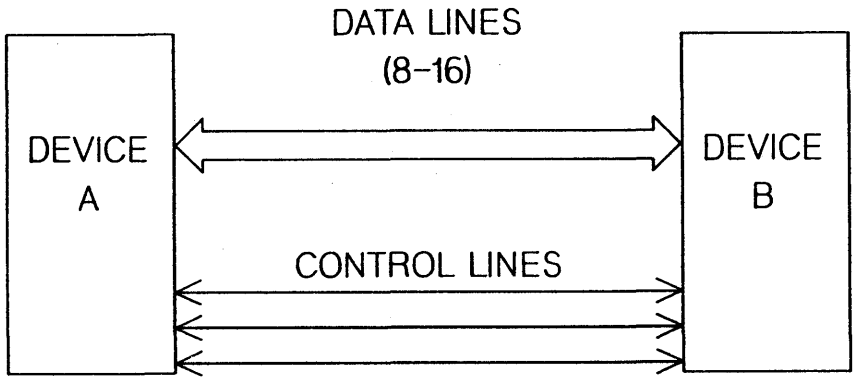


Figure 1-2. A Parallel Interface

A serial interface uses only one or two data lines as shown in Figure 1-3. Data is transferred one bit at a time in packets or frames usually consisting of 8 bits plus control bits. The control bits are added to the beginning and end of the actual data to allow the receiver to synchronize and check for errors. Thus if 8 data bits were to be transmitted serially, a frame of 11 bits might be required. If data transmission is to occur in both directions, usually two data lines are used. Obviously, the one main advantage of serial transmission is that the physical connection is much simpler than a parallel method. Data rates will generally be lower for a serial data transmission scheme.

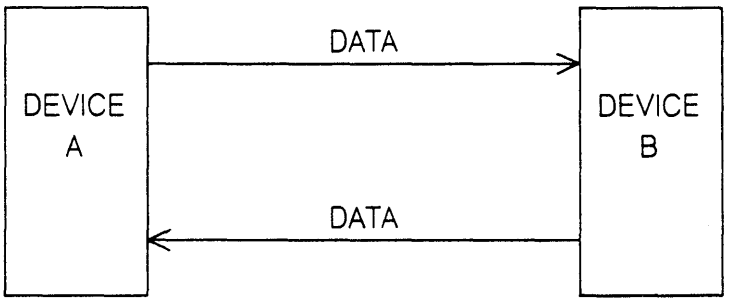


Figure 1-3. A Bi-Directional Serial Interface

The primary objectives of HP-HIL are to make the interface simple, low cost, and flexible enough to support multiple devices. Since human speed input is relatively slow, the interface speed is not a factor. Cabling is to be minimized both to keep the cost low and to keep the size of the cables small. Small cables are desirable as they are easier to handle and generally simplify the device design. Because of these reasons, a serial interface is a clear choice.

There are three configurations or structures which could be used with the serial interface. These are the ring or loop structure, a star or central node structure, and a daisy-chain or link structure.

In the loop structure, information is sent by the Host and passes from device to device, until it returns to the source. For example, consider Figure 1-4. Assume the Host wants to send information to Device B. The information first travels to Device A. Device A then retransmits the data to Device B, the intended receiver. Device B then stores the data as required. The information is again retransmitted to Device C and then back to the Host. At this point, the Host can compare the received data with that which it transmitted to verify that no errors have occurred.

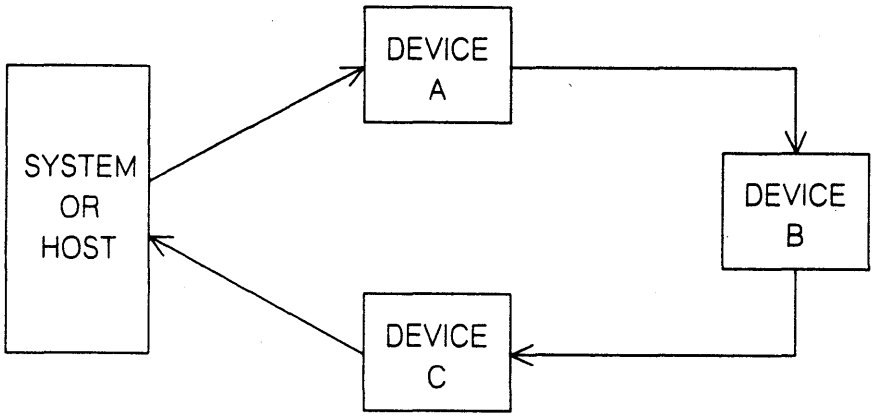


Figure 1-4. A Ring or Loop Structure

The loop configuration has some drawbacks in that transmission time for data to travel around the loop can be limiting. However for human-speed data rates, a loop would be acceptable. Another disadvantage of the loop is the physical connection requiring a second cable to return to the Host. A benefit of the loop configuration is that it can be very low cost, simple, and has some inherent error checking features.

A star or central node configuration consists of the Host in the center with each device as a sattelite as shown in Figure 1-5. In this configuration, communication occurs between the Host and a device one-on-one. This method has advantages of allowing simultaneous data reporting by several devices. However, this occurs at the cost of increased complexity of the Host. Since data rates for input devices will be low, simultaneous data reporting over a serial interface can be easily handled by buffering data or in other ways. Implied in this method of connection is having individual receptacles for the maximum amount of input devices residing on the Host. This is not advantageous from a cabling standpoint.

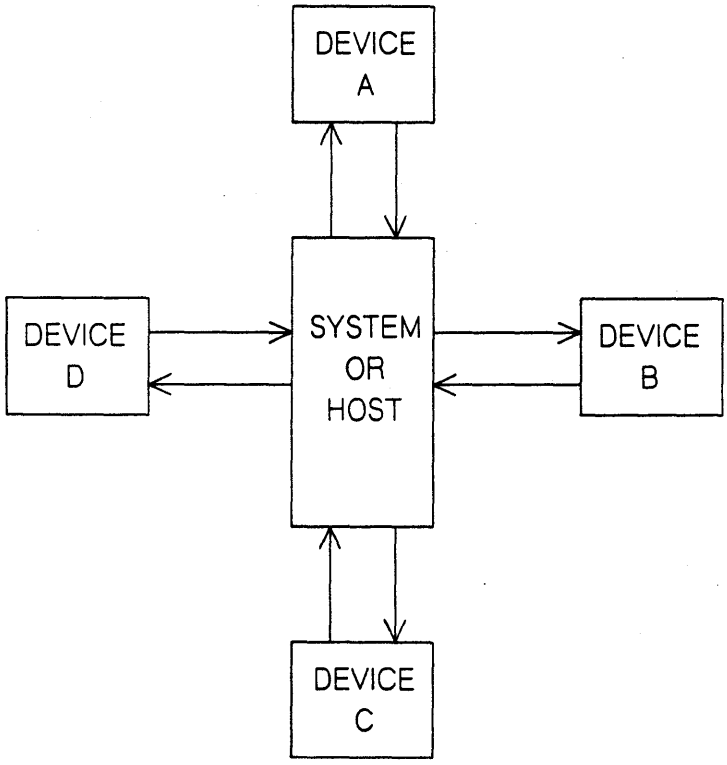


Figure 1-5. A Star or Central Node Structure

A daisy-chain or link configuration maintains a physically serial communication link. Figure 1-6 shows three devices connected by a daisy-chain to a system. Basically, a serial communications link between two devices is repeated as more devices are added. To be truly useful, data has to be able to be sent from the Host to any device and from any device to the Host. A link configuration could actually be implemented logically as a loop, but the cabling and device interconnection would look like a link. Or a combination of the link and loop could be used. Physically, the link is desirable for ease of connection and simplicity of cabling. The loop can be implemented electrically such that each device can switch the data path to actually modify the loop and the number of devices logically connected in the loop.

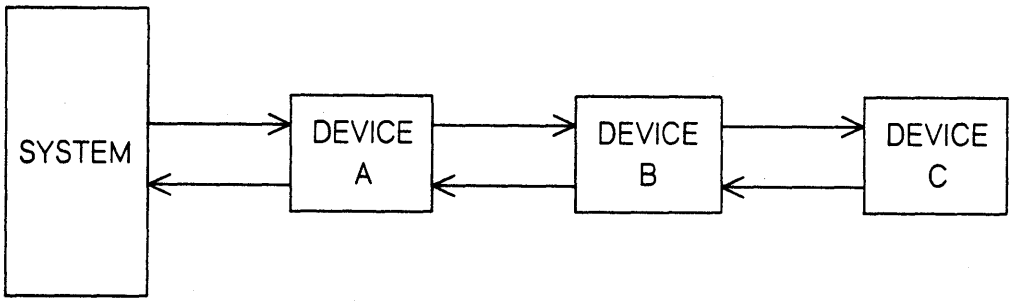


Figure 1-6. A Daisy-Chain or Link Structure

The daisy-chain structure was chosen as the best method for implementing HP-HIL. It provides the desired features and flexibility required for input devices. The implementation of HP-HIL will now be examined.

INTRODUCTION TO HP-HIL ARCHITECTURE

Interface Structure

The HP-HIL interface structure is shown in Figure 1-7. The first device is connected directly to the Host's HP-HIL port. The second device connects to the first device. Each additional device connects to the previous or upstream device. Up to seven devices can be daisy-chained or linked together in this method.

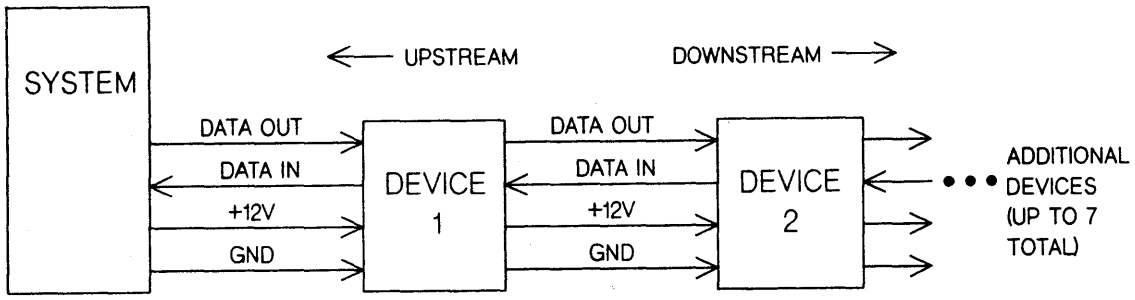


Figure 1-7. The HP-HIL Structure

To allow daisy chaining, each device must have two ports. One port is keyed such that it will only be connected to the Host or upstream device. The second port is keyed differently from the first so that downstream devices only will be connected to this port. The interconnecting cables, separate from the devices, are also keyed to ensure proper interconnection.

Some devices may not have two ports. If a second port is not available for chaining, the device will by definition reside at the end of the Link. It is not recommended for a device to have a single port but in some cases, it may be necessary to minimize the size of the device. An example is the HP Mouse. Obviously, having two receptacles and possibly two cables would make the Mouse much larger and less maneuverable than desired. Thus the Mouse has a permanent cable with a single male Shielded Data Link (SDL) connector on the end. Note that a single ported device is not a requirement for the end of the Link. Any device may be located anywhere in the Link provided that the physical connection is available. Thus a Mouse could be plugged directly into the Host. But since the Mouse has no additional ports, no other devices could be added after the Mouse. However, up to six devices could be placed between the Mouse and the Host.

The physical link for HP-HIL consists of four conductors with a shield. They are +12 volts, Ground (power and signal reference), Data In, and Data Out. The shield is separate from ground in the devices and is for channeling ESD back to the Host for supression. Also, the shield helps minimize Radio Frequency Interference (RFI).

HP Standard ICs

As previously mentioned, HP-HIL hardware is constructed around two IC's developed by Hewlett-Packard. The first IC, referred to as the Master Link Controller (MLC), provides the hardware interface between the System microcontroller and the devices connected to the HP-HIL. The MLC accepts commands from the System processor and transmits messages through HP-HIL with the proper format. The MLC can also collect data entered by the user from the input devices, and relay it to the Host. An eight bit parallel, bi-directional data bus is used to transfer data to and from the Host's processor. The MLC also contains a 16 frame FIFO which reduces the number of interruptions to the Host processor. Automatic polling (data collection from the devices) is also possible by the MLC which requires processor intervention only when data is received. The Host processor can also be reset by the MLC through the HP-HIL devices. The MLC also handles error checking, and has an internal loopback mode for local testing.

The second IC is the Slave Link Controller (SLC). The SLC is basically an intelligent UART which provides the communication interface between HP-HIL (the MLC or other SLCs) and the device microprocessor. The SLC receives commands and data for the device microprocessor, transmits data, retransmits commands, and detects communication errors. The SLC provides self-test capabilities and clock generation for the device processor. Communication with the device processor is serial and is commonly used with the National COPs family, although other processors can be used. Link protocol is handled by the device processor as well as data collection and scanning of the actual input device.

Power Supply from System

An integral part of HP-HIL is the ability to supply power to the input devices from the Host. 12 volts DC is supplied separately onto the Link from the Host's

power supply for use by input devices on the Link, as shown in Figure 1-8. Each device locally regulates the +12 volts to +5 volts.

Note that the shield shown in Figure 1-8 is separate from the power supply ground. The shield is only connected to ground at the System, but is separate from ground in the input devices and their cabling.

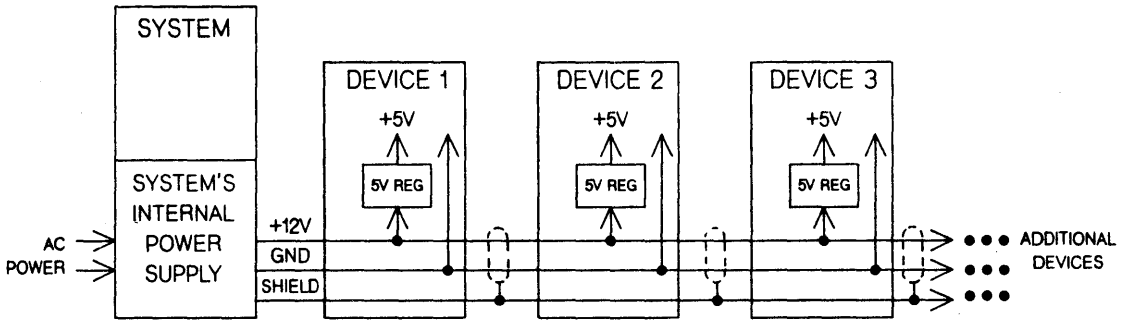


Figure 1-8. Power Supply Distribution and Regulation

Data and Data Paths

Data moves around the Link in packets called "frames". A frame consists of 15 bits including start, stop, command, parity, address, and data bits.

Frames always originate from the Host (except for a hard reset command originating from a device or if a framing or parity error is detected by a device) and are always returned to the Host. If data is sent back to the Host in response to a command, then the command trails the data. This insures that the Host can determine when all data has been received. When a frame is transmitted by the Host, the frame travels around the Link until the command's address matches a device address. The device then processes the command, transmits data if required, and then retransmits the command. The command originally transmitted by the Host traverses the entire Link and is received by the Host for verification.

Consider a system with 2 devices attached as shown in Figure 1-9. When the System (Host) transmits a frame, it is sent out the SO (Serial Data Out) line of the MLC. The frame then is received by the first device on the SI (Serial Data In) line of its SLC. The device checks for an address match. If no match is found, the frame is retransmitted from its SO line. If the address matches Device 1, then Device 1 processes the command. After the command is processed, the command is retransmitted from its SO line. Device 2 then receives the frame on its SI line and checks for and address match and processes the command if the address matches. The command at this point is then retransmitted on its RO (Return Data Out) line rather than on its SO line. This is because Device 2 is the last device on the Link. The last device is set to return data on RO rather than SO during a configuration process which occurs upon Link startup. During the return path the frame is received on the RI (Return Data In) line of Device 1. Device 1 passes the frame directly (buffered only) out of RO and finally back to the Host. The System receives the frame on its SI (Serial Data In) line to complete the process.

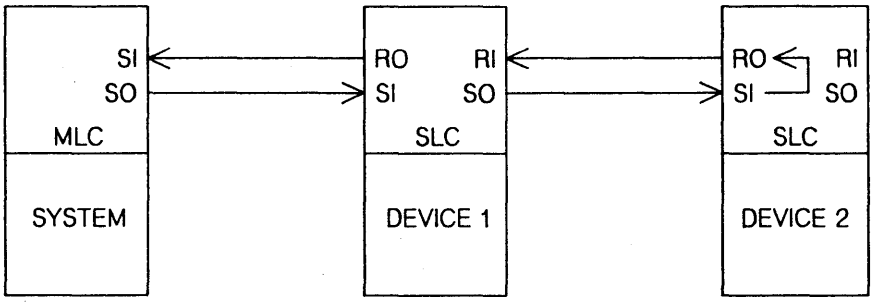


Figure 1-9. Data Path for a Two Device System

The configuration process which occurs at System startup or application startup prepares the Link for communication with the Host. Upon power up, all devices are in the same condition, with a device match address of 0, Power-Up Mode set, and the SLC in Loop-Back Mode as shown in Figure 1-10. The goal of configuration is to assign a unique address to each device on the Link and configure the SLCs' to provide a continuous closed data path to all devices.

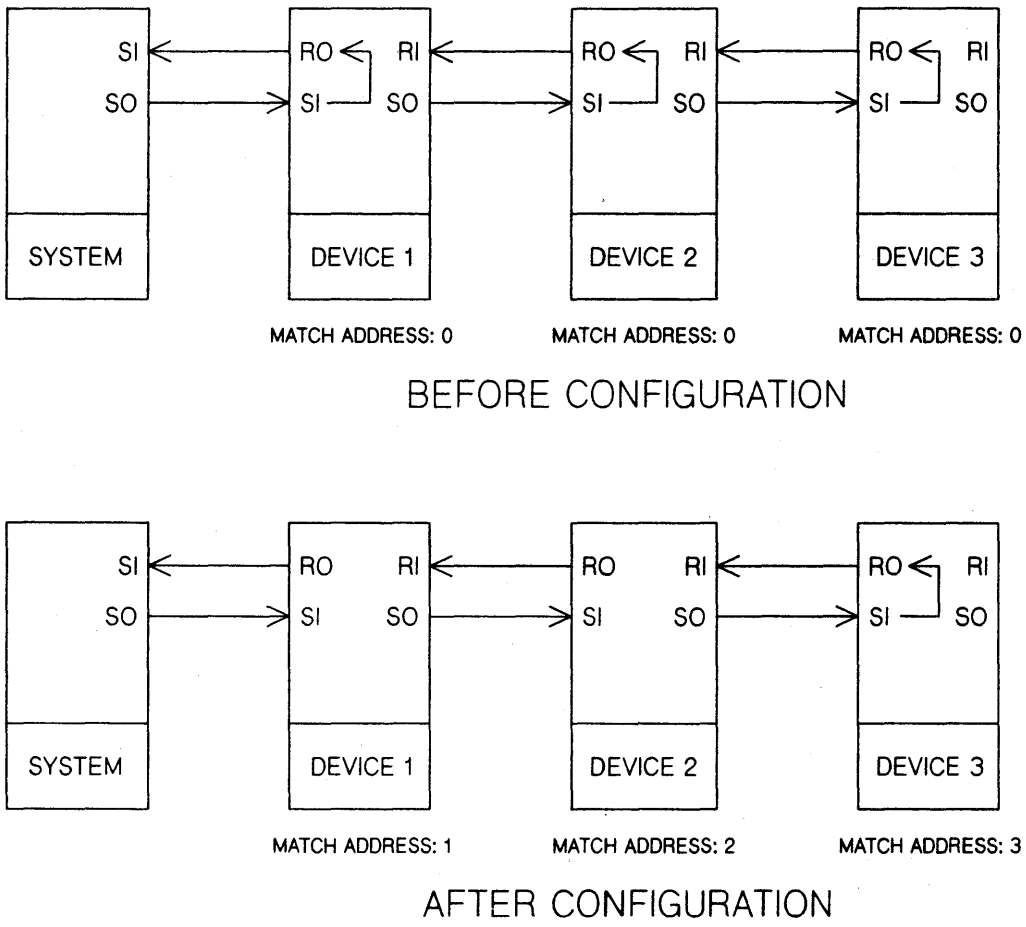


Figure 1-10. Example of Link Configuration

A MORE DETAILED LOOK AT HP-HIL

System Block Diagram

The terminal, workstation, or personal computer (referred to as the System or Host) contains the MLC, address decoding, protection circuitry, the System microprocessor, and the System power supply as shown in Figure 1-11.

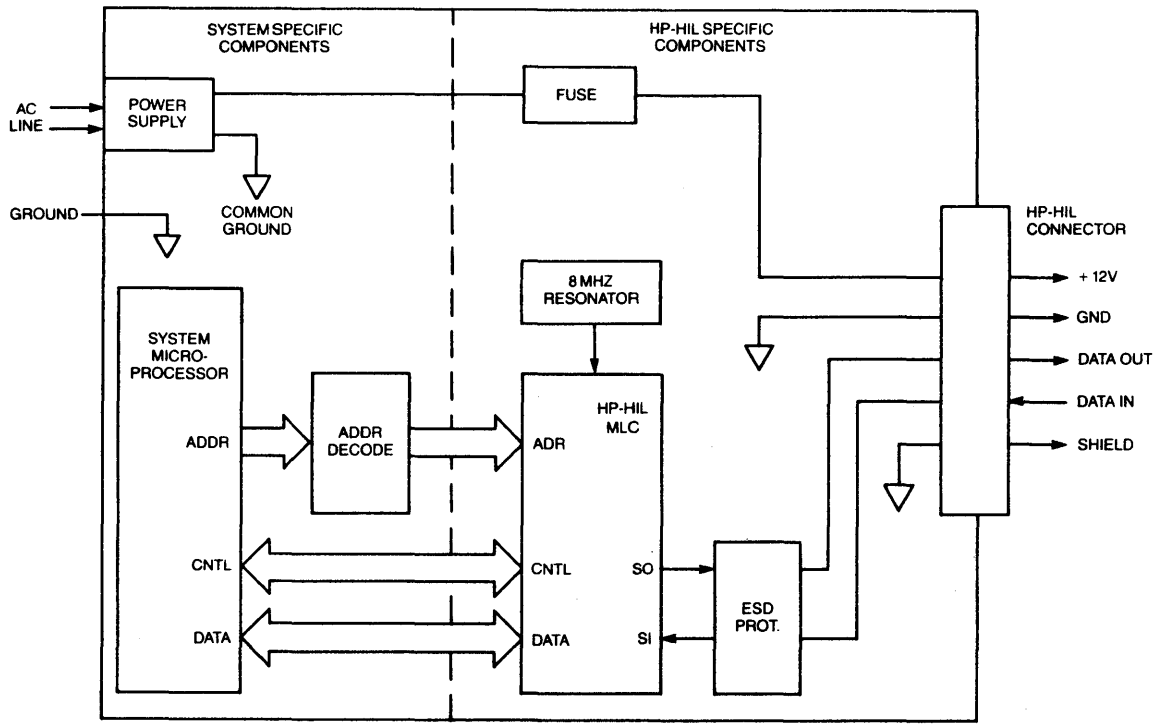


Figure 1-11. System Block Diagram

The Power Supply provides +12 Volts DC, for use by the HP-HIL devices. The maximum amount of current available for the devices may vary among Systems, depending on the devices supported and the unique requirements and capabilities of the System itself. HP-HIL devices typically require 100 mA on +12V, so the average System should provide 750 mA as a minimum. Increasing use of low-power technologies will lower this requirement in the future.

Shown in the power supply line is a fuse. A fuse or other power limiting means may be required for some regulatory agencies. The fuse limits the energy available outside of the System in case of any fault conditions. Consult Sections 2 and 3 for guidelines on hardware design.

The System microprocessor provides support for the HP-HIL protocol, and is responsible for configuring the Link, processing input device data, error recovery, and generally initiating commands onto the Link. The processor supplies address, control, and data signals to which the MLC is connected.

The MLC serves to interface the System microprocessor to HP-HIL, functioning as the Link controller. The MLC accepts commands from the System processor, transmitting and receiving messages with the HP-HIL frame format. It can be used to manually poll attached devices for data, or can be placed into

Auto-Poll mode, where given the appropriate clock (typically 60 Hz) on the AP pin the MLC will automatically poll the Link, interrupting the microprocessor only when one or more devices report data.

There are two data lines originating from the MLC. These are the SO (Serial Data Out) and SI (Serial Data In) lines. Before going to the external HP-HIL connector, a simple transient protection circuit is used to clamp any ESD between ground and +5 volts. This circuit employs 4 diodes and 2 resistors and is used on all HP-HIL data lines at the System and also for all input devices using the SLC. The shield connection is made through the shell on the SDL connector. The shield is separate from power supply ground in the actual cable and input devices but is usually connected to power supply ground at the System.

The MLC can interface directly to the System processor's bus. Generally, address lines will need to be decoded to place the MLC in the desired portion of the processor's memory map. The control lines (read, write, interrupt) and the data bus tie directly to the MLC. The MLC can generate its own clock with an external resonator or it can use the System processor clock. The clock frequency is 8.0 MHz.

Device Block Diagram

HP-HIL Devices contain many of the same functional blocks as the System, however the device organization is slightly different. The devices typically contain a SLC IC, device microprocessor, a voltage regulator, and any device-specific components. A block diagram of an HP-HIL device is shown in Figure 1-12.

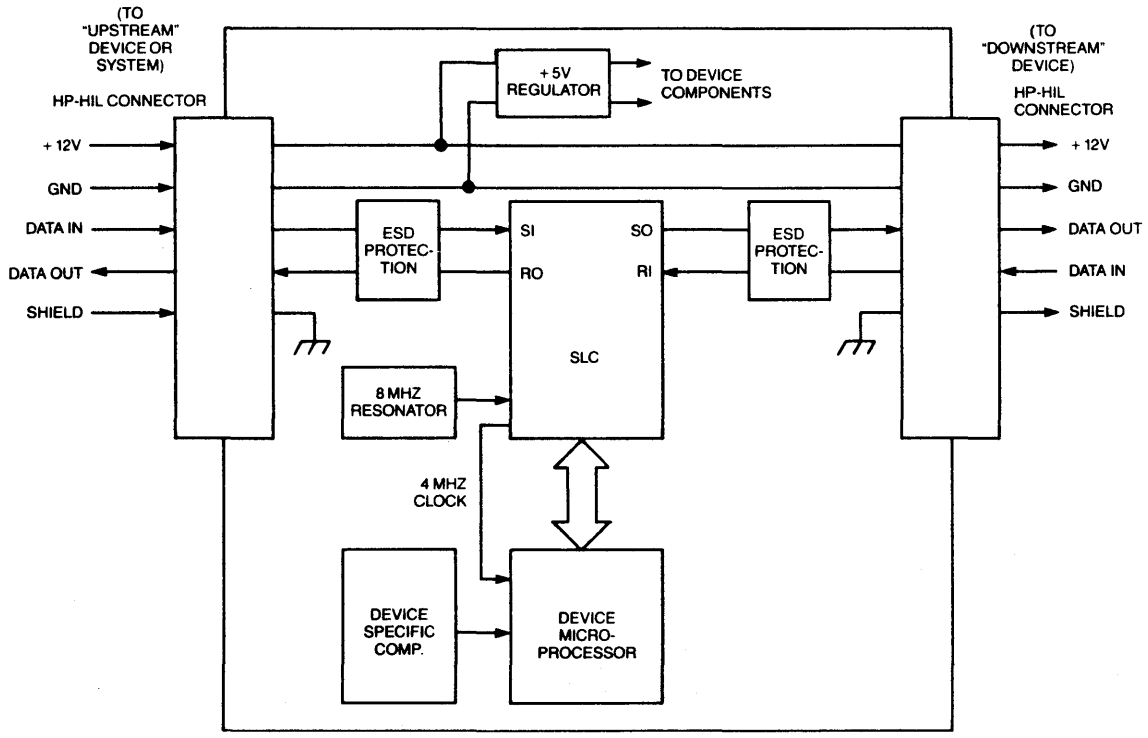


Figure 1-12. Device Block Diagram

The SLC serves as the communications Link between the device microprocessor and the System, transmitting and receiving data via HP-HIL, interrupting the device processor only when a frame with the correct match address or improper format is received. The SLC also provides the hardware reset functionality for the device, lowering the NMI (Non-Maskable Interrupt) line both at power up and in response to the Device Hard Reset command. Also contained in the SLC is a clock generation circuit which requires an external ceramic resonator. This circuit generates an 8 MHz clock which the SLC divides to 4 MHz and supplies this to the local processor. Internally, the SLC further divides the clock to 1 MHz for its own use.

The device microprocessor maintains the HP-HIL interface through the SLC and performs tasks required for device data collection. Performance requirements for the processor vary with the complexity of the data collection task and any optional HP-HIL features supported by the device, and thus a wide variety of microprocessors or microcontrollers are likely to be used. Existing devices make extensive use of the National Semiconductor COPS family of microcontrollers due to their inherent low cost and the ease with which they are interfaced to the SLC IC.

Device specific components are those components which capture input data to be sent back to the System. For example, a keyboard could require multiplexers, gates, and a keyswitch array. For a mouse, a mechanism to detect movement would be needed. In most cases, the device processor actually has a dual role of collecting data and managing the HP-HIL interface.

In a device, the +12 volts passes through the device and supplies the local regulator. The local regulator supplies the required +5 volts for the SLC, device processor, and any other circuitry needing +5 volts.

It is recommended that future devices limit current consumption to under 100 mA to provide for maximum configuration flexibility and System portability. Although a few existing devices may consume up to 150 mA or more, this level of power consumption can impose premature limitations on the number of devices which may be attached to a system and the cable length between system and devices.

Abnormally high input voltage requirements may also limit Link configuration flexibility. Most commercially available regulators typically require an input voltage of +7.3V to regulate to +5V. The specified minimum input voltage for HP-HIL devices is +7.3V.

Referring to Figure 1-12 again, note the data paths inherent in the device. Data enters the SI input of the device from the "Upstream" or System side. If a "Downstream" device has been configured onto the Link, the SLC will pass commands out the SO line to the next device, eventually receiving it again through the RI line. The command is then buffered only and is sent out the RO line to the upstream device or the System. In this case, the SLC is in "Pass-Thru" Mode. If a downstream device was not configured onto the Link, the data entering SI would then be sent out the RO line after any processing. This illustrates how data is routed when the SLC is in "Loop-Back" Mode.

Signal Description

Following are descriptions of the signals used in HP-HIL:

+12V Positive 12 Volts DC, measured with respect to GND at the System. Supplied by the System for use by all HP-HIL devices. Individual devices locally regulate this line down to +5 volts. Note that the voltage level at individual devices will be less due to losses in the cable.

GND Ground. Power supply and signal reference.

SHIELD This is the cable shield used for RFI reduction and it provides an ESD discharge path back to the System.

SI (System) - Serial Data In. This is an HP-HIL input signal found on the MLC, driven by the RO line on the first device.

SI (HP-HIL Devices) - Serial Data In. This is an HP-HIL input signal on the SLC, driven by the SO line on the upstream device or the System.

SO Serial Data Out. This is an HP-HIL output signal found on both the MLC and SLC ICs. This line drives SI on the next (or downstream) device (if present).

RI Return Data In. This is an HP-HIL input signal found on the MLC IC. This line is driven by RO on the previous (downstream) device (if present). It is internally pulled up to logic "1".

RO Return Data Out. This is an HP-HIL output signal on the SLC, and drives RI on the previous (upstream) device, or SI on the System.

Note that the idle state of the HP-HIL signals is a logic "1".

Frame Structure

Information travels through the Link in a fixed format called a "frame", which consists of 15 bits of information including start, stop, command, parity, address, and data bits as shown Figure 1-13. These frames are transmitted around the Link at the rate of 10 microseconds per bit, or 150 mircoseconds per frame. The idle state of the Link is a logic "1", with the first bit in a frame (the start bit) at logic "0" and the last bit (the stop bit) at logic "1". A minimum of 4 microsconds of idle time is required between frames, allowing frames to be transmitted at a maximum rate of 1 per 154 microseconds. The parity bit is computed so that the total number of logic "1" bits in the 15-bit frame (including start, stop, command, parity, address, and data bits) is odd.

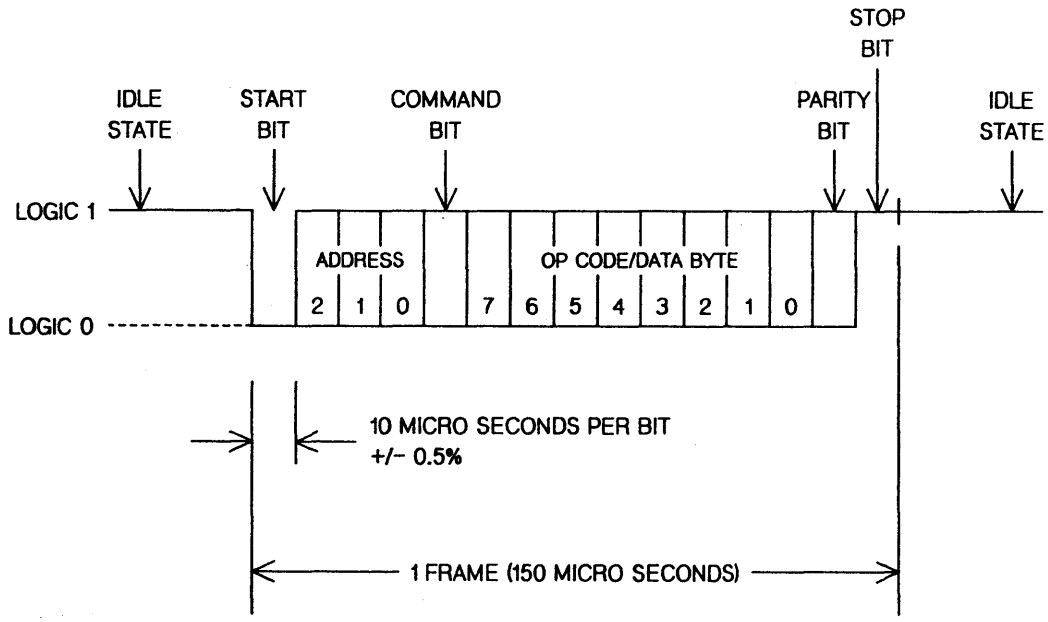


Figure 1-13. HP-HIL Frame Structure

HP-HIL can achieve data transfer rates as high as 6500 bytes/second (although typical data rates are much lower.) The HP-HIL Protocol supports automatic configuration, identification, and polling of up to seven devices, as well as sophisticated error recovery, device and System reset functionality, primitive output, and many more specific commands which provide for a simple yet universal approach to input device integration.

Note that frames are generally referred to by a three digit hexadecimal number, with the most significant bit being the command bit, followed by A2 - A0, followed by D7 - D0. Thus a command with address 0 (universal), opcode 34h would be referred to as 834h, while a data frame with address 5 and data byte of DFh would be 5DFh. This is consistent with the format of the frames when read from the SLC and MLC. Note that the command bit is placed to the right of the address bits when transmitted. However, the command bit is placed at the left of the address in the MLC and SLC registers.

HP-HIL Protocol

Number of Devices

As previously mentioned, the frames used to carry information around the Link have an address field of 3 bits. This allows for a maximum of 8 addresses. Address 0 is assigned as a universal address which is used when a command is to be sent to every device on the Link. The balance of addresses, 1 through 7, are assigned to individual devices during the configuration process.

Devices are assigned unique addresses so that each device on the Link can be distinguished from one another. The type of device (i.e, mouse, keyboard) is not enough for identification since more than one of the same type of device (i.e., two identical keyboards) are permitted on the Link at the same time. The device address limits the number of devices on the Link to a maximum of 7.

Basic Functions

HP-HIL has a command set through which all necessary functions to set-up and maintain the Link are performed. Basic operation of the Link can be broken down into five categories. These are configuration, error recovery, data extraction, identification, and special functions. All of the HP-HIL commands fall into one of these categories and are explained further in Section 4. A brief explanation of the purpose of the five functional areas will be given here.

The first and most fundamental category is configuration. Configuration is the process by which the Link is setup so it can provide the Host with data in an orderly manner. Configuration typically occurs when the Host is first powered up and any time where error recovery calls for a reconfiguration of the Link. The goal of the configuration process is to assign a unique address to each device on the Link, and to set the device modes such that data will be looped back by the last device on the Link. In the process, each device may be requested to identify itself and report parameters necessary for scaling the device data to the Host and utilizing any advanced features of the device.

The second category is error recovery. Errors may occur under various conditions on HP-HIL, and the correct System response to these errors varies as well. HP-HIL provides for several levels of error recovery so that if an error occurs, the error recovery process will preserve the maximum amount of data and minimize the time and amount of interaction with the Link. Errors are corrected from the System, but detected by both devices and the System.

Data extraction is the third category. Data extraction covers the means by which the Host gathers information from the input devices connected to the Link. Character data, position data, and a limited amount of status information can be communicated back to the System using the data extraction commands. When used with information obtained by the identification commands, most types of input device data can be completely processed.

The fourth category is Identification. Identification commands are used to determine the type of the attached devices, as well as some general characteristics of these devices required to understand the data they report. Device types could be keyboards, relative positioning devices, or other devices similarly classified. Characteristics of devices are typically resolutions (counts per cm), maximum counts, directional information, and information on how the device reports data. Specifics are covered in detail in Section 4.

The fifth and last category of HP-HIL capabilities is defined as special functions. Special functions include those commands which are designed to take advantage of more advanced features of some devices. These features are related to register manipulation, keyswitch auto-repeat, output, System reset, and are not part of the basic HP-HIL functionality. Although these capabilities are not commonly used, they do provide for devices with enhanced features.

INTERFACE SPECIFICATIONS

SECTION 2

SYSTEM SPECIFICATIONS

Voltage

Measuring at the System's HP-HIL connector with respect to ground, the System's output voltage should be 12 volts DC +/- 5%.

Current

Available current provided for HP-HIL devices should be 750 mA, minimum. If less than 750 mA is available, restrictions must be made on the number and/or the type of devices to be used.

Signals

Signal compatibility on HP-HIL data lines (SO, SI, RO, RI) is maintained through use of the HP Standard IC for system applications, the MLC.

Shielding and Grounding

An integral part of the HP-HIL design is the use of shielding for protection against ESD and RFI. Shielding is provided through the shell of the HP-HIL connector on the System. See Section 3 for implementation details.

Mechanical

The System provides HP-HIL through a single, HP-HIL recepatacle. This recepatacle is of the "E" keying designation.

NOTE: Consultation with a product regulatory specialist is critical to ensure that the product complies with applicable regulations.

Safety

The Host shall provide isolated power supply circuits and appropriate current limiting of the power supply lines feeding the HP-HIL circuits to meet safety requirements. See Section 3 for recommended design methods.

EMI

The host product shall be tested with the various HP-HIL accessories which are to be supported on the System in accordance with the various national and

international radio frequency emission control requirements. In some cases, licences and/or compliance declarations may be required.

DEVICE SPECIFICATIONS

Voltage

Although the output voltage from the System onto the Link is 12 volts DC, there are finite voltage drops due to the cables and connectors. This means that each successive device while moving further down the Link away from the System, will have a lower DC input voltage, with the last device on the Link having the lowest input voltage. To insure that Link integrity is maintained, devices should operate correctly and reliably with a minimum input voltage of 7.3 volts DC. Devices should also operate at the maximum of 12.6 volts DC and all values between the minimum and maximum values.

Current

Input devices should be limited to a maximum input current of 100 mA per device, over the entire range of input voltages. Devices requiring greater than 100 mA will cause excessive voltage drops on the Link which may prohibit connecting the maximum (seven) devices on the Link.

Signals

Compatibility of the HP-HIL signals shall be maintained by use of the HP standard IC for use in devices, the SLC.

Shielding

Input devices shall keep the cable shield separate from the signal reference line. The signal reference line is used as power supply and signal common. The cable shield is used for RFI shielding and a drain path for ESD. Input devices must be fully protected from ESD applied externally on the device.

Mechanical

HP-HIL devices shall provide connection paths to both the upstream device (or System) and the downstream device. Connection to the upstream device is provided through a female SDL connector of the "A" keying polarity. Connection to the downstream device is provided through a female SDL connector of the "E" keying polarity.

For some devices, providing the two SDL connectors will be unacceptable because of the devices size and/or characteristics. In this case, a permanently attached cable with a "E" keyed male SDL connector on the end can be used. An example of a device which two SDL connectors is inappropriate is a mouse. However, this method of cabling is not recommended. If a device does not allow for additional devices to be connected to it, then the device can only be placed at the end of the Link as a "last device". Obviously, only a single "last device" can be used at a time on the Link.

NOTE: Consultation with a product regulatory specialist is critical to ensure that the product complies with applicable regulations.

Safety

Plastic enclosure materials, printed circuit boards, and wiring should have an appropriate flame rating as specified by those test houses/agencies for which approval is required.

The device or accessory should also be marked to include the supply voltage (+12 volts DC) and the current consumption. Markings on the device are needed to satisfy certain test house requirements, and allow the user to determine if the combination of HP-HIL devices to be connected to the Host exceed the Host's current supplying capabilities for HP-HIL. The current consumption specified should be a value which is the maximum current required by the device. Actual current consumption by the device cannot exceed by more than 10% the rating on the product. It is usually best to base the specified value on measurements of the device's current consumption. Calculated values of current consumption tend to greatly exceed measured values and are not an accurate representation of the device's requirements.

EMI

The device or accessory product will require testing in a typical systems environment, including connection to other HP-HIL devices. Given the devices are user purchased and connected, the devices themselves should meet the various EMI levels for FCC, VDE, and CISPR 22 requirements.

CABLE AND CONNECTOR SPECIFICATIONS

Interconnection Method

HP-HIL devices are interconnected to each other and the Host by shielded, 4 conductor cables with connectors on each end. For maximum flexibility, devices contain two receptacles, and are connected to one another with separate cables. This allows different lengths and styles of cables to be used for device connection. Furthermore, since cables are not captive to a device, transportation and storage are simplified.

Interconnection between devices and the Host is accomplished with SDL (Shielded Data Link) connectors and receptacles. The receptacles, used in devices and the System, provide contacts for four conductors and a 360 degree shield. Interconnection cables have SDL plugs on each end, while devices and the System contain the SDL receptacles.

Typically, devices have two receptacles; one for connection to the System or previous device, and another to which the next device may be connected. To prevent improper device connection, two different keying styles are used. These are referred to as "A" keying and "E" keying configurations, and graphically referred to with one dot and two dots, repectively. Figure 2-1 shows how a typical system and devices are interconnected with the SDL connectors and cables. Figure 2-2 shows the signal connections in the HP-HIL system. The two receptacles should be located on the rear of the device such that the receptacle with "A" keying is on the right of the other, when viewing the device form the rear. This is shown in Figure 2-1.

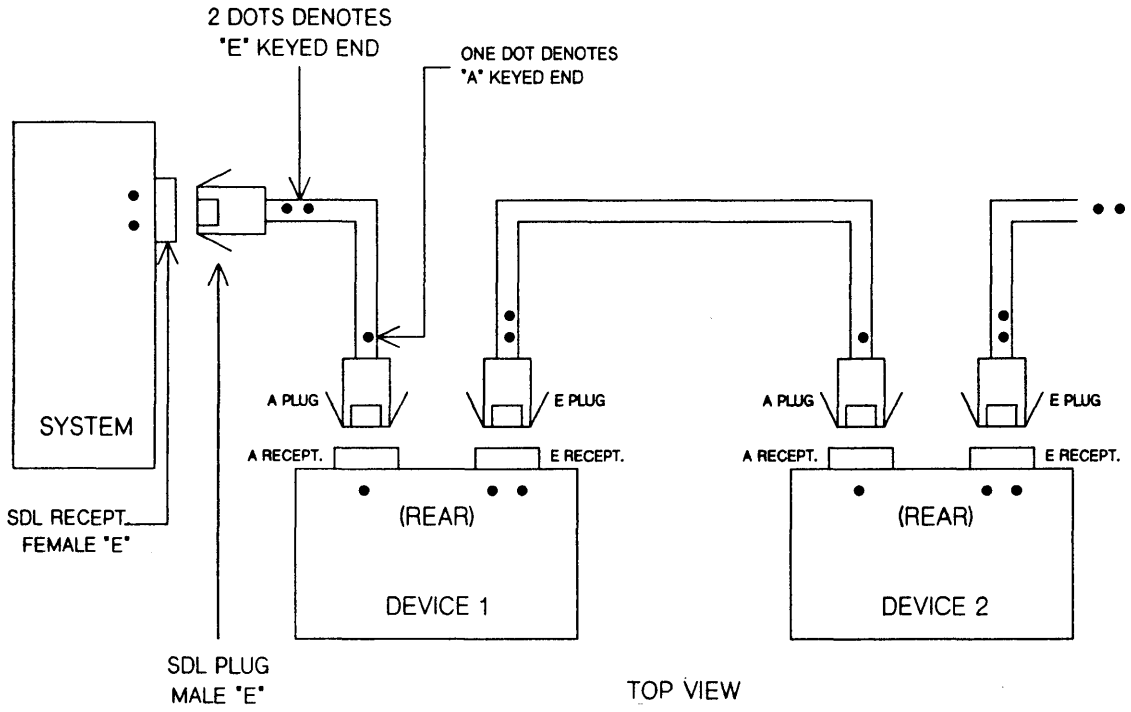


Figure 2-1. Typical System Interconnection Using SDL Connectors

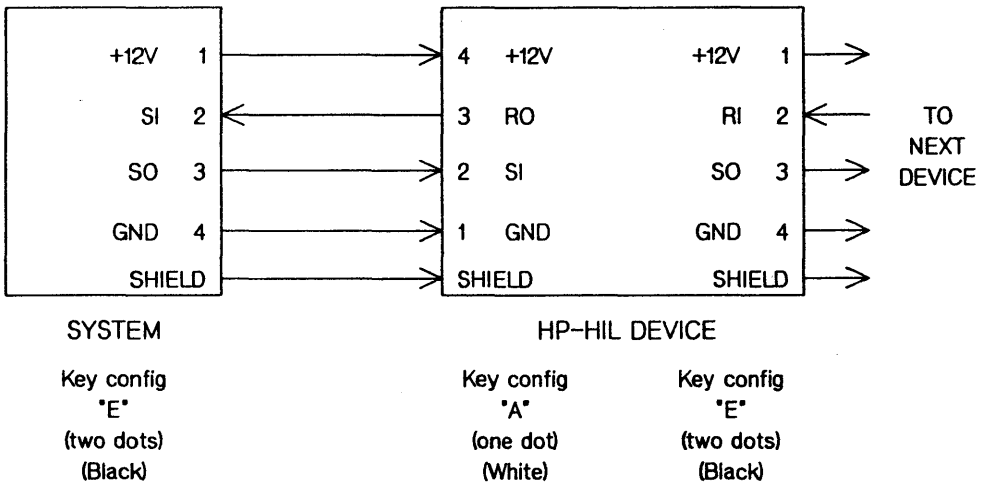


Figure 2-2. Signal Connections Through SDL Connectors

SDL Receptacles

As previously mentioned, two types of SDL receptacles are used in the HP-HIL system: "A" and "E" keying configurations. Keying is accomplished in the SDL connectors by two ridges which protrude from the inside ceiling of the receptacles. For a SDL plug to be inserted into the receptacle, the plug must have groves which match the location of the ridges in the receptacle. Thus, different keying configurations are achieved by relocating the ridges.

To identify the keying of a receptacle, two methods are used. First, the receptacles usually will have an "A" or "E" visible on the outside back or on the inside back (difficult to see when present). Second, the "A" keyed receptacles are now molded in white plastic, while the "E" keyed receptacles are black. Figure 2-3 shows the pinouts of the SDL receptacle.

The SDL connectors are not the standard SDL connector available from AMP, Inc. The HP version has stronger keying ridges and is color coded (black, white). It is recommended to use the HP type SDL connectors.

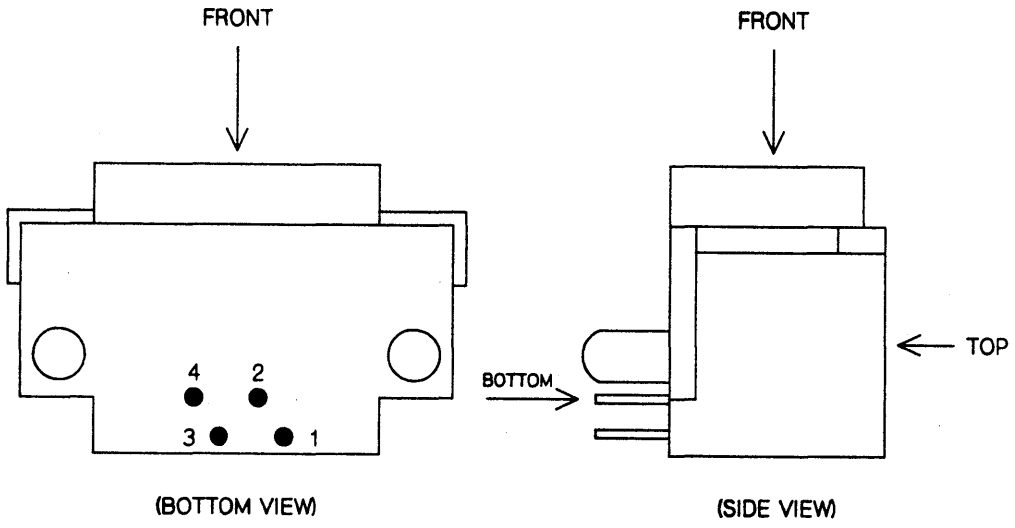


Figure 2-3. SDL Female Connector Pinouts

The HP part numbers for the SDL receptacles are as follows:

"A" Keying, White, Female SDL. . . . . AMP P/N 1-520792-1

"E" Keying, Black, Female SDL. . . . . AMP P/N 5-520791-1

Interconnection Cables

There are currently three different styles of cables used to connect devices to one another and the System. These are described here:

Coiled cable, extended length approximately 1.5 m.
Color: Dove Gray enclosure, HP P/N 46020-60001

Flat cable, length 2.4 m.
Color: Dove Gray enclosure, HP P/N 46080-61601

Flat cable, length 0.5 m.
Color: Dove Gray enclosure, HP P/N 46083-61601

The pinouts and connections of HP-HIL cables are shown in Figure 2-4. As with the receptacles, the plugs are molded in colors to denote keying. Clear plugs are "A" keyed, and correspond to white receptacles. Smoke colored plugs are "E" keyed and correspond to black receptacles.

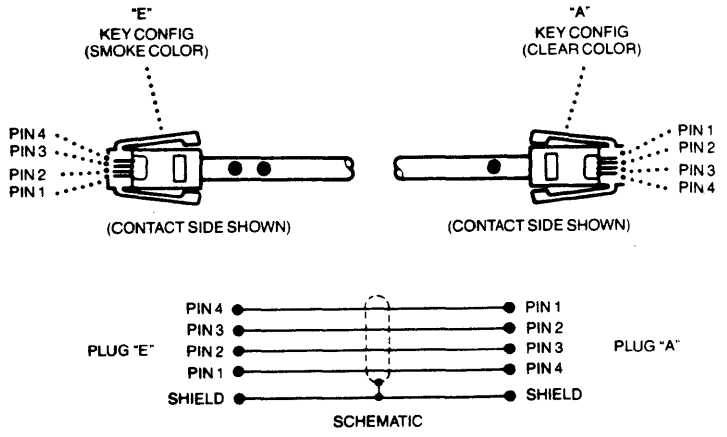


Figure 2-4. HP-HIL Cable Pinouts

Cable Specifications

RESISTANCE

The maximum cable resistance shall be 0.8 ohms per line, contact to contact. (This is measured with plugs attached to each end of the cable.) Shield resistance shall be less than 0.4 ohms per line, measured from plug shell to plug shell. Insulation resistance shall be 100 megohms, minimum.

CAPACITANCE

Capacitance between any signal line and all other parts of the cable shall be 600 pF, maximum. (Measured with other conductors and shield shorted together.)

DIELECTRIC

Dielectric withstand voltage shall be 1500 VRMS, minimum.

Additional Cable Considerations

Since the cabling used to connect most HP-HIL devices may be specified at the System level to suit specific System requirements, the following is a discussion of the electrical parameters which should be considered when determining the suitability of a particular cable assembly.

CABLE RESISTANCE

Cable resistance is a factor which must be taken into account on the +12V and GND conductors if other than recommended cables are to be used. A generalized model of an HP-HIL implementation is shown below in Figure 2-5.

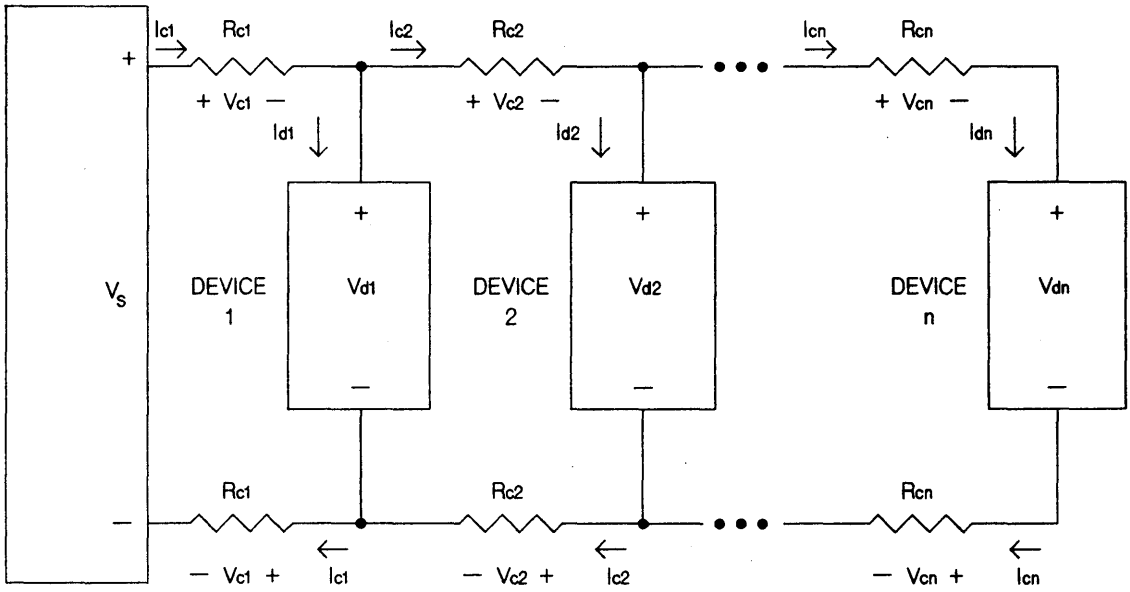


Figure 2-5. Device Interconnection Resistance Model

NAME	DESCRIPTION
Vs	+12 Volts DC as provided by the System (+/- 5%)
Ic1	Total current through cable connecting Device 1 to the System.
Rc1	Total resistance of one conductor of the cable connecting Device 1 to the System.
Vc1	Total voltage drop through each conductor of the cable connecting Device 1 to the System (power supply lines only), computed as Ic1 * Rc1.
Id1	Maximum current required by Device 1 for operation.
Vd1	Input voltage to Device 1, which must exceed the specified minimum for the device to ensure correct operation.
Ic2	Total current through cable connecting Device 2 to Device 1, which may be computed as Ic1 - Id1.
Rc2	Total resistance of one conductor of the cable connecting Device 2 to Device 1.
Vc2	Total voltage drop through each conductor of the cable connecting Device 2 to Device 1, computed as Ic1 * Rc1.
Id2	Maximum current required by Device 2 for operation.
Vd2	Input voltage to Device 2, which must exceed the specified minimum for the device to ensure correct operation.
Icn	Total current through the cable connecting Device N to Device (N-1), which may be computed as Ic(n-1) - Id(n-1).
Rcn	Total resistance of one conductor of the cable connecting Device N to Device (N-1).
Vcn	Total voltage drop through each conductor of the cable connecting Device N to Device (N-1), computed as Icn * Rcn.
Idn	Maximum current required by Device N for operation.
Vdn	Input voltage to Device N, which must exceed the specified minimum for the device to ensure correct operation.

In general, for all configurations of N devices supported by the System, cable resistance must be such that the input voltage to Device N (Vdn) is sufficiently high to guarantee correct operation of the device. In addition, the voltage drop in the reference conductor (GND) must be sufficiently low to guarantee correct logic levels between devices. Consider the following model in Figure 2-6.

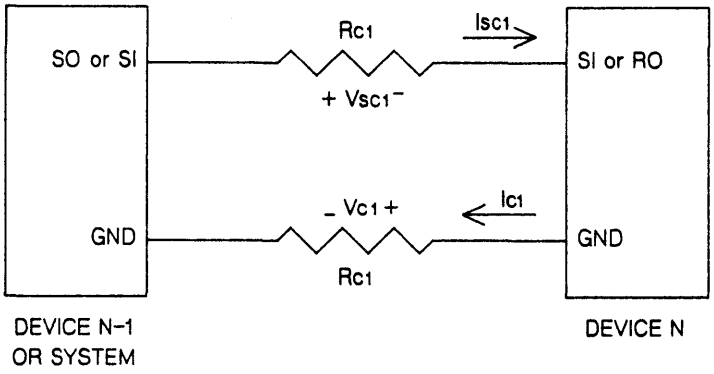


Figure 2-6. Signal & Ground Resistance Model

NAME	DESCRIPTION
Isc1	Total current through an HP-HIL signal line between Device 1 and the System.
Vsc1	Total voltage drop through an HP-HIL signal line conductor of the cable connecting Device 1 to the System, computed as Isc1 * Rc1.

Assuming Isc1 to be negligibly small with respect to Ic1, and therefore Vsc1 to be effectively 0 volts, the cable resistance (Rc) must be sufficiently low to guarantee correct logic 1 and 0 levels between a device and the previous device or the System when considering Ic to be the maximum value for a fully configured Link. Refer to the SLC and MLC Data Sheets in the appendix for the HP-HIL signal specifications.

CABLE CAPACITANCE

In addition to considerations of cable resistance are those of cable capacitance, defined as the total capacitance of the HP-HIL signal conductors to all other conductors. Cable size and length may also be limited by the maximum capacitive drive capability of the SLC and MLC IC's. Calculations are based on the following model:

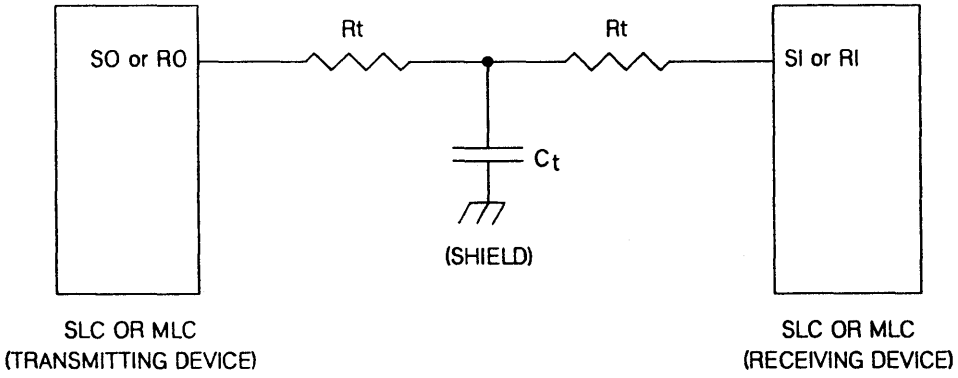


Figure 2-7. Cable Resistance and Capacitance Model

NAME	DESCRIPTION
Rt	Total resistance in the HP-HIL signal line external to the SLC or MLC IC, including 1/2 the cable conductor resistance and any transient protection circuitry.
Ct	Total capacitance of the HP-HIL signal line conductor to all other conductors.

For specifications concerning the maximum capacitive drive capability of the SLC and MLC IC's, refer to the respective data sheets in the appendices.

HP-HIL HARDWARE

SECTION 3

HARDWARE OVERVIEW

To maintain flexibility and consistency of HP-HIL, some guidelines should be followed when designing either systems or devices which support HP-HIL. For your reference, here are some guidelines we have followed in developing HP-HIL devices. You should be knowledgeable in the areas of RFI, EMI, and product safety regulations. Also, you should be knowledgeable about appropriate grounding, shielding, and electrostatic discharge techniques.

SYSTEM HARDWARE

Connectors

For ease of use, the SDL receptacle should be placed at the front of the unit or on a side (but placed near the front). Since it is anticipated that some users will frequently change input devices (or move them from system to system), it is most desirable to be sure the HP-HIL port can be easily accessed. This also means that the System should not have to be turned around to reach the receptacle. Once the cable is plugged in, it should not exit the unit such that it creates an obstacle for other devices, e.g., the keyboard. There should be adequate room so that the user can get his/her hand and fingers on the SDL plug to remove it from the receptacle. Recessing the receptacle should be minimized for best accessibility.

Because there are two different keying configurations used with HP-HIL, the receptacle should be clearly marked. There are two schemes used to show the correct polarity. First, an icon of the cable plug clearly showing the two dots (for the System end of the cable) may be located adjacent to the HP-HIL port. A second method would be to show the two dots only. The icon method is preferred. A phrase labeling the port and indicating to use the end of the cable with two dots is acceptable as dictated by the product's industrial design. Note that labeling the connectors with an "A" or "E" is not acceptable. Figure 3-1 shows two ways of indicating receptacle polarity.

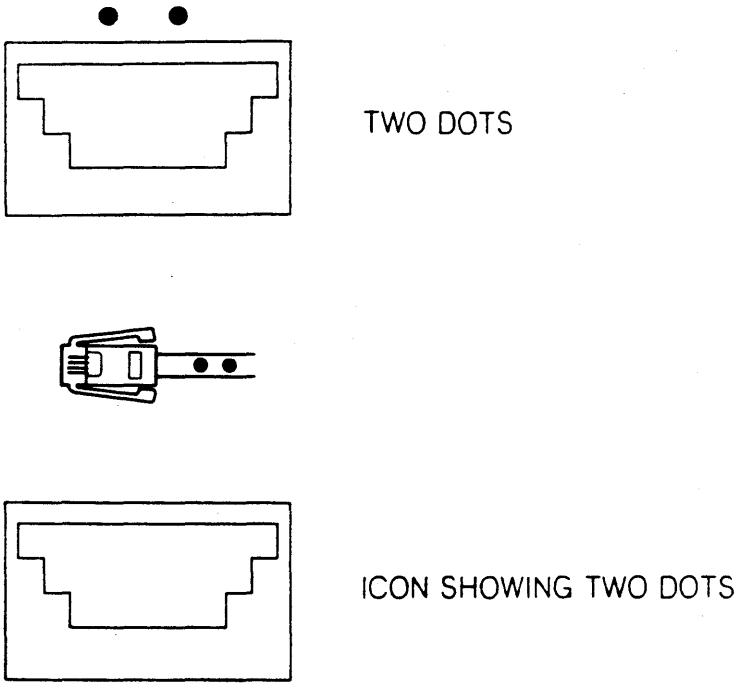


Figure 3-1. Receptacle Markings

Grounding

At the System end, the SDL connector shell (shield connection to cable) should be grounded to the System chassis ground. Additionally, the HP-HIL logic ground should also be connected to the System chassis ground. This is important for a proper drain path in electro static discharge (ESD) events. ESD will be conducted down the shield on the cable to the System, where it should then drain to safety ground. Typically, systems perform best where safety ground, logic ground, chassis ground, and HP-HIL shield are all connected perform best. Regulatory Agencies (UL, CSA, etc.) and their requirements must be considered during system design.

Power Supply

The 12 volts DC power supply connected to the HP-HIL port has two main requirements. First, the supply should provide a minimum of 750 milliamps. This is to allow for the maximum of 7 devices on the Link. Second, the power supplied to the Link MUST be limited to meet safety requirements. In addition to these requirements, the 12 volts should be bypassed at the SDL connector with both 0.01 and 25 microfarad capacitors.

The energy/current limiting for the power supplied to the SDL connector follow the various Information Processing Equipment safety standards used by various test houses such as CSA, UL, TUV, etc.

Designing for ESD and RFI

For best ESD protection, good grounding via separate discharge paths is necessary. Provide sufficient conductors back to earth ground. Protect ESD entry points by isolating internal circuitry or providing a discharge path. The shell of the HP-HIL receptacle should be well grounded and preferably connected to the System's chassis ground.

RF sources should be kept away from HP-HIL interface cicuitry and connector. This is necessary to keep internal energy sources from coupling onto the HP-HIL cabling and radiating. If a separate resonator is used for the MLC, keep the resonator close to the MLC. If a separate clock is used, route the clock line to minimize coupling onto the HP-HIL data lines.

Using the MLC

Refer to Figure 3-2 for an example of interfacing the MLC to an 8088 microprocessor. The example assumes that the data and address busses have been demultiplexed and latched from the System's microprocessor. Appendix I contains additional information on using the MLC.

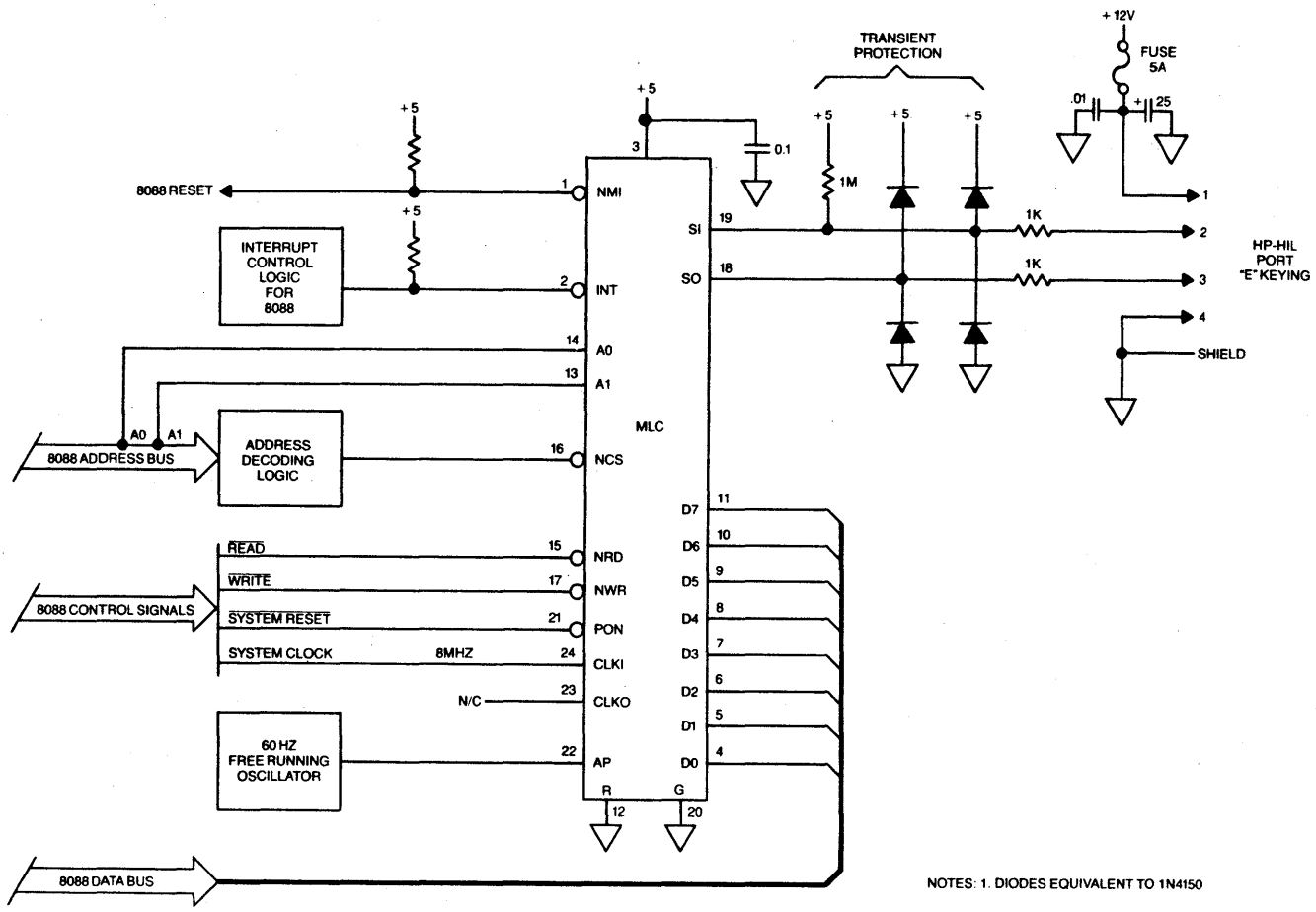


Figure 3-2. Example MLC Interface

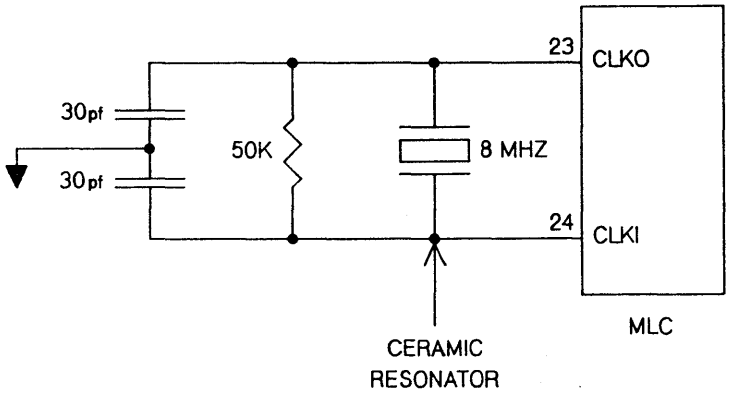
Connection to the MLC can be separated into three categories: data, address, and control signals. The MLC has three-state capability so buffering of data lines is usually not required. Eight data lines are provided by the MLC for connection to the host's data bus.

Address connections to the MLC are made through three pins. A0 and A1 are used to select the internal registers of the MLC. Typically these are connected to the processor's Address 0 and Address 1 lines, respectively. The third connection is to the NCS pin, which is the MLC chip select, and is logic 0 active. Decoding logic is required to generate the MLC chip select for the desired address(es).

The last connections from the processor to the MLC are the control signals. NRD and NWR are logic 0 true signals and should be connected to the processors Read and Write lines respectively. PON is connected to the System's reset line (logic 0 true) so that the MLC is reset upon power up or whenever the processor is reset.

If the System clock is 8.0 MHz (50% duty cycle), this can be tied directly to the MLC clock input, CLKI. If the System has a different frequency clock, then the System clock can be divided down to 8.0 MHz or a separate resonator can be

used. When the resonator circuit is not used, no connection is made to the CLKO pin. Figure 3-3 shows the resonator circuit which is connected between CLKI (clock input) and CLKO (clock output). The resonator is not a quartz crystal, but a ceramic resonator (similar concept). A dual capacitor of 30 picofarads per section and a 50K resistor are in parallel with the resonator to complete the circuit. The 50K resistor improves stability during transients and decreases the startup time. Recommended resonators are shown in the MLC appendix.



NOTE: Capacitors are packaged together.

Figure 3-3. Resonator Circuit

Optionally, the AP (auto-poll) pin can be connected to a 60 Hz clock if auto-polling is desired. The MLC data sheet (Appendix I) describes this feature in greater detail. The 60 Hz clock can be a stand-alone circuit or divided down from other clocks in the System. A stand-alone clock can be implemented with a timer IC and a few other components and typically results in better RFI performance. However, the accuracies and variations of the IC and components must be considered so that the clock will always operate in a frequency range of no more than +/- 10% (including time and temperature).

The MLC provides two interrupts, NMI and INT. NMI is the non-maskable interrupt and is used to reset the System microprocessor. INT is the interrupt which the MLC uses to signal the host processor that data or other information is

available. This should be connected to the System's interrupt controller or other logic used to handle incomming interrupts.

The HP-HIL output of the MLC is passed through a transient protection circuit before connection to the SDL receptacle. Fast clamping diodes (equivalent to 1N4150) are used on the SI and SO lines. The diodes clamp the input and outputs between +5 volts and ground. Placed in series with these lines between the diodes and the receptacle are 1K ohm resistors for current limiting. The 1M ohm resistor is to ensure that the SI line remains high if no devices are connected. As previously mentioned, depending on the design of the System, the 1K ohm resistors may have the second function of current limitation of the +5 volts for safety requirements.

The balance of the HP-HIL interface connections consist of the power, ground, and shield connections. As mentioned previously, +12 volts is fused and bypassed at the SDL receptacle. A fuse is not recommended due to difficulty of replacement. A preferred method is inherently limiting the available current output to less than 8 amps. Also, the logic ground and shield are connected as this provides the best performance in systems with a single ground.

DEVICE HARDWARE

Connectors

HP-HIL devices having two connectors will generally want to locate the ports on the rear of the device. However, the intended use and design of the device must be a consideration as to port location. As with systems, cable routing, accessibility, and clearances must also be considered. When devices locate the two connectors adjacent to each other, for consistency the receptacle for connection to the System (keyed as "A" on an input device) is found on the right of the other receptacle when facing the rear of the device. (See Section 2, Interconnection Method.)

Markings

HP-HIL receptacles should be marked using the same guidelines as for the System. It is especially important to make a clear distinction between the two ports and which end of the cable should be plugged into a given connector.

The device should also be marked to include the supply voltage (+12 volts DC) and the current consumption. These markings on the device are required as specified in Section 2.

Designing for ESD and RFI

ESD and RFI must be considered and planned for at the beginning of input device design. Input devices are especially vulnerable to ESD because of their intended "hands on" use. All openings, screws, conductive labels, and controls must be anticipated as possible entry points for static discharge. Circuitry protection from a direct strike must be the first concern, and data integrity next. Extensive testing is vital to establish the performance and reliability of a device under an ESD situation.

To prevent damage and drain ESD away, several steps have proven useful. A direct and low impedance path from any entry point on the device must be made to the HP-HIL shield. The shield is the cable shield and should not be connected with the logic ground in an input device. Shielding can be accomplished with sheet metal or direct metal deposition onto the device's case parts, depending upon the requirements and design of the device. When using metalized case parts, the most important detail is providing for a reliable and sturdy method to connect the case to the HP-HIL cable shield. Again, performance can only be verified through testing. The shield must be connected to both receptacles, as shown in Figure 3-4.

To minimize any RF radiation, the resonator circuit should be kept close to the SLC. The capacitor used with the resonator should have a good ground. Grounds should be short and preferably made into a ground plane.

When there is an RFI problem, it first must be isolated to the device or system. What can happen is the Link (cables and devices) will act as an antenna if the System is coupling RF energy onto the Link. This requires system modifications to better isolate the Link from any host RF problem areas. As with ESD, testing must be done to verify compliance.

5 Volt Regulator

Because input devices utilize the SLC, a 5 volt regulator will be required. Typically a 7805, LM330, or LM340 three terminal regulator is used, usually in TO-220 package. Depending upon the input device, a primary consideration is heat dissipation from the regulator. A typical input device using 100 milliamps of current with an input voltage of 12 volts, would dissipate 0.7 watts in the regulator alone. If the device is small, there is usually little room for heat sinks and virtually no ventilation. Heat sinks should be isolated from the shield. Care must be taken to prevent overheating and hot spots which may be uncomfortable for a user's hand on the device. However, for a device requiring little current, a smaller regulator could be used. On/Off switches are not employed in input devices to simplify design and add convenience for the user.

For added protection against polarity reversal (if an HP-HIL cable is forced into the wrong receptacle), it is recommended that some protection is used. Either a diode or regulator which can withstand polarity reversal is a good idea. Consider the minimum input voltage which the device will require to work reliably when selecting a protection method. The input bypass capacitor must also withstand the polarity reversal (if a diode is not used).

Safety Requirements

Plastic enclosure materials should have the correct flame ratings, as well as printed circuit boards and interconnection cables.

Example: Input Device Circuit

Shown in Figure 3-4 is an example circuit showning how the SLC can be used. The protection circuitry, resonator circuit, power regulator, and connections between J1 and J2 remain the same for nearly any input device. The protection circuitry is identical as was described under the System hardware, and is used on the signal lines from both receptacles. The resonator circuit is also the same as was discussed with the System. Power is supplied through the three terminal regulator equivalent to an LM330. Ground and shield connections are shown and described previously under grounding. An LM330 which can withstand reverse polarity is shown. The input filter capacitor will withstand the reverse polarity as well as the regulator. In this example, the input bypass capacitor is non-polarized.

The SLC uses a capacitor (0.22 microfarads) for a power-on reset. This provides sufficient delay so that the power and other hardware have sufficient time to settle before the SLC becomes active.

For illustration, a COP422 microprocessor is shown as it would be interfaced to the SLC. The microprocessor is then interfaced to the device hardware as required. This will vary depending on the input device and its characteristics. Note that other types of microprocessors can be used with the SLC. For additional information on interfacing the SLC, see Appendix J.

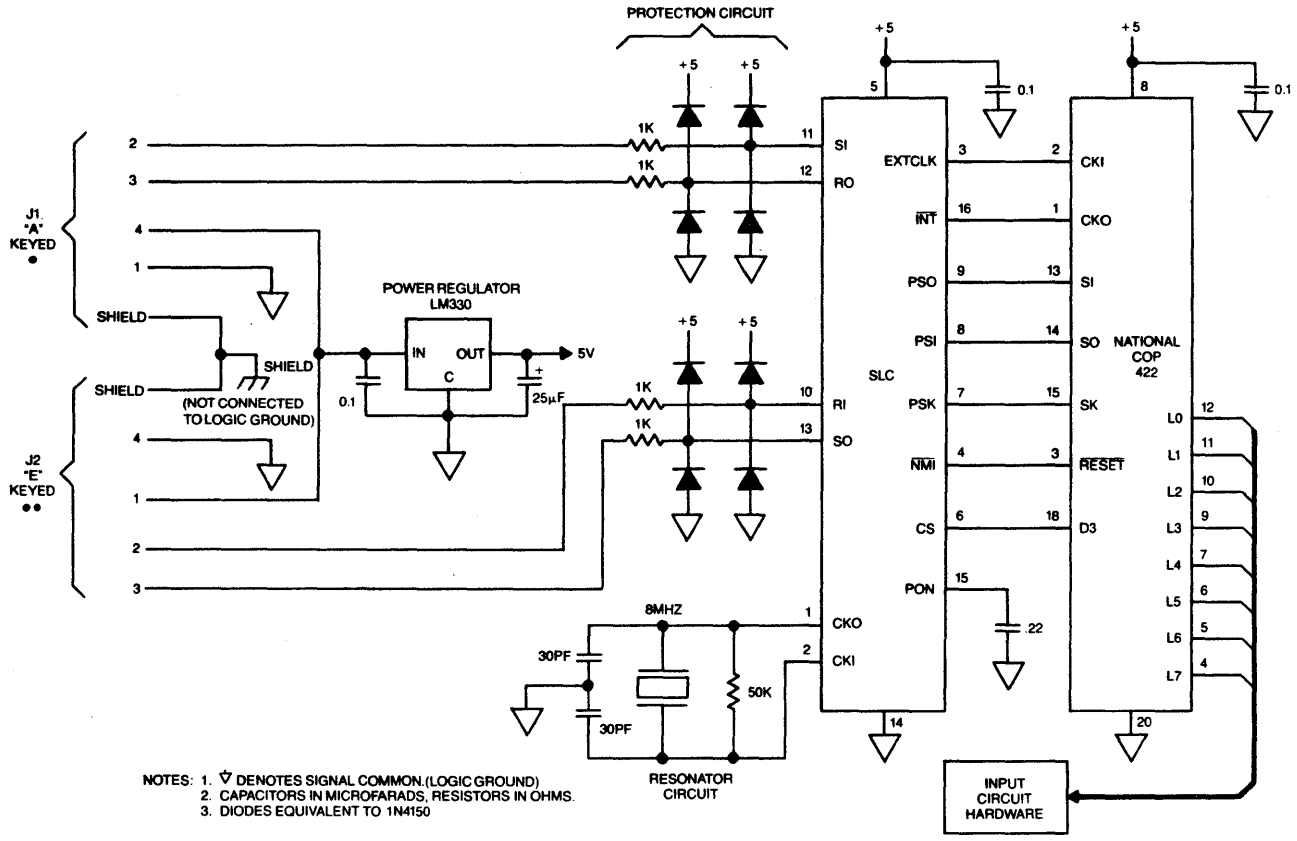


Figure 3-4. Example of SLC Use

HP-HIL PROTOCOL

SECTION 4

This section contains descriptions of the various HP-HIL commands, an extensive discussion of the Link operation from both system and device perspectives, and a discussion of the advanced features available with HP-HIL.

HP-HIL COMMANDS

This subsection will discuss the various HP-HIL commands, including their use, effects, and format when transmitted and received. Each command is assigned a two digit hexadecimal opcode, which appears in the command frame, and thus distinguishes what command is being sent (see Figure 1-13). For quick reference, each command has been assigned a three letter mnemonic. All the commands currently defined for HP-HIL, their opcodes and mnemonics are shown in Table 4-1. Note that there are many opcodes which are not defined. This is to allow for future enhancement of the HP-HIL command set.

Table 4-1. HP-HIL Command Set

Command Opcode (hex)	Mnemonic	Description
00h	IFC	Interface Clear
01h	EPT	Enter Pass-Thru Mode
02h	ELB	Enter Loop-Back Mode
03h	IDD	Identify and Describe
04h	DSR	Device Soft Reset
05h	PST	Perform Self Test
06h	RRG	Read Register
07h	WRG	Write Register
08 .. 0Fh	ACF	Auto Configure
10 .. 1Fh	POL	Poll
20 .. 2Fh	RPL	RePoll
30h	RNM	Report Name
31h	RST	Report Status
32h	EXD	Extended Describe
33h	RSC	Report Security Code
34 .. 3Ch		RESERVED FOR FUTURE USE
3Dh	DKA	Disable Keyswitch AutoRepeat
3Eh	EK1	Enable Keyswitch AutoRepeat, cursor key repeat rate = 1/30 second *
3Fh	EK2	Enable Keyswitch AutoRepeat, cursor key repeat rate = 1/60 second *
40 .. 46h	PR1 .. PR7	Prompt 1 .. Prompt 7
47h	PRM	Prompt (General Purpose)
48 .. 4Eh	AK1 .. AK7	Acknowledge 1 .. Acknowledge 7
4Fh	ACK	Acknowledge (General Purpose)
50 .. 7Fh		RESERVED FOR FUTURE USE
80 .. EFh		Device-Specific Commands
F0 .. F9h		RESERVED FOR FUTURE USE
FAh	RIO	Register I/O Error
FBh	SHR	System Hard Reset
FCh	TER	Transmission Error
FDh	CAE	Configuration Address Error
FEh	DHR	Device Hard Reset
FFh		RESERVED - Prohibited Opcode

General Information for Commands

In general, commands are always initiated by the System, although certain commands (described later) may be initiated by a device under the proper conditions. Unless otherwise noted, all commands will by definition be returned to the System (assuming a properly configured Link), preceded by any data reported by the addressed devices. Only one command should be pending on the Link at any one time; hence the System should always wait for either the command to return or a sufficient period of time so as to indicate that no response is forthcoming before the next transmission. HP-HIL devices are allowed up to 500 microseconds per frame to transmit their response after receiving a command. Allowing for data transmission times and worst case Link configuration, the System should receive the response to a command no later than 10 milliseconds after transmission in most cases. Commands which do not require data to be returned and those transmitted with device-specific addresses will return much more quickly. See Appendix A for specific time-outs associated with commands.

Note that some commands are generally sent with a universal address (address bits all zero) while others must always be used with device-specific addresses of 1 through 7. Unless otherwise noted, all commands are returned as transmitted, including the address bits A2 - A0.

HP-HIL devices always recognize commands and data with the universal address of zero, as well as any frames with an address field equal to the assigned address (match address) of the device. Frames which meet neither of these two criteria (such as data frames from a previous device) are automatically retransmitted by the SLC, and are therefore not acknowledged by the device. Any frame with a parity or framing error will be recognized by any device, and the appropriate action taken. Devices will ignore any commands which they are not programmed to support, simply retransmitting the command with no action taken. Data frames transmitted by the System to devices are not retransmitted, thus allowing large numbers of consecutive data frames to be sent to a device without danger of overflowing the SLC.

Note that opcode FFh (Prohibited Opcode) is not allowed for use on HP-HIL, since this particular opcode has a much higher likelihood of accidental generation at power-up or during other transient conditions. A device receiving opcode FFh will set Power-Up Mode, and if it was not previously in Power-Up Mode will send a Transmission Error (TER) frame.

Any deviations from the format described are considered error conditions, and should be dealt with appropriately, based on the operation being performed at the time. All commands not related to the configuration processes or error recovery assume a properly configured Link for correct operation.

Commands can be grouped into five basic categories. These are configuration, error recovery, data extraction, identification, and specialized commands. Some commands could be placed in more than one category, however each command usually has a primary purpose and will be categorized accordingly.

This information presented for the commands is general and intended to give an overview of what commands exist and their purposes. For more specific information concerning actual frames, records, timeouts, etc., see Appendix A and those appendicies pertaining to commands requiring lengthy descriptions.

Configuration Commands

Interface Clear (IFC, opcode 00h)

Interface Clear is used to clear error conditions on the Link and clear Power-Up Mode following following power-up, Device Hard Reset (DHR), Device Soft Reset (DSR), or detection of any error condition on the Link including Configuration Address Error, Transmission Error, Data Transfer Error, or reception of the prohibited opcode FFh.

The primary function of the command is to clear Power-Up Mode in the devices and to verify the integrity of the Link as configured. Interface Clear is generally transmitted with a universal address. No configuration information is affected by Interface Clear. Upon receiving the command, each device will clear Power-Up Mode, then retransmit the command as received.

Enter Pass-Thru Mode (EPT, opcode 01h)

Used during the configuration process, Enter Pass-Thru Mode allows the System to sequentially open up the Link to additional devices until the last device on the Link is determined.

Enter Pass-Thru Mode instructs the addressed device to set itself into Pass-Thru Mode, passing all transmitted frames onto the the next device in the Link. The device, upon reception of the command with the correct match address, places its SLC into Pass-Thru Mode, then retransmits the command. If another device exists on the Link, depending on that device's configuration and match address the command will either return to the System or continue down the Link. Enter Pass-Thru Mode will not return to the System if the addressed device is the last device on the Link. Note that this command should always be sent with a device-specific address.

Enter Loop-Back Mode (ELB, opcode 02h)

Also used at configuration time, the Enter Loop-Back Mode command is used to "close the end" of the Link, returning the last device on the Link to Loop-Back Mode so that frames may be returned to the System. At the end of the configuration process, the last device should be in Loop-Back Mode, while all others are in Pass-Thru Mode.

The HP-HIL device, upon reception of the Enter Loop-Back Mode command, places its SLC into Loop-Back Mode, then retransmits the command back to the System. Enter Loop-Back Mode should always be sent with a device-specific address.

Auto Configure (ACF, opcodes 08 ... 0Fh)

Auto Configure is used to assign unique addresses to each device configured onto the Link, up to the maximum of seven devices. The command may also be used to determine the number of devices configured at any time.

Although Auto Configure is specified as a range of commands, the System always transmits opcode 09h as the Auto Configure command. The low three bits of the opcode become the assigned match address of the receiving device, which then increments these three bits and retransmits the command. If there are eight or more devices on the Link, then the command would be received by the eighth device with opcode 08h, indicating an error. Auto Configure is always used with a universal address.

Error Recovery Commands

Device Soft Reset (DSR, opcode 04h)

Device Soft Reset serves to reset the Link configuration of all devices, without producing any data loss within the device. The command is used in error recovery where loss of any existing information within the devices is undesireable.

When a device receives the Device Soft Reset, it places its SLC into Pass-Thru Mode, retransmits the command, then places the SLC into Loop-Back Mode, clears the match address, and enters Power-Up Mode. The result is that all devices on the Link will receive the command, but it will not be returned to the System since the last device on the Link will enter Pass-Thru Mode and transmit the frame "off the end" of the Link.

Following the DSR command, all devices will be in Loop-Back Mode, Power-Up Mode, and match address clear (=0).

Device Soft Reset should be sent with a universal address, and should always be followed by an Interface Clear command, since Power-Up Mode will be set.

Perform Self Test (PST, opcode 05h)

This command causes the addressed device(s) to perform a self test, returning 1-15 data bytes indicating the results of the test.

Each device is allowed up to 200 milliseconds to complete its individual self test, after which the results of the test are transmitted as a data frames, followed by retransmission of the Perform Self Test Command as received. A single data byte of 00h indicates a successful test, with non-zero values representing device-specific failures. Also, devices with catastrophic failures may not respond to the PST command at all.

The reponse will vary in length from 1 to 15 data bytes, and thus should never be sent with a universal address or an MLC FIFO overflow may result.

RePoll (RPL, opcodes 20 ... 2Fh)

The RePoll command provides a means for recovering any information which may have been lost in response to a Poll which sustained some error. Devices will respond to the RePoll command with exactly the same information reported on the last Poll. This implies that if a device reported no data in response to the last Poll command, even if new data is available the device should respond with no data to the RePoll command. The RePoll command is also incremented in the same way as Poll, with the System always initiating the command with opcode 20h. RePoll is generally sent with a universal address.

Register I/O Error (RIO, opcode FAh)

Register I/O Error is generated by the device upon receipt of a Write Register or Read Register command which does not conform to the proper format, or upon receipt of any command not supported for data transfer following reception of a data frame. Note that reception of a Transmission Error during a data transfer may result in the device returning Register I/O Error as well, so it is recommended that reception of Data Transfer Error by the System always be followed by transmission of Interface Clear to reset any error conditions which may be present on the Link. Refer to the Read Register and Write Register commands for more details concerning Register I/O Errors.

System Hard Reset (SHR, opcode FBh)

This command is used to provide a Non-Maskable Interrupt (NMI) or Reset signal to the System processor, allowing for full System reset functionality using devices residing on HP-HIL.

System Hard Reset is the only command which may be initiated by a device without any action on the part of the System. It is trapped by the MLC IC, which lowers its NMI line and sets an internal bit as described in the MLC data sheet. Although the device initiating the command will transmit with its own match address associated with the Reset, the MLC ignores the address field in generating the NMI to the System. The SHR frame is not propagated through the MLC FIFO. Note that System Hard Reset does not affect the configuration of the Link in any way.

Transmission Error (TER, opcode FCh)

Transmission Error is initiated by a device detecting a Parity or Framing Error in a received frame, or by a device receiving the Prohibited Opcode of FFh.

This command is transmitted with the address of the device detecting the error. If the MLC detects a Parity or Framing Error, it places the Transmission Error frame with a universal address into the FIFO and interrupts the System processor. Note that the device generating the Transmission Error frame and any device receiving the frame with a matching address will set Power-Up Mode, and thus transmission of the Interface Clear command should be the next action by the System as part of the error recovery procedure. Devices with Power-Up Mode

set previous to detection of the error or reception of the Transmission Error command will not send the Transmission Error command.

Configuration Address Error (CAE, opcode FDh)

Configuration Address Error is an indication that too many devices are attached to the Link at any one time (more than seven), and it is impossible to assign a unique address to all devices. Note that the device which generates the Configuration Address Error frame and any device receiving it with the proper match address sets Power-Up Mode. For additional information concerning the conditions for a Configuration Address Error refer to the description of the Auto Configure command.

Device Hard Reset (DHR, opcode FEh)

This command provides a full reset to attached devices, destroying the Link configuration along with any pending device data. Device Hard Reset is used to return devices to their condition at power-up.

When a DHR is received by a device, the SLC lowers the NMI line to the device microprocessor. The SLC then goes into Pass-Thru Mode and retransmits the command as received to the next device or off the end of the Link. All devices on the Link will receive the command, and it will not return to the System. After 50 us, the NMI line is raised and the device begins power-up initialization.

Following the DHR command, all devices will be in Loop-Back Mode, and all device microprocessors will be in their power-on state. DHR is always transmitted with a universal address, and should always be followed by an IFC command since Power-Up Mode will be set.

Data Extraction Commands

Poll (POL, opcodes 10 . . . 1Fh)

The Poll command is the fundamental means for extracting information from the input devices attached to the Link. It provides a structure whereby character data, position data, and a limited amount of status information may be communicated back to the System in a single, consistent format. This information, used with that acquired by the Identify and Describe command, should allow for complete processing of most types of input device data.

Data returned from HP-HIL devices is in record form. Each device transmits its individual Poll Record, followed by the Poll command incremented by the number of data frames in the Record, only if sufficient room remains on the Link without overflowing the MLC FIFO. More than one device's Poll Record may be returned in response to a single Poll command. Note that it may not be required for the device to report all available information in response to a single Poll request; data may be split between Polls provided correct formatting is observed for each record reported.

For detailed information on the Poll Record, see Appendix E.

Read Register (RRG, opcode 06h)

Read Register and Write Register provide a means for interaction with more complex devices via HP-HIL, allowing for types of data transfer not generally supported by the HP-HIL devices.

A device indicates support of the Read Register command in the Extended Describe Record, also indicating the specific read registers contained in the device. To perform a register read, the System transmits a data frame containing the address of the register it is to read, followed by the Read Register command. The device, upon receiving the command, transmits the contents of the register indicated by the data frame, followed by retransmission the Read Register command.

Read Register, along with the register address, should be sent with a device-specific address.

Write Register (WRG, opcode 07h)

Write Register provides a means of setting the contents of individual registers in devices supporting this advanced feature, as well as providing the means for transmitting a large amount of data to a device at speeds approaching the Link maximum of 6500 bytes/second.

There are two forms of the Write Register Record which may be used separately or mixed in the proper order to provide the maximum degree of flexibility. Devices indicate support of the two types of Write Register in the Extended Describe Record. In Write Register Type I, the System transmits the register address, followed by the intended contents of that register. Several address/data pairs may be transmitted in sequence. In Write Register Type II, the System sends the several bytes to a single register in sequence. The register address is first sent (the high bit is set to 1 indicating Type II) followed by as many data frames as desired. In both, the data is always followed by the Write Register command. The device will never retransmit any data frames, and will respond only by retransmitting the Write Register command. The Write Register should be sent with a device-specific address only, as should all frames of the Write Register Record.

Identification Commands

Identify and Describe (IDD, opcode 03h)

Identify and Describe is used by the System to determine the type of the attached devices, as well as some general characteristics of these devices required to understand the data they report. The command is usually transmitted immediately following the configuration process, before any polling of devices takes place.

Each device responds to the Identify and Describe command with a device ID byte, followed by a series of data bytes referred to as the Describe Record, followed by retransmission of the original command as received. The Record will vary in length from 1 to 10 data bytes. Additional information about individual bytes of the Describe Record can be found in Appendix C.

Following the Describe Record will be the original command as received by the device. Note that the IDD command should never be sent with a universal address or an MLC FIFO overflow may result.

Report Name (RNM, opcode 30h)

Report Name is used to request a string of up to 15 characters (8-bit ASCII) which would aid in describing the device to the user. The command should always be sent with a device-specific address to avoid the possibility of a MLC FIFO overflow. Devices indicate support of the Report Name command in the Extended Describe Record.

Report Status (RST, opcode 31h)

Report Status is used to extract device-specific status information from devices configured on the Link. Devices indicate support of the Report Status command in the Extended Describe Record. Devices supporting the command will respond with from 1 to 15 bytes of device-specific status information, followed by retransmission of the command as received. Interpretation of the status bytes will necessarily depend upon the device in question. Report Status should always be sent with a device-specific address.

Extended Describe (EXD, opcode 32h)

Support of the Extended Describe command is indicated in the Describe Record header. It provides additional information concerning more advanced device features which may not be required for basic operation.

Devices supporting the Extended Describe command respond with a series of data bytes referred to as the Extended Describe Record, followed by retransmission of the command as received. The record length may vary from 1 to 15 bytes (although only 6 bytes are currently defined), and thus should never be sent with a universal address. See Appendix D for specific information on the Extended Describe Record.

Report Security Code (RSC, opcode 33h)

The Report Security Code command is used to extract a unique identifier from the device. Support of the command is indicated in the Describe Record Header. The security code is a record of from 1 to 15 bytes which uniquely identify the device in question, followed by retransmission of the Report Security Code command. Similar in purpose to a serial number, it may also contain information related to user identity, network address, or other information which is unique to a particular user or environment. The command should always be sent with a

device-specific address. See Appendix H for more information on the Report Security Code Record.

Other Commands

Disable Keyswitch AutoRepeat (DKA, opcode 3DH)

This command is used to disable the "repeating keys" feature in the addressed device, reducing returned data to one report per keyswitch transition. Disable Keyswitch AutoRepeat may be sent with either a universal or device-specific address. The device responds by retransmitting the command as received. The default state for devices supporting this command is AutoRepeat disabled.

Enable Keyswitch Autorepeat (EK1, opcode 3Eh; EK2, opcode 3Fh)

These two commands are used to enable the "repeating keys" feature in the addressed device (if the feature is supported). Generally keys will repeat at the rate of one report every 1/30 second (based on a System Poll rate of 1/60 second). Modifier keys (Shift, CTRL, Extend char, etc.) will not repeat, while based on the opcode of the Enable Keyswitch AutoRepeat command the Cursor Keys (cursor left, right, up, and down) will repeat at either 1/30 second intervals (opcode 3Eh) or 1/60 second intervals (opcode 3Fh). Most keys "repeat" by generating repeated down transitions corresponding to the key position being repeated, although repeating Cursor Keys will report a keycode of 02h. The response of the device to the Enable Keyswitch AutoRepeat commands is retransmission of the command as received. More advanced key repeat features may be implemented using device-specific commands.

Prompt 1 .. Prompt 7 (PR1 .. PR7, opcodes 40 .. 46h, respectively)

These commands are used to provide an audible or visual stimulus to the user, perhaps indicating that the System is ready for a particular type of input. Although intended to be directly associated with Acknowledge 1 .. Acknowledge 7 and Button 1 .. Button 7, this association is not a requirement.

Due the possible prolonged nature of executing a Prompt command, the device, upon receiving the command, will retransmit the command, then execute the Prompt functionality. The Prompts supported by the device are indicated in the Describe Record. All unsupported Prompts will be treated the same as other unsupported commands. Prompt 1 .. Prompt 7 should generally be transmitted with a device-specific address.

Prompt (PRM, opcode 47h)

Intended as a general-purpose stimulus to the user, Prompt is not intended to be associated with a particular Button as are Prompt 1 .. Prompt 7. A device indicates support of Prompt in the Describe Record, and responds to the command by retransmitting it as received. A device-specific address should be used.

Acknowledge 1.. Acknowledge 7 (AK1 . . AK7, opcodes 48 . .4Eh)

These commands, similar to the Prompt 1 .. Prompt 7 commands, are intended to provide an audible or visual response to the user, and are generally directly associated with the corresponding Prompt and Button of the same number, although this is not a requirement. The device responds to Acknowledge 1 .. Acknowledge 7 by retransmitting the command, then executing the function. Unsupported Acknowledge commands are retransmitted with no action taken. Acknowledges should be sent with device-specific addresses. Since there is no explicit "Prompt Off" function provided, this functionality may be part of the Acknowledge definition for a particular device, if required.

Acknowledge (ACK, opcode 4Fh)

Similar to Prompt, Acknowledge is not associated with any particular Button, but merely as a general purpose audible or visual response to the user. The device responds to Acknowledge by retransmitting the command as received, then executing the function if supported. Acknowledge should be sent with a device-specific address.

Device-Specific Commands (opcodes 80 .. EFh)

A range of 112 commands has been reserved for use as "device-specific" commands. The commands are intended for use by devices with special requirements which the remainder of the HP-HIL protocol does not readily support. The commands should only be used to access specific device features not supportable through the use of commands such as Read and Write Register and the Prompts and Acknowledges to help maintain the uniformity of the HP-HIL command set and functionality.

HP-HIL SYSTEM OPERATION AND CONTROL DIAGRAM

This section describes the basic sequences of HP-HIL commands required to initialize the Link, collect data from input devices, request the devices to perform diagnostics, and perform error recovery. All System implementations of HP-HIL must include these capabilities, and all HP-HIL devices must support these command sequences.

The control of the Link by the System is shown graphically in Figure 4-1. This diagram is not a state diagram, but is intended to show how the System deals with configuration, error recovery, polling, adding devices, and special commands. The notation used in Figure 4-1 follows:

Definitions:

ERR — Error condition. The command did not return as expected, possibly due to a Link parity or framing error.

TO — Time Out. A time out will occur if the System does not get a response from a command.

INT — Interrupt. This is an interrupt generated by the MLC in response to the anticipated frame/data returning to the MLC.

DC — Device Count. This is the number of devices configured onto the Link, and can have a value from 0 to 7.

Notation:

\+ — Logical "OR".

o — Logical "AND".

⬭ — The ovals indicate that a command is to be sent out on the Link and/or another action is also to be taken. This is indicated inside of the oval. Commands are referenced by their three letter mnemonic (see Table 4-1). After the action is taken (e.g., a command is issued), the System will wait until a condition (indicated on the connecting lines between ovals) becomes true. Control will then transfer to the oval indicated by the true condition.

⟶ — The connecting lines indicate control flow based upon a condition (indicated on the line) being true.

Notes for Figure 4-1:

(1) This path is taken when the System checks for added devices.

(2) This path is taken when the System continues polling.

(3) This path is taken when the System is going to issue a special command to the Link. For example, a RSC or PST command.

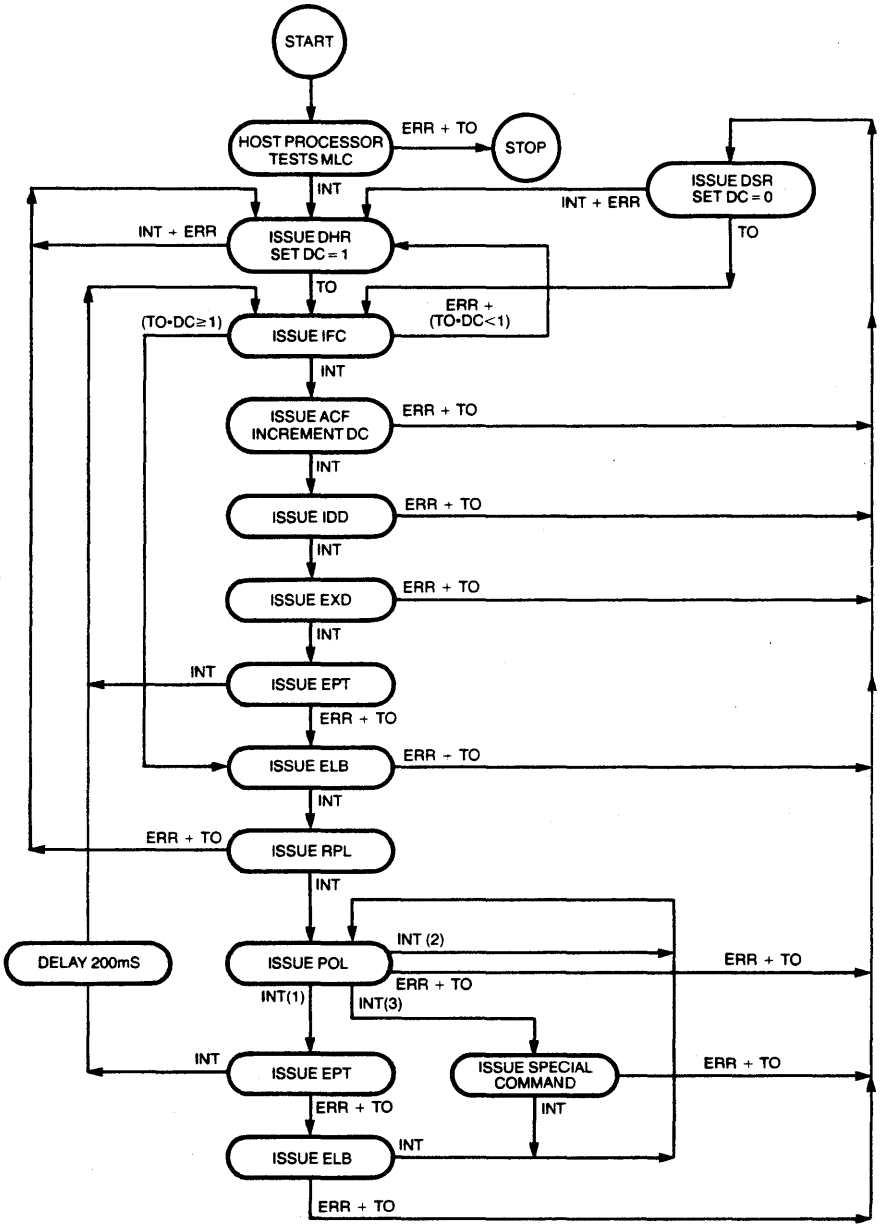


Figure 4-1. System Control Diagram

Referring to Figure 4-1, the control process for HP-HIL can be broken up into four major areas of operation. These are configuration and error recovery, polling (data collection), adding devices to the Link, and handling special commands. Note that control of HP-HIL from the System is based upon timing or interrupts which cause the System to take action. Because of this, the controlling software will generally not be running continuously, but will be part of a larger interrupt driven environment. Thus, after an action has been taken, during the waiting for a condition to become true and cause the next action to be taken, the host processor will generally be doing other unrelated tasks.

Configuration begins with the System testing the MLC. This is done by setting the MLC in Test Mode, and writing frames into registers W0 and W1. If the frames are received in the FIFO, an interupt is generated. If the frames in the FIFO match the frames transmitted, then the MLC has passed the test. If an error or a timeout occurs, then something is wrong with the MLC. Before proceeding, the cause of the error must be cleared. At this point, a message to the console is usually necessary to encourage user participation.

Note that the control diagram relies on timeouts. A timeout occurs when a response to an action is expected, but does not occur. Thus a timeout allows the System to interceed and take appropriate action rather than allow control to come to a halt. Timeouts durations vary depending upon the command and the expected response. Appendix A gives timeout information for all of the HP-HIL commands. The typical response to a command being issued is the command (or data) returning to the MLC and an interrupt being generated.

When the MLC has passed its test, control passes to the next oval and a DHR (Device Hard Reset) is sent. The device count (DC) is cleared at this point. Because DHR should not be received by the MLC, the correct action will be a timeout occurring. An interrupt indicates a frame was received which is not expected. For an interrupt or an error, the action repeats by issuing another DHR. A stop point could inserted here if additional DHRs do not correct the problem. All devices on the Link should now be in Loop-Back Mode, Power-Up Mode (PUP Mode), and have a cleared match address (=0). Graphically, the condition of the Link is shown in Figure 4-2. A more detailed discussion of PUP Mode can be found later in this section under "HP-HIL Device Operation and Control Diagrams."

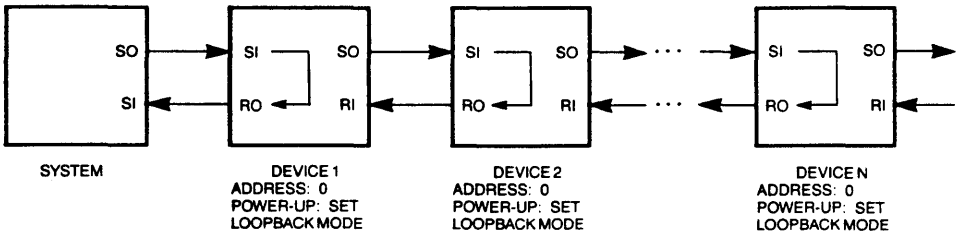


Figure 4-2. Link Power-Up State

At this point, the configuration process begins. This process can be seen as a loop in Figure 4-1, consisting of IFC, ACF, IDD, EXD, EPT, and back to IFC. The goal of the configuration process is to assign a unique address to each device on the Link, placing all but the last into Pass-Thru Mode. In the process each device may be requested to identify itself and report parameters necessary for scaling the device data to the System and utilizing any advanced features of the device.

Once the timeout has occurred following the DHR, an IFC (Interface Clear) is issued with a universal address. This causes any errors and PUP Mode to be cleared from the first device only since all devices are in Loop-Back Mode (the IFC command will only reach the first device). The IFC command is then transmitted back to the System. If an error or timeout occurs, then control will go back to the DHR oval. If no errors have occurred, and the IFC returned to the MLC, then control passes to the ACF (Auto Configure) oval.

The System sends the Auto Configure command (opcode 09h), again with a universal address. This assigns a match address of 1 to the first device, which returns the command incremented by 1 (opcode 0Ah). DC is incremented by 1 to reflect a new device being configured onto the Link.

Next, the IDD (Identify and Describe) command is issued with a device address of one. Device One will then report its ID and other characteristics of the device. If data is not received or if an error occurs, control passes to Device Soft Reset. DSR is used first (rather than going directly to DHR) as part of the error recovery process to save any pending data. With data returning to the MLC and generating an interrupt, the EXD (Extended Describe) command is issued.

Similar in operation to the IDD, the EXD allows the System to get information on what advanced features Device One supports. As with the IDD, error and timeout routes control back to DSR. Following the EXD is EPT, Enter Pass-Thru.

The System now transmits the Enter Pass-Thru command (opcode 01h), addressed to Device 1. The device sets its SLC to Pass-Thru Mode, then retransmits the command to the next device. Since the command carries address 1, the SLC in Device 2 automatically retransmits the command back to the System. The Link configuration now appears as in Figure 4-3.

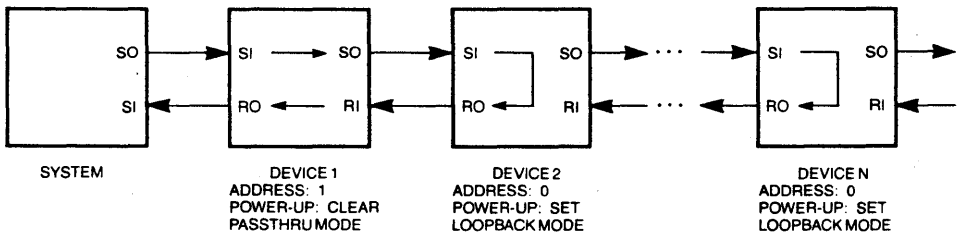


Figure 4-3. Link Configuration, First Device Configured

If the Enter Pass-Thru command was returned, it is evident to the System that additional device(s) exist beyond Device 1. If the command did not return, then the System would know that there was only a single device on the Link. When additional devices are present, an interrupt occurs and control transfers back to the IFC oval. Note that the IFC command does not affect device configuration information.

The System transmits a universal Interface Clear. This has no effect on Device 1, which retransmits the command to Device 2. Device 2 clears Power-Up Mode and returns the command to the System. The System follows with the Auto Configure command (universal address). Device 1 maintains address 1, increments the opcode to 0Ah, then transmits the command to Device 2. Device 2 assumes match address 2, increments the opcode to 0Bh, then returns the command to the System. Identify and Describe is sent to Device 2 at this time, followed by Enter Pass-Thru (again to address 2). The next device on the Link returns the Enter Pass-Thru command addressed to Device 2 back to the System, leaving the Link configuration as shown in Figure 4-4.

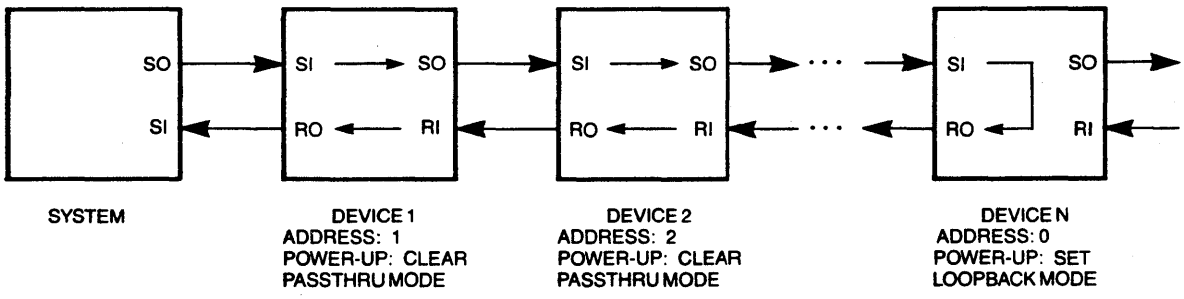


Figure 4-4. Link Configuration, First and Second Devices Configured

This process continues, configuring N devices onto the Link, until the Enter Pass-Thru command to a specific device is not returned, indicating no additional devices are attached, and the Link configuration appears as shown in Figure 4-5.

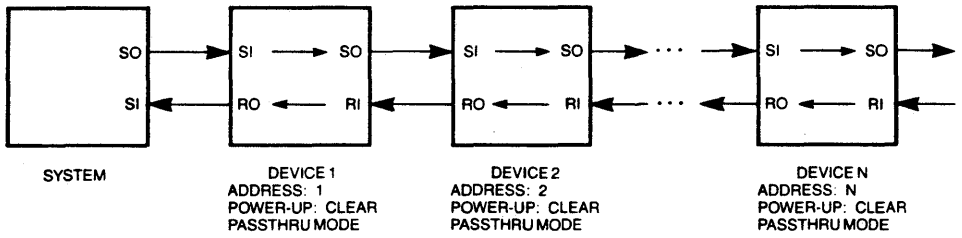


Figure 4-5. Link Configuration, Last Device Configured

When the EPT command is not returned, a timeout occurs transferring control to the ELB (Enter Loop-Back Mode) oval. The System transmits the Enter Loop-Back command (opcode 02h) to Device N, which places its SLC back into Loop-Back Mode, and returns the command to the System. The Link, now fully configured, is illustrated in Figure 4-6.

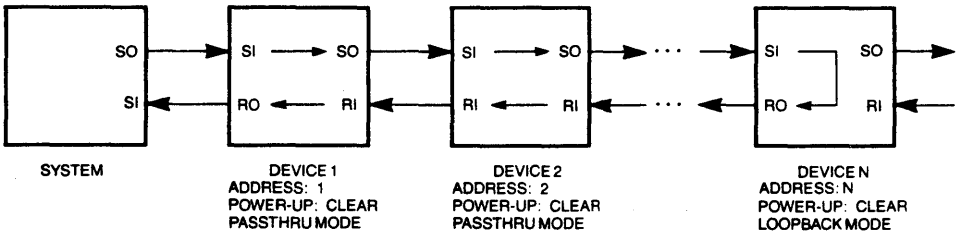


Figure 4-6. Link Configuration, All Devices Configured

Polling

Once the Link has been fully configured as described above, the input devices are ready to be Polled. The System may initiate HP-HIL Polls either by manually transmitting the Poll command or by configuring MLC to perform Auto Polling. Since in either case the transmitted opcode remains the same, the Polling method used is transparent to the attached devices. Auto Polling generally requires less time from the System processor for continuous operation, and is therefore the choice of most Systems. In addition, the use of Auto Polling guarantees a regular Poll interval, which may be required for optional device features such as Keyswitch AutoRepeat.

Typical input devices should be polled for data approximately 60 times per second to maintain acceptable performance levels. Significantly slower poll rates may result in lost key transitions or unacceptably coarse cursor movement; while quicker poll rates may result in false keyswitch transitions due to keyswitch bounce being reported, along with a general degradation of input device performance (due to the increased time spent servicing the HP-HIL interface).

To initiate Auto Polling, the System should first set the Ignore Poll Frame (IPF) bit in MLC register W2. This will prevent incoming Poll commands with opcode 10h (indicating no device data reported) from interrupting the System processor. The Auto Poll Enable bit (APE) should then be set in MLC register W3. This initiates Auto Polling with the next rising edge on the Auto Poll pin of MLC, continuing until an error on the Link or a device reports data in response to the poll, at which time the System processor is interrupted and APE is cleared. To continue Auto Polling, the System must set the APE bit as part of the MLC interrupt service routine. Typically the Auto Poll pin will be tied to a 60 Hertz clock signal, providing the optimum HP-HIL Polling rate.

To terminate Auto Polling at any time other than on a MLC interrupt, the System processor should clear the IPF bit in MLC. This will result in the last Poll command initiated by MLC during Auto Polling producing an interrupt (even if no device data is reported), clearing the APE bit and returning MLC to the state before Auto Polling was initiated. For more information concerning the various control bits in MLC, refer to Appendix I.

Referring again to Figure 4-1, after the configuration of all devices has been completed, the next action to occur is the issuing of the RPL (RePoll). RPL is placed here as part of the error recovery process. If devices transmitted data, and an error occurred during polling, the Link would be reconfigured, and the lost data may be retrieved by the RPL command. If the Link is being configured for the first time, and polling has not yet started, the RPL command will not have any effect.

After the RPL command returns, the POL (Poll) command is sent. The System controlling the Link will remain in this oval most of the time. As explained above, polling can take place on a automatic (Auto Poll) basic or on an individual basis. To continue polling, control returns to the same oval, along the path marked with note (2). No other commands are required between polls. Errors or timeouts transfer control to the DSR oval at the top right of Figure 4-1. Two other conditions may cause polling to suspend. These are checking for added devices on the Link and processing special commands (e.g., Write Register).

Checking for Added Devices

It is possible to check for devices added to the end of the Link after the configuration process is complete and device polling has begun. However, checking for added devices is not an automatic feature of HP-HIL. Generally, the System should check for added devices about one time per second. Checking more or less often depends upon overhead and performance requirements.

Checking for additional devices is similar to the end of the configuration process. Control transfers from polling along the path marked with note (1). The EPT command is sent to the last device currently configured on the Link. This allows the System to determine if another device has been added to the Link. If a timeout occurs, then the command was retransmitted "off the end" of the Link. This means there is not an added device. If an interrupt occurred, then there must be an added device (devices power-up in Loop-Back Mode).

An added device (interrupt occurred) produces a 200 ms delay (allows for device self-test), sends control to the IFC oval and the configuration process begins for the added device. After configuration, control again ends up at the POL oval, device polling resumes again.

When there is no added device, a timeout occurs and control passes to the ELB oval. This command is sent out to the last device on the Link which puts it in Loop-Back, closing the end of the Link. When the frame returns, an interrupt is generated and polling begins again. Errors and timouts are again transferred to the DSR oval.

Processing Other Commands

It is very important when utilizing advanced features (special commands) that the performance of the Link as the primary human-input interface for the System is not compromised. In order to disrupt the input functionality (Polling) of the Link as little as possible it is suggested that transmission of Poll commands be interleaved with the optional commands being used, maintaining a minimum poll rate of 30 Polls per second. This allows approximately 50% of the Link capacity for use of any advanced commands, while minimally impacting input performance.

When other commands are to be issued, the polling process is exited and the System then proceeds with the new command. This is shown in Figure 4-1 with control transfer occurring along the route marked with note (3). Other commands includes all those commands not explicitly shown in Figure 4-1, such as Register commands, Report commands, Prompts, Acknowledge, etc., and commands which are device specific. These commands are explained in Appendix A.

HP-HIL extensions which take advantage of specific device capabilities not required for basic Link configuration, data acquisition, and error recovery are not supported by all devices. However, all Systems should possess the ability to access these features, even if not supported in the default operating mode.

Error Recovery

Errors may occur under various conditions on HP-HIL, and the correct System response to these errors varies as well. However, there are recovery procedures which apply to most situations, and these are described here. Refer again to Figure 4-1.

During most processes, the normal error recovery path is to attempt recovery without losing data. If recovery is not made, then more drastic steps are taken. As shown in the System Control Diagram, errors and timeouts transfer control to the DSR oval. Here a Device Soft Reset is issued, causing all devices on the Link to go into PUP Mode. If a timeout occurs, then an IFC is issued and the Link is reconfigured as described earlier. Because the DSR command does not produce any data loss in the devices, the RPL (RePoll) command will gather any data which the devices had transmitted when the error occurred. If the DSR was indeed successful at clearing the error, then the configuration

will be completed, the RPL will get any previously pending data, and polling will resume.

Note that for the RePoll command, an error or timeout transfers control to DHR, not DSR. The jump to DHR will insure correction of the error condition and reestablish Link intergrity, although device data loss may occur.

If an interrupt or error occurred after the DSR command was issued, then the error condition was not cleared. In this case, a Device Hard Reset (DHR) is issued. The DHR does cause data loss in the devices. At this point, the configuration process begins as if the System had just powered up. The Link will be reconfigured and polling will begin again. As stated previously, if the DHR does not clear the error, then the next level of error recovery would be user intervention (power cycling the devices and/or the entire System).

ADVANCED FEATURES

HP-HIL extensions which take advantage of specific device capabilities not required for basic Link configuration, data acquisition, and error recovery are described here. These commands will not be supported by all devices, although all Systems should possess the ability to access these features, even if not supported in the default operating mode.

As stated previously, when processing special commands, the Link performance must not be compromised. This means that a minimum poll rate of 30 Polls per second should be maintained. The optional commands may be interleaved with the Poll commands.

Prompts and Acknowledges

Prompts and Acknowledges represent the simplest form of Link output. Generally speaking, a Prompt is an audible or visual indication to the user that the System is ready for some form of input. Similarly, an Acknowledge is an indication to the user that the input has been received. Prompts and Acknowledges may be associated with specific Buttons on input devices, or may be used as general purpose output commands. Devices supporting the Prompt/Acknowledge functionality will indicate the level of support in response to the Identify and Describe command transmitted by the System during the configuration process. Refer to Appendix A for details concerning the syntax of the Prompt and Acknowledge commands.

Register Operations and High-Speed Output

The Read Register and Write Register commands (opcodes 06h and 07h) allow for types of data transfer not normally supported by HP-HIL. A device may contain up to 128 read registers and 128 write registers, as indicated in the device's response to the Extended Describe command.

Read Register may be used for accessing device data which does not conform to the standard formats defined within the Poll Record. It may also be used to extract complex status information from a device. Write Register, on the other hand, may be used to alter specific registers in a device to control device-specific configuration parameters, or for rudimentary device programming. Other uses for the Write Register command include transmitting large amounts of data to a specific device register at data rates approaching the Link maximum. The maximum number of data frames the device is capable of receiving at one time is reported in response to the Extended Describe command.

Any errors detected by a device during data transfers with Read Register or Write Register result in the addressed device returning the Register I/O Error opcode rather than the anticipated response. If this occurs, the System should transmit an Interface Clear (universal address) to clear any device errors and verify proper Link operation, then attempt to repeat the data transfer, being certain to conform to the syntax defined in Appendix A.

Additional Functions

Other features which may optionally be implemented in HP-HIL devices are used to switch the AutoRepeat functionality of a Keyboard, to request the name (in ASCII) of a device not defined in the Device ID Byte Definition (Appendix B), or to request the status of an HP-HIL device. The syntax required for the use of these commands, along with limitations on their usage, are described in Appendix A. Due to the device-dependent nature of these commands, implementation details should be contained in the documentation for the device.

HP-HIL DEVICE OPERATION AND CONTROL DIAGRAMS

This section deals with HP-HIL devices and how they handle the Link protocol. In this section, flow diagrams are used to show how the device microprocessor should be controlled. The flow diagrams show a recommended method of controlling a device. Other methods may also be acceptable, however, attention should be paid to the levels of priority inherent in these diagrams.

The control diagrams shown here are an example of how the HP-HIL firmware may be implemented for a simple input device. The diagrams show support of the basic commands only. A more sophisicated device would need to integrate added features and special command support into the given diagrams.

The notation used in Figures 4-7 thru 4-13 is simple. Circles represent points of entry, exit, or control transfer (i.e., go to a subroutine). Rectangles depict a process which is to occur at that point. Finally, diamond shapes show a decision process, often a yes or no result, but sometimes multiple paths are shown when there is a branching action.

Device control can be grouped into four areas. These are initialization, data processing, command processing, and error recovery. Note that the last two groups are interrupt driven.

Initialization

Shown in Figure 4-7 is the HP-HIL Device Control Diagram. This is the upper or top level of control from the device firmware point of view. Upon power-up, the initialization process starts. This means any clearing of registers or memory, setting any flags, reading an ID number, etc. Next the firmware performs a self test on the device. If the self test passes, then the SLC is initialized by setting Master Mode clear, Test Mode clear, Match Address clear, Pass-Thru Mode clear (thus SLC is in Loop-Back Mode), and PUP (Power-Up) Mode is set. With the initialization process complete, the device spends all its time processing interrupts and generating data.

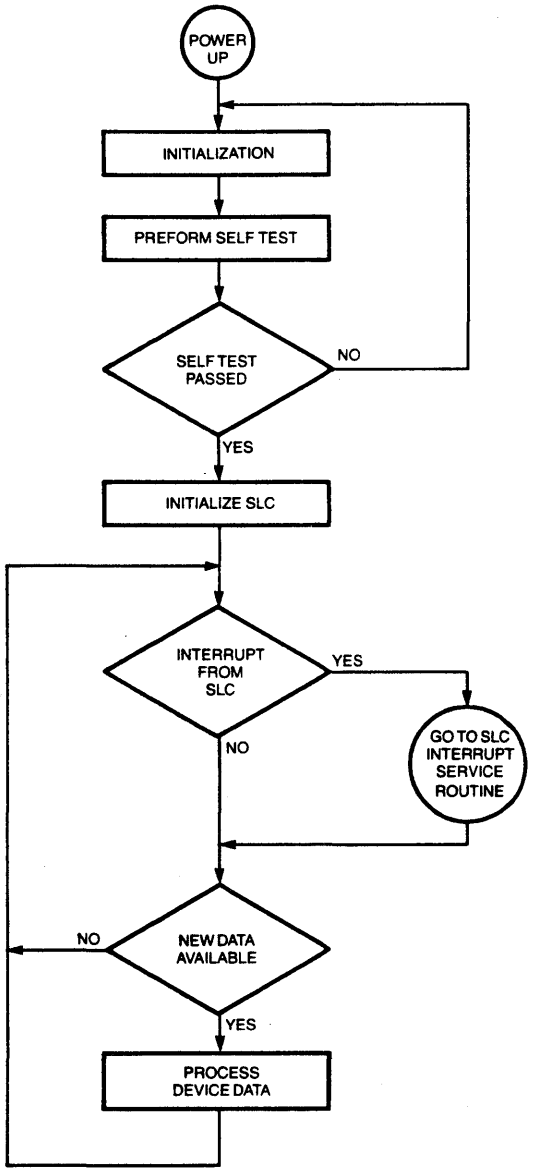


Figure 4-7. HP-HIL Device Control Diagram

PUP Mode

At this point, a description of PUP (Power-Up) Mode is necessary. PUP Mode is necessary so that there is a known state that the device will go into upon power-up or upon an error condition. PUP mode will be set upon power-up, reception of a Device Soft Reset (DSR), reception of a Device Hard Reset (DHR), or reception of any error except a Register I/O (RIO) error. A RIO error indicates that an error occurred because of a software related problem as oposed to a Link problem (parity or framing error), and does not typically require Link reconfiguration.

Only an Interface Clear (IFC) will take the device out of PUP Mode. Note that the device microprocessor keeps track if the device is in or out of PUP Mode. Also, when a device is put into PUP Mode, other configuration information (flags, match address, etc.) is not lost. Thus if an error occurs and the device goes into PUP Mode, upon reception of an IFC, the device can return to a normal operating state without loss of data. A complete reconfiguration of the Link is generally not necessary as well.

Data Processing

If an interrupt is not pending, then the device checks to see if new data is available. It is important to make the distinction between existing data and new data. If data has already been available (processor has passes through this loop once before), but is still waiting to be transmitted, then the data is not new. New data is that which has not been collected or seen by the device microprocessor before.

To process the data, the processor must format the data so that it is in the correct form to be transmitted onto the Link in response to a Poll command. This includes necessary multiplications, divisions, additions, separating high and low bytes, translating key closures to keycodes and transitions, etc.

Interrupt Handling

When the SLC interrupts the device processor, control transfers to the interrupt service routine. The interrupt service routine is shown in Figure 4-8. There are two basic functions handled in this routine, error recovery and command sorting. Once in the routine, the processor reads the frame received by the SLC and checks for a parity or framing error. If an error has occurred, then PUP Mode is set. If PUP Mode is already set, then control returns to the top level, and the processor continues looking for data and interrupts. If the SLC was already in PUP Mode, a Transmission Error (TER) is not transmitted. If not, then the processor instructs the SLC to issue a TER and returns to the top level.

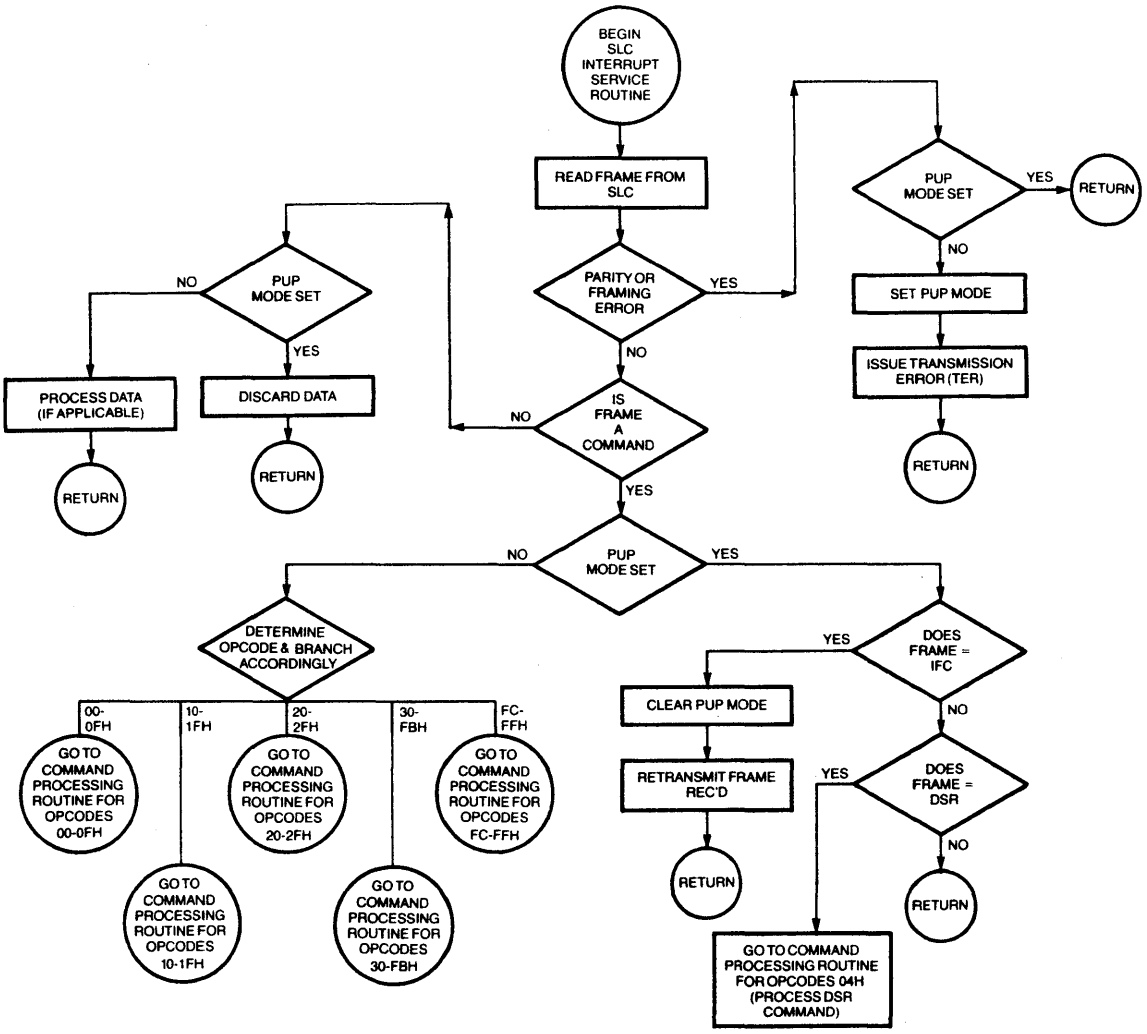


Figure 4-8. Device Interrupt Service Routine

If no error has occurred, then the frame command bit is checked. If clear (0), then control transfers to the left and PUP Mode is checked as shown in Figure 4-8. If PUP Mode is clear, then the frame is a data frame and should now be processed, if applicable. An example might be a data frame which preceeds a Write Register command. However, if the device does not support the Write Register command, then the data cannot be processed and control returns to the top level. If PUP Mode is set, then the data is discarded because the device must ignore data when in PUP Mode. Control returns to the top level.

When the frame is a command (and no errors have occurred), then PUP mode is checked. With PUP Mode clear, then the command opcode is determined. Control then passes to a command processing routine depending upon the range which the opcode falls. Here, there are five different routines used to process all HP-HIL commands. Processing of commands is explained in detail under the section Command Processing.

Finally, if the frame was a command, and PUP Mode is set, then the opcode is checked to see if the command is an IFC or DSR. If an IFC, then PUP Mode is cleared and the frame is retransmitted as received. If the command was a DSR, then this is processed just as if PUP Mode was not set by jumping to the appropriate command processing routing (and processing the DSR command). If the frame was neither an IFC or DSR, then control returns to the top level. Only the IFC and DSR commands are active in PUP Mode, all others are ignored and not transmitted.

Command Processing

Command proccessing is handled by five routines, shown in Figures 4-9 thru 4-13. Each routine handles a range of opcodes such that all HP-HIL commands are covered. For the most part, the routines show the steps required to process all the various commands and follow closely with the information given in Appendix A.

Processing for commands with opcodes 00h thru 0Fh are shown in Figure 4-9. For opcode 00h, the command is retransmitted since IFC requires processing only when the device is in PUP Mode (see Figure 4-8). Opcodes 06h and 07h (RPG and WRG) are retransmitted because they are not supported in this example.

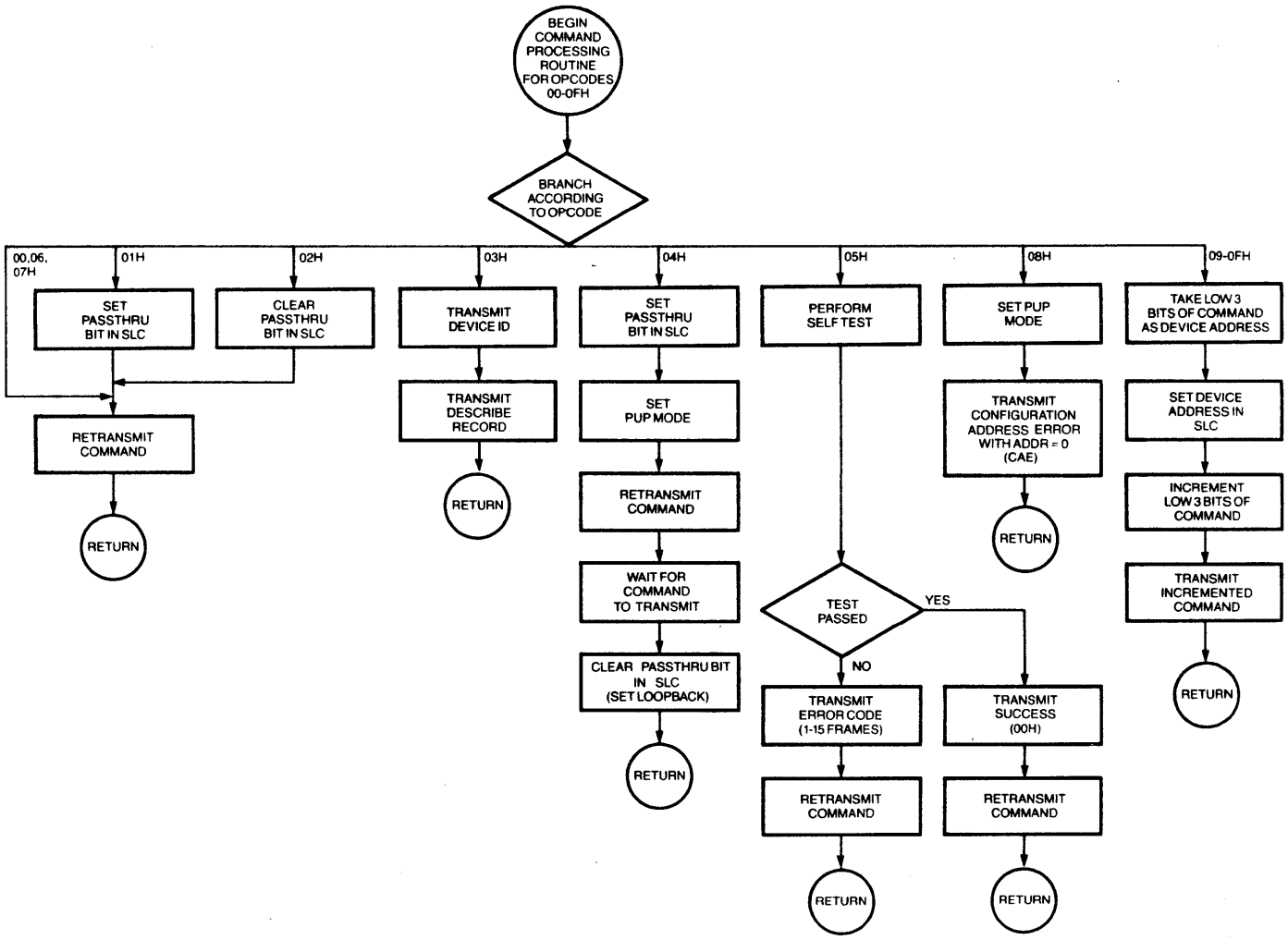


Figure 4-9. Command Processing Routine for Opcodes 00 - 0Fh

Devices receiving opcode 08h set PUP Mode and transmit CAE since this is the eighth device (only seven devices are allowed). The valid opcodes (09-0Fh) show the correct processing of the Auto Configure command.

The next range of opcodes, 10h thru 1Fh, are for the Poll command and are shown in Figure 4-10. First, the number of data frames to report is checked. If zero, then the RePoll buffer is cleared since this should reflect what was transmitted during this Poll. The Poll command is then retransmitted. Control returns to the top level.

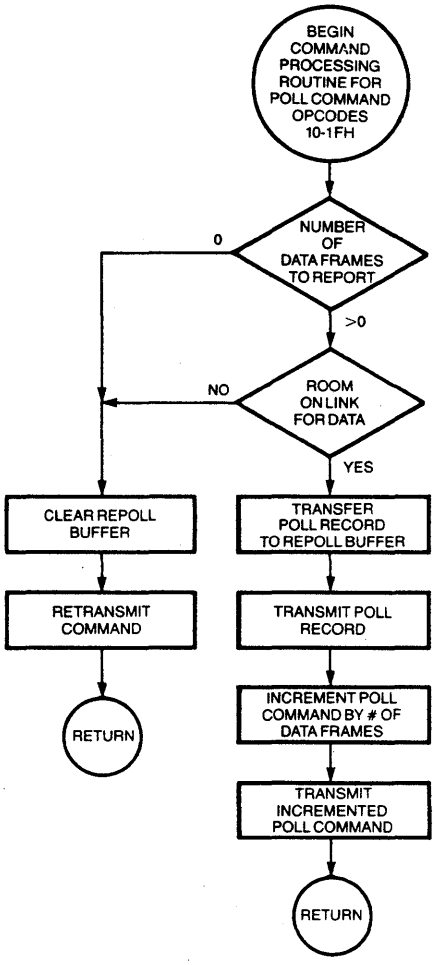


Figure 4-10. Command Processing Routine for Opcodes 10 - 1Fh

When data frames are available, and there is room on the Link for the data, then the Poll record is ready to be transmitted. To check for room on the Link, the lower four bits of the Poll command should be checked. These four bits indicate how many frames are on the Link. Thus the number of frames which can be added onto the Link will be 15 minus the lower 4 bits. The Poll record is transferred to the RePoll buffer so that it will reflect what was last reported. The Poll record is transmitted, followed by the incremented Poll command. Control returns to the top level.

The processing of the RePoll command (opcodes 20h thru 2Fh) is shown in Figure 4-11. This command is quite similar to the Poll command previously described. The RePoll buffer is checked. If clear, then no data was transmitted on the previous Poll command, and the RePoll command is retransmitted. If there is data in the RePoll buffer, and if there is room on the Link for the data, then the Poll record present in the RePoll buffer is transmitted, followed by the incremented RePoll command. If no room on the Link is available, then the RePoll command is retransmitted and the contents of the RePoll buffer unchanged. To transmit the RePoll buffer, the device must wait for another RePoll command (with sufficient room on the Link). Note that if a Poll command occurs first, the RePoll buffer will be overwritten or cleared (the current contents of the RePoll buffer would be lost).

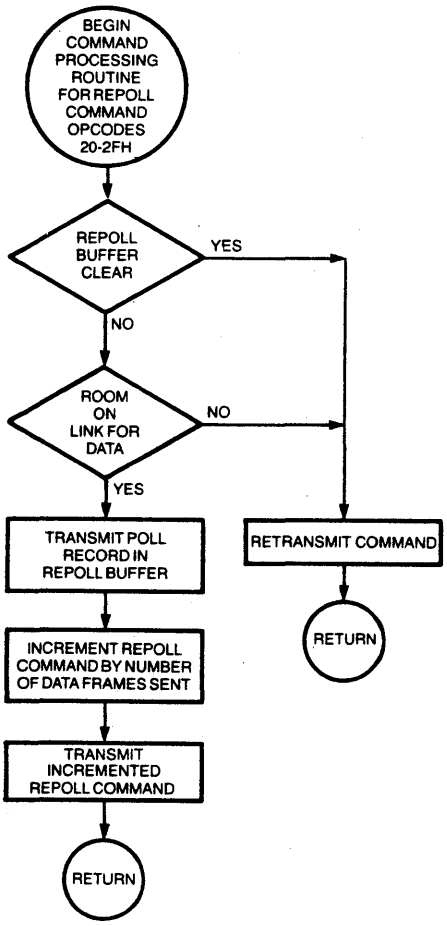


Figure 4-11. Command Processing Routine for Opcodes 20 - 2Fh

The command processing sequence for opcodes 30h thru FBh is shown in Figure 4-12. If the command is not supported by the device, it is retransmitted. If supported, the command is processed and the appropriate response transmitted. Rather than show the processing steps for all of the commands here, refer to Appendix A for the action to be taken and the response to be transmitted.

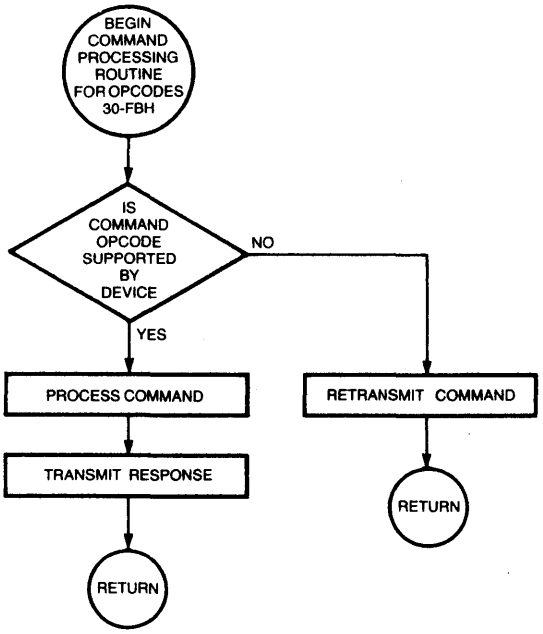


Figure 4-12. Command Processing Routine for Opcodes 30 - FBh

Commands with opcodes FCh thru FFh are handled as shown in Figure 4-13. For Transmission Error and Configuration Address Error (FCh and FDh), PUP Mode is set and the command retransmitted. For Device Hard Reset (FEh) and the prohibited opcode FFh, PUP Mode is set and a Transmission Error (TER) command is sent. (The DHR command is recognized by the SLC and should never be read by the processor.) Similarly, opcode FFh is prohibited and implies an error condition. Control is transferred back to the top level in both cases.

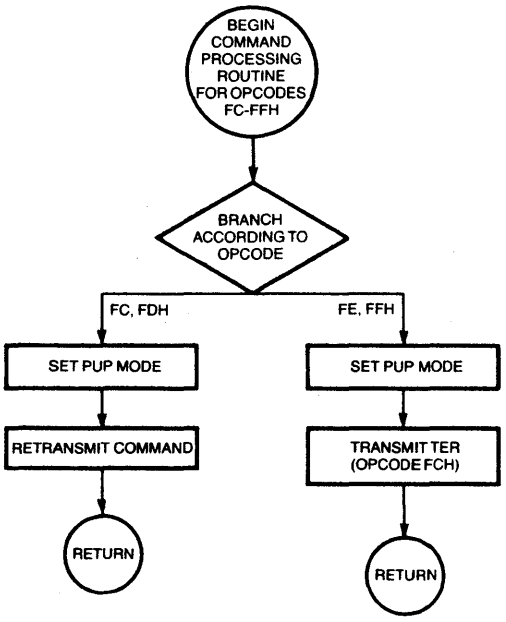


Figure 4-13. Command Processing Routine for Opcodes FC - FFh

HP-HIL COMMAND REFERENCE

APPENDIX
A

This appendix provides detailed information for each of the existing HP-HIL commands. A single page is dedicated to each command. The usage of the command is given first, followed by a brief listing of the effects the command has on the System/device. The effects give information as to what the command is used for, what effects it has on the device (i.e., setting, clearing modes, etc.), addresses the command is used with, and system interrupts generated.

The characteristics which a command has upon a device(s), and the System are also given. The characteristics fall into four categories: (1) how or what the command is used for, (2) how device modes are affected, (3) address information, and (4) interrupt information. The effects are listed here:

Used in configuration.
Used in error recovery.
Used for device identification.
Used for data input.
Used for data output.
Not supported by most devices.

Clears Power-Up Mode.
Sets Pass-Thru Mode.
Sets Loop-Back Mode.
Sets Power-Up Mode.
Sets device address.
Active in Power-Up Mode.

Use with universal address.
Use with device-specific address.

Generates interrupt in MLC.
Generates non-maskable interrupt in MLC.

Timeout information is given for each command. There are five different timeouts specified. For any command, one of the timeouts will apply. The timeouts are recommended values, while the actual time required for a command to be processed will be less. For simplification, Systems can use two timeouts (200 ms and 16 ms) to cover the cases listed here. The timeouts used are listed here:

5 milliseconds (ms)	Only one device will respond
10 ms	Multiple devices may respond
10 ms	Device may not respond
16 ms	Multiple devices may respond with data
200 ms	Device(s) must have time to complete self test.

After timeout information, the frame sequence transmitted by the System and received by the System is given. When more than one frame is shown, the top frame is the first frame to be transmitted or received. The format for the frames contents is given here in Figure A-1. Lastly, a verbal description of the operation of the command is given. Note that "Device Address" refers to a specific address for a single device (address range 1-7).

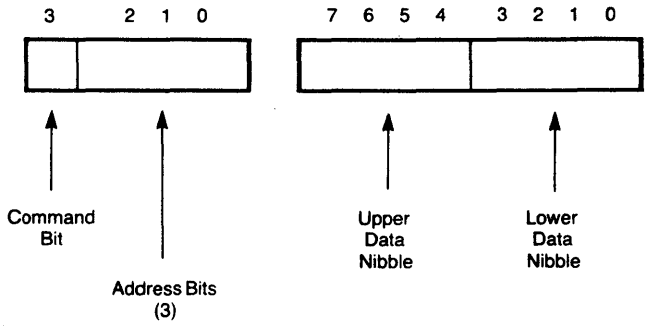


Figure A-1. Frame Format

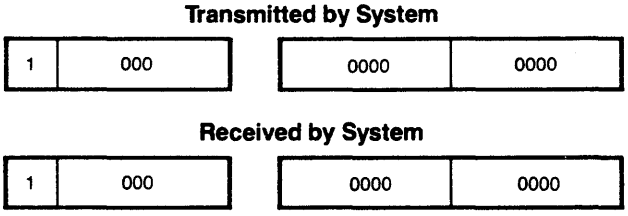
INTERFACE CLEAR (IFC) **OPCODE: 00h**

Usage: Interface Clear is used to clear error conditions on the Link and clear Power-Up Mode following power-up, Device Hard Reset, Device Soft Reset, or detection of any error condition on the Link including Configuration Address Error, Transmission Error, Data Transfer Error, or reception of the prohibited opcode FFh.

Characteristics:
Used in configuration.
Used in error recovery.
Clears Power-Up Mode.
Active in Power-Up Mode.
Use with universal address.
Generates interrupt in MLC.

Timeouts: 10 ms (Multiple devices may respond).

Frames:



Description: The primary function of the command is to clear Power-Up Mode in devices and to verify the Link integrity. Configuration information is not affected by IFC. Upon receiving the command, each device will clear Power-Up Mode, and retransmit the command as received.

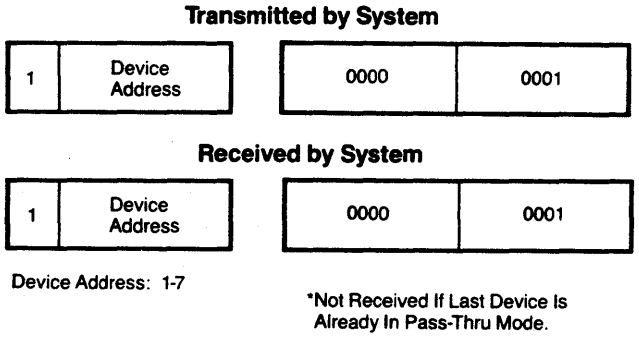
ENTER PASS-THRU MODE (EPT) OPCODE: 01h

Usage: Enter Pass-Thru Mode allows the system to sequentially open up the Link to additional devices until the last device on the Link is determined.

Characteristics:
Used in configuration.
Sets Pass-Thru Mode.
Use with device-specific Address.
Generates interrupt in MLC.

Timeouts: 5 ms (Only one device will respond).

Frames:



Description: Instructs the addressed device to set itself into Pass-Thru Mode. Once in Pass-Thru Mode, the device retransmits the command. If the device is the last device, the command will not return to the System. If another device exists downstream from the addressed device, the command will be looped back to the System by the SLC in the device.

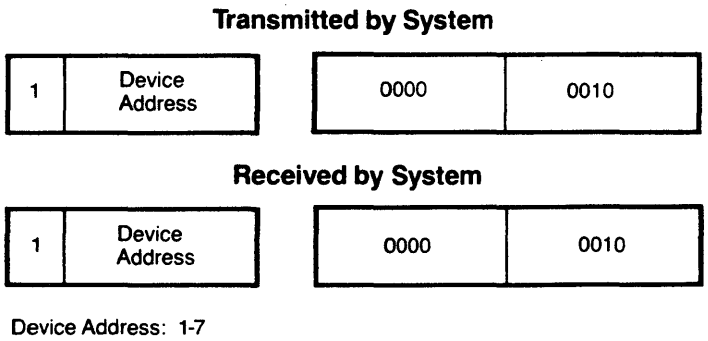
ENTER LOOPBACK MODE (ELB) OPCODE: 02h

Usage: Used during configuration to "close" the end of the Link by returning the last device on the Link to Loop-Back Mode.

Characteristics:
Used in configuration.
Sets Loop-Back Mode.
Use with device-specific address.
Generates interrupt in MLC.

Timeouts: 5 ms (only one device may respond).

Frames:



Description: The device upon reception of the ELB command, puts the SLC into Loop-Back Mode, then retransmits the command back to the System. At the end of configuration, the last device should be in Loop-Back Mode and all others in Pass-Thru Mode. Always send with a device specific address.

IDENTIFY AND DESCRIBE (IDD) OPCODE: 03h

Usage: The IDD command is used to determine the type of the attached devices, as well as some general characteristics of the device required to understand the data it reports.

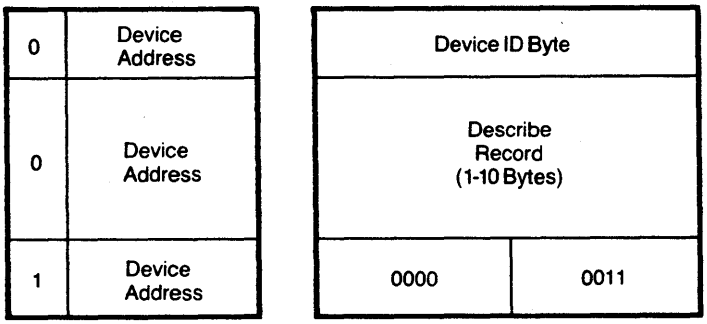
Characteristics: Used for device identification.
Use with device-specific address.
Generates interrupt in MLC.

Timeouts: 10 ms (device may respond with data).

Frames:

Transmitted by System

Received by System



Description: A device responds to the IDD command by first transmitting the device ID byte. The Device ID Byte is used to identify the general class of device and the nationality (in the case of a keyboard or keypad). After the ID byte, a series of data bytes, referred to as the Describe Record, is transmitted followed by the original command as received. This Record will vary in length from 1 to 10 data bytes. IDD should never be sent with a universal address or an MLC FIFO overflow may result. The command is usually sent immediately following the configuration process, before any polling of devices takes place.

See also Appendix C.

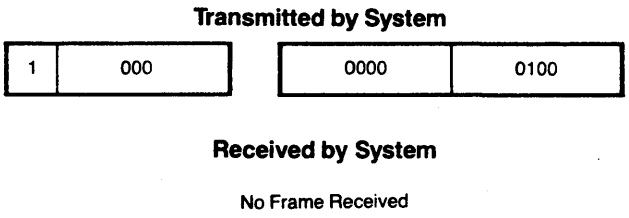
DEVICE SOFT RESET (DSR) OPCODE: 04h

Usage: Device Soft Reset serves to reset the Link configuration of all devices, without producing any data loss within the device. The command is used in error recovery where loss of any existing information within the devices is undesireable.

Characteristics:
Used in error recovery.
Sets Power-Up Mode.
Active in Power-Up Mode.
Use with universal address.

Timeouts: 10 ms (no frame returns).

Frames:



Description: When a device receives the Device Soft Reset, it places its SLC into Pass-Thru Mode, retransmits the command, then places the SLC into Loop-Back Mode and enters Power-Up Mode. The result is that all devices on the Link will receive the command, but it will not be returned to the System since the last device on the Link will enter Pass-Thru Mode and transmit the frame "off the end" of the Link. The System should delay 10 ms after sending this command before any additional transmissions to allow for propagation around the Link, at which time the Link configuration will be in its power-up state, with all devices in Loop-Back Mode, with Power-Up Mode set and all match addresses clear. However, the device microcontrollers will not be reset, and no device data will have been lost.

Device Soft Reset should be sent with a universal address, and should always be followed by an Interface Clear command, since Power-Up Mode will be set.

PERFORM SELF TEST (PST) **OPCODE: 05h**

Usage: This command causes the addressed device(s) to perform a self test.

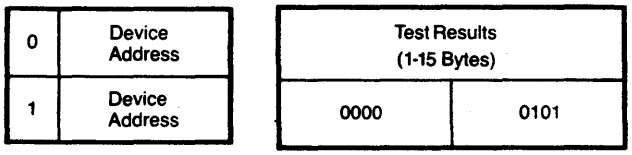
Characteristics: Used in configuration.
Use device-specific address.
Generates interrupt in MLC.

Timeouts: 200 ms (device must complete self-test).

Frames:

Transmitted by System

Received by System



– Or –
No Frame Received
(See Description)

Description: Each device is allowed up to 200 milliseconds to complete its individual self test, after which the results of the test are transmitted (1 to 15 data frames), followed by retransmission of the PST command as received. A single data frame of 00h indicates a successful test, with non-zero values representing device-specific failures. Alternatively, an HP-HIL device detecting a failure which will likely impair its ability to report the failure may elect not to respond the PST command at all. The System should wait a minimum of 200 milliseconds for a response, then assume that the device has failed the self test. Devices which fail in this way will cease to respond to HP-HIL commands until receiving a Device Hard Reset.

PST should never be sent with a universal address or a MLC FIFO overflow may result.

READ REGISTER (RRG) OPCODE: 06h

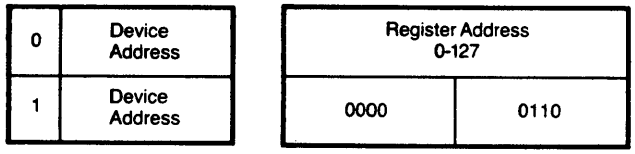
Usage: Read Register provides the System with an alternate method of collecting data from a device supporting RRG. RRG is not supported by most HP-HIL devices.

Characteristics:
Used for data input.
Not supported by most devices.
Use with device-specific address.
Generates interrupt in MLC.

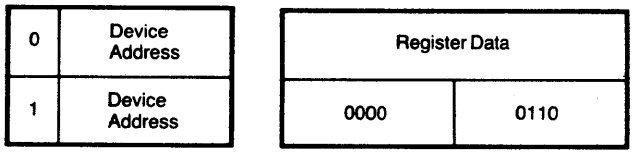
Timeouts: 10 ms (device may respond with data).

Frames:

Transmitted by System



Received by System



Description: A device indicates support of the Read Register command in the Extended Describe Record, also indicating the specific read registers contained in the device. To perform a register read, the System transmits a data frame containing the address of the register it is to read, followed by the Read Register command. The device, upon receiving the command, transmits the contents of the register as a data frame, followed by retransmission the Read Register command.

If a device receives the Read Register command after receiving anything other than 1 data frame, or if the register address is greater than 127, or if a single data frame is followed by a command other than Read Register, it returns Register I/O Error in place of the register data and command. Power-Up Mode is NOT set. No Link Link configuration information or device data is lost. Note, however, that the frame(s) producing the error are not processed in this context. It is not possible to read more than a single register at a time using this command.

Devices which do not support the Read Register command will discard all data frames and simply retransmit the Read Register command unaltered, consistent with HP-HIL conventions regarding unrecognized commands and data frames. Read Register, along with the register address, should be sent with a device-specific address.

WRITE REGISTER (WRG) OPCODE: 07h

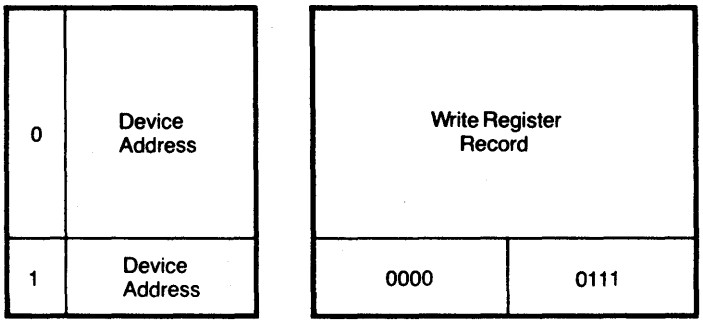
Usage: Write Register provides a means of setting the contents of individual registers in devices supporting this advanced feature, as well as providing the means for transmitting a large amount of data to a device at speeds approaching the Link maximum of 6500 bytes/second.

Characteristics:
Used for data output.
Not supported by most devices.
Use with device-specific address.
Generates interrupt in MLC.

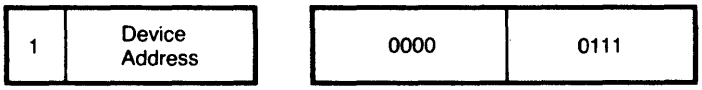
Timeouts: 5 ms (only one device will respond).

Frames:

Type 1: **Transmitted by System**



Received by System



Description: There are two forms of the Write Register Record which may be used separately or mixed in the proper order. Devices indicate support of either of these two forms (or both) in the Extended Describe Record. The two forms of the Write Register Record refer to how the address and data information is organized within the Record. For a detailed discussion of the Write Register Record, see Appendix G.

To write to individual registers in a device, the System transmits the Write Register Record followed by the WRG command. The device retransmits only the WRG command to the System.

If the device receives a register address without receiving data, or the Maximum Write Buffer Length is exceeded, or if WRG is received without preceeding data, or if another command follows the Write Register Record, or if an unsupported type of transfer is used, then the Register I/O Error is transmitted instead of the Write Register Command from the device. Power-Up Mode is not set. Device data and Link configuration information is not lost. Data frames are not processed in this context. Devices not supporting WRG

will discard all data frames and simply retransmit the WRG command unaltered.

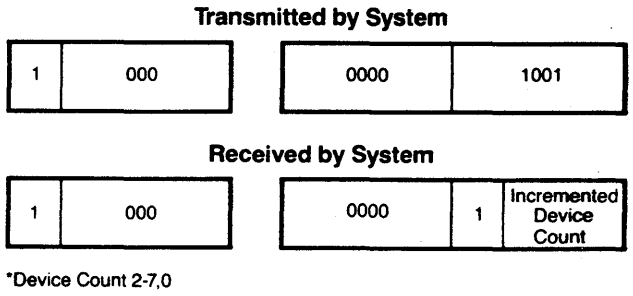
AUTO CONFIGURE (ACF) OPCODES: 08 .. 0Fh

Usage: Auto Configure is used to assign unique addresses to each device configured onto the Link, up to the maximum of seven devices. The command may also be used to determine the number of devices configured at any time.

Characteristics:
Used in configuration.
Sets device address.
Use universal address.
Generates interrupt in MLC.

Timeouts: 10 ms (multiple devices may respond).

Frames:



*Device Count 2-7,0

Description: Although Auto Configure is specified as a range of commands, the System always transmits opcode 09h as the Auto Configure command. The low three bits of the opcode become the assigned match address of the receiving device. The device increments these three bits and retransmits the command. Thus the first device, receiving opcode 09h, assumes match address 1, then retransmits the command with opcode 0Ah. The second device assumes address 2, transmitting 0Bh, and so on. Note that when a device receives opcode 0Fh, it assumes address 7 as expected but retransmits opcode 08h, consistent with the definition of only incrementing the lower three bits. A device receiving opcode 08h leaves its match address unchanged, sets Power-Up Mode, then transmits Configuration Address Error, since the Auto Configure command has already been incremented seven times from the original opcode of 09h, indicating the receiving device is the eighth on the Link, which is not permitted in the HP-HIL protocol. Auto Configure should always be sent with a universal address.

POLL (POL) **OPCODES: 10 .. 1Fh**

Usage: The Poll command is the fundamental means for extracting information from the input devices attached to the Link. It provides a structure whereby character data, position data, and a limited amount of status information may be communicated back to the system in a single, consistent format. This information, used with that acquired by the Identify and Describe command, should allow for complete processing of most types of input device data.

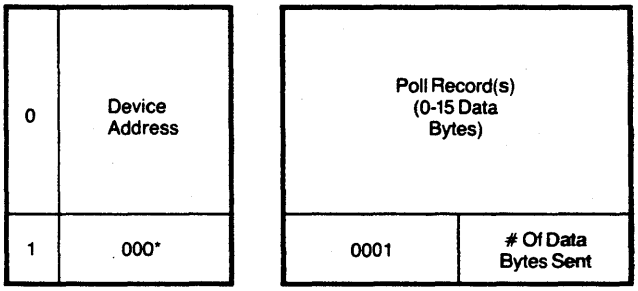
Characteristics: Used for data input.
Use universal address (or device specific address).
Generates interrupt in MLC.

Timeouts: 16 ms (multiple devices may respond).

Frames:

Transmitted by System

Received by System



* Typically Used With Universal Address (Shown)
But Can Be Used With Device Specific Address If Required.

Description: The System always transmits opcode 10h. Devices responding to the Poll will transmit their Poll Record, followed by the Poll command with the opcode incremented by the number of data frames contained in the device's Poll Record. Each device on the Link may respond respond to the Poll command similarly until a maximum of 15 bytes of data are contained in all the Poll Records associated with the Poll command. The maximum incremented opcode is 1Fh, reflecting 15 bytes of data.

Note that it may not be required for the device to report all available information in response to a single Poll request; data may be split between Polls provided correct formatting is observed for each record reported. The Poll Record is explained in detail in Appendix E.

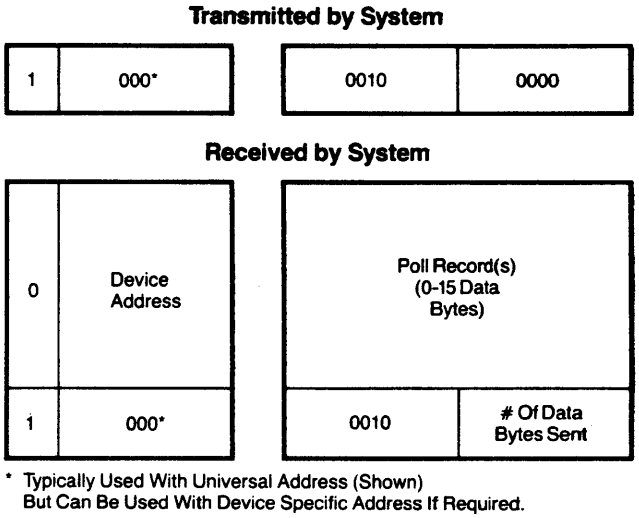
REPOLL (RPL) **OPCODES: 20 .. 2Fh**

Usage: The RePoll command provides a means for recovering any information which may have been lost in response to a Poll which sustained some error.

Characteristics: Used in error recovery.
Used for data input.
Use with universal address.
Generates interrupt in MLC.

Timeouts: 16 ms (multiple devices may respond with data).

Frames:



* Typically Used With Universal Address (Shown)
But Can Be Used With Device Specific Address If Required.

Description: Devices will respond to the RePoll command with exactly the same information reported on the last Poll. This implies that if a device reported no data in response to the last Poll command, even if new data is available the device should respond with no data to the RePoll command. The RePoll command is incremented in the same way as Poll, with the System always initiating the command with opcode 20h. RePoll is generally sent with a universal address.

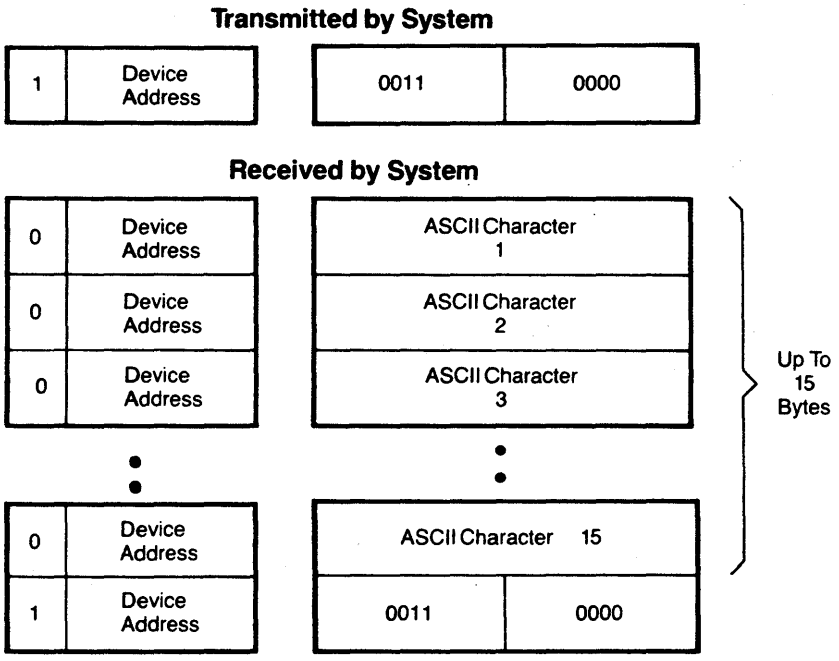
REPORT NAME (RNM) **OPCODE: 30h**

Usage: Report Name is used to request a string of characters which aid in describing the device to the user.

Characteristics: Used for device identification.
Not supported by most devices.
Use Device-Specific address.
Generates interrupt in MLC.

Timeouts: 10 ms (device may respond with data).

Frames:



Description: Characters returned are US ASCII. The command should always be sent with a device-specific address to avoid the possibility of an MLC FIFO overflow. Devices indicate support of the Report Name command in the Extended Describe Record.

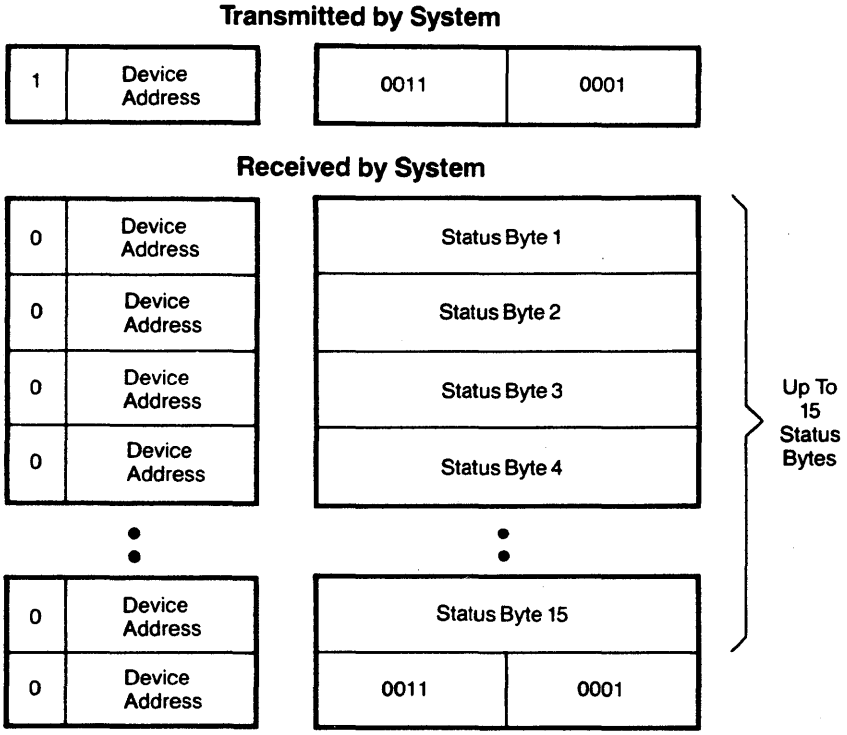
REPORT STATUS (RST) **OPCODE: 31h**

Usage: Report Status is used to extract device-specific status information from devices configured on the Link.

Characteristics: Used for data input.
Not supported by most devices.
Use device-specific address.
Generates interrupt in MLC.

Timeouts: 10 ms (device may respond with data).

Frames:



Description: Devices indicate support of the Report Status command in the Extended Describe Record. Devices supporting the command will respond with from 1 to 15 bytes of device-specific status information, followed by retransmission of the command as received. Interpretation of the status bytes will necessarily depend upon the device in question. Report Status should always be sent with a device-specific address.

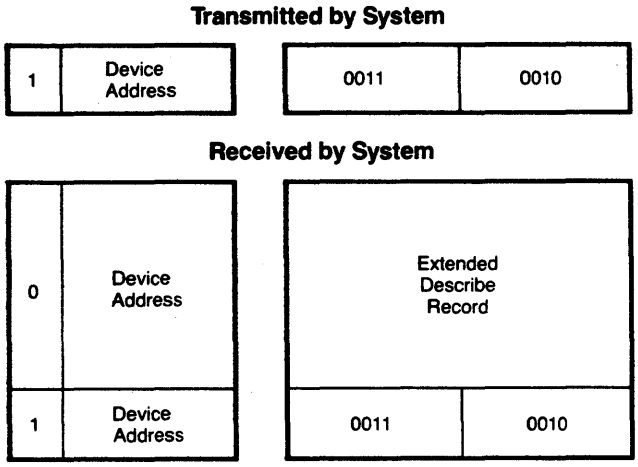
EXTENDED DESCRIBE (EXD) OPCODE: 32h

Usage: Extended Describe provides additional information concerning more advanced device features which may not be required for basic operation.

Characteristics: Used for device identification.
Not supported by most devices.
Use device-specific address.
Generates interrupt in MLC.

Timeouts: 10 ms (device may respond with data).

Frames:



Description: Support of the Extended Describe command is indicated in the Describe Record. Devices supporting the EXD command respond with a series of data bytes referred to as the Extended Describe Record, followed by retransmission of the command as received. The record length may vary from 1 to 15 bytes (although only 5 bytes are currently defined). The EXD command should always be sent with a device-specific address. Detailed information on the Extended Describe Record can be found in Appendix D.

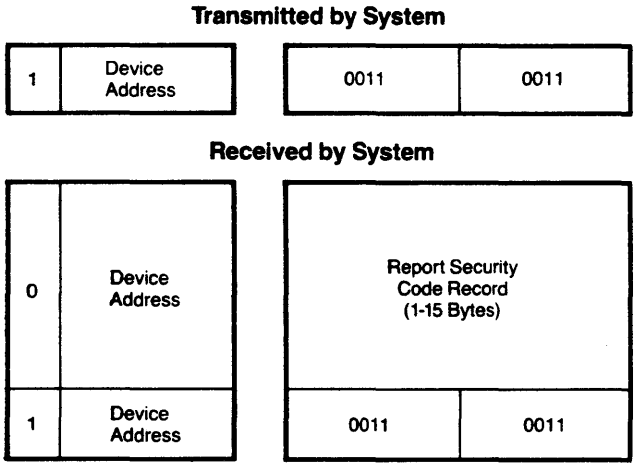
REPORT SECURITY CODE (RSC) **OPCODE: 33h**

Usage: The Report Security Code command is used to extract a unique identifier from a device.

Characteristics:
Used for data input.
Not supported by most devices.
Use device-specific address.
Generates interrupt in MLC.

Timeouts: 10 ms (device may respond with data).

Frames:



Description: Support of the command is indicated in the Describe Record. The Security Code Record consists of a Header and 1-15 bytes of data, followed by the Report Security Code command. See the Report Security Code Record description in Appendix H.

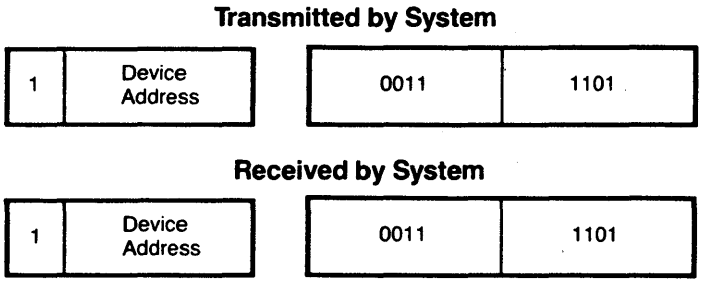
DISABLE KEYSWITCH AUTOREPEAT (DKA) OPCODE: 3Dh

Usage: This command is used to disable the "repeating keys" feature in the addressed device, reducing returned data to one report per keyswitch transition.

Characteristics: Not supported by most devices.
Use with universal or device-specific address (See below)
Generates interrupt in MLC.

Timeouts: 5 ms (only one device will respond)

Frames:



Description: Either a universal address or a device-specific address can be used. However, it is recommended to use a device-specific address so that only the desired device acts on the command. Using a universal address may cause other devices on the Link to respond to the command when this is not desired. Note that the timeout will be 10 ms (multiple devices may respond) when a universdal address is used. The device reponds by retransmitting the command as received.

The default condition of devices supporting DKA and EK1/2 AutoRepeat Commands is Keyswitch AutoRepeat Disabled. More advanced key repeat features may be implemented using device specific commands.

ENABLE KEYSWITCH AUTOREPEAT (EK1, EK2) OPCODES: 3E, 3Fh

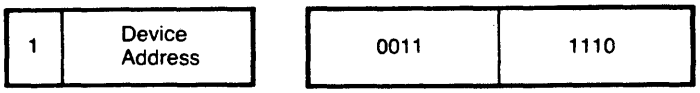
Usage: These two commands are used to enable the "repeating keys" feature in the addressed device (if the feature is supported).

Characteristics: Not supported by most devices.
Use with universal or device-specific address. (See below)
Generates interrupt in MLC.

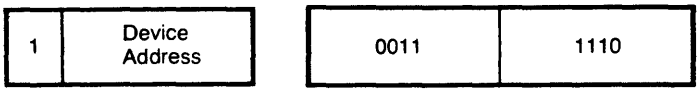
Timeouts: 5 ms (only one device will respond).

Frames:

1/30 Sec: **Transmitted by System**



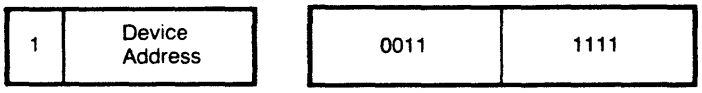
Received by System



– Or –

1/60 Sec: **Transmitted by System**

Received by System



Description: When keyswitch AutoRepeat is enabled, most keys will repeat at the rate of one report every 1/30 second. (Note that all Keyswitch AutoRepeat timing is based on the Poll rate, assumed to be 1/60 second.) Following a keyswitch down transition, a delay of 200 ms will occur and the key begins to repeat. Modifier keys (Shift, CTRL, Extend char, etc.) will not repeat, while based on the opcode of the Enable Keyswitch AutoRepeat command the Cursor Keys (cursor left, right, up, and down) will repeat at either 1/30 or 1/60 second intervals (opcodes 3Eh or 3Fh, respectively). Most keys repeat by generating repeated down transitions corresponding to the key position being repeated, although repeating cursor keys will report a keycode of 02h.

Either a universal address or a device-specific address can be used. However, it is recommended to use a device-specific address so that only the desired device acts on the command. Using a universal address may cause other devices on the Link to respond to the command when this is not desired. Note that the timeout will be 10 ms (multiple devices may respond) when a universal address is used. More advanced key repeat features may be implemented using device-specific commands.

PROMPT 1 .. PROMPT 7 (PR1 .. PR7) **OPCODES: 40 .. 46h**

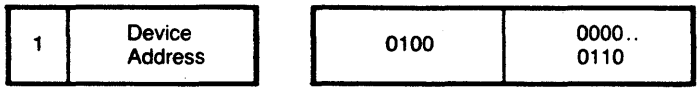
Usage: These commands are used to provide an audible or visual stimulus to the user, perhaps indicating that the System is ready for a particular type of input. Although intended to be directly associated with Acknowledge 1 .. Acknowledge 7 and Button 1 .. Button 7, this association is not a requirement.

Characteristics: Used for data output.
Not supported by most devices.
Use with universal or device-specific address. (See below)
Generates interrupt in MLC.

Timeouts: 5 ms (only one device will respond).

Frames:

Transmitted by System



Received by System

Description: Due to the possible prolonged nature of executing a Prompt command, the device, upon receiving the command, will retransmit the command, then execute the Prompt functionality. The Prompts and Acknowledges supported by indicated in the Describe Record, and all unsupported Prompts will be treated the same as other unsupported commands.

Either a universal address or a device-specific address can be used. However, it is recommended to use a device-specific address so that only the desired device acts on the command. Using a universal address may cause other devices on the Link to respond to the command when this is not desired. Note that the timeout will be 10 ms (mulitple devices may respond when a universal address is used.

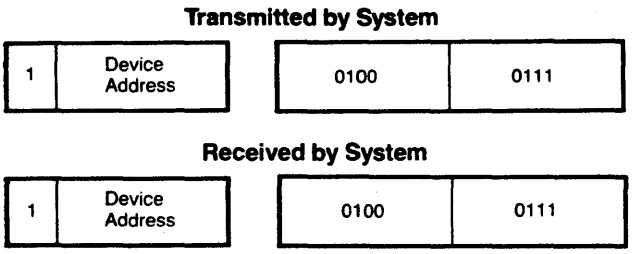
PROMPT (PRM) **OPCODE: 47h**

Usage: Intended as a general-purpose stimulus to the user, Prompt is not intended to be associated with a particular Button as are Prompt 1 .. Prompt 7.

Characteristics: Used for data output.
Not supported by most devices.
Use with universal or device-specific address. (See below)
Generates interrupt in MLC.

Timeouts: 5 ms (only one device will respond).

Frames:



Description: Due to the possible prolonged nature of executing a Prompt command, the device upon receiving the command will retransmit the command, and then execute the Prompt. A device indicates support of Prompt in the Describe Record, and responds to the command by retransmitting it as received.

Either a universal address or a device-specific address can be used. However, it is recommended to use a device-specific address so that only the desired device acts on the command. Using a universal address may cause other devices on the Link to respond to the command when this is not desired. Note that the timeout will be 10 ms (multiple devices may respond) when a universal address is used.

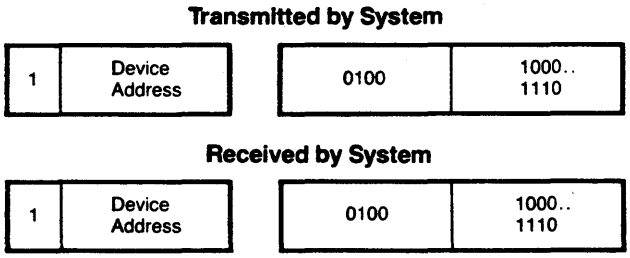
ACKNOWLEDGE 1 .. ACKNOWLEDGE 7 (AK1 .. AK7) OPCODES: 48 .. 4Eh

Usage: These commands, similar to the Prompt 1 .. Prompt 7 commands, are intended to provide an audible or visual response to the user, and are generally directly associated with the corresponding Prompt and Button of the same number, although this is not a requirement.

Characteristics: Used for data output.
Not supported by most devices.
Use with device-specific address. (See below)
Generates interrupt in MLC.

Timeouts: 5 ms (only one device will respond).

Frames:



Description: The device responds to Acknowledge 1 .. Acknowledge 7 by retransmitting the command, then executing the function. Unsupported Acknowledge commands are retransmitted with no action taken. Since there is no explicit "Prompt Off" function provided, this functionality may be part of the Acknowledge definition for a particular device, if required.

The Prompts and Acknowledges supported by the devices are indicated in the Describe Record, and all unsupported Prompts will be treared the same as other unsupported commands.

Either a universal address or a device-specific address can be used. However, it is recommended to use a device-specific address so that only the desired device acts on the command. Using a universal address may cause other devices on the Link to respond to the command when this is not desired. Note that the timeout will be 10 ms (multiple devices may respond when a universal address is used.

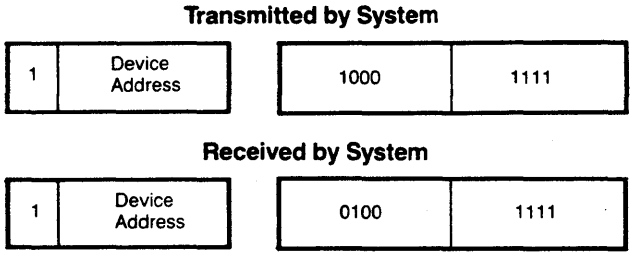
ACKNOWLEDGE (ACK) OPCODE: 4Fh

Usage: Similar to Prompt, Acknowledge is not associated with any particular Button, but merely as a general purpose audio or visual response to the user.

Characteristics: Used for data output.
Not supported by most devices.
Use with universal or device-specific address. (see below)
Generates interrupt in MLC.

Timeouts: 5 ms (only one device will respond).

Frames:



Description: The device responds to Acknowledge by retransmitting the command as received, then executing the function if supported.

Since there is no explicit "Prompt Off" function provided, this functionality may be part of the Acknowledge definition for a particular device, if required. Support of Prompt and Acknowledge is indicated in the Describe Record.

Either a universal address or a device-specific address can be used. However, it is recommended to use a device-specific address so that only the desired device acts on the command. Using a universal address may cause other devices on the Link to respond to the command when this is not desired. Note that the timeout will be 10 ms (multiple devices may respond when a universal address is used.

REGISTER I/O ERROR (RIO) OPCODE: FAh

Usage: The Register I/O Error is used to indicate to the System that an error has occurred during the data transfer associated with a Write Register or Read Register command.

Characteristics: Used for error recovery.
Not supported by most devices.
Generates interrupt in MLC.

Timeouts: N/A (This command sent by device only in response to an error condition).

Frames:

Transmitted by System

Received by System

Description: Register I/O Error is generated by the device upon receipt of a Write Register or Read Register command which does not conform to the proper format, or upon receipt of any command not supported for data transfer following reception of a data frame. Note that reception of a Transmission Error during a data transfer may result in the device returning Register I/O Error as well. It is recommended that reception of Register I/O Error by the System always be followed by transmission of Interface Clear to reset any error conditions which may be present on the Link. Refer to the Read Register and Write Register commands for more details concerning Register I/O Errors.

SYSTEM HARD RESET (SHR) OPCODE: FBh

Usage: This command is used to provide a Non-Maskable Interrupt (NMI) or Reset signal to the System processor, allowing for full system reset functionality by devices residing on HP-HIL.

Characteristics: Not supported by mosr devices.
Generates non-maskable interrupt in MLC.

Timeouts: N/A (command sent by device, can be initiated at any time).

Frames:

Transmitted by System

Received by System

Description: System Hard Reset is the only command which may be initiated by a device without any action on the part of the System. It is trapped by the MLC IC, which lowers its NMI line and sets an internal bit as described in the MLC Data Sheet. Although the device initiating the command will transmit with its own match address associated with Reset, the MLC ignores the address field in generating the NMI to the System. Note that System Hard Reset does not affect the configuration of the Link in any way.

TRANSMISSION ERROR (TER) OPCODE: FCh

Usage: Transmission Error is initiated by a device detecting a Parity or Framing Error in a received frame, or by a device receiving the Prohibited Opcode of FFh.

Characteristics:
Used for error recovery.
Sets Power-Up Mode.
Use device-specific address.
Generates interrupt in MLC.

Timeouts: N/A (command sent by device in response to error condition).

Frames:

Transmitted by System

Received by System

Description: This command is transmitted with the address of the device detecting the error. If the MLC detects a Parity or Framing Error, it places the Transmission Error frame with a universal address into the FIFO and interrupts the System processor. Note that the device generating the Transmission Error frame and any device receiving the frame with a matching address will set Power-Up Mode, and thus transmission of the Interface Clear command should be the next action by the System as part of the error recovery procedure. Devices with Power-Up Mode set previous to detection of the error or reception of the Transmission Error command will not send the Transmission Error command.

CONFIGURATION ADDRESS ERROR (CAE) OPCODE: FDh

Usage: Configuration Address Error indicates to the System that too many devices are attached in the Link at any one time (more than seven), and it is impossible to assign a unique address to all devices.

Characteristics: Used for error recovery.
Sets Power-Up Mode.
Generates interrupt in MLC.

Timeouts: N/A (command sent by device in response to error condition).

Frames:

Transmitted by System

Received by System

Description: Note that the device which generates the Configuration Address Error frame and any device receiving it with the proper match address sets Power-Up Mode. For additional information concerning the conditions for a Configuration Address Error refer to the description of the Auto Configure command.

DEVICE HARD RESET (DHR) OPCODE: FEh

Usage: This command provides a full reset to attached devices, destroying the Link configuration along with any pending device data. Device Hard Reset is used to return devices to their condition at power-up.

Characteristics:
Used in configuration.
Used for error recovery.
Sets Power-Up Mode.
Sets Loop-Back Mode.
Use with universal address.

Timeouts: 200 ms (devices must perform self-test).

Frames:

Transmitted by System

Received by System

Description: When a device receives the Device Hard Reset, the SLC lowers the NMI line to the device microprocessor, then places itself into Pass-Thru Mode and retransmits the command as received to the next device, or "off the end" of the Link. Thus all devices on the Link will receive the Device Hard Reset, and the command will not be returned to the System. The SLC, after a period of 50 microseconds, then raises the NMI line and the device microprocessor executes its power-up initialization and self-test, places the SLC into Loop-Back Mode, sets Power-Up Mode, and clears its match address and any acquired data. Since the devices perform their self-test in response to the Device Hard Reset, at least 200 milliseconds must be allowed for its completion, and no commands should be initiated by the system until this period is expired.

Since the SLC recognizes the Device Hard Reset opcode, the device microprocessor should never read this opcode in response to a SLC interrupt. If this should occur (an error condition in the device), the device should set Power-Up Mode, and if it was not previously in Power-Up Mode send a Transmission Error frame.

Note that following the Device Hard Reset command all devices will be in Loop-Back Mode, and all device microprocessors will be in their power-on state (with the possible exception of devices which failed their power-on self-test.) Device Hard Reset should always be transmitted with a universal address.

DEVICE ID BYTE

APPENDIX

B

This appendix defines the device ID bytes for all types of devices currently defined or anticipated. Nationalization for Keyboard and Keypads are given in the second table. The third table lists the ID numbers which have currently been allocated.

The Device ID Byte is used to identify the general class of device and the nationality (language) in the case of a keyboard or keypad. Since it is not possible to designate the characteristics of all future devices, the ID Byte should be used to identify only the basic type of device and the nationality (for a keyboard or keypad).

The followoing table gives device ID Byte definitions for general classes of devices (keyboards, absolute positioners, etc.). For keyboard type devices, note that the ID has a range of 1Fh. This allows for the nationalization to be embedded in the ID Byte. The table of nationalized ID definitions gives the lower five bits of the ID Byte. Thus a French keyboard with an ID range of E0 .. FFh, would report its ID Byte as FBh (E0 + 1Bh).

DEVICE ID BYTE DEFINITIONS

Device Type	ID Range (hex)	Device Description
Keyboard	E0 .. FFh	Reserved
	C0 .. DFh	ITF Keyboard
	A0 .. BFh	Integral Keyboard
Absolute Positioners	98 .. 9Fh	Reserved
	90 .. 97h	Graphics Tablets and Digitizers
	8C .. 8Fh	Touchscreen
	88 .. 8Bh	Reserved
	80 .. 87h	Reserved
Relative Positioners	70 .. 7Fh	Reserved
	6C .. 6Fh	Reserved
	68 .. 6Bh	Mouse
	60 .. 67h	Other Quadrature Devices
Character Entry	5C .. 5Fh	Barcode Reader
	50 .. 5Bh	Reserved
	40 .. 4Fh	Reserved
Other	30 .. 3Fh	Reserved
	2C .. 2Fh	Tone Generator
	20 .. 2Bh	Reserved
Keypads	00 .. 1Fh	Vectra Keyboard

KEYBOARD NATIONALIZED ID DEFINITION

Low 5 Bits of Device ID BYTE (hex)	Nationality of Keyboard/Keypad
00h	Other *
01h	Reserved
02h	Reserved
03h	Swiss/French
04h	Portugese
05h	Arabic
06h	Hebrew
07h	Canadian/English
08h	Turkish
09h	Greek
0Ah	Thai (Thailand)
0Bh	Italian
0Ch	Hangul (Korea)
0Dh	Dutch
0Eh	Swedish
0Fh	German
10h	Chinese-PRC (China)
11h	Chinese-ROC (Taiwan)
12h	Swiss/French II
13h	Spanish
14h	Swiss/German II
15h	Belgian (Flemish)
16h	Finnish
17h	United Kingdom
18h	French/Canadian
19h	Swiss/German
1Ah	Norwegian
1Bh	French
1Ch	Danish
1Dh	Katakana
1Eh	Latin American/Spanish
1Fh	United States

* See Extended Describe Record for usage.

DEVICE ID BYTES FOR EXISTING DEVICES

ID (hex)	Description	HP Product Number
0 .. 1Fh	Keyboard, Vectra	46030A
2Ch	Audio Interface Unit	45262A
30h	Function Box	46086A
34h	HP-HIL ID	46084A
5Ch	Bar-Code Reader	92916A
60h	Rotary Control Knob	46083A
61h	HP-HIL Quadrature Port	46094A
61h	Control Dials	46085A
68h	HP Mouse	46060A
8Ch	HP-HIL/Touch Bezel	35723A
93h	A-Size Digitizer	46087A
94h	B-Size Digitizer	46088A
C0 .. DFh	Keyboard, ITF	46020A, 46021A
A0 .. BFh	Keyboard, Integral	----

DESCRIBE RECORD

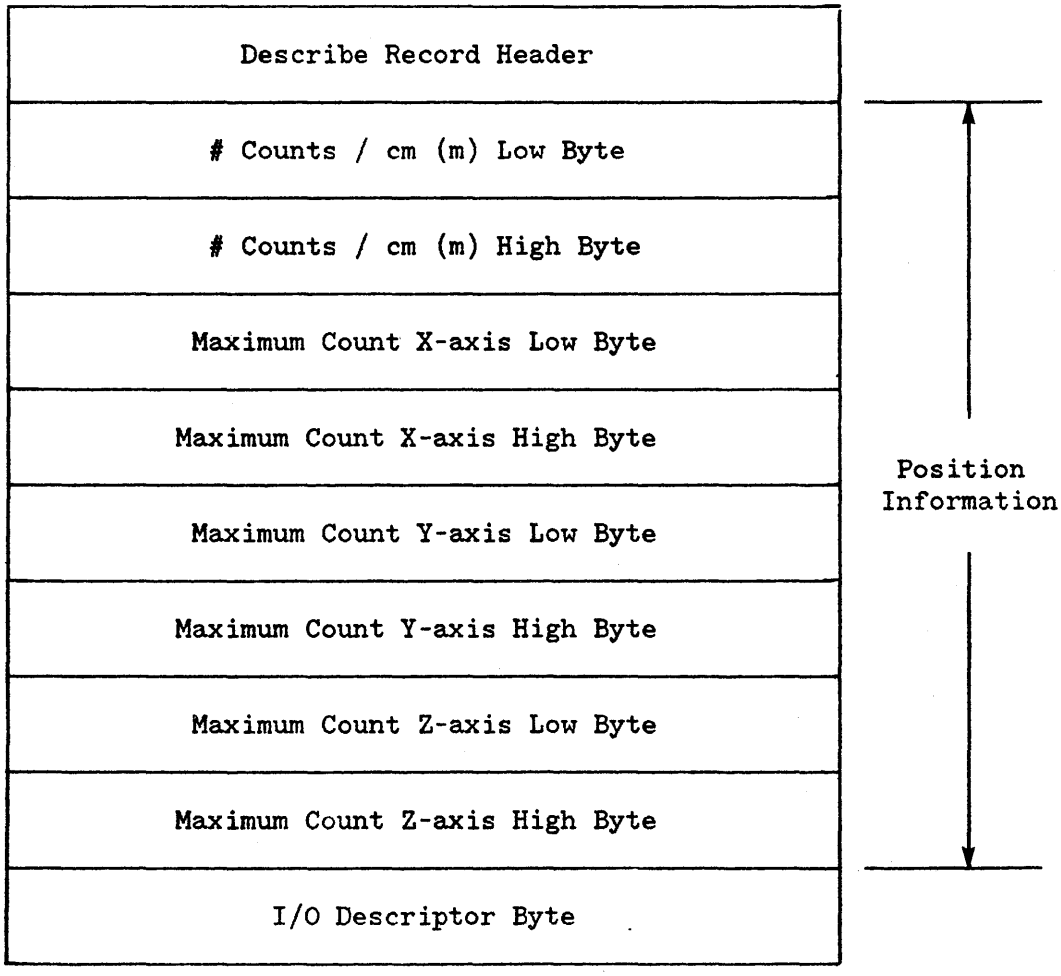
APPENDIX C

The Identify and Describe command is used to determine the type of device(s) attached to the Link and also what their characteristics are.

When a device receives the IDD command, the device will respond by returning a device ID byte followed by the Describe Record. The Record consists of 1-10 bytes of information. The first byte of the Describe Record is the Describe Record Header. If the device reports positional information, then 2 bytes will follow containing the resolution of the device. If the device is an absolute positioner, then the maximum count per axis is then reported (for each axis), 2 bytes per axis. The last byte of the Describe Record is the I/O Descriptor Byte.

The Describe Record is shown graphically below:

THE DESCRIBE RECORD



Describe Record

Every device will respond to the IDD command with at least 2 bytes of data, the Device ID Byte, and the Describe (1-10 bytes). Cursor positioning devices and devices containing buttons, proximity detection, and/or prompt/acknowledge functions will need to report additional information. The Describe Record Header contains some information about the device and provides an indicator of how much additional information is to follow the Header. The description of the Describe Record Header follows:

Bit 7 — Set if the device contains two independent sets of coordinate axes. Consider, for example, a device which interfaces two joysticks to HP-HIL, each with its own independent set of X, Y axes. It is assumed, however, that both sets of coordinate axes share common characteristics as identified in the remainder of the record. Default (clear) indicates a maximum of one set of axes. (Note that this capability may not be supported by all systems.)

Bit 6 — Set if the device is to return absolute positional data (unsigned integers). Default (clear) indicates relative data (2's complement).

Bit 5 — Set if the device returns all positional information at 16-bits/axis. Default (clear) is 8-bits/axis.

Bit 4 — Set if the I/O Descriptor Byte is to follow later in the Describe Record. Default (clear) indicates that the device has no buttons, no proximity detection, and no prompt/acknowledge functionality, with no I/O Descriptor Byte to follow.

Bit 3 — Set if the device supports the Extended Describe command. Default (clear) indicates Extended Describe command is not supported.

Bit 2 — Set if the device supports the Report Security Code command. (See Appendix H for additional information on the Report Security Code Record.) Default (clear) indicates Report Security Code is not supported.

Bit 1,0 — Bit 1 and bit 0 indicate the coordinate axes the device will report. If non-zero, then following the header will be 16 bits describing the resolution of the device, and in the case of an absolute positioner, 16 bits/axis detailing the extent of each coordinate axis.

Bit 1	Bit 0	Axes Reported
0	0	none
0	1	X
1	0	X and Y
1	1	X, Y, and Z

If the Describe Record Header indicates a non-zero number of axes for which the device will report positional information, then following the Header will be 16 bits describing the resolution of the device in counts per centimeter if the device reports data in a 16-bit format, or in counts per meter if 8-bit format. In the case of an absolute positioner, following the # Counts/cm (m) will be 16 bits per axis indicating the maximum extent of each axis for which the device reports data, assuming an origin at the lower left. This is the maximum count per axis the device is capable of reporting, based on a minimum value of 0. Note that these values are reported as 16 bits regardless of whether the device indicates 8-bit or 16-bit data reporting format.

The I/O Descriptor Byte indicates the buttons on the device will report keycodes for whether the device has proximity detection, and what Prompt/Acknowledge functions, if any, are implemented in the device. Note that Prompt and Acknowledge are treated as a set, and no device may indicate support of any particular Prompt or Acknowledge without also supporting its counterpart. If none of the above features are implemented, the I/O Descriptor byte is not transmitted. Following is the definition of the I/O Descriptor byte:

Bit 7 — Set if the device implements the general purpose Prompt and Acknowledge functions. Default (clear) implies these functions not implemented.

Bits 6,5,4 — Bits 6, 5, and 4 indicate specific Prompt/Acknowledges (Prompt 1 .. 7 and Acknowledge 1 .. 7) implemented the device. Default (clear) indicates none.

Bit 6	Bit 5	Bit 4	Prompt/Acks. Implemented
0	0	0	none
0	0	1	1
0	1	0	1 and 2
0	1	1	1, 2, and 3
1	0	0	1 .. 4
1	0	1	1 .. 5
1	1	0	1 .. 6
1	1	1	1 .. 7

Bit 3 — Set if the device will report the Proximity In/Out keycodes. Default (clear) indicates no proximity detection.

Bits 2,1,0 Bits 2, 1, and 0 indicate the buttons for which the device will report keycodes.

Bit 2	Bit 1	Bit 0	Buttons Reported
0	0	0	none
0	0	1	1
0	1	0	1 and 2
0	1	1	1, 2, and 3
1	0	0	1 .. 4
1	0	1	1 .. 5
1	1	0	1 .. 6
1	1	1	1 .. 7

EXTENDED DESCRIBE RECORD

APPENDIX D

Support of the Extended Describe command is indicated in the Describe Record Header. The Extended Describe Record provides additional information concerning more advanced features which may not be required for basic operation.

Devices supporting the Extended Describe command respond with a series of data bytes referred to as the Extended Describe Record, followed by retransmission of the command as received. The record length may vary from 1 to 15 bytes (although only 6 bytes are currently defined,) and thus should never be sent with a universal address. The Extended Describe Record has the following format:

Extended Describe Record Header	
0	Maximum Read Register Supported
0	Maximum Write Register Supported
Maximum Write Buffer Length Low Byte	
Maximum Write Buffer Length High Byte	
Localization Code	

Devices responding to the Extended Describe command return at least 1 byte of data, the Extended Describe Record Header. Devices supporting Read Register or Write Register or those returning a Localization Code will need to report additional information so that their capabilities may be more fully defined. The Extended Describe Record Header both supplies some of the parameters of the device and provides an indication of how much additional information is to follow. The meanings of the individual bits in the Header are as follows:

Bit 7 Reserved for future use. Default will be clear.

Bit 6 Set if the Localization Code is supported. If set, then following the Maximum Write Buffer Length High Byte will be one byte indicating the nationality of the device (keyboard or keypad). See Table D-1 at the end of this appendix for a listing of the Localization Codes. Default (clear) indicates that the Localization Code is not supported.

Bit 5 Set if the Report Status command is supported. Default (clear) indicates Report Status not supported.

Bit 4 Set if the Report Name command is supported. Default (clear) indicated Report Name not supported.

Bit 3 Reserved for future use. Default will be clear.

Bit 2 Set if Read Register supported. If set, immediately following the Header is a byte indicating the registers supported for reading in the device. Default will be clear, indicating Read Register not supported.

Bit 1,0 Bit 1 and bit 0 indicate support of the Write Register command. If bit 1 is set, Write Register Type 2 is supported by the device. If bit 0 is set, Write Register Type 1 is supported. If both bits are set, then the device supports both Type 1 and Type 2. If either bit 1 or bit 0 is set, then following in the Record will be information indicating the registers supported for writing in the device. If bit 1 is set, then an additional 16 bits will be returned indicating the maximum number of data bytes which may be written to the device at a time using Write Register Type 2 without data loss.

If the device indicated support for the Read Register command in the Header, then following the Header is a byte indicating the read registers supported by the device. This byte, the Maximum Read Register Supported byte, indicates the largest read register address supported. Note that it is assumed that all addresses less than this maximum are also supported. Thus a byte of 0Fh indicates that the device contains 16 read registers, addressed as read registers 0 .. 15. HP-HIL protocol allows for devices containing up to 128 read registers, addressed as 0 .. 127.

If Write Register (Type 1 or Type 2) support is indicated, then next is a byte indicating the write registers supported. The Maximum Write Register Supported byte indicates the largest write register address supported in the device. It is assumed that all addresses less than the maximum are also supported. Up to 128 write registers, addressed as 0 .. 127, are supported in the HP-HIL protocol.

If Write Register Type 2 is supported, as indicated by bit 1 of the Extended Describe Record Header being set, then following the Maximum Write Register Supported byte is 16 bits of data indicating the maximum number of bytes which may be transmitted to the device in a Type 2 transfer without overflowing the device's internal buffer. This number, transmitted first low byte, then high byte, represents the buffer length of the device - 1. Thus a device capable of buffering 1024 bytes of data would transmit a Maximum Buffer Length Low Byte of FFh and a Maximum Buffer Length High Byte of 03h.

If the Localization code is supported, then the Localization Code byte will be included in the Extended Describe Record. The Localization Code is an 8 bit number which corresponds to a nationality (language) of a keyboard or keypad. Table D-1, which follows, lists Localization Codes and languages.

Table D-1. Localization Codes

Localization Code (hex)	Nationality
00 .. 02h	Reserved
03h	Swiss/French
04h	Portugese
05h	Arabic
06h	Hebrew
07h	Canadian/English
08h	Turkish
09h	Greek
0Ah	Thai (Thailand)
0Bh	Italian
0Ch	Hangul (Korea)
0Dh	Dutch
0Eh	Swedish
0Fh	German
10h	Chinese-PRC (China)
11h	Chinese-ROC Taiwan)
12h	Swiss/French II
13h	Spanish
14h	Swiss/German II
15h	Belgian (Flemish)
16h	Finnish
17h	United Kingdom
18h	French/Canadian
19h	Swiss/German
1Ah	Norwegian
1Bh	French
1Ch	Danish
1Dh	Katakana
1Eh	Latin American/Spanish
1Fh	United States
20 .. FFh	Reserved

POLL RECORD

APPENDIX

E

The Poll command is the fundamental means for extracting data from the input devices attached to the Link. Data is sent back to the host in the form of a record, which may contain character data, position data, or some status information.

Data returned from HP-HIL devices is in record form, similar to the response to the Describe command. Each device transmits its individual Poll Record, followed by the Poll command incremented by the number of data frames in the Record, only if sufficient room remains on the Link without overflowing the MLC FIFO. Note that it may not be required for the device to report all available information in response to a single Poll request; data may be split between Polls provided correct formatting is observed for each record reported. The Poll Record is structured as follows:

Table E-1. The Poll Record

Poll Record Header
X-axis Data Low Byte
X-axis Data High Byte
Y-axis Data Low Byte
Y-axis Data High Byte
Z-axis Data Low Byte
Z-axis Data High Byte
Character Data
Character Data
. . .
Character Data
Incremented POLL COMMAND

The function of the Poll Record Header is to indicate to the System the type and quantity of information to follow, as well as to report simple status information. The bits of the Header are assigned as follows:

Bit 7 Set if the device is reporting data from the second set of coordinate axes. Default (clear) indicates data from set 1.

Bit 6,5,4 Based on the value of these 3 bits, following all position information will be character data (up to 8 bytes):

Bit 6	Bit 5	Bit 4	Character Data Description
0	0	0	No character data to follow
0	0	1	Reserved Character Set 1
0	1	0	US ASCII Characters
0	1	1	Binary Data
1	0	0	Keycode Set 1
1	0	1	Reserved Character Set 2
1	1	0	Keycode Set 2 *
1	1	1	Keycode Set 3

* These keycodes are device dependent and user definable. Use the LSB to indicate the key transition (0 = Down, 1 = Up). 128 keys maximum.

Bit 3 Set indicates request for status check. Clear (default) indicates status unchanged.

Bit 2 Set indicates device ready for data. Default (clear) indicates not ready for data transfer at this time.

Bit 1,0 Bit 1 and bit 0 indicate the coordinate axes the device is reporting:

Bit 1	Bit 0	Axes Reported
0	0	none
0	1	X
1	0	X and Y
1	1	X, Y, and Z

Following the Header is the device data. If the device indicated that it would report coordinate information 16-bits/axis in the Describe Record, then for each axis reported will be first the low, then high byte coordinate data. Otherwise, the high byte will not be transmitted. In general, the Poll Record format indicates the maximum data which can be reported; most devices will transmit only a subset each time. Following the positional information will be up to 8 bytes of character data, as specified in the Poll Record Header. The different types of character data may not be mixed. Not all keycode sets will be supported on all Systems. The Poll command is generally sent with a universal address. Note that more than one device may respond to the Poll command; each will respond with an individual Poll Record, distinguishable from the previous by the address field of the data.

HP-HIL CHARACTER SET DEFINITIONS

APPENDIX F

KEYCODE SET 1

Keycode for Transition (hex)		United States Keycap Legend	Notes
Down	Up		
00h	01h	5 +Char	1.
02h	03h		2.
04h	05h	Extend Char	Right side
06h	07h	Extend Char	Left side
08h	09h	Shift	Right side
0Ah	0Bh	Shift	Left side
0Ch	0Dh	CTRL	
0Eh	0Fh	Break Reset	
10h	11h	4	Numeric pad
12h	13h	8	Numeric pad, 4.
14h	15h	5	Numeric pad, 4.
16h	17h	9	Numeric pad, 4.
18h	19h	6	Numeric pad, 4.
1Ah	1Bh	7	Numeric pad
1Ch	1Dh	,	Numeric pad, 4.
1Eh	1Fh	Enter	Numeric pad, 4.
20h	21h	1	Numeric pad
22h	23h	/	Numeric pad, 4.
24h	25h	2	Numeric pad
26h	27h	+	Numeric pad, 4.
28h	29h	3	Numeric pad, 4.
2Ah	2Bh	*	Numeric pad, 4.
2Ch	2Dh	0	Numeric pad
2Eh	2Fh	-	Numeric pad, 4.
30h	31h	B	
32h	33h	V	
34h	35h	C	
36h	37h	X	
38h	39h	Z	
3Ah	3Bh		Left side, 3.
3Ch	3Dh		Reserved
3Eh	3Fh	ESC	DEL

NOTE

1. This key is used on the Integral PC's keyboard, but not on the ITF Keyboard (46020A).

2. Keycode 02h is reserved for Cursor Repeat. Refer to the DKA and EKA commnads.

3. Key position is not loaded. Position is covered by a non-positional filler key.

4. Not used on the Integral PC's keyboard, but is used on the ITF Keyboard (46020A).

5. Typically used in positioning devices and not found on keyboards.

Keycode for Transition (hex)		United States Keycap Legend		Notes
Down	Up			
40h	41h	6	-Char	1.
42h	43h	<blank/f10>		Numeric pad, 4.
44h	45h	3	Prev	1.
46h	47h	<blank/f11>		Numeric pad, 4.
48h	49h	.		Numeric pad, 4.
4Ah	4Bh	<blank/f9>		Numeric pad, 4.
4Ch	4Dh	Tab		Numeric pad, 4.
4Eh	4Fh	<blank/f12>		Numeric pad, 4.
50h	51h	H		
52h	53h	G		
54h	55h	F		
56h	57h	D		
58h	59h	S		
5Ah	5Bh	A		
5Ch	5Dh			Reserved
5Eh	5Fh	Caps		
60h	61h	U		
62h	63h	Y		
64h	65h	T		
66h	67h	R		
68h	69h	E		
6Ah	6Bh	W		
6Ch	6Dh	Q		
6Eh	6Fh	Tab		
70h	71h	7	&	
72h	73h	6		
74h	75h	5	%	
76h	77h	4	$	
78h	79h	3	#	
7Ah	7Bh	2	@	
7Ch	7Dh	1	!	
7Eh	7Fh	`	~	

1. This key is used on the Integral PC's keyboard, but not on the ITF Keyboard (46020A).

4. Not used on the Integral PC's keyboard, but is used on the ITF Keyboard (46020A).

Keycode for Transition (hex)		United States Keycap Legend		Notes
Down	Up			
80h	81h	<BUTTON 1>		5.
82h	83h	<BUTTON 2>		5.
84h	85h	<BUTTON 3>		5
86h	87h	<BUTTON 4>		5.
88h	89h	<BUTTON 5>		5.
8Ah	8Bh	<BUTTON 6>		5.
8Ch	8Dh	<BUTTON 7>		5.
8Eh	8Fh	<PROXIMITY IN/OUT>		5.
90h	91h	Menu		
92h	93h	f4		
94h	95h	f3		
96h	97h	f2		
98h	99h	f1		
9Ah	9Bh	8	+Line	1.
9Ch	9Dh	Stop		
9Eh	9Fh	Enter	Print	
A0h	A1h	System	User	
A2h	A3h	f5		
A4h	A5h	f6		
A6h	A7h	f7		
A8h	A9h	f8		
AAh	ABh	9	-Line	1.
ACh	ADh	Clear line		
AEh	AFh	Clear display		
B0h	B1h	8	*	
B2h	B3h	9	(	
B4h	B5h	0	)	
B6h	B7h	-	_	
B8h	B9h	=	+	
BAh	BBh	Back space		
BCh	BDh	Insert line		4.
BEh	BFh	Delete line		4.

1. This key is used on the Integral PC's keyboard, but not on the ITF Keyboard (46020A).

4. Not used on the Integral PC's keyboard, but is used on the ITF Keyboard (46020A).

5. Typically used in positioning devices and not found on keyboards.

Keycode for Transition (hex)		United States Keycap Legend	Notes
Down	Up		
C0h	C1h	I	
C2h	C3h	O	
C4h	C5h	P	
C6h	C7h	[{	
C8h	C9h	] }	
CAh	CBh	\ |	
CCh	CDh	Insert char	4.
CEh	CFh	Delete char	4.
D0h	D1h	J	
D2h	D3h	K	
D4h	D5h	L	
D6h	D7h	; :	
D8h	D9h	' "	
DAh	DBh	Return	
DCh	DDh	<home cursor>	
DEh	DFh	Prev	4.
E0h	E1h	M	
E2h	E3h	, <	
E4h	E5h	. >	
E6h	E7h	/ ?	
E8h	E9h		Reserved
EAh	EBh	Select	
ECh	EDh		Reserved
EEh	EFh	Next	4.
F0h	F1h	N	
F2h	F3h	<space bar>	
F4h	F5h	. Next	1.
F6h	F7h		Right side, 3.
F8h	F9h	<left cursor>	
FAh	FBh	<down cursor>	
FCh	FDh	<up cursor>	
FEh	FFh	<right cursor>	

1. This key is used on the Integral PC's keyboard, but not on the ITF Keyboard (46020A).

3. Key position is not loaded. Position is covered by a non-positional filler key.

4. Not used on the Integral PC's keyboard, but is used on the ITF Keyboard (46020A).

KEYCODE SET 3

Keycode for Transition (hex)		United States Keycap Legend	Notes
Down	Up		
00h	80h		Reserved
01h	81h	ESC	
02h	82h	1 !	
03h	83h	2 @	
04h	84h	3 #	
05h	85h	4 $	
06h	86h	5 %	
07h	87h	6	
08h	88h	7 &	
09h	89h	8 *	
0Ah	8Ah	9 (	
0Bh	8Bh	0)	
0Ch	8Ch	- _	
0Dh	8Dh	= +	
0Eh	8Eh	<back space>	
0Fh	8Fh	Tab	
10h	90h	Q	
11h	91h	W	
12h	92h	E	
13h	93h	R	
14h	94h	T	
15h	95h	Y	
16h	96h	U	
17h	97h	I	
18h	98h	O	
19h	99h	P	
1Ah	9Ah	[{	
1Bh	9Bh	] }	
1Ch	9Ch	Enter	
1Dh	9Dh	CTRL	
1Eh	9Eh	A	
1Fh	9Fh	S	
20h	A0h	D	

Keycode for Transition (hex)		United States Keycap Legend	Notes
Down	Up		
21h	A1h	F	
22h	A2h	G	
23h	A3h	H	
24h	A4h	J	
25h	A5h	K	
26h	A6h	K	
27h	A7h	; :	
28h	A8h	' "	
29h	A9h	` ~	
2Ah	AAh	Shift	Left side
2Bh	ABh	\ |	
2Ch	ACh	Z	
2Dh	ADh	X	
2Eh	AEh	C	
2Fh	AFh	V	
30h	B0h	B	
31h	B1h	N	
32h	B2h	M	
33h	B3h	, <	
34h	B4h	. >	
35h	B5h	/ ?	
36h	B6h	Shift	Right side
37h	B7h	* Prt Sc	
38h	B8h	Alt	
39h	B9h	<space bar>	
3Ah	BAh	Caps lock	
3Bh	BBh	F1	
3Ch	BCh	F2	
3Dh	BDh	F3	
3Eh	BEh	F4	
3Fh	BFh	F5	

Keycode for Transition (hex)		United States Keycap Legend	Notes
Down	Up		
40h	C0h	F6	
41h	C1h	F7	
42h	C2h	F8	
43h	C3h	F9	
44h	C4h	F10	
45h	C5h	Num lock	
46h	C6h	Break ScrLck	
47h	C7h	Home 7	
48h	C8h	<up cursor> 8	
49h	C9h	Pg Up 9	
4Ah	CAh	-	
4Bh	CBh	<left cursor> 4	
4Ch	CCh	5	
4Dh	CDh	<rt. cursor> 6	
4Eh	CEh	+	
4Fh	CFh	End 1	
50h	D0h	<down cursor> 2	
51h	D1h	Pg Dn 3	
52h	D2h	Ins 0	
53h	D3h	DEL .	
54h	D4h	Sysreq	
55h	D5h		Reserved
56h	D6h		Reserved
57h	D7h		Reserved
58h	D8h		Reserved
59h	D9h		Reserved
5Ah	DAh		Reserved
5Bh	DBh		Reserved
5Ch	DCh		Reserved
5Dh	DDh		Reserved
5Eh	DEh		Left side, 3.
5Fh	DFh		Right side, 3.

3. Key position is not loaded. Position is covered by a non-positional filler key.

Keycode for Transition (hex)		United States Keycap Legend	Notes
Down	Up		
60h	E0h	<up cursor>	Cursor pad
61h	E1h	<left cursor>	Cursor pad
62h	E2h	<down cursor>	Cursor pad
63h	E3h	<right cursor>	Cursor pad
64h	E4h	Home	Cursor pad
65h	E5h	Pg Up	Cursor pad
66h	E6h	End	Cursor pad
67h	E7h	Pg Dn	Cursor pad
68h	E8h	Ins	Cursor pad
69h	E9h	DEL	Cursor pad
6Ah	EAh	<unlabeled>	Cursor pad
6Bh	EBh		Reserved
6Ch	ECh		Reserved
6Dh	EDh		Reserved
6Eh	EEh		Reserved
6Fh	EFh		Reserved
70h	F0h	f1	
71h	F1h	f2	
72h	F2h	f3	
73h	F3h	f4	
74h	F4h	f5	
75h	F5h	f6	
76h	F6h	f7	
77h	F7h	f8	
78h	F8h		Reserved
79h	F9h		Reserved
7Ah	FAh		Reserved
7Bh	FBh		Reserved
7Ch	FCh		Reserved
7Dh	FDh		Reserved
7Eh	FEh		Reserved
7Fh	FFh		Reserved

US ASCII Character Codes

ASCII Char.	EQUIVALENT FORMS			
	Dec	Binary	Oct	Hex
NUL	0	00000000	000	00
SOH	1	00000001	001	01
STX	2	00000010	002	02
ETX	3	00000011	003	03
EOT	4	00000100	004	04
ENQ	5	00000101	005	05
ACK	6	00000110	006	06
BEL	7	00000111	007	07
BS	8	00001000	010	08
HT	9	00001001	011	09
LF	10	00001010	012	0A
VT	11	00001011	013	0B
FF	12	00001100	014	0C
CR	13	00001101	015	0D
SO	14	00001110	016	0E
SI	15	00001111	017	0F
DLE	16	00010000	020	10
DC1	17	00010001	021	11
DC2	18	00010010	022	12
DC3	19	00010011	023	13
DC4	20	00010100	024	14
NAK	21	00010101	025	15
SYNC	22	00010110	026	16
ETB	23	00010111	027	17
CAN	24	00011000	030	18
EM	25	00011001	031	19
SUB	26	00011010	032	1A
ESC	27	00011011	033	1B
FS	28	00011100	034	1C
GS	29	00011101	035	1D
RS	30	00011110	036	1E
US	31	00011111	037	1F

ASCII Char.	EQUIVALENT FORMS			
	Dec	Binary	Oct	Hex
space	32	00100000	040	20
!	33	00100001	041	21
"	34	00100010	042	22
#	35	00100011	043	23
$	36	00100100	044	24
%	37	00100101	045	25
&	38	00100110	046	26
'	39	00100111	047	27
(	40	00101000	050	28
)	41	00101001	051	29
*	42	00101010	052	2A
+	43	00101011	053	2B
,	44	00101100	054	2C
-	45	00101101	055	2D
.	46	00101110	056	2E
/	47	00101111	057	2F
0	48	00110000	060	30
1	49	00110001	061	31
2	50	00110010	062	32
3	51	00110011	063	33
4	52	00110100	064	34
5	53	00110101	065	35
6	54	00110110	066	36
7	55	00110111	067	37
8	56	00111000	070	38
9	57	00111001	071	39
:	58	00111010	072	3A
;	59	00111011	073	3B
<	60	00111100	074	3C
=	61	00111101	075	3D
>	62	00111110	076	3E
?	63	00111111	077	3F

US ASCII Character Codes

ASCII Char.	EQUIVALENT FORMS			
	Dec	Binary	Oct	Hex
@	64	01000000	100	40
A	65	01000001	101	41
B	66	01000010	102	42
C	67	01000011	103	43
D	68	01000100	104	44
E	69	01000101	105	45
F	70	01000110	106	46
G	71	01000111	107	47
H	72	01001000	110	48
I	73	01001001	111	49
J	74	01001010	112	4A
K	75	01001011	113	4B
L	76	01001100	114	4C
M	77	01001101	115	4D
N	78	01001110	116	4E
O	79	01001111	117	4F
P	80	01010000	120	50
Q	81	01010001	121	51
R	82	01010010	122	52
S	83	01010011	123	53
T	84	01010100	124	54
U	85	01010101	125	55
V	86	01010110	126	56
W	87	01010111	127	57
X	88	01011000	130	58
Y	89	01011001	131	59
Z	90	01011010	132	5A
[	91	01011011	133	5B
\	92	01011100	134	5C
]	93	01011101	135	5D
^	94	01011110	136	5E
_	95	01011111	137	5F

ASCII Char.	EQUIVALENT FORMS			
	Dec	Binary	Oct	Hex
`	96	01100000	140	60
a	97	01100001	141	61
b	98	01100010	142	62
c	99	01100011	143	63
d	100	01100100	144	64
e	101	01100101	145	65
f	102	01100110	146	66
g	103	01100111	147	67
h	104	01101000	150	68
i	105	01101001	151	69
j	106	01101010	152	6A
k	107	01101011	153	6B
l	108	01101100	154	6C
m	109	01101101	155	6D
n	110	01101110	156	6E
o	111	01101111	157	6F
p	112	01110000	160	70
q	113	01110001	161	71
r	114	01110010	162	72
s	115	01110011	163	73
t	116	01110100	164	74
u	117	01110101	165	75
v	118	01110110	166	76
w	119	01110111	167	77
x	120	01111000	170	78
y	121	01111001	171	79
z	122	01111010	172	7A
{	123	01111011	173	7B
|	124	01111100	174	7C
}	125	01111101	175	7D
~	126	01111110	176	7E
DEL	127	01111111	177	7F

WRITE REGISTER RECORD

APPENDIX G

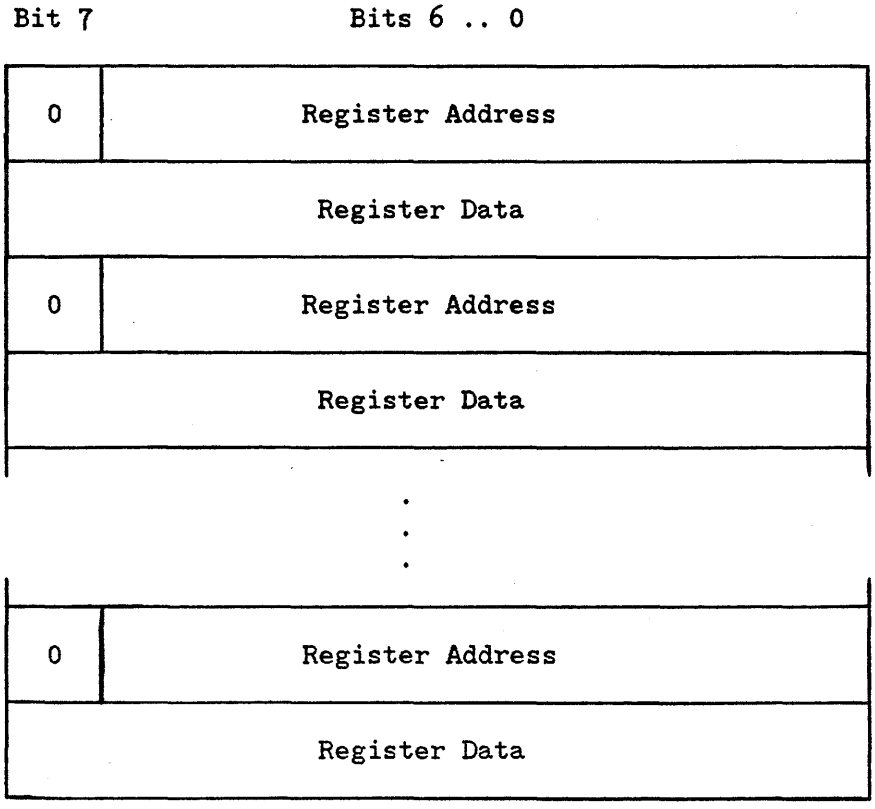
Write Register (WRG) provides a means of setting the contents of individual registers in devices supporting this feature. This features also allows for transfer of large amounts of data to a device approaching a maximum of 6500 bytes/second.

There are two forms of the Write Register Record which may be used separately or mixed in the proper order to provide the maximum degree of flexibility. Devices indicate support of either of these two forms (or both) in the Extended Describe Record.

Write Register Type 1

To write to individual registers in a device, the System transmits the register address, followed by the intended contents of that register. This is called Write Register Type 1. Several register address/register data pairs may be transmitted in sequence, with the Write Register command following all data as shown below. The Register Address/Register Data pairs comprise the Write Register Record for Write Register Type 1.

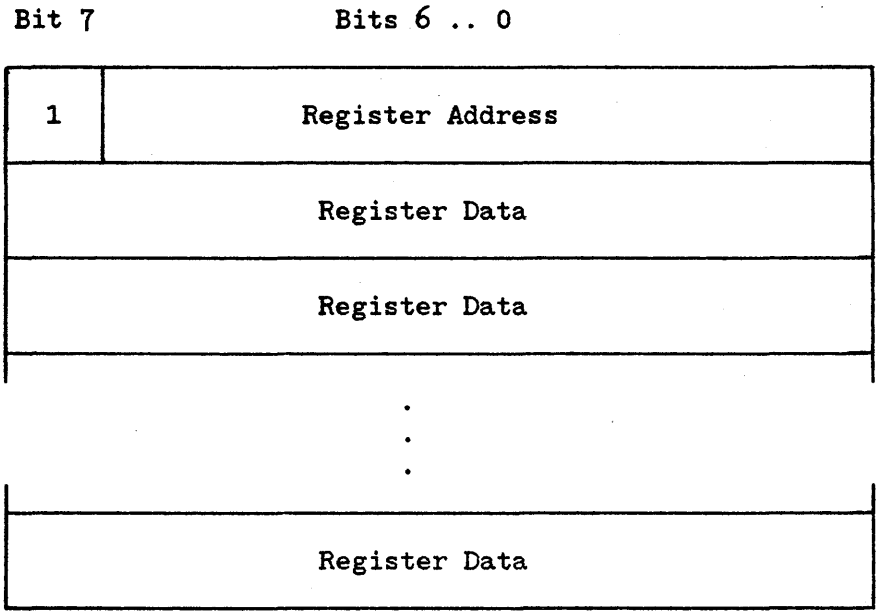
WRITE REGISTER RECORD, TYPE 1



Write Register Type 2

The System may also wish to write several bytes to a single register in sequence, utilizing Write Register Record Type 2. Type 2 transfers are indicated to the device by setting the most significant bit in the byte containing the register address, followed by as many data frames as desired (up to the Maximum Write Buffer Length of the device, reported in the Extended Describe Record), followed by the Write Register command. Although it is also be possible to write several bytes to the same register using Type 1 transfers in devices supporting both types (repeating the register address before each byte of data), the intention of the two types of data transfer is quite different, and use of Type 2 is recommended. The Write Register Record Type 2 has the following format:

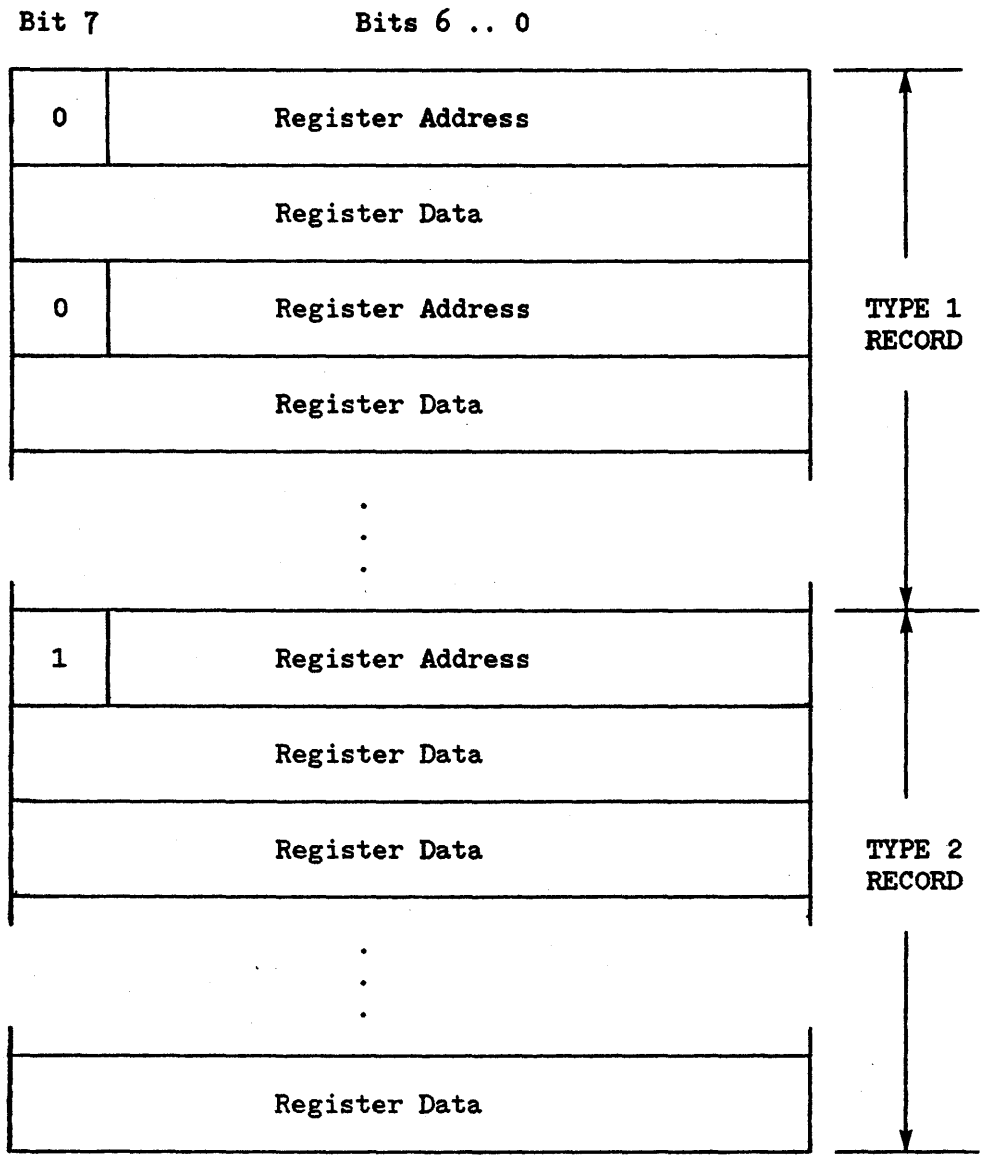
WRITE REGISTER RECORD, TYPE 2



Combining Type 1 and Type 2

The two Record formats may also be mixed for devices supporting both Write Register Type 1 and Type 2. However, with the restriction that writes to individual registers occur first in the Record. Once the device detects the most significant bit in the register address byte to bet set, it assumes all following data frames to be data for that register.

WRITE REGISTER RECORD, TYPE 1 AND 2



REPORT SECURITY CODE RECORD

APPENDIX H

The Report Security Code command is used to retrieve a unique identifier from a device.

When a device responds to the RSC command, the device transmits the Report Security Code Record followed by the RSC command. The Report Security Code Record consists of a header (1byte), followed by 1 to 14 bytes of data. The organization of the data in the record is defined in the header. Currently, there is only one data format defined for the Report Security Code Record. This format is designated as Type 1. A graphical representation of the Report Security Code Record is shown in Figure H-1.

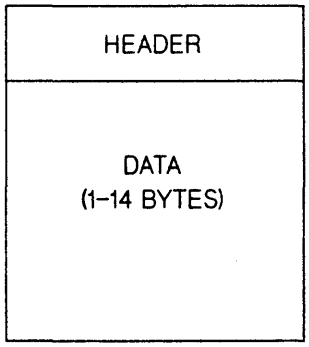


Figure H-1. Report Security Code Record

The header byte defines the format of the data following the header. The number of bytes to follow the header is part of the data format definition. Bits 7 .. 4 specify the data format type. Currently, only one data format type is defined, Type 1. Bits 3 .. 0 are reserved, and should be set to zero. Thus, the only valid header is for Type 1 and it would be 10h.

Data Format Type 1

Data Format Type 1 defines eight bytes of data which follow the header. The eight bytes are the packed product and serial number of the HP-HIL device.

The HP ID Module may have two different part number formats. The ID Module will have the normal five digit product number with a single letter suffix, or it will have a 10 digit part number. The 10 digit part number is given to the module when it becomes an exchange module (for field service requirements). In the case where the ID Module is an exchange module (with the ten digit part number) the five digit prefix is used and the product number letter is replaced by the least significant digit of the part number.

The product number, exchange module number, and serial number formats are:

```
Header                  : H           (1 byte header)
Product number          : DDDDDA      (5 digits and 1 ASCII char.)
Exchange module number  : DDDDDd      (5 digits and 1 ASCII char.)
Serial number           : YYWW@NNNNN  (9 digits and 1 ASCII char.)
```

where:

H	is the data header
DDDDD	is the product number (e.g. 46084)
A	is the product number alpha character (suffix)
d	is the least significant numeric character of the exchange module number
YY	is the year code (year minus 60)
WW	is the week code (0 to 51)
@	is the letter designation of the country manufacturing the device
NNNNN	is the serial suffix (0 to 99999)

The five digits of the product or exchange part number prefix are converted to a two byte binary number and the high order bit of a third byte. The remaining lower seven bits of the third byte contain the ASCII character. In products where two alpha characters are used in the product number, only the first character is used in the format data. The order of the bytes have been arranged to transmit the least significant byte of the number first.

In a similar manner, the nine digits of the serial number are converted to a four byte binary number. The country of manufacture letter designation is in the last byte to be transmitted and is an ASCII character.

The bytes are transmitted in the following order, starting with byte 1 through 9. Bits are numbered starting with 0 at the right most position of the byte to bit 7, left most position.

The Report Security Code Record format for Type 1 is:

Byte	Bits	Description
1	7..0	The first byte is the header containing the number 10h.
2	7..0	The second and third bytes and bit 7 of the fourth byte represent the 5 digits of the product or exchange part number DDDDD in binary form. The least significant bit is bit 0 of byte two.
3	7..0	
4	7	

4	6..0	The least significant seven bits of byte four represent the product letter or the least significant digit of the exchange module part number (a numeric character). The character is the US ASCII 7 bit representation of the character.
5 6 7 8	7..0 7..0 7..0 5..0	The fifth, sixth, seventh, and six least significant bits of byte eight represent the 9 digits of the seial number YYWWNNNNN in binary form, without the alpha character. The least significant bit is bit 0 of byte 5.
8	7..6	The two most significant bits of byte eight are reserved for future use and should be set to 0.
9	6..0	The least significant seven bits of byte nine represent the serial number letter. The character is the US ASCII 7 bit representation of the character.
9	7	The most significant bit of byte nine is reserved for futere use and is set to zero.

A graphical representation of the Type 1 Report Security Code Record is shown in Figure H-2.

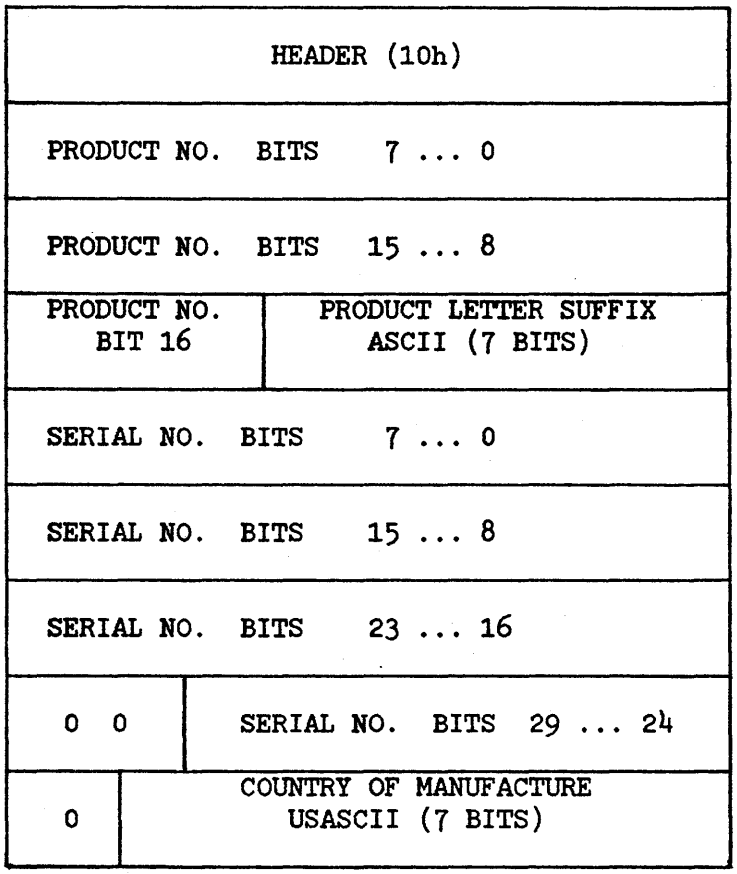


Figure H-2. Report Security Code Record, Type 1

An example of the information returned upon receiving a RSC command for a product (vs. exchange) module is given here. This example is for a device having a product number of 46084A and a serial number of 2519A00001. The serial number corresponds with year of 85, week of 19, country of manufacture letter A, and serial suffix of 00001. The ID module is located at device address 1.

System:		Transmits	933h	RSC command, opcode 33h, addr 1
ID Module:	1	Returns	110h	Header, command bit clear, addr 1
Byte	2		104h	Part of product number 46084
	3		1B4h	Part of product number 46084
	4		141h	Product letter "A" and 46084
	5		161h	Part of serial number
	6		1B0h	Part of serial number
	7		103h	Part of serial number
	8		10Fh	Part of serial number
	9		141h	Country of Manufacture Letter

10	933h	RSC command, opcode 33h, addr 1

Notes: 46084 decimal = 0B404h

251900001 decimal = 0F03B061h

US ASCII "A" = 41h

HP-HIL MASTER LINK CONTROLLER

APPENDIX

I

DESCRIPTION

The Master Link Controller (MLC) is the communication controller that interfaces the Host to the HP-HIL input devices. The MLC can accept commands from the System processor and transmit the messages through HP-HIL with the proper format. It can also poll the input devices, collect data entered by the user, and relay it to the Host.

The HP-HIL ICs are used in HP products and are described here for reference only.

BLOCK DIAGRAM

A summary of the major blocks in the MLC are described here. Figure I-1 shows the block diagram of the MLC.

ISTATE: The Input State Machine, a PLA, reads the incoming data. ISTATE shifts each good bit of the incoming frame into ISHIFT, and executes an error-handling routine in case of a parity or framing error. ISTATE controls polling the Link and interrupting the processor with returned data.

ISHIFT: The Input Shifter converts the serial input from the Link to parallel data. It checks the parity of the frame and looks for a device hard reset command or an address match.

PINTERF: The Universal Processor Interface executes read/write commands from an Intel processor. The processor can write into the registers W0-W3 (data and control) or read from the top of the FIFO using the bi-directional pins D0-D7. The PINTERF tells the ISTATE if the top of the FIFO is a universal poll command.

OSHIFT: The Output Shifter multiplexes between processor data and an internally generated poll command. The out-going word is converted to frame format by generating the parity bit and shifting the data serially to the SDI block.

SDI: The Serial Data Interface routes the serial data SI (from the Link) and DO (from the PINTERF). Normally SI is sent to the processor and DO is sent to the Link through SO. In test mode, SI is ignored and DO is looped back to the processor by treating it like a Link input.

OSTATE: The Output State Machine, a PLA, controls multiplexing, loading, and shifting for OSHIFT. It also clears R1 (Output Busy) after the frame has been transmitted.

FIFO: The FIFO stores up to 16 frames from the Link. The ISTATE continuously pushes them to the top where the processor can pop them.

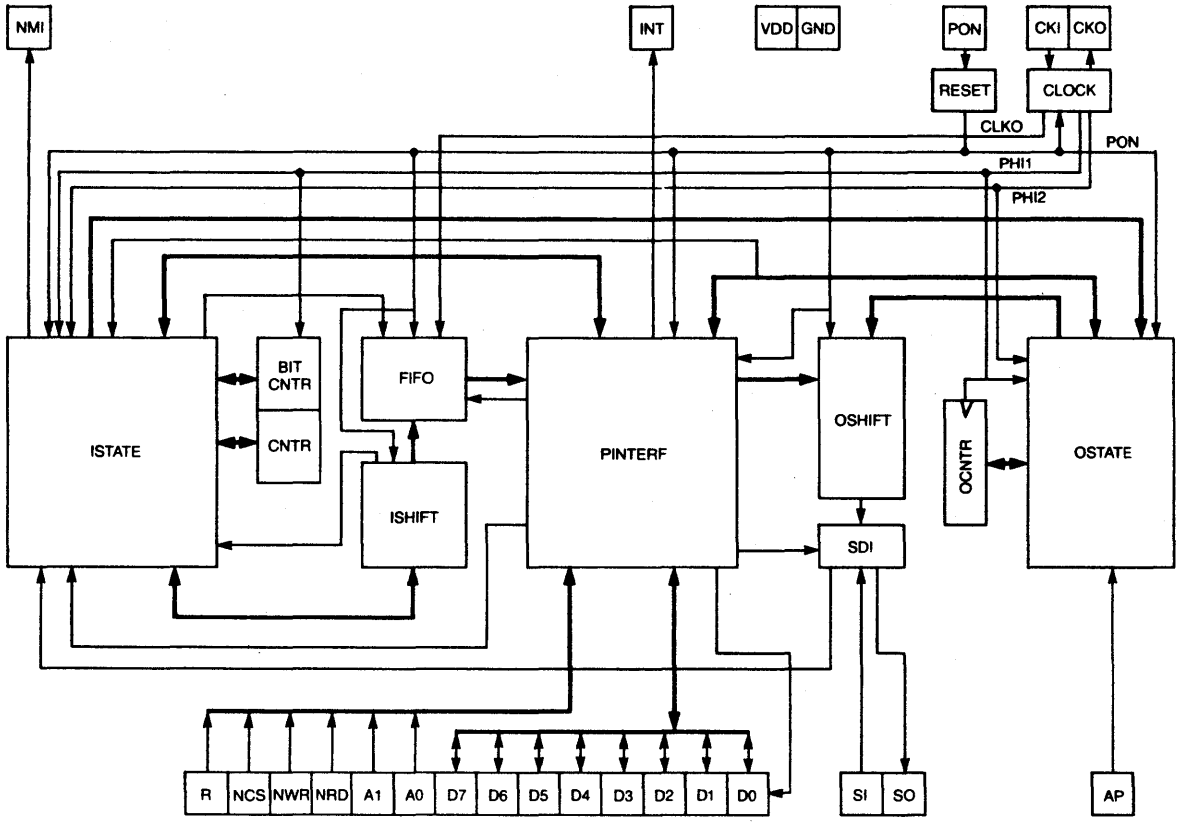


Figure I-1. MLC Block Diagram

Pinouts

The pinouts for the MLC are shown in Figure I-2.

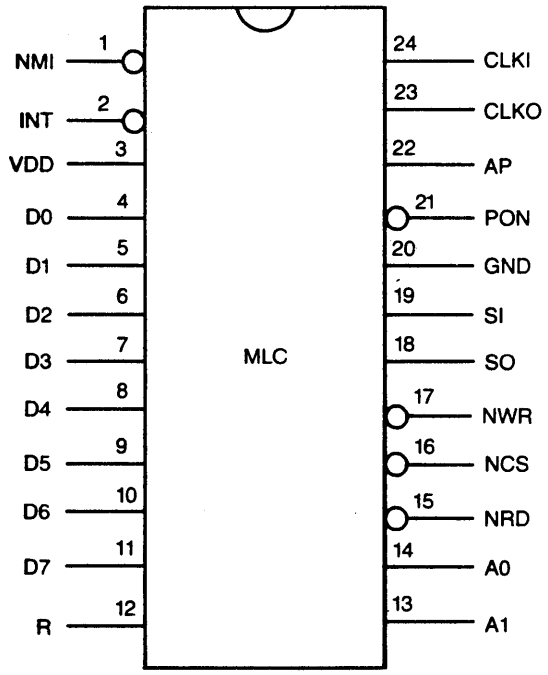


Figure I-2. MLC Pinouts

Pin Description

Pin#	Name	Description	I/O Type
1	NMI	Non-Maskable Interrupt, open collector	Output
2	INT	Interrupt, open collector	Output
3	VDD	Power source, +5V	Power
4	D0	Data bit 0 of reg's W0-3 (writes) or R0-3 (reads)	I/O
5	D1	" " 1	I/O
6	D2	" " 2	I/O
7	D3	" " 3	I/O
8	D4	" " 4	I/O
9	D5	" " 5	I/O
10	D6	" " 6	I/O
11	D7	" " 7	I/O
12	R	Reserved for future use. MUST be grounded	Input
13	A1	Address bit 1 of reg's W0-3 (writes) or R0-3 (reads)	Input
14	A0	Address bit 0 of reg's W0-3 (writes) or R0-3 (reads)	Input
15	NRD	Not Read from R0-3	Input
16	NCS	Not Chip Select, reads/writes	Input

17	NWR	Not Write to reg's W0-2	Input
18	SO	Serial Output, HP-HIL	Output
19	SI	Serial Input, HP-HIL	Input
20	GND	Ground +0V	Power
21	PON	Power-On reset, active low	Input
22	AP	Auto Poll, rising edge	Input
23	CLKO	Clock Out, resonator hook-up only	Output
24	CLKI	Clock In, resonator or TTL clock	Input

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENT

Absolute maximum ratings are limits beyond which permanent device failure may occur. These are stress ratings only; the device should not be expected to operate under these conditions (except for maximum operating ambient temperature.)

Operating Ambient Temp	0 to 70 degrees C
Package Thermal Res. (Plastic)	140 degrees C/watt max
Substrate Bias Voltage (VBB) wrt GND	-2 V to -4 V
Max Vdd Supply Voltage wrt GND	7 V
Voltage Between Any Pin And GND	-1 V to 7 V
Voltage Between Any Pin And VDD	-7 V to 1 V
Power Dissipation At VDD=5.5 V, temp=0 Deg. C.	0.22 Watts

PACKAGE DESCRIPTION

The MLC is packaged in a 24-pin DIP with rows spaced 15.2 mm (0.6 inches) apart.

Conditions:

24-lead plastic package
18700 mills-square die,
No air flow

Thermal Resistance:

100 Degrees C/W

Tj max = 100 C

Ta max = 70 C

DC SPECIFICATIONS

Signal	Condition	Min	Typ*	Max	Units
Operating Voltage VDD		4.75	5.0	5.25	V
Operating Supply Current	Temp=0 C VDD=5.25 V			55	mA
INPUT VOLTAGE LEVELS					
Crystal Input (if driven by TTL)					
logic high (VIH)			1.75		V
logic low (VIL)			1.0		V
Gain:					
measured at CKO	CKI=2.0 V		0.5		V/V
TTL Input					
logic high (VIH)	VDD=max	2.0			V
logic low (VIL)	VDD=min			0.8	V
HP-HIL Input (Schmitt Trigger)					
logic high (VIH)	VDD=max	3.0			V
logic low (VIL)	VDD=min			0.8	V
hysteresis			1.1		V
Input Leakage Current	VDD=5.5 V		-10		uA
OUTPUT VOLTAGE LEVELS					
HP-HIL Output	VDD=4.5 V				
logic high (VOH)	IOH=0 mA	3.3			V
logic low (VOL)	IOL=0 mA			0.4	V
TTL Output	VDD=4.5 V				
logic high (VOH)	IOH=-0.4 mA	2.4			V
logic low (VOL)	IOL=1.6 mA			0.4	V
Open Collector Output	VDD=4.5 V				
logic low (VOL)	IOL=2.5 mA			0.4	V

*Typical values are for reference only. They are not tested.

AC SPECIFICATIONS

External Capacitance

Maximum capacitive load for SO = 600 pF.

Maximum capacitive load = 60 pF for all other outputs.
This is equivalent to two TTL packs.

Internal Capacitance

Maximum capacitance seen at input = 10 pF.

AC Timing

There are two sections in MLC, the clock oscillator and the processor interface, that were designed to operate under stricter timing requirements than are currently being used. Certain sections of this timing are no longer being supported. Their description is included here for possible future uses, but they are not guaranteed by production testing at this time.

Timing waveforms are exhibited in Figures I-3 thru I-5.

TTL Input Clock Timing

CKI Freq 8 MHz +/- 0.5%
Duty cycle of 50% high, 50% low, nominal

PON Reset Timing

	TYP	DEFINITION
TP1	5000 ns	Width of low period, PON reset
TP2	0 ns	Delay before first Chip Select
TPNMI1	50 ns	Delay before fall of NMI after fall of PON.
TPNMI2	50 ns	Delay before rise of NMI after rise of PON.

Processor Interface Timing Requirements

Specifications are in nanoseconds.

	MIN	MAX	DEFINITION
TLLAX	0		Address valid before fall of NRD or NWR
TRLRH	180		NRD low period
TWLWH	100		NWR low period
TC	60		Data valid before rise of NWR
TWHDX	25		Data hold after rise of NWR
TRHAV	0	65	Data hold after rise of NRD
TA		200	Delay before valid data after fall of NRD
TB	0		Addr hold after rise of NRD or NWR
TCS	0		NCS hold after rise of NRD in read cycle, or NWR in write cycle for Intel mode, or NRD for Motorola mode.
Tdelay	180		Delay between successive read or write operations (not guaranteed). (Delay from rise of NWR to next fall or NWR, and delay from rise of NRD to next fall of NRD.)

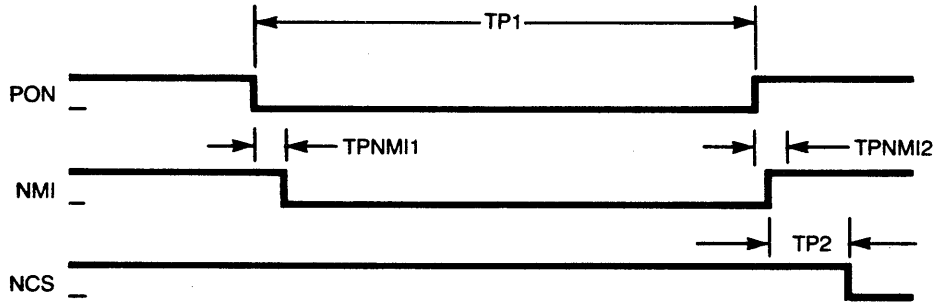


Figure I-3. PON Reset Timing

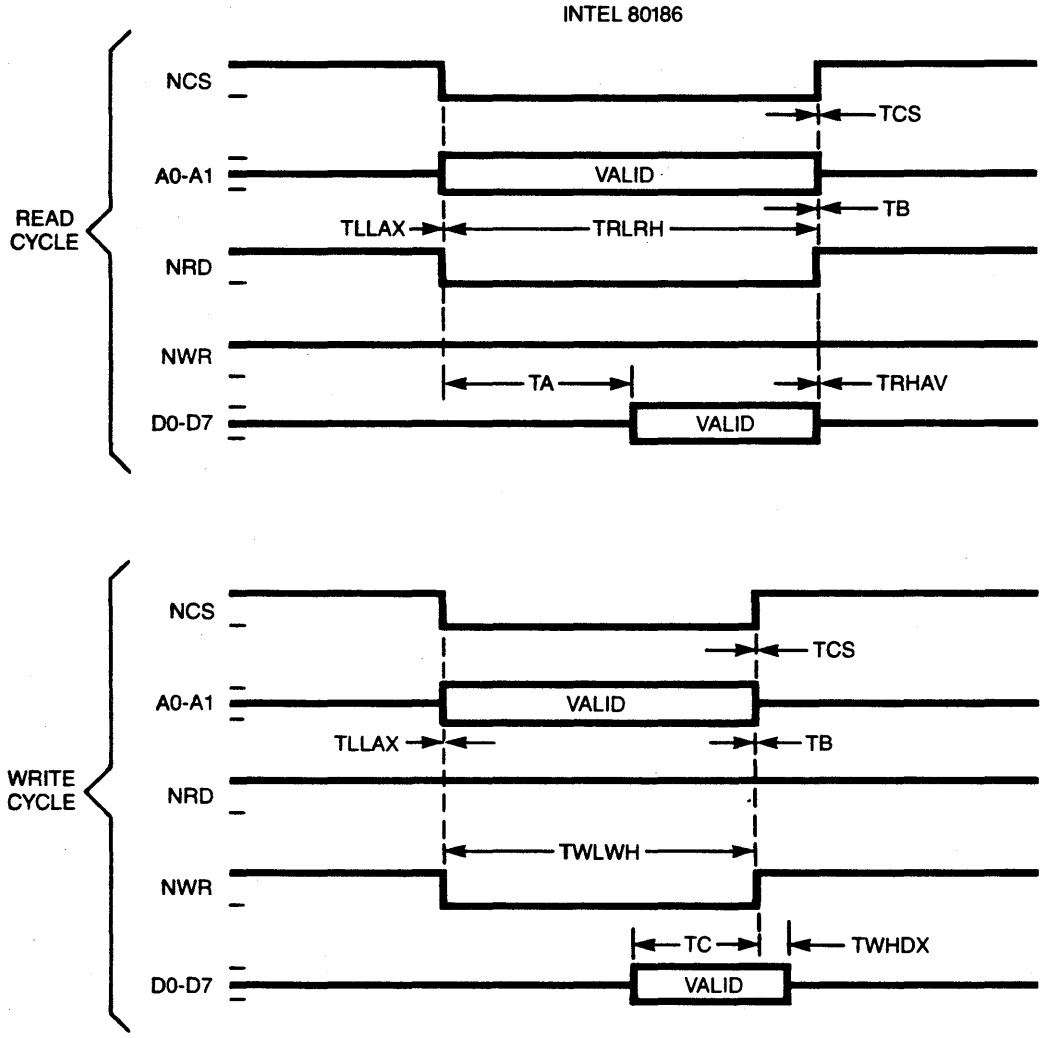


Figure I-4. Processor Interface Timing

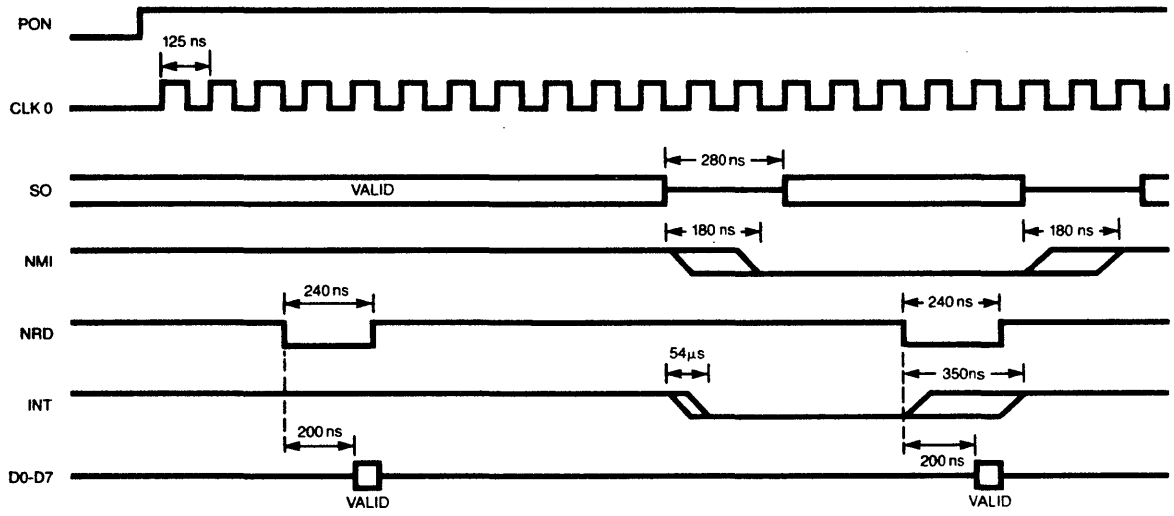


Figure I-5. MLC Output Timing

MLC OPERATION

Communication Protocol

Information is received from HP-HIL devices by polling, with the main processor being the originator of most commands including data polls. The MLC passes on these command or data frames to the SLC chips in 15-bit frames as shown in figure I-6.

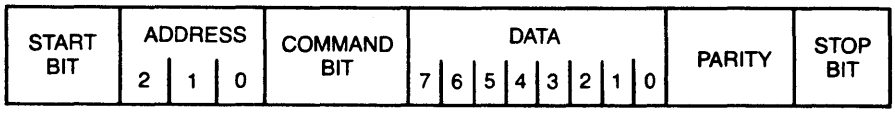


Figure I-6. Frame Bit Allocation

The command bit distinguishes a command from data. The address field indicates the destination device in a frame sent by the main processor, or the source device in a frame sent by a device. A universal address (000) is used to send a single command to all devices. The 8-bit data field contains the opcode for a command, or 8 bits of data.

In addition to the command frames originated by the main processor, the MLC can automatically generate a universal poll frame. This feature allows the System to automatically poll the HP-HIL devices periodically without processor intervention.

When a device (a SLC and a COPS processor) receives a command frame, it responds by sending either some data frames followed by the command frame, or just the command frame on to the next device. This continues until all the data frames followed by the command frame are sent back by the last device in the Link and are captured by the The MLC. The MLC has two modes of interrupt operation; in the first, the processor is always interrupted when the command frame is returned. In the second, the processor is interrupted only when data has been received prior to the command frame. This feature allows the processor to limit the interrupts from MLC in response to universal polls to only those cases where actual data has been received.

MLC and HP-HIL

Most of the commands sent by the MLC are eventually returned to SI. The exceptions occur when no devices are attached, when the last SLC is not in Loop-Back Mode (its power-up configuration), or as a result of certain commands such as Device Hard Reset that take the last SLC out of Loop-Back Mode. The MLC chip traps all returned frames (data and commands) in its FIFO. When a command frame or error code reaches the MLC chip, the MLC interrupts the main processor for data collection. Further incoming frames are subsequently ignored except for Master Hard Reset until the next command is sent.

Specific Link restrictions require that only one command frame can be on the Link at one time in the normal operating mode. Thus a device that has received a command frame knows that it can take as much time as necessary to respond to that command since no new commands will arrive. Devices have the ability to originate certain commands such as data error occurrence (frame or parity error) and Master Hard Reset.

MLC and the Main Processor

The Link address of each HP-HIL device is assigned sequentially, begining with address one (1), during the configuration sequence (initiated by the main processor after power on). The main processor can send commands to an HP-HIL device by writing the appropriate device address, command bit, and opcode to the MLC's registers W1-W0. The address (0 0 0) is the universal address; all HP-HIL devices will respond to it. After the main processor writes a command, the MLC computes the parity bit, adds the start and stop bits, and transmits the frame to the HP-HIL devices. The MLC stores any returned data in its FIFO until any command has also returned. MLC then signals an interrupt (INT = "0"). Further incoming frames are ignored with the exception of a hard reset frame. The main processor clears the interrupt by reading register R3. The main processor reads the frames stored in the FIFO by alternately reading R1 (address and command) and R0 (data) until a command frame is read. Commands sent to a nonexistent address (i.e., the "fifth" device when only two devices are on the Link) are simply returned without any data or errors.

Modes of Operation

MLC can be set into three different modes by writing registers W2 and W3: Auto Poll, Ignore Poll Frame, and Test Mode. Any combination of these modes can be set at the same time.

Test Mode

When the test bit is set, any frame written to registers W1 and W0 will behave as though SO had been shorted to SI. Each frame will be transmitted, received with no data, and if it is a command, cause an interrupt. The frame may then be read from the FIFO. While in Test Mode, the SO pin is held high ("1"). Any input externally to the SI pin will be ignored.

Ignore Poll Frame

IPF mode is used in conjunction with auto polls to ignore any polls returned without data. If IPF is set, an auto poll returned with no data will not cause an interrupt. APE will not be cleared, and the next rising edge on AP will cause another auto poll to be sent. A poll returning with data will cause an interrupt, and will clear APE. If IPF is clear, an interrupt will be generated every time a poll is returned and APE will be cleared. IPF works both for auto polls (rising edge on AP) and manual polls.

Auto Poll

Polling may be done somewhat automatically by setting the Auto Poll Enable bit. When APE is set, universal data polls are transmitted on every rising edge of the AP pin. When the poll is returned with data, (or no data and IPF is clear), APE is cleared and the main processor is interrupted. Data may then be read from the FIFO. APE must be set again before the next rising edge on AP to trigger another auto poll.

Error and Status Bits

The registers R3-R1 contains error and status information that should be read every time an interrupt or non-maskable interrupt occurs or before a command is written. Generally, when an error occurs, the appropriate error bit is set, any existing data is pushed to the top of the FIFO, and INT is pulled low. The error condition is cleared when the processor reads registers R3-R2.

Output Busy

The OB bit indicates when the registers R1 and R0 are full and may not yet be written. OB is set (= "1") when the processor writes R0 and is cleared (= "0") when the command is transfered to the output shifter. OB will clear within four microseconds if the output shifter is empty (no data being transmitted out SO), and within 154 microseconds if the output shifter is active. Reading register R1 does not clear the OB value.

FIFO Overflow

If the FIFO receives more than sixteen frames, the FOF bit is set. Normally, the FIFO is large enough to hold all the data returned by a single command. As data frames are received, they fill the sixteen FIFO words. Further incoming frames will overwrite any data in the input shifter (the "seventeenth" word in the FIFO) until the command is received. The command causes INT to go low and further frames to be ignored. In this way, sixteen data frames will be preserved, followed by the command frame stored in the input shifter. Since there is no way to know if more than sixteen data frames were received before the command was returned (since the command will have erased any data stored in

the input shifter,) the FOF bit is set. In normal operation, MLC will never receive more than fifteen data frames. Reading register R2 clears the FOF bit.

Framing Error

An FERR will occur if the STOP bit of a frame is missing (equals "0"). If the MLC was receiving data when the FERR occured, the FERR bit is set, INT is pulled low, further frames are ignored, whatever data was received is pushed to the top of the FIFO, and then the MLC enters its resynchronization routine. To resynchronize the line, MLC waits until 150 microseconds of logic "1" has been detected on the SI line. (The SI line has been idle, or high, for 150 usec.) ESD detection (a two-out-of-three voting scheme to "debounce" the input in case of an ESD hit) continues in this routine. If MLC is not receiving frames (the normal state when a command has been returned and a second command has not yet been sent) when an FERR is detected, it will still enter the resyncchronization routine, but will not set FERR, nor pull INT low. Reading register R2 clears the FERR bit.

Parity Error

If a PERR occurs (the sum of all the bits, including start and stop, is even) while MLC is receiving frames, the PERR bit is set, INT is pulled low, any data in the FIFO is bubbled to the top, and further frames (other than hard reset) are ignored. Reading register R2 clears the PERR bit.

Link Error

This error occurs when MLC tries to send an auto poll (APE="1" and AP->"1") while it is waiting for a command to be returned. This situation can happen when auto polls are sent too fast, or they are sent when the last device is not in Loop-Back Mode, or a device has failed. Or, it can occur when an automatic auto poll is the first command MLC tries to send after power-up. This is an error because the Link has not yet been configured. When an LERR occurs, MLC sets the LERR bit, clears APE, and pulls INT low. Reading register R3 clears LERR.

Non-Maskable Interrupt Bit

The NMI bit will be set only when MLC has received a hard reset command from the Link. (i.e., a CTRL-Shift-Reset on the keyboard.) When a hard reset is received, the NMI pin is pulled low for five microseconds and the NMI bit is set. The hard reset frame is not pushed into the FIFO. The NMI bit is cleared when register R3 is read.

Interrupt

The INT bit is set whenever a command is returned or an error is detected. The INT pin is pulled low and remains low until the main processor reads register R3. This will also clear the INT bit.

PROCESSOR INTERFACE

MLC requires a demultiplexed bus. It has an 8-bit wide (data bus compatible with the) Intel 80186 processor interface. It may also be interfaced to the Intel 8085/8086/8088 with virtually no additional parts.

Data is written to MLC's registers 8 bits at a time. Two read or write operations are thus required to read or write a single frame. The pin connections for the MLC - processor interface are indicated in the following diagram.

FIFO

MLC contains a 16-frame first-in first-out queue for buffering incoming data. As a frame is received, it is shifted into the FIFO. If more than 16 frames are received, the FIFO overflow bit, FOF, is set and incoming frames overwrite the last frame in the input shifter. (The input shifter acts like the 17th word in the FIFO and can be read by reading from the FIFO 17 times.) If the incoming frame is a command frame (has its command bit set), frames are shifted to the top of the FIFO, the INT line is lowered (interrupting the processor), and APE is cleared. Any frames received after this command frame (there should not be any) will be ignored until a new frame is transmitted (by a write operation to W0). If a frame with bad parity or a framing error is received, the Data Error frame (opcode FCh with address bits cleared) is written into the FIFO, the parity or framing error bit (PERR or FERR) is set, and operation continues as if a command frame were received.

The FIFO will never contain more than one command frame (and its associated data) at a time. If the contents of the FIFO are not read when an INT is signaled, the next command written to register W0 will overwrite the FIFO when it returns. As FIFO frames are read and shifted, the bottom of the FIFO fills with copies of the last FIFO item, which is usually a command frame. Continued reading of the FIFO after the command has been read will merely repeat the command frame. The FIFO is NOT cleared or set on power-up. The only way to initialize the FIFO is to send and receive a command.

Reception of a master hard reset frame (opcode FB) is the only exception to the above discussion. In this case, the NMI line is lowered for 5 us and the NMI bit in R3 is set but, the frame is not shifted into the FIFO. Further frames are received in this case. A master hard reset is always recognized when the chip is not in test mode, regardless of whether other frames are currently being ignored.

Register Allocation

There are four 8-bit output registers and four 8-bit input registers on MLC. By reading or writing to these registers, the system processor causes a command frame to be transmitted to the HP-HIL devices, a data frame to be read from one of the input devices, or the chip's operation mode to be changed. Data read from the output registers should be stored away immediately since most of the register contents will change (e.g. flag register cleared) following a read operation.

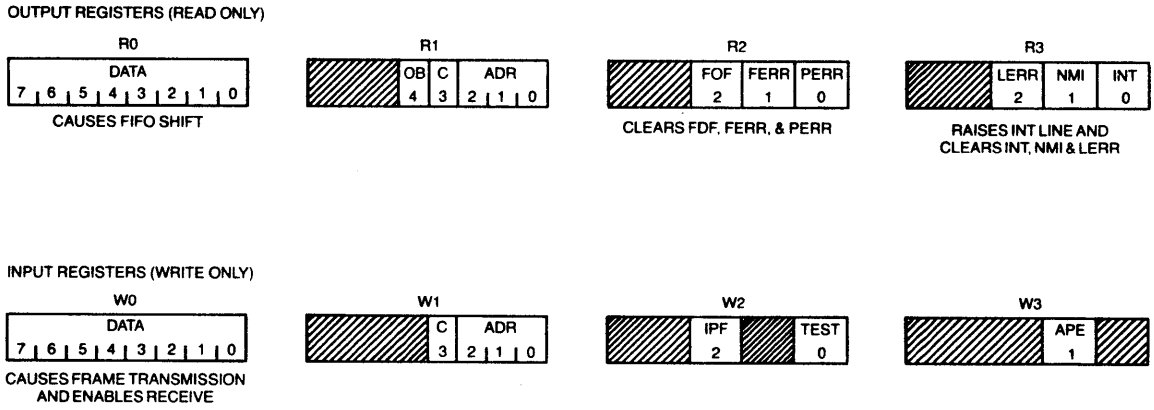


Figure I-7. MLC I/O Registers

R0,R1:

R0 and R1 contain the Link information at the top of the FIFO. The Command bit and the Address of the originator are stored in R1. The corresponding data byte is stored in R0. Reading R0 causes the next frame information in the FIFO to be loaded into the R1 and R0 registers at the end of the read cycle. By reading R1 and R0 alternately, (always read R1 before R0) information in the FIFO is transferred from the HP-HIL devices to the main system. Before initiating a Write operation to HP-HIL, the OUTPUT BUSY (OB) bit in R1 should be checked. Reading the OB bit in R1 does not destroy the data.

R2:

R2 contains the FIFO OVERFLOW bit (FOF), set when more than 16 frames (more than 15 data frames and one command frame) are returned from the input devices within the same poll cycle. It also contains the FRAMING ERROR (FERR) and PARITY ERROR (PERR) information. If any of these three bits are set, the Link integrity is compromised and the INT pin to the processor is lowered. Reading this register results in clearing of the overflow, parity error, and framing error bits.

R3:

R3 contains the LINK ERROR (LERR) bit, set during an auto-poll period when the previous poll frame did not return before the poll period expired. It is also the home for INTERRUPT bit (INT), initiated whenever an error condition is encountered (FOF, FERR, PERR, or LERR bit set), or when a command frame is received and the processor should be alerted to collect data. The NON-MASKABLE INTERRUPT bit (NMI) is set when a system hard reset command generated by one of the input devices reaches MLC. Reading this register results in clearing of LERR, NMI, and INT bits.

When the main processor is interrupted, it should read register R3 to confirm that MLC was the source of the interrupt. If that turns out to be the case, it should read register R2 to check the status of overflow, parity error, and framing error bits. If the Link integrity is sound, the processor should then read the output registers R1 and R0 and proceed to examine data returned by the input devices.

W0,W1:

When the processor wishes to send a command frame to the Link, it writes the frame into registers W1 and W0 in two seperate write cycles after the OUTPUT BUSY (OB) status bit in R1 is checked. At the end of a W0 write cycle, the frame is transmitted to the first HP-HIL device. Internally, the output data is buffered one level deep; OB will clear, allowing a second frame to be written, before the first frame transmission is complete.

W2:

The IGNORE POLL FRAME (IPF) bit in W2 can be set to cause no processor interrupt when there is no data returned from input devices in a poll period. The TEST bit is used for internal testing only; setting it will cause MLC to internally loop all data transmitted out SO back to the input SI and to ignore any external input to the SI pin. Setting the AUTO POLL ENABLE bit (APE) causes a universal poll frame to be sent to the HP-HIL output whenever a rising edge of the AUTO POLL pin (AP) occurs. This feature allows the System to automatically poll the HP-HIL devices periodically without processor intervention. It is envisioned that the video vertical sync line is tied to the AP pin, allowing automatic polling of the Link every vertical retrace time. The AUTO POLL ENABLE (APE) bit is cleared by the MLC whenever it interrupts the processor. It should thus be set by the processor as part of the interrupt handling routine.

Generation of Processor Interrupts

The INT signal is an open collector, active low output. This feature allows the INT line to be wire ORed with other interrupt signals with a single pullup resistor to provide a single interrupt line to the processor.

The NMI signal is an open collector, active low output which is held low for 5 microseconds whenever a master hard reset command (opcode FB with any address bit pattern) is received by the MLC. This feature allows the NMI line to be wire ORed with other hard reset and power on lines to provide a single reset signal. The NMI bit in R3 is set whenever MLC asserts the NMI line (except in power on; NMI pin is held low for the duration of power on without the R3 bit set). It may be read by the processor to determine that it was the MLC which produced the NMI rather than some other function (such as power on.) This may be used to determine whether or not to perform a full memory test, for instance. Note that when PON is active (low), NMI is also asserted for as long as PON is asserted. The NMI bit in register R3 is NOT set.

Clock Generator Interface

The clock signal for MLC is generated by an 8 MHz ceramic resonator connected between the CKO and CKI pins with a capacitor on each end. In addition, CKI is a TTL compatible input. This feature allows an 8MHz +/- 0.5% TTL level clock signal (such as the System clock) to be tied to CLKI to provide the clock signal for MLC. If a TTL clock signal is the input, its duty cycle must be 50% high, 50% low. Tie no additional loads to CKI or CKO. If CKI is driven by a TTL clock, CKO must remain unconnected. Do not tie CKO to ground or VDD.

While PON is active (low), the oscillator will continue to function, but the internal clock will be disabled. The following diagram indicates pin connections.

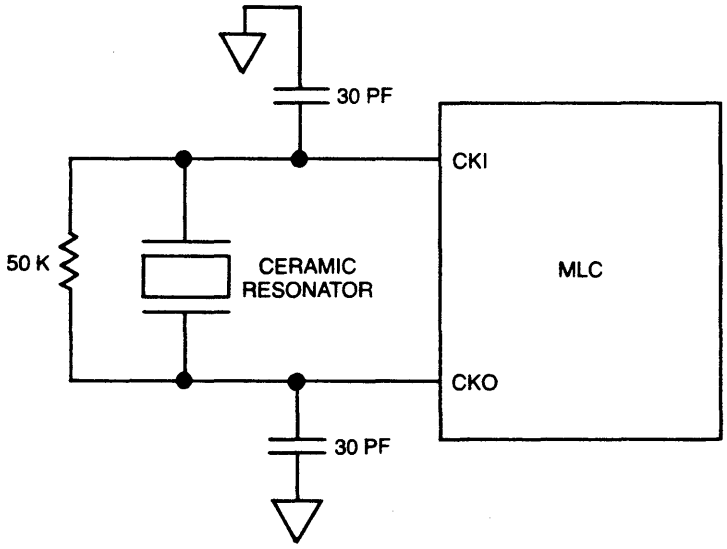


Figure I-8. Clock Interface

Power On Reset

The Power On reset pin PON is used to initialize MLC. Below is a table of pins and their values while PON is asserted (low.)

PIN #	PIN NAME	VALUE DURING PON RESET
1	NMI	ON (LOW)
2	INT	OFF (HIGH)
3	VDD	NO CHANGE
4	D0	FLOATING
5	D1	FLOATING
6	D2	FLOATING
7	D3	FLOATING
8	D4	FLOATING
9	D5	FLOATING
10	D6	FLOATING
11	D7	FLOATING
12	R	IGNORED
13	A1	IGNORED
14	A0	IGNORED
15	NRD	IGNORED
16	NCS	IGNORED
17	NWR	IGNORED
18	SO	IGNORED
19	SI	IGNORED
20	GND	NO CHANGE
21	PON	"0" WHILE ASSERTED
22	AP	IGNORED
23	CLKO	NO CHANGE, OSCILLATOR STILL WORKS
24	CLKI	NO CHANGE, OSCILLATOR STILL WORKS

Figure I-9. Pin Values after Reset

PON should be held low for 5 microseconds to ensure MLC is reset. While PON is held low, NMI is also held low, but the NMI bit of register R3 is not set. Also, the internal clock is disabled, but the oscillator (CKI and CKO) is not.

PON reset will clear (set to "0") registers R3-R0 and W3-W0. It will also clear Interrupt and will initialize the state machines. It will not clear the remainder of the FIFO. PON reset also sets the the I/O pins D7-D0 in their inactive (floating) state. They will remain floating after PON goes inactive, until the processor initiates a read or write cycle.

RFI and ESD Specifications

The MLC chip itself will be able to withstand 2.5 kV ESD hit on any of its pins without suffering hardware failure. It has been designed to tolerate ESD "noise" on its data lines up to 1.0 microsecond in duration without a data error occurring. An additional ESD protection network should be placed on the data lines since the product level ESD specification is much higher than 2.5 kV.

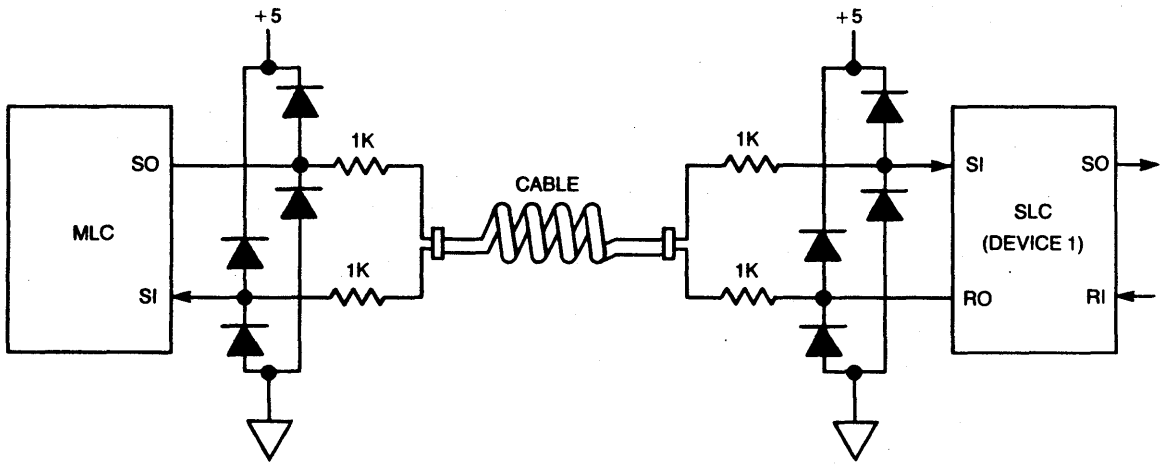


Figure I-10. ESD Protection

Preliminary RFI data indicated that the MLC data lines are sufficiently isolated from the rest of the System to cause no radiation problems. Some method of filtering on the HP-HIL power lines is recommended in order to meet the FCC specifications.

ANOMALIES

PON Reset

The PON reset input will not clear or initialize the FIFO.

While PON is asserted, NMI is also asserted. Be careful how you connect NMI and PON to the main system! If your System has NMI connected to the main processor, and this same processor controls the PON pin, the following could occur: MLC receives a hard reset and lowers NMI which causes the processor to give MLC a PON reset, which causes MLC to lower NMI, which causes a PON reset, which causes an NMI, and so on. The solution here is to connect the processor to not(not(NMI) and PON) , or alternatively, (NMI or not(PON)).

Auto Polling

Automatic auto polls (rising edge on AP when APE = 1) will work ONLY after a command (of any kind) has been sent and returned after a PON reset. This is because you cannot auto poll the Link until it has been configured. A Link Error will will occur if you make this mistake.

SI (HP-HIL) Input Pin

The SI input does not have an internal pullup. This means that unless an HP-HIL device is connected to MLC, the line will float and probably cause an error. This can be avoided by connecting a very large (probably 1 megohm) resistor pullup to SI.

Test Mode

When the TEST bit is set, registers R2 and R3 should be read to clear any old information. Do this before writing to any of the registers.

HP-HIL SLAVE LINK CONTROLLER

APPENDIX J

DESCRIPTION

The Slave Link Controller (SLC) is an intelligent UART. It allows a wide variety of human interface devices to be connected simultaneously to a terminal or personal computer. The SLC is designed to work in the HP-HIL interface, and handle the serial-parallel conversion of data and the hardware protocol for an HP-HIL device.

The SLC chip performs the serial link data handling including parity, framing error checking, and data collision avoidance. It performs address matching, data loopback, and device hard reset functionality as well as providing self test capabilities and processor clock generation.

The SLC is designed to operate with a microcomputer, specifically a member of the National COPS family, which performs the Link protocol handling as well as device data scanning. Other microprocessors can be used as well.

The HP-HIL ICs are used in HP products and are described here for reference only.

BLOCK DIAGRAM

Figure J-1 shows the block diagram for the SLC. A summary of the major blocks in the SLC are described as follows:

ISTATE: The Input State Machine, a PLA, reads the incoming data packet from the input SI and checks for ESD hits and framing errors. The packet is read RS232 style, with the start bit synchronizing the data. The data is expected at 0.1MHz (+- 2.5%). ISTATE shifts each good bit of the incoming frame into ISHIFT, and executes an error-handling routine in case of a parity or framing error. If the frame has an address match, or is a reset command, ISTATE controls resetting or interrupting the processor.

ISHIFT: The Input Shifter converts the serial input from the Link to parallel data. It checks the parity of the frame, checks for a reset command, and compares the address with the SLC's address and the group address.

OREG: The Output Register block holds the read-only registers R0 and R1. These registers are read by the processor, and are loaded with the processed data from each new frame.

SPINTERF: The Serial Processor Interface executes read/write commands from the processor. It writes the serial processor input PSI into the write-only registers W0 and W1. It reads serially from the read-only registers R0 and R1 to the serial output PSO.

OSHIFT: The Output Shifter multiplexes between processor data and incoming frame data. It builds a new frame by generating the parity bit and loading the data in correct frame format for serial transmission.

SDI: The Serial Data Interface routes the serial data SI,RI,SO RO (from the Link), and DO (from PSI). In Pass-Thru Mode, SI is sent to the processor, DO is sent to the Link through SO, and RO = RI. In Loop-Back Mode, DO is sent out RO, SO = 1, and SI is sent to the processor. In test mode, SI is ignored, DO is ultimately looped back to the processor and is sent out RO, and SO = 1.

OSTATE: The Output State Machine, a PLA, controls multiplexing, loading, and shifting for OSHIFT. It also clears R1 (Output Busy) after the frame has been transmitted.

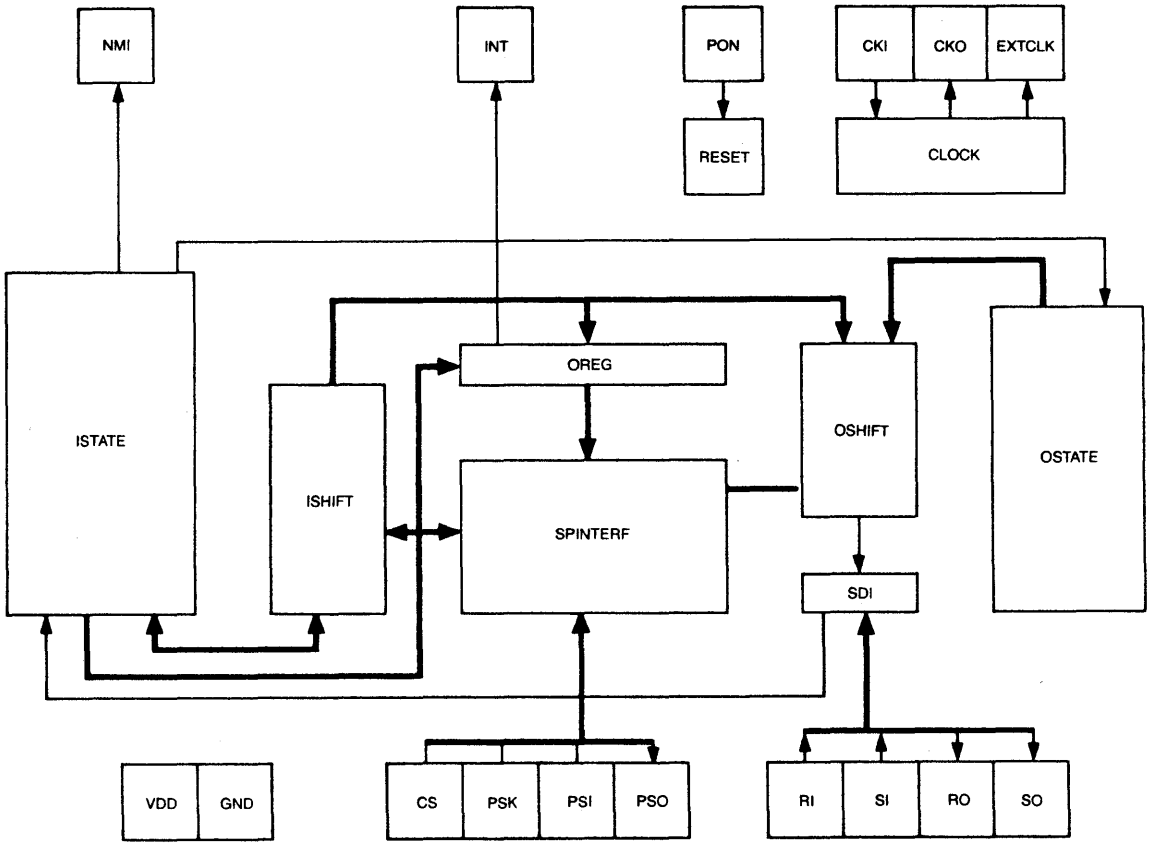


Figure J-1. SLC Block Diagram

Pinouts

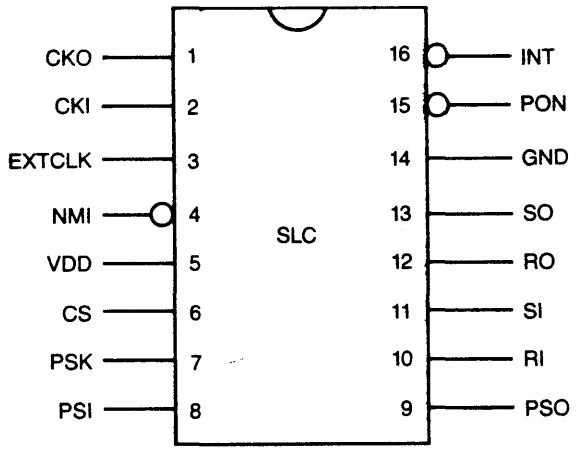


Figure J-2. SLC Pinouts

Pin Description

Pin#	Name	Description	I/O Type
1	CLKO	Clock Out, crystal hook-up only	Output
2	CLKI	Clock In, crystal or TTL clock	Input
3	EXTCLK	External Clock (=CKI/2)	Output
4	NMI	Non-maskable Interrupt, active low	Output
5	VDD	Power source, +5v	Power
6	CS	Chip Select, reads/writes	Input
7	PSK	Processor serial clock	Input
8	PSI	Processor serial input	Input
9	PSO	Processor serial output	Output
10	RI	HP-HIL return, serial in	Input
11	SI	HP-HIL send, serial in	Input
12	RO	HP-HIL return, serial out	Output
13	SO	HP-HIL send, serial out	Output
14	GND	Ground source, +0v	Power
15	PON	Power-On reset, active low Connected to external cap. (0.22uf)	I/O
16	INT	Interrupt, active low	Output

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENT

Absolute maximum ratings are limits beyond which permanent device failure may occur. These are stress ratings only; the device should not be expected to operate under these conditions (except for maximum operating ambient temperature).

Operating Ambient Temp	0 to 70 degrees C
Package Thermal Res. (Plastic)	154 degrees C/watt max
Substrate Bias Voltage (VBB) wrt GND	-2 V to -4 V
Max Vdd Supply Voltage wrt GND	7 V
Voltage Between Any Pin And GND	-1 V to 7 V
Voltage Between Any Pin And VDD	-7 V to 1 V

AC SPECIFICATIONS

Power Dissipation at VDD=5.25 V	0.03 amp, temp=0 Deg. C,

PACKAGE DESCRIPTION

The SLC is packaged in a 16-pin DIP. The rows are spaced at 7.6 mm (0.3 inches).

Conditions:

16-lead plastic package
12500 mills-square die
No air flow

Thermal Resistance:
154 Degrees C/W
Tj max = 100 C
Ta max = 70 C

DC SPECIFICATIONS

DC electrical specifications for the SLC follow. The typical values are for reference only; they are not tested.

Signal	Condition	Min	Typ	Max	Units
Operating Voltage VDD		4.75	5.0	5.25	V
Operating Supply Current	Temp=0 C VDD=max			30	mA
INPUT VOLTAGE LEVELS					
Crystal Input (if driven by TTL)					
logic high (VIH)		2.0			V
logic low (VIL)				0.8	V
Gain:					
measured at CKO	CKI=2.0 V	0.5			V/V
TTL Input					
logic high (VIH)	VDD=max	2.0			V
logic low (VOL)	VDD=min			0.8	V
HP-HIL (Schmitt Trigger)					
logic high (VIH)	VDD=max	3.0			V
logic low (VIL)	VDD=min			0.8	V
hysteresis			1.1		V
Pon Input (if driven by TTL)					
logic high (VIH)	VDD=max	3.0			V
logic low (VIL)	VDD=min			0.8	V
Input leakage Current					
RI,SI	Vin=0	-20.0			uA
Other inputs	Vin=0	-10.0			uA
PON	Vin=VDD max		60.0		uA
Other inputs	Vin=VDD max			10.0	uA

OUTPUT VOLTAGE LEVELS

HP-HIL Output				
logic high (VOH)	VDD= min			
	IOH= 0 mA	3.3		V
logic low (VOL)	IOL= 5 uA		0.4	V
TTL Output	VDD=min			
logic high (VOH)	IOH=-0.1 mA	2.4		V
logic low (VOL)	IOL= 1.6 mA		0.4	V
Interrupt Output	VDD=min			
logic high (VOH)	IOH=-0.1 mA	3.3		V
logic low (VOL)	IOL= 1.6 mA		0.4	V
Pon Output				
logic high (VOH)	VDD=min			
	IOH=0.0 mA	3.0		V
logic low (VOL)	VDD=3.5 V			
	IOL=0.0 mA		0.5	V

AC SPECIFICATIONS

Clock Specifications

AC clock specifications for the SLC are listed below.

	min	max	units
Clock Frequency (CKI)	7.96	8.04	MHz
Clock Duty Cycle (Low/High)	33/67	67/33	%

Capacitance - External

Maximum capacitive load for SO = 600 pF.

Maximum capacitive load = 60 pF for all other outputs. This is equivalent to two TTL loads.

PON Reset capacitor = 0.22 +/- 20% uF. This capacitor is connected between the PON input and ground.

Capacitance - Internal

Maximum capacitance seen at input = 10 pF.

SLC Basic Timing

Figure J-3 shows the SLC timing relationships.

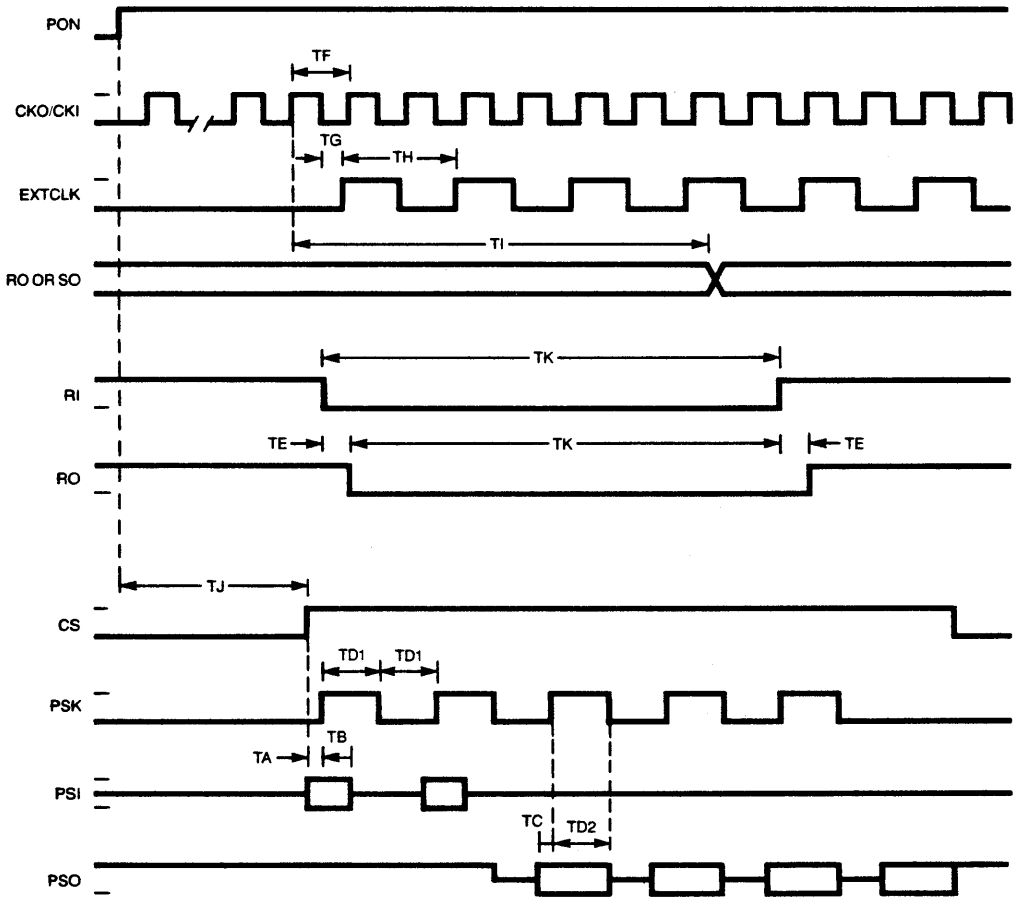


Figure J-3. SLC Timing

Name	Nominal*	Guaranteed
TA - PSI valid time before rise of PSK. Also, delay from rise of CS to first rise of PSK.		800nS min
TB - PSI data hold time after rise of PSK.	1000nS typ	950nS min

TC -	PSO valid before rise of PSK.	1700nS typ	300nS min
TD1-	Width of PSK high or low.		2000nS min
TD2-	Data hold time for PSO after rise of PSK.	2000nS typ	460nS min
TE -	In Pass-Thru Mode, delay of RO from RI.	440nS max**	
TF -	Period of CKO or CKI.	125nS typ	120nS min
TG -	Delay from fall of CKO to rise of EXTCLK.	100nS max**	
TH -	Period of EXTCLK. (=2 x CKO)	250nS min	
TI -	In Loop-Back Mode, delay of RO from CKO, or, in Pass-Thru Mode, delay of SO from CKO	910nS max**	
TJ -	CS disable period after rise of PON or rise of NMI. (=256 x CKI)	32uS typ**	
TK -	Period of RI, RO, SI, or SO. (=10 x [CKI/8])	10uS typ**	

* Nominal values are for reference only. They will not be tested.
** Calculated

SLC and Processor Interface Timing

The processor interface is intended to be connected directly to the serial MICROWIRE (TM) interface of a National COPS (TM) microcomputer. Specifically, members of the COPS 400, 410, 420, 440, and 2440 families may be directly interfaced to the serial SLC. The COP 422 will be most commonly used. It is possible to interface other processors to the SLC if these processors provide signals which emulate the MICROWIRE (TM) interface as shown in Figure J-4. The timing for the SLC and processor interface is shown in Figure J-5.

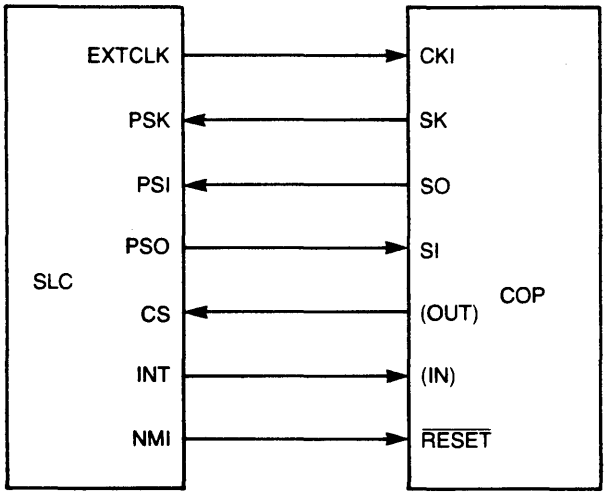


Figure J-4. Processor Interface

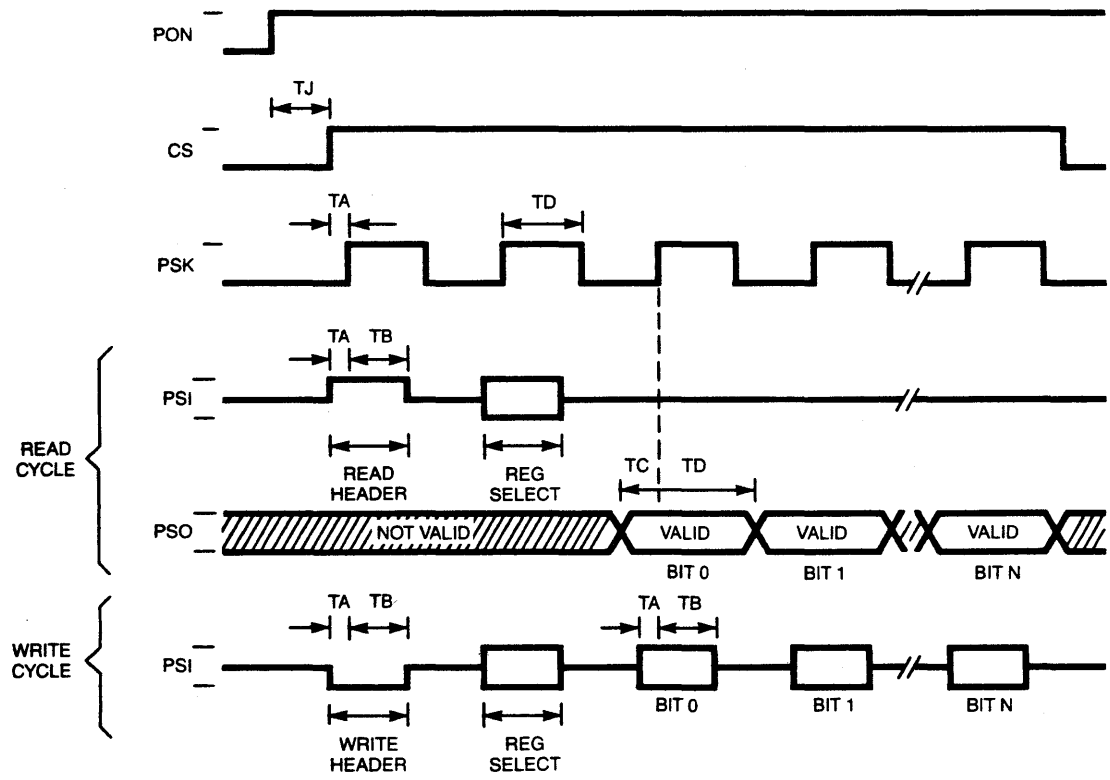


Figure J-5. Processor Interface Timing

Name	Value
TA - PSI valid time before rise of PSK. Also, delay from rise of CS to first rise of PSK.	800nS min
TB - PSI data hold time after rise of PSK.	1000nS min
TC - PSO valid before rise of PSK.	1700nS max
TD - Width of PSK high or low. Also, data hold time for PSO after rise of PSK.	2000nS min
TJ - CS disable time from rise of PON or rise of NMI. (=256 x CLKI)	32uS typ

SLC OPERATION

Register Allocation

The data registers on the SLC are organized as two read only shift registers R0 and R1 (14 bits and 1 bit) and two write only shift registers W0 and W1 (12 bits and 7 bits.) All registers are accessed serially.

Figure J-6 indicates the actual bit allocations for the registers. The arrow indicates the direction data is shifted in or out of each register. For example, when reading register R0, the first bit read will be FERR. When writing register W0, the first bit written will be C.

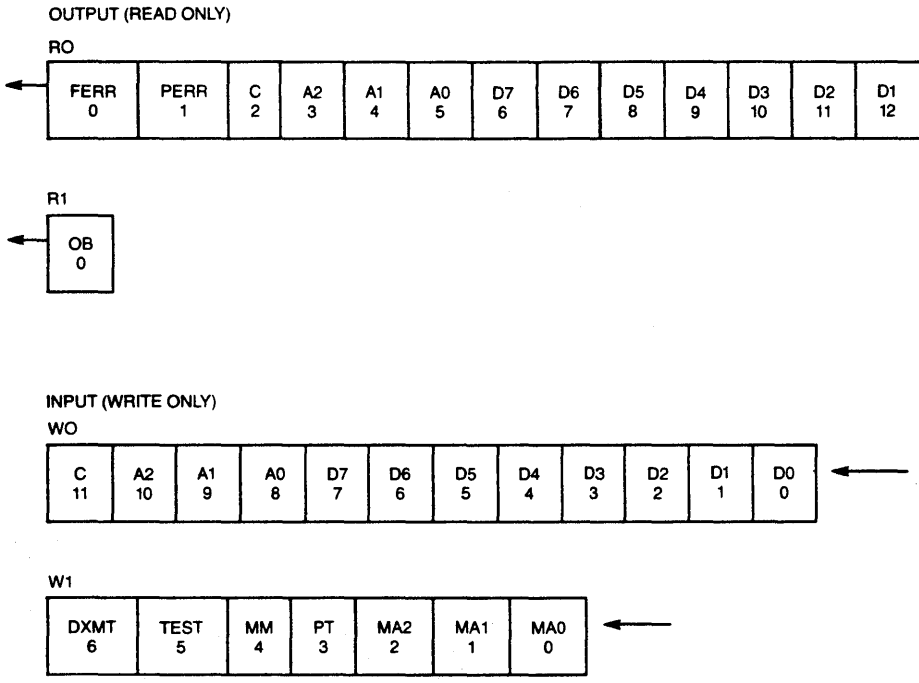


Figure J-6. SLC Read & Write Registers

The meaning of the IO register bits follows:

RO: Reading RO clears the INT line.

FERR - Set if a frame with a framing error has been received. Clear otherwise. This bit is reset after RO is read.

PERR - Set if a parity error was detected on the most recently received frame. Clear otherwise.

C - The command bit of the most recently received data frame.

A0-A2 - The address bits of the most recently received data frame.

D0-D7 - The data bits of the most recently received data frame.

R1: OB - Output Busy. Set while a frame is in WO, awaiting transmission. Clear when WO is empty.

WO: Transmission of frame is initiated upon completion of write to WO.

C - Command bit for frame to be transmitted.

A0-A2 - Address bits for frame to be transmitted.

D0-D7 - Data bits for frame to be transmitted.

W1: DXMT - Disable Transmit mode. When this bit is clear, any data frame that is received whose address does not match is retransmitted either out the SO or the RO line, depending on the setting of PT. If this bit is set, however, any unmatched frames are not retransmitted. This bit should remain clear except while self test is being performed.

TEST - Test mode enable. Setting this bit causes serial data from the output register to be transmitted back to the input register for testing purposes regardless of the setting of the PT bit.

MM - Master Mode enable. Setting this bit causes all frames to be trapped regardless of their address. All devices will in general have this bit clear, except during self test.

PT - Pass-Thru Mode enable. Setting this bit causes all frames to be transmitted out the SO (serial data out) line, generally to the next device on the Link. Clearing this bit causes frames to be transmitted out the RO (return data out) line, generally to the previous device on the Link. The last device in the Link should clear this bit, all others should set it.

MA0-2 - Match Address. Any received frame which has this address in its address field is trapped.

All bits in all registers are initialized to 0 on power up.

Read/Write Operations

SLC's processor interface has four signals that perform read and write operations. On the COP microprocessor, these signals are part of the COP MICROWIRE interface. CS is the SLC chip select, asserted by the micro. PSK is the data clock, PSI is serial data in, and PSO is serial data out.

Both read and write operations have the following format:

Chip Select	+ R/W header	+ Reg.#	+ Clock (data)	+ Clock (data)	+	+ Clock (data)	+ End Select

The fist two bits are the header the microprocessor writes to the SLC to initiate an opertaion. The R/W header is "1" for a read and "0" for a write. The Reg.# is "1" for register R1 or W1, and "0" for register R0 or W0. The remaining clocks either clock data in for a write operation, or clock data out for a read operation. Figure J-7 has examples of both operations.

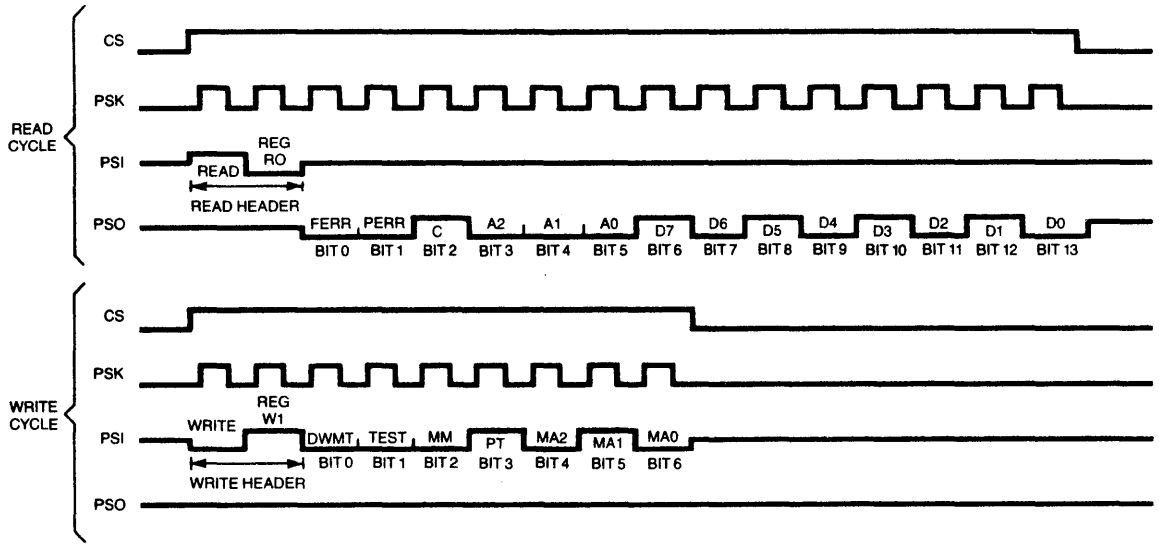


Figure J-7. Example Read/Write Operations

Link Data Handling

SLC handles all HP-HIL communication for the microprocessor. The HP-HIL pins (SI, SO, RI, RO) connect the SLC to the previous and possibly the following device.

HP-HIL communication is a simple asynchronous serial protocol between the main processor and the input device. Information travels asynchronously in the Link in a fixed format called a "frame." Each frame consists of 15 bits of information including start, stop, command, parity, address, and data bits. Information packets are transmitted around the Link at the rate of 10 microseconds per bit, or 150 microseconds per frame. The idle state of the Link is a logic "1", with the first bit in a frame (the start bit) at logic "0" and the last bit (the stop bit) at logic "1." The parity bit is computed so that the total number of logic "1" bits in the 15-bit frame (including start, address, command, data, parity, and stop) is odd. Figure J-8 shows the frame bit allocation.

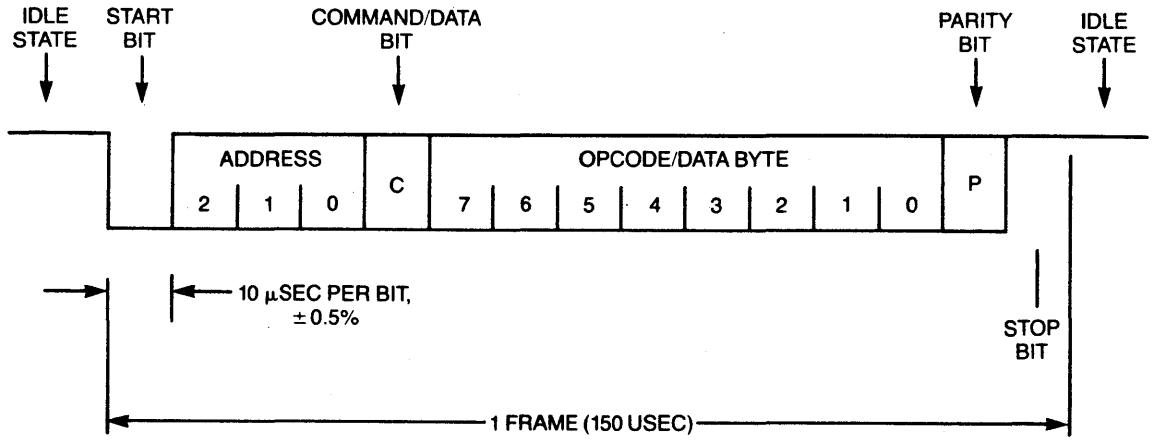


Figure J-8. Frame Bit Allocation

The command bit distinguishes a command (command bit set) from data.

The address field contains the destination device(s) of a frame. An address field of 000 is used as the universal address, indicating that all devices are targetted as destinations for the frame.

The data field contains the 8 bit opcode in the case of a command, or 8 bits of data.

A frame which is received by the SLC is automatically retransmitted unless one or more of the following conditions occur:

1. The address bits of the frame are 000 - the universal address.

2. The address bits of the frame equal those contained in the MA field of W1 - the device's individual address.

3. The frame has a parity or framing error.

4. The DXMT bit in W1 is set.

If one of the above cases has occurred, the frame is transferred to the R0 register where it can be read by the processor and the INT line is lowered, interrupting the COP. The INT line is raised upon completion of a read from R0.

Besides automatically retransmitting frames which do not satisfy any of the above conditions, the SLC transmits any frame which is written by the microprocessor into the W0 register. Anticollision logic ensures that a frame written to W0 will not interfere with one being retransmitted. Data written to W0 is buffered one level deep. After the data written to W0 is transferred to an output shifter for formatting and transmission on HP-HIL, the SLC indicates that W0 may be written again by clearing the output busy bit OB in R1.

Similarly, received data is buffered one level deep. Frames are received by an input shifter. Data frames are transferred to the ouput shifter for retransmission. Command frames are loaded into R0 upon completion. The next frame may be received as soon as the first is transferred to R0. Although the command in R0 could be overwritten should another frame be received, HP-HIL protocol ensures only one command will be on the Link at a time. (Specifically, only one universal address command, or one device-specific command will be on the Link at a time.) In the special cases where devices initiate commands, such as hard reset, they add their own address to the frame, thus allowing that command to be ignored by other devices.

The SLC can receive a new frame every 153 microseconds and transmit a frame every 154 microseconds. This implies a minimum required idle period of 3 microseconds between receiving frames and a minimum of 4 microseconds between sending frames. The only exception to this is the Device Hard Reset command. In this case an idle period of at least 60 microseconds is required between receiving the hard reset and the next frame.

Processor Hard Reset Handling

The device's processor handles all commands and data except for two special commands which are handled directly by the SLC. If a Device Hard Reset frame (data field of FEh, the command bit set, and a matching address) is received, the SLC lowers its NMI line for 50 uS - generally resetting the device processor. The frame is automatically retransmitted, even though an address match has occurred.

Test and Loopback Capabilities

The SLC is set into Loop-Back Mode by clearing the PT bit in register W1. In this mode, SO and RI are connected internally. All data normally transmitted out SO will be transmitted out RO. This is necessary for the last device on the Link to return data to the main processor. SO will be held at "1". Any external input to the RI pin will be ignored.

By setting the TEST bit, SO and SI are connected internally so that the SLC will transmit frames to itself, allowing the chip to be functionally tested. While in this mode, SO is held at "1" and any external input to the SI pin is ignored. RO and RI are not affected, so any input to RI is transmitted out RO.

Figure J-9 illustrates these modes.

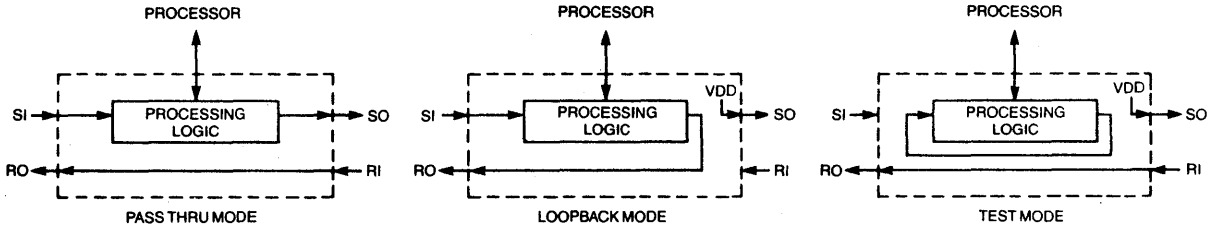


Figure J-9. Data Interface Modes

Clock Generator Functionality

The clock signal for the SLC is generated by an 8 MHz ceramic resonator and capacitor pair connected between the CKO and CKI pins. For correct operation with a ceramic resonator, absolutely no other loads should be connected to CKO or CKI. Alternatively, an 8 MHz TTL clock signal may be input to CKI, with CKO remaining disconnected. The chip outputs a 4 MHz square clock signal on the EXTCLK line for use by the COP microcomputer. Figure J-10 shows the clock circuit.

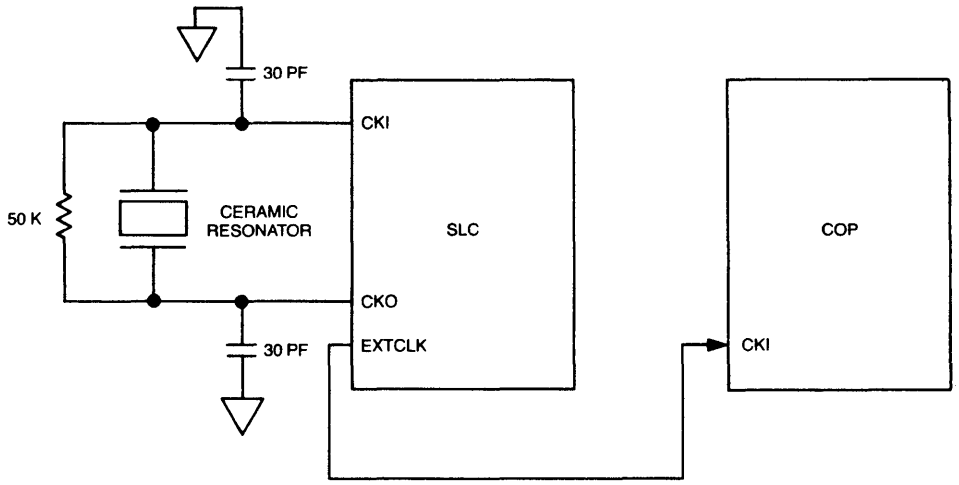


Figure J-10. Clock Generator Circuit

RFI and ESD Specifications

The SLC chip itself will be able to withstand 2.5 kV ESD spikes on any of its pins without suffering hardware failure. Each device should be able to withstand 25 kV spikes on any of its data or power lines without suffering a hardware failure. the SLC has been designed to tolerated ESD or RFI "noise" on its data lines up to 1000 nanoseconds in duration without a data error occurring.

RECOMMENDED COMPATIBLE PARTS

The following parts are recommended for use on devices as being the most compatible with the SLC.

Recommended Device Microcontrollers

The COP400 family microcontrollers are recommended for ease of integration with the SLC, and low cost. Alternatively, any controller may be used to emulate the CS, PSK, PSO, and PSI signals.

Recommended Clock Generators

The clock generator logic on the SLC has been designed to function correctly with the following ceramic resonator and temperature compensating capacitor pair. Use of other components is discouraged.

HP part# 0410-1556

(Kit includes 8MHz ceramic resonator and temperature compensating dual capacitor.)

Recommended PON (Power-On Reset) Capacitor

The PON pin should be connected to ground through a capacitor. The value of the capacitor should be chosen so that NMI goes high (unasserted) only after VDD has reached the minimum operating voltage. This is to prevent the microprocessor from waking up before a good VDD voltage has been reached. A capacitor value of 0.22 +- 20% microfarads is recommended.

ANOMALIES

PON Reset

The PON reset will clear (set to "0") registers W1, W0, R1, and R0. While PON reset is asserted, the following signals are affected:

EXTCLK is held at "0", but the oscillator continues to function.

NMI is held at "0".

CS is ignored.

PSO

The serial output signal PSO does not tristate when the chip is deselected (CS = "0").

Self Test

After setting the TEST bit, read registers R1 and R0 to clear any data that may have been present. Do this before writing any data to W1 or W0.

GLOSSARY OF TERMS

APPENDIX K

Absolute Positioner:

Any input device which provides positional information based on a fixed coordinate grid, with the origin at the lower left. All position data from this type of device will consist of unsigned integers.

Acknowledge:

An audible or visual indicator signaling to the user that some type of input has been received.

Button:

A specialized keyswitch typically found on cursor-positioning devices.

Character Data:

Data which can be subgrouped as keyswitch transitions (keycodes), ASCII data, or Binary data.

Character Entry Device:

This type of input device reports data as a series of 8-bit ASCII characters, keyswitch transitions, or binary data bytes.

Command:

Any HP-HIL frame in which the command bit is set.

Configuration:

The process by which HP-HIL devices are electrically chained together, assigned a unique address based on their position in the Link, and characterized based on their Device ID and other capabilities.

COPS:

Any member of a family of 4-bit microcontrollers manufactured by National Semiconductor Corp. The SLC is specially designed for simple interface to the COPS family. Interface with other microprocessors or microcontrollers may be accomplished as well.

Data:

Any HP-HIL frame in which the command bit is clear.

Device ID:

One byte indicating the device type and localization (in the case of a keyboard or keypad).

Downstream:

Meaning away from the System. A reference made at a given input device on the Link to indicate a direction away from the System. Moving downstream is moving logically away from the System.

Electromagnetic Interference (EMI):

Interference caused by computing (or other equipment) which can interfere with television and radio reception, and operation of other electronic equipment.

Electrostatic Discharge (ESD):

Static electricity generated by objects and people and may be discharged through equipment and other objects. Common to most any working environment unless special protection measures are taken. Voltage levels of 10,000 volts are easily generated by a person walking across carpeting. When a statically charged person touches something (like an input device), the object will generally provide a path (directly or indirectly) to ground. When equipment is not protected against ESD, the discharge path often becomes sensitive circuitry, which can easily be destroyed by only several thousand volts or less.

Ergonomics:

An aspect of technology concerned with the relations of humans and machines.

FIFO:

A queue or data stack which provides data in the order it is entered, i.e., first in, first out. This is abbreviated FIFO.

Frame:

A series of 15 bits of information, including start, stop, command, parity, address, and data bits, according to the HP-HIL standard. These frames are transmitted around the Link at the rate of 10 microseconds per bit, or 150 microseconds per frame. Note that frames are generally referred to by a three digit hexadecimal number, with the most significant bit being the command bit, followed by address bits A2 - A0, and by data bits D7 - D0. Thus, a command with address 0 (universal), and opcode 34h would be referred to as 834h; while a data frame with address 5 and data byte of DFh would be 5DFh.

HP-HIL:

The Hewlett-Packard Human Interface Link, a standard for interfacing a personal computer, terminal, or workstation to its input devices, and providing a standard interface across the Hewlett-Packard personal computer product line.

Input Device:

Any device conforming to the HP-HIL standard for data entry and cursor positioning, is designed to collect information from the user and relay this data to the System.

Keyboard:

A character entry device consisting of an array of keyswitches, reporting information as a sequence of keyswitch transitions. The keyboard provides the primary form of textual input to the System.

Keycode:

Character data which indicates that an up or down transition of a keyswitch or button has occurred.

Keying:

A physical method used to prevent similar types of connectors from being inserted into the wrong recepatacles.

Keypad:

Similar to a keyboard, but possessing fewer keyswitches and designed to support more specialized data entry, such as numeric data input.

Keyswitch AutoRepeat:

A function of a keyboard providing multiple reports for a single transition. This may be used to generate the "repeating keys" feature in the System.

Last Device (or End Device):

An input device characterized by having only one SDL connector, thereby not allowing other devices to be connected to it. This device will always reside at the end of the Link. This is not recommended when designing input devices.

Loop-Back Mode:

A mode in the SLC which causes the device to transmit all frames back toward the previous device and System.

Master Link Controller (MLC):

An HP standard IC developed by Hewlett-Packard that interfaces the System to the HP-HIL input devices. The MLC accepts commands from the System processor and transmits and receives information via HP-HIL. It also polls the input devices, collects data entered by the user, and relays it to the System.

Match Address:

The address given to devices during the configuration process. The match address corresponds to the order of devices connected on the Link. The device connected directly to the Host will have a match address of 1. The next device connected to the device with address 1 will have match address 2, etc. The maximum match address is 7. Address 0 is a universal address.

Output Device:

A printer, plotter, tone generator, or any device primarily intended to direct information back to the user. In contrast, the role of the input device collects information from the user and directs it to the System.

Pass-Thru Mode:

A mode in the SLC which causes the device to transmit all frames to the next device on the Link, if there is one. If no additional device is connected, the transmitted informtion is lost.

Polling:

The process of requesting data from the input devices.

Power-Up Mode:

A condition in an HP-HIL device during which all HP-HIL commands except for Interface Clear, Device Hard Reset, and Device Soft Reset are ignored. This mode is cleared upon reception of the Interface Clear command, and set when an error is detected or the device is reset.

Prompt:

An audible or visual indicator signalling the user that the System is ready for some particular type of input.

Radio Frequency Interference (RFI):

Interference caused by computing (or other) equipment which can interfere with television and radio reception. Both foreign and domestic regulatory agencies set limits and verify compliance of new equipment.

Relative Positioner:

This type of input device reports positional information as movement relative to the previous position, with no established origin. Thus, all information is reported as a series of 2's complement integers reflecting an offset from the previously reported position. Positive movement is defined as up and to the right.

SELV:

Stands for Safety Extra Low Voltage. A term used by the IEC (International Electrotechnical Commission) to denote voltage less than 42.4 volts peak, provided by an SELV transformer.

Shielded Data Link (SDL):

Denotes the style of connector used for connecting devices and systems together which support HP-HIL.

Slave Link Controller (SLC):

An HP standard IC developed by Hewlett-Packard that provides the communication interface between MLC, the HP-HIL communications master, and the microprocessor which controls the input device's hardware.

System:

The personal computer, terminal, or workstation which contains the HP-HIL controller and the MLC.

UART:

Universal Asynchronous Receiver Transmitter. A communications device or IC which serves as a communications controller by providing an interface to a system and handling both transmission and reception of data, asynchronously.

Universal Address:

This is an address of 0 (zero) which causes all devices on the Link to respond.

Upstream:

Meaning toward the System. A reference made to indicate direction from an input device on the Link. Moving toward the System from a given device is moving "upstream."

INDEX

A

B

C

D

E

F

G

H

I

L

M

N

O

P

R

S

T

U

V

W

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HP-HIL Technical Reference Manual

Product No. 45918A January 1986

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