Computer Peripherals

HP-82901 M/S & HP-82902 M/S

Flexible Disc Drive Service Manual

HEWLETT PACKARD

SERVICE MANUAL

HP 82901M/S & HP 82902M/S Flexible Disc Drive Service Documentation

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Table of Contents

Chapter 1
General Information

Introduction

This service manual contains information to help you troubleshoot and repair HP 82901M/S and HP 82902M/S Flexible Disc Drives.

The manual is divided into six Chapters, which give:

A description of the disc drives (Chapter 1).

An explanation of how they work (Chapter 2).

Information for disassembling and reassembling a disc drive (Chapter 3).

Steps for troubleshooting, repairing, and testing a disc drive (Chapter 4).

Lists of replaceable parts (Chapter 5).

Reference diagrams (Chapter 6).

Before using this manual in an actual repair, read through Chapters 1 and 2 to learn about the disc drives and their operation, and Chapters 3 through 6 to become familiar with the service procedures.

Description

HP 82900-Series Flexible Disc Drives are peripheral mass-storage devices that connect to a computer (such as the HP 85 Personal Computer with a Mass Storage ROM) using an HP-IB (Hewlett Packard Interface Bus). These devices use two-sided flexible discs, providing fast storage and retrieval of data.

Master disc drives and add-on disc drives are available. A master unit connects directly to the HP-IB and interacts with the computer. An add-on unit expands the capacity of a master unit by connecting directly to the master unit and interacting with it.

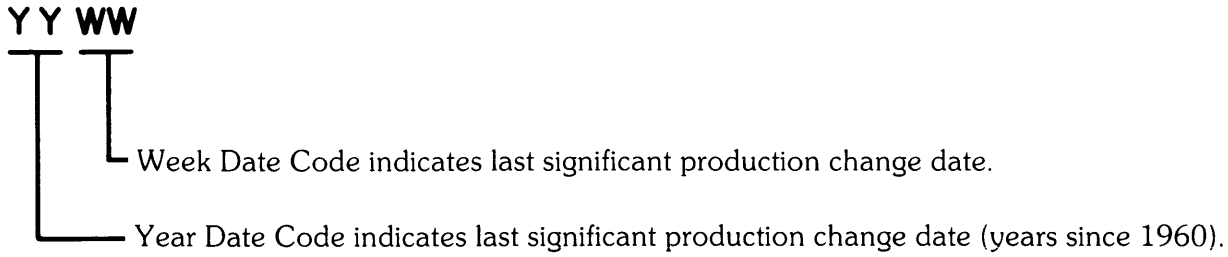
Specifications of HP 82900-Series Flexible Disc Drives are listed in table 1-1.

Table 1-1. Specifications

Physical Properties	
Height:	11.0 cm (4.31 in.).
Depth:	37.5 cm (14.75 in.).
Width:	
HP 82901M/S:	42.5 cm (16.75 in.).
HP 82902M/S:	27.9 cm (11.00 in.).
Weight:	
HP 82901M/S:	9 kg (20 pounds).
HP 82902M/S:	6 kg (14 pounds).
Power Requirements	
AC Line Voltage:	90-127 or 200-254 Vac (switchable).
Line Frequency:	50-60 Hz.
Fuse:	AC
Line Voltage:	1A (115V), T 500 mA (230V).
Power Consumption (maximum):	
HP 82901M/S:	80 watts.
HP 82902M/S:	55 watts.
Compatibility:	
HP 82901M/82902M:	Interfaces with computer using HP-IB.
HP 82901S/82902S:	Connects to HP 82901M/82902M.
Drives	
HP 82901M/S:	2 drive assemblies.
HP 82902M/S:	1 drive assembly.
Rotational Speed:	300 rpm 1.5 (4.5 rpm).
Recording Format:	MFM (Modified Frequency Modulation).
Head Life:	More than 20,000 operating hours with HP-approved disc.
Flexible Disc	
Diameter:	130 mm (5.12 in.).
Recording Surfaces:	2 per disc.
Tracks:	70 per disc (35 per side).
Sectors:	16 per track.
Bytes:	256 per sector.
Life:	More than 3,000,000 revolutions (200 hours rotating).
Temperature Limits:	10 to 52 degrees C (50 to 125 degrees F).
Environmental Limits	
Operating Temperature:	10 to 40 degrees C (50 to 104 degrees F).
Storage Temperature:	340 to 70 degrees C (340 to 158 degrees F).
Operating Humidity:	20 to 80 percent, with maximum wet-bulb temperature (non-condensing) not to exceed 25.5 degrees C (77.9 degrees F).
Storage Humidity:	5 to 95 percent (non-condensing).
Operating Altitude:	0 to 4600 m (0 to 15,000 ft).
Storage Altitude:	3300 to 15,200 m (31000 to 50,000 ft).

Identification

The serial number of the disc drive is used for identification and determination of warranty status. It is located on the rear panel next to the power receptacle. Its format is described below.



Accessories

Part numbers and descriptions of power cords used with HP 82900-Series Flexible Disc Drives are listed in table 1-2.

The part number of the interconnect cable supplied with HP 82901S/82902S Flexible Disc Drives is 82901-60007.

Table 1-2. Power Cord Description

HP Part Number	Identification
8120-1351	United Kingdom
8120-1369	Australia
8120-1378	United States (grounded)
8120-1689	Europe (grounded)
8120-2104	Switzerland
8120-2956	Denmark

CAUTION

DISC DRIVE PERFORMANCE AND RELIABILITY ARE DEPENDENT ON THE TYPE OF MEDIA USED. DISC DRIVE SPECIFICATIONS CAN BE ASSURED ONLY WHEN USING HP MEDIA. THE USE OF IMPROPER MEDIA CAN RESULT IN PREMATURE DISC FAILURE OR DAMAGE TO THE DISC DRIVE.

ON SOME DISC PRODUCTS HP MAY QUALIFY OTHER NON-HP MEDIA. WHEN TESTED, THIS MEDIA MET HP SPECIFICATIONS. HOWEVER, HP DOES NOT WARRANT OR SUPPORT THIS MEDIA AND CANNOT CONTROL CHANGES IN ITS SPECIFICATIONS OR QUALITY. THE SELECTION AND USE OF SUCH PRODUCTS IS THE CUSTOMER'S RESPONSIBILITY. HP RESERVES THE RIGHT TO EXCLUDE FROM WARRANTY AND MAINTENANCE AGREEMENT COVERAGE ANY REPAIRS WHICH HP REASONABLY DETERMINES OR BELIEVES WERE CAUSED BY THE USE OF MEDIA NOT PROVIDED BY HP. HP WILL UPON REQUEST PROVIDE SUCH REPAIRS ON A TIME AND MATERIAL BASIS.

WARRANTY AND MAINTENANCE AGREEMENT COVERAGE OF REPAIRS NOT CAUSED BY THE USE OF NON-HP MEDIA IS UNAFFECTED.

Chapter 2
Theory of Operation

Functional Description

The HP 82901M and HP 82902M Flexible Disc Drives (see Figure 2-1) are based on five primary electrical circuits:

The processor circuit.
The HP-IB (HP Interface Bus) interface circuit.
The drive assembly (one or two).
The power supply.

The processor circuit, HP-IB interface circuit, and drive interface circuit are contained on the controller PCA (printed-circuit assembly). (See Figure 6-2 for the schematic diagram of the controller PCA.) The drive and power supply assemblies are individually mounted in the unit. The HP 82901M contains two drive assemblies; the HP 82902M contains one drive assembly.

The HP 82901S and HP 82902S Flexible Disc Drives are add-on units that utilize two primary electrical circuits:

The drive assembly (one or two).

The power supply.

The HP 82901S contains two drive assemblies; the HP 82902S contains one drive assembly. The drive control function for each of these units must be provided by the controller PCA either HP 82901M or HP 82902M master unit. An add-on unit is connected to a master unit by an interconnect cable.

Flexible Disc Drive Controller PCA Theory of Operation (P/N 82901-69002)

The 82900 series flexible disc drive and 9135A disc memory may contain either the controller PCA P/N 82901-69002 or 82901-66503. The theory of operation is provided for both PCAs.

Processor Circuit

The processor circuit consists of the Processor IC, two RAM IC's, two ROM IC's and 13 other IC's and associated ciruitry that provide timing, logic and control functions.

Processor

The processor IC controls and links the HP-IB and drive interface circuits. It also provides system timing, instruction decoding, data transfer and storage, and addressing.

The processor converts a 4MHz external timing signal (EXTL) into a square-wave clock signal (CLK) having a frequency of 1 MHz.

The processor sends and receives data and instructions via the data bus. (The data bus consists of lines D0 through D7). The processor also sends information on the address bus (lines A0 through A15), activating appropriate IC's as needed.

Four input command signals also control the processor's operation. A low RES signal deactivates the processor, clearing all stored information; a subsequent high signal resets the processor to its power on state. An active NMIL or IRQ signal interrupts the processor operation after its current instruction is completed, and then initiates a new sequence of instructions. An active HALT signal stops all processor activity after the current instruction is completed; no further activity occurs until HALT goes high.

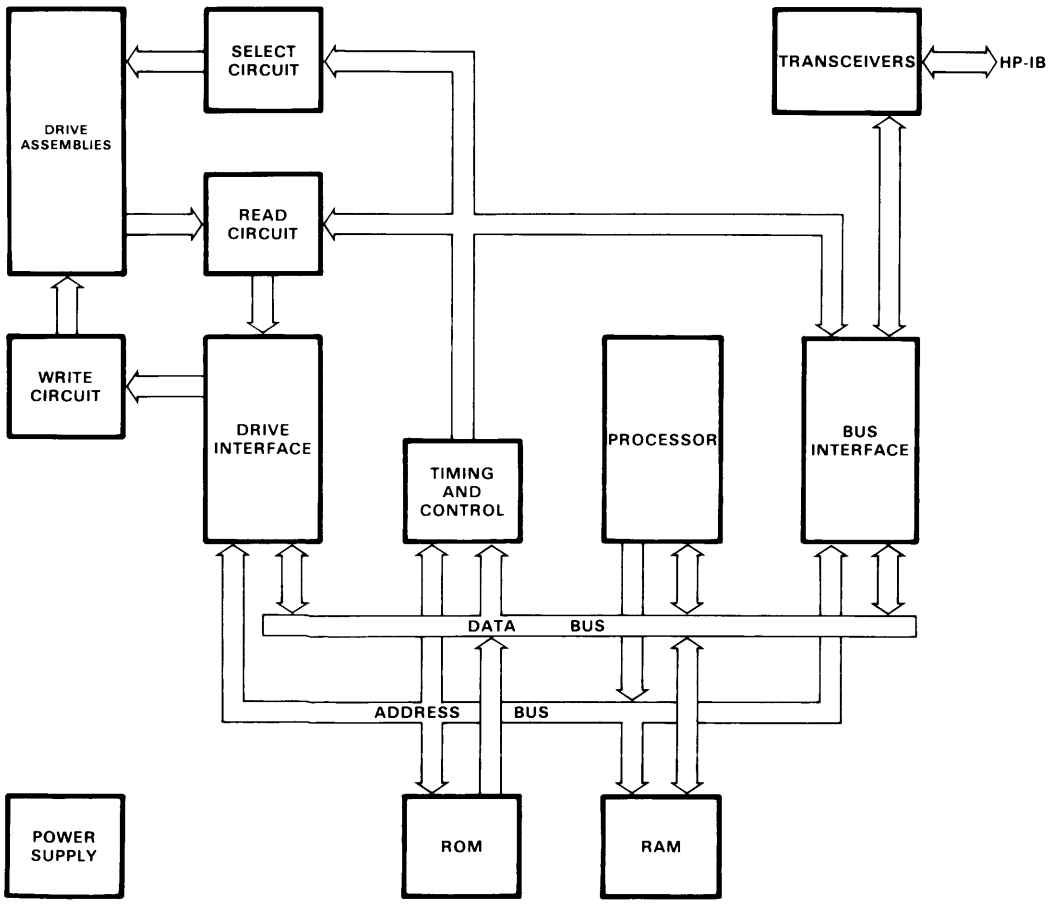


Figure 2-1. Flexible Disc Drive Controller Block Diagram

Two output signals control the operation of other IC's. The BA signal, when low, indicates that the address bus is being driven by the processor. The R/W signal indicates whether a read or write operation is occurring at the disc.

The processor IC contains 128 eight-bit registers in RAM. The RAM is used for data storage during read and write operations and for temporary storage of internal information.

RAM
Two RAM IC's, each containing 128 eight-bit registers, act as an extension to the processor's internal RAM. IC selection and address information is provided via 12 lines of the address bus. Data is sent and received on the data bus. The R/W signal controls the direction of data transmission and the CLK signal provides timing.

ROM
Two ROM IC's, each containing 2048 eight-bit microprogrammed instructions, provide information that is used by the processor to perform its operations. Only one ROM IC is enabled at any time via the CE input. Addressing is provided by eleven lines of the address bus. Instructions are sent out on the data bus.

Timing and Control

An 8-MHz signal is generated by a crystal controlled oscillator U7. Flip-flop U5B divides the frequency of the oscillator creating the 4 MHz clock signal for the processor.

Decoders U16 and U17 each use three input signals to activate up to eight output signals. The input signals are provided by the address bus and W/R line. The decoders are each activated by three gate signals provided by the CLK, BA and A14 (address) lines. The output signals activate various IC's so that they can perform their appropriate functions.

When buffer U9 is selected by U17, eight signals are transmitted on the data bus. The input signals include the interface bus address lines IBA0-IBA2, self-test and write enable switch lines, loop select line, WRPT signal and Q from U1A. The Q signal from U1A is generated from the drive INDX signal. As long as a positive INDX transition occurs each disc revolution, U1A keeps the Q signal low; otherwise Q goes high.

Latches U12 and U13, when selected by U17, set their eight output lines to the same logical states as are present on the eight data-bus lines. U12 controls the self-test LED display (DS1 and DS2). U13 controls the select circuit lines in the drive interface circuit.

The NAND gates of U11 and U14 perform two functions. Six of the gates generate the HALT signal for the processor. The HALT signal is active low when DRQ from the drive interface is low and the NMIL, IRQ and output of Q7 of latch U13 are all high. (IRQL goes low if either INTR from the drive interface or Q not from U1A goes high.) Two NAND gates convert the R/W signal to clocked WE and RE signals.

Inverters U3F and U4F use the initial rise of the +5V supply to generate reset signals RS and RST.

HP-IB Interface Circuit

The HP-IB interface circuit consists of the bus interface IC and four transceiver IC's

Bus Interface IC

The bus interface IC transfers data and commands between the processor and HP-IB, and monitors or controls the operation of the HP-IB as needed.

The bus interface contains 16 eight-bit registers. One register is used for data transfer from the HP-IB, and one register is used for data transfer to the HP-IB. The remaining registers are for monitoring the state of the HP-IB and for controlling the operation of the bus interface IC. Information is transferred to and from the processor on the data bus. Eight lines (DIO1 through DIO8) transfer information to and from the transceivers, which are connected to the HP-IB.

Eight input signals from the processor circuit control the operation of the bus interface. A high RS signal initializes the IC; a low signal enables its operation. A low CSL signal enables the interface, allowing it to send or receive data on the data bus. A low RE (or WE) specifies that the data is to be sent to (or sent from) an internal register. The register is specified by the logic states of the three address lines A0, A1, and A2 and the RE and WE lines. The CLK signal provides timing.

Six lines from the HP-IB are used for its management and control by the bus interface IC. A low ATN signal from the HP-IB causes the bus interface to monitor the DIO lines for an HP-IB command. A low IFC signal from the HP-IB causes the bus interface to discontinue its use of the HP-IB. Four bi-directional lines are controlled or monitored by the bus interface, depending on the direction of data transfer. During a read (or write) operation, the following indications are given for the signals NRFD, DAV, NDAC, and EOI:

1. A low NRFD signal indicates that the computer (or bus interface) is not ready to recieve data on the DIO lines.
2. A low DAV signal indicates that the data placed on the DIO lines by the bus interface (or computer) is valid.
3. A low NDAC signal indicates that the computer (or bus interface) has not yet read the data on the DIO lines.
4. A low EOI signal indicates the end of a sequence of information on the DIO lines.

(Low signals on both the ATN and EOI lines causes a preset "parallel poll" response to be sent on the appropriate DIO line.) Two HP-IB lines (SRQ and REN) are not used by the bus interface.

Output lines TR1 and TR2 control the direction of data flow through the transceivers. A high (or low) TR1 signal indicates that the bus interface is transmitting (or receiving) on the DIO and DAV lines and receiving) or transmitting) on the NRFD and NDAC lines. A high (or low) TR2 signal indicates that the bus interface is transmitting (or receiving) on the EOI line.

Transceiver IC's

Four non-inverting bus transceivers (U23 through U26) form the link between the bus interface and the HP-IB. Each transceiver has four data paths, each controlled by and SR input signal. A

low SR signal for a particular data path specifies transmission from the HP-IB to the bus interface IC along that path; a high SR signal specifies transmission from the bus interface IC to the HP-IB. With no power applied to a transceiver, the transceiver does not load the HP-IB lines. The transceivers also isolate the HP-IB from transient signals during power-on and power-off.

Drive Interface Circuit

The drive interface circuit consists of the drive interface IC, the read circuit, the write circuit and the select circuit.

Drive Interface

The drive interface IC encodes and transmits data between the processor the drive assembly, and controls the operation of the drive assembly. Six eight-bit registers are contained in the drive interface. One is a shift register that is used to for serial data transfer to and from the drive assembly. Another is used for the data being sent to or received from the processor. The remaining registers store status, command, and disc track/sector information.

The drive interface includes logic to generate and check the 16 CRC (cyclic redundancy check) bits in each identification and data field on the disc. These bits are used to detect errors that occur during writing to and reading from the disc.

Eight data lines (DAL0 through DAL7) are connected to the data bus. These output lines use logic that is inverted compared to the processor. Commands, status information, and data are transmitted on the DAL lines. The state of address lines A0 and A1 is used by the drive interface to determine which internal register to connect to the DAL lines.

Five input signals from the processor circuit control the operation of the drive interface IC. A low RST signal initializes the IC; the following high signal permits it to begin operation. A low CS signal from U21 enables the IC. The CLK signal is used for timing. A low RE (or WE) signal specifies that the data is to be sent to (or received from) the drive assembly and, together with A0 and A1, connects the proper internal DAL lines.

Two output signals to the processor indicate the state of the drive interface. A high INTR signal from the drive interface indicates that it has completed an operation; the signal is set low when the IC receives a new command. A high DRQ signal during a read (or write) operation at the disc indicates that the internal data register is full (or empty) and that the processor should read the data (or send additional data). The drive interface sets the DRQ low when the processor responds to the signal.

Four signals are used by the drive interface to monitor and control the operation of the drive assembly. Each high pulse to the drive assembly on the STEP line causes the head to move to the next track on the disc; A high DIRC signal causes the head to move inward on the disc; a low DIRC signal causes the head to move outward on the disc. A low TR00 signal from the drive assembly to the drive interface indicates that the head is at track 0 on the disc. A momentary INDX signal from the drive assembly indicates to the drive interface that the disc is in its reference position. (This signal occurs once every disc revolution as it spins.)

Two signals from the drive assembly are used during a read operation. Each low pulse on the

RWRD line indicates the occurrence of a magnetic flux transition on the disc. The RCLK input signal is a square wave that is derived from the data pulses on the RWRD line and is used as a timing reference for decoding the pulses.

During a write operation, the drive interface uses one input signal from the drive assembly and four output signals to the drive assembly. A low WRPT input signal indicates that a disc is write protected, preventing a write command from being executed. A high WG output signal indicates to the drive assembly that a write operation is being executed. Each high pulse on the WD output line specifies that a flux transition should be recorded on the disc. A high signal on the ERLY (or LATE) output line indicates that the corresponding pulse on the WD line should be shifted earlier (or later) in time as it is recorded on the disc. This shift compensates for distortion in the pulse patterns that occurs when the data is read from the disc.

Read Circuit

Inverters U15A, U15B, and U15D and U16A through U16C in the WRPT, INDX, and TR00 lines from the drive assembly provide buffered signals to the drive interface and the processor circuit. The data pulses on the RDTA line from the drive assembly are used to generate two signals for the drive interface: the RWRD data pulses and RCLK clock signal. The RCLK signal approximates a square wave with a nominal frequency of 8 MHz. The RCLK signal is generated such that data pulse on the RWRD line occur about midway between transitions in the RCLK signal. Data pulses are nominally received at up to 1/32 of the 8 MHz clock frequency, but the exact frequency is determined by the drive speeds at which the disc was recorded and read.

Write Circuit

Inverters U1A, U7C, U7D and U7E provide buffered STEP, DIRC, WG, and WDTA signals to the drive assembly. A data pulse on the WD line from the drive interface causes U18A to generate a short (100-ns) pulse. This pulse causes U18B to generate a similar pulse immediately following the first one. U17A and U17B each generate a data pulse immediately following its short input pulse. In effect, these four IC's create two additional data pulses, one delayed 100 ns from the WD pulse and another delayed 200 ns from the WD pulse. The three data pulses are sent to selector U12. Input signals ERLY and Late determine which of the three data pulses U32 sends to the drive assembly on the WDTA line. If ERLY and LATE are both low, the second pulse is sent.

Select Circuit

Inverters U1B through U1F, and U7B provide buffered HDSL, DRV0, DRV1, DRV2, and DRV3 signals to the drive assembly from the drive latch in the processor circuit.

Flexible Disc Drive Controller PCA Theory of Operation (P/N 82901-66503)

Processor Circuit

The processor circuit consists of the Processor IC, two RAM IC's, two ROM IC's and 13 other IC's and associated ciruitry that provide timing, logic and control functions.

Processor

The processor IC controls and links the HP-IB and drive interface circuits. It also provides system timing, instruction decoding, data transfer and storage, and addressing.

The processor converts a 4MHz external timing signal (EXTL) into a square-wave clock signal (CLK) having a frequency of 1 MHz.

The processor sends and receives data and instructions via the data bus. (The data bus consists of lines D0 through D7). The processor also sends information on the address bus (lines A0 through A15), activating appropriate IC's as needed.

Four input command signals also control the processor's operation. A low RES signal deactivates the processor, clearing all stored information; a subsequent high signal resets the processor to its power on state. An active NMIL or IRQ signal interrupts the processor operation after its current instruction is completed, and then initiates a new sequence of instructions. An active HALT signal stops all processor activity after the current instruction is completed; no further activity occurs until HALT goes high.

Two output signals control the operation of other IC's. The BA signal, when low, indicates that the address bus is being driven by the processor. The R/W signal indicates whether a read or write operation is occurring at the disc.

The processor IC contains 128 eight-bit registers in RAM. The RAM is used for data storage during read and write operations and for temporary storage of internal information.

RAM

Two RAM IC's, each containing 128 eight-bit registers, act as an extension to the processor's internal RAM. IC selection and address information is provided via 12 lines of the address bus. Data is sent and received on the data bus. The R/W signal controls the direction of data transmission and the CLK signal provides timing.

ROM

Two ROM IC's, each containing 2048 eight-bit microprogrammed instructions, provide information that is used by the processor to perform its operations. Only one ROM IC is enabled at any time via the CE input. Addressing is provided by eleven lines of the address bus. Instructions are sent out on the data bus.

Phase Lock Loop (PLL)

The phase lock loop consists of a phase clamp, frequency clamp, filter, voltage controlled oscillator (VCO) and sampler.

The VCO is a triangle wave generator with a nominal output frequency of 500 KHz. The voltage on the base of Q10 is converted to a current by darlington Q9 and Q10 and resistors R22 and VR1. The voltage drop accross R22 and VR1 is equivalent to two base-emmiter voltage drops lower than the input voltage. The current through the two resistors is directly proportional to the control voltage. That current also flows through the collector of the darlington. It is the control current supplying a current mirror consisting of Q2, Q11, Q8 and Q5 and resistors R16 and R21.

The comparator, U35, can be in one of two states. The differential outputs can have pin 9 of U35 high and pin 11 low or vice-versa. The output of U24 pin 4 is used to generate a square wave at the positive input of the comparator. The high level voltage of the square wave occurs when U24 pin 4 is high and the voltage rises to CR7's zener voltage. When the output of U24 pin 4 is low, the square wave is at the low voltage of CR8's zener plus approximately 0.2V. In both cases, the zener diodes are biased by R19.

Each time the comparator changes the triangle from increasing to decreasing slope, U4 pin is clocked. U4's output is read clock (RCLK). RCLK changes state at each triangle peak. The frequency of RCLK is one half the VCO frequency (nominally 250KHz).

The second part of the PLL is the sampling section. The triangle wave is buffered so that the sampling activity does not disturb the VCO.

The current mirror consisting of Q6, Q7, Q13 and Q14 uses the sampling current from Q2 to either pump up or pump down the filter voltage to track the data.

If sample occurs while the triangle is ramping down, the pulse is early. The VCO frequency is then increased by directing the sampling current into the filter through Q6. The other three transistors in the mirror are cut off at this time. If the pulse is late, the frequency of the VCO is high. The filter voltage is then decreased by mirroring the sampling current out of the filter. to so this, transistors Q7, Q13, and Q14 are turned on.

As the pulse moves from the triangle wave trough, the sampled triangle current increases, and the correction required is increased. The result is that the sampling pulses cause the VCO to change in such a way as to center the triangle wave troughs on the sampling pulses. Once they are centered, small changes in the data stream frequency are tracked.

The purpose of the filter is to slowly adjust the VCO control input in response to sampling pulses. The filter is required to average out the bit shift variations and to mask out some of the noise impulses.

Whenever the PLL is not tracking data, it returns to a free run state. The job of bringing the frequency to the free run value is done by the frequency clamp.

Phase clamping is used to put the VCO output at a given point in its cycle (where the read data pulses are to be locked to). The triangle wave is held to its minimum and then released on the first read data pulse. In this way, the PLL need only have to correct for frequency differences and not phase differences. This improves the probability of achieving a locked condition.

The discriminator has the task of finding the sync fields for the phase lock loop to lock to. Every section of read data that can be independently read is preceeded by a sync field. This is the part of the data stream that is intended for lock up. The discriminator consists of one half of U14 and gates U6C and U6D.

The lock up controller is responsible for the generation of the track and locked signals. It responds to the inputs from the data stream, the discriminator, and the read gate.

Control Circuit

Decoders U16 and U17 each use three input signals to activate up to eight output signals. The input signals are provided by the address bus and W/R line. The decoders are each activated by three gate signals provided by the CLK, BA and A14 (address) lines. The output signals activate various IC's so that they can perform their appropriate functions.

When buffer U9 is selected by U17, eight signals are transmitted on the data bus. The input signals include the interface bus address lines IBA0-IBA2, self-test and write enable switch lines, loop select line, WRPT signal and Q from U1A. The Q signal from U1A is generated from the drive INDX signal. As long as a positive INDX transition occurs each disc revolution, U1A keeps the Q signal low; otherwise Q goes high.

Latches U12 and U13, when selected by U17, set their eight output lines to the same logical states as are present on the eight data-bus lines. U12 controls the self-test LED display (DS1 and DS2). U13 controls the select circuit lines in the drive interface circuit.

The NAND gates of U11 and U14 perform two functions. Six of the gates generate the HALT signal for the processor. The HALT signal is active low when DRQ from the drive interface is low and the NMIL, IRQ and output of Q7 of latch U13 are all high. (IRQL goes low if either INTR from the drive interface or Q not from U1A goes high.) Two NAND gates convert the R/W signal to clocked WE and RE signals.

Inverters U3F and U4F use the initial rise of the +5V supply to generate reset signals RS and RST.

HP-IB Interface Circuit

The HP-IB interface circuit consists of the bus interface IC and four transceiver IC's.

Bus Interface IC

The bus interface IC transfers data and commands between the processor and HP-IB, and monitors or controls the operation of the HP-IB as needed.

The bus interface contains 16 eight-bit registers. One register is used for data transfer from the HP-IB, and one register is used for data transfer to the HP-IB. The remaining registers are for monitoring the state of the HP-IB and for controlling the operation of the bus interface IC. Information is transferred to and from the processor on the data bus. Eight lines (DIO1 through DIO8) transfer information to and from the transceivers, which are connected to the HP-IB.

Eight input signals from the processor circuit control the operation of the bus interface. A high RS signal initializes the IC; a low signal enables its operation. A low CSL signal enables the interface, allowing it to send or receive data on the data bus. A low RE (or WE) specifies that the data is to be sent to (or sent from) an internal register. The register is specified by the logic states of the three address lines A0, A1, and A2 and the RE and WE lines. The CLK signal provides timing.

Six lines from the HP-IB are used for its management and control by the bus interface IC. A low ATN signal from the HP-IB causes the bus interface to monitor the DIO lines for an HP-IB command. A low IFC signal from the HP-IB causes the bus interface to discontinue its use of the

HP-IB. Four bi-directional lines are controlled or monitored by the bus interface, depending on the direction of data transfer. During a read (or write) operation, the following indications are given for the signals NRFD, DAV, NDAC, and EOI:

1. A low NRFD signal indicates that the computer (or bus interface) is not ready to recieve data on the DIO lines.
2. A low DAV signal indicates that the data placed on the DIO lines by the bus interface (or computer) is valid.
3. A low NDAC signal indicates that the computer (or bus interface) has not yet read the data on the DIO lines.
4. A low EOI signal indicates the end of a sequence of information on the DIO lines.

(Low signals on both the ATN and EOI lines causes a preset "parallel poll" response to be sent on the appropriate DIO line.) Two HP-IB lines (SRQ and REN) are not used by the bus interface.

Output lines TR1 and TR2 control the direction of data flow through the transceivers. A high (or low) TR1 signal indicates that the bus interface is transmitting (or receiving) on the DIO and DAV lines and receiving) or transmitting) on the NRFD and NDAC lines. A high (or low) TR2 signal indicates that the bus interface is transmitting (or receiving) on the EOI line.

Transceiver IC's

Four non-inverting bus transceivers (U23 through U26) form the link between the bus interface and the HP-IB. Each transceiver has four data paths, each controlled by and SR input signal. A low SR signal for a particular data path specifies transmission from the HP-IB to the bus interface IC along that path; a high SR signal specifies transmission from the bus interface IC to the HP-IB. With no power applied to a transceiver, the transceiver does not load the HP-IB lines. The transceivers also isolate the HP-IB from transient signals during power-on and power-off.

Drive Interface Circuit

The drive interface circuit consists of the drive interface IC, the read circuit, the write circuit and the select circuit.

Drive Interface

The drive interface IC encodes and transmits data between the processor the drive assembly, and controls the operation of the drive assembly. Six eight-bit registers are contained in the drive interface. One is a shift register that is used to for serial data transfer to and from the drive assembly. Another is used for the data being sent to or received from the processor. The remaining registers store status, command, and disc track/sector information.

The drive interface includes logic to generate and check the 16 CRC (cyclic redundancy check) bits in each identification and data field on the disc. These bits are used to detect errors that occur during writing to and reading from the disc.

Eight data lines (DAL0 through DAL7) are connected to the data bus. These output lines use logic that is inverted compared to the processor. Commands, status information, and data are

transmitted on the DAL lines. The state of address lines A0 and A1 is used by the drive interface to determine which internal register to connect to the DAL lines.

Five input signals from the processor circuit control the operation of the drive interface IC. A low RST signal initializes the IC; the following high signal permits it to begin operation. A low CS signal from U16 enables the IC. The CLK signal is used for timing. A low RE (or WE) signal specifies that the data is to be sent to (or received from) the drive assembly and, together with A0 and A1, connects the proper internal DAL lines.

Two output signals to the processor indicate the state of the drive interface. A high INTR signal from the drive interface indicates that it has completed an operation; the signal is set low when the IC receives a new command. A high DRQ signal during a read (or write) operation at the disc indicates that the internal data register is full (or empty) and that the processor should read the data (or send additional data). The drive interface sets the DRQ low when the processor responds to the signal.

Four signals are used by the drive interface to monitor and control the operation of the drive assembly. Each high pulse to the drive assembly on the STEP line causes the head to move to the next track on the disc; A high DIRC signal causes the head to move inward on the disc; a low DIRC signal causes the head to move outward on the disc. A low TR00 signal from the drive assembly to the drive interface indicates that the head is at track 0 on the disc. A momentary INDX signal from the drive assembly indicates to the drive interface that the disc is in its reference position. (This signal occurs once every disc revolution as it spins.)

Two signals from the drive assembly are used during a read operation. Each low pulse on the RWRD line indicates the occurrence of a magnetic flux transition on the disc. The RCLK input signal is a square wave that is derived from the data pulses on the RWRD line and is used as a timing reference for decoding the pulses.

During a write operation, the drive interface uses one input signal from the drive assembly and four output signals to the drive assembly. A low WRPT input signal indicates that a disc is write protected, preventing a write command from being executed. A high WG output signal indicates to the drive assembly that a write operation is being executed. Each high pulse on the WD output line specifies that a flux transition should be recorded on the disc. A high signal on the ERLY (or LATE) output line indicates that the corresponding pulse on the WD line should be shifted earlier (or later) in time as it is recorded on the disc. This shift compensates for distortion in the pulse patterns that occurs when the data is read from the disc.

Read Circuit

Inverters U3A through U3C and U4A through U4C in the WRPT, INDX, and TR00 lines from the drive assembly provide buffered signals to the drive interface and the processor circuit. The data pulses on the RDTA line from the drive assembly are used to generate two signals for the drive interface: the RWRD data pulses and RCLK clock signal. The RCLK signal approximates a square wave with a nominal frequency of 8 MHz. The RCLK signal is generated such that data pulse on the RWRD line occur about midway between transitions in the RCLK signal. Data pulses are nominally received at up to 1/32 of the 8 MHz clock frequency, but the exact frequency is determined by the drive speeds at which the disc was recorded and read. Dual flip-flop U31 shapes the incoming pulses and syncronizes them with oscillator U27. Counter U6

generates a square wave signal at 1/16 the frequency of the oscillator; the square wave is restarted at each data pulse from U31. Flip-flop U5A uses this signal to generate the RCLK signal at 1/32 of the oscillator frequency. Logic gates U28A, U28B and U28D control the frequency of the oscillator U27. If data pulses occur early (while the output of U6 is high), U28B turns on transistor Q1, increasing the charge on C23 and raising the voltage at the cathode of varactor CR3. This decreases the capacitance of CR3 thereby increasing the frequency of the oscillator U27. The negative transitions of the signal from U6 then synchronizes with the data pulses. Conversely, if the data pulses occur late (while the output of U6 is low), U28A and U28D use the same means to decrease the oscillator frequency. Inductor L1 is adjusted so that the oscillator (U27) frequency is set to 8 MHz when the voltage at the cathode of CR3 is +5V.

Write Circuit

Inverters U2B through U2E provide buffered STEP, DIRC, WG, and WDTA signals to the drive assembly. A data pulse on the WD line from the drive interface causes U33A to generate a short (100-ns) pulse. This pulse causes U33B to generate a similar pulse immediately following the first one. U34A and U34B each generate a data pulse immediately following its short input pulse. In effect, these four IC's create two additional data pulses, one delayed 100 ns from the WD pulse and another delayed 200 ns from the WD pulse. The three data pulses are sent to selector U32. Input signals ERLY and Late determine which of the three data pulses U32 sends to the drive assembly on the WDTA line. If ERLY and LATE are both low, the second pulse is sent.

Select Circuit

Inverters U8A through U8F provide buffered HDSL, DRV0, DRV1, DRV2, and DRV3 signals to the drive assembly from the drive latch in the processor circuit.

Drive Assembly

The drive assembly is an electromechanical device that stores and reads data on removable, flexible discs. The drive assembly includes the drive circuit (one or two PCA's) mounted on the drive mechanism.

Flexible Disc

The flexible magnetic disc is 130 millimeters (5.12 inches) in diameter and is enclosed in a protective jacket. The disc is free to rotate inside the jacket, and is cleaned while it turns. A large hole at the center of the disc is used for mounting it on the drive hub, which spins the disc. The head slots in the jacket provide access to both recording surfaces by the magnetic heads. Index holes in the disc and jacket provide a reference for the position of the disc. A notch near the corner of the jacket indicates whether or not the disc can be written on. If the notch is covered by an adhesive label, the disc is "protected" and cannot be written on.

Drive Mechanism

By opening the front latch, a disc may be inserted into the guides in the drive mechanism. When the latch is closed, the disc is centered and clamped to a central hub. The hub is driven by a servo-controlled dc motor at a speed of 295.5 to 304.5 rpm. Two magnetic heads are located on one carriage, with one head on each side of the disc. A trim-erase portion of the head erases spurious signals. A stepper motor moves the heads one track for each step,

producing 70 tracks on a disc (35 on each side). The heads are in contact with the disc whenever the front latch is closed.

Three sensors provide information about drive status. The index sensor detects when the index hole in the disc passes the reference hole in the jacket. It consists of an LED and phototransistor mounted on opposite sides of the disc. The track 00 sensor detects when the head carriage is at the outer track; other head positions are not physically sensed. The write-protect sensor detects the condition of the write-protect notch in the disc jacket.

Drive Circuit

The logic section of the drive circuit contains a drive-select shunt on the PCA. The position of the jumper determines which of the drive-select lines (DRV0 through DRV3) activates the drive assembly. When the WG input signal is low, the logic section generates the signals for the recording head in response to the WDTA input line. Head 0 is selected when the HDSL input line is high; head 1 is selected when the line is low. An amplifier, filter, differentiator, and comparator convert low-level signals from the head into low pulses on the RDTA output line. A low pulse is generated on the INDX output line each time the index hole passes the sensor. If the notch at the corner of the jacket has been covered, the WRPT output preventing any data from being written onto the disc.

The servo section of the drive circuit contains a circuit that turns on the drive motor when the MTON input line is low and maintains a constant hub speed. The motor is disabled if it draws excessive current. The stepper-motor control moves the head carriage one track for each pulse on the STEP input line. The heads step toward the center of the disc (high track numbers) when the DIRC input line is low; they step toward the outer edge when the line is high.

Power Supply

The power supply (see Figure 6-4) consists of a power supply assembly, transformer, and related components.

The power supply assembly is mounted at the rear of the bottom cover. Two similar circuits provide regulated supply voltage of +5 Vdc and +12 Vdc. In each circuit, a full-wave rectifier provides an input to a voltage regulator (U1 and U2). Resistor-dividers (R1-R2 and R3-R4) convert the regulated output voltages to reference voltages for the regulators, forming a feedback loop. Diodes CR9 and CR10 provide protection for the regulators against reverse voltages. Capacitors C1 and C4 filter the ac input. Capacitors C2, C3, C5, and C6 improve transient response. Fuses F1 and F2 protect the secondary windings of transformer T1.

The power supply operates from either 115 or 230 Vac nominal. The line-voltage switch on the rear panel connects the input windings of the transformer according to the selected voltage. The input line is controlled by the ON-OFF switch on the front panel. A fuse located on the rear panel protects against current overloads (1A at 115V or T 500 mA at 230V).

System Operation

The following paragraphs describe how the circuits in the disc drive interact with each other and with the HP-IB.

Power On

When the disc drive is turned on, the RS and RST signals initialize the processor, bus interface, and drive interface IC's. The processor executes a portion of the self test, checking that the RAM and ROM IC's working properly. If any RAM or ROM IC fails the test, the processor disables the disc drive, displays the appropriate code on the controller LED's, and flashes the LED's on the front panel.

HP-IB Operation

Commands from the computer are sent on the DIO lines. The first byte (one bit on each of the eight DIO lines) is accompanied by a low ATN signal. Commands can enable or disable individual devices on the HP-IB. Devices can be instructed to send or receive data on the DIO lines, send status information, or execute other instructions.

Information is transmitted on the HP-IB using a sequence of interacting responses. Devices on the HP-IB do not accept information on the DIO lines until the DAV signal is low. Each device receiving information sets its NDAC signal high after it has accepted the information. When all NDAC lines are high, the HP-IB DAV line goes high until the next data byte is valid and each device has set its NRFD line high (indicating that it is ready for additional information). This sequence is repeated for each byte sent on the HP-IB. The sequence is used by the computer and any other device that sends information.

Writing Data

When the disc drive is to write data onto the flexible disc, the computer instructs the unit to seek a specific drive assembly, track, head, and sector, to verify that operation, to enable the unit to write data, and to enable the unit to receive the data to be written. For each of these commands, the computer instructs the unit either to receive or to send information on the HP-IB, as required.

Internally, the bus interface sets the transceivers either to receive or to send information on the HP-IB. The processor activates the proper drive assembly and head, and sends the track and sector information to the drive interface, which steps the head to the proper track as determined by reading indentification fields on the disc. Data bytes requested and received by the bus interface are sent to the processor one at a time. The processor stores each byte in RAM. When all of the data bytes (up to 256) have been received and stored, the processor stops monitoring the bus interface and enables the drive interface to write data. The drive interface reads the identification field of each sector until the proper one is found. The WG line is then set high. The processor then reads one byte of data from RAM and sends it to the drive interface. When a data byte is sent to the drive-interface input register, the data is transferred to the shift register. The drive interface then sets the DRQ line high, indicating that the processor should send the next data byte. Meanwhile, each of the eight bits is encoded by the drive interface into a series of pulses on the WD line and recorded on the disc by the magnetic head. As each data byte is recorded, the byte in the input register is transferred to the shift register and the next byte is sent by the processor. After all of the data bytes have been written on the disc, the processor

disables the drive interface and drive assembly, and begins monitoring the bus interface. The bus interface sets the NRFD line high and waits for the next command.

Reading Data

The operation of reading data from the flexible disc closely parallels that of writing data. The computer instructs the disc drive to seek a specific drive assembly, track, head, and sector, to verify that operation, to enable the unit to read data, and to enable the unit to transmit the data it reads.

Internally, a read operation is much like a write operation. Flux transitions are converted by the drive assembly into pulses on the RDTA line. These pulses are processed by the read circuit and passed to the drive interface. When the proper identification field is located, the drive interface begins reading the data field. Data bits are decoded and moved into the shift register. The drive interface then sets the DRQ line high, signaling the processor to read the data byte. As each byte is accumulated by the drive interface, the processor reads the byte and stores it in RAM. After the entire record has been read and stored, and enables the bus interface to send data. The processor reads one byte of data from RAM and sends it to the bus interface, which transmits it on the HP-IB. The bus interface then informs the processor via the data bus to send each successive byte.

Self Test

The processor can be instructed to perform tests of various portions of the disc drive. The self tests can check RAM IC's ROM IC's, the bus interface IC, the drive interface IC, speed of drive motors, head-stepping mechanisms, disc formatting, and read verification. If the SELF TEST switch is pressed (on 82901-60002) or if the SELF TEST jumpers are momentarily shorted (on 82901-66503), the processor uses the setting of the address switch to select the test to perform. If a test involves writing onto a disc, the WRITE-ENABLE switch must be turned on (on 82901-60002) or the WRITE-ENABLE pins must be jumpered (on 82901-66503) to perform that part of the test; otherwise that part is skipped. If the two LOOP terminals on the controller PCA are connected, the test will repeat until the terminals are disconnected. Six LED's (in DS1 and DS2) on the controller PCA indicate the result of each test.

Chapter 3
Disassembly and Reassembly

Introduction

The following procedures describe the steps necessary to disassemble and reassemble HP 82900-Series Flexible Disc Drives in order to replace or repair components that are faulty:

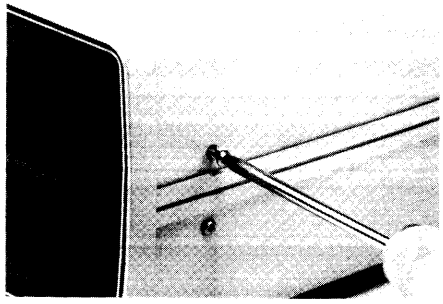
1. Removing the Cover.
2. Removing the Controller PCA.
3. Removing the Drive Assembly.
4. Replacing the Drive Motor and Belt.
5. Installing the Drive Assembly.
6. Replacing the Power Supply.
7. Replacing the I/O Cable Assembly.
8. Installing the Controller PCA.
9. Replacing the Power Cable Assembly.
10. Removing the Rear Panel Assembly.
11. Replacing the Fan.
12. Replacing the Transformer Assembly.
13. Installing the Rear Panel Assembly.
14. Installing the Cover.

CAUTION

ENSURE THAT ADEQUATE PRECAUTIONS ARE TAKEN REGARDING ELECTROSTATIC PROTECTION. WORK AT A BENCH SETUP THAT IS ELECTROSTATICALLY PROTECTED. OTHERWISE, COMPONENTS MAY BE DAMAGED.

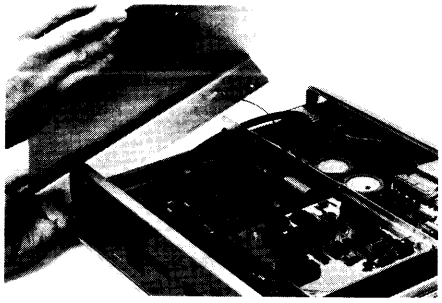
Removing the Cover

a. Remove the four screws holding the sides of the top cover.



b. Lift off the cover.

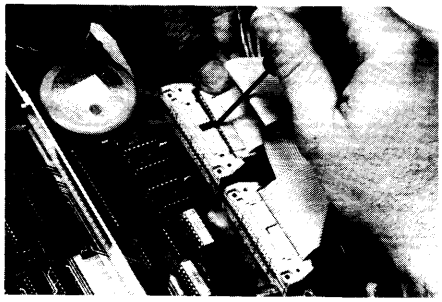
c. If necessary, disconnect the ground wire from the stud on the cover.



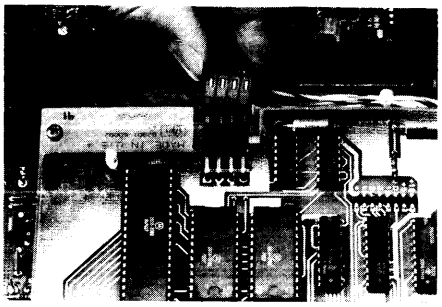
Removing the Controller PCA

After removing the cover:

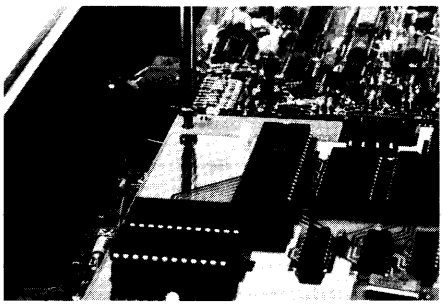
a. Disconnect the two I/O cable connectors from the PCA. Use a small, flat-bladed screwdriver to pry each one apart at the center slot of the connector.



b. Unplug the power connector from the side of the PCA.



c. Unscrew the two screws holding the front of the PCA.

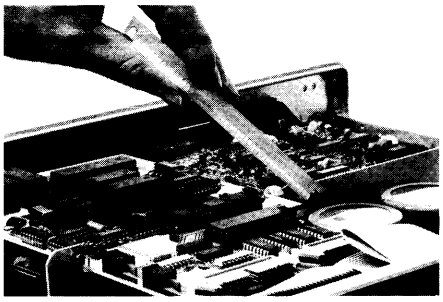


NOTE

Two plastic washers under the drive PCA are not retained when these screws are removed. Take precautions to prevent losing the washers.

d. Remove or swing aside the PCA clamp by loosening the two screws that hold the clamp.

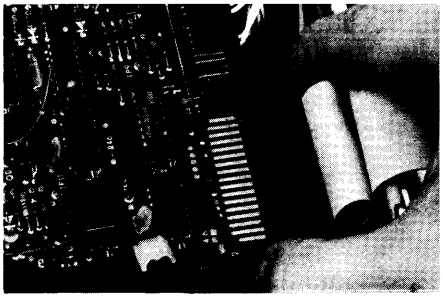
e. Lift out the PCA.



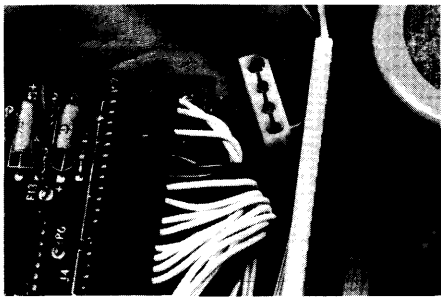
Removing the Drive Assembly

After removing the cover and the controller PCA (if one is mounted above the drive assembly):

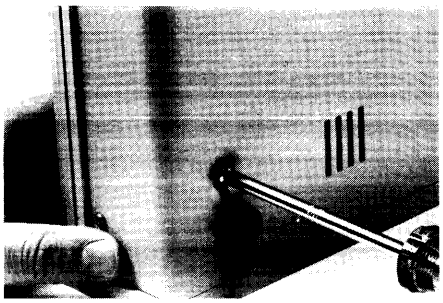
a. Unplug the I/O cable connector by sliding it off the rear of the drive PCA.



b. Unplug the power connector from the drive PCA.



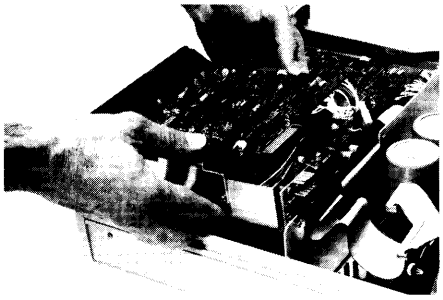
c. Remove the four screws holding the drive assembly to the bottom cover. Be sure the front latches are closed, then remove the screws with the unit standing on its front surface.



CAUTION

BE SURE THE FRONT LATCHES ARE CLOSED BEFORE STANDING THE UNIT ON ITS FRONT SURFACE. OTHERWISE, THE LATCH MECHANISMS MAY BE DAMAGED.

d. Lift the drive assembly back and out of the case after laying the unit flat.



Replacing Drive Motor and Belt

NOTE

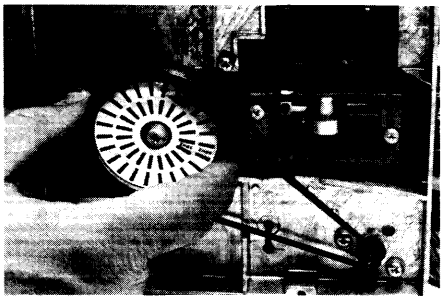
If only the belt is to be replaced, perform steps a and j only.

CAUTION

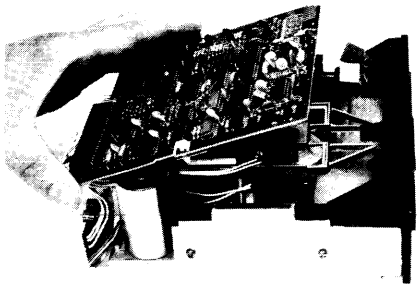
BE CAREFUL NOT TO PULL ON THE DRIVE BELT, POSSIBLY STRETCHING IT. IF THE BELT IS STRETCHED, IT MAY NOT PROVIDE THE NECESSARY TENSION TO OPERATE THE DRIVE ASSEMBLY RELIABLY.

After removing the cover, controller PCA (if one is mounted above the drive assembly), and drive assembly:

a. Remove the drive belt from the two pulleys by turning the large pulley and easing the belt off.
b. Unplug the motor connector (number 21) from the drive PCA.

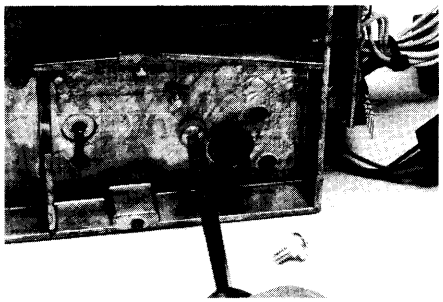


c. Remove the upper drive PCA. Do this by unplugging connectors 5 and 6, removing the two screws (if present) holding the front of the PCA, and then sliding the PCA back. When the PCA clears the retaining clips, swing the PCA upward, pivoting it at its back end.

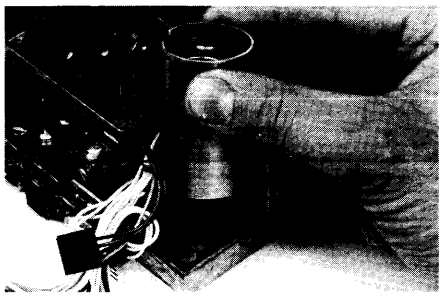


d. Remove the two screws and bushings holding the motor.

e. Lift out the motor. The clear spacer may also come out.



f. Install the motor and spacer in the frame. The wires should face toward the center-rear of the drive assembly.

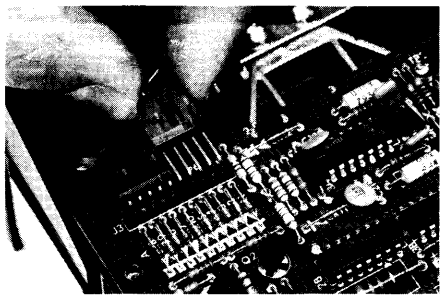


CAUTION

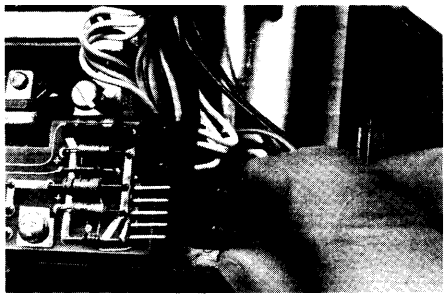
BE SURE THE SPACER AND BUSHINGS ARE INSTALLED WITH THE MOTOR. OTHERWISE, COMPONENTS MAY BE DAMAGED BY THE MOTOR SHORTING TO THE DRIVE ASSEMBLY FRAME.

g. Install the two screws and plastic bushings that hold the motor.

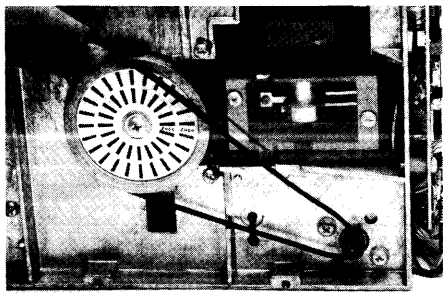
h. Install the upper drive PCA. Do this by lowering the PCA notches over the clips on the drive assembly, sliding the PCA forward, and installing the two screws through the PCA (if no controller mounts above it). Plug in connector 5 nearest to the edge of the PCA (with the stamped number facing up), and connector 6 next to it. (Be sure the two plastic washers are properly located under the front screw holes in the PCA.)



i. Plug in the motor connector (number 21) into the drive PCA, keeping the stamped number facing outward.



j. Install the drive belt over the motor pulley, then over the large pulley, turning it slowly. Keep the smooth, black surface of the belt toward the pulleys.

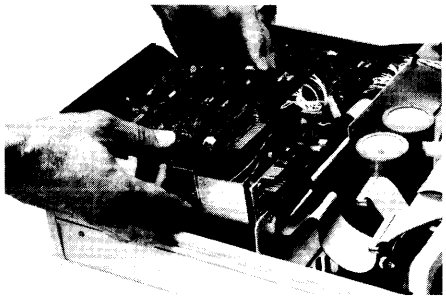


CAUTION

DO NOT STRETCH THE DRIVE BELT. IF IT IS STRETCHED, IT MAY NOT PROVIDE THE NECESSARY TENSION TO OPERATE THE DRIVE ASSEMBLY RELIABLY.

Installing the Drive Assembly

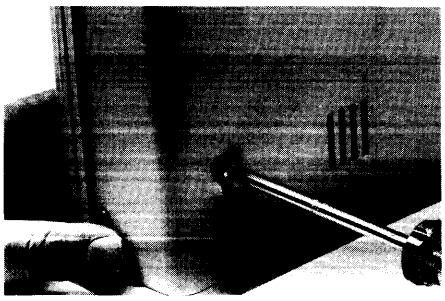
a. Place the drive assembly into position in the case.



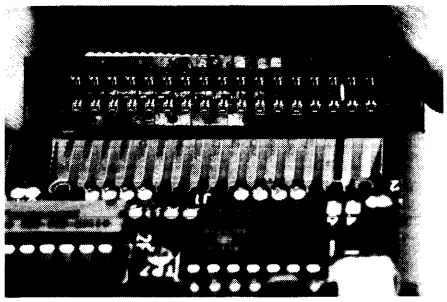
CAUTION

BE SURE THE FRONT LATCHES ON THE DRIVE ASSEMBLIES ARE CLOSED BEFORE STANDING THEM ON THEIR FRONT SURFACES. OTHERWISE, THE LATCH MECHANISMS MAY BE DAMAGED.

b. Install the four screws and lock washers through the bottom cover and into the drive assembly. Be sure that the raised part of the slot is flush with the panel surface.



c. Plug in the power connector, which is keyed for proper insertion.

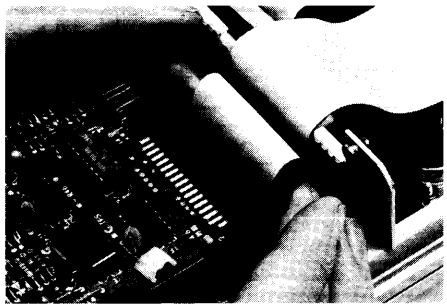


CAUTION

BE SURE THE I/O CABLE CONNECTOR HAS A KEY INSTALLED BETWEEN THE SECOND AND THIRD PAIRS OF CONTACTS FROM THE RED EDGE--BUT ONLY IF THE DRIVE PCA HAS A CORRESPONDING NOTCH. OTHERWISE, THE CONNECTOR MAY BE MISALIGNED AND COMPONENTS DAMAGED.

d. Check the I/O cable connector to be sure it is properly keyed according to the drive PCA contacts. Use a key in the connector if, and only if, thePCA is notched.

e. Install the I/O cable connector to the drive PCA, with the cable's red edge facing away from the power connector.



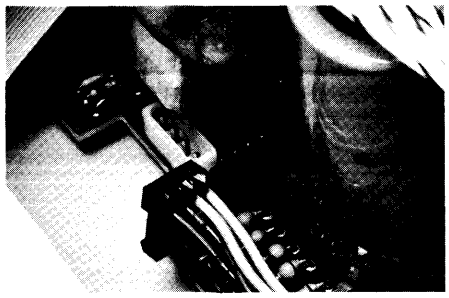
CAUTION

BE SURE THE I/O CABLE IS CONNECTED WITH ITS RED EDGE AWAY FROM THE POWER CONNECTOR ON THE DRIVE ASSEMBLY. OTHERWISE, COMPONENTS MAY BE DAMAGED.

Replacing the Power Supply

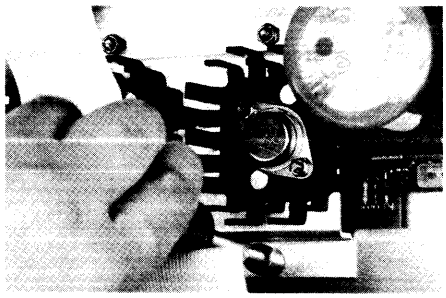
After removing the cover and controller PCA (if present):

a. Unplug the two connectors from the power supply. (One connector is for the transformer wires; the other connector is for the power cable.)

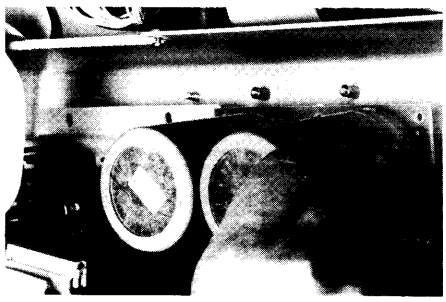


b. Remove the five screws holding the capacitor end of the power supply to the bottom cover.

c. Remove the four locknuts holding the metal power-supply bracket to the bottom cover.
d. Lift the power supply out of the case.



e. Place the power supply into the case, locating the metal bracket on the four studs.
f. Install the five screws at the capacitor end of the power supply.
g. Install the four locknuts onto the studs.

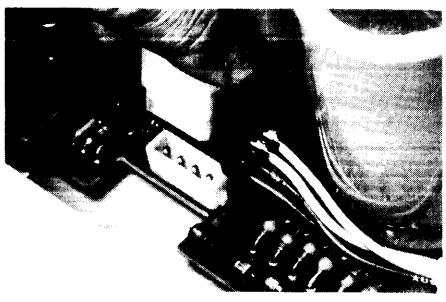


h. Plug in the transformer connector. Be sure that the four wires face toward the transformer so that the locking tab properly engages the connector.

CAUTION

INSTALL THE TRANSFORMER CONNECTOR SO THAT ITS WIRES FACE TOWARD THE TRANSFORMER. IF THE CONNECTOR IS INSTALLED BACKWARDS, COMPONENTS MAY BE DAMAGED BY EXCESSIVE VOLTAGE.

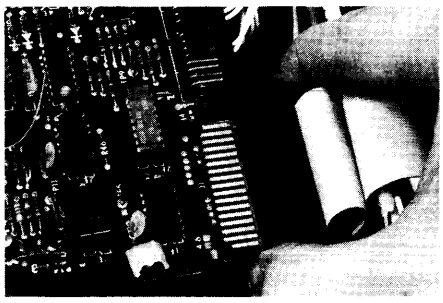
i. Plug in the power-cable connector, which is keyed for proper insertion.



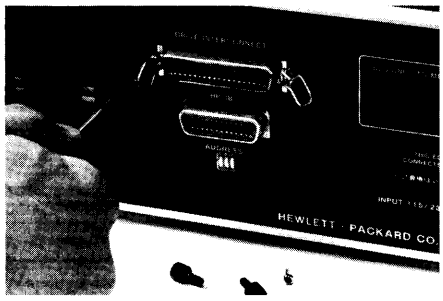
Replacing the I/O Cable Assembly

After removing the cover controller PCA (if present):

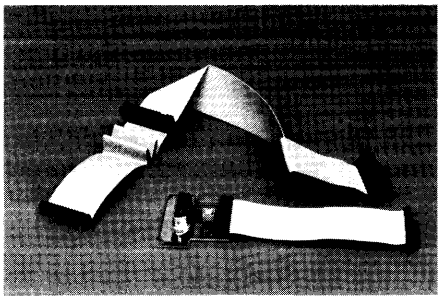
a. Unplug the I/O cable connectors from the drive assemblies.
b. For an add-on unit, release the I/O cable by removing the cable clamp on the divider panel.
c. Slip the cable out of the cable clip(s) on the divider panel.



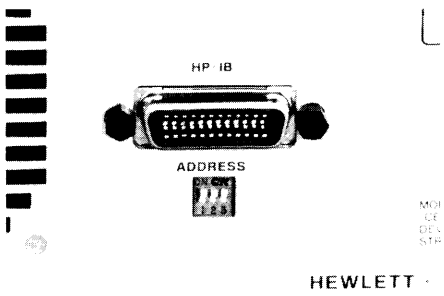
d. Unplug the fan connector in the fan cable.
e. Remove the four screws holding the I/O circuit board to the rear panel. On a master unit, the two lower screws are hex stand-off screws; use a 9/32-inch nut driver. On an add-on unit, the two lower screws hold a cover plate.
f. Lift out the I/O cable assembly.



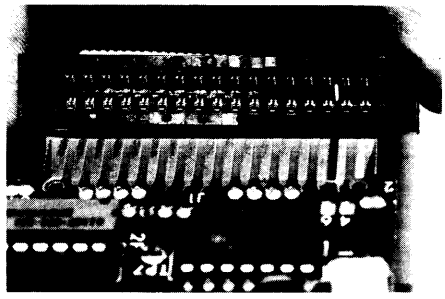
g. Form the I/O cable assembly so that it will properly fit into the case. Use the old cable as a guide.
h. Place the I/O assembly into the case, locating the receptacle(s) in the rear panel opening(s). The lower edge of the board slips between the fan cable and the rear panel.



i. Install the four screws that hold the circuit board in place. On a master unit, the lower receptacle is held by two hex standoff-screws. On an add-on unit, install the cover plate using the two lower screws (next photo).



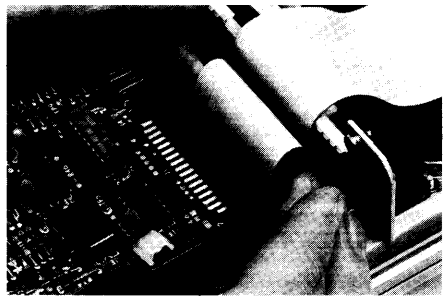
j. Check each I/O cable connector to be sure it is properly keyed according to the drive PCA contacts. Use a key in a connector if, and only if, the corresponding PCA is notched.



CAUTION

BE SURE EACH I/O CABLE CONNECTOR HAS A KEY INSTALLED BETWEEN THE SECOND AND THIRD PAIRS OF CONTACTS FROM THE RED EDGE--BUT ONLY IF THAT DRIVE PCA HAS A CORRESPONDING NOTCH. OTHERWISE, THE CONNECTOR MAY BE MISALIGNED AND COMPONENTS DAMAGED.

k. Install the drive I/O connector(s) onto the drive PCA(s). Be sure the red edge of the I/O cable faces away from the power-cable connector on each drive assembly.



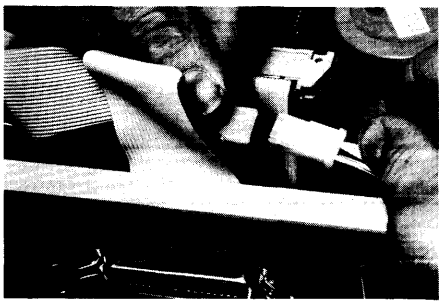
CAUTION

BE SURE THAT THE RED EDGE OF THE I/O CABLE FACES AWAY FROM THE POWER-CABLE CONNECTOR ON THE DRIVE ASSEMBLY. IF THE CONNECTOR IS INSTALLED UP-SIDE-DOWN, COMPONENTS MAY BE DAMAGED.

l. Slip the cable into the cable clip(s) on the divider panel.

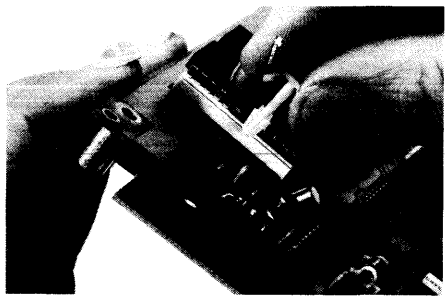
m. For an add-on unit, secure the cable clamp on the divider panel. Allow some slack in the cable at the drive assembly.

n. Plug in the fan connector, which is keyed for proper insertion. The fan cable should be below the upper I/O cable.

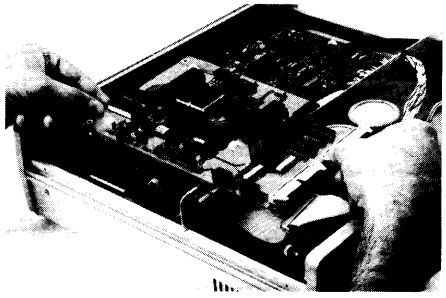


Installing the Controller PCA

a. Check the shield to be sure it is securely held to the underside of the controller PCA by the three buttons.

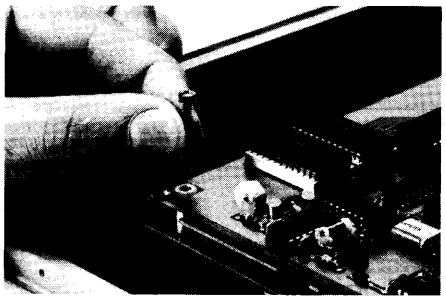


b. Place the controller PCA on top of the (right-hand) drive assembly. The two standoffs should be over the screw holes in the drive PCA. Be sure the insulator is properly installed on the divider panel.

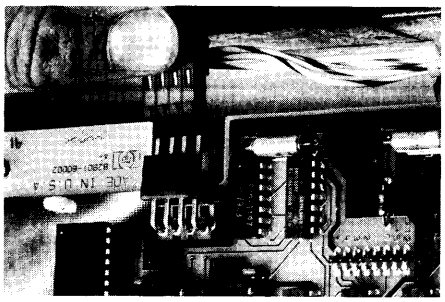


c. Install the two screws at the front of the controller PCA. (Be sure the two plastic washer are properly located under front screw holes in the drive PCA.)

d. Fasten the clamp over the PCA. Be sure the insulator is properly installed on the clamp.



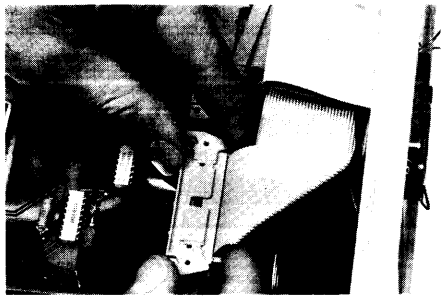
e. Connect the power connector to the side of the controller PCA. Be sure the wires from the connector face downward so that the locking tab properly engages the connector.



CAUTION

INSTALL THE POWER CONNECTOR SO THAT THE WIRES FACE DOWNWARD. OTHERWISE, COMPONENTS MAY BE DAMAGED BY EXCESSIVE VOLTAGE.

f. Connect the two I/O connectors to the controller PCA. The red edges of the cables should face away from each other at the connectors.



CAUTION

BE SURE THAT THE RED EDGES OF THE TWO I/O CABLES FACE AWAY FROM EACH OTHER AT THE CONTROLLER CONNECTORS. IF THE CONNECTORS ARE INSTALLED WRONG, COMPONENTS MAY BE DAMAGED.

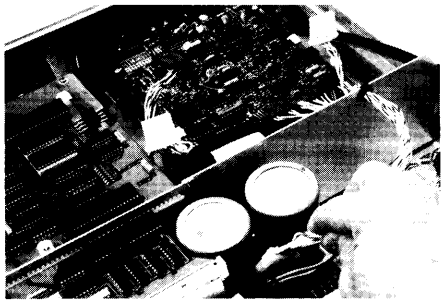
Replacing the Power Cable Assembly

After removing the top cover:

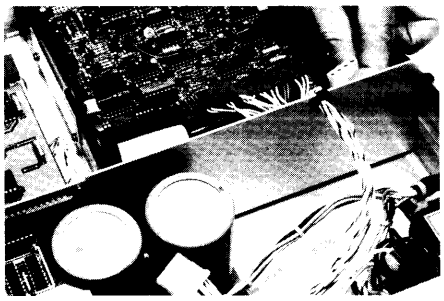
a. Unplug the connectors from the power supply, drive assemblies, and controller PCA (if present).

b. Remove the cable assembly by slipping the grommet from the divider panel.

c. Place the cable assembly in the unit, slipping the grommet into the slot in the divider panel.



e. Plug in the power-cable connectors. The power-supply and drive assembly connectors are keyed for proper insertion. The controller power connector (if present) must be installed with the wires facing downward.



CAUTION

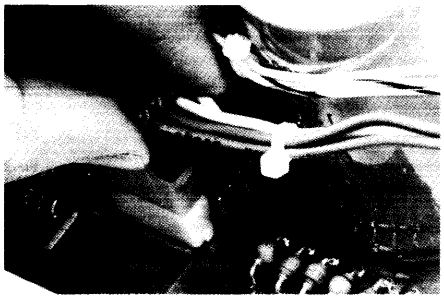
INSTALL THE CONTROLLER POWER CONNECTOR SO THAT THE WIRES FACE DOWNWARD. OTHERWISE, COMPONENTS MAY BE DAMAGED BY EXCESSIVE VOLTAGE.

Removing the Rear Panel Assembly

After removing the cover:

a. Unplug the transformer connector from the power supply assembly.

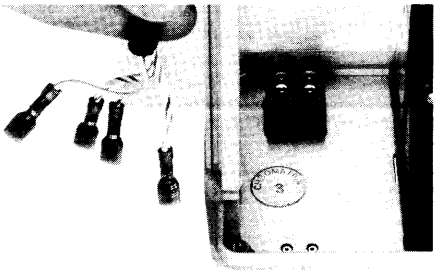
b. If necessary, remove the four screws holding the I/O circuit board to the rear panel. On a master unit, the two lower screws are hex standoff-screws; use a 9/32-inch nut driver. On an add-on unit, the lower screws hold a cover plate.



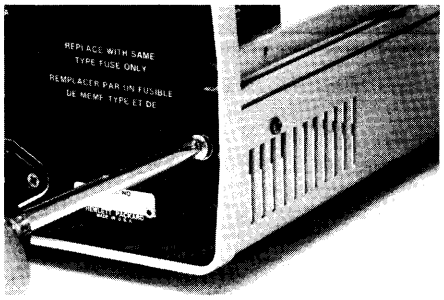
c. Unplug the four wires at the ON-OFF switch and slide them out the side of the divider panel.

d. If necessary, disconnect the ground wire from the stud on the bottom cover.

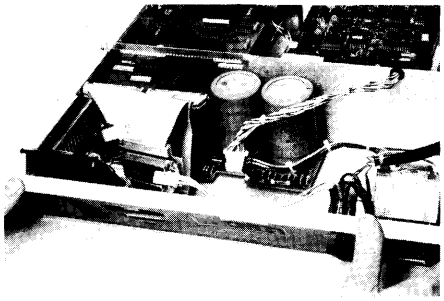
e. Unplug the fan connector in the fan cable.



f. Remove the four screws holding the rear panel to the side rails.



g. Pull off the rear panel assembly.

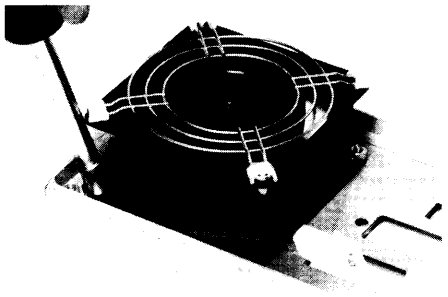


Replacing the Fan

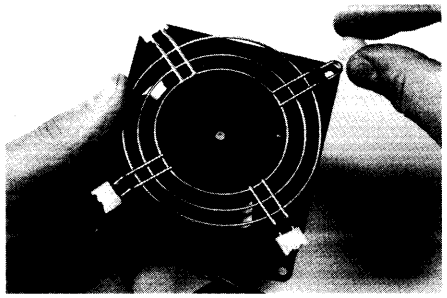
After removing the cover and rear panel:

a. Remove the two locknuts holding the fan to the rear panel. Use either a 1/4-inch nut driver or a 1/4-inch combination wrench (part number 8720-0014).

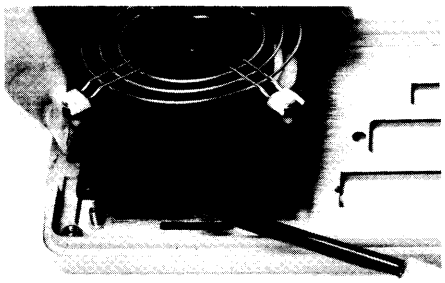
b. Remove the fan.



c. Check the grille to be sure it is held to the fan by four buttons. It should be installed next to the movable fan blade. (This only applies to older units.)



e. Install the fan on the two studs on the rear panel. The fan should be placed so that the wires are against the top of the panel.



CAUTION

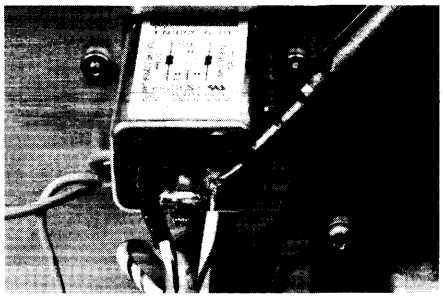
BE SURE THE FAN IS INSTALLED WITH ITS WIRES AGAINST THE REAR PANEL. OTHERWISE, COMPONENTS MAY BE DAMAGED BY IMPROPER COOLING CAUSED BY REVERSE AIR FLOW.

f. Install the two locknuts on the studs.

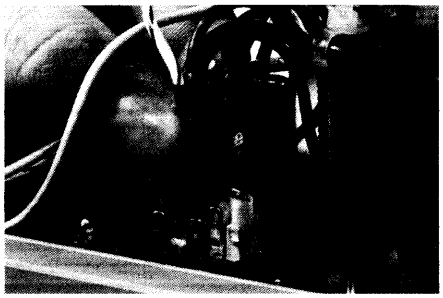
Replacing the Transformer Assembly

After removing the cover and rear panel:

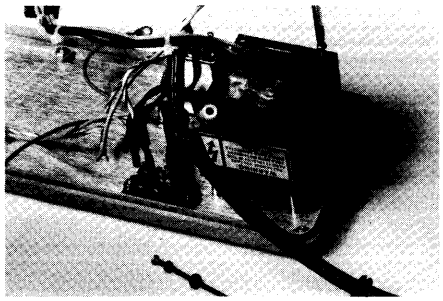
a. Unsolder the white/gray wire from the line filter after removing the heat-shrink tubing.
b. Unsolder the white/brown/gray wire from the fuseholder after removing the heat-shrink tubing.



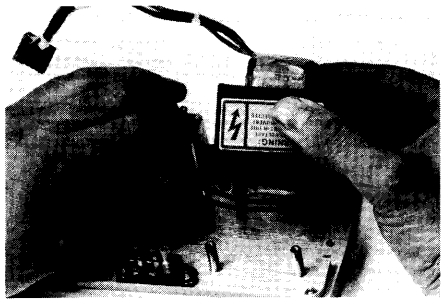
c. Unplug the four connectors from the line-voltage switch.
d. On a dual-drive unit, remove the nut that holds the mounting cable tie at the top center of the rear panel.



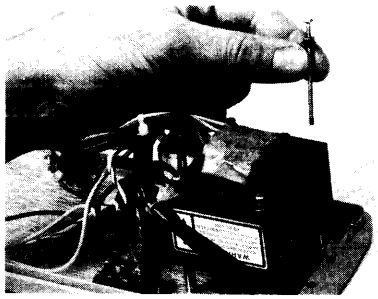
e. Remove four screws holding the transformer to the rear panel.
f. Remove the transformer assembly, cutting cable ties as needed.



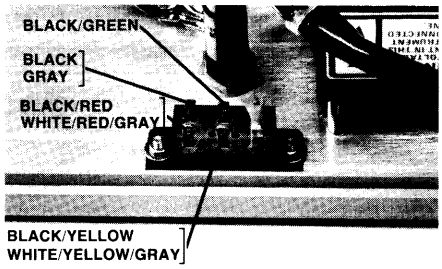
g. Place the new transformer assembly on the four posts on the rear panel. The yellow and brown secondary wires should face toward the fan. The black and black/yellow wires should cross between the transformer and rear panel between the posts.



h. Install the four screws and washers to hold the transformer. The screw closest to the line-voltage switch should also hold the cable clamp for the ON-OFF switch wires.



i. Connect the four connectors to the line-voltage switch, being sure to observe the indicated color coding.



CAUTION

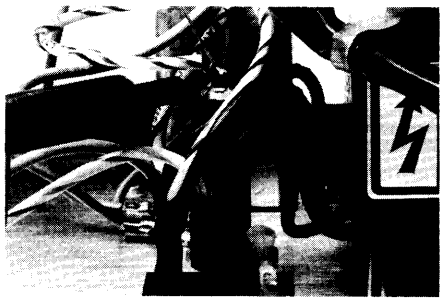
BE SURE TO FOLLOW THE INDICATED COLOR CODING AT THE LINE-VOLTAGE SWITCH. OTHERWISE, COMPONENTS MAY BE DAMAGED BY EXCESSIVE VOLTAGE.

j. On a master unit, install a mounting cable tie on the top center stud of the rear panel to hold the fan cable.

k. Solder the white/brown/gray wire to the side terminal of the fuseholder.

l. Install heat-shrink tubing over the fuseholder.

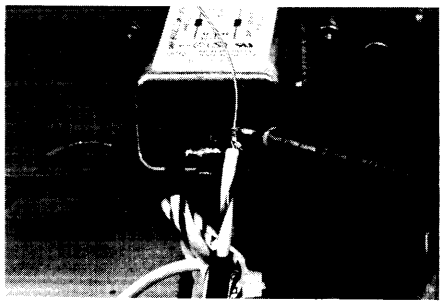
m. Slip a length of heat-shrink tubing over the end of the white/gray wire.



n. Solder the white/gray wire to the line-filter terminal next to the transformer.

o. Install the heat-shrink tubing over the line-filter terminal.

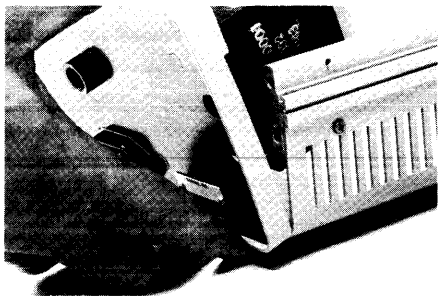
p. Install any needed cable ties.



Installing the Rear Panel Assembly

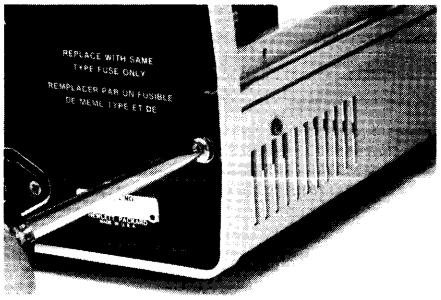
a. If the rear panel has been replaced, prepare a safety-approval label and install it on the new panel. Prepare the label by punching out the label to match the markings on the old panel.

b. Place the rear panel assembly into the back opening of the unit. The lip on the panel should fit inside the bottom cover.

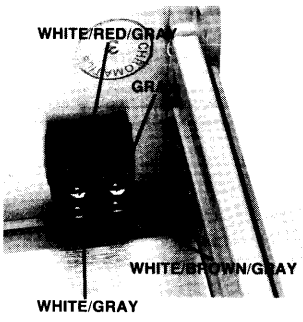


c. Install the four screws and lockwashers that hold the panel to the side rails. The side rails may have to be pressed inward slightly.

d. Check the ground wire to be sure it is fastened to the bottom cover with a locknut.



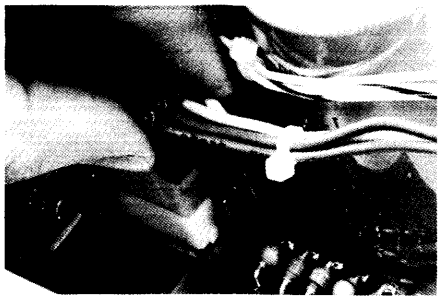
e. Connect the four wires to the ON-OFF switch. Be sure the wires are connected as shown. Slide the grommet into the slot in the divider panel.



CAUTION

BE SURE TO FOLLOW THE INDICATED COLOR CODING WHEN CONNECTING THE WIRES TO THE ON-OFF SWITCH. OTHERWISE, COMPONENTS MAY BE DAMAGED BY A SHORT CIRCUIT.

f. Connect the transformer connector to the power supply assembly. Be sure that the four wires face toward the transformer so that the locking tab properly engages the connector.



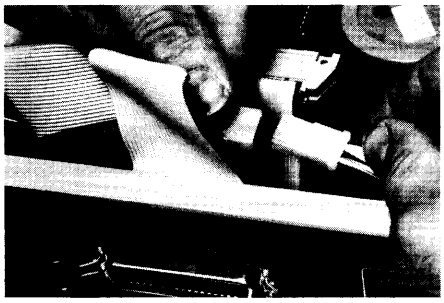
CAUTION

INSTALL THE TRANSFORMER CONNECTOR SO THAT ITS WIRES FACE TOWARD THE TRANSFORMER. IF THE CONNECTOR IS INSTALLED BACKWARDS, COMPONENTS MAY BE DAMAGED BY EXCESSIVE VOLTAGE.

g. Install the four screws that hold the I/O circuit board in place. On a master unit, the lower connector is held by two hex standoff-screws. On an add-on unit, install the cover plate using the two lower screws.

h. Plug in the fan connector, which is keyed for proper insertion. The fan cable should be below the upper I/O cable.

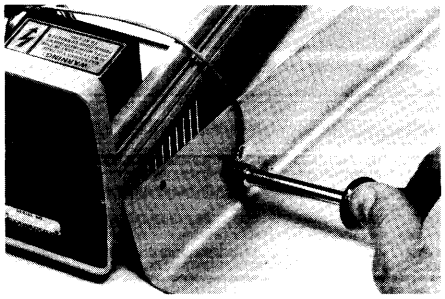
i. Check the I/O cable connectors at the controller PCA (if present) to be sure they are connected.



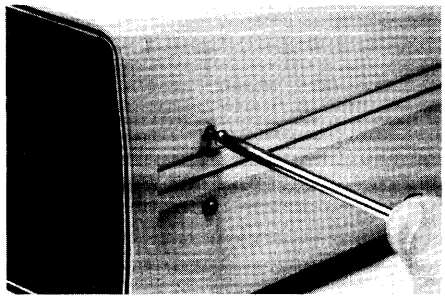
Installing the Cover

a. Check the ground wire to be sure it is fastened to the top cover with a locknut.

b. Place the cover on the unit.



c. Install the four screws that hold the cover to the side rails. Press down on the cover to be sure it seats in the grooves in the side rails.



Chapter 4
Troubleshooting and Testing

Introduction

This section contains the procedures you should follow to isolate the cause of a problem in an HP 82900-Series Flexible Disc Drive. The same procedures are used to test a disc drive. Tools that facilitate service are listed in Table 4-1.

CAUTION

ENSURE THAT ADEQUATE PRECAUTIONS ARE TAKEN REGARDING ELECTROSTATIC PROTECTION. WORK AT A BENCH SETUP THAT IS ELECTROSTATICALLY PROTECTED. OTHERWISE, COMPONENTS MAY BE DAMAGED.

Table 4-1. Recommended Tools

HP Part/Model Number	Description
0470-0722	Adhesive, general (for nameplate)
0960-0062	Continuity Tester
9164-0129	Flexible Disc, package of 10
HP 5315A	Frequency Counter, capable of measuring periods of 200 ms.
HP 3469B	Multimeter
8720-0001	Nut Driver, 3/16-inch
8720-0002	Nut Driver, 1/4-inch
8710-0797	Nut Driver, 9/32-inch
8720-0003	Nut Driver, 5/16-inch
HP 1220A*	Oscilloscope
8710-1107	Pliers, long-nosed
8710-0899	Screwdriver, 71 Posidriv
8710-0900	Screwdriver, 72 Posidriv
8730-0008	Screwdriver, flat-bladed
8690-0129	Soldering Iron
8690-0130	Soldering Iron Stand

* Or equivalent.

Always begin troubleshooting or testing a disc drive using the procedures described in paragraph 4-17. The troubleshooting and testing procedures make use of the self tests that are built into master units. A computer and HP-IB module are used to test the interface circuit in a master unit and to exercise all disc drives.

The following techniques should be used during the troubleshooting procedure when needed. They are described below.

a. Connecting the Disc Drives.
b. Setting the Address Switch.
c. Substituting a Controller PCA.
d. Replacing Socketed IC's.

Connecting the Disc Drives

CAUTION

ALWAYS TURN OFF THE COMPUTER AND ALL PERIPHERALS BEFORE INSTALLING OR REMOVING MODULES OR CABLES. OTHERWISE, THE SYSTEM MAY BE DAMAGED.

To connect a master unit:

a. Turn off the computer and the disc drive.
b. Connect the HP-IB interface to the computer according to the installation instructions for the interface.
c. Insert the HP-IB connector into the HP-IB receptacle on the rear panel of the disc drive. Secure the connector with its two screws.

To connect an add-on unit:

a. turn off the computer and disc drives.
b. Insert one end of the interconnect cable into the DRIVE INTERCONNECT receptacle on the rear panel of the master unit. Secure the connector with the clips.
c. Insert the other end of the interconnect cable into the DRIVE INTERCONNECT receptacle on the rear panel of the add-on unit. Secure the connector with the clips.

Setting the Address Switch

The address switch on the rear panel of each master disc drive identifies that master unit to the HP-IB. The setting of the switch determines the address of the master unit:

Switch			Address
1	2	3	
ON	ON	ON	0
ON	ON	OFF	1
ON	OFF	ON	2
ON	OFF	OFF	3
OFF	ON	ON	4
OFF	ON	OFF	5
OFF	OFF	ON	6
OFF	OFF	OFF	7

For a rocker-type address switch, the depressed ends of the switches show the settings of the switches. To set a rocker-type switch, use a pointed object and press on the rocker at the desired end. That end of the rocker will snap in, indicating the new setting. (See Figure 4-1.)

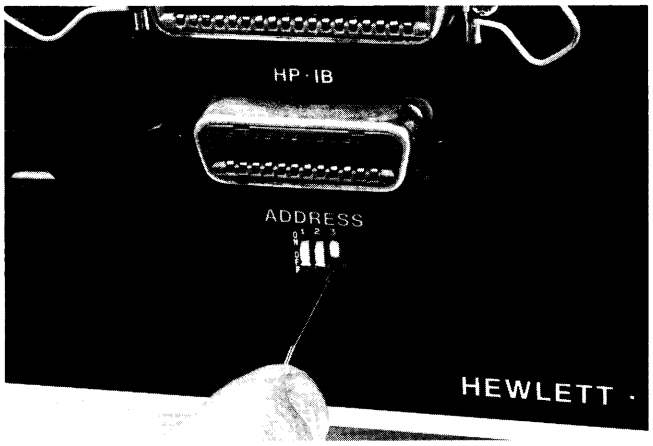


Figure 4-1. Setting the Address Switch

Substituting a Controller PCA

During troubleshooting, you may need to substitute a new controller PCA in order to isolate the faulty component or assembly. The following procedure allows a new PCA to be wired into a master unit without removing the original PCA. (See Figure 4-2.)

a. Turn off the disc drive.
b. Place a piece of insulating material over the controller PCA. The plastic bag in which the PCA's are packaged is suitable for this purpose.
c. Transfer the two I/O connectors from the original PCA to the new one.
d. Transfer the power connector from the original PCA to the new one.

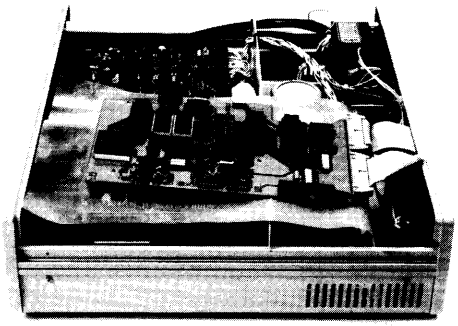


Figure 4-2. Substituting a Controller PCA

Replace Socketed IC's 4-14. The socketed IC's are held tightly in their sockets and cannot easily be removed with your fingers. Unless you are careful, you could bend the pins of an IC while inserting it in a socket. The drive interface IC (U10) is especially susceptible to mechanical damage—use extreme care.

To remove an IC from its socket (see figure 4-3):

a. Insert a small, flat-bladed screwdriver between one end of the IC and the socket.

CAUTION

BE SURE THE SCREWDRIVER IS NOT INSERTED MORE THAN 2 1/2 MILLIMETERS (3/32 INCH) UNDER THE IC BEFORE YOU PRY OUT THE IC. OTHERWISE WITH CERTAIN SOCKETS, THE SCREWDRIVER COULD DAMAGE TRACES ON THE PC BOARD.

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b. Pry the end of the IC up by raising the handle of the screwdriver.

c. Raise the other end of the IC either by prying it with the screwdriver, if possible, or by pushing the first end down so that the other end rocks up.

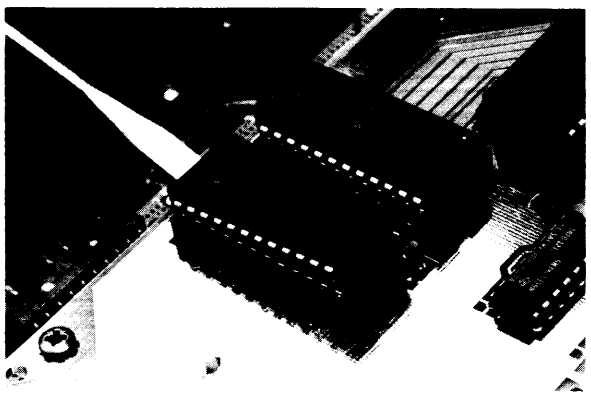


Figure 4-3. Removing an IC from Its Socket

To insert an IC into its socket:

a. Position the IC on the socket so that the semicircle in the top end of the IC is pointing in the same direction as the semicircle in the socket.

b. Press the IC down evenly along both sides until it is secured in the socket. When the IC is properly inserted, both of its sides should be the same height above the socket.

c. Check that all of the pins on the IC are in the socket.

Initial Preparation

Perform the following steps before troubleshooting a disc drive. They may indicate the nature or severity of the problem. If you are checking an add-on unit, you must also use a master unit.

a. Determine the customer's problem, if possible. This information can be helpful in evaluating test results, although you should still follow the recommended procedures. In particular, if the customer was using a certain flexible disc or setup when the problem occurred, make an effort to duplicate that condition.

b. Disconnect the power cord.

WARNING

ALWAYS DISCONNECT THE DISC DRIVE FROM ANY POWER SOURCE BEFORE ADJUSTING THE LINE-VOLTAGE SWITCH OR CHANGING FUSES. FAILURE TO DO SO COULD RESULT IN ELECTRICAL SHOCK OR DAMAGE TO THE UNIT.

c. Check the line-voltage switch to be sure that it is set to the proper voltage.

d. Check the fuse to be sure that it is good and has the proper rating. Use a 1A fuse for 115V operation; use a T 500 mA (0.5A time-delay) fuse for 230V operation.

e. Remove the top cover. If the disc drive being tested is an add-on unit, also remove the cover on the master unit.

f. Visually inspect the unit for physical damage and loose connections.

CAUTION

ALWAYS TURN OFF THE COMPUTER AND ANY CONNECTED PERIPHERALS BEFORE INSTALLING OR REMOVING MODULES OR CABLES. IF THIS IS NOT DONE, THE SYSTEM MAY BE DAMAGED.

g. Connect the disc drive to a computer with an HP-IB cable (if it is a master) or to a master unit with an interconnect cable (if it is an add-on).

h. Connect the power cord.

i. Turn on the disc drive(s). For proper operation on many computers, peripherals (such as disc drives) must be turned on before the computer.

If the DRIVE lights blink momentarily, the controller in the master unit is operating. Continue.

For any other occurrence (such as no response or flashing DRIVE lights on all drive assemblies), immediately perform the test sequence (paragraph 4-19).

j. Turn on the computer.
k. Insert a recorded disc into the slot the faulty drive assembly.
l. Execute a simple read command, specifying the drive assembly containing the disc. (For an HP 85 with a Mass Storage ROM, use the CAT ":Dxyz" command, where x is the select code of the HP-IB module used with the disc drives, 3 through 10; y is the address setting of the master unit, 0 through 7; and z is the DRIVE number, 0 through 3.)

If the proper response occurs (such as a normal catalog), perform the test sequence (paragraph 4-19). If a disc-related error is displayed by the computer, the disc medium may be the cause of the customer's problem. Try the command again using another disc. If this corrects the problem, perform the test sequence (paragraph 4-19) to verify proper operation; otherwise, use the test sequence to determine the cause of the problem. For any other response, try the command again using another disc in the same or a different drive assembly (in the same or another unit), if available. This might suggest whether the drive assembly or disc medium is faulty. Perform the test sequence (paragraph 4-19) to determine the cause of the problem.

Test Sequence

Perform the following steps to determine and repair the causes of improper operation of a disc drive and to test a disc drive. For reference information about part locations and numbers, use Figure 5-1, 5-2, and 6-1 through 6-4 and Tables 5-1 and 5-2.

a. Check the WRITE ENABLE switch on the controller (82901-60002) PCA in the master unit. Be sure it is turned off (switch lever parallel to SELF TEST lever).

   Check the WRITE ENABLE and SELF TEST jumpers (82901-66503) to be sure they are removed.

b. Check the jumpers on the drive PCA's to be sure they are set properly. (See Figure 4-4.) The jumpers should be placed in the socket as shown by the O's below. (A jumper in position 1 will not affect operation.) Turn off the disc drive before changing the jumpers.

Controller PCA 82901-60002

Drive Number	Jumper Locations (1 2 3 4 5 6 7 8)
0	- 0 - - - - - -
1	- - 0 - - - - -
2	- - - 0 - - - -
3	- - - - 0 - - -

c. Check jumpers W1 and W2 on the controller PCA in the master unit to be sure they are installed properly. The jumpers should be placed in socket XW1 in position 1 and 2 (toward the I/O connector end of the PCA).

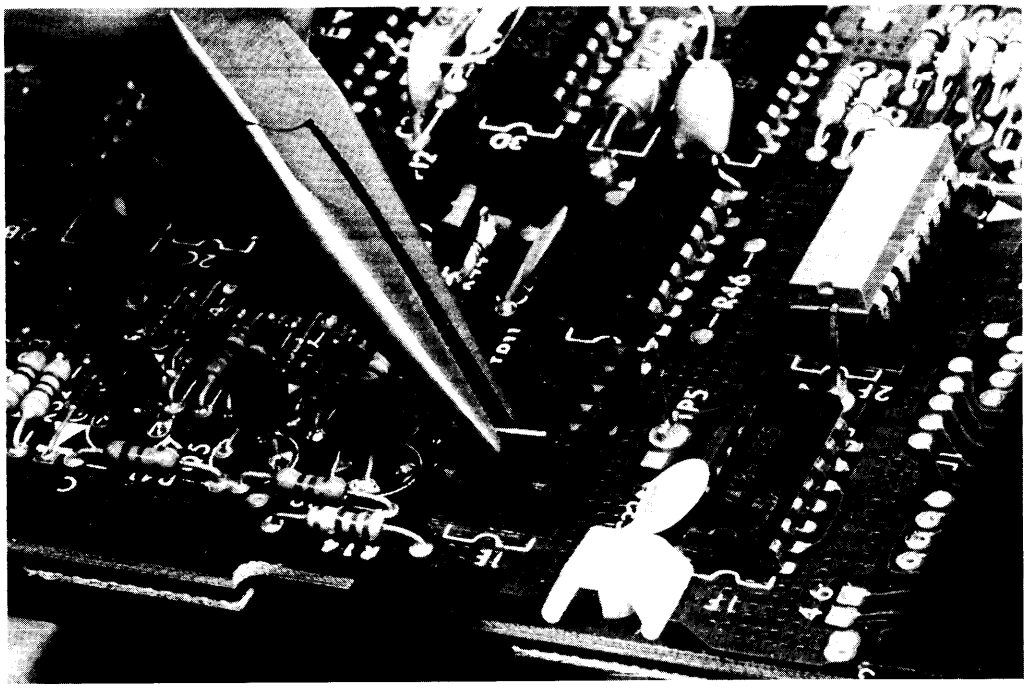


Figure 4-4. Checking Jumpers on the Drive PCA

d. Measure the +5V and +12V supply voltages in the unit being checked. For a master unit, measure them at the controller PCA power connector J3 pin 4 (+5V) and pin 1 (+12V), using LOOP terminal E2 for ground; for an add-on unit, measure them at the power supply connector J2 pins 4 to 3 (+5V) and pins 1 to 3 (+12V). (For a master unit, the +5V and +12V LED's should be on.)

If the two voltages are within 4.75 to 5.25 Vdc and 11.4 to 12.6 Vdc, the power supply is working properly. Continue.

If either voltage is outside its range, repair the power supply using the procedure in Table 4-2. For a master unit, then check the read oscillator frequency (paragraph 4-26). Then repeat the test sequence.

Table 4-2. Troubleshooting the Power Supply

Use this table to find the cause of improper power supply voltages. If only one supply voltage is bad, make only those measurements that apply to that voltage. If you make repairs in any step, recheck the supply voltage to see if they are correct. (Figure 6-3 shows the component location diagram.)

CAUTION

HAZARDOUS VOLTAGE IS PRESENT NEAR THE TRANSFORMER AND POWER RECEPTACLE WHENEVER THE POWER CORD IS PLUGGED IN. UNPLUG THE CORD BEFORE CHANGING COMPONENTS IN THIS AREA.

Step	Specification	Action
Disconnect the power cable at the power supply.		
Measure the +5V (J2 4 to pin 3) and +12V (J2 pin 1 to pin 3) supplies.	4.75 to 5.25 Vdc 11.4 to 12.6 Vdc	If either voltage is zero, check continuity of power supply fuses (f1 for +5V, F2 for +12V). If within range, repeat this step after connecting the power cable and each assembly, one at a time. Replace the assembly that pulls the voltage down.
Measure the regulator voltages (for +5V: from J2 pin 4 to R3 lead toward fan; for +12V: from J2 pin 1 to R2 lead away from PC edge).	1.20 to 1.30 Vdc	If outside range, replace that regulator (U1 for +5V; U2 for +12V)
Unplug power cord.		
Check the forward and reverse continuity of the 10 diodes (CR1 to CR10).		Replace any bad diodes.
Unplug transformer from power supply.		
Measure the ac line voltage (VL) at the outlet.	90 to 127 Vac OR 200 to 254 Vac	
Connect the power cord and turn on the unit.		
Measure ac output voltages of the transformer (pins 3 to 4 and pins 1 to 2 of the transformer plug).	Pins 3-4 (yellow wires): (VL/115)x12.7 Vac ±.6V (VL/230)x12.7 Vac ±.6V Pins 1-2 (brown wires): (VL/115)x22.9 Vac ±1.0V (VL/230)x12.9 Vac ±1.0V	If both voltages are within range, replace power supply assembly. If either voltage is outside range, replace transformer assembly.
For a master unit, check the read oscillator frequency. (82901-60002 only)	7.95 to 8.05 Mhz	If outside range, adjust inductor L1 on controller PCA.

e. Insert spare discs into each drive assembly. Data will be recorded on these discs during the test that follow.

f. Perform the self tests described in Table 4-3, making any repairs that are indicated. If you are not testing a master unit, skip tests 1 through 4.

Table 4-3. Self Tests

This table lists the information needed to perform the self tests built into the disc drives. An add-on unit must be connected to a master unit in order to test the add-on unit.

Insert a spare disc into each drive assembly. For each test, do the following:

a. Set the address switch on the master unit to the setting shown.
b. Press the SELF TEST switch or jumper the SELF TEST pins.
c. Take any action indicated for the final LED status of that test. The light on a drive assembly turns on for 10 seconds if an error occurs while it is being tested. If action is needed, try the suggestions in the order they are presented, then repeat all of the self tests.

Test	Address Switch Settings (2 3 4)	LED Status * 4 3 2 1 0	Comments/Action
1. RAM	up up up	o - - - - -	Test passed
		o - - - - o	(82901-69002) Replace RAM (U20 or U21) or processor (U15). (82901-66503) Replace RAM (U30 or U31) or processor (U33).
2. ROM	up up down	o - - - - -	Test passed.
		o - - - o -	(82901-69002) Replace ROM (U18 P/N 1818-1565 or U19 P/N 1818-1864). (82901-66503) Replace ROM (U38 P/N 1818-1835 or U39 P/N 1818-1834).
3. Bus Interface	up down up	o - - - - -	Test passed.
		o - - - o o	(82901-69002) Replace bus interface (U22 P/N 1820-2357). (82901-66503) Replace bus interface (U27 P/N 1820-2748).
4. Drive Interface	up down down	o - - - - -	Test passed.
		o - - o - -	(82901-69002)
		o - - o - -	Replace drive interface (U10) (82901-66503) Replace drive interface (U29)
5. Motor Speed	down up up	o - - - - -	Test passed.
		o - - o - o	Adjust motor speed. (This test requires enough time to test four drives, even if only one is present.)

6. Seek Track 0	down up down		Listen for stepper motor moving head in drive before LED status is displayed, time is allowed for testing four drives.
		o - - - - -	If the head moves, the drive passes the test. If the head does not move replace the controller PCA, drive assembly or I/O (power supply) assembly.
7. Format	down down up		Before starting this test, the WRITE ENABLE switch must be turned on or the WRITE ENABLE pins must be jumpered (for this test only) and a disc (not write protected) inserted into the drive.
		o - - - - -	Test passed.
		o - - o o o	Check conditions listed above, check oscillator freqency, then replace controller PCA or drive assembly.
8. Read Verify	down down down		Before starting this test, a formatted disc (preferably from the present system-previous-test) must be inserted into the drive.
		o - - - - -	Test passed.
		o - o - - -	Use different disc, check oscillator frequency, substitute controller PCA and/or drive interface (U10) or drive assembly or I/O (power supply) assembly.

g. If any repairs have been made during the self tests, repeat the self tests (Table 4-3) to verify operation.

h. Reset the computer system. This can be done by turning the computer off and on. (The HP 85 can be reset by pressing the RESET key.) For most computers, the disc drives must already be on when the computer is turned on or reset.

i. For each drive assembly being tested, execute a command that reads and writes data on the disc. (For the HP 85 with a Mass Storage ROM, use the INITIALIZE "NAME","":Dxyz" command, where x is the select code of the HP-IB module used with the disc drives, 3 through 10; y is the address setting of the master unit, 0 through 7; and z is the DRIVE number, 0 through 3. Execution time can be from 1 to 6 minutes.)

CAUTION

WHEN USING THE HP 85 OR HP 83, DO NOT USE THE SYNTAX "INITIALIZE":Dxyz". UNLIKE THE OTHER MASS STORAGE COMMANDS, INITIALIZE CANNOT BE ROUTED TO THE DRIVE UNLESS THE VOLUME LABEL IS INCLUDED BEFORE THE MSUS.

If the command is performed properly (and the self tests were passed) for each drive assembly in the unit, the unit is good.

If an error is displayed indicating a faulty disc, try the command again using another disc in the drive assembly.

Any other occurrence indicates faulty operation. Because most of the internal components have already been tested by the self tests, the most likely cause of improper operation is in the interface portion of the system. To help determine the cause, try

1. substituting a new HP-IB (only if all drive assemblies operate improperly),
2. substituting a new controller PCA and/or a new bus interface (U22),
3. replacing the I/O assembly in the master unit.

j. If repairs have been made, repeat the test sequence (paragraph 4-19) to verify proper operation

Adjusting the Drive-Motor Speed

You may use either of two methods to adjust the drive-motor speed: using a frequency counter or using the motor-speed self test. The frequency counter method is preferred; the self test method may be used if a counter is not available. To adjust an add-on, it must be connected to a master unit.

Adjusting the Read Oscillator (82901-69002 only)

The read oscillator on the controller PCA is adjusted at the factory and does not normally require further adjustment. However, the frequency should be checked and adjusted if needed in the following cases:

If the power supply or any of its components have been replaced in a master unit. (The oscillator frequency is affected by the power supply voltage.)

If errors repeatedly occur during read operations for drives in or connected to a particular master unit. To check and adjust the read oscillator:

a. Connect a frequency counter to the lead of R15 toward the front of the unit (away from the I/O connectors) on the controller PCA. For the ground connection, use LOOP terminal E2 (closest to the edge of the PCA).
b. Set the counter to measure frequencies of approximately 8 MHz.
c. Have the disc drive(s) in an idle condition (turned on but not performing any function). Only the 25, 212, and number 2 LED's should be on.
d. If necessary, adjust inductor L1 to obtain a frequency between 7.95 and 8.05 MHz.

Adjusting the Read Oscillator (82901-66503 only)

For controller PCA 82901-69503, connect frequency counter to U24, pin 12. Adjust trimpot VR1 for a frequency of 500 K Hz, ±1%.

Chapter 5
Replaceable Parts

Introduction

This chapter provides a complete replaceable parts list for the 82900 series flexible disc drives.

Reference designators are used in lieu of item numbers on printed circuit assemblies.

The check digit shown in the CD column is required when ordering a part from HP. Please include this number with your order.

The various 82900 series products are listed at the begining of the parts list. There is a useage code (shown in the Useage Code column) assigned to each of the 82900 series products. The Useage Code column shows how many, and on what product, the parts are used.

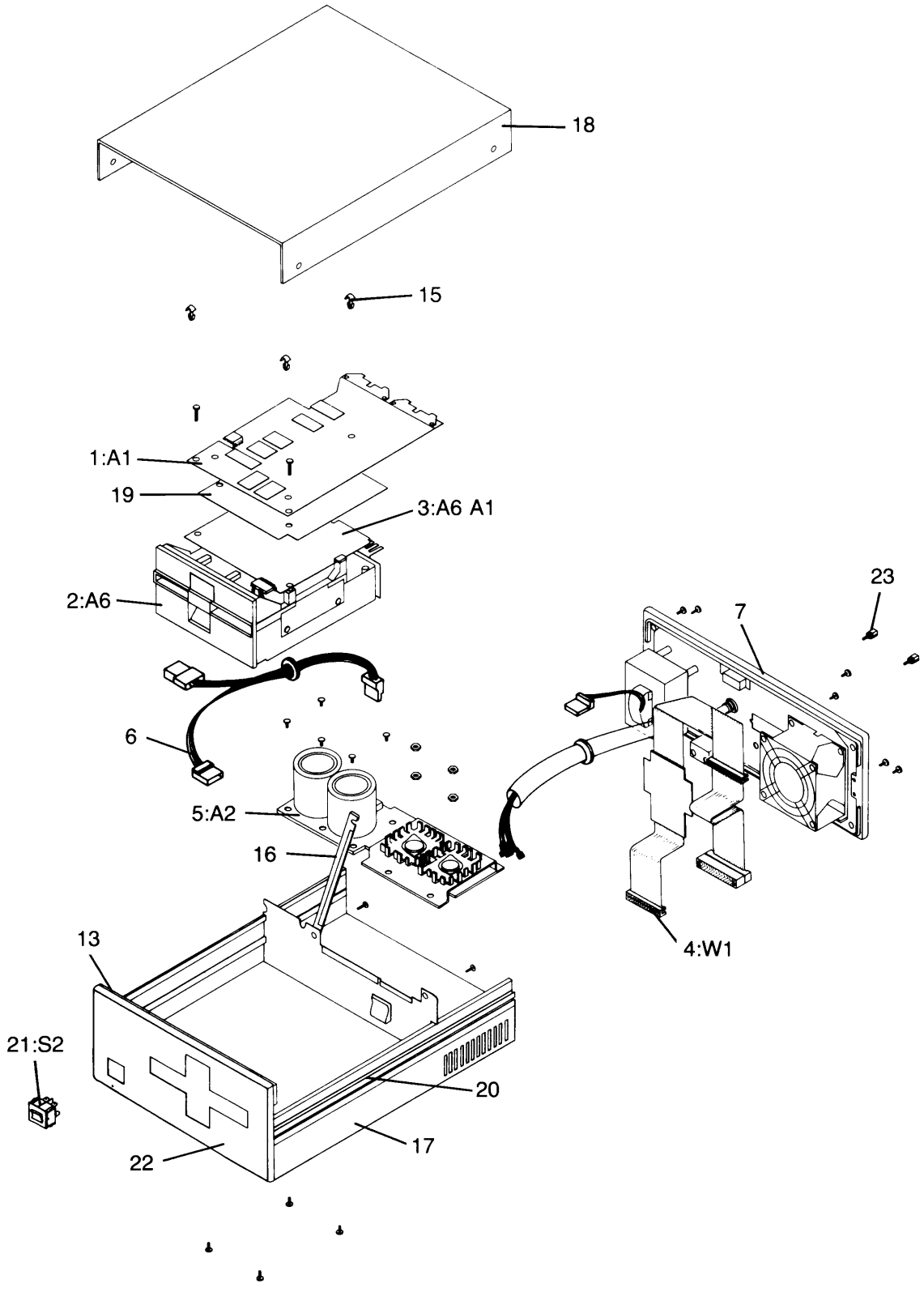


Figure 5-1. 82900 Exploded View

82900 Series Parts List

Item Number	Ref Des	Part Number	CD	TQ	Description	Useage Code
		82901M			Dual Disc Memory (Master)	A
		82902M			Single Disc Memory (Master)	B
		82901S			Dual Disc Memory (Slave)	C
		82902S			Single Disc Memory (Slave)	D
1	A1	82901-69002	9	1	Controller PCA	A,B
					OR	
1	A1	82901-69503	0	1	Controller PCA	A,B
2	A6	09130-69601	2	2	Drive Assembly	A,C
2	A6	09130-69601	2	1	Drive Assembly	B,D
		0950-0448	5	1	Belt, Drive	
		82901-60709	0	1	Motor, Drive	
3	A6A1	09130-66501	5	1	Drive Electronics PCA	
					OR	
3	A6A1	82901-60015	1	1	Drive Electronics PCA	
		82901-60030	0	1	Fuse Assembly (110-120Vac)	
	F1	2110-0001	8	1	Fuse, 1A	
					OR	
		82901-60031	1	1	Fuse Assembly (220-240Vac)	
	F1	2110-0621	8	1	Fuse, 500ma	
4	A4	82901-60905	8	1	Cable Assembly, I/O (Note 1)	A
					OR	
4	A4	82901-62536	5	1	Cable Assembly, I/O (Note 2)	A
4	A4	82901-60902	5	1	Cable Assembly, I/O (Note 3)	B
					OR	
4	A4	82901-62508	1	1	Cable Assembly, I/O (Note 4)	B
4	A4	82901-60906	9	1	Cable Assembly, I/O	C
4	A4	82901-60903	6	1	Cable Assembly, I/O	D
5	A2	82901-60908	1	1	Power Supply Assembly	
		2200-0521	8	7	Screw, 4-40 X .25	
		0590-0077	2	4	Nut, Locking	
6	W1	82901-60009	3	1	Cable Assembly, Power	A
6	W1	82901-60010	6	1	Cable Assembly, Power	C
6	W1	82901-60002	6	1	Cable Assembly, Power	B
6	W1	82901-60003	7	1	Cable Assembly, Power	D
7		82901-60038	8	1	Panel Assembly, Rear (Note 1)	A
7		82901-60005	9	1	Panel Assembly, Rear (Note 2)	A
7		82901-60009	3	1	Panel Assembly, Rear (Note 3)	B
7		82901-60001	5	1	Panel Assembly, Rear (Note 4)	B
8		2110-0610	5	1	Fuseholder body	
		2110-0569	3	1	Nut, Fuseholder	
		0905-0090	8	1	O-Ring	

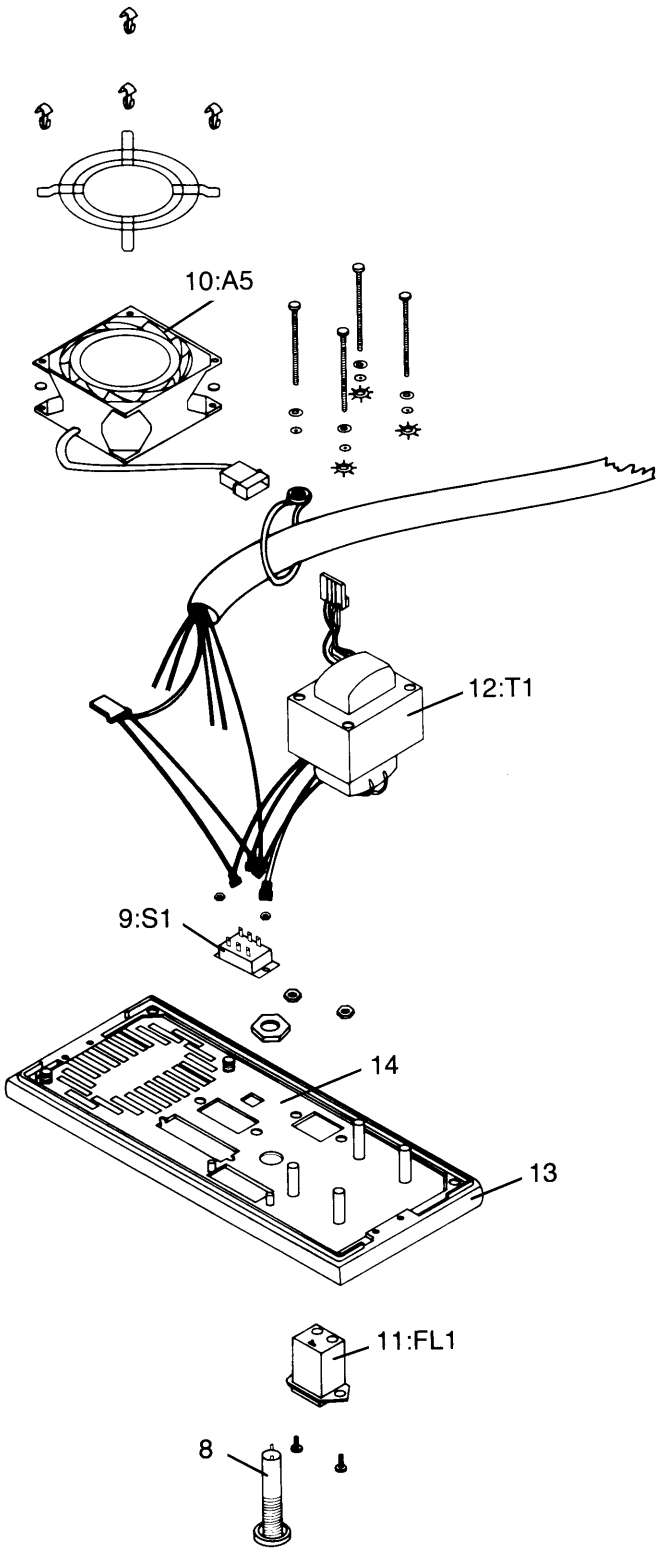


Figure 5-2. Rear Panel Assembly Exploded View

82900 Series Parts List (Continued)

Item Number	Ref Des	Part Number	CD	TQ	Description	Useage Code
9	S1	3101-2299	2	1	Switch, Slide	
10	A5	82901-60904	7	1	Fan Assembly	
11	FL1	9135-0038	0	1	Filter, Line	
		2260-0007	1	2	Nut, Line Filter	
		2200-0778	7	2	Screw, Line Filter	
12	T1	82901-60014	0	1	Transformer Assembly	A,C
12	T1	82901-60006	0	1	Transformer Assembly	B,D
		2200-0129	2	4	Screw, Transformer	
		2190-0411	2	3	Washer, #4, Locking	
		3050-0222	8	6	Washer, Flat	
		2190-0003	8	6	Washer, Split	
13		82901-20014	6	2	Casting	A,C
13		82902-20008	8	2	Casting	B,D
14		82901-00003	2	1	Panel, Rear (Note 1)	A,C
14		82901-00004	2	1	Panel, Rear (Note 2)	A,C
14		82902-00003	2	1	Panel, Rear (Note 3)	B,D
14		82902-00004	3	1	Panel, Rear (Note 4)	B,D
15		0510-0679	2	3	Button, Controller Shield	
16		1600-0951	5	1	Clamp, Controller	A,B
17		7101-0532	6	1	Cover, Bottom	A,C
17		7101-0531	5	1	Cover, Bottom	B,D
18		7101-0533	7	1	Cover, Top	A,C
18		7101-0530	4	1	Cover, Top	B,D
		0430-0064	9	4	Foot	
		2360-0370	3	14	Screw, 6-32 X .38	
19		4040-1759	8	1	Shield, Controller	A,B
20		7101-0529	1	2	Rail, Side	
		2510-0181	3	8	Screw, 8-32 X .5	
21		3101-0402	5	1	Switch, Power	
22		82901-00001	9	1	Panel, Front	A
22		82901-00002	0	1	Panel, Front	C
22		82902-00001	0	1	Panel, Front	B
22		82902-20002	1	1	Panel, Front	D
23		0380-0643	3	2	Standoff, Hex	A,B
24		1600-0952	6	1	Plate, Cover, Add-on	C,D
25		1600-0964	0	1	Sub-panel	A,C
25		1600-0963	9	1	Sub-panel	B,D

Notes: 1. 82901M Serial Numbers before 2101A09200
2. 82901M Serial Numbers after 2101A09200
3. 82902M Manufactured before 11/82
4. 82902M Manufactured after 11/82

Power Supply Assembly Replace Parts

Reference Designator	CD	HP Part No.	TQ	Description
C1	4	0180-2800	1	C-F: .01UF; 40VDC
C2	5	0160-0576	1	C-F: .1UF; 50VDC
C3	3	0180-0374	1	C-F: 10UF; 20VDC
C4	0	0180-2799	1	C-F: .017UF; 20VDC
C5	5	0160-0576	1	C-F: .1UF; 50VDC
C6	3	0180-0374	1	C-F: 10UF; 20VDC
C7	5	0160-0576	1	C-F: .1UF; 50VDC
C8	5	0160-0576	1	C-F: .1UF; 50VDC
CR1	6	1901-0673	1	Diode: PWR Rectifier
CR2	6	1901-0673	1	Diode: PWR Rectifier
CR3	6	1901-0673	1	Diode: PWR Rectifier
CR4	6	1901-0673	1	Diode: PWR Rectifier
CR5	6	1901-0673	1	Diode: PWR Rectifier
CR6	6	1901-0673	1	Diode: PWR Rectifier
CR7	6	1901-0673	1	Diode: PWR Rectifier
CR8	6	1901-0673	1	Diode: PWR Rectifier
CR9	6	1901-0673	1	Diode: PWR Rectifier
CR10	6	1901-0673	1	Diode: PWR Rectifier
J1	6	1251-5755	1	Connector: 4-Pin; X Former
J2	7	1251-4617	4	Connector: 4-Pin; Power
F1	6	2110-0596	1	Fuse: 3.15A; 250V
F2	6	2110-0596	1	Fuse: 3.15A; 250V
U1	6	1826-0631	1	IC: Regulator
U2	6	1826-0631	1	IC: Regulator
R1	6	0698-3241	1	R-F: 250 OHM; ¼ Watt
R2	9	0699-0024	1	R-F: 2.162K; 1/8 Watt
R3	6	0698-6261	1	R-F: 600 OHM; ¼ Watt
R4	8	0698-7518	1	R-F: 200 OHM; ¼ Watt

Chapter 6
Schematic Diagrams

This Chapter provides schematic and component location diagrams for the 82900 series flexible disc drives.

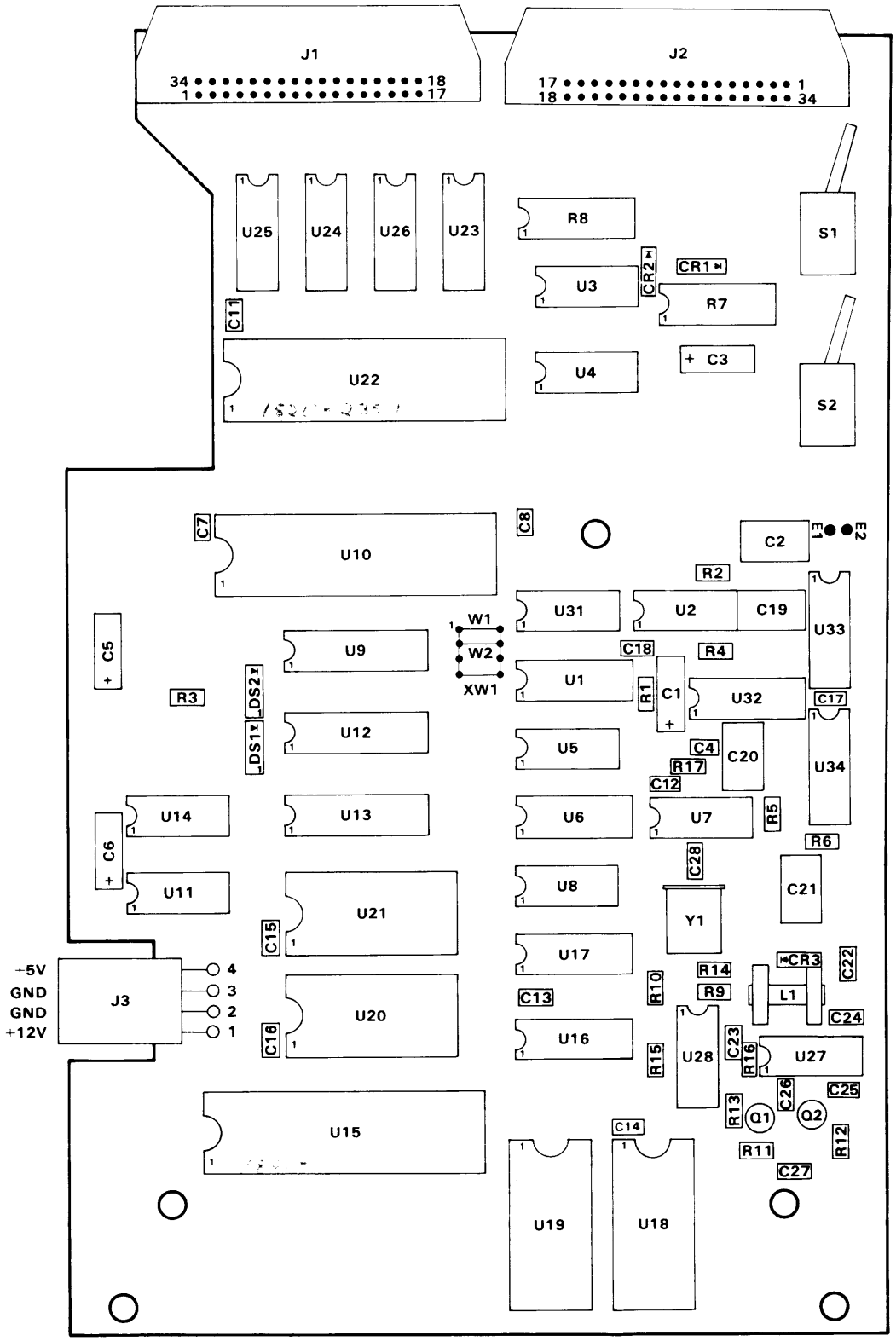
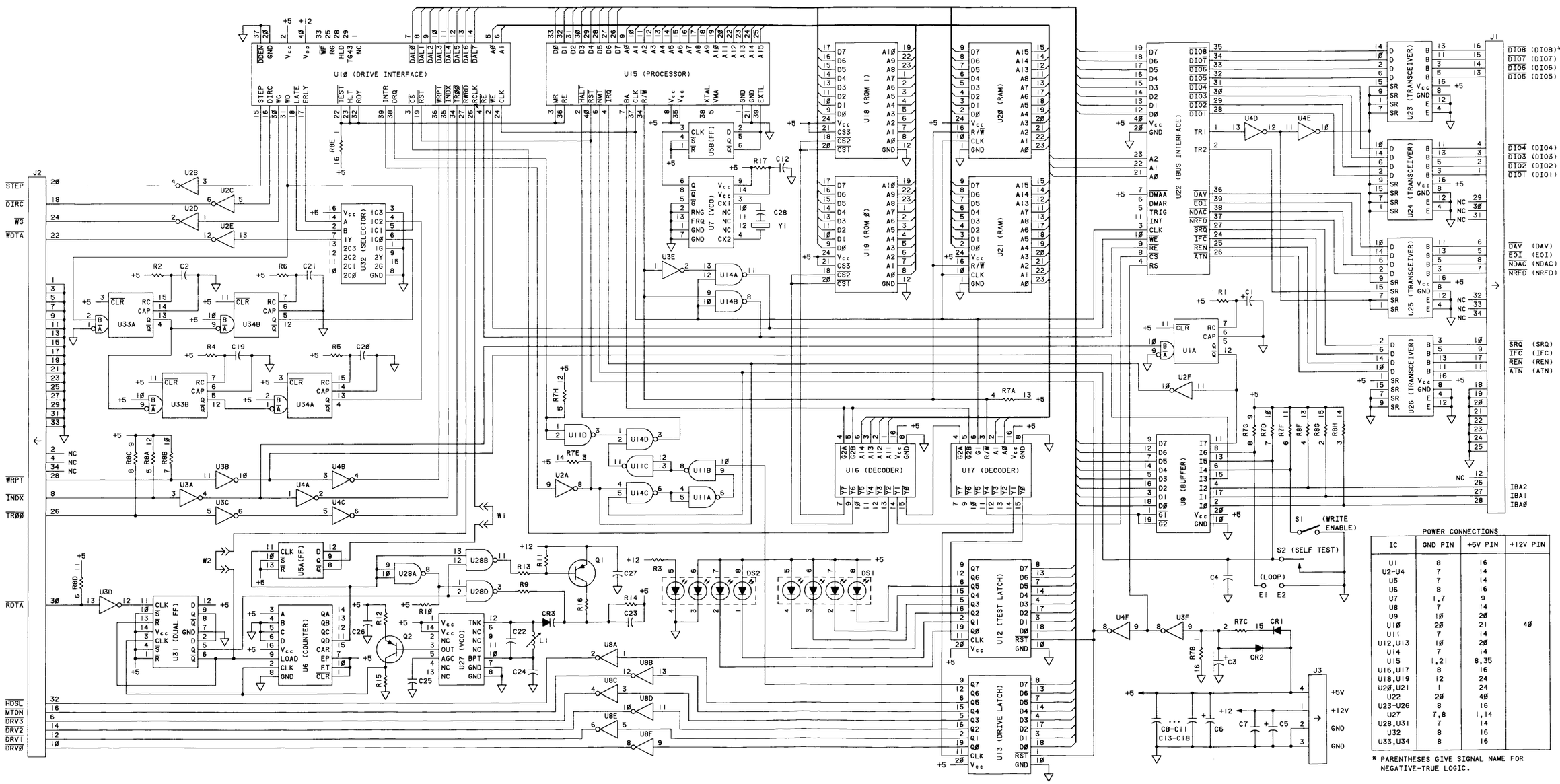


Figure 6-1. Controller PCA Component Location Diagram (P/N 82901-69002)



POWER CONNECTIONS

IC	GND PIN	+5V PIN	+12V PIN
U1	8	16	
U2–U4	7	14	
U5	7	14	
U6	8	16	
U7	1,7	9	
U8	7	14	
U9	1Ø	2Ø	
U1Ø	2Ø	21	4Ø
U11	7	14	
U12,U13	1Ø	2Ø	
U14	7	14	
U15	1,21	8,35	
U16,U17	8	16	
U18,U19	12	24	
U2Ø,U21	1	24	
U22	2Ø	4Ø	
U23–U26	8	16	
U27	7,8	1,14	
U28,U31	7	14	
U32	8	16	
U33,U34	8	16	

* PARENTHESES GIVE SIGNAL NAME FOR NEGATIVE-TRUE LOGIC.

Figure 6-2. Controller PCA Schematic Diagram (P/N 82901-69002)

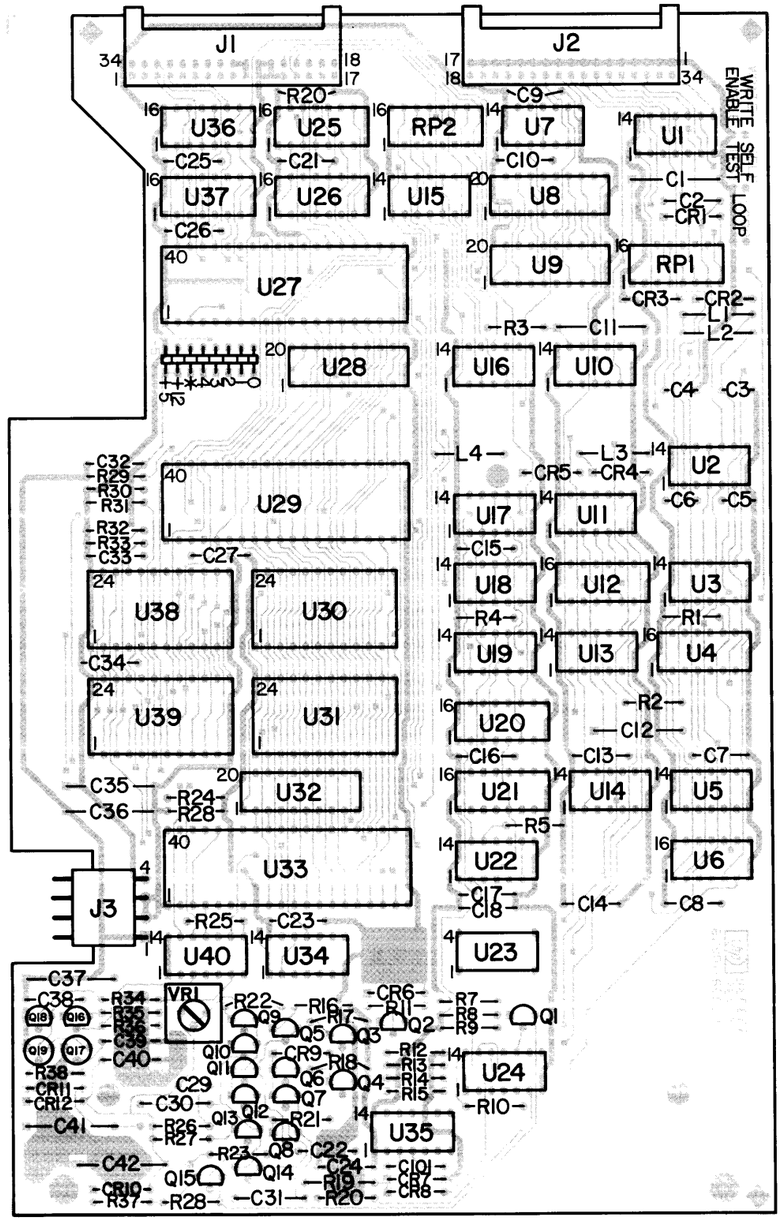


Figure 6-3. Controller PCA Component Location Diagram (P/N 82901-66503)

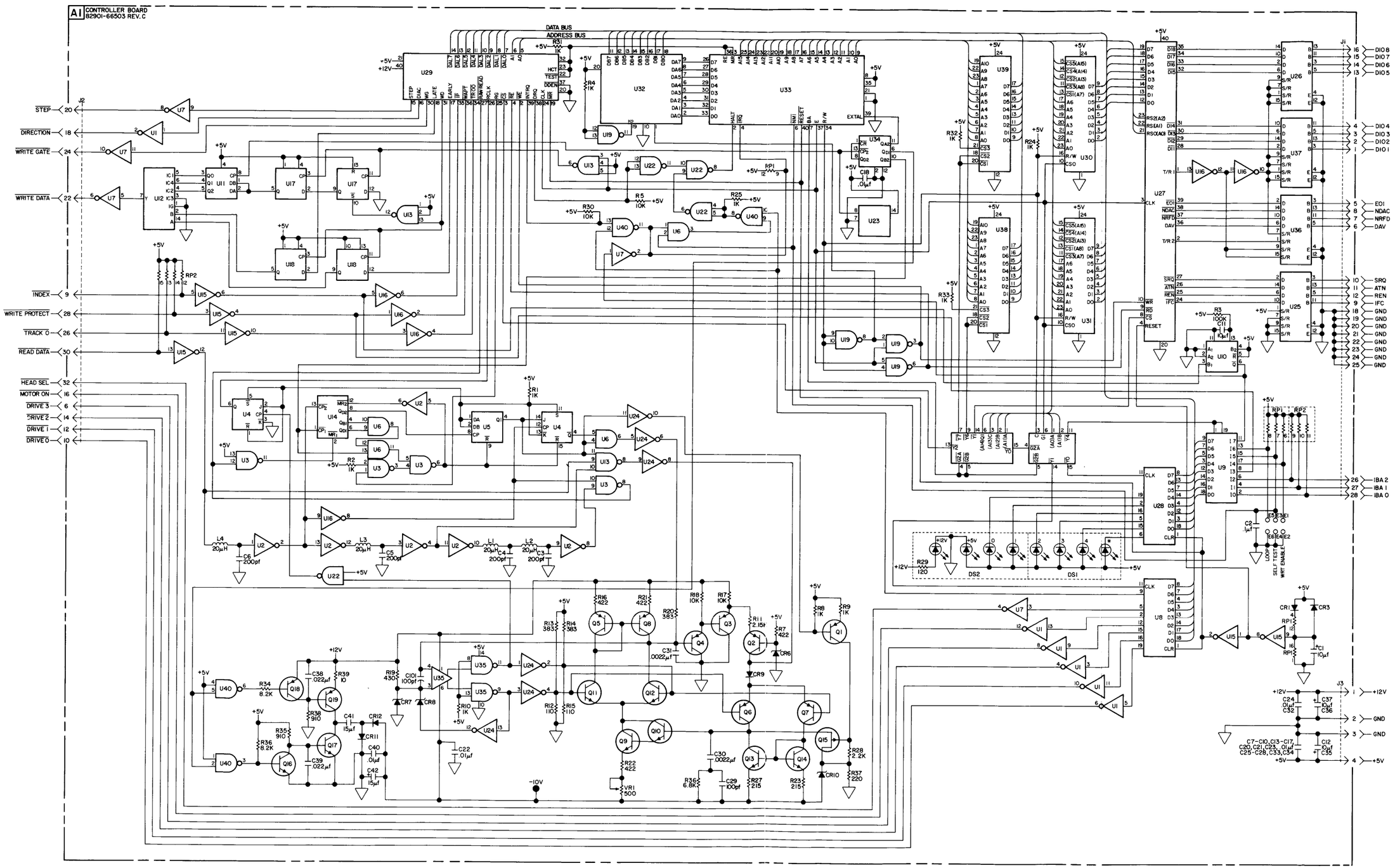


Figure 6-4. Controller PCA Schematic Diagram (P/N 82901-66503)

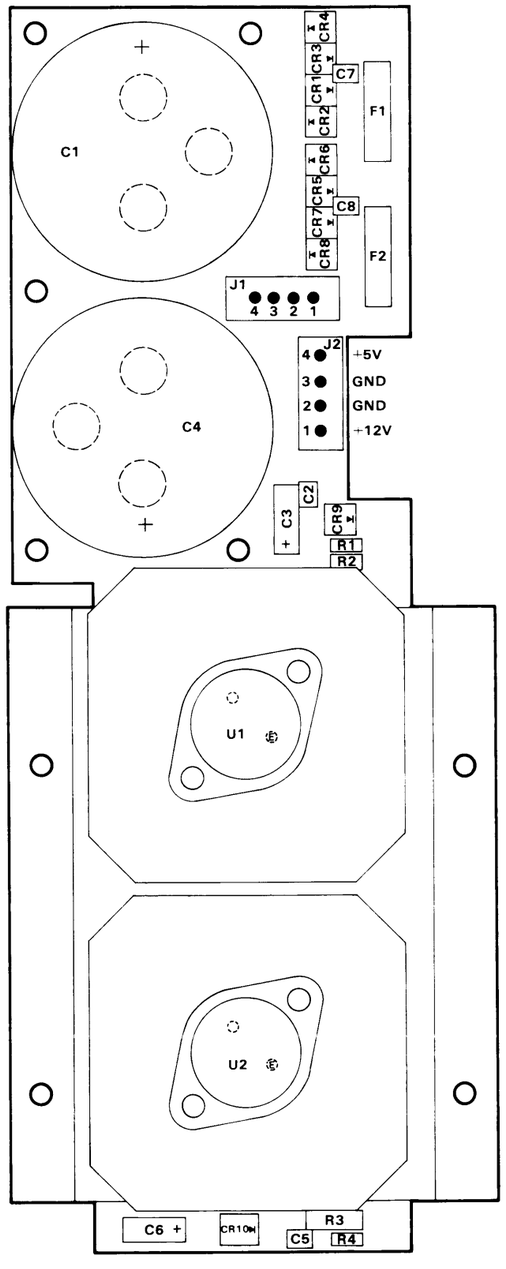


Figure 6-5. Power Supply Component Location Diagram

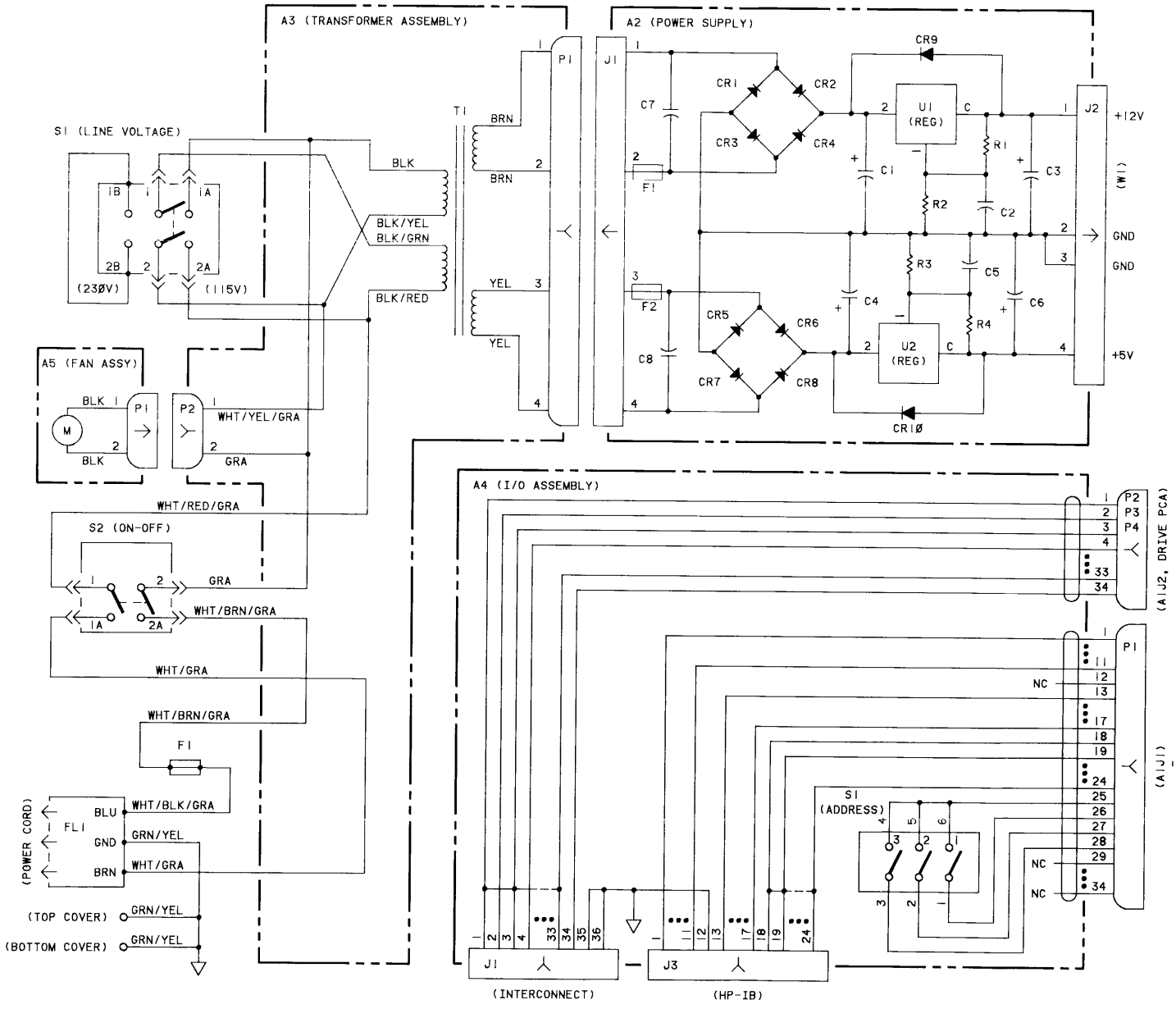


Figure 6-6. Power Supply Schematic Diagram

82901-90031

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